User's Manual

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Renesas RA6M3 Group

User's Manual: Hardware

32-Bit MCU
Renesas Advanced (RA) Family
Renesas RA6 Series

Renesas Electronics
www.renesas.com

Rev.1.10 Dec 2020

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瑞萨电子高级(RA)系列32位MCU
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(Rev.5.0-1 October 2020)

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(Rev.5.0-1 October 2020)

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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

处理微处理单元和微控制器单元的一般注意事项
Products

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1. 防止静电放电(ESD)
   当暴露于CMOS器件时，强电场会导致栅极氧化物的破坏并最终降低器件的运行性能。步骤必须是采取措施，尽可能地阻止静电的产生，并在出现时迅速消散。环境控制必须充分。当它干燥，应使用加湿器。建议避免使用容易产生静电的绝缘体。半导体器件必须是在防静电容器、静电屏蔽袋或导电材料中储存和运输。所有测试和测量工具，包括工作台和地板必须接地。操作员还必须使用腕带接地。不得赤手触摸半导体器件。相似的必须对安装有半导体器件的印刷电路板采取预防措施。
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   specified.
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4. 处理未使用的引脚
   按照手册中未使用引脚处理中给出的说明处理未使用的引脚。CMOS产品的输入引脚一般在高阻抗状态。在未使用的引脚处于开路状态的情况下，在LSI附近会感应出额外的电磁噪声，相关的直通电流在内部流动，并且由于将引脚状态错误识别为输入信号而发生故障成为可能。
5. 时钟信号
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6. 输入引脚的电压施加波形
   由于输入噪声或反射波导致的波形失真可能会导致故障。如果CMOS器件的输入保持在VIL(Max.)和VIH(Min.)由于噪音，例如设备可能发生故障。当输入电平固定时，注意防止抖动噪声进入设备，以及在输入电平通过VIL(Max.)和VIH(Min.)之间的区域时的过渡期。
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   product.

Preface

1. About this Document

This manual is generally organized into an overview of the product, descriptions of the CPU, system control functions, peripheral functions, electrical characteristics, and usage notes. This manual describes the product specification of the microcontroller (MCU) superset. Depending on your product, some pins, registers, or functions might not exist. Address space that store unavailable registers are reserved.

2. Audience

This manual is written for system designers who are designing and programming applications using this MCU. The user is expected to have basic knowledge of electrical circuits, logic circuits, and the MCU.

3. Related documents

Renesas provides the following documents for this MCU.

Document type	Description
Datasheet	Features, overview, and electrical characteristics of the MCU
User's Manual: Hardware	MCU specifications such as pin assignments, memory maps, peripheral functions, electrical characteristics, timing diagrams, and operation descriptions
Application Notes	Technical notes, board design guidelines, and software migration information
Technical Update (TU)	Preliminary reports on product specifications such as restriction and errata

4. Numbering Notation

The following numbering notation is used throughout this manual:

Example	Description
011b	Binary number. For example, the binary equivalent of the number 3 is 011b.
1Fh	Hexadecimal number. For example, the hexadecimal equivalent of the number 31 is described 1Fh. In some cases, a hexadecimal number is shown with the prefix 0x, based on C/C++ formatting.
1234	Decimal number. Decimal numbers are generally shown without a suffix.

Preface

1. 关于本文档

本手册一般由产品概述、CPU说明、系统控制功能、外围功能、电气特性和使用说明组成。本手册描述了微控制器(MCU)超集的产品规格。根据您的产品，某些引脚、寄存器或功能可能不存在。保留存储不可用寄存器的地址空间。

2. Audience

本手册是为使用该MCU设计和编程应用程序的系统设计人员编写的。要求用户具备电路、逻辑电路和MCU的基本知识。

3. 相关文件

瑞萨为此MCU提供了以下文档。

文件类型	Description
Datasheet	MCU的特性、概述和电气特性
User's Manual: Hardware	MCU规范，例如引脚分配、存储器映射、外设功能、电气特性、时序图和操作描述
应用笔记	技术说明、电路板设计指南和软件迁移信息
技术更新(TU)	限制、勘误等产品规格的初步报告

4. 编号符号

本手册通篇使用以下编号符号：

Example	Description
011b	二进制数。例如，数字3的二进制等价物是011b。
1Fh	十六进制数。例如，数字31的十六进制等值表示为1Fh。在某些情况下，根据CC++格式，显示带有前缀0x的十六进制数。
1234	十进制数。十进制数字通常不带后缀。

5. Typographic Notation

The following typographic notation is used throughout this manual:

Example	Description
ICU.NMICR.NMIMD	Periods separate a function module symbol (ICU), register symbol (NMICR), and bit field symbol (NMIMD)
ICU.NMICR	A period separates a function module symbol (ICU) and register symbol (NMICR)
NMICR.NMIMD	A period separates a register symbol (NMICR) and bit field symbol (NMIMD)
NFCLKSEL[1:0]	In a register bit name, the bit range enclosed in square brackets indicates the number of bits in the field at this location. In this example, NFCLKSEL[1:0] represents a 2-bit field at the specified location in the NMI Pin Interrupt Control Register (NMICR).

6. Unit Prefix

The following unit prefixes are sometimes misleading. Those unit prefixes are described throughout this manual with the following meaning:

Prefix	Description
b	Bit
B	Byte. This unit prefix is generally used for memory specification of the MCU and address space.
k	1000 = 10^3. k is also used to denote 1024 (2^{10}) but this unit prefix is used to denote 1000 (10^3) throughout this manual.
K	1024 = 2^{10}. This unit prefix is used to denote 1024 (2^{10}) not 1000 (10^3) throughout this manual.

7. Special Terms

The following terms have special meanings:

Term	Description
NC	Not connected pin. NC means the pin is not connected to the MCU.
Hi-Z	High impedance

5. 排版符号

本手册通篇使用以下印刷符号：

Example	Description
ICU.NMICR.NMIMD	句点分隔功能模块符号(ICU)、寄存器符号(NMICR)和位域符号(NMIMD)
ICU.NMICR	句点分隔功能模块符号(ICU)和寄存器符号(NMICR)
NMICR.NMIMD	句点分隔寄存器符号(NMICR)和位域符号(NMIMD)
NFCLKSEL[1:0]	在寄存器位名称中，方括号中的位范围表示该位置的字段中的位数。在本例中，NFCLKSEL[1:0]表示NMI引脚中断控制寄存器(NMICR)中指定位置的2位字段。

6. 单位前缀

以下单位前缀有时会产生误导。这些单位前缀在本手册中进行了描述，含义如下：

Prefix	Description
b	Bit
B	字节。该单元前缀一般用于MCU的内存规范和地址空间。
k	1000=103。k也用于表示1024(210)，但在本手册中，此单位前缀用于表示1000(103)。
K	1024=210。在本手册中，该单位前缀用于表示1024(210)而不是1000(103)。

7. 特别条款

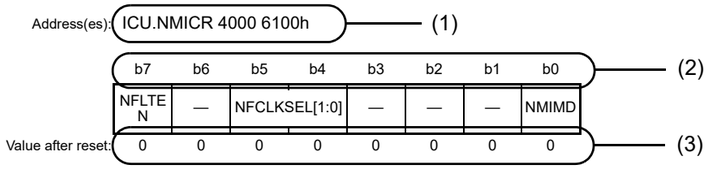
以下术语具有特殊含义：

Term	Description
NC	未连接引脚。NC表示该引脚未连接到MCU。
Hi-Z	高阻抗

8. Register Description

Each register description includes both a register diagram that shows the bit assignments and a register bit table that describes the content of each bit. The example of symbols used in these tables are described in the sections that follow. The following is an example of a register description and associated bit field definition.

X.X.X NMI Pin Interrupt Control Register (NMICR)



(4) (5) (6)

Bit	Symbol	Bit name	Description	R/W
b0	NMIMD	NMI Detection Set	0: Falling edge 1: Rising edge.	R/W
b3 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b5, b4	NFCLKSEL[1:0]	NMI Digital Filter Sampling Clock Select	b5 b4 0 0: PCLKB 0 1: PCLKB/8 1 0: PCLKB/32 1 1: PCLKB/64.	R/W
b6	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b7	NFLTEN	NMI Digital Filter Enable	0: Disable the digital filter 1: Enable the digital filter.	R/W

(1) Function module symbol, register symbol, and address assignment

Function module symbol, register symbol, and address assignment of this register are generally expressed. ICU.NMICR 4000 6100h means NMI Pin Interrupt Control Register (NMICR) of Interrupt Controller Unit (ICU) is assigned to address 4000 6100h.

(2) Bit number

This number indicates the bit number. These bits are shown in order from b31 to b0 for a 32-bit register, from b15 to b0 for a 16-bit register, and from b7 to b0 for an 8-bit register.

(3) Value after reset

This symbol or number indicates the value of each bit after a reset. The value is shown in binary unless specified otherwise.
0: Indicates that the value is 0 after a reset.
1: Indicates that the value is 1 after a reset.
x: Indicates that the value is undefined after a reset.

(4) Bit symbol

Bit symbol indicates the short name of the bit field. Reserved bit is expressed with a —.

(5) Bit name

Bit name indicates the full name of the bit field.

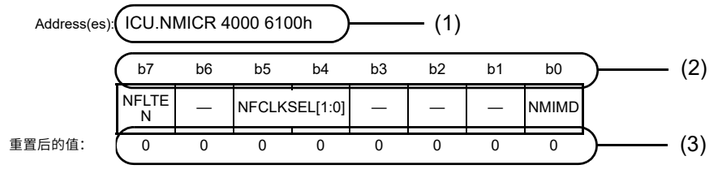
(6) R/W

The R/W column indicates access type: whether the bit field is read or write.
R/W: The bit field is read and write.
R/(W): The bit field is read and write. But writing to this bit field has some limitations. For details on the limitations, see the description or notes of respective registers.
R: The bit field is read-only. Writing to this bit field has no effect.
W: The bit field is write-only. The read value is undefined.

8. 注册说明

每个寄存器描述都包括一个显示位分配的寄存器图和一个描述每个位内容的寄存器位表。这些表中使用的符号示例将在以下部分中描述。以下是寄存器描述和相关位字段定义的示例。

X.X.X NMI引脚中断控制寄存器(NMICR)



(4) (5) (6)

Bit	Symbol	位名称	Description	R/W
b0	NMIMD	NMI检测集	0：下降沿1： 上升沿。	R/W
b3 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b5, b4	NFCLKSEL[1:0]	NMI数字滤波器采样时钟 Select	b5 b4 0 0: PCLKB 0 1: PCLKB/8 1 0: PCLKB/32 1 1: PCLKB/64.	R/W
b6	—	Reserved	该位读取为0。写入值应为0。	R/W
b7	NFLTEN	NMI数字滤波器启用	0：禁用数字滤波器1：启 用数字滤波器。	R/W

(1) 功能模块符号、寄存器符号、地址分配

一般表示该寄存器的功能模块符号、寄存器符号、地址分配。ICU.NMICR40006100h表示中断控制器单元(ICU)的NMI引脚中断控制寄存器(NMICR)分配到地址40006100h。

(2) 位号

该数字表示位数。对于32位寄存器，这些位按照从b31到b0的顺序显示，对于16位寄存器，这些位从b15到b0，对于8位寄存器，按照从b7到b0的顺序显示。

(3) 重置后的值

该符号或数字表示复位后每个位的值。除非另有说明，否则该值以二进制显示。0：表示复位后值为0。
1：表示复位后值为1。x：表示复位后该值未定义。

(4) 位符号

位符号表示位域的简称。保留位用—表示。

(5) 位名称

位名表示位域的全称。

(6) R/W

RW列表示访问类型：位域是读还是写。
RW：位域可读写。
R(W)：位域可读写。但是写入这个位域有一些限制。有关限制的详细信息，请参见各个寄存器的说明或注释。R：位域是只读的。写入该位域无效。

W：位域是只写的。读取值未定义。

9. Abbreviations

Abbreviations used in this manual are shown in the following table:

Abbreviation	Description
AES	Advanced Encryption Standard
AHB	Advanced High-Performance Bus
AHB-AP	AHB Access Port
APB	Advanced Peripheral Bus
ARC	Alleged RC
ATB	Advanced Trace Bus
BCD	Binary Coded Decimal
BSDL	Boundary Scan Description Language
DES	Data Encryption Standard
DSA	Digital Signature Algorithm
ECC	Elliptic Curve Cryptography
ETB	Embedded Trace Buffer
ETM	Embedded Trace Macrocell
FLL	Frequency Locked Loop
FPU	Floating-Point Unit
GSM	Global System for Mobile communications
HMI	Human Machine Interface
IrDA	Infrared Data Association
LSB	Least Significant Bit
MSB	Most Significant Bit
NVIC	Nested Vector Interrupt Controller
PC	Program Counter
PFS	Port Function Select
PLL	Phase Locked Loop
POR	Power-On Reset
PWM	Pulse Width Modulation
RSA	Rivest Shamir Adleman
SHA	Secure Hash Algorithm
S/H	Sample and Hold
SP	Stack Pointer
SWD	Serial Wire Debug
SW-DP	Serial Wire-Debug Port
TRNG	True Random Number Generator
UART	Universal Asynchronous Receiver/Transmitter

9. Abbreviations

本手册中使用的缩写如下表所示：

Abbreviation	Description
AES	高级加密标准
AHB	先进的高性能总线
AHB-AP	AHB访问端口
APB	先进的外围总线
ARC	Alleged RC
ATB	高级跟踪总线
BCD	二进制编码的十进制
BSDL	边界扫描描述语言
DES	数据加密标准
DSA	数字签名算法
ECC	椭圆曲线密码学
ETB	嵌入式跟踪缓冲区
ETM	嵌入式跟踪宏单元
FLL	锁频环
FPU	Floating-Point Unit
GSM	全球移动通信系统
HMI	人机接口
IrDA	红外数据协会
LSB	最低有效位
MSB	最高有效位
NVIC	嵌套向量中断控制器
PC	程序计数器
PFS	端口功能选择
PLL	锁相环
POR	Power-On Reset
PWM	脉冲宽度调制
RSA	Rivest Shamir Adleman
SHA	安全哈希算法
S/H	采样和保持
SP	堆栈指针
SWD	串口线调试
SW-DP	串行线调试端口
TRNG	真随机数发生器
UART	通用异步收发器

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RA6M3 Group

User's Manual

Leading performance 120-MHz Arm® Cortex®-M4 core, up to 2-MB code flash memory, 640-KB SRAM, Graphics LCD Controller, 2D Drawing Engine, Capacitive Touch Sensing Unit, Ethernet MAC Controller with IEEE 1588 PTP, USB 2.0 High-Speed, USB 2.0 Full-Speed, SDHI, Quad SPI, security and safety features, and advanced analog.

Features

■ Arm Cortex-M4 Core with Floating Point Unit (FPU)
- Armv7E-M architecture with DSP instruction set
- Maximum operating frequency: 120 MHz
- Support for 4-GB address space
- On-chip debugging system: JTAG, SWD, and ETM
- Boundary scan and Arm Memory Protection Unit (Arm MPU)

■ Memory
- Up to 2-MB code flash memory (40 MHz zero wait states)
- 64-KB data flash memory (125,000 erase/write cycles)
- Up to 640-KB SRAM
- Flash Cache (FCACHE)
- Memory Protection Units (MPU)
- Memory Mirror Function (MMF)
- 128-bit unique ID

■ Connectivity
- Ethernet MAC Controller (ETHERC)
- Ethernet DMA Controller (EDMAC)
- Ethernet PTP Controller (EPTPC)
- USB 2.0 High-Speed (USBHS) module
  - On-chip transceiver with voltage regulator
  - Compliant with USB Battery Charging Specification 1.2
- USB 2.0 Full-Speed (USBFS) module
  - On-chip transceiver with voltage regulator
- Serial Communications Interface (SCI) with FIFO × 10
- Serial Peripheral Interface (SPI) × 2
- I^2C bus interface (IIC) × 3
- Controller Area Network (CAN) × 2
- Serial Sound Interface Enhanced (SSIE) × 2
- SD/MMC Host Interface (SDHI) × 2
- Quad Serial Peripheral Interface (QSPI)
- IrDA interface
- Sampling Rate Converter (SRC)
- External address space
  - 8-bit or 16-bit bus space is selectable per area
  - SDRAM support

■ Analog
- 12-bit A/D Converter (ADC12) with 3 sample-and-hold circuits each × 2
- 12-bit D/A Converter (DAC12) × 2
- High-Speed Analog Comparator (ACMPHS) × 6
- Programmable Gain Amplifier (PGA) × 6
- Temperature Sensor (TSN)

■ Timers
- General PWM Timer 32-bit Enhanced High Resolution (GPT32EH) × 4
- General PWM Timer 32-bit Enhanced (GPT32E) × 4
- General PWM Timer 32-bit (GPT32) × 6
- Asynchronous General-Purpose Timer (AGT) × 2
- Watchdog Timer (WDT)

■ Safety
- Error Correction Code (ECC) in SRAM
- SRAM parity error check
- Flash area protection
- ADC self-diagnosis function
- Clock Frequency Accuracy Measurement Circuit (CAC)
- Cyclic Redundancy Check (CRC) calculator
- Data Operation Circuit (DOC)
- Port Output Enable for GPT (POEG)
- Independent Watchdog Timer (IWDT)
- GPIO readback level detection
- Register write protection
- Main oscillator stop detection
- Illegal memory access

■ System and Power Management
- Low power modes
- Realtime Clock (RTC) with calendar and VBATT support
- Event Link Controller (ELC)
- DMA Controller (DMAC) × 8
- Data Transfer Controller (DTC)
- Key Interrupt Function (KINT)
- Power-on reset
- Low Voltage Detection (LVD) with voltage settings

■ Security and Encryption
- AES128/192/256
- 3DES/ARC4
- SHA1/SHA224/SHA256/MD5
- GHASH
- RSA/DSA/ECC
- True Random Number Generator (TRNG)

■ Human Machine Interface (HMI)
- Graphics LCD Controller (GLCDC)
- JPEG codec
- 2D Drawing Engine (DRW)
- Capacitive Touch Sensing Unit (CTSU)
- Parallel Data Capture Unit (PDC)

■ Multiple Clock Sources
- Main clock oscillator (MOSC) (8 to 24 MHz)
- Sub-clock oscillator (SOSC) (32.768 kHz)
- High-speed on-chip oscillator (HOCO) (16/18/20 MHz)
- Middle-speed on-chip oscillator (MOCO) (8 MHz)
- Low-speed on-chip oscillator (LOCO) (32.768 kHz)
- IWDT-dedicated on-chip oscillator (15 kHz)
- Clock trim function for HOCO/MOCO/LOCO
- Clock out support

■ General-Purpose I/O Ports
- Up to 133 input/output pins
  - Up to 9 CMOS input
  - Up to 124 CMOS input/output
    - Up to 21 input/output 5 V tolerant
    - Up to 18 high current (20 mA)

■ Operating Voltage
- VCC: 2.7 to 3.6 V

■ Operating Temperature and Packages
- Ta = -40°C to +85°C
  - 176-pin BGA (13 mm × 13 mm, 0.8 mm pitch)
  - 145-pin LGA (7 mm × 7 mm, 0.5 mm pitch)
- Ta = -40°C to +105°C
  - 176-pin LQFP (24 mm × 24 mm, 0.5 mm pitch)
  - 144-pin LQFP (20 mm × 20 mm, 0.5 mm pitch)
  - 100-pin LQFP (14 mm × 14 mm, 0.5 mm pitch)

RA6M3 Group

User's Manual

领先的性能120-MHzArm®Cortex®-M4内核、高达2-MB代码闪存、640-KBSRAM、图形LCD控制器、2D绘图引擎、电容式触摸传感单元、具有IEEE1588PTP、USB2.0的以太网MAC控制器

高速、USB2.0全速、SDHI、QuadSPI、安全和安全功能以及高级模拟。

Features

■带浮点单元(FPU)的ArmCortex-M4内核带DSP指令集的Armv7E-M架构最大工作频率：120MHz支持4GB地址空间片上调试系统：JTAG、SWD和ETM　边界扫描和Arm内存保护单元(ArmMPU)

■系统和电源管理　低功耗模式　支持日历和VBATT的实时时钟(RTC)　事件链接控制器(ELC)　DMA控制器(DMAC)×8　数据传输控制器(DTC)　按键中断功能(KINT)　上电复位　具有电压设置的低电压检测(LVD)

■ Memory
高达2MB代码闪存（40MHz零等待状态）　64KB数据闪存（125 000个擦除写入周期）　高达640KBSRAM　闪存高速缓存(FCACHE)　内存保护单元(MPU)　内存镜像功能(MMF)　128位唯一ID

■安全和加密　AES128192256　3DESARC4　SHA1SHA224SHA256MD5　GHASH　RSADSAECC　真随机数生成器(TRNG)

■ Connectivity
以太网MAC控制器(ETHERC)　以太网DMA控制器(EDMAC)　以太网PTP控制器(EPTPC)　USB2.0高速(USBHS)模块

带有稳压器的片上收发器符合USB电池充电规范1.2　USB2.0全速(USBFS)模块

带稳压器的片上收发器带FIFO的串行通信接口(SCI)×10串行外设接口(SPI)×2I2C总线接口(IIC)×3控制器局域网(CAN)×2串行声音增强型接口(SSIE)×2　SDMMC主机接口(SDHI)×2　四路串行外设接口(QSPI)　IrDA接口　采样率转换器(SRC)　外部地址空间

■人机界面(HMI)　图形LCD控制器(GLCDC)　JPEG编解码器　2D绘图引擎(DRW)　电容式触摸传感单元(CTSU)　并行数据采集单元(PDC)

■多个时钟源

主时钟振荡器(MOSC)(8至24MHz)　副时钟振荡器(SOSC)(32.768kHz)　高速片上振荡器(HOCO)(161820MHz)　中速片上振荡器(MOCO)(8MHz)　低速片上振荡器(LOCO)(32.768kHz)　IWDT专用片上振荡器(15kHz)　HOCOMOCOLOCO的时钟微调功能　时钟输出支持

每个区域可选择8位或16位总线空间SDRAM支持

■通用IO端口　多达133个输入输出引脚
多达9个CMOS输入多达124个CMOS输入输出多达21个输入输出5V耐受多达18个高电流(20mA)

■ Analog
12位模数转换器(ADC12)，每个具有3个采样和保持电路×2　12位模数转换器(DAC12)×2　高速模拟比较器(ACMPHS)×6　可编程增益放大器(PGA)×6　温度传感器(TSN)

■工作电压　VCC：2.7至3.6V

■工作温度和封装　Ta=−40°C至+85°C

■ Timers
通用PWM定时器32位增强型高分辨率(GPT32EH)×4　通用PWM定时器32位(GPT32E)×4　通用PWM定时器32位(GPT32)×6　异步通用定时器(AGT)×2　看门狗定时器(WDT)

176引脚BGA（13毫米×13毫米，0.8毫米间距）145引脚LGA（7毫米×7毫米，0.5毫米间距）　Ta=−40°C至+105°C
- 176-pin LQFP (24 mm × 24 mm, 0.5 mm pitch)
- 144-pin LQFP (20 mm × 20 mm, 0.5 mm pitch)
- 100-pin LQFP (14 mm × 14 mm, 0.5 mm pitch)

■ Safety
SRAM中的纠错码(ECC)　SRAM奇偶校验错误检查　闪存区域保护　ADC自诊断功能　时钟频率精度测量电路(CAC)　循环冗余校验(CRC)计算器　数据操作电路(DOC)　端口GPT(POEG)的输出使能　独立看门狗定时器(IWDT)　GPIO回读电平检测　寄存器写保护　主振荡器停止检测　非法内存访问

1. Overview

The MCU integrates multiple series of software- and pin-compatible Arm®-based 32-bit cores that share the same set of Renesas peripherals to facilitate design scalability and efficient platform-based product development.

The MCU in this series incorporates a high-performance Arm Cortex®-M4 core running up to 120 MHz, with the following features:

- Up to 2-MB code flash memory
- 640-KB SRAM
- Graphics LCD Controller (GLCDC)
- 2D Drawing Engine (DRW)
- Capacitive Touch Sensing Unit (CTSU)
- Ethernet MAC Controller (ETHERC) with IEEE 1588 PTP, USBFS, USBHS, SD/MMC Host Interface
- Quad Serial Peripheral Interface (QSPI)
- Security and safety features
- Analog peripherals.

1.1 Function Outline

Table 1.1 Arm core

Feature	Functional description
Arm Cortex-M4 core	• Maximum operating frequency: up to 120 MHz • Arm Cortex-M4 core: - Revision: r0p1-01rel0 - ARMv7E-M architecture profile - Single precision floating-point unit compliant with the ANSI/IEEE Std 754-2008. • Arm Memory Protection Unit (Arm MPU): - ARMv7 Protected Memory System Architecture - 8 protect regions. • SysTick timer: - Driven by SYSTICCLK (LOCO) or ICLK.

Table 1.2 Memory

Feature	Functional description
Code flash memory	Maximum 2-MB code flash memory. See section 55, Flash Memory.
Data flash memory	64-KB data flash memory. See section 55, Flash Memory.
Memory Mirror Function (MMF)	The Memory Mirror Function (MMF) can be configured to mirror the target application image load address in code flash memory to the application image link address in the 23-bit unused memory space (memory mirror space addresses). Your application code is developed and linked to run from this MMF destination address. The application code does not need to know the load location where it is stored in code flash memory. See section 5, Memory Mirror Function (MMF).
Option-setting memory	The option-setting memory determines the state of the MCU after a reset. See section 7, Option-Setting Memory.
SRAM	On-chip high-speed SRAM with either parity-bit or Error Correction Code (ECC). The first 32 KB in SRAM0 provides error correction capability using ECC. Parity check is performed for other areas. See section 53, SRAM.
Standby SRAM	On-chip SRAM that can retain data in Deep Software Standby mode. See section 54, Standby SRAM.

1. Overview

MCU集成了多个系列的软件和基于Arm®引脚兼容的32位内核，它们共享同一组瑞萨外围设备可促进设计可扩展性和高效的基于平台的产品开发。

该系列中的MCU包含一个运行频率高达120MHz的高性能ArmCortex®-M4内核，具有以下特性：

- 高达2MB的代码闪存
- 640-KB SRAM
- 图形LCD控制器(GLCDC)
- 2D绘图引擎(DRW)
- 电容式触控感应单元(CTSU)
- 具有IEEE1588PTP、USBFS、USBHS、SDMMC主机接口的以太网MAC控制器(ETHERC)
- 四路串行外设接口(QSPI)
- 安全和安全功能
- 模拟外设。

1.1 功能概要

Table 1.1 臂芯

Feature	功能说明
ArmCortex-M4内核	最大工作频率：高达120MHz ArmCortex-M4内核：修订版：r0p1-01rel0ARMv7E-M架构配置文件符合ANSIIEEEStd754-2008的单精度浮点单元。 Arm内存保护单元（ArmMPU）： ARMv7ProtectedMemorySystemArchitecture8保护区域。 SysTick计时器： 由SYSTICCLK(LOCO)或ICLK驱动。

Table 1.2 Memory

Feature	功能说明
代码闪存	最大2MB代码闪存。请参阅第55节，闪存。
数据闪存	64KB数据闪存。请参阅第55节，闪存。
内存镜像功能(MMF)	内存镜像功能(MMF)可配置为将代码闪存中的目标应用程序映像加载地址镜像到23位未使用的内存空间（内存镜像空间地址）中的应用程序映像链接地址。您的应用程序代码已开发并链接到从该MMF目标地址运行。应用程序代码不需要知道它存储在代码闪存中的加载位置。请参阅第5节，内存镜像功能(MMF)。
Option-setting memory	选项设置存储器确定复位后MCU的状态。见第7节，Option-Setting Memory.
SRAM	具有奇偶校验位或纠错码(ECC)的片上高速SRAM。SRAM0中的前32KB使用ECC提供纠错能力。对其他区域执行奇偶校验。参见第53节，SRAM。
Standby SRAM	可以在深度软件待机模式下保留数据的片上SRAM。见第54节，备用SRAM.

Table 1.3 System (1 of 2)

Feature	Functional description
Operating modes	Two operating modes: - Single-chip mode - SCI or USB boot mode. See section 3, Operating Modes.
Resets	14 resets: • RES pin reset • Power-on reset • Voltage monitor 0 reset • Voltage monitor 1 reset • Voltage monitor 2 reset • Independent watchdog timer reset • Watchdog timer reset • Deep software standby reset • SRAM parity error reset • SRAM ECC error reset • Bus master MPU error reset • Bus slave MPU error reset • Stack pointer error reset • Software reset. See section 6, Resets.
Low Voltage Detection (LVD)	The Low Voltage Detection (LVD) function monitors the voltage level input to the VCC pin, and the detection level can be selected using a software program. See section 8, Low Voltage Detection (LVD).
Clocks	• Main clock oscillator (MOSC) • Sub-clock oscillator (SOSC) • High-speed on-chip oscillator (HOCO) • Middle-speed on-chip oscillator (MOCO) • Low-speed on-chip oscillator (LOCO) • PLL frequency synthesizer • IWDT-dedicated on-chip oscillator • Clock out support. See section 9, Clock Generation Circuit.
Clock Frequency Accuracy Measurement Circuit (CAC)	The Clock Frequency Accuracy Measurement Circuit (CAC) counts pulses of the clock to be measured (measurement target clock) within the time generated by the clock to be used as a measurement reference (measurement reference clock), and determines the accuracy depending on whether the number of pulses is within the allowable range. When measurement is complete or the number of pulses within the time generated by the measurement reference clock is not within the allowable range, an interrupt request is generated. See section 10, Clock Frequency Accuracy Measurement Circuit (CAC).
Interrupt Controller Unit (ICU)	The Interrupt Controller Unit (ICU) controls which event signals are linked to the NVIC/DTC module and DMAC module. The ICU also controls NMI interrupts. See section 14, Interrupt Controller Unit (ICU).
Key Interrupt Function (KINT)	A key interrupt can be generated by setting the Key Return Mode Register (KRM) and inputting a rising or falling edge to the key interrupt input pins. See section 21, Key Interrupt Function (KINT).
Low power modes	Power consumption can be reduced in multiple ways, such as by setting clock dividers, controlling EBCLK output, controlling SDCLK output, stopping modules, selecting power control mode in normal operation, and transitioning to low power modes. See section 11, Low Power Modes.
Battery backup function	A battery backup function is provided for partial powering by a battery. The battery-powered area includes the RTC, SOSC, backup memory, and switch between VCC and VBATT. See section 12, Battery Backup Function.
Register write protection	The register write protection function protects important registers from being overwritten because of software errors. See section 13, Register Write Protection.
Memory Protection Unit (MPU)	Four Memory Protection Units (MPUs) and a CPU stack pointer monitor function are provided for memory protection. See section 16, Memory Protection Unit (MPU).

Table 1.3 系统(1of2)

Feature	功能说明
操作模式	两种工作模式：单片机模式SCI或USB启动模式。请参阅第3节，操作模式。
Resets	14次复位： RES引脚复位 上电复位 电压监控器0复位 电压监控器1复位 电压监控器2复位 独立看门狗定时器复位 看门狗定时器复位 深度软件待机复位 SRAM奇偶校验错误复位 SRAMEC C错误复位 总线主MPU错误复位 总线从属MPU错误复位 堆栈指针错误复位 软件复位。请参阅第6节，重置。
低电压检测(LVD)	低电压检测(LVD)功能监控输入到VCC引脚的电压电平，并且可以使用软件程序选择检测电平。请参见第8节，低电压检测(LVD)。
Clocks	主时钟振荡器(MOSC) 子时钟振荡器(SOSC) 高速片上振荡器(HOCO) 中速片上振荡器(MOCO) 低速片上振荡器(LOCO) PLL频率合成器 IWDT专用片上振荡器 时钟输出支持。请参见第9节，时钟生成电路。
时钟频率精度测量电路(CAC)	时钟频率精度测量电路(CAC)在用作测量基准的时钟（测量基准时钟）生成的时间内对要测量的时钟（测量目标时钟）的脉冲进行计数，并根据是否脉冲数在允许范围内。当测量完成或测量参考时钟在时间内产生的脉冲数不在允许范围内时，将产生中断请求。请参见第10节，时钟频率精度测量电路(CAC)。
中断控制器单元(ICU)	中断控制器单元(ICU)控制哪些事件信号链接到NVICDTC模块和DMAC模块。ICU还控制NMI中断。参见第14节，中断控制器单元(ICU)。
按键中断功能(KINT)	通过设置按键返回模式寄存器(KRM)并向按键中断输入引脚输入上升沿或下降沿，可以生成按键中断。请参见第21节，按键中断功能(KINT)。
低功耗模式	可以通过多种方式降低功耗，例如通过设置时钟分频器、控制EBCLK输出、控制SDCLK 输出、停止模块、在正常操作中选择电源控制模式以及转换到低功耗模式。请参见第11节，低功耗模式。
电池备份功能	提供电池备份功能，由电池部分供电。电池供电区域包括RTC、SOSC、备份存储器以及VCC和VBATT之间的切换。请参阅第12节，电池备份功能。
寄存器写保护	寄存器写保护功能可保护重要寄存器不因软件错误而被覆盖。请参见第13节，寄存器写保护。
内存保护单元(MPU)	提供四个内存保护单元(MPU)和一个CPU堆栈指针监控功能用于内存保护。请参阅第16节，内存保护单元(MPU)。

Table 1.3 System (2 of 2)

Feature	Functional description
Watchdog Timer (WDT)	The Watchdog Timer (WDT) is a 14-bit down-counter that can be used to reset the MCU when the counter underflows because the system has run out of control and is unable to refresh the WDT. In addition, a non-maskable interrupt or interrupt can be generated by an underflow. A refresh-permitted period can be set to refresh the counter and be used as the condition for detecting when the system runs out of control. See section 27, Watchdog Timer (WDT).
Independent Watchdog Timer (IWDT)	The Independent Watchdog Timer (IWDT) consists of a 14-bit down-counter that must be serviced periodically to prevent counter underflow. It can be used to reset the MCU or to generate a non-maskable interrupt or interrupt for a timer underflow. Because the timer operates with an independent, dedicated clock source, it is particularly useful in returning the MCU to a known state as a fail safe mechanism when the system runs out of control. The IWDT can be triggered automatically on a reset, underflow, refresh error, or by a refresh of the count value in the registers. See section 28, Independent Watchdog Timer (IWDT).

Table 1.4 Event link

Feature	Functional description
Event Link Controller (ELC)	The Event Link Controller (ELC) uses the interrupt requests generated by various peripheral modules as event signals to connect them to different modules, enabling direct interaction between the modules without CPU intervention. See section 19, Event Link Controller (ELC).

Table 1.5 Direct memory access

Feature	Functional description
Data Transfer Controller (DTC)	A Data Transfer Controller (DTC) module is provided for transferring data when activated by an interrupt request. See section 18, Data Transfer Controller (DTC).
DMA Controller (DMAC)	An 8-channel DMA Controller (DMAC) module is provided for transferring data without the CPU. When a DMA transfer request is generated, the DMAC transfers data stored at the transfer source address to the transfer destination address. See section 17, DMA Controller (DMAC).

Table 1.6 External bus interface

Feature	Functional description
External buses	• CS area (EXBIU): Connected to the external devices (external memory interface) • SDRAM area (EXBIU): Connected to the SDRAM (external memory interface) • QSPI area (EXBIUT2): Connected to the QSPI (external device interface).

Table 1.7 Timers

Feature	Functional description
General PWM Timer (GPT)	The General PWM Timer (GPT) is a 32-bit timer with 14 channels. PWM waveforms can be generated by controlling the up-counter, down-counter, or the up- and down-counter. In addition, PWM waveforms can be generated for controlling brushless DC motors. The GPT can also be used as a general-purpose timer. See section 23, General PWM Timer (GPT).
Port Output Enable for GPT (POEG)	Use the Port Output Enable for GPT (POEG) function to place the General PWM Timer (GPT) output pins in the output disable state. See section 22, Port Output Enable for GPT (POEG).
Asynchronous General-Purpose Timer (AGT)	The Asynchronous General-Purpose Timer (AGT) is a 16-bit timer that can be used for pulse output, external pulse width or period measurement, and counting of external events. This 16-bit timer consists of a reload register and a down-counter. The reload register and the down-counter are allocated to the same address, and can be accessed with the AGT register. See section 25, Asynchronous General-Purpose Timer (AGT).
Realtime Clock (RTC)	The Realtime Clock (RTC) has two counting modes, calendar count mode and binary count mode, that are controlled by the register settings. For calendar count mode, the RTC has a 100-year calendar from 2000 to 2099 and automatically adjusts dates for leap years. For binary count mode, the RTC counts seconds and retains the information as a serial value. Binary count mode can be used for calendars other than the Gregorian (Western) calendar. See section 26, Realtime Clock (RTC).

Table 1.3 系统(2之2)

Feature	功能说明
看门狗定时器(WDT)	看门狗定时器(WDT)是一个14位递减计数器，可用于在计数器下溢时复位MCU，因为系统已失控且无法刷新WDT。此外，下溢可能会产生不可屏蔽的中断或中断。 可以设置一个允许刷新周期来刷新计数器，作为检测系统何时失控的条件。请参见第27节，看门狗定时器(WDT)。
独立看门狗定时器(IWDT)	独立看门狗定时器(IWDT)包含一个14位递减计数器，必须定期对其进行服务以防止计数器下溢。它可用于复位MCU或为定时器下溢生成不可屏蔽中断或中断。由于定时器使用独立的专用时钟源运行，因此当系统失控时，它在将MCU作为故障安全机制返回到已知状态时特别有用。这 IWDT可以在复位、下溢、刷新错误或寄存器中的计数值刷新时自动触发。请参见第28节，独立看门狗定时器(IWDT)。

Table 1.4 活动链接

Feature	功能说明
事件链接控制器(ELC)	EventLinkController(ELC)使用各种外围模块产生的中断请求作为事件信号，将它们连接到不同的模块，实现模块之间的直接交互，无需CPU干预。请参阅第19节，事件链接控制器(ELC)。

Table 1.5 直接内存访问

Feature	功能说明
数据传输控制器(DTC)	数据传输控制器(DTC)模块用于在被中断请求激活时传输数据。请参阅第18节，数据传输控制器(DTC)。
DMA Controller (DMAC)	提供了一个8通道DMA控制器(DMAC)模块，用于在没有CPU的情况下传输数据。当产生DMA传输请求时，DMAC将存储在传输源地址的数据传输到传输目标地址。请参见第17节，DMA控制器(DMAC)。

Table 1.6 外部总线接口

Feature	功能说明
外部总线	CS区（EXBIU）：连接到外部设备（外部存储器接口） SDRAM区（EXBIU）：连接到SDRAM（外部存储器接口） QSPI区（EXBIUT2）：连接到QSPI（外部设备接口） 。

Table 1.7 Timers

Feature	功能说明
通用PWM定时器(GPT)	通用PWM定时器(GPT)是一个具有14个通道的32位定时器。PWM波形可以通过控制加计数器、减计数器或加减计数器来产生。此外，可以生成PWM波形来控制无刷直流电机。GPT也可以用作通用定时器。请参见第23节，通用PWM定时器(GPT)。
GPT(POEG)的端口输出使能	使用PortOutputEnableforGPT(POEG)功能将通用PWM定时器(GPT)输出引脚置于输出禁用状态。请参阅第22节，GPT(POEG)的端口输出启用。
Asynchronous General-Purpose Timer (AGT)	异步通用定时器(AGT)是一个16位定时器，可用于脉冲输出、外部脉冲宽度或周期测量以及外部事件计数。这个16位定时器由一个重载寄存器和一个递减计数器组成。重载寄存器和递减计数器分配到同一个地址，可以通过AGT寄存器访问。请参见第25节，异步通用定时器(AGT)。
实时时钟(RTC)	实时时钟(RTC)有两种计数模式，日历计数模式和二进制计数模式，由寄存器设置控制。对于日历计数模式，RTC有一个从2000年到2099年的100年日历，并自动调整闰年的日期。对于二进制计数模式，RTC会计算秒数并将信息保留为序列值。 二进制计数模式可用于公历（西方）以外的日历。 请参阅第26节，实时时钟(RTC)。

Table 1.8 Communication interfaces (1 of 2)

Feature	Functional description
Serial Communications Interface (SCI)	The Serial Communications Interface (SCI) is configurable to five asynchronous and synchronous serial interfaces: • Asynchronous interfaces (UART and Asynchronous Communications Interface Adapter (ACIA)) • 8-bit clock synchronous interface • Simple IIC (master-only) • Simple SPI • Smart card interface. The smart card interface complies with the ISO/IEC 7816-3 standard for electronic signals and transmission protocol. Each SCI has FIFO buffers to enable continuous and full-duplex communication, and the data transfer speed can be configured independently using an on-chip baud rate generator. See section 34, Serial Communications Interface (SCI).
IrDA interface	The IrDA interface sends and receives IrDA data communication waveforms in cooperation with the SCI1 based on the IrDA (Infrared Data Association) standard 1.0. See section 35, IrDA Interface.
I²C bus interface (IIC)	The 3-channel I²C bus interface (IIC) conforms with and provides a subset of the NXP I²C (Inter-Integrated Circuit) bus interface functions. See section 36, I²C Bus Interface (IIC).
Serial Peripheral Interface (SPI)	Two independent Serial Peripheral Interface (SPI) channels are capable of high-speed, full-duplex synchronous serial communications with multiple processors and peripheral devices. See section 38, Serial Peripheral Interface (SPI).
Serial Sound Interface Enhanced (SSIE)	The Serial Sound Interface Enhanced (SSIE) peripheral provides functionality to interface with digital audio devices for transmitting I²S 2ch, 4ch, 6ch, 8ch, WS Continue/Monaural/TDM audio data over a serial bus. The SSIE supports an audio clock frequency of up to 50 MHz, and can be operated as a slave or master receiver, transmitter, or transceiver to suit various applications. The SSIE includes 32-stage FIFO buffers in the receiver and transmitter, and supports interrupts and DMA-driven data reception and transmission. See section 41, Serial Sound Interface Enhanced (SSIE).
Quad Serial Peripheral Interface (QSPI)	The Quad Serial Peripheral Interface (QSPI) is a memory controller for connecting a serial ROM (nonvolatile memory such as a serial flash memory, serial EEPROM, or serial FeRAM) that has an SPI-compatible interface. See section 39, Quad Serial Peripheral Interface (QSPI).
Controller Area Network (CAN) module	The Controller Area Network (CAN) module provides functionality to receive and transmit data using a message-based protocol between multiple slaves and masters in electromagnetically-noisy applications. The CAN module complies with the ISO 11898-1 (CAN 2.0A/CAN 2.0B) standard and supports up to 32 mailboxes, which can be configured for transmission or reception in normal mailbox and FIFO modes. Both standard (11-bit) and extended (29-bit) messaging formats are supported. See section 37, Controller Area Network (CAN) Module.
USB 2.0 Full-Speed (USBFS) module	The USB 2.0 Full-Speed (USBFS) module can operate as a host controller or device controller. The module supports full-speed and low-speed (host controller only) transfer as defined in Universal Serial Bus Specification 2.0. The module has an internal USB transceiver and supports all of the transfer types defined in the Universal Serial Bus Specification 2.0. The USB has buffer memory for data transfer, providing a maximum of 10 pipes. Pipes 1 to 9 can be assigned any endpoint number based on the peripheral devices used for communication or based on your system. See section 32, USB 2.0 Full-Speed Module (USBFS).
USB 2.0 High-Speed (USBHS) module	The USB 2.0 High-Speed (USBHS) module can operate as a host controller or a device controller. As a host controller, the USBHS supports high-speed transfer, full-speed transfer, and low-speed transfer as defined in the Universal Serial Bus Specification 2.0. As a device controller, the USBHS supports high-speed transfer and full-speed transfer as defined in the Universal Serial Bus Specification 2.0. The USBHS has an internal USB transceiver and supports all of the transfer types defined in the Universal Serial Bus Specification 2.0. The USBHS has FIFO buffers for data transfer, providing a maximum of 10 pipes. Any endpoint number can be assigned to pipes 1 to 9, based on the peripheral devices or your system for communication. See section 33, USB 2.0 High-Speed Module (USBHS).

Table 1.8 通信接口（2个中的1个）

Feature	功能说明
串行通信接口(SCI)	串行通信接口(SCI)可配置为五个异步和同步串行接口： 异步接口（UART和异步通信接口适配器(ACIA)） 8位时钟同步接口 简单IIC（仅限主机） 简单SPI 智能卡接口。智能卡接口符合ISOIEC7816-3电子信号和传输协议标准。每个SCI都有FIFO缓冲区以实现连续和全双工通信，并且可以使用片上波特率发生器独立配置数据传输速度。参见第34节，串行通信接口(SCI)。
IrDA interface	IrDA接口与基于IrDA（InfraredDataAssociation）标准1.0的SCI1协同发送和接收IrDA数据通信波形。参见第35节，IrDA接口。
I2C总线接口(IIC)	3通道I2C总线接口(IIC)符合并提供NXPI2C（内部集成电路）总线接口功能的子集。参见第36节，I2C总线接口(IIC)。
串行外设接口(SPI)	两个独立的串行外围接口(SPI)通道能够与多个处理器和外围设备进行高速、全双工同步串行通信。请参阅第38节，串行外设接口(SPI)。
串行声音接口增强(SSIE)	串行声音接口增强(SSIE)外设提供与数字音频设备接口的功能，用于通过串行总线传输I2S2ch、4ch、6ch、8ch、WSContinue单声道TDM音频数据。SSIE支持高达50MHz的音频时钟频率，并可作为从属或主接收器、发送器或收发器运行，以适应各种应用。SSIE在接收器和发送器中包含32级FIFO缓冲区，并支持中断和DMA驱动的数据接收和发送。请参阅第41节，增强的串行声音接口(SSIE)。
四路串行外设接口(QSPI)	QuadSerialPeripheralInterface(QSPI)是一种存储器控制器，用于连接串行具有SPI兼容接口的ROM（非易失性存储器，例如串行闪存、串行EEPROM或串行FeRAM）。请参见第39节，四通道串行外设接口(QSPI)。
控制器局域网(CAN)模块	控制器局域网(CAN)模块提供了在电磁噪声应用中使用基于消息的协议在多个从机和主机之间接收和传输数据的功能。CAN模块符合ISO11898-1(CAN2.0ACAN2.0B)标准，最多支持32个邮箱，可配置为普通邮箱和FIFO模式下的发送或接收。支持标准（11位）和扩展（29位）消息格式。请参阅第37节，控制器局域网(CAN)模块。
USB2.0全速(USBFS)模块	USB2.0全速(USBFS)模块可以作为主机控制器或设备控制器运行。该模块支持全速和低速（仅限主机控制器）传输，如通用串行总线规范2.0。该模块有一个内部USB收发器，支持通用串行总线规范2.0中定义的所有传输类型。USB具有用于数据传输的缓冲存储器，最多可提供10个管道。可以根据用于通信的外围设备或根据您的系统为管道1到9分配任何端点编号。请参阅第32节，USB2.0全速模块(USBFS)。
USB2.0高速(USBHS)模块	USB2.0高速(USBHS)模块可用作主机控制器或设备控制器。作为主机控制器，USBHS支持通用串行总线规范2.0中定义的高速传输、全速传输和低速传输。作为设备控制器，USBHS支持通用串行总线规范2.0中定义的高速传输和全速传输。USBHS有一个内部USB收发器，支持通用串行总线规范2.0中定义的所有传输类型。USBHS具有用于数据传输的FIFO缓冲区，最多提供10个管道。根据外围设备或您的通信系统，可以将任何端点编号分配给管道1到9。请参阅第33节，USB2.0高速模块(USBHS)。

Table 1.8 Communication interfaces (2 of 2)

Feature	Functional description
Ethernet MAC with IEEE 1588 PTP (ETHERC)	One-channel Ethernet MAC Controller (ETHERC) compliant with the Ethernet/IEEE802.3 Media Access Control (MAC) layer protocol. An ETHERC channel provides one channel of the MAC layer interface, connecting the MCU to the physical layer LSI (PHY-LSI) that allows transmission and reception of frames compliant with the Ethernet and IEEE802.3 standards. The ETHERC is connected to the Ethernet DMA Controller (EDMAC) so data can be transferred without using the CPU. To handle timing and synchronization between devices, an on-chip Precision Time Protocol (PTP) module for the Ethernet PTP Controller (EPTPC) applies the PTP defined in the IEEE 1588-2008 version 2.0 standard. The EPTPC is composed of: • Synchronization Frame Processing unit (SYNFP0) • A Statistical Time Correction Algorithm unit (STCA). Use the EPTPC in combination with the on-chip Ethernet MAC Controller (ETHERC) and the DMA Controller for the PTP Ethernet Controller (PTPEDMAC). See section 29, Ethernet MAC Controller (ETHERC).
SD/MMC Host Interface (SDHI)	The SDHI and MultiMediaCard (MMC) interface module provides the functionality required to connect a variety of external memory cards to the MCU. The SDHI supports both 1-bit and 4-bit buses for connecting memory cards that support SD, SDHC, and SDXC formats. When developing host devices that are compliant with the SD Specifications, you must comply with the SD Host/Ancillary Product License Agreement (SD HALA). The MMC interface supports 1-bit, 4-bit, and 8-bit MMC buses that provide eMMC 4.51 (JEDEC Standard JESD 84-B451) device access. This interface also provides backward compatibility and supports high-speed SDR transfer modes. See section 43, SD/MMC Host Interface (SDHI).

Table 1.9 Analog

Feature	Functional description
12-bit A/D Converter (ADC12)	Up to two successive approximation 12-bit A/D Converters (ADC12) are provided. In unit 0, up to 13 analog input channels are selectable. In unit 1, up to 11 analog input channels, the temperature sensor output, and an internal reference voltage are selectable for conversion. The A/D conversion accuracy is selectable from 12-bit, 10-bit, and 8-bit conversion, making it possible to optimize the tradeoff between speed and resolution in generating a digital value. See section 47, 12-Bit A/D Converter (ADC12).
12-bit D/A Converter (DAC12)	The 12-bit D/A Converter (DAC12) converts data and includes an output amplifier. See section 48, 12-Bit D/A Converter (DAC12).
Temperature Sensor (TSN)	The on-chip Temperature Sensor (TSN) determines and monitors the die temperature for reliable operation of the device. The sensor outputs a voltage directly proportional to the die temperature, and the relationship between the die temperature and the output voltage is linear. The output voltage is provided to the ADC12 for conversion and can also be used by the end application. See section 49, Temperature Sensor (TSN).
High-Speed Analog Comparator (ACMPHS)	The High-Speed Analog Comparator (ACMPHS) compares a test voltage with a reference voltage and provides a digital output based on the conversion result. Both the test and reference voltages can be provided to the comparator from internal sources such as the DAC12 output and internal reference voltage, and an external source with or without an internal PGA. Such flexibility is useful in applications that require go/no-go comparisons to be performed between analog signals without necessarily requiring A/D conversion. See section 50, High-Speed Analog Comparator (ACMPHS).

Table 1.10 Human machine interfaces

Feature	Functional description
Capacitive Touch Sensing Unit (CTSU)	The Capacitive Touch Sensing Unit (CTSU) measures the electrostatic capacitance of the touch sensor. Changes in the electrostatic capacitance are determined by software, which enables the CTSU to detect whether a finger is in contact with the touch sensor. The electrode surface of the touch sensor is usually enclosed with an electrical insulator so that fingers do not come into direct contact with the electrodes. See section 51, Capacitive Touch Sensing Unit (CTSU).

Table 1.8 通信接口（2个中的2个）

Feature	功能说明
具有IEEE1588PTP(ETHERC)的以太网MAC	符合以太网IEEE802.3媒体访问控制(MAC)层协议的单通道以太网MAC控制器(ETHERC)。一个ETHERC通道提供一个通道 MAC层接口，将MCU连接到物理层LSI(PHY-LSI)，允许发送和接收符合以太网和IEEE802.3标准的帧。ETHERC连接到以太网DMA控制器(EDMAC)，因此可以在不使用CPU的情况下传输数据。为了处理设备之间的定时和同步，以太网PTP控制器(EPTPC)的片上精确时间协议(PTP)模块应用了IEEE1588-20082.0版标准中定义的PTP。EPTPC由以下部分组成：•同步帧处理单元(SYNFP0)•统计时间校正算法单元(STCA)。将EPTPC与片上以太网MAC控制器(ETHERC)和用于PTP以太网控制器(PTPEDMAC)的DMA控制器结合使用。参见第29节，以太网MAC Controller (ETHERC).
SDMMC主机接口(SDHI)	SDHI和多媒体卡(MMC)接口模块提供将各种外部存储卡连接到MCU所需的功能。SDHI支持1位和4位总线，用于连接支持SD、SDHC和SDXC格式的存储卡。在开发符合SD规范的主机设备时，您必须遵守SD主机辅助产品许可协议(SDHALA)。MMC接口支持提供eMMC4.51（JEDEC标准JESD84-B451）器件访问的1位、4位和8位MMC总线。该接口还提供向后兼容性并支持高速SDR传输模式。请参阅第43节，SDMMC主机接口(SDHI)。

Table 1.9 Analog

Feature	功能说明
12-bit A/D Converter (ADC12)	最多提供两个逐次逼近型12位模数转换器(ADC12)。在单元0中，最多可选择13个模拟输入通道。在单元1中，可以选择多达11个模拟输入通道、温度传感器输出和内部参考电压进行转换。AD转换精度可从12位、10位和8位转换中选择，从而可以在生成数字值时优化速度和分辨率之间的折衷。请参阅第47节，12位AD转换器(ADC12)。
12-bit D/A Converter (DAC12)	12位DA转换器(DAC12)转换数据并包括一个输出放大器。请参阅第48节，12位DA转换器(DAC12)。
温度传感器(TSN)	片上温度传感器(TSN)确定并监控芯片温度，以确保器件可靠运行。传感器输出与管芯温度成正比的电压，管芯温度与输出电压呈线性关系。输出电压提供给ADC12进行转换，也可供最终应用使用。请参见第49节，温度传感器(TSN)。
高速模拟比较器(ACMPHS)	高速模拟比较器(ACMPHS)将测试电压与参考电压进行比较，并根据转换结果提供数字输出。测试电压和参考电压都可以从内部源（例如DAC12输出和内部参考电压）以及带有或不带有内部PGA的外部源提供给比较器。这种灵活性在需要在模拟信号之间执行go-no-go比较而不一定需要AD转换的应用中很有用。请参见第50节，高速模拟比较器(ACMPHS)。

Table 1.10 人机界面

Feature	功能说明
电容式触控感应单元(CTSU)	电容式触摸传感单元(CTSU)测量触摸传感器的静电电容。静电电容的变化由软件确定，使CTSU能够检测手指是否与触摸传感器接触。触摸传感器的电极表面通常被电绝缘体包围，因此手指不会直接接触电极。请参阅第51节，电容式触摸传感单元(CTSU)。

Table 1.11 Graphics

Feature	Functional description
Graphics LCD Controller (GLCDC)	The Graphics LCD Controller (GLCDC) provides multiple functions and supports various data formats and panels. Key GLCDC features include: • GPX bus master function for accessing graphics data • Superimposition of three planes (single-color background plane, graphic 1-plane, and graphic 2-plane) • Support for many types of 32-bit or 16-bit per pixel graphics data and 8-bit, 4-bit, or 1-bit LUT data format • Digital interface signal output supporting a video image size of WVGA or greater. See section 58, Graphics LCD Controller (GLCDC).
2D Drawing Engine (DRW)	The 2D Drawing Engine (DRW) provides flexible functions that can support almost any object geometry rather than being bound to only a few specific geometries such as lines, triangles, or circles. The edges of every object can be independently blurred or antialiased. Rasterization is executed at one pixel per clock on the bounding box of the object from left to right and top to bottom. The DRW can also raster from bottom to top to optimize the performance in certain cases. In addition, optimization methods are available to avoid rasterization of many empty pixels of the bounding box. The distances to the edges of the object are calculated by a set of edge equations for every pixel of the bounding box. These edge equations can be combined to describe the entire object. If a pixel is inside the object, it is selected for rendering. If it is outside, it is discarded. If it is on the edge, an alpha value can be chosen proportional to the distance of the pixel to the nearest edge for antialiasing. Every pixel that is selected for rendering can be textured. The resulting aRGB quadruple can be modified by a general raster operation approach independently for each of the four channels. The aRGB quadruples can then be blended with one of the multiple blend modes of the DRW. The DRW provides two inputs (texture read and framebuffer read), and one output (framebuffer write). The internal color format is always aRGB (8888). The color formats from the inputs are converted to the internal format on read and a conversion back is made on write. See section 56, 2D Drawing Engine (DRW).
JPEG codec	The JPEG incorporates a JPEG codec that conforms to the JPEG baseline compression and decompression standard. This provides high-speed compression of image data and high-speed decoding of JPEG data. See section 57, JPEG Codec (JPEG).
Parallel Data Capture (PDC) unit	One Parallel Data Capture (PDC) unit is provided for communicating with external I/O devices, including image sensors, and transferring parallel data, such as an image output from the external I/O device through the DTC or DMAC to the on-chip SRAM and external address spaces (the CS and SDRAM areas). See section 44, Parallel Data Capture Unit (PDC).

Table 1.12 Data processing

Feature	Functional description
Cyclic Redundancy Check (CRC) calculator	The Cyclic Redundancy Check (CRC) calculator generates CRC codes to detect errors in the data. The bit order of CRC calculation results can be switched for LSB-first or MSB-first communication. Additionally, various CRC-generating polynomials are available. The snoop function allows monitoring reads from and writes to specific addresses. This function is useful in applications that require CRC code to be generated automatically in certain events, such as monitoring writes to the serial transmit buffer and reads from the serial receive buffer. See section 40, Cyclic Redundancy Check (CRC) Calculator.
Data Operation Circuit (DOC)	The Data Operation Circuit (DOC) compares, adds, and subtracts 16-bit data. See section 52, Data Operation Circuit (DOC).
Sampling Rate Converter (SRC)	The Sampling Rate Converter (SRC) converts the sampling rate of data produced by various audio decoders, such as the WMA, MP3, and AAC. Both 16-bit stereo and monaural data are supported. See section 42, Sampling Rate Converter (SRC).

Table 1.11 Graphics

Feature	功能说明
图形LCD控制器(GLCDC)	图形LCD控制器(GLCDC)提供多种功能并支持各种数据格式和面板。主要GLCDC功能包括： 用于访问图形数据的GPX总线主控功能 三个平面的叠加（单色背景平面、图形1平面和图形2平面）支持多种32位或16位每像素图形数据和8位、4位或1位LUT数据格式 支持WVGA或更大视频图像大小的数字接口信号输出。请参阅第58节，图形LCD控制器(GLCDC)。
2D绘图引擎(DRW)	2D绘图引擎(DRW)提供了灵活的功能，可以支持几乎任何对象几何形状，而不是仅绑定到一些特定的几何形状，例如线条、三角形或圆形。每个对象的边缘都可以独立模糊或抗锯齿。在对象的边界框上从左到右和从上到下以每个时钟一个像素执行光栅化。在某些情况下，DRW还可以从下到上进行光栅化以优化性能。此外，还可以使用优化方法来避免边界框的许多空像素的光栅化。到对象边缘的距离由边界框的每个像素的一组边缘方程计算。这些边缘方程可以组合起来描述整个物体。如果像素在对象内部，则选择它进行渲染。如果它在外面，它就会被丢弃。如果它在边缘，则可以选择与像素到最近边缘的距离成比例的alpha值以进行抗锯齿。每个被选择用于渲染的像素都可以被纹理化。可以通过通用光栅操作方法对四个通道中的每一个独立地修改得到的aRGB四元组。然后可以将aRGB四元组与DRW的多种混合模式之一混合。DRW提供两个输入（纹理读取和帧缓冲区读取）和一个输出（帧缓冲区写入）。内部颜色格式始终为aRGB(8888)。来自输入的颜色格式在读取时转换为内部格式，并在写入时进行转换。请参阅第56节，2D绘图引擎(DRW)。
JPEG编解码器	JPEG包含符合JPEG基线压缩和解压缩标准的JPEG编解码器。这提供了图像数据的高速压缩和JPEG数据的高速解码。请参阅第57节，JPEG编解码器(JPEG)。
并行数据采集(PDC)单元	提供一个并行数据采集(PDC)单元，用于与外部IO设备（包括图像传感器）通信，并传输并行数据，例如通过DTC或DMAC从外部IO设备输出的图像到片上SRAM和外部地址空间（CS和SDRAM区域）。请参见第44节，并行数据采集单元(PDC)。

Table 1.12 数据处理

Feature	功能说明
循环冗余校验(CRC)计算器	循环冗余校验(CRC)计算器生成CRC代码以检测数据中的错误。CRC计算结果的位顺序可以切换为LSB-first或MSB-first通信。此外，还可以使用各种生成CRC的多项式。snoop功能允许监视对特定地址的读取和写入。此功能在需要在某些事件中自动生成CRC代码的应用中很有用，例如监视对串行发送缓冲区的写入和从串行接收缓冲区的读取。请参阅第40节，循环冗余校验(CRC)计算器。
数据运算电路(DOC)	数据运算电路(DOC)对16位数据进行比较、加法和减法。见第52节，数据运算电路（DOC）。
采样率转换器(SRC)	采样率转换器(SRC)转换各种音频解码器（如WMA、MP3和AAC）产生的数据的采样率。支持16位立体声和单声道数据。请参见第42节，采样率转换器(SRC)。

Table 1.13 Security

Feature	Functional description
Secure Crypto Engine 7 (SCE7)	• Security algorithms: - Symmetric algorithms: AES, 3DES, and ARC4 - Asymmetric algorithms: RSA, DSA, and ECC. • Other support features: - TRNG (True Random Number Generator) - Hash-value generation: SHA1, SHA224, SHA256, GHASH, and MD5 - 128-bit unique ID. See section 46, Secure Cryptographic Engine (SCE7).

Table 1.13 Security

Feature	功能说明
安全加密引擎7(SCE7)	• Security algorithms: 对称算法：AES、3DES和ARC4非对称算法：RSA 、DSA和ECC。 其他支持功能： TRNG（真随机数生成器）哈希值生成：SHA1、SHA224、SHA256、GH ASH和MD5128位唯一ID。请参阅第46节，安全加密引擎(SCE7)。

1.2 Block Diagram

Figure 1.1 shows a block diagram of the MCU superset, some individual devices within the group have a subset of the features.

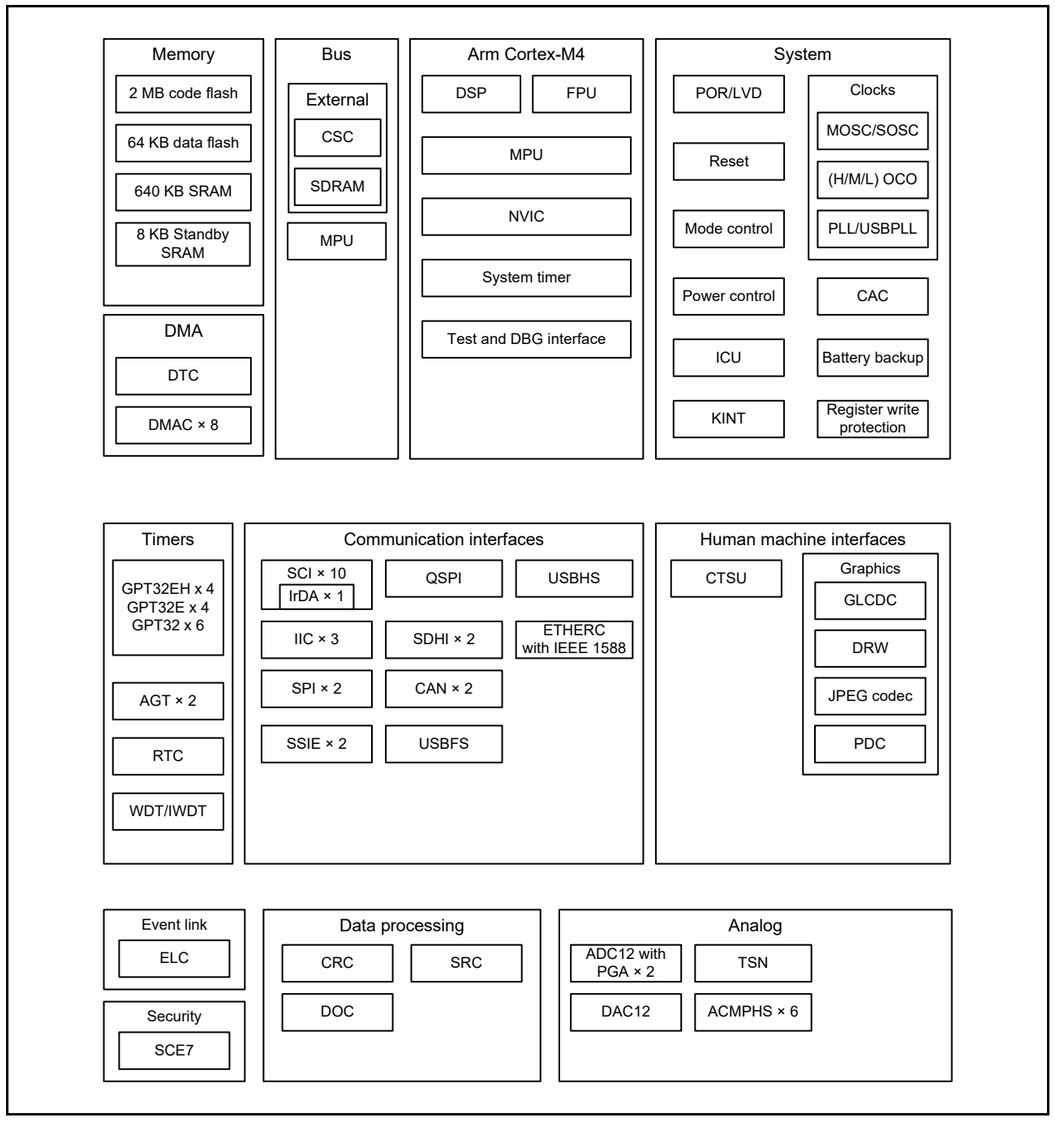


Figure 1.1 Block diagram

1.2 框图

图1.1显示了MCU超集的框图，该组中的一些单独的设备具有功能的子集。

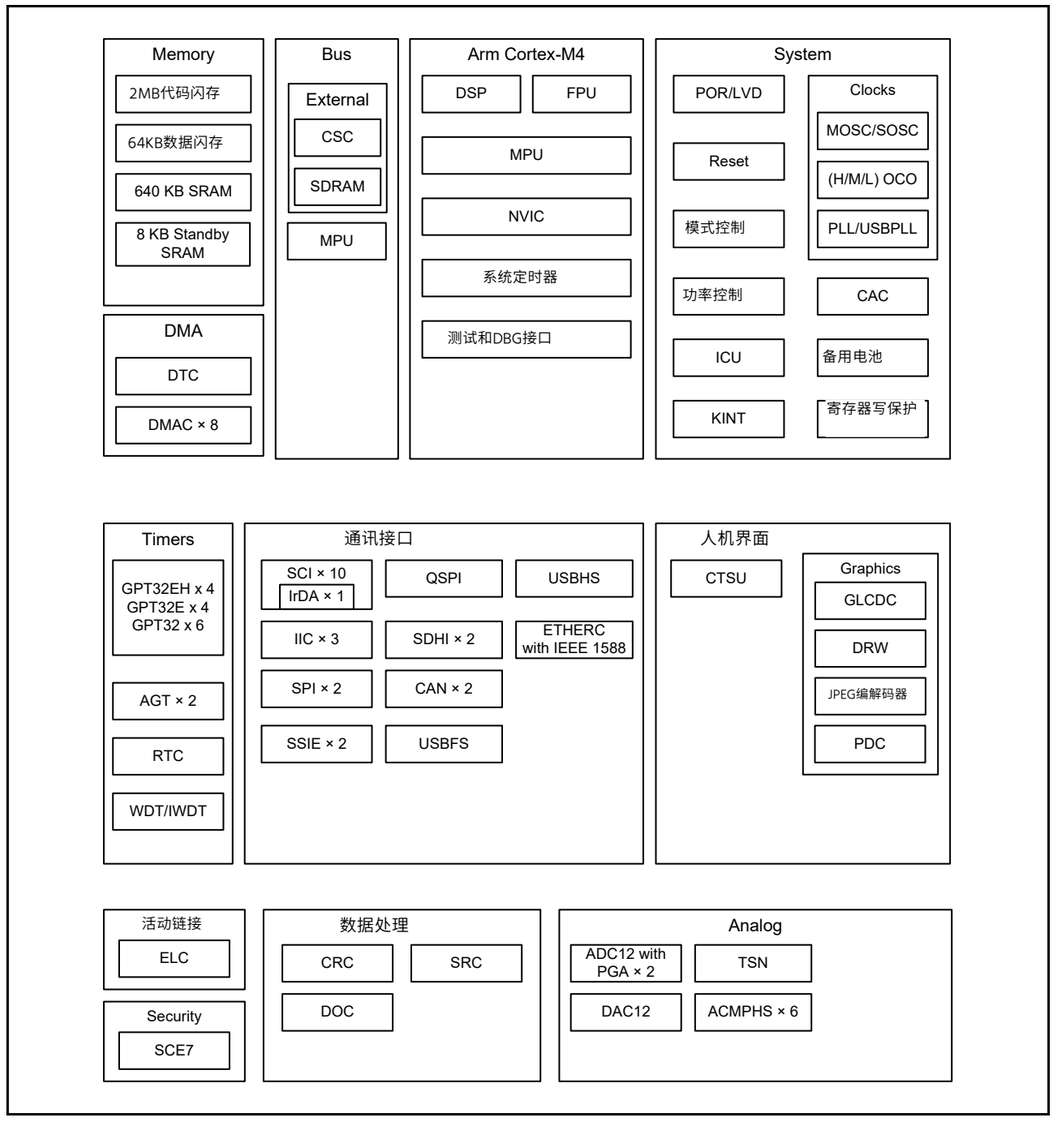


Figure 1.1 框图

1.3 Part Numbering

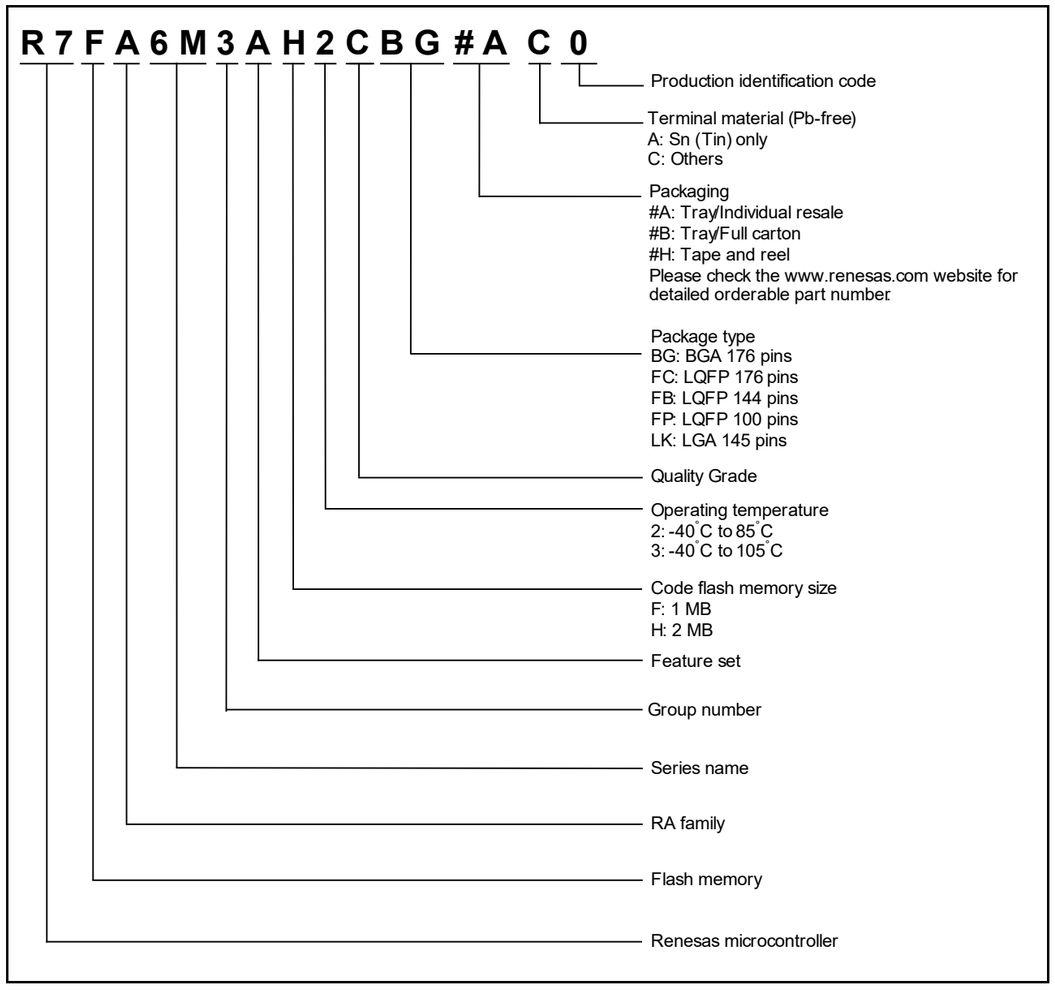


Figure 1.2 Part numbering scheme

1.3 零件编号

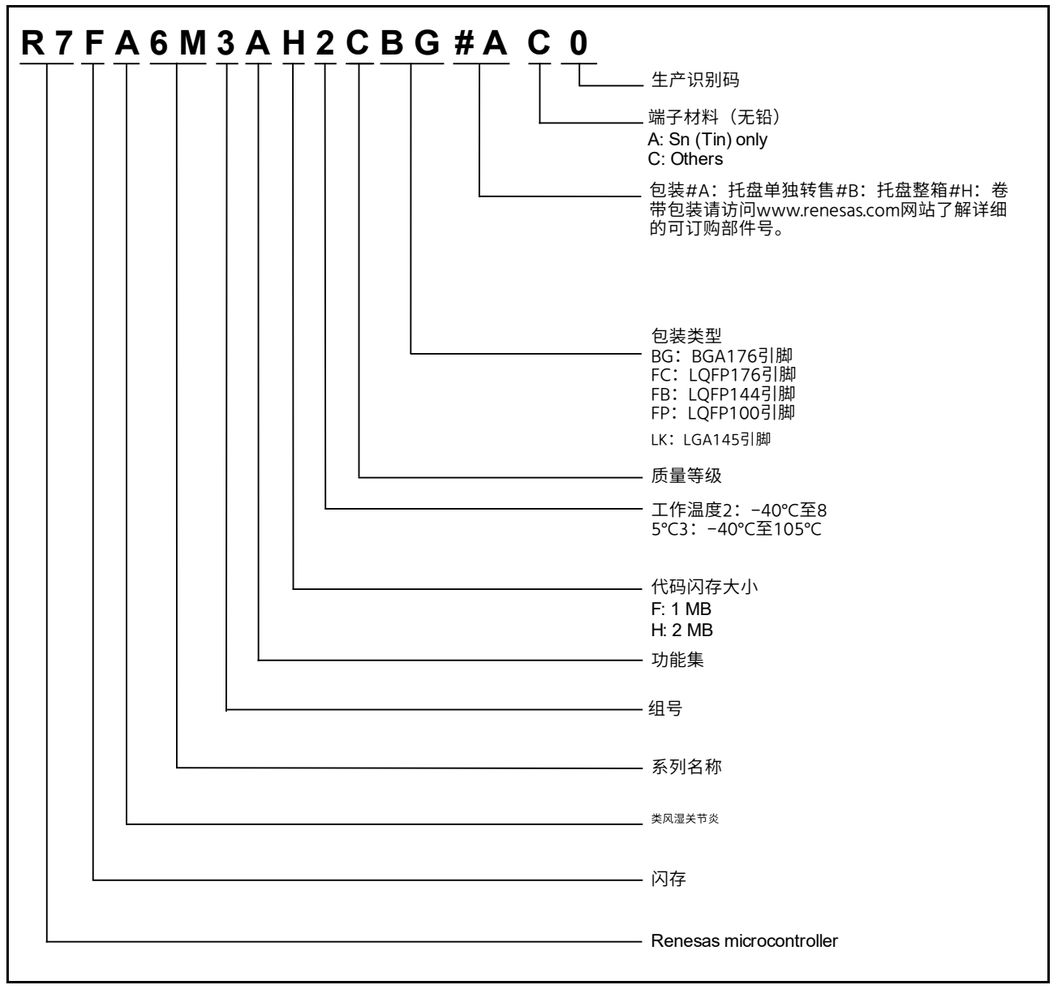


Figure 1.2 零件编号方案

Table 1.14 Product list

Product part number	Package code	Code flash	Data flash	SRAM	Operating temperature
R7FA6M3AH2CBG	PLBG0176GE-A	2 MB	64 KB	640 KB	-40 to +85°C
R7FA6M3AH3CFC	PLQP0176KB-A				-40 to +105°C
R7FA6M3AH2CLK	PTLG0145KA-A				-40 to +85°C
R7FA6M3AH3CFB	PLQP0144KA-B				-40 to +105°C
R7FA6M3AH3CFP	PLQP0100KB-B				-40 to +105°C
R7FA6M3AF2CBG	PLBG0176GE-A	1 MB			-40 to +85°C
R7FA6M3AF3CFC	PLQP0176KB-A				-40 to +105°C
R7FA6M3AF2CLK	PTLG0145KA-A				-40 to +85°C
R7FA6M3AF3CFB	PLQP0144KA-B				-40 to +105°C
R7FA6M3AF3CFP	PLQP0100KB-B				-40 to +105°C

Table 1.14 产品列表

产品部件号	包装代码	代码闪存	数据闪存	SRAM	工作温度
R7FA6M3AH2CBG	PLBG0176GE-A	2 MB	64 KB	640 KB	-40 to +85°C
R7FA6M3AH3CFC	PLQP0176KB-A				-40 to +105°C
R7FA6M3AH2CLK	PTLG0145KA-A				-40 to +85°C
R7FA6M3AH3CFB	PLQP0144KA-B				-40 to +105°C
R7FA6M3AH3CFP	PLQP0100KB-B				-40 to +105°C
R7FA6M3AF2CBG	PLBG0176GE-A	1 MB			-40 to +85°C
R7FA6M3AF3CFC	PLQP0176KB-A				-40 to +105°C
R7FA6M3AF2CLK	PTLG0145KA-A				-40 to +85°C
R7FA6M3AF3CFB	PLQP0144KA-B				-40 to +105°C
R7FA6M3AF3CFP	PLQP0100KB-B				-40 to +105°C

1.4 Function Comparison

Table 1.15 Functional comparison

Function		Part numbers				
		R7FA6M3AH2CBG/ R7FA6M3AF2CBG	R7FA6M3AH3CFC/ R7FA6M3AF3CFC	R7FA6M3AH2CLK/ R7FA6M3AF2CLK	R7FA6M3AH3CFB/ R7FA6M3AF3CFB	R7FA6M3AH3CFP/ R7FA6M3AF3CFP
Pin count		176	176	145	144	100
Package		BGA	LQFP	LGA	LQFP	LQFP
Code flash memory		2/1 MB				
Data flash memory		64 KB				
SRAM		640 KB				
	Parity	608 KB				
	ECC	32 KB				
Standby SRAM		8 KB				
System	CPU clock	120 MHz				
	Backup registers	512 B				
	ICU	Yes				
	KINT	8				
Event link	ELC	Yes				
DMA	DTC	Yes				
	DMAC	8				
BUS	External bus	16-bit bus				8-bit bus
	SDRAM	Yes				No
Timers	GPT32EH	4	4	4	4	4
	GPT32E	4	4	4	4	4
	GPT32	6	6	6	6	5
	AGT	2	2	2	2	2
	RTC	Yes				
	WDT/IWDT	Yes				
Communication	SCI	10				
	IIC	3				2
	SPI	2				
	SSIE	2				1
	QSPI	1				
	SDHI	2				
	CAN	2				
	USBFS	Yes				
	USBHS	Yes		No		
	ETHERC	1				
Analog	ADC12	24		22		19
	DAC12	2				
	ACMPHS	6				
	TSN	Yes				
HMI	CTSU	13		18		12
Graphics	GLCDC	RGB888				
	DRW	Yes				
	JPEG	Yes				
	PDC	Yes				
Data processing	CRC	Yes				
	DOC	Yes				
	SRC	Yes				
Security		SCE7				

1.4 功能比较

Table 1.15 功能比较

Function		零件号				
		R7FA6M3AH2CBG/ R7FA6M3AF2CBG	R7FA6M3AH3CFC/ R7FA6M3AF3CFC	R7FA6M3AH2CLK/ R7FA6M3AF2CLK	R7FA6M3AH3CFB/ R7FA6M3AF3CFB	R7FA6M3AH3CFP/ R7FA6M3AF3CFP
针数		176	176	145	144	100
Package		BGA	LQFP	LGA	LQFP	LQFP
代码闪存		2/1 MB				
数据闪存		64 KB				
SRAM		640 KB				
	Parity	608 KB				
	ECC	32 KB				
Standby SRAM		8 KB				
System	中央处理器时钟	120 MHz				
	备份寄存器	512 B				
	ICU	Yes				
	KINT	8				
活动链接	ELC	Yes				
DMA	DTC	Yes				
	DMAC	8				
BUS	外部总线	16-bit bus				8-bit bus
	SDRAM	Yes				No
Timers	GPT32EH	4	4	4	4	4
	GPT32E	4	4	4	4	4
	GPT32	6	6	6	6	5
	AGT	2	2	2	2	2
	RTC	Yes				
	WDT/IWDT	Yes				
Communication	SCI	10				
	IIC	3				2
	SPI	2				
	SSIE	2				1
	QSPI	1				
	SDHI	2				
	CAN	2				
	USBFS	Yes				
	USBHS	Yes		No		
	ETHERC	1				
Analog	ADC12	24		22		19
	DAC12	2				
	ACMPHS	6				
	TSN	Yes				
HMI	CTSU	13		18		12
Graphics	GLCDC	RGB888				
	DRW	Yes				
	JPEG	Yes				
	PDC	Yes				
数据处理	CRC	Yes				
	DOC	Yes				
	SRC	Yes				
Security		SCE7				

1.5 Pin Functions

Table 1.16 Pin functions (1 of 5)

Function	Signal	I/O	Description
Power supply	VCC	Input	Digital voltage supply pin. This is used as the digital power supply for the respective modules and internal voltage regulator, and used to monitor the voltage of the POR/LVD. Connect to the system power supply. Connect to VSS through a 0.1-μF smoothing capacitor close to each VCC pin.
	VCL0	-	Connect to VSS through a 0.1-μF smoothing capacitor close to each VCL pin. Stabilize the internal power supply.
	VCL	-	
	VSS	Input	Ground pin. Connect to the system power supply (0 V).
	VBATT	Input	Backup power pin
Clock	XTAL	Output	Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin.
	EXTAL	Input	
	XCIN	Input	Input/output pins for the sub-clock oscillator. Connect a crystal resonator between XCOUT and XCIN.
	XCOUT	Output	
	EBCLK	Output	Outputs the external bus clock for external devices
	SDCLK	Output	Outputs the SDRAM-dedicated clock
	CLKOUT	Output	Clock output pin
Operating mode control	MD	Input	Pin for setting the operating mode. The signal level on this pin must not be changed during operation mode transition on release from the reset state.
System control	RES	Input	Reset signal input pin. The MCU enters the reset state when this signal goes low.
CAC	CACREF	Input	Measurement reference clock input pin
Interrupt	NMI	Input	Non-maskable interrupt request pin
	IRQ0 to IRQ15	Input	Maskable interrupt request pins
KINT	KR00 to KR07	Input	A key interrupt can be generated by inputting a falling edge to the key interrupt input pins
On-chip emulator	TMS	I/O	On-chip emulator or boundary scan pins
	TDI	Input	
	TCK	Input	
	TDO	Output	
	TCLK	Output	This pin outputs the clock for synchronization with the trace data
	TDATA0 to TDATA3	Output	Trace data output
	SWDIO	I/O	Serial wire debug data input/output pin
	SWCLK	Input	Serial wire clock pin
	SWO	Output	Serial wire trace output pin
External bus interface	RD	Output	Strobe signal indicating that reading from the external bus interface space is in progress, active low
	WR	Output	Strobe signal indicating that writing to the external bus interface space is in progress, in 1-write strobe mode, active low
	WR0 to WR1	Output	Strobe signals indicating that either group of data bus pins (D07 to D00 or D15 to D08) is valid in writing to the external bus interface space, in byte strobe mode, active low
	BC0 to BC1	Output	Strobe signals indicating that either group of data bus pins (D07 to D00 or D15 to D08) is valid in access to the external bus interface space, in 1-write strobe mode, active low
	ALE	Output	Address latch signal when address/data multiplexed bus is selected
	WAIT	Input	Input pin for wait request signals in access to the external space, active low
	CS0 to CS7	Output	Select signals for CS areas, active low
	A00 to A23	Output	Address bus
	D00 to D15	I/O	Data bus
	A00/D00 to A15/D15	I/O	Address/data multiplexed bus

1.5 引脚功能

Table 1.16 引脚功能(1of5)

Function	Signal	I/O	Description
电源	VCC	Input	数字电压电源引脚。这用作各个模块和内部稳压器的数字电源，并用于监控PORLVD的电压。连接到系统电源。通过靠近每个VCC引脚的0.1μF平滑电容器连接到VSS。
	VCL0	-	通过靠近每个VCL引脚的0.1μF平滑电容器连接到VSS。稳定内部电源。
	VCL	-	
	VSS	Input	接地引脚。连接到系统电源(0V)。
	VBATT	Input	备用电源引脚
Clock	XTAL	Output	晶体谐振器的引脚。外部时钟信号可以通过输入 EXTAL pin.
	EXTAL	Input	
	XCIN	Input	副时钟振荡器的输入输出引脚。在XCOUT和XCIN之间连接一个晶体谐振器。
	XCOUT	Output	
	EBCLK	Output	为外部设备输出外部总线时钟
	SDCLK	Output	输出SDRAM专用时钟
	CLKOUT	Output	时钟输出引脚
操作模式控制	MD	Input	用于设置操作模式的引脚。在从复位状态释放的操作模式转换期间，不得更改此引脚上的信号电平。
系统控制	RES	Input	复位信号输入引脚。当该信号变低时，MCU进入复位状态。
CAC	CACREF	Input	测量参考时钟输入引脚
Interrupt	NMI	Input	不可屏蔽中断请求引脚
	IRQ0 to IRQ15	Input	可屏蔽中断请求引脚
KINT	KR00 to KR07	Input	通过向按键中断输入引脚输入下降沿可以产生按键中断
On-chip emulator	TMS	I/O	片上仿真器或边界扫描引脚
	TDI	Input	
	TCK	Input	
	TDO	Output	
	TCLK	Output	该引脚输出与跟踪数据同步的时钟
	TDATA0 to TDATA3	Output	跟踪数据输出
	SWDIO	I/O	串行线调试数据输入输出引脚
	SWCLK	Input	串行线时钟引脚
	SWO	Output	串行线迹输出引脚
外部总线接口	RD	Output	指示正在从外部总线接口空间读取的选通信号，低电平有效
	WR	Output	Strobe信号指示正在写入外部总线接口空间，在1-writestrobe模式下，低电平有效
	WR0 to WR1	Output	选通信号指示任一组数据总线引脚（D07到D00或D15到D08）在写入外部总线接口空间时有效，在字节选通模式下，低电平有效
	BC0 to BC1	Output	选通信号指示任一组数据总线引脚（D07至D00或 D15到D08）在访问外部总线接口空间时有效，在1-write选通模式下，低电平有效
	ALE	Output	选择地址数据复用总线时的地址锁存信号
	WAIT	Input	用于访问外部空间的等待请求信号的输入引脚，低电平有效
	CS0 to CS7	Output	CS区域的选择信号，低电平有效
	A00 to A23	Output	地址总线
	D00 to D15	I/O	数据总线
	A00/D00 to A15/D15	I/O	Address/data multiplexed bus

Table 1.16 Pin functions (2 of 5)

Function	Signal	I/O	Description
SDRAM interface	CKE	Output	SDRAM clock enable signal
	SDCS	Output	SDRAM chip select signal, active low
	RAS	Output	SDRAM low address strobe signal, active low
	CAS	Output	SDRAM column address strobe signal, active low
	WE	Output	SDRAM write enable signal, active low
	DQM0	Output	SDRAM I/O data mask enable signal for DQ07 to DQ00
	DQM1	Output	SDRAM I/O data mask enable signal for DQ15 to DQ08
	A00 to A15	Output	Address bus
	DQ00 to DQ15	I/O	Data bus
GPT	GTETRGA, GTETRGB, GTETRGC, GTETRGD	Input	External trigger input pins
	GTIOC0A to GTIOC13A, GTIOC0B to GTIOC13B	I/O	Input capture, output compare, or PWM output pins
	GTIU	Input	Hall sensor input pin U
	GTIV	Input	Hall sensor input pin V
	GTIW	Input	Hall sensor input pin W
	GTOUUP	Output	3-phase PWM output for BLDC motor control (positive U phase)
	GTOULO	Output	3-phase PWM output for BLDC motor control (negative U phase)
	GTOVUP	Output	3-phase PWM output for BLDC motor control (positive V phase)
	GTOVLO	Output	3-phase PWM output for BLDC motor control (negative V phase)
	GTOWUP	Output	3-phase PWM output for BLDC motor control (positive W phase)
	GTOWLO	Output	3-phase PWM output for BLDC motor control (negative W phase)
AGT	AGTEE0, AGTEE1	Input	External event input enable signals
	AGTIO0, AGTIO1	I/O	External event input and pulse output pins
	AGTO0, AGTO1	Output	Pulse output pins
	AGTOA0, AGTOA1	Output	Output compare match A output pins
	AGTOB0, AGTOB1	Output	Output compare match B output pins
RTC	RTCOUT	Output	Output pin for 1-Hz or 64-Hz clock
	RTCIC0 to RTCIC2	Input	Time capture event input pins
SCI	SCK0 to SCK9	I/O	Input/output pins for the clock (clock synchronous mode)
	RXD0 to RXD9	Input	Input pins for received data (asynchronous mode/clock synchronous mode)
	TXD0 to TXD9	Output	Output pins for transmitted data (asynchronous mode/clock synchronous mode)
	CTS0_RTS0 to CTS9_RTS9	I/O	Input/output pins for controlling the start of transmission and reception (asynchronous mode/clock synchronous mode), active low
	SCL0 to SCL9	I/O	Input/output pins for the I^2C clock (simple IIC mode)
	SDA0 to SDA9	I/O	Input/output pins for the I^2C data (simple IIC mode)
	SCK0 to SCK9	I/O	Input/output pins for the clock (simple SPI mode)
	MISO0 to MISO9	I/O	Input/output pins for slave transmission of data (simple SPI mode)
	MOSI0 to MOSI9	I/O	Input/output pins for master transmission of data (simple SPI mode)
	SS0 to SS9	Input	Chip-select input pins (simple SPI mode), active low
IIC	SCL0 to SCL2	I/O	Input/output pins for the clock
	SDA0 to SDA2	I/O	Input/output pins for data
SSIE	SSIBCK0	I/O	SSIE serial bit clock pins
	SSIBCK1		
	SSILRCK0/SSIFS0	I/O	LR clock/frame synchronization pins
	SSILRCK1/SSIFS1		
	SSITXD0	Output	Serial data output pins
	SSIRXD0	Input	Serial data input pins
	SSIDATA1	I/O	Serial data input/output pins
	AUDIO_CLK	Input	External clock pin for audio (input oversampling clock)

Table 1.16 引脚功能（2个，共5个）

Function	Signal	I/O	Description
SDRAM interface	CKE	Output	SDRAM时钟使能信号
	SDCS	Output	SDRAM片选信号，低电平有效
	RAS	Output	SDRAM低地址选通信号，低电平有效
	CAS	Output	SDRAM列地址选通信号，低电平有效
	WE	Output	SDRAM写使能信号，低电平有效
	DQM0	Output	DQ07到DQ00的SDRAMIO数据屏蔽使能信号
	DQM1	Output	DQ15至DQ08的SDRAMIO数据屏蔽使能信号
	A00 to A15	Output	地址总线
	DQ00 to DQ15	I/O	数据总线
GPT	GTETRGA, GTETRGB, GTETRGC, GTETRGD	Input	外部触发输入引脚
	GTIOC0A to GTIOC13A, GTIOC0B to GTIOC13B	I/O	输入捕捉、输出比较或PWM输出引脚
	GTIU	Input	霍尔传感器输入引脚U
	GTIV	Input	霍尔传感器输入引脚V
	GTIW	Input	霍尔传感器输入引脚W
	GTOUUP	Output	用于BLDC电机控制的3相PWM输出（正U相）
	GTOULO	Output	用于BLDC电机控制的3相PWM输出（负U相）
	GTOVUP	Output	用于BLDC电机控制的3相PWM输出（正V相）
	GTOVLO	Output	用于BLDC电机控制的3相PWM输出（负V相）
	GTOWUP	Output	用于BLDC电机控制的3相PWM输出（正W相）
	GTOWLO	Output	用于BLDC电机控制的3相PWM输出（负W相）
AGT	AGTEE0, AGTEE1	Input	外部事件输入使能信号
	AGTIO0, AGTIO1	I/O	外部事件输入和脉冲输出引脚
	AGTO0, AGTO1	Output	脉冲输出引脚
	AGTOA0, AGTOA1	Output	输出比较匹配A输出引脚
	AGTOB0, AGTOB1	Output	输出比较匹配B输出引脚
RTC	RTCOUT	Output	用于1Hz或64Hz时钟的输出引脚
	RTCIC0 to RTCIC2	Input	时间捕捉事件输入引脚
SCI	SCK0 to SCK9	I/O	时钟输入输出引脚（时钟同步模式）
	RXD0 to RXD9	Input	接收数据的输入引脚（异步模式时钟同步模式）
	TXD0 to TXD9	Output	传输数据的输出引脚（异步模式时钟同步模式）
	CTS0_RTS0 to CTS9_RTS9	I/O	输入输出引脚用于控制发送和接收的开始（异步模式时钟同步模式），低电平有效
	SCL0 to SCL9	I/O	I2C时钟的输入输出引脚（简单IIC模式）
	SDA0 to SDA9	I/O	I2C数据的输入输出引脚（简单IIC模式）
	SCK0 to SCK9	I/O	时钟输入输出引脚（简单SPI模式）
	MISO0 to MISO9	I/O	用于从机传输数据的输入输出引脚（简单SPI模式）
	MOSI0 to MOSI9	I/O	输入输出引脚用于主数据传输（简单SPI模式）
	SS0 to SS9	Input	片选输入引脚（简单SPI模式），低电平有效
IIC	SCL0 to SCL2	I/O	时钟的输入输出引脚
	SDA0 to SDA2	I/O	数据输入输出引脚
SSIE	SSIBCK0	I/O	SSIE串行位时钟引脚
	SSIBCK1		
	SSILRCK0/SSIFS0	I/O	LR时钟帧同步管脚
	SSILRCK1/SSIFS1		
	SSITXD0	Output	串行数据输出引脚
	SSIRXD0	Input	串行数据输入引脚
	SSIDATA1	I/O	串行数据输入输出引脚
	AUDIO_CLK	Input	音频外部时钟引脚（输入过采样时钟）

Table 1.16 Pin functions (3 of 5)

Function	Signal	I/O	Description
SPI	RSPCKA, RSPCKB	I/O	Clock input/output pin
	MOSIA, MOSIB	I/O	Input or output pins for data output from the master
	MISOA, MISOB	I/O	Input or output pins for data output from the slave
	SSLA0, SSLB0	I/O	Input or output pin for slave selection
	SSLA1 to SSLA3, SSLB1 to SSLB3	Output	Output pins for slave selection
QSPI	QSPCLK	Output	QSPI clock output pin
	QSSL	Output	QSPI slave output pin
	QIO0 to QIO3	I/O	Data0 to Data3
CAN	CRX0, CRX1	Input	Receive data
	CTX0, CTX1	Output	Transmit data
USBFS	VCC_USB	Input	Power supply pins
	VSS_USB	Input	Ground pins
	USB_DP	I/O	D+ I/O pin of the USB on-chip transceiver. Connect this pin to the D+ pin of the USB bus
	USB_DM	I/O	D- I/O pin of the USB on-chip transceiver. Connect this pin to the D- pin of the USB bus
	USB_VBUS	Input	USB cable connection monitor pin. Connect this pin to VBUS of the USB bus. The VBUS pin status (connected or disconnected) can be detected when the USB module is operating as a function controller.
	USB_EXICEN	Output	Low-power control signal for external power supply (OTG) chip
	USB_VBUSEN	Output	VBUS (5 V) supply enable signal for external power supply chip
	USB_OVRCURA, USB_OVRCURB	Input	Connect the external overcurrent detection signals to these pins. Connect the VBUS comparator signals to these pins when the OTG power supply chip is connected.
	USB_ID	Input	Connect the MicroAB connector ID input signal to this pin during operation in OTG mode
USBHS	VCC_USBHS	Input	Power supply pin
	VSS1_USBHS	Input	Ground pin
	VSS2_USBHS	Input	Ground pin
	AVCC_USBHS	Input	Analog power supply pin for the USBHS
	AVSS_USBHS	Input	Analog ground pin for the USBHS. Must be shorted to the PVSS_USBHS pin
	PVSS_USBHS	Input	PLL circuit ground pin for the USBHS. Must be shorted to the AVSS_USBHS pin
	USBHS_RREF	I/O	USBHS reference current source pin. Connect this pin to the AVSS_USBHS pin through a 2.2-kΩ resistor (±1%)
	USBHS_DP	I/O	USB bus D+ data pin
	USBHS_DM	I/O	USB bus D- data pin
	USBHS_EXICEN	Output	Connect this pin to the OTG power supply IC
	USBHS_ID	Input	Connect this pin to the OTG power supply IC
	USBHS_VBUSEN	Output	VBUS power enable signal for USB
	USBHS_OVRCURA, USBHS_OVRCURB	Input	Overcurrent pin for USB
	USBHS_VBUS	Input	USB cable connection monitor input pin

Table 1.16 引脚功能(3of5)

Function	Signal	I/O	Description
SPI	RSPCKA, RSPCKB	I/O	时钟输入输出引脚
	MOSIA, MOSIB	I/O	用于从主机输出数据的输入或输出引脚
	MISOA, MISOB	I/O	从机数据输出的输入或输出引脚
	SSLA0, SSLB0	I/O	从机选择的输入或输出引脚
	SSLA1 to SSLA3, SSLB1 to SSLB3	Output	从机选择的输出引脚
QSPI	QSPCLK	Output	QSPI时钟输出引脚
	QSSL	Output	QSPI从机输出引脚
	QIO0 to QIO3	I/O	Data0 to Data3
CAN	CRX0, CRX1	Input	接收数据
	CTX0, CTX1	Output	传输数据
USBFS	VCC_USB	Input	电源引脚
	VSS_USB	Input	接地引脚
	USB_DP	I/O	USB片上收发器的D+IO引脚。将此引脚连接到USB总线的D+引脚
	USB_DM	I/O	USB片上收发器的DIO引脚。将此引脚连接到USB总线的Dpin
	USB_VBUS	Input	USB电缆连接监视器引脚。将此引脚连接到USB总线的VBUS。当USB模块作为功能控制器运行时，可以检测VBUS引脚状态（连接或断开）。
	USB_EXICEN	Output	用于外部电源(OTG)芯片的低功耗控制信号
	USB_VBUSEN	Output	VBUS(5V)为外部供电芯片供电使能信号
	USB_OVRCURA, USB_OVRCURB	Input	将外部过电流检测信号连接到这些引脚。连接OTG电源芯片时，将VBUS比较器信号连接到这些引脚。
	USB_ID	Input	在操作期间将MicroAB连接器ID输入信号连接到此引脚 OTG mode
USBHS	VCC_USBHS	Input	电源引脚
	VSS1_USBHS	Input	接地引脚
	VSS2_USBHS	Input	接地引脚
	AVCC_USBHS	Input	USBHS的模拟电源引脚
	AVSS_USBHS	Input	USBHS的模拟接地引脚。必须短接到PVSS_USBHS引脚
	PVSS_USBHS	Input	USBHS的PLL电路接地引脚。必须短接到AVSS_USBHS引脚
	USBHS_RREF	I/O	USBHS参考电流源引脚。通过一个2.2-kΩ电阻(　1%)将此引脚连接到AVSS_USBHS引脚
	USBHS_DP	I/O	USB总线D+数据引脚
	USBHS_DM	I/O	USB总线Ddata引脚
	USBHS_EXICEN	Output	将此引脚连接到OTG电源IC
	USBHS_ID	Input	将此引脚连接到OTG电源IC
	USBHS_VBUSEN	Output	USB的VBUS电源使能信号
	USBHS_OVRCURA, USBHS_OVRCURB	Input	USB过流引脚
	USBHS_VBUS	Input	USB线连接显示器输入引脚

Table 1.16 Pin functions (4 of 5)

Function	Signal	I/O	Description
ETHERC	REF50CK0	Input	50-MHz reference clock. This pin inputs reference signal for transmission/reception timing in RMII mode.
	RMII0_CRS_DV	Input	Indicates carrier detection signals and valid receive data on RMII0_RXD1 and RMII0_RXD0 in RMII mode
	RMII0_TXD0, RMII0_TXD1	Output	2-bit transmit data in RMII mode
	RMII0_RXD0, RMII0_RXD1	Input	2-bit receive data in RMII mode
	RMII0_TXD_EN	Output	Output pin for data transmit enable signal in RMII mode
	RMII0_RX_ER	Input	Indicates an error occurred during reception of data in RMII mode
	ET0_CRS	Input	Carrier detection/data reception enable signal
	ET0_RX_DV	Input	Indicates valid receive data on ET0_ERXD3 to ET0_ERXD0
	ET0_EXOUT	Output	General-purpose external output pin
	ET0_LINKSTA	Input	Input link status from the PHY-LSI
	ET0_ETXD0 to ET0_ETXD3	Output	4 bits of MII transmit data
	ET0_ERXD0 to ET0_ERXD3	Input	4 bits of MII receive data
	ET0_TX_EN	Output	Transmit enable signal. Functions as signal indicating that transmit data is ready on ET0_ETXD3 to ET0_ETXD0
	ET0_TX_ER	Output	Transmit error pin. Functions as signal notifying the PHY_LSI of an error during transmission
	ET0_RX_ER	Input	Receive error pin. Functions as signal to recognize an error during reception
	ET0_TX_CLK	Input	Transmit clock pin. This pin inputs reference signal for output timing from ET0_TX_EN, ET0_ETXD3 to ET0_ETXD0, and ET0_TX_ER
	ET0_RX_CLK	Input	Receive clock pin. This pin inputs reference signal for input timing to ET0_RX_DV, ET0_ERXD3 to ET0_ERXD0, and ET0_RX_ER
	ET0_COL	Input	Input collision detection signal
	ET0_WOL	Output	Receive Magic packets
	ET0_MDC	Output	Output reference clock signal for information transfer through ET0_MDIO.
	ET0_MDIO	I/O	Input or output bidirectional signal for exchange of management data with PHY-LSI
SDHI	SD0CLK, SD1CLK	Output	SD clock output pins
	SD0CMD, SD1CMD	I/O	Command output pin and response input signal pins
	SD0DAT0 to SD0DAT7, SD1DAT0 to SD1DAT7	I/O	SD and MMC data bus pins
	SD0CD, SD1CD	Input	SD card detection pins
	SD0WP, SD1WP	Input	SD write-protect signals
Analog power supply	AVCC0	Input	Analog voltage supply pin. This is used as the analog power supply for the respective modules. Supply this pin with the same voltage as the VCC pin.
	AVSS0	Input	Analog ground pin. This is used as the analog ground for the respective modules. Supply this pin with the same voltage as the VSS pin.
	VREFH0	Input	Analog reference voltage supply pin for the ADC12 (unit 0). Connect this pin to VCC when not using the ADC12 (unit 0) and sample-and-hold circuit for AN000 to AN002.
	VREFL0	Input	Analog reference ground pin for the ADC12. Connect this pin to VSS when not using the ADC12 (unit 0) and sample-and-hold circuit for AN000 to AN002
	VREFH	Input	Analog reference voltage supply pin for the ADC12 (unit 1) and D/A Converter. Connect this pin to VCC when not using the ADC12 (unit 1), sample-and-hold circuit for AN100 to AN102, and D/A Converter.
	VREFL	Input	Analog reference ground pin for the ADC12 and D/A Converter. Connect this pin to VSS when not using the ADC12 (unit 1), sample-and-hold circuit for AN100 to AN102, and D/A Converter.

Table 1.16 引脚功能(4of5)

Function	Signal	I/O	Description
ETHERC	REF50CK0	Input	50MHz参考时钟。该引脚输入RMII模式下发送接收时序的参考信号。
	RMII0_CRS_DV	Input	在RMII模式下指示RMII0_RXD1和RMII0_RXD0上的载波检测信号和有效接收数据
	RMII0_TXD0, RMII0_TXD1	Output	RMII模式下的2位发送数据
	RMII0_RXD0, RMII0_RXD1	Input	RMII模式下的2位接收数据
	RMII0_TXD_EN	Output	RMII模式下数据发送使能信号的输出引脚
	RMII0_RX_ER	Input	表示在RMII模式下接收数据时发生错误
	ET0_CRS	Input	载波检测数据接收使能信号
	ET0_RX_DV	Input	指示ET0_ERXD3到ET0_ERXD0上的有效接收数据
	ET0_EXOUT	Output	通用外部输出引脚
	ET0_LINKSTA	Input	从PHY-LSI输入链路状态
	ET0_ETXD0 to ET0_ETXD3	Output	4位MII传输数据
	ET0_ERXD0 to ET0_ERXD3	Input	4位MII接收数据
	ET0_TX_EN	Output	发送使能信号。用作指示在ET0_ETXD3到ET0_ETXD0上传输数据已准备好的信号
	ET0_TX_ER	Output	发送错误引脚。作为信号通知PHY_LSI传输过程中的错误
	ET0_RX_ER	Input	接收错误引脚。在接收过程中用作识别错误的信号
	ET0_TX_CLK	Input	发送时钟引脚。该引脚输入参考信号用于从ET0_TX_EN、ET0_ETXD3到ET0_ETXD0和ET0_TX_ER
	ET0_RX_CLK	Input	接收时钟引脚。该引脚输入用于输入时序的参考信号ET0_RX_DV、ET0_ERXD3到ET0_ERXD0和ET0_RX_ER
	ET0_COL	Input	输入碰撞检测信号
	ET0_WOL	Output	接收魔术包
	ET0_MDC	Output	通过ET0_MDIO输出用于信息传输的参考时钟信号。
	ET0_MDIO	I/O	用于交换管理数据的输入或输出双向信号PHY-LSI
SDHI	SD0CLK, SD1CLK	Output	SD时钟输出引脚
	SD0CMD, SD1CMD	I/O	命令输出引脚和响应输入信号引脚
	SD0DAT0 to SD0DAT7, SD1DAT0 to SD1DAT7	I/O	SD和MMC数据总线引脚
	SD0CD, SD1CD	Input	SD卡检测引脚
	SD0WP, SD1WP	Input	SD write-protect signals
模拟电源	AVCC0	Input	模拟电压电源引脚。这用作各个模块的模拟电源。为该引脚提供与VCC引脚相同的电压。
	AVSS0	Input	模拟接地引脚。这用作各个模块的模拟地。为该引脚提供与VSS引脚相同的电压。
	VREFH0	Input	ADC12（单元0）的模拟参考电压电源引脚。当不使用ADC12（单元0）和AN000到AN002的采样保持电路时，将此引脚连接到VCC。
	VREFL0	Input	ADC12的模拟参考接地引脚。不使用ADC12（单元0）和AN000至AN002的采样保持电路时，将此引脚连接到VSS
	VREFH	Input	ADC12（单元1）和DA的模拟参考电压电源引脚转换器。不使用ADC12（单元1）、AN100至AN102的采样保持电路和DA转换器时，将此引脚连接到VCC。
	VREFL	Input	ADC12和DA转换器的模拟参考接地引脚。不使用ADC12（单元1）、AN100至AN102的采样保持电路和DA转换器时，将此引脚连接到VSS。

Table 1.16 Pin functions (5 of 5)

Function	Signal	I/O	Description
ADC12	AN000 to AN007, AN016 to AN020	Input	Input pins for the analog signals to be processed by the ADC12
	AN100 to AN103, AN105 to AN107, AN116 to AN119	Input	
	ADTRG0	Input	Input pins for the external trigger signals that start the A/D conversion
	ADTRG1	Input	
	PGAVSS000/PGAVSS100	Input	Differential input pins
DAC12	DA0, DA1	Output	Output pins for the analog signals processed by the D/A converter
ACMPHS	VCOUT	Output	Comparator output pin
	IVREF0 to IVREF3	Input	Reference voltage input pins for comparator
	IVCMP0 to IVCMP2	Input	Analog voltage input pins for comparator
CTSU	TS00 to TS17	Input	Capacitive touch detection pins (touch pins)
	TSCAP	-	Secondary power supply pin for the touch driver
I/O ports	P000 to P007	Input	General-purpose input pins
	P008 to P010, P014, P015	I/O	General-purpose input/output pins
	P100 to P115	I/O	General-purpose input/output pins
	P200	Input	General-purpose input pin
	P201 to P214	I/O	General-purpose input/output pins
	P300 to P315	I/O	General-purpose input/output pins
	P400 to P415	I/O	General-purpose input/output pins
	P500 to P508, P511 to P513	I/O	General-purpose input/output pins
	P600 to P615	I/O	General-purpose input/output pins
	P700 to P713	I/O	General-purpose input/output pins
	P800 to P806	I/O	General-purpose input/output pins
	P900, P901, P905 to P908	I/O	General-purpose input/output pins
	PA00, PA01, PA08 to PA10	I/O	General-purpose input/output pins
	PB00, PB01	I/O	General-purpose input/output pins
GLCDC	LCD_DATA23 to LCD_DATA00	Output	Data output pins for panel
	LCD_TCON3 to LCD_TCON0	Output	Output pins for panel timing adjustment
	LCD_CLK	Output	Panel clock output pin
	LCD_EXTCLK	Input	Panel clock source input pin
PDC	PIXCLK	Input	Image transfer clock pin
	VSYNC	Input	Vertical synchronization signal pin
	HSYNC	Input	Horizontal synchronization signal pin
	PIXD0 to PIXD7	Input	8-bit image data pins
	PCKO	Output	Output pin for dot clock

Table 1.16 引脚功能（5个中的5个）

Function	Signal	I/O	Description
ADC12	AN000 to AN007, AN016 to AN020	Input	ADC12处理的模拟信号的输入引脚
	AN100 to AN103, AN105 to AN107, AN116 to AN119	Input	
	ADTRG0	Input	用于启动AD转换的外部触发信号的输入引脚
	ADTRG1	Input	
	PGAVSS000/PGAVSS100	Input	差分输入引脚
DAC12	DA0, DA1	Output	DA转换器处理的模拟信号的输出引脚
ACMPHS	VCOUT	Output	比较器输出引脚
	IVREF0 to IVREF3	Input	比较器的参考电压输入引脚
	IVCMP0 to IVCMP2	Input	比较器的模拟电压输入引脚
CTSU	TS00 to TS17	Input	电容式触摸检测引脚（触摸引脚）
	TSCAP	-	触摸驱动器的辅助电源引脚
I/O ports	P000 to P007	Input	通用输入引脚
	P008 to P010, P014, P015	I/O	General-purpose input/output pins
	P100 to P115	I/O	General-purpose input/output pins
	P200	Input	通用输入引脚
	P201 to P214	I/O	General-purpose input/output pins
	P300 to P315	I/O	General-purpose input/output pins
	P400 to P415	I/O	General-purpose input/output pins
	P500 to P508, P511 to P513	I/O	General-purpose input/output pins
	P600 to P615	I/O	General-purpose input/output pins
	P700 to P713	I/O	General-purpose input/output pins
	P800 to P806	I/O	General-purpose input/output pins
	P900, P901, P905 to P908	I/O	General-purpose input/output pins
	PA00, PA01, PA08 to PA10	I/O	General-purpose input/output pins
	PB00, PB01	I/O	General-purpose input/output pins
GLCDC	LCD_DATA23 to LCD_DATA00	Output	面板数据输出引脚
	LCD_TCON3 to LCD_TCON0	Output	用于面板时序调整的输出引脚
	LCD_CLK	Output	面板时钟输出引脚
	LCD_EXTCLK	Input	面板时钟源输入引脚
PDC	PIXCLK	Input	图像传输时钟引脚
	VSYNC	Input	垂直同步信号引脚
	HSYNC	Input	水平同步信号引脚
	PIXD0 to PIXD7	Input	8位图像数据引脚
	PCKO	Output	点时钟的输出引脚

1.6 Pin Assignments

Figure 1.3 to Figure 1.7 show the pin assignments.

R7FA6M3XX2CBG

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	
15	P407	P409	P411	P414	P708	USBHS_DM	PVSS_USBHS	P212/EXTAL	XCIN	VCL0	P707	P703	P700	P405	P401	15
14	USB_DP	USB_DM	P410	P412	P415	USBHS_DP	AVSS_USBHS	P213/XTAL	XCOUT	VBATT	P706	P701	P406	P402	P512	14
13	P204	VCC_USB	VSS_USB	P408	P413	VCC_USBHS	USBHS_RREF	AVCC_USBHS	VSS	PB01	P704	P404	P400	P511	P805	13
12	P313	P202	P207	P206	P205	VSS1_USBHS	VSS2_USBHS	VCC	PB00	P705	P702	P403	P513	P806	P000	12
11	P900	P315	P314	P203								VCC	P001	P004	P002	11
10	P214	P211	P901	VSS								VSS	P006	P008	P005	10
9	P210	P209	RES	VCC								P009	AVSS0	VREFL0	VREFH0	9
8	P208	P201/MD	P200	P908								P010	AVCC0	VREFL	VREFH	8
7	P906	P905	P312	P907								VCC	VSS	P015	P014	7
6	P310	P309	P307	P311								P007	P507	P505	P508	6
5	P308	P305	VSS	VCC								P003	P503	P504	P506	5
4	P306	P304	P300/TCK/SWCLK	P111	VSS	P613	PA09	PA00	P607	VCC	VSS	VSS	VCC	P501	P502	4
3	P303	P302	P108/TMS SWDIO	P110/TDI	VCC	P610	VCC	VSS	P604	P603	P105	P102	P800	P804	P500	3
2	P301	P112	P114	P608	P611	P614	PA10	PA01	P605	P601	P107	P104	P101	P802	P803	2
1	P109/TDO	P113	P115	P609	P612	P615	PA08	VCL	P606	P602	P600	P106	P103	P100	P801	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	

Figure 1.3 Pin assignment for 176-pin BGA (top view)

1.6 引脚分配

图1.3至图1.7显示了引脚分配。

R7FA6M3XX2CBG

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	
15	P407	P409	P411	P414	P708	USBHS_DM	PVSS_USBHS	P212/EXTAL	XCIN	VCL0	P707	P703	P700	P405	P401	15
14	USB_DP	USB_DM	P410	P412	P415	USBHS_DP	AVSS_USBHS	P213/XTAL	XCOUT	VBATT	P706	P701	P406	P402	P512	14
13	P204	VCC_USB	VSS_USB	P408	P413	VCC_USBHS	USBHS_RREF	AVCC_USBHS	VSS	PB01	P704	P404	P400	P511	P805	13
12	P313	P202	P207	P206	P205	VSS1_USBHS	VSS2_USBHS	VCC	PB00	P705	P702	P403	P513	P806	P000	12
11	P900	P315	P314	P203								VCC	P001	P004	P002	11
10	P214	P211	P901	VSS								VSS	P006	P008	P005	10
9	P210	P209	RES	VCC								P009	AVSS0	VREFL0	VREFH0	9
8	P208	P201/MD	P200	P908								P010	AVCC0	VREFL	VREFH	8
7	P906	P905	P312	P907								VCC	VSS	P015	P014	7
6	P310	P309	P307	P311								P007	P507	P505	P508	6
5	P308	P305	VSS	VCC								P003	P503	P504	P506	5
4	P306	P304	P300/TCK/SWCLK	P111	VSS	P613	PA09	PA00	P607	VCC	VSS	VSS	VCC	P501	P502	4
3	P303	P302	P108/TMS SWDIO	P110/TDI	VCC	P610	VCC	VSS	P604	P603	P105	P102	P800	P804	P500	3
2	P301	P112	P114	P608	P611	P614	PA10	PA01	P605	P601	P107	P104	P101	P802	P803	2
1	P109/TDO	P113	P115	P609	P612	P615	PA08	VCL	P606	P602	P600	P106	P103	P100	P801	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	

Figure 1.3 176引脚BGA的引脚分配（顶视图）

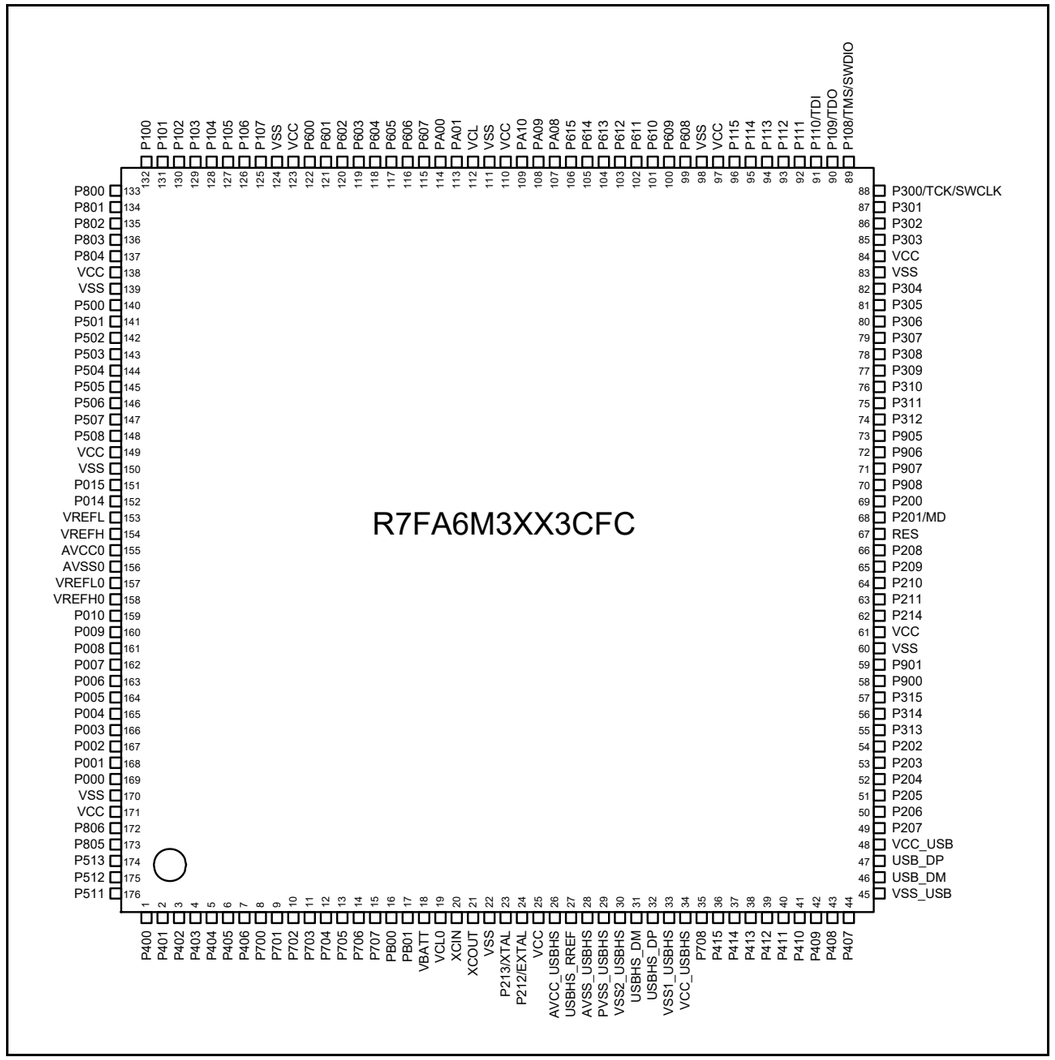


Figure 1.4 Pin assignment for 176-pin LQFP (top view)

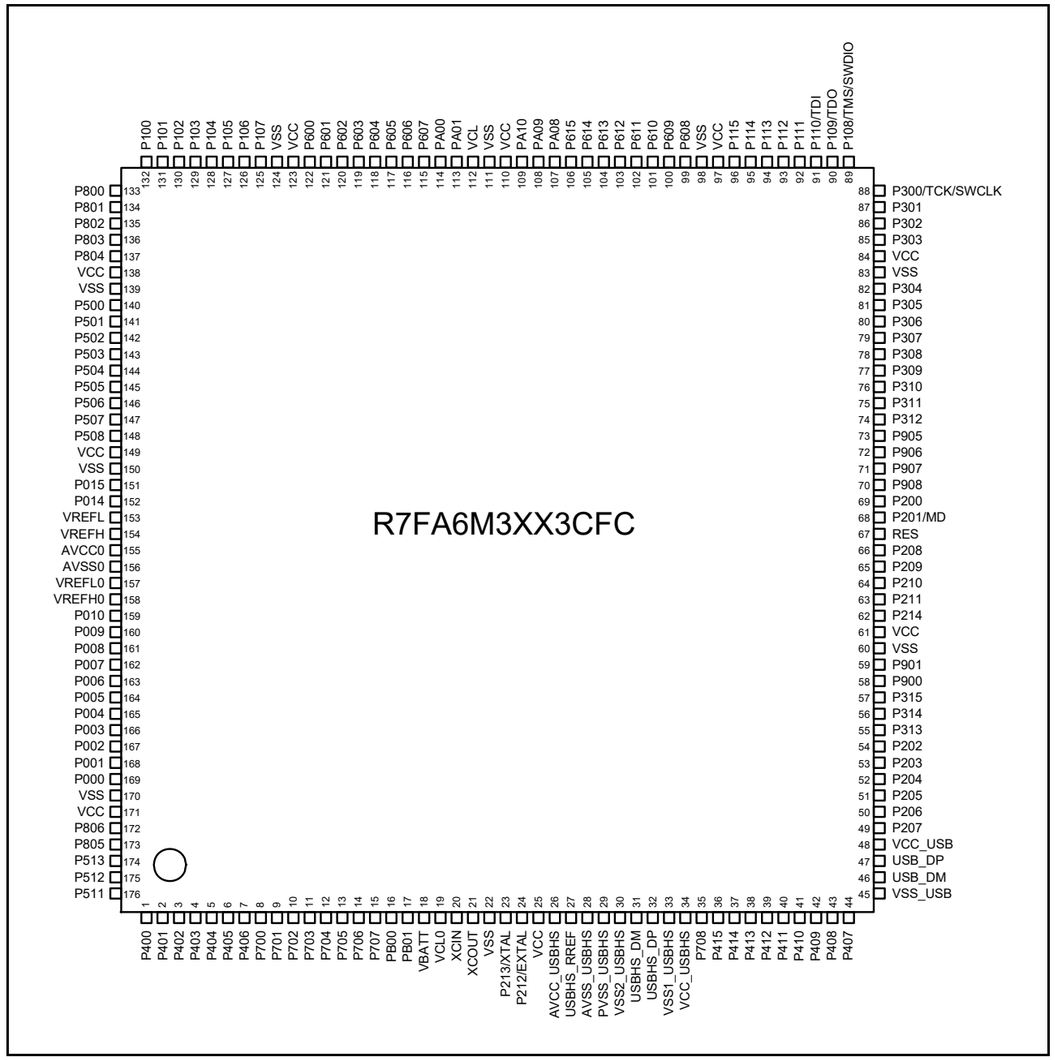


Figure 1.4 176引脚LQFP的引脚分配（俯视图）

R7FA6M3XX2CLK

	A	B	C	D	E	F	G	H	J	K	L	M	N	
13	P407	P409	P412	P708	P711	VCC	P212 /EXTAL	XCIN	VCL0	P702	P405	P402	P400	13
12	USB_DM	USB_DP	P410	P414	P710	VSS	P213 /XTAL	XCOUT	VBATT	P701	P404	P511	VCC	12
11	VCC_ USB	VSS_ USB	P207	P411	P415	P712	P705	P704	P703	P403	P401	P512	VSS	11
10	P205	P206	P204	P408	P413	P709	P713	P700	P406	P003	P000	P002	P001	10
9	P203	P313	P202	VSS						P004	P006	P009	P008	9
8	P214	P211	P200	VCC						P005	AVSS0	VREFL0	VREFH0	8
7	P210	P209	RES	P310						P007	AVCC0	VREFL	VREFH	7
6	P208	P201/MD	P312	P305						P505	P506	P015	P014	6
5	P309	P311	P308	P303	NC					P503	P504	VSS	VCC	5
4	P307	P306	P304	P109/TDO	P114	P608	P604	P600	P105	P500	P502	P501	P508	4
3	VSS	VCC	P301	P112	P115	P610	P614	P603	P107	P106	P104	VSS	VCC	3
2	P302	P300/TCK /SWCLK	P111	VCC	P609	P612	VSS	P605	P601	VCC	P800	P101	P801	2
1	P108/TMS /SWDIO	P110/TDI	P113	VSS	P611	P613	VCC	VCL	P602	VSS	P103	P102	P100	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	

Figure 1.5 Pin assignment for 145-pin LGA (top view)

R7FA6M3XX2CLK

	A	B	C	D	E	F	G	H	J	K	L	M	N	
13	P407	P409	P412	P708	P711	VCC	P212 /EXTAL	XCIN	VCL0	P702	P405	P402	P400	13
12	USB_DM	USB_DP	P410	P414	P710	VSS	P213 /XTAL	XCOUT	VBATT	P701	P404	P511	VCC	12
11	VCC_ USB	VSS_ USB	P207	P411	P415	P712	P705	P704	P703	P403	P401	P512	VSS	11
10	P205	P206	P204	P408	P413	P709	P713	P700	P406	P003	P000	P002	P001	10
9	P203	P313	P202	VSS						P004	P006	P009	P008	9
8	P214	P211	P200	VCC						P005	AVSS0	VREFL0	VREFH0	8
7	P210	P209	RES	P310						P007	AVCC0	VREFL	VREFH	7
6	P208	P201/MD	P312	P305						P505	P506	P015	P014	6
5	P309	P311	P308	P303	NC					P503	P504	VSS	VCC	5
4	P307	P306	P304	P109/TDO	P114	P608	P604	P600	P105	P500	P502	P501	P508	4
3	VSS	VCC	P301	P112	P115	P610	P614	P603	P107	P106	P104	VSS	VCC	3
2	P302	P300/TCK /SWCLK	P111	VCC	P609	P612	VSS	P605	P601	VCC	P800	P101	P801	2
1	P108/TMS /SWDIO	P110/TDI	P113	VSS	P611	P613	VCC	VCL	P602	VSS	P103	P102	P100	1
	A	B	C	D	E	F	G	H	J	K	L	M	N	

Figure 1.5 145引脚LGA的引脚分配（俯视图）

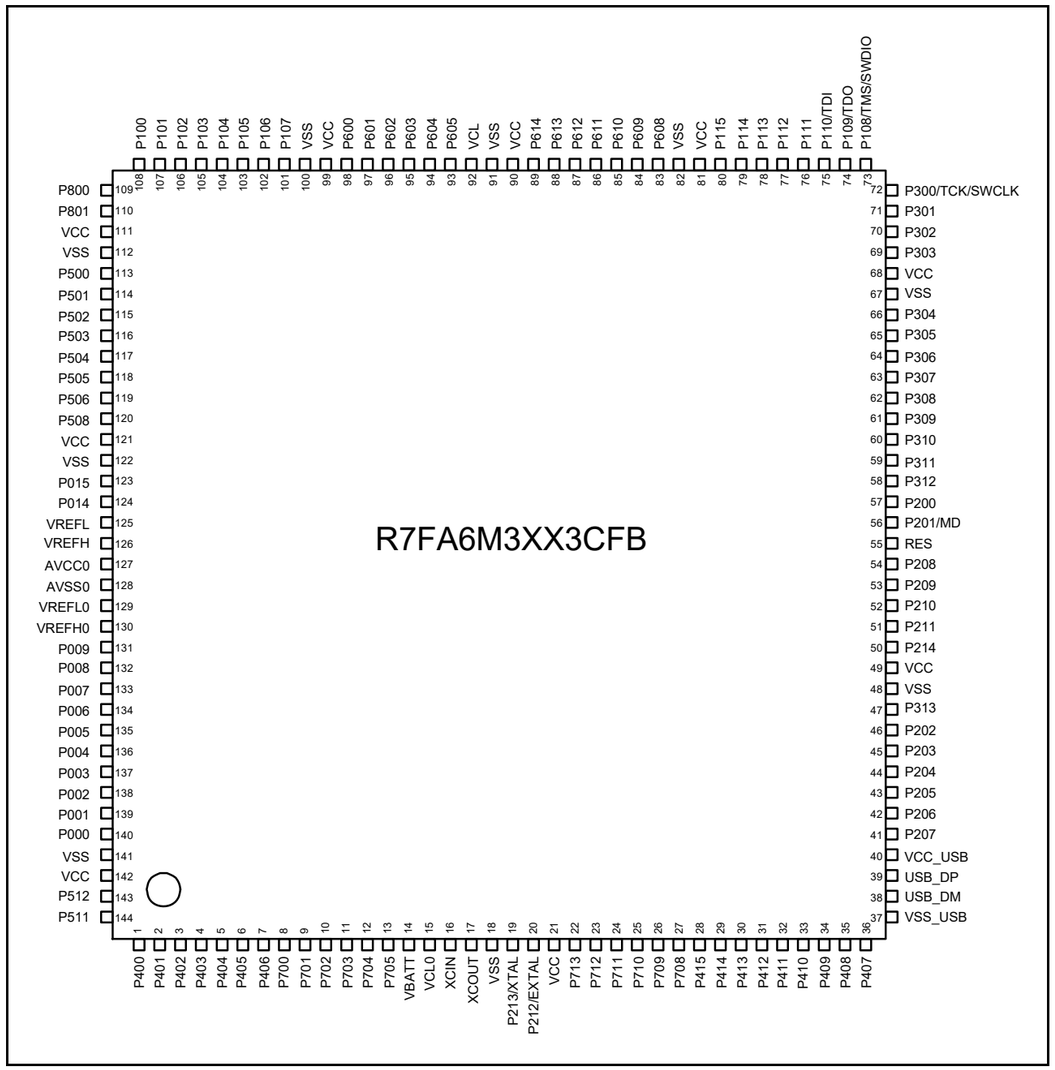


Figure 1.6 Pin assignment for 144-pin LQFP (top view)

RA6M3 Group 1. Overview

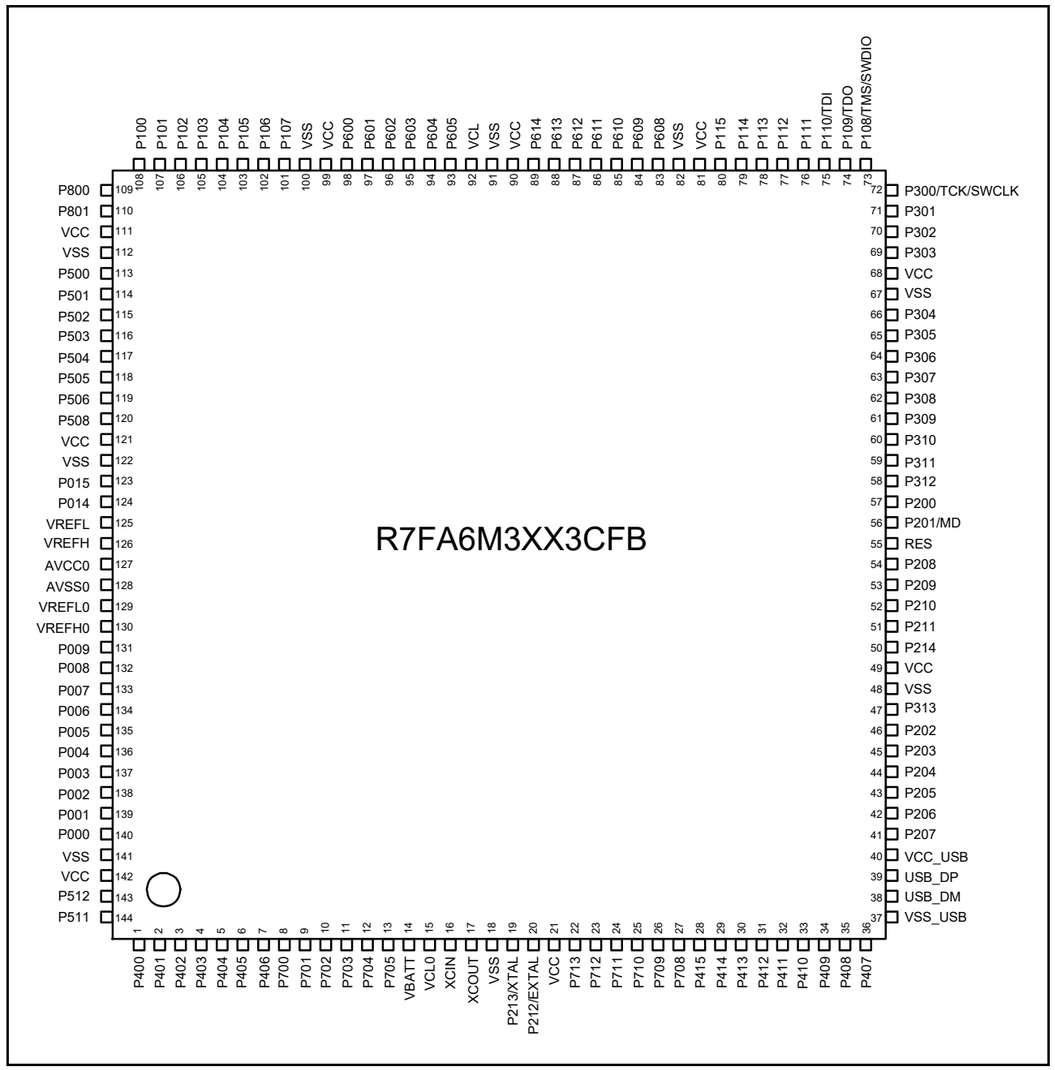


Figure 1.6 144引脚LQFP的引脚分配（俯视图）

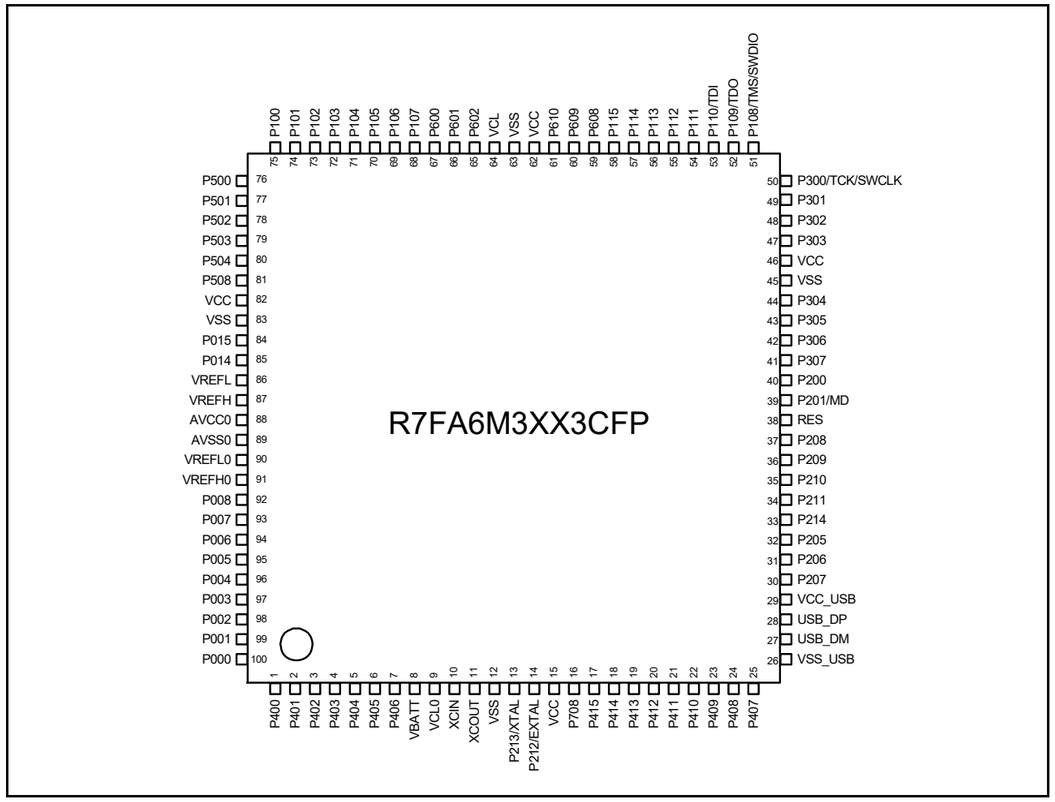


Figure 1.7 Pin assignment for 100-pin LQFP (top view)

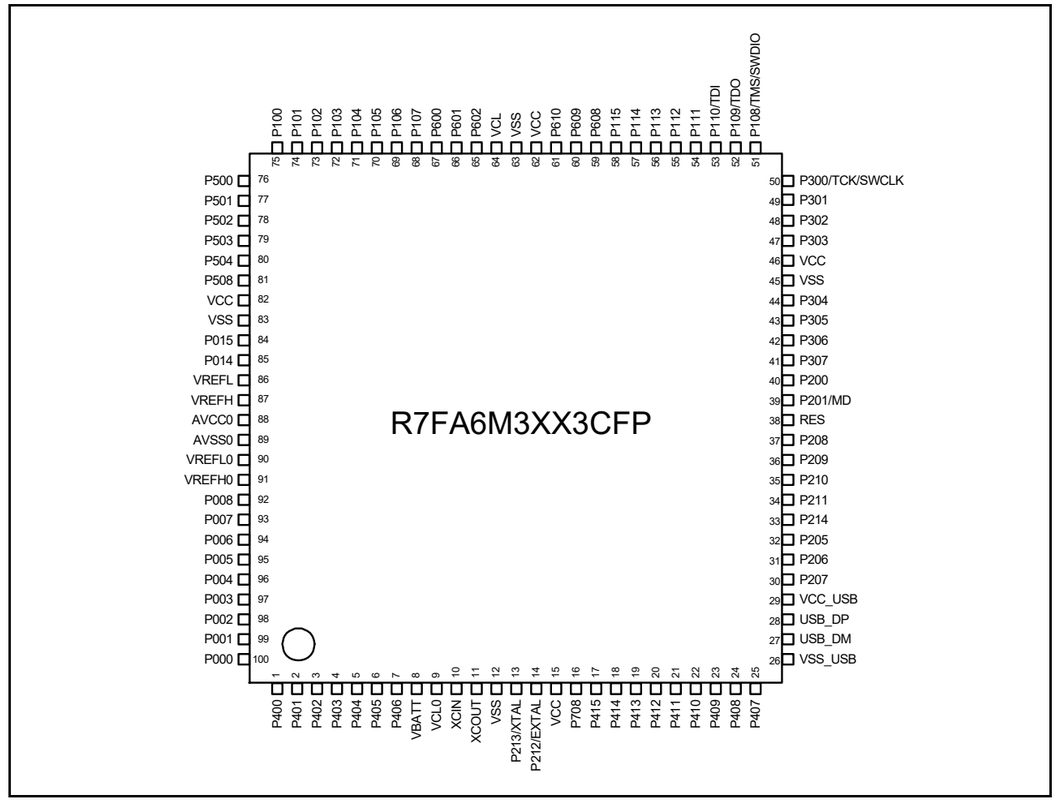


Figure 1.7 100引脚LQFP的引脚分配（顶视图）

1.7 Pin Lists

Pin number					Power, System, Clock, Debug, CAC	Interrupt	I/O port	Extbus		Timers				Communication interfaces									Analog		HMI	
BGA176	LQFP176	LGA145	LQFP144	LQFP100				External bus	SDRAM	AGT	GPT	GPT	RTC	USBFS, CAN	SCI0,2,4,6,8 (30 MHz)	SCI1,3,5,7,9 (30 MHz)	IIC	SPI, QSPI	SSIE	ETHERC (MII) (25 MHz)	ETHERC (RMII) (50 MHz)	USBHS	SDHI	ADC12	DAC12, ACMPHS	CTSU	GLCDC, PDC
N13	1	N13	1	1	-	IRQ0	P400	-	-	AGTIO1	-	GTIOC 6A	-	-	SCK4	SCK7	SCL0 _A	-	AUDIO _CLK	ET0_W OL	ET0_ WOL	-	-	ADTRG 1	-	-	-
R15	2	L11	2	2	-	IRQ5-DS	P401	-	-	-	GTETRGA	GTIOC 6B	-	CTX0	CTS4_ RTS4/ SS4	TXD7/ MOSI7 /SDA7	SDA0 _A	-	-	ET0_M DC	ET0_M DC	-	-	-	-	-	-
P14	3	M13	3	3	CACREF	IRQ4-DS	P402	-	-	AGTIO0/ AGTIO1	-	-	RTC IC0	CRX0	-	RXD7/ MISO7 /SCL7	-	-	AUDIO _CLK	ET0_M DIO	ET0_M DIO	-	-	-	-	-	VSYNC
M12	4	K11	4	4	-	-	P403	-	-	AGTIO0/ AGTIO1	-	GTIOC 3A	RTC IC1	-	-	CTS7_ RTS7/ SS7	-	-	SSIBC K0_A	ET0_LI NKSTA	ET0_LI NKST A	-	SD1 DAT7 _B	-	-	-	PIXD7
M13	5	L12	5	5	-	-	P404	-	-	-	-	GTIOC 3B	RTC IC2	-	-	-	-	-	SSILR CK0/S SIFS0_ A	ET0_EX OUT	ET0_E XOUT	-	SD1 DAT6 _B	-	-	-	PIXD6
P15	6	L13	6	6	-	-	P405	-	-	-	-	GTIOC 1A	-	-	-	-	-	-	SSITX D0_A	ET0_TX _EN	RMII0_ TXD_E N_B	-	SD1 DAT5 _B	-	-	-	PIXD5
N14	7	J10	7	7	-	-	P406	-	-	-	-	GTIOC 1B	-	-	-	-	-	SSLB3 _C	SSIRX D0_A	ET0_RX _ER	RMII0_ TXD1_ B	-	SD1 DAT4 _B	-	-	-	PIXD4
N15	8	H10	8	-	-	-	P700	-	-	-	-	GTIOC 5A	-	-	-	-	-	MISOB _C	-	ET0_ET XD1	RMII0_ TXD0_ B	-	SD1 DAT3 _B	-	-	-	PIXD3
M14	9	K12	9	-	-	-	P701	-	-	-	-	GTIOC 5B	-	-	-	-	-	MOSIB _C	-	ET0_ET XD0	REF50 CK0_B	-	SD1 DAT2 _B	-	-	-	PIXD2
L12	10	K13	10	-	-	-	P702	-	-	-	-	GTIOC 6A	-	-	-	-	-	RSPC KB_C	-	ET0_ER XD1	RMII0_ RXD0_ B	-	SD1 DAT1 _B	-	-	-	PIXD1
M15	11	J11	11	-	-	-	P703	-	-	-	-	GTIOC 6B	-	-	-	-	-	SSLB0 _C	-	ET0_ER XD0	RMII0_ RXD1_ B	-	SD1 DAT0 _B	-	VCOUT	-	PIXD0
L13	12	H11	12	-	-	-	P704	-	-	AGTO0	-	-	-	CTX0	-	-	-	SSLB1 _C	-	ET0_RX _CLK	RMII0_ RX_E R_B	-	SD1 CLK_ B	-	-	-	HSYNC
K12	13	G11	13	-	-	-	P705	-	-	AGTIO0	-	-	-	CRX0	-	-	-	SSLB2 _C	-	ET0_C RS	RMII0_ CRS_ DV_B	-	SD1 CMD _B	-	-	-	PIXCLK
L14	14	-	-	-	-	IRQ7	P706	-	-	-	-	-	-	-	-	RXD3/ MISO3 /SCL3	-	-	-	-	-	USB HS_ OVR CUR B	SD1 CD_ B	-	-	-	-
L15	15	-	-	-	-	IRQ8	P707	-	-	-	-	-	-	-	-	TXD3/ MOSI3 /SDA3	-	-	-	-	-	USB HS_ OVR CUR A	SD1 WP_ B	-	-	-	-
J12	16	-	-	-	-	-	PB00	-	-	-	-	-	-	-	-	SCK3	-	-	-	-	-	USB HS_ VBU SEN	-	-	-	-	-
K13	17	-	-	-	-	-	PB01	-	-	-	-	-	-	-	-	CTS3_ RTS3/ SS3	-	-	-	-	-	USB HS_ VBU S	-	-	-	-	-
K14	18	J12	14	8	VBATT	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
K15	19	J13	15	9	VCL0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
J15	20	H13	16	10	XCIN	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
J14	21	H12	17	11	XCOUT	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
J13	22	F12	18	12	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
H14	23	G12	19	13	XTAL	IRQ2	P213	-	-	-	GTETRGC	GTIOC 0A	-	-	-	TXD1/ MOSI1 /SDA1	-	-	-	-	-	-	-	ADTRG 1	-	-	-
H15	24	G13	20	14	EXTAL	IRQ3	P212	-	-	AGTEE1	GTETRGD	GTIOC 0B	-	-	-	RXD1/ MISO1 /SCL1	-	-	-	-	-	-	-	-	-	-	-
H12	25	F13	21	15	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
H13	26	-	-	-	AVCC_U SBHS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
G13	27	-	-	-	USBHS_ RREF	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
G14	28	-	-	-	AVSS_U SBHS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
G15	29	-	-	-	PVSS_U SBHS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
G12	30	-	-	-	VSS2_U SBHS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
F15	31	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	USB HS_ DM	-	-	-	-	-
F14	32	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	USB HS_ DP	-	-	-	-	-
F12	33	-	-	-	VSS1_U SBHS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
F13	34	-	-	-	VCC_US BHS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
-	-	G10	22	-	-	-	P713	-	-	AGTOA0	-	GTIOC 2A	-	-	-	-	-	-	-	-	-	-	-	-	-	TS17	-

1.7 引脚列表

针号					电源系统，时钟，调试，CAC			Extbus		Timers				通讯接口									Analog		HMI	
BGA176	LQFP176	LGA145	LQFP144	LQFP100		Interrupt	I/O port	外部总线	SDRAM	AGT	GPT	GPT	RTC	USBFS, CAN	SCI0,2,4,6,8 (30 MHz)	SCI1,3,5,7,9 (30 MHz)	IIC	SPI, QSPI	SSIE	ETHERC (MII) (25 MHz)	ETHERC (RMII) (50 MHz)	USBHS	SDHI	ADC12	DAC12, ACMPHS	CTSU	GLCDC, PDC
N13	1	N13	1	1	-	IRQ0	P400	-	-	AGTIO1	-	GTIOC 6A	-	-	SCK4	SCK7	SCL0 _A	-	AUDIO _CLK	ET0_W OL	ET0_ WOL	-	-	ADTRG 1	-	-	-
R15	2	L11	2	2	-	IRQ5-DS	P401	-	-	-	GTETRGA	GTIOC 6B	-	CTX0	CTS4_ RTS4/ SS4	TXD7/ MOSI7 /SDA7	SDA0 _A	-	-	ET0_M DC	ET0_M DC	-	-	-	-	-	-
P14	3	M13	3	3	CACREF	IRQ4-DS	P402	-	-	AGTIO0/ AGTIO1	-	-	RTC IC0	CRX0	-	RXD7/ MISO7 /SCL7	-	-	AUDIO _CLK	ET0_M DIO	ET0_M DIO	-	-	-	-	-	VSYNC
M12	4	K11	4	4	-	-	P403	-	-	AGTIO0/ AGTIO1	-	GTIOC 3A	RTC IC1	-	-	CTS7_ RTS7/ SS7	-	-	SSIBC K0_A	ET0_LI NKSTA	ET0_LI NKST A	-	SD1 DAT7 _B	-	-	-	PIXD7
M13	5	L12	5	5	-	-	P404	-	-	-	-	GTIOC 3B	RTC IC2	-	-	-	-	-	SSILR CK0/S SIFS0_ A	ET0_EX OUT	ET0_E XOUT	-	SD1 DAT6 _B	-	-	-	PIXD6
P15	6	L13	6	6	-	-	P405	-	-	-	-	GTIOC 1A	-	-	-	-	-	-	SSITX D0_A	ET0_TX _EN	RMII0_ TXD_E N_B	-	SD1 DAT5 _B	-	-	-	PIXD5
N14	7	J10	7	7	-	-	P406	-	-	-	-	GTIOC 1B	-	-	-	-	-	SSLB3 _C	SSIRX D0_A	ET0_RX _ER	RMII0_ TXD1_ B	-	SD1 DAT4 _B	-	-	-	PIXD4
N15	8	H10	8	-	-	-	P700	-	-	-	-	GTIOC 5A	-	-	-	-	-	MISOB _C	-	ET0_ET XD1	RMII0_ TXD0_ B	-	SD1 DAT3 _B	-	-	-	PIXD3
M14	9	K12	9	-	-	-	P701	-	-	-	-	GTIOC 5B	-	-	-	-	-	MOSIB _C	-	ET0_ET XD0	REF50 CK0_B	-	SD1 DAT2 _B	-	-	-	PIXD2
L12	10	K13	10	-	-	-	P702	-	-	-	-	GTIOC 6A	-	-	-	-	-	RSPC KB_C	-	ET0_ER XD1	RMII0_ RXD0_ B	-	SD1 DAT1 _B	-	-	-	PIXD1
M15	11	J11	11	-	-	-	P703	-	-	-	-	GTIOC 6B	-	-	-	-	-	SSLB0 _C	-	ET0_ER XD0	RMII0_ RXD1_ B	-	SD1 DAT0 _B	-	VCOUT	-	PIXD0
L13	12	H11	12	-	-	-	P704	-	-	AGTO0	-	-	-	CTX0	-	-	-	SSLB1 _C	-	ET0_RX _CLK	RMII0_ RX_E R_B	-	SD1 CLK_ B	-	-	-	HSYNC
K12	13	G11	13	-	-	-	P705	-	-	AGTIO0	-	-	-	CRX0	-	-	-	SSLB2 _C	-	ET0_C RS	RMII0_ CRS_ DV_B	-	SD1 CMD _B	-	-	-	PIXCLK
L14	14	-	-	-	-	IRQ7	P706	-	-	-	-	-	-	-	-	RXD3/ MISO3 /SCL3	-	-	-	-	-	USB HS_ OVR CUR B	SD1 CD_ B	-	-	-	-
L15	15	-	-	-	-	IRQ8	P707	-	-	-	-	-	-	-	-	TXD3/ MOSI3 /SDA3	-	-	-	-	-	USB HS_ OVR CUR A	SD1 WP_ B	-	-	-	-
J12	16	-	-	-	-	-	PB00	-	-	-	-	-	-	-	-	SCK3	-	-	-	-	-	USB HS_ VBU SEN	-	-	-	-	-
K13	17	-	-	-	-	-	PB01	-	-	-	-	-	-	-	-	CTS3_ RTS3/ SS3	-	-	-	-	-	USB HS_ VBU S	-	-	-	-	-
K14	18	J12	14	8	VBATT	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
K15	19	J13	15	9	VCL0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
J15	20	H13	16	10	XCIN	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
J14	21	H12	17	11	XCOUT	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
J13	22	F12	18	12	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
H14	23	G12	19	13	XTAL	IRQ2	P213	-	-	-	GTETRGC	GTIOC 0A	-	-	-	TXD1/ MOSI1 /SDA1	-	-	-	-	-	-	-	ADTRG 1	-	-	-
H15	24	G13	20	14	EXTAL	IRQ3	P212	-	-	AGTEE1	GTETRGD	GTIOC 0B	-	-	-	RXD1/ MISO1 /SCL1	-	-	-	-	-	-	-	-	-	-	-
H12	25	F13	21	15	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
H13	26	-	-	-	AVCC_U SBHS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
G13	27	-	-	-	USBHS_ RREF	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
G14	28	-	-	-	AVSS_U SBHS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
G15	29	-	-	-	PVSS_U SBHS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
G12	30	-	-	-	VSS2_U SBHS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
F15	31	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	USB HS_ DM	-	-	-	-	-
F14	32	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	USB HS_ DP	-	-	-	-	-
F12	33	-	-	-	VSS1_U SBHS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
F13	34	-	-	-	VCC_US BHS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
-	-	G10	22	-	-	-	P713	-	-	AGTOA0	-	GTIOC 2A	-	-	-	-	-	-	-	-	-	-	-	-	-	TS17	-

Pin number								Extbus		Timers				Communication interfaces										Analog		HMI	
BGA176	LQFP176	LGA145	LQFP144	LQFP100	Power, System, Clock, Debug, CAC	Interrupt	I/O port	External bus	SDRAM	AGT	GPT	GPT	RTC	USBFS, CAN	SCI0,2,4,6,8 (30 MHz)	SCI1,3,5,7,9 (30 MHz)	IIC	SPI, QSPI	SSIE	ETHERC (MII) (25 MHz)	ETHERC (RMII) (50 MHz)	USBHS	SDHI	ADC12	DAC12, ACMPHS	CTSU	GLCDC, PDC
-	-	F11	23	-	-	-	P712	-	-	AGTOB0	-	GTIOC 2B	-	-	-	-	-	-	-	-	-	-	-	-	-	TS16	-
-	-	E13	24	-	-	-	P711	-	-	AGTEE0	-	-	-	-	-	CTS1_ RTS1/ SS1	-	-	-	ET0_TX _CLK	-	-	-	-	-	TS15	-
-	-	E12	25	-	-	-	P710	-	-	-	-	-	-	-	-	SCK1	-	-	-	ET0_TX _ER	-	-	-	-	-	TS14	-
-	-	F10	26	-	-	IRQ10	P709	-	-	-	-	-	-	-	-	TXD1/ MOSI1 /SDA1	-	-	-	ET0_ET XD2	-	-	-	-	-	TS13	-
E15	35	D13	27	16	CACREF	IRQ11	P708	-	-	-	-	-	-	-	-	RXD1/ MISO1 /SCL1	-	SSLA3 _B	AUDIO _CLK	ET0_ET XD3	-	-	-	-	-	TS12	PCKO
E14	36	E11	28	17	-	IRQ8	P415	-	-	-	-	GTIOC 0A	-	USB_ VBUS EN	-	-	-	SSLA2 _B	-	ET0_TX _EN	RMII0_ TXD_E N_A	-	SD0 CD_ A	-	-	TS11	PIXD5
D15	37	D12	29	18	-	IRQ9	P414	-	-	-	-	GTIOC 0B	-	-	-	-	-	SSLA1 _B	-	ET0_RX _ER	RMII0_ TXD1_ A	-	SD0 WP_ A	-	-	TS10	PIXD4
E13	38	E10	30	19	-	-	P413	-	-	-	GTOUUP	-	-	-	CTS0_ RTS0/ SS0	-	-	SSLA0 _B	-	ET0_ET XD1	RMII0_ TXD0_ A	-	SD0 CLK_ A	-	-	TS09	PIXD3
D14	39	C13	31	20	-	-	P412	-	-	AGTEE1	GTOULO	-	-	-	SCK0	-	-	RSPC KA_B	-	ET0_ET XD0	REF50 CK0_A	-	SD0 CMD _A	-	-	TS08	PIX02
C15	40	D11	32	21	-	IRQ4	P411	-	-	AGTOA1	GTOVUP	GTIOC 9A	-	-	TXD0/ MOSI0 /SDA0	CTS3_ RTS3/ SS3	-	MOSIA _B	-	ET0_ER XD1	RMII0_ RXD0_ A	-	SD0 DAT0 _A	-	-	TS07	PIX01
C14	41	C12	33	22	-	IRQ5	P410	-	-	AGTOB1	GTOVLO	GTIOC 9B	-	-	RXD0/ MISO0 /SCL0	SCK3	-	MISOA _B	-	ET0_ER XD0	RMII0_ RXD1_ A	-	SD0 DAT1 _A	-	-	TS06	PIXD0
B15	42	B13	34	23	-	IRQ6	P409	-	-	-	GTOWUP	GTIOC 10A	-	USB_ EXIC EN	-	TXD3/ MOSI3 /SDA3	-	-	-	ET0_RX _CLK	RMII0_ RX_E R_A	USB HS_ EXIC EN	-	-	-	TS05	HSYNC
D13	43	D10	35	24	-	IRQ7	P408	-	-	-	GTOWLO	GTIOC 10B	-	USB_ ID	-	RXD3/ MISO3 /SCL3	SCL0 _B	-	-	ET0_C RS	RMII0_ CRS_ DV_A	USB HS_I D	-	-	-	TS04	PIXCLK
A15	44	A13	36	25	-	-	P407	-	-	AGTIO0	-	-	RTC OUT	USB_ VBUS	CTS4_ RTS4/ SS4	-	SDA0 _B	SSLB3 _A	-	ET0_EX OUT	ET0_E XOUT	-	-	ADTRG 0	-	TS03	-
C13	45	B11	37	26	VSS_US B	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
B14	46	A12	38	27	-	-	-	-	-	-	-	-	-	USB_ DM	-	-	-	-	-	-	-	-	-	-	-	-	-
A14	47	B12	39	28	-	-	-	-	-	-	-	-	-	USB_ DP	-	-	-	-	-	-	-	-	-	-	-	-	-
B13	48	A11	40	29	VCC_US B	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
C12	49	C11	41	30	-	-	P207	A17	-	-	-	-	-	-	-	-	-	SSLB2 _A/QS SL	-	-	-	-	-	-	-	TS02	LCD_DATA 23_B
D12	50	B10	42	31	-	IRQ0-DS	P206	WAIT	-	-	GTIU	-	-	USB_ VBUS EN	RXD4/ MISO4 /SCL4	-	SDA1 _A	SSLB1 _A	SSIDA TA1_A	ET0_LI NKSTA	ET0_LI NKST A	-	SD0 DAT2 _A	-	-	TS01	-
E12	51	A10	43	32	CLKOUT	IRQ1-DS	P205	A16	-	AGTO1	GTIV	GTIOC 4A	-	USB_ OVR CUR A-DS	TXD4/ MOSI4 /SDA4	CTS9_ RTS9/ SS9	SCL1 _A	SSLB0 _A	SSILR CK1/S SIFS1_ A	ET0_W OL	ET0_ WOL	-	SD0 DAT3 _A	-	-	TSCA P	-
A13	52	C10	44	-	CACREF	-	P204	A18	-	AGTIO1	GTIW	GTIOC 4B	-	USB_ OVR CUR B-DS	SCK4	SCK9	SCL0 _B	RSPC KB_A	SSIBC K1_A	ET0_RX _DV	-	-	SD0 DAT4 _A	-	-	TS00	-
D11	53	A9	45	-	-	IRQ2-DS	P203	A19	-	-	-	GTIOC 5A	-	CTX0	CTS2_ RTS2/ SS2	TXD9/ MOSI9 /SDA9	-	MOSIB _A	-	ET0_C OL	-	-	SD0 DAT5 _A	-	-	TSCA P	-
B12	54	C9	46	-	-	IRQ3-DS	P202	WR1/ BC1	-	-	-	GTIOC 5B	-	CRX0	SCK2	RXD9/ MISO9 /SCL9	-	MISOB _A	-	ET0_ER XD2	-	-	SD0 DAT6 _A	-	-	-	LCD_TCO N3_B
A12	55	B9	47	-	-	-	P313	A20	-	-	-	-	-	-	-	-	-	-	-	ET0_ER XD3	-	-	SD0 DAT7 _A	-	-	-	LCD_TCO N2_B
C11	56	-	-	-	-	-	P314	A21	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	ADTRG 0	-	-	LCD_TCO N1_B
B11	57	-	-	-	-	-	P315	A22	-	-	-	-	-	-	RXD4	-	-	-	-	-	-	-	-	-	-	-	LCD_TCO N0_B
A11	58	-	-	-	-	-	P900	A23	-	-	-	-	-	-	TXD4	-	-	-	-	-	-	-	-	-	-	-	LCD_CLK_ B
C10	59	-	-	-	-	-	P901	-	-	AGTIO1	-	-	-	-	SCK4	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA 15_B
D10	60	D9	48	-	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
D9	61	D8	49	-	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
A10	62	A8	50	33	TRCLK	-	P214	-	-	-	GTIU	-	-	-	-	-	-	QSPC LK	-	ET0_M DC	ET0_M DC	-	SD0 CLK_ B	-	-	-	LCD_DATA 22_B
B10	63	B8	51	34	TRDATA 0	-	P211	-	-	-	GTIV	-	-	-	-	-	-	QIO0	-	ET0_M DIO	ET0_M DIO	-	SD0 CMD _B	-	-	-	LCD_DATA 21_B
A9	64	A7	52	35	TRDATA 1	-	P210	-	-	-	GTIW	-	-	-	-	-	-	QIO1	-	ET0_W OL	ET0_ WOL	-	SD0 CD_ B	-	-	-	LCD_DATA 20_B
B9	65	B7	53	36	TRDATA 2	-	P209	-	-	-	GTOVUP	-	-	-	-	-	-	QIO2	-	ET0_EX OUT	ET0_E XOUT	-	SD0 WP_ B	-	-	-	LCD_DATA 19_B

针号								Extbus		Timers				通讯接口										Analog		HMI	
BGA176	LQFP176	LGA145	LQFP144	LQFP100	电源系统、时钟、调试、CAC	Interrupt	I/O port	外线总部	SDRAM	AGT	GPT	GPT	RTC	USBFS, CAN	SCI0,2,4,6,8 (30 MHz)	SCI1,3,5,7,9 (30 MHz)	IIC	SPI, QSPI	SSIE	ETHERC (MII) (25 MHz)	ETHERC (RMII) (50 MHz)	USBHS	SDHI	ADC12	DAC12, ACMPHS	CTSU	GLCDC, PDC
-	-	F11	23	-	-	-	P712	-	-	AGTOB0	-	GTIOC 2B	-	-	-	-	-	-	-	-	-	-	-	-	-	TS16	-
-	-	E13	24	-	-	-	P711	-	-	AGTEE0	-	-	-	-	-	CTS1_ RTS1/ SS1	-	-	-	ET0_TX _CLK	-	-	-	-	-	TS15	-
-	-	E12	25	-	-	-	P710	-	-	-	-	-	-	-	-	SCK1	-	-	-	ET0_TX _ER	-	-	-	-	-	TS14	-
-	-	F10	26	-	-	IRQ10	P709	-	-	-	-	-	-	-	-	TXD1/ MOSI1 /SDA1	-	-	-	ET0_ET XD2	-	-	-	-	-	TS13	-
E15	35	D13	27	16	CACREF	IRQ11	P708	-	-	-	-	-	-	-	-	RXD1/ MISO1 /SCL1	-	SSLA3 _B	AUDIO _CLK	ET0_ET XD3	-	-	-	-	-	TS12	PCKO
E14	36	E11	28	17	-	IRQ8	P415	-	-	-	-	GTIOC 0A	-	USB_ VBUS EN	-	-	-	SSLA2 _B	-	ET0_TX _EN	RMII0_ TXD_E N_A	-	SD0 CD_ A	-	-	TS11	PIXD5
D15	37	D12	29	18	-	IRQ9	P414	-	-	-	-	GTIOC 0B	-	-	-	-	-	SSLA1 _B	-	ET0_RX _ER	RMII0_ TXD1_ A	-	SD0 WP_ A	-	-	TS10	PIXD4
E13	38	E10	30	19	-	-	P413	-	-	-	GTOUUP	-	-	-	CTS0_ RTS0/ SS0	-	-	SSLA0 _B	-	ET0_ET XD1	RMII0_ TXD0_ A	-	SD0 CLK_ A	-	-	TS09	PIXD3
D14	39	C13	31	20	-	-	P412	-	-	AGTEE1	GTOULO	-	-	-	SCK0	-	-	RSPC KA_B	-	ET0_ET XD0	REF50 CK0_A	-	SD0 CMD _A	-	-	TS08	PIX02
C15	40	D11	32	21	-	IRQ4	P411	-	-	AGTOA1	GTOVUP	GTIOC 9A	-	-	TXD0/ MOSI0 /SDA0	CTS3_ RTS3/ SS3	-	MOSIA _B	-	ET0_ER XD1	RMII0_ RXD0_ A	-	SD0 DAT0 _A	-	-	TS07	PIX01
C14	41	C12	33	22	-	IRQ5	P410	-	-	AGTOB1	GTOVLO	GTIOC 9B	-	-	RXD0/ MISO0 /SCL0	SCK3	-	MISOA _B	-	ET0_ER XD0	RMII0_ RXD1_ A	-	SD0 DAT1 _A	-	-	TS06	PIXD0
B15	42	B13	34	23	-	IRQ6	P409	-	-	-	GTOWUP	GTIOC 10A	-	USB_ EXIC EN	-	TXD3/ MOSI3 /SDA3	-	-	-	ET0_RX _CLK	RMII0_ RX_E R_A	USB HS_E XICE N	-	-	-	TS05	HSYNC
D13	43	D10	35	24	-	IRQ7	P408	-	-	-	GTOWLO	GTIOC 10B	-	USB_ ID	-	RXD3/ MISO3 /SCL3	SCL0 _B	-	-	ET0_C RS	RMII0_ CRS_ DV_A	USB HS_I D	-	-	-	TS04	PIXCLK
A15	44	A13	36	25	-	-	P407	-	-	AGTIO0	-	-	RTC OUT	USB_ VBUS	CTS4_ RTS4/ SS4	-	SDA0 _B	SSLB3 _A	-	ET0_EX OUT	ET0_E XOUT	-	-	ADTRG 0	-	TS03	-
C13	45	B11	37	26	VSS_US B	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
B14	46	A12	38	27	-	-	-	-	-	-	-	-	-	USB_ DM	-	-	-	-	-	-	-	-	-	-	-	-	-
A14	47	B12	39	28	-	-	-	-	-	-	-	-	-	USB_ DP	-	-	-	-	-	-	-	-	-	-	-	-	-
B13	48	A11	40	29	VCC_US B	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
C12	49	C11	41	30	-	-	P207	A17	-	-	-	-	-	-	-	-	-	SSLB2 _A/QS SL	-	-	-	-	-	-	-	TS02	LCD_DATA 23_B
D12	50	B10	42	31	-	IRQ0-DS	P206	WAIT	-	-	GTIU	-	-	USB_ VBUS EN	RXD4/ MISO4 /SCL4	-	SDA1 _A	SSLB1 _A	SSIDA TA1_A	ET0_LI NKSTA	ET0_LI NKST A	-	SD0 DAT2 _A	-	-	TS01	-
E12	51	A10	43	32	CLKOUT	IRQ1-DS	P205	A16	-	AGTO1	GTIV	GTIOC 4A	-	USB_ OVR CUR A-DS	TXD4/ MOSI4 /SDA4	CTS9_ RTS9/ SS9	SCL1 _A	SSLB0 _A	SSILR CK1/S SIFS1_ A	ET0_W OL	ET0_ WOL	-	SD0 DAT3 _A	-	-	TSCA P	-
A13	52	C10	44	-	CACREF	-	P204	A18	-	AGTIO1	GTIW	GTIOC 4B	-	USB_ OVR CUR B-DS	SCK4	SCK9	SCL0 _B	RSPC KB_A	SSIBC K1_A	ET0_RX _DV	-	-	SD0 DAT4 _A	-	-	TS00	-
D11	53	A9	45	-	-	IRQ2-DS	P203	A19	-	-	-	GTIOC 5A	-	CTX0	CTS2_ RTS2/ SS2	TXD9/ MOSI9 /SDA9	-	MOSIB _A	-	ET0_C OL	-	-	SD0 DAT5 _A	-	-	TSCA P	-
B12	54	C9	46	-	-	IRQ3-DS	P202	WR1/ BC1	-	-	-	GTIOC 5B	-	CRX0	SCK2	RXD9/ MISO9 /SCL9	-	MISOB _A	-	ET0_ER XD2	-	-	SD0 DAT6 _A	-	-	-	LCD_TCO N3_B
A12	55	B9	47	-	-	-	P313	A20	-	-	-	-	-	-	-	-	-	-	-	ET0_ER XD3	-	-	SD0 DAT7 _A	-	-	-	LCD_TCO N2_B
C11	56	-	-	-	-	-	P314	A21	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	ADTRG 0	-	-	LCD_TCO N1_B
B11	57	-	-	-	-	-	P315	A22	-	-	-	-	-	-	RXD4	-	-	-	-	-	-	-	-	-	-	-	LCD_TCO N0_B
A11	58	-	-	-	-	-	P900	A23	-	-	-	-	-	-	TXD4	-	-	-	-	-	-	-	-	-	-	-	LCD_CLK_ B
C10	59	-	-	-	-	-	P901	-	-	AGTIO1	-	-	-	-	SCK4	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA 15_B
D10	60	D9	48	-	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
D9	61	D8	49	-	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
A10	62	A8	50	33	TRCLK	-	P214	-	-	-	GTIU	-	-	-	-	-	-	QSPC LK	-	ET0_M DC	ET0_M DC	-	SD0 CLK_ B	-	-	-	LCD_DATA 22_B
B10	63	B8	51	34	TRDATA 0	-	P211	-	-	-	GTIV	-	-	-	-	-	-	QIO0	-	ET0_M DIO	ET0_M DIO	-	SD0 CMD _B	-	-	-	LCD_DATA 21_B
A9	64	A7	52	35	TRDATA 1	-	P210	-	-	-	GTIW	-	-	-	-	-	-	QIO1	-	ET0_W OL	ET0_ WOL	-	SD0 CD_ B	-	-	-	LCD_DATA 20_B
B9	65	B7	53	36	TRDATA 2	-	P209	-	-	-	GTOVUP	-	-	-	-	-	-	QIO2	-	ET0_EX OUT	ET0_E XOUT	-	SD0 WP_ B	-	-	-	LCD_DATA 19_B

Pin number					Power, System, Clock, Debug, CAC	Interrupt	I/O port	Extbus		Timers				Communication interfaces										Analog		HMI	
BGA176	LQFP176	LGA145	LQFP144	LQFP100				External bus	SDRAM	AGT	GPT	GPT	RTC	USBFS, CAN	SCI0,2,4,6,8 (30 MHz)	SCI1,3,5,7,9 (30 MHz)	IIC	SPI, QSPI	SSIE	ETHERC (MII) (25 MHz)	ETHERC (RMII) (60 MHz)	USBHS	SDHI	ADC12	DAC12, ACMPHS	CTSU	GLCDC, PDC
A8	66	A6	54	37	TRDATA3	-	P208	-	-	-	GTOVLO	-	-	-	-	-	-	QIO3	-	ET0_LINKSTA	ET0_LINKSTA	-	SD0DAT0_B	-	-	-	LCD_DATA18_B
C9	67	C7	55	38	RES	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
B8	68	B6	56	39	MD	-	P201	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
C8	69	C8	57	40	-	NMI	P200	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
D8	70	-	-	-	-	-	P908	CS7	-	-	-	GTIOC2A	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA14_B
D7	71	-	-	-	-	-	P907	CS6	-	-	-	GTIOC2B	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA13_B
A7	72	-	-	-	-	-	P906	CS5	-	-	-	GTIOC3A	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA12_B
B7	73	-	-	-	-	-	P905	CS4	-	-	-	GTIOC3B	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA11_B
C7	74	C6	58	-	-	-	P312	CS3	CAS	AGTOA1	-	-	-	-	-	CTS3_RTS3/SS3	-	-	-	-	-	-	-	-	-	-	-
D6	75	B5	59	-	-	-	P311	CS2	RAS	AGTOB1	-	-	-	-	-	SCK3	-	-	-	-	-	-	-	-	-	-	LCD_DATA23_A
A6	76	D7	60	-	-	-	P310	A15	A15	AGTEE1	-	-	-	-	-	TXD3	-	QIO3	-	-	-	-	-	-	-	-	LCD_DATA22_A
B6	77	A5	61	-	-	-	P309	A14	A14	-	-	-	-	-	-	RXD3	-	QIO2	-	-	-	-	-	-	-	-	LCD_DATA21_A
A5	78	C5	62	-	-	-	P308	A13	A13	-	-	-	-	-	-	-	-	QIO1	-	-	-	-	-	-	-	-	LCD_DATA20_A
C6	79	A4	63	41	-	-	P307	A12	A12	-	GTOUUP	-	-	-	CTS6	-	-	QIO0	-	-	-	-	-	-	-	-	LCD_DATA19_A
A4	80	B4	64	42	-	-	P306	A11	A11	-	GTOULO	-	-	-	SCK6	-	-	QSSL	-	-	-	-	-	-	-	-	LCD_DATA18_A
B5	81	D6	65	43	-	IRQ8	P305	A10	A10	-	GTOWUP	-	-	-	TXD6/MOSI6/SDA6	-	-	QSPCLK	-	-	-	-	-	-	-	-	LCD_DATA17_A
B4	82	C4	66	44	-	IRQ9	P304	A09	A09	-	GTOWLO	GTIOC7A	-	-	RXD6/MISO6/SCL6	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA16_A
C5	83	A3	67	45	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
D5	84	B3	68	46	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
A3	85	D5	69	47	-	-	P303	A08	A08	-	-	GTIOC7B	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA15_A
B3	86	A2	70	48	-	IRQ5	P302	A07	A07	-	GTOUUP	GTIOC4A	-	-	TXD2/MOSI2/SDA2	-	-	SSLB3_B	-	-	-	-	-	-	-	-	LCD_DATA14_A
A2	87	C3	71	49	-	IRQ6	P301	A06	A06	AGTIO0	GTOULO	GTIOC4B	-	-	RXD2/MISO2/SCL2	CTS9_RTS9/SS9	-	SSLB2_B	-	-	-	-	-	-	-	-	LCD_DATA13_A
C4	88	B2	72	50	TCK/SWCLK	-	P300	-	-	-	GTOUUP	GTIOC0A_A	-	-	-	-	-	SSLB1_B	-	-	-	-	-	-	-	-	-
C3	89	A1	73	51	TMS/SWDIO	-	P108	-	-	-	GTOULO	GTIOC0B_A	-	-	-	CTS9_RTS9/SS9	-	SSLB0_B	-	-	-	-	-	-	-	-	-
A1	90	D4	74	52	CLKOUT/TDO/SWO	-	P109	-	-	-	GTOVUP	GTIOC1A_A	-	CTX1	-	TXD9/MOSI9/SDA9	-	MOSIB_B	-	-	-	-	-	-	-	-	-
D3	91	B1	75	53	TDI	IRQ3	P110	-	-	-	GTOVLO	GTIOC1B_A	-	CRX1	CTS2_RTS2/SS2	RXD9/MISO9/SCL9	-	MISOB_B	-	-	-	-	-	-	VCOUT	-	-
D4	92	C2	76	54	-	IRQ4	P111	A05	A05	-	-	GTIOC3A_A	-	-	SCK2	SCK9	-	RSPCKB_B	-	-	-	-	-	-	-	-	LCD_DATA12_A
B2	93	D3	77	55	-	-	P112	A04	A04	-	-	GTIOC3B_A	-	-	TXD2/MOSI2/SDA2	SCK1	-	SSLB0_B	SSIBCK0_B	-	-	-	-	-	-	-	LCD_DATA11_A
B1	94	C1	78	56	-	-	P113	A03	A03	-	-	GTIOC2A	-	-	RXD2/MISO2/SCL2	-	-	-	SSILRCK0/SSIFS0_B	-	-	-	-	-	-	-	LCD_DATA10_A
C2	95	E4	79	57	-	-	P114	A02	A02	-	-	GTIOC2B	-	-	-	-	-	-	SSIRXD0_B	-	-	-	-	-	-	-	LCD_DATA09_A
C1	96	E3	80	58	-	-	P115	A01	A01	-	-	GTIOC4A	-	-	-	-	-	-	SSITXD0_B	-	-	-	-	-	-	-	LCD_DATA08_A
E3	97	D2	81	-	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
E4	98	D1	82	-	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
D2	99	F4	83	59	-	-	P608	A00/BC0	A00/DQM1	-	-	GTIOC4B	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA07_A
D1	100	E2	84	60	-	-	P609	CS1	CKE	-	-	GTIOC5A	-	CTX1	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA06_A
F3	101	F3	85	61	-	-	P610	CS0	WE	-	-	GTIOC5B	-	CRX1	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA05_A
E2	102	E1	86	-	CLKOUT/CACREF	-	P611	-	SDCS	-	-	-	-	-	-	CTS7_RTS7/SS7	-	-	-	-	-	-	-	-	-	-	-
E1	103	F2	87	-	-	-	P612	D08[A08/D08]	DQ08	-	-	-	-	-	-	SCK7	-	-	-	-	-	-	-	-	-	-	-
F4	104	F1	88	-	-	-	P613	D09[A09/D09]	DQ09	-	-	-	-	-	-	TXD7	-	-	-	-	-	-	-	-	-	-	-
F2	105	G3	89	-	-	-	P614	D10[A10/D10]	DQ10	-	-	-	-	-	-	RXD7	-	-	-	-	-	-	-	-	-	-	-
F1	106	-	-	-	-	-	P615	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA10_B
G1	107	-	-	-	-	-	PA08	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA09_B

RA6M3 Group 1. Overview

针号					电源系统，时钟，调试，CAC	Interrupt	I/O port	Extbus		Timers				通讯接口										Analog		HMI	
BGA176	LQFP176	LGA145	LQFP144	LQFP100				外线总部	SDRAM	AGT	GPT	GPT	RTC	USBFS, CAN	SCI0,2,4,6,8 (30 MHz)	SCI1,3,5,7,9 (30 MHz)	IIC	SPI, QSPI	SSIE	ETHERC (MII) (25 MHz)	ETHERC (RMII) (60 MHz)	USBHS	SDHI	ADC12	DAC12, ACMPHS	CTSU	GLCDC, PDC
A8	66	A6	54	37	TRDATA3	-	P208	-	-	-	GTOVLO	-	-	-	-	-	-	QIO3	-	ET0_LINKSTA	ET0_LINKSTA	-	SD0DAT0_B	-	-	-	LCD_DATA18_B
C9	67	C7	55	38	RES	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
B8	68	B6	56	39	MD	-	P201	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
C8	69	C8	57	40	-	NMI	P200	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
D8	70	-	-	-	-	-	P908	CS7	-	-	-	GTIOC2A	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA14_B
D7	71	-	-	-	-	-	P907	CS6	-	-	-	GTIOC2B	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA13_B
A7	72	-	-	-	-	-	P906	CS5	-	-	-	GTIOC3A	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA12_B
B7	73	-	-	-	-	-	P905	CS4	-	-	-	GTIOC3B	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA11_B
C7	74	C6	58	-	-	-	P312	CS3	CAS	AGTOA1	-	-	-	-	-	CTS3_RTS3/SS3	-	-	-	-	-	-	-	-	-	-	-
D6	75	B5	59	-	-	-	P311	CS2	RAS	AGTOB1	-	-	-	-	-	SCK3	-	-	-	-	-	-	-	-	-	-	LCD_DATA23_A
A6	76	D7	60	-	-	-	P310	A15	A15	AGTEE1	-	-	-	-	-	TXD3	-	QIO3	-	-	-	-	-	-	-	-	LCD_DATA22_A
B6	77	A5	61	-	-	-	P309	A14	A14	-	-	-	-	-	-	RXD3	-	QIO2	-	-	-	-	-	-	-	-	LCD_DATA21_A
A5	78	C5	62	-	-	-	P308	A13	A13	-	-	-	-	-	-	-	-	QIO1	-	-	-	-	-	-	-	-	LCD_DATA20_A
C6	79	A4	63	41	-	-	P307	A12	A12	-	GTOUUP	-	-	-	CTS6	-	-	QIO0	-	-	-	-	-	-	-	-	LCD_DATA19_A
A4	80	B4	64	42	-	-	P306	A11	A11	-	GTOULO	-	-	-	SCK6	-	-	QSSL	-	-	-	-	-	-	-	-	LCD_DATA18_A
B5	81	D6	65	43	-	IRQ8	P305	A10	A10	-	GTOWUP	-	-	-	TXD6/MOSI6/SDA6	-	-	QSPCLK	-	-	-	-	-	-	-	-	LCD_DATA17_A
B4	82	C4	66	44	-	IRQ9	P304	A09	A09	-	GTOWLO	GTIOC7A	-	-	RXD6/MISO6/SCL6	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA16_A
C5	83	A3	67	45	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
D5	84	B3	68	46	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
A3	85	D5	69	47	-	-	P303	A08	A08	-	-	GTIOC7B	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA15_A
B3	86	A2	70	48	-	IRQ5	P302	A07	A07	-	GTOUUP	GTIOC4A	-	-	TXD2/MOSI2/SDA2	-	-	SSLB3_B	-	-	-	-	-	-	-	-	LCD_DATA14_A
A2	87	C3	71	49	-	IRQ6	P301	A06	A06	AGTIO0	GTOULO	GTIOC4B	-	-	RXD2/MISO2/SCL2	CTS9_RTS9/SS9	-	SSLB2_B	-	-	-	-	-	-	-	-	LCD_DATA13_A
C4	88	B2	72	50	TCK/SWCLK	-	P300	-	-	-	GTOUUP	GTIOC0A_A	-	-	-	-	-	SSLB1_B	-	-	-	-	-	-	-	-	-
C3	89	A1	73	51	TMS/SWDIO	-	P108	-	-	-	GTOULO	GTIOC0B_A	-	-	-	CTS9_RTS9/SS9	-	SSLB0_B	-	-	-	-	-	-	-	-	-
A1	90	D4	74	52	CLKOUT/TDO/SWO	-	P109	-	-	-	GTOVUP	GTIOC1A_A	-	CTX1	-	TXD9/MOSI9/SDA9	-	MOSIB_B	-	-	-	-	-	-	-	-	-
D3	91	B1	75	53	TDI	IRQ3	P110	-	-	-	GTOVLO	GTIOC1B_A	-	CRX1	CTS2_RTS2/SS2	RXD9/MISO9/SCL9	-	MISOB_B	-	-	-	-	-	-	VCOUT	-	-
D4	92	C2	76	54	-	IRQ4	P111	A05	A05	-	-	GTIOC3A_A	-	-	SCK2	SCK9	-	RSPCKB_B	-	-	-	-	-	-	-	-	LCD_DATA12_A
B2	93	D3	77	55	-	-	P112	A04	A04	-	-	GTIOC3B_A	-	-	TXD2/MOSI2/SDA2	SCK1	-	SSLB0_B	SSIBCK0_B	-	-	-	-	-	-	-	LCD_DATA11_A
B1	94	C1	78	56	-	-	P113	A03	A03	-	-	GTIOC2A	-	-	RXD2/MISO2/SCL2	-	-	-	SSILRCK0/SSIFS0_B	-	-	-	-	-	-	-	LCD_DATA10_A
C2	95	E4	79	57	-	-	P114	A02	A02	-	-	GTIOC2B	-	-	-	-	-	-	SSIRXD0_B	-	-	-	-	-	-	-	LCD_DATA09_A
C1	96	E3	80	58	-	-	P115	A01	A01	-	-	GTIOC4A	-	-	-	-	-	-	SSITXD0_B	-	-	-	-	-	-	-	LCD_DATA08_A
E3	97	D2	81	-	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
E4	98	D1	82	-	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
D2	99	F4	83	59	-	-	P608	A00/BC0	A00/DQM1	-	-	GTIOC4B	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA07_A
D1	100	E2	84	60	-	-	P609	CS1	CKE	-	-	GTIOC5A	-	CTX1	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA06_A
F3	101	F3	85	61	-	-	P610	CS0	WE	-	-	GTIOC5B	-	CRX1	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA05_A
E2	102	E1	86	-	CLKOUT/CACREF	-	P611	-	SDCS	-	-	-	-	-	-	CTS7_RTS7/SS7	-	-	-	-	-	-	-	-	-	-	-
E1	103	F2	87	-	-	-	P612	D08[A08/D08]	DQ08	-	-	-	-	-	-	SCK7	-	-	-	-	-	-	-	-	-	-	-
F4	104	F1	88	-	-	-	P613	D09[A09/D09]	DQ09	-	-	-	-	-	-	TXD7	-	-	-	-	-	-	-	-	-	-	-
F2	105	G3	89	-	-	-	P614	D10[A10/D10]	DQ10	-	-	-	-	-	-	RXD7	-	-	-	-	-	-	-	-	-	-	-
F1	106	-	-	-	-	-	P615	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA10_B
G1	107	-	-	-	-	-	PA08	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA09_B

Pin number					Power, System, Clock, Debug, CAC	Interrupt	I/O port	Extbus		Timers				Communication interfaces										Analog		HMI	
BGA176	LQFP176	LGA145	LQFP144	LQFP100				External bus	SDRAM	AGT	GPT	GPT	RTC	USBFS, CAN	SCI0,2,4,6,8 (30 MHz)	SCI1,3,5,7,9 (30 MHz)	IIC	SPI, QSPI	SSIE	ETHERC (MII) (25 MHz)	ETHERC (RMII) (50 MHz)	USBHS	SDHI	ADC12	DAC12, ACMPHS	CTSU	GLCDC, PDC
G4	108	-	-	-	-	-	PA09	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA 08_B
G2	109	-	-	-	-	-	PA10	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA 07_B
G3	110	G1	90	62	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
H3	111	G2	91	63	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
H1	112	H1	92	64	VCL	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
H2	113	-	-	-	-	-	PA01	-	-	-	-	-	-	-	SCK8	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA 06_B
H4	114	-	-	-	-	-	PA00	-	-	-	-	-	-	-	TXD8	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA 05_B
J4	115	-	-	-	-	-	P607	-	-	-	-	-	-	-	RXD8	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA 04_B
J1	116	-	-	-	-	-	P606	-	-	-	-	-	RTC OUT	-	CTS8_ RTS8/ SS8	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA 03_B
J2	117	H2	93	-	-	-	P605	D11[A11/ D11]	DQ11	-	-	GTIOC 8A	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
J3	118	G4	94	-	-	-	P604	D12[A12/ D12]	DQ12	-	-	GTIOC 8B	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
K3	119	H3	95	-	-	-	P603	D13[A13/ D13]	DQ13	-	-	GTIOC 7A	-	-	-	CTS9_ RTS9/ SS9	-	-	-	-	-	-	-	-	-	-	-
K1	120	J1	96	65	-	-	P602	EBC LK	SDCL K	-	-	GTIOC 7B	-	-	-	TXD9	-	-	-	-	-	-	-	-	-	-	LCD_DATA 04_A
K2	121	J2	97	66	-	-	P601	WR/ WR0	DQM0	-	-	GTIOC 6A	-	-	-	RXD9	-	-	-	-	-	-	-	-	-	-	LCD_DATA 03_A
L1	122	H4	98	67	CLKOUT /CACRE F	-	P600	RD	-	-	-	GTIOC 6B	-	-	-	SCK9	-	-	-	-	-	-	-	-	-	-	LCD_DATA 02_A
K4	123	K2	99	-	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
L4	124	K1	100	-	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
L2	125	J3	101	68	-	KR07	P107	D07[A07/ D07]	DQ07	AGTOA0	-	GTIOC 8A	-	-	CTS8_ RTS8/ SS8	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA 01_A
M1	126	K3	102	69	-	KR06	P106	D06[A06/ D06]	DQ06	AGTOB0	-	GTIOC 8B	-	-	SCK8	-	-	SSLA3 _A	-	-	-	-	-	-	-	-	LCD_DATA 00_A
L3	127	J4	103	70	-	IRQ0/ KR05	P105	D05[A05/ D05]	DQ05	-	GTETRGA	GTIOC 1A	-	-	TXD8/ MOSI8 /SDA8	-	-	SSLA2 _A	-	-	-	-	-	-	-	-	LCD_TCO N3_A
M2	128	L3	104	71	-	IRQ1/ KR04	P104	D04[A04/ D04]	DQ04	-	GTETRGB	GTIOC 1B	-	-	RXD8/ MISO8 /SCL8	-	-	SSLA1 _A	-	-	-	-	-	-	-	-	LCD_TCO N2_A
N1	129	L1	105	72	-	KR03	P103	D03[A03/ D03]	DQ03	-	GTOWUP	GTIOC 2A_A	-	CTX0	CTS0_ RTS0/ SS0	-	-	SSLA0 _A	-	-	-	-	-	-	-	-	LCD_TCO N1_A
M3	130	M1	106	73	-	KR02	P102	D02[A02/ D02]	DQ02	AGTO0	GTOWLO	GTIOC 2B_A	-	CRX0	SCK0	-	-	RSPC KA_A	-	-	-	-	-	ADTRG 0	-	-	LCD_TCO N0_A
N2	131	M2	107	74	-	IRQ1/ KR01	P101	D01[A01/ D01]	DQ01	AGTEE0	GTETRGB	GTIOC 5A	-	-	TXD0/ MOSI0 /SDA0	CTS1_ RTS1/ SS1	SDA1 _B	MOSIA _A	-	-	-	-	-	-	-	-	LCD_CLK_ A
P1	132	N1	108	75	-	IRQ2/ KR00	P100	D00[A00/ D00]	DQ00	AGTIO0	GTETRGA	GTIOC 5B	-	-	RXD0/ MISO0 /SCL0	SCK1	SCL1 _B	MISOA _A	-	-	-	-	-	-	-	-	LCD_EXT CLK_A
N3	133	L2	109	-	-	-	P800	D14[A14/ D14]	DQ14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R1	134	N2	110	-	-	-	P801	D15[A15/ D15]	DQ15	-	-	-	-	-	-	-	-	-	-	-	-	-	SD1 DAT4 _A	-	-	-	-
P2	135	-	-	-	-	-	P802	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	SD1 DAT5 _A	-	-	-	LCD_DATA 02_B
R2	136	-	-	-	-	-	P803	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	SD1 DAT6 _A	-	-	-	LCD_DATA 01_B
P3	137	-	-	-		-	P804	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	SD1 DAT7 _A	-	-	-	LCD_DATA 00_B
N4	138	N3	111	-	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
M4	139	M3	112	-	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R3	140	K4	113	76	-	-	P500	-	-	AGTOA0	GTIU	GTIOC 11A	-	USB_ VBUS EN	-	-	-	QSPC LK	-	-	-	-	SD1 CLK_ A	AN016	IVREF0	-	-
P4	141	M4	114	77	-	IRQ11	P501	-	-	AGTOB0	GTIV	GTIOC 11B	-	USB_ OVR_ CUR A	-	TXD5/ MOSI5 /SDA5	-	QSSL	-	-	-	-	SD1 CMD _A	AN116	IVREF1	-	-
R4	142	L4	115	78	-	IRQ12	P502	-	-	-	GTIW	GTIOC 12A	-	USB_ OVR_ CUR B	-	RXD5/ MISO5 /SCL5	-	QIO0	-	-	-	-	SD1 DAT0 _A	AN017	IVCMP0	-	-
N5	143	K5	116	79	-	-	P503	-	-	-	GTETRGC	GTIOC 12B	-	USB_ EXIC EN	CTS6_ RTS6/ SS6	SCK5	-	QIO1	-	-	-	-	SD1 DAT1 _A	AN117	-	-	-
P5	144	L5	117	80	-	-	P504	ALE	-	-	GTETRGD	GTIOC 13A	-	USB_ ID	SCK6	CTS5_ RTS5/ SS5	-	QIO2	-	-	-	-	SD1 DAT2 _A	AN018	-	-	-
P6	145	K6	118	-	-	IRQ14	P505	-	-	-	-	GTIOC 13B	-	-	RXD6/ MISO6 /SCL6	-	-	QIO3	-	-	-	-	SD1 DAT3 _A	AN118	-	-	-

针号					电源系统、时钟、调试、CAC	Interrupt	I/O port	Extbus		Timers				通讯接口										Analog		HMI	
BGA176	LQFP176	LGA145	LQFP144	LQFP100				外线总部	SDRAM	AGT	GPT	GPT	RTC	USBFS, CAN	SCI0,2,4,6,8 (30 MHz)	SCI1,3,5,7,9 (30 MHz)	IIC	SPI, QSPI	SSIE	ETHERC (MII) (25 MHz)	ETHERC (RMII) (50 MHz)	USBHS	SDHI	ADC12	DAC12, ACMPHS	CTSU	GLCDC, PDC
G4	108	-	-	-	-	-	PA09	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA 08_B
G2	109	-	-	-	-	-	PA10	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA 07_B
G3	110	G1	90	62	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
H3	111	G2	91	63	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
H1	112	H1	92	64	VCL	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
H2	113	-	-	-	-	-	PA01	-	-	-	-	-	-	-	SCK8	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA 06_B
H4	114	-	-	-	-	-	PA00	-	-	-	-	-	-	-	TXD8	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA 05_B
J4	115	-	-	-	-	-	P607	-	-	-	-	-	-	-	RXD8	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA 04_B
J1	116	-	-	-	-	-	P606	-	-	-	-	-	RTC OUT	-	CTS8_ RTS8/ SS8	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA 03_B
J2	117	H2	93	-	-	-	P605	D11[A11/ D11]	DQ11	-	-	GTIOC 8A	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
J3	118	G4	94	-	-	-	P604	D12[A12/ D12]	DQ12	-	-	GTIOC 8B	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
K3	119	H3	95	-	-	-	P603	D13[A13/ D13]	DQ13	-	-	GTIOC 7A	-	-	-	CTS9_ RTS9/ SS9	-	-	-	-	-	-	-	-	-	-	-
K1	120	J1	96	65	-	-	P602	EBC LK	SDCL K	-	-	GTIOC 7B	-	-	-	TXD9	-	-	-	-	-	-	-	-	-	-	LCD_DATA 04_A
K2	121	J2	97	66	-	-	P601	WR/ WR0	DQM0	-	-	GTIOC 6A	-	-	-	RXD9	-	-	-	-	-	-	-	-	-	-	LCD_DATA 03_A
L1	122	H4	98	67	CLKOUT /CACRE F	-	P600	RD	-	-	-	GTIOC 6B	-	-	-	SCK9	-	-	-	-	-	-	-	-	-	-	LCD_DATA 02_A
K4	123	K2	99	-	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
L4	124	K1	100	-	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
L2	125	J3	101	68	-	KR07	P107	D07[A07/ D07]	DQ07	AGTOA0	-	GTIOC 8A	-	-	CTS8_ RTS8/ SS8	-	-	-	-	-	-	-	-	-	-	-	LCD_DATA 01_A
M1	126	K3	102	69	-	KR06	P106	D06[A06/ D06]	DQ06	AGTOB0	-	GTIOC 8B	-	-	SCK8	-	-	SSLA3 _A	-	-	-	-	-	-	-	-	LCD_DATA 00_A
L3	127	J4	103	70	-	IRQ0/ KR05	P105	D05[A05/ D05]	DQ05	-	GTETRGA	GTIOC 1A	-	-	TXD8/ MOSI8 /SDA8	-	-	SSLA2 _A	-	-	-	-	-	-	-	-	LCD_TCO N3_A
M2	128	L3	104	71	-	IRQ1/ KR04	P104	D04[A04/ D04]	DQ04	-	GTETRGB	GTIOC 1B	-	-	RXD8/ MISO8 /SCL8	-	-	SSLA1 _A	-	-	-	-	-	-	-	-	LCD_TCO N2_A
N1	129	L1	105	72	-	KR03	P103	D03[A03/ D03]	DQ03	-	GTOWUP	GTIOC 2A_A	-	CTX0	CTS0_ RTS0/ SS0	-	-	SSLA0 _A	-	-	-	-	-	-	-	-	LCD_TCO N1_A
M3	130	M1	106	73	-	KR02	P102	D02[A02/ D02]	DQ02	AGTO0	GTOWLO	GTIOC 2B_A	-	CRX0	SCK0	-	-	RSPC KA_A	-	-	-	-	-	ADTRG 0	-	-	LCD_TCO N0_A
N2	131	M2	107	74	-	IRQ1/ KR01	P101	D01[A01/ D01]	DQ01	AGTEE0	GTETRGB	GTIOC 5A	-	-	TXD0/ MOSI0 /SDA0	CTS1_ RTS1/ SS1	SDA1 _B	MOSIA _A	-	-	-	-	-	-	-	-	LCD_CLK_ A
P1	132	N1	108	75	-	IRQ2/ KR00	P100	D00[A00/ D00]	DQ00	AGTIO0	GTETRGA	GTIOC 5B	-	-	RXD0/ MISO0 /SCL0	SCK1	SCL1 _B	MISOA _A	-	-	-	-	-	-	-	-	LCD_EXT CLK_A
N3	133	L2	109	-	-	-	P800	D14[A14/ D14]	DQ14	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R1	134	N2	110	-	-	-	P801	D15[A15/ D15]	DQ15	-	-	-	-	-	-	-	-	-	-	-	-	-	SD1 DAT4 _A	-	-	-	-
P2	135	-	-	-	-	-	P802	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	SD1 DAT5 _A	-	-	-	LCD_DATA 02_B
R2	136	-	-	-	-	-	P803	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	SD1 DAT6 _A	-	-	-	LCD_DATA 01_B
P3	137	-	-	-		-	P804	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	SD1 DAT7 _A	-	-	-	LCD_DATA 00_B
N4	138	N3	111	-	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
M4	139	M3	112	-	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R3	140	K4	113	76	-	-	P500	-	-	AGTOA0	GTIU	GTIOC 11A	-	USB_ VBUS EN	-	-	-	QSPC LK	-	-	-	-	SD1 CLK_ A	AN016	IVREF0	-	-
P4	141	M4	114	77	-	IRQ11	P501	-	-	AGTOB0	GTIV	GTIOC 11B	-	USB_ OVR_ CUR A	-	TXD5/ MOSI5 /SDA5	-	QSSL	-	-	-	-	SD1 CMD _A	AN116	IVREF1	-	-
R4	142	L4	115	78	-	IRQ12	P502	-	-	-	GTIW	GTIOC 12A	-	USB_ OVR_ CUR B	-	RXD5/ MISO5 /SCL5	-	QIO0	-	-	-	-	SD1 DAT0 _A	AN017	IVCMP0	-	-
N5	143	K5	116	79	-	-	P503	-	-	-	GTETRGC	GTIOC 12B	-	USB_ EXIC EN	CTS6_ RTS6/ SS6	SCK5	-	QIO1	-	-	-	-	SD1 DAT1 _A	AN117	-	-	-
P5	144	L5	117	80	-	-	P504	ALE	-	-	GTETRGD	GTIOC 13A	-	USB_ ID	SCK6	CTS5_ RTS5/ SS5	-	QIO2	-	-	-	-	SD1 DAT2 _A	AN018	-	-	-
P6	145	K6	118	-	-	IRQ14	P505	-	-	-	-	GTIOC 13B	-	-	RXD6/ MISO6 /SCL6	-	-	QIO3	-	-	-	-	SD1 DAT3 _A	AN118	-	-	-

Pin number																																			
								Extbus		Timers				Communication interfaces												Analog		HMI			
BGA176	LQFP176	LGA145	LQFP144	LQFP100	Power, System, Clock, Debug, CAC	Interrupt	I/O port	External bus	SDRAM	AGT	GPT	GPT	RTC	USBFS, CAN	SCI0,2,4,6,8 (30 MHz)	SCI1,3,5,7,9 (30 MHz)	IIC	SPI, QSPI	SSIE	ETHERC (MII) (25 MHz)	ETHERC (RMII) (50 MHz)	USBHS	SDHI	ADC12	DAC12, ACMPHS	CTSU	GLCDC, PDC
R5	146	L6	119	-	-	IRQ15	P506	-	-	-	-	-	-	-	TXD6/ MOSI6 /SDA6	-	-	-	-	-	-	-	SD1 CD_ A	AN019	-	-	-
N6	147	-	-	-	-	-	P507	-	-	-	-	-	-	-	-	CTS5_ RTS5/ SS5	-	-	-	-	-	-	-	SD1 WP_ A	AN119	-	-	-
R6	148	N4	120	81	-	-	P508	-	-	-	-	-	-	-	SCK6	SCK5	-	-	-	-	-	-	-	-	AN020	-	-	-
M7	149	N5	121	82	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
N7	150	M5	122	83	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
P7	151	M6	123	84	-	IRQ13	P015	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	AN006/ AN106	DA1/ IVCMP1	-	-
R7	152	N6	124	85	-	-	P014	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	AN005/ AN105	DA0/ IVREF3	-	-
P8	153	M7	125	86	VREFL	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R8	154	N7	126	87	VREFH	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
N8	155	L7	127	88	AVCC0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
N9	156	L8	128	89	AVSS0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
P9	157	M8	129	90	VREFL0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R9	158	N8	130	91	VREFH0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
M8	159	-	-	-	-	IRQ14 -DS	P010	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	AN103	-	-	-
M9	160	M9	131	-	-	IRQ13 -DS	P009	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	AN004	-	-	-
P10	161	N9	132	92	-	IRQ12 -DS	P008	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	AN003	-	-	-
M6	162	K7	133	93	-	-	P007	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	PGAVS S100/A N107	-	-	-
N10	163	L9	134	94	-	IRQ11- DS	P006	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	AN102	IVCMP2	-	-
R10	164	K8	135	95	-	IRQ10 -DS	P005	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	AN101	IVCMP2	-	-
P11	165	K9	136	96	-	IRQ9- DS	P004	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	AN100	IVCMP2	-	-
M5	166	K10	137	97	-	-	P003	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	PGAVS S000/A N007	-	-	-
R11	167	M10	138	98	-	IRQ8- DS	P002	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	AN002	IVCMP2	-	-
N11	168	N10	139	99	-	IRQ7- DS	P001	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	AN001	IVCMP2	-	-
R12	169	L10	140	100	-	IRQ6- DS	P000	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	AN000	IVCMP2	-	-
M10	170	N11	141	-	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
M11	171	N12	142	-	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
P12	172	-	-	-	-	-	P806	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_EXT CLK_B
R13	173	-	-	-	-	-	P805	-	-	-	-	-	-	-	-	TXD5	-	-	-	-	-	-	-	-	-	-	LCD_DATA 17_B
N12	174	-	-	-	-	-	P513	-	-	-	-	-	-	-	-	RXD5	-	-	-	-	-	-	-	-	-	-	LCD_DATA 16_B
R14	175	M11	143	-	-	IRQ14	P512	-	-	-	-	GTIOC 0A	-	CTX1	TXD4/ MOSI4 /SDA4	-	SCL2	-	-	-	-	-	-	-	-	-	VSYNC
P13	176	M12	144	-	-	IRQ15	P511	-	-	-	-	GTIOC 0B	-	CRX1	RXD4/ MISO4 /SCL4	-	SDA2	-	-	-	-	-	-	-	-	-	PCKO

Note: Some pin names have the added suffix of _A, _B, and _C. When assigning the GPT, IIC, SPI, SSIE, ETHERC (RMII), SDHI, and GLCDC functionality, select the functional pins with the same suffix.

针号								Extbus		Timers				通讯接口												Analog		HMI			
BGA176	LQFP176	LGA145	LQFP144	LQFP100	电源系统、时钟、调试、CAC	Interrupt	I/O port	外线总部	SDRAM	AGT	GPT	GPT	RTC	USBFS, CAN	SCI0,2,4,6,8 (30 MHz)	SCI1,3,5,7,9 (30 MHz)	IIC	SPI, QSPI	SSIE	ETHERC (MII) (25 MHz)	ETHERC (RMII) (50 MHz)	USBHS	SDHI	ADC12	DAC12, ACMPHS	CTSU	GLCDC, PDC
R5	146	L6	119	-	-	IRQ15	P506	-	-	-	-	-	-	-	TXD6/ MOSI6 /SDA6	-	-	-	-	-	-	-	SD1 CD_ A	AN019	-	-	-
N6	147	-	-	-	-	-	P507	-	-	-	-	-	-	-	-	CTS5_ RTS5/ SS5	-	-	-	-	-	-	-	SD1 WP_ A	AN119	-	-	-
R6	148	N4	120	81	-	-	P508	-	-	-	-	-	-	-	SCK6	SCK5	-	-	-	-	-	-	-	-	AN020	-	-	-
M7	149	N5	121	82	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
N7	150	M5	122	83	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
P7	151	M6	123	84	-	IRQ13	P015	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	AN006/ AN106	DA1/ IVCMP1	-	-
R7	152	N6	124	85	-	-	P014	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	AN005/ AN105	DA0/ IVREF3	-	-
P8	153	M7	125	86	VREFL	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R8	154	N7	126	87	VREFH	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
N8	155	L7	127	88	AVCC0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
N9	156	L8	128	89	AVSS0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
P9	157	M8	129	90	VREFL0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
R9	158	N8	130	91	VREFH0	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
M8	159	-	-	-	-	IRQ14 -DS	P010	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	AN103	-	-	-
M9	160	M9	131	-	-	IRQ13 -DS	P009	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	AN004	-	-	-
P10	161	N9	132	92	-	IRQ12 -DS	P008	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	AN003	-	-	-
M6	162	K7	133	93	-	-	P007	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	PGAVS S100/A N107	-	-	-
N10	163	L9	134	94	-	IRQ11- DS	P006	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	AN102	IVCMP2	-	-
R10	164	K8	135	95	-	IRQ10 -DS	P005	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	AN101	IVCMP2	-	-
P11	165	K9	136	96	-	IRQ9- DS	P004	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	AN100	IVCMP2	-	-
M5	166	K10	137	97	-	-	P003	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	PGAVS S000/A N007	-	-	-
R11	167	M10	138	98	-	IRQ8- DS	P002	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	AN002	IVCMP2	-	-
N11	168	N10	139	99	-	IRQ7- DS	P001	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	AN001	IVCMP2	-	-
R12	169	L10	140	100	-	IRQ6- DS	P000	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	AN000	IVCMP2	-	-
M10	170	N11	141	-	VSS	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
M11	171	N12	142	-	VCC	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-
P12	172	-	-	-	-	-	P806	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	-	LCD_EXT CLK_B
R13	173	-	-	-	-	-	P805	-	-	-	-	-	-	-	-	TXD5	-	-	-	-	-	-	-	-	-	-	LCD_DATA 17_B
N12	174	-	-	-	-	-	P513	-	-	-	-	-	-	-	-	RXD5	-	-	-	-	-	-	-	-	-	-	LCD_DATA 16_B
R14	175	M11	143	-	-	IRQ14	P512	-	-	-	-	GTIOC 0A	-	CTX1	TXD4/ MOSI4 /SDA4	-	SCL2	-	-	-	-	-	-	-	-	-	VSYNC
P13	176	M12	144	-	-	IRQ15	P511	-	-	-	-	GTIOC 0B	-	CRX1	RXD4/ MISO4 /SCL4	-	SDA2	-	-	-	-	-	-	-	-	-	PCKO

Note: 一些引脚名称添加了_A、_B和_C的后缀。分配GPT、IIC、SPI、SSIE、ETHERC(RMII)、SDHI和GLCDC功能时，选择具有相同后缀的功能管脚。

2. CPU

2.1 Overview

The MCU is based on the Arm® Cortex®-M4 core.

2.1.1 CPU

- Arm Cortex-M4
  - Revision: r0p1-01rel0
  - Armv7E-M architecture profile
  - Single Precision Floating Point Unit compliant with the ANSI/IEEE Std 754-2008.
- Memory Protection Unit (MPU)
  - Armv7 Protected Memory System Architecture
  - 8 protected regions.
- SysTick timer
  - Driven by SYSTICCLK (LOCO) or ICLK.

See reference 1. and reference 2. for details.

2.1.2 Debug

- Arm CoreSight™ ETM-M4
  - Revision: r0p1-00rel0
  - Arm ETM architecture version 3.5.
- CoreSight Instrumentation Trace Macrocell (ITM)
- Data Watchpoint and Trace Unit (DWT)
  - 4 comparators for watchpoints and triggers.
- Flash Patch and Breakpoint Unit (FPB)
  - Flash Patch (remap) function is unavailable, only breakpoint function is available
  - 6 instruction comparators
  - 2 literal comparators.
- CoreSight Time Stamp Generator (TSG)
  - Time stamp for ETM and ITM
  - Driven by CPU clock.
- Debug Register Module (DBGREG)
  - Reset control
  - Halt control.
- CoreSight Debug Access Port (DAP)
  - JTAG Debug Port (JTAG-DP)
  - Serial Wire Debug Port (SW-DP).
- Cortex-M4 Trace Port Interface Unit (TPIU)
  - 4-bit TPIU formatter output
  - Serial Wire Output.

2. CPU

2.1 Overview

MCU基于Arm®Cortex®-M4内核。

2.1.1 CPU

- Arm Cortex-M4
  - Revision: r0p1-01rel0
  - Armv7E-M架构简介
  - 符合ANSIIEEEStd754-2008的单精度浮点单元。
- 内存保护单元(MPU)
  - Armv7受保护的内存系统架构
  - 8个保护区。
- SysTick timer
  - 由SYSTICCLK(LOCO)或ICLK驱动。

有关详细信息，请参阅参考1.和参考2。

2.1.2 Debug

- Arm CoreSight™ ETM-M4
  - Revision: r0p1-00rel0
  - ArmETM架构版本3.5。
- CoreSight仪表跟踪宏单元(ITM)
- 数据观察点和跟踪单元(DWT)
  - 4个用于观察点和触发器的比较器。
- 闪存补丁和断点单元(FPB)
  - FlashPatch（remap）功能不可用，只有断点功能可用
  - 6 instruction comparators
  - 2 literal comparators.
- CoreSight时间戳生成器(TSG)
  - ETM和ITM的时间戳
  - 由CPU时钟驱动。
- 调试寄存器模块(DBGREG)
  - 重置控制
  - 停止控制。
- CoreSight调试访问端口(DAP)
  - JTAG调试端口(JTAG-DP)
  - 串行线调试端口(SW-DP)。
- Cortex-M4跟踪端口接口单元(TPIU)
  - 4-bit TPIU formatter output
  - 串行线输出。

- CoreSight Embedded Trace Buffer (ETB)
  - CoreSight Trace Memory Controller with ETB configuration
  - Buffer size: 2 KB.

See reference 1. and reference 2. for details.

2.1.3 Operating Frequency

The operating frequencies for the MCU are as follows:

- CPU core: maximum 120 MHz
- Trace (4-bit TPIU): maximum 60 MHz
- Trace (SWO): maximum 60 MHz
- JTAG interface: maximum 25 MHz
- SWD interface: maximum 25 MHz.

Figure 2.1 shows a block diagram of the Cortex-M4 CPU.

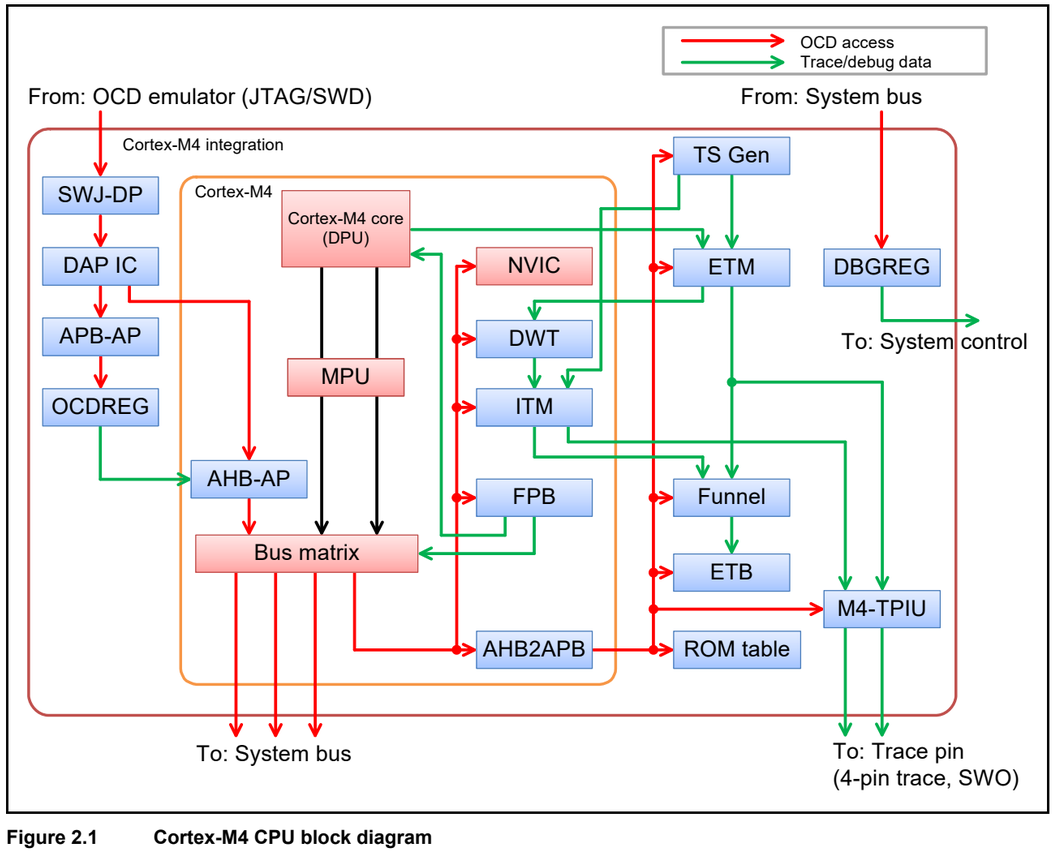


Figure 2.1 Cortex-M4 CPU block diagram

- CoreSight嵌入式跟踪缓冲区(ETB)
  - 具有ETB配置的CoreSight跟踪内存控制器
  - Buffer size: 2 KB.

有关详细信息，请参阅参考1.和参考2.。

2.1.3 工作频率

MCU的工作频率如下：

- CPU内核：最大120MHz
- 跟踪（4位TPIU）：最大60MHz
- 迹线(SWO)：最大60MHz
- JTAG interface: maximum 25 MHz
- SWD interface: maximum 25 MHz.

图2.1显示了Cortex-M4CPU的框图。

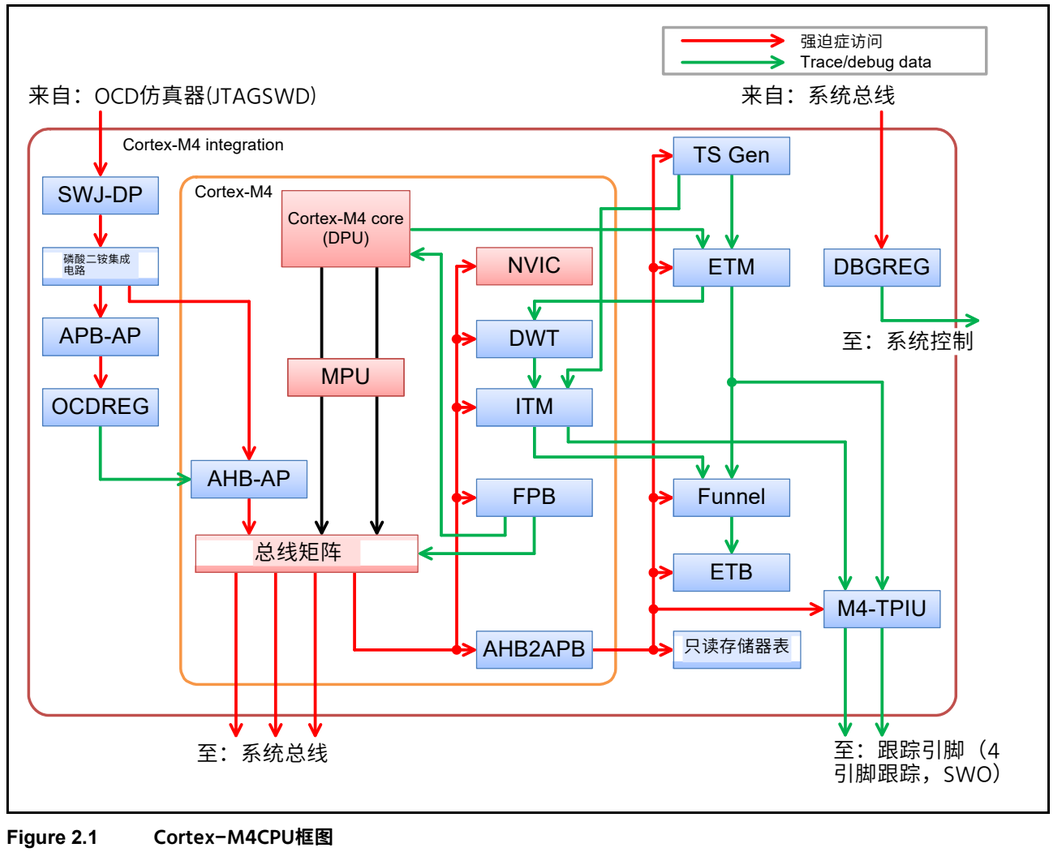


Figure 2.1 Cortex-M4CPU框图

2.2 MCU Implementation Options

Table 2.1 Implementation options

Option	Implementation
MPU	Included, 8 protect regions
FPB	Flash Patch (remap) function is unavailable, only breakpoint function is available
FPU	Included
Number of interrupts	96
Number of priority bits	4
Number of Wakeup Interrupt Controllers (WIC*1)	Not included
Sleep mode power saving	Sleep mode and other low power modes are supported. For more details, see section 11, Low Power Modes. Note: SCB.SCR.SLEEPDEEP is ignored.
Endianness	Little-endian
SysTick SYST_CALIB register	SYST_CALIB = 4000 0147h Bit [31] = 0 Reference clock provided Bit [30] = 1 TERMS value is inexact Bits [29:24] = 00h Reserved Bits [23:0] = 000147h TERM: (32768 × 10 ms) - 1 / 32.768 kHz = 326.66 decimal = 327 with skew = 000147h
Event input/output	Not implemented
System reset request output	The SYSRESETREQ bit in the Application Interrupt and Reset Control Register causes a CPU reset
Auxiliary fault inputs (AUXFAULT)	Not implemented

Note 1. The ICU can wake up the CPU instead of the Wakeup Interrupt Controller (WIC). For details, see section 14, Interrupt Controller Unit (ICU).

2.3 Trace Interface

A Trace Port Interface Unit (TPIU) and Serial Wire Output (SWO) provide trace output. Table 2.2 shows the MCU pins for the function. These pins are multiplexed with other functions.

Table 2.2 Trace function pins

Name	I/O	Width	Function
TCLK	Output	1 bit	Trace clock
TDATA0	Output	1 bit	Trace data output 0
TDATA1	Output	1 bit	Trace data output 1
TDATA2	Output	1 bit	Trace data output 2
TDATA3	Output	1 bit	Trace data output 3
TDO/SWO	Output	1 bit	Serial wire output Multiplexed with JTAG TDO pin

2.4 JTAG/SWD Interface

Table 2.3 shows the JTAG/SWD pins.

2.2 MCU实施选项

Table 2.1 实施选项

Option	Implementation
MPU	包括，8个保护区
FPB	FlashPatch（remap）功能不可用，只有断点功能可用
FPU	Included
中断数	96
优先级位数	4
唤醒中断控制器数量(WIC*1)	不包含
睡眠模式省电	支持睡眠模式和其他低功耗模式。有关详细信息，请参阅第11节，低功耗模式。 Note: SCB.SCR.SLEEPDEEP被忽略。
Endianness	Little-endian
SysTick SYST_CALIB register	SYST_CALIB = 4000 0147h 位[31]=0提供参考时钟 位[30]=1TERMS值不准确 位[29:24]=00h保留 位[23:0]=000147hTERM：(32768×10ms)132.768kHz=326.66十进制=327，偏斜=000147h
Event input/output	未实现
系统复位请求输出	应用程序中断和复位控制寄存器中的SYSRESETREQ位导致CPU复位
辅助故障输入(AUXFAULT)	未实现

Note 1. ICU可以唤醒CPU而不是唤醒中断控制器(WIC)。有关详细信息，请参阅第14节，中断控制器单元（ICU）。

2.3 跟踪接口

跟踪端口接口单元(TPIU)和串行线输出(SWO)提供跟踪输出。表2.2显示了该功能的MCU引脚。这些引脚与其他功能复用。

Table 2.2 跟踪功能引脚

Name	I/O	Width	Function
TCLK	Output	1 bit	跟踪时钟
TDATA0	Output	1 bit	跟踪数据输出0
TDATA1	Output	1 bit	跟踪数据输出1
TDATA2	Output	1 bit	跟踪数据输出2
TDATA3	Output	1 bit	跟踪数据输出3
TDO/SWO	Output	1 bit	串行线输出 与JTAGTDO引脚复用

2.4 JTAG/SWD Interface

表2.3显示了JTAGSWD引脚。

Table 2.3 JTAG/SWD pins

Name	I/O	P/N	Width	Function	When not in use
TCK/SWCLK	Input	Pos.	1 bit	JTAG clock pin	Pull-up
TMS/SWDIO	I/O	Neg.	1 bit	JTAG TMS pin SWD I/O pin	Pull-up
TDI	Input	Pos.	1 bit	JTAG TDI pin	Pull-up
TDO/SWO	Output	Neg.	1 bit	JTAG TDO pin Multiplexed with serial wire output	Open

2.5 Debug Mode

2.5.1 Debug Mode Definition

In single chip mode, the debugger state of the connection is defined as OCD mode, the debugger state of the unconnected is defined as User mode.

Table 2.4 shows the CPU debug modes and conditions.

Table 2.4 CPU debug mode and conditions

Conditions		Mode	
OCD connect	**JTAG/SWD authentication**	**Debug mode**	**Debug authentication**
Not connected	—	User mode	Disabled
Connected	Failed	User mode	Disabled
Connected	Passed	OCD mode	Enabled

Note 1. OCD connect is determined by the CDBGPWRUPREQ bit output in the SWJ-DP register. The bit can only be written by the OCD. However, the level of the bit can be confirmed by reading the DBGSTR.CDBGPWRUPREQ bit.
Note 2. Debug Authentication is defined by the ARMv7-M Architecture. Enabled means that both invasive and non-invasive CPU debugging are permitted. Disabled means that both are not permitted.

2.5.2 Debug Mode Effects

This section describes the effects of debug mode, which occur both internally and externally to the CPU.

2.5.2.1 Low power mode

All CoreSight debug components can store the register settings even when the CPU enters Software Standby, Snooze, or Deep Software Standby mode. However, AHB-AP cannot respond to On-Chip Debug (OCD) access in these low power modes. The OCD must wait for cancellation of the low power mode to access the CoreSight debug components. To request low power mode cancellation, the OCD can set the DBIRQ bit in the MCUCTRL register. For details, see section 2.6.5.3, MCU Control Register (MCUCTRL).

2.5.2.2 Reset

In OCD mode, some resets depend on the CPU status and the DBGSTOPCR setting.

Table 2.5 Reset or interrupt and mode setting (1 of 2)

	Control in On-Chip Debug (OCD) mode	
Reset or interrupt name	**OCD break mode**	**OCD run mode**
RES pin reset	Same as user mode	
Power-on reset	Same as user mode	
Independent watchdog timer reset/interrupt	Does not occur*1	Depends on DBGSTOPCR setting*2
Watchdog timer reset/interrupt	Does not occur*1	Depends on DBGSTOPCR setting*2
Voltage monitor 0 reset	Depends on DBGSTOPCR setting*3	

Table 2.3 JTAG/SWD pins

Name	I/O	P/N	Width	Function	不使用时
TCK/SWCLK	Input	Pos.	1 bit	JTAG时钟引脚	Pull-up
TMS/SWDIO	I/O	Neg.	1 bit	JTAG TMS pin SWD I/O pin	Pull-up
TDI	Input	Pos.	1 bit	JTAG TDI pin	Pull-up
TDO/SWO	Output	Neg.	1 bit	JTAGTDO引脚 与串行线输出复用	Open

2.5 调试模式

2.5.1 调试模式定义

在单片机模式下，连接的调试器状态定义为OCD模式，未连接的调试器状态定义为用户模式。

表2.4显示了CPU调试模式和条件。

Table 2.4 CPU调试模式和条件

Conditions		Mode	
强迫症连接	**JTAG/SWD authentication**	**调试模式**	**调试认证**
未连接	—	用户模式	Disabled
Connected	Failed	用户模式	Disabled
Connected	Passed	强迫症模式	Enabled

Note 1. OCD连接由SWJ-DP寄存器中的CDBGPWRUPREQ位输出决定。该位只能由强迫症。但是，可以通过读取DBGSTR.CDBGPWUPREQ位来确认该位的电平。
Note 2. 调试身份验证由ARMv7-M体系结构定义。启用意味着允许侵入式和非侵入式CPU调试。禁用意味着两者都不允许。

2.5.2 调试模式效果

本节描述调试模式的影响，它在CPU内部和外部都发生。

2.5.2.1 低功耗模式

即使CPU进入软件待机、贪睡或深度软件待机模式，所有CoreSight调试组件都可以存储寄存器设置。但是，AHB-AP在这些低功耗模式下无法响应片上调试(OCD)访问。OCD必须等待取消低功耗模式才能访问CoreSight调试组件。要请求取消低功耗模式，OCD可以设置MCUCTRL寄存器中的DBIRQ位。有关详细信息，请参见第2.6.5.3节，MCU控制寄存器（MCUCTRL）。

2.5.2.2 Reset

在OCD模式下，一些复位取决于CPU状态和DBGSTOPCR设置。

Table 2.5 复位或中断和模式设置（1of2）

	片上调试(OCD)模式下的控制	
重置或中断名称	**强迫症休息模式**	**强迫症运行模式**
RES引脚复位	与用户模式相同	
Power-on reset	与用户模式相同	
独立看门狗定时器复位中断	不发生*1	取决于DBGSTOPCR设置*2
看门狗定时器复位中断	不发生*1	取决于DBGSTOPCR设置*2
电压监控器0复位	取决于DBGSTOPCR设置*3	

Table 2.5 Reset or interrupt and mode setting (2 of 2)

Reset or interrupt name	Control in On-Chip Debug (OCD) mode	
	OCD break mode	OCD run mode
Voltage monitor 1 reset/interrupt	Depends on DBGSTOPCR setting*3	
Voltage monitor 2 reset/interrupt	Depends on DBGSTOPCR setting*3	
SRAM parity error reset/interrupt	Depends on DBGSTOPCR setting*3	
SRAM ECC error reset/interrupt	Depends on DBGSTOPCR setting*3	
MPU bus master reset/interrupt	Same as user mode	
MPU bus slave reset/interrupt	Same as user mode	
Stack pointer error reset/interrupt	Same as user mode	
Deep software standby reset	Same as user mode	
Software reset	Same as user mode	

Note: In OCD break mode, the CPU is halted. In OCD run mode, the CPU is in OCD mode and the CPU is not halted.
Note 1. The IWDT and WDT always stop in this mode.
Note 2. IWDT and WDT operation depends on the DBGSTOPCR setting.
Note 3. Reset or interrupt masking depends on the DBGSTOPCR setting.

2.6 Programmers Model

2.6.1 Address Spaces

The MCU debug system includes two CoreSight Access Ports (AP):

- AHB-AP, which is connected to the CPU bus matrix and has the same access to the system address space as the CPU
- APB-AP, which has a dedicated address space (OCD address space) and is connected to the OCD register.

Figure 2.2 shows a block diagram of the AP connection and address spaces.

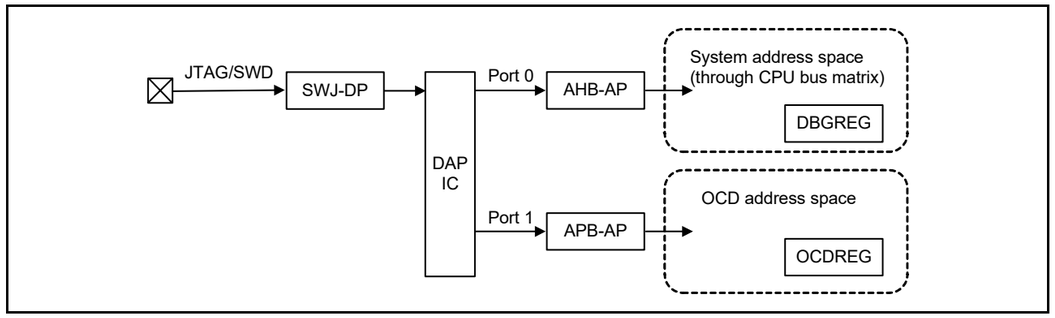


Figure 2.2 JTAG/SWD authentication block diagram

For debugging purposes, there are two register modules, DBGREG and OCDREG. DBGREG is located in the system address space can be accessed from the OCD emulator, CPU, and other bus masters in the MCU. OCDREG is located in the OCD address space and can only be accessed from the OCD tool. The CPU and other bus masters cannot access the OCD registers.

2.6.2 Cortex-M4 Peripheral Address Map

In the system address space, the Cortex-M4 core has a Private Peripheral Bus (PPB), which can be accessed only from the CPU and OCD emulator. The PPB is expanded from the Cortex-M4 original implementation for this MCU. Table 2.6 shows the address map of the MCU.

Table 2.5 复位或中断和模式设置(2of2)

重置或中断名称	片上调试(OCD)模式下的控制	
	强迫症休息模式	强迫症运行模式
电压监视器1复位中断	取决于DBGSTOPCR设置*3	
电压监视器2复位中断	取决于DBGSTOPCR设置*3	
SRAM奇偶校验错误复位中断	取决于DBGSTOPCR设置*3	
SRAM ECC error reset/interrupt	取决于DBGSTOPCR设置*3	
MPU总线主机复位中断	与用户模式相同	
MPU总线从机复位中断	与用户模式相同	
堆栈指针错误复位中断	与用户模式相同	
深度软件待机复位	与用户模式相同	
软件复位	与用户模式相同	

Note: 在OCD中断模式下，CPU停止。在OCD运行模式下，CPU处于OCD模式并且CPU不会停止。
Note 1. IWDT和WDT始终在此模式下停止。
Note 2. IWDT和WDT操作取决于DBGSTOPCR设置。
Note 3. 复位或中断屏蔽取决于DBGSTOPCR设置。

2.6 程序员模型

2.6.1 地址空间

MCU调试系统包括两个CoreSight访问端口(AP)：

- AHB-AP，与CPU总线矩阵相连，与系统地址空间具有相同的访问权限
CPU
- APB-AP，它有一个专用的地址空间（OCD地址空间），并与OCD寄存器相连。

图2.2显示了AP连接和地址空间的框图。

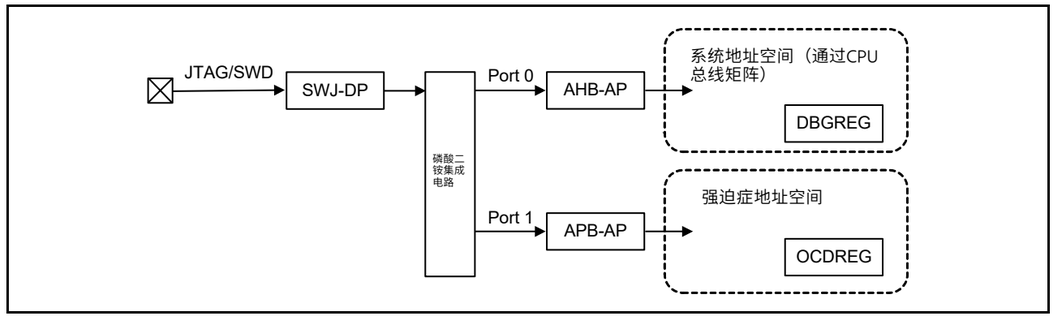


Figure 2.2 JTAGSWD认证框图

出于调试目的，有两个寄存器模块，DBGREG和OCDREG。DBGREG位于系统地址空间，可以从OCD仿真器、CPU和MCU中的其他总线主控器访问。OCDREG位于OCD地址空间，只能从OCD工具访问。CPU和其他总线主机无法访问OCD寄存器。

2.6.2 Cortex-M4外设地址映射

在系统地址空间中，Cortex-M4内核有一个私有外设总线(PPB)，只能从CPU和OCD仿真器访问。PPB是从该MCU的Cortex-M4原始实现扩展而来的。表2.6显示了MCU的地址映射。

Table 2.6 Cortex-M4 peripheral address map

Component name	Start address	End address	Note
ITM	E000 0000h	E000 0FFFh	See reference 2.
DWT	E000 1000h	E000 1FFFh	See reference 2.
FPB	E000 2000h	E000 2FFFh	See reference 2.
SCS	E000 E000h	E000 EFFFh	See reference 2.
TPIU	E004 0000h	E004 0FFFh	See reference 2.
ETM	E004 1000h	E004 1FFFh	See reference 5.
ATB funnel	E004 2000h	E004 2FFFh	See section 2.7 and reference 4.
ETB	E004 3000h	E004 3FFFh	See reference 6.
Time Stamp Generator	E004 4000h	E004 4FFFh	See section 2.10 and reference 4.
ROM Table	E00F F000h	E00F FFFFh	See section 2.6.3 and reference 7.

2.6.3 CoreSight ROM Table

The MCU contains one CoreSight ROM Table, which lists the Arm components.

2.6.3.1 ROM entries

Table 2.7 shows the ROM entries in the CoreSight ROM Table. The OCD emulator can use the ROM entries to determine which components are implemented in a system. See reference 7. for details.

Table 2.7 CoreSight ROM Table

#	Address	Access size	R/W	Value	Component
0	E00F F000h	32 bits	R	FFF0F003	NVIC
1	E00F F004h	32 bits	R	FFF02003	SWT
2	E00F F008h	32 bits	R	FFF03003	FPB
3	E00F F00Ch	32 bits	R	FFF01003	ITM
4	E00F F010h	32 bits	R	FFF41003	TPIU
5	E00F F014h	32 bits	R	FFF42003	ETM
6	E00F F018h	32 bits	R	FFF43003	Funnel
7	E00F F01Ch	32 bits	R	FFF44003	ETB
8	E00F F020h	32 bits	R	FFF45003	TSG
9	E00F F024h	32 bits	R	00000000	(End of entries)

2.6.3.2 CoreSight component registers

The CoreSight ROM Table lists the CoreSight component registers defined in the Arm CoreSight architecture.

Table 2.8 shows the registers. See reference 7. for details of each register.

Table 2.8 CoreSight component registers in the CoreSight ROM Table (1 of 2)

Name	Address	Access size	R/W	Initial value
DEVTYPE	E00F FFCCh	32 bits	R	00000001h
PID4	E00F FFD0h	32 bits	R	00000004h
PID5	E00F FFD4h	32 bits	R	00000000h
PID6	E00F FFD8h	32 bits	R	00000000h

Table 2.6 Cortex-M4外设地址映射

组件名称	起始地址	结束地址	Note
ITM	E000 0000h	E000 0FFFh	参见参考文献2。
DWT	E000 1000h	E000 1FFFh	参见参考文献2。
FPB	E000 2000h	E000 2FFFh	参见参考文献2。
SCS	E000 E000h	E000 EFFFh	参见参考文献2。
TPIU	E004 0000h	E004 0FFFh	参见参考文献2。
ETM	E004 1000h	E004 1FFFh	参见参考文献5。
ATB funnel	E004 2000h	E004 2FFFh	参见第2.7节和参考4。
ETB	E004 3000h	E004 3FFFh	参见参考文献6。
时间戳生成器	E004 4000h	E004 4FFFh	请参阅第2.10节和参考4。
只读存储器表	E00F F000h	E00F FFFFh	参见第2.6.3节和参考7。

2.6.3 CoreSightROM表

MCU包含一个CoreSightROM表，其中列出了Arm组件。

2.6.3.1 ROM条目

表2.7显示了CoreSightROM表中的ROM条目。OCD仿真器可以使用ROM条目来确定系统中实现了哪些组件。有关详细信息，请参见参考资料7。

Table 2.7 CoreSightROM表

#	Address	访问大小	R/W	Value	Component
0	E00F F000h	32 bits	R	FFF0F003	NVIC
1	E00F F004h	32 bits	R	FFF02003	SWT
2	E00F F008h	32 bits	R	FFF03003	FPB
3	E00F F00Ch	32 bits	R	FFF01003	ITM
4	E00F F010h	32 bits	R	FFF41003	TPIU
5	E00F F014h	32 bits	R	FFF42003	ETM
6	E00F F018h	32 bits	R	FFF43003	Funnel
7	E00F F01Ch	32 bits	R	FFF44003	ETB
8	E00F F020h	32 bits	R	FFF45003	TSG
9	E00F F024h	32 bits	R	00000000	(End of entries)

2.6.3.2 CoreSight组件寄存器

CoreSightROM表列出了ArmCoreSight架构中定义的CoreSight组件寄存器。

表2.8显示了寄存器。有关每个寄存器的详细信息，请参见参考资料7。

Table 2.8 CoreSightROM表中的CoreSight组件寄存器(1of2)

Name	Address	访问大小	R/W	初始值
DEVTYPE	E00F FFCCh	32 bits	R	00000001h
PID4	E00F FFD0h	32 bits	R	00000004h
PID5	E00F FFD4h	32 bits	R	00000000h
PID6	E00F FFD8h	32 bits	R	00000000h

Table 2.8 CoreSight component registers in the CoreSight ROM Table (2 of 2)

Name	Address	Access size	R/W	Initial value
PID7	E00F FFDCh	32 bits	R	00000000h
PID0	E00F FFE0h	32 bits	R	00000010h
PID1	E00F FFE4h	32 bits	R	00000030h
PID2	E00F FFE8h	32 bits	R	0000000Ah
PID3	E00F FFECh	32 bits	R	00000000h
CID0	E00F FFF0h	32 bits	R	0000000Dh
CID1	E00F FFF4h	32 bits	R	00000010h
CID2	E00F FFF8h	32 bits	R	00000005h
CID3	E00F FFFCh	32 bits	R	000000B1h

2.6.4 DBGREG Module

The DBGREG register module controls the debug functionalities and is implemented as a CoreSight-compliant component.

Table 2.9 shows the DBGREG registers other than the CoreSight component registers.

Table 2.9 Non-CoreSight DBGREG registers

Name		DAP port	Address	Access size	R/W
Debug Status Register	DBGSTR	Port 0	4001 B000h	32 bits	R
Debug Stop Control Register	DBGSTOPCR	Port 0	4001 B010h	32 bits	R/W
Trace Control Register	TRACECTR	Port 0	4001 B020h	32 bits	R/W

2.6.4.1 Debug Status Register (DBGSTR)

Address(es): DBG.DBGSTR 4001 B000h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	CDBGPWRUPACK	CDBGPWRUPREQ	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b27 to b0	—	Reserved	These bits are read as 0	R
b28	CDBGPWRUPREQ	Debug power-up request	0: OCD is not requesting debug power-up 1: OCD is requesting debug power-up.	R
b29	CDBGPWRUPACK	Debug power-up acknowledge	0: Debug power-up request is not acknowledged 1: Debug power-up request is acknowledged.	R
b31, b30	—	Reserved	These bits are read as 0	R

Table 2.8 CoreSightROM表中的CoreSight组件寄存器(2of2)

Name	Address	访问大小	R/W	初始值
PID7	E00F FFDCh	32 bits	R	00000000h
PID0	E00F FFE0h	32 bits	R	00000010h
PID1	E00F FFE4h	32 bits	R	00000030h
PID2	E00F FFE8h	32 bits	R	0000000Ah
PID3	E00F FFECh	32 bits	R	00000000h
CID0	E00F FFF0h	32 bits	R	0000000Dh
CID1	E00F FFF4h	32 bits	R	00000010h
CID2	E00F FFF8h	32 bits	R	00000005h
CID3	E00F FFFCh	32 bits	R	000000B1h

2.6.4 DBGREG Module

DBGREG寄存器模块控制调试功能，并被实现为符合CoreSight的组件。

表2.9显示了除CoreSight组件寄存器之外的DBGREG寄存器。

Table 2.9 Non-CoreSight DBGREG registers

Name		端口	Address	访问大小	R/W
调试状态寄存器	DBGSTR	Port 0	4001 B000h	32 bits	R
调试停止控制寄存器	DBGSTOPCR	Port 0	4001 B010h	32 bits	R/W
跟踪控制寄存器	TRACECTR	Port 0	4001 B020h	32 bits	R/W

2.6.4.1 调试状态寄存器(DBGSTR)

Address(es): DBG.DBGSTR 4001 B000h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	CDBGPWRUPACK	CDBGPWRUPREQ	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b27 to b0	—	Reserved	这些位被读为0	R
b28	CDBGPWRUPREQ	调试上电请求	0：OCD不请求调试上电1：OCD请求调试上电。	R
b29	CDBGPWRUPACK	调试上电确认	0：未确认调试上电请求1：确认调试上电请求。	R
b31, b30	—	Reserved	这些位被读为0	R

2.6.4.2 Debug Stop Control Register (DBGSTOPCR)

Address(es): DBG.DBGSTOPCR 4001 B010h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	DBGSTOP_RECCR	DBGSTOP_RPER	—	—	—	—	—	DBGSTOP_LVD[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DBGSTOP_WDT	DBGSTOP_IWDT
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bit	Symbol	Bit name	Description	R/W
b0	DBGSTOP_IWDT	Mask bit for IWDT reset or interrupt	0: Enable IWDT reset or interrupt 1: Mask IWDT reset or interrupt and stop WDT count when CPU is in OCD break mode.	R/W
b1	DBGSTOP_WDT	Mask bit for WDT reset or interrupt	0: Enable WDT reset or interrupt 1: Mask WDT reset or interrupt and stop WDT count when CPU is in OCD break mode.	R/W
b15 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b16	DBGSTOP_LVD[2:0]	Mask bit for LVD0 reset	0: Enable LVD0 reset 1: Mask LVD0 reset.	R/W
b17		Mask bit for LVD1 reset or interrupt	0: Enable LVD1 reset or interrupt 1: Mask LVD1 reset or interrupt.	R/W
b18		Mask bit for LVD2 reset or interrupt	0: Enable LVD2 reset or interrupt 1: Mask LVD2 reset or interrupt.	R/W
b23 to b19	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b24	DBGSTOP_RPER	Mask bit for SRAM parity error reset or interrupt	0: Enable SRAM parity error reset or interrupt 1: Mask SRAM parity error reset or interrupt.	R/W
b25	DBGSTOP_RECCR	Mask bit for SRAM ECC error reset or interrupt	0: Enable SRAM ECC error reset or interrupt 1: Mask SRAM ECC error reset or interrupt.	R/W
b31 to b26	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The Debug Stop Control Register (DBGSTOPCR) specifies the functional stop in OCD mode. All bits in the register are regarded as 0 when the MCU is not in OCD mode.

2.6.4.3 Trace Control Register (TRACECTR)

Address(es): DBG.TRACECTR 4001 B020h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	ENETB FULL	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b30 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

2.6.4.2 调试停止控制寄存器(DBGSTOPCR)

Address(es): DBG.DBGSTOPCR 4001 B010h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	DBGSTOP_RECCR	DBGSTOP_RPER	—	—	—	—	—	DBGSTOP_LVD[2:0]		
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DBGSTOP_WDT	DBGSTOP_IWDT
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bit	Symbol	位名称	Description	R/W
b0	DBGSTOP_IWDT	IWDT复位或中断屏蔽位	0：使能IWDT复位或中断1：当CPU处于OCD中断模式时，屏蔽IWDT复位或中断并停止WDT计数。	R/W
b1	DBGSTOP_WDT	WDT复位或中断屏蔽位	0：使能WDT复位或中断1：当CPU处于OCD中断模式时，屏蔽WDT复位或中断并停止WDT计数。	R/W
b15 to b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b16	DBGSTOP_LVD[2:0]	LVD0复位屏蔽位	0：使能LVD0复位1 ：屏蔽LVD0复位。	R/W
b17		LVD1复位或中断的屏蔽位	0：使能LVD1复位或中断1：屏蔽LVD1复位或中断。	R/W
b18		LVD2复位或中断的屏蔽位	0：使能LVD2复位或中断1：屏蔽LVD2复位或中断。	R/W
b23 to b19	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b24	DBGSTOP_RPER	SRAM奇偶校验错误复位或中断的屏蔽位	0：使能SRAM奇偶校验错误复位或中断1：屏蔽SRAM奇偶校验错误复位或中断。	R/W
b25	DBGSTOP_RECCR	SRAMECC错误复位或中断的屏蔽位	0：使能SRAMECC错误复位或中断1：屏蔽SRAMECC错误复位或中断。	R/W
b31 to b26	—	Reserved	这些位被读取为0。写入值应为0。	R/W

调试停止控制寄存器(DBGSTOPCR)指定OCD模式下的功能停止。当MCU不处于OCD模式时，寄存器中的所有位都被视为0。

2.6.4.3 跟踪控制寄存器(TRACECTR)

Address(es): DBG.TRACECTR 4001 B020h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	ENETB FULL	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b30 to b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Bit	Symbol	Bit name	Description	R/W
b31	ENETBFULL	Enable bit for halt request on ETB full	0: ETB full does not cause a CPU halt 1: ETB full causes a CPU halt.	R/W

2.6.4.4 DBGREG CoreSight component registers

The DBGREG module provides the CoreSight component registers defined in the Arm CoreSight architecture.

Table 2.10 shows these registers. See reference 7. for details of each register.

Table 2.10 DBGREG CoreSight component registers

Name	Address	Access size	R/W	Initial value
PID4	4001 BFD0h	32 bits	R	00000004h
PID5	4001 BFD4h	32 bits	R	00000000h
PID6	4001 BFD8h	32 bits	R	00000000h
PID7	4001 BFDCh	32 bits	R	00000000h
PID0	4001 BFE0h	32 bits	R	00000005h
PID1	4001 BFE4h	32 bits	R	00000030h
PID2	4001 BFE8h	32 bits	R	0000001Ah
PID3	4001 BFECh	32 bits	R	00000000h
CID0	4001 BFF0h	32 bits	R	0000000Dh
CID1	4001 BFF4h	32 bits	R	000000F0h
CID2	4001 BFF8h	32 bits	R	00000005h
CID3	4001 BFFCh	32 bits	R	000000B1h

2.6.5 OCDREG Module

The OCDREG register module controls the On-Chip Debug (OCD) emulator functionalities and is implemented as a CoreSight-compliant component.

Table 2.11 shows the OCDREG registers other than the CoreSight component registers.

Table 2.11 Non-CoreSight OCDREG registers

Name		DAP port	Address	Access size	R/W
ID Authentication Code Register 0	IAUTH0	Port 1	8000_0000	32 bits	W
ID Authentication Code Register 1	IAUTH1	Port 1	8000_0100	32 bits	W
ID Authentication Code Register 2	IAUTH2	Port 1	8000_0200	32 bits	W
ID Authentication Code Register 3	IAUTH3	Port 1	8000_0300	32 bits	W
MCU Status Register	MCUSTAT	Port 1	8000 0400h	32 bits	R
MCU Control Register	MCUCTRL	Port 1	8000 0410h	32 bits	R/W

Note: OCDREG is located in the dedicated OCD address space. This address map is independent from the system address map. See section 2.6.2, Cortex-M4 Peripheral Address Map.

2.6.5.1 ID Authentication Code Register (IAUTH0 to 3)

Four authentication registers are provided for writing the 128-bit key. The registers must be written in sequential order from IAUTH0 to IAUTH3. If the set of register writes is not compliant with this order, the result is unpredictable.

Only 32-bit writes are permitted. The initial value of the registers is all 1s. This means that JTAG/SWD access is initially permitted when the ID code in the OSIS register has the initial value. See section 2.11.2, Unlock ID Code.

Bit	Symbol	位名称	Description	R/W
b31	ENETBFULL	启用停止请求的位 ETB full	0：ETB满不导致CPU停止1：ETB满导致CPU停止。	R/W

2.6.4.4 DBGREGCoreSight组件寄存器

DBGREG模块提供在ArmCoreSight架构中定义的CoreSight组件寄存器。

表2.10显示了这些寄存器。有关每个寄存器的详细信息，请参见参考资料7。

Table 2.10 DBGREGCoreSight组件寄存器

Name	Address	访问大小	R/W	初始值
PID4	4001 BFD0h	32 bits	R	00000004h
PID5	4001 BFD4h	32 bits	R	00000000h
PID6	4001 BFD8h	32 bits	R	00000000h
PID7	4001 BFDCh	32 bits	R	00000000h
PID0	4001 BFE0h	32 bits	R	00000005h
PID1	4001 BFE4h	32 bits	R	00000030h
PID2	4001 BFE8h	32 bits	R	0000001Ah
PID3	4001 BFECh	32 bits	R	00000000h
CID0	4001 BFF0h	32 bits	R	0000000Dh
CID1	4001 BFF4h	32 bits	R	000000F0h
CID2	4001 BFF8h	32 bits	R	00000005h
CID3	4001 BFFCh	32 bits	R	000000B1h

2.6.5 OCDREG Module

OCDREG寄存器模块控制片上调试(OCD)仿真器功能，并实现为CoreSight-compliant component.

表2.11显示了除CoreSight组件寄存器之外的OCDREG寄存器。

Table 2.11 Non-CoreSight OCDREG registers

Name		端口	Address	访问大小	R/W
ID验证码寄存器0	IAUTH0	Port 1	8000_0000	32 bits	W
ID验证码寄存器1	IAUTH1	Port 1	8000_0100	32 bits	W
ID验证码寄存器2	IAUTH2	Port 1	8000_0200	32 bits	W
ID验证码寄存器3	IAUTH3	Port 1	8000_0300	32 bits	W
MCU状态寄存器	MCUSTAT	Port 1	8000 0400h	32 bits	R
MCU控制寄存器	MCUCTRL	Port 1	8000 0410h	32 bits	R/W

Note: OCDREG位于专用的OCD地址空间中。该地址映射独立于系统地址映射。
请参阅第2.6.2节，Cortex-M4外设地址映射。

2.6.5.1 ID验证码寄存器（IAUTH0至3）

提供了四个认证寄存器用于写入128位密钥。寄存器必须按IAUTH0到IAUTH3的顺序写入。如果寄存器写入的集合不符合此顺序，则结果是不可预测的。

只允许32位写入。寄存器的初始值全为1。这意味着当OSIS寄存器中的ID代码具有初始值时，最初允许JTAGS WD访问。请参阅第2.11.2节，解锁ID代码。

Address(es): IAUTH0 8000 0000h

b31	b0
IAUTH0: AID 31-0 bits	

Value after reset: 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1

Address(es): IAUTH1 8000 0100h

b31	b0
IAUTH1: AID 63-32 bits	

Value after reset: 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1

Address(es): IAUTH2 8000 0200h

b31	b0
IAUTH2: AID 95-64 bits	

Value after reset: 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1

Address(es): IAUTH3 8000 0300h

b31	b0
IAUTH3: AID 127-96 bits	

Value after reset: 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1

2.6.5.2 MCU Status Register (MCUSTAT)

Address(es): MCUSTAT 8000 0400h

b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Value after reset:

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
—	—	—	—	—	—	—	—	—	—	—	—	—	CPUSTOPCLK	CPUSLEEP	AUTH
0	0	0	0	0	0	0	0	0	0	0	0	0	1/0*1	1/0*1	0

Value after reset:

Bit	Symbol	Bit name	Description	R/W
b0	AUTH	Authentication status	0: Authentication failed 1: Authentication succeeded.	R
b1	CPUSLEEP		0: CPU is not in Sleep mode 1: CPU is in Sleep mode.	R
b2	CPUSTOPCLK		0: CPU clock is not stopped. This indicates that the MCU is in Normal or Sleep mode 1: CPU clock is stopped. This indicates that the MCU is in Snooze or Software Standby mode.	R
b31 to b3	—	Reserved	These bits are read as 0.	R

Note 1. Depends on the MCU status.

Address(es): IAUTH0 8000 0000h

b31	b0
IAUTH0：AID31-0位	

重置后的值: 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1

Address(es): IAUTH1 8000 0100h

b31	b0
IAUTH1：AID63-32位	

重置后的值: 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1

Address(es): IAUTH2 8000 0200h

b31	b0
IAUTH2：AID95-64位	

重置后的值: 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1

Address(es): IAUTH3 8000 0300h

b31	b0
IAUTH3：AID127-96位	

重置后的值: 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1 1

2.6.5.2 MCU状态寄存器(MCUSTAT)

Address(es): MCUSTAT 8000 0400h

b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

重置后的值:

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
—	—	—	—	—	—	—	—	—	—	—	—	—	CPUSTOPCLK	CPUSLEEP	AUTH
0	0	0	0	0	0	0	0	0	0	0	0	0	1/0*1	1/0*1	0

重置后的值:

Bit	Symbol	位名称	Description	R/W
b0	AUTH	认证状态	0：认证失败1：认证成功。	R
b1	CPUSLEEP		0：CPU不处于休眠模式1： CPU处于休眠模式。	R
b2	CPUSTOPCLK		0：CPU时钟不停止。这表明MCU处于正常或睡眠模式1：CPU时钟停止。这表明MCU处于贪睡或软件待机模式。	R
b31 to b3	—	Reserved	这些位读为0。	R

Note 1. 取决于MCU状态。

2.6.5.3 MCU Control Register (MCUCTRL)

Address(es): MCUCTRL 8000 0410h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	DBIRQ	—	—	—	—	—	—	—	EDBGRQ
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	EDBGRQ	External Debug Request	Writing 1 to the bit causes a CPU halt or debug monitor exception: 0: Debug event not requested 1: Debug event requested. When the EDBGRQ bit is set to 0 or the CPU is halted, the EDBCRQ bit is cleared.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	DBIRQ	Debug Interrupt Request	Writing 1 to the bit wakes the MCU from low power mode: 0: Debug interrupt not requested 1: Debug interrupt requested. The condition can be cleared by writing 0 to the DBIRQ bit.	R/W
b31 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Set DBIRQ and EDBGRQ to the same value.

2.6.5.4 CoreSight component registers

The DBGREG module provides the CoreSight component registers defined in the Arm CoreSight architecture. Table 2.12 lists these registers. See reference 7. for details.

Table 2.12 DBGREG registers

Name	Address	Access size	R/W	Initial value
PID4	8000 0FD0h	32 bits	R	00000004h
PID5	8000 0FD4h	32 bits	R	00000000h
PID6	8000 0FD8h	32 bits	R	00000000h
PID7	8000 0FDCh	32 bits	R	00000000h
PID0	8000 0FE0h	32 bits	R	00000004h
PID1	8000 0FE4h	32 bits	R	00000030h
PID2	8000 0FE8h	32 bits	R	0000000Ah
PID3	8000 0FECh	32 bits	R	00000000h
CID0	8000 0FF0h	32 bits	R	0000000Dh
CID1	8000 0FF4h	32 bits	R	000000F0h
CID2	8000 0FF8h	32 bits	R	00000005h
CID3	8000 0FFCh	32 bits	R	000000B1h

2.7 CoreSight ATB Funnel

There is one CoreSight ATB funnel in the MCU. The funnel has two ATB slaves and one ATB master, and it is used to select the debug trace source from ETM and ITM to ETB. Figure 2.3 shows the CoreSight ATB connection in the MCU.

2.6.5.3 MCU控制寄存器(MCUCTRL)

Address(es): MCUCTRL 8000 0410h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	DBIRQ	—	—	—	—	—	—	—	EDBGRQ
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	EDBGRQ	外部调试 Request	向该位写入1会导致CPU停止或调试监视器异常：0：未请求调试事件1：已请求调试事件。当EDBGRQ位设置为0或CPU停止时， EDBCRQ位清零。	R/W
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b8	DBIRQ	调试中断 Request	向该位写入1将MCU从低功耗模式唤醒：0：未请求调试中断1：请求调试中断。可以通过将0写入DBIRQ位来清除该条件。	R/W
b31 to b9	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note: 将DBIRQ和EDBGRQ设置为相同的值。

2.6.5.4 CoreSight组件寄存器

DBGREG模块提供在ArmCoreSight架构中定义的CoreSight组件寄存器。表2.12列出了这些寄存器。有关详细信息，请参见参考资料7。

Table 2.12 DBGREG registers

Name	Address	访问大小	R/W	初始值
PID4	8000 0FD0h	32 bits	R	00000004h
PID5	8000 0FD4h	32 bits	R	00000000h
PID6	8000 0FD8h	32 bits	R	00000000h
PID7	8000 0FDCh	32 bits	R	00000000h
PID0	8000 0FE0h	32 bits	R	00000004h
PID1	8000 0FE4h	32 bits	R	00000030h
PID2	8000 0FE8h	32 bits	R	0000000Ah
PID3	8000 0FECh	32 bits	R	00000000h
CID0	8000 0FF0h	32 bits	R	0000000Dh
CID1	8000 0FF4h	32 bits	R	000000F0h
CID2	8000 0FF8h	32 bits	R	00000005h
CID3	8000 0FFCh	32 bits	R	000000B1h

2.7 CoreSight ATB Funnel

MCU中有一个CoreSightATB漏斗。该漏斗有两个ATB从机和一个ATB主机，用于选择从ETM和ITM到ETB的调试跟踪源。图2.3显示了MCU中的CoreSightATB连接。

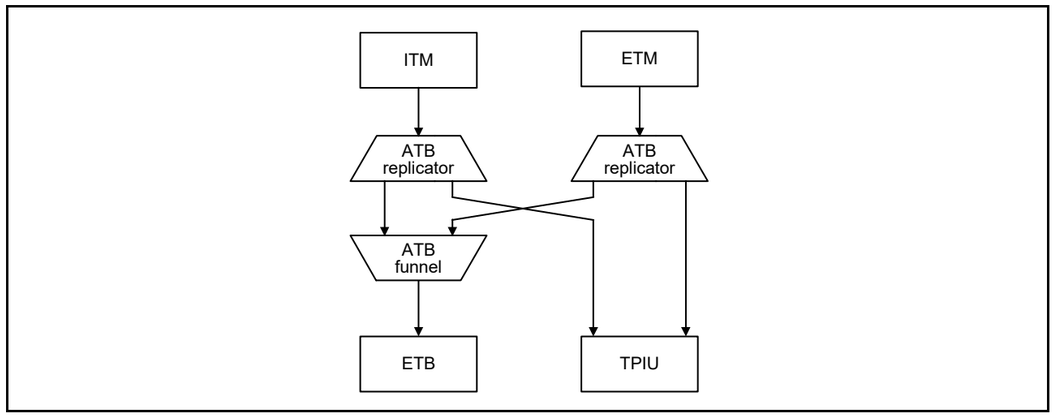


Figure 2.3 CoreSight ATB connection

Table 2.13 shows the ATB slave connection for the funnel.

Table 2.13 ATB slave connection

ATB slave number	Connected trace source
#0	ITM
#1	ETM

For details on the ATB and funnel, see reference 4.

2.8 Flash Patch and Break Unit

The MCU has a Flash Patch and Break Unit. Breakpoint function is available, but flash patch (remap) function is unavailable. Therefore, do not set 00b as the REPLACE bit (bit[31:30]) of the FP_COMPn register. Bit 28 of FP_REMAP register is fixed at 1b. When writing in this register, write 1b in bit 28. When reading this register, bit 28 always is read as 1b.

For details, see “Flash Patch and Breakpoint unit” chapter of reference 1.

2.9 SysTick System Timer

The SysTick system timer provides a simple 24-bit down counter. The reference clock for the timer can be selected as the CPU clock (ICLK) or SysTick Timer clock (SYSTICCLK). See reference 1.*1 for details.

Note 1. In the reference, the IMPLEMENTATION DEFINED external reference clock is SYSTICCLK (LOCO), and the processor clock is ICLK.

2.10 CoreSight Time Stamp Generator

A CoreSight Time Stamp Generator provides a CPU clock-based timestamp to ITM and ETM. The 48 LSB bits of the 64-bit counter are used for the two components. See reference 4. for details.

2.11 OCD Emulator Connection

A JTAG/SWD authentication mechanism checks access permission for debug and MCU resources. To obtain full debug functionality, a pass result of the authentication mechanism is required.

Figure 2.4 shows a block diagram of the authentication mechanism.

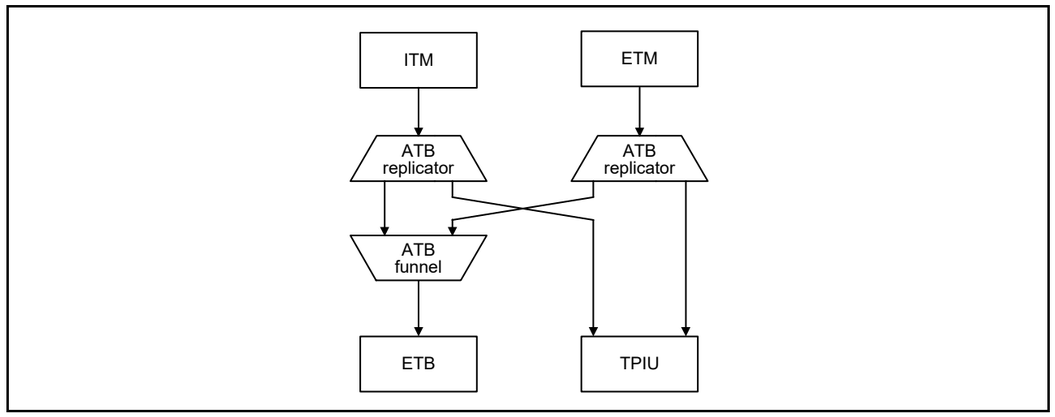


Figure 2.3 CoreSight ATB connection

表2.13显示了漏斗的ATB从属连接。

Table 2.13 ATB从机连接

ATB从机号	连接的跟踪源
#0	ITM
#1	ETM

有关ATB和漏斗的详细信息，请参见参考资料4。

2.8 闪存补丁和中断单元

MCU有一个闪存补丁和中断单元。断点功能可用，但闪存补丁（重映射）功能不可用。因此，不要将00b设置为FP_COMPn寄存器的REPLACE位(bit[31:30])。FP_REMAP寄存器的第28位固定为1b。写入该寄存器时，将1b写入位28。读取该寄存器时，位28始终被读取为1b。

有关详细信息，请参阅参考资料1的“Flash补丁和断点单元”一章。

2.9 SysTick系统定时器

SysTick系统定时器提供了一个简单的24位递减计数器。定时器的参考时钟可以选择为CPU时钟(ICLK)或SysTick定时器时钟(SYSTICCLK)。详见参考文献1。*1。

注1.在参考中，实现定义的外部参考时钟是SYSTICCLK(LOCO)，处理器时钟是ICLK。

2.10 CoreSight时间戳生成器

CoreSight时间戳生成器为ITM和ETM提供基于CPU时钟的时间戳。64位计数器的48个LSB位用于这两个组件。详见参考文献4。

2.11 OCD模拟器连接

JTAGSWD验证机制检查调试和MCU资源的访问权限。要获得完整的调试功能，需要验证机制的通过结果。

图2.4显示了认证机制的框图。

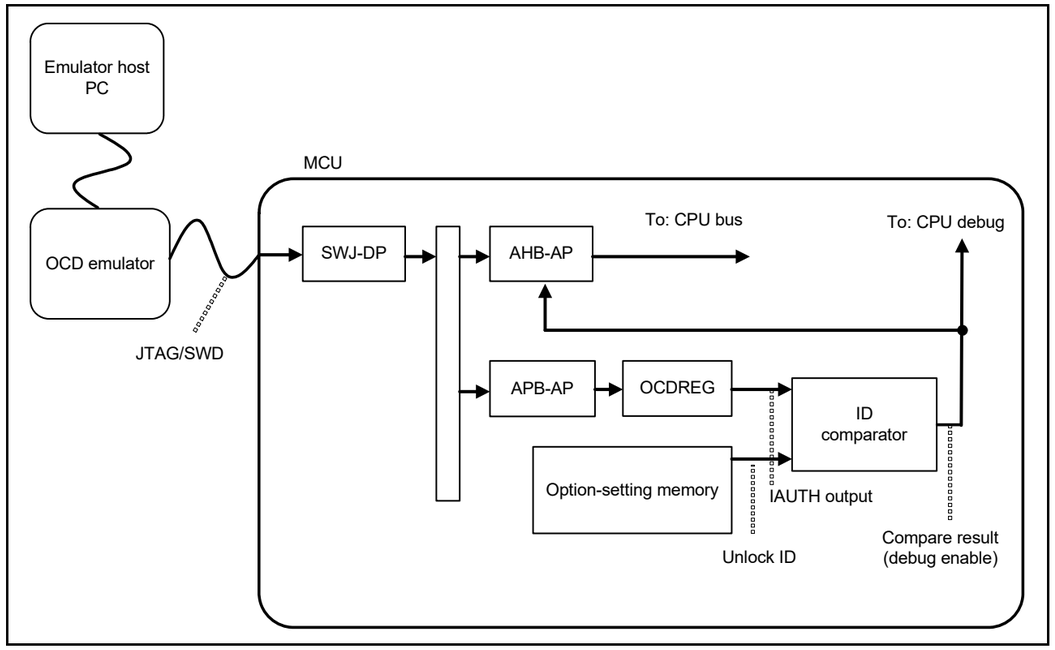


Figure 2.4 Authentication mechanism block diagram

An ID comparator is available in the MCU for authentication. The comparator compares the 128-bit IAUTH output from OCDREG and the 128-bit unlock ID code from the option-setting memory. When the two outputs are identical, the CPU debug functions and system bus access from the OCD emulator are permitted. After the OCD emulator gets access permission, the OCD emulator must set the DBGEN bit in the System Control OCD Control Register (SYOCDCR). In addition, the OCD emulator must clear the DBGEN bit before disconnecting.

2.11.1 DBGEN

After the OCD emulator gets access permission, the OCD emulator must set the DBGEN bit in the System Control OCD Control Register (SYOCDCR). In addition, the OCD emulator must clear the DBGEN bit before disconnecting it. See section 11, Low Power Modes for details.

2.11.2 Unlock ID Code

The unlock ID code is used for checking permission for debug and access to on-chip resources. If the unlock ID code matches the 128-bit data written in ID Authentication Registers 0 to 3, the JTAG/SWD debugger obtains access permission. The unlock ID code is written in the OCD/Serial Programmer ID Setting Register (OSIS) in the option-setting memory. The initial value of the unlock ID code is all 1s (FFFFFFFF_FFFFFFFF_FFFFFFFFh). See section 7, Option-Setting Memory.

2.11.3 Restrictions on Connecting an OCD Emulator

This section describes the restrictions on emulator access.

2.11.3.1 Starting connection while in a low power mode

When starting a JTAG/SWD connection from an OCD emulator, the MCU must be in Normal or Sleep mode. If the MCU is in Software Standby, Snooze, or Deep Software Standby mode, the OCD emulator can cause the MCU to hang.

2.11.3.2 Changing low power mode while in OCD mode

When the MCU is in OCD mode, the low power mode can be changed. However, system bus access from AHB-AP is prohibited in Software Standby, Snooze, or Deep Software Standby mode. Only SWJ-DP, APB-AP, and OCDREG can

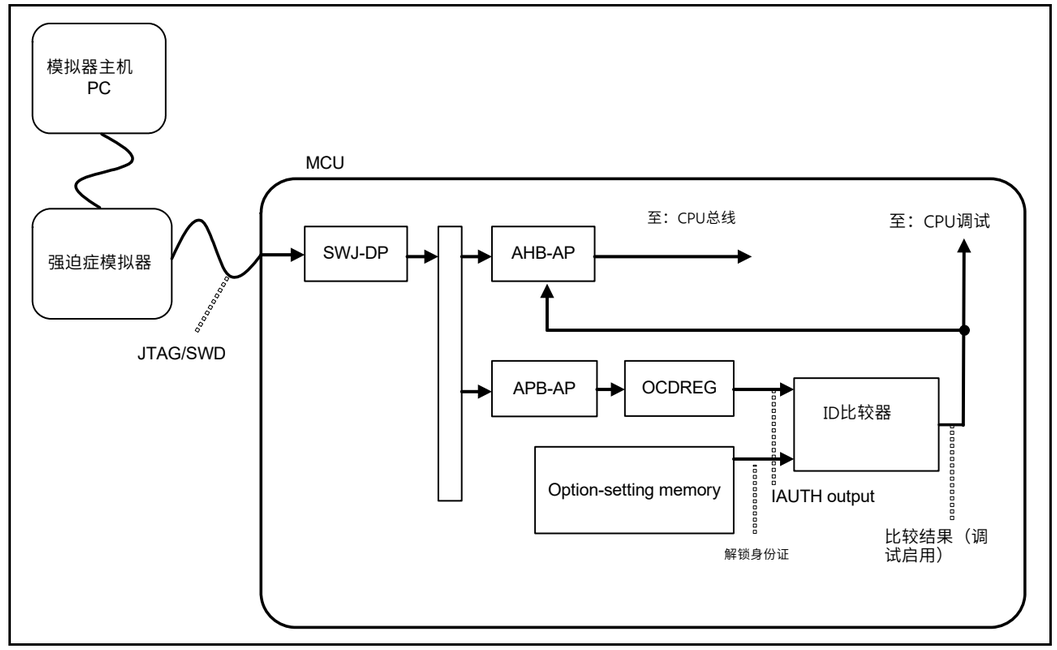


Figure 2.4 认证机制框图

MCU中有一个ID比较器用于身份验证。比较器比较来自OCDREG的128位IAUTH输出和来自选项设置存储器的128位解锁ID代码。当两个输出相同时，允许从OCD仿真器访问CPU调试功能和系统总线。在OCD仿真器获得访问权限后，OCD仿真器必须设置系统控制OCD控制寄存器(SYOCDCR)中的DBGEN位。此外，OCD仿真器必须在断开连接之前清除DBGEN位。

2.11.1 DBGEN

OCD模拟器获得访问权限后，OCD模拟器必须设置SystemControlOCD中的DBGEN位控制寄存器(SYOCDCR)。此外，OCD仿真器必须在断开连接之前清除DBGEN位。有关详细信息，请参见第11节，低功耗模式。

2.11.2 解锁ID码

解锁ID码用于检查是否允许调试和访问片上资源。如果解锁ID代码与ID验证寄存器0到3中写入的128位数据匹配，则JTAGSWD调试器获得访问权限。解锁ID代码写入选项设置存储器中的OCD串行编程器ID设置寄存器(OSIS)。解锁ID码初始值为全1（FFFFFFFF_FFFFFFFF_FFFFFFFFh）。请参阅第7节，选项设置内存。

2.11.3 连接强迫症模拟器的限制

本节介绍对仿真器访问的限制。

2.11.3.1 在低功耗模式下开始连接

从OCD仿真器启动JTAGSWD连接时，MCU必须处于正常或睡眠模式。如果MCU处于软件待机、贪睡或深度软件待机模式，OCD仿真器会导致MCU挂起。

2.11.3.2 在OCD模式下更改低功耗模式

当MCU处于OCD模式时，可以更改低功耗模式。但是，在软件待机、贪睡或深度软件待机模式下，禁止从AHB-AP访问系统总线。只有SWJ-DP、APB-AP和OCDREG可以

be accessed from the OCD emulator in these modes. Table 2.14 shows the restrictions.

Table 2.14 Constraints by mode

Active mode	Start OCD emulator connection	Change low power mode	Access AHB-AP and system bus	Access APB-AP and OCDREG
Normal	Yes	Yes	Yes	Yes
Sleep	Yes	Yes	Yes	Yes
Software Standby	No	Yes	No	Yes
Snooze	No	Yes	No	Yes
Deep Software Standby	No	Yes	No	Yes

If system bus access is required in Software Standby, Snooze, or Deep Software Standby mode, set the OCUCTRL.DBIRG bit in OCDREG to wake the MCU from the low power modes. Simultaneously, using the OCUCTRL.EDBGRQ bit in OCDREG, the OCD emulator can wake the MCU without starting CPU execution by using a CPU break.

2.11.3.3 Modifying the unlock ID code in OSIS

After changing the Unlock ID code in the OSIS, the OCD emulator must reset the MCU by asserting the RES pin or setting the SYSRESETREQ bit of the Application Interrupt and Reset Control Register in the system control block to 1. The changed Unlock ID code is reflected after reset.

2.11.3.4 Connecting Sequence and JTAG/SWD Authentication

Because the OCD emulator is protected by the JTAG/SWD authentication mechanism, the OCD might be required to input the ID code to the authentication registers. The OSIS value in the option-setting memory determines whether the code is required.

After the negation of reset, a 5 µs wait time is required before comparing the OSIS value at the time of cold start.

(1) When MSB of OSIS is 0 (bit [127] = 0)

The ID code is always mismatching and connection to the OCD is prohibited.

(2) When OSIS is all 1s (default)

OCD authentication is not required and the OCD can use the AHB-AP without authentication.

1. Connect the OCD emulator to the MCU through the JTAG or SWD interface.
2. Set up SWJ-DP to access the DAP bus. In the setup, the OCD emulator must assert CDBGPWRUPREQ in the SWJ-DP Control Status Register, then wait until CSDBGPWRUPACK in the same register is asserted.
3. Set up the AHB-AP to access the system address space. The AHB-AP is connected to DAP bus port 0.
4. Start accessing the CPU debug resources using the AHB-AP.

(3) When OSIS[127:126] = 2’b10

OCD authentication is required and the OCD must write the unlock ID code to IAUTH registers 0 to 3 in the OCDREG before using the AHB-AP.

1. Connect the OCD debugger to the MCU through the JTAG or SWD interface.
2. Set up SWJ-DP to access the DAP bus. In the setup, the OCD emulator must assert CDBGPWRUPREQ in the SWJ-DP Control Status Register, and then wait until CSDBGPWRUPACK in the same register is asserted.
3. Set up the APB-AP to access OCDREG. The APB-AP is connected to the DAP bus port 1.
4. Write the 128-bit ID code to IAUTH registers 0 to 3 in the OCDREG using the APB-AP.
5. If the 128-bit ID code matches the OSIS value, the AHB-AP is authorized to issue an AHB transaction. The authorization result can be confirmed in the AUTH bit in the MCUSTAT Register or the DbgStatus bit in the AHB-AP Control Status Word Register.

在这些模式下可以从OCD仿真器访问。表2.14显示了这些限制。

Table 2.14 模式约束

主动模式	启动强迫症模拟器连接	更改低功耗模式	访问AHB-AP和系统总线	访问APB-AP和OCDREG
Normal	Yes	Yes	Yes	Yes
Sleep	Yes	Yes	Yes	Yes
软件待机	No	Yes	No	Yes
Snooze	No	Yes	No	Yes
深度软件待机	No	Yes	No	Yes

如果在软件待机、贪睡或深度软件待机模式下需要系统总线访问，请将OCDREG中的OCUCTRL.DBIRG位将MCU从低功耗模式唤醒。同时，使用OCDREG中的OCUCTRL.EDBGRQ位，OCD仿真器可以使用CPU中断唤醒MCU而无需启动CPU执行。

2.11.3.3 修改OSIS中的解锁ID码

更改OSIS中的解锁ID代码后，OCD仿真器必须通过置位RES引脚或将系统控制块中的应用程序中断和复位控制寄存器的SYSRESETREQ位设置为1来复位MCU。更改的解锁ID代码会反映复位后。

2.11.3.4 连接序列和JTAGSWD验证

由于OCD仿真器受JTAGSWD身份验证机制的保护，因此可能需要OCD将ID代码输入到身份验证寄存器中。选项设置内存中的OSIS值决定是否需要该代码。

复位否定后，在冷启动时比较OSIS值之前需要5µs的等待时间。

(1) 当OSIS的MSB为0时（位[127]=0）

ID代码总是不匹配，并且禁止连接到OCD。

(2) 当OSIS全为1时（默认）

不需要OCD身份验证，OCD无需身份验证即可使用AHB-AP。

1. 通过JTAG或SWD接口将OCD仿真器连接到MCU。
2. 设置SWJ-DP以访问DAP总线。在设置中，OCD仿真器必须在SWJ中断言CDBGPWRUPREQ DP控制状态寄存器，然后等到同一寄存器中的CSDBGPWRUPACK置位。
3. 设置AHB-AP以访问系统地址空间。AHB-AP连接到DAP总线端口0。
4. 开始使用AHB-AP访问CPU调试资源。

(3) When OSIS[127:126] = 2’b10

需要OCD身份验证，并且OCD必须在使用AHB-AP之前将解锁ID代码写入OCDREG中的IAUTH寄存器0到3。

1. 通过JTAG或SWD接口将OCD调试器连接到MCU。
2. 设置SWJ-DP以访问DAP总线。在设置中，OCD仿真器必须在SWJ中断言CDBGPWRUPREQ DP控制状态寄存器，然后等待同一寄存器中的CSDBGPWRUPACK置位。
3. 设置APB-AP以访问OCDREG。APB-AP连接到DAP总线端口1。
4. 使用APB-AP将128位ID代码写入OCDREG中的IAUTH寄存器0到3。
5. 如果128位ID代码与OSIS值匹配，则授权AHB-AP发出AHB事务。授权结果可以通过MCUSTAT寄存器中的AUTH位或AHBAP控制状态字寄存器中的DbgStatus位来确认。

- When the DbgStatus bit is 1, the 128-bit ID code is a match with the OSIS value. AHB transfers are permitted.
- When the DbgStatus bit is 0, the 128-bit ID code is not a match with the OSIS value. AHB transfers are not permitted.

6. Set up the AHB-AP to access the system address space. The AHB-AP is connected to DAP bus port 0.
7. Start accessing the CPU debug resources using the AHB-AP.

(4) When OSIS[127:126] = 2’b11

OCD authentication is required and the OCD must write the unlock ID code to IAUTH registers 0 to 3 in OCDREG. The connection sequence is the same when OSIS[127:126] is 2’b10 except for “ALeRASE” capability. When IATUH0-3 are “ALeRASE” in ASCII code, the contents of the code flash, data flash, and configuration area are erased at once. See section 55, Flash Memory for details.

ALeRASE sequence:

1. Connect the OCD debugger to the MCU through the JTAG or SWD interface.
2. Set up SWJ-DP to access DAP bus. In the setup, the OCD emulator must assert CDBGPWRUPREQ in the SWJDP Control Status Register, and then wait until CSDBGPWRUPACK in the same register is asserted.
3. Set the APB-AP to access OCDREG. This APB-AP is connected to DAP bus port 1.
4. Write the 128-bit ID code to IAUTH registers 0 to 3 in the OCDREG using the APB-AP.
5. If the 128-bit ID code is “ALeRASE” in ASCII code (414C_6552_4153_45FF_FFFF_FFFF_FFFF_FFFFh), the contents of code flash, data flash, and configuration area are erased. After that, the MCU transitions to Sleep mode.

2.12 References

1. *ARM® v7-M Architecture Reference Manual* (ARM DDI 0403D)
2. *ARM® Cortex®-M4 Processor Technical Reference Manual* (ARM DDI 0439D)
3. *ARM® Cortex®-M4 Devices Generic User Guide* (ARM DUI 0553A)
4. *ARM® CoreSight™ SoC-400 Technical Reference Manual* (ARM DDI 0480F)
5. *ARM® CoreSight™ ETM-M4 Technical Reference Manual* (ARM DDI 0440C)
6. *ARM® CoreSight™ Trace Memory Controller Technical Reference Manual* (ARM DDI 0461B)
7. *ARM® CoreSight™ Architecture Specification* (ARM IHI 0029D).

- 当DbgStatus位为1时，128位ID码与OSIS值匹配。允许AHB转移。
- 当DbgStatus位为0时，128位ID代码与OSIS值不匹配。不允许AHB转移。

6. 设置AHB-AP以访问系统地址空间。AHB-AP连接到DAP总线端口0。
7. 开始使用AHB-AP访问CPU调试资源。

(4) When OSIS[127:126] = 2’b11

需要OCD身份验证，并且OCD必须将解锁ID代码写入OCDREG中的IAUTH寄存器0到3。当OSIS[127:126]为2'b10时，连接顺序相同，但“ALeRASE”功能除外。当IATUH0-3在ASCII码中为“ALeRASE”时，代码闪存、数据闪存和配置区的内容会被一次性擦除。有关详细信息，请参见第55节，闪存。

ALeRASE sequence:

1. 通过JTAG或SWD接口将OCD调试器连接到MCU。
2. 设置SWJ-DP以访问DAP总线。在设置中，OCD仿真器必须在SWJDP中断言CDBGPWRUPREQ控制状态寄存器，然后等待同一寄存器中的CSDBGPWRUPACK被断言。
3. 设置APB-AP以访问OCDREG。此APB-AP连接到DAP总线端口1。
4. 使用APB-AP将128位ID代码写入OCDREG中的IAUTH寄存器0到3。
5. 如果128位ID代码是ASCII代码中的“ALeRASE”（414C_6552_4153_45FF_FFFF_FFFF_FFFF_FFFFh），则代码闪存、数据闪存和配置区域的内容将被擦除。之后，MCU转换到休眠模式。

2.12 References

1. ARM®v7-M架构参考手册(ARMDDI0403D)
2. ARM®Cortex®-M4处理器技术参考手册(ARMDDI0439D)
3. ARM®Cortex®-M4设备通用用户指南(ARMDUI0553A)
4. ARM®CoreSight SoC-400技术参考手册(ARMDDI0480F)
5. ARM®CoreSight ETM-M4技术参考手册(ARMDDI0440C)
6. ARM®CoreSight 跟踪内存控制器技术参考手册(ARMDDI0461B)
7. ARM®CoreSight 架构规范(ARMIHI0029D)。

3. Operating Modes

3.1 Overview

Table 3.1 shows the selection of operating modes by the mode-setting pin. For details, see section 3.2, Details of Operating Modes. Operation starts with the on-chip flash memory enabled, regardless of the mode in which operation started.

Table 3.1 Selection of operating modes by the mode-setting pin

Mode-setting pin			
MD	Operating mode	On-chip flash memory	External bus
1	Single-chip mode	Enable	Disable
0	SCI/USB boot mode	Enable	Disable

3.2 Details of Operating Modes

3.2.1 Single-Chip Mode

In single-chip mode, all I/O pins are available for use as input or output port, inputs or outputs for peripheral functions, or as interrupt inputs. When a reset is released while the MD pin is high, the MCU starts in single-chip mode and the on-chip flash is enabled.

3.2.2 SCI Boot Mode

In this mode, the on-chip flash memory programming routine (SCI boot program), stored in a dedicated area within the MCU, is used. The on-chip flash, including code flash memory and data flash memory, can be modified from outside the MCU by using a universal asynchronous receiver/transmitter (UART) SCI. For details, see section 55, Flash Memory. The MCU starts in SCI boot mode if the MD pin is held low on release from the reset state.

3.2.3 USB Boot Mode

In this mode, the on-chip flash memory programming routine (USB boot program), stored in the boot area within the MCU, is used. The on-chip flash, including code flash memory and data flash memory, can be modified from outside the MCU by using USB. For details, see section 55, Flash Memory. The chip starts in USB boot mode if the MD pin is held low on release from the reset state.

3.3 Operating Mode Transitions

3.3.1 Operating Mode Transitions as Determined by the Mode-Setting Pin

Figure 3.1 shows operating mode transitions determined by the settings of the MD pin.

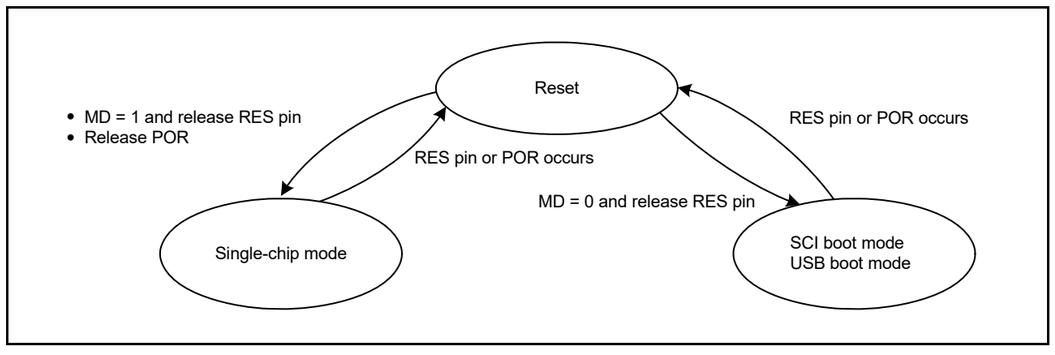


Figure 3.1 Mode-setting pin level and operating mode

3. 操作模式

3.1 Overview

表3.1显示了通过模式设置引脚选择的工作模式。有关详细信息，请参阅第3.2节，详细信息
操作模式。无论操作以何种模式开始，操作都会从启用片上闪存开始。

Table 3.1 通过模式设置引脚选择工作模式

Mode-setting pin			
MD	操作模式	片上闪存	外部总线
1	Single-chip mode	Enable	Disable
0	SCIUSB启动模式	Enable	Disable

3.2 操作模式的详细信息

3.2.1 Single-Chip Mode

在单片机模式下，所有IO引脚都可用作输入或输出端口、外围功能的输入或输出，或用作中断输入。当MD引脚为高电平时释放复位时，MCU以单芯片模式启动，并启用片上闪存。

3.2.2 SCI启动模式

在这种模式下，使用存储在MCU内的专用区域中的片上闪存编程例程（SCI引导程序）。片上闪存，包括代码闪存和数据闪存，可以从外部修改
MCU通过使用通用异步接收发送器(UART)SCI。有关详细信息，请参阅第55节，闪存。
如果MD引脚在从复位状态释放时保持低电平，则MCU以SCI启动模式启动。

3.2.3 USB启动模式

在这种模式下，片上闪存编程例程（USB引导程序），存储在引导区域内
单片机，使用。片上闪存，包括代码闪存和数据闪存，可以通过USB从MCU外部进行修改。有关详细信息，请参阅第55节，闪存。如果MD引脚在从复位状态释放时保持低电平，则芯片以USB启动模式启动。

3.3 操作模式转换

3.3.1 由模式设置引脚确定的操作模式转换

图3.1显示了由MD引脚的设置决定的操作模式转换。

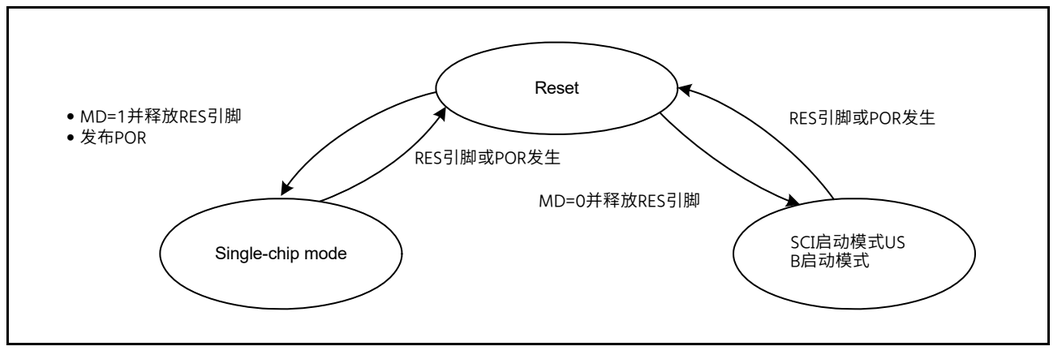
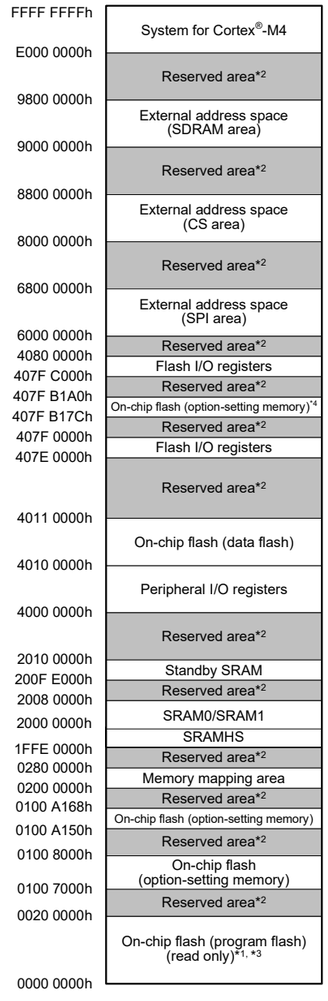


Figure 3.1 模式设置引脚电平和操作模式

4. Address Space

4.1 Address Space

The MCU supports a 4-GB linear address space ranging from 0000 0000h to FFFF FFFFh that can contain both program and data. Figure 4.1 shows the memory map.



Note 1. The capacity of the flash differs depending on the product.

Code flash memory capacity	Address	Data flash memory capacity	Address	RAM capacity	Address
2 Mbytes	0000 0000h - 001F FFFFh	64 Kbytes	4010 0000h - 4010 FFFFh	640 Kbyte	1FFE 0000h - 2007 FFFFh
1 Mbytes	0000 0000h - 000F FFFFh				

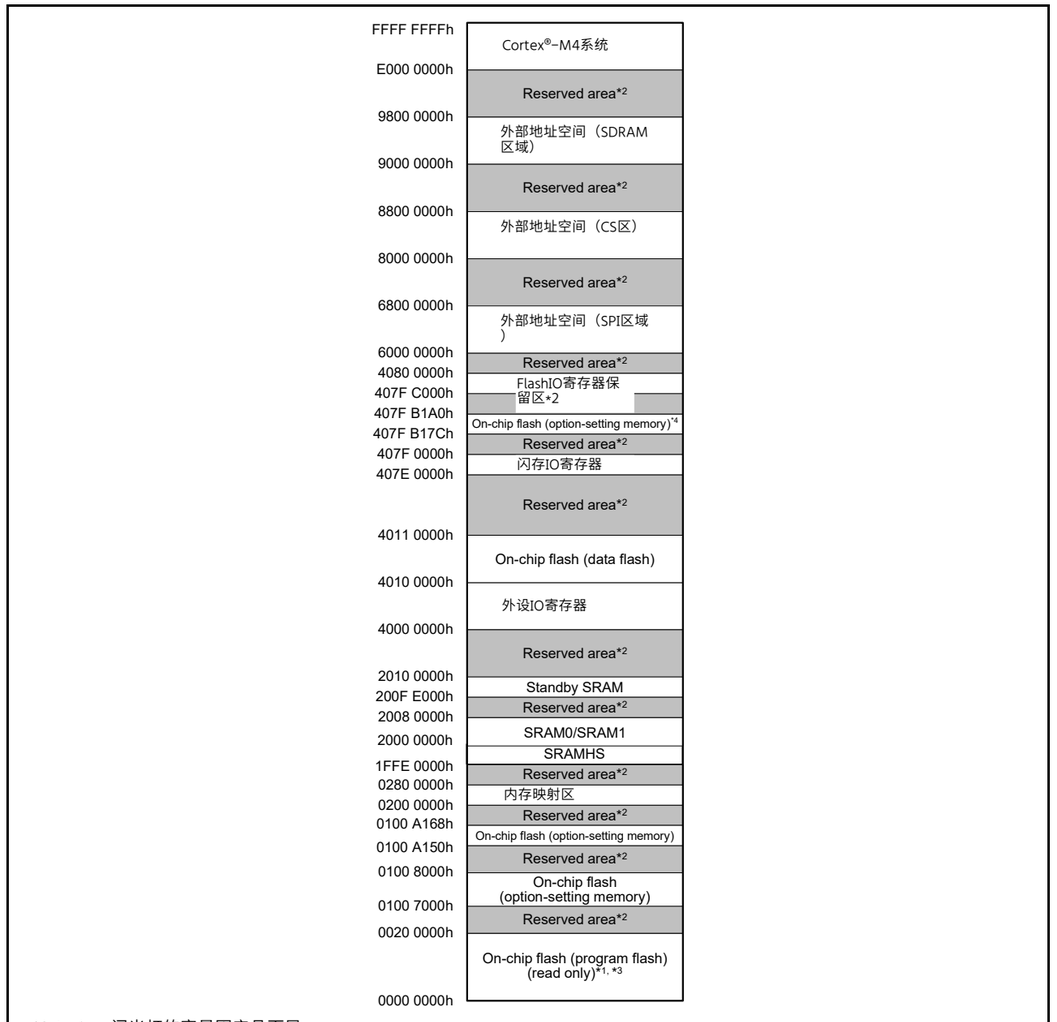
Note 2. Do not access reserved areas.
Note 3. Some regions are reserved for the option-setting memory. For details, see section 7, Option-Setting Memory.
Note 4. Do not access from 407F B180h to 407F B19Bh.

Figure 4.1 Memory map

4. 地址空间

4.1 地址空间

MCU支持4-GB线性地址空间，范围从00000000h到FFFFFFFFh，可以同时包含程序和数据。图4.1显示了内存映射。



Note 1. 闪光灯的容量因产品而异。

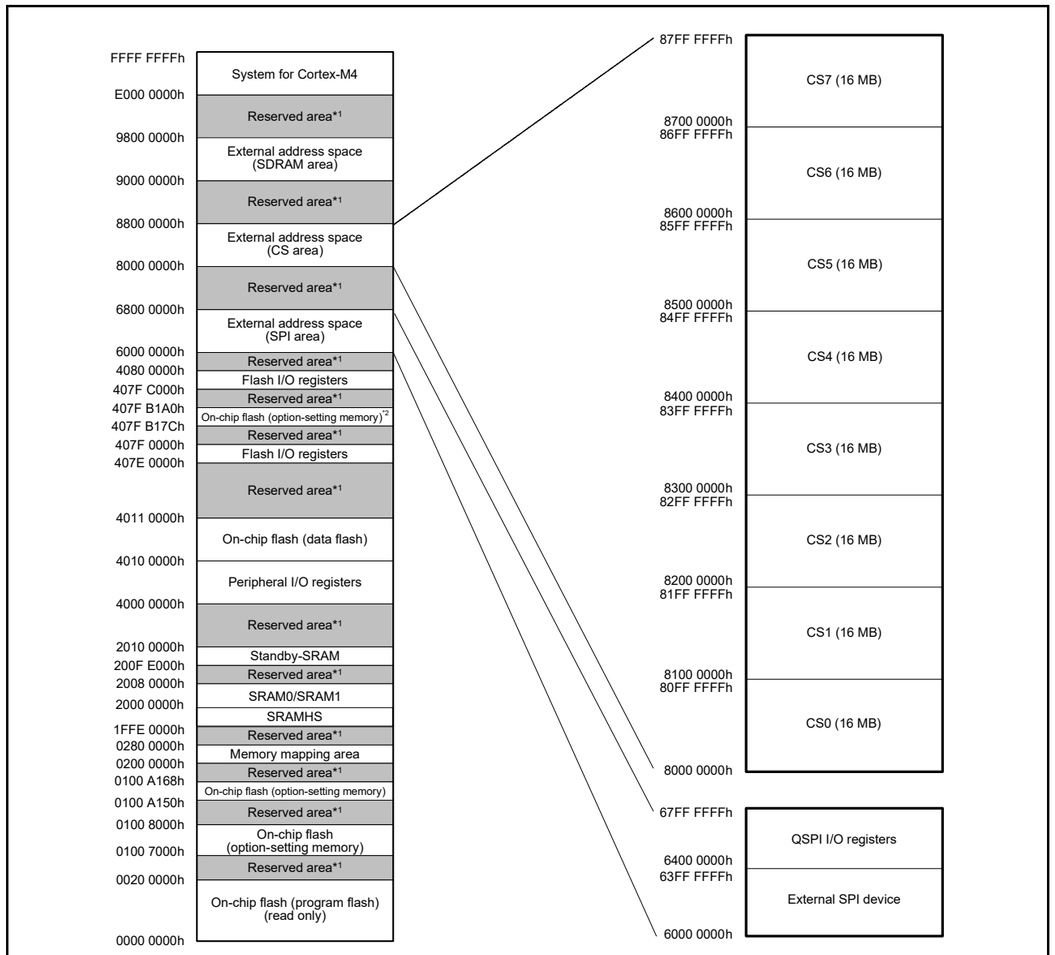
代码闪存容量	Address	数据闪存容量	Address	内存容量	Address
2 Mbytes	0000 0000h - 001F FFFFh	64 Kbytes	4010 0000h - 4010 FFFFh	640 Kbyte	1FFE 0000h - 2007 FFFFh
1 Mbytes	0000 0000h - 000F FFFFh				

Note 2. 不要进入保留区域。
Note 3. 某些区域是为选项设置内存保留的。有关详细信息，请参阅第7节，选项设置内存。
Note 4. 请勿从407FB180h访问407FB19Bh。

Figure 4.1 内存映射

4.2 External Address Space

The external address space is divided into CS areas (CS0 to CS7), SDRAM area (SDCS), and SPI area. The eight CS areas (CS0 to CS7) each correspond to the CSn signal output from a CSn (n = 0 to 7) pin. The SPI area is divided into two areas, QSPI I/O registers and external SPI device space. Figure 4.2 shows the address ranges corresponding to the individual CS areas (CS0 to CS7), SDRAM area (SDCS) and SPI area.

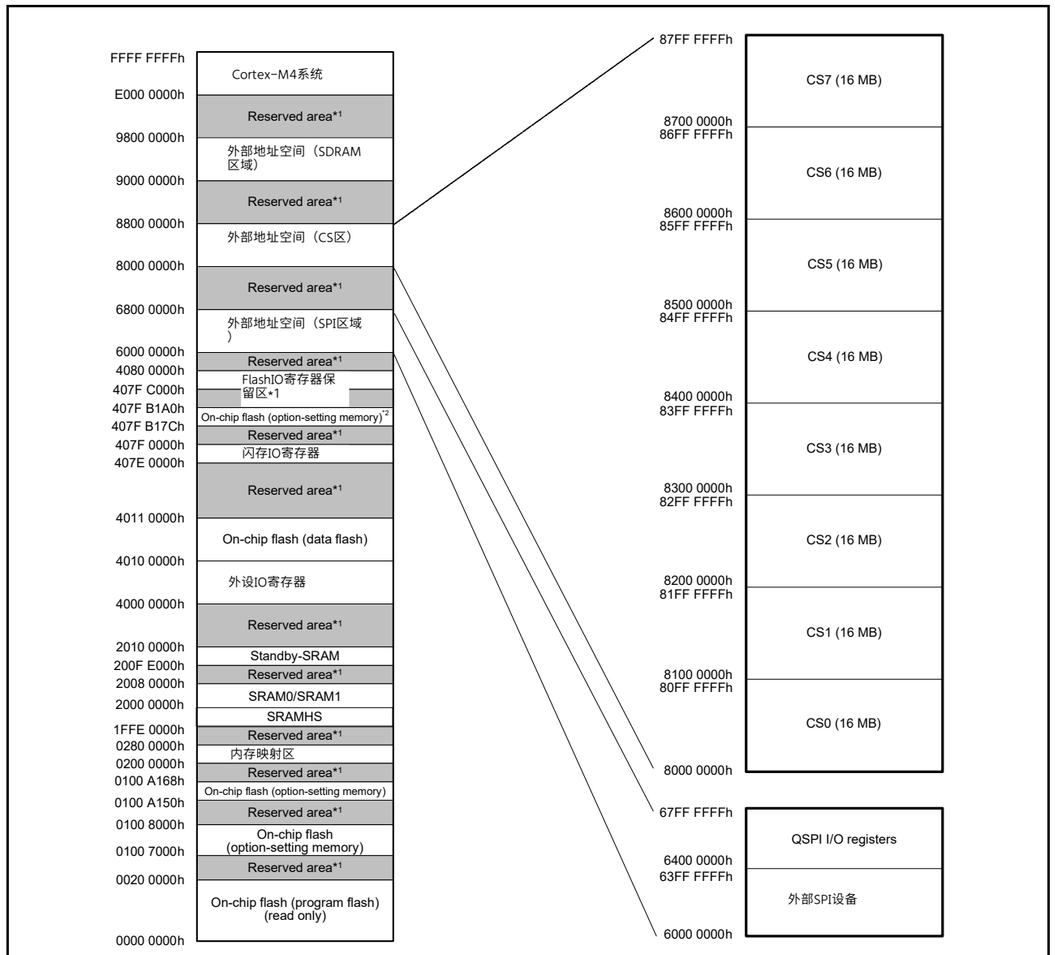


Note 1. Do not access reserved areas.
Note 2. Do not access from 407F B180h to 407F B19Bh.

Figure 4.2 Association between external address spaces and CS areas

4.2 外部地址空间

外部地址空间分为CS区（CS0到CS7）、SDRAM区（SDCS）和SPI区。8个CS区域（CS0至CS7）分别对应于从CSn（n=0至7）引脚输出的CSn信号。SPI区域分为两个区域，QSPIIO寄存器和外部SPI设备空间。图4.2显示了对应于各个CS区域（CS0至CS7）、SDRAM区域（SDCS）和SPI区域的地址范围。



Note 1. 不要进入保留区域。
Note 2. 请勿从407FB180h访问407FB19Bh。

Figure 4.2 外部地址空间与CS区域之间的关联

5. Memory Mirror Function (MMF)

5.1 Overview

The MCU provides a Memory Mirror Function (MMF). You can configure the MMF to map an application image load address in the code flash memory to the application image link address in the unused 23-bit memory mirror space addresses. Your application code must be developed and linked to run from this MMF destination address. The code is not required to know the load location where it is stored in the code flash memory.

Table 5.1 lists the MMF specifications.

Table 5.1 MMF specifications

Parameter	Specifications
Memory mirror space	8 MB (0200 0000h to 027F FFFFh)
Memory mirror boundary	128 bytes

5.2 Register Descriptions

5.2.1 MemMirror Special Function Register (MMSFR)

Address(es): MMF.MMSFR 4000 1000h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	KEY[7:0]								—	MEMMIRADDR[15:9]						
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MEMMIRADDR[8:0]									—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Symbol	Bit name	Description	R/W
b6 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b22 to b7	MEMMIRADDR[15:0]	Memory Mirror Address	0000h to FFFFh (8 MB)	R/W
b23	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b31 to b24	KEY[7:0]	MMSFR Key Code	These bits enable or disable rewriting of the MEMMIRADDR bits	R/W

MEMMIRADDR[15:0] bits (Memory Mirror Address)

The MEMMIRADDR bits specify bits [22:7] of the memory mirror address. They define where the start address of the memory mirror space addresses (0200 0000h) is linked to. Writing to these bits is enabled only when this register is accessed in 32-bit words and DBh is written to the KEY[7:0] bits.

KEY[7:0] bits (MMSFR Key Code)

The KEY[7:0] bits enable or disable rewriting of the MEMMIRADDR bits. Data written to the KEY bits is not saved. These bits are read as 0. The KEY code and MEMMIRADDR must be written to in the same cycle.

5. 内存镜像功能(MMF)

5.1 Overview

MCU提供内存镜像功能(MMF)。您可以配置MMF以将代码闪存中的应用程序映像加载地址映射到未使用的23位内存镜像空间地址中的应用程序映像链接地址。您的应用程序代码必须经过开发和链接才能从此MMF目标地址运行。代码不需要知道它存储在代码闪存中的加载位置。

表5.1列出了MMF规范。

Table 5.1 MMF specifications

Parameter	Specifications
内存镜像空间	8 MB (0200 0000h to 027F FFFFh)
内存镜像边界	128 bytes

5.2 注册说明

5.2.1 MemMirror特殊功能寄存器(MMSFR)

Address(es): MMF.MMSFR 4000 1000h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	KEY[7:0]								—	MEMMIRADDR[15:9]						
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MEMMIRADDR[8:0]									—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Symbol	位名称	Description	R/W
b6 to b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b22 to b7	MEMMIRADDR[15:0]	内存镜像地址	0000h to FFFFh (8 MB)	R/W
b23	—	Reserved	该位读取为0。写入值应为0。	R/W
b31 to b24	KEY[7:0]	MMSFR密钥代码	这些位启用或禁用重写 MEMMIRADDR bits	R/W

MEMMIRADDR[15:0]位（内存镜像地址）

MEMMIRADDR位指定内存镜像地址的位[22:7]。它们定义了内存镜像空间地址（02000000h）的起始地址链接到哪里。仅当以32位字访问该寄存器并将DBh写入KEY[7:0]位时，才能写入这些位。

KEY[7:0]位（MMSFR密钥代码）

KEY[7:0]位启用或禁用MEMMIRADDR位的重写。不保存写入KEY位的数据。
这些位读为0。KEY代码和MEMMIRADDR必须在同一个周期内写入。

5.2.2 MemMirror Enable Register (MMEN)

Address(es): MMF.MMEN 4000 1004h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	KEY[7:0]								—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	EN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Symbol	Bit name	Description	R/W
b0	EN	Memory Mirror Function Enable	0: Disable MMF 1: Enable MMF.	R/W
b23 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b31 to b24	KEY[7:0]	MMEN Key Code	These bits enable or disable rewriting of the EN bit	R/W

EN bit (Memory Mirror Function Enable)

Writing to the EN bit is enabled only when the MemMirror Enable Register is accessed in 32-bit words and DBh is written to the KEY[7:0] bits.

KEY[7:0] bits (MMEN Key Code)

The KEY[7:0] bits enable or disable rewriting of the EN bit. Data written to the KEY[7:0] bits is not saved. These bits are read as 0. The KEY code and EN must be written to in the same cycle.

5.3 Operation

5.3.1 MMF Operation

The MMF links the memory mirror space (0200 0000h to 027F FFFFh) to the code flash area. If MMEN.EN = 1, the CPU can access code flash using both normal addresses (starting at 0000 0000h) and memory mirror space addresses (starting at 0200 0000h). Figure 5.1 shows an overview of the MMF. MMSFR.MEMMIRADDR specifies where the start address of the memory mirror space addresses (0200 0000h) is linked to. Figure 5.2, Figure 5.3, and Figure 5.4 show the MMF operation. Figure 5.5 shows the setting procedure of the MMF.

5.2.2 MemMirror启用寄存器(MMEN)

Address(es): MMF.MMEN 4000 1004h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	KEY[7:0]								—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	EN
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Symbol	位名称	Description	R/W
b0	EN	内存镜像功能 Enable	0：禁用MMF1 ：启用MMF。	R/W
b23 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b31 to b24	KEY[7:0]	MMEN键码	这些位启用或禁用EN位的重写	R/W

EN位（内存镜像功能使能）

仅当以32位字访问MemMirror启用寄存器并将DBh写入KEY[7:0]位时，才启用写入EN位。

KEY[7:0]位（MMEN键码）

KEY[7:0]位启用或禁用EN位的重写。写入KEY[7:0]位的数据不保存。这些位读为0。KEY代码和EN必须在同一个周期内写入。

5.3 Operation

5.3.1 MMF Operation

MMF将内存镜像空间（02000000h到027FFFFFh）链接到代码闪存区域。如果MMEN.EN=1，CPU可以使用普通地址（从00000000h开始）和内存镜像空间地址（从02000000h开始）访问代码闪存。图5.1显示了MMF的概述。MMSFR.MEMMIRADDR指定内存镜像空间地址(02000000h)的起始地址链接到的位置。图5.2、图5.3和图5.4显示了MMF操作。图5.5显示了MMF的设置过程。

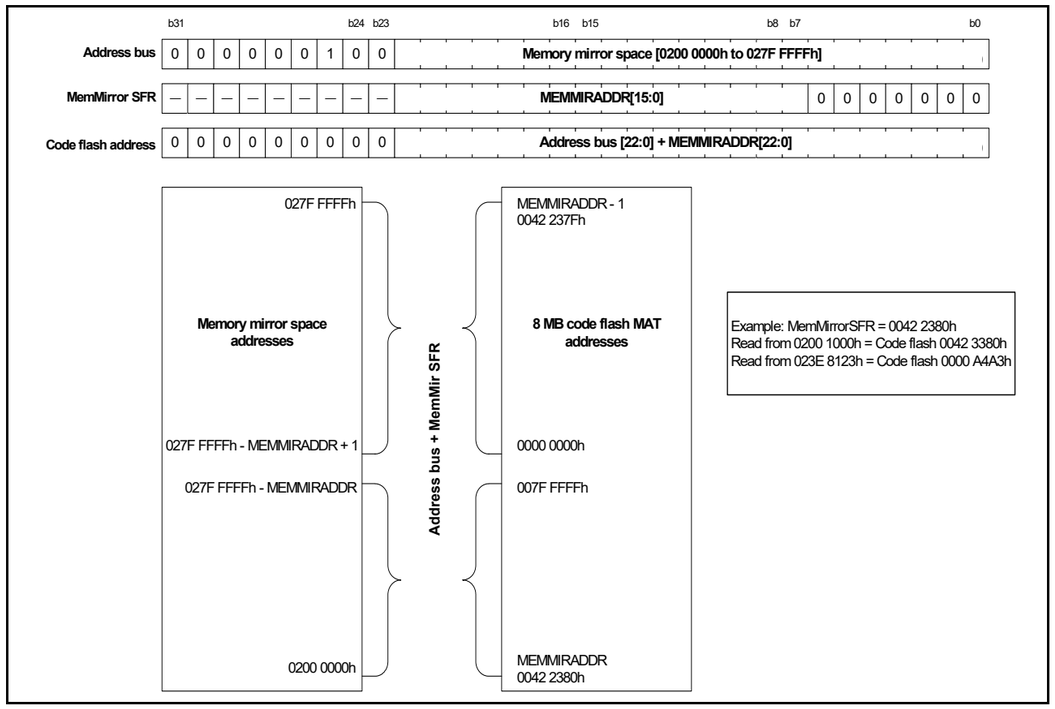


Figure 5.1 MMF operation

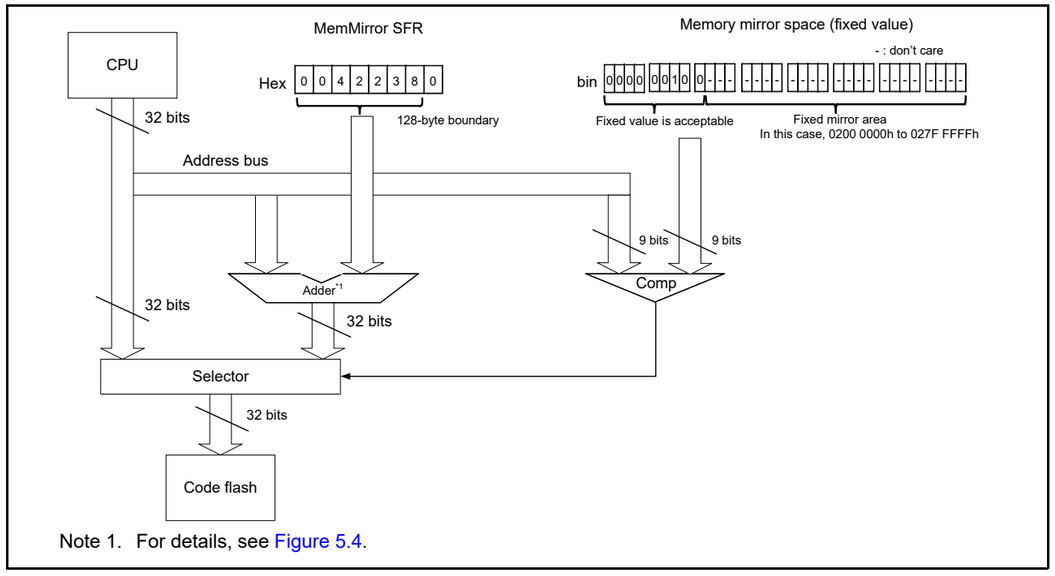


Figure 5.2 MMF block diagram

Figure 5.3 shows addresses handled by each module. The Arm® MPU uses the original address of the CPU.

The Security MPU and code flash memory each use an address after conversion through the memory mirror function.

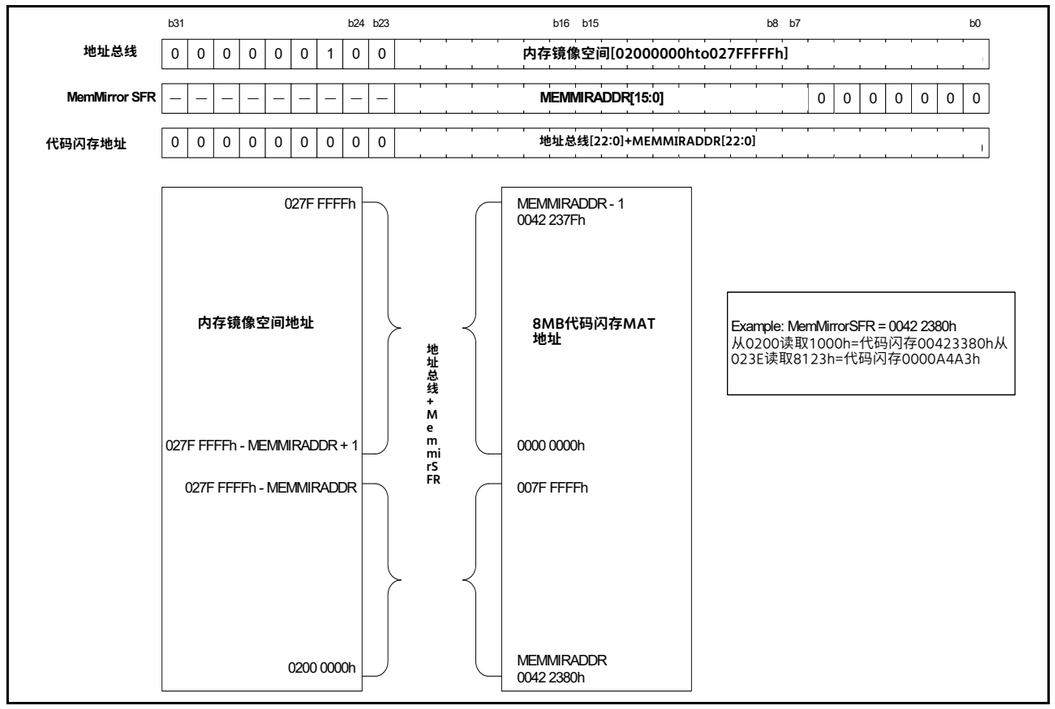


Figure 5.1 MMF operation

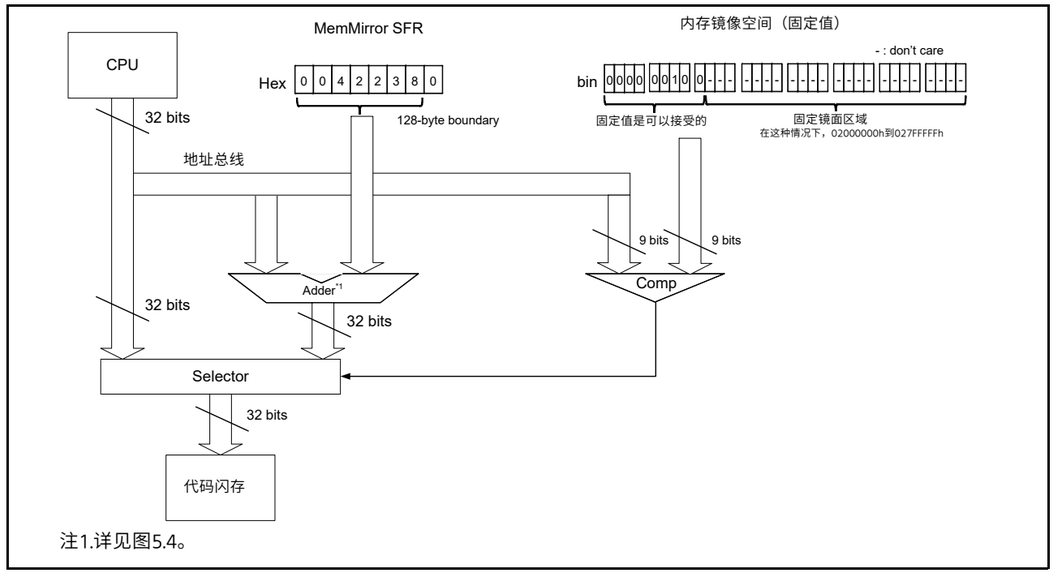


Figure 5.2 MMF框图

图5.3显示了每个模块处理的地址。Arm®MPU使用CPU的原始地址。

SecurityMPU和codeflashmemory各使用一个通过内存镜像功能转换后的地址。

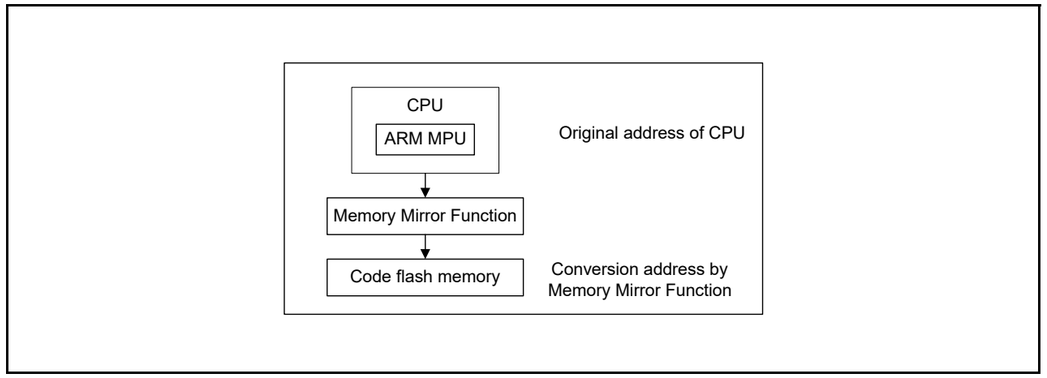


Figure 5.3 MMF address handling

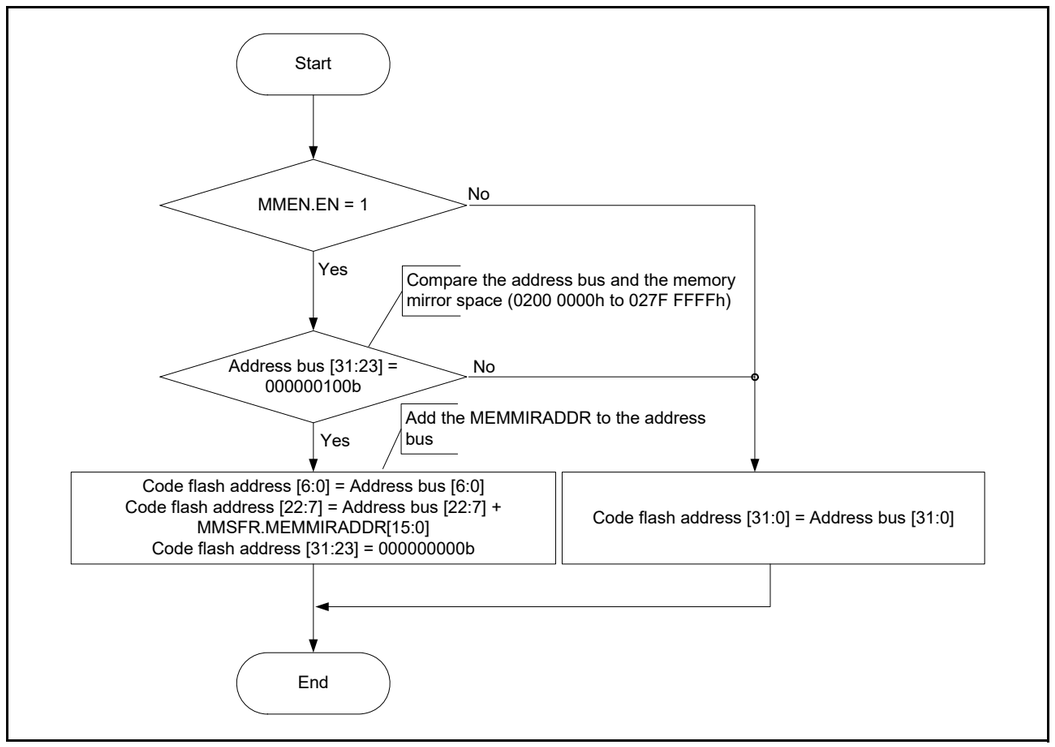


Figure 5.4 MMF operation flow

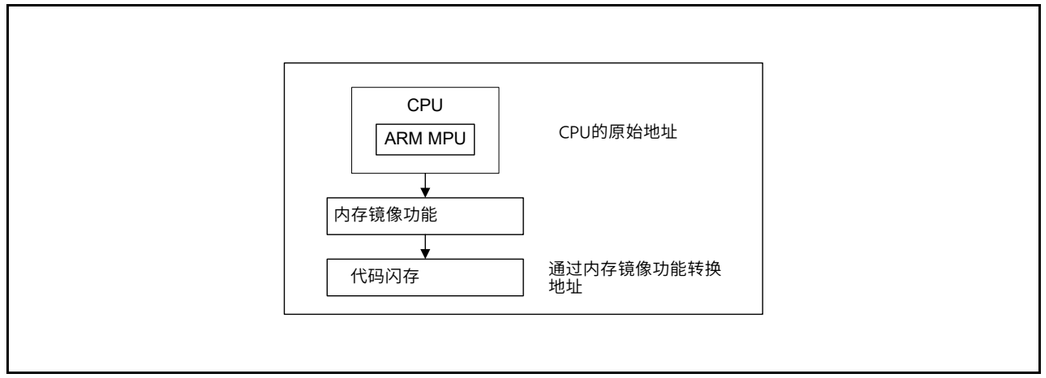


Figure 5.3 MMF地址处理

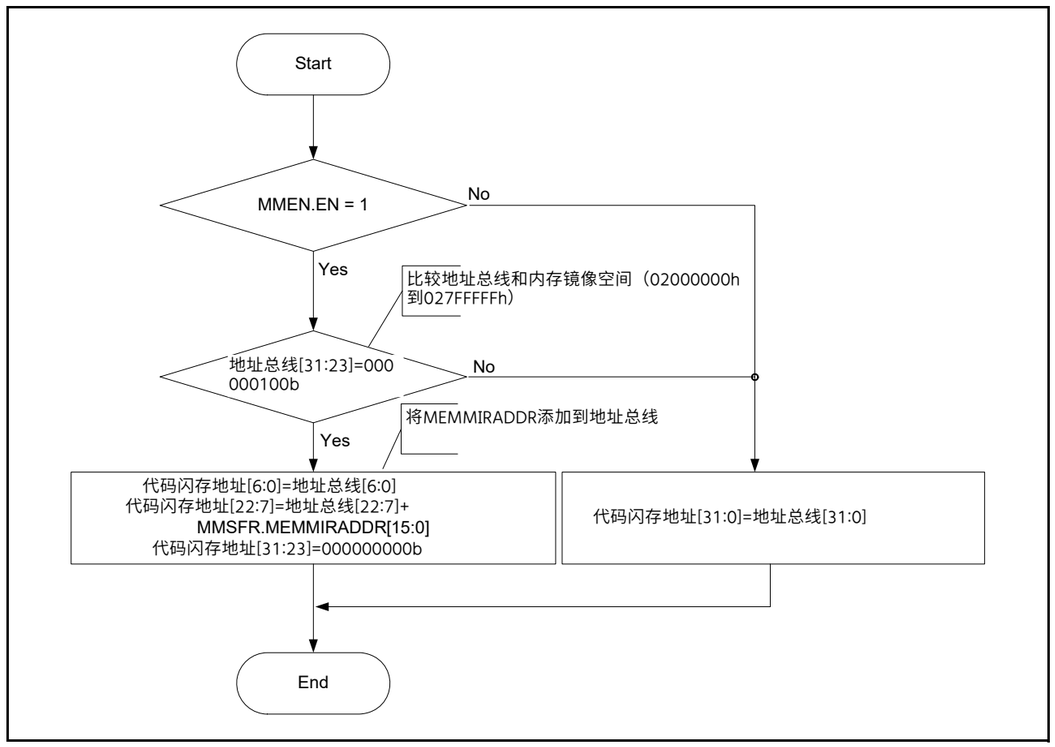


Figure 5.4 MMF操作流程

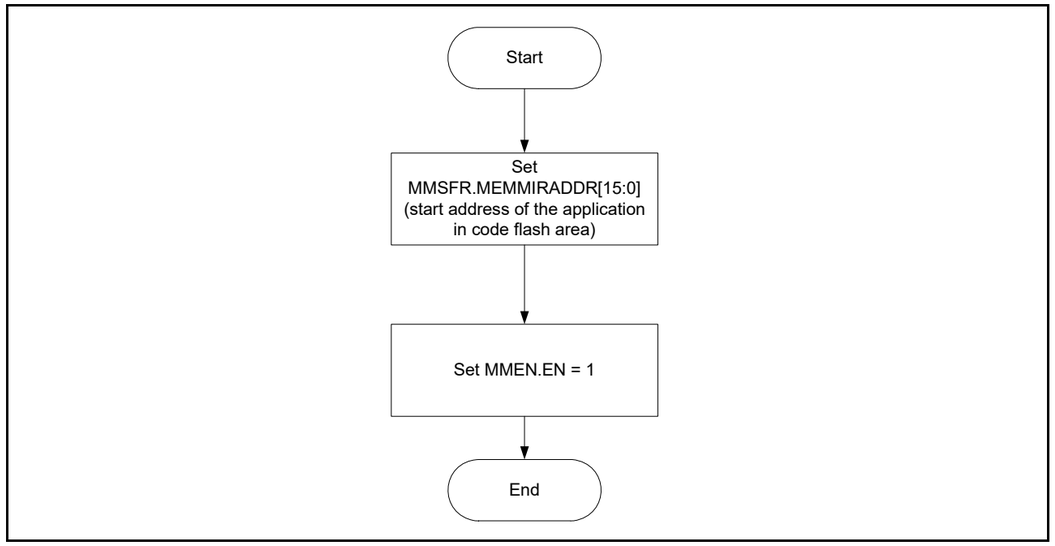


Figure 5.5 MMF setup flow

5.3.2 Setting Example

The target application code on the code flash can be accessed from address 0200 0000h on the memory mirror space by setting up the code flash start address in MMSFR.MEMMIRADDR and setting MMEN.EN = 1. Figure 5.6 shows an example of how to use the MMF.

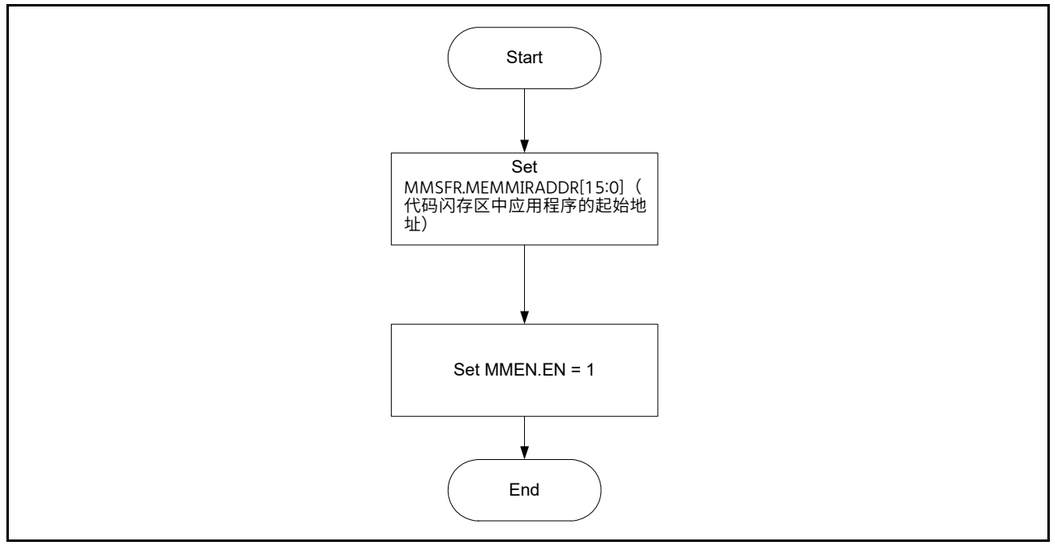


Figure 5.5 MMF设置流程

5.3.2 设置示例

通过在MMSFR.MEMMIRADDR中设置代码闪存起始地址并设置MMEN.EN=1，可以从内存镜像空间的地址0200 0000h访问代码闪存上的目标应用程序代码。图5.6显示了如何使用多发性硬化症。

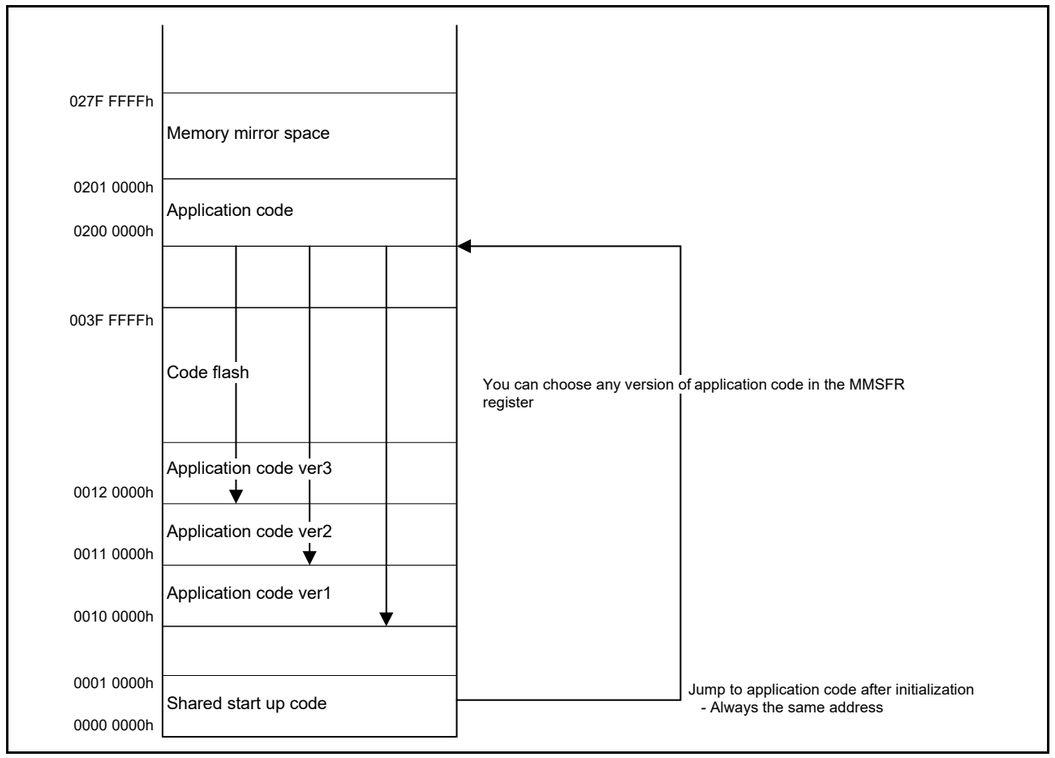


Figure 5.6 MMF setting example

- Set the MMSFR register to DB10 0000h to use the application code ver1
- Set the MMSFR register to DB11 0000h to use the application code ver2
- Set the MMSFR register to DB12 0000h to use the application code ver3.

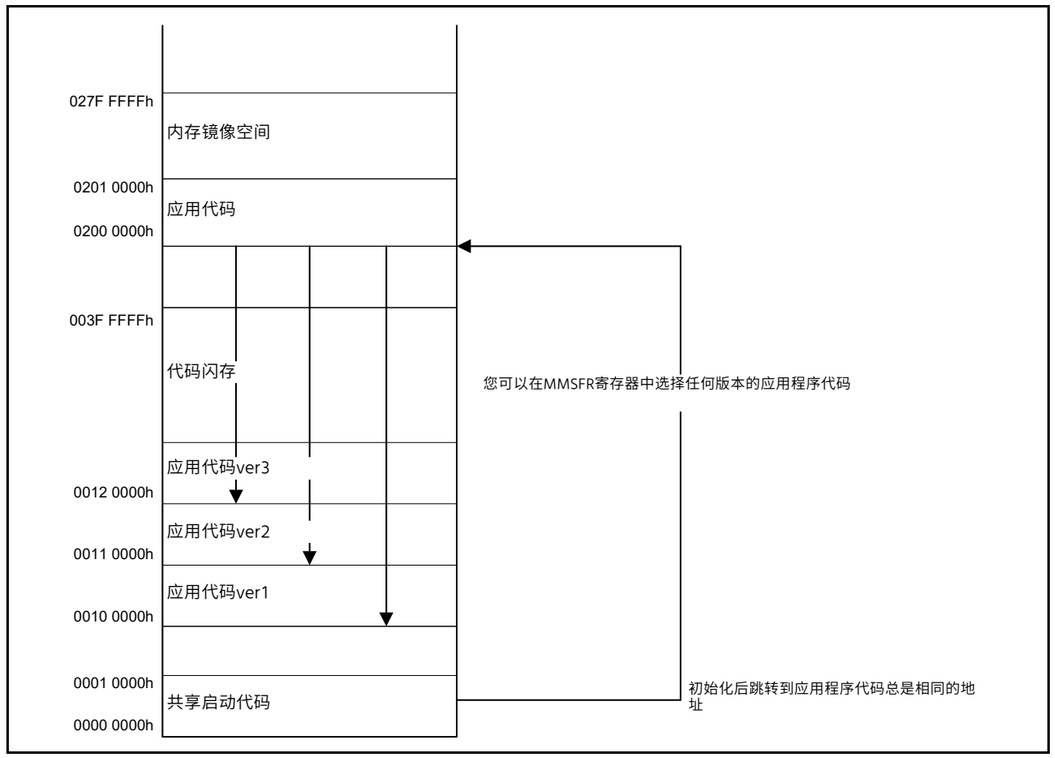


Figure 5.6 MMF设置示例

- 将MMSFR寄存器设置为DB100000h以使用应用程序代码ver1
- 将MMSFR寄存器设置为DB110000h以使用应用程序代码ver2
- 将MMSFR寄存器设置为DB120000h以使用应用程序代码ver3。

6. Resets

6.1 Overview

The MCU provides 14 resets:

- RES pin reset
- Power-on reset
- Independent watchdog timer reset
- Watchdog timer reset
- Voltage monitor 0 reset
- Voltage monitor 1 reset
- Voltage monitor 2 reset
- SRAM parity error reset
- SRAM ECC error reset
- Bus master MPU error reset
- Bus slave MPU error reset
- Stack pointer error reset
- Deep software standby reset
- Software reset.

Table 6.1 lists the reset names and sources.

Table 6.1 Reset names and sources

Reset name	Source
RES pin reset	Voltage input to the RES pin is driven low
Power-on reset	VCC rise (voltage detection V_{POR})*1
Independent watchdog timer reset	IWDT underflow or refresh error
Watchdog timer reset	WDT underflow or refresh error
Voltage monitor 0 reset	VCC fall (voltage detection V_{det0})*1
Voltage monitor 1 reset	VCC fall (voltage detection V_{det1})*1
Voltage monitor 2 reset	VCC fall (voltage detection V_{det2})*1
SRAM parity error reset	SRAM parity error detection
SRAM ECC error reset	SRAM ECC error detection
Bus master MPU error reset	Bus master MPU error detection
Bus slave MPU error reset	Bus slave MPU error detection
Stack pointer error reset	Stack pointer error detection
Deep software standby reset	Canceling of Deep Software Standby mode by an interrupt
Software reset	Register setting (use the Arm® software reset bit AIRCR.SYSRESETREQ)

Note 1. For details on the voltages to be monitored (V_{POR}, V_{det0}, V_{det1}, and V_{det2}), see section 8, Low Voltage Detection (LVD) and section 60, Electrical Characteristics.

6. Resets

6.1 Overview

MCU提供14次复位：

- RES引脚复位
- Power-on reset
- 独立看门狗定时器复位
- 看门狗定时器复位
- 电压监控器0复位
- 电压监视器1复位
- 电压监视器2复位
- SRAM奇偶校验错误复位
- SRAMECC错误复位
- 总线主控MPU错误复位
- 总线从机MPU错误复位
- 堆栈指针错误复位
- 深度软件待机复位
- 软件复位。

表6.1列出了复位名称和来源。

Table 6.1 重置名称和来源

重设名称	Source
RES引脚复位	输入到RES引脚的电压被驱动为低电平
Power-on reset	VCC上升（电压检测VPOR）*1
独立看门狗定时器复位	IWDT下溢或刷新错误
看门狗定时器复位	WDT下溢或刷新错误
电压监控器0复位	VCC下降（电压检测Vdet0）*1
电压监视器1复位	VCC下降（电压检测Vdet1）*1
电压监视器2复位	VCC下降（电压检测Vdet2）*1
SRAM奇偶校验错误复位	SRAM奇偶校验错误检测
SRAMECC错误复位	SRAMECC错误检测
总线主控MPU错误复位	总线主控MPU错误检测
总线从机MPU错误复位	总线从机MPU错误检测
堆栈指针错误复位	堆栈指针错误检测
深度软件待机复位	通过中断取消深度软件待机模式
软件复位	寄存器设置（使用Arm®软件复位位AIRCR.SYSRESETREQ）

Note 1. 有关要监控的电压（VPOR、Vdet0、Vdet1和Vdet2）的详细信息，请参见第8节，低电压检测(LVD)和第60节，电气特性。

The internal state and pins are initialized by a reset. Table 6.2 and Table 6.3 list the targets initialized by resets.

Table 6.2 Reset detect flags initialized by each reset source

Flag to be initialized	Reset source							
	RES pin reset	Power-on reset	Voltage monitor 0 reset	Independent watchdog timer reset	Watchdog timer reset	Voltage monitor 1 reset	Voltage monitor 2 reset	Software reset
Power-On Reset Detect Flag (RSTSR0.PORF)	✓	×	×	×	×	×	×	×
Voltage Monitor 0 Reset Detect Flag (RSTSR0.LVD0RF)	✓	✓	×	×	×	×	×	×
Independent Watchdog Timer Reset Detect Flag (RSTSR1.IWDTRF)	✓	✓	✓	×	×	×	×	×
Watchdog Timer Reset Detect Flag (RSTSR1.WDTRF)	✓	✓	✓	×	×	×	×	×
Voltage Monitor 1 Reset Detect Flag (RSTSR0.LVD1RF)	✓	✓	✓	×	×	×	×	×
Voltage Monitor 2 Reset Detect Flag (RSTSR0.LVD2RF)	✓	✓	✓	×	×	×	×	×
Software Reset Detect Flag (RSTSR1.SWRF)	✓	✓	✓	×	×	×	×	×
SRAM Parity Error Reset Detect Flag (RSTSR1.RPERF)	✓	✓	✓	×	×	×	×	×
SRAM ECC Error Reset Detect Flag (RSTSR1.REERF)	✓	✓	✓	×	×	×	×	×
Bus Slave MPU Error Reset Detect Flag (RSTSR1.BUSSRF)	✓	✓	✓	×	×	×	×	×
Bus Master MPU Error Reset Detect Flag (RSTSR1.BUSMRF)	✓	✓	✓	×	×	×	×	×
Stack Pointer Error Reset Detect Flag (RSTSR1.SPERF)	✓	✓	✓	×	×	×	×	×
Deep Software Standby Reset Detect Flag (RSTSR0.DPSRSTF)	✓	✓	✓	×	×	×	×	×
Cold Start/Warm Start Determination Flag (RSTSR2.CWSF)	×	✓	×	×	×	×	×	×

Flag to be initialized	Reset source						
	SRAM parity error reset	SRAM ECC error reset	Bus master MPU error reset	Bus slave MPU error reset	Stack pointer error reset	Deep Software Standby reset	
						DEEPCUT[0] = 0	DEEPCUT[0] = 1
Power-On Reset Detect Flag (RSTSR0.PORF)	×	×	×	×	×	×	×
Voltage Monitor 0 Reset Detect Flag (RSTSR0.LVD0RF)	×	×	×	×	×	×	×
Independent Watchdog Timer Reset Detect Flag (RSTSR1.IWDTRF)	×	×	×	×	×	✓	✓
Watchdog Timer Reset Detect Flag (RSTSR1.WDTRF)	×	×	×	×	×	✓	✓
Voltage Monitor 1 Reset Detect Flag (RSTSR0.LVD1RF)	×	×	×	×	×	×	×
Voltage Monitor 2 Reset Detect Flag (RSTSR0.LVD2RF)	×	×	×	×	×	×	×
Software Reset Detect Flag (RSTSR1.SWRF)	×	×	×	×	×	✓	✓
SRAM Parity Error Reset Detect Flag (RSTSR1.RPERF)	×	×	×	×	×	✓	✓
SRAM ECC Error Reset Detect Flag (RSTSR1.REERF)	×	×	×	×	×	✓	✓
Bus Slave MPU Error Reset Detect Flag (RSTSR1.BUSSRF)	×	×	×	×	×	✓	✓
Bus Master MPU Error Reset Detect Flag (RSTSR1.BUSMRF)	×	×	×	×	×	✓	✓
Stack Pointer Error Reset Detect Flag (RSTSR1.SPERF)	×	×	×	×	×	✓	✓
Deep Software Standby Reset Detect Flag (RSTSR0.DPSRSTF)	×	×	×	×	×	×	×
Cold Start/Warm Start Determination Flag (RSTSR2.CWSF)	×	×	×	×	×	×	×

✓: Initialized to 0, ×: Not initialized

内部状态和引脚由复位初始化。表6.2和表6.3列出了由复位初始化的目标。

Table 6.2 由每个复位源初始化的复位检测标志

要初始化的标志	重置源							
	RES引脚复位	Power-on reset	电压监控器0复位	独立看门狗定时器复位	看门狗定时器复位	电压监视器1复位	电压监视器2复位	软件复位
上电复位检测标志(RSTSR0.PORF)	✓	×	×	×	×	×	×	×
电压监视器0复位检测标志(RSTSR0.LVD0RF)	✓	✓	×	×	×	×	×	×
独立看门狗定时器复位检测标志(RSTSR1.IWDTRF)	✓	✓	✓	×	×	×	×	×
看门狗定时器复位检测标志(RSTSR1.WDTRF)	✓	✓	✓	×	×	×	×	×
电压监视器1复位检测标志(RSTSR0.LVD1RF)	✓	✓	✓	×	×	×	×	×
电压监视器2复位检测标志(RSTSR0.LVD2RF)	✓	✓	✓	×	×	×	×	×
软件复位检测标志(RSTSR1.SWRF)	✓	✓	✓	×	×	×	×	×
SRAM奇偶校验错误复位检测标志（RSTSR1.RPERF）	✓	✓	✓	×	×	×	×	×
SRAMECC错误复位检测标志(RSTSR1.REERF)	✓	✓	✓	×	×	×	×	×
总线从机MPU错误复位检测标志(RSTSR1.BUSSRF)	✓	✓	✓	×	×	×	×	×
总线主控MPU错误复位检测标志(RSTSR1.BUSMRF)	✓	✓	✓	×	×	×	×	×
堆栈指针错误复位检测标志(RSTSR1.SPERF)	✓	✓	✓	×	×	×	×	×
深度软件待机复位检测标志(RSTSR0.DPRSTF)	✓	✓	✓	×	×	×	×	×
冷启动热启动确定标志(RSTSR2.CWSF)	×	✓	×	×	×	×	×	×

要初始化的标志	重置源						
	SRAM奇偶校验错误复位	SRAMECC错误复位	总线主控MPU错误复位	总线从机MPU错误复位	堆栈指针错误复位	深度软件待机复位	
						DEEPCUT[0] = 0	DEEPCUT[0] = 1
上电复位检测标志(RSTSR0.PORF)	×	×	×	×	×	×	×
电压监视器0复位检测标志(RSTSR0.LVD0RF)	×	×	×	×	×	×	×
独立看门狗定时器复位检测标志(RSTSR1.IWDTRF)	×	×	×	×	×	✓	✓
看门狗定时器复位检测标志(RSTSR1.WDTRF)	×	×	×	×	×	✓	✓
电压监视器1复位检测标志(RSTSR0.LVD1RF)	×	×	×	×	×	×	×
电压监视器2复位检测标志(RSTSR0.LVD2RF)	×	×	×	×	×	×	×
软件复位检测标志(RSTSR1.SWRF)	×	×	×	×	×	✓	✓
SRAM奇偶校验错误复位检测标志（RSTSR1.RPERF）	×	×	×	×	×	✓	✓
SRAMECC错误复位检测标志(RSTSR1.REERF)	×	×	×	×	×	✓	✓
总线从机MPU错误复位检测标志(RSTSR1.BUSSRF)	×	×	×	×	×	✓	✓
总线主控MPU错误复位检测标志(RSTSR1.BUSMRF)	×	×	×	×	×	✓	✓
堆栈指针错误复位检测标志(RSTSR1.SPERF)	×	×	×	×	×	✓	✓
深度软件待机复位检测标志(RSTSR0.DPRSTF)	×	×	×	×	×	×	×
冷启动热启动确定标志(RSTSR2.CWSF)	×	×	×	×	×	×	×

：初始化为0，×：未初始化

Table 6.3 Module-related registers initialized by each reset source

Registers to be initialized		Reset source							
		RES pin reset	Power-on reset	Voltage monitor 0 reset	Independent watchdog timer reset	Watchdog timer reset	Voltage monitor 1 reset	Voltage monitor 2 reset	Software reset
Watchdog timer registers	WDTRR, WDTCR, WDTSR, WDTRCR, WDTCSTPR	✓	✓	✓	✓	✓	✓	✓	✓
Voltage monitor function 1 registers	LVD1CR0, LVCMPCR.LVD1E, LVDLVLR.LVD1LVL	✓	✓	✓	✓	✓	×	×	×
	LVD1CR1/LVD1SR	✓	✓	✓	✓	✓	×	×	×
Voltage monitor function 2 registers	LVD2CR0, LVCMPCR.LVD2E, LVDLVLR.LVD2LVL	✓	✓	✓	✓	✓	×	×	×
	LVD2CR1/LVD2SR	✓	✓	✓	✓	✓	×	×	×
SOSC register	SOSCCR	×	✓*1	×	×	×	×	×	×
	SOMCR	×	×	×	×	×	×	×	×
LOCO registers	LOCOCR	✓	✓	✓	✓	✓	✓	✓	✓
	LOCOUTCR	×	✓	✓	×	×	✓	✓	×
MOSC register	MOMCR	✓	✓	✓	✓	✓	✓	✓	✓
Realtime Clock (RTC) register*2		×	×	×	×	×	×	×	×
AGT registers		×	✓	✓	×	×	✓	✓	×
USBFS registers	Except DPUSR0R, DPUSR1R	✓	✓	✓	✓	✓	✓	✓	✓
	DPUSR0R, DPUSR1R	✓	✓	✓	✓	✓	✓	✓	✓
USBHS registers	Except DPUSR0R, DPUSR1R, DPUSR2R, DPUSRCR	✓	✓	✓	✓	✓	✓	✓	✓
	DPUSR0R, DPUSR1R, DPUSR2R, DPUSRCR	✓	✓	✓	✓	✓	✓	✓	✓
MPU register		✓	✓	✓	✓	✓	✓	✓	✓
Pin states (except XCIN/XCOUT pin)		✓	✓	✓	✓	✓	✓	✓	✓
Pin states (XCIN/XCOUT pin)		×	×	×	×	×	×	×	×
Low-power function registers	DPSBYCR, DPSIER0 to DPSIER3, DPSIFR0 to DPSIFR3, DPSIEGR0 to DPSIEGR2	✓	✓	✓	✓	✓	✓	✓	✓
Battery backup register		×	×	×	×	×	×	×	×
Registers other than those shown, CPU, and internal state		✓	✓	✓	✓	✓	✓	✓	✓

Registers to be initialized		Reset source						
		SRAM parity error reset	SRAM ECC error reset	Bus master MPU error reset	Bus slave MPU error reset	Stack pointer error reset	Deep Software Standby reset	
							DEEPCUT[0] = 0	DEEPCUT[0] = 1
Watchdog timer registers	WDTRR, WDTCR, WDTSR, WDTRCR, WDTCSTPR	✓	✓	✓	✓	✓	✓	✓
Voltage monitor function 1 registers	LVD1CR0, LVCMPCR.LVD1E, LVDLVLR.LVD1LVL	×	×	×	×	×	×	×
	LVD1CR1/LVD1SR	×	×	×	×	×	✓	✓
Voltage monitor function 2 registers	LVD2CR0, LVCMPCR.LVD2E, LVDLVLR.LVD2LVL	×	×	×	×	×	×	×
	LVD2CR1/LVD2SR	×	×	×	×	×	✓	✓
SOSC register	SOSCCR	×	×	×	×	×	×	×
	SOMCR	×	×	×	×	×	×	×
LOCO register	LOCOCR	✓	✓	✓	✓	✓	✓	✓
	LOCOUTCR	×	×	×	×	×	×	✓
MOSC registers	MOMCR	✓	✓	✓	✓	✓	×	×
Realtime Clock (RTC) register*2		×	×	×	×	×	×	×
AGT register		×	×	×	×	×	×	✓
USBFS registers	Except DPUSR0R, DPUSR1R	✓	✓	✓	✓	✓	✓	✓
	DPUSR0R, DPUSR1R	✓	✓	✓	✓	✓	×	✓
USBHS registers	Except DPUSR0R, DPUSR1R, DPUSR2R, DPUSRCR	✓	✓	✓	✓	✓	✓	✓
	DPUSR0R, DPUSR1R, DPUSR2R, DPUSRCR	✓	✓	✓	✓	✓	×	✓
MPU register		✓	✓	×	×	×	✓	✓
Pin states (except XCIN/XCOUT pin)		✓	✓	✓	✓	✓	*3	*3
Pin states (XCIN/XCOUT pin)		×	×	×	×	×	×	×

Table 6.3 每个复位源初始化的模块相关寄存器

待初始化的寄存器		重置源							
		RES引脚复位	Power-on reset	电压监控器0复位	独立看门狗定时器复位	看门狗定时器复位	电压监视器1复位	电压监视器2复位	软件复位
看门狗定时器寄存器	WDTRR, WDTCR, WDTSR, WDTRCR, WDTCSTPR	✓	✓	✓	✓	✓	✓	✓	✓
电压监控功能1个寄存器	LVD1CR0, LVCMPCR.LVD1E, LVDLVLR.LVD1LVL	✓	✓	✓	✓	✓	×	×	×
	LVD1CR1/LVD1SR	✓	✓	✓	✓	✓	×	×	×
电压监控功能2个寄存器	LVD2CR0, LVCMPCR.LVD2E, LVDLVLR.LVD2LVL	✓	✓	✓	✓	✓	×	×	×
	LVD2CR1/LVD2SR	✓	✓	✓	✓	✓	×	×	×
SOSC register	SOSCCR	×	✓*1	×	×	×	×	×	×
	SOMCR	×	×	×	×	×	×	×	×
LOCO寄存器	LOCOCR	✓	✓	✓	✓	✓	✓	✓	✓
	LOCOUTCR	×	✓	✓	×	×	✓	✓	×
MOSC register	MOMCR	✓	✓	✓	✓	✓	✓	✓	✓
实时时钟(RTC)寄存器*2		×	×	×	×	×	×	×	×
AGT registers		×	✓	✓	×	×	✓	✓	×
USBFS registers	Except DPUSR0R, DPUSR1R	✓	✓	✓	✓	✓	✓	✓	✓
	DPUSR0R, DPUSR1R	✓	✓	✓	✓	✓	✓	✓	✓
USBHS registers	Except DPUSR0R, DPUSR1R, DPUSR2R, DPUSRCR	✓	✓	✓	✓	✓	✓	✓	✓
	DPUSR0R, DPUSR1R, DPUSR2R, DPUSRCR	✓	✓	✓	✓	✓	✓	✓	✓
MPU register		✓	✓	✓	✓	✓	✓	✓	✓
引脚状态（XCINXCOUT引脚除外）		✓	✓	✓	✓	✓	✓	✓	✓
引脚状态（XCINXCOUT引脚）		×	×	×	×	×	×	×	×
低功耗功能寄存器	DPSBYCR, DPSIER0 to DPSIER3, DPSIFR0 to DPSIFR3, DPSIEGR0 to DPSIEGR2	✓	✓	✓	✓	✓	✓	✓	✓
电池备份寄存器		×	×	×	×	×	×	×	×
未显示的寄存器、CPU和内部状态		✓	✓	✓	✓	✓	✓	✓	✓

待初始化的寄存器		重置源						
		SRAM奇偶校验错误复位	SRAM ECC错误复位	总线主控MPU错误复位	总线从机MPU错误复位	堆栈指针错误复位	深度软件待机复位	
							DEEPCUT[0] = 0	DEEPCUT[0] = 1
看门狗定时器寄存器	WDTRR, WDTCR, WDTSR, WDTRCR, WDTCSTPR	✓	✓	✓	✓	✓	✓	✓
电压监控功能1个寄存器	LVD1CR0, LVCMPCR.LVD1E, LVDLVLR.LVD1LVL	×	×	×	×	×	×	×
	LVD1CR1/LVD1SR	×	×	×	×	×	✓	✓
电压监控功能2个寄存器	LVD2CR0, LVCMPCR.LVD2E, LVDLVLR.LVD2LVL	×	×	×	×	×	×	×
	LVD2CR1/LVD2SR	×	×	×	×	×	✓	✓
SOSC register	SOSCCR	×	×	×	×	×	×	×
	SOMCR	×	×	×	×	×	×	×
本地寄存器	LOCOCR	✓	✓	✓	✓	✓	✓	✓
	LOCOUTCR	×	×	×	×	×	×	✓
MOSC registers	MOMCR	✓	✓	✓	✓	✓	×	×
实时时钟(RTC)寄存器*2		×	×	×	×	×	×	×
AGT register		×	×	×	×	×	×	✓
USBFS registers	Except DPUSR0R, DPUSR1R	✓	✓	✓	✓	✓	✓	✓
	DPUSR0R, DPUSR1R	✓	✓	✓	✓	✓	×	✓
USBHS registers	Except DPUSR0R, DPUSR1R, DPUSR2R, DPUSRCR	✓	✓	✓	✓	✓	✓	✓
	DPUSR0R, DPUSR1R, DPUSR2R, DPUSRCR	✓	✓	✓	✓	✓	×	✓
MPU register		✓	✓	×	×	×	✓	✓
引脚状态（XCINXCOUT引脚除外）		✓	✓	✓	✓	✓	*3	*3
引脚状态（XCINXCOUT引脚）		×	×	×	×	×	×	×

Registers to be initialized		Reset source						
		SRAM parity error reset	SRAM ECC error reset	Bus master MPU error reset	Bus slave MPU error reset	Stack pointer error reset	Deep Software Standby reset	
							DEEPCUT[0] = 0	DEEPCUT[0] = 1
Low-power function registers	DPSBYCR, DPSIER0 to DPSIER3, DPSIFR0 to DPSIFR3, DPSIEGR0 to DPSIEGR2	✓	✓	✓	✓	✓	×	×
Battery backup register		×	×	×	×	×	×	×
Registers other than those shown, CPU, and internal state		✓	✓	✓	✓	✓	✓	✓

✓: Initialized, ×: Not initialized

Note 1. For the initial value of each register, see section 9, Clock Generation Circuit.
Note 2. The RTC has a software reset. RCR1.RTCOS, CIE and RCR2.RTCOE, ADJ30, and RESET are initialized by all types of resets. For details on the target bits, see section 26, Realtime Clock (RTC).
Note 3. Depends on the setting of DPSBYCR.IOKEEP.

The RTC is not initialized by any reset source. SOSC and LOCO can be selected as the clock source of RTC. The following are the states of SOSC and LOCO when a reset occurs.

Table 6.4 States of SOSC when a reset occurs

		Reset source	
		POR	Other
SOSC	Enable or disable	Initialized to enable	Continue with the state that was selected before the reset occurred
	Drive capability	Continue with the state that was selected before the reset occurred	

Table 6.5 States of LOCO when a reset occurs

		Reset source	
		POR, LVD0, LVD1, LVD2/ Deep Software Standby (DEEPCUT[0] = 1)	Other
LOCO	Enable or disable	Initialized to enable	
	Oscillation accuracy*1	Initialized to accuracy before trimming by LOCOUTCR (accuracy: ± 15%)	Continue with the accuracy that was trimmed by LOCOUTCR

Note 1. The LOCO User Trimming Control Register (LOCOUTCR) is reset by POR, LVD0, LVD1, LVD2, and Deep Software Standby (DEEPCUT[0] = 1) resets, returning the LOCO to the default oscillation accuracy. This can affect RTC accuracy if the RTC uses the LOCO (with a user trimming value in LOCOUTCR) as the RTC source clock. To restore the pre-reset LOCO oscillation accuracy, reload the required trimming value into LOCOUTCR after any of these resets.

Table 6.6 lists the pin related to the reset function.

Table 6.6 Reset I/O pin

Pin name	I/O	Function
RES	Input	Reset pin

待初始化的寄存器		重置源						
		SRAM奇偶校验错误复位	SRAM ECC错误复位	总线主控MPU错误复位	总线从机MPU错误复位	堆栈指针错误复位	深度软件待机复位	
							DEEPCUT[0] = 0	DEEPCUT[0] = 1
低功耗功能寄存器	DPSBYCR, DPSIER0 to DPSIER3, DPSIFR0 to DPSIFR3, DPSIEGR0 to DPSIEGR2	✓	✓	✓	✓	✓	×	×
电池备份寄存器		×	×	×	×	×	×	×
未显示的寄存器、CPU和内部状态		✓	✓	✓	✓	✓	✓	✓

：已初始化，×：未初始化

Note 1. 对于每个寄存器的初始值，请参见第9节，时钟生成电路。
Note 2. RTC具有软件复位功能。RCR1.RTCOS、CIE和RCR2.RTCOE、ADJ30和RESET由所有类型的复位初始化。有关目标位的详细信息，请参见第26节，实时时钟(RTC)。
Note 3. 取决于DPSBYCR.IOKEEP的设置。

RTC不会被任何复位源初始化。可选择SOSC和LOCO作为RTC的时钟源。以下是复位发生时SOSC和LOCO的状态。

Table 6.4 发生复位时SOSC的状态

		重置源	
		POR	Other
SOSC	启用或禁用	初始化为启用	继续使用重置发生之前选择的状态
	驱动能力	继续使用重置发生之前选择的状态	

Table 6.5 发生复位时的LOCO状态

		重置源	
		POR、LVD0、LVD1、LVD2深度软件待机（DEEPCUT[0]=1）	Other
LOCO	启用或禁用	初始化为启用	
	Oscillation accuracy*1	由LOCOUTCR微调前初始化为精度（精度：±15%）	继续使用被修剪的精度 LOCOUTCR

Note 1. LOCO用户微调控制寄存器(LOCOUTCR)通过POR、LVD0、LVD1、LVD2和深度软件待机(DEEPCUT[0]=1)复位，将LOCO返回到默认振荡精度。如果RTC使用LOCO（在LOCOUTCR中具有用户修整值）作为RTC源时钟，这可能会影响RTC精度。要恢复预复位的LOCO振荡精度，请在任何这些复位后将所需的微调值重新加载到LOCOUTCR。

表6.6列出了与复位功能相关的引脚。

Table 6.6 复位IO引脚

引脚名称	I/O	Function
RES	Input	复位引脚

6.2 Register Descriptions

6.2.1 Reset Status Register 0 (RSTSR0)

Address(es): SYSTEM.RSTSR0 4001 E410h

	b7	b6	b5	b4	b3	b2	b1	b0
	DPSRSTF	—	—	—	LVD2RF	LVD1RF	LVD0RF	PORF
Value after reset:	x*1	0	0	0	x*1	x*1	x*1	x*1

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b0	PORF	Power-On Reset Detect Flag	0: Power-on reset not detected 1: Power-on reset detected.	R(/W)*2
b1	LVD0RF	Voltage Monitor 0 Reset Detect Flag	0: Voltage monitor 0 reset not detected 1: Voltage monitor 0 reset detected.	R(/W)*2
b2	LVD1RF	Voltage Monitor 1 Reset Detect Flag	0: Voltage monitor 1 reset not detected 1: Voltage monitor 1 reset detected.	R(/W)*2
b3	LVD2RF	Voltage Monitor 2 Reset Detect Flag	0: Voltage monitor 2 reset not detected 1: Voltage monitor 2 reset detected.	R(/W)*2
b6 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	DPSRSTF	Deep Software Standby Reset Flag	0: Deep Software Standby mode cancellation not requested by an interrupt 1: Deep Software Standby mode cancellation requested by an interrupt.	R(/W)*2

Note 1. The value after reset depends on the reset source.
Note 2. Only 0 can be written, to clear the flag. The flag must be cleared by writing 0 after 1 is read.

PORF flag (Power-On Reset Detect Flag)

The PORF flag indicates that a power-on reset occurred.

[Setting condition]

- When a power-on reset occurs.

[Clearing conditions]

- When a reset listed in Table 6.2 occurs
- When 1 is read from and then 0 is written to PORF.

LVD0RF flag (Voltage Monitor 0 Reset Detect Flag)

The LVD0RF flag indicates that the VCC voltage fell below V_{det0}.

[Setting condition]

- When a voltage monitor 0 reset occurs.

[Clearing conditions]

- When a reset listed in Table 6.2 occurs
- When 1 is read from and then 0 is written to LVD0RF.

LVD1RF flag (Voltage Monitor 1 Reset Detect Flag)

The LVD1RF flag indicates that the VCC voltage fell below V_{det1}.

[Setting condition]

- When a voltage monitor 1 reset occurs.

6.2 注册说明

6.2.1 复位状态寄存器0(RSTSR0)

Address(es): SYSTEM.RSTSR0 4001 E410h

	b7	b6	b5	b4	b3	b2	b1	b0
	DPSRSTF	—	—	—	LVD2RF	LVD1RF	LVD0RF	PORF
重置后的值：	x*1	0	0	0	x*1	x*1	x*1	x*1

x: Undefined

Bit	Symbol	位名称	Description	R/W
b0	PORF	上电复位检测标志	0：未检测到上电复位1：检测到上电复位。	R(/W)*2
b1	LVD0RF	电压监视器0复位检测标志	0：未检测到电压监控器0复位1：检测到电压监控器0复位。	R(/W)*2
b2	LVD1RF	电压监视器1复位检测标志	0：未检测到电压监控器1复位1：检测到电压监控器1复位。	R(/W)*2
b3	LVD2RF	电压监视器2复位检测标志	0：未检测到电压监控器2复位1：检测到电压监控器2复位。	R(/W)*2
b6 to b4	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b7	DPSRSTF	深度软件待机复位标志	0：中断未请求深度软件待机模式取消1：中断请求深度软件待机模式取消。	R(/W)*2

Note 1. 复位后的值取决于复位源。
Note 2. 只能写入0，以清除标志。该标志必须在读取1后写入0来清除。

PORF标志（上电复位检测标志）

PORF标志表示发生了上电复位。

[Setting condition]

- 发生上电复位时。

[Clearing conditions]

- 发生表6.2中列出的复位时
- 当从PORF读取1然后将0写入PORF。

LVD0RF标志（电压监视器0复位检测标志）

LVD0RF标志表示VCC电压低于Vdet0。

[Setting condition]

- 发生电压监视器0复位时。

[Clearing conditions]

- 发生表6.2中列出的复位时
- 从LVD0RF读取1然后将0写入LVD0RF。

LVD1RF标志（电压监视器1复位检测标志）

LVD1RF标志表示VCC电压低于Vdet1。

[Setting condition]

- 当电压监视器1发生复位时。

[Clearing conditions]

- When a reset listed in Table 6.2 occurs
- When 1 is read from and then 0 is written to LVD1RF.

LVD2RF flag (Voltage Monitor 2 Reset Detect Flag)

The LVD2RF flag indicates that the VCC voltage fell below V_{det2}.

[Setting condition]

- When a voltage monitor 2 reset occurs.

[Clearing conditions]

- When a reset listed in Table 6.2 occurs
- When 1 is read from and then 0 is written to LVD2RF.

DPSRSTF flag (Deep Software Standby Reset Flag)

The DPSRSTF flag indicates that Deep Software Standby mode was canceled by an external or internal interrupt and that an internal reset (Deep Software Standby reset) occurred when an exception from Deep Software Standby mode occurred.

[Setting condition]

- When Deep Software Standby mode is canceled by an external or internal interrupt. For details, see section 11, Low Power Modes.

[Clearing conditions]

- When a reset listed in Table 6.2 occurs
- When 1 is read from and then 0 is written to DPSRSTF.

6.2.2 Reset Status Register 1 (RSTSR1)

Address(es): SYSTEM.RSTSR1 4001 E0C0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	SPERF	BUSMRF	BUSSRF	REERF	RPERF	—	—	—	—	—	SWRF	WDTRF	IWDTRF
Value after reset:	0	0	0	x*1	x*1	x*1	x*1	x*1	0	0	0	0	0	x*1	x*1	x*1

Bit	Symbol	Bit name	Description	R/W
b0	IWDTRF	Independent Watchdog Timer Reset Detect Flag	0: Independent watchdog timer reset not detected 1: Independent watchdog timer reset detected	R(/W) *2
b1	WDTRF	Watchdog Timer Reset Detect Flag	0: Watchdog Timer reset not detected 1: Watchdog Timer reset detected.	R(/W) *2
b2	SWRF	Software Reset Detect Flag	0: Software reset not detected 1: Software reset detected.	R(/W) *2
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	RPERF	SRAM Parity Error Reset Detect Flag	0: SRAM parity error reset not detected 1: SRAM parity error reset detected.	R(/W) *2
b9	REERF	SRAM ECC Error Reset Detect Flag	0: SRAM ECC error reset not detected 1: SRAM ECC error reset detected.	R(/W) *2
b10	BUSSRF	Bus Slave MPU Error Reset Detect Flag	0: Bus slave MPU error reset not detected 1: Bus slave MPU error reset detected.	R(/W) *2
b11	BUSMRF	Bus Master MPU Error Reset Detect Flag	0: Bus master MPU error reset not detected 1: Bus master MPU error reset detected.	R(/W) *2

[Clearing conditions]

- 发生表6.2中列出的复位时
- 从LVD1RF读取1然后将0写入LVD1RF。

LVD2RF标志（电压监视器2复位检测标志）

LVD2RF标志表示VCC电压低于Vdet2。

[Setting condition]

- 当电压监视器2发生复位时。

[Clearing conditions]

- 发生表6.2中列出的复位时
- 当从1读取然后0写入LVD2RF。

DPRSTF标志（深度软件待机复位标志）

DPSRSTF标志表示深度软件待机模式已被外部或内部中断取消，并且当深度软件待机模式发生异常时发生内部复位（深度软件待机复位）。

[Setting condition]

- 当深度软件待机模式被外部或内部中断取消时。有关详细信息，请参阅第11节，低电源模式。

[Clearing conditions]

- 发生表6.2中列出的复位时
- 当从1被读取，然后0被写入DPRSTF。

6.2.2 复位状态寄存器1(RSTSR1)

Address(es): SYSTEM.RSTSR1 4001 E0C0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	SPERF	BUSMRF	BUSSRF	REERF	RPERF	—	—	—	—	—	SWRF	WDTRF	IWDTRF
重置后的值：	0	0	0	x*1	x*1	x*1	x*1	x*1	0	0	0	0	0	x*1	x*1	x*1

Bit	Symbol	位名称	Description	R/W
b0	IWDTRF	独立看门狗定时器复位检测标志	0：未检测到独立看门狗定时器复位1：检测到独立看门狗定时器复位	R(/W) *2
b1	WDTRF	看门狗定时器复位检测标志	0：未检测到看门狗定时器复位1：检测到看门狗定时器复位。	R(/W) *2
b2	SWRF	软件复位检测标志	0：未检测到软件复位1：检测到软件复位。	R(/W) *2
b7 to b3	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b8	RPERF	SRAM奇偶校验错误复位检测标志	0：未检测到SRAM奇偶校验错误复位1：检测到SRAM奇偶校验错误复位。	R(/W) *2
b9	REERF	SRAMECC错误复位检测标志	0：未检测到SRAMECC错误复位1：检测到SRAMECC错误复位。	R(/W) *2
b10	BUSSRF	总线从机MPU错误复位检测标志	0：未检测到总线从机MPU错误复位1：检测到总线从机MPU错误复位。	R(/W) *2
b11	BUSMRF	总线主控MPU错误复位检测标志	0：未检测到总线主控MPU错误复位1：检测到总线主控MPU错误复位。	R(/W) *2

Bit	Symbol	Bit name	Description	R/W
b12	SPERF	SP Error Reset Detect Flag	0: SP error reset not detected 1: SP error reset detected.	R(/W) *2
b15 to b13	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. The value after reset depends on the reset source.
Note 2. Only 0 can be written to clear the flag. The flag must be cleared by writing 0 after 1 is read.

IWDTRF flag (Independent Watchdog Timer Reset Detect Flag)

The IWDTRF flag indicates that an independent watchdog timer reset occurred.

[Setting condition]

- When an independent watchdog timer reset occurs.

[Clearing conditions]

- When a reset listed in Table 6.2 occurs
- When 1 is read from and then 0 is written to IWDTRF.

WDTRF flag (Watchdog Timer Reset Detect Flag)

The WDTRF flag indicates that a watchdog timer reset occurred.

[Setting condition]

- When a watchdog timer reset occurs.

[Clearing conditions]

- When a reset listed in Table 6.2 occurs
- When 1 is read from and then 0 is written to WDTRF.

SWRF flag (Software Reset Detect Flag)

The SWRF flag indicates that a software reset occurred.

[Setting condition]

- When a software reset occurs.

[Clearing conditions]

- When a reset listed in Table 6.2 occurs
- When 1 is read from and then 0 is written to SWRF.

RPERF flag (SRAM Parity Error Reset Detect Flag)

The RPERF flag indicates that a SRAM parity error reset occurred.

[Setting condition]

- When an SRAM parity error reset occurs.

[Clearing conditions]

- When a reset listed in Table 6.2 occurs
- When 1 is read from and then 0 is written to RPERF.

REERF flag (SRAM ECC Error Reset Detect Flag)

The REERF flag indicates that an SRAM ECC error reset occurred.

[Setting condition]

- When an SRAM ECC error reset occurs.

Bit	Symbol	位名称	Description	R/W
b12	SPERF	SP错误复位检测标志	0：未检测到SP错误复位1： 检测到SP错误复位。	R(/W) *2
b15 to b13	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 复位后的值取决于复位源。
Note 2. 只能写入0来清除标志。该标志必须在读取1后写入0来清除。

IWDTRF标志（独立看门狗定时器复位检测标志）

IWDTRF标志指示发生了独立的看门狗定时器复位。

[Setting condition]

- 当发生独立的看门狗定时器复位时。

[Clearing conditions]

- 发生表6.2中列出的复位时
- 从IWDTRF读取1然后将0写入IWDTRF。

WDTRF标志（看门狗定时器复位检测标志）

WDTRF标志表示发生了看门狗定时器复位。

[Setting condition]

- 当发生看门狗定时器复位时。

[Clearing conditions]

- 发生表6.2中列出的复位时
- 当从WDTRF读取1然后将0写入WDTRF。

SWRF标志（软件复位检测标志）

SWRF标志表明发生了软件复位。

[Setting condition]

- 当发生软件复位时。

[Clearing conditions]

- 发生表6.2中列出的复位时
- 从1读取然后0写入SWRF。

RPERF标志（SRAM奇偶校验错误复位检测标志）

RPERF标志表明发生了SRAM奇偶校验错误复位。

[Setting condition]

- 当SRAM奇偶校验错误复位发生时。

[Clearing conditions]

- 发生表6.2中列出的复位时
- 当从RPERF读取1然后将0写入RPERF。

REERF标志（SRAMECC错误复位检测标志）

REERF标志表明发生了SRAMECC错误复位。

[Setting condition]

- 当SRAMECC错误复位发生时。

[Clearing conditions]

- When a reset listed in Table 6.2 occurs
- When 1 is read from and then 0 is written to REERF.

BUSSRF flag (Bus Slave MPU Error Reset Detect Flag)

The BUSSRF flag indicates that a bus slave MPU error reset occurred.

[Setting condition]

- When a bus slave MPU error reset occurs.

[Clearing conditions]

- When a reset listed in Table 6.2 occurs
- When 1 is read from and then 0 is written to BUSSRF.

BUSMRF flag (Bus Master MPU Error Reset Detect Flag)

The BUSMRF flag indicates that a bus master MPU error reset occurred.

[Setting condition]

- When a bus master MPU error reset occurs.

[Clearing conditions]

- When a reset listed in Table 6.2 occurs
- When 1 is read from and then 0 is written to BUSMRF.

SPERF flag (SP Error Reset Detect Flag)

The SPERF flag indicates that a stack pointer error reset occurred.

[Setting condition]

- When a stack pointer error reset occurs.

[Clearing conditions]

- When a reset listed in Table 6.2 occurs
- When 1 is read from and then 0 is written to SPERF.

6.2.3 Reset Status Register 2 (RSTSR2)

Address(es): SYSTEM.RSTSR2 4001 E411h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	CWSF
Value after reset:	0	0	0	0	0	0	0	x*1

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b0	CWSF	Cold/Warm Start Determination Flag	0: Cold start 1: Warm start.	R(/W) *2
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. The value after reset depends on the reset source.
Note 2. Only 1 can be written, to set the flag.

RSTSR2 determines whether a power-on reset caused the reset processing (cold start) or a reset signal input during operation caused the reset processing (warm start).

[Clearing conditions]

- 发生表6.2中列出的复位时
- 当从REERF读取1然后将0写入REERF。

BUSSRF标志（总线从机MPU错误复位检测标志）

BUSSRF标志表示发生了总线从机MPU错误复位。

[Setting condition]

- 当发生总线从机MPU错误复位时。

[Clearing conditions]

- 发生表6.2中列出的复位时
- 当从1被读取然后0被写入BUSSRF。

BUSMRF标志（总线主控MPU错误复位检测标志）

BUSMRF标志指示发生了总线主控MPU错误复位。

[Setting condition]

- 当发生总线主控MPU错误复位时。

[Clearing conditions]

- 发生表6.2中列出的复位时
- 读取1，然后将0写入BUSMRF。

SPERF标志（SP错误复位检测标志）

SPERF标志表明发生了堆栈指针错误复位。

[Setting condition]

- 发生堆栈指针错误复位时。

[Clearing conditions]

- 发生表6.2中列出的复位时
- 当从SPERF读取1然后将0写入SPERF。

6.2.3 复位状态寄存器2(RSTSR2)

Address(es): SYSTEM.RSTSR2 4001 E411h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	CWSF
重置后的值：	0	0	0	0	0	0	0	x*1

x: Undefined

Bit	Symbol	位名称	Description	R/W
b0	CWSF	冷暖启动确定标志	0：冷启动1： 热启动。	R(/W) *2
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 复位后的值取决于复位源。
Note 2. 只能写入1来设置标志。

RSTSR2判断是上电复位导致复位处理（冷启动）还是操作期间输入的复位信号导致复位处理（热启动）。

CWSF flag (Cold/Warm Start Determination Flag)

The CWSF flag indicates the type of reset processing, either cold start or warm start. The CWSF flag is initialized by a power-on reset. It is not initialized by a reset signal generated by the RES pin.

[Setting condition]

- When 1 is written through the software. Writing 0 to CWSF does not set it to 0.

[Clearing condition]

- When a reset listed in Table 6.2 occurs.

6.3 Operation

6.3.1 RES Pin Reset

The RES pin generates this reset. When the RES pin is driven low, all the processing in progress is aborted and the MCU enters a reset state. To successfully reset the MCU, the RES pin must be held low for the power supply stabilization time specified at power-on.

When the RES pin is driven high from low, the internal reset is canceled after the post-RES cancellation wait time (t_{RESWT}) elapses. The CPU then starts the reset exception handling.

For details, see section 60, Electrical Characteristics.

6.3.2 Power-On Reset

The power-on reset circuit generates this internal reset. If the RES pin is in a high-level state when power is supplied, a power-on reset is generated. After VCC exceeds VPOR and the specified period (power-on reset time) elapses, the internal reset is canceled and the CPU starts the reset exception handling. The power-on reset time is the stabilization period for the external power supply and the MCU circuit. After a power-on reset is generated, the PORF flag in the RSTSR0 is set to 1. The PORF flag is initialized by the RES pin reset.

The voltage monitor 0 reset is an internal reset generated by the voltage monitor circuit. If the Voltage Detection 0 Circuit Start bit (LVDAS) in Option Function Select Register 1 (OFS1) is 0 (voltage monitor 0 reset is enabled after a reset) and VCC falls below V_{det0}, the RSTSR0.LVD0RF flag is set to 1 and the voltage detection circuit generates a voltage monitor 0 reset. Clear the OFS1.LVDAS bit to 0 if the voltage monitor 0 reset is to be used.

After VCC exceeds V_{det0} and the voltage monitor 0 reset time (tLVD0) elapses, the internal reset is canceled and the CPU starts the reset exception handling. The V_{det0} voltage detection level can be changed by the setting in the VDSEL[1:0] bits in Option Function Select Register 1 (OFS1).

Figure 6.1 shows an example of operations during a power-on reset and voltage monitor 0 reset.

CWSF标志（冷暖启动确定标志）

CWSF标志指示复位处理的类型，冷启动或热启动。CWSF标志由上电复位初始化。它不会被RES引脚产生的复位信号初始化。

[Setting condition]

- 当通过软件写入1时。将0写入CWSF不会将其设置为0。

[Clearing condition]

- 发生表6.2中列出的复位时。

6.3 Operation

6.3.1 RES引脚复位

RES引脚产生此复位。当RES引脚被驱动为低电平时，所有正在进行的处理都被中止，MCU进入复位状态。要成功复位MCU，RES引脚必须在上电时指定的电源稳定时间内保持低电平。

当RES引脚从低电平驱动为高电平时，内部复位会在RES取消后等待时间(tRESWT)过去后取消。CPU然后开始复位异常处理。

有关详细信息，请参见第60节，电气特性。

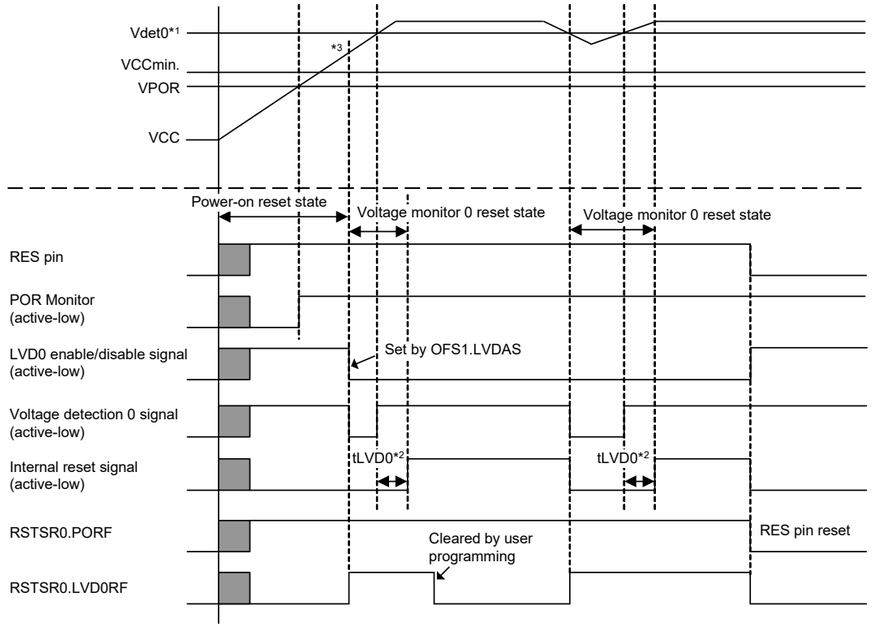
6.3.2 Power-On Reset

上电复位电路产生这个内部复位。如果上电时RES管脚处于高电平状态，则产生上电复位。在VCC超过VPOR并经过指定的周期（上电复位时间）后，内部复位被取消，CPU开始复位异常处理。上电复位时间是外部电源和MCU电路的稳定期。上电复位产生后，RSTSR0中的PORF标志设置为1。PORF标志由RES引脚复位初始化。

电压监控器0复位是由电压监控器电路产生的内部复位。如果电压检测0选项功能选择寄存器1(OFS1)中的电路起始位(LVDAS)为0（复位后使能电压监控器0复位）且VCC低于Vdet0，RSTSR0.LVD0RF标志设置为1，电压检测电路生成电压监视器0复位。如果要使用电压监视器0复位，则将OFS1.LVDAS位清零。

在VCC超过Vdet0并且电压监视器0复位时间(tLVD0)过去后，内部复位被取消，并且CPU启动复位异常处理。Vdet0电压检测电平可以通过在选项功能选择寄存器1(OFS1)中的VDSEL[1:0]位。

图6.1显示了上电复位和电压监视器0复位期间的操作示例。



Note: For details on the electrical characteristics, see section 60, Electrical Characteristics.
Note 1. V_{det0} shows a voltage monitor 0 reset detection level, VPOR shows a power-on reset detection level, and VCCmin shows minimum guaranteed voltage of MCU.
Note 2. tLVD0 shows a time for voltage monitor 0 reset.
Note 3. At power-on, VCC should have risen to the minimum guaranteed voltage before the POR reset is released.

Figure 6.1 Example of operations during power-on and voltage monitor 0 resets

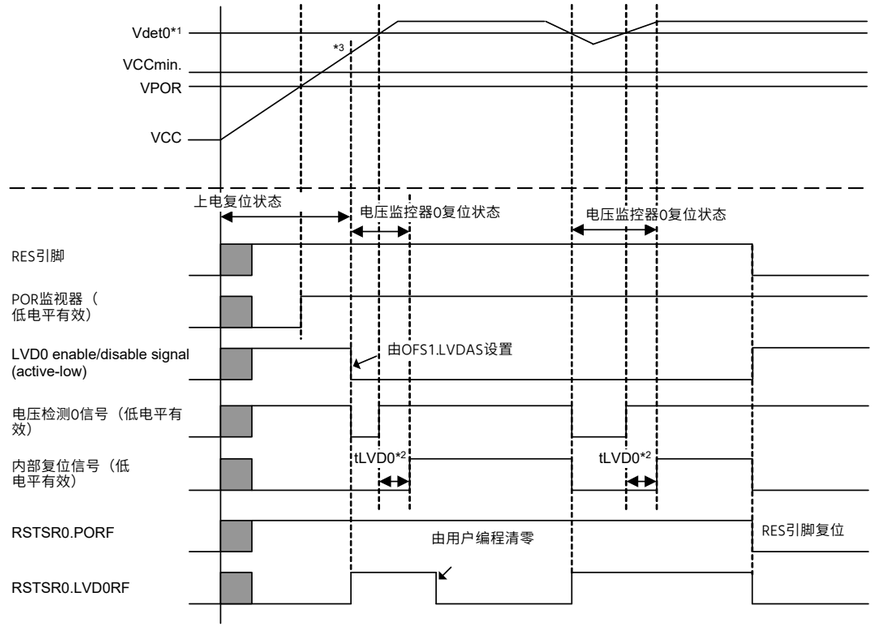
6.3.3 Voltage Monitor Reset

The voltage monitor circuit generates this internal reset. If the Voltage Detection 0 Circuit Start bit (LVDAS) in Option Function Select Register 1 (OFS1) is 0 (voltage monitor 0 reset is enabled after a reset) and VCC falls below V_{det0}, the RSTSR0.LVD0RF flag is set to 1 and the voltage detection circuit generates voltage monitor 0 reset. Clear the OFS1.LVDAS bit to 0 if the voltage monitor 0 reset is to be used. After VCC exceeds V_{det0} and the voltage monitor 0 reset time (tLVD0) elapses, the internal reset is canceled and the CPU starts the reset exception handling.

When the Voltage Monitor 1 Interrupt/Reset Enable bit (RIE) is set to 1 (enabling generation of a reset or interrupt by the voltage detection circuit) and the voltage monitor 1 circuit mode select bit (LVD1CR0.RI) is set to 1 (selecting generation of a reset in response to detection of a low voltage) in Voltage Monitor 1 Circuit Control Register 0 (LVD1CR0), the RSTSR0.LVD1RF flag is set to 1 and the voltage detection circuit generates a voltage monitor 1 reset if VCC falls to or below V_{det1}.

Likewise, when the Voltage Monitor 2 Interrupt/Reset Enable bit (RIE) is set to 1 (enabling generation of a reset or interrupt by the voltage detection circuit) and the Voltage Monitor 2 Circuit Mode Select bit (RI) is set to 1 (selecting generation of a reset in response to detection of a low voltage) in Voltage Monitor 2 Circuit Control Register 0 (LVD2CR0), the RSTSR0.LVD2RF flag is set to 1 and the voltage detection circuit generates a voltage monitor 2 reset if VCC falls to or below V_{det2}.

Similarly, timing for release from the voltage monitor 1 reset state is selectable in the Voltage Monitor 1 Reset Negate Select bit (RN) in LVD1CR0. When the RN bit is 0 and VCC falls to or below V_{det1}, the CPU is released from the internal reset state and starts reset exception handling when the LVD1 reset time (tLVD1) elapses after VCC rises above V_{det1}. When the LVD1CR0.RN bit is 1 and VCC falls to or below V_{det1}, the CPU is released from the internal reset state and starts reset exception handling when the LVD1 reset time (tLVD1) elapses.



Note: 有关电气特性的详细信息，请参见第60节，电气特性。
Note 1. Vdet0表示电压监视器0复位检测电平，VPOR表示上电复位检测电平，VCCmin表示MCU的最低保证电压。
Note 2. tLVD0显示电压监视器0复位的时间。
Note 3. 上电时，VCC应该在POR复位释放之前上升到最低保证电压。

Figure 6.1 上电和电压监控0复位期间的操作示例

6.3.3 电压监视器复位

电压监控电路产生这个内部复位。如果选项功能选择寄存器1(OFS1)中的电压检测0电路启动位(LVDAS)为0（复位后使能电压监视器0复位）并且VCC低于Vdet0，则RSTSR0.LVD0RF标志设置为1并且电压检测电路产生电压监测0复位。清除

如果要使用电压监视器0复位，则OFS1.LVDAS位为0。在VCC超过Vdet0并且电压监视器0复位时间(tLVD0)过去后，内部复位被取消，CPU开始复位异常处理。

当电压监视器1中断复位允许位(RIE)设置为1（允许电压检测电路产生复位或中断）且电压监视器1电路模式选择位(LVD1CR0.RI)设置为1（选择在电压监控器1电路控制寄存器0(LVD1CR0)中响应检测到低电压产生复位，RSTSR0.LVD1RF标志设置为1，如果VCC下降到或电压检测电路产生电压监控器1复位低于Vdet1。

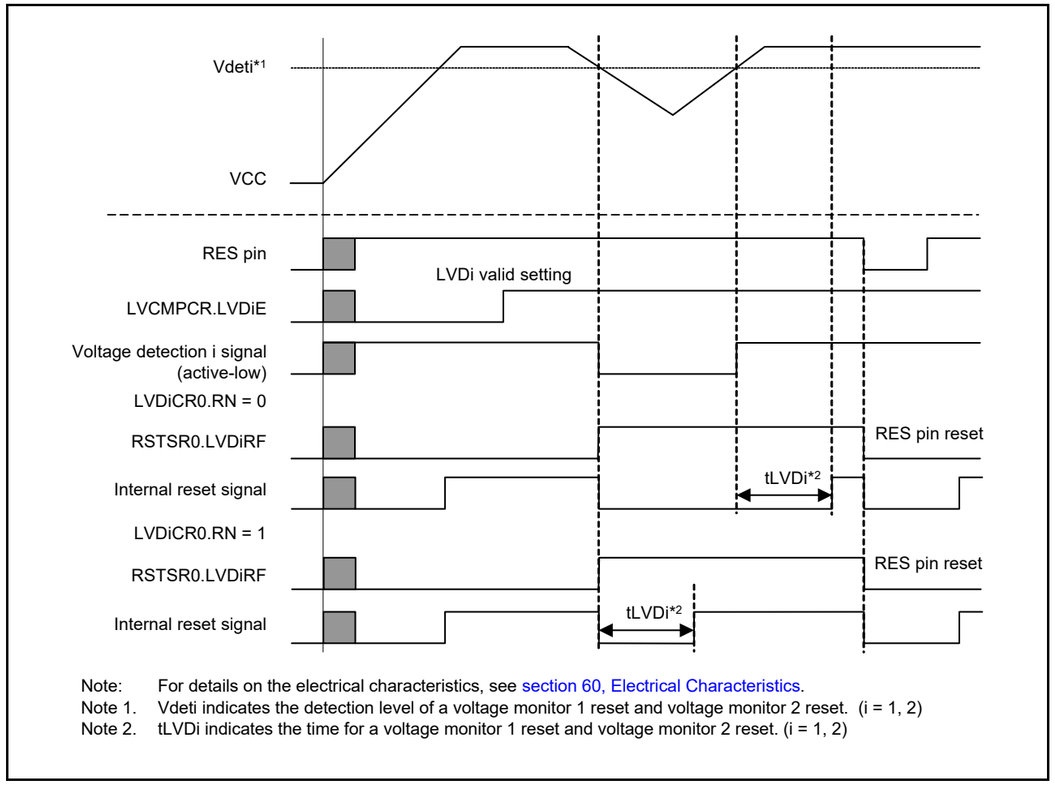
同样，当电压监视器2中断复位使能位(RIE)设置为1（允许电压检测电路产生复位或中断）并且电压监视器2电路模式选择位(RI)设置为1（选择在电压监控器2电路控制寄存器0(LVD2CR0)中响应检测到低电压产生复位），RSTSR0.LVD2RF标志设置为1，如果VCC下降到或电压检测电路产生电压监控器2复位低于Vdet2。

类似地，从电压监视器1复位状态释放的时间可在电压监视器1复位否定中选择
LVD1CR0中的选择位(RN)。当RN位为0且VCC下降至或低于Vdet1时，CPU会从内部复位状态中释放，并在VCC上升至高于Vdet1后经过LVD1复位时间(tLVD1)时开始复位异常处理。当LVD1CR0.RN位为1且VCC下降到或低于Vdet1时，CPU会从内部复位状态中释放，并在LVD1复位时间(tLVD1)过后开始复位异常处理。

Likewise, timing for release from the voltage monitor 2 reset state is selectable in the Voltage Monitor 2 Reset Negate Select bit (RN) in the LDV2CR0 register.

Detection levels V_{det1} and V_{det2} can be changed in the Voltage Detection Level Select Register (LDVLVLR).

Figure 6.2 shows examples of operations during voltage monitor 1 and 2 resets. For details on the voltage monitor 1 reset and voltage monitor 2 reset, see section 8, Low Voltage Detection (LVD).



Note: For details on the electrical characteristics, see section 60, Electrical Characteristics.
Note 1. Vdeti indicates the detection level of a voltage monitor 1 reset and voltage monitor 2 reset. (i = 1, 2)
Note 2. tLVDi indicates the time for a voltage monitor 1 reset and voltage monitor 2 reset. (i = 1, 2)

Figure 6.2 Example operations during voltage monitor 1 and voltage monitor 2 resets

6.3.4 Deep Software Standby Reset

This internal reset is generated when Deep Software Standby mode is canceled by an associated interrupt. The Deep Software Standby reset is canceled after tDSBY (return time after Deep Software Standby mode cancellation) elapses. At the same time, Deep Software Standby mode is also canceled.

When tDSBYWT (wait time after Deep Software Standby mode cancellation) elapses after Deep Software Standby mode is canceled, the internal reset is canceled and the CPU starts the reset exception handling.

For details on the Deep Software Standby reset, see section 11, Low Power Modes.

6.3.5 Independent Watchdog Timer Reset

The independent watchdog timer reset is an internal reset generated from the Independent Watchdog Timer (IWDT). Output of the reset from the IWDT can be selected in the Option Function Select Register 0 (OFS0).

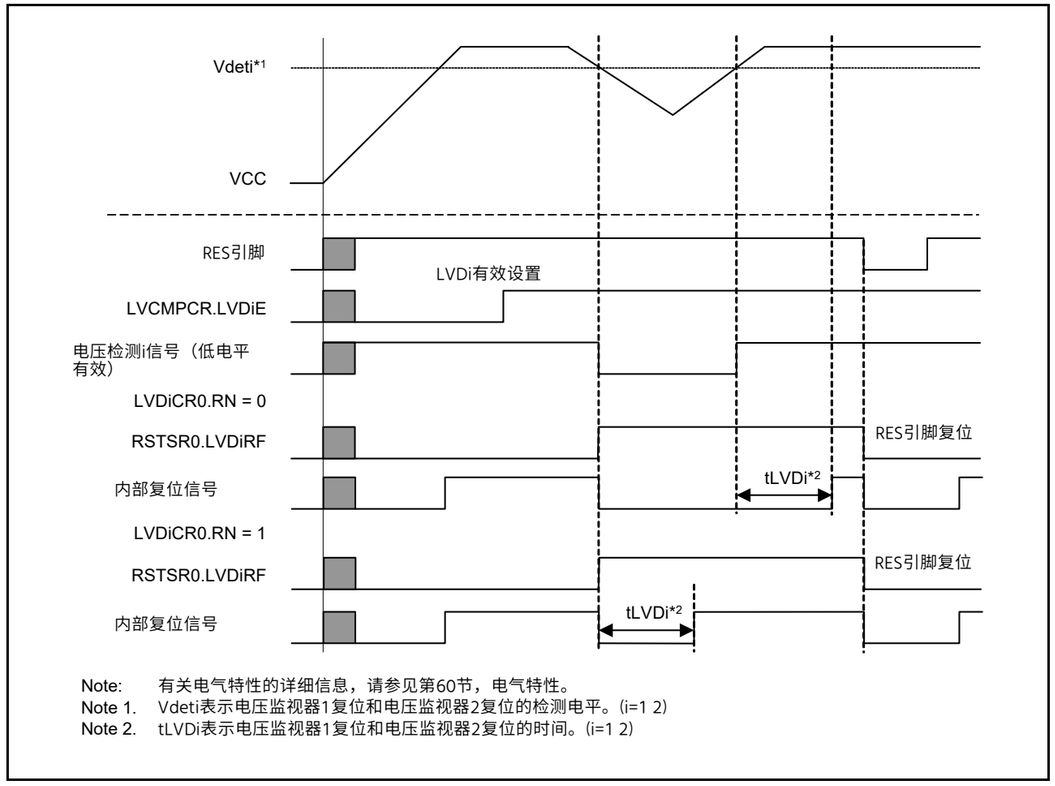
When output of the independent watchdog timer reset is selected, the reset is generated if the IWDT underflows, or if data is written when refresh operation is disabled. When the internal reset time (tRESW2) elapses after the independent watchdog timer reset is generated, the internal reset is canceled and the CPU starts the reset exception handling.

For details on the independent watchdog timer reset, see section 28, Independent Watchdog Timer (IWDT).

同样，从电压监视器2复位状态中释放的时间可在电压监视器2复位否定中选择LDV2CR0寄存器中的选择位(RN)。

检测电平Vdet1和Vdet2可以在电压检测电平选择寄存器(LDVLVLR)中更改。

图6.2显示了电压监视器1和2复位期间的操作示例。有关电压监视器1复位和电压监视器2复位的详细信息，请参阅第8节，低电压检测(LVD)。



Note: 有关电气特性的详细信息，请参见第60节，电气特性。
Note 1. Vdeti表示电压监视器1复位和电压监视器2复位的检测电平。(i=1 2)
Note 2. tLVDi表示电压监视器1复位和电压监视器2复位的时间。(i=1 2)

Figure 6.2 电压监视器1和电压监视器2复位期间的示例操作

6.3.4 深度软件待机复位

当深度软件待机模式被相关中断取消时，会产生此内部复位。深渊软件待机复位在tDSBY（深度软件待机模式取消后的返回时间）过去后取消。同时，深度软件待机模式也被取消。

当深度软件待机模式取消后经过tDSBYWT（深度软件待机模式取消后的等待时间）时，内部复位被取消并且CPU开始复位异常处理。

有关深度软件待机复位的详细信息，请参见第11节，低功耗模式。

6.3.5 独立看门狗定时器复位

独立看门狗定时器复位是由独立看门狗定时器（IWDT）产生的内部复位。可以在选项功能选择寄存器0(OFS0)中选择IWDT的复位输出。

Whenoutputoftheindependentwatchdogtimerresetisselected theresetisgeneratediftheIWDTunderflows orifdataiswrittenwhenrefreshoperationisdisabled.当独立看门狗定时器复位产生后经过内部复位时间(tRESW2)时，内部复位被取消，CPU开始复位异常处理。

有关独立看门狗定时器复位的详细信息，请参见第28节，独立看门狗定时器(IWDT)。

6.3.6 Watchdog Timer Reset

The watchdog timer generates this internal reset. Output of the reset from the WDT can be selected in the WDT Reset Control Register (WDTRCR) or Option Function Select Register 0 (OFS0).

When output of the watchdog timer reset is selected, the reset is generated if the WDT underflows, or if data is written when refresh operation is disabled. When the internal reset time (tRESW2) elapses after the watchdog timer reset is generated, the internal reset is canceled and the CPU starts the reset exception handling.

For details on the watchdog timer reset, see section 27, Watchdog Timer (WDT).

6.3.7 Software Reset

This internal reset is generated by a software setting of the SYSRESETREQ bit in the AIRCR register in the Arm core. When the SYSRESETREQ bit is set to 1, a software reset is generated. When the internal reset time (tRESW2) elapses after the software reset is generated, the internal reset is canceled and the CPU starts the reset exception handling.

For details on the SYSRESETREQ bit, see the *ARM® Cortex®-M4 Technical Reference Manual*.

6.3.8 Determination of Cold/Warm Start

Read the CWSF flag in RSTSR2 to determine the cause of reset processing. The flag indicates whether a power-on reset caused the reset processing (cold start) or a reset signal input during operation caused the reset processing (warm start).

The flag is set to 0 when a power-on reset occurs (cold start). Otherwise, the flag is not set to 0. The flag is set to 1 when 1 is written to it through software. It is not set to 0 even on writing 0 to it.

Figure 6.3 shows an example of a cold/warm start determination operation.

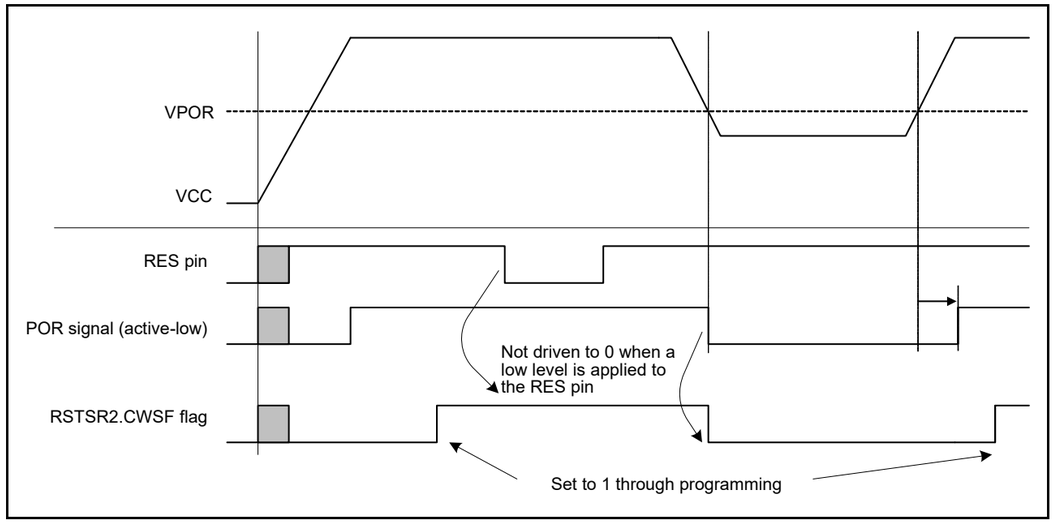


Figure 6.3 Example of cold/warm start determination operation

6.3.9 Determination of Reset Generation Source

Read RSTSR0 and RSTSR1 to determine which reset is used to execute the reset exception handling. Figure 6.4 shows an example of the flow for identifying a reset generation source. The reset flag must be written with 0 after it is read as 1.

6.3.6 看门狗定时器复位

看门狗定时器产生这个内部复位。WDT的复位输出可以在WDT复位中选择控制寄存器(WDTRCR)或选项功能选择寄存器0(OFS0)。

选择看门狗定时器复位的输出时，如果WDT下溢，或者在禁止刷新操作时写入数据，则产生复位。当看门狗定时器复位产生后经过内部复位时间(tRESW2)时，内部复位被取消，CPU开始复位异常处理。

有关看门狗定时器复位的详细信息，请参见第27节，看门狗定时器(WDT)。

6.3.7 软件复位

此内部复位由Arm内核中AIRCR寄存器中的SYSRESETREQ位的软件设置生成。当SYSRESETREQ位设置为1时，会产生软件复位。当软件复位产生后经过内部复位时间(tRESW2)时，内部复位被取消，CPU开始复位异常处理。

有关SYSRESETREQ位的详细信息，请参阅ARM®Cortex®-M4技术参考手册。

6.3.8 冷暖启动的测定

读取RSTSR2中的CWSF标志以确定复位处理的原因。该标志指示是上电复位导致复位处理（冷启动）还是操作期间输入的复位信号导致复位处理（热启动）。

当发生上电复位（冷启动）时，该标志设置为0。否则，该标志不设置为0。当通过软件向其写入1时，该标志设置为1。即使向其写入0，它也不会设置为0。

图6.3显示了冷暖启动确定操作的示例。

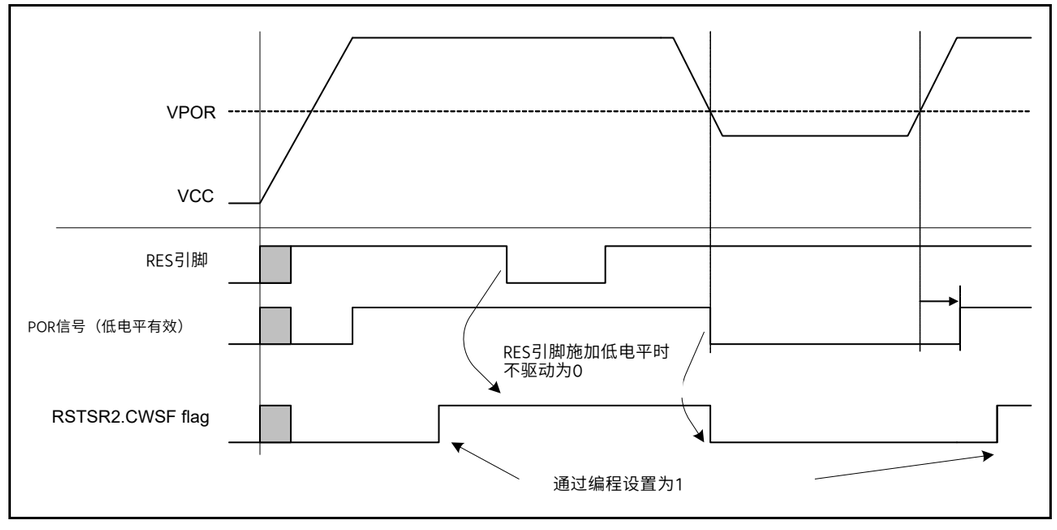
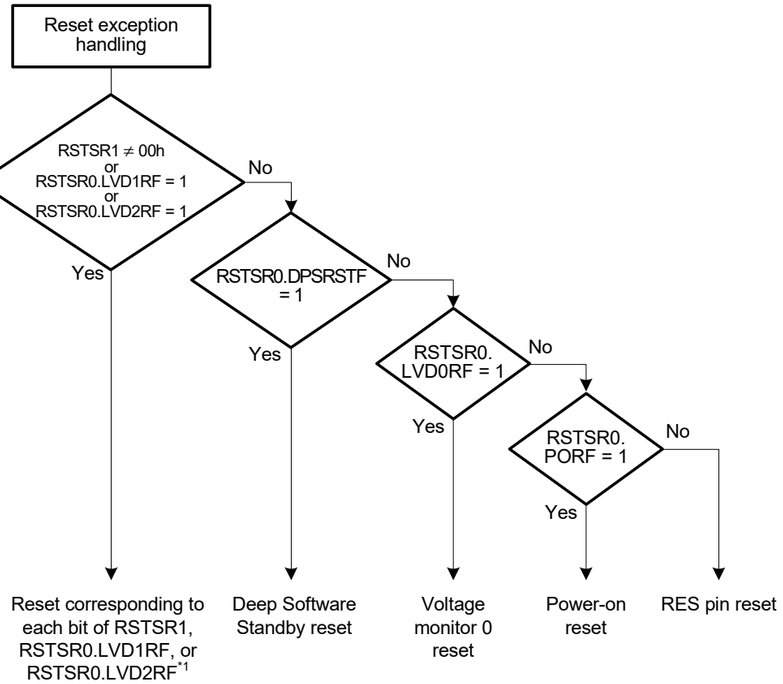


Figure 6.3 冷暖启动判定动作示例

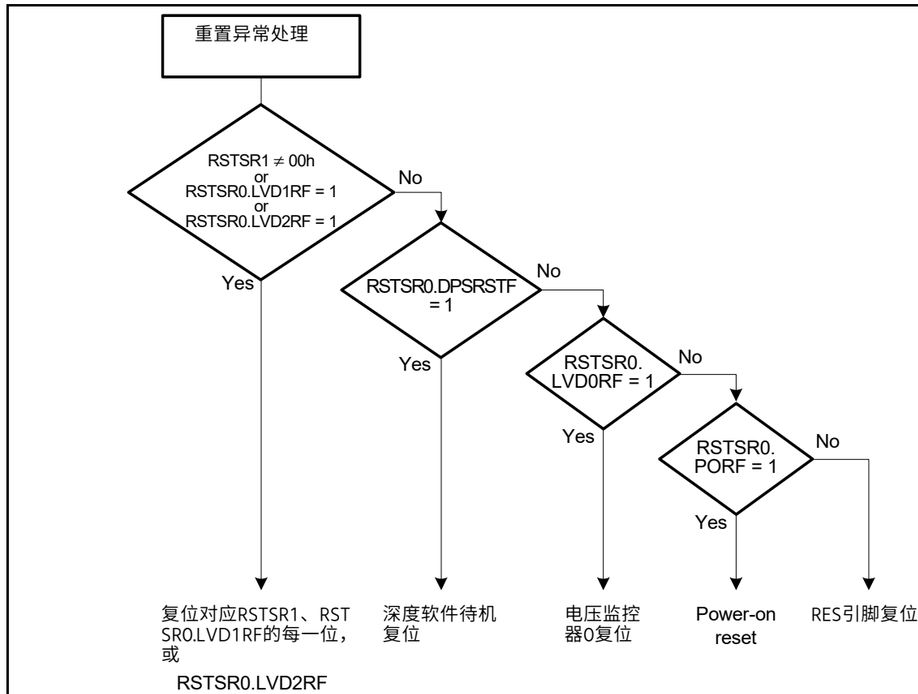
6.3.9 复位产生源的确定

读取RSTSR0和RSTSR1以确定使用哪个复位来执行复位异常处理。图6.4显示了识别复位产生源的流程示例。复位标志读为1后必须写为0。



Note 1. If two or more resets associated with the RSTSR1, RSTSR0.LVD1RF, or RSTSR0.LVD2RF bits occur at the same time, all reset flags are set to 1.

Figure 6.4 Example of reset generation source determination flow



Note 1. 如果与RSTSR1、RSTSR0.LVD1RF或RSTSR0.LVD2RF位相关的两个或多个复位同时发生，则所有复位标志都设置为1。

Figure 6.4 复位产生源确定流程示例

7. Option-Setting Memory

7.1 Overview

The option-setting memory determines the state of the MCU after a reset. It is allocated to the configuration setting area and the program flash area of the flash memory, and the available methods of setting are different for the two areas. Figure 7.1 shows the option-setting memory area.

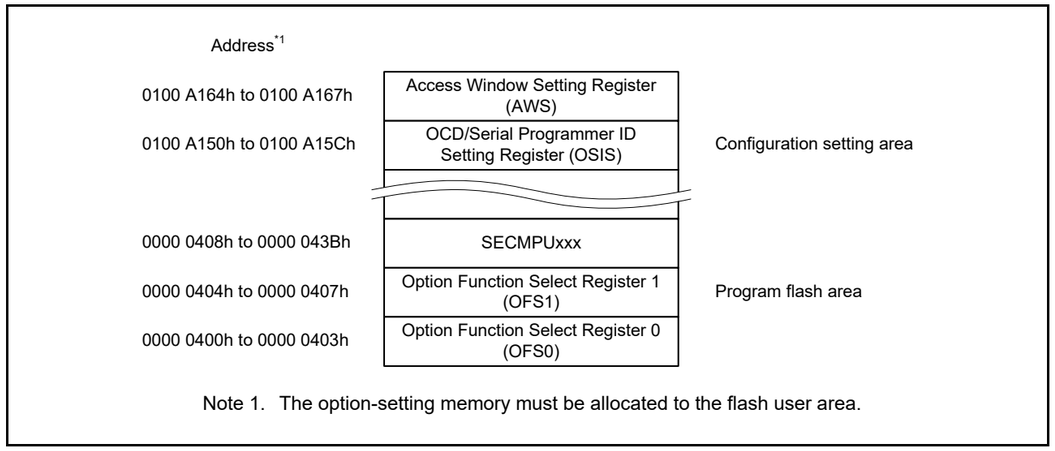


Figure 7.1 Option-setting memory area

7.2 Register Descriptions

7.2.1 Option Function Select Register 0 (OFS0)

Address(es): OFS0 0000 0400h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	WDTST PCTL	—	WDTRS TIRQS	WDTRPSS[1:0]		WDTRPES[1:0]		WDTCKS[3:0]				WDTTOPS[1:0]		WDTST RT	—
Value after reset:					User setting*1											

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	IWDTS TPCTL	—	IWDTRS TIRQS	IWDTRPSS[1:0]		IWDTRPES[1:0]		IWDTCKS[3:0]				IWDTTOPS[1:0]		IWDTS TRT	—
Value after reset:					User setting*1											

Bit	Symbol	Bit name	Description	R/W
b0	—	Reserved	When read, this bit returns the written value. The write value should be 1.	R
b1	IWDTSTRT	IWDT Start Mode Select	0: Automatically activate IWDT after a reset (auto start mode) 1: Disable IWDT.	R
b3, b2	IWDTTOPS[1:0]	IWDT Timeout Period Select	b3 b2 0 0: 128 cycles (007Fh) 0 1: 512 cycles (01FFh) 1 0: 1024 cycles (03FFh) 1 1: 2048 cycles (07FFh).	R

7. Option-Setting Memory

7.1 Overview

选项设置存储器确定复位后MCU的状态。它被分配到闪存的配置设置区和程序闪存区，两个区域的可用设置方法不同。图7.1显示了选项设置存储区。

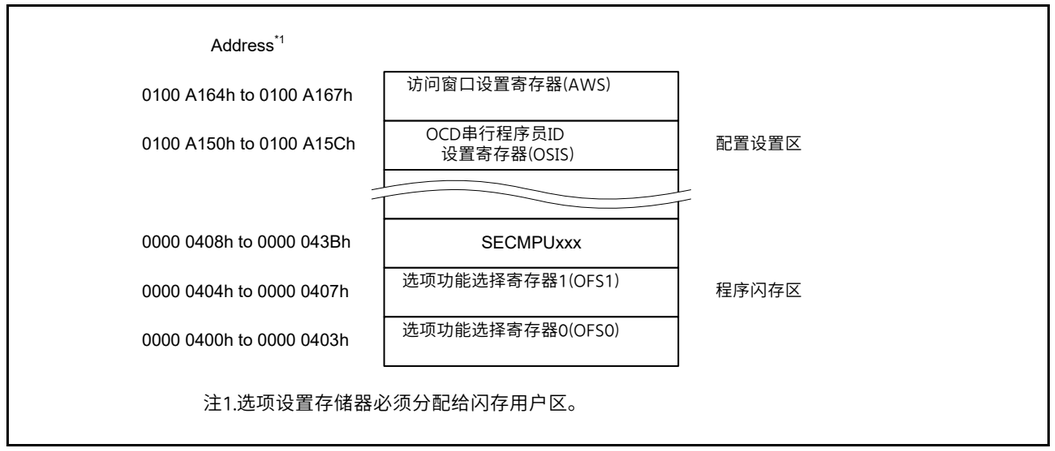


Figure 7.1 选项设置存储区

7.2 注册说明

7.2.1 选项功能选择寄存器0(OFS0)

Address(es): OFS0 0000 0400h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	WDTST PCTL	—	WDTRS TIRQS	WDTRPSS[1:0]		WDTRPES[1:0]		WDTCKS[3:0]				WDTTOPS[1:0]		WDTST RT	—
重置后的值:					用户设置*1											

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	IWDTS TPCTL	—	IWDTRS TIRQS	IWDTRPSS[1:0]		IWDTRPES[1:0]		IWDTCKS[3:0]				IWDTTOPS[1:0]		IWDTS TRT	—
重置后的值:					用户设置*1											

Bit	Symbol	位名称	Description	R/W
b0	—	Reserved	读取时，该位返回写入的值。写入值应为1。	R
b1	IWDTSTRT	IWDT启动模式选择	0：复位后自动激活IWDT（自动启动模式）1：禁用IWDT。	R
b3, b2	IWDTTOPS[1:0]	IWDT超时周期选择	b3 b2 0 0: 128 cycles (007Fh) 0 1: 512 cycles (01FFh) 1 0: 1024 cycles (03FFh) 1 1: 2048 cycles (07FFh).	R

Bit	Symbol	Bit name	Description	R/W
b7 to b4	IWDTCKS[3:0]	IWDT-Dedicated Clock Frequency Division Ratio Select	b7 b4 0 0 0 0: × 1 0 0 1 0: × 1/16 0 0 1 1: × 1/32 0 1 0 0: × 1/64 1 1 1 1: × 1/128 0 1 0 1: × 1/256. Other settings are prohibited.	R
b9, b8	IWDTRPES[1:0]	IWDT Window End Position Select	b9 b8 0 0: 75% 0 1: 50% 1 0: 25% 1 1: 0% (no window end position setting).	R
b11, b10	IWDTRPSS[1:0]	IWDT Window Start Position Select	b11 b10 0 0: 25% 0 1: 50% 1 0: 75% 1 1: 100% (no window start position setting).	R
b12	IWDTRSTIRQS	IWDT Reset Interrupt Request Select	0: Enable non-maskable interrupt requests or interrupt requests 1: Enable resets.	R
b13	—	Reserved	When read, this bit returns the written value. The write value should be 1.	R
b14	IWDTSTPCTL	IWDT Stop Control	0: Continue counting 1: Stop counting when in Sleep, Snooze mode, Software Standby, or Deep Software Standby mode.	R
b16, b15	—	Reserved	When read, these bits return the written value. The write value should be 1.	R
b17	WDTSTRT	WDT Start Mode Select	0: Automatically activate WDT after a reset (auto start mode) 1: Stop WDT after a reset (register start mode).	R
b19, b18	WDTTOPS[1:0]	WDT Timeout Period Select	b19 b18 0 0: 1024 cycles (03FFh) 0 1: 4096 cycles (0FFFh) 1 0: 8192 cycles (1FFFh) 1 1: 16384 cycles (3FFFh).	R
b23 to b20	WDTCKS[3:0]	WDT Clock Frequency Division Ratio Select	b23 b20 0 0 0 1: PCLKB divided by 4 0 1 0 0: PCLKB divided by 64 1 1 1 1: PCLKB divided by 128 0 1 1 0: PCLKB divided by 512 0 1 1 1: PCLKB divided by 2048 1 0 0 0: PCLKB divided by 8192. Other settings are prohibited.	R
b25, b24	WDTRPES[1:0]	WDT Window End Position Select	b25 b24 0 0: 75% 0 1: 50% 1 0: 25% 1 1: 0% (No window end position setting).	R
b27, b26	WDTRPSS[1:0]	WDT Window Start Position Select	b27 b26 0 0: 25% 0 1: 50% 1 0: 75% 1 1: 100% (No window start position setting).	R
b28	WDTRSTIRQS	WDT Reset Interrupt Request Select	WDT Behavior Select 0: NMI 1: Reset.	R
b29	—	Reserved	When read, these bits return the written value. The write value should be 1.	R
b30	WDTSTPCTL	WDT Stop Control	0: Continue counting 1: Stop counting when entering Sleep mode.	R
b31	—	Reserved	When read, these bits return the written value. The write value should be 1.	R

Bit	Symbol	位名称	Description	R/W
b7 to b4	IWDTCKS[3:0]	IWDT-Dedicated Clock 分频比 Select	b7b40000：×10010：×116 0011：×1320100：×16411 11：×11280101：×1256。 禁止其他设置。	R
b9, b8	IWDTRPES[1:0]	IWDT窗口结束位置 Select	b9b800：75%01：50%10：25%11：0% （无窗口结束位置设置）。	R
b11, b10	IWDTRPSS[1:0]	IWDT窗口起始位置 Select	b11b1000：25%01：50%10：75%11：100 %（无窗口起始位置设置）。	R
b12	IWDTRSTIRQS	IWDT复位中断 请求选择	0：使能不可屏蔽的中断请求或中断请求1：使能复位 。	R
b13	—	Reserved	读取时，该位返回写入的值。写入值应为1。	R
b14	IWDTSTPCTL	IWDT停止控制	0：继续计数1：在休眠、贪睡模式、软件待机或深度软件待机模式下停止计数。	R
b16, b15	—	Reserved	读取时，这些位返回写入的值。写入值应为1。	R
b17	WDTSTRT	WDT启动模式选择	0：复位后自动激活WDT（自动启动模式）1：复位后停止WDT（寄存器启动模式）。	R
b19, b18	WDTTOPS[1:0]	WDT超时周期选择	b19 b18 0 0: 1024 cycles (03FFh) 0 1: 4096 cycles (0FFFh) 1 0: 8192 cycles (1FFFh) 1 1: 16384 cycles (3FFFh).	R
b23 to b20	WDTCKS[3:0]	WDT时钟频率 分频比选择	b23b200001：PCLKB除以40100： PCLKB除以641111：PCLKB除以12 80110：PCLKB除以5120111：PCL KB除以20481000：PCLKB除以819 2。禁止其他设置。	R
b25, b24	WDTRPES[1:0]	WDT窗口结束位置 Select	b25b2400：75%01：50%10：25%11：0 %（无窗口结束位置设置）。	R
b27, b26	WDTRPSS[1:0]	WDT窗口起始位置 Select	b27b2600：25%01：50%10：75%11：100 %（无窗口起始位置设置）。	R
b28	WDTRSTIRQS	WDT复位中断请求 Select	WDT行为选择0：NM I1：复位。	R
b29	—	Reserved	读取时，这些位返回写入的值。写入值应为1。	R
b30	WDTSTPCTL	WDT停止控制	0：继续计数1：进入休眠模式时停止计数。	R
b31	—	Reserved	读取时，这些位返回写入的值。写入值应为1。	R

Note 1. The value in a blank product is FFFF FFFFh. It is set to the value written by your application.

IWDTSTRT bit (IWDT Start Mode Select)

The IWDTSTRT bit selects the mode in which the IWDT is activated after a reset (stopped state or activated state).

IWDTTOPS[1:0] bits (IWDT Timeout Period Select)

The IWDTTOPS[1:0] bits specify the timeout period, the time it takes for the down counter to underflow, as 128, 512, 1024, or 2048 cycles of the frequency-divided clock set in the IWDTCKS[3:0] bits. The number of clock cycles that the counter takes to underflow after a refresh operation is determined by the combination of the IWDTCKS[3:0] and IWDTTOPS[1:0] bits.

For details, see section 28, Independent Watchdog Timer (IWDT).

IWDTCKS[3:0] bits (IWDT-Dedicated Clock Frequency Division Ratio Select)

The IWDTCKS[3:0] bits specify the division ratio of the prescaler for dividing the frequency of the clock for the IWDT as 1/1, 1/16, 1/32, 1/64, 1/128, or 1/256. Using this setting combined with the IWDTTOPS[1:0] bit setting, the IWDT counting period can be set from 128 to 524,288 IWDT clock cycles.

For details, see section 28, Independent Watchdog Timer (IWDT).

IWDTRPES[1:0] bits (IWDT Window End Position Select)

The IWDTRPES[1:0] bits specify the position where the window for the down counter ends as 0%, 25%, 50%, or 75% of the count value. The value of the window end position must be smaller than the value of the window start position. Otherwise, only the value for the window start position is valid.

The counter values corresponding to the settings for the start and end positions of the window, in the IWDTRPSS[1:0] and IWDTRPES[1:0] bits, vary with the setting in the IWDTTOPS[1:0] bits.

For details, see section 28, Independent Watchdog Timer (IWDT).

IWDTRPSS[1:0] bits (IWDT Window Start Position Select)

The IWDTRPSS[1:0] bits specify the position where the window for the down counter starts as 25%, 50%, 75%, or 100% of the counted value. The point at which counting starts is 100% and the point at which an underflow occurs is 0%. The interval between the window start and end positions becomes the period in which a refresh is possible. Refresh is not possible outside this period.

For details, see section 28, Independent Watchdog Timer (IWDT).

IWDTRSTIRQS bit (IWDT Reset Interrupt Request Select)

The IWDTRSTIRQS bit selects the operation on an underflow of the down counter or generation of a refresh error. The selected operation can be an independent watchdog timer reset, non-maskable interrupt request, or interrupt request.

For details, see section 28, Independent Watchdog Timer (IWDT).

IWDTSTPCTL bit (IWDT Stop Control)

The IWDTSTPCTL bit specifies whether to stop counting when entering Sleep, Snooze, or Software Standby mode.

For details, see section 28, Independent Watchdog Timer (IWDT).

WDTSTRT bit (WDT Start Mode Select)

The WDTSTRT bit selects the mode in which the WDT is activated after a reset (stopped state or activated state). When the WDT is activated in auto start mode, the OFS0 register setting for the WDT is effective.

WDTTOPS[1:0] bits (WDT Timeout Period Select)

The WDTTOPS[1:0] bits specify the timeout period, the time it takes for the down counter to underflow, as 1024, 4096, 8192, or 16384 cycles of the frequency-divided clock set in the WDTCKS[3:0] bits. The number of PCLKB cycles that the counter takes to underflow after a refresh operation is determined by the combination of the WDTCKS[3:0] and WDTTOPS[1:0] bits.

For details, see section 27, Watchdog Timer (WDT).

Note 1. 空白产品中的值为FFFFFFFFh。它设置为您的应用程序写入的值。

IWDTSTRT位（IWDT启动模式选择）

IWDTSTRT位选择复位后激活IWDT的模式（停止状态或激活状态）。

IWDTTOPS[1:0]位（IWDT超时周期选择）

IWDTTOPS[1:0]位指定超时周期，即递减计数器下溢所需的时间，如IWDTCKS[3:0]位中设置的分频时钟的128、512、1024或2048个周期.刷新操作后计数器下溢的时钟周期数由IWDTCKS[3:0]和IWDTCKS[1:0]位的组合决定。

有关详细信息，请参见第28节，独立看门狗定时器(IWDT)。

IWDTCKS[3:0]位（IWDT专用时钟分频比选择）

IWDTCKS[3:0]位指定用于将IWDT的时钟频率分频为11、116、132、164、1128或1256的预分频器的分频比。将此设置与IWDTTOPS[1:0]位设置，IWDT计数周期可以设置为128到524 288个IWDT时钟周期。

有关详细信息，请参见第28节，独立看门狗定时器(IWDT)。

IWDTRPES[1:0]位（IWDT窗口结束位置选择）

IWDTRPES[1:0]位指定递减计数器窗口结束的位置为计数值的0%、25%、50%或75%。窗口结束位置的值必须小于窗口开始位置的值。否则，只有窗口起始位置的值有效。

IWDTRPSS[1:0]和IWDTRPES[1:0]位中与窗口的开始和结束位置设置相对应的计数器值随IWDTTOPS[1:0]位中的设置而变化。

有关详细信息，请参见第28节，独立看门狗定时器(IWDT)。

IWDTRPSS[1:0]位（IWDT窗口起始位置选择）

IWDTRPSS[1:0]位指定递减计数器窗口的起始位置为计数值的25%、50%、75%或100%。计数开始点为100%，下溢发生点为0%。窗口开始位置和结束位置之间的间隔成为可以刷新的时间段。在此期间之外无法刷新。

有关详细信息，请参见第28节，独立看门狗定时器(IWDT)。

IWDTRSTIRQS位（IWDT复位中断请求选择）

IWDTRSTIRQS位选择在递减计数器下溢或产生刷新错误时的操作。选择的操作可以是独立的看门狗定时器复位、不可屏蔽中断请求或中断请求。

有关详细信息，请参见第28节，独立看门狗定时器(IWDT)。

IWDTSTPCTL位（IWDT停止控制）

IWDTSTPCTL位指定在进入休眠、贪睡或软件待机模式时是否停止计数。

有关详细信息，请参见第28节，独立看门狗定时器(IWDT)。

WDTSTRT位（WDT启动模式选择）

WDTSTRT位选择复位后WDT激活的模式（停止状态或激活状态）。当WDT在自动启动模式下激活时，WDT的OFS0寄存器设置有效。

WDTOPS[1:0]位（WDT超时周期选择）

WDTTOPS[1:0]位指定超时周期，即递减计数器下溢所需的时间，如WDTCKS[3:0]位中设置的分频时钟的1024、4096、8192或16384个周期.刷新操作后计数器下溢的PCLKB周期数由WDTCKS[3:0]和WDTTOPS[1:0]位的组合决定。

有关详细信息，请参见第27节，看门狗定时器(WDT)。

WDTCKS[3:0] bits (WDT Clock Frequency Division Ratio Select)

The WDTCKS[3:0] bits specify the division ratio of the prescaler for dividing the PCLKB frequency as 1/4, 1/64, 1/128, 1/512, 1/2048, or 1/8192. Using this setting combined with the WDTTOPS[1:0] bit setting, the WDT counting period can be set from 4,096 to 134,217,728 PCLKB cycles.

For details, see section 27, Watchdog Timer (WDT).

WDTRPES[1:0] bits (WDT Window End Position Select)

The WDTRPES[1:0] bits specify the position where the window for the down counter ends as 0%, 25%, 50%, or 75% of the counted value. The value of the window end position must be smaller than the value of the window start position. Otherwise, only the value for the window start position is valid.

The counter values corresponding to the settings for the start and end positions of the window, in the WDTRPSS[1:0] and WDTRPES[1:0] bits, vary with the setting of the WDTTOPS[1:0] bits.

For details, see section 27, Watchdog Timer (WDT).

WDTRPSS[1:0] bits (WDT Window Start Position Select)

The WDTRPSS[1:0] bits specify the position where the window for the down counter starts as 25%, 50%, 75%, or 100% of the counted value. The point at which counting starts is 100% and the point at which an underflow occurs is 0%. The interval between the window start and end positions becomes the period in which a refresh is possible. Refresh is not possible outside this period.

For details, see section 27, Watchdog Timer (WDT).

WDTRSTIRQS bit (WDT Reset Interrupt Request Select)

The WDTRSTIRQS bit selects the operation on an underflow of the down counter or generation of a refresh error. The selected operation can be a watchdog timer reset, non-maskable interrupt request, or interrupt request.

For details, see section 27, Watchdog Timer (WDT).

WDTSTPCTL bit (WDT Stop Control)

The WDTSTPCTL bit specifies whether to stop counting when entering Sleep mode. For details, see section 27, Watchdog Timer (WDT).

7.2.2 Option Function Select Register 1 (OFS1)

Address(es): OFS1 0000 0404h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	User setting*1															

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	—	—	—	—	—	HOCOFRQ0[1:0]		HOCOEN	—	—	—	—	—	LVDAS	VDSEL0[1:0]	
	User setting*1															

Bit	Symbol	Bit name	Description	R/W
b1, b0	VDSEL0[1:0]	Voltage Detection 0 Level Select	b1 b0 0 0: Setting prohibited 0 1: Select 2.94 V 1 0: Select 2.87 V 1 1: Select 2.80 V.	R
b2	LVDAS	Voltage Detection 0 Circuit Start	0: Enable voltage monitor 0 reset after a reset 1: Disable voltage monitor 0 reset after a reset.	R
b7 to b3	—	Reserved	When read, these bits return the written value. The write value should be 1.	R

WDTCKS[3:0]位（WDT时钟分频比选择）

WDTCKS[3:0]位指定用于将PCLKB频率分频为14、164、1128、1512、12048或18192的预分频器的分频比。将此设置与WDTTOPS[1结合使用：0]位设置，WDT计数周期可设置为4 096至134 217 728个PCLKB周期。

有关详细信息，请参见第27节，看门狗定时器(WDT)。

WDTRPES[1:0]位（WDT窗口结束位置选择）

WDTRPES[1:0]位指定递减计数器窗口结束的位置为计数值的0%、25%、50%或75%。窗口结束位置的值必须小于窗口开始位置的值。否则，只有窗口起始位置的值有效。

WDTRPSS[1:0]和WDTRPES[1:0]位中与窗口开始和结束位置设置相对应的计数器值随WDTTOPS[1:0]位的设置而变化。

有关详细信息，请参见第27节，看门狗定时器(WDT)。

WDTRPSS[1:0]位（WDT窗口起始位置选择）

WDTRPSS[1:0]位指定递减计数器窗口的起始位置为计数值的25%、50%、75%或100%。计数开始点为100%，下溢发生点为0%。窗口开始位置和结束位置之间的间隔成为可以刷新的时间段。在此期间之外无法刷新。

有关详细信息，请参见第27节，看门狗定时器(WDT)。

WDTRSTIRQS位（WDT复位中断请求选择）

WDTRSTIRQS位选择在递减计数器下溢或产生刷新错误时的操作。所选操作可以是看门狗定时器复位、不可屏蔽中断请求或中断请求。

有关详细信息，请参见第27节，看门狗定时器(WDT)。

WDTSTPCTL位（WDT停止控制）

WDTSTPCTL位指定进入休眠模式时是否停止计数。有关详细信息，请参阅第27节，看门狗定时器（WDT）。

7.2.2 选项功能选择寄存器1(OFS1)

Address(es): OFS1 0000 0404h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值：	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
	用户设置*1															

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	—	—	—	—	—	HOCOFRQ0[1:0]		HOCOEN	—	—	—	—	—	LVDAS	VDSEL0[1:0]	
	用户设置*1															

Bit	Symbol	位名称	Description	R/W
b1, b0	VDSEL0[1:0]	电压检测0级别选择	b1b000：禁止设置01：选择2.94V10：选择2.87V11：选择2.80V。	R
b2	LVDAS	电压检测0电路启动	0：启用电压监控器0复位后复位1：禁用电压监控器0复位后复位。	R
b7 to b3	—	Reserved	读取时，这些位返回写入的值。写入值应为1。	R

Bit	Symbol	Bit name	Description	R/W
b8	HOCOEN	HOCO Oscillation Enable	0: Enable HOCO oscillation after a reset 1: Disable HOCO oscillation after a reset.	R
b10, b9	HOCOFRQ0[1:0]	HOCO Frequency Setting 0	b10 b9 0 0: 16 MHz 0 1: 18 MHz 1 0: 20 MHz 1 1: Setting prohibited.	R
b31 to b11	—	Reserved	When read, these bits return the written value. The write value should be 1.	R

Note 1. The value in a blank product is FFFF FFFFh. It is set to the value written by your application.

VDSEL0[1:0] bits (Voltage Detection 0 Level Select)

The VDSEL0[1:0] bits select the voltage detection level of the voltage detection 0 circuit.

LVDAS bit (Voltage Detection 0 Circuit Start)

The LVDAS bit selects whether the voltage monitor 0 reset is enabled or disabled after a reset.

HOCOEN bit (HOCO Oscillation Enable)

The HOCOEN bit selects whether the HOCO oscillation is enable or disable after a reset. Setting this bit to 0 allows the HOCO oscillation to start before the CPU starts operation, which reduces the wait time for oscillation stabilization.

Note: When the HOCOEN bit is set to 0, the system clock source is not switched to HOCO. The system clock source is only switched to HOCO by setting the clock source select bits (SCKSCR.CKSEL[2:0]). If you use the HOCO clock, you must set the OFS1.HOCOFRQ0[1:0] bits to an optimum value.

HOCOFRQ0[1:0] bits (HOCO Frequency Setting 0)

The HOCOFRQ0[1:0] bits specify the HOCO frequency after a reset as 16, 18, or 20 MHz.

7.2.3 Access Window Setting Register (AWS)

Address(es): AWS 0100 A164h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	BTFLG	—	—	—	—	FAWE[10:0]										
Value after reset:						User setting										

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	FSPR	—	—	—	—	FAWS[10:0]										
Value after reset:						User setting										

Bit	Symbol	Bit name	Description	R/W
b10 to b0	FAWS[10:0]	Access Window Start Block Address	These bits specify the start block address for the access window. They do not represent the block number of the access window. The access window is only valid in the program flash area. The block address specifies the first address of the block and consists of address bits [23:13].	R
b14 to b11	—	Reserved	When read, these bits return the written value. The write value should be 1.	R

Bit	Symbol	位名称	Description	R/W
b8	HOCOEN	HOCO Oscillation Enable	0：复位后启用HOCO振荡1：复位后禁用HOCO振荡。	R
b10, b9	HOCOFRQ0[1:0]	HOCO Frequency Setting 0	b10b900：16MHz01：18MHz10：20MHz11：禁止设置。	R
b31 to b11	—	Reserved	读取时，这些位返回写入的值。写入值应为1。	R

Note 1. 空白产品中的值为FFFFFFFFh。它设置为您的应用程序写入的值。

VDSEL0[1:0]位（电压检测0电平选择）

VDSEL0[1:0]位选择电压检测0电路的电压检测电平。

LVDAS位（电压检测0电路启动）

LVDAS位选择在复位后是启用还是禁用电压监视器0复位。

HOCOEN位（HOCO振荡使能）

HOCOEN位选择在复位后是启用还是禁用HOCO振荡。将此位设置为0允许在CPU开始运行之前启动HOCO振荡，减少了振荡稳定的等待时间。

Note: 当HOCOEN位设置为0时，系统时钟源不切换到HOCO。系统时钟源只能通过设置时钟源选择位(SCKSCR.CKSEL[2:0])切换到HOCO。如果使用HOCO时钟，则必须将OFS1.HOCOFRQ0[1:0]位设置为最佳值。

HOCOFRQ0[1:0]位（HOCO频率设置0）

HOCOFRQ0[1:0]位指定复位后的HOCO频率为16、18或20MHz。

7.2.3 访问窗口设置寄存器(AWS)

Address(es): AWS 0100 A164h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	BTFLG	—	—	—	—	FAWE[10:0]										
重置后的值：						用户设置										

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	FSPR	—	—	—	—	FAWS[10:0]										
重置后的值：						用户设置										

Bit	Symbol	位名称	Description	R/W
b10 to b0	FAWS[10:0]	访问窗口启动块 Address	这些位指定访问窗口的起始块地址。它们不代表访问窗口的块号。访问窗口仅在程序闪存区有效。块地址指定块的第一个地址，由地址位[23:13]组成。	R
b14 to b11	—	Reserved	读取时，这些位返回写入的值。写入值应为1。	R

Bit	Symbol	Bit name	Description	R/W
b15	FSPR	Protection of Access Window and Startup Area Select Function	This bit controls programming of the program/erase protection for the access window, the Startup Area Select flag (AWS.BTFLG), and the temporary boot swap. Once this bit is set to 0, it is impossible to change this bit to 1. 0: Executing the configuration setting command for programming the access window (FAWE[10:0], FAWS[10:0]) and the Startup Area Select flag (AWS.BTFLG) is invalid 1: Executing the configuration setting command for programming the access window (FAWE[10:0], FAWS[10:0]) and the Startup Area Select flag (AWS.BTFLG) is valid.	R
b26 to b16	FAWE[10:0]	Access Window End Block Address	These bits specify the end block address for the access window. They do not represent the block number of the access window. The access window is only valid in the program flash area. The end block address for the access window is the next block to the region acceptable for programming and erasure defined by the access window. The block address specifies the first address of the block and consists of the address bits [23:13].	R
b30 to b27	—	Reserved	When read, these bits return the written value. The write value should be 1.	R
b31	BTFLG	Startup Area Select Flag	This bit specifies whether the address of the startup area is exchanged for the boot swap function or not: 0: Exchange the first 8-KB area (0000 0000h to 0000 1FFFh) and second 8-KB area (0000 2000h to 0000 3FFFh) 1: Do not exchange the first 8-KB area (0000 0000h to 0000 1FFFh) and second 8-KB area (0000 2000h to 0000 3FFFh).	R

Issuing the program or erase (P/E) command to the area outside the access window causes a command-locked state. The access window is only valid in the program flash area. The access window provides protection in self-programming mode, serial programming mode, and on-chip debug mode. The access window can be locked by the FSPR bit.

The access window is specified in FAWS[10:0] and FAWE[10:0]:

- FAWE[10:0] = FAWS[10:0]: The P/E command is allowed to execute in the full program flash area
- FAWE[10:0] > FAWS[10:0]: The P/E command is only allowed to execute into the window from the block pointed to by the FAWS bits to the block one lower than the block pointed to by the FAWE bits
- FAWE[10:0] < FAWS[10:0]: The P/E command is not allowed to execute in the program flash area.

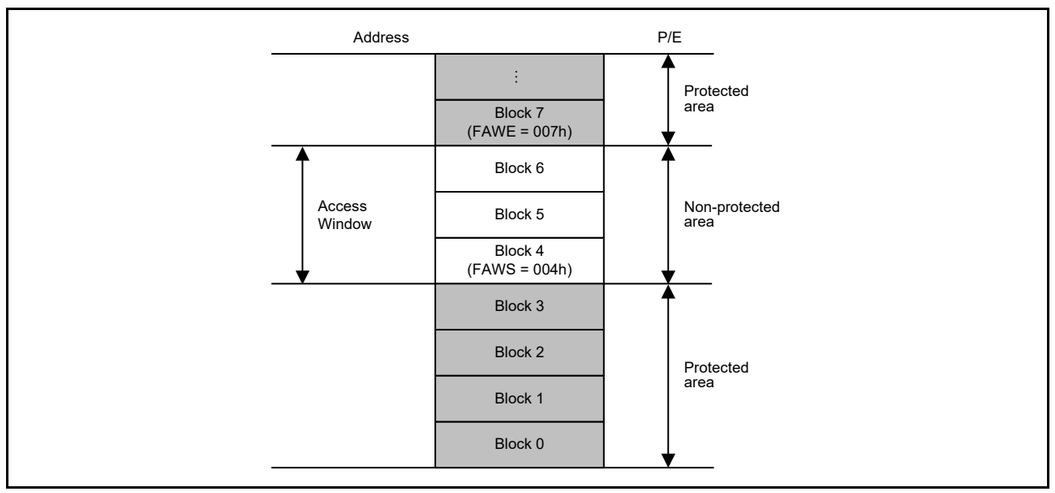


Figure 7.2 Access window overview

Bit	Symbol	位名称	Description	R/W
b15	FSPR	访问保护 窗口和启动区 选择功能	该位控制访问窗口、启动区域选择标志(AWS.BTFLG)和临时引导交换的程序擦除保护的编程。一旦该位设置为0，则无法将该位更改为1。0：执行用于编程访问窗口（FAWE[10:0]、FAWS[10:0]）和启动区域选择的配置设置命令flag(AWS.BTFLG)无效1：执行访问窗口编程的配置设置命令（FAWE[10:0]、FAWS[10:0]）和启动区域选择标志（AWS.BTFLG）有效。	R
b26 to b16	FAWE[10:0]	访问窗口结束块 Address	这些位指定访问窗口的结束块地址。它们不代表访问窗口的块号。访问窗口仅在程序闪存区有效。访问窗口的结束块地址是访问窗口定义的可用于编程和擦除的区域的下一个块。块地址指定块的第一个地址，由地址位[23:13]组成。	R
b30 to b27	—	Reserved	读取时，这些位返回写入的值。写入值应为1。	R
b31	BTFLG	启动区选择标志	该位指定启动区域的地址是否交换用于引导交换功能：0：交换第一个8-KB区域（00000000h到00001FFFh）和第二个8-KB区域（00002000h到00003FFFh）1:不要交换第一个8-KB区域（00000000h到00001FFFh）和第二个8-KB区域（00002000h到00003FFFh）。	R

向访问窗口外的区域发出编程或擦除(PE)命令会导致命令锁定状态。访问窗口仅在程序闪存区有效。访问窗口在自编程模式、串行编程模式和片上调试模式下提供保护。访问窗口可以通过FSPR位锁定。

访问窗口在FAWS[10:0]和FAWE[10:0]中指定：

- FAWE[10:0]=FAWS[10:0]：允许PE命令在整个程序flash区执行
- FAWE[10:0]>FAWS[10:0]：PE命令只允许从FAWS位指向的块到比FAWE位指向的块低一级的窗口执行
- FAWE[10:0]<FAWS[10:0]：不允许在程序闪存区执行PE命令。

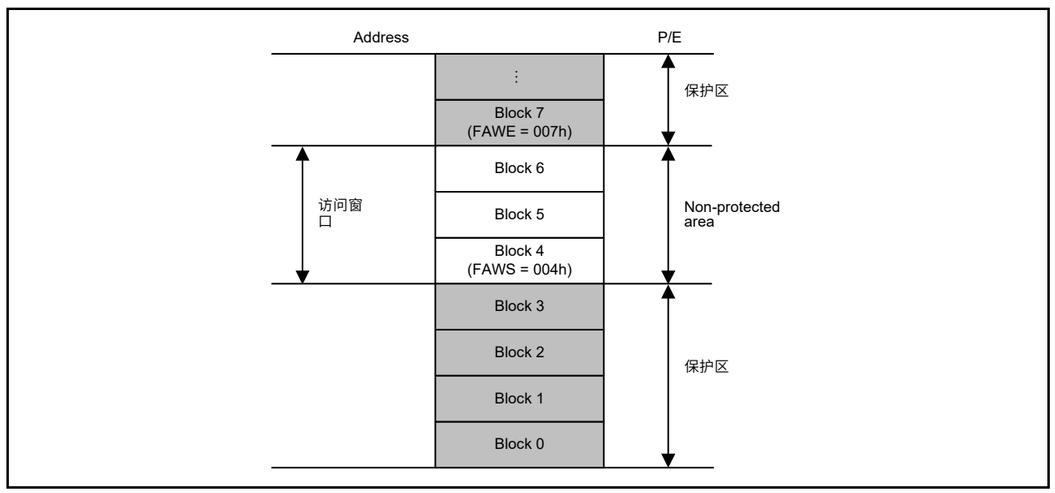


Figure 7.2 访问窗口概述

7.2.4 OCD/Serial Programmer ID Setting Register (OSIS)

The OSIS register stores the ID for ID code protection of the OCD/serial programmer. When connecting the OCD/serial programmer, write values so that the MCU can determine whether to permit the connection. Use this register to check whether a code transmitted from the OCD/serial programmer matches the ID code in the option-setting memory.

When the ID codes match, connection of the OCD/serial programmer is permitted. If the ID codes do not match, connection with the OCD/serial programmer is not possible. The OSIS register must be set in 32-bit units.

Address(es): OSIS 0100 A150h, OSIS 0100 A154h, OSIS 0100 A158h, OSIS 0100 A15Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:									User setting							

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:									User setting							

These fields hold the ID for use in ID authentication for the OCD/serial programmer.

ID code bits [127] and [126] determine whether ID code protection is enabled and the method of authentication to use with the host. Table 7.1 shows how ID code determines the method of authentication.

Table 7.1 Specifications for ID code protection

Operating mode on boot up	ID code	State of protection	Operations on connection to programmer or on-chip debugger
Serial programming mode (SCI/USB boot mode) On-chip debug mode (JTAG/SWD boot mode)	FFh, …, FFh (all bytes are FFh)	Protection disabled	The ID code is not checked, ID code always matches, and connection to programmer or on-chip debugger is permitted
	Bit [127] = 1 and [126] = 1, and at least one of the 16 bytes is not FFh.	Protection enabled	Matching ID code = Authentication is complete and connection with the programmer or the on-chip debugger is permitted. Non-matching ID code = Transition to the ID code protection wait state. When the ID code sent from the programmer or the on-chip debugger is ALeRASE in ASCII code (414C_6552_4153_45FF_FFFF_FFFF_FFFF_FFFFh), the contents of the user flash (code and data) area, and the configuration area are erased. However, forced erasure is not executed when the FSPR bit is 0.
	Bit [127] = 1 and bit [126] = 0	Protection enabled	Matching ID code = Authentication is complete and connection with the programmer or the on-chip debugger is permitted. Non-matching ID code = Transition to the ID code protection wait state.
	Bit [127] = 0	Protection enabled	The ID code is not checked, the ID code is always non-matching, and connection to the programmer or the on-chip debugger is prohibited

7.3 Setting the Option-Setting Memory

7.3.1 Allocation of Data in the Option-Setting Memory

Data for programming in the option-setting memory should be allocated to the addresses shown in Figure 7.1. The allocation of data is for use by tools such as a flash programming software or an on-chip debugger.

Note: Programming formats vary depending on the compiler. See the compiler manual for details.

7.2.4 OCD串行编程器ID设置寄存器(OSIS)

OSIS寄存器存储用于保护OCD串行编程器的ID代码的ID。连接OCD串口编程器时，写入数值，让MCU判断是否允许连接。使用该寄存器检查从OCD串行编程器发送的代码是否与选项设置存储器中的ID代码匹配。

当ID代码匹配时，允许连接OCD串行编程器。如果ID代码不匹配，则无法与OCD串行编程器连接。OSIS寄存器必须以32位为单位进行设置。

Address(es): OSIS 0100 A150h, OSIS 0100 A154h, OSIS 0100 A158h, OSIS 0100 A15Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值：									用户设置							

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：									用户设置							

这些字段保存用于OCD串行编程器身份验证的ID。

ID代码位[127]和[126]确定是否启用ID代码保护以及与主机一起使用的身份验证方法。表7.1显示了ID代码如何确定身份验证方法。

Table 7.1 ID码保护规范

启动时的操作模式	身份证号码	保护状态	连接到编程器或片上调试器的操作
串行编程模式（SCIUSB启动模式） 片上调试模式（JTAGSWD启动模式）	FFh … FFh（所有字节均为FFh）	保护已禁用	ID码不检查，ID码始终匹配，允许连接编程器或片上调试器
	位[127]=1且[126]=1，且16个字节中至少有一个不是FFh。	启用保护	匹配ID代码=验证完成，允许与编程器或片上调试器连接。ID代码不匹配=转换到ID代码保护等待状态。当编程器或片上调试器发送的ID码为ASCII码（414C_6552_4153_45FF_FFFF_FFFF_FFFF_FFFFh）的ALeRASE时，用户闪存（代码和数据）区和配置区的内容被擦除。然而，强制擦除不执行时 FSPR位为0。
	位[127]=1和位[126]=0	启用保护	匹配ID代码=验证完成，允许与编程器或片上调试器连接。ID代码不匹配=转换到ID代码保护等待状态。
	Bit [127] = 0	启用保护	ID码不校验，ID码始终不匹配，禁止连接编程器或片上调试器

7.3 设置选项设置内存

7.3.1 选项设置存储器中的数据分配

用于在选项设置存储器中编程的数据应分配到图7.1所示的地址。数据分配供闪存编程软件或片上调试器等工具使用。

Note: 编程格式因编译器而异。有关详细信息，请参阅编译器手册。

7.3.2 Setting Data for Programming the Option-Setting Memory

Allocating data as described in section 7.3.1, Allocation of Data in the Option-Setting Memory does not alone result in the data being written to the option-setting memory. You must also follow one of the actions described in this section.

(1) Changing the option-setting memory by self-programming

To write data to the program flash area, use the programming command. To write data to the option-setting memory in the configuration setting area, use the configuration setting command. In addition, use startup area select function to safely update the boot program that includes the option-setting memory.

For details on the programming command, the configuration setting command, and the startup area select function, see section 55, Flash Memory.

Note: While programming the configuration setting area, the following restrictions apply:

- The code must not access addresses that satisfy the ranges described by the expression defined in Expression 1 from all bus masters
- The code must not execute on addresses that satisfy the ranges described by the expression defined in Expression 1.

Expression 1

If (((address & 0x0101F800) = = 0x01010000) || ((address & 0x0101FC00) = = 0x01012000))

For example, the ranges of addresses 0x1FFF0000 to 0x1FFF07FF or 0x1FFF2000 to 0x1FFF23FF are associated with the SRAMHS area that is tagged as restricted. Also, interrupts are allowed, however, the ISR has these specified restrictions. Therefore, it is highly recommended that you disable all interrupts, and bus masters except the CPU while programming the configuration setting area because the interrupts and these modules might access prohibited area in Expression 1.

(2) Debugging through an OCD or programming by a flash writer

This procedure depends on the tool in use, so refer to the tool manual for details. There are two setting procedures:

- Read the data, allocated as described in section 7.3.1, Allocation of Data in the Option-Setting Memory, from an object file or Motorola S-format file generated by the compiler, and write the data to the MCU
- Use the GUI interface of the tool to program the same data, allocated as described in section 7.3.1, Allocation of Data in the Option-Setting Memory.

Note: While programming the OSIS or AWS registers, the following restrictions apply:

- The code must not access addresses that satisfy the ranges described by the expression defined in Expression 1 from all bus masters
- The code must not execute on addresses that satisfy the ranges described by the expression defined in Expression 1.

7.4 Usage Notes

7.4.1 Data for Programming Reserved Areas and Reserved Bits in the Option-Setting Memory

When reserved areas and reserved bits in the option-setting memory are within the scope of programming, write 1 to all bits in reserved areas and all reserved bits. Operation is not guaranteed if 0 is written to these bits.

7.3.2 用于编程选项设置存储器的设置数据

如第7.3.1节所述分配数据，在选项设置存储器中分配数据并不单独导致数据被写入选项设置存储器。您还必须遵循本节中描述的操作之一。

(1) 通过自编程更改选项设置存储器

要将数据写入程序闪存区域，请使用编程命令。要将数据写入配置设置区域中的选项设置存储器，请使用配置设置命令。此外，使用启动区域选择功能可以安全地更新包含选项设置内存的引导程序。

有关编程命令、配置设置命令和启动区域选择功能的详细信息，请参见第55节，闪存。

Note: 在对配置设置区域进行编程时，有以下限制：

- 代码不得从所有总线主机访问满足表达式1中定义的表达式所描述范围的地址
- 代码不得在满足表达式1中定义的表达式描述的范围的地址上执行。

Expression 1

If (((address & 0x0101F800) = = 0x01010000) || ((address & 0x0101FC00) = = 0x01012000))

例如，地址范围0x1FFF0000到0x1FFF07FF或0x1FFF2000到0x1FFF23FF与标记为受限的SRAMHS区域相关联。此外，允许中断，但是，ISR有这些指定的限制。因此，强烈建议您在对配置设置区域进行编程时禁用除CPU之外的所有中断和总线主控，因为中断和这些模块可能会访问表达式1中的禁止区域。

(2) 通过OCD进行调试或通过闪存写入器进行编程

此过程取决于所使用的工具，因此请参阅工具手册了解详细信息。设置过程有两种：

- 从编译器生成的目标文件或MotorolaS格式文件中读取如第7.3.1节“选项设置内存中的数据分配”中所述分配的数据，并将数据写入MCU
- 使用工具的GUI界面对相同的数据进行编程，如第7.3.1节所述分配选项设置内存中的数据。

Note: 在对OSIS或AWS寄存器进行编程时，适用以下限制：

- 代码不得从所有总线主机访问满足表达式1中定义的表达式所描述范围的地址
- 代码不得在满足表达式1中定义的表达式描述的范围的地址上执行。

7.4 使用说明

7.4.1 用于编程选项设置中的保留区域和保留位的数据 Memory

当期权设置内存中的保留区域和保留位在编程范围内，请在保留区域和所有保留位中写入1个。如果将0写入这些位，则无法保证操作。

8. Low Voltage Detection (LVD)

8.1 Overview

The Low Voltage Detection (LVD) module monitors the voltage level input to the VCC pin, and the detection level can be selected using a software program. The LVD module consists of three separate voltage level detectors, 0, 1, and 2, which measure the voltage level input to the VCC pin. LVD voltage detection registers allow your application to configure detection of VCC changes at various voltage thresholds.

Each voltage level detector has a voltage monitor associated with it, for example voltage monitors 0, 1, and 2. Voltage monitor registers are used to configure the LVD to trigger an interrupt, event link output, or reset when the thresholds are crossed.

Table 8.1 lists the LVD specifications. Figure 8.1 shows a block diagram of voltage detectors 0, 1, and 2, Figure 8.2 shows a block diagram of the voltage monitor 1 interrupt and reset circuit, and Figure 8.3 shows a block diagram of the voltage monitor 2 interrupt and reset circuit.

Table 8.1 LVD specifications

Parameter		Voltage monitor 0	Voltage monitor 1	Voltage monitor 2
VCC monitoring	Monitored voltage	V_{det0}	V_{det1}	V_{det2}
	Detected event	Voltage falls past V_{det0}	Voltage rises or falls past V_{det1}	Voltage rises or falls past V_{det2}
	Detection voltage	Selectable from three different levels in the OFS1.VDSEL0[1:0] bits	Selectable from three different levels in the LVDLVLR.LVD1LVL[4:0] bits	Selectable from three different levels in the LVDLVLR.LVD2LVL[2:0] bits
	Monitor flag	None	LVD1SR.MON flag: Monitors whether voltage is higher or lower than V_{det1}	LVD2SR.MON flag: Monitors whether voltage is higher or lower than V_{det2}
			LVD1SR.DET flag: V_{det1} passage detection	LVD2SR.DET flag: V_{det2} passage detection
Process on voltage detection	Reset	Voltage monitor 0 reset	Voltage monitor 1 reset	Voltage monitor 2 reset
		Reset when V_{det0} > VCC CPU restart after specified time with VCC > V_{det0}	Reset when V_{det1} > VCC CPU restart timing selectable: after specified time with VCC > V_{det1} or V_{det1} > VCC	Reset when V_{det2} > VCC CPU restart timing selectable: after specified time with VCC > V_{det2} or V_{det2} > VCC
	Interrupt	No interrupt	Voltage monitor 1 interrupt	Voltage monitor 2 interrupt
			Non-maskable or maskable interrupt selectable	Non-maskable or maskable interrupt selectable
			Interrupt request issued when V_{det1} > VCC or VCC > V_{det1}	Interrupt request issued when V_{det2} > VCC or VCC > V_{det2}
Digital filter	Enable/ Disable switching	Digital filter function not available	Available	Available
	Sampling time	—	1/n LOCO frequency × 2 (n: 2, 4, 8, 16)	1/n LOCO frequency × 2 (n: 2, 4, 8, 16)
Event linking		None	Available Output of event signals on detection of V_{det1} crossings	Available Output of event signals on detection of V_{det2} crossings

8. 低电压检测(LVD)

8.1 Overview

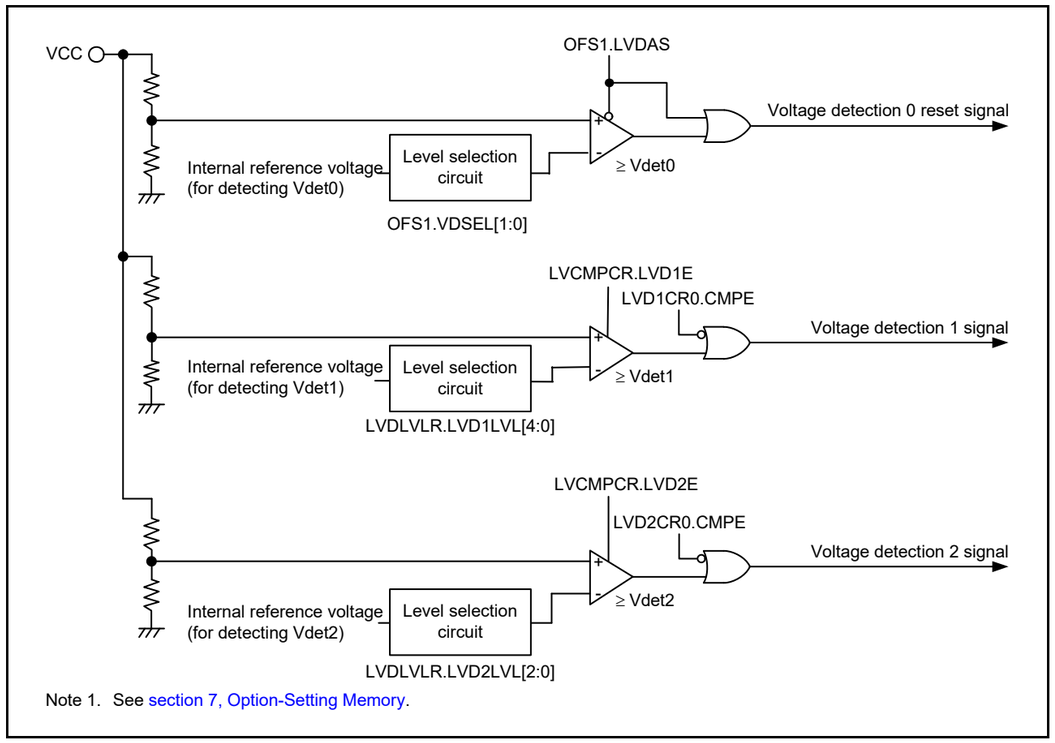
低电压检测(LVD)模块监控输入到VCC引脚的电压电平，并且可以使用软件程序选择检测电平。LVD模块由三个独立的电压电平检测器0、1和2组成，它们测量输入到VCC引脚的电压电平。LVD电压检测寄存器允许您的应用程序配置在各种电压阈值下检测VCC变化。

每个电压电平检测器都有一个与之关联的电压监视器，例如电压监视器0、1和2。电压监视器寄存器用于配置LVD，以在超过阈值时触发中断、事件链接输出或复位。

表8.1列出了LVD规格。图8.1显示了电压检测器0、1和2的框图，图8.2显示了电压监测器1中断和复位电路的框图，图8.3显示了电压监测器2中断和复位电路的框图。

Table 8.1 LVD specifications

Parameter		电压监视器0	电压监视器1	电压监测器2
VCC monitoring	监控电压	V_{det0}	V_{det1}	V_{det2}
	检测到的事件	电压下降超过Vdet0	电压上升或下降超过Vdet1	电压上升或下降超过Vdet2
	检测电压	可从OFS1.VDSEL0[1:0]位的三个不同级别中选择	可从LVDLVLR.LVD1LVL[4:0]位的三个不同级别中选择	可从LVDLVLR.LVD2LVL[2:0]位的三个不同级别中选择
	监控标志	None	LVD1SR.MON标志：监控电压是高于还是低于Vdet1	LVD2SR.MON标志：监控电压是高于还是低于Vdet2
			LVD1SR.DET标志：Vdet1通过检测	LVD2SR.DET标志：Vdet2通过检测
电压检测流程	Reset	电压监控器0复位	电压监视器1复位	电压监视器2复位
		当Vdet0>VCC时复位 CPU在VCC>Vdet0指定时间后重启	当Vdet1>VCC时复位 CPU重启时间可选：在VCC>Vdet1或Vdet1>VCC的指定时间后	当Vdet2>VCC时复位 CPU重启时间可选：在VCC>Vdet2或Vdet2>VCC的指定时间后
	Interrupt	无中断	电压监视器1中断	电压监视器2中断
			可选择不可屏蔽或可屏蔽中断	可选择不可屏蔽或可屏蔽中断
			中断请求发出时 V_{det1} > VCC or VCC > V_{det1}	中断请求发出时 V_{det2} > VCC or VCC > V_{det2}
数字滤波器	启用禁用切换	数字滤波器功能不可用	Available	Available
	采样时间	—	1nLOCO频率 2(n:2 4 8 16)	1nLOCO频率 2(n:2 4 8 16)
事件链接		None	Available 在检测到Vdet1交叉点时输出事件信号	Available 在检测到Vdet2交叉点时输出事件信号



Note 1. See section 7, Option-Setting Memory.

Figure 8.1 Voltage detection 0, 1, and 2 block diagram

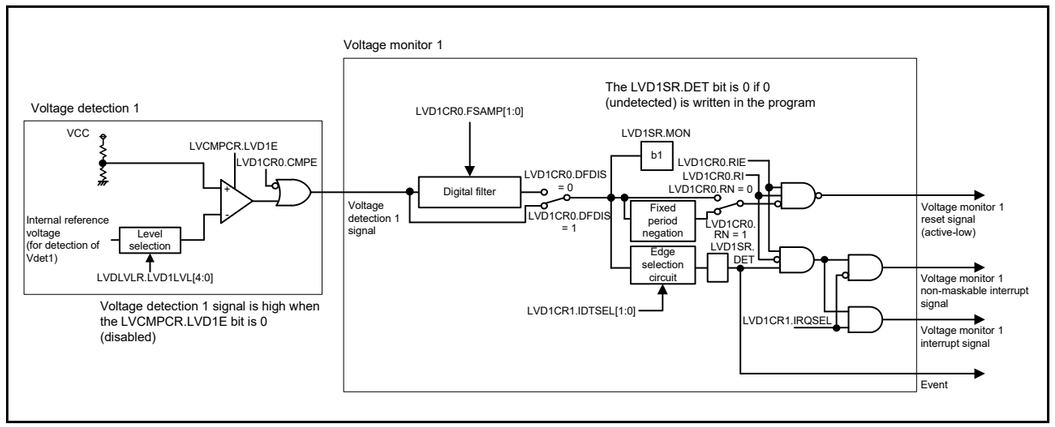
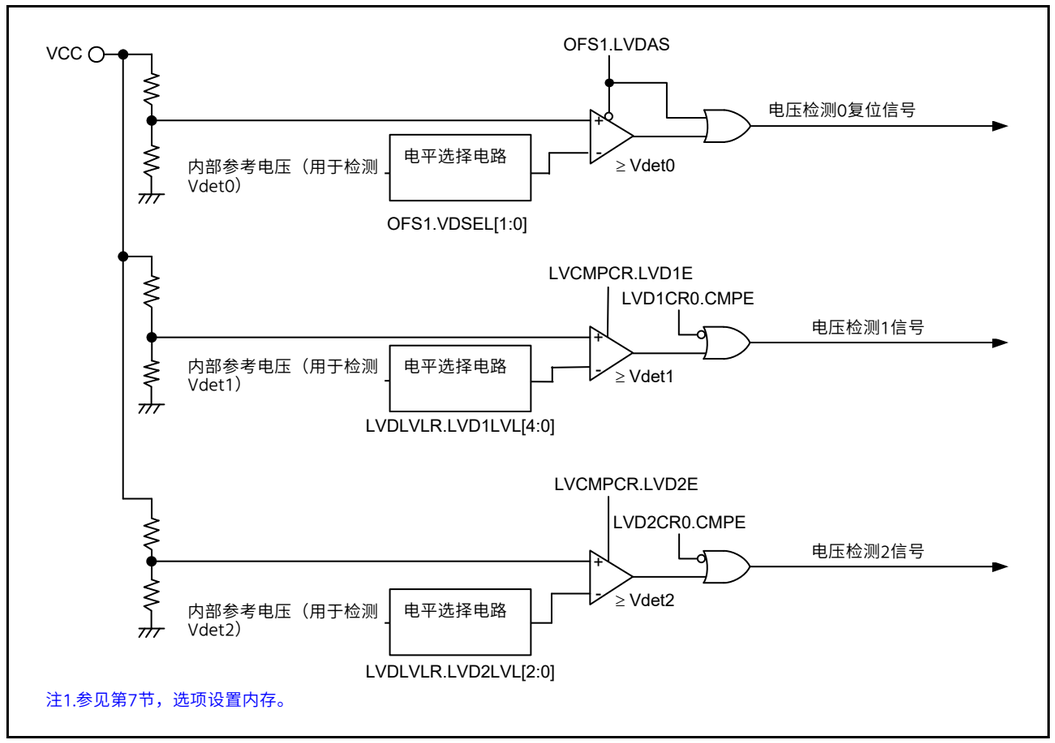


Figure 8.2 Voltage monitor 1 interrupt/reset circuit block diagram



注1.参见第7节，选项设置内存。

Figure 8.1 电压检测0、1和2框图

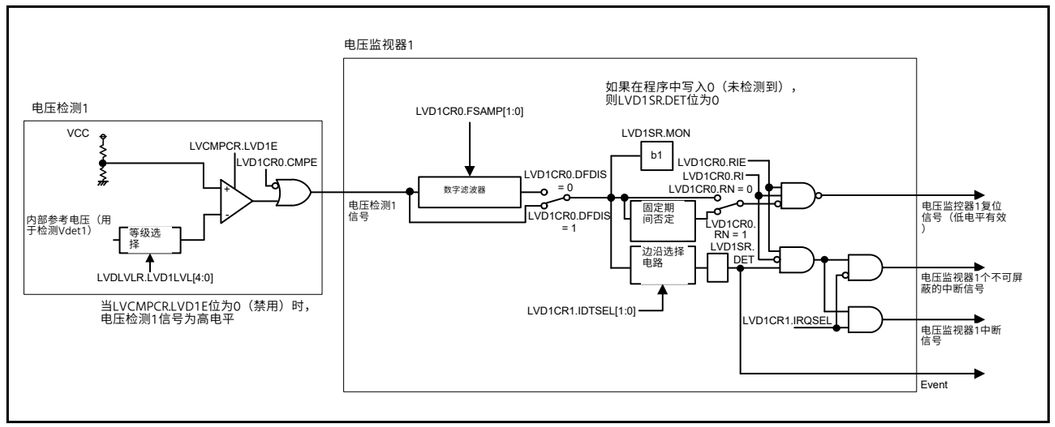


Figure 8.2 电压监视器1中断复位电路框图

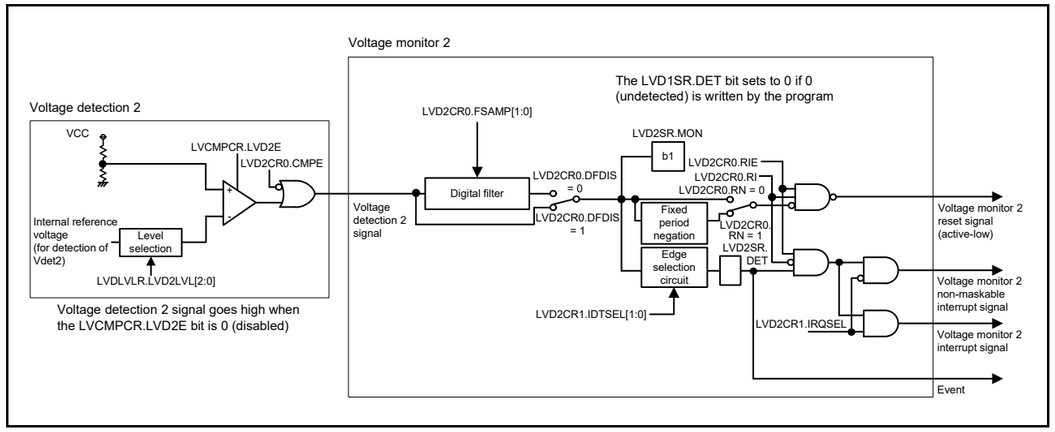


Figure 8.3 Voltage monitor 2 interrupt/reset circuit block diagram

8.2 Register Descriptions

8.2.1 Voltage Monitor 1 Circuit Control Register 1 (LVD1CR1)

Address(es): SYSTEM.LVD1CR1 4001 E0E0h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	IRQSEL	IDTSEL[1:0]	
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Bit name	Description	R/W
b1, b0	IDTSEL[1:0]	Voltage Monitor 1 Interrupt Generation Condition Select	b1 b0 0 0: When VCC ≥ V_{det1} (rise) is detected 0 1: When VCC < V_{det1} (fall) is detected 1 0: When fall and rise are detected 1 1: Settings prohibited.	R/W
b2	IRQSEL	Voltage Monitor 1 Interrupt Type Select	0: Non-maskable interrupt 1: Maskable interrupt.*1	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.
Note 1. When enabling maskable interrupts, do not change the value of the NMIER.LVD1EN bit in the ICU from the reset state.

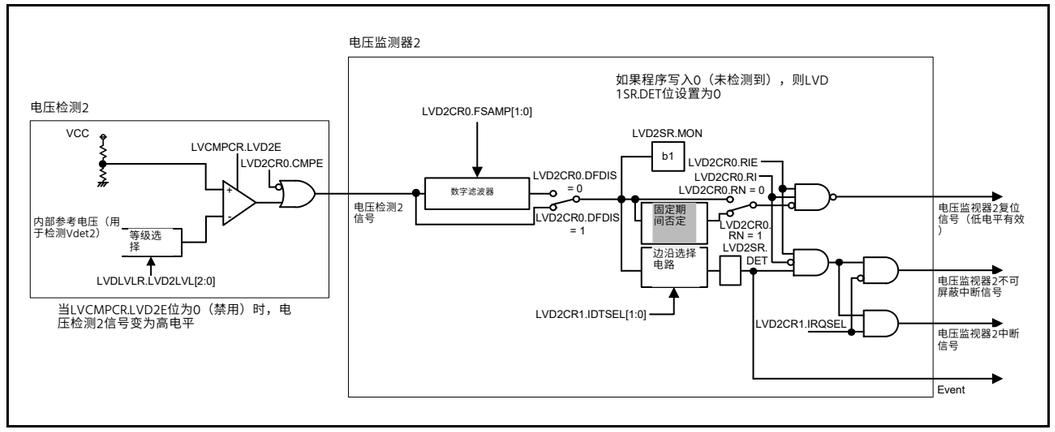


Figure 8.3 电压监测器2中断复位电路框图

8.2 注册说明

8.2.1 电压监视器1电路控制寄存器1(LVD1CR1)

Address(es): SYSTEM.LVD1CR1 4001 E0E0h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	IRQSEL	IDTSEL[1:0]	
重置后的值:	0	0	0	0	0	0	0	1

Bit	Symbol	位名称	Description	R/W
b1, b0	IDTSEL[1:0]	电压监视器1中断发生条件选择	b1b000：检测到VCC Vdet1（上升）时01：检测到VCC<Vdet1（下降）时10：检测到下降和上升时11：禁止设置。	R/W
b2	IRQSEL	电压监视器1中断类型 Select	0: Non-maskable interrupt 1: Maskable interrupt.*1	R/W
b7 to b3	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note: 在重写该寄存器之前将PRCR.PRC3位设置为1（允许写入）。
Note 1. 当启用可屏蔽中断时，不要从复位状态更改ICU中NMIER.LVD1EN位的值。

8.2.2 Voltage Monitor 1 Circuit Status Register (LVD1SR)

Address(es): SYSTEM.LVD1SR 4001 E0E1h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	MON	DET
Value after reset:	0	0	0	0	0	0	1	0

Bit	Symbol	Bit name	Description	R/W
b0	DET	Voltage Monitor 1 Voltage Change Detection Flag	0: Not detected 1: V_{det1} passage detected.	R(/W) *1
b1	MON	Voltage Monitor 1 Signal Monitor Flag	0: VCC < V_{det1} 1: VCC ≥ V_{det1} or MON is disabled.	R
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Only 0 can be written to this bit. After writing 0 to this bit, 2 system clock cycles are required for the bit to be read as 0.

DET flag (Voltage Monitor 1 Voltage Change Detection Flag)

The DET flag is enabled when the LVCMPCR.LVD1E bit is 1 (voltage detection 1 circuit enabled) and the LVD1CR0.CMPE bit is 1 (voltage monitor 1 circuit comparison result output enabled).

Set the DET flag to 0 after LVD1CR0.RIE is set to 0 (disabled). LVD1CR0.RIE can be set to 1 (enabled) after 2 or more PCLKB cycles have elapsed.

MON flag (Voltage Monitor 1 Signal Monitor Flag)

The MON flag is enabled when the LVCMPCR.LVD1E bit is 1 (voltage detection 1 circuit enabled) and the LVD1CR0.CMPE bit is 1 (voltage monitor 1 circuit comparison result output enabled).

Note: Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.

8.2.3 Voltage Monitor 2 Circuit Control Register 1 (LVD2CR1)

Address(es): SYSTEM.LVD2CR1 4001 E0E2h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	IRQSEL	IDTSEL[1:0]	
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Bit name	Description	R/W
b1, b0	IDTSEL[1:0]	Voltage Monitor 2 Interrupt Generation Condition Select	b1 b0 0 0: When VCC ≥ V_{det2} (rise) is detected 0 1: When VCC < V_{det2} (fall) is detected 1 0: When fall and rise are detected 1 1: Settings prohibited.	R/W
b2	IRQSEL	Voltage Monitor 2 Interrupt Type Select	0: Non-maskable interrupt 1: Maskable interrupt.*1	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.
Note 1. When enabling maskable interrupts, do not change the value of the NMIER.LVD1EN bit in the ICU from the reset state.

8.2.2 电压监视器1电路状态寄存器(LVD1SR)

Address(es): SYSTEM.LVD1SR 4001 E0E1h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	MON	DET
重置后的值:	0	0	0	0	0	0	1	0

Bit	Symbol	位名称	Description	R/W
b0	DET	电压监视器1电压变化检测标志	0：未检测到1：检测到Vdet1通过。	R(/W) *1
b1	MON	电压监视器1信号监视器标志	0：VCC<Vdet11：VCC Vdet1或MON被禁用。	R
b7 to b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 该位只能写入0。向该位写入0后，需要2个系统时钟周期才能将该位读为0。

DET标志（电压监视器1电压变化检测标志）

当LVCMPCR.LVD1E位为1（使能电压检测1电路）且LVD1CR0.CMPE位为1（电压监视器1电路比较结果输出使能）。

在LVD1CR0.RIE设置为0（禁用）后，将DET标志设置为0。LVD1CR0.RIE可以在2或更多之后设置为1（启用）PCLKB周期已经过去。

MON标志（电压监视器1信号监视器标志）

当LVCMPCR.LVD1E位为1（使能电压检测1电路）且LVD1CR0.CMPE位为1（电压监视器1电路比较结果输出使能）。

Note: 在重写该寄存器之前将PRCR.PRC3位设置为1（允许写入）。

8.2.3 电压监视器2电路控制寄存器1(LVD2CR1)

Address(es): SYSTEM.LVD2CR1 4001 E0E2h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	IRQSEL	IDTSEL[1:0]	
重置后的值:	0	0	0	0	0	0	0	1

Bit	Symbol	位名称	Description	R/W
b1, b0	IDTSEL[1:0]	电压监视器2中断发生条件选择	b1b000：检测到VCC Vdet2（上升）时01：检测到VCC<Vdet2（下降）时10：检测到下降和上升时11：禁止设置。	R/W
b2	IRQSEL	电压监视器2中断类型Select	0: Non-maskable interrupt 1: Maskable interrupt.*1	R/W
b7 to b3	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note: 在重写该寄存器之前将PRCR.PRC3位设置为1（允许写入）。
Note 1. 当启用可屏蔽中断时，不要从复位状态更改ICU中NMIER.LVD1EN位的值。

8.2.4 Voltage Monitor 2 Circuit Status Register (LVD2SR)

Address(es): SYSTEM.LVD2SR 4001 E0E3h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	MON	DET
Value after reset:	0	0	0	0	0	0	1	0

Bit	Symbol	Bit name	Description	R/W
b0	DET	Voltage Monitor 2 Voltage Change Detection Flag	0: Not detected 1: V_{det2} passage detection.	R(/W) *1
b1	MON	Voltage Monitor 2 Signal Monitor Flag	0: VCC < V_{det2} 1: VCC ≥ V_{det2} or MON is disabled.	R
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Only 0 can be written to this bit. After writing 0 to this bit, 2 system clock cycles are required for the bit to be read as 0.

DET flag (Voltage Monitor 2 Voltage Change Detection Flag)

The DET flag is enabled when the LVCMPCR.LVD2E bit is 1 (voltage detection 2 circuit enabled) and the LVD2CR0.CMPE bit is 1 (voltage monitor 2 circuit comparison result output enabled).

The DET flag must be set to 0 after LVD2CR0.RIE is set to 0 (disabled). LVD2CR0.RIE can be set to 1 (enabled) after 2 or more PCLKB cycles have elapsed.

MON flag (Voltage Monitor 2 Signal Monitor Flag)

The MON flag is enabled when the LVCMPCR.LVD2E bit is 1 (voltage detection 2 circuit enabled) and the LVD2CR0.CMPE bit is 1 (voltage monitor 2 circuit comparison result output enabled).

Note: Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.

8.2.5 Voltage Monitor Circuit Control Register (LVCMPCR)

Address(es): SYSTEM.LVCMPCR 4001 E417h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	LVD2E	LVD1E	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b4 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b5	LVD1E	Voltage Detection 1 Enable	0: Voltage detection 1 circuit disabled 1: Voltage detection 1 circuit enabled.	R/W
b6	LVD2E	Voltage Detection 2 Enable	0: Voltage detection 2 circuit disabled 1: Voltage detection 2 circuit enabled.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

LVD1E bit (Voltage Detection 1 Enable)

When using voltage detection 1 interrupt/reset or the LVD1SR.MON bit, set the LVD1E bit to 1. The voltage detection 1 circuit starts when td(E-A) elapses after the LVD1E bit value is changed from 0 to 1. When using the voltage detection 1 circuit in Deep Software Standby mode, do not set the DPSBYCR.DEEPCUT[1:0] bits to 11b.

8.2.4 电压监视器2电路状态寄存器(LVD2SR)

Address(es): SYSTEM.LVD2SR 4001 E0E3h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	MON	DET
重置后的值:	0	0	0	0	0	0	1	0

Bit	Symbol	位名称	Description	R/W
b0	DET	电压监视器2电压变化检测标志	0：未检测到1：Vdet2通过检测。	R(/W) *1
b1	MON	电压监视器2信号监视器Flag	0：VCC<Vdet21：VCC Vdet2或MON被禁用。	R
b7 to b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 该位只能写入0。向该位写入0后，需要2个系统时钟周期才能将该位读为0。

DET标志（电压监视器2电压变化检测标志）

当LVCMPCR.LVD2E位为1（使能电压检测2电路）且LVD2CR0.CMPE位为1（电压监控器2电路比较结果输出使能）。

在LVD2CR0.RIE设置为0（禁用）后，DET标志必须设置为0。LVD2CR0.RIE可以在2个或更多PCLKB周期过去后设置为1（启用）。

MON标志（电压监视器2信号监视器标志）

当LVCMPCR.LVD2E位为1（电压检测2电路使能）且LVD2CR0.CMPE位为1（电压监控器2电路比较结果输出使能）。

Note: 在重写该寄存器之前将PRCR.PRC3位设置为1（允许写入）。

8.2.5 电压监控电路控制寄存器(LVCMPCR)

Address(es): SYSTEM.LVCMPCR 4001 E417h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	LVD2E	LVD1E	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b4 to b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b5	LVD1E	电压检测1使能	0：电压检测1电路无效1：电压检测1电路有效。	R/W
b6	LVD2E	电压检测2使能	0：电压检测2电路无效1：电压检测2电路有效。	R/W
b7	—	Reserved	该位读取为0。写入值应为0。	R/W

LVD1E位（电压检测1使能）

使用电压检测1中断复位或LVD1SR.MON位时，将LVD1E位设置为1。LVD1E位值从0变为1后经过td(E-A)时，电压检测1电路启动。使用电压检测时1电路处于深度软件待机模式，请勿将DPSBYCR.DEEPCUT[1:0]位设置为11b。

LVD2E bit (Voltage Detection 2 Enable)

When using voltage detection 2 interrupt/reset or the LVD2SR.MON bit, set the LVD2E bit to 1. The voltage detection 2 circuit starts when td(E-A) elapses after the LVD2E bit value is changed from 0 to 1. When using the voltage detection 2 circuit in Deep Software Standby mode, do not set the DPSBYCR.DEEPCUT[1:0] bits to 11b.

Note: Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.

8.2.6 Voltage Detection Level Select Register (LVDLVLR)

Address(es): SYSTEM.LVDLVLR 4001 E418h

	b7	b6	b5	b4	b3	b2	b1	b0
	LVD2LVL[2:0]			LVD1LVL[4:0]				
Value after reset	1	1	1	1	0	0	1	1

Bit	Symbol	Bit name	Description	R/W
b4 to b0	LVD1LVL[4:0]	Voltage Detection 1 Level Select (Standard voltage during fall in voltage)	b4 b0 1 0 0 0 1: 2.99 V (V_{det1_1}) 1 0 0 1 0: 2.92 V (V_{det1_2}) 1 0 0 1 1: 2.85 V (V_{det1_3}). Other settings are prohibited.	R/W
b7 to b5	LVD2LVL[2:0]	Voltage Detection 2 Level Select (Standard voltage during fall in voltage)	b7 b5 1 0 1: 2.99 V (V_{det2_1}) 1 1 0: 2.92 V (V_{det2_2}) 1 1 1: 2.85 V V_{det2_3}). Other settings are prohibited.	R/W

Note: Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.

The contents of the LVDLVLR register can only be changed if the LVCMPCR.LVD1E and LVCMPCR.LVD2E bits (voltage detection n circuit disable, n = 1, 2) are both 0. Do not set LVD detectors 1 and 2 to the same voltage detection level.

8.2.7 Voltage Monitor 1 Circuit Control Register 0 (LVD1CR0)

Address(es): SYSTEM.LVD1CR0 4001 E41Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	RN	RI	FSAMP[1:0]		—	CMPE	DFDIS	RIE
Value after reset:	1	0	0	0	x	0	1	0

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b0	RIE	Voltage Monitor 1 Interrupt/Reset Enable	0: Disable 1: Enable.	R/W
b1	DFDIS	Voltage Monitor 1 Digital Filter Disable Mode Select	0: Enable digital filter 1: Disable digital filter.	R/W
b2	CMPE	Voltage Monitor 1 Circuit Comparison Result Output Enable	0: Disable voltage monitor 1 circuit comparison result output 1: Enable voltage monitor 1 circuit comparison result output.	R/W
b3	—	Reserved	The read value is undefined. The write value should be 1.	R/W

LVD2E位（电压检测2使能）

使用电压检测2中断复位或LVD2SR.MON位时，将LVD2E位设置为1。LVD2E位值从0变为1后经过td(E-A)时，电压检测2电路启动。使用电压检测时2电路处于深度软件待机模式，请勿将DPSBYCR.DEEPCUT[1:0]位设置为11b。

Note: 在重写该寄存器之前将PRCR.PRC3位设置为1（允许写入）。

8.2.6 电压检测电平选择寄存器(LVDLVLR)

Address(es): SYSTEM.LVDLVLR 4001 E418h

	b7	b6	b5	b4	b3	b2	b1	b0
	LVD2LVL[2:0]			LVD1LVL[4:0]				
重置后的值	1	1	1	1	0	0	1	1

Bit	Symbol	位名称	Description	R/W
b4 to b0	LVD1LVL[4:0]	电压检测1电平选择（电压下降时的标准电压）	b4b010001:2.99V(Vdet1_1)10010:2.92V(Vdet1_2)10011:2.85V(Vdet1_3)。禁止其他设置。	R/W
b7 to b5	LVD2LVL[2:0]	电压检测2电平选择（电压下降时的标准电压）	b7b5101：2.99V(Vdet2_1)110：2.92V(Vdet2_2)111：2.85VVdet2_3)。禁止其他设置。	R/W

Note: 在重写该寄存器之前将PRCR.PRC3位设置为1（允许写入）。

LVDLVLR寄存器的内容只有在LVCMPCR.LVD1E和LVCMPCR.LVD2E位（电压检测n电路禁用，n=1 2）都为0时才能更改。不要将LVD检测器1和2设置为相同的电压检测等级。

8.2.7 电压监视器1电路控制寄存器0(LVD1CR0)

Address(es): SYSTEM.LVD1CR0 4001 E41Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	RN	RI	FSAMP[1:0]		—	CMPE	DFDIS	RIE
重置后的值：	1	0	0	0	x	0	1	0

x: Undefined

Bit	Symbol	位名称	Description	R/W
b0	RIE	电压监视器1 Interrupt/Reset Enable	0：禁用1 ：启用。	R/W
b1	DFDIS	电压监视器1数字滤波器禁用模式选择	0：启用数字滤波器1 ：禁用数字滤波器。	R/W
b2	CMPE	电压监视器1电路比较结果输出 Enable	0：禁止电压监视1电路比较结果输出1：使能电压监视1电路比较结果输出。	R/W
b3	—	Reserved	读取值未定义。写入值应为1。	R/W

Bit	Symbol	Bit name	Description	R/W
b5, b4	FSAMP[1:0]	Sampling Clock Select	b5 b4 0 0: 1/2 LOCO frequency 0 1: 1/4 LOCO frequency 1 0: 1/8 LOCO frequency 1 1: 1/16 LOCO frequency.	R/W
b6	RI	Voltage Monitor 1 Circuit Mode Select	0: Generate voltage monitor 1 interrupt on V_{det1} passage 1: Enable voltage monitor 1 reset when the voltage falls to and below V_{det1}.	R/W
b7	RN	Voltage Monitor 1 Reset Negate Select	0: Negate after a stabilization time (tLVD1) when VCC > V_{det1} is detected 1: Negate after a stabilization time (tLVD1) on assertion of the LVD1 reset.	R/W

RIE bit (Voltage Monitor 1 Interrupt/Reset Enable)

The RIE bit enables or disables voltage monitor 1 interrupt/reset. Set this bit to 1 to ensure that neither a voltage monitor 1 interrupt nor a voltage monitor 1 reset is generated during programming or erasure of the flash memory.

DFDIS bit (Voltage Monitor 1 Digital Filter Disable Mode Select)

The DFDIS bit enables the digital filter circuit. Set the LOCOCR.LCSTP bit to 0 (LOCO operating) if this bit is 0 (enabled). Set the bit to 1 (disabled) when using the voltage monitor 1 circuit in Software Standby or Deep Software Standby mode.

FSAMP[1:0] bits (Sampling Clock Select)

Only change the FSAMP[1:0] bits when the LVD1CR0.DFDIS bit is 1 (digital filter circuit disabled), but not when LVD1CR0.DFDIS is 0 (digital filter circuit enabled).

RI bit (Voltage Monitor 1 Circuit Mode Select)

When the RI bit is 1 (voltage monitor 1 reset selected) or when the LVD2CR0.RI bit is 1 (voltage monitor 2 reset selected), transition to Deep Software Standby mode cannot be made, and operation transitions to Software Standby mode instead. To enter Deep Software Standby mode, set the RI bit to 0 (voltage monitor 1 interrupt selected) and the LVD2CR0.RI bit to 0 (voltage monitor 2 interrupt selected).

RN bit (Voltage Monitor 1 Reset Negate Select)

If the RN bit is to be set to 1 (negation follows a stabilization time on assertion of the LVD1 reset signal), set the LOCOCR.LCSTP bit to 0 (the LOCO operates). Additionally, for a transition to Software Standby or Deep Software Standby, the only possible value for the RN bit is 0 (negation follows a stabilization time when VCC > V_{det1} is detected). Do not set the RN bit to 1 when this is the case.

Note: Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.

8.2.8 Voltage Monitor 2 Circuit Control Register 0 (LVD2CR0)

Address(es): SYSTEM.LVD2CR0 4001 E41Bh

	b7	b6	b5	b4	b3	b2	b1	b0
	RN	RI	FSAMP[1:0]		—	CMPE	DFDIS	RIE
Value after reset:	1	0	0	0	x	0	1	0

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b0	RIE	Voltage Monitor 2 Interrupt/Reset Enable	0: Disable 1: Enable.	R/W
b1	DFDIS	Voltage Monitor 2 Digital Filter Disable Mode Select	0: Enable digital filter 1: Disable digital filter.	R/W

Bit	Symbol	位名称	Description	R/W
b5, b4	FSAMP[1:0]	采样时钟选择	b5b400：12LOCO频率01：14LOCO频率10：18LOCO频率11：116LOCO频率。	R/W
b6	RI	电压监视器1电路模式选择	0：在Vdet1通过时产生电压监控1中断1：当电压下降到Vdet1或低于Vdet1时，使能电压监控1复位。	R/W
b7	RN	电压监视器1复位否定选择	0：当检测到VCC>Vdet1时，在稳定时间(tLVD1)后取反1：在LVD1复位断言有效后稳定时间(tLVD1)后取反。	R/W

RIE位（电压监视器1中断复位使能）

RIE位启用或禁用电压监视器1中断复位。将此位设置为1以确保在闪存的编程或擦除期间不会产生电压监视器1中断或电压监视器1复位。

DFDIS位（电压监视器1数字滤波器禁用模式选择）

DFDIS位使能数字滤波器电路。如果该位为0（启用），则将LOCOCR.LCSTP位设置为0（LOCO操作）。当在软件待机或深度软件待机模式下使用电压监视器1电路时，将该位设置为1（禁用）。

FSAMP[1:0]位（采样时钟选择）

仅当LVD1CR0.DFDIS位为1（禁用数字滤波器电路）时更改FSAMP[1:0]位，但当LVD1CR0.DFDIS为0（启用数字滤波器电路）。

RI位（电压监视器1电路模式选择）

当RI位为1（选择电压监控器1复位）或LVD2CR0.RI位为1（选择电压监控器2复位）时，不能转换到深度软件待机模式，而是操作转换到软件待机模式。要进入深度软件待机模式，请将RI位设置为0（选择电压监视器1中断）并将LVD2CR0.RI位设置为0（选择电压监视器2中断）。

RN位（电压监视器1复位否定选择）

如果RN位被设置为1（否定遵循LVD1复位信号置位的稳定时间），设置LOCOCR.LCSTP位为0（LOCO运行）。此外，对于过渡到软件待机或深度软件待机时，RN位唯一可能的值是0（当检测到VCC>Vdet1时，否定遵循稳定时间）。在这种情况下，请勿将RN位设置为1。

Note: 在重写该寄存器之前将PRCR.PRC3位设置为1（允许写入）。

8.2.8 电压监视器2电路控制寄存器0(LVD2CR0)

Address(es): SYSTEM.LVD2CR0 4001 E41Bh

	b7	b6	b5	b4	b3	b2	b1	b0
	RN	RI	FSAMP[1:0]		—	CMPE	DFDIS	RIE
重置后的值：	1	0	0	0	x	0	1	0

x: Undefined

Bit	Symbol	位名称	Description	R/W
b0	RIE	电压监视器2中断复位Enable	0：禁用1 ：启用。	R/W
b1	DFDIS	电压监视器2数字滤波器禁用模式选择	0：启用数字滤波器1 ：禁用数字滤波器。	R/W

Bit	Symbol	Bit name	Description	R/W
b2	CMPE	Voltage Monitor 2 Circuit Comparison Result Output Enable	0: Disable voltage monitor 2 circuit comparison result output 1: Enable voltage monitor 2 circuit comparison result output.	R/W
b3	—	Reserved	The read value is undefined. The write value should be 1.	R/W
b5, b4	FSAMP[1:0]	Sampling Clock Select	b5 b4 0 0: 1/2 LOCO frequency 0 1: 1/4 LOCO frequency 1 0: 1/8 LOCO frequency 1 1: 1/16 LOCO frequency.	R/W
b6	RI	Voltage Monitor 2 Circuit Mode Select	0: Generate voltage monitor 2 interrupt on V_{det2} passage 1: Enable voltage monitor 2 reset when the voltage falls to and below V_{det2}.	R/W
b7	RN	Voltage Monitor 2 Reset Negate Select	0: Negate after a stabilization time (tLVD2) when VCC > V_{det2} is detected 1: Negate after a stabilization time (tLVD2) on assertion of the LVD2 reset.	R/W

RIE bit (Voltage Monitor 2 Interrupt/Reset Enable)

The RIE bit enables or disables voltage monitor 2 interrupt/reset. Set this bit to 1 to ensure that neither a voltage monitor 2 interrupt nor a voltage monitor 2 reset is generated during programming or erasure of the flash memory.

DFDIS bit (Voltage Monitor 2 Digital Filter Disable Mode Select)

The DFDIS bit enables the digital filter circuit. Set the LOCOCR.LCSTP bit to 0 (the LOCO operates) if this bit is 0 (enabled). Set the bit to 1 (disabled) when using the voltage monitor 2 circuit in Software Standby or Deep Software Standby mode.

FSAMP[1:0] bits (Sampling Clock Select)

Only change the FSAMP[1:0] bits when the LVD2CR0.DFDIS bit is 1 (digital filter circuit disabled), but not when LVD2CR0.DFDIS is 0 (digital filter circuit enabled).

RI bit (Voltage Monitor 2 Circuit Mode Select)

When the RI bit is 1 (voltage monitor 2 reset selected) or when the LVD1CR0.RI bit is 1 (voltage monitor 1 reset selected), transition to Deep Software Standby mode cannot be made, and operation transitions to Software Standby mode instead. To enter Deep Software Standby mode, set the RI bit to 0 (voltage monitor 2 interrupt selected) and the LVD1CR0.RI bit to 0 (voltage monitor 1 interrupt selected).

RN bit (Voltage Monitor 2 Reset Negate Select)

If the RN bit is to be set to 1 (negation follows a stabilization time on assertion of the LVD2 reset signal), set the LOCOCR.LCSTP bit to 0 (the LOCO operates). In addition, for a transition to Software Standby or Deep Software Standby, the only possible value for the RN bit is 0 (negation follows a stabilization time when VCC > V_{det2} is detected). Do not set the RN bit to 1 when this is the case.

Note: Set the PRCR.PRC3 bit to 1 (write enabled) before rewriting this register.

8.3 VCC Input Voltage Monitor

8.3.1 Monitoring V_{det0}

The comparison results from voltage monitor 0 are not available for reading.

8.3.2 Monitoring V_{det1}

Table 8.2 shows the procedure to set up monitoring against V_{det1}. After the settings are complete, the comparison results from voltage monitor 1 can be monitored with the LVD1SR.MON flag.

Bit	Symbol	位名称	Description	R/W
b2	CMPE	电压监视器2电路比较结果输出使能	0：禁止电压监视2电路比较结果输出1：使能电压监视2电路比较结果输出。	R/W
b3	—	Reserved	读取值未定义。写入值应为1。	R/W
b5, b4	FSAMP[1:0]	采样时钟选择	b5b400：12LOCO频率01：14LOCO频率10：18LOCO频率11：116LOCO频率。	R/W
b6	RI	电压监视器2电路模式Select	0：在Vdet2通道时产生电压监视器2中断1：当电压下降到Vdet2或低于Vdet2时，使能电压监视器2复位。	R/W
b7	RN	电压监视器2复位否定Select	0：当检测到VCC>Vdet2时，在稳定时间(tLVD2)后取反1：在LVD2复位有效时，在稳定时间(tLVD2)后取反。	R/W

RIE位（电压监视器2中断复位使能）

RIE位启用或禁用电压监视器2中断复位。将此位设置为1以确保在闪存的编程或擦除期间不会产生电压监视器2中断或电压监视器2复位。

DFDIS位（电压监视器2数字滤波器禁用模式选择）

DFDIS位使能数字滤波器电路。如果该位为0（启用），则将LOCOCR.LCSTP位设置为0（LOCO运行）。当在软件待机或深度软件待机模式下使用电压监视器2电路时，将该位设置为1（禁用）。

FSAMP[1:0]位（采样时钟选择）

仅在LVD2CR0.DFDIS位为1（禁用数字滤波器电路）时更改FSAMP[1:0]位，但在LVD2CR0.DFDIS为0（启用数字滤波器电路）。

RI位（电压监视器2电路模式选择）

当RI位为1（选择电压监控器2复位）或LVD1CR0.RI位为1（选择电压监控器1复位）时，无法转换到深度软件待机模式，而是操作转换到软件待机模式。要进入深度软件待机模式，请将RI位设置为0（选择电压监视器2中断）并将LVD1CR0.RI位设置为0（选择电压监视器1中断）。

RN位（电压监视器2复位否定选择）

如果RN位被设置为1（否定遵循LVD2复位信号置位的稳定时间），设置LOCOCR.LCSTP位为0（LOCO运行）。此外，为了过渡到软件待机或深度软件待机时，RN位唯一可能的值是0（当检测到VCC>Vdet2时，否定遵循稳定时间）。在这种情况下，请勿将RN位设置为1。

Note: 在重写该寄存器之前将PRCR.PRC3位设置为1（允许写入）。

8.3 VCC输入电压监视器

8.3.1 Monitoring V_{det0}

电压监视器0的比较结果不可读取。

8.3.2 Monitoring V_{det1}

表8.2显示了针对Vdet1设置监控的过程。设置完成后，电压监视器1的比较结果可以通过LVD1SR.MON标志进行监视。

Table 8.2 Procedure to set up monitoring against V_{det1}

Step		Monitoring the results of comparison by voltage monitor 1
Setting up the voltage detection 1 circuit	1	Set LVCMPCR.LVD1E = 0 to disable voltage detection 1 before writing to LVDLVLR register.
	2	Select the detection voltage in the LVDLVLR.LVD1LVL[4:0] bits.
	3	Set LVCMPCR.LVD1E = 1 to enable voltage detection 1.
	4	Wait for at least td(E-A) for the LVD operation stabilization time after LVD is enabled.*1
Setting up the digital filter*2	5	Select the sampling clock for the digital filter in the LVD1CR0.FSAMP[1:0] bits.
	6	Set LVD1CR0.DFDIS = 0 to enable the digital filter.
	7	Wait for at least 2n + 3 cycles of the LOCO, where n = 2, 4, 8, 16 and the sampling clock for the digital filter is the LOCO frequency-divided by n.
Enabling output	8	Set LVD1CR0.CMPE = 1 to enable output of the comparison results from voltage monitor 1.

Note 1. Steps 5 to 7 can be performed during the wait time in step 4. For details on td(E-A), see section 60, Electrical Characteristics.
Note 2. Steps 5 to 7 are not required if the digital filter is not in use.

8.3.3 Monitoring V_{det2}

Table 8.3 shows the procedure to set up monitoring against V_{det2}. After the settings are complete, the comparison results from voltage monitor 2 can be monitored with the LVD2SR.MON flag.

Table 8.3 Procedure to set up monitoring against V_{det2}

Step		Monitoring the results of comparison by voltage monitor 2
Setting up the voltage detection 2 circuit	1	Set LVCMPCR.LVD2E = 0 to disable voltage detection 2 before writing to the LVDLVLR register.
	2	Select the detection voltage in the LVDLVLR.LVD2LVL[2:0] bits.
	3	Set LVCMPCR.LVD2E = 1 to enable the voltage detection 2 circuit.
	4	Wait for at least td(E-A) for the LVD operation stabilization time after LVD is enabled.*1
Setting up the digital filter*2	5	Select the sampling clock for the digital filter in the LVD2CR0.FSAMP[1:0] bits.
	6	Set LVD2CR0.DFDIS = 0 to enable the digital filter.
	7	Wait for at least 2n + 3 cycles of the LOCO, where n = 2, 4, 8, 16 and the sampling clock for the digital filter is the LOCO frequency-divided by n.
Enabling output	8	Set LVD2CR0.CMPE = 1 to enable output of the comparison results from voltage monitor 2.

Note 1. Steps 5 to 7 can be performed during the wait time in step 4. For details on td(E-A), see section 60, Electrical Characteristics.
Note 2. Steps 5 to 7 are not required if the digital filter is not in use.

8.4 Reset from Voltage Monitor 0

When using the reset from voltage monitor 0, clear the OFS1.LVDAS bit to 0 to enable the voltage monitor 0 reset after a reset. However, at boot mode, the reset from voltage monitor 0 is disabled regardless of the value of OFS1.LVDAS bit. Figure 8.4 shows an example of operations for a voltage monitor 0 reset.

Table 8.2 针对Vdet1设置监控的程序

Step		通过电压监视器1监视比较结果
设置电压检测1电路	1	设置LVCMPCR.LVD1E=0以在写入LVDLVLR寄存器之前禁用电压检测1。
	2	在LVDLVLR.LVD1LVL[4:0]位中选择检测电压。
	3	设置LVCMPCR.LVD1E=1以启用电压检测1。
	4	启用LVD后，至少等待td(E-A)的LVD操作稳定时间。*1
设置数字滤波器*2	5	在LVD1CR0.FSAMP[1:0]位中选择数字滤波器的采样时钟。
	6	设置LVD1CR0.DFDIS=0以启用数字滤波器。
	7	等待至少2n+3个LOCO周期，其中n=2、4、8、16，数字滤波器的采样时钟是LOCO除以n的频率。
启用输出	8	设置LVD1CR0.CMPE=1以使能电压监视器1的比较结果输出。

Note 1. 步骤5至7可以在步骤4的等待时间内执行。有关td(E-A)的详细信息，请参见第60节，电气特性。
Note 2. 如果不使用数字滤波器，则不需要步骤5到7。

8.3.3 Monitoring V_{det2}

表8.3显示了针对Vdet2设置监控的过程。设置完成后，电压监视器2的比较结果可以通过LVD2SR.MON标志进行监视。

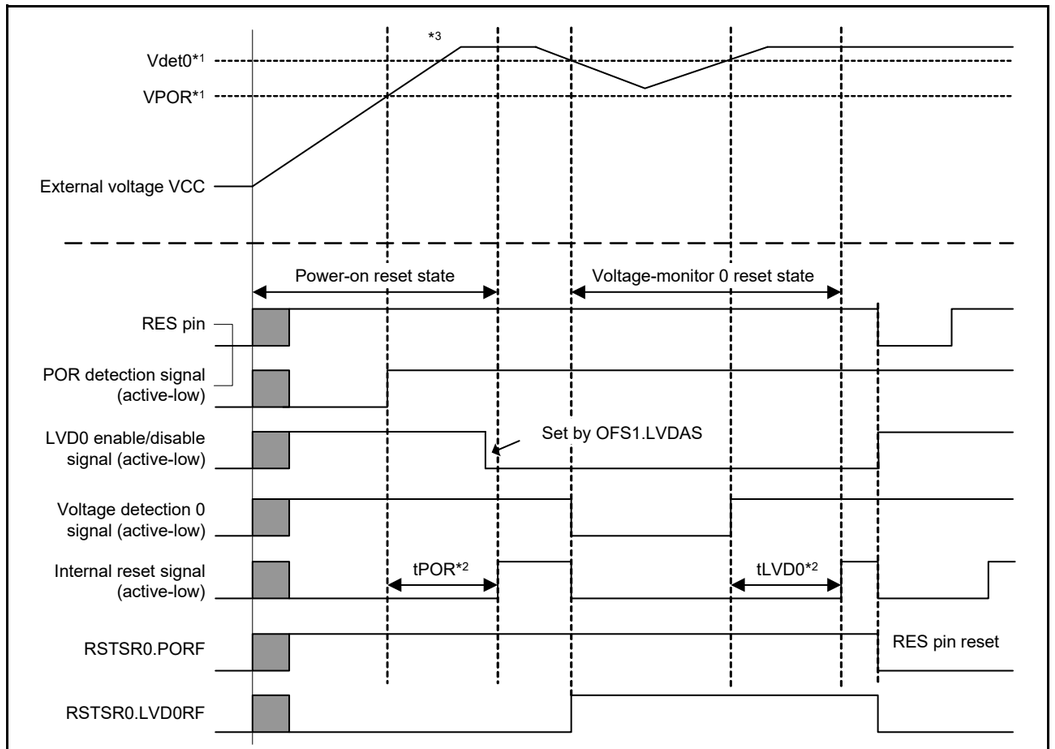
Table 8.3 针对Vdet2设置监控的程序

Step		通过电压监视器2监视比较结果
设置电压检测2电路	1	在写入LVDLVLR寄存器之前，设置LVCMPCR.LVD2E=0以禁用电压检测2。
	2	在LVDLVLR.LVD2LVL[2:0]位中选择检测电压。
	3	设置LVCMPCR.LVD2E=1以启用电压检测2电路。
	4	启用LVD后，至少等待td(E-A)的LVD操作稳定时间。*1
设置数字滤波器*2	5	在LVD2CR0.FSAMP[1:0]位中选择数字滤波器的采样时钟。
	6	设置LVD2CR0.DFDIS=0以启用数字滤波器。
	7	等待至少2n+3个LOCO周期，其中n=2、4、8、16，数字滤波器的采样时钟是LOCO除以n的频率。
启用输出	8	设置LVD2CR0.CMPE=1以使能电压监视器2的比较结果输出。

Note 1. 步骤5至7可以在步骤4的等待时间内执行。有关td(E-A)的详细信息，请参见第60节，电气特性。
Note 2. 如果不使用数字滤波器，则不需要步骤5到7。

8.4 从电压监视器复位0

使用电压监控器0复位时，将OFS1.LVDAS位清零以在复位后启用电压监控器0复位。但是，在引导模式下，无论OFS1.LVDAS位的值如何，都禁止从电压监视器0进行的复位。图8.4显示了电压监视器0复位的操作示例。



Note: For details on the electrical characteristics, see section 60, Electrical Characteristics.
Note 1. VPOR indicates the detection level for a power-on reset and V_{det0} indicates the detection level for a voltage monitor 0 reset.
Note 2. tPOR indicates the period of a power-on reset and tLVD0 indicates the period of a voltage monitor 0 reset.
Note 3. At power-on, raise VCC to the minimum guaranteed voltage before releasing the POR reset.

Figure 8.4 Example of voltage monitor 0 reset operation

8.5 Interrupt and Reset from Voltage Monitor 1

An interrupt or reset can be generated in response to the results of comparison from the voltage monitor 1 circuit.

Table 8.4 shows the procedure for setting bits related to the voltage monitor 1 interrupt and reset so that voltage monitoring operates. Table 8.5 shows the procedure for setting bits related to the voltage monitor 1 interrupt and reset so that voltage monitoring stops. Figure 8.5 shows an example of operations for a voltage monitor 1 interrupt. For the operation of the voltage monitor 1 reset, see Figure 6.2 in section 6, Resets.

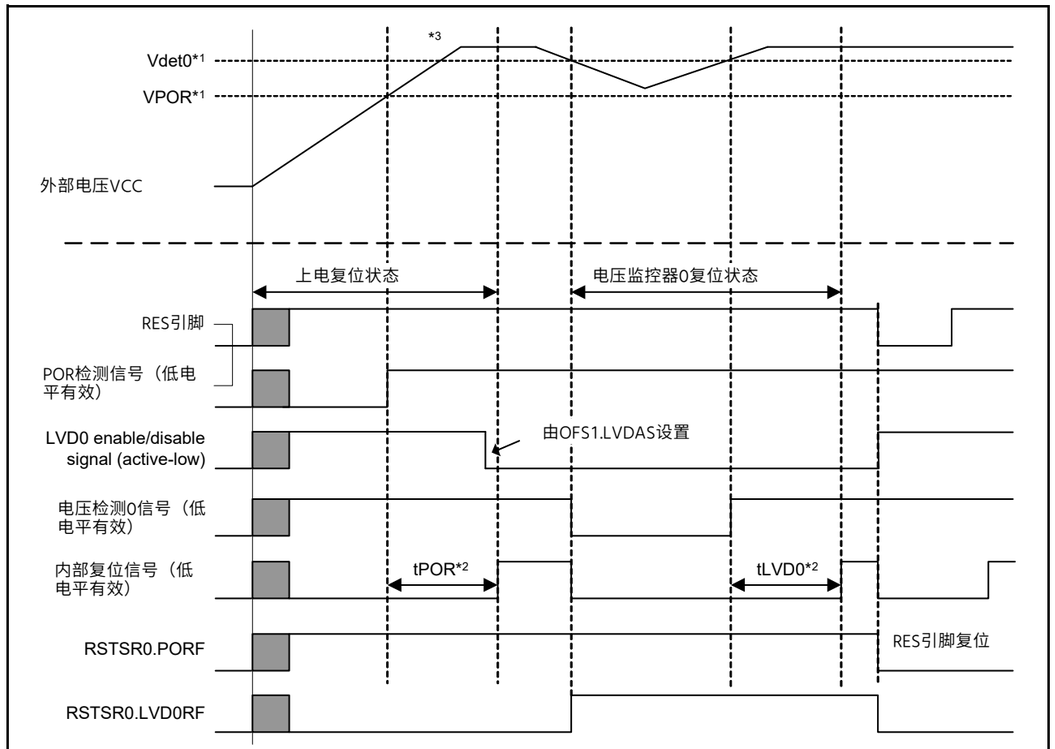
When using the voltage monitor 1 circuit in Software Standby or Deep Software Standby, set up the circuit with the following procedures.

(1) Settings in Software Standby mode

- Disable the digital filter (LVD1CR0.DFDIS = 1)
- When VCC > V_{det1} is detected, negate the voltage monitor 1 reset signal (LVD1CR0.RN = 0) following a stabilization time.

(2) Settings in Deep Software Standby mode

- Disable the digital filter (LVD1CR0.DFDIS = 1)



Note: 有关电气特性的详细信息，请参见第60节，电气特性。
Note 1. VPOR表示上电复位的检测电平，Vdet0表示电压监视器0复位的检测电平。
Note 2. tPOR表示上电复位周期，tLVD0表示电压监视器0复位周期。
Note 3. 上电时，在释放POR复位之前将VCC提高到最低保证电压。

Figure 8.4 电压监视器0复位操作示例

8.5 电压监视器1的中断和复位

响应来自电压监视器1电路的比较结果，可以产生中断或复位。

表8.4显示了设置与电压监控器1中断和复位相关的位以使电压监控器工作的过程。表8.5显示了设置与电压监控1中断和复位相关的位以停止电压监控的过程。图8.5显示了电压监视器1中断的操作示例。有关电压监视器1复位的操作，请参见第6节“复位”中的图6.2。

在软件待机或深度软件待机中使用电压监视器1电路时，请按照以下步骤设置电路。

(1) 软件待机模式中的设置

- 禁用数字滤波器(LVD1CR0.DFDIS=1)
- 当检测到VCC>Vdet1时，在一段稳定时间后取消电压监视器1复位信号(LVD1CR0.RN=0)。

(2) 深度软件待机模式中的设置

- 禁用数字滤波器(LVD1CR0.DFDIS=1)

- Enable voltage monitor 1 interrupts (LVD1CR0.RI = 0). If the voltage monitor 1 reset is enabled (LVD1CR0.RI = 1), a transition to Deep Software Standby mode is not possible, and the operation transitions to Software Standby mode instead
- When the DPSBYCR.DEEPCUT[1:0] bits are 11b, the voltage monitor 1 circuit stops. To use the voltage monitor 1 circuit in Deep Software Standby mode, set the DPSBYCR.DEEPCUT[1:0] bits to a value other than 11b.

Table 8.4 Procedure for setting bits related to the voltage monitor 1 interrupt and voltage monitor 1 reset so that voltage monitoring operates

Step		Voltage monitor 1 interrupt (voltage monitor 1 ELC event output)	Voltage monitor 1 reset
Setting up the voltage detection 1 circuit	1	Set LVCMPCR.LVD1E = 0 to disable voltage detection 1 before writing to the LVDLVLR register.	
	2	Select the detection voltage in the LVDLVLR.LVD1LVL[3:0] bits.	
	3	Set LVCMPCR.LVD1E = 1 to enable the voltage detection 1 circuit.	
	4	Wait for at least td(E-A) for the LVD operation stabilization time after LVD is enabled.*1	
Setting up the digital filter *2	5	Select the sampling clock for the digital filter in the LVD1CR0.FSAMP[1:0] bits.	
	6	Set LVD1CR0.DFDIS = 0 to enable the digital filter.	
	7	Wait for at least 2n + 3 cycles of the LOCO, where n = 2, 4, 8, 16 and the sampling clock for the digital filter is the LOCO frequency-divided by n.*4	
Setting up the voltage monitor 1 interrupt or reset	8	Set LVD1CR0.RI = 0 to select the voltage monitor 1 interrupt.	• Set LVD1CR0.RI = 1 to select the voltage monitor 1 reset • Select the type of reset negation in the LVD1CR0.RN bit.
	9	• Select the interrupt request timing in the LVD1CR1.IDTSEL[1:0] bits • Select the interrupt type in the LVD1CR1.IRQSEL bit.	—
Enabling output	10	Set LVD1SR.DET = 0.	
	11	Set LVD1CR0.RIE = 1 to enable the voltage monitor 1 interrupt or reset.*3	
	12	Set LVD1CR0.CMPE = 1 to enable output of the comparison results from voltage monitor 1.	

Note 1. Steps 5 to 11 can be performed during the wait time in step 4. For details on td(E-A), see section 60, Electrical Characteristics.
Note 2. Steps 5 to 7 are not required if the digital filter is not in use.
Note 3. Step 11 is not required if only the ELC event signal is to be output.
Note 4. Steps 8 to 11 can be performed during the wait time in step 7.

Table 8.5 Procedure for setting bits related to the voltage monitor 1 interrupt and voltage monitor 1 reset so that voltage monitoring stops

Step		Voltage monitor 1 interrupt (voltage monitor 1 ELC event output), voltage monitor 1 reset
Settings to stop enabling output	1	Set LVD1CR0.CMPE = 0 to disable output of the comparison results from voltage monitor 1.
	2	Wait for at least 2n + 3 cycles of the LOCO, where n = 2, 4, 8, 16 and the sampling clock for the digital filter is the LOCO frequency-divided by n.*1
	3	Set LVD1CR0.RIE = 0 to disable the voltage monitor 1 interrupt or reset.*2
Stopping the digital filter	4	Set LVD1CR0.DFDIS = 1 to disable the digital filter.*1, *3
Stopping the voltage detection 1 circuit	5	Set LVCMPCR.LVD1E = 0 to disable the voltage detection 1 circuit.

Note 1. Steps 2 and 4 are not required if the digital filter is not in use.
Note 2. Step 3 is not required if only the ELC event signal is to be output.
Note 3. To disable the digital filter from its enabled state and then re-enable it, disable it and wait for at least 2 LOCO clock cycles before re-enabling it.

- 启用电压监视器1中断(LVD1CR0.RI=0)。如果启用了电压监视器1复位(LVD1CR0.RI=1)，则无法转换到深度软件待机模式，而是将操作转换到软件待机模式
- 当DPSBYCR.DEEPCUT[1:0]位为11b时，电压监视器1电路停止。要在深度软件待机模式下使用电压监视器1电路，请将DPSBYCR.DEEPCUT[1:0]位设置为11b以外的值。

Table 8.4 设置与电压监控器1中断和电压监控器1复位相关的位以使电压监控器运行的步骤

Step		电压监视器1中断（电压监视器1 ELC event output)	电压监视器1复位
设置电压检测1电路	1	设置LVCMPCR.LVD1E=0以在写入LVDLVLR寄存器之前禁用电压检测1。	
	2	在LVDLVLR.LVD1LVL[3:0]位中选择检测电压。	
	3	设置LVCMPCR.LVD1E=1以启用电压检测1电路。	
	4	启用LVD后，至少等待td(E-A)的LVD操作稳定时间。*1	
设置数字滤波器*2	5	在LVD1CR0.FSAMP[1:0]位中选择数字滤波器的采样时钟。	
	6	设置LVD1CR0.DFDIS=0以启用数字滤波器。	
	7	等待至少2n+3个LOCO周期，其中n=2、4、8、16，数字滤波器的采样时钟是LOCO除以n的频率。*4	
设置电压监视器1中断或复位	8	设置LVD1CR0.RI=0以选择电压监视器1中断。	设置LVD1CR0.RI=1以选择电压监视器1复位在LVD1CR0.RN位中选择复位否定类型。
	9	在LVD1CR1.IDTSEL[1:0]位中选择中断请求时序 在LVD1CR1.IRQSEL位中选择中断类型。	—
启用输出	10	Set LVD1SR.DET = 0.	
	11	设置LVD1CR0.RIE=1以启用电压监视器1中断或复位。*3	
	12	设置LVD1CR0.CMPE=1以使能电压监视器1的比较结果输出。	

Note 1. 步骤5至11可以在步骤4的等待时间内执行。有关td(E-A)的详细信息，请参见第60节，电气特性。
Note 2. 如果不使用数字滤波器，则不需要步骤5到7。
Note 3. 如果只输出ELC事件信号，则不需要步骤11。
Note 4. 步骤8至11可以在步骤7的等待时间内执行。

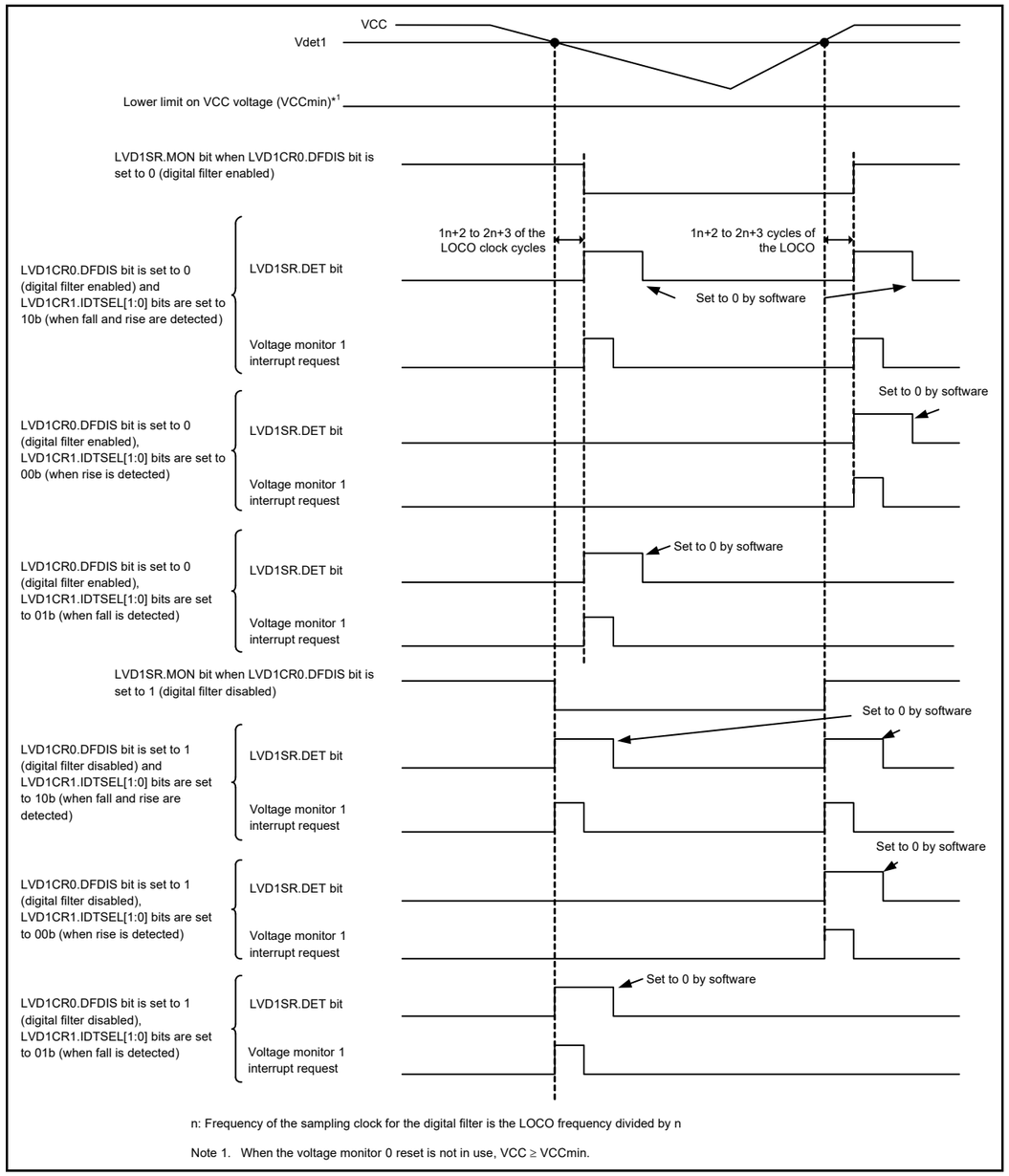
Table 8.5 设置与电压监控1中断和电压监控1复位相关的位以停止电压监控的步骤

Step		电压监视器1中断（电压监视器1ELC事件输出），电压监视器1复位
停止启用输出的设置	1	设置LVD1CR0.CMPE=0以禁用电压监视器1的比较结果输出。
	2	等待至少2n+3个LOCO周期，其中n=2、4、8、16，数字滤波器的采样时钟是LOCO除以n的频率。*1
	3	设置LVD1CR0.RIE=0以禁用电压监视器1中断或复位。*2
停止数字滤波器	4	设置LVD1CR0.DFDIS=1以禁用数字滤波器。*1 *3
停止电压检测1电路	5	设置LVCMPCR.LVD1E=0以禁用电压检测1电路。

Note 1. 如果不使用数字滤波器，则不需要步骤2和4。
Note 2. 如果只输出ELC事件信号，则不需要步骤3。
Note 3. 要从启用状态禁用数字滤波器然后重新启用它，请禁用它并等待至少2个LOCO时钟周期，然后再重新启用它。

If the voltage monitor 1 interrupt or reset setting is to be made again after it is used and stopped once, omit the following steps in the procedures for stopping and setting, depending on the conditions:

- Setting or stopping the voltage detection 1 circuit is not required if the settings for the circuit do not change
- Setting or stopping the digital filter is not required if the settings for the digital filter do not change
- Setting the voltage monitor 1 interrupt or reset is not required if the settings for the voltage monitor 1 interrupt or reset do not change.



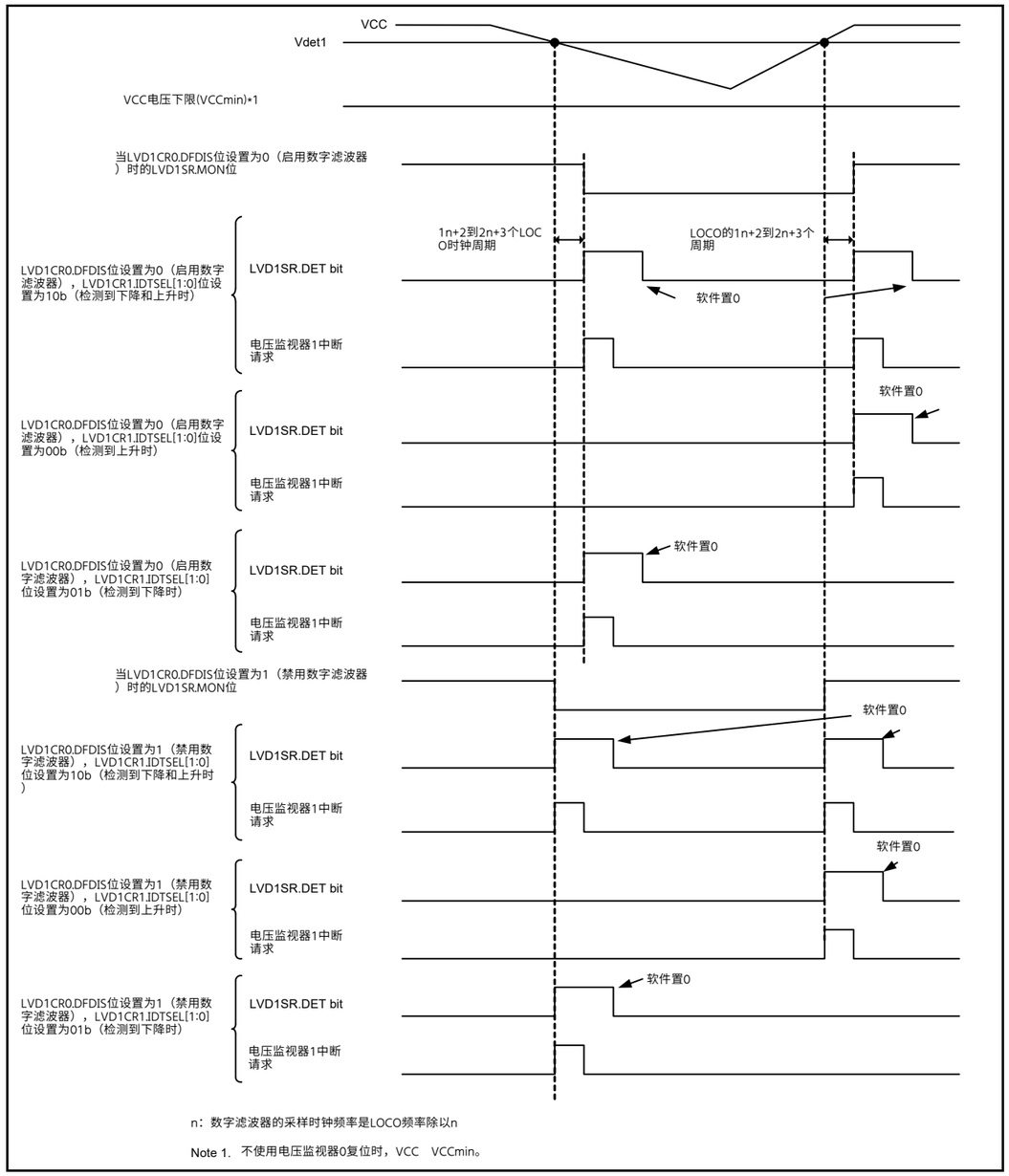
n: Frequency of the sampling clock for the digital filter is the LOCO frequency divided by n

Note 1. When the voltage monitor 0 reset is not in use, VCC ≥ VCCmin.

Figure 8.5 Voltage monitor 1 interrupt operation example

如果电压监视器1在使用和停止一次后再次进行中断或复位设置，则根据条件省略停止和设置过程中的以下步骤：

- 如果电路的设置不改变，则不需要设置或停止电压检测1电路
- 如果数字滤波器的设置不变，则不需要设置或停止数字滤波器
- 如果电压监视器1中断或复位的设置没有改变，则不需要设置电压监视器1中断或复位。



n：数字滤波器的采样时钟频率是LOCO频率除以n

Note 1. 不使用电压监视器0复位时，VCC VCCmin。

Figure 8.5 电压监视器1中断操作示例

8.6 Interrupt and Reset from Voltage Monitor 2

An interrupt or reset can be generated in response to the comparison results from the voltage monitor 2 circuit.

Table 8.6 shows the procedure for setting bits related to the voltage monitor 2 interrupt and reset so that voltage monitoring operates. Table 8.7 shows the procedure for setting bits related to the voltage monitor 2 interrupt and reset so that voltage monitoring stops. Figure 8.6 shows an example of operations for a voltage monitor 2 interrupt. For the operation of the voltage monitor 2 reset, see Figure 6.2 in section 6, Resets.

When using the voltage monitor 2 circuit in Software Standby or Deep Software Standby, set up the circuit with the following procedures.

(1) Settings in Software Standby mode

- Disable the digital filter (LVD2CR0.DFDIS = 1)
- When VCC > V_{det2} is detected, negate the voltage monitor 2 reset signal (LVD2CR0.RN = 0) following a stabilization time.

(2) Settings in Deep Software Standby mode

- Disable the digital filter (LVD2CR0.DFDIS = 1)
- Enable voltage monitor 2 interrupts (LVD2CR0.RI = 0). If the voltage monitor 2 reset is enabled (LVD2CR0.RI = 1), a transition to Deep Software Standby mode is not possible, and the operation transitions to Software Standby mode instead.
- When the DPSBYCR.DEEPCUT[1:0] bits are 11b, the voltage monitor 2 circuit stops. To use the voltage monitor 2 circuit in Deep Software Standby mode, set the DPSBYCR.DEEPCUT[1:0] bits to a value other than 11b.

Table 8.6 Procedures for setting bits related to voltage monitor 2 interrupt and voltage monitor 2 reset so that voltage monitoring occurs

Step		Voltage monitor 2 interrupt (voltage monitor 2 ELC event output)	Voltage monitor 2 reset
Setting up the voltage detection 2 circuit	1	Set LVCMPCR.LVD2E = 0 to disable voltage detection 2 before writing to the LVDLVLR register.	
	2	Select the detection voltage in the LVDLVLR.LVD2LVL[2:0] bits.	
	3	Set LVCMPCR.LVD2E = 1 to enable the voltage detection 2 circuit.	
	4	Wait for at least td(E-A) for the LVD operation stabilization time after LVD is enabled.*1	
Setting up the digital filter *2	5	Select the sampling clock for the digital filter in the LVD2CR0.FSAMP[1:0] bits.	
	6	Set LVD2CR0.DFDIS = 0 to enable the digital filter.	
	7	Wait for at least 2n + 3 LOCO clock cycles, where n = 2, 4, 8, 16, and the sampling clock for the digital filter is the LOCO frequency-divided by n.*4	
Setting up the voltage monitor 2 interrupt or reset	8	Set LVD2CR0.RI = 0 to select the voltage monitor 2 interrupt.	• Set LVD2CR0.RI = 1 to select the voltage monitor 2 reset • Select the type of reset negation in the LVD2CR0.RN bit.
	9	• Select the interrupt request timing in the LVD2CR1.IDTSEL[1:0] bits • Select the interrupt type in the LVD2CR1.IRQSEL bit.	—
Enabling output	10	Set LVD2SR.DET = 0.	
	11	Set LVD2CR0.RIE = 1 to enable the voltage monitor 2 interrupt or reset.*3	
	12	Set LVD2CR0.CMPE = 1 to enable output of the comparison results from voltage monitor 2.	

Note 1. Steps 5 to 11 can be performed during the wait time in step 4. For details on td(E-A), see section 60, Electrical Characteristics.
Note 2. Steps 5 to 7 are not required if the digital filter is not in use.
Note 3. Step 11 is not required if only the ELC event signal is to be output.
Note 4. Steps 8 to 10 can be performed during the wait time in step 7.

8.6 电压监视器2的中断和复位

响应电压监视器2电路的比较结果，可以产生中断或复位。

表8.6显示了设置与电压监控器2中断和复位相关的位以使电压监控器工作的过程。表8.7显示了设置与电压监控2中断和复位相关的位以停止电压监控的过程。图8.6显示了电压监视器2中断的操作示例。有关电压监视器2复位的操作，请参见第6节“复位”中的图6.2。

在软件待机或深度软件待机中使用电压监视器2电路时，请按照以下步骤设置电路。

(1) 软件待机模式中的设置

- 禁用数字滤波器(LVD2CR0.DFDIS=1)
- 当检测到VCC>Vdet2时，在一段稳定时间后取消电压监视器2复位信号(LVD2CR0.RN=0)。

(2) 深度软件待机模式中的设置

- 禁用数字滤波器(LVD2CR0.DFDIS=1)
- 启用电压监视器2中断(LVD2CR0.RI=0)。如果启用电压监视器2复位(LVD2CR0.RI=1)，则无法转换到深度软件待机模式，而是将操作转换到软件待机模式。
- 当DPSBYCR.DEEPCUT[1:0]位为11b时，电压监视器2电路停止。要在深度软件待机模式下使用电压监视器2电路，请将DPSBYCR.DEEPCUT[1:0]位设置为11b以外的值。

Table 8.6 设置与电压监控器2中断和电压监控器2相关的位以进行电压监控的步骤

Step		电压监视器2中断（电压监视器2 ELC event output)	电压监视器2复位
设置电压检测2电路	1	在写入LVDLVLR寄存器之前，设置LVCMPCR.LVD2E=0以禁用电压检测2。	
	2	在LVDLVLR.LVD2LVL[2:0]位中选择检测电压。	
	3	设置LVCMPCR.LVD2E=1以启用电压检测2电路。	
	4	启用LVD后，至少等待td(E-A)的LVD操作稳定时间。*1	
设置数字滤波器*2	5	在LVD2CR0.FSAMP[1:0]位中选择数字滤波器的采样时钟。	
	6	设置LVD2CR0.DFDIS=0以启用数字滤波器。	
	7	等待至少2n+3个LOCO时钟周期，其中n=2 4 8 16，数字滤波器的采样时钟是LOCO除以n.*4	
设置电压监视器2中断或复位	8	设置LVD2CR0.RI=0以选择电压监视器2中断。	设置LVD2CR0.RI=1以选择电压监视器2复位 在LVD2CR0.RN位中选择复位否定类型。
	9	在LVD2CR1.IDTSEL[1:0]位中选择中断请求时序 在LVD2CR1.IRQSEL位中选择中断类型。	—
启用输出	10	Set LVD2SR.DET = 0.	
	11	设置LVD2CR0.RIE=1以启用电压监视器2中断或复位。*3	
	12	设置LVD2CR0.CMPE=1以使能电压监视器2的比较结果输出。	

Note 1. 步骤5至11可以在步骤4的等待时间内执行。有关td(E-A)的详细信息，请参见第60节，电气特性。
Note 2. 如果不使用数字滤波器，则不需要步骤5到7。
Note 3. 如果只输出ELC事件信号，则不需要步骤11。
Note 4. 步骤8至10可以在步骤7的等待时间内执行。

Table 8.7 Procedure for setting bits related to voltage monitor 2 interrupt and voltage monitor 2 reset so that voltage monitoring stops

Step		Voltage monitor 2 interrupt (voltage monitor 2 ELC event output), voltage monitor 2 reset
Settings to stop enabling output	1	Set LVD2CR0.CMPE = 0 to disable output of the comparison results from voltage monitor 2.
	2	Wait for at least 2n + 3 LOCO clock cycles, where n = 2, 4, 8, 16, and the sampling clock for the digital filter is the LOCO frequency-divided by n.*1
	3	Set LVD2CR0.RIE = 0 to disable the voltage monitor 2 interrupt or reset.*2
Stopping the digital filter	4	Set LVD2CR0.DFDIS = 1 to disable the digital filter.*1, *3
Stopping the voltage detection 1 circuit	5	Set LVCMPCR.LVD2E = 0 to disable the voltage detection 2 circuit.

Note 1. Steps 2 and 4 are not required if the digital filter is not in use.
Note 2. Step 3 is not required if only the ELC event signal is to be output.
Note 3. To disable the digital filter from its enabled state and then re-enable it, disable it and wait for at least 2 LOCO clock cycles before re-enabling it.

If the voltage monitor 2 interrupt or reset setting is to be made again after it is used and stopped once, omit the following steps in the procedures for stopping and setting, depending on the conditions:

- Setting or stopping the voltage detection 2 circuit is not required if the settings for the circuit do not change
- Setting or stopping the digital filter is not required if the settings for the digital filter do not change
- Setting the voltage monitor 2 interrupt or reset is not required if the settings for the voltage monitor 2 interrupt or voltage monitor 2 reset do not change.

Table 8.7 设置与电压监控2中断和电压监控2复位相关的位以停止电压监控的步骤

Step		电压监控器2中断（电压监控器2ELC事件输出），电压监控器2复位
停止启用输出的设置	1	设置LVD2CR0.CMPE=0以禁用电压监视器2的比较结果输出。
	2	等待至少2n+3个LOCO时钟周期，其中n=2、4、8、16，数字滤波器的采样时钟是LOCO除以n的频率。*1
	3	设置LVD2CR0.RIE=0以禁用电压监视器2中断或复位。*2
停止数字滤波器	4	设置LVD2CR0.DFDIS=1以禁用数字滤波器。*1 *3
停止电压检测1电路	5	设置LVCMPCR.LVD2E=0以禁用电压检测2电路。

Note 1. 如果不使用数字滤波器，则不需要步骤2和4。
Note 2. 如果只输出ELC事件信号，则不需要步骤3。
Note 3. 要从启用状态禁用数字滤波器然后重新启用它，请禁用它并等待至少2个LOCO时钟周期，然后再重新启用它。

如果电压监视器2在使用和停止一次后再次进行中断或复位设置，则在停止和设置过程中省略以下步骤，视情况而定：

- 如果电路的设置不变，则不需要设置或停止电压检测2电路
- 如果数字滤波器的设置不变，则不需要设置或停止数字滤波器
- 如果电压监视器2中断或电压监视器2复位的设置没有改变，则不需要设置电压监视器2中断或复位。

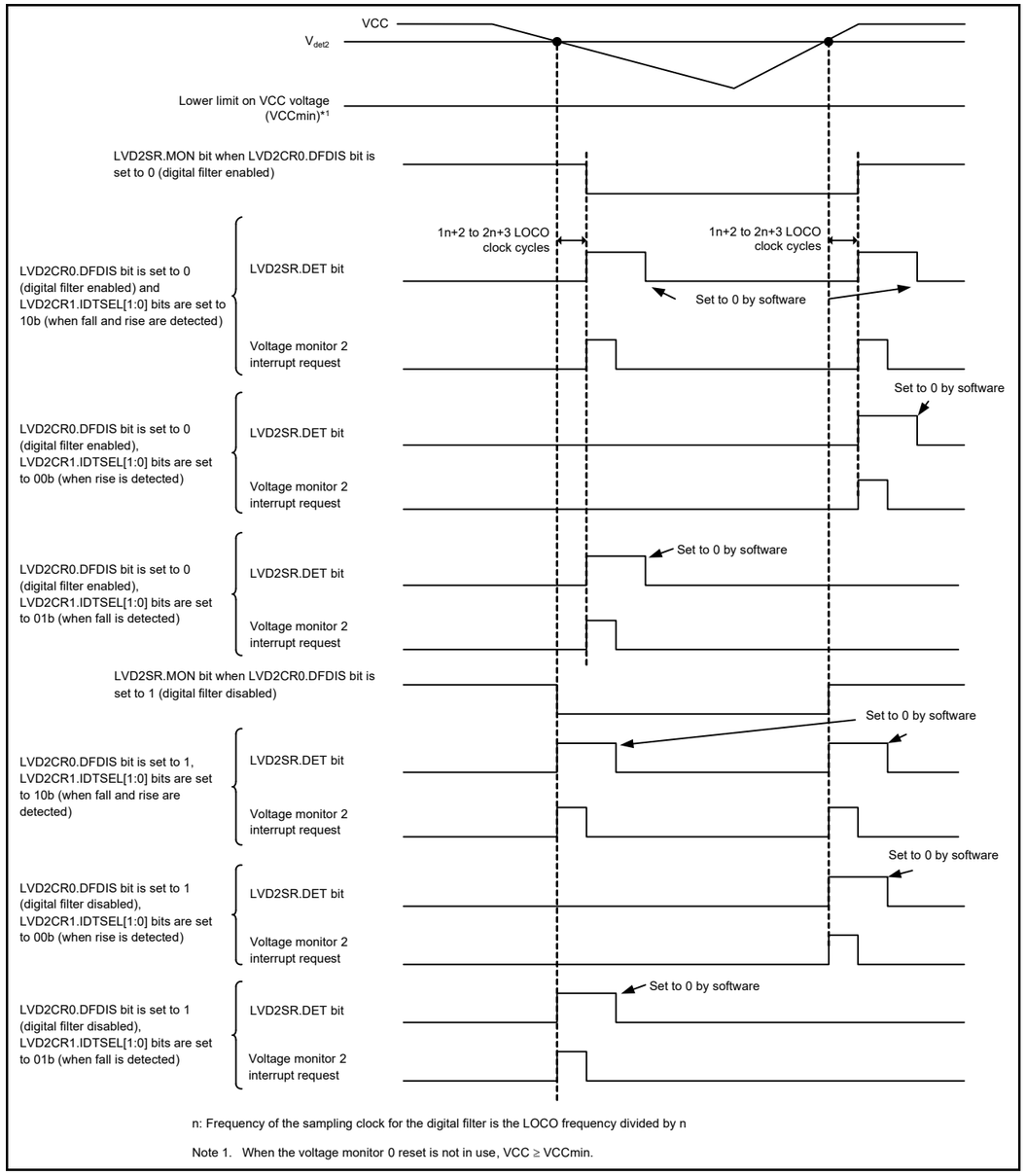


Figure 8.6 Example of voltage monitor 2 interrupt operation

8.7 Event Link Output

The LVD can output the event signals to the Event Link Controller (ELC).

(1) V_{det1} Crossing Detection Event

The LVD outputs the event signal when it detects that the voltage has passed the V_{det1} voltage while both the voltage detection 1 circuit and the voltage monitor 1 circuit comparison result output are enabled.

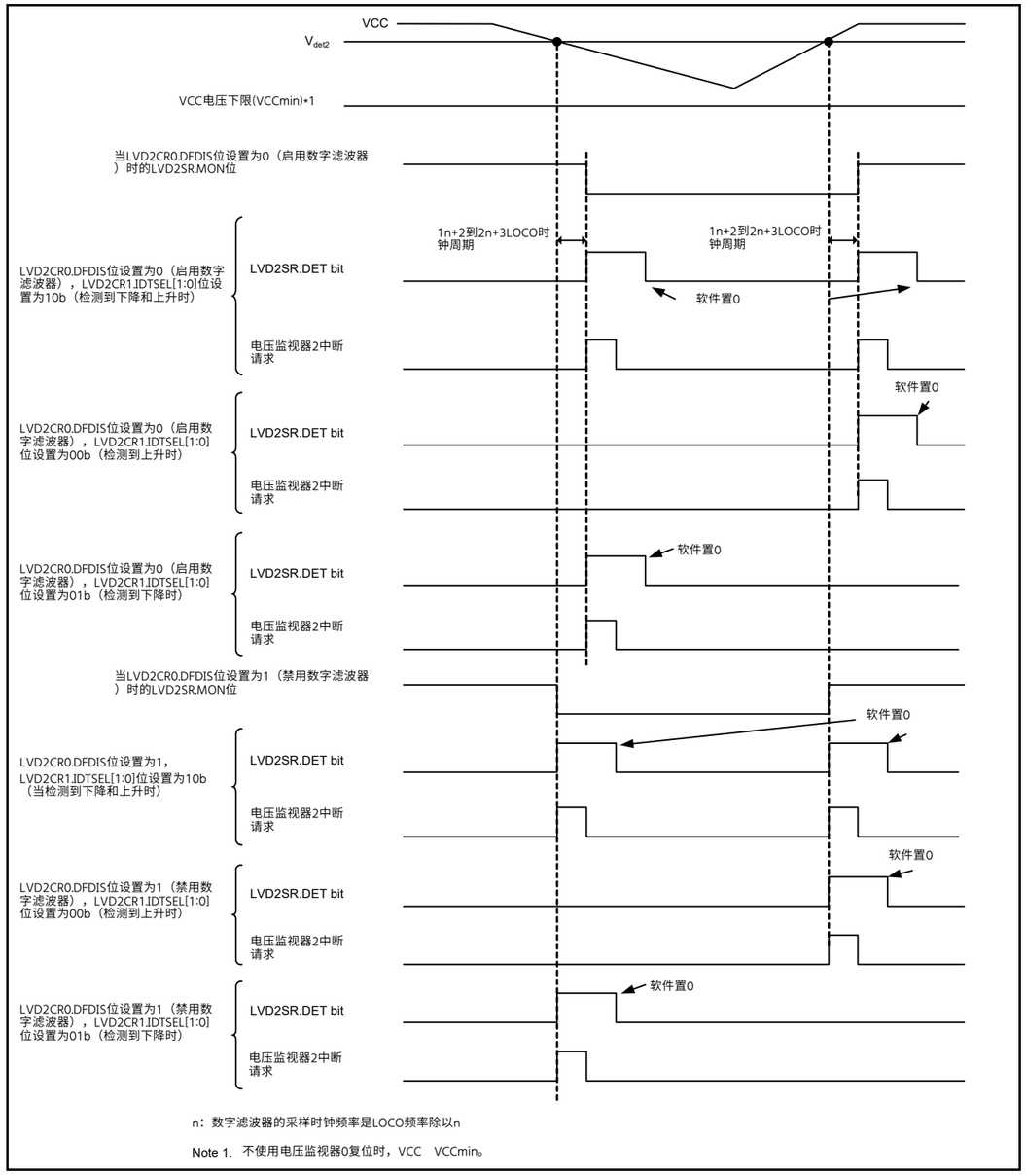


Figure 8.6 电压监视器2中断操作示例

8.7 事件链接输出

LVD可以将事件信号输出到事件链接控制器(ELC)。

(1) Vdet1交叉检测事件

当电压检测1电路和电压监视器1电路比较结果输出都启用时，LVD检测到电压已超过Vdet1电压时输出事件信号。

(2) V_{det2} Crossing Detection Event

The LVD outputs the event signal when it detects that the voltage has passed the V_{det2} voltage while both the voltage detection 2 circuit and the voltage monitor 2 circuit comparison result output are enabled.

When enabling the event link output function of the LVD, you must enable the LVD before enabling the LVD event link function of the ELC. To stop the event link output function of the LVD, you must stop the LVD before disabling the LVD event link function of the ELC.

8.7.1 Interrupt Handling and Event Linking

The LVD provides bits to individually enable or disable the voltage monitor 1 and 2 interrupts. When an interrupt source is generated and the interrupt is enabled by the interrupt enable bit, the interrupt signal (LVD1CR0.RIE or LVD2CR0.RIE) is output to the CPU.

On the other hand, as soon as an interrupt source is generated, an event link signal is output as the event signal to the other module through the ELC, regardless of the state of the interrupt enable bit.

It is possible to output voltage monitor 1 and 2 interrupts in Software Standby and Deep Software Standby modes. The event signals for the ELC in Software Standby and Deep Software Standby modes are output as follows:

- When a V_{det1} or V_{det2} passage event is detected in Software Standby mode, event signals are not generated for the ELC because the clock is not supplied in Software Standby mode. Because the V_{det1} and V_{det2} passage detection flags are saved, when the clock supply resumes after returning from Software Standby mode, the event signals for the ELC are output based on the state of the V_{det1} and V_{det2} detection flags.
- When a V_{det1} or V_{det2} passage events is detected in Deep Software Standby mode, event signals are not generated for the ELC.

(2) Vdet2交叉检测事件

当电压检测2电路和电压监测器2电路比较结果输出都启用时，LVD检测到电压已超过Vdet2电压时输出事件信号。

使能LVD的事件链接输出功能时，必须先使能LVD，再使能ELC的LVD事件链接功能。要停止LVD的事件链接输出功能，必须先停止LVD，然后再禁用ELC的LVD事件链接功能。

8.7.1 中断处理和事件链接

LVD提供位来单独启用或禁用电压监视器1和2中断。当产生中断源并通过中断使能位使能中断时，向CPU输出中断信号（LVD1CR0.RIE或LVD2CR0.RIE）。

另一方面，一旦产生中断源，无论中断使能位的状态如何，都会通过ELC将事件链接信号作为事件信号输出到其他模块。

在软件待机和深度软件待机模式下，可以输出电压监视器1和2中断。软件待机和深度软件待机模式下ELC的事件信号输出如下：

- 当在软件待机模式下检测到Vdet1或Vdet2通过事件时，不会为ELC生成事件信号，因为在软件待机模式下不提供时钟。因为保存了Vdet1和Vdet2通过检测标志，所以当从软件待机模式恢复后时钟供应恢复时，ELC的事件信号将根据Vdet1和Vdet2检测标志的状态输出。
- 当在深度软件待机模式下检测到Vdet1或Vdet2通过事件时，不会为ELC生成事件信号。

9. Clock Generation Circuit

9.1 Overview

The MCU provides a clock generation circuit.

Table 9.1 and Table 9.2 list the clock generation circuit specifications, Figure 9.1 shows a block diagram, and Table 9.3 lists the I/O pins.

Table 9.1 Specifications of the clock generation circuit for the clock sources

Clock source	Parameter	Specifications
Main clock oscillator (MOSC)	Resonator frequency	8 to 24 MHz USB boot mode: 8, 10, 12, 15, 16, 20, 24 MHz
	External clock input frequency	Up to 24 MHz
	External resonator or additional circuit: ceramic resonator, crystal	Available
	Connection pins EXTAL, XTAL	
	Drive capability switching	
	Oscillation stop detection function	
Sub-clock oscillator (SOSC)	Resonator frequency	32.768 kHz
	External resonator or additional circuit: crystal resonator	Available
	Connection pins: XCIN, XCOUT	
	Drive capability switching	
PLL circuit	Input clock source	MOSC, HOCO
	Input pulse frequency division ratio	Selectable from 1, 2, and 3
	Input frequency	8 to 24 MHz
	Frequency multiplication ratio	Selectable from 10 to 30 (0.5 steps) *1,*2
	PLL output frequency	120 to 240 MHz
High-speed on-chip oscillator (HOCO)	Oscillation frequency	16, 18, 20 MHz
	User trimming	Available
Middle-speed on-chip oscillator (MOCO)	Oscillation frequency	8 MHz
	User trimming	Available
Low-speed on-chip oscillator (LOCO)	Oscillation frequency	32.768 kHz
	User trimming	Available
IWDT-dedicated on-chip oscillator (IWDTLOCO)	Oscillation frequency	15 kHz
External clock input for JTAG (TCK)	Input clock frequency	Up to 25 MHz
External clock input for SWD (SWCLK)	Input clock frequency	Up to 25 MHz

Note 1. Selectable from 10 to 20 when oscillation stop detection function is enabled and input frequency less than 12 MHz is used.
Note 2. Except for the condition in note 1, oscillation stop detection function is available by CAC.

Table 9.2 Specifications of the clock generation circuit for the internal clocks (1 of 3)

Parameter	Clock sources	Clock supply	Specifications
System clock (ICLK)	MOSC, SOSC, HOCO, MOCO, LOCO, PLL	CPU, DTC, DMAC, Flash, SRAM	Up to 120 MHz Division ratios: 1, 2, 4, 8, 16, 32, 64

9. 时钟产生电路

9.1 Overview

MCU提供时钟生成电路。

表9.1和表9.2列出了时钟生成电路规格，图9.1显示了框图，表9.3列出了IO引脚。

Table 9.1 时钟源的时钟产生电路规格

时钟源	Parameter	Specifications
主时钟振荡器(MOSC)	谐振器频率	8至24MHzUSB启动模式：8、10、12、15、16、20、24 MHz
	外部时钟输入频率	高达24MHz
	外部谐振器或附加电路：陶瓷谐振器、晶体	Available
	连接针EXTAL、XTAL	
	驱动能力切换	
	振荡停止检测功能	
Sub-clock oscillator (SOSC)	谐振器频率	32.768 kHz
	外部谐振器或附加电路：晶体谐振器	Available
	Connection pins: XCIN, XCOUT	
	驱动能力切换	
PLL circuit	输入时钟源	MOSC, HOCO
	输入脉冲分频比	可从1、2和3中选择
	输入频率	8 to 24 MHz
	倍频比	可从10到30（0.5步）*1 *2中选择
	锁相环输出频率	120 to 240 MHz
High-speed on-chip oscillator (HOCO)	振荡频率	16, 18, 20 MHz
	用户修剪	Available
Middle-speed on-chip oscillator (MOCO)	振荡频率	8 MHz
	用户修剪	Available
Low-speed on-chip oscillator (LOCO)	振荡频率	32.768 kHz
	用户修剪	Available
IWDT-dedicated on-chip oscillator (IWDTLOCO)	振荡频率	15 kHz
JTAG(TCK)的外部时钟输入	输入时钟频率	高达25MHz
SWD的外部时钟输入(SWCLK)	输入时钟频率	高达25MHz

Note 1. 当振荡停止检测功能启用并且使用低于12MHz的输入频率时，可以从10到20中选择。
Note 2. 除注1中的条件外，CAC提供振荡停止检测功能。

Table 9.2 内部时钟的时钟生成电路的规格(1of3)

Parameter	时钟源	时钟电源	Specifications
系统时钟(ICLK)	MOSC, SOSC, HOCO, MOCO, LOCO, PLL	CPU、DTC、DMAC、闪存、SRAM	高达120MHz Division ratios: 1, 2, 4, 8, 16, 32, 64

Table 9.2 Specifications of the clock generation circuit for the internal clocks (2 of 3)

Parameter	Clock sources	Clock supply	Specifications
Peripheral module clock A (PCLKA)	MOSC, SOSC, HOCO, MOCO, LOCO, PLL	Peripheral modules (ETHERC, EDMAC, USBHS, QSPI, SPI, SCI, SCE7, GLCDC, SDHI, CRC, JPEG engine, DRW, IrDA, GPT bus-clock)	Up to 120 MHz*2 Division ratios: 1, 2, 4, 8, 16, 32, 64
Peripheral module clock B (PCLKB)	MOSC, SOSC, HOCO, MOCO, LOCO, PLL	Peripheral modules (IIC, SSIE, SRC, DOC, CAC, CAN, DAC12, POEG, CTSU, AGT, Standby SRAM, ELC, I/O ports, RTC, WDT, IWDT, ADC12, KINT, USBFS, ACMPHS, TSN, PDC)	Up to 60 MHz Division ratios: 1, 2, 4, 8, 16, 32, 64
Peripheral module clock C (PCLKC)	MOSC, SOSC, HOCO, MOCO, LOCO, PLL	Peripheral module (ADC12 conversion clock)	Up to 60 MHz Division ratios: 1, 2, 4, 8, 16, 32, 64
Peripheral module clock D (PCLKD)	MOSC, SOSC, HOCO, MOCO, LOCO, PLL	Peripheral module (GPT count-clock)	Up to 120 MHz Division ratios: 1, 2, 4, 8, 16, 32, 64
Flash interface clock (FCLK)	MOSC, SOSC, HOCO, MOCO, LOCO, PLL	Flash interface	4 to 60 MHz (P/E) Up to 60 MHz (read) *1 Division ratios: 1, 2, 4, 8, 16, 32, 64
External bus clock (BCLK)	MOSC, SOSC, HOCO, MOCO, LOCO, PLL	External bus	Up to 120 MHz Division ratios: 1, 2, 4, 8, 16, 32, 64
EBCLK pin output (EBCLK)	BCLK or 1/2 BCLK	EBCLK pin	Up to 60 MHz Division ratios: 1, 2
SDCLK pin output (SDCLK)	BCLK	SDCLK pin	Up to 120 MHz
USB clock (UCLK)	PLL	USB	48 MHz Division ratios: 3, 4, 5
USB-PHY clock (USBMCLK)	MOSC	USB-PHY	12, 20, 24 MHz
CAN clock (CANMCLK)	MOSC	CAN	8 to 24 MHz
LCD_CLK pin output (LCD_CLK) and graphic LCD pixel clock (PXCLK)	LCD_EXTCLK, PLL output	LCD_CLK pin, peripheral module (Graphics LCD Controller)	Up to 54 MHz (parallel RGB) Up to 60 MHz (serial RGB) LCD_CLK division ratios: 1, 2, 3, 4, 5, 6, 7, 8, 9, 12, 16, 24, 32 LCD_CLK : PXCLK = 1:1 (parallel RGB) LCD_CLK : PXCLK = 4:1 (serial RGB)
AGT clock (AGTSCLK, AGTLCLK)	SOSC, LOCO	AGT	32.768 MHz
CAC main clock (CACMCLK)	MOSC	CAC	Up to 24 MHz
CAC sub-clock (CACSCLK)	SOSC	CAC	32.768 kHz
CAC LOCO clock (CACLCLK)	LOCO	CAC	32.768 kHz
CAC MOCO clock (CACMOCLK)	MOCO	CAC	8 MHz
CAC HOCO clock (CACHCLK)	HOCO	CAC	16, 18, 20 MHz
CAC IWDTLOCO clock (CACILCLK)	IWDTLOCO	CAC	15 kHz
RTC clock (RTCSCLK, RTCLCLK)	SOSC, LOCO	RTC	32.768 kHz
IWDT clock (IWDTCLK)	IWDTLOCO	IWDT	15 kHz
SysTick timer clock (SYSTICCLK)	LOCO	SysTick timer	32.768 kHz
JTAG clock (JTAGTCK)	TCK pin	JTAG	Up to 25 MHz

Table 9.2 内部时钟的时钟生成电路的规格（2of3）

Parameter	时钟源	时钟电源	Specifications
外设模块时钟A(PCLKA)	MOSC, SOSC, HOCO, MOCO, LOCO, PLL	外围模块（ETHERC、EDMAC、USBHS、QSPI、SPI、SCI, SCE7, GLCDC, SDHI, CRC、JPEG引擎、DRW、IrDA、GPT bus-clock)	高达120MHz*2 Division ratios: 1, 2, 4, 8, 16, 32, 64
外设模块时钟B(PCLKB)	MOSC, SOSC, HOCO, MOCO, LOCO, PLL	外围模块（IIC、SSIE、SRC、DOC、CAC、CAN、DAC12、POEG、CTSU、AGT、备用SRAM、ELC、IO端口、RTC、WDT, IWDT, ADC12, KINT, USBFS, ACMPHS, TSN, PDC)	高达60MHz Division ratios: 1, 2, 4, 8, 16, 32, 64
外设模块时钟C(PCLKC)	MOSC, SOSC, HOCO, MOCO, LOCO, PLL	外设模块（ADC12转换时钟）	高达60MHz Division ratios: 1, 2, 4, 8, 16, 32, 64
外设模块时钟D(PCLKD)	MOSC, SOSC, HOCO, MOCO, LOCO, PLL	外围模块（GPT计数时钟）	高达120MHz Division ratios: 1, 2, 4, 8, 16, 32, 64
闪存接口时钟(FCLK)	MOSC, SOSC, HOCO, MOCO, LOCO, PLL	闪存接口	4至60MHz(PE)最高60 MHz（读取）*1 Division ratios: 1, 2, 4, 8, 16, 32, 64
外部总线时钟(BCLK)	MOSC, SOSC, HOCO, MOCO, LOCO, PLL	外部总线	高达120MHz Division ratios: 1, 2, 4, 8, 16, 32, 64
EBCLK引脚输出(EBCLK)	BCLK or 1/2 BCLK	EBCLK pin	高达60MHz Division ratios: 1, 2
SDCLK 引脚输出(SDCLK	)BCLK	SDCLK pin	高达120MHz
USB时钟(UCLK)	PLL	USB	48 MHz Division ratios: 3, 4, 5
USB-PHY clock (USBMCLK)	MOSC	USB-PHY	12, 20, 24 MHz
CAN时钟(CANMCLK)	MOSC	CAN	8 to 24 MHz
LCD_CLK引脚输出(LCD_CLK)和图形LCD像素时钟(PXCLK)	LCD_EXTCLK, PLL output	LCD_CLK引脚，外围模块（图形LCD控制器）	高达54MHz（并行RGB） 高达60MHz（串行RGB） LCD_CLK division ratios: 1, 2, 3, 4, 5, 6, 7, 8, 9, 12, 16, 24, 32 LCD_CLK : PXCLK = 1:1 (parallel RGB) LCD_CLK : PXCLK = 4:1 (serial RGB)
AGT clock (AGTSCLK, AGTLCLK)	SOSC, LOCO	AGT	32.768 MHz
CAC主时钟(CACMCLK)	MOSC	CAC	高达24MHz
CAC sub-clock (CACSCLK)	SOSC	CAC	32.768 kHz
CACLOCO时钟(CACLCLK)	LOCO	CAC	32.768 kHz
CACMOCO时钟(CACMOCLK)	MOCO	CAC	8 MHz
CACHOCO时钟(CACHCLK)	HOCO	CAC	16, 18, 20 MHz
CACIWDTLOCO时钟(CACILCLK)	IWDTLOCO	CAC	15 kHz
RTC clock (RTCSCLK, RTCLCLK)	SOSC, LOCO	RTC	32.768 kHz
IWDT clock (IWDTCLK)	IWDTLOCO	IWDT	15 kHz
SysTick定时器时钟(SYSTICCLK)	LOCO	SysTick timer	32.768 kHz
JTAG clock (JTAGTCK)	TCK pin	JTAG	高达25MHz

Table 9.2 Specifications of the clock generation circuit for the internal clocks (3 of 3)

Parameter	Clock sources	Clock supply	Specifications
Clock and buzzer output (CLKOUT)	MOSC, SOSC, LOCO, MOCO, HOCO	CLKOUT pin	Up to 24 MHz Division ratios: 1, 2, 4, 8, 16, 32, 64, 128
Serial wire clock (SWCLK)	SWCLK pin	OCD	Up to 25 MHz
Trace clock (TRCLK)	MOSC, SOSC, HOCO, MOCO, LOCO, PLL	CPU-OCD	Up to 60 MHz Division ratios: 1, 2, 4
TCLK pin output (TCLK)	1/2 TRCLK	TCLK pin	Up to 30 MHz

Note: Constraints on clock frequency settings: ICLK ≥ PCLKA ≥ PCLKB, PCLKD ≥ PCLKA ≥ PCLKB
Constraints on clock frequency ratio (N: integer, and up to 64):
ICLK:FCLK = N:1, ICLK:BCLK = N:1, ICLK:PCLKA = N:1, ICLK:PCLKB = N:1
ICLK:PCLKC = N:1 or 1:N, ICLK:PCLKD = N:1 or 1:N
If the A/D converter is enabled, clock frequency ratio is constrained as below:
PCLKB:PCLKC = 1:1 or 1:2 or 1:4 or 2:1 or 4:1 or 8:1.

Note: Clocks have a permissible frequency range. See Table 9.2.
Flash memory and SRAM also have a permissible operating frequency range in each wait cycle setting. See section 53, SRAM, section 55, Flash Memory.
Those clock frequency ranges must be satisfied even if the HOCO has its maximum or minimum frequency. See section 60, Electrical Characteristics.

Note: If PLL reference clock source is HOCO, PLL multiplication setting must be set to 120 - 240 MHz in consideration of HOCO frequency (minimum/maximum).

Note 1. The minimum FCLK frequency is 4 MHz in Programming/Erasure (P/E) mode.
Note 2. When using ETHERC, the PCLKA frequency is in the range 12.5 MHz ≤ PCLKA ≤ 120 MHz.
When using ETHERC, GLCDC, DRW, and JPEG, PCLKA = ICLK.

Table 9.2 内部时钟的时钟生成电路规格(3of3)

Parameter	时钟源	时钟电源	Specifications
时钟和蜂鸣器输出(CLKOUT)	MOSC, SOSC, LOCO, MOCO, HOCO	CLKOUT pin	高达24MHz Division ratios: 1, 2, 4, 8, 16, 32, 64, 128
串行线时钟(SWCLK)	SWCLK pin	OCD	高达25MHz
跟踪时钟(TRCLK)	MOSC, SOSC, HOCO, MOCO, LOCO, PLL	CPU-OCD	高达60MHz Division ratios: 1, 2, 4
TCLK引脚输出(TCLK)	1/2 TRCLK	TCLK pin	高达30MHz

Note: 时钟频率设置约束：ICLK≥PCLKA≥PCLKB，PCLKD≥PCLKA≥PCLKB
时钟频率比的约束（N：整数，最大为64）：
ICLK:FCLK=N:1 ICLK:BCLK=N:1 ICLK:PCLKA=N:1 ICLK:PCLKB=N:1ICLK:PCLKC=N:1或1:N ICLK:PCLKD=N:1或1:N如果启用AD转换器，则时钟频率比限制如下：
PCLKB:PCLKC = 1:1 or 1:2 or 1:4 or 2:1 or 4:1 or 8:1.

Note: 时钟具有允许的频率范围。见表9.2。
闪存和SRAM在每个等待周期设置中也有一个允许的工作频率范围。参见第53节，SRAM，第55节，闪存。即使HOCO具有其最大或最小频率，也必须满足这些时钟频率范围。见第60节，
电气特性。

Note: 如果PLL参考时钟源是HOCO，考虑HOCO频率（最小最大），PLL倍频设置必须设置为120240MHz。

Note 1. 在编程擦除(PE)模式下，最小FCLK频率为4MHz。
Note 2. 使用ETHERC时，PCLKA频率在12.5MHz≤PCLKA≤120MHz范围内。
使用ETHERC、GLCDC、DRW和JPEG时，PCLKA=ICLK。

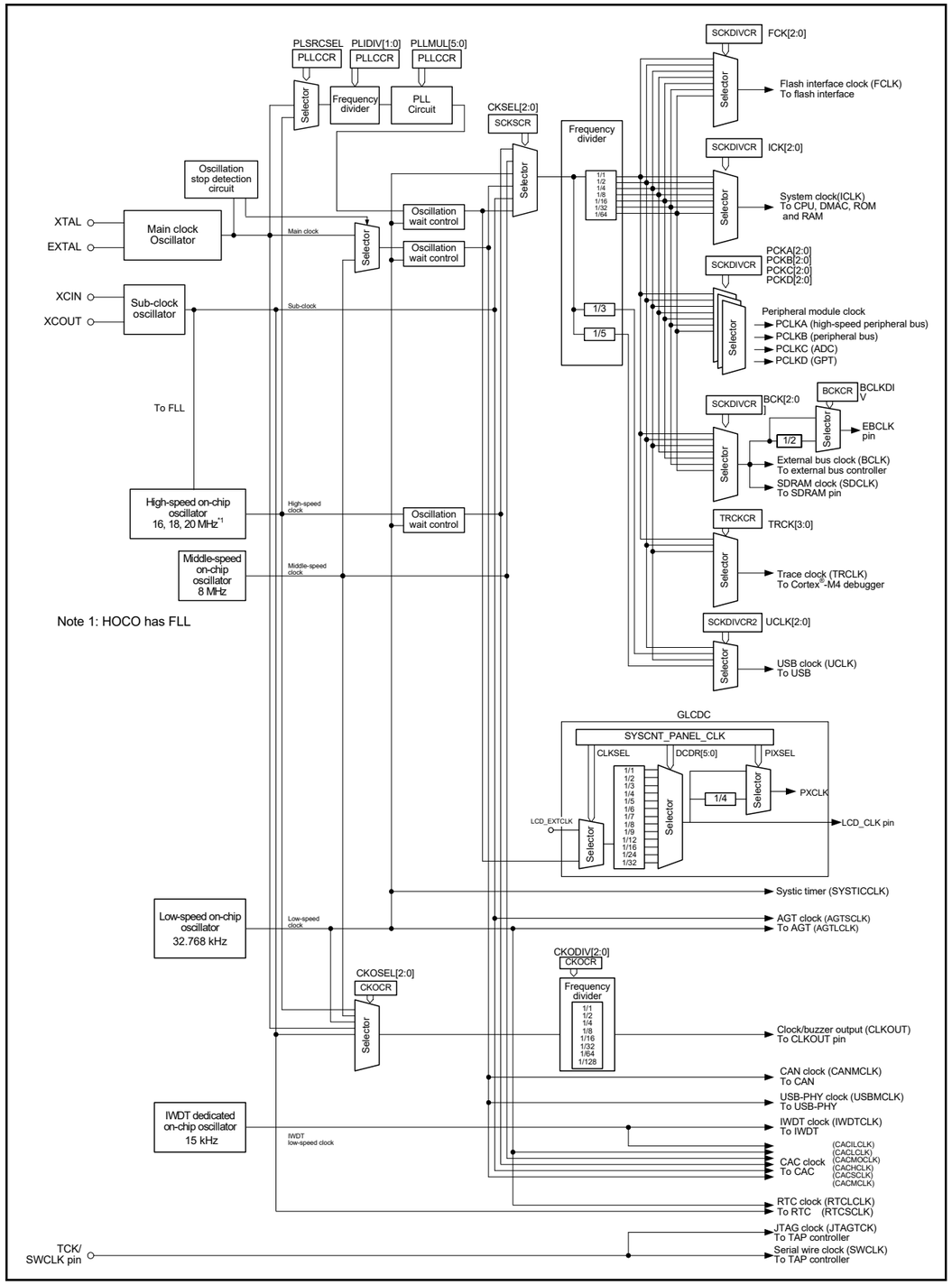


Figure 9.1 Clock generation circuit block diagram

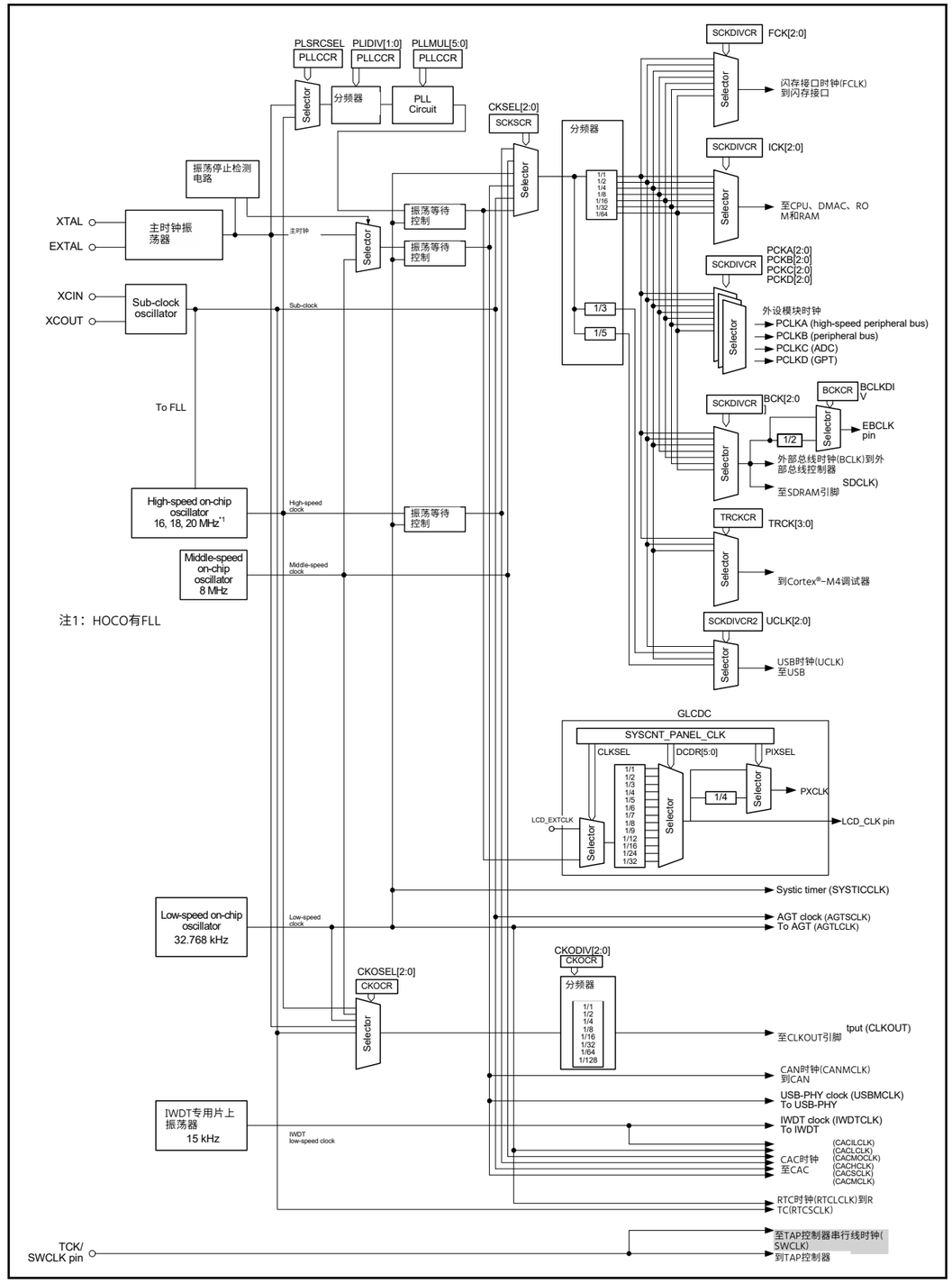


Figure 9.1 时钟产生电路框图

Table 9.3 Clock Generation Circuit I/O pins

Pin name	I/O	Description
XTAL	Output	Crystal resonator connections The EXTAL pin can also be used to input an external clock. For details, section 9.3.2, External Clock Input.
EXTAL	Input	
XCIN	Input	32.768-kHz crystal resonator connection
XCOUT	Output	
TCK/SWCLK	Input	JTAG clock input
EBCLK	Output	External bus clock (EBCLK) supply for external devices
SDCLK	Output	SDRAM clock (SDCLK) supply for external devices
CLKOUT	Output	CLKOUT and BUZZER clock output

9.2 Register Descriptions

9.2.1 System Clock Division Control Register (SCKDIVCR)

Address(es): SYSTEM.SCKDIVCR 4001 E020h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	FCK[2:0]			—	ICK[2:0]			—	—	—	—	—	BCK[2:0]		
Value after reset:	0	0	1	0	0	0	1	0	0	0	0	0	0	0	1	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	PCKA[2:0]			—	PCKB[2:0]			—	PCKC[2:0]			—	PCKD[2:0]		
Value after reset:	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	PCKD[2:0]	Peripheral Module Clock D (PCLKD) Select*4	b2 b0 0 0 0: ×1/1 0 0 1: ×1/2 0 1 0: ×1/4 0 1 1: ×1/8 1 0 0: ×1/16 1 0 1: ×1/32 1 1 0: ×1/64. Other settings are prohibited.	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6 to b4	PCKC[2:0]	Peripheral Module Clock C (PCLKC) Select*4	b6 b4 0 0 0: ×1/1 0 0 1: ×1/2 0 1 0: ×1/4 0 1 1: ×1/8 1 0 0: ×1/16 1 0 1: ×1/32 1 1 0: ×1/64. Other settings are prohibited.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Table 9.3 时钟生成电路IO引脚

引脚名称	I/O	Description
XTAL	Output	晶体谐振器连接 EXTAL引脚也可用于输入外部时钟。有关详细信息，请参阅第9.3.2节，外部时钟输入。
EXTAL	Input	
XCIN	Input	32.768kHz晶体谐振器连接
XCOUT	Output	
TCK/SWCLK	Input	JTAG时钟输入
EBCLK	Output	为外部设备提供外部总线时钟(EBCLK)
SDCLK	Output	为外部设备提供SDRAM时钟(SDCLK)
CLKOUT	Output	CLKOUT和BUZZER时钟输出

9.2 注册说明

9.2.1 系统时钟分频控制寄存器(SCKDIVCR)

Address(es): SYSTEM.SCKDIVCR 4001 E020h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	FCK[2:0]			—	ICK[2:0]			—	—	—	—	—	BCK[2:0]		
重置后的值:	0	0	1	0	0	0	1	0	0	0	0	0	0	0	1	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	PCKA[2:0]			—	PCKB[2:0]			—	PCKC[2:0]			—	PCKD[2:0]		
重置后的值:	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1	0

Bit	Symbol	位名称	Description	R/W
b2 to b0	PCKD[2:0]	外设模块时钟D(PCLKD)选择	b2 b0 0 0 0: ×1/1 0 0 1: ×1/2 0 1 0: ×1/4 0 1 1: ×1/8 1 0 0: ×1/16 1 0 1: ×1/32 10：×164。禁止其他设置。	R/W
b3	—	Reserved	该位读取为0。写入值应为0。	R/W
b6 to b4	PCKC[2:0]	外设模块时钟C(PCLKC)选择	b6 b4 0 0 0: ×1/1 0 0 1: ×1/2 0 1 0: ×1/4 0 1 1: ×1/8 1 0 0: ×1/16 1 0 1: ×1/32 10：×164。禁止其他设置。	R/W
b7	—	Reserved	该位读取为0。写入值应为0。	R/W

Bit	Symbol	Bit name	Description	R/W
b10 to b8	PCKB[2:0]	Peripheral Module Clock B (PCLKB) Select*3	b10 b8 0 0 0: ×1/1 0 0 1: ×1/2 0 1 0: ×1/4 0 1 1: ×1/8 1 0 0: ×1/16 1 0 1: ×1/32 1 1 0: ×1/64. Other settings are prohibited.	R/W
b11	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b14 to b12	PCKA[2:0]	Peripheral Module Clock A (PCLKA) Select*3	b14 b12 0 0 0: ×1/1 0 0 1: ×1/2 0 1 0: ×1/4 0 1 1: ×1/8 1 0 0: ×1/16 1 0 1: ×1/32 1 1 0: ×1/64. Other settings are prohibited.	R/W
b15	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b18 to b16	BCK[2:0]	External Bus Clock (BCLK) Select*2	b18 b16 0 0 0: ×1/1 0 0 1: ×1/2 0 1 0: ×1/4 0 1 1: ×1/8 1 0 0: ×1/16 1 0 1: ×1/32 1 1 0: ×1/64. Other settings are prohibited.	R/W
b23 to b19	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b26 to b24	ICK[2:0]	System Clock (ICLK) Select*1,*2,*3,*4,*5	b26 b24 0 0 0: ×1/1 0 0 1: ×1/2 0 1 0: ×1/4 0 1 1: ×1/8 1 0 0: ×1/16 1 0 1: ×1/32 1 1 0: ×1/64. Other settings are prohibited.	R/W
b27	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b30 to b28	FCK[2:0]	Flash Interface Clock (FCLK) Select*1	b30 b28 0 0 0: ×1/1 0 0 1: ×1/2 0 1 0: ×1/4 0 1 1: ×1/8 1 0 0: ×1/16 1 0 1: ×1/32 1 1 0: ×1/64. Other settings are prohibited.	R/W
b31	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Note 1. The following association is required between the frequencies of the system clock (ICLK) and the flash interface clock (FCLK):
ICLK:FCLK = N:1 (N: integer)
If a setting where ICLK < FCLK is written, the write is ignored.

Note 2. The following association is required between the frequencies of the system clock (ICLK) and the external bus clock (BCLK):
ICLK:BCLK = N:1 (N: integer)
If a setting where ICLK < BCLK is written, the write is ignored.

Note 3. The following association is required between the frequencies of the system clock (ICLK) and the peripheral module clocks (PCLKA, PCLKB): ICLK:PCLKA = N:1, ICLK:PCLKB = N:1 (N: integer)
If a setting where ICLK < PCLKA or ICLK < PCLKB is written, the write is ignored.

Note 4. The following association is required between the frequencies of the system clock (ICLK) and the peripheral module clocks (PCLKC, PCLKD): ICLK:PCLKC, PCLKD = N:1 or 1:N (N: integer).

Note 5. The frequency of the system clock (ICLK) is limited to the flash wait cycle register (FLWT). Refer to section 55, Flash Memory.

Bit	Symbol	位名称	Description	R/W
b10 to b8	PCKB[2:0]	外设模块时钟B(PCLKB)选择	b10 b8 0 0 0: ×1/1 0 0 1: ×1/2 0 1 0: ×1/4 0 1 1: ×1/8 1 0 0: ×1/16 1 0 1: ×1/32 10：×164。禁止其他设置。	R/W
b11	—	Reserved	该位读取为0。写入值应为0。	R/W
b14 to b12	PCKA[2:0]	外设模块时钟A(PCLKA)选择	b14 b12 0 0 0: ×1/1 0 0 1: ×1/2 0 1 0: ×1/4 0 1 1: ×1/8 1 0 0: ×1/16 1 0 1: ×1/32 10：×164。禁止其他设置。	R/W
b15	—	Reserved	该位读取为0。写入值应为0。	R/W
b18 to b16	BCK[2:0]	外部总线时钟(BCLK) Select*2	b18 b16 0 0 0: ×1/1 0 0 1: ×1/2 0 1 0: ×1/4 0 1 1: ×1/8 1 0 0: ×1/16 1 0 1: ×1/32 10：×164。禁止其他设置。	R/W
b23 to b19	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b26 to b24	ICK[2:0]	系统时钟(ICLK) Select*1,*2,*3,*4,*5	b26 b24 0 0 0: ×1/1 0 0 1: ×1/2 0 1 0: ×1/4 0 1 1: ×1/8 1 0 0: ×1/16 1 0 1: ×1/32 10：×164。禁止其他设置。	R/W
b27	—	Reserved	该位读取为0。写入值应为0。	R/W
b30 to b28	FCK[2:0]	闪存接口时钟(FCLK) Select*1	b30 b28 0 0 0: ×1/1 0 0 1: ×1/2 0 1 0: ×1/4 0 1 1: ×1/8 1 0 0: ×1/16 1 0 1: ×1/32 10：×164。禁止其他设置。	R/W
b31	—	Reserved	该位读取为0。写入值应为0。	R/W

Note 1. 系统时钟(ICLK)和闪存接口时钟(FCLK)的频率之间需要以下关联：
ICLK:FCLK = N:1 (N: integer)
如果写入ICLK<FCLK的设置，则忽略写入。

Note 2. 系统时钟(ICLK)和外部总线时钟(BCLK)的频率之间需要以下关联：
ICLK:BCLK = N:1 (N: integer)
如果写入ICLK<BCLK的设置，则忽略写入。

Note 3. 系统时钟(ICLK)和外围模块时钟(PCLKA PCLKB)的频率之间需要以下关联：ICLK:PCLKA=N:1 ICLK:PCLKB=N:1(N:integer)如果设置为写入ICLK<PCLKA或ICLK<PCLKB，写入被忽略。

Note 4. 系统时钟(ICLK)和外设模块时钟(PCLKC PCLKD)的频率之间需要以下关联：ICLK:PCLKC PCLKD=N:1或1:N(N:integer)。

Note 5. 系统时钟(ICLK)的频率仅限于闪存等待周期寄存器(FLWT)。请参阅第55节，闪存。

The SCKDIVCR register selects the frequencies of the system clock (ICLK), peripheral module clocks (PCLKA, PCLKB, PCLKC, PCLKD), flash interface clock (FCLK), external bus clock (BCLK), and SDRAM clock (SDCLK).

When the PLL is selected as the clock source, set the following modules into the module-stop state before changing the value of SCKDIVCR: ETHERC, EPTPC, EDMAC, SCE7, DRW, JPEG, GLCDC, GPT32EH, and GPT32E.

In addition, when changing any value in SCKDIVCR from a lower division ratio to a higher division ratio, wait at least 750 ns before changing the value. When changing any value from a higher division ratio to a lower division ratio, wait at least 250 ns after changing the value before starting subsequent processing.

The recommended method to measure the wait time is to do so in software. Be sure to consider the worst-case use conditions to ensure that the required wait time elapses.

Figure 9.2 shows an example flow for changing the value of SCKDIVCR.

PCKD[2:0] bits (Peripheral Module Clock D (PCLKD) Select)

The PCKD[2:0] bits select the frequency for peripheral module clock D (PCLKD).

PCKC[2:0] bits (Peripheral Module Clock C (PCLKC) Select)

The PCKC[2:0] bits select the frequency for peripheral module clock C (PCLKC).

PCKB[2:0] bits (Peripheral Module Clock B (PCLKB) Select)

The PCKB[2:0] bits select the frequency for peripheral module clock B (PCLKB).

PCKA[2:0] bits (Peripheral Module Clock A (PCLKA) Select)

The PCKA[2:0] bits select the frequency for peripheral module clock A (PCLKA).

BCK[2:0] bits (External Bus Clock (BCLK) Select)

The BCK[2:0] bits select the frequency for the external bus clock (BCLK) and the SDRAM clock (SDCLK).

ICK[2:0] bits (System Clock (ICLK) Select)

The ICK[2:0] bits select the frequency for the system clock for the CPU, DMAC, and DTC.

FCK[2:0] bits (Flash Interface Clock (FCLK) Select)

The FCK[2:0] bits select the frequency for the flash interface clock (FCLK).

SCKDIVCR寄存器选择系统时钟(ICLK)、外设模块时钟(PCLKA、
PCLKB、PCLKC、PCLKD)、闪存接口时钟(FCLK)、外部总线时钟(BCLK)和SDRAM时钟(SDCLK)。

WhenthePLLisselectedastheclocksource setthefollowingmodulesintothemodule-stopstatebeforechangingth evalueofSCKDIVCR:ETHERC EPTPC EDMAC SCE7 DRW JPEG GLCDC GPT32EH andGPT32E.

此外，将SCKDIVCR中的任何值从较低的分频比更改为较高的分频比时，在更改该值之前至少等待750ns。将任何值从较高的分频比更改为较低的分频比时，在更改该值后至少等待250ns，然后再开始后续处理。

测量等待时间的推荐方法是在软件中进行。请务必考虑最坏的使用条件，以确保经过所需的等待时间。

图9.2显示了更改SCKDIVCR值的示例流程。

PCKD[2:0]位（外设模块时钟D(PCLKD)选择）

PCKD[2:0]位选择外设模块时钟D(PCLKD)的频率。

PCKC[2:0]位（外设模块时钟C(PCLKC)选择）

PCKC[2:0]位选择外设模块时钟C(PCLKC)的频率。

PCKB[2:0]位（外设模块时钟B(PCLKB)选择）

PCKB[2:0]位选择外设模块时钟B(PCLKB)的频率。

PCKA[2:0]位（外设模块时钟A(PCLKA)选择）

PCKA[2:0]位选择外设模块时钟A(PCLKA)的频率。

BCK[2:0]位（外部总线时钟（BCLK）选择）

BCK[2:0]位选择外部总线时钟(BCLK)和SDRAM时钟(SDCLK)的频率。

ICK[2:0]位（系统时钟（ICLK）选择）

ICK[2:0]位选择CPU、DMAC和DTC的系统时钟频率。

FCK[2:0]位（闪存接口时钟(FCLK)选择）

FCK[2:0]位选择闪存接口时钟(FCLK)的频率。

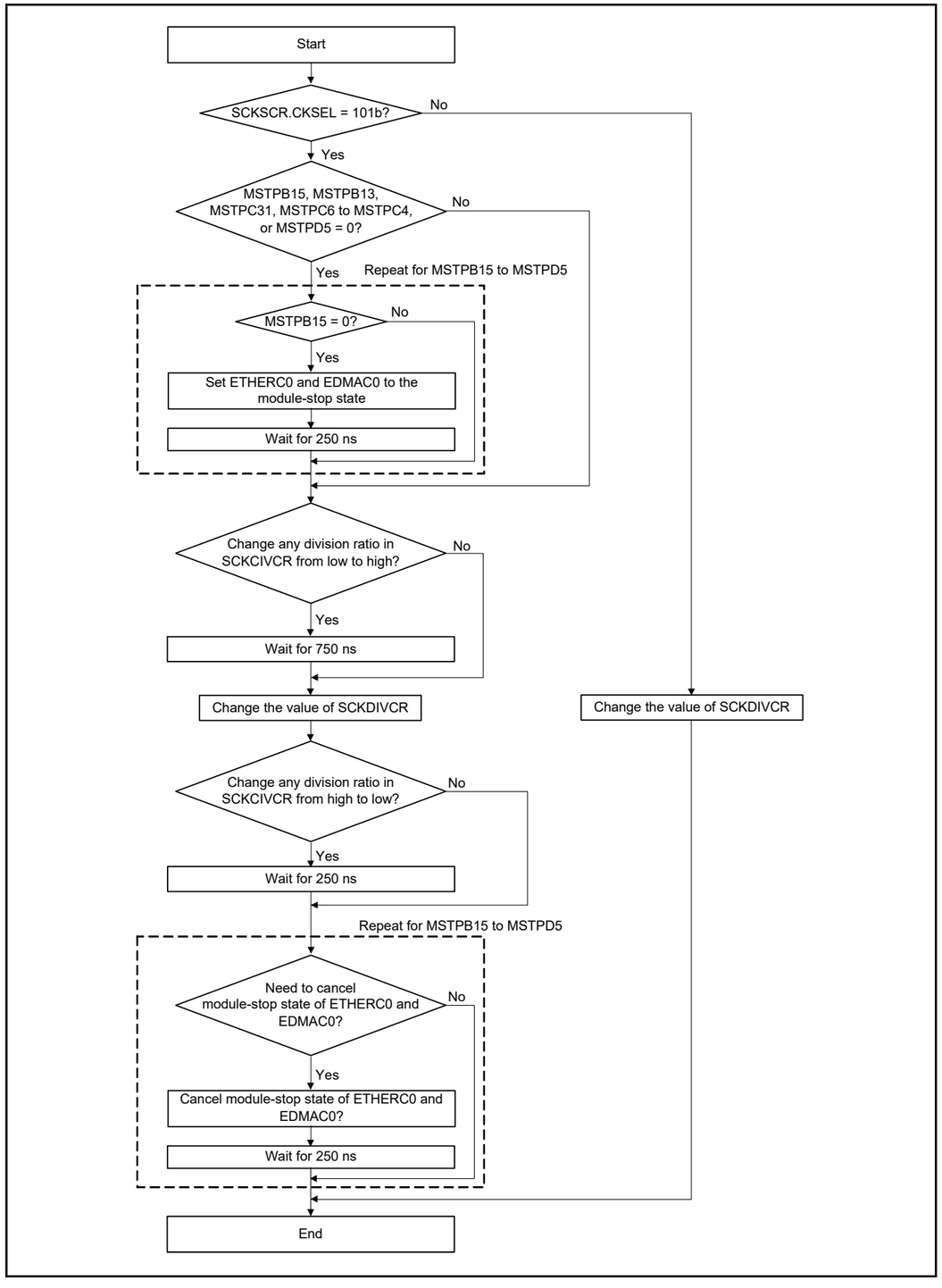


Figure 9.2 Example flow for changing the value of SCKDIVCR

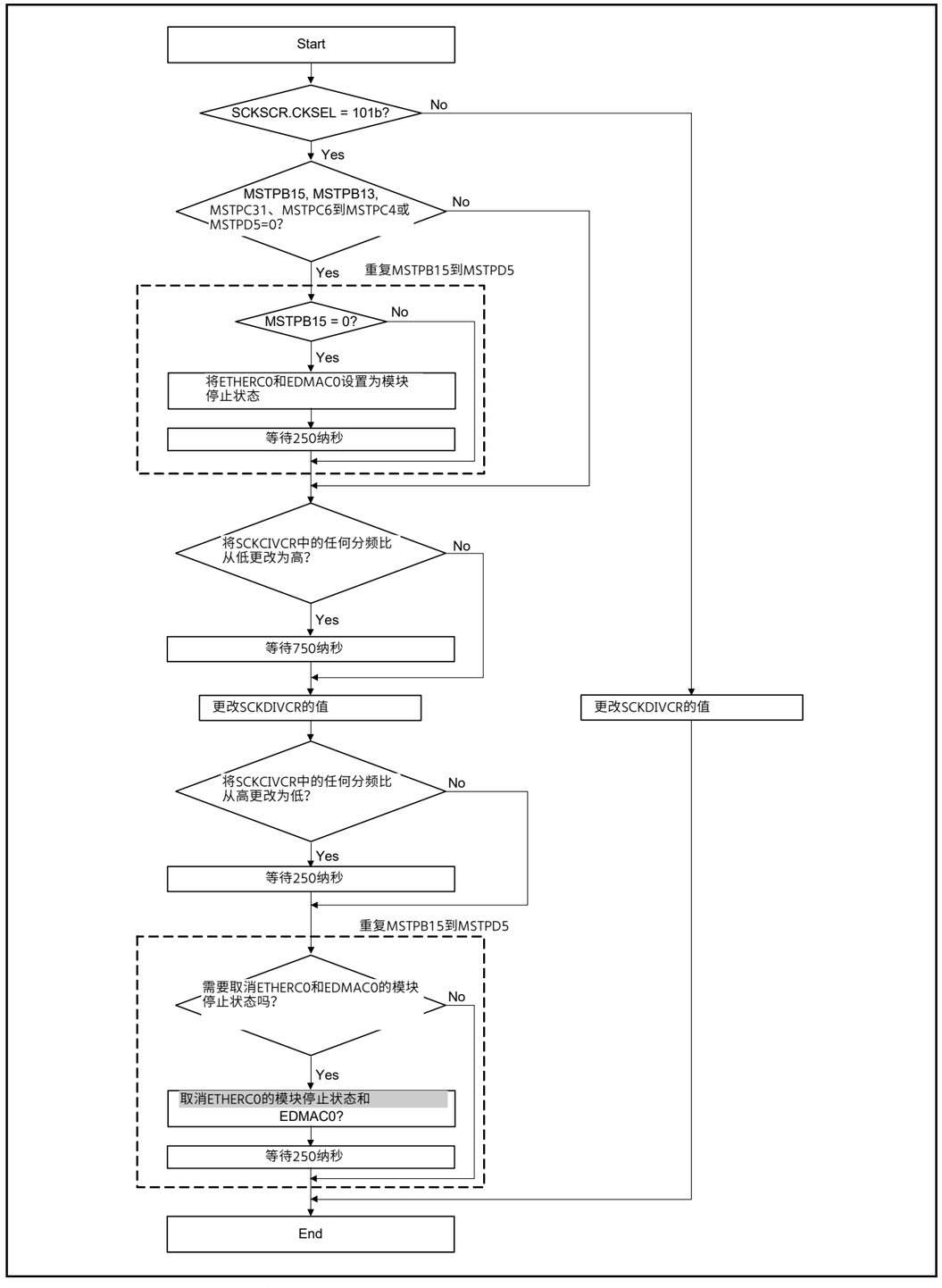


Figure 9.2 更改SCKDIVCR值的示例流程

9.2.2 System Clock Division Control Register 2 (SCKDIVCR2)

Address(es): SYSTEM.SCKDIVCR2 4001 E024h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	UCK[2:0]			—	—	—	—
Value after reset:	0	1	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6 to b4	UCK[2:0]	USB Clock (UCLK) Select	b6 b4 0 1 0: ×1/3 0 1 1: ×1/4 1 0 0: ×1/5. Other settings are prohibited.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Note: Do not write to SCKDIVCR2 and SCKSCR at the same time by 32-bit access.

The SCKDIVCR2 register selects the frequency of the USB clock (UCLK).

UCK[2:0] bits (USB Clock (UCLK) Select)

The UCK[2:0] bits select the frequency of the USB clock (UCLK). The duty ratio is 2:1 when ×1/3 is selected or 3:2 when ×1/5 is selected.

9.2.3 System Clock Source Control Register (SCKSCR)

Address(es): SYSTEM.SCKSCR 4001 E026h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	CKSEL[2:0]		
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Bit name	Description	R/W
b2 to b0	CKSEL[2:0]	Clock Source Select	b2 b0 0 0 0: HOCO 0 0 1: MOCO 0 1 0: LOCO 0 1 1: Main clock oscillator 1 0 0: Sub-clock oscillator 1 0 1: PLL. Other settings are prohibited.	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Do not write to SCKDIVCR2 and SCKSCR at the same time by 32-bit access.

The SCKSCR register selects the clock source for the system clock.

When changing the value of SCKSCR to either select or deselect the PLL, set the following modules into the module-stop state before changing the SCKSCR value: ETHERC, EPTPC, EDMAC, SCE7, DRW, JPEG, GLCDC, GPT32EH, GPT32E.

In addition, when changing the value of SCKSCR from the PLL to a different clock source, wait at least 750 ns before changing the value. When changing the value from a non-PLL clock source to the PLL, wait at least 250 ns after changing the value before starting subsequent processing.

9.2.2 系统时钟分频控制寄存器2(SCKDIVCR2)

Address(es): SYSTEM.SCKDIVCR2 4001 E024h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	UCK[2:0]			—	—	—	—
重置后的值:	0	1	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b3 to b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b6 to b4	UCK[2:0]	USB时钟(UCLK)选择	b6b4010：×13011：×1410 0：×15、禁止其他设置。	R/W
b7	—	Reserved	该位读取为0。写入值应为0。	R/W

Note: 不要通过32位访问同时写入SCKDIVCR2和SCKSCR。

SCKDIVCR2寄存器选择USB时钟(UCLK)的频率。

UCK[2:0]位（USB时钟(UCLK)选择）

UCK[2:0]位选择USB时钟(UCLK)的频率。选择×13时占空比为2:1，选择×15时占空比为3:2。

9.2.3 系统时钟源控制寄存器(SCKSCR)

Address(es): SYSTEM.SCKSCR 4001 E026h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	CKSEL[2:0]		
重置后的值:	0	0	0	0	0	0	0	1

Bit	Symbol	位名称	Description	R/W
b2 to b0	CKSEL[2:0]	时钟源选择	b2 b0 0 0 0: HOCO 0 0 1: MOCO 0 1 0: LOCO 0 1 1：主时钟振荡器 1 0 0: Sub-clock oscillator 01：锁相环。禁止其他设置 。	R/W
b7 to b3	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note: 不要通过32位访问同时写入SCKDIVCR2和SCKSCR。

SCKSCR寄存器选择系统时钟的时钟源。

当更改SCKSCR的值以选择或取消选择PLL时，在更改SCKSCR值之前将以下模块设置为modulestop状态：ETHERC、EPTPC、EDMAC、SCE7、DRW、JPEG、GLCDC、GPT32EH、GPT32E。

此外，当将SCKSCR的值从PLL更改为不同的时钟源时，在更改值之前至少等待750ns。将值从非PLL时钟源更改为PLL时，更改值后至少等待250ns，然后再开始后续处理。

The recommended method to measure the wait time is to do so in software. Be sure to consider the worst-case use conditions to ensure that the required wait time elapses.

Figure 9.3 shows an example flow for changing the value of SCKSCR.

CKSEL[2:0] bits (Clock Source Select)

The CKSEL[2:0] bits select the clock source for the following modules:

- System clock (ICLK)
- Peripheral module clocks (PCLKA, PCLKB, PCLKC, and PCLKD)
- Flash interface clock (FCLK)
- External bus clock (BCLK)
- SDRAM clock (SDCLK)
- USBFS and USBHS clock (UCLK).

The bits select from one of the following sources:

- Low-speed on-chip oscillator (LOCO)
- Middle-speed on-chip oscillator (MOCO)
- High-speed on-chip oscillator (HOCO)
- Main clock oscillator
- Sub-clock oscillator
- PLL circuit.

The clock sources should be switched when there are no occurring internal asynchronous interrupt.

Transitions to clock sources that are not in operation are prohibited.

测量等待时间的推荐方法是在软件中进行。请务必考虑最坏的使用条件，以确保经过所需的等待时间。

图9.3显示了更改SCKSCR值的示例流程。

CKSEL[2:0]位（时钟源选择）

CKSEL[2:0]位选择以下模块的时钟源：

- 系统时钟(ICLK)
- 外围模块时钟（PCLKA、PCLKB、PCLKC和PCLKD）
- 闪存接口时钟(FCLK)
- 外部总线时钟(BCLK)
- SDRAM clock (SDCLK)
- USBFS和USBHS时钟(UCLK)。

这些位从以下来源之一中选择：

- Low-speed on-chip oscillator (LOCO)
- Middle-speed on-chip oscillator (MOCO)
- High-speed on-chip oscillator (HOCO)
- 主时钟振荡器
- Sub-clock oscillator
- PLL circuit.

当没有发生内部异步中断时，应切换时钟源。

禁止转换到未运行的时钟源。

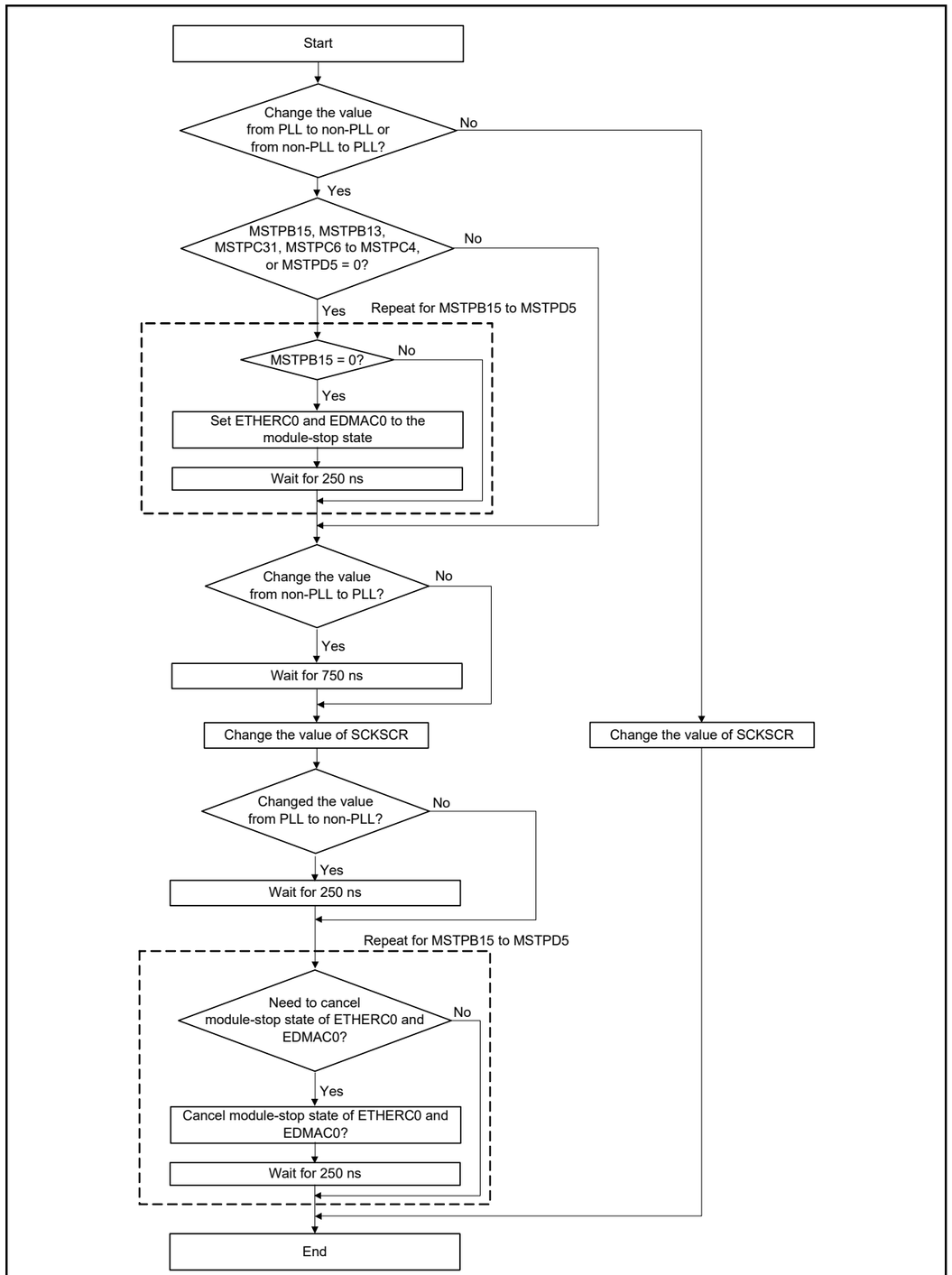


Figure 9.3 Example flow for changing the value of SCKSCR

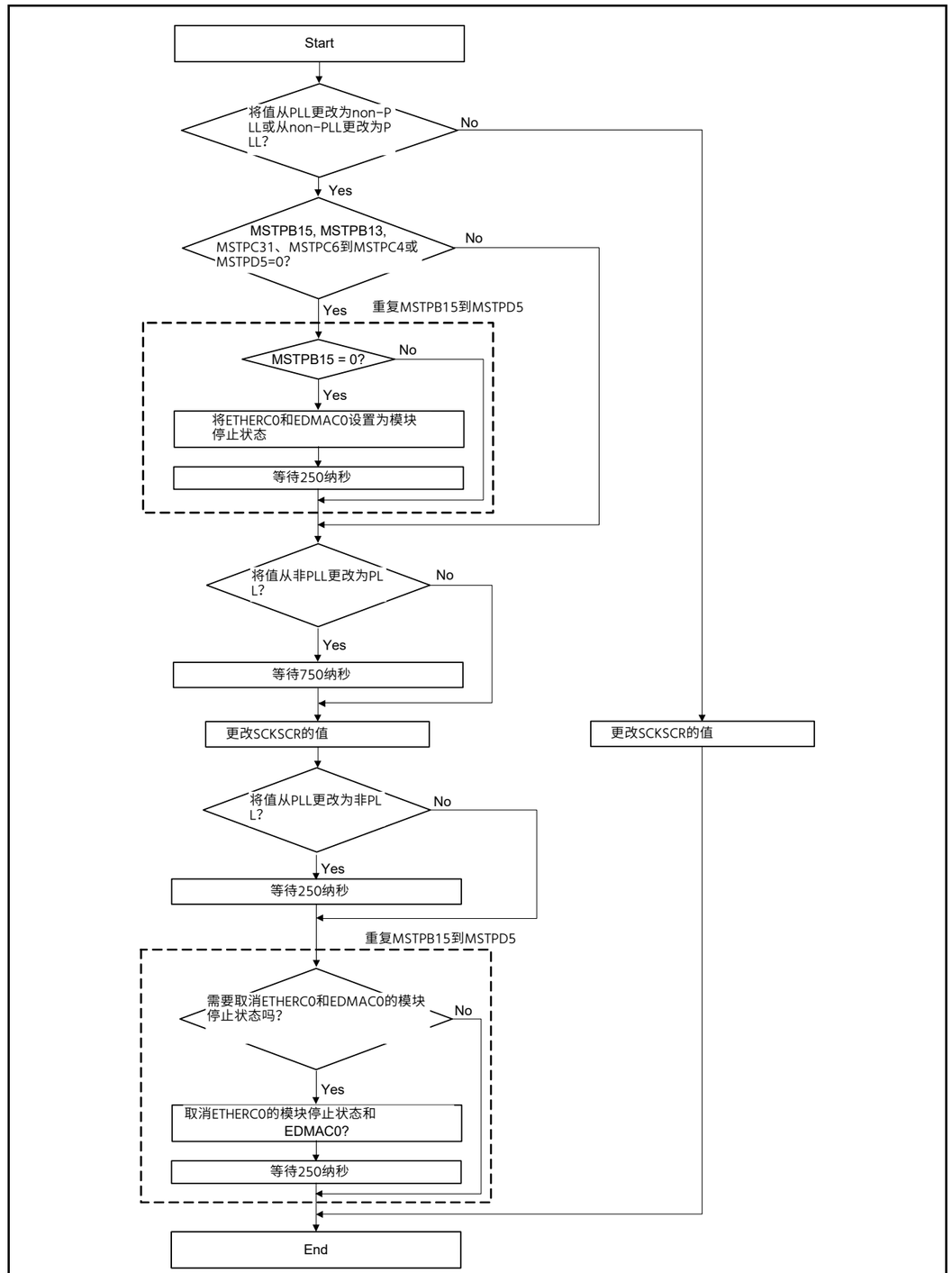


Figure 9.3 更改SCKSCR值的示例流程

9.2.4 PLL Clock Control Register (PLLCCR)

Address(es): SYSTEM.PLLCCR 4001 E028h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	PLLMUL[5:0]						—	—	—	PLSRC SEL	—	—	PLIDIV[1:0]	
Value after reset:	0	0	0	1	0	0	1	1	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	PLIDIV[1:0]	PLL Input Frequency Division Ratio Select*1	b1 b0 0 0: × 1 0 1: × 1/2 1 0: × 1/3 1 1: Setting prohibited.	R/W
b3, b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	PLSRCSEL	PLL Clock Source Select	0: Main clock oscillator*4 1: HOCO.	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b13 to b8	PLLMUL[5:0]	PLL Frequency Multiplication Factor Select*2,*3	b13 b8 0 1 0 0 1 1: × 10.0 0 1 0 1 0 0: × 10.5 0 1 0 1 0 1: × 11.0 … 0 1 1 1 0 0: × 14.5 0 1 1 1 0 1: × 15.0 0 1 1 1 1 0: × 15.5 … 1 1 1 0 1 0: × 29.5 1 1 1 0 1 1: × 30.0. Other settings are prohibited.	R/W
b15, b14	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. PLIDIV[1:0] must be set so that the frequency of the PLL input signal is within the range listed in Table 9.1.
Note 2. PLLMUL[5:0] must be set so that the frequency of the PLL output signal is within the range listed in Table 9.1.
Note 3. PLLMUL[5:0] should be set up to 20 when oscillation stop detection function is enabled and input frequency less than 12 MHz is used.
Note 4. PLSRCSEL must be set to 0 when using UCLK.

The PLLCCR register sets up the operation of the PLL circuit. Writing to the PLLCCR is prohibited when the PLL is operating (when the PLLCR.PLLSTP bit is 0).

PLIDIV[1:0] bits (PLL Input Frequency Division Ratio Select*1)

The PLIDIV[1:0] bits select the frequency division ratio for the PLL clock source.

PLSRCSEL bit (PLL Clock Source Select)

The PLSRCSEL bit selects the clock source for the PLL.

PLLMUL[5:0] bits (PLL Frequency Multiplication Factor Select*2,*3)

The PLLMUL[5:0] bits select the frequency multiplication factor for the PLL circuit.

9.2.4 PLL时钟控制寄存器(PLLCCR)

Address(es): SYSTEM.PLLCCR 4001 E028h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	PLLMUL[5:0]						—	—	—	PLSRC SEL	—	—	PLIDIV[1:0]	
重置后的值:	0	0	0	1	0	0	1	1	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b1, b0	PLIDIV[1:0]	PLL输入分频 Ratio Select*1	b1 b0 0 0: × 1 0 1: × 1/2 1 0: × 1/3 1 1：禁止设置。	R/W
b3, b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b4	PLSRCSEL	PLL时钟源选择	0：主时钟振荡器*41：HOCO。	R/W
b7 to b5	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b13 to b8	PLLMUL[5:0]	PLL倍频 Factor Select*2,*3	b13 b8 0 1 0 0 1 1: × 10.0 0 1 0 1 0 0: × 10.5 0 1 0 1 0 1: × 11.0 … 0 1 1 1 0 0: × 14.5 0 1 1 1 0 1: × 15.0 0 1 1 1 1 0: × 15.5 … 1 1 1 0 1 0: × 29.5 11：×30.0。禁止其他设置。	R/W
b15, b14	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. PLIDIV[1:0]必须设置为使PLL输入信号的频率在表9.1中列出的范围内。
Note 2. 必须设置PLLMUL[5:0]，以使PLL输出信号的频率在表9.1中列出的范围内。
Note 3. PLLMUL[5:0]在使能振荡停止检测功能且输入频率小于12MHz时应设置为20。
Note 4. 使用UCLK时PLSRCSEL必须设置为0。

PLLCCR寄存器设置PLL电路的操作。当PLL运行时（当PLLCR.PLLSTP位为0时），禁止写入PLLCCR。

PLIDIV[1:0]位（PLL输入分频比选择*1）

PLIDIV[1:0]位选择PLL时钟源的分频比。

PLSRCSEL位（PLL时钟源选择）

PLSRCSEL位选择PLL的时钟源。

PLLMUL[5:0]位（PLL倍频因子选择*2 *3）

PLLMUL[5:0]位选择PLL电路的倍频因子。

9.2.5 PLL Control Register (PLLCR)

Address(es): SYSTEM.PLLCR 4001 E02Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	PLLSTP
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Bit name	Description	R/W
b0	PLLSTP	PLL Stop Control	0: Operate the PLL 1: Stop the PLL.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The PLLCR register controls the operation of the PLL circuit.

PLLSTP bit (PLL Stop Control)

The PLLSTP bit starts or stops the PLL circuit. When selecting the main clock oscillator as the clock source for the PLL in the PLLCCR.PLSRCSEL bit, you must also set the Main Clock Oscillator Wait Control Register (MOSCWTCR).

After setting the PLLSTP bit to 0, confirm that the OSCSF.PLLSF bit is set to 1 before using the PLL clock. A fixed stabilization wait is required after setting the PLL to start operation. A fixed wait for oscillation to stop is also required.

The following constraints apply when starting and stopping operation:

- After stopping the PLL, confirm that the OSCSF.PLLSF bit is 0 before restarting the PLL
- Confirm that the PLL is operating and that the OSCSF.PLLSF bit is 1 before stopping the PLL
- Regardless of whether the PLL clock is selected as the system clock, after setting the PLL to start operation, confirm that the OSCSF.PLLSF is set to 1 before executing a WFI instruction to place the MCU in Software Standby or Deep Software Standby mode
- When a transition to Software Standby or Deep Software Standby mode is to follow a setting to stop the PLL, confirm that the OSCSF.PLLSF bit is cleared to 0 before executing the WFI instruction.

Writing 1 to PLLSTP is prohibited under the following condition:

- SCKSCR.CKSEL[2:0] = 101b (system clock source = PLL).

Make sure the following conditions apply before writing 0 to PLLSTP:

- When PLL source clock = MOSC, OSCSF.MOSCSF bit = 1
- When PLL source clock = HOCO, OSCSF.HOCOSF bit = 1.

9.2.6 External Bus Clock Control Register (BCKCR)

Address(es): SYSTEM.BCKCR 4001 E030h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	BCLKDIV
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	BCLKDIV	EBCLK Pin Output Select	0: BCLK 1: BCLK/2.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

9.2.5 PLL控制寄存器(PLLCR)

Address(es): SYSTEM.PLLCR 4001 E02Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	PLLSTP
重置后的值：	0	0	0	0	0	0	0	1

Bit	Symbol	位名称	Description	R/W
b0	PLLSTP	PLL停止控制	0：运行PLL1：停止PLL。	R/W
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

PLLCR寄存器控制PLL电路的操作。

PLLSTP位（PLL停止控制）

PLLSTP位启动或停止PLL电路。在PLLCCR.PLSRCSEL位中选择主时钟振荡器作为PLL的时钟源时，您还必须设置主时钟振荡器等待控制寄存器(MOSCWTCR)。

将PLLSTP位设置为0后，在使用PLL时钟之前确认OSCSF.PLLSF位设置为1。将PLL设置为开始操作后，需要一个固定的稳定等待。还需要固定等待振荡停止。

启动和停止操作时适用以下约束：

- 停止PLL后，在重启PLL之前确认OSCSF.PLLSF位为0
- 在停止PLL之前确认PLL正在运行并且OSCSF.PLLSF位为1
- 无论是否选择PLL时钟作为系统时钟，在设置PLL开始运行后，在执行WFI指令之前确认OSCSF.PLLSF设置为1，将MCU置于软件待机或深度软件待机模式
- 当转换到软件待机或深度软件待机模式要遵循停止PLL的设置时，在执行WFI指令之前确认OSCSF.PLLSF位被清零。

在以下情况下禁止向PLLSTP写入1：

- SCKSCR.CKSEL[2:0]=101b（系统时钟源=PLL）。

在将0写入PLLSTP之前，请确保满足以下条件：

- 当PLL源时钟=MOSC时，OSCSF.MOSCSF位=1
- 当PLL源时钟=HOCO时，OSCSF.HOCOSF位=1。

9.2.6 外部总线时钟控制寄存器(BCKCR)

Address(es): SYSTEM.BCKCR 4001 E030h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	BCLKDIV
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	BCLKDIV	EBCLK引脚输出选择	0: BCLK 1: BCLK/2.	R/W
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

The BCKCR register controls the external bus clock pin.

BCLKDIV bit (EBCLK Pin Output Select)

The BCLKDIV bit selects the clock signal for output from the EBCLK pin. The signal can be selected from either the BCLK clock with the frequency selected in the BCK[2:0] bits in SCKDIVCR or the BCLK clock divided by 2.

9.2.7 Main Clock Oscillator Control Register (MOSCCR)

Address(es): SYSTEM.MOSCCR 4001 E032h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	MOSTP
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Bit name	Description	R/W
b0	MOSTP	Main Clock Oscillator Stop	0: Operate the main clock oscillator*1 1: Stop the main clock oscillator.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. The MOMCR register must be set before setting MOSTP to 0.

The MOSCCR register controls the main clock oscillator.

MOSTP bit (Main Clock Oscillator Stop)

The MOSTP bit starts or stops the main clock oscillator. To start the main clock oscillator, set this bit to 0. When changing the value of the bit, only execute subsequent instructions after reading the bit to check that the value was updated. When using the main clock oscillator, you must set the Main Clock Oscillator Mode Oscillation Control Register (MOMCR) and the Main Clock Oscillator Wait Control Register (MOSCWTCR) before setting MOSTP to 0.

After setting the MOSTP bit to 0, confirm that the OSCSF.MOSCSF bit is set to 1 before using the main clock oscillator. A fixed stabilization wait is required after setting the main clock oscillator to start operation. A fixed wait for oscillation to stop is also required.

The following constraints apply when starting and stopping operation:

- After stopping the main clock oscillator, confirm that the OSCSF.MOSCSF bit is 0 before restarting the main clock oscillator
- Confirm that the main clock oscillator is operating and that the OSCSF.MOSCSF bit is 1 before stopping the main clock oscillator
- Regardless of whether the main clock oscillator is selected as the system clock, confirm that the OSCSF.MOSCSF bit is set to 1 before executing a WFI instruction to place the MCU in Software Standby or Deep Software Standby mode
- When a transition to Software Standby or Deep Software Standby mode is to follow a setting to stop the main clock oscillator, confirm that the OSCSF.MOSCSF bit is cleared to 0 before executing the WFI instruction.

Writing 1 to MOSTP is prohibited under the following conditions:

- SCKSCR.CKSEL[2:0] = 011b (system clock source = MOSC)
- PLLCCR.PLSRCSEL = 0 (PLL source clock = MOSC) and SCKSCR.CKSEL[2:0] = 101b (system clock source = PLL)
- PLLCCR.PLSRCSEL = 0 (PLL source clock = MOSC) and PLLCR.PLLSTP = 0 (PLL is operating).

BCKCR寄存器控制外部总线时钟引脚。

BCLKDIV位（EBCLK引脚输出选择）

BCLKDIV位选择用于从EBCLK引脚输出的时钟信号。信号可以从任一选择频率在SCKDIVCR的BCK[2:0]位中选择的BCLK时钟或BCLK时钟除以2。

9.2.7 主时钟振荡器控制寄存器(MOSCCR)

Address(es): SYSTEM.MOSCCR 4001 E032h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	MOSTP
重置后的值：	0	0	0	0	0	0	0	1

Bit	Symbol	位名称	Description	R/W
b0	MOSTP	主时钟振荡器停止	0：运行主时钟振荡器*11：停止主时钟振荡器。	R/W
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

注1.在将MOSTP设置为0之前，必须设置MOMCR寄存器。

MOSCCR寄存器控制主时钟振荡器。

MOSTP位（主时钟振荡器停止）

MOSTP位启动或停止主时钟振荡器。要启动主时钟振荡器，请将该位设置为0。更改该位的值时，仅在读取该位后执行后续指令以检查该值是否已更新。使用主时钟振荡器时，必须先设置主时钟振荡器模式振荡控制寄存器(MOMCR)和主时钟振荡器等待控制寄存器(MOSCWTCR)，然后再将MOSTP设置为0。

将MOSTP位设置为0后，在使用主时钟振荡器之前确认OSCSF.MOSCSF位设置为1。将主时钟振荡器设置为开始运行后，需要一个固定的稳定等待时间。还需要固定等待振荡停止。

启动和停止操作时适用以下约束：

- 停止主时钟振荡器后，在重新启动主时钟振荡器之前确认OSCSF.MOSCSF位为0
- 在停止主时钟振荡器之前，确认主时钟振荡器正在运行并且OSCSF.MOSCSF位为1
- 无论是否选择主时钟振荡器作为系统时钟，在执行WFI指令将MCU置于软件待机或深度软件待机模式之前，请确认OSCSF.MOSCSF位设置为1
- 当转换到软件待机或深度软件待机模式要遵循停止主时钟振荡器的设置时，在执行WFI指令之前确认OSCSF.MOSCSF位被清零。

在以下情况下禁止向MOSTP写入1：

- SCKSCR.CKSEL[2:0]=011b（系统时钟源=MOSC）
- PLLCCR.PLSRCSEL=0（PLL源时钟=MOSC）和SCKSCR.CKSEL[2:0]=101b（系统时钟源=PLL）
- PLLCCR.PLSRCSEL=0（PLL源时钟=MOSC）和PLLCR.PLLSTP=0（PLL正在运行）。

9.2.8 Subclock Oscillator Control Register (SOSCCR)

Address(es): SYSTEM.SOSCCR 4001 E480h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	SOSTP
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	SOSTP	Sub-Clock Oscillator Stop	0: Operate the sub-clock oscillator*1 1: Stop the sub-clock oscillator.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. The SOMCR register must be set before setting SOSTP to 0.

The SOSCCR register controls the sub-clock oscillator.

SOSTP bit (Sub-Clock Oscillator Stop)

The SOSTP bit starts or stops the sub-clock oscillator. When changing the value of the bit, only execute subsequent instructions after reading the bit to check that the value was updated. Use the SOSTP bit when using the sub-clock oscillator as the source for a peripheral module, for example the RTC. When using the sub-clock oscillator, you must set the Sub-Clock Oscillator Mode Control Register (SOMCR) before setting SOSTP to 0.

After setting SOSTP to 0, only use the sub-clock oscillator after the sub-clock oscillation stabilization wait time (tSUBOSCOWT) elapses. A fixed stabilization wait is required after setting the sub-clock oscillator to start operation. A fixed wait for oscillation to stop is also required.

The following constraints apply when starting and stopping operation:

- After stopping the sub-clock oscillator, allow a stop interval of at least 5 SOSC cycles before restarting it
- Confirm that sub-clock oscillation is stable before stopping the sub-clock oscillator
- Regardless of whether the sub-clock oscillator is selected as the system clock, confirm that sub-clock oscillation is stable before executing a WFI instruction to place the MCU in Software Standby mode
- When a transition to Software Standby mode is to follow a setting to stop the sub-clock oscillator, wait for at least 3 SOSC cycles after the stop setting before executing the WFI instruction.

Writing 1 to SOSTP is prohibited under the following condition:

- SCKSCR.CKSEL[2:0] = 100b (system clock source = SOSC).

9.2.9 Low-Speed On-Chip Oscillator Control Register (LOCOCR)

Address(es): SYSTEM.LOCOCR 4001 E490h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	LCSTP
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	LCSTP	LOCO Stop	0: Operate the LOCO clock 1: Stop the LOCO clock.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The LOCOCR register controls the LOCO clock.

9.2.8 副时钟振荡器控制寄存器(SOSCCR)

Address(es): SYSTEM.SOSCCR 4001 E480h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	SOSTP
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	SOSTP	副时钟振荡器停止	0：运行副时钟振荡器*11：停止副时钟振荡器。	R/W
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 在将SOSTP设置为0之前，必须设置SOMCR寄存器。

SOSCCR寄存器控制副时钟振荡器。

SOSTP位（副时钟振荡器停止）

SONTP位启动或停止副时钟振荡器。更改位的值时，仅在读取该位后执行后续指令以检查该值是否已更新。当使用副时钟振荡器作为外围模块（例如RTC）的源时，使用SOTP位。使用副时钟振荡器时，必须先设置副时钟振荡器模式控制寄存器(SOMCR)，然后再将SOSTP设置为0。

将SOSTP设置为0后，仅在副时钟振荡稳定等待时间(tSUBOSCOWT)过后才使用副时钟振荡器。设置副时钟振荡器开始运行后，需要一个固定的稳定等待。还需要固定等待振荡停止。

启动和停止操作时适用以下约束：

- 停止子时钟振荡器后，在重新启动之前允许至少5个SOSC周期的停止间隔
- 在停止副时钟振荡器之前确认副时钟振荡稳定
- 无论是否选择副时钟振荡器作为系统时钟，在执行WFI指令之前确认副时钟振荡稳定，使MCU进入软件待机模式
- 当转换到软件待机模式要遵循停止副时钟振荡器的设置时，至少等待3
  在停止设置之后执行WFI指令之前的SOSC循环。

在以下情况下禁止向SOTP写入1：

- SCKSCR.CKSEL[2:0]=100b（系统时钟源=SOSC）。

9.2.9 低速片上振荡器控制寄存器(LOCOCR)

Address(es): SYSTEM.LOCOCR 4001 E490h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	LCSTP
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	LCSTP	机车站	0：运行LOCO时钟1：停止LOCO时钟。	R/W
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

LOCOCR寄存器控制LOCO时钟。

LCSTP bit (LOCO Stop)

The LCSTP bit starts or stops the LOCO clock. After setting LCSTP bit to 0 to start the LOCO clock, only use the clock after the LOCO clock oscillation stabilization wait time (tLOCOWT) elapses. A fixed stabilization wait is required after setting the LOCO clock to start operation. A fixed wait for oscillation to stop is also required.

The following constraints apply when starting and stopping operation:

- After stopping the LOCO clock, allow a stop interval of at least 5 LOCO cycles before restarting it
- Confirm that LOCO oscillation is stable before stopping the LOCO clock
- Regardless of whether the LOCO clock is selected as the system clock, confirm that LOCO oscillation is stable before executing a WFI instruction to place the MCU in Software Standby or Deep Software Standby mode
- When a transition to Software Standby or Deep Software Standby mode is to follow a setting to stop the LOCO clock, wait for at least 3 LOCO cycles after the stop setting before executing the WFI instruction.

Writing 1 to LOSTP is prohibited under the following condition:

- SCKSCR.CKSEL[2:0] = 010b (system clock source = LOCO).

Because the LOCO clock measures the wait time for other oscillators, it continues to oscillate while measuring this time, regardless of the setting in LOCOCR.LCSTP. As a result, the LOCO clock might be unintentionally supplied even when the LCSTP is set to stop.

9.2.10 High-Speed On-Chip Oscillator Control Register (HOCOCR)

Address(es): SYSTEM.HOCOCR 4001 E036h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	HCSTP
Value after reset:	0	0	0	0	0	0	0	0/1*1

Bit	Symbol	Bit name	Description	R/W
b0	HCSTP	HOCO Stop	0: Operate the HOCO clock*2 1: Stop the HOCO clock.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. The HCSTP bit value after a reset is 0 when the OFS1.HOCOEN bit is 0. It is 1 when the OFS1.HOCOEN bit is 1.
Note 2. If you are using the HOCO (HCSTP = 0), you must set the OFS1.HOCOFRQ0[1:0] bits to the optimum value.

The HOCOCR register controls the HOCO clock.

HCSTP bit (HOCO Stop)

The HCSTP bit starts or stops the HOCO clock. After setting the HCSTP bit to 0 to start the HOCO clock, confirm that the OSCSF.HOSCSF bit is set to 1 before using the clock. When OFS1.HOCOEN is set to 0, confirm that the OSCSF.HOCOSF is set to 1 before using the HOCO clock. A fixed stabilization wait is required after setting the HOCO clock to start operation. A fixed wait for oscillation to stop is also required. For the HOCO to operate, the HOCO Wait Control Register (HOCOWTCR) must also be set.

The following constraints apply when starting and stopping operation:

- After stopping the HOCO, confirm that the OSCSF.HOCOSF bit is 0 before restarting the HOCO clock
- Confirm that the HOCO clock is operating and that the OSCSF.HOCOSF bit is 1 before stopping the HOCO clock
- Regardless of whether the HOCO clock is selected as the system clock, confirm that the OSCSF.HOSCSF bit is set to 1 before executing a WFI instruction to place the MCU in Software Standby or Deep Software Standby mode while HOCOCR. HCSTP bit is 0
- When a transition to Software Standby or Deep Software Standby mode is to follow a setting to stop the HOCO

LCSTP位（LOCO停止）

LCSTP位启动或停止LOCO时钟。将LCSTP位设置为0以启动LOCO时钟后，仅在LOCO时钟振荡稳定等待时间(tLOCOWT)过去后使用时钟。将LOCO时钟设置为开始操作后，需要进行固定的稳定等待。还需要固定等待振荡停止。

启动和停止操作时适用以下约束：

- 停止LOCO时钟后，在重新启动之前允许至少5个LOCO周期的停止间隔
- 在停止LOCO时钟之前确认LOCO振荡稳定
- 无论是否选择LOCO时钟作为系统时钟，在执行WFI指令将MCU置于软件待机或深度软件待机模式之前，请确认LOCO振荡稳定
- 当转换到软件待机或深度软件待机模式要遵循停止LOCO时钟的设置时，在停止设置之后等待至少3个LOCO周期，然后再执行WFI指令。

在以下情况下禁止向LOSTP写入1：

- SCKSCR.CKSEL[2:0]=010b（系统时钟源=LOCO）。

因为LOCO时钟测量其他振荡器的等待时间，所以无论LOCOCR.LCSTP中的设置如何，它都会在测量该时间时继续振荡。因此，即使LCSTP设置为停止，也可能会无意中提供LOCO时钟。

9.2.10 高速片上振荡器控制寄存器(HOCOCR)

Address(es): SYSTEM.HOCOCR 4001 E036h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	HCSTP
重置后的值：	0	0	0	0	0	0	0	0/1*1

Bit	Symbol	位名称	Description	R/W
b0	HCSTP	HOCO Stop	0：运行HOCO时钟*21：停止HOCO时钟。	R/W
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 当OFS1.HOCOEN位为0时复位后的HCSTP位值为0。当OFS1.HOCOEN位为1时为1。
Note 2. 如果您使用HOCO(HCSTP=0)，则必须将OFS1.HOCOFRQ0[1:0]位设置为最佳值。

HOCOCR寄存器控制HOCO时钟。

HCSTP位（HOCO停止）

HCSTP位启动或停止HOCO时钟。将HCSTP位设置为0以启动HOCO时钟后，在使用时钟之前确认OSCSF.HOSCSF位设置为1。当OFS1.HOCOEN设置为0时，在使用HOCO时钟之前确认OSCSF.HOCOSF设置为1。在设置HOCO时钟开始操作后，需要一个固定的稳定等待。还需要固定等待振荡停止。为了使HOCO运行，还必须设置HOCO等待控制寄存器（HOCOWTCR）。

启动和停止操作时适用以下约束：

- 停止HOCO后，确认OSCSF.HOCOSF位为0后再重启HOCO时钟
- 在停止HOCO时钟之前，确认HOCO时钟正在运行并且OSCSF.HOCOSF位为1
- 无论是否选择HOCO时钟作为系统时钟，在执行WFI指令以在HOCOCR期间将MCU置于软件待机或深度软件待机模式之前，请确认OSCSF.HOSCSF位设置为1。HCSTP位为0
- 当转换到软件待机或深度软件待机模式时要遵循停止HOCO的设置

clock, confirm that the OSCSF.MOSCSF bit is cleared to 0 before executing the WFI instruction.

Writing 1 to HCSTP is prohibited under the following conditions:

- SCKSCR.CKSEL[2:0] = 000b (system clock source = HOCO)
- PLLCCR.PLSRCSEL = 1 (PLL source clock = HOCO) and SCKSCR.CKSEL[2:0] = 101b (system clock source = PLL)
- PLLCCR.PLSRCSEL = 1 (PLL source clock = HOCO) and PLLCR.PLLSTP = 0 (PLL is operating).

9.2.11 High-Speed On-Chip Oscillator Wait Control Register (HOCOWTCR)

Address(es): SYSTEM.HOCOWTCR 4001 E0A5h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	HSTS[2:0]		
Value after reset:	0	0	0	0	0	0	1	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	HSTS[2:0]	HOCO Wait Time Setting	Wait time (s) = (HSTS[2:0] setting +3) /fLOCO	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R

HSTS[2:0] bit (HOCO Wait Time Setting)

The HOCOWTCR.HSTS[2:0] bits must be set to 110b, except when using SCI0 in Snooze mode. When using SCI0 in Snooze mode, HOCOWTCR.HSTS[2:0] must be set to 010b.

9.2.12 Middle-Speed On-Chip Oscillator Control Register (MOCOCR)

Address(es): SYSTEM.MOCOCR 4001 E038h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	MCSTP
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	MCSTP	MOCO Stop	0: Operate the MOCO clock 1: Stop the MOCO clock.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The MOCOCR register controls the MOCO clock.

MCSTP bit (MOCO Stop)

The MCSTP bit starts or stops the MOCO clock. After setting MCSTP to 0 to start the MOCO clock, only use the clock after the MOCO clock oscillation stabilization time (tMOCOWT) elapses. A fixed stabilization wait is required after setting the MOCO clock to start operation. A fixed wait for oscillation to stop is also required.

The following constraints apply when starting and stopping operation:

- After stopping the MOCO clock, allow a stop interval of at least 5 MOCO cycles before restarting it
- Confirm that MOCO oscillation is stable before stopping the MOCO clock
- Regardless of whether the MOCO clock is selected as the system clock, confirm that MOCO oscillation is stable before executing a WFI instruction to place the MCU in Software Standby or Deep Software Standby mode
- When a transition to Software Standby or Deep Software Standby mode is to follow a setting to stop the MOCO

时钟，请确认OSCSF.MOSCSF位在执行WFI指令之前被清除为0。

在以下情况下禁止向HCSTP写入1：

- SCKSCR.CKSEL[2:0]=000b（系统时钟源=HOCO）
- PLLCCR.PLSRCSEL=1（PLL源时钟=HOCO）和SCKSCR.CKSEL[2:0]=101b（系统时钟源=PLL）
- PLLCCR.PLSRCSEL=1（PLL源时钟=HOCO）和PLLCR.PLLSTP=0（PLL正在运行）。

9.2.11 高速片上振荡器等待控制寄存器(HOCOWTCR)

Address(es): SYSTEM.HOCOWTCR 4001 E0A5h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	HSTS[2:0]		
重置后的值：	0	0	0	0	0	0	1	0

Bit	Symbol	位名称	Description	R/W
b2 to b0	HSTS[2:0]	HOCO等待时间设置	等待时间(s)=(HSTS[2:0]设置+3)fLOCO	R/W
b7 to b3	—	Reserved	这些位被读取为0。写入值应为0。	R

HSTS[2:0]位（HOCO等待时间设置）

HOCOWTCR.HSTS[2:0]位必须设置为110b，除非在贪睡模式下使用SCI0。在使用SCI0时贪睡模式，HOCOWTCR.HSTS[2:0]必须设置为010b。

9.2.12 中速片上振荡器控制寄存器(MOCOCR)

Address(es): SYSTEM.MOCOCR 4001 E038h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	MCSTP
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	MCSTP	MOCO Stop	0：运行MOCO时钟1：停止MOCO时钟。	R/W
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

MOCOCR寄存器控制MOCO时钟。

MCSTP位（MOCO停止）

MCSTP位启动或停止MOCO时钟。将MCSTP设置为0以启动MOCO时钟后，请仅在经过MOCO时钟振荡稳定时间(tMOCOWT)后使用该时钟。在设置MOCO时钟开始操作后，需要一个固定的稳定等待。还需要固定等待振荡停止。

启动和停止操作时适用以下约束：

- 停止MOCO时钟后，在重新启动之前允许至少5个MOCO周期的停止间隔
- 在停止MOCO时钟之前确认MOCO振荡稳定
- 无论是否选择MOCO时钟作为系统时钟，在执行WFI指令将MCU置于软件待机或深度软件待机模式之前，请确认MOCO振荡稳定
- 当转换到软件待机或深度软件待机模式时要遵循停止MOCO的设置

clock, wait for at least 3 MOCO clock cycles after the stop setting before executing the WFI instruction.

Writing 1 to MCSTP is prohibited under the following condition:

- SCKSCR.CKSEL[2:0] = 001b (system clock source = MOCO).

Writing 1 to the MCSTP bit (stopping the MOCO) is prohibited if oscillation stop detection is enabled in the Oscillation Stop Detection Control Register (OSTDCR.OSTDE).

9.2.13 FLL Control Register 1 (FLLCR1)

Address(es): SYSTEM.FLLCR1 4001 E039h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	FLLEN
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	FLLEN	FLL Enable	0: FLL function is disabled 1: FLL function is enabled.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: HOCO must be stopped (HOCOCR.HCSTP = 1) before FLLCR1.FLLEN is changed.
Note: SOSC must be operating with stabilization while FLL is enabled (FLLCR1.FLLEN = 1).

The FLLCR1 register controls the FLL function of the HOCO. The purpose of FLL is to utilize SOSC when available for better accuracy in HOCO.

FLLEN bit (FLL Enable)

This bit enables or disables the FLL function of the HOCO.

If FLL is enabled, the frequency accuracy is guaranteed after FLL is stabilized. The FLL stabilization can be checked by the frequency measurement of the Clock Frequency Accuracy Measurement Circuit (CAC) after the HOCO is stabilized.

The FLL must be disabled before the transition to Software Standby mode. Therefore, this bit must be set to 0 before the transition to Software Standby mode.

Figure 9.4 and Figure 9.5 show an example flow of the FLL setting in each case.

时钟，在停止设置后等待至少3个MOCO时钟周期，然后再执行WFI指令。

在以下情况下禁止向MCSTP写入1：

- SCKSCR.CKSEL[2:0]=001b（系统时钟源=MOCO）。

如果在Oscillation中使能了振荡停止检测，则禁止向MCSTP位写入1（停止MOCO）
停止检测控制寄存器(OSTDCR.OSTDE)。

9.2.13 FLL控制寄存器1(FLLCR1)

Address(es): SYSTEM.FLLCR1 4001 E039h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	FLLEN
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	FLLEN	FLL Enable	0：禁用FLL功能1：启用FL L功能。	R/W
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note: 在更改FLLCR1.FLLEN之前，必须停止HOCO（HOCOCR.HCSTP=1）。
Note: SOSC必须在启用FLL时稳定运行(FLLCR1.FLLEN=1)。

FLLCR1寄存器控制HOCO的FLL功能。FLL的目的是在可用时利用SOSC以提高HOCO的准确性。

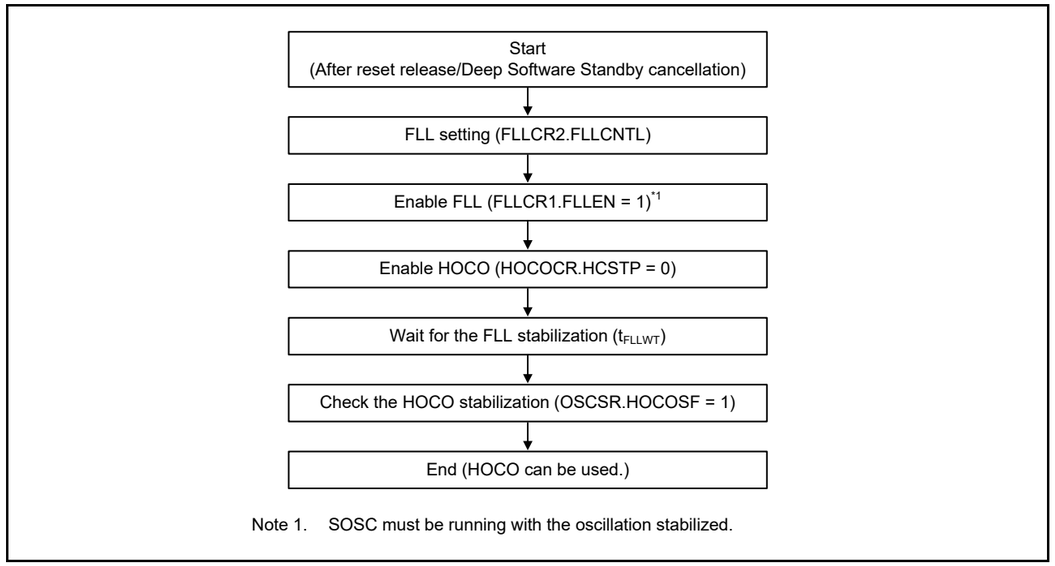
FLLEN位（FLL使能）

该位启用或禁用HOCO的FLL功能。

如果启用FLL，则在FLL稳定后，频率精度得到保证。在HOCO稳定后，可以通过时钟频率精度测量电路(CAC)的频率测量来检查FLL的稳定性。

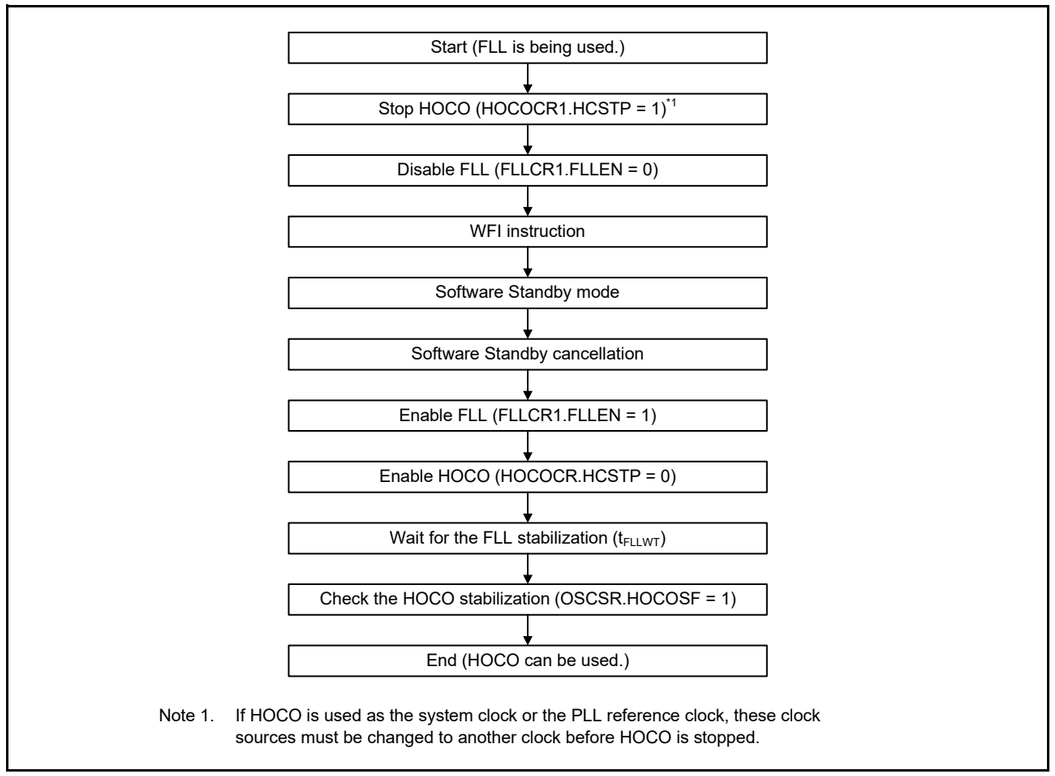
在转换到软件待机模式之前，必须禁用FLL。因此，在转换到软件待机模式之前，该位必须设置为0。

图9.4和图9.5显示了每种情况下FLL设置的示例流程。



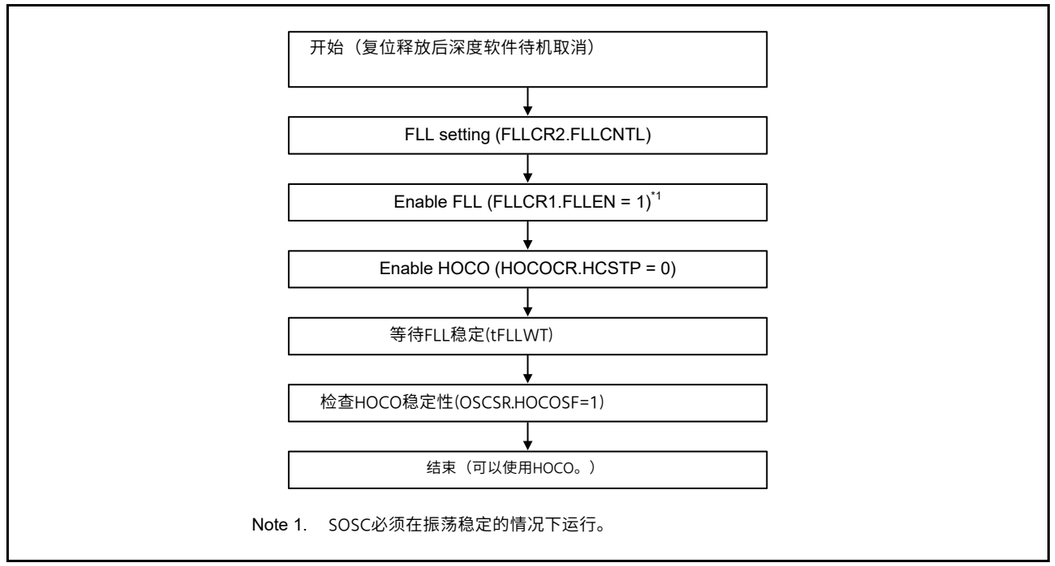
Note 1. SOSC must be running with the oscillation stabilized.

Figure 9.4 FLL setting flow (after reset release / Deep Software Standby cancellation)



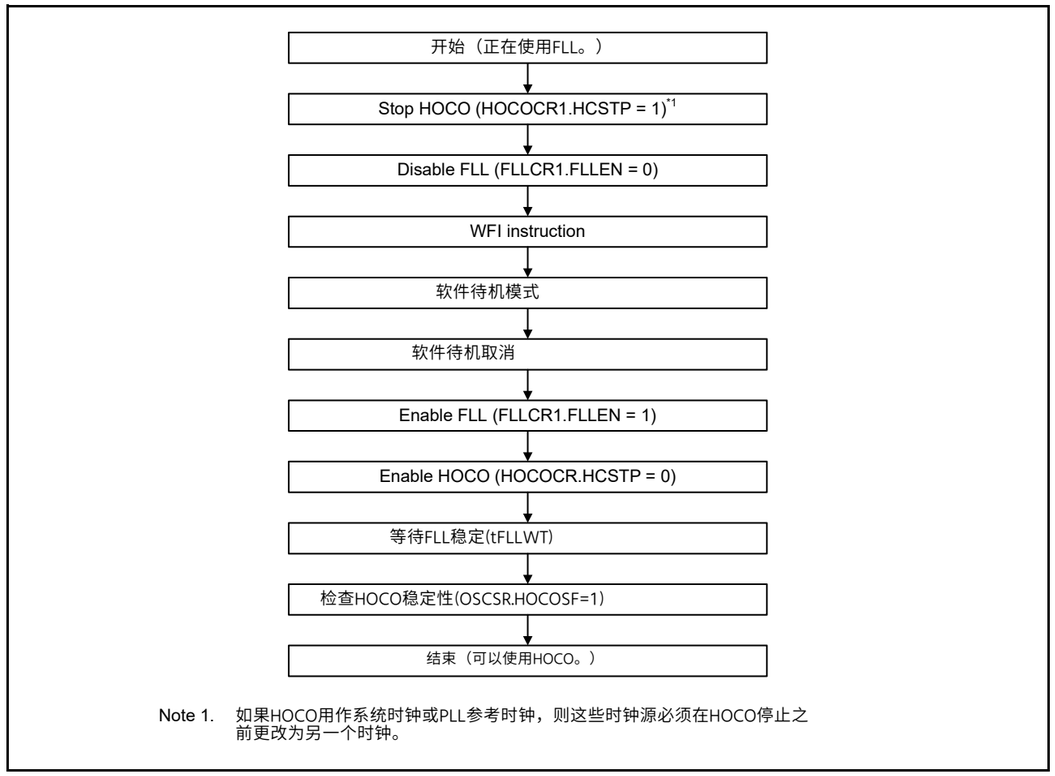
Note 1. If HOCO is used as the system clock or the PLL reference clock, these clock sources must be changed to another clock before HOCO is stopped.

Figure 9.5 Software Standby transition / cancellation flow



Note 1. SOSC必须在振荡稳定的情况下运行。

Figure 9.4 FLL设置流程（复位释放深度软件待机取消后）



Note 1. 如果HOCO用作系统时钟或PLL参考时钟，则这些时钟源必须在HOCO停止之前更改为另一个时钟。

Figure 9.5 软件待机转换取消流程

9.2.14 FLL Control Register 2 (FLLCR2)

Address(es): SYSTEM.FLLCR2.4001 E03Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	FLLCNTL[10:0]										
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b10 to b0	FLLCNTL[10:0]	FLL Multiplication Control	• When OFS1.HOCOFRQ0[1:0] is 00b (16 MHz), these bits must be set to 1E9h • When OFS1.HOCOFRQ0[1:0] is 01b (18 MHz), these bits must be set to 226h • When OFS1.HOCOFRQ0[1:0] is 10b (20 MHz), these bits must be set to 263h. Other settings are prohibited.	R/W
b15 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The FLLCR2 register controls the FLL function of the HOCO.

FLLCNTL[10:0] bits (FLL Multiplication Control)

These bits select the multiplication ratio of the FLL reference clock.

These bits must be set before FLL is enabled (FLLCR1.FLLEN = 1).

9.2.15 Oscillation Stabilization Flag Register (OSCSF)

Address(es): SYSTEM.OSCSF 4001 E03Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	PLLSF	—	MOSCSF	—	—	HOCOSF
Value after reset:	0	0	0	0	0	0	0	0/1*1

Bit	Symbol	Bit name	Description	R/W
b0	HOCOSF	HOCO Clock Oscillation Stabilization Flag	0: HOCO clock is stopped or is not yet stable 1: HOCO clock is stable, so is available for use as the system clock.	R
b2, b1	—	Reserved	These bits are read as 0.	R
b3	MOSCSF	Main Clock Oscillation Stabilization Flag	0: Main clock oscillator is stopped (MOSTP = 1) or is not yet stable*2 1: Main clock oscillator is stable, so is available for use as the system clock.	R
b4	—	Reserved	This bit is read as 0.	R
b5	PLLSF	PLL Clock Oscillation Stabilization Flag	0: PLL clock is stopped or is not yet stable 1: PLL clock is stable, so is available for use as the system clock.	R
b7, b6	—	Reserved	These bits are read as 0.	R

Note 1. The value after reset depends on the OFS1.HOCOEN setting.
When OFS1.HOCOEN = 1, the value after reset of HOCOSF is 0.
When OFS1.HOCOEN = 0, the HOCOSF value is set to 0 immediately after reset is released, and HOCOSF is set to 1 after the HOCO oscillation stabilization wait time elapses.

Note 2. This is true when an appropriate value is set in the wait control register for the given oscillator. If the wait time value is not sufficient, the oscillation stabilization flag is set to 1 and supply of the clock signal to the internal circuits starts before oscillation

9.2.14 FLL控制寄存器2(FLLCR2)

Address(es): SYSTEM.FLLCR2.4001 E03Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	FLLCNTL[10:0]										
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b10 to b0	FLLCNTL[10:0]	FLL乘法控制	当OFS1.HOCOFRQ0[1:0]为00b(16MHz)时，这些位必须设置为1E9h 当OFS1.HOCOFRQ0[1:0]为01b(18MHz)时，这些位必须设置为226h 当OFS1.HOCOFRQ0[1:0]为10b(20MHz)，这些位必须设置为263h。禁止其他设置。	R/W
b15 to b11	—	Reserved	这些位被读取为0。写入值应为0。	R/W

FLLCR2寄存器控制HOCO的FLL功能。

FLLCNTL[10:0]位（FLL乘法控制）

这些位选择FLL参考时钟的倍频比。

这些位必须在启用FLL之前设置（FLLCR1.FLLEN=1）。

9.2.15 振荡稳定标志寄存器(OSCSF)

Address(es): SYSTEM.OSCSF 4001 E03Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	PLLSF	—	MOSCSF	—	—	HOCOSF
重置后的值:	0	0	0	0	0	0	0	0/1*1

Bit	Symbol	位名称	Description	R/W
b0	HOCOSF	HOCO时钟振荡稳定标志	0：HOCO时钟停止或尚未稳定1：HOCO时钟稳定，可用作系统时钟。	R
b2, b1	—	Reserved	这些位读为0。	R
b3	MOSCSF	主时钟振荡稳定标志	0：主时钟振荡器停止（MOSTP=1）或尚未稳定*21：主时钟振荡器稳定，可用作系统时钟。	R
b4	—	Reserved	该位读为0。	R
b5	PLLSF	PLL时钟振荡稳定Flag	0：PLL时钟停止或尚未稳定1：PLL时钟稳定，可用作系统时钟。	R
b7, b6	—	Reserved	这些位读为0。	R

Note 1. 复位后的值取决于OFS1.HOCOEN设置。
当OFS1.HOCOEN=1时，HOCOSF复位后的值为0。
当OFS1.HOCOEN=0时，HOCOSF值在复位释放后立即设置为0，HOCOSF值在复位后设置为1
HOCO振荡稳定等待时间已过。

Note 2. 当给定振荡器的等待控制寄存器中设置了适当的值时，这是正确的。如果等待时间值不够，则将振荡稳定标志设置为1，并在振荡之前开始向内部电路提供时钟信号

is stable.

The OSCSF register flags indicate the operating status of the counters in the oscillation stabilization wait circuits for the individual oscillators. After oscillation starts, these counters measure the wait time until their associated oscillator output clocks are supplied to the internal circuits. An overflow of a counter indicates that the clock supply is stable and available for the associated circuit.

HOCOSF flag (HOCO Clock Oscillation Stabilization Flag)

The HOCOSF flag indicates the operating status of the counter that measures the wait time for the high-speed clock oscillator (HOCO). When OFS1.HOCOEN is set to 0, confirm that the OSCSF.HOCOSF is set to 1 before using the HOCO clock.

[Setting condition]

- After the HOCO clock stops and the HOCOCR.HCSTP bit is set to 0, supply of the MCU clock starts after the number of LOCO cycles associated with the setting of the HOCOWTCR register elapse.

[Clearing condition]

- When the HOCO clock is operating and then is deactivated because the HOCOCR.HCSTP bit is set to 1.

MOSCSF flag (Main Clock Oscillation Stabilization Flag)

The MOSCSF flag indicates the operating status of the counter that measures the wait time for the main clock oscillator.

[Setting condition]

- After the main clock oscillator stops and the MOSCCR.MOSTP bit is set to 0, supply of the MCU clock starts after the number of LOCO cycles associated with the setting of the MOSCWTCR register elapse.

[Clearing condition]

- When the main clock oscillator is operating and then is deactivated because the MOSCCR.MOSTP bit is set to 1.

PLLSF flag (PLL Clock Oscillation Stabilization Flag)

The PLLSF flag indicates the operating status of the counter that measures the wait time for the PLL.

[Setting condition]

- After the PLL stops and the PLLCR.PLLSTP bit is set to 0, supply of the MCU clock starts after 31 LOCO cycles. If oscillation by the PLL clock source selected in the PLLCCR.PLSRCSEL bit is not stable when the PLLSTP bit is set to 0, counting of the LOCO cycles continues after the PLL clock source oscillation is stabilized. Wait time is calculated as:

  1 cycle = LOCO (32.768 kHz) x 8 (3.81 µs typical).

[Clearing condition]

- When the PLL is operating and then is deactivated because the PLLCCR.PLLSTP bit is set to 1.

9.2.16 Oscillation Stop Detection Control Register (OSTDCR)

Address(es): SYSTEM.OSTDCR 4001 E040h

	b7	b6	b5	b4	b3	b2	b1	b0
	OSTDE	—	—	—	—	—	—	OSTDIE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	OSTDIE	Oscillation Stop Detection Interrupt Enable	0: Disable oscillation stop detection interrupt (do not notify the POEG) 1: Enable oscillation stop detection interrupt (notify the POEG).	R/W

是稳定的。

OSCSF寄存器标志指示各个振荡器的振荡稳定等待电路中的计数器的操作状态。振荡开始后，这些计数器测量等待时间，直到其相关的振荡器输出时钟被提供给内部电路。计数器溢出表明时钟供应稳定并可用于相关电路。

HOCOSF标志（HOCO时钟振荡稳定标志）

HOCOSF标志指示测量高速时钟振荡器(HOCO)等待时间的计数器的操作状态。当OFS1.HOCOEN设置为0时，在使用HOCO时钟之前确认OSCSF.HOCOSF设置为1。

[Setting condition]

- 在HOCO时钟停止并且HOCOCR.HCSTP位设置为0后，在与设置HOCOWTCR寄存器相关的LOCO周期数过去后，MCU时钟的供应开始。

[Clearing condition]

- 当HOCO时钟运行，然后因为HOCOCR.HCSTP位设置为1而被停用时。

MOSCSF标志（主时钟振荡稳定标志）

MOSCSF标志指示测量主时钟振荡器等待时间的计数器的操作状态。

[Setting condition]

- 在主时钟振荡器停止并且MOSCCR.MOSTP位设置为0后，MCU时钟的供应在与MOSCWTCR寄存器设置相关的LOCO周期数过去后开始。

[Clearing condition]

- 当主时钟振荡器正在运行，然后因为MOSCCR.MOSTP位设置为1而被停用时。

PLLSF标志（PLL时钟振荡稳定标志）

PLLSF标志指示测量PLL等待时间的计数器的操作状态。

[Setting condition]

- 在PLL停止并且PLLCR.PLLSTP位设置为0后，MCU时钟在31个LOCO周期后开始提供。如果在PLLSTP位设置为0时PLLCCR.PLSRCSEL位中选择的PLL时钟源的振荡不稳定，则在PLL时钟源振荡稳定后继续计数LOCO周期。等待时间计算如下：

1个周期=LOCO(32.768kHz)x8（典型值为3.81µs）
。【结算条件】

- 当PLL正在运行然后因为PLLCCR.PLLSTP位设置为1而被停用时。

9.2.16 振荡停止检测控制寄存器(OSTDCR)

Address(es): SYSTEM.OSTDCR 4001 E040h

	b7	b6	b5	b4	b3	b2	b1	b0
	OSTDE	—	—	—	—	—	—	OSTDIE
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	OSTDIE	振荡停止检测中断使能	0：禁止振荡停止检测中断（不通知POEG）1：使能振荡停止检测中断（通知POEG）。	R/W

Bit	Symbol	Bit name	Description	R/W
b6 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	OSTDE	Oscillation Stop Detection Function Enable	0: Disable oscillation stop detection function 1: Enable oscillation stop detection function.	R/W

The OSTDCR register controls the oscillation stop detection function.

OSTDIE bit (Oscillation Stop Detection Interrupt Enable)

The OSTDIE bit enables the oscillation stop detection function interrupt. It also controls whether oscillation stop detection is reported to the POEG.

If the oscillation stop detection flag in the Oscillation Stop Detection Status Register (OSTDSR.OSTDF) requires clearing, clear the OSTDIE bit to 0 before clearing OSTDF. Wait for at least 2 cycles of PCLKB before setting OSTDIE to 1. A longer PCLKB wait time might be required, depending on the number of cycles required to read a given I/O register.

OSTDE bit (Oscillation Stop Detection Function Enable)

The OSTDE bit enables the oscillation stop detection function. When OSTDE is 1 (enable), the MOCO stop bit (MOCOCR.MCSTP) is cleared to 0 and MOCO operation starts. The MOCO clock cannot be stopped while the oscillation stop detection function is enabled. Writing 1 to the MOCOCR.MCSTP bit (MOCO stopped) is invalid.

When the oscillation stop detection flag in the Oscillation Stop Detection Status Register (OSTDSR.OSTDF) is 1 (main clock oscillation stop detected), writing 0 to the OSTDE bit is invalid.

OSTDE must be cleared before invoking Software Standby or Deep Software Standby mode. To transition to either of these modes, first clear OSTDE to 0 and then execute the WFI instruction.

The following constraints apply when using the oscillation stop detection function:

- In low-speed mode, selecting division by 1, 2, 4, 8 for ICLK, FCLK, BCLK, PCLKA, PCLKB, PCLKC, PCLKD is prohibited.

9.2.17 Oscillation Stop Detection Status Register (OSTDSR)

Address(es): SYSTEM.OSTDSR 4001 E041h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	OSTDF
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	OSTDF	Oscillation Stop Detection Flag	0: Main clock oscillation stop not detected 1: Main clock oscillation stop detected.	R(/W)*1
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R

Note 1. This bit can only be set to 0.

The OSTDSR register indicates the stop detection status of the main clock oscillator.

OSTDF flag (Oscillation Stop Detection Flag)

The OSTDF flag indicates the main clock oscillator status. When OSTDF is 1, it indicates that a main clock oscillation stop was detected. After this stop is detected, the OSTDF bit is not cleared to 0 even when oscillation is restarted. The OSTDF bit is cleared to 0 by writing 0 after reading it as 1.

At least 3 ICLK cycles of wait time are required between writing 0 to OSTDF and reading OSTDF as 0. If the OSTDF bit is cleared to 0 when the main clock oscillation is stopped, the OSTDF bit becomes 0 and then returns to 1.

Bit	Symbol	位名称	Description	R/W
b6 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b7	OSTDE	振荡停止检测 功能启用	0：禁用振荡停止检测功能1：启用振荡停止 检测功能。	R/W

OSTDCR寄存器控制振荡停止检测功能。

OSTDIE位（振荡停止检测中断使能）

OSTDIE位使能振荡停止检测功能中断。它还控制是否将振荡停止检测报告给POEG。

如果振荡停止检测状态寄存器(OSTDSR.OSTDF)中的振荡停止检测标志需要清零，请在清零OSTDF之前将OSTDIE位清零。在将OSTDIE设置为1之前等待至少2个PCLKB周期。可能需要更长的PCLKB等待时间，具体取决于读取给定IO寄存器所需的周期数。

OSTDE位（振荡停止检测功能使能）

OSTDE位使能振荡停止检测功能。当OSTDE为1（使能）时，MOCO停止位（MOCOCR.MCSTP）被清零并开始MOCO操作。MOCO时钟在振荡停止检测功能启用时不能停止。将1写入MOCOCR.MCSTP位（MOCO停止）无效。

当振荡停止检测状态寄存器(OSTDSR.OSTDF)中的振荡停止检测标志为1（检测到主时钟振荡停止）时，向OSTDE位写入0无效。

在调用软件待机或深度软件待机模式之前，必须清除OSTDE。要转换到这两种模式中的任何一种，首先将OSTDE清除为0，然后执行WFI指令。

使用振荡停止检测功能时适用以下约束：

- 在低速模式下，禁止为ICLK、FCLK、BCLK、PCLKA、PCLKB、PCLKC、PCLKD选择1、2、4、8分频。

9.2.17 振荡停止检测状态寄存器(OSTDSR)

Address(es): SYSTEM.OSTDSR 4001 E041h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	OSTDF
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	OSTDF	振荡停止检测标志	0：未检测到主时钟振荡停止1：检测到主 时钟振荡停止。	R(/W)*1
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R

Note 1. 该位只能设置为0。

OSTDSR寄存器指示主时钟振荡器的停止检测状态。

OSTDF标志（振荡停止检测标志）

OSTDF标志指示主时钟振荡器状态。当OSTDF为1时，表示检测到主时钟振荡停止。检测到该停止后，即使重新启动振荡，OSTDF位也不会被清零。OSTDF位在读为1后写入0清零。

从向OSTDF写入0到将OSTDF读取为0之间至少需要3个ICLK周期的等待时间。如果在主时钟振荡停止时将OSTDF位清除为0，则OSTDF位变为0，然后返回1。

OSTDSR.OSTDF cannot be cleared to 0 under the following conditions:

- SCKSCR.CKSEL[2:0] = 011b (system clock source = MOSC)
- PLLCCR.PLSRCSEL = 0 (PLL source clock = MOSC) and SCKSCR.CKSEL[2:0] = 101b (system clock source = PLL).

The OSTDF bit must be set to 0 after switching the clock source to sources other than the main clock oscillator and PLL.

[Setting condition]

- The main clock oscillator is stopped while OSTDCR.OSTDE = 1 (oscillation stop detection enabled).

[Clearing condition]

- 1 is read and then 0 is written when the SCKSCR.CKSEL[2:0] bits are not 011b (system clock = MOSC) or 101b (system clock = PLL) and the PLLCCR.PLSRCSEL bit is not 0 (PLL source clock = MOSC).

9.2.18 Main Clock Oscillator Wait Control Register (MOSCWTCR)

Address(es): SYSTEM.MOSCWTCR 4001 E0A2h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	MSTS[3:0]			
Value after reset:	0	0	0	0	0	1	0	1

Bit	Symbol	Bit name	Description	R/W
b3 to b0	MSTS[3:0]	Main Clock Oscillator Wait Time Setting	When drive capability automatic switching function is disabled (MOMCR.AUTODRVEN = 0 [default]): b3 b0 0 0 0 1: Wait time = 35 cycles (133.5 µs) 0 0 1 0: Wait time = 67 cycles (255.6 µs) 0 0 1 1: Wait time = 131 cycles (499.7 µs) 0 1 0 0: Wait time = 259 cycles (988.0 µs) 0 1 0 1: Wait time = 547 cycles (2086.6 µs) (value after reset) 0 1 1 0: Wait time = 1059 cycles (4039.8 µs) 0 1 1 1: Wait time = 2147 cycles (8190.2 µs) 1 0 0 0: Wait time = 4291 cycles (16368.9 µs) 1 0 0 1: Wait time = 8163 cycles (31139.4 µs). When drive capability automatic switching function is enabled (MOMCR.AUTODRVEN = 1): b3 b0 0 0 0 1: Wait time = 36 cycles (137.3 µs) 0 0 1 0: Wait time = 68 cycles (259.4 µs) 0 0 1 1: Wait time = 132 cycles (503.5 µs) 0 1 0 0: Wait time = 260 cycles (991.8 µs) 0 1 0 1: Wait time = 548 cycles (2090.5 µs) (value after reset) 0 1 1 0: Wait time = 1060 cycles (4043.6 µs) 0 1 1 1: Wait time = 2148 cycles (8194.0 µs) 1 0 0 0: Wait time = 4292 cycles (16372.7 µs) 1 0 0 1: Wait time = 8164 cycles (31143.2 µs). Other settings are prohibited. Wait time is calculated as: 1 cycle (µs) = 1 / (f_LOCO [MHz] × 8) = 1 / (0.032768 × 8) = 3.81 µs	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R

MSTS[3:0] bits (Main Clock Oscillator Wait Time Setting)

Set the MSTS[3:0] bits to select the oscillation stabilization wait time for the main clock oscillator. Specify a time period longer than or equal to the stabilization time recommended by the oscillator manufacturer. When the main clock is input externally, set these bits to 0001b, because the oscillation stabilization time is not required.

在下列情况下，OSTDSR.OSTDF不能清为0：

- SCKSCR.CKSEL[2:0]=011b（系统时钟源=MOSC）
- PLLCCR.PLSRCSEL=0（PLL源时钟=MOSC）和SCKSCR.CKSEL[2:0]=101b（系统时钟源=PLL).

将时钟源切换到主时钟振荡器和PLL以外的源后，必须将OSTDF位设置为0。

[Setting condition]

- 当OSTDCR.OSTDE=1（使能振荡停止检测）时，主时钟振荡器停止。

[Clearing condition]

- 当SCKSCR.CKSEL[2:0]位不是011b（系统时钟=MOSC）或101b（系统时钟=PLL）且PLLCCR.PLSRCSEL位不为0（PLL源时钟=MOSC）。

9.2.18 主时钟振荡器等待控制寄存器(MOSCWTCR)

Address(es): SYSTEM.MOSCWTCR 4001 E0A2h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	MSTS[3:0]			
重置后的值：	0	0	0	0	0	1	0	1

Bit	Symbol	位名称	Description	R/W
b3 to b0	MSTS[3:0]	主时钟振荡器等待时间设定	禁用驱动能力自动切换功能时（MOMCR.AUTODRVEN=0[默认]）：b3 0 0 0 1：等待时间=35个周期(133.5µs) 0 0 1 0：等待时间=67个周期(255.6µs) 0 0 1 1：等待时间=131个周期(499.7µs) 0 1 0 0：等待时间=259个周期(988.0µs) 0 1 0 1：等待时间=547个周期（2086.6µs）（复位后的值） 0 1 1 0：等待时间=1059个周期（4039.8µs） 0 1 1 1：等待时间=2147个周期（8190.2µs） 1 0 0 0：等待时间=4291个周期（16368.9µs） 1 0 0 1：等待时间=8163个周期（31139.4µs）。 当驱动能力自动切换功能启用时（MOMCR.AUTODRVEN=1）：b3 0 0 0 1：等待时间=36个周期(137.3µs) 0 0 1 0：等待时间=68个周期(259.4µs) 0 0 1 1：等待时间=132个周期(503.5µs) 0 1 0 0：等待时间=260个周期(991.8µs) 0 1 0 1：等待时间=548个周期（2090.5µs）（复位后的值） 0 1 1 0：等待时间=1060个周期（4043.6µs） 0 1 1 1：等待时间=2148个周期（8194.0µs） 1 0 0 0：等待时间=4292个周期（16372.7µs） 01：等待时间=8164个周期（31143.2µs）。禁止其他设置。 等待时间计算如下：1个周期(µs)=1(f_LOCO[MHz]×8)=1(0.032768×8)=3.81µs	R/W
b7 to b4	—	Reserved	这些位被读取为0。写入值应为0。	R

MSTS[3:0]位（主时钟振荡器等待时间设置）

设置MSTS[3:0]位以选择主时钟振荡器的振荡稳定等待时间。指定一个长于或等于振荡器制造商推荐的稳定时间的时间段。当外部输入主时钟时，将这些位设置为0001b，因为不需要振荡稳定时间。

The wait time set in these bits is counted using:

1 cycle (µs) = 1 / (f_ LOCO [MHz] × 8) = 1 / (0.032768 x 8) = 3.81 (µs).

The LOCO clock automatically oscillates when necessary, regardless of the value of the LOCOCR.LOSTP bit. After the specified wait time elapses, supply of the main clock oscillator starts internally in the MCU, and the OSCSF.MOSCSF flag is set to 1. If the specified wait time is short, supply of the main clock oscillator starts before oscillation of the clock becomes stable.

Only rewrite the MOSCWTCR register when the MOSCCR.MOSTP bit is 1 and the OSCSF.MOSCSF flag is 0. Do not rewrite this register under any other conditions.

9.2.19 Main Clock Oscillator Mode Oscillation Control Register (MOMCR)

Address(es): SYSTEM.MOMCR 4001 E413h

	b7	b6	b5	b4	b3	b2	b1	b0
	AUTODRVEN	MOSEL	MODRV0[1:0]		—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b5, b4	MODRV0[1:0]	Main Clock Oscillator Drive Capability 0 Switching	b5 b4 0 0: 20 to 24 MHz 0 1: 16 to 20 MHz 1 0: 8 to 16 MHz 1 1: 8 MHz.	R/W
b6	MOSEL	Main Clock Oscillator Switching	0: Resonator 1: External clock input.	R/W
b7	AUTODRVEN	Main Clock Oscillator Drive Capability Auto Switching Enable	0: Disable 1: Enable.	R/W

Note: The EXTAL/XTAL pins are also used as ports. In the initial state, the port function is selected.
Note: The MOSTP bit must be 1 (MOSC = stopped) before changing this register.

MODRV0[1:0] bits (Main Clock Oscillator Drive Capability 0 Switching)

The MODRV0[1:0] bits switch the drive capability of the main clock oscillator.

MOSEL bit (Main Clock Oscillator Switching)

The MOSEL bit switches the source for the main clock oscillator.

AUTODRVEN bit (Main Clock Oscillator Drive Capability Auto Switching Enable)

The AUTODRVEN bit controls the drive capability auto switching of the main clock oscillator.

When AUTODRVEN = 1, after the time set in the MSTS bits in the Main Clock Oscillator Wait Control Register elapses, the effective main clock oscillator drive capability is automatically set to the lowest, regardless of the MOMCR.MODRV0[1:0] setting. The main clock oscillator restarts oscillation with MOMCR.MODRV0 specified drive capability after oscillation stops by MOSCCR.MOSTP setting or by entering Software Standby mode.

这些位中设置的等待时间使用以下方法计算：

1个周期(µs)=1(f_LOCO[MHz]×8)=1(0.032768x8)=3.81(µs)。

无论LOCOCR.LOSTP位的值如何，LOCO时钟都会在必要时自动振荡。经过指定的等待时间后，MCU内部开始提供主时钟振荡器，并将OSCSF.MOSCSF标志设置为1。如果指定的等待时间短，则在时钟振荡之前开始提供主时钟振荡器变得稳定。

仅当MOSCCR.MOSTP位为1且OSCSF.MOSCSF标志为0时才重写MOSCWTCR寄存器。在任何其他情况下请勿重写此寄存器。

9.2.19 主时钟振荡器模式振荡控制寄存器(MOMCR)

Address(es): SYSTEM.MOMCR 4001 E413h

	b7	b6	b5	b4	b3	b2	b1	b0
	AUTODRVEN	MOSEL	MODRV0[1:0]		—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b3 to b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b5, b4	MODRV0[1:0]	主时钟振荡器驱动能力0切换	b5 b4 0 0: 20 to 24 MHz 0 1: 16 to 20 MHz 1 0: 8 to 16 MHz 1 1: 8 MHz.	R/W
b6	MOSEL	主时钟振荡器切换	0：谐振器1：外部时钟输入。	R/W
b7	AUTODRVEN	主时钟振荡器驱动能力自动切换启用	0：禁用1 ：启用。	R/W

Note: EXTALXTAL引脚也用作端口。在初始状态下，选择端口功能。
Note: 在更改此寄存器之前，MOSTP位必须为1（MOSC=停止）。

MODRV0[1:0]位（主时钟振荡器驱动能力0切换）

MODRV0[1:0]位切换主时钟振荡器的驱动能力。

MOSEL位（主时钟振荡器切换）

MOSEL位切换主时钟振荡器的源。

AUTODRVEN位（主时钟振荡器驱动能力自动切换使能）

AUTODRVEN位控制主时钟振荡器的驱动能力自动切换。

当AUTODRVEN=1时，在主时钟振荡器等待控制寄存器的MSTS位中设置的时间过去后，有效的主时钟振荡器驱动能力自动设置为最低，而与MOMCR.MODRV0[1:0]设置无关。在通过MOCCR.MOSTP设置或进入软件待机模式停止振荡后，主时钟振荡器以MOMCR.MODRV0指定的驱动能力重新开始振荡。

9.2.20 Subclock Oscillator Mode Control Register (SOMCR)

Address(es): SYSTEM.SOMCR 4001 E481h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	SODRV1	—
Value after reset:	0	0	0	0	0	0	x	0

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b0	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b1	SODRV1	Sub-Clock Oscillator Drive Capability Switching	0: Standard 1: Low.	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: The SOSCCR.SOSTP bit must be 1 (SOSC = stopped) before changing this register.

SODRV1 bit (Sub-Clock Oscillator Drive Capability Switching)

The SODRV1 bit switches the drive capability of the sub-clock oscillator. This bit is undefined at the first power on, but the value after reset of SOSCCR.SOSTP is 0 (SOSC = operating). Set up the SOSC as follows at the first power on:

1. Set the SOSCCR.SOSTP bit to 1 (SOSC = stopped).
2. Set this bit to the correct value for the current capacitor.
3. Clear the SOSCCR.SOSTP to 0 (SOSC = operating).

9.2.21 Clock Out Control Register (CKOCR)

Address(es): SYSTEM.CKOCR 4001 E03Eh

	b7	b6	b5	b4	b3	b2	b1	b0
	CKOEN	CKODIV[2:0]			—	CKOSEL[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	CKOSEL[2:0]	Clock Out Source Select	b2 b0 0 0: HOCO 0 1: MOCO 1 0: LOCO 1 1: MOSC 0 0: SOSC. Other settings are prohibited.	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6 to b4	CKODIV[2:0]	Clock Out Input Frequency Division Select	b6 b4 0 0: ×1 0 1: /2 1 0: /4 1 1: /8 0 0: /16 0 1: /32 1 0: /64 1 1: /128.	R/W
b7	CKOEN	Clock Out Enable	0: Disable clock out 1: Enable clock out.	R/W

9.2.20 副时钟振荡器模式控制寄存器(SOMCR)

Address(es): SYSTEM.SOMCR 4001 E481h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	SODRV1	—
重置后的值：	0	0	0	0	0	0	x	0

x: Undefined

Bit	Symbol	位名称	Description	R/W
b0	—	Reserved	该位读取为0。写入值应为0。	R/W
b1	SODRV1	副时钟振荡器驱动能力切换	0：标准1 ：低。	R/W
b7 to b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note: 在更改此寄存器之前，SOSCCR.SOSTP位必须为1（SOSC=停止）。

SODRV1位（副时钟振荡器驱动能力切换）

SODRV1位切换副时钟振荡器的驱动能力。该位在第一次上电时未定义，但SOSCCR.SOSTP复位后的值为0（SOSC=运行）。首次上电时按如下方式设置SOSC：

1. 将SOSCCR.SOSTP位设置为1（SOSC=停止）。
2. 将此位设置为当前电容器的正确值。
3. 将SOSCCR.SOSTP清除为0（SOSC=运行）。

9.2.21 时钟输出控制寄存器(CKOCR)

Address(es): SYSTEM.CKOCR 4001 E03Eh

	b7	b6	b5	b4	b3	b2	b1	b0
	CKOEN	CKODIV[2:0]			—	CKOSEL[2:0]		
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b2 to b0	CKOSEL[2:0]	时钟输出源选择	b2 b0 0 0: HOCO 0 1: MOCO 1 0: LOCO 1 1: MOSC 00：SOSC。禁止其他设置。	R/W
b3	—	Reserved	该位读取为0。写入值应为0。	R/W
b6 to b4	CKODIV[2:0]	时钟输出输入频率分区选择	b6 b4 0 0: ×1 0 1: /2 1 0: /4 1 1: /8 0 0: /16 0 1: /32 1 0: /64 1 1: /128.	R/W
b7	CKOEN	时钟输出使能	0：禁用时钟输出1 ：启用时钟输出。	R/W

CKOSEL[2:0] bits (Clock Out Source Select)

The CKOSEL[2:0] bits specify the HOCO, MOCO, LOCO, MOSC, or SOSC clock as the source of the clock to be output from the CLKOUT pin. When changing the CLKOUT source clock, clear the CKOEN bit to 0.

CKODIV[2:0] bits (Clock Out Input Frequency Division Select)

The CKODIV[2:0] bits specify the clock division ratio. Clear the CKOEN bit to 0 when changing the division ratio. The division ratio of the output clock frequency must be set to a value no higher than the characteristics of the CLKOUT pin output frequency. For details on the characteristics of the CLKOUT pin, see section 60, Electrical Characteristics.

CKOEN bit (Clock Out Enable)

The CKOEN bit enables output from the CLKOUT pin. When CKOEN is set to 1, the selected clock is output. When CKOEN is set to 0, low is output. When changing this bit, confirm that the clock out source clock selected in the CKOSEL[2:0] bits is stable. Otherwise, a glitch might be generated in the output.

The CKOEN bit must be cleared before entering Software Standby or Deep Software Standby mode if the selected clock out source clock is stopped in that mode.

9.2.22 External Bus Clock Output Control Register (EBCKOCR)

Address(es): SYSTEM.EBCKOCR 4001 E052h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	EBCKOEN
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	EBCKOEN	EBCLK Pin Output Control	0: Disable EBCLK pin output (fixed high) 1: Enable EBCLK pin output.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

9.2.23 SDRAM Clock Output Control Register (SDCKOCR)

Address(es): SYSTEM.SDCKOCR 4001 E053h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	SDCKOEN
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	SDCKOEN	SDCLK Pin Output Control	0: Disable SDCLK pin output (fixed high) 1: Enable SDCLK pin output.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

CKOSEL[2:0]位（时钟输出源选择）

CKOSEL[2:0]位指定HOCO、MOCO、LOCO、MOSC或SOSC时钟作为从CLKOUT引脚输出的时钟源。更改CLKOUT源时钟时，将CKOEN位清零。

CKODIV[2:0]位（时钟输出输入分频选择）

CKODIV[2:0]位指定时钟分频比。更改分频比时将CKOEN位清零。输出时钟频率的分频比必须设置为不高于CLKOUT引脚输出频率特性的值。有关CLKOUT引脚特性的详细信息，请参见第60节，电气特性。

CKOEN位（时钟输出使能）

CKOEN位使能CLKOUT引脚的输出。当CKOEN设置为1时，输出选定的时钟。什么时候CKOEN设置为0，输出低电平。当改变该位时，确认时钟输出源时钟选择在CKOSEL[2:0]位是稳定的。否则，可能会在输出中产生故障。

如果所选时钟输出源时钟在该模式下停止，则必须在进入软件待机或深度软件待机模式之前清零CKOEN位。

9.2.22 外部总线时钟输出控制寄存器（EBCKOCR）

Address(es): SYSTEM.EBCKOCR 4001 E052h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	EBCKOEN
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	EBCKOEN	EBCLK引脚输出控制	0：禁止EBCLK引脚输出（固定为高电平）1：使能EBCLK引脚输出。	R/W
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

9.2.23 SDRAM时钟输出控制寄存器(SDCKOCR)

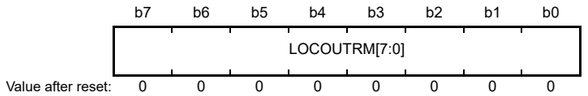
Address(es): SYSTEM.SDCKOCR 4001 E053h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	SDCKOEN
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	SDCKOEN	SDCLK 引脚输出控制	0：禁用SDCLK 引脚输出（固定高）1：启用SDCLK 引脚输出。	R/W
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

9.2.24 LOCO User Trimming Control Register (LOCOUTCR)

Address(es): SYSTEM.LOCOUTCR 4001 E492h

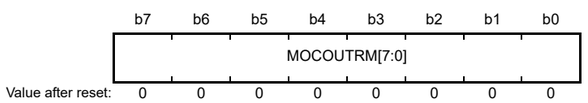


Bit	Symbol	Bit name	Description	R/W
b7 to b0	LOCOUTRM[7:0]	LOCO User Trimming	b7 b0 1 0 0 0 0 0 0 0: -128 1 0 0 0 0 0 0 1: -127 1 0 0 0 0 0 1 0: -126 … 1 1 1 1 1 1 1 1: -1 0 0 0 0 0 0 0 0: Center Code 0 0 0 0 0 0 0 1: +1 … 0 1 1 1 1 1 0 1: +125 0 1 1 1 1 1 1 0: +126 0 1 1 1 1 1 1 1: +127. These bits are added to the original LOCO trimming bits.	R/W

Note: MCU operation is not guaranteed when LOCOUTCR is set to a value that causes the LOCO frequency to be outside of the specification range.
Note: When LOCOUTCR is changed, the frequency stabilization wait required corresponds to the frequency stabilization wait at the start of MCU operation.

9.2.25 MOCO User Trimming Control Register (MOCOUTCR)

Address(es): SYSTEM.MOCOUTCR 4001 E061h

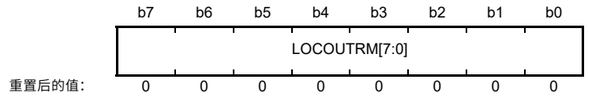


Bit	Symbol	Bit name	Description	R/W
b7 to b0	MOCOUTRM[7:0]	MOCO User Trimming	b7 b0 1 0 0 0 0 0 0 0: -128 1 0 0 0 0 0 0 1: -127 1 0 0 0 0 0 1 0: -126 … 1 1 1 1 1 1 1 1: -1 0 0 0 0 0 0 0 0: Center Code 0 0 0 0 0 0 0 1: +1 … 0 1 1 1 1 1 0 1: +125 0 1 1 1 1 1 1 0: +126 0 1 1 1 1 1 1 1: +127. These bits are added to the original MOCO trimming bits.	R/W

Note: MCU operation is not guaranteed when MOCOUTCR is set to a value that causes the MOCO frequency to be outside of the specification range.
Note: When MOCOUTCR is changed, the frequency stabilization wait required corresponds to the frequency stabilization wait at the start of MCU operation.

9.2.24 LOCO用户微调控制寄存器(LOCOUTCR)

Address(es): SYSTEM.LOCOUTCR 4001 E492h

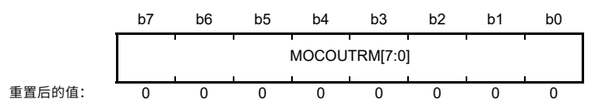


Bit	Symbol	位名称	Description	R/W
b7 to b0	LOCOUTRM[7:0]	LOCO用户修整	b7b010000000：-1281000 0001：-12710000010：-1 26…11111111：-10000000 0：中心代码00000001：+1 …01111101：+1250111111 0：+12601111111：+127。 这些位被添加到原始的LOCO修整位。	R/W

Note: 当LOCOUTCR设置为导致LOCO频率超出规范范围的值时，MCU操作无法保证。
Note: 当LOCOUTCR改变时，所需的频率稳定等待对应于MCU操作开始时的频率稳定等待。

9.2.25 MOCO用户微调控制寄存器(MOCOUTCR)

Address(es): SYSTEM.MOCOUTCR 4001 E061h



Bit	Symbol	位名称	Description	R/W
b7 to b0	MOCOUTRM[7:0]	MOCO用户修整	b7b010000000：-1281000 0001：-12710000010：-1 26…11111111：-10000000 0：中心代码00000001：+1 …01111101：+1250111111 0：+12601111111：+127。 这些位被添加到原始MOCO修整位中。	R/W

Note: 当MOCOUTCR设置为导致MOCO频率超出规格范围的值时，无法保证MCU操作。
Note: 当MOCOUTCR改变时，所需的频率稳定等待对应于MCU操作开始时的频率稳定等待。

9.2.26 HOCO User Trimming Control Register (HOCOUTCR)

Address(es): SYSTEM.HOCOUTCR 4001 E062h

	b7	b6	b5	b4	b3	b2	b1	b0
	HOCOUTRM[7:0]							
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	HOCOUTRM[7:0]	HOCO User Trimming	b7 b0 1 0 0 0 0 0 0 0: -128 1 0 0 0 0 0 0 1: -127 1 0 0 0 0 0 1 0: -126 … 1 1 1 1 1 1 1 1: -1 0 0 0 0 0 0 0 0: Center Code 0 0 0 0 0 0 0 1: +1 … 0 1 1 1 1 1 1 0: +125 0 1 1 1 1 1 1 1: +126 0 1 1 1 1 1 1 1: +127. These bits are added to the original HOCO trimming bits.	R/W

Note: MCU operation is not guaranteed when HOCOUTCR is set to a value that causes the HOCO frequency to be outside of the specification range.

Note: When HOCOUTCR is changed, the frequency stabilization wait required corresponds to the frequency stabilization wait at the start of MCU operation.

Note: These bits must be 00000000b when FLL is enabled (FLLCR1.FLLEN = 1).

9.2.27 Trace Clock Control Register (TRCKCR)

Address(es): SYSTEM.TRCKCR 4001 E03Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	TRCKEN	—	—	—	TRCK[3:0]			
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Bit name	Description	R/W
b3 to b0	TRCK[3:0]	Trace Clock Operating Frequency Select	b3 b0 0 0 0 0: /1 0 0 0 1: /2 (value after reset) 0 0 1 0: /4. Other settings are prohibited.	R/W
b6 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	TRCKEN	Trace Clock Operation Enable	0: Disable operation 1: Enable operation.	R/W

The Trace Clock Control Register controls the switching of the trace clock. Before changing the TRCLK frequency, set the TRCKEN bit to 0. The TRCKCR register is initialized by all reset sources.

9.3 Main Clock Oscillator

Use one of the following ways to supply the clock signal to the main clock oscillator:

- Connect an oscillator
- Connect the input of an external clock signal.

9.2.26 HOCO用户微调控制寄存器(HOCOUTCR)

Address(es): SYSTEM.HOCOUTCR 4001 E062h

	b7	b6	b5	b4	b3	b2	b1	b0
	HOCOUTRM[7:0]							
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b7 to b0	HOCOUTRM[7:0]	HOCO用户修整	b7b010000000：-1281000 0001：-12710000010：-1 26…11111111：-10000000 0：中心代码00000001：+1 …01111101：+1250111111 0：+12601111111：+127。 这些位被添加到原始HOCO修整位中。	R/W

Note: 当HOCOUTCR设置为导致HOCO频率超出规范范围的值时，MCU操作无法保证。

Note: 当HOCOUTCR改变时，所需的频率稳定等待对应于MCU操作开始时的频率稳定等待。

Note: 当FLL使能时（FLLCR1.FLLEN=1），这些位必须为00000000b。

9.2.27 跟踪时钟控制寄存器(TRCKCR)

Address(es): SYSTEM.TRCKCR 4001 E03Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	TRCKEN	—	—	—	TRCK[3:0]			
重置后的值:	0	0	0	0	0	0	0	1

Bit	Symbol	位名称	Description	R/W
b3 to b0	TRCK[3:0]	跟踪时钟运行频率选择	b3b00000：10001：2（复位后的值）0010：4。禁止其他设置。	R/W
b6 to b4	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b7	TRCKEN	跟踪时钟操作Enable	0：禁用操作1：启用操作。	R/W

跟踪时钟控制寄存器控制跟踪时钟的切换。在更改TRCLK频率之前，将TRCKEN位设置为0。TRCKCR寄存器由所有复位源初始化。

9.3 主时钟振荡器

使用以下方法之一向主时钟振荡器提供时钟信号：

- 连接振荡器
- 连接外部时钟信号的输入。

9.3.1 Connecting the Crystal Resonator

Figure 9.6 shows an example connection to a crystal resonator. A damping resistor (Rd) can be added, if required. Because the resistor values vary according to the resonator and the oscillation drive capability, use values recommended by the resonator manufacturer. If the manufacturer recommends using an external feedback resistor (Rf), insert an Rf between EXTAL and XTAL by following the instructions.

When connecting a resonator to supply the clock, the frequency of the resonator must be in the frequency range of the resonator for the main clock oscillator as described in Table 9.1.

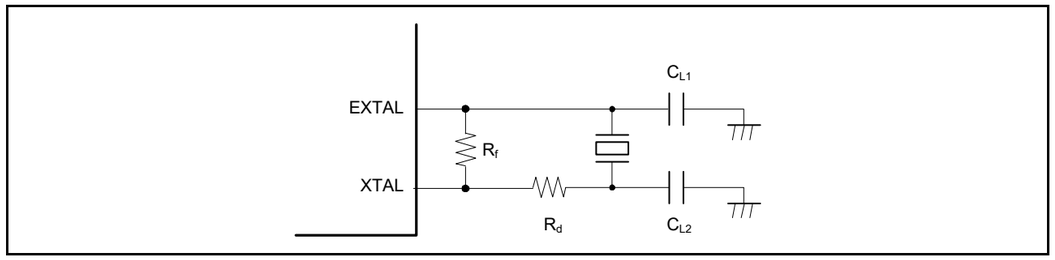


Figure 9.6 Example of crystal resonator connection

Figure 9.7 shows an equivalent circuit of the crystal resonator.

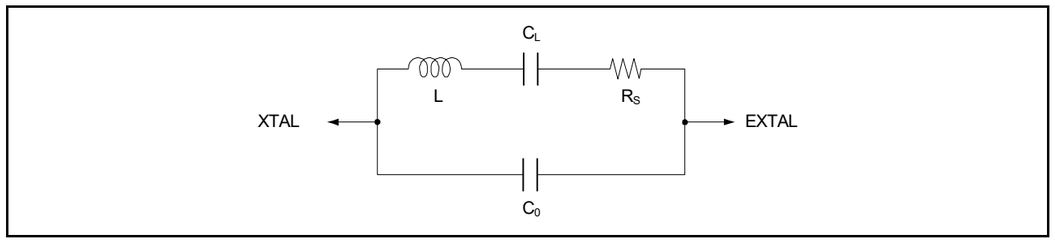


Figure 9.7 Equivalent circuit of the crystal resonator

9.3.2 External Clock Input

Figure 9.8 shows an example connection to an external clock input. To operate the oscillator with an external clock signal, set the MOMCR.MOSEL bit to 1. The XTAL pin is the function that is set in PFS.P213PFS.

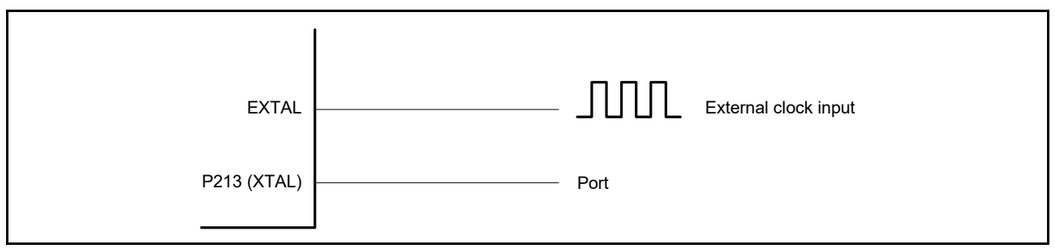


Figure 9.8 Equivalent circuit for external clock

9.3.3 Notes on External Clock Input

The frequency of the external clock input can only be changed while the main clock oscillator is stopped. Do not change the frequency of the external clock input when the main clock oscillator stop bit (MOSCCR.MOSTP) is 0.

9.3.1 连接晶体谐振器

图9.6显示了与晶体谐振器的示例连接。如果需要，可以添加一个阻尼电阻器(Rd)。
由于电阻值因谐振器和振荡驱动能力而异，请使用谐振器制造商推荐的值。如果制造商建议使用外部反馈电阻器(Rf)，请按照说明在EXTAL和XTAL之间插入一个Rf。

连接谐振器以提供时钟时，谐振器的频率必须在表9.1中所述的主时钟振荡器的谐振器频率范围内。

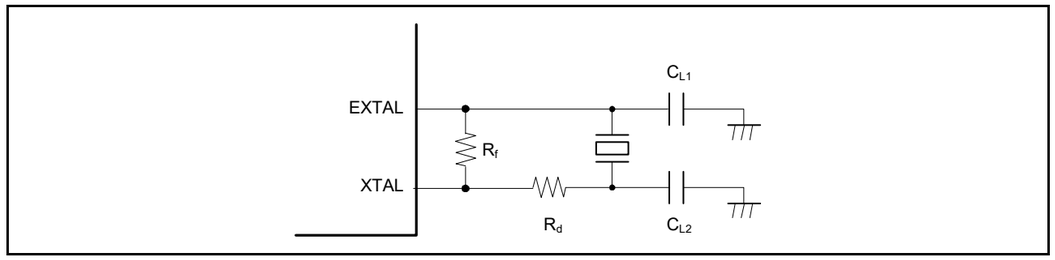


Figure 9.6 晶体谐振器连接示例

图9.7显示了晶体谐振器的等效电路。

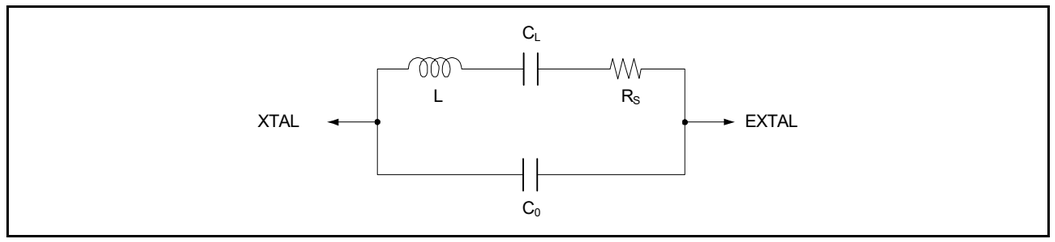


Figure 9.7 晶体谐振器的等效电路

9.3.2 外部时钟输入

图9.8显示了与外部时钟输入的连接示例。要使用外部时钟信号操作振荡器，请将MOMCR.MOSEL位设置为1。XTAL引脚是在PFS.P213PFS中设置的功能。

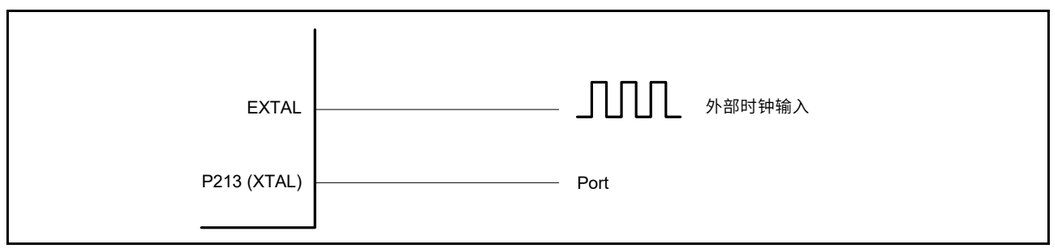


Figure 9.8 外部时钟等效电路

9.3.3 外部时钟输入注意事项

外部时钟输入的频率只能在主时钟振荡器停止时改变。当主时钟振荡器停止位(MOSCCR.MOSTP)为0时，请勿更改外部时钟输入的频率。

9.4 Sub-Clock Oscillator

The only way of supplying a clock signal to the sub-clock oscillator is by connecting a crystal oscillator.

9.4.1 Connecting a 32.768-kHz Crystal Resonator

To supply a clock to the sub-clock oscillator, connect a 32.768-kHz crystal resonator as shown in Figure 9.9. A damping resistor (Rd) can be added, if required. Because the resistor values vary according to the resonator and the oscillation drive capability, use values recommended by the resonator manufacturer. If the manufacturer recommends using an external feedback resistor (Rf), insert an Rf between XCIN and XCOUT by following the instructions.

When connecting a resonator to supply the clock, the frequency of the resonator must be in the frequency range of the resonator for the sub-clock oscillator as described in Table 9.1.

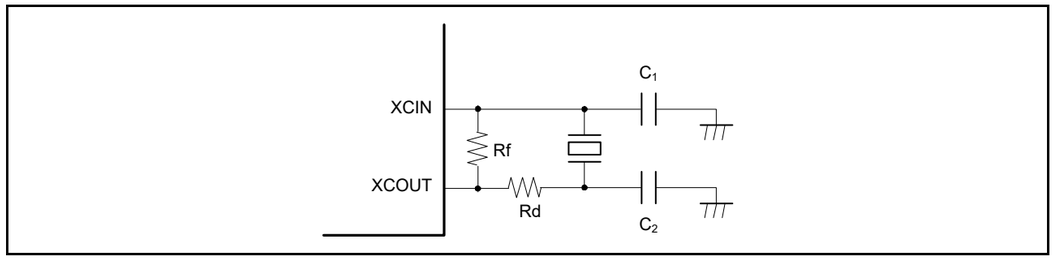


Figure 9.9 Connection example of 32.768-kHz crystal resonator

Figure 9.10 shows an equivalent circuit for the 32.768-kHz crystal resonator.

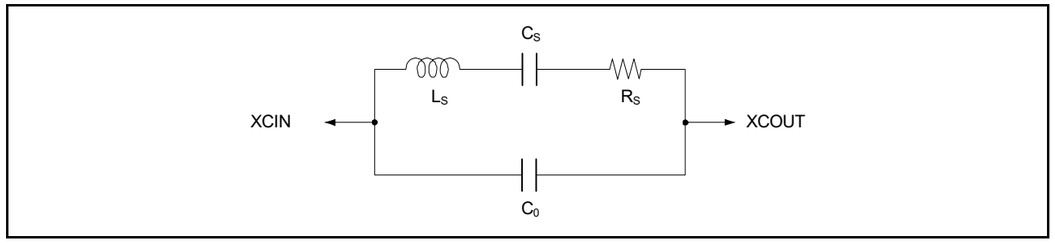


Figure 9.10 Equivalent circuit for the 32.768-kHz crystal resonator

9.4.2 Handling of Pins When the Sub-Clock Oscillator Is Not Used

When the sub-clock oscillator is not in use, connect the XCIN pin to VSS through a resistor (to pull VSS down) and leave the XCOUT pin open as shown in Figure 9.11. In addition, if an oscillator is not connected, set the sub-clock oscillator stop bit (SOSCCR.SOSTP) to 1 to stop the oscillator.

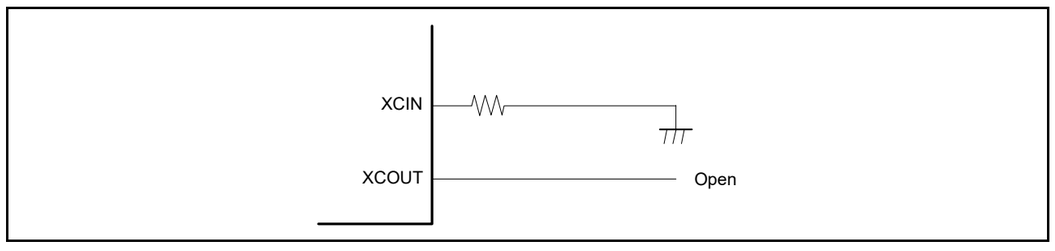


Figure 9.11 Pin handling when the sub-clock oscillator is not used

9.4 Sub-Clock Oscillator

向副时钟振荡器提供时钟信号的唯一方法是连接晶体振荡器。

9.4.1 连接32.768kHz晶体谐振器

要为副时钟振荡器提供时钟，请连接一个32.768-kHz晶体谐振器，如图9.9所示。如果需要，可以添加一个阻尼电阻器(Rd)。由于电阻值因谐振器和振荡驱动能力而异，请使用谐振器制造商推荐的值。如果制造商建议使用外部反馈电阻器(Rf)，请按照说明在XCIN和XCOUT之间插入一个Rf。

连接谐振器以提供时钟时，谐振器的频率必须在表9.1中所述的副时钟振荡器的谐振器频率范围内。

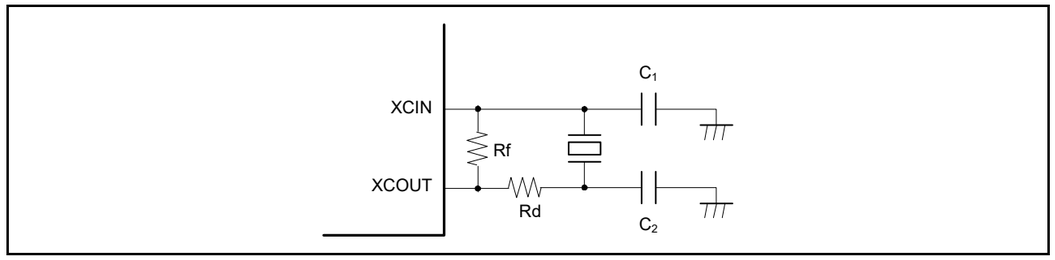


Figure 9.9 32.768-kHz晶体谐振器的连接示例

图9.10显示了32.768-kHz晶体谐振器的等效电路。

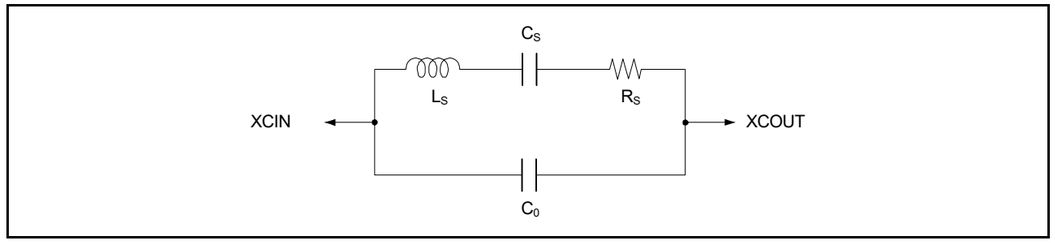


Figure 9.10 32.768kHz晶体谐振器的等效电路

9.4.2 不使用副时钟振荡器时的引脚处理

不使用副时钟振荡器时，通过一个电阻将XCIN引脚连接到VSS（将VSS下拉）并使XCOUT引脚保持开路，如图9.11所示。此外，如果未连接振荡器，则将副时钟振荡器停止位(SOSCCR.SOSTP)设置为1以停止振荡器。

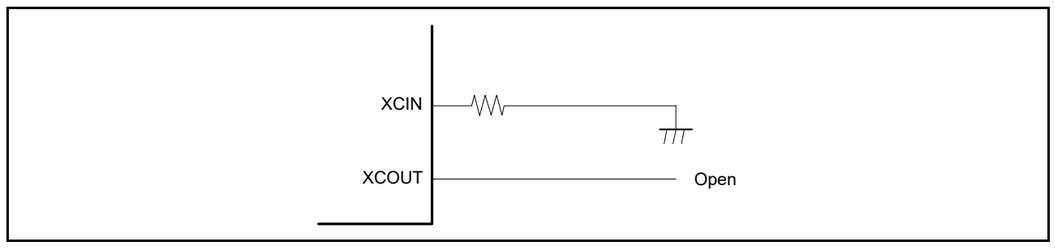


Figure 9.11 不使用副时钟振荡器时的引脚处理

9.5 Oscillation Stop Detection Function

9.5.1 Oscillation Stop Detection and Operation after Detection

The oscillation stop detection function detects the main clock oscillator stop. When an oscillation stop is detected, the system clock switches as follows:

- If an oscillation stop is detected with SCKSCR.CKSEL[2:0] = 011b (system clock source = MOSC), the system clock source switches to the MOCO clock.
- If an oscillation stop is detected with PLLCCR.PLSRCSEL = 0 (PLL source clock = MOSC) and SCKSCR.CKSEL[2:0] = 101b (system clock source = PLL), the PLL clock remains as the system clock source. The frequency becomes free-running, and the setting in the SCKSCR.CKSEL[2:0] bits does not change.

An oscillation stop detection interrupt request can be generated when an oscillation stop is detected. In addition, the General PWM Timer (GPT) output can be forced to a high-impedance state on detection.

The main clock oscillation stop is detected when the input clock remains at 0 or 1 for a certain period, for example, when a malfunction occurs in the main clock oscillator. See section 60, Electrical Characteristics.

Switching between the main clock oscillator and the MOCO clock or between the PLL clock and the PLL free-running clock is controlled by the oscillation stop detection flag (OSTDSR.OSTDF).

The OSTDF flag controls the switched clock as follows:

- When SCKSCR.CKSEL[2:0] = 011b (system clock source = MOSC):
  - When OSTDF changes from 0 to 1, the clock source switches to the MOCO clock.
  - When OSTDF changes from 1 to 0, the clock source switches to MOSC again.
- When PLLCCR.PLSRCSEL = 0 (PLL source clock = MOSC) and SCKSCR.CKSEL[2:0] = 101b (system clock source = PLL)
  - When OSTDF changes from 0 to 1, the clock source switches to the PLL free-running oscillation clock.
  - When OSTDF changes from 1 to 0, the clock source switches to PLL again.

To switch the clock source to the main clock oscillator or PLL clock again after oscillation stop detection, set the CKSEL[2:0] bits to a clock source other than the main clock oscillator or PLL clock, and clear the OSTDF flag to 0. Also, check that the OSTDF flag is not 1, and then set the CKSEL[2:0] bits to the main clock oscillator or PLL clock after the specified oscillation stabilization time elapses.

After a reset release, the main clock oscillator is stopped and the oscillation stop detection function is disabled. To enable the oscillation stop detection function, activate the main clock oscillator and write 1 to the oscillation stop detection function enable bit (OSTDCR.OSTDE) after the specified oscillation stabilization time elapses.

The oscillation stop detection function detects when the main clock oscillator is stopped by an external cause. This means that the oscillation stop detection function must be disabled before the main clock oscillator is stopped by software or before entering Software Standby or Deep Software Standby mode.

The oscillation stop detection function switches the following clocks to the MOCO clock (when the system clock is MOSC) or the PLL free-running clock (when the system clock is PLL):

- All clocks that can be selected as the MOSC clock or PLL except CLKOUT
- The system clock (ICLK) frequency during MOCO operation (when the system clock is MOSC) or PLL free-running operation (when the system clock is PLL) is specified in the MOCO oscillation frequency and the division ratio set in the system clock select bits (SCKDIVCR.ICK[2:0]).

9.5 振荡停止检测功能

9.5.1 振荡停止检测和检测后操作

振荡停止检测功能检测主时钟振荡器停止。当检测到振荡停止时，系统时钟切换如下：

- 如果通过SCKSCR.CKSEL[2:0]=011b（系统时钟源=MOSC）检测到振荡停止，则系统时钟源切换到MOCO时钟。
- 如果在PLLCCR.PLSRCSEL=0（PLL源时钟=MOSC）的情况下检测到振荡停止并且SCKSCR.CKSEL[2:0]=101b(系统时钟源=PLL)，PLL时钟保持为系统时钟源。频率变为自由运行，并且SCKSCR.CKSEL[2:0]位中的设置不会改变。

当检测到振荡停止时，可以产生一个振荡停止检测中断请求。除此之外
通用PWM定时器(GPT)输出可在检测时强制为高阻抗状态。

当输入时钟保持在0或1一段时间，例如，当主时钟振荡器发生故障时，检测到主时钟振荡停止。请参见第60节，电气特性。

主时钟振荡器和MOCO时钟之间或PLL时钟和PLL自由运行时钟之间的切换由振荡停止检测标志(OSTDSR.OSTDF)控制。

OSTDF标志控制切换时钟如下：

- 当SCKSCR.CKSEL[2:0]=011b（系统时钟源=MOSC）时：
  - 当OSTDF从0变为1时，时钟源切换到MOCO时钟。
  - 当OSTDF从1变为0时，时钟源再次切换到MOSC。
- 当PLLCCR.PLSRCSEL=0（PLL源时钟=MOSC）且SCKSCR.CKSEL[2:0]=101b（系统时钟源=PLL）时
  - 当OSTDF从0变为1时，时钟源切换到PLL自由振荡时钟。
  - 当OSTDF从1变为0时，时钟源再次切换到PLL。

要在检测到振荡停止后再次将时钟源切换到主时钟振荡器或PLL时钟，请设置
CKSEL[2:0]位到主时钟振荡器或PLL时钟以外的时钟源，并将OSTDF标志清除为0。另外，检查OSTDF标志不是1，然后设置CKSEL[2:0]在指定的振荡稳定时间过后，位到主时钟振荡器或PLL时钟。

复位释放后，主时钟振荡器停止，振荡停止检测功能被禁用。要启用振荡停止检测功能，激活主时钟振荡器并在指定的振荡稳定时间过去后将1写入振荡停止检测功能使能位(OSTDCR.OSTDE)。

振荡停止检测功能检测主时钟振荡器何时因外部原因停止。这意味着在软件停止主时钟振荡器之前或进入软件待机或深度软件待机模式之前，必须禁用振荡停止检测功能。

振荡停止检测功能将以下时钟切换到MOCO时钟（当系统时钟为
MOSC）或PLL自由运行时钟（当系统时钟为PLL时）：

- 除CLKOUT外，所有可选择作为MOSC时钟或PLL的时钟
- MOCO操作（系统时钟为MOSC时）或PLL自由运行操作（系统时钟为PLL时）期间的系统时钟(ICLK)频率在MOCO振荡频率和系统时钟选择位中设置的分频比中指定(SCKDIVCR.ICK[2:0]）。

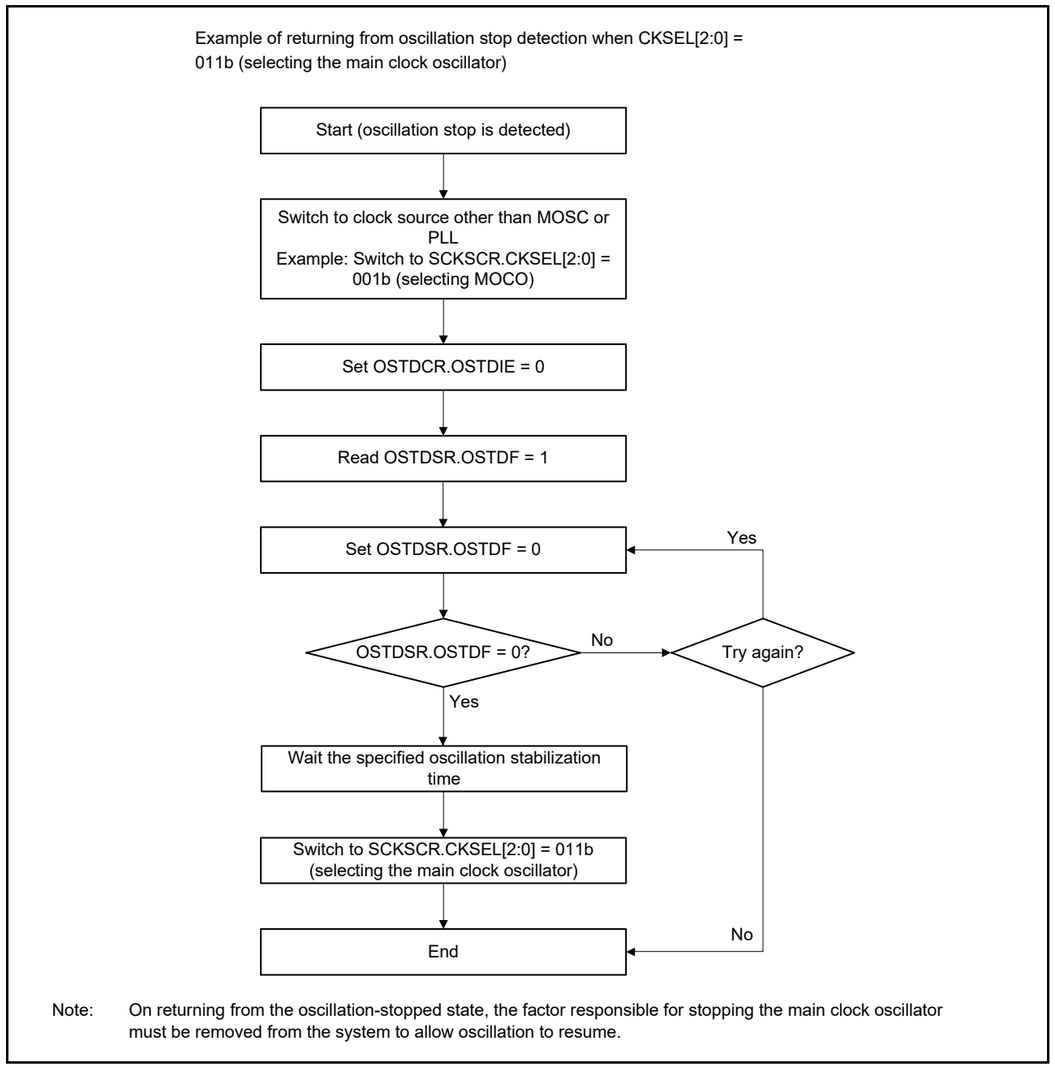


Figure 9.12 Flow of recovery on detection of oscillator stop

9.5.2 Oscillation Stop Detection Interrupts

An oscillation stop detection interrupt (MOSC_STOP) is generated when the oscillation stop detection flag (OSTDSR.OSTDF) is 1 and the oscillation stop detection interrupt enable bit in the Oscillation Stop Detection Control Register (OSTDCR.OSTDIE) is 1 (enabled). The Port Output Enable for GPT (POEG) is notified of the main clock oscillator stop. On receiving the notification, the POEG sets the Oscillation Stop Detection Flag in the POEG Group n Setting Register (POEGGn.OSTPF) to 1 (n = A, B, C, D).

After the oscillation stop is detected, wait at least 10 cycles of PCLKB before writing to the POEGGn.OSTPF flag. When the OSTDSR.OSTDF flag requires clearing, do so after clearing the oscillation stop detection interrupt enable bit in the Oscillation Stop Detection Control Register (OSTDCR.OSTDIE). Wait for at least 2 cycles of the PCLKB clock before setting the OSTDCR.OSTDIE bit to 1 again. A longer PCLKB wait time might be required, depending on the number of cycles required to read a given I/O register.

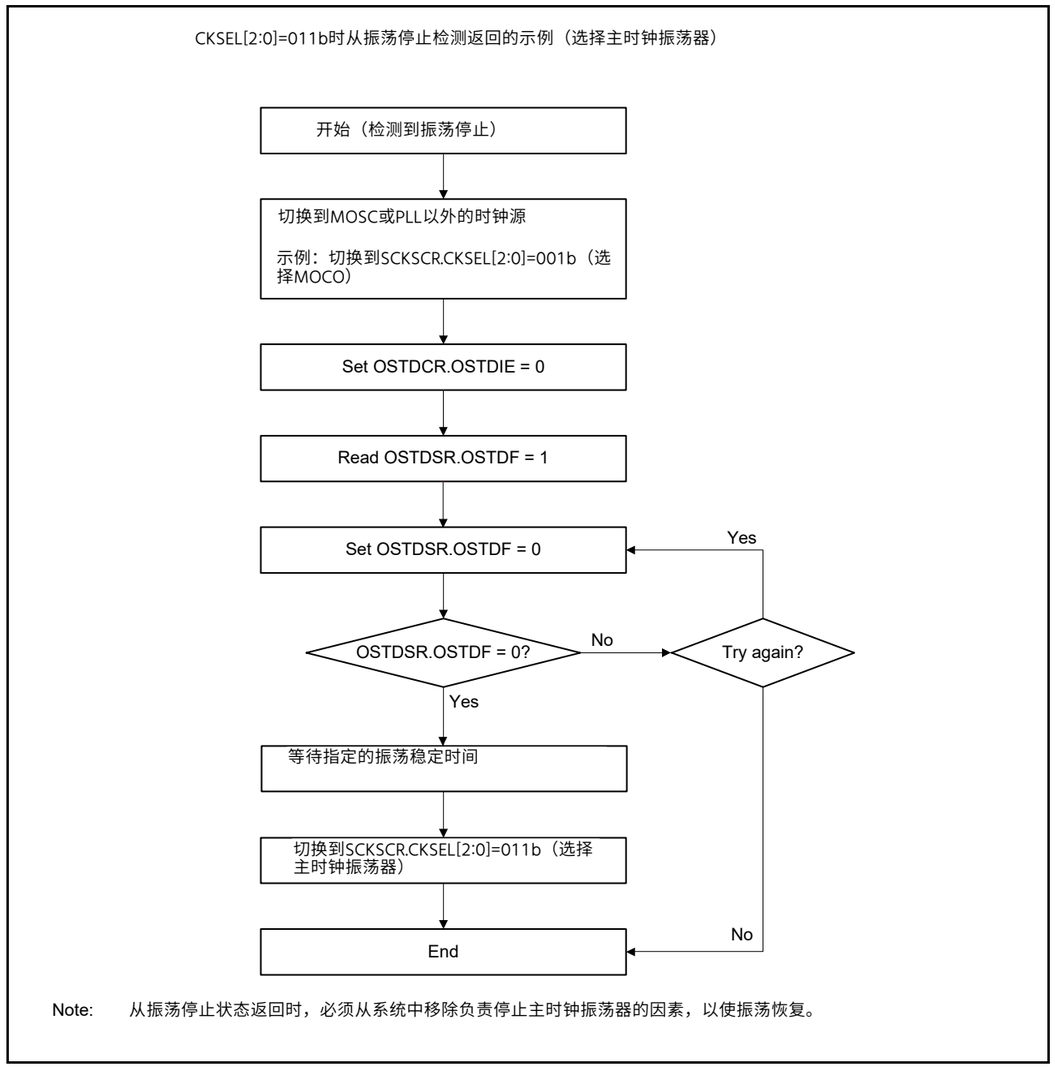


Figure 9.12 检测到振荡器停止时的恢复流程

9.5.2 振荡停止检测中断

当振荡停止检测标志(OSTDSR.OSTDF)为1且振荡停止检测控制寄存器(OSTDCR.OSTDIE)中的振荡停止检测中断使能位为1（启用）时，将产生振荡停止检测中断(MOSC_STOP)。GPT端口输出使能(POEG)被通知主时钟振荡器停止。收到通知后，POEG将POEG组n设置寄存器(POEGGn.OSTPF)中的振荡停止检测标志设置为1(n=A B C D)。

检测到振荡停止后，在写入POEGGn.OSTPF标志之前至少等待10个PCLKB周期。
当需要清除OSTDSR.OSTDF标志时，请在清除振荡停止检测控制寄存器(OSTDCR.OSTDIE)中的振荡停止检测中断使能位后进行。等待至少2个PCLKB时钟周期，然后再将OSTDCR.OSTDIE位设置为1。可能需要更长的PCLKB等待时间，具体取决于读取给定IO寄存器所需的周期数。

The oscillation stop detection interrupt is a non-maskable interrupt. Because non-maskable interrupts are disabled in the initial state after a reset release, enable non-maskable interrupts through software before using oscillation stop detection interrupts. For details, see section 14, Interrupt Controller Unit (ICU).

9.6 PLL Circuit

The PLL circuit provides a function for multiplying the frequency from the oscillator.

9.7 Internal Clock

Clock sources for the internal clock signals include:

- Main clock oscillator
- Sub-clock oscillator
- HOCO clock
- MOCO clock
- LOCO clock
- PLL clock
- Dedicated clock for the IWDT
- External clock for JTAG.

The following internal clocks are produced from these sources:

- Operating clock for the CPU, DMAC, DTC, flash memory, and SRAM — system clock (ICLK)
- Operating clocks for peripheral modules — PCLKA, PCLKB, PCLKC, and PCLKD
- Operating clock for the flash interface — FCLK
- Clock for the external bus controller and external pin output — EBCLK
- Clock for the external bus controller and external pin output for the SDRAM — SDCLK
- Operating clock for the USBFS and USBHS — UCLK
- Operating clock for the USB-PHY — USBMCLK
- Operating clock for the CAN — CANMCLK
- Operating clock for the CAC — CACCLK
- Operating clock for the RTC LOCO clock — RTCLCLK
- Operating clock for the RTC sub-clock — RTCSCLK
- Operating clock for the IWDT — IWDTCLK
- Operating clock for the AGT LOCO clock — AGTLCLK
- Operating clock for the AGT sub-clock — AGTSCLK
- Operating clock for the SysTick timer — SYSTICCLK
- Clock for external pin output — CLKOUT
- Operating clock for the JTAG — JTAGTCK.

For details on the registers used to set the frequencies of the internal clocks, see section 9.7.1, System Clock (ICLK) to section 9.7.15, JTAG Clock (JTAGTCK). If the value of any of these bits is changed, subsequent operation is at the frequency determined by the new value.

振荡停止检测中断是一个不可屏蔽的中断。由于不可屏蔽中断在复位释放后的初始状态下被禁用，因此在使用振荡停止检测中断之前，请通过软件启用不可屏蔽中断。有关详细信息，请参阅第14节，中断控制器单元(ICU)。

9.6 PLL Circuit

PLL电路提供了将振荡器的频率倍增的功能。

9.7 内部时钟

内部时钟信号的时钟源包括：

- 主时钟振荡器
- Sub-clock oscillator
- HOCO clock
- MOCO clock
- 机车时钟
- PLL clock
- IWDT的专用时钟
- JTAG的外部时钟。

以下内部时钟由这些源产生：

- CPU、DMAC、DTC、闪存和SRAM的工作时钟—系统时钟(ICLK)
- 外围模块的工作时钟—PCLKA、PCLKB、PCLKC和PCLKD
- 闪存接口的工作时钟——FCLK
- 外部总线控制器和外部引脚输出的时钟—EBCLK
- 外部总线控制器的时钟和SDRAM的外部引脚输出—SDCLK
- USBFS和USBHS的工作时钟—UCLK
- USB-PHY的工作时钟—USBMCLK
- CAN的工作时钟—CANMCLK
- CAC的工作时钟—CACCLK
- RTCLOCO时钟的工作时钟—RTCLCLK
- RTC子时钟的工作时钟—RTCSCLK
- IWDT的工作时钟—IWDTCLK
- AGTLOCO时钟的工作时钟—AGTLCLK
- AGT子时钟的工作时钟—AGTSCLK
- SysTick定时器的工作时钟—SYSTICCLK
- 外部引脚输出时钟—CLKOUT
- JTAG的工作时钟—JTAGTCK。

有关用于设置内部时钟频率的寄存器的详细信息，请参见第9.7.1节，系统时钟(ICLK)至第9.7.15节，JTAG时钟(JTAGTCK)。如果这些位中的任何一个的值发生变化，则后续操作将以新值确定的频率进行。

9.7.1 System Clock (ICLK)

The system clock, ICLK, is the operating clock for the CPU, DMAC, DTC, flash memory, and SRAM. Specify the frequency in the following bits:

- ICK[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[5:0] and PLIDIV[1:0] bits in PLLCCR
- HOCOFRQ0[1:0] bits in OFS1.

When the ICLK clock source is switched, the duration of the ICLK clock cycle becomes longer during the clock source transition period. See Figure 9.13 and Figure 9.14.

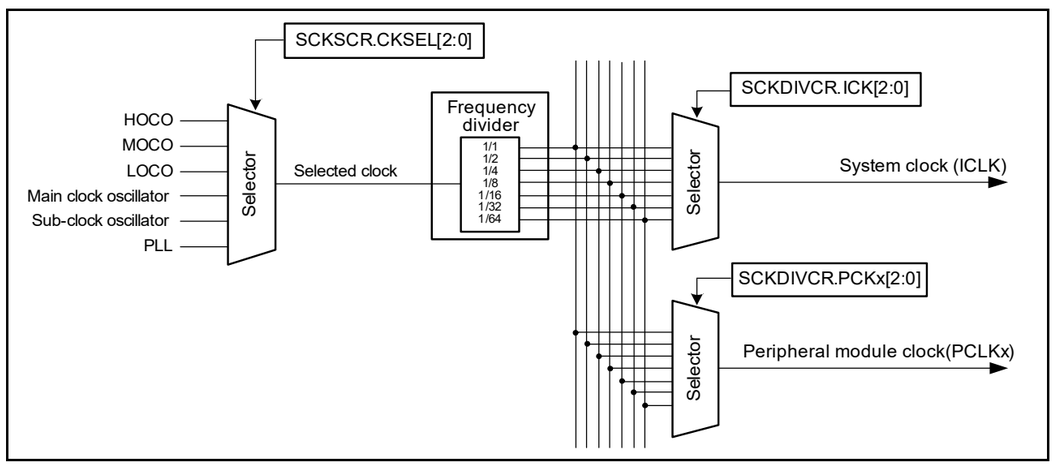


Figure 9.13 Clock source selector block diagram

9.7.1 系统时钟(ICLK)

系统时钟ICLK是CPU、DMAC、DTC、闪存和SRAM的工作时钟。在以下位中指定频率：

- SCKDIVCR中的ICK[2:0]位
- SCKSCR中的CKSEL[2:0]位
- PLLCCR中的PLLMUL[5:0]和PLIDIV[1:0]位
- OFS1中的HOCOFRQ0[1:0]位。

当ICLK时钟源切换时，ICLK时钟周期的持续时间在时钟源转换期间变长。请参见图9.13和图9.14。

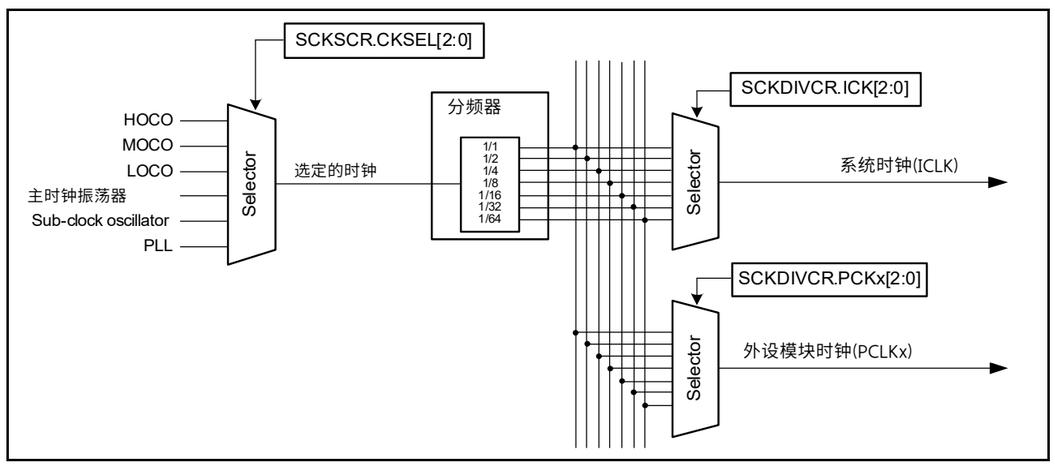


Figure 9.13 时钟源选择器框图

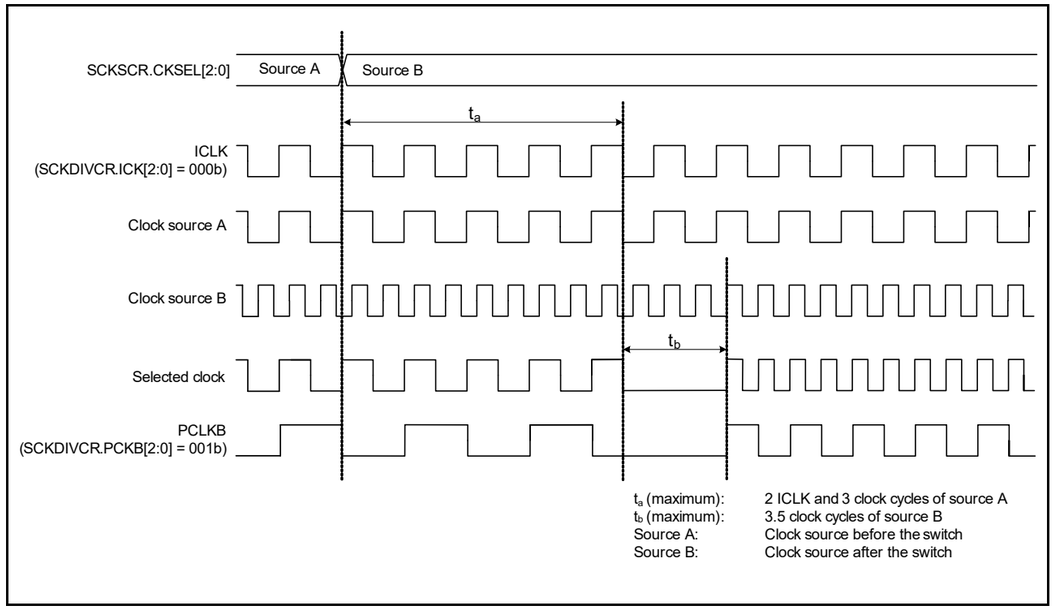


Figure 9.14 Clock source switching timing diagram

9.7.2 Peripheral Module Clock (PCLKA, PCLKB, PCLKC, PCLKD)

The peripheral module clocks, PCLKA, PCLKB, PCLKC, and PCLKD, are the operating clocks for the peripheral modules. Specify the frequency in the following bits:

- PCKA[2:0], PCKB[2:0], PCKC[2:0], and PCKD[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[5:0] and PLIDIV[1:0] bits in PLLCCR
- HOCOFRQ0[1:0] bits in OFS1.

When the clock source of the peripheral module clock is switched, the duration of the peripheral module clock cycle becomes longer during the clock source transition period. See Figure 9.13 and Figure 9.14.

9.7.3 Flash Interface Clock (FCLK)

The flash interface clock, FCLK, is the operating clock for the flash memory interface. In addition to reading from the data flash, it is used for the programming and erasure of the code flash and data flash. Specify the frequency in the following bits:

- FCK[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[5:0] and PLIDIV[1:0] bits in PLLCCR
- HOCOFRQ0[1:0] bits in OFS1.

9.7.4 External Bus Clock (BCLK)

The external bus clock, BCLK, is an operating clock for the external bus controller. It is also output externally from the EBCLK pin for the external connection bus. To output BCLK from the EBCLK pin, set the EBCKOCR.EBCKOEN bit to 1 and set the PmnPFS.PSEL[4:0] bits to 01011b. Only change the PmnPFS.PSEL[4:0] bits to 01011b when the EBCKOCR.EBCKOEN bit is 0. When the BCKCR.BCLKDIV bit is set to 1, the BCLK clock divided by 2 is output from the EBCLK pin. Specify the frequency in the following bits:

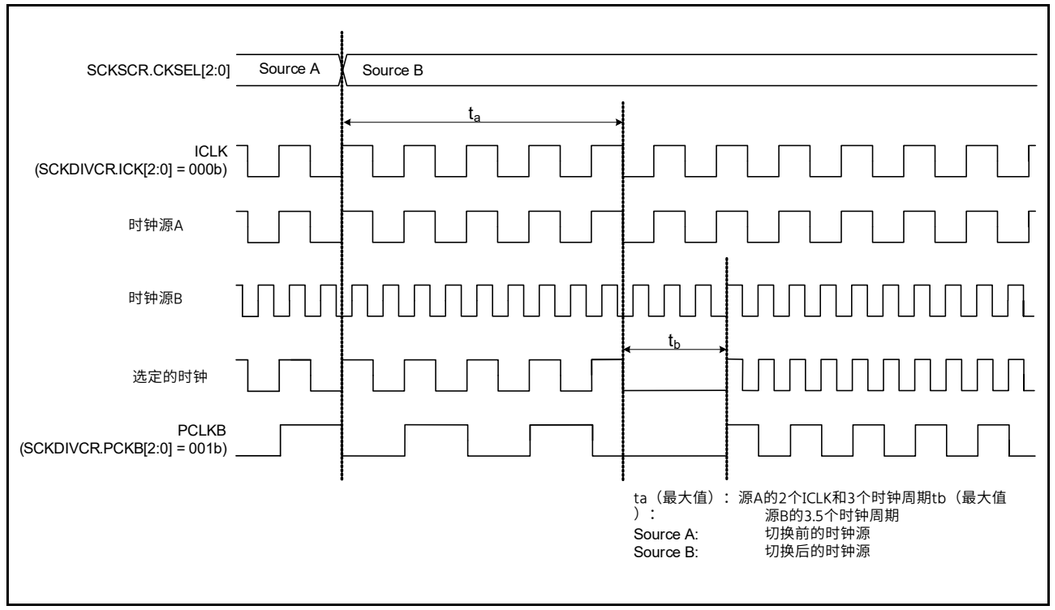


Figure 9.14 时钟源切换时序图

9.7.2 外设模块时钟（PCLKA、PCLKB、PCLKC、PCLKD）

外围模块时钟PCLKA、PCLKB、PCLKC和PCLKD是外围模块的工作时钟。在以下位中指定频率：

- SCKDIVCR中的PCKA[2:0]、PCKB[2:0]、PCKC[2:0]和PCKD[2:0]位
- SCKSCR中的CKSEL[2:0]位
- PLLCCR中的PLLMUL[5:0]和PLIDIV[1:0]位
- OFS1中的HOCOFRQ0[1:0]位。

当外围模块时钟的时钟源切换时，外围模块时钟周期的持续时间在时钟源转换期间会变长。请参见图9.13和图9.14。

9.7.3 闪存接口时钟(FCLK)

闪存接口时钟FCLK是闪存接口的工作时钟。除了从数据闪存中读取外，它还用于代码闪存和数据闪存的编程和擦除。在以下位中指定频率：

- SCKDIVCR中的FCK[2:0]位
- SCKSCR中的CKSEL[2:0]位
- PLLCCR中的PLLMUL[5:0]和PLIDIV[1:0]位
- OFS1中的HOCOFRQ0[1:0]位。

9.7.4 外部总线时钟(BCLK)

外部总线时钟BCLK是外部总线控制器的工作时钟。它也从外部连接总线的EBCLK引脚向外输出。要从EBCLK引脚输出BCLK，请将EBCKOCR.EBCKOEN位设置为1，并将PmnPFS.PSEL[4:0]位设置为01011b。仅当EBCKOCR.EBCKOEN位为0时将PmnPFS.PSEL[4:0]位更改为01011b。当BCKCR.BCLKDIV位设置为1时，从EBCLK引脚输出BCLK时钟除以2。在以下位中指定频率：

- BCK[2:0] bits in SCKDIVCR
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[5:0] and PLIDIV[1:0] bits in PLLCCR
- HOCOFRQ0[1:0] bits in OFS1.

Do not set BCLK to a frequency higher than that of the system clock (ICLK).

9.7.5 SDRAM Clock (SDCLK)

The SDRAM clock, SDCLK, is an operating clock for the external bus controller. It is output externally from the SDCLK pin for the SDRAM that is connected to the external bus. To output SDCLK on the SDCLK pin, set the SDCKOCR.SDCKOEN bit to 1 and set the PmnPFS.PSEL[4:0] bits to 01011b (enabling SDCLK output). Only change the value in the PmnPFS.PSEL[4:0] bits when the SDCKOCR.SDCKOEN bit is 0. Specify the frequency in the following bits:

- SCKDIVCR.BCK[2:0], SCKSCR.CKSEL[2:0], the PLLMUL[5:0], and PLIDIV[1:0] bits in PLLCCR
- HOCOFRQ0[1:0] bits in OFS1.

Do not set SDCLK to a frequency higher than that of the system clock (ICLK).

9.7.6 USB Clock (UCLK)

The USB clock, UCLK, is the operating clock for the USBFS and USBHS module. A 48-MHz clock must be supplied to the USBFS and USBHS module. When the module is used, the UCLK clock must be specified as 48 MHz. Specify the frequency in the following bits:

- UCK[2:0] bits in SCKDIVCR2
- CKSEL[2:0] bits in SCKSCR
- PLLMUL[5:0] and PLIDIV[1:0] bits in PLLCCR.

9.7.7 USB-PHY Clock (USBMCLK)

The USB-PHY clock, USBMCLK, is the operating clock for the USBHS-PHY. The USBMCLK frequency is 12, 20, or 24 MHz supplied from the main clock oscillator.

9.7.8 CAN Clock (CANMCLK)

The CAN clock, CANMCLK, is the operating clock for the CAN module. CANMCLK is generated by the main clock oscillator.

9.7.9 CAC Clock (CACCLK)

The CAC clock, CACCLK, is the operating clock for the CAC. CACCLK is generated by the following oscillators:

- Main clock oscillator
- Sub-clock oscillator
- High-speed clock oscillator (HOCO)
- Middle-speed clock oscillator (MOCO)
- Low-speed on-chip oscillator (LOCO)
- IWDT-dedicated on-chip oscillator.

9.7.10 RTC-Dedicated Clock (RTCSCLK, RTCLCLK)

The RTC-dedicated clocks, RTCSCLK and RTCLCLK, are the operating clocks for the RTC. RTCSCLK is generated by the sub-clock oscillator and RTCLCLK by the LOCO clock.

- SCKDIVCR中的BCK[2:0]位
- SCKSCR中的CKSEL[2:0]位
- PLLCCR中的PLLMUL[5:0]和PLIDIV[1:0]位
- OFS1中的HOCOFRQ0[1:0]位。

不要将BCLK设置为高于系统时钟(ICLK)的频率。

9.7.5 SDRAM Clock (SDCLK)

SDRAM时钟SDCLK 是外部总线控制器的工作时钟。它从连接到外部总线的SDRAM的SDCLK 引脚向外输出。要在SDCLK 引脚上输出SDCLK ，请将SDCKOCR.SDCKOEN位设置为1，并将PmnPFS.PSEL[4:0]位设置为01011b（启用SDCLK 输出）。仅当SDCKOCR.SDCKOEN位为0时更改PmnPFS.PSEL[4:0]位中的值。在以下位中指定频率：

- PLLCCR中的SCKDIVCR.BCK[2:0]、SCKSCR.CKSEL[2:0]、PLLMUL[5:0]和PLIDIV[1:0]位
- OFS1中的HOCOFRQ0[1:0]位。

不要将SDCLK 设置为高于系统时钟(ICLK)的频率。

9.7.6 USB时钟(UCLK)

USB时钟UCLK是USBFS和USBHS模块的工作时钟。必须为USBFS和USBHS模块提供48MHz时钟。使用模块时，UCLK时钟必须指定为48MHz。在以下位中指定频率：

- SCKDIVCR2中的UCK[2:0]位
- SCKSCR中的CKSEL[2:0]位
- PLLCCR中的PLLMUL[5:0]和PLIDIV[1:0]位。

9.7.7 USB-PHY Clock (USBMCLK)

USB-PHY时钟USBMCLK是USBHS-PHY的工作时钟。USBMCLK频率为12、20或24MHz，由主时钟振荡器提供。

9.7.8 CAN时钟(CANMCLK)

CAN时钟CANMCLK是CAN模块的工作时钟。CANMCLK由主时钟振荡器产生。

9.7.9 CAC时钟(CACCLK)

CAC时钟CACCLK是CAC的工作时钟。CACCLK由以下振荡器产生：

- 主时钟振荡器
- Sub-clock oscillator
- 高速时钟振荡器(HOCO)
- 中速时钟振荡器(MOCO)
- Low-speed on-chip oscillator (LOCO)
- IWDT-dedicated on-chip oscillator.

9.7.10 RTC-Dedicated Clock (RTCSCLK, RTCLCLK)

RTC专用时钟RTCSCLK和RTCLCLK是RTC的工作时钟。RTCSCLK由副时钟振荡器产生，RTCLCLK由LOCO时钟产生。

9.7.11 IWDT-Dedicated Clock (IWDTCLK)

The IWDT-dedicated clock, IWDTCLK, is the operating clock for the IWDT. IWDTCLK is internally generated by the IWDT-dedicated on-chip oscillator.

9.7.12 AGT-Dedicated Clock (AGTSCLK, AGTLCLK)

The AGT-dedicated clocks, AGTSCLK and AGTLCLK, are the operating clocks for the AGT. AGTSCLK is generated by the sub-clock oscillator and AGTLCLK is generated by the LOCO clock.

9.7.13 SysTick Timer-Dedicated Clock (SYSTICCLK)

The SysTick timer-dedicated clock, SYSTICCLK, is the operating clock for the SYSTICCLK. SYSTICCLK is generated by the LOCO clock.

9.7.14 Clock/Buzzer Output Clock (CLKOUT)

The CLKOUT is output externally from the CLKOUT pin for the clock or buzzer output. CLKOUT is output to the CLKOUT pin when CKOCR.CKOEN is set to 1. Only change the value in the CKODIV[2:0] or CKOSEL[2:0] bits in CKOCR when the CKOCR.CKOEN bit is 0. Specify the frequency in the following bits:

- CKODIV[2:0] or CKOSEL[2:0] bits in CKOCR
- HOCOFRQ0[1:0] bits in OFS1.

9.7.15 JTAG Clock (JTAGTCK)

The JTAG-dedicated clock, JTAGTCK, is the operating clock for the JTAG. JTAGTCK is generated by the external clock for JTAG (TCK).

9.8 Usage Notes

9.8.1 Constraints on Clock Generation Circuit

The frequencies of the system clock (ICLK), peripheral module clock (PCLKA to PCLKD), flash interface clock (FCLK), external bus clock (BCLK), and SDRAM clock (SDCLK) supplied to each module change according to the settings in SCKDIVCR. Each frequency must meet the following conditions:

- Each frequency must be selected within the operation-guaranteed range of the clock cycle time (tcyc) specified in the AC electrical characteristics. See section 60, Electrical Characteristics.
- The frequencies must not exceed the ranges listed in Table 9.2.
- The peripheral modules operate on PCLKB and PCLKA. As a result, the operating speed of modules such as the timer and SCI is different before and after the frequency is changed.
- The system clock (ICLK), peripheral module clock (PCLKA to PCLKD), flash interface clock (FCLK), and external bus clock (BCLK) must be set as shown in Table 9.2.

Do not change the clock frequency during external bus access. Additionally, when external bus access starts after a change to the clock frequency, always confirm that the frequency changes are complete before starting the access. To ensure correct processing after the clock frequency changes, first write to the relevant clock control register to change the frequency, then read the value from the register, and finally perform the subsequent processing.

9.8.2 Constraints on the Resonator

Because the resonator characteristics relate closely to your board design, adequate evaluation is required before use. See the resonator connection example in Figure 9.9. The circuit constants for the resonator depend on the resonator to be used and the stray capacitance of the mounting circuit. Always consult the resonator manufacturer when determining the circuit constants. The voltage to be applied between the resonator pins must be within the absolute maximum rating.

9.8.3 Constraints on Board Design

When using a crystal resonator, place the resonator and its load capacitors as close to the XTAL and EXTAL pins as possible. Route other signal lines away from the oscillation circuit, as shown in Figure 9.15, to prevent electromagnetic

9.7.11 IWDT-Dedicated Clock (IWDTCLK)

IWDT专用时钟IWDTCLK是IWDT的工作时钟。IWDTCLK由内部产生
IWDT-dedicated on-chip oscillator.

9.7.12 AGT-Dedicated Clock (AGTSCLK, AGTLCLK)

AGT专用时钟AGTSCLK和AGTLCLK是AGT的工作时钟。AGTSCLK由副时钟振荡器产生，AGTLCLK由LOCO时钟产生。

9.7.13 SysTick Timer-Dedicated Clock (SYSTICCLK)

SysTick定时器专用时钟SYSTICCLK是SYSTICCLK的工作时钟。SYSTICCLK由LOCO时钟生成。

9.7.14 时钟蜂鸣器输出时钟(CLKOUT)

CLKOUT从CLKOUT引脚外部输出，用于时钟或蜂鸣器输出。CLKOUT被输出到CKOCR.CKOEN设置为1时的CLKOUT引脚。仅更改CKODIV[2:0]或CKOSEL[2:0]位中的值CKOCR.CKOEN位为0时的CKOCR。在以下位中指定频率：

- CKOCR中的CKODIV[2:0]或CKOSEL[2:0]位
- OFS1中的HOCOFRQ0[1:0]位。

9.7.15 JTAG Clock (JTAGTCK)

JTAG专用时钟JTAGTCK是JTAG的工作时钟。JTAGTCK由JTAG的外部时钟(TCK)生成。

9.8 使用说明

9.8.1 时钟产生电路的约束

提供给每个模块的系统时钟(ICLK)、外围模块时钟(PCLKA至PCLKD)、闪存接口时钟(FCLK)、外部总线时钟(BCLK)和SDRAM时钟(SDCLK)的频率根据SCKDIVCR中的设置而变化.每个频率必须满足以下条件：

- 必须在AC电气特性中规定的时钟周期时间(tcyc)的操作保证范围内选择每个频率。请参见第60节，电气特性。
- 频率不得超过表9.2中列出的范围。
- 外围模块在PCLKB和PCLKA上运行。因此，定时器和SCI等模块在频率改变前后的运行速度是不同的。
- 系统时钟（ICLK）、外设模块时钟（PCLKA到PCLKD）、闪存接口时钟（FCLK）和外部总线时钟（BCLK）必须按照表9.2进行设置。

在外部总线访问期间不要改变时钟频率。此外，在时钟频率更改后开始外部总线访问时，请务必在开始访问之前确认频率更改已完成。为保证时钟频率改变后的正确处理，首先写入相关的时钟控制寄存器改变频率，然后从寄存器中读取值，最后进行后续处理。

9.8.2 对谐振器的约束

由于谐振器特性与您的电路板设计密切相关，因此在使用前需要进行充分评估。请参见图9.9中的谐振器连接示例。谐振器的电路常数取决于要使用的谐振器和安装电路的杂散电容。在确定电路常数时，请务必咨询谐振器制造商。施加在谐振器引脚之间的电压必须在绝对最大额定值范围内。

9.8.3 电路板设计的约束

使用晶体谐振器时，将谐振器及其负载电容尽可能靠近XTAL和EXTAL引脚。将其他信号线远离振荡电路，如图9.15所示，以防止电磁

induction from interfering with correct oscillation.

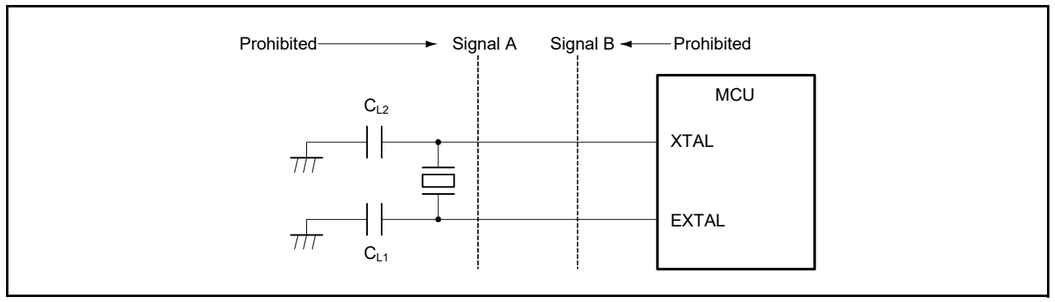


Figure 9.15 Notes on board design for oscillation circuit (applicable to the sub-clock oscillator as well as main clock oscillator)

9.8.4 Constraints on the Resonator Connect Pin

When the main clock oscillator is not used, the EXTAL and XTAL pins can be used as general ports P212 and P213. When these pins are used as general ports, the main clock oscillator must be stopped (MOSCCR.MOSTP must be set to 1).

9.8.5 Constraints on Using Sub-Clock Oscillator for BGA and LGA Packages

The output of the P212 (EXTAL) and P213 (XTAL) pins may affect the oscillation by the sub-clock oscillator.

If the sub-clock oscillator is used, implement the board design so as not to affect to the oscillation. Renesas strongly recommends setting the DSCR[1:0] bits to 00b or 01b when using P212 (EXTAL) and P213 (XTAL) as output pins and using the sub-clock oscillator.

In addition, when using the sub-clock oscillator in middle drive capability (SOMCR.SODRV1 = 1), Renesas recommends not to use P212 (EXTAL) and P213 (XTAL) simultaneously as output pins to avoid affecting the oscillation.

9.8.6 Constraints on the Main Clock Oscillator Drive Capability Auto Switching Function

The drive capability auto switching function lowers the main clock oscillator drive capability automatically after the main clock oscillator starts and suppresses the EMI associated with the main clock oscillator.

To enable drive capability auto switching, set MOMCR.AUTODRVEN to 1 while the main clock oscillator is stopped (MOSCCR.MOSTP = 1). Regardless of the MOMCR.AUTODRVEN setting, the drive capability switching register (MOMCR.MODRV0[1:0]) must be set properly according to the selected oscillator.

Then, enable the main clock oscillator (MOSCCR.MOSTP = 0). After the oscillation stabilization flag (OSCSF.MOSCSF) becomes 1, the main clock can be used.

EMI suppression is gained in return for an extension in the oscillation stabilization wait time. For more information, see section 9.2.18, Main Clock Oscillator Wait Control Register (MOSCWTCR).

感应干扰正确的振荡。

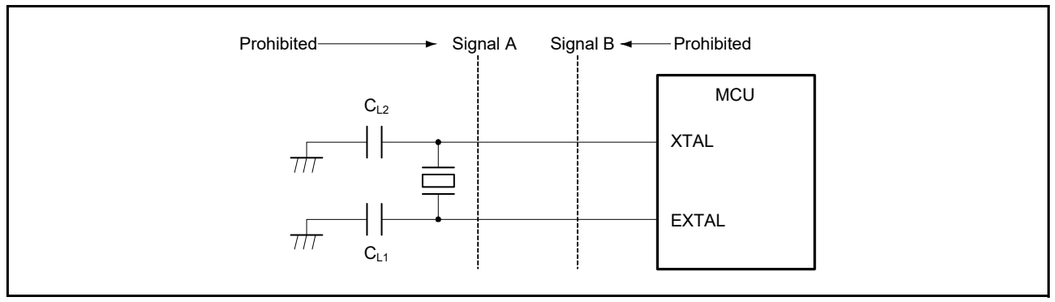


Figure 9.15 振荡电路板设计注意事项（适用于副时钟振荡器和主时钟振荡器）

9.8.4 谐振器连接引脚上的约束

当不使用主时钟振荡器时，EXTAL和XTAL引脚可用作通用端口P212和P213。
当这些引脚用作通用端口时，必须停止主时钟振荡器（MOSCCR.MOSTP必须设置为1）。

9.8.5 BGA和LGA封装使用副时钟振荡器的限制

P212(EXTAL)和P213(XTAL)引脚的输出可能会影响副时钟振荡器的振荡。

如果使用副时钟振荡器，请在不影响振荡的情况下进行板卡设计。当使用P212(EXTAL)和P213(XTAL)作为输出引脚并使用副时钟振荡器时，瑞萨强烈建议将DSCR[1:0]位设置为00b或01b。

另外，在中间驱动能力（SOMCR.SODRV1=1）中使用副时钟振荡器时，瑞萨推荐不要同时使用P212（EXTAL）和P213（XTAL）作为输出引脚，以免影响振荡。

9.8.6 主时钟振荡器驱动能力自动切换的约束 Function

驱动能力自动切换功能在主时钟振荡器启动后自动降低主时钟振荡器的驱动能力，并抑制与主时钟振荡器相关的EMI。

要启用驱动能力自动切换，在主时钟振荡器停止(M OSCCR.MOSTP=1)时将MOMCR.AUTODRVEN设置为1。无论MOMCR.AUTODRVEN设置如何，驱动能力切换寄存器(MOMCR.MODRV0[1:0])必须根据所选振荡器正确设置。

然后，使能主时钟振荡器（MOSCCR.MOSTP=0）。振荡稳定标志(OSCSF.MOSCSF)变为1后，可以使用主时钟。

获得EMI抑制以换取振荡稳定等待时间的延长。有关详细信息，请参阅第9.2.18节，主时钟振荡器等待控制寄存器(MOSCWTCR)。

10. Clock Frequency Accuracy Measurement Circuit (CAC)

10.1 Overview

The Clock Frequency Accuracy Measurement Circuit (CAC) counts pulses of the clock to be measured (measurement target clock) within the time generated by the clock selected as the measurement reference (measurement reference clock), and determines the accuracy depending on whether the number of pulses is within the allowable range.

The reference clock can be provided externally through an I/O port pin or internally from various on-chip oscillators. Interrupt signals can be generated when the clock does not match or measurement ends. This feature is useful in implementing a fail-safe mechanism for home and industrial automation applications.

Table 10.1 lists the CAC specifications, Figure 10.1 shows a block diagram, and Table 10.2 describes the I/O pin.

Table 10.1 CAC specifications

Parameter	Specifications
Measurement target clocks	Frequency can be measured for: • Main clock oscillator • Sub-clock oscillator • HOCO clock • MOCO clock • LOCO clock • IWDTCLK clock • Peripheral module clock B (PCLKB)
Measurement reference clocks	Frequency can be referenced to: • External clock input to the CACREF pin • Main clock oscillator • Sub-clock oscillator • HOCO clock • MOCO clock • LOCO clock • IWDTCLK clock • Peripheral module clock B (PCLKB)
Selectable function	Digital filter
Interrupt sources	• Measurement end • Frequency error • Overflow
Module-stop function	Module-stop state can be set to reduce power consumption

10. 时钟频率精度测量电路(CAC)

10.1 Overview

时钟频率精度测量电路(CAC)在被选为测量基准的时钟（测量基准时钟）产生的时间内对要测量的时钟（测量目标时钟）的脉冲进行计数，并根据脉冲在允许范围内。

参考时钟可以通过IO端口引脚从外部提供，也可以从各种片上振荡器内部提供。
当时钟不匹配或测量结束时会产生中断信号。此功能可用于为家庭和工业自动化应用实施故障安全机制。

表10.1列出了CAC规格，图10.1显示了框图，表10.2描述了IO引脚。

Table 10.1 CAC规格

Parameter	Specifications
测量目标时钟	频率可以测量： 主时钟振荡器 子时钟振荡器 HOCO时钟 MOCO时钟 LOCO时钟 IWDTCLK时钟 外围模块时钟B(PCLKB)
测量参考时钟	频率可以参考： CACREF引脚的外部时钟输入 主时钟振荡器 子时钟振荡器 HOCO时钟 MOCO时钟 LOCO时钟 IWDTCLK时钟 外设模块时钟B(PCLKB)
可选择的功能	数字滤波器
中断源	测量结束 频率误差溢出
Module-stop function	可设置模块停止状态以降低功耗

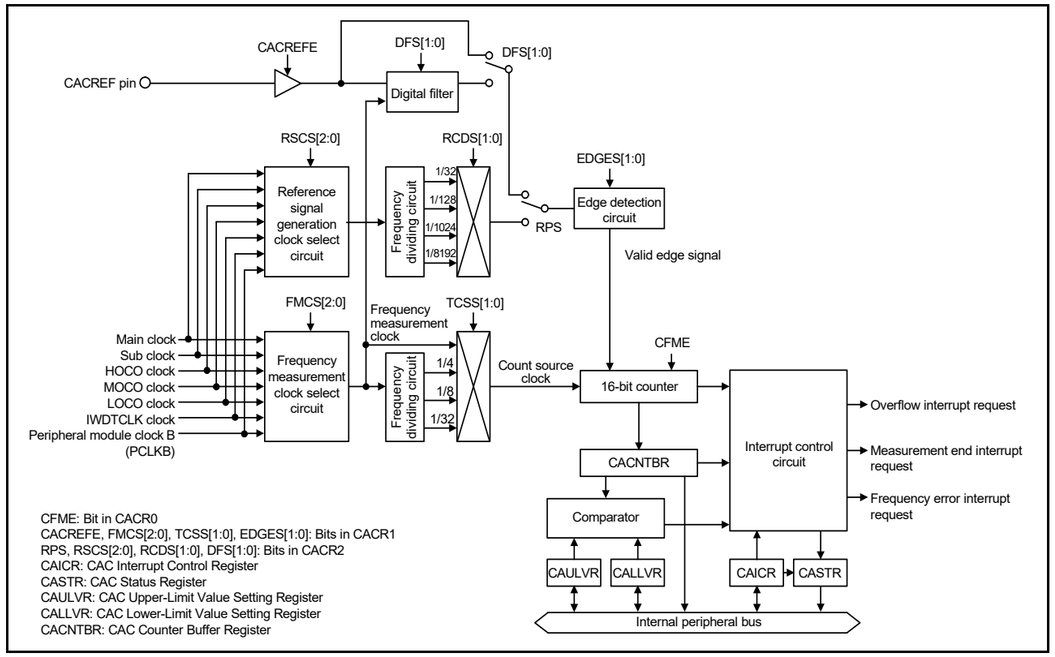


Figure 10.1 CAC block diagram

Table 10.2 CAC I/O pin

Pin name	I/O	Function
CACREF	Input	Measurement reference clock input pin

10.2 Register Descriptions

10.2.1 CAC Control Register 0 (CACR0)

Address(es): CAC.CACR0 4004 4600h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	CFME
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	CFME	Clock Frequency Measurement Enable	0: Disable 1: Enable.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

CFME bit (Clock Frequency Measurement Enable)

The CFME bit enables clock frequency measurement. Read the CFME bit to confirm that the bit value has changed. Additional write accesses are ignored before the change is complete.

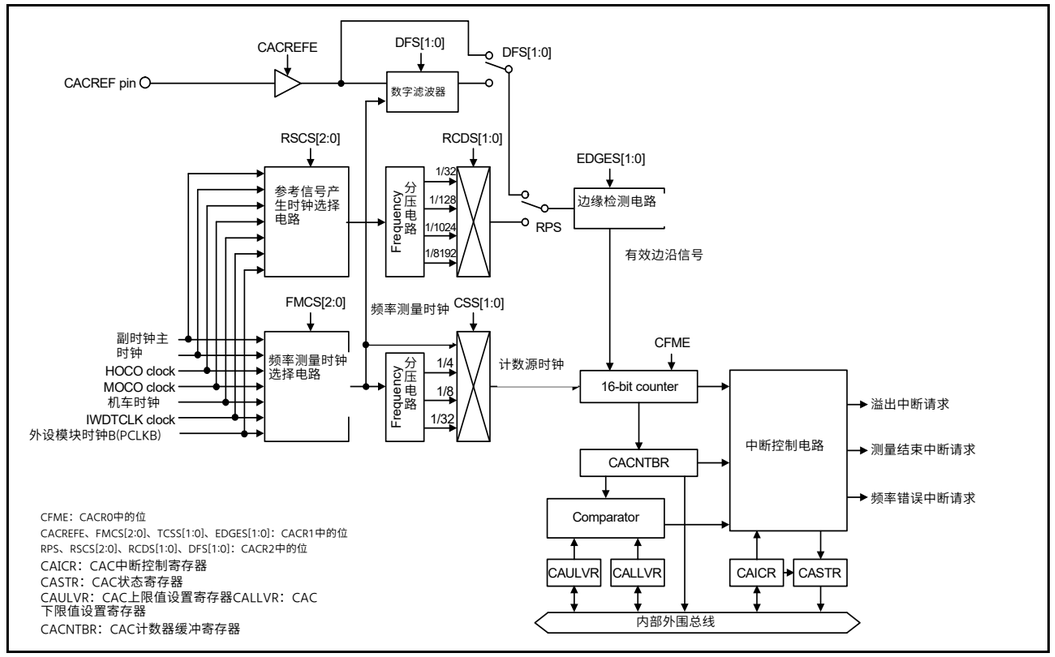


Figure 10.1 CAC框图

Table 10.2 CACIO引脚

引脚名称	I/O	Function
CACREF	Input	测量参考时钟输入引脚

10.2 注册说明

10.2.1 CAC控制寄存器0(CACR0)

Address(es): CAC.CACR0 4004 4600h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	CFME
重置后的值：	0	0	0	0	0	0	0	0

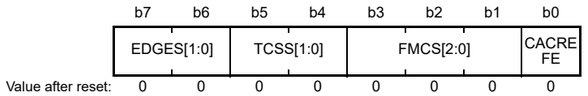
Bit	Symbol	位名称	Description	R/W
b0	CFME	时钟频率测量启用	0：禁用1 ：启用。	R/W
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

CFME位（时钟频率测量使能）

CFME位使能时钟频率测量。读取CFME位以确认该位值已更改。
在更改完成之前，将忽略其他写入访问。

10.2.2 CAC Control Register 1 (CACR1)

Address(es): CAC.CACR1 4004 4601h



Bit	Symbol	Bit name	Description	R/W
b0	CACREFE	CACREF Pin Input Enable	0: Disable 1: Enable.	R/W
b3 to b1	FMCS[2:0]	Measurement Target Clock Select	b3 b1 0 0 0: Main clock oscillator 0 0 1: Sub-clock oscillator 0 1 0: HOCO clock 0 1 1: MOCO clock 1 0 0: LOCO clock 1 0 1: Peripheral module clock (PCLKB) 1 1 0: IWDTCLK clock 1 1 1: Setting prohibited.	R/W
b5, b4	TCSS[1:0]	Measurement Target Clock Frequency Division Ratio Select	b5 b4 0 0: No division 0 1: ×1/4 clock 1 0: ×1/8 clock 1 1: ×1/32 clock.	R/W
b7, b6	EDGES[1:0]	Valid Edge Select	b7 b6 0 0: Rising edge 0 1: Falling edge 1 0: Both rising and falling edges 1 1: Setting prohibited.	R/W

Note: Set the CACR1 register when the CACR0.CFME bit is 0.

CACREFE bit (CACREF Pin Input Enable)

The CACREFE bit enables the CACREF pin input.

FMCS[2:0] bits (Measurement Target Clock Select)

The FMCS[2:0] bits select the clock for which the frequency is to be measured.

TCSS[1:0] bits (Measurement Target Clock Frequency Division Ratio Select)

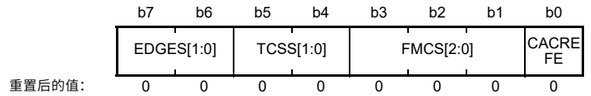
The TCSS[1:0] bits select the division ratio of the measurement target clock.

EDGES[1:0] bits (Valid Edge Select)

The EDGES[1:0] bits select the valid edge for the reference signal.

10.2.2 CAC控制寄存器1(CACR1)

Address(es): CAC.CACR1 4004 4601h



Bit	Symbol	位名称	Description	R/W
b0	CACREFE	CACREF引脚输入使能	0：禁用1 ：启用。	R/W
b3 to b1	FMCS[2:0]	测量目标时钟选择	b3b1000：主时钟振荡器001：副时钟振荡器010：HOCO时钟011：MOCO时钟100：LOCO时钟101：外围模块时钟（PCLKB）110：IWDTCLK时钟111：禁止设置。	R/W
b5, b4	TCSS[1:0]	测量目标时钟 分频比选择	b5b400：不分频 01：×14个时钟1 0：×18个时钟11 ：×132个时钟。	R/W
b7, b6	EDGES[1:0]	有效边选择	b7b600：上升沿01：下降沿10：上升沿和下降沿11：禁止设置。	R/W

Note: 当CACR0.CFME位为0时设置CACR1寄存器。

CACREFE位（CACREF引脚输入使能）

CACREFE位使能CACREF引脚输入。

FMCS[2:0]位（测量目标时钟选择）

FMCS[2:0]位选择要测量频率的时钟。

TCSS[1:0]位（测量目标时钟分频比选择）

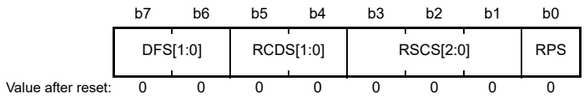
TCSS[1:0]位选择测量目标时钟的分频比。

EDGES[1:0]位（有效边沿选择）

EDGES[1:0]位选择参考信号的有效边沿。

10.2.3 CAC Control Register 2 (CACR2)

Address(es): CAC.CACR2 4004 4602h



Bit	Symbol	Bit name	Description	R/W
b0	RPS	Reference Signal Select	0: CACREF pin input 1: Internal clock (internally generated signal).	R/W
b3 to b1	RSCS[2:0]	Measurement Reference Clock Select	b3 b1 0 0 0: Main clock oscillator 0 0 1: Sub-clock oscillator 0 1 0: HOCO clock 0 1 1: MOCO clock 1 0 0: LOCO clock 1 0 1: Peripheral module clock (PCLKB) 1 1 0: IWDTCLK clock 1 1 1: Setting prohibited.	R/W
b5, b4	RCDS[1:0]	Measurement Reference Clock Frequency Division Ratio Select	b5 b4 0 0: ×1/32 clock 0 1: ×1/128 clock 1 0: ×1/1024 clock 1 1: ×1/8192 clock.	R/W
b7, b6	DFS[1:0]	Digital Filter Select	b7 b6 0 0: Disable digital filtering 0 1: Use sampling clock for the digital filter as the frequency measuring clock 1 0: Use sampling clock for the digital filter as the frequency measuring clock divided by 4 1 1: Use sampling clock for the digital filter as the frequency measuring clock divided by 16.	R/W

Note: Set the CACR2 register when the CACR0.CFME bit is 0.

RPS bit (Reference Signal Select)

The RPS bit selects whether to use the CACREF pin input or an internal clock (internally generated signal) as the reference signal.

RSCS[2:0] bits (Measurement Reference Clock Select)

The RSCS[2:0] bits select the clock source for generating the measurement reference clock.

RCDS[1:0] bits (Measurement Reference Clock Frequency Division Ratio Select)

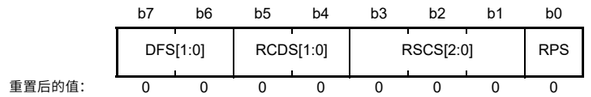
The RCDS[1:0] bits select the frequency division ratio of the measurement reference clock, when an internal reference clock is selected (RPS = 1). When RPS = 0 (CACREF pin is used as the reference clock source), the reference clock is not divided.

DFS[1:0] bits (Digital Filter Select)

The setting of the DFS[1:0] bits enables or disables the digital filter and selects its sampling clock.

10.2.3 CAC控制寄存器2(CACR2)

Address(es): CAC.CACR2 4004 4602h



Bit	Symbol	位名称	Description	R/W
b0	RPS	参考信号选择	0：CACREF引脚输入1：内部时钟（内部产生的信号）。	R/W
b3 to b1	RSCS[2:0]	测量参考时钟Select	b3b1000：主时钟振荡器001：副时钟振荡器010：HOCO时钟011：MOCO时钟100：LOCO时钟101：外围模块时钟（PCLKB）110：IWDTCLK时钟111：禁止设置。	R/W
b5, b4	RCDS[1:0]	测量参考时钟分频比选择	b5 b4 0 0: ×1/32 clock 0 1: ×1/128 clock 1 0: ×1/1024 clock 1 1: ×1/8192 clock.	R/W
b7, b6	DFS[1:0]	数字滤波器选择	b7b600：禁用数字滤波01：使用数字滤波器的采样时钟作为频率测量时钟10：使用数字滤波器的采样时钟作为频率测量时钟除以411：使用数字滤波器的采样时钟滤波器作为频率测量时钟除以16。	R/W

Note: 当CACR0.CFME位为0时设置CACR2寄存器。

RPS位（参考信号选择）

RPS位选择是使用CACREF引脚输入还是使用内部时钟（内部产生的信号）作为参考信号。

RSCS[2:0]位（测量参考时钟选择）

RSCS[2:0]位选择生成测量参考时钟的时钟源。

RCDS[1:0]位（测量参考时钟分频比选择）

TheRCDS[1:0]bitsselectthefrequencydivisionratiooftheMeasurementReferenceClock whenaninternalreferenceclockisselected(RPS=1).当RPS=0（CACREF引脚用作参考时钟源）时，参考时钟不分频。

DFS[1:0]位（数字滤波器选择）

DFS[1:0]位的设置启用或禁用数字滤波器并选择其采样时钟。

10.2.4 CAC Interrupt Control Register (CAICR)

Address(es): CAC.CAICR 4004 4603h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	OVFFCL	MENDFCL	FERRFCL	—	OVFIE	MENDIE	FERRIE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	FERRIE	Frequency Error Interrupt Request Enable	0: Disable 1: Enable.	R/W
b1	MENDIE	Measurement End Interrupt Request Enable	0: Disable 1: Enable.	R/W
b2	OVFIE	Overflow Interrupt Request Enable	0: Disable 1: Enable.	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	FERRFCL	FERRF Clear	When 1 is written to this bit, the CASTR.FERRF flag is cleared. This bit is read as 0.	R/W
b5	MENDFCL	MENDF Clear	When 1 is written to this bit, the CASTR.MENDF flag is cleared. This bit is read as 0.	R/W
b6	OVFFCL	OVFF Clear	When 1 is written to this bit, the CASTR.OVFF flag is cleared. This bit is read as 0.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

FERRIE bit (Frequency Error Interrupt Request Enable)

The FERRIE bit enables the frequency error interrupt request.

MENDIE bit (Measurement End Interrupt Request Enable)

The MENDIE bit enables the measurement end interrupt request.

OVFIE bit (Overflow Interrupt Request Enable)

The OVFIE bit enables the overflow interrupt request.

FERRFCL bit (FERRF Clear)

Writing 1 to the FERRFCL bit to 1 clears the CASTR.FERRF flag.

MENDFCL bit (MENDF Clear)

Writing 1 to the MENDFCL bit to 1 clears the CASTR.MENDF flag.

OVFFCL bit (OVFF Clear)

Writing 1 to the OVFFCL bit to 1 clears the CASTR.OVFF flag.

10.2.4 CAC中断控制寄存器(CAICR)

Address(es): CAC.CAICR 4004 4603h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	OVFFCL	MENDFCL	FERRFCL	—	OVFIE	MENDIE	FERRIE
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	FERRIE	频率错误中断请求 Enable	0：禁用1 ：启用。	R/W
b1	MENDIE	测量结束中断 请求启用	0：禁用1 ：启用。	R/W
b2	OVFIE	溢出中断请求使能	0：禁用1 ：启用。	R/W
b3	—	Reserved	该位读取为0。写入值应为0。	R/W
b4	FERRFCL	FERRF Clear	向该位写入1时，清除CASTR.FERRF标志。该位读为0。	R/W
b5	MENDFCL	MENDF Clear	向该位写入1时，清除CASTR.MENDF标志。该位读为0。	R/W
b6	OVFFCL	OVFF Clear	向该位写入1时，清除CASTR.OVFF标志。 该位读为0。	R/W
b7	—	Reserved	该位读取为0。写入值应为0。	R/W

FERRIE位（频率错误中断请求使能）

FERRIE位使能频率错误中断请求。

MENDIE位（测量结束中断请求使能）

MENDIE位使能测量结束中断请求。

OVFIE位（溢出中断请求使能）

OVFIE位使能溢出中断请求。

FERRFCL位（FERRF清除）

将1写入FERRFCL位到1会清除CASTR.FERRF标志。

MENDFCL位（MENDF清除）

将1写入MENDFCL位到1会清除CASTR。MENDF标志。

OVFFCL位（OVFF清除）

将1写入OVFFCL位到1会清除CASTR。OVFF标志。

10.2.5 CAC Status Register (CASTR)

Address(es): CAC.CASTR 4004 4604h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	OVFF	MENDF	FERRF
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	FERRF	Frequency Error Flag	0: Clock frequency is within the allowable range 1: Clock frequency has deviated beyond the allowable range (frequency error).	R
b1	MENDF	Measurement End Flag	0: Measurement is in progress 1: Measurement ended.	R
b2	OVFF	Overflow Flag	0: Counter has not overflowed 1: Counter overflowed.	R
b7 to b3	—	Reserved	These bits are read as 0.	R

FERRF flag (Frequency Error Flag)

The FERRF flag indicates a deviation of the clock frequency from the set value (frequency error).

[Setting condition]

- The clock frequency is outside the allowable range defined in the CAULVR and CALLVR registers.

[Clearing condition]

- 1 is written to the FERRFCL bit.

MENDF flag (Measurement End Flag)

The MENDF flag indicates the end of measurement.

[Setting condition]

- Measurement completes.

[Clearing condition]

- 1 is written to the MENDFCL bit.

OVFF flag (Overflow Flag)

The OVFF flag indicates that the counter overflowed.

[Setting condition]

- The counter overflows.

[Clearing condition]

- 1 is written to the OVFFCL bit.

10.2.5 CAC状态寄存器(CASTR)

Address(es): CAC.CASTR 4004 4604h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	OVFF	MENDF	FERRF
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	FERRF	频率错误标志	0：时钟频率在允许范围内1：时钟频率偏离允许范围（频率误差）。	R
b1	MENDF	测量结束标志	0：测量中1：测量结束。	R
b2	OVFF	溢出标志	0：计数器未溢出1：计数器溢出。	R
b7 to b3	—	Reserved	这些位读为0。	R

FERRF标志（频率误差标志）

FERRF标志表示时钟频率与设定值的偏差（频率误差）。

[Setting condition]

- 时钟频率超出CAULVR和CALLVR寄存器中定义的允许范围。

[Clearing condition]

- 1被写入FERRFCL位。

MENDF标志（测量结束标志）

MENDF标志表示测量结束。

[Setting condition]

- 测量完成。

[Clearing condition]

- 1被写入MENDFCL位。

OVFF标志（溢出标志）

OVFF标志表示计数器溢出。

[Setting condition]

- 计数器溢出。

[Clearing condition]

- 1写入OVFFCL位。

10.2.6 CAC Upper-Limit Value Setting Register (CAULVR)

Address(es): CAC.CAULVR 4004 4606h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CAULVR is a 16-bit read/write register that specifies the upper value of the allowable range. When the counter value exceeds the value specified in this register, a frequency error is detected. Write to this register when the CACR0.CFME bit is 0.

The counter value stored in CACNTBR can vary depending on the difference between the phases of the digital filter and edge-detection circuit and the signal on the CACREF pin. Ensure that this setting allows an adequate margin.

10.2.7 CAC Lower-Limit Value Setting Register (CALLVR)

Address(es): CAC.CALLVR 4004 4608h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CALLVR is a 16-bit read/write register that specifies the lower value of the allowable range. When the counter value falls below the value specified in this register, a frequency error is detected. Write to this register when the CACR0.CFME bit is 0.

The counter value stored in CACNTBR can vary depending on the difference between the phases of the digital filter and edge-detection circuit and the signal on the CACREF pin. Ensure that this setting allows an adequate margin.

10.2.8 CAC Counter Buffer Register (CACNTBR)

Address(es): CAC.CACNTBR 4004 460Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CACNTBR is a 16-bit read-only register that stores the measurement result.

10.3 Operation

10.3.1 Measuring Clock Frequency

The CAC measures the clock frequency using the CACREF pin input or an internal clock as a reference. Figure 10.2 shows an operating example of the CAC.

10.2.6 CAC上限值设置寄存器(CAULVR)

Address(es): CAC.CAULVR 4004 4606h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CAULVR是一个16位读写寄存器，用于指定允许范围的上限值。当计数器值超过此寄存器中指定的值时，检测到频率错误。当CACR0.CFME位为0时写入该寄存器。

存储在CACNTBR中的计数器值会根据数字滤波器和边沿检测电路的相位以及CACREF引脚上的信号之间的差异而变化。确保此设置允许有足够的余量。

10.2.7 CAC下限值设置寄存器(CALLVR)

Address(es): CAC.CALLVR 4004 4608h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CALLVR是一个16位读写寄存器，用于指定允许范围的下限值。当计数器值低于此寄存器中指定的值时，检测到频率错误。当CACR0.CFME位为0时写入该寄存器。

存储在CACNTBR中的计数器值会根据数字滤波器和边沿检测电路的相位以及CACREF引脚上的信号之间的差异而变化。确保此设置允许有足够的余量。

10.2.8 CAC计数器缓冲寄存器(CACNTBR)

Address(es): CAC.CACNTBR 4004 460Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CACNTBR是一个16位只读寄存器，用于存储测量结果。

10.3 Operation

10.3.1 测量时钟频率

CAC使用CACREF引脚输入或内部时钟作为参考来测量时钟频率。图10.2显示了CAC的操作示例。

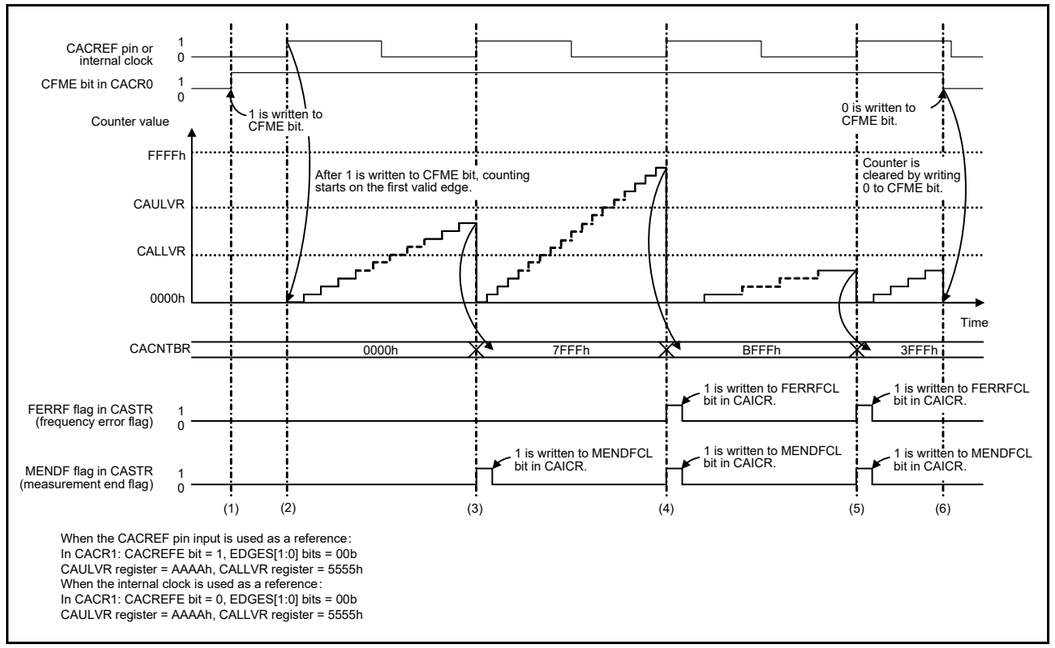


Figure 10.2 CAC operating example

The events in Figure 10.2 are:

1. Before writing 1 to CACR0.CFME, set CACR1 and CACR2 to define the measurement target clock and measurement reference clock. Writing 1 to the CACR0.CFME bit enables clock frequency measurement.
2. The timer starts counting up if the valid edge selected in the CACR1.EDGES[1:0] bits is input from the measurement reference clock. In Figure 10.2, the valid edge is a rising edge (CACR1.EDGES[1:0] = 00b).
3. When the next valid edge is input, the counter value is transferred to CACNTBR and compared with the values in CAULVR and CALLVR. If both CACNTBR ≤ CAULVR and CACNTBR ≥ CALLVR are true, only the MENDF flag in CASTR is set to 1, because the clock frequency is correct. If the MENDIE bit in CAICR is 1, a measurement end interrupt is generated.
4. When the next valid edge is input, the counter value is transferred to CACNTBR and compared with the values in CAULVR and CALLVR. If CACNTBR > CAULVR, the FERRF flag in CASTR is set to 1, because the clock frequency is erroneous. If the FERRIE bit in CAICR is 1, a frequency error interrupt is generated. The MENDF flag in CASTR is set to 1 at the end of measurement. If the MENDIE bit in CAICR is 1, a measurement end interrupt is generated.
5. When the next valid edge is input, the counter value is transferred to CACNTBR and compared with the values in CAULVR and CALLVR. If CACNTBR < CALLVR, the FERRF flag in CASTR is set to 1, because the clock frequency is erroneous. If the FERRIE bit in CAICR is 1, a frequency error interrupt is generated. The MENDF flag in CASTR is set to 1 at the end of measurement. If the MENDIE bit in CAICR is 1, a measurement end interrupt is generated.
6. When the CFME bit in CACR0 is 1, the counter value is transferred to CACNTBR and compared with the values in CAULVR and CALLVR every time a valid edge is input. Writing 0 to the CFME bit in CACR0 clears the counter and stops up-counting.

10.3.2 Digital Filtering of Signals on CACREF Pin

The CACREF pin has a digital filter, and levels on the CACREF pin are transmitted to the internal circuitry after three consecutive matches in the selected sampling interval. The same level continues to be transmitted internally until the level on the pin has three consecutive matches again. Enabling or disabling of the digital filter and its sampling clock are

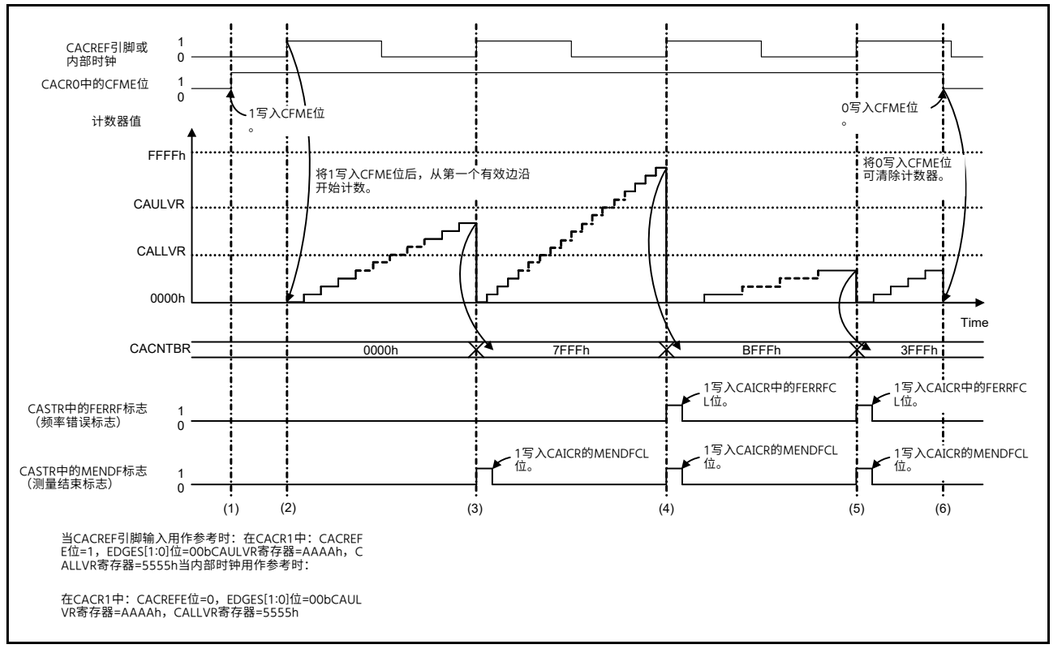


Figure 10.2 CAC操作示例

图10.2中的事件是：

1. 在向CACR0.CFME写入1之前，设置CACR1和CACR2以定义测量目标时钟和测量参考时钟。向CACR0.CFME位写入1可启用时钟频率测量。
2. 如果在CACR1.EDGES[1:0]位中选择的有效边沿从测量参考时钟输入，则定时器开始计数。在图10.2中，有效边沿是上升沿(CACR1.EDGES[1:0]=00b)。
3. 当输入下一个有效边沿时，计数器值被传送到CACNTBR并与CAULVR和CALLVR中的值进行比较。如果CACNTBR≤CAULVR和CACNTBR≥CALLVR都为真，则只有CASTR中的MENDF标志设置为1，因为时钟频率是正确的。如果CAICR中的MENDIE位为1，则产生测量结束中断。
4. 当输入下一个有效边沿时，计数器值被传送到CACNTBR并与CAULVR和CALLVR中的值进行比较。如果CACNTBR>CAULVR，则CASTR中的FERRF标志设置为1，因为时钟频率错误。如果CAICR中的FERRIE位为1，则产生频率错误中断。CASTR中的MENDF标志在测量结束时设置为1。如果CAICR中的MENDIE位为1，则产生测量结束中断。
5. 当输入下一个有效边沿时，计数器值被传送到CACNTBR并与CAULVR和CALLVR中的值进行比较。如果CACNTBR<CALLVR，则CASTR中的FERRF标志设置为1，因为时钟频率错误。如果CAICR中的FERRIE位为1，则产生频率错误中断。CASTR中的MENDF标志在测量结束时设置为1。如果CAICR中的MENDIE位为1，则产生测量结束中断。
6. 当CACR0中的CFME位为1时，每次输入有效边沿时，计数器值被传送到CACNTBR并与CAULVR和CALLVR中的值进行比较。向CACR0中的CFME位写入0将清除计数器并停止向上计数。

10.3.2 CACREF引脚上的信号数字滤波

CACREF引脚有一个数字滤波器，CACREF引脚上的电平在选定的采样间隔内连续三个匹配后传输到内部电路。同一电平继续在内部传输，直到引脚上的电平再次连续匹配三个。启用或禁用数字滤波器及其采样时钟

selectable.

The counter value transferred to CACNTBR might be in error by up to one cycle of the sampling clock because of the difference between the phases of the digital filter and the signal input to the CACREF pin. When a frequency dividing clock is selected as a count source clock, the counter value error is obtained by the following formula:

Counter value error = (One cycle of the count source clock) / (One cycle of the sampling clock)

10.4 Interrupt Requests

The CAC generates three interrupt requests:

- Frequency error interrupt
- Measurement end interrupt
- Overflow interrupt.

When an interrupt source is generated, the associated status flag is set to 1. Table 10.3 provides information on the CAC interrupt requests.

Table 10.3 CAC interrupt requests

Interrupt request	Interrupt enable bit	Status flag	Interrupt sources
Frequency error interrupt	CAICR.FERRIE	CASTR.FERRF	Result of comparing CACNTBR with CAULVR and CALLVR is either CACNTBR > CAULVR or CACNTBR < CALLVR
Measurement end interrupt	CAICR.MENDIE	CASTR.MENDF	• Valid edge is input from the CACREF pin or internal clock • Measurement end interrupt does not occur at the first valid edge after writing 1 to the CACR0.CFME bit.
Overflow interrupt	CAICR.OVFIE	CASTR.OVFF	Counter overflows

10.5 Usage Notes

10.5.1 Settings for the Module-Stop Function

CAC operation can be disabled or enabled using Module Stop Control Register C (MSTPCRC). The CAC module is initially stopped after reset. Releasing the module-stop state enables access to the registers. For details, see section 11, Low Power Modes.

selectable.

由于数字滤波器的相位和输入到CACREF引脚的信号之间存在差异，传输到CACNTBR的计数器值可能会出现最多一个采样时钟周期的错误。Whenafrequencydividingclockisselectedasacountsourceclock thecounterval ueerrorisobtainedbythefollowingformula:

计数器值误差=（计数源时钟的一个周期）（采样时钟的一个周期）

10.4 中断请求

CAC产生三个中断请求：

- 频率错误中断
- 测量结束中断
- 溢出中断。

产生中断源时，相关状态标志设置为1。表10.3提供了有关CAC中断请求的信息。

Table 10.3 CAC中断请求

中断请求	中断使能位	状态标志	中断源
频率错误中断	CAICR.FERRIE	CASTR.FERRF	CACNTBR与CAULVR和CALLVR的比较结果是CACNTBR>CAULVR或CACNTBR<CALLVR
测量结束中断	CAICR.MENDIE	CASTR.MENDF	从CACREF引脚或内部时钟输入有效边沿 将1写入CACR0.CFME位后，在第一个有效边沿不会发生测量结束中断。
溢出中断	CAICR.OVFIE	CASTR.OVFF	计数器溢出

10.5 使用说明

10.5.1 模块停止功能的设置

可以使用模块停止控制寄存器C(MSTPCRC)禁用或启用CAC操作。CAC模块在复位后最初停止。释放模块停止状态可以访问寄存器。有关详细信息，请参阅第11节，低功耗模式。

11. Low Power Modes

11.1 Overview

The MCU provides several functions for reducing power consumption, such as setting clock dividers, controlling EBCLK output, controlling SDCLK output, stopping modules, selecting power control mode in normal mode, and transitioning to low power modes.

Table 11.1 lists the specifications of the low power mode functions. Table 11.2 list the conditions to transition to low power modes, the states of the CPU and peripheral modules, and the method for canceling each mode. After a reset, the MCU enters the program execution state, but only the DMAC, DTC, and SRAM operate.

Table 11.1 Specifications of the low power mode functions

Parameter	Specifications
Reducing power consumption by switching clock signals	The frequency division ratio can be selected independently for the system clock (ICLK), peripheral module clocks (PCLKA, PCLKB, PCLKC, PCLKD), external bus clock (BCLK), and flash interface clock (FCLK)*1
EBCLK output control	Selectable to BCLK output or high-level output
SDCLK output control	Selectable to SDCLK output or high-level output
Module-stop state	Peripheral module functions can be stopped independently
Low power modes	• Sleep mode • Software Standby mode • Snooze mode • Deep Software Standby mode.
Power control modes	Power consumption can be reduced in Normal, Sleep, and Snooze modes by selecting an appropriate operating power control mode according to the operating frequency and voltage. Three operating power control modes are available: • High-speed mode • Low-speed mode • Subosc-speed mode.

Note 1. For details, refer to section 9, Clock Generation Circuit.

Table 11.2 Operating conditions of each low power mode (1 of 3)

Parameter	Sleep mode	Software Standby mode	Snooze mode*1	Deep Software Standby mode
Transition condition	WFI instruction while SBYCR.SSBY = 0	WFI instruction while SBYCR.SSBY = 1 and DPSBYCR.DPSBY = 0	Snooze request trigger in Software Standby mode. SNZCR.SNZE = 1	WFI instruction while SBYCR.SSBY = 1 and DPSBYCR.DPSBY = 1
Canceling method	All interrupts. Any reset available in the mode.	Interrupts shown in Table 11.3. Any reset available in the mode.	Interrupts shown in Table 11.3. Any reset available in the mode.	Interrupts shown in Table 11.3. Any reset available in the mode.
State after cancellation by an interrupt	Program execution state (interrupt processing)	Program execution state (interrupt processing)	Program execution state (interrupt processing)	Reset state
State after cancellation by a reset	Reset state	Reset state	Reset state	Reset state
Main clock oscillator	Selectable	Stop	Selectable*2	Stop
Sub-clock oscillator	Selectable	Selectable	Selectable	Selectable
High-speed on-chip oscillator	Selectable	Stop	Selectable	Stop
Middle-speed on-chip oscillator	Selectable	Stop	Selectable	Stop
Low-speed on-chip oscillator	Selectable	Selectable	Selectable	Selectable*3

11. 低功耗模式

11.1 Overview

MCU提供了多种降低功耗的功能，例如设置时钟分频器、控制EBCLK输出、控制SDCLK 输出、停止模块、在正常模式下选择电源控制模式以及转换到低功耗模式。

表11.1列出了低功耗模式功能的规格。表11.2列出了转换到低功耗模式的条件、CPU和外围模块的状态以及取消每种模式的方法。复位后，MCU进入程序执行状态，但只有DMAC、DTC和SRAM运行。

Table 11.1 低功耗模式功能的规格

Parameter	Specifications
通过切换时钟信号降低功耗	分频比可独立选择系统时钟（ICLK）、外围模块时钟（PCLKA、PCLKB、PCLKC、PCLKD）、外部总线时钟（BCLK）和闪存接口时钟（FCLK）*1
EBCLK输出控制	可选择BCLK输出或高电平输出
SDCLK 输出控制	可选择SDCLK 输出或高电平输出
Module-stop state	外围模块功能可独立停止
低功耗模式	睡眠模式 软件待机模式 贪睡模式 深度软件待机模式。
电源控制模式	通过根据工作频率和电压选择合适的工作功率控制模式，可以降低Normal、Sleep和Snooze模式下的功耗。提供三种工作功率控制模式： 高速模式 低速模式 Subosc速度模式。

Note 1. 有关详细信息，请参阅第9节，时钟生成电路。

Table 11.2 每种低功耗模式的操作条件（3个中的1个）

Parameter	睡眠模式	软件待机模式	Snooze mode*1	深度软件待机模式
过渡条件	WFI指令同时 SBYCR.SSBY = 0	WFI指令同时 SBYCR.SSBY = 1 and DPSBYCR.DPSBY = 0	软件待机模式下的贪睡请求触发。SNZCR.SNZE=1	WFI指令同时 SBYCR.SSBY = 1 and DPSBYCR.DPSBY = 1
取消方法	所有中断。 该模式下可用的任何复位。	中断如表11.3所示。该模式下可用的任何复位。	中断如表11.3所示。该模式下可用的任何复位。	中断如表11.3所示。该模式下可用的任何复位。
中断取消后的状态	程序执行状态（中断处理）	程序执行状态（中断处理）	程序执行状态（中断处理）	重置状态
通过复位取消后的状态	重置状态	重置状态	重置状态	重置状态
主时钟振荡器	Selectable	Stop	Selectable*2	Stop
Sub-clock oscillator	Selectable	Selectable	Selectable	Selectable
High-speed on-chip oscillator	Selectable	Stop	Selectable	Stop
Middle-speed on-chip oscillator	Selectable	Stop	Selectable	Stop
Low-speed on-chip oscillator	Selectable	Selectable	Selectable	Selectable*3

Table 11.2 Operating conditions of each low power mode (2 of 3)

Parameter	Sleep mode	Software Standby mode	Snooze mode*1	Deep Software Standby mode
IWDT-dedicated on-chip oscillator	Selectable*7	Selectable*7	Selectable*7	Stop
PLL	Selectable	Stop	Selectable*2	Stop
Oscillation stop detection function	Selectable	Operation prohibited	Operation prohibited	Operation prohibited
Clock/buzzer output function	Selectable	Selectable*4	Selectable	Stop (Undefined)
External bus (EBCLK)	Selectable	Stop (Retained)	Operation prohibited	Stop (Retained)
CPU	Stop (Retained)	Stop (Retained)	Stop (Retained)	Stop (Undefined)
SRAMn (n = 0, 1), SRAMHS, ECC SRAM	Selectable	Stop (Retained)	Selectable	Stop (Undefined)
Standby SRAM	Selectable	Stop (Retained)	Selectable	Stop (Retained/Undefined)*5
Flash memory	Operating	Stop (Retained)	Stop (Retained)	Stop (Retained)
DMA Controller (DMAC)	Selectable	Stop (Retained)	Operation prohibited	Stop (Undefined)
Data Transfer Controller (DTC)	Selectable	Stop (Retained)	Selectable	Stop (Undefined)
USB 2.0 Full-Speed Module (USBFS)	Selectable	Stop (Retained). Detection of USB resumption is possible.	Operation prohibited. Detection of USB resumption is possible.	Stop (Retained/Undefined) Detection of USB resumption is possible.*6
USB 2.0 High-Speed Module (USBHS)	Selectable	Stop (Retained). Detection of USB resumption is possible.	Operation prohibited. Detection of USB resumption is possible.	Stop (Retained/Undefined) Detection of USB resumption is possible.*6
Watchdog Timer (WDT)	Selectable*7	Stop (Retained)	Stop (Retained)	Stop (Undefined)
Independent Watchdog Timer (IWDT)	Selectable*7	Selectable*7	Selectable *7	Stop (Undefined)
Realtime clock (RTC)	Selectable	Selectable	Selectable	Selectable*8
Asynchronous General Purpose Timer (AGTn, n = 0, 1)	Selectable	Selectable*9	Selectable*9	Selectable*9
12-Bit A/D Converter (ADC12)	Selectable	Stop (Retained)	Selectable*19	Stop (Undefined)
Programmable Gain Amplifiers (PGAs)	Selectable*13	Selectable*13	Selectable*13	Stop (Undefined)
12-Bit D/A Converter (DAC12)	Selectable	Stop (Retained)	Selectable	Stop (Undefined)
Capacitive Touch Sensing Unit (CTSU)	Selectable	Stop (Retained)	Selectable	Stop (Undefined)
Data Operation Circuit (DOC)	Selectable	Stop (Retained)	Selectable	Stop (Undefined)
Serial Communications Interface (SCI0)	Selectable	Stop (Retained)	Selectable (RXD0 falling edge is available, to enter Snooze mode) (only in asynchronous mode).*15	Stop (Undefined)
Serial Communications Interface (SCIn, n = 1 to 9)	Selectable	Stop (Retained)	Operation prohibited	Stop (Undefined)
I2C Bus Interface (IIC0)	Selectable	Selectable*14	Selectable*14	Stop (Undefined)
I2C Bus Interface (IICn, n = 1, 2)	Selectable	Stop (Retained)	Operation prohibited	Stop (Undefined)

Table 11.2 每种低功耗模式的操作条件（3个中的2个）

Parameter	睡眠模式	软件待机模式	Snooze mode*1	深度软件待机模式
IWDT-dedicated on-chip oscillator	Selectable*7	Selectable*7	Selectable*7	Stop
PLL	Selectable	Stop	Selectable*2	Stop
振荡停止检测功能	Selectable	禁止操作	禁止操作	禁止操作
时钟蜂鸣器输出功能	Selectable	Selectable*4	Selectable	Stop (Undefined)
外部总线(EBCLK)	Selectable	Stop (Retained)	禁止操作	Stop (Retained)
CPU	Stop (Retained)	Stop (Retained)	Stop (Retained)	Stop (Undefined)
SRAMn (n = 0, 1), SRAMHS, ECC SRAM	Selectable	Stop (Retained)	Selectable	Stop (Undefined)
Standby SRAM	Selectable	Stop (Retained)	Selectable	Stop (Retained/Undefined)*5
闪存	Operating	Stop (Retained)	Stop (Retained)	Stop (Retained)
DMA Controller (DMAC)	Selectable	Stop (Retained)	禁止操作	Stop (Undefined)
数据传输控制器(DTC)	Selectable	Stop (Retained)	Selectable	Stop (Undefined)
USB 2.0 Full-Speed Module (USBFS)	Selectable	停止（保留）。可以检测USB恢复。	禁止操作。可以检测USB恢复。	停止(RetainedUndefined)可以检测USB恢复。*6
USB 2.0 High-Speed Module (USBHS)	Selectable	停止（保留）。可以检测USB恢复。	禁止操作。可以检测USB恢复。	停止(RetainedUndefined)可以检测USB恢复。*6
看门狗定时器(WDT)	Selectable*7	Stop (Retained)	Stop (Retained)	Stop (Undefined)
独立看门狗 Timer (IWDT)	Selectable*7	Selectable*7	Selectable *7	Stop (Undefined)
实时时钟(RTC)	Selectable	Selectable	Selectable	Selectable*8
异步通用 用途定时器(AGTn n=0 1)	Selectable	Selectable*9	Selectable*9	Selectable*9
12-Bit A/D Converter (ADC12)	Selectable	Stop (Retained)	Selectable*19	Stop (Undefined)
可编程增益 Amplifiers (PGAs)	Selectable*13	Selectable*13	Selectable*13	Stop (Undefined)
12-Bit D/A Converter (DAC12)	Selectable	Stop (Retained)	Selectable	Stop (Undefined)
Capacitive Touch 传感单元(CTSU)	Selectable	Stop (Retained)	Selectable	Stop (Undefined)
数据运算电路(DOC)	Selectable	Stop (Retained)	Selectable	Stop (Undefined)
串行通信 Interface (SCI0)	Selectable	Stop (Retained)	可选（RXD0下降沿可用，进入贪睡模式）（仅在异步模式下）。*15	Stop (Undefined)
串行通信接口（SCIn，n =1至9）	Selectable	Stop (Retained)	禁止操作	Stop (Undefined)
I2C总线接口(IIC0)	Selectable	Selectable*14	Selectable*14	Stop (Undefined)
I2C总线接口(IICn n=1 2)	Selectable	Stop (Retained)	禁止操作	Stop (Undefined)

Table 11.2 Operating conditions of each low power mode (3 of 3)

Parameter	Sleep mode	Software Standby mode	Snooze mode*1	Deep Software Standby mode
Event Link Controller (ELC)	Selectable	Stop (Retained)	Selectable*10	Stop (Undefined)
High-Speed Analog Comparator (ACMPHS0)	Selectable	Selectable*12	Selectable. VCOUT function only.*12	Stop (Undefined)
High-Speed Analog Comparator (ACMPHSn, n = 1 to 5)	Selectable	Selectable*11	Selectable. VCOUT function only.*11	Stop (Undefined)
IRQn (n = 0 to 15) pin interrupt	Selectable	Selectable	Selectable	Stop (Undefined)
NMI, IRQn-DS (n = 0 to 14) pin interrupt	Selectable	Selectable	Selectable	Selectable
Key Interrupt Function (KINT)	Selectable	Selectable	Selectable	Stop (Undefined)
Low Voltage Detection (LVD)	Selectable	Selectable	Selectable	Selectable*16
Power-on reset circuit	Operating	Operating	Operating	Operating*17
Other peripheral modules	Selectable	Stop (Retained)	Operation prohibited	Stop (Undefined)
I/O ports	Operating	Retained*18	Operating	Retained*18

Note: Selectable means that operating or not operating can be selected by the control registers.
Stop (Retained) means that the contents of the internal registers are retained but the operations are suspended.
Operation prohibited means that the function must be stopped before entering Software Standby mode.
Stop (Undefined) means that the contents of the internal registers are undefined and power to the internal circuit is cut off.

Note 1. All modules whose module-stop bits are 0 start as soon as PCLKs are supplied after entering Snooze mode. To avoid an increase in ICC in Snooze mode, set the module-stop bit of modules that are not required in Snooze mode to 1 before entering Software Standby mode.
Note 2. When using SCI0 in Snooze mode, the MOSCCR.MOSTP and PLLCR.PLLSTP bits must be 1.
Note 3. If the DPSBYCR.DEEPCUT[1:0] bits are 00b, the oscillator status is the same as before entering Deep Software Standby mode. When the DPSBYCR.DEEPCUT[1:0] bits are not 00b, the oscillator stops when the MCU enters Deep Software Standby mode.
Note 4. Stopped when the clock output source select bits (CKOCR.CKOSEL[2:0]) are set to a value other than 010b (LOCO) and 100b (SOSC).
Note 5. If the DPSBYCR.DEEPCUT[1:0] bits are 00b, data in the Standby SRAM is retained in Deep Software Standby mode. When the DPSBYCR.DEEPCUT[1:0] bits are not 00b, data in the Standby SRAM is retained is undefined in Deep Software Standby mode.
Note 6. If the DPSBYCR.DEEPCUT[1:0] bits are 00b, the values of the USB resume detection circuit registers are retained and detection of USB resumption is enabled, and the values of other registers are undefined in Deep Software Standby mode. When the DPSBYCR.DEEPCUT[1:0] bits are not 00b, the values of all registers are undefined in Deep Software Standby mode.
Note 7. In IWDT-dedicated on-chip oscillator and IWDT, operating or stopping is selected by setting the IWDT Stop Control bit (IWDTSTPCTL) in Option Function Select register 0 (OFS0) in IWDT auto start mode. In WDT, operating or stopping is selected by setting the WDT Stop Control bit (WDTSTPCTL) in Option Function Select register 0 (OFS0) in WDT auto start mode.
Note 8. When the RCR4.RCKSEL bit set to 1 (LOCO), the DPSBYCR.DEEPCUT[1:0] bits must set to 00b before entering Deep Software Standby mode.
Note 9. AGT0 operation is possible when 100b (AGTLCLK) or 110b (AGTSCLK) is selected in the AGT0.AGTMR1.TCK[2:0] bits.
AGT1 operation is possible when 100b (AGTLCLK), 110b (AGTSCLK) or 101 (underflow event signal from AGT0) is selected in the AGT1.AGTMR1.TCK[2:0] bits.
When 100b (AGTLCLK) is selected in AGTn.AGTMR1.TCK[2:0] bits (n = 0, 1), the DPSBYCR.DEEPCUT[1:0] bits must set to 00b before entering Deep Software Standby mode.
Note 10. Event lists the restrictions described in section 11.10.13, ELC Events in Snooze Mode.
Note 11. Only VCOUT function is permitted. The VCOUT pin operates when ACMPHS uses no digital filter.
For details on digital filter, see section 50, High-Speed Analog Comparator (ACMPHS).
Note 12. When CMPCTL0.CSTEN bit is 1, canceling Software Standby Mode or entering Snooze mode by the comparator detection is available.
Note 13. When using the Programmable Gain Amplifiers, MSTPDn (n = 15, 16) must be set to 0. For details, see section 47.3.12, Programmable Gain Amplifiers.
Note 14. IIC0 wakeup interrupt is available.
Note 15. Serial communication mode of SCI0 is asynchronous mode.
Note 16. When using LVD in Deep Software Standby mode, DPSBYCR.DEEPCUT[1:0] bits must be 00b or 01b before entering Deep

Table 11.2 每种低功耗模式的操作条件（3个中的3个）

Parameter	睡眠模式	软件待机模式	Snooze mode*1	深度软件待机模式
事件链接控制器(ELC)	Selectable	Stop (Retained)	Selectable*10	Stop (Undefined)
High-Speed Analog Comparator (ACMPHS0)	Selectable	Selectable*12	Selectable. VCOUT function only.*12	Stop (Undefined)
High-Speed Analog 比较器（ACMPHSn，n=1至5）	Selectable	Selectable*11	Selectable. VCOUT function only.*11	Stop (Undefined)
IRQn(n=0to15)引脚中断	Selectable	Selectable	Selectable	Stop (Undefined)
NMI IRQn-DS(n=0to14)引脚中断	Selectable	Selectable	Selectable	Selectable
按键中断功能(KINT)	Selectable	Selectable	Selectable	Stop (Undefined)
低电压检测(LVD)	Selectable	Selectable	Selectable	Selectable*16
上电复位电路	Operating	Operating	Operating	Operating*17
其他外围模块	Selectable	Stop (Retained)	禁止操作	Stop (Undefined)
I/O ports	Operating	Retained*18	Operating	Retained*18

Note: 可选择的意思是可以通过控制寄存器来选择操作或不操作。
停止（Retained）表示内部寄存器的内容被保留但操作被暂停。
禁止操作意味着在进入软件待机模式之前必须停止该功能。
停止（未定义）表示内部寄存器的内容未定义，内部电路的电源被切断。

Note 1. 进入贪睡模式后，一旦提供PCLK，所有模块停止位为0的模块都会启动。为避免在贪睡模式下增加ICC，请在进入软件待机模式之前将贪睡模式下不需要的模块的模块停止位设置为1。
Note 2. 在贪睡模式下使用SCI0时，MOSCCR.MOSTP和PLLCR.PLLSTP位必须为1。
Note 3. 如果DPSBYCR.DEEPCUT[1:0]位为00b，则振荡器状态与进入深度软件待机模式之前相同。当DPSBYCR.DEEPCUT[1:0]位不为00b时，当MCU进入深度软件待机模式时振荡器停止。
Note 4. 当时钟输出源选择位(CKOCR.CKOSEL[2:0])设置为010b(LOCO)和100b(SOSC)以外的值时停止。
Note 5. 如果DPSBYCR.DEEPCUT[1:0]位为00b，则待机SRAM中的数据在深度软件待机模式下保留。当DPSBYCR.DEEPCUT[1:0]位不为00b时，待机SRAM中的数据保留在深度软件待机模式下未定义。
Note 6. 如果DPSBYCR.DEEPCUT[1:0]位为00b，则保留USB恢复检测电路寄存器的值并启用USB恢复检测，并且在深度软件待机模式下其他寄存器的值未定义。当DPSBYCR.DEEPCUT[1:0]位不为00b时，深度软件待机模式下所有寄存器的值未定义。
Note 7. 在IWDT专用内部振荡器和IWDT中，在IWDT自动启动模式下，通过设置选项功能选择寄存器0(OFS0)中的IWDT停止控制位(IWDTSTPCL)来选择操作或停止。在WDT中，在WDT自动启动模式下，通过设置选项功能选择寄存器0(OFS0)中的WDT停止控制位(WDTSTPCTL)来选择操作或停止。
Note 8. 当RCR4.RCKSEL位设置为1(LOCO)时，DPSBYCR.DEEPCUT[1:0]位必须设置为00b才能进入Deep软件待机模式。
Note 9. 当在AGT0.AGTMR1.TCK[2:0]位中选择100b(AGTLCLK)或110b(AGTSCLK)时，可以进行AGT0操作。
当在AGT1.AGTMR1.TCK[2:0]位中选择100b(AGTLCLK)、110b(AGTSCLK)或101（来自AGT0的下溢事件信号）时，可以进行AGT1操作。当在AGTn.AGTMR1.TCK[2:0]位(n=0 1)中选择100b(AGTLCLK)时，DPSBYCR.DEEPCUT[1:0]位必须在进入深度软件待机模式之前设置为00b。
注10.事件列出了第11.10.13节"贪睡模式下的ELC事件"中描述的限制。

注11.仅允许使用VCOUT功能。当ACMPHS不使用数字滤波器时，VCOUT引脚工作。
有关数字滤波器的详细信息，请参见第50节，高速模拟比较器(ACMPHS)。
注12.当CMPCTL0.CSTEN位为1时，可以通过比较器检测取消软件待机模式或进入贪睡模式。注13.使用可编程增益放大器时，MSTPDn(n=15 16)必须设置为0。有关详细信息，请参阅第47.3.12节，

可编程增益放大器。
注14.IIC0唤醒中断可用。
注15.SCI0的串行通信模式为异步模式。
注16.在深度软件待机模式下使用LVD时，DPSBYCR.DEEPCUT[1:0]位在进入深度之前必须为00b或01b

Software Standby mode.

Note 17. When the MCU enters Deep Software Standby mode with the DPSBYCR.DEEPCUT[1:0] bits set to 11b, the LVD circuit stops and the low-power function of the power-on reset circuit is enabled.

Note 18. For the address bus and bus control signals (For CSC: [CS0 to CS7, RD, WR0 to WR1, WR, BC0 to BC1, and ALE], and for SDRAMC: [SDCS, RAS, CAS and WE]), keeping the output state or changing to the high-impedance state can be selected in the SBYCR.OPE bit.

Note 19. When using the 12-Bit A/D Converter in Snooze mode, the ADCMPCR.CMPAE and ADCMPCR.CMPBE bits must be 1.

Table 11.3 Interrupt sources for canceling Snooze, Software Standby, and Deep Software Standby modes

Interrupt source	Name	Software Standby mode	Snooze mode	Deep Software Standby mode
NMI		Yes	Yes	Yes
Port	PORT_IRQn (n = 0 to 15)	Yes	Yes	No
	PORT_IRQn-DS (n = 0 to 14)	Yes	Yes	Yes
LVD	LVD_LVD1	Yes	Yes	Yes
	LVD_LVD2	Yes	Yes	Yes
IWDT	IWDT_NMIUNDF	Yes	Yes	No
USBFS	USBFS_USBR	Yes	Yes	Yes
USBHS	USBHS_USBIR	Yes	Yes	Yes
RTC	RTC_ALM	Yes	Yes	Yes
	RTC_PRD	Yes	Yes	Yes
KINT	KEY_INTKR	Yes	Yes	No
AGT1	AGT1_AGTI	Yes	Yes*3	Yes
	AGT1_AGTCMAI	Yes	Yes	No
	AGT1_AGTCMBI	Yes	Yes	No
ACMPHS	ACMP_HS0	Yes	Yes	No
IIC0	IIC0_WUI	Yes	Yes	No
ADC12n (n = 0, 1)	ADC12n_WCMPM	No	Yes with SELSR0*1,*3	No
	ADC12n_WCMPUM	No	Yes with SELSR0*1,*3	No
SCI0	SCI0_AM	No	Yes with SELSR0*1,*2	No
	SCI0_RXI_OR_ERI	No	Yes with SELSR0*1,*2	No
DTC	DTC_COMPLETE	No	Yes with SELSR0*1,*3	No
DOC	DOC_DOPCI	No	Yes with SELSR0*1	No
CTSU	CTSU_CTSUFN	No	Yes with SELSR0*1	No

Note 1. To use the interrupt request as a trigger for exiting Snooze mode, the request must be selected in SELSR0. See section 14, Interrupt Controller Unit (ICU). When a trigger selected in SELSR0 occurs after executing a WFI instruction and during the transition from Normal to Software Standby mode, the request might or might not be accepted, depending on the timing of the occurrence.

Note 2. Only one of either SCI0_AM or SCI0_RXI_OR_ERI can be set.

Note 3. The event that is enabled by the SNZEDCR register must not be used.

软件待机模式。

注17.当MCU进入深度软件待机模式且DPSBYCR.DEEPCUT[1:0]位设置为11b时，LVD电路停止并启用上电复位电路的低功耗功能。注18.对于地址总线和总线控制信号（对于CSC：[CS0到CS7、RD、WR0到WR1、WR、BC0到BC1和ALE]，以及

SDRAMC:[SDCS RAS CASandWE])，在SBYCR.OPE位可以选择保持输出状态或变为高阻状态。注19.在贪睡模式下使用12位AD转换器时，ADCMPCR.CMPAE和ADCMPCR.CMPBE位必须为1。

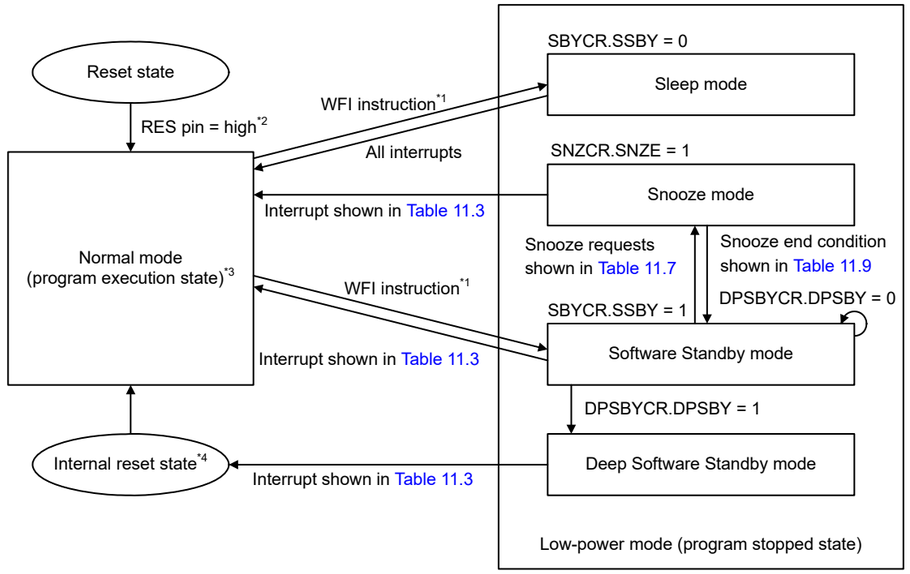
Table 11.3 用于取消贪睡、软件待机和深度软件待机模式的中断源

中断源	Name	软件待机模式	贪睡模式	深度软件待机模式
NMI		Yes	Yes	Yes
Port	PORT_IRQn (n = 0 to 15)	Yes	Yes	No
	PORT_IRQn-DS (n = 0 to 14)	Yes	Yes	Yes
LVD	LVD_LVD1	Yes	Yes	Yes
	LVD_LVD2	Yes	Yes	Yes
IWDT	IWDT_NMIUNDF	Yes	Yes	No
USBFS	USBFS_USBR	Yes	Yes	Yes
USBHS	USBHS_USBIR	Yes	Yes	Yes
RTC	RTC_ALM	Yes	Yes	Yes
	RTC_PRD	Yes	Yes	Yes
KINT	KEY_INTKR	Yes	Yes	No
AGT1	AGT1_AGTI	Yes	Yes*3	Yes
	AGT1_AGTCMAI	Yes	Yes	No
	AGT1_AGTCMBI	Yes	Yes	No
ACMPHS	ACMP_HS0	Yes	Yes	No
IIC0	IIC0_WUI	Yes	Yes	No
ADC12n (n = 0, 1)	ADC12n_WCMPM	No	是SELSR0*1 *3	No
	ADC12n_WCMPUM	No	是SELSR0*1 *3	No
SCI0	SCI0_AM	No	是SELSR0*1 *2	No
	SCI0_RXI_OR_ERI	No	是SELSR0*1 *2	No
DTC	DTC_COMPLETE	No	是SELSR0*1 *3	No
DOC	DOC_DOPCI	No	是SELSR0*1	No
CTSU	CTSU_CTSUFN	No	是SELSR0*1	No

Note 1. 要将中断请求用作退出贪睡模式的触发器，必须在SELSR0中选择该请求。见第14节，中断控制器单元（ICU）。当SELSR0中选择的触发发生在执行WFI指令之后以及从正常模式到软件待机模式的转换期间，请求可能会被接受，也可能不会被接受，这取决于发生的时间。

Note 2. 只能设置SCI0_AM或SCI0_RXI_OR_ERI之一。

Note 3. 不得使用由SNZEDCR寄存器启用的事件。



Note 1. When an interrupt that acts as a trigger for cancel is received during a transition to the program stopped state after the execution of a WFI instruction, the MCU executes interrupt exception handling instead of transitioning to low power mode.
Note 2. The MOCO clock is the source of the operating clock following a transition from the reset state to Normal mode.
Note 3. The transition to Normal mode is made because of an interrupt from Sleep, Snooze, or Software Standby mode. The clock source is the same as before entering the low power mode.
Note 4. When an available interrupt request is generated, an internal reset (Deep Software Standby reset) is generated over a fixed period. Canceling of Deep Software Standby mode accompanies release from the internal reset state, and then the MCU transitions to Normal mode and execute a reset exception processing with the MOCO clock as the source of the operating clock.

Figure 11.1 Mode transitions

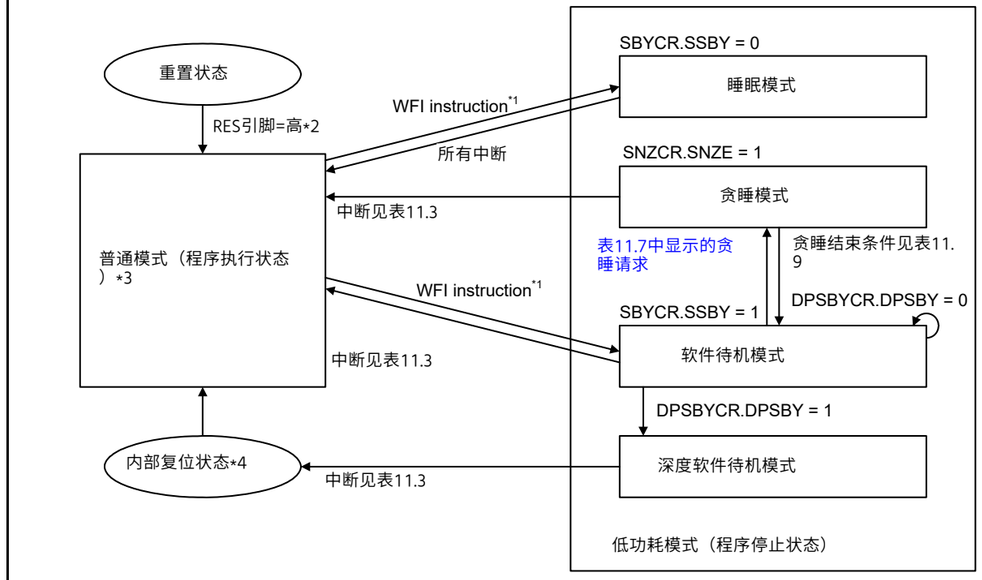
11.2 Register Descriptions

11.2.1 Standby Control Register (SBYCR)

Address(es): SYSTEM.SBYCR 4001 E00Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SSBY	OPE	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b13 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b14	OPE	Output Port Enable	0: In Software Standby or Deep Software Standby mode, set the address bus and bus control signals to the high-impedance state. In Snooze mode, the status of the address bus and bus control signals are the same as before entering Software Standby mode. 1: In Software Standby or Deep Software Standby mode, retain the output state of the address bus and bus control signals.	R/W
b15	SSBY	Software Standby	0: Sleep mode 1: Software Standby mode when DPSBYCR.DPSBY = 0 and Deep Software Standby mode when DPSBYCR.DPSBY = 1.	R/W



Note 1. 当在执行WFI指令后转换到程序停止状态期间接收到用作取消触发器的中断时，MCU将执行中断异常处理，而不是转换到低功耗模式。
Note 2. MOCO时钟是从复位状态转换到正常模式后的工作时钟源。
Note 3. 由于休眠、贪睡或软件待机模式的中断，会转换到正常模式。时钟源与进入低功耗模式前相同。
Note 4. 当产生可用中断请求时，会在固定周期内产生内部复位（深度软件待机复位）。
深度软件待机模式的取消伴随着内部复位状态的释放，然后MCU转换到正常模式并以MOCO时钟作为工作时钟源执行复位异常处理。

Figure 11.1 模式转换

11.2 注册说明

11.2.1 待机控制寄存器(SBYCR)

Address(es): SYSTEM.SBYCR 4001 E00Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SSBY	OPE	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b13 to b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b14	OPE	输出端口使能	0：在软件待机或深度软件待机模式下，设置地址总线和总线控制信号为高阻状态。在贪睡模式下，地址总线和总线控制信号的状态与进入软件待机模式前相同。1：在软件待机或深度软件待机模式下，保持地址总线和总线控制信号的输出状态。	R/W
b15	SSBY	软件待机	0：休眠模式1：当DPSBYCR.DPSBY=0时为软件待机模式，当DPSBYCR.DPSBY=1时为深度软件待机模式。	R/W

OPE bit (Output Port Enable)

The OPE bit specifies whether to set to the high-impedance state or to retain the output of the address bus and bus control signals (for CSC: [CS0 to CS7, RD, WR0 to WR1, WR, BC0 to BC1, and ALE], and for SDRAMC: [SDCS, RAS, CAS, and WE]) in Software Standby mode or Deep Software Standby mode.

SSBY bit (Software Standby)

The SSBY bit specifies the target transition after a WFI instruction is executed. When the SSBY bit is set to 1, the MCU enters Software Standby mode after executing the WFI instruction. When the MCU cancels Software Standby mode by an interrupt, the SSBY bit remains set to 1. The SSBY bit can be cleared by writing 0 to it.

When the OSTDCR.OSTDE bit is 1, the SSBY bit is ignored. Even if the SSBY bit is 1, the MCU enters Sleep mode on execution of a WFI instruction.

When the FENTRYR.FENTRYi bit (i = 0 to 3) is 1 or the FENTRYR.FENTRYD bit is 1, the SSBY is ignored. Even if the SSBY bit is 1, the MCU enters Sleep mode on execution of a WFI instruction. See Table 11.6 for details.

When using the HOCO clock to enter Software Standby mode, STCONR.STCON[1:0] must be set to 00b and HOCOWTCR.HSTS[2:0] must be set to 110b. However, when using SCI0 in Snooze mode, HOCOWTCR.HSTS[2:0] must be set to 010b.

11.2.2 Module Stop Control Register A (MSTPCRA)

Address(es): SYSTEM.MSTPCRA 4001 E01Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	MSTPA22	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	MSTPA7	MSTPA6	MSTPA5	—	—	—	MSTPA1	MSTPA0
Value after reset:	1	1	1	1	1	1	1	1	0	0	0	1	1	1	0	0

Bit	Symbol	Bit name	Description	R/W
b0	MSTPA0	SRAM0 Module Stop*1	Target module: SRAM0 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b1	MSTPA1	SRAM1 Module Stop	Target module: SRAM1 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b4 to b2	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b5	MSTPA5	High-Speed SRAM Module Stop	Target module: high-speed SRAM 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b6	MSTPA6	ECC SRAM Module Stop*1	Target module: ECC SRAM 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b7	MSTPA7	Standby SRAM Module Stop	Target module: Standby SRAM 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b21 to b8	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b22	MSTPA22	DMA Controller/Data Transfer Controller Module Stop*2	Target modules: DMAC, DTC 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b31 to b23	—	Reserved	These bits are read as 1. The write value should be 1.	R/W

Note 1. The MSTPA0 and MSTPA6 bit settings must be the same.
Note 2. When rewriting the MSTPA22 bit from 0 to 1, disable the DMAC and DTC before setting the MSTPA22 bit.

OPE位（输出端口使能）

OPE位指定是设置为高阻状态还是保留地址总线和总线控制信号的输出（对于CSC：[CS0到CS7、RD、WR0到WR1、WR、BC0到BC1和ALE]，对于SDRAMC：[SDCS、RAS、CAS和WE]）处于软件待机模式或深度软件待机模式。

SSBY位（软件待机）

SSBY位指定执行WFI指令后的目标转换。当SSBY位设置为1时，MCU在执行WFI指令后进入软件待机模式。当MCU通过中断取消软件待机模式时，SSBY位保持设置为1。SSBY位可以通过向其写入0来清除。

当OSTDCR.OSTDE位为1时，SSBY位被忽略。即使SSBY位为1，MCU也会在执行WFI指令时进入休眠模式。

当FENTRYR.FENTRYi位（i=0到3）为1或FENTRYR.FENTRYD位为1时，忽略SSBY。即使SSBY位为1，MCU也会在执行WFI指令时进入休眠模式。详见表11.6。

当使用HOCO时钟进入软件待机模式时，STCONR.STCON[1:0]必须设置为00b并且HOCOWTCR.HSTS[2:0]必须设置为110b。但是，在贪睡模式下使用SCI0时，HOCOWTCR.HSTS[2:0]必须设置为010b。

11.2.2 模块停止控制寄存器A(MSTPCRA)

Address(es): SYSTEM.MSTPCRA 4001 E01Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	MSTPA22	—	—	—	—	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	MSTPA7	MSTPA6	MSTPA5	—	—	—	MSTPA1	MSTPA0
重置后的值:	1	1	1	1	1	1	1	1	0	0	0	1	1	1	0	0

Bit	Symbol	位名称	Description	R/W
b0	MSTPA0	SRAM0 Module Stop*1	目标模块：SRAM00：取消模块停止状态1：进入模块停止状态。	R/W
b1	MSTPA1	SRAM1模块停止	目标模块：SRAM10：取消模块停止状态1：进入模块停止状态。	R/W
b4 to b2	—	Reserved	这些位被读取为1。写入值应为1。	R/W
b5	MSTPA5	High-Speed SRAM Module Stop	目标模块：高速SRAM0：取消模块停止状态1：进入模块停止状态。	R/W
b6	MSTPA6	ECC SRAM Module Stop*1	目标模块：ECCSRAM0：取消模块停止状态1：进入模块停止状态。	R/W
b7	MSTPA7	备用SRAM模块 Stop	目标模块：StandbySRAM0：取消模块停止状态1：进入模块停止状态。	R/W
b21 to b8	—	Reserved	这些位被读取为1。写入值应为1。	R/W
b22	MSTPA22	DMA Controller/Data 传输控制器模块 Stop*2	目标模块：DMAC，DTC0：取消模块停止状态1：进入模块停止状态。	R/W
b31 to b23	—	Reserved	这些位被读取为1。写入值应为1。	R/W

Note 1. MSTPA0和MSTPA6位设置必须相同。
Note 2. 将MSTPA22位从0重写为1时，在设置MSTPA22位之前禁用DMAC和DTC。

11.2.3 Module Stop Control Register B (MSTPCRB)

Address(es): MSTP.MSTPCRB 4004 7000h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	MSTPB31	MSTPB30	MSTPB29	MSTPB28	MSTPB27	MSTPB26	MSTPB25	MSTPB24	MSTPB23	MSTPB22	—	—	MSTPB19	MSTPB18	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MSTPB15	—	MSTPB13	MSTPB12	MSTPB11	—	MSTPB9	MSTPB8	MSTPB7	MSTPB6	MSTPB5	—	—	MSTPB2	MSTPB1	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Bit name	Description	R/W
b0	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b1	MSTPB1	Controller Area Network 1 Module Stop*1	Target module: CAN1 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b2	MSTPB2	Controller Area Network 0 Module Stop*1	Target module: CAN0 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b4, b3	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b5	MSTPB5	IrDA Module Stop	Target module: IrDA 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b6	MSTPB6	Quad Serial Peripheral Interface Module Stop	Target module: QSPI 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b7	MSTPB7	I²C Bus Interface 2 Module Stop	Target module: IIC2 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b8	MSTPB8	I²C Bus Interface 1 Module Stop	Target module: IIC1 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b9	MSTPB9	I²C Bus Interface 0 Module Stop	Target module: IIC0 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b10	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b11	MSTPB11	Universal Serial Bus 2.0 FS Interface Module Stop*2	Target module: USBFS 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b12	MSTPB12	Universal Serial Bus 2.0 HS Interface Module Stop	Target module: USBHS 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b13	MSTPB13	EPTPC and PTPEDMAC Module Stop*3	Target modules: EPTPC and PTPEDMAC 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b14	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b15	MSTPB15	ETHERC0 and EDMAC0 Controller Module Stop	Target modules: ETHERC0, EDMAC0 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b17, b16	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b18	MSTPB18	Serial Peripheral Interface 1 Module Stop	Target module: SPI1 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W

11.2.3 模块停止控制寄存器B(MSTPCRB)

Address(es): MSTP.MSTPCRB 4004 7000h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	MSTPB31	MSTPB30	MSTPB29	MSTPB28	MSTPB27	MSTPB26	MSTPB25	MSTPB24	MSTPB23	MSTPB22	—	—	MSTPB19	MSTPB18	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MSTPB15	—	MSTPB13	MSTPB12	MSTPB11	—	MSTPB9	MSTPB8	MSTPB7	MSTPB6	MSTPB5	—	—	MSTPB2	MSTPB1	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	位名称	Description	R/W
b0	—	Reserved	该位读取为1。写入值应为1。	R/W
b1	MSTPB1	控制器局域网1模块 Stop*1	目标模块：CAN10：取消模块停止状态1：进入模块停止状态。	R/W
b2	MSTPB2	控制器局域网0模块 Stop*1	目标模块：CAN00：取消模块停止状态1：进入模块停止状态。	R/W
b4, b3	—	Reserved	这些位被读取为1。写入值应为1。	R/W
b5	MSTPB5	IrDA模块停止	目标模块：IrDA0：取消模块停止状态1：进入模块停止状态。	R/W
b6	MSTPB6	四路串行外设接口 模块停止	目标模块：QSPI0：取消模块停止状态1：进入模块停止状态。	R/W
b7	MSTPB7	I2C总线接口2模块停止	目标模块：IIC20：取消模块停止状态1：进入模块停止状态。	R/W
b8	MSTPB8	I2C总线接口1模块停止	目标模块：IIC10：取消模块停止状态1：进入模块停止状态。	R/W
b9	MSTPB9	I2C总线接口0模块停止	目标模块：IIC00：取消模块停止状态1：进入模块停止状态。	R/W
b10	—	Reserved	该位读取为1。写入值应为1。	R/W
b11	MSTPB11	通用串行总线2.0FS 接口模块停止*2	目标模块：USBFS0：取消模块停止状态1：进入模块停止状态。	R/W
b12	MSTPB12	通用串行总线2.0HS 接口模块停止	目标模块：USBHS0：取消模块停止状态1：进入模块停止状态。	R/W
b13	MSTPB13	EPTPC和PTPEDMAC模块 Stop*3	目标模块：EPTPC和PTPEDMAC0：取消模块停止状态1：进入模块停止状态。	R/W
b14	—	Reserved	该位读取为1。写入值应为1。	R/W
b15	MSTPB15	ETHERC0和EDMAC0控制器 模块停止	目标模块：ETHERC0、EDMAC00：取消模块停止状态1：进入模块停止状态。	R/W
b17, b16	—	Reserved	这些位被读取为1。写入值应为1。	R/W
b18	MSTPB18	串行外设接口1模块 Stop	目标模块：SPI10：取消模块停止状态1：进入模块停止状态。	R/W

Bit	Symbol	Bit name	Description	R/W
b19	MSTPB19	Serial Peripheral Interface 0 Module Stop	Target module: SPI0 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b21, b20	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b22	MSTPB22	Serial Communication Interface 9 Module Stop	Target module: SCI9 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b23	MSTPB23	Serial Communication Interface 8 Module Stop	Target module: SCI8 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b24	MSTPB24	Serial Communication Interface 7 Module Stop	Target module: SCI7 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b25	MSTPB25	Serial Communication Interface 6 Module Stop	Target module: SCI6 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b26	MSTPB26	Serial Communication Interface 5 Module Stop	Target module: SCI5 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b27	MSTPB27	Serial Communication Interface 4 Module Stop	Target module: SCI4 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b28	MSTPB28	Serial Communication Interface 3 Module Stop	Target module: SCI3 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b29	MSTPB29	Serial Communication Interface 2 Module Stop	Target module: SCI2 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b30	MSTPB30	Serial Communication Interface 1 Module Stop	Target module: SCI1 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b31	MSTPB31	Serial Communication Interface 0 Module Stop	Target module: SCI0 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W

Note 1. The MSTPBi bit must be written to while the oscillation of the clock controlled by this bit is stable. To enter Software Standby mode after writing to this bit, wait for two CAN clock (CANMCLK) cycles after writing, then execute a WFI instruction (i = 1, 2).

Note 2. To enter Software Standby mode after writing to the MSTPB11 bit, wait for two USB clock (UCLK) cycles after writing, then execute a WFI instruction.

Note 3. Even when EPTPC and PTPEDMAC operation is enabled (MSTPB13 = 0), some registers in the EPTPC module become inaccessible depending on the combination of the MSTPB15 bit and EPTPC bypass bit (EPTPC_CFG.BYPASS.BYPASS0) settings. For details, see section 30, Ethernet PTP Controller (EPTPC).

Bit	Symbol	位名称	Description	R/W
b19	MSTPB19	串行外设接口0模块 Stop	目标模块：SPI00：取消模块停止状态1：进入模块停止状态。	R/W
b21, b20	—	Reserved	这些位被读取为1。写入值应为1。	R/W
b22	MSTPB22	串行通讯接口9模块停止	目标模块：SCI90：取消模块停止状态1：进入模块停止状态。	R/W
b23	MSTPB23	串行通讯接口8模块停止	目标模块：SCI80：取消模块停止状态1：进入模块停止状态。	R/W
b24	MSTPB24	串行通讯接口7模块停止	目标模块：SCI70：取消模块停止状态1：进入模块停止状态。	R/W
b25	MSTPB25	串行通讯接口6模块停止	目标模块：SCI60：取消模块停止状态1：进入模块停止状态。	R/W
b26	MSTPB26	串行通讯接口5模块停止	目标模块：SCI50：取消模块停止状态1：进入模块停止状态。	R/W
b27	MSTPB27	串行通讯接口4模块停止	目标模块：SCI40：取消模块停止状态1：进入模块停止状态。	R/W
b28	MSTPB28	串行通讯接口3模块停止	目标模块：SCI30：取消模块停止状态1：进入模块停止状态。	R/W
b29	MSTPB29	串行通讯接口2模块停止	目标模块：SCI20：取消模块停止状态1：进入模块停止状态。	R/W
b30	MSTPB30	串行通讯接口1模块停止	目标模块：SCI10：取消模块停止状态1：进入模块停止状态。	R/W
b31	MSTPB31	串行通讯接口0模块停止	目标模块：SCI00：取消模块停止状态1：进入模块停止状态。	R/W

Note 1. MSTPBi位必须在该位控制的时钟振荡稳定时写入。要在写入该位后进入软件待机模式，写入后等待两个CAN时钟(CANMCLK)周期，然后执行WFI指令(i=1 2)。

Note 2. 要在写入MSTPB11位后进入软件待机模式，写入后等待两个USB时钟(UCLK)周期，然后执行WFI指令。

Note 3. 即使启用了EPTPC和PTPEDMAC操作(MSTPB13=0)，根据MSTPB15位和EPTPC旁路位(EPTPC_CFG.BYPASS.BYPASS0)设置的组合，EPTPC模块中的一些寄存器也变得不可访问。有关详细信息，请参阅第30节，以太网PTP控制器(EPTPC)。

11.2.4 Module Stop Control Register C (MSTPCRC)

Address(es): MSTP.MSTPCRC 4004 7004h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	MSTPC31	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	MSTPC14	MSTPC13	MSTPC12	MSTPC11	—	MSTPC9	MSTPC8	MSTPC7	MSTPC6	MSTPC5	MSTPC4	MSTPC3	MSTPC2	MSTPC1	MSTPC0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Bit name	Description	R/W
b0	MSTPC0*1	Clock Frequency Accuracy Measurement Circuit Module Stop	Target module: CAC 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b1	MSTPC1	Cyclic Redundancy Check Calculator Module Stop	Target module: CRC 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b2	MSTPC2	Parallel Data Capture Module Stop	Target module: PDC 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b3	MSTPC3	Capacitive Touch Sensing Unit Module Stop	Target module: CTSU 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b4	MSTPC4	Graphics LCD Controller Module Stop	Target module: GLCDC 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b5	MSTPC5	JPEG Codec Engine Module Stop	Target module: JPEG 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b6	MSTPC6	2D Drawing Engine Module Stop	Target module: DRW 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b7	MSTPC7	Serial Sound Interface Enhanced (channel 1) Module Stop	Target module: SSIE1 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b8	MSTPC8	Serial Sound Interface Enhanced (channel 0) Module Stop	Target module: SSIE0 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b9	MSTPC9	Sampling Rate Converter Module Stop	Target module: SRC 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b10	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b11	MSTPC11	Secure Digital Host IF/ MultiMediaCard 1 Module Stop	Target module: SDHI/MMC1 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b12	MSTPC12	Secure Digital Host IF/ MultiMediaCard 0 Module Stop	Target module: SDHI/MMC0 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b13	MSTPC13	Data Operation Circuit Module Stop	Target module: DOC 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b14	MSTPC14	Event Link Controller Module Stop	Target module: ELC 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W

11.2.4 模块停止控制寄存器C(MSTPCRC)

Address(es): MSTP.MSTPCRC 4004 7004h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	MSTPC31	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	MSTPC14	MSTPC13	MSTPC12	MSTPC11	—	MSTPC9	MSTPC8	MSTPC7	MSTPC6	MSTPC5	MSTPC4	MSTPC3	MSTPC2	MSTPC1	MSTPC0
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	位名称	Description	R/W
b0	MSTPC0*1	时钟频率精度测量电路模块停止	目标模块：CAC0：取消模块停止状态1：进入模块停止状态。	R/W
b1	MSTPC1	循环冗余检查计算器模块Stop	目标模块：CRC0：取消模块停止状态1：进入模块停止状态。	R/W
b2	MSTPC2	并行数据采集模块停止	目标模块：PDC0：取消模块停止状态1：进入模块停止状态。	R/W
b3	MSTPC3	Capacitive Touch传感单元模块停止	目标模块：CTSU0：取消模块停止状态1：进入模块停止状态。	R/W
b4	MSTPC4	图形液晶控制器模块停止	目标模块：GLCDC0：取消模块停止状态1：进入模块停止状态。	R/W
b5	MSTPC5	JPEG编解码引擎模块停止	目标模块：JPEG0：取消模块停止状态1：进入模块停止状态。	R/W
b6	MSTPC6	2D绘图引擎模块停止	目标模块：DRW0：取消模块停止状态1：进入模块停止状态。	R/W
b7	MSTPC7	串行声音接口增强（通道1）模块停止	目标模块：SSIE10：取消模块停止状态1：进入模块停止状态。	R/W
b8	MSTPC8	串行声音接口增强（通道0）模块停止	目标模块：SSIE00：取消模块停止状态1：进入模块停止状态。	R/W
b9	MSTPC9	采样率转换器模块停止	目标模块：SRC0：取消模块停止状态1：进入模块停止状态。	R/W
b10	—	Reserved	该位读取为1。写入值应为1。	R/W
b11	MSTPC11	安全数字主机IF MultiMediaCard 1 Module Stop	目标模块：SDHIMMC10：取消模块停止状态1：进入模块停止状态。	R/W
b12	MSTPC12	安全数字主机IF MultiMediaCard 0 Module Stop	目标模块：SDHIMMC00：取消模块停止状态1：进入模块停止状态。	R/W
b13	MSTPC13	数据运算电路模块停止	目标模块：DOC0：取消模块停止状态1：进入模块停止状态。	R/W
b14	MSTPC14	事件链接控制器模块停止	目标模块：ELC0：取消模块停止状态1：进入模块停止状态。	R/W

Bit	Symbol	Bit name	Description	R/W
b30 to b15	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b31	MSTPC31	SCE7 Module Stop	Target module: SCE7 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W

Note 1. The MSTPC0 bit must be written to while the oscillation of the clock controlled by this bit is stable. To enter Software Standby mode after writing to this bit, wait for two cycles of the slowest clock among the clocks output by the oscillators, then execute a WFI instruction.

11.2.5 Module Stop Control Register D (MSTPCRD)

Address(es): MSTP.MSTPCRD 4004 7008h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	MSTPD28	MSTPD27	MSTPD26	MSTPD25	MSTPD24	MSTPD23	MSTPD22	—	MSTPD20	—	—	—	MSTPD16
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MSTPD15	MSTPD14	—	—	—	—	—	—	—	MSTPD6	MSTPD5	—	MSTPD3	MSTPD2	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	Bit name	Description	R/W
b1, b0	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b2	MSTPD2	Asynchronous General Purpose Timer 1 Module Stop*1	Target module: AGT1 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b3	MSTPD3	Asynchronous General Purpose Timer 0 Module Stop*2	Target module: AGT0 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b4	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b5	MSTPD5	General PWM Timer 32EH0 to 32EH3 and 32E4 to 32E7 and PWM Delay Generation Circuit Module Stop	Target modules: GPT32EHx (x = 0 to 3), GPT32Ey (y = 4 to 7), and PWM Delay Generation Circuit 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b6	MSTPD6	General PWM Timer 328 to 3213 Module Stop	Target modules: GPT32x (x = 8 to 13) 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b13 to b7	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b14	MSTPD14	Port Output Enable for GPT Module Stop	Target module: POEG 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b15	MSTPD15	12-Bit A/D Converter 1 Module Stop	Target module: ADC121 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b16	MSTPD16	12-Bit A/D Converter 0 Module Stop	Target module: ADC120 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b19 to b17	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b20	MSTPD20	12-Bit D/A Converter Module Stop	Target module: DAC12 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b21	—	Reserved	This bit is read as 1. The write value should be 1.	R/W

Bit	Symbol	位名称	Description	R/W
b30 to b15	—	Reserved	这些位被读取为1。写入值应为1。	R/W
b31	MSTPC31	SCE7模块停止	目标模块：SCE70：取消模块停止状态1：进入模块停止状态。	R/W

Note 1. 必须在该位控制的时钟振荡稳定时写入MSTPC0位。要在写入该位后进入软件待机模式，请等待振荡器输出时钟中最慢时钟的两个周期，然后执行WFI指令。

11.2.5 模块停止控制寄存器D(MSTPCRD)

Address(es): MSTP.MSTPCRD 4004 7008h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	MSTPD28	MSTPD27	MSTPD26	MSTPD25	MSTPD24	MSTPD23	MSTPD22	—	MSTPD20	—	—	—	MSTPD16
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MSTPD15	MSTPD14	—	—	—	—	—	—	—	MSTPD6	MSTPD5	—	MSTPD3	MSTPD2	—	—
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Symbol	位名称	Description	R/W
b1, b0	—	Reserved	这些位被读取为1。写入值应为1。	R/W
b2	MSTPD2	异步通用 用途定时器1模块 Stop*1	目标模块：AGT10：取消模块停止状态1：进入模块停止状态。	R/W
b3	MSTPD3	异步通用 用途定时器0模块 Stop*2	目标模块：AGT00：取消模块停止状态1：进入模块停止状态。	R/W
b4	—	Reserved	该位读取为1。写入值应为1。	R/W
b5	MSTPD5	通用PWM定时器32EH0至32EH3和32E4至32E7和PWM延迟发生电路 模块停止	目标模块：GPT32EHx(x=0to3) GPT32Ey(y=4to7) PWM延迟产生电路0：取消模块停止状态1：进入模块停止状态。	R/W
b6	MSTPD6	通用PWM定时器328至3213模块停止	目标模块：GPT32x(x=8to13)0：取消模块停止状态1：进入模块停止状态。	R/W
b13 to b7	—	Reserved	这些位被读取为1。写入值应为1。	R/W
b14	MSTPD14	GPT的端口输出使能 模块停止	目标模块：POEG0：取消模块停止状态1：进入模块停止状态。	R/W
b15	MSTPD15	12位AD转换器1模块停止	目标模块：ADC1210：取消模块停止状态1：进入模块停止状态。	R/W
b16	MSTPD16	12位AD转换器0模块停止	目标模块：ADC1200：取消模块停止状态1：进入模块停止状态。	R/W
b19 to b17	—	Reserved	这些位被读取为1。写入值应为1。	R/W
b20	MSTPD20	12位DA转换器模块停止	目标模块：DAC120：取消模块停止状态1：进入模块停止状态。	R/W
b21	—	Reserved	该位读取为1。写入值应为1。	R/W

Bit	Symbol	Bit name	Description	R/W
b22	MSTPD22	Temperature Sensor Module Stop	Target module: TSN 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b23	MSTPD23	High-Speed Analog Comparator 5 Module Stop	Target module: ACMPHS5 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b24	MSTPD24	High-Speed Analog Comparator 4 Module Stop	Target module: ACMPHS4 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b25	MSTPD25	High-Speed Analog Comparator 3 Module Stop	Target module: ACMPHS3 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b26	MSTPD26	High-Speed Analog Comparator 2 Module Stop	Target module: ACMPHS2 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b27	MSTPD27	High-Speed Analog Comparator 1 Module Stop	Target module: ACMPHS1 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b28	MSTPD28	High-Speed Analog Comparator 0 Module Stop	Target module: ACMPHS0 0: Cancel the module-stop state 1: Enter the module-stop state.	R/W
b31 to b29	—	Reserved	These bits are read as 1. The write value should be 1.	R/W

Note 1. When the count source is sub-clock oscillator or LOCO, AGT1 counting does not stop even if MSTPD2 is set to 1. If the count source is the sub-clock oscillator or LOCO, this bit must be set to 1 except when accessing the AGT1 registers.

Note 2. When the count source is sub-clock oscillator or LOCO, AGT0 counting does not stop even if MSTPD3 is set to 1. If the count source is the sub-clock oscillator or LOCO, this bit must be set to 1 except when accessing the AGT0 registers.

11.2.6 Operating Power Control Register (OPCCR)

Address(es): SYSTEM.OPCCR 4001 E0A0h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	OPCMTSF	—	—	OPCM[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	OPCM[1:0]	Operating Power Control Mode Select	b1 b0 0 0: High-speed mode 1 1: Low-speed mode. Other settings are prohibited.	R/W
b3, b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	OPCMTSF	Operating Power Control Mode Transition Status Flag	• Read 0: Transition complete 1: Transition in progress. • Write The write value should be 0.	R
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The OPCCR register is used to reduce power consumption in Normal and Sleep modes by specifying a lower operating frequency and operating voltage. For the procedure for changing the operating power control modes, see section 11.5, Function for Lower Operating Power Consumption.

When transitioning from Software Standby mode to Normal or Snooze mode, the settings in the OPCCR.OPCM[1:0] and SOPCCR.SOPCM bits are as follows, regardless of their settings before entering Software Standby mode:

- OPCCR.OPCM[1:0] = 00b (High-speed mode)

Bit	Symbol	位名称	Description	R/W
b22	MSTPD22	温度传感器模块 Stop	目标模块：TSN0：取消模块停止状态1：进入模块停止状态。	R/W
b23	MSTPD23	High-Speed Analog 比较器5模块停止	目标模块：ACMPHS50：取消模块停止状态1：进入模块停止状态。	R/W
b24	MSTPD24	High-Speed Analog 比较器4模块停止	目标模块：ACMPHS40：取消模块停止状态1：进入模块停止状态。	R/W
b25	MSTPD25	High-Speed Analog 比较器3模块停止	目标模块：ACMPHS30：取消模块停止状态1：进入模块停止状态。	R/W
b26	MSTPD26	High-Speed Analog 比较器2模块停止	目标模块：ACMPHS20：取消模块停止状态1：进入模块停止状态。	R/W
b27	MSTPD27	High-Speed Analog 比较器1模块停止	目标模块：ACMPHS10：取消模块停止状态1：进入模块停止状态。	R/W
b28	MSTPD28	High-Speed Analog 比较器0模块停止	目标模块：ACMPHS00：取消模块停止状态1：进入模块停止状态。	R/W
b31 to b29	—	Reserved	这些位被读取为1。写入值应为1。	R/W

Note 1. 当计数源为副时钟振荡器或LOCO时，即使MSTPD2设置为1，AGT1计数也不会停止。如果计数源为副时钟振荡器或LOCO，则该位必须设置为1，除非访问AGT1寄存器。

Note 2. 当计数源为副时钟振荡器或LOCO时，即使MSTPD3设置为1，AGT0计数也不会停止。如果计数源为副时钟振荡器或LOCO，该位必须设置为1，除非访问AGT0寄存器。

11.2.6 工作电源控制寄存器(OPCCR)

Address(es): SYSTEM.OPCCR 4001 E0A0h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	OPCMTSF	—	—	OPCM[1:0]	
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b1, b0	OPCM[1:0]	工作功率控制模式选择	b1b000：高速模式11：低速模式。禁止其他设置。	R/W
b3, b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b4	OPCMTSF	工作功率控制模式转换状态 Flag	读取0：转换完成1：转换正在进行中。 写入写入值应为0。	R
b7 to b5	—	Reserved	这些位被读取为0。写入值应为0。	R/W

OPCCR寄存器用于通过指定较低的工作频率和工作电压来降低正常和休眠模式下的功耗。有关更改运行功耗控制模式的步骤，请参阅第11.5节"降低运行功耗的功能"。

当从软件待机模式转换到正常或贪睡模式时，OPCCR.OPCM[1:0]中的设置和SOPCCR.SOPCM位如下，无论它们在进入软件待机模式之前的设置如何：

- OPCCR.OPCM[1:0] = 00b (High-speed mode)

- SOPCCR.SOPCM = 0b (not Subosc-speed mode).

If Software Standby mode is canceled before the transition to Software Standby completes, the OPCCR.OPCM[1:0] and SOPCCR.SOPCM bits retain their settings from before the WFI instruction executed. If this causes any problem, set the MCU to High-speed mode during the exception handling procedure when canceling Software Standby mode.

OPCM[1:0] bits (Operating Power Control Mode Select)

The OPCM[1:0] bits select the operating power control mode in Normal and Sleep modes. Table 11.4 shows the relationship between the operating power control modes and the OPCM[1:0] and SOPCM settings.

OPCMTSF flag (Operating Power Control Mode Transition Status Flag)

The OPCMTSF flag indicates the switching control state when the operating power control mode is switched. The flag is set to 1 on a write access to the OPCM[1:0] bits, and to 0 when the mode transition completes. Confirm that the flag is 0 before proceeding.

11.2.7 Sub Operating Power Control Register (SOPCCR)

Address(es): SYSTEM.SOPCCR 4001 E0AAh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	SOPCMTSF	—	—	—	SOPCM
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	SOPCM	Sub Operating Power Control Mode Select	0: Not Subosc-speed mode 1: Subosc-speed mode.	R/W
b3 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	SOPCMTSF	Sub Operating Power Control Mode Transition Status Flag	0: Transition complete 1: Transition in progress.	R
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The SOPCCR register is used to reduce power consumption in Normal and Sleep modes by initiating entry to and exit from Subosc-speed mode. Subosc-speed mode is only available when using the sub-clock oscillator or LOCO without dividing the frequency.

The flash cache function should be set to disabled by setting FCACHEE.FCACHEEN to 0 before switching the operating power control mode. For details, see section 55, Flash Memory.

For the procedure for changing operating power control modes, see section 11.5, Function for Lower Operating Power Consumption.

SOPCM bit (Sub Operating Power Control Mode Select)

The SOPCM bit selects the operating power control mode in Normal and Sleep modes. Setting this bit to 1 allows transition to Subosc-speed mode. Setting this bit to 0 allows a return to the operating mode (set in OPCCR.OPCM[1:0]) that was active prior to the transition to Subosc-speed mode.

When transitioning from Software Standby mode to Normal mode or Snooze mode, the OPCCR.OPCM[1:0] and SOPCCR.SOPCM settings are as follows, regardless of their settings before entering Software Standby mode:

- OPCCR.OPCM[1:0] = 00b (High-speed mode)
- SOPCCR.SOPCM = 0b (not Subosc-speed mode).

If Software Standby mode is canceled before the transition to Software Standby completes, the OPCCR.OPCM[1:0] and SOPCCR.SOPCM bits retain their settings from before the WFI instruction executed. If this causes any problem, set the MCU to High-speed mode during the exception handling procedure when canceling Software Standby mode.

Table 11.4 shows the relationship between the operating power control modes and the OPCM[1:0] and SOPCM settings.

- SOPCCR.SOPCM = 0b (not Subosc-speed mode).

如果在转换到软件待机完成之前取消软件待机模式，则OPCCR.OPCM[1:0]和SOPCCR.SOPCM位将保留其在WFI指令执行之前的设置。如果这导致任何问题，请设置
取消软件待机模式时，MCU在异常处理过程中进入高速模式。

OPCM[1:0]位（工作电源控制模式选择）

OPCM[1:0]位选择正常和休眠模式下的工作功率控制模式。表11.4显示了工作功率控制模式与OPCM[1:0]和SOPCM设置之间的关系。

OPCMTSF标志（工作电源控制模式转换状态标志）

OPCMTSF标志指示切换操作功率控制模式时的切换控制状态。该标志在对OPCM[1:0]位进行写访问时设置为1，在模式转换完成时设置为0。在继续之前确认标志为0。

11.2.7 副操作功率控制寄存器(SOPCCR)

Address(es): SYSTEM.SOPCCR 4001 E0AAh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	SOPCMTSF	—	—	—	SOPCM
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	SOPCM	副操作功率控制模式选择	0：非Subosc速度模式1：Subosc速度模式。	R/W
b3 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b4	SOPCMTSF	副操作功率控制模式转换状态标志	0：转换完成1：转换进行中。	R
b7 to b5	—	Reserved	这些位被读取为0。写入值应为0。	R/W

SOPCCR寄存器用于通过启动进入和退出Subosc速度模式来降低正常和睡眠模式下的功耗。Subosc速度模式仅在使用副时钟振荡器或LOCO而不分频时可用。

在切换工作电源控制模式之前，应通过将FCACHEE.FCACHEEN设置为0将闪存缓存功能设置为禁用。有关详细信息，请参阅第55节，闪存。

有关更改运行功率控制模式的步骤，请参阅第11.5节"降低运行功率的功能"
Consumption.

SOPCM位（副工作功率控制模式选择）

SOPCM位选择正常和休眠模式下的工作功率控制模式。将此位设置为1允许转换到Subosc速度模式。将此位设置为0允许返回到转换到Subosc速度模式之前处于活动状态的操作模式（在OPCCR.OPCM[1:0]中设置）。

当从软件待机模式转换到正常模式或贪睡模式时，OPCCR.OCM[1:0]和
SOPCCR.SOPCM设置如下，无论其进入软件待机模式前的设置如何：

- OPCCR.OPCM[1:0] = 00b (High-speed mode)
- SOPCCR.SOPCM = 0b (not Subosc-speed mode).

如果在转换到软件待机完成之前取消软件待机模式，则OPCCR.OPCM[1:0]和SOPCCR.SOPCM位将保留其在WFI指令执行之前的设置。如果这导致任何问题，请设置
取消软件待机模式时，MCU在异常处理过程中进入高速模式。

表11.4显示了工作功率控制模式与OPCM[1:0]和SOPCM设置之间的关系。

SOPCMTSF flag (Sub Operating Power Control Mode Transition Status Flag)

The SOPCMTSF flag indicates the switching control state when the operating power control mode is switched to Subosc-speed mode or from Subosc-speed mode. The flag is set to 1 on a write access to the SOPCM bit, and to 0 when the mode transition completes. Confirm that the flag is 0 before proceeding.

Table 11.4 Relationship between the operating power control modes and the OPCM[1:0] and SOPCM settings

Operating power control mode	OPCM[1:0] bits	SOPCM bit	Power consumption
High-speed mode	00b	0	High
Low-speed mode	11b	0	↓
Subosc-speed mode	00b, 11b	1	Low

Note: See section 60, Electrical Characteristics, for the operating frequency range and voltage range.

High-speed operating mode

After a reset cancellation, the MCU is activated in this mode.

Low-speed mode

The following constraints apply in Low-speed mode:

- Programming and erasure operations for the flash memory are prohibited
- Using the PLL is prohibited. See section 11.10.1, Register Access.

In this mode, lower power consumption is possible than in High-speed mode when the same operation is performed under the same conditions, such as operating frequency and operating voltage.

Subosc-speed mode

The following constraints apply in Subosc-speed mode:

- Programming and erasure operations for the flash memory are prohibited
- Reading of the data flash is prohibited
- Using MOSC, PLL, MOCO, or HOCO is prohibited. See section 11.10.1, Register Access.
- Using the divided clock for ICK or FCK is prohibited. See section 11.10.1, Register Access.
- Using the oscillation stop detection function of the main clock oscillator is prohibited.

11.2.8 Snooze Control Register (SNZCR)

Address(es): SYSTEM.SNZCR 4001 E092h

	b7	b6	b5	b4	b3	b2	b1	b0
	SNZE	—	—	—	—	—	SNZDTCEN	RXDREQEN
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	RXDREQEN	RXD0 Snooze Request Enable	0: Ignore the RXD0 falling edge in Software Standby mode 1: Detect the RXD0 falling edge in Software Standby mode.	R/W
b1	SNZDTCEN	DTC Enable in Snooze mode	0: Disable DTC operation in Snooze mode 1: Enable DTC operation in Snooze mode.	R/W
b6 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	SNZE	Snooze Mode Enable	0: Disable Snooze mode 1: Enable Snooze mode.	R/W

SOPCMTSF标志（子工作电源控制模式转换状态标志）

SOPCMTSF标志指示当操作功率控制模式切换到时的切换控制状态
Subosc-speed模式或从Subosc-speed模式。该标志在对SOPCM位进行写访问时设置为1，在模式转换完成时设置为0。在继续之前确认标志为0。

Table 11.4 工作功率控制模式与OPCM[1:0]和SOPCM设置之间的关系

工作功率控制方式	OPCM[1:0] bits	SOPCM bit	能量消耗
High-speed mode	00b	0	High
Low-speed mode	11b	0	↓
Subosc-speed mode	00b, 11b	1	Low

Note: 有关工作频率范围和电压范围，请参见第60节，电气特性。

高速运行模式

复位取消后，MCU在此模式下激活。

Low-speed mode

以下约束适用于低速模式：

- 禁止对闪存进行编程和擦除操作
- 禁止使用PLL。请参阅第11.10.1节，注册访问。

在这种模式下，如果在相同的条件下（例如工作频率和工作电压）执行相同的操作，则功耗可能低于高速模式。

Subosc-speed mode

以下约束适用于Subosc速度模式：

- 禁止对闪存进行编程和擦除操作
- 禁止读取数据闪存
- 禁止使用MOSC、PLL、MOCO或HOCO。请参阅第11.10.1节，注册访问。
- 禁止将分频时钟用于ICK或FCK。请参阅第11.10.1节，注册访问。
- 禁止使用主时钟振荡器的振荡停止检测功能。

11.2.8 贪睡控制寄存器(SNZCR)

Address(es): SYSTEM.SNZCR 4001 E092h

	b7	b6	b5	b4	b3	b2	b1	b0
	SNZE	—	—	—	—	—	SNZDTCEN	RXDREQEN
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	RXDREQEN	RXD0贪睡请求启用	0：在软件待机模式下忽略RXD0下降沿1：在软件待机模式下检测RXD0下降沿。	R/W
b1	SNZDTCEN	在贪睡模式下启用DTC	0：在贪睡模式下禁用DTC操作1：在贪睡模式下启用DTC操作。	R/W
b6 to b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b7	SNZE	贪睡模式启用	0：禁用贪睡模式1：启用贪睡模式。	R/W

RXDREQEN bit (RXD0 Snooze Request Enable)

The RXDREQEN bit specifies whether to detect a falling edge of the RXD0 pin in Software Standby mode. This bit is only available when SCI0 is operating in asynchronous mode. To detect a falling edge of the RXD0 pin, set this bit before entering Software Standby mode. When this bit is set to 1, a falling edge of the RXD0 pin in Software Standby mode causes the MCU to enter Snooze mode.

SNZDTCEN bit (DTC Enable in Snooze mode)

The SNZDTCEN bit specifies whether to use the DTC and SRAM in Snooze mode. To use the DTC and SRAM in Snooze mode, set this bit to 1 before entering Software Standby mode. When this bit is set to 1, the DTC can be activated by setting IELSRn (ICU Event Link setting Register n).

SNZE bit (Snooze Mode Enable)

The SNZE bit enables or disables a transition from Software Standby to Snooze mode. To use Snooze mode, set this bit to 1 before entering Software Standby mode. When this bit is set to 1, one of the event triggers shown in Table 11.7 occurring in Software Standby mode causes the MCU to enter Snooze mode. After the MCU transitions from Software Standby or Snooze mode to Normal mode, clear the SNZE bit once and then set it before re-entering Software Standby mode. For details, see section 11.8, Snooze Mode.

11.2.9 Snooze End Control Register (SNZEDCR)

Address(es): SYSTEM.SNZEDCR 4001 E094h

	b7	b6	b5	b4	b3	b2	b1	b0
	SCI0UMTED	AD1UMTED	AD1MATED	AD0UMTED	AD0MATED	DTCNZRED	DTCZRED	AGTUNFED
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	AGTUNFED	AGT1 Underflow Snooze End Enable	0: Disable the Snooze end request 1: Enable the Snooze end request.	R/W
b1	DTCZRED	Last DTC Transmission Completion Snooze End Enable	0: Disable the Snooze end request 1: Enable the Snooze end request.	R/W
b2	DTCNZRED	Not Last DTC Transmission Completion Snooze End Enable	0: Disable the Snooze end request 1: Enable the Snooze end request.	R/W
b3	AD0MATED	AD Compare Match 0 Snooze End Enable	0: Disable the Snooze end request 1: Enable the Snooze end request.	R/W
b4	AD0UMTED	AD Compare Mismatch 0 Snooze End Enable	0: Disable the Snooze end request 1: Enable the Snooze end request.	R/W
b5	AD1MATED	AD Compare Match 1 Snooze End Enable	0: Disable the Snooze end request 1: Enable the Snooze end request.	R/W
b6	AD1UMTED	AD Compare Mismatch 1 Snooze End Enable	0: Disable the Snooze end request 1: Enable the Snooze end request.	R/W
b7	SCI0UMTED	SCI0 Address Mismatch Snooze End Enable	0: Disable the Snooze end request 1: Enable the Snooze end request.	R/W

To use one of the triggers shown in Table 11.8 as a condition for switching from Snooze to Software Standby mode, set the associated bit in the SNZEDCR register to 1.

The event that is used for returning to Normal mode from Snooze mode as listed in Table 11.3 must not be enabled in the SNZEDCR register.

AGTUNFED bit (AGT1 Underflow Snooze End Enable)

The AGTUNFED bit enables or disables a transition from Snooze to Software Standby mode on an AGT1 underflow. For details on the trigger conditions, see section 25, Asynchronous General-Purpose Timer (AGT).

RXDREQEN位（RXD0贪睡请求使能）

RXDREQEN位指定在软件待机模式下是否检测RXD0引脚的下降沿。该位仅在SCI0工作在异步模式时可用。要检测RXD0引脚的下降沿，请在进入软件待机模式之前设置该位。当该位设置为1时，软件待机模式下RXD0引脚的下降沿会导致MCU进入贪睡模式。

SNZDTCEN位（在贪睡模式下启用DTC）

SNZDTCEN位指定是否在贪睡模式下使用DTC和SRAM。使用DTC和SRAM
贪睡模式，在进入软件待机模式之前将该位设置为1。当该位设置为1时，可以通过设置IELSRn（ICU事件链接设置寄存器n）来激活DTC。

SNZE位（贪睡模式启用）

SNZE位启用或禁用从软件待机到贪睡模式的转换。要使用贪睡模式，请在进入软件待机模式之前将此位设置为1。当该位设置为1时，在软件待机模式下发生的表11.7中所示的事件触发之一会导致MCU进入贪睡模式。在MCU从软件待机或贪睡模式转换到正常模式后，清除一次SNZE位，然后在重新进入软件待机模式之前将其设置。有关详细信息，请参阅第11.8节，贪睡模式。

11.2.9 贪睡结束控制寄存器(SNZEDCR)

Address(es): SYSTEM.SNZEDCR 4001 E094h

	b7	b6	b5	b4	b3	b2	b1	b0
	SCI0UMTED	AD1UMTED	AD1MATED	AD0UMTED	AD0MATED	DTCNZRED	DTCZRED	AGTUNFED
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	AGTUNFED	AGT1下溢贪睡结束使能	0：禁用贪睡结束请求1：启用贪睡结束请求。	R/W
b1	DTCZRED	上次DTC传输完成 贪睡结束启用	0：禁用贪睡结束请求1：启用贪睡结束请求。	R/W
b2	DTCNZRED	不是最后一个DTC传输完成 贪睡结束启用	0：禁用贪睡结束请求1：启用贪睡结束请求。	R/W
b3	AD0MATED	AD比较匹配0暂停结束 Enable	0：禁用贪睡结束请求1：启用贪睡结束请求。	R/W
b4	AD0UMTED	AD比较不匹配0暂停结束 Enable	0：禁用贪睡结束请求1：启用贪睡结束请求。	R/W
b5	AD1MATED	AD比较匹配1暂停结束 Enable	0：禁用贪睡结束请求1：启用贪睡结束请求。	R/W
b6	AD1UMTED	AD比较不匹配1暂停结束 Enable	0：禁用贪睡结束请求1：启用贪睡结束请求。	R/W
b7	SCI0UMTED	SCI0地址不匹配贪睡结束 Enable	0：禁用贪睡结束请求1：启用贪睡结束请求。	R/W

要将表11.8中所示的触发器之一用作从贪睡模式切换到软件待机模式的条件，请将SNZEDCR寄存器中的相关位设置为1。

表11.3中列出的用于从贪睡模式返回到正常模式的事件不得在
SNZEDCR register.

AGTUNFED位（AGT1下溢贪睡结束使能）

AGTUNFED位启用或禁用在AGT1下溢时从贪睡到软件待机模式的转换。
有关触发条件的详细信息，请参见第25节，异步通用定时器(AGT)。

DTCZRED bit (Last DTC Transmission Completion Snooze End Enable)

The DTCZRED bit enables or disables a transition from Snooze to Software Standby mode on completion of the last DTC transmission, signaled when the CRA or CRB register in the DTC is 0. For details on the trigger conditions, see section 18, Data Transfer Controller (DTC).

DTCNZRED bit (Not Last DTC Transmission Completion Snooze End Enable)

The DTCNZRED bit enables or disables a transition from Snooze to Software Standby mode on completion of each DTC transmission, signaled when the CRA or CRB register in the DTC is not 0. For details on the trigger conditions, see section 18, Data Transfer Controller (DTC).

AD0MATED bit (AD Compare Match 0 Snooze End Enable)

The AD0MATED bit enables or disables a transition from Snooze to Software Standby mode on an AD0 event when a conversion result matches the expected data. For details on the trigger conditions, see section 47, 12-Bit A/D Converter (ADC12).

AD0UMTED bit (AD Compare Mismatch 0 Snooze End Enable)

The AD0UMTED bit enables or disables a transition from Snooze to Software Standby mode on an AD0 event when the conversion result does not match the expected data. For details on the trigger conditions, see section 47, 12-Bit A/D Converter (ADC12).

AD1MATED bit (AD Compare Match 1 Snooze End Enable)

The AD1MATED bit enables or disables a transition from Snooze to Software Standby mode on an AD1 event when the conversion result matches the expected data. For details on the trigger conditions, see section 47, 12-Bit A/D Converter (ADC12).

AD1UMTED bit (AD Compare Mismatch 1 Snooze End Enable)

The AD1UMTED bit enables or disables a transition from Snooze to Software Standby mode on an AD1 event when the conversion result does not match the expected data. For details on the trigger conditions, see section 47, 12-Bit A/D Converter (ADC12).

SCI0UMTED bit (SCI0 Address Mismatch Snooze End Enable)

The SCI0UMTED bit enables or disables a transition from Snooze to Software Standby mode on an SCI0 event when an address received in Software Standby mode does not match the expected data. For details on the trigger conditions, see section 34, Serial Communications Interface (SCI). Only set this bit to 1 when SCI0 is operating in asynchronous mode.

11.2.10 Snooze Request Control Register (SNZREQCR)

Address(es): SYSTEM.SNZREQCR 4001 E098h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	SNZREQEN30	SNZREQEN29	SNZREQEN28	—	—	SNZREQEN25	SNZREQEN24	—	SNZREQEN22	—	—	—	—	SNZREQEN17	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SNZREQEN15	SNZREQEN14	SNZREQEN13	SNZREQEN12	SNZREQEN11	SNZREQEN10	SNZREQEN9	SNZREQEN8	SNZREQEN7	SNZREQEN6	SNZREQEN5	SNZREQEN4	SNZREQEN3	SNZREQEN2	SNZREQEN1	SNZREQEN0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	SNZREQEN0	Snooze Request Enable 0	Enables the IRQ0 pin Snooze request: 0: Disable 1: Enable.	R/W

DTCZRED位（最后一个DTC传输完成贪睡结束使能）

当DTC中的CRA或CRB寄存器为0时，DTCZRED位启用或禁用从贪睡到软件待机模式的转换，当DTC中的CRA或CRB寄存器为0时发出信号。有关触发条件的详细信息，请参见第18节，数据传输控制器(故障诊断码）。

DTCNZRED位（非最后一个DTC传输完成贪睡结束使能）

DTCNZRED位在每次DTC传输完成时启用或禁用从贪睡到软件待机模式的转换，当DTC中的CRA或CRB寄存器不为0时发出信号。有关触发条件的详细信息，请参见第18节，数据传输控制器(故障诊断码）。

AD0MATED位（AD比较匹配0贪睡结束使能）

当转换结果与预期数据匹配时，AD0MATED位在AD0事件时启用或禁用从贪睡到软件待机模式的转换。有关触发条件的详细信息，请参阅第47节，12位AD转换器(ADC12)。

AD0UMTED位（AD比较不匹配0贪睡结束使能）

当转换结果与预期数据不匹配时，AD0事件发生时AD0UMTED位启用或禁用从贪睡到软件待机模式的转换。有关触发条件的详细信息，请参阅第47节，12位AD转换器(ADC12)。

AD1MATED位（AD比较匹配1贪睡结束使能）

当转换结果与预期数据匹配时，AD1MATED位在AD1事件发生时启用或禁用从贪睡到软件待机模式的转换。有关触发条件的详细信息，请参阅第47节，12位AD转换器(ADC12)。

AD1UMTED位（AD比较不匹配1贪睡结束使能）

当转换结果与预期数据不匹配时，AD1UMTED位在AD1事件发生时启用或禁用从贪睡模式到软件待机模式的转换。有关触发条件的详细信息，请参阅第47节，12位AD转换器(ADC12)。

SCI0UMTED位（SCI0地址不匹配贪睡结束使能）

当在软件待机模式下接收到的地址与预期数据不匹配时，SCI0UMTED位启用或禁用在SCI0事件上从贪睡到软件待机模式的转换。有关触发条件的详细信息，请参阅第34节，串行通信接口(SCI)。只有当SCI0工作在异步模式时，该位才设置为1。

11.2.10 贪睡请求控制寄存器(SNZREQCR)

Address(es): SYSTEM.SNZREQCR 4001 E098h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	SNZREQEN30	SNZREQEN29	SNZREQEN28	—	—	SNZREQEN25	SNZREQEN24	—	SNZREQEN22	—	—	—	—	SNZREQEN17	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SNZREQEN15	SNZREQEN14	SNZREQEN13	SNZREQEN12	SNZREQEN11	SNZREQEN10	SNZREQEN9	SNZREQEN8	SNZREQEN7	SNZREQEN6	SNZREQEN5	SNZREQEN4	SNZREQEN3	SNZREQEN2	SNZREQEN1	SNZREQEN0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	SNZREQEN0	暂停请求启用0	启用IRQ0引脚贪睡请求：0：禁用1：启用。	R/W

Bit	Symbol	Bit name	Description	R/W
b1	SNZREQEN1	Snooze Request Enable 1	Enables the IRQ1 pin Snooze request: 0: Disable 1: Enable.	R/W
b2	SNZREQEN2	Snooze Request Enable 2	Enables the IRQ2 pin Snooze request: 0: Disable 1: Enable.	R/W
b3	SNZREQEN3	Snooze Request Enable 3	Enables the IRQ3 pin Snooze request: 0: Disable 1: Enable.	R/W
b4	SNZREQEN4	Snooze Request Enable 4	Enables the IRQ4 pin Snooze request: 0: Disable 1: Enable.	R/W
b5	SNZREQEN5	Snooze Request Enable 5	Enables the IRQ5 pin Snooze request: 0: Disable 1: Enable.	R/W
b6	SNZREQEN6	Snooze Request Enable 6	Enables the IRQ6 pin Snooze request: 0: Disable 1: Enable.	R/W
b7	SNZREQEN7	Snooze Request Enable 7	Enables the IRQ7 pin Snooze request: 0: Disable 1: Enable.	R/W
b8	SNZREQEN8	Snooze Request Enable 8	Enables the IRQ8 pin Snooze request: 0: Disable 1: Enable.	R/W
b9	SNZREQEN9	Snooze Request Enable 9	Enables the IRQ9 pin Snooze request: 0: Disable 1: Enable.	R/W
b10	SNZREQEN10	Snooze Request Enable 10	Enables the IRQ10 pin Snooze request: 0: Disable 1: Enable.	R/W
b11	SNZREQEN11	Snooze Request Enable 11	Enables the IRQ11 pin Snooze request: 0: Disable 1: Enable.	R/W
b12	SNZREQEN12	Snooze Request Enable 12	Enables the IRQ12 pin Snooze request: 0: Disable 1: Enable.	R/W
b13	SNZREQEN13	Snooze Request Enable 13	Enables the IRQ13 pin Snooze request: 0: Disable 1: Enable.	R/W
b14	SNZREQEN14	Snooze Request Enable 14	Enables the IRQ14 pin Snooze request: 0: Disable 1: Enable.	R/W
b15	SNZREQEN15	Snooze Request Enable 15	Enables the IRQ15 pin Snooze request: 0: Disable 1: Enable.	R/W
b16	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b17	SNZREQEN17	Snooze Request Enable 17	Enables the Key Interrupt Snooze request: 0: Disable 1: Enable.	R/W
b21 to b18	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b22	SNZREQEN22	Snooze Request Enable 22	Enables the ACMPHS0 Snooze request: 0: Disable 1: Enable.	R/W
b23	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b24	SNZREQEN24	Snooze Request Enable 24	Enables the RTC alarm Snooze request: 0: Disable 1: Enable.	R/W

Bit	Symbol	位名称	Description	R/W
b1	SNZREQEN1	贪睡请求启用1	启用IRQ1引脚贪睡请求：0：禁用1：启用。	R/W
b2	SNZREQEN2	贪睡请求启用2	启用IRQ2引脚贪睡请求：0：禁用1：启用。	R/W
b3	SNZREQEN3	贪睡请求启用3	启用IRQ3引脚贪睡请求：0：禁用1：启用。	R/W
b4	SNZREQEN4	贪睡请求启用4	启用IRQ4引脚贪睡请求：0：禁用1：启用。	R/W
b5	SNZREQEN5	贪睡请求启用5	启用IRQ5引脚贪睡请求：0：禁用1：启用。	R/W
b6	SNZREQEN6	贪睡请求启用6	启用IRQ6引脚贪睡请求：0：禁用1：启用。	R/W
b7	SNZREQEN7	暂停请求启用7	启用IRQ7引脚贪睡请求：0：禁用1：启用。	R/W
b8	SNZREQEN8	贪睡请求启用8	启用IRQ8引脚贪睡请求：0：禁用1：启用。	R/W
b9	SNZREQEN9	贪睡请求启用9	启用IRQ9引脚贪睡请求：0：禁用1：启用。	R/W
b10	SNZREQEN10	暂停请求启用10	启用IRQ10引脚贪睡请求：0：禁用1：启用。	R/W
b11	SNZREQEN11	暂停请求启用11	启用IRQ11引脚贪睡请求：0：禁用1：启用。	R/W
b12	SNZREQEN12	暂停请求启用12	启用IRQ12引脚贪睡请求：0：禁用1：启用。	R/W
b13	SNZREQEN13	暂停请求启用13	启用IRQ13引脚贪睡请求：0：禁用1：启用。	R/W
b14	SNZREQEN14	暂停请求启用14	启用IRQ14引脚贪睡请求：0：禁用1：启用。	R/W
b15	SNZREQEN15	暂停请求启用15	启用IRQ15引脚贪睡请求：0：禁用1：启用。	R/W
b16	—	Reserved	该位读取为0。写入值应为0。	R/W
b17	SNZREQEN17	暂停请求启用17	启用按键中断贪睡请求：0：禁用1：启用。	R/W
b21 to b18	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b22	SNZREQEN22	贪睡请求启用22	启用ACMPHS0贪睡请求：0：禁用1：启用。	R/W
b23	—	Reserved	该位读取为0。写入值应为0。	R/W
b24	SNZREQEN24	贪睡请求启用24	启用RTC闹钟贪睡请求：0：禁用1：启用。	R/W

Bit	Symbol	Bit name	Description	R/W
b25	SNZREQEN25	Snooze Request Enable 25	Enables the RTC period Snooze request: 0: Disable 1: Enable.	R/W
b27, b26	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b28	SNZREQEN28	Snooze Request Enable 28	Enables the AGT1 underflow Snooze request: 0: Disable 1: Enable.	R/W
b29	SNZREQEN29	Snooze Request Enable 29	Enables the AGT1 compare match A Snooze request: 0: Disable 1: Enable.	R/W
b30	SNZREQEN30	Snooze Request Enable 30	Enables the AGT1 compare match B Snooze request: 0: Disable 1: Enable.	R/W
b31	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

The SNZREQCR register controls which triggers cause the MCU to switch from Software Standby to Snooze mode. If a trigger is selected as a request to cancel Software Standby mode in the WUPEN register (see section 14, Interrupt Controller Unit (ICU)), the MCU enters Normal mode when the trigger is generated even when the associated bit of the SNZREQCR is 1. The WUPEN register setting always has higher priority than the SNZREQCR register setting. For details, see section 11.8, Snooze Mode, and section 14, Interrupt Controller Unit (ICU).

11.2.11 Deep Software Standby Control Register (DPSBYCR)

Address(es): SYSTEM.DPSBYCR 4001 E400h

	b7	b6	b5	b4	b3	b2	b1	b0
	DPSBY	IOKEEP	—	—	—	—	DEEPCUT[1:0]	
Value after reset:	0	0	0	0	0	0	0	1

Bit	Symbol	Bit name	Description	R/W
b1, b0	DEEPCUT[1:0]	Power-Supply Control	b1 b0 0 0: Supply power to the Standby SRAM, low-speed on-chip oscillator, AGTn, and USBFS/USBHS resume detecting unit in Deep Software Standby mode 0 1: Do not supply power to the Standby SRAM, low-speed on-chip oscillator, AGTn, and USBFS/USBHS resume detecting unit in Deep Software Standby mode 1 0: Setting prohibited 1 1: Do not supply power to the Standby SRAM, low-speed on-chip oscillator, AGTn, and USBFS/USBHS resume detecting unit in Deep Software Standby mode. In addition, disable the LVD and enable the low-power function of the power-on reset circuit.	R/W
b5 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6	IOKEEP	I/O Port Retention	0: When Deep Software Standby mode is canceled, clear the I/O ports to the reset state 1: When Deep Software Standby mode is canceled, keep the I/O ports in the same state as in Deep Software Standby mode.	R/W
b7	DPSBY	Deep Software Standby	0: Sleep mode (SBYCR.SSBY = 0) or Software Standby mode (SBYCR.SSBY = 1) 1: Sleep mode (SBYCR.SSBY = 0) or Deep Software Standby mode (SBYCR.SSBY = 1).	R/W

The DPSBYCR register is not initialized by the internal reset signal that cancels Deep Software Standby mode. For details, see Table 6.2, Reset detect flags initialized by each reset source.

DEEPCUT[1:0] bits (Power-Supply Control)

The DEEPCUT[1:0] bits control the internal power supply to the Standby SRAM, low-speed on-chip oscillator, AGTn, and USBFS/USBHS resume detecting unit in Deep Software Standby mode. In addition, these bits control the state of the LVD and power-on reset circuit in Deep Software Standby mode. When a USBFS/HS suspend/resume interrupt is used

Bit	Symbol	位名称	Description	R/W
b25	SNZREQEN25	暂停请求启用25	启用RTC周期贪睡请求：0：禁用1：启用 。	R/W
b27, b26	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b28	SNZREQEN28	贪睡请求启用28	启用AGT1下溢贪睡请求：0：禁用1：启用。	R/W
b29	SNZREQEN29	贪睡请求启用29	启用AGT1比较匹配A贪睡请求：0：禁用1：启用。	R/W
b30	SNZREQEN30	暂停请求启用30	启用AGT1比较匹配B贪睡请求：0：禁用1：启用。	R/W
b31	—	Reserved	该位读取为0。写入值应为0。	R/W

SNZREQCR寄存器控制哪些触发器导致MCU从软件待机切换到贪睡模式。如果在WUPEN寄存器中选择触发作为取消软件待机模式的请求（参见第14节，中断控制器单元(ICU)），则MCU在产生触发时进入正常模式，即使

SNZREQCR为1。WUPEN寄存器设置的优先级始终高于SNZREQCR寄存器设置。有关详细信息，请参阅第11.8节，贪睡模式和第14节，中断控制器单元(ICU)。

11.2.11 深度软件待机控制寄存器(DPSBYCR)

Address(es): SYSTEM.DPSBYCR 4001 E400h

	b7	b6	b5	b4	b3	b2	b1	b0
	DPSBY	IOKEEP	—	—	—	—	DEEPCUT[1:0]	
重置后的值:	0	0	0	0	0	0	0	1

Bit	Symbol	位名称	Description	R/W
b1, b0	DEEPCUT[1:0]	Power-Supply Control	b1b000：为StandbySRAM、低速片内振荡器、AGTn和USBFS供电深度软件待机模式下USBHS恢复检测单元01：不给StandbySRAM供电，低速on-芯片振荡器、AGTn和USBFS深度软件待机模式下的USBHS恢复检测单元10：设置禁止11：不给待机SRAM、低速片上振荡器、AGTn和USBFSUSBHS恢复检测单元供电深度软件待机模式。另外，禁用LVD，启用上电复位电路的低功耗功能。	R/W
b5 to b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b6	IOKEEP	IO端口保留	0：取消深度软件待机模式时，将IO端口清除为复位状态1：取消深度软件待机模式时，保持IO端口处于与深度软件待机模式相同的状态。	R/W
b7	DPSBY	深度软件Standby	0：休眠模式（SBYCR.SSBY=0）或软件待机模式（SBYCR.SSBY=1）1：休眠模式（SBYCR.SSBY=0）或深度软件待机模式（SBYCR.SSBY=1）。	R/W

取消深度软件待机模式的内部复位信号不会初始化DPSBYCR寄存器。有关详细信息，请参见表6.2，每个复位源初始化的复位检测标志。

DEEPCUT[1:0]位（电源控制）

DEEPCUT[1:0]位控制深度软件待机模式下待机SRAM、低速片上振荡器、AGTn和USBFSUSBHS恢复检测单元的内部电源。此外，这些位在深度软件待机模式下控制LVD和上电复位电路的状态。当使用USBFSHS挂起恢复中断时

as a canceling source for Deep Software Standby mode, the DEEPCUT[1:0] bits must be set to 00b. When an LVD interrupt is used in Deep Software Standby mode, the DEEPCUT[1:0] bits must be set to 00b or 01b.

For lower power consumption, set the DEEPCUT[1:0] bits to 11b so that the LVD is stopped and the low power mode function of the power-on reset circuit is enabled. The internal power supply of the SRAM stops in Deep Software Standby mode regardless of the DEEPCUT[1:0] bit settings.

IOKEEP bit (I/O Port Retention)

In Deep Software Standby mode, the I/O ports keep the same states as in Software Standby mode. The IOKEEP bit specifies whether to reset the state of the I/O ports when Deep Software Standby mode is canceled.

DPSBY bit (Deep Software Standby)

The DPSBY bit controls transitions to Deep Software Standby mode. See Table 11.6 for details.

When the WFI instruction is executed while the SBYCR.SSBY and DPSBYCR.DPSBY bits are both 1, the MCU enters Deep Software Standby mode through Software Standby mode.

The DPSBY bit remains 1 when Deep Software Standby mode is canceled by certain pins that are the sources of external pin interrupts (NMI and IRQ0-DS to IRQ14-DS) or by a peripheral interrupt (RTC alarm, RTC interval, USB suspend/resume, voltage monitor 1, or voltage monitor 2). Write 0 to this bit to clear it.

The DPSBY setting is invalid when the OFS0.IWDTSTPCTL bit is 0 (counting continues), regardless of the setting in the OFS0.IWDTSTRT bit. When the SBYCR.SSBY and DPSBY bits are 1, the MCU transitions to Software Standby mode on execution of a WFI instruction.

The DPSBY setting is invalid when the voltage monitor 1 reset is enabled (LVD1CR0.RI = 1) or when the voltage monitor 2 reset is enabled (LVD2CR0.RI = 1). When the SBYCR.SSBY and the DPSBY bits are 1, the MCU transitions to Software Standby mode on execution of a WFI instruction.

11.2.12 Deep Software Standby Interrupt Enable Register 0 (DPSIER0)

Address(es): SYSTEM.DPSIER0 4001 E402h

	b7	b6	b5	b4	b3	b2	b1	b0
	DIRQ7E	DIRQ6E	DIRQ5E	DIRQ4E	DIRQ3E	DIRQ2E	DIRQ1E	DIRQ0E
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	DIRQ0E	IRQ0-DS Pin Enable	Enables canceling of Deep Software Standby mode by the IRQ0-DS pin: 0: Disable 1: Enable.	R/W
b1	DIRQ1E	IRQ1-DS Pin Enable	Enables canceling of Deep Software Standby mode by the IRQ1-DS pin: 0: Disable 1: Enable.	R/W
b2	DIRQ2E	IRQ2-DS Pin Enable	Enables canceling of Deep Software Standby mode by the IRQ2-DS pin: 0: Disable 1: Enable.	R/W
b3	DIRQ3E	IRQ3-DS Pin Enable	Enables canceling of Deep Software Standby mode by the IRQ3-DS pin: 0: Disable 1: Enable.	R/W
b4	DIRQ4E	IRQ4-DS Pin Enable	Enables canceling of Deep Software Standby mode by the IRQ4-DS pin: 0: Disable 1: Enable.	R/W
b5	DIRQ5E	IRQ5-DS Pin Enable	Enables canceling of Deep Software Standby mode by the IRQ5-DS pin: 0: Disable 1: Enable.	R/W

作为深度软件待机模式的取消源，DEEPCUT[1:0]位必须设置为00b。在深度软件待机模式下使用LVD中断时，DEEPCUT[1:0]位必须设置为00b或01b。

为降低功耗，将DEEPCUT[1:0]位设置为11b，以使LVD停止并启用上电复位电路的低功耗模式功能。无论DEEPCUT[1:0]位设置如何，SRAM的内部电源都会在深度软件待机模式下停止。

IOKEEP位（IO端口保留）

在深度软件待机模式下，IO端口保持与软件待机模式相同的状态。IOKEEP位指定当深度软件待机模式被取消时是否复位IO端口的状态。

DPSBY位（深度软件待机）

DPSBY位控制向深度软件待机模式的转换。详见表11.6。

当SBYCR.SSBY和DPSBYCR.DPSBY位均为1时执行WFI指令，MCU进入
深度软件待机模式到软件待机模式。

当某些作为外部引脚中断源（NMI和IRQ0-DS到IRQ14-DS）或外设中断（RTC警报、RTC间隔、USB挂起恢复、电压监视器1，或电压监视器2）。向该位写入0以清除它。

当OFS0.IWDTSTPCTL位为0（计数继续）时，DPSBY设置无效，无论OFS0.IWDTSTRT位中的设置如何。当SBYCR.SSBY和DPSBY位为1时，MCU在执行WFI指令时转换到软件待机模式。

启用电压监视器1复位(LVD1CR0.RI=1)或启用电压监视器2复位(LVD2CR0.RI=1)时，DPSBY设置无效。当SBYCR.SSBY和DPSBY位为1时，MCU在执行WFI指令时转换到软件待机模式。

11.2.12 深度软件待机中断使能寄存器0(DPSIER0)

Address(es): SYSTEM.DPSIER0 4001 E402h

	b7	b6	b5	b4	b3	b2	b1	b0
	DIRQ7E	DIRQ6E	DIRQ5E	DIRQ4E	DIRQ3E	DIRQ2E	DIRQ1E	DIRQ0E
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	DIRQ0E	IRQ0-DS引脚使能	启用通过IRQ0-DS引脚取消深度软件待机模式：0：禁用1：启用。	R/W
b1	DIRQ1E	IRQ1-DS引脚使能	启用通过IRQ1-DS引脚取消深度软件待机模式：0：禁用1：启用。	R/W
b2	DIRQ2E	IRQ2-DS引脚使能	启用通过IRQ2-DS引脚取消深度软件待机模式：0：禁用1：启用。	R/W
b3	DIRQ3E	IRQ3-DS引脚使能	启用通过IRQ3-DS引脚取消深度软件待机模式：0：禁用1：启用。	R/W
b4	DIRQ4E	IRQ4-DS引脚使能	启用通过IRQ4-DS引脚取消深度软件待机模式：0：禁用1：启用。	R/W
b5	DIRQ5E	IRQ5-DS引脚使能	启用通过IRQ5-DS引脚取消深度软件待机模式：0：禁用1：启用。	R/W

Bit	Symbol	Bit name	Description	R/W
b6	DIRQ6E	IRQ6-DS Pin Enable	Enables canceling of Deep Software Standby mode by the IRQ6-DS pin: 0: Disable 1: Enable.	R/W
b7	DIRQ7E	IRQ7-DS Pin Enable	Enables canceling of Deep Software Standby mode by the IRQ7-DS pin: 0: Disable 1: Enable.	R/W

The DPSIER0 register is not initialized by the internal reset signal that cancels Deep Software Standby mode. For details, see Table 6.2, Reset detect flags initialized by each reset source. After a setting in DPSIER0 is changed, an edge can be internally generated depending on the associated pin state, resulting in the associated DPSIFR0 bit being set to 1. Clear DPSIFR0 to 0 before entering Deep Software Standby mode.

11.2.13 Deep Software Standby Interrupt Enable Register 1 (DPSIER1)

Address(es): SYSTEM.DPSIER1 4001 E403h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	DIRQ14E	DIRQ13E	DIRQ12E	DIRQ11E	DIRQ10E	DIRQ9E	DIRQ8E
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	DIRQ8E	IRQ8-DS Pin Enable	Enables canceling of Deep Software Standby mode by the IRQ8-DS pin: 0: Disable 1: Enable.	R/W
b1	DIRQ9E	IRQ9-DS Pin Enable	Enables canceling of Deep Software Standby mode by the IRQ9-DS pin: 0: Disable 1: Enable.	R/W
b2	DIRQ10E	IRQ10-DS Pin Enable	Enables canceling of Deep Software Standby mode by the IRQ10-DS pin: 0: Disable 1: Enable.	R/W
b3	DIRQ11E	IRQ11-DS Pin Enable	Enables canceling of Deep Software Standby mode by the IRQ11-DS pin: 0: Disable 1: Enable.	R/W
b4	DIRQ12E	IRQ12-DS Pin Enable	Enables canceling of Deep Software Standby mode by the IRQ12-DS pin: 0: Disable 1: Enable.	R/W
b5	DIRQ13E	IRQ13-DS Pin Enable	Enables canceling of Deep Software Standby mode by the IRQ13-DS pin: 0: Disable 1: Enable.	R/W
b6	DIRQ14E	IRQ14-DS Pin Enable	Enables canceling of Deep Software Standby mode by the IRQ14-DS pin: 0: Disable 1: Enable.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

The DPSIER1 register is not initialized by the internal reset signal that cancels Deep Software Standby mode. For details, see Table 6.2, Reset detect flags initialized by each reset source. After a setting in DPSIER1 is changed, an edge can be internally generated depending on the associated pin state, resulting in the associated DPSIFR1 bit being set to 1. Clear DPSIFR1 to 0 before entering Deep Software Standby mode.

Bit	Symbol	位名称	Description	R/W
b6	DIRQ6E	IRQ6-DS引脚使能	启用通过IRQ6-DS引脚取消深度软件待机模式：0：禁用1：启用。	R/W
b7	DIRQ7E	IRQ7-DS引脚使能	启用通过IRQ7-DS引脚取消深度软件待机模式：0：禁用1：启用。	R/W

DPSIER0寄存器不会被取消深度软件待机模式的内部复位信号初始化。有关详细信息，请参见表6.2，每个复位源初始化的复位检测标志。更改DPSIER0中的设置后，可根据相关引脚状态在内部生成边沿，从而将相关DPSIFR0位设置为1。在进入深度软件待机模式之前将DPSIFR0清零。

11.2.13 深度软件待机中断使能寄存器1(DPSIER1)

Address(es): SYSTEM.DPSIER1 4001 E403h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	DIRQ14E	DIRQ13E	DIRQ12E	DIRQ11E	DIRQ10E	DIRQ9E	DIRQ8E
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	DIRQ8E	IRQ8-DS引脚使能	启用通过IRQ8-DS引脚取消深度软件待机模式：0：禁用1：启用。	R/W
b1	DIRQ9E	IRQ9-DS引脚使能	启用通过IRQ9-DS引脚取消深度软件待机模式：0：禁用1：启用。	R/W
b2	DIRQ10E	IRQ10-DS引脚使能	启用通过IRQ10-DS引脚取消深度软件待机模式：0：禁用1：启用。	R/W
b3	DIRQ11E	IRQ11-DS引脚使能	启用通过IRQ11-DS引脚取消深度软件待机模式：0：禁用1：启用。	R/W
b4	DIRQ12E	IRQ12-DS引脚使能	启用通过IRQ12-DS引脚取消深度软件待机模式：0：禁用1：启用。	R/W
b5	DIRQ13E	IRQ13-DS引脚使能	启用通过IRQ13-DS引脚取消深度软件待机模式：0：禁用1：启用。	R/W
b6	DIRQ14E	IRQ14-DS引脚使能	启用通过IRQ14-DS引脚取消深度软件待机模式：0：禁用1：启用。	R/W
b7	—	Reserved	该位读取为0。写入值应为0。	R/W

DPSIER1寄存器未被取消深度软件待机模式的内部复位信号初始化。有关详细信息，请参见表6.2，每个复位源初始化的复位检测标志。更改DPSIER1中的设置后，可根据相关引脚状态在内部生成边沿，从而将相关DPSIFR1位设置为1。在进入深度软件待机模式之前将DPSIFR1清零。

11.2.14 Deep Software Standby Interrupt Enable Register 2 (DPSIER2)

Address(es): SYSTEM.DPSIER2 4001 E404h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	DNMIE	DRTCAIE	DRTCIIE	DLVD2IE	DLVD1IE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	DLVD1IE	LVD1 Deep Software Standby Cancel Signal Enable	Enables canceling of Deep Software Standby mode by the voltage monitor 1 signal: 0: Disable 1: Enable.	R/W
b1	DLVD2IE	LVD2 Deep Software Standby Cancel Signal Enable	Enables canceling of Deep Software Standby mode by the voltage monitor 2 signal: 0: Disable 1: Enable.	R/W
b2	DRTCIIE	RTC Interval Interrupt Deep Software Standby Cancel Signal Enable	Enables canceling of Deep Software Standby mode by the RTC interval interrupt signal: 0: Disable 1: Enable.	R/W
b3	DRTCAIE	RTC Alarm Interrupt Deep Software Standby Cancel Signal Enable	Enables canceling of Deep Software Standby mode by the RTC alarm interrupt signal: 0: Disable 1: Enable.	R/W
b4	DNMIE	NMI Pin Enable	Enables canceling of Deep Software Standby mode by the NMI pin: 0: Disable 1: Enable.	R/W*1
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. 1 can be written only once. After 1 is written to this bit, subsequent write accesses are disabled.

The DPSIER2 register is not initialized by the internal reset signal that cancels Deep Software Standby mode. For details, see Table 6.2, Reset detect flags initialized by each reset source. After a setting in DPSIER2 is changed, an edge can be internally generated depending on the associated pin state, resulting in the associated DPSIFR2 bit being set to 1. Clear DPSIFR2 to 0 before entering Deep Software Standby mode.

11.2.15 Deep Software Standby Interrupt Enable Register 3 (DPSIER3)

Address(es): SYSTEM.DPSIER3 4001 E405h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	DAGT1IE	DUSBHSIE	DUSBFSIE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	DUSBFSIE	USBFS Suspend/Resume Deep Software Standby Cancel Signal Enable	Enables canceling of Deep Software Standby mode by a USBFS suspend/resume: 0: Disable 1: Enable.	R/W

11.2.14 深度软件待机中断使能寄存器2(DPSIER2)

Address(es): SYSTEM.DPSIER2 4001 E404h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	DNMIE	DRTCAIE	DRTCIIE	DLVD2IE	DLVD1IE
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	DLVD1IE	LVD1深度软件待机取消信号启用	通过电压监视器1信号启用深度软件待机模式的取消：0：禁用1：启用。	R/W
b1	DLVD2IE	LVD2深度软件待机取消信号启用	通过电压监视器2信号启用深度软件待机模式的取消：0：禁用1：启用。	R/W
b2	DRTCIIE	RTC间隔中断深度软件待机取消信号Enable	启用取消深度软件待机模式 RTC间隔中断信号：0：禁用 1：启用。	R/W
b3	DRTCAIE	RTC警报中断深度软件待机取消信号Enable	启用取消深度软件待机模式 RTC闹钟中断信号：0：禁用1：启用。	R/W
b4	DNMIE	NMI引脚使能	启用取消深度软件待机模式 NMI引脚： 0：禁用1 ：启用。	R/W*1
b7 to b5	—	Reserved	这些位被读取为0。写入值应为0。	R/W

注1.1只能写一次。向该位写入1后，禁止后续写访问。

DPSIER2寄存器不会被取消深度软件待机模式的内部复位信号初始化。有关详细信息，请参见表6.2，每个复位源初始化的复位检测标志。更改DPSIER2中的设置后，可根据相关引脚状态在内部生成边沿，从而将相关DPSIFR2位设置为1。在进入深度软件待机模式之前将DPSIFR2清零。

11.2.15 深度软件待机中断使能寄存器3(DPSIER3)

Address(es): SYSTEM.DPSIER3 4001 E405h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	DAGT1IE	DUSBHSIE	DUSBFSIE
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	DUSBFSIE	USBFS暂停恢复深度软件待机取消信号使能	启用取消深度软件待机模式 USBFS挂起恢复：0：禁用1：启用。	R/W

Bit	Symbol	Bit name	Description	R/W
b1	DUSBHSIE	USBHS Suspend/Resume Deep Software Standby Cancel Signal Enable	Enables canceling of Deep Software Standby mode by a USBHS suspend/resume: 0: Disable 1: Enable.	R/W
b2	DAGT1IE	AGT1 Underflow Deep Software Standby Cancel Signal Enable	Enables canceling of Deep Software Standby mode by an AGT1 underflow: 0: Disable 1: Enable.	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The DPSIER3 register is not initialized by the internal reset signal that cancels Deep Software Standby mode. For details, see Table 6.2, Reset detect flags initialized by each reset source. After a setting in DPSIER3 is changed, an edge can be internally generated depending on the associated pin state, resulting in the associated DPSIFR3 bit setting to 1. Clear DPSIFR3 to 0 before entering Deep Software Standby mode.

11.2.16 Deep Software Standby Interrupt Flag Register 0 (DPSIFR0)

Address(es): SYSTEM.DPSIFR0 4001 E406h

	b7	b6	b5	b4	b3	b2	b1	b0
	DIRQ7F	DIRQ6F	DIRQ5F	DIRQ4F	DIRQ3F	DIRQ2F	DIRQ1F	DIRQ0F
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	DIRQ0F	IRQ0-DS Deep Software Standby Cancel Flag	Indicates Deep Software Standby cancel request by the IRQ0-DS pin: 0: No request generated 1: Request generated.	R(/W) *1
b1	DIRQ1F	IRQ1-DS Deep Software Standby Cancel Flag	Indicates Deep Software Standby cancel request by the IRQ1-DS pin: 0: No request generated 1: Request generated.	R(/W) *1
b2	DIRQ2F	IRQ2-DS Deep Software Standby Cancel Flag	Indicates Deep Software Standby cancel request by the IRQ2-DS pin: 0: No request generated 1: Request generated.	R(/W) *1
b3	DIRQ3F	IRQ3-DS Deep Software Standby Cancel Flag	Indicates Deep Software Standby cancel request by the IRQ3-DS pin: 0: No request generated 1: Request generated.	R(/W) *1
b4	DIRQ4F	IRQ4-DS Deep Software Standby Cancel Flag	Indicates Deep Software Standby cancel request by the IRQ4-DS pin: 0: No request generated 1: Request generated.	R(/W) *1
b5	DIRQ5F	IRQ5-DS Deep Software Standby Cancel Flag	Indicates Deep Software Standby cancel request by the IRQ5-DS pin: 0: No request generated 1: Request generated.	R(/W) *1
b6	DIRQ6F	IRQ6-DS Deep Software Standby Cancel Flag	Indicates Deep Software Standby cancel request by the IRQ6-DS pin: 0: No request generated 1: Request generated.	R(/W) *1
b7	DIRQ7F	IRQ7-DS Deep Software Standby Cancel Flag	Indicates Deep Software Standby cancel request by the IRQ7-DS pin: 0: No request generated 1: Request generated.	R(/W) *1

Note 1. Only 0 can be written to clear the flag.

Bit	Symbol	位名称	Description	R/W
b1	DUSBHSIE	USBHS Suspend/Resume Deep 软件待机取消信号使能	启用取消深度软件待机模式 USBHS暂停恢复：0：禁用1：启用。	R/W
b2	DAGT1IE	AGT1下溢深度软件待机取消信号启用	允许通过AGT1下溢取消深度软件待机模式：0：禁用1：启用。	R/W
b7 to b3	—	Reserved	这些位被读取为0。写入值应为0。	R/W

DPSIER3寄存器未被取消深度软件待机模式的内部复位信号初始化。有关详细信息，请参见表6.2，每个复位源初始化的复位检测标志。更改DPSIER3中的设置后，可根据相关引脚状态在内部生成边沿，从而导致相关DPSIFR3位设置为1。在进入深度软件待机模式之前将DPSIFR3清零。

11.2.16 深度软件待机中断标志寄存器0(DPSIFR0)

Address(es): SYSTEM.DPSIFR0 4001 E406h

	b7	b6	b5	b4	b3	b2	b1	b0
	DIRQ7F	DIRQ6F	DIRQ5F	DIRQ4F	DIRQ3F	DIRQ2F	DIRQ1F	DIRQ0F
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	DIRQ0F	IRQ0-DS深度软件待机取消标志	表示深度软件待机取消请求由IRQ0-DS引脚：0：未产生请求1：产生请求。	R(/W) *1
b1	DIRQ1F	IRQ1-DS深度软件待机取消标志	表示深度软件待机取消请求由IRQ1-DS引脚：0：未产生请求1：产生请求。	R(/W) *1
b2	DIRQ2F	IRQ2-DS深度软件待机取消标志	表示深度软件待机取消请求由IRQ2-DS引脚：0：未产生请求1：产生请求。	R(/W) *1
b3	DIRQ3F	IRQ3-DS深度软件待机取消标志	表示深度软件待机取消请求由IRQ3-DS引脚：0：未产生请求1：产生请求。	R(/W) *1
b4	DIRQ4F	IRQ4-DS深度软件待机取消标志	表示深度软件待机取消请求由IRQ4-DS引脚：0：未产生请求1：产生请求。	R(/W) *1
b5	DIRQ5F	IRQ5-DS深度软件待机取消标志	表示深度软件待机取消请求由IRQ5-DS引脚：0：未产生请求1：产生请求。	R(/W) *1
b6	DIRQ6F	IRQ6-DS深度软件待机取消标志	表示深度软件待机取消请求由IRQ6-DS引脚：0：未产生请求1：产生请求。	R(/W) *1
b7	DIRQ7F	IRQ7-DS深度软件待机取消标志	表示深度软件待机取消请求由IRQ7-DS引脚：0：未产生请求1：产生请求。	R(/W) *1

Note 1. 只能写入0来清除标志。

The flags in the DPSIFR0 register set to 1 when the associated cancel request specified in DPSIEGR0 is generated. Each flag can be set to 1 when a cancel request is generated in any mode, not only in Deep Software Standby mode, or when the setting in DPSIER0 is changed. Clear DPSIFR0 to 00h before entering Deep Software Standby mode.

To clear DPSIFR0 to 00h after modifying DPSIER0, wait for at least 6 PCLKB cycles, read DPSIFR0, and then write 0 to DPSIFR0. 6 or more PCLKB cycles can be secured, for example, by reading DPSIER0. DPSIFR0 is not initialized by the internal reset signal that cancels Deep Software Standby mode. For details, see Table 6.2, Reset detect flags initialized by each reset source.

DIRQnF flags (IRQn-DS Deep Software Standby Cancel Flag) (n = 0 to 7)

The DIRQnF flag indicates that a cancel request was generated by the IRQn-DS pin.

[Setting condition]

- A cancel request generated by an IRQn-DS pin specified in DPSIEGR0.

[Clearing condition]

- Writing 0 to the flag after reading it as 1.

11.2.17 Deep Software Standby Interrupt Flag Register 1 (DPSIFR1)

Address(es): SYSTEM.DPSIFR1 4001 E407h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	DIRQ14F	DIRQ13F	DIRQ12F	DIRQ11F	DIRQ10F	DIRQ9F	DIRQ8F
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	DIRQ8F	IRQ8-DS Deep Software Standby Cancel Flag	Indicates Deep Software Standby cancel request by the IRQ8-DS pin: 0: No request generated 1: Request generated.	R(/W)*1
b1	DIRQ9F	IRQ9-DS Deep Software Standby Cancel Flag	Indicates Deep Software Standby cancel request by the IRQ9-DS pin: 0: No request generated 1: Request generated.	R(/W)*1
b2	DIRQ10F	IRQ10-DS Deep Software Standby Cancel Flag	Indicates Deep Software Standby cancel request by the IRQ10-DS pin: 0: No request generated 1: Request generated.	R(/W)*1
b3	DIRQ11F	IRQ11-DS Deep Software Standby Cancel Flag	Indicates Deep Software Standby cancel request by the IRQ11-DS pin: 0: No request generated 1: Request generated.	R(/W)*1
b4	DIRQ12F	IRQ12-DS Deep Software Standby Cancel Flag	Indicates Deep Software Standby cancel request by the IRQ12-DS pin: 0: No request generated 1: Request generated.	R(/W)*1
b5	DIRQ13F	IRQ13-DS Deep Software Standby Cancel Flag	Indicates Deep Software Standby cancel request by the IRQ13-DS pin: 0: No request generated 1: Request generated.	R(/W)*1
b6	DIRQ14F	IRQ14-DS Deep Software Standby Cancel Flag	Indicates Deep Software Standby cancel request by the IRQ14-DS pin: 0: No request generated 1: Request generated.	R(/W)*1
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R(/W)*1

Note 1. Only 0 can be written to clear the flag.

当生成DPSIEGR0中指定的相关取消请求时，DPSIFR0寄存器中的标志设置为1。当在任何模式下生成取消请求时，每个标志都可以设置为1，不仅在深度软件待机模式下，或者当DPSIER0中的设置更改时。在进入深度软件待机模式之前将DPSIFR0清零。

要在修改DPSIER0后将DPSIFR0清除为00h，请等待至少6个PCLKB周期，读取DPSIFR0，然后将0写入DPSIFR0。例如，通过读取DPSIER0可以确保6个或更多PCLKB周期。DPSIFR0不会被取消深度软件待机模式的内部复位信号初始化。有关详细信息，请参见表6.2，每个复位源初始化的复位检测标志。

DIRQnF标志（IRQn-DS深度软件待机取消标志）（n=0到7）

DIRQnF标志表示取消请求是由IRQn-DS管脚产生的。

[Setting condition]

- 由DPSIEGR0中指定的IRQn-DS管脚生成的取消请求。

[Clearing condition]

- 读为1后将0写入标志。

11.2.17 深度软件待机中断标志寄存器1(DPSIFR1)

Address(es): SYSTEM.DPSIFR1 4001 E407h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	DIRQ14F	DIRQ13F	DIRQ12F	DIRQ11F	DIRQ10F	DIRQ9F	DIRQ8F
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	DIRQ8F	IRQ8-DS深度软件待机取消标志	表示深度软件待机取消请求由IRQ8-DS引脚：0：未产生请求1：产生请求。	R(/W)*1
b1	DIRQ9F	IRQ9-DS深度软件待机取消标志	表示深度软件待机取消请求由IRQ9-DS引脚：0：未产生请求1：产生请求。	R(/W)*1
b2	DIRQ10F	IRQ10-DS深度软件待机取消标志	表示深度软件待机取消请求由IRQ10-DS引脚：0：未产生请求1：产生请求。	R(/W)*1
b3	DIRQ11F	IRQ11-DS深度软件待机取消标志	表示深度软件待机取消请求由IRQ11-DS引脚：0：未产生请求1：产生请求。	R(/W)*1
b4	DIRQ12F	IRQ12-DS深度软件待机取消标志	表示深度软件待机取消请求由IRQ12-DS引脚：0：未产生请求1：产生请求。	R(/W)*1
b5	DIRQ13F	IRQ13-DS深度软件待机取消标志	表示深度软件待机取消请求由IRQ13-DS引脚：0：未产生请求1：产生请求。	R(/W)*1
b6	DIRQ14F	IRQ14-DS深度软件待机取消标志	表示深度软件待机取消请求由IRQ14-DS引脚：0：未产生请求1：产生请求。	R(/W)*1
b7	—	Reserved	该位读取为0。写入值应为0。	R(/W)*1

Note 1. 只能写入0来清除标志。

The flags in the DPSIFR1 register set to 1 when the associated cancel request specified in DPSIEGR1 is generated. Each flag can be set to 1 when a cancel request is generated in any mode, not only in Deep Software Standby mode, or when the setting in DPSIER1 is changed. Clear DPSIFR1 to 00h before entering Deep Software Standby mode.

To clear DPSIFR1 to 00h after modifying DPSIER1, wait for at least 6 PCLKB cycles, read DPSIFR1, and then write 0 to DPSIFR1. 6 or more PCLKB cycles can be secured, for example, by reading DPSIER1. DPSIFR1 is not initialized by the internal reset signal that cancels Deep Software Standby mode. For details, see Table 6.2, Reset detect flags initialized by each reset source.

DIRQnF flags (IRQn-DS Deep Software Standby Cancel Flag) (n = 8 to 14)

The DIRQnF flag indicates that a cancel request was generated by the IRQn-DS pin.

[Setting condition]

- A cancel request generated by the IRQn-DS pin specified in DPSIEGR1.

[Clearing condition]

- Writing 0 to the flag after reading it as 1.

11.2.18 Deep Software Standby Interrupt Flag Register 2 (DPSIFR2)

Address(es): SYSTEM.DPSIFR2 4001 E408h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	DNMIF	DRTCAIF	DRTCIIF	DLVD2IF	DLVD1IF
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	DLVD1IF	LVD1 Deep Software Standby Cancel Flag	Indicates Deep Software Standby cancel request by the voltage monitor 1 signal: 0: No request generated 1: Request generated.	R(/W)*1
b1	DLVD2IF	LVD2 Deep Software Standby Cancel Flag	Indicates Deep Software Standby cancel request by the voltage monitor 2 signal: 0: No request generated 1: Request generated.	R(/W)*1
b2	DRTCIIF	RTC Interval Interrupt Deep Software Standby Cancel Flag	Indicates Deep Software Standby cancel request by the RTC interval interrupt signal: 0: No request generated 1: Request generated.	R(/W)*1
b3	DRTCAIF	RTC Alarm Interrupt Deep Software Standby Cancel Flag	Indicates Deep Software Standby cancel request by the RTC alarm interrupt signal: 0: No request generated 1: Request generated.	R(/W)*1
b4	DNMIF	NMI Deep Software Standby Cancel Flag	Indicates Deep Software Standby cancel request by the NMI pin: 0: No request generated 1: Request generated.	R(/W)*1
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Only 0 can be written to clear the flag.

The flags in the DPSIFR2 register set to 1 when the associated cancel request specified in DPSIEGR2 is generated. Each flag can be set to 1 when a cancel request is generated in any mode, not only in Deep Software Standby mode, or when the setting in DPSIER2 is changed. Clear DPSIFR2 to 00h before entering Deep Software Standby mode.

To clear DPSIFR2 to 00h after modifying DPSIER2, wait for at least 6 PCLKB cycles, read DPSIFR2, and then write 0 to DPSIFR2. 6 or more PCLKB cycles can be secured, for example, by reading DPSIER2. DPSIFR2 is not initialized by the internal reset signal that cancels Deep Software Standby mode. For details, see Table 6.2, Reset detect flags initialized by each reset source.

当生成DPSIEGR1中指定的相关取消请求时，DPSIFR1寄存器中的标志设置为1。当在任何模式下生成取消请求时，每个标志都可以设置为1，不仅在深度软件待机模式下，或者当DPSIER1中的设置更改时。在进入深度软件待机模式之前将DPSIFR1清零。

要在修改DPSIER1后将DPSIFR1清除为00h，请等待至少6个PCLKB周期，读取DPSIFR1，然后将0写入DPSIFR1。例如，通过读取DPSIER1可以确保6个或更多PCLKB周期。DPSIFR1不会被取消深度软件待机模式的内部复位信号初始化。有关详细信息，请参见表6.2，每个复位源初始化的复位检测标志。

DIRQnF标志（IRQn-DS深度软件待机取消标志）（n=8到14）

DIRQnF标志表示取消请求是由IRQn-DS管脚产生的。

[Setting condition]

- 由DPSIEGR1中指定的IRQn-DS引脚生成的取消请求。

[Clearing condition]

- 读为1后将0写入标志。

11.2.18 深度软件待机中断标志寄存器2(DPSIFR2)

Address(es): SYSTEM.DPSIFR2 4001 E408h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	DNMIF	DRTCAIF	DRTCIIF	DLVD2IF	DLVD1IF
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	DLVD1IF	LVD1深度软件待机取消标志	通过电压监视器1信号指示深度软件待机取消请求：0：未生成请求1：已生成请求。	R(/W)*1
b1	DLVD2IF	LVD2深度软件待机取消标志	通过电压监视器2信号指示深度软件待机取消请求：0：未生成请求1：已生成请求。	R(/W)*1
b2	DRTCIIF	RTC间隔中断深度软件待机取消标志	通过RTC间隔中断信号指示深度软件待机取消请求：0：未产生请求1：产生请求。	R(/W)*1
b3	DRTCAIF	RTC警报中断深度软件待机取消标志	通过RTC警报中断信号指示深度软件待机取消请求：0：未产生请求1：产生请求。	R(/W)*1
b4	DNMIF	NMI深度软件待机取消标志	通过NMI引脚指示深度软件待机取消请求：0：未生成请求1：已生成请求。	R(/W)*1
b7 to b5	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 只能写入0来清除标志。

当生成DPSIEGR2中指定的相关取消请求时，DPSIFR2寄存器中的标志设置为1。当在任何模式下生成取消请求时，每个标志都可以设置为1，不仅在深度软件待机模式下，或者当DPSIER2中的设置更改时。在进入深度软件待机模式之前将DPSIFR2清零。

要在修改DPSIER2后将DPSIFR2清除为00h，请等待至少6个PCLKB周期，读取DPSIFR2，然后将0写入DPSIFR2。例如，可以通过读取DPSIER2来确保6个或更多PCLKB周期。DPSIFR2不会被取消深度软件待机模式的内部复位信号初始化。有关详细信息，请参见表6.2，每个复位源初始化的复位检测标志。

DLVDmIF flag (LVDm Deep Software Standby Cancel Flag) (m = 1 or 2)

The DLVDmIF flag indicates that a cancel request was generated by the voltage monitor m signal.

[Setting condition]

- A cancel request generated by the voltage monitor m signal specified in DPSIEGR2.

[Clearing condition]

- Writing 0 to the flag after reading it as 1.

DRTCIIF flag (RTC Interval Interrupt Deep Software Standby Cancel Flag)

The DRTCIIF flag indicates that a cancel request was generated by the RTC interval interrupt signal.

[Setting condition]

- A cancel request generated by the RTC interval interrupt signal.

[Clearing condition]

- Writing 0 to the flag after reading it as 1.

DRTCAIF flag (RTC Alarm Interrupt Deep Software Standby Cancel Flag)

The DRTCAIF flag indicates that a cancel request was generated by the RTC alarm interrupt signal.

[Setting condition]

- A cancel request generated by the RTC alarm interrupt signal.

[Clearing condition]

- Writing 0 to the flag after reading it as 1.

DNMIF flag (NMI Deep Software Standby Cancel Flag)

The DNMIF flag indicates that a cancel request was generated by the NMI pin.

[Setting condition]

- A cancel request generated by the NMI pin specified in DPSIEGR2.

[Clearing condition]

- Writing 0 to the flag after reading it as 1.

11.2.19 Deep Software Standby Interrupt Flag Register 3 (DPSIFR3)

Address(es): SYSTEM.DPSIFR3 4001 E409h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	DAGT1IF	DUSBHSIF	DUSBFSIF
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	DUSBFSIF	USBFS Suspend/Resume Deep Software Standby Cancel Flag	Indicates Deep Software Standby cancel request by a USBFS suspend/resume: 0: No request generated 1: Request generated.	R(/W)*1
b1	DUSBHSIF	USBHS Suspend/Resume Deep Software Standby Cancel Flag	Indicates Deep Software Standby cancel request by a USBHS suspend/resume: 0: No request generated 1: Request generated.	R(/W)*1

DLVDmIF标志（LVDm深度软件待机取消标志）（m=1或2）

DLVDmIF标志表示电压监视器m信号产生了取消请求。

[Setting condition]

- 由DPSIEGR2中指定的电压监视器m信号生成的取消请求。

[Clearing condition]

- 读为1后将0写入标志。

DRTCIIF标志（RTC间隔中断深度软件待机取消标志）

DRTCIIF标志表明取消请求是由RTC间隔中断信号产生的。

[Setting condition]

- 由RTC间隔中断信号产生的取消请求。

[Clearing condition]

- 读为1后将0写入标志。

DRTCAIF标志（RTC报警中断深度软件待机取消标志）

DRTCAIF标志表明取消请求是由RTC警报中断信号产生的。

[Setting condition]

- 由RTC闹钟中断信号产生的取消请求。

[Clearing condition]

- 读为1后将0写入标志。

DNMIF标志（NMI深度软件待机取消标志）

DNMIF标志表示取消请求由NMI引脚生成。

[Setting condition]

- 由DPSIEGR2中指定的NMI引脚生成的取消请求。

[Clearing condition]

- 读为1后将0写入标志。

11.2.19 深度软件待机中断标志寄存器3(DPSIFR3)

Address(es): SYSTEM.DPSIFR3 4001 E409h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	DAGT1IF	DUSBHSIF	DUSBFSIF
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	DUSBFSIF	USBFS Suspend/Resume Deep 软件待机取消标志	表示深度软件待机取消请求由USBFS暂停恢复：0：未生成请求1：已生成请求。	R(/W)*1
b1	DUSBHSIF	USBHS Suspend/Resume Deep 软件待机取消标志	表示深度软件待机取消请求由USBHS暂停恢复：0：未生成请求1：生成请求。	R(/W)*1

Bit	Symbol	Bit name	Description	R/W
b2	DAGT1IF	AGT1 Underflow Deep Software Standby Cancel Flag	Indicates Deep Software Standby cancel request by an AGT1 underflow: 0: No request generated 1: Request generated.	R(/W)*1
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Only 0 can be written to clear the flag.

The flags in the DPSIFR3 register set to 1 when the associated cancel request is generated. Each flag can be set to 1 when a cancel request is generated in any mode, not only in Deep Software Standby mode, or when the setting in DPSIER3 is changed. Clear DPSIFR3 to 00h before entering Deep Software Standby mode.

To clear DPSIFR3 to 00h after modifying DPSIER3, wait for at least 6 PCLKB cycles, read DPSIFR3, and then write 0 to DPSIFR3. 6 or more PCLKB cycles can be secured, for example, by reading DPSIER3. DPSIFR3 is not initialized by the internal reset signal that cancels Deep Software Standby mode. For details, see section 6, Resets.

DUSBFSIF flag (USBFS Suspend/Resume Deep Software Standby Cancel Flag)

The DUSBFSIF flag indicates that a cancel request was generated by a USBFS suspend/resume.

[Setting condition]

- A cancel request generated by the USBFS suspend/resume.

[Clearing condition]

- Writing 0 to the flag after reading it as 1.

DUSBHSIF flag (USBHS Suspend/Resume Deep Software Standby Cancel Flag)

This DUSBHSIF flag indicates that a cancel request was generated by a USBHS suspend/resume.

[Setting condition]

- A cancel request generated by the USBHS suspend/resume.

[Clearing condition]

- Writing 0 to the flag after reading it as 1.

DAGT1IF flag (AGT1 Underflow Deep Software Standby Cancel Flag)

The DAGT1IF flag indicates that a cancel request was generated by an AGT1 underflow.

[Setting condition]

- A cancel request generated by the AGT1 underflow.

[Clearing condition]

- Writing 0 to the flag after reading it as 1.

11.2.20 Deep Software Standby Interrupt Edge Register 0 (DPSIEGR0)

Address(es): SYSTEM.DPSIEGR0 4001 E40Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	DIRQ7EG	DIRQ6EG	DIRQ5EG	DIRQ4EG	DIRQ3EG	DIRQ2EG	DIRQ1EG	DIRQ0EG
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	DIRQ0EG	IRQ0-DS Pin Edge Select	0: Generate cancel request on falling edge 1: Generate cancel request on rising edge.	R/W

Bit	Symbol	位名称	Description	R/W
b2	DAGT1IF	AGT1下溢深度软件待机取消标志	表示深度软件待机取消请求由AGT1下溢：0：未生成请求1：生成请求。	R(/W)*1
b7 to b3	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 只能写入0来清除标志。

当产生相关的取消请求时，DPSIFR3寄存器中的标志设置为1。当在任何模式下生成取消请求时，每个标志都可以设置为1，不仅在深度软件待机模式下，或者当DPSIER3中的设置更改时。在进入深度软件待机模式之前将DPSIFR3清零。

要在修改DPSIER3后将DPSIFR3清除为00h，请等待至少6个PCLKB周期，读取DPSIFR3，然后将0写入DPSIFR3。例如，通过读取DPSIER3可以确保6个或更多PCLKB周期。DPSIFR3不会被取消深度软件待机模式的内部复位信号初始化。有关详细信息，请参阅第6节，重置。

DUSBFSIF标志（USBFSSuspendResumeDeepSoftwareStandbyCancelFlag）

DUSBFSIF标志指示取消请求是由USBFS挂起恢复生成的。

[Setting condition]

- USBFS挂起恢复生成的取消请求。

[Clearing condition]

- 读为1后将0写入标志。

DUSBHSIF标志（USBHSSuspendResumeDeepSoftwareStandbyCancelFlag）

此DUSBHSIF标志指示取消请求是由USBHS挂起恢复生成的。

[Setting condition]

- USBHS暂停恢复生成的取消请求。

[Clearing condition]

- 读为1后将0写入标志。

DAGT1IF标志（AGT1下溢深度软件待机取消标志）

DAGT1IF标志指示取消请求是由AGT1下溢产生的。

[Setting condition]

- AGT1下溢生成的取消请求。

[Clearing condition]

- 读为1后将0写入标志。

11.2.20 深度软件待机中断边沿寄存器0(DPSIEGR0)

Address(es): SYSTEM.DPSIEGR0 4001 E40Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	DIRQ7EG	DIRQ6EG	DIRQ5EG	DIRQ4EG	DIRQ3EG	DIRQ2EG	DIRQ1EG	DIRQ0EG
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	DIRQ0EG	IRQ0-DS引脚边沿选择	0：下降沿产生取消请求1：上升沿产生取消请求。	R/W

Bit	Symbol	Bit name	Description	R/W
b1	DIRQ1EG	IRQ1-DS Pin Edge Select	0: Generate cancel request on falling edge 1: Generate cancel request on rising edge.	R/W
b2	DIRQ2EG	IRQ2-DS Pin Edge Select	0: Generate cancel request on falling edge 1: Generate cancel request on rising edge.	R/W
b3	DIRQ3EG	IRQ3-DS Pin Edge Select	0: Generate cancel request on falling edge 1: Generate cancel request on rising edge.	R/W
b4	DIRQ4EG	IRQ4-DS Pin Edge Select	0: Generate cancel request on falling edge 1: Generate cancel request on rising edge.	R/W
b5	DIRQ5EG	IRQ5-DS Pin Edge Select	0: Generate cancel request on falling edge 1: Generate cancel request on rising edge.	R/W
b6	DIRQ6EG	IRQ6-DS Pin Edge Select	0: Generate cancel request on falling edge 1: Generate cancel request on rising edge.	R/W
b7	DIRQ7EG	IRQ7-DS Pin Edge Select	0: Generate cancel request on falling edge 1: Generate cancel request on rising edge.	R/W

The DPSIEGR0 register is not initialized by the internal reset signal that cancels Deep Software Standby mode. For details, see Table 6.2, Reset detect flags initialized by each reset source.

11.2.21 Deep Software Standby Interrupt Edge Register 1 (DPSIEGR1)

Address(es): SYSTEM.DPSIEGR1 4001 E40Bh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	DIRQ14EG	DIRQ13EG	DIRQ12EG	DIRQ11EG	DIRQ10EG	DIRQ9EG	DIRQ8EG
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	DIRQ8EG	IRQ8-DS Pin Edge Select	0: Generate cancel request on falling edge 1: Generate cancel request on rising edge.	R/W
b1	DIRQ9EG	IRQ9-DS Pin Edge Select	0: Generate cancel request on falling edge 1: Generate cancel request on rising edge.	R/W
b2	DIRQ10EG	IRQ10-DS Pin Edge Select	0: Generate cancel request on falling edge 1: Generate cancel request on rising edge.	R/W
b3	DIRQ11EG	IRQ11-DS Pin Edge Select	0: Generate cancel request on falling edge 1: Generate cancel request on rising edge.	R/W
b4	DIRQ12EG	IRQ12-DS Pin Edge Select	0: Generate cancel request on falling edge 1: Generate cancel request on rising edge.	R/W
b5	DIRQ13EG	IRQ13-DS Pin Edge Select	0: Generate cancel request on falling edge 1: Generate cancel request on rising edge.	R/W
b6	DIRQ14EG	IRQ14-DS Pin Edge Select	0: Generate cancel request on falling edge 1: Generate cancel request on rising edge.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

The DPSIEGR1 register is not initialized by the internal reset signal that cancels Deep Software Standby mode. For details, see Table 6.2, Reset detect flags initialized by each reset source.

Bit	Symbol	位名称	Description	R/W
b1	DIRQ1EG	IRQ1-DS引脚边沿选择	0：下降沿产生取消请求1：上升沿产生取消请求。	R/W
b2	DIRQ2EG	IRQ2-DS引脚边沿选择	0：下降沿产生取消请求1：上升沿产生取消请求。	R/W
b3	DIRQ3EG	IRQ3-DS引脚边沿选择	0：下降沿产生取消请求1：上升沿产生取消请求。	R/W
b4	DIRQ4EG	IRQ4-DS引脚边沿选择	0：下降沿产生取消请求1：上升沿产生取消请求。	R/W
b5	DIRQ5EG	IRQ5-DS引脚边沿选择	0：下降沿产生取消请求1：上升沿产生取消请求。	R/W
b6	DIRQ6EG	IRQ6-DS引脚边沿选择	0：下降沿产生取消请求1：上升沿产生取消请求。	R/W
b7	DIRQ7EG	IRQ7-DS引脚边沿选择	0：下降沿产生取消请求1：上升沿产生取消请求。	R/W

DPSIEGR0寄存器不会被取消深度软件待机模式的内部复位信号初始化。有关详细信息，请参见表6.2，每个复位源初始化的复位检测标志。

11.2.21 深度软件待机中断边沿寄存器1(DPSIEGR1)

Address(es): SYSTEM.DPSIEGR1 4001 E40Bh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	DIRQ14EG	DIRQ13EG	DIRQ12EG	DIRQ11EG	DIRQ10EG	DIRQ9EG	DIRQ8EG
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	DIRQ8EG	IRQ8-DS引脚边沿选择	0：下降沿产生取消请求1：上升沿产生取消请求。	R/W
b1	DIRQ9EG	IRQ9-DS引脚边沿选择	0：下降沿产生取消请求1：上升沿产生取消请求。	R/W
b2	DIRQ10EG	IRQ10-DS引脚边沿选择	0：下降沿产生取消请求1：上升沿产生取消请求。	R/W
b3	DIRQ11EG	IRQ11-DS引脚边沿选择	0：下降沿产生取消请求1：上升沿产生取消请求。	R/W
b4	DIRQ12EG	IRQ12-DS引脚边沿选择	0：下降沿产生取消请求1：上升沿产生取消请求。	R/W
b5	DIRQ13EG	IRQ13-DS引脚边沿选择	0：下降沿产生取消请求1：上升沿产生取消请求。	R/W
b6	DIRQ14EG	IRQ14-DS引脚边沿选择	0：下降沿产生取消请求1：上升沿产生取消请求。	R/W
b7	—	Reserved	该位读取为0。写入值应为0。	R/W

DPSIEGR1寄存器不会被取消深度软件待机模式的内部复位信号初始化。有关详细信息，请参见表6.2，每个复位源初始化的复位检测标志。

11.2.22 Deep Software Standby Interrupt Edge Register 2 (DPSIEGR2)

Address(es): SYSTEM.DPSIEGR2 4001 E40Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	DNMIEG	—	—	DLVD2EG	DLVD1EG
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	DLVD1EG	LVD1 Edge Select	0: Generate cancel request when VCC < V_{det1} (fall) is detected 1: Generate cancel request when VCC ≥ V_{det1} (rise) is detected.	R/W
b1	DLVD2EG	LVD2 Edge Select	0: Generate cancel request when VCC < V_{det2} (fall) is detected 1: Generate cancel request when VCC ≥ V_{det2} (rise) is detected.	R/W
b3, b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	DNMIEG	NMI Pin Edge Select	0: Generate cancel request on falling edge 1: Generate cancel request on rising edge.	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The DPSIEGR2 register is not initialized by the internal reset signal that cancels Deep Software Standby mode. For details, see Table 6.2, Reset detect flags initialized by each reset source.

11.2.23 System Control OCD Control Register (SYOCDCR)

Address(es): SYSTEM.SYOCDCR 4001 E40Eh

	b7	b6	b5	b4	b3	b2	b1	b0
	DBGEN	—	—	—	—	—	—	DOCDF
Value after reset:	0	0	0	0	0	0	0	x

Bit	Symbol	Bit name	Description	R/W
b0	DOCDF	Deep Software Standby OCD Flag	Indicates cancel request by the DBIRQ: 0: DBIRQ is not generated 1: DBIRQ is generated.	R/(W)*1
b6 to b1	—	Reserved	These bits are read as 0. The write value must be 0.	R/W
b7	DBGEN	Debugger Enable Bit	0: Disable on-chip debugger 1: Enable on-chip debugger. Set to 1 first in on-chip debug mode.	R/W

Note 1. Writing 0 clears the flag. Writing 1 is ignored.

SYOCDCR is not initialized by the internal reset signal that cancels Deep Software Standby mode.

DOCDF flag (Deep Software Standby OCD Flag)

The DOCDF flag indicates that a Deep Software Standby cancel request was generated by the MCUCTRL.DBIRQ bit. The flag is set to 1 when the cancel request is generated. The flag can be set to 1 when a cancel request is generated in any mode, not only in Deep Software Standby mode. Clear the DOCDF flag to 0 before entering Deep Software Standby mode.

[Setting condition]

- A cancel request generated by the MCUCTRL.DBIRQ bit.

[Clearing condition]

- Writing 0 to the flag after reading it as 1

11.2.22 深度软件待机中断边沿寄存器2(DPSIEGR2)

Address(es): SYSTEM.DPSIEGR2 4001 E40Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	DNMIEG	—	—	DLVD2EG	DLVD1EG
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	DLVD1EG	LVD1边沿选择	0：检测到VCC<Vdet1（下降）时产生取消请求1：检测到VCC Vdet1（上升）时产生取消请求。	R/W
b1	DLVD2EG	LVD2边沿选择	0：检测到VCC<Vdet2（下降）时产生取消请求1：检测到VCC Vdet2（上升）时产生取消请求。	R/W
b3, b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b4	DNMIEG	NMI引脚边沿选择	0：下降沿产生取消请求1：上升沿产生取消请求。	R/W
b7 to b5	—	Reserved	这些位被读取为0。写入值应为0。	R/W

DPSIEGR2寄存器不会被取消深度软件待机模式的内部复位信号初始化。有关详细信息，请参见表6.2，每个复位源初始化的复位检测标志。

11.2.23 系统控制OCD控制寄存器(SYOCDCR)

Address(es): SYSTEM.SYOCDCR 4001 E40Eh

	b7	b6	b5	b4	b3	b2	b1	b0
	DBGEN	—	—	—	—	—	—	DOCDF
重置后的值：	0	0	0	0	0	0	0	x

Bit	Symbol	位名称	Description	R/W
b0	DOCDF	深度软件待机OCD标志	表示DBIRQ的取消请求：0：不产生DBIRQ1：产生DBIRQ。	R/(W)*1
b6 to b1	—	Reserved	这些位被读取为0。写入值必须为0。	R/W
b7	DBGEN	调试器启用位	0：禁用片上调试器1：启用片上调试器。在片上调试模式下首先设置为1。	R/W

Note 1. 写入0清除标志。写入1被忽略。

取消深度软件待机模式的内部复位信号不会初始化SOOCDCR。

DOCDF标志（深度软件待机OCD标志）

DOCDF标志表示深度软件待机取消请求由MCUCTRL.DBIRQ位生成。生成取消请求时，该标志设置为1。当在任何模式下生成取消请求时，该标志可以设置为1，而不仅仅是在深度软件待机模式下。在进入深度软件待机模式之前将DOCDF标志清零。

[Setting condition]

- 由MCUCTRL.DBIRQ位生成的取消请求。

[Clearing condition]

- 读为1后将0写入标志

- When the DBGEN bit is 0.

DBGEN bit (Debugger Enable Bit)

The DBGEN bit enables the on-chip debugger mode. This bit must be set to 1 first in the on-chip debug mode.

[Setting condition]

- Writing 1 to the bit when the debugger is connected.

[Clearing condition]

- Power-on reset is generated
- Writing 0 to the bit.

11.2.24 Standby Condition Register (STCONR)

Address(es): SYSTEM.STCONR 4001 E40Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	STCON[1:0]	
Value after reset:	1	1	0	0	0	0	1	1

Bit	Symbol	Bit name	Description	R/W
b1 to b0	STCON[1:0]	SSTBY Condition Bit	b1 b0 0 0: Set this value to transition to Software Standby mode when using HOCO 1 1: Set this value to transition to Software Standby mode when not using HOCO.	R/W
b5 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7 to b6	—	Reserved	These bits are read as 1. The write value should be 1.	R/W

STCON[1:0] bits (SSTBY Condition Bit)

The STCON[1:0] bits must always be set to 00b when using HOCO to enter Software Standby mode.

11.3 Reducing Power Consumption by Switching Clock Signals

When the SCKDIVCR.FCK[2:0], ICK[2:0], BCK[2:0], PCKA[2:0], PCKB[2:0], PCKC[2:0], and PCKD[2:0] bits are set, the clock frequency changes. The module and clock associations are as follows:

- The CPU, DMAC, DTC, flash, and SRAM use the operating clock specified in the ICK[2:0] bits
- Peripheral modules use the operating clocks specified in the PCKA[2:0], PCKB[2:0], PCKC[2:0], and PCKD[2:0] bits
- The flash memory interface uses the operating clock specified in the FCK[2:0] bits
- The external bus uses the operating clock specified in the BCK[2:0] bits.

For details, see section 9, Clock Generation Circuit.

11.4 Module-Stop Function

The module-stop function can be set for each on-chip peripheral module. When the MSTPmi bit (m = A to D; i = 31 to 0) in MSTPCRA to MSTPCRD is set to 1, the specified module stops operating and enters the module-stop state, but the CPU continues to operate independently. Clearing the MSTPmi bit to 0 cancels the module-stop state, allowing the module to resume operation at the end of the bus cycle. The internal states of the modules are retained in the module-stop state.

After a reset is canceled, all modules other than the DMAC, DTC, and SRAM modules are placed in the module-stop state. Do not access the module while the associated MSTPmi bit is 1. Otherwise, the read/write data and the operation of the module is not guaranteed. Do not set the MSTPmi bit to 1 while the associated module is being accessed.

- DBGEN位为0时。

DBGEN位（调试器启用位）

DBGEN位使能片上调试器模式。在片上调试模式下，该位必须首先设置为1。

[Setting condition]

- 连接调试器时向该位写入1。

[Clearing condition]

- 上电复位产生
- 将0写入该位。

11.2.24 待机条件寄存器(STCONR)

Address(es): SYSTEM.STCONR 4001 E40Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	STCON[1:0]	
重置后的值：	1	1	0	0	0	0	1	1

Bit	Symbol	位名称	Description	R/W
b1 to b0	STCON[1:0]	SSTBY条件位	b1b000：设置该值以在使用HOCO时转换到软件待机模式11：设置该值以在不使用HOCO时转换到软件待机模式。	R/W
b5 to b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b7 to b6	—	Reserved	这些位被读取为1。写入值应为1。	R/W

STCON[1:0]位（SSTBY条件位）

当使用HOCO进入软件待机模式时，STCON[1:0]位必须始终设置为00b。

11.3 通过切换时钟信号降低功耗

当SCKDIVCR.FCK[2:0]、ICK[2:0]、BCK[2:0]、PCKA[2:0]、PCKB[2:0]、PCKC[2:0]和PCKD[2:0]位被设置，时钟频率改变。模块和时钟关联如下：

- CPU、DMAC、DTC、闪存和SRAM使用ICK[2:0]位指定的工作时钟
- 外设模块使用PCKA[2:0]、PCKB[2:0]、PCKC[2:0]和PCKD[2:0]位中指定的工作时钟
- 闪存接口使用FCK[2:0]位中指定的工作时钟
- 外部总线使用BCK[2:0]位中指定的工作时钟。

有关详细信息，请参见第9节，时钟生成电路。

11.4 Module-Stop Function

可以为每个片上外围模块设置模块停止功能。当MSTPCRA到MSTPCRD中的MSTPmi位（m=A到D；i=31到0）设置为1时，指定模块停止运行并进入模块停止状态，但CPU继续独立运行。将MSTPmi位清0可取消模块停止状态，允许模块在总线周期结束时恢复运行。模块的内部状态保持在模块停止状态。

取消复位后，除DMAC、DTC和SRAM模块之外的所有模块都置于模块停止状态。相关MSTPmi位为1时请勿访问模块，否则无法保证读写数据和模块的操作。在访问相关模块时不要将MSTPmi位设置为1。

When the PLL is selected as the clock source, MSTPmi bits must be changed only one bit at a time. In this case, wait at least 250 ns after changing each MSTPmi bit before starting subsequent processing if you change any of the following bits: MSTPA22 (DMAC, DTC), MSTPB15 (ETHERC0, EDMAC0), MSTPB13 (EPTPC, PTPEDMAC), MSTPB12 (USBHS), MSTPC31 (SCE7), MSTPC6 (DRW), MSTPC5 (JPEG), MSTPC4 (GLCDC), or MSTPD5 (GPT32EH, GPT32E).

The recommended method to measure the wait time is to do so in software. Be sure to consider the worst-case use conditions to ensure that the required wait time elapses

11.5 Function for Lower Operating Power Consumption

Power consumption can be reduced in Normal, Sleep, and Snooze modes by selecting an appropriate operating power mode for the given operating frequency and operating voltage.

11.5.1 Setting the Operating Power Control Mode

Make sure that the operating conditions, such as the voltage and frequency ranges, are always within the specified ranges before and after switching the operating power control modes. This section provides example procedures for switching operating power control modes.

Table 11.5 Available oscillators in each mode

	Oscillator						
Mode	PLL	High-speed on-chip oscillator	Middle-speed on-chip oscillator	Low-speed on-chip oscillator	Main clock oscillator	Sub-clock oscillator	IWDT-dedicated on-chip oscillator
High-speed	Available	Available	Available	Available	Available	Available	Available
Low-speed	N/A	Available	Available	Available	Available	Available	Available
Subosc-speed	N/A	N/A	N/A	Available	N/A	Available	Available

(1) Switching from a higher to a lower power mode

Example 1: To switch from High-speed mode to Low-speed mode:

Operation begins in High-speed mode.

1. Change the oscillator to that used in Low-speed mode. Set the frequency of each clock lower than the maximum operating frequency in Low-speed mode.
2. Turn off the oscillator that is not required in Low-speed mode.
3. Confirm that the OPCCR.OPCMTSF flag is 0 (indicates transition completed).
4. Set the OPCCR.OPCM[1:0] bits to 11b (Low-speed mode).
5. Confirm that the OPCCR.OPCMTSF flag is 0 (indicates transition completed).

Operation is now in Low-speed mode.

Example 2: To switch from High-speed mode to Subosc-speed mode:

Operation begins in High-speed mode.

1. Change the clock source to the sub-clock oscillator. Turn off HOCO, MOCO, LOCO, main oscillator, and PLL.
2. Confirm that all clock sources except the sub-clock oscillator are stopped.
3. Confirm that the SOPCCR.SOPCMTSF flag is 0 (indicates transition completed).
4. Set the SOPCCR.SOPCM bit to 1 (Subosc-speed mode).
5. Confirm that the SOPCCR.SOPCMTSF flag is 0 (indicates transition completed).

Operation is now in Subosc-speed mode.

WhenthePLLisselectedastheclocksource MSTPmibitsmustbechangedonlyonebitatatime.在这种情况下，如果更改以下任何位，请在更改每个MSTPmi位后至少等待250ns，然后再开始后续处理：MSTPB22(DMAC DTC) MSTPB15(ETHERC0 EDMAC0) MSTPB13(EPTPC PTPEDMAC) MSTPB12(USBHS)、MSTPC31(SCE7)、MSTPC6(DRW)、MSTPC5(JPEG)、MSTPC4(GLCDC)或MSTPD5(GPT32EH、GPT32E)。

测量等待时间的推荐方法是在软件中进行。请务必考虑最坏情况下的使用条件，以确保经过所需的等待时间

11.5 降低运行功耗的功能

通过为给定的工作频率和工作电压选择合适的工作功率模式，可以降低正常、睡眠和贪睡模式下的功耗。

11.5.1 设置工作电源控制模式

确保操作条件，例如电压和频率范围，在切换操作功率控制模式之前和之后始终在指定范围内。本节提供切换操作电源控制模式的示例程序。

Table 11.5 每种模式下可用的振荡器

	Oscillator						
Mode	PLL	High-speed on-chip oscillator	Middle-speed on-chip oscillator	Low-speed on-chip oscillator	主时钟振荡器	Sub-clock oscillator	IWDT-dedicated on-chip oscillator
High-speed	Available	Available	Available	Available	Available	Available	Available
Low-speed	N/A	Available	Available	Available	Available	Available	Available
Subosc-speed	N/A	N/A	N/A	Available	N/A	Available	Available

(1) 从高功率模式切换到低功率模式

示例1：从高速模式切换到低速模式：

操作以高速模式开始。

1. 将振荡器更改为低速模式中使用的振荡器。将每个时钟的频率设置为低于低速模式下的最大工作频率。
2. 关闭低速模式下不需要的振荡器。
3. 确认OPCCR.OPCMTSF标志为0（表示转换完成） 。
4. 将OPCCR.OPCM[1:0]位设置为11b（低速模式）。
5. 确认OPCCR.OPCMTSF标志为0（表示转换完成） 。

操作现在处于低速模式。

示例2：从高速模式切换到Subosc速度模式：

操作以高速模式开始。

1. 将时钟源更改为副时钟振荡器。关闭HOCO、MOCO、LOCO、主振荡器和PLL。
2. 确认除副时钟振荡器之外的所有时钟源都已停止。
3. 确认SOPCCR.SOPCMTSF标志为0（表示转换完成） 。
4. 将SOPCCR.SOPCM位设置为1（Subosc速度模式）。
5. 确认SOPCCR.SOPCMTSF标志为0（表示转换完成） 。

操作现在处于Subosc速度模式。

(2) Switching from a lower to a higher power mode

Example 1: To switch from Subosc-speed mode to High-speed mode:

Operation begins in Subosc-speed mode.

1. Confirm that the SOPCCR.SOPCMTSF flag is 0 (indicates transition completed).
2. Set the SOPCCR.SOPCM bit to 0 (High-speed mode).
3. Confirm that the SOPCCR.SOPCMTSF flag is 0 (indicates transition completed).
4. Turn on the oscillator wanted in High-speed mode.
5. Set the frequency of each clock lower than the maximum operating frequency for High-speed mode.

Operation is now in High-speed mode.

Example 2: To switch Low-speed mode to High-speed mode:

Operation begins in Low-speed mode.

1. Confirm that the OPCCR.OPCMTSF flag is 0 (indicates transition completed).
2. Set the OPCCR.OPCM[1:0] bits to 00b (High-speed mode).
3. Confirm that the OPCCR.OPCMTSF flag is 0 (indicates transition completed).
4. Turn on any oscillator wanted in High-speed mode.
5. Set the frequency of each clock lower than the maximum operating frequency for High-speed mode.

Operation is now in High-speed mode.

11.6 Sleep Mode

11.6.1 Transition to Sleep Mode

When a WFI instruction is executed while the SBYCR.SSBY bit is 0, the MCU enters Sleep mode. In Sleep mode, the CPU stops operating, but the contents of its internal registers are retained. Other peripheral functions do not stop. Available resets or interrupts in Sleep mode cause the MCU to cancel Sleep mode. All interrupt sources are available. If using an interrupt to cancel Sleep mode, you must set the associated IELSRn register before executing a WFI instruction. For details, see section 14, Interrupt Controller Unit (ICU).

Counting by the IWDT stops when the MCU enters Sleep mode while the IWDT is in auto start mode and the OFS0.IWDTSTPCTL bit is 1 (IWDT stops in Sleep, Software Standby, or Snooze mode).

Counting by the IWDT continues when the MCU enters Sleep mode while the IWDT is in auto start mode and the OFS0.IWDTSTPCTL bit is 0 (IWDT does not stop in Sleep, Software Standby, or Snooze mode).

Counting by the WDT stops when the MCU enters Sleep mode while the WDT is in auto start mode and the OFS0.WDTSTPCTL bit is 1 (WDT stops in Sleep mode). In the same way, counting by the WDT stops when the MCU enters Sleep mode while the WDT is in register start mode and the WDTCSTPR.SLCSTP bit in is 1 (WDT stops in Sleep mode).

Counting by the WDT continues when the MCU enters Sleep mode while the WDT is in auto start mode and the OFS0. WDTSTPCTL bit is 0 (WDT does not stop in Sleep mode). In the same way, counting by the WDT continues when the MCU enters Sleep mode while the WDT is in register start mode and the WDTCSTPR.SLCSTP bit is 0 (WDT does not stop in Sleep mode).

11.6.2 Canceling Sleep Mode

Sleep mode is canceled by any interrupt, RES pin reset, power-on reset, voltage monitor reset, SRAM parity error reset, SRAM ECC error reset, Bus master MPU error reset, Bus slave MPU error reset, or reset caused by IWDT or WDT underflow. The operations are as follows:

- Canceling by an interrupt
  When an available interrupt request (see Table 11.3) is generated, Sleep mode is canceled and the MCU starts the

(2) 从低功率模式切换到高功率模式

示例1：从Subosc速度模式切换到高速模式：

操作以Subosc速度模式开始。

1. 确认SOPCCR.SOPCMTSF标志为0（表示转换完成） 。
2. 将SOPCCR.SOPCM位设置为0（高速模式）。
3. 确认SOPCCR.SOPCMTSF标志为0（表示转换完成） 。
4. 在高速模式下打开所需的振荡器。
5. 将每个时钟的频率设置为低于高速模式的最大工作频率。

操作现在处于高速模式。

示例2：将低速模式切换到高速模式：

操作以低速模式开始。

1. 确认OPCCR.OPCMTSF标志为0（表示转换完成） 。
2. 将OPCCR.OPCM[1:0]位设置为00b（高速模式）。
3. 确认OPCCR.OPCMTSF标志为0（表示转换完成） 。
4. 在高速模式下打开任何需要的振荡器。
5. 将每个时钟的频率设置为低于高速模式的最大工作频率。

操作现在处于高速模式。

11.6 睡眠模式

11.6.1 过渡到睡眠模式

当SBYCR.SSBY位为0时执行WFI指令时，MCU进入休眠模式。在睡眠模式下，CPU停止运行，但其内部寄存器的内容被保留。其他外围功能不会停止。

休眠模式下可用的复位或中断会导致MCU取消休眠模式。所有中断源均可用。如果使用中断取消休眠模式，则必须在执行WFI指令之前设置相关的IELSRn寄存器。有关详细信息，请参阅第14节，中断控制器单元(ICU)。

当MCU进入休眠模式且IWDT处于自动启动模式且
OFS0.IWDTSTPCTL位为1（IWDT在休眠、软件待机或贪睡模式下停止）。

当MCU进入休眠模式且IWDT处于自动启动模式且
OFS0.IWDTSTPCTL位为0（IWDT在休眠、软件待机或贪睡模式下不停止）。

当MCU进入休眠模式且WDT处于自动启动模式且WDT处于自动启动模式时，WDT停止计数
OFS0.WDTSTPCTL位为1（WDT在休眠模式下停止）。同样，当MCU进入休眠模式，而WDT处于寄存器启动模式且WDTCSTPR.SLCSTP位为1（休眠模式下WDT停止）时，WDT停止计数。

当MCU进入休眠模式且WDT处于自动启动模式和OFS0时，WDT继续计数。WDTSTPCTL位为0（WDT在休眠模式下不停止）。同样，当MCU进入休眠模式且WDT处于寄存器启动模式且WDTCSTPR.SLCSTP位为0（休眠模式下WDT不会停止）时，WDT继续计数。

11.6.2 取消睡眠模式

任何中断、RES引脚复位、上电复位、电压监视器复位、SRAM奇偶校验错误复位、
SRAMECC错误复位、总线主控MPU错误复位、总线从属MPU错误复位或由IWDT或WDT下溢引起的复位。
操作如下：

- 通过中断取消
  当产生一个可用的中断请求（见表11.3）时，休眠模式被取消并且MCU启动

interrupt handling.

- Canceling by RES pin reset
  When the RES pin is driven low, the MCU enters the reset state. You must keep the RES pin low for the time period specified in section 60, Electrical Characteristics. When the RES pin is driven high after the specified time period, the CPU starts reset exception handling.
- Canceling by IWDT reset
  Sleep mode is canceled by an internal reset generated by an IWDT underflow, and the MCU starts reset exception handling. Under the following conditions, the IWDT stops in Sleep mode and an internal reset for canceling Sleep mode is not generated:
  - OFS0.IWDTSTRT = 0 and OFS0.IWDTSTPCTL = 1.
- Canceling by WDT reset
  Sleep mode is canceled by an internal reset generated by an WDT underflow and the MCU starts reset exception handling. Under the following conditions, the WDT stops in Sleep mode even when counting in Normal mode and an internal reset for canceling Sleep mode is not generated:
  - OFS0.WDTSTRT = 0 (auto start mode) and OFS0.WDTSTPCTL = 1
  - OFS0.WDTSTRT = 1 (register start mode) and WDTCSTPR.SLCSTP = 1.
- Canceling by other resets available in Sleep mode
  Sleep mode is canceled by the associated resets, and the MCU starts reset exception handling.

Note: For details on correct setting of the interrupts, see section 14, Interrupt Controller Unit (ICU).

11.7 Software Standby Mode

11.7.1 Transition to Software Standby Mode

When a WFI instruction is executed while the SBYCR.SSBY bit is 1 and the DPSBYCR.DPSBY bit is 0, the MCU enters Software Standby mode. In this mode, the CPU, most of the on-chip peripheral functions, and the oscillators stop. However, the contents of the CPU internal registers and the SRAM data, the states of the on-chip peripheral functions, and the I/O port states are retained. Software Standby mode allows a significant reduction in power consumption because most of the oscillators stop in this mode. Table 11.2 shows the status of the on-chip peripheral functions and oscillators. Available resets or interrupts in Software Standby mode cause the MCU to cancel Software Standby mode. See Table 11.3 for available interrupt sources and section 14.2.9, Wake Up Interrupt Enable Register (WUPEN) for information on waking up the MCU from Software Standby mode. If using an interrupt to cancel Software Standby mode, you must set the associated IELSRn register before executing a WFI instruction. For details, see section 14, Interrupt Controller Unit (ICU).

The status of the address bus and bus control signals in Software Standby mode can be selected with the SBYCR.OPE bit.

Clear the DMAST.DMST and DTCST.DTCST bits to 0 before executing a WFI instruction, except when using the DTC in Snooze mode. If the DTC is required in Snooze mode, set the DTCST.DTCST bit to 1 before executing a WFI instruction.

Counting by the IWDT stops when the MCU enters Software Standby mode while the IWDT is in auto start mode and the OFS0.IWDTSTPCTL bit is 1 (IWDT stops in Sleep, Software Standby, or Snooze mode).

Counting by the IWDT continues when the MCU enters Software Standby mode while the IWDT is in auto start mode and the OFS0.IWDTSTPCTL bit is 0 (IWDT does not stop in Sleep mode, Software Standby, or Snooze mode).

The WDT stops counting when the MCU enters Software Standby mode.

Do not enter Software Standby mode while OSTDCR.OSTDE is 1 (oscillation stop detection function enabled). To enter Software Standby mode, execute a WFI instruction after disabling the oscillation stop detection function (OSTDCR.OSTDE is 0). If the software executes a WFI instruction while OSTDCR.OSTDE is 1, the MCU enters Sleep mode even when SBYCR.SSBY is 1. Do not enter Software Standby mode while the flash memory is performing a programming or erasing procedure. To enter Software Standby mode, execute a WFI instruction after the programming or erasing procedure completes.

When the PLL is selected as the clock source, set the following modules into the module-stop state before executing a

中断处理。

- 通过RES引脚复位取消
  当RES引脚驱动为低电平时，MCU进入复位状态。您必须在第60节“电气特性”中指定的时间段内保持RES引脚为低电平。当RES引脚在指定时间后被驱动为高电平时，CPU开始复位异常处理。
- 通过IWDT复位取消
  休眠模式由IWDT下溢产生的内部复位取消，MCU开始复位异常处理。在以下情况下，IWDT停止在休眠模式，并且不会产生用于取消休眠模式的内部复位：
  - OFS0.IWDTSTRT = 0 and OFS0.IWDTSTPCTL = 1.
- 通过WDT复位取消
  休眠模式由WDT下溢产生的内部复位取消，MCU开始复位异常处理。在以下情况下，即使在正常模式下计数，WDT也会在休眠模式下停止，并且不会产生用于取消休眠模式的内部复位：
  - OFS0.WDTSTRT=0（自动启动模式）和OFS0.WDTSTPCTL=1
  - OFS0.WDTSTRT=1（寄存器启动模式）和WDTCSTPR.SLCSTP=1。
- 通过睡眠模式下可用的其他复位取消
  睡眠模式被相关的复位取消，MCU开始复位异常处理。

Note: 有关正确设置中断的详细信息，请参阅第14节，中断控制器单元(ICU)。

11.7 软件待机模式

11.7.1 过渡到软件待机模式

当SBYCR.SSBY位为1且DPSBYCR.DPSBY位为0时执行WFI指令，MCU进入软件待机模式。在此模式下，CPU、大部分片上外围功能和振荡器停止。但是，CPU内部寄存器和SRAM数据的内容、片上外围功能的状态以及IO端口状态都被保留。软件待机模式可显着降低功耗，因为大多数振荡器在此模式下停止。表11.2显示了片上外围功能和振荡器的状态。软件待机模式下可用的复位或中断会导致MCU取消软件待机模式。有关可用中断源的信息，请参见表11.3，有关将MCU从软件待机模式唤醒的信息，请参见第14.2.9节，唤醒中断使能寄存器(WUPEN)。如果使用中断取消软件待机模式，则必须在执行WFI指令之前设置相关的IELSRn寄存器。有关详细信息，请参阅第14节，中断控制器单元(ICU)。

软件待机模式下的地址总线和总线控制信号的状态可以通过SBYCR.OPE位来选择。

在执行WFI指令之前将DMAST.DMST和DTCST.DTCST位清零，除非在贪睡模式下使用DTC。如果在贪睡模式下需要DTC，请在执行WFI指令之前将DTCST.DTCST位设置为1。

当IWDT处于自动启动模式且OFS0.IWDTSTPCTL位为1（IWDT在休眠、软件待机或贪睡模式下停止）时，当MCU进入软件待机模式时，IWDT停止计数。

当MCU进入软件待机模式且IWDT处于自动启动模式且OFS0.IWDTSTPCTL位为0（IWDT在睡眠模式、软件待机或贪睡模式下不停止）时，IWDT继续计数。

当MCU进入软件待机模式时，WDT停止计数。

OSTDCR.OSTDE为1（振荡停止检测功能启用）时不要进入软件待机模式。要进入软件待机模式，请在禁用振荡停止检测功能（OSTDCR.OSTDE为0）后执行WFI指令。如果软件在OSTDCR.OSTDE为1时执行WFI指令，即使SBYCR.SSBY为1，MCU也会进入休眠模式。在闪存执行编程或擦除过程时不要进入软件待机模式。要进入软件待机模式，请在编程或擦除过程完成后执行WFI指令。

WhenthePLLisselectedastheclocksource setthefollowingmodulesintothemodule-stopstatebeforeexecutinga

WFI instruction: ETHERC, EPTPC, EDMAC, SCE7, DRW, JPEG, GLCDC, GPT32EH, GPT32E. In this case, you must also insert wait time at least 750 ns before executing the WFI instruction. The recommended method to measure the wait time is to do so in software. Be sure to consider the worst-case use conditions to ensure that the required wait time elapses.

Table 11.6 shows the setting of the related control bits and the modes entered on execution of a WFI instruction.

Figure 11.2 shows an example flow for transitioning to Software Standby or Deep Software Standby mode.

Table 11.6 Bit settings that affect modes on WFI instruction execution

Other bit settings		SBYCR.SSBY and DPSBYCR.DPSBY bit settings			
		SSBY = 0, DPSBY = 0	SSBY = 0, DPSBY = 1	SSBY = 1, DPSBY = 0	SSBY = 1, DPSBY = 1
OSTDCR.OSTDE	0	Sleep mode	Sleep mode	Software Standby mode	Deep Software Standby mode
	1			Sleep mode	Sleep mode
FENTRYR.FENTRYi	0	Sleep mode	Sleep mode	Software Standby mode	Deep Software Standby mode
	1			Sleep mode	Sleep mode
OFS0.IWDTSTPCTL	0	Sleep mode	Sleep mode	Software Standby mode	Software Standby mode
	1				Deep Software Standby mode
LVD1CR0.RI	0	Sleep mode	Sleep mode	Software Standby mode	Deep Software Standby mode
	1				Software Standby mode
LVD2CR0.RI	0	Sleep mode	Sleep mode	Software Standby mode	Deep Software Standby mode
	1				Software Standby mode

WFI指令：ETHERC、EPPTC、EDMAC、SCE7、DRW、JPEG、GLCDC、GPT32EH、GPT32E。在这种情况下，您还必须在执行WFI指令之前插入至少750ns的等待时间。测量等待时间的推荐方法是在软件中进行。请务必考虑最坏的使用条件，以确保经过所需的等待时间。

表11.6显示了相关控制位的设置以及在执行WFI指令时进入的模式。

图11.2显示了转换到软件待机或深度软件待机模式的示例流程。

Table 11.6 影响WFI指令执行模式的位设置

其他位设置		SBYCR.SSBY和DPSBYCR.DPSBY位设置			
		SSBY = 0, DPSBY = 0	SSBY = 0, DPSBY = 1	SSBY = 1, DPSBY = 0	SSBY = 1, DPSBY = 1
OSTDCR.OSTDE	0	睡眠模式	睡眠模式	软件待机模式	深度软件待机模式
	1			睡眠模式	睡眠模式
FENTRYR.FENTRYi	0	睡眠模式	睡眠模式	软件待机模式	深度软件待机模式
	1			睡眠模式	睡眠模式
OFS0.IWDTSTPCTL	0	睡眠模式	睡眠模式	软件待机模式	软件待机模式
	1				深度软件待机模式
LVD1CR0.RI	0	睡眠模式	睡眠模式	软件待机模式	深度软件待机模式
	1				软件待机模式
LVD2CR0.RI	0	睡眠模式	睡眠模式	软件待机模式	深度软件待机模式
	1				软件待机模式

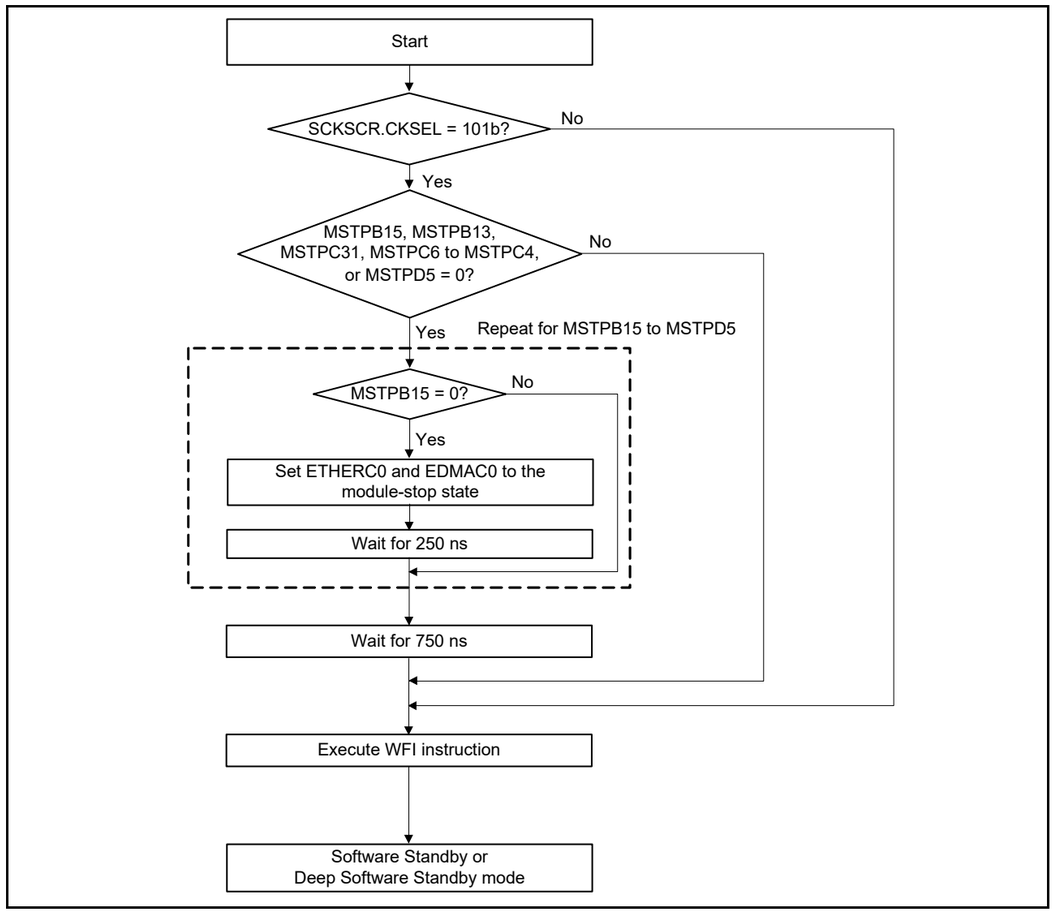


Figure 11.2 Example flow for transition to Software Standby or Deep Software Standby mode

11.7.2 Canceling Software Standby Mode

Software Standby mode is canceled by:

- An available interrupt shown in Table 11.3
- A RES pin reset
- A power-on reset
- A voltage monitor reset
- A reset caused by an IWDT underflow.

On exiting Software Standby, the oscillators that operate before transitioning to the mode restart. After all of these oscillators are stabilized, the MCU returns to Normal mode from Software Standby mode. See section 14.2.9, Wake Up Interrupt Enable Register (WUPEN), for information on waking up the MCU from Software Standby mode.

You can cancel Software Standby mode in any of the following ways:

- Canceling by an interrupt
  When an available interrupt request (see Table 11.3) is generated, all oscillators that were operating before the transition to Software Standby mode restart. After all of these oscillators are stabilized, the MCU cancels Software Standby mode and starts the interrupt handling. When the PLL is selected as the clock source, you must insert wait

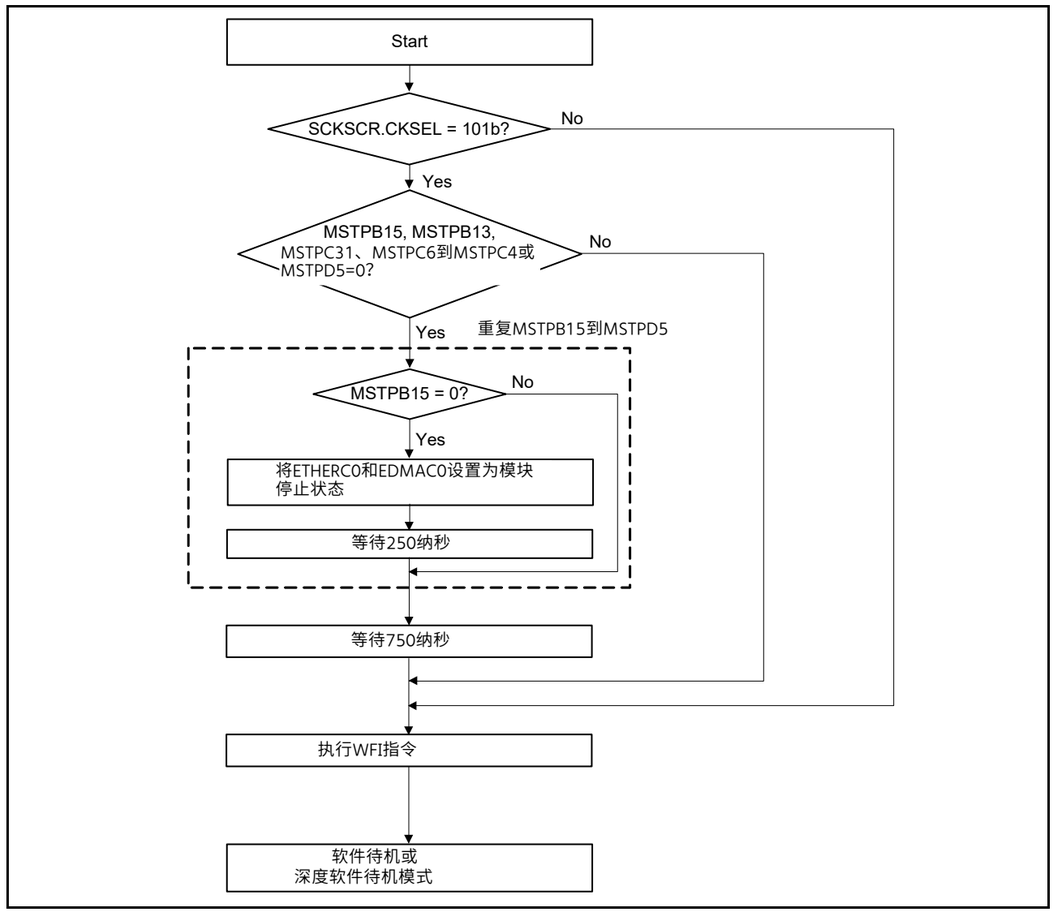


Figure 11.2 转换到软件待机或深度软件待机模式的示例流程

11.7.2 取消软件待机模式

软件待机模式通过以下方式取消：

- 表11.3中显示的可用中断
- ARES引脚复位
- A power-on reset
- 电压监视器复位
- 由IWDT下溢引起的复位。

在退出软件待机时，在转换到模式之前运行的振荡器会重新启动。在所有这些振荡器都稳定后，MCU从软件待机模式返回到正常模式。有关将MCU从软件待机模式唤醒的信息，请参见第14.2.9节，唤醒中断使能寄存器(WUPEN)。

您可以通过以下任一方式取消软件待机模式：

- 通过中断取消
  当产生一个可用的中断请求（见表11.3）时，所有在转换到软件待机模式之前工作的振荡器都会重新启动。在所有这些振荡器都稳定后，MCU取消软件待机模式并开始中断处理。WhenthePLLisselectedastheclocksource youmustinsertwait

time at least 250 ns at the beginning of the interrupt handling. The recommended method to measure the wait time is to do so in software. Be sure to consider the worst-case use conditions to ensure that the required wait time elapses. Figure 11.3 shows an example flow for canceling Software Standby by an interrupt.

- Canceling by RES pin reset
  When the RES pin is driven low, the MCU enters the reset state and the oscillators start operating in their default status. Make sure to keep the RES pin low for the time period specified in section 60, Electrical Characteristics. When the RES pin is driven high after the specified time period, the CPU starts reset exception handling.
- Canceling by a power-on reset
  Software Standby mode is canceled by a power-on reset and the MCU starts the reset exception handling.
- Canceling by a voltage monitor reset
  Software Standby mode is canceled by a voltage monitor reset from the voltage detection circuit and the MCU starts the reset exception handling.
- Canceling by IWDT reset
  Software Standby mode is canceled by an internal reset generated by an IWDT underflow, and the MCU starts reset exception handling. However, the IWDT stops in Software Standby mode and an internal reset for canceling Software Standby mode is not generated in the following conditions:
  - OFS0.IWDTSTRT = 0 and OFS0.IWDTSTPCTL = 1.
- Canceling by other resets available in Software Standby mode
  Software Standby mode is canceled by the associated resets, and the MCU starts reset exception handling.

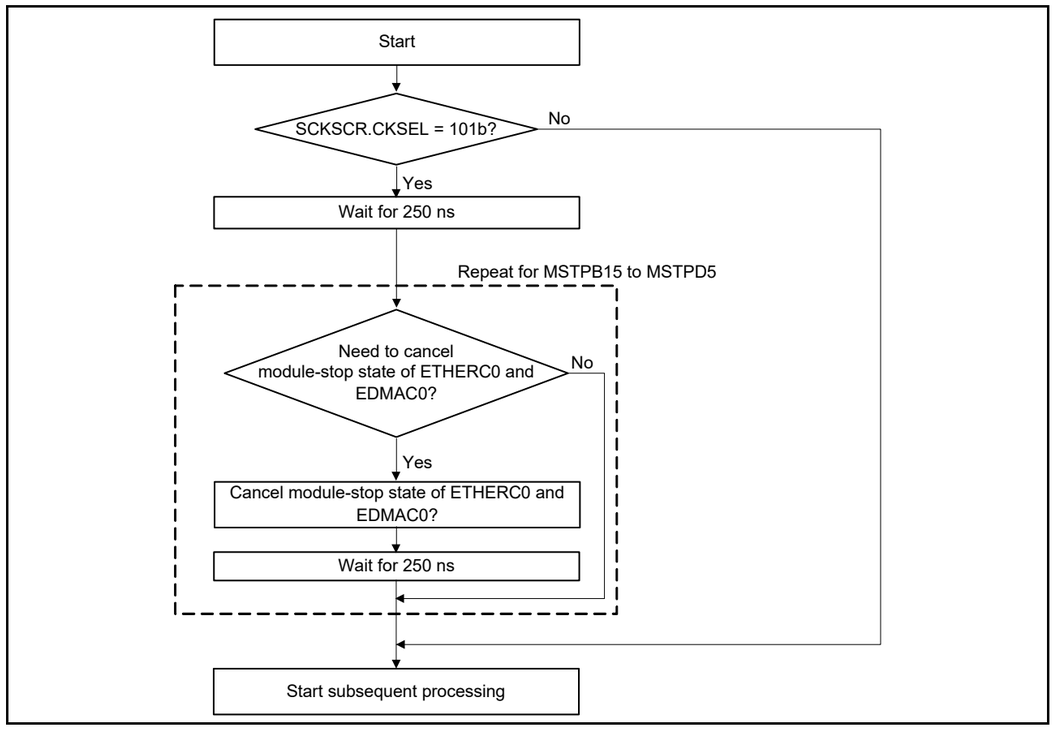


Figure 11.3 Example flow for canceling Software Standby mode

11.7.3 Example of Software Standby Mode Application

Figure 11.4 shows an example of entry to Software Standby mode on detection of a falling edge of the IRQn pin, and exit from Software Standby mode on a rising edge of the IRQn pin. In this example, an IRQn pin interrupt is accepted when the IRQCRi.IRQMD[1:0] bits of the ICU are set to 01b (falling edge) in Normal mode, and then set to 10b (rising edge).

在中断处理的开始时间至少250ns。测量等待时间的推荐方法是在软件中进行。请务必考虑最坏的使用条件，以确保经过所需的等待时间。图11.3显示了通过中断取消软件待机的示例流程。

- 通过RES引脚复位取消
  当RES引脚驱动为低电平时，MCU进入复位状态，振荡器开始在默认状态下运行。确保在第60节“电气特性”中指定的时间段内保持RES引脚为低电平。当RES引脚在指定时间后被驱动为高电平时，CPU开始复位异常处理。
- 通过上电复位取消
  软件待机模式通过上电复位取消，MCU启动复位异常处理。
- 通过电压监视器复位取消
  软件待机模式通过电压检测电路的电压监视器复位取消，MCU开始复位异常处理。
- 通过IWDT复位取消
  软件待机模式由IWDT下溢产生的内部复位取消，MCU开始复位异常处理。但是，IWDT在软件待机模式下停止，并且在以下情况下不会产生用于取消软件待机模式的内部复位：
  - OFS0.IWDTSTRT = 0 and OFS0.IWDTSTPCTL = 1.
- 通过软件待机模式下可用的其他复位取消
  软件待机模式被相关的复位取消，MCU开始复位异常处理。

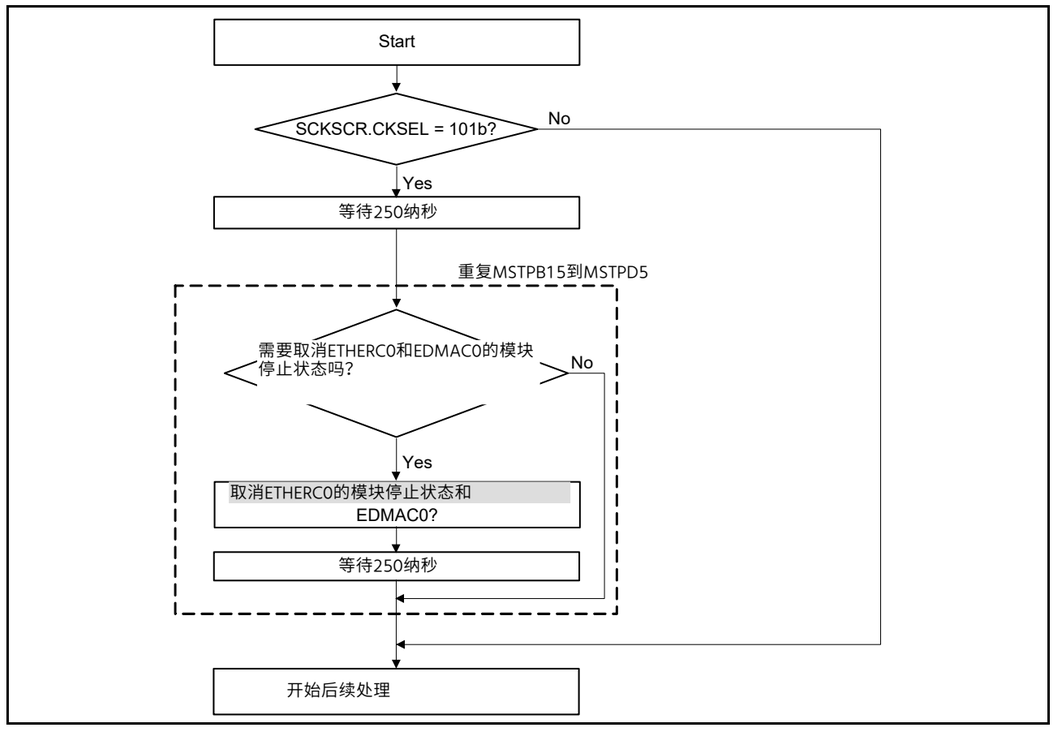


Figure 11.3 取消软件待机模式的示例流程

11.7.3 软件待机模式应用示例

图11.4显示了在检测到IRQn引脚的下降沿进入软件待机模式并在IRQn引脚的上升沿退出软件待机模式的示例。在本例中，当ICU的IRQCRi.IRQMD[1:0]位在正常模式下设置为01b（下降沿），然后设置为10b（上升沿）时，将接受IRQn引脚中断。

Next, the SBYCR.SSBY bit is set to 1 and a WFI instruction is executed. As a result, entry to Software Standby mode completes, and exit from Software Standby mode is initiated by a rising edge of the IRQn pin.

Setting the ICU is also required to exit Software Standby mode. For details, see section 14, Interrupt Controller Unit (ICU). The oscillation stabilization time in Figure 11.4 is specified in section 60, Electrical Characteristics.

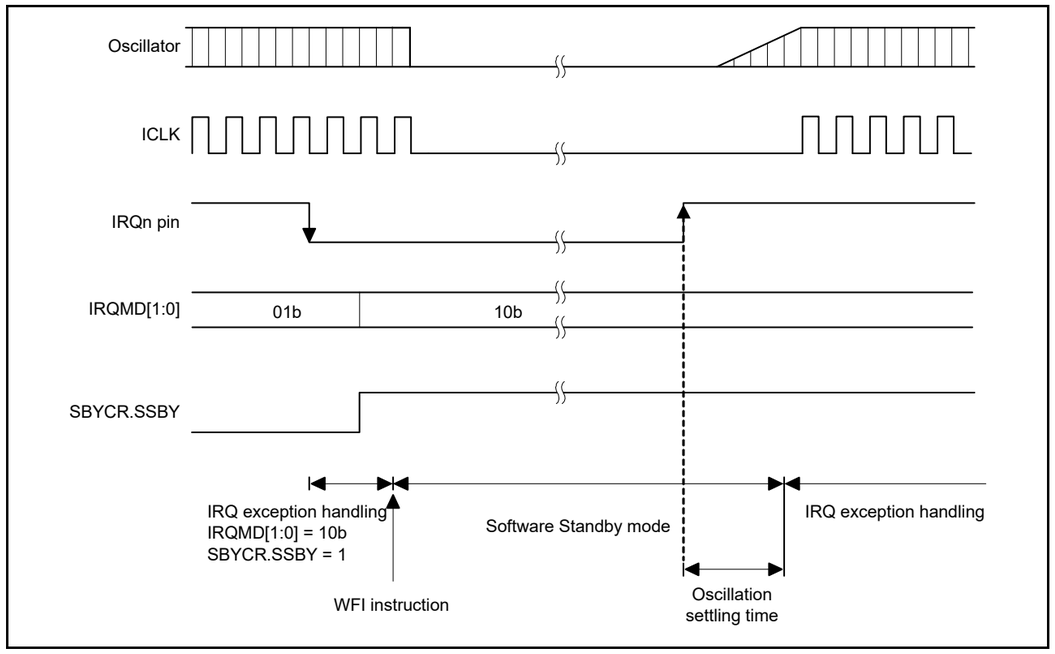


Figure 11.4 Example of Software Standby mode application

11.8 Snooze Mode

11.8.1 Transition to Snooze Mode

Figure 11.5 shows Snooze mode entry configuration. When the Snooze control circuit receives a Snooze request in Software Standby mode, the MCU transitions to Snooze mode. In this mode, some peripheral modules operate without waking up the CPU. Table 11.2 shows the peripheral modules that can operate in Snooze mode. Also, DTC operation can be selected in Snooze mode by setting the SNZCR.SNZDTCEN bit.

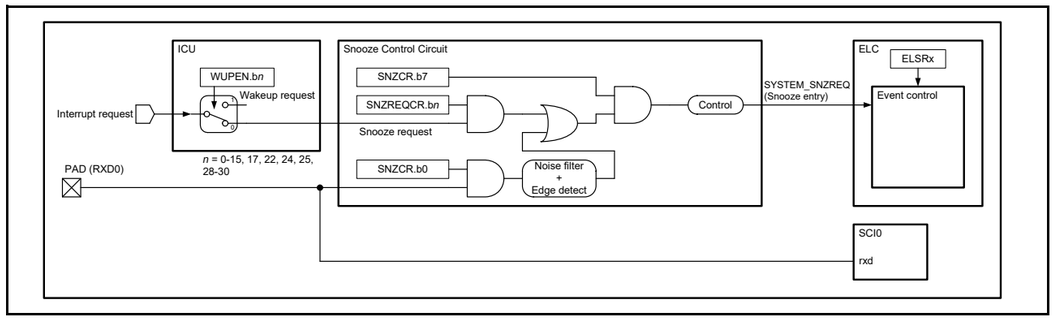


Figure 11.5 Snooze entry configuration

Table 11.7 shows the Snooze requests that switch the MCU from Software Standby to Snooze mode. To use a listed Snooze requests as a trigger to switch to Snooze mode, you must set the associated SNZREQENn bit of the SNZREQCR

接下来，将SBYCR.SSBY位设置为1，并执行WFI指令。结果，进入软件待机模式完成，并且退出软件待机模式由IRQn引脚的上升沿启动。

退出软件待机模式也需要设置ICU。有关详细信息，请参阅第14节，中断控制器单元(ICU)。图11.4中的振荡稳定时间在第60节"电气特性"中指定。

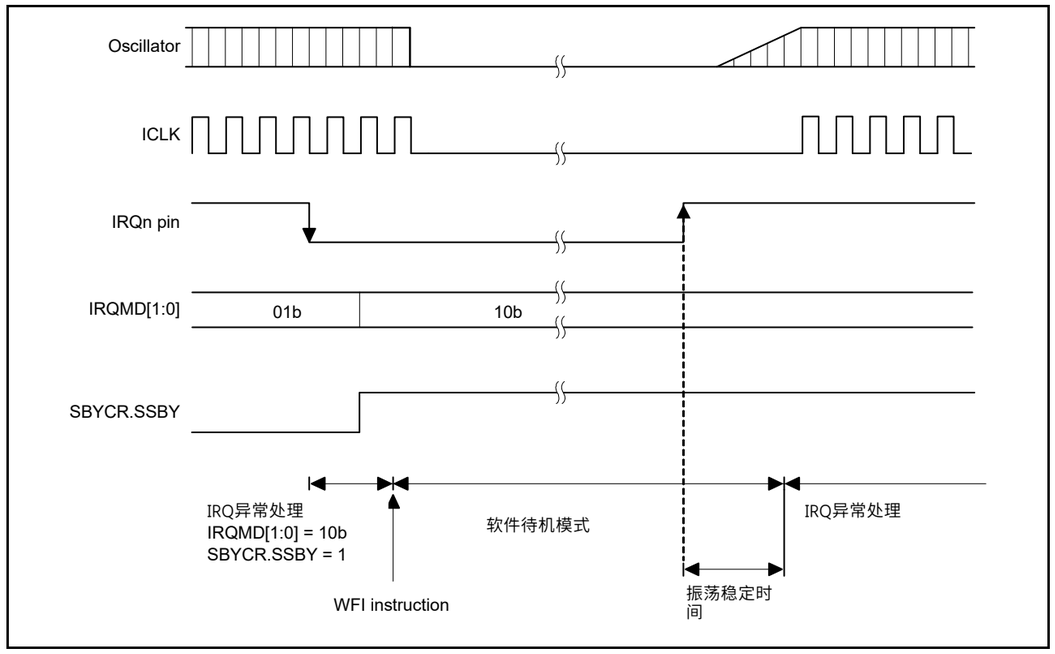


Figure 11.4 软件待机模式应用示例

11.8 贪睡模式

11.8.1 过渡到贪睡模式

图11.5显示了贪睡模式进入配置。当贪睡控制电路接收到贪睡请求时
软件待机模式，MCU转换到贪睡模式。在这种模式下，一些外围模块在不唤醒CPU的情况下运行。表11.2显示了可以在贪睡模式下运行的外围模块。此外，通过设置SNZCR.SNZDTCEN位，可以在贪睡模式下选择DTC操作。

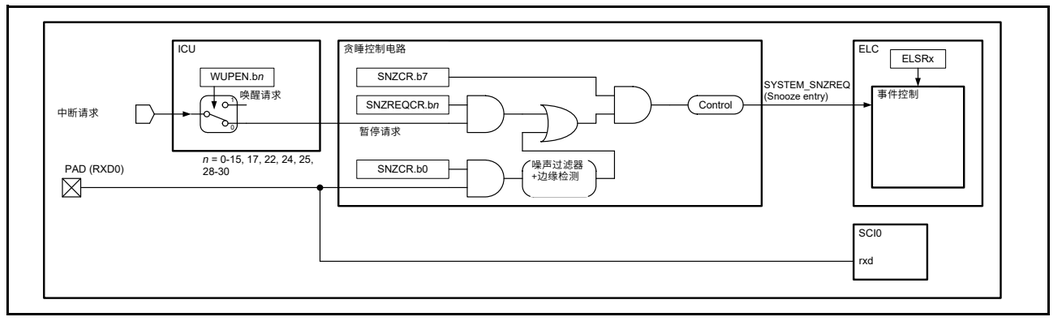


Figure 11.5 贪睡入口配置

表11.7显示了将MCU从软件待机模式切换到贪睡模式的贪睡请求。使用列出的
贪睡请求作为切换到贪睡模式的触发器，您必须设置SNZREQCR的相关SNZREQENn位

register or RXDREQEN bit of the SNZCR register before entering Software Standby mode.

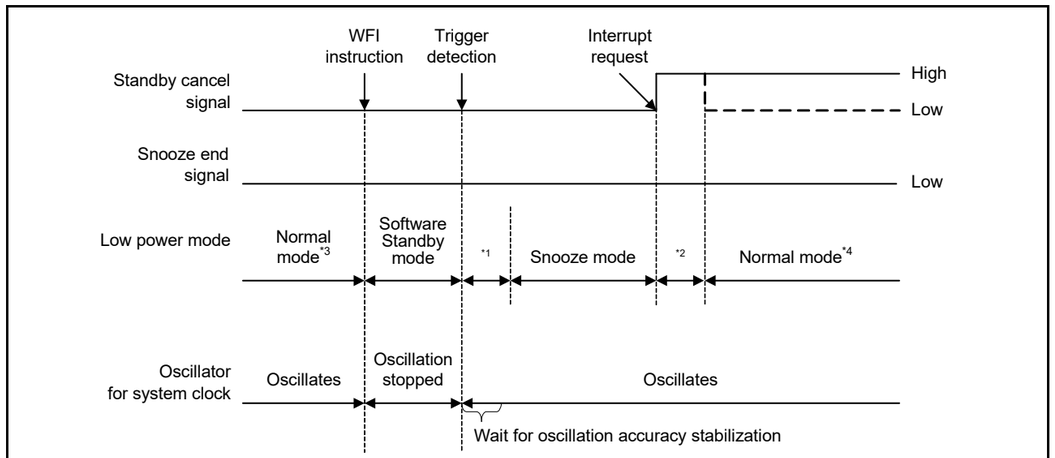
Table 11.7 Available events for invoking Snooze mode

	Control Register	
Snooze request	**Register**	**Bit*1**
PORT_IRQn (n = 0 to 15)	SNZREQCR	SNZREQENn (n = 0 to 15)
KEY_INTKR	SNZREQCR	SNZREQEN17
ACMP_HS0	SNZREQCR	SNZREQEN22
RTC_ALM	SNZREQCR	SNZREQEN24
RTC_PRD	SNZREQCR	SNZREQEN25
AGT1_AGTI	SNZREQCR	SNZREQEN28
AGT1_AGTCMAI	SNZREQCR	SNZREQEN29
AGT1_AGTCMBI	SNZREQCR	SNZREQEN30
RXD0 falling edge	SNZCR	RXDREQEN*2

Note 1. Do not enable multiple Snooze requests at the same time.
Note 2. Do not set the RXDREQEN bit to 1 except in asynchronous mode.

11.8.2 Canceling Snooze Mode

Snooze mode is canceled by any interrupt request that is available in Software Standby mode or any reset. Table 11.3 shows the requests that can be used to exit each mode. On exiting Snooze mode, the MCU transitions to Normal mode and proceeds with exception processing for the given interrupt or reset. An action triggered by the interrupt requests selected in SELSR0 cancels Snooze mode. The interrupt(s) canceling Snooze mode must be selected in IELSRn (n = 0 to 96) to link to the NVIC for the corresponding interrupt handling. See section 14, Interrupt Controller Unit (ICU), for information on setting SELSR0 and IELSRn.



Note 1. Transition time from Software Standby to Snooze mode.
Note 2. Transition time from Snooze mode to Normal mode.
Note 3. Enable Snooze mode (SNZCR.SNZE = 1) immediately before entering to Software Standby mode.
Note 4. You must disable Snooze mode (SNZCR.SNZE = 0) immediately after canceling Snooze mode.

Figure 11.6 Canceling of Snooze mode when an interrupt request signal is generated

11.8.3 Return to Software Standby Mode

Table 11.8 shows the Snooze end requests that can be used as triggers to return to Software Standby mode. The Snooze end requests are available only in Snooze mode. If the requests are generated when the MCU is not in Snooze mode, they are ignored. When multiple requests are selected, each one of the requests invokes transition to Software Standby mode

寄存器或SNZCR寄存器的RXDREQEN位，然后进入软件待机模式。

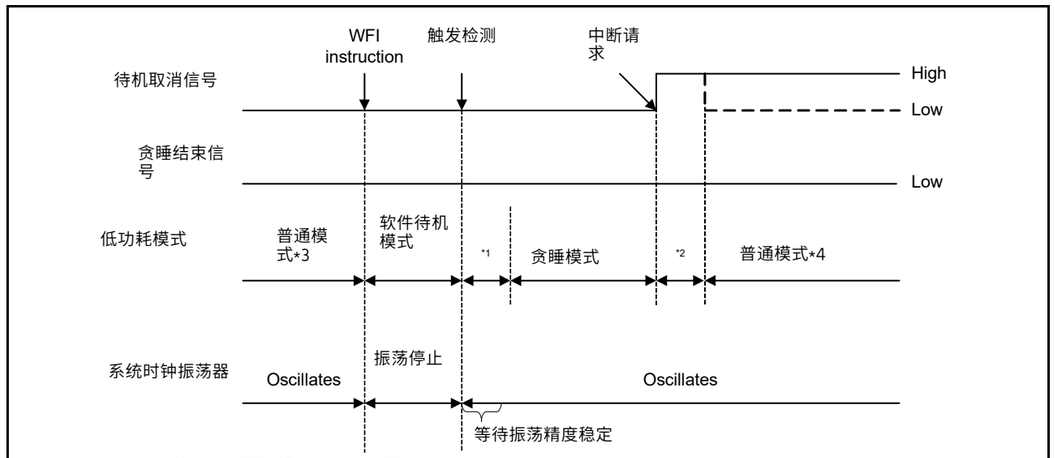
Table 11.7 用于调用贪睡模式的可用事件

	控制寄存器	
暂停请求	**Register**	**Bit*1**
PORT_IRQn (n = 0 to 15)	SNZREQCR	SNZREQENn (n = 0 to 15)
KEY_INTKR	SNZREQCR	SNZREQEN17
ACMP_HS0	SNZREQCR	SNZREQEN22
RTC_ALM	SNZREQCR	SNZREQEN24
RTC_PRD	SNZREQCR	SNZREQEN25
AGT1_AGTI	SNZREQCR	SNZREQEN28
AGT1_AGTCMAI	SNZREQCR	SNZREQEN29
AGT1_AGTCMBI	SNZREQCR	SNZREQEN30
RXD0下降沿	SNZCR	RXDREQEN*2

Note 1. 不要同时启用多个贪睡请求。
Note 2. 除非在异步模式下，否则不要将RXDREQEN位设置为1。

11.8.2 取消贪睡模式

在软件待机模式下可用的任何中断请求或任何复位都会取消贪睡模式。表11.3显示了可用于退出每种模式的请求。在退出贪睡模式时，MCU转换到正常模式并继续进行给定中断或复位的异常处理。由在SELSR0中选择的中断请求触发的动作会取消贪睡模式。必须在IELSRn（n=0到96）中选择取消贪睡模式的中断，以链接到NVIC以进行相应的中断处理。有关设置SELSR0和IELSRn的信息，请参见第14节，中断控制器单元(ICU)。



Note 1. 从软件待机到贪睡模式的转换时间。
Note 2. 从贪睡模式到正常模式的过渡时间。
Note 3. 在进入软件待机模式之前立即启用贪睡模式(SNZCR.SNZE=1)。
Note 4. 您必须在取消贪睡模式后立即禁用贪睡模式(SNZCR.SNZE=0)。

Figure 11.6 产生中断请求信号时取消贪睡模式

11.8.3 返回软件待机模式

表11.8显示了可用作触发器以返回软件待机模式的贪睡结束请求。贪睡结束请求仅在贪睡模式下可用。如果请求是在MCU未处于贪睡模式时生成的，则它们将被忽略。选择多个请求时，每个请求都调用过渡到软件待机模式

from Snooze mode.

Table 11.9 shows the Snooze end conditions that consist of the Snooze end requests and the conditions of the peripheral modules. The CTSU, SCI0, ADC120, ADC121, and DTC modules can keep the MCU in Snooze mode until they complete their operation.

An AGT1 underflow as a trigger to return to Software Standby mode cancels Snooze mode without waiting for the completion of the SCI0 operation.

Figure 11.7 shows the timing diagram for the transition from Snooze mode to Software Standby mode. This mode transition occurs according to which Snooze end requests are set in the SNZEDCR register. A Snooze request is cleared automatically after it is returned to Software Standby mode.

Table 11.8 Available Snooze end requests (triggers to return to Software Standby mode)

Snooze end request	Enable/disable control	
	Register	Bit
AGT1 Unterflow or measurement complete (AGT1_AGTI)	SNZEDCR	b0
DTC transfer completion (DTC_COMPLETE)	SNZEDCR	b1
Not DTC transfer completion (DTC_TRANSFER)	SNZEDCR	b2
ADC120 window A/B compare match (ADC120_WCMPM)	SNZEDCR	b3
ADC120 window A/B compare mismatch (ADC120_WCMPUM)	SNZEDCR	b4
ADC121 window A/B compare match (ADC121_WCMPM)	SNZEDCR	b5
ADC121 window A/B compare mismatch (ADC121_WCMPUM)	SNZEDCR	b6
SCI0 address mismatch (SCI0_DCUF)	SNZEDCR	b7

Table 11.9 Snooze end conditions

Module operating when a Snooze end request occurs	Snooze end request	
	AGT1 underflow	All except AGT1 underflow
DTC	The MCU transitions to Software Standby mode after all of these modules complete operation	The MCU transitions to Software Standby mode after all of these modules complete operation
ADC120		
ADC121		
CTSU		
SCI0	The MCU transitions to Software Standby mode immediately after the Snooze end request is generated	
All other modules	The MCU transitions to Software Standby mode immediately after the Snooze end request is generated	

Note: If the DTC is used to activate the ADC120, ADC121, CTSU, or SCI, the MCU transitions to Software Standby mode immediately after a Snooze end request is generated.

从贪睡模式。

表11.9显示了贪睡结束条件，包括贪睡结束请求和外围模块的条件。CTSU、SCI0、ADC120、ADC121和DTC模块可以使MCU保持在贪睡模式，直到它们完成操作。

AGT1下溢作为返回软件待机模式的触发器会取消贪睡模式，而无需等待SCI0操作完成。

图11.7显示了从贪睡模式转换到软件待机模式的时序图。该模式转换根据SNZEDCR寄存器中设置的贪睡结束请求发生。贪睡请求在返回到软件待机模式后会自动清除。

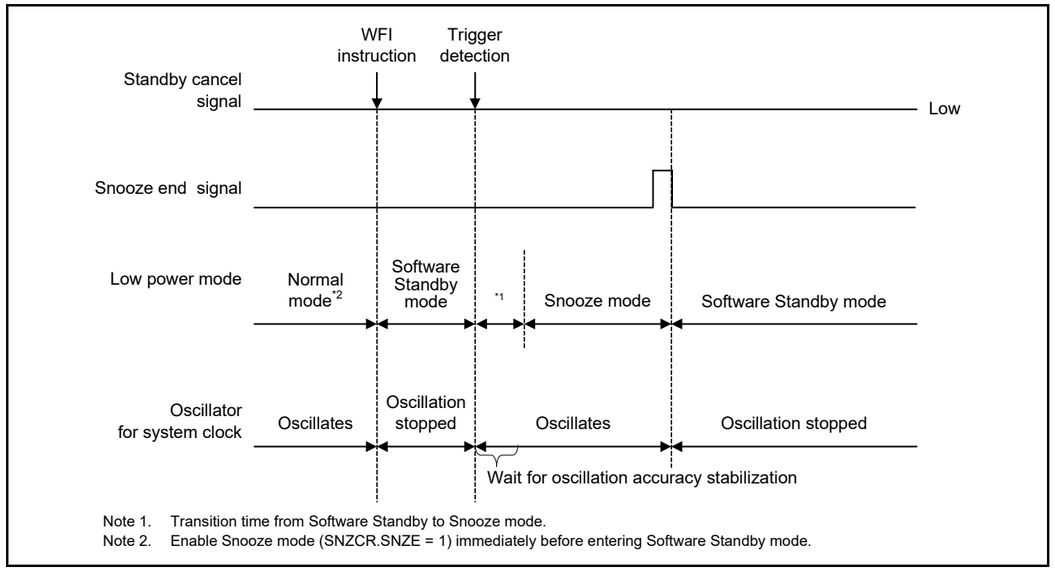
Table 11.8 可用的贪睡结束请求（触发返回到软件待机模式）

暂停结束请求	Enable/disable control	
	Register	Bit
AGT1溢流或测量完成(AGT1_AGTI)	SNZEDCR	b0
DTC传输完成(DTC_COMPLETE)	SNZEDCR	b1
不是DTC传输完成(DTC_TRANSFER)	SNZEDCR	b2
ADC120窗口AB比较匹配(ADC120_WCMPM)	SNZEDCR	b3
ADC120窗口AB比较不匹配(ADC120_WCMPUM)	SNZEDCR	b4
ADC121窗口AB比较匹配(ADC121_WCMPM)	SNZEDCR	b5
ADC121窗口AB比较不匹配(ADC121_WCMPUM)	SNZEDCR	b6
SCI0地址不匹配(SCI0_DCUF)	SNZEDCR	b7

Table 11.9 暂停结束条件

模块运行时 发生暂停结束请求	暂停结束请求	
	AGT1 underflow	所有除AGT1下溢
DTC	在所有这些模块完成操作后，MCU转换到软件待机模式	在所有这些模块完成操作后，MCU转换到软件待机模式
ADC120		
ADC121		
CTSU		
SCI0	产生贪睡结束请求后，MCU立即转换到软件待机模式	
所有其他模块	产生贪睡结束请求后，MCU立即转换到软件待机模式	

Note: 如果DTC用于激活ADC120、ADC121、CTSU或SCI，则MCU在产生贪睡结束请求后立即转换到软件待机模式。

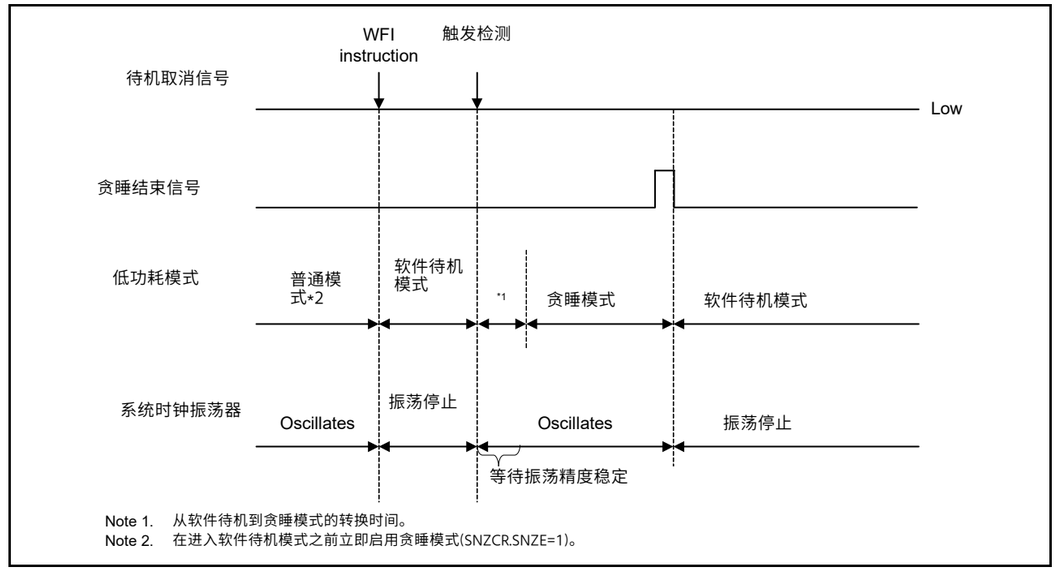


Note 1. Transition time from Software Standby to Snooze mode.
Note 2. Enable Snooze mode (SNZCR.SNZE = 1) immediately before entering Software Standby mode.

Figure 11.7 Canceling of Snooze mode when interrupt request signal is not generated

11.8.4 Snooze Operation Example

Figure 11.8 shows an example setting for using ELC in Snooze mode.



Note 1. 从软件待机到贪睡模式的转换时间。
Note 2. 在进入软件待机模式之前立即启用贪睡模式(SNZCR.SNZE=1)。

Figure 11.7 未产生中断请求信号时取消贪睡模式

11.8.4 贪睡操作示例

图11.8显示了在贪睡模式下使用ELC的示例设置。

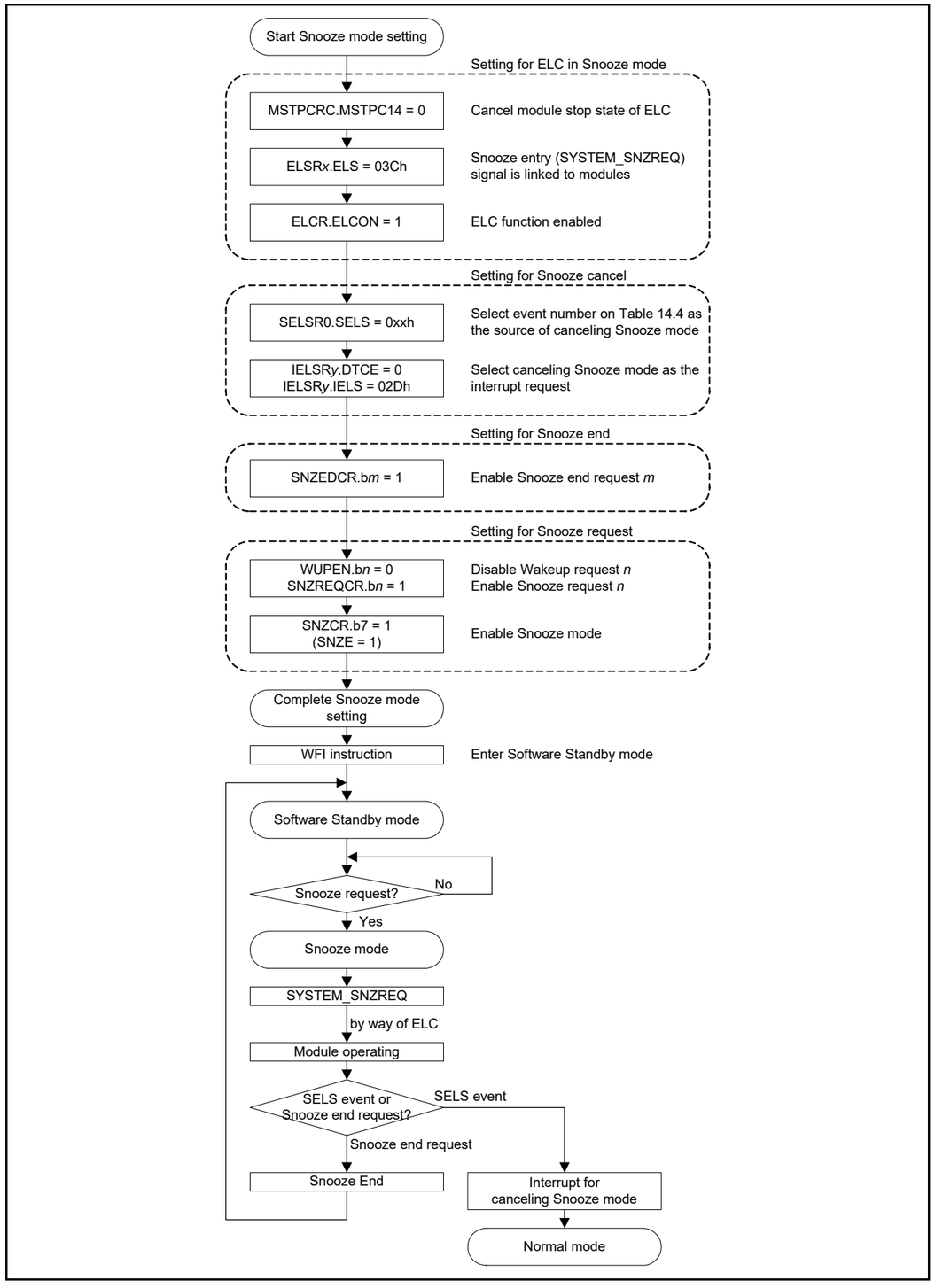


Figure 11.8 Setting example of using ELC in Snooze mode

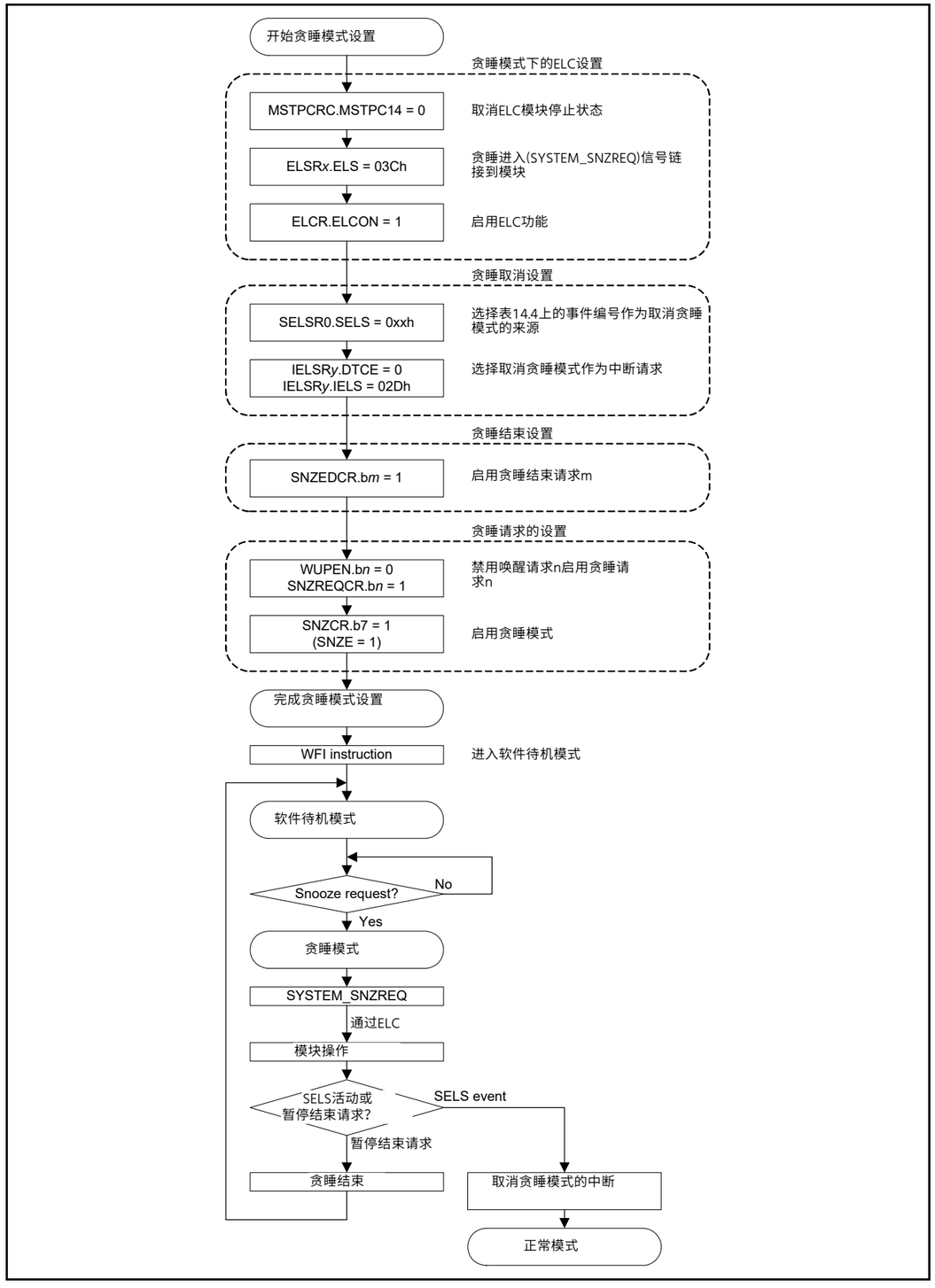


Figure 11.8 在贪睡模式下使用ELC的设置示例

The MCU is capable of data transmission/reception in SCI0 asynchronous mode without CPU intervention. Table 11.10 shows the maximum transfer rate of SCI0 in Snooze mode. When using the SCI0 in Snooze mode use one of the following operating modes: High-speed mode or Low-speed mode.

Do not use Subosc-speed mode.

Table 11.10 HOCO: ± 1.4% (Ta = -20 to 105°C) (Unit: bps)

Maximum division ratio of ICLK, PCLKA, PCLKB, PCLKC, PCLKD, FCLK, BCLK, and TRCLK	HOCO frequency					
	LOCO is not operating			LOCO is operating		
	16 MHz	18 MHz	20 MHz	16 MHz	18 MHz	20 MHz
1	2400			4800		
2						
4						
8						
16	1200			2400		
32						
64						

Figure 11.9 shows an example setting for using SCI0 in Snooze mode entry.

MCU能够在SCI0异步模式下进行数据传输接收，无需CPU干预。表11.10显示了贪睡模式下SCI0的最大传输速率。在贪睡模式下使用SCI0时，请使用以下操作模式之一：高速模式或低速模式。

不要使用Subosc速度模式。

Table 11.10 HOCO: ± 1.4% (Ta = -20 to 105°C) (Unit: bps)

ICLK、PCLKA、PCLKB、PCLKC的最大分频比，PCLKD, FCLK, BCLK, and TRCLK	HOCO frequency					
	LOCO没有运行			LOCO正在运营		
	16 MHz	18 MHz	20 MHz	16 MHz	18 MHz	20 MHz
1	2400			4800		
2						
4						
8						
16	1200			2400		
32						
64						

图11.9显示了在贪睡模式进入中使用SCI0的示例设置。

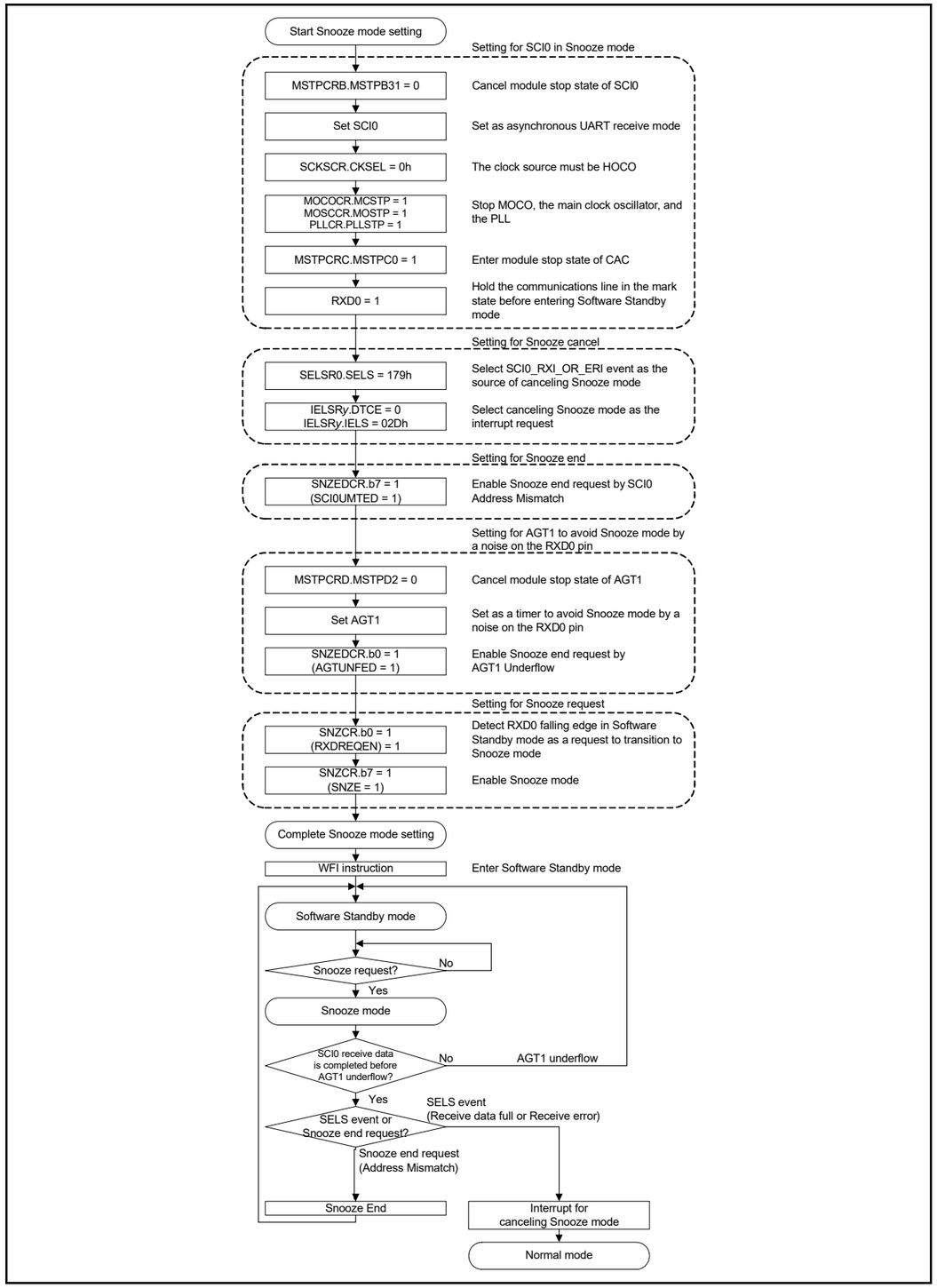


Figure 11.9 Setting example of using SCI0 in Snooze mode entry

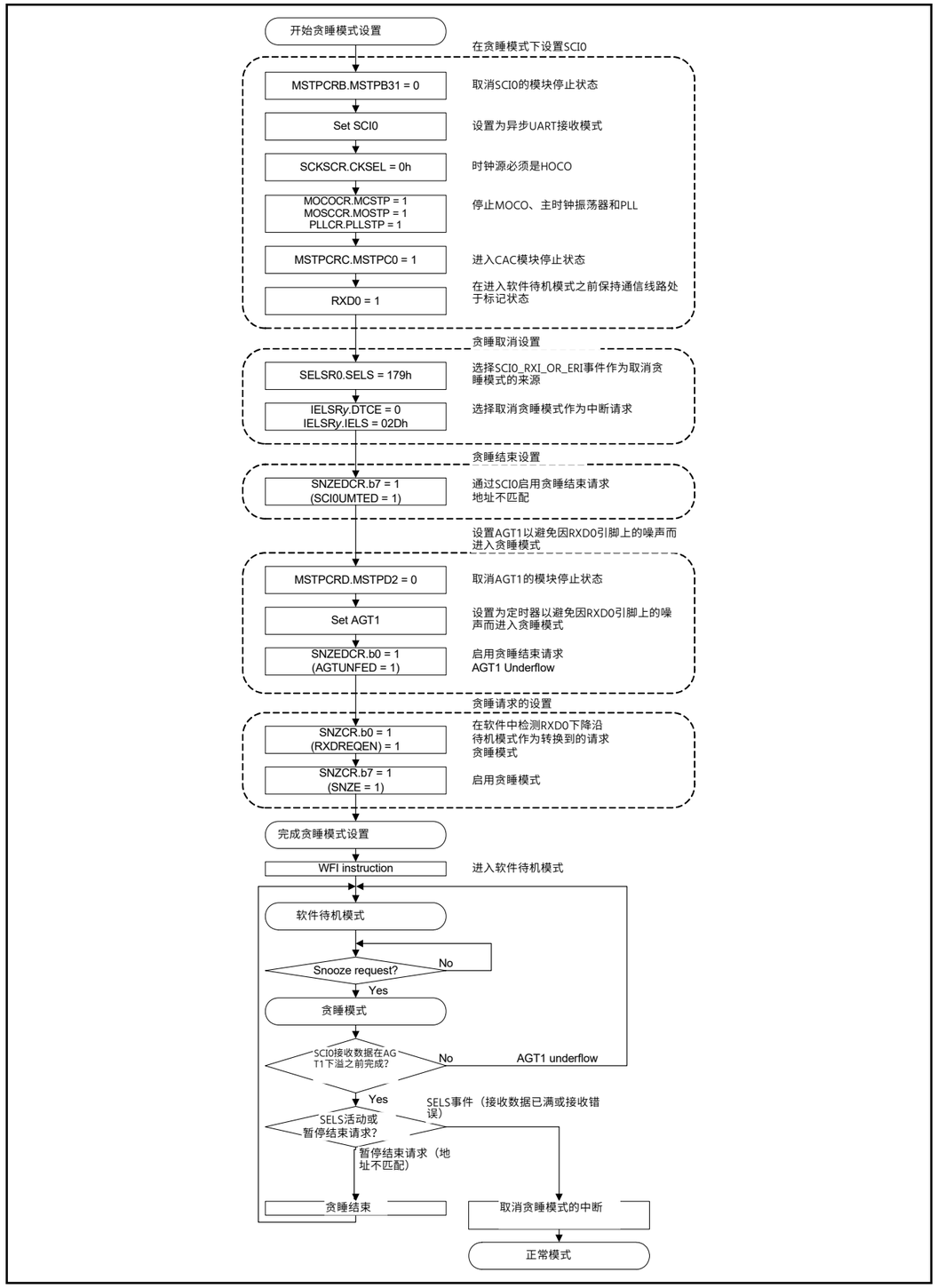


Figure 11.9 在Snooze模式进入使用SCI0的设置示例

11.9 Deep Software Standby Mode

11.9.1 Transition to Deep Software Standby Mode

The MCU enters Deep Software Standby mode when a WFI instruction is executed with the SBYCR.SSBY bit set to 1 and the DPSBYCR.DPSBY bit set to 1. See Table 11.6 for the settings of the related control bits.

In Deep Software Standby mode, the CPU, on-chip peripheral functions except for the RTC alarm, RTC interval, and USB suspend/resume detecting unit, SRAM (not the Standby SRAM), and all oscillators except for the sub-clock oscillator and low-speed on-chip oscillator are stopped. Power consumption is reduced because the internal power supply to these modules is stopped. The contents of all of the CPU registers and internal peripheral modules, except for the RTC alarm, RTC interval, and USB suspend/resume detecting unit, become undefined.

Data in the Standby SRAM is saved if the setting in the DEEPCUT[1:0] bits is 00b. If the setting in the DEEPCUT[1:0] bits is 01b, the internal power supply to the Standby SRAM and the USB resume detecting unit is cut off, and power consumption is reduced. Data in the Standby SRAM becomes undefined at this time.

If the setting in the DEEPCUT[1:0] bits is 11b, the internal power supply to the Standby SRAM and the USB resume detecting unit is cut off, the LVD is stopped, and the low power mode function of the power-on reset circuit is enabled. Therefore, power consumption is further reduced. For details, see section 60, Electrical Characteristics.

When the MCU enters Deep Software Standby mode while the IWDT is in auto start mode and the OFS0.IWDTSTPCTL bit is 1, power supply to the IWDT-dedicated clock and the IWDT is cut off. Counting by the IWDT also stops.

When the OFS0.IWDTSTPCTL bit is 0, the MCU enters Software Standby mode instead of Deep Software Standby mode, regardless of the setting in the OFS0.IWDTSTRT or DPSBYCR.DPSBY bit. When the OFS0.IWDTSTPCTL bit is 0 while the OFS0.IWDTSTRT bit is 0 (auto start mode), the IWDT-dedicated clock and IWDT continue operation.

When the LVD1CR0.RI bit is 1 (selecting the voltage monitor 1 reset) or the LVD2CR0.RI bit is 1 (selecting the voltage monitor 2 reset), the MCU enters Software Standby mode instead of Deep Software Standby mode. The I/O port states are the same as in Software Standby mode.

When the PLL is selected as the clock source, set the following modules into the module-stop state before executing a WFI instruction: ETHERC, EPTPC, EDMAC, SCE7, DRW, JPEG, GLCDC, GPT32EH, GPT32E. In this case, you must also insert wait time at least 750 ns before executing the WFI instruction. The recommended method to measure the wait time is to do so in software. Be sure to consider the worst-case use conditions to ensure that the required wait time elapses.

Figure 11.2 shows an example flow for transitioning to Software Standby or Deep Software Standby mode.

Note 1. Conditions on the DTC, DMAC, and IWDT for transition to Software Standby mode must be met before the WFI instruction is executed. For details, see section 11.7, Software Standby Mode.

11.9.2 Canceling Deep Software Standby Mode

Deep Software Standby mode is canceled by the interrupts shown in Table 11.3, a RES pin reset, a power-on reset, or a voltage monitor 0 reset. The operations are as follows:

1. Canceling by an interrupt
   Canceling by interrupts is controlled by DPSIERn (n = 0 to 3) and DPSIFRn (n = 0 to 3). When an available interrupt request is generated, the associated flag in DPSIFRn is set to 1. If the interrupt is enabled in DPSIERn, Deep Software Standby mode is canceled. Rising or falling edge detection can be selected in DPSIEGRn (n = 0 to 2). The detection edge can be selected for the NMI, IRQ0-DS to IRQ14-DS, voltage monitor 1, and voltage monitor 2 interrupts. When a Deep Software Standby mode canceling request occurs, internal power is supplied, the MOCO clock starts to oscillate, and then an internal reset (Deep Software Standby reset) is generated for the entire MCU. The stable MOCO clock is supplied to the entire MCU and Deep Software Standby reset is canceled. The MCU starts reset exception handling.
   When Deep Software Standby mode is canceled by an external interrupt pin or internal interrupt signal, the RSTSR0.DPSRSTF flag is set to 1.

11.9 深度软件待机模式

11.9.1 过渡到深度软件待机模式

当SBYCR.SSBY位设置为1且DPSBYCR.DPSBY位设置为1时执行WFI指令，MCU进入深度软件待机模式。相关控制位设置见表11.6。

在深度软件待机模式下，除了RTC警报、RTC间隔和
USB挂起恢复检测单元、SRAM（不是StandbySRAM）以及除副时钟振荡器和低速片内振荡器之外的所有振荡器都停止。由于停止了对这些模块的内部供电，因此降低了功耗。除了RTC警报、RTC间隔和USB挂起恢复检测单元之外，所有CPU寄存器和内部外围模块的内容都未定义。

如果DEEPCUT[1:0]位的设置为00b，则保存备用SRAM中的数据。如果DEEPCUT[1:0]位设置为01b，则内部对StandbySRAM和USB恢复检测单元的供电将被切断，从而降低功耗。此时备用SRAM中的数据变为未定义。

如果DEEPCUT[1:0]位设置为11b，则内部对StandbySRAM和USB恢复检测单元的供电被切断，LVD停止，上电复位的低功耗模式功能电路启用。因此，进一步降低了功耗。有关详细信息，请参见第60节，电气特性。

当MCU在IWDT处于自动启动模式且OFS0.IWDTSTPCTL位为1时进入深度软件待机模式时，IWDT专用时钟和IWDT的电源将被切断。IWDT的计数也停止。

当OFS0.IWDTSTPCTL位为0时，MCU进入软件待机模式而不是深度软件待机模式，无论OFS0.IWDTSTRT或DPSBYCR.DPSBY位的设置如何。当OFS0.IWDTSTPCTL位为0而OFS0.IWDTSTRT位为0（自动启动模式）时，IWDT专用时钟和IWDT继续运行。

当LVD1CR0.RI位为1（选择电压监控1复位）或LVD2CR0.RI位为1（选择电压监控2复位）时，MCU进入软件待机模式而不是深度软件待机模式。IO端口状态与软件待机模式相同。

WhenthePLLisselectedastheclocksource setthefollowingmodulesintothemodule-stopstatebeforeexecutinga
WFI指令：ETHERC、EPPTC、EDMAC、SCE7、DRW、JPEG、GLCDC、GPT32EH、GPT32E。在这种情况下，您还必须在执行WFI指令之前插入至少750ns的等待时间。测量等待时间的推荐方法是在软件中进行。请务必考虑最坏的使用条件，以确保经过所需的等待时间。

图11.2显示了转换到软件待机或深度软件待机模式的示例流程。

注1.在执行WFI指令之前，必须满足DTC、DMAC和IWDT转换到软件待机模式的条件。有关详细信息，请参阅第11.7节，软件待机模式。

11.9.2 取消深度软件待机模式

深度软件待机模式由表11.3中所示的中断、RES引脚复位、上电复位或电压监视器0复位取消。操作如下：

1. 通过中断取消
   中断取消由DPSIERn(n=0到3)和DPSIFRn(n=0到3)控制。当产生可用中断请求时，DPSIFRn中的相关标志设置为1。如果在DPSIERn中使能中断，则取消深度软件待机模式。上升沿或下降沿检测可以在DPSIEGRn(n=0到2)中选择。可以为NMI、IRQ0-DS至IRQ14-DS、电压监视器1和电压监视器2中断选择检测沿。当产生深度软件待机模式取消请求时，内部供电，MOCO时钟开始振荡，然后对整个MCU产生内部复位（深度软件待机复位）。为整个MCU提供稳定的MOCO时钟，并取消深度软件待机复位。MCU开始复位异常处理。
   当深度软件待机模式被外部中断引脚或内部中断信号取消时，
   RSTSR0.DPSRSTF标志设置为1。

2. Canceling by RES pin reset
When the RES pin is driven low, the MCU cancels Deep Software Standby mode and enters a reset state. Make sure to keep the RES pin low for the time period specified in section 60, Electrical Characteristics. When the RES pin is driven high after the specified time period, the CPU starts reset exception handling.
3. Canceling by power-on reset
Deep Software Standby mode is canceled by a power-on reset, and the MCU starts reset exception handling.
4. Canceling by voltage monitor 0 reset
Deep Software Standby mode is canceled by a voltage monitor 0 reset from the voltage detection circuit, and the MCU starts reset exception handling.

11.9.3 Pin States when Deep Software Standby Mode is Canceled

In Deep Software Standby mode, the I/O ports retain the same states from Software Standby mode. The MCU is initialized by an internal reset generated when Deep Software Standby mode is canceled, and reset exception handling starts immediately. The DPSBYCR.IOKEEP bit setting determines whether to initialize the I/O ports or to retain the I/O ports states for Software Standby mode. The following is the state of the I/O ports for each bit setting:

- When the DPSBYCR.IOKEEP bit = 0
The I/O ports are initialized by an internal reset generated when Deep Software Standby mode is canceled.
- When the DPSBYCR.IOKEEP bit = 1
Although the MCU is initialized by an internal reset generated when Deep Software Standby mode is canceled, the I/O ports retain their states from Software Standby mode regardless of the MCU internal state. The I/O ports states remain unchanged from Software Standby mode even when settings are made to the I/O ports or peripheral modules. The retained I/O ports states are released by clearing the DPSBYCR.IOKEEP bit to 0, and the MCU operates in accordance with the internal state. The DPSBYCR.IOKEEP bit is not initialized by any internal reset generated when Deep Software Standby mode is canceled.

11.9.4 Example of Deep Software Standby Mode Application

(1) Entering and exiting Deep Software Standby mode

Figure 11.10 shows an example transition to Deep Software Standby mode on the falling edge of the IRQn-DS pin, and an exit from Deep Software Standby mode on the rising edge of the IRQn-DS pin. In this example, an IRQn interrupt is accepted with the IRQCRi.IRQMD[1:0] bits of the ICU set to 01b (falling edge). After the DPSIEGRy.DIRQnEG bit (y = 0, 1 and n = 0 to 14) is set to 1 (rising edge) and the SBYCR.SSBY and DPSBYCR.DPSBY bits are both set to 1, the WFI instruction is executed. As a result, the MCU transitions to Deep Software Standby mode. Deep Software Standby mode is then canceled on the rising edge of the IRQn-DS pin.

2. 通过RES引脚复位取消
当RES引脚被驱动为低电平时，MCU取消深度软件待机模式并进入复位状态。确保在第60节“电气特性”中指定的时间段内保持RES引脚为低电平。当RES引脚在指定时间后被驱动为高电平时，CPU开始复位异常处理。
3. 通过上电复位取消
深度软件待机模式通过上电复位取消，MCU开始复位异常处理。
4. 通过电压监视器0复位取消深度软件待机模式通过电压检测电路的电压监视器0复位取消，并且

MCU开始复位异常处理。

11.9.3 取消深度软件待机模式时的引脚状态

在深度软件待机模式下，IO端口保持与软件待机模式相同的状态。MCU通过取消深度软件待机模式时产生的内部复位进行初始化，并立即开始复位异常处理。DPSBYCR.IOKEEP位设置确定是初始化IO端口还是保留软件待机模式下的IO端口状态。以下是每个位设置的IO端口状态：

- 当DPSBYCR.IOKEEP位=0
IO端口由取消深度软件待机模式时产生的内部复位进行初始化。
- 当DPSBYCR.IOKEEP位=1
虽然MCU由取消深度软件待机模式时产生的内部复位来初始化，但无论MCU内部状态如何，IO端口仍会保持软件待机模式下的状态。即使对IO端口或外围模块进行了设置，IO端口状态在软件待机模式下也保持不变。通过将DPSBYCR.IOKEEP位清0来释放保留的IO端口状态，MCU按照内部状态运行。DPSBYCR.IOKEEP位不会被取消深度软件待机模式时产生的任何内部复位初始化。

11.9.4 深度软件待机模式应用示例

(1) 进入和退出深度软件待机模式

图11.10显示了在IRQn-DS引脚的下降沿转换到深度软件待机模式的示例，以及在IRQn-DS引脚的上升沿退出深度软件待机模式的示例。在此示例中，接受IRQn中断，同时ICU的IRQCRi.IRQMD[1:0]位设置为01b（下降沿）。在DPSIEGRy.DIRQnEG位（y=0、1和n=0到14）设置为1（上升沿）并且SBYCR.SSBY和DPSBYCR.DPSBY位都设置为1后，执行WFI指令。结果，MCU转换到深度软件待机模式。然后在IRQn-DS引脚的上升沿取消深度软件待机模式。

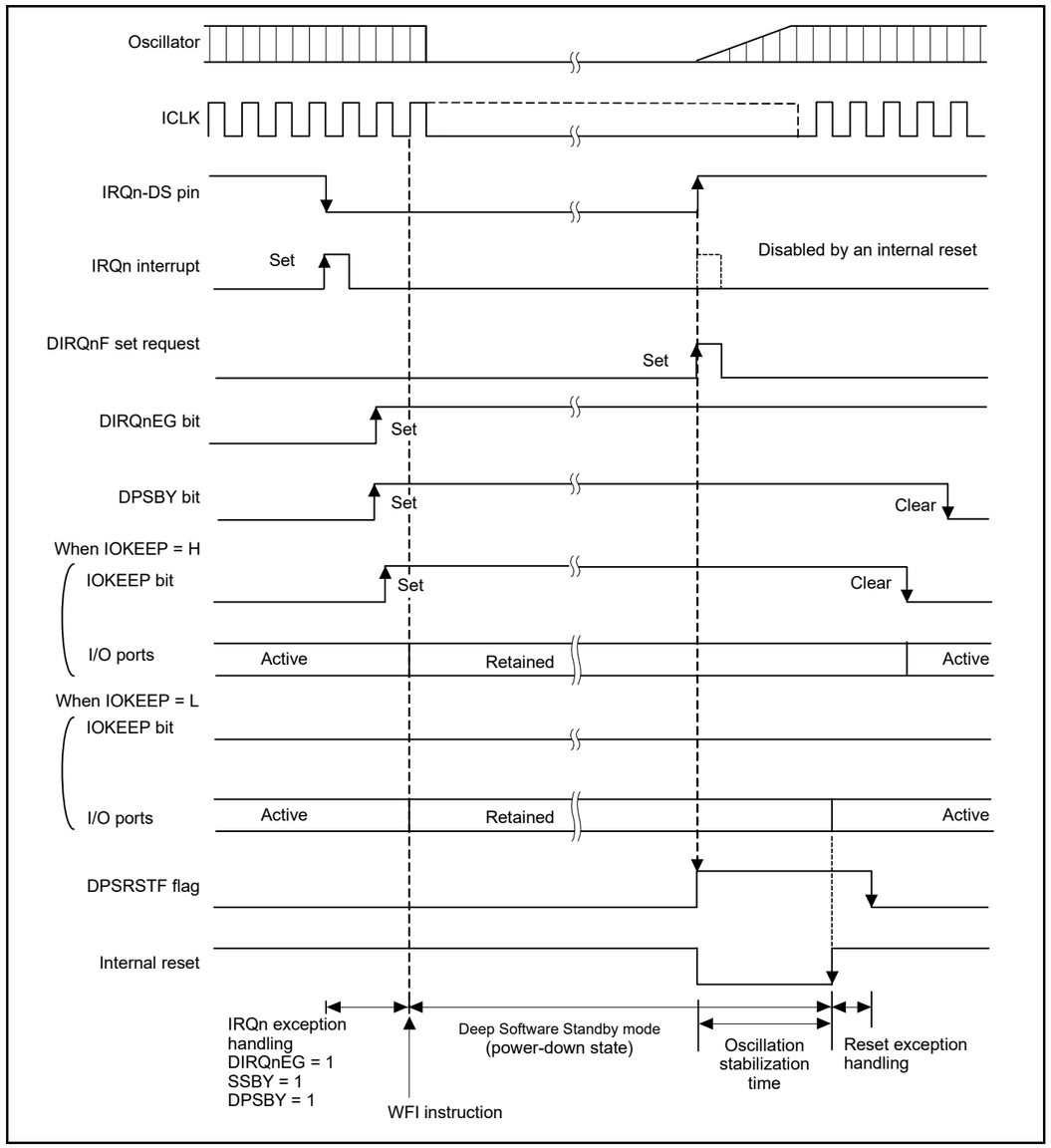


Figure 11.10 Example of Deep Software Standby mode application

11.9.5 Usage Flow for Deep Software Standby Mode

Figure 11.11 shows an example flow for using Deep Software Standby mode. In this example, the RSTSR0.DPSRSTF flag of the reset function is read after reset exception handling to determine whether the reset was generated by the RES pin or by the cancellation of Deep Software Standby mode. For a reset by the RES pin, the MCU transitions to Deep Software Standby mode after the required register settings are made. For a reset by the cancellation of Deep Software Standby mode, the DPSBYCR.IOKEEP bit clears to 0 after the I/O port settings are made.

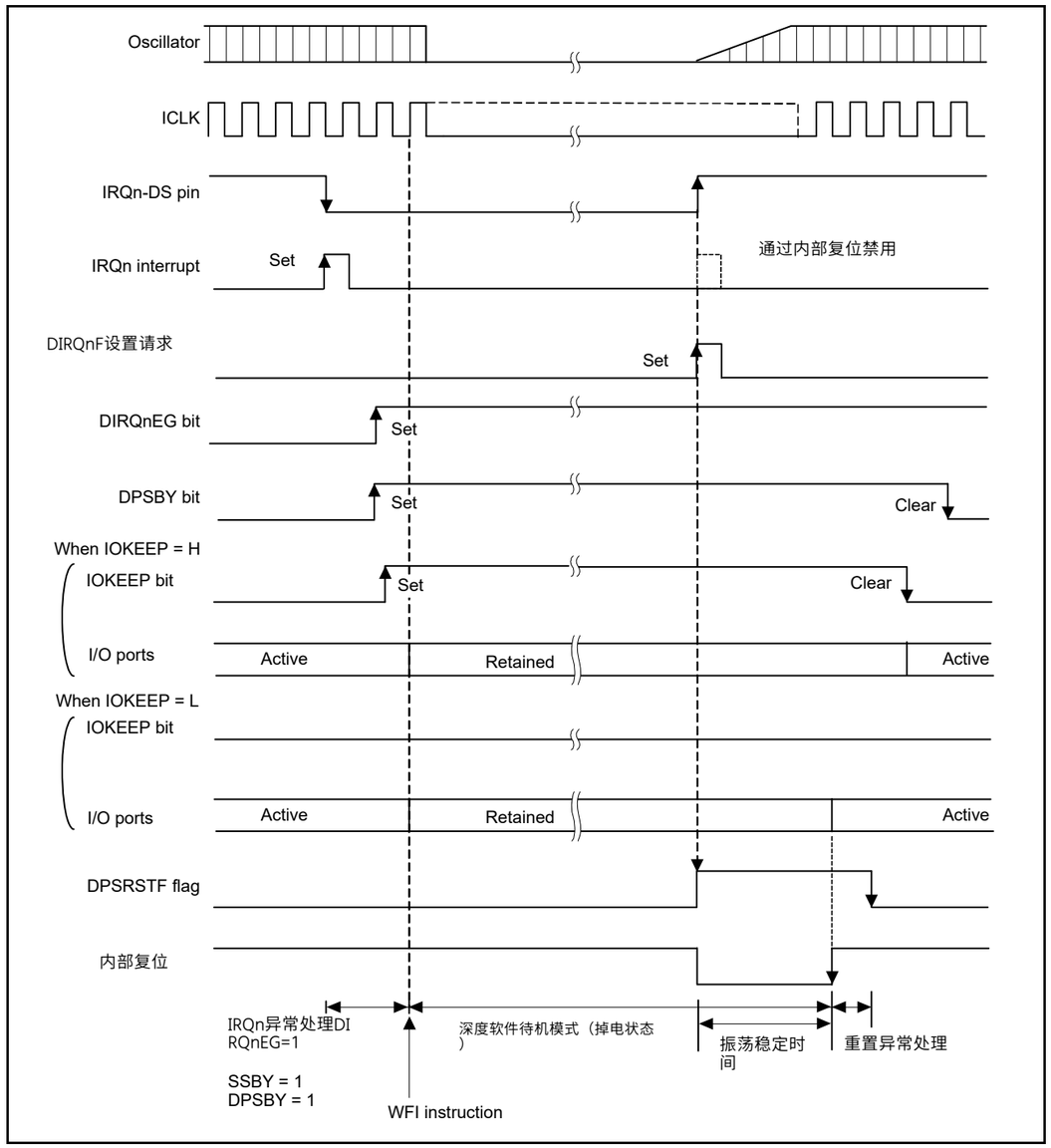


Figure 11.10 深度软件待机模式应用示例

11.9.5 深度软件待机模式的使用流程

图11.11显示了使用深度软件待机模式的示例流程。在本例中，复位功能的RSTSR0.DPRSTF标志在复位异常处理后被读取，以确定复位是由RES引脚产生还是由深度软件待机模式的取消产生。对于通过RES引脚进行的复位，在进行所需的寄存器设置后，MCU会转换到深度软件待机模式。通过取消DeepSoftware进行重置

待机模式下，在IO端口设置完成后DPSBYCR.IOKEEP位清0。

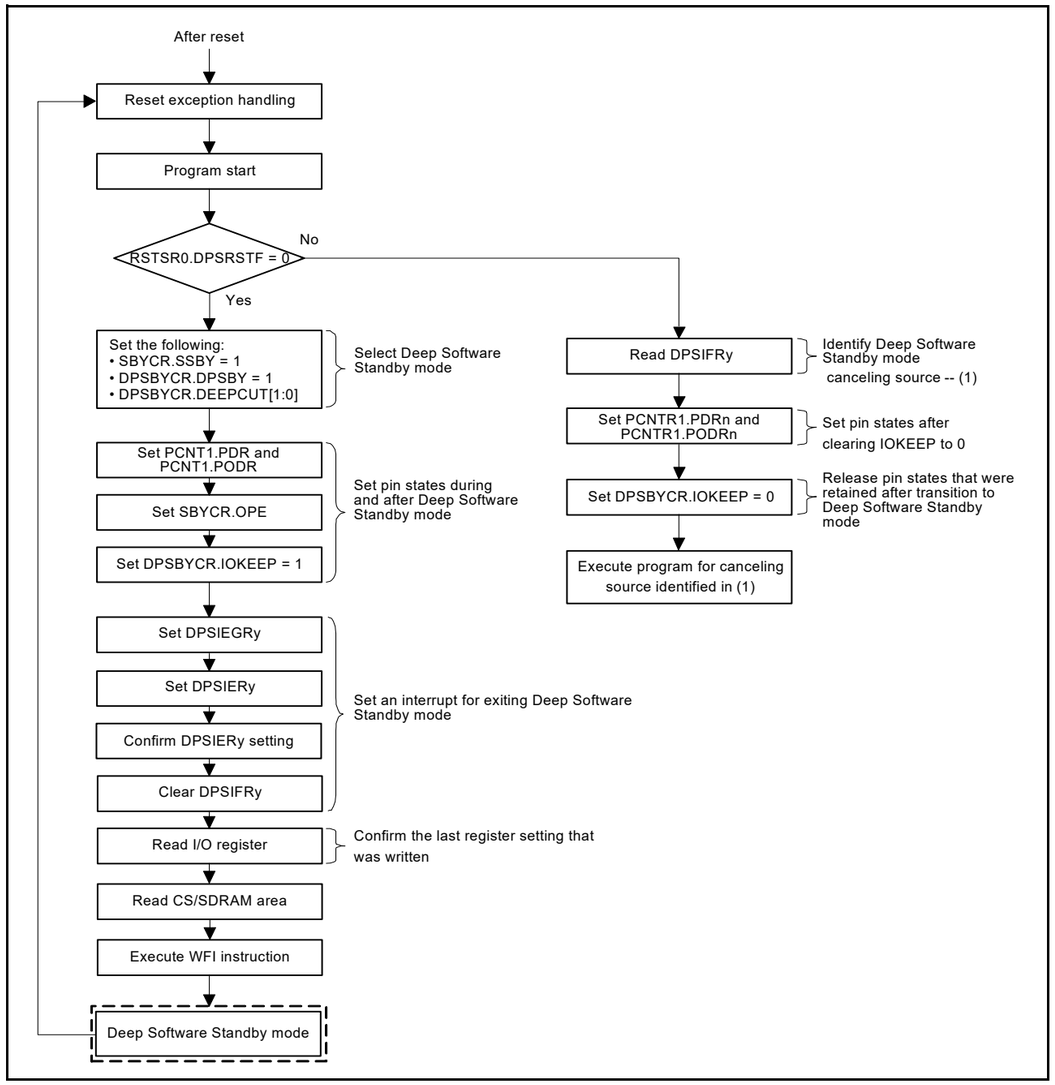


Figure 11.11 Example flow for use of Deep Software Standby mode

11.10 Usage Notes

11.10.1 Register Access

(1) Invalid register write accesses during specific modes or transitions

Do not write to registers listed in this section under any of the listed conditions.

[Registers]

- All registers with a peripheral name of “SYSTEM”.

[Conditions]

- OPCCR.OPCMTSF = 1 or SOPCCR.SOPCMTSF = 1 (during transition of the operating power control mode)

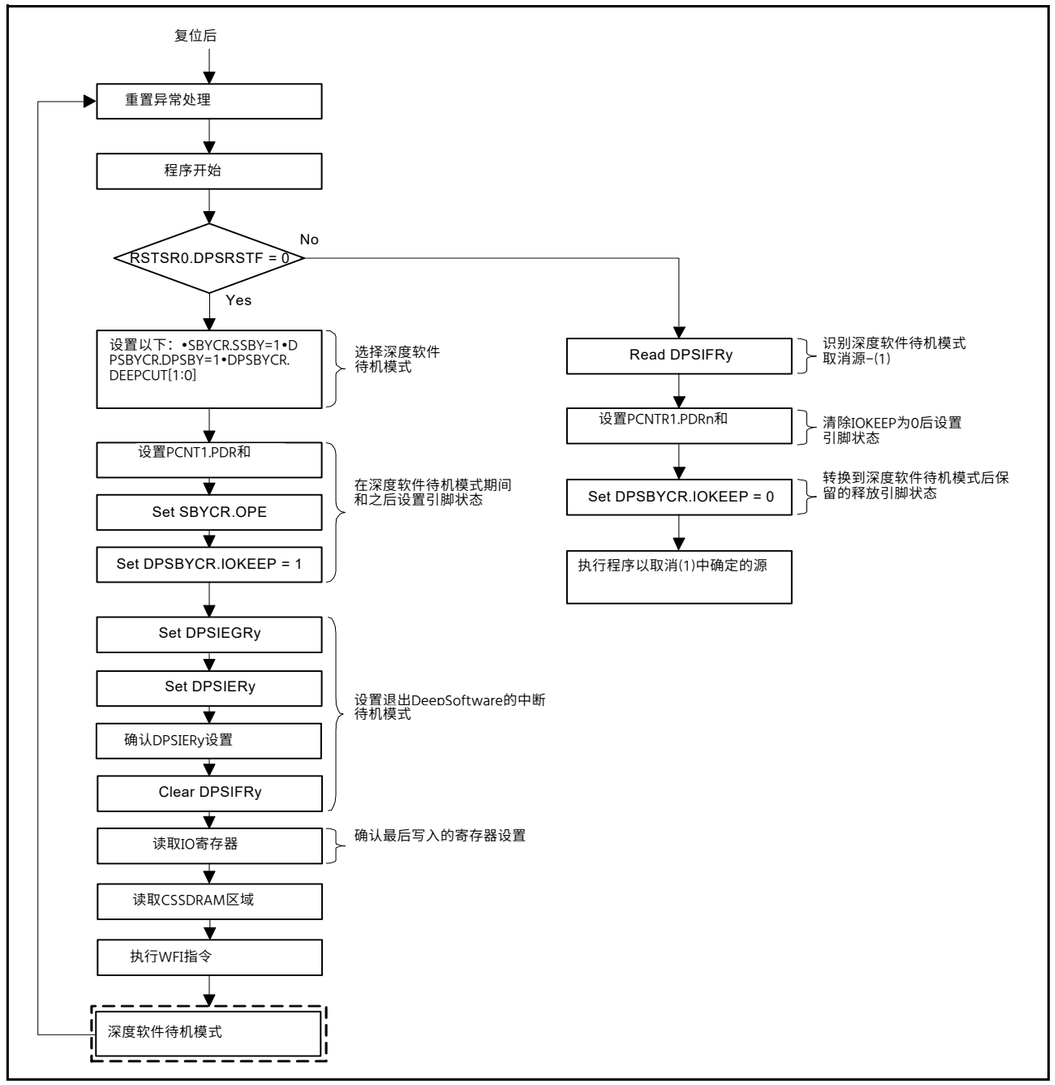


Figure 11.11 使用深度软件待机模式的示例流程

11.10 使用说明

11.10.1 注册访问

(1) 特定模式或转换期间的无效寄存器写访问

不要在任何列出的条件下写入本节中列出的寄存器。

[Registers]

- 外设名称为“SYSTEM”的所有寄存器。

[Conditions]

- OPCCR.OPCMTSF=1或SOPCCR.SOPCMTSF=1（在工作功率控制模式转换期间）

- During time period from executing a WFI instruction to returning to Normal mode
- When FENTRYR.FENTRYi = 1 (i = 0 to 3) (flash P/E mode) or FENTRYR.FENTRYD = 1 (data flash P/E mode).

(2) Valid settings for the clock-related registers

Table 11.11 and Table 11.12 show the valid settings of the clock-related registers in each operating power control mode. Do not write any value other than the valid setting. Any other written value is ignored. Each register has certain prohibited settings under conditions other than those related to the operating power control modes. See section 9, Clock Generation Circuit, for these other conditions for each register.

Table 11.11 Valid settings for the clock-related registers (1)

Mode	Valid settings							
	SCKSCR.CKSEL[2:0], CKOCR.CKOSEL[2:0]	SCKDIVCR.FCK[2:0], ICK[2:0]	PLLCR.PLLSTP	HOCOCR. HCSTP	MOCOCR. MCSTP	LOCOCR. LCSTP	MOSCCR. MOSTP	SOSCCR. SOSTP
High-speed	000b (HOCO) 001b (MOCO) 010b (LOCO) 011b (Main clock) 100b (Sub-clock) 101b (PLL)*Note:	000b (1/1) 001b (1/2) 010b (1/4) 011b (1/8) 100b (1/16) 101b (1/32) 110b (1/64)	0 (operating) 1 (stopped)	0 (operating) 1 (stopped)	0 (operating) 1 (stopped)	0 (operating) 1 (stopped)	0 (operating) 1 (stopped)	0 (operating) 1 (stopped)
Low-speed	000b (HOCO) 001b (MOCO) 010b (LOCO) 011b (Main clock) 100b (Sub-clock)		1 (stopped)					
Subosc-speed	010b (LOCO) 100b (Sub-clock)	000b (1/1)	1 (stopped)	1 (stopped)	1 (stopped)	0 (operating) 1 (stopped)	1 (stopped)	0 (operating) 1 (stopped)

Note: SCKSCR.CKSEL[2:0] only.

Table 11.12 Valid settings for the clock related registers (2)

Operating oscillator	Valid settings	
	OPCCR.OPCM[1:0]	SOPCCR.SOPCM
PLL	00b	0
High-speed on-chip oscillator	00b, 11b	0
Middle-speed on-chip oscillator		
Main clock oscillator		
Low-speed on-chip oscillator	00b, 11b	0, 1
Sub-clock oscillator		
IWDT-dedicated on-chip oscillator		

(3) Invalid register write accesses in subosc-speed mode

Do not write to registers listed in this section under the listed condition.

[Registers]

- SCKSCR, OPCCR.

[Condition]

- SOPCCR.SOPCM = 1 (Subosc-speed mode).

(4) Invalid register write accesses by the DTC or DMAC

Do not write to registers listed in this section by the DTC or DMAC.

[Registers]

- MSTPCRA.

- 从执行WFI指令到返回正常模式的时间段内
- 当FENTRYR.FENTRYi=1（i=0到3）（闪存PE模式）或FENTRYR.FENTRYD=1（数据闪存PE模式）时。

(2) 时钟相关寄存器的有效设置

表11.11和表11.12显示了每种工作电源控制模式下时钟相关寄存器的有效设置。请勿写入有效设置以外的任何值。任何其他写入值都将被忽略。每个寄存器在与工作功率控制模式相关的条件下都有某些禁止设置。有关每个寄存器的这些其他条件，请参见第9节，时钟生成电路。

Table 11.11 时钟相关寄存器的有效设置(1)

Mode	有效设置							
	SCKSCR.CKSEL[2:0], CKOCR.CKOSEL[2:0]	SCKDIVCR.FCK[2:0], ICK[2:0]	PLLCR.PLLSTP	HOCOCR. HCSTP	MOCOCR. MCSTP	LOCOCR. LCSTP	MOSCCR. MOSTP	SOSCCR. SOSTP
High-speed	000b (HOCO) 001b (MOCO) 010b (LOCO) 011b (Main clock) 100b (Sub-clock) 101b (PLL)*Note:	000b (1/1) 001b (1/2) 010b (1/4) 011b (1/8) 100b (1/16) 101b (1/32) 110b (1/64)	0 (operating) 1 (stopped)	0 (operating) 1 (stopped)	0 (operating) 1 (stopped)	0 (operating) 1 (stopped)	0 (operating) 1 (stopped)	0 (operating) 1 (stopped)
Low-speed	000b (HOCO) 001b (MOCO) 010b (LOCO) 011b (Main clock) 100b (Sub-clock)		1 (stopped)					
Subosc-speed	010b (LOCO) 100b (Sub-clock)	000b (1/1)	1 (stopped)	1 (stopped)	1 (stopped)	0 (operating) 1 (stopped)	1 (stopped)	0 (operating) 1 (stopped)

Note: SCKSCR.CKSEL[2:0] only.

Table 11.12 时钟相关寄存器的有效设置(2)

操作振荡器	有效设置	
	OPCCR.OPCM[1:0]	SOPCCR.SOPCM
PLL	00b	0
High-speed on-chip oscillator	00b, 11b	0
Middle-speed on-chip oscillator		
主时钟振荡器		
Low-speed on-chip oscillator	00b, 11b	0, 1
Sub-clock oscillator		
IWDT-dedicated on-chip oscillator		

(3) subosc-speed模式下的无效寄存器写访问

不要在列出的条件下写入本节中列出的寄存器。

[Registers]

- SCKSCR, OPCCR.

[Condition]

- SOPCCR.SOPCM = 1 (Subosc-speed mode).

(4) DTC或DMAC的无效寄存器写访问

不要写入DTC或DMAC在本节中列出的寄存器。

[Registers]

- MSTPCRA.

(5) Invalid register write accesses in Snooze mode

Do not write to registers listed in this section in Snooze mode. They must be set before entering Software Standby mode.

[Registers]

- SNZCR, SNZEDCR, SNZREQCR.

(6) Invalid write access to FLWT.FLWT[2:0]

Do not write any value other than 000b to the FLWT.FLWT[2:0] bits under the listed condition.

[Condition]

- SOPCCR.SOPCM = 1 (Subosc-speed mode)

(7) Invalid write access when PRCR.PRC1 is 0

Do not write to registers listed in this section when the PRCR.PRC1 bit is 0.

[Registers]

- SBYCR, SNZCR, SNZEDCR, SNZREQCR, OPCCR, SOPCCR, DPSBYCR, DPSIERn (n = 0 to 3), DPSIFRn (n = 0 to 3), DPSIEGRn (n = 0 to 2), and SYOCDCR.

11.10.2 I/O Port States

The I/O port states in Software Standby, Deep Software Standby, and Snooze modes (except when modifying in Snooze mode) are the same before entering the modes. Therefore, the power consumption is not reduced while the output signals are held high.

11.10.3 Module-Stop State of DMAC and DTC

Before writing 1 to MSTPCRA.MSTPA22, clear the DMAST.DMST bit of the DMAC and the DTCST.DTCST bit of the DTC to 0.

11.10.4 Internal Interrupt Sources

Interrupts do not operate in the module-stop state. If the module-stop bit is set when an interrupt request is generated, a CPU interrupt source or a DMAC or DTC startup source cannot be cleared. Always disable the associated interrupts before setting the module-stop bits.

11.10.5 Input Buffer Control by the DIRQnE Bit (n = 0 to 14)

Setting the DPSIERy.DIRQnE bit (y = 0, 1 and n = 0 to 14) to 1 enables the associated input buffer of the IRQ0-DS to IRQ14-DS pins. Although inputs to these pins are sent to the DPSIFRy.DIRQnF bits (y = 0, 1 and n = 0 to 14), they are not sent to the ICU, peripheral modules, or I/O ports.

11.10.6 Transition to Low-Power Modes

Because the MCU does not support wakeup by events, do not enter the low power modes (Sleep, Software Standby, or Deep Software Standby mode) by executing a WFE instruction. Also, do not set the SLEEPDEEP bit of the System Control Register in the Cortex®-M4 core, because the MCU does not support low power modes by SLEEPDEEP.

11.10.7 Timing of WFI Instruction

It is possible for the WFI instruction to be executed before I/O register and CS/SDRAM area writes are complete, in which case operation might not proceed as intended. This can happen if the WFI is placed immediately after a write to an I/O register or CS/SDRAM area. To avoid this problem, read back the register or CS/SDRAM area that was written to confirm that the write completed. For example, reading MSTPCRB register before execution of WFI instruction can secure the period to complete writing to the I/O register.

11.10.8 Writing to the WDT and IWDT Registers by the DMAC or DTC in Sleep or Snooze Mode

Do not write to the WDT or IWDT registers by the DMAC or DTC while the WDT or IWDT is stopped after entering

(5) 贪睡模式下的无效寄存器写访问

不要在贪睡模式下写入本节中列出的寄存器。必须在进入软件待机模式之前设置它们。

[Registers]

- SNZCR, SNZEDCR, SNZREQCR.

(6) 对FLWT.FLWT[2:0]的写入访问无效

在所列条件下，请勿将000b以外的任何值写入FLWT.FLWT[2:0]位。

[Condition]

- SOPCCR.SOPCM = 1 (Subosc-speed mode)

(7) 当PRCR.PRC1为0时，写入访问无效

当PRCR.PRC1位为0时，不要写入本节中列出的寄存器。

[Registers]

- SBYCR、SNZCR、SNZEDCR、SNZREQCR、OPCCR、SOPCCR、DPSBYCR、DPSIERn（n=0到3）、DPSIFRn（n=0到3）、DPSIEGRN（n=0到2）和SOOCDCR。

11.10.2 IO端口状态

软件待机、深度软件待机和贪睡模式下的IO端口状态（在贪睡模式下修改时除外）在进入这些模式之前是相同的。因此，在输出信号保持高电平的同时不会降低功耗。

11.10.3 DMAC和DTC的模块停止状态

在将1写入MSTPCRA.MSTPA22之前，清除DMAC的DMAST.DMST位和DTCST.DTCST位
DTC to 0.

11.10.4 内部中断源

中断不会在模块停止状态下运行。如果在产生中断请求时设置模块停止位，则
无法清除CPU中断源或DMAC或DTC启动源。在设置模块停止位之前，始终禁用相关的中断。

11.10.5 通过DIRQnE位（n=0到14）控制输入缓冲器

将DPSIERy.DIRQnE位（y=0、1和n=0至14）设置为1可启用IRQ0-DS至IRQ14-DS引脚的相关输入缓冲器。尽管这些引脚的输入被发送到DPSIFRy.DIRQnF位（y=0、1和n=0到14），但它们不会被发送到ICU、外设模块或IO端口。

11.10.6 过渡到低功耗模式

由于MCU不支持事件唤醒，请勿进入低功耗模式（睡眠、软件待机或
深度软件待机模式）通过执行WFE指令。此外，不要设置系统的SLEEPDEEP位
Cortex®-M4内核中的控制寄存器，因为MCU不支持SLEEPDEEP的低功耗模式。

11.10.7 WFI指令的时间安排

WFI指令可能在IO寄存器和CSSDRAM区域写入完成之前执行，在这种情况下操作可能不会按预期进行。如果在写入IO寄存器或CSSDRAM区域后立即放置WFI，则会发生这种情况。为避免此问题，请回读已写入的寄存器或CSSDRAM区域以确认写入已完成。例如，在执行WFI指令之前读取MSTPCRB寄存器可以确保完成写入IO寄存器的时间。

11.10.8 在休眠或休眠状态下由DMAC或DTC写入WDT和IWDT寄存器贪睡模式

当WDT或IWDT进入后停止时，请勿通过DMAC或DTC写入WDT或IWDT寄存器

Sleep or Snooze mode.

11.10.9 Oscillators in Snooze Mode

Oscillators that stop on entering Software Standby mode automatically restart when a trigger for switching to Snooze mode is generated. The MCU does not enter Snooze mode until all of the oscillators stabilize. In Snooze mode, you must disable oscillators that are not required in Snooze mode before entering Software Standby mode. Otherwise, the transition from Software Standby to Snooze mode takes longer.

11.10.10 Snooze Mode Entry by RXD0 Falling Edge

When the SNZCR.RXDREQEN bit is 1, noise on the RXD0 pin might cause the MCU transition from Software Standby to Snooze mode. Any subsequent RXD0 data can be received in Snooze mode by noise on the RXD0 pin. If the MCU does not receive any RXD0 data after the noise, interrupts such as SCI0_ERI or SCI0_RXI, and address mismatch events are not generated, and the MCU stays in Snooze mode. To avoid this, an AGT1 underflow interrupt must be used to return to Software Standby or Normal mode when using SCI0 in Snooze mode. However, do not use the AGT1 underflow as a source to return to Software Standby mode during an SCI communication. This makes the SCI0 stop the operation in a half-finished state.

11.10.11 Using SCI0 in Snooze Mode

When using SCI0 in Snooze mode, the AGT1 underflow must be used for the interrupt request or Snooze end request. Do not use any other trigger.

When using SCI0 in Snooze mode, the following conditions must be satisfied:

- The clock source must be HOCO
- MOCO, the main clock oscillator, and the PLL must stop before entering Software Standby mode
- The RXD0 pin must be kept at the high level before entering Software Standby mode
- A transition to Software Standby mode must not occur during an SCI communication
- The MSTPCRC.MSTPC0 bit must be 1 before entering Software Standby mode.

11.10.12 Conditions of A/D Conversion Start in Snooze Mode

The ADC12 can only be triggered by the ELC in Snooze mode. Do not use a software trigger or ADTRGn pin.

11.10.13 ELC Events in Snooze Mode

Only the ELC events listed in this section are available in Snooze mode. Do not use any other events. If starting peripheral modules for the first time after entering Snooze mode, the Event Link Setting Register (ELSRn) must set a Snooze mode entry event (SYSTEM_SNZREQ) as the trigger.

- Snooze mode entry (SYSTEM_SNZREQ)
- DTC transfer end (DTC_DTCEND)
- ADC12n Window A/B compare match (ADC12n_WCMPM) (n = 0, 1)
- ADC12n Window A/B compare mismatch (ADC12n_WCMPUM) (n = 0, 1)
- Data operation circuit interrupt (DOC_DOPCI).

11.10.14 Conditions of CTSU in Snooze Mode

The CTSU can only be started by the ELC in Snooze mode.

睡眠或贪睡模式。

11.10.9 贪睡模式下的振荡器

进入软件待机模式时停止的振荡器会在生成切换到贪睡模式的触发器时自动重新启动。在所有振荡器稳定之前，MCU不会进入贪睡模式。在贪睡模式下，您必须先禁用贪睡模式下不需要的振荡器，然后才能进入软件待机模式。否则，从软件待机到贪睡模式的转换需要更长的时间。

11.10.10 通过RXD0下降沿进入贪睡模式

当SNZCR.RXDREQEN位为1时，RXD0引脚上的噪声可能会导致MCU从软件待机模式转换到贪睡模式。任何后续的RXD0数据都可以通过RXD0引脚上的噪声在贪睡模式下接收。如果噪声后MCU没有收到任何RXD0数据，则不会产生SCI0_ERI或SCI0_RXI等中断和地址不匹配事件，并且MCU处于贪睡模式。为避免这种情况，在贪睡模式下使用SCI0时，必须使用AGT1下溢中断返回到软件待机或正常模式。但是，不要将AGT1下溢用作SCI通信期间返回软件待机模式的源。这使得SCI0在半完成状态下停止操作。

11.10.11 在贪睡模式下使用SCI0

在贪睡模式下使用SCI0时，AGT1下溢必须用于中断请求或贪睡结束请求。不要使用任何其他触发器。

在贪睡模式下使用SCI0时，必须满足以下条件：

- 时钟源必须是HOCO
- MOCO、主时钟振荡器和PLL在进入软件待机模式之前必须停止
- 进入软件待机模式前，RXD0引脚必须保持高电平
- 在SCI通信期间不得转换到软件待机模式
- 在进入软件待机模式之前，MSTPCRC.MSTPC0位必须为1。

11.10.12 贪睡模式下AD转换开始的条件

ADC12只能由ELC在贪睡模式下触发。不要使用软件触发或ADTRGn引脚。

11.10.13 贪睡模式下的ELC事件

只有本节中列出的ELC事件在贪睡模式下可用。不要使用任何其他事件。如果进入贪睡模式后第一次启动外围模块，事件链接设置寄存器（ELSRn）必须设置贪睡模式进入事件（SYSTEM_SNZREQ）作为触发器。

- 贪睡模式进入(SYSTEM_SNZREQ)
- DTC传输结束(DTC_DTCEND)
- ADC12n窗口AB比较匹配(ADC12n_WCMPM)(n=0 1)
- ADC12n窗口AB比较失配(ADC12n_WCMPUM)(n=0 1)
- 数据操作电路中断（DOC_DOPCI）。

11.10.14 CTSU在贪睡模式下的情况

CTSU只能由ELC在贪睡模式下启动。

12. Battery Backup Function

12.1 Overview

The battery backup function maintains partial battery powering in the event of power loss. Switching between VCC and VBATT, it always maintains power to the RTC, SOSC, and backup memory. During normal operation, the battery powered area is powered by the main power supply, the VCC pin. When a VCC voltage drop is detected, the power source switches to the dedicated battery backup power pin, the VBATT pin. When the voltage rises again, the power source switches back from VBATT to VCC.

12.1.1 Features of Battery Backup Function

Battery backup features include:

- Battery power supply switch
- Backup registers
- Time capture pin detection.

12.1.2 Battery Power Supply Switch

When the voltage applied to the VCC pin drops, this feature switches the power supply from the VCC pin to the VBATT pin. When the voltage rises, it switches the power supply from the VBATT pin back to the VCC pin.

12.1.3 Backup Registers

The battery powered area provides 512 one-byte backup registers. These registers retain data only when VBATT is supplied and VCC is powered off.

12.1.4 Time Capture Pin Detection

The RTC detects input level changes on the time capture pin. For more information, see section 26, Realtime Clock (RTC).

Note: When VCC is < $V_{DETBATT}$ and > (VBATT + 0.6 V), the injected current connects from the VCC to the VBATT pin through an internal diode. If the power supply battery connected to the VBATT pin cannot support this current injection, for example if the battery is not rechargeable, Renesas strongly recommends that you connect through a low-voltage threshold diode between the power supply battery and the VBATT pin.

Note: You must enable voltage monitor 0 resets to use the battery backup function. The voltage monitor 0 level must be higher than the VBATT switch level.

Figure 12.1 shows the configuration of the battery backup function.

12. 电池备份功能

12.1 Overview

电池备份功能可在断电时保持部分电池供电。VCC和之间切换
VBATT，它始终保持对RTC、SOSC和备份存储器的供电。在正常运行期间，电池供电区域由主电源VCC引脚供电。当检测到VCC电压下降时，电源切换到专用电池备用电源引脚VBATT引脚。当电压再次上升时，电源从VBATT切换回VCC。

12.1.1 电池备份功能的特点

电池备份功能包括：

- 电池供电开关
- 备份寄存器
- 时间捕捉引脚检测。

12.1.2 电池电源开关

当施加到VCC引脚的电压下降时，此功能将电源从VCC引脚切换到VBATT引脚。当电压上升时，它将电源从VBATT引脚切换回VCC引脚。

12.1.3 备份寄存器

电池供电区提供512个单字节备份寄存器。这些寄存器仅在提供VBATT且VCC断电时保留数据。

12.1.4 时间捕捉引脚检测

RTC检测时间捕捉引脚上的输入电平变化。有关详细信息，请参阅第26节，实时时钟(RTC)。

Note: 当VCC<VDETBATT且>(VBATT+0.6V)时，注入电流从VCC连接到VBATT引脚
通过内部二极管。如果连接到VBATT引脚的电源电池不能支持这种电流注入，例如，如果电池不可充电，瑞萨强烈建议您通过电源电池和VBATT引脚之间的低压阈值二极管进行连接。

Note: 您必须启用电压监视器0复位才能使用电池备份功能。电压监视器0电平必须高于VBATT开关电平。

图12.1显示了电池备份功能的配置。

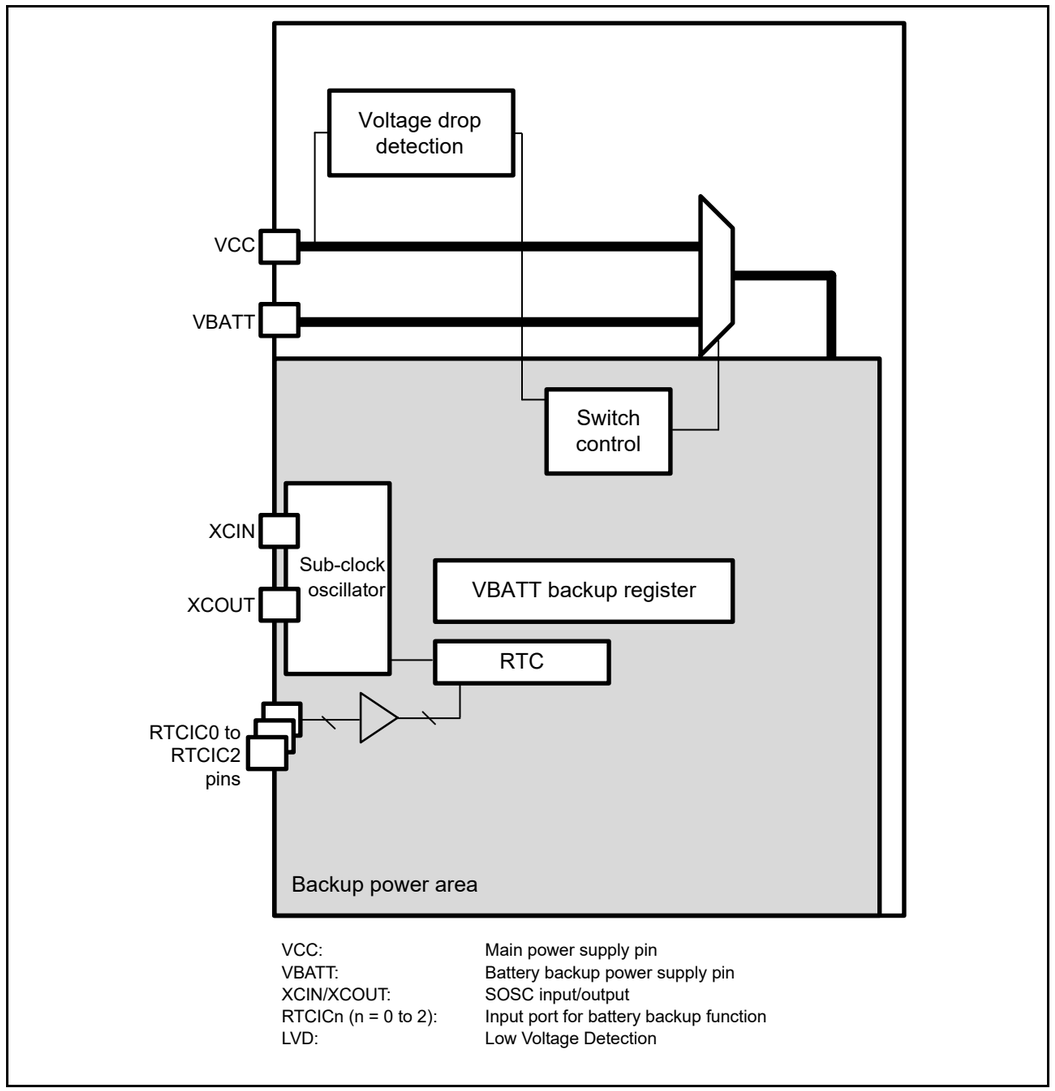


Figure 12.1 Configuration of the battery backup function

12.2 Register Descriptions

12.2.1 VBATT Backup Register (VBTBKRn) (n = 0 to 511)

Address(es): SYSTEM.VBTBKR[0] 4001 E500h to SYSTEM.VBTBKR[511] 4001 E6FFh

	b7	b6	b5	b4	b3	b2	b1	b0
	VBTBKR[7:0]							
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

VBTBKRn is an 8-bit access read/write register for storing data powered by VBATT. The value of this register is

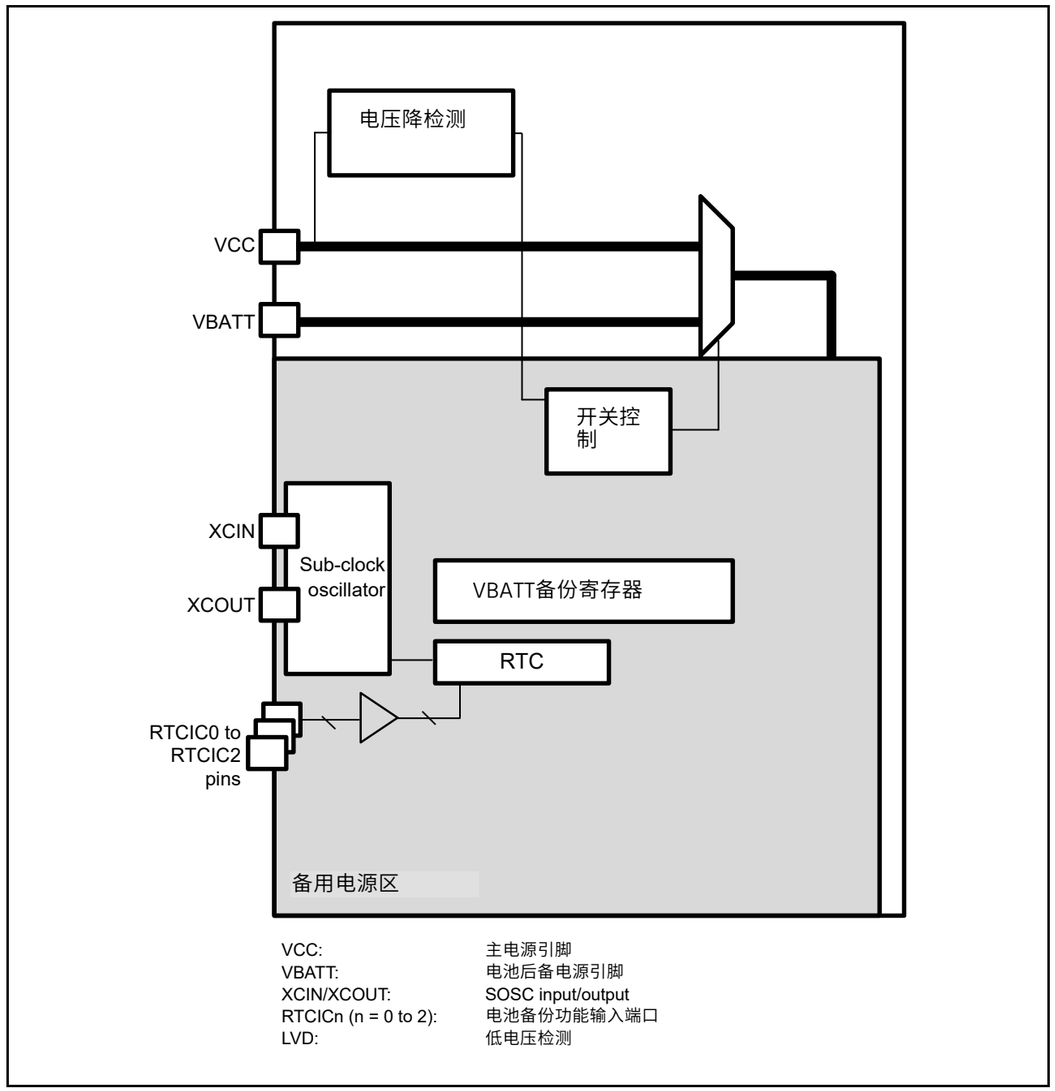


Figure 12.1 电池备份功能的配置

12.2 注册说明

12.2.1 VBATT备份寄存器(VBTBKRn)(n=0至511)

地址：系统。VBTBKR[0]4001E500h到系统。VBTBKR[511]4001E6FFh

	b7	b6	b5	b4	b3	b2	b1	b0
	VBTBKR[7:0]							
重置后的值：	x	x	x	x	x	x	x	x

x: Undefined

VBTBKRn是一个8位访问读写寄存器，用于存储由VBATT供电的数据。该寄存器的值为

retained when VCC is not powered and VBATT is powered. This register is not initialized by any reset.

12.2.2 VBATT Input Control Register (VBTICTLR)

Address(es): SYSTEM.VBTICTLR 4001 E4BBh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	VCH2INEN	VCH1INEN	VCH0INEN
Value after reset:	0	0	0	0	0	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b0	VCH0INEN	VBATT CH0 Input Enable	0: Disable 1: Enable.	R/W
b1	VCH1INEN	VBATT CH1 Input Enable	0: Disable 1: Enable.	R/W
b2	VCH2INEN	VBATT CH2 Input Enable	0: Disable 1: Enable.	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The VBTICTLR register selects the VBATT I/O direction as input.

VCHnINEN bit (VBATT CHn Input Enable Bit) (n = 0 to 2)

The VCHnINEN bit enables the input direction on the associated VBATT channel.

For more information on CH0 to CH2 corresponding function, see section 20.5.5, I/O Buffer Specification.

12.3 Operation

12.3.1 Battery Backup Function

When the voltage on the VCC pin drops, power can be supplied to the RTC and sub-clock oscillator from the VBATT pin. When a power supply drop from the VCC pin is detected, the power connection switches from the power supply to the VBATT pin. The power supply from the VCC pin is resumed when the voltage on the VCC pin exceeds $V_{DETBATT}$. This power supply change does not affect the RTC operation.

You must enable voltage monitor 0 resets to use the battery backup function. The RTC supports time capture detection, triggered by a change to the time capture pin input level.

The VBATT pin supplies power to the following modules:

- RTC
- Sub-clock oscillator (including XCIN and XCOUT pins)
- VBATT Backup Register.

Table 12.1 shows the operating states in VBATT mode.

Table 12.1 Operating states in VBATT mode (1 of 2)

Operating state	VBATT mode
Transition condition	Detection of VCC voltage drop
Canceling method other than reset	Detection of VCC voltage rise
State after cancellation by an interrupt	—
State after cancellation by a reset	—
Main clock oscillator	Stopped

当VCC未通电且VBATT通电时保留。该寄存器不会被任何复位初始化。

12.2.2 VBATT输入控制寄存器(VBTICTLR)

Address(es): SYSTEM.VBTICTLR 4001 E4BBh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	VCH2INEN	VCH1INEN	VCH0INEN
重置后的值：	0	0	0	0	0	x	x	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b0	VCH0INEN	VBATTCH0输入使能	0：禁用1 ：启用。	R/W
b1	VCH1INEN	VBATTCH1输入使能	0：禁用1 ：启用。	R/W
b2	VCH2INEN	VBATTCH2输入使能	0：禁用1 ：启用。	R/W
b7 to b3	—	Reserved	这些位被读取为0。写入值应为0。	R/W

VBTICTLR寄存器选择VBATTIO方向作为输入。

VCHnINEN位（VBATTCHn输入使能位）（n=0至2）

VCHnINEN位使能相关VBATT通道上的输入方向。

有关CH0到CH2对应功能的更多信息，请参阅第20.5.5节，IO缓冲器规范。

12.3 Operation

12.3.1 电池备份功能

当VCC引脚上的电压下降时，可以从VBATT引脚为RTC和副时钟振荡器供电。当检测到VCC引脚的电源下降时，电源连接从电源切换到VBATT引脚。当VCC引脚上的电压超过VDETBATT时，重新从VCC引脚供电。此电源更改不会影响RTC操作。

您必须启用电压监视器0复位才能使用电池备份功能。RTC支持时间捕捉检测，由时间捕捉引脚输入电平的变化触发。

VBATT引脚为以下模块供电：

- RTC
- 副时钟振荡器（包括XCIN和XCOUT引脚）
- VBATT备份寄存器。

表12.1显示了VBATT模式下的操作状态。

Table 12.1 VBATT模式下的操作状态（1of2）

运行状态	VBATT mode
过渡条件	检测VCC电压降
复位以外的取消方法	检测VCC电压上升
中断取消后的状态	—
通过复位取消后的状态	—
主时钟振荡器	Stopped

Table 12.1 Operating states in VBATT mode (2 of 2)

Operating state	VBATT mode
Sub-clock oscillator	Operating
High-speed on-chip oscillator	Stopped
Middle-speed on-chip oscillator	Stopped
Low-speed on-chip oscillator	Stopped
IWDT-dedicated on-chip oscillator	Stopped
PLL	Stopped
CPU	Stopped (undefined)
SRAM (ECC SRAM included)	Stopped (undefined)
Standby SRAM	Stopped (undefined)
VBATT Backup Register	Stopped (retained)
Flash memory	Stopped (retained)
Realtime Clock (RTC)	Selectable when selecting clock that serves as the count source
AGTn (n = 0, 1)	Stopped (undefined)
Low Voltage Detection (LVD)	Stopped
Power-on reset circuit	Stopped
Other peripheral modules	Stopped (undefined)
I/O ports	• RTCICn ports (n = 0 to 2): Operating • All ports not specified here: Undefined.

Note: *Selectable* means that operating or stopped is selectable in the control registers. Some modules are also controlled by the associated module-stop bit.
Note: *Stopped (retained)* means that the contents of the internal registers are retained but the operations are suspended.
Note: *Stop (undefined)* means that the contents of the internal registers are undefined and power to the internal circuit is cut off.

Figure 12.2 shows the switching sequence of the battery backup function.

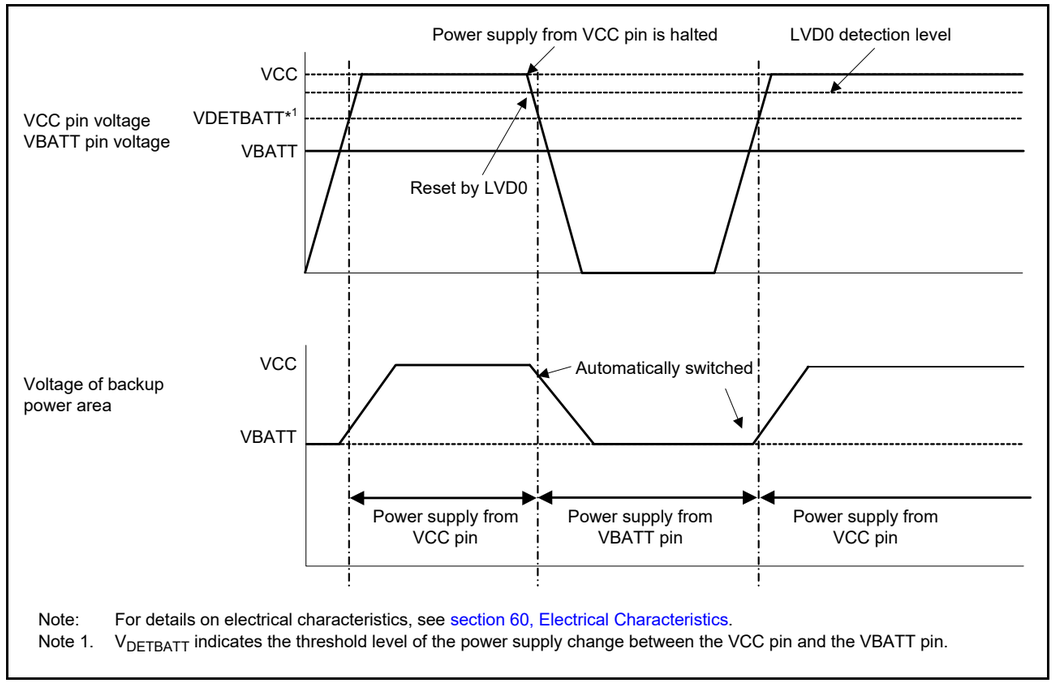
Table 12.1 VBATT模式下的操作状态（2个中的2个）

运行状态	VBATT mode
Sub-clock oscillator	Operating
High-speed on-chip oscillator	Stopped
Middle-speed on-chip oscillator	Stopped
Low-speed on-chip oscillator	Stopped
IWDT-dedicated on-chip oscillator	Stopped
PLL	Stopped
CPU	Stopped (undefined)
SRAM (ECC SRAM included)	Stopped (undefined)
Standby SRAM	Stopped (undefined)
VBATT备份寄存器	Stopped (retained)
闪存	Stopped (retained)
实时时钟(RTC)	选择作为计数源的时钟时可选择
AGTn (n = 0, 1)	Stopped (undefined)
低电压检测(LVD)	Stopped
上电复位电路	Stopped
其他外围模块	Stopped (undefined)
I/O ports	RTCICn端口（n=0到2）：运行中 此处未指定的所有端口：未定义。

Note: 可选意味着在控制寄存器中可以选择操作或停止。一些模块也由相关的模块停止位控制。

Note: 停止（retained）是指内部寄存器的内容被保留，但操作被暂停。
Note: 停止（未定义）表示内部寄存器的内容未定义，内部电路的电源被切断。

图12.2显示了电池备份功能的切换顺序。



Note: For details on electrical characteristics, see section 60, Electrical Characteristics.
Note 1. $V_{DETBATT}$ indicates the threshold level of the power supply change between the VCC pin and the VBATT pin.

Figure 12.2 Switching sequence for the battery backup function

12.3.2 VBATT Battery Power Supply Switch Usage

The battery power supply switch can switch the power supply from the VCC pin to the VBATT pin when the voltage being applied to the VCC pin drops. When the voltage rises, this switch changes the power supply from the VBATT pin to the VCC pin.

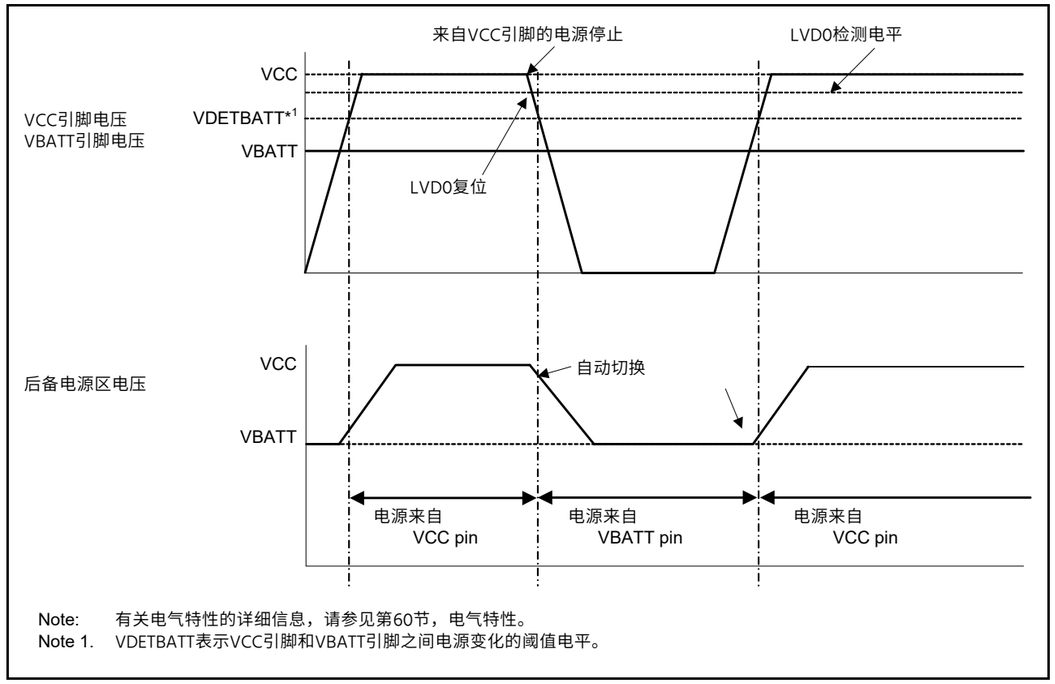
Note: You must enable voltage monitor 0 resets to use the battery backup function. Voltage monitor 0 level must be higher than the VBATT switch level.

12.3.3 VBATT Backup Register Usage

Use the VBATT backup registers VBTBKRn, where n = 0 to 511, to store or restore data with an 8-bit read or write operation.

12.4 Usage Notes

1. Operation of the sub-clock oscillator and RTC are not guaranteed when the voltage level on VBATT is lower than the guaranteed operation range. The RTC must be initialized to restart the power supply after the VBATT pin falls below the guaranteed operating voltage.
2. A reset generated while writing to registers described in this section might destroy the register value.
3. When VCC is higher than $V_{DETBATT}$, the VCC pin and VBATT pin are separated. When VCC is lower than $V_{DETBATT}$ and the switch is connected to the VBATT pin, and if the voltage on VBATT drops lower than (VCC - 0.6 V), current might flow into the VBATT pin through the parasitic diode between the VCC and VBATT pins.
4. During RTC operation using the voltage from the VBATT pin and the I/O ports (P402, P403 and P404) within the backup, the power supply area can only be used as time capture event input pins for the RTC.



Note: 有关电气特性的详细信息，请参见第60节，电气特性。
Note 1. VDETBATT表示VCC引脚和VBATT引脚之间电源变化的阈值电平。

Figure 12.2 电池备份功能的切换顺序

12.3.2 VBATT电池电源开关使用

当施加到VCC引脚的电压下降时，电池电源开关可以将电源从VCC引脚切换到VBATT引脚。当电压上升时，该开关将电源从VBATT引脚切换到VCC引脚。

Note: 您必须启用电压监视器0复位才能使用电池备份功能。电压监视器0电平必须高于VBATT开关电平。

12.3.3 VBATT备份寄存器使用

使用VBATT备份寄存器VBTBKRn，其中n=0到511，通过8位读取或写入操作来存储或恢复数据。

12.4 使用说明

1. 当VBATT上的电压电平低于保证的工作范围时，不保证子时钟振荡器和RTC的工作。在VBATT引脚低于保证工作电压后，必须初始化RTC以重新启动电源。
2. 写入本节中描述的寄存器时产生的复位可能会破坏寄存器值。
3. 当VCC高于VDETBATT时，VCC管脚和VBATT管脚是分开的。当VCC低于VDETBATT和开关连接到VBATT引脚，如果VBATT上的电压低于(VCC0.6V)，电流可能会通过VCC和VBATT引脚之间的寄生二极管流入VBATT引脚。
4. 在使用来自VBATT引脚和备用IO端口（P402、P403和P404）的电压进行RTC操作期间，电源区域只能用作RTC的时间捕捉事件输入引脚。

13. Register Write Protection

13.1 Overview

The register write protection function protects important registers from being overwritten because of software errors. The registers to be protected are set with the Protect Register (PRCR). Table 13.1 lists the association between the PRCR bits and the registers to be protected.

Table 13.1 Association between PRCR bits and registers to be protected

PRCR bit	Registers to be protected
PRC0	• Registers related to the Clock Generation Circuit: SCKDIVCR, SCKDIVCR2, SCKSCR, PLLCCR, PLLCR, BCKCR, MOSCCR, HOCOCR, MOCOCR, CKOCR, TRCKCR, OSTDCR, OSTDSR, EBCKOCR, SDCKOCR, MOCOUTCR, HOCOUTCR, MOSCWTCR, MOMCR, SOSCCR, SOMCR, LOCOCR, LOCOUTCR, HOCOWTCR, FLLCR1, FLLCR2
PRC1	• Registers related to the low power modes: SBYCR, SNZCR, SNZEDCR, SNZREQCR, OPCCR, SOPCCR, DPSBYCR, DPSIER0-3, DPSIFR0-3, DPSIEGR0-2, SYOCDCR, STCONR • Registers related to the battery backup function: VBTBKRn (n = 0 to 511), VBTICTLR
PRC3	• Registers related to the LVD: LVD1CR1, LVD1SR, LVD2CR1, LVD2SR, LVCMPCR, LVDLVLR, LVD1CR0, LVD2CR0

13.2 Register Descriptions

13.2.1 Protect Register (PRCR)

Address(es): SYSTEM.PRCR 4001 E3FEh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PRKEY[7:0]								—	—	—	—	PRC3	—	PRC1	PRC0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Function	R/W
b0	PRC0	Protect Bit 0	Enables writing to the registers related to the Clock Generation Circuit: 0: Disable writes 1: Enable writes.	R/W
b1	PRC1	Protect Bit 1	Enables writing to the registers related to the low power modes and the battery backup function: 0: Disable writes 1: Enable writes.	R/W
b2	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b3	PRC3	Protect Bit 3	Enables writing to the registers related to the LVD: 0: Disable writes 1: Enable writes.	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15 to b8	PRKEY[7:0]	PRC Key Code	These bits control write access to the PRCR register. To modify the PRCR register, write A5h to the eight higher-order bits and the wanted value to the eight lower-order bits as a 16-bit unit.	W*1

Note 1. Write data is not retained. Always reads 00h.

PRCn bits (Protect Bit n) (n = 0, 1, 3)

The PRCn bits enable or disable writing to the protected registers listed in Table 13.1. Setting PRCn to 1 or 0 enables or disables writing, respectively.

13. 寄存器写保护

13.1 Overview

寄存器写保护功能可保护重要寄存器不因软件错误而被覆盖。要保护的寄存器由保护寄存器(PRCR)设置。表13.1列出了PRCR位与要保护的寄存器之间的关联。

Table 13.1 PRCR位和要保护的寄存器之间的关联

PRCR bit	受保护的寄存器
PRC0	与时钟生成电路相关的寄存器： SCKDIVCR, SCKDIVCR2, SCKSCR, PLLCCR, PLLCR, BCKCR, MOSCCR, HOCOCR, MOCOCR, CKOCR, TRCKCR, OSTDCR, OSTDSR, EBCKOCR, SDCKOCR, MOCOUTCR, HOCOUTCR, MOSCWTCR, MOMCR, SOSCCR, SOMCR, LOCOCR, LOCOUTCR, HOCOWTCR, FLLCR1, FLLCR2
PRC1	与低功耗模式相关的寄存器： SBYCR, SNZCR, SNZEDCR, SNZREQCR, OPCCR, SOPCCR, DPSBYCR, DPSIER0-3, DPSIFR0-3, DPSIEGR0-2、SYOCDCR、STCONR 与电池备份功能相关的寄存器：VBTBKRn（n=0至511）、VBTICTLR
PRC3	与LVD相关的寄存器： LVD1CR1, LVD1SR, LVD2CR1, LVD2SR, LVCMPCR, LVDLVLR, LVD1CR0, LVD2CR0

13.2 注册说明

13.2.1 保护寄存器(PRCR)

Address(es): SYSTEM.PRCR 4001 E3FEh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PRKEY[7:0]								—	—	—	—	PRC3	—	PRC1	PRC0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Function	R/W
b0	PRC0	保护位0	允许写入与时钟生成电路相关的寄存器：0：禁止写入1：允许写入。	R/W
b1	PRC1	保护位1	允许写入与低功耗模式和电池备份功能相关的寄存器：0：禁止写入1：允许写入。	R/W
b2	—	Reserved	该位读取为0。写入值应为0。	R/W
b3	PRC3	保护位3	允许写入与LVD相关的寄存器：0：禁止写入1：允许写入。	R/W
b7 to b4	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b15 to b8	PRKEY[7:0]	中华人民共和国密钥代码	这些位控制对PRCR寄存器的写访问。要修改PRCR寄存器，将A5h写入高8位，将所需值写入低8位，以16位为单位。	W*1

Note 1. 不保留写入数据。始终读取00h。

PRCn位（保护位n）（n=0、1、3）

PRCn位启用或禁用对表13.1中列出的受保护寄存器的写入。将PRCn设置为1或0分别启用或禁用写入。

14. Interrupt Controller Unit (ICU)

14.1 Overview

The Interrupt Controller Unit (ICU) controls which event signals are linked to the NVIC, DTC, and DMAC modules. The ICU also controls non-maskable interrupts. Table 14.1 lists the ICU specifications, Figure 14.1 shows a block diagram, and Table 14.2 lists the I/O pins.

Table 14.1 ICU specifications

Parameter		Specifications
Interrupts	Peripheral function interrupts	• Interrupts from peripheral modules Number of sources: 315 (select factors within event list numbers 64 to 511)
	External pin interrupts	• Interrupt detection on low level, falling edge, rising edge, rising and falling edges One of these detection methods can be set for each source. • Digital filter function supported • 16 sources, with interrupts from IRQ0 to IRQ15 pins.
	DTC and DMAC control	The DTC and DMAC can be activated using interrupt sources*1
	Interrupt sources for NVIC	96 sources
Non-maskable interrupts*2	NMI pin interrupt	• Interrupt from the NMI pin • Interrupt detection on falling edge or rising edge • Digital filter function supported.
	Oscillation stop detection interrupt*3	Interrupt on detecting that the main oscillator has stopped
	WDT underflow/refresh error*3	Interrupt on an underflow of the down-counter or occurrence of a refresh error
	IWDT underflow/refresh error*3	Interrupt on an underflow of the down-counter or occurrence of a refresh error
	Voltage monitor 1 interrupt*3	Voltage monitor interrupt of Low Voltage Detection detector 1 (LVD1)
	Voltage monitor 2 interrupt*3	Voltage monitor interrupt of Low Voltage Detection detector 2 (LVD2)
	RPEST	Interrupt on SRAM parity error
	RECCST	Interrupt on SRAM ECC error
	BUSSST	Interrupt on MPU bus slave error
	BUSMST	Interrupt on MPU bus master error
	SPEST	Interrupt on CPU stack pointer monitor
Return from low power mode*4		• Sleep mode: Return is initiated by non-maskable interrupts or any other interrupt source • Software Standby mode: Return is initiated by non-maskable interrupts Interrupts can be selected in the WUPEN register. • Snooze mode: Return is initiated by non-maskable interrupts Interrupts can be selected in the SELSR0 and WUPEN registers. See section 14.2.8, SYS Event Link Setting Register (SELSR0), and section 14.2.9, Wake Up Interrupt Enable Register (WUPEN).

Note 1. For the DTC and DMAC activation sources, see Table 14.4.
Note 2. Non-maskable interrupts can be enabled only once after a reset release.
Note 3. These non-maskable interrupts can also be used as event signals. When used as interrupts, do not change the value of the NMIER register from the reset state. To enable voltage monitor 1 and 2 interrupts, set the LVD1CR1.IRQSEL and LVD2CR1.IRQSEL bits to 1.
Note 4. For return from Deep Software Standby mode, see section 11.9, Deep Software Standby Mode.

14. 中断控制器单元(ICU)

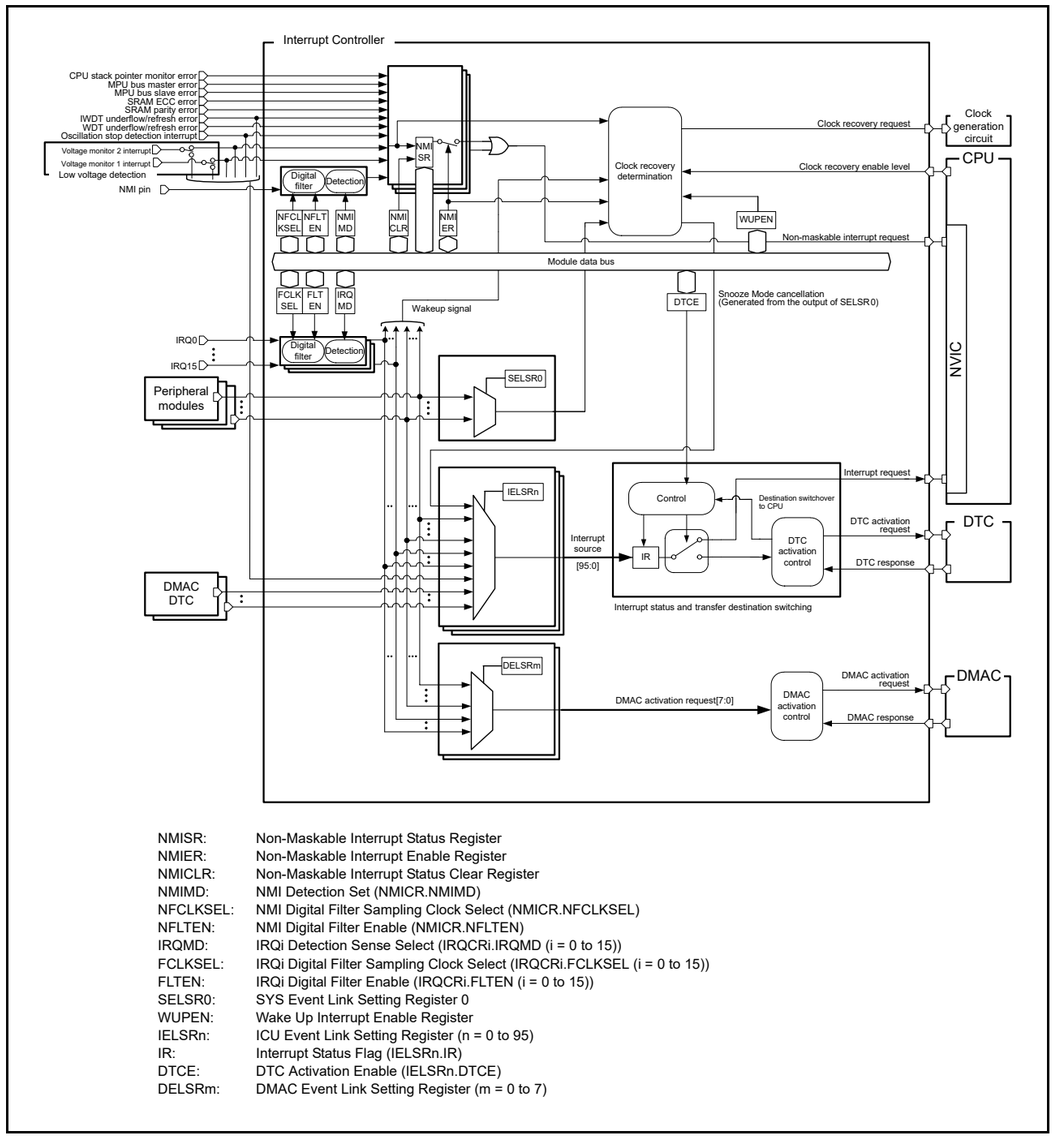
14.1 Overview

中断控制器单元(ICU)控制哪些事件信号链接到NVIC、DTC和DMAC模块。
ICU还控制不可屏蔽的中断。表14.1列出了ICU规格，图14.1显示了框图，表14.2列出了IO引脚。

Table 14.1 ICU规格

Parameter		Specifications
Interrupts	外设功能中断	来自外围模块的中断 来源数量：315（在事件列表编号64到511中选择因素）
	外部引脚中断	低电平、下降沿、上升沿、上升沿和下降沿的中断检测可以为每个源设置其中一种检测方法。 支持数字滤波器功能 16个源，中断从IRQ0到IRQ15引脚。
	DTC和DMAC控制	DTC和DMAC可以使用中断源*1激活
	NVIC的中断源	96 sources
Non-maskable interrupts*2	NMI引脚中断	来自NMI引脚的中断 下降沿或上升沿中断检测 支持数字滤波器功能。
	振荡停止检测中断*3	检测到主振荡器停止时中断
	WDT underflow/refresh error*3	递减计数器下溢或发生刷新错误时中断
	IWDT underflow/refresh error*3	递减计数器下溢或发生刷新错误时中断
	电压监视器1中断*3	低电压检测检测器1(LVD1)的电压监控中断
	电压监视器2中断*3	低电压检测检测器2(LVD2)的电压监控中断
	RPEST	SRAM奇偶校验错误中断
	RECCST	SRAMECC错误中断
	BUSSST	MPU总线从机错误中断
	BUSMST	MPU总线主机错误中断
	SPEST	CPU堆栈指针监视器中断
从低功耗模式返回*4		睡眠模式：由不可屏蔽中断或任何其他中断源启动返回 软件待机模式：由不可屏蔽中断启动返回可以在WUPEN寄存器中选择中断。 贪睡模式：返回由不可屏蔽的中断启动 可以在SELSR0和WUPEN寄存器中选择中断。 请参阅第14.2.8节，SYS事件链接设置寄存器(SELSR0)和第14.2.9节，唤醒中断使能寄存器（WUPEN）。

Note 1. 有关DTC和DMAC激活源，请参见表14.4。
Note 2. 不可屏蔽中断只能在复位释放后启用一次。
Note 3. 这些不可屏蔽的中断也可以用作事件信号。当用作中断时，不要改变NMIER寄存器从复位状态。要启用电压监视器1和2中断，请设置LVD1CR1.IRQSEL和LVD2CR1.IRQSEL位为1。
Note 4. 要从深度软件待机模式返回，请参阅第11.9节，深度软件待机模式。



NMISR: Non-Maskable Interrupt Status Register
NMIER: Non-Maskable Interrupt Enable Register
NMICLR: Non-Maskable Interrupt Status Clear Register
NMIMD: NMI Detection Set (NMICR.NMIMD)
NFCLKSEL: NMI Digital Filter Sampling Clock Select (NMICR.NFCLKSEL)
NFLTEN: NMI Digital Filter Enable (NMICR.NFLTEN)
IRQMD: IRQi Detection Sense Select (IRQCRi.IRQMD (i = 0 to 15))
FCLKSEL: IRQi Digital Filter Sampling Clock Select (IRQCRi.FCLKSEL (i = 0 to 15))
FLTEN: IRQi Digital Filter Enable (IRQCRi.FLTEN (i = 0 to 15))
SELSR0: SYS Event Link Setting Register 0
WUPEN: Wake Up Interrupt Enable Register
IELSRn: ICU Event Link Setting Register (n = 0 to 95)
IR: Interrupt Status Flag (IELSRn.IR)
DTCE: DTC Activation Enable (IELSRn.DTCE)
DELSRm: DMAC Event Link Setting Register (m = 0 to 7)

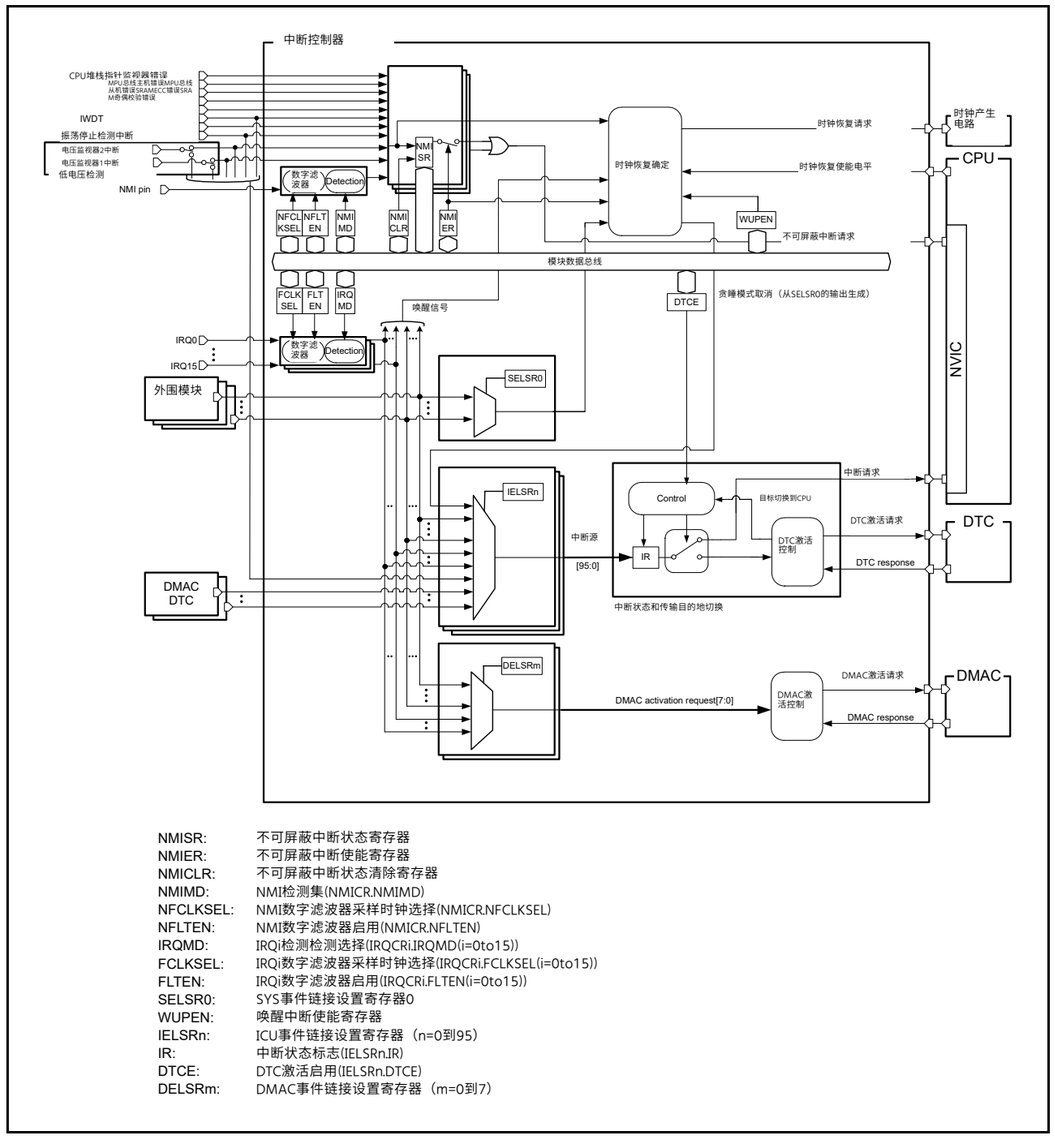
Figure 14.1 ICU block diagram

Table 14.2 ICU I/O pins

Pin name	I/O	Description
NMI	Input	Non-maskable interrupt request pin
IRQ0 to IRQ15	Input	External interrupt request pins

14.2 Register Descriptions

This chapter does not describe the Arm® NVIC internal registers. For information on these registers, see the *ARM® Cortex®-M4 Processor Technical Reference Manual* (ARM DDI 0439D).



NMISR: 不可屏蔽中断状态寄存器
NMIER: 不可屏蔽中断使能寄存器
NMICLR: 不可屏蔽中断状态清除寄存器
NMIMD: NMI检测集(NMICR.NMIMD)
NFCLKSEL: NMI数字滤波器采样时钟选择(NMICR.NFCLKSEL)
NFLTEN: NMI数字滤波器启用(NMICR.NFLTEN)
IRQMD: IRQi检测检测选择(IRQCRi.IRQMD(i=0to15))
FCLKSEL: IRQi数字滤波器采样时钟选择(IRQCRi.FCLKSEL(i=0to15))
FLTEN: IRQi数字滤波器启用(IRQCRi.FLTEN(i=0to15))
SELSR0: SYS事件链接设置寄存器0
WUPEN: 唤醒中断使能寄存器
IELSRn: ICU事件链接设置寄存器（n=0到95）
IR: 中断状态标志(IELSRn.IR)
DTCE: DTC激活启用(IELSRn.DTCE)
DELSRm: DMAC事件链接设置寄存器（m=0到7）

Figure 14.1 ICU框图

Table 14.2 ICUIO引脚

引脚名称	I/O	Description
NMI	Input	不可屏蔽中断请求引脚
IRQ0 to IRQ15	Input	外部中断请求引脚

14.2 注册说明

本章不介绍Arm®NVIC内部寄存器。有关这些寄存器的信息，请参阅ARM® Cortex®-M4处理器技术参考手册(ARMDDI0439D)。

14.2.1 IRQ Control Register i (IRQCRi) (i = 0 to 15)

Address(es): ICU.IRQCR0 4000 6000h, ICU.IRQCR1 4000 6001h, ICU.IRQCR2 4000 6002h, ICU.IRQCR3 4000 6003h, ICU.IRQCR4 4000 6004h, ICU.IRQCR5 4000 6005h, ICU.IRQCR6 4000 6006h, ICU.IRQCR7 4000 6007h ICU.IRQCR8 4000 6008h, ICU.IRQCR9 4000 6009h, ICU.IRQCR10 4000 600Ah, ICU.IRQCR11 4000 600Bh, ICU.IRQCR12 4000 600Ch, ICU.IRQCR13 4000 600Dh, ICU.IRQCR14 4000 600Eh, ICU.IRQCR15 4000 600Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	FLTEN	—	FCLKSEL[1:0]		—	—	IRQMD[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	IRQMD[1:0]	IRQi Detection Sense Select	b1 b0 0 0: Falling edge 0 1: Rising edge 1 0: Rising and falling edges 1 1: Low level.	R/W
b3, b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b5, b4	FCLKSEL[1:0]	IRQi Digital Filter Sampling Clock Select	b5 b4 0 0: PCLKB 0 1: PCLKB/8 1 0: PCLKB/32 1 1: PCLKB/64.	R/W
b6	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b7	FLTEN	IRQi Digital Filter Enable	0: Disable 1: Enable.	R/W

IRQCRi register changes must satisfy the following conditions:

- For a CPU interrupt or DTC trigger:
  Change the IRQCRi register setting before setting the target IELSRn register (n = 0 to 95).
  You can change the register values only when the IELSRn.IELS[8:0] bits are 000h.
- For a DMAC trigger:
  Change the IRQCRi register setting before setting the target DELSRn register (n = 0 to 7).
  You can change the register values only when the DELSRn.DELR[8:0] bits are 000h.
- For a wakeup enable signal:
  Change the IRQCRi register setting before setting the target WUPEN.IRQWUPENn bit (n = 0 to 15).
  You can only change the register values when the target WUPEN.IRQWUPENn bit is 0.

IRQMD[1:0] bits (IRQi Detection Sense Select)

The IRQMD[1:0] bits set the detection sensing method for the IRQi external pin interrupt sources. For more information on the settings, see section 14.4.4, External Pin Interrupts.

FCLKSEL[1:0] bits (IRQi Digital Filter Sampling Clock Select)

The FCLKSEL[1:0] bits select the digital filter sampling clock for the IRQi external pin interrupt requests, selectable to:

- PCLKB (every cycle)
- PCLKB/8 (once every eight cycles)
- PCLKB/32 (once every 32 cycles)
- PCLKB/64 (once every 64 cycles).

For details on the digital filter, see section 14.4.3, Digital Filter.

FLTEN bit (IRQi Digital Filter Enable)

The FLTEN bit enables the digital filter used for the IRQi external pin interrupt sources. The filter is enabled when FLTEN is 1 and disabled when FLTEN is 0. The IRQi pin level is sampled at the cycle specified in FCLKSEL[1:0].

14.2.1 IRQ控制寄存器i(IRQCRi)(i=0到15)

Address(es): ICU.IRQCR0 4000 6000h, ICU.IRQCR1 4000 6001h, ICU.IRQCR2 4000 6002h, ICU.IRQCR3 4000 6003h, ICU.IRQCR4 4000 6004h, ICU.IRQCR5 4000 6005h, ICU.IRQCR6 4000 6006h, ICU.IRQCR7 4000 6007h ICU.IRQCR8 4000 6008h, ICU.IRQCR9 4000 6009h, ICU.IRQCR10 4000 600Ah, ICU.IRQCR11 4000 600Bh, ICU.IRQCR12 4000 600Ch, ICU.IRQCR13 4000 600Dh, ICU.IRQCR14 4000 600Eh, ICU.IRQCR15 4000 600Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	FLTEN	—	FCLKSEL[1:0]		—	—	IRQMD[1:0]	
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b1, b0	IRQMD[1:0]	IRQi检测检测选择	b1 b0 0 0：下降沿 0 1：上升沿 1 0：上升沿和下降沿 1 1：低电平。	R/W
b3, b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b5, b4	FCLKSEL[1:0]	IRQi数字滤波器采样时钟 Select	b5 b4 0 0: PCLKB 0 1: PCLKB/8 1 0: PCLKB/32 1 1: PCLKB/64.	R/W
b6	—	Reserved	该位读取为0。写入值应为0。	R/W
b7	FLTEN	IRQi数字滤波器启用	0：禁用1 ：启用。	R/W

IRQCRi寄存器变更必须满足以下条件：

- 对于CPU中断或DTC触发器：
  在设置目标IELSRn寄存器（n=0到95）之前更改IRQCRi寄存器设置。
  仅当IELSRn.IELS[8:0]位为000h时才能更改寄存器值。
- For a DMAC trigger:
  在设置目标DELSRn寄存器（n=0到7）之前更改IRQCRi寄存器设置。
  只有当DELSRn.DELR[8:0]位为000h时，您才能更改寄存器值。
- 对于唤醒使能信号：
  在设置目标WUPEN.IRQWUPENn位（n=0到15）之前更改IRQCRi寄存器设置。
  只有当目标WUPEN.IRQWUPENn位为0时，您才能更改寄存器值。

IRQMD[1:0]位（IRQi检测检测选择）

IRQMD[1:0]位设置IRQi外部引脚中断源的检测检测方法。有关设置的更多信息，请参见第14.4.4节，外部引脚中断。

FCLKSEL[1:0]位（IRQi数字滤波器采样时钟选择）

FCLKSEL[1:0]位为IRQi外部引脚中断请求选择数字滤波器采样时钟，可选择：

- PCLKB (every cycle)
- PCLKB8（每八个周期一次）
- PCLKB/32 (once every 32 cycles)
- PCLKB/64 (once every 64 cycles).

有关数字滤波器的详细信息，请参阅第14.4.3节，数字滤波器。

FLTEN位（IRQi数字滤波器使能）

FLTEN位使能用于IRQi外部引脚中断源的数字滤波器。当FLTEN为1时使能滤波器，当FLTEN为0时禁用滤波器。IRQi引脚电平在FCLKSEL[1:0]中指定的周期进行采样。

When the sampled level matches three times, the output level from the digital filter changes. For details on the digital filter, see section 14.4.3, Digital Filter.

14.2.2 Non-Maskable Interrupt Status Register (NMISR)

Address(es): ICU.NMISR 4000 6140h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	SPEST	BUSMST	BUSSST	RECCST	RPEST	NMIST	OSTST	—	—	LVD2ST	LVD1ST	WDTST	IWDTST
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	IWDTST	IWDT Underflow/Refresh Error Status Flag	0: Interrupt not requested 1: Interrupt requested.	R
b1	WDTST	WDT Underflow/Refresh Error Status Flag	0: Interrupt not requested 1: Interrupt requested.	R
b2	LVD1ST	Voltage Monitor 1 Interrupt Status Flag	0: Interrupt not requested 1: Interrupt requested.	R
b3	LVD2ST	Voltage Monitor 2 Interrupt Status Flag	0: Interrupt not requested 1: Interrupt requested.	R
b5, b4	—	Reserved	These bits are read as 0.	R
b6	OSTST	Main Oscillation Stop Detection Interrupt Status Flag	0: Interrupt not requested for main oscillation stop 1: Interrupt requested for main oscillation stop.	R
b7	NMIST	NMI Status Flag	0: NMI pin interrupt not requested 1: NMI pin interrupt requested.	R
b8	RPEST	SRAM Parity Error Interrupt Status Flag	0: Interrupt not requested 1: Interrupt requested.	R
b9	RECCST	SRAM ECC Error Interrupt Status Flag	0: Interrupt not requested 1: Interrupt requested.	R
b10	BUSSST	MPU Bus Slave Error Interrupt Status Flag	0: Interrupt not requested 1: Interrupt requested.	R
b11	BUSMST	MPU Bus Master Error Interrupt Status Flag	0: Interrupt not requested 1: Interrupt requested.	R
b12	SPEST	CPU Stack Pointer Monitor Interrupt Status Flag	0: Interrupt not requested 1: Interrupt requested.	R
b15 to b13	—	Reserved	These bits are read as 0.	R

The NMISR register monitors the status of non-maskable interrupt sources. Writes to the NMISR register are ignored. The setting in the Non-Maskable Interrupt Enable Register (NMIER) does not affect the status flags in this register. Before the end of the non-maskable interrupt handler, check that all of the bits in this register are set to 0 to confirm that no other NMI requests have occurred during handler processing.

IWDTST flag (IWDT Underflow/Refresh Error Status Flag)

The IWDTST flag indicates an IWDT underflow/refresh error interrupt request. It is read-only and cleared by the NMICLR.IWDTCLR bit.

[Setting condition]

When an IWDT underflow/refresh error interrupt occurs and this interrupt source is enabled.

[Clearing condition]

When 1 is written to the NMICLR.IWDTCLR bit.

WDTST flag (WDT Underflow/Refresh Error Status Flag)

The WDTST flag indicates a WDT underflow/refresh error interrupt request. It is read-only and cleared by the

当采样电平匹配3次时，数字滤波器的输出电平会发生变化。有关数字滤波器的详细信息，请参阅第14.4.3节，数字滤波器。

14.2.2 不可屏蔽中断状态寄存器(NMISR)

Address(es): ICU.NMISR 4000 6140h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	SPEST	BUSMST	BUSSST	RECCST	RPEST	NMIST	OSTST	—	—	LVD2ST	LVD1ST	WDTST	IWDTST
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	IWDTST	IWDT下溢刷新错误状态标志	0：未请求中断1：请求中断。	R
b1	WDTST	WDT下溢刷新错误状态标志	0：未请求中断1：请求中断。	R
b2	LVD1ST	电压监视器1中断状态标志	0：未请求中断1：请求中断。	R
b3	LVD2ST	电压监视器2中断状态标志	0：未请求中断1：请求中断。	R
b5, b4	—	Reserved	这些位读为0。	R
b6	OSTST	主振荡停止检测中断状态标志	0：主振荡停止时不请求中断1：主振荡停止时请求中断。	R
b7	NMIST	NMI状态标志	0：未请求NMI引脚中断1：请求了NMI引脚中断。	R
b8	RPEST	SRAM奇偶校验错误中断状态标志	0：未请求中断1：请求中断。	R
b9	RECCST	SRAMECC错误中断状态标志	0：未请求中断1：请求中断。	R
b10	BUSSST	MPU总线从机错误中断状态标志	0：未请求中断1：请求中断。	R
b11	BUSMST	MPU总线主机错误中断状态标志	0：未请求中断1：请求中断。	R
b12	SPEST	CPU堆栈指针监视器中断状态Flag	0：未请求中断1：请求中断。	R
b15 to b13	—	Reserved	这些位读为0。	R

NMISR寄存器监视不可屏蔽中断源的状态。忽略对NMISR寄存器的写入。
不可屏蔽中断使能寄存器(NMIER)中的设置不会影响该寄存器中的状态标志。
在不可屏蔽中断处理程序结束之前，检查该寄存器中的所有位是否都设置为0，以确认在处理程序处理期间没有发生其他NMI请求。

IWDTST标志（IWDT下溢刷新错误状态标志）

IWDTST标志指示IWDT下溢刷新错误中断 请求。它是只读的并由NMICLR.IWDTCLR bit.

[Setting condition]

当IWDT下溢刷新错误中断 发生并且该中断源被使能时。

[Clearing condition]

当1写入NMICLR.IWDTCLR位时。

WDTST标志（WDT下溢刷新错误状态标志）

WDTST标志指示WDT下溢刷新错误中断 请求。它是只读的并由

NMICLR.WDTCLR bit.

[Setting condition]

When a WDT underflow/refresh error interrupt occurs.

[Clearing condition]

When 1 is written to the NMICLR.WDTCLR bit.

LVD1ST flag (Voltage Monitor 1 Interrupt Status Flag)

The LVD1ST flag indicates a request for voltage monitor 1 interrupt. It is read-only and cleared by the NMICLR.LVD1CLR bit.

[Setting condition]

When a voltage monitor 1 interrupt occurs and this interrupt source is enabled.

[Clearing condition]

When 1 is written to the NMICLR.LVD1CLR bit.

LVD2ST flag (Voltage Monitor 2 Interrupt Status Flag)

The LVD2ST flag indicates a request for voltage monitor 2 interrupt. It is read-only and cleared by the NMICLR.LVD2CLR bit.

[Setting condition]

When a voltage monitor 2 interrupt occurs and this interrupt source is enabled.

[Clearing condition]

When 1 is written to the NMICLR.LVD2CLR bit.

OSTST flag (Main Oscillation Stop Detection Interrupt Status Flag)

The OSTST flag indicates a main oscillation stop detection interrupt request. It is read-only and cleared by the NMICLR.OSTCLR bit.

[Setting condition]

When an oscillation stop detection interrupt occurs.

[Clearing condition]

When 1 is written to the NMICLR.OSTCLR bit.

NMIST flag (NMI Status Flag)

The NMIST flag indicates an NMI pin interrupt request. It is read-only and cleared by the NMICLR.NMICLR bit.

[Setting condition]

When an edge specified in the NMICR.NMIMD bit is input to the NMI pin.

[Clearing condition]

When 1 is written to the NMICLR.NMICLR bit.

RPEST flag (SRAM Parity Error Interrupt Status Flag)

The RPEST flag indicates an SRAM parity error interrupt request.

[Setting condition]

When an interrupt occurs in response to an SRAM parity error.

[Clearing condition]

When 1 is written to the NMICLR.RPECLR bit.

NMICLR.WDTCLR bit.

[Setting condition]

当WDT下溢刷新错误中断　　发生时。

[Clearing condition]

当1写入NMICLR.WDTCLR位时。

LVD1ST标志（电压监视器1中断状态标志）

LVD1ST标志指示电压监视器1中断请求。它是只读的并由NMICLR.LVD1CLR bit.

[Setting condition]

当电压监视器1中断发生并且该中断源被使能时。

[Clearing condition]

当1写入NMICLR.LVD1CLR位时。

LVD2ST标志（电压监视器2中断状态标志）

LVD2ST标志指示电压监视器2中断请求。它是只读的并由NMICLR.LVD2CLR bit.

[Setting condition]

当电压监视器2中断发生并且该中断源被启用时。

[Clearing condition]

当1写入NMICLR.LVD2CLR位时。

OSTST标志（主振荡停止检测中断状态标志）

OSTST标志表示主振荡停止检测中断请求。它是只读的并由NMICLR.OSTCLR bit.

[Setting condition]

发生振荡停止检测中断时。

[Clearing condition]

当1写入NMICLR.OSTCLR位时。

NMIST标志（NMI状态标志）

NMIST标志指示NMI引脚中断请求。它是只读的，由NMICLR.NMICLR位清零。

[Setting condition]

当NMICR.NMIMD位中指定的边沿输入到NMI引脚时。

[Clearing condition]

当1写入NMICLR.NMICLR位时。

RPEST标志（SRAM奇偶校验错误中断状态标志）

RPEST标志指示SRAM奇偶校验错误中断请求。

[Setting condition]

当响应SRAM奇偶校验错误而发生中断时。

[Clearing condition]

当1写入NMICLR.RPECLR位时。

RECCST flag (SRAM ECC Error Interrupt Status Flag)

The RECCST flag indicates an SRAM ECC error interrupt request.

[Setting condition]

When an interrupt occurs in response to an SRAM ECC error.

[Clearing condition]

When 1 is written to the NMICLR.RECCCLR bit.

BUSSST flag (MPU Bus Slave Error Interrupt Status Flag)

The BUSSST flag indicates a bus slave error interrupt request.

[Setting condition]

When an interrupt occurs in response to a bus slave error.

[Clearing condition]

When 1 is written to the NMICLR.BUSSCLR bit.

BUSMST flag (MPU Bus Master Error Interrupt Status Flag)

The BUSMST flag indicates a bus master error interrupt request.

[Setting condition]

When an interrupt occurs in response to a bus master error.

[Clearing condition]

When 1 is written to the NMICLR.BUSMCLR bit.

SPEST flag (CPU Stack Pointer Monitor Interrupt Status Flag)

The SPEST flag indicates a CPU stack pointer monitor interrupt request.

[Setting condition]

When an interrupt occurs in response to a CPU stack pointer monitor error.

[Clearing condition]

When 1 is written to the NMICLR.SPECLR bit.

14.2.3 Non-Maskable Interrupt Enable Register (NMIER)

Address(es): ICU.NMIER 4000 6120h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	SPEEN	BUSMEN	BUSSEN	RECCEN	RPEEN	NMIEN	OSTEN	—	—	LVD2EN	LVD1EN	WDTEN	IWDTEN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	IWDTEN	IWDT Underflow/Refresh Error Interrupt Enable	0: Disable 1: Enable.	R/(W) *1, *2
b1	WDTEN	WDT Underflow/Refresh Error Interrupt Enable	0: Disable 1: Enable.	R/(W) *1, *2
b2	LVD1EN	Voltage Monitor 1 Interrupt Enable	0: Disable 1: Enable.	R/(W) *1, *2
b3	LVD2EN	Voltage Monitor 2 Interrupt Enable	0: Disable 1: Enable.	R/(W) *1, *2
b5 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

RECCST标志（SRAMECC错误中断状态标志）

RECCST标志指示SRAMECC错误中断请求。

[Setting condition]

当响应SRAMECC错误而发生中断时。

[Clearing condition]

当1写入NMICLR.RECCCLR位时。

BUSSST标志（MPU总线从机错误中断状态标志）

BUSSST标志指示总线从机错误中断请求。

[Setting condition]

当响应总线从机错误而发生中断时。

[Clearing condition]

当1写入NMICLR.BUSSCLR位时。

BUSMST标志（MPU总线主机错误中断状态标志）

BUSMST标志指示总线主机错误中断请求。

[Setting condition]

当响应总线主机错误而发生中断时。

[Clearing condition]

当1写入NMICLR.BUSMCLR位时。

SPEST标志（CPU堆栈指针监视器中断状态标志）

SPEST标志指示CPU堆栈指针监视中断请求。

[Setting condition]

当响应CPU堆栈指针监视器错误而发生中断时。

[Clearing condition]

当1写入NMICLR.SPECLR位时。

14.2.3 不可屏蔽中断使能寄存器(NMIER)

Address(es): ICU.NMIER 4000 6120h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	SPEEN	BUSMEN	BUSSEN	RECCEN	RPEEN	NMIEN	OSTEN	—	—	LVD2EN	LVD1EN	WDTEN	IWDTEN
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	IWDTEN	IWDT下溢刷新错误中断 Enable	0：禁用1 ：启用。	R/(W) *1, *2
b1	WDTEN	WDT下溢刷新错误中断 Enable	0：禁用1 ：启用。	R/(W) *1, *2
b2	LVD1EN	电压监视器1中断使能	0：禁用1 ：启用。	R/(W) *1, *2
b3	LVD2EN	电压监视器2中断使能	0：禁用1 ：启用。	R/(W) *1, *2
b5 to b4	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Bit	Symbol	Bit name	Description	R/W
b6	OSTEN	Oscillation Stop Detection Interrupt Enable	0: Disable for main oscillation 1: Enable for main oscillation.	R/(W) *1, *2
b7	NMIEN	NMI Pin Interrupt Enable	0: Disable 1: Enable.	R/(W) *1
b8	RPEEN	SRAM Parity Error Interrupt Enable	0: Disable 1: Enable.	R/(W) *1, *2
b9	RECCEN	SRAM ECC Error Interrupt Enable	0: Disable 1: Enable.	R/(W) *1, *2
b10	BUSSEN	MPU Bus Slave Error Interrupt Enable	0: Disable 1: Enable.	R/(W) *1, *2
b11	BUSMEN	MPU Bus Master Error Interrupt Enable	0: Disable 1: Enable.	R/(W) *1, *2
b12	SPEEN	CPU Stack Pointer Monitor Interrupt Enable	0: Disable 1: Enable.	R/(W) *1, *2
b15 to b13	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. A 1 can be written to this bit only once after reset, and subsequent write accesses are invalid. Writing 0 to this bit is invalid.
Note 2. Do not write 1 to this bit when the source is used as an event signal.

IWDTEN bit (IWDT Underflow/Refresh Error Interrupt Enable)

The IWDTEN bit enables IWDT underflow/refresh error interrupts as an NMI trigger.

WDTEN bit (WDT Underflow/Refresh Error Interrupt Enable)

The WDTEN bit enables WDT underflow/refresh error interrupts as an NMI trigger.

LVD1EN bit (Voltage Monitor 1 Interrupt Enable)

The LVD1EN bit enables voltage monitor 1 interrupts as an NMI trigger.

LVD2EN bit (Voltage Monitor 2 Interrupt Enable)

The LVD2EN bit enables voltage monitor 2 interrupts as an NMI trigger.

OSTEN bit (Oscillation Stop Detection Interrupt Enable)

The OSTEN bit enables main oscillation stop detection interrupts as an NMI trigger.

NMIEN bit (NMI Pin Interrupt Enable)

The NMIEN bit enables NMI pin interrupts as an NMI trigger.

RPEEN bit (SRAM Parity Error Interrupt Enable)

The RPEEN bit enables SRAM parity error interrupts as an NMI trigger.

RECCEN bit (SRAM ECC Error Interrupt Enable)

The RECCEN bit enables SRAM ECC error interrupts as an NMI trigger.

BUSSEN bit (MPU Bus Slave Error Interrupt Enable)

The BUSSEN bit enables bus slave error interrupts as an NMI trigger.

BUSMEN bit (MPU Bus Master Error Interrupt Enable)

The BUSMEN bit enables bus master error interrupts as an NMI trigger.

SPEEN bit (CPU Stack Pointer Monitor Interrupt Enable)

The SPEEN bit enables CPU stack pointer monitor interrupts as an NMI trigger.

Bit	Symbol	位名称	Description	R/W
b6	OSTEN	振荡停止检测中断Enable	0：主振荡禁止1：主振荡使能。	R/(W) *1, *2
b7	NMIEN	NMI引脚中断使能	0：禁用1 ：启用。	R/(W) *1
b8	RPEEN	SRAM奇偶校验错误中断使能	0：禁用1 ：启用。	R/(W) *1, *2
b9	RECCEN	SRAMECC错误中断使能	0：禁用1 ：启用。	R/(W) *1, *2
b10	BUSSEN	MPU总线从机错误中断使能	0：禁用1 ：启用。	R/(W) *1, *2
b11	BUSMEN	MPU总线主机错误中断使能	0：禁用1 ：启用。	R/(W) *1, *2
b12	SPEEN	CPU堆栈指针监视器中断Enable	0：禁用1 ：启用。	R/(W) *1, *2
b15 to b13	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 复位后该位只能写入一次1，后续写访问无效。向该位写入0无效。
Note 2. 当源用作事件信号时，不要向该位写入1。

IWDTEN位（IWDT下溢刷新错误中断 使能）

IWDTEN位使能IWDT下溢刷新错误中断 作为NMI触发。

WDTEN位（WDT下溢刷新错误中断 使能）

WDTEN位使能WDT下溢刷新错误中断 作为NMI触发。

LVD1EN位（电压监视器1中断允许）

LVD1EN位使能电压监视器1中断作为NMI触发。

LVD2EN位（电压监视器2中断允许）

LVD2EN位使能电压监视器2中断作为NMI触发。

OSTEN位（振荡停止检测中断使能）

OSTEN位使能主振荡停止检测中断作为NMI触发。

NMIEN位（NMI引脚中断允许）

NMIEN位使能NMI引脚中断作为NMI触发器。

RPEEN位（SRAM奇偶校验错误中断使能）

RPEEN位启用SRAM奇偶校验错误中断作为NMI触发器。

RECCEN位（SRAMECC错误中断使能）

RECCEN位启用SRAMECC错误中断作为NMI触发器。

BUSSEN位（MPU总线从机错误中断使能）

BUSSEN位使能总线从机错误中断作为NMI触发器。

BUSMEN位（MPU总线主机错误中断使能）

BUSMEN位启用总线主机错误中断作为NMI触发器。

SPEEN位（CPU堆栈指针监视器中断使能）

SPEEN位使能CPU堆栈指针监视中断作为NMI触发器。

14.2.4 Non-Maskable Interrupt Status Clear Register (NMICLR)

Address(es): ICU.NMICLR 4000 6130h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	SPECLR	BUSMCLR	BUSSCLR	RECCCLR	RPECLR	NMICLR	OSTCLR	—	—	LVD2CLR	LVD1CLR	WDTCLR	IWDTCLR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	IWDTCLR	IWDT Clear	0: No effect 1: Clear the NMISR.IWDTST flag.	R/(W)*1
b1	WDTCLR	WDT Clear	0: No effect 1: Clear the NMISR.WDTST flag.	R/(W)*1
b2	LVD1CLR	LVD1 Clear	0: No effect 1: Clear the NMISR.LVD1ST flag.	R/(W)*1
b3	LVD2CLR	LVD2 Clear	0: No effect 1: Clear the NMISR.LVD2ST flag.	R/(W)*1
b5 to b4	—	Reserved	The write value should be 0.	R/(W)*1
b6	OSTCLR	OST Clear	0: No effect 1: Clear the NMISR.OSTST flag.	R/(W)*1
b7	NMICLR	NMI Clear	0: No effect 1: Clear the NMISR.NMIST flag.	R/(W)*1
b8	RPECLR	SRAM Parity Error Clear	0: No effect 1: Clear the NMISR.RPEST flag.	R/(W)*1
b9	RECCCLR	SRAM ECC Error Clear	0: No effect 1: Clear the NMISR.RECCST flag.	R/(W)*1
b10	BUSSCLR	Bus Slave Error Clear	0: No effect 1: Clear the NMISR.BUSSST flag.	R/(W)*1
b11	BUSMCLR	Bus Master Error Clear	0: No effect 1: Clear the NMISR.BUSMST flag.	R/(W)*1
b12	SPECLR	CPU Stack Pointer Monitor Interrupt Clear	0: No effect 1: Clear the NMISR.SPEST flag.	R/(W)*1
b15 to b13	—	Reserved	These bits are read as 0. The write value should be 0.	R/(W)*1

Note 1. Only 1 can be written to this bit.

IWDTCLR bit (IWDT Clear)

Writing 1 to the IWDTCLR bit clears the NMISR.IWDTST flag. This bit is read as 0.

WDTCLR bit (WDT Clear)

Writing 1 to the WDTCLR bit clears the NMISR.WDTST flag. This bit is read as 0.

LVD1CLR bit (LVD1 Clear)

Writing 1 to the LVD1CLR bit clears the NMISR.LVD1ST flag. This bit is read as 0.

LVD2CLR bit (LVD2 Clear)

Writing 1 to the LVD2CLR bit clears the NMISR.LVD2ST flag. This bit is read as 0.

OSTCLR bit (OST Clear)

Writing 1 to the OSTCLR bit clears the NMISR.OSTST flag. This bit is read as 0.

NMICLR bit (NMI Clear)

Writing 1 to the NMICLR bit clears the NMISR.NMIST flag. This bit is read as 0.

14.2.4 不可屏蔽中断状态清除寄存器(NMICLR)

Address(es): ICU.NMICLR 4000 6130h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	SPECLR	BUSMCLR	BUSSCLR	RECCCLR	RPECLR	NMICLR	OSTCLR	—	—	LVD2CLR	LVD1CLR	WDTCLR	IWDTCLR
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	IWDTCLR	IWDT Clear	0：无效1：清除NMISR.IWDTST标志。	R/(W)*1
b1	WDTCLR	WDT Clear	0：无效1：清除NMISR.WDTST标志。	R/(W)*1
b2	LVD1CLR	LVD1 Clear	0：无效1：清除NMISR.LVD1ST标志。	R/(W)*1
b3	LVD2CLR	LVD2 Clear	0：无效1：清除NMISR.LVD2ST标志。	R/(W)*1
b5 to b4	—	Reserved	写入值应为0。	R/(W)*1
b6	OSTCLR	原声清除	0：无效1：清除NMISR.OSTST标志。	R/(W)*1
b7	NMICLR	NMI Clear	0：无效1：清除NMISR.NMIST标志。	R/(W)*1
b8	RPECLR	SRAM奇偶校验错误清除	0：无效1：清除NMISR.RPEST标志。	R/(W)*1
b9	RECCCLR	SRAMECC错误清除	0：无效1：清除NMISR.RECCST标志。	R/(W)*1
b10	BUSSCLR	总线从机错误清除	0：无效1：清除NMISR.BUSSST标志。	R/(W)*1
b11	BUSMCLR	总线主机错误清除	0：无效1：清除NMISR.BUSMST标志。	R/(W)*1
b12	SPECLR	CPU堆栈指针监视器中断Clear	0：无效1：清除NMISR.SPEST标志。	R/(W)*1
b15 to b13	—	Reserved	这些位被读取为0。写入值应为0。	R/(W)*1

Note 1. 该位只能写入1。

IWDTCLR位（IWDT清除）

将1写入IWDTCLR位会清除NMISR.IWDTST标志。该位读为0。

WDTCLR位（WDT清除）

将1写入WDTCLR位会清除NMISR.WDTST标志。该位读为0。

LVD1CLR位（LVD1清零）

将1写入LVD1CLR位会清除NMISR.LVD1ST标志。该位读为0。

LVD2CLR位（LVD2清除）

将1写入LVD2CLR位会清除NMISR.LVD2ST标志。该位读为0。

OSTCLR位（OST清除）

将1写入OSTCLR位会清除NMISR.OSTST标志。该位读为0。

NMICLR位（NMI清除）

将1写入NMICLR位会清除NMISR.NMIST标志。该位读为0。

RPECLR bit (SRAM Parity Error Clear)

Writing 1 to the RPECLR bit clears the NMISR.RPEST flag. This bit is read as 0.

RECCCLR bit (SRAM ECC Error Clear)

Writing 1 to the RECCCLR bit clears the NMISR.RECCST flag. This bit is read as 0.

BUSSCLR bit (Bus Slave Error Clear)

Writing 1 to the BUSSCLR bit clears the NMISR.BUSSST flag. This bit is read as 0.

BUSMCLR bit (Bus Master Error Clear)

Writing 1 to the BUSMCLR bit clears the NMISR.BUSMSST flag. This bit is read as 0.

SPECLR bit (CPU Stack Pointer Monitor Interrupt Clear)

Writing 1 to the SPECLR bit clears the NMISR.SPEST flag. This bit is read as 0.

14.2.5 NMI Pin Interrupt Control Register (NMICR)

Address(es): ICU.NMICR 4000 6100h

	b7	b6	b5	b4	b3	b2	b1	b0
	NFLTEN	—	NFCLKSEL[1:0]		—	—	—	NMIMD
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	NMIMD	NMI Detection Set	0: Falling edge 1: Rising edge.	R/W
b3 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b5, b4	NFCLKSEL[1:0]	NMI Digital Filter Sampling Clock Select	b5 b4 0 0: PCLKB 0 1: PCLKB/8 1 0: PCLKB/32 1 1: PCLKB/64.	R/W
b6	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b7	NFLTEN	NMI Digital Filter Enable	0: Disable 1: Enable.	R/W

Change the NMICR register settings before enabling NMI pin interrupts (before setting NMIER.NMIEN to 1).

NMIMD bit (NMI Detection Set)

The NMIMD bit selects the detection sensing method for NMI pin interrupts.

NFCLKSEL[1:0] bits (NMI Digital Filter Sampling Clock Select)

The NFCLKSEL[1:0] bits select the digital filter sampling clock for NMI pin interrupts, selectable to:

- PCLKB (every cycle)
- PCLKB/8 (once every eight cycles)
- PCLKB/32 (once every 32 cycles)
- PCLKB/64 (once every 64 cycles).

For details on the digital filter, see section 14.4.3, Digital Filter.

NFLTEN bit (NMI Digital Filter Enable)

The NFLTEN bit enables the digital filter used for NMI pin interrupts. The filter is enabled when NFLTEN is 1 and disabled when NFLTEN is 0. The NMI pin level is sampled at the cycle specified in NMIFLTC.NFCLKSEL[1:0]. When

RPECLR位（SRAM奇偶校验错误清除）

将1写入RPECLR位会清除NMISR.RPEST标志。该位读为0。

RECCCLR位（SRAMECC错误清除）

将1写入RECCCLR位会清除NMISR.RECCST标志。该位读为0。

BUSSCLR位（总线从机错误清除）

将1写入BUSSCLR位会清除NMISR.BUSSST标志。该位读为0。

BUSMCLR位（总线主机错误清除）

将1写入BUSMCLR位会清除NMISR.BUSMSST标志。该位读为0。

SPECLR位（CPU堆栈指针监视器中断清除）

将1写入SPECLR位会清除NMISR.SPEST标志。该位读为0。

14.2.5 NMI引脚中断控制寄存器(NMICR)

Address(es): ICU.NMICR 4000 6100h

	b7	b6	b5	b4	b3	b2	b1	b0
	NFLTEN	—	NFCLKSEL[1:0]		—	—	—	NMIMD
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	NMIMD	NMI检测集	0：下降沿1： 上升沿。	R/W
b3 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b5, b4	NFCLKSEL[1:0]	NMI数字滤波器采样时钟 Select	b5 b4 0 0: PCLKB 0 1: PCLKB/8 1 0: PCLKB/32 1 1: PCLKB/64.	R/W
b6	—	Reserved	该位读取为0。写入值应为0。	R/W
b7	NFLTEN	NMI数字滤波器启用	0：禁用1 ：启用。	R/W

在启用NMI引脚中断之前（在将NMIER.NMIEN设置为1之前）更改NMICR寄存器设置。

NMIMD位（NMI检测集）

NMIMD位选择NMI引脚中断的检测检测方法。

NFCLKSEL[1:0]位（NMI数字滤波器采样时钟选择）

NFCLKSEL[1:0]位选择用于NMI引脚中断的数字滤波器采样时钟，可选择：

- PCLKB (every cycle)
- PCLKB8（每八个周期一次）
- PCLKB/32 (once every 32 cycles)
- PCLKB/64 (once every 64 cycles).

有关数字滤波器的详细信息，请参阅第14.4.3节，数字滤波器。

NFLTEN位（NMI数字滤波器使能）

NFLTEN位使能用于NMI引脚中断的数字滤波器。滤波器在NFLTEN为1时启用，在NFLTEN为0时禁用。NMI引脚电平以NMIFLTC.NFCLKSEL[1:0]中指定的周期进行采样。什么时候

the sampled level matches three times, the output level from the digital filter changes. For details on the digital filter, see section 14.4.3, Digital Filter.

14.2.6 ICU Event Link Setting Register n (IELSRn) (n = 0 to 95)

Address(es): ICU.IELSR0 4000 6300h, ICU.IELSR1 4000 6304h, ICU.IELSR2 4000 6308h, ICU.IELSR3 4000 630Ch.....
.....ICU.IELSR92 4000 6470h, ICU.IELSR93 4000 6474h, ICU.IELSR94 4000 6478h, ICU.IELSR95 4000 647Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	DTCE	—	—	—	—	—	—	—	IR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	IELS[8:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b8 to b0	IELS[8:0]	ICU Event Link Select	b8 b0 000000000:Disable interrupts to the associated NVIC or DTC module 000000001 to 111111111: Event signal number to be linked. For details, see Table 14.4.	R/W*1
b15 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b16	IR	Interrupt Status Flag	0: No interrupt request occurred 1: Interrupt request occurred.	R/(W)*2
b23 to b17	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b24	DTCE	DTC Activation Enable	0: Disable 1: Enable.	R/W
b31 to b25	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. This register requires halfword or word access.
Note 2. Writing 1 to the IR flag is prohibited.

The IELSRn register selects the IRQ source used by the NVIC. For details, see Table 14.4. IELSRn, where n = 0 to 95, corresponds to the NVIC IRQ input source numbers 0 to 95.

IELS[8:0] bits (ICU Event Link Select)

The IELS[8:0] bits link an event signal to the associated NVIC or DTC module. All IELS[8:0] bits must be written to simultaneously.

IR flag (Interrupt Status Flag)

The IR flag indicates an individual interrupt request from the event specified in IELS[8:0].

[Setting condition]

When an interrupt request is received from the associated peripheral module or IRQi pin.

[Clearing conditions]

When 0 is written to the bit. DTCE must be set to 0 before writing 0 to the IR flag.

To clear the IR flag:

1. Negate the input interrupt signal.
2. Read access the peripheral once and wait for 2 clock cycles of the target module clock.
3. Clear the IR flag by writing 0.

采样电平匹配3次，数字滤波器的输出电平发生变化。有关数字滤波器的详细信息，请参阅第14.4.3节，数字滤波器。

14.2.6 ICU事件链接设置寄存器n(IELSRn)(n=0到95)

Address(es): ICU.IELSR0 4000 6300h, ICU.IELSR1 4000 6304h, ICU.IELSR2 4000 6308h, ICU.IELSR3 4000 630Ch.....
.....ICU.IELSR92 4000 6470h, ICU.IELSR93 4000 6474h, ICU.IELSR94 4000 6478h, ICU.IELSR95 4000 647Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	DTCE	—	—	—	—	—	—	—	IR
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	IELS[8:0]								
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b8 to b0	IELS[8:0]	ICU事件链接选择	b8b0000000000：禁用对相关NVIC或DTC模块的中断00000 0001至111111111：要链接的事件信号编号。详见表14.4。	R/W*1
b15 to b9	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b16	IR	中断状态标志	0：未发生中断请求1：发生中断请求。	R/(W)*2
b23 to b17	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b24	DTCE	DTC激活启用	0：禁用1：启用。	R/W
b31 to b25	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 该寄存器需要半字或字访问。
Note 2. 禁止向IR标志写入1。

IELSRn寄存器选择NVIC使用的IRQ源。详见表14.4。IELSRn，其中n=0到95，对应于NVICIRQ输入源编号0到95。

IELS[8:0]位（ICU事件链接选择）

IELS[8:0]位将事件信号链接到相关的NVIC或DTC模块。必须同时写入所有IELS[8:0]位。

IR标志（中断状态标志）

IR标志指示来自IELS[8:0]中指定事件的单个中断请求。

[Setting condition]

当从相关外设模块或IRQi引脚接收到中断请求时。

[Clearing conditions]

当0写入该位时。在将0写入IR标志之前，必须将DTCE设置为0。

清除IR标志：

1. 取反输入中断信号。
2. 读取访问外设一次并等待目标模块时钟的2个时钟周期。
3. 通过写入0清除IR标志。

DTCE bit (DTC Activation Enable)

When the DTCE bit is set to 1, the associated event is selected as the source for DTC activation.

[Setting condition]

When 1 is written to the DTCE bit.

[Clearing conditions]

- When the specified number of transfers is complete. For chain transfers, when the specified number of transfers for the last chain transfer is complete.
- When 0 is written to the bit.

14.2.7 DMAC Event Link Setting Register n (DELSRn) (n = 0 to 7)

Address(es): ICU.DELSR0 4000 6280h, ICU.DELSR1 4000 6284h, ICU.DELSR2 4000 6288h, ICU.DELSR3 4000 628Ch, ICU.DELSR4 4000 6290h, ICU.DELSR5 4000 6294h, ICU.DELSR6 4000 6298h, ICU.DELSR7 4000 629Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	DELS[8:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b8 to b0	DELS[8:0]	DMAC Event Link Select	b8 b0 000000000:Disable DMA start requests to the associated DMAC module 000000001 to 111111111: Event signal number to be linked. For details, see Table 14.4.	R/W*1
b15 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b16	IR	Interrupt Status Flag for DMAC	0: No interrupt request is generated 1: An interrupt request is generated.	R/(W)*2
b31 to b17	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. This register requires halfword or word access.
Note 2. Writing 1 to the IR flag is prohibited.

DELS[8:0] bits (DMAC Event Link Select)

The DELS[8:0] bits link an event signal to the DMAC module. All DELS[8:0] bits must be written to simultaneously.

IR flag (Interrupt Status Flag for DMAC)

This is the status flag of an individual DMA transfer request. This corresponds to DELS[8:0] bits of the same register.

[Setting condition]

The flag is set to 1 when a DMA transfer request is generated from the corresponding peripheral module or IRQi pin.

[Clearing conditions]

- When 0 is written to the flag.
- At the start of the DMA transfer after the DMA transfer request is issued.

DTCE位（DTC激活使能）

当DTCE位设置为1时，相关事件被选为DTC激活源。

[Setting condition]

当1写入DTCE位时。

[Clearing conditions]

- 当指定数量的传输完成时。对于链式转移，当最后一次链式转移的指定转移次数完成时。
- 当0写入该位时。

14.2.7 DMAC事件链接设置寄存器n(DELSRn)(n=0到7)

Address(es): ICU.DELSR0 4000 6280h, ICU.DELSR1 4000 6284h, ICU.DELSR2 4000 6288h, ICU.DELSR3 4000 628Ch, ICU.DELSR4 4000 6290h, ICU.DELSR5 4000 6294h, ICU.DELSR6 4000 6298h, ICU.DELSR7 4000 629Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IR
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	DELS[8:0]								
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b8 to b0	DELS[8:0]	DMAC事件链接选择	b8b0000000000：禁用对相关DMAC模块的DMA启动请求 000000001至111111111：要链接的事件信号编号。详见表14.4。	R/W*1
b15 to b9	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b16	IR	DMAC的中断状态标志	0：不产生中断请求1：产生中断请求。	R/(W)*2
b31 to b17	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 该寄存器需要半字或字访问。
Note 2. 禁止向IR标志写入1。

DELS[8:0]位（DMAC事件链接选择）

DELS[8:0]位将事件信号链接到DMAC模块。所有DELS[8:0]位必须同时写入。

IR标志（DMAC的中断状态标志）

这是单个DMA传输请求的状态标志。这对应于同一寄存器的DELS[8:0]位。

[Setting condition]

当相应外设模块或IRQi引脚产生DMA传输请求时，该标志设置为1。

[Clearing conditions]

- 当0写入标志时。
- 在发出DMA传输请求后开始DMA传输。

14.2.8 SYS Event Link Setting Register (SELSR0)

Address(es): ICU.SELSR0 4000 6200h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	SELS[8:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b8 to b0	SELS[8:0]	SYS Event Link Select	b8 b0 000000000: Disable event output to the associated low power mode module 000000001 to 111111111: Event signal number to be linked. For details, see Table 14.4.	R/W
b15 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: This register requires halfword access.

The SELSR0 register selects the events that wake the CPU from Snooze mode. You can only use the events listed in Table 14.4 checked under “Canceling Snooze using SELSR0”. Events specified in this register are defined as ICU_SNZCANCEL (02Dh) in Table 14.4. When 02Dh is set in IELSRn.IELS, the SELSR0 event interrupt occurs.

SELS[8:0] bits (SYS Event Link Select)

All SELS[8:0] bits must be written to simultaneously.

14.2.9 Wake Up Interrupt Enable Register (WUPEN)

Address(es): ICU.WUPEN 4000 61A0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	IIC0WUPEN	AGT1CBWUPEN	AGT1CAWUPEN	AGT1UDWUPEN	USBFSWUPEN	USBHSWUPEN	RTCPRDWUPEN	RTCALMWUPEN	—	ACMPHS0WUPEN	—	—	LVD2WUPEN	LVD1WUPEN	KEYWUPEN	IWDTWUPEN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	IRQWUPEN[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b15 to b0	IRQWUPEN[15:0]	IRQ Interrupt Software Standby Returns Enable	0: Disable Software Standby returns by IRQ interrupts 1: Enable Software Standby returns by IRQ interrupts.	R/W
b16	IWDTWUPEN	IWDT Interrupt Software Standby Returns Enable	0: Disable Software Standby returns by IWDT interrupts 1: Enable Software Standby returns by IWDT interrupts.	R/W
b17	KEYWUPEN	Key Interrupt Software Standby Returns Enable	0: Disable Software Standby returns by KEY interrupts 1: Enable Software Standby returns by KEY interrupts.	R/W
b18	LVD1WUPEN	LVD1 Interrupt Software Standby Returns Enable	0: Disable Software Standby returns by LVD1 interrupts 1: Enable Software Standby returns by LVD1 interrupts.	R/W
b19	LVD2WUPEN	LVD2 Interrupt Software Standby Returns Enable	0: Disable Software Standby returns by LVD2 interrupts 1: Enable Software Standby returns by LVD2 interrupts.	R/W
b21 to b20	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

14.2.8 SYS事件链接设置寄存器(SELSR0)

Address(es): ICU.SELSR0 4000 6200h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	SELS[8:0]								
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b8 to b0	SELS[8:0]	SYS事件链接选择	b8b0000000000：禁用到相关低功耗模式模块的事件输出00000000001至111111111：要链接的事件信号编号。详见表14.4。	R/W
b15 to b9	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note: 该寄存器需要半字访问。

SELSR0寄存器选择将CPU从贪睡模式唤醒的事件。您只能使用中列出的事件在“使用SELSR0取消贪睡”下检查了表14.4。该寄存器中指定的事件定义为ICU_SNZCANCEL(02Dh)在表14.4中。在IELSRn.IELS中设置02Dh时，发生SELSR0事件中断。

SELS[8:0]位（SYS事件链接选择）

所有SELS[8:0]位必须同时写入。

14.2.9 唤醒中断使能寄存器(WUPEN)

Address(es): ICU.WUPEN 4000 61A0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	IIC0WUPEN	AGT1CBWUPEN	AGT1CAWUPEN	AGT1UDWUPEN	USBFSWUPEN	USBHSWUPEN	RTCPRDWUPEN	RTCALMWUPEN	—	ACMPHS0WUPEN	—	—	LVD2WUPEN	LVD1WUPEN	KEYWUPEN	IWDTWUPEN
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	IRQWUPEN[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b15 to b0	IRQWUPEN[15:0]	IRQ中断软件待机返回使能	0：禁止通过IRQ中断返回软件待机1：使能通过IRQ中断返回软件待机。	R/W
b16	IWDTWUPEN	IWDT中断软件待机返回使能	0：禁止通过IWDT中断返回软件待机1：使能通过IWDT中断返回软件待机。	R/W
b17	KEYWUPEN	按键中断软件待机返回使能	0：禁止通过KEY中断返回软件待机1：使能通过KEY中断返回软件待机。	R/W
b18	LVD1WUPEN	LVD1中断软件待机返回使能	0：禁止通过LVD1中断返回软件待机1：使能通过LVD1中断返回软件待机。	R/W
b19	LVD2WUPEN	LVD2中断软件待机返回使能	0：禁止通过LVD2中断返回软件待机1：使能通过LVD2中断返回软件待机。	R/W
b21 to b20	—	Reserved	该位读取为0。写入值应为0。	R/W

Bit	Symbol	Bit name	Description	R/W
b22	ACMPHS0WUPEN	ACMPHS0 Interrupt Software Standby Returns Enable	0: Disable Software Standby returns by ACMPHS0 interrupts 1: Enable Software Standby returns by ACMPHS0 interrupts.	R/W
b23	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b24	RTCALMWUPEN	RTC Alarm Interrupt Software Standby Returns Enable	0: Disable Software Standby returns by RTC alarm interrupts 1: Enable Software Standby returns by RTC alarm interrupts.	R/W
b25	RTCPRDWUPEN	RTC Period Interrupt Software Standby Returns Enable	0: Disable Software Standby returns by RTC period interrupts 1: Enable Software Standby returns by RTC period interrupts.	R/W
b26	USBHSWUPEN	USBHS Interrupt Software Standby Returns Enable	0: Disable Software Standby returns by USBHS interrupts 1: Enable Software Standby returns by USBHS interrupts.	R/W
b27	USBFSWUPEN	USBFS Interrupt Software Standby Returns Enable	0: Disable Software Standby returns by USBFS interrupts 1: Enable Software Standby returns by USBFS interrupts.	R/W
b28	AGT1UDWUPEN	AGT1 Underflow Interrupt Software Standby Returns Enable	0: Disable Software Standby returns by AGT1 underflow interrupts 1: Enable Software Standby returns by AGT1 underflow interrupts.	R/W
b29	AGT1CAWUPEN	AGT1 Compare Match A Interrupt Software Standby Returns Enable	0: Disable Software Standby returns by AGT1 compare match A interrupts 1: Enable Software Standby returns by AGT1 compare match A interrupts.	R/W
b30	AGT1CBWUPEN	AGT1 Compare Match B Interrupt Software Standby Returns Enable	0: Disable Software Standby returns by AGT1 compare match B interrupts 1: Enable Software Standby returns by AGT1 compare match B interrupts.	R/W
b31	IIC0WUPEN	IIC0 Address Match Interrupt Software Standby Returns Enable	0: Disable Software Standby returns by IIC0 address match interrupts 1: Enable Software Standby returns by IIC0 address match interrupts.	R/W

The bits in this register control whether the associated interrupt can wake the CPU from Software Standby mode.

IRQWUPEN[15:0] bits (IRQ Interrupt Software Standby Returns Enable)

The IRQWUPEN[15:0] bits enable the use of IRQn interrupts to cancel Software Standby mode.

IWDTWUPEN bit (IWDT Interrupt Software Standby Returns Enable)

The IWDTWUPEN bit enables the use of IWDT interrupts to cancel Software Standby mode.

KEYWUPEN bit (Key Interrupt Software Standby Returns Enable)

The KEYWUPEN bit enables the use of key interrupts to cancel Software Standby mode.

LVD1WUPEN bit (LVD1 Interrupt Software Standby Returns Enable)

The LVD1WUPEN bit enables the use of LVD1 interrupts to cancel Software Standby mode.

LVD2WUPEN bit (LVD2 Interrupt Software Standby Returns Enable)

The LVD2WUPEN bit enables the use of LVD2 interrupts to cancel Software Standby mode.

ACMPHS0WUPEN bit (ACMPHS0 Interrupt Software Standby Returns Enable)

The ACMPHS0WUPEN bit enables the use of ACMPHS0 interrupts to cancel Software Standby mode.

Bit	Symbol	位名称	Description	R/W
b22	ACMPHS0WUPEN	ACMPHS0 Interrupt 软件待机返回 Enable	0：禁用ACMPHS0中断返回的软件待机1：启用ACMPHS0中断返回的软件待机。	R/W
b23	—	Reserved	该位读取为0。写入值应为0。	R/W
b24	RTCALMWUPEN	RTC闹钟中断 软件待机返回 Enable	0：禁止通过RTC闹钟中断返回软件待机1：使能通过RTC闹钟中断返回软件待机。	R/W
b25	RTCPRDWUPEN	RTC周期中断 软件待机返回 Enable	0：禁用RTC周期中断返回的软件待机1：启用RTC周期中断返回的软件待机。	R/W
b26	USBHSWUPEN	USBHS中断软件待机返回启用	0：禁止通过USBHS中断返回软件待机1：使能通过USBHS中断返回软件待机。	R/W
b27	USBFSWUPEN	USBFS中断软件待机返回启用	0：禁止通过USBFS中断返回软件待机1：使能通过USBFS中断返回软件待机。	R/W
b28	AGT1UDWUPEN	AGT1下溢中断软件待机返回 Enable	0：禁用AGT1下溢中断返回的软件待机1：启用AGT1下溢中断返回的软件待机。	R/W
b29	AGT1CAWUPEN	AGT1比较匹配A中断软件待机退货启用	0：禁用由AGT1比较匹配A中断返回的软件待机1：启用由AGT1比较匹配A中断返回的软件待机。	R/W
b30	AGT1CBWUPEN	AGT1比较匹配B中断软件待机退货启用	0：禁用由AGT1比较匹配B中断返回的软件待机1：启用由AGT1比较匹配B中断返回的软件待机。	R/W
b31	IIC0WUPEN	IIC0地址匹配中断软件待机退货启用	0：禁用IIC0地址匹配中断返回的软件待机1：启用IIC0地址匹配中断返回的软件待机。	R/W

该寄存器中的位控制相关中断是否可以将CPU从软件待机模式唤醒。

IRQWUPEN[15:0]位（IRQ中断软件待机返回使能）

IRQWUPEN[15:0]位允许使用IRQn中断来取消软件待机模式。

IWDTWUPEN位（IWDT中断软件待机返回使能）

IWDTWUPEN位允许使用IWDT中断来取消软件待机模式。

KEYWUPEN位（按键中断软件待机返回使能）

KEYWUPEN位允许使用按键中断来取消软件待机模式。

LVD1WUPEN位（LVD1中断软件待机返回使能）

LVD1WUPEN位允许使用LVD1中断来取消软件待机模式。

LVD2WUPEN位（LVD2中断软件待机返回使能）

LVD2WUPEN位允许使用LVD2中断来取消软件待机模式。

ACMPHS0WUPEN位（ACMPHS0中断软件待机返回使能）

ACMPHS0WUPEN位允许使用ACMPHS0中断来取消软件待机模式。

RTCALMWUPEN bit (RTC Alarm Interrupt Software Standby Returns Enable)

The RTCALMWUPEN bit enables the use of RTC alarm interrupts to cancel Software Standby mode.

RTCPRDWUPEN bit (RTC Period Interrupt Software Standby Returns Enable)

The RTCPRDWUPEN bit enables the use of RTC period interrupts to cancel Software Standby mode.

USBHSWUPEN bit (USBHS Interrupt Software Standby Returns Enable)

The USBHSWUPEN bit enables the use of USBHS interrupts to cancel Software Standby mode.

USBFSWUPEN bit (USBFS Interrupt Software Standby Returns Enable)

The USBFSWUPEN bit enables the use of USBFS interrupts to cancel Software Standby mode.

AGT1UDWUPEN bit (AGT1 Underflow Interrupt Software Standby Returns Enable)

The AGT1UDWUPEN bit enables the use of AGT1 underflow interrupts to cancel Software Standby mode.

AGT1CAWUPEN bit (AGT1 Compare Match A Interrupt Software Standby Returns Enable)

The AGT1CAWUPEN bit enables the use of AGT1 compare match A interrupts to cancel Software Standby mode.

AGT1CBWUPEN bit (AGT1 Compare Match B Interrupt Software Standby Returns Enable)

The AGT1CBWUPEN bit enables the use of AGT1 compare match B interrupts to cancel Software Standby mode.

IIC0WUPEN bit (IIC0 Address Match Interrupt Software Standby Returns Enable)

The IIC0WUPEN bit enables the use of IIC0 interrupts to cancel Software Standby mode.

14.3 Vector Table

The ICU detects two types of interrupts, maskable and non-maskable. Interrupt priorities are set up in the Arm NVIC. See the NVIC chapter of the *ARM® Cortex®-M4 Processor Technical Reference Manual* (ARM DDI 0439D).

14.3.1 Interrupt Vector Table

Table 14.3 describes the interrupt vectors. The addresses conform to the NVIC specifications.

Table 14.3 Interrupt vector table (1 of 4)

Exception number	IRQ number	Vector offset	Source	Description
0	-	000h	Arm	Initial stack pointer
1	-	004h	Arm	Initial program counter (reset vector)
2	-	008h	Arm	Non-maskable interrupt (NMI)
3	-	00Ch	Arm	Hard fault
4	-	010h	Arm	MemManage fault
5	-	014h	Arm	Bus fault
6	-	018h	Arm	Usage fault
7	-	01Ch	Arm	Reserved
8	-	020h	Arm	Reserved
9	-	024h	Arm	Reserved
10	-	028h	Arm	Reserved
11	-	02Ch	Arm	Supervisor call (SVCall)
12	-	030h	Arm	Debug Monitor
13	-	034h	Arm	Reserved
14	-	038h	Arm	Pendable request for system service (PendableSrvReq)
15	-	03Ch	Arm	System tick timer (SysTick)

RTCALMWUPEN位（RTC闹钟中断软件待机返回使能）

RTCALMWUPEN位允许使用RTC闹钟中断来取消软件待机模式。

RTCPRDWUPEN位（RTC周期中断软件待机返回使能）

RTCPRDWUPEN位允许使用RTC周期中断来取消软件待机模式。

USBHSWUPEN位（USBHS中断软件待机返回使能）

USBHSWUPEN位允许使用USBHS中断来取消软件待机模式。

USBFSWUPEN位（USBFS中断软件待机返回使能）

USBFSWUPEN位允许使用USBFS中断来取消软件待机模式。

AGT1UDWUPEN位（AGT1下溢中断软件待机返回使能）

AGT1UDWUPEN位允许使用AGT1下溢中断来取消软件待机模式。

AGT1CAWUPEN位（AGT1比较匹配中断软件待机返回使能）

AGT1CAWUPEN位允许使用AGT1比较匹配A中断来取消软件待机模式。

AGT1CBWUPEN位（AGT1比较匹配B中断软件待机返回使能）

AGT1CBWUPEN位允许使用AGT1比较匹配B中断来取消软件待机模式。

IIC0WUPEN位（IIC0地址匹配中断软件待机返回使能）

IIC0WUPEN位允许使用IIC0中断来取消软件待机模式。

14.3 向量表

ICU检测两种类型的中断，可屏蔽和不可屏蔽。中断优先级在ArmNVIC中设置。
请参阅ARM®Cortex®–M4处理器技术参考手册(ARMDDI0439D)的NVIC章节。

14.3.1 中断向量表

表14.3描述了中断向量。地址符合NVIC规范。

Table 14.3 中断向量表(1of4)

异常编号	IRQ number	矢量偏移	Source	Description
0	-	000h	Arm	初始堆栈指针
1	-	004h	Arm	初始程序计数器（复位向量）
2	-	008h	Arm	Non-maskable interrupt (NMI)
3	-	00Ch	Arm	硬故障
4	-	010h	Arm	MemManage fault
5	-	014h	Arm	总线故障
6	-	018h	Arm	使用故障
7	-	01Ch	Arm	Reserved
8	-	020h	Arm	Reserved
9	-	024h	Arm	Reserved
10	-	028h	Arm	Reserved
11	-	02Ch	Arm	主管呼叫(SVCall)
12	-	030h	Arm	调试监视器
13	-	034h	Arm	Reserved
14	-	038h	Arm	系统服务的挂起请求(PendableSrvReq)
15	-	03Ch	Arm	系统滴答计时器(SysTick)

Table 14.3 Interrupt vector table (2 of 4)

Exception number	IRQ number	Vector offset	Source	Description
16	0	040h	ICU.IELSR0	Event selected in the ICU.IELSR0 register
17	1	044h	ICU.IELSR1	Event selected in the ICU.IELSR1 register
18	2	048h	ICU.IELSR2	Event selected in the ICU.IELSR2 register
19	3	04Ch	ICU.IELSR3	Event selected in the ICU.IELSR3 register
20	4	050h	ICU.IELSR4	Event selected in the ICU.IELSR4 register
21	5	054h	ICU.IELSR5	Event selected in the ICU.IELSR5 register
22	6	058h	ICU.IELSR6	Event selected in the ICU.IELSR6 register
23	7	05Ch	ICU.IELSR7	Event selected in the ICU.IELSR7 register
24	8	060h	ICU.IELSR8	Event selected in the ICU.IELSR8 register
25	9	064h	ICU.IELSR9	Event selected in the ICU.IELSR9 register
26	10	068h	ICU.IELSR10	Event selected in the ICU.IELSR10 register
27	11	06Ch	ICU.IELSR11	Event selected in the ICU.IELSR11 register
28	12	070h	ICU.IELSR12	Event selected in the ICU.IELSR12 register
29	13	074h	ICU.IELSR13	Event selected in the ICU.IELSR13 register
30	14	078h	ICU.IELSR14	Event selected in the ICU.IELSR14 register
31	15	07Ch	ICU.IELSR15	Event selected in the ICU.IELSR15 register
32	16	080h	ICU.IELSR16	Event selected in the ICU.IELSR16 register
33	17	084h	ICU.IELSR17	Event selected in the ICU.IELSR17 register
34	18	088h	ICU.IELSR18	Event selected in the ICU.IELSR18 register
35	19	08Ch	ICU.IELSR19	Event selected in the ICU.IELSR19 register
36	20	090h	ICU.IELSR20	Event selected in the ICU.IELSR20 register
37	21	094h	ICU.IELSR21	Event selected in the ICU.IELSR21 register
38	22	098h	ICU.IELSR22	Event selected in the ICU.IELSR22 register
39	23	09Ch	ICU.IELSR23	Event selected in the ICU.IELSR23 register
40	24	0A0h	ICU.IELSR24	Event selected in the ICU.IELSR24 register
41	25	0A4h	ICU.IELSR25	Event selected in the ICU.IELSR25 register
42	26	0A8h	ICU.IELSR26	Event selected in the ICU.IELSR26 register
43	27	0ACh	ICU.IELSR27	Event selected in the ICU.IELSR27 register
44	28	0B0h	ICU.IELSR28	Event selected in the ICU.IELSR28 register
45	29	0B4h	ICU.IELSR29	Event selected in the ICU.IELSR29 register
46	30	0B8h	ICU.IELSR30	Event selected in the ICU.IELSR30 register
47	31	0BCh	ICU.IELSR31	Event selected in the ICU.IELSR31 register
48	32	0C0h	ICU.IELSR32	Event selected in the ICU.IELSR32 register
49	33	0C4h	ICU.IELSR33	Event selected in the ICU.IELSR33 register
50	34	0C8h	ICU.IELSR34	Event selected in the ICU.IELSR34 register
51	35	0CCh	ICU.IELSR35	Event selected in the ICU.IELSR35 register
52	36	0D0h	ICU.IELSR36	Event selected in the ICU.IELSR36 register
53	37	0D4h	ICU.IELSR37	Event selected in the ICU.IELSR37 register
54	38	0D8h	ICU.IELSR38	Event selected in the ICU.IELSR38 register
55	39	0DCh	ICU.IELSR39	Event selected in the ICU.IELSR39 register
56	40	0E0h	ICU.IELSR40	Event selected in the ICU.IELSR40 register
57	41	0E4h	ICU.IELSR41	Event selected in the ICU.IELSR41 register
58	42	0E8h	ICU.IELSR42	Event selected in the ICU.IELSR42 register
59	43	0ECh	ICU.IELSR43	Event selected in the ICU.IELSR43 register
60	44	0F0h	ICU.IELSR44	Event selected in the ICU.IELSR44 register

Table 14.3 中断向量表(2of4)

异常编号	IRQ number	矢量偏移	Source	Description
16	0	040h	ICU.IELSR0	在ICU.IELSR0寄存器中选择的事件
17	1	044h	ICU.IELSR1	在ICU.IELSR1寄存器中选择的事件
18	2	048h	ICU.IELSR2	在ICU.IELSR2寄存器中选择的事件
19	3	04Ch	ICU.IELSR3	在ICU.IELSR3寄存器中选择的事件
20	4	050h	ICU.IELSR4	在ICU.IELSR4寄存器中选择的事件
21	5	054h	ICU.IELSR5	在ICU.IELSR5寄存器中选择的事件
22	6	058h	ICU.IELSR6	在ICU.IELSR6寄存器中选择的事件
23	7	05Ch	ICU.IELSR7	在ICU.IELSR7寄存器中选择的事件
24	8	060h	ICU.IELSR8	在ICU.IELSR8寄存器中选择的事件
25	9	064h	ICU.IELSR9	在ICU.IELSR9寄存器中选择的事件
26	10	068h	ICU.IELSR10	在ICU.IELSR10寄存器中选择的事件
27	11	06Ch	ICU.IELSR11	在ICU.IELSR11寄存器中选择的事件
28	12	070h	ICU.IELSR12	在ICU.IELSR12寄存器中选择的事件
29	13	074h	ICU.IELSR13	在ICU.IELSR13寄存器中选择的事件
30	14	078h	ICU.IELSR14	在ICU.IELSR14寄存器中选择的事件
31	15	07Ch	ICU.IELSR15	在ICU.IELSR15寄存器中选择的事件
32	16	080h	ICU.IELSR16	在ICU.IELSR16寄存器中选择的事件
33	17	084h	ICU.IELSR17	在ICU.IELSR17寄存器中选择的事件
34	18	088h	ICU.IELSR18	在ICU.IELSR18寄存器中选择的事件
35	19	08Ch	ICU.IELSR19	在ICU.IELSR19寄存器中选择的事件
36	20	090h	ICU.IELSR20	在ICU.IELSR20寄存器中选择的事件
37	21	094h	ICU.IELSR21	在ICU.IELSR21寄存器中选择的事件
38	22	098h	ICU.IELSR22	在ICU.IELSR22寄存器中选择的事件
39	23	09Ch	ICU.IELSR23	在ICU.IELSR23寄存器中选择的事件
40	24	0A0h	ICU.IELSR24	在ICU.IELSR24寄存器中选择的事件
41	25	0A4h	ICU.IELSR25	在ICU.IELSR25寄存器中选择的事件
42	26	0A8h	ICU.IELSR26	在ICU.IELSR26寄存器中选择的事件
43	27	0ACh	ICU.IELSR27	在ICU.IELSR27寄存器中选择的事件
44	28	0B0h	ICU.IELSR28	在ICU.IELSR28寄存器中选择的事件
45	29	0B4h	ICU.IELSR29	在ICU.IELSR29寄存器中选择的事件
46	30	0B8h	ICU.IELSR30	在ICU.IELSR30寄存器中选择的事件
47	31	0BCh	ICU.IELSR31	在ICU.IELSR31寄存器中选择的事件
48	32	0C0h	ICU.IELSR32	在ICU.IELSR32寄存器中选择的事件
49	33	0C4h	ICU.IELSR33	在ICU.IELSR33寄存器中选择的事件
50	34	0C8h	ICU.IELSR34	在ICU.IELSR34寄存器中选择的事件
51	35	0CCh	ICU.IELSR35	在ICU.IELSR35寄存器中选择的事件
52	36	0D0h	ICU.IELSR36	在ICU.IELSR36寄存器中选择的事件
53	37	0D4h	ICU.IELSR37	在ICU.IELSR37寄存器中选择的事件
54	38	0D8h	ICU.IELSR38	在ICU.IELSR38寄存器中选择的事件
55	39	0DCh	ICU.IELSR39	在ICU.IELSR39寄存器中选择的事件
56	40	0E0h	ICU.IELSR40	在ICU.IELSR40寄存器中选择的事件
57	41	0E4h	ICU.IELSR41	在ICU.IELSR41寄存器中选择的事件
58	42	0E8h	ICU.IELSR42	在ICU.IELSR42寄存器中选择的事件
59	43	0ECh	ICU.IELSR43	在ICU.IELSR43寄存器中选择的事件
60	44	0F0h	ICU.IELSR44	在ICU.IELSR44寄存器中选择的事件

Table 14.3 Interrupt vector table (3 of 4)

Exception number	IRQ number	Vector offset	Source	Description
61	45	0F4h	ICU.IELSR45	Event selected in the ICU.IELSR45 register
62	46	0F8h	ICU.IELSR46	Event selected in the ICU.IELSR46 register
63	47	0FCh	ICU.IELSR47	Event selected in the ICU.IELSR47 register
64	48	100h	ICU.IELSR48	Event selected in the ICU.IELSR48 register
65	49	104h	ICU.IELSR49	Event selected in the ICU.IELSR49 register
66	50	108h	ICU.IELSR50	Event selected in the ICU.IELSR50 register
67	51	10Ch	ICU.IELSR51	Event selected in the ICU.IELSR51 register
68	52	110h	ICU.IELSR52	Event selected in the ICU.IELSR52 register
69	53	114h	ICU.IELSR53	Event selected in the ICU.IELSR53 register
70	54	118h	ICU.IELSR54	Event selected in the ICU.IELSR54 register
71	55	11Ch	ICU.IELSR55	Event selected in the ICU.IELSR55 register
72	56	120h	ICU.IELSR56	Event selected in the ICU.IELSR56 register
73	57	124h	ICU.IELSR57	Event selected in the ICU.IELSR57 register
74	58	128h	ICU.IELSR58	Event selected in the ICU.IELSR58 register
75	59	12Ch	ICU.IELSR59	Event selected in the ICU.IELSR59 register
76	60	130h	ICU.IELSR60	Event selected in the ICU.IELSR60 register
77	61	134h	ICU.IELSR61	Event selected in the ICU.IELSR61 register
78	62	138h	ICU.IELSR62	Event selected in the ICU.IELSR62 register
79	63	13Ch	ICU.IELSR63	Event selected in the ICU.IELSR63 register
80	64	140h	ICU.IELSR64	Event selected in the ICU.IELSR64 register
81	65	144h	ICU.IELSR65	Event selected in the ICU.IELSR65 register
82	66	148h	ICU.IELSR66	Event selected in the ICU.IELSR66 register
83	67	14Ch	ICU.IELSR67	Event selected in the ICU.IELSR67 register
84	68	150h	ICU.IELSR68	Event selected in the ICU.IELSR68 register
85	69	154h	ICU.IELSR69	Event selected in the ICU.IELSR69 register
86	70	158h	ICU.IELSR70	Event selected in the ICU.IELSR70 register
87	71	15Ch	ICU.IELSR71	Event selected in the ICU.IELSR71 register
88	72	160h	ICU.IELSR72	Event selected in the ICU.IELSR72 register
89	73	164h	ICU.IELSR73	Event selected in the ICU.IELSR73 register
90	74	168h	ICU.IELSR74	Event selected in the ICU.IELSR74 register
91	75	16Ch	ICU.IELSR75	Event selected in the ICU.IELSR75 register
92	76	170h	ICU.IELSR76	Event selected in the ICU.IELSR76 register
93	77	174h	ICU.IELSR77	Event selected in the ICU.IELSR77 register
94	78	178h	ICU.IELSR78	Event selected in the ICU.IELSR78 register
95	79	17Ch	ICU.IELSR79	Event selected in the ICU.IELSR79 register
96	80	180h	ICU.IELSR80	Event selected in the ICU.IELSR80 register
97	81	184h	ICU.IELSR81	Event selected in the ICU.IELSR81 register
98	82	188h	ICU.IELSR82	Event selected in the ICU.IELSR82 register
99	83	18Ch	ICU.IELSR83	Event selected in the ICU.IELSR83 register
100	84	190h	ICU.IELSR84	Event selected in the ICU.IELSR84 register
101	85	194h	ICU.IELSR85	Event selected in the ICU.IELSR85 register
102	86	198h	ICU.IELSR86	Event selected in the ICU.IELSR86 register
103	87	19Ch	ICU.IELSR87	Event selected in the ICU.IELSR87 register
104	88	1A0h	ICU.IELSR88	Event selected in the ICU.IELSR88 register
105	89	1A4h	ICU.IELSR89	Event selected in the ICU.IELSR89 register

Table 14.3 中断向量表(3of4)

异常编号	IRQ number	矢量偏移	Source	Description
61	45	0F4h	ICU.IELSR45	在ICU.IELSR45寄存器中选择的事件
62	46	0F8h	ICU.IELSR46	在ICU.IELSR46寄存器中选择的事件
63	47	0FCh	ICU.IELSR47	在ICU.IELSR47寄存器中选择的事件
64	48	100h	ICU.IELSR48	在ICU.IELSR48寄存器中选择的事件
65	49	104h	ICU.IELSR49	在ICU.IELSR49寄存器中选择的事件
66	50	108h	ICU.IELSR50	在ICU.IELSR50寄存器中选择的事件
67	51	10Ch	ICU.IELSR51	在ICU.IELSR51寄存器中选择的事件
68	52	110h	ICU.IELSR52	在ICU.IELSR52寄存器中选择的事件
69	53	114h	ICU.IELSR53	在ICU.IELSR53寄存器中选择的事件
70	54	118h	ICU.IELSR54	在ICU.IELSR54寄存器中选择的事件
71	55	11Ch	ICU.IELSR55	在ICU.IELSR55寄存器中选择的事件
72	56	120h	ICU.IELSR56	在ICU.IELSR56寄存器中选择的事件
73	57	124h	ICU.IELSR57	在ICU.IELSR57寄存器中选择的事件
74	58	128h	ICU.IELSR58	在ICU.IELSR58寄存器中选择的事件
75	59	12Ch	ICU.IELSR59	在ICU.IELSR59寄存器中选择的事件
76	60	130h	ICU.IELSR60	在ICU.IELSR60寄存器中选择的事件
77	61	134h	ICU.IELSR61	在ICU.IELSR61寄存器中选择的事件
78	62	138h	ICU.IELSR62	在ICU.IELSR62寄存器中选择的事件
79	63	13Ch	ICU.IELSR63	在ICU.IELSR63寄存器中选择的事件
80	64	140h	ICU.IELSR64	在ICU.IELSR64寄存器中选择的事件
81	65	144h	ICU.IELSR65	在ICU.IELSR65寄存器中选择的事件
82	66	148h	ICU.IELSR66	在ICU.IELSR66寄存器中选择的事件
83	67	14Ch	ICU.IELSR67	在ICU.IELSR67寄存器中选择的事件
84	68	150h	ICU.IELSR68	在ICU.IELSR68寄存器中选择的事件
85	69	154h	ICU.IELSR69	在ICU.IELSR69寄存器中选择的事件
86	70	158h	ICU.IELSR70	在ICU.IELSR70寄存器中选择的事件
87	71	15Ch	ICU.IELSR71	在ICU.IELSR71寄存器中选择的事件
88	72	160h	ICU.IELSR72	在ICU.IELSR72寄存器中选择的事件
89	73	164h	ICU.IELSR73	在ICU.IELSR73寄存器中选择的事件
90	74	168h	ICU.IELSR74	在ICU.IELSR74寄存器中选择的事件
91	75	16Ch	ICU.IELSR75	在ICU.IELSR75寄存器中选择的事件
92	76	170h	ICU.IELSR76	在ICU.IELSR76寄存器中选择的事件
93	77	174h	ICU.IELSR77	在ICU.IELSR77寄存器中选择的事件
94	78	178h	ICU.IELSR78	在ICU.IELSR78寄存器中选择的事件
95	79	17Ch	ICU.IELSR79	在ICU.IELSR79寄存器中选择的事件
96	80	180h	ICU.IELSR80	在ICU.IELSR80寄存器中选择的事件
97	81	184h	ICU.IELSR81	在ICU.IELSR81寄存器中选择的事件
98	82	188h	ICU.IELSR82	在ICU.IELSR82寄存器中选择的事件
99	83	18Ch	ICU.IELSR83	在ICU.IELSR83寄存器中选择的事件
100	84	190h	ICU.IELSR84	在ICU.IELSR84寄存器中选择的事件
101	85	194h	ICU.IELSR85	在ICU.IELSR85寄存器中选择的事件
102	86	198h	ICU.IELSR86	在ICU.IELSR86寄存器中选择的事件
103	87	19Ch	ICU.IELSR87	在ICU.IELSR87寄存器中选择的事件
104	88	1A0h	ICU.IELSR88	在ICU.IELSR88寄存器中选择的事件
105	89	1A4h	ICU.IELSR89	在ICU.IELSR89寄存器中选择的事件

Table 14.3 Interrupt vector table (4 of 4)

Exception number	IRQ number	Vector offset	Source	Description
106	90	1A8h	ICU.IELSR90	Event selected in the ICU.IELSR90 register
107	91	1ACh	ICU.IELSR91	Event selected in the ICU.IELSR91 register
108	92	1B0h	ICU.IELSR92	Event selected in the ICU.IELSR92 register
109	93	1B4h	ICU.IELSR93	Event selected in the ICU.IELSR93 register
110	94	1B8h	ICU.IELSR94	Event selected in the ICU.IELSR94 register
111	95	1BCh	ICU.IELSR95	Event selected in the ICU.IELSR95 register

14.3.2 Event Numbers

The following table lists heading details for Table 14.4, which describes each event number.

Heading	Description
Interrupt request source	Name of the source generating the interrupt request
Name	Name of the interrupt
Connect to NVIC	"✓" indicates the interrupt can be used as a CPU interrupt (IELSRn setting)
Invoke DTC	"✓" indicates the interrupt can be used to request DTC activation (IELSRn setting)
Invoke DMAC	"✓" indicates the interrupt can be used to request DMAC activation (DELSRn setting)
Canceling Snooze mode	"✓" indicates the interrupt can be used to request a return from Snooze mode using SELSR0. Otherwise, "✓" indicates it can be used directly
Canceling Software Standby mode	"✓" indicates the interrupt can be used to request a return from Software Standby mode
Canceling Deep Software Standby mode	"✓" indicates the interrupt can be used to request a return from Deep Software Standby mode

Table 14.4 Event table (1 of 9)

Event number	Interrupt request source	Name	IELSRn		DELSRn	Canceling Snooze mode	Canceling Software Standby mode	Canceling Deep Software Standby mode
			Connect to NVIC	Invoke DTC	Invoke DMAC			
001h	Port	PORT_IRQ0	✓	✓	✓	✓	✓	✓
002h		PORT_IRQ1	✓	✓	✓	✓	✓	✓
003h		PORT_IRQ2	✓	✓	✓	✓	✓	✓
004h		PORT_IRQ3	✓	✓	✓	✓	✓	✓
005h		PORT_IRQ4	✓	✓	✓	✓	✓	✓
006h		PORT_IRQ5	✓	✓	✓	✓	✓	✓
007h		PORT_IRQ6	✓	✓	✓	✓	✓	✓
008h		PORT_IRQ7	✓	✓	✓	✓	✓	✓
009h		PORT_IRQ8	✓	✓	✓	✓	✓	✓
00Ah		PORT_IRQ9	✓	✓	✓	✓	✓	✓
00Bh		PORT_IRQ10	✓	✓	✓	✓	✓	✓
00Ch		PORT_IRQ11	✓	✓	✓	✓	✓	✓
00Dh		PORT_IRQ12	✓	✓	✓	✓	✓	✓
00Eh		PORT_IRQ13	✓	✓	✓	✓	✓	✓
00Fh		PORT_IRQ14	✓	✓	✓	✓	✓	✓
010h		PORT_IRQ15	✓	✓	✓	✓	✓	-
020h	DMAC0	DMAC0_INT	✓	✓	-	-	-	-
021h	DMAC1	DMAC1_INT	✓	✓	-	-	-	-
022h	DMAC2	DMAC2_INT	✓	✓	-	-	-	-

Table 14.3 中断向量表(4of4)

异常编号	IRQ number	矢量偏移	Source	Description
106	90	1A8h	ICU.IELSR90	在ICU.IELSR90寄存器中选择的事件
107	91	1ACh	ICU.IELSR91	在ICU.IELSR91寄存器中选择的事件
108	92	1B0h	ICU.IELSR92	在ICU.IELSR92寄存器中选择的事件
109	93	1B4h	ICU.IELSR93	在ICU.IELSR93寄存器中选择的事件
110	94	1B8h	ICU.IELSR94	在ICU.IELSR94寄存器中选择的事件
111	95	1BCh	ICU.IELSR95	在ICU.IELSR95寄存器中选择的事件

14.3.2 事件编号

下表列出了表14.4的标题详细信息，其中描述了每个事件编号。

Heading	Description
中断请求源	产生中断请求的源名称
Name	中断名称
连接到NVIC	" "表示该中断可以作为CPU中断使用（IELSRn设置）
Invoke DTC	" "表示中断可用于请求DTC激活（IELSRn设置）
Invoke DMAC	" "表示中断可用于请求DMAC激活（DELSRn设置）
取消贪睡模式	" "表示该中断可用于使用SELSR0请求从贪睡模式返回。否则，" "表示可以直接使用
取消软件待机模式	" "表示中断可用于请求从软件待机模式返回
取消深度软件待机模式	" "表示中断可用于请求从深度软件待机模式返回

Table 14.4 事件表(1of9)

事件编号	中断请求源	Name	IELSRn		DELSRn	Canceling 贪睡模式	取消软件待机模式	取消深度 软件待机模式
			连接到NVIC	Invoke DTC	Invoke DMAC			
001h	Port	PORT_IRQ0	✓	✓	✓	✓	✓	✓
002h		PORT_IRQ1	✓	✓	✓	✓	✓	✓
003h		PORT_IRQ2	✓	✓	✓	✓	✓	✓
004h		PORT_IRQ3	✓	✓	✓	✓	✓	✓
005h		PORT_IRQ4	✓	✓	✓	✓	✓	✓
006h		PORT_IRQ5	✓	✓	✓	✓	✓	✓
007h		PORT_IRQ6	✓	✓	✓	✓	✓	✓
008h		PORT_IRQ7	✓	✓	✓	✓	✓	✓
009h		PORT_IRQ8	✓	✓	✓	✓	✓	✓
00Ah		PORT_IRQ9	✓	✓	✓	✓	✓	✓
00Bh		PORT_IRQ10	✓	✓	✓	✓	✓	✓
00Ch		PORT_IRQ11	✓	✓	✓	✓	✓	✓
00Dh		PORT_IRQ12	✓	✓	✓	✓	✓	✓
00Eh		PORT_IRQ13	✓	✓	✓	✓	✓	✓
00Fh		PORT_IRQ14	✓	✓	✓	✓	✓	✓
010h		PORT_IRQ15	✓	✓	✓	✓	✓	-
020h	DMAC0	DMAC0_INT	✓	✓	-	-	-	-
021h	DMAC1	DMAC1_INT	✓	✓	-	-	-	-
022h	DMAC2	DMAC2_INT	✓	✓	-	-	-	-

Table 14.4 Event table (2 of 9)

Event number	Interrupt request source	Name	IELSRn		DELSRn	Canceling Snooze mode	Canceling Software Standby mode	Canceling Deep Software Standby mode
			Connect to NVIC	Invoke DTC	Invoke DMAC			
023h	DMAC3	DMAC3_INT	✓	✓	-	-	-	-
024h	DMAC4	DMAC4_INT	✓	✓	-	-	-	-
025h	DMAC5	DMAC5_INT	✓	✓	-	-	-	-
026h	DMAC6	DMAC6_INT	✓	✓	-	-	-	-
027h	DMAC7	DMAC7_INT	✓	✓	-	-	-	-
029h	DTC	DTC_COMPLETE	✓	-	-	✓*5	-	-
02Dh	ICU	ICU_SNZCANCEL	✓	-	-	✓	-	-
030h	FCU	FCU_FIFERR	✓	-	-	-	-	-
031h		FCU_FRDYI	✓	-	-	-	-	-
038h	LVD	LVD_LVD1	✓	-	-	✓	✓	✓
039h		LVD_LVD2	✓	-	-	✓	✓	✓
03Bh	MOSC	MOSC_STOP	✓	-	-	-	-	-
03Ch	Low-power mode	SYSTEM_SNZREQ	-	✓	-	-	-	-
040h	AGT0	AGT0_AGTI	✓	✓	✓	-	-	-
041h		AGT0_AGTCMAI	✓	✓	✓	-	-	-
042h		AGT0_AGTCMBI	✓	✓	✓	-	-	-
043h	AGT1	AGT1_AGTI	✓	✓	✓	✓	✓	✓
044h		AGT1_AGTCMAI	✓	✓	✓	✓	✓	-
045h		AGT1_AGTCMBI	✓	✓	✓	✓	✓	-
046h	IWDT	IWDT_NMIUNDF	✓	-	-	✓	✓	-
047h	WDT	WDT_NMIUNDF	✓	-	-	-	-	-
048h	RTC	RTC_ALM	✓	-	-	✓	✓	✓
049h		RTC_PRD	✓	-	-	✓	✓	✓
04Ah		RTC_CUP	✓	-	-	-	-	-
04Bh	ADC120	ADC120_ADI	✓	✓	✓	-	-	-
04Ch		ADC120_GBADI	✓	✓	✓	-	-	-
04Dh		ADC120_CMPAI	✓	-	-	-	-	-
04Eh		ADC120_CMPBI	✓	-	-	-	-	-
04Fh		ADC120_WCMPM	-	✓	✓	✓*5	-	-
050h		ADC120_WCMPUM	-	✓	✓	✓*5	-	-
051h	ADC121	ADC121_ADI	✓	✓	✓	-	-	-
052h		ADC121_GBADI	✓	✓	✓	-	-	-
053h		ADC121_CMPAI	✓	-	-	-	-	-
054h		ADC121_CMPBI	✓	-	-	-	-	-
055h		ADC121_WCMPM	-	✓	✓	✓*5	-	-
056h		ADC121_WCMPUM	-	✓	✓	✓*5	-	-
057h	ACMPHS	ACMP_HS0	✓	-	-	✓*1	✓*1	-
058h		ACMP_HS1	✓	-	-	-	-	-
059h		ACMP_HS2	✓	-	-	-	-	-
05Ah		ACMP_HS3	✓	-	-	-	-	-
05Bh		ACMP_HS4	✓	-	-	-	-	-
05Ch		ACMP_HS5	✓	-	-	-	-	-
05Fh	USBFS	USBFS_D0FIFO	✓	✓	✓	-	-	-
060h		USBFS_D1FIFO	✓	✓	✓	-	-	-
061h		USBFS_USBI	✓	-	-	-	-	-
062h		USBFS_USBR	✓	-	-	✓	✓	✓

Table 14.4 事件表（2个，共9个）

事件编号	中断请求源	Name	IELSRn		DELSRn	Canceling 贪睡模式	取消软件待机模式	取消深度软件待机模式
			连接到NVIC	Invoke DTC	Invoke DMAC			
023h	DMAC3	DMAC3_INT	✓	✓	-	-	-	-
024h	DMAC4	DMAC4_INT	✓	✓	-	-	-	-
025h	DMAC5	DMAC5_INT	✓	✓	-	-	-	-
026h	DMAC6	DMAC6_INT	✓	✓	-	-	-	-
027h	DMAC7	DMAC7_INT	✓	✓	-	-	-	-
029h	DTC	DTC_COMPLETE	✓	-	-	✓*5	-	-
02Dh	ICU	ICU_SNZCANCEL	✓	-	-	✓	-	-
030h	FCU	FCU_FIFERR	✓	-	-	-	-	-
031h		FCU_FRDYI	✓	-	-	-	-	-
038h	LVD	LVD_LVD1	✓	-	-	✓	✓	✓
039h		LVD_LVD2	✓	-	-	✓	✓	✓
03Bh	MOSC	MOSC_STOP	✓	-	-	-	-	-
03Ch	Low-power mode	SYSTEM_SNZREQ	-	✓	-	-	-	-
040h	AGT0	AGT0_AGTI	✓	✓	✓	-	-	-
041h		AGT0_AGTCMAI	✓	✓	✓	-	-	-
042h		AGT0_AGTCMBI	✓	✓	✓	-	-	-
043h	AGT1	AGT1_AGTI	✓	✓	✓	✓	✓	✓
044h		AGT1_AGTCMAI	✓	✓	✓	✓	✓	-
045h		AGT1_AGTCMBI	✓	✓	✓	✓	✓	-
046h	IWDT	IWDT_NMIUNDF	✓	-	-	✓	✓	-
047h	WDT	WDT_NMIUNDF	✓	-	-	-	-	-
048h	RTC	RTC_ALM	✓	-	-	✓	✓	✓
049h		RTC_PRD	✓	-	-	✓	✓	✓
04Ah		RTC_CUP	✓	-	-	-	-	-
04Bh	ADC120	ADC120_ADI	✓	✓	✓	-	-	-
04Ch		ADC120_GBADI	✓	✓	✓	-	-	-
04Dh		ADC120_CMPAI	✓	-	-	-	-	-
04Eh		ADC120_CMPBI	✓	-	-	-	-	-
04Fh		ADC120_WCMPM	-	✓	✓	✓*5	-	-
050h		ADC120_WCMPUM	-	✓	✓	✓*5	-	-
051h	ADC121	ADC121_ADI	✓	✓	✓	-	-	-
052h		ADC121_GBADI	✓	✓	✓	-	-	-
053h		ADC121_CMPAI	✓	-	-	-	-	-
054h		ADC121_CMPBI	✓	-	-	-	-	-
055h		ADC121_WCMPM	-	✓	✓	✓*5	-	-
056h		ADC121_WCMPUM	-	✓	✓	✓*5	-	-
057h	ACMPHS	ACMP_HS0	✓	-	-	✓*1	✓*1	-
058h		ACMP_HS1	✓	-	-	-	-	-
059h		ACMP_HS2	✓	-	-	-	-	-
05Ah		ACMP_HS3	✓	-	-	-	-	-
05Bh		ACMP_HS4	✓	-	-	-	-	-
05Ch		ACMP_HS5	✓	-	-	-	-	-
05Fh	USBFS	USBFS_D0FIFO	✓	✓	✓	-	-	-
060h		USBFS_D1FIFO	✓	✓	✓	-	-	-
061h		USBFS_USBI	✓	-	-	-	-	-
062h		USBFS_USBR	✓	-	-	✓	✓	✓

Table 14.4 Event table (3 of 9)

Event number	Interrupt request source	Name	IELSRn		DELSRn	Canceling Snooze mode	Canceling Software Standby mode	Canceling Deep Software Standby mode
			Connect to NVIC	Invoke DTC	Invoke DMAC			
063h	IIC0	IIC0_RXI	✓	✓	✓	-	-	-
064h		IIC0_TXI	✓	✓	✓	-	-	-
065h		IIC0_TEI	✓	-	-	-	-	-
066h		IIC0_EEI	✓	-	-	-	-	-
067h		IIC0_WUI	✓	-	-	✓	✓	-
068h	IIC1	IIC1_RXI	✓	✓	✓	-	-	-
069h		IIC1_TXI	✓	✓	✓	-	-	-
06Ah		IIC1_TEI	✓	-	-	-	-	-
06Bh		IIC1_EEI	✓	-	-	-	-	-
06Dh	IIC2	IIC2_RXI	✓	✓	✓	-	-	-
06Eh		IIC2_TXI	✓	✓	✓	-	-	-
06Fh		IIC2_TEI	✓	-	-	-	-	-
070h		IIC2_EEI	✓	-	-	-	-	-
072h	SSIE0	SSIE0_SSITXI	✓	✓	✓	-	-	-
073h		SSIE0_SSIRXI	✓	✓	✓	-	-	-
075h		SSIE0_SSIF	✓	-	-	-	-	-
078h	SSIE1	SSIE1_SSIRT	✓	✓	✓	-	-	-
079h		SSIE1_SSIF	✓	-	-	-	-	-
07Ah	SRC	SRC_IDEI	✓	✓	✓	-	-	-
07Bh		SRC_ODFI	✓	✓	✓	-	-	-
07Ch		SRC_OVFI	✓	-	-	-	-	-
07Dh		SRC_UDFI	✓	-	-	-	-	-
07Eh		SRC_CEFI	✓	-	-	-	-	-
07Fh	PDC	PDC_PCDFI	✓	✓	✓	-	-	-
080h		PDC_PCFEI	✓	-	-	-	-	-
081h		PDC_PCERI	✓	-	-	-	-	-
082h	CTSU	CTSU_CTSUWR	✓	✓	✓	-	-	-
083h		CTSU_CTSURD	✓	✓	✓	-	-	-
084h		CTSU_CTSUFN	✓	-	-	✓*5	-	-
085h	KINT	KEY_INTKR	✓	-	-	✓*2	✓*2	-
086h	DOC	DOC_DOPCI	✓	-	-	✓*5	-	-
087h	CAC	CAC_FERRI	✓	-	-	-	-	-
088h		CAC_MENDI	✓	-	-	-	-	-
089h		CAC_OVFI	✓	-	-	-	-	-
08Ah	CAN0	CAN0_ERS	✓	-	-	-	-	-
08Bh		CAN0_RXF	✓	-	-	-	-	-
08Ch		CAN0_TXF	✓	-	-	-	-	-
08Dh		CAN0_RXM	✓	-	-	-	-	-
08Eh		CAN0_TXM	✓	-	-	-	-	-
08Fh	CAN1	CAN1_ERS	✓	-	-	-	-	-
090h		CAN1_RXF	✓	-	-	-	-	-
091h		CAN1_TXF	✓	-	-	-	-	-
092h		CAN1_RXM	✓	-	-	-	-	-
093h		CAN1_TXM	✓	-	-	-	-	-

Table 14.4 事件表（3个，共9个）

事件编号	中断请求源	Name	IELSRn		DELSRn	Canceling 贪睡模式	取消软件待机模式	取消深度软件待机模式
			连接到NVIC	Invoke DTC	Invoke DMAC			
063h	IIC0	IIC0_RXI	✓	✓	✓	-	-	-
064h		IIC0_TXI	✓	✓	✓	-	-	-
065h		IIC0_TEI	✓	-	-	-	-	-
066h		IIC0_EEI	✓	-	-	-	-	-
067h		IIC0_WUI	✓	-	-	✓	✓	-
068h	IIC1	IIC1_RXI	✓	✓	✓	-	-	-
069h		IIC1_TXI	✓	✓	✓	-	-	-
06Ah		IIC1_TEI	✓	-	-	-	-	-
06Bh		IIC1_EEI	✓	-	-	-	-	-
06Dh	IIC2	IIC2_RXI	✓	✓	✓	-	-	-
06Eh		IIC2_TXI	✓	✓	✓	-	-	-
06Fh		IIC2_TEI	✓	-	-	-	-	-
070h		IIC2_EEI	✓	-	-	-	-	-
072h	SSIE0	SSIE0_SSITXI	✓	✓	✓	-	-	-
073h		SSIE0_SSIRXI	✓	✓	✓	-	-	-
075h		SSIE0_SSIF	✓	-	-	-	-	-
078h	SSIE1	SSIE1_SSIRT	✓	✓	✓	-	-	-
079h		SSIE1_SSIF	✓	-	-	-	-	-
07Ah	SRC	SRC_IDEI	✓	✓	✓	-	-	-
07Bh		SRC_ODFI	✓	✓	✓	-	-	-
07Ch		SRC_OVFI	✓	-	-	-	-	-
07Dh		SRC_UDFI	✓	-	-	-	-	-
07Eh		SRC_CEFI	✓	-	-	-	-	-
07Fh	PDC	PDC_PCDFI	✓	✓	✓	-	-	-
080h		PDC_PCFEI	✓	-	-	-	-	-
081h		PDC_PCERI	✓	-	-	-	-	-
082h	CTSU	CTSU_CTSUWR	✓	✓	✓	-	-	-
083h		CTSU_CTSURD	✓	✓	✓	-	-	-
084h		CTSU_CTSUFN	✓	-	-	✓*5	-	-
085h	KINT	KEY_INTKR	✓	-	-	✓*2	✓*2	-
086h	DOC	DOC_DOPCI	✓	-	-	✓*5	-	-
087h	CAC	CAC_FERRI	✓	-	-	-	-	-
088h		CAC_MENDI	✓	-	-	-	-	-
089h		CAC_OVFI	✓	-	-	-	-	-
08Ah	CAN0	CAN0_ERS	✓	-	-	-	-	-
08Bh		CAN0_RXF	✓	-	-	-	-	-
08Ch		CAN0_TXF	✓	-	-	-	-	-
08Dh		CAN0_RXM	✓	-	-	-	-	-
08Eh		CAN0_TXM	✓	-	-	-	-	-
08Fh	CAN1	CAN1_ERS	✓	-	-	-	-	-
090h		CAN1_RXF	✓	-	-	-	-	-
091h		CAN1_TXF	✓	-	-	-	-	-
092h		CAN1_RXM	✓	-	-	-	-	-
093h		CAN1_TXM	✓	-	-	-	-	-

Table 14.4 Event table (4 of 9)

Event number	Interrupt request source	Name	IELSRn		DELSRn	Canceling Snooze mode	Canceling Software Standby mode	Canceling Deep Software Standby mode
			Connect to NVIC	Invoke DTC	Invoke DMAC			
094h	I/O port	IOPORT_GROUP1	✓	✓*3	✓*3	-	-	-
095h		IOPORT_GROUP2	✓	✓*3	✓*3	-	-	-
096h		IOPORT_GROUP3	✓	✓*3	✓*3	-	-	-
097h		IOPORT_GROUP4	✓	✓*3	✓*3	-	-	-
098h	ELC	ELC_SWEVT0	✓*4	✓	-	-	-	-
099h		ELC_SWEVT1	✓*4	✓	-	-	-	-
09Ah	POEG	POEG_GROUP0	✓	-	-	-	-	-
09Bh		POEG_GROUP1	✓	-	-	-	-	-
09Ch		POEG_GROUP2	✓	-	-	-	-	-
09Dh		POEG_GROUP3	✓	-	-	-	-	-
0B0h	GPT32EH0	GPT0_CCMPA	✓	✓	✓	-	-	-
0B1h		GPT0_CCMPB	✓	✓	✓	-	-	-
0B2h		GPT0_CMPC	✓	✓	✓	-	-	-
0B3h		GPT0_CMPD	✓	✓	✓	-	-	-
0B4h		GPT0_CMPE	✓	✓	✓	-	-	-
0B5h		GPT0_CMPF	✓	✓	✓	-	-	-
0B6h		GPT0_OVF	✓	✓	✓	-	-	-
0B7h		GPT0_UDF	✓	✓	✓	-	-	-
0B8h		GPT0_ADTRGA	✓	✓	✓	-	-	-
0B9h		GPT0_ADTRGB	✓	✓	✓	-	-	-
0BAh	GPT32EH1	GPT1_CCMPA	✓	✓	✓	-	-	-
0BBh		GPT1_CCMPB	✓	✓	✓	-	-	-
0BCh		GPT1_CMPC	✓	✓	✓	-	-	-
0BDh		GPT1_CMPD	✓	✓	✓	-	-	-
0BEh		GPT1_CMPE	✓	✓	✓	-	-	-
0BFh		GPT1_CMPF	✓	✓	✓	-	-	-
0C0h		GPT1_OVF	✓	✓	✓	-	-	-
0C1h		GPT1_UDF	✓	✓	✓	-	-	-
0C2h		GPT1_ADTRGA	✓	✓	✓	-	-	-
0C3h		GPT1_ADTRGB	✓	✓	✓	-	-	-
0C4h	GPT32EH2	GPT2_CCMPA	✓	✓	✓	-	-	-
0C5h		GPT2_CCMPB	✓	✓	✓	-	-	-
0C6h		GPT2_CMPC	✓	✓	✓	-	-	-
0C7h		GPT2_CMPD	✓	✓	✓	-	-	-
0C8h		GPT2_CMPE	✓	✓	✓	-	-	-
0C9h		GPT2_CMPF	✓	✓	✓	-	-	-
0CAh		GPT2_OVF	✓	✓	✓	-	-	-
0CBh		GPT2_UDF	✓	✓	✓	-	-	-
0CCh		GPT2_ADTRGA	✓	✓	✓	-	-	-
0CDh		GPT2_ADTRGB	✓	✓	✓	-	-	-

Table 14.4 事件表（4个，共9个）

事件编号	中断请求源	Name	IELSRn		DELSRn	Canceling 贪睡模式	取消软件待机模式	取消深度软件待机模式
			连接到NVIC	Invoke DTC	Invoke DMAC			
094h	I/O port	IOPORT_GROUP1	✓	✓*3	✓*3	-	-	-
095h		IOPORT_GROUP2	✓	✓*3	✓*3	-	-	-
096h		IOPORT_GROUP3	✓	✓*3	✓*3	-	-	-
097h		IOPORT_GROUP4	✓	✓*3	✓*3	-	-	-
098h	ELC	ELC_SWEVT0	✓*4	✓	-	-	-	-
099h		ELC_SWEVT1	✓*4	✓	-	-	-	-
09Ah	POEG	POEG_GROUP0	✓	-	-	-	-	-
09Bh		POEG_GROUP1	✓	-	-	-	-	-
09Ch		POEG_GROUP2	✓	-	-	-	-	-
09Dh		POEG_GROUP3	✓	-	-	-	-	-
0B0h	GPT32EH0	GPT0_CCMPA	✓	✓	✓	-	-	-
0B1h		GPT0_CCMPB	✓	✓	✓	-	-	-
0B2h		GPT0_CMPC	✓	✓	✓	-	-	-
0B3h		GPT0_CMPD	✓	✓	✓	-	-	-
0B4h		GPT0_CMPE	✓	✓	✓	-	-	-
0B5h		GPT0_CMPF	✓	✓	✓	-	-	-
0B6h		GPT0_OVF	✓	✓	✓	-	-	-
0B7h		GPT0_UDF	✓	✓	✓	-	-	-
0B8h		GPT0_ADTRGA	✓	✓	✓	-	-	-
0B9h		GPT0_ADTRGB	✓	✓	✓	-	-	-
0BAh	GPT32EH1	GPT1_CCMPA	✓	✓	✓	-	-	-
0BBh		GPT1_CCMPB	✓	✓	✓	-	-	-
0BCh		GPT1_CMPC	✓	✓	✓	-	-	-
0BDh		GPT1_CMPD	✓	✓	✓	-	-	-
0BEh		GPT1_CMPE	✓	✓	✓	-	-	-
0BFh		GPT1_CMPF	✓	✓	✓	-	-	-
0C0h		GPT1_OVF	✓	✓	✓	-	-	-
0C1h		GPT1_UDF	✓	✓	✓	-	-	-
0C2h		GPT1_ADTRGA	✓	✓	✓	-	-	-
0C3h		GPT1_ADTRGB	✓	✓	✓	-	-	-
0C4h	GPT32EH2	GPT2_CCMPA	✓	✓	✓	-	-	-
0C5h		GPT2_CCMPB	✓	✓	✓	-	-	-
0C6h		GPT2_CMPC	✓	✓	✓	-	-	-
0C7h		GPT2_CMPD	✓	✓	✓	-	-	-
0C8h		GPT2_CMPE	✓	✓	✓	-	-	-
0C9h		GPT2_CMPF	✓	✓	✓	-	-	-
0CAh		GPT2_OVF	✓	✓	✓	-	-	-
0CBh		GPT2_UDF	✓	✓	✓	-	-	-
0CCh		GPT2_ADTRGA	✓	✓	✓	-	-	-
0CDh		GPT2_ADTRGB	✓	✓	✓	-	-	-

Table 14.4 Event table (5 of 9)

Event number	Interrupt request source	Name	IELSRn		DELSRn	Canceling Snooze mode	Canceling Software Standby mode	Canceling Deep Software Standby mode
			Connect to NVIC	Invoke DTC	Invoke DMAC			
0CEh	GPT32EH3	GPT3_CCMPA	✓	✓	✓	-	-	-
0CFh		GPT3_CCMPB	✓	✓	✓	-	-	-
0D0h		GPT3_CMPC	✓	✓	✓	-	-	-
0D1h		GPT3_CMPD	✓	✓	✓	-	-	-
0D2h		GPT3_CMPE	✓	✓	✓	-	-	-
0D3h		GPT3_CMPF	✓	✓	✓	-	-	-
0D4h		GPT3_OVF	✓	✓	✓	-	-	-
0D5h		GPT3_UDF	✓	✓	✓	-	-	-
0D6h		GPT3_ADTRGA	✓	✓	✓	-	-	-
0D7h		GPT3_ADTRGB	✓	✓	✓	-	-	-
0D8h	GPT32E4	GPT4_CCMPA	✓	✓	✓	-	-	-
0D9h		GPT4_CCMPB	✓	✓	✓	-	-	-
0DAh		GPT4_CMPC	✓	✓	✓	-	-	-
0DBh		GPT4_CMPD	✓	✓	✓	-	-	-
0DCh		GPT4_CMPE	✓	✓	✓	-	-	-
0DDh		GPT4_CMPF	✓	✓	✓	-	-	-
0DEh		GPT4_OVF	✓	✓	✓	-	-	-
0DFh		GPT4_UDF	✓	✓	✓	-	-	-
0E0h		GPT4_ADTRGA	✓	✓	✓	-	-	-
0E1h		GPT4_ADTRGB	✓	✓	✓	-	-	-
0E2h	GPT32E5	GPT5_CCMPA	✓	✓	✓	-	-	-
0E3h		GPT5_CCMPB	✓	✓	✓	-	-	-
0E4h		GPT5_CMPC	✓	✓	✓	-	-	-
0E5h		GPT5_CMPD	✓	✓	✓	-	-	-
0E6h		GPT5_CMPE	✓	✓	✓	-	-	-
0E7h		GPT5_CMPF	✓	✓	✓	-	-	-
0E8h		GPT5_OVF	✓	✓	✓	-	-	-
0E9h		GPT5_UDF	✓	✓	✓	-	-	-
0EAh		GPT5_ADTRGA	✓	✓	✓	-	-	-
0EBh		GPT5_ADTRGB	✓	✓	✓	-	-	-
0ECh	GPT32E6	GPT6_CCMPA	✓	✓	✓	-	-	-
0EDh		GPT6_CCMPB	✓	✓	✓	-	-	-
0EEh		GPT6_CMPC	✓	✓	✓	-	-	-
0EFh		GPT6_CMPD	✓	✓	✓	-	-	-
0F0h		GPT6_CMPE	✓	✓	✓	-	-	-
0F1h		GPT6_CMPF	✓	✓	✓	-	-	-
0F2h		GPT6_OVF	✓	✓	✓	-	-	-
0F3h		GPT6_UDF	✓	✓	✓	-	-	-
0F4h		GPT6_ADTRGA	✓	✓	✓	-	-	-
0F5h		GPT6_ADTRGB	✓	✓	✓	-	-	-

Table 14.4 事件表（5个，共9个）

事件编号	中断请求源	Name	IELSRn		DELSRn	Canceling 贪睡模式	取消软件待机模式	取消深度软件待机模式
			连接到NVIC	Invoke DTC	Invoke DMAC			
0CEh	GPT32EH3	GPT3_CCMPA	✓	✓	✓	-	-	-
0CFh		GPT3_CCMPB	✓	✓	✓	-	-	-
0D0h		GPT3_CMPC	✓	✓	✓	-	-	-
0D1h		GPT3_CMPD	✓	✓	✓	-	-	-
0D2h		GPT3_CMPE	✓	✓	✓	-	-	-
0D3h		GPT3_CMPF	✓	✓	✓	-	-	-
0D4h		GPT3_OVF	✓	✓	✓	-	-	-
0D5h		GPT3_UDF	✓	✓	✓	-	-	-
0D6h		GPT3_ADTRGA	✓	✓	✓	-	-	-
0D7h		GPT3_ADTRGB	✓	✓	✓	-	-	-
0D8h	GPT32E4	GPT4_CCMPA	✓	✓	✓	-	-	-
0D9h		GPT4_CCMPB	✓	✓	✓	-	-	-
0DAh		GPT4_CMPC	✓	✓	✓	-	-	-
0DBh		GPT4_CMPD	✓	✓	✓	-	-	-
0DCh		GPT4_CMPE	✓	✓	✓	-	-	-
0DDh		GPT4_CMPF	✓	✓	✓	-	-	-
0DEh		GPT4_OVF	✓	✓	✓	-	-	-
0DFh		GPT4_UDF	✓	✓	✓	-	-	-
0E0h		GPT4_ADTRGA	✓	✓	✓	-	-	-
0E1h		GPT4_ADTRGB	✓	✓	✓	-	-	-
0E2h	GPT32E5	GPT5_CCMPA	✓	✓	✓	-	-	-
0E3h		GPT5_CCMPB	✓	✓	✓	-	-	-
0E4h		GPT5_CMPC	✓	✓	✓	-	-	-
0E5h		GPT5_CMPD	✓	✓	✓	-	-	-
0E6h		GPT5_CMPE	✓	✓	✓	-	-	-
0E7h		GPT5_CMPF	✓	✓	✓	-	-	-
0E8h		GPT5_OVF	✓	✓	✓	-	-	-
0E9h		GPT5_UDF	✓	✓	✓	-	-	-
0EAh		GPT5_ADTRGA	✓	✓	✓	-	-	-
0EBh		GPT5_ADTRGB	✓	✓	✓	-	-	-
0ECh	GPT32E6	GPT6_CCMPA	✓	✓	✓	-	-	-
0EDh		GPT6_CCMPB	✓	✓	✓	-	-	-
0EEh		GPT6_CMPC	✓	✓	✓	-	-	-
0EFh		GPT6_CMPD	✓	✓	✓	-	-	-
0F0h		GPT6_CMPE	✓	✓	✓	-	-	-
0F1h		GPT6_CMPF	✓	✓	✓	-	-	-
0F2h		GPT6_OVF	✓	✓	✓	-	-	-
0F3h		GPT6_UDF	✓	✓	✓	-	-	-
0F4h		GPT6_ADTRGA	✓	✓	✓	-	-	-
0F5h		GPT6_ADTRGB	✓	✓	✓	-	-	-

Table 14.4 Event table (6 of 9)

Event number	Interrupt request source	Name	IELSRn		DELSRn	Canceling Snooze mode	Canceling Software Standby mode	Canceling Deep Software Standby mode
			Connect to NVIC	Invoke DTC	Invoke DMAC			
0F6h	GPT32E7	GPT7_CCMPA	✓	✓	✓	-	-	-
0F7h		GPT7_CCMPB	✓	✓	✓	-	-	-
0F8h		GPT7_CMPC	✓	✓	✓	-	-	-
0F9h		GPT7_CMPD	✓	✓	✓	-	-	-
0FAh		GPT7_CMPE	✓	✓	✓	-	-	-
0FBh		GPT7_CMPF	✓	✓	✓	-	-	-
0FCh		GPT7_OVF	✓	✓	✓	-	-	-
0FDh		GPT7_UDF	✓	✓	✓	-	-	-
0FEh		GPT7_ADTRGA	✓	✓	✓	-	-	-
0FFh		GPT7_ADTRGB	✓	✓	✓	-	-	-
100h	GPT328	GPT8_CCMPA	✓	✓	✓	-	-	-
101h		GPT8_CCMPB	✓	✓	✓	-	-	-
102h		GPT8_CMPC	✓	✓	✓	-	-	-
103h		GPT8_CMPD	✓	✓	✓	-	-	-
104h		GPT8_CMPE	✓	✓	✓	-	-	-
105h		GPT8_CMPF	✓	✓	✓	-	-	-
106h		GPT8_OVF	✓	✓	✓	-	-	-
107h		GPT8_UDF	✓	✓	✓	-	-	-
10Ah	GPT329	GPT9_CCMPA	✓	✓	✓	-	-	-
10Bh		GPT9_CCMPB	✓	✓	✓	-	-	-
10Ch		GPT9_CMPC	✓	✓	✓	-	-	-
10Dh		GPT9_CMPD	✓	✓	✓	-	-	-
10Eh		GPT9_CMPE	✓	✓	✓	-	-	-
10Fh		GPT9_CMPF	✓	✓	✓	-	-	-
110h		GPT9_OVF	✓	✓	✓	-	-	-
111h		GPT9_UDF	✓	✓	✓	-	-	-
114h	GPT3210	GPT10_CCMPA	✓	✓	✓	-	-	-
115h		GPT10_CCMPB	✓	✓	✓	-	-	-
116h		GPT10_CMPC	✓	✓	✓	-	-	-
117h		GPT10_CMPD	✓	✓	✓	-	-	-
118h		GPT10_CMPE	✓	✓	✓	-	-	-
119h		GPT10_CMPF	✓	✓	✓	-	-	-
11Ah		GPT10_OVF	✓	✓	✓	-	-	-
11Bh		GPT10_UDF	✓	✓	✓	-	-	-
11Eh	GPT3211	GPT11_CCMPA	✓	✓	✓	-	-	-
11Fh		GPT11_CCMPB	✓	✓	✓	-	-	-
120h		GPT11_CMPC	✓	✓	✓	-	-	-
121h		GPT11_CMPD	✓	✓	✓	-	-	-
122h		GPT11_CMPE	✓	✓	✓	-	-	-
123h		GPT11_CMPF	✓	✓	✓	-	-	-
124h		GPT11_OVF	✓	✓	✓	-	-	-
125h		GPT11_UDF	✓	✓	✓	-	-	-

Table 14.4 事件表（6个，共9个）

事件编号	中断请求源	Name	IELSRn		DELSRn	Canceling 贪睡模式	取消软件待机模式	取消深度软件待机模式
			连接到NVIC	Invoke DTC	Invoke DMAC			
0F6h	GPT32E7	GPT7_CCMPA	✓	✓	✓	-	-	-
0F7h		GPT7_CCMPB	✓	✓	✓	-	-	-
0F8h		GPT7_CMPC	✓	✓	✓	-	-	-
0F9h		GPT7_CMPD	✓	✓	✓	-	-	-
0FAh		GPT7_CMPE	✓	✓	✓	-	-	-
0FBh		GPT7_CMPF	✓	✓	✓	-	-	-
0FCh		GPT7_OVF	✓	✓	✓	-	-	-
0FDh		GPT7_UDF	✓	✓	✓	-	-	-
0FEh		GPT7_ADTRGA	✓	✓	✓	-	-	-
0FFh		GPT7_ADTRGB	✓	✓	✓	-	-	-
100h	GPT328	GPT8_CCMPA	✓	✓	✓	-	-	-
101h		GPT8_CCMPB	✓	✓	✓	-	-	-
102h		GPT8_CMPC	✓	✓	✓	-	-	-
103h		GPT8_CMPD	✓	✓	✓	-	-	-
104h		GPT8_CMPE	✓	✓	✓	-	-	-
105h		GPT8_CMPF	✓	✓	✓	-	-	-
106h		GPT8_OVF	✓	✓	✓	-	-	-
107h		GPT8_UDF	✓	✓	✓	-	-	-
10Ah	GPT329	GPT9_CCMPA	✓	✓	✓	-	-	-
10Bh		GPT9_CCMPB	✓	✓	✓	-	-	-
10Ch		GPT9_CMPC	✓	✓	✓	-	-	-
10Dh		GPT9_CMPD	✓	✓	✓	-	-	-
10Eh		GPT9_CMPE	✓	✓	✓	-	-	-
10Fh		GPT9_CMPF	✓	✓	✓	-	-	-
110h		GPT9_OVF	✓	✓	✓	-	-	-
111h		GPT9_UDF	✓	✓	✓	-	-	-
114h	GPT3210	GPT10_CCMPA	✓	✓	✓	-	-	-
115h		GPT10_CCMPB	✓	✓	✓	-	-	-
116h		GPT10_CMPC	✓	✓	✓	-	-	-
117h		GPT10_CMPD	✓	✓	✓	-	-	-
118h		GPT10_CMPE	✓	✓	✓	-	-	-
119h		GPT10_CMPF	✓	✓	✓	-	-	-
11Ah		GPT10_OVF	✓	✓	✓	-	-	-
11Bh		GPT10_UDF	✓	✓	✓	-	-	-
11Eh	GPT3211	GPT11_CCMPA	✓	✓	✓	-	-	-
11Fh		GPT11_CCMPB	✓	✓	✓	-	-	-
120h		GPT11_CMPC	✓	✓	✓	-	-	-
121h		GPT11_CMPD	✓	✓	✓	-	-	-
122h		GPT11_CMPE	✓	✓	✓	-	-	-
123h		GPT11_CMPF	✓	✓	✓	-	-	-
124h		GPT11_OVF	✓	✓	✓	-	-	-
125h		GPT11_UDF	✓	✓	✓	-	-	-

Table 14.4 Event table (7 of 9)

Event number	Interrupt request source	Name	IELSRn		DELSRn	Canceling Snooze mode	Canceling Software Standby mode	Canceling Deep Software Standby mode
			Connect to NVIC	Invoke DTC	Invoke DMAC			
128h	GPT3212	GPT12_CCMPA	✓	✓	✓	-	-	-
129h		GPT12_CCMPB	✓	✓	✓	-	-	-
12Ah		GPT12_CMPC	✓	✓	✓	-	-	-
12Bh		GPT12_CMPD	✓	✓	✓	-	-	-
12Ch		GPT12_CMPE	✓	✓	✓	-	-	-
12Dh		GPT12_CMPF	✓	✓	✓	-	-	-
12Eh		GPT12_OVF	✓	✓	✓	-	-	-
12Fh		GPT12_UDF	✓	✓	✓	-	-	-
132h	GPT3213	GPT13_CCMPA	✓	✓	✓	-	-	-
133h		GPT13_CCMPB	✓	✓	✓	-	-	-
134h		GPT13_CMPC	✓	✓	✓	-	-	-
135h		GPT13_CMPD	✓	✓	✓	-	-	-
136h		GPT13_CMPE	✓	✓	✓	-	-	-
137h		GPT13_CMPF	✓	✓	✓	-	-	-
138h		GPT13_OVF	✓	✓	✓	-	-	-
139h		GPT13_UDF	✓	✓	✓	-	-	-
150h	GPT	GPT_UVWEDGE	✓			-	-	-
160h	Ethernet Controller	ETHER_IPLS	✓	✓	✓	-	-	-
161h		ETHER_MINT	✓	-	-	-	-	-
162h		ETHER_PINT	✓	-	-	-	-	-
163h		ETHER_EINT0	✓	-	-	-	-	-
171h	USBHS	USBHS_D0FIFO	✓	✓	✓	-	-	-
172h		USBHS_D1FIFO	✓	✓	✓	-	-	-
173h		USBHS_USBIR	✓	-	-	✓	✓	✓
174h	SCI0	SCI0_RXI	✓	✓	✓	-	-	-
175h		SCI0_TXI	✓	✓	✓	-	-	-
176h		SCI0_TEI	✓	-	-	-	-	-
177h		SCI0_ERI	✓	-	-	-	-	-
178h		SCI0_AM	✓	-	-	✓*5	-	-
179h		SCI0_RXI_OR_ERI	-	-	-	✓*5	-	-
17Ah	SCI1	SCI1_RXI	✓	✓	✓	-	-	-
17Bh		SCI1_TXI	✓	✓	✓	-	-	-
17Ch		SCI1_TEI	✓	-	-	-	-	-
17Dh		SCI1_ERI	✓	-	-	-	-	-
17Eh		SCI1_AM	✓	-	-	-	-	-
180h	SCI2	SCI2_RXI	✓	✓	✓	-	-	-
181h		SCI2_TXI	✓	✓	✓	-	-	-
182h		SCI2_TEI	✓	-	-	-	-	-
183h		SCI2_ERI	✓	-	-	-	-	-
184h		SCI2_AM	✓	-	-	-	-	-
186h	SCI3	SCI3_RXI	✓	✓	✓	-	-	-
187h		SCI3_TXI	✓	✓	✓	-	-	-
188h		SCI3_TEI	✓	-	-	-	-	-
189h		SCI3_ERI	✓	-	-	-	-	-
18Ah		SCI3_AM	✓	-	-	-	-	-

Table 14.4 事件表（7个，共9个）

事件编号	中断请求源	Name	IELSRn		DELSRn	Canceling 贪睡模式	取消软件待机模式	取消深度软件待机模式
			连接到NVIC	Invoke DTC	Invoke DMAC			
128h	GPT3212	GPT12_CCMPA	✓	✓	✓	-	-	-
129h		GPT12_CCMPB	✓	✓	✓	-	-	-
12Ah		GPT12_CMPC	✓	✓	✓	-	-	-
12Bh		GPT12_CMPD	✓	✓	✓	-	-	-
12Ch		GPT12_CMPE	✓	✓	✓	-	-	-
12Dh		GPT12_CMPF	✓	✓	✓	-	-	-
12Eh		GPT12_OVF	✓	✓	✓	-	-	-
12Fh		GPT12_UDF	✓	✓	✓	-	-	-
132h	GPT3213	GPT13_CCMPA	✓	✓	✓	-	-	-
133h		GPT13_CCMPB	✓	✓	✓	-	-	-
134h		GPT13_CMPC	✓	✓	✓	-	-	-
135h		GPT13_CMPD	✓	✓	✓	-	-	-
136h		GPT13_CMPE	✓	✓	✓	-	-	-
137h		GPT13_CMPF	✓	✓	✓	-	-	-
138h		GPT13_OVF	✓	✓	✓	-	-	-
139h		GPT13_UDF	✓	✓	✓	-	-	-
150h	GPT	GPT_UVWEDGE	✓			-	-	-
160h	以太网控制器	ETHER_IPLS	✓	✓	✓	-	-	-
161h		ETHER_MINT	✓	-	-	-	-	-
162h		ETHER_PINT	✓	-	-	-	-	-
163h		ETHER_EINT0	✓	-	-	-	-	-
171h	USBHS	USBHS_D0FIFO	✓	✓	✓	-	-	-
172h		USBHS_D1FIFO	✓	✓	✓	-	-	-
173h		USBHS_USBIR	✓	-	-	✓	✓	✓
174h	SCI0	SCI0_RXI	✓	✓	✓	-	-	-
175h		SCI0_TXI	✓	✓	✓	-	-	-
176h		SCI0_TEI	✓	-	-	-	-	-
177h		SCI0_ERI	✓	-	-	-	-	-
178h		SCI0_AM	✓	-	-	✓*5	-	-
179h		SCI0_RXI_OR_ERI	-	-	-	✓*5	-	-
17Ah	SCI1	SCI1_RXI	✓	✓	✓	-	-	-
17Bh		SCI1_TXI	✓	✓	✓	-	-	-
17Ch		SCI1_TEI	✓	-	-	-	-	-
17Dh		SCI1_ERI	✓	-	-	-	-	-
17Eh		SCI1_AM	✓	-	-	-	-	-
180h	SCI2	SCI2_RXI	✓	✓	✓	-	-	-
181h		SCI2_TXI	✓	✓	✓	-	-	-
182h		SCI2_TEI	✓	-	-	-	-	-
183h		SCI2_ERI	✓	-	-	-	-	-
184h		SCI2_AM	✓	-	-	-	-	-
186h	SCI3	SCI3_RXI	✓	✓	✓	-	-	-
187h		SCI3_TXI	✓	✓	✓	-	-	-
188h		SCI3_TEI	✓	-	-	-	-	-
189h		SCI3_ERI	✓	-	-	-	-	-
18Ah		SCI3_AM	✓	-	-	-	-	-

Table 14.4 Event table (8 of 9)

Event number	Interrupt request source	Name	IELSRn		DELSRn	Canceling Snooze mode	Canceling Software Standby mode	Canceling Deep Software Standby mode
			Connect to NVIC	Invoke DTC	Invoke DMAC			
18Ch	SCI4	SCI4_RXI	✓	✓	✓	-	-	-
18Dh		SCI4_TXI	✓	✓	✓	-	-	-
18Eh		SCI4_TEI	✓	-	-	-	-	-
18Fh		SCI4_ERI	✓	-	-	-	-	-
190h		SCI4_AM	✓	-	-	-	-	-
192h	SCI5	SCI5_RXI	✓	✓	✓	-	-	-
193h		SCI5_TXI	✓	✓	✓	-	-	-
194h		SCI5_TEI	✓	-	-	-	-	-
195h		SCI5_ERI	✓	-	-	-	-	-
196h		SCI5_AM	✓	-	-	-	-	-
198h	SCI6	SCI6_RXI	✓	✓	✓	-	-	-
199h		SCI6_TXI	✓	✓	✓	-	-	-
19Ah		SCI6_TEI	✓	-	-	-	-	-
19Bh		SCI6_ERI	✓	-	-	-	-	-
19Ch		SCI6_AM	✓	-	-	-	-	-
19Eh	SCI7	SCI7_RXI	✓	✓	✓	-	-	-
19Fh		SCI7_TXI	✓	✓	✓	-	-	-
1A0h		SCI7_TEI	✓	-	-	-	-	-
1A1h		SCI7_ERI	✓	-	-	-	-	-
1A2h		SCI7_AM	✓	-	-	-	-	-
1A4h	SCI8	SCI8_RXI	✓	✓	✓	-	-	-
1A5h		SCI8_TXI	✓	✓	✓	-	-	-
1A6h		SCI8_TEI	✓	-	-	-	-	-
1A7h		SCI8_ERI	✓	-	-	-	-	-
1A8h		SCI8_AM	✓	-	-	-	-	-
1AAh	SCI9	SCI9_RXI	✓	✓	✓	-	-	-
1ABh		SCI9_TXI	✓	✓	✓	-	-	-
1ACh		SCI9_TEI	✓	-	-	-	-	-
1ADh		SCI9_ERI	✓	-	-	-	-	-
1AEh		SCI9_AM	✓	-	-	-	-	-
1BCh	SPI0	SPI0_SPRI	✓	✓	✓	-	-	-
1BDh		SPI0_SPTI	✓	✓	✓	-	-	-
1BEh		SPI0_SPII	✓	-	-	-	-	-
1BFh		SPI0_SPEI	✓	-	-	-	-	-
1C0h		SPI0_SPTEND	✓	-	-	-	-	-
1C1h	SPI1	SPI1_SPRI	✓	✓	✓	-	-	-
1C2h		SPI1_SPTI	✓	✓	✓	-	-	-
1C3h		SPI1_SPII	✓	-	-	-	-	-
1C4h		SPI1_SPEI	✓	-	-	-	-	-
1C5h		SPI1_SPTEND	✓	-	-	-	-	-
1C6h	QSPI	QSPI_INTR	✓	-	-	-	-	-
1C7h	SDHI0	SDHI_MMC0_ACCS	✓	-	-	-	-	-
1C8h		SDHI_MMC0_SDIO	✓	-	-	-	-	-
1C9h		SDHI_MMC0_CARD	✓	-	-	-	-	-
1CAh		SDHI_MMC0_ODMSDBREQ	-	✓	✓	-	-	-

Table 14.4 事件表（8个，共9个）

事件编号	中断请求源	Name	IELSRn		DELSRn	Canceling 贪睡模式	取消软件待机模式	取消深度软件待机模式
			连接到NVIC	Invoke DTC	Invoke DMAC			
18Ch	SCI4	SCI4_RXI	✓	✓	✓	-	-	-
18Dh		SCI4_TXI	✓	✓	✓	-	-	-
18Eh		SCI4_TEI	✓	-	-	-	-	-
18Fh		SCI4_ERI	✓	-	-	-	-	-
190h		SCI4_AM	✓	-	-	-	-	-
192h	SCI5	SCI5_RXI	✓	✓	✓	-	-	-
193h		SCI5_TXI	✓	✓	✓	-	-	-
194h		SCI5_TEI	✓	-	-	-	-	-
195h		SCI5_ERI	✓	-	-	-	-	-
196h		SCI5_AM	✓	-	-	-	-	-
198h	SCI6	SCI6_RXI	✓	✓	✓	-	-	-
199h		SCI6_TXI	✓	✓	✓	-	-	-
19Ah		SCI6_TEI	✓	-	-	-	-	-
19Bh		SCI6_ERI	✓	-	-	-	-	-
19Ch		SCI6_AM	✓	-	-	-	-	-
19Eh	SCI7	SCI7_RXI	✓	✓	✓	-	-	-
19Fh		SCI7_TXI	✓	✓	✓	-	-	-
1A0h		SCI7_TEI	✓	-	-	-	-	-
1A1h		SCI7_ERI	✓	-	-	-	-	-
1A2h		SCI7_AM	✓	-	-	-	-	-
1A4h	SCI8	SCI8_RXI	✓	✓	✓	-	-	-
1A5h		SCI8_TXI	✓	✓	✓	-	-	-
1A6h		SCI8_TEI	✓	-	-	-	-	-
1A7h		SCI8_ERI	✓	-	-	-	-	-
1A8h		SCI8_AM	✓	-	-	-	-	-
1AAh	SCI9	SCI9_RXI	✓	✓	✓	-	-	-
1ABh		SCI9_TXI	✓	✓	✓	-	-	-
1ACh		SCI9_TEI	✓	-	-	-	-	-
1ADh		SCI9_ERI	✓	-	-	-	-	-
1AEh		SCI9_AM	✓	-	-	-	-	-
1BCh	SPI0	SPI0_SPRI	✓	✓	✓	-	-	-
1BDh		SPI0_SPTI	✓	✓	✓	-	-	-
1BEh		SPI0_SPII	✓	-	-	-	-	-
1BFh		SPI0_SPEI	✓	-	-	-	-	-
1C0h		SPI0_SPTEND	✓	-	-	-	-	-
1C1h	SPI1	SPI1_SPRI	✓	✓	✓	-	-	-
1C2h		SPI1_SPTI	✓	✓	✓	-	-	-
1C3h		SPI1_SPII	✓	-	-	-	-	-
1C4h		SPI1_SPEI	✓	-	-	-	-	-
1C5h		SPI1_SPTEND	✓	-	-	-	-	-
1C6h	QSPI	QSPI_INTR	✓	-	-	-	-	-
1C7h	SDHI0	SDHI_MMC0_ACCS	✓	-	-	-	-	-
1C8h		SDHI_MMC0_SDIO	✓	-	-	-	-	-
1C9h		SDHI_MMC0_CARD	✓	-	-	-	-	-
1CAh		SDHI_MMC0_ODMSDBREQ	-	✓	✓	-	-	-

Table 14.4 Event table (9 of 9)

Event number	Interrupt request source	Name	IELSRn		DELSRn	Canceling Snooze mode	Canceling Software Standby mode	Canceling Deep Software Standby mode
			Connect to NVIC	Invoke DTC	Invoke DMAC			
1CBh	SDHI1	SDHI_MMC1_ACCS	✓	-	-	-	-	-
1CCh		SDHI_MMC1_SDIO	✓	-	-	-	-	-
1CDh		SDHI_MMC1_CARD	✓	-	-	-	-	-
1CEh		SDHI_MMC1_ODMSDBREQ	-	✓	✓	-	-	-
1FAh	GLCDC	GLCDC_VPOS	✓	-	-	-	-	-
1FBh		GLCDC_L1UNDF	✓	-	-	-	-	-
1FCh		GLCDC_L2UNDF	✓	-	-	-	-	-
1FDh	DRW	DRW_IRQ	✓	-	-	-	-	-
1FEh	JPEG	JPEG_JEDI	✓	-	-	-	-	-
1FFh		JPEG_JDTI	✓	-	-	-	-	-

Note 1. Only supported when CMPCTL0.CSTEN = 1.
Note 2. Only supported when KRCTL.KRMD = 1.
Note 3. Only the first edge detection is valid.
Note 4. Only interrupts after DTC transfer are supported.
Note 5. Using SELSR0.

14.4 Interrupt Operation

The ICU performs the following functions:

- Detecting interrupts
- Enabling and disabling interrupts
- Selecting interrupt request destinations such as CPU interrupt, DTC activation, or DMAC activation.

14.4.1 Detecting Interrupts

External pin interrupt requests are detected by either the edge or level (falling edge, rising edge, rising and falling edges, or low level) of the interrupt signal. Set the IRQMD[1:0] bits in the IRQCRi register to select the detection mode for the IRQi pins. For interrupt sources associated with peripheral modules, see section 14.3.2, Event Numbers. Events must be accepted by the NVIC before an interrupt occurs and is accepted by the CPU.

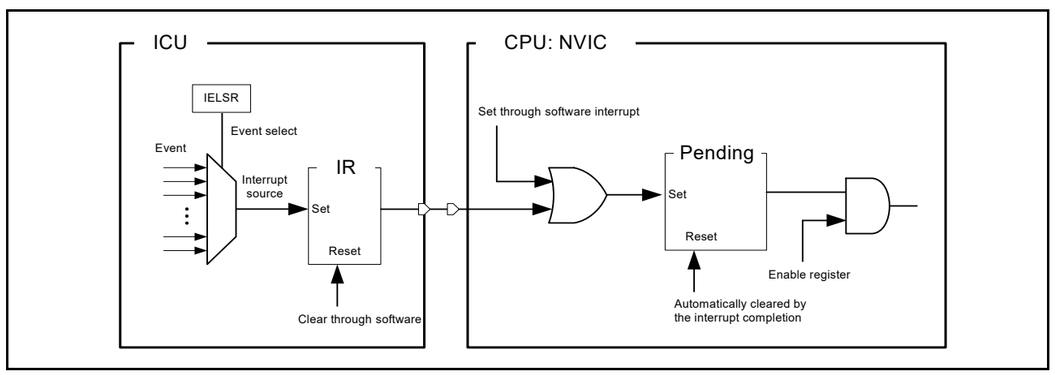


Figure 14.2 Interrupt path of the ICU and CPU: NVIC

Use the procedures in this section to detect interrupts:

- General operations during an interrupt
  - When a non-software interrupt occurs:
    The IELSRn.IR flag and Interrupt Set/Clear-Pending register (NVIC) are set.

Table 14.4 事件表（9个中的9个）

事件编号	中断请求源	Name	IELSRn		DELSRn	Canceling 贪睡模式	取消软件待机模式	取消深度软件待机模式
			连接到NVIC	Invoke DTC	Invoke DMAC			
1CBh	SDHI1	SDHI_MMC1_ACCS	✓	-	-	-	-	-
1CCh		SDHI_MMC1_SDIO	✓	-	-	-	-	-
1CDh		SDHI_MMC1_CARD	✓	-	-	-	-	-
1CEh		SDHI_MMC1_ODMSDBREQ	-	✓	✓	-	-	-
1FAh	GLCDC	GLCDC_VPOS	✓	-	-	-	-	-
1FBh		GLCDC_L1UNDF	✓	-	-	-	-	-
1FCh		GLCDC_L2UNDF	✓	-	-	-	-	-
1FDh	DRW	DRW_IRQ	✓	-	-	-	-	-
1FEh	JPEG	JPEG_JEDI	✓	-	-	-	-	-
1FFh		JPEG_JDTI	✓	-	-	-	-	-

Note 1. 仅当CMPCTL0.CSTEN=1时支持。
Note 2. 仅当KRCTL.KRMD=1时支持。
Note 3. 只有第一个边缘检测有效。
Note 4. 仅支持DTC传输后的中断。
Note 5. Using SELSR0.

14.4 中断操作

ICU执行以下功能：

- 检测中断
- 启用和禁用中断
- 选择中断请求目标，例如CPU中断、DTC激活或DMAC激活。

14.4.1 检测中断

通过中断信号的边沿或电平（下降沿、上升沿、上升沿和下降沿或低电平）来检测外部引脚中断请求。设置IRQCRi寄存器中的IRQMD[1:0]位以选择IRQi引脚的检测模式。对于与外围模块相关的中断源，请参见第14.3.2节，事件编号。事件必须在中断发生之前被NVIC接受并被CPU接受。

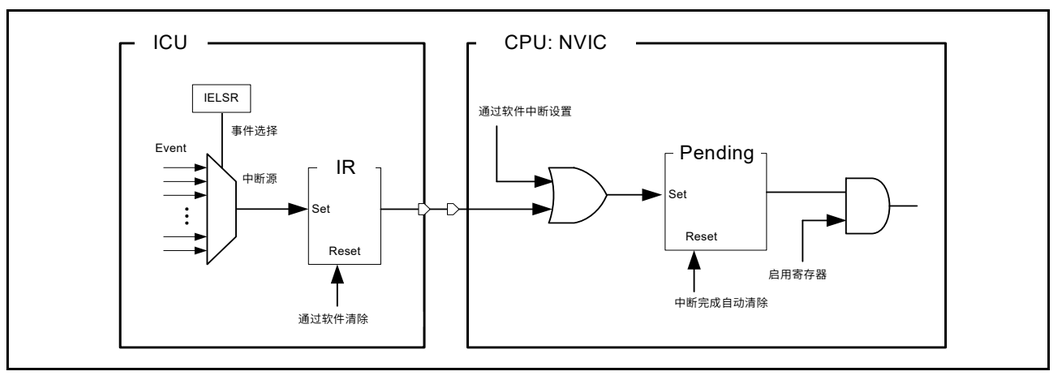


Figure 14.2 ICU和CPU的中断路径：NVIC

使用本节中的过程来检测中断：

- 中断期间的一般操作
  - 当发生非软件中断时：
    IELSRn.IR标志和中断设置清除挂起寄存器(NVIC)已设置。

- When a software interrupt occurs:
  Set the Interrupt Set-Pending register.
- When an interrupt is complete:
  Clear the IELSRn.IR flag in the software.
  The Interrupt Set/Clear-Pending register clears automatically.

- When interrupts are enabled
  a. Set the Interrupt Set-Enable register (NVIC).
  b. Set the IELSRn.IELS bits as the interrupt source.
  c. Specify the operation settings for the event source.
- When interrupts are disabled
  a. Disable the settings for the event source.
  b. Clear the IELSRn.IELS bits (IELSRn.IELS = 0000h). Clear the IELSRn.IR flag as required.
  c. Clear the Interrupt Clear-Enable register. Clear the Interrupt Clear-Pending register as required.
- When polling for interrupts
  a. Set the Interrupt Clear-Enable register (disabling interrupts).
  b. Set the IELSRn.IELS bits (selecting the source).
  c. Specify the operation settings for the event source.
  d. Poll the Interrupt Set-Pending register.
  e. When polling is no longer required, follow the procedure for clearing an interrupt when it is complete. Clear the IELSRn.IR flag in the software.

14.4.2 Selecting Interrupt Request Destinations

The interrupt output destination, CPU, DTC, or DMAC, can be independently selected for each interrupt source. The available destinations are fixed for each interrupt, as described in Table 14.4.

Note: Do not use an interrupt request destination setting that is not indicated by a "✓" in the event list (Table 14.4).

If you select the CPU or DTC in one IELSRn register, setting the same interrupt factor in any other IELSRn register is prohibited. Similarly, if you select the DMAC in one DELSRn register, setting the same interrupt factor in any other DELSRn register is prohibited.

Note: Setting the same interrupt factor for IELSRn and DELSRn is prohibited.

If the DMAC or DTC is selected as the destination for requests from an IRQi pin, you must set the IRQMD[1:0] bits in IRQCRi for that interrupt to select edge detection.

14.4.2.1 CPU interrupt request

When IELSRn.DTCE = 0, the event specified in the IELSRn register is output to the NVIC. Use the following procedure:

Set the IELSRn.IELS bits to the target event and the IELSRn.DTCE bit to 0.

14.4.2.2 DTC activation

When IELSRn.DTCE = 1, the event specified in the IELSRn register is output to the DTC. After DTC transmission completes, the associated interrupt occurs. Use the following procedure:

1. Set the IELSRn.IELS bits to the target event and the IELSRn.DTCE bit to 1.
2. Set the DTC module start bit (DTCST.DTCST) to 1.

Table 14.5 shows operation when the DTC is the request destination.

- 当发生软件中断时：
  设置中断设置挂起寄存器。
- 当中断完成时：
  清除软件中的IELSRn.IR标志。
  中断设置清除挂起寄存器自动清除。

- 启用中断时
  一个。设置中断设置启用寄存器(NVIC)。
  湾。将IELSRn.IELS位设置为中断源。
  C。指定事件源的操作设置。
- 禁用中断时
  一个。禁用事件源的设置。
  湾。清零IELSRn.IELS位（IELSRn.IELS=0000h）。根据需要清除IELSRn.IR标志。
  C。清除中断清除启用寄存器。根据需要清除中断清除挂起寄存器。
- 轮询中断时
  一个。设置中断清除启用寄存器（禁用中断）。
  湾。设置IELSRn.IELS位（选择源）。
  C。指定事件源的操作设置。
  d。轮询中断设置挂起寄存器。
  e.当不再需要轮询时，按照完成后清除中断的过程。清除软件中的IELSRn.IR标志。

14.4.2 选择中断请求目标

可以为每个中断源独立选择中断输出目标CPU、DTC或DMAC。每个中断的可用目的地都是固定的，如表14.4中所述。

Note: 请勿使用事件列表（表14.4）中未用" "表示的中断请求目标设置。

如果在一个IELSRn寄存器中选择CPU或DTC，则禁止在任何其他IELSRn寄存器中设置相同的中断因子。同样，如果您在一个DELSRn寄存器中选择DMAC，则禁止在任何其他DELSRn寄存器中设置相同的中断因子。

Note: 禁止为IELSRn和DELSRn设置相同的中断因子。

如果选择DMAC或DTC作为来自IRQi引脚的请求的目标，则必须将IRQMD[1:0]位设置为IRQCRi用于选择边缘检测的中断。

14.4.2.1 CPU中断请求

当IELSRn.DTCE=0时，将IELSRn寄存器中指定的事件输出到NVIC。使用以下过程：

将IELSRn.IELS位设置为目标事件，并将IELSRn.DTCE位设置为0。

14.4.2.2 DTC activation

当IELSRn.DTCE=1时，将IELSRn寄存器中指定的事件输出到DTC。DTC传输完成后，将发生相关中断。使用以下过程：

1. 将IELSRn.IELS位设置为目标事件，并将IELSRn.DTCE位设置为1。
2. 将DTC模块起始位(DTCST.DTCST)设置为1。

表14.5显示了DTC是请求目的地时的操作。

Table 14.5 Operations when the DTC is activated

Interrupt request destination	DISEL*1	Remaining transfer operations	Operations per request	IR*2	Interrupt request destination after transfer
DTC*3	1	≠ 0	DTC transfer → CPU interrupt	Cleared on interrupt acceptance by the CPU	DTC
		= 0	DTC transfer → CPU interrupt	Cleared on interrupt acceptance by the CPU	The IELSRn.DTCE bit is cleared and the CPU becomes the destination
	0	≠ 0	DTC transfer	Cleared at the start of DTC data transfer after DTC transfer data is read	DTC
		= 0	DTC transfer → CPU interrupt	Cleared on interrupt acceptance by the CPU	The IELSRn.DTCE bit is cleared and the CPU becomes the destination

Note 1. Set the interrupt request mode for the DTC in the DTC.MRB.DISEL bit.
Note 2. When the IELSRn.IR flag is 1, an interrupt request (DTC activation request) that occurs again is ignored.
Note 3. For chain transfers, DTC transfer continues until the last chain transfer ends. At this point, the DISEL bit state and the remaining transfer count determine whether a CPU interrupt occurs, the IELSRn.IR flag clear timing, and the interrupt request destination after transfer. See Table 18.3, Chain transfer conditions, in section 18, Data Transfer Controller (DTC).

14.4.2.3 Operations with the DMAC activated

Events specified in the DELSRn registers are output to the DMAC. When using interrupts, you must select the DMAC as the interrupt source in the IELSRn.IELS[8:0] bits and enable DMAC output by setting IELSRn.DTCE to 1. When IELSRn.DTCE is 0, the events specified in the IELSRn registers are output to the NVIC. Use the following procedure:

1. Set the DELSRn.DELS[8:0] bits to the target event.
2. When using interrupts, set the IELSRn.IELS bit to DMAC interrupts as the source, and set the IELSRn.DTCE bit to 1.
3. Set the activation source for the target DMAC channel (DMACm.DMTMD.DCTG[1:0]) to 01b (interrupt module detection).
4. Set the DMAC transfer enable bit for the target DMAC channel (DMACm.DMCNT.DTE) to 1.
5. Set the DMAC operation enable bit (DMACm.DMAST.DMST) to 1.

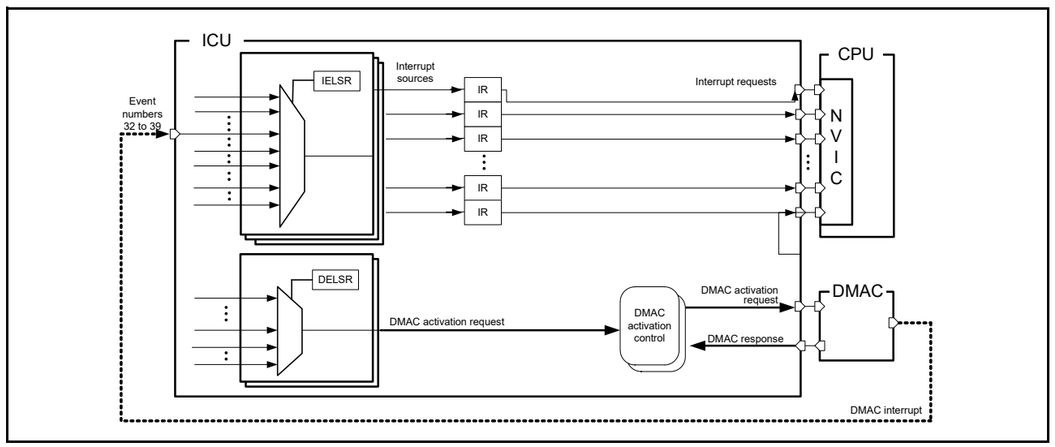


Figure 14.3 DMAC request trigger and interrupt path

Table 14.5 DTC激活时的操作

中断请求目的地	DISEL*1	剩余的转移操作	每个请求的操作	IR*2	传输后的中断请求目的地
DTC*3	1	≠ 0	DTC传输 CPU中断	CPU接受中断时清零	DTC
		= 0	DTC传输 CPU中断	CPU接受中断时清零	IELSRn.DTCE位清零，CPU成为目标
	0	≠ 0	DTC transfer	读取DTC传输数据后，在DTC数据传输开始时清零	DTC
		= 0	DTC传输 CPU中断	CPU接受中断时清零	IELSRn.DTCE位清零，CPU成为目标

Note 1. 在DTC.MRB.DISEL位中设置DTC的中断请求模式。
Note 2. IELSRn.IR标志为1时，忽略再次发生的中断请求（DTC激活请求）。
Note 3. 对于链式传输，DTC传输将持续到最后一个链式传输结束。此时，DISEL位状态和剩余传输计数决定是否发生CPU中断、IELSRn.IR标志清除时序以及传输后的中断请求目的地。请参阅第18节，数据传输控制器(DTC)中的表18.3，链传输条件。

14.4.2.3 激活DMAC的操作

在DELSRn寄存器中指定的事件被输出到DMAC。使用中断时，必须在IELSRn.IELS[8:0]位中选择DMAC作为中断源，并通过将IELSRn.DTCE设置为1来使能DMAC输出。当IELSRn.DTCE为0时，在IELSRn寄存器中指定的事件输出到NVIC。使用以下过程：

1. 将DELSrn.DELS[8:0]位设置为目标事件。
2. 使用中断时，将IELSRn.IELS位设置为DMAC中断作为源，并将IELSRn.DTCE位设置为1。
3. 将目标DMAC通道(DMACm.DMTMD.DCTG[1:0])的激活源设置为01b（中断模块检测）。
4. 将目标DMAC通道(DMACm.DMCNT.DTE)的DMAC传输使能位设置为1。
5. 将DMAC操作使能位(DMACm.DMAST.DMST)设置为1。

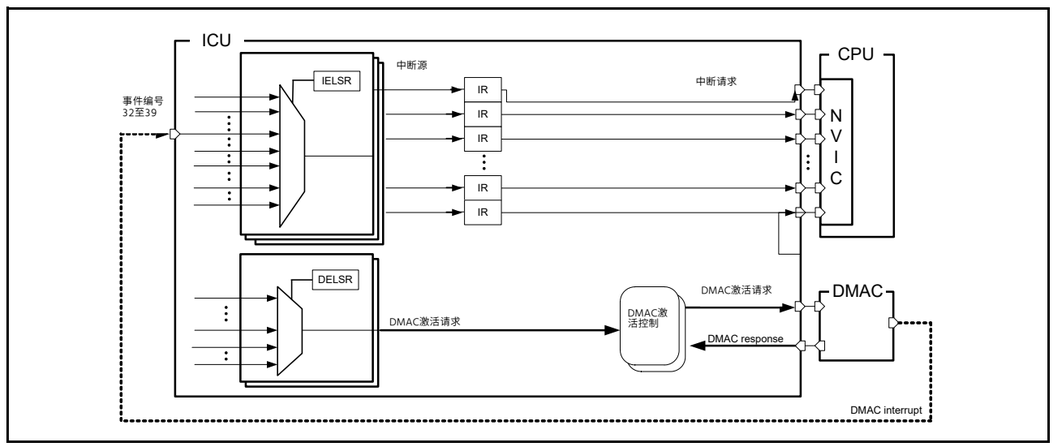


Figure 14.3 DMAC请求触发和中断路径

14.4.3 Digital Filter

A digital filter function is provided for the external interrupt request pins (IRQi, i = 0 to 15) and NMI pin interrupt. It samples input signals on the filter sampling clock (PCLKB) and removes any signal with a pulse width less than three sampling cycles.

To use the digital filter for an IRQi pin:

1. Set the sampling clock cycle to PCLKB, PCLKB/8, PCLKB/32, or PCLKB/64 in the IRQCRi.FCLKSEL[1:0] bits.
2. Set the IRQCRi.FLTEN bit to 1 (digital filter enabled).

To use the digital filter for an NMI pin:

1. Set the sampling clock cycle to PCLKB, PCLKB/8, PCLKB/32, or PCLKB/64 in the NMICR.NFCLKSEL[1:0] bits.
2. Set the NMICR.NFLTEN bit to 1 (digital filter enabled).

Figure 14.4 shows an example of digital filter operation.

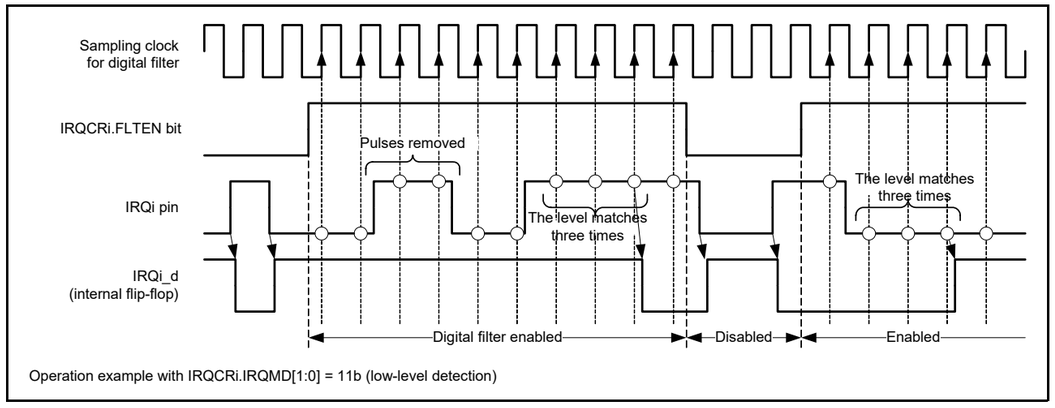


Figure 14.4 Digital filter operation example

Before entering Software Standby mode, disable the digital filters by clearing the IRQCRi.FLTEN and NMICR.NFLTEN bits. The clock for the ICU stops in Software Standby mode. On exiting Software Standby, the circuit detects the edge by comparing the state before standby to the state after standby release. If the input changes during Software Standby, an incorrect edge might be detected. You can enable the digital filters again after exiting Software Standby mode.

14.4.4 External Pin Interrupts

To use external pin interrupts:

1. Clear the IRQCRi.FLTEN bit (i = 0 to 15) to 0 (digital filter disabled).
2. Make or confirm the I/O port settings.
3. Set the IRQMD[1:0] bits, FCLKSEL[1:0] bits, and FLTEN bit of the IRQCRi register.
4. Select the IRQ pin as follows:
   - If the IRQ pin is to be used for CPU interrupt requests, set the IELSRn.IELS bits and set the IELSRn.DTCE bit to 0
   - If the IRQ pin is to be used for DTC activation, set the IELSRn.IELS bits and set the IELSRn.DTCE bit to 1
   - If the IRQ pin is to be used for DMAC activation, set the DELSRn.DELS bits.

14.4.3 数字滤波器

为外部中断请求引脚（IRQi，i=0至15）和NMI引脚中断提供了数字过滤功能。它在滤波器采样时钟(PCLKB)上对输入信号进行采样，并去除脉冲宽度小于三个采样周期的任何信号。

为IRQi引脚使用数字滤波器：

1. 在IRQCRi.FCLKSEL[1:0]位中将采样时钟周期设置为PCLKB、PCLKB8、PCLKB32或PCLKB64。
2. 将IRQCRi.FLTEN位设置为1（启用数字滤波器）。

要将数字滤波器用于NMI引脚：

1. 在NMICR.NFCLKSEL[1:0]位中将采样时钟周期设置为PCLKB、PCLKB8、PCLKB32或PCLKB64。
2. 将NMICR.NFLTEN位设置为1（启用数字滤波器）。

图14.4显示了数字滤波器操作的示例。

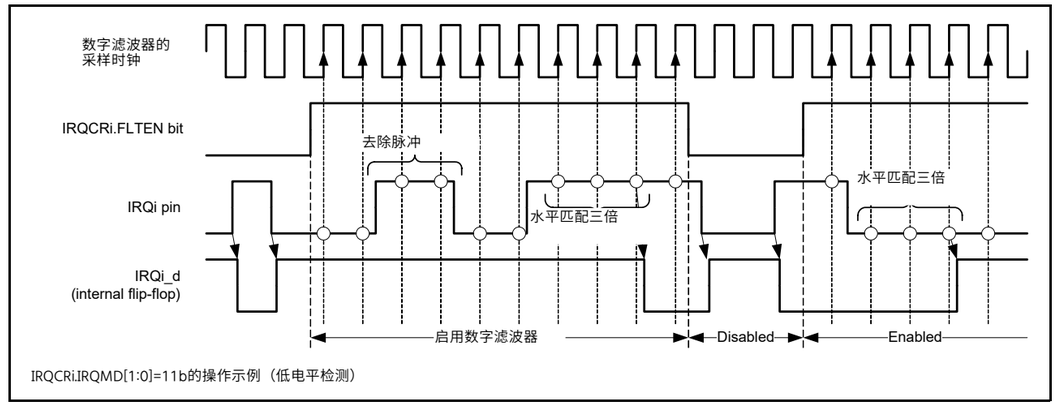


Figure 14.4 数字滤波器操作示例

在进入软件待机模式之前，通过清除IRQCRi.FLTEN和NMICR.NFLTEN位来禁用数字滤波器。ICU的时钟在软件待机模式下停止。在退出软件待机时，电路通过将待机前的状态与待机释放后的状态进行比较来检测边沿。如果在软件待机期间输入发生变化，则可能会检测到不正确的边沿。您可以在退出软件待机模式后再次启用数字滤波器。

14.4.4 外部引脚中断

要使用外部引脚中断：

1. 将IRQCRi.FLTEN位（i=0到15）清零（禁用数字滤波器）。
2. 进行或确认IO端口设置。
3. 设置IRQCRi寄存器的IRQMD[1:0]位、FCLKSEL[1:0]位和FLTEN位。
4. 选择IRQ引脚如下：
   - 如果IRQ引脚用于CPU中断请求，设置IELSRn.IELS位并将IELSRn.DTCE位设置为0
   - 如果IRQ引脚用于DTC激活，设置IELSRn.IELS位并将IELSRn.DTCE位设置为1
   - 如果IRQ引脚用于DMAC激活，则设置DELSRn.DELS位。

14.5 Non-Maskable Interrupt Operation

The following sources can trigger a non-maskable interrupt:

- NMI pin interrupt
- Oscillation stop detection interrupt
- WDT underflow/refresh error interrupt
- IWDT underflow/refresh error interrupt
- Voltage monitor 1 interrupt
- Voltage monitor 2 interrupt
- SRAM parity error interrupt
- SRAM ECC error interrupt
- MPU bus master error interrupt
- MPU bus slave error interrupt
- CPU stack pointer monitor interrupt.

Non-maskable interrupts can only be used with the CPU, not to activate the DTC or DMAC. Non-maskable interrupts take precedence over all other interrupts. The non-maskable interrupt states can be verified in the Non-Maskable Interrupt Status Register (NMISR). Confirm that all bits in the NMISR are 0 before returning from the NMI handler.

Non-maskable interrupts are disabled by default. To use non-maskable interrupts, you must:

1. To use the NMI pin, clear the NMICR.NFLTEN bit to 0 (digital filter disabled).
2. To use the NMI pin, set the NMIMD bit, NFCLKSEL[1:0] bits, and NFLTEN bit of NMICR register.
3. To use the NMI pin, write 1 to the NMICLR.NMICLR bit to clear the NMISR.NMIST flag to 0.
4. Enable the non-maskable interrupt by writing 1 to the associated bit in the Non-Maskable Interrupt Enable Register (NMIER).

After 1 is written to the NMIER register, subsequent write access to the NMIEN bit in NMIER is ignored. An NMI interrupt cannot be disabled when enabled, except by a reset.

14.6 Return from Low-Power Modes

Table 14.4 lists the interrupt sources you can use to exit Sleep or Software Standby mode. For more information, see section 11, Low Power Modes. Sections 14.6.1 to 14.6.3 describe how to use interrupts to return from Sleep, Software Standby, and Snooze modes. For Deep Software Standby, see section 11.9, Deep Software Standby Mode.

14.6.1 Return from Sleep Mode

To return from Sleep mode in response to an interrupt:

1. Select the CPU as the interrupt request destination.
2. Enable the interrupt in the NVIC.

To return from Sleep mode in response to a non-maskable interrupt, enable the wanted interrupt request in the NMIER register.

14.6.2 Return from Software Standby Mode

The ICU can return from Software Standby mode using a non-maskable interrupt or an interrupt selected in the WUPEN register. See section 14.2.9, Wake Up Interrupt Enable Register (WUPEN).

To return from Software Standby mode, you must:

1. Select the interrupt source that enables return from Software Standby.

- For non-maskable interrupts, use the NMIER register to enable the wanted interrupt request

14.5 不可屏蔽中断操作

以下源可以触发不可屏蔽中断：

- NMI引脚中断
- 振荡停止检测中断
- WDT下溢刷新错误中断
- IWDT下溢刷新错误中断
- 电压监视器1中断
- 电压监视器2中断
- SRAM奇偶校验错误中断
- SRAMECC错误中断
- MPU总线主机错误中断
- MPU总线从机错误中断
- CPU堆栈指针监视中断。

不可屏蔽中断只能用于CPU，不能激活DTC或DMAC。不可屏蔽中断优先于所有其他中断。不可屏蔽中断状态可以在不可屏蔽中断状态寄存器(NMISR)中验证。在从NMI处理程序返回之前，确认NMISR中的所有位都为0。

默认情况下禁用不可屏蔽中断。要使用不可屏蔽中断，您必须：

1. 要使用NMI引脚，请将NMICR.NFLTEN位清除为0（禁用数字滤波器）。
2. 要使用NMI引脚，请设置NMICR寄存器的NMIMD位、NFCLKSEL[1:0]位和NFLTEN位。
3. 要使用NMI引脚，向NMICLR.NMICLR位写入1以将NMISR.NMIST标志清零。
4. 通过将1写入不可屏蔽中断启用寄存器(NMIER)中的相关位来启用不可屏蔽中断。

将1写入NMIER寄存器后，随后对NMIER中的NMIEN位的写访问将被忽略。启用时不能禁用NMI中断，除非通过复位。

14.6 从低功耗模式返回

表14.4列出了可用于退出睡眠或软件待机模式的中断源。有关详细信息，请参阅第11节，低功耗模式。14.6.1到14.6.3节描述了如何使用中断从休眠、软件待机和贪睡模式返回。对于深度软件待机，请参阅第11.9节，深度软件待机模式。

14.6.1 从睡眠模式返回

从睡眠模式返回以响应中断：

1. 选择CPU作为中断请求目标。
2. 在NVIC中启用中断。

要从休眠模式返回以响应不可屏蔽的中断，请在NMIER寄存器中启用所需的中断请求。

14.6.2 从软件待机模式返回

ICU可以使用不可屏蔽中断或在WUPEN寄存器中选择的中断从软件待机模式返回。请参见第14.2.9节，唤醒中断使能寄存器(WUPEN)。

要从软件待机模式返回，您必须：

1. 选择允许从软件待机返回的中断源。

- 对于不可屏蔽的中断，使用NMIER寄存器来启用想要的中断请求

- For maskable interrupts, use the WUPEN register to enable the wanted interrupt request.

2. Select the CPU as the interrupt request destination.
3. Enable the interrupt in the NVIC.

Interrupt requests through IRQ pins that do not satisfy these conditions are not detected while the clock is stopped in Software Standby mode.

14.6.3 Return from Snooze Mode

The ICU can return from Snooze mode using the interrupts provided for this mode.

To return to Normal mode from Snooze mode:

1. Use either of the following methods to select the event that you want to trigger a return from Snooze mode to Normal mode:
   - Set the event that you want to trigger a return from Snooze mode to Normal mode in SELSR0.SEL and set the value 02Dh (ICU_SNZCANCEL) in IELSRn.IELS
   - Set the event that you want to trigger a return from Snooze mode to Normal mode in IELSRn.IELS.
2. Select the CPU as the interrupt request destination.
3. Enable the interrupt in the NVIC.

Note: In Snooze mode, a clock is supplied to ICU. If an event selected in IELSRn is detected, the CPU can acknowledge the interrupt after returning to Normal mode from Software Standby mode. If an event selected in DELSRn is detected, the DMAC can acknowledge the interrupt after returning to Normal mode from Software Standby mode.

14.7 Using the WFI Instruction with Non-Maskable Interrupts

Whenever a WFI instruction is executed, confirm that all status flags in the NMISR register are 0.

14.8 Reference

ARM® Cortex®-M4 Processor Technical Reference Manual (ARM DDI 0439D).

- 对于可屏蔽中断，使用WUPEN寄存器启用所需的中断请求。

2. 选择CPU作为中断请求目标。
3. 在NVIC中启用中断。

当时钟停止时，不会检测到通过不满足这些条件的IRQ引脚的中断请求
软件待机模式。

14.6.3 从贪睡模式返回

ICU可以使用为该模式提供的中断从贪睡模式返回。

要从贪睡模式返回正常模式：

1. 使用以下任一方法选择要触发从贪睡模式返回到的事件
   Normal mode:
   - 在SELSR0.SEL中设置要触发从贪睡模式返回到正常模式的事件，并在IELSRn.IELS中设置值02Dh(ICU_SNZCANCEL)
   - 在IELSRn.IELS中设置要触发从贪睡模式返回到正常模式的事件。
2. 选择CPU作为中断请求目标。
3. 在NVIC中启用中断。

Note: 在贪睡模式下，向ICU提供时钟。如果检测到在IELSRn中选择的事件，CPU可以在从软件待机模式返回到正常模式后确认中断。如果检测到在DELSRn中选择的事件，则DMAC可以在从软件返回到正常模式后确认中断

待机模式。

14.7 将WFI指令与不可屏蔽中断一起使用

每当执行WFI指令时，请确认NMISR寄存器中的所有状态标志为0。

14.8 Reference

ARM®Cortex®-M4处理器技术参考手册(ARMDDI0439D)。

15. Buses

15.1 Overview

Table 15.1 lists the bus specifications, Figure 15.1 shows the bus configuration, and Table 15.2 lists the addresses assigned for each bus.

Table 15.1 Bus specifications

Bus type		Specifications
Main bus	ICode bus (CPU)	• Connected to the CPU • Connected to the on-chip memory (code flash memory, SRAMHS).
	DCode bus (CPU)	• Connected to the CPU • Connected to the on-chip memory (code flash memory, SRAMHS).
	System bus (CPU)	• Connected to the CPU • Connected to the on-chip memory, internal peripheral buses, and external bus.
	DMA bus	• Connected to the DMAC and DTC • Connected to the on-chip memory, internal peripheral buses, and external bus.
	ETHER bus	• Connected to the EDMAC • Connected to the on-chip memory, internal peripheral buses, and external bus.
	GPX bus	• Connected to the JPEG, GLCDC, and DRW • Connected to the on-chip memory and external bus.
Slave interface	Memory bus 1	• Connected to code flash memory
	Memory bus 2	• Connected to the SRAMHS
	Memory bus 3	• Connected to code flash memory and SRAMHS through the DMA bus, ETHER bus, and GPX bus
	Memory bus 4	• Connected to SRAM0
	Memory bus 5	• Connected to SRAM1 and the Standby SRAM
	Internal peripheral bus 1	• Connected to system control related to peripheral modules
	Internal peripheral bus 3	• Connected to peripheral modules (CAC, ELC, I/O ports, POEG, RTC, WDT, IWDT, IIC, CAN, SSIE, SRC, ADC12, DAC12, TSN, and DOC)
	Internal peripheral bus 4	• Connected to peripheral modules (GPT, ETHERC, EPTPC, EDMAC, USBHS, SCI, IrDA, SPI, CRC, and SDHI)
	Internal peripheral bus 5	• Connected to peripheral modules (KINT, AGT, USBFS, PDC, ACMPHS, and CTSU)
	Internal peripheral bus 7	• Connected to Secure IPs (SCE7)
	Internal peripheral bus 8	• Connected to graphic IPs (JPEG, GLCDC, and DRW)
	Internal peripheral bus 9	• Connected to flash memory (in P/E)*1, data flash memory, and TSN
External bus	CS area	• Connected to the external devices
	SDRAM area	• Connected to SDRAM
	QSPI area	• Connected to the external SPI devices

Note 1. P/E: Programming and erasure.

15. Buses

15.1 Overview

表15.1列出了总线规格，图15.1显示了总线配置，表15.2列出了分配给每个总线的地址。

Table 15.1 总线规格

巴士类型		Specifications
主要总线	ICode bus (CPU)	连接到CPU 连接到片上存储器（代码闪存，SRAMHS）。
	DCode bus (CPU)	连接到CPU 连接到片上存储器（代码闪存，SRAMHS）。
	系统总线(CPU)	连接到CPU 连接到片上存储器、内部外围总线和外部总线。
	DMA bus	连接到DMAC和DTC 连接到片上存储器、内部外围总线和外部总线。
	以太总线	连接到EDMAC 连接到片上存储器、内部外围总线和外部总线。
	GPX bus	连接到JPEG、GLCDC和DRW 连接到片上存储器和外部总线。
从接口	内存总线1	连接到代码闪存
	内存总线2	连接到SRAMHS
	内存总线3	通过DMA总线、ETHER总线和GPX总线连接到代码闪存和SRAMHS
	内存总线4	连接到SRAM0
	内存总线5	连接到SRAM1和备用SRAM
	内部外围总线1	连接到与外围模块相关的系统控制
	内部外围总线3	连接外围模块（CAC、ELC、IO端口、POEG、RTC、WDT、IWDT、IIC、CAN、SSIE、SRC、ADC12、DAC12、TSN和DOC）
	内部外围总线4	连接到外围模块（GPT、ETHERC、EPTPC、EDMAC、USBHS、SCI、IrDA、SPI、CRC和SDHI）
	内部外围总线5	连接到外围模块（KINT、AGT、USBFS、PDC、ACMPHS和CTSU）
	内部外围总线7	连接到安全IP(SCE7)
	内部外围总线8	连接到图形IP（JPEG、GLCDC和DRW）
	内部外围总线9	连接到闪存（在PE中）*1、数据闪存和TSN
外部总线	CS area	连接到外部设备
	SDRAM area	连接到SDRAM
	QSPI area	连接到外部SPI设备

注1.PE：编程和擦除。

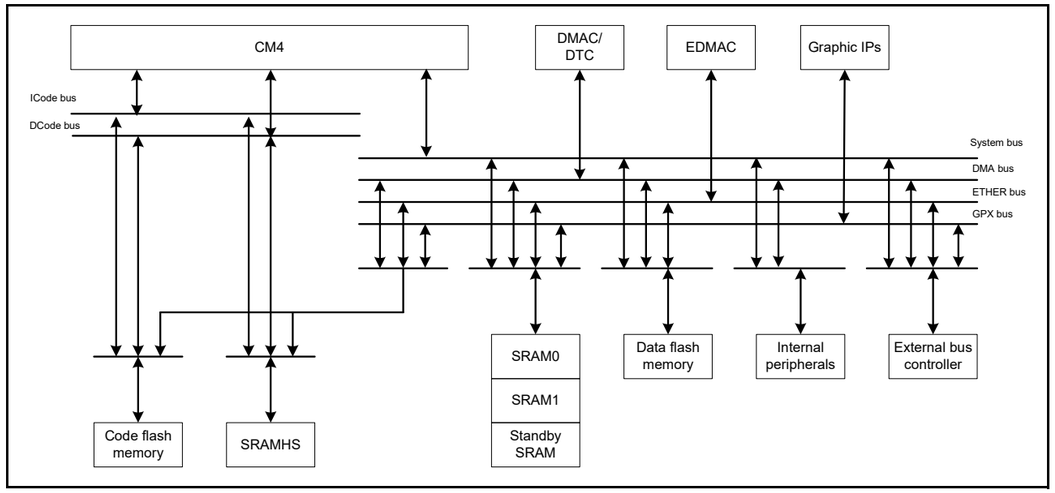


Figure 15.1 Bus configuration

Table 15.2 Addresses assigned for each bus

Addresses	Bus	Area
0000 0000h to 01FF FFFFh	Memory bus 1, 3	Code flash memory
1FFE 0000h to 1FFF FFFFh	Memory bus 2, 3	SRAMHS
2000 0000h to 2003 FFFFh	Memory bus 4	SRAM0
2004 0000h to 200F FFFFh	Memory bus 5	SRAM1 and Standby SRAM
4000 0000h to 4001 FFFFh	Internal peripheral bus 1	Peripheral I/O registers
4004 0000h to 4005 FFFFh	Internal peripheral bus 3	
4006 0000h to 4007 FFFFh	Internal peripheral bus 4	
4008 0000h to 4009 FFFFh	Internal peripheral bus 5	
400C 0000h to 400D FFFFh	Internal peripheral bus 7	Secure IPs
400E 0000h to 400F FFFFh	Internal peripheral bus 8	Graphic IPs (JPEG, GLCDC, and DRW)
4010 0000h to 407F FFFFh	Internal peripheral bus 9	Flash memory (in P/E*1), data flash memory, and TSN
6000 0000h to 67FF FFFFh	External bus	QSPI area
8000 0000h to 97FF FFFFh	External bus	CS area and SDRAM area

Note 1. P/E: Programming and erasure.

15.2 Description of Buses

15.2.1 Main Buses

The main buses for the CPU constitute the ICode bus, DCode bus, and system bus.

- The ICode and DCode buses are connected to the code flash memory and SRAMHS. The ICode bus is used for instruction access to the CPU, and the DCode bus is used for data access to the CPU.
- The system bus is connected to the SRAM0, SRAM1, Standby SRAM, data flash memory, internal peripheral buses, and external bus. It is used for instruction and data accesses to the CPU.

The main bus for modules other than the CPU consists of the DMA bus, ETHER bus, and GPX bus.

- The DMA bus is connected to the code flash memory, SRAMHS, SRAM0, SRAM1, Standby SRAM, data flash memory, and external bus.

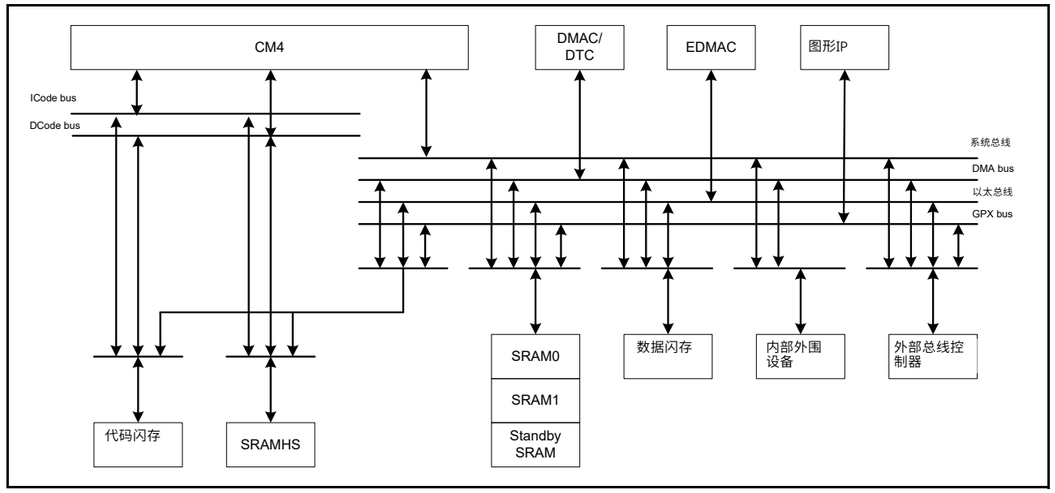


Figure 15.1 总线配置

Table 15.2 为每条总线分配的地址

Addresses	Bus	Area
0000 0000h to 01FF FFFFh	内存总线1、3	代码闪存
1FFE 0000h to 1FFF FFFFh	内存总线2、3	SRAMHS
2000 0000h to 2003 FFFFh	内存总线4	SRAM0
2004 0000h to 200F FFFFh	内存总线5	SRAM1和备用SRAM
4000 0000h to 4001 FFFFh	内部外围总线1	外设IO寄存器
4004 0000h to 4005 FFFFh	内部外围总线3	
4006 0000h to 4007 FFFFh	内部外围总线4	
4008 0000h to 4009 FFFFh	内部外围总线5	
400C 0000h to 400D FFFFh	内部外围总线7	安全IP
400E 0000h to 400F FFFFh	内部外围总线8	图形IP（JPEG、GLCDC和DRW）
4010 0000h to 407F FFFFh	内部外围总线9	闪存（在PE*1中）、数据闪存和TSN
6000 0000h to 67FF FFFFh	外部总线	QSPI area
8000 0000h to 97FF FFFFh	外部总线	CS区和SDRAM区

Note 1. PE：编程和擦除。

15.2 巴士的描述

15.2.1 主要巴士

CPU的主要总线构成ICode总线、DCode总线和系统总线。

- ICode和DCode总线连接到代码闪存和SRAMHS。ICode总线用于对CPU的指令访问，而DCode总线用于对CPU的数据访问。
- 系统总线连接到SRAM0、SRAM1、待机SRAM、数据闪存、内部外围总线和外部总线。它用于对CPU的指令和数据访问。

CPU以外的模块的主总线由DMA总线、ETHER总线和GPX总线组成。

- DMA总线连接到代码闪存、SRAMHS、SRAM0、SRAM1、待机SRAM、数据闪存和外部总线。

- The ETHER bus is connected to the code flash memory, SRAMHS, SRAM0, SRAM1, Standby SRAM, data flash memory, and external bus.
- The GPX bus is connected to the code flash memory, SRAMHS, SRAM0, SRAM1, Standby SRAM, and external bus.

Different master and slave transfer combinations can proceed simultaneously.

Arbitration between the DMAC and DTC for the mastership of the DMA bus occurs in the DMAC and DTC. The following fixed-priority order is used:

DMAC0 > DMAC1 > DMAC2 > DMAC3 > DMAC4 > DMAC5 > DMAC6 > DMAC7 > DTC.

Only one DTC and DMAC channels that have accepted the activation requests can issue bus mastership requests. In addition, requests for bus access from masters other than the DTC are not accepted during reads of transfer control information for the DTC.

Requests for mastership of the GPX bus from the JPEG, GLCDC, and DRW are arbitrated. The arbitration protocol is selectable as either fixed-priority or round-robin. For more information, see section 15.3.20, Slave Bus Control Register (BUSSCNT<slave>).

15.2.2 Slave Interface

Products using the Cortex®-M4 core contain ICode and DCode bus areas and a system bus area.

To create the ICode and DCode bus areas, a bus matrix connects the ICode bus, DCode bus, and memory bus 3 from the main bus to the slave interfaces of the code flash memory and SRAMHS. Bus access to the slave interfaces is arbitrated between the three buses. The arbitration protocol is selectable as either fixed-priority or round-robin. For more information, see section 15.3.20, Slave Bus Control Register (BUSSCNT<slave>).

To create the system bus area, a bus matrix connects the system bus, DMA bus, ETHER bus, and GPX bus from the main bus to the slave interfaces of the SRAM0, SRAM1, Standby SRAM, data flash memory, internal peripherals, and external bus. Bus access to the slave interfaces is arbitrated between the four buses. The arbitration protocol is selectable as either fixed-priority or round-robin. For more information, see section 15.3.20, Slave Bus Control Register (BUSSCNT<slave>).

For connections from the main bus to the slave interfaces, see the slave interfaces in Table 15.1. For a description of the external bus, see section 15.2.3, External Bus.

Different master and slave transfer combinations can proceed simultaneously.

15.2.3 External Bus

The external bus controller arbitrates requests for bus access on the external address space from the CPU system bus, DMAC bus, ETHER bus, and GPX bus. The priority order can be set using the external bus priority control bits (BUSSCNT.ARBMET[1:0]). For more information, see section 15.3.20, Slave Bus Control Register (BUSSCNT<slave>).

The bus system provides an external space for the QSPI. See section 39, Quad Serial Peripheral Interface (QSPI).

Table 15.3 lists the external bus specifications and Table 15.4 lists the I/O pins.

Table 15.3 External bus specifications (1 of 2)

Parameter	Specifications
External address space	• The external address space is divided into 8 CS areas (CS0 to CS7) and the SDRAM area (SDCS) for management • Chip select signals can be output for each area • The bus width can be set for each area: - Separate bus: Selectable to 8-bit or 16-bit bus space - Address/data multiplexed bus: Selectable to 8-bit or 16-bit bus space • Endian mode can be specified for each area.

- ETHER总线连接到代码闪存、SRAMHS、SRAM0、SRAM1、待机SRAM、数据闪存和外部总线。
- GPX总线连接到代码闪存、SRAMHS、SRAM0、SRAM1、备用SRAM和外部总线。

不同的主从传输组合可以同时进行。

DMAC和DTC之间对DMA总线的主控权的仲裁发生在DMAC和DTC中。使用以下固定优先级顺序：

DMAC0 > DMAC1 > DMAC2 > DMAC3 > DMAC4 > DMAC5 > DMAC6 > DMAC7 > DTC.

只有一个接受激活请求的DTC和DMAC通道可以发出总线主控请求。此外，在读取DTC的传输控制信息期间，不接受来自DTC以外的主机的总线访问请求。

对来自JPEG、GLCDC和DRW的GPX总线主控请求进行仲裁。仲裁协议可选择为固定优先级或循环。有关详细信息，请参阅第15.3.20节，从总线控制寄存器(BUSSCNT<slave>)。

15.2.2 从接口

使用Cortex®-M4内核的产品包含ICode和DCode总线区域以及系统总线区域。

为了创建ICode和DCode总线区域，总线矩阵将ICode总线、DCode总线和存储器总线3从主总线连接到代码闪存和SRAMHS的从接口。对从接口的总线访问在三个总线之间进行仲裁。仲裁协议可选择为固定优先级或循环。有关详细信息，请参阅第15.3.20节，从总线控制寄存器(BUSSCNT<slave>)。

为了创建系统总线区域，总线矩阵将系统总线、DMA总线、ETHER总线和GPX总线从主总线连接到SRAM0、SRAM1、备用SRAM、数据闪存、内部外围设备和外部公共汽车。对从接口的总线访问在四个总线之间进行仲裁。仲裁协议可选择为固定优先级或循环。有关详细信息，请参阅第15.3.20节，从总线控制寄存器(BUSSCNT<slave>)。

对于从主总线到从接口的连接，请参见表15.1中的从接口。有关外部总线的描述，请参见第15.2.3节，外部总线。

不同的主从传输组合可以同时进行。

15.2.3 外部总线

外部总线控制器对来自CPU系统总线的外部地址空间的总线访问请求进行仲裁，DMAC总线、ETHER总线和GPX总线。可以使用外部总线优先级控制位(BUSSCNT.ARBMET[1:0])设置优先级顺序。有关详细信息，请参阅第15.3.20节，从总线控制寄存器(BUSSCNT<slave>)。

总线系统为QSPI提供了一个外部空间。请参见第39节，四通道串行外设接口(QSPI)。

表15.3列出了外部总线规范，表15.4列出了IO引脚。

Table 15.3 外部总线规格（1of2）

Parameter	Specifications
外部地址空间	外部地址空间分为8个CS区（CS0到CS7）和SDRAM区（SDCS）进行管理 每个区域可以输出片选信号 可以为每个区域设置总线宽度： 独立总线：可选择8位或16位总线空间地址数据复用总线：可选择8位或16位总线空间 可为每个区域指定Endian模式。

Table 15.3 External bus specifications (2 of 2)

Parameter	Specifications
CS area controller	• Recovery cycles can be inserted: - Read recovery: Up to 15 cycles - Write recovery: Up to 15 cycles • Cycle wait function: Wait for up to 31 cycles (for page access, up to 7 cycles) • Use wait control to set up: - Assertion and negation timing of chip select signals (CS0 to CS7) - Assertion timing of the read signal (RD) and write signals (WR0/WR and WR1) - Timing of data output starts and ends • Write access modes: - Single-write strobe mode and byte strobe mode • Separate bus or address/data multiplexed bus can be set for each area.
SDRAM area controller	• Multiplexed output of row address and column address (8, 9, 10, or 11 bits) • Self-refresh and auto-refresh selectable • CAS latency can be specified from 1 to 3 cycles.
Write buffer function	When write data from the bus master is written to the write buffer, write access by the bus master is complete
Frequency	• The CS area controller (CSC) operates in synchronization with the external bus clock (BCLK)*1 • The frequency of the EBCLK pin output is the same as BCLK by default. Half of the BCLK cycles can be supplied by setting the EBCLK Pin Output Select bit, BCKCR.BCLKDIV, in the External Bus Clock Control Register. For more information, see section 9, Clock Generation Circuit. • The SDRAM area controller (SDRAMC) operates in synchronization with the SDRAM clock (SDCLK).

Note 1. BCLK and SDCLK must operate at the same frequency when the SDRAM is in use.

Table 15.4 External bus I/O pins (1 of 2)

Pin name	I/O	Description	
EBCLK, SDCLK*1	Output	CSC, SDRAMC	Clock output pin
A23 to A00*2	Output	CSC, SDRAMC	Address output pins
D15 to D00 DQ15 to DQ00	I/O	CSC, SDRAMC	D15 to D00 are CSC data input/output pins DQ15 to DQ00 are SDRAMC data input/output pins • D015 to D00, DQ15 to DQ00 pins are enabled when the 16-bit bus space is specified • D07 to D00, DQ07 to DQ00 pins are enabled when the 8-bit bus space is specified.
BC0	Output	CSC	• Strobe signal that indicates (when low) that D07 to D00 are valid during access to an external address space in single-write strobe mode, active-low • When an 8-bit bus space is specified, this output pin is always held low regardless of the write access mode.
BC1	Output	CSC	• Strobe signal that indicates (when low) that D15 to D08 are valid during access to an external address space in single-write strobe mode, active-low • This pin is not used when the 8-bit bus space is specified.
CS0*3	Output	CSC	Chip select signal for area 0 (CS0), active-low
CS1*3	Output	CSC	Chip select signal for area 1 (CS1), active-low
CS2*3	Output	CSC	Chip select signal for area 2 (CS2), active-low
CS3*3	Output	CSC	Chip select signal for area 3 (CS3), active-low
CS4	Output	CSC	Chip select signal for area 4 (CS4), active-low
CS5	Output	CSC	Chip select signal for area 5 (CS5), active-low
CS6	Output	CSC	Chip select signal for area 6 (CS6), active-low
CS7	Output	CSC	Chip select signal for area 7 (CS7), active-low
RD	Output	CSC	Strobe signal that indicates that a read from an external address space (CS0 to CS7) is in progress, active-low

Table 15.3 外部总线规范(2of2)

Parameter	Specifications
CS区域控制器	可以插入恢复周期：读取恢复：最多15个周期写入恢复：最多15个周期 循环等待功能：最多等待31个周期（对于页面访问，最多7个周期） 使用等待控制来设置： 片选信号（CS0到CS7）的断言和否定时序读信号（RD）和写信号（WR0WR和WR1）的断言时序数据输出的开始和结束时序 写访问模式： 单写选通模式和字节选通模式 可以为每个区域设置单独的总线或地址数据复用总线。
SDRAM区域控制器	行地址和列地址的多路复用输出（8、9、10或11位） 自刷新和自动刷新可选 CAS延迟可以指定为1到3个周期。
写缓冲功能	当来自总线主机的写数据被写入写缓冲区时，总线主机的写访问就完成了
Frequency	CS区域控制器(CSC)与外部总线时钟(BCLK)*1同步运行 EBCLK引脚输出的频率默认与BCLK相同。通过设置外部总线时钟控制寄存器中的EBCLK引脚输出选择位BCKCR.BCLKDIV，可以提供一半的BCLK周期。更多信息，请参见第9节，时钟生成电路。 SDRAM区域控制器(SDRAMC)与SDRAM时钟(SDCLK)同步运行。

Note 1. 在使用SDRAM时，BCLK和SDCLK 必须以相同的频率运行。

Table 15.4 外部总线IO引脚（2个中的1个）

引脚名称	I/O	Description	
EBCLK, SDCLK*1	Output	CSC, SDRAMC	时钟输出引脚
A23 to A00*2	Output	CSC, SDRAMC	地址输出引脚
D15 to D00 DQ15 to DQ00	I/O	CSC, SDRAMC	D15到D00是CSC数据输入输出引脚 DQ15到DQ00是SDRAMC数据输入输出引脚 当指定16位总线空间时启用D015到D00、DQ15到DQ00引脚 当指定8位总线空间时启用D07到D00、DQ07到DQ00引脚。
BC0	Output	CSC	指示D07到D00在单写选通模式下访问外部地址空间期间（低电平时）有效的选通信号，低电平有效 当指定8位总线空间时，该输出引脚始终保持低电平无论写访问模式如何。
BC1	Output	CSC	指示D15到D08在单写选通模式下访问外部地址空间期间（低电平时）有效的选通信号，低电平有效 当指定8位总线空间时，不使用该引脚。
CS0*3	Output	CSC	区域0(CS0)的片选信号，低电平有效
CS1*3	Output	CSC	区域1(CS1)的片选信号，低电平有效
CS2*3	Output	CSC	区域2(CS2)的片选信号，低电平有效
CS3*3	Output	CSC	区域3(CS3)的片选信号，低电平有效
CS4	Output	CSC	区域4(CS4)的片选信号，低电平有效
CS5	Output	CSC	区域5(CS5)的片选信号，低电平有效
CS6	Output	CSC	区域6(CS6)的片选信号，低电平有效
CS7	Output	CSC	区域7(CS7)的片选信号，低电平有效
RD	Output	CSC	指示正在从外部地址空间（CS0到CS7）读取的选通信号，低电平有效

Table 15.4 External bus I/O pins (2 of 2)

Pin name	I/O		Description
WR0/WR*4	Output	CSC	• WR0 signal is a strobe signal that indicates that a write to an external address space is in progress in byte strobe mode, and D07 to D00 are valid, active-low • WR signal is a strobe signal that indicates that a write to an external address space is in progress in single-write strobe mode, active-low • When an 8-bit bus space is specified, this output pin is held low during a write access regardless of the write access mode.
WR1	Output	CSC	• Strobe signal that indicates that D15 to D08 are valid during a write to an external address space in byte strobe mode, active-low • This signal is invalid in single-write strobe mode • This pin is not used when the 8-bit bus space is specified.
ALE	Output	CSC	Address latch signal when address/data multiplexed bus is selected
WAIT	Input	CSC	Wait request signal used when accessing the external address space (CS0 to CS7), active-low
CKE	Output	SDRAMC	Clock enable signal
SDCS	Output	SDRAMC	Chip select signal, active-low
RAS	Output	SDRAMC	Row address strobe signal, active-low
CAS	Output	SDRAMC	Column address strobe signal, active-low
WE	Output	SDRAMC	Write enable signal, active-low
DQM0	Output	SDRAMC	I/O data mask enable signal for DQ07 to DQ00
DQM1	Output	SDRAMC	I/O data mask enable signal for DQ15 to DQ08

Note 1. The EBCLK and the SDCLK pin functions are shared by the CS area controller (CSC) and the SDRAM area controller (SDRAMC).
When using the CSC and the SDRAMC simultaneously, the SDCLK pin function is valid.
Note 2. The A23 to A00 pin functions are shared by the CSC and the SDRAMC.
When using the CSC only:
The A00 and BC0 pin functions share the same pin, and either becomes effective according to the area, with the function being A00 in byte strobe mode and BC0 in single-write strobe mode. Setting the 8-bit external bus width is prohibited in single-write strobe mode.
When using the SDRAMC only:
The A15 to A00 pin functions are valid.
The A00 and DQM1 pin functions share the same pin, and either becomes effective according to the external bus width.
When selecting 8-bit bus width, the pin function is A00. When selecting 16-bit bus width, the pin function is DQM1.
When using the CSC and the SDRAMC simultaneously:
The A23 to A16 pin functions are valid for CSC. The A15 to A00 pin functions are shared by the CSC and the SDRAMC.
In the SDRAMC functions, the A00 and the DQM1 pin function works as described above.
In the CSC functions, the A00 and the BC0 pin function works as described above.
Note 3. The CS0 to CS3 (CSC) and SDRAMC pin functions share the same pin. When using the CSC and the SDRAMC simultaneously, the CS0 to CS3 pin functions are invalid.
Note 4. The WR0 signal and WR signal are identical. The WR0 signal is referred to as WR in single-write strobe mode.

15.2.4 Parallel Operations

Parallel operations are possible when different bus masters request access to different slave modules. For example, if the CPU fetches an instruction from the flash and an operand from the SRAM, the DMAC can handle transfers between a peripheral bus and the external bus at the same time.

An example of parallel operations is shown in Figure 15.2. In this example, the CPU uses the instruction and operand buses for simultaneous access to the flash and SRAM, respectively. Additionally, the DMAC/DTC, EDMAC, and JPEG/GLCDC/DRW simultaneously use the DMA bus (DMAC/DTC), ETHER bus (EDMAC), and GPX bus (JPEG/GLCDC/DRW) for access to a peripheral bus or external bus during access to the flash memory and SRAM by the CPU.

Table 15.4 外部总线IO引脚（2个中的2个）

引脚名称	I/O		Description
WR0/WR*4	Output	CSC	WR0信号是一个选通信号，指示在字节选通模式下正在对外部地址空间进行写入，并且D07到D00有效，低电平有效 WR信号是一个选通信号，指示对外部地址空间的写入地址空间在单写选通模式下进行中，低电平有效 当指定8位总线空间时，无论写访问模式如何，在写访问期间该输出引脚都保持低电平。
WR1	Output	CSC	指示D15到D08在字节选通模式下写入外部地址空间期间有效的选通信号，低电平有效空间被指定。
ALE	Output	CSC	选择地址数据复用总线时的地址锁存信号
WAIT	Input	CSC	访问外部地址空间（CS0到CS7）时使用的等待请求信号，低电平有效
CKE	Output	SDRAMC	时钟使能信号
SDCS	Output	SDRAMC	片选信号，低电平有效
RAS	Output	SDRAMC	行地址选通信号，低电平有效
CAS	Output	SDRAMC	列地址选通信号，低电平有效
WE	Output	SDRAMC	写使能信号，低电平有效
DQM0	Output	SDRAMC	DQ07至DQ00的IO数据屏蔽使能信号
DQM1	Output	SDRAMC	DQ15至DQ08的IO数据屏蔽使能信号

Note 1. EBCLK和SDCLK 引脚功能由CS区域控制器(CSC)和SDRAM区域控制器(SDRAMC)共享。同时使用CSC和SDRAMC时，SDCLK 引脚功能有效。
Note 2. A23至A00引脚功能由CSC和SDRAMC共享。
仅使用CSC时：
A00和BC0引脚功能共用一个引脚，根据区域分别生效，功能为A00字节选通模式和BC0单写选通模式。在单写选通模式下禁止设置8位外部总线宽度。仅使用SDRAMC时：
A15至A00引脚功能有效。
A00和DQM1引脚功能共用同一个引脚，根据外部总线宽度分别生效。
选择8位总线宽度时，引脚功能为A00。选择16位总线宽度时，引脚功能为DQM1。
同时使用CSC和SDRAMC时：
A23至A16引脚功能对CSC有效。A15至A00引脚功能由CSC和SDRAMC共享。
在SDRAMC功能中，A00和DQM1引脚功能如上所述。
在CSC功能中，A00和BC0引脚功能如上所述。
Note 3. CS0至CS3(CSC)和SDRAMC引脚功能共用同一个引脚。同时使用CSC和SDRAMC时，CS0到CS3引脚功能无效。
Note 4. WR0信号和WR信号是相同的。WR0信号在单写选通模式中称为WR。

15.2.4 并行操作

当不同的总线主机请求访问不同的从模块时，并行操作是可能的。例如，如果
CPU从闪存中获取指令，从SRAM中获取操作数，DMAC可以同时处理外设总线和外部总线之间的传输。

图15.2显示了并行操作的示例。在本例中，CPU使用指令和操作数总线分别同时访问闪存和SRAM。此外，DMACDTC、EDMAC和JPEGGLCDCDRW在访问闪存期间同时使用DMA总线(DMACDTC)、ETHER总线(EDMAC)和GPX总线(JPEGGLCDCDRW)来访问外围总线或外部总线内存和SRAM由CPU。

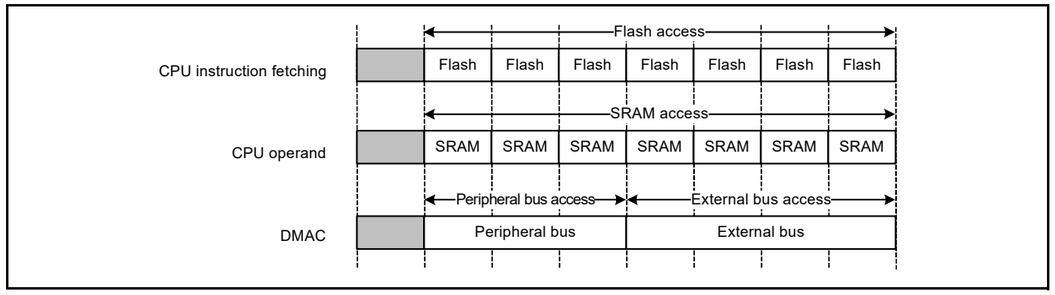


Figure 15.2 Example of parallel operations

15.2.5 Bus Settings

Set up the external bus with the following registers:

- Mode settings:
  CSn Mode Register (CSnMOD), CSn Wait Control Register 1 (CSnWCR1), CSn Wait Control Register 2 (CSnWCR2), CSn Control Register (CSnCR), CSn Recovery Cycle Setting Register (CSnREC), CS Recovery Cycle Insertion Enable Register (CSRECEN), and Bus Priority Control Register (BUSSCNT)
- I/O port assignments:
  PmnPFS.PMR = 1 and PmnPFS.PSEL[4:0] = 0Bh
- Frequency of the external bus clock (BCLK) and SDRAM clock (SDCLK):
  SCKDIVCR register.

See section 20, I/O Ports, for information on PmnPFS and section 9, Clock Generation Circuit for information on SCKDIVCR.

15.2.6 Restrictions

(1) Endianness constraint

Memory space must be little-endian to execute code on the Cortex-M4 core.

15.3 Register Descriptions

15.3.1 CSn Control Register (CSnCR) (n = 0 to 7)

Address(es): BUS.CS0CR 4000 3802h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	MPXEN	—	—	—	EMODE	—	—	BSIZE[1:0]		—	—	—	EXENB
Value after reset:	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1

Address(es): BUS.CS1CR 4000 3812h, BUS.CS2CR 4000 3822h, BUS.CS3CR 4000 3832h, BUS.CS4CR 4000 3842h, BUS.CS5CR 4000 3852h, BUS.CS6CR 4000 3862h, BUS.CS7CR 4000 3872h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	MPXEN	—	—	—	EMODE	—	—	BSIZE[1:0]		—	—	—	EXENB
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	EXENB	Operation Enable	0: Disable operation 1: Enable operation.	R/W

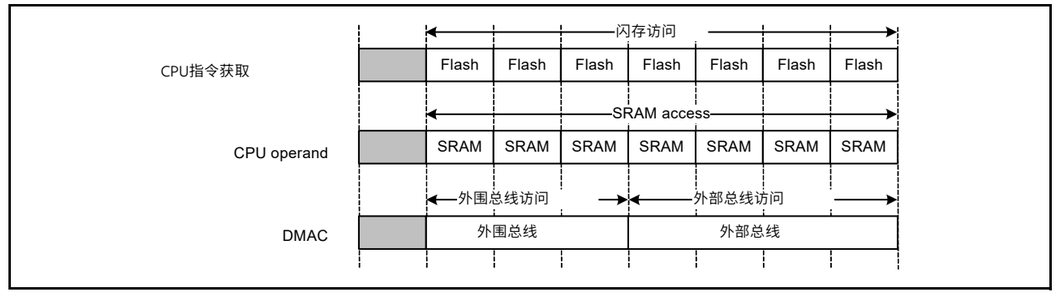


Figure 15.2 并行操作示例

15.2.5 总线设置

使用以下寄存器设置外部总线：

- Mode settings:
  CSn模式寄存器(CSnMOD) CSn等待控制寄存器1(CSnWCR1) CSn等待控制寄存器2(CSnWCR2) CSn控制寄存器(CSnCR) CSn恢复周期设置寄存器(CSnREC) CS恢复周期插入使能寄存器(CSRECEN)和总线优先级控制寄存器(BUSSCNT)
- I/O port assignments:
  PmnPFS.PMR = 1 and PmnPFS.PSEL[4:0] = 0Bh
- 外部总线时钟(BCLK)和SDRAM时钟(SDCLK)的频率：
  SCKDIVCR register.

有关PmnPFS的信息，请参见第20节，IO端口；有关有关PmnPFS的信息，请参见第9节，时钟生成电路。
SCKDIVCR.

15.2.6 Restrictions

(1) Endianness constraint

内存空间必须是little-endian才能在Cortex-M4内核上执行代码。

15.3 注册说明

15.3.1 CSn控制寄存器(CSnCR)(n=0到7)

Address(es): BUS.CS0CR 4000 3802h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	MPXEN	—	—	—	EMODE	—	—	BSIZE[1:0]		—	—	—	EXENB
重置后的值：	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1

Address(es): BUS.CS1CR 4000 3812h, BUS.CS2CR 4000 3822h, BUS.CS3CR 4000 3832h, BUS.CS4CR 4000 3842h, BUS.CS5CR 4000 3852h, BUS.CS6CR 4000 3862h, BUS.CS7CR 4000 3872h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	MPXEN	—	—	—	EMODE	—	—	BSIZE[1:0]		—	—	—	EXENB
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	EXENB	操作启用	0：禁用操作1：启用操作。	R/W

Bit	Symbol	Bit name	Description	R/W
b3 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b5, b4	BSIZE[1:0]	External Bus Width Select	b5 b4 0 0: 16-bit bus space 0 1: Setting prohibited 1 0: 8-bit bus space 1 1: Setting prohibited.	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	EMODE	Endian Mode	0: Little-endian 1: Big-endian.	R/W
b11 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b12	MPXEN	Address/Data Multiplexed I/O Interface Select	0: Separate bus interface is selected for area n 1: Address/data multiplexed I/O interface is selected for area n. (n = 0 to 7).	
b15 to b13	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Do not attempt to write to the CSnCR register while the external bus is being accessed.

EXENB bit (Operation Enable)

The EXENB bit enables operation of the associated CS area. On MCU reset, operation is enabled (EXENB = 1) only for area 0. Operation in other areas is disabled (EXENB = 0). Attempts to access disabled areas have no effect.

When the CSC and SDRAMC are in use at the same time, BCLK and SDCLK must operate at the same frequency.

BSIZE[1:0] bits (External Bus Width Select)

The BSIZE[1:0] bits specify the data bus width for the associated area.

EMODE bit (Endian Mode)

The EMODE bit specifies the endianness for the associated area. The Cortex-M4 core is fixed at little-endian order, so instruction code can only be allocated to external spaces with little-endian specified. If an area is specified as big-endian, no instruction code can be allocated to it.

MPXEN bit (Address/Data Multiplexed I/O Interface Select)

Th MPXEN bit specifies separate bus interface or address/data multiplexed I/O interface of each area.

Bit	Symbol	位名称	Description	R/W
b3 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b5, b4	BSIZE[1:0]	外部总线宽度选择	b5b400：16位总线空间01：禁止设置10：8位总线空间11：禁止设置。	R/W
b7, b6	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b8	EMODE	Endian Mode	0: Little-endian 1: Big-endian.	R/W
b11 to b9	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b12	MPXEN	Address/Data Multiplexed I/O 接口选择	0：n区选择单独的总线接口1：n区选择地址数据复用IO接口。（n=0到7）。	
b15 to b13	—	Reserved	这些位被读取为0。写入值应为0。	R/W

在访问外部总线时不要尝试写入CSnCR寄存器。

EXENB位（操作使能）

EXENB位使能相关CS区域的操作。在MCU复位时，仅允许区域0的操作（EXENB=1）。禁止其他区域的操作（EXENB=0）。尝试进入残疾人区没有效果。

当CSC和SDRAMC同时使用时，BCLK和SDCLK 必须工作在相同的频率。

BSIZE[1:0]位（外部总线宽度选择）

BSIZE[1:0]位指定相关区域的数据总线宽度。

EMODE位（字节序模式）

EMODE位指定相关区域的字节顺序。Cortex-M4内核固定为little-endian顺序，因此指令代码只能分配到指定little-endian的外部空间。如果一个区域被指定为大端，则不能为其分配指令代码。

MPXEN位（地址数据复用IO接口选择）

MPXEN位指定每个区域的单独总线接口或地址数据复用IO接口。

15.3.2 CSn Recovery Cycle Register (CSnREC) (n = 0 to 7)

Address(es): BUS.CS0REC 4000 380Ah, BUS.CS1REC 4000 381Ah, BUS.CS2REC 4000 382Ah, BUS.CS3REC 4000 383Ah, BUS.CS4REC 4000 384Ah, BUS.CS5REC 4000 385Ah, BUS.CS6REC 4000 386Ah, BUS.CS7REC 4000 387Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	WRCV[3:0]				—	—	—	—	RRCV[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	RRCV[3:0]	Read Recovery	b3 b0 0 0 0 0: Do not insert any recovery cycles 0 0 0 1: Insert 1 recovery cycle 0 0 1 0: Insert 2 recovery cycles 0 0 1 1: Insert 3 recovery cycles 0 1 0 0: Insert 4 recovery cycles 0 1 0 1: Insert 5 recovery cycles 0 1 1 0: Insert 6 recovery cycles 0 1 1 1: Insert 7 recovery cycles 1 0 0 0: Insert 8 recovery cycles 1 0 0 1: Insert 9 recovery cycles 1 0 1 0: Insert 10 recovery cycles 1 0 1 1: Insert 11 recovery cycles 1 1 0 0: Insert 12 recovery cycles 1 1 0 1: Insert 13 recovery cycles 1 1 1 0: Insert 14 recovery cycles 1 1 1 1: Insert 15 recovery cycles.	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b11 to b8	WRCV[3:0]	Write Recovery	b11 b8 0 0 0 0: Do not insert any recovery cycles 0 0 0 1: Insert 1 recovery cycle 0 0 1 0: Insert 2 recovery cycles 0 0 1 1: Insert 3 recovery cycles 0 1 0 0: Insert 4 recovery cycles 0 1 0 1: Insert 5 recovery cycles 0 1 1 0: Insert 6 recovery cycles 0 1 1 1: Insert 7 recovery cycles 1 0 0 0: Insert 8 recovery cycles 1 0 0 1: Insert 9 recovery cycles 1 0 1 0: Insert 10 recovery cycles 1 0 1 1: Insert 11 recovery cycles 1 1 0 0: Insert 12 recovery cycles 1 1 0 1: Insert 13 recovery cycles 1 1 1 0: Insert 14 recovery cycles 1 1 1 1: Insert 15 recovery cycles.	R/W
b15 to b12	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Do not attempt to write to the CSnREC register while the external bus is being accessed.

When the preceding bus access is from a separate bus, CSnREC is valid when the recovery cycle insertion is enabled in the Separate Bus Recovery Cycle Insertion Enable bit (RCVENi (i = 0 to 7)) in CSRECEN. When the preceding bus access is an address/data multiplexed bus access, CSnREC is valid when the recovery cycle insertion is enabled with the Multiplexed Bus Recovery Cycle Insertion Enable bit (RCVENMj (j = 0 to 7)) in CSRECEN. For more information, see section 15.5.4, Insertion of Recovery Cycles.

RRCV[3:0] bits (Read Recovery)

The RRCV[3:0] bits specify the number of recovery cycles inserted after a read access on the external bus for CSn (n = 0 to 7). When recovery cycle insertion is enabled and a value other than 0000b is set, 1 to 15 recovery cycles are inserted when:

- After a read access to the external bus, a read access is made to the external bus in the same area

15.3.2 CSn恢复周期寄存器(CSnREC)(n=0到7)

Address(es): BUS.CS0REC 4000 380Ah, BUS.CS1REC 4000 381Ah, BUS.CS2REC 4000 382Ah, BUS.CS3REC 4000 383Ah, BUS.CS4REC 4000 384Ah, BUS.CS5REC 4000 385Ah, BUS.CS6REC 4000 386Ah, BUS.CS7REC 4000 387Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	WRCV[3:0]				—	—	—	—	RRCV[3:0]			
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b3 to b0	RRCV[3:0]	读取恢复	b3b00000：不插入任何恢复周期0001：插入1个恢复周期0010：插入2个恢复周期0011：插入3个恢复周期0100：插入4个恢复周期0101：插入5个恢复周期0110：插入6个恢复周期0111：插入7个恢复周期1000：插入8个恢复周期1001：插入9个恢复周期1010：插入10个恢复周期1011：插入11个恢复周期1100：插入12个恢复周期1101：插入13个恢复周期1110：插入14个恢复周期1111：插入15个恢复周期。	R/W
b7 to b4	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b11 to b8	WRCV[3:0]	写恢复	b11b80000：不插入任何恢复周期0001：插入1个恢复周期0010：插入2个恢复周期0011：插入3个恢复周期0100：插入4个恢复周期0101：插入5个恢复周期0110：插入6个恢复周期0111：插入7个恢复周期1000：插入8个恢复周期1001：插入9个恢复周期1010：插入10个恢复周期1011：插入11个恢复周期1100：插入12个恢复周期1101：插入13个恢复周期1110：插入14个恢复周期1111：插入15个恢复周期。	R/W
b15 to b12	—	Reserved	这些位被读取为0。写入值应为0。	R/W

在访问外部总线时不要尝试写入CSnREC寄存器。

当前面的总线访问来自单独的总线时，CSnREC在CSRECEN的单独总线恢复周期插入使能位(RCVENi(i=0to7))中使能恢复周期插入时有效。当前面的总线访问是地址数据多路复用总线访问时，CSnREC在通过CSRECEN中的多路复用总线恢复周期插入使能位(RCVENMj(j=0至7))使能恢复周期插入时有效。有关详细信息，请参阅第15.5.4节，恢复周期的插入。

RRCV[3:0]位（读取恢复）

RRCV[3:0]位指定在CSn（n=0到7）的外部总线上进行读访问后插入的恢复周期数。当启用恢复周期插入并设置0000b以外的值时，在以下情况下插入1到15个恢复周期：

- 对外部总线进行读访问后，对同一区域的外部总线进行读访问

- After a read access to the external bus, a read access is made to the external bus in a different area
- After a read access to the external bus, a write access is made to the external bus in the same area
- After a read access to the external bus, a write access is made to the external bus in a different area.

WRCV[3:0] bits (Write Recovery)

The WRCV[3:0] bits specify the number of recovery cycles inserted after a write access on the external bus for CSn (n = 0 to 7). When recovery cycle insertion is enabled and a value other than 0000b is set, 1 to 15 recovery cycles are inserted when:

- After a write access to the external bus, a read access is made to the external bus in the same area
- After a write access to the external bus, a read access is made to the external bus in a different area
- After a write access to the external bus, a write access is made to the external bus in the same area
- After a write access to the external bus, a write access is made to the external bus in a different area.

15.3.3 CS Recovery Cycle Insertion Enable Register (CSRECEN)

Address(es): BUS.CSRECEN 4000 3880h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RCVENM7	RCVENM6	RCVENM5	RCVENM4	RCVENM3	RCVENM2	RCVENM1	RCVENM0	RCVEN7	RCVEN6	RCVEN5	RCVEN4	RCVEN3	RCVEN2	RCVEN1	RCVEN0
Value after reset:	0	0	1	1	1	1	1	0	0	0	1	1	1	1	1	0

Bit	Symbol	Bit name	Description	R/W
b0	RCVEN0	Separate Bus Recovery Cycle Insertion Enable 0	0: Disable 1: Enable.	R/W
b1	RCVEN1	Separate Bus Recovery Cycle Insertion Enable 1	0: Disable 1: Enable.	R/W
b2	RCVEN2	Separate Bus Recovery Cycle Insertion Enable 2	0: Disable 1: Enable.	R/W
b3	RCVEN3	Separate Bus Recovery Cycle Insertion Enable 3	0: Disable 1: Enable.	R/W
b4	RCVEN4	Separate Bus Recovery Cycle Insertion Enable 4	0: Disable 1: Enable.	R/W
b5	RCVEN5	Separate Bus Recovery Cycle Insertion Enable 5	0: Disable 1: Enable.	R/W
b6	RCVEN6	Separate Bus Recovery Cycle Insertion Enable 6	0: Disable 1: Enable.	R/W
b7	RCVEN7	Separate Bus Recovery Cycle Insertion Enable 7	0: Disable 1: Enable.	R/W
b8	RCVENM0	Multiplexed Bus Recovery Cycle Insertion Enable 0	0: Disable 1: Enable.	R/W
b9	RCVENM1	Multiplexed Bus Recovery Cycle Insertion Enable 1	0: Disable 1: Enable.	R/W
b10	RCVENM2	Multiplexed Bus Recovery Cycle Insertion Enable 2	0: Disable 1: Enable.	R/W
b11	RCVENM3	Multiplexed Bus Recovery Cycle Insertion Enable 3	0: Disable 1: Enable.	R/W
b12	RCVENM4	Multiplexed Bus Recovery Cycle Insertion Enable 4	0: Disable 1: Enable.	R/W
b13	RCVENM5	Multiplexed Bus Recovery Cycle Insertion Enable 5	0: Disable 1: Enable.	R/W

- 对外部总线进行读访问后，对不同区域的外部总线进行读访问
- 对外部总线进行读访问后，对同一区域的外部总线进行写访问
- 在对外部总线进行读访问之后，对不同区域中的外部总线进行写访问。

WRCV[3:0]位（写恢复）

WRCV[3:0]位指定在对CSn（n=0到7）的外部总线进行写访问后插入的恢复周期数。当启用恢复周期插入并设置0000b以外的值时，在以下情况下插入1到15个恢复周期：

- 对外部总线进行写访问后，对同一区域的外部总线进行读访问
- 对外部总线进行写访问后，对不同区域的外部总线进行读访问
- 对外部总线进行写访问后，对同一区域的外部总线进行写访问
- 在对外部总线进行写访问之后，对不同区域中的外部总线进行写访问。

15.3.3 CS恢复周期插入使能寄存器(CSRECEN)

Address(es): BUS.CSRECEN 4000 3880h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RCVENM7	RCVENM6	RCVENM5	RCVENM4	RCVENM3	RCVENM2	RCVENM1	RCVENM0	RCVEN7	RCVEN6	RCVEN5	RCVEN4	RCVEN3	RCVEN2	RCVEN1	RCVEN0
重置后的值：	0	0	1	1	1	1	1	0	0	0	1	1	1	1	1	0

Bit	Symbol	位名称	Description	R/W
b0	RCVEN0	单独的总线恢复周期插入 Enable 0	0：禁用1 ：启用。	R/W
b1	RCVEN1	单独的总线恢复周期插入 Enable 1	0：禁用1 ：启用。	R/W
b2	RCVEN2	单独的总线恢复周期插入 Enable 2	0：禁用1 ：启用。	R/W
b3	RCVEN3	单独的总线恢复周期插入 Enable 3	0：禁用1 ：启用。	R/W
b4	RCVEN4	单独的总线恢复周期插入 Enable 4	0：禁用1 ：启用。	R/W
b5	RCVEN5	单独的总线恢复周期插入 Enable 5	0：禁用1 ：启用。	R/W
b6	RCVEN6	单独的总线恢复周期插入 Enable 6	0：禁用1 ：启用。	R/W
b7	RCVEN7	单独的总线恢复周期插入 Enable 7	0：禁用1 ：启用。	R/W
b8	RCVENM0	多路复用总线恢复周期插入 Enable 0	0：禁用1 ：启用。	R/W
b9	RCVENM1	多路复用总线恢复周期插入 Enable 1	0：禁用1 ：启用。	R/W
b10	RCVENM2	多路复用总线恢复周期插入 Enable 2	0：禁用1 ：启用。	R/W
b11	RCVENM3	多路复用总线恢复周期插入 Enable 3	0：禁用1 ：启用。	R/W
b12	RCVENM4	多路复用总线恢复周期插入 Enable 4	0：禁用1 ：启用。	R/W
b13	RCVENM5	多路复用总线恢复周期插入 Enable 5	0：禁用1 ：启用。	R/W

Bit	Symbol	Bit name	Description	R/W
b14	RCVENM6	Multiplexed Bus Recovery Cycle Insertion Enable 6	0: Disable 1: Enable.	R/W
b15	RCVENM7	Multiplexed Bus Recovery Cycle Insertion Enable 7	0: Disable 1: Enable.	R/W

Do not attempt to write to the CSRECEN register while the external bus is being accessed. For more information on insertion recovery cycles, see 15.5.4 Insertion of Recovery Cycles.

RCVENi bit (Separate Bus Recovery Cycle Insertion Enable i) (i = 0 to 7)

This bit enables the insertion of read or write recovery cycles when, after a read or write access on the external bus, a read or write access is made on the external bus to the same or different area.

RCVENMj bit (Multiplexed Bus Recovery Cycle Insertion Enable j) (j = 0 to 7)

This bit enables the insertion of read or write recovery cycles when, after a read or write access on the external bus, a read or write access is made on the external bus to the same or different area.

Table 15.5 Insertion of recovery cycles

Access type	External address space	Insertion of recovery cycles	Corresponding bits (Separate/Multiplexed)
Read access after read access	Same area	Recovery cycles specified in the RRCV[3:0] bits are inserted for the priority access area	RCVEN0/RCVENM0
	Different area	Recovery cycles specified in the RRCV[3:0] bits are inserted for the priority access area	RCVEN1/RCVENM1
Write access after read access	Same area	Recovery cycles specified in the RRCV[3:0] bits are inserted for the priority access area	RCVEN2/RCVENM2
	Different area	Recovery cycles specified in the RRCV[3:0] bits are inserted for the priority access area	RCVEN3/RCVENM3
Read access after write access	Same area	Recovery cycles specified in the WRCV[3:0] bits are inserted for the priority access area	RCVEN4/RCVENM4
	Different area	Recovery cycles specified in the WRCV[3:0] bits are inserted for the priority access area	RCVEN5/RCVENM5
Write access after write access	Same area	Recovery cycles specified in the WRCV[3:0] bits are inserted for the priority access area	RCVEN6/RCVENM6
	Different area	Recovery cycles specified in the WRCV[3:0] bits are inserted for the priority access area	RCVEN7/RCVENM7

Bit	Symbol	位名称	Description	R/W
b14	RCVENM6	多路复用总线恢复周期插入 Enable 6	0：禁用1 ：启用。	R/W
b15	RCVENM7	多路复用总线恢复周期插入 Enable 7	0：禁用1 ：启用。	R/W

在访问外部总线时不要尝试写入CSRECEN寄存器。有关插入恢复周期的更多信息，请参阅15.5.4插入恢复周期。

RCVENi位（单独的总线恢复周期插入使能i）（i=0到7）

当在外部总线上进行读或写访问后，在外部总线上对相同或不同区域进行读或写访问时，该位允许插入读或写恢复周期。

RCVENMj位（多路复用总线恢复周期插入使能j）（j=0至7）

当在外部总线上进行读或写访问后，在外部总线上对相同或不同区域进行读或写访问时，该位允许插入读或写恢复周期。

Table 15.5 插入恢复周期

访问类型	外部地址空间	插入恢复周期	对应位（分离复用）
读访问后读访问	同一地区	中指定的恢复周期 RRCV[3:0]位被插入优先访问区域	RCVEN0/RCVENM0
	不同区域	中指定的恢复周期 RRCV[3:0]位被插入优先访问区域	RCVEN1/RCVENM1
读访问后写访问	同一地区	中指定的恢复周期 RRCV[3:0]位被插入优先访问区域	RCVEN2/RCVENM2
	不同区域	中指定的恢复周期 RRCV[3:0]位被插入优先访问区域	RCVEN3/RCVENM3
写访问后读访问	同一地区	中指定的恢复周期 为优先访问区域插入WRCV[3:0]位	RCVEN4/RCVENM4
	不同区域	中指定的恢复周期 为优先访问区域插入WRCV[3:0]位	RCVEN5/RCVENM5
写访问后的写访问	同一地区	中指定的恢复周期 为优先访问区域插入WRCV[3:0]位	RCVEN6/RCVENM6
	不同区域	中指定的恢复周期 为优先访问区域插入WRCV[3:0]位	RCVEN7/RCVENM7

15.3.4 CSn Mode Register (CSnMOD) (n = 0 to 7)

Address(es): BUS.CS0MOD 4000 3002h, BUS.CS1MOD 4000 3012h, BUS.CS2MOD 4000 3022h, BUS.CS3MOD 4000 3032h, BUS.CS4MOD 4000 3042h, BUS.CS5MOD 4000 3052h, BUS.CS6MOD 4000 3062h, BUS.CS7MOD 4000 3072h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PRMOD	—	—	—	—	—	PWENB	PRENB	—	—	—	—	EWENB	—	—	WRMOD
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	WRMOD	Write Access Mode Select	0: Byte strobe mode 1: Single-write strobe mode.	R/W
b2, b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b3	EWENB	External Wait Enable	0: Disable 1: Enable.	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	PRENB	Page Read Access Enable	0: Disable 1: Enable.	R/W
b9	PWENB	Page Write Access Enable	0: Disable 1: Enable.	R/W
b14 to b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15	PRMOD	Page Read Access Mode Select	0: Normal access compatible mode 1: External data read continuous assertion mode.	R/W

Do not write to the CSnMOD register while access to the CSn area is in progress.

WRMOD bit (Write Access Mode Select)

The WRMOD bit selects the write access operating mode. Writing 0 selects byte strobe mode, in which data writes are controlled by the WRn signals (n = 0 to 1) associated with the respective byte positions. Writing 1 selects single-write strobe mode, in which data writes are controlled by the BCn (n = 0 to 1) and WR signals associated with the respective byte positions.

Note: Setting the external bus width to 8 bits is prohibited in single-write strobe mode.

Table 15.6 Control signals for write access modes

	Pin name			
Write access mode	WR1	WR0/WR	BC1	BC0
Byte strobe mode	✓	✓ (WR0)	×	×
Single-write strobe mode	×	✓ (WR)	✓	✓

✓: Enabled, ×: Disabled

EWENB bit (External Wait Enable)

The EWENB bit enables external waits. Writing 0 disables the WAIT signal. Writing 1 selects external wait and allows the WAIT signal to control the number of waits per cycle. In this state, wait cycles are inserted when the WAIT signal is low.

PRENB bit (Page Read Access Enable)

The PRENB bit enables page read accesses.

Note: When the address/data multiplexed I/O interface is selected with the CSnCR.MPXEN bit, PRENB should not be set to enable page read accesses. Page read accesses are not supported in the address/data multiplexed I/O interface.

15.3.4 CSn模式寄存器(CSnMOD)(n=0到7)

Address(es): BUS.CS0MOD 4000 3002h, BUS.CS1MOD 4000 3012h, BUS.CS2MOD 4000 3022h, BUS.CS3MOD 4000 3032h, BUS.CS4MOD 4000 3042h, BUS.CS5MOD 4000 3052h, BUS.CS6MOD 4000 3062h, BUS.CS7MOD 4000 3072h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PRMOD	—	—	—	—	—	PWENB	PRENB	—	—	—	—	EWENB	—	—	WRMOD
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	WRMOD	写访问模式选择	0：字节选通模式1：单写选通模式。	R/W
b2, b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b3	EWENB	外部等待启用	0：禁用1：启用。	R/W
b7 to b4	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b8	PRENB	页面读取访问启用	0：禁用1：启用。	R/W
b9	PWENB	页面写访问启用	0：禁用1：启用。	R/W
b14 to b10	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b15	PRMOD	页面读取访问模式选择	0：正常访问兼容模式1：外部数据读取连续断言模式。	R/W

在访问CSn区域的过程中不要写入CSnMOD寄存器。

WRMOD位（写访问模式选择）

WRMOD位选择写访问操作模式。写入0选择字节选通模式，其中数据写入由与相应字节位置相关的WRn信号（n=0到1）控制。写1选择单写选通模式，其中数据写入由与各个字节位置相关的BCn（n=0到1）和WR信号控制。

Note: 在单写选通模式下，禁止将外部总线宽度设置为8位。

Table 15.6 写访问模式的控制信号

	引脚名称			
写访问模式	WR1	WR0/WR	BC1	BC0
字节选通模式	✓	✓ (WR0)	×	×
单写频闪模式	×	✓ (WR)	✓	✓

：启用，×：禁用

EWENB位（外部等待使能）

EWENB位使能外部等待。写入0禁用WAIT信号。写1选择外部等待并允许WAIT信号控制每个周期的等待数。在这种状态下，当WAIT信号为低时插入等待周期。

PRENB位（页面读取访问使能）

PRENB位使能页面读取访问。

Note: 当使用CSnCR.MPXEN位选择地址数据复用IO接口时，不应设置PRENB以启用页面读取访问。地址数据复用IO接口不支持页面读取访问。

PWENB bit (Page Write Access Enable)

The PWENB bit enables page write accesses.

Note: When the address/data multiplexed I/O interface is selected with the CSnCR.MPXEN bit, PWENB should not be set to enable page write accesses. Page write accesses are not supported in the address/data multiplexed I/O interface.

PRMOD bit (Page Read Access Mode Select)

The PRMOD bit selects the operating mode for page read accesses. Writing 0 selects normal access compatible mode, in which the RD signal is negated and an RD assert wait is inserted each time a unit of data is read. When there is no RD assert wait, the RD signal is negated only in the final transfer of the external bus access.

Writing 1 selects external data read continuous assertion mode, in which an RD assert wait is inserted and the RD signal is continuously asserted during the wait.

15.3.5 CSn Wait Control Register 1 (CSnWCR1) (n = 0 to 7)

Address(es): BUS.CS0WCR1 4000 3004h, BUS.CS1WCR1 4000 3014h, BUS.CS2WCR1 4000 3024h, BUS.CS3WCR1 4000 3034h, BUS.CS4WCR1 4000 3044h, BUS.CS5WCR1 4000 3054h, BUS.CS6WCR1 4000 3064h, BUS.CS7WCR1 4000 3074h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	CSRWAIT[4:0]					—	—	—	CSWWAIT[4:0]				
Value after reset:	0	0	0	0	0	1	1	1	0	0	0	0	0	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	CSPRWAIT[2:0]			—	—	—	—	—	CSPWWAIT[2:0]		
Value after reset:	0	0	0	0	0	1	1	1	0	0	0	0	0	1	1	1

Bit	Symbol	Bit name	Description	R/W
b2 to b0	CSPWWAIT[2:0]	Page Write Cycle Wait Select*1	b2 b0 0 0 0: Do not insert wait 0 0 1: Insert wait of 1 clock cycle 0 1 0: Insert wait of 2 clock cycles 0 1 1: Insert wait of 3 clock cycles 1 0 0: Insert wait of 4 clock cycles 1 0 1: Insert wait of 5 clock cycles 1 1 0: Insert wait of 6 clock cycles 1 1 1: Insert wait of 7 clock cycles.	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b10 to b8	CSPRWAIT[2:0]	Page Read Cycle Wait Select*2	b10 b8 0 0 0: Do not insert wait 0 0 1: Insert wait of 1 clock cycle 0 1 0: Insert wait of 2 clock cycles 0 1 1: Insert wait of 3 clock cycles 1 0 0: Insert wait of 4 clock cycles 1 0 1: Insert wait of 5 clock cycles 1 1 0: Insert wait of 6 clock cycles 1 1 1: Insert wait of 7 clock cycles.	R/W
b15 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

PWENB位（页写访问使能）

PWENB位使能页写访问。

Note: 当使用CSnCR.MPXEN位选择地址数据复用IO接口时，不应设置PWENB以启用页面写访问。地址数据复用IO接口不支持页写访问。

PRMOD位（页面读取访问模式选择）

PRMOD位选择页面读取访问的操作模式。写入0选择正常访问兼容模式，其中RD信号被否定，并且每次读取一个数据单元时插入一个RD断言等待。当没有RD断言等待时，RD信号仅在外部总线访问的最终传输中被否定。

写1选择外部数据读取连续断言模式，在该模式下插入一个RD断言等待，并且在等待期间RD信号连续断言。

15.3.5 CSn等待控制寄存器1(CSnWCR1)(n=0to7)

Address(es): BUS.CS0WCR1 4000 3004h, BUS.CS1WCR1 4000 3014h, BUS.CS2WCR1 4000 3024h, BUS.CS3WCR1 4000 3034h, BUS.CS4WCR1 4000 3044h, BUS.CS5WCR1 4000 3054h, BUS.CS6WCR1 4000 3064h, BUS.CS7WCR1 4000 3074h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	CSRWAIT[4:0]					—	—	—	CSWWAIT[4:0]				
重置后的值:	0	0	0	0	0	1	1	1	0	0	0	0	0	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	CSPRWAIT[2:0]			—	—	—	—	—	CSPWWAIT[2:0]		
重置后的值:	0	0	0	0	0	1	1	1	0	0	0	0	0	1	1	1

Bit	Symbol	位名称	Description	R/W
b2 to b0	CSPWWAIT[2:0]	页写周期等待选择*1	b2b0000：不插入等待001：插入等待1个时钟周期010：插入等待2个时钟周期011：插入等待3个时钟周期100：插入等待4个时钟周期101：插入等待5个时钟周期110：插入等待6个时钟周期111：插入等待7个时钟周期。	R/W
b7 to b3	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b10 to b8	CSPRWAIT[2:0]	页面读取周期等待选择*2	b10b8000：不插入等待001：插入等待1个时钟周期010：插入等待2个时钟周期011：插入等待3个时钟周期100：插入等待4个时钟周期101：插入等待5个时钟周期110：插入等待6个时钟周期111：插入等待7个时钟周期。	R/W
b15 to b11	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Bit	Symbol	Bit name	Description	R/W
b20 to b16	CSWWAIT[4:0]	Normal Write Cycle Wait Select	b20 b16 0 0 0 0 0: Do not insert wait 0 0 0 0 1: Insert wait of 1 clock cycle 0 0 0 1 0: Insert wait of 2 clock cycles 0 0 0 1 1: Insert wait of 3 clock cycles ... 1 1 1 0 1: Insert wait of 29 clock cycles 1 1 1 1 0: Insert wait of 30 clock cycles 1 1 1 1 1: Insert wait of 31 clock cycles.	R/W
b23 to b21	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b28 to b24	CSRWAIT[4:0]	Normal Read Cycle Wait Select	b28 b24 0 0 0 0 0: Do not insert wait 0 0 0 0 1: Insert wait of 1 clock cycle 0 0 0 1 0: Insert wait of 2 clock cycles 0 0 0 1 1: Insert wait of 3 clock cycles. ... 1 1 1 0 1: Insert wait of 29 clock cycles 1 1 1 1 0: Insert wait of 30 clock cycles 1 1 1 1 1: Insert wait of 31 clock cycles.	R/W
b31 to b29	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. The CSPWWAIT[2:0] value is only valid when the CSnMOD.PWENB bit is set to 1.
Note 2. The CSPRWAIT[2:0] value is only valid when the CSnMOD.PRENB bit is set to 1.

Do not attempt to write to the CSnWCR1 register while the external bus is being accessed. Set each of these bits within a range of the restrictions described in section 15.5.7, Constraints, (1) Constraints on using a separate bus interface or section 15.5.7, Constraints, (2) Constraints on using address/data multiplexed bus interface, according to the bus interface used.

CSPWWAIT[2:0] bits (Page Write Cycle Wait Select)

The CSPWWAIT[2:0] bits specify the number of wait cycles to be inserted into the second and subsequent accesses during a page write cycle. The setting is enabled when the CSnMOD.PWENB bit is set to 1.

Note: The settings must satisfy 1 ≤ CSnWCR2.WDON[2:0] value ≤ CSnWCR2.WRON[2:0] value ≤ CSnWCR1.CSPWWAIT[2:0] value, and CSnWCR2.CSON[2:0] value ≤ CSnWCR2.WRON[2:0] value ≤ CSnWCR1.CSPWWAIT[2:0] value.

CSPRWAIT[2:0] bits (Page Read Cycle Wait Select)

The CSPRWAIT[2:0] bits specify the number of wait cycles to be inserted into the second and subsequent accesses during a page read cycle. The setting is enabled when the CSnMOD.PRENB bit is set to 1.

Note: The settings must satisfy CSnWCR2.CSON[2:0] value ≤ CSnWCR2.RDON[2:0] value ≤ CSnWCR1.CSPRWAIT[2:0] value.

CSWWAIT[4:0] bits (Normal Write Cycle Wait Select)

The CSWWAIT[4:0] bits specify the number of wait cycles to be inserted into the first access during a normal write cycle or page write cycle.

Note: The settings must satisfy 1 ≤ CSnWCR2.WDON[2:0] value ≤ CSnWCR2.WRON[2:0] value ≤ CSnWCR1.CSWWAIT[4:0] value, and CSnWCR2.CSON[2:0] value ≤ CSnWCR2.WRON[2:0] value ≤ CSnWCR1.CSWWAIT[4:0] value.

CSRWAIT[4:0] bits (Normal Read Cycle Wait Select)

The CSRWAIT[4:0] bits specify the number of wait cycles to be inserted into the first access during a normal read cycle or page read cycle.

Bit	Symbol	位名称	Description	R/W
b20 to b16	CSWWAIT[4:0]	正常写周期等待选择	b20b1600000：不插入等待00001：插入等待1个时钟周期00010：插入等待2个时钟周期00011：插入等待3个时钟周期 ... 11101：插入等待29个时钟周期11110：插入等待30个时钟周期11111：插入等待31个时钟周期。	R/W
b23 to b21	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b28 to b24	CSRWAIT[4:0]	正常读周期等待选择	b28b2400000：不插入等待00001：插入等待1个时钟周期00010：插入等待2个时钟周期00011：插入等待3个时钟周期。 ... 11101：插入等待29个时钟周期11110：插入等待30个时钟周期11111：插入等待31个时钟周期。	R/W
b31 to b29	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. CSPWWAIT[2:0]值仅在CSnMOD.PWENB位设置为1时有效。
Note 2. CSPRWAIT[2:0]值仅在CSnMOD.PRENB位设置为1时有效。

在访问外部总线时不要尝试写入CSnWCR1寄存器。将这些位中的每一个设置在第15.5.7节，约束，(1)使用单独总线接口或第15.5.7节，约束，(2)使用地址数据复用总线接口的约束中描述的限制范围内，根据使用的总线接口。

CSWWAIT[2:0]位（页写周期等待选择）

CSPWWAIT[2:0]位指定在页写周期期间插入第二次和后续访问的等待周期数。当CSnMOD.PWENB位设置为1时启用该设置。

Note: 设置必须满足1≤CSnWCR2.WDON[2:0]value≤CSnWCR2.WRON[2:0]value≤CSnWCR1.CSPWWAIT[2:0]值，CSnWCR2.CSON[2:0]值≤CSnWCR2.WRON[2:0]值≤CSnWCR1.CSPWWAIT[2:0] value.

CSPRWAIT[2:0]位（页面读取周期等待选择）

CSPRWAIT[2:0]位指定在页读取周期期间插入第二次和后续访问的等待周期数。当CSnMOD.PRENB位设置为1时启用该设置。

Note: 设置必须满足CSnWCR2.CSON[2:0]value≤CSnWCR2.RDON[2:0]value≤CSnWCR1.CSPRWAIT[2:0] value.

CSWWAIT[4:0]位（正常写周期等待选择）

CSWWAIT[4:0]位指定在正常写周期或页写周期期间插入第一次访问的等待周期数。

Note: 设置必须满足1≤CSnWCR2.WDON[2:0]value≤CSnWCR2.WRON[2:0]value≤CSnWCR1.CSWWAIT[4:0]值，CSnWCR2.CSON[2:0]值≤CSnWCR2.WRON[2:0]值≤CSnWCR1.CSWWAIT[4:0] value.

CSRWAIT[4:0]位（正常读取周期等待选择）

CSRWAIT[4:0]位指定在正常读取周期或页面读取周期期间插入第一次访问的等待周期数。

Note: The settings must satisfy CSnWCR2.CSON[2:0] value ≤ CSnWCR2.RDON[2:0] value ≤ CSnWCR1.CSRWAIT[4:0] value.

15.3.6 CSn Wait Control Register 2 (CSnWCR2) (n = 0 to 7)

Address(es): BUS.CS0WCR2 4000 3008h, BUS.CS1WCR2 4000 3018h, BUS.CS2WCR2 4000 3028h, BUS.CS3WCR2 4000 3038h, BUS.CS4WCR2 4000 3048h, BUS.CS5WCR2 4000 3058h, BUS.CS6WCR2 4000 3068h, BUS.CS7WCR2 4000 3078h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	CSON[2:0]			—	WDON[2:0]			—	WRON[2:0]			—	RDON[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	AWAIT[1:0]		—	WDOFF[2:0]			—	CSWOFF[2:0]			—	CSROFF[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bit	Symbol	Bit name	Description	R/W
b2 to b0	CSROFF[2:0]	Read-Access CS Extension Cycle Select	b2 b0 0 0 0: Do not insert wait 0 0 1: Insert wait of 1 clock cycle 0 1 0: Insert wait of 2 clock cycles 0 1 1: Insert wait of 3 clock cycles 1 0 0: Insert wait of 4 clock cycles 1 0 1: Insert wait of 5 clock cycles 1 1 0: Insert wait of 6 clock cycles 1 1 1: Insert wait of 7 clock cycles.	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6 to b4	CSWOFF[2:0]	Write-Access CS Extension Cycle Select	b6 b4 0 0 0: Do not insert wait 0 0 1: Insert wait of 1 clock cycle 0 1 0: Insert wait of 2 clock cycles 0 1 1: Insert wait of 3 clock cycles 1 0 0: Insert wait of 4 clock cycles 1 0 1: Insert wait of 5 clock cycles 1 1 0: Insert wait of 6 clock cycles 1 1 1: Insert wait of 7 clock cycles.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b10 to b8	WDOFF[2:0]	Write Data Output Extension Cycle Select	b10 b8 0 0 0: Do not insert wait 0 0 1: Insert wait of 1 clock cycle 0 1 0: Insert wait of 2 clock cycles 0 1 1: Insert wait of 3 clock cycles 1 0 0: Insert wait of 4 clock cycles 1 0 1: Insert wait of 5 clock cycles 1 1 0: Insert wait of 6 clock cycles 1 1 1: Insert wait of 7 clock cycles.	R/W
b11	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b13, b12	AWAIT[1:0]	Address Cycle Wait Select	b13 b12 0 0: Do not insert wait 0 1: Insert wait of 1 clock cycle 1 0: Insert wait of 2 clock cycles 1 1: Insert wait of 3 clock cycles.	R/W
b15, b14	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: 设置必须满足CSnWCR2.CSON[2:0]value≤CSnWCR2.RDON[2:0]value≤CSnWCR1.CSRWAIT[4:0] value.

15.3.6 CSn等待控制寄存器2(CSnWCR2)(n=0to7)

Address(es): BUS.CS0WCR2 4000 3008h, BUS.CS1WCR2 4000 3018h, BUS.CS2WCR2 4000 3028h, BUS.CS3WCR2 4000 3038h, BUS.CS4WCR2 4000 3048h, BUS.CS5WCR2 4000 3058h, BUS.CS6WCR2 4000 3068h, BUS.CS7WCR2 4000 3078h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	CSON[2:0]			—	WDON[2:0]			—	WRON[2:0]			—	RDON[2:0]		
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	AWAIT[1:0]		—	WDOFF[2:0]			—	CSWOFF[2:0]			—	CSROFF[2:0]		
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bit	Symbol	位名称	Description	R/W
b2 to b0	CSROFF[2:0]	读访问CS扩展周期 Select	b2b0000：不插入等待001：插入等待1个时钟周期010：插入等待2个时钟周期011：插入等待3个时钟周期100：插入等待4个时钟周期101：插入等待5个时钟周期110：插入等待6个时钟周期111：插入等待7个时钟周期。	R/W
b3	—	Reserved	该位读取为0。写入值应为0。	R/W
b6 to b4	CSWOFF[2:0]	写访问CS扩展周期 Select	b6b4000：不插入等待001：插入1个时钟周期的等待010：插入2个时钟周期的等待011：插入3个时钟周期的等待100：插入4个时钟周期的等待101：插入等待5个时钟周期110：插入等待6个时钟周期111：插入等待7个时钟周期。	R/W
b7	—	Reserved	该位读取为0。写入值应为0。	R/W
b10 to b8	WDOFF[2:0]	写数据输出扩展周期 Select	b10b8000：不插入等待001：插入等待1个时钟周期010：插入等待2个时钟周期011：插入等待3个时钟周期100：插入等待4个时钟周期101：插入等待5个时钟周期110：插入等待6个时钟周期111：插入等待7个时钟周期。	R/W
b11	—	Reserved	该位读取为0。写入值应为0。	R/W
b13, b12	AWAIT[1:0]	地址周期等待选择	b13b1200：不插入等待01：插入1个时钟周期的等待10：插入2个时钟周期的等待11：插入3个时钟周期的等待。	R/W
b15, b14	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Bit	Symbol	Bit name	Description	R/W
b18 to b16	RDON[2:0]	RD Assert Wait Select	b18 b16 0 0 0: Do not insert wait 0 0 1: Insert wait of 1 clock cycle 0 1 0: Insert wait of 2 clock cycles 0 1 1: Insert wait of 3 clock cycles 1 0 0: Insert wait of 4 clock cycles 1 0 1: Insert wait of 5 clock cycles 1 1 0: Insert wait of 6 clock cycles 1 1 1: Insert wait of 7 clock cycles.	R/W
b19	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b22 to b20	WRON[2:0]	WR Assert Wait Select	b22 b20 0 0 0: Do not insert wait 0 0 1: Insert wait of 1 clock cycle 0 1 0: Insert wait of 2 clock cycles 0 1 1: Insert wait of 3 clock cycles 1 0 0: Insert wait of 4 clock cycles 1 0 1: Insert wait of 5 clock cycles 1 1 0: Insert wait of 6 clock cycles 1 1 1: Insert wait of 7 clock cycles.	R/W
b23	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b26 to b24	WDON[2:0]	Write Data Output Wait Select	b26 b24 0 0 0: Do not insert wait 0 0 1: Insert wait of 1 clock cycle 0 1 0: Insert wait of 2 clock cycles 0 1 1: Insert wait of 3 clock cycles 1 0 0: Insert wait of 4 clock cycles 1 0 1: Insert wait of 5 clock cycles 1 1 0: Insert wait of 6 clock cycles 1 1 1: Insert wait of 7 clock cycles.	R/W
b27	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b30 to b28	CSON[2:0]	CS Assert Wait Select	b30 b28 0 0 0: Do not insert wait 0 0 1: Insert wait of 1 clock cycle 0 1 0: Insert wait of 2 clock cycles 0 1 1: Insert wait of 3 clock cycles 1 0 0: Insert wait of 4 clock cycles 1 0 1: Insert wait of 5 clock cycles 1 1 0: Insert wait of 6 clock cycles 1 1 1: Insert wait of 7 clock cycles.	R/W
b31	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Do not attempt to write to the CSnWCR2 register while the external bus is being accessed. Set each of these bits within a range of the restrictions described in section 15.5.7, Constraints, (1) Constraints on using a separate bus interface. or section 15.5.7, Constraints, (2) Constraints on using address/data multiplexed bus interface, according to the bus interface used.

CSROFF[2:0] bits (Read-Access CS Extension Cycle Select)

The CSROFF[2:0] bits specify the number of wait cycles to be inserted during the period from the end of a wait cycle (RD signal negated) until the CSn signal (n = 0 to 7) is negated in read access mode.

CSWOFF[2:0] bits (Write-Access CS Extension Cycle Select)

The CSWOFF[2:0] bits specify the number of wait cycles to be inserted during the period from the end of a wait cycle (WRn signal (n = 0, 1) negated) until the CSn signal (n = 0 to 7) is negated in write access mode.

Note: The settings must satisfy CSnWCR2.WDOFF[2:0] value ≤ CSnWCR2.CSWOFF[2:0] value.

WDOFF[2:0] bits (Write Data Output Extension Cycle Select)

The WDOFF[2:0] bits specify the number of wait cycles to be inserted during the period from the end of a wait cycle (WRn signal (n = 0, 1) negated) until the write-data output is complete in write access mode.

Note: The settings must satisfy CSnWCR2.WDOFF[2:0] value ≤ CSnWCR2.CSWOFF[2:0] value.

Bit	Symbol	位名称	Description	R/W
b18 to b16	RDON[2:0]	RD断言等待选择	b18b16000：不插入等待001：插入等待1个时钟周期010：插入等待2个时钟周期011：插入等待3个时钟周期100：插入等待4个时钟周期101：插入等待5个时钟周期110：插入等待6个时钟周期111：插入等待7个时钟周期。	R/W
b19	—	Reserved	该位读取为0。写入值应为0。	R/W
b22 to b20	WRON[2:0]	WR断言等待选择	b22b20000：不插入等待001：插入1个时钟周期的等待010：插入2个时钟周期的等待011：插入3个时钟周期的等待100：插入4个时钟周期的等待101：插入等待5个时钟周期110：插入等待6个时钟周期111：插入等待7个时钟周期。	R/W
b23	—	Reserved	该位读取为0。写入值应为0。	R/W
b26 to b24	WDON[2:0]	写数据输出等待选择	b26b24000：不插入等待001：插入等待1个时钟周期010：插入等待2个时钟周期011：插入等待3个时钟周期100：插入等待4个时钟周期101：插入等待5个时钟周期110：插入等待6个时钟周期111：插入等待7个时钟周期。	R/W
b27	—	Reserved	该位读取为0。写入值应为0。	R/W
b30 to b28	CSON[2:0]	CS断言等待选择	b30b28000：不插入等待001：插入等待1个时钟周期010：插入等待2个时钟周期011：插入等待3个时钟周期100：插入等待4个时钟周期101：插入等待5个时钟周期110：插入等待6个时钟周期111：插入等待7个时钟周期。	R/W
b31	—	Reserved	该位读取为0。写入值应为0。	R/W

在访问外部总线时不要尝试写入CSnWCR2寄存器。将这些位中的每一个设置在第15.5.7节，约束，(1)使用单独总线接口的约束中描述的限制范围内。或第15.5.7节，约束，(2)使用地址数据复用总线接口的约束，根据所使用的总线接口。

CSROFF[2:0]位（读访问CS扩展周期选择）

CSROFF[2:0]位指定在读访问模式下从等待周期结束（RD信号取反）到CSn信号（n=0到7）取反期间插入的等待周期数。

CSWOFF[2:0]位（写访问CS扩展周期选择）

CSWOFF[2:0]位指定从等待周期结束（WRn信号(n=0 1)取反）到CSn信号（n=0到7）期间插入的等待周期数在写访问模式下被否定。

Note: 设置必须满足CSnWCR2.WDOFF[2:0]值≤CSnWCR2.CSWOFF[2:0]值。

WDOFF[2:0]位（写数据输出扩展周期选择）

WDOFF[2:0]位指定从等待周期结束（WRn信号(n=0 1)取反）到在写访问中完成写数据输出期间要插入的等待周期数模式。

Note: 设置必须满足CSnWCR2.WDOFF[2:0]值≤CSnWCR2.CSWOFF[2:0]值。

AWAIT[1:0] bits (Address Cycle Wait Select)

The AWAIT[1:0] bits specify the number of wait cycles to be inserted into an address output cycle with the address/data multiplexed I/O interface.

Note: CSnWCR2.CSON[2:0] value ≤ CSnWCR2.AWAIT[1:0] value.
For read access, satisfy CSnWCR2.AWAIT[1:0] value + 2 ≤ CSnWCR2.RDON[2:0] value ≤ CSnWCR1.CSRWAIT[4:0] value.
For write access, satisfy CSnWCR2.AWAIT[1:0] value + 2 ≤ CSnWCR2.WRON[2:0] value ≤ CSnWCR1.CSWWAIT[4:0] value and CSnWCR2.AWAIT[1:0] value + 2 ≤ CSnWCR2.WDON[2:0] value ≤ CSnWCR1.CSWWAIT[4:0] value.

RDON[2:0] bits (RD Assert Wait Select)

The RDON[2:0] bits specify the number of wait cycles to be inserted before the RD signal is asserted.

Note: For normal read access, satisfy CSnWCR2.CSON[2:0] value ≤ CSnWCR2.RDON[2:0] value ≤ CSnWCR1.CSRWAIT[4:0] value.
For page read access, satisfy CSnWCR2.CSON[2:0] value ≤ CSnWCR2.RDON[2:0] value ≤ CSnWCR1.CSPRWAIT[2:0] value.
When the address/data multiplexed I/O interface is selected, satisfy CSnWCR2.AWAIT[1:0] value + 2 ≤ CSnWCR2.RDON[2:0] value ≤ CSnWCR1.CSRWAIT[4:0] value.

WRON[2:0] bits (WR Assert Wait Select)

The WRON[2:0] bits specify the number of wait cycles to be inserted before the WRn signal (n = 0, 1) is asserted.

Note: For normal write access, satisfy 1 ≤ CSnWCR2.WDON[2:0] value ≤ CSnWCR2.WRON[2:0] value ≤ CSnWCR1.CSWWAIT[4:0] value, and CSnWCR2.CSON[2:0] value ≤ CSnWCR2.WRON[2:0] value ≤ CSnWCR1.CSWWAIT[4:0] value.
For page write access, satisfy 1 ≤ CSnWCR2.WDON[2:0] value ≤ CSnWCR2.WRON[2:0] value ≤ CSnWCR1.CSPWWAIT[2:0] value, and CSnWCR2.CSON[2:0] value ≤ CSnWCR2.WRON[2:0] value ≤ CSnWCR1.CSPWWAIT[2:0] value.
When the address/data multiplexed I/O interface is selected, satisfy CSnWCR2.AWAIT[1:0] value + 2 ≤ CSnWCR2.WRON[2:0] value ≤ CSnWCR1.CSWWAIT[4:0] value.

WDON[2:0] bits (Write Data Output Wait Select)

The WDON[2:0] bits specify the number of wait cycles to be inserted before the write data is output.

Note: For normal write access, satisfy 1 ≤ CSnWCR2.WDON[2:0] value ≤ CSnWCR2.WRON[2:0] value ≤ CSnWCR1.CSWWAIT[4:0] value.
For page write access, satisfy 1 ≤ CSnWCR2.WDON[2:0] value ≤ CSnWCR2.WRON[2:0] value ≤ CSnWCR1.CSPWWAIT[2:0] value.
When the address/data multiplexed I/O interface is selected, satisfy CSnWCR2.AWAIT[1:0] value + 2 ≤ CSnWCR2.WDON[2:0] value ≤ CSnWCR1.CSWWAIT[4:0] value.

CSON[2:0] bits (CS Assert Wait Select)

The CSON[2:0] bits specify the number of wait cycles to be inserted before the CSn signal (n = 0 to 7) is asserted.

Note: For normal read access, satisfy CSnWCR2.CSON[2:0] value ≤ CSnWCR2.RDON[2:0] value ≤ CSnWCR1.CSRWAIT[4:0] value.
For page read access, satisfy CSnWCR2.CSON[2:0] value ≤ CSnWCR2.RDON[2:0] value ≤ CSnWCR1.CSPRWAIT[2:0] value.
For normal write access, satisfy CSnWCR2.CSON[2:0] value ≤ CSnWCR2.WRON[2:0] value ≤ CSnWCR1.CSWWAIT[4:0] value.
For page write access, satisfy CSnWCR2.CSON[2:0] value ≤ CSnWCR2.WRON[2:0] value ≤ CSnWCR1.CSPWWAIT[2:0] value.
When the address/data multiplexed I/O interface is selected, satisfy CSnWCR2.CSON[2:0] value ≤

AWAIT[1:0]位（地址周期等待选择）

AWAIT[1:0]位指定通过地址数据复用IO接口插入地址输出周期的等待周期数。

Note: CSnWCR2.CSON[2:0] value ≤ CSnWCR2.AWAIT[1:0] value.
对于读访问，满足CSnWCR2.AWAIT[1:0]值+2≤CSnWCR2.RDON[2:0]值≤CSnWCR1.CSRWAIT[4:0]值。
对于写访问，满足CSnWCR2.AWAIT[1:0]value+2≤CSnWCR2.WRON[2:0]value≤CSnWCR1.CSWWAIT[4:0]值和CSnWCR2.AWAIT[1:0]值+2≤CSnWCR2.WDON[2:0]值≤CSnWCR1.CSWWAIT[4:0] value.

RDON[2:0]位（RD断言等待选择）

RDON[2:0]位指定在RD信号置位之前要插入的等待周期数。

Note: 对于正常的读访问，满足CSnWCR2.CSON[2:0]value≤CSnWCR2.RDON[2:0]value≤CSnWCR1.CSRWAIT[4:0] value.
对于页读访问，满足CSnWCR2.CSON[2:0]value≤CSnWCR2.RDON[2:0]value≤CSnWCR1.CSPRWAIT[2:0] value.
选择地址数据复用IO接口时，满足CSnWCR2.AWAIT[1:0]值+2≤CSnWCR2.RDON[2:0] value ≤ CSnWCR1.CSRWAIT[4:0] value.

WRON[2:0]位（WR断言等待选择）

WRON[2:0]位指定在WRn信号(n=0 1)置位之前要插入的等待周期数。

Note: 对于正常写访问，满足1≤CSnWCR2.WDON[2:0]value≤CSnWCR2.WRON[2:0]value≤CSnWCR1.CSWWAIT[4:0]值，CSnWCR2.CSON[2:0]值≤CSnWCR2.WRON[2:0]值≤CSnWCR1.CSWWAIT[4:0] value.
对于页写访问，满足1≤CSnWCR2.WDON[2:0]value≤CSnWCR2.WRON[2:0]value≤CSnWCR1.CSPWWAIT[2:0]值，CSnWCR2.CSON[2:0]值≤CSnWCR2.WRON[2:0]值≤CSnWCR1.CSPWWAIT[2:0]值。
选择地址数据复用IO接口时，满足CSnWCR2.AWAIT[1:0]值+2≤CSnWCR2.WRON[2:0] value ≤ CSnWCR1.CSWWAIT[4:0] value.

WDON[2:0]位（写数据输出等待选择）

WDON[2:0]位指定在输出写数据之前要插入的等待周期数。

Note: 对于正常写访问，满足1≤CSnWCR2.WDON[2:0]value≤CSnWCR2.WRON[2:0]value≤CSnWCR1.CSWWAIT[4:0] value.
对于页写访问，满足1≤CSnWCR2.WDON[2:0]value≤CSnWCR2.WRON[2:0]value≤CSnWCR1.CSPWWAIT[2:0] value.
选择地址数据复用IO接口时，满足CSnWCR2.AWAIT[1:0]值+2≤CSnWCR2.WDON[2:0] value ≤ CSnWCR1.CSWWAIT[4:0] value.

CSON[2:0]位（CS断言等待选择）

CSON[2:0]位指定在CSn信号（n=0到7）置位之前要插入的等待周期数。

Note: 对于正常的读访问，满足CSnWCR2.CSON[2:0]value≤CSnWCR2.RDON[2:0]value≤CSnWCR1.CSRWAIT[4:0] value.
对于页读访问，满足CSnWCR2.CSON[2:0]value≤CSnWCR2.RDON[2:0]value≤CSnWCR1.CSPRWAIT[2:0]值。对于正常的写访问，满足CSnWCR2.CSON[2:0]value≤CSnWCR2.WRON[2:0]value≤CSnWCR1.CSWWAIT[4:0] value.
对于页写访问，满足CSnWCR2.CSON[2:0]value≤CSnWCR2.WRON[2:0]value≤CSnWCR1.CSPWWAIT[2:0] value.
选择地址数据复用IO接口时，满足CSnWCR2.CSON[2:0]值≤

CSnWCR2.AWAIT[1:0] value.

15.3.7 SDC Control Register (SDCCR)

Address(es): BUS.SDCCR 4000 3C00h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	BSIZE[1:0]		—	—	—	EXENB
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	EXENB	Operation Enable	0: Disable 1: Enable.	R/W
b3 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b5, b4	BSIZE[1:0]	SDRAM Bus Width Select	b5 b4 0 0: 16-bit bus space 0 1: Setting prohibited 1 0: 8-bit bus space 1 1: Setting prohibited.	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

EXENB bit (Operation Enable)

The EXENB bit enables the operation of the SDRAM address space. On reset, operation is disabled (EXENB = 0). Attempts to access disabled areas have no effect.

When CSC and SDRAMC are in use at the same time, BCLK and SDCLK must operate at the same frequency.

15.3.8 SDC Mode Register (SDCMOD)

Address(es): BUS.SDCMOD 4000 3C01h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	EMODE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	EMODE	Endian Mode	0: Endian order of SDRAM address space is the same as the endian order of the operating mode 1: Endian order of SDRAM address space is not the endian order of the operating mode.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Writing to this register is possible only once after release from reset. Operation is not guaranteed if more than one write access is attempted.

EMODE bit (Endian Mode)

The EMODE bit specifies the endianness for the SDRAM address space. The Cortex-M4 core is fixed at little-endian order, so instruction code can only be allocated to external spaces with little-endian specified. If an area is specified as big-endian, no instruction code can be allocated to it.

CSnWCR2.AWAIT[1:0] value.

15.3.7 SDC控制寄存器(SDCCR)

Address(es): BUS.SDCCR 4000 3C00h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	BSIZE[1:0]		—	—	—	EXENB
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	EXENB	操作启用	0：禁用1 ：启用。	R/W
b3 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b5, b4	BSIZE[1:0]	SDRAM总线宽度选择	b5b400：16位总线空间01：禁止设置10：8位总线空间11：禁止设置。	R/W
b7, b6	—	Reserved	这些位被读取为0。写入值应为0。	R/W

EXENB位（操作使能）

EXENB位使能SDRAM地址空间的操作。复位时，操作被禁用（EXENB=0）。
尝试进入残疾人区没有效果。

当CSC和SDRAMC同时使用时，BCLK和SDCLK 必须工作在相同的频率。

15.3.8 SDC模式寄存器(SDCMOD)

Address(es): BUS.SDCMOD 4000 3C01h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	EMODE
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	EMODE	Endian Mode	0：SDRAM地址空间的字节序与工作模式的字节序相同 1：SDRAM地址空间的字节序不是工作模式的字节序。	R/W
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

解除复位后只能写入该寄存器一次。如果尝试多次写入访问，则无法保证操作。

EMODE位（字节序模式）

EMODE位指定SDRAM地址空间的字节顺序。Cortex-M4内核固定为little-endian顺序，因此指令代码只能分配到指定little-endian的外部空间。如果一个区域被指定为大端，则不能为其分配指令代码。

15.3.9 SDRAM Access Mode Register (SDAMOD)

Address(es): BUS.SDAMOD 4000 3C02h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	BE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	BE	Continuous Access Enable	0: Disable 1: Enable.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Set the SDAMOD register only when the conditions in Table 15.14 are satisfied. Otherwise, operation is not guaranteed.

BE bit (Continuous Access Enable)

The BE bit enables continuous access to the SDRAM access space.

Note: When the SDRAM area is accessed from bus masters other than graphic IPs, continuous access is always disabled regardless of the setting.

15.3.10 SDRAM Self-Refresh Control Register (SDSELF)

Address(es): BUS.SDSELF 4000 3C10h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	SFEN
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	SFEN	SDRAM Self-Refresh Enable	0: Disable 1: Enable.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Set the SDSELF register only when the conditions in Table 15.14 are satisfied. Otherwise, operation is not guaranteed.

SFEN bit (SDRAM Self-Refresh Enable)

The SFEN bit controls the self-refresh operation. Setting this bit to 1 initiates an auto-refresh cycle, after which self-refresh begins. Clearing this bit to 0 ends the self-refresh, and auto-refresh resumes. When the bit is set to 1, the write value takes effect when the self-refresh operation starts. When it is cleared to 0, the write value has already taken effect when auto-refresh starts after the end of the self-refresh.

15.3.9 SDRAM访问模式寄存器(SDAMOD)

Address(es): BUS.SDAMOD 4000 3C02h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	BE
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	BE	连续访问启用	0：禁用1 ：启用。	R/W
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

仅当满足表15.14中的条件时才设置SDAMOD寄存器。否则，无法保证操作。

BE位（连续访问使能）

BE位使能对SDRAM访问空间的连续访问。

Note: 当从图形IP以外的总线主控器访问SDRAM区域时，无论设置如何，都始终禁用连续访问。

15.3.10 SDRAM自刷新控制寄存器(SDSELF)

Address(es): BUS.SDSELF 4000 3C10h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	SFEN
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	SFEN	SDRAM Self-Refresh Enable	0：禁用1 ：启用。	R/W
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

仅当满足表15.14中的条件时才设置SDSELF寄存器。否则，无法保证操作。

SFEN位（SDRAM自刷新使能）

SFEN位控制自刷新操作。将该位设置为1会启动一个自动刷新周期，然后开始自刷新。将该位清0结束自刷新，并继续自动刷新。当该位设置为1时，写入值在自刷新操作开始时生效。清0时，自刷新结束后自刷新开始时写入值已经生效。

15.3.11 SDRAM Refresh Control Register (SDRFCR)

Address(es): BUS.SDRFCR 4000 3C14h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	REFW[3:0]				RFC[11:0]											
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Bit name	Description	R/W
b11 to b0	RFC[11:0]	Auto-Refresh Request Interval Setting	b11 b0 0 0 0 0 0 0 0 0 0 0 0 0: Setting prohibited 0 0 0 0 0 0 0 0 0 0 0 1: 2 cycles 0 0 0 0 0 0 0 0 0 0 1 0: 3 cycles : 1 1 1 1 1 1 1 1 1 1 1 1: 4096 cycles.	R/W
b15 to b12	REFW[3:0]	Auto-Refresh Cycle/Self-Refresh Clearing Cycle Count Setting	b15 b12 0 0 0 0: 1 cycle 0 0 0 1: 2 cycles 0 0 1 0: 3 cycles 0 0 1 1: 4 cycles 0 1 0 0: 5 cycles 0 1 0 1: 6 cycles 0 1 1 0: 7 cycles 0 1 1 1: 8 cycles 1 0 0 0: 9 cycles 1 0 0 1: 10 cycles 1 0 1 0: 11 cycles 1 0 1 1: 12 cycles 1 1 0 0: 13 cycles 1 1 0 1: 14 cycles 1 1 1 0: 15 cycles 1 1 1 1: 16 cycles.	R/W

RFC[11:0] bits (Auto-Refresh Request Interval Setting)

The RFC[11:0] bits specify the auto-refresh request interval. They can be written to at any time, regardless of the state of the Auto-Refresh Operation Enable bit (RFEN) in SDRFEN. If auto-refresh is enabled, the write value takes effect after the end of the auto-refresh cycles. The refresh counter uses SDCLK.

REFW[3:0] bits (Auto-Refresh Cycle/Self-Refresh Clearing Cycle Count Setting)

The REFW[3:0] bits specify the number of auto-refresh cycles and the number of self-refresh clearing cycles. They can be written to at any time, regardless of the state of the Auto-Refresh Operation Enable bit (RFEN) in SDRFEN. If an auto-refresh cycle is in progress, the value written to the bits while auto-refresh is enabled takes effect after the cycle completes.

Note: Auto-refresh requests are not accepted while the SDRAM is being accessed. This means they must sometimes wait until the access completes for the auto-refresh interval to be extended. Set the RFC[11:0] bits to an auto-refresh request interval value that meets the specifications of the SDRAM being used. Additionally, make sure to set the auto-refresh request interval to a duration longer than the auto-refresh cycle. The auto-refresh interval cannot be automatically adjusted when the frequency is changed during operation. In this case, perform a self-refresh operation and set the auto-refresh interval to an appropriate value for the frequency again.

15.3.11.1 Auto-refresh request interval and RFC set value

The SDRAMC (SDRAM area controller) includes a 12-bit refresh counter that generates auto-refresh requests at fixed intervals. Use the following equation to calculate the set value for the RFC[11:0] bits from the auto-refresh request interval:

RFC = (Auto-refresh request interval / SDCLK cycle) - 1

15.3.11 SDRAM刷新控制寄存器(SDRFCR)

Address(es): BUS.SDRFCR 4000 3C14h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	REFW[3:0]				RFC[11:0]											
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	位名称	Description	R/W
b11 to b0	RFC[11:0]	自动刷新请求间隔设置	b11b0000000000000：禁止设置000000000001：2个周期000000000010：3个周期：111111111111：4096次循环。	R/W
b15 to b12	REFW[3:0]	Auto-Refresh Cycle/Self-Refresh 清算周期计数设置	b15b120000：1个周期0001：2个周期0010：3个周期0011：4个周期0100：5个周期0101：6个周期0110：7循环0111：8循环1000：9循环1001：10循环1010：11循环1011：12循环1100：13循环1101：14循环1110：15个周期1111：16个周期。	R/W

RFC[11:0]位（自动刷新请求间隔设置）

RFC[11:0]位指定自动刷新请求间隔。无论SDRFEN中的自动刷新操作使能位(RFEN)的状态如何，它们都可以随时被写入。如果启用了自动刷新，则写入值在自动刷新周期结束后生效。刷新计数器使用SDCLK 。

REFW[3:0]位（自动刷新周期自刷新清除周期计数设置）

REFW[3:0]位指定自动刷新周期数和自刷新清除周期数。无论SDRFEN中的自动刷新操作使能位(RFEN)的状态如何，它们都可以随时被写入。如果正在进行自动刷新周期，则在启用自动刷新时写入位的值将在周期完成后生效。

Note: 访问SDRAM时不接受自动刷新请求。这意味着他们有时必须等到访问完成才能延长自动刷新间隔。将RFC[11:0]位设置为满足正在使用的SDRAM规范的自动刷新请求间隔值。此外，请确保将自动刷新请求间隔设置为比自动刷新周期更长的持续时间。在运行过程中改变频率时，自动刷新间隔不能自动调整。在这种情况下，请执行自刷新操作并再次将自动刷新间隔设置为适合频率的值。

15.3.11.1 自动刷新请求间隔和RFC设置值

SDRAMC（SDRAM区域控制器）包括一个12位刷新计数器，它以固定的时间间隔生成自动刷新请求。使用以下公式从自动刷新请求间隔计算RFC[11:0]位的设置值：

RFC=（自动刷新请求间隔SDCLK 周期）1

Note: Auto-refresh requests are not accepted while the SDRAM is being accessed. They must wait until the access completes. However, the counter value is updated regardless of whether or not the request was accepted. If two or more auto-refresh requests are generated while the SDRAM is being accessed, the second and subsequent requests are ignored.

15.3.12 SDRAM Auto-Refresh Control Register (SDRFEN)

Address(es): BUS.SDRFEN 4000 3C16h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	RFEN
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	RFEN	Auto-Refresh Operation Enable	0: Disable 1: Enable.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

RFEN bit (Auto-Refresh Operation Enable)

The RFEN bit enables auto-refresh operation. When auto-refresh is required, set the RFEN bit to 1 before SDRAM access.

Clearing this bit to 0 while auto-refreshing is enabled causes RFEN to be cleared to 0 and auto-refresh operation to halt after the end of the auto-refresh cycle.The interval at which refresh requests are generated is determined by the value in the Auto-Refresh Request Interval Setting bits (RFC[11:0]) in the SDRAM Refresh Control Register (SDRFCR).

15.3.13 SDRAM Initialization Sequence Control Register (SDICR)

Address(es): BUS.SDICR 4000 3C20h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	INIRQ
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	INIRQ	Initialization Sequence Start	0: Invalid 1: Start initialization sequence.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Writing to this register is possible only once after release from reset. Operation is not guaranteed if more than one write access is attempted.

INIRQ bit (Initialization Sequence Start)

Setting the INIRQ bit to 1 starts the SDRAM initialization sequence and automatically sets the Initialization Status bit (INIST) in the SDRAM Status Register (SDSR) to 1. The INIST bit clears automatically after the initialization sequence ends. The value written to the INIRQ bit is not retained.

Note: Set the INIRQ bit to start the SDRAM initialization sequence only when the conditions in Table 15.14 are satisfied. Otherwise, operation is not guaranteed.

Note: 访问SDRAM时不接受自动刷新请求。他们必须等到访问完成。但是，无论请求是否被接受，计数器值都会更新。如果在访问SDRAM时产生了两个或多个自动刷新请求，则忽略第二个和后续请求。

15.3.12 SDRAM自动刷新控制寄存器(SDRFEN)

Address(es): BUS.SDRFEN 4000 3C16h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	RFEN
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	RFEN	自动刷新操作启用	0：禁用1 ：启用。	R/W
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

RFEN位（自动刷新操作使能）

RFEN位使能自动刷新操作。当需要自动刷新时，在访问SDRAM之前将RFEN位设置为1。

在启用自动刷新时将此位清零会导致RFEN被清零，并且自动刷新操作在自动刷新周期结束后停止。生成刷新请求的时间间隔由SDRAM刷新控制寄存器(SDRFCR)中的自动刷新请求间隔设置位(RFC[11:0])。

15.3.13 SDRAM初始化序列控制寄存器(SDICR)

Address(es): BUS.SDICR 4000 3C20h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	INIRQ
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	INIRQ	初始化序列开始	0：无效1：开始初始化序列。	R/W
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

解除复位后只能写入该寄存器一次。如果尝试多次写入访问，则无法保证操作。

INIRQ位（初始化序列开始）

将INIRQ位设置为1启动SDRAM初始化序列，并自动将SDRAM状态寄存器(SDSR)中的初始化状态位(INIST)设置为1。初始化序列结束后INIST位自动清除。写入INIRQ位的值不保留。

Note: 仅当满足表15.14中的条件时，才设置INIRQ位以启动SDRAM初始化序列。否则，无法保证操作。

15.3.14 SDRAM Initialization Register (SDIR)

Address(es): BUS.SDIR 4000 3C24h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	PRC[2:0]			ARFC[3:0]				ARFI[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	ARFI[3:0]	Initialization Auto-Refresh Interval	b3 b0 0 0 0 0: 3 cycles 0 0 0 1: 4 cycles 0 0 1 0: 5 cycles 0 0 1 1: 6 cycles 0 1 0 0: 7 cycles 0 1 0 1: 8 cycles 0 1 1 0: 9 cycles 0 1 1 1: 10 cycles 1 0 0 0: 11 cycles 1 0 0 1: 12 cycles 1 0 1 0: 13 cycles 1 0 1 1: 14 cycles 1 1 0 0: 15 cycles 1 1 0 1: 16 cycles 1 1 1 0: 17 cycles 1 1 1 1: 18 cycles.	R/W
b7 to b4	ARFC[3:0]	Initialization Auto-Refresh Count	b7 b4 0 0 0 0: Setting prohibited 0 0 0 1: 1 time 0 0 1 0: 2 times 0 0 1 1: 3 times 0 1 0 0: 4 times 0 1 0 1: 5 times 0 1 1 0: 6 times 0 1 1 1: 7 times 1 0 0 0: 8 times 1 0 0 1: 9 times 1 0 1 0: 10 times 1 0 1 1: 11 times 1 1 0 0: 12 times 1 1 0 1: 13 times 1 1 1 0: 14 times 1 1 1 1: 15 times.	R/W
b10 to b8	PRC[2:0]	Initialization Precharge Cycle Count	b10 b8 0 0 0: 3 cycles 0 0 1: 4 cycles 0 1 0: 5 cycles 0 1 1: 6 cycles 1 0 0: 7 cycles 1 0 1: 8 cycles 1 1 0: 9 cycles 1 1 1: 10 cycles.	R/W
b15 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Writing to this register is possible only once after release from reset. Operation is not guaranteed if more than one write access is attempted.

ARFI[3:0] bits (Initialization Auto-Refresh Interval)

The ARFI[3:0] bits specify the interval at which the auto-refresh commands are issued in the SDRAM initialization sequence.

15.3.14 SDRAM初始化寄存器(SDIR)

Address(es): BUS.SDIR 4000 3C24h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	PRC[2:0]			ARFC[3:0]				ARFI[3:0]			
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b3 to b0	ARFI[3:0]	初始化自动刷新间隔	b3 b0 0 0 0 0: 3 cycles 0 0 0 1: 4 cycles 0 0 1 0: 5 cycles 0 0 1 1: 6 cycles 0 1 0 0: 7 cycles 0 1 0 1: 8 cycles 0 1 1 0: 9 cycles 0 1 1 1: 10 cycles 1 0 0 0: 11 cycles 1 0 0 1: 12 cycles 1 0 1 0: 13 cycles 1 0 1 1: 14 cycles 1 1 0 0: 15 cycles 1 1 0 1: 16 cycles 1 1 1 0: 17 cycles 1 1 1 1: 18 cycles.	R/W
b7 to b4	ARFC[3:0]	初始化自动刷新计数	b7b40000：禁止设置0001：1次0010：2次0011：3次0100：4次0101：5次0110：6次0111：7次1000：8次1001：9次1010：10次1011：11次1100：12次1101：13次1110：14次1111：15次。	R/W
b10 to b8	PRC[2:0]	初始化预充电循环计数	b10 b8 0 0 0: 3 cycles 0 0 1: 4 cycles 0 1 0: 5 cycles 0 1 1: 6 cycles 1 0 0: 7 cycles 1 0 1: 8 cycles 1 1 0: 9 cycles 1 1 1: 10 cycles.	R/W
b15 to b11	—	Reserved	这些位被读取为0。写入值应为0。	R/W

解除复位后只能写入该寄存器一次。如果尝试多次写入访问，则无法保证操作。

ARFI[3:0]位（初始化自动刷新间隔）

ARFI[3:0]位指定在SDRAM初始化序列中发出自动刷新命令的时间间隔。

ARFC[3:0] bits (Initialization Auto-Refresh Count)

The ARFC[3:0] bits specify the number of times auto-refresh is to be performed in the SDRAM initialization sequence.

PRC[2:0] bits (Initialization Precharge Cycle Count)

The PRC[2:0] bits specify the number of precharged cycles in the SDRAM initialization sequence.

Note: Implement settings that satisfy the specifications of the connected SDRAM before starting the initialization sequence.

15.3.15 SDRAM Address Register (SDADR)

Address(es): BUS.SDADR 4000 3C40h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	MXC[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	MXC[1:0]	Address Multiplex Select	b1 b0 0 0: 8-bit shift 0 1: 9-bit shift 1 0: 10-bit shift 1 1: 11-bit shift.	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Set SDADR only when the conditions in Table 15.14 are satisfied. Otherwise, operation is not guaranteed.

MXC[1:0] bits (Address Multiplex Select)

The MXC[1:0] bits select the size of the shift towards the lower half of the row address in row address/column address multiplexing. These bits also select the row address bits to be used for comparison in SDRAMC continuous access operation. For details, see Table 15.19.

15.3.16 SDRAM Timing Register (SDTR)

Address(es): BUS.SDTR 4000 3C44h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	RAS[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	RCD[1:0]		RP[2:0]			WR	—	—	—	—	—	CL[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	CL[2:0]	SDRAMC Column Latency	b2 b0 0 0 0: Setting prohibited 0 0 1: 1 cycle 0 1 0: 2 cycles 0 1 1: 3 cycles 1 0 0: Setting prohibited 1 0 1: Setting prohibited 1 1 0: Setting prohibited 1 1 1: Setting prohibited.	R/W

ARFC[3:0]位（初始化自动刷新计数）

ARFC[3:0]位指定在SDRAM初始化序列中执行自动刷新的次数。

PRC[2:0]位（初始化预充电周期计数）

PRC[2:0]位指定SDRAM初始化序列中的预充电周期数。

Note: 在开始初始化序列之前实施满足连接的SDRAM规范的设置。

15.3.15 SDRAM地址寄存器(SDADR)

Address(es): BUS.SDADR 4000 3C40h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	MXC[1:0]	
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b1, b0	MXC[1:0]	地址复用选择	b1 b0 0 0: 8-bit shift 0 1: 9-bit shift 1 0: 10-bit shift 1 1: 11-bit shift.	R/W
b7 to b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W

仅当满足表15.14中的条件时才设置SDADR。否则，无法保证操作。

MXC[1:0]位（地址复用选择）

MXC[1:0]位选择在行地址列地址复用中向行地址下半部分移动的大小。这些位还选择在SDRAMC连续存取操作中用于比较的行地址位。详见表15.19。

15.3.16 SDRAM时序寄存器(SDTR)

Address(es): BUS.SDTR 4000 3C44h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	RAS[2:0]		
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	RCD[1:0]		RP[2:0]			WR	—	—	—	—	—	CL[2:0]		
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bit	Symbol	位名称	Description	R/W
b2 to b0	CL[2:0]	SDRAMC列延迟	b2b0000：禁止设置001 ：1个周期010：2个周期0 11：3个周期100：禁止设 置101：禁止设置110：禁 止设置111：禁止设置.	R/W

Bit	Symbol	Bit name	Description	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	WR	Write Recovery Interval	0: 1 cycle 1: 2 cycles.	R/W
b11 to b9	RP[2:0]	Row Precharge Interval	b11 b9 0 0 0: 1 cycle 0 0 1: 2 cycles 0 1 0: 3 cycles 0 1 1: 4 cycles 1 0 0: 5 cycles 1 0 1: 6 cycles 1 1 0: 7 cycles 1 1 1: 8 cycles.	R/W
b13, b12	RCD[1:0]	Row Column Latency	b13 b12 0 0: 1 cycle 0 1: 2 cycles 1 0: 3 cycles 1 1: 4 cycles.	R/W
b15, b14	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b18 to b16	RAS[2:0]	Row Active Interval	b18 b16 0 0 0: 1 cycle 0 0 1: 2 cycles 0 1 0: 3 cycles 0 1 1: 4 cycles 1 0 0: 5 cycles 1 0 1: 6 cycles 1 1 0: 7 cycles 1 1 1: Setting prohibited.	R/W
b31 to b19	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The SDTR register specifies the timing for read and write accesses to the SDRAM. For more information, see section 15.6.11.3, Timing register settings and access timing.

Set the SDTR register only when the conditions in Table 15.14 are satisfied. Otherwise, operation is not guaranteed.

Writing to this register is possible only once after release from reset. Operation is not guaranteed if more than one write access is attempted.

CL[2:0] bits (SDRAMC Column Latency)

The CL[2:0] bits specify the column latency of the SDRAM controller. This setting only affects the latency setting on the SDRAM controller side. To specify the column latency for externally connected SDRAM, use the SDRAM mode register (SDMOD).

WR bit (Write Recovery Interval)

The WR bit specifies the interval that must elapse between the SDRAM write command (WRIT) and deactivation (PALL).

RP[2:0] bits (Row Precharge Interval)

The RP[2:0] bits specify the minimum number of cycles that must elapse between the SDRAM deactivation command (PALL) and the next valid command.

RAS[2:0] bits (Row Active Interval)

The RAS[2:0] bits specify the minimum interval that must elapse between the SDRAM row activation command (ACTV) and deactivation (PALL). The value specified in these bits must be less than or equal to the sum of the row column latency (RCD[1:0]) and column latency (CL[2:0]) settings.

Bit	Symbol	位名称	Description	R/W
b7 to b3	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b8	WR	写恢复间隔	0：1个周期1 ：2个周期。	R/W
b11 to b9	RP[2:0]	行预充电间隔	b11b9000：1个 周期001：2个周 期010：3个周期 011：4个周期10 0：5个周期101 ：6个周期110： 7个周期111：8 个周期.	R/W
b13, b12	RCD[1:0]	行列延迟	b13b1200：1 个周期01：2 个周期10：3 个周期11：4 个周期。	R/W
b15, b14	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b18 to b16	RAS[2:0]	行活动间隔	b18b16000：1个周期001 ：2个周期010：3个周期0 11：4个周期100：5个周 期101：6个周期110：7个 周期111：设置禁止.	R/W
b31 to b19	—	Reserved	这些位被读取为0。写入值应为0。	R/W

SDTR寄存器指定对SDRAM的读写访问的时序。有关详细信息，请参阅第15.6.11.3节，时序寄存器设置和访问时序。

仅当满足表15.14中的条件时才设置SDTR寄存器。否则，无法保证操作。

解除复位后只能写入该寄存器一次。如果尝试多次写入访问，则无法保证操作。

CL[2:0]位（SDRAMC列延迟）

CL[2:0]位指定SDRAM控制器的列延迟。此设置仅影响延迟设置
SDRAM控制器端。要指定外部连接的SDRAM的列延迟，请使用SDRAM模式寄存器(SDMOD)。

WR位（写恢复间隔）

WR位指定SDRAM写命令(WRIT)和停用(PALL)之间必须经过的时间间隔。

RP[2:0]位（行预充电间隔）

RP[2:0]位指定SDRAM停用命令(PALL)和下一个有效命令之间必须经过的最小周期数。

RAS[2:0]位（行活动间隔）

RAS[2:0]位指定SDRAM行激活命令(ACTV)和去激活(PALL)之间必须经过的最小间隔。这些位中指定的值必须小于或等于行列延迟(RCD[1:0])和列延迟(CL[2:0])设置的总和。

15.3.17 SDRAM Mode Register (SDMOD)

Address(es): BUS.SDMOD 4000 3C48h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	MR[14:0]														
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b14 to b0	MR[14:0]	Mode Register Setting	Writing to these bits triggers a mode register set command.	R/W
b15	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

The SDMOD register specifies the value to be written to the SDRAM mode register. Writing to SDMOD causes a mode register set command to be issued automatically to the SDRAM. Set SDMOD only when the conditions in Table 15.14 are satisfied. Otherwise, operation is not guaranteed.

Writing to this register is possible only once after release from reset. Operation is not guaranteed if more than one write access is attempted.

MR[14:0] bits (Mode Register Setting)

Writing to the MR[14:0] bits causes a mode register set command to be issued to the SDRAM, and the setting in the MR[14:0] bits is output to the lower bits of the address. For more information, see section 15.6.10, Setting the Mode Register.

Note: Set a burst length of 1 for the SDRAM. Operation is not guaranteed with any other burst length setting.
Note: The SDRAM column latency must match the setting in the SDRAMC Column Latency setting (CL[2:0]) in the SDRAM Timing Register (SDTR). Operation is not guaranteed if the latency settings do not agree.
Note: Make sure the SRFST, INIST, and MRSST status bits in the SDRAM Status Register (SDSR) are all 0.

15.3.18 SDRAM Status Register (SDSR)

Address(es): BUS.SDSR 4000 3C50h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	SRFST	INIST	—	—	MRSST
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	MRSST	Mode Register Setting Status	0: Mode register setting not in progress 1: Mode register setting in progress.	R
b2, b1	—	Reserved	These bits are read as 0.	R
b3	INIST	Initialization Status	0: Initialization sequence not in progress 1: Initialization sequence in progress.	R
b4	SRFST	Self-Refresh Transition/Recovery Status	0: Transition/recovery not in progress 1: Transition/recovery in progress.	R
b7 to b5	—	Reserved	These bits are read as 0.	R

MRSST bit (Mode Register Setting Status)

When set to 1, the MRSST bit indicates that SDRAM mode register setting is in progress.

15.3.17 SDRAM模式寄存器(SDMOD)

Address(es): BUS.SDMOD 4000 3C48h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	MR[14:0]														
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b14 to b0	MR[14:0]	模式寄存器设置	写入这些位会触发模式寄存器设置命令。	R/W
b15	—	Reserved	该位读取为0。写入值应为0。	R/W

SDMOD寄存器指定要写入SDRAM模式寄存器的值。写入SDMOD会导致自动向SDRAM发出模式寄存器设置命令。仅当满足表15.14中的条件时才设置SDMOD。否则，无法保证操作。

解除复位后只能写入该寄存器一次。如果尝试多次写入访问，则无法保证操作。

MR[14:0]位（模式寄存器设置）

写入MR[14:0]位会导致向SDRAM发出模式寄存器设置命令，并将MR[14:0]位中的设置输出到地址的低位。有关详细信息，请参阅第15.6.10节，设置模式
Register.

Note: 将SDRAM的突发长度设置为1。任何其他突发长度设置都不能保证操作。
Note: SDRAM列延迟必须与SDRAMC列延迟设置(CL[2:0])中的设置匹配
SDRAM时序寄存器(SDTR)。如果延迟设置不一致，则无法保证操作。
Note: 确保SDRAM状态寄存器(SDSR)中的SRFST、INIST和MRSST状态位均为0。

15.3.18 SDRAM状态寄存器(SDSR)

Address(es): BUS.SDSR 4000 3C50h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	SRFST	INIST	—	—	MRSST
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	MRSST	模式寄存器设置状态	0：模式寄存器设置未进行1：模式寄存器设置正在进行。	R
b2, b1	—	Reserved	这些位读为0。	R
b3	INIST	初始化状态	0：初始化序列未进行1：初始化序列正在进行。	R
b4	SRFST	Self-Refresh Transition/Recovery Status	0：过渡恢复未进行1：过渡恢复正在进行。	R
b7 to b5	—	Reserved	这些位读为0。	R

MRSST位（模式寄存器设置状态）

当设置为1时，MRSST位指示SDRAM模式寄存器设置正在进行中。

INIST bit (Initialization Status)

When set to 1, the INIST bit indicates that the SDRAM initialization sequence is in progress.

SRFST bit (Self-Refresh Transition/Recovery Status)

When set to 1, the SRFST bit indicates that a transition to or recovery from a self-refresh operation is in progress for the SDRAM. The in progress interval begins when the bits in Table 15.7 are written to and lasts until the associated commands are issued.

Note: Execution of a self-refresh, initialization sequence, or mode register setting can only be performed when all the status bits are 0. Do not rewrite the registers and bits in Table 15.7 when any of the SRFST, INIST, or MRSST status bits is set to 1.

Table 15.7 Registers and bits requiring status bit checking

Function	Register	Bits
Self-refresh	SDSELF	SFEN
Initialization sequence	SDICR	INIRQ
Mode register setting	SDMOD	MR[14:0]

15.3.19 Master Bus Control Register (BUSMCNT<master>)

Address(es): BUS.BUSMCNTM4I 4000 4000h, BUS.BUSMCNTM4D 4000 4004h, BUS.BUSMCNTSYS 4000 4008h, BUS.BUSMCNTDMA 4000 400Ch, BUS.BUSMCNTEDM 4000 4010h, BUS.BUSMCNTGPX 4000 4014h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	IERES	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b14 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15	IERES	Ignore Error Responses	0: Report bus errors 1: Do not report bus errors.	R/W

Note: Changing reserved bits from the initial value of 0 is prohibited. Operation during the change is not guaranteed.

Table 15.8 shows the registers associated with each bus type.

INIST位（初始化状态）

当设置为1时，INIST位指示SDRAM初始化序列正在进行中。

SRFST位（自刷新转换恢复状态）

当设置为1时，SRFST位指示正在转换到自刷新操作或从自刷新操作恢复
动态随机存取存储器。进行中间隔从写入表15.7中的位开始，一直持续到发出相关命令。

Note: 仅当所有状态位都为0时才能执行自刷新、初始化序列或模式寄存器设置。当任何SRFST、INIST或MRSST状态位设置时，请勿重写表15.7中的寄存器和位为1。

Table 15.7 需要状态位检查的寄存器和位

Function	Register	Bits
Self-refresh	SDSELF	SFEN
初始化序列	SDICR	INIRQ
模式寄存器设置	SDMOD	MR[14:0]

15.3.19 主总线控制寄存器(BUSMCNT<master>)

Address(es): BUS.BUSMCNTM4I 4000 4000h, BUS.BUSMCNTM4D 4000 4004h, BUS.BUSMCNTSYS 4000 4008h, BUS.BUSMCNTDMA 4000 400Ch, BUS.BUSMCNTEDM 4000 4010h, BUS.BUSMCNTGPX 4000 4014h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	IERES	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b14 to b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b15	IERES	忽略错误响应	0：报告总线错误1：不报告总线错误。	R/W

Note: 禁止从初始值0更改保留位。不保证更改期间的操作。

表15.8显示了与每种总线类型相关的寄存器。

Table 15.8 Associations between bus types and registers

Bus type	Master Bus Control Register	Slave Bus Control Register	Bus Error Address Register	Bus Error Status Register
ICode bus (CPU)	BUSMCNTM4I	-	BUS1ERRADD	BUS1ERRSTAT
DCode bus (CPU)	BUSMCNTM4D	-	BUS2ERRADD	BUS2ERRSTAT
System bus (CPU)	BUSMCNTSYS	-	BUS3ERRADD	BUS3ERRSTAT
DMA bus	BUSMCNTDMA	-	BUS4ERRADD	BUS4ERRSTAT
EDMAC bus	BUSMCNTEDM	-	BUS5ERRADD	BUS5ERRSTAT
GPX bus from JPEG (data input)	BUSMCNTGPX	BUSSCNTGPX	BUS6ERRADD	BUS6ERRSTAT
GPX bus from JPEG (data output)	BUSMCNTGPX	BUSSCNTGPX	BUS7ERRADD	BUS7ERRSTAT
GPX bus from GLCDC (Graphic1)	BUSMCNTGPX	BUSSCNTGPX	BUS8ERRADD	BUS8ERRSTAT
GPX bus from GLCDC (Graphic2)	BUSMCNTGPX	BUSSCNTGPX	BUS9ERRADD	BUS9ERRSTAT
GPX bus from DRW (texture)	BUSMCNTGPX	BUSSCNTGPX	BUS10ERRADD	BUS10ERRSTAT
GPX bus from DRW (data)	BUSMCNTGPX	BUSSCNTGPX	BUS11ERRADD	BUS11ERRSTAT
Memory bus 1	-	BUSSCNTFLI	-	-
Memory bus 2	-	BUSSCNTRAMH	-	-
Memory bus 3	-	BUSSCNTMBIU	-	-
Memory bus 4	-	BUSSCNTRAM0	-	-
Memory bus 5	-	BUSSCNTRAM1	-	-
Internal peripheral bus 1, 3, 4, 5, 7, 8	-	BUSSCNTPnB (n = 0, 2, 3, 4, 6, 7)	-	-
Internal peripheral bus 9	-	BUSSCNTFBU	-	-
External bus (CS and SDRAM areas)	-	BUSSCNTEXT	-	-
External bus (QSPI area)	-	BUSSCNTEXT2	-	-

IERES bit (Ignore Error Responses)

The IERES bit, when set, disables the AHB-Lite protocol error response.

15.3.20 Slave Bus Control Register (BUSSCNT<slave>)

Address(es): BUS.BUSSCNTFLI 4000 4100h, BUS.BUSSCNTRAMH 4000 4104h, BUS.BUSSCNTMBIU 4000 4108h, BUS.BUSSCNTRAM0 4000 410Ch, BUS.BUSSCNTRAM1 4000 4110h, BUS.BUSSCNTP0B 4000 4114h, BUS.BUSSCNTP2B 4000 4118h, BUS.BUSSCNTP3B 4000 411Ch, BUS.BUSSCNTP4B 4000 4120h, BUS.BUSSCNTP6B 4000 4128h, BUS.BUSSCNTP7B 4000 412Ch, BUS.BUSSCNTFBU 4000 4130h, BUS.BUSSCNTEXT 4000 4134h, BUS.BUSSCNTEXT2 4000 4138h, BUS.BUSSCNTGPX 4000 413Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	EWRES	—	—	ARBMET[1:0]		—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Table 15.8 总线类型和寄存器之间的关联

巴士类型	主总线控制寄存器	从总线控制寄存器	总线错误地址 Register	总线错误状态 Register
ICode bus (CPU)	BUSMCNTM4I	-	BUS1ERRADD	BUS1ERRSTAT
DCode bus (CPU)	BUSMCNTM4D	-	BUS2ERRADD	BUS2ERRSTAT
系统总线(CPU)	BUSMCNTSYS	-	BUS3ERRADD	BUS3ERRSTAT
DMA bus	BUSMCNTDMA	-	BUS4ERRADD	BUS4ERRSTAT
EDMAC bus	BUSMCNTEDM	-	BUS5ERRADD	BUS5ERRSTAT
来自JPEG的GPX总线（数据输入）	BUSMCNTGPX	BUSSCNTGPX	BUS6ERRADD	BUS6ERRSTAT
来自JPEG的GPX总线（数据输出）	BUSMCNTGPX	BUSSCNTGPX	BUS7ERRADD	BUS7ERRSTAT
来自GLCDC的GPX总线（图1）	BUSMCNTGPX	BUSSCNTGPX	BUS8ERRADD	BUS8ERRSTAT
来自GLCDC的GPX总线（图形2）	BUSMCNTGPX	BUSSCNTGPX	BUS9ERRADD	BUS9ERRSTAT
来自DRW的GPX总线（纹理）	BUSMCNTGPX	BUSSCNTGPX	BUS10ERRADD	BUS10ERRSTAT
来自DRW的GPX总线（数据）	BUSMCNTGPX	BUSSCNTGPX	BUS11ERRADD	BUS11ERRSTAT
内存总线1	-	BUSSCNTFLI	-	-
内存总线2	-	BUSSCNTRAMH	-	-
内存总线3	-	BUSSCNTMBIU	-	-
内存总线4	-	BUSSCNTRAM0	-	-
内存总线5	-	BUSSCNTRAM1	-	-
内部外围总线1、3、4、5、7、8	-	BUSSCNTPnB (n = 0, 2, 3, 4, 6, 7)	-	-
内部外围总线9	-	BUSSCNTFBU	-	-
外部总线（CS和SDRAM areas)	-	BUSSCNTEXT	-	-
外部总线（QSPI区域）	-	BUSSCNTEXT2	-	-

IERES位（忽略错误响应）

IERES位在设置时禁用AHB-Lite协议错误响应。

15.3.20 从总线控制寄存器(BUSSCNT<slave>)

Address(es): BUS.BUSSCNTFLI 4000 4100h, BUS.BUSSCNTRAMH 4000 4104h, BUS.BUSSCNTMBIU 4000 4108h, BUS.BUSSCNTRAM0 4000 410Ch, BUS.BUSSCNTRAM1 4000 4110h, BUS.BUSSCNTP0B 4000 4114h, BUS.BUSSCNTP2B 4000 4118h, BUS.BUSSCNTP3B 4000 411Ch, BUS.BUSSCNTP4B 4000 4120h, BUS.BUSSCNTP6B 4000 4128h, BUS.BUSSCNTP7B 4000 412Ch, BUS.BUSSCNTFBU 4000 4130h, BUS.BUSSCNTEXT 4000 4134h, BUS.BUSSCNTEXT2 4000 4138h, BUS.BUSSCNTGPX 4000 413Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	EWRES	—	—	ARBMET[1:0]		—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b3 to b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Bit	Symbol	Bit name	Description	R/W
b5, b4	ARBMET[1:0]	Arbitration Method	Specifies the group priorities. b5 b4 0 0: Fixed priority 0 1: Round-robin 1 0: Setting prohibited 1 1: Setting prohibited.	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	EWRES	Early Write Response	0: Disable early write response 1: Enable early write response.	R/W
b15 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Changing reserved bits from the initial value of 0 is prohibited. Operation during the change is not guaranteed.

Table 15.8 lists the registers associated with each bus type.

ARBMET[1:0] bits (Arbitration Method)

The ARBMET[1:0] bits specify the arbitration protocol, with priority defined for all bus masters. For fixed priority, see Table 15.9. For round-robin, see Table 15.10.

EWRES bit (Early Write Response)

The EWRES bit indicates whether the next write request is accepted before the response for the current write transaction occurs. When the value is 1, the next write request is accepted and high-speed transfer is possible, but AHB-Lite error responses are not detected. Bus errors are returned to the requesting master IP using the error response protocol for AHB-Lite. For details on errors that occur on each bus, see section 15.7, Bus Error Monitoring Section. Only use the BUSSCNTMBIU, BUSSCNTP0B, and BUSSCNTEXT registers.

Table 15.9 Bus priorities with fixed-priority arbitration (ARBMET[1:0] = 00b)

Slave Bus Control Register	Slave interface	Priority order
BUSSCNTFLI	Memory bus 1	Memory bus 3 > DCode bus (CPU) > ICode bus (CPU)
BUSSCNTRAMH	Memory bus 2	Memory bus 3 > DCode bus (CPU) > ICode bus (CPU)
BUSSCNTMBIU	Memory bus 3	GPX bus > ETHER bus > DMA bus
BUSSCNTRAM0	Memory bus 4	GPX bus > ETHER bus > DMA bus > system bus (CPU)
BUSSCNTRAM1	Memory bus 5	GPX bus > ETHER bus > DMA bus > system bus (CPU)
BUSSCNTPnB (n = 0, 2, 3, 4, 6, 7)	Internal peripheral bus 1, 3, 4, 5, 7, 8	DMA bus > system bus (CPU)
BUSSCNTFBU	Internal peripheral bus 9	ETHER bus > DMA bus > system bus (CPU)
BUSSCNTEXT	External bus (CS and SDRAM areas)	GPX bus > ETHER bus > DMA bus > system bus (CPU)
BUSSCNTEXT2	External bus (QSPI area)	GPX bus > ETHER bus > DMA bus > system bus (CPU)
BUSSCNTGPX	GPX bus	GLCDC (Graphic 1) > DRW (texture) > DRW (data) > JPEG (input) > GLCDC (Graphic 2) > JPEG (output)

Bit	Symbol	位名称	Description	R/W
b5, b4	ARBMET[1:0]	仲裁方式	指定组优先级。b5b400：固定优先级01：循环10：禁止设置11：禁止设置。	R/W
b7, b6	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b8	EWRES	早期写响应	0：禁用早期写入响应1：启用早期写入响应。	R/W
b15 to b9	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note: 禁止从初始值0更改保留位。不保证更改期间的操作。

表15.8列出了与每种总线类型相关的寄存器。

ARBMET[1:0]位（仲裁方法）

ARBMET[1:0]位指定仲裁协议，并为所有总线主机定义优先级。对于固定优先级，请参阅表15.9。对于循环，请参见表15.10。

EWRES位（早期写响应）

EWRES位指示在当前写事务的响应发生之前是否接受下一个写请求。值为1时，接受下一个写请求，可以进行高速传输，但未检测到AHB-Lite错误响应。使用AHBLite的错误响应协议将总线错误返回给请求的主IP。有关各总线上发生的错误的详细信息，请参阅第15.7节，总线错误监视部分。仅使用

BUSSCNTMBIU、BUSSCNTP0B和BUSSCNTEXT寄存器。

Table 15.9 具有固定优先级仲裁的总线优先级(ARBMET[1:0]=00b)

从总线控制寄存器	从接口	优先顺序
BUSSCNTFLI	内存总线1	内存总线3>DCode总线(CPU)>ICode总线(CPU)
BUSSCNTRAMH	内存总线2	内存总线3>DCode总线(CPU)>ICode总线(CPU)
BUSSCNTMBIU	内存总线3	GPX总线>ETHER总线>DMA总线
BUSSCNTRAM0	内存总线4	GPX总线>ETHER总线>DMA总线>系统总线(CPU)
BUSSCNTRAM1	内存总线5	GPX总线>ETHER总线>DMA总线>系统总线(CPU)
BUSSCNTPnB (n = 0, 2, 3, 4, 6, 7)	内部外围总线1、3、4、5、7、8	DMA总线>系统总线(CPU)
BUSSCNTFBU	内部外围总线9	ETHER总线>DMA总线>系统总线(CPU)
BUSSCNTEXT	外部总线（CS和SDRAM区域）	GPX总线>ETHER总线>DMA总线>系统总线(CPU)
BUSSCNTEXT2	外部总线（QSPI区域）	GPX总线>ETHER总线>DMA总线>系统总线(CPU)
BUSSCNTGPX	GPX bus	GLCDC (Graphic 1) > DRW (texture) > DRW (data) > JPEG (input) > GLCDC (Graphic 2) > JPEG (output)

Table 15.10 Bus priorities with round-robin priority arbitration (ARBMET[1:0] = 01b)

Slave Bus Control Register	Slave interface	Priority order*1
BUSSCNTFLI	Memory bus 1	Memory bus 3 <=> DCode bus (CPU) <=> ICode bus (CPU)
BUSSCNTRAMH	Memory bus 2	Memory bus 3 <=> DCode bus (CPU) <=> ICode bus (CPU)
BUSSCNTMBIU	Memory bus 3	GPX bus <=> ETHER bus <=> DMA bus
BUSSCNTRAM0	Memory bus 4	GPX bus <=> ETHER bus <=> DMA bus <=> system bus (CPU)
BUSSCNTRAM1	Memory bus 5	GPX bus <=> ETHER bus <=> DMA bus <=> system bus (CPU)
BUSSCNTPnB (n = 0, 2, 3, 4, 6, 7)	Internal peripheral bus 1, 3, 4, 5, 7, 8	DMA bus <=> system bus (CPU)
BUSSCNTFBU	Internal peripheral bus 9	ETHER bus <=> DMA bus <=> system bus (CPU)
BUSSCNTEXT	External bus (CS and SDRAM areas)	GPX bus <=> ETHER bus <=> DMA bus <=> system bus (CPU)
BUSSCNTEXT2	External bus (QSPI area)	GPX bus <=> ETHER bus <=> DMA bus <=> system bus (CPU)
BUSSCNTGPX	GPX bus	GLCDC (Graphic 1) > DRW (texture) > DRW (data) > JPEG (input) <=> GLCDC (Graphic 2) > JPEG (output)

Note 1. Round-robin priority is denoted by <=>.

15.3.21 Bus Error Address Register (BUSnERRADD) (n = 1 to 11)

Address(es): BUS.BUS1ERRADD 4000 4800h, BUS.BUS2ERRADD 4000 4810h, BUS.BUS3ERRADD 4000 4820h, BUS.BUS4ERRADD 4000 4830h, BUS.BUS5ERRADD 4000 4840h, BUS.BUS6ERRADD 4000 4850h, BUS.BUS7ERRADD 4000 4860h, BUS.BUS8ERRADD 4000 4870h, BUS.BUS9ERRADD 4000 4880h, BUS.BUS10ERRADD 4000 4890h, BUS.BUS11ERRADD 4000 48A0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	BERAD[31:16]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BERAD[15:0]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Bit	Symbol	Bit name	Description	R/W
b31 to b0	BERAD[31:0]	Bus Error Address	When a bus error occurs, these bits store the error address.	R

Note: This register is cleared only by reset other than MPU related reset. For more information, see section 6, Resets, and section 16, Memory Protection Unit (MPU).

Table 15.8 lists the registers associated with each bus type.

BERAD[31:0] bits (Bus Error Address)

When a bus error occurs, the BERAD[31:0] bits store the access address. For more information, see the BUSnERRSTAT.ERRSTAT bit description and section 15.7, Bus Error Monitoring Section.

A value of BUSnERRADD.BERAD[31:0] (n = 1 to 11) is only valid when BUSnERRSTAT.ERRSTAT (n = 1 to 11) is set to 1.

Table 15.10 具有循环优先级仲裁的总线优先级(ARBMET[1:0]=01b)

从总线控制寄存器	从接口	Priority order*1
BUSSCNTFLI	内存总线1	内存总线3<=>DCode总线(CPU)<=>ICode总线(CPU)
BUSSCNTRAMH	内存总线2	内存总线3<=>DCode总线(CPU)<=>ICode总线(CPU)
BUSSCNTMBIU	内存总线3	GPX总线<=>ETHER总线<=>DMA总线
BUSSCNTRAM0	内存总线4	GPX总线<=>ETHER总线<=>DMA总线<=>系统总线(CPU)
BUSSCNTRAM1	内存总线5	GPX总线<=>ETHER总线<=>DMA总线<=>系统总线(CPU)
BUSSCNTPnB (n = 0, 2, 3, 4, 6, 7)	内部外围总线1、3、4、5、7、8	DMA总线<=>系统总线(CPU)
BUSSCNTFBU	内部外围总线9	ETHER总线<=>DMA总线<=>系统总线(CPU)
BUSSCNTEXT	外部总线（CS和SDRAM区域）	GPX总线<=>ETHER总线<=>DMA总线<=>系统总线(CPU)
BUSSCNTEXT2	外部总线（QSPI区域）	GPX总线<=>ETHER总线<=>DMA总线<=>系统总线(CPU)
BUSSCNTGPX	GPX bus	GLCDC (Graphic 1) > DRW (texture) > DRW (data) > JPEG (input) <=> GLCDC (Graphic 2) > JPEG (output)

Note 1. 循环优先级由<=>表示。

15.3.21 总线错误地址寄存器(BUSnERRADD)(n=1到11)

Address(es): BUS.BUS1ERRADD 4000 4800h, BUS.BUS2ERRADD 4000 4810h, BUS.BUS3ERRADD 4000 4820h, BUS.BUS4ERRADD 4000 4830h, BUS.BUS5ERRADD 4000 4840h, BUS.BUS6ERRADD 4000 4850h, BUS.BUS7ERRADD 4000 4860h, BUS.BUS8ERRADD 4000 4870h, BUS.BUS9ERRADD 4000 4880h, BUS.BUS10ERRADD 4000 4890h, BUS.BUS11ERRADD 4000 48A0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	BERAD[31:16]															
重置后的值:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BERAD[15:0]															
重置后的值:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Bit	Symbol	位名称	Description	R/W
b31 to b0	BERAD[31:0]	总线错误地址	当发生总线错误时，这些位存储错误地址。	R

Note: 该寄存器只能通过复位而不是与MPU相关的复位来清除。有关详细信息，请参阅第6节“重置”和第16节，内存保护单元（MPU）。

表15.8列出了与每种总线类型相关的寄存器。

BERAD[31:0]位（总线错误地址）

当发生总线错误时，BERAD[31:0]位存储访问地址。有关详细信息，请参阅BUSnERRSTAT.ERRSTAT位描述和第15.7节，总线错误监控部分。

BUSnERRADD.BERAD[31:0]（n=1到11）的值仅在BUSnERRSTAT.ERRSTAT（n=1到11）设置为1时有效。

15.3.22 Bus Error Status Register (BUSnERRSTAT) (n = 1 to 11)

Address(es): BUS.BUS1ERRSTAT 4000 4804h, BUS.BUS2ERRSTAT 4000 4814h, BUS.BUS3ERRSTAT 4000 4824h, BUS.BUS4ERRSTAT 4000 4834h, BUS.BUS5ERRSTAT 4000 4844h, BUS.BUS6ERRSTAT 4000 4854h, BUS.BUS7ERRSTAT 4000 4864h, BUS.BUS8ERRSTAT 4000 4874h, BUS.BUS9ERRSTAT 4000 4884h, BUS.BUS10ERRSTAT 4000 4894h, BUS.BUS11ERRSTAT 4000 48A4h

	b7	b6	b5	b4	b3	b2	b1	b0
	ERRSTAT	—	—	—	—	—	—	ACCSTAT
Value after reset:	0	0	0	0	0	0	0	x

Bit	Symbol	Bit name	Description	R/W
b0	ACCSTAT	Error Access Status	Access status when the error occurred: 1: Write access 0: Read access.	R
b6 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	ERRSTAT	Bus Error Status	0: No bus error occurred 1: Bus error occurred.	R

Note: This register is cleared only by reset other than MPU related reset. For more information, see section 6, Resets, and section 16, Memory Protection Unit (MPU).

Table 15.8 lists the registers associated with each bus type.

ACCSTAT bit (Error Access Status)

The ACCSTAT bit indicates the access status, write access or read access, when an error occurs on the associated bus. For more information, see the BUSnERRSTAT.ERRSTAT bit description and section 15.7, Bus Error Monitoring Section.

The value is only valid when BUSnERRSTAT.ERRSTAT (n = 1 to 11) is set to 1.

ERRSTAT bit (Bus Error Status)

The ERRSTAT bit indicates whether a bus error occurred. When an error occurs on the associated bus, the access address and status of write or read access are stored. BUSnERRSTATn.ERRSTAT (n = 1 to 11) is set to 1.

The following types of errors can occur on each bus:

- Illegal address access
- Bus master MPU error
- Bus slave MPU error
- Time out.

When detecting bus master MPU errors or bus slave MPU errors, and reset is selected in the respective OAD bit, BUSnERRSTAT.ERRSTAT (n = 1 to 11) is not set to 1 if the bus access that caused the MPU error completes later than the internal reset signal being generated, which may occur depending on the wait setting.

When detecting bus master MPU errors or bus slave MPU errors, and NMI is selected in the respective OAD bit, BUSnERRSTAT.ERRSTAT (n = 1 to 11) is set to 1 when the bus access that caused the MPU error completes.

For more information on errors that occur on each bus, see section 15.7, Bus Error Monitoring Section, and section 16, Memory Protection Unit (MPU). For the GPX bus, BUSnERRSTAT.ERRSTAT (n = 6 to 11) is normally set to 1 unless a transfer request by different master bus is made after access with a bus master MPU error.

15.4 Endianness and Data Alignment

The external bus has a data alignment function to control which byte of the data bus (D15 to D08, D07 to D00) is used when accessing the external address space (the CS and SDRAM areas). Alignment is based on the bus specifications of the area to be accessed (8-bit or 16-bit bus space), the data size, and the endian order.

15.3.22 总线错误状态寄存器(BUSnERRSTAT)(n=1到11)

Address(es): BUS.BUS1ERRSTAT 4000 4804h, BUS.BUS2ERRSTAT 4000 4814h, BUS.BUS3ERRSTAT 4000 4824h, BUS.BUS4ERRSTAT 4000 4834h, BUS.BUS5ERRSTAT 4000 4844h, BUS.BUS6ERRSTAT 4000 4854h, BUS.BUS7ERRSTAT 4000 4864h, BUS.BUS8ERRSTAT 4000 4874h, BUS.BUS9ERRSTAT 4000 4884h, BUS.BUS10ERRSTAT 4000 4894h, BUS.BUS11ERRSTAT 4000 48A4h

	b7	b6	b5	b4	b3	b2	b1	b0
	ERRSTAT	—	—	—	—	—	—	ACCSTAT
重置后的值:	0	0	0	0	0	0	0	x

Bit	Symbol	位名称	Description	R/W
b0	ACCSTAT	错误访问状态	发生错误时的访问状态：1：写访问0： 读访问。	R
b6 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b7	ERRSTAT	总线错误状态	0：未发生总线错误1： 发生总线错误。	R

Note: 该寄存器只能通过复位而不是与MPU相关的复位来清除。有关详细信息，请参阅第6节“重置”和第16节，内存保护单元（MPU）。

表15.8列出了与每种总线类型相关的寄存器。

ACCSTAT位（错误访问状态）

当相关总线上发生错误时，ACCSTAT位指示访问状态、写访问或读访问。

有关详细信息，请参阅BUSnERRSTAT.ERRSTAT位描述和第15.7节，总线错误监控Section.

该值仅在BUSnERRSTAT.ERRSTAT（n=1到11）设置为1时有效。

ERRSTAT位（总线错误状态）

ERRSTAT位指示是否发生总线错误。当相关总线上发生错误时，将存储访问地址和写入或读取访问的状态。BUSnERRSTATn.ERRSTAT（n=1到11）设置为1。

每条总线上都可能发生以下类型的错误：

- 非法地址访问
- 总线主控MPU错误
- 总线从机MPU错误
- 暂停。

当检测到总线主MPU错误或总线从MPU错误时，在相应的OAD位中选择复位，BUSnERRSTAT.ERRSTAT(n=1到11)如果导致MPU错误的总线访问在内部复位信号生成之后完成，则不将其设置为1，这可能取决于等待设置。

当检测到总线主机MPU错误或总线从机MPU错误时，在各自的OAD位中选择NMI，当导致MPU错误的总线访问完成时，BUSnERRSTAT.ERRSTAT（n=1到11）设置为1。

有关每条总线上发生的错误的更多信息，请参阅第15.7节，总线错误监控部分和第16节，内存保护单元(MPU)。对于GPX总线，BUSnERRSTAT.ERRSTAT（n=6到11）通常设置为1，除非在访问后因总线主控MPU错误发出不同主控总线的传输请求。

15.4 字节顺序和数据对齐

外部总线具有数据对齐功能，用于控制访问外部地址空间（CS和SDRAM区域）时使用数据总线的哪个字节（D15到D08，D07到D00）。对齐基于要访问的区域的总线规范（8位或16位总线空间）、数据大小和字节序。

15.4.1 Data Alignment Control for the CS Areas

(1) 16-bit bus space

When a 16-bit bus space is selected in the BSIZE[1:0] bits in CSnCR, address buses A23 to A01 are enabled to output address signals in 16-bit units, and the address bus A00 is disabled (always outputs low).

When byte strobe mode is selected (WRMOD = 0 in CSnMOD), the WR0 and WR1 pins are enabled. The BC0 and BC1 pins are not used.

When single-write strobe mode is selected (WRMOD = 1 in CSnMOD), only the WR0 pin is enabled, and it always outputs low during write access, regardless of the data size. The WR1 pin is invalid (always outputs high). The valid byte position is indicated by the BC0 and BC1 pins.

The valid positions of control signals and data external to the chip differ depending on the endian order. See Figure 15.3 and Figure 15.4.

Page access can occur for accesses to data in 32-bit units. Page access can only occur when an access does not extend over a 32-bit boundary and causes no change in the BC0 and BC1 signals. The situations in which page access occurs are indicated by the letter (p) in Figure 15.3 and Figure 15.4.

Data size	Accessed address	Number of accesses	Bus cycle	Unit of data	Address		WR1/BC1 / WR0/BC0 RD Data bus D15–D08	D07–D00
8 bits	4n	One	First	8 bits	4n			7–0
	4n+1	One	First	8 bits	4n		7–0	
	4n+2	One	First	8 bits	4n+2			7–0
	4n+3	One	First	8 bits	4n+2		7–0	
16 bits	4n	One	First	16 bits	4n		15–8	7–0
	4n+2	One	First	16 bits	4n+2		15–8	7–0
32 bits	4n	Two	First	16 bits	4n		15–8	7–0
			Second	16 bits	4n+2	(p)	31–24	23–16

(p): Page access (only when page access is enabled in the PRENB and PWENB bits in CSnMOD).

Figure 15.3 Data alignment in 16-bit bus space with little-endian order for CS areas

15.4.1 CS区域的数据对齐控制

(1) 16位总线空间

在CSnCR的BSIZE[1:0]位中选择16位总线空间时，地址总线A23到A01被使能，以16位为单位输出地址信号，地址总线A00被禁用（始终输出低电平）.

Whenbytestrobemodeisselected(WRMOD=0inCSnMOD) theWR0andWR1pinsareenabled.不使用BC0和BC1引脚。

Whensingle-writestrobemodeisselected(WRMOD=1inCSnMOD) onlytheWR0pinisenabled anditalwaysoutput slowduringwriteaccess regardlessofthedatasize.WR1引脚无效（始终输出高电平）。有效字节位置由BC0和BC1引脚指示。

芯片外部控制信号和数据的有效位置因字节序而异。请参见图15.3和图15.4。

对32位单元中的数据的访问可能会发生页面访问。只有当访问不超过32位边界并且不会导致BC0和BC1信号发生变化时，才会发生页面访问。页面访问发生的情况由图15.3和图15.4中的字母(p)表示。

数据大小	访问地址	访问次数	巴士循环	数据单位	Address		WR1/BC1 / WR0/BC0 RD 数据总线 D15–D08	D07–D00
8 bits	4n	One	First	8 bits	4n			7–0
	4n+1	One	First	8 bits	4n		7–0	
	4n+2	One	First	8 bits	4n+2			7–0
	4n+3	One	First	8 bits	4n+2		7–0	
16 bits	4n	One	First	16 bits	4n		15–8	7–0
	4n+2	One	First	16 bits	4n+2		15–8	7–0
32 bits	4n	Two	First	16 bits	4n		15–8	7–0
			Second	16 bits	4n+2	(p)	31–24	23–16

(p)：页面访问（仅当在CSnMOD的PRENB和PWENB位中启用页面访问时）。

Figure 15.3 16位总线空间中的数据对齐，CS区域采用little-endian顺序

Data size	Accessed address	Number of accesses	Bus cycle	Unit of data	Address	WR1/BC1 / WR0/BC0 / RD — Data bus D15 D08 D07 D00
8 bits	4n	One	First	8 bits	4n	7 0
	4n+1	One	First	8 bits	4n	7 0
	4n+2	One	First	8 bits	4n+2	7 0
	4n+3	One	First	8 bits	4n+2	7 0
16 bits	4n	One	First	16 bits	4n	15 8 7 0
	4n+2	One	First	16 bits	4n+2	15 8 7 0
32 bits	4n	Two	First	16 bits	4n	31 24 23 16
			Second	16 bits	4n+2 (p)	15 8 7 0

(p): Page access (only when page access is enabled in the PRENB and PWENB bits in CSnMOD).

Figure 15.4 Data alignment in 16-bit bus space with big-endian order for CS areas

(2) 8-bit bus space

When an 8-bit bus space is selected in the BSIZE[1:0] bits in CSnCR, the address buses A23 to A00 are enabled to output address signals in byte units.

In 8-bit bus space, only the WR0 pin is valid, regardless of the write access mode, and it always outputs low during write access. The WR1 and BC0 pins are not used.

The valid positions of data external to the chip are D07 to D00, and WR0 is used as the control signal, regardless of the endian mode. See Figure 15.5 and Figure 15.6.

Page access can occur for accesses to data in 16-bit or 32-bit units. Page access can only occur when an access does not extend over a 32-bit boundary. The situations in which page access occurs are indicated by the letter (p) in Figure 15.5 and Figure 15.6.

数据大小	访问地址	访问次数	巴士循环	数据单位	Address	WR1/BC1 / WR0/BC0 / RD — 数据总线 D15 D08 D07 D00
8 bits	4n	One	First	8 bits	4n	7 0
	4n+1	One	First	8 bits	4n	7 0
	4n+2	One	First	8 bits	4n+2	7 0
	4n+3	One	First	8 bits	4n+2	7 0
16 bits	4n	One	First	16 bits	4n	15 8 7 0
	4n+2	One	First	16 bits	4n+2	15 8 7 0
32 bits	4n	Two	First	16 bits	4n	31 24 23 16
			Second	16 bits	4n+2 (p)	15 8 7 0

(p)：页面访问（仅当在CSnMOD的PRENB和PWENB位中启用页面访问时）。

Figure 15.4 16位总线空间中的数据对齐，CS区域采用大端顺序

(2) 8位总线空间

当在CSnCR的BSIZE[1:0]位中选择8位总线空间时，地址总线A23到A00被启用，以字节为单位输出地址信号。

在8位总线空间中，只有WR0引脚有效，与写访问模式无关，并且在写访问期间始终输出低电平。不使用WR1和BC0引脚。

片外数据的有效位置为D07～D00，WR0作为控制信号，与endian模式无关。请参见图15.5和图15.6。

对16位或32位单元中的数据的访问可能会发生页访问。只有当访问不超过32位边界时，才会发生页面访问。页面访问发生的情况在图15.5和图15.6中用字母(p)表示。

Data size	Accessed address	Number of accesses	Bus cycle	Unit of data	Address		WR1/BC1 RD D15 D08	WR0/BC0 RD D07 D00
8 bits	4n	One	First	8 bits	4n			7 0
	4n+1	One	First	8 bits	4n+1			7 0
	4n+2	One	First	8 bits	4n+2			7 0
	4n+3	One	First	8 bits	4n+3			7 0
16 bits	4n	Two	First	8 bits	4n			7 0
			Second	8 bits	4n+1	(p)		15 8
	4n+2	Two	First	8 bits	4n+2			7 0
			Second	8 bits	4n+3	(p)		15 8
32 bits	4n	Four	First	8 bits	4n			7 0
			Second	8 bits	4n+1	(p)		15 8
			Third	8 bits	4n+2	(p)		23 16
			Fourth	8 bits	4n+3	(p)		31 24

(p): Page access (only when page access is enabled in the PRENB and PWENB bits in CSnMOD)

Figure 15.5 Data alignment in 8-bit bus space with little-endian order for CS areas

Data size	Accessed address	Number of accesses	Bus cycle	Unit of data	Address		WR1/BC1 RD D15 D08	WR0/BC0 RD D07 D00
8 bits	4n	One	First	8 bits	4n			7 0
	4n+1	One	First	8 bits	4n+1			7 0
	4n+2	One	First	8 bits	4n+2			7 0
	4n+3	One	First	8 bits	4n+3			7 0
16 bits	4n	Two	First	8 bits	4n			15 8
			Second	8 bits	4n+1	(p)		7 0
	4n+2	Two	First	8 bits	4n+2			15 8
			Second	8 bits	4n+3	(p)		7 0
32 bits	4n	Four	First	8 bits	4n			31 24
			Second	8 bits	4n+1	(p)		23 16
			Third	8 bits	4n+2	(p)		15 8
			Fourth	8 bits	4n+3	(p)		7 0

(p): Page access (only when page access is enabled in the PRENB and PWENB bits in CSnMOD)

Figure 15.6 Data alignment in 8-bit bus space with big-endian order for CS areas

数据大小	访问地址	访问次数	巴士循环	数据单位	Address		WR1/BC1 RD D15 D08	WR0/BC0 RD D07 D00
8 bits	4n	One	First	8 bits	4n			7 0
	4n+1	One	First	8 bits	4n+1			7 0
	4n+2	One	First	8 bits	4n+2			7 0
	4n+3	One	First	8 bits	4n+3			7 0
16 bits	4n	Two	First	8 bits	4n			7 0
			Second	8 bits	4n+1	(p)		15 8
	4n+2	Two	First	8 bits	4n+2			7 0
			Second	8 bits	4n+3	(p)		15 8
32 bits	4n	Four	First	8 bits	4n			7 0
			Second	8 bits	4n+1	(p)		15 8
			Third	8 bits	4n+2	(p)		23 16
			Fourth	8 bits	4n+3	(p)		31 24

(p)：页面访问（仅当在CSnMOD的PRENB和PWENB位中启用页面访问时）

Figure 15.5 8位总线空间中的数据对齐，CS区域采用little-endian顺序

数据大小	访问地址	访问次数	巴士循环	数据单位	Address		WR1/BC1 RD D15 D08	WR0/BC0 RD D07 D00
8 bits	4n	One	First	8 bits	4n			7 0
	4n+1	One	First	8 bits	4n+1			7 0
	4n+2	One	First	8 bits	4n+2			7 0
	4n+3	One	First	8 bits	4n+3			7 0
16 bits	4n	Two	First	8 bits	4n			15 8
			Second	8 bits	4n+1	(p)		7 0
	4n+2	Two	First	8 bits	4n+2			15 8
			Second	8 bits	4n+3	(p)		7 0
32 bits	4n	Four	First	8 bits	4n			31 24
			Second	8 bits	4n+1	(p)		23 16
			Third	8 bits	4n+2	(p)		15 8
			Fourth	8 bits	4n+3	(p)		7 0

(p)：页面访问（仅当在CSnMOD的PRENB和PWENB位中启用页面访问时）

Figure 15.6 8位总线空间中的数据对齐，CS区域采用大端顺序

15.4.2 Data Alignment Control for the SDRAM Area

(1) 16-bit bus space

When a 16-bit bus space is selected in the BSIZE[1:0] bits in SDCCR, address buses A26 to A01 are enabled to output address signals in 16-bit units, and the address bus A00 is disabled (always outputs low). The valid byte position is indicated by the DQM0 and DQM1 signals.

External data is accessed using the DQ15 to DQ08 and DQ07 to DQ00 pins and DQM0 and DQM1 control signals. Data can be accessed in either 8-bit or 16-bit units at a time.

The valid positions of control signals and data external to the chip differ depending on the endian order. See Figure 15.7 and Figure 15.8.

Consecutive access can occur for accesses to data in 8- or 16-bit units. Consecutive access can only occur when a single bus access is generated in response to a single transfer request. The situations in which consecutive access occurs are indicated by “(r1)” in Figure 15.7 and Figure 15.8.

Data size	Accessed address	Number of accesses	Bus cycle	Unit of data	Address		DQM1 / DQM0 / WE / Data bus DQ15 DQ08 DQ07 DQ00
8 bits	4n	One	First	8 bits	4n	(r1)	7 0
	4n+1	One	First	8 bits	4n	(r1)	7 0
	4n+2	One	First	8 bits	4n+2	(r1)	7 0
	4n+3	One	First	8 bits	4n+2	(r1)	7 0
16 bit	4n	One	First	16 bits	4n	(r1)	15 8 7 0
	4n+2	One	First	16 bits	4n+2	(r1)	15 8 7 0
32 bits	4n	Two	First	16 bits	4n		15 8 7 0
			Second	16 bits	4n+2		31 24 23 16

(r1): Consecutive access (only when consecutive access is enabled by BE = 1 in SDAMOD during the HMI burst transfer.)

Figure 15.7 Data alignment in 16-bit bus space with little-endian order for SDRAM area

Data size	Accessed address	Number of accesses	Bus cycle	Unit of data	Address		DQM1 / DQM0 / WE / Data bus DQ15 DQ08 DQ07 DQ00
8 bits	4n	One	First	8 bits	4n	(r1)	7 0
	4n+1	One	First	8 bits	4n	(r1)	7 0
	4n+2	One	First	8 bits	4n+2	(r1)	7 0
	4n+3	One	First	8 bits	4n+2	(r1)	7 0
16 bits	4n	One	First	16 bits	4n	(r1)	15 8 7 0
	4n+2	One	First	16 bits	4n+2	(r1)	15 8 7 0
32 bits	4n	Two	First	16 bits	4n		31 24 23 16
			Second	16 bits	4n+2		15 8 7 0

(r1): Consecutive access (only when consecutive access is enabled by BE = 1 in SDAMOD during the HMI burst transfer.)

Figure 15.8 Data alignment in 16-bit bus space with big-endian order for SDRAM area

(2) 8-bit bus space

When an 8-bit width is selected in the BSIZE[1:0] bits in SDCCR, address buses A26 to A00 are enabled to output address signals in 8-bit units.

15.4.2 SDRAM区域的数据对齐控制

(1) 16位总线空间

在SDCCR的BSIZE[1:0]位中选择16位总线空间时，地址总线A26到A01被使能，以16位为单位输出地址信号，地址总线A00被禁用（始终输出低电平）.有效字节位置由DQM0和DQM1信号指示。

使用DQ15至DQ08和DQ07至DQ00引脚以及DQM0和DQM1控制信号访问外部数据。一次可以以8位或16位单元访问数据。

芯片外部控制信号和数据的有效位置因字节序而异。请参见图15.7和图15.8。

对8位或16位单元中的数据的访问可能会发生连续访问。只有在响应单个传输请求而生成单个总线访问时，才能发生连续访问。发生连续访问的情况在图15.7和图15.8中用“(r1)”表示。

数据大小	访问地址	访问次数	巴士循环	数据单位	Address		DQM1 / DQM0 / WE / 数据总线 DQ15 DQ08 DQ07 DQ00
8 bits	4n	One	First	8 bits	4n	(r1)	7 0
	4n+1	One	First	8 bits	4n	(r1)	7 0
	4n+2	One	First	8 bits	4n+2	(r1)	7 0
	4n+3	One	First	8 bits	4n+2	(r1)	7 0
16 bit	4n	One	First	16 bits	4n	(r1)	15 8 7 0
	4n+2	One	First	16 bits	4n+2	(r1)	15 8 7 0
32 bits	4n	Two	First	16 bits	4n		15 8 7 0
			Second	16 bits	4n+2		31 24 23 16

(r1)：连续访问（仅当在HMI突发传输期间通过SDAMOD中的BE=1启用连续访问时。）

Figure 15.7 16位总线空间中的数据对齐，SDRAM区域采用little-endian顺序

数据大小	访问地址	访问次数	巴士循环	数据单位	Address		DQM1 / DQM0 / WE / 数据总线 DQ15 DQ08 DQ07 DQ00
8 bits	4n	One	First	8 bits	4n	(r1)	7 0
	4n+1	One	First	8 bits	4n	(r1)	7 0
	4n+2	One	First	8 bits	4n+2	(r1)	7 0
	4n+3	One	First	8 bits	4n+2	(r1)	7 0
16 bits	4n	One	First	16 bits	4n	(r1)	15 8 7 0
	4n+2	One	First	16 bits	4n+2	(r1)	15 8 7 0
32 bits	4n	Two	First	16 bits	4n		31 24 23 16
			Second	16 bits	4n+2		15 8 7 0

(r1)：连续访问（仅当在HMI突发传输期间通过SDAMOD中的BE=1启用连续访问时。）

Figure 15.8 16位总线空间中的数据对齐，SDRAM区域的大端顺序

(2) 8位总线空间

当在SDCCR的BSIZE[1:0]位中选择8位宽度时，地址总线A26到A00被启用以输出8位单元的地址信号。

External data is accessed using the DQ07 to DQ00 pins and DQM0 control signal. 8-bit data is accessed in single 8-bit accesses, 16-bit data with two 8-bit accesses, and 32-bit data with four 8-bit accesses.

The valid positions of control signals and data external to the chip differ depending on the endian order. See Figure 15.9 and Figure 15.10.

Consecutive access can occur in access to data in 8-bit units. Consecutive access can only occur when a single bus access is generated in response to a single transfer request. The situations in which consecutive access occurs are indicated by "(r1)" in Figure 15.9 and Figure 15.10.

Data size	Accessed address	Number of accesses	Bus cycle	Unit of data	Address		DQM1 / DQM0 / WE / Data bus DQ15 DQ08 DQ07 DQ00
8 bits	4n	One	First	8 bits	4n	(r1)	7 0
	4n+1	One	First	8 bits	4n+1	(r1)	7 0
	4n+2	One	First	8 bits	4n+2	(r1)	7 0
	4n+3	One	First	8 bits	4n+3	(r1)	7 0
16 bits	4n	Two	First	8 bits	4n		7 0
			Second	8 bits	4n+1		15 8
	4n+2	Two	First	8 bits	4n+2		7 0
			Second	8 bits	4n+3		15 8
32 bits	4n	Four	First	8 bits	4n		7 0
			Second	8 bits	4n+1		15 8
			Third	8 bits	4n+2		23 16
			Fourth	8 bits	4n+3		31 24

(r1): Consecutive access (only when consecutive access is enabled by BE = 1 in SDAMOD during the HMI burst transfer.)

Figure 15.9 Data alignment in 8-bit bus space with little-endian order for SDRAM area

Data size	Accessed address	Number of accesses	Bus cycle	Unit of data	Address		DQM1 / DQM0 / WE / Data bus DQ15 DQ08 DQ07 DQ00
8 bits	4n	One	First	8 bits	4n	(r1)	7 0
	4n+1	One	First	8 bits	4n+1	(r1)	7 0
	4n+2	One	First	8 bits	4n+2	(r1)	7 0
	4n+3	One	First	8 bits	4n+3	(r1)	7 0
16 bits	4n	Two	First	8 bits	4n		15 8
			Second	8 bits	4n+1		7 0
	4n+2	Two	First	8 bits	4n+2		15 8
			Second	8 bits	4n+3		7 0
32 bits	4n	Four	First	8 bits	4n		31 24
			Second	8 bits	4n+1		23 16
			Third	8 bits	4n+2		15 8
			Fourth	8 bits	4n+3		7 0

(r1): Consecutive access (only when consecutive access is enabled by BE = 1 in SDAMOD during the HMI burst transfer.)

Figure 15.10 Data alignment in 8-bit bus space with big-endian order for SDRAM area

使用DQ07至DQ00引脚和DQM0控制信号访问外部数据。8位数据通过单个8位访问进行访问，16位数据通过两个8位访问进行访问，32位数据通过四个8位访问进行访问。

芯片外部控制信号和数据的有效位置因字节序而异。请参见图15.9和图15.10。

连续访问可以发生在访问8位单元中的数据时。只有在响应单个传输请求而生成单个总线访问时，才能发生连续访问。发生连续访问的情况在图15.9和图15.10中用"(r1)"表示。

数据大小	访问地址	访问次数	巴士循环	数据单位	Address		DQM1 / DQM0 / WE / 数据总线 DQ15 DQ08 DQ07 DQ00
8 bits	4n	One	First	8 bits	4n	(r1)	7 0
	4n+1	One	First	8 bits	4n+1	(r1)	7 0
	4n+2	One	First	8 bits	4n+2	(r1)	7 0
	4n+3	One	First	8 bits	4n+3	(r1)	7 0
16 bits	4n	Two	First	8 bits	4n		7 0
			Second	8 bits	4n+1		15 8
	4n+2	Two	First	8 bits	4n+2		7 0
			Second	8 bits	4n+3		15 8
32 bits	4n	Four	First	8 bits	4n		7 0
			Second	8 bits	4n+1		15 8
			Third	8 bits	4n+2		23 16
			Fourth	8 bits	4n+3		31 24

(r1)：连续访问（仅当在HMI突发传输期间通过SDAMOD中的BE=1启用连续访问时。）

Figure 15.9 8位总线空间中的数据对齐，SDRAM区域采用little-endian顺序

数据大小	访问地址	访问次数	巴士循环	数据单位	Address		DQM1 / DQM0 / WE / 数据总线 DQ15 DQ08 DQ07 DQ00
8 bits	4n	One	First	8 bits	4n	(r1)	7 0
	4n+1	One	First	8 bits	4n+1	(r1)	7 0
	4n+2	One	First	8 bits	4n+2	(r1)	7 0
	4n+3	One	First	8 bits	4n+3	(r1)	7 0
16 bits	4n	Two	First	8 bits	4n		15 8
			Second	8 bits	4n+1		7 0
	4n+2	Two	First	8 bits	4n+2		15 8
			Second	8 bits	4n+3		7 0
32 bits	4n	Four	First	8 bits	4n		31 24
			Second	8 bits	4n+1		23 16
			Third	8 bits	4n+2		15 8
			Fourth	8 bits	4n+3		7 0

(r1)：连续访问（仅当在HMI突发传输期间通过SDAMOD中的BE=1启用连续访问时。）

Figure 15.10 8位总线空间中的数据对齐，SDRAM区域的大端顺序

15.5 Operation of CS Area Controller

15.5.1 Separate Bus

This section describes the periods shown in the timing diagrams. The CS area controller (CSC) operates in synchronization with the external bus clock, BCLK. Operation cycles, such as wait cycles, specified in the CSC register, are counted on BCLK. In the following description, the frequencies of BCLK and EBCLK pin output are the same, unless otherwise noted. Access through the external bus starts at the same point as the output of a rising edge on the EBCLK pin. However, if the external bus clock, BCLK, and the output on the EBCLK pin are at different frequencies, the wait settings can cause the start of access for the second and subsequent rounds to coincide with the falling edge of the output on the EBCLK pin. See Figure 15.16 to Figure 15.20. If recovery cycles are inserted for bus access, the setting for the number of recovery cycles can also cause the start of access for the second and subsequent rounds to coincide with the falling edge of the output on the EBCLK pin. See Figure 15.38.

(a) Tw1 to Twn (clock cycles for waiting for a normal read cycle or normal write cycle)

The period from Tw1 to Twn is the number of clock cycles from the start of access through the external bus clock to 1 cycle before the strobe signal is valid. The number of cycles is selectable from 0 to 31. Within this period, the timing of CSn, RD, and WRn assertion (driving the signals low) is determined by the respective wait settings. The wait periods are controlled by the CS Assert Wait Select bits (CSON), the RD Assert Wait Select bits (RDON), the WR Assert Wait Select bits (WRON), and the Write-Data Output Wait Select bits (WDON) in CSn Wait Control Register 2 (CSnWCR2). The number of clock cycles for each of these wait periods is selectable as a value from 0 to 7, counted from the start of external bus access. The selectable number of cycles is also within the overall number of clock cycles required for waiting to read or write.

(b) Tend (clock cycle where the strobe signal is valid)

Tend is the next clock cycle after completion of the wait period for a normal cycle of read or write, or for a cycle of page reading or page writing. If the wait select bit for these cycles is 0, bus access starts on the clock cycle where the strobe signal is valid. The RD and WRn signals are negated in the next clock cycle. For a read access, the clock cycle where the strobe signal is valid is where the data to be read is sampled. If an external wait is enabled, the wait signal is sampled on the cycle where the strobe signal is valid. The bus cycle is extended if the wait signal is low. The bus cycle completes in the next clock cycle if the wait signal is high. Tend indicates the cycle where sampling of the wait signal starts.

After the first cycle where the strobe signal is valid during page access, second and subsequent page access operations (see section (e), Tpw1 to Tpwn (page read cycle wait or page write cycle wait)) start in the next cycle, except during write access with a setting other than 0 for write-data output extension clock cycles (see section (d), Tdw1 to Tdwn (clock cycles for write-data output extension)). If the setting for the RD or WR assertion wait is any value other than 0, the RD and WRn signals are negated in the next clock cycle. If the setting is 0, assertion continues. Additionally, the CSn signal continues to be asserted rather than negated.

(c) Tn1 to Tnm (clock cycles for CS extension)

For normal access, Tn1 to Tnm represent the clock cycles of the period following the cycle where the strobe signal is valid (Tend) up to negation of the CSn signal. For read or write access, the negation timing can be controlled by the read-access CS Extension Cycle Select bits (CSROFF) and the write-access CS Extension Cycle Select bits (CSWOFF) in the CSn Wait Control Register 2 (CSnWCR2). The number of cycles is counted from the cycle following the cycle where the strobe signal is valid.

For page access, Tn1 to Tnm represent the clock cycles of the period following the last cycle where the strobe signal is valid up to negation of the CSn signal.

For write access, setting the Write Data Output Extension Cycle Select bits (WDOFF) controls extension of the period where the address and output data is valid.

(d) Tdw1 to Tdwn (clock cycles for write-data output extension)

For write access, if the wait setting for the write-data output extension is any value other than 0, the specified clock cycles are inserted from the cycle following the cycle where the strobe signal is valid (Tend).

For normal access, this period is inserted within the clock cycle period for CS extension (Tn1 to Tnm).

For page access, this period is inserted within the clock cycle period where the strobe signal is valid and subsequent page accesses, or within the clock cycle period for the CS extension (Tn1 to Tnm). Valid address and data output are extended

15.5 CS区域控制器的操作

15.5.1 独立巴士

本节介绍时序图中显示的周期。CS区域控制器(CSC)与外部总线时钟BCLK同步运行。在CSC寄存器中指定的操作周期（例如等待周期）在BCLK上计数。在以下描述中，BCLK和EBCLK引脚输出的频率是相同的，除非另有说明。通过外部总线的访问与EBCLK引脚上的上升沿输出在同一点开始。但是，如果外部总线时钟、BCLK和EBCLK引脚上的输出频率不同，则等待设置可能会导致第二轮和后续轮次的访问开始与EBCLK引脚上输出的下降沿重合.请参见图15.16至图15.20。如果为总线访问插入恢复周期，则恢复周期数的设置也会导致第二轮和后续轮次的访问开始与EBCLK引脚输出的下降沿一致。请参见图15.38。

(a) Tw1到Twn（等待正常读周期或正常写周期的时钟周期）

从Tw1到Twn的周期是从通过外部总线时钟开始访问到选通信号有效之前的1个周期的时钟周期数。周期数可在0到31之间选择。在此周期内，CSn、RD和WRn断言的时序（将信号驱动为低电平）由各自的等待设置确定。等待周期由CSn中的CS断言等待选择位(CSON)、RD断言等待选择位(RDON)、WR断言等待选择位(WRON)和写数据输出等待选择位(WDON)控制等待控制寄存器2(CSnWCR2)。每个等待周期的时钟周期数可选择从0到7的值，从外部总线访问开始计数。可选择的周期数也在等待读取或写入所需的时钟周期总数之内。

(b) Tend（选通信号有效的时钟周期）

Tend是完成正常读取或写入周期或页面读取或页面写入周期的等待周期后的下一个时钟周期。如果这些周期的等待选择位为0，则总线访问在选通信号有效的时钟周期开始。RD和WRn信号在下一个时钟周期被否定。对于读访问，选通信号有效的时钟周期是对要读取的数据进行采样的地方。如果启用了外部等待，则在选通信号有效的周期对等待信号进行采样。如果等待信号为低，则延长总线周期。如果等待信号为高电平，则总线周期在下一个时钟周期完成。Tend表示等待信号采样开始的周期。

在页面访问期间选通信号有效的第一个周期之后，第二个和随后的页面访问操作（参见(e)节，Tpw1到Tpwn（页面读取周期等待或页面写入周期等待））在下一个周期开始，除了在写入数据输出扩展时钟周期设置为0以外的写入访问（参见(d)节，Tdw1到Tdwn（写入数据输出扩展的时钟周期））。如果RD或WR断言等待的设置为0以外的任何值，则RD和WRn信号在下一个时钟周期被否定。如果设置为0，则断言继续。此外，CSn信号继续被断言而不是被否定。

(c) Tn1到Tnm（CS扩展的时钟周期）

对于正常访问，Tn1到Tnm表示从选通信号有效(Tend)到CSn信号无效的周期之后的周期的时钟周期。对于读或写访问，取反时序可由CSn等待控制寄存器2(CSnWCR2)中的读访问CS扩展周期选择位(CSROFF)和写访问CS扩展周期选择位(CSWOFF)控制。周期数从选通信号有效的周期之后的周期开始计数。

对于页访问，Tn1到Tnm表示从选通信号有效直到CSn信号取反的最后一个周期之后的周期的时钟周期。

对于写访问，设置写数据输出延长周期选择位(WDOFF)控制地址和输出数据有效期间的延长。

(d) Tdw1到Tdwn（写数据输出扩展的时钟周期）

对于写访问，如果写数据输出扩展的等待设置为0以外的任何值，则从选通信号有效(Tend)周期的下一个周期插入指定的时钟周期。

对于正常访问，该周期插入到CS扩展的时钟周期周期内（Tn1到Tnm）。

对于页面访问，该周期插入在选通信号有效和后续页面访问的时钟周期周期内，或者在CS扩展（Tn1到Tnm）的时钟周期周期内。有效地址和数据输出扩展

over this period, and the WRn signal is negated.

(e) Tpw1 to Tpwn (page read cycle wait or page write cycle wait)

For the second and subsequent bus cycles during page access, the values for a page read cycle wait or page write cycle wait are used instead of the settings for a normal read or write cycle wait. The settings in the WR Assert Wait Select bits become enabled in the same way as for the first access. The RD assertion control operation depends on the page read access mode setting (the PRMOD bit in CSnMOD) as follows:

- CSnMOD.PRMOD = 0: A wait for RD assertion is inserted in the same way as for the first access, and the RD signal is negated
- CSnMOD.PRMOD = 1: Although a wait for RD assertion is inserted in the same way as for normal-access compatibility mode, the RD signal continues to be asserted over this period.

(f) Tr1 to Trn (recovery cycles)

Recovery cycles can be inserted from the point where a bus cycle is complete (CSn signal negation). The number of recovery cycles can be controlled by setting the Read Recovery (RRCV) or Write Recovery (WRCV) bits in the CSn Recovery Cycle Register (CSnREC). Both numbers of recovery cycles are counted from the end of a bus cycle (CSn negation) and can be selected from 0 to 15 cycles. For more information, see section 15.5.4, Insertion of Recovery Cycles.

(1) Normal access

When the PRENB and PWENB bits in CSnMOD are set to 0 to disable page read and page write access, all bus accesses take the form of normal read and write operations. Even when these bits are set to 1 to enable page read and page write access, bus access other than page access takes the form of normal read and write operations. Figure 15.11 to Figure 15.13 show the normal access operations.

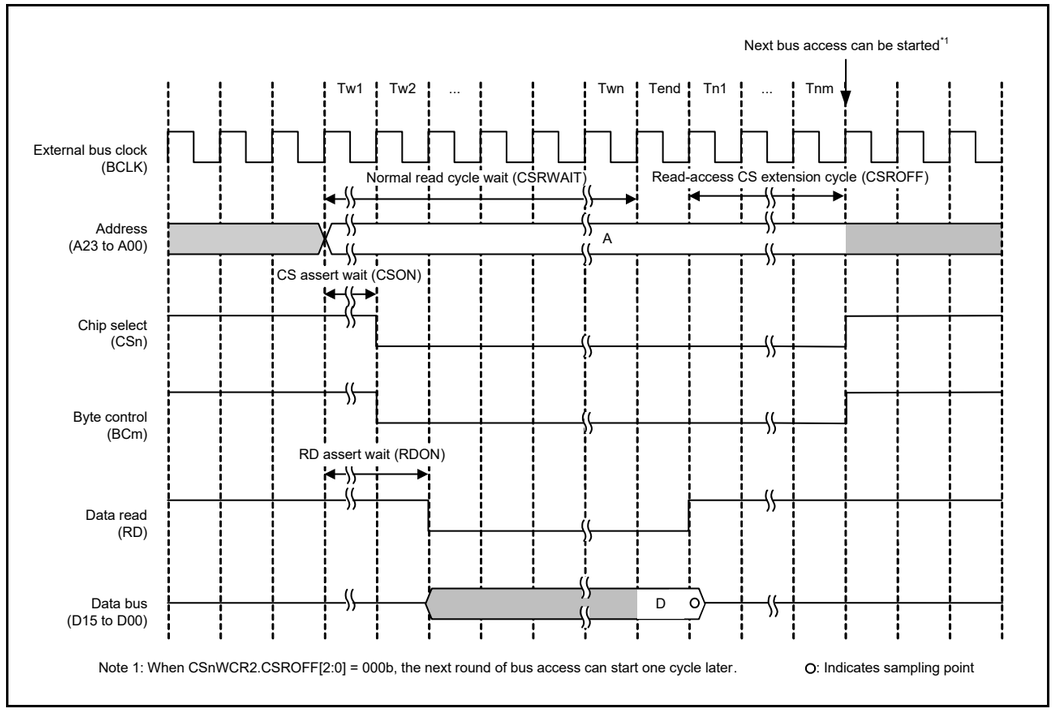


Figure 15.11 Bus timing for normal read operation (n = 0 to 7, m = 0, 1)

在此期间，WRn信号被否定。

(e) Tpw1到Tpwn（页面读取周期等待或页面写入周期等待）

对于页面访问期间的第二个和后续总线周期，使用页面读取周期等待或页面写入周期等待的值，而不是正常读取或写入周期等待的设置。WRAssertWaitSelect位中的设置以与第一次访问相同的方式启用。RD断言控制操作取决于页面读取访问模式设置（CSnMOD中的PRMOD位），如下所示：

- CSnMOD.PRMOD=0：以与第一次访问相同的方式插入等待RD断言，并且RD信号被取反
- CSnMOD.PRMOD=1：虽然以与正常访问兼容模式相同的方式插入等待RD断言，但在此期间继续断言RD信号。

(f) Tr1 to Trn (recovery cycles)

恢复周期可以从总线周期完成的点插入（CSn信号否定）。可以通过设置CSn恢复周期寄存器(CSnREC)中的读取恢复(RRCV)或写入恢复(WRCV)位来控制恢复周期的数量。两个恢复周期数都是从总线周期结束（CSn否定）开始计算的，可以从0到15个周期中选择。有关详细信息，请参阅第15.5.4节，恢复周期的插入。

(1) 正常访问

当CSnMOD中的PRENB和PWENB位设置为0以禁用页面读取和页面写入访问时，所有总线访问都采用正常读写操作的形式。即使将这些位设置为1以启用页面读取和页面写入访问，页面访问以外的总线访问仍采用正常读取和写入操作的形式。图15.11至图15.13显示了正常的访问操作。

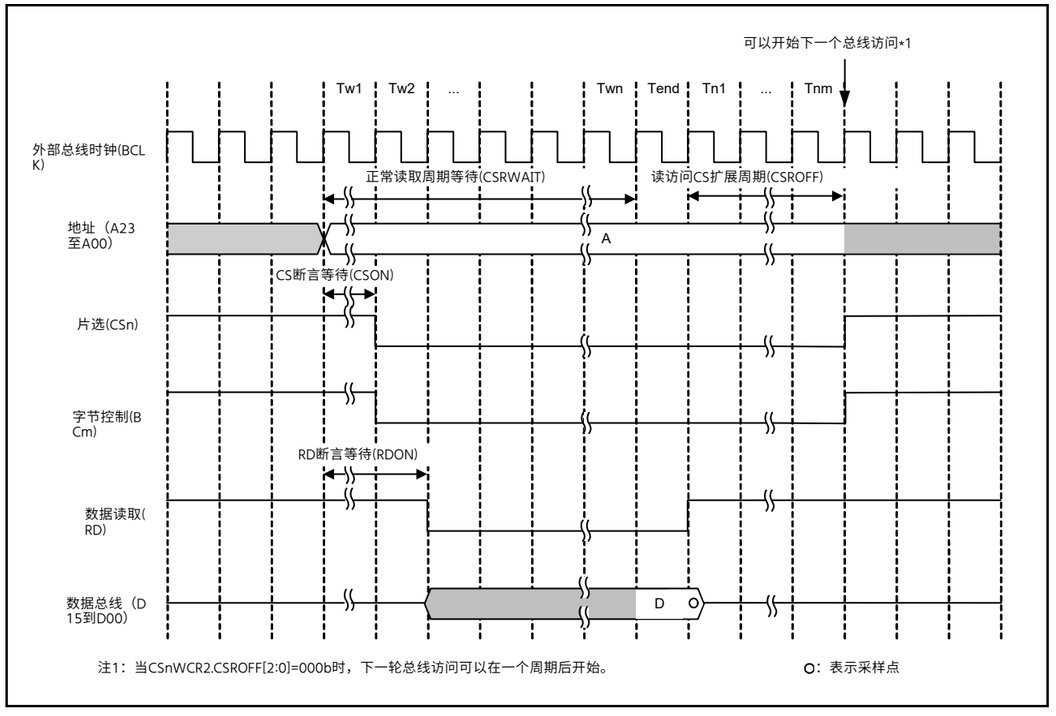


Figure 15.11 正常读取操作的总线时序（n=0到7，m=0、1）

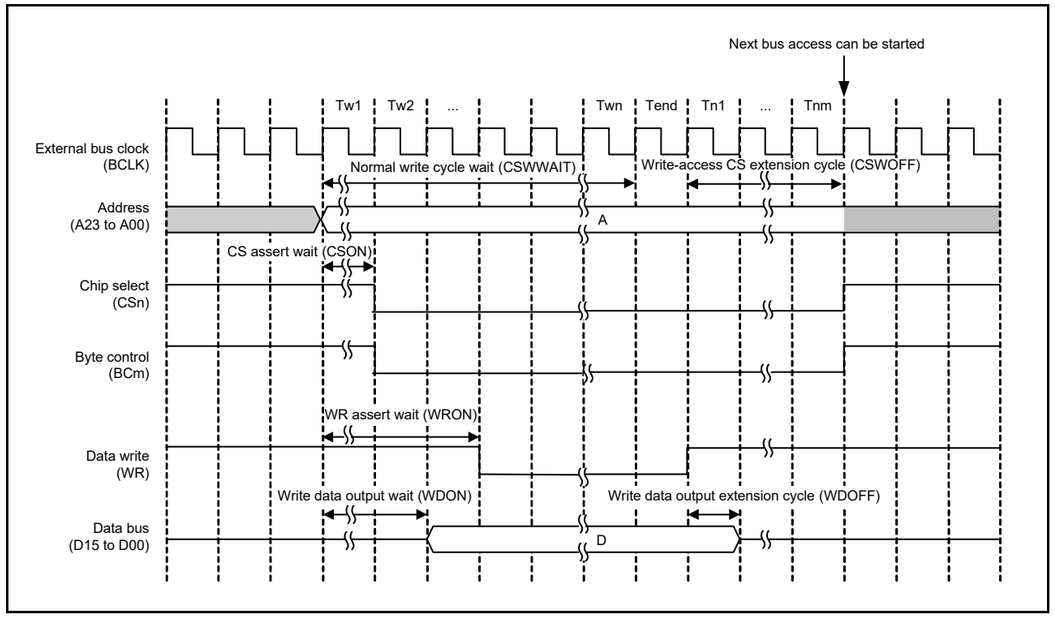


Figure 15.12 Bus timing for normal write operation in single-write strobe mode (n = 0 to 7, m = 0, 1)

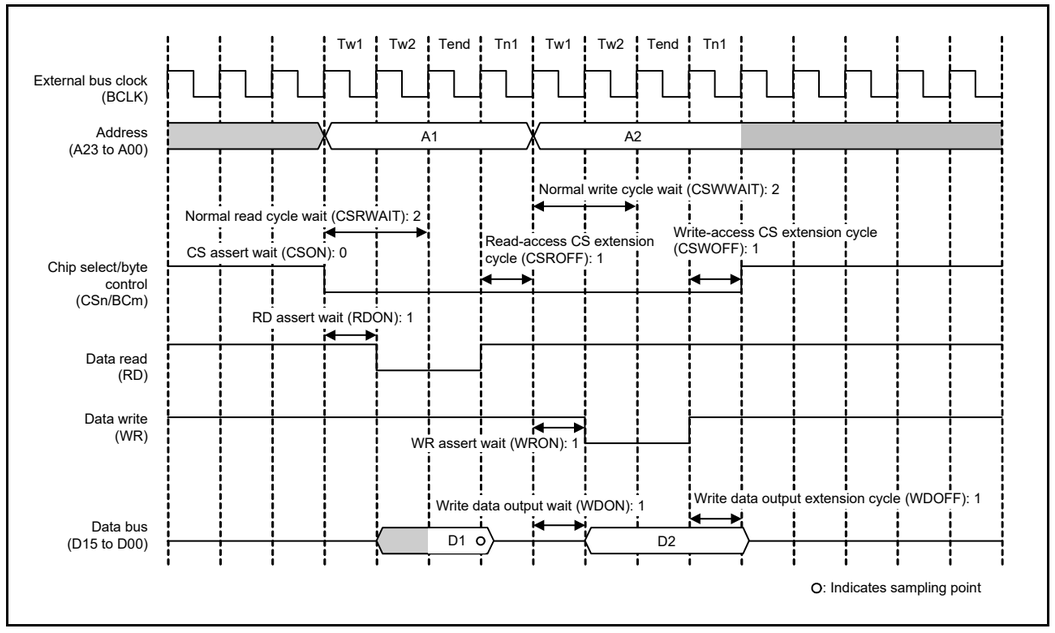


Figure 15.13 Example of normal access operation for read and write (n = 0 to 7, m = 0, 1)

When two or more rounds of external bus access are required in response to a single request for transfer from a bus master, normal access operations are repeated. See section (a), Tw1 to Twn (clock cycles for waiting for a normal read cycle or normal write cycle) to section (d), Tdw1 to Tdwn (clock cycles for write-data output extension). Figure 15.14 and Figure 15.15 show examples of operations when two rounds of bus access are generated in response to a single transfer request. If the recovery cycle insertion condition is satisfied, recovery cycles (section (f), Tr1 to Trn (recovery

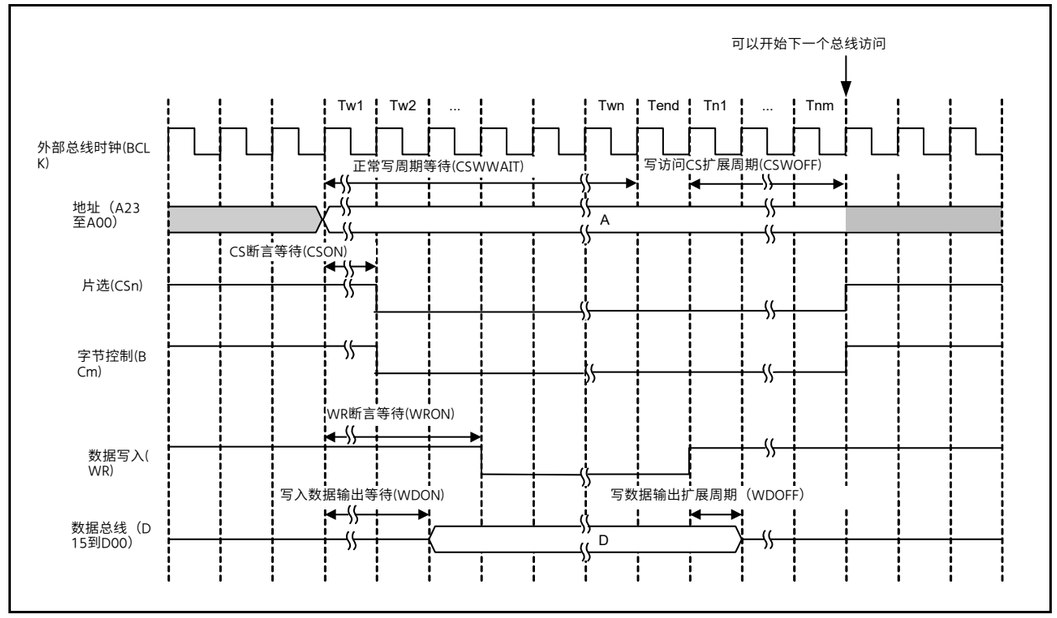


Figure 15.12 单次写入选通模式下正常写入操作的总线时序（n=0到7，m=0、1）

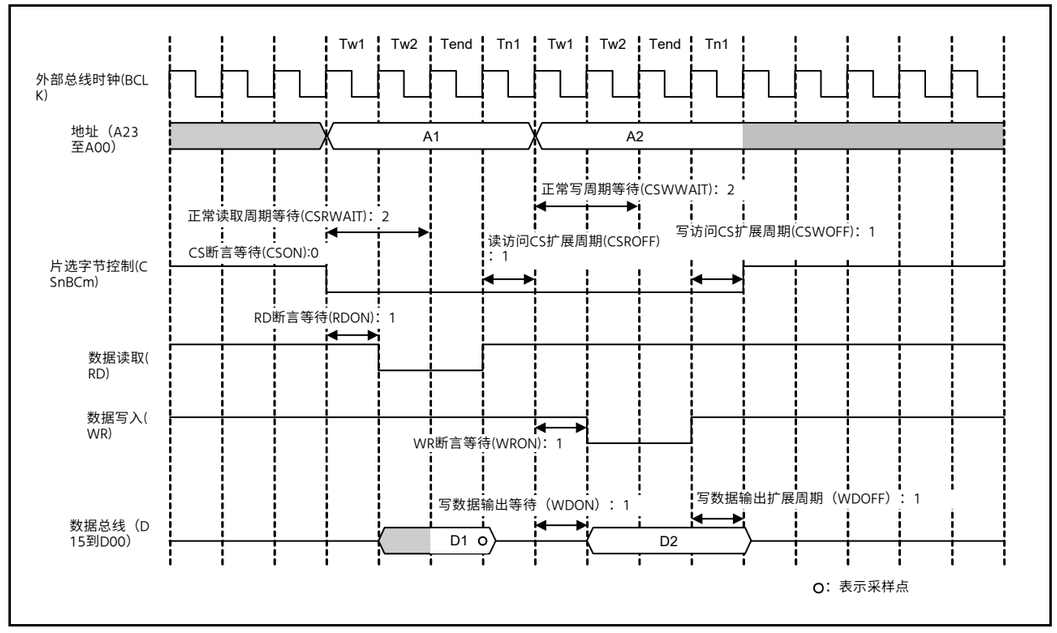


Figure 15.13 读写的正常访问操作示例（n=0到7，m=0 1）

当响应来自总线主机的单个传输请求需要两轮或多轮外部总线访问时，重复正常访问操作。参见(a)部分，Tw1到Twn（等待正常读周期或正常写周期的时钟周期）到(d)部分，Tdw1到Tdwn（写数据输出扩展的时钟周期）。图15.14和图15.15显示了为响应单个传输请求而生成两轮总线访问时的操作示例。如果恢复循环插入条件满足，恢复循环（部分（f），Tr1到Trn（恢复

cycles)) are also inserted in the second and subsequent external bus accesses. See Figure 15.36.

The values in the wait control registers shown in the figures are example settings. In your application, set the registers appropriately for the specifications of connected devices.

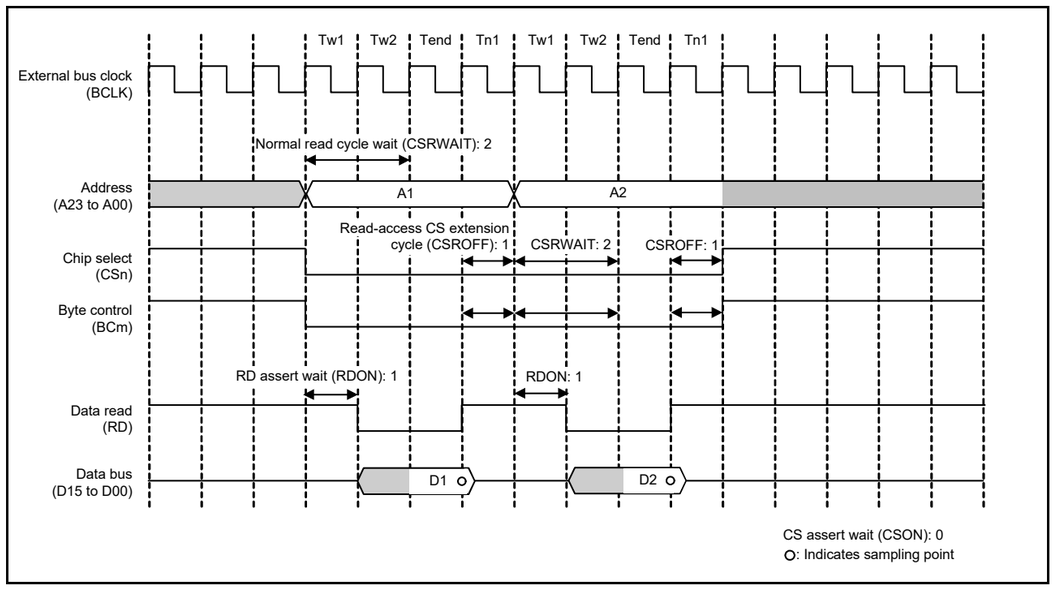


Figure 15.14 Example of normal read operation when two rounds of bus access are generated in response to a single transfer request (n = 0 to 7, m = 0, 1)

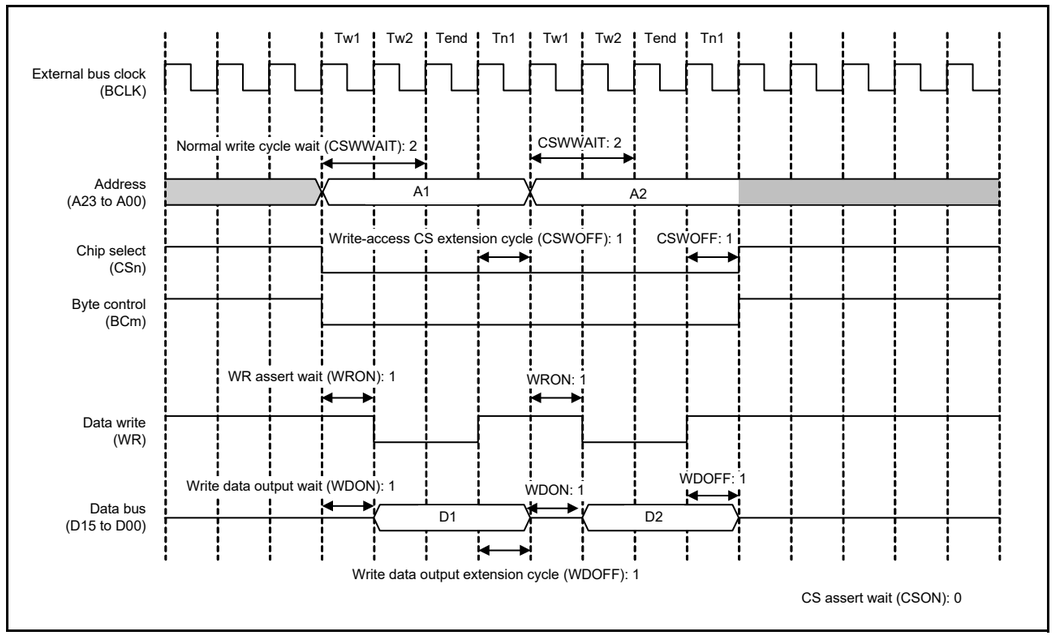


Figure 15.15 Example of normal write operation when two rounds of bus access are generated in response to a single transfer request in single-write strobe mode (n = 0 to 7, m = 0, 1)

周期））也被插入到第二次和随后的外部总线访问中。请参见图15.36。

图中显示的等待控制寄存器中的值是示例设置。在您的应用程序中，根据连接设备的规格适当设置寄存器。

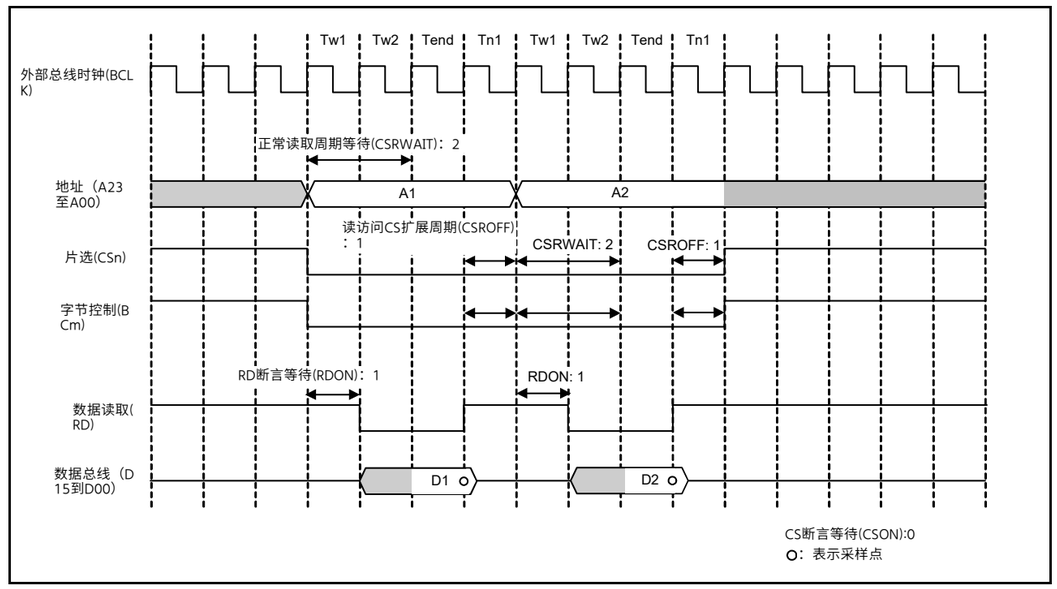


Figure 15.14 为响应单个传输请求（n=0到7，m=0 1）生成两轮总线访问时的正常读取操作示例

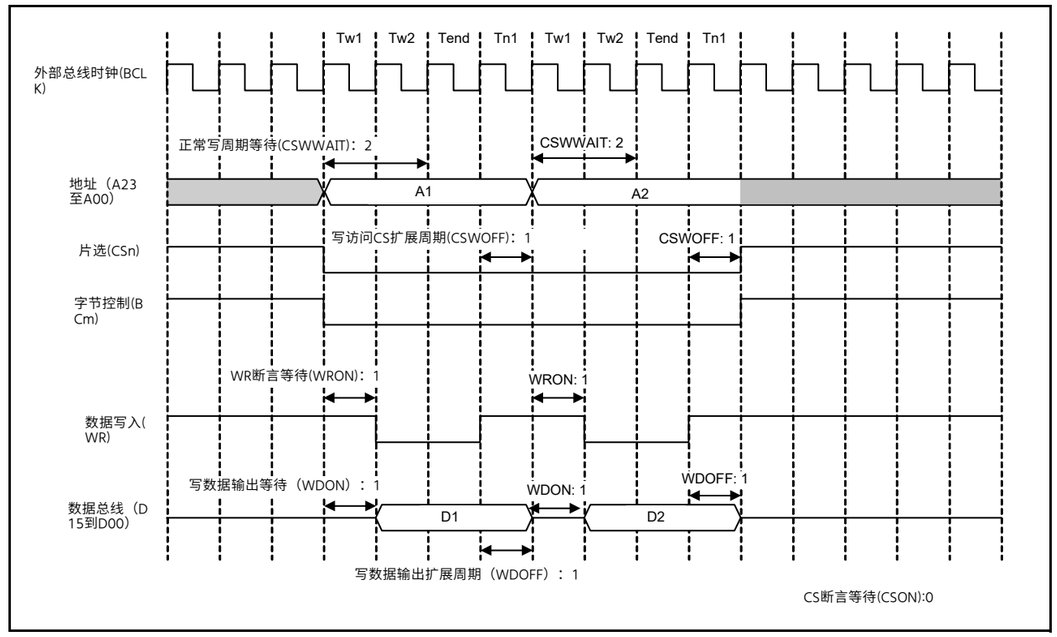


Figure 15.15 在单写选通模式（n=0到7，m=0 1）下响应单次传输请求而生成两轮总线访问时的正常写操作示例

Figure 15.16 to Figure 15.20 show examples of normal accesses made when BCLK/2 is selected as the frequency division in the EBCLK Pin Output Select bit.

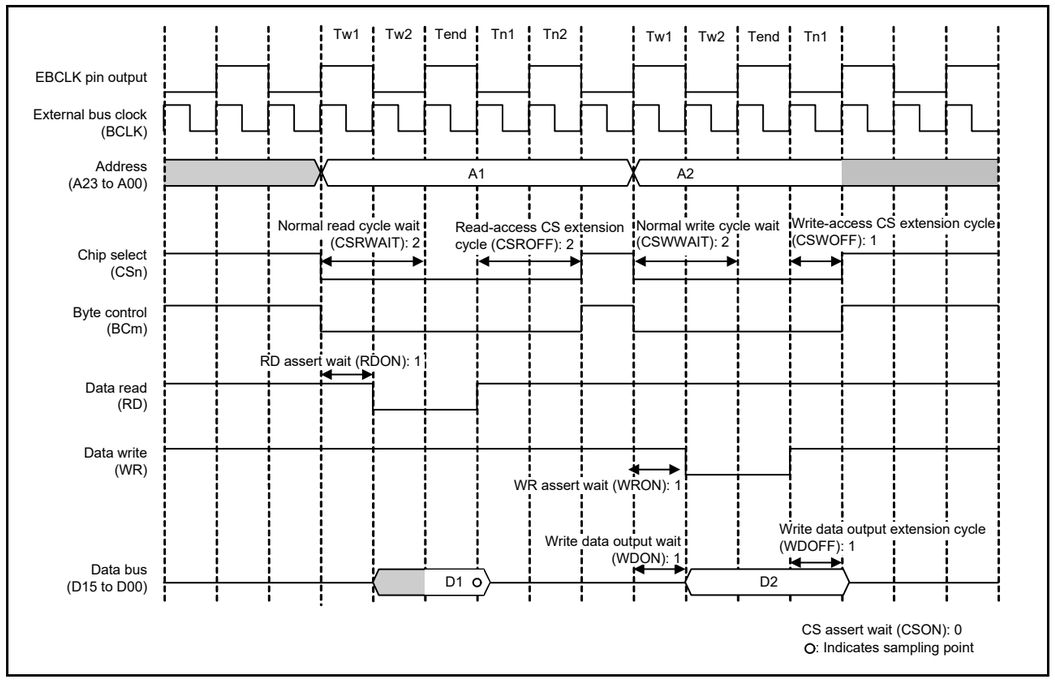


Figure 15.16 Example of normal access when BCLK/2 is selected in the EBCLK Pin Output Select bit (n = 0 to 7, m = 0, 1)

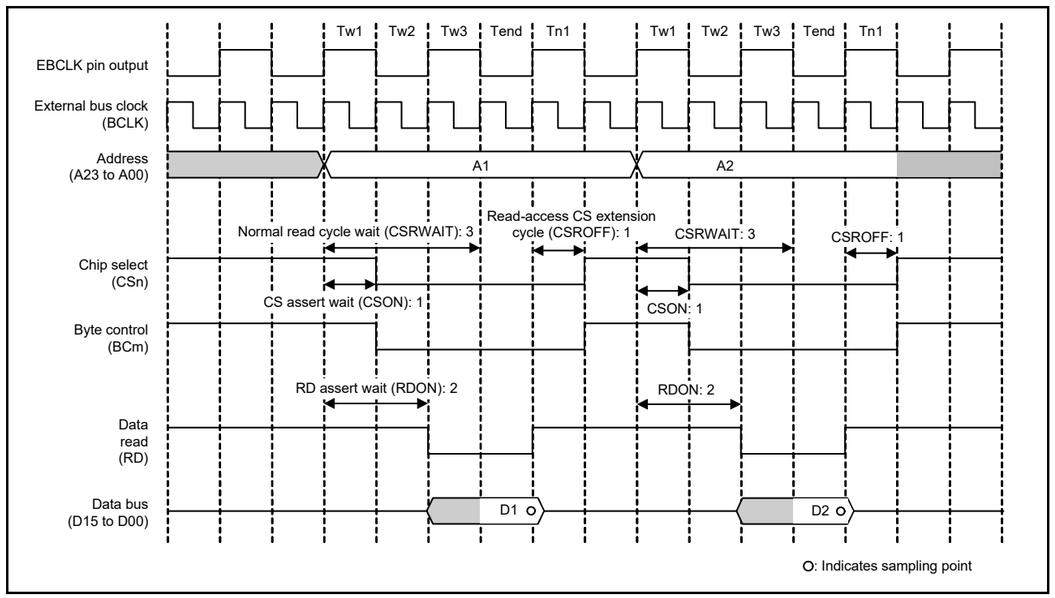


Figure 15.17 Example of normal read operation when BCLK/2 is selected in the EBCLK Pin Output Select bit (n = 0 to 7, m = 0, 1)

图15.16至图15.20显示了在EBCLK引脚输出选择位中选择BCLK2作为分频时进行的正常访问示例。

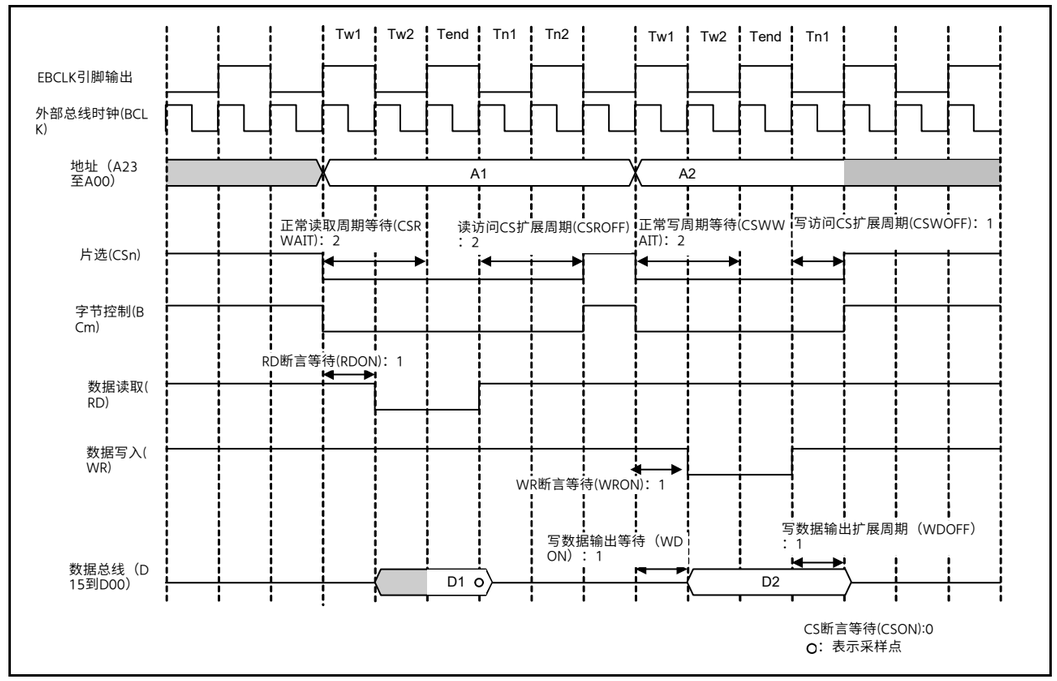


Figure 15.16 在EBCLK引脚输出选择位（n=0至7，m=0、1）中选择BCLK2时的正常访问示例

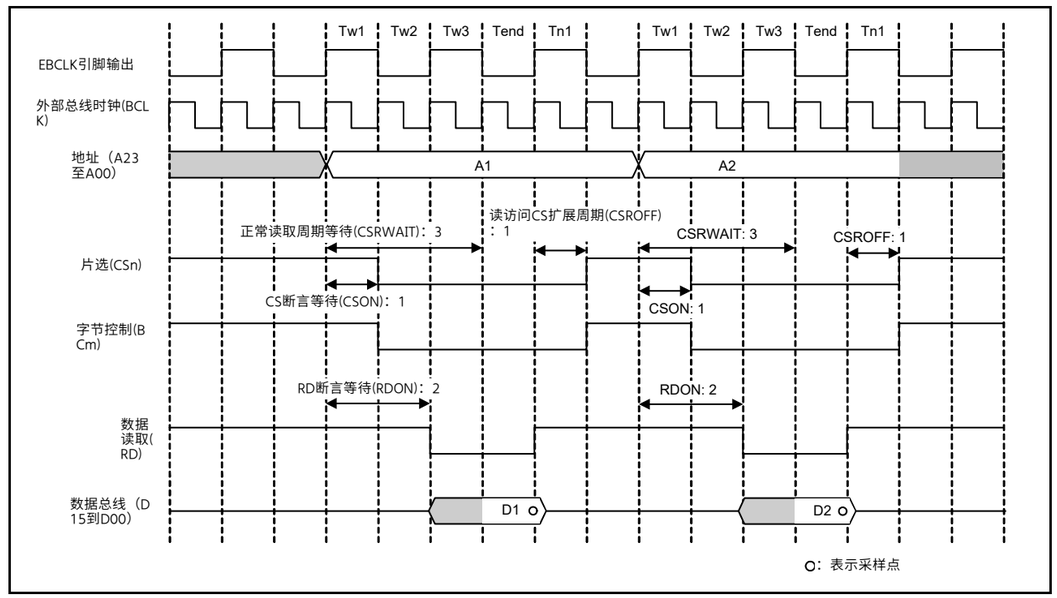


Figure 15.17 在EBCLK引脚输出选择位（n=0至7，m=0、1）中选择BCLK2时的正常读取操作示例

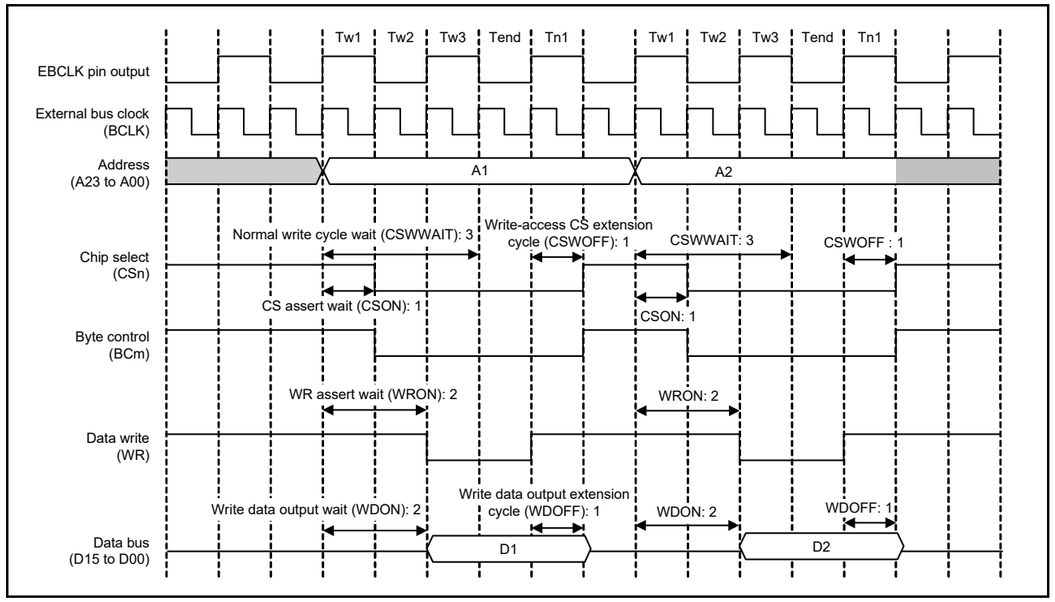


Figure 15.18 Example of normal write operation when BCLK/2 is selected in the EBCLK Pin Output Select bit (n = 0 to 7, m = 0, 1)

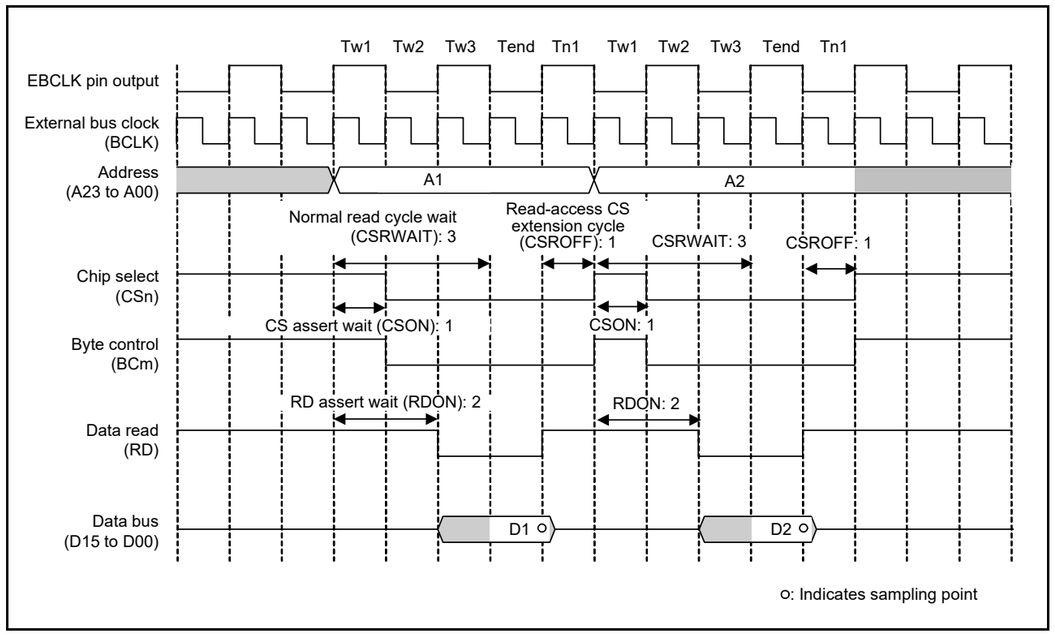


Figure 15.19 Example of normal read operation when BCLK/2 is selected in the EBCLK Pin Output Select bit and two rounds of bus access are generated in response to a single transfer request (n = 0 to 7, m = 0, 1)

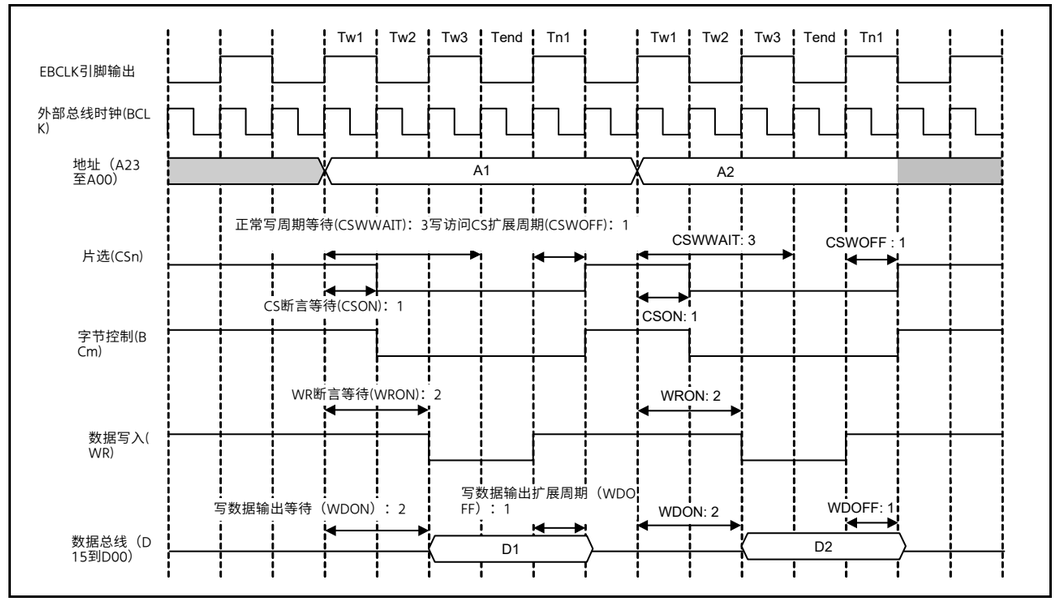


Figure 15.18 在EBCLK引脚输出选择位（n=0至7，m=0、1）中选择BCLK2时的正常写操作示例

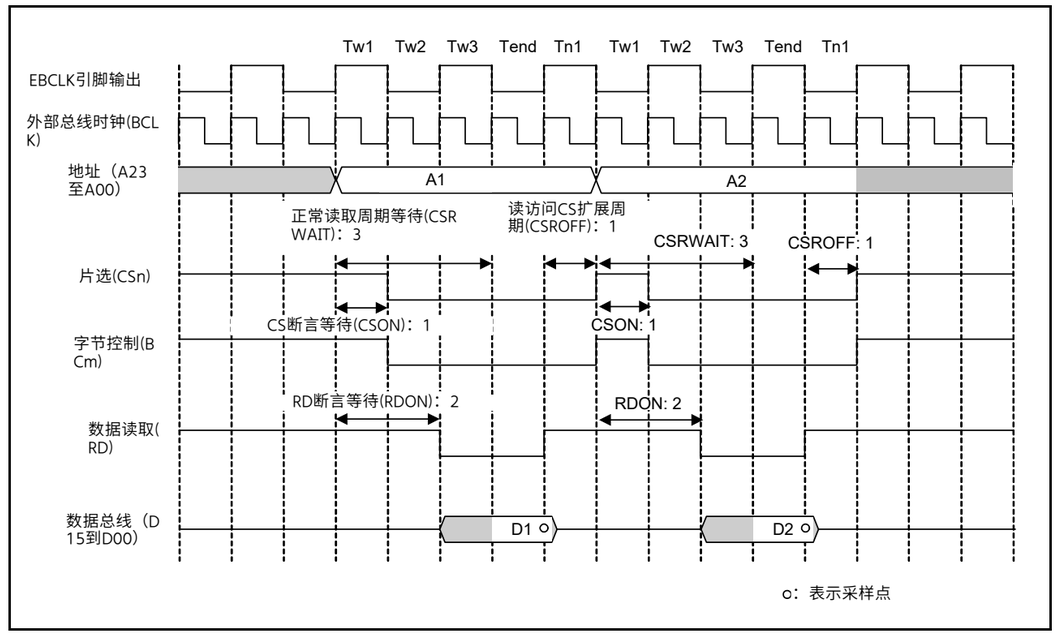


Figure 15.19 当在EBCLK引脚输出选择位中选择BCLK2并且响应单个传输请求（n=0到7，m=0、1）产生两轮总线访问时的正常读取操作示例

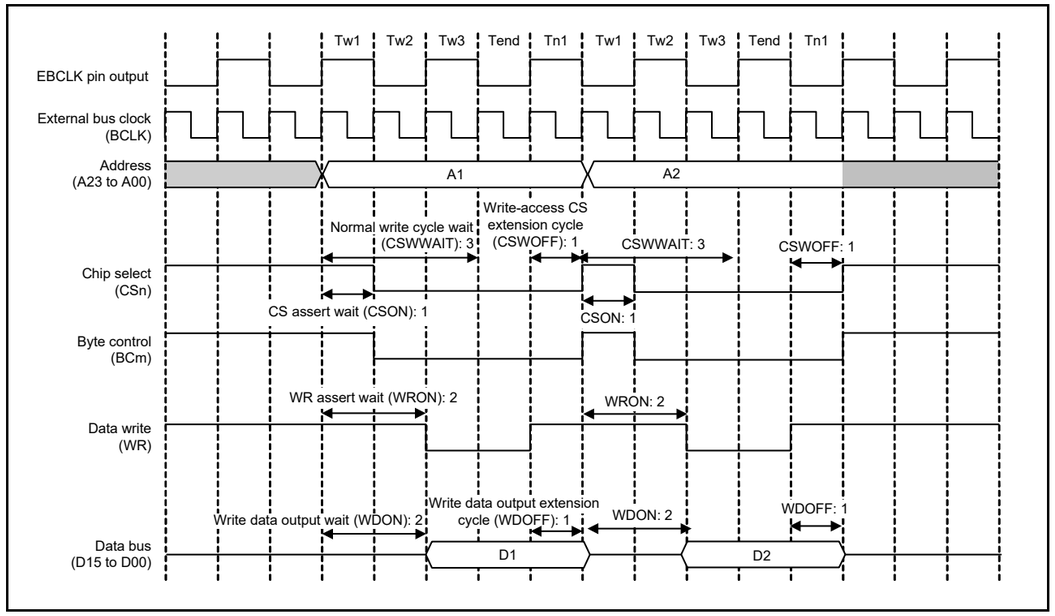


Figure 15.20 Example of normal write operation when BCLK/2 is selected in the EBCLK Pin Output Select bit and two rounds of bus access are generated in response to a single transfer request (n = 0 to 7, m = 0, 1)

(2) Page access

When the PRENB and PWENB bits in CSnMOD are set to 1 to enable page read and page write access, the bus access for page access operations becomes page reading and writing. Page access can only occur when two or more rounds of external bus access are required for a single transfer request from the bus master. However, normal access is made when split accesses are not aligned or access extends across the 32-bit boundary. See Figure 15.3 to Figure 15.6 for the conditions under which page access occurs.

Figure 15.21 and Figure 15.22 show examples of page access operations.

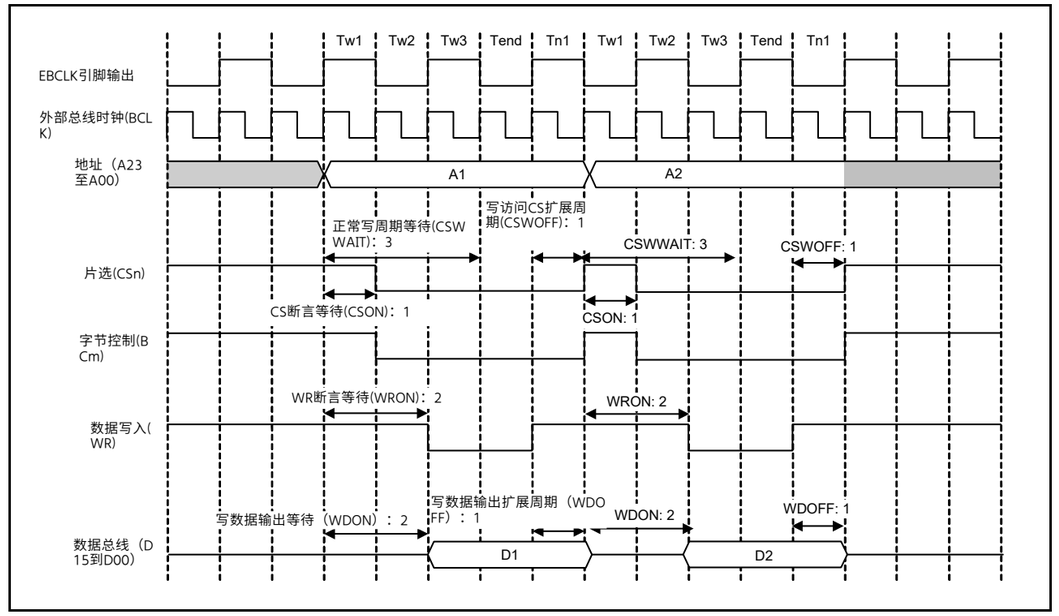


Figure 15.20 当在EBCLK引脚输出选择位中选择BCLK2并且响应单个传输请求（n=0到7，m=0、1）产生两轮总线访问时的正常写操作示例

(2) 页面访问

当CSnMOD中的PRENB和PWENB位设置为1以启用页面读取和页面写入访问时，页面访问操作的总线访问变为页面读取和写入。只有当来自总线主机的单个传输请求需要两轮或多轮外部总线访问时，才会发生页面访问。但是，当拆分访问未对齐或访问超出32位边界时，将进行正常访问。有关页面访问发生的条件，请参见图15.3至图15.6。

图15.21和图15.22显示了页面访问操作的示例。

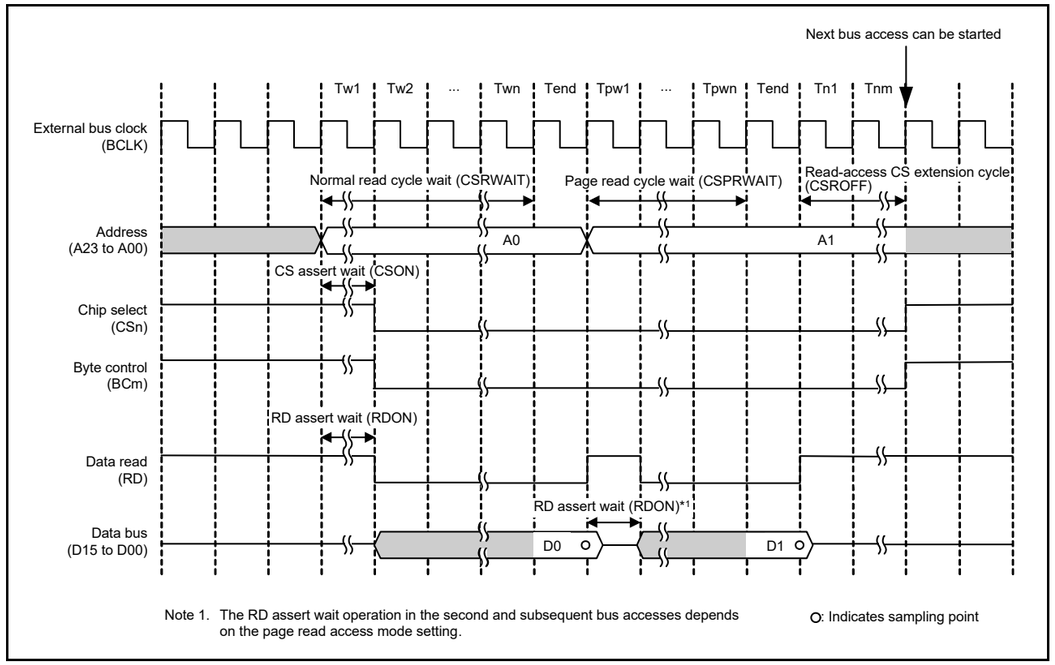


Figure 15.21 Page read access timing (n = 0 to 7, m = 0, 1)

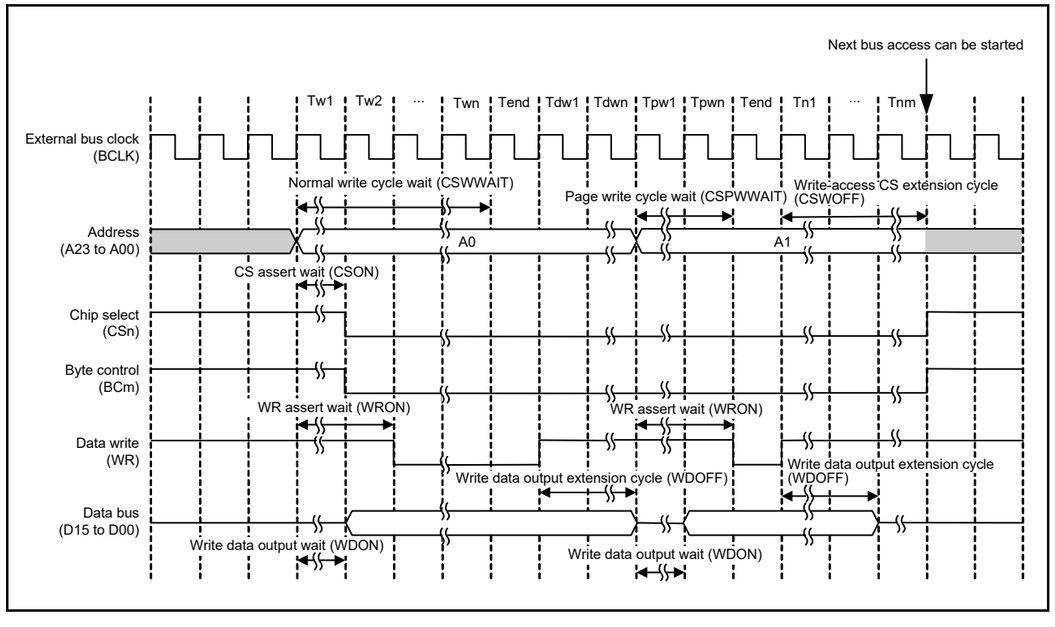


Figure 15.22 Page write access timing (n = 0 to 7, m = 0, 1)

Figure 15.23 and Figure 15.24 show examples of operations for access to a 16-bit bus space in 32 bits. The values of the wait control registers shown in the figures are example settings. In your application, set the registers appropriately for the specifications of connected devices.

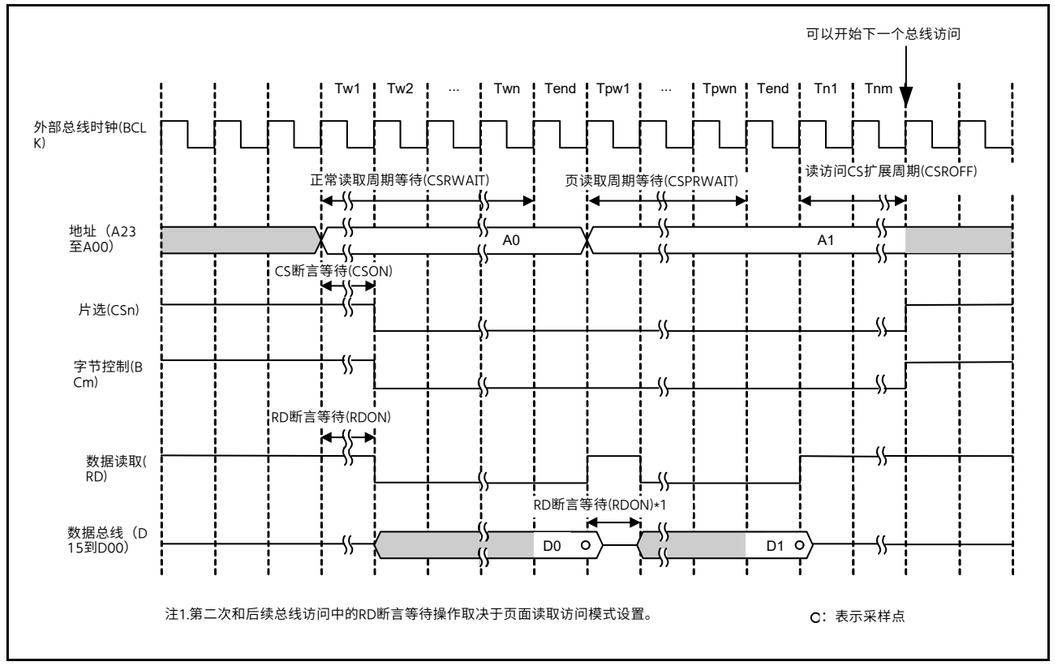


Figure 15.21 页读取访问时序（n=0到7，m=0、1）

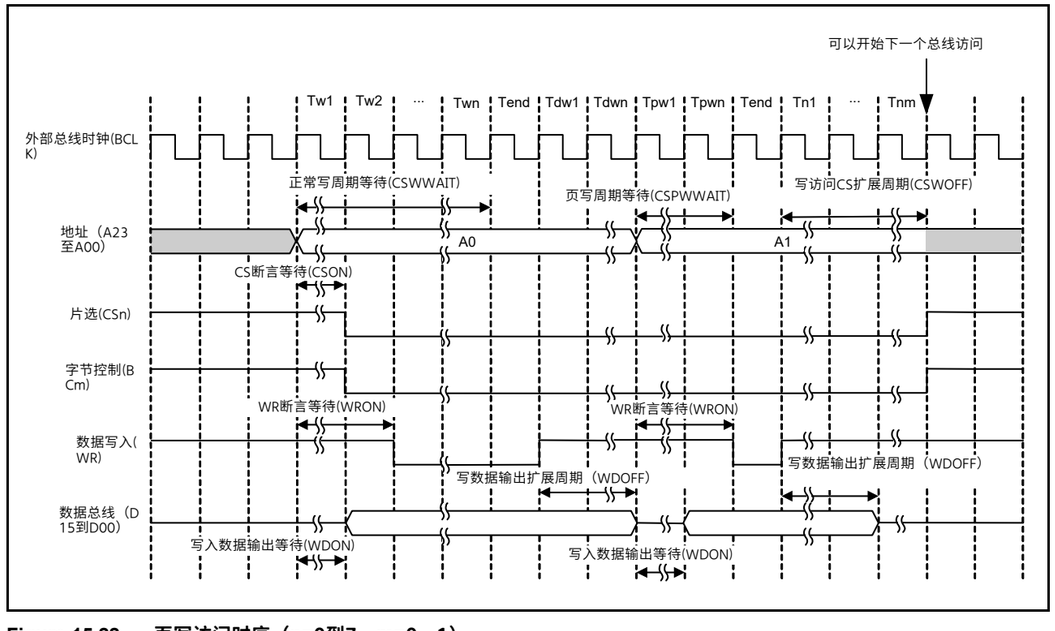


Figure 15.22 页写访问时序（n=0到7，m=0、1）

图15.23和图15.24显示了以32位访问16位总线空间的操作示例。图中所示的等待控制寄存器的值是示例设置。在您的应用程序中，根据连接设备的规格适当设置寄存器。

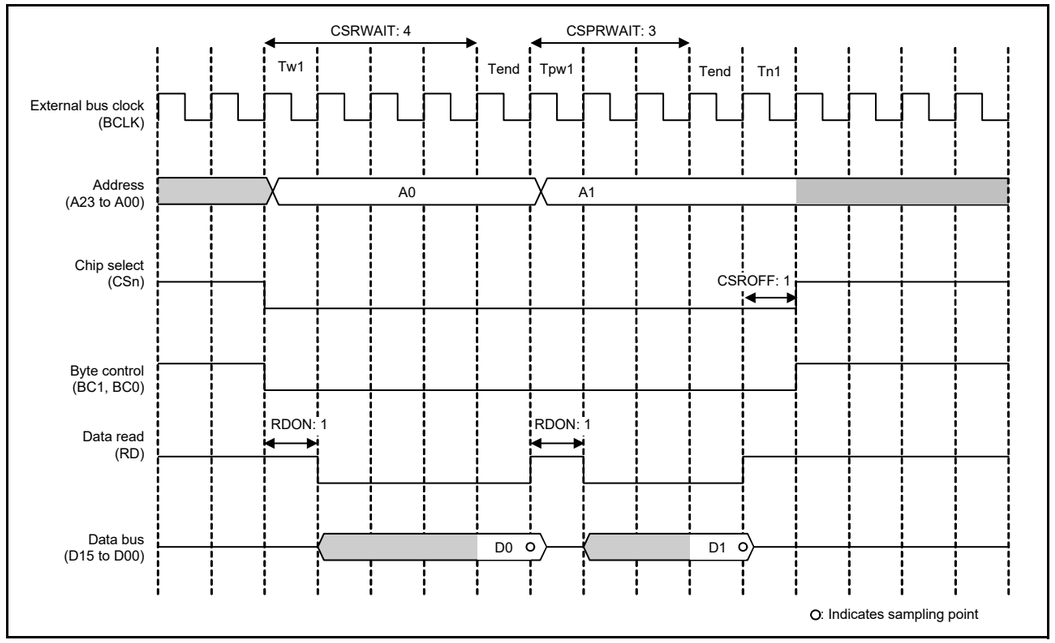


Figure 15.23 Example page read access operation when 16-bit bus space is accessed in 32 bits (n = 0 to 7)

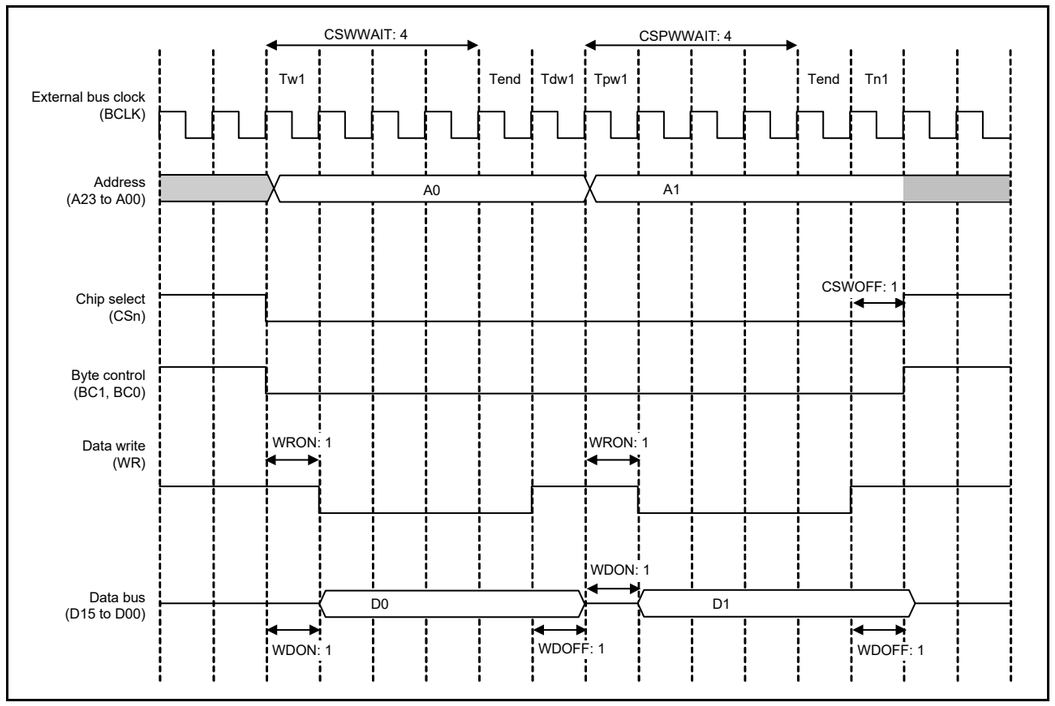


Figure 15.24 Example page write access operation when 16-bit bus space is accessed in 32 bits in single-write strobe mode (n = 0 to 7)

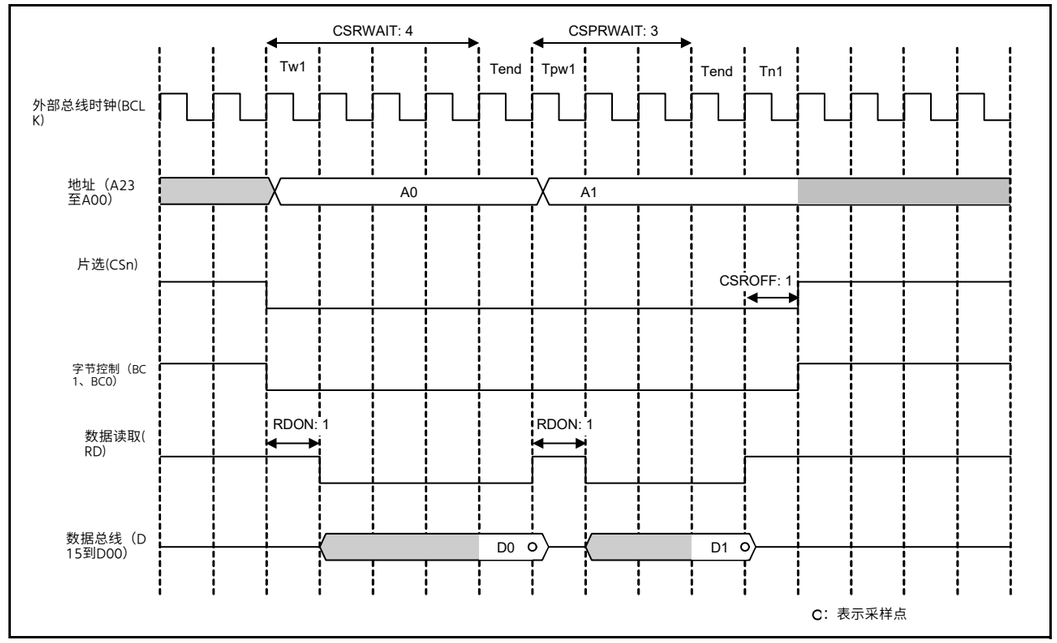


Figure 15.23 以32位（n=0到7）访问16位总线空间时的页读取访问操作示例

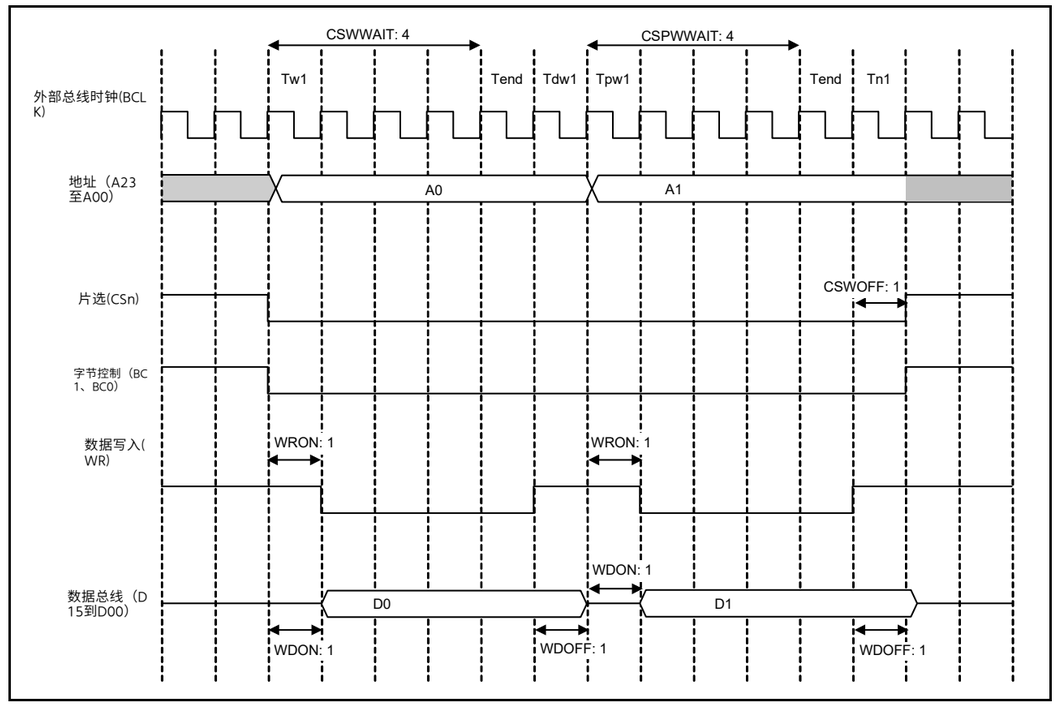


Figure 15.24 在单写选通模式（n=0到7）下以32位访问16位总线空间时的页写访问操作示例

Figure 15.25 and Figure 15.26 show examples of page access operations when BCLK/2 is selected as the frequency division in the EBCLK Pin Output Select bit.

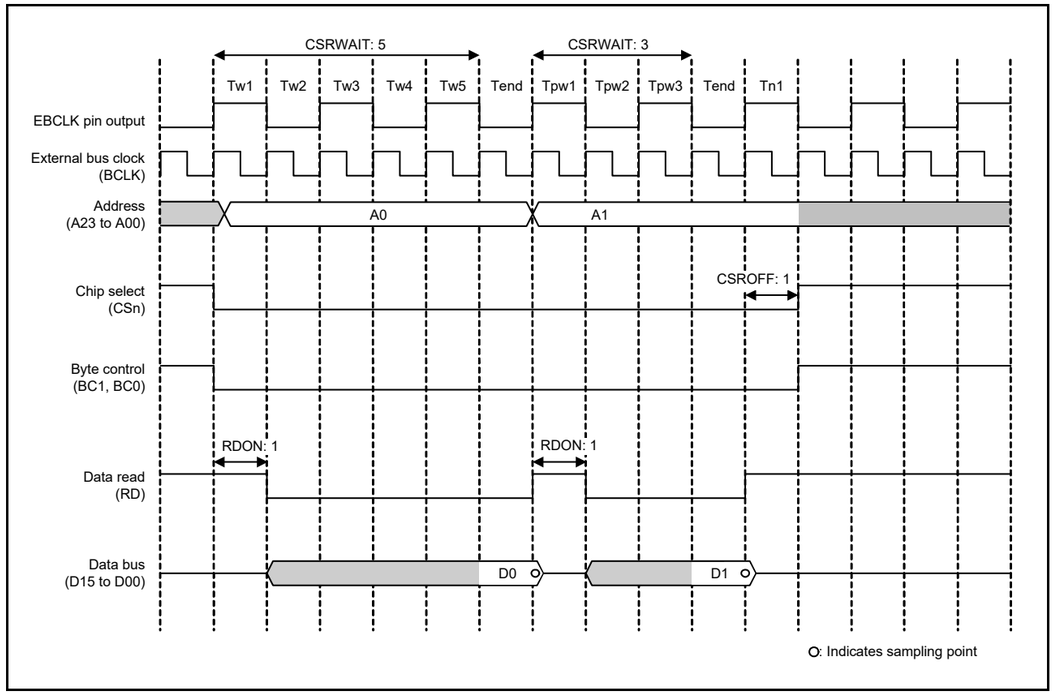


Figure 15.25 Example page read access operation when BCLK/2 is selected in the EBCLK Pin Output Select bit and two rounds of bus access are generated in response to a single transfer request (n = 0 to 7)

图15.25和图15.26显示了在EBCLK引脚输出选择位中选择BCLK2作为分频时的页面访问操作示例。

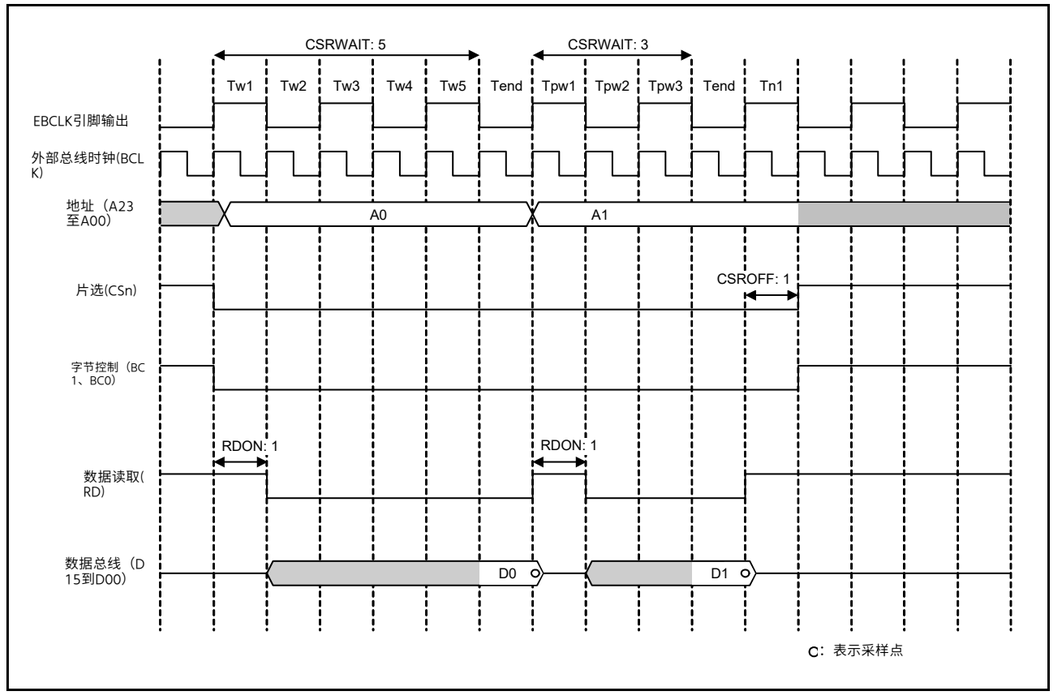


Figure 15.25 在EBCLK引脚输出选择位中选择BCLK2并且响应单个传输请求（n=0到7）生成两轮总线访问时的示例页面读取访问操作

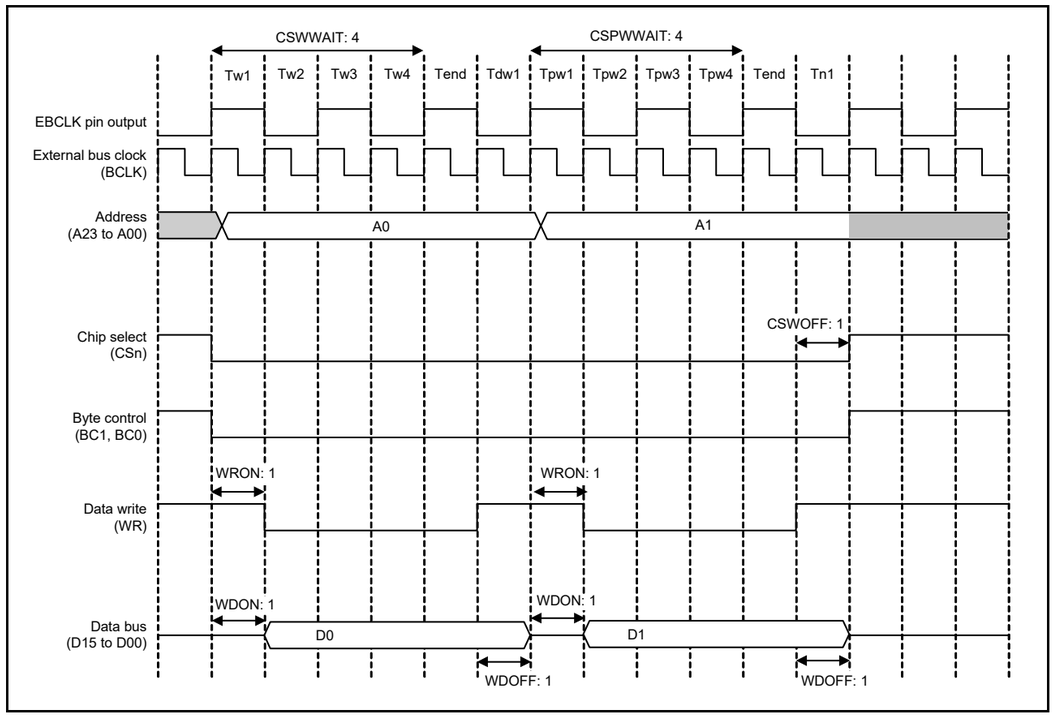


Figure 15.26 Example page write access operation when BCLK/2 is selected in the EBCLK Pin Output Select bit and two rounds of bus access are generated in response to a single transfer request, in single-write strobe mode (n = 0 to 7)

15.5.2 Address/Data Multiplexed Bus

When the address/data Multiplexed I/O Interface Select bit (MPXEN) in CSnCR is set to 1, addresses and data can be multiplexing input/output to/from the D15 to D00 pins in the corresponding area. Using this function enables direct connection of this LSI to peripheral LSIs requiring address/data multiplexing. When 8-bit width is selected with the BSIZE[1:0] bits in CSnCR, D7 to D00 are multiplexed with A07 to A00. When 16-bit width is selected, D15 to D00 are multiplexed with A15 to A00. In the address/data multiplexed I/O space, accesses are controlled with the ALE, RD, WRn, and BCn signals.

Byte strobe mode or single-write strobe mode is selectable in the same way as for a separate bus. However, with regard to the BCn signals within the address cycle, the byte-control signal is output for the data being read or written.

During the address/data multiplexed I/O space access, after the number of wait cycles specified by the address cycle wait select bits (AWAIT[1:0]) in CSnWCR2 is inserted in the address output cycle, data access is performed.

Ta1 to Tan (Address Cycle Wait)
The period Ta1 to Tan is valid only when the address/data multiplexed I/O space is specified. This period is made up of the number of clock cycles between the start of external bus access and 1 cycle before the address latch (ALE) signal is negated. The number of cycles are selectable within the range from zero to three. Addresses are output until the next cycle of ALE signal negation (address cycle). The timing of ALE signal is the same as that of CS assertion. After the address cycle, a data cycle is started. CSnWCR1 and CSnWCR2 should be set so that an address cycle and a data cycle do not overlap.

Page access to the address/data multiplexed I/O space is invalid. When the PRENB or PWENB bit in CSnMOD is set to 1 to enable page-read or page-write access, these settings are ignored and normal read or write operation is performed.

Figure 15.27 to Figure 15.29 show examples of operations with the address/data multiplexed I/O interface

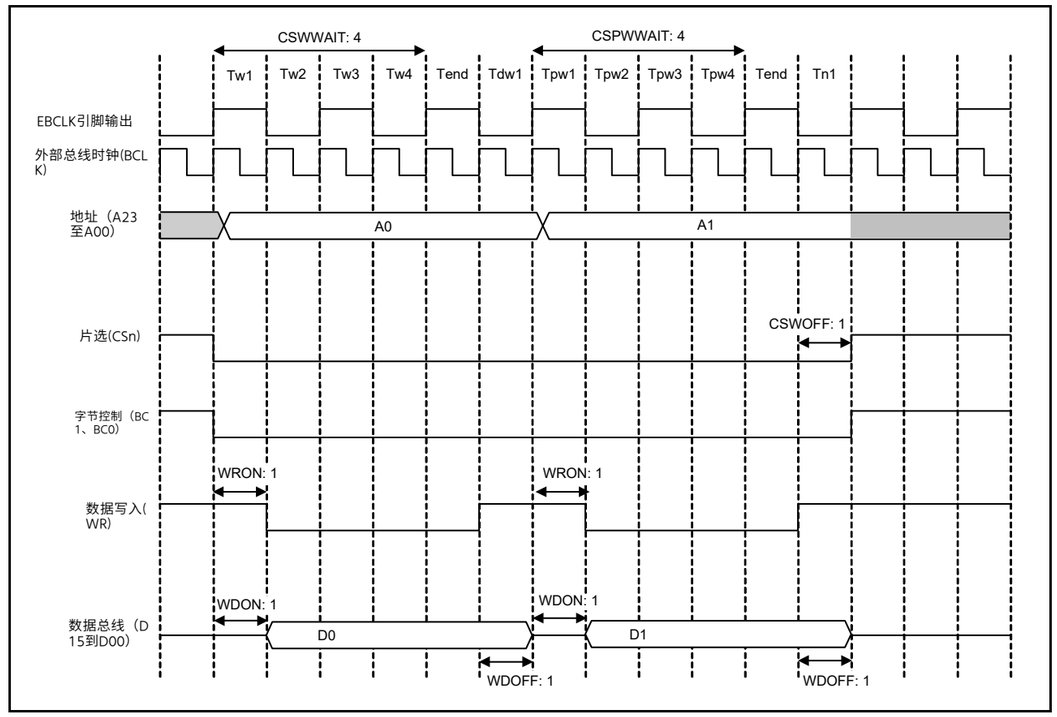


Figure 15.26 当在EBCLK引脚输出选择位中选择BCLK2并且在单次写入选通模式（n=0到7）下响应单个传输请求而生成两轮总线访问时的示例页面写入访问操作

15.5.2 Address/Data Multiplexed Bus

当CSnCR中的地址数据复用IO接口选择位(MPXEN)设置为1时，地址和数据可以复用输入输出到相应区域的D15到D00引脚。使用该功能可以将该LSI直接连接到需要地址数据复用的外围LSI。当使用CSnCR中的BSIZE[1:0]位选择8位宽度时，D7至D00与A07至A00复用。When16-bitwidthisselected D15toD00aremultiplexedwithA15 toA00.在地址数据复用IO空间中，访问由ALE、RD、WRn和BCn信号控制。

字节选通模式或单写选通模式可以以与单独总线相同的方式进行选择。然而，对于地址周期内的BCn信号，字节控制　　信号被输出用于正在读取或写入的数据。

在地址数据复用IO空间访问期间，在地址输出周期插入CSnWCR2中的地址周期等待选择位（AWAIT[1:0]）指定的等待周期数后，执行数据访问。

Ta1到Tan（地址周期等待）
只有在指定地址数据复用IO空间时，周期Ta1到Tan才有效。该周期由外部总线访问开始到地址锁存(ALE)信号被否定之前的1个周期之间的时钟周期数组成。循环次数可以在零到三的范围内选择。地址输出到ALE信号否定的下一个周期（地址周期）。ALE信号的时序与CS断言的时序相同。在地址周期之后，开始一个数据周期。CSnWCR1和CSnWCR2应设置为地址周期和数据周期不重叠。

页访问地址数据复用的IO空间是无效的。当CSnMOD中的PRENB或PWENB位设置为1以启用页面读取或页面写入访问时，这些设置将被忽略并执行正常的读取或写入操作。

图15.27至图15.29显示了地址数据复用IO接口的操作示例

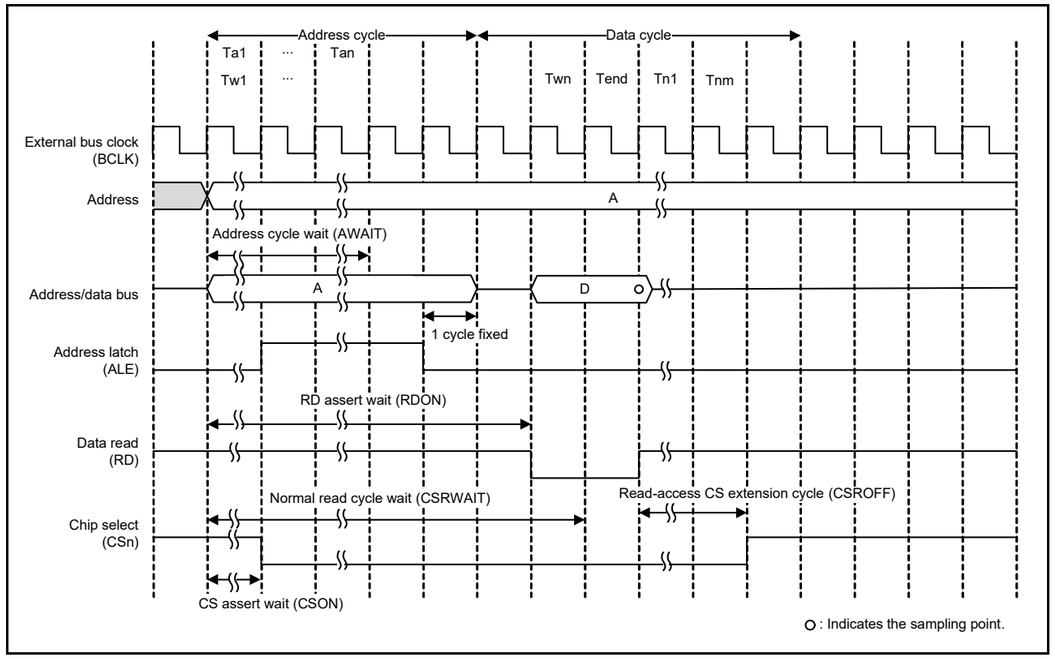


Figure 15.27 Example of read access operation with address/data multiplexed I/O interface (n = 0 to 7)

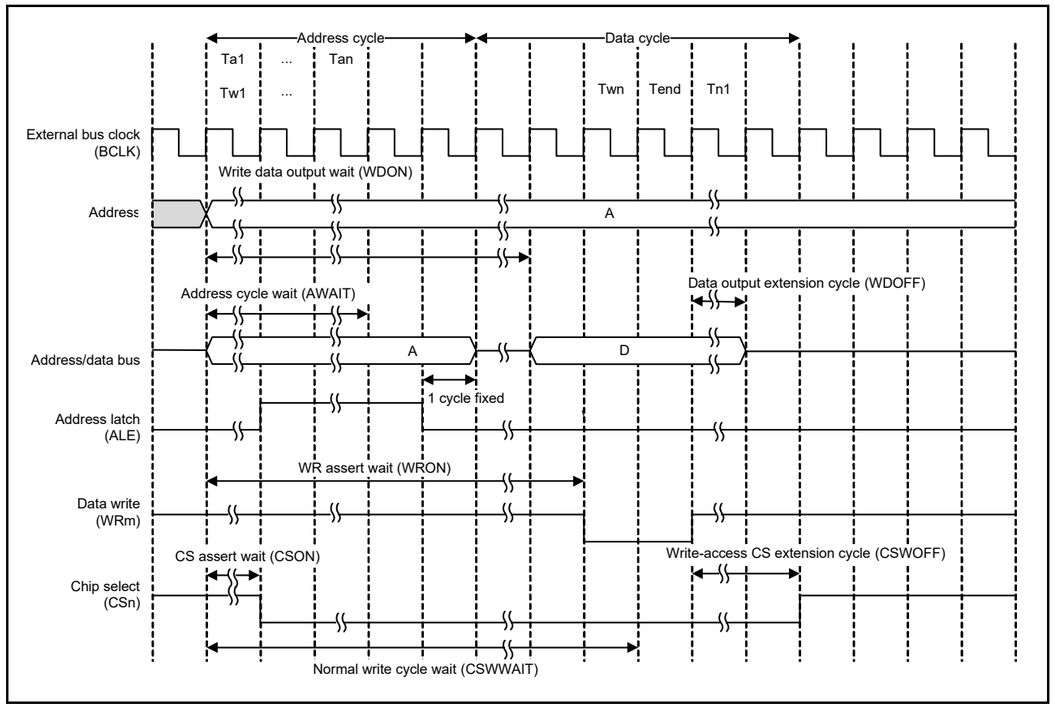


Figure 15.28 Example of write access operation with address/data multiplexed I/O interface (m = 0, 1)

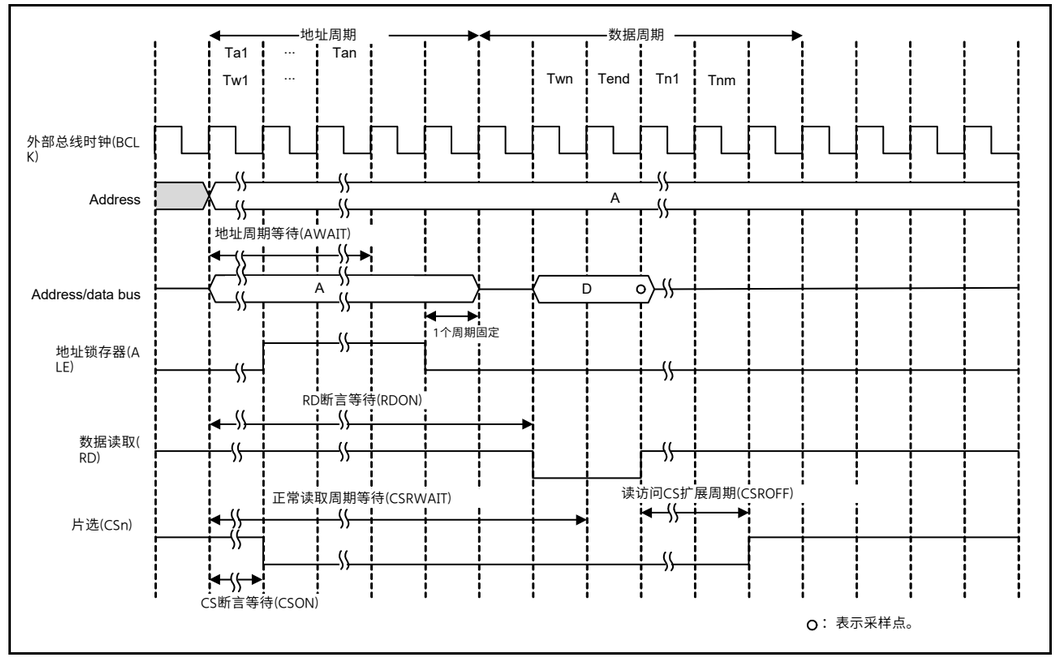


Figure 15.27 地址数据复用IO接口（n=0到7）的读访问操作示例

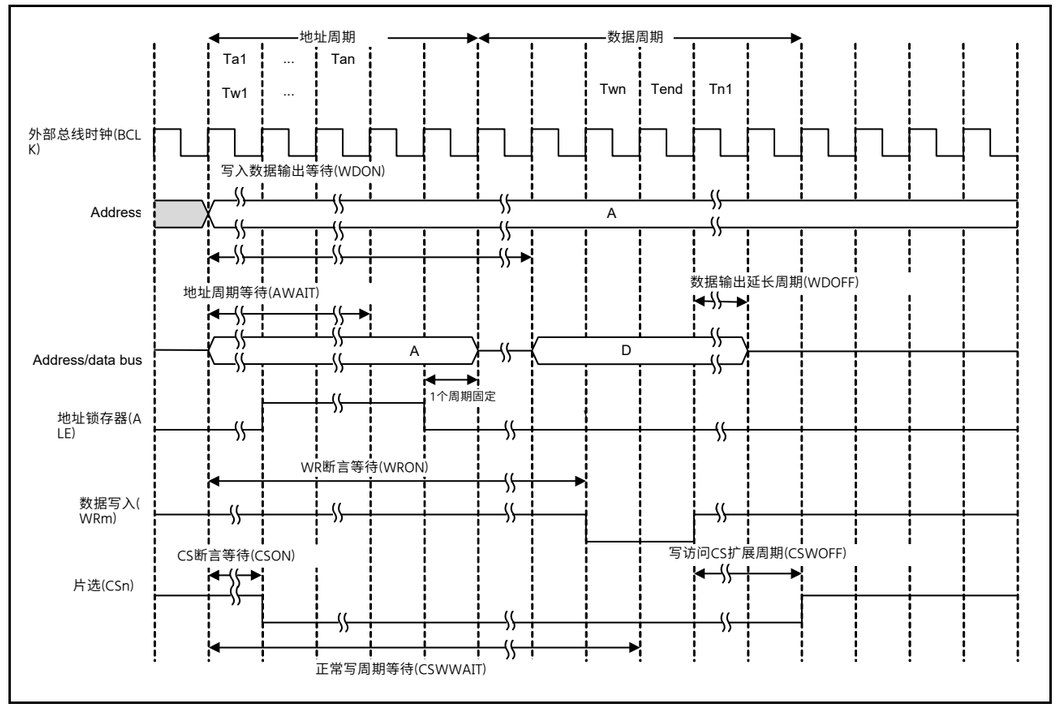


Figure 15.28 地址数据复用IO接口的写访问操作示例(m=0 1)

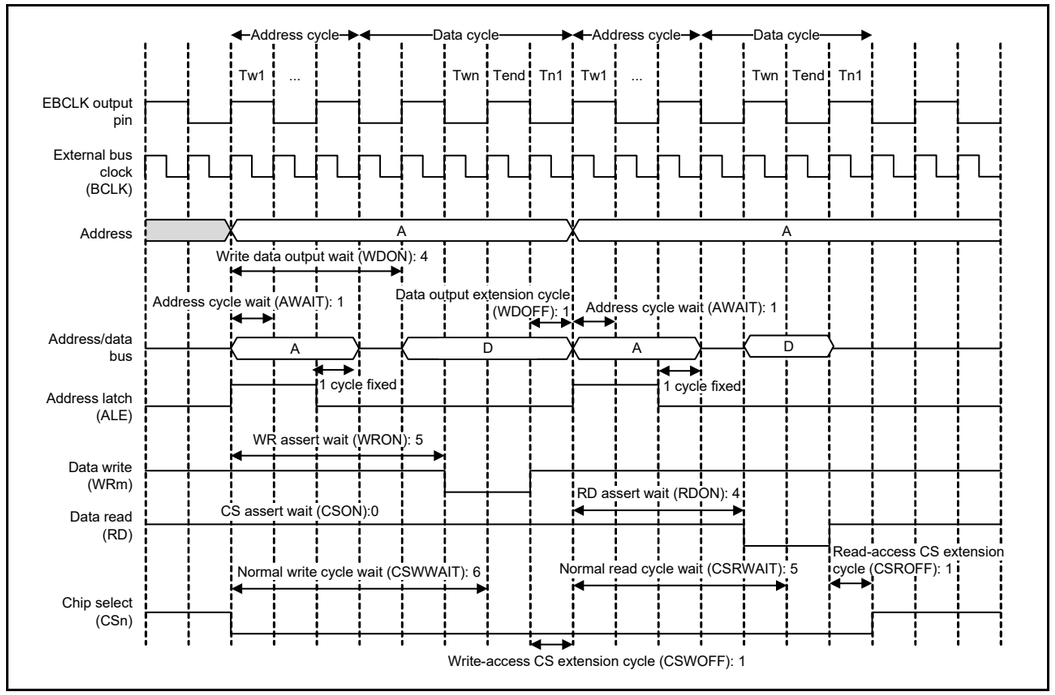


Figure 15.29 Example of bus timing with address/data multiplexed I/O interface (m = 0, 1)

15.5.3 External Wait Function

Wait cycles can be extended by the WAIT signal beyond the length of the normal access cycle wait specified in the CSRWAIT[4:0] and CSWWAIT[4:0] bits in CSnWCR1, and the page access cycle wait specified in the CSPRWAIT[2:0] and CSPWWAIT[2:0] bits in CSnWCR1.

When external wait is enabled (EWENB = 1 in CSnMOD), wait cycles are inserted while the WAIT signal is held low. When external wait is disabled (EWENB = 0 in CSnMOD), the WAIT signal has no effect. All wait cycles specified in CSnWCR1 are inserted independently of the WAIT signal.

(1) Normal access

Sampling of the WAIT signal begins on completion of the wait cycle (Tend) specified in CSnWCR1. The bus cycle is extended while the WAIT signal is held low. The wait cycle ends (Tend) at the next cycle after the WAIT signal goes high.

(2) Page access

The first access operation is the same as the normal access operation. Sampling of the WAIT signal begins on completion of the wait cycle (Tend) specified in the CSnWCR1 register. The bus cycle is extended while the WAIT signal is held low. The wait cycle (Tend) ends at the next cycle after the WAIT signal goes high.

For the second and subsequent accesses, sampling of the WAIT signal begins on completion of the page access wait cycle (Tend). The page access wait cycle is extended while the WAIT signal is held low, and ends (Tend) at the next cycle after the WAIT signal goes high.

Figure 15.30 to Figure 15.33 show examples of external wait insertion timing with the separate bus interface.

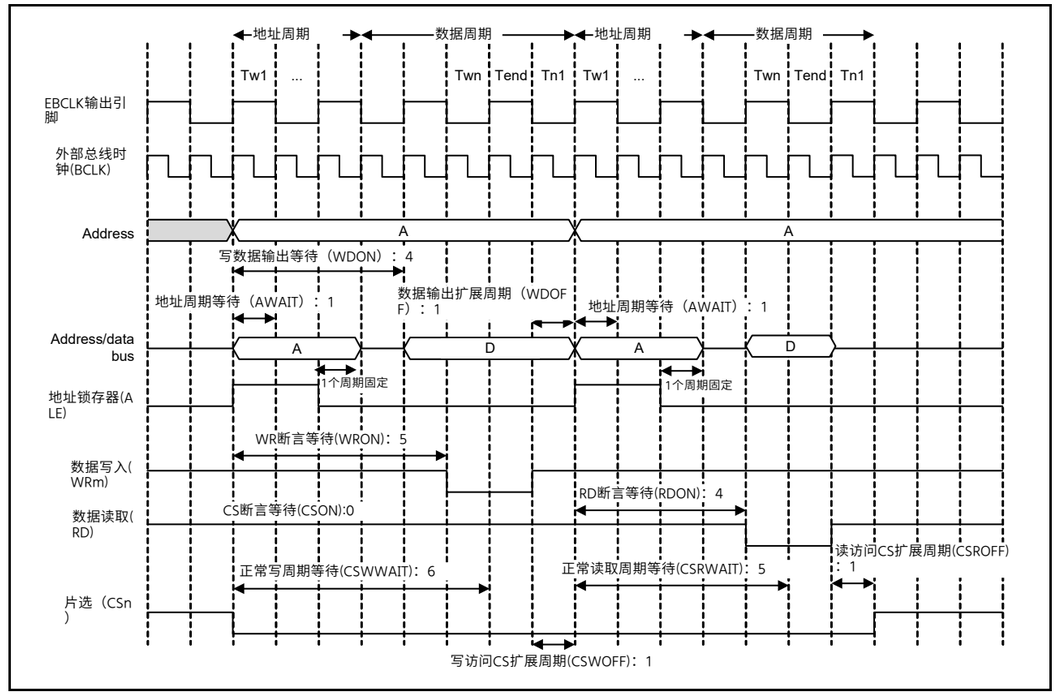


Figure 15.29 地址数据复用IO接口的总线时序示例(m=0 1)

15.5.3 外部等待功能

等待周期可以通过WAIT信号延长到超出在指定的正常访问周期等待的长度
CSnWCR1中的CSRWAIT[4:0]和CSWWAIT[4:0]位，以及在CSnWCR1中的CSPRWAIT[2:0]和CSWWWAIT[2:0]位中指定的页面访问周期等待。

当启用外部等待时（CSnMOD中的EWENB=1），在WAIT信号保持低电平时插入等待周期。当外部等待被禁用时（CSnMOD中的EWENB=0），WAIT信号无效。中指定的所有等待周期
CSnWCR1独立于WAIT信号插入。

(1) 正常访问

WAIT信号的采样在CSnWCR1中指定的等待周期(Tend)完成时开始。当WAIT信号保持低电平时，总线周期会延长。等待周期在WAIT信号变高后的下一个周期结束(Tend)。

(2) 页面访问

第一次访问操作与正常访问操作相同。WAIT信号的采样在CSnWCR1寄存器中指定的等待周期(Tend)完成时开始。当WAIT信号保持低电平时，总线周期会延长。等待周期(Tend)在WAIT信号变为高电平后的下一个周期结束。

对于第二次和后续访问，WAIT信号的采样在页面访问等待周期(Tend)完成时开始。页面访问等待周期在WAIT信号保持低电平时延长，并在WAIT信号变为高电平后的下一个周期结束(Tend)。

图15.30至图15.33显示了使用独立总线接口的外部等待插入时序示例。

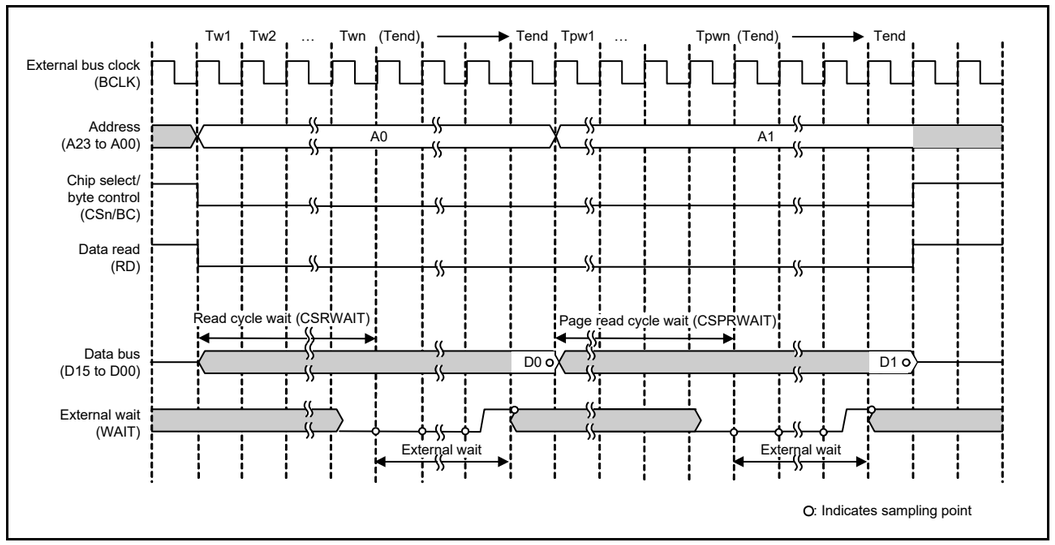


Figure 15.30 Example external wait timing for page read access to 16-bit bus space (when 1/1 BCLK is selected with the BCLK Pin Output Select bit) (n = 0 to 7, m = 0, 1)

Figure 15.31 Example external wait timing for page read access to 16-bit bus space (when 1/2 BCLK is Selected with the BCLK Pin Output Select bit) (n = 0 to 7, m = 0, 1)

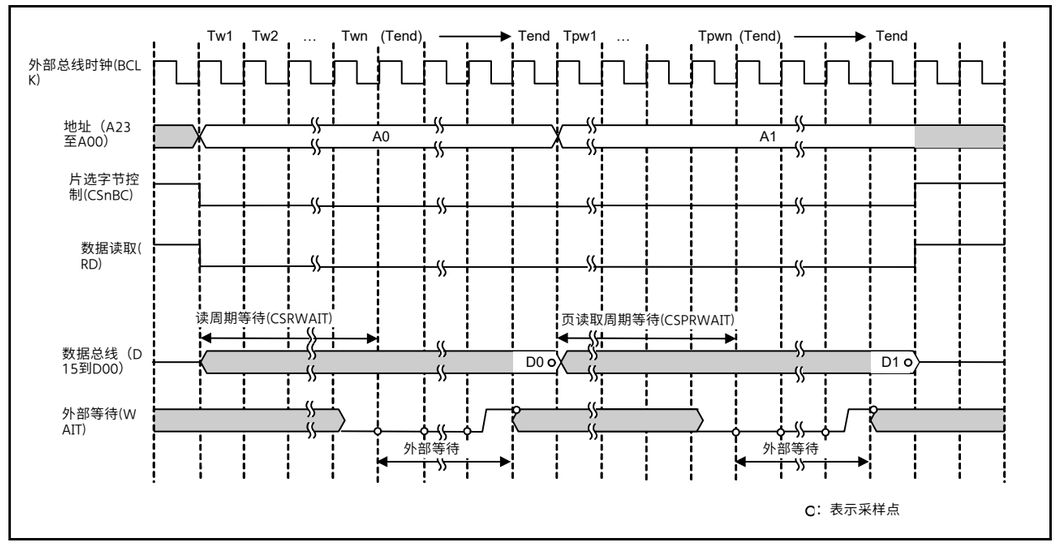


Figure 15.30 对16位总线空间进行页面读取访问的外部等待时序示例（当使用BCLK引脚输出选择位选择11BCLK时）（n=0到7，m=0、1）

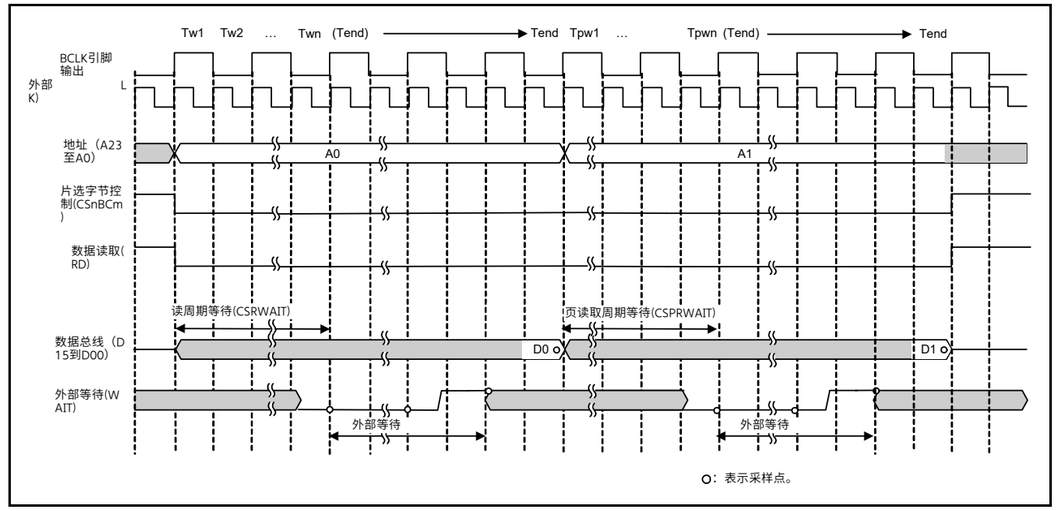


Figure 15.31 对16位总线空间进行页面读取访问的外部等待时序示例（当12BCLK为通过BCLK引脚输出选择位选择）（n=0至7，m=0、1）

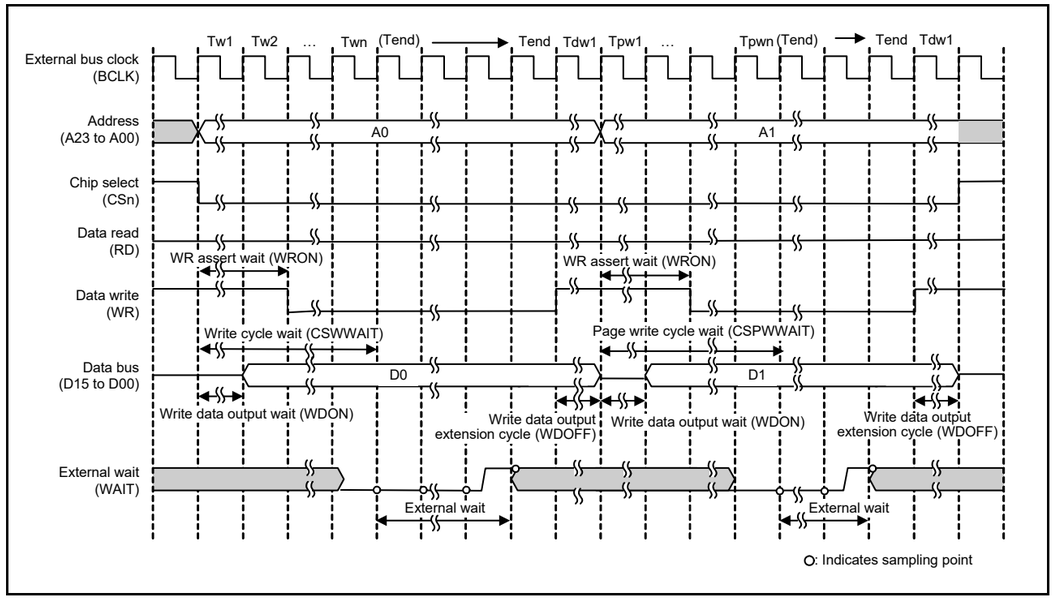


Figure 15.32 Example external wait timing for page write access to 16-bit bus space in byte strobe mode (when 1/1 BCLK is selected with the BCLK Pin Output Select bit) (n = 0 to 7, m = 0, 1)

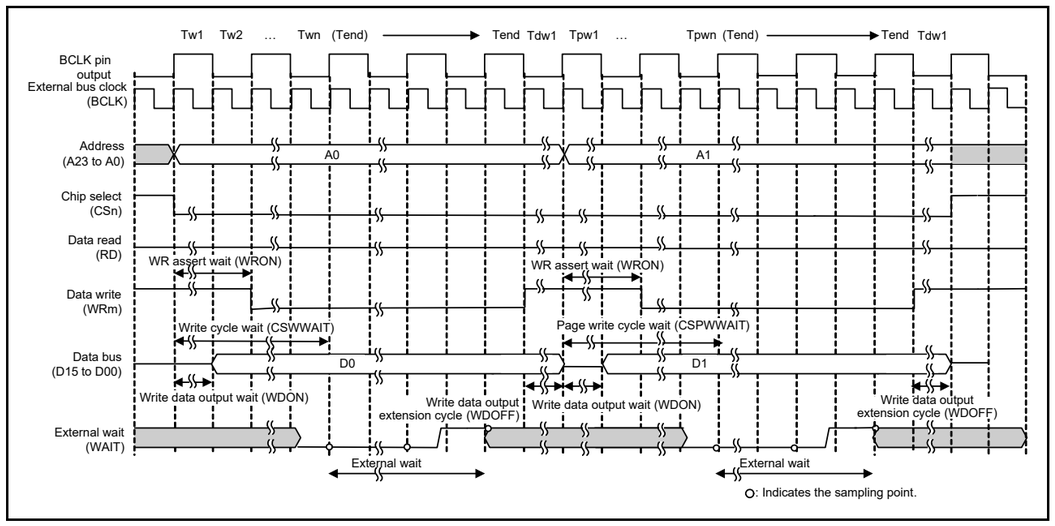


Figure 15.33 Example external wait timing for page write access to 16-bit bus space in byte strobe mode (when 1/2 BCLK is selected with the BCLK Pin Output Select bit) (n = 0 to 7, m = 0, 1)

(3) Address/data multiplexed I/O interface

In a data cycle with the address/data multiplexed I/O interface, programmed waits and pin waits using the WAIT pin can be inserted in the same way as that with the separate bus interface.

Address cycles are not affected by the wait control settings. Figure 15.34 shows an example of external wait insertion timing with the address/data multiplexed I/O interface.

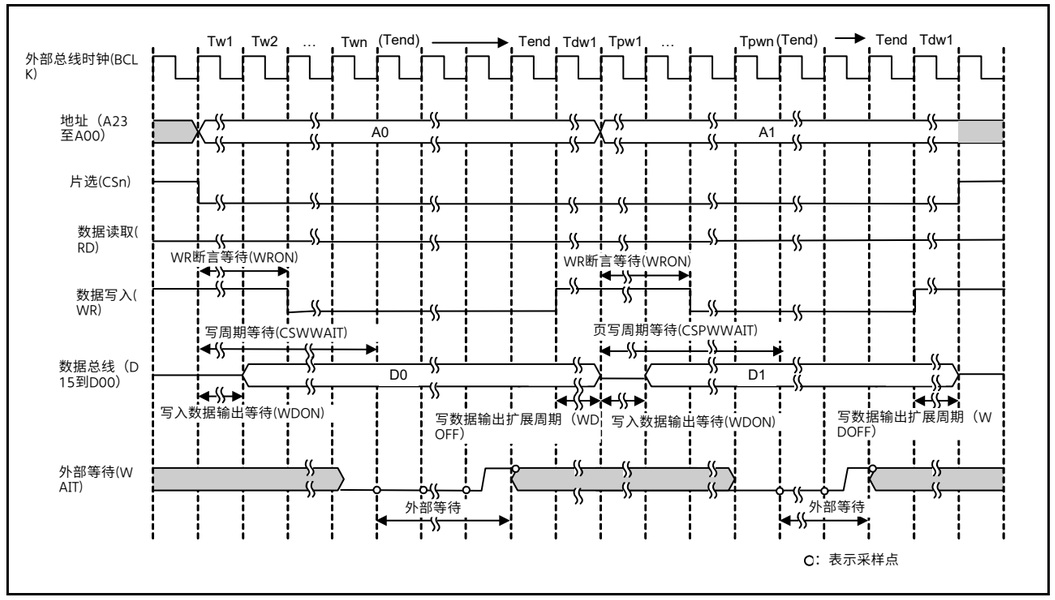


Figure 15.32 字节选通模式下对16位总线空间的页面写访问的外部等待时序示例（当使用BCLK引脚输出选择位选择11 BCLK时）（n=0到7，m=0、1）

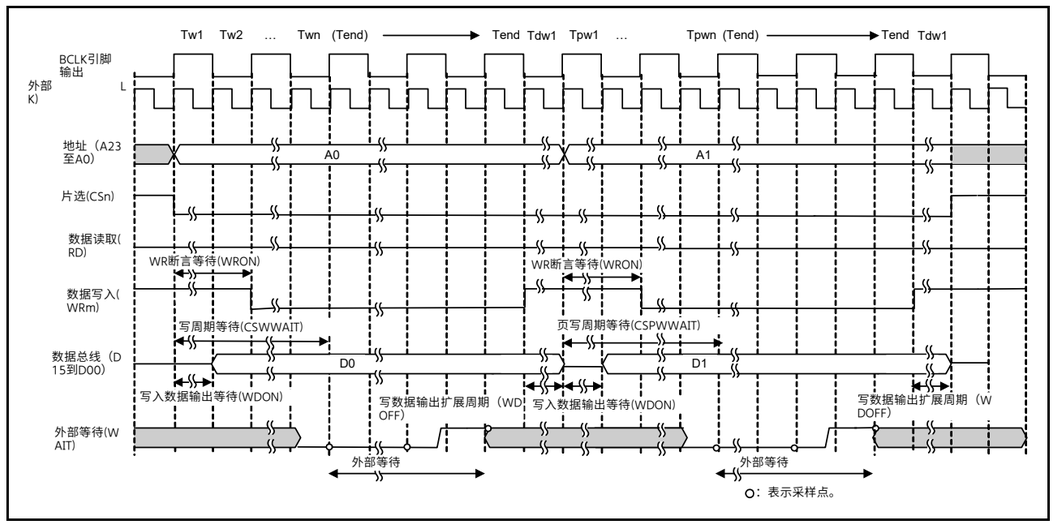


Figure 15.33 字节选通模式下对16位总线空间的页面写访问的外部等待时序示例（当使用BCLK引脚输出选择位选择12 BCLK时）（n=0到7，m=0、1）

(3) Address/data multiplexed I/O interface

在地址数据复用IO接口的数据周期中，编程等待和使用WAIT引脚的引脚等待可以以与单独总线接口相同的方式插入。

地址周期不受等待控制设置的影响。图15.34显示了地址数据复用IO接口的外部等待插入时序示例。

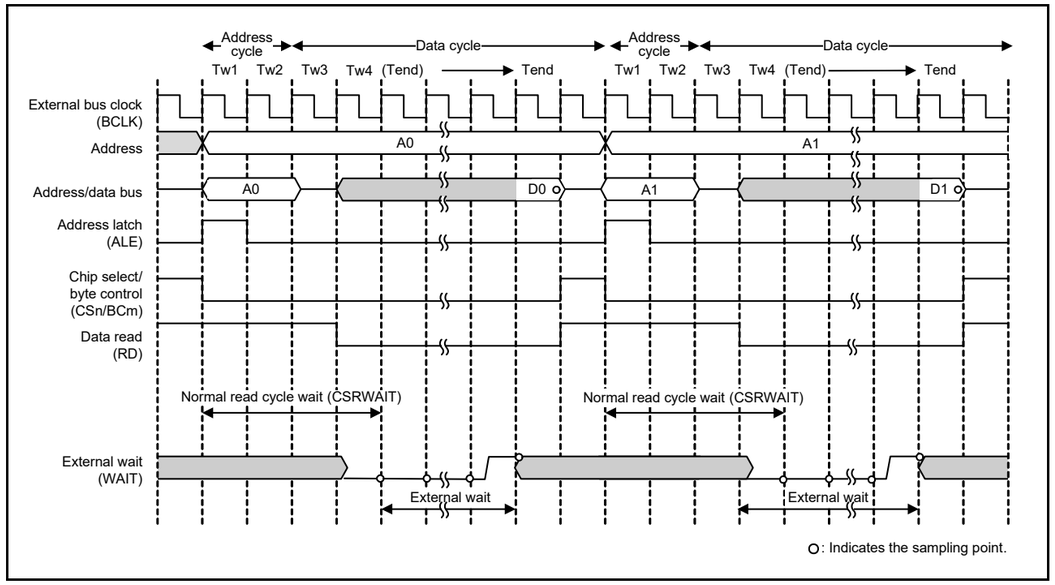


Figure 15.34 Example external wait Insertion timing with address/data multiplexed I/O interface (m = 0, 1)

15.5.4 Insertion of Recovery Cycles

Recovery cycles can be inserted between consecutive rounds of external bus access by setting the Recovery Cycle Insertion Enable bit in CSRECEN to 1.

The number of recovery cycles to be inserted after read cycles and write cycles can be independently set for each area using CSnREC. When the preceding bus cycle is a write access, the number of write recovery cycles must be set with the WRCV[3:0] bits for the associated area. When the preceding bus cycle is a read access, the number of read recovery cycles must be set with the RRCV[3:0] bits for the associated area. For example, when a CS1 read access occurs after a CS0 read access, the number of recovery cycles to be inserted between them is set in the RRCV[3:0] bits in CS0REC.

Recovery cycle insertion can be enabled or disabled with RCVENi (i = 0 to 7) in CSRECEN when the preceding bus access is a separate bus access, and with RCVENMj (j = 0 to 7) when the preceding bus access is an address/data multiplexed bus access.

Recovery cycles can be inserted on any of the following conditions:

- After a read access to the external bus, a read access is made to the external bus in the same area
- After a read access to the external bus, a read access is made to the external bus in a different area
- After a read access to the external bus, a write access is made to the external bus in the same area
- After a read access to the external bus, a write access is made to the external bus in a different area
- After a write access to the external bus, a read access is made to the external bus in the same area
- After a write access to the external bus, a read access is made to the external bus in a different area
- After a write access to the external bus, a write access is made to the external bus in the same area
- After a write access to the external bus, a write access is made to the external bus in a different area.

The recovery cycle starts at the end of the preceding bus cycle, for example when the CSn signal (n = 0 to 7) is negated. A high-level period of the CSn signal is inserted for the specified recovery cycle period starting from this point.

In the fastest case, the CSn signal for the next round of bus access is asserted immediately after the end of the recovery cycles. Even if the next request for access to an external address space is generated during the recovery period, the next access over the external bus starts immediately after the end of the recovery cycles.

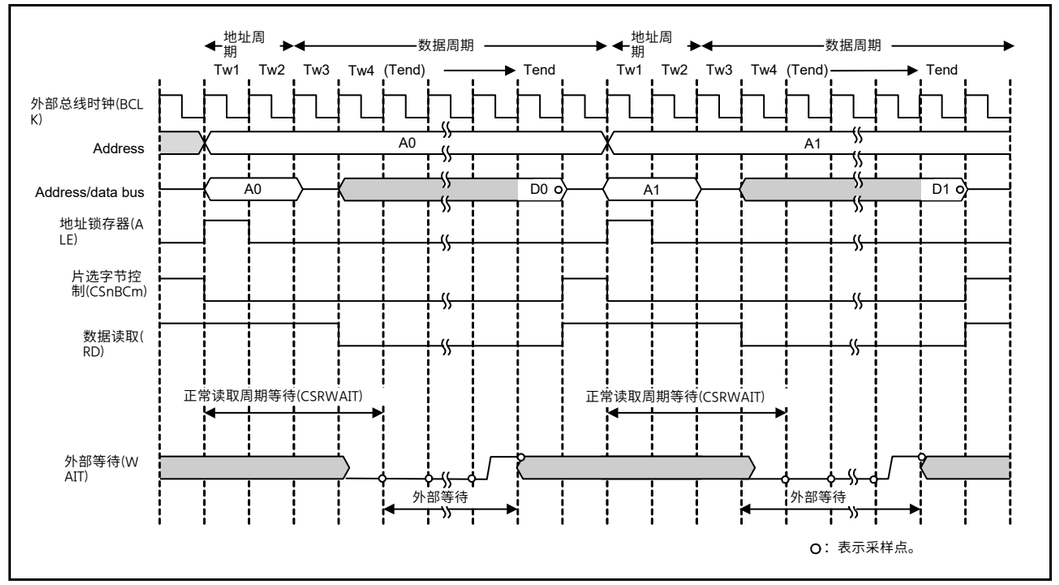


Figure 15.34 示例外部等待插入时序与地址数据多路复用IO接口(m=0 1)

15.5.4 恢复周期的插入

通过设置恢复周期，可以在连续几轮外部总线访问之间插入恢复周期
CSRECEN中的插入使能位为1。

可以使用CSnREC为每个区域独立设置读取周期和写入周期后插入的恢复周期数。当前一个总线周期是写访问时，必须使用相关区域的WRCV[3:0]位设置写恢复周期数。当前一个总线周期是读访问时，必须使用相关区域的RRCV[3:0]位设置读恢复周期数。例如，当CS1读访问发生在CS0读访问之后，要在它们之间插入的恢复周期数在CS0REC的RRCV[3:0]位中设置。

当前面的总线访问是单独的总线访问时，可以使用CSRECEN中的RCVENi(i=0到7)启用或禁用恢复周期插入，
当前面的总线访问是多路复用的地址数据时，可以使用RCVENMj(j=0到7)启用或禁用恢复周期插入总线访问
。

可以在以下任何条件下插入恢复周期：

- 对外部总线进行读访问后，对同一区域的外部总线进行读访问
- 对外部总线进行读访问后，对不同区域的外部总线进行读访问
- 对外部总线进行读访问后，对同一区域的外部总线进行写访问
- 对外部总线进行读访问后，对不同区域的外部总线进行写访问
- 对外部总线进行写访问后，对同一区域的外部总线进行读访问
- 对外部总线进行写访问后，对不同区域的外部总线进行读访问
- 对外部总线进行写访问后，对同一区域的外部总线进行写访问
- 在对外部总线进行写访问之后，对不同区域中的外部总线进行写访问。

恢复周期在前一个总线周期结束时开始，例如当CSn信号（n=0到7）被否定时。
从该点开始，在指定的恢复周期周期内插入CSn信号的高电平周期。

在最快的情况下，下一轮总线访问的CSn信号在恢复周期结束后立即生效。即使在恢复期间产生了访问外部地址空间的下一个请求，通过外部总线的下一次访问也会在恢复周期结束后立即开始。

When two or more external bus access cycles are required for a single transfer request from a bus master, and the recovery cycle insertion condition is satisfied, recovery cycles are also inserted between these bus access cycles. However, when page read access is enabled (CSnMOD.PRENB = 1) or page write access is enabled (CSnMOD.PWENB = 1), recovery cycles are not inserted except after the last bus access cycle of the transfer, even if the recovery cycle insertion condition is satisfied. See Figure 15.37.

Similarly, during normal access with page access enabled, recovery cycles are not inserted between bus access cycles but only after the last bus access cycle of the transfer. With the address/data multiplexed I/O interface, when the recovery cycle insertion condition is satisfied, recovery cycles are inserted between bus access cycles regardless of the page access enable setting.

Figure 15.35 to Figure 15.37 show examples of recovery cycle insertion with the separate bus interface.

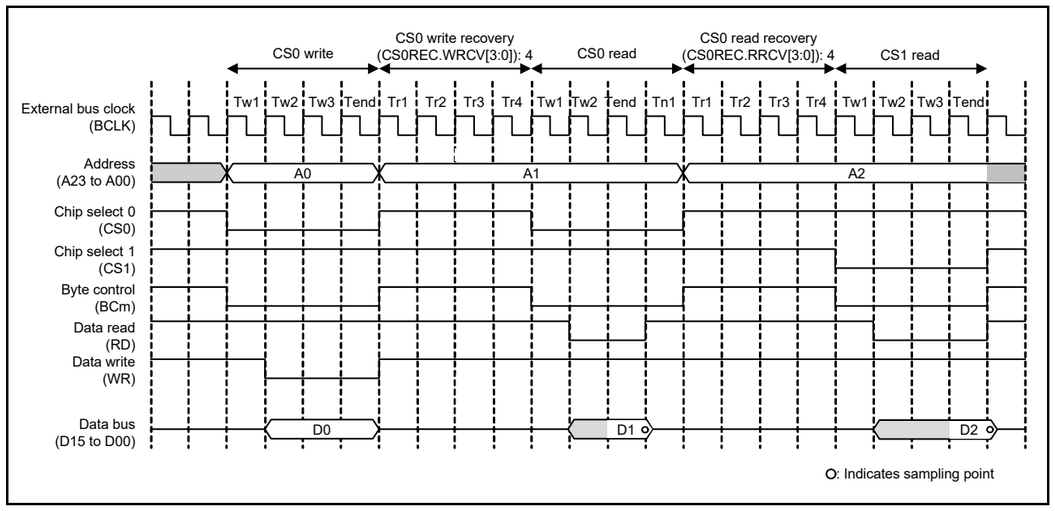


Figure 15.35 Example recovery cycle insertion with separate bus interface (m = 0, 1)

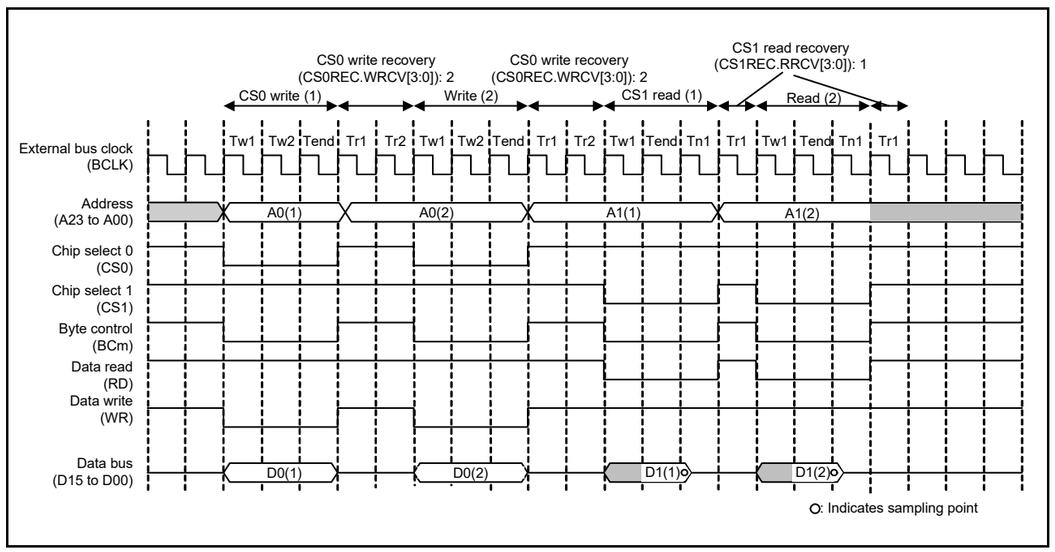


Figure 15.36 Example recovery cycle insertion when bus access is split, with separate bus interface and normal access (m = 0, 1)

当来自总线主机的单个传输请求需要两个或多个外部总线访问周期，并且恢复周期插入条件满足时，恢复周期也在这些总线访问周期之间插入。但是，当启用页面读取访问(CSnMOD.PRENB=1)或启用页面写入访问(CSnMOD.PWENB=1)时，不会插入恢复周期，除非在传输的最后一个总线访问周期之后，即使恢复周期满足插入条件。请参见图15.37。

类似地，在启用页面访问的正常访问期间，恢复周期不会插入总线访问周期之间，而是仅在传输的最后一个总线访问周期之后插入。对于地址数据复用IO接口，当恢复周期插入条件满足时，无论页面访问使能设置如何，都会在总线访问周期之间插入恢复周期。

图15.35至图15.37显示了使用单独的总线接口插入恢复周期的示例。

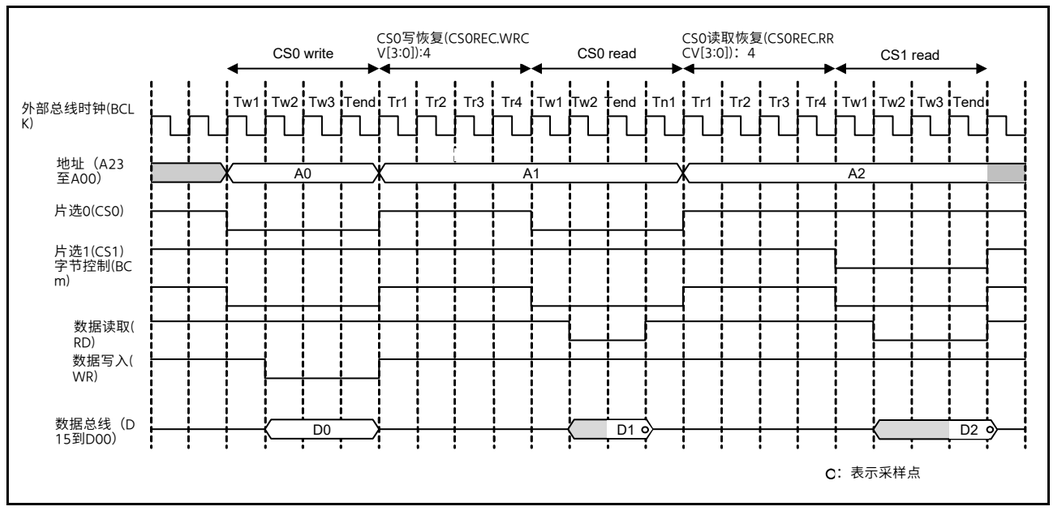


Figure 15.35 使用单独的总线接口(m=0 1)插入恢复周期示例

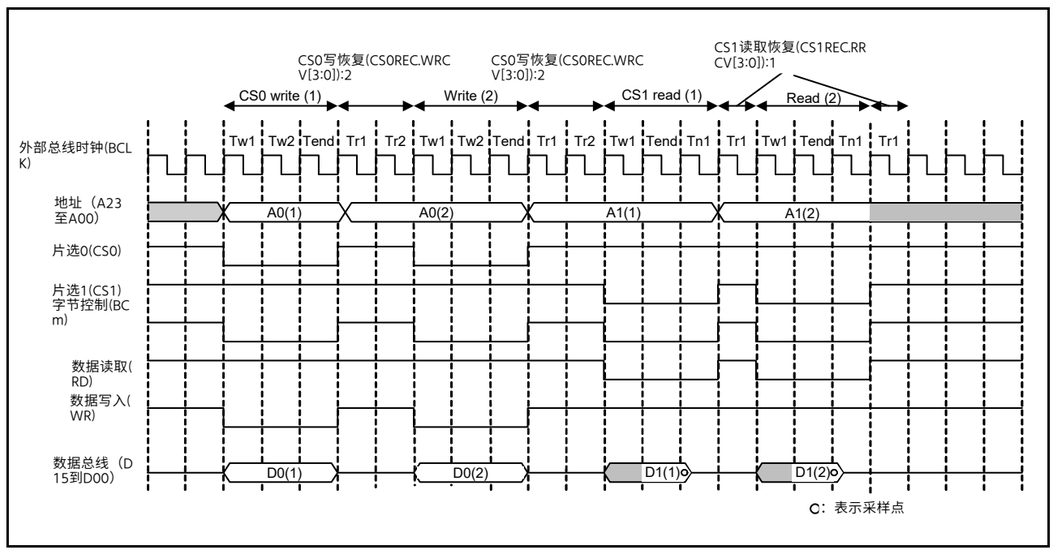


Figure 15.36 总线访问分离时的恢复周期插入示例，具有单独的总线接口和正常访问(m=0 1)

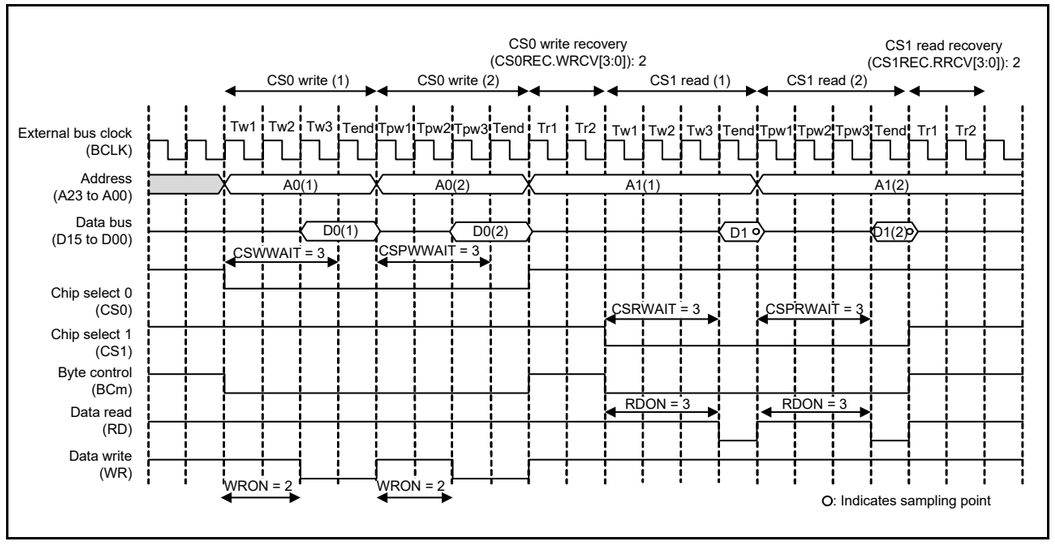


Figure 15.37 Example recovery cycle insertion when bus access is split, with separate bus interface and page access (m = 0, 1)

Figure 15.38 shows an example operation when BCLK/2 is selected as the frequency division in the EBCLK Pin Output Select bit.

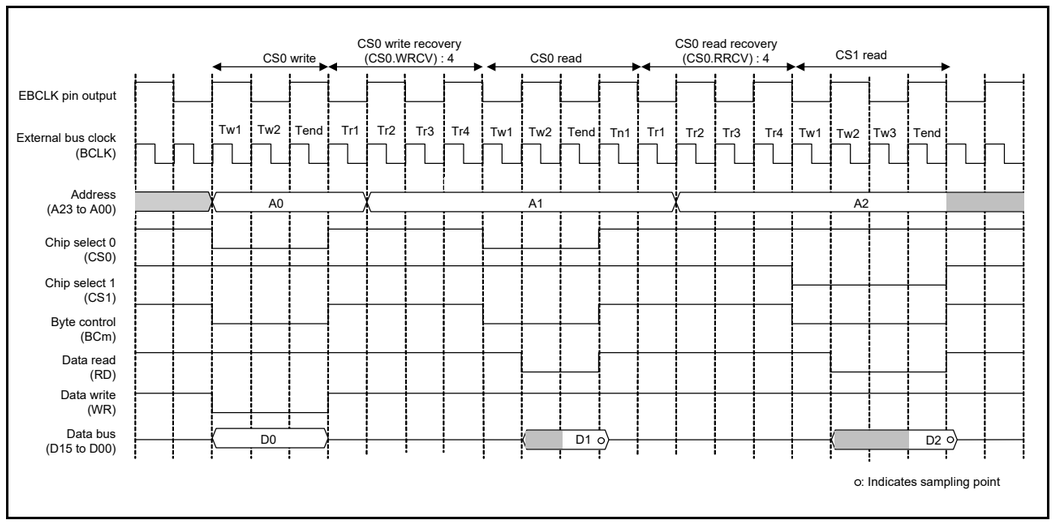


Figure 15.38 Example operation for recovery cycles when BCLK/2 is selected in the EBCLK Pin Output Select bit, with normal access through a separate bus interface (m = 0, 1)

With the address/data multiplexed I/O interface, recovery cycles are inserted in the same way as that with the separate bus interface. Figure 15.39 and Figure 15.40 show examples of recovery cycle insertion with the address/data multiplexed I/O interface.

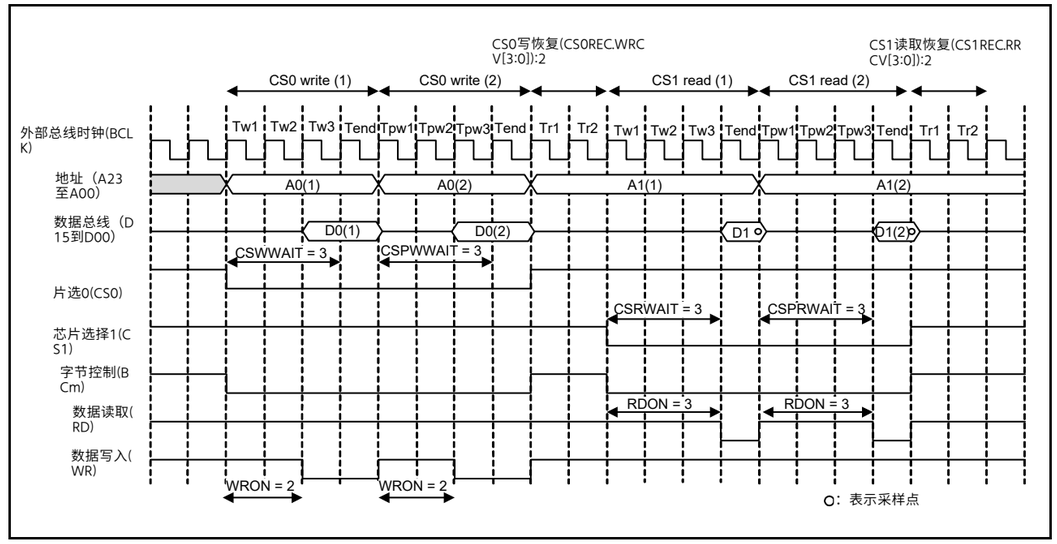


Figure 15.37 总线访问分离时的示例恢复周期插入，具有单独的总线接口和页面访问(m=0 1)

图15.38显示了在EBCLK引脚输出中选择BCLK2作为分频时的示例操作选择位。

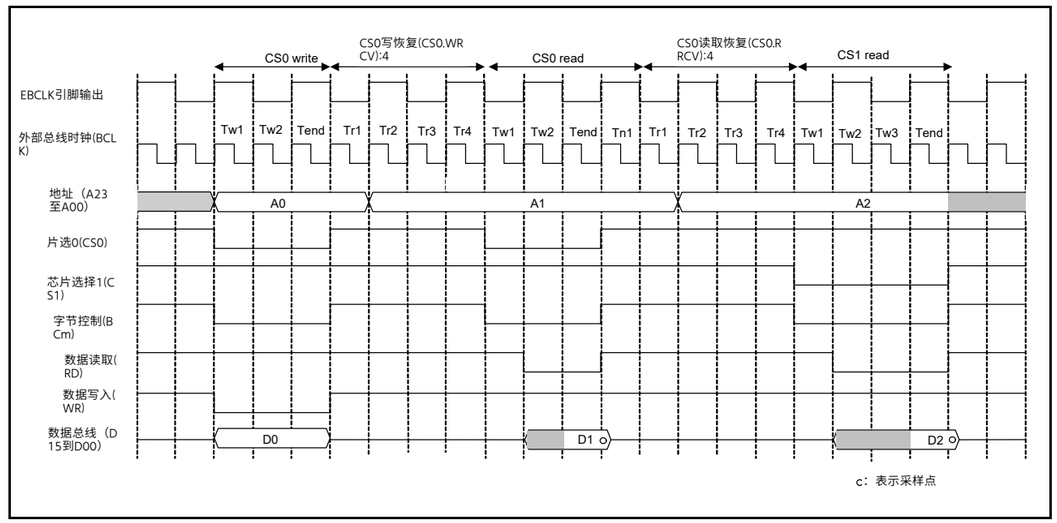


Figure 15.38 在EBCLK引脚输出选择位中选择BCLK2时恢复周期的示例操作，通过单独的总线接口正常访问(m=0 1)

对于地址数据复用IO接口，恢复周期的插入方式与单独总线接口的插入方式相同。图15.39和图15.40显示了使用地址数据复用IO接口插入恢复周期的示例。

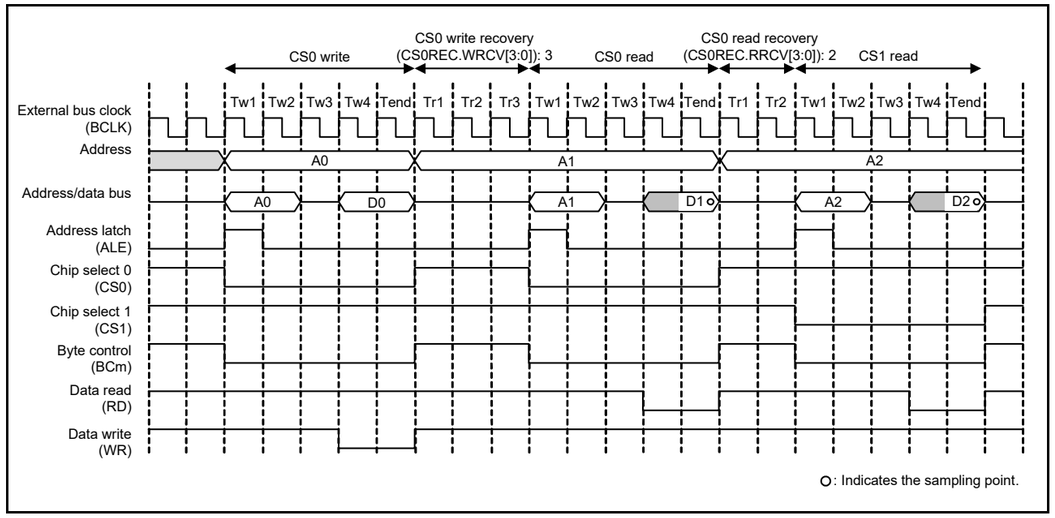


Figure 15.39 Example of recovery cycle insertion with address/data multiplexed I/O interface (m = 0, 1)

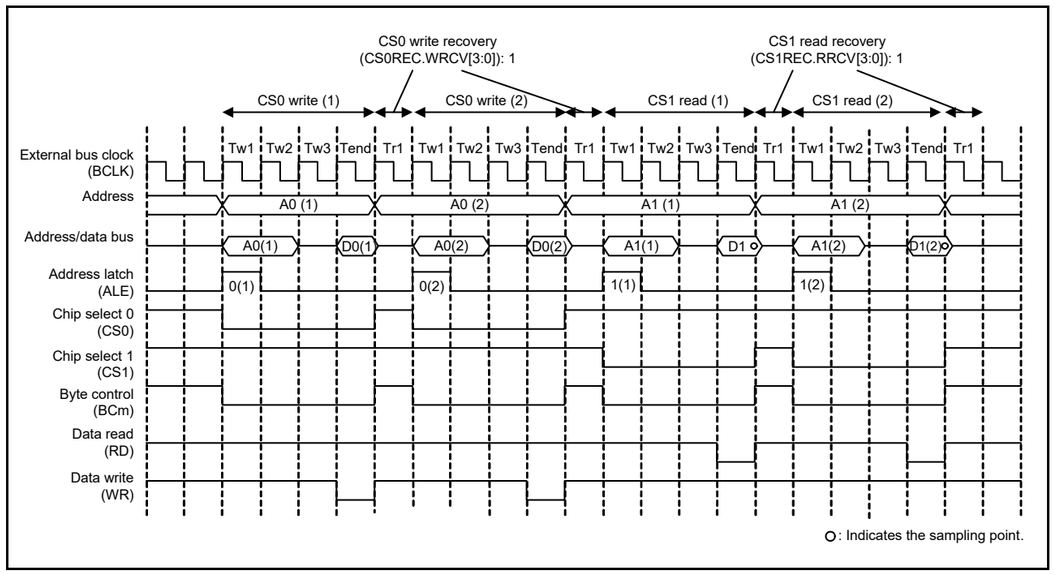


Figure 15.40 Example of recovery cycle insertion when a bus access is split with address/data multiplexed I/O interface (m = 0, 1)

15.5.5 No Access State

When no external address space is accessed, the CSn, BCn, WRn, RD signals are high, ALE signal is low, and D15 to D00 are in the high-impedance state.

15.5.6 Write Buffer Function (External Bus)

In write access, the main bus is released by writing data to the write buffer before the access is complete. This allows the next round of bus access to start. However, if the next access is to an external address space or to a register of the external bus controller, it is suspended until the external bus operations already in progress are complete.

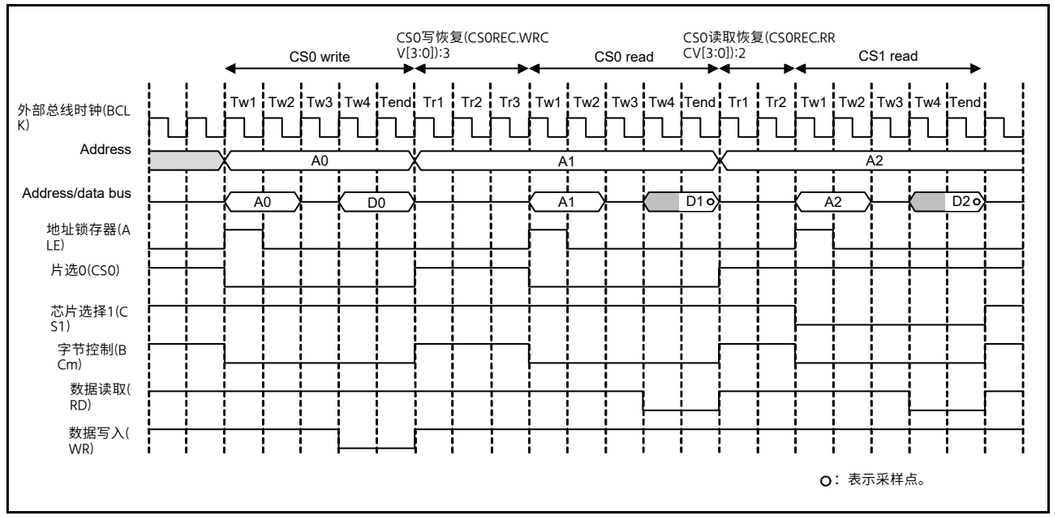


Figure 15.39 使用地址数据多路复用IO接口(m=0 1)插入恢复周期的示例

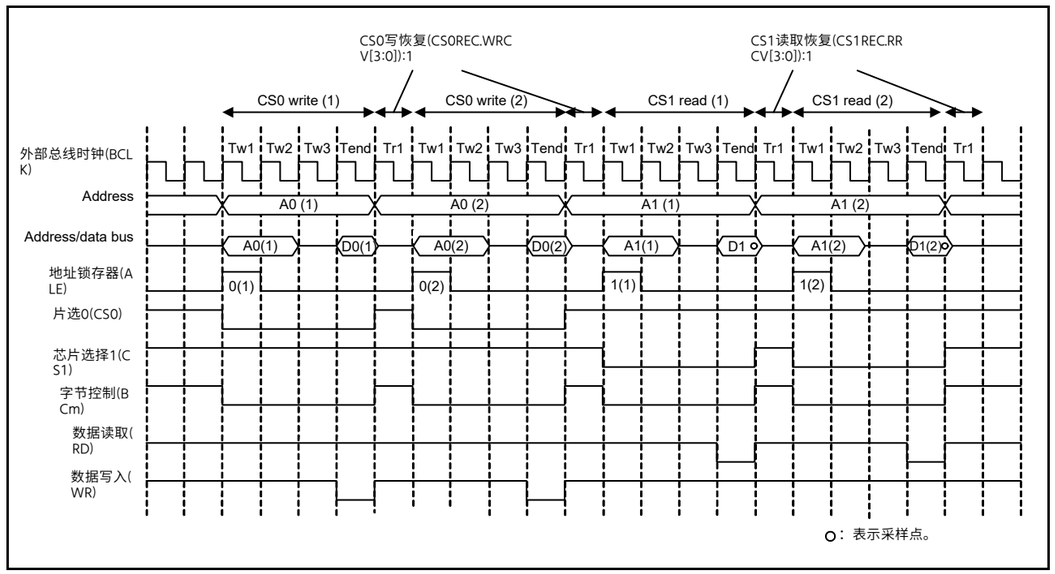


Figure 15.40 使用地址数据复用IO接口(m=0 1)拆分总线访问时的恢复周期插入示例

15.5.5 无访问状态

当没有访问外部地址空间时，CSn、BCn、WRn、RD信号为高电平，ALE信号为低电平，D15到D00处于高阻状态。

15.5.6 写缓冲功能（外部总线）

在写访问中，通过在访问完成之前将数据写入写缓冲区来释放主总线。这允许下一轮总线访问开始。然而，如果下一次访问是对外部地址空间或外部总线控制器的寄存器，则它会被挂起，直到已经在进行中的外部总线操作完成。

Figure 15.41 shows an example of operation when the write buffer function is in use. When this function is in use, if the next operation after an external write is an internal access, the internal access is executed in parallel with the external write, for example without waiting for completion of the latter operation.

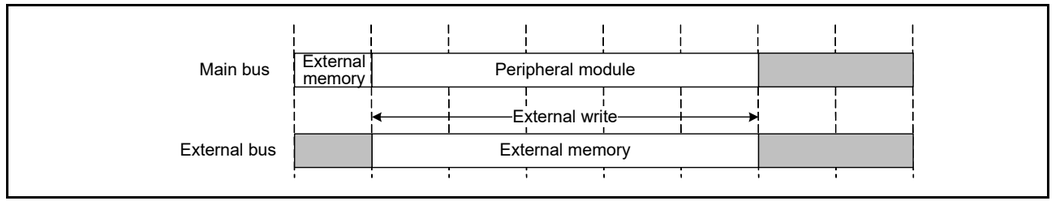


Figure 15.41 Example operation when the write buffer function is in use

15.5.7 Constraints

(1) Constraints on using a separate bus interface

Table 15.11 lists the constraints that apply to bits in the CSn Wait Control Register 1 (CSnWCR1) and CSn Wait Control Register 2 (CSnWCR2) when normal and page accesses occur.

Even if the Page Read Access Enable bit or Page Write Access Enable bit in the CSn Mode Register is set to enable (CSnMOD.PRENB = 1 or CSnMOD.PWENB = 1), the first page access or access that does not fall within the scope of a page access is a normal access operation. Because of this, constraints on normal access must be satisfied.

Table 15.11 Constraints on normal access and page access

Constraints on normal access		Constraints on page access	
Reading	**Writing**	**Reading**	**Writing**
CSON[2:0] ≤ CSRWAIT RDON[2:0] ≤ CSRWAIT CSON[2:0] ≤ RDON	1 ≤ WDON[2:0] CSON[2:0] ≤ CSWWAIT WRON[2:0] ≤ CSWWAIT WDON[2:0] ≤ CSWWAIT WDOFF[2:0] ≤ CSWOFF WDON[2:0] ≤ WRON CSON[2:0] ≤ WRON	CSON[2:0] ≤ CSPRWAIT RDON[2:0] ≤ CSPRWAIT CSON[2:0] ≤ RDON	1 ≤ WDON[2:0] CSON[2:0] ≤ CSPWWAIT WRON[2:0] ≤ CSPWWAIT WDON[2:0] ≤ CSPWWAIT WDOFF[2:0] ≤ CSWOFF WDON[2:0] ≤ WRON CSON[2:0] ≤ WRON

Note: When two or more external bus access cycles are required for a single transfer request from a bus master, and the recovery cycle insertion condition is satisfied, with page read access enabled (CSnMOD.PRENB = 1) or page write access enabled (CSnMOD.PWENB = 1), recovery cycles are not inserted between bus access cycles and are inserted only after the last bus access cycle of the transfer.

(2) Constraints on using address/data multiplexed bus interface

In the address/data multiplexed I/O space, page accesses are invalid. If a page access setting is specified, the setting is ignored and the normal read or write operation is performed.

Table 15.12 Constraints at the time of normal access

Constraints at the time of normal access	
Reading	**Writing**
CSON[2:0] ≤ CSRWAIT RDON[2:0] ≤ CSRWAIT CSON[2:0] ≤ RDON AWAIT[1:0] + 2 ≤ RDON CSON[2:0] ≤ AWAIT	CSON[2:0] ≤ CSWWAIT WRON[2:0] ≤ CSWWAIT WDON[2:0] ≤ CSWWAIT WDOFF[2:0] ≤ CSWOFF WDON[2:0] ≤ WRON CSON[2:0] ≤ WRON AWAIT[1:0] + 2 ≤ WRON AWAIT[1:0] + 2 ≤ WDON CSON[2:0] ≤ AWAIT

图15.41显示了使用写入缓冲区功能时的操作示例。使用此功能时，如果外部写入后的下一个操作是内部访问，则内部访问与外部写入并行执行，例如无需等待后一个操作完成。

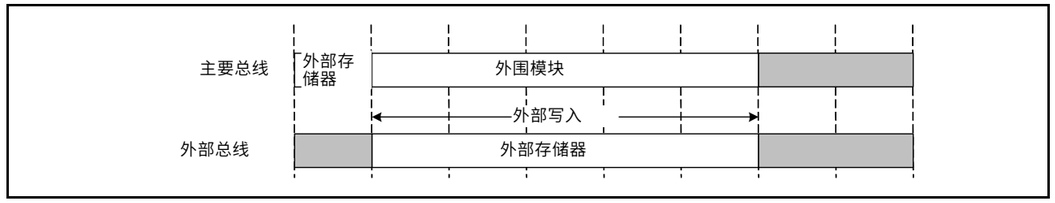


Figure 15.41 使用写入缓冲区功能时的示例操作

15.5.7 Constraints

(1) 使用单独总线接口的限制

表15.11列出了应用于CSn等待控制寄存器1(CSnWCR1)和CSn等待控制中的位的约束
发生正常和页面访问时的寄存器2(CSnWCR2)。

即使CSn模式寄存器中的页面读访问使能位或页面写访问使能位设置为使能（CSnMOD.PRENB=1或CSnMOD.PWENB=1），第一个页面访问或不在范围内的访问页面访问是正常的访问操作。因此，必须满足对正常访问的限制。

Table 15.11 对正常访问和页面访问的限制

正常访问的限制		页面访问限制	
Reading	**Writing**	**Reading**	**Writing**
CSON[2:0] ≤ CSRWAIT RDON[2:0] ≤ CSRWAIT CSON[2:0] ≤ RDON	1 ≤ WDON[2:0] CSON[2:0] ≤ CSWWAIT WRON[2:0] ≤ CSWWAIT WDON[2:0] ≤ CSWWAIT WDOFF[2:0] ≤ CSWOFF WDON[2:0] ≤ WRON CSON[2:0] ≤ WRON	CSON[2:0] ≤ CSPRWAIT RDON[2:0] ≤ CSPRWAIT CSON[2:0] ≤ RDON	1 ≤ WDON[2:0] CSON[2:0] ≤ CSPWWAIT WRON[2:0] ≤ CSPWWAIT WDON[2:0] ≤ CSPWWAIT WDOFF[2:0] ≤ CSWOFF WDON[2:0] ≤ WRON CSON[2:0] ≤ WRON

Note: 当来自总线主机的单个传输请求需要两个或多个外部总线访问周期，并且恢复周期插入条件满足时，启用页面读取访问(CSnMOD.PRENB=1)或启用页面写入访问(CSnMOD.PWENB=1)，恢复周期不在总线访问周期之间插入，仅在传输的最后一个总线访问周期之后插入。

(2) 使用地址数据复用总线接口的限制

在地址数据复用的IO空间中，页面访问是无效的。如果指定了页面访问设置，则忽略该设置并执行正常的读取或写入操作。

Table 15.12 正常访问时的限制

正常访问时的限制	
Reading	**Writing**
CSON[2:0] ≤ CSRWAIT RDON[2:0] ≤ CSRWAIT CSON[2:0] ≤ RDON AWAIT[1:0] + 2 ≤ RDON CSON[2:0] ≤ AWAIT	CSON[2:0] ≤ CSWWAIT WRON[2:0] ≤ CSWWAIT WDON[2:0] ≤ CSWWAIT WDOFF[2:0] ≤ CSWOFF WDON[2:0] ≤ WRON CSON[2:0] ≤ WRON AWAIT[1:0] + 2 ≤ WRON AWAIT[1:0] + 2 ≤ WDON CSON[2:0] ≤ AWAIT

(3) Constraint on pin multiplexing between the A00 and BC0 functions

Setting the single-write strobe mode is prohibited in the 8-bit bus space.

(4) Constraints when BCLK/2 is selected in the EBCLK Pin Output Select bit

When 1/2 cycle of BCLK is selected in the EBCLK Pin Output Select bit, the external bus access cycle starts on the rising edge of the EBCLK pin output. However, when 2 or more external bus access cycles are generated for a single transfer request from a bus master, the second or subsequent external bus access cycle can start on the falling edge of the EBCLK pin output, depending on the wait cycle settings. Set the registers appropriately for the specifications of connected devices.

(5) Instruction code constraint

You must fix the instruction code to little-endian order.

15.6 SDRAM Area Controller Operation

This section describes how the SDRAM area controller (SDRAMC) is enabled and the SDRAM bus width is set, followed by a description of the SDRAMC operations, including read, write, auto-refresh, self-refresh, initialization sequence, and mode register settings.

15.6.1 Enabling/Disabling SDRAM Access and Setting the SDRAM Bus Width

SDRAM access can be enabled or disabled using the SDC Control Register (SDCCR). The SDRAM bus width can also be set using SDCCR. The refresh operation is available even when the operation of the SDRAM address space is disabled, as long as self-refresh or auto-refresh is enabled.

15.6.2 No Access State

When no external address space is accessed, the SDCS, WE, RAS and CAS signals are high.

15.6.3 Insertion of Recovery Cycles

When access to the SDRAM area follows access to the CS area, data recovery cycles are inserted for the CS area controller (CSC). If the number of recovery cycles for the CSC is 0, the ACT command for the next SDRAM access is issued immediately after negation of CSn signal at the earliest. If the number of recovery cycles are not 0, the ACT command is issued 2 cycles after the specified recovery cycle period elapsed after negation of CSn signal at the earliest. Because no data conflicts can occur during access to the SDRAM area, there is no need to set data recovery cycles for the SDRAM (fixed to 0 cycle).

(3) A00和BC0功能之间引脚复用的约束

在8位总线空间中禁止设置单写选通模式。

(4) 在EBCLK引脚输出选择位中选择BCLK2时的约束

当在EBCLK引脚输出选择位选择BCLK的12个周期时，外部总线访问周期在EBCLK引脚输出的上升沿开始。然而，当来自总线主机的单个传输请求产生2个或更多外部总线访问周期时，第二个或随后的外部总线访问周期可以在EBCLK引脚输出的下降沿开始，具体取决于等待周期设置。根据连接设备的规格适当设置寄存器。

(5) 指令码约束

您必须将指令代码修复为little-endian顺序。

15.6 SDRAM区域控制器操作

本节介绍如何启用SDRAM区域控制器(SDRAMC)和设置SDRAM总线宽度，然后描述SDRAMC操作，包括读、写、自动刷新、自刷新、初始化序列和模式寄存器设置.

15.6.1 启用禁用SDRAM访问和设置SDRAM总线宽度

可以使用SDC控制寄存器(SDCCR)启用或禁用SDRAM访问。SDRAM总线宽度也可以使用SDCCR设置。即使禁用了SDRAM地址空间的操作，只要启用自刷新或自动刷新，刷新操作也可用。

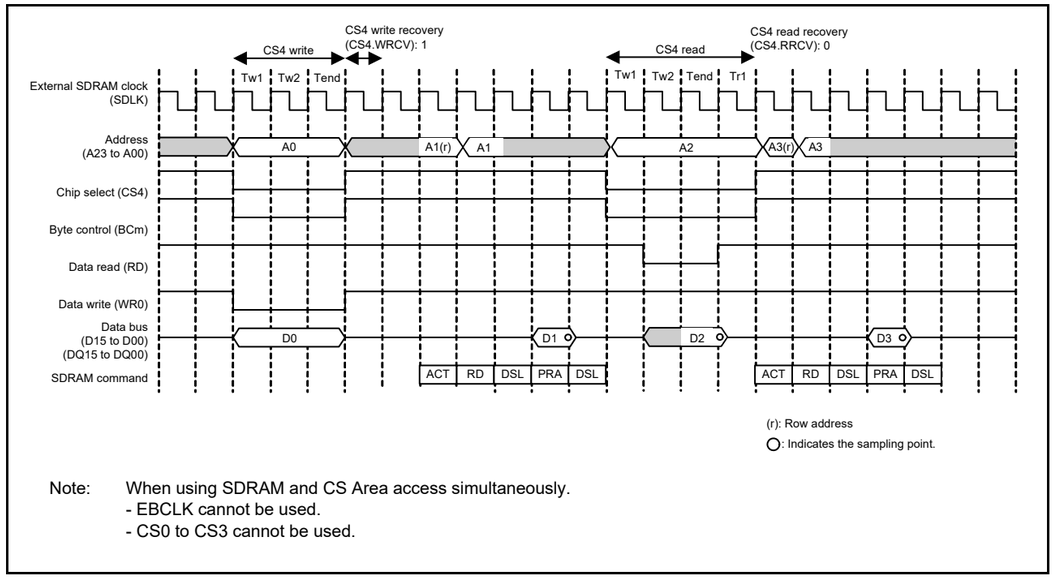
15.6.2 无访问状态

当没有访问外部地址空间时，SDCS、WE、RAS和CAS信号为高电平。

15.6.3 恢复周期的插入

当访问SDRAM区域之后访问CS区域时，为CS区域控制器(CSC)插入数据恢复周期。如果CSC的恢复周期数为0，则最早在CSn信号取反后立即发出下一次SDRAM访问的ACT命令。如果恢复周期数不为0，则最早在CSn信号取反后经过指定的恢复周期周期后2个周期发出ACT命令。由于在访问SDRAM区域的过程中不会发生数据冲突，因此无需为SDRAM区域设置数据恢复周期。

SDRAM (fixed to 0 cycle).



Note: When using SDRAM and CS Area access simultaneously.
- EBCLK cannot be used.
- CS0 to CS3 cannot be used.

Figure 15.42 Example of recovery timing for SDRAM access

15.6.4 Write Buffer Function

In write access, the main bus is released by writing data to the write buffer before access is complete. This allows the next round of bus access to start. However, if the next access is to an external address space or to a register of the external bus controller, it is suspended until the external bus operations already in progress are complete.

15.6.5 SDRAM Commands

To control the SDRAM, the SDRAMC issues a command for each bus cycle. Commands are defined by a combination of the SDCS, RAS, CAS, WE, CKE, and other signals. Table 15.13 lists the commands issued by the SDRAMC.

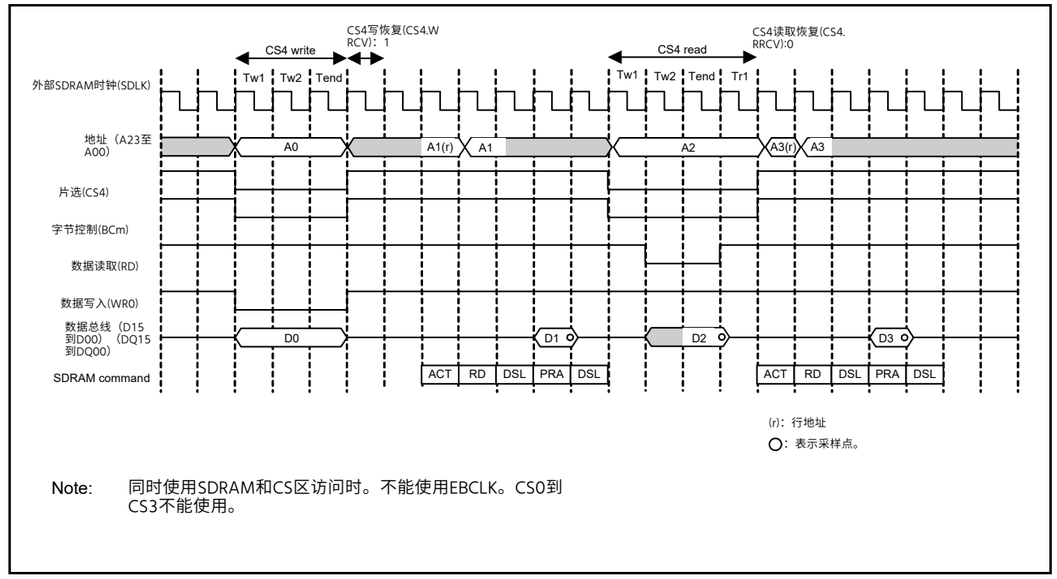
Table 15.13 SDRAMC commands

							CKE			
Name	**Abbreviation**	**Command**	**SDCS**	**RAS**	**CAS**	**WE**	**n-1**	**n**	**BA1**	**BA0**
DESL	DSL	Device deselect	H	x	x	x	H	x	x	x
ACTV	ACT	Bank active	L	L	H	H	H	x	V	V
READ	RD	Read	L	H	L	H	H	x	V	V
WRIT	WRI	Write	L	H	L	L	H	x	V	V
PALL	PRA	All bank precharge	L	L	H	L	H	x	x	x
REF	RFA	Auto-refresh	L	L	L	H	H	x	x	x
MRS	MRS	Mode register set	L	L	L	L	H	x	L	L
SELF	RFS	Self-refresh entry	L	L	L	H	H	L	x	x
SELFX	RFX	Self-refresh end	H	x	x	x	L	H	x	x

Note: H = high level, L = low level, V = valid, x = don't care.
n = command issue cycle, n - 1 = 1 cycle before the command is issued.

15.6.6 Conditions for Setting the SDRAMC Registers

The SDRAMC registers must only be modified when all the conditions shown in Table 15.14 are satisfied.



Note: 同时使用SDRAM和CS区访问时。不能使用EBCLK。CS0到CS3不能使用。

Figure 15.42 SDRAM访问的恢复时序示例

15.6.4 写缓冲功能

在写访问中，通过在访问完成之前将数据写入写缓冲区来释放主总线。这允许下一轮总线访问开始。然而，如果下一次访问是对外部地址空间或外部总线控制器的寄存器，则它会被挂起，直到已经在进行中的外部总线操作完成。

15.6.5 SDRAM Commands

为了控制SDRAM，SDRAMC为每个总线周期发出一个命令。命令由SDCS、RAS、CAS、WE、CKE和其他信号的组合定义。表15.13列出了SDRAMC发出的命令。

Table 15.13 SDRAMC commands

							CKE			
Name	**Abbreviation**	**Command**	**SDCS**	**RAS**	**CAS**	**WE**	**n-1**	**n**	**BA1**	**BA0**
DESL	DSL	设备取消选择	H	x	x	x	H	x	x	x
ACTV	ACT	银行活跃	L	L	H	H	H	x	V	V
READ	RD	Read	L	H	L	H	H	x	V	V
WRIT	WRI	Write	L	H	L	L	H	x	V	V
PALL	PRA	所有银行预充	L	L	H	L	H	x	x	x
REF	RFA	Auto-refresh	L	L	L	H	H	x	x	x
MRS	MRS	模式寄存器组	L	L	L	L	H	x	L	L
SELF	RFS	Self-refresh entry	L	L	L	H	H	L	x	x
SELFX	RFX	Self-refresh end	H	x	x	x	L	H	x	x

Note: H=高电平，L=低电平，V=有效，x=无关。n=命令发出周期，n1=发出命令前的1个周期。

15.6.6 设置SDRAMC寄存器的条件

仅当满足表15.14中所示的所有条件时，才必须修改SDRAMC寄存器。

Table 15.14 Conditions for register modification

Function or operation	Registers	Conditions
Self-refresh	SDSELF*1	• SDRAM access is disabled (SDCCR.EXENB = 0*2) • Auto-refresh operation is enabled (SDRFEN.RFEN = 1).
Auto-refresh	SDRFCR	Self-refresh operation is disabled (SDSELF.SFEN = 0)
	SDRFEN	• SDRAM access is disabled (SDCCR.EXENB = 0*2) • Self-refresh operation is disabled (SDSELF.SFEN = 0).
Initialization sequence	SDIR*1	SDICR is not set yet, and the same conditions as for SDICR modification are satisfied
	SDICR*1	• SDRAM access is disabled (SDCCR.EXENB = 0*2) • Auto-refresh operation is disabled (SDRFEN.RFEN = 0) • Self-refresh operation is disabled (SDSELF.SFEN = 0).
Address register	SDADR	• SDRAM access is disabled (SDCCR.EXENB = 0*2) • Auto-refresh operation is disabled (SDRFEN.RFEN = 0) • Self-refresh operation is disabled (SDSELF.SFEN = 0).
Timing register	SDTR	• Self-refresh operation is in progress (SDSELF.SFEN = 1) or • SDRAM access is disabled (SDCCR.EXENB = 0*2) • Auto-refresh operation is disabled (SDRFEN.RFEN = 0) • Self-refresh operation is disabled (SDSELF.SFEN = 0).
Mode register	SDMOD*1	• SDRAM access is disabled (SDCCR.EXENB = 0*2) • Self-refresh operation is disabled (SDSELF.SFEN = 0).
Access mode register	SDAMOD	• SDRAM access is disabled (SDCCR.EXENB = 0*2) • Auto-refresh operation is disabled (SDRFEN.RFEN = 0) • Self-refresh operation is disabled (SDSELF.SFEN = 0).

Note 1. Before modifying this register, confirm that all the status bits in SDSR are 0.
Note 2. After writing 0 to the EXENB bit, confirm that it is cleared to 0.

15.6.7 Self-Refresh

Transition to or recovery from self-refresh mode is controlled with the SDRAM Self-Refresh Control Register (SDSELF). Immediately before the transition to self-refresh mode, an auto-refresh operation is performed. In self-refresh mode, the CKE signal is low. Immediately after recovery from self-refresh mode, the auto-refresh cycle starts.

Figure 15.43 and Figure 15.44 show timing examples of the transition to and recovery from self-refresh mode.

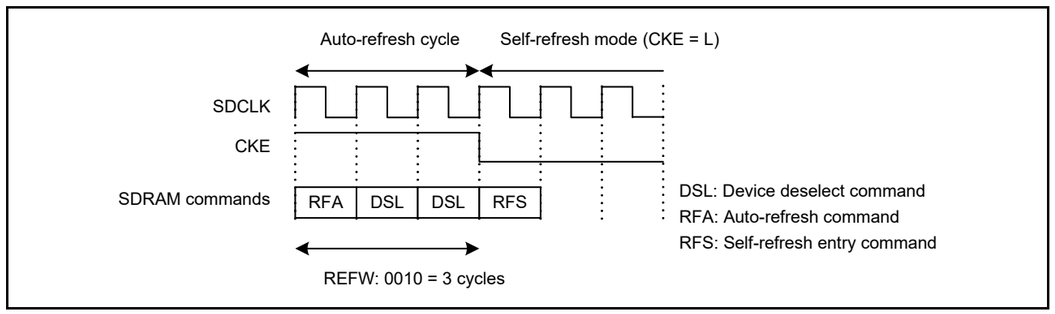


Figure 15.43 Example timing for transition to self-refresh mode when SDRFCR.REFW[3:0] = 0010b (3 cycles)

Table 15.14 寄存器修改条件

功能或操作	Registers	Conditions
Self-refresh	SDSELF*1	禁用SDRAM访问(SDCCR.EXENB=0*2) 启用自动刷新操作(SDRFEN.RFEN=1)。
Auto-refresh	SDRFCR	自刷新操作被禁用(SDSELF.SFEN=0)
	SDRFEN	禁用SDRAM访问(SDCCR.EXENB=0*2) 禁用自刷新操作(SDSELF.SFEN=0)。
初始化序列	SDIR*1	SDICR尚未设置，满足与SDICR修改相同的条件
	SDICR*1	禁用SDRAM访问(SDCCR.EXENB=0*2) 禁用自动刷新操作(SDRFEN.RFEN=0) 禁用自刷新操作(SDSELF.SFEN=0)。
地址寄存器	SDADR	禁用SDRAM访问(SDCCR.EXENB=0*2) 禁用自动刷新操作(SDRFEN.RFEN=0) 禁用自刷新操作(SDSELF.SFEN=0)。
定时寄存器	SDTR	自刷新操作正在进行(SDSELF.SFEN=1)或 SDRAM访问已禁用(SDCCR.EXENB=0*2) 自动刷新操作已禁用(SDRFEN.RFEN=0) 自刷新操作已禁用禁用 （SDSELF.SFEN=0）。
模式寄存器	SDMOD*1	禁用SDRAM访问(SDCCR.EXENB=0*2) 禁用自刷新操作(SDSELF.SFEN=0)。
访问模式寄存器	SDAMOD	禁用SDRAM访问(SDCCR.EXENB=0*2) 禁用自动刷新操作(SDRFEN.RFEN=0) 禁用自刷新操作(SDSELF.SFEN=0)。

Note 1. 修改此寄存器前，请确认SDSR中的所有状态位均为0。
Note 2. 将0写入EXENB位后，确认它被清除为0。

15.6.7 Self-Refresh

自刷新模式的转换或恢复由SDRAM自刷新控制寄存器(SDSELF)控制。就在转换到自刷新模式之前，执行自动刷新操作。在自刷新模式下，CKE信号为低电平。从自刷新模式恢复后，自动刷新周期立即开始。

图15.43和图15.44显示了从自刷新模式转换和恢复的时序示例。

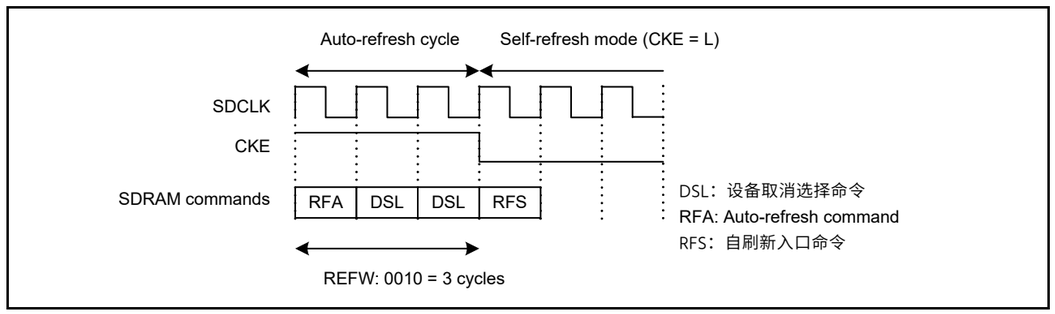


Figure 15.43 当SDRFCR.REFW[3:0]=0010b（3个周期）时转换到自刷新模式的示例时序

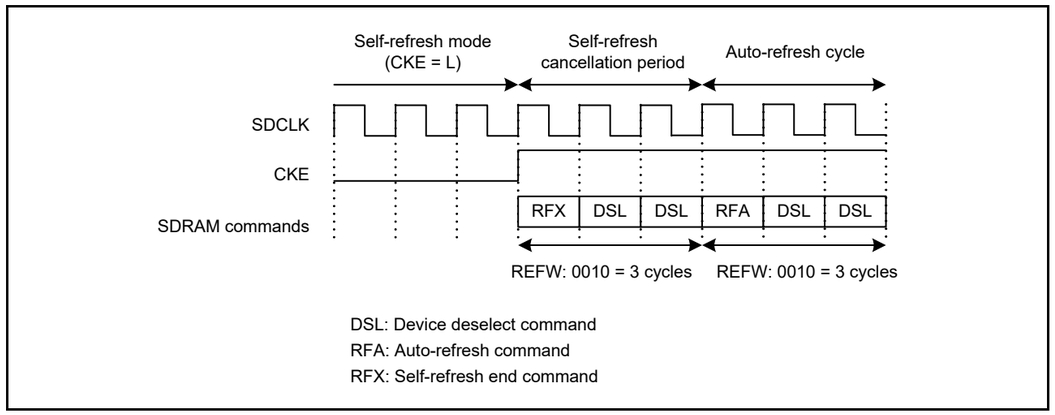


Figure 15.44 Example timing for recovery from self-refresh mode

(1) Self-refresh in Software Standby mode

When invoking self-refresh in Software Standby mode, first follow the procedure shown in section 15.6.11.2, Procedure for transitioning to and recovering from self-refresh mode. Next set up the transition to Software Standby mode. In this mode, set the Output Port Enable bit (OPE) in the Standby Control Register (SBYCR) to 1 to hold the output state of the address bus and bus control signals.

After canceling Software Standby mode, follow the procedure shown in section 15.6.11.2, Procedure for transitioning to and recovering from self-refresh mode. For details on invoking and canceling Software Standby mode, see section 11, Low Power Modes.

(2) Self-refresh in Deep Software Standby mode

Deep Software Standby mode is invoked from within Software Standby mode. On this transition, the pin states remain unchanged. Therefore, invoking of self-refresh in Deep Software Standby mode can be handled the same as for Software Standby mode with one additional setting. You must also set the I/O Port Keep bit (IOKEEP) in the Deep Software Standby mode Control Register (DPSBYCR) to 1.

Because the SDRAMC is reset internally when Deep Software Standby mode is canceled, the SDRAM control registers must be set again. After canceling Software Standby mode, follow the procedure in this section to cancel self-refresh.

Figure 15.45 shows self-refresh timing in Deep Software Standby mode. For details on invoking and canceling Deep Software Standby mode, see section 11, Low Power Modes.

To cancel self-refresh mode:

1. Set DPSBYCR.IOKEEP to 1 to keep the CKE signal output low in Deep Software Standby mode.
2. Start the clock supply to the SDRAMC.
3. Set the SDRAM control registers (SDCMOD, SDAMOD, SDADR, and SDTR) again. These registers were initialized by an internal reset on entering Deep Software Standby mode.
4. Enable an auto-refresh operation by setting SDRFEN.RFEN to 1.
5. Check that all the status bits in SDSR are cleared to 0 and set SDSELF.SFEN to 1 to select self-refresh mode again.
6. Modify the port settings for the SDRAM interface.
7. Set SDCKOCR.SDCKOEN to 1 to start the clock supply to the SDRAM with the SDCLK pin.
8. Check that all the status bits in SDSR are cleared to 0 and set SDSELF.SFEN to 0 to cancel self-refresh mode.

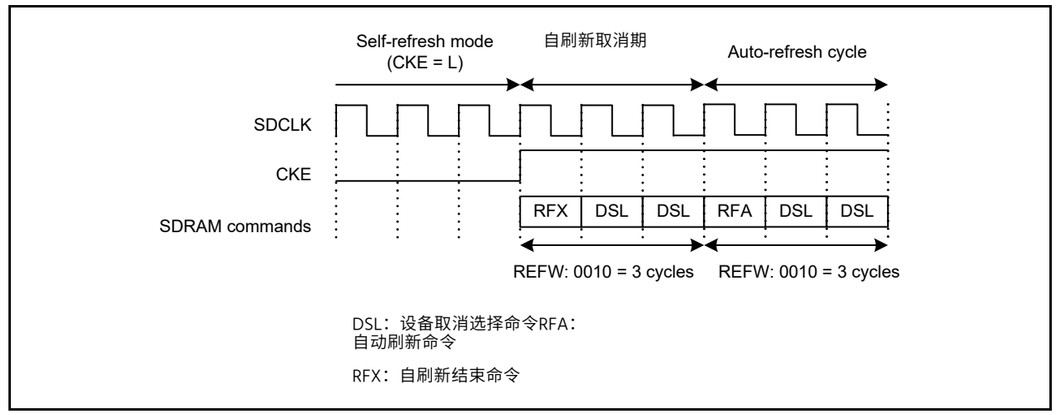


Figure 15.44 从自刷新模式恢复的示例时序

(1) 软件待机模式下的自刷新

在软件待机模式下调用自刷新时，首先按照第15.6.11.2节，转换到自刷新模式和从自刷新模式恢复的过程中所示的过程。接下来设置到软件待机模式的转换。在此模式下，将待机控制寄存器(SBYCR)中的输出端口使能位(OPE)设置为1，以保持地址总线和总线控制信号的输出状态。

取消软件待机模式后，按照第15.6.11.2节，转换到自刷新模式和从自刷新模式恢复的过程中所示的过程。有关调用和取消软件待机模式的详细信息，请参阅第11节，低功耗模式。

(2) 深度软件待机模式下的自刷新

深度软件待机模式是从软件待机模式中调用的。在此转换中，引脚状态保持不变。因此，在深度软件待机模式下调用自刷新的处理方式与软件待机模式相同，但需要增加一项设置。您还必须在DeepSoftware中设置IO端口保持位(IOKEEP)

待机模式控制寄存器(DPSBYCR)为1。

因为当深度软件待机模式被取消时SDRAMC在内部复位，所以必须重新设置SDRAM控制寄存器。取消软件待机模式后，按照本节中的步骤取消自刷新。

图15.45显示了深度软件待机模式下的自刷新时序。有关调用和取消Deep的详细信息
软件待机模式，请参见第11节，低功耗模式。

取消自刷新模式：

1. 将DPSBYCR.IOKEEP设置为1，以在深度软件待机模式下保持CKE信号输出为低电平。
2. 开始向SDRAMC提供时钟。
3. 再次设置SDRAM控制寄存器（SDCMOD、SDAMOD、SDADR和SDTR）。这些寄存器在进入深度软件待机模式时通过内部复位进行初始化。
4. 通过将SDRFEN.RFEN设置为1来启用自动刷新操作。
5. 检查SDSR中的所有状态位是否被清除为0并将SDSELF.SFEN设置为1以再次选择自刷新模式。
6. 修改SDRAM接口的端口设置。
7. 将SDCKOCR.SDCKOEN设置为1以使用SDCLK 引脚开始向SDRAM提供时钟。
8. 检查SDSR中的所有状态位是否被清除为0，并将SDSELF.SFEN设置为0以取消自刷新模式。

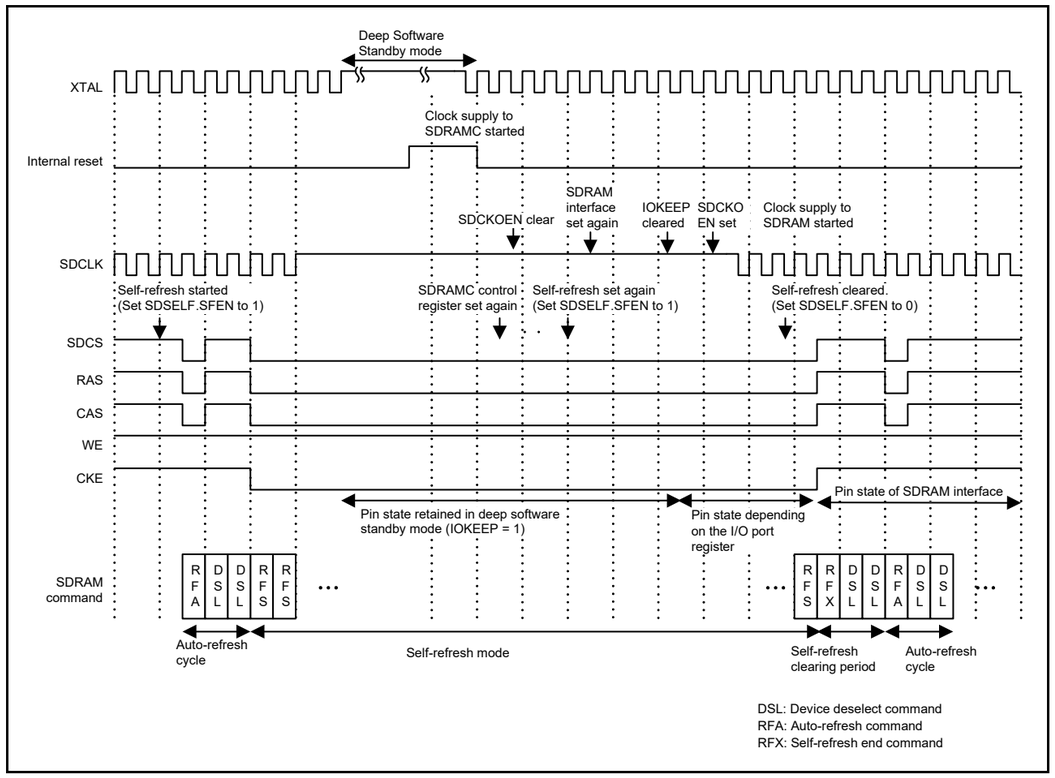


Figure 15.45 Example timing for self-refresh cycle in Deep Software Standby mode

15.6.8 Auto-Refresh

The auto-refresh cycle can be started by setting the Auto-Refresh Operation Enable bit (RFEN) in the SDRAM Auto-Refresh Control Register (SDRFEN) to 1. After the cycle starts, refresh requests are generated at fixed intervals determined by the refresh counter. However, because refresh requests are not accepted during read or write access, the auto-refresh cycle might be suspended. If an auto-refresh request is issued during consecutive accesses to the SDRAM, the auto-refresh cycle starts after completion of the bus access in response to a single transfer request from the bus master.

If an SDRAM access and a refresh request are generated at the same time, the refresh request takes precedence. A CS area access and a refresh request can be made at the same if the SDCS, RAS, CAS, WE, and CKE signals, which are required for issuing the refresh command, are exclusively provided for SDRAM access.

The refresh counter is halted during a self-refresh operation. After recovery from the self-refresh mode, the auto-refresh cycle starts and the counter value is reset, resuming the counter operation.

Figure 15.46 shows a timing example of an auto-refresh cycle.

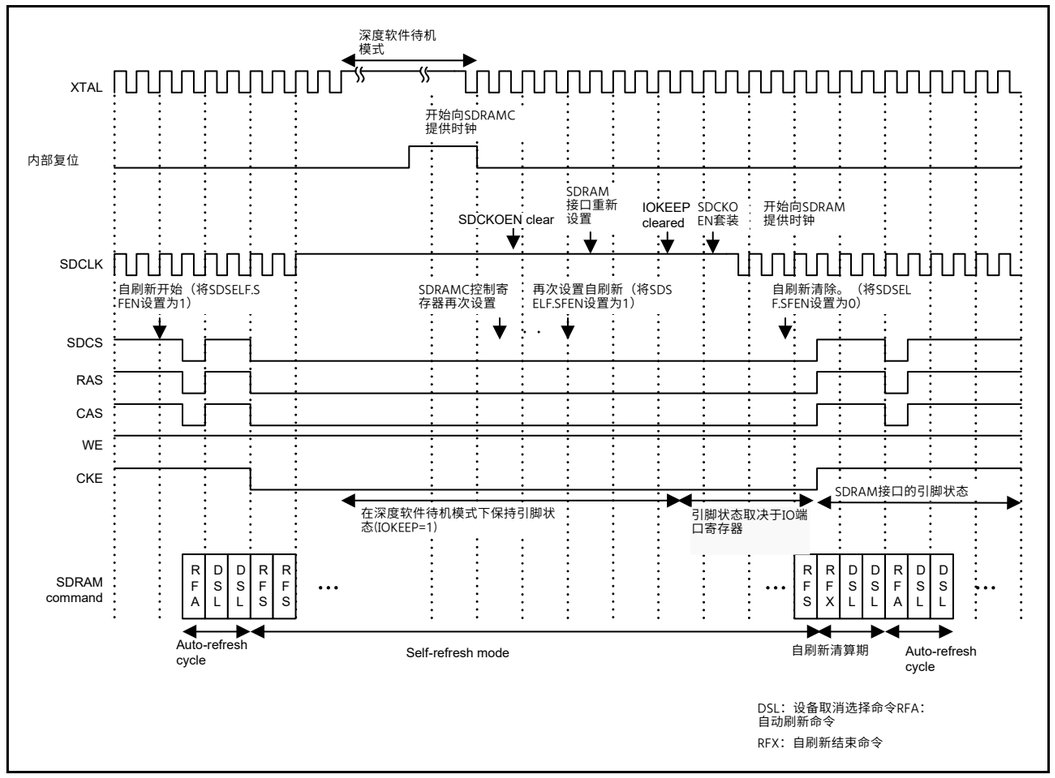


Figure 15.45 深度软件待机模式下自刷新周期的示例时序

15.6.8 Auto-Refresh

自动刷新周期可以通过设置SDRAMAuto中的自动刷新操作使能位(RFEN)来启动刷新控制寄存器(SDRFEN)为1。循环开始后，刷新请求以由刷新计数器确定的固定间隔生成。但是，由于在读取或写入访问期间不接受刷新请求，因此可能会暂停自动刷新周期。如果在对SDRAM的连续访问期间发出自动刷新请求，则自动刷新周期在总线访问完成后开始，以响应来自总线主机的单个传输请求。

如果同时产生SDRAM访问和刷新请求，则刷新请求优先。如果发出刷新命令所需的SDCS、RAS、CAS、WE和CKE信号专门用于SDRAM访问，则可以同时进行CS区域访问和刷新请求。

刷新计数器在自刷新操作期间停止。从自刷新模式恢复后，自动刷新周期开始，计数器值复位，恢复计数器操作。

图15.46显示了自动刷新周期的时序示例。

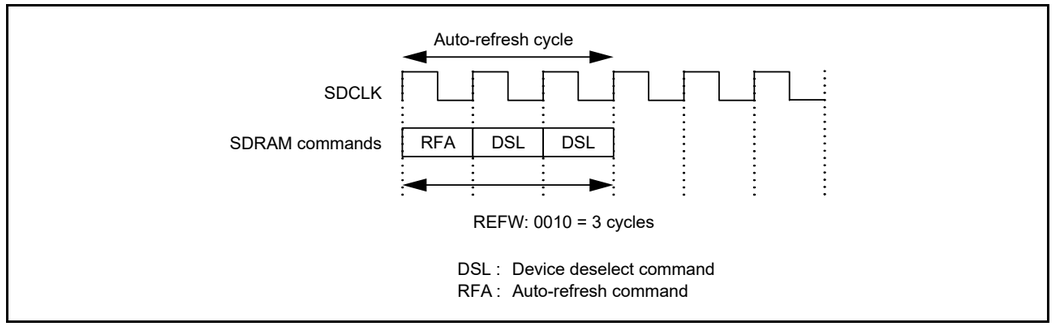


Figure 15.46 Example timing for auto-refresh cycle (1)

Figure 15.47 and Figure 15.48 show examples of operation when an auto-refresh request is generated during single access and continuous access.

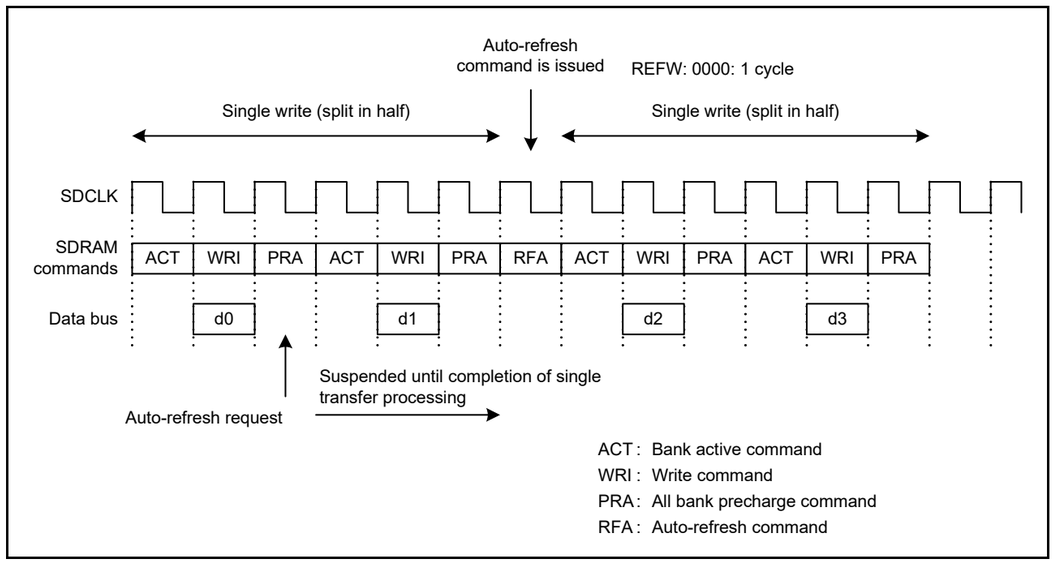


Figure 15.47 Example timing for auto-refresh cycle (2), when the auto-refresh request is made during single access

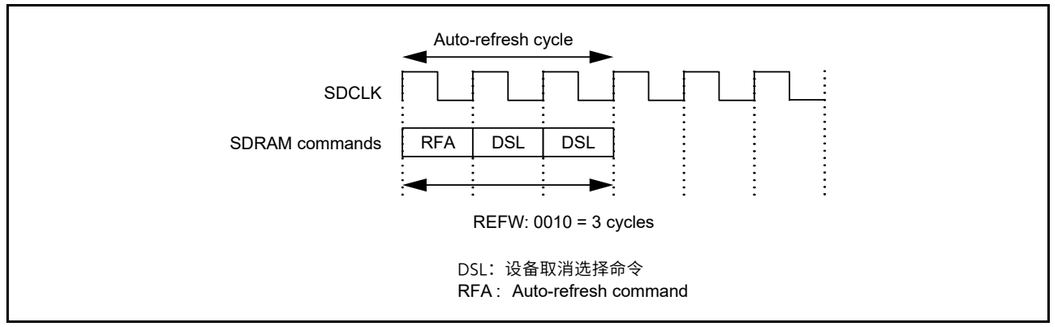


Figure 15.46 自动刷新周期的示例时序(1)

图15.47和图15.48显示了在单次访问和连续访问期间生成自动刷新请求时的操作示例。

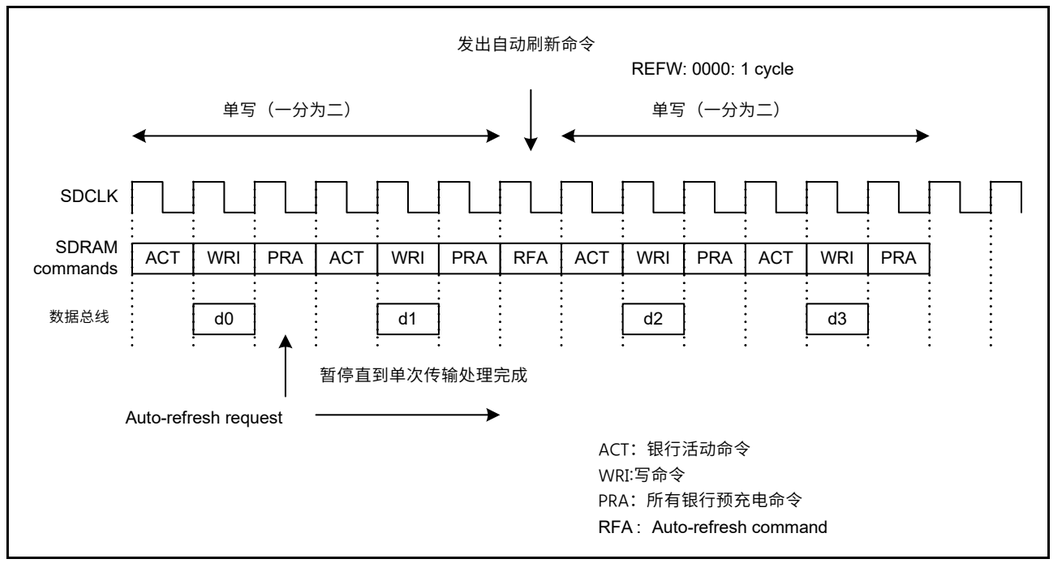


Figure 15.47 自动刷新周期的示例时序(2)，在单次访问期间发出自动刷新请求时

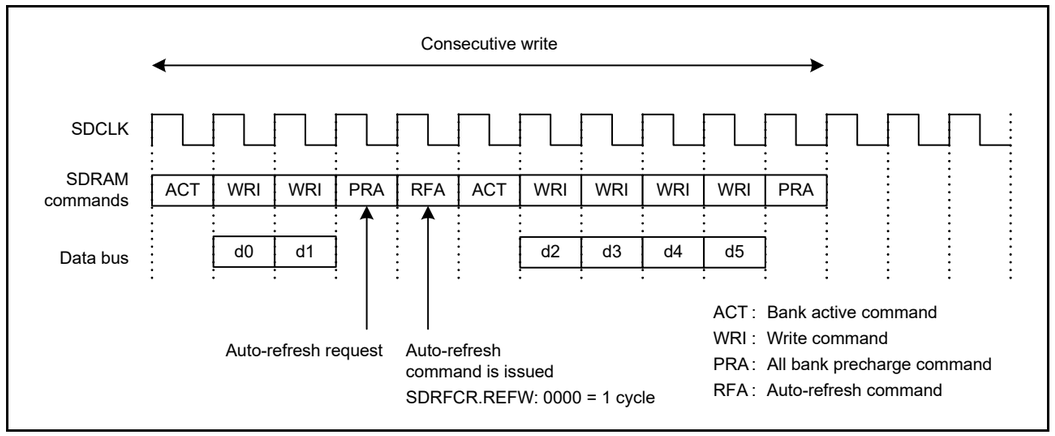


Figure 15.48 Example timing for auto-refresh cycle (3) when auto-refresh request is made during continuous access

15.6.9 Initialization Sequencer

The SDRAMC has a sequencer to issue SDRAM initialization commands. After a reset, the initialization sequencer must be activated without fail. Operation is not guaranteed if the SDRAM is not initialized.

The SDRAM initialization sequencer issues an all-bank precharge command followed by auto-refresh commands n times, where n = 1 to 15. The SDRAM initialization sequence timing can be set using the SDRAM Initialization Register (SDIR). The SDRAM initialization sequence can be activated using the SDRAM Initialization Sequence Control Register (SDICR). These registers must be set only when the conditions listed in Table 15.14 are satisfied.

Figure 15.49 shows a timing example of the SDRAM initialization sequence. When the ARFC[3:0] bits in SDIR are set so that auto-refresh operation is performed two or more times, auto-refresh cycles are repeated in the initialization sequence accordingly.

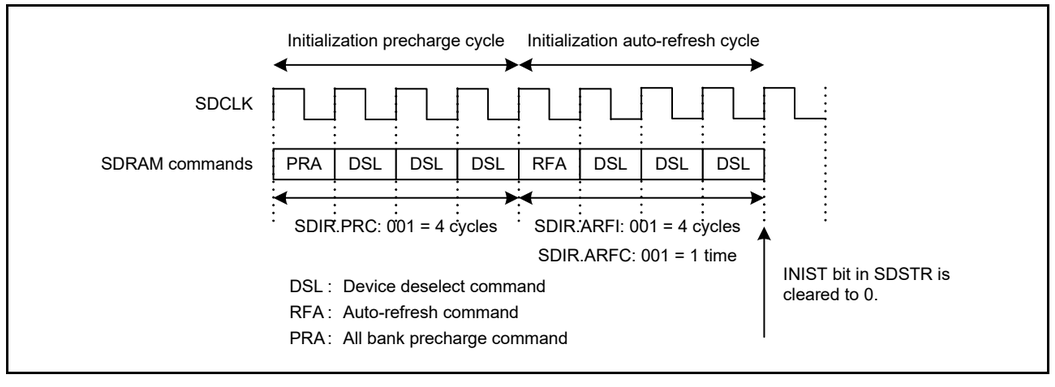


Figure 15.49 Example timing for SDRAM initialization sequence

15.6.10 Setting the Mode Register

Setting the SDRAM Mode Register (SDMOD) allows the mode register set command to be issued to the SDRAM and the value set in the MR[14:0] bits in SDMOD to be output to the lower bits of the address, specifically to A14 to A00 for 8-bit bus width or A15 to A01 for 16-bit bus width. Before setting the mode register, set the SDRAM Bus Width Select bits in the SDC Control Register (SDCCR.BSIZE[1:0]) to determine the data bus width of the SDRAM.

Figure 15.50 shows the mode register setting timing.

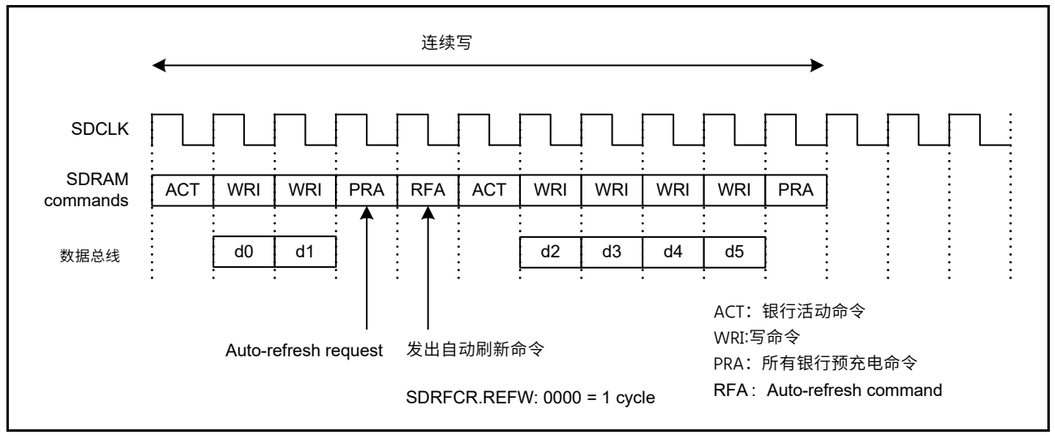


Figure 15.48 连续访问期间发出自动刷新请求时的自动刷新周期示例时序(3)

15.6.9 初始化排序器

SDRAMC有一个定序器来发出SDRAM初始化命令。复位后，初始化定序器必须正确激活。如果SDRAM未初始化，则无法保证操作。

SDRAM初始化序列器发出一个全存储体预充电命令，随后发出n次自动刷新命令，其中n=1到15。可以使用SDRAM初始化寄存器(SDIR)设置SDRAM初始化序列时序。SDRAM初始化序列可以使用SDRAM初始化序列控制寄存器(SDICR)激活。只有当满足表15.14中列出的条件时，才必须设置这些寄存器。

图15.49显示了SDRAM初始化序列的时序示例。当SDIR中的ARFC[3:0]位设置为自动刷新操作执行两次或更多次时，自动刷新周期在初始化序列中相应地重复。

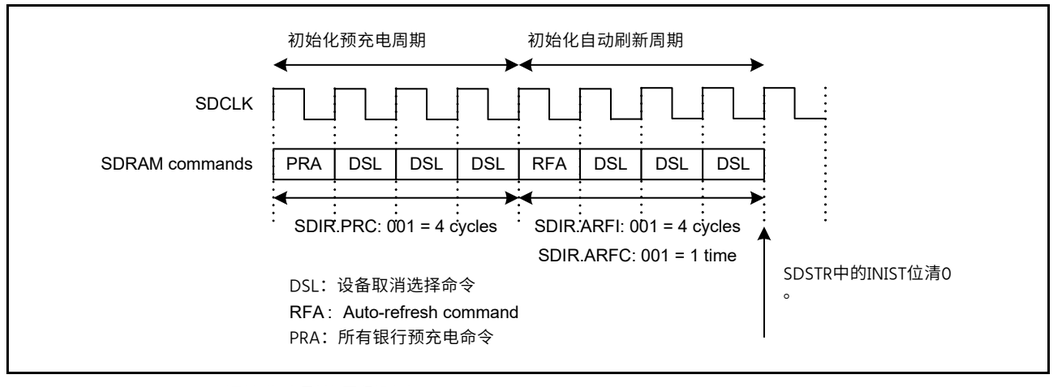


Figure 15.49 SDRAM初始化序列的示例时序

15.6.10 设置模式寄存器

设置SDRAM模式寄存器(SDMOD)允许向SDRAM发出模式寄存器设置命令，并将SDMOD中MR[14:0]位中设置的值输出到地址的低位，具体到A14以A00用于8位总线宽度或A15至A01用于16位总线宽度。在设置模式寄存器之前，先设置SDC控制寄存器中的SDRAM总线宽度选择位（SDCCR.BSIZE[1:0]），以确定SDRAM的数据总线宽度。

图15.50显示了模式寄存器设置时序。

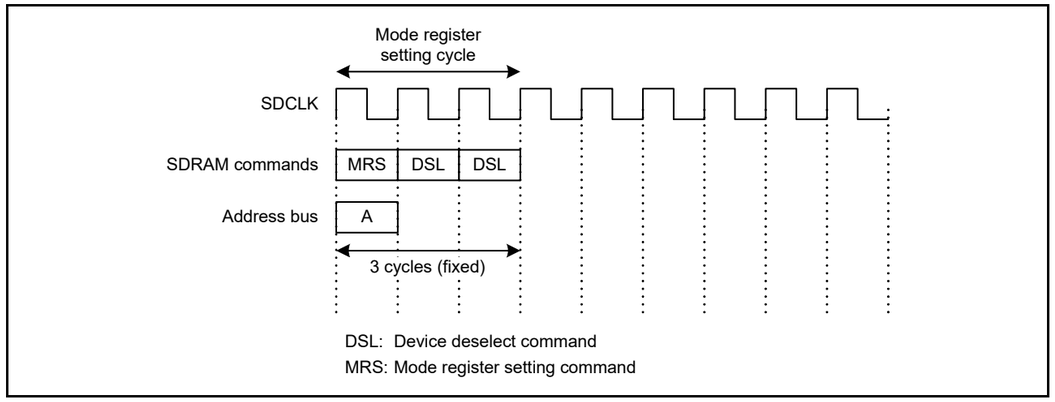


Figure 15.50 Mode register setting timing

15.6.11 SDRAMC Setting Examples

This section describes the following:

- SDRAMC setting procedure
- Timing register setting examples
- Procedure for transitioning to and recovering from self-refresh mode.

15.6.11.1 SDRAMC access procedure

Figure 15.51 shows the SDRAMC setting procedure.

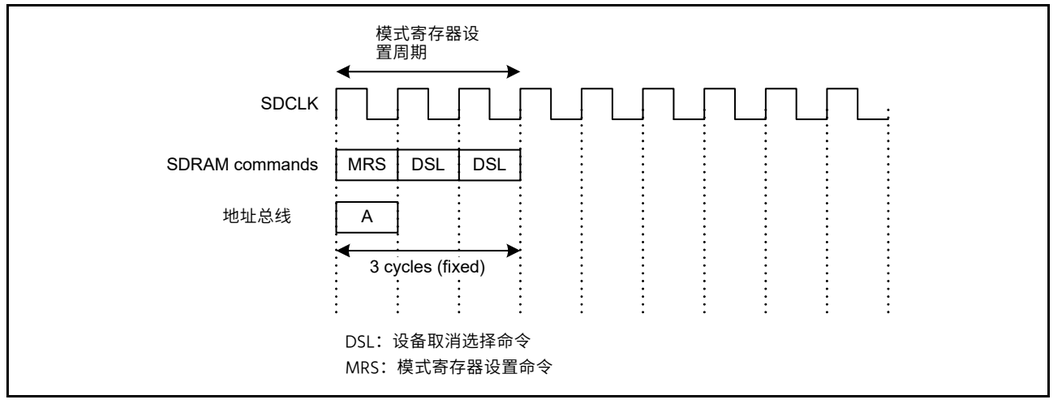


Figure 15.50 模式寄存器设置时序

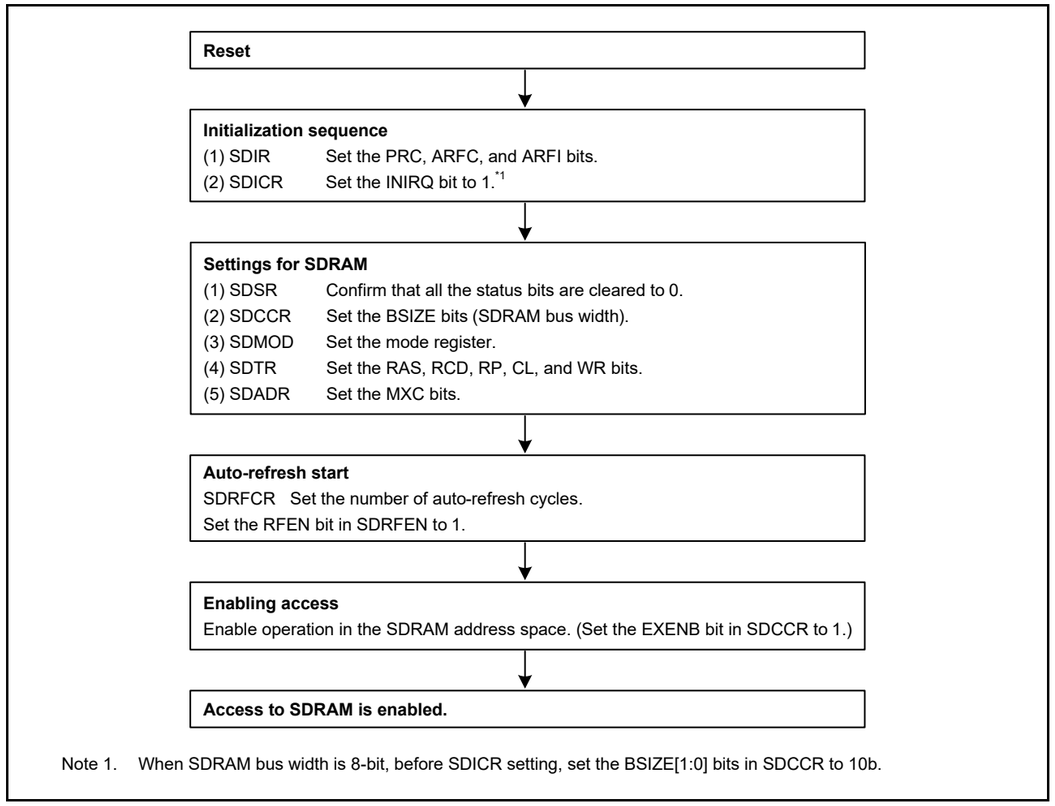
15.6.11 SDRAMC设置示例

本节介绍以下内容：

- SDRAMC设定程序
- 时序寄存器设置示例
- 转换到自刷新模式和从自刷新模式恢复的过程。

15.6.11.1 SDRAMC访问程序

图15.51显示了SDRAMC设置过程。

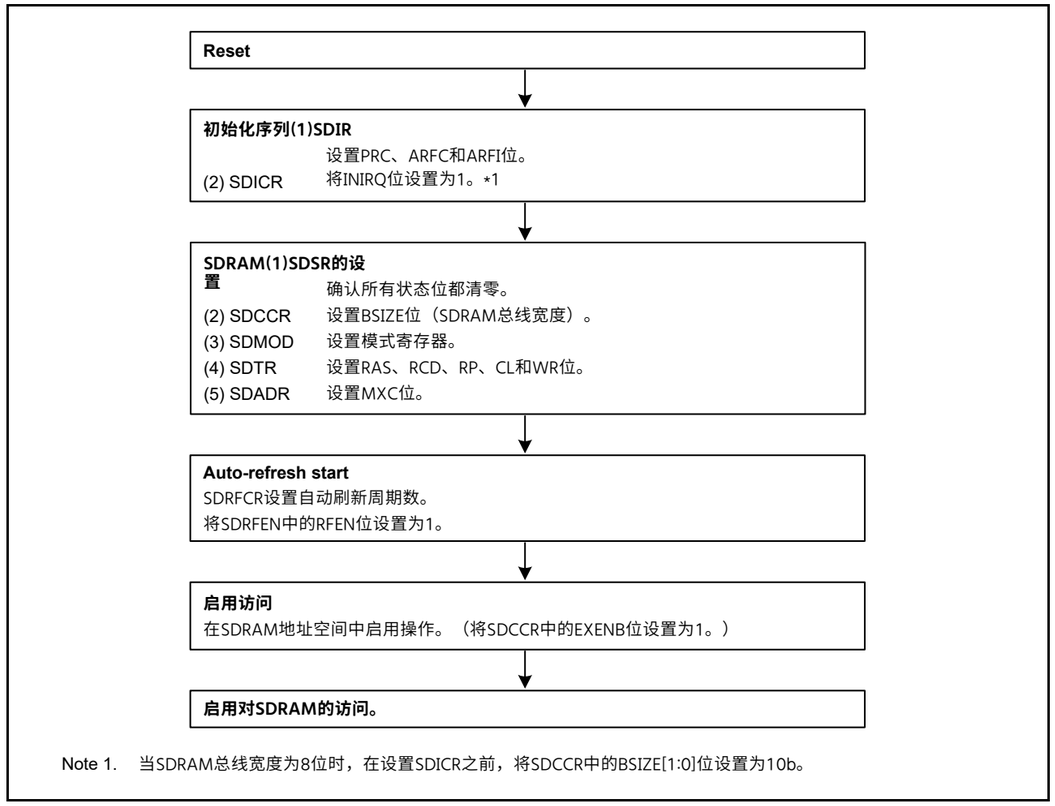


Note 1. When SDRAM bus width is 8-bit, before SDICR setting, set the BSIZE[1:0] bits in SDCCR to 10b.

Figure 15.51 SDRAMC setting procedure

15.6.11.2 Procedure for transitioning to and recovering from self-refresh mode

Figure 15.52 shows the procedure for transitioning to and recovering from self-refresh mode.



Note 1. 当SDRAM总线宽度为8位时，在设置SDICR之前，将SDCCR中的BSIZE[1:0]位设置为10b。

Figure 15.51 SDRAMC设定程序

15.6.11.2 转换到自刷新模式和从自刷新模式恢复的过程

图15.52显示了转换到自刷新模式和从自刷新模式恢复的过程。

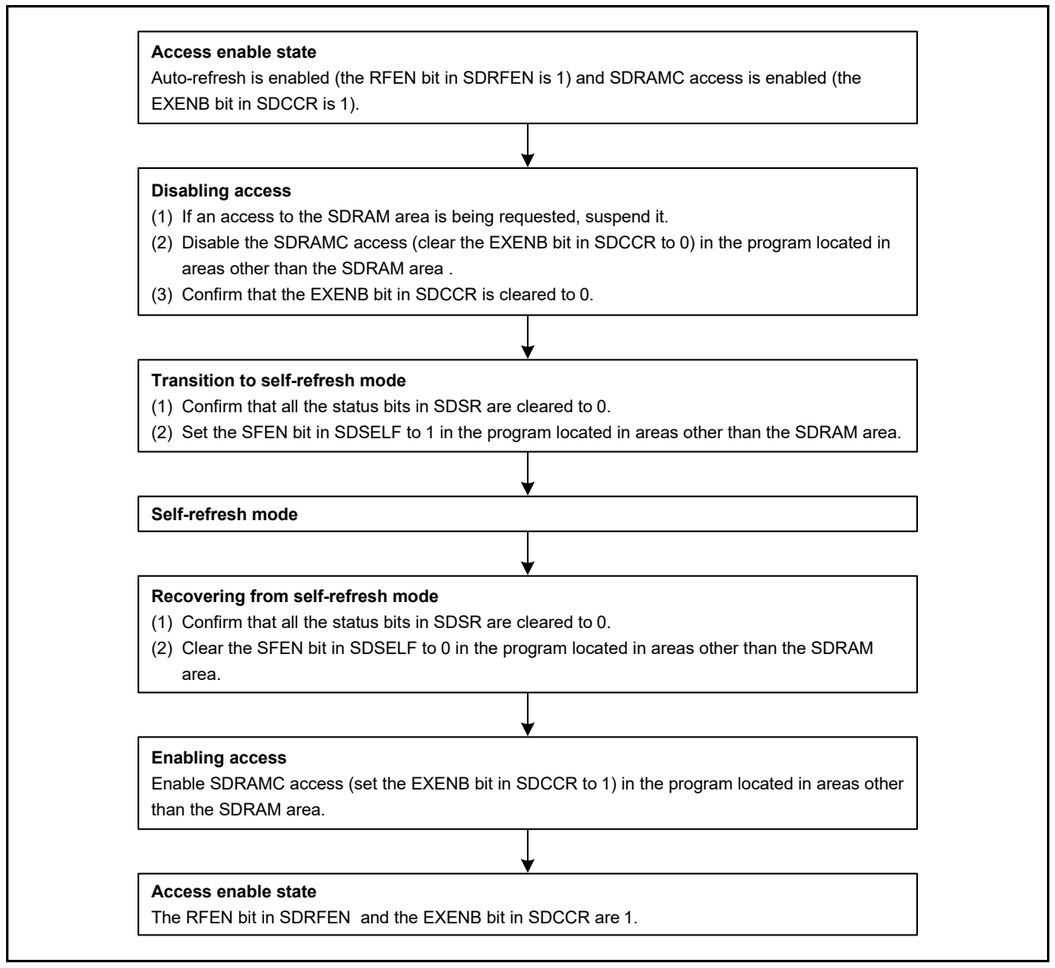


Figure 15.52 Procedure for transitioning to and recovering from self-refresh mode

Note: Self-refresh mode cannot be invoked during SDRAM access. SDRAM access must be disabled during both transition to and recovery from self-refresh mode. Follow the programming instructions shown in Figure 15.53.
Before transitioning to self-refresh mode, disable access to the SDRAM area.
During transition to self-refresh mode, self-refresh operation, and recovery from self-refresh mode, do not allow any operand access or instruction fetch, including prefetch to the SDRAM area, to be generated.

Figure 15.53 shows the procedure for transitioning to and recovering from self-refresh mode in Deep Software Standby mode.

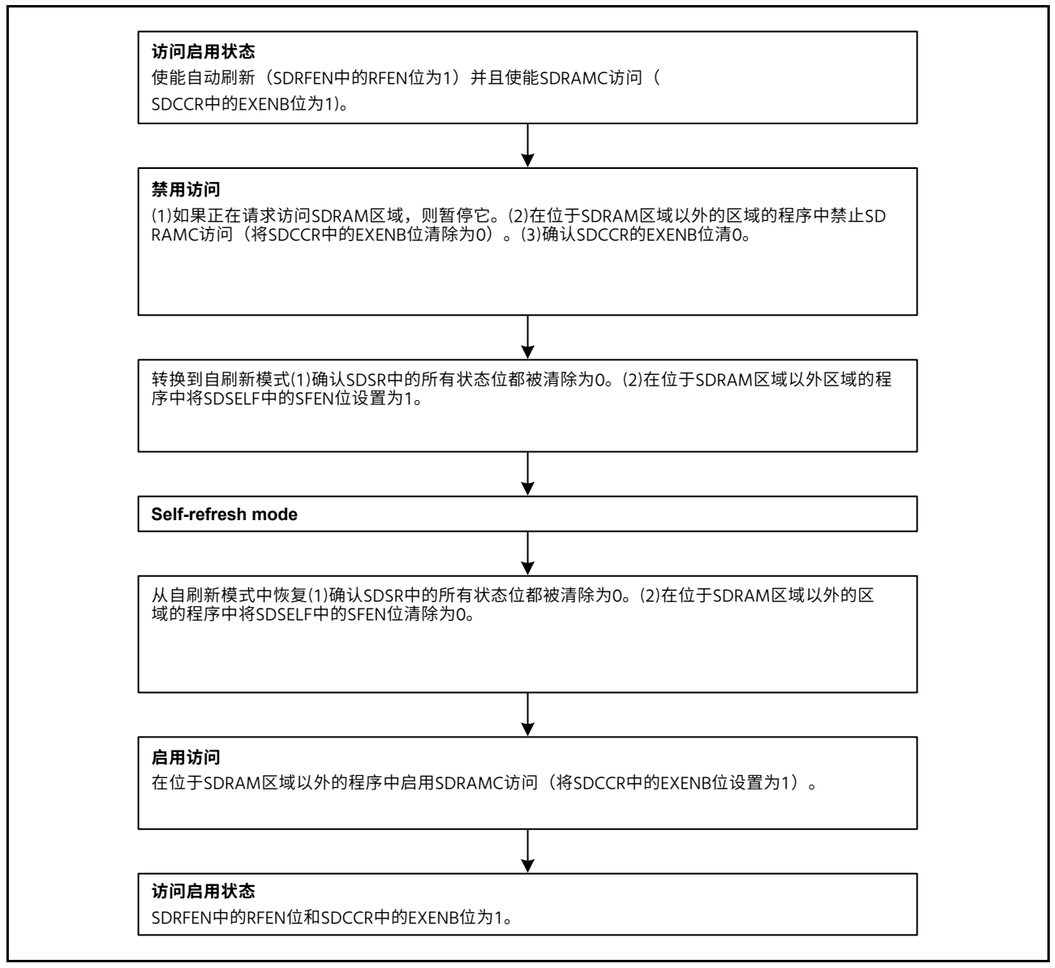


Figure 15.52 转换到自刷新模式和从自刷新模式恢复的过程

Note: 在SDRAM访问期间不能调用自刷新模式。在转换到自刷新模式和从自刷新模式恢复期间，必须禁用SDRAM访问。按照图15.53所示的编程说明进行操作。在转换到自刷新模式之前，禁用对SDRAM区域的访问。

在转换到自刷新模式、自刷新操作和从自刷新模式恢复期间，不允许生成任何操作数访问或指令提取，包括对SDRAM区域的预取。

图15.53显示了在深度软件待机模式下转换到自刷新模式并从中恢复的过程。

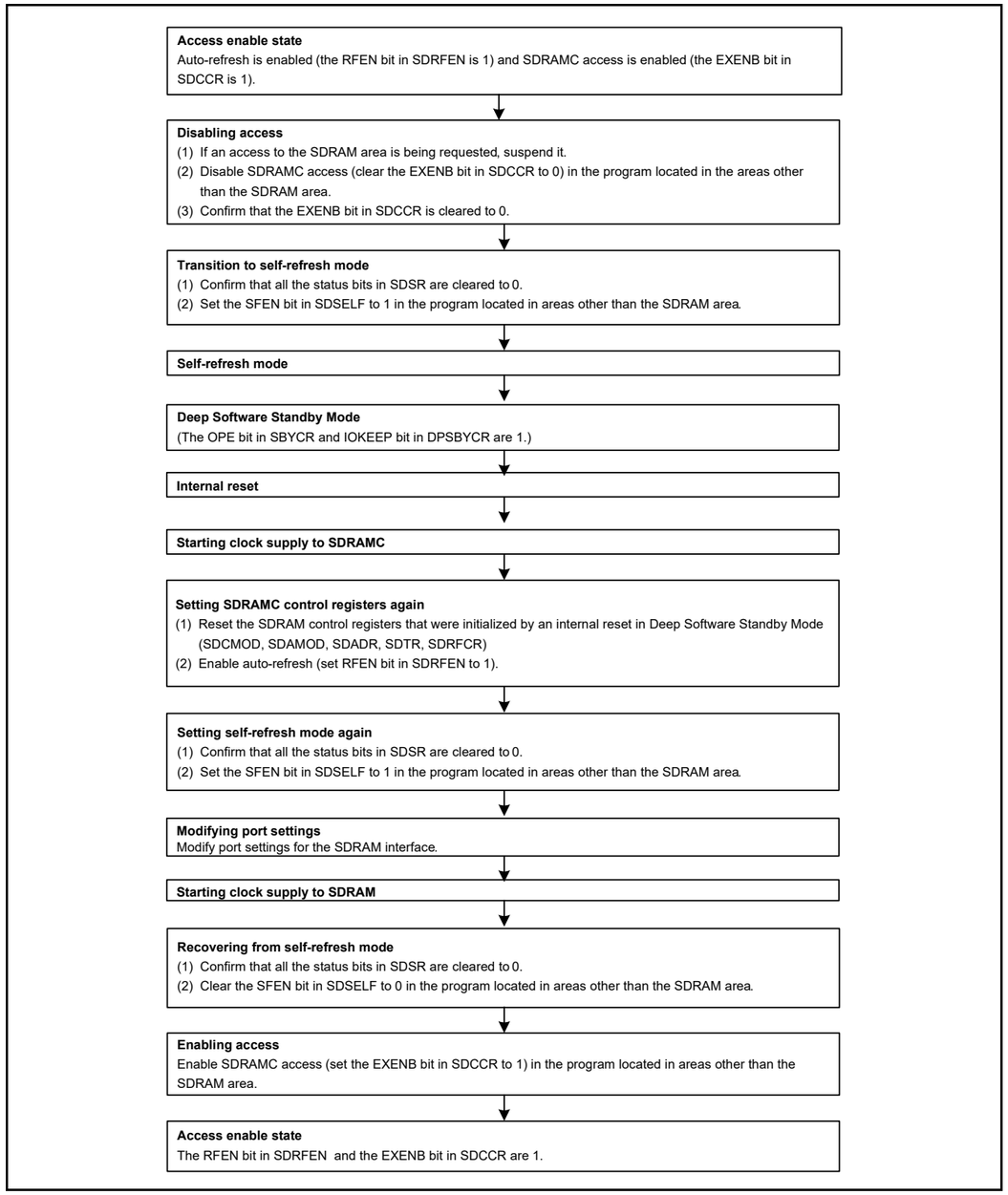


Figure 15.53 Procedure for transitioning to and recovering from self-refresh mode in Deep Software Standby mode

15.6.11.3 Timing register settings and access timing

This section describes the relationship between read and write timing and the settings in the SDRAM Timing Register (SDTR).

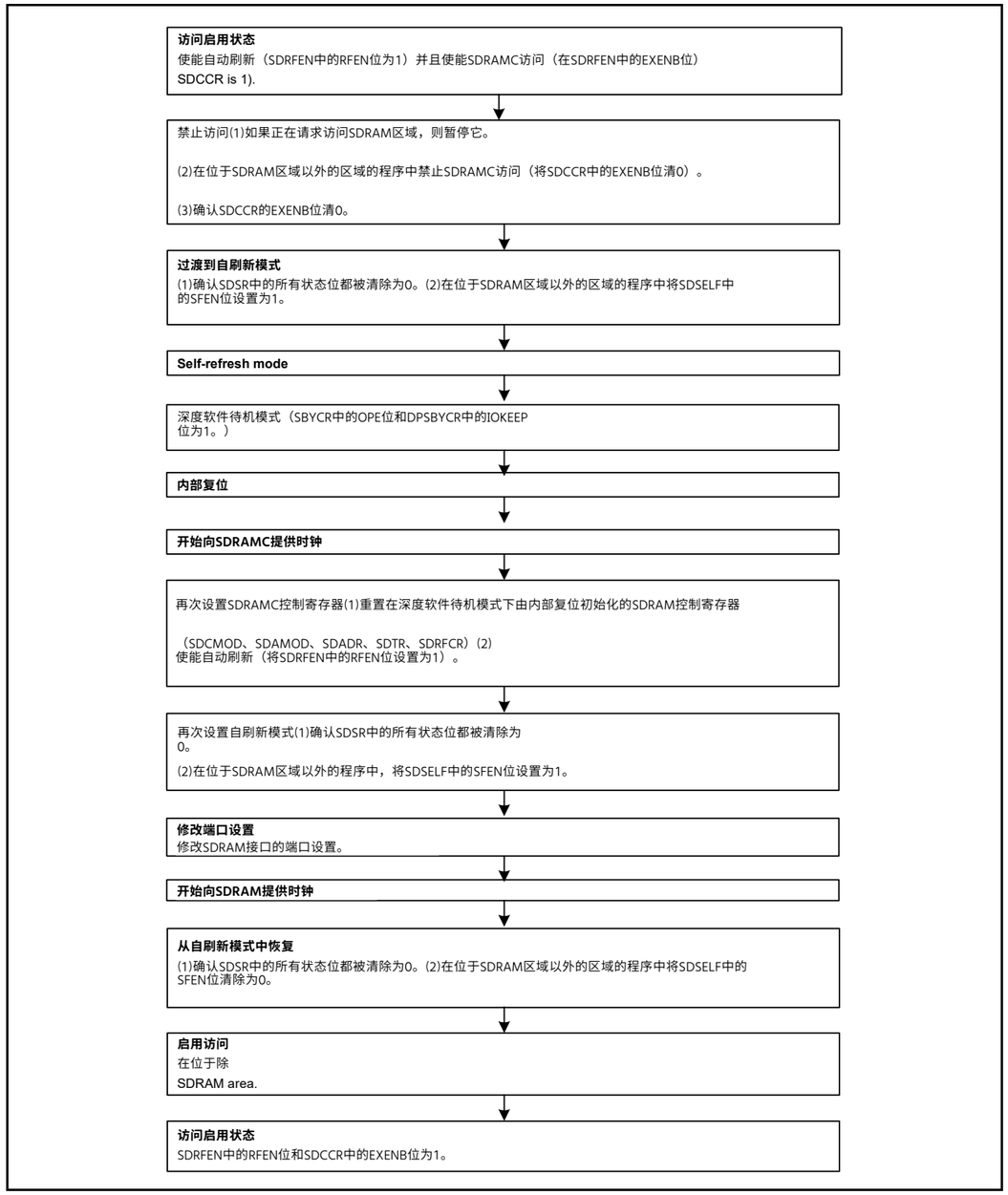


Figure 15.53 在深度软件待机模式下转换到自刷新模式并从中恢复的过程

15.6.11.3 时序寄存器设置和访问时序

本节介绍读写时序与SDRAM时序寄存器(SDTR)中的设置之间的关系。

(1) Single read timing examples

Figure 15.54 to Figure 15.58 show the relationship between single read timing and the SDTR register settings. Table 15.15 shows the association between the figures and the SDTR register settings.

During read access, the next bus access is enabled at the earliest 2 cycles after the read data becomes valid. However, if two or more accesses occur for one transfer request, the next bus access is enabled at the earliest 1 cycle after the read data becomes valid, as shown in Figure 15.58.

Table 15.15 Association between timing figures and STDR register settings for single read timing

Figure number	RAS[2:0] settings	Number of cycles	RCD[1:0] settings	Number of cycles	RP[2:0] settings	Number of cycles	CL[2:0] settings	Number of cycles
Figure 15.54	010	3	00	1	001	2	010	2
Figure 15.55	000	1	01	2	001	2	010	2
Figure 15.56	000	1	01	2	001	2	011	3
Figure 15.57, Figure 15.58	010	3	00	1	000	1	010	2

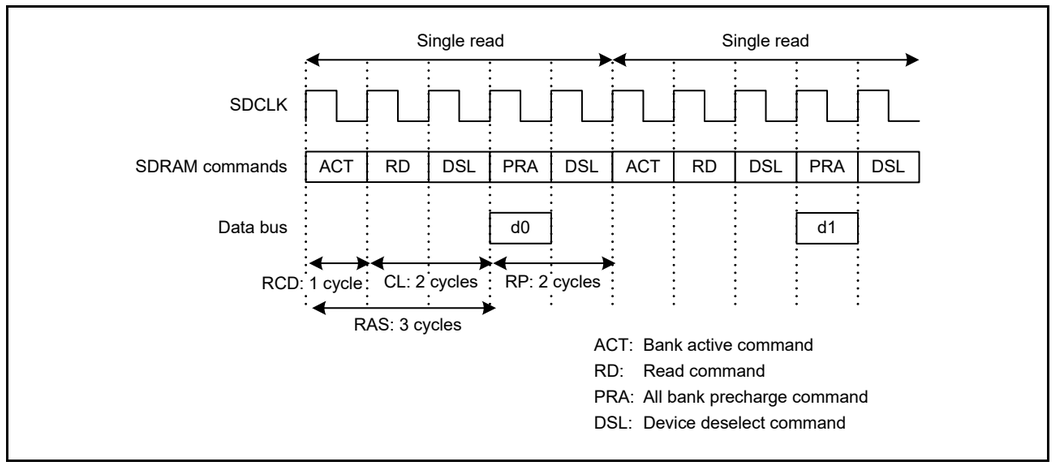


Figure 15.54 Example timing for single read (1)

(1) 单次读取时序示例

图15.54至图15.58显示了单次读取时序和SDTR寄存器设置之间的关系。表15.15显示了数字和SDTR寄存器设置之间的关联。

在读访问期间，在读数据变为有效后最早的2个周期启用下一次总线访问。但是，如果一个传输请求发生两次或更多次访问，则在读取数据有效后最早的1个周期启用下一次总线访问，如图15.58所示。

Table 15.15 单次读取时序的时序图和STDR寄存器设置之间的关联

图号	RAS[2:0] settings	循环次数	RCD[1:0] settings	循环次数	RP[2:0] settings	循环次数	CL[2:0] settings	循环次数
Figure 15.54	010	3	00	1	001	2	010	2
Figure 15.55	000	1	01	2	001	2	010	2
Figure 15.56	000	1	01	2	001	2	011	3
Figure 15.57, Figure 15.58	010	3	00	1	000	1	010	2

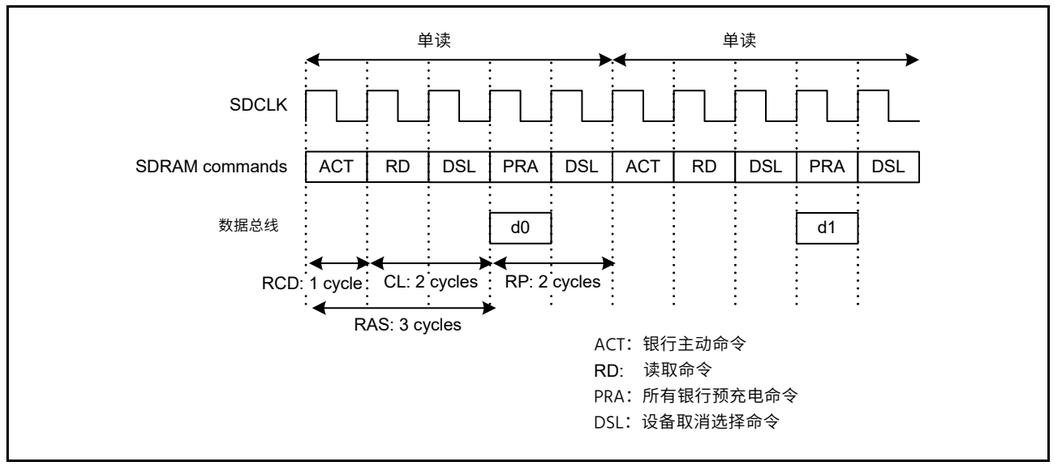


Figure 15.54 单次读取的示例时序(1)

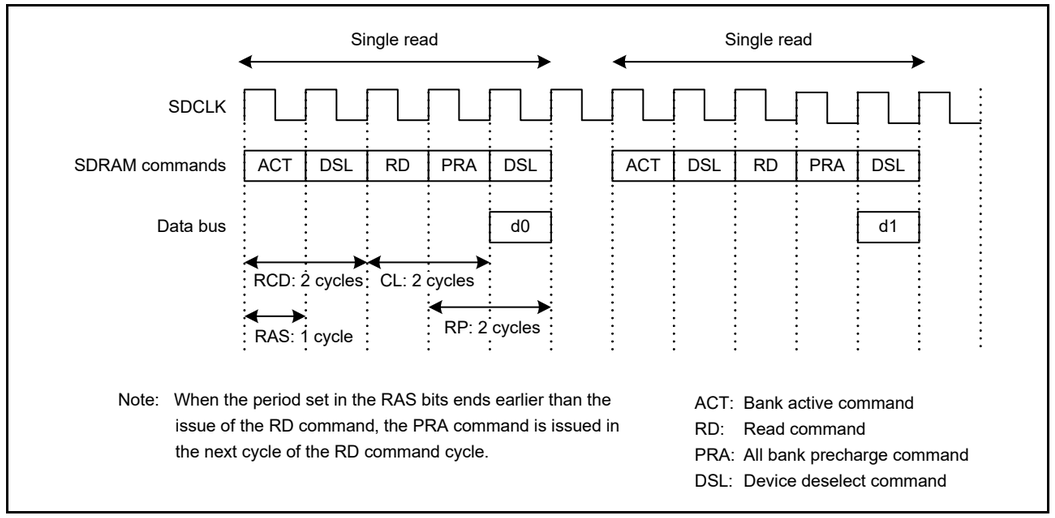


Figure 15.55 Example timing for single read (2)

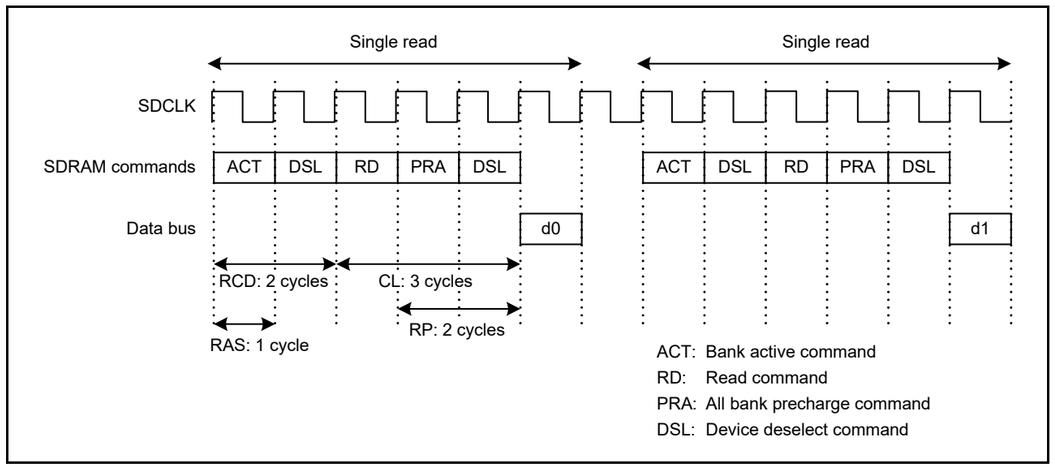


Figure 15.56 Example timing for single read (3)

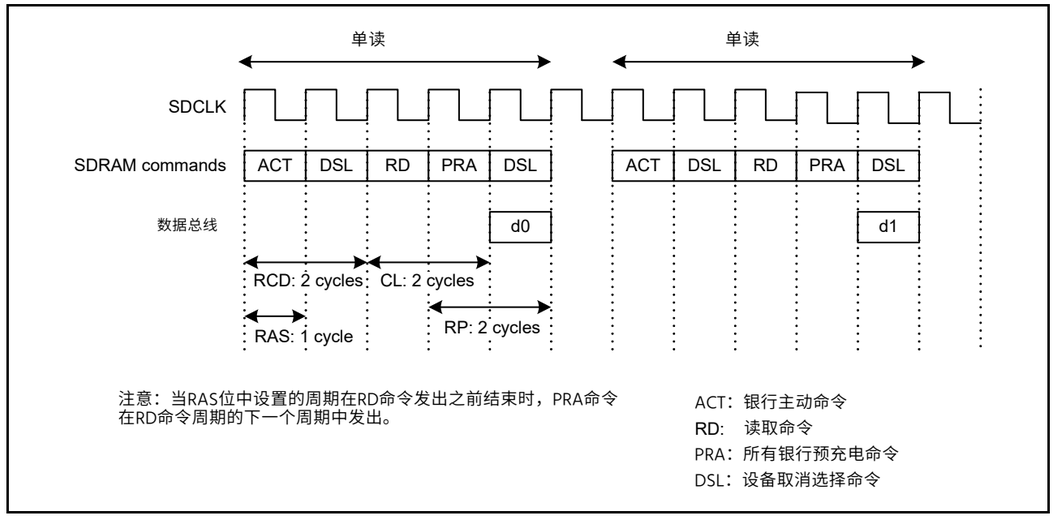


Figure 15.55 单次读取的示例时序(2)

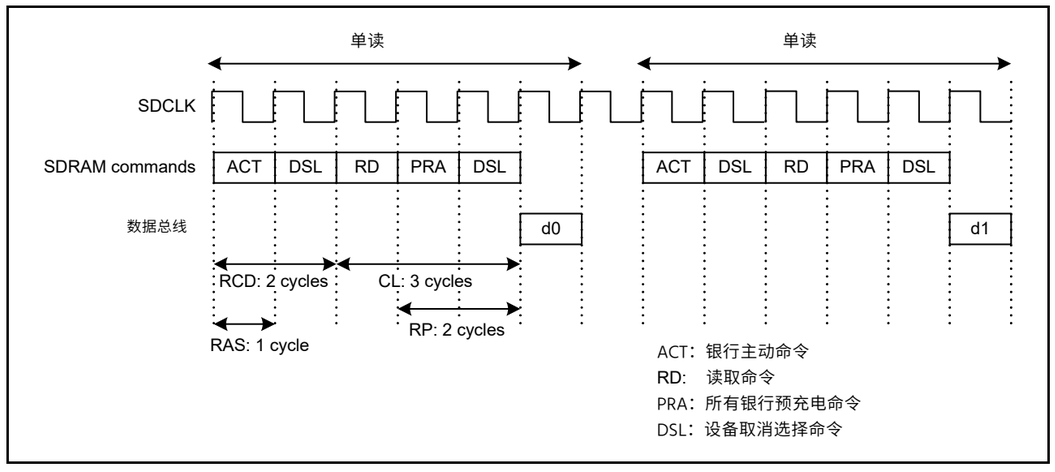


Figure 15.56 单次读取的示例时序(3)

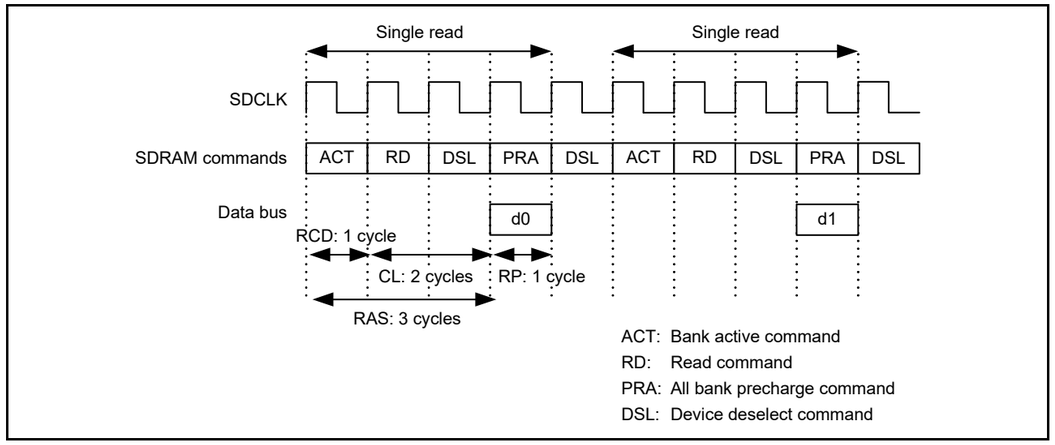


Figure 15.57 Example timing for single read (4)

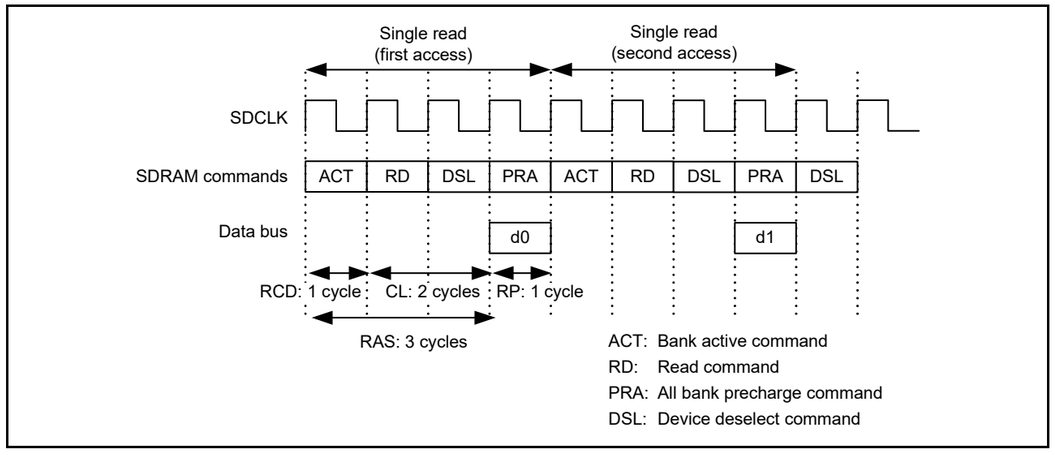


Figure 15.58 Example timing for single read (5), when two bus accesses occur for one transfer request

(2) Single write timing examples

Figure 15.59 to Figure 15.60 show the relationship between the single write timing and the SDTR register settings. Table 15.16 shows the association between the figures and the SDTR register settings. During write access, the next bus access is enabled at the earliest 2 cycles after an all bank precharge command (PRA) is issued. However, if two or more accesses occur for one transfer request, the next bus access is enabled at the earliest 1 cycle after the PRA is issued, as shown in Figure 15.63.

Table 15.16 Association between timing figures and STDR register settings for single write timing

Figure number	RAS[2:0] settings	Number of cycles	RCD[1:0] settings	Number of cycles	RP[2:0] settings	Number of cycles	WR settings	Number of cycles
Figure 15.59	010	3	00	1	001	2	0	1
Figure 15.60	000	1	01	2	001	2	0	1
Figure 15.61	000	1	01	2	001	2	1	2
Figure 15.62, Figure 15.63	010	3	00	0	000	2	0	1

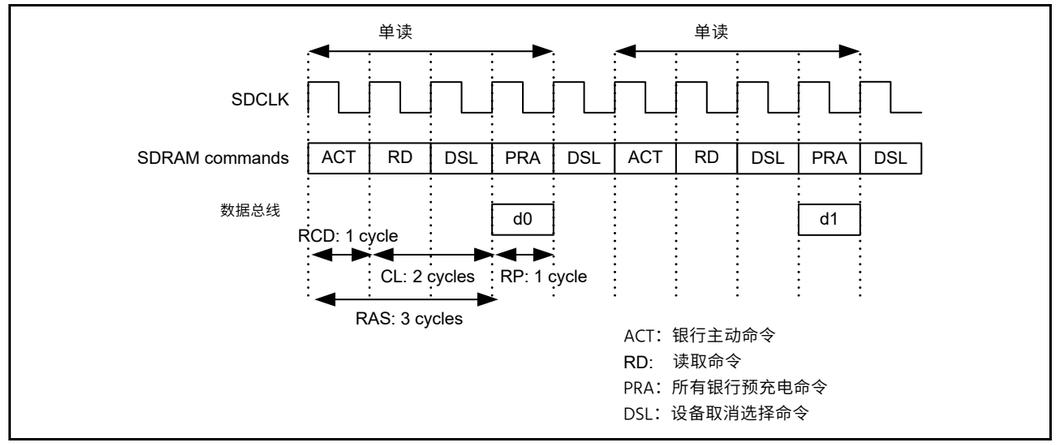


Figure 15.57 单次读取的示例时序(4)

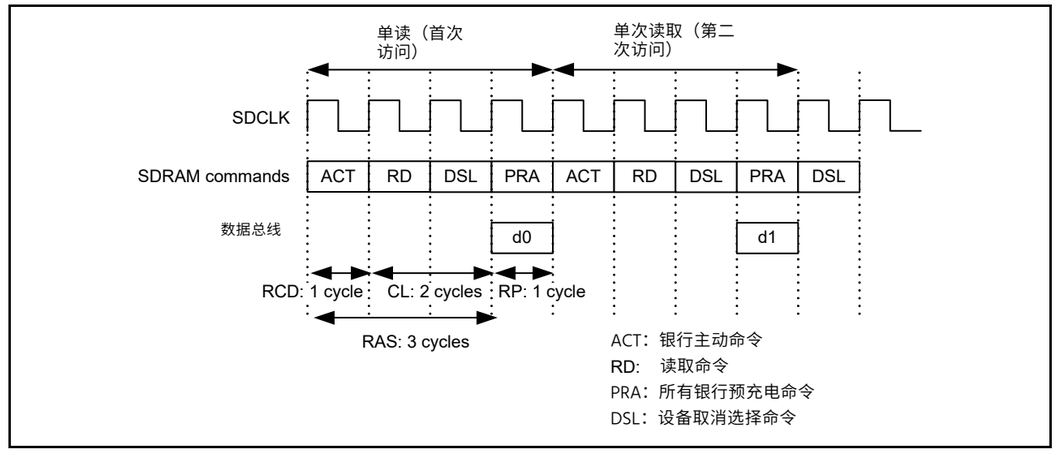


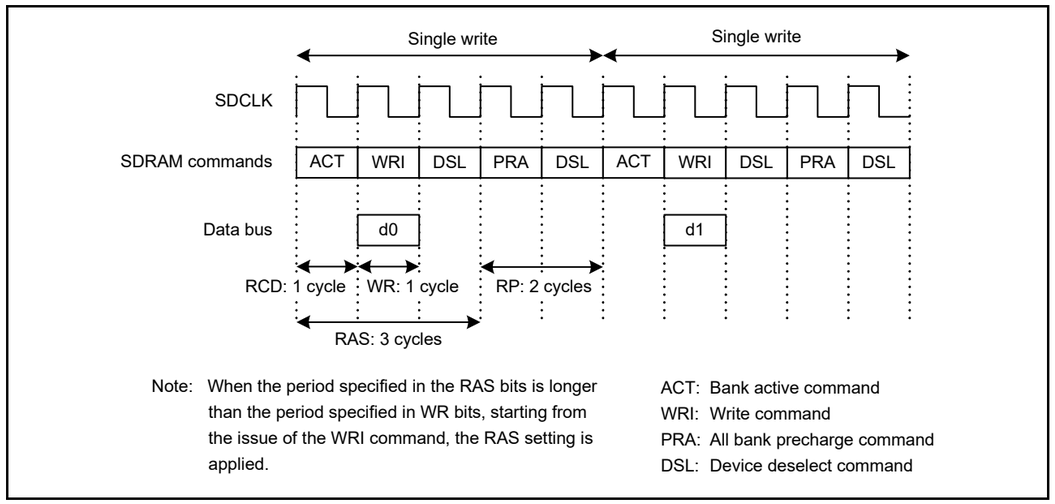
Figure 15.58 单次读取的示例时序(5)，当一个传输请求发生两次总线访问时

(2) 单次写入时序示例

图15.59至图15.60显示了单次写入时序和SDTR寄存器设置之间的关系。表15.16显示了数字和SDTR寄存器设置之间的关联。在写访问期间，下一个总线访问在发出所有存储体预充电命令(PRA)后最早的2个周期启用。但是，如果一个传输请求发生两次或多次访问，则在发出PRA后最早的1个周期启用下一次总线访问，如图15.63所示。

Table 15.16 单次写入时序的时序图和STDR寄存器设置之间的关联

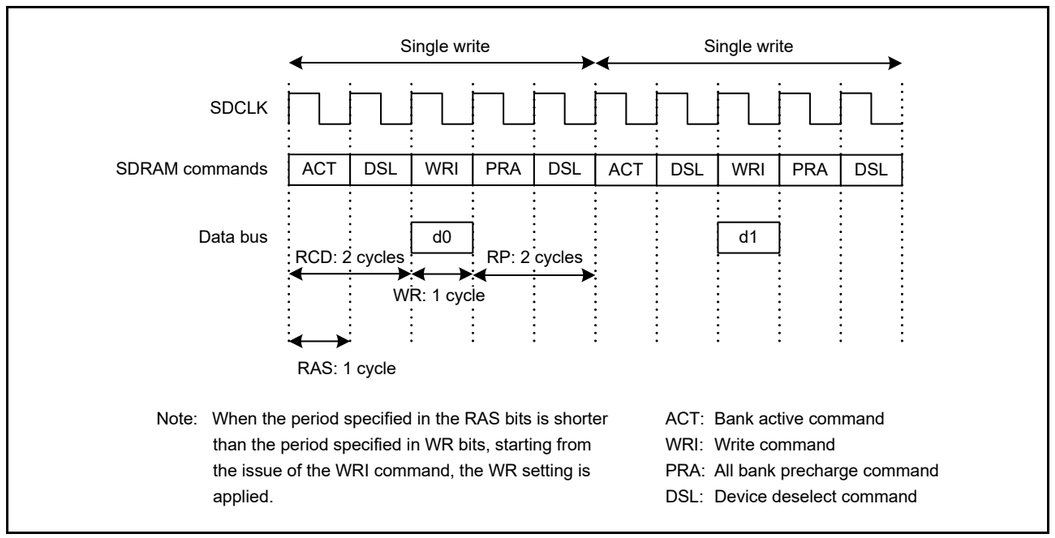
图号	RAS[2:0] settings	循环次数	RCD[1:0] settings	循环次数	RP[2:0] settings	循环次数	WR settings	循环次数
Figure 15.59	010	3	00	1	001	2	0	1
Figure 15.60	000	1	01	2	001	2	0	1
Figure 15.61	000	1	01	2	001	2	1	2
Figure 15.62, Figure 15.63	010	3	00	0	000	2	0	1



Note: When the period specified in the RAS bits is longer than the period specified in WR bits, starting from the issue of the WRI command, the RAS setting is applied.

ACT: Bank active command
WRI: Write command
PRA: All bank precharge command
DSL: Device deselect command

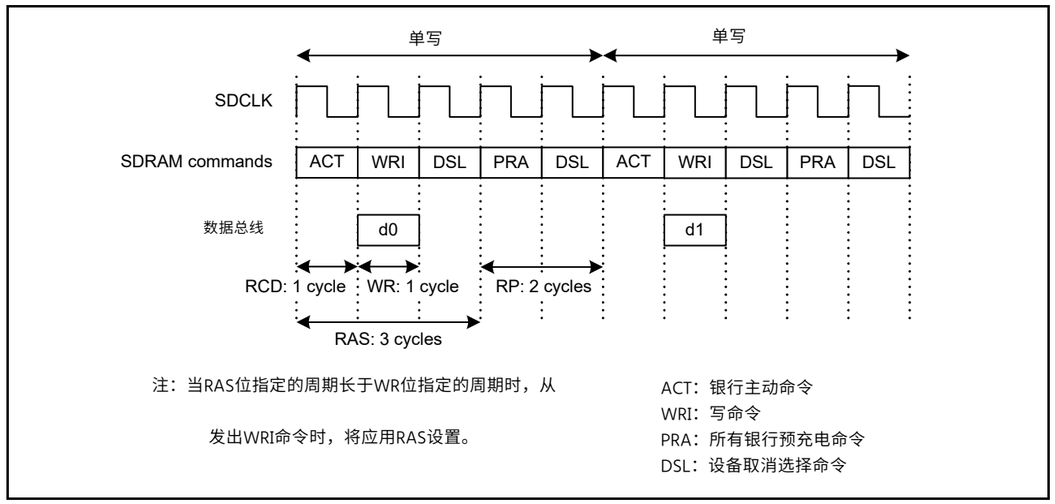
Figure 15.59 Example timing for single write (1)



Note: When the period specified in the RAS bits is shorter than the period specified in WR bits, starting from the issue of the WRI command, the WR setting is applied.

ACT: Bank active command
WRI: Write command
PRA: All bank precharge command
DSL: Device deselect command

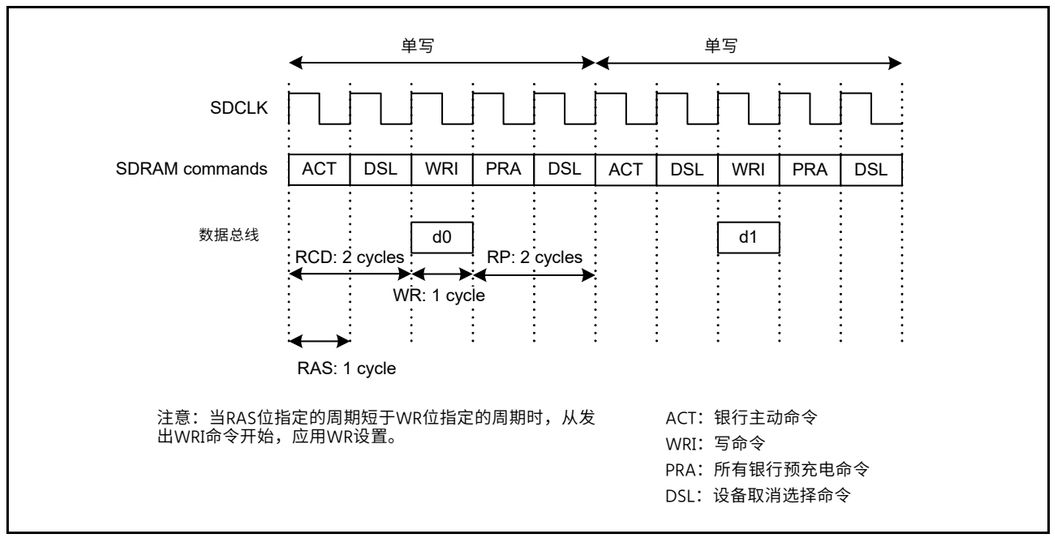
Figure 15.60 Example timing for single write (2)



注：当RAS位指定的周期长于WR位指定的周期时，从发出WRI命令时，将应用RAS设置。

ACT：银行主动命令
WRI：写命令
PRA：所有银行预充电命令
DSL：设备取消选择命令

Figure 15.59 单次写入的示例时序(1)



注意：当RAS位指定的周期短于WR位指定的周期时，从发出WRI命令开始，应用WR设置。

ACT：银行主动命令
WRI：写命令
PRA：所有银行预充电命令
DSL：设备取消选择命令

Figure 15.60 单次写入的示例时序(2)

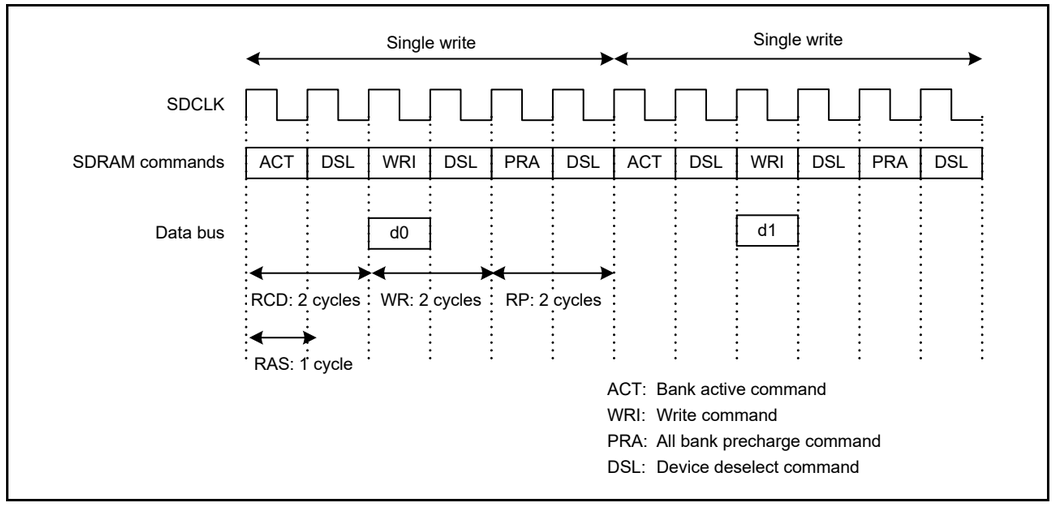


Figure 15.61 Example timing for single write (3)

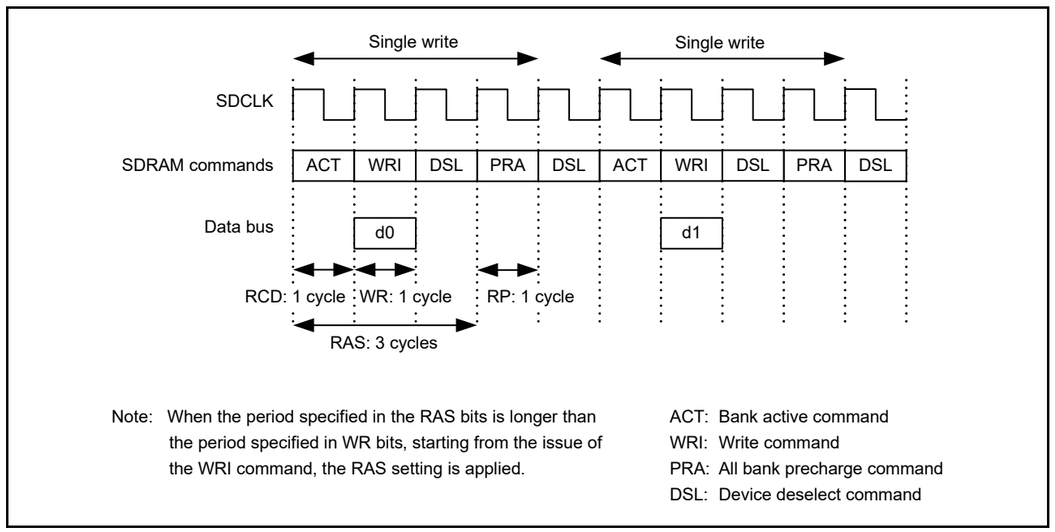


Figure 15.62 Example timing for single write (4)

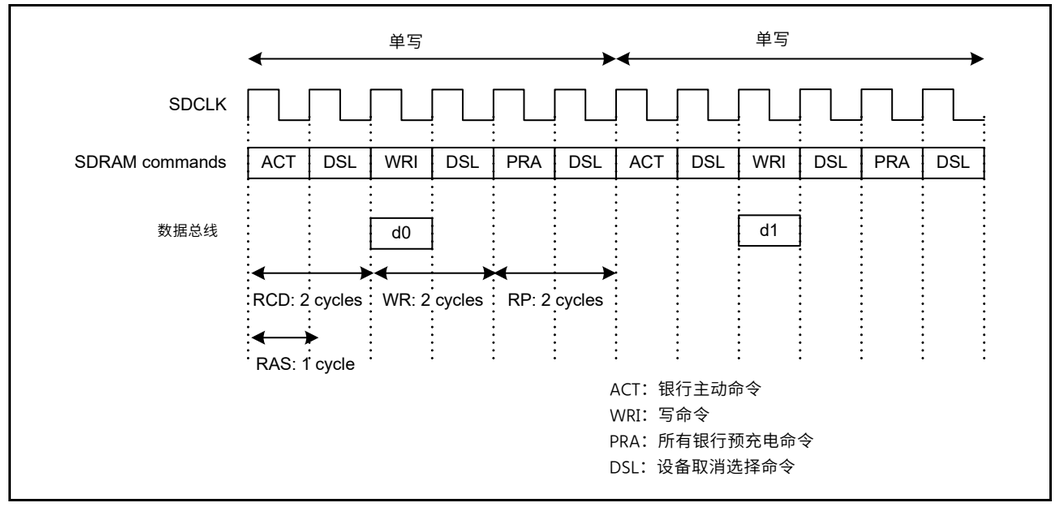


Figure 15.61 单次写入的示例时序(3)

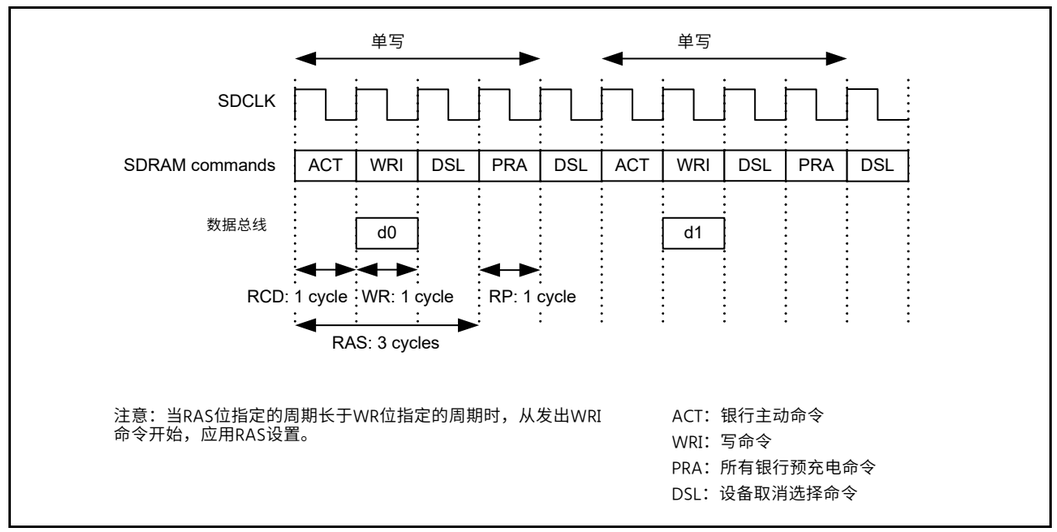


Figure 15.62 单次写入的示例时序(4)

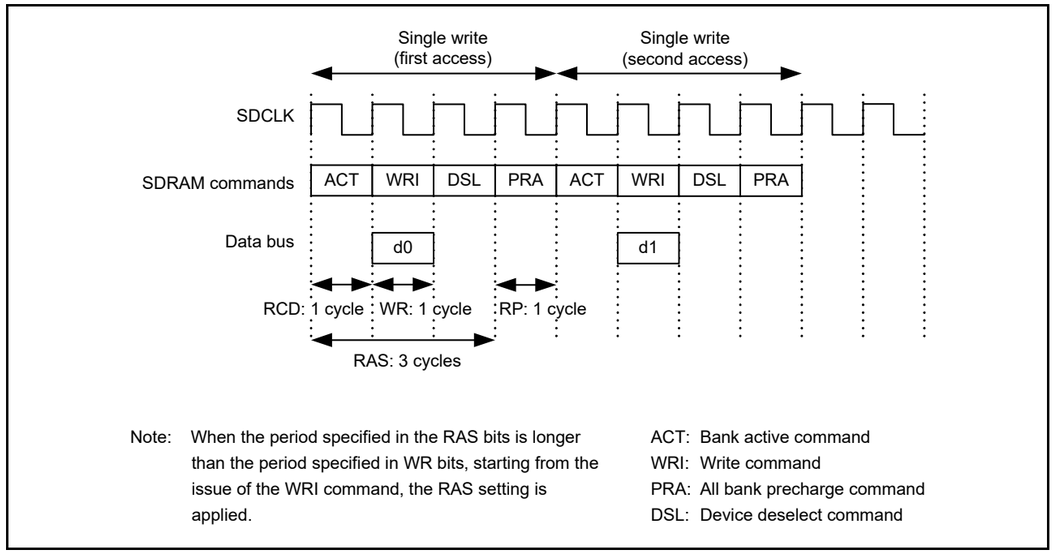


Figure 15.63 Example timing for single write (5), when two bus accesses occur for one transfer request

(3) Consecutive read timing examples

Figure 15.64 to Figure 15.66 show the relationship between the consecutive read timing for four data reads and the SDTR register settings. Table 15.17 shows the correspondence between the figures and the SDTR register settings.

Table 15.17 Correspondence between timing figures and STDR register settings for consecutive read timing

Figure number	RAS[2:0] settings	Number of cycles	RCD[1:0] settings	Number of cycles	RP[2:0] settings	Number of cycles	CL[2:0] settings	Number of cycles
Figure 15.64	010	3	00	1	001	2	010	2
Figure 15.65	000	1	01	2	001	2	010	2
Figure 15.66	000	1	01	2	001	2	011	3

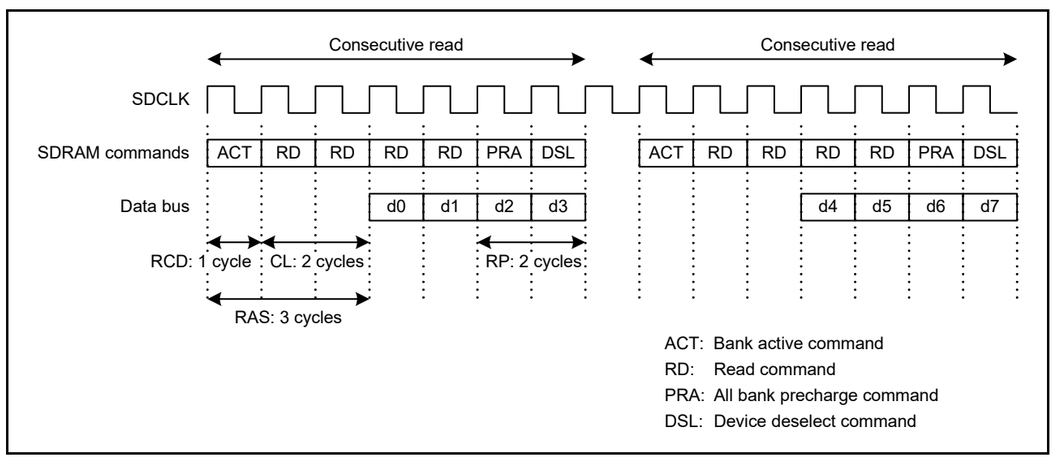


Figure 15.64 Example timing for consecutive read (1)

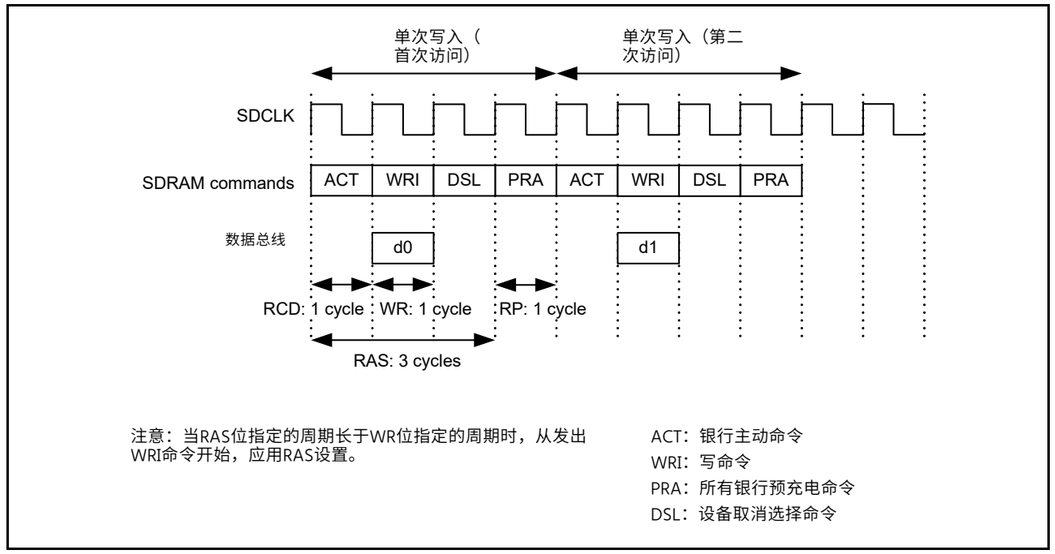


Figure 15.63 单次写入的示例时序(5)，当一个传输请求发生两次总线访问时

(3) 连续读取时序示例

图15.64至图15.66显示了四次数据读取的连续读取时序与SDTR寄存器设置之间的关系。表15.17显示了数字和SDTR寄存器设置之间的对应关系。

Table 15.17 连续读取时序的时序图和STDR寄存器设置之间的对应关系

图号	RAS[2:0] settings	循环次数	RCD[1:0] settings	循环次数	RP[2:0] settings	循环次数	CL[2:0] settings	循环次数
Figure 15.64	010	3	00	1	001	2	010	2
Figure 15.65	000	1	01	2	001	2	010	2
Figure 15.66	000	1	01	2	001	2	011	3

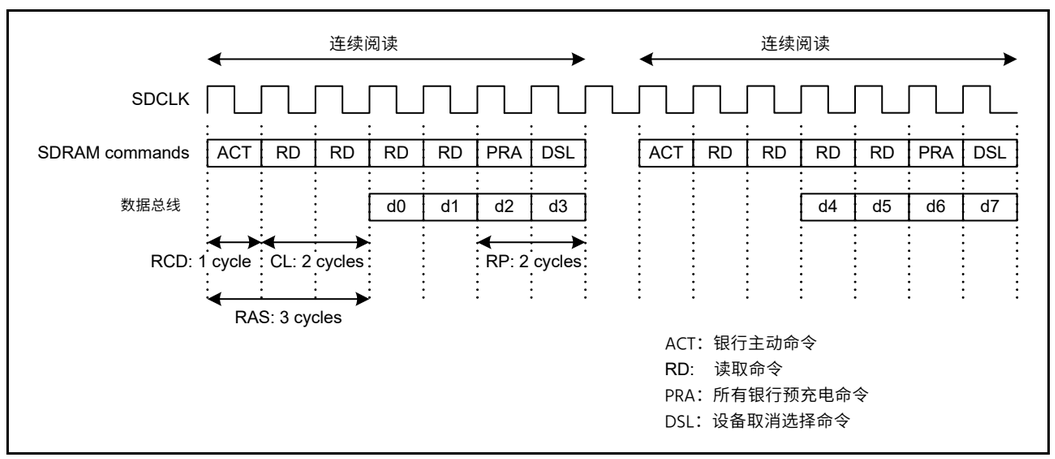


Figure 15.64 连续读取的示例时序(1)

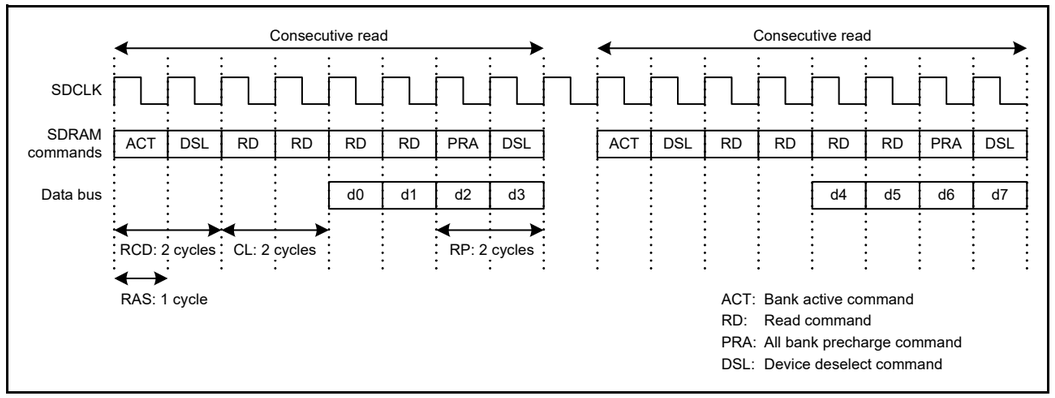


Figure 15.65 Example timing for consecutive read (2)

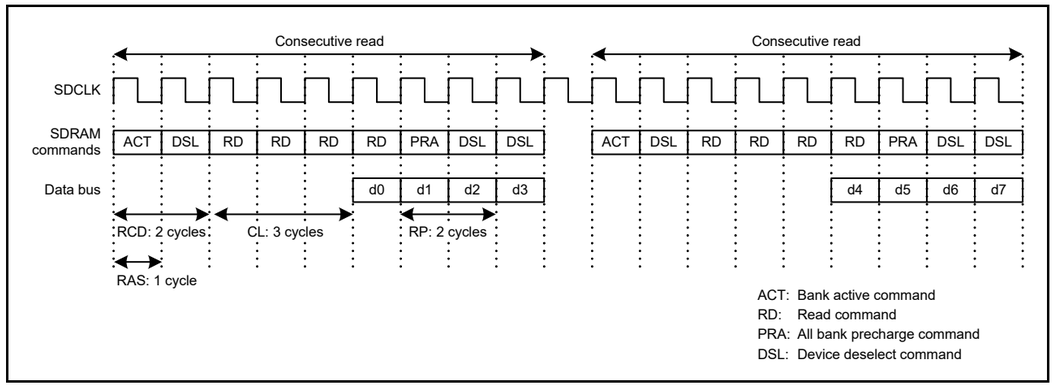


Figure 15.66 Example timing for consecutive read (3)

(4) Consecutive write timing examples

Figure 15.67 to Figure 15.69 show the relationship between the consecutive write timing for four data reads and the SDTR register settings. Table 15.18 shows the association between the figures and the SDTR register settings.

Table 15.18 Association between timing figures and STDR register settings for consecutive write timing

Figure number	RAS[2:0] settings	Number of cycles	RCD[1:0] settings	Number of cycles	RP[2:0] settings	Number of cycles	WR settings	Number of cycles
Figure 15.67	010	3	00	1	001	2	0	1
Figure 15.68	000	1	01	2	001	2	0	1
Figure 15.69	000	1	01	2	001	2	1	2

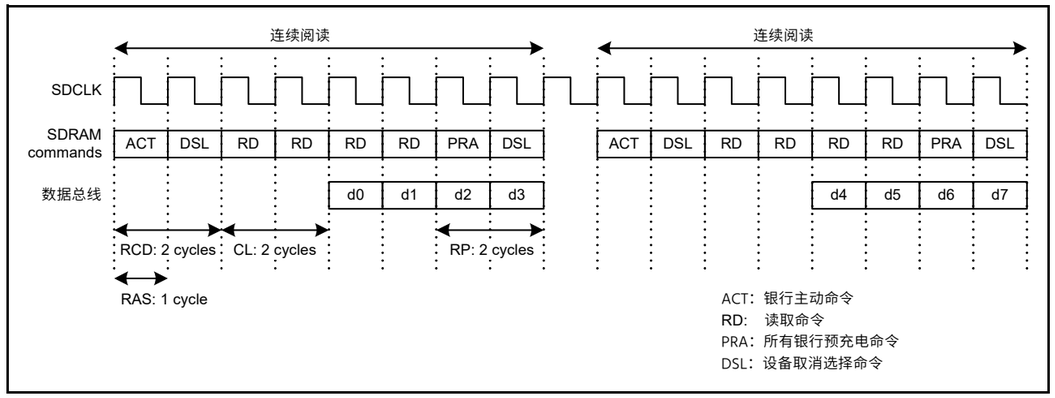


Figure 15.65 连续读取的示例时序(2)

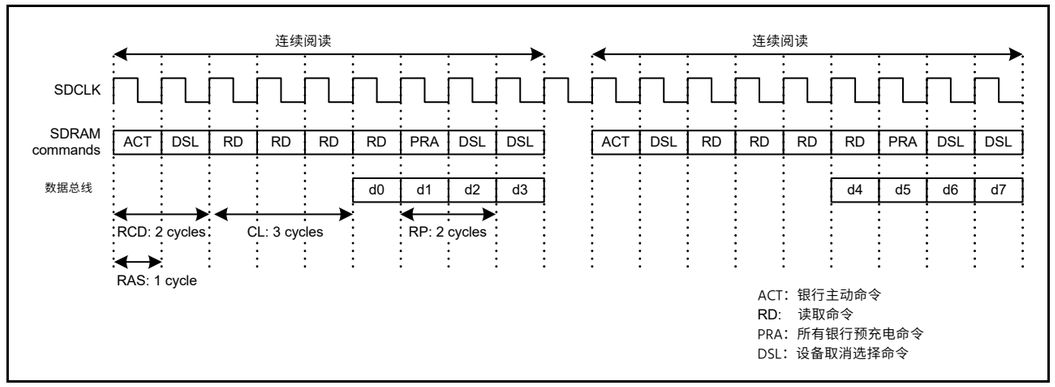


Figure 15.66 连续读取的示例时序(3)

(4) 连续写入时序示例

图15.67至图15.69显示了4次数据读取的连续写入时序与SDTR寄存器设置。表15.18显示了数字和SDTR寄存器设置之间的关联。

Table 15.18 时序图和STDR寄存器设置之间的关联，用于连续写入时序

图号	RAS[2:0] settings	循环次数	RCD[1:0] settings	循环次数	RP[2:0] settings	循环次数	WR settings	循环次数
Figure 15.67	010	3	00	1	001	2	0	1
Figure 15.68	000	1	01	2	001	2	0	1
Figure 15.69	000	1	01	2	001	2	1	2

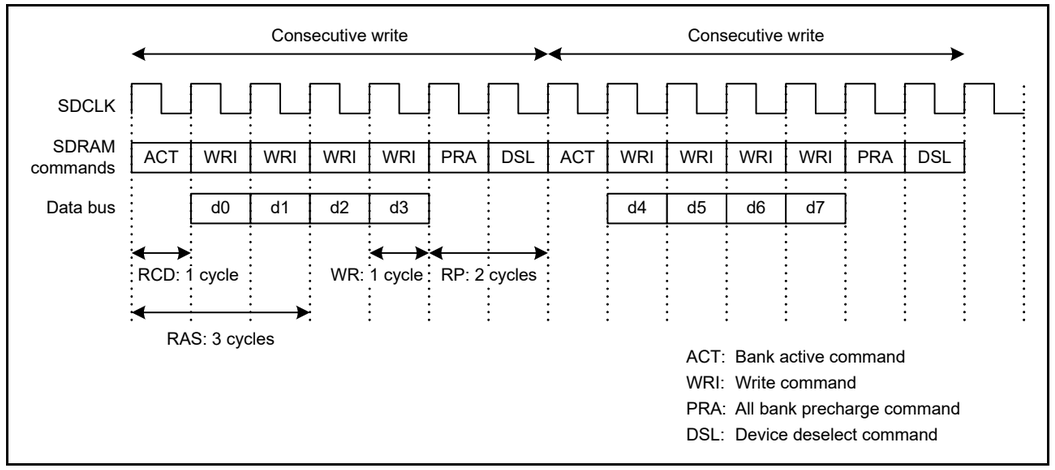


Figure 15.67 Example timing for consecutive write (1)

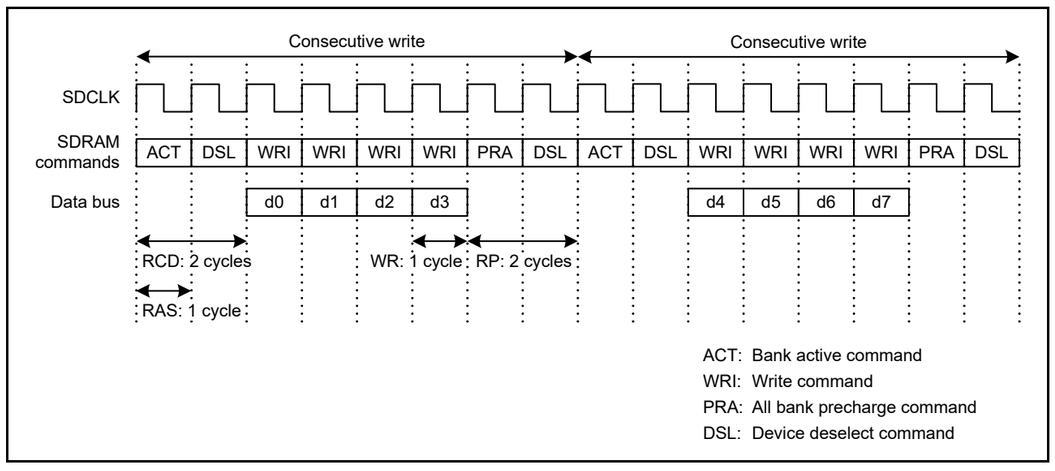


Figure 15.68 Example timing for consecutive write (2)

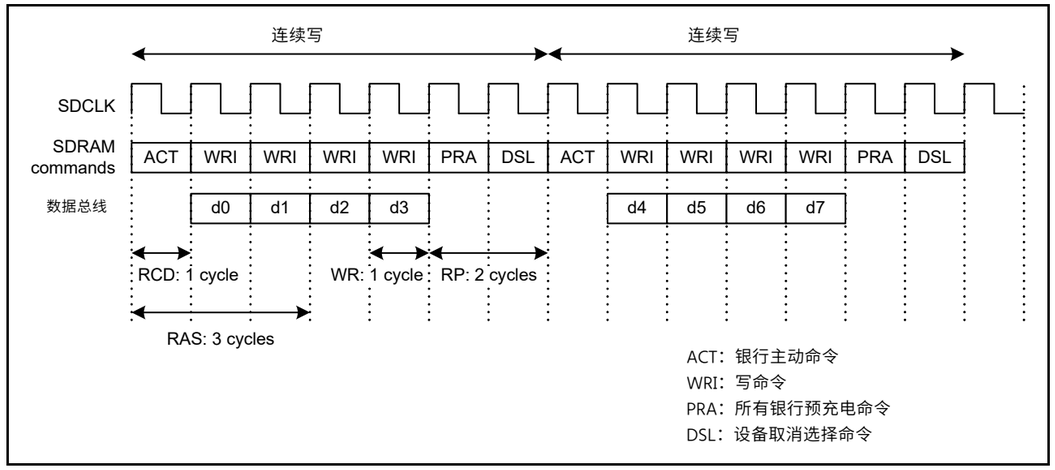


Figure 15.67 连续写入的示例时序(1)

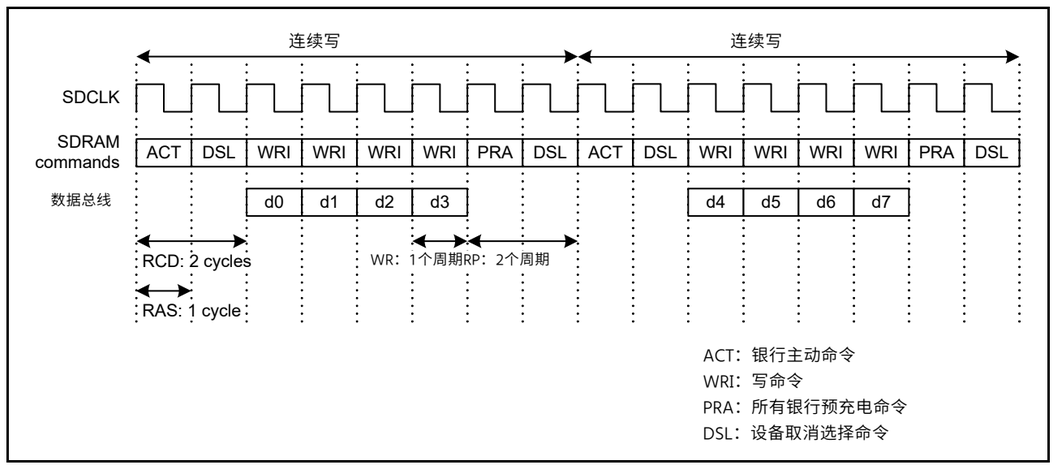


Figure 15.68 连续写入的示例时序(2)

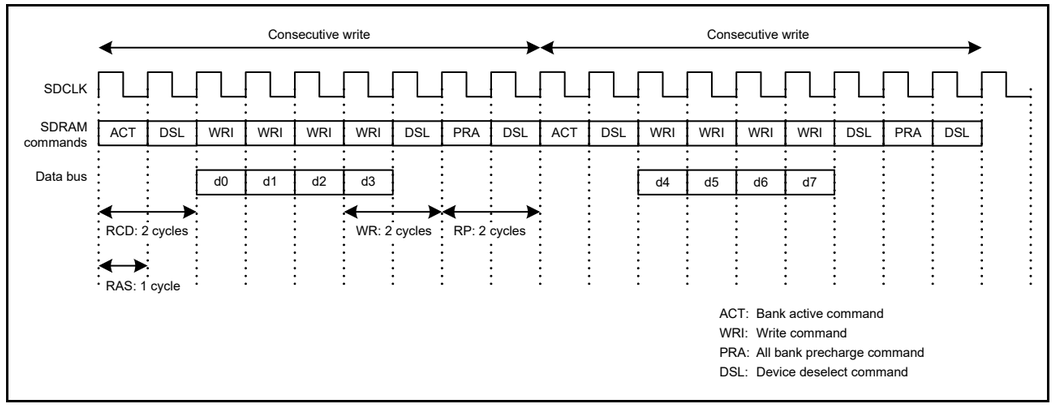


Figure 15.69 Example timing for consecutive write (3)

15.6.12 Address Multiplexing

In the SDRAM space, row and column addresses are multiplexed. The size of the shift in a row address must be specified in the Address Multiplex Select bits (SDADR.MXC[1:0]) in the SDRAM Address Register (SDADR). Additionally, in the SDRAM space, the address precharge-select command (Precharge-sel) is output to the upper bits of column addresses. Table 15.19 shows the relationship between the SDADR.MXC[1:0] settings and the shift amount.

Table 15.19 Address multiplexing

MXC [1:0]	Shift amount	Data bus width	Address	Address pins external to the MCU															
				A15	A14	A13	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01	A00
00	8 bits	8 bits	Row	A23	A22	A21	A20	A19	A18*	A17	A16	A15	A14	A13	A12	A11	A10	A09	A08
			Column	A23	A22	A21	A20	A19	P	A09	A08	A07	A06	A05	A04	A03	A02	A01	A00
		16 bits	Row	A23	A22	A21	A20	A19*	A18	A17	A16	A15	A14	A13	A12	A11	A10	A09	A08
			Column	A23	A22	A21	A20	P	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01	A00
01	9 bits	8 bits	Row	A24	A23	A22	A21	A20	A20*	A18	A17	A16	A15	A14	A13	A12	A11	A10	A09
			Column	A24	A23	A22	A21	A20	P	A09	A08	A07	A06	A05	A04	A03	A02	A01	A00
		16 bits	Row	A24	A23	A22	A21	A20*	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A09
			Column	A24	A23	A22	A21	P	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01	A00
10	10 bits	8 bits	Row	A25	A24	A23	A22	A21	A20*	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10
			Column	A25	A24	A23	A22	A21	P	A09	A08	A07	A06	A05	A04	A03	A02	A01	A00
		16 bits	Row	A25	A24	A23	A22	A21*	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10
			Column	A25	A24	A23	A22	P	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01	A00
11	11 bits	8 bits	Row	A26	A25	A24	A23	A22	A21*	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11
			Column	A26	A25	A24	A23	A10	P	A09	A08	A07	A06	A05	A04	A03	A02	A01	A00
		16 bits	Row	A26	A25	A24	A23	A22*	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11
			Column	A26	A25	A24	A11	P	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01	A00

Note: P: Precharge-select command (Precharge-sel) is output.
*: When the PALL command is issued, Precharge-sel = 1 (high) is output. When the Active command is issued, the associated address is output.

15.6.13 Example SDRAM Connections

15.6.13.1 16-Bit bus space

Figure 15.70 shows an example connection to two 512-Mb SDRAMs with a 13-bit row address, 11-bit column address, and 8-bit bus.

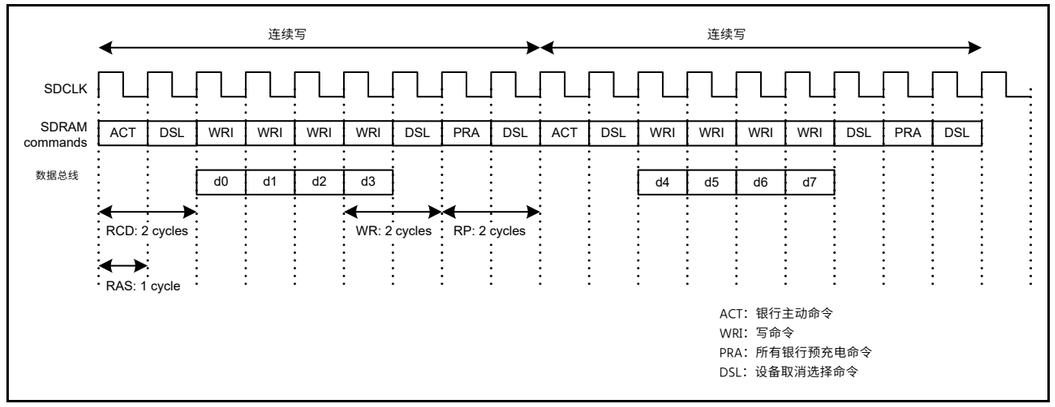


Figure 15.69 连续写入的示例时序(3)

15.6.12 Address Multiplexing

在SDRAM空间中，行和列地址是多路复用的。行地址的移位大小必须在SDRAM地址寄存器(SDADR)的地址复用选择位(SDADR.MXC[1:0])中指定。此外，在SDRAM空间中，地址预充电选择命令（Precharge-sel）被输出到列地址的高位。表15.19显示了SDADR.MXC[1:0]设置和移位量之间的关系。

Table 15.19 Address multiplexing

MXC [1:0]	班次金额	数据总线宽度	Address	MCU外部的地址引脚															
				A15	A14	A13	A12	A11	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01	A00
00	8 bits	8 bits	Row	A23	A22	A21	A20	A19	A18*	A17	A16	A15	A14	A13	A12	A11	A10	A09	A08
			Column	A23	A22	A21	A20	A19	P	A09	A08	A07	A06	A05	A04	A03	A02	A01	A00
		16 bits	Row	A23	A22	A21	A20	A19*	A18	A17	A16	A15	A14	A13	A12	A11	A10	A09	A08
			Column	A23	A22	A21	A20	P	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01	A00
01	9 bits	8 bits	Row	A24	A23	A22	A21	A20	A20*	A18	A17	A16	A15	A14	A13	A12	A11	A10	A09
			Column	A24	A23	A22	A21	A20	P	A09	A08	A07	A06	A05	A04	A03	A02	A01	A00
		16 bits	Row	A24	A23	A22	A21	A20*	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10	A09
			Column	A24	A23	A22	A21	P	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01	A00
10	10 bits	8 bits	Row	A25	A24	A23	A22	A21	A20*	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10
			Column	A25	A24	A23	A22	A21	P	A09	A08	A07	A06	A05	A04	A03	A02	A01	A00
		16 bits	Row	A25	A24	A23	A22	A21*	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11	A10
			Column	A25	A24	A23	A22	P	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01	A00
11	11 bits	8 bits	Row	A26	A25	A24	A23	A22	A21*	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11
			Column	A26	A25	A24	A23	A10	P	A09	A08	A07	A06	A05	A04	A03	A02	A01	A00
		16 bits	Row	A26	A25	A24	A23	A22*	A21	A20	A19	A18	A17	A16	A15	A14	A13	A12	A11
			Column	A26	A25	A24	A11	P	A10	A09	A08	A07	A06	A05	A04	A03	A02	A01	A00

Note: P：输出预充电选择指令（Precharge-sel）。*：发出PALL命令时，输出Precharge-sel=1（高）。发出Active命令时，会输出相关地址。

15.6.13 示例SDRAM连接

15.6.13.1 16位总线空间

图15.70显示了与两个512-MbSDRAM的示例连接，具有13位行地址、11位列地址和8位总线。

This MCU (shift amount: 11 bits)				SDRAM (512 Mb, with 8-bit bus)			
No.	Pin name	Row	Column	Pin name	BA/AP	Row	Column
1	RAS			RAS#			
2	CAS			CAS#			
3	WE			WE#			
4	CKE			CKE			
5	SDCS			CS#			
6	SDCLK			CLK			
7	DQM0			LDQM			
8	A15	A26	A26	BA1(A14)	BA1	–	–
9	A14	A25	A25	BA0(A13)	BA0	–	–
10	A13	A24	A24	A12		A12	–
11	A12	A23	A11	A11		A11	A11
12	A11	A22	P	A10	AP	A10	–
13	A10	A21	A10	A9		A9	A9
14	A09	A20	A9	A8		A8	A8
15	A08	A19	A8	A7		A7	A7
16	A07	A18	A7	A6		A6	A6
17	A06	A17	A6	A5		A5	A5
18	A05	A16	A5	A4		A4	A4
19	A04	A15	A4	A3		A3	A3
20	A03	A14	A3	A2		A2	A2
21	A02	A13	A2	A1		A1	A1
22	A01	A12	A1	A0		A0	A0
23	DQ07 to DQ00			DQ[7:0]			
No.				SDRAM (512 Mb, with 8-bit bus)			
(1)	RAS			RAS#			
(2)	CAS			CAS#			
(3)	WE			WE#			
(4)	CKE			CKE			
(5)	SDCS			CS#			
(6)	SDCLK			CLK			
24	DQM1			LDQM			
(8)	A15	A26	A26	BA1(A14)	BA1	–	–
(9)	A14	A25	A25	BA0(A13)	BA0	–	–
(10)	A13	A24	A24	A12		A12	–
(11)	A12	A23	A11	A11		A11	A11
(12)	A11	A22	P	A10	AP	A10	–
(13)	A10	A21	A10	A9		A9	A9
(14)	A09	A20	A9	A8		A8	A8
(15)	A08	A19	A8	A7		A7	A7
(16)	A07	A18	A7	A6		A6	A6
(17)	A06	A17	A6	A5		A5	A5
(18)	A05	A16	A5	A4		A4	A4
(19)	A04	A15	A4	A3		A3	A3
(20)	A03	A14	A3	A2		A2	A2
(21)	A02	A13	A2	A1		A1	A1
(22)	A01	A12	A1	A0		A0	A0
25	DQ15 to DQ08			DQ[7:0]			

Figure 15.70 SDRAM connection example with 512-Mb × 2 and 8-bit bus

Figure 15.71 shows an example connection to a 512-Mb SDRAMs with a 13-bit row address, 10-bit column address, and 16-bit bus.

This MCU (shift amount: 11 bits)				SDRAM (512 Mb, with 8-bit bus)			
No.	引脚名称	Row	Column	引脚名称	BA/AP	Row	Column
1	RAS			RAS#			
2	CAS			CAS#			
3	WE			WE#			
4	CKE			CKE			
5	SDCS			CS#			
6	SDCLK			CLK			
7	DQM0			LDQM			
8	A15	A26	A26	BA1(A14)	BA1	–	–
9	A14	A25	A25	BA0(A13)	BA0	–	–
10	A13	A24	A24	A12		A12	–
11	A12	A23	A11	A11		A11	A11
12	A11	A22	P	A10	AP	A10	–
13	A10	A21	A10	A9		A9	A9
14	A09	A20	A9	A8		A8	A8
15	A08	A19	A8	A7		A7	A7
16	A07	A18	A7	A6		A6	A6
17	A06	A17	A6	A5		A5	A5
18	A05	A16	A5	A4		A4	A4
19	A04	A15	A4	A3		A3	A3
20	A03	A14	A3	A2		A2	A2
21	A02	A13	A2	A1		A1	A1
22	A01	A12	A1	A0		A0	A0
23	DQ07 to DQ00			DQ[7:0]			
No.				SDRAM (512 Mb, with 8-bit bus)			
(1)	RAS			RAS#			
(2)	CAS			CAS#			
(3)	WE			WE#			
(4)	CKE			CKE			
(5)	SDCS			CS#			
(6)	SDCLK			CLK			
24	DQM1			LDQM			
(8)	A15	A26	A26	BA1(A14)	BA1	–	–
(9)	A14	A25	A25	BA0(A13)	BA0	–	–
(10)	A13	A24	A24	A12		A12	–
(11)	A12	A23	A11	A11		A11	A11
(12)	A11	A22	P	A10	AP	A10	–
(13)	A10	A21	A10	A9		A9	A9
(14)	A09	A20	A9	A8		A8	A8
(15)	A08	A19	A8	A7		A7	A7
(16)	A07	A18	A7	A6		A6	A6
(17)	A06	A17	A6	A5		A5	A5
(18)	A05	A16	A5	A4		A4	A4
(19)	A04	A15	A4	A3		A3	A3
(20)	A03	A14	A3	A2		A2	A2
(21)	A02	A13	A2	A1		A1	A1
(22)	A01	A12	A1	A0		A0	A0
25	DQ15 to DQ08			DQ[7:0]			

Figure 15.70 使用512−Mb×2和8位总线的SDRAM连接示例

图15.71显示了与具有13位行地址、10位列地址和16位总线的512−MbSDRAM的示例连接。

This MCU (shift amount: 10 bits)				SDRAM (512 Mb, with 16-bit bus)			
No.	Pin name	Row	Column	Pin name	BA/AP	Row	Column
1	RAS			RAS#			
2	CAS			CAS#			
3	WE			WE#			
4	CKE			CKE			
5	SDCS			CS#			
6	SDCLK			CLK			
7	DQM1			UDQM			
8	DQM0			LDQM			
9	A15	A25	A25	BA1(A14)	BA1	–	–
10	A14	A24	A24	BA0(A13)	BA0	–	–
11	A13	A23	A23	A12		A12	–
12	A12	A22	A22	A11		A11	–
13	A11	A21	P	A10	AP	A10	–
14	A10	A20	A10	A9		A9	A9
15	A09	A19	A9	A8		A8	A8
16	A08	A18	A8	A7		A7	A7
17	A07	A17	A7	A6		A6	A6
18	A06	A16	A6	A5		A5	A5
19	A05	A15	A5	A4		A4	A4
20	A04	A14	A4	A3		A3	A3
21	A03	A13	A3	A2		A2	A2
22	A02	A12	A2	A1		A1	A1
23	A01	A11	A1	A0		A0	A0
24	DQ15 to DQ08			DQ[15:8]			
25	DQ07 to DQ00			DQ[7:0]			

Figure 15.71 SDRAM connection example with 512-Mb × 1 and 16-bit bus

Figure 15.72 shows an example connection to a 256-Mb SDRAMs with a 13-bit row address, 9-bit column address, and 16-bit bus.

This MCU (shift amount: 10 bits)				SDRAM (512 Mb, with 16-bit bus)			
No.	引脚名称	Row	Column	引脚名称	BA/AP	Row	Column
1	RAS			RAS#			
2	CAS			CAS#			
3	WE			WE#			
4	CKE			CKE			
5	SDCS			CS#			
6	SDCLK			CLK			
7	DQM1			UDQM			
8	DQM0			LDQM			
9	A15	A25	A25	BA1(A14)	BA1	–	–
10	A14	A24	A24	BA0(A13)	BA0	–	–
11	A13	A23	A23	A12		A12	–
12	A12	A22	A22	A11		A11	–
13	A11	A21	P	A10	AP	A10	–
14	A10	A20	A10	A9		A9	A9
15	A09	A19	A9	A8		A8	A8
16	A08	A18	A8	A7		A7	A7
17	A07	A17	A7	A6		A6	A6
18	A06	A16	A6	A5		A5	A5
19	A05	A15	A5	A4		A4	A4
20	A04	A14	A4	A3		A3	A3
21	A03	A13	A3	A2		A2	A2
22	A02	A12	A2	A1		A1	A1
23	A01	A11	A1	A0		A0	A0
24	DQ15 to DQ08			DQ[15:8]			
25	DQ07 to DQ00			DQ[7:0]			

Figure 15.71 使用512−Mb×1和16位总线的SDRAM连接示例

图15.72显示了与具有13位行地址、9位列地址和16位总线的256−MbSDRAM的示例连接。

This MCU (shift amount: 9 bits)				SDRAM (256 Mb, with 16-bit bus)			
No.	Pin name	Row	Column	Pin name	BA/AP	Row	Column
1	RAS			RAS#			
2	CAS			CAS#			
3	WE			WE#			
4	CKE			CKE			
5	SDCS			CS#			
6	SDCLK			CLK			
7	DQM1			UDQM			
8	DQM0			LDQM			
9	A15	A24	A24	BA1(A14)	BA1	–	–
10	A14	A23	A23	BA0(A13)	BA0	–	–
11	A13	A22	A22	A12		A12	–
12	A12	A21	A21	A11		A11	–
13	A11	A20	P	A10	AP	A10	–
14	A10	A19	A10	A9		A9	–
15	A09	A18	A9	A8		A8	A8
16	A08	A17	A8	A7		A7	A7
17	A07	A16	A7	A6		A6	A6
18	A06	A15	A6	A5		A5	A5
19	A05	A14	A5	A4		A4	A4
20	A04	A13	A4	A3		A3	A3
21	A03	A12	A3	A2		A2	A2
22	A02	A11	A2	A1		A1	A1
23	A01	A10	A1	A0		A0	A0
24	DQ15 to DQ08			DQ[15:8]			
25	DQ07 to DQ00			DQ[7:0]			

Figure 15.72 SDRAM connection example with 256-Mb × 1 and 16-bit bus

15.6.14 Constraints

(1) Low-power states

In Software Standby and Deep Software Standby modes, auto-refresh operation is not available because the clock supply to the SDRAMC is stopped. To retain the data in the SDRAM when the SDRAM is externally connected, use the self-refresh function. For the procedure for transitioning to and recovering from self-refresh mode, see section 15.6.7, Self-Refresh.

(2) Setting the SDRAM Timing Register

Set the RAS[2:0] bits in the SDRAM Timing Register (SDTR) to a value less than or equal to the sum of the row column latency (SDTR.RCD[1:0]) and column latency (SDTR.CL[2:0]) settings. Operation is not guaranteed if this condition is not satisfied.

(3) Instruction code constraint

You must fix the instruction code to little-endian order.

15.7 Bus Error Monitoring Section

This monitoring system monitors each individual area, and whenever it detects an error, it returns the error to the requesting master IP using the AHB-Lite error response protocol.

This MCU (shift amount: 9 bits)				SDRAM (256 Mb, with 16-bit bus)			
No.	引脚名称	Row	Column	引脚名称	BA/AP	Row	Column
1	RAS			RAS#			
2	CAS			CAS#			
3	WE			WE#			
4	CKE			CKE			
5	SDCS			CS#			
6	SDCLK			CLK			
7	DQM1			UDQM			
8	DQM0			LDQM			
9	A15	A24	A24	BA1(A14)	BA1	–	–
10	A14	A23	A23	BA0(A13)	BA0	–	–
11	A13	A22	A22	A12		A12	–
12	A12	A21	A21	A11		A11	–
13	A11	A20	P	A10	AP	A10	–
14	A10	A19	A10	A9		A9	–
15	A09	A18	A9	A8		A8	A8
16	A08	A17	A8	A7		A7	A7
17	A07	A16	A7	A6		A6	A6
18	A06	A15	A6	A5		A5	A5
19	A05	A14	A5	A4		A4	A4
20	A04	A13	A4	A3		A3	A3
21	A03	A12	A3	A2		A2	A2
22	A02	A11	A2	A1		A1	A1
23	A01	A10	A1	A0		A0	A0
24	DQ15 to DQ08			DQ[15:8]			
25	DQ07 to DQ00			DQ[7:0]			

Figure 15.72 使用256−Mb×1和16位总线的SDRAM连接示例

15.6.14 Constraints

(1) Low-power states

在软件待机和深度软件待机模式下，自动刷新操作不可用，因为SDRAMC的时钟供应已停止。要在外接SDRAM时保留SDRAM中的数据，请使用自刷新功能。有关转换到自刷新模式和从自刷新模式恢复的过程，请参阅第15.6.7节，SelfRefresh。

(2) 设置SDRAM时序寄存器

将SDRAM时序寄存器(SDTR)中的RAS[2:0]位设置为小于或等于行列延迟(SDTR.RCD[1:0])和列延迟(SDTR.CL[2:0])设置。如果不满足此条件，则无法保证操作。

(3) 指令码约束

您必须将指令代码修复为little−endian顺序。

15.7 总线错误监控部分

该监控系统监控每个单独的区域，当它检测到错误时，它会使用AHB−Lite错误响应协议将错误返回给请求的主IP。

15.7.1 Bus Error Types

The following types of errors can occur on each bus:

- Illegal address access
- Bus master MPU error
- Bus slave MPU error
- Timeout.

Table 15.20 lists the address ranges where access leads to illegal address access errors. The reserved area in the slave does not trigger an illegal address access error. For more information on the bus master MPU and bus slave MPU, see section 16, Memory Protection Unit (MPU).

15.7.2 Operation When a Bus Error Occurs

When a bus error occurs, operation is not guaranteed and the error is returned to the requesting master IP. The bus errors that occur for each master are stored in the BUSnERRADD and BUSnERRSTAT registers. These registers must only be cleared by a reset. For more information, see section 15.3.21, Bus Error Address Register (BUSnERRADD) (n = 1 to 11) and section 15.3.22, Bus Error Status Register (BUSnERRSTAT) (n = 1 to 11).

Note: The DMAC and DTC do not receive bus errors. If the DMAC or DTC accesses the bus, the transfer continues. For other masters that receive bus errors, see the following sections:

- section 31, Ethernet DMA Controller (EDMAC)
- section 56, 2D Drawing Engine (DRW)
- section 57, JPEG Codec (JPEG)
- section 58, Graphics LCD Controller (GLCDC).

15.7.3 Conditions Leading to Illegal Address Access Errors

Table 15.20 lists the address spaces for each bus that trigger illegal address access errors.

Table 15.20 Conditions leading to illegal address access errors (1 of 2)

Address	Slave bus name	Master bus			
		CPU (ICode, DCode, System)	DMA	ETHER	GPX
0000 0000h to 01FF FFFFh	Memory bus 1 Memory bus 3	—	—	—	—
0200 0000h to 027F FFFFh	Memory mapping area	*1	E	E	E
0280 0000h to 1FFD FFFFh	Reserved	E	E	E	E
1FFE 0000h to 1FFF FFFFh	Memory bus 2 Memory bus 3	—	—	—	—
2000 0000h to 2003 FFFFh	Memory bus 4	—	—	—	—
2004 0000h to 200F FFFFh	Memory bus 5	—	—	—	—
2010 0000h to 3FFF FFFFh	Reserved	E	E	E	E
4000 0000h to 4001 FFFFh	Peripheral bus 1	—	—	E	E
4002 0000h to 4003 FFFFh	Reserved	E	E	E	E
4004 0000h to 4005 FFFFh	Peripheral bus 3	—	—	E	E
4006 0000h to 4007 FFFFh	Peripheral bus 4	—	—	E	E
4008 0000h to 4009 FFFFh	Peripheral bus 5	—	—	E	E
400A 0000h to 400B FFFFh	Reserved	—	—	E	E
400C 0000h to 400D FFFFh	Peripheral bus 7	—	—	E	E
400E 0000h to 400F FFFFh	Peripheral bus 8	—	—	E	E
4010 0000h to 407F FFFFh	Peripheral bus 9	—	—	—	E

15.7.1 总线错误类型

每条总线上都可能发生以下类型的错误：

- 非法地址访问
- 总线主控MPU错误
- 总线从机MPU错误
- Timeout.

表15.20列出了访问导致非法地址访问错误的地址范围。从机中的保留区域不会触发非法地址访问错误。有关总线主控MPU和总线从属MPU的更多信息，请参阅第16节，内存保护单元(MPU)。

15.7.2 发生总线错误时的操作

当发生总线错误时，无法保证操作，错误会返回到请求的主IP。每个主机发生的总线错误存储在BUSnERRADD和BUSnERRSTAT寄存器中。这些寄存器只能通过复位清除。有关详细信息，请参阅第15.3.21节，总线错误地址寄存器(BUSnERRADD)（n=1到11）和第15.3.22节，总线错误状态寄存器(BUSnERRSTAT)（n=1到11）。

Note: DMAC和DTC不接收总线错误。如果DMAC或DTC访问总线，则传输继续。对于接收到总线错误的其他主机，请参阅以下部分：

- 第31节，以太网DMA控制器(EDMAC)
- 第56节，2D绘图引擎(DRW)
- 第57节，JPEG编解码器(JPEG)
- 第58节，图形LCD控制器(GLCDC)。

15.7.3 导致非法地址访问错误的条件

表15.20列出了触发非法地址访问错误的每条总线的地址空间。

Table 15.20 导致非法地址访问错误的条件(1of2)

Address	从总线名称	主总线			
		CPU (ICode, DCode, System)	DMA	ETHER	GPX
0000 0000h to 01FF FFFFh	内存总线1内存总线3	—	—	—	—
0200 0000h to 027F FFFFh	内存映射区	*1	E	E	E
0280 0000h to 1FFD FFFFh	Reserved	E	E	E	E
1FFE 0000h to 1FFF FFFFh	内存总线2内存总线3	—	—	—	—
2000 0000h to 2003 FFFFh	内存总线4	—	—	—	—
2004 0000h to 200F FFFFh	内存总线5	—	—	—	—
2010 0000h to 3FFF FFFFh	Reserved	E	E	E	E
4000 0000h to 4001 FFFFh	外围总线1	—	—	E	E
4002 0000h to 4003 FFFFh	Reserved	E	E	E	E
4004 0000h to 4005 FFFFh	外围总线3	—	—	E	E
4006 0000h to 4007 FFFFh	外围总线4	—	—	E	E
4008 0000h to 4009 FFFFh	周边总线5	—	—	E	E
400A 0000h to 400B FFFFh	Reserved	—	—	E	E
400C 0000h to 400D FFFFh	周边总线7	—	—	E	E
400E 0000h to 400F FFFFh	外围总线8	—	—	E	E
4010 0000h to 407F FFFFh	周边总线9	—	—	—	E

Table 15.20 Conditions leading to illegal address access errors (2 of 2)

Address	Slave bus name	Master bus			
		CPU (ICode, DCode, System)	DMA	ETHER	GPX
4080 0000h to 5FFF FFFFh	Reserved	E	E	E	E
6000 0000h to 67FF FFFFh	QSPI area	—	—	—	—
6800 0000h to 7FFF FFFFh	Reserved	E	E	E	E
8000 0000h to 97FF FFFFh	CS/SDRAM area	—	—	—	—
9800 0000h to DFFF FFFFh	Reserved	E	E	E	E
E000 0000h to FFFF FFFFh	System for Cortex-M4	—	E	E	E

E: Path where an illegal address access error occurs

Note 1. The bus module does not detect whether the MMF switched the address. Therefore, if the MMF is enabled and the CPU accesses 0200 0000h, no error occurs. This depends on the switched address.
If the MMF is disabled and the CPU accesses 0200 0000h, the bus module can detect the error.

The bus module detects an access error resulting from access to a reserved area, for example if no area is assigned to the slave.

- 0200 0000h to 1FFD FFFFh: access error detection
- 0000 0000h to 01FF FFFFh: memory bus 1 no access error detection.

15.7.4 Timeout

For some peripheral modules, a timeout error occurs with the module-stop function. When there is no response from the slave for a certain period of time, a timeout error is detected. A timeout error is returned to the requesting master IP using the AHB-Lite error response protocol.

15.8 Notes on Using Flash Cache

When using flash cache through access from the CPU, the Arm® MPU should also be set to cacheable. See references 1. and 2. for more information.

15.9 References

1. *ARM®v7-M Architecture Reference Manual* (ARM DDI 0403D)
2. *ARM® Cortex®-M4 Devices Generic User Guide* (ARM DUI 0553A).

Table 15.20 导致非法地址访问错误的条件(2of2)

Address	从总线名称	主总线			
		CPU (ICode, DCode, System)	DMA	ETHER	GPX
4080 0000h to 5FFF FFFFh	Reserved	E	E	E	E
6000 0000h to 67FF FFFFh	QSPI area	—	—	—	—
6800 0000h to 7FFF FFFFh	Reserved	E	E	E	E
8000 0000h to 97FF FFFFh	CS/SDRAM area	—	—	—	—
9800 0000h to DFFF FFFFh	Reserved	E	E	E	E
E000 0000h to FFFF FFFFh	Cortex-M4系统	—	E	E	E

E：发生非法地址访问错误的路径

注1.总线模块不检测MMF是否切换了地址。因此，如果启用MMF并且CPU访问02000000h，则不会发生错误。这取决于交换的地址。如果MMF被禁用并且CPU访问02000000h，则总线模块可以检测到错误。

总线模块检测到因访问保留区域而导致的访问错误，例如，如果没有为从站分配区域。

- 02000000h至1FFDFFFFh：访问错误检测
- 00000000h至01FFFFFFh：内存总线1无访问错误检测。

15.7.4 Timeout

对于某些外围模块，模块停止功能会发生超时错误。当从机在一段时间内没有响应时，检测到超时错误。使用AHB-Lite错误响应协议将超时错误返回给请求的主IP。

15.8 使用FlashCache的注意事项

当通过CPU访问使用闪存缓存时，Arm®MPU也应设置为可缓存。有关详细信息，请参阅参考文献1.和2.。

15.9 References

1. ARM®v7-M架构参考手册(ARMDDI0403D)
2. ARM®Cortex®-M4设备通用用户指南(ARMDUI0553A)。

16. Memory Protection Unit (MPU)

16.1 Overview

The MCU provides four Memory Protection Units (MPUs) and a CPU stack pointer monitor function. Table 16.1 lists the MPU specifications and Table 16.2 shows the behavior on detection of each MPU error.

Table 16.1 MPU specifications

Classification	Module/Function	Description
Illegal memory access	Arm® Cortex®-M4 CPU	• Arm CPU has a default memory map. If the CPU makes an illegal access, an exception interrupt occurs. • MPU can change a default memory map.
	CPU stack pointer monitor	2 regions: • Main Stack Pointer (MSP) • Process Stack Pointer (PSP).
Memory protection	Arm MPU	Memory protection function for the CPU: • 8 MPU regions with subregions and background region.
	Bus master MPU	Memory protection function for each bus master except for the CPU: • Bus master MPU group A: 32 regions • Bus master MPU group B: 8 regions • Bus master MPU group C: 8 regions.
	Bus slave MPU	Memory protection function for each bus slave.
Security	Security MPU	Protects against non-secure program access to the following secure regions: • 2 regions (PC) • 4 regions (code flash, SRAM, two secure functions).

Table 16.2 Behavior on MPU error detection

MPU type	Notification type	Bus access on error detection	Storing of error access information
CPU stack pointer monitor	Reset or non-maskable interrupt	Don't care	Not stored
Arm MPU	Hard fault	• Does not correctly have write access • Does not correctly have read access.	Stored in the Cortex-M4 processor
Bus master MPU	Reset or non-maskable interrupt	• Write access to the protected region • Read access to the protected region.	Stored
Bus slave MPU	• Reset or non-maskable interrupt • Hard fault.	• Write access ignored • Read access read as 0.	Stored
Security MPU	Not notified	• Does not correctly have write access • Does not correctly have read access.	Do not hold

For information on error access for the Arm MPU, see section 16.7. For information on error access for other MPUs, see section 15.3.21, Bus Error Address Register (BUSnERRADD) (n = 1 to 11) and section 15.3.22, Bus Error Status Register (BUSnERRSTAT) (n = 1 to 11) in section 15, Buses.

16.2 CPU Stack Pointer Monitor

The CPU stack pointer monitor detects underflows and overflows of the stack pointer. Because the Arm CPU has two stack pointers, a Main Stack Pointer (MSP) and Process Stack Pointer (PSP), it supports two CPU stack pointer monitors. If a stack pointer underflow or overflow is detected, the CPU stack pointer monitor generates a reset or a non-maskable interrupt.

16. 内存保护单元(MPU)

16.1 Overview

MCU提供四个内存保护单元(MPU)和一个CPU堆栈指针监控功能。表16.1列出了MPU规格和表16.2显示了检测每个MPU错误时的行为。

Table 16.1 MPU specifications

Classification	Module/Function	Description
非法内存访问	Arm®Cortex®–M4CPU	ArmCPU有一个默认的内存映射。如果CPU进行非法访问，则会发生异常中断。MPU可以更改默认内存映射。
	CPU堆栈指针监视器	2个区域： 主堆栈指针(MSP) 进程堆栈指针(PSP)。
内存保护	Arm MPU	CPU的内存保护功能： 8个带有子区域和背景区域的MPU区域。
	总线主控MPU	除CPU外的每个总线主控器的内存保护功能： 总线主控MPU组A：32个区域 总线主控MPU组B：8个区域 总线主控MPU组C：8个区域。
	总线从机MPU	每个总线从机的内存保护功能。
Security	Security MPU	防止非安全程序访问以下安全区域： 2个区域(PC) 4个区域（代码闪存、SRAM、两个安全功能）。

Table 16.2 MPU错误检测的行为

MPU type	通知类型	错误检测时的总线访问	存储错误访问信息
CPU堆栈指针监视器	复位或不可屏蔽中断	Don't care	未存储
Arm MPU	硬故障	没有正确的写入权限 没有正确的读取权限。	存储在Cortex-M4处理器中
总线主控MPU	复位或不可屏蔽中断	对受保护区域的写访问权 对受保护区域的读访问权。	Stored
总线从机MPU	复位或不可屏蔽中断 硬故障。	写访问被忽略 读访问读为0。	Stored
Security MPU	未通知	没有正确的写入权限 没有正确的读取权限。	不要持有

有关ArmMPU的错误访问的信息，请参阅第16.7节。有关其他MPU的错误访问的信息，请参阅第15.3.21节，总线错误地址寄存器(BUSnERRADD)(n=1到11)和第15.3.22节，总线错误状态寄存器(BUSnERRSTAT)(n=1到11)第15节，公共汽车。

16.2 CPU堆栈指针监视器

CPU堆栈指针监视器检测堆栈指针的下溢和溢出。由于ArmCPU有两个堆栈指针，一个主堆栈指针(MSP)和一个进程堆栈指针(PSP)，因此它支持两个CPU堆栈指针监视器。如果检测到堆栈指针下溢或溢出，CPU堆栈指针监视器会生成复位或不可屏蔽中断。

To enable the CPU stack pointer monitor, set the Stack Pointer Monitor Enable bit in the Stack Pointer Monitor Access Control Register (MSPMPUCTL, PSPMPUCTL) to 1.

Table 16.3 lists the specifications of the CPU stack pointer monitor, Figure 16.1 shows a block diagram, and Figure 16.2 shows the register setting flow.

Table 16.3 CPU stack pointer monitor specifications

Parameter	Description
Protected region	SRAM region
Number of regions	2 regions: • Main Stack Pointer • Process Stack Pointer.
Address specification for individual regions	Region start and end addresses configurable
Stack pointer monitor enable or disable setting for individual regions	Stack pointer monitor for individual regions can be enabled or disabled
Operation on error detection	Reset or non-maskable interrupts can be generated
Register protection	Registers can be protected from illegal writes

要启用CPU堆栈指针监视器，请设置堆栈指针监视器访问中的堆栈指针监视器启用位控制寄存器(MSPMPUCTL PSPMPUCTL)为1。

表16.3列出了CPU堆栈指针监视器的规格，图16.1显示了框图，图16.2显示了寄存器设置流程。

Table 16.3 CPU堆栈指针监视器规格

Parameter	Description
保护区	SRAM region
地区数量	2个区域： 主堆栈指针 进程堆栈指针。
个别地区的地址规范	区域开始和结束地址可配置
堆栈指针监视器启用或禁用各个区域的设置	可以启用或禁用各个区域的堆栈指针监视器
错误检测操作	可以产生复位或不可屏蔽中断
注册保护	可以保护寄存器免受非法写入

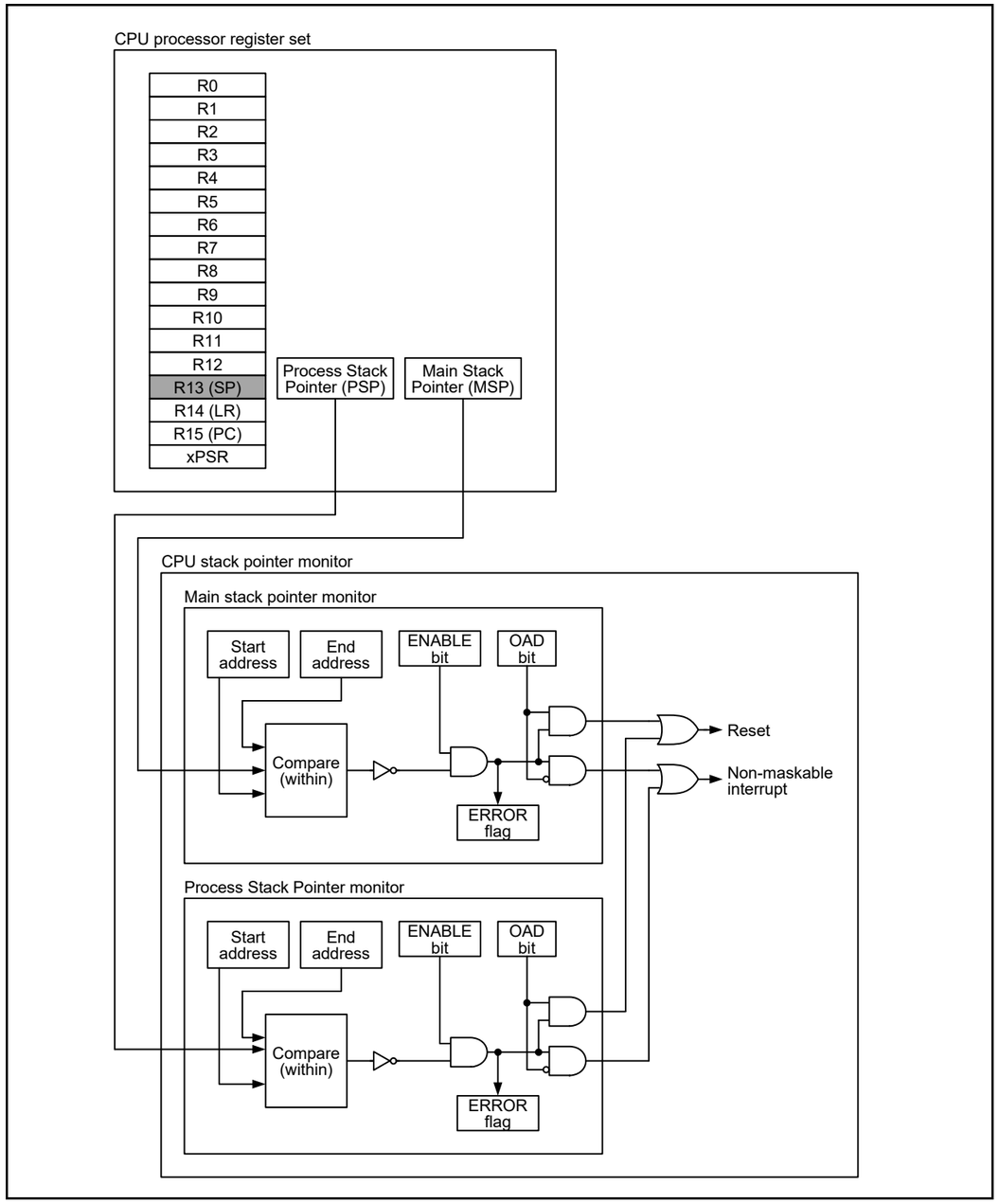


Figure 16.1 CPU stack pointer monitor block diagram

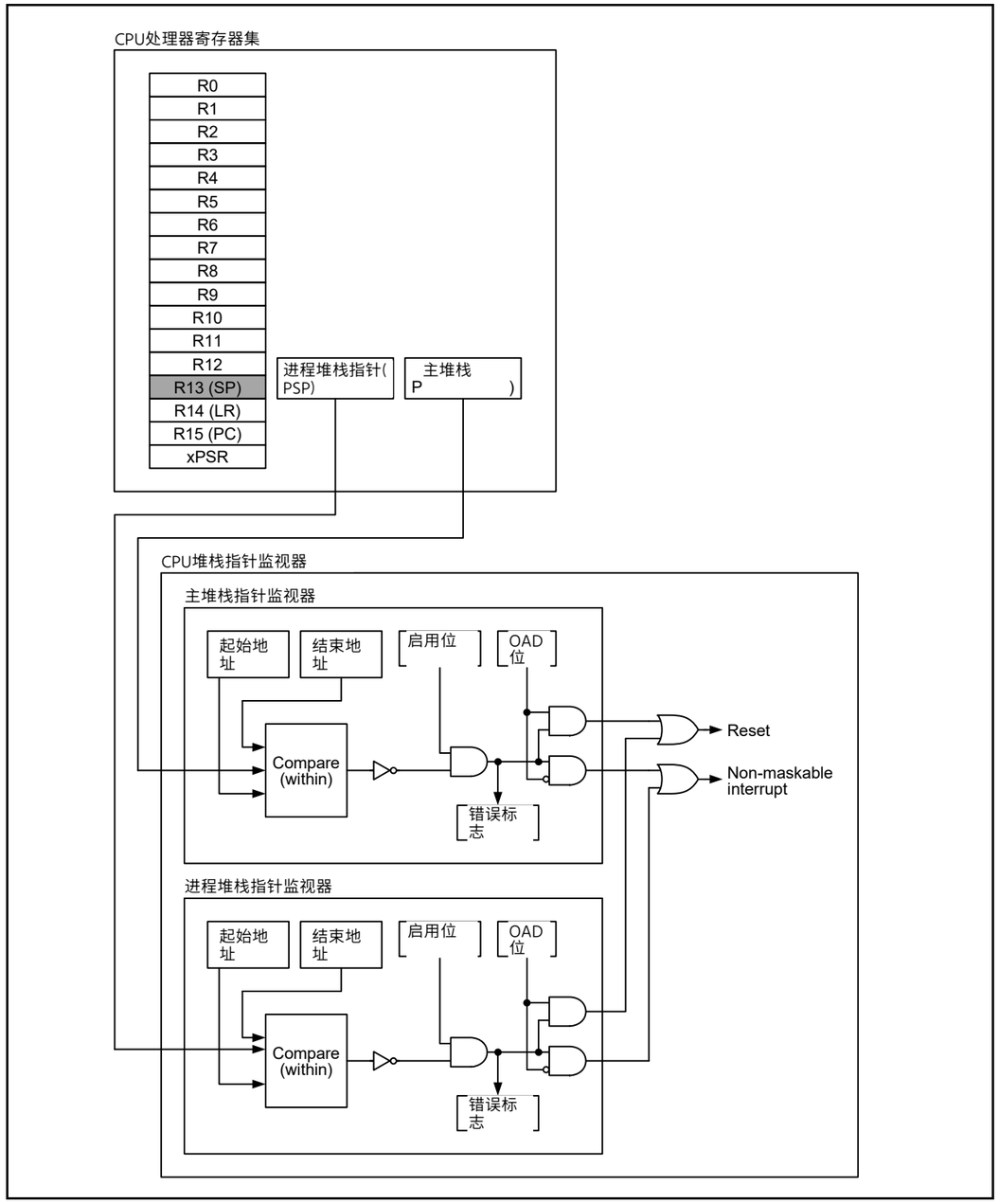


Figure 16.1 CPU堆栈指针监视器框图

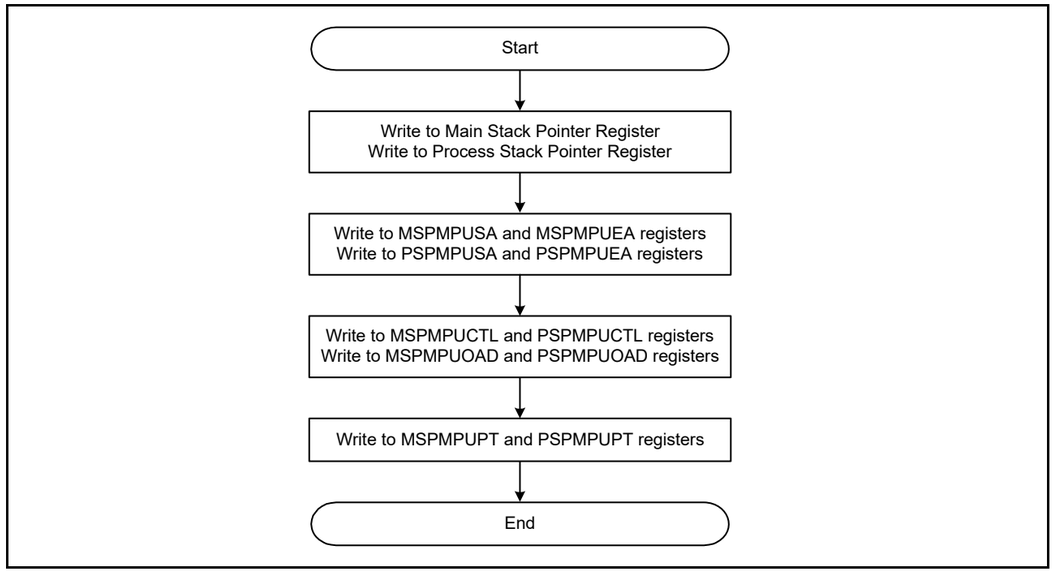


Figure 16.2 Register setting flow

16.2.1 Register Descriptions

Note: Bus access must be stopped before writing to MPU registers.

16.2.1.1 Main Stack Pointer Monitor Start Address Register (MSPMPUSA)

Address(es): SPMON.MSPMPUSA 4000 0D08h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	MSPMPUSA[31:16]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MSPMPUSA[15:0]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0	0

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b31 to b0	MSPMPUSA[31:0]	Region Start Address	Address where the region starts, for use in region determination. The lower 2 bits should be 0. The value range must be 1FF0 0000h to 200F FFFCh, excluding reserved areas.	R/W

The MSPMPUSA and MSPMPUEA registers specify the CPU stack region in the SRAM (1FF0 0000h to 200F FFFFh, excluding reserved areas). For SRAM area to be covered, see Figure 4.1, Memory map.

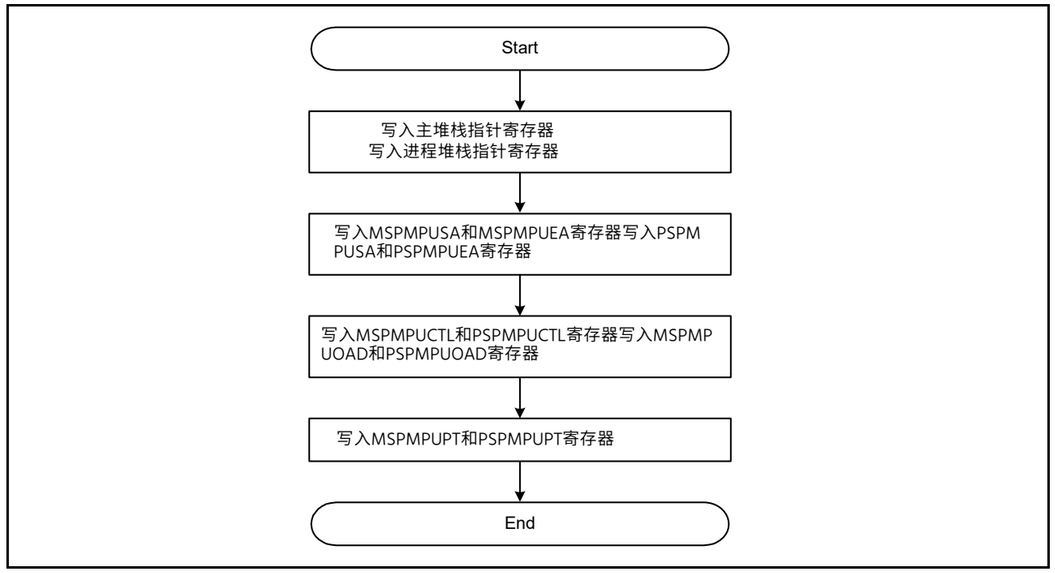


Figure 16.2 注册设置流程

16.2.1 注册说明

Note: 在写入MPU寄存器之前必须停止总线访问。

16.2.1.1 主堆栈指针监视器起始地址寄存器(MSPMPUSA)

Address(es): SPMON.MSPMPUSA 4000 0D08h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	MSPMPUSA[31:16]															
重置后的值:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MSPMPUSA[15:0]															
重置后的值:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0	0

x: Undefined

Bit	Symbol	位名称	Description	R/W
b31 to b0	MSPMPUSA[31:0]	区域起始地址	区域开始的地址，用于区域确定。 低2位应为0。取值范围必须为1FF00000h到200FFFFCh，不包括保留区。	R/W

MSPMPUSA和MSPMPUEA寄存器指定SRAM中的CPU堆栈区域（1FF00000h到200FFFFFh，不包括保留区域）。对于要覆盖的SRAM区域，请参见图4.1，存储器映射。

16.2.1.2 Main Stack Pointer Monitor End Address Register (MSPMPUEA)

Address(es): SPMON.MSPMPUEA 4000 0D0Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	MSPMPUEA[31:16]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MSPMPUEA[15:0]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	1	1

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b31 to b0	MSPMPUEA[31:0]	Region End Address	Address where the region ends, for use in region determination. The lower 2 bits should be 1. The value range must be 1FF0 0003h to 200F FFFFh, excluding reserved areas.	R/W

16.2.1.3 Process Stack Pointer Monitor Start Address Register (PSPMPUSA)

Address(es): SPMON.PSPMPUSA 4000 0D18h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	PSPMPUSA[31:16]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PSPMPUSA[15:0]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0	0

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b31 to b0	PSPMPUSA[31:0]	Region Start Address	Address where the region starts, for use in region determination. The lower 2 bits should be 0. The value range must be 1FF0 0000h to 200F FFFCh, excluding reserved areas.	R/W

The PSPMPUSA and PSPMPUEA registers specify the CPU stack region in the SRAM (1FF0 0000h to 200F FFFFh, excluding reserved areas). For SRAM area to be covered, see Figure 4.1, Memory map.

16.2.1.2 主堆栈指针监视器结束地址寄存器(MSPMPUEA)

Address(es): SPMON.MSPMPUEA 4000 0D0Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	MSPMPUEA[31:16]															
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MSPMPUEA[15:0]															
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	1	1

x: Undefined

Bit	Symbol	位名称	Description	R/W
b31 to b0	MSPMPUEA[31:0]	区域结束地址	区域结束的地址，用于区域确定。 低2位应为1。取值范围必须为1FF00003h到200FFFFFh，不包括保留区。	R/W

16.2.1.3 进程堆栈指针监视器起始地址寄存器(PSPMPUSA)

Address(es): SPMON.PSPMPUSA 4000 0D18h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	PSPMPUSA[31:16]															
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PSPMPUSA[15:0]															
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0	0

x: Undefined

Bit	Symbol	位名称	Description	R/W
b31 to b0	PSPMPUSA[31:0]	区域起始地址	区域开始的地址，用于区域确定。 低2位应为0。取值范围必须为1FF00000h到200FFFFCh，不包括保留区。	R/W

PSPMPUSA和PSPMPUEA寄存器指定SRAM中的CPU堆栈区域（1FF00000h到200FFFFFh，不包括保留区域）。对于要覆盖的SRAM区域，请参见图4.1，存储器映射。

16.2.1.4 Process Stack Pointer Monitor End Address Register (PSPMPUEA)

Address(es): SPMON.PSPMPUEA 4000 0D1Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	PSPMPUEA[31:16]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PSPMPUEA[15:0]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	1	1

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b31 to b0	PSPMPUEA[31:0]	Region End Address	Address where the region ends, for use in region determination. The lower 2 bits should be 1. The value range must be 1FF0 0003h to 200F FFFFh, excluding reserved areas.	R/W

16.2.1.5 Stack Pointer Monitor Operation After Detection Register (MSPMPUOAD, PSPMPUOAD)

Address(es): SPMON.MSPMPUOAD 4000 0D00h, SPMON.PSPMPUOAD 4000 0D10h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	KEY[7:0]								—	—	—	—	—	—	—	OAD
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	OAD	Operation after Detection	0: Non-maskable interrupt 1: Reset.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15 to b8	KEY[7:0]	Key Code	These bits enable or disable writes to the OAD bit.	R/(W)*1

Note 1. Write data is not saved.

OAD bit (Operation after Detection)

The OAD bit selects either a reset or a non-maskable interrupt to occur when a stack pointer underflow or overflow is detected by the CPU stack pointer monitor. The main and the process stack pointer monitors each use an OAD bit to determine which signal is generated when a stack pointer underflow or overflow is detected. When writing to the OAD bit, write A5h simultaneously to the KEY[7:0] bits using halfword access.

KEY[7:0] bits (Key Code)

The KEY[7:0] bits enable or disable writing to the OAD bit. When writing to the OAD bit, write A5h simultaneously to the KEY[7:0] bits. When values other than A5h are written to the KEY[7:0] bits, the OAD bit is not updated. The KEY[7:0] bits are always read as 00h.

16.2.1.4 进程堆栈指针监视器结束地址寄存器(PSPMPUEA)

Address(es): SPMON.PSPMPUEA 4000 0D1Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	PSPMPUEA[31:16]															
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PSPMPUEA[15:0]															
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	1	1

x: Undefined

Bit	Symbol	位名称	Description	R/W
b31 to b0	PSPMPUEA[31:0]	区域结束地址	区域结束的地址，用于区域确定。 低2位应为1。取值范围必须为1FF00003h到200FFFFFh，不包括保留区。	R/W

16.2.1.5 检测寄存器后的堆栈指针监视器操作（MSPPUOAD，PSPMPUOAD)

Address(es): SPMON.MSPMPUOAD 4000 0D00h, SPMON.PSPMPUOAD 4000 0D10h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	KEY[7:0]								—	—	—	—	—	—	—	OAD
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	OAD	检测后的操作	0：不可屏蔽中断1：复位 。	R/W
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b15 to b8	KEY[7:0]	关键代码	这些位启用或禁用对OAD位的写入。	R/(W)*1

注1.写入数据不保存。

OAD位（检测后操作）

当CPU堆栈指针监视器检测到堆栈指针下溢或溢出时，OAD位选择发生复位或不可屏蔽中断。主堆栈指针监视器和进程堆栈指针监视器各自使用一个OAD位来确定在检测到堆栈指针下溢或溢出时生成哪个信号。写入OAD位时，使用半字访问同时将A5h写入KEY[7:0]位。

KEY[7:0]位（键码）

KEY[7:0]位启用或禁用写入OAD位。写入OAD位时，同时将A5h写入KEY[7:0]位。将A5h以外的值写入KEY[7:0]位时，不会更新OAD位。KEY[7:0]位总是读为00h。

16.2.1.6 Stack Pointer Monitor Access Control Register (MSPMPUCTL, PSPMPUCTL)

Address(es): SPMON.MSPMPUCTL 4000 0D04h, SPMON.PSPMPUCTL 4000 0D14h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	ERROR	—	—	—	—	—	—	—	ENABLE
Value after reset:	0	0	0	0	0	0	0	0/1*1	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	ENABLE	Stack Pointer Monitor Enable	0: Disable stack pointer monitor 1: Enable stack pointer monitor.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	ERROR	Stack Pointer Monitor Error Flag	0: No stack pointer overflow and underflow occurred 1: Stack pointer overflow or underflow occurred.	R/W
b15 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. The initial value depends on the reset generation source.

ENABLE bit (Stack Pointer Monitor Enable)

The ENABLE bit enables or disables the stack pointer monitor function, independently set for the main stack pointer monitor and the process stack pointer monitor.

When the MSPMPUCTL.ENABLE bit is set to 1, the following registers are available:

- MSPMPUSA
- MSPMPUEA
- MSPMPUOAD.

When the PSPMPUCTL.ENABLE bit is set to 1, the following registers are available:

- PSPMPUSA
- PSPMPUEA
- PSPMPUOAD.

ERROR bit (Stack Pointer Monitor Error Flag)

The ERROR bit indicates the status of the stack pointer monitor. Each stack pointer monitor has an independent ERROR bit. Only 0 can be written to this bit.

[Setting condition]

- Overflow or underflow of the stack pointer.

[Clearing conditions]

- 0 is written to this bit.
- A reset other than the bus master MPU error reset, bus slave MPU error reset, and stack pointer error reset.

Note: Only 0 can be written to the ERROR bit.

16.2.1.6 堆栈指针监视器访问控制寄存器(MSMPPUCTL PSPMPUCTL)

Address(es): SPMON.MSPMPUCTL 4000 0D04h, SPMON.PSPMPUCTL 4000 0D14h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	ERROR	—	—	—	—	—	—	—	ENABLE
重置后的值：	0	0	0	0	0	0	0	0/1*1	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	ENABLE	堆栈指针监视器 Enable	0：禁用堆栈指针监视器1：启用堆栈指针监视器。	R/W
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b8	ERROR	堆栈指针监视器错误标志	0：未发生堆栈指针上溢和下溢1：发生堆栈指针上溢或下溢。	R/W
b15 to b9	—	Reserved	这些位被读取为0。写入值应为0。	R/W

注1.初始值取决于复位产生源。

ENABLE位（堆栈指针监视器启用）

ENABLE位启用或禁用堆栈指针监视器功能，分别为主堆栈指针监视器和进程堆栈指针监视器设置。

当MSMPPUCTL.ENABLE位设置为1时，以下寄存器可用：

- MSPMPUSA
- MSPMPUEA
- MSPMPUOAD.

当PSPMPUCTL.ENABLE位设置为1时，以下寄存器可用：

- PSPMPUSA
- PSPMPUEA
- PSPMPUOAD.

ERROR位（堆栈指针监视器错误标志）

ERROR位指示堆栈指针监视器的状态。每个堆栈指针监视器都有一个独立的ERROR位。该位只能写入0。

[Setting condition]

- 堆栈指针上溢或下溢。

[Clearing conditions]

- 0写入该位。
- 总线主MPU错误复位、总线从MPU错误复位和堆栈指针错误复位以外的复位。

Note: ERROR位只能写入0。

16.2.1.7 Stack Pointer Monitor Protection Register (MSPMPUPT, PSPMPUPT)

Address(es): SPMON.MSPMPUPT 4000 0D06h, SPMON.PSPMPUPT 4000 0D16h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	KEY[7:0]								—	—	—	—	—	—	—	PROTECT
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	PROTECT	Protection of Register	0: Stack pointer monitor register writes are permitted 1: Stack pointer monitor register writes are protected. Reads are permitted.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15 to b8	KEY[7:0]	Key Code	These bits enable or disable writes to the PROTECT bit.	R/(W)*1

Note 1. Write data is not saved.

PROTECT bit (Protection of Register)

The PROTECT bit enables or disables writes to the associated registers to be protected, independently set for the Main Stack Pointer monitor and the Process Stack Pointer monitor.

MSPMPUPT.PROTECT controls the following Main Stack Pointer protection registers:

- MSPMPUCTL
- MSPMPUSA
- MSPMPUEA.

PSPMPUT.PROTECT controls the following Process Stack Pointer protection registers:

- PSPMPUCTL
- PSPMPUSA
- PSPMPUEA.

When writing to the PROTECT bit, write A5h simultaneously to the KEY[7:0] bits, using halfword access.

KEY[7:0] bits (Key Code)

The KEY[7:0] bits enable or disable writing to the PROTECT bit. When writing to the PROTECT bit, write A5h simultaneously to the KEY[7:0] bits. When other values are written, the PROTECT bit is not updated. The KEY[7:0] bits are always read as 00h.

16.2.2 Operation

16.2.2.1 Protecting the registers

To protect registers related to the CPU stack pointer monitor, set the associated PROTECT bit.

16.2.2.2 Overflow and underflow errors

The CPU stack pointer monitor generates an error if an overflow or underflow error is detected. Set the OAD bit to select whether the error is reported as a non-maskable interrupt or reset. The non-maskable interrupt status is indicated in ICU.NMISR.SPEST, see section 14, Interrupt Controller Unit (ICU). Reset status is indicated in SYSTEM.RSTSR1.SPERF, see section 6, Resets.

When ICU.NMISR.SPEST indicates that a CPU stack pointer monitor interrupt occurred, confirm it by checking the ERROR bit in MSPMPUCTL and PSPMPUCTL to determine whether the error is a main stack pointer monitor error or process stack pointer monitor error.

16.2.1.7 堆栈指针监视器保护寄存器(MSPMPUPT PSPMPUPT)

Address(es): SPMON.MSPMPUPT 4000 0D06h, SPMON.PSPMPUPT 4000 0D16h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	KEY[7:0]								—	—	—	—	—	—	—	PROTECT
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	PROTECT	登记保护	0：允许堆栈指针监视寄存器写入1：堆栈指针监视寄存器写入受到保护。允许读取。	R/W
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b15 to b8	KEY[7:0]	关键代码	这些位启用或禁用对PROTECT位的写入。	R/(W)*1

注1.写入数据不保存。

PROTECT位（寄存器保护）

PROTECT位启用或禁用对要保护的相关寄存器的写入，独立设置为Main
堆栈指针监视器和进程堆栈指针监视器。

MSPMPUPT.PROTECT控制以下主堆栈指针保护寄存器：

- MSPMPUCTL
- MSPMPUSA
- MSPMPUEA.

PSPMPUT.PROTECT控制以下进程堆栈指针保护寄存器：

- PSPMPUCTL
- PSPMPUSA
- PSPMPUEA.

写入PROTECT位时，使用半字访问同时将A5h写入KEY[7:0]位。

KEY[7:0]位（键码）

KEY[7:0]位启用或禁用对PROTECT位的写入。写入PROTECT位时，同时将A5h写入KEY[7:0]位。写入其他值时，PROTECT位不会更新。KEY[7:0]位总是读为00h。

16.2.2 Operation

16.2.2.1 保护寄存器

要保护与CPU堆栈指针监视器相关的寄存器，请设置相关的PROTECT位。

16.2.2.2 上溢和下溢错误

如果检测到上溢或下溢错误，CPU堆栈指针监视器会生成错误。设置OAD位以选择将错误报告为不可屏蔽中断还是复位。不可屏蔽中断状态在ICU.NMISR.SPEST中指示，参见第14节，中断控制器单元(ICU)。复位状态显示在

SYSTEM.RSTSR1.SPERF，参见第6节，重置。

当ICU.NMISR.SPEST指示发生CPU堆栈指针监视器中断时，请通过检查
MSPMPUCTL和PSPMPUCTL中的ERROR位来确定该错误是主堆栈指针监视器错误还是进程堆栈指针监视器错误。

A non-maskable interrupt remains set when a stack pointer overflows or underflows. To clear the error, clear the non-maskable interrupt flag by writing 1 to ICU.NMICLR.SPECLR. Write 0 to clear the ERROR bit in MSPMPUCTL and PSPMPUCTL.

16.3 Arm MPU

The Arm MPU has eight region MPUs and provides full support for:

- Protected regions
- Overlapping protected regions, with ascending priority:
  7 = highest priority
  0 = lowest priority.
- Access permissions
- Export of memory attributes to the system.

Arm MPU mismatches and permission violations invoke the programmable-priority MemManage fault (HardFault) handler. For details, see section 16.7.

16.4 Bus Master MPU

The bus master MPU monitors the addresses accessed by the bus masters in the entire address space (0000 0000h to FFFF FFFFh). The access control information, consisting of read and write permissions, can be independently set for up to 32 regions. The bus master MPU monitors access to each region based on these settings. If access to a protected region is detected, the bus master MPU generates a reset or a non-maskable interrupt. For details on error access, see section 15.3.21 and section 15.3.22 in section 15, Buses.

Table 16.4 lists the specifications of the bus master MPU and Figure 16.3 shows a block diagram. Figure 16.4 shows bus master MPU groups A, B, and C.

Table 16.4 Bus master MPU specifications

Parameter	Specifications
Protected master groups	• Bus master MPU group A: DMA bus • Bus master MPU group B: ETHER bus • Bus master MPU group C: GPX bus.
Protected region	0000 0000h to FFFF FFFFh
Number of regions	• Bus master MPU group A: 32 regions • Bus master MPU group B: 8 regions • Bus master MPU group C: 8 regions.
Address specification for individual regions	Region start and end addresses configurable
Enable/disable setting for memory protection in individual regions	Settings enabled or disabled for the associated region
Access-control settings for individual regions	Permission to read and write
Operation on error detection	Reset or non-maskable interrupt
Register protection	Register can be protected from illegal writes

当堆栈指针上溢或下溢时，不可屏蔽中断保持设置。要清除错误，请通过将1写入ICU.NMICLR.SPECLR来清除不可屏蔽中断标志。写入0以清除MSMPPUCTL和PSPMPUCTL中的ERROR位。

16.3 Arm MPU

ArmMPU有8个区域MPU，并为以下方面提供全面支持：

- 保护区
- 重叠的受保护区域，优先级升序：7=最高优先级0=
  最低优先级。
- 访问权限
- 将内存属性导出到系统。

ArmMPU不匹配和权限违规调用可编程优先级MemManage故障(HardFault)处理程序。有关详细信息，请参阅第16.7节。

16.4 总线主控MPU

总线主控MPU监视总线主控在整个地址空间（00000000h到FFFFFFFFh）。访问控制信息，由读写权限组成，最多可独立设置32个区域。总线主控MPU根据这些设置监控对每个区域的访问。如果检测到对受保护区域的访问，总线主控MPU会产生复位或不可屏蔽中断。有关错误访问的详细信息，请参阅第15节，总线中的第15.3.21节和第15.3.22节。

表16.4列出了总线主控MPU的规格，图16.3显示了框图。图16.4显示了总线主控MPU组A、B和C。

Table 16.4 总线主控MPU规格

Parameter	Specifications
受保护的主组	总线主控MPU组A：DMA总线 总线主控MPU组B：ETHER总线 总线主控MPU组C：GPX总线。
保护区	0000 0000h to FFFF FFFFh
地区数量	总线主控MPU组A：32个区域 总线主控MPU组B：8个区域 总线主控MPU组C：8个区域。
个别地区的地址规范	区域开始和结束地址可配置
在各个区域启用禁用内存保护设置	为关联区域启用或禁用的设置
各个区域的访问控制设置	读写权限
错误检测操作	复位或不可屏蔽中断
注册保护	可以保护寄存器免受非法写入

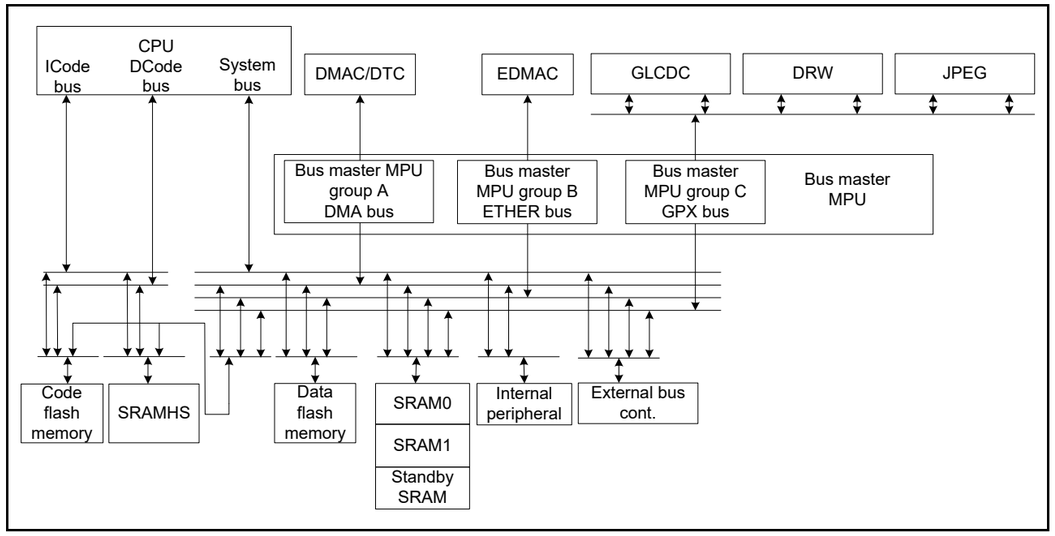


Figure 16.3 Bus master MPU block diagram

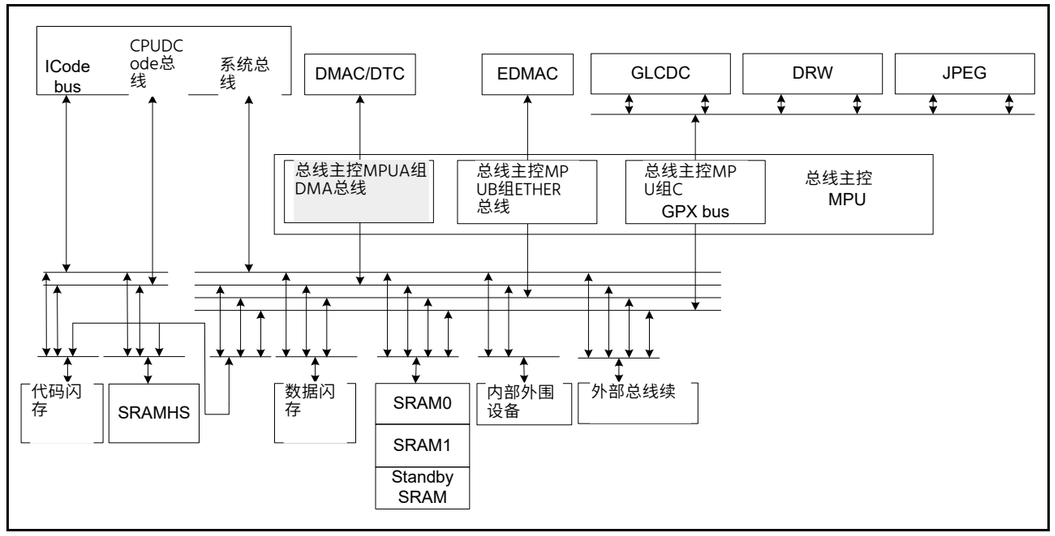


Figure 16.3 总线主控MPU框图

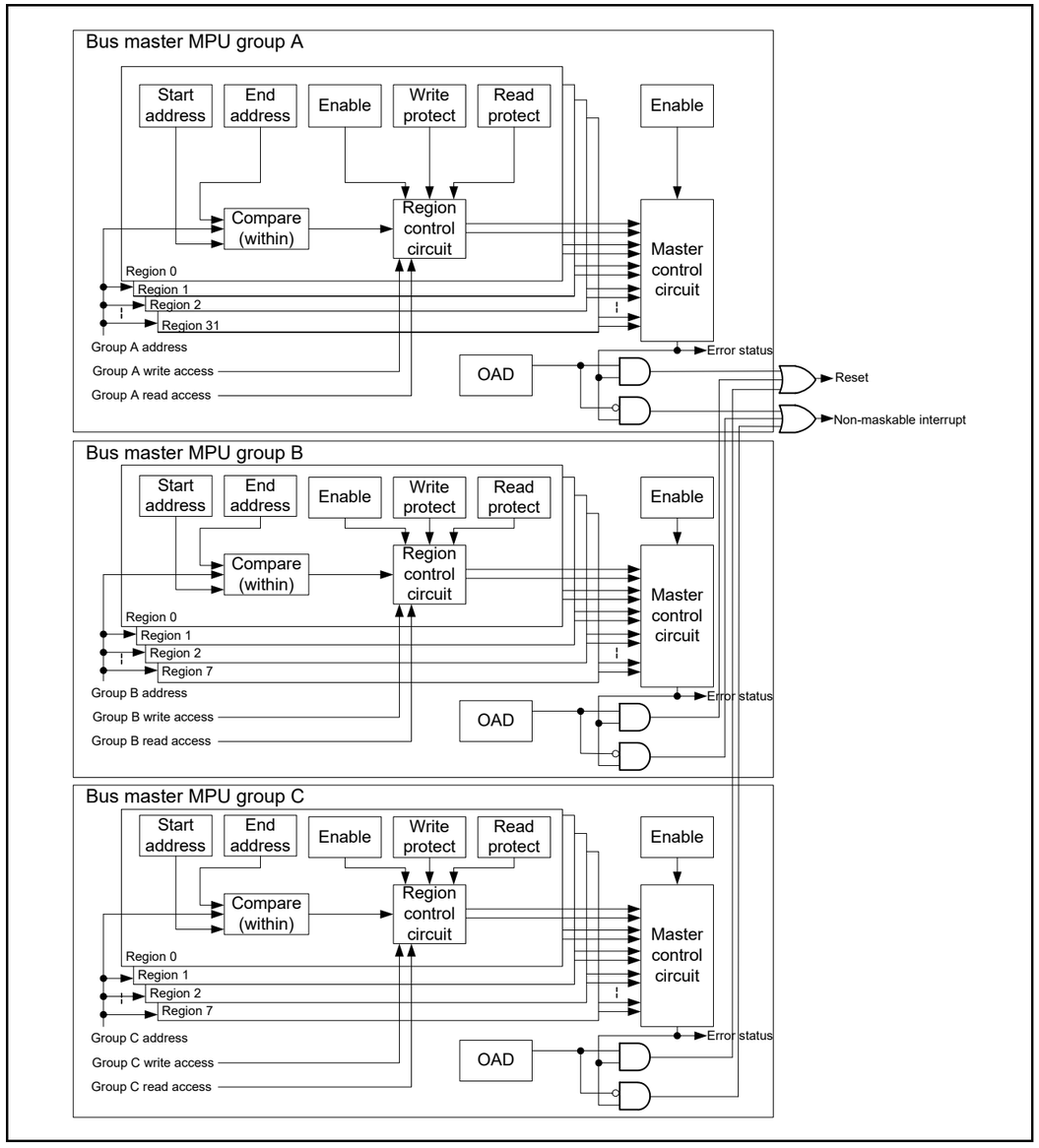


Figure 16.4 Bus master MPU groups A, B, and C

16.4.1 Register Descriptions

Note: Bus access must be stopped before writing to MPU registers.

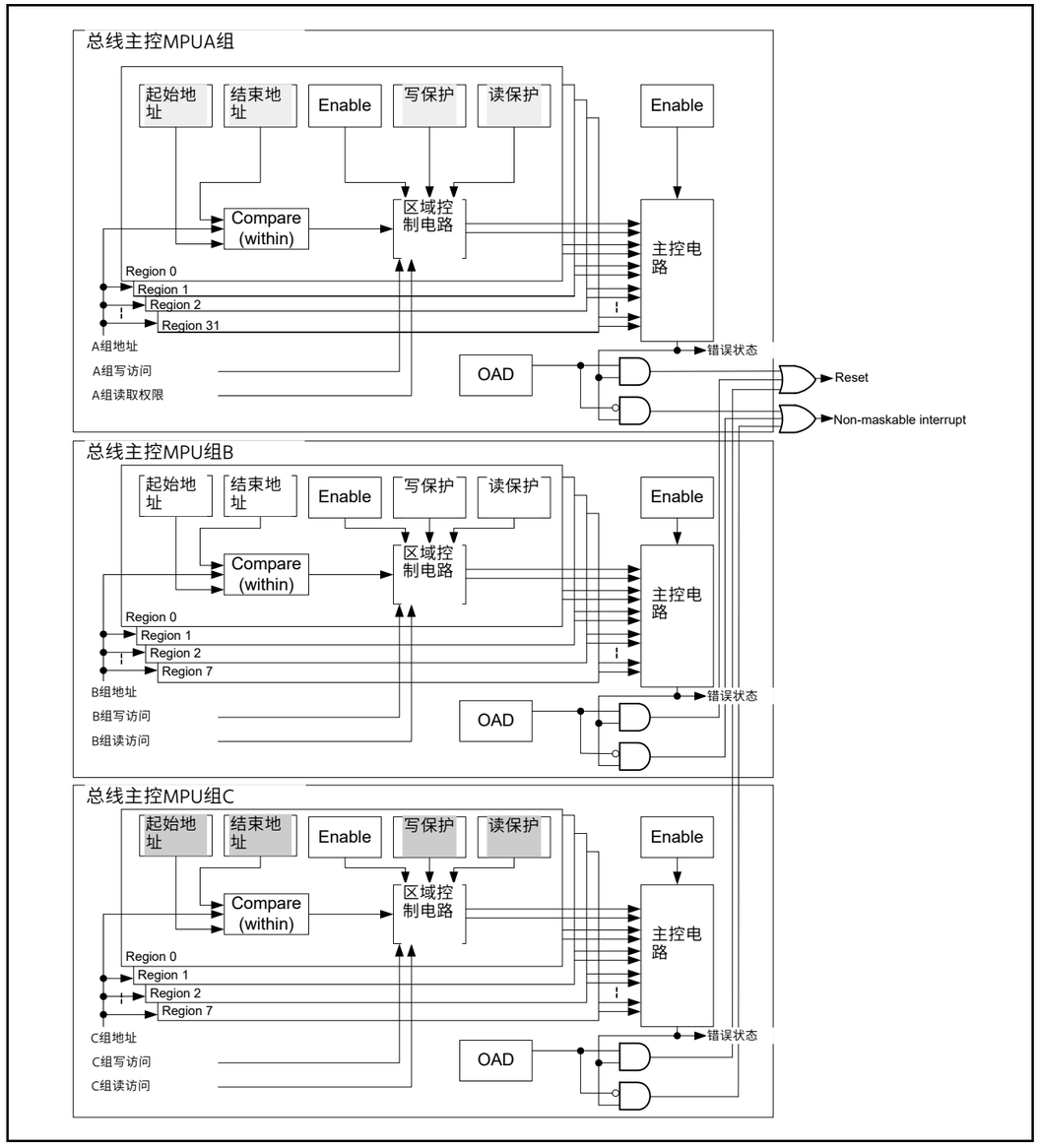


Figure 16.4 总线主控MPU组A、B和C

16.4.1 注册说明

Note: 在写入MPU寄存器之前必须停止总线访问。

16.4.1.1 Group m Region n Start Address Register (MMPUSmn) (m = A to C; n = 0 to 31)

Address(es): MMPU.MMPUSA0 4000 0204h, MMPU.MMPUSA1 4000 0214h, MMPU.MMPUSA2 4000 0224h, MMPU.MMPUSA3 4000 0234h, MMPU.MMPUSA4 4000 0244h, MMPU.MMPUSA5 4000 0254h, MMPU.MMPUSA6 4000 0264h, MMPU.MMPUSA7 4000 0274h, MMPU.MMPUSA8 4000 0284h, MMPU.MMPUSA9 4000 0294h, MMPU.MMPUSA10 4000 02A4h, MMPU.MMPUSA11 4000 02B4h, MMPU.MMPUSA12 4000 02C4h, MMPU.MMPUSA13 4000 02D4h, MMPU.MMPUSA14 4000 02E4h, MMPU.MMPUSA15 4000 02F4h, MMPU.MMPUSA16 4000 0304h, MMPU.MMPUSA17 4000 0314h, MMPU.MMPUSA18 4000 0324h, MMPU.MMPUSA19 4000 0334h, MMPU.MMPUSA20 4000 0344h, MMPU.MMPUSA21 4000 0354h, MMPU.MMPUSA22 4000 0364h, MMPU.MMPUSA23 4000 0374h, MMPU.MMPUSA24 4000 0384h, MMPU.MMPUSA25 4000 0394h, MMPU.MMPUSA26 4000 03A4h, MMPU.MMPUSA27 4000 03B4h, MMPU.MMPUSA28 4000 03C4h, MMPU.MMPUSA29 4000 03D4h, MMPU.MMPUSA30 4000 03E4h, MMPU.MMPUSA31 4000 03F4h, MMPU.MMPUSB0 4000 0604h, MMPU.MMPUSB1 4000 0614h, MMPU.MMPUSB2 4000 0624h, MMPU.MMPUSB3 4000 0634h, MMPU.MMPUSB4 4000 0644h, MMPU.MMPUSB5 4000 0654h, MMPU.MMPUSB6 4000 0664h, MMPU.MMPUSB7 4000 0674h, MMPU.MMPUSC0 4000 0A04h, MMPU.MMPUSC1 4000 0A14h, MMPU.MMPUSC2 4000 0A24h, MMPU.MMPUSC3 4000 0A34h, MMPU.MMPUSC4 4000 0A44h, MMPU.MMPUSC5 4000 0A54h, MMPU.MMPUSC6 4000 0A64h, MMPU.MMPUSC7 4000 0A74h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	MMPUSm[31:16](m = A to C)															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MMPUSm[15:0](m = A to C)															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0	0

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b31 to b0	MMPUSmn[31:0](m = A to C)	Region Start Address	Address where the region starts, for use in region determination. The lower 2 bits to 00b.	R/W

16.4.1.2 Group m Region n End Address Register (MMPUEmn) (m = A to C; n = 0 to 31)

Address(es): MMPU.MMPUEA0 4000 0208h, MMPU.MMPUEA1 4000 0218h, MMPU.MMPUEA2 4000 0228h, MMPU.MMPUEA3 4000 0238h, MMPU.MMPUEA4 4000 0248h, MMPU.MMPUEA5 4000 0258h, MMPU.MMPUEA6 4000 0268h, MMPU.MMPUEA7 4000 0278h, MMPU.MMPUEA8 4000 0288h, MMPU.MMPUEA9 4000 0298h, MMPU.MMPUEA10 4000 02A8h, MMPU.MMPUEA11 4000 02B8h, MMPU.MMPUEA12 4000 02C8h, MMPU.MMPUEA13 4000 02D8h, MMPU.MMPUEA14 4000 02E8h, MMPU.MMPUEA15 4000 02F8h, MMPU.MMPUEA16 4000 0308h, MMPU.MMPUEA17 4000 0318h, MMPU.MMPUEA18 4000 0328h, MMPU.MMPUEA19 4000 0338h, MMPU.MMPUEA20 4000 0348h, MMPU.MMPUEA21 4000 0358h, MMPU.MMPUEA22 4000 0368h, MMPU.MMPUEA23 4000 0378h, MMPU.MMPUEA24 4000 0388h, MMPU.MMPUEA25 4000 0398h, MMPU.MMPUEA26 4000 03A8h, MMPU.MMPUEA27 4000 03B8h, MMPU.MMPUEA28 4000 03C8h, MMPU.MMPUEA29 4000 03D8h, MMPU.MMPUEA30 4000 03E8h, MMPU.MMPUEA31 4000 03F8h, MMPU.MMPUEB0 4000 0608h, MMPU.MMPUEB1 4000 0618h, MMPU.MMPUEB2 4000 0628h, MMPU.MMPUEB3 4000 0638h, MMPU.MMPUEB4 4000 0648h, MMPU.MMPUEB5 4000 0658h, MMPU.MMPUEB6 4000 0668h, MMPU.MMPUEB7 4000 0678h, MMPU.MMPUEC0 4000 0A08h, MMPU.MMPUEC1 4000 0A18h, MMPU.MMPUEC2 4000 0A28h, MMPU.MMPUEC3 4000 0A38h, MMPU.MMPUEC4 4000 0A48h, MMPU.MMPUEC5 4000 0A58h, MMPU.MMPUEC6 4000 0A68h, MMPU.MMPUEC7 4000 0A78h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	MMPUEm[31:16](m = A to C)															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MMPUEm[15:0](m = A to C)															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	1	1

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b31 to b0	MMPUEm[31:0](m = A to C)	Region End Address	Address where the region ends, for use in region determination. The lower 2 bits should be 1.	R/W

16.4.1.1 组m区域n起始地址寄存器(MMPUSmn)（m=A到C；n=0到31）

Address(es): MMPU.MMPUSA0 4000 0204h, MMPU.MMPUSA1 4000 0214h, MMPU.MMPUSA2 4000 0224h, MMPU.MMPUSA3 4000 0234h, MMPU.MMPUSA4 4000 0244h, MMPU.MMPUSA5 4000 0254h, MMPU.MMPUSA6 4000 0264h, MMPU.MMPUSA7 4000 0274h, MMPU.MMPUSA8 4000 0284h, MMPU.MMPUSA9 4000 0294h, MMPU.MMPUSA10 4000 02A4h, MMPU.MMPUSA11 4000 02B4h, MMPU.MMPUSA12 4000 02C4h, MMPU.MMPUSA13 4000 02D4h, MMPU.MMPUSA14 4000 02E4h, MMPU.MMPUSA15 4000 02F4h, MMPU.MMPUSA16 4000 0304h, MMPU.MMPUSA17 4000 0314h, MMPU.MMPUSA18 4000 0324h, MMPU.MMPUSA19 4000 0334h, MMPU.MMPUSA20 4000 0344h, MMPU.MMPUSA21 4000 0354h, MMPU.MMPUSA22 4000 0364h, MMPU.MMPUSA23 4000 0374h, MMPU.MMPUSA24 4000 0384h, MMPU.MMPUSA25 4000 0394h, MMPU.MMPUSA26 4000 03A4h, MMPU.MMPUSA27 4000 03B4h, MMPU.MMPUSA28 4000 03C4h, MMPU.MMPUSA29 4000 03D4h, MMPU.MMPUSA30 4000 03E4h, MMPU.MMPUSA31 4000 03F4h, MMPU.MMPUSB0 4000 0604h, MMPU.MMPUSB1 4000 0614h, MMPU.MMPUSB2 4000 0624h, MMPU.MMPUSB3 4000 0634h, MMPU.MMPUSB4 4000 0644h, MMPU.MMPUSB5 4000 0654h, MMPU.MMPUSB6 4000 0664h, MMPU.MMPUSB7 4000 0674h, MMPU.MMPUSC0 4000 0A04h, MMPU.MMPUSC1 4000 0A14h, MMPU.MMPUSC2 4000 0A24h, MMPU.MMPUSC3 4000 0A34h, MMPU.MMPUSC4 4000 0A44h, MMPU.MMPUSC5 4000 0A54h, MMPU.MMPUSC6 4000 0A64h, MMPU.MMPUSC7 4000 0A74h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	MMPUSm[31:16](m = A to C)															
重置后的值:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MMPUSm[15:0](m = A to C)															
重置后的值:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0	0

x: Undefined

Bit	Symbol	位名称	Description	R/W
b31 to b0	MMPUSmn[31:0](m = A to C)	区域起始地址	区域开始的地址，用于区域确定。低2位为00b。	R/W

16.4.1.2 第m组区域n结束地址寄存器(MMPUEmn)（m=A到C；n=0到31）

Address(es): MMPU.MMPUEA0 4000 0208h, MMPU.MMPUEA1 4000 0218h, MMPU.MMPUEA2 4000 0228h, MMPU.MMPUEA3 4000 0238h, MMPU.MMPUEA4 4000 0248h, MMPU.MMPUEA5 4000 0258h, MMPU.MMPUEA6 4000 0268h, MMPU.MMPUEA7 4000 0278h, MMPU.MMPUEA8 4000 0288h, MMPU.MMPUEA9 4000 0298h, MMPU.MMPUEA10 4000 02A8h, MMPU.MMPUEA11 4000 02B8h, MMPU.MMPUEA12 4000 02C8h, MMPU.MMPUEA13 4000 02D8h, MMPU.MMPUEA14 4000 02E8h, MMPU.MMPUEA15 4000 02F8h, MMPU.MMPUEA16 4000 0308h, MMPU.MMPUEA17 4000 0318h, MMPU.MMPUEA18 4000 0328h, MMPU.MMPUEA19 4000 0338h, MMPU.MMPUEA20 4000 0348h, MMPU.MMPUEA21 4000 0358h, MMPU.MMPUEA22 4000 0368h, MMPU.MMPUEA23 4000 0378h, MMPU.MMPUEA24 4000 0388h, MMPU.MMPUEA25 4000 0398h, MMPU.MMPUEA26 4000 03A8h, MMPU.MMPUEA27 4000 03B8h, MMPU.MMPUEA28 4000 03C8h, MMPU.MMPUEA29 4000 03D8h, MMPU.MMPUEA30 4000 03E8h, MMPU.MMPUEA31 4000 03F8h, MMPU.MMPUEB0 4000 0608h, MMPU.MMPUEB1 4000 0618h, MMPU.MMPUEB2 4000 0628h, MMPU.MMPUEB3 4000 0638h, MMPU.MMPUEB4 4000 0648h, MMPU.MMPUEB5 4000 0658h, MMPU.MMPUEB6 4000 0668h, MMPU.MMPUEB7 4000 0678h, MMPU.MMPUEC0 4000 0A08h, MMPU.MMPUEC1 4000 0A18h, MMPU.MMPUEC2 4000 0A28h, MMPU.MMPUEC3 4000 0A38h, MMPU.MMPUEC4 4000 0A48h, MMPU.MMPUEC5 4000 0A58h, MMPU.MMPUEC6 4000 0A68h, MMPU.MMPUEC7 4000 0A78h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	MMPUEm[31:16](m = A to C)															
重置后的值:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MMPUEm[15:0](m = A to C)															
重置后的值:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	1	1

x: Undefined

Bit	Symbol	位名称	Description	R/W
b31 to b0	MMPUEm[31:0](m = A to C)	区域结束地址	区域结束的地址，用于区域确定。低2位应为1。	R/W

16.4.1.3 Group m Region n Access Control Register (MMPUACmn) (m = A to C; n = 0 to 31)

Address(es): MMPU.MMPUACA0 4000 0200h, MMPU.MMPUACA1 4000 0210h, MMPU.MMPUACA2 4000 0220h, MMPU.MMPUACA3 4000 0230h, MMPU.MMPUACA4 4000 0240h, MMPU.MMPUACA5 4000 0250h, MMPU.MMPUACA6 4000 0260h, MMPU.MMPUACA7 4000 0270h, MMPU.MMPUACA8 4000 0280h, MMPU.MMPUACA9 4000 0290h, MMPU.MMPUACA10 4000 02A0h, MMPU.MMPUACA11 4000 02B0h, MMPU.MMPUACA12 4000 02C0h, MMPU.MMPUACA13 4000 02D0h, MMPU.MMPUACA14 4000 02E0h, MMPU.MMPUACA15 4000 02F0h, MMPU.MMPUACA16 4000 0300h, MMPU.MMPUACA17 4000 0310h, MMPU.MMPUACA18 4000 0320h, MMPU.MMPUACA19 4000 0330h, MMPU.MMPUACA20 4000 0340h, MMPU.MMPUACA21 4000 0350h, MMPU.MMPUACA22 4000 0360h, MMPU.MMPUACA23 4000 0370h, MMPU.MMPUACA24 4000 0380h, MMPU.MMPUACA25 4000 0390h, MMPU.MMPUACA26 4000 03A0h, MMPU.MMPUACA27 4000 03B0h, MMPU.MMPUACA28 4000 03C0h, MMPU.MMPUACA29 4000 03D0h, MMPU.MMPUACA30 4000 03E0h, MMPU.MMPUACA31 4000 03F0h, MMPU.MMPUACB0 4000 0600h, MMPU.MMPUACB1 4000 0610h, MMPU.MMPUACB2 4000 0620h, MMPU.MMPUACB3 4000 0630h, MMPU.MMPUACB4 4000 0640h, MMPU.MMPUACB5 4000 0650h, MMPU.MMPUACB6 4000 0660h, MMPU.MMPUACB7 4000 0670h, MMPU.MMPUACC0 4000 0A00h, MMPU.MMPUACC1 4000 0A10h, MMPU.MMPUACC2 4000 0A20h, MMPU.MMPUACC3 4000 0A30h, MMPU.MMPUACC4 4000 0A40h, MMPU.MMPUACC5 4000 0A50h, MMPU.MMPUACC6 4000 0A60h, MMPU.MMPUACC7 4000 0A70h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	WP	RP	ENABLE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	ENABLE	Region Enable	0: Group m region n unit disabled 1: Group m region n unit enabled.	R/W
b1	RP	Read Protection	0: Read access permitted 1: Read access protected.	R/W
b2	WP	Write Protection	0: Write access permitted 1: Write access protected.	R/W
b15 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Individually configurable ENABLE, RP, and WP bits are provided for each group m region n unit.

ENABLE bit (Region Enable)

The ENABLE bit enables or disables the group m region n unit. When the ENABLE bit is set to 1, the RP and WP bits can be set to permit or protect access to the region that is set in MMPUSmn and MMPUEmn. When the ENABLE bit is set to 0, no region is specified for group m region n access.

RP bit (Read Protection)

The RP bit enables or disables read protection for group m region n. The RP bit is available when the ENABLE bit is set to 1.

WP bit (Write Protection)

The WP bit enables or disables write protection for group m region n. The WP bit is available when the ENABLE bit is set to 1.

Table 16.5 Function of region control circuit (1 of 2)

MMPUACmn.ENABLE*1	MMPUACmn.RP*1	MMPUACmn.WP*1	Access	Region	Output of group m region n unit*1
0	—	—	Read	—	Outside of region
			Write	—	Outside of region

16.4.1.3 第m组区域n访问控制寄存器(MMPUACmn)（m=A到C；n=0到31）

Address(es): MMPU.MMPUACA0 4000 0200h, MMPU.MMPUACA1 4000 0210h, MMPU.MMPUACA2 4000 0220h, MMPU.MMPUACA3 4000 0230h, MMPU.MMPUACA4 4000 0240h, MMPU.MMPUACA5 4000 0250h, MMPU.MMPUACA6 4000 0260h, MMPU.MMPUACA7 4000 0270h, MMPU.MMPUACA8 4000 0280h, MMPU.MMPUACA9 4000 0290h, MMPU.MMPUACA10 4000 02A0h, MMPU.MMPUACA11 4000 02B0h, MMPU.MMPUACA12 4000 02C0h, MMPU.MMPUACA13 4000 02D0h, MMPU.MMPUACA14 4000 02E0h, MMPU.MMPUACA15 4000 02F0h, MMPU.MMPUACA16 4000 0300h, MMPU.MMPUACA17 4000 0310h, MMPU.MMPUACA18 4000 0320h, MMPU.MMPUACA19 4000 0330h, MMPU.MMPUACA20 4000 0340h, MMPU.MMPUACA21 4000 0350h, MMPU.MMPUACA22 4000 0360h, MMPU.MMPUACA23 4000 0370h, MMPU.MMPUACA24 4000 0380h, MMPU.MMPUACA25 4000 0390h, MMPU.MMPUACA26 4000 03A0h, MMPU.MMPUACA27 4000 03B0h, MMPU.MMPUACA28 4000 03C0h, MMPU.MMPUACA29 4000 03D0h, MMPU.MMPUACA30 4000 03E0h, MMPU.MMPUACA31 4000 03F0h, MMPU.MMPUACB0 4000 0600h, MMPU.MMPUACB1 4000 0610h, MMPU.MMPUACB2 4000 0620h, MMPU.MMPUACB3 4000 0630h, MMPU.MMPUACB4 4000 0640h, MMPU.MMPUACB5 4000 0650h, MMPU.MMPUACB6 4000 0660h, MMPU.MMPUACB7 4000 0670h, MMPU.MMPUACC0 4000 0A00h, MMPU.MMPUACC1 4000 0A10h, MMPU.MMPUACC2 4000 0A20h, MMPU.MMPUACC3 4000 0A30h, MMPU.MMPUACC4 4000 0A40h, MMPU.MMPUACC5 4000 0A50h, MMPU.MMPUACC6 4000 0A60h, MMPU.MMPUACC7 4000 0A70h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	WP	RP	ENABLE
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	ENABLE	区域启用	0：组m区域n单元禁用1：组m区域n单元启用。	R/W
b1	RP	读保护	0：允许读访问1：读访问受保护。	R/W
b2	WP	写保护	0：允许写访问1：写访问受保护。	R/W
b15 to b3	—	Reserved	这些位被读取为0。写入值应为0。	R/W

为每个组m区域n单元提供可单独配置的ENABLE、RP和WP位。

ENABLE位（区域启用）

ENABLE位启用或禁用组m区域n单元。当ENABLE位设置为1时，可以设置RP和WP位以允许或保护对MMPUSmn和MMPUEmn中设置的区域的访问。当ENABLE位设置为0时，没有为组m区域n访问指定区域。

RP位（读保护）

RP位启用或禁用组m区域n的读保护。当ENABLE位设置为1时，RP位可用。

WP位（写保护）

WP位启用或禁用组m区域n的写保护。当ENABLE位设置为1时，WP位可用。

Table 16.5 区域控制电路的功能(1of2)

MMPUACmn.ENABLE*1	MMPUACmn.RP*1	MMPUACmn.WP*1	Access	Region	组m区域n单元的输出*1
0	—	—	Read	—	区域外
			Write	—	区域外

Table 16.5 Function of region control circuit (2 of 2)

MMPUACmn.ENABLE*1	MMPUACmn.RP*1	MMPUACmn.WP*1	Access	Region	Output of group m region n unit*1
1	0	0	Read	Inside	Permitted region
				Outside	Outside of region
			Write	Inside	Permitted region
				Outside	Outside of region
	0	1	Read	Inside	Permitted region
				Outside	Outside of region
			Write	Inside	Protected region
				Outside	Outside of region
	1	0	Read	Inside	Protected region
				Outside	Outside of region
			Write	Inside	Permitted region
				Outside	Outside of region
	1	1	Read	Inside	Protected region
				Outside	Outside of region
			Write	Inside	Protected region
				Outside	Outside of region

Note 1. m = A to C,
In the case of m = A: n = 0 to 31
In the case of m = B or C: n = 0 to 7.

Table 16.6 Function of master control circuit

MMPUCTLm.ENABLE*1	Output of group m region 0 unit*1	Output of group m region 1 unit*1	Output of group A Region 2 to 31 unit, Output of group B or C Region 2 to 7 unit	Function of group m*1
1	Protected region	Don't care	Don't care	Generate error
1	Don't care	Protected region	Don't care	Generate error
1	Don't care	Don't care	Protected region	Generate error
1	Outside of region	Outside of region	Outside of region	Generate error
Other case				No error

Note 1. m = A to C.

A master MPU error occurs on the following conditions:

- MMPUCTLm.ENABLE = 1, and output of one or more region n units is to a protected region
- MMPUCTLm.ENABLE = 1, and output of all region n units is outside of region.

Other cases are handled as permitted regions.

16.4.1.4 Bus Master MPU Control Register (MMPUCTLm) (m = A to C)

Address(es): MMPU.MMPUCTLA 4000 0000h, MMPU.MMPUCTLB 4000 0400h, MMPU.MMPUCTLC 4000 0800h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	KEY[7:0]								—	—	—	—	—	—	OAD	ENABLE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	ENABLE	Master Group Enable	0: Master group m disabled 1: Master group m enabled.	R/W

Table 16.5 区域控制电路的功能(2of2)

MMPUACmn.ENABLE*1	MMPUACmn.RP*1	MMPUACmn.WP*1	Access	Region	组m区域n单元的输出*1
1	0	0	Read	Inside	许可区域
				Outside	区域外
			Write	Inside	许可区域
				Outside	区域外
	0	1	Read	Inside	许可区域
				Outside	区域外
			Write	Inside	保护区
				Outside	区域外
	1	0	Read	Inside	保护区
				Outside	区域外
			Write	Inside	许可区域
				Outside	区域外
	1	1	Read	Inside	保护区
				Outside	区域外
			Write	Inside	保护区
				Outside	区域外

注1.m=A到C，
在m=A的情况下：n=0到31
在m=B或C的情况下：n=0到7。

Table 16.6 主控电路功能

MMPUCTLm.ENABLE*1	组m区域0单元的输出*1	第m组区域1单元的输出*1	A组区域2到31单元的输出， B组或C组的输出区域2至7单元	m*1组的功能
1	保护区	Don't care	Don't care	产生错误
1	Don't care	保护区	Don't care	产生错误
1	Don't care	Don't care	保护区	产生错误
1	区域外	区域外	区域外	产生错误
其他情况				没有错误

注1.m=A到C。

主控MPU错误发生在以下情况：

- MMPUCTLm.ENABLE=1，一个或多个区域n个单元的输出到受保护区域
- MMPUCTLm.ENABLE=1，所有区域n个单元的输出都在区域之外。

其他情况按许可区域处理。

16.4.1.4 总线主控MPU控制寄存器(MMPUCTLm)(m=AtoC)

Address(es): MMPU.MMPUCTLA 4000 0000h, MMPU.MMPUCTLB 4000 0400h, MMPU.MMPUCTLC 4000 0800h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	KEY[7:0]								—	—	—	—	—	—	OAD	ENABLE
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	ENABLE	主组启用	0：主组m禁用1：主组m启用。	R/W

Bit	Symbol	Bit name	Description	R/W
b1	OAD	Operation After Detection	0: Non-maskable interrupt 1: Reset.	R/W
b7 to b2	—	Reserved	These bits are read as 0.The write value should be 0.	R/W
b15 to b8	KEY[7:0]	Key Code	These bits enable or disable writes to the OAD and ENABLE bits.	R/(W)*1

Note 1. Write data is not saved.

ENABLE bit (Master Group Enable)

The ENABLE bit enables or disables the bus master MPU function for each master group. When this bit is set to 1, MMPUACmn is available. When this bit is set to 0, MMPUACmn is unavailable, including permission for all regions. The bus master MPU function of each master group uses the ENABLE bit. When writing to the ENABLE bit, write A5h to the KEY[7:0] bits simultaneously using halfword access.

OAD bit (Operation After Detection)

The OAD bit selects either a reset or a non-maskable interrupt to occur when access to the protected region is detected by the bus master MPU. The bus master MPU function for each master group uses its OAD bit independently. When writing to the OAD bit, write A5h to the KEY[7:0] bits simultaneously using halfword access.

KEY[7:0] bits (Key Code)

The KEY[7:0] bits enable or disable writes to the ENABLE and OAD bits. When writing to the ENABLE and OAD bits, write A5h to the KEY[7:0] bits simultaneously. When other values are written, the ENABLE and OAD bits are not updated. The KEY[7:0] bits are always read as 00h.

16.4.1.5 Group m Protection of Register (MMPUPTm) (m = A to C)

Address(es): MMPU.MMPUPTA 4000 0102h, MMPU.MMPUPTB 4000 0502h, MMPU.MMPUPTC 4000 0902h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	KEY[7:0]								—	—	—	—	—	—	—	PROTECT
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	PROTECT	Protection of register	0: All bus master MPU group m register writes are permitted 1: All bus master MPU group m register writes are protected. Read is permitted.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15 to b8	KEY[7:0]	Key Code	These bits enable or disable writes to the PROTECT bit.	R/(W)*1

Note 1. Write data is not saved.

PROTECT bit (Protection of register)

The PROTECT bit enables or disables writes to the associated registers to be protected. MMPUTm.PROTECT controls the following bus master MPU group m protection registers:

- MMPUSmn
- MMPUEmn
- MMPUACmn
- MMPUCTLm.

When writing to the PROTECT bit, write A5h to the KEY[7:0] bits simultaneously using halfword access.

Bit	Symbol	位名称	Description	R/W
b1	OAD	检测后的操作	0：不可屏蔽中断1：复位 。	R/W
b7 to b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b15 to b8	KEY[7:0]	关键代码	这些位启用或禁用对OAD的写入和启用位。	R/(W)*1

注1.写入数据不保存。

ENABLE位（主组启用）

ENABLE位启用或禁用每个主机组的总线主机MPU功能。当该位设置为1时，MMPUACmn可用。当该位设置为0时，MMPUACmn不可用，包括所有区域的权限。每个主机组的总线主机MPU功能使用ENABLE位。写入ENABLE位时，使用半字访问同时将A5h写入KEY[7:0]位。

OAD位（检测后操作）

当总线主控MPU检测到对受保护区域的访问时，OAD位选择发生复位或不可屏蔽中断。每个主控组的总线主控MPU功能独立使用其OAD位。写入OAD位时，使用半字访问同时将A5h写入KEY[7:0]位。

KEY[7:0]位（键码）

KEY[7:0]位启用或禁用对ENABLE和OAD位的写入。写入ENABLE和OAD位时，同时将A5h写入KEY[7:0]位。写入其他值时，ENABLE和OAD位不会更新。KEY[7:0]位总是读为00h。

16.4.1.5 组m寄存器保护(MMPUPTm)(m=A到C)

Address(es): MMPU.MMPUPTA 4000 0102h, MMPU.MMPUPTB 4000 0502h, MMPU.MMPUPTC 4000 0902h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	KEY[7:0]								—	—	—	—	—	—	—	PROTECT
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	PROTECT	注册保护	0：允许所有总线主控MPU组m寄存器写入1：所有总线主控MPU组m寄存器写入受到保护。允许读取 。	R/W
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b15 to b8	KEY[7:0]	关键代码	这些位启用或禁用对PROTECT位的写入。	R/(W)*1

注1.写入数据不保存。

PROTECT位（保护寄存器）

PROTECT位启用或禁用对要保护的相关寄存器的写入。MMPUTm.PROTECT控制以下总线主控MPU组m保护寄存器：

- MMPUSmn
- MMPUEmn
- MMPUACmn
- MMPUCTLm.

写入PROTECT位时，使用半字访问同时将A5h写入KEY[7:0]位。

KEY[7:0] bits (Key Code)

The KEY[7:0] bits enable or disable writing to the PROTECT bit. When writing to the PROTECT bit, write A5h simultaneously to the KEY[7:0] bits. When other values are written, the PROTECT bit is not updated. The KEY[7:0] bits are always read as 00h.

16.4.2 Operation

16.4.2.1 Memory protection

The bus master MPU monitors memory access using control settings made individually for the access control regions. If access to a protected region is detected, the bus master MPU generates a memory protection error.

The bus master MPU can be configured for up to 32 protection regions. Protected regions include those with overlapping permitted and protected regions, and those with two overlapping permitted regions.

The bus master MPU provides three groups: A, B, and C. The memory protection function checks the address of the bus for a unified master group, and all accesses by a master group are protected. The bus master MPU sets the permission for all of the regions after reset. Setting MMPUCTLm.ENABLE to 1 protects all of the regions. A permitted region is set up within the protected region for each region. If access to a protected region is detected, the bus master MPU generates an error.

Figure 16.5 shows the use case of a bus master MPU.

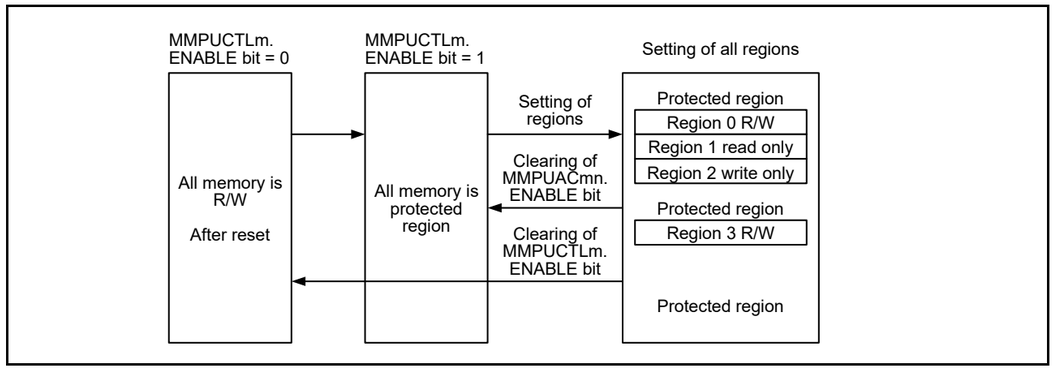


Figure 16.5 Use case of bus master MPU

Figure 16.6 shows the access permission or protection for overlapping bus master MPU regions. Access control for overlapping regions is as follows:

- The region is handled as protected when output of one or more region units is a protected region
- The region is handled as protected when output of all region units is outside of the regions
- Other cases are handled as permitted regions.

KEY[7:0]位（键码）

KEY[7:0]位启用或禁用对PROTECT位的写入。写入PROTECT位时，同时将A5h写入KEY[7:0]位。写入其他值时，PROTECT位不会更新。KEY[7:0]位总是读为00h。

16.4.2 Operation

16.4.2.1 内存保护

总线主控MPU使用为访问控制区域单独进行的控制设置来监视内存访问。如果检测到对受保护区域的访问，则总线主控MPU会产生内存保护错误。

总线主控MPU最多可配置32个保护区域。保护区包括允许区域和保护区域重叠的区域，以及两个允许区域重叠的区域。

总线主控MPU提供三组：A、B、C。内存保护功能检查总线地址为一个统一的主控组，一个主控组的所有访问都受到保护。总线主控MPU在复位后设置所有区域的权限。将MMPUCTLm.ENABLE设置为1可保护所有区域。在保护区域内为每个区域设置一个允许区域。如果检测到对受保护区域的访问，则总线主控MPU会产生错误。

图16.5显示了总线主控MPU的用例。

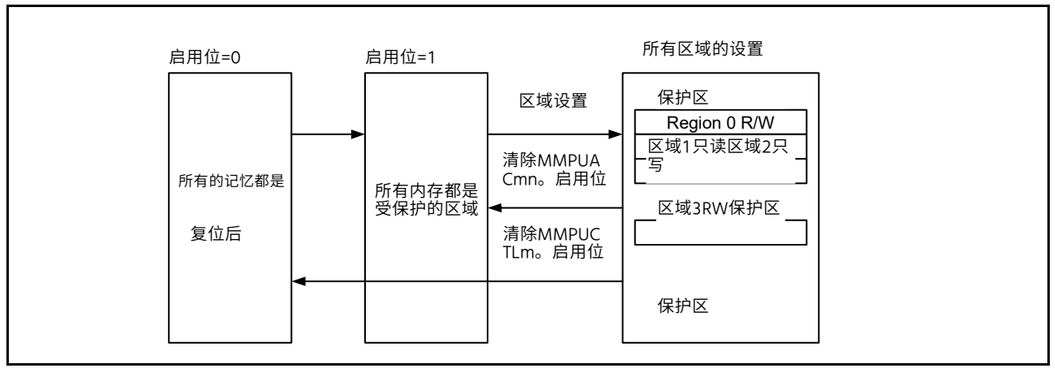


Figure 16.5 总线主控MPU用例

图16.6显示了重叠总线主控MPU区域的访问许可或保护。重叠区域的访问控制如下：

- 当一个或多个区域单元的输出是受保护区域时，该区域被视为受保护区域
- 当所有区域单元的输出都在区域之外时，该区域被视为受保护
- 其他情况按许可区域处理。

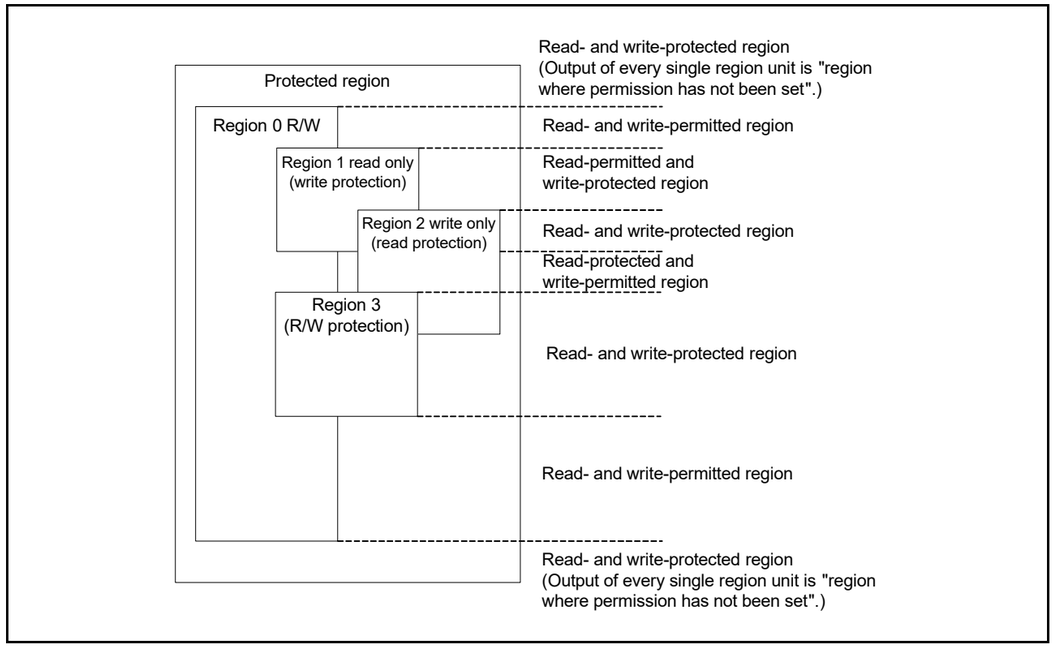


Figure 16.6 Access permission or protection by overlap of the bus master MPU region

Figure 16.7 shows the register setting flow after reset. During this register setting, stop all masters except the CPU.

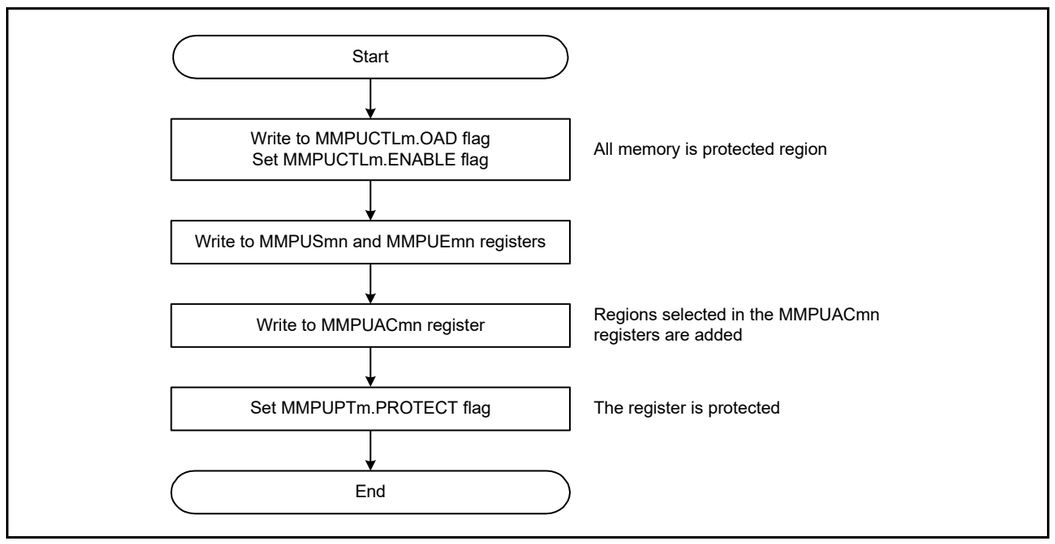


Figure 16.7 Register setting flow after reset

Figure 16.8 shows the register setting flow for adding regions. During this register setting, stop all masters except the CPU.

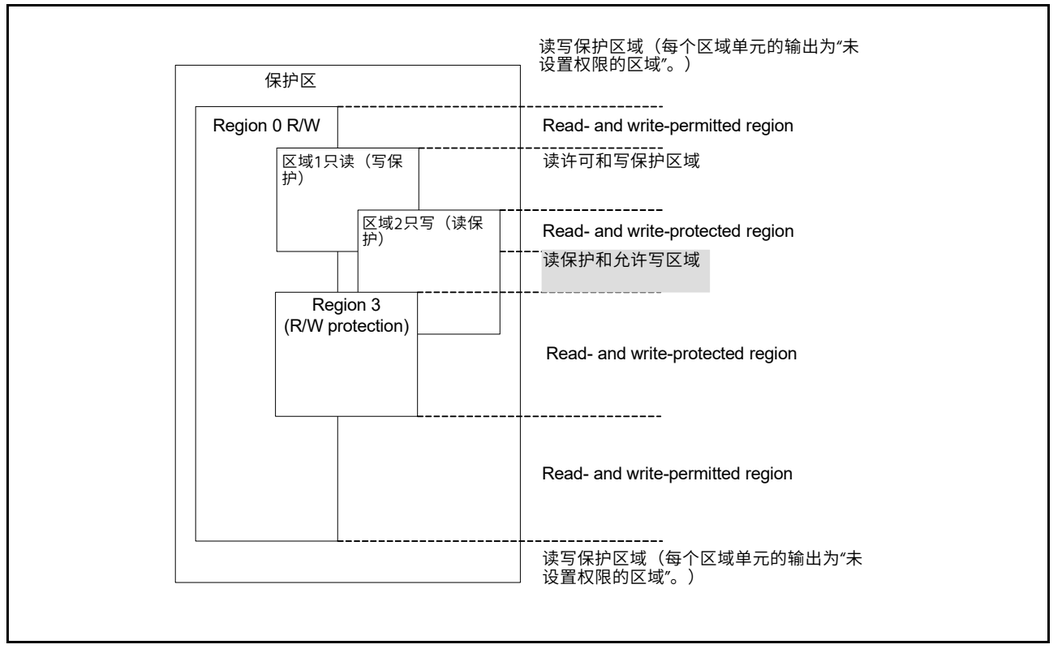


Figure 16.6 通过总线主控MPU区域的重叠访问许可或保护

图16.7显示了复位后的寄存器设置流程。在此寄存器设置期间，停止除CPU之外的所有主机。

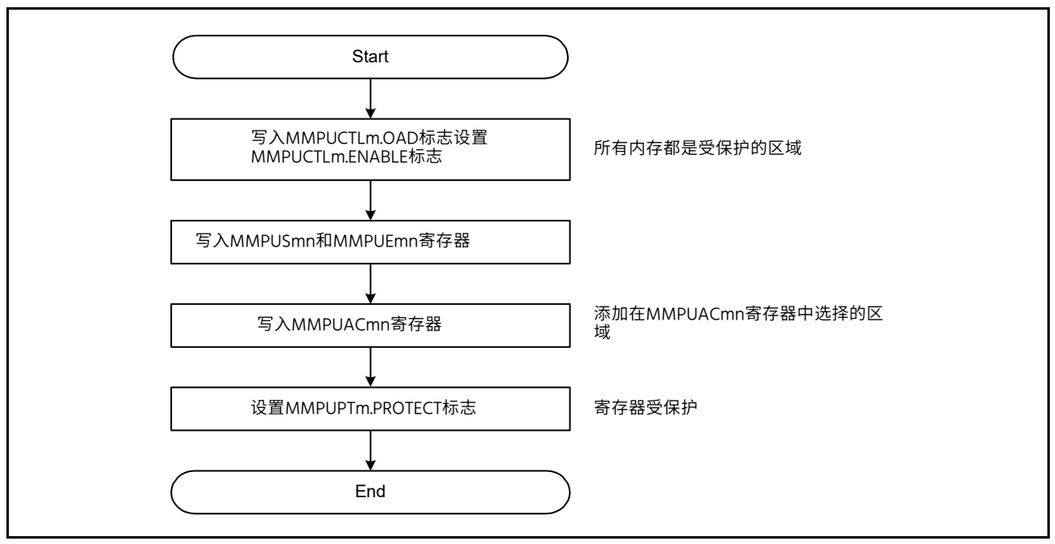


Figure 16.7 复位后的寄存器设置流程

图16.8显示了添加区域的寄存器设置流程。在此寄存器设置期间，停止除CPU.

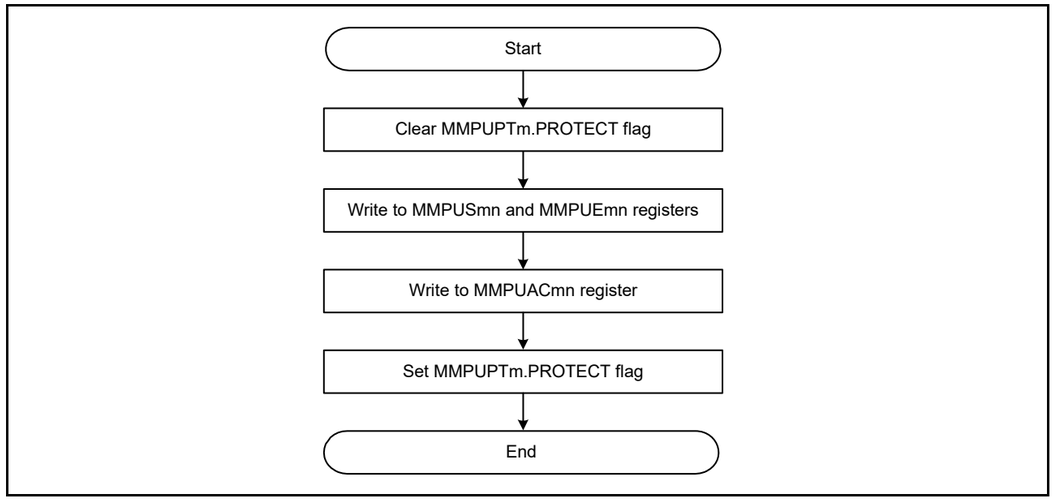


Figure 16.8 Register setting flow for region addition

16.4.2.2 Protecting the registers

To protect registers related to the bus master MPU, set the PROTECT bit in the associated MMPUPTm register.

16.4.2.3 Memory protection error

The bus master MPU generates an error if access to a protected region is detected. Set the OAD bit to select whether the error is reported as a non-maskable interrupt or reset. The non-maskable interrupt or reset is shared between bus master MPU groups A, B, and C. The non-maskable interrupt status is indicated in ICU.NMISR.BUSMST, see section 14, Interrupt Controller Unit (ICU). Reset status is indicated in SYSTEM.RSTSR1.BUSMRF, see section 6, Resets.

16.5 Bus Slave MPU

The bus slave MPU monitors access to the bus slave functions, such as flash or SRAM. The function can be accessed from four bus masters, the CPU, and bus master MPU groups A, B, and C. The bus slave MPU has a separate protection register for each of the four bus masters, with independent access protection control, consisting of read and write permission. If access to a protected region is detected, the bus slave MPU generates a reset or a non-maskable interrupt, and can store the bus error address, bus error status, and error access status. For details, see 15.3.21 and 15.3.22 in section 15, Buses.

Table 16.7 lists the specifications of the bus slave MPU and Figure 16.9 shows a block diagram.

Table 16.7 Bus slave MPU specifications (1 of 2)

Specifications	Description
Protected bus masters	• Bus master MPU group A: DMA bus • Bus master MPU group B: ETHER bus • Bus master MPU group C: GPX bus.
Protected slave functions	• Memory bus 3: Code flash memory, SRAMHS • Internal peripheral bus 9: Flash memory (in P/E), data flash memory, and TSN • Memory bus 4: SRAM0 • Memory bus 5: SRAM1, Standby SRAM • Internal peripheral bus 1: DTC, DMAC, interrupt controller, flash registers, MPU, CSC, SDRAMC, SRAM registers, system controller and bus controller • Internal peripheral bus 3, 4, 5: Other peripherals • Internal peripheral bus 7: Secure IPs (SCE7) • Internal peripheral bus 8: Graphic IPs (JPEG/GLCDC/DRW) • EXBIU: External memory interface (SDRAM, CSC) • EXBIU2: External device interface (QSPI).

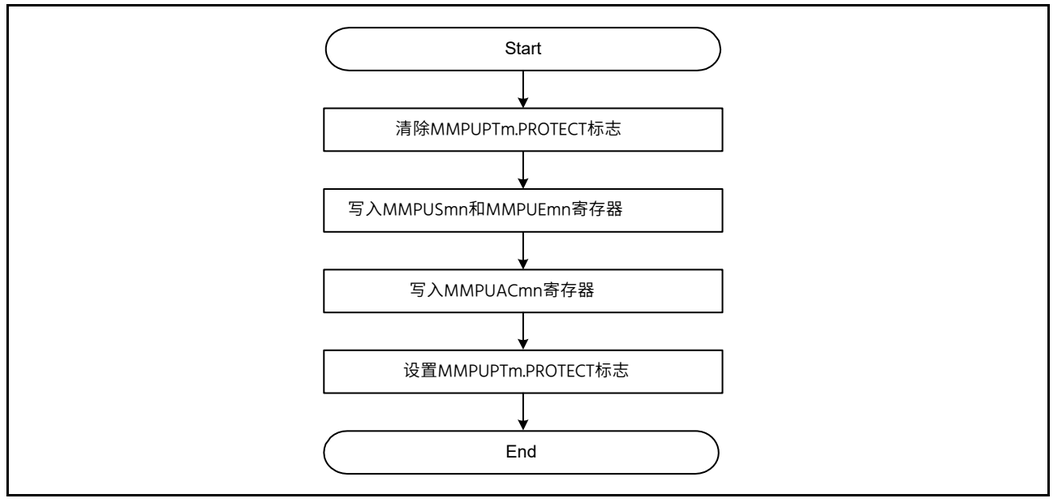


Figure 16.8 区域添加的注册设置流程

16.4.2.2 保护寄存器

要保护与总线主控MPU相关的寄存器，请设置相关MMPUPTm寄存器中的PROTECT位。

16.4.2.3 内存保护错误

如果检测到对受保护区域的访问，则总线主控MPU会产生错误。设置OAD位以选择将错误报告为不可屏蔽中断还是复位。不可屏蔽中断或复位在总线主控MPU组A、B和C之间共享。不可屏蔽中断状态在ICU.NMISR.BUSMST中指示，参见第14节，

中断控制器单元（ICU）。复位状态在SYSTEM.RSTSR1.BUSMRF中指示，参见第6节，复位。

16.5 总线从MPU

总线从机MPU监控对总线从机功能的访问，例如闪存或SRAM。该功能可以从四个总线主控CPU、总线主控MPU组A、B和C访问。总线从属MPU对四个总线主控都有一个单独的保护寄存器，具有独立的访问保护控制，包括读写权限。如果检测到对受保护区域的访问，则总线从MPU产生复位或不可屏蔽中断，并可以存储总线错误地址、总线错误状态和错误访问状态。有关详细信息，请参阅第15节“公共汽车”中的15.3.21和15.3.22。

表16.7列出了总线从MPU的规格，图16.9显示了框图。

Table 16.7 总线从机MPU规格(1of2)

Specifications	Description
受保护的总线主机	总线主控MPU组A：DMA总线 总线主控MPU组B：ETHER总线 总线主控MPU组C：GPX总线。
受保护的从属功能	内存总线3：代码闪存、SRAMHS 内部外围总线9：闪存（在PE中）、数据闪存和TSN 内存总线4：SRAM0 内存总线5：SRAM1、备用SRAM 内部外围总线1：DTC、DMAC、中断控制器、闪存寄存器、MPU、CSC、SDRAMC、SRAM寄存器、系统控制器和总线控制器 内部外围总线3、4、5：其他外围 内部外围总线7：安全IP(SCE7) 内部外围总线8：图形IP(JPEGGLCDCDRW) EXBIU：外部存储器接口（SDRAM、CSC）EXBIU2：外部设备接口(QSPI)。

Table 16.7 Bus slave MPU specifications (2 of 2)

Specifications	Description
Access-control settings for individual regions	Permission to read and write
Operation on error detection	Reset, non-maskable interrupt, or exception
Register protection	Register can be protected from illegal writes

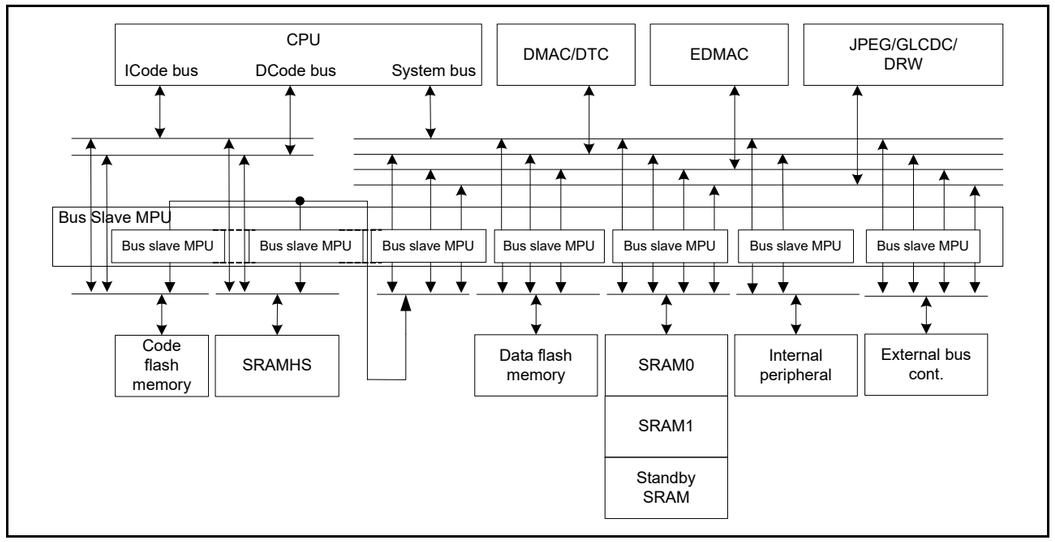


Figure 16.9 Bus slave MPU block diagram

16.5.1 Register Descriptions

Note: Bus access must be stopped before writing to the MPU registers.

16.5.1.1 Access Control Register for Memory Bus 3 (SMPUMBIU)

Address(es): SMPU.SMPUMBIU 4000 0C10h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	WPSRAMHS	RPSRAMHS	WPFLI	RPFLI	—	—	—	—	WPGRPC	RPGRPC	WPGRPB	RPGRPB	WPGRPA	RPGRPA	—	—
Value after reset:	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b2	RPGRPA	Master Group A Read Protection	0: Memory protection for master group A reads disabled 1: Memory protection for master group A reads enabled.	R/W
b3	WPGRPA	Master Group A Write Protection	0: Memory protection for master group A writes disabled 1: Memory protection for master group A writes enabled.	R/W
b4	RPGRPB	Master Group B Read Protection	0: Memory protection for master group B reads disabled 1: Memory protection for master group B reads enabled.	R/W
b5	WPGRPB	Master Group B Write Protection	0: Memory protection for master group B writes disabled 1: Memory protection for master group B writes enabled.	R/W
b6	RPGRPC	Master Group C Read Protection	0: Memory protection for master group C reads disabled 1: Memory protection for master group C reads enabled.	R/W

Table 16.7 总线从MPU规格(2of2)

Specifications	Description
各个区域的访问控制设置	读写权限
错误检测操作	复位、不可屏蔽中断或异常
注册保护	可以保护寄存器免受非法写入

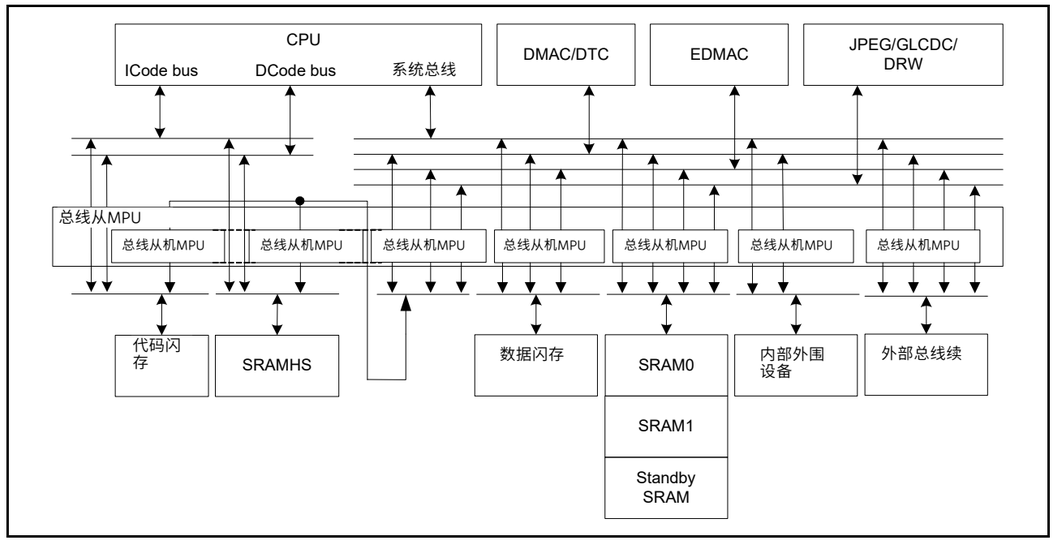


Figure 16.9 总线从机MPU框图

16.5.1 注册说明

Note: 在写入MPU寄存器之前必须停止总线访问。

16.5.1.1 内存总线3的访问控制寄存器(SMPUMBIU)

Address(es): SMPU.SMPUMBIU 4000 0C10h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	WPSRAMHS	RPSRAMHS	WPFLI	RPFLI	—	—	—	—	WPGRPC	RPGRPC	WPGRPB	RPGRPB	WPGRPA	RPGRPA	—	—
重置后的值:	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b1, b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b2	RPGRPA	大师组A读 Protection	0：禁用主组A读取的内存保护1：启用主组A读取的内存保护。	R/W
b3	WPGRPA	大师组A写 Protection	0：禁用主组A写入的内存保护1：启用主组A写入的内存保护。	R/W
b4	RPGRPB	主组B读取 Protection	0：禁用主机组B读取的内存保护1：启用主机组B读取的内存保护。	R/W
b5	WPGRPB	主组B写 Protection	0：禁用主组B写入的内存保护1：启用主组B写入的内存保护。	R/W
b6	RPGRPC	大师组C读 Protection	0：禁用主组C读取的内存保护1：启用主组C读取的内存保护。	R/W

Bit	Symbol	Bit name	Description	R/W
b7	WPGRPC	Master Group C Write Protection	0: Memory protection for master group C writes disabled 1: Memory protection for master group C writes enabled.	R/W
b11 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b12	RPFLI	Code Flash Memory Read Protection	0: Memory protection for code flash memory reads from master group A, B, and C disabled 1: Memory protection for code flash memory reads from master group A, B, and C enabled.	R/W
b13	WPFLI	Code Flash Memory Write Protection	1: Memory protection for code flash memory writes from master group A, B, and C enabled. This bit is read as 1. The write value should be 1.	R/W
b14	RPSRAMHS	SRAMHS Read Protection	0: Memory protection for SRAMHS reads from master group A, B, and C disabled 1: Memory protection for SRAMHS reads from master group A, B, and C enabled.	R/W
b15	WPSRAMHS	SRAMHS Write Protection	0: Memory protection for SRAMHS writes from master group A, B, and C disabled 1: Memory protection for SRAMHS writes from master group A, B, and C enabled.	R/W

The SMPUMBIU register enables memory protection for the specified master and slave for access from master group A, B, or C to code flash memory and SRAMHS.

RPGRPA bit (Master Group A Read Protection)

The RPGRPA bit enables or disables memory protection for reads by master group A on memory bus 3.

WPGRPA bit (Master Group A Write Protection)

The WPGRPA bit enables or disables memory protection for writes by master group A on memory bus 3.

RPGRPB bit (Master Group B Read Protection)

The RPGRPB bit enables or disables memory protection for reads by master group B on memory bus 3.

WPGRPB bit (Master Group B Write Protection)

The WPGRPB bit enables or disables memory protection for writes by master group B on memory bus 3.

RPGRPC bit (Master Group C Read Protection)

The RPGRPC bit enables or disables memory protection for reads by master group C on memory bus 3.

WPGRPC bit (Master Group C Write Protection)

The WPGRPC bit enables or disables memory protection for writes by master group C on memory bus 3.

RPFLI bit (Code Flash Memory Read Protection)

The RPFLI bit enables or disables memory protection for reads by master group A, B, or C on the code flash memory.

WPFLI bit (Code Flash Memory Write Protection)

The WPFLI bit enables memory protection for writes by master group A, B, or C on the code flash memory.

RPSRAMHS bit (SRAMHS Read Protection)

The RPSRAMHS bit enables or disables memory protection for reads by master group A, B, or C on the SRAMHS.

WPSRAMHS bit (SRAMHS Write Protection)

The WPSRAMHS bit enables or disables memory protection for writes by master group A, B, or C on the SRAMHS.

Bit	Symbol	位名称	Description	R/W
b7	WPGRPC	大师组C写 Protection	0：禁用主机组C写入的内存保护1：启用主机组C写入的内存保护。	R/W
b11 to b8	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b12	RPFLI	代码闪存读取 Protection	0：禁用从主机组A、B和C读取代码闪存的内存保护1：启用从主机组A、B和C读取代码闪存的内存保护。	R/W
b13	WPFLI	代码闪存写入 Protection	1：使能主组A、B和C的代码闪存写入的存储器保护。该位读取为1。写入值应为1。	R/W
b14	RPSRAMHS	SRAMHS读保护	0：禁用从主机组A、B和C读取SRAMHS的内存保护1：启用从主机组A、B和C读取SRAMHS的内存保护。	R/W
b15	WPSRAMHS	SRAMHS写保护	0：禁止从主机组A、B和C写入SRAMHS的存储器保护1：启用从主机组A、B和C写入SRAMHS的存储器保护。	R/W

SMPUMBIU寄存器为指定的主机和从机启用内存保护，以便从主机组A访问，B或C对闪存和SRAMHS进行编码。

RRPGRPA位（主组A读保护）

RPGRPA位启用或禁用内存总线3上的主组A读取的内存保护。

WPGRPA位（主组A写保护）

WPGRPA位启用或禁用内存总线3上主机组A写入的内存保护。

RPGRPB位（MasterGroupB读保护）

RPGRPB位启用或禁用内存总线3上主机组B读取的内存保护。

WPGRPB位（主机组B写保护）

WPGRPB位启用或禁用主机组B在内存总线3上写入的内存保护。

RPGRPC位（MasterGroupC读保护）

RPGRPC位启用或禁用内存总线3上的主组C读取的内存保护。

WPGRPC位（主控组C写保护）

WPGRPC位启用或禁用内存总线3上的主组C写入的内存保护。

RPFLI位（代码闪存读保护）

RPFLI位启用或禁用主组A、B或C对代码闪存的读取的存储器保护。

WPFLI位（代码闪存写保护）

WPFLI位为代码闪存上的主机组A、B或C的写入启用存储器保护。

RPSRAMHS位（SRAMHS读保护）

RPSRAMHS位启用或禁用SRAMHS上的主机组A、B或C读取的存储器保护。

WPSRAMHS位（SRAMHS写保护）

WPSRAMHS位启用或禁用主组A、B或C对SRAMHS的写操作的存储器保护。

16.5.1.2 Access Control Register for Internal Peripheral Bus 9 (SMPUFBIU)

Address(es): SMPU.SMPUFBIU 4000 0C14h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	WPGRPC	RPGRPC	WPGRPB	RPGRPB	WPGRPA	RPGRPA	WPCPU	RPCPU
Value after reset:	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	RPCPU	CPU Read Protection	0: Memory protection for CPU reads disabled 1: Memory protection for CPU reads enabled.	R/W
b1	WPCPU	CPU Write Protection	0: Memory protection for CPU writes disabled 1: Memory protection for CPU writes enabled.	R/W
b2	RPGRPA	Master Group A Read Protection	0: Memory protection for master group A reads disabled 1: Memory protection for master group A reads enabled.	R/W
b3	WPGRPA	Master Group A Write Protection	0: Memory protection for master group A writes disabled 1: Memory protection for master group A writes enabled.	R/W
b4	RPGRPB	Master Group B Read Protection	0: Memory protection for master group B reads disabled 1: Memory protection for master group B reads enabled.	R/W
b5	WPGRPB	Master Group B Write Protection	0: Memory protection for master group B writes disabled 1: Memory protection for master group B writes enabled.	R/W
b6	RPGRPC	Master Group C Read Protection	1: Memory protection for master group C reads enabled. This bit is read as 1. The write value should be 1.	R/W
b7	WPGRPC	Master Group C Write Protection	1: Memory protection for master group C writes enabled. This bit is read as 1. The write value should be 1.	R/W
b15 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

RPCPU bit (CPU Read Protection)

The RPCPU bit enables or disables memory protection for reads by the CPU on internal peripheral bus 9.

WPCPU bit (CPU Write Protection)

The WPCPU bit enables or disables memory protection for writes by the CPU on internal peripheral bus 9.

RPGRPA bit (Master Group A Read Protection)

The RPGRPA bit enables or disables memory protection for reads by master group A on internal peripheral bus 9.

WPGRPA bit (Master Group A Write Protection)

The WPGRPA bit enables or disables memory protection for writes by master group A on internal peripheral bus 9.

RPGRPB bit (Master Group B Read Protection)

The RPGRPB bit enables or disables memory protection for reads by master group B on internal peripheral bus 9.

WPGRPB bit (Master Group B Write Protection)

The WPGRPB bit enables or disables memory protection for writes by master group B on internal peripheral bus 9.

RPGRPC bit (Master Group C Read Protection)

The RPGRPC bit enables memory protection for reads by master group C on internal peripheral bus 9. There is no connection between master group C and internal peripheral bus 9. This bit is read as 1, and the write value should be 1.

WPGRPC bit (Master Group C Write Protection)

The WPGRPC bit enables memory protection for writes by master group C on internal peripheral bus 9. There is no connection between master group C and internal peripheral bus 9. This bit is read as 1, and the write value should be 1.

16.5.1.2 内部外围总线9(SMPUFBIU)的访问控制寄存器

Address(es): SMPU.SMPUFBIU 4000 0C14h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	WPGRPC	RPGRPC	WPGRPB	RPGRPB	WPGRPA	RPGRPA	WPCPU	RPCPU
重置后的值：	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	RPCPU	CPU读保护	0：禁用CPU读取的内存保护1：启用CPU读取的内存保护。	R/W
b1	WPCPU	CPU写保护	0：禁用CPU写入的内存保护1：启用CPU写入的内存保护。	R/W
b2	RPGRPA	大师组A读Protection	0：禁用主组A读取的内存保护1：启用主组A读取的内存保护。	R/W
b3	WPGRPA	大师组A写Protection	0：禁用主组A写入的内存保护1：启用主组A写入的内存保护。	R/W
b4	RPGRPB	主组B读取Protection	0：禁用主机组B读取的内存保护1：启用主机组B读取的内存保护。	R/W
b5	WPGRPB	主组B写Protection	0：禁用主组B写入的内存保护1：启用主组B写入的内存保护。	R/W
b6	RPGRPC	大师组C读Protection	1：启用主组C读取的内存保护。该位读取为1。写入值应为1。	R/W
b7	WPGRPC	大师组C写Protection	1：启用主组C写入的内存保护。该位读取为1。写入值应为1。	R/W
b15 to b8	—	Reserved	这些位被读取为0。写入值应为0。	R/W

RPCPU位（CPU读保护）

RPCPU位启用或禁用CPU在内部外围总线9上读取的内存保护。

WPCPU位（CPU写保护）

WPCPU位启用或禁用CPU在内部外围总线9上写入的内存保护。

RRPGRPA位（主组A读保护）

RPGRPA位启用或禁用内部外设总线9上主机组A读取的内存保护。

WPGRPA位（主组A写保护）

WPGRPA位启用或禁用内部外设总线9上主组A写入的存储器保护。

RPGRPB位（MasterGroupB读保护）

RPGRPB位启用或禁用内部外设总线9上的主机组B读取的内存保护。

WPGRPB位（主机组B写保护）

WPGRPB位启用或禁用内部外设总线9上的主机组B写入的存储器保护。

RPGRPC位（MasterGroupC读保护）

RPGRPC位为主机组C在内部外围总线9上的读取启用内存保护。主机组C和内部外围总线9之间没有连接。该位读取为1，写入值应为1。

WPGRPC位（主控组C写保护）

WPGRPC位使能主组C对内部外设总线9的写的内存保护。主组C和内部外设总线9之间没有连接。该位读为1，写值应为1。

16.5.1.3 Access Control Register for Memory Bus 4 (SMPUSRAM0)

Address(es): SMPU.SMPUSRAM0 4000 0C18h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	WPGRPC	RPGRPC	WPGRPB	RPGRPB	WPGRPA	RPGRPA	WPCPU	RPCPU
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	RPCPU	CPU Read protection	0: Memory protection for CPU reads disabled 1: Memory protection for CPU reads enabled.	R/W
b1	WPCPU	CPU Write protection	0: Memory protection for CPU writes disabled 1: Memory protection for CPU writes enabled.	R/W
b2	RPGRPA	Master Group A Read protection	0: Memory protection for master group A reads disabled 1: Memory protection for master group A reads enabled.	R/W
b3	WPGRPA	Master Group A Write protection	0: Memory protection for master group A writes disabled 1: Memory protection for master group A writes enabled.	R/W
b4	RPGRPB	Master Group B Read protection	0: Memory protection for master group B reads disabled 1: Memory protection for master group B reads enabled.	R/W
b5	WPGRPB	Master Group B Write protection	0: Memory protection for master group B writes disabled 1: Memory protection for master group B writes enabled.	R/W
b6	RPGRPC	Master Group C Read protection	0: Memory protection for master group C reads disabled 1: Memory protection for master group C reads enabled.	R/W
b7	WPGRPC	Master Group C Write protection	0: Memory protection for master group C writes disabled 1: Memory protection for master group C writes enabled.	R/W
b15 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

RPCPU bit (CPU Read protection)

The RPCPU bit enables or disables memory protection for reads by the CPU on memory bus 4.

WPCPU bit (CPU Write protection)

The WPCPU bit enables or disables memory protection for writes by the CPU on memory bus 4.

RPGRPA bit (Master Group A Read protection)

The RPGRPA bit enables or disables memory protection for reads by master group A on memory bus 4.

WPGRPA bit (Master Group A Write protection)

The WPGRPA bit enables or disables memory protection for writes by master group A on memory bus 4.

RPGRPB bit (Master Group B Read protection)

The RPGRPB bit enables or disables memory protection for reads by master group B on memory bus 4.

WPGRPB bit (Master Group B Write protection)

The WPGRPB bit enables or disables memory protection for writes by master group B on memory bus 4.

RPGRPC bit (Master Group C Read protection)

The RPGRPC bit enables or disables memory protection for reads by master group C on memory bus 4.

WPGRPC bit (Master Group C Write protection)

The WPGRPC bit enables or disables memory protection for writes by master group C on memory bus 4.

16.5.1.3 存储器总线4的访问控制寄存器(SMPUSRAM0)

Address(es): SMPU.SMPUSRAM0 4000 0C18h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	WPGRPC	RPGRPC	WPGRPB	RPGRPB	WPGRPA	RPGRPA	WPCPU	RPCPU
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	RPCPU	CPU读保护	0：禁用CPU读取的内存保护1：启用CPU读取的内存保护。	R/W
b1	WPCPU	CPU写保护	0：禁用CPU写入的内存保护1：启用CPU写入的内存保护。	R/W
b2	RPGRPA	主组A读保护	0：禁用主组A读取的内存保护1：启用主组A读取的内存保护。	R/W
b3	WPGRPA	主组A写保护	0：禁用主组A写入的内存保护1：启用主组A写入的内存保护。	R/W
b4	RPGRPB	MasterGroupB读保护	0：禁用主机组B读取的内存保护1：启用主机组B读取的内存保护。	R/W
b5	WPGRPB	主组B写保护	0：禁用主组B写入的内存保护1：启用主组B写入的内存保护。	R/W
b6	RPGRPC	MasterGroupC读保护	0：禁用主组C读取的内存保护1：启用主组C读取的内存保护。	R/W
b7	WPGRPC	主控组C写保护	0：禁用主机组C写入的内存保护1：启用主机组C写入的内存保护。	R/W
b15 to b8	—	Reserved	这些位被读取为0。写入值应为0。	R/W

RPCPU位（CPU读保护）

RPCPU位启用或禁用内存总线4上CPU读取的内存保护。

WPCPU位（CPU写保护）

WPCPU位启用或禁用内存总线4上CPU写入的内存保护。

RRPGRPA位（主组A读保护）

RPGRPA位启用或禁用内存总线4上主机组A读取的内存保护。

WPGRPA位（主组A写保护）

WPGRPA位启用或禁用内存总线4上主机组A写入的内存保护。

RPGRPB位（MasterGroupB读保护）

RPGRPB位启用或禁用内存总线4上主机组B读取的内存保护。

WPGRPB位（MasterGroupB写保护）

WPGRPB位启用或禁用内存总线4上主机组B写入的内存保护。

RPGRPC位（MasterGroupC读保护）

RPGRPC位启用或禁用内存总线4上的主组C读取的内存保护。

WPGRPC位（MasterGroupC写保护）

WPGRPC位启用或禁用主组C在内存总线4上写入的内存保护。

16.5.1.4 Access Control Register for Memory Bus 5 (SMPUSRAM1)

Address(es): SMPU.SMPUSRAM1 4000 0C1Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	WPGRPC	RPGRPC	WPGRPB	RPGRPB	WPGRPA	RPGRPA	WPCPU	RPCPU
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	RPCPU	CPU Read Protection	0: Memory protection for CPU reads disabled 1: Memory protection for CPU reads enabled.	R/W
b1	WPCPU	CPU Write Protection	0: Memory protection for CPU writes disabled 1: Memory protection for CPU writes enabled.	R/W
b2	RPGRPA	Master Group A Read Protection	0: Memory protection for master group A reads disabled 1: Memory protection for master group A reads enabled.	R/W
b3	WPGRPA	Master Group A Write Protection	0: Memory protection for master group A writes disabled 1: Memory protection for master group A writes enabled.	R/W
b4	RPGRPB	Master Group B Read Protection	0: Memory protection for master group B reads disabled 1: Memory protection for master group B reads enabled.	R/W
b5	WPGRPB	Master Group B Write Protection	0: Memory protection for master group B writes disabled 1: Memory protection for master group B writes enabled.	R/W
b6	RPGRPC	Master Group C Read Protection	0: Memory protection for master group C reads disabled 1: Memory protection for master group C reads enabled.	R/W
b7	WPGRPC	Master Group C Write Protection	0: Memory protection for master group C writes disabled 1: Memory protection for master group C writes enabled.	R/W
b15 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

RPCPU bit (CPU Read Protection)

The RPCPU bit enables or disables memory protection for reads by the CPU on memory bus 5.

WPCPU bit (CPU Write Protection)

The WPCPU bit enables or disables memory protection for writes by the CPU on memory bus 5.

RPGRPA bit (Master Group A Read Protection)

The RPGRPA bit enables or disables memory protection for reads by master group A on memory bus 5.

WPGRPA bit (Master Group A Write Protection)

The WPGRPA bit enables or disables memory protection for writes by master group A on memory bus 5.

RPGRPB bit (Master Group B Read Protection)

The RPGRPB bit enables or disables memory protection for reads by master group B on memory bus 5.

WPGRPB bit (Master Group B Write Protection)

The WPGRPB bit enables or disables memory protection for writes by master group B on memory bus 5.

RPGRPC bit (Master Group C Read Protection)

The RPGRPC bit enables or disables memory protection for reads by master group C on memory bus 5.

WPGRPC bit (Master Group C Write Protection)

The WPGRPC bit enables or disables memory protection for writes by master group C on memory bus 5.

16.5.1.4 存储器总线5(SMPUSRAM1)的访问控制寄存器

Address(es): SMPU.SMPUSRAM1 4000 0C1Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	WPGRPC	RPGRPC	WPGRPB	RPGRPB	WPGRPA	RPGRPA	WPCPU	RPCPU
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	RPCPU	CPU读保护	0：禁用CPU读取的内存保护1：启用CPU读取的内存保护。	R/W
b1	WPCPU	CPU写保护	0：禁用CPU写入的内存保护1：启用CPU写入的内存保护。	R/W
b2	RPGRPA	大师组A读Protection	0：禁用主组A读取的内存保护1：启用主组A读取的内存保护。	R/W
b3	WPGRPA	大师组A写Protection	0：禁用主组A写入的内存保护1：启用主组A写入的内存保护。	R/W
b4	RPGRPB	主组B读取Protection	0：禁用主机组B读取的内存保护1：启用主机组B读取的内存保护。	R/W
b5	WPGRPB	主组B写Protection	0：禁用主组B写入的内存保护1：启用主组B写入的内存保护。	R/W
b6	RPGRPC	大师组C读Protection	0：禁用主组C读取的内存保护1：启用主组C读取的内存保护。	R/W
b7	WPGRPC	大师组C写Protection	0：禁用主机组C写入的内存保护1：启用主机组C写入的内存保护。	R/W
b15 to b8	—	Reserved	这些位被读取为0。写入值应为0。	R/W

RPCPU位（CPU读保护）

RPCPU位启用或禁用内存总线5上CPU读取的内存保护。

WPCPU位（CPU写保护）

WPCPU位启用或禁用内存总线5上CPU写入的内存保护。

RRPGRPA位（主组A读保护）

RPGRPA位启用或禁用内存总线5上主机组A读取的内存保护。

WPGRPA位（主组A写保护）

WPGRPA位启用或禁用内存总线5上主机组A写入的内存保护。

RPGRPB位（MasterGroupB读保护）

RPGRPB位启用或禁用内存总线5上的主组B读取的内存保护。

WPGRPB位（主机组B写保护）

WPGRPB位启用或禁用内存总线5上主机组B写入的内存保护。

RPGRPC位（MasterGroupC读保护）

RPGRPC位启用或禁用内存总线5上的主组C读取的内存保护。

WPGRPC位（主控组C写保护）

WPGRPC位启用或禁用主组C对内存总线5的写入的内存保护。

16.5.1.5 Access Control Register for Internal Peripheral Bus 1 (SMPUP0BIU)

Address(es): SMPU.SMPUP0BIU 4000 0C20h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	WPGRPC	RPGRPC	WPGRPB	RPGRPB	WPGRPA	RPGRPA	WPCPU	RPCPU
Value after reset:	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	RPCPU	CPU Read Protection	0: Memory protection for CPU reads disabled 1: Memory protection for CPU reads enabled.	R/W
b1	WPCPU	CPU Write Protection	0: Memory protection for CPU writes disabled 1: Memory protection for CPU writes enabled.	R/W
b2	RPGRPA	Master Group A Read Protection	0: Memory protection for master group A reads disabled 1: Memory protection for master group A reads enabled.	R/W
b3	WPGRPA	Master Group A Write Protection	0: Memory protection for master group A writes disabled 1: Memory protection for master group A writes enabled.	R/W
b4	RPGRPB	Master Group B Read Protection	1: Memory protection for master group B reads enabled. Master group B is protected, and is not detected. This bit is read as 1. The write value should be 1.	R/W
b5	WPGRPB	Master Group B Write Protection	1: Memory protection for master group B writes enabled. Master group B is protected, and is not detected. This bit is read as 1. The write value should be 1.	R/W
b6	RPGRPC	Master Group C Read Protection	0: Memory protection for master group C reads disabled 1: Memory protection for master group C reads enabled. Master group C is protected, and is not detected. This bit is read as 1. The write value should be 1.	R/W
b7	WPGRPC	Master Group C Write Protection	0: Memory protection for master group C writes disabled 1: Memory protection for master group C writes enabled. Master group C is protected, and is not detected. This bit is read as 1. The write value should be 1.	R/W
b15 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

RPCPU bit (CPU Read Protection)

The RPCPU bit enables or disables memory protection for reads by the CPU on internal peripheral bus 1.

WPCPU bit (CPU Write Protection)

The WPCPU bit enables or disables memory protection for writes by the CPU on internal peripheral bus 1.

RPGRPA bit (Master Group A Read Protection)

The RPGRPA bit enables or disables memory protection for reads by master group A on internal peripheral bus 1.

WPGRPA bit (Master Group A Write Protection)

The WPGRPA bit enables or disables memory protection for writes by master group A on internal peripheral bus 1.

RPGRPB bit (Master Group B Read Protection)

The RPGRPB bit enables memory protection for reads by master group B on internal peripheral bus 1. There is no connection between master group B and internal peripheral bus 1. This bit is read as 1, and the write value should be 1.

WPGRPB bit (Master Group B Write Protection)

The WPGRPB bit enables memory protection for writes by master group B on internal peripheral bus 1. There is no connection between master group B and internal peripheral bus 1. This bit is read as 1, and the write value should be 1.

16.5.1.5 内部外围总线1(SMPUP0BIU)的访问控制寄存器

Address(es): SMPU.SMPUP0BIU 4000 0C20h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	WPGRPC	RPGRPC	WPGRPB	RPGRPB	WPGRPA	RPGRPA	WPCPU	RPCPU
重置后的值：	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	RPCPU	CPU读保护	0：禁用CPU读取的内存保护1：启用CPU读取的内存保护。	R/W
b1	WPCPU	CPU写保护	0：禁用CPU写入的内存保护1：启用CPU写入的内存保护。	R/W
b2	RPGRPA	大师组A读Protection	0：禁用主组A读取的内存保护1：启用主组A读取的内存保护。	R/W
b3	WPGRPA	大师组A写Protection	0：禁用主组A写入的内存保护1：启用主组A写入的内存保护。	R/W
b4	RPGRPB	主组B读取Protection	1：启用主组B读取的内存保护。主组B受保护，未被检测到。该位读取为1。写入值应为1。	R/W
b5	WPGRPB	主组B写Protection	1：启用主组B写入的内存保护。主组B受保护，未被检测到。该位读取为1。写入值应为1。	R/W
b6	RPGRPC	大师组C读Protection	0：禁用主组C读取的内存保护1：启用主组C读取的内存保护。主组C受保护，未被检测到。该位读取为1。写入值应为1。	R/W
b7	WPGRPC	大师组C写Protection	0：禁用主机组C写入的内存保护1：启用主机组C写入的内存保护。主组C受保护，未被检测到。该位读取为1。写入值应为1。	R/W
b15 to b8	—	Reserved	这些位被读取为0。写入值应为0。	R/W

RPCPU位（CPU读保护）

RPCPU位启用或禁用CPU在内部外围总线1上读取的内存保护。

WPCPU位（CPU写保护）

WPCPU位启用或禁用CPU在内部外围总线1上写入的内存保护。

RRPGRPA位（主组A读保护）

RPGRPA位启用或禁用内部外设总线1上主机组A读取的内存保护。

WPGRPA位（主组A写保护）

WPGRPA位启用或禁用内部外设总线1上主机组A写入的存储器保护。

RPGRPB位（MasterGroupB读保护）

RPGRPB位为主机组B在内部外围总线1上的读取启用内存保护。主机组B和内部外围总线1之间没有连接。该位读取为1，写入值应为1。

WPGRPB位（主机组B写保护）

WPGRPB位为主机组B对内部外设总线1的写入启用内存保护。主机组B和内部外设总线1之间没有连接。该位读取为1，写入值应为1。

RPGRPC bit (Master Group C Read Protection)

The RPGRPC bit enables memory protection for reads by master group C on internal peripheral bus 1. There is no connection between master group C and internal peripheral bus 1. This bit is read as 1, and the write value should be 1.

WPGRPC bit (Master Group C Write Protection)

The WPGRPC bit enables memory protection for writes by master group C on internal peripheral bus 1. There is no connection between master group C and internal peripheral bus 1. This bit is read as 1, and the write value should be 1.

16.5.1.6 Access Control Register for Internal Peripheral Bus 3 (SMPUP2BIU)

Address(es): SMPU.SMPUP2BIU 4000 0C24h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	WPGRPC	RPGRPC	WPGRPB	RPGRPB	WPGRPA	RPGRPA	WPCPU	RPCPU
Value after reset:	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	RPCPU	CPU Read Protection	0: Memory protection for CPU reads disabled 1: Memory protection for CPU reads enabled.	R/W
b1	WPCPU	CPU Write Protection	0: Memory protection for CPU writes disabled 1: Memory protection for CPU writes enabled.	R/W
b2	RPGRPA	Master Group A Read Protection	0: Memory protection for master group A reads disabled 1: Memory protection for master group A reads enabled.	R/W
b3	WPGRPA	Master Group A Write Protection	0: Memory protection for master group A writes disabled 1: Memory protection for master group A writes enabled.	R/W
b4	RPGRPB	Master Group B Read Protection	1: Memory protection for master group B reads enabled. Master group B is protected, and is not detected. This bit is read as 1. The write value should be 1.	R/W
b5	WPGRPB	Master Group B Write Protection	1: Memory protection for master group B writes enabled. Master group B is protected, and is not detected. This bit is read as 1. The write value should be 1.	R/W
b6	RPGRPC	Master Group C Read Protection	1: Memory protection for master group C reads enabled. Master group C is protected, and is not detected. This bit is read as 1. The write value should be 1.	R/W
b7	WPGRPC	Master Group C Write Protection	1: Memory protection for master group C writes enabled. Master group C is protected, and is not detected. This bit is read as 1. The write value should be 1.	R/W
b15 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

RPCPU bit (CPU Read Protection)

The RPCPU bit enables or disables memory protection for reads by the CPU on internal peripheral buses 3, 4, and 5.

WPCPU bit (CPU Write Protection)

The WPCPU bit enables or disables memory protection for writes by the CPU on internal peripheral buses 3, 4, and 5.

RPGRPA bit (Master Group A Read Protection)

The RPGRPA bit enables or disables memory protection for reads by master group A on internal peripheral buses 3, 4, and 5.

WPGRPA bit (Master Group A Write Protection)

The WPGRPA bit enables or disables memory protection for writes by master group A on internal peripheral buses 3, 4, and 5.

RPGRPC位（MasterGroupC读保护）

RPGRPC位使能主组C在内部外设总线1上读取的内存保护。主组C和内部外设总线1之间没有连接。该位读取为1，写入值应为1。

WPGRPC位（主控组C写保护）

WPGRPC位使能主机组C对内部外设总线1的写操作的内存保护。主机组C和内部外设总线1之间没有连接。该位读为1，写入值应为1。

16.5.1.6 内部外围总线3(SMPUP2BIU)的访问控制寄存器

Address(es): SMPU.SMPUP2BIU 4000 0C24h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	WPGRPC	RPGRPC	WPGRPB	RPGRPB	WPGRPA	RPGRPA	WPCPU	RPCPU
重置后的值：	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	RPCPU	CPU读保护	0：禁用CPU读取的内存保护1：启用CPU读取的内存保护。	R/W
b1	WPCPU	CPU写保护	0：禁用CPU写入的内存保护1：启用CPU写入的内存保护。	R/W
b2	RPGRPA	大师组A读Protection	0：禁用主组A读取的内存保护1：启用主组A读取的内存保护。	R/W
b3	WPGRPA	大师组A写Protection	0：禁用主组A写入的内存保护1：启用主组A写入的内存保护。	R/W
b4	RPGRPB	主组B读取Protection	1：启用主组B读取的内存保护。主组B受保护，未被检测到。该位读取为1。写入值应为1。	R/W
b5	WPGRPB	主组B写Protection	1：启用主组B写入的内存保护。主组B受保护，未被检测到。该位读取为1。写入值应为1。	R/W
b6	RPGRPC	大师组C读Protection	1：启用主组C读取的内存保护。主组C受保护，未被检测到。该位读取为1。写入值应为1。	R/W
b7	WPGRPC	大师组C写Protection	1：启用主组C写入的内存保护。主组C受保护，未被检测到。该位读取为1。写入值应为1。	R/W
b15 to b8	—	Reserved	这些位被读取为0。写入值应为0。	R/W

RPCPU位（CPU读保护）

RPCPU位启用或禁用CPU在内部外围总线3、4和5上读取的内存保护。

WPCPU位（CPU写保护）

WPCPU位启用或禁用CPU在内部外围总线3、4和5上写入的内存保护。

RRPGRPA位（主组A读保护）

RPGRPA位启用或禁用内部外设总线3、4和5上主机组A读取的内存保护。

WPGRPA位（主组A写保护）

WPGRPA位启用或禁用主机组A在内部外围总线3、4和5上写入的内存保护。

RPGRPB bit (Master Group B Read Protection)

The RPGRPB bit enables memory protection for reads by master group B on internal peripheral buses 3, 4, and 5. There is no connection between master group B and internal peripheral buses 3, 4, and 5. This bit is read as 1, and the write value should be 1.

WPGRPB bit (Master Group B Write Protection)

The WPGRPB bit enables memory protection for writes by master group B on internal peripheral buses 3, 4, and 5. There is no connection between master group B and internal peripheral buses 3, 4, and 5. This bit is read as 1, and the write value should be 1.

RPGRPC bit (Master Group C Read Protection)

The RPGRPC bit enables memory protection for reads by master group C on internal peripheral buses 3, 4, and 5. There is no connection between master group C and internal peripheral buses 3, 4, and 5. This bit is read as 1, and the write value should be 1.

WPGRPC bit (Master Group C Write Protection)

The WPGRPC bit enables memory protection for writes by master group C on internal peripheral buses 3, 4, and 5. There is no connection between master group C and internal peripheral buses 3, 4, and 5. This bit is read as 1, and the write value should be 1.

16.5.1.7 Access Control Register for Internal Peripheral Bus 7 (SMPUP6BIU)

Address(es): SMPU.SMPUP6BIU 4000 0C28h

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
—	—	—	—	—	—	—	—	WPGRPC	RPGRPC	WPGRPB	RPGRPB	WPGRPA	RPGRPA	WPCPU	RPCPU
Value after reset:	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	RPCPU	CPU Read Protection	0: Memory protection for CPU reads disabled 1: Memory protection for CPU reads enabled.	R/W
b1	WPCPU	CPU Write Protection	0: Memory protection for CPU writes disabled 1: Memory protection for CPU writes enabled.	R/W
b2	RPGRPA	Master Group A Read Protection	0: Memory protection for master group A reads disabled 1: Memory protection for master group A reads enabled.	R/W
b3	WPGRPA	Master Group A Write Protection	0: Memory protection for master group A writes disabled 1: Memory protection for master group A writes enabled.	R/W
b4	RPGRPB	Master Group B Read Protection	1: Memory protection for master group B reads enabled. Master group B is protected, and is not detected. This bit is read as 1. The write value should be 1.	R/W
b5	WPGRPB	Master Group B Write Protection	1: Memory protection for master group B writes enabled. Master group B is protected, and is not detected. This bit is read as 1. The write value should be 1.	R/W
b6	RPGRPC	Master Group C Read Protection	1: Memory protection for master group C reads enabled. Master group C is protected, and is not detected. This bit is read as 1. The write value should be 1.	R/W
b7	WPGRPC	Master Group C Write Protection	1: Memory protection for master group C writes enabled. Master group C is protected, and is not detected. This bit is read as 1. The write value should be 1.	R/W
b15 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

RPCPU bit (CPU Read Protection)

The RPCPU bit enables or disables memory protection for reads by the CPU on internal peripheral bus 7.

RPGRPB位（MasterGroupB读保护）

RPGRPB位启用内存保护，以便主机组B在内部外围总线3、4和5上进行读取。主机组B与内部外围总线3、4和5之间没有连接。该位被读取为1，并且写入值应为1。

WPGRPB位（主机组B写保护）

WPGRPB位启用内存保护，以保护主机组B在内部外围总线3、4和5上的写入。
主机组B与内部外围总线3、4、5之间没有连接。该位读为1，写值应为1。

RPGRPC位（MasterGroupC读保护）

RPGRPC位为主机组C在内部外围总线3、4和5上的读取启用内存保护。主机组C与内部外围总线3、4和5之间没有连接。该位被读取为1，并且写入值应为1。

WPGRPC位（主控组C写保护）

WPGRPC位为内部外围总线3、4和5上的主组C的写入启用内存保护。
主机组C与内部外围总线3、4、5之间没有连接。该位读为1，写值应为1。

16.5.1.7 内部外设总线7的访问控制寄存器(SMPUP6BIU)

Address(es): SMPU.SMPUP6BIU 4000 0C28h

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
—	—	—	—	—	—	—	—	WPGRPC	RPGRPC	WPGRPB	RPGRPB	WPGRPA	RPGRPA	WPCPU	RPCPU
重置后的值:	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	RPCPU	CPU读保护	0：禁用CPU读取的内存保护1：启用CPU读取的内存保护。	R/W
b1	WPCPU	CPU写保护	0：禁用CPU写入的内存保护1：启用CPU写入的内存保护。	R/W
b2	RPGRPA	大师组A读Protection	0：禁用主组A读取的内存保护1：启用主组A读取的内存保护。	R/W
b3	WPGRPA	大师组A写Protection	0：禁用主组A写入的内存保护1：启用主组A写入的内存保护。	R/W
b4	RPGRPB	主组B读取Protection	1：启用主组B读取的内存保护。主组B受保护，未被检测到。该位读取为1。写入值应为1。	R/W
b5	WPGRPB	主组B写Protection	1：启用主组B写入的内存保护。主组B受保护，未被检测到。该位读取为1。写入值应为1。	R/W
b6	RPGRPC	大师组C读Protection	1：启用主组C读取的内存保护。主组C受保护，未被检测到。该位读取为1。写入值应为1。	R/W
b7	WPGRPC	大师组C写Protection	1：启用主组C写入的内存保护。主组C受保护，未被检测到。该位读取为1。写入值应为1。	R/W
b15 to b8	—	Reserved	这些位被读取为0。写入值应为0。	R/W

RPCPU位（CPU读保护）

RPCPU位启用或禁用CPU在内部外围总线7上读取的内存保护。

WPCPU bit (CPU Write Protection)

The WPCPU bit enables or disables memory protection for writes by the CPU on internal peripheral bus 7.

RPGRPA bit (Master Group A Read Protection)

The RPGRPA bit enables or disables memory protection for reads by master group A on internal peripheral bus 7.

WPGRPA bit (Master Group A Write Protection)

The WPGRPA bit enables or disables memory protection for writes by master group A on internal peripheral bus 7.

RPGRPB bit (Master Group B Read Protection)

The RPGRPB bit enables memory protection for reads by master group B on internal peripheral bus 7. There is no connection between master group B and internal peripheral bus 7. This bit is read as 1, and the write value should be 1.

WPGRPB bit (Master Group B Write Protection)

The WPGRPB bit enables memory protection for writes by master group B on internal peripheral bus 7. There is no connection between master group B and internal peripheral bus 7. This bit is read as 1, and the write value should be 1.

RPGRPC bit (Master Group C Read Protection)

The RPGRPC bit enables memory protection for reads by master group C on internal peripheral bus 7. There is no connection between master group C and internal peripheral bus 7. This bit is read as 1, and the write value should be 1.

WPGRPC bit (Master Group C Write Protection)

The WPGRPC bit enables memory protection for writes by master group C on internal peripheral bus 7. There is no connection between master group C and internal peripheral bus 7. This bit is read as 1, and the write value should be 1.

16.5.1.8 Access Control Register for Internal Peripheral Bus 8 (SMPUP7BIU)

Address(es): SMPU.SMPUP7BIU 4000 0C2Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	WPGRPC	RPGRPC	WPGRPB	RPGRPB	WPGRPA	RPGRPA	WPCPU	RPCPU
Value after reset:	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	RPCPU	CPU Read Protection	0: Memory protection for CPU reads disabled 1: Memory protection for CPU reads enabled.	R/W
b1	WPCPU	CPU Write Protection	0: Memory protection for CPU writes disabled 1: Memory protection for CPU writes enabled.	R/W
b2	RPGRPA	Master Group A Read Protection	0: Memory protection for master group A reads disabled 1: Memory protection for master group A reads enabled.	R/W
b3	WPGRPA	Master Group A Write Protection	0: Memory protection for master group A writes disabled 1: Memory protection for master group A writes enabled.	R/W
b4	RPGRPB	Master Group B Read Protection	1: Memory protection for master group B reads enabled. Master group B is protected, and is not detected. This bit is read as 1. The write value should be 1.	R/W
b5	WPGRPB	Master Group B Write Protection	1: Memory protection for master group B writes enabled. Master group B is protected, and is not detected. This bit is read as 1. The write value should be 1.	R/W
b6	RPGRPC	Master Group C Read Protection	1: Memory protection for master group C reads enabled. Master group C is protected, and is not detected. This bit is read as 1. The write value should be 1.	R/W
b7	WPGRPC	Master Group C Write Protection	1: Memory protection for master group C writes enabled. Master group C is protected, and is not detected. This bit is read as 1. The write value should be 1.	R/W

WPCPU位（CPU写保护）

WPCPU位启用或禁用CPU在内部外围总线7上写入的内存保护。

RRPGRPA位（主组A读保护）

RPGRPA位启用或禁用内部外设总线7上主机组A读取的内存保护。

WPGRPA位（主组A写保护）

WPGRPA位启用或禁用内部外设总线7上主组A写入的存储器保护。

RPGRPB位（MasterGroupB读保护）

RPGRPB位为内部外设总线7上的主机组B读取启用内存保护。主机组B和内部外围总线7之间没有连接。该位读取为1，写入值应为1。

WPGRPB位（主机组B写保护）

WPGRPB位使能主组B在内部外设总线7上写入的存储器保护。主组B和内部外设总线7之间没有连接。该位读为1，写入值应为1。

RPGRPC位（MasterGroupC读保护）

RPGRPC位为主机组C在内部外围总线7上的读取启用内存保护。主机组C和内部外围总线7之间没有连接。该位读取为1，写入值应为1。

WPGRPC位（主控组C写保护）

WPGRPC位使能主组C对内部外设总线7的写的内存保护。主组C和内部外设总线7之间没有连接。该位读为1，写值应为1。

16.5.1.8 内部外围总线8(SMPUP7BIU)的访问控制寄存器

Address(es): SMPU.SMPUP7BIU 4000 0C2Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	WPGRPC	RPGRPC	WPGRPB	RPGRPB	WPGRPA	RPGRPA	WPCPU	RPCPU
重置后的值：	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	RPCPU	CPU读保护	0：禁用CPU读取的内存保护1：启用CPU读取的内存保护。	R/W
b1	WPCPU	CPU写保护	0：禁用CPU写入的内存保护1：启用CPU写入的内存保护。	R/W
b2	RPGRPA	大师组A读Protection	0：禁用主组A读取的内存保护1：启用主组A读取的内存保护。	R/W
b3	WPGRPA	大师组A写Protection	0：禁用主组A写入的内存保护1：启用主组A写入的内存保护。	R/W
b4	RPGRPB	主组B读取Protection	1：启用主组B读取的内存保护。主组B受保护，未被检测到。该位读取为1。写入值应为1。	R/W
b5	WPGRPB	主组B写Protection	1：启用主组B写入的内存保护。主组B受保护，未被检测到。该位读取为1。写入值应为1。	R/W
b6	RPGRPC	大师组C读Protection	1：启用主组C读取的内存保护。主组C受保护，未被检测到。该位读取为1。写入值应为1。	R/W
b7	WPGRPC	大师组C写Protection	1：启用主组C写入的内存保护。主组C受保护，未被检测到。该位读取为1。写入值应为1。	R/W

Bit	Symbol	Bit name	Description	R/W
b15 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

RPCPU bit (CPU Read Protection)

The RPCPU bit enables or disables memory protection for reads by the CPU on internal peripheral bus 8.

WPCPU bit (CPU Write Protection)

The WPCPU bit enables or disables memory protection for writes by the CPU on internal peripheral bus 8.

RPGRPA bit (Master Group A Read Protection)

The RPGRPA bit enables or disables memory protection for reads by master group A on internal peripheral bus 8.

WPGRPA bit (Master Group A Write Protection)

The WPGRPA bit enables or disables memory protection for writes by master group A on internal peripheral bus 8.

RPGRPB bit (Master Group B Read Protection)

The RPGRPB bit enables memory protection for reads by master group B on internal peripheral bus 8. There is no connection between master group B and internal peripheral bus 8. This bit is read as 1, and the write value should be 1.

WPGRPB bit (Master Group B Write Protection)

The WPGRPB bit enables memory protection for writes by master group B on internal peripheral bus 8. There is no connection between master group B and internal peripheral bus 8. This bit is read as 1, and the write value should be 1.

RPGRPC bit (Master Group C Read Protection)

The RPGRPC bit enables memory protection for reads by master group C on internal peripheral bus 8. There is no connection between master group C and internal peripheral bus 8. This bit is read as 1, and the write value should be 1.

WPGRPC bit (Master Group C Write Protection)

The WPGRPC bit enables memory protection for writes by master group C on internal peripheral bus 8. There is no connection between master group C and internal peripheral bus 8. This bit is read as 1, and the write value should be 1.

16.5.1.9 Access Control Register for CS Area and SDRAM Area (SMPUEXBIU)

Address(es): SMPU.SMPUEXBIU 4000 0C30h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	WPGRPC	RPGRPC	WPGRPB	RPGRPB	WPGRPA	RPGRPA	WPCPU	RPCPU
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	RPCPU	CPU Read Protection	0: Memory protection for CPU reads disabled 1: Memory protection for CPU reads enabled.	R/W
b1	WPCPU	CPU Write Protection	0: Memory protection for CPU writes disabled 1: Memory protection for CPU writes enabled.	R/W
b2	RPGRPA	Master Group A Read Protection	0: Memory protection for master group A reads disabled 1: Memory protection for master group A reads enabled.	R/W
b3	WPGRPA	Master Group A Write Protection	0: Memory protection for master group A writes disabled 1: Memory protection for master group A writes enabled.	R/W
b4	RPGRPB	Master Group B Read Protection	0: Memory protection for master group B reads disabled 1: Memory protection for master group B reads enabled.	R/W
b5	WPGRPB	Master Group B Write Protection	0: Memory protection for master group B writes disabled 1: Memory protection for master group B writes enabled.	R/W

Bit	Symbol	位名称	Description	R/W
b15 to b8	—	Reserved	这些位被读取为0。写入值应为0。	R/W

RPCPU位（CPU读保护）

RPCPU位启用或禁用CPU在内部外围总线8上读取的内存保护。

WPCPU位（CPU写保护）

WPCPU位启用或禁用CPU在内部外围总线8上写入的内存保护。

RRPGRPA位（主组A读保护）

RPGRPA位启用或禁用内部外设总线8上主机组A读取的内存保护。

WPGRPA位（主组A写保护）

WPGRPA位启用或禁用主机组A在内部外围总线8上写入的内存保护。

RPGRPB位（MasterGroupB读保护）

RPGRPB位为主机组B在内部外围总线8上的读取启用内存保护。主机组B和内部外围总线8之间没有连接。该位读取为1，写入值应为1。

WPGRPB位（主机组B写保护）

WPGRPB位使能主组B在内部外设总线8上写入的存储器保护。主组B和内部外设总线8之间没有连接。该位读为1，写值应为1。

RPGRPC位（MasterGroupC读保护）

RPGRPC位为主机组C在内部外围总线8上的读取启用内存保护。主机组C和内部外围总线8之间没有连接。该位读取为1，写入值应为1。

WPGRPC位（主控组C写保护）

WPGRPC位使能主机组C在内部外设总线8上的写操作的内存保护。主机组C和内部外设总线8之间没有连接。该位读为1，写入值应为1。

16.5.1.9 CS区和SDRAM区的访问控制寄存器(SMPUEXBIU)

Address(es): SMPU.SMPUEXBIU 4000 0C30h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	WPGRPC	RPGRPC	WPGRPB	RPGRPB	WPGRPA	RPGRPA	WPCPU	RPCPU
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	RPCPU	CPU读保护	0：禁用CPU读取的内存保护1：启用CPU读取的内存保护。	R/W
b1	WPCPU	CPU写保护	0：禁用CPU写入的内存保护1：启用CPU写入的内存保护。	R/W
b2	RPGRPA	大师组A读Protection	0：禁用主组A读取的内存保护1：启用主组A读取的内存保护。	R/W
b3	WPGRPA	大师组A写Protection	0：禁用主组A写入的内存保护1：启用主组A写入的内存保护。	R/W
b4	RPGRPB	主组B读取Protection	0：禁用主机组B读取的内存保护1：启用主机组B读取的内存保护。	R/W
b5	WPGRPB	主组B写Protection	0：禁用主组B写入的内存保护1：启用主组B写入的内存保护。	R/W

Bit	Symbol	Bit name	Description	R/W
b6	RPGRPC	Master Group C Read Protection	0: Memory protection for master group C reads disabled 1: Memory protection for master group C reads enabled.	R/W
b7	WPGRPC	Master Group C Write Protection	0: Memory protection for master group C writes disabled 1: Memory protection for master group C writes enabled.	R/W
b15 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

RPCPU bit (CPU Read Protection)

The RPCPU bit enables or disables memory protection for reads by the CPU in the CS and SDRAM areas.

WPCPU bit (CPU Write Protection)

The WPCPU bit enables or disables memory protection for writes by the CPU in the CS and SDRAM areas.

RPGRPA bit (Master Group A Read Protection)

The RPGRPA bit enables or disables memory protection for reads by master group A in the CS and SDRAM areas.

WPGRPA bit (Master Group A Write Protection)

The WPGRPA bit enables or disables memory protection for writes by master group A in the CS and SDRAM areas.

RPGRPB bit (Master Group B Read Protection)

The RPGRPB bit enables or disables memory protection for reads by master group B in the CS and SDRAM areas.

WPGRPB bit (Master Group B Write Protection)

The WPGRPB bit enables or disables memory protection for writes by master group B in the CS and SDRAM areas.

RPGRPC bit (Master Group C Read Protection)

The RPGRPC bit enables or disables memory protection for reads by master group C in the CS and SDRAM areas.

WPGRPC bit (Master Group C Write Protection)

The WPGRPC bit enables or disables memory protection for writes by master group C in the CS and SDRAM areas.

16.5.1.10 Access Control Register for QSPI Area (SMPUEXBIU2)

Address(es): SMPU.SMPUEXBIU2 4000 0C34h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	WPGRPC	RPGRPC	WPGRPB	RPGRPB	WPGRPA	RPGRPA	WPCPU	RPCPU
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	RPCPU	CPU Read Protection	0: Memory protection for CPU reads disabled 1: Memory protection for CPU reads enabled.	R/W
b1	WPCPU	CPU Write Protection	0: Memory protection for CPU writes disabled 1: Memory protection for CPU writes enabled.	R/W
b2	RPGRPA	Master Group A Read Protection	0: Memory protection for master group A reads disabled 1: Memory protection for master group A reads enabled.	R/W
b3	WPGRPA	Master Group A Write Protection	0: Memory protection for master group A writes disabled 1: Memory protection for master group A writes enabled.	R/W
b4	RPGRPB	Master Group B Read Protection	0: Memory protection for master group B reads disabled 1: Memory protection for master group B reads enabled.	R/W
b5	WPGRPB	Master Group B Write Protection	0: Memory protection for master group B writes disabled 1: Memory protection for master group B writes enabled.	R/W

Bit	Symbol	位名称	Description	R/W
b6	RPGRPC	大师组C读Protection	0：禁用主组C读取的内存保护1：启用主组C读取的内存保护。	R/W
b7	WPGRPC	大师组C写Protection	0：禁用主机组C写入的内存保护1：启用主机组C写入的内存保护。	R/W
b15 to b8	—	Reserved	这些位被读取为0。写入值应为0。	R/W

RPCPU位（CPU读保护）

RPCPU位启用或禁用CPU在CS和SDRAM区域中读取的内存保护。

WPCPU位（CPU写保护）

WPCPU位启用或禁用CPU在CS和SDRAM区域中写入的内存保护。

RRPGRPA位（主组A读保护）

RPGRPA位启用或禁用主机组A在CS和SDRAM区域中读取的内存保护。

WPGRPA位（主组A写保护）

WPGRPA位启用或禁用主机组A在CS和SDRAM区域中写入的存储器保护。

RPGRPB位（MasterGroupB读保护）

RPGRPB位启用或禁用主机组B在CS和SDRAM区域中读取的内存保护。

WPGRPB位（主机组B写保护）

WPGRPB位启用或禁用主机组B在CS和SDRAM区域中写入的存储器保护。

RPGRPC位（MasterGroupC读保护）

RPGRPC位启用或禁用主机组C在CS和SDRAM区域中读取的内存保护。

WPGRPC位（主控组C写保护）

WPGRPC位启用或禁用主机组C在CS和SDRAM区域中写入的内存保护。

16.5.1.10 QSPI区域的访问控制寄存器(SMPUEXBIU2)

Address(es): SMPU.SMPUEXBIU2 4000 0C34h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	WPGRPC	RPGRPC	WPGRPB	RPGRPB	WPGRPA	RPGRPA	WPCPU	RPCPU
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	RPCPU	CPU读保护	0：禁用CPU读取的内存保护1：启用CPU读取的内存保护。	R/W
b1	WPCPU	CPU写保护	0：禁用CPU写入的内存保护1：启用CPU写入的内存保护。	R/W
b2	RPGRPA	大师组A读Protection	0：禁用主组A读取的内存保护1：启用主组A读取的内存保护。	R/W
b3	WPGRPA	大师组A写Protection	0：禁用主组A写入的内存保护1：启用主组A写入的内存保护。	R/W
b4	RPGRPB	主组B读取Protection	0：禁用主机组B读取的内存保护1：启用主机组B读取的内存保护。	R/W
b5	WPGRPB	主组B写Protection	0：禁用主组B写入的内存保护1：启用主组B写入的内存保护。	R/W

Bit	Symbol	Bit name	Description	R/W
b6	RPGRPC	Master Group C Read Protection	0: Memory protection for master group C reads disabled 1: Memory protection for master group C reads enabled.	R/W
b7	WPGRPC	Master Group C Write Protection	0: Memory protection for master group C writes disabled 1: Memory protection for master group C writes enabled.	R/W
b15 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

RPCPU bit (CPU Read Protection)

The RPCPU bit enables or disables memory protection for reads by the CPU in the QSPI area.

WPCPU bit (CPU Write Protection)

The WPCPU bit enables or disables memory protection for writes by the CPU in the QSPI area.

RPGRPA bit (Master Group A Read Protection)

The RPGRPA bit enables or disables memory protection for reads by master group A in the QSPI area.

WPGRPA bit (Master Group A Write Protection)

The WPGRPA bit enables or disables memory protection for writes by master group A in the QSPI area.

RPGRPB bit (Master Group B Read Protection)

The RPGRPB bit enables or disables memory protection for reads by master group B in the QSPI area.

WPGRPB bit (Master Group B Write Protection)

The WPGRPB bit enables or disables memory protection for writes by master group B in the QSPI area.

RPGRPC bit (Master Group C Read Protection)

The RPGRPC bit enables or disables memory protection for reads by master group C in the QSPI area.

WPGRPC bit (Master Group C Write Protection)

The WPGRPC bit enables or disables memory protection for writes by master group C in the QSPI area.

16.5.1.11 Slave MPU Control Register (SMPUCTL)

Address(es): SMPU.SMPUCTL 4000 0C00h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	KEY[7:0]								—	—	—	—	—	—	PROTECT	OAD
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	OAD	Operation After Detection	0: Non-maskable interrupt 1: Reset.	R/W
b1	PROTECT	Protection of Register	0: All bus slave MPU register writes are permitted 1: All bus slave MPU register writes are protected. Reads are permitted.	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15 to b8	KEY[7:0]	Key Code	These bits enable or disable writes to the OAD and PROTECT bits.	R/(W)*1

Note 1. Write data is not saved.

OAD bit (Operation After Detection)

The OAD bit selects either a reset or non-maskable interrupt to occur when access to the protected region is detected by the bus slave MPU. When writing to the OAD bit, write A5h simultaneously to the KEY[7:0] bits using halfword access.

Bit	Symbol	位名称	Description	R/W
b6	RPGRPC	大师组C读Protection	0：禁用主组C读取的内存保护1：启用主组C读取的内存保护。	R/W
b7	WPGRPC	大师组C写Protection	0：禁用主机组C写入的内存保护1：启用主机组C写入的内存保护。	R/W
b15 to b8	—	Reserved	这些位被读取为0。写入值应为0。	R/W

RPCPU位（CPU读保护）

RPCPU位启用或禁用CPU在QSPI区域中读取的内存保护。

WPCPU位（CPU写保护）

WPCPU位启用或禁用CPU在QSPI区域中写入的内存保护。

RRPGRPA位（主组A读保护）

RPGRPA位启用或禁用QSPI区域中主机组A读取的内存保护。

WPGRPA位（主组A写保护）

WPGRPA位启用或禁用主机组A在QSPI区域中写入的存储器保护。

RPGRPB位（MasterGroupB读保护）

RPGRPB位启用或禁用QSPI区域中主机组B读取的内存保护。

WPGRPB位（主机组B写保护）

WPGRPB位启用或禁用主机组B在QSPI区域中写入的存储器保护。

RPGRPC位（MasterGroupC读保护）

RPGRPC位启用或禁用QSPI区域中主机组C读取的内存保护。

WPGRPC位（主控组C写保护）

WPGRPC位启用或禁用主机组C在QSPI区域中写入的内存保护。

16.5.1.11 从MPU控制寄存器(SMPUCTL)

Address(es): SMPU.SMPUCTL 4000 0C00h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	KEY[7:0]								—	—	—	—	—	—	PROTECT	OAD
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	OAD	之后的操作Detection	0：不可屏蔽中断1：复位。	R/W
b1	PROTECT	登记保护	0：允许所有总线从MPU寄存器写入1：所有总线从MPU寄存器写入受到保护。允许读取。	R/W
b7 to b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b15 to b8	KEY[7:0]	关键代码	这些位启用或禁用对OAD和PROTECT位的写入。	R/(W)*1

注1.写入数据不保存。

OAD位（检测后操作）

当总线从机MPU检测到对受保护区域的访问时，OAD位选择发生复位或不可屏蔽中断。写入OAD位时，使用半字访问同时将A5h写入KEY[7:0]位。

PROTECT bit (Protection of Register)

The PROTECT bit enables or disables writes to the associated registers to be protected. SMPUCTL.PROTECT controls the following registers:

- SMPUMBIU
- SMPUFBIU
- SMPUSRAM0
- SMPUSRAM1
- SMPUP0BIU
- SMPUP2BIU
- SMPUP6BIU
- SMPUP7BIU
- SMPUEXBIU
- SMPUEXBIU2.

When writing to the PROTECT bit, write A5h simultaneously to the KEY[7:0] bits, using halfword access.

KEY[7:0] bits (Key Code)

The KEY[7:0] bits enable or disable writing to the OAD and PROTECT bits. When writing to the OAD and PROTECT bits, write A5h simultaneously to the KEY[7:0] bits. When other values are written, the OAD and PROTECT bits are not updated. The KEY[7:0] bits always read as 00h.

16.5.2 Operation

16.5.2.1 Memory protection

The bus slave MPU monitoring functions with access control information that is set for the individual access control registers. If access to a protected region is detected, the bus slave MPU generates a memory protection error.

The bus slave MPU is enabled by writing 1 to the Write Protect (WPCPU or WPGRPA) bit or the Read Protect (RPCPU or RPGRPA) bit in the access control register (SMPUMBIU, SMPUFBIU, SMPUSRAM0, SMPUSRAM1, SMPUP0BIU, SMPUP2BIU, SMPUP6BIU, SMPUP7BIU, SMPUEXBIU and SMPUEXBIU2).

16.5.2.2 Protecting the registers

To protect registers related to the bus slave MPU, set the PROTECT bit in the SMPUCTL register.

16.5.2.3 Memory protection error

The slave master MPU generates an error if access to a protected region is detected. Set the OAD bit to select whether the error is reported as a non-maskable interrupt or reset. The non-maskable interrupt status is indicated in ICU.NMISR.BUSSST. (See section 14, Interrupt Controller Unit (ICU).) Reset status is indicated in SYSTEM.RSTSR1.BUSSRF. (See section 6, Resets.)

16.6 Security MPU

The MCU incorporates a security MPU with four secure regions that include the code flash, the SRAM, and two security functions. The secure regions can be protected from non-secure program accesses. Access to a protected region from a non-secure program is not permitted.

Table 16.8 lists the specifications of the security MPU and Figure 16.10 shows a block diagram of the security MPU.

Table 16.8 Security MPU specifications

Specifications	Description
Secure regions	Code flash, SRAM, two security function

PROTECT位（寄存器保护）

PROTECT位启用或禁用对要保护的相关寄存器的写入。SMPUCTL.PROTECT控制以下寄存器：

- SMPUMBIU
- SMPUFBIU
- SMPUSRAM0
- SMPUSRAM1
- SMPUP0BIU
- SMPUP2BIU
- SMPUP6BIU
- SMPUP7BIU
- SMPUEXBIU
- SMPUEXBIU2.

写入PROTECT位时，使用半字访问同时将A5h写入KEY[7:0]位。

KEY[7:0]位（键码）

KEY[7:0]位启用或禁用对OAD和PROTECT位的写入。写入OAD和PROTECT位时，同时将A5h写入KEY[7:0]位。写入其他值时，不会更新OAD和PROTECT位。KEY[7:0]位总是读为00h。

16.5.2 Operation

16.5.2.1 内存保护

总线从属MPU使用为各个访问控制寄存器设置的访问控制信息来监控功能。如果检测到对受保护区域的访问，则总线从MPU会产生内存保护错误。

通过向访问控制寄存器（SMPUMBIU、SMPUFBIU、SMPUSRAM0、SMPUSRAM1、SMPUP0BIU、SMPUP2BIU、SMPUP6BIU、SMPUP7BIU）中的写保护（WPCPU或WPGRPA）位或读保护（RPCPU或RPGRPA）位写1来启用总线从MPU SMPUEXBIU和SMPUEXBIU2)。

16.5.2.2 保护寄存器

为了保护与总线从MPU相关的寄存器，设置SMPUCTL寄存器中的PROTECT位。

16.5.2.3 内存保护错误

如果检测到对受保护区域的访问，则从属主控MPU生成错误。设置OAD位以选择将错误报告为不可屏蔽中断还是复位。不可屏蔽中断状态在ICU.NMISR.BUSSST中指示。（参见第14节，中断控制器单元(ICU)。）复位状态在

SYSTEM.RSTSR1.BUSSRF。（参见第6节，重置。）

16.6 Security MPU

MCU包含一个安全MPU，它具有四个安全区域，包括代码闪存、SRAM和两个安全功能。可以保护安全区域免受非安全程序访问。不允许从非安全程序访问受保护区域。

表16.8列出了安全MPU的规格，图16.10显示了安全MPU的框图。

Table 16.8 安全MPU规格

Specifications	Description
安全区域	Codeflash、SRAM、两个安全功能

Table 16.8 Security MPU specifications

Specifications	Description
Protected regions	0000 0000h to FFFF FFFFh
Number of regions	Program Counter: 2 regions Data access: 4 regions
Address specification for individual regions	Setting the address where regions start and end
Enable/disable setting for memory protection in individual regions	Settings enabled or disabled for the associated region

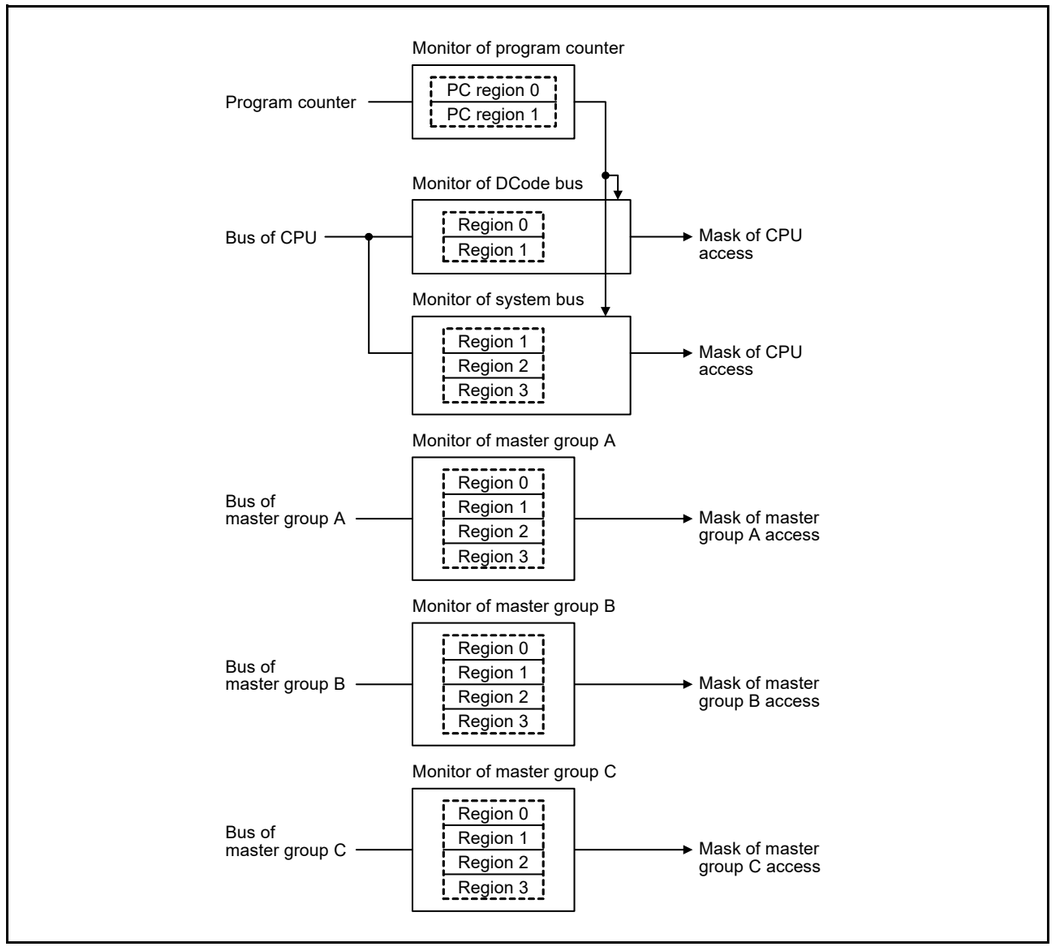


Figure 16.10 Security MPU block diagram

16.6.1 Register Descriptions (Option-Setting memory)

All security MPU registers are option-setting memory. Option-setting memory refers to a set of registers that are provided for selecting the state of the microcontroller after a reset. The option-setting memory is allocated in the flash.

Table 16.8 安全MPU规格

Specifications	Description
保护区	0000 0000h to FFFF FFFFh
地区数量	节目计数器：2个地区 数据访问：4个地区
个别地区的地址规范	设置区域开始和结束的地址
在各个区域启用禁用内存保护设置	为关联区域启用或禁用的设置

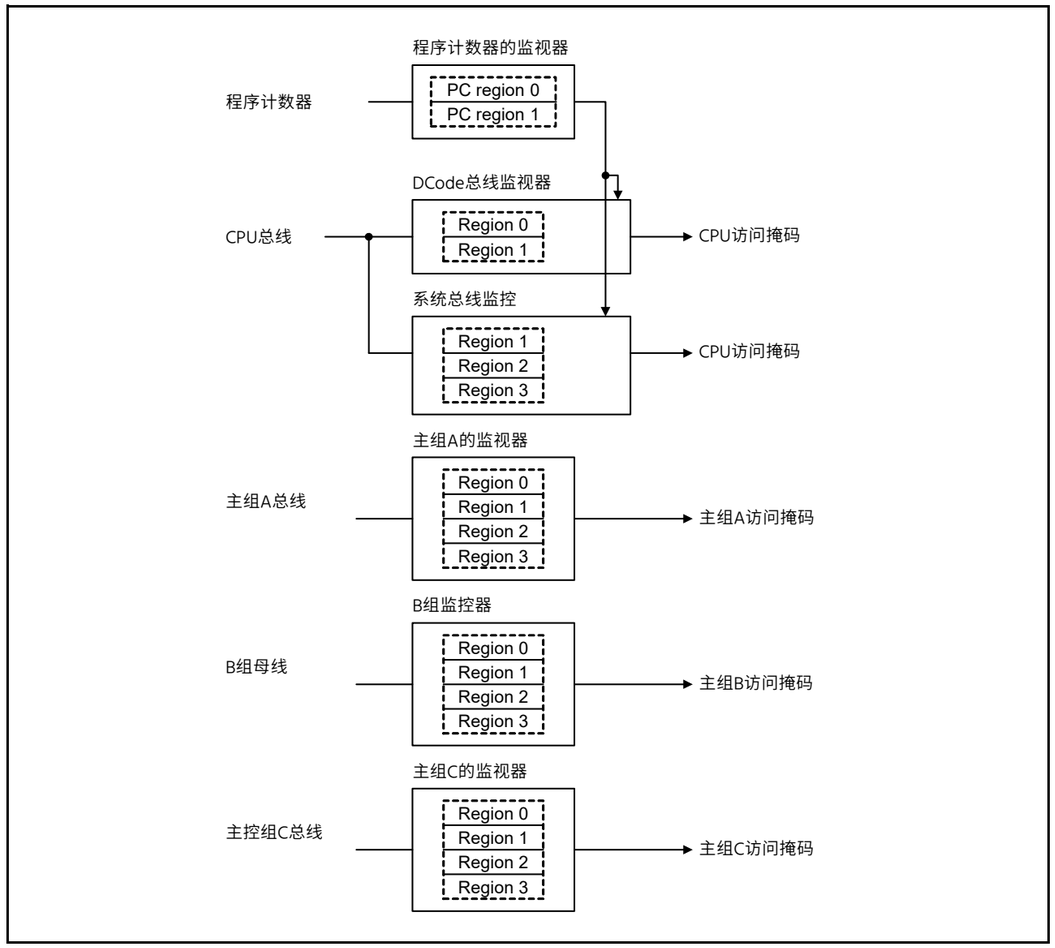


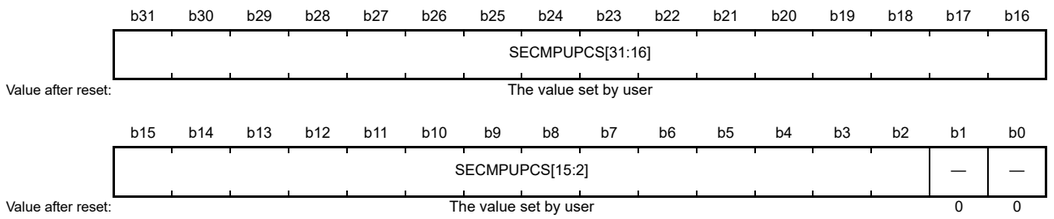
Figure 16.10 安全MPU框图

16.6.1 寄存器说明（选项设置存储器）

所有安全MPU寄存器都是选项设置存储器。选项设置存储器是指一组寄存器，用于在复位后选择微控制器的状态。选项设置内存在闪存中分配。

16.6.1.1 Security MPU Program Counter Start Address Register (SECMPUPCSn) (n = 0, 1)

Address(es): SECMPUPCS0 0000 0408h, SECMPUPCS1 0000 0410h



Bit	Symbol	Bit name	Description	R/W
b1, b0	—	Reserved	These bits are read as 0. When writing to flash, the write value should always be 0.	R
b31 to b2	SECMPUPCS[31:2]	Region Start Address	Address where the region starts, for use in region determination.	R

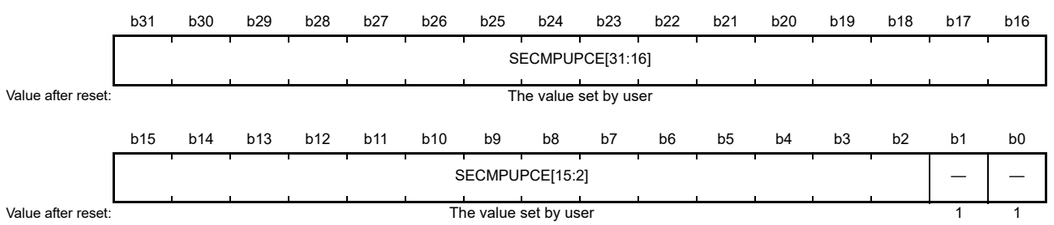
The SECMPUPCSn and SECMPUPCEn registers specify the security fetch region of the code flash or SRAM (0000 0000h to FFFF FFFFh). The secure program is executed in the memory space defined by the SECMPUPCSn and SECMPUPCEn registers and can access the secure data specified in the SECMPUSm and SECMPUEm registers (m = 0 to 3).

The SECMPUPCSn register specifies the start address where the region starts. Setting of the memory mirror space (0200 0000h to 027F FFFFh) for MMF is prohibited.

An address space of greater than 12 bytes is required between the last instruction of the non-secure program and the first instruction of the secure program.

16.6.1.2 Security MPU Program Counter End Address Register (SECMPUPCEn) (n = 0, 1)

Address(es): SECMPUPCE0 0000 040Ch, SECMPUPCE1 0000 0414h



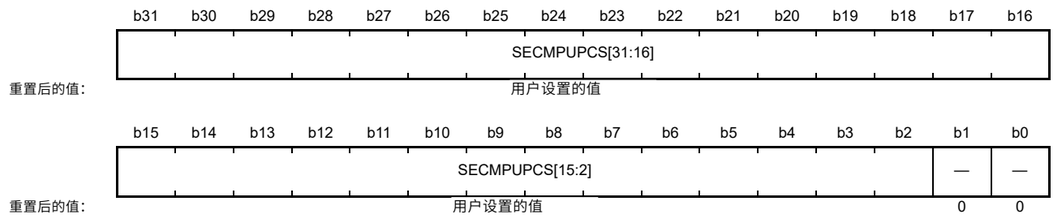
Bit	Symbol	Bit name	Description	R/W
b1, b0	—	Reserved	These bits are read as 1. When writing to flash, the write value should always be 1.	R
b31 to b2	SECMPUPCE[31:2]	Region End Address	Address where the region ends, for use in region determination.	R

The SECMPUPCSn and SECMPUPCEn registers specify the security fetch region of code flash or SRAM (0000 0000h to FFFF FFFFh).

The SECMPUPCEn register specifies the end address where the region ends.

16.6.1.1 安全MPU程序计数器起始地址寄存器(SECMPUPCSn)(n=0 1)

Address(es): SECMPUPCS0 0000 0408h, SECMPUPCS1 0000 0410h



Bit	Symbol	位名称	Description	R/W
b1, b0	—	Reserved	这些位被读取为0。写入闪存时，写入值应始终为0。	R
b31 to b2	SECMPUPCS[31:2]	区域起始地址	区域开始的地址，用于区域确定。	R

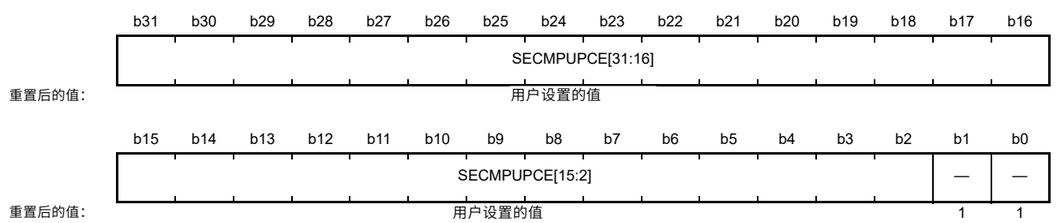
SECMPUPCSn和SECMPPCEn寄存器指定代码闪存或SRAM的安全提取区域（00000000h至FFFFFFFFh）。安全程序在由SECMPUPCSn和SECMPPCEn寄存器定义的存储空间中执行，并且可以访问在SECMPUSm和SECMPUEm寄存器（m=0到3）中指定的安全数据。

SECMPUPCSn寄存器指定区域开始的起始地址。禁止为MMF设置内存镜像空间（02000000h到027FFFFFh）。

在非安全程序的最后一条指令和安全程序的第一条指令之间需要一个大于12字节的地址空间。

16.6.1.2 安全MPU程序计数器结束地址寄存器(SECMPUPCEn)(n=0 1)

Address(es): SECMPUPCE0 0000 040Ch, SECMPUPCE1 0000 0414h



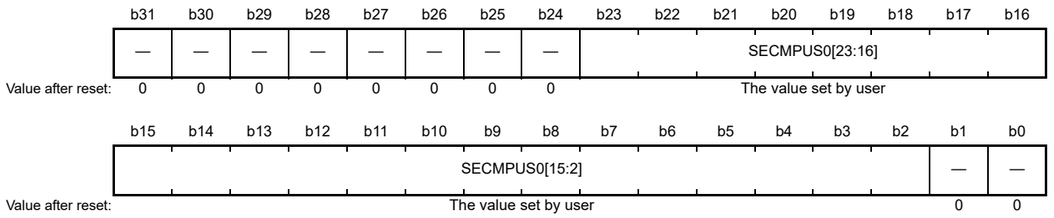
Bit	Symbol	位名称	Description	R/W
b1, b0	—	Reserved	这些位读取为1。写入闪存时，写入值应始终为1。	R
b31 to b2	SECMPUPCE[31:2]	区域结束地址	区域结束的地址，用于区域确定。	R

SECMPUPCSn和SECMPPCEn寄存器指定代码闪存或SRAM的安全提取区域（00000000h至FFFFFFFFh）。

SECPUPCEn寄存器指定区域结束的结束地址。

16.6.1.3 Security MPU Region 0 Start Address Register (SECMPUS0)

Address(es): SECMPUS0 0000 0418h



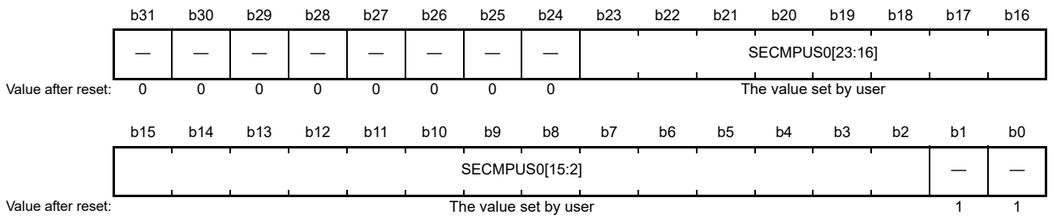
Bit	Symbol	Bit name	Description	R/W
b1, b0	—	Reserved	These bits are read as 0. When writing to flash, the write value should always be 0.	R
b23 to b2	SECMPUS0[23:2]	Region Start Address	Address where the region starts, for use in region determination.	R
b31 to b24	—	Reserved	These bits are read as 0. When writing to flash, the write value should always be 0.	R

The SECMPUS0 and SECMPUE0 registers specify the secure region of flash (0000 0000 to 00FF FFFFh), which can be accessed only from the secure program set up by SECMPUPCSn and SECMPUPCEn.

The SECMPUS0 register specifies the start address where the region starts. Setting of the vector table area is prohibited.

16.6.1.4 Security MPU Region 0 End Address Register (SECMPUE0)

Address(es): SECMPUE0 0000 041Ch



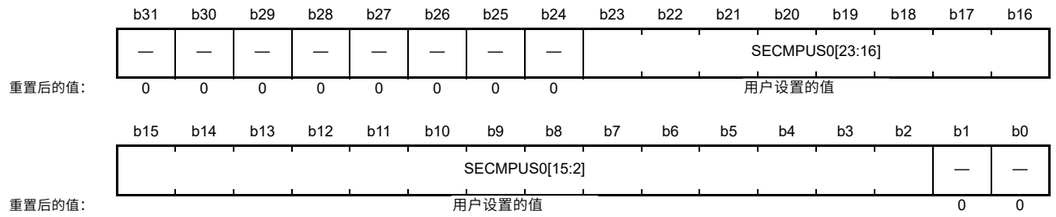
Bit	Symbol	Bit name	Description	R/W
b1, b0	—	Reserved	These bits are read as 1. When writing to flash, the write value should always be 1.	R
b23 to b2	SECMPUE0[23:2]	Region End Address	Address where the region end, for use in region determination.	R
b31 to b24	—	Reserved	These bits are read as 0. When writing to flash, the write value should always be 0.	R

The SECMPUS0 and SECMPUE0 registers specify the secure region of flash (0000 0000 to 00FF FFFFh). The memory space defined in the SECMPUS0 and SECMPUE0 registers can only be accessed from the secure program set up in the SECMPUPCSn and SECMPUPCEn registers.

The SECMPUE0 register specifies the end address where the region ends.

16.6.1.3 安全MPU区域0起始地址寄存器(SECMPUS0)

Address(es): SECMPUS0 0000 0418h



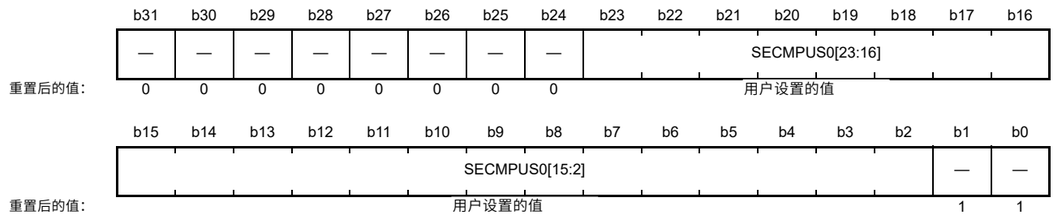
Bit	Symbol	位名称	Description	R/W
b1, b0	—	Reserved	这些位被读取为0。写入闪存时，写入值应始终为0。	R
b23 to b2	SECMPUS0[23:2]	区域起始地址	区域开始的地址，用于区域确定。	R
b31 to b24	—	Reserved	这些位被读取为0。写入闪存时，写入值应始终为0。	R

SECMPUS0和SECMPUE0寄存器指定闪存的安全区域（00000000到00FFFFFFh），只能从由SECMPUPCSn和SECMPPCEn设置的安全程序访问。

SECMPUS0寄存器指定区域开始的起始地址。禁止设置向量表区域。

16.6.1.4 安全MPU区域0结束地址寄存器(SECMPUE0)

Address(es): SECMPUE0 0000 041Ch



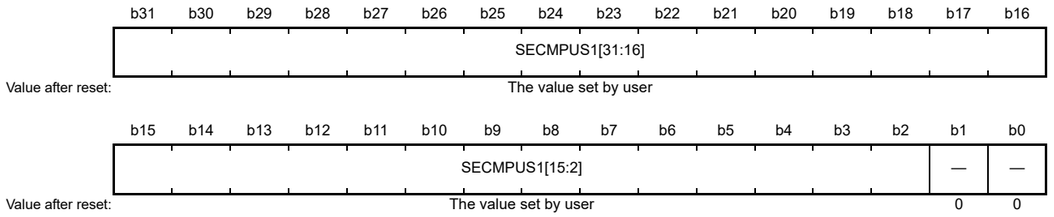
Bit	Symbol	位名称	Description	R/W
b1, b0	—	Reserved	这些位读取为1。写入闪存时，写入值应始终为1。	R
b23 to b2	SECMPUE0[23:2]	区域结束地址	区域结束的地址，用于区域确定。	R
b31 to b24	—	Reserved	这些位被读取为0。写入闪存时，写入值应始终为0。	R

SECMPUS0和SECMPUE0寄存器指定闪存的安全区域（00000000到00FFFFFFh）。SECMPUS0和SECMPUE0寄存器中定义的存储空间只能从SECMPUPCSn和SECMPPCEn寄存器中设置的安全程序访问。

SECMPUE0寄存器指定区域结束的结束地址。

16.6.1.5 Security MPU Region 1 Start Address Register (SECMPUS1)

Address(es): SECMPUS1 0000 0420h



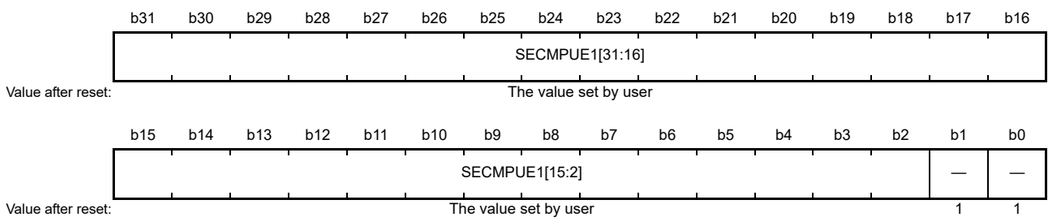
Bit	Symbol	Bit name	Description	R/W
b1, b0	—	Reserved	These bits are read as 0. When writing to flash, the write value should always be 0.	R
b19 to b2	SECMPUS1[19:2]	Region Start Address	Address where the region starts, for use in region determination.	R
b31 to b20	SECMPUS1[31:20]	Region Start Address	Address where the region starts, for use in region determination. The write value should always be 1FFh or 200h.	R

The SECMPUS1 and SECMPUE1 registers specify the secure region of SRAM (1FF0 0000h to 200F FFFFh), which can be accessed only from the secure program set up by SECMPUPCSn and SECMPUPCEn.

The SECMPUS1 register specifies the start address where the region starts. Setting of the stack area and the vector table are prohibited.

16.6.1.6 Security MPU Region 1 End Address Register (SECMPUE1)

Address(es): SECMPUE1 0000 0424h



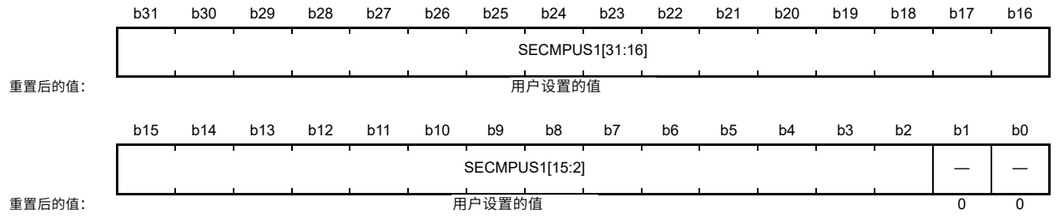
Bit	Symbol	Bit name	Description	R/W
b1, b0	—	Reserved	These bits are read as 1. When writing to flash, the write value should always be 1.	R
b19 to b2	SECMPUE1[19:2]	Region End Address	Address where the region ends, for use in region determination.	R
b31 to b20	SECMPUE1[31:20]	Region End Address	Address where the region end, for use in region determination. The write value should always be 1FFh or 200h.	R

The SECMPUS1 and SECMPUE1 registers specify the secure region of SRAM (1FF0 0000h to 200F FFFFh). The memory space defined in the SECMPUS1 and SECMPUE1 registers can only be accessed from the secure program set up in the SECMPUPCSn and SECMPUPCEn registers.

The SECMPUE1 register specifies the end address where the region ends.

16.6.1.5 安全MPU区域1起始地址寄存器(SECMPUS1)

Address(es): SECMPUS1 0000 0420h



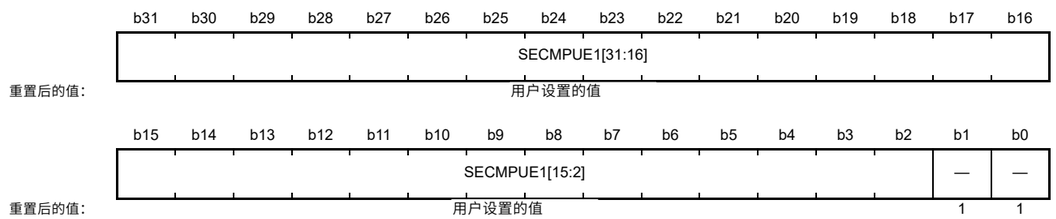
Bit	Symbol	位名称	Description	R/W
b1, b0	—	Reserved	这些位被读取为0。写入闪存时，写入值应始终为0。	R
b19 to b2	SECMPUS1[19:2]	区域起始地址	区域开始的地址，用于区域确定。	R
b31 to b20	SECMPUS1[31:20]	区域起始地址	区域开始的地址，用于区域确定。写入值应始终为1FFh或200h。	R

SECMPUS1和SECMPUE1寄存器指定SRAM的安全区域（1FF00000h到200FFFFFh），只能从SECMPUPCSn和SECMPPCEn设置的安全程序访问。

SECMPUS1寄存器指定区域开始的起始地址。禁止设置堆栈区和向量表。

16.6.1.6 安全MPU区域1结束地址寄存器(SECMPUE1)

Address(es): SECMPUE1 0000 0424h



Bit	Symbol	位名称	Description	R/W
b1, b0	—	Reserved	这些位读取为1。写入闪存时，写入值应始终为1。	R
b19 to b2	SECMPUE1[19:2]	区域结束地址	区域结束的地址，用于区域确定。	R
b31 to b20	SECMPUE1[31:20]	区域结束地址	区域结束的地址，用于区域确定。写入值应始终为1FFh或200h。	R

SECMPUS1和SECMPUE1寄存器指定SRAM的安全区域（1FF00000h到200FFFFFh）。SECMPUS1和SECMPUE1寄存器中定义的存储空间只能从SECMPUPCSn和SECMPPCEn寄存器中设置的安全程序访问。

SECMPUE1寄存器指定区域结束的结束地址。

16.6.1.7 Security MPU Region 2 Start Address Register (SECMPUS2)

Address(es): SECMPUS2 0000 0428h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	SECMPUS2[22:16]						
Value after reset:	0	1	0	0	0	0	0	0	0	The value set by user						

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SECMPUS2[15:2]														—	—
Value after reset:	The value set by user														0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	—	Reserved	These bits are read as 0. When writing to flash, the write value should always be 0.	R
b22 to b2	SECMPUS2[22:2]	Region Start Address	Address where the region starts, for use in region determination	R
b29 to b23	—	Reserved	These bits are read as 0. When writing to flash, the write value should always be 0.	R
b30	—	Reserved	This bit is read as 1. When writing to flash, the write value should always be 1.	R
b31	—	Reserved	This bit is read as 0. When writing to flash, the write value should always be 0.	R

The SECMPUS2 and SECMPUE2 registers specify the secure region for security function 1 (400C 0000 to 400D FFFFh and 4010 0000 to 407F FFFFh). The secure region can be accessed only from the secure program set up by SECMPUPCSn and SECMPUPCEn.

The SECMPUS2 register specifies the start address where the region starts.

16.6.1.8 Security MPU Region 2 End Address Register (SECMPUE2)

Address(es): SECMPUE2 0000 042Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	SECMPUE2[22:16]						
Value after reset:	0	1	0	0	0	0	0	0	0	The value set by user						

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SECMPUE2[15:2]														—	—
Value after reset:	The value set by user														1	1

Bit	Symbol	Bit name	Description	R/W
b1, b0	—	Reserved	These bits are read as 1. When writing to flash, the write value should always be 1.	R
b22 to b2	SECMPUE2[22:2]	Region End Address	Address where the region ends, for use in region determination.	R
b29 to b23	—	Reserved	These bits are read as 0. When writing to flash, the write value should always be 0.	R
b30	—	Reserved	This bit is read as 1. When writing to flash, the write value should always be 1.	R

16.6.1.7 安全MPU区域2起始地址寄存器(SECMPUS2)

Address(es): SECMPUS2 0000 0428h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	SECMPUS2[22:16]						
重置后的值：	0	1	0	0	0	0	0	0	0	用户设置的值						

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SECMPUS2[15:2]														—	—
重置后的值：	用户设置的值														0	0

Bit	Symbol	位名称	Description	R/W
b1, b0	—	Reserved	这些位被读取为0。写入闪存时，写入值应始终为0。	R
b22 to b2	SECMPUS2[22:2]	区域起始地址	区域起始地址，用于区域确定	R
b29 to b23	—	Reserved	这些位被读取为0。写入闪存时，写入值应始终为0。	R
b30	—	Reserved	该位读为1。写入闪存时，写入值应始终为1。	R
b31	—	Reserved	该位读为0。写入flash时，写入值应始终为0。	R

SECMPUS2和SECMPUE2寄存器指定安全功能1的安全区域（400C0000到400DFFFFh和40100000到407FFFFFh）。只能从SECMPUPCSn和SECMPPCEn设置的安全程序访问安全区域。

SECMPUS2寄存器指定区域开始的起始地址。

16.6.1.8 安全MPU区域2结束地址寄存器(SECMPUE2)

Address(es): SECMPUE2 0000 042Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	SECMPUE2[22:16]						
重置后的值：	0	1	0	0	0	0	0	0	0	用户设置的值						

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SECMPUE2[15:2]														—	—
重置后的值：	用户设置的值														1	1

Bit	Symbol	位名称	Description	R/W
b1, b0	—	Reserved	这些位读取为1。写入闪存时，写入值应始终为1。	R
b22 to b2	SECMPUE2[22:2]	区域结束地址	区域结束的地址，用于区域确定。	R
b29 to b23	—	Reserved	这些位被读取为0。写入闪存时，写入值应始终为0。	R
b30	—	Reserved	该位读为1。写入闪存时，写入值应始终为1。	R

Bit	Symbol	Bit name	Description	R/W
b31	—	Reserved	This bit is read as 0. When writing to flash, the write value should always be 0.	R

The SECMPUS2 and SECMPUE2 registers specify the secure region for security function 1 (400C 0000 to 400D FFFFh and 4010 0000 to 407F FFFFh). The memory space defined in the SECMPUS2 and SECMPUE2 registers can only be accessed from the secure program set up in the SECMPUPCSn and SECMPUPCEn registers.

The SECMPUE2 register specifies the end address where the region ends.

16.6.1.9 Security MPU Region 3 Start Address Register (SECMPUS3)

Address(es): SECMPUS3 0000 0430h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	SECMPUS3[22:16]						
Value after reset:	0	1	0	0	0	0	0	0	0	The value set by user						

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SECMPUS3[15:2]														—	—
Value after reset:	The value set by user														0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	—	Reserved	These bits are read as 0. When writing to flash, the write value should always be 0.	R
b22 to b2	SECMPUS3[22:2]	Region Start Address	Address where the region starts, for use in region determination.	R
b29 to b23	—	Reserved	These bits are read as 0. When writing to flash, the write value should always be 0.	R
b30	—	Reserved	This bit is read as 1. When writing to flash, the write value should always be 1.	R
b31	—	Reserved	This bit is read as 0. When writing to flash, the write value should always be 0.	R

The SECMPUS3 and SECMPUE3 registers specify the secure region for security function 2 (400C 0000h to 400D FFFFh and 4010 0000h to 407F FFFFh). The secure region can be accessed only from the secure program set up by SECMPUPCSn and SECMPUPCEn.

The SECMPUS3 register specifies the start address where the region starts.

Bit	Symbol	位名称	Description	R/W
b31	—	Reserved	该位读为0。写入flash时，写入值应始终为0。	R

SECMPUS2和SECMPUE2寄存器指定安全功能1的安全区域（400C0000到400DFFFFh和40100000到407FFFFFh）。SECMPUS2和SECMPUE2寄存器中定义的存储空间只能从SECMPUPCSn和SECMPPCEn寄存器中设置的安全程序访问。

SECMPUE2寄存器指定区域结束的结束地址。

16.6.1.9 安全MPU区域3起始地址寄存器(SECMPUS3)

Address(es): SECMPUS3 0000 0430h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	SECMPUS3[22:16]						
重置后的值:	0	1	0	0	0	0	0	0	0	用户设置的值						

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SECMPUS3[15:2]														—	—
重置后的值:	用户设置的值														0	0

Bit	Symbol	位名称	Description	R/W
b1, b0	—	Reserved	这些位被读取为0。写入闪存时，写入值应始终为0。	R
b22 to b2	SECMPUS3[22:2]	区域起始地址	区域开始的地址，用于区域确定。	R
b29 to b23	—	Reserved	这些位被读取为0。写入闪存时，写入值应始终为0。	R
b30	—	Reserved	该位读为1。写入闪存时，写入值应始终为1。	R
b31	—	Reserved	该位读为0。写入flash时，写入值应始终为0。	R

SECMPUS3和SECMPUE3寄存器指定安全功能2的安全区域（400C0000h到400DFFFFh和40100000h到407FFFFFh）。安全区域只能从由设置的安全程序访问
SECMPUPCSn and SECMPUPCEn.

SECMPUS3寄存器指定区域开始的起始地址。

16.6.1.10 Security MPU Region 3 End Address Register (SECMPUE3)

Address(es): SECMPUE3 0000 0434h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	SECMPUE3[22:16]						
Value after reset:	0	1	0	0	0	0	0	0	0	The value set by user						

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SECMPUE3[15:2]														—	—
Value after reset:	The value set by user														1	1

Bit	Symbol	Bit name	Description	R/W
b1, b0	—	Reserved	These bits are read as 1. When writing to flash, the write value should always be 1.	R
b22 to b2	SECMPUE3[22:2]	Region End Address	Address where the region ends, for use in region determination.	R
b29 to b23	—	Reserved	These bits are read as 0. When writing to flash, the write value should always be 0.	R
b30	—	Reserved	This bit is read as 1. When writing to flash, the write value should always be 1.	R
b31	—	Reserved	This bit is read as 0. When writing to flash, the write value should always be 0.	R

The SECMPUS3 and SECMPUE3 registers specify the secure region for security function 2 (400C 0000h to 400D FFFFh and 4010 0000h to 407F FFFFh). The memory space defined in the SECMPUS3 and SECMPUE3 registers can only be accessed from the secure program set up in the SECMPUPCSn and SECMPUPCEn registers.

The SECMPUE3 register specifies the end address where the region ends.

16.6.1.11 Security MPU Access Control Register (SECMPUAC)

Address(es): SECMPUAC 0000 0438h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	DISPC1	DISPC0	—	—	—	—	DIS3	DIS2	DIS1	DIS0
Value after reset:	1	1	1	1	1	1	The value set by user		1	1	1	1	The value set by user			

Bit	Symbol	Bit name	Description	R/W
b0	DIS0	Region 0 Disable	0: Security MPU region 0 is enabled 1: Security MPU region 0 is disabled.	R
b1	DIS1	Region 1 Disable	0: Security MPU region 1 is enabled 1: Security MPU region 1 is disabled.	R
b2	DIS2	Region 2 Disable	0: Security MPU region 2 is enabled 1: Security MPU region 2 is disabled.	R
b3	DIS3	Region 3 Disable	0: Security MPU region 3 is enabled 1: Security MPU region 3 is disabled.	R
b7 to b4	—	Reserved	These bits are read as 1. When writing to flash, the write value should always be 1.	R
b8	DISPC0	PC Region 0 Disable	0: Security MPU PC region 0 is enabled 1: Security MPU PC region 0 is disabled.	R

16.6.1.10 安全MPU区域3结束地址寄存器(SECMPUE3)

Address(es): SECMPUE3 0000 0434h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	SECMPUE3[22:16]						
重置后的值：	0	1	0	0	0	0	0	0	0	用户设置的值						

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SECMPUE3[15:2]														—	—
重置后的值：	用户设置的值														1	1

Bit	Symbol	位名称	Description	R/W
b1, b0	—	Reserved	这些位读取为1。写入闪存时，写入值应始终为1。	R
b22 to b2	SECMPUE3[22:2]	区域结束地址	区域结束的地址，用于区域确定。	R
b29 to b23	—	Reserved	这些位被读取为0。写入闪存时，写入值应始终为0。	R
b30	—	Reserved	该位读为1。写入闪存时，写入值应始终为1。	R
b31	—	Reserved	该位读为0。写入flash时，写入值应始终为0。	R

SECMPUS3和SECMPUE3寄存器指定安全功能2的安全区域（400C0000h到400D FFFFh和40100000h到407FFFFFh）。SECMPUS3和SECMPUE3寄存器中定义的存储空间只能从SECMPUPCSn和SECMPPCEn寄存器中设置的安全程序访问。

SECMPUE3寄存器指定区域结束的结束地址。

16.6.1.11 安全MPU访问控制寄存器(SECPUAC)

Address(es): SECMPUAC 0000 0438h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	DISPC1	DISPC0	—	—	—	—	DIS3	DIS2	DIS1	DIS0
重置后的值：	1	1	1	1	1	1	用户设置的值		1	1	1	1	用户设置的值			

Bit	Symbol	位名称	Description	R/W
b0	DIS0	区域0禁用	0：启用安全MPU区域01：禁用安全MPU区域0。	R
b1	DIS1	区域1禁用	0：启用安全MPU区域11：禁用安全MPU区域1。	R
b2	DIS2	区域2禁用	0：启用安全MPU区域21：禁用安全MPU区域2。	R
b3	DIS3	区域3禁用	0：启用安全MPU区域31：禁用安全MPU区域3。	R
b7 to b4	—	Reserved	这些位读取为1。写入闪存时，写入值应始终为1。	R
b8	DISPC0	PC区域0禁用	0：启用安全MPUPC区域01：禁用安全MPUPC区域0。	R

Bit	Symbol	Bit name	Description	R/W
b9	DISPC1	PC Region 1 Disable	0: Security MPU PC region 1 is enabled 1: Security MPU PC region 1 is disabled.	R
b15 to b10	—	Reserved	These bits are read as 1. When writing to flash, the write value should always be 1.	R

Note: When flash memory is erased, the security MPU is disabled.
To enable and disable the security MPU, see section 16.6.2.1, Memory protection.

DIS0 bit (Region 0 Disable)

DIS0 bit enables or disables security MPU region 0.

If security MPU region 0 is enabled, the code flash region within the limits set up by SECMPUS0 and SECMPUE0 is a secure region.

DIS1 bit (Region 1 Disable)

DIS1 bit enables or disables security MPU region 1.

If security MPU region 1 is enabled, the SRAM region within the limits set up by SECMPUS1 and SECMPUE1 is a secure region.

DIS2 bit (Region 2 Disable)

DIS2 bit enables or disables security MPU region 2.

If security MPU region 2 is enabled, the region within the limits set up by SECMPUS2 and SECMPUE2 is a secure region.

DIS3 bit (Region 3 Disable)

DIS3 bit enables or disables security MPU region 3.

If security MPU region 3 is enabled, the region within the limits set up by SECMPUS3 and SECMPUE3 is a secure region.

DISPC0 bit (PC Region 0 Disable)

DISPC0 bit enables or disables security MPU PC region 0.

If security MPU PC region 0 is enabled, the code flash or SRAM region within the limits set up by SECMPUPCS0 and SECMPUPCE0 is a secure program.

DISPC1 bit (PC Region 1 Disable)

DISPC1 bit enables or disables security MPU PC region 1.

If security MPU PC region 1 is enabled, the code flash or SRAM region within the limits set up by SECMPUPCS1 and SECMPUPCE1 is a secure program.

16.6.2 Operation

16.6.2.1 Memory protection

The security MPU protects the regions (code flash, SRAM, two security function regions) from non-secure program access. If access to the protected region is detected, access becomes invalid.

When the security MPU is enabled, DISPC0 or DISPC1 in the Security MPU Access Control Register (SECMPUAC) must be cleared to 0 and DIS0, DIS1, DIS2, or DIS3 in the Security MPU Access Control Register (SECMPUAC) must be cleared to 0.

When security MPU is disabled, all of bits DISPC0, DISPC1, DIS0, DIS1, DIS2, and DIS3 in the Security MPU Access Control Register (SECMPUAC) must be set to 1.

Other settings of the Security MPU Access Control Register (SECMPUAC) are prohibited.

Bit	Symbol	位名称	Description	R/W
b9	DISPC1	PC区域1禁用	0：启用安全MPUPC区域11：禁用安全MPUPC区域1。	R
b15 to b10	—	Reserved	这些位读取为1。写入闪存时，写入值应始终为1。	R

Note: 当闪存被擦除时，安全MPU被禁用。
要启用和禁用安全MPU，请参阅第16.6.2.1节，内存保护。

DIS0位（区域0禁用）

DIS0位启用或禁用安全MPU区域0。

如果启用安全MPU区域0，则在SECMPUS0和SECMPUE0设置的限制范围内的代码闪存区域是安全区域。

DIS1位（区域1禁用）

DIS1位启用或禁用安全MPU区域1。

如果启用安全MPU区域1，则在SECMPUS1和SECMPUE1设置的限制范围内的SRAM区域是安全区域。

DIS2位（区域2禁用）

DIS2位启用或禁用安全MPU区域2。

如果启用安全MPU区域2，则在SECMPUS2和SECMPUE2设置的限制范围内的区域是安全区域。

DIS3位（区域3禁用）

DIS3位启用或禁用安全MPU区域3。

如果启用安全MPU区域3，则在SECMPUS3和SECMPUE3设置的限制范围内的区域是安全区域。

DISPC0位（PC区域0禁用）

DISPC0位启用或禁用安全MPUPC区域0。

如果启用了安全MPUPC区域0，则代码闪存或SRAM区域在SECMPUPCS0和SECMPUPCE0是一个安全程序。

DISPC1位（PC区域1禁用）

DISPC1位启用或禁用安全MPUPC区域1。

如果启用了安全MPUPC区域1，则代码闪存或SRAM区域在SECMPUPCS1和SECMPUPCE1是一个安全程序。

16.6.2 Operation

16.6.2.1 内存保护

安全MPU保护区域（代码闪存、SRAM、两个安全功能区域）免受非安全程序访问。如果检测到对受保护区域的访问，则访问变为无效。

启用安全MPU时，必须将安全MPU访问控制寄存器(SECMPUAC)中的DISPC0或DISPC1清除为0，并且必须将安全MPU访问控制寄存器(SECMPUAC)中的DIS0、DIS1、DIS2或DIS3清除为0。

禁用安全MPU时，安全MPU访问中的所有位DISPC0、DISPC1、DIS0、DIS1、DIS2和DIS3控制寄存器(SECMPUAC)必须设置为1。

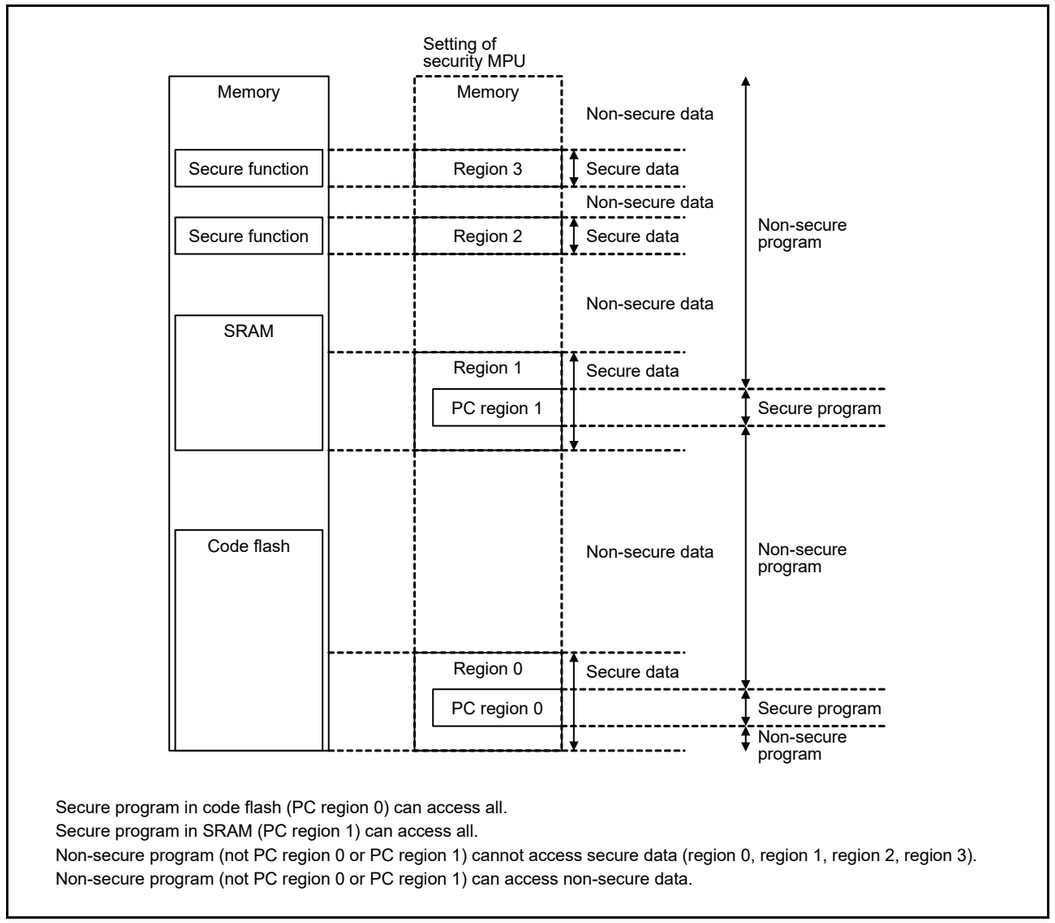
禁止安全MPU访问控制寄存器(SECMPUAC)的其他设置。

The security MPU provides protection of secure regions when:

- Secure data is accessed from a non-secure program
- Secure data is accessed from other than the CPU (DMAC, DTC, EDMAC, GLCDC, DRW, JPEG)
- Secure data is accessed from the debugger.

Secure data can be accessed from a secure program.

Note: Secure program: Code flash or SRAM region within the limits set up by SECMPUPCS0 and SECMPUPCE0.
Code flash or SRAM region within the limits set up by SECMPUPCS1 and SECMPUPCE1.
Non-secure program: All regions without the secure program.
Secure data: Code flash region within the limits set up by SECMPUS0 and SECMPUE0.
SRAM region within the limits set up by SECMPUS1 and SECMPUE1.
Security function region within the limits set up by SECMPUS2 and SECMPUE2.
Security Function region within the limits set up by SECMPUS3 and SECMPUE3.



Secure program in code flash (PC region 0) can access all.
Secure program in SRAM (PC region 1) can access all.
Non-secure program (not PC region 0 or PC region 1) cannot access secure data (region 0, region 1, region 2, region 3).
Non-secure program (not PC region 0 or PC region 1) can access non-secure data.

Figure 16.11 Use case of security MPU

16.6.2.2 Notes on debug

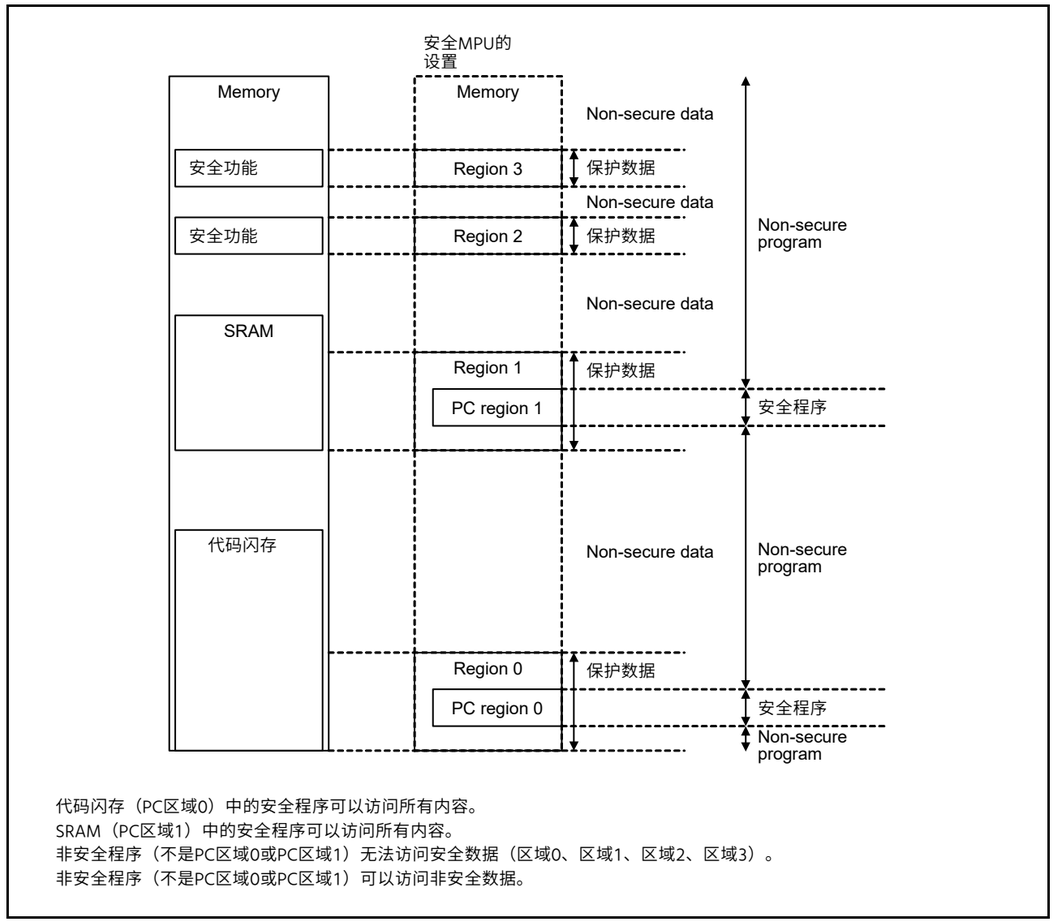
The protected memory cannot be debugged if the security MPU is enable. Disable the security MPU when debugging a security program.

安全MPU在以下情况下提供安全区域保护：

- 从非安全程序访问安全数据
- 从CPU以外的其他地方访问安全数据（DMAC、DTC、EDMAC、GLCDC、DRW、JPEG）
- 从调试器访问安全数据。

可以从安全程序访问安全数据。

Note: Secure program: 在SECMPUPCS0和SECMPUPCE0设置的限制范围内对闪存或SRAM区域进行编码。在SECMPUPCS1和SECMPUPCE1设置的限制范围内对闪存或SRAM区域进行编码。
非安全程序：没有安全程序的所有地区。
Secure data: 在SECMPUS0和SECMPUE0设置的限制范围内编码flash区域。
SRAM区域在SECMPUS1和SECMPUE1设置的范围内。
在SECMPUS2和SECMPUE2设置的限制范围内的安全功能区域。在SECMPUS3和SECMPUE3设置的限制范围内的安全功能区域。



代码闪存（PC区域0）中的安全程序可以访问所有内容。
SRAM（PC区域1）中的安全程序可以访问所有内容。
非安全程序（不是PC区域0或PC区域1）无法访问安全数据（区域0、区域1、区域2、区域3）。
非安全程序（不是PC区域0或PC区域1）可以访问非安全数据。

Figure 16.11 安全MPU用例

16.6.2.2 调试注意事项

如果启用了安全MPU，则无法调试受保护的内存。调试安全程序时关闭安全MPU。

16.7 References

1. *ARM®v7-M Architecture Reference Manual* (ARM DDI 0403D).
2. *ARM® Cortex®-M4 Processor Technical Reference Manual* (ARM DDI 0439D).
3. *ARM® Cortex®-M4 Devices Generic User Guide* (ARM DUI 0553A).

16.7 References

1. ARM®v7-M架构参考手册(ARMDDI0403D)。
2. ARM®Cortex®-M4处理器技术参考手册(ARMDDI0439D)。
3. ARM®Cortex®-M4设备通用用户指南(ARMDUI0553A)。

17. DMA Controller (DMAC)

The 8-channel DMA Controller (DMAC) can transfer data without intervention from the CPU. When a DMA transfer request is generated, the DMAC transfers data stored at the transfer source address to the transfer destination address.

17.1 Overview

Table 17.1 lists the DMAC specifications and Figure 17.1 shows a block diagram.

Table 17.1 DMAC specifications

Parameter		Specifications
Number of channels		8 channels (DMACm, m = 0 to 7)
Transfer space		4 GB (0000 0000h to FFFF FFFFh, excluding reserved areas)
Maximum transfer volume		64M data units (maximum number of transfers in block transfer mode: 1,024 data units × 65,536 blocks)
DMA activation source		Selectable for each channel: • Software trigger • Interrupt requests from peripheral modules or trigger from external interrupt input pins.*1
Channel priority		Channel 0 > Channel 1 > Channel 2 > Channel 3... > Channel 7 (Channel 0: highest)
Transfer data	Single data	Bit length: 8, 16, 32 bits
	Block size	Number of data: 1 to 1,024
Transfer mode	Normal transfer mode	• One data transfer by one DMA transfer request • Selectable free running mode (total number of data transfers is not specified).
	Repeat transfer mode	• One data transfer by one DMA transfer request • Program returns to the transfer start address on completion of the repeat size of data transfer specified for the transfer source or destination • Maximum settable repeat size: 1,024.
	Block transfer mode	• One data block transfer by one DMA transfer request • Maximum settable block size: 1,024 data.
Selective functions	Extended repeat area function	• Allows data to be transferred by repeating the address values in the specified range, with the upper bit values in the transfer address register remaining fixed • Area of 2 bytes to 128 MB individually selectable as the extended repeat area for transfer source and destination.
Interrupt request (DMACm_INT)	Transfer end interrupt	Generated on completion of transferring data volume specified in the transfer counter
	Transfer escape end interrupt	Generated when: • The repeat size of data transfer is complete • The source address of the extended repeat area overflows • The destination address of the extended repeat area overflows.
Event link activation (DMACm_INT)		An event link request is generated after each data transfer (for block transfer, after each block is transferred)
Module-stop function		Module-stop state can be set to reduce power consumption

Note 1. For details on DMAC activation sources, see Table 14.3, Interrupt vector table, in section 14, Interrupt Controller Unit (ICU).

17. DMA Controller (DMAC)

8通道DMA控制器(DMAC)无需CPU干预即可传输数据。当产生DMA传输请求时，DMAC将存储在传输源地址的数据传输到传输目标地址。

17.1 Overview

表17.1列出了DMAC规范，图17.1显示了框图。

Table 17.1 DMAC specifications

Parameter		Specifications
通道数		8个通道（DMACm，m=0到7）
转移空间		4GB（00000000h到FFFFFFFFh，不包括保留区域）
最大传输量		64M数据单元（块传输模式下的最大传输数：1 024个数据单元×65 536个块）
DMA激活源		每个通道可选择： 软件触发 来自外围模块的中断请求或来自外部中断输入引脚的触发。*1
通道优先级		Channel 0 > Channel 1 > Channel 2 > Channel 3... > Channel 7 (Channel 0: highest)
传输数据	单一数据	位长：8、16、32位
	块大小	数据数量：1至1 024
传输模式	正常传输模式	一个DMA传输请求传输一个数据 可选择的自由运行模式（未指定数据传输的总数）。
	重复传输模式	通过一个DMA传输请求进行一次数据传输 完成为传输源或目标指定的重复数据传输大小后，程序返回传输起始地址 最大可设置重复大小：1 024。
	块传输模式	一个DMA传输请求传输一个数据块 最大可设置块大小：1 024个数据。
选择性功能	扩展重复区域功能	允许通过重复指定范围内的地址值来传输数据，传输地址寄存器中的高位值保持固定。 2字节到128MB的区域可以单独选择作为传输源和目标的扩展重复区域。
中断请求(DMACm_INT)	传输结束中断	在传输计数器中指定的传输数据量完成时生成
	传输转义结束中断	在以下情况下生成： 数据传输的重复大小已完成 扩展重复区域的源地址溢出 扩展重复区域的目标地址溢出。
事件链接激活(DMACm_INT)		每次数据传输后都会产生一个事件链接请求（对于块传输，在每个块传输后）
Module-stop function		可设置模块停止状态以降低功耗

Note 1. 有关DMAC激活源的详细信息，请参见第14节，中断控制器单元(ICU)中的表14.3，中断向量表。

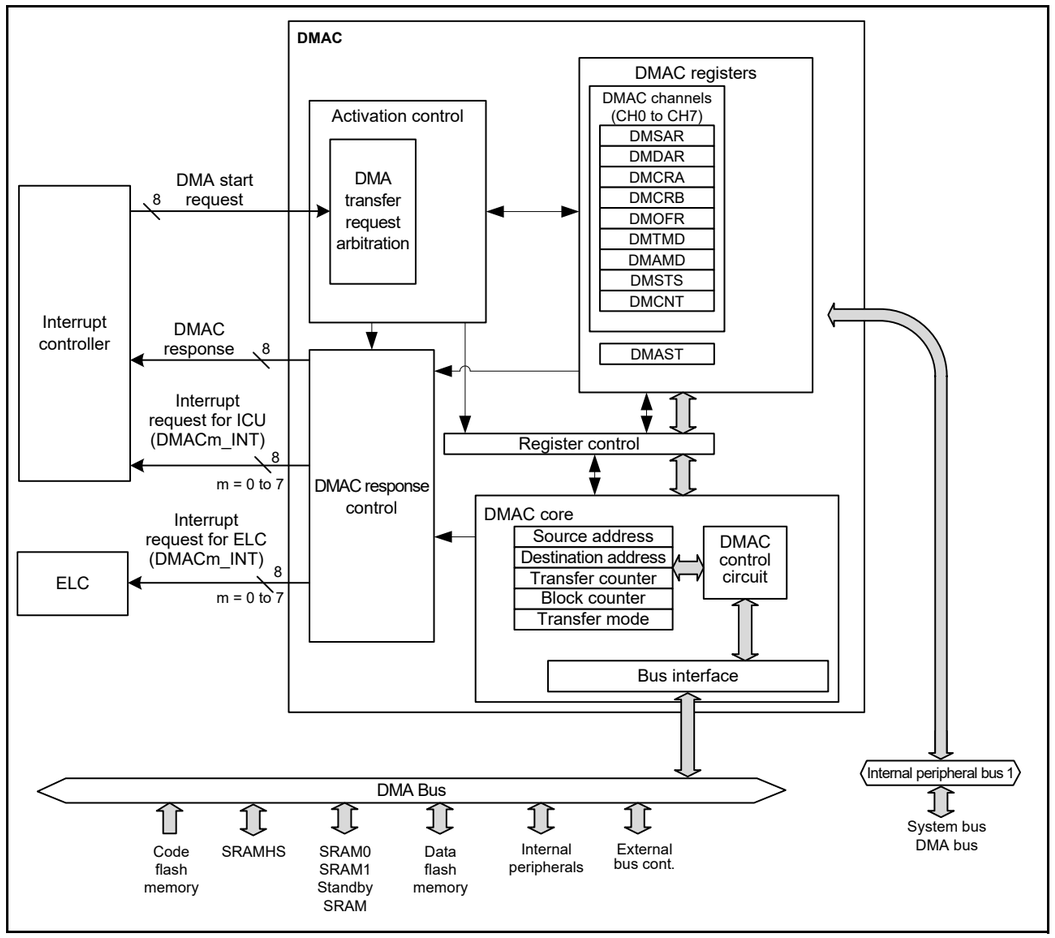


Figure 17.1 DMAC block diagram

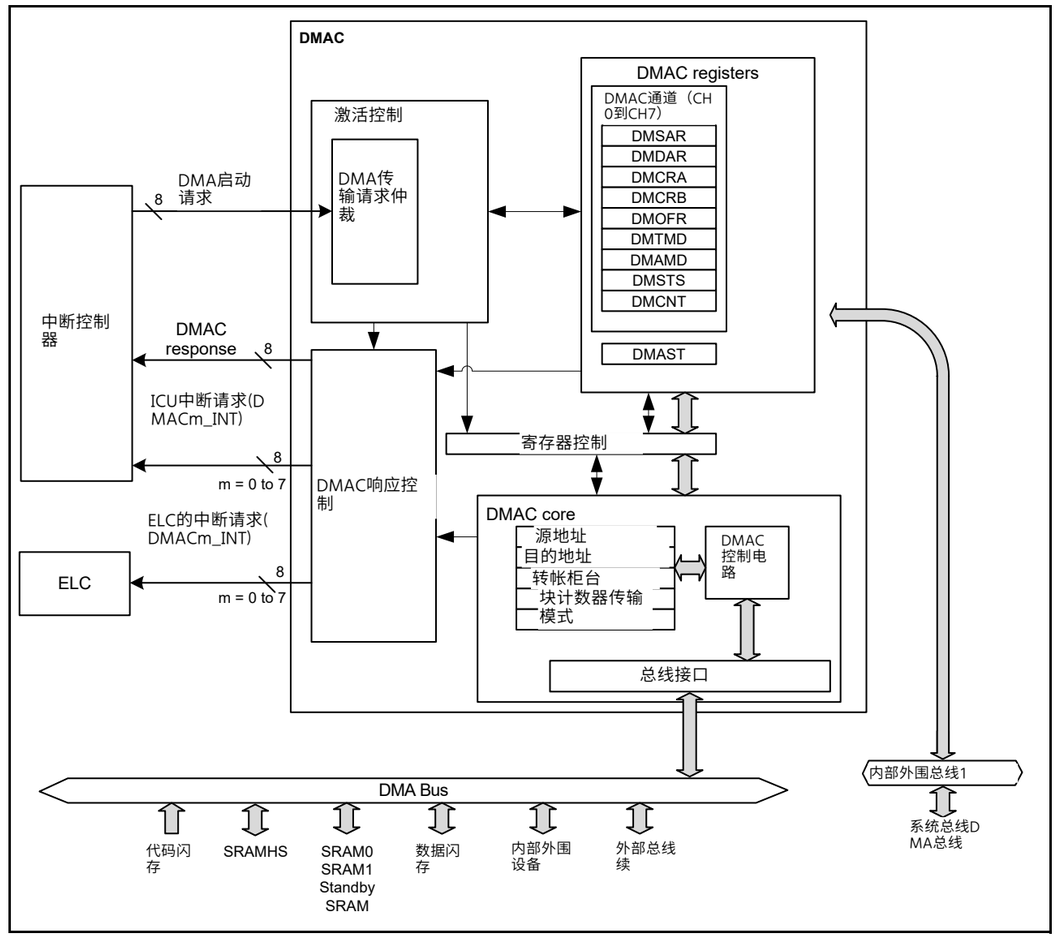


Figure 17.1 DMAC框图

17.2 Register Descriptions

17.2.1 DMA Source Address Register (DMSAR)

Address(es): DMAC0.DMSAR 4000 5000h, DMAC1.DMSAR 4000 5040h, DMAC2.DMSAR 4000 5080h, DMAC3.DMSAR 4000 50C0h, DMAC4.DMSAR 4000 5100h, DMAC5.DMSAR 4000 5140h, DMAC6.DMSAR 4000 5180h, DMAC7.DMSAR 4000 51C0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Description	Setting range	R/W
b31 to b0	Specifies the transfer source start address	0000 0000h to FFFF FFFFh (4 GB)	R/W

Set DMSAR while DMAC activation is disabled (the DMST bit in DMAST = 0) or DMA transfer is disabled (the DTE bit in DMCNT = 0).

Note: Address alignment in this register must match the transfer data size value selected in the SZ bit in DMTMD.

17.2.2 DMA Destination Address Register (DMDAR)

Address(es): DMAC0.DMDAR 4000 5004h, DMAC1.DMDAR 4000 5044h, DMAC2.DMDAR 4000 5084h, DMAC3.DMDAR 4000 50C4h, DMAC4.DMDAR 4000 5104h, DMAC5.DMDAR 4000 5144h, DMAC6.DMDAR 4000 5184h, DMAC7.DMDAR 4000 51C4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Description	Setting range	R/W
b31 to b0	Specifies the transfer destination start address	0000 0000h to FFFF FFFFh (4 GB)	R/W

Set DMDAR while DMAC activation is disabled (the DMST bit in DMAST = 0) or DMA transfer is disabled (the DTE bit in DMCNT = 0).

Note: Address alignment in this register must match the transfer data size value selected in the SZ bit in DMTMD.

17.2 注册说明

17.2.1 DMA源地址寄存器(DMSAR)

Address(es): DMAC0.DMSAR 4000 5000h, DMAC1.DMSAR 4000 5040h, DMAC2.DMSAR 4000 5080h, DMAC3.DMSAR 4000 50C0h, DMAC4.DMSAR 4000 5100h, DMAC5.DMSAR 4000 5140h, DMAC6.DMSAR 4000 5180h, DMAC7.DMSAR 4000 51C0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Description	设定范围	R/W
b31 to b0	指定传输源起始地址	0000 0000h to FFFF FFFFh (4 GB)	R/W

在禁用DMAC激活（DMAST中的DMST位=0）或禁用DMA传输（DMCNT中的DTE位=0）时设置DMSAR。

Note: 该寄存器中的地址对齐必须与在DMTMD的SZ位中选择的传输数据大小值相匹配。

17.2.2 DMA目标地址寄存器(DMDAR)

Address(es): DMAC0.DMDAR 4000 5004h, DMAC1.DMDAR 4000 5044h, DMAC2.DMDAR 4000 5084h, DMAC3.DMDAR 4000 50C4h, DMAC4.DMDAR 4000 5104h, DMAC5.DMDAR 4000 5144h, DMAC6.DMDAR 4000 5184h, DMAC7.DMDAR 4000 51C4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Description	设定范围	R/W
b31 to b0	指定传输目标起始地址	0000 0000h to FFFF FFFFh (4 GB)	R/W

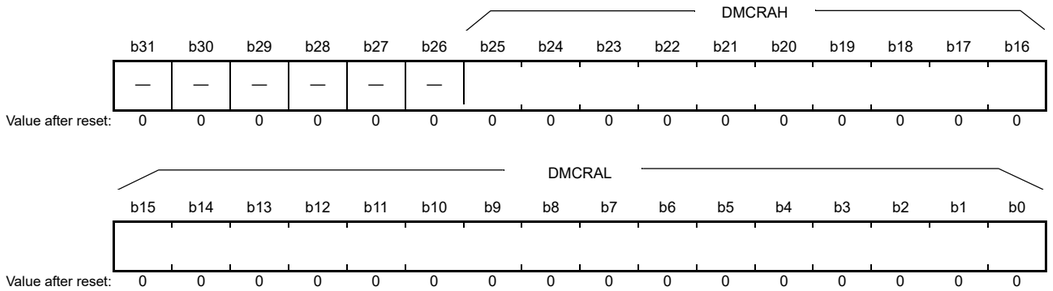
在禁用DMAC激活（DMAST中的DMST位=0）或禁用DMA传输（DMCNT中的DTE位=0）时设置DMDAR。

Note: 该寄存器中的地址对齐必须与在DMTMD的SZ位中选择的传输数据大小值相匹配。

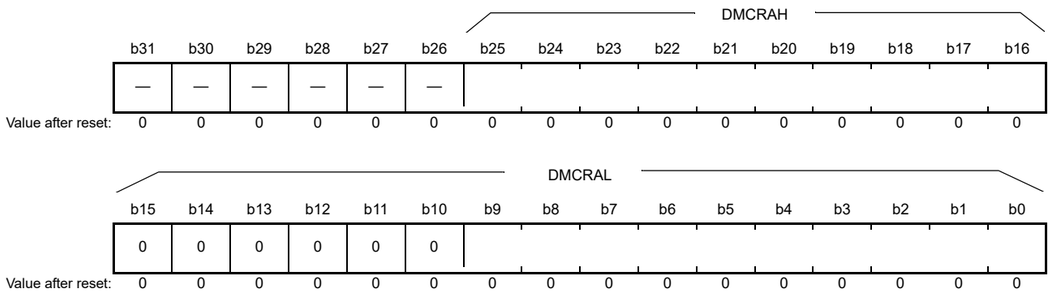
17.2.3 DMA Transfer Count Register (DMCRA)

Address(es): DMAC0.DMCRA 4000 5008h, DMAC1.DMCRA 4000 5048h, DMAC2.DMCRA 4000 5088h, DMAC3.DMCRA 4000 50C8h
DMAC4.DMCRA 4000 5108h, DMAC5.DMCRA 4000 5148h, DMAC6.DMCRA 4000 5188h, DMAC7.DMCRA 4000 51C8h

- Normal transfer mode



- Repeat transfer mode, block transfer mode



Symbol	Bit name	Description	R/W
DMCRAL	Lower bits of transfer count	Specifies the number of transfer operations	R/W
DMCRAH	Upper bits of transfer count		R/W

Note: In repeat and block transfer modes, set the same value for DMCRAH and DMCRAL.

(1) Normal transfer mode (MD[1:0] bits in DMACm.DMTMD = 00b)

In normal transfer mode, DMCRAL functions as a 16-bit transfer counter. The number of transfer operations is one when the setting is 0001h, and 65,535 when it is FFFFh. The value is decremented by one each time data is transferred.

A setting of 0000h indicates an unspecified number of transfer operations. Data transfer is performed with the transfer counter stopped, that is, in free running mode.

Do not use DMCRAH in normal transfer mode. Write 0000h to DMCRAH.

(2) Repeat transfer mode (MD[1:0] bits in DMACm.DMTMD = 01b)

In repeat transfer mode, DMCRAH specifies the repeat size and DMCRAL functions as a 10-bit transfer counter. The number of transfer operations is one when the setting is 001h, 1,023 when it is 3FFh, and 1,024 when it is 000h. In this mode, a value in the range of 000h to 3FFh (1 to 1,024) can be set for DMCRAH and DMCRAL.

Setting bits 15 to 10 in DMCRAL is invalid. Write 0 to these bits. The value in DMCRAL is decremented by one each time data is transferred until it reaches 000h, at which time the value in DMCRAH is loaded into DMCRAL.

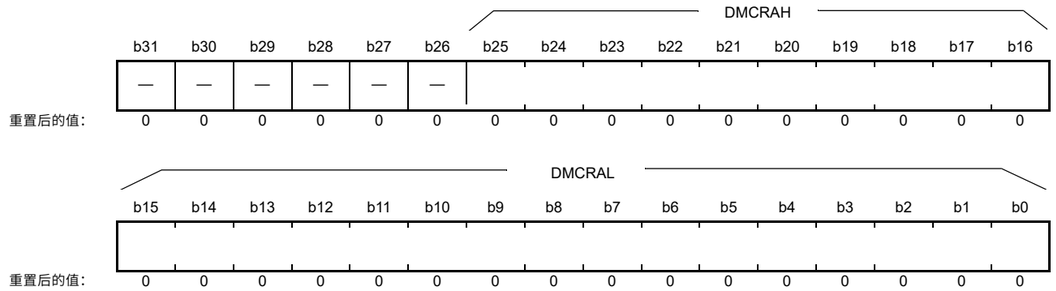
(3) Block transfer mode (MD[1:0] bits in DMACm.DMTMD = 10b)

In block transfer mode, DMCRAH specifies the block size and DMCRAL functions as a 10-bit block size counter. The

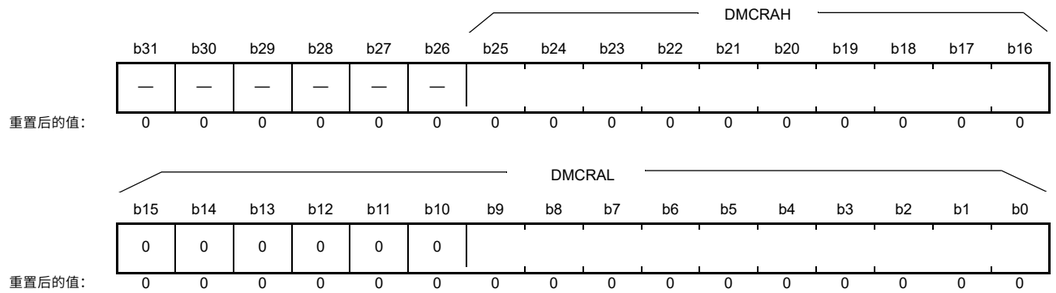
17.2.3 DMA传输计数寄存器(DMCRA)

Address(es): DMAC0.DMCRA 4000 5008h, DMAC1.DMCRA 4000 5048h, DMAC2.DMCRA 4000 5088h, DMAC3.DMCRA 4000 50C8h
DMAC4.DMCRA 4000 5108h, DMAC5.DMCRA 4000 5148h, DMAC6.DMCRA 4000 5188h, DMAC7.DMCRA 4000 51C8h

正常传输模式



重复传输模式、块传输模式



Symbol	位名称	Description	R/W
DMCRAL	传输计数的低位	指定传输操作的次数	R/W
DMCRAH	传输计数的高位		R/W

Note: 在重复和块传输模式下，为DMCRAH和DMCRAL设置相同的值。

(1) 正常传输模式（DMACm.DMTMD=00b中的MD[1:0]位）

在正常传输模式下，DMCRAL用作16位传输计数器。设置为0001h时传输操作数为1，设置为FFFFh时为65 535。每次传输数据时，该值减一。

设置为0000h表示未指定数量的传输操作。数据传输是在传输计数器停止的情况下执行的，即在自由运行模式下。

不要在正常传输模式下使用DMCRAH。将0000h写入DMCRAH。

(2) 重复传输模式（DMACm.DMTMD=01b中的MD[1:0]位）

在重复传输模式下，DMCRAH指定重复大小，DMCRAL用作10位传输计数器。设置为001h时传输操作数为1，设置为3FFh时为1 023，设置为000h时为1 024。在此模式下，可以为DMCRAH和DMCRAL设置000h到3FFh（1到1 024）范围内的值。

在DMCRAL中设置位15至10无效。将0写入这些位。每次传输数据时，DMCRAL中的值减1，直到到达000h，此时DMCRAH中的值被加载到DMCRAL中。

(3) 块传输模式（DMACm.DMTMD=10b中的MD[1:0]位）

在块传输模式下，DMCRAH指定块大小，DMCRAL用作10位块大小计数器。这

block size is one when the setting is 001h, 1,023 when it is 3FFh, and 1,024 when it is 000h. In this mode, a value in the range of 000h to 3FFh can be set for DMCRAH and DMCRAL.

Setting bits 15 to 10 in DMCRAL is invalid. Write 0 to these bits. The value in DMCRAL is decremented by one each time data is transferred until it reaches 000h, at which time the value in DMCRAH is loaded into DMCRAL.

17.2.4 DMA Block Transfer Count Register (DMCRB)

Address(es): DMAC0.DMCRB 4000 500Ch, DMAC1.DMCRB 4000 504Ch, DMAC2.DMCRB 4000 508Ch, DMAC3.DMCRB 4000 50CCh, DMAC4.DMCRB 4000 510Ch, DMAC5.DMCRB 4000 514Ch, DMAC6.DMCRB 4000 518Ch, DMAC7.DMCRB 4000 51CCh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Description	Setting range	R/W
b15 to b0	Specifies the number of block or repeat transfer operations	0001h to FFFFh (1 to 65,535) 0000h (65,536).	R/W

DMCRB specifies the number of operations in block and repeat transfer modes. The number of transfer operations is one when the setting is 0001h, 65,535 when it is FFFFh, and 65,536 when it is 0000h.

In repeat transfer mode, the value is decremented by one when the final data of one repeat size is transferred. In block transfer mode, the value is decremented by one when the final data of one block size is transferred. Do not use DMCRB in normal transfer mode as the setting is invalid.

17.2.5 DMA Transfer Mode Register (DMTMD)

Address(es): DMAC0.DMTMD 4000 5010h, DMAC1.DMTMD 4000 5050h, DMAC2.DMTMD 4000 5090h, DMAC3.DMTMD 4000 50D0h, DMAC4.DMTMD 4000 5110h, DMAC5.DMTMD 4000 5150h, DMAC6.DMTMD 4000 5190h, DMAC7.DMTMD 4000 51D0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MD[1:0]		DTS[1:0]		—	—	SZ[1:0]		—	—	—	—	—	—	DCTG[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	DCTG[1:0]	Transfer Request Source Select	b1 b0 0 0: Software 0 1: Interrupts*1 from peripheral modules or external interrupt input pins 1 0: Setting prohibited 1 1: Setting prohibited.	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b9, b8	SZ[1:0]	Transfer Data Size Select	b9 b8 0 0: 8 bits 0 1: 16 bits 1 0: 32 bits 1 1: Setting prohibited.	R/W
b11, b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b13, b12	DTS[1:0]	Repeat Area Select	b13 b12 0 0: Specify destination as the repeat area or block area 0 1: Specify source as the repeat area or block area 1 0: Do not specify repeat area or block area 1 1: Setting prohibited.	R/W

当设置为001h时块大小为1，设置为3FFh时为1 023，设置为000h时为1 024。在此模式下，可以为DMCRAH和DMCRAL设置000h到3FFh范围内的值。

在DMCRAL中设置位15至10无效。将0写入这些位。每次传输数据时，DMCRAL中的值减1，直到到达000h，此时DMCRAH中的值被加载到DMCRAL中。

17.2.4 DMA块传输计数寄存器(DMRCB)

Address(es): DMAC0.DMCRB 4000 500Ch, DMAC1.DMCRB 4000 504Ch, DMAC2.DMCRB 4000 508Ch, DMAC3.DMCRB 4000 50CCh, DMAC4.DMCRB 4000 510Ch, DMAC5.DMCRB 4000 514Ch, DMAC6.DMCRB 4000 518Ch, DMAC7.DMCRB 4000 51CCh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Description	设定范围	R/W
b15 to b0	指定块或重复传输操作的数量	0001h to FFFFh (1 to 65,535) 0000h (65,536).	R/W

DMCRB指定块和重复传输模式中的操作数。设置为0001h时传输操作数为1，设置为FFFFh时为65 535，设置为0000h时为65 536。

在重复传输模式下，当传输一个重复大小的最终数据时，该值减一。在块传输模式下，当传输一个块大小的最终数据时，该值减一。请勿在正常传输模式下使用DMCRB，因为该设置无效。

17.2.5 DMA传输模式寄存器(DMTMD)

Address(es): DMAC0.DMTMD 4000 5010h, DMAC1.DMTMD 4000 5050h, DMAC2.DMTMD 4000 5090h, DMAC3.DMTMD 4000 50D0h, DMAC4.DMTMD 4000 5110h, DMAC5.DMTMD 4000 5150h, DMAC6.DMTMD 4000 5190h, DMAC7.DMTMD 4000 51D0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MD[1:0]		DTS[1:0]		—	—	SZ[1:0]		—	—	—	—	—	—	DCTG[1:0]	
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b1, b0	DCTG[1:0]	转移要求 来源选择	b1b000：软件01：来自外围模块或外部中断输入引脚的中断*110：禁止设置11：禁止设置。	R/W
b7 to b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b9, b8	SZ[1:0]	传输数据大小 Select	b9b800：8位01：16位 10：32位11：禁止设置 。	R/W
b11, b10	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b13, b12	DTS[1:0]	重复区域选择	b13b1200：指定目标为重复区域或块区域01：指定源为重复区域或块区域10：不指定重复区域或块区域11：禁止设置。	R/W

Bit	Symbol	Bit name	Description	R/W
b15, b14	MD[1:0]	Transfer Mode Select	b15 b14 0 0: Normal transfer 0 1: Repeat transfer 1 0: Block transfer 1 1: Setting prohibited.	R/W

Note 1. To select the DMAC activation source, use the DELSRn registers of the ICU. For details on DMAC activation sources, see Table 14.4, Event table in section 14, Interrupt Controller Unit (ICU).

DTS[1:0] bits (Repeat Area Select)

The DTS[1:0] bits select either the source or destination as the repeat area in repeat transfer mode and the block area in block transfer mode. In normal transfer mode, these bit settings are invalid.

17.2.6 DMA Interrupt Setting Register (DMINT)

Address(es): DMAC0.DMINT 4000 5013h, DMAC1.DMINT 4000 5053h, DMAC2.DMINT 4000 5093h, DMAC3.DMINT 4000 50D3h, DMAC4.DMINT 4000 5113h, DMAC5.DMINT 4000 5153h, DMAC6.DMINT 4000 5193h, DMAC7.DMINT 4000 51D3h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	DTIE	ESIE	RPTIE	SARIE	DARIE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	DARIE	Destination Address Extended Repeat Area Overflow Interrupt Enable	0: Disable 1: Enable.	R/W
b1	SARIE	Source Address Extended Repeat Area Overflow Interrupt Enable	0: Disable 1: Enable.	R/W
b2	RPTIE	Repeat Size End Interrupt Enable	0: Disable 1: Enable.	R/W
b3	ESIE	Transfer Escape End Interrupt Enable	0: Disable 1: Enable.	R/W
b4	DTIE	Transfer End Interrupt Enable	0: Disable 1: Enable.	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

DARIE bit (Destination Address Extended Repeat Area Overflow Interrupt Enable)

When an extended repeat area overflow occurs on the destination address while the DARIE bit is set to 1, the DTE bit in DMCNT clears to 0. At the same time, the ESIF flag in DMSTS is set to 1 to indicate an interrupt request triggered by an extended repeat area overflow on the destination address.

When block transfer mode is used with the extended repeat area function, an interrupt occurs after completion of a 1-block size transfer. When the DTE bit is set to 1 in DMACm.DMCNT of the channel associated with the stopped transfer, the transfer resumes from the state it was in when the transfer stopped.

When the extended repeat area is not specified for the destination address, this bit is ignored.

SARIE bit (Source Address Extended Repeat Area Overflow Interrupt Enable)

When an extended repeat area overflow occurs on the source address while the SARIE bit is set to 1, the DTE bit in DMCNT clears to 0. At the same time, the ESIF flag in DMSTS is set to 1 to indicate an interrupt request triggered by an extended repeat area overflow on the source address.

When block transfer mode is used with the extended repeat area function, an interrupt occurs after completion of a 1-block size transfer. When the DTE bit is set to 1 in DMACm.DMCNT of the channel associated with the stopped transfer, the transfer resumes from the state it was in when the transfer stopped.

When the extended repeat area is not specified for the source address, this bit is ignored.

Bit	Symbol	位名称	Description	R/W
b15, b14	MD[1:0]	传输模式选择	b15b1400：正常传送0 1：重复传送10：块传 送11：禁止设置。	R/W

Note 1. 要选择DMAC激活源，请使用ICU的DELSRn寄存器。有关DMAC激活源的详细信息，请参阅表14.4，第14节中的事件表，中断控制器单元(ICU)。

DTS[1:0]位（重复区域选择）

DTS[1:0]位在重复传输模式中选择源或目标作为重复区域，在块传输模式中选择块区域。在正常传输模式下，这些位设置无效。

17.2.6 DMA中断设置寄存器(DMINT)

Address(es): DMAC0.DMINT 4000 5013h, DMAC1.DMINT 4000 5053h, DMAC2.DMINT 4000 5093h, DMAC3.DMINT 4000 50D3h, DMAC4.DMINT 4000 5113h, DMAC5.DMINT 4000 5153h, DMAC6.DMINT 4000 5193h, DMAC7.DMINT 4000 51D3h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	DTIE	ESIE	RPTIE	SARIE	DARIE
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	DARIE	目标地址扩展重复区域 溢出中断使能	0：禁用1 ：启用。	R/W
b1	SARIE	源地址扩展重复区 溢出中断使能	0：禁用1 ：启用。	R/W
b2	RPTIE	重复大小结束中断使能	0：禁用1 ：启用。	R/W
b3	ESIE	传输转义结束中断使能	0：禁用1 ：启用。	R/W
b4	DTIE	传输结束中断使能	0：禁用1 ：启用。	R/W
b7 to b5	—	Reserved	这些位被读取为0。写入值应为0。	R/W

DARIE位（目标地址扩展重复区域溢出中断使能）

当DARIE位设置为1时目标地址发生扩展重复区域溢出时，DMCNT中的DTE位清为0。同时，DMSTS中的ESIF标志位设置为1，表示由目标地址上的扩展重复区域溢出。

当块传输模式与扩展重复区域功能一起使用时，在完成1块大小的传输后会发生中断。当与停止传输关联的通道的DMACm.DMCNT中的DTE位设置为1时，传输将从传输停止时的状态恢复。

当没有为目标地址指定扩展重复区域时，该位被忽略。

SARIE位（源地址扩展重复区溢出中断使能）

当SARIE位设置为1时源地址发生扩展重复区域溢出时，DTE位
DMCNT清零。同时，DMSTS中的ESIF标志置1，表示源地址上的扩展重复区溢出触发的中断请求。

当块传输模式与扩展重复区域功能一起使用时，在完成1块大小的传输后会发生中断。当与停止传输关联的通道的DMACm.DMCNT中的DTE位设置为1时，传输将从传输停止时的状态恢复。

当源地址没有指定扩展重复区域时，该位被忽略。

RPTIE bit (Repeat Size End Interrupt Enable)

When the RPTIE bit is set to 1 in repeat transfer mode, the DTE bit in DMCNT clears to 0 after completion of a 1-repeat size data transfer. At the same time, the ESIF flag in DMSTS is set to 1 to indicate that the repeat size end interrupt request occurred. The repeat size end interrupt request can be generated even when the DTS[1:0] bits in DMTMD are 10b (repeat area or block area is not specified).

When the RPTIE bit is set to 1 in block transfer mode, the DTE bit in DMCNT clears to 0 after completion of a 1-block data transfer in the same way as repeat transfer mode. At the same time, the ESIF flag in DMSTS is set to 1 to indicate that the repeat size end interrupt request occurred. The repeat size end interrupt request can be generated even when the DTS[1:0] bits in DMTMD are 10b (repeat area or block area is not specified).

ESIE bit (Transfer Escape End Interrupt Enable)

The ESIE bit enables the transfer escape end interrupt requests (repeat size end interrupt request and extended repeat area overflow interrupt request) that occur during DMA transfer. The interrupt occurs when this bit is 1 and the ESIF flag in DMSTS is set to 1. To clear the transfer escape end interrupt, clear this bit or the ESIF flag in DMSTS to 0.

DTIE bit (Transfer End Interrupt Enable)

The DTIE bit enables the transfer end interrupt request that occurs on completion of a specified number of data transfers. The interrupt occurs when this bit is 1 and the DTIF flag in DMSTS is set to 1. To clear the transfer end interrupt, clear this bit or the DTIF flag in DMSTS to 0.

17.2.7 DMA Address Mode Register (DMAMD)

Address(es): DMAC0.DMAMD 4000 5014h, DMAC1.DMAMD 4000 5054h, DMAC2.DMAMD 4000 5094h, DMAC3.DMAMD 4000 50D4h, DMAC4.DMAMD 4000 5114h, DMAC5.DMAMD 4000 5154h, DMAC6.DMAMD 4000 5194h, DMAC7.DMAMD 4000 51D4h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SM[1:0]		—	SARA[4:0]					DM[1:0]		—	DARA[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b4 to b0	DARA[4:0]	Destination Address Extended Repeat Area	Specifies the extended repeat area on the destination address. For details on the settings, see Table 17.2.	R/W
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b7, b6	DM[1:0]	Destination Address Update Mode	b7 b6 0 0: Fixed address 0 1: Offset addition 1 0: Incremented address 1 1: Decremented address.	R/W
b12 to b8	SARA[4:0]	Source Address Extended Repeat Area	Specifies the extended repeat area on the source address. For details on the settings, see Table 17.2.	R/W
b13	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b15, b14	SM[1:0]	Source Address Update Mode	b15 b14 0 0: Fixed address 0 1: Offset addition 1 0: Incremented address 1 1: Decremented address.	R/W

DARA[4:0] bits (Destination Address Extended Repeat Area)

The DARA[4:0] bits specify the extended repeat area on the destination address. The extended repeat area function is realized through an update of the specified lower address bits with the remaining upper address bits fixed. The size of the extended repeat area can be any power of two between 2 bytes and 128 MB.

The start address of the extended repeat area is set when the lower address overflows the extended repeat area on an address increment. Similarly, the end address of the extended repeat area is set when the lower address underflows the extended repeat area on an address decrement.

RPTIE位（重复大小结束中断使能）

当RPTIE位在重复传输模式下设置为1时，DMCNT中的DTE位在完成1次重复大小的数据传输后清为0。同时，DMSTS中的ESIF标志设置为1，表示发生了重复大小结束中断请求。即使DMTMD中的DTS[1:0]位为10b（未指定重复区域或块区域），也可以产生重复大小结束中断请求。

当RPTIE位在块传输模式下设置为1时，DMCNT中的DTE位在完成1块数据传输后清零，方法与重复传输模式相同。同时，DMSTS中的ESIF标志设置为1，表示发生了重复大小结束中断请求。即使DMTMD中的DTS[1:0]位为10b（未指定重复区域或块区域），也可以产生重复大小结束中断请求。

ESIE位（传输转义结束中断使能）

ESIE位使能在DMA传输期间发生的传输转义结束中断请求（重复大小结束中断请求和扩展重复区域溢出中断请求）。该位为1且DMSTS中的ESIF标志设置为1时发生中断。要清除传输转义结束中断，请将该位或DMSTS中的ESIF标志清除为0。

DTIE位（传输结束中断使能）

DTIE位使能在完成指定数量的数据传输时发生的传输结束中断请求。当该位为1且DMSTS中的DTIF标志设置为1时发生中断。要清除传输结束中断，请将该位或DMSTS中的DTIF标志清除为0。

17.2.7 DMA地址模式寄存器(DMAMD)

Address(es): DMAC0.DMAMD 4000 5014h, DMAC1.DMAMD 4000 5054h, DMAC2.DMAMD 4000 5094h, DMAC3.DMAMD 4000 50D4h, DMAC4.DMAMD 4000 5114h, DMAC5.DMAMD 4000 5154h, DMAC6.DMAMD 4000 5194h, DMAC7.DMAMD 4000 51D4h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SM[1:0]		—	SARA[4:0]					DM[1:0]		—	DARA[4:0]				
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b4 to b0	DARA[4:0]	目标地址扩展重复区	指定目标地址上的扩展重复区域。有关设置的详细信息，请参见表17.2。	R/W
b5	—	Reserved	该位读取为0。写入值应为0。	R/W
b7, b6	DM[1:0]	目的地地址更新Mode	b7b600：固定地址01：偏移加法10：递增地址11：递减地址。	R/W
b12 to b8	SARA[4:0]	源地址扩展重复区	指定源地址上的扩展重复区域。有关设置的详细信息，请参见表17.2。	R/W
b13	—	Reserved	该位读取为0。写入值应为0。	R/W
b15, b14	SM[1:0]	源地址更新模式	b15b1400：固定地址01：偏移加法10：递增地址11：递减地址。	R/W

DARA[4:0]位（目标地址扩展重复区域）

DARA[4:0]位指定目标地址上的扩展重复区域。扩展重复区功能是通过更新指定的低地址位来实现的，而其余的高地址位是固定的。扩展重复区域的大小可以是2字节到128MB之间的任意二的幂。

当低地址在地址增量上溢出扩展重复区域时，设置扩展重复区域的起始地址。类似地，在地址减量时，当低位地址下溢扩展重复区域时，设置扩展重复区域的结束地址。

Do not specify the extended repeat area on the destination address when a repeat or block area is specified as the transfer destination. When repeat or block transfer is selected, and when DMACm.DMTMD.DTS[1:0] = 00b (the transfer destination is specified as the repeat or block area), write 00000b in the DARA[4:0] bits.

To request an interrupt when an overflow or underflow occurs in the extended repeat area, set the DARIE bit in DMINT to 1. Table 17.2 lists the extended repeat areas associated with each setting.

DM[1:0] bits (Destination Address Update Mode)

The DM[1:0] bits select the update mode for the destination address:

- When increment is selected and the SZ[1:0] bits in DMTMD are set to 00b, 01b, and 10b, the destination address is incremented by 1, 2, and 4, respectively
- When decrement is selected and the SZ[1:0] bits in DMTMD are set to 00b, 01b, and 10b, the destination address is decremented by 1, 2, and 4, respectively
- When offset addition is selected, the offset specified in the DMACm.DMOFR register is added to the address.

SARA[4:0] bits (Source Address Extended Repeat Area)

The SARA[4:0] bits specify the extended repeat area on the source address. The extended repeat area function is realized through an update of the specified lower address bits with the remaining upper address bits fixed. The size of the extended repeat area can be any power of two between 2 bytes and 128 MB.

The start address of the extended repeat area is set when the lower address overflows the extended repeat area on an address increment. Similarly, the end address of the extended repeat area is set when the lower address underflows the extended repeat area on an address decrement.

Do not specify the extended repeat area on the source address when a repeat or block area is specified as the transfer source. When repeat or block transfer is selected, and when DMACm.DMTMD.DTS[1:0] = 01b (the transfer source is specified as the repeat or block area), write 00000b in the SARA[4:0] bits.

To request an interrupt when an overflow or underflow occurs in the extended repeat area, set the SARIE bit in DMINT to 1. Table 17.2 lists the extended repeat areas associated with each setting.

SM[1:0] bits (Source Address Update Mode)

The SM[1:0] bits select the update mode for the source address:

- When increment is selected and the SZ[1:0] bits in DMTMD are set to 00b, 01b, and 10b, the source address is incremented by 1, 2, and 4, respectively
- When decrement is selected and the SZ[1:0] bits in DMTMD are set to 00b, 01b, and 10b, the source address is decremented by 1, 2, and 4, respectively
- When offset addition is selected, the offset specified in the DMACm.DMOFR register is added to the address.

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Table 17.2 SARA[4:0] or DARA[4:0] settings and corresponding repeat areas (1 of 2)

SARA[4:0] or DARA[4:0]	Extended repeat area
00000b	Not specified
00001b	2 bytes specified as extended repeat area by the lower 1 bit of the address
00010b	4 bytes specified as extended repeat area by the lower 2 bits of the address
00011b	8 bytes specified as extended repeat area by the lower 3 bits of the address
00100b	16 bytes specified as extended repeat area by the lower 4 bits of the address
00101b	32 bytes specified as extended repeat area by the lower 5 bits of the address
00110b	64 bytes specified as extended repeat area by the lower 6 bits of the address
00111b	128 bytes specified as extended repeat area by the lower 7 bits of the address
01000b	256 bytes specified as extended repeat area by the lower 8 bits of the address
01001b	512 bytes specified as extended repeat area by the lower 9 bits of the address
01010b	1 KB specified as extended repeat area by the lower 10 bits of the address

将重复或块区域指定为传输目标时，请勿在目标地址上指定扩展重复区域。选择重复或块传输时，并且当DMACm.DMTMD.DTS[1:0]=00b（传输目标指定为重复或块区域）时，将00000b写入DARA[4:0]位。

要在扩展重复区域发生上溢或下溢时请求中断，请将DMINT中的DARIE位设置为1。表17.2列出了与每个设置相关的扩展重复区域。

DM[1:0]位（目标地址更新模式）

DM[1:0]位选择目标地址的更新模式：

- WhenincrementisselectedandtheSZ[1:0]bitsinDMTMDaresetto00b 01b and10b thedestinationaddressisincrementedby1 2 and4 respectively
- WhendecrementisselectedandtheSZ[1:0]bitsinDMTMDaresetto00b 01b and10b thedestinationaddressisdecrementedby1 2 and4 respectively
- 选择偏移添加后，将dmacm.dmofr寄存器中指定的偏移添加到地址中。

SARA[4:0]位（源地址扩展重复区）

SARA[4:0]位指定源地址上的扩展重复区域。扩展重复区功能是通过更新指定的低地址位来实现的，而其余的高地址位是固定的。扩展重复区域的大小可以是2字节到128MB之间的任意二的幂。

当低地址在地址增量上溢出扩展重复区域时，设置扩展重复区域的起始地址。类似地，在地址减量时，当低位地址下溢扩展重复区域时，设置扩展重复区域的结束地址。

当重复或块区域被指定为传输源时，不要在源地址上指定扩展重复区域。选择重复或块传输时，并且当DMACm.DMTMD.DTS[1:0]=01b（传输源指定为重复或块区域）时，将00000b写入SARA[4:0]位。

要在扩展重复区域发生上溢或下溢时请求中断，请将DMINT中的SARIE位设置为1。表17.2列出了与每个设置相关的扩展重复区域。

SM[1:0]位（源地址更新模式）

SM[1:0]位选择源地址的更新模式：

- WhenincrementisselectedandtheSZ[1:0]bitsinDMTMDaresetto00b 01b and10b thesourceaddressisincrementedby1 2 and4 respectively
- WhendecrementisselectedandtheSZ[1:0]bitsinDMTMDaresetto00b 01b and10b thesourceaddressisdecrementedby1 2 and4 respectively
- 选择偏移添加后，将dmacm.dmofr寄存器中指定的偏移添加到地址中。

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Table 17.2 SARA[4:0]或DARA[4:0]设置和相应的重复区域（1of2）

SARA[4:0] or DARA[4:0]	扩展重复区域
00000b	未指定
00001b	由地址的低1位指定为扩展重复区域的2个字节
00010b	由地址的低2位指定为扩展重复区域的4个字节
00011b	由地址的低3位指定为扩展重复区域的8个字节
00100b	由地址的低4位指定为扩展重复区域的16个字节
00101b	由地址的低5位指定为扩展重复区域的32个字节
00110b	由地址的低6位指定为扩展重复区域的64个字节
00111b	由地址的低7位指定为扩展重复区域的128个字节
01000b	由地址的低8位指定为扩展重复区域的256个字节
01001b	由地址的低9位指定为扩展重复区域的512个字节
01010b	1KB由地址的低10位指定为扩展重复区域

Table 17.2 SARA[4:0] or DARA[4:0] settings and corresponding repeat areas (2 of 2)

SARA[4:0] or DARA[4:0]	Extended repeat area
01011b	2 KB specified as extended repeat area by the lower 11 bits of the address
01100b	4 KB specified as extended repeat area by the lower 12 bits of the address
01101b	8 KB specified as extended repeat area by the lower 13 bits of the address
01110b	16 KB specified as extended repeat area by the lower 14 bits of the address
01111b	32 KB specified as extended repeat area by the lower 15 bits of the address
10000b	64 KB specified as extended repeat area by the lower 16 bits of the address
10001b	128 KB specified as extended repeat area by the lower 17 bits of the address
10010b	256 KB specified as extended repeat area by the lower 18 bits of the address
10011b	512 KB specified as extended repeat area by the lower 19 bits of the address
10100b	1 MB specified as extended repeat area by the lower 20 bits of the address
10101b	2 MB specified as extended repeat area by the lower 21 bits of the address
10110b	4 MB specified as extended repeat area by the lower 22 bits of the address
10111b	8 MB specified as extended repeat area by the lower 23 bits of the address
11000b	16 MB specified as extended repeat area by the lower 24 bits of the address
11001b	32 MB specified as extended repeat area by the lower 25 bits of the address
11010b	64 MB specified as extended repeat area by the lower 26 bits of the address
11011b	128 MB specified as extended repeat area by the lower 27 bits of the address
11100b to 11111b	Setting prohibited

17.2.8 DMA Offset Register (DMOFR)

Address(es): DMAC0.DMOFR 4000 5018h, DMAC1.DMOFR 4000 5058h, DMAC2.DMOFR 4000 5098h, DMAC3.DMOFR 4000 50D8h, DMAC4.DMOFR 4000 5118h, DMAC5.DMOFR 4000 5158h, DMAC6.DMOFR 4000 5198h, DMAC7.DMOFR 4000 51D8h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Description	Setting range	R/W
b31 to b0	Specifies the offset when offset addition is selected as the address update mode for transfer source or destination	0000 0000h to 00FF FFFFh (0 bytes to (16 MB - 1 byte)) FF00 0000h to FFFF FFFFh (-16 MB to -1 byte).	R/W

Only write to this register while DMAC operation is stopped or DMA transfer is disabled, not during data transfer. Setting bits 31 to 25 is invalid. The value in bit 24 is extended to bits 31 to 25. Reading DMOFR returns the extended value.

Table 17.2 SARA[4:0]或DARA[4:0]设置和相应的重复区域(2of2)

SARA[4:0] or DARA[4:0]	扩展重复区域
01011b	2KB由地址的低11位指定为扩展重复区域
01100b	4KB由地址的低12位指定为扩展重复区域
01101b	8KB由地址的低13位指定为扩展重复区域
01110b	16KB由地址的低14位指定为扩展重复区域
01111b	32KB由地址的低15位指定为扩展重复区域
10000b	64KB由地址的低16位指定为扩展重复区域
10001b	128KB由地址的低17位指定为扩展重复区域
10010b	256KB由地址的低18位指定为扩展重复区域
10011b	512KB由地址的低19位指定为扩展重复区域
10100b	1MB由地址的低20位指定为扩展重复区域
10101b	2MB由地址的低21位指定为扩展重复区域
10110b	4MB由地址的低22位指定为扩展重复区域
10111b	8MB由地址的低23位指定为扩展重复区域
11000b	16MB由地址的低24位指定为扩展重复区域
11001b	32MB由地址的低25位指定为扩展重复区域
11010b	64MB由地址的低26位指定为扩展重复区域
11011b	128MB由地址的低27位指定为扩展重复区域
11100b to 11111b	禁止设定

17.2.8 DMA偏移寄存器(DMOFR)

Address(es): DMAC0.DMOFR 4000 5018h, DMAC1.DMOFR 4000 5058h, DMAC2.DMOFR 4000 5098h, DMAC3.DMOFR 4000 50D8h, DMAC4.DMOFR 4000 5118h, DMAC5.DMOFR 4000 5158h, DMAC6.DMOFR 4000 5198h, DMAC7.DMOFR 4000 51D8h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Description	设定范围	R/W
b31 to b0	Specifiestheoffsetwhenoffsetadditionisselectedastheaddressupdatemodefortransfersourceordestination	00000000h至00FFFFFFh（0字节至（16MB1字节））FF000000h至FFFFFFFFh（-16MB至-1字节）。	R/W

仅在DMAC操作停止或DMA传输被禁用时写入该寄存器，而不是在数据传输期间。
设置位31到25无效。位24中的值扩展为位31到25。读取DMOFR将返回扩展值。

17.2.9 DMA Transfer Enable Register (DMCNT)

Address(es): DMAC0.DMCNT 4000 501Ch, DMAC1.DMCNT 4000 505Ch, DMAC2.DMCNT 4000 509Ch, DMAC3.DMCNT 4000 50DCh, DMAC4.DMCNT 4000 511Ch, DMAC5.DMCNT 4000 515Ch, DMAC6.DMCNT 4000 519Ch, DMAC7.DMCNT 4000 51DCh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	DTE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	DTE	DMA Transfer Enable	0: Disable 1: Enable.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

DTE bit (DMA Transfer Enable)

The DTE bit enables DMA transfer. To enable DMA transfer, set the DMST bit in DMAST to 1 to enable DMAC activation, then set the DTE bit to 1 to enable DMA transfer for the associated channel.

[Setting condition]

- When 1 is written to this bit.

[Clearing conditions]

- When 0 is written to this bit
- When the specified volume of data transfer is complete
- When DMA transfer is stopped by a repeat size end interrupt
- When DMA transfer is stopped by an extended repeat area overflow interrupt.

17.2.10 DMA Software Start Register (DMREQ)

Address(es): DMAC0.DMREQ 4000 501Dh, DMAC1.DMREQ 4000 505Dh, DMAC2.DMREQ 4000 509Dh, DMAC3.DMREQ 4000 50DDh, DMAC4.DMREQ 4000 511Dh, DMAC5.DMREQ 4000 515Dh, DMAC6.DMREQ 4000 519Dh, DMAC7.DMREQ 4000 51DDh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	CLRS	—	—	—	SWREQ
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	SWREQ	DMA Software Start	0: Do not request DMA transfer 1: Request DMA transfer.	R/W
b3 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	CLRS	DMA Software Start Bit Auto Clear Select	0: Clear SWREQ bit after DMA transfer is started by software 1: Do not clear SWREQ bit after DMA transfer is started by software.	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

SWREQ bit (DMA Software Start)

Writing 1 to the SWREQ bit generates a DMA transfer request. After DMA transfer starts in response, SWREQ clears to 0 if the CLRS bit is 0.

SWREQ does not clear to 0 if CLRS is 1. A DMA transfer request is issued again after completion of the transfer.

Note: Setting this bit is valid and DMA transfer by software is enabled only when the DCTG[1:0] bits in DMTMD are set

17.2.9 DMA传输使能寄存器(DMCNT)

Address(es): DMAC0.DMCNT 4000 501Ch, DMAC1.DMCNT 4000 505Ch, DMAC2.DMCNT 4000 509Ch, DMAC3.DMCNT 4000 50DCh, DMAC4.DMCNT 4000 511Ch, DMAC5.DMCNT 4000 515Ch, DMAC6.DMCNT 4000 519Ch, DMAC7.DMCNT 4000 51DCh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	DTE
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	DTE	DMA传输使能	0：禁用1 ：启用。	R/W
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

DTE位（DMA传输使能）

DTE位启用DMA传输。要启用DMA传输，请将DMAST中的DMST位设置为1以启用DMAC激活，然后将DTE位设置为1以启用相关通道的DMA传输。

[Setting condition]

- 当1写入该位时。

[Clearing conditions]

- 当0写入该位时
- 当指定的数据传输量完成时
- 当DMA传输因重复大小结束中断而停止时
- 当DMA传输因扩展重复区域溢出中断而停止时。

17.2.10 DMA软件启动寄存器(DMREQ)

Address(es): DMAC0.DMREQ 4000 501Dh, DMAC1.DMREQ 4000 505Dh, DMAC2.DMREQ 4000 509Dh, DMAC3.DMREQ 4000 50DDh, DMAC4.DMREQ 4000 511Dh, DMAC5.DMREQ 4000 515Dh, DMAC6.DMREQ 4000 519Dh, DMAC7.DMREQ 4000 51DDh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	CLRS	—	—	—	SWREQ
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	SWREQ	DMA软件启动	0：不请求DMA传输1：请求DMA传输。	R/W
b3 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b4	CLRS	DMA软件启动位自动清除选择	0：软件启动DMA传输后清除SWREQ位1：软件启动DMA传输后不清除SWREQ位。	R/W
b7 to b5	—	Reserved	这些位被读取为0。写入值应为0。	R/W

SWREQ位（DMA软件启动）

将1写入SWREQ位会生成DMA传输请求。在响应开始DMA传输后，如果CLRS位为0，则SWREQ清除为0。

如果CLRS为1，则SWREQ不会清除为0。传输完成后再次发出DMA传输请求。

Note: 只有当DMTMD中的DCTG[1:0]位被置位时，设置该位才有效并且软件的DMA传输被使能

to 00b, specifying software as the DMA activation source. Setting this bit is invalid when the DCTG[1:0] bits in DMTMD are set to any value other than 00b.

To start DMA transfer by software with the CLRS bit set to 0, ensure that the SWREQ bit is 0, then write 1 to the SWREQ bit.

[Setting condition]

- When 1 is written to this bit.

[Clearing conditions]

- When a DMA transfer request by software is accepted and DMA transfer is started with the CLRS bit set to 0 (the SWREQ bit is cleared after DMA transfer is started by software)
- When 0 is written to this bit.

CLRS bit (DMA Software Start Bit Auto Clear Select)

When an SWREQ setting of 1 triggers a transfer request, the CLRS bit specifies whether to clear the SWREQ bit to 0 after DMA transfer starts in response:

- When CLRS is set to 0, SWREQ clears to 0 after DMA transfer starts.
- When CLRS is set to 1, SWREQ does not clear to 0. A DMA transfer request is issued again after completion of the transfer.

17.2.11 DMA Status Register (DMSTS)

Address(es): DMAC0.DMSTS 4000 501Eh, DMAC1.DMSTS 4000 505Eh, DMAC2.DMSTS 4000 509Eh, DMAC3.DMSTS 4000 50DEh, DMAC4.DMSTS 4000 511Eh, DMAC5.DMSTS 4000 515Eh, DMAC6.DMSTS 4000 519Eh, DMAC7.DMSTS 4000 51DEh

	b7	b6	b5	b4	b3	b2	b1	b0
	ACT	—	—	DTIF	—	—	—	ESIF
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	ESIF	Transfer Escape End Interrupt Flag	0: No interrupt occurred 1: Interrupt occurred.	R/W*1
b3 to b1	—	Reserved	These bits are read as 0. Writing to these bits has no effect.	R
b4	DTIF	Transfer End Interrupt Flag	0: No interrupt occurred 1: Interrupt occurred.	R/W*1
b6, b5	—	Reserved	These bits are read as 0. Writing to these bits has no effect.	R
b7	ACT	DMA Active Flag	0: DMAC operation suspended 1: DMAC operating.	R

Note 1. Only 0 can be written, to clear the flag.

ESIF flag (Transfer Escape End Interrupt Flag)

The ESIF flag indicates that a transfer escape end interrupt occurred.

[Setting conditions]

- In repeat transfer mode, when one repeat size data transfer completes with the RPTIE bit in DMINT set to 1
- In block transfer mode, when one block data transfer completes with the RPTIE bit in DMINT set to 1
- When an extended repeat area overflow on the source address occurs with the SARIE bit in DMINT set to 1, and the SARA[4:0] bits in DMAMD set to any value other than 00000b (extended repeat area is specified on the transfer source address)
- When an extended repeat area overflow on the destination address occurs with the DARIE bit in DMINT set to 1,

到00b，指定软件作为DMA激活源。当DMTMD中的DCTG[1:0]位设置为00b以外的任何值时，设置该位无效。

要在CLRS位设置为0的情况下通过软件启动DMA传输，请确保SWREQ位为0，然后将1写入SWREQ bit.

[Setting condition]

- 当1写入该位时。

[Clearing conditions]

- 当软件的DMA传输请求被接受并且DMA传输开始时CLRS位设置为0（SWREQ位在软件启动DMA传输后清零）
- 当0写入该位时。

CLRS位（DMA软件起始位自动清除选择）

当SWREQ设置为1触发传输请求时，CLRS位指定在DMA传输开始后是否将SWREQ位清除为0作为响应：

- 当CLRS设置为0时，在DMA传输开始后SWREQ清除为0。
- 当CLRS设置为1时，SWREQ不会清除为0。传输完成后再次发出DMA传输请求。

17.2.11 DMA状态寄存器(DMSTS)

Address(es): DMAC0.DMSTS 4000 501Eh, DMAC1.DMSTS 4000 505Eh, DMAC2.DMSTS 4000 509Eh, DMAC3.DMSTS 4000 50DEh, DMAC4.DMSTS 4000 511Eh, DMAC5.DMSTS 4000 515Eh, DMAC6.DMSTS 4000 519Eh, DMAC7.DMSTS 4000 51DEh

	b7	b6	b5	b4	b3	b2	b1	b0
	ACT	—	—	DTIF	—	—	—	ESIF
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	ESIF	传输转义结束中断Flag	0：未发生中断1：发生中断。	R/W*1
b3 to b1	—	Reserved	这些位被读取为0。写入这些位无效。	R
b4	DTIF	传输结束中断标志	0：未发生中断1：发生中断。	R/W*1
b6, b5	—	Reserved	这些位被读取为0。写入这些位无效。	R
b7	ACT	DMA活动标志	0：DMAC操作暂停1：DMAC操作。	R

Note 1. 只能写入0，以清除标志。

ESIF标志（传输转义结束中断标志）

ESIF标志表示发生了传输转义结束中断。

[Setting conditions]

- 在重复传输模式下，当一个重复大小的数据传输完成且DMINT中的RPTIE位设置为1时
- 在块传输模式下，当一个块数据传输完成且DMINT中的RPTIE位设置为1
- 当源地址发生扩展重复区域溢出且DMINT中的SARIE位设置为1，并且DMAMD中的SARA[4:0]位设置为00000b以外的任何值（在传输源地址上指定扩展重复区域）
- 当目标地址发生扩展重复区域溢出且DMINT中的DARIE位设置为1时，

and the DARA[4:0] bits in DMAMD set to any value other than 00000b (extended repeat area is specified on the transfer destination address).

[Clearing conditions]

- When 0 is written to this flag
- When 1 is written to the DTE bit in DMCNT.

DTIF flag (Transfer End Interrupt Flag)

The DTIF flag indicates that a transfer end interrupt occurred.

[Setting conditions]

- In normal transfer mode, when the specified number of unit transfers completes (the value of DMCRAL becomes 0 on completion of transfer)
- In repeat transfer mode, when the specified number of repeat transfer operations completes (the value of DMCRB becomes 0 on completion of transfer)
- In block transfer mode, when the specified number of blocks is transferred (the value of DMCRB becomes 0 on completion of transfer).

[Clearing conditions]

- When 0 is written to this flag
- When 1 is written to the DTE bit in DMCNT.

ACT flag (DMA Active Flag)

The ACT flag indicates whether the DMAC is in the idle or active state.

[Setting condition]

- When the DMAC starts a data transfer.

[Clearing condition]

- When the data transfer in response to one transfer request completes.

17.2.12 DMAC Module Activation Register (DMAST)

Address(es): DMA.DMAST 4000 5200h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	DMST
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	DMST	DMAC Operation Enable	0: Disable 1: Enable.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

DMST bit (DMAC Operation Enable)

Setting the DMST bit to 1 enables DMAC activation for all channels. When the DMST bit is set to 1 (DMAC activation is enabled), and 1 is written to the DMACm.DMCNT.DTE bit (DMA transfer is enabled) for multiple channels, all of the associated channels can be placed in the transfer request ready state at the same time.

When the DMST bit is cleared to 0 during DMA transfer, DMA transfer is suspended after the current data transfer corresponding to a single transfer request completes. To resume DMA transfer, set the DMST bit to 1 again.

[Setting condition]

并且DMAMD中的DARA[4:0]位设置为00000b以外的任何值（在传输目标地址上指定扩展重复区域）。

[Clearing conditions]

- 当0写入此标志时
- 当1写入DMCNT中的DTE位时。

DTIF标志（传输结束中断标志）

DTIF标志表示发生了传输结束中断。

[Setting conditions]

- 在正常传输模式下，当指定数量的单元传输完成时（传输完成时DMCRAL的值变为0）
- 在重复传输模式下，当指定次数的重复传输操作完成时（传输完成时DMRCB的值变为0）
- 在块传输模式下，当传输指定数量的块时（传输完成时DMCRB的值变为0）。

[Clearing conditions]

- 当0写入此标志时
- 当1写入DMCNT中的DTE位时。

ACT标志（DMA活动标志）

ACT标志指示DMAC是处于空闲状态还是活动状态。

[Setting condition]

- 当DMAC开始数据传输时。

[Clearing condition]

- 当响应一个传输请求的数据传输完成时。

17.2.12 DMAC模块激活寄存器(DMAST)

Address(es): DMA.DMAST 4000 5200h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	DMST
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	DMST	DMAC操作使能	0：禁用1 ：启用。	R/W
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

DMST位（DMAC操作使能）

将DMST位设置为1启用所有通道的DMAC激活。当DMST位设置为1（启用DMAC激活），并为多个通道向DMA Cm.DMCNT.DTE位写入1（启用DMA传输）时，所有相关通道都可以置于传输请求就绪状态同时状态。

当DMA传输期间DMST位清0时，在当前与单个传输请求对应的数据传输完成后，DMA传输将暂停。要恢复DMA传输，请将DMST位再次设置为1。

[Setting condition]

- When 1 is written to this bit.

[Clearing condition]

- When 0 is written to this bit.

17.3 Operation

17.3.1 Transfer Mode

(1) Normal transfer mode

In normal transfer mode, one data unit is transferred for one transfer request. You can specify the number of transfer operations, up a maximum of 65,535, in DMACm.DMCRAL. When these bits are set to 0000h, no number of operations is specified and data transfer is performed with the transfer counter stopped (free running mode).

A transfer end interrupt request can be generated after completion of the specified number of transfer operations, except when data transfers are occurring in free running mode.

Setting DMACm.DMCRB is invalid in normal transfer mode.

Table 17.3 summarizes the register update operation in normal transfer mode.

Table 17.3 Register update operation in normal transfer mode

Register	Function	Update operation after completion of a transfer for one transfer request
DMACm.DMSAR	Transfer source address	Increment, decrement, fixed, or offset addition
DMACm.DMDAR	Transfer destination address	Increment, decrement, fixed, or offset addition
DMACm.DMCRAL	Transfer count	Decremented by one or not updated (in free running mode)
DMACm.DMCRAH	-	Not updated (not used in normal transfer mode)
DMACm.DMCRB	-	Not updated (not used in normal transfer mode)

Figure 17.2 shows the operation in normal transfer mode.

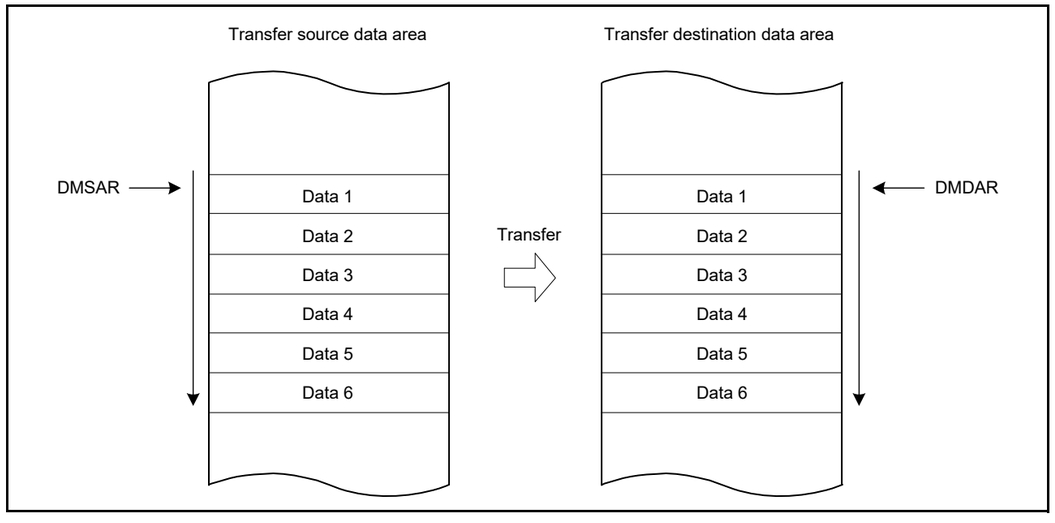


Figure 17.2 Operation in normal transfer mode

(2) Repeat transfer mode

In repeat transfer mode, one data unit is transferred for one transfer request. The repeat transfer size, up to a maximum of 1K data units, is set in DMACm.DMCRA.

- 当1写入该位时。

[Clearing condition]

- 当0写入该位时。

17.3 Operation

17.3.1 传输模式

(1) 正常传输模式

在正常传输模式下，对于一个传输请求传输一个数据单元。您可以在DMACm.DMCRAL中指定传输操作的数量，最多为65 535。当这些位设置为0000h时，不指定操作数，并且在传输计数器停止的情况下执行数据传输（自由运行模式）。

在完成指定数量的传输操作后，可以生成传输结束中断请求，除非数据传输发生在自由运行模式下。

在正常传输模式下设置DMACm.DMCRB无效。

表17.3总结了正常传输模式下的寄存器更新操作。

Table 17.3 正常传输模式下的寄存器更新操作

Register	Function	一个传输请求的传输完成后的更新操作
DMACm.DMSAR	传输源地址	递增、递减、固定或偏移添加
DMACm.DMDAR	转移目的地地址	递增、递减、固定或偏移添加
DMACm.DMCRAL	转移计数	减一或不更新（在自由运行模式下）
DMACm.DMCRAH	-	未更新（ 未在正常传输模式下使用）
DMACm.DMCRB	-	未更新（ 未在正常传输模式下使用）

图17.2显示了正常传输模式下的操作。

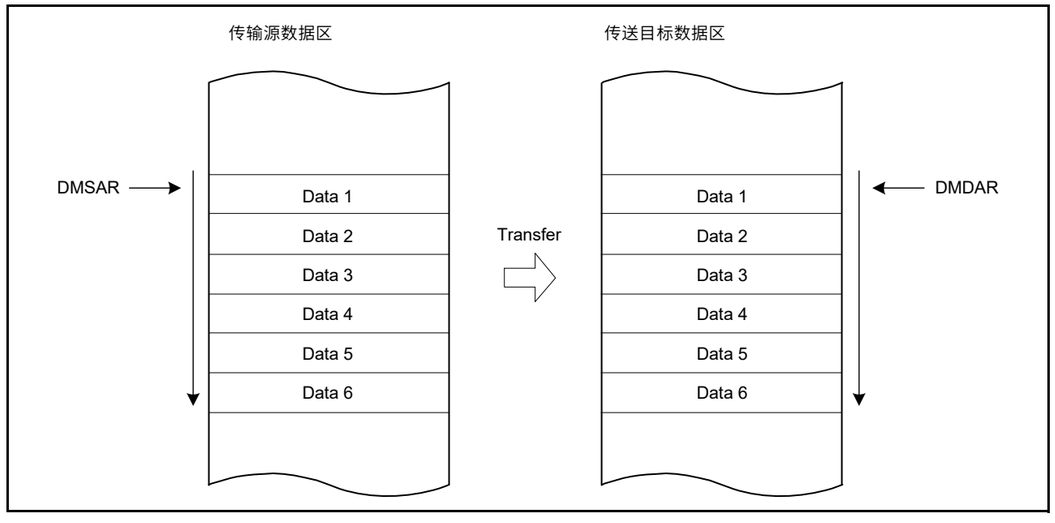


Figure 17.2 正常传输模式下的操作

(2) 重复传输模式

在重复传输模式中，对于一个传输请求传输一个数据单元。在DMACm.DMCRA中设置了最多1K数据单元的重复传输大小。

The number of repeat transfer operations, up to a maximum of 64K, is set in DMACm.DMCRB. A maximum of 64M data units (1K data units × 64K repeat transfer operations) can be set as a total data transfer size.

You can specify either the transfer source or destination as a repeat area. When transfer of the repeat size data is complete, the address of the specified repeat area (DMSAR or DMDAR in DMACm) returns to the transfer start address. In this mode, when all data of the specified repeat size is transferred, DMA transfer can be stopped and a repeat size end interrupt can be requested. To resume DMA transfer, write 1 to the DTE bit in DMACm.DMCNT during repeat size end interrupt handling.

A transfer end interrupt request can be generated after completion of the specified number of repeat transfers.

Table 17.4 summarizes the register update operation in repeat transfer mode, and Figure 17.3 shows the operation in repeat transfer mode.

Table 17.4 Register update operation in repeat transfer mode

		Update operation after completion of a transfer for one transfer request	
Register	**Function**	**When DMACm.DMCRAL is not 1**	**When DMACm.DMCRAL is 1 (transfer of the last repeat size data unit)**
DMACm.DMSAR	Transfer source address	Increment, decrement, fixed, or offset addition	• DMACm.DMTMD.DTS[1:0] = 00b Increment, decrement, fixed, or offset addition • DMACm.DMTMD.DTS[1:0] = 01b Initial value of DMACm.DMSAR • DMACm.DMTMD.DTS[1:0] = 10b Increment, decrement, fixed, or offset addition
DMACm.DMDAR	Transfer destination address	Increment, decrement, fixed, or offset addition	• DMACm.DMTMD.DTS[1:0] = 00b Initial value of DMACm.DMDAR • DMACm.DMTMD.DTS[1:0] = 01b Increment, decrement, fixed, or offset addition • DMACm.DMTMD.DTS[1:0] = 10b Increment, decrement, fixed, or offset addition
DMACm.DMCRAH	Repeat size	Not updated	Not updated
DMACm.DMCRAL	Transfer count	Decremented by one	DMACm.DMCRAH
DMACm.DMCRB	Count of repeat transfer operations	Not updated	Decremented by one

在DMACm.DMCRB中设置重复传输操作的数量，最大为64K。最多可将64M数据单元（1K数据单元×64K重复传输操作）设置为总数据传输大小。

您可以将传输源或目标指定为重复区域。当重复大小数据的传输完成时，指定的重复区域（DMACm中的DMSAR或DMDAR）的地址返回到传输起始地址。在此模式下，当指定重复大小的所有数据都传输完毕后，可以停止DMA传输并请求重复大小结束中断。要恢复DMA传输，请在重复大小结束中断处理期间将1写入DMACm.DMCNT中的DTE位。

完成指定次数的重复传输后，可以产生传输结束中断请求。

表17.4总结了重复传输模式下的寄存器更新操作，图17.3显示了重复传输模式下的操作。

Table 17.4 重复传输模式下的寄存器更新操作

		一个传输请求的传输完成后的更新操作	
Register	**Function**	**当DMACm.DMCRAL不为1时**	**当DMACm.DMCRAL为1时（传输最后一个重复大小数据单元）**
DMACm.DMSAR	传输源地址	递增、递减、固定或偏移添加	• DMACm.DMTMD.DTS[1:0] = 00b 递增、递减、固定或偏移加法 DMACm.DMTMD.DTS[1:0]=01bDMACm.DMSAR的初始值 DMACm.DMTMD.DTS[1:0]=10b 递增、递减、固定或偏移添加
DMACm.DMDAR	转移目的地地址	递增、递减、固定或偏移添加	DMACm.DMTMD.DTS[1:0]=00bDMACm.DMDAR的初始值 DMACm.DMTMD.DTS[1:0]=01b 递增、递减、固定或偏移加法 DMACm.DMTMD.DTS[1:0]=10b 递增、递减、固定或偏移添加
DMACm.DMCRAH	重复大小	未更新	未更新
DMACm.DMCRAL	转移计数	减一	DMACm.DMCRAH
DMACm.DMCRB	重复传输操作的计数	未更新	减一

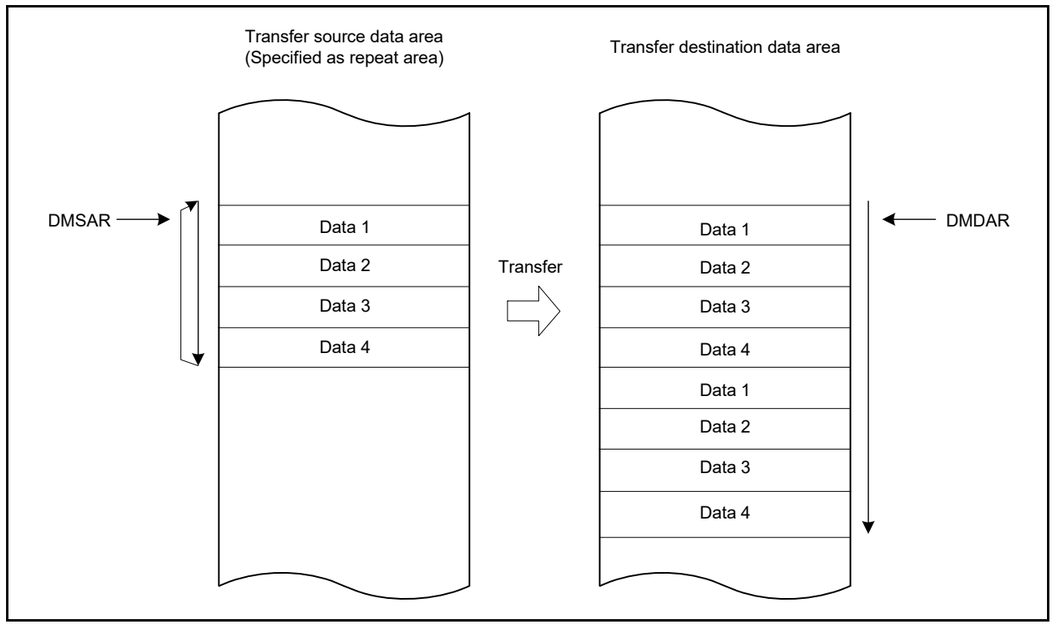


Figure 17.3 Operation in repeat transfer mode

(3) Block transfer mode

In block transfer mode, a single data block is transferred for one transfer request. The block size, up to a maximum of 1K data units, is set in DMACm.DMCRA.

The number of block transfers, up to a maximum of 64K, is set in DMACm.DMCRB. A maximum of 64M data units (1K data units × 64K block transfer operations) can be set as a total data transfer size.

You can specify either the transfer source or destination as a block area. When transfer of a single data block is complete, the address of the specified block area (DMSAR or DMDAR in DMACm) returns to the transfer start address. In this mode, when all data in a single block is transferred, DMA transfer can be stopped and a repeat size end interrupt can be requested. To resume DMA transfer, write 1 to the DTE bit in DMACm.DMCNT during repeat size end interrupt handling.

A transfer end interrupt request can be generated after completion of the specified number of block transfers.

Table 17.5 summarizes the register update operation in block transfer mode, and Figure 17.4 shows the operation in block transfer mode.

Table 17.5 Register update operation in block transfer mode (1 of 2)

Register	Function	Update operation after completion of single-block transfer for one transfer request
DMACm.DMSAR	Transfer source address	• DMACm.DMTMD.DTS[1:0] = 00b Increment, decrement, fixed, or offset addition • DMACm.DMTMD.DTS[1:0] = 01b Initial value of DMACm.DMSAR • DMACm.DMTMD.DTS[1:0] = 10b Increment, decrement, fixed, or offset addition.
DMACm.DMDAR	Transfer destination address	• DMACm.DMTMD.DTS[1:0] = 00b Initial value of DMACm.DMDAR • DMACm.DMTMD.DTS[1:0] = 01b Increment, decrement, fixed, or offset addition • DMACm.DMTMD.DTS[1:0] = 10b Increment, decrement, fixed, or offset addition.

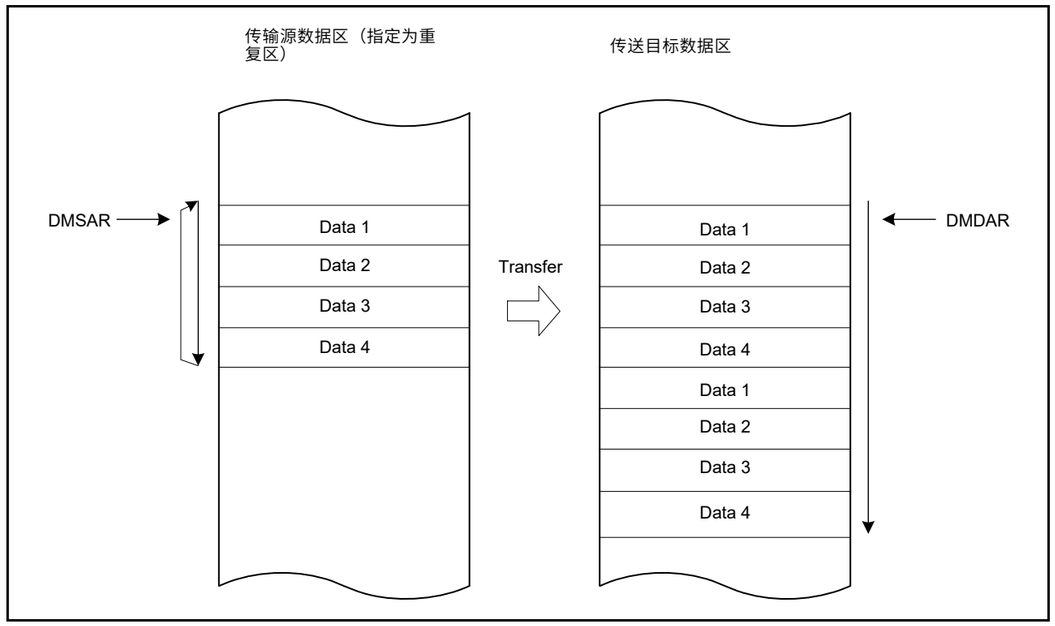


Figure 17.3 重复传输模式下的操作

(3) 块传输模式

在块传输模式下，为一个传输请求传输一个数据块。在DMACm.DMCRA中设置了最多1K个数据单元的块大小。

在DMACm.DMCRB中设置了最多64K的块传输次数。最多可以设置64M数据单元（1K数据单元×64K块传输操作）作为总数据传输大小。

您可以将传输源或目标指定为块区域。当单个数据块的传输完成时，指定块区域的地址（DMACm中的DMSAR或DMDAR）返回到传输起始地址。在这种模式下，当单个块中的所有数据都传输完毕后，可以停止DMA传输并请求重复大小结束中断。要恢复DMA传输，请在重复大小结束中断处理期间将1写入DMACm.DMCNT中的DTE位。

完成指定数量的块传输后，可以产生传输结束中断请求。

表17.5总结了块传输模式下的寄存器更新操作，图17.4显示了块传输模式下的操作。

Table 17.5 块传输模式下的寄存器更新操作（1of2）

Register	Function	一个传输请求的单块传输完成后的更新操作
DMACm.DMSAR	传输源地址	• DMACm.DMTMD.DTS[1:0] = 00b 递增、递减、固定或偏移加法 DMACm.DMTMD.DTS[1:0]=01bDMACm.DMSAR的初始值 DMACm.DMTMD.DTS[1:0]=10b 递增、递减、固定或偏移添加。
DMACm.DMDAR	转移目的地地址	DMACm.DMTMD.DTS[1:0]=00bDMACm.DMDAR的初始值 DMACm.DMTMD.DTS[1:0]=01b 递增、递减、固定或偏移加法 DMACm.DMTMD.DTS[1:0]=10b 递增、递减、固定或偏移添加。

Table 17.5 Register update operation in block transfer mode (2 of 2)

Register	Function	Update operation after completion of single-block transfer for one transfer request
DMACm.DMCRAH	Block size	Not updated
DMACm.DMCRAL	Transfer count	DMACm.DMCRAH
DMACm.DMCRB	Count of block transfer operations	Decremented by one

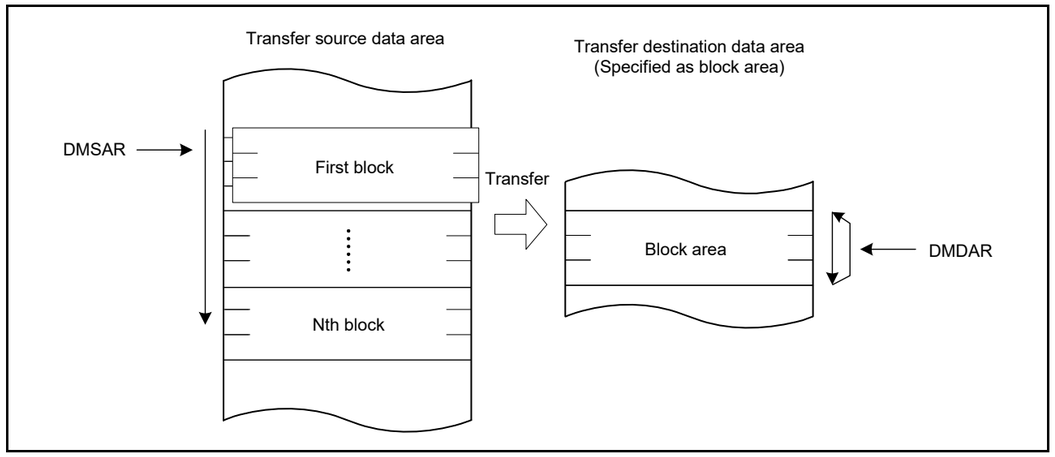


Figure 17.4 Operation in block transfer mode

17.3.2 Extended Repeat Area Function

The DMAC supports extended repeat areas on the transfer source and destination addresses, specified separately in the transfer source address register (DMSAR) and transfer destination address register (DMDAR) of DMACm. When this function is set, the address registers repeatedly indicate the addresses of the specified extended repeat areas.

The extended repeat area on the source address is specified in the SARA[4:0] bits in DMACm.DMAMD. The extended repeat area on the destination address is specified in the DARA[4:0] bits in DMACm.DMAMD. You can specify different sizes for the source and destination. However, you must not specify a transfer source or destination that is set as the repeat or block area as the extended repeat area.

When the address register value reaches the end address of the extended repeat area and the extended repeat area overflows, DMA transfer is stopped and an extended repeat area overflow interrupt can be requested. When an overflow occurs in the extended repeat area on the transfer source while the SARIE bit in DMACm.DMINT is set to 1, the ESIF flag in DMACm.DMSTS is set to 1 and the DTE bit in DMACm.DMCNT is cleared to 0 to stop DMA transfer. At this point, if the ESIE bit in DMACm.DMINT is set to 1, an extended repeat area overflow interrupt is requested. When the DARIE bit in DMACm.DMINT is set to 1, the destination address register becomes a target for the function. To resume DMA transfer, write 1 to the DTE bit in DMACm.DMCNT during interrupt handling.

Figure 17.5 shows an example of the extended repeat area operation.

Table 17.5 块传输模式下的寄存器更新操作(2of2)

Register	Function	一个传输请求的单块传输完成后的更新操作
DMACm.DMCRAH	块大小	未更新
DMACm.DMCRAL	转移计数	DMACm.DMCRAH
DMACm.DMCRB	块传输操作的计数	减一

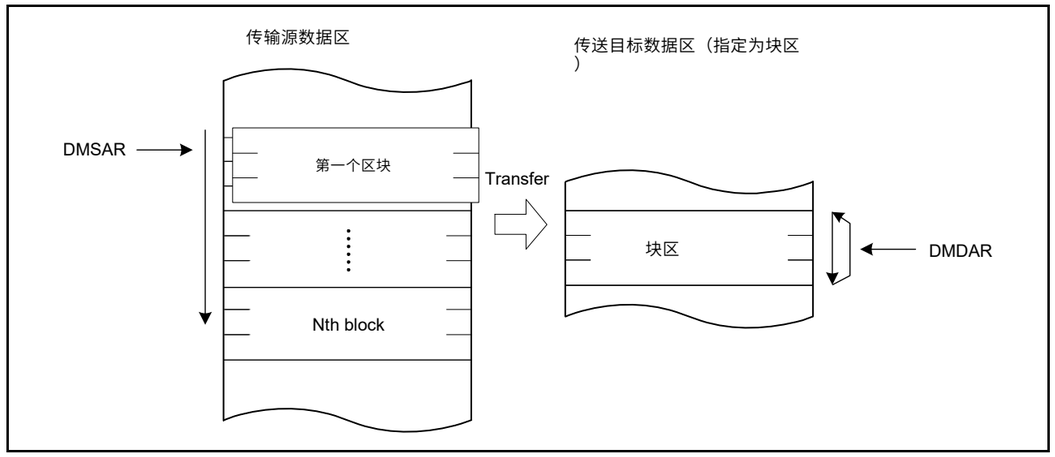


Figure 17.4 块传输模式下的操作

17.3.2 扩展重复区域功能

DMAC支持在传输源地址和目标地址上扩展重复区域，分别在DMACm的传输源地址寄存器(DMSAR)和传输目标地址寄存器(DMDAR)中指定。设置此功能时，地址寄存器重复指示指定扩展重复区域的地址。

源地址上的扩展重复区域在DMACm.DMAMD中的SARA[4:0]位中指定。目标地址上的扩展重复区域在DMACm.DMAMD中的DARA[4:0]位中指定。您可以为源和目标指定不同的大小。但是，您不能将设置为重复或块区域的传输源或目标指定为扩展重复区域。

当地址寄存器值到达扩展重复区的结束地址且扩展重复区溢出时，停止DMA传输，可以请求扩展重复区溢出中断。当DMACm.DMINT中的SARIE位设置为1时，传输源的扩展重复区域发生溢出时，DMACm.DMSTS中的ESIF标志设置为1，DMACm.DMCNT中的DTE位清为0停止DMA传输。此时，如果DMACm.DMINT中的ESIE位设置为1，则请求扩展重复区域溢出中断。当DMACm.DMINT中的DARIE位设置为1时，目标地址寄存器成为函数的目标。恢复

DMA传输，在中断处理期间将1写入DMACm.DMCNT中的DTE位。

图17.5显示了扩展重复区域操作的示例。

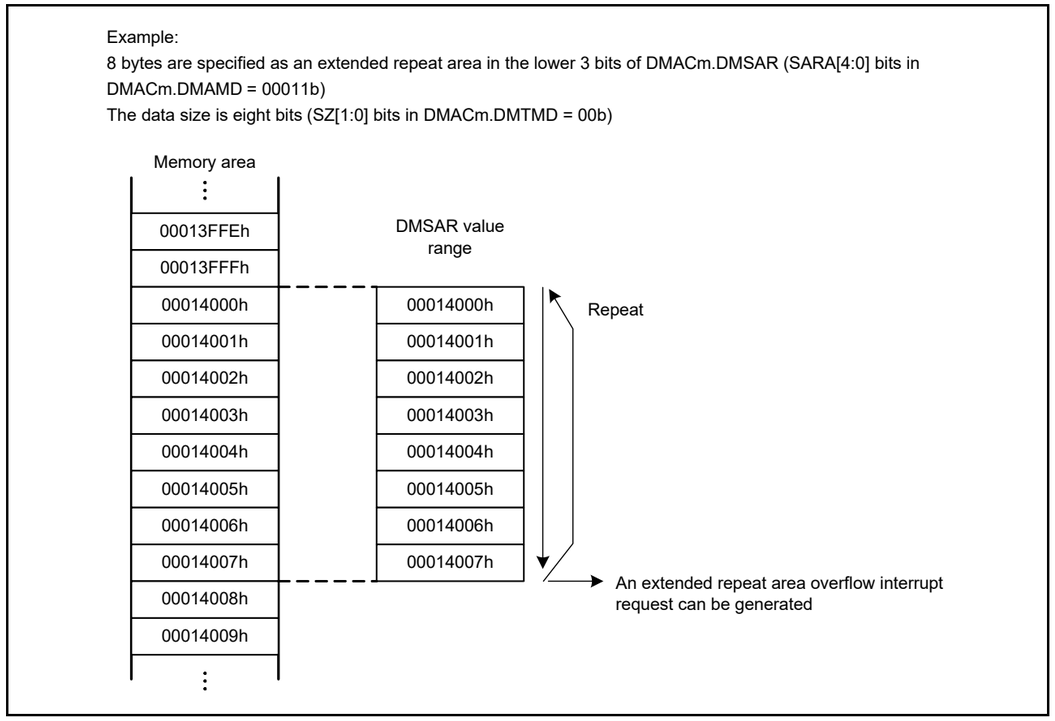


Figure 17.5 Example of extended repeat area operation

When using extended repeat area overflow interrupts in block transfer mode, consider the following points:

- When a transfer is stopped by an extended repeat area overflow interrupt, the address register must be set so that the block size is a power of 2 or the block size boundary is aligned with the extended repeat area boundary. When an overflow on the extended repeat area occurs during a transfer of one block, the overflow interrupt is suspended until transfer of the block is complete, and the transfer overruns.

Figure 17.6 shows an example of using the extended repeat area function in block transfer mode.

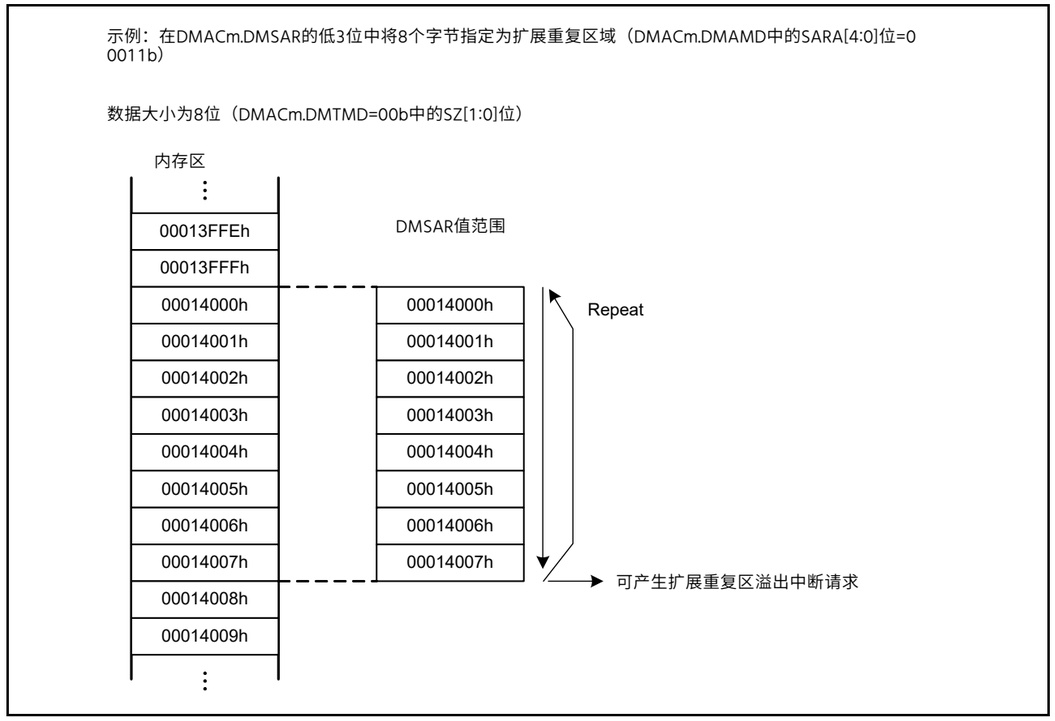


Figure 17.5 扩展重复区域操作示例

在块传输模式下使用扩展重复区域溢出中断时，请考虑以下几点：

- 当传输由扩展重复区域溢出中断停止时，地址寄存器必须设置为块大小为2的幂或块大小边界与扩展重复区域边界对齐。当一个块的传输过程中扩展重复区域发生溢出时，溢出中断被暂停，直到块的传输完成，传输溢出。

图17.6显示了在块传输模式下使用扩展重复区域功能的示例。

Example:
8 bytes are specified as an extended repeat area in the lower 3 bits of DMACm.DMSAR (SARA[4:0] bits in DMACm.DMAMD = 00011b)
Block transfer mode with block size 5 is set (DMACm.DMCRA = 00050005h)
The transfer source address is not specified as a block area
The data size is 8 bits (SZ[1:0] bits in DMACm.DMTMD = 00b)

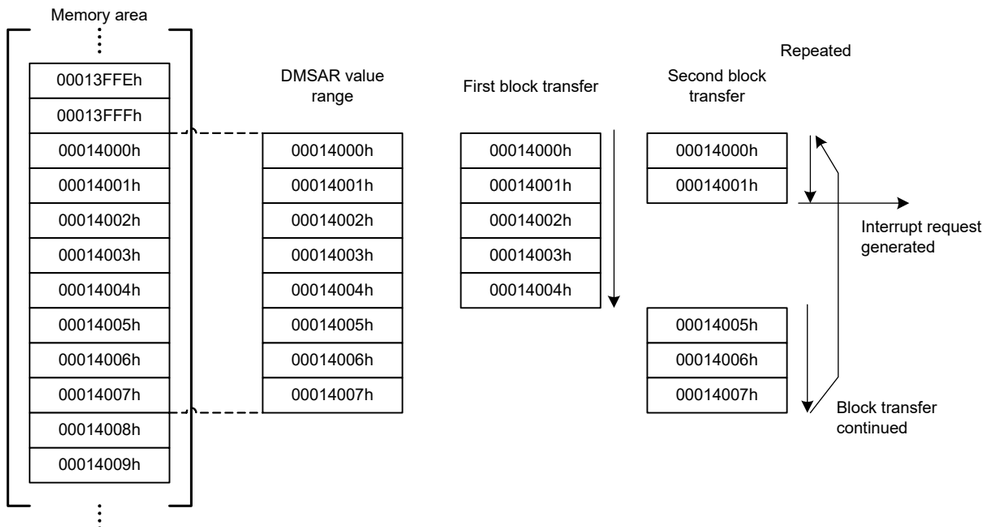


Figure 17.6 Example of extended repeat area function in block transfer mode

17.3.3 Address Update Function Using Offset

The source and destination addresses can be updated by fixing, incrementing, decrementing, or adding an offset. When offset addition is selected, the offset specified in the DMA Offset Register (DMACm.DMOFR) is added to the address every time the DMAC performs one data transfer. You can also subtract an offset by setting a negative value in DMACm.DMOFR. The negative value must be in two's complement.

Table 17.6 shows the address update method in each address update mode.

Table 17.6 Address update method in each address update mode

Address update mode	Settings of DMACm.DMAMD.SM[1:0] and DMACm.DMAMD.DM[1:0] for address update modes	Address update method for different SZ[1:0] settings in DMACm.DMTMD		
		SZ[1:0] = 00b	SZ[1:0] = 01b	SZ[1:0] = 10b
Address fixed	00b	Fixed		
Offset addition	01b	+DMACm.DMOFR*1		
Increment	10b	+1	+2	+4
Decrement	11b	-1	-2	-4

Note 1. When setting a negative value in the DMA Offset Register, the value must be in two's complement, obtained by the following formula:
two's complement of a negative offset value = ~ (offset) + 1 (~ = bit inversion)

(1) Basic transfer using offset addition

Figure 17.7 shows an example of address updating using offset addition.

示例：在DMACm.DMSAR的低3位中指定8个字节作为扩展重复区域（DMACm.DMAMD中的SARA[4:0]位=00011b）设置块大小为5的块传输模式（DMACm.DMCRA=00050005h）

传输源地址未指定为块区域
数据大小为8位（DMACm.DMTMD=00b中的SZ[1:0]位）

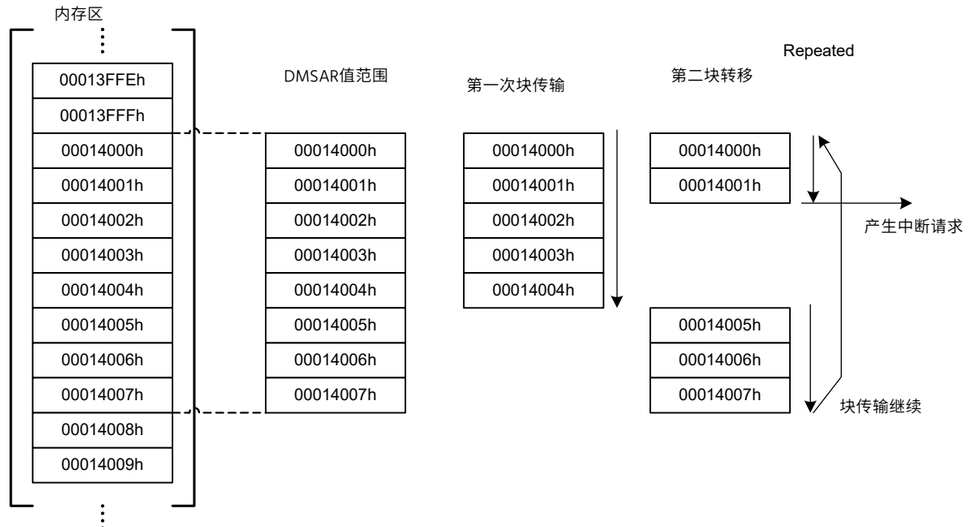


Figure 17.6 块传输模式下的扩展重复区域功能示例

17.3.3 使用偏移的地址更新功能

可以通过固定、递增、递减或添加偏移量来更新源地址和目标地址。选择偏移添加时，DMA偏移寄存器(DMACm.DMOFR)中指定的偏移会在每次DMAC执行一次数据传输时添加到地址。您还可以通过在DMACm.DMOFR中设置负值来减去偏移量。负值必须是二进制补码。

表17.6显示了每种地址更新模式下的地址更新方法。

Table 17.6 各地址更新模式下的地址更新方法

地址更新方式	的设置DMACm.DMAMD.SM[1:0]和DMACm.DMAMD.DM[1:0]用于地址更新模式	不同SZ[1:0]设置的地址更新方法DMACm.DMTMD		
		SZ[1:0] = 00b	SZ[1:0] = 01b	SZ[1:0] = 10b
地址固定	00b	Fixed		
偏移量加法	01b	+DMACm.DMOFR*1		
Increment	10b	+1	+2	+4
Decrement	11b	-1	-2	-4

Note 1. 在DMA偏移寄存器中设置负值时，该值必须是二进制补码，由以下公式获得：负偏移值的二进制补码=~(offset)+1(~=bitinversion)

(1) 使用偏移加法的基本传输

图17.7显示了使用偏移量加法进行地址更新的示例。

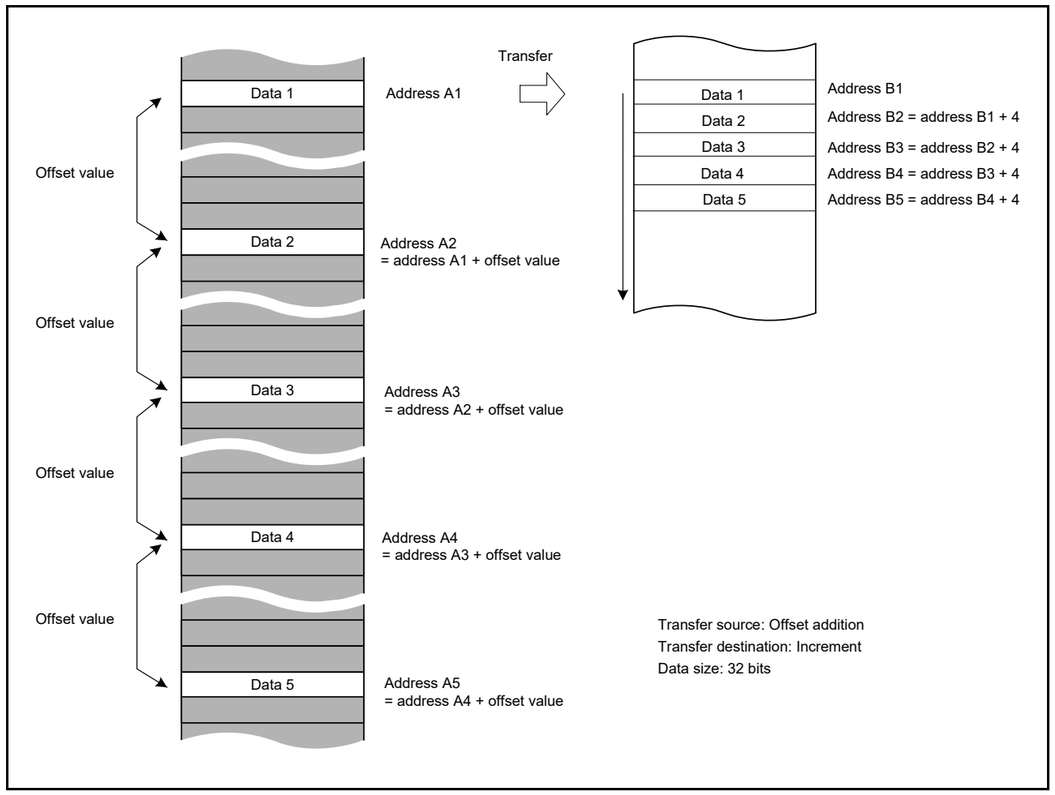


Figure 17.7 Example of address updating through offset addition

In Figure 17.7:

- The transfer data is 32 bits long
- Offset addition is set as the transfer source address update mode
- Increment is set as the transfer destination address update mode.

The second and subsequent data units are each read from the source address obtained by adding the offset value to the previous address. The data read from the addresses at the specified intervals is written to continuous locations on the destination.

(2) Example of XY conversion using offset addition

Figure 17.8 shows XY conversion using offset addition in repeat transfer mode. The settings are as follows:

- DMAC0.DMAMD — Transfer source address update mode: offset addition
- DMAC0.DMAMD — Transfer destination address update mode: destination address is incremented
- DMAC0.DMTMD — Transfer data size select: 32 bits
- DMAC0.DMTMD — Transfer mode select: repeat transfer
- DMAC0.DMTMD — Repeat area select: the source is specified as the repeat area
- DMAC0.DMOFR — Offset address: 10h
- DMAC0.DMCRA — Repeat size: 4h
- DMAC0.DMINT — The repeat size end interrupt is enabled.

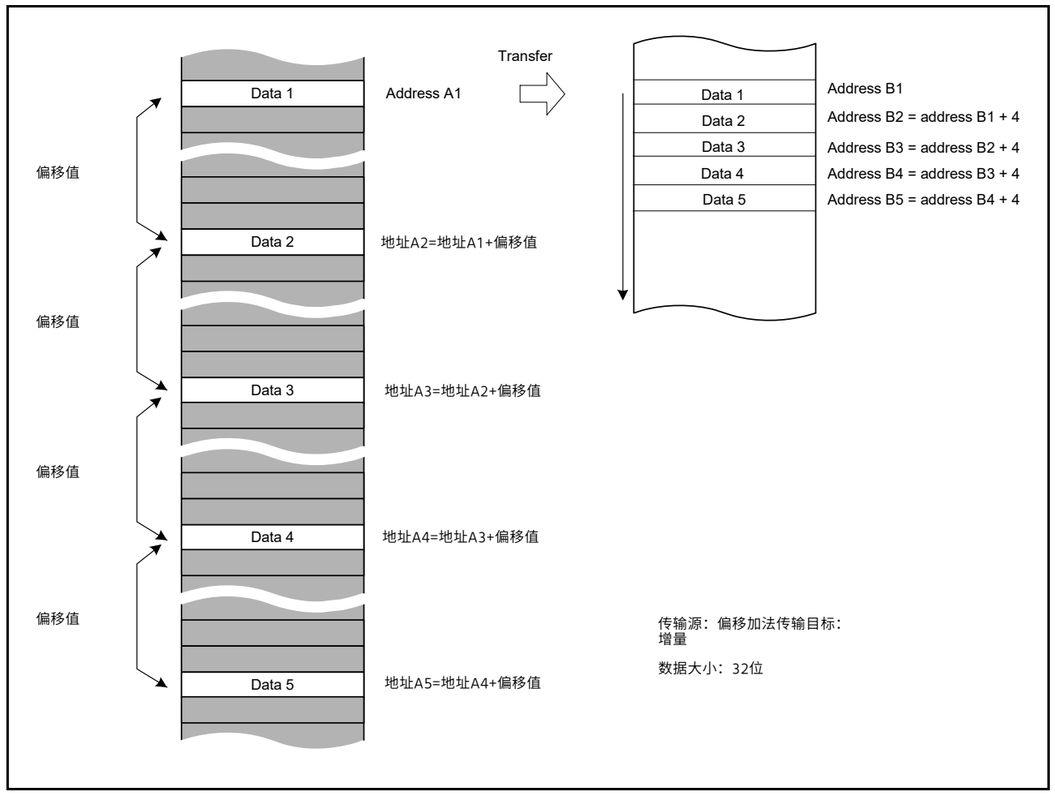


Figure 17.7 通过偏移量添加来更新地址的示例

在图17.7中：

- 传输数据为32位长
- 偏移量加法设置为传输源地址更新方式
- 增量设置为传送目的地地址更新模式。

第二个和随后的数据单元分别从通过将偏移值与前一个地址相加而获得的源地址读取。以指定间隔从地址读取的数据被写入目标上的连续位置。

(2) 使用偏移加法的XY转换示例

图17.8显示了在重复传输模式下使用偏移添加的XY转换。设置如下：

- DMAC0.DMAMD—传输源地址更新模式：偏移量加法
- DMAC0.DMAMD—传输目标地址更新模式：目标地址递增
- DMAC0.DMTMD—传输数据大小选择：32位
- DMAC0.DMTMD—传输模式选择：重复传输
- DMAC0.DMTMD—重复区域选择：源指定为重复区域
- DMAC0.DMOFR — Offset address: 10h
- DMAC0.DMCRA — Repeat size: 4h
- DMAC0.DMINT—启用重复大小结束中断。

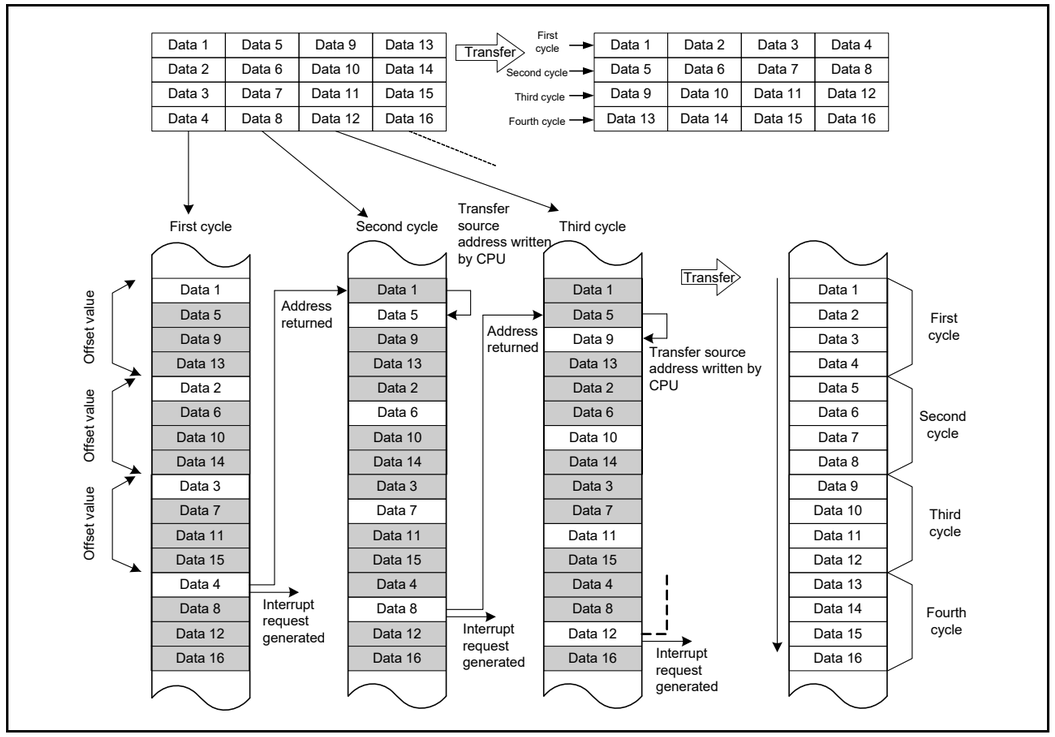


Figure 17.8 XY conversion operation using offset addition in repeat transfer mode

When a transfer starts, the offset value is added to the transfer source address every time data is transferred. The transfer data is written to continuous destination addresses. When data 4 is transferred:

- The repeat size of the transfers is complete
- The transfer source address returns to the transfer start address (the address of data 1 on the transfer source)
- A repeat size end interrupt is requested.

During the time this interrupt pauses the transfer, perform the following:

- DMAC0.DMSAR — Rewrite the DMA transfer source address to the address of data 5 (in this example, the data 1 address + 4)
- DMAC0.DMCNT — Set the DTE bit to 1.

The DMA transfer resumes from the state when the DMA transfer was stopped. The same operations are repeated until the transfer source data is transposed to the destination area (XY conversion).

Figure 17.9 shows the flow of the XY conversion.

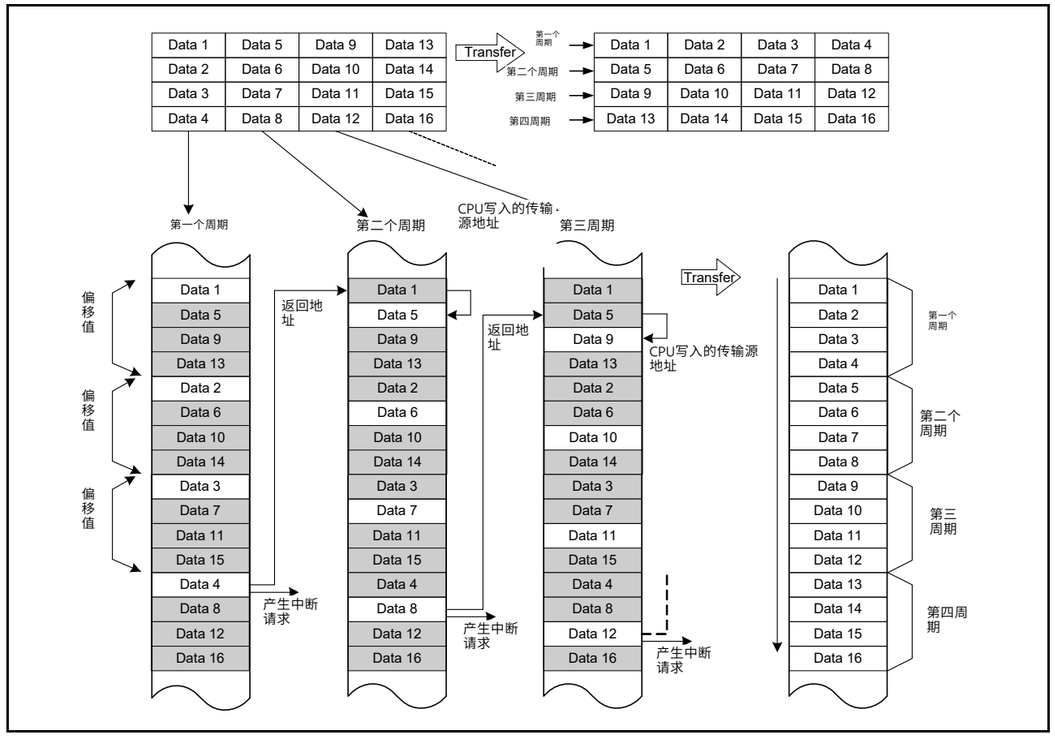


Figure 17.8 重复传输模式下使用偏移加法的XY转换操作

传输开始时，每次传输数据时，都会将偏移值添加到传输源地址。传输数据被写入连续的目标地址。传输数据4时：

- 传输的重复大小已完成
- 传输源地址返回传输起始地址（传输源上数据1的地址）
- 请求重复大小结束中断。

在此中断暂停传输期间，请执行以下操作：

- DMAC0.DMSAR—将DMA传输源地址重写为数据5的地址（在本例中，数据1地址+4）
- DMAC0.DMCNT—将DTE位设置为1。

DMA传输从DMA传输停止时的状态恢复。重复相同的操作，直到将传输源数据转置到目标区域（XY转换）。

图17.9显示了XY转换的流程。

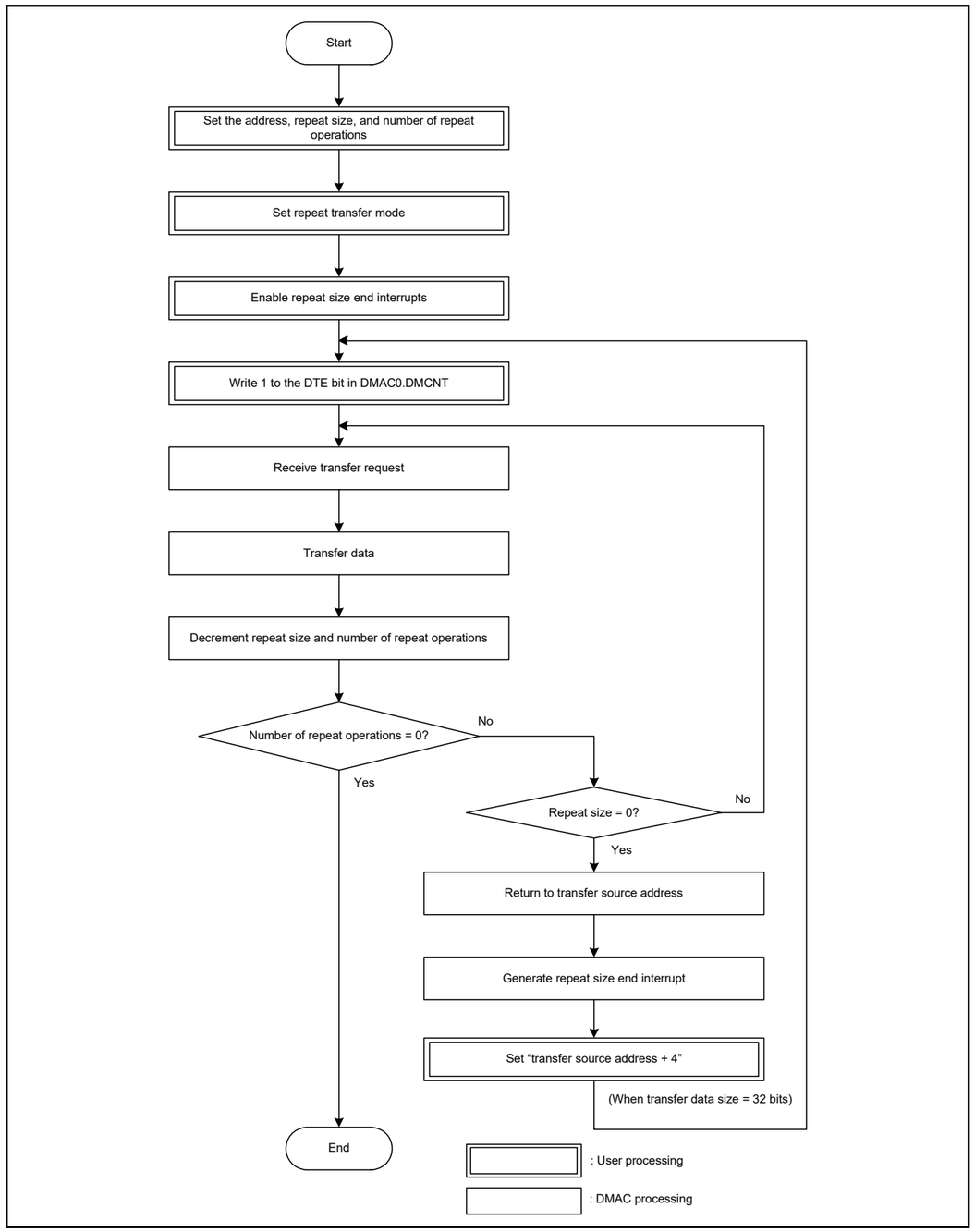


Figure 17.9 XY conversion flow using offset addition in repeat transfer mode

17.3.4 Activation Sources

Software, interrupt requests from the peripheral modules, and external interrupt requests can all be specified as DMAC activation sources. Set the DCTG[1:0] bits in DMACm.DMTMD to select the activation source.

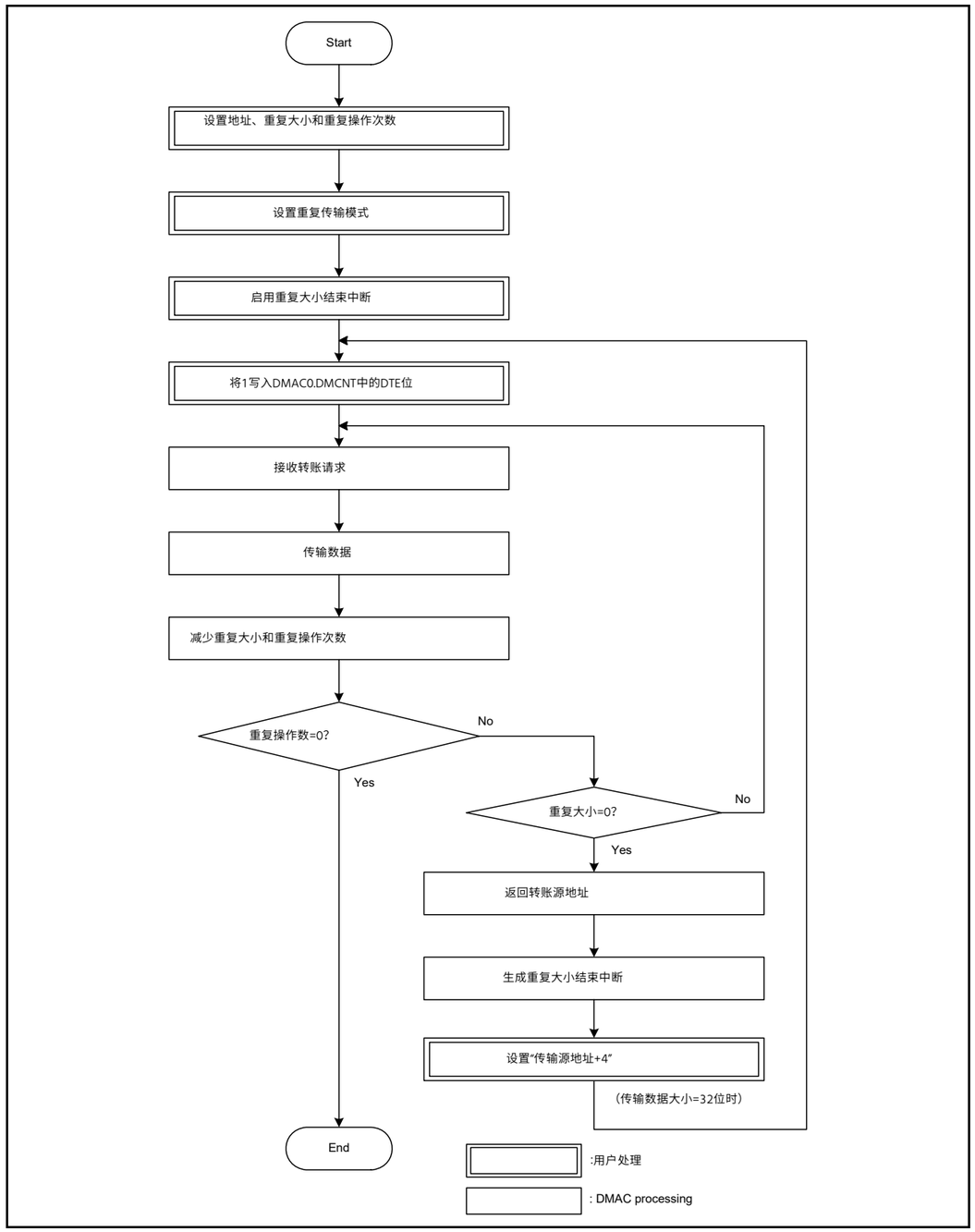


Figure 17.9 在重复传输模式中使用偏移添加的XY转换流程

17.3.4 激活源

软件、外设模块的中断请求和外部中断请求都可以指定为DMAC激活源。设置DMACm.DMTMD中的DCTG[1:0]位以选择激活源。

(1) DMAC activation through software

To start DMA transfer through software:

1. Set the DCTG[1:0] bits in DMACm.DMTMD to 00b.
2. Set the DTE bit in DMACm.DMCNT to 1 (enable DMA transfer).
3. Set the DMST bit in DMAST to 1 (enable DMAC activation).
4. Set the SWREQ bit in DMACm.DMREQ to 1 (request DMA).

When the DMAC is activated by software while the CLRS bit in DMACm.DMREQ is 0, the SWREQ bit in DMACm.DMREQ clears to 0 after data transfer starts in response to a DMA transfer request.

When the DMAC is activated by software while the CLRS bit is 1, SWREQ does not clear to 0 after data transfer starts. A DMA transfer request is issued again after completion of a transfer.

(2) DMAC activation through interrupt requests from on-chip peripheral modules or external interrupt requests

You can specify interrupt requests from on-chip peripheral modules and external interrupt requests as DMAC activation sources. The activation source can be individually selected for each channel in ICU.DELSRn.DELS[8:0] (n = 0 to 7).

To start DMAC transfer through an interrupt request from an on-chip peripheral module or an external interrupt request:

1. Set the DCTG[1:0] bits in DMACm.DMTMD to 01b (select interrupts from the peripheral modules and the external interrupt pins).
2. Set the DTE bit in DMACm.DMCNT to 1 (enable DMA transfer).
3. Set ICU.DELSRn.DSEL to the event number (select the DMAC event link).
4. Set the DMST bit in DMAST to 1 (enable DMAC activation).

For interrupt requests specified as DMAC activation sources, see Table 14.3, Interrupt vector table, in section 14, Interrupt Controller Unit (ICU).

17.3.5 Operation Timing

The following diagrams show the timing with the minimum number of execution cycles.

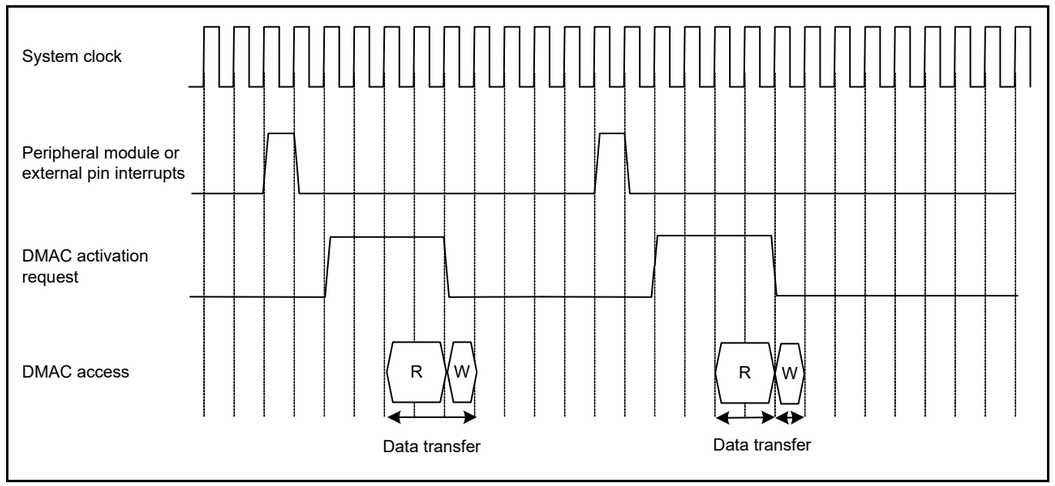


Figure 17.10 DMAC operation timing example 1: DMA activation by interrupt from peripheral module or external interrupt input pin, in normal transfer mode or repeat transfer mode

(1) 通过软件激活DMAC

通过软件启动DMA传输：

1. 将DMACm.DMTMD中的DCTG[1:0]位设置为00b。
2. 将DMACm.DMCNT中的DTE位设置为1（启用DMA传输）。
3. 将DMAST中的DMST位设置为1（启用DMAC激活）。
4. 将DMACm.DMREQ中的SWREQ位设置为1（请求DMA）。

当DMACm.DMREQ中的CLRS位为0时由软件激活DMAC，则DMACm.DMREQ中的SWREQ位在响应DMA传输请求而开始数据传输后，DMACm.DMREQ清零。

当CLRS位为1时由软件激活DMAC时，数据传输开始后SWREQ不会清为0。传输完成后再次发出DMA传输请求。

(2) 通过来自片上外围模块的中断请求或外部中断请求激活DMAC

您可以将来自片上外围模块的中断请求和外部中断请求指定为DMAC激活源。可以为ICU.DELSRn.DELS[8:0]（n=0到7）中的每个通道单独选择激活源。

通过来自片上外围模块的中断请求或外部中断请求启动DMAC传输：

1. 将DMACm.DMTMD中的DCTG[1:0]位设置为01b（从外围模块和外部中断引脚选择中断）。
2. 将DMACm.DMCNT中的DTE位设置为1（启用DMA传输）。
3. 将ICU.DELSRn.DSEL设置为事件编号（选择DMAC事件链接）。
4. 将DMAST中的DMST位设置为1（启用DMAC激活）。

对于指定为DMAC激活源的中断请求，请参见第14节中的表14.3，中断向量表，中断控制器单元（ICU）。

17.3.5 操作时间

下图显示了具有最少执行周期数的时序。

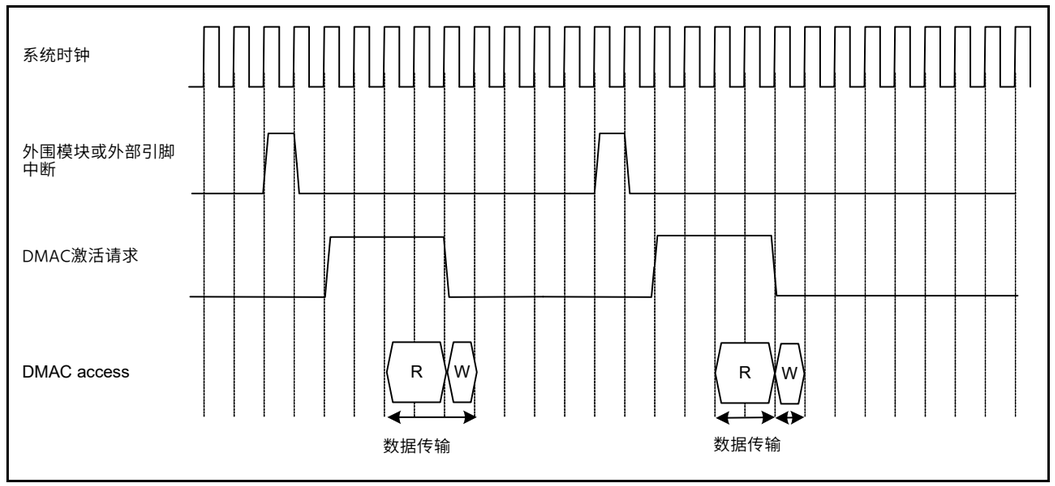


Figure 17.10 DMAC操作时序示例1：通过来自外围模块的中断或外部中断输入引脚激活DMA，处于正常传输模式或重复传输模式

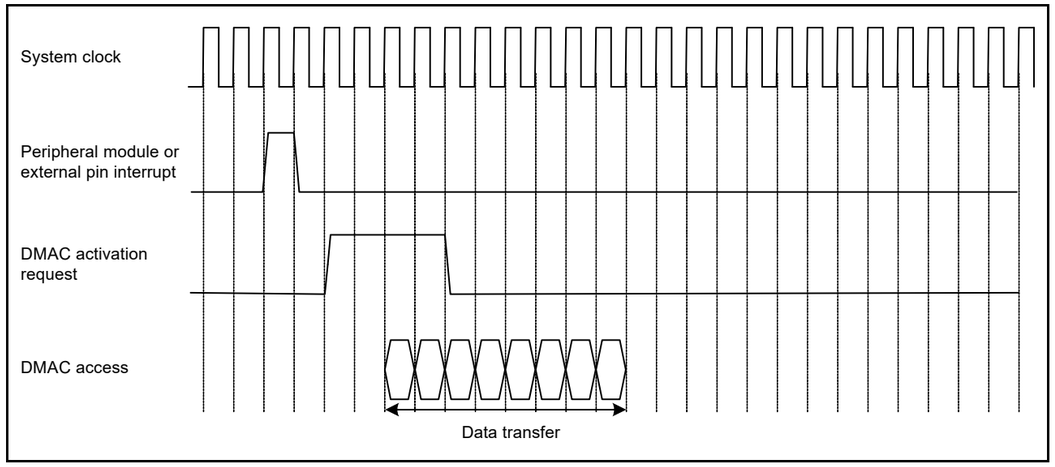


Figure 17.11 DMAC operation timing example 2: DMA activation by interrupt from peripheral module or external interrupt input pin, in block transfer mode with block size = 4

17.3.6 Execution Cycles of DMAC

Table 17.7 lists the execution cycles in one DMAC data transfer operation.

Table 17.7 DMAC execution cycles

Transfer mode	Data transfer (read)	Data transfer (write)
Normal	Cr+Cs+1	Cw+Cs
Repeat	Cr+Cs+1	Cw+Cs
Block*1	P × (Cr+Cs)	P × (Cw+Cs)

Note: P = Block size (DMCRAH register setting).
Cr = Read destination access cycle.
Cw = Data write destination access cycle.
Cs = When accessing SRAMHS and peripheral modules related to system control: 2 cycles.
When accessing elsewhere: 0 cycles.
When a slave bus changes by a read/write data transfer, add 1 more cycle.
Note 1. This is the case when the block size is 2 or more. When the block size is 1, normal transfer cycle applies.

Cr and Cw depend on the access destination. For the number of cycles for each access destination, see section 53, SRAM, section 55, Flash Memory, and section 15.2.3, External Bus. The frequency ratio of the system clock and the peripheral clock is also taken into consideration.

The unit for +1 in the data transfer (read) column is 1 system clock cycle, ICLK. For the operation example, see section 17.3.5, Operation Timing.

The DMAC response time is the time from when the DMAC activation source is detected until the DMAC transfer starts.

Table 17.7 does not include the time until the DMAC data transfer starts after the DMAC activation source becomes active.

17.3.7 Activating the DMAC

Figure 17.12 shows the register setting procedure.

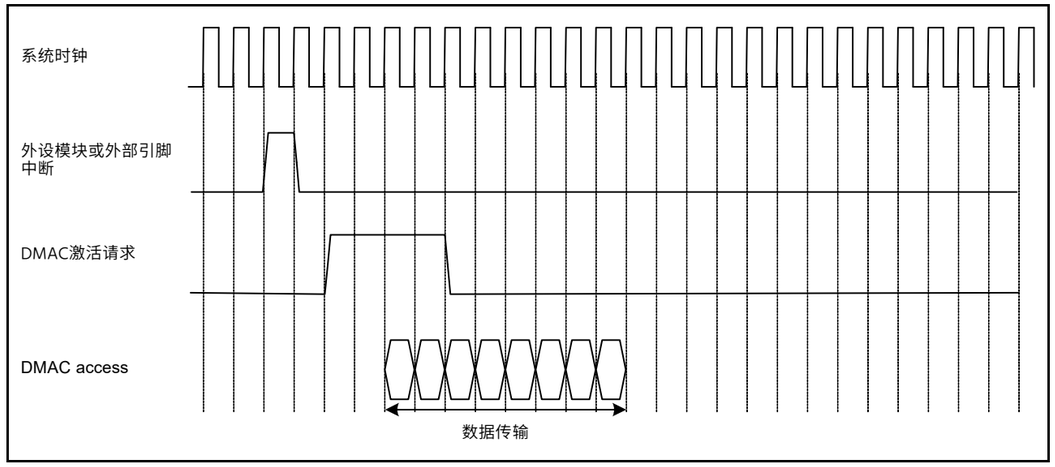


Figure 17.11 DMAC操作时序示例2：通过来自外围模块或外部中断输入引脚的中断激活DMA，在块大小=4的块传输模式下

17.3.6 DMAC的执行周期

表17.7列出了一个DMAC数据传输操作中的执行周期。

Table 17.7 DMAC执行周期

传输模式	数据传输（读取）	数据传输（写入）
Normal	Cr+Cs+1	Cw+Cs
Repeat	Cr+Cs+1	Cw+Cs
Block*1	P × (Cr+Cs)	P × (Cw+Cs)

Note: P=块大小（DMCRAH寄存器设置）。Cr=
读取目标访问周期。
Cw=数据写入目标访问周期。
Cs=访问SRAMHS和与系统控制相关的外围模块时：2个周期。
在其他地方访问时：0个周期。
当从总线因读写数据传输而改变时，再增加1个周期。
Note 1. 当块大小为2或更大时就是这种情况。当块大小为1时，应用正常传输周期。

Cr和Cw取决于访问目的地。对于每个访问目的地的周期数，请参阅第53节，
SRAM，第55节，闪存和第15.2.3节，外部总线。系统时钟和外设时钟的频率比也被考虑在内。

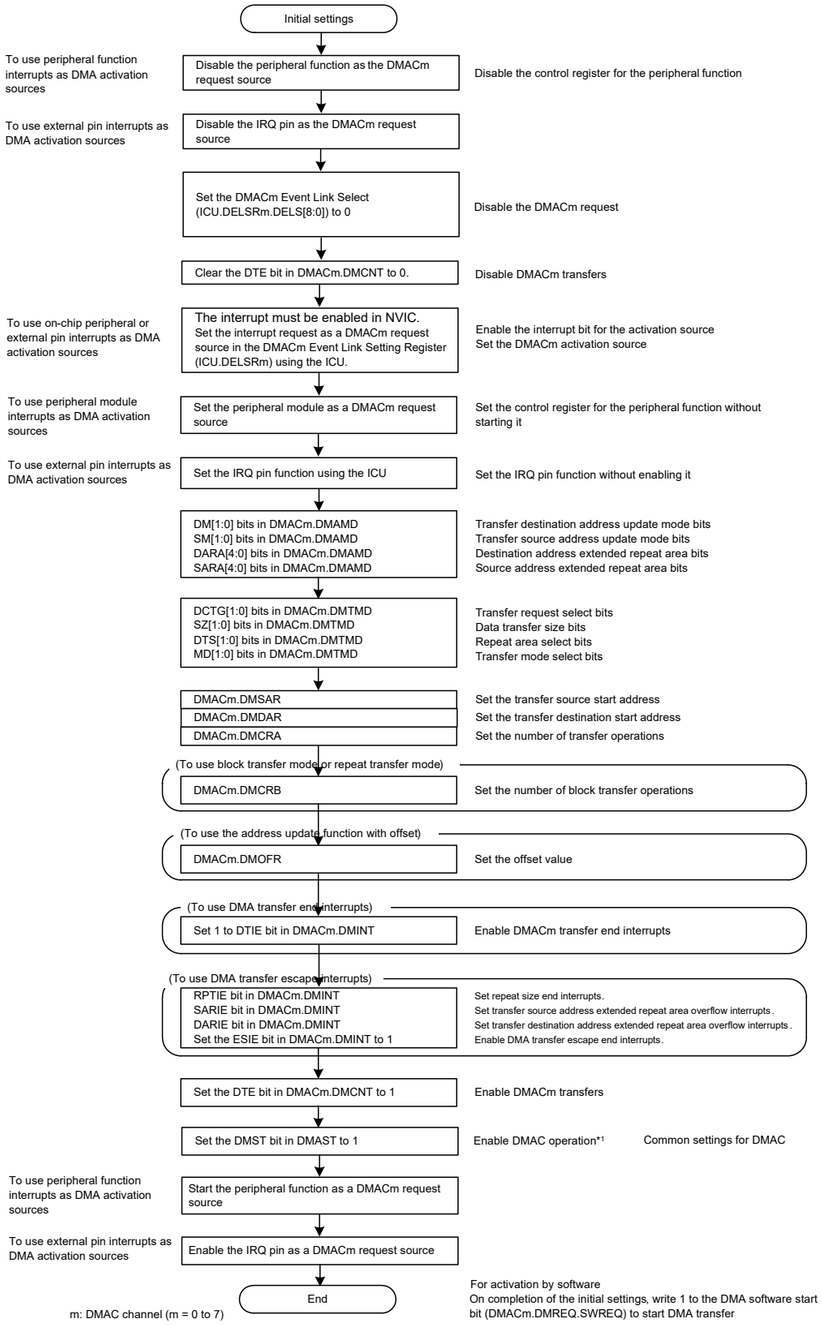
数据传输（读取）列中+1的单位是1个系统时钟周期，ICLK。有关操作示例，请参阅第17.3.5节，操作时序。

DMAC响应时间是从检测到DMAC激活源到DMAC传输开始的时间。

表17.7不包括从DMAC激活源激活到DMAC数据传输开始的时间。

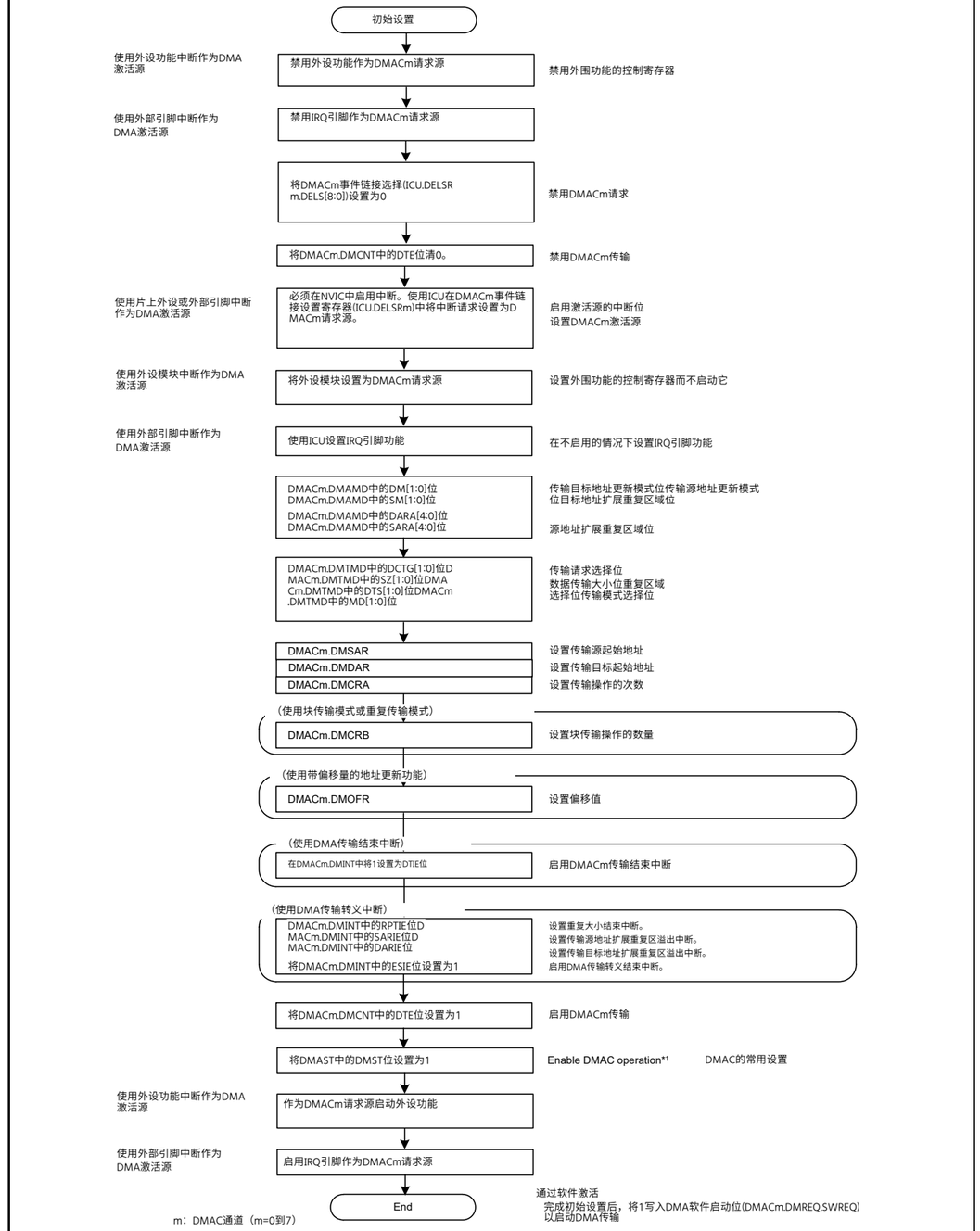
17.3.7 激活DMAC

图17.12显示了寄存器设置过程。



Note 1. Setting of the DMAST.DMST bit does not necessarily have to follow the settings for the individual activation sources.

Figure 17.12 Register setting procedure



Note 1. DMAST.DMST位的设置不一定要遵循各个激活源的设置。

Figure 17.12 注册设置步骤

17.3.8 Starting DMA Transfer

To enable a DMA transfer of channel m, set the DTE bit in DMACm.DMCNT to 1 (DMA transfer enabled) and set the DMST bit in DMAST to 1 (DMAC activation enabled). New activation requests are not accepted during the transfer of another DMAC channel or DTC. When the proceeding transfer is complete, channel arbitration selects the DMA transfer request of the highest priority channel, and DMA transfer of that channel starts. When DMA transfer starts, the ACT flag in DMACm.DMSTS sets to 1 (the DMAC is in the active state).

17.3.9 Registers during DMA Transfer

The DMAC registers are updated by a DMA transfer. The value to be updated differs according to the other settings and the transfer state. The registers that are updated are DMSAR, DMDAR, DMCRA, DMCRB, DMCNT, and DMACm.DMSTS, described in the following sections. For details on register update operations in each transfer mode, see Table 17.3 to Table 17.5.

(1) DMA Source Address Register (DMACm.DMSAR)

After the data for one transfer request is transferred, the contents of DMSAR are updated to the address to be accessed by the next transfer request.

(2) DMA Destination Address Register (DMACm.DMDAR)

After the data for one transfer request is transferred, the contents of DMDAR are updated to the address to be accessed by the next transfer request.

(3) DMA Transfer Count Register (DMACm.DMCRA)

After the data for one transfer request is transferred, the count value is updated. The update operation depends on the transfer mode selected.

(4) DMA Block Transfer Count Register (DMACm.DMCRB)

After the data for one transfer request is transferred, the count value is updated. The update operation depends on the transfer mode selected.

(5) DMA Transfer Enable bit (DMACm.DMCNT.DTE)

The DMACm.DMCNT.DTE bit enables or disables data transfer through register write access. It is automatically cleared to 0 by the DMAC based on the DMA transfer state.

The conditions for clearing this bit by the DMAC are as follows:

- When the specified total volume of data transfer is complete
- When DMA transfer is stopped by a repeat size end interrupt
- When DMA transfer is stopped by an extended repeat area overflow interrupt.

Writing to the registers for channels whose associated DMACm.DMCNT.DTE bit is set to 1 is prohibited except for DMACm.DMCNT. Writes are only possible after the bit clears to 0.

(6) DMA Active flag (DMACm.DMSTS.ACT)

The ACT flag in DMSTS of DMACm indicates whether the DMACm is in the idle or active state. This flag sets to 1 when the DMAC starts data transfer, and clears to 0 when data transfer for one transfer request is complete. Even when DMA transfer is stopped by write of 0 to the DTE bit in DMACm.DMCNT, this flag remains 1 until DMA transfer is complete.

(7) Transfer End Interrupt Flag (DMACm.DMSTS.DTIF)

The DTIF flag in DMACm.DMSTS sets to 1 after DMA transfer of the total transfer size is complete. When both this flag and the DTIE bit in DMACm.DMINT are 1, a transfer end interrupt is requested. This flag sets to 1 when the DMA transfer bus cycle is complete and the ACT flag in DMACm.DMSTS clears to 0, indicating the DMA transfer end. The flag automatically clears to 0 when the DTE bit in DMACm.DMCNT is set to 1 during interrupt handling.

(8) Transfer Escape End Interrupt Flag (DMACm.DMSTS.ESIF)

The ESIF flag in DMACm.DMSTS sets to 1 when a repeat size end interrupt or extended repeat area overflow interrupt

17.3.8 启动DMA传输

要启用通道m的DMA传输，请将DMACm.DMCNT中的DTE位设置为1（启用DMA传输）并将DMAST中的DMST位设置为1（启用DMAC激活）。在传输另一个DMAC通道或DTC期间不接受新的激活请求。当正在进行的传输完成时，通道仲裁选择最高优先级通道的DMA传输请求，并开始该通道的DMA传输。当DMA传输开始时，DMACm.DMSTS中的ACT标志设置为1（DMAC处于活动状态）。

17.3.9 DMA传输期间的寄存器

DMAC寄存器由DMA传输更新。要更新的值根据其他设置和传输状态而有所不同。更新的寄存器是DMSAR、DMDAR、DMCRA、DMRCB、DMCNT和DMACm.DMSTS，如下节所述。每种传输模式下寄存器更新操作的详细信息，请参见表17.3至表17.5。

(1) DMA源地址寄存器(DMACm.DMSAR)

一个传输请求的数据传输完成后，DMSAR的内容被更新为下一个传输请求访问的地址。

(2) DMA目标地址寄存器(DMACm.DMDAR)

一个传输请求的数据被传输后，DMDAR的内容被更新为下一个传输请求要访问的地址。

(3) DMA传输计数寄存器(DMACm.DMCRA)

在传输一个传输请求的数据后，更新计数值。更新操作取决于选择的传输模式。

(4) DMA块传输计数寄存器(DMACm.DMCRB)

在传输一个传输请求的数据后，更新计数值。更新操作取决于选择的传输模式。

(5) DMA传输使能位(DMACm.DMCNT.DTE)

DMACm.DMCNT.DTE位通过寄存器写访问启用或禁用数据传输。它由DMAC根据DMA传输状态自动清零。

DMAC清除该位的条件如下：

- 当指定的总数据传输量完成时
- 当DMA传输因重复大小结束中断而停止时
- 当DMA传输因扩展重复区域溢出中断而停止时。

禁止写入相关DMACm.DMCNT.DTE位设置为1的通道的寄存器，除非DMACm.DMCNT。只有在该位清为0后才能写入。

(6) DMA活动标志(DMACm.DMSTS.ACT)

DMACm的DMSTS中的ACT标志指示DMACm是处于空闲状态还是活动状态。该标志在DMAC开始数据传输时设置为1，并在一个传输请求的数据传输完成时清除为0。即使通过将0写入DMACm.DMCNT中的DTE位来停止DMA传输，该标志仍 保持为1，直到DMA传输完成。

(7) 传输结束中断标志(DMACm.DMSTS.DTIF)

在完成总传输大小的DMA传输后，DMACm.DMSTS中的DTIF标志设置为1。当该标志和DMACm.DMINT中的DTIE位都为1时，请求传输结束中断。当DMA传输总线周期完成并且DMACm.DMSTS中的ACT标志清为0时，该标志设置为1，表示DMA传输结束。在中断处理期间，当DMACm.DMCNT中的DTE位设置为1时，该标志自动清除为0。

(8) 传输转义结束中断标志(DMACm.DMSTS.ESIF)

当重复大小结束中断或扩展重复区域溢出中断时，DMACm.DMSTS中的ESIF标志设置为1

is requested. When this bit and the ESIE bit in DMACm.DMINT are 1, a transfer escape end interrupt is requested. This flag sets to 1 when the bus cycle of the DMA transfer that caused the interrupt request is complete and the ACT flag in DMACm.DMSTS clears to 0, indicating the DMA transfer end. The flag automatically clears to 0 when the DTE bit in DMACm.DMCNT is set to 1 during interrupt handling.

You must set the interrupt control register before sending an interrupt request from the DMAC to the CPU or the DTC. For more information, see section 14, Interrupt Controller Unit (ICU).

17.3.10 Channel Priority

When multiple DMA transfer requests occur, the DMAC determines the priority of channels that have DMA transfer requests.

The priority is fixed as channel 0 > channel 1 > channel 2 > channel 3 > channel 4 > channel 5 > channel 6 > channel 7. (Channel 0 is the highest.)

When a DMA transfer request occurs during data transfer, channel arbitration starts after the final data unit is transferred, and DMA transfer of the highest-priority channel starts.

17.4 Ending DMA Transfer

The operation for ending a DMA transfer depends on the transfer end conditions. When a DMA transfer ends, the DTE bit in DMCNT and the ACT flag in DMACm.DMSTS change from 1 to 0.

17.4.1 Transfer End by Completion of Specified Total Number of Transfer Operations

(1) In normal transfer mode (DMACm.DMTMD.MD[1:0] = 00b)

When the value of DMACm.DMCRAL changes from 1 to 0, DMA transfer ends on the associated channel, the DTE bit in DMACm.DMCNT clears to 0, and the DTIF flag in DMACm.DMSTS sets to 1. If the DTIE bit in DMACm.DMINT is 1 at this time, a transfer end interrupt request is sent to the CPU or the DTC.

(2) In repeat transfer mode (DMACm.DMTMD.MD[1:0] = 01b)

When the value of DMACm.DMCRB changes from 1 to 0, DMA transfer ends on the associated channel, the DTE bit in DMACm.DMCNT clears to 0, and the DTIF flag in DMACm.DMSTS sets to 1. If the DTIE bit in DMACm.DMINT is 1 at this time, an interrupt request is sent to the CPU or the DTC.

(3) In block transfer mode (DMACm.DMTMD.MD[1:0] = 10b)

When the value of DMACm.DMCRB changes from 1 to 0, DMA transfer ends on the associated channel, the DTE bit in DMACm.DMCNT clears to 0, and the DTIF flag in DMACm.DMSTS sets to 1. If the DTIE bit in DMACm.DMINT is 1 at this time, an interrupt request is sent to the CPU or the DTC.

You must set the interrupt control register before sending an interrupt request from the DMAC to the CPU or the DTC. For more information, see section 14, Interrupt Controller Unit (ICU).

17.4.2 Transfer End by Repeat Size End Interrupt

In repeat transfer mode, if the RPTIE bit in DMACm.DMINT is 1, a repeat size end interrupt is requested when transfer of a single repeat size of data is complete. The DTE bit in DMACm.DMCNT clears to 0 and the ESIF flag in DMACm.DMSTS sets to 1. If the ESIE bit in DMACm.DMINT is 1 at this time, an interrupt request is sent to the CPU or the DTC. To resume the transfer, write 1 to the DTE bit in DMACm.DMCNT.

A repeat size end interrupt can also be requested in block transfer mode. When transfer of a single block size of data is complete, the interrupt is requested in the same way as in repeat transfer mode.

You must set the interrupt control register before sending an interrupt request from the DMAC to the CPU or the DTC. For more information, see section 14, Interrupt Controller Unit (ICU).

17.4.3 Transfer End by Interrupt on Extended Repeat Area Overflow

When an overflow on the extended repeat area occurs while the extended repeat area is specified and the SARIE or DARIE bit in DMACm.DMINT is 1, an extended repeat area overflow interrupt is requested. The DMA transfer is terminated, the DTE bit in DMACm.DMCNT clears to 0, and the ESIF flag in DMACm.DMSTS sets to 1. If the ESIE

被要求。当该位和DMACm.DMINT中的ESIE位为1时，请求传输转义结束中断。当导致中断请求的DMA传输的总线周期完成并且DMACm.DMSTS中的ACT标志清为0时，该标志设置为1，表示DMA传输结束。当DTE位在

DMACm.DMCNT在中断处理期间设置为1。

在从DMAC向CPU或DTC发送中断请求之前，您必须设置中断控制寄存器。
有关详细信息，请参阅第14节，中断控制器单元(ICU)。

17.3.10 频道优先级

当出现多个DMA传输请求时，DMAC确定有DMA传输请求的通道的优先级。

优先级固定为通道0>通道1>通道2>通道3>通道4>通道5>通道6>通道7。（通道0最高。）

当数据传输过程中出现DMA传输请求时，在传输完最后一个数据单元后开始通道仲裁，并开始最高优先级通道的DMA传输。

17.4 结束DMA传输

结束DMA传输的操作取决于传输结束条件。当DMA传输结束时，DMCNT中的DTE位和DMACm.DMSTS中的ACT标志从1变为0。

17.4.1 完成指定的转移操作总数后转移结束

(1) 在正常传输模式下（DMACm.DMTMD.MD[1:0]=00b）

当DMACm.DMCRAL的值从1变为0时，DMA传输在相关通道上结束，DMACm.DMCNT中的DTE位清为0，并且DMACm.DMSTS中的DTIF标志设置为1。如果DMACm中的DTIE位此时.DMINT为1，向CPU或DTC发送传输结束中断请求。

(2) 在重复传输模式下（DMACm.DMTMD.MD[1:0]=01b）

当DMACm.DMCRB的值从1变为0时，DMA传输在关联通道上结束，DMACm.DMCNT中的DTE位清为0，DMACm.DMSTS中的DTIF标志设置为1。如果DMACm中的DTIE位此时.DMINT为1，向CPU或DTC发送中断请求。

(3) 在块传输模式下（DMACm.DMTMD.MD[1:0]=10b）

当DMACm.DMCRB的值从1变为0时，DMA传输在关联通道上结束，DMACm.DMCNT中的DTE位清为0，DMACm.DMSTS中的DTIF标志设置为1。如果DMACm中的DTIE位此时.DMINT为1，向CPU或DTC发送中断请求。

在从DMAC向CPU或DTC发送中断请求之前，您必须设置中断控制寄存器。
有关详细信息，请参阅第14节，中断控制器单元(ICU)。

17.4.2 按重复大小结束传输结束中断

在重复传输模式下，如果DMACm.DMINT中的RPTIE位为1，则在单个重复大小的数据传输完成时请求重复大小结束中断。DMACm.DMCNT中的DTE位清为0，DMACm.DMSTS中的ESIF标志位设置为1。如果此时DMACm.DMINT中的ESIE位为1，则向CPU或DTC发送中断请求。要恢复传输，请将1写入DMACm.DMCNT中的DTE位。

在块传输模式下也可以请求重复大小结束中断。当单个块大小的数据传输完成时，以与重复传输模式相同的方式请求中断。

在从DMAC向CPU或DTC发送中断请求之前，您必须设置中断控制寄存器。
有关详细信息，请参阅第14节，中断控制器单元(ICU)。

17.4.3 扩展重复区溢出中断传输结束

如果在指定扩展重复区域且DMACm.DMINT中的SARIE或DARIE位为1时扩展重复区域发生溢出，则请求扩展重复区域溢出中断。DMA传输终止，DMACm.DMCNT中的DTE位清为0，DMACm.DMSTS中的ESIF标志设置为1。如果ESIE

bit in DMACm.DMINT is 1 at this time, an interrupt request is sent to the CPU or the DTC.

If this interrupt is requested during a read cycle, the subsequent write cycle is performed. In block transfer mode, if the interrupt is requested during a 1-block transfer, the remaining data in the block is transferred before transfer stops.

Before sending an interrupt request from the DMAC to the CPU or the DTC, the interrupt control register must be set. For more information, see section 14, Interrupt Controller Unit (ICU).

17.4.4 Precautions for the End of DMA Transfer

A DMA activation request source might occur in the next request after a DMA transfer completes. If this happens, the DMA transfer starts and the DMA activation request is held in DMAC. To prevent this, stop the DMA activation requests by clearing the DELSRn.DSELS[8:0] bits in the ICU to 0.

When the DMA activation request occurs after the last round of the DMA transfer is generated, clear the DMA activation request by setting ICU.DELSRm.IR bit to 0.

17.5 Interrupts

Each DMAC channel can output an interrupt request (DMACm_INT) to the CPU or DTC after transfer for one request is complete. When the transfer destination is the external bus, an interrupt request is generated after completion of a data write to the write buffer, and not to the actual transfer destination.

Table 17.8 lists the interrupt sources and their associated status flags and enable bits. Figure 17.13 shows the schematic logic diagram of the interrupt outputs (DMAC0 to DMAC7). Figure 17.14 shows the DMAC interrupt handling routine for resuming and terminating DMA transfers.

Table 17.8 Associations among interrupt sources, interrupt status flags, and interrupt enable bits

Interrupt sources		Interrupt enable bits	Interrupt status flags	Request output enable bits
Transfer end		—	DMACm.DMSTS.DTIF	DMACm.DMINT.DTIE
Escape transfer end	Repeat size end	DMACm.DMINT.RPTIE	DMACm.DMSTS.ESIF	DMACm.DMINT.ESIE
	Source address extended repeat area overflow	DMACm.DMINT.SARIE		
	Destination address extended repeat area overflow	DMACm.DMINT.DARIE		

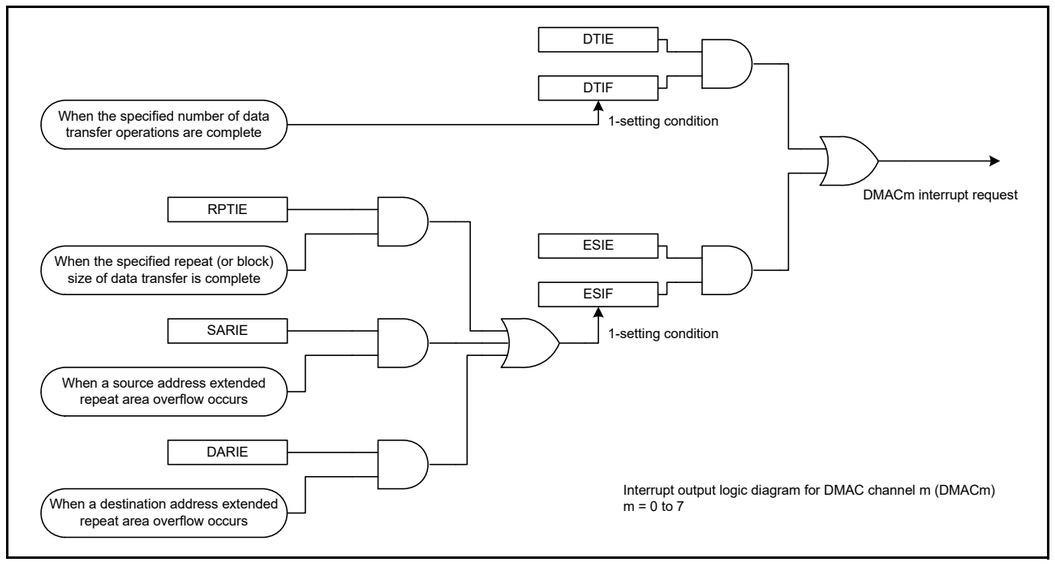


Figure 17.13 Schematic logic diagram of interrupt outputs for DMAC0 to DMAC7

此时DMACm.DMINT中的位为1，向CPU或DTC发送中断请求。

如果在读周期内请求此中断，则执行后续写周期。在块传输模式下，如果在1块传输期间请求中断，则在传输停止之前传输块中剩余的数据。

在从DMAC向CPU或DTC发送中断请求之前，必须设置中断控制寄存器。
有关详细信息，请参阅第14节，中断控制器单元(ICU)。

17.4.4 DMA传输结束的注意事项

DMA传输完成后的下一个请求中可能会出现DMA激活请求源。如果发生这种情况，
DMA传输开始，DMA激活请求保存在DMAC中。为防止这种情况发生，通过将ICU中的DELSRn.DSELS[8:0]位清除为0来停止DMA激活请求。

当最后一轮DMA传输产生后发生DMA激活请求时，通过将ICU.DELSRm.IR位设置为0来清除DMA激活请求。

17.5 Interrupts

每个DMAC通道可以在一个请求的传输完成后向CPU或DTC输出一个中断请求(DMACm_INT)。当传输目的地是外部总线时，在写入缓冲区的数据写入完成后会产生中断请求，而不是实际传输目的地。

表17.8列出了中断源及其相关的状态标志和使能位。图17.13显示了中断输出（DMAC0到DMAC7）的示意逻辑图。图17.14显示了用于恢复和终止DMA传输的DMAC中断处理程序。

Table 17.8 中断源、中断状态标志和中断使能位之间的关联

中断源		中断使能位	中断状态标志	请求输出使能位
转账结束		—	DMACm.DMSTS.DTIF	DMACm.DMINT.DTIE
逃生转移结束	重复大小结束	DMACm.DMINT.RPTIE	DMACm.DMSTS.ESIF	DMACm.DMINT.ESIE
	源地址扩展重复区溢出	DMACm.DMINT.SARIE		
	目的地址扩展重复区溢出	DMACm.DMINT.DARIE		

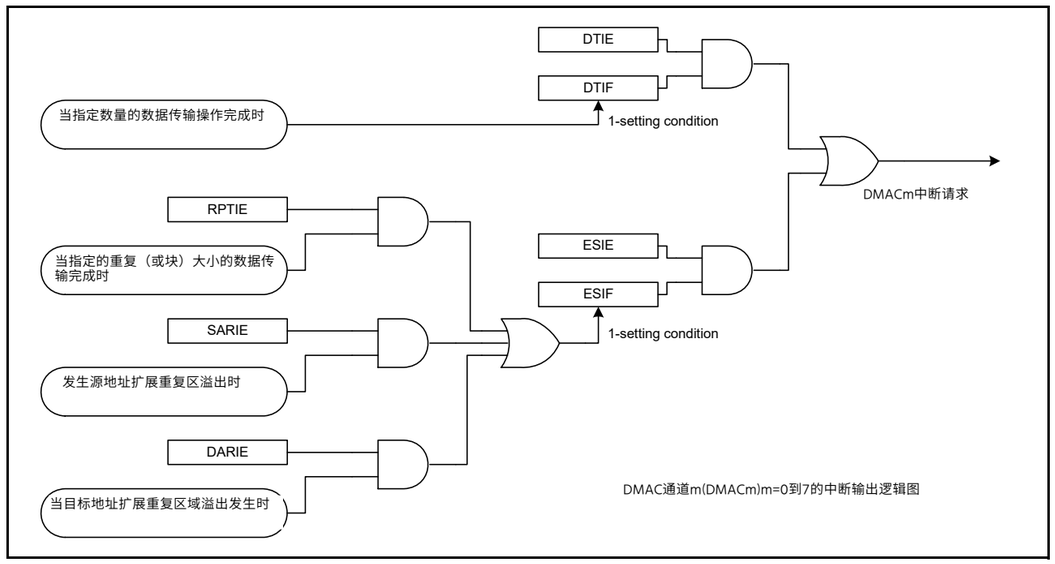


Figure 17.13 DMAC0到DMAC7的中断输出逻辑示意图

Different procedures are used for canceling an interrupt to restart a DMA transfer in the following cases:

- When terminating a DMA transfer
- When continuing a DMA transfer.

(1) When terminating a DMA transfer

Write 0 to the DTIF flag in DMACm.DMSTS to clear a transfer end interrupt, and to the ESIF flag in DMACm.DMSTS to clear a repeat size interrupt or an extended repeat area overflow interrupt. DMACm remains in the stopped state. When starting another DMA transfer, set the appropriate registers and set the DTE bit in DMACm.DMCNT to 1 (DMA transfer enabled).

(2) When continuing a DMA transfer

Write 1 to the DTE bit in DMACm.DMCNT. The ESIF flag in DMSTS of DMACm automatically clears to 0 (interrupt source cleared), and the DMA transfer resumes.

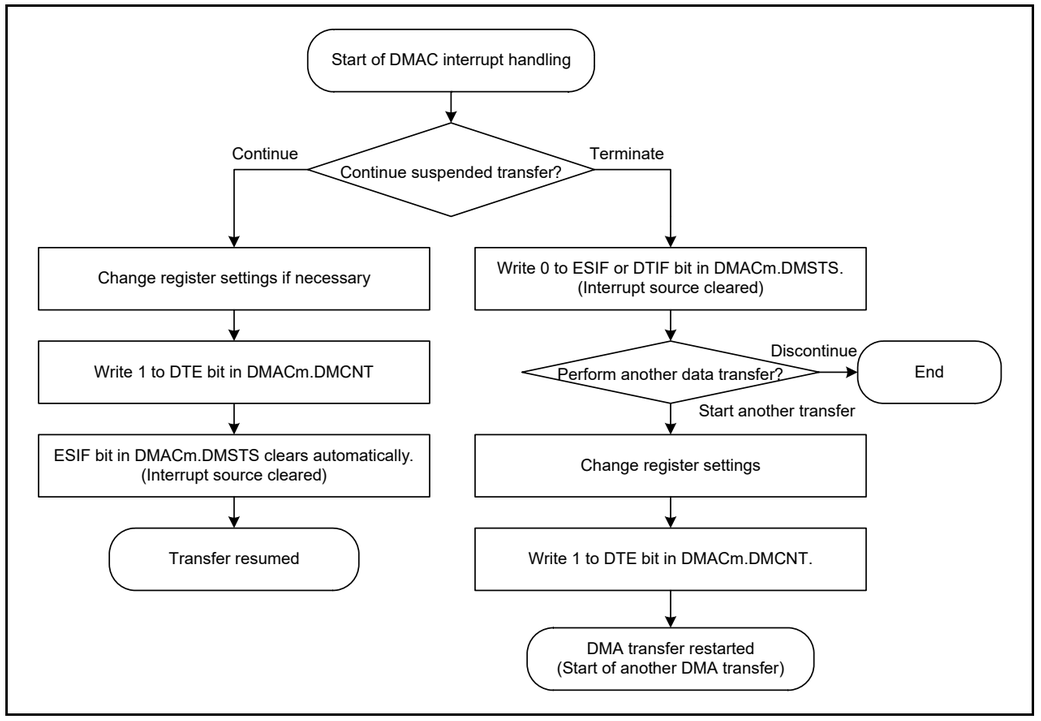


Figure 17.14 DMAC interrupt handling routine to resume or terminate a DMA transfer

17.6 Event Link

Each DMAC channel outputs an event link request signal (DMACm_INT) every time it completes a data transfer, or a block transfer in block transfer mode. When the transfer destination is the external bus, the signal is generated when writing to the write buffer is accepted. For more information, see section 19, Event Link Controller (ELC).

17.7 Low-Power Functions

Before entering the module-stop state, Software Standby mode, or Deep Software Standby mode, you must first clear the DMST bit in DMAST to 0 (DMAC suspended) and use the settings in the sections that follow.

(1) Module-stop function

Writing 1 to the MSTPA22 bit in MSTPCRA enables the module-stop function of the DMAC. If a DMA transfer is in

在以下情况下，不同的程序用于取消中断以重新启动DMA传输：

- 终止DMA传输时
- 继续DMA传输时。

(1) 终止DMA传输时

将0写入DMACm.DMSTS中的DTIF标志以清除传输结束中断，并写入DMACm.DMSTS中的ESIF标志以清除重复大小中断或扩展重复区域溢出中断。DMACm保持在停止状态。当开始另一个DMA传输时，设置适当的寄存器并将DMACm.DMCNT中的DTE位设置为1（启用DMA传输）。

(2) 继续DMA传输时

将1写入DMACm.DMCNT中的DTE位。DMACm的DMSTS中的ESIF标志位自动清零（中断源清零），DMA传输恢复。

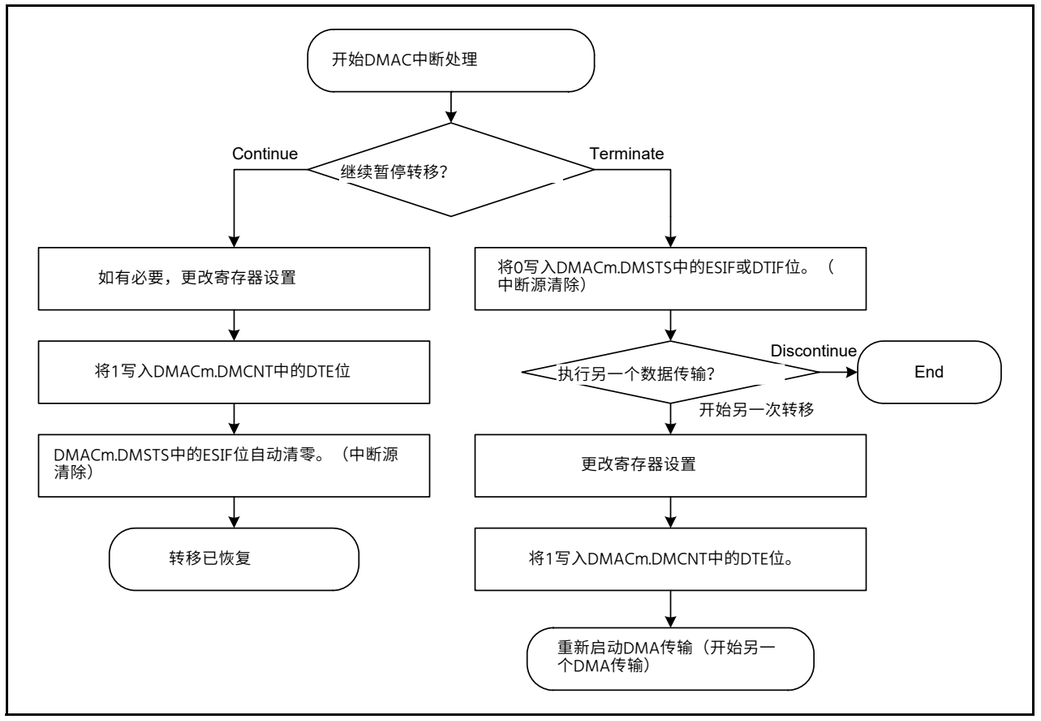


Figure 17.14 用于恢复或终止DMA传输的DMAC中断处理例程

17.6 活动链接

每个DMAC通道在每次完成数据传输或块传输模式下的块传输时都会输出一个事件链接请求信号(DMACm_INT)。当传输目标是外部总线时，当接受写入写缓冲器时产生信号。有关详细信息，请参阅第19节，事件链接控制器(ELC)。

17.7 Low-Power Functions

在进入模块停止状态、软件待机模式或深度软件待机模式之前，您必须先清除DMAST中的DMST位为0（DMAC暂停）并使用以下部分中的设置。

(1) Module-stop function

向MSTPCRA中的MSTPA22位写入1使能DMAC的模块停止功能。如果DMA传输在

progress when 1 is written to MSTPA22, the transition to the module-stop state continues after DMA transfer ends. Access to the DMAC registers is prohibited while MSTPA22 is 1. Writing 0 to the MSTPA22 bit releases the DMAC from the module-stop state.

(2) Software Standby and Deep Software Standby modes

Use the settings described in section 11.7.1, Transition to Software Standby Mode and section 11.9.1, Transition to Deep Software Standby Mode.

If DMA transfer operations are in progress when the WFI instruction is executed, the DMA transfer completes before the transition to Software Standby mode or Deep Software Standby mode.

(3) Notes on the low-power function

For information on the WFI instruction and register settings, see section 11.10.7, Timing of WFI Instruction.

To perform a DMA transfer after returning from a low power mode, set the DMST bit in DMAST to 1 again. To use a request that is generated in Software Standby mode as an interrupt request to the CPU but not as a DMAC startup request, specify the CPU as the interrupt request destination, as described in section 14.4.2, Selecting Interrupt Request Destinations, then execute the WFI instruction.

17.8 Usage Notes

17.8.1 DMA Transfer to External Devices

In a DMA transfer to an external device, the ACT flag in DMACm.DMSTS may be cleared to 0 (DMAC transfer suspended) from the beginning of the final data write to the end of the external bus access.

17.8.2 Access to Registers during DMA Transfer

Do not write to the following registers of DMACm while the ACT flag in DMSTS of the associated channel is set to 1 (DMAC active state) or the DTE bit in DMCNT of the associated channel is set to 1 (DMA transfer enabled):

- DMSAR
- DMDAR
- DMCRA
- DMCRB
- DMTMD
- DMINT
- DMAMD
- DMOFR.

17.8.3 DMA Transfer to Reserved Areas

DMA transfer to reserved areas is prohibited. If such an access is made, transfer results are not guaranteed. For details on reserved areas, see section 4, Address Space.

17.8.4 Setting the DMAC Event Link Setting Register of the Interrupt Controller Unit (ICU) (ICU.DELSRn)

Before setting the DMAC Event Link Setting Register (ICU.DELSRn), make sure the DMA transfer enable bit (DMACm.DMCNT.DTE) is cleared to 0, disabling DMA transfer. Additionally, ensure that the DTC activation enable register (ICU.IELSRn.DTCE) associated with the event number set in the ICU.DELSRn register is not set to 1. For details on ICU.IELSRn.DTCE and ICU.DELSRn, see section 14, Interrupt Controller Unit (ICU).

17.8.5 Suspending or Restarting DMA Activation

To suspend a DMA activation request, write 0 to the DMAC Event Link select bits (ICU.DELSRn.DELS[8:0]). To restart the DMA transfer, write the event number to the ICU.DELSRn.DELS[8:0] bit with the settings shown in section 17.3.7, Activating the DMAC.

向MSTPA22写入1时，在DMA传输结束后继续转换到模块停止状态。当MSTPA22为1时，禁止访问DMAC寄存器。将0写入MSTPA22位可将DMAC从模块停止状态释放。

(2) 软件待机和深度软件待机模式

使用第11.7.1节，转换到软件待机模式和第11.9.1节，转换到深度中描述的设置软件待机模式。

如果在执行WFI指令时DMA传输操作正在进行，则DMA传输在转换到软件待机模式或深度软件待机模式之前完成。

(3) 低功耗功能注意事项

有关WFI指令和寄存器设置的信息，请参阅第11.10.7节，WFI指令的时序。

要在从低功耗模式返回后执行DMA传输，请将DMAST中的DMST位再次设置为1。要将在软件待机模式下生成的请求用作对CPU的中断请求但不用作DMAC启动请求，请指定CPU作为中断请求目标，如第14.4.2节，选择中断请求目标中所述，然后执行WFI指令。

17.8 使用说明

17.8.1 DMA传输到外部设备

在向外部设备进行DMA传输时，从最后一次数据写入开始到外部总线访问结束，DMACm.DMSTS中的ACT标志可能被清除为0（DMAC传输暂停）。

17.8.2 在DMA传输期间访问寄存器

当相关通道的DMSTS中的ACT标志设置为1（DMAC活动状态）或相关通道的DMCNT中的DTE位设置为1（启用DMA传输）时，请勿写入DMACm的以下寄存器：

- DMSAR
- DMDAR
- DMCRA
- DMCRB
- DMTMD
- DMINT
- DMAMD
- DMOFR.

17.8.3 DMA传输到保留区域

禁止对保留区域进行DMA传输。如果进行此类访问，则无法保证传输结果。有关保留区域的详细信息，请参阅第4节，地址空间。

17.8.4 设置中断控制器单元(ICU)(ICU.DELSRn)的DMAC事件链接设置寄存器

在设置DMAC事件链接设置寄存器(ICU.DELSRn)之前，请确保DMA传输启用位(DMACm.DMCNT.DTE)被清除为0，禁用DMA传输。此外，请确保与ICU.DELSRn寄存器中设置的事件编号相关的DTC激活启用寄存器(ICU.IELSRn.DTCE)未设置为1。有关ICU.IELSRn.DTCE和ICU.DELSRn的详细信息，请参阅第14节，中断控制器单元（ICU）。

17.8.5 暂停或重新启动DMA激活

要暂停DMA激活请求，请将0写入DMAC事件链接选择位(ICU.DELSRn.DELS[8:0])。要重新启动DMA传输，请将事件编号写入ICU.DELSRn.DELS[8:0]位，设置见第17.3.7节，激活DMAC。

18. Data Transfer Controller (DTC)

18.1 Overview

The Data Transfer Controller (DTC) performs data transfers when activated by an interrupt request.

Table 18.1 lists the DTC specifications and Figure 18.1 shows a block diagram.

Table 18.1 DTC specifications

Parameter	Specifications
Transfer modes	• Normal transfer mode A single activation leads to a single data transfer. • Repeat transfer mode A single activation leads to a single data transfer. The transfer address returns to the start address after the number of data transfers reaches the specified repeat size. The maximum number of repeat transfers is 256 and the maximum data transfer size is 256 × 32 bits (1024 bytes). • Block transfer mode A single activation leads to a transfer of a single block. The maximum block size is 256 × 32 bits = 1024 bytes.
Transfer channel	• Channel transfer can be associated with the interrupt source (transferred by a DTC activation request from the ICU) • Multiple data units can be transferred on a single activation source (chain transfer) • Chain transfers can be set to either execute when the counter is 0 or always execute
Transfer space	• 4 GB (0000 0000h to FFFF FFFFh, excluding reserved areas)
Data transfer units	• Single data unit: 1 byte (8 bits), 1 halfword (16 bits), or 1 word (32 bits) • Single block size: 1 to 256 data units
CPU interrupt source	• An interrupt request can be generated to the CPU on a DTC activation interrupt • An interrupt request can be generated to the CPU after a single data transfer • An interrupt request can be generated to the CPU after a data transfer of a specified volume.
Event link function	An event link request is generated after one data transfer (for block, after one block transfer)
Read skip	Read of transfer information can be skipped
Write-back skip	When the transfer source or destination address is specified as fixed, write-back of transfer information can be skipped
Module-stop function	Module-stop state can be set to reduce power consumption

18. 数据传输控制器(DTC)

18.1 Overview

数据传输控制器(DTC)在被中断请求激活时执行数据传输。

表18.1列出了DTC规范，图18.1显示了框图。

Table 18.1 DTC specifications

Parameter	Specifications
传输模式	正常传输模式 单次激活导致单次数据传输。 重复传输模式 单次激活导致单次数据传输。 数据传输次数达到指定的重复大小后，传输地址返回起始地址。最大重复传输次数为256，最大数据传输大小为256×32位（1024字节）。 块传输模式 单个激活导致单个块的传输。最大块大小为256×32位=1024字节。
传输通道	通道传输可以与中断源相关联（通过来自ICU的DTC激活请求传输） 多个数据单元可以在单个激活源上传输（链传输） 链传输可以设置为在计数器运行时执行0或始终执行
转移空间	4GB（00000000h到FFFFFFFFh，不包括保留区域）
数据传输单元	单个数据单元：1个字节（8位）、1个半字（16位）或1个字（32位） 单个块大小：1到256个数据单元
CPU中断源	可以在DTC激活中断时向CPU生成中断请求 可以在单次数据传输后向CPU生成中断请求 可以在指定量的数据传输后向CPU生成中断请求。
事件链接功能	一次数据传输后产生事件链接请求（对于块，在一次块传输后）
阅读跳过	可以跳过读取传输信息
Write-back skip	当传输源或目标地址指定为固定时，可以跳过传输信息的回写
Module-stop function	可设置模块停止状态以降低功耗

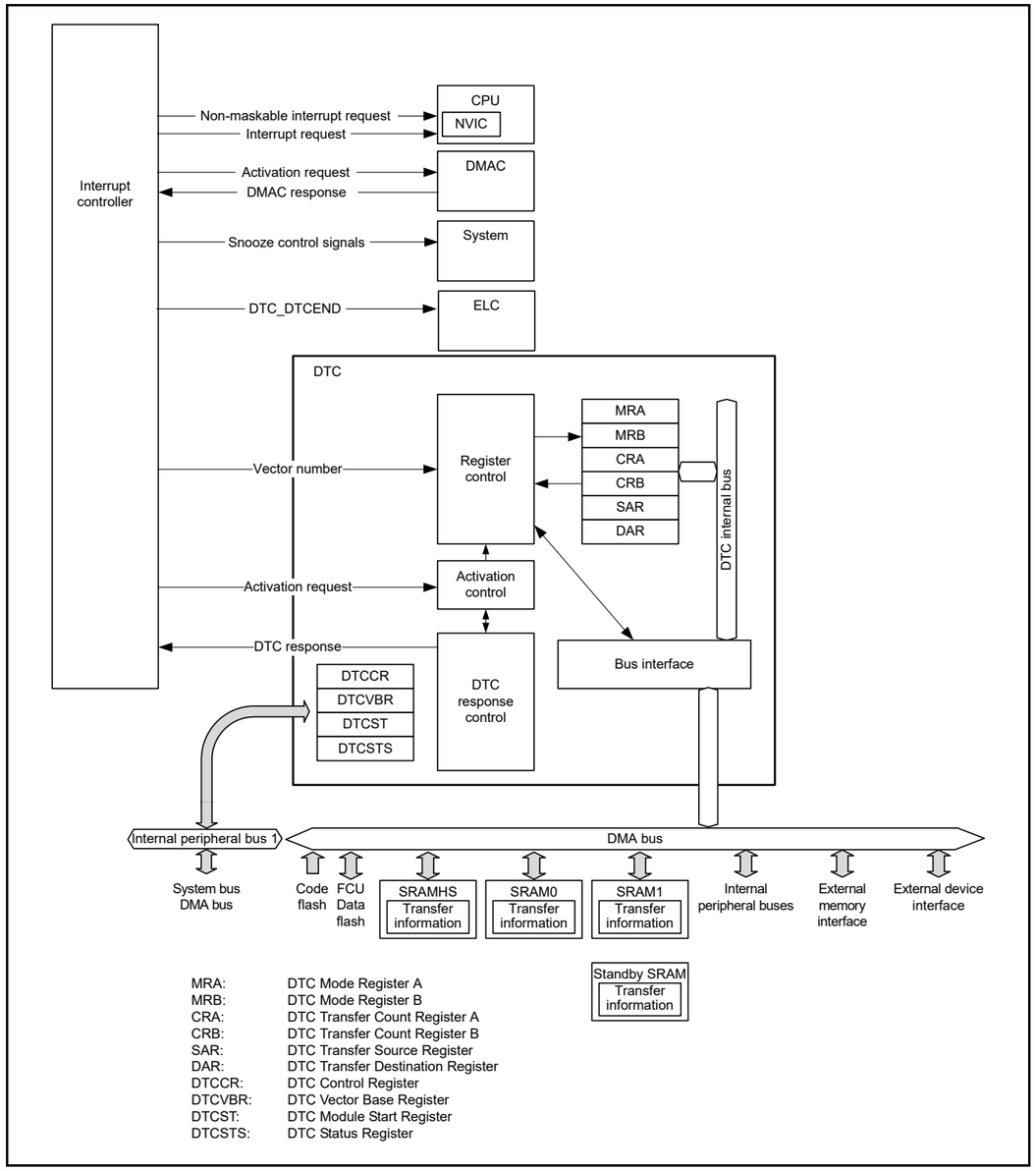


Figure 18.1 DTC block diagram

See 14.1 Overview, in section 14, Interrupt Controller Unit (ICU), for the connections between the DTC and NVIC (in the CPU).

18.2 Register Descriptions

MRA, MRB, SAR, DAR, CRA, and CRB are all DTC internal registers that cannot be directly accessed from the CPU. Values to be set in these DTC internal registers are placed in the SRAM area as transfer information. When an activation request is generated, the DTC reads the transfer information from the SRAM area and sets it in its internal registers. After the data transfer ends, the internal register contents are written back to the SRAM area as transfer information.

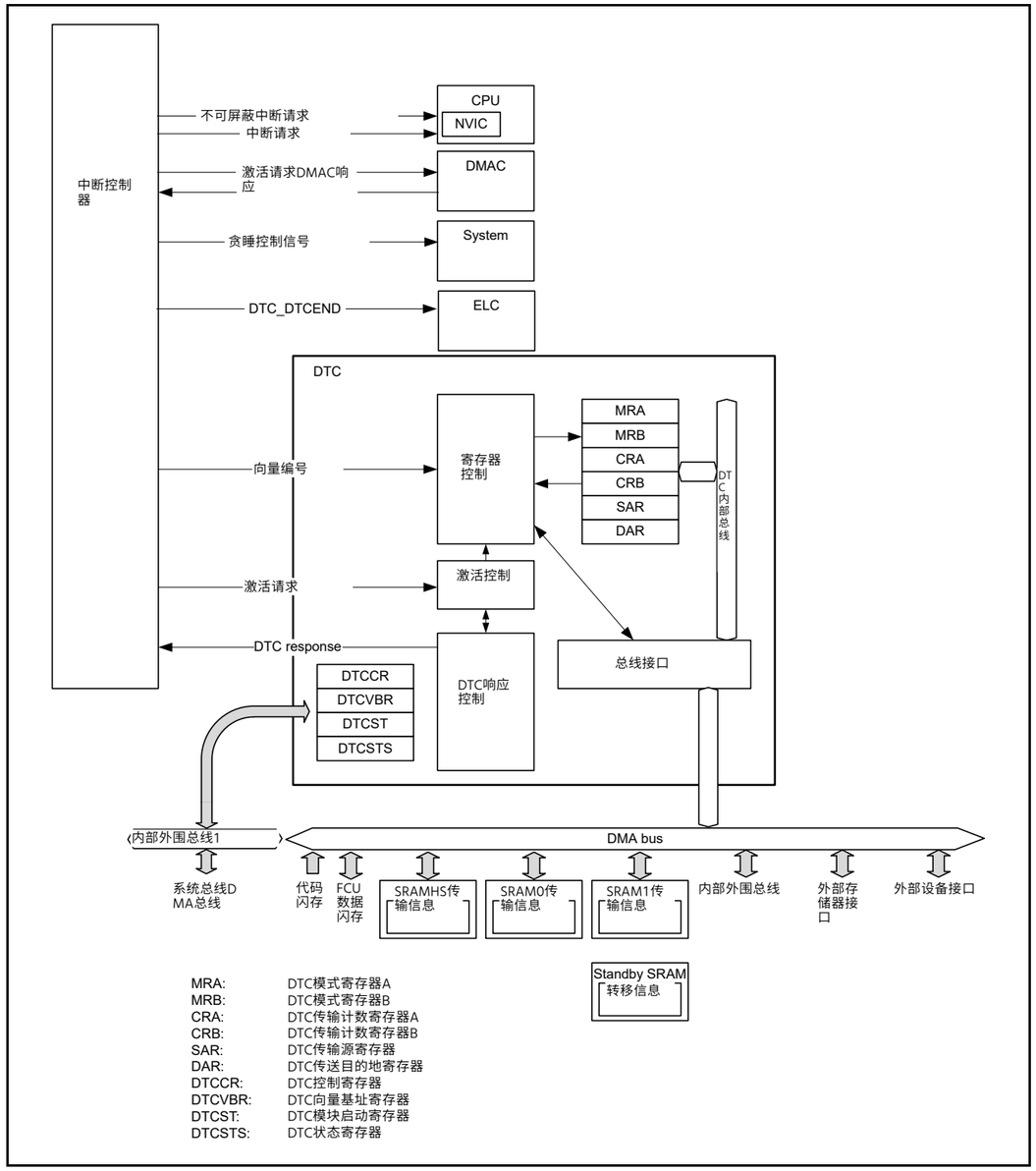


Figure 18.1 故障诊断代码框图

有关DTC和NVIC（在CPU中）之间的连接，请参见第14节“中断控制器单元(ICU)”中的14.1概述。

18.2 注册说明

MRA、MRB、SAR、DAR、CRA、CRB都是DTC内部寄存器，不能直接从CPU访问。在这些DTC内部寄存器中设置的值作为传输信息放置在SRAM区域中。当产生激活请求时，DTC从SRAM区域读取传输信息并将其设置在其内部寄存器中。数据传输结束后，内部寄存器内容作为传输信息回写到SRAM区域。

18.2.1 DTC Mode Register A (MRA)

Address(es): (Inaccessible directly from the CPU. See section 18.3.1.)

	b7	b6	b5	b4	b3	b2	b1	b0
	MD[1:0]		SZ[1:0]		SM[1:0]		—	—
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b1, b0	—	Reserved	These bits are read as undefined. The write value should be 0.	—
b3, b2	SM[1:0]	Transfer Source Address Addressing Mode	b3 b2 0 0: Address in the SAR register is fixed (write-back to SAR is skipped) 0 1: Address in the SAR register is fixed (write-back to SAR is skipped) 1 0: SAR value is incremented after data transfer: +1 when SZ[1:0] = 00b +2 when SZ[1:0] = 01b +4 when SZ[1:0] = 10b. 1 1: SAR value is decremented after data transfer: -1 when SZ[1:0] = 00b -2 when SZ[1:0] = 01b -4 when SZ[1:0] = 10b.	—
b5, b4	SZ[1:0]	DTC Data Transfer Size	b5 b4 0 0: Byte (8-bit) transfer 0 1: Halfword (16-bit) transfer 1 0: Word (32-bit) transfer 1 1: Setting prohibited.	—
b7, b6	MD[1:0]	DTC Transfer Mode Select	b7 b6 0 0: Normal transfer mode 0 1: Repeat transfer mode 1 0: Block transfer mode 1 1: Setting prohibited.	—

The MRA register cannot be accessed directly from the CPU, however the CPU can access the SRAM area (transfer information (n) start address + 03h) and the DTC automatically transfers the MRA transfer information to and from the MRA register. See section 18.3.1, Allocating Transfer Information and the DTC Vector Table.

18.2.2 DTC Mode Register B (MRB)

Address(es): (Inaccessible directly from the CPU. See section 18.3.1.)

	b7	b6	b5	b4	b3	b2	b1	b0
	CHNE	CHNS	DISEL	DTS	DM[1:0]		—	—
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b1, b0	—	Reserved	These bits are read as undefined. The write value should be 0.	—

18.2.1 DTC模式寄存器A(MRA)

地址：（无法直接从CPU访问。请参阅第18.3.1节。）

	b7	b6	b5	b4	b3	b2	b1	b0
	MD[1:0]		SZ[1:0]		SM[1:0]		—	—
重置后的值：	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b1, b0	—	Reserved	这些位被读取为未定义。写入值应为0。	—
b3, b2	SM[1:0]	传输源地址寻址 Mode	b3b200：SAR寄存器中的地址固定（跳过对SAR的回写）01：SAR寄存器中的地址固定（跳过对SAR的回写）10：数据传输后SAR值递增:+1当SZ[1:0]=00b时+2当SZ[1:0]=01b时+4当SZ[1:0]=10b时。11：数据传输后SAR值递减：-1当SZ[1:0]=00b-2当SZ[1:0]=01b-4当SZ[1:0]=10b。	—
b5, b4	SZ[1:0]	DTC数据传输大小	b5b400：字节（8位）传送01：半字（16位）传送10：字（32位）传送11：禁止设置。	—
b7, b6	MD[1:0]	DTC传输模式选择	b7b600：正常传输模式01：重复传输模式10：块传输模式11：禁止设置。	—

MRA寄存器不能直接从CPU访问，但是CPU可以访问SRAM区域（传输信息(n)起始地址+03h），并且DTC会自动将MRA传输信息传输到MRA寄存器或从MRA寄存器传输信息。请参阅第18.3.1节，分配传输信息和DTC向量表。

18.2.2 DTC模式寄存器B(MRB)

地址：（无法直接从CPU访问。请参阅第18.3.1节。）

	b7	b6	b5	b4	b3	b2	b1	b0
	CHNE	CHNS	DISEL	DTS	DM[1:0]		—	—
重置后的值：	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b1, b0	—	Reserved	这些位被读取为未定义。写入值应为0。	—

Bit	Symbol	Bit name	Description	R/W
b3, b2	DM[1:0]	Transfer Destination Address Addressing Mode	b3 b2 0 0: Address in the DAR register is fixed (write-back to DAR is skipped) 0 1: Address in DAR register is fixed (write-back to DAR is skipped) 1 0: DAR value is incremented after data transfer: +1 when MRA.SZ[1:0] = 00b +2 when MRA.SZ[1:0] = 01b +4 when MRA.SZ[1:0] = 10b. 1 1: DAR value is decremented after data transfer: -1 when MRA.SZ[1:0] = 00b -2 when MRA.SZ[1:0] = 01b -4 when MRA.SZ[1:0] = 10b.	—
b4	DTS	DTC Transfer Mode Select	0: Select transfer destination as repeat or block area 1: Select transfer source as repeat or block area.	—
b5	DISEL	DTC Interrupt Select	0: Generate an interrupt request to CPU when specified data transfer is complete 1: Generate an interrupt request to CPU each time DTC data transfer is performed.	—
b6	CHNS	DTC Chain Transfer Select	0: Select continuous chain transfer 1: Select chain transfer occurring only when the transfer counter is changed from 1 to 0 or 1 to CRAH.	—
b7	CHNE	DTC Chain Transfer Enable	0: Chain transfer disabled 1: Chain transfer enabled.	—

The MRB register cannot be accessed directly from the CPU, however the CPU can access the SRAM area (transfer information (n) start address + 02h) and the DTC automatically transfers the MRB transfer information to and from the MRB register. See section 18.3.1, Allocating Transfer Information and the DTC Vector Table.

DTS bit (DTC Transfer Mode Select)

The DTS bit selects either the transfer source or transfer destination as the repeat area or block area in repeat or block transfer mode.

CHNS bit (DTC Chain Transfer Select)

The CHNS bit selects the chain transfer condition. When CHNE is 0, the CHNS setting is ignored. For details on the conditions for chain transfer, see Table 18.3, Chain transfer conditions.

When the next transfer is a chain transfer, completion of the specified number of transfers is not determined, the activation source flag is not cleared, and an interrupt request to the CPU is not generated.

CHNE bit (DTC Chain Transfer Enable)

The CHNE bit enables chain transfer. The chain transfer condition is selected in the CHNS bit. For details on chain transfer, see section 18.4.6, Chain Transfer.

18.2.3 DTC Transfer Source Register (SAR)

Address(es): (Inaccessible directly from the CPU. See section 18.3.1.)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

The SAR register sets the transfer source start address and cannot be accessed directly from the CPU. However, the CPU

Bit	Symbol	位名称	Description	R/W
b3, b2	DM[1:0]	转移目的地地址寻址方式	b3b200：DAR寄存器中的地址固定（跳过对DAR的回写）01：DAR寄存器中的地址固定（跳过对DAR的回写）10：数据传输后DAR值递增：+1当MRA.SZ[1:0]=00b时+2当MRA.SZ[1:0]=01b时+4当MRA.SZ[1:0]=10b时。11：数据传输后DAR值递减：−1当MRA.SZ[1:0]=00b−2当MRA.SZ[1:0]=01b−4当MRA.SZ[1:0]=10b.	—
b4	DTS	DTC传输模式选择	0：选择传输目标为重复或块区域1：选择传输源为重复或块区域。	—
b5	DISEL	DTC中断选择	0：指定数据传输完成时向CPU产生中断请求1：每次执行DTC数据传输时，向CPU产生中断请求。	—
b6	CHNS	DTC链转移选择	0：选择连续链转移1：选择仅在转移计数器从1变为0或从1变为CRAH时发生的链转移。	—
b7	CHNE	DTC链转移启用	0：禁止链转移1：允许链转移。	—

MRB寄存器不能直接从CPU访问，但是CPU可以访问SRAM区域（传输信息(n)起始地址+02h），并且DTC自动将MRB传输信息传输到MRB寄存器或从MRB寄存器传输信息。请参阅第18.3.1节，分配传输信息和DTC向量表。

DTS位（DTC传输模式选择）

在重复或块传输模式下，DTS位选择传输源或传输目标作为重复区域或块区域。

CHNS位（DTC链传输选择）

CHNS位选择链传输条件。当CHNE为0时，忽略CHNS设置。有关链转移条件的详细信息，请参见表18.3，链转移条件。

当下一次传输是链式传输时，指定传输次数的完成未确定，激活源标志未清零，也不向CPU产生中断请求。

CHNE位（DTC链传输使能）

CHNE位启用链式传输。在CHNS位中选择链传输条件。有关链转移的详细信息，请参阅第18.4.6节，链转移。

18.2.3 DTC传输源寄存器(SAR)

地址：（无法直接从CPU访问。请参阅第18.3.1节。）

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

SAR寄存器设置传输源起始地址，不能直接从CPU访问。但是，CPU

can access the SRAM area (transfer information (n) start address + 04h) and the DTC automatically transfers the SAR transfer information to and from the SAR register. See section 18.3.1, Allocating Transfer Information and the DTC Vector Table.

Note: Misalignment is prohibited for DTC transfers. Bit [0] must be 0 when MRA.SZ[1:0] = 01b.
Bits [1] and [0] must be 0 when MRA.SZ[1:0] = 10b.

18.2.4 DTC Transfer Destination Register (DAR)

Address(es): (Inaccessible directly from the CPU. See section 18.3.1.)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

The DAR register sets the transfer destination start address and cannot be accessed directly from the CPU. However, the CPU can access the SRAM area (transfer information (n) start address + 08h) and the DTC automatically transfers the DAR transfer information to and from the DAR register. See section 18.3.1, Allocating Transfer Information and the DTC Vector Table.

Note: Misalignment is prohibited for DTC transfers. Bit [0] must be 0 when MRA.SZ[1:0] = 01b.
Bits [1] and [0] must be 0 when MRA.SZ[1:0] = 10b.

18.2.5 DTC Transfer Count Register A (CRA)

Address(es): (Inaccessible directly from the CPU. See section 18.3.1.)

- Normal transfer mode

	CRA															
	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

- Repeat transfer mode/block transfer mode

	CRAH								CRAL							
	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Symbol	Register name	Description	R/W
CRAL	Transfer Counter A Lower Register	Specify the transfer count	—
CRAH	Transfer Counter A Upper Register		—

Note: The function depends on the transfer mode.
Note: Set CRAH and CRAL to the same value in repeat transfer mode and block transfer mode.

The CRA register cannot be accessed directly from the CPU, however the CPU can access the SRAM area (transfer

可以访问SRAM区域（传输信息(n)起始地址+04h），并且DTC自动将SAR传输信息传输到SAR寄存器和从SAR寄存器传输信息。请参阅第18.3.1节，分配传输信息和DTC向量表。

Note: DTC传输禁止错位。当MRA.SZ[1:0]=01b时，位[0]必须为0。
当MRA.SZ[1:0]=10b时，位[1]和[0]必须为0。

18.2.4 DTC传输目的地寄存器(DAR)

地址：（无法直接从CPU访问。请参阅第18.3.1节。）

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

DAR寄存器设置传输目标起始地址，不能直接从CPU访问。但是，那CPU可以访问SRAM区域（传输信息(n)起始地址+08h）并且DTC会自动传输DAR将信息传入和传出DAR寄存器。请参阅第18.3.1节，分配传输信息和DTC向量表。

Note: DTC传输禁止错位。当MRA.SZ[1:0]=01b时，位[0]必须为0。
当MRA.SZ[1:0]=10b时，位[1]和[0]必须为0。

18.2.5 DTC传输计数寄存器A(CRA)

地址：（无法直接从CPU访问。请参阅第18.3.1节。）

正常传输模式

	CRA															
	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

重复传输模式块传输模式

	CRAH								CRAL							
	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Symbol	注册名称	Description	R/W
CRAL	传送计数器A低位寄存器	指定传输计数	—
CRAH	传送计数器A高位寄存器		—

Note: 该功能取决于传输模式。
Note: 在重复传输模式和块传输模式下，将CRAH和CRAL设置为相同的值。

CRA寄存器不能直接从CPU访问，但是CPU可以访问SRAM区域（传输

information (n) start address + 0Eh) and the DTC automatically transfers the CRA transfer information to and from the CRA register. See section 18.3.1, Allocating Transfer Information and the DTC Vector Table.

(1) Normal transfer mode (MRA.MD[1:0] = 00b)

In normal transfer mode, CRA functions as a 16-bit transfer counter. The transfer count is 1, 65,535, and 65,536 when the set value is 0001h, FFFFh, and 0000h, respectively. The CRA value is decremented (-1) on each data transfer.

(2) Repeat transfer mode (MRA.MD[1:0] = 01b)

In repeat transfer mode, the CRAH register holds the transfer count and the CRAL register functions as an 8-bit transfer counter. The transfer count is 1, 255, and 256 when the set value is 01h, FFh, and 00h, respectively. The CRAL value is decremented (-1) on each data transfer. When it reaches 00h, the CRAH value is transferred to CRAL.

(3) Block transfer mode (MRA.MD[1:0] = 10b)

In block transfer mode, the CRAH register holds the block size and the CRAL register functions as an 8-bit block size counter. The transfer count is 1, 255, and 256 when the set value is 01h, FFh, and 00h, respectively. The CRAL value is decremented (-1) at each data transfer. When it reaches 00h, the CRAH value is transferred to CRAL.

18.2.6 DTC Transfer Count Register B (CRB)

Address(es): (Inaccessible directly from the CPU. See section 18.3.1.)

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

The CRB register sets the block transfer count for block transfer mode. The transfer count is 1, 65,535, and 65,536 when the set value is 0001h, FFFFh, and 0000h, respectively. The CRB value is decremented (-1) when the final data of a single block size is transferred. When normal transfer mode or repeat transfer mode is selected, this register is not used and the set value is ignored.

CRB cannot be accessed directly from the CPU, however the CPU can access the SRAM area (transfer information (n) start address + 0ch) and the DTC automatically transfers the CRB transfer information to and from the CRB register. See section 18.3.1, Allocating Transfer Information and the DTC Vector Table.

18.2.7 DTC Control Register (DTCCR)

Address(es): DTC.DTCCR 4000 5400h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	RRS	—	—	—	—
Value after reset:	0	0	0	0	1	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b3	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b4	RRS	DTC Transfer Information Read Skip Enable	0: Transfer information read is not skipped 1: Transfer information read is skipped when vector numbers match.	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

RRS bit (DTC Transfer Information Read Skip Enable)

The RRS bit enables skipping of transfer information reads when vector numbers match.

The DTC vector number is compared with the vector number in the previous activation process. When these vector

信息(n)起始地址+0Eh)和DTC自动将CRA传输信息传输到CRA寄存器和从CRA寄存器传输信息。请参阅第18.3.1节，分配传输信息和DTC向量表。

(1) 正常传输模式（MRA.MD[1:0]=00b）

在正常传输模式下，CRA用作16位传输计数器。当设置值为0001h、FFFFh和0000h时，传输计数分别为1、65 535和65 536。CRA值在每次数据传输时递减(−1)。

(2) 重复传输模式(MRA.MD[1:0]=01b)

在重复传输模式下，CRAH寄存器保存传输计数，CRAL寄存器用作8位传输计数器。当设置值为01h、FFh和00h时，传输计数分别为1、255和256。CRAL值在每次数据传输时递减(−1)。当它达到00h时，CRAH值被传送到CRAL。

(3) 块传输模式（MRA.MD[1:0]=10b）

在块传输模式下，CRAH寄存器保存块大小，CRAL寄存器用作8位块大小计数器。当设置值为01h、FFh和00h时，传输计数分别为1、255和256。CRAL值在每次数据传输时递减(−1)。当它达到00h时，CRAH值被传送到CRAL。

18.2.6 DTC传输计数寄存器B(CRB)

地址：（无法直接从CPU访问。请参阅第18.3.1节。）

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

CRB寄存器设置块传输模式的块传输计数。当设置值为0001h、FFFFh和0000h时，传输计数分别为1、65 535和65 536。当传输单个块大小的最终数据时，CRB值递减(−1)。Whennormaltransfermodeorrepeattransfermodeisselected thisregisterisnotusedandthesetvalueisignored.

CRB不能直接从CPU访问，但是CPU可以访问SRAM区域（传输信息(n)起始地址+0ch），并且DTC会自动将CRB传输信息传输到CRB寄存器或从CRB寄存器传输信息。请参阅第18.3.1节，分配传输信息和DTC向量表。

18.2.7 DTC控制寄存器(DTCCR)

Address(es): DTC.DTCCR 4000 5400h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	RRS	—	—	—	—
重置后的值：	0	0	0	0	1	0	0	0

Bit	Symbol	位名称	Description	R/W
b2 to b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b3	—	Reserved	该位读取为1。写入值应为1。	R/W
b4	RRS	DTC传输信息 读取跳过启用	0：不跳过传输信息读取1：当向量编号匹配时，跳过传输信息读取。	R/W
b7 to b5	—	Reserved	这些位被读取为0。写入值应为0。	R/W

RRS位（DTC传输信息读取跳过使能）

当向量编号匹配时，RRS位允许跳过传输信息读取。

将DTC向量编号与之前激活过程中的向量编号进行比较。当这些向量

numbers match and the RRS bit is set to 1, DTC data transfer is performed without reading the transfer information. However, when the previous transfer is a chain transfer, the transfer information is read regardless of the value in the RRS bit.

When the transfer counter (CRA register) becomes 0 during the previous normal transfer and when the transfer counter (CRB register) becomes 0 during the previous block transfer, the transfer information is read regardless of the RRS bit value.

18.2.8 DTC Vector Base Register (DTCVBR)

Address(es): DTC.DTCVBR 4000 5404h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Bit name	Description	R/W
b31 to b0	DTC Vector Base Address	Specify the DTC vector base address. The lower 10 bits should be 0.	R/W

The DTCVBR register sets the base address for calculating the DTC vector table address, which can be set in the range of 0000 0000h to FFFF FFFFh (4 GB) in 1-KB units.

18.2.9 DTC Module Start Register (DTCST)

Address(es): DTC.DTCST 4000 540Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	DTCST
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	DTCST	DTC Module Start	0: DTC module stopped 1: DTC module started.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

DTCST bit (DTC Module Start)

Set the DTCST bit to 1 to enable the DTC to accept transfer requests. When DTCST is set to 0, transfer requests are no longer accepted. If DTCST is set to 0 during a data transfer, the accepted transfer request is active until processing is complete.

DTCST must be set to 0 before transitioning to any of the following state or mode:

- Module-stop state
- Software Standby mode without Snooze mode transition
- Deep Software Standby mode.

For details on these transitions, see section 18.10, Module-Stop Function, and section 11, Low Power Modes.

如果数字匹配并且RRS位设置为1，则执行DTC数据传输而不读取传输信息。但是，当上一次传输是链式传输时，无论传输中的值如何，都会读取传输信息。

RRS bit.

如果在前一次正常传输期间传输计数器（CRA寄存器）变为0，并且在前一次块传输期间传输计数器（CRB寄存器）变为0，则无论RRS位的值如何，都将读取传输信息。

18.2.8 DTC向量基址寄存器(DTCVBR)

Address(es): DTC.DTCVBR 4000 5404h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	位名称	Description	R/W
b31 to b0	DTC向量基地址	指定DTC向量基地址。低10位应为0。	R/W

DTCVBR寄存器设置计算DTC向量表地址的基地址，可以设置在00000000h到FFFFFFFFh(4GB)的范围内，以1KB为单位。

18.2.9 DTC模块启动寄存器(DTCST)

Address(es): DTC.DTCST 4000 540Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	DTCST
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	DTCST	DTC模块启动	0：DTC模块停止1：DTC模块启动。	R/W
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

DTCST位（DTC模块启动）

将DTCST位设置为1以使DTC接受传输请求。当DTCST设置为0时，不再接受传输请求。如果在数据传输期间将DTCST设置为0，则接受的传输请求将处于活动状态，直到处理完成。

在转换到以下任何状态或模式之前，必须将DTCST设置为0：

- Module-stop state
- 没有贪睡模式转换的软件待机模式
- 深度软件待机模式。

有关这些转换的详细信息，请参阅第18.10节，模块停止功能和第11节，低功耗模式。

18.2.10 DTC Status Register (DTCSTS)

Address(es): DTC.DTCSTS 4000 540Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ACT	—	—	—	—	—	—	—	VECN[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	VECN[7:0]	DTC-Activating Vector Number Monitoring	These bits indicate the vector number for the activation source when a DTC transfer is in progress. The value is only valid if a DTC transfer is in progress (ACT flag is 1).	R
b14 to b8	—	Reserved	These bits are read as 0. Writing to these bits has no effect.	R
b15	ACT	DTC Active Flag	0: DTC transfer operation is not in progress 1: DTC transfer operation is in progress.	R

VECN[7:0] bits (DTC-Activating Vector Number Monitoring)

While transfer by the DTC is in progress, the VECN[7:0] bits indicate the vector number associated with the activation source for the transfer. The value read from the VECN[7:0] bits is valid if the value of the ACT flag is 1, indicating a DTC transfer is in progress, and invalid if the value of the ACT flag is 0, indicating no DTC transfer is in progress.

ACT flag (DTC Active Flag)

The ACT flag indicates the state of the DTC transfer operation.

[Setting condition]

- When the DTC is activated by a transfer request.

[Clearing condition]

- When transfer by the DTC, in response to a transfer request, is complete.

18.3 Activation Sources

The DTC is activated by an interrupt request. Setting the ICU.IELSRn.DTCE bit to 1 enables activation of the DTC by the associated interrupt. The selector output *n* number set in ICU.IELSRn is defined as the interrupt vector number, where n = 0 to 95. For an enabled interrupt, the specific DTC interrupt source associated with each interrupt vector number n is selected in ICU.IELSRn.IELS[8:0], as listed in Table 14.4, Event table, in section 14, Interrupt Controller Unit (ICU).

For activation by software, see section 19.2.2, Event Link Software Event Generation Register n (ELSEGRn) (n = 0, 1).

The interrupt vector number is equivalent to the DTC vector table number. After the DTC accepts an activation request, it does not accept another activation request until transfer for that single request is complete, regardless of the priority of the requests. When multiple activation requests are generated during a DMAC or DTC transfer, a highest priority request is accepted on completion of the transfer. When multiple activation requests are generated while the DTC module start bit (DTCST.DTCST) is 0, the DTC accepts the highest priority request when DTCST.DTCST is subsequently set to 1. The smaller interrupt vector number has higher priority.

The DTC performs the following operations at the start of a single data transfer or for a chain transfer, after the last of the consecutive transfers:

- On completion of a specified round of data transfer, the ICU.IELSRn.DTCE bit is set to 0, and an interrupt request is sent to the CPU
- If the MRB.DISEL bit is 1, an interrupt request is sent to the CPU on completion of a data transfer
- For other transfers, the ICU.IELSRn.IR bit of the activation source is set to 0 at the start of the data transfer.

18.2.10 DTC状态寄存器(DTCSTS)

Address(es): DTC.DTCSTS 4000 540Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ACT	—	—	—	—	—	—	—	VECN[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b7 to b0	VECN[7:0]	DTC-Activating Vector 号码监控	当DTC传输正在进行时，这些位指示激活源的向量编号。该值仅在DTC传输正在进行（ACT标志为1）时有效。	R
b14 to b8	—	Reserved	这些位被读取为0。写入这些位无效。	R
b15	ACT	DTC活动标志	0：未进行DTC传输操作1：正在进行DTC传输操作。	R

VECN[7:0]位（DTC–激活向量编号监控）

当DTC进行传输时，VECN[7:0]位指示与传输激活源相关的向量编号。如果ACT标志的值为1，则从VECN[7:0]位读取的值有效，表示正在进行DTC传输，如果ACT标志的值为0，则表示没有DTC传输。进步。

ACT标志（DTC活动标志）

ACT标志指示DTC传输操作的状态。

[Setting condition]

- 当DTC被传输请求激活时。

[Clearing condition]

- 当DTC响应传输请求传输完成时。

18.3 激活源

DTC由中断请求激活。将ICU.IELSRn.DTCE位设置为1可以通过相关中断激活DTC。ICU.IELSRn中设置的选择器输出n号定义为中断向量号，其中n=0到95。对于启用的中断，在ICU.IELSRn.IELS中选择与每个中断向量号n关联的特定DTC中断源[8:0]，如表14.4，事件表，第14节，中断控制器单元(ICU)中所列。

对于软件激活，请参见第19.2.2节，事件链接软件事件生成寄存器n(ELSEGRn)(n=0 1)。

中断向量编号相当于DTC向量表编号。在DTC接受激活请求后，它不会接受另一个激活请求，直到该单个请求的传输完成，无论请求的优先级如何。如果在DMAC或DTC传输期间生成多个激活请求，则在传输完成时接受最高优先级的请求。当DTC模块起始位(DTCST.DTCST)为0时产生多个激活请求时，当DTCST.DTCST随后设置为1时，DTC接受最高优先级请求。较小的中断向量编号具有较高的优先级。

DTC在单次数据传输开始时执行以下操作，或者对于链式传输，在最后一次连续传输之后执行以下操作：

- 完成指定的一轮数据传输后，ICU.IELSRn.DTCE位设置为0，并向CPU发送中断请求
- 如果MRB.DISEL位为1，则在数据传输完成时向CPU发送中断请求
- 对于其他传输，激活源的ICU.IELSRn.IR位在数据传输开始时设置为0。

18.3.1 Allocating Transfer Information and the DTC Vector Table

The DTC reads the start address of the transfer information associated with each activation source from the vector table and reads the transfer information starting at that address.

The vector table must be located so that the lower 10 bits of the base address (start address) are 0. Use the DTC Vector Base Register (DTCVBR) to set the base address of the DTC vector table. Transfer information is allocated in the SRAM area. In the SRAM area, the start address of the transfer information (n) with vector number n must be 4n added to the base address in the vector table.

Figure 18.2 shows the relationship between the DTC vector table and transfer information. Figure 18.3 shows the allocation of transfer information in the SRAM area.

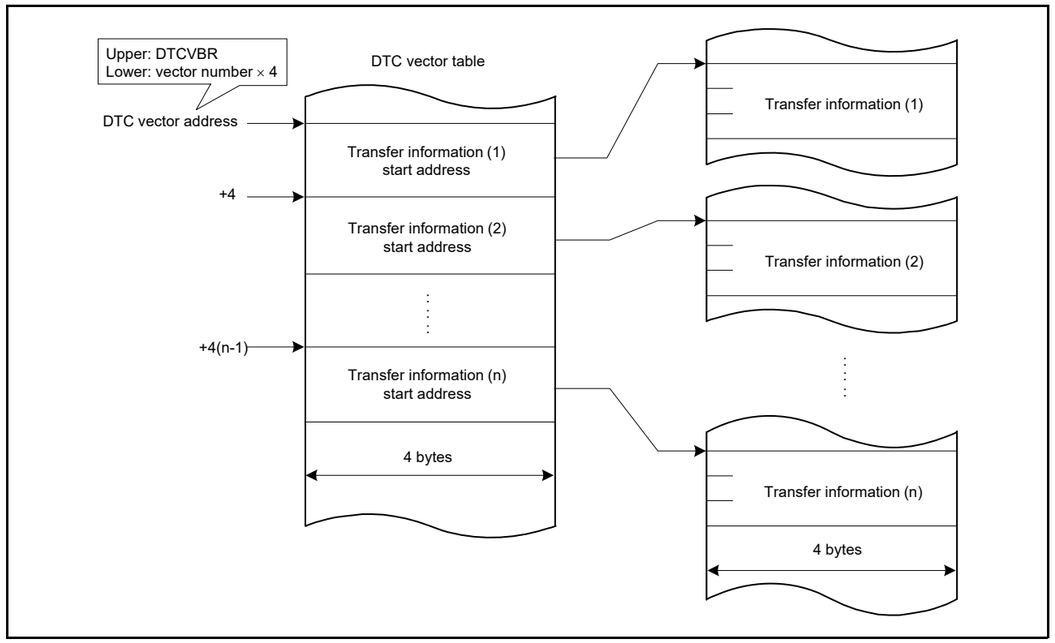


Figure 18.2 DTC vector table and transfer information

18.3.1 分配传输信息和DTC向量表

DTC从向量表中读取与每个激活源相关联的传输信息的起始地址，并读取从该地址开始的传输信息。

向量表的定位必须使基地址（起始地址）的低10位为0。使用DTC向量基址寄存器(DTCVBR)设置DTC向量表的基地址。传输信息分配在SRAM区域中。在SRAM区域中，向量编号为n的传输信息(n)的起始地址必须与向量表中的基地址相加4n。

图18.2显示了DTC向量表和传输信息之间的关系。图18.3显示了SRAM区域中传输信息的分配。

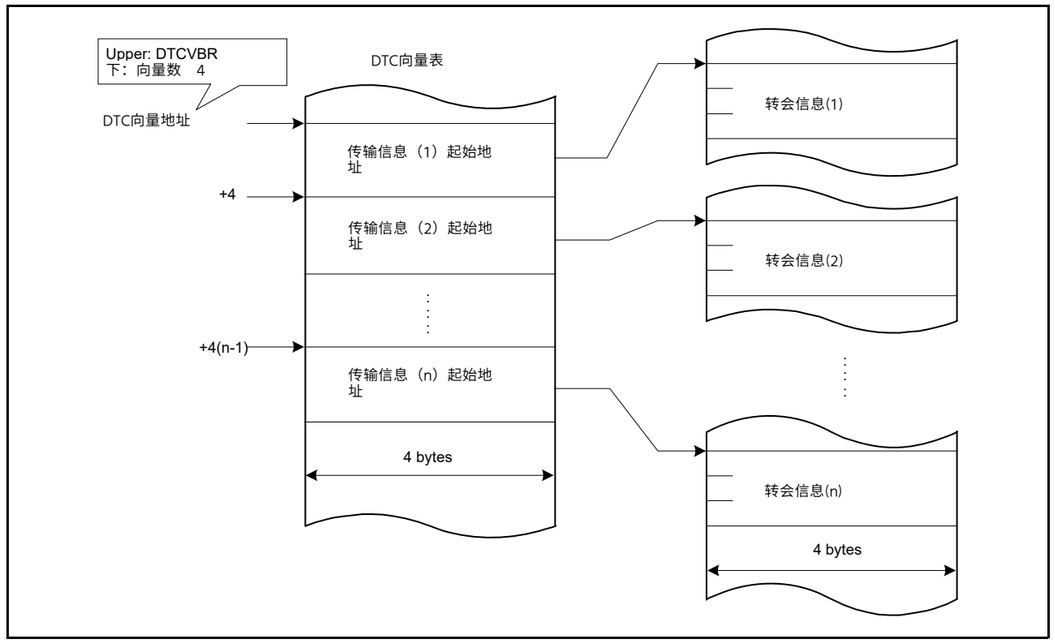


Figure 18.2 DTC向量表和传输信息

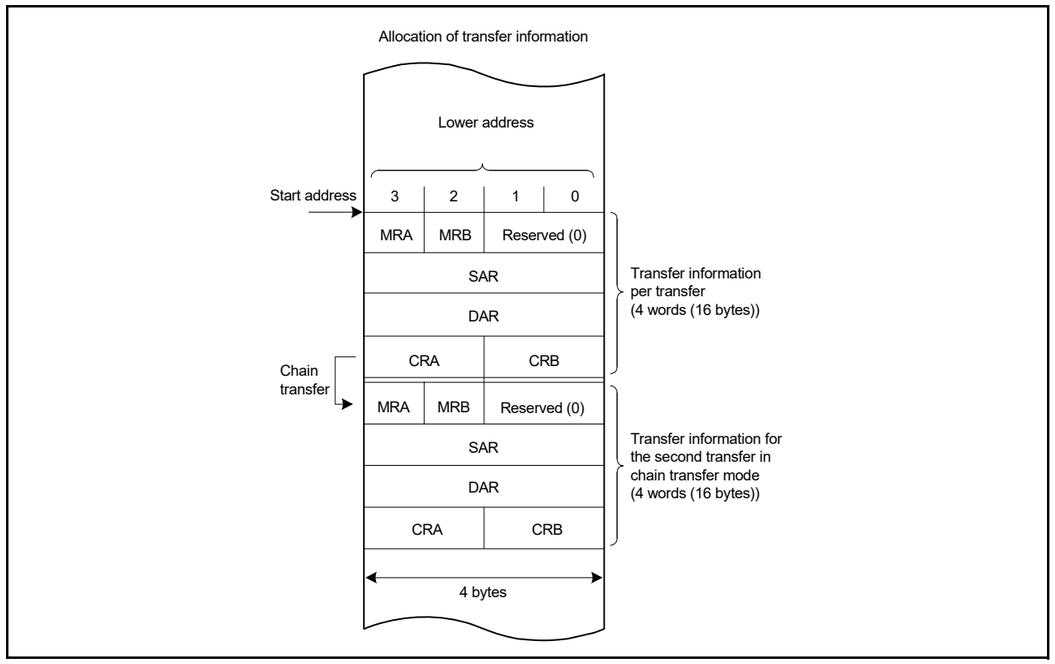


Figure 18.3 Allocation of transfer information in the SRAM area

18.4 Operation

The DTC transfers data according to the transfer information. Storage of the transfer information in the SRAM area is required before a DTC operation. When the DTC is activated, it reads the DTC vector associated with the vector number. The DTC then reads the transfer information from the transfer information store address referenced by the DTC vector and transfers the data. After the data transfer, the DTC writes back the transfer information. Storing the transfer information in the SRAM area allows data transfer of any number of channels.

The transfer modes include:

- Normal transfer mode
- Repeat transfer mode
- Block transfer mode.

The DTC specifies a transfer source address in the SAR register and a transfer destination address in the DAR register. The values in these registers are incremented, decremented, or address-fixed independently after the data transfer.

Table 18.2 describes the DTC transfer modes.

Table 18.2 DTC transfer modes

Transfer mode	Data size transferred on single transfer request	Increment or decrement of memory address	Settable transfer count
Normal transfer mode	1 byte (8 bits), 1 halfword (16 bits), or 1 word (32 bits)	Incremented or decremented by 1, 2, or 4 or address fixed	1 to 65,536
Repeat transfer mode*1	1 byte (8 bits), 1 halfword (16 bits), or 1 word (32 bits)	Incremented or decremented by 1, 2, or 4 or address fixed	1 to 256*3
Block transfer mode*2	Block size specified in CRAH (1 to 256 bytes, 1 to 256 halfwords (2 to 512 bytes), or 1 to 256 words (4 to 1024 bytes))	Incremented or decremented by 1, 2, or 4 or address fixed	1 to 65,536

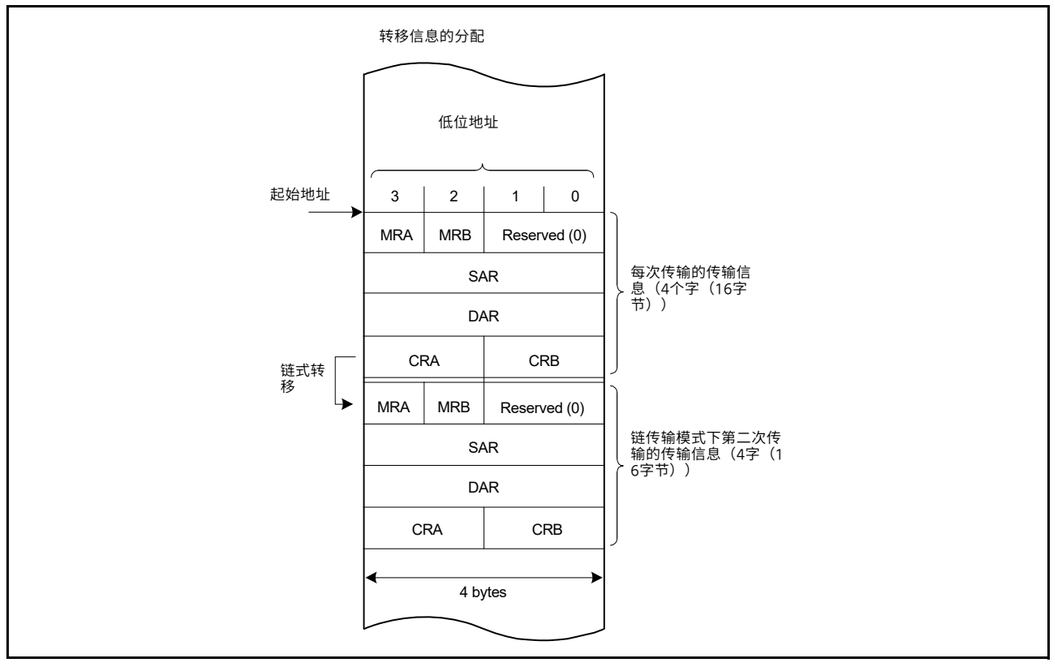


Figure 18.3 SRAM区域中传输信息的分配

18.4 Operation

DTC根据传输信息传输数据。在进行DTC操作之前，需要在SRAM区域中存储传输信息。当DTC被激活时，它会读取与向量编号相关联的DTC向量。然后DTC从DTC向量引用的传输信息存储地址中读取传输信息并传输数据。数据传输后，DTC写回传输信息。将传输信息存储在SRAM区域中可以实现任意数量的通道的数据传输。

传输模式包括：

- 正常传输模式
- 重复传输模式
- 块传输模式。

DTC指定SAR寄存器中的传输源地址和DAR寄存器中的传输目标地址。
这些寄存器中的值在数据传输后独立地递增、递减或固定地址。

表18.2描述了DTC传输模式。

Table 18.2 DTC传输模式

传输模式	在单个传输请求上传输的数据大小	内存地址的递增或递减	可设置的传输次数
正常传输模式	1个字节（8位）、1个半字（16位）或1个字（32位）	递增或递减1、2或4或固定地址	1 to 65,536
重复传输模式*1	1个字节（8位）、1个半字（16位）或1个字（32位）	递增或递减1、2或4或固定地址	1 to 256*3
块传输模式*2	CRAH中指定的块大小（1到256字节、1到256个半字（2到512字节）或1到256字（4到1024字节））	递增或递减1、2或4或固定地址	1 to 65,536

Note 1. Set the transfer source or destination as the repeat area.
Note 2. Set the transfer source or destination as the block area.
Note 3. After a data transfer of the specified count, the initial state is restored and operation restarts.

Setting the MRB.CHNE bit to 1 allows multiple transfers or a chain transfer on a single activation source. It also enables a chain transfer when the specified data transfer is complete.

Figure 18.4 shows the operation flow of the DTC. Table 18.3 lists the chain transfer conditions. The combination of control information for the second and subsequent transfers are omitted in this table.

Note 1. 将传输源或目标设置为重复区域。
Note 2. 将传输源或目标设置为块区域。
Note 3. 在指定计数的数据传输后，恢复初始状态并重新开始操作。

将MRB.CHNE位设置为1允许在单个激活源上进行多次传输或链式传输。当指定的数据传输完成时，它还启用链式传输。

图18.4显示了DTC的操作流程。表18.3列出了链转移条件。该表中省略了用于第二次和后续传输的控制信息的组合。

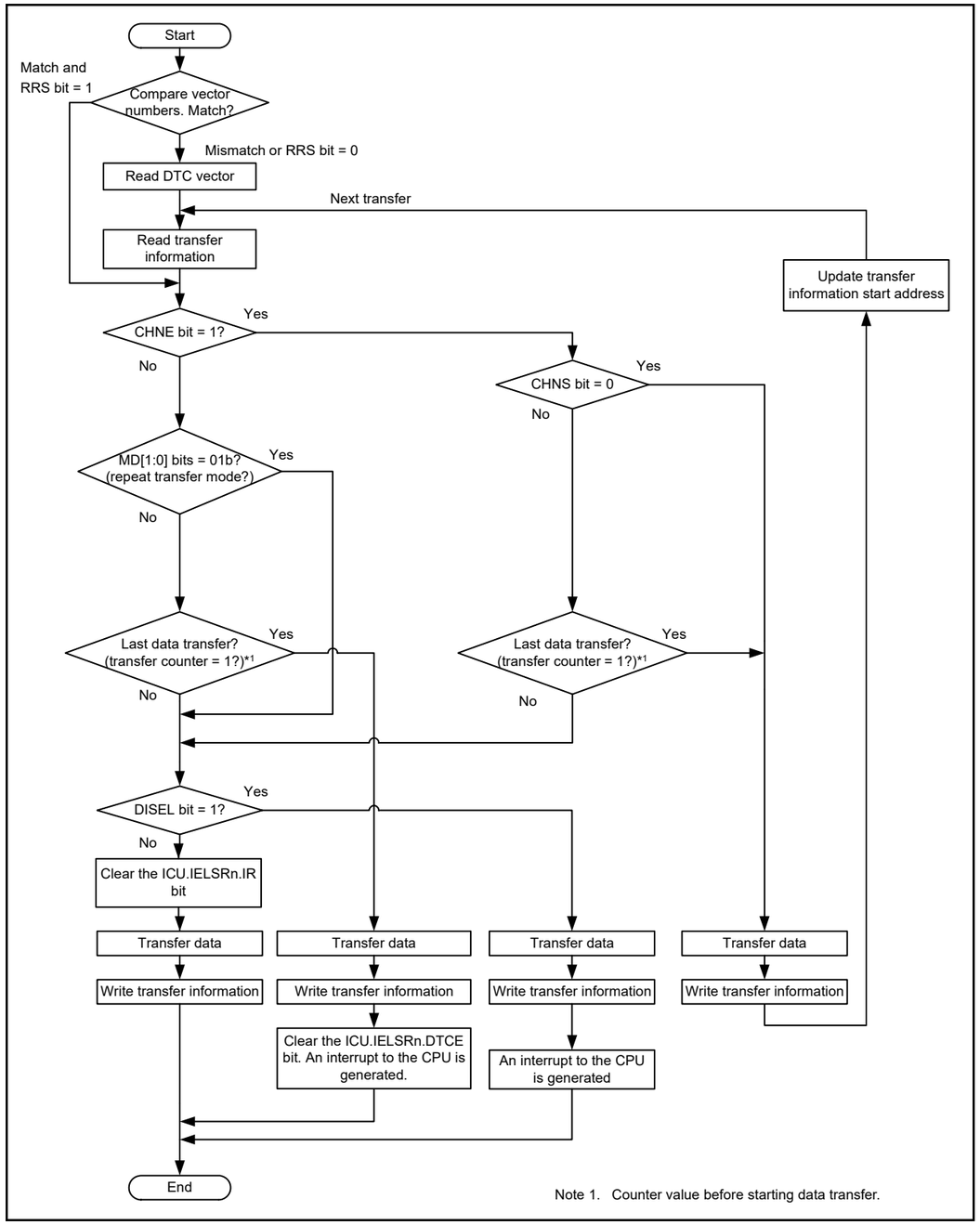


Figure 18.4 DTC operation flow

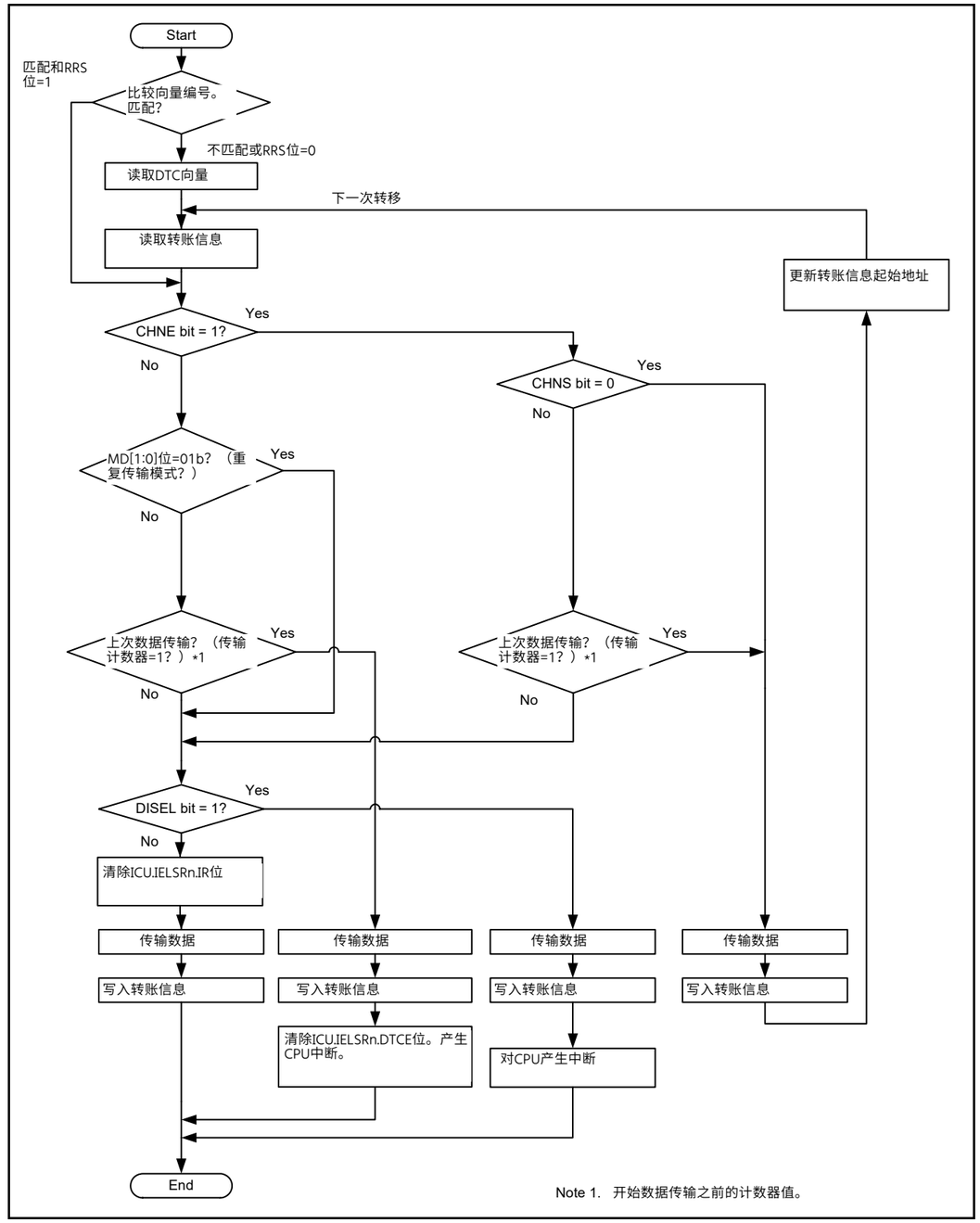


Figure 18.4 DTC操作流程

Table 18.3 Chain transfer conditions

First transfer				Second transfer*3				DTC transfer
CHNE bit	CHNS bit	DISEL bit	Transfer counter*1,*2	CHNE bit	CHNS bit	DISEL bit	Transfer counter*1,*2	
0	—	0	Other than (1 → 0)	—	—	—	—	Ends after the first transfer
0	—	0	(1 → 0)	—	—	—	—	Ends after the first transfer with an interrupt request to the CPU
0	—	1	—	—	—	—	—	
1	0	—	—	0	—	0	Other than (1 → 0)	Ends after the second transfer
				0	—	0	(1 → 0)	Ends after the second transfer with an interrupt request to the CPU
				0	—	1	—	
1	1	0	Other than (1 → *)	—	—	—	—	Ends after the first transfer
1	1	—	(1 → *)	0	—	0	Other than (1 → 0)	Ends after the second transfer
				0	—	0	(1 → 0)	Ends after the second transfer with an interrupt request to the CPU
				0	—	1	—	
1	1	1	Other than (1 → *)	—	—	—	—	Ends after the first transfer with an interrupt request to the CPU

Note 1. The transfer counter used depends on the transfer modes as follows:
Normal transfer mode — CRA register
Repeat transfer mode — CRAL register
Block transfer mode — CRB register

Note 2. On completion of a data transfer, the counters operate as follows:
1 → 0 in normal and block transfer modes
1 → CRAH in repeat transfer mode
(1 → *) in the table indicates both of these two operations, depending on the mode.

Note 3. Chain transfer can be selected for the second or subsequent transfers. The conditions for the combination of the second transfer and CHNE bit = 1 is omitted.

18.4.1 Transfer Information Read Skip Function

Reading of vector addresses and transfer information can be skipped by setting the DTCCR.RRS bit. When a DTC activation request is generated, the current DTC vector number is compared to the DTC vector number in the previous activation process. When these vector numbers match and the RRS bit is set to 1, the DTC data transfer is performed without reading the vector address and transfer information. However, when the previous transfer is a chain transfer, the vector address and transfer information are read. Additionally, when the transfer counter (CRA register) becomes 0 during the previous normal transfer, or when the transfer counter (CRB register) becomes 0 during the previous block transfer, transfer information is read regardless of the value of the RRS bit. Figure 18.12 shows an example of a transfer information read skip.

To update the vector table and transfer information, set the RRS bit to 0, update the vector table and transfer information, and then set the RRS bit to 1. The stored vector number is discarded by setting the RRS bit to 0. The updated DTC vector table and transfer information are read in the next activation process.

18.4.2 Transfer Information Write-Back Skip Function

When the MRA.SM[1:0] bits or the MRB.DM[1:0] bits are set to address fixed, a part of the transfer information is not written back. Table 18.4 lists the transfer information write-back skip conditions and associated registers. The CRA and CRB registers are written back, and the write-back of the MRA and MRB registers is skipped.

Table 18.3 链转移条件

首次转让				Second transfer*3				DTC transfer
CHNE bit	CHNS bit	DISEL bit	Transfer counter*1,*2	CHNE bit	CHNS bit	DISEL bit	Transfer counter*1,*2	
0	—	0	（1→0）以外	—	—	—	—	在第一次传输后结束
0	—	0	(1 → 0)	—	—	—	—	在第一次传输后结束，向CPU发出中断请求
0	—	1	—	—	—	—	—	
1	0	—	—	0	—	0	（1→0）以外	在第二次转移后结束
				0	—	0	(1 → 0)	在第二次传输后结束，向CPU发出中断请求
				0	—	1	—	
1	1	0	(1→*)以外	—	—	—	—	在第一次传输后结束
1	1	—	(1 → *)	0	—	0	（1→0）以外	在第二次转移后结束
				0	—	0	(1 → 0)	在第二次传输后结束，向CPU发出中断请求
				0	—	1	—	
1	1	1	(1→*)以外	—	—	—	—	在第一次传输后结束，向CPU发出中断请求

Note 1. 使用的传输计数器取决于传输模式，如下所示：
正常传输模式—CRA寄存器重复传输模式—CRAL寄存器
块传输模式——CRB寄存器

Note 2. 数据传输完成后，计数器操作如下：1→0在正常和块传输模式下1→CRAH在重复传输模式下(1→*)表中表示这两种操作，具体取决于模式。

Note 3. 可以为第二次或后续转移选择链转移。省略了第二次传输和CHNE位=1的组合条件。

18.4.1 传输信息读取跳过功能

通过设置DTCCR.RRS位可以跳过向量地址和传输信息的读取。当产生一个DTC激活请求时，当前的DTC向量编号将与之前激活过程中的DTC向量编号进行比较。当这些向量编号匹配且RRS位设置为1时，执行DTC数据传输而不读取向量地址和传输信息。但是，当上一次传输是链式传输时，会读取向量地址和传输信息。此外，如果在上次正常传输期间传输计数器（CRA寄存器）变为0，或者在前一次块传输期间传输计数器（CRB寄存器）变为0，则无论RRS位的值如何，都将读取传输信息。图18.12显示了传输信息读取跳过的示例。

要更新向量表和传输信息，请将RRS位设置为0，更新向量表和传输信息，然后将RRS位设置为1。通过将RRS位设置为0，丢弃存储的向量编号。更新的DTC向量表和传输信息在下一个激活过程中被读取。

18.4.2 传输信息回写跳过功能

当MRA.SM[1:0]位或MRB.DM[1:0]位设置为地址固定时，部分传输信息不会被写回。表18.4列出了传输信息回写跳过条件和相关寄存器。回写CRA和CRB寄存器，跳过回写MRA和MRB寄存器。

Table 18.4 Transfer information write-back skip conditions and applicable registers

MRA.SM[1:0] bits		MRB.DM[1:0] bits			
b3	b2	b3	b2	SAR register	DAR register
0	0	0	0	Skip	Skip
0	0	0	1		
0	1	0	0		
0	1	0	1		
0	0	1	0	Skip	Write-back
0	0	1	1		
0	1	1	0		
0	1	1	1		
1	0	0	0	Write-back	Skip
1	0	0	1		
1	1	0	0		
1	1	0	1		
1	0	1	0	Write-back	Write-back
1	0	1	1		
1	1	1	0		
1	1	1	1		

18.4.3 Normal Transfer Mode

Normal transfer mode allows a 1-byte (8-bit), 1-halfword (16-bit), or 1-word (32-bit) data transfer on a single activation source. The transfer count can be set from 1 to 65,536. Transfer source and destination addresses can be independently set to increment, decrement, or remain fixed. This mode enables an interrupt request to the CPU to be generated at the end of a specified-count transfer.

Table 18.5 lists register functions in normal transfer mode, and Figure 18.5 shows the memory map of normal transfer mode.

Table 18.5 Register functions in normal transfer mode

Register	Description	Value written back by writing transfer information
SAR	Transfer source address	Increment, decrement, or fixed*1
DAR	Transfer destination address	Increment, decrement, or fixed*1
CRA	Transfer counter A	CRA - 1
CRB	Transfer counter B	Not updated

Note 1. Write-back operation is skipped in address-fixed mode.

Table 18.4 传输信息回写跳过条件和适用寄存器

MRA.SM[1:0] bits		MRB.DM[1:0] bits			
b3	b2	b3	b2	SAR寄存器	DAR寄存器
0	0	0	0	Skip	Skip
0	0	0	1		
0	1	0	0		
0	1	0	1		
0	0	1	0	Skip	Write-back
0	0	1	1		
0	1	1	0		
0	1	1	1		
1	0	0	0	Write-back	Skip
1	0	0	1		
1	1	0	0		
1	1	0	1		
1	0	1	0	Write-back	Write-back
1	0	1	1		
1	1	1	0		
1	1	1	1		

18.4.3 正常传输模式

正常传输模式允许在单个激活源上传输1字节（8位）、1半字（16位）或1字（32位）数据。传输计数可以设置为1到65 536。传输源地址和目标地址可以独立设置为递增、递减或保持固定。此模式允许在指定计数传输结束时向CPU生成中断请求。

表18.5列出了正常传输模式下的寄存器功能，图18.5显示了正常传输模式下的内存映射。

Table 18.5 正常传输模式下的寄存器功能

Register	Description	通过写入传输信息回写的值
SAR	传输源地址	递增、递减或固定*1
DAR	转移目的地地址	递增、递减或固定*1
CRA	转帐柜台A	CRA - 1
CRB	转帐柜台B	未更新

Note 1. 在地址固定模式下会跳过回写操作。

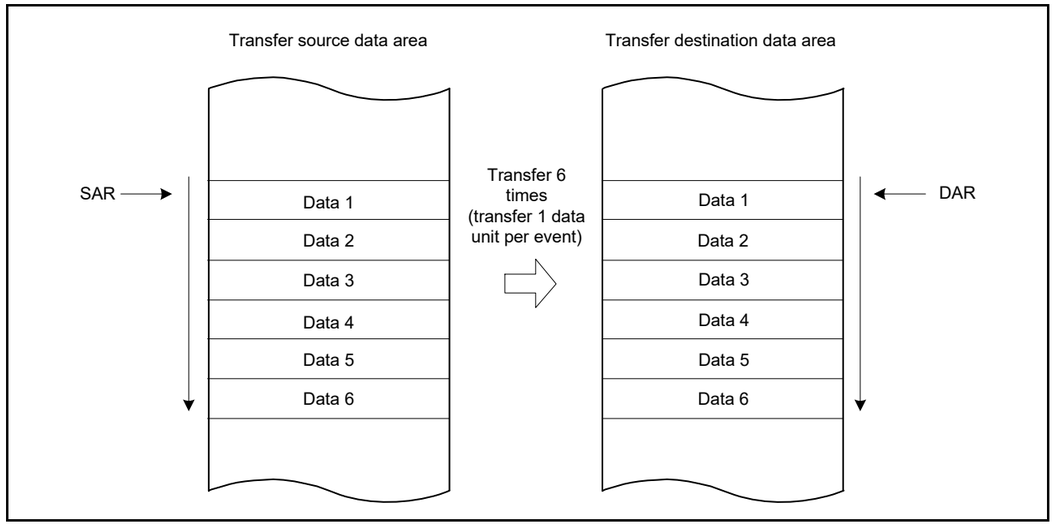


Figure 18.5 Memory map of normal transfer mode (MRA.SM[1:0] = 10b, MRB.DM[1:0] = 10b, CRA = 0006h)

18.4.4 Repeat Transfer Mode

Repeat transfer mode allows a 1-byte (8-bit), 1-halfword (16-bit), or 1-word (32-bit) data transfer on a single activation source. Specify either transfer source or transfer destination for the repeat area in the MRB.DTS bit. The transfer count can be set from 1 to 256. When the specified-count transfer is complete, the initial value of the address register specified in the repeat area is restored, the initial value of the transfer counter is restored, and transfer is repeated. The other address register is incremented or decremented continuously or remains unchanged.

When the transfer counter CRAL decrements to 00h in repeat transfer mode, the CRAL value is updated to the value set in the CRAH register. As a result, the transfer counter does not become 00h, which disables interrupt requests to the CPU when the MRB.DISEL bit is set to 0. An interrupt request to the CPU is generated when the specified data transfer is complete.

Table 18.6 lists the register functions in repeat transfer mode, and Figure 18.6 shows the memory map of repeat transfer mode.

Table 18.6 Register functions in repeat transfer mode

Register	Description	Value written back by writing transfer information	
		When CRAL is not 1	**When CRAL is 1**
SAR	Transfer source address	Increment, decrement, or fixed*1	• When the MRB.DTS bit is 0 Increment, decrement, or fixed*1 • When the MRB.DTS bit is 1 SAR register initial value.
DAR	Transfer destination address	Increment, decrement, or fixed*1	• When the MRB.DTS bit is 0 DAR register initial value • When the MRB.DTS bit is 1 Increment, decrement, or fixed.*1
CRAH	Holds transfer counter	CRAH	CRAH
CRAL	Transfer counter A	CRAL - 1	CRAH
CRB	Transfer counter B	Not updated	Not updated

Note 1. Write-back is skipped in address-fixed mode.

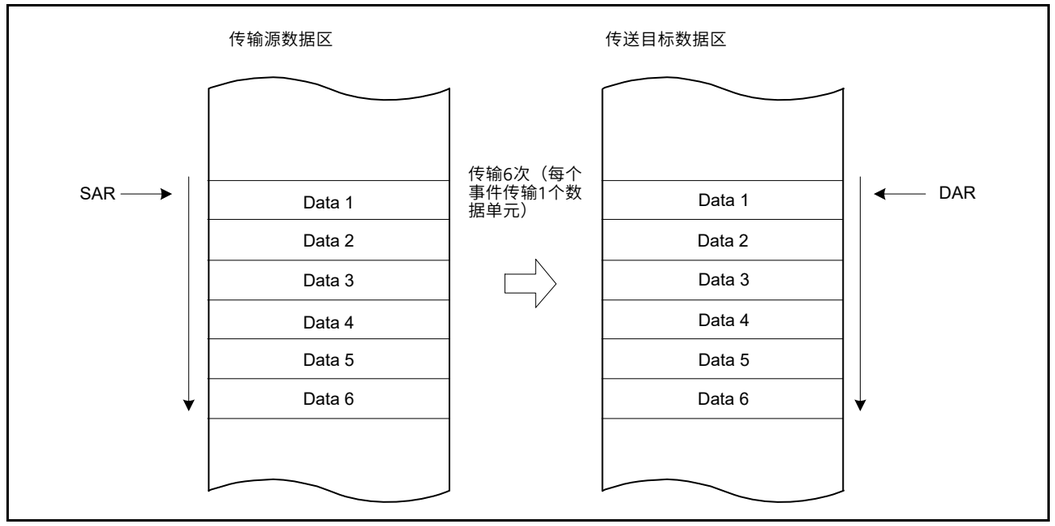


Figure 18.5 正常传输模式的内存映射(MRA.SM[1:0]=10b MRB.DM[1:0]=10b CRA=0006h)

18.4.4 重复传输模式

重复传输模式允许在单个激活源上传输1字节（8位）、1半字（16位）或1字（32位）数据。在MRB.DTS位中指定重复区域的传输源或传输目标。传送计数可设置为1到256。当指定计数传送完成时，重复区域中指定的地址寄存器的初始值被恢复，传送计数器的初始值被恢复，并重复传送。另一个地址寄存器连续递增或递减或保持不变。

当传输计数器CRAL在重复传输模式下递减到00h时，CRAL值将更新为CRAH寄存器中设置的值。因此，传输计数器不会变为00h，这会在MRB.DISEL位设置为0时禁用对CPU的中断请求。当指定的数据传输完成时，会向CPU发出中断请求。

表18.6列出了重复传输模式下的寄存器功能，图18.6显示了重复传输模式的内存映射。

Table 18.6 重复传输模式下的寄存器功能

Register	Description	通过写入传输信息回写的值	
		当CRAL不为1时	**当CRAL为1时**
SAR	传输源地址	递增、递减或固定*1	当MRB.DTS位为0时递增、递减或固定*1 当MRB.DTS位为1时SAR寄存器初始值。
DAR	转移目的地地址	递增、递减或固定*1	当MRB.DTS位为0时DAR寄存器初始值 当MRB.DTS位为1时递增、递减或固定。*1
CRAH	持有转账柜台	CRAH	CRAH
CRAL	转帐柜台A	CRAL - 1	CRAH
CRB	转帐柜台B	未更新	未更新

Note 1. 在地址固定模式下会跳过回写。

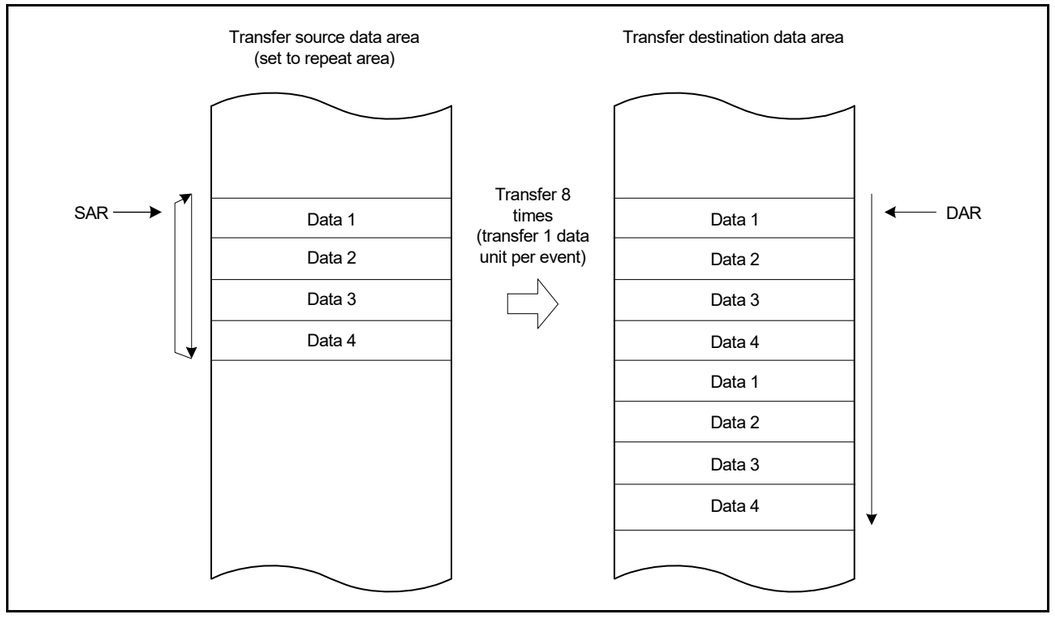


Figure 18.6 Memory map of repeat transfer mode when the transfer source is a repeat area (MRA.SM[1:0] = 10b, MRB.DM[1:0] = 10b, CRAH = 04h)

18.4.5 Block Transfer Mode

Block transfer mode allows single-block data transfer on a single activation source. Transfer source or transfer destination for the block area must be specified in the MRB.DTS bit. The block size can be set from 1 to 256 bytes, 1 to 256 halfwords (2 to 512 bytes), or 1 to 256 words (4 to 1024 bytes). When transfer of the specified block completes, the initial values of the block size counter CRAL and the address register (the SAR register when the MRB.DTS bit = 1 or the DAR register when the DTS bit = 0) specified in the block area are restored. The other address register is incremented or decremented continuously or remains unchanged.

The transfer count (block count) can be set from 1 to 65,536. This mode enables an interrupt request to the CPU to be generated at the end of the specified-count block transfer.

Table 18.7 lists register functions in block transfer mode, and Figure 18.7 shows the memory map of block transfer mode.

Table 18.7 Register functions in block transfer mode

Register	Description	Value written back by writing transfer information
SAR	Transfer source address	• When MRB.DTS bit is 0 Increment, decrement, or fixed*1 • When MRB.DTS bit is 1 SAR register initial value.
DAR	Transfer destination address	• When MRB.DTS bit is 0 DAR register initial value • When MRB.DTS bit is 1 Increment, decrement, or fixed.*1
CRAH	Holds the block size	CRAH
CRAL	Block size counter	CRAH
CRB	Block transfer counter	CRB - 1

Note 1. Write-back is skipped in address-fixed mode.

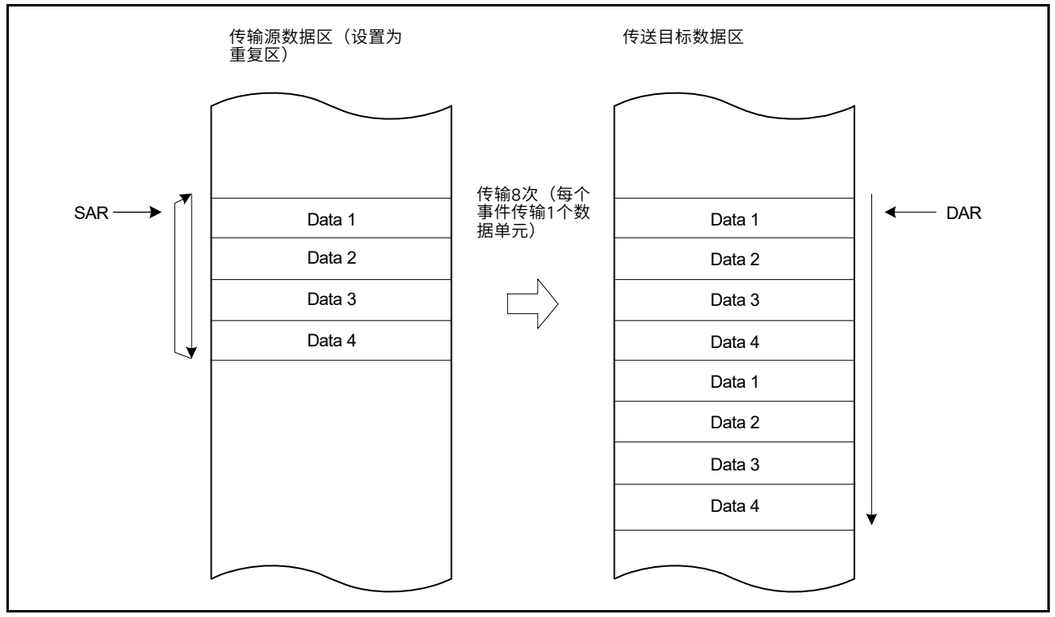


Figure 18.6 传输源为重复区域时重复传输模式的内存映射（MRA.SM[1:0]=10b MRB.DM[1:0]=10b CRAH=04h）

18.4.5 块传输模式

块传输模式允许在单个激活源上进行单块数据传输。块区域的传输源或传输目标必须在MRB.DTS位中指定。块大小可以设置为1到256字节、1到256个半字（2到512字节）或1到256字（4到1024字节）。当指定块的传输完成时，块区域中指定的块大小计数器CRAL和地址寄存器（当MRB.DTS位=1时为SAR寄存器或当DTS位=0时为DAR寄存器）的初始值是恢复。另一个地址寄存器连续递增或递减或保持不变。

传输计数（块计数）可以设置为1到65 536。此模式允许在指定计数块传输结束时向CPU生成中断请求。

表18.7列出了块传输模式下的寄存器功能，图18.7显示了块传输模式的内存映射。

Table 18.7 块传输模式下的寄存器功能

Register	Description	通过写入传输信息回写的值
SAR	传输源地址	当MRB.DTS位为0时递增、递减或固定*1 当MRB.DTS位为1时SAR寄存器初始值。
DAR	转移目的地地址	当MRB.DTS位为0时DAR寄存器初始值 当MRB.DTS位为1时递增、递减或固定。*1
CRAH	保存块大小	CRAH
CRAL	块大小计数器	CRAH
CRB	块传输计数器	CRB - 1

Note 1. 在地址固定模式下会跳过回写。

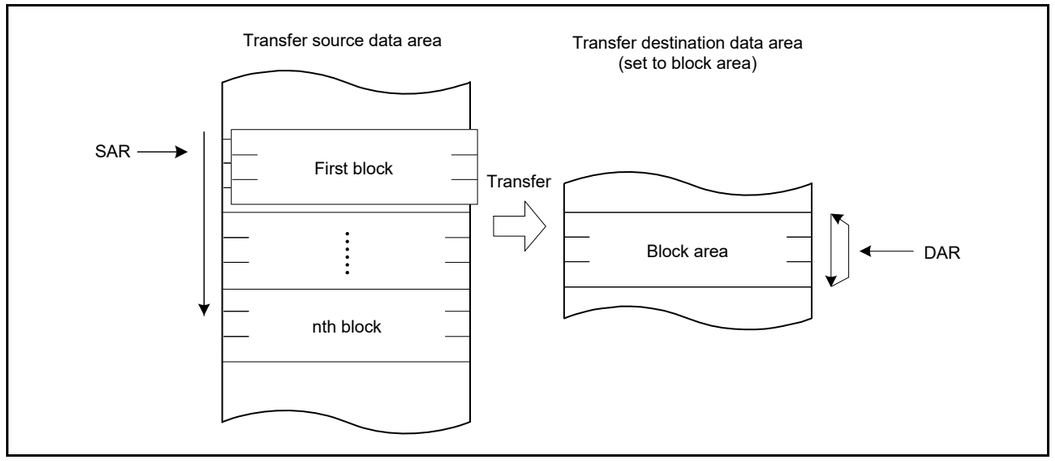


Figure 18.7 Memory map of block transfer mode

18.4.6 Chain Transfer

Setting the MRB.CHNE bit to 1 allows chain transfer to be performed continuously on a single activation source. If MRB.CHNE is set to 1 and CHNS to 0, an interrupt request to the CPU is not generated on completion of the specified number of rounds of transfer or by setting the MRB.DISEL bit to 1. An interrupt request is sent to the CPU each time DTC data transfer is performed. Data transfer has no effect on the ICU.IELSRn.IR bit of the activation source.

The SAR, DAR, CRA, CRB, MRA, and MRB registers can be set independently of each other to define the data transfer. Figure 18.8 shows a chain transfer operation.

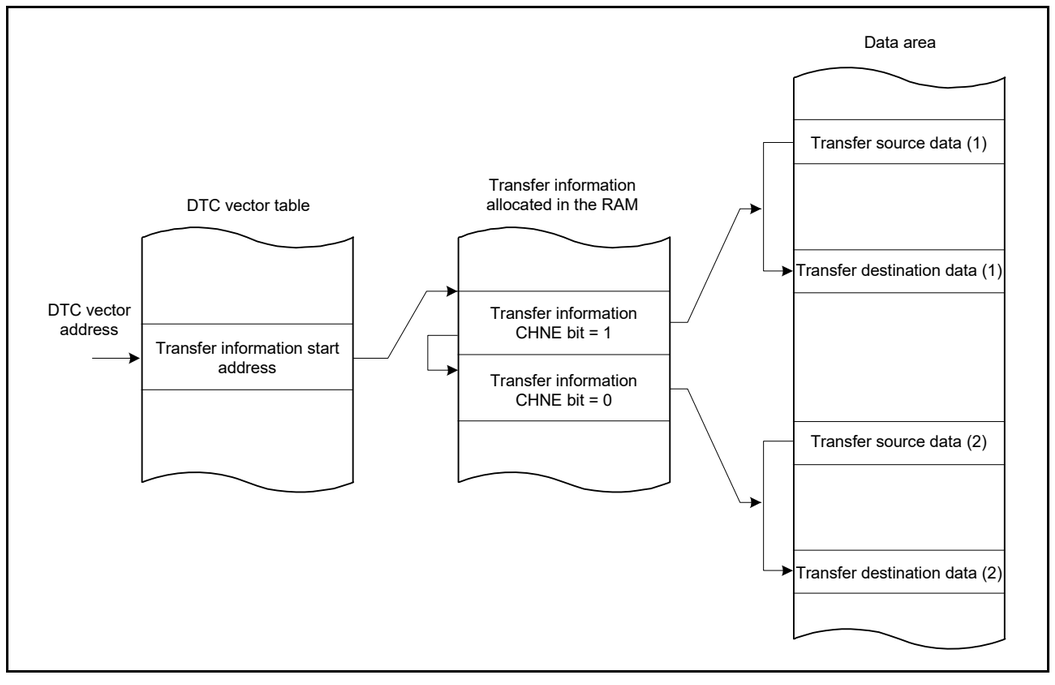


Figure 18.8 Chain transfer operation

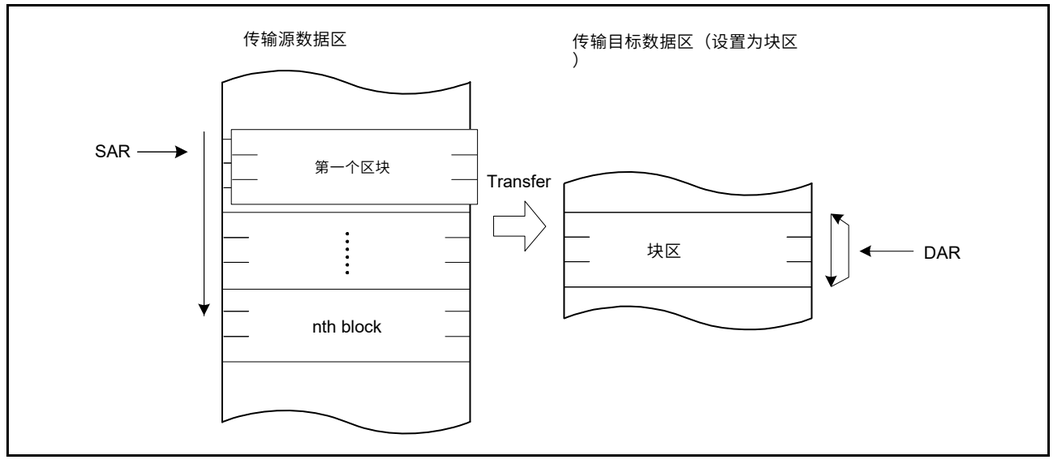


Figure 18.7 块传输模式的内存映射

18.4.6 链转移

将MRB.CHNE位设置为1允许在单个激活源上连续执行链传输。如果
MRB.CHNE设置为1，CHNS设置为0，在完成指定的传输轮数或将MRB.DISEL位设置为1时不会向CPU产生中断请求。向CPU发送中断请求每次执行DTC数据传输。数据传输对激活源的ICU.IELSRn.IR位没有影响。

SAR、DAR、CRA、CRB、MRA和MRB寄存器可以相互独立设置以定义数据传输。
图18.8显示了一个链式转移操作。

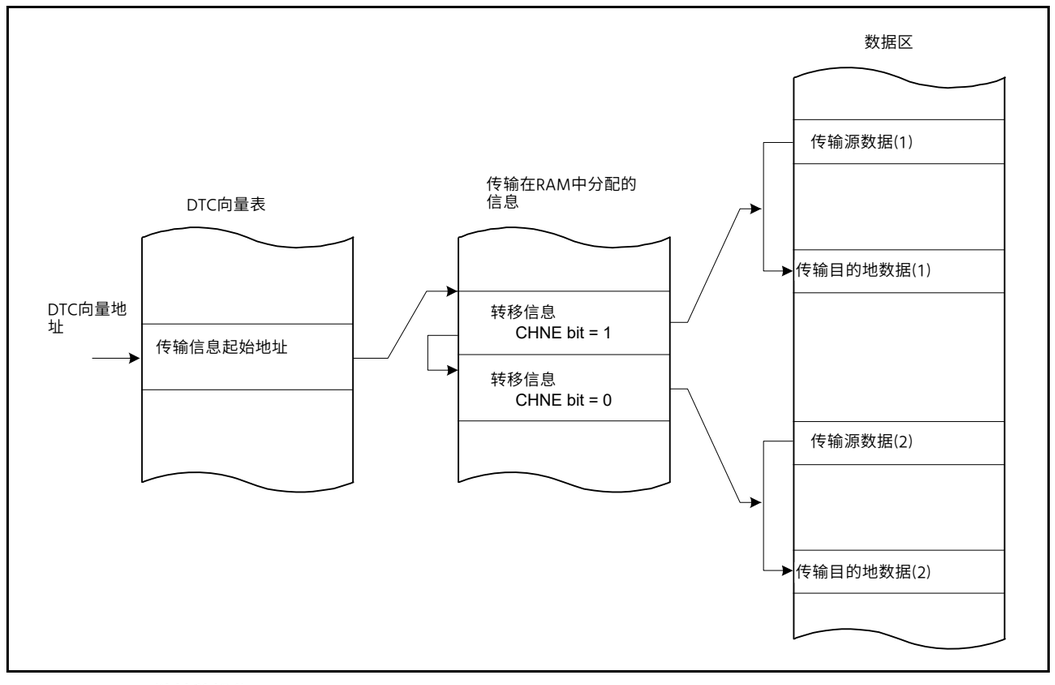


Figure 18.8 链转移操作

Writing 1 to the MRB.CHNE and CHNS bits enables chain transfer to be performed only after completion of the specified data transfer. In repeat transfer mode, chain transfer is performed after completion of the specified data transfer. For details on chain transfer conditions, see Table 18.3, Chain transfer conditions.

18.4.7 Operation Timing

Figure 18.9 to Figure 18.12 are timing diagrams that show the minimum number of execution cycles.

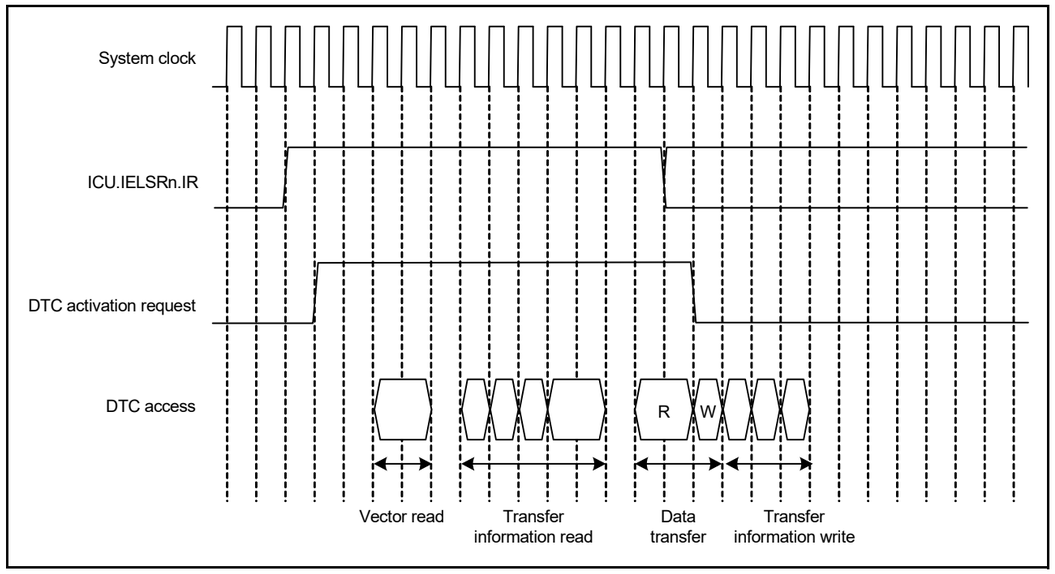


Figure 18.9 Example 1 of DTC operation timing in normal transfer and repeat transfer modes

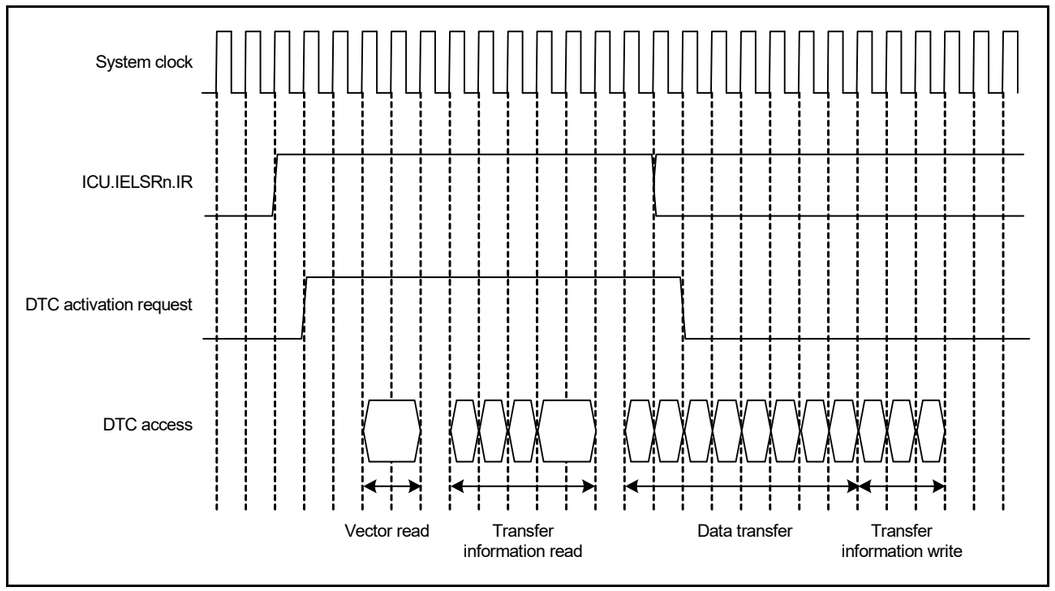


Figure 18.10 Example 2 of DTC operation timing in block transfer mode when the block size = 4

将1写入MRB.CHNE和CHNS位可以使链式传输仅在完成指定的数据传输后执行。在重复传输模式下，在完成指定的数据传输后执行链式传输。有关链转移条件的详细信息，请参见表18.3，链转移条件。

18.4.7 操作时间

图18.9至图18.12是显示最小执行周期数的时序图。

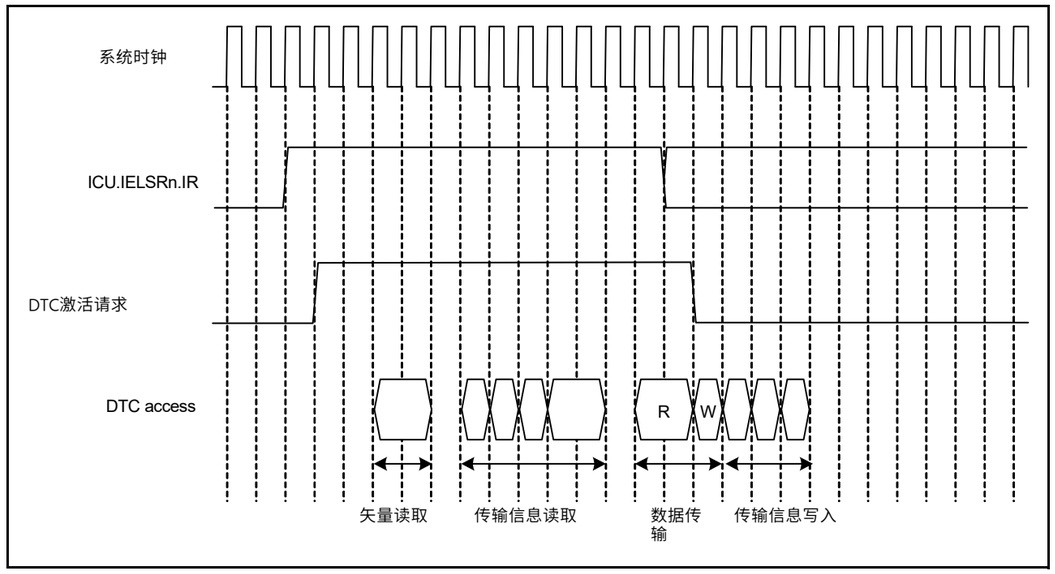


Figure 18.9 正常传输和重复传输模式下的DTC操作时序示例1

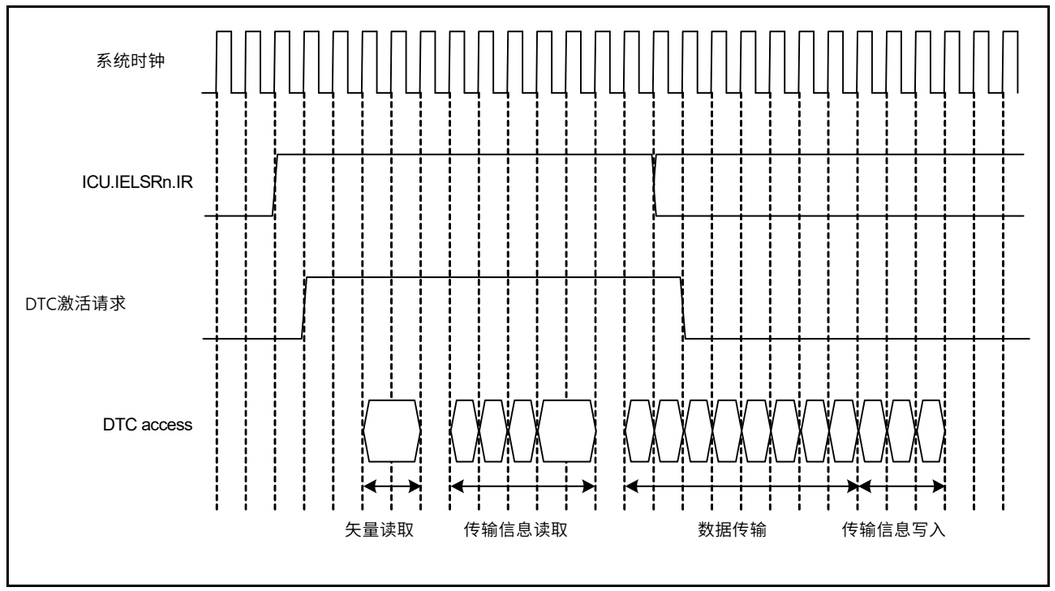


Figure 18.10 块大小=4时块传输模式下的DTC操作时序示例2

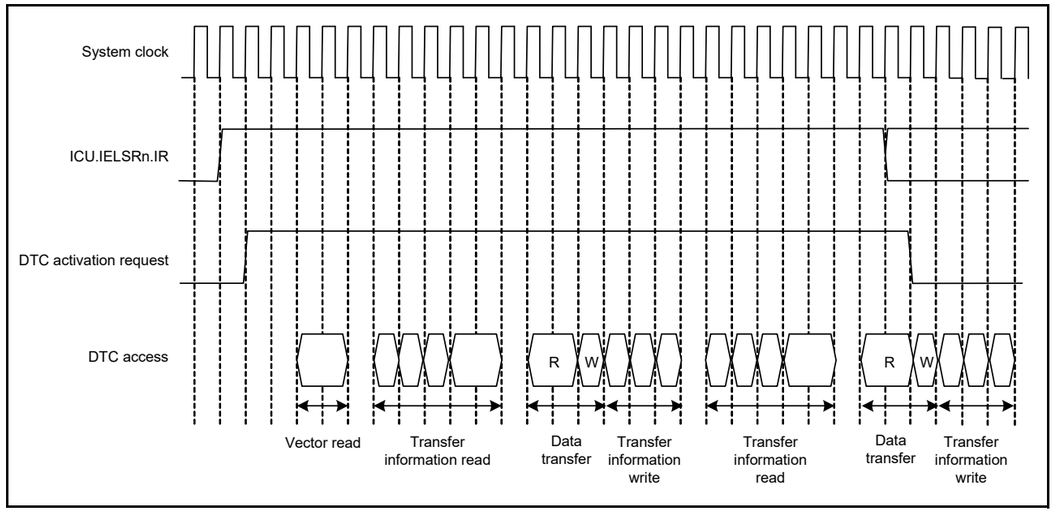
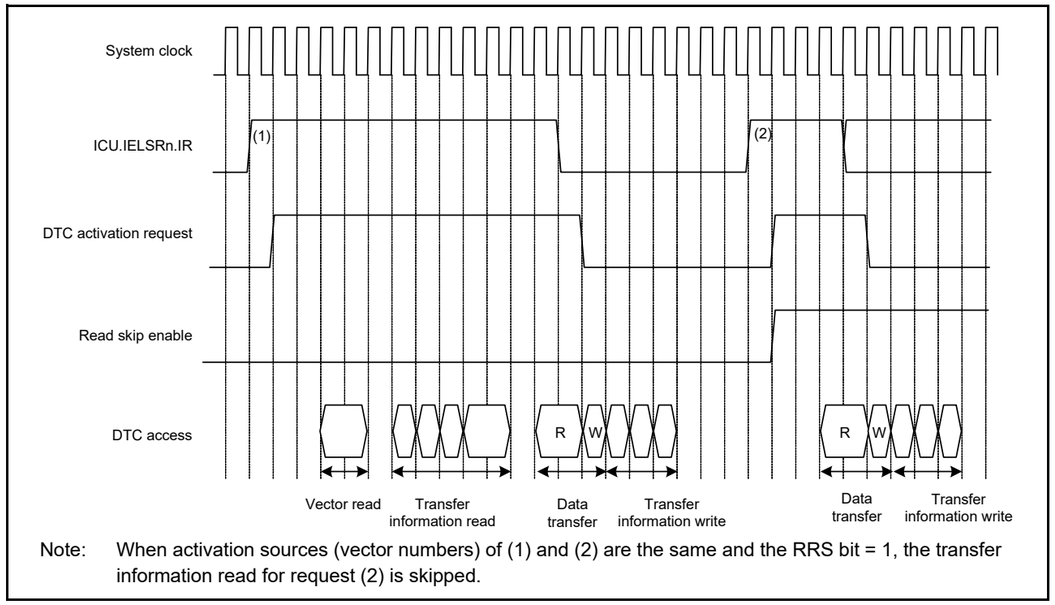


Figure 18.11 Example 3 of DTC operation timing for chain transfer



Note: When activation sources (vector numbers) of (1) and (2) are the same and the RRS bit = 1, the transfer information read for request (2) is skipped.

Figure 18.12 Example of operation when a transfer information read is skipped, with the vector, transfer information, and transfer destination data on the SRAM, and the transfer source data on the peripheral module

18.4.8 Execution Cycles of DTC

Table 18.8 lists the execution cycles of single data transfer of the DTC.

For the order of the execution states, see section 18.4.7, Operation Timing.

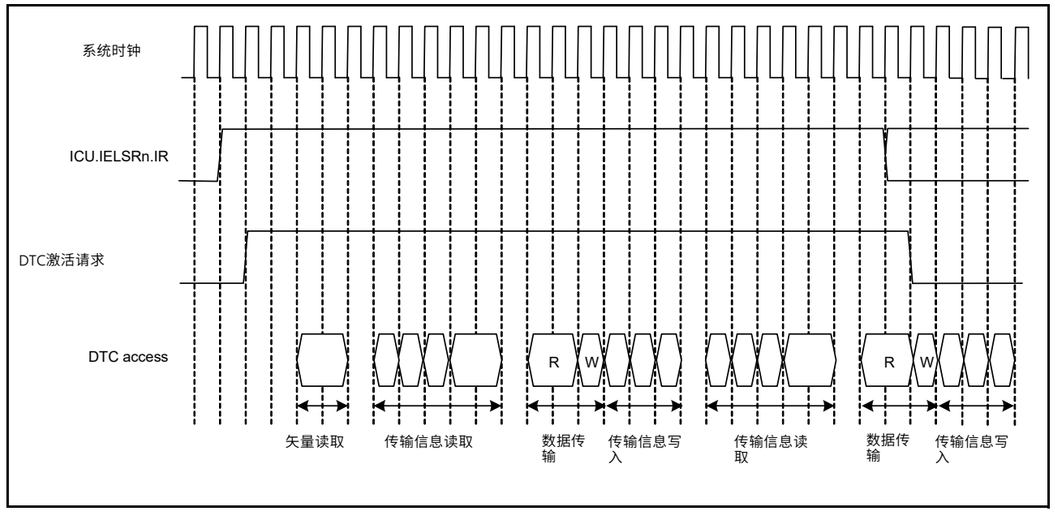
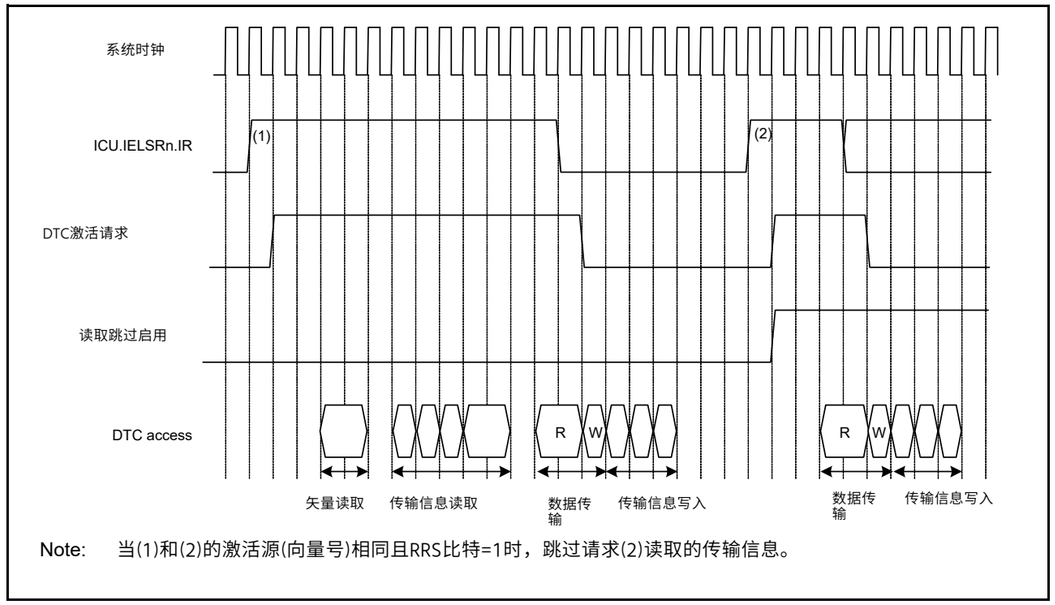


Figure 18.11 链转移的DTC操作时序示例3



Note: 当(1)和(2)的激活源(向量号)相同且RRS比特=1时，跳过请求(2)读取的传输信息。

Figure 18.12 跳过传输信息读取时的操作示例，向量、传输信息和传输目标数据位于SRAM上，传输源数据位于外围模块上

18.4.8 DTC的执行周期

表18.8列出了DTC单次数据传输的执行周期。

有关执行状态的顺序，请参阅第18.4.7节，操作时序。

Table 18.8 Execution cycles of DTC

Transfer mode	Vector read		Transfer information read		Transfer information write			Data transfer		Internal operation	
								Read	Write		
Normal	Cv + Cs1 + 1	0*1	4 × (Ci + Cs1) + 1	0*1	3 × (Ci + Cs1) + 1*2	2 × (Ci + Cs1) + 1*3	(Ci + Cs1)*4	Cr + Cs2 + 1	Cw + Cs2 + 1	2	0*1
Repeat								Cr + Cs2 + 1	Cw + Cs2 + 1		
Block*5								P × (Cr + Cs2)	P × (Cw + Cs2)		

Note 1. When transfer information read is skipped.
Note 2. When neither SAR nor DAR is set to address-fixed mode.
Note 3. When SAR or DAR is set to address-fixed mode.
Note 4. When SAR and DAR are set to address-fixed mode.
Note 5. When the block size is 2 or more. If the block size is 1, the cycle number for normal transfer is applied.

P: Block size (initial settings of CRAH and CRAL)
Cv: Cycles for access to vector transfer information storage destination
Ci: Cycles for access to transfer information storage destination address
Cr: Cycles for access to data read destination
Cw: Cycles for access to data write destination
Cs1: When accessing SRAMHS: 2 cycles.
When accessing elsewhere: 0 cycles.
When a slave bus changes by a read/write data transfer, add 1 more cycle.
Cs2: When accessing SRAMHS and peripheral modules related to system control: 2 cycles.
When accessing elsewhere: 0 cycle.
When a slave bus change by a read/write data transfer, add 1 more cycle.
The unit is system clocks (ICLK) + 1 in the Vector read, Transfer information read, and Data transfer read columns and 2 in the Internal operation column.
Cv, Ci, Cr, and Cw vary depending on the corresponding access destination. For the number of cycles for respective access destinations, see section 53, SRAM, section 55, Flash Memory, and section 15.2.3, External Bus.
The frequency ratio of the system clock and peripheral clock is also taken into consideration.
The DTC response time is the time from when the DTC activation source is detected until DTC transfer starts.
This table does not include the time until DTC data transfer starts after the DTC activation source becomes active.

18.4.9 DTC Bus Mastership Release Timing

The DTC does not release bus mastership during transfer information reads. Before the transfer information is read or written, the bus is arbitrated according to the priority determined by the bus master arbitrator. For bus arbitration, see section 15, Buses.

18.5 DTC Setting Procedure

Before using the DTC, set the DTC Vector Base Register (DTCVBR). Figure 18.13 shows the procedure for setting the DTC.

Table 18.8 DTC的执行周期

传输模式	矢量读取		传输信息读取		传输信息写入			数据传输		内部运作	
								Read	Write		
Normal	Cv + Cs1 + 1	0*1	4 × (Ci + Cs1) + 1	0*1	3 × (Ci + Cs1) + 1*2	2 × (Ci + Cs1) + 1*3	(Ci + Cs1)*4	Cr + Cs2 + 1	Cw + Cs2 + 1	2	0*1
Repeat								Cr + Cs2 + 1	Cw + Cs2 + 1		
Block*5								P × (Cr + Cs2)	P × (Cw + Cs2)		

Note 1. 跳过传输信息读取时。
Note 2. 当SAR和DAR均未设置为地址固定模式时。
Note 3. 当SAR或DAR设置为地址固定模式时。
Note 4. 当SAR和DAR设置为地址固定模式时。
Note 5. 当块大小为2或更大时。如果块大小为1，则应用正常传输的周期数。

P：块大小（CRAH和CRAL的初始设置）
Cv：访问向量传输信息存储目标的周期Ci：访问传输信息存储目标地址的周期
Cr：访问数据读取目标的周期Cw：访问数据写入目标的周期
Cs1：访问SRAMHS时：2个周期。在其他地方访问时：0个周期。
当从总线因读写数据传输而改变时，再增加1个周期。
Cs2：访问SRAMHS和与系统控制相关的外围模块时：2个周期。
在别处访问时：0循环。
当从总线发生读写数据传输变化时，再增加1个周期。
单位是Vectorread、Transferinformationread和Datatransferread列中的系统时钟(ICLK)+1和Internaloperation列中的2。Cv、Ci、Cr和Cw根据相应的访问目的地而变化。有关各个访问目标的周期数，请参见第53节，SRAM，第55节，闪存和第15.2.3节，外部总线。系统时钟和外设时钟的频率比也被考虑在内。
DTC响应时间是从检测到DTC激活源到DTC传输开始的时间。
此表不包括从DTC激活源激活到DTC数据传输开始的时间。

18.4.9 DTC总线主控释放时序

在传输信息读取期间，DTC不会释放总线控制权。在读取或写入传输信息之前，根据总线主仲裁器确定的优先级对总线进行仲裁。对于总线仲裁，请参见第15节，总线。

18.5 DTC设置程序

在使用DTC之前，请设置DTC向量基址寄存器(DTCVBR)。图18.13显示了设置DTC.

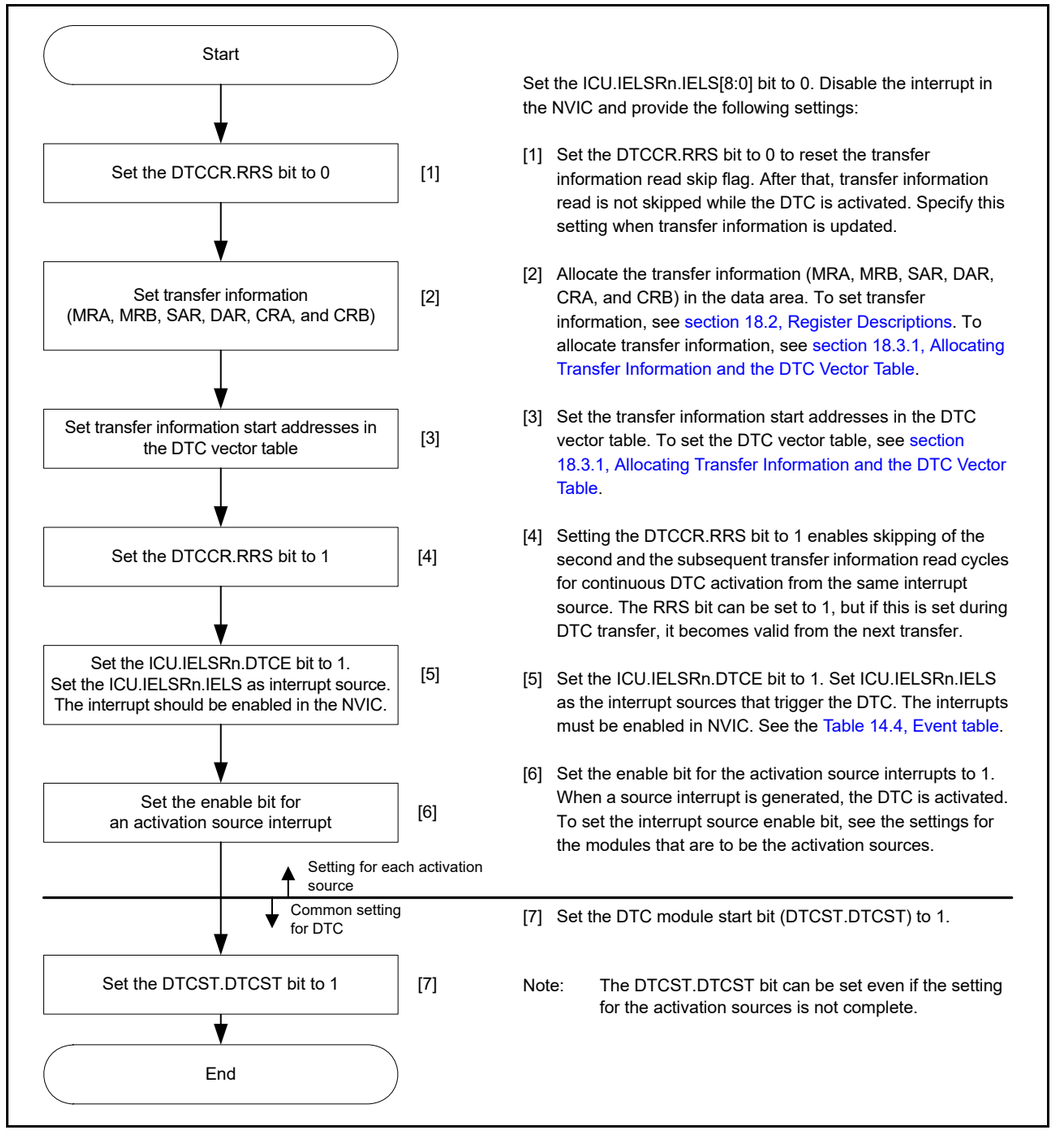


Figure 18.13 DTC setting procedure

18.6 Examples of DTC Usage

18.6.1 Normal Transfer

This section provides an example of DTC usage and its application when receiving 128 bytes of data from an SCI.

(1) Transfer information settings

In the MRA register, select a fixed source address (MRA.SM[1:0] = 00b), normal transfer mode (MRA.MD[1:0] = 00b), and byte-sized transfer (MRA.SZ[1:0] = 00b). In the MRB register, specify incrementation of the destination address (MRB.DM[1:0] = 10b) and single data transfer by a single interrupt (MRB.CHNE = 0 and MRB.DISEL = 0). The MRB.DTS bit can be set to any value. Set the RDR register address of the SCI in the SAR register, the start address of

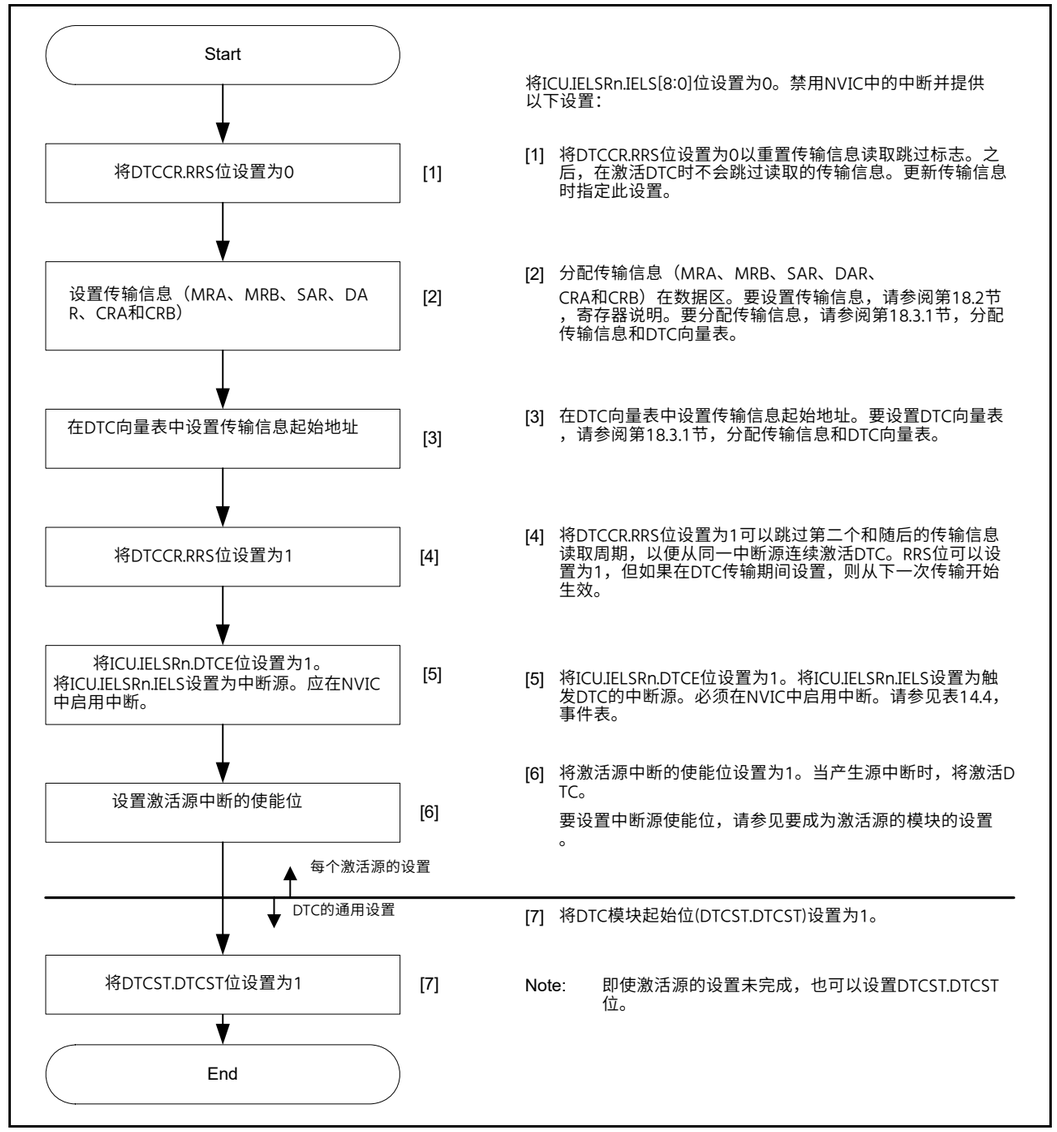


Figure 18.13 DTC设置程序

18.6 DTC使用示例

18.6.1 正常转移

本节提供从SCI接收128字节数据时的DTC用法及其应用示例。

(1) 传输信息设置

在MRA寄存器中，选择固定源地址（MRA.SM[1:0]=00b）、正常传输模式（MRA.MD[1:0]=00b）和字节大小传输（MRA.SZ[1:0]=00b)。在MRB寄存器中，指定目标地址的递增(MRB.DM[1:0]=10b)和单个中断的单个数据传输(MRB.CHNE=0和MRB.DISEL=0)。MRB.DTS位可以设置为任何值。在SAR寄存器中设置SCI的RDR寄存器地址，

the SRAM area for data storage in the DAR register, and 128 (0080h) in the CRA register. The CRB register can be set to any value.

(2) DTC vector table setting

The start address of the transfer information for the RXI interrupt is set in the vector table for the DTC.

(3) ICU settings and DTC module activation

Set the ICU.IELSRn.DTCE bit to 1 and set ICU.IELSRn.IELS as the SCI interrupt. The interrupt must be enabled in the NVIC. Set the DTCST.DTCST bit to 1.

(4) SCI settings

Enable the RXI interrupt by setting the SCR.RIE bit in the SCI to 1. If a reception error occurs during the SCI receive operation, reception stops. To manage this, use settings that allow the CPU to accept receive error interrupts.

(5) DTC transfer

Every time a reception of 1 byte by the SCI is complete, an RXI interrupt is generated to activate the DTC. The DTC transfers the received byte from the RDR of the SCI to the SRAM, after which the DAR register is incremented and the CRA register is decremented.

(6) Interrupt handling

After 128 rounds of data transfer are complete and the value in the CRA register becomes 0, an RXI interrupt request is generated for the CPU. Complete the process in the handling routine for this interrupt.

18.6.2 Chain Transfer

This section provides an example of chain transfer by the DTC and describes its use in the output of pulses by the General PWM Timer (GPT). You can use chain transfer to transfer PWM timer compare data and change the period of the PWM timer for GPT.

For the first of the chain transfers, normal transfer mode is specified for transfer to the GPT32m.GTCCRC register. For the second transfer, normal transfer mode is specified for transfer to the GPT32m.GTCCRE register. For the third transfer, normal transfer mode is specified for transfer to the GPT32m.GTPBR register. This is because clearing of the activation source and generation of an interrupt on completion of the specified number of transfers are restricted to the third of the chain transfers, that is, transfer while MRB.CHNE = 0.

The following example shows how to use the counter overflow interrupt with a GPT32EH0.GTPR register as an activating source for the DTC.

(1) First transfer information settings

Set up transfer to the GPT32EH0.GTCCRC register:

1. In the MRA register, select incrementation of the source address (MRA.SM[1:0] = 10b).
2. Set the transfer to normal transfer mode (MRA.MD[1:0] = 00b) and word-sized transfer (MRA.SZ[1:0] = 10b).
3. In the MRB register, select the destination address as fixed (MRB.DM[1:0] = 00b) and set up chain transfer (MRB.CHNE = 1 and MRB.CHNS = 0).
4. Set the SAR register to the first address of the data table.
5. Set the DAR register to the address of the GPT32EH0.GTCCRC register.
6. Set the CRAH and CRAL registers to the size of the data table. The CRB register can be set to any value.

(2) Second transfer information settings

Set up transfer to the GPT32EH0.GTCCRE register:

1. In the MRA register, select incrementation of the source address (MRA.SM[1:0] = 10b).
2. Set the transfer to normal transfer mode (MRA.MD[1:0] = 00b) and word-sized transfer (MRA.SZ[1:0] = 10b).
3. In the MRB register, select the destination address as fixed (MRB.DM[1:0] = 00b) and set up chain transfer (MRB.CHNE = 1 and MRB.CHNS = 0).

DAR寄存器中用于数据存储的SRAM区域，以及CRA寄存器中的128(0080h)。CRB寄存器可以设置为任何值。

(2) DTC向量表设置

RXI中断的传输信息的起始地址在DTC的向量表中设置。

(3) ICU设置和DTC模块激活

将ICU.IELSRn.DTCE位设置为1，并将ICU.IELSRn.IELS设置为SCI中断。中断必须在启用
英伟达。将DTCST.DTCST位设置为1。

(4) SCI设置

通过将SCI中的SCR.RIE位设置为1来启用RXI中断。如果在SCI接收操作期间发生接收错误，则接收停止。要管理此问题，请使用允许CPU接受接收错误中断的设置。

(5) DTC transfer

每次SCI完成1个字节的接收，就会产生一个RXI中断来激活DTC。DTC将接收到的字节从SCI的RDR传输到SRAM，之后DAR寄存器递增，CRA寄存器递减。

(6) 中断处理

在128轮数据传输完成后，CRA寄存器中的值变为0，产生一个RXI中断请求给CPU。完成该中断处理程序中的处理。

18.6.2 链转移

本节提供了DTC链传输的示例，并描述了其在DTC输出脉冲中的使用
通用PWM定时器(GPT)。您可以使用链传输来传输PWM定时器比较数据并更改GPT的PWM定时器的周期。

对于第一个链传输，指定正常传输模式以传输到GPT32m.GTCCRC寄存器。对于第二次传输，指定正常传输模式以传输到GPT32m.GTCCRE寄存器。对于第三次传输，指定正常传输模式以传输到GPT32m.GTPBR寄存器。这是因为在完成指定数量的传输时清除激活源和产生中断仅限于链传输的第三个，即在MRB.CHNE=0时传输。

以下示例显示如何使用带有GPT32EH0.GTPR寄存器的计数器溢出中断作为DTC的激活源。

(1) 首次转账信息设置

设置传输到GPT32EH0.GTCCRC寄存器：

1. 在MRA寄存器中，选择源地址的递增(MRA.SM[1:0]=10b)。
2. 将传输设置为正常传输模式(MRA.MD[1:0]=00b)和字大小传输(MRA.SZ[1:0]=10b)。
3. 在MRB寄存器中，选择固定的目标地址（MRB.DM[1:0]=00b）并设置链式传输（MRB.CHNE=1和MRB.CHNS=0）。
4. 将SAR寄存器设置为数据表的首地址。
5. 将DAR寄存器设置为GPT32EH0.GTCCRC寄存器的地址。
6. 将CRAH和CRAL寄存器设置为数据表的大小。CRB寄存器可以设置为任何值。

(2) 二转信息设置

设置传输到GPT32EH0.GTCCRE寄存器：

1. 在MRA寄存器中，选择源地址的递增(MRA.SM[1:0]=10b)。
2. 将传输设置为正常传输模式(MRA.MD[1:0]=00b)和字大小传输(MRA.SZ[1:0]=10b)。
3. 在MRB寄存器中，选择固定的目标地址（MRB.DM[1:0]=00b）并设置链式传输（MRB.CHNE=1和MRB.CHNS=0）。

4. Set the SAR register to the first address of the data table.
5. Set the DAR register to the address of the GPT32EH0.GTCCRE register.
6. Set the CRAH and CRAL registers to the size of the data table. The CRB register can be set to any value.

(3) Third transfer information settings

Set up transfer to the GPT32EH0.GTPBR registers:

1. In the MRA register, select incrementation of the source address (MRA.SM[1:0] = 10b).
2. Set the transfer to normal transfer mode (MRA.MD[1:0] = 00b) and word-sized transfer (MRA.SZ[1:0] = 10b).
3. In the MRB register, select the destination address as fixed (MRB.DM[1:0] = 00b) and set up single data transfer per interrupt (MRB.CHNE = 0, MRB.DISEL = 0). The MRB.DTS bit can be set to any value.
4. Set the SAR register to the first address of the data table.
5. Set the DAR register to the address of the GPT32EH0.GTPBR register.
6. Set the CRA register to the size of the data table. The CRB register can be set to any value.

(4) Transfer information assignment

Place the transfer information for use in the transfer to GPT32EH0.GTPBR immediately after the transfer control information for use in the GPT32EH0.GTCCRC and GPT32EH0.GTCCRE registers.

(5) DTC vector table

In the DTC vector table, set the address where the transfer control information for use in transfer to the GPT32EH0.GTCCRC and GPT32EH0.GTCCRE registers starts.

(6) ICU settings and DTC module activation

1. Set the ICU.IELSRn.DTCE bit associated with the GPT32EH0 counter overflow interrupt.
2. Set ICU.IELSRn.IELS[8:0] to 182 (B6h) for the GPT32EH0 counter overflow.
3. Set the DTCST.DTCST bit to 1.

(7) GPT settings

1. Set the GPT32EH0.GTIOR register so that the GTCCRA and GTCCRB registers operate as output compare registers.
2. Set the default PWM timer compare values in the GPT32EH0.GTCCRA and GPT32EH0.GTCCRB registers and the next PWM timer compare values in the GPT32EH0.GTCCRC and GPT32EH0.GTCCRE registers.
3. Set the default PWM timer period values in the GPT32EH0.GTPR register and the next PWM timer period values in the GPT32EH0.GTPBR register.
4. Set 1 to the output bit in PmnPFS.PDR, and set 00011b to the peripheral select bits in PmnPFS.PSEL[4:0].

(8) GPT activation

Set the GPT32EH0.GTSTR.CSTRT bit to 1 to start the GPT32EH0.GTCNT counter.

(9) DTC transfer

Each time a GPT32EH0 counter overflow is generated with the GPT32EH0.GTPR register, the next PWM timer compare values are transferred to the GPT32EH0.GTCCRC and GPT32EH0.GTCCRE registers. The setting for the next PWM timer period is transferred to the GPT32EH0.GTPBR register.

(10) Interrupt handling

After the specified rounds of data transfer are complete, for example when the value in the CRA register for GPT transfer becomes 0, a GPT counter overflow interrupt request is issued for the CPU. Complete the process for this interrupt in the handling routine.

4. 将SAR寄存器设置为数据表的首地址。
5. 将DAR寄存器设置为GPT32EH0.GTCCRE寄存器的地址。
6. 将CRAH和CRAL寄存器设置为数据表的大小。CRB寄存器可以设置为任何值。

(3) 第三次转账信息设置

设置传输到GPT32EH0.GTPBR寄存器：

1. 在MRA寄存器中，选择源地址的递增(MRA.SM[1:0]=10b)。
2. 将传输设置为正常传输模式(MRA.MD[1:0]=00b)和字大小传输(MRA.SZ[1:0]=10b)。
3. 在MRB寄存器中，选择固定的目标地址（MRB.DM[1:0]=00b）并设置每次中断的单次数据传输（MRB.CHNE=0，MRB.DISEL=0）。MRB.DTS位可以设置为任何值。
4. 将SAR寄存器设置为数据表的首地址。
5. 将DAR寄存器设置为GPT32EH0.GTPBR寄存器的地址。
6. 将CRA寄存器设置为数据表的大小。CRB寄存器可以设置为任何值。

(4) 转移信息分配

将用于传输到GPT32EH0.GTPBR的传输信息放置在GPT32EH0.GTCCRC和GPT32EH0.GTCCRE寄存器中使用的传输控制信息之后。

(5) DTC向量表

在DTC向量表中，设置传输控制信息的地址，用于传输到GPT32EH0.GTCCRC和GPT32EH0.GTCCRE寄存器启动。

(6) ICU设置和DTC模块激活

1. 设置与GPT32EH0计数器溢出中断相关的ICU.IELSRn.DTCE位。
2. 将ICU.IELSRn.IELS[8:0]设置为182(B6h)以应对GPT32EH0计数器溢出。
3. 将DTCST.DTCST位设置为1。

(7) GPT settings

1. 设置GPT32EH0.GTIOR寄存器，使GTCCRA和GTCCRB寄存器作为输出比较寄存器运行。
2. 在GPT32EH0.GTCCRA和GPT32EH0.GTCCRB寄存器中设置默认PWM定时器比较值，在GPT32EH0.GTCCRC和GPT32EH0.GTCCRE寄存器中设置下一个PWM定时器比较值。
3. 在GPT32EH0.GTPR寄存器中设置默认PWM定时器周期值，在GPT32EH0.GTPBR寄存器中设置下一个PWM定时器周期值。
4. 将PmnPFS.PDR中的输出位设置为1，并将PmnPFS.PSEL[4:0]中的外设选择位设置为00011b。

(8) GPT activation

将GPT32EH0.GTSTR.CSTRT位设置为1以启动GPT32EH0.GTCNT计数器。

(9) DTC transfer

每次使用GPT32EH0.GTPR寄存器产生GPT32EH0计数器溢出时，下一个PWM定时器比较值被传送到GPT32EH0.GTCCRC和GPT32EH0.GTCCRE寄存器。下一个PWM定时器周期的设置被传送到GPT32EH0.GTPBR寄存器。

(10)中断处理

在指定轮次的数据传输完成后，例如当GPT传输的CRA寄存器中的值变为0时，会向CPU发出GPT计数器溢出中断请求。在处理例程中完成该中断的处理。

18.6.3 Chain Transfer When Counter = 0

The second data transfer is performed only when the transfer counter is set to 0 in the first data transfer, and the first data transfer information is repeatedly changed in the second transfer. Chain transfer enables transfers to be repeated 256 times or more.

The following procedure shows an example of configuring a 128-KB input buffer, where the input buffer is set so that its lower address starts with 0000h. Figure 18.14 shows a chain transfer when the counter = 0.

1. Set the normal transfer mode to input data for the first data transfer. Set the following:
   a. Transfer source address = fixed.
   b. CRA register = 0000h (65,536) times.
   c. MRB.CHNE bit = 1 (chain transfer is enabled).
   d. MRB.CHNS bit = 1 (chain transfer is performed only when the transfer counter is 0).
   e. MRB.DISEL bit = 0 (an interrupt request to the CPU is generated when the specified data transfer completes).
2. Prepare the upper 8-bit address of the start address at every 65,536 times of the transfer destination address for the first data transfer in different area such as the flash. For example, when setting the input buffer to 20 0000h to 21 FFFFh, prepare 21h and 20h.
3. For the second data transfer:
   a. Set the repeat transfer mode (with the source as the repeat area) to reset the transfer destination address of the first data transfer.
   b. Specify the upper 8 bits of the DAR register in the first transfer information area for the transfer destination.
   c. Set the MRB.CHNE bit = 0 (chain transfer is disabled).
   d. Set the MRB.DISEL bit = 0 (an interrupt request to the CPU is generated when the specified data transfer completes).
   e. When setting the input buffer to 20 0000h to 21 FFFFh, also set the transfer counter to 2.
4. The first data transfer is performed by an interrupt 65,536 times. When the transfer counter of the first data transfer becomes 0, the second data transfer starts. Set the upper 8 bits of the transfer destination address of the first data transfer to 21h. The lower 16 bits of the transfer destination address and the transfer counter of the first data transfer become 0000h.
5. In succession, the first data transfer is performed by an interrupt 65,536 times as specified for the first data transfer. When the transfer counter of the first data transfer becomes 0, the second data transfer starts. Set the upper 8 bits of the transfer destination address of the first data transfer to 20h. The lower 16 bits of the transfer destination address and the transfer counter of the first data transfer become 0000h.
6. Steps 4 and 5 are repeated indefinitely. Because the second data transfer is in repeat transfer mode, no interrupt request to the CPU is generated.

18.6.3 Counter=0时的链式转移

仅当在第一次数据传输中将传输计数器设置为0时才执行第二次数据传输，并且在第二次传输中重复改变第一数据传输信息。链式转移使转移可以重复256次或更多。

以下过程显示了配置128KB输入缓冲区的示例，其中输入缓冲区设置为使其低地址以0000h开头。图18.14显示了当计数器=0时的链式传输。

1. 将正常传输模式设置为第一次数据传输的输入数据。设置以下内容：
   一个。传输源地址=固定。
   湾。CRA寄存器=0000h(65 536)次。
   C。MRB.CHNE位=1（启用链式传输）。
   d。MRB.CHNS位=1（仅当传输计数器为0时才执行链式传输）。
   e.MRB.DISEL位=0（指定数据传输完成时向CPU产生中断请求）。
2. 在闪存等不同区域的第一次数据传输中，每65 536次传输目标地址准备起始地址的高8位地址。例如，将输入缓冲区设置为200000h到21FFFFh时，准备21h和20h。
3. 对于第二次数据传输：
   一个。设置重复传输模式（以源为重复区域）重置第一次数据传输的传输目标地址。
   湾。在传输目标的第一个传输信息区域中指定DAR寄存器的高8位。
   C。设置MRB.CHNE位=0（禁用链传输）。
   d。设置MRB.DISEL位=0（当指定的数据传输完成时向CPU产生一个中断请求）。
   e.将输入缓冲区设置为200000h至21FFFFh时，还要将传输计数器设置为2。
4. 第一次数据传输由中断执行65 536次。当第一次数据传输的传输计数器变为0时，第二次数据传输开始。将第一次数据传输的传输目标地址的高8位设置为21h。第一次数据传输的传输目标地址和传输计数器的低16位变为0000h。
5. 随后，第一次数据传输由中断执行65 536次，如为第一次数据传输指定的那样。当第一次数据传输的传输计数器变为0时，第二次数据传输开始。将第一次数据传输的传输目标地址的高8位设置为20h。第一次数据传输的传输目标地址和传输计数器的低16位变为0000h。
6. 步骤4和5无限重复。因为第二次数据传输是重复传输模式，所以不会产生对CPU的中断请求。

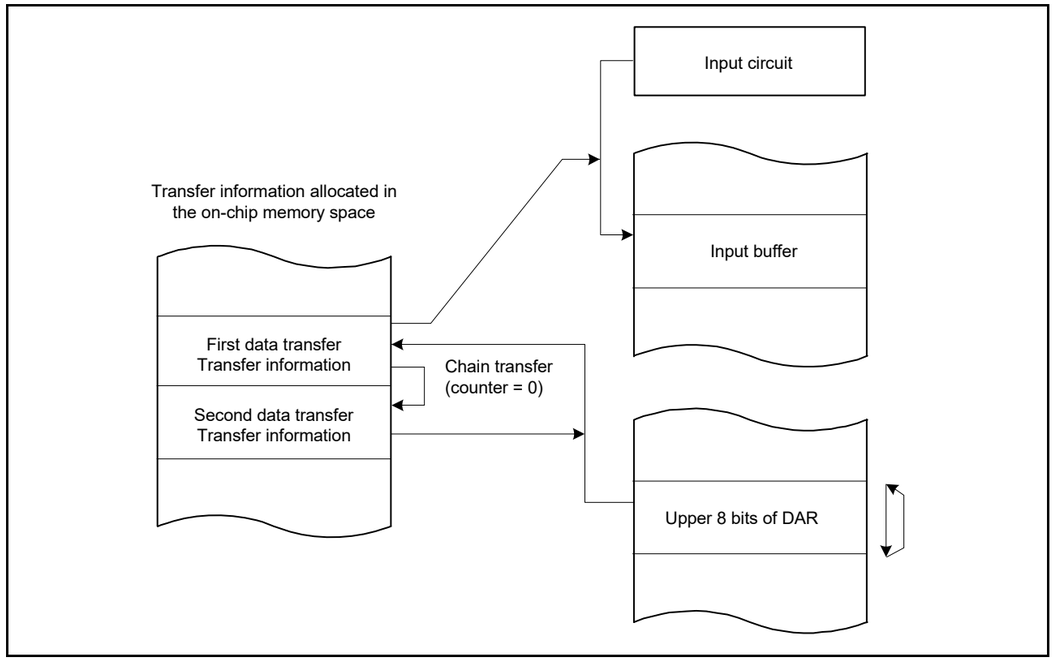


Figure 18.14 Chain transfer when counter = 0

18.7 Interrupt Sources

When the DTC finishes data transfer of the specified count or when data transfer with the MRB.DISEL bit set to 1 is complete, a DTC activation source generates an interrupt to the CPU. Interrupts to the CPU are controlled according to the settings in the NVIC and ICU.IELSRn.IELS[8:0]. See section 14, Interrupt Controller Unit (ICU).

The DTC prioritizes activation sources by granting the smaller interrupt vector numbers higher priority. The priority of interrupts to the CPU is determined by the NVIC priority.

18.8 Event Link

The DTC is capable of producing an event link request on completion of one transfer request. When the destination for the transfer is an external bus, the event link request is issued after completion of writing to the write buffer rather than after completion of writing to the actual transfer destination.

18.9 Snooze Control Interface

To return to Software Standby mode from Snooze mode through the DTC, set SYSTEM.SNZEDCR.DTCZRED or SYSTEM.SNZEDCR.DTCNZRED to 1. See section 11.8.3, Return to Software Standby Mode.

SYSTEM.SNZEDCR.DTCZRED enables or disables a Snooze end request on completion of the last DTC transmission, detected on DTC transmission completion when CRA and CRB are 0.

SYSTEM.SNZEDCR.DTCNZRED enables or disables a Snooze end request on a not last DTC transmission completion, detected on DTC transmission completion when CRA and CRB are not 0.

18.10 Module-Stop Function

Before transitioning to the module-stop function, Software Standby mode without a Snooze mode transition, or Deep Software Standby mode, set the DTCST.DTCST bit to 0, then perform the operations described in the following sections. The DTC is available in Snooze mode by setting LPW.SNZCR.SNZDTCEN to 1. See section 11, Low Power Modes.

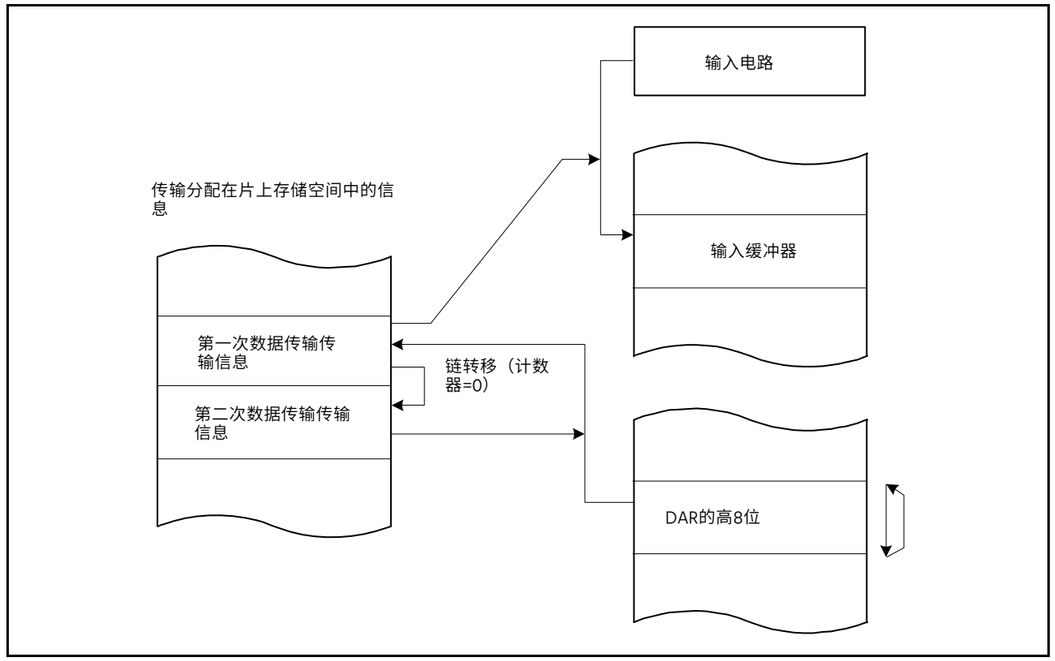


Figure 18.14 counter=0时的链转移

18.7 中断源

当DTC完成指定计数的数据传输或MRB.DISEL位设置为1的数据传输完成时，DTC激活源向CPU产生中断。根据NVIC和ICU.IELSRn.IELS[8:0]中的设置控制对CPU的中断。参见第14节，中断控制器单元(ICU)。

DTC通过授予较小的中断向量编号较高的优先级来确定激活源的优先级。CPU中断的优先级由NVIC优先级决定。

18.8 活动链接

DTC能够在完成一个传输请求时生成事件链接请求。当传输目的地是外部总线时，事件链接请求是在写入缓冲区写入完成后发出，而不是在实际传输目标写入完成后发出。

18.9 贪睡控制界面

要通过DTC从贪睡模式返回到软件待机模式，请设置SYSTEM.SNZEDCR.DTCZRED或SYSTEM.SNZEDCR.DTCNZRED为1。请参见第11.8.3节，返回软件待机模式。

SYSTEM.SNZEDCR.DTCZRED在最后一次DTC传输完成时启用或禁用贪睡结束请求，当CRA和CRB为0时在DTC传输完成时检测到。

SYSTEM.SNZEDCR.DTCNZRED在非最后一个DTC传输完成时启用或禁用贪睡结束请求，当CRA和CRB不为0时在DTC传输完成时检测到。

18.10 Module-Stop Function

在转换到模块停止功能、没有贪睡模式转换的软件待机模式或深度软件待机模式之前，将DTCST.DTCST位设置为0，然后执行以下部分中描述的操作。

通过将LPW.SNZCR.SNZDTCEN设置为1，可以在贪睡模式下使用DTC。请参阅第11节，低功耗模式。

(1) Module-stop function

Writing 1 to the MSTPCRA.MSTPA22 bit enables the module-stop function of the DTC. If the DTC transfer is in progress at the time 1 is written to the MSTPCRA.MSTPA22 bit, the transition to the module-stop state proceeds after DTC transfer ends. When the MSTPCRA.MSTPA22 bit is 1, accessing the DTC registers is prohibited.

Writing 0 to the MSTPCRA.MSTPA22 bit releases the DTC from the module-stop state.

(2) Software Standby and Deep Software Standby modes

Use the settings described in section 11.7.1, Transition to Software Standby Mode, or section 11.9.1, Transition to Deep Software Standby Mode.

If DTC transfer operations are in progress when the WFI instruction is executed, the transition to Software Standby mode or Deep Software Standby mode follows the completion of the DTC transfer.

When the Snooze control circuit receives a Snooze request in Software Standby mode, the MCU transfers to Snooze mode. See section 11.8.1, Transition to Snooze Mode. DTC operation in Snooze mode can be selected in the SYSTEM.SNZCR.SNZDTCEN bit. If DTC operation is enabled in Snooze mode, transitioning to Software Standby mode, set the DTCST.DTCST bit to 1. To return to Software Standby mode through the DTC, set SYSTEM.SNZEDCR.DTCZRED or SYSTEM.SNZEDCR.DTCNZRED to 1. See section 11.8.3, Return to Software Standby Mode. The DTC activation request from the ICU is stopped during Software Standby mode but not during Snooze mode.

(3) Notes on the module-stop function

For the WFI instruction and the register setting procedure, see section 11, Low Power Modes.

To perform a DTC transfer after returning from a low power mode without Snooze mode transition, set the DTCST.DTCST bit to 1 again.

To use a request that is generated in Software Standby mode as an interrupt request to the CPU but not as a DTC activation request, specify the CPU as the interrupt request destination as described in section 14.4.2, Selecting Interrupt Request Destinations, then execute a WFI instruction. If DTC operation is enabled in Snooze mode, do not use the module-stop function of the DTC.

18.11 Usage Notes

18.11.1 Transfer information Start Address

You must set multiples of 4 for the transfer information start addresses in the vector table. Otherwise, such addresses are accessed with their lowest 2 bits regarded as 00b.

(1) Module-stop function

向MSTPCRA.MSTPA22位写入1可启用DTC的模块停止功能。如果在向MSTPCRA.MSTPA22位写入1时正在进行DTC传输，则在DTC传输结束后继续向模块停止状态的转换。当MSTPCRA.MSTPA22位为1时，禁止访问DTC寄存器。

将0写入MSTPCRA.MSTPA22位可将DTC从模块停止状态释放。

(2) 软件待机和深度软件待机模式

使用第11.7.1节，过渡到软件待机模式或第11.9.1节，过渡到深度中描述的设置软件待机模式。

如果在执行WFI指令时DTC传输操作正在进行，则在DTC传输完成后转换到软件待机模式或深度软件待机模式。

当贪睡控制电路在软件待机模式下接收到贪睡请求时，MCU转入贪睡模式。请参阅第11.8.1节，过渡到贪睡模式。可以在SYSTEM.SNZCR.SNZDTCEN位中选择贪睡模式下的DTC操作。如果在贪睡模式下启用DTC操作，转换到软件待机模式，请将DTCST.DTCST位设置为1。要通过DTC返回到软件待机模式，请将SYSTEM.SNZEDCR.DTCZRED或SYSTEM.SNZEDCR.DTCNZRED设置为1。请参阅第11.8.3节，返回软件待机模式。来自ICU的DTC激活请求在软件待机模式期间停止，但在贪睡模式。

(3) 关于模块停止功能的注意事项

关于WFI指令和寄存器设置过程，请参见第11节，低功耗模式。

要在从低功耗模式返回后执行DTC传输而没有贪睡模式转换，请设置DTCST.DTCST位再次为1。

要将在软件待机模式下生成的请求用作对CPU的中断请求但不用作DTC激活请求，请按照第14.4.2节“选择中断请求目标”中的说明将CPU指定为中断请求目标，然后执行WFI指令。如果在贪睡模式下启用DTC操作，请勿使用DTC的模块停止功能。

18.11 使用说明

18.11.1 传输信息起始地址

您必须为向量表中的传输信息起始地址设置4的倍数。否则，这些地址的最低2位被视为00b。

19. Event Link Controller (ELC)

19.1 Overview

The Event Link Controller (ELC) uses the event requests generated by various peripheral modules as source signals to connect them to different modules, allowing direct link between modules without CPU intervention.

Table 19.1 lists the ELC specifications and Figure 19.1 shows a block diagram.

Table 19.1 ELC specifications

Parameter	Specifications
Event link function	270 types of event signals can be directly connected to modules.The ELC can generate an ELC event signal, and events that activate the DTC.
Module-stop function	Module-stop state can be set to reduce power consumption

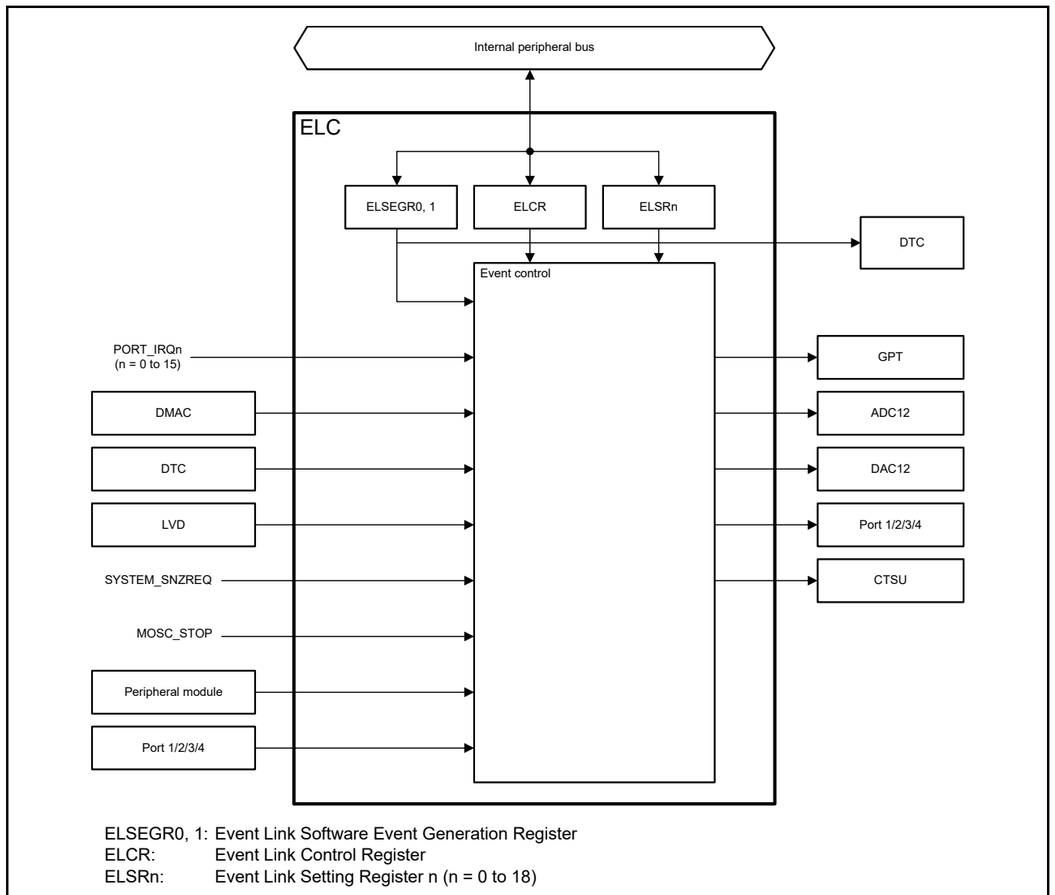


Figure 19.1 ELC block diagram

19. 事件链接控制器(ELC)

19.1 Overview

EventLinkController(ELC)使用各种外围模块产生的事件请求作为源信号，将它们连接到不同的模块，允许模块之间直接链接，无需CPU干预。

表19.1列出了ELC规范，图19.1显示了框图。

Table 19.1 ELC specifications

Parameter	Specifications
事件链接功能	270种事件信号可以直接连接到模块。ELC可以产生ELC事件信号，以及激活DTC的事件。
Module-stop function	可设置模块停止状态以降低功耗

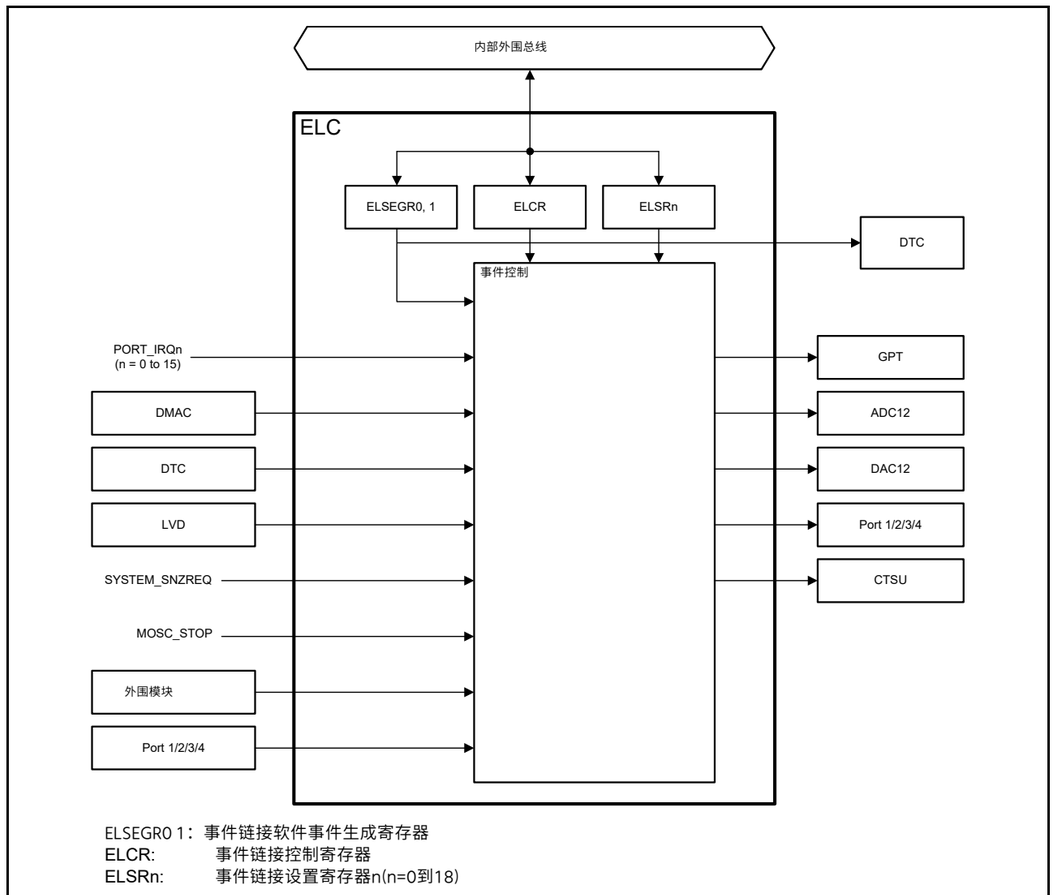


Figure 19.1 ELC框图

19.2 Register Descriptions

19.2.1 Event Link Controller Register (ELCR)

Address(es): ELC.ELCR 4004 1000h

	b7	b6	b5	b4	b3	b2	b1	b0
	ELCON	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b6 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	ELCON	All Event Link Enable	0: ELC function disabled 1: ELC function enabled.	R/W

The ELCR register controls the ELC operation.

19.2.2 Event Link Software Event Generation Register n (ELSEGRn) (n = 0, 1)

Address(es): ELC.ELSEGR0 4004 1002h, ELC.ELSEGR1 4004 1004h

	b7	b6	b5	b4	b3	b2	b1	b0
	WI	WE	—	—	—	—	—	SEG
Value after reset:	1	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	SEG	Software Event Generation	0: Normal operation 1: Software event is generated.	W
b5 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6	WE	SEG Bit Write Enable	0: Writes to SEG bit disabled 1: Writes to SEG bit enabled.	R/W
b7	WI	ELSEGR Register Write Disable	0: Writes to ELSEGR register enabled 1: Writes to ELSEGR register disabled.	W

SEG bit (Software Event Generation)

When 1 is written to the SEG bit while the WE bit is 1, a software event is generated. This bit is read as 0. Even when 1 is written to this bit, data is not stored. The WE bit must be set to 1 before writing to this bit.

A software event can trigger a linked DTC event.

WE bit (SEG Bit Write Enable)

The SEG bit can only be written to when the WE bit is 1. Clear the WI bit to 0 before writing to this bit.

[Setting condition]

- If 1 is written to this bit while the WI bit is 0, this bit becomes 1.

[Clearing condition]

- If 0 is written to this bit while the WI bit is 0, this bit becomes 0.

WI bit (ELSEGR Register Write Disable)

The ELSEGR register can only be written to when the write value to the WI bit is 0. This bit is read as 1. Before setting the WE or SEG bit, the WI bit must be set to 0.

19.2 注册说明

19.2.1 事件链接控制器寄存器(ELCR)

Address(es): ELC.ELCR 4004 1000h

	b7	b6	b5	b4	b3	b2	b1	b0
	ELCON	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b6 to b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b7	ELCON	所有事件链接启用	0：ELC功能禁用1：ELC 功能启用。	R/W

ELCR寄存器控制ELC操作。

19.2.2 事件链接软件事件生成寄存器n(ELSEGRn)(n=0 1)

Address(es): ELC.ELSEGR0 4004 1002h, ELC.ELSEGR1 4004 1004h

	b7	b6	b5	b4	b3	b2	b1	b0
	WI	WE	—	—	—	—	—	SEG
重置后的值：	1	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	SEG	软件事件生成	0：正常操作1：产生软件事件 。	W
b5 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b6	WE	SEG位写使能	0：禁止写入SEG位1：允许 写入SEG位。	R/W
b7	WI	ELSEGR寄存器写入禁用	0：允许写入ELSEGR寄存器1：禁止写 入ELSEGR寄存器。	W

SEG位（软件事件生成）

当WE位为1时向SEG位写入1时，将产生软件事件。该位被读取为0。即使向该位写入1，也不存储数据。在写入该位之前，WE位必须设置为1。

软件事件可以触发链接的DTC事件。

WE位（SEG位写使能）

SEG位只能在WE位为1时写入。在写入该位之前将WI位清零。

[Setting condition]

- 如果在WI位为0时向该位写入1，则该位变为1。

[Clearing condition]

- 如果在WI位为0时向该位写入0，则该位变为0。

WI位（ELSEGR寄存器写禁止）

只有当WI位的写入值为0时，才能写入ELSEGR寄存器。该位读为1。在设置WE或SEG位之前，必须将WI位设置为0。

19.2.3 Event Link Setting Register n (ELSRn) (n = 0 to 18)

Address(es): ELC.ELSR0 4004 1010h, ELC.ELSR1 4004 1014h, ELC.ELSR2 4004 1018h, ELC.ELSR3 4004 101Ch, ELC.ELSR4 4004 1020h, ELC.ELSR5 4004 1024h, ELC.ELSR6 4004 1028h, ELC.ELSR7 4004 102Ch, ELC.ELSR8 4004 1030h, ELC.ELSR9 4004 1034h, ELC.ELSR10 4004 1038h, ELC.ELSR11 4004 103Ch, ELC.ELSR12 4004 1040h, ELC.ELSR13 4004 1044h, ELC.ELSR14 4004 1048h, ELC.ELSR15 4004 104Ch, ELC.ELSR16 4004 1050h, ELC.ELSR17 4004 1054h, ELC.ELSR18 4004 1058h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	ELS[8:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b8 to b0	ELS[8:0]	Event Link Select	b8 b0 000000000: Event output disabled for the associated peripheral module 000000001 to 111000101b: Number setting for the event signal to be linked. Other settings are prohibited.	R/W
b15 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The ELSRn register specifies an event signal to be linked to for each peripheral module. Table 19.2 shows the association between the ELSRn registers and the peripheral modules. Table 19.3 shows the association between the event signal names set in the ELSRn register and the signal numbers.

Table 19.2 Association between the ELSRn registers and peripheral functions

Register name	Peripheral function (module)	Event name
ELSR0	GPT (A)	ELC_GPTA
ELSR1	GPT (B)	ELC_GPTB
ELSR2	GPT (C)	ELC_GPTC
ELSR3	GPT (D)	ELC_GPTD
ELSR4	GPT (E)	ELC_GPTE
ELSR5	GPT (F)	ELC_GPTF
ELSR6	GPT (G)	ELC_GPTG
ELSR7	GPT (H)	ELC_GPTH
ELSR8	ADC12A0	ELC_AD00
ELSR9	ADC12B0	ELC_AD01
ELSR10	ADC12A1	ELC_AD10
ELSR11	ADC12B1	ELC_AD11
ELSR12	DAC12 channel 0	ELC_DA0
ELSR13	DAC12 channel 1	ELC_DA1
ELSR14	PORT 1	ELC_PORT1
ELSR15	PORT 2	ELC_PORT2
ELSR16	PORT 3	ELC_PORT3
ELSR17	PORT 4	ELC_PORT4
ELSR18	CTSU	ELC_CTSU

19.2.3 事件链接设置寄存器n(ELSRn)(n=0到18)

Address(es): ELC.ELSR0 4004 1010h, ELC.ELSR1 4004 1014h, ELC.ELSR2 4004 1018h, ELC.ELSR3 4004 101Ch, ELC.ELSR4 4004 1020h, ELC.ELSR5 4004 1024h, ELC.ELSR6 4004 1028h, ELC.ELSR7 4004 102Ch, ELC.ELSR8 4004 1030h, ELC.ELSR9 4004 1034h, ELC.ELSR10 4004 1038h, ELC.ELSR11 4004 103Ch, ELC.ELSR12 4004 1040h, ELC.ELSR13 4004 1044h, ELC.ELSR14 4004 1048h, ELC.ELSR15 4004 104Ch, ELC.ELSR16 4004 1050h, ELC.ELSR17 4004 1054h, ELC.ELSR18 4004 1058h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	ELS[8:0]								
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b8 to b0	ELS[8:0]	活动链接选择	b8b0000000000：相关外围模块的事件输出禁用000000001至111000101b：要链接的事件信号的编号设置。禁止其他设置。	R/W
b15 to b9	—	Reserved	这些位被读取为0。写入值应为0。	R/W

ELSRn寄存器为每个外围模块指定一个要链接到的事件信号。表19.2显示了ELSRn寄存器和外设模块之间的关联。表19.3显示了在ELSRn寄存器中设置的事件信号名称和信号编号之间的关联。

Table 19.2 ELSRn寄存器和外设功能之间的关联

注册名称	外设功能（模块）	活动名称
ELSR0	GPT (A)	ELC_GPTA
ELSR1	GPT (B)	ELC_GPTB
ELSR2	GPT (C)	ELC_GPTC
ELSR3	GPT (D)	ELC_GPTD
ELSR4	GPT (E)	ELC_GPTE
ELSR5	GPT (F)	ELC_GPTF
ELSR6	GPT (G)	ELC_GPTG
ELSR7	GPT (H)	ELC_GPTH
ELSR8	ADC12A0	ELC_AD00
ELSR9	ADC12B0	ELC_AD01
ELSR10	ADC12A1	ELC_AD10
ELSR11	ADC12B1	ELC_AD11
ELSR12	DAC12 channel 0	ELC_DA0
ELSR13	DAC12 channel 1	ELC_DA1
ELSR14	PORT 1	ELC_PORT1
ELSR15	PORT 2	ELC_PORT2
ELSR16	PORT 3	ELC_PORT3
ELSR17	PORT 4	ELC_PORT4
ELSR18	CTSU	ELC_CTSU

Table 19.3 Association between event signal names set in ELSRn.ELS bits and signal numbers (1 of 7)

Event number	Interrupt request source	Name	Description
001h	Port	PORT_IRQ0*1	External pin interrupt 0
002h		PORT_IRQ1*1	External pin interrupt 1
003h		PORT_IRQ2*1	External pin interrupt 2
004h		PORT_IRQ3*1	External pin interrupt 3
005h		PORT_IRQ4*1	External pin interrupt 4
006h		PORT_IRQ5*1	External pin interrupt 5
007h		PORT_IRQ6*1	External pin interrupt 6
008h		PORT_IRQ7*1	External pin interrupt 7
009h		PORT_IRQ8*1	External pin interrupt 8
00Ah		PORT_IRQ9*1	External pin interrupt 9
00Bh		PORT_IRQ10*1	External pin interrupt 10
00Ch		PORT_IRQ11*1	External pin interrupt 11
00Dh		PORT_IRQ12*1	External pin interrupt 12
00Eh		PORT_IRQ13*1	External pin interrupt 13
00Fh		PORT_IRQ14*1	External pin interrupt 14
010h		PORT_IRQ15*1	External pin interrupt 15
020h	DMAC0	DMAC0_INT	DMAC transfer end 0
021h	DMAC1	DMAC1_INT	DMAC transfer end 1
022h	DMAC2	DMAC2_INT	DMAC transfer end 2
023h	DMAC3	DMAC3_INT	DMAC transfer end 3
024h	DMAC4	DMAC4_INT	DMAC transfer end 4
025h	DMAC5	DMAC5_INT	DMAC transfer end 5
026h	DMAC6	DMAC6_INT	DMAC transfer end 6
027h	DMAC7	DMAC7_INT	DMAC transfer end 7
02Ah	DTC	DTC_DTCEND*3	DTC transfer end
038h	LVD	LVD_LVD1	Voltage monitor 1 interrupt
039h		LVD_LVD2	Voltage monitor 2 interrupt
03Bh	MOSC	MOSC_STOP	Main clock oscillation stop
03Ch	Low-power mode	SYSTEM_SNZREQ*2, *3	Snooze entry
040h	AGT0	AGT0_AGTI	AGT interrupt
041h		AGT0_AGTCMAI	Compare match A
042h		AGT0_AGTCMBI	Compare match B
043h	AGT1	AGT1_AGTI	AGT interrupt
044h		AGT1_AGTCMAI	Compare match A
045h		AGT1_AGTCMBI	Compare match B
046h	IWDT	IWDT_NMIUNDF	IWDT underflow
047h	WDT	WDT_NMIUNDF	WDT underflow
049h	RTC	RTC_PRD	Periodic interrupt
04Bh	ADC120	ADC120_ADI	A/D scan end interrupt
04Fh		ADC120_WCMPM*3	Compare match
050h		ADC120_WCMPUM*3	Compare mismatch
051h	ADC121	ADC121_ADI	A/D scan end interrupt
055h		ADC121_WCMPM*3	Compare match
056h		ADC121_WCMPUM*3	Compare mismatch

Table 19.3 在ELSRn.ELS位中设置的事件信号名称与信号编号之间的关联（7个中的1个）

事件编号	中断请求源	Name	Description
001h	Port	PORT_IRQ0*1	外部引脚中断0
002h		PORT_IRQ1*1	外部引脚中断1
003h		PORT_IRQ2*1	外部引脚中断2
004h		PORT_IRQ3*1	外部引脚中断3
005h		PORT_IRQ4*1	外部引脚中断4
006h		PORT_IRQ5*1	外部引脚中断5
007h		PORT_IRQ6*1	外部引脚中断6
008h		PORT_IRQ7*1	外部引脚中断7
009h		PORT_IRQ8*1	外部引脚中断8
00Ah		PORT_IRQ9*1	外部引脚中断9
00Bh		PORT_IRQ10*1	外部引脚中断10
00Ch		PORT_IRQ11*1	外部引脚中断11
00Dh		PORT_IRQ12*1	外部引脚中断12
00Eh		PORT_IRQ13*1	外部引脚中断13
00Fh		PORT_IRQ14*1	外部引脚中断14
010h		PORT_IRQ15*1	外部引脚中断15
020h	DMAC0	DMAC0_INT	DMAC传输结束0
021h	DMAC1	DMAC1_INT	DMAC传输结束1
022h	DMAC2	DMAC2_INT	DMAC传输结束2
023h	DMAC3	DMAC3_INT	DMAC传输结束3
024h	DMAC4	DMAC4_INT	DMAC传输结束4
025h	DMAC5	DMAC5_INT	DMAC传输结束5
026h	DMAC6	DMAC6_INT	DMAC传输结束6
027h	DMAC7	DMAC7_INT	DMAC传输结束7
02Ah	DTC	DTC_DTCEND*3	DTC传输结束
038h	LVD	LVD_LVD1	电压监视器1中断
039h		LVD_LVD2	电压监视器2中断
03Bh	MOSC	MOSC_STOP	主时钟振荡停止
03Ch	Low-power mode	SYSTEM_SNZREQ*2, *3	贪睡进入
040h	AGT0	AGT0_AGTI	AGT interrupt
041h		AGT0_AGTCMAI	比较匹配A
042h		AGT0_AGTCMBI	比较匹配B
043h	AGT1	AGT1_AGTI	AGT interrupt
044h		AGT1_AGTCMAI	比较匹配A
045h		AGT1_AGTCMBI	比较匹配B
046h	IWDT	IWDT_NMIUNDF	IWDT underflow
047h	WDT	WDT_NMIUNDF	WDT underflow
049h	RTC	RTC_PRD	周期性中断
04Bh	ADC120	ADC120_ADI	AD扫描结束中断
04Fh		ADC120_WCMPM*3	比较匹配
050h		ADC120_WCMPUM*3	比较不匹配
051h	ADC121	ADC121_ADI	AD扫描结束中断
055h		ADC121_WCMPM*3	比较匹配
056h		ADC121_WCMPUM*3	比较不匹配

Table 19.3 Association between event signal names set in ELSRn.ELS bits and signal numbers (2 of 7)

Event number	Interrupt request source	Name	Description
057h	ACMPHS	ACMP_HS0*1	High-Speed Analog Comparator interrupt 0
058h		ACMP_HS1*1	High-Speed Analog Comparator interrupt 1
059h		ACMP_HS2*1	High-Speed Analog Comparator interrupt 2
05Ah		ACMP_HS3*1	High-Speed Analog Comparator interrupt 3
05Bh		ACMP_HS4*1	High-Speed Analog Comparator interrupt 4
05Ch		ACMP_HS5*1	High-Speed Analog Comparator interrupt 5
063h	IIC0	IIC0_RXI	Receive data full
064h		IIC0_TXI	Transmit data empty
065h		IIC0_TEI	Transmit end
066h		IIC0_EEI	Transfer error
068h	IIC1	IIC1_RXI	Receive data full
069h		IIC1_TXI	Transmit data empty
06Ah		IIC1_TEI	Transmit end
06Bh		IIC1_EEI	Transfer error
06Dh	IIC2	IIC2_RXI	Receive data full
06Eh		IIC2_TXI	Transmit data empty
06Fh		IIC2_TEI	Transmit end
070h		IIC2_EEI	Transfer error
086h	DOC	DOC_DOPCI*3	Data Operation Circuit interrupt
094h	I/O port	IOPORT_GROUP1	Port 1 event
095h		IOPORT_GROUP2	Port 2 event
096h		IOPORT_GROUP3	Port 3 event
097h		IOPORT_GROUP4	Port 4 event
098h	ELC	ELC_SWEVT0	Software event 0
099h		ELC_SWEVT1	Software event 1
0B0h	GPT32EH0	GPT0_CCMPA	Compare match A
0B1h		GPT0_CCMPB	Compare match B
0B2h		GPT0_CMPC	Compare match C
0B3h		GPT0_CMPD	Compare match D
0B4h		GPT0_CMPE	Compare match E
0B5h		GPT0_CMPF	Compare match F
0B6h		GPT0_OVF	Overflow
0B7h		GPT0_UDF	Underflow
0B8h		GPT0_ADTRGA	A/D converter start request A
0B9h		GPT0_ADTRGB	A/D converter start request B
0BAh	GPT32EH1	GPT1_CCMPA	Compare match A
0BBh		GPT1_CCMPB	Compare match B
0BCh		GPT1_CMPC	Compare match C
0BDh		GPT1_CMPD	Compare match D
0BEh		GPT1_CMPE	Compare match E
0BFh		GPT1_CMPF	Compare match F
0C0h		GPT1_OVF	Overflow
0C1h		GPT1_UDF	Underflow
0C2h		GPT1_ADTRGA	A/D converter start request A
0C3h		GPT1_ADTRGB	A/D converter start request B

Table 19.3 在ELSRn.ELS位中设置的事件信号名称和信号编号之间的关联（7个中的2个）

事件编号	中断请求源	Name	Description
057h	ACMPHS	ACMP_HS0*1	高速模拟比较器中断0
058h		ACMP_HS1*1	高速模拟比较器中断1
059h		ACMP_HS2*1	高速模拟比较器中断2
05Ah		ACMP_HS3*1	高速模拟比较器中断3
05Bh		ACMP_HS4*1	高速模拟比较器中断4
05Ch		ACMP_HS5*1	高速模拟比较器中断5
063h	IIC0	IIC0_RXI	接收数据已满
064h		IIC0_TXI	传输数据为空
065h		IIC0_TEI	发射端
066h		IIC0_EEI	传输错误
068h	IIC1	IIC1_RXI	接收数据已满
069h		IIC1_TXI	传输数据为空
06Ah		IIC1_TEI	发射端
06Bh		IIC1_EEI	传输错误
06Dh	IIC2	IIC2_RXI	接收数据已满
06Eh		IIC2_TXI	传输数据为空
06Fh		IIC2_TEI	发射端
070h		IIC2_EEI	传输错误
086h	DOC	DOC_DOPCI*3	数据运算电路中断
094h	I/O port	IOPORT_GROUP1	端口1事件
095h		IOPORT_GROUP2	端口2事件
096h		IOPORT_GROUP3	端口3事件
097h		IOPORT_GROUP4	端口4事件
098h	ELC	ELC_SWEVT0	软件事件0
099h		ELC_SWEVT1	软件事件1
0B0h	GPT32EH0	GPT0_CCMPA	比较匹配A
0B1h		GPT0_CCMPB	比较匹配B
0B2h		GPT0_CMPC	比较匹配C
0B3h		GPT0_CMPD	比较匹配D
0B4h		GPT0_CMPE	比较匹配E
0B5h		GPT0_CMPF	比较匹配F
0B6h		GPT0_OVF	Overflow
0B7h		GPT0_UDF	Underflow
0B8h		GPT0_ADTRGA	AD转换器启动请求A
0B9h		GPT0_ADTRGB	AD转换器启动请求B
0BAh	GPT32EH1	GPT1_CCMPA	比较匹配A
0BBh		GPT1_CCMPB	比较匹配B
0BCh		GPT1_CMPC	比较匹配C
0BDh		GPT1_CMPD	比较匹配D
0BEh		GPT1_CMPE	比较匹配E
0BFh		GPT1_CMPF	比较匹配F
0C0h		GPT1_OVF	Overflow
0C1h		GPT1_UDF	Underflow
0C2h		GPT1_ADTRGA	AD转换器启动请求A
0C3h		GPT1_ADTRGB	AD转换器启动请求B

Table 19.3 Association between event signal names set in ELSRn.ELS bits and signal numbers (3 of 7)

Event number	Interrupt request source	Name	Description
0C4h	GPT32EH2	GPT2_CCMPA	Compare match A
0C5h		GPT2_CCMPB	Compare match B
0C6h		GPT2_CMPC	Compare match C
0C7h		GPT2_CMPD	Compare match D
0C8h		GPT2_CMPE	Compare match E
0C9h		GPT2_CMPF	Compare match F
0CAh		GPT2_OVF	Overflow
0CBh		GPT2_UDF	Underflow
0CCh		GPT2_ADTRGA	A/D converter start request A
0CDh		GPT2_ADTRGB	A/D converter start request B
0CEh	GPT32EH3	GPT3_CCMPA	Compare match A
0CFh		GPT3_CCMPB	Compare match B
0D0h		GPT3_CMPC	Compare match C
0D1h		GPT3_CMPD	Compare match D
0D2h		GPT3_CMPE	Compare match E
0D3h		GPT3_CMPF	Compare match F
0D4h		GPT3_OVF	Overflow
0D5h		GPT3_UDF	Underflow
0D6h		GPT3_ADTRGA	A/D converter start request A
0D7h		GPT3_ADTRGB	A/D converter start request B
0D8h	GPT32E4	GPT4_CCMPA	Compare match A
0D9h		GPT4_CCMPB	Compare match B
0DAh		GPT4_CMPC	Compare match C
0DBh		GPT4_CMPD	Compare match D
0DCh		GPT4_CMPE	Compare match E
0DDh		GPT4_CMPF	Compare match F
0DEh		GPT4_OVF	Overflow
0DFh		GPT4_UDF	Underflow
0E0h		GPT4_ADTRGA	A/D converter start request A
0E1h		GPT4_ADTRGB	A/D converter start request B
0E2h	GPT32E5	GPT5_CCMPA	Compare match A
0E3h		GPT5_CCMPB	Compare match B
0E4h		GPT5_CMPC	Compare match C
0E5h		GPT5_CMPD	Compare match D
0E6h		GPT5_CMPE	Compare match E
0E7h		GPT5_CMPF	Compare match F
0E8h		GPT5_OVF	Overflow
0E9h		GPT5_UDF	Underflow
0EAh		GPT5_ADTRGA	A/D converter start request A
0EBh		GPT5_ADTRGB	A/D converter start request B

Table 19.3 在ELSRn.ELS位中设置的事件信号名称和信号编号之间的关联（3of7）

事件编号	中断请求源	Name	Description
0C4h	GPT32EH2	GPT2_CCMPA	比较匹配A
0C5h		GPT2_CCMPB	比较匹配B
0C6h		GPT2_CMPC	比较匹配C
0C7h		GPT2_CMPD	比较匹配D
0C8h		GPT2_CMPE	比较匹配E
0C9h		GPT2_CMPF	比较匹配F
0CAh		GPT2_OVF	Overflow
0CBh		GPT2_UDF	Underflow
0CCh		GPT2_ADTRGA	AD转换器启动请求A
0CDh		GPT2_ADTRGB	AD转换器启动请求B
0CEh	GPT32EH3	GPT3_CCMPA	比较匹配A
0CFh		GPT3_CCMPB	比较匹配B
0D0h		GPT3_CMPC	比较匹配C
0D1h		GPT3_CMPD	比较匹配D
0D2h		GPT3_CMPE	比较匹配E
0D3h		GPT3_CMPF	比较匹配F
0D4h		GPT3_OVF	Overflow
0D5h		GPT3_UDF	Underflow
0D6h		GPT3_ADTRGA	AD转换器启动请求A
0D7h		GPT3_ADTRGB	AD转换器启动请求B
0D8h	GPT32E4	GPT4_CCMPA	比较匹配A
0D9h		GPT4_CCMPB	比较匹配B
0DAh		GPT4_CMPC	比较匹配C
0DBh		GPT4_CMPD	比较匹配D
0DCh		GPT4_CMPE	比较匹配E
0DDh		GPT4_CMPF	比较匹配F
0DEh		GPT4_OVF	Overflow
0DFh		GPT4_UDF	Underflow
0E0h		GPT4_ADTRGA	AD转换器启动请求A
0E1h		GPT4_ADTRGB	AD转换器启动请求B
0E2h	GPT32E5	GPT5_CCMPA	比较匹配A
0E3h		GPT5_CCMPB	比较匹配B
0E4h		GPT5_CMPC	比较匹配C
0E5h		GPT5_CMPD	比较匹配D
0E6h		GPT5_CMPE	比较匹配E
0E7h		GPT5_CMPF	比较匹配F
0E8h		GPT5_OVF	Overflow
0E9h		GPT5_UDF	Underflow
0EAh		GPT5_ADTRGA	AD转换器启动请求A
0EBh		GPT5_ADTRGB	AD转换器启动请求B

Table 19.3 Association between event signal names set in ELSRn.ELS bits and signal numbers (4 of 7)

Event number	Interrupt request source	Name	Description
0ECh	GPT32E6	GPT6_CCMPA	Compare match A
0EDh		GPT6_CCMPB	Compare match B
0EEh		GPT6_CMPC	Compare match C
0EFh		GPT6_CMPD	Compare match D
0F0h		GPT6_CMPE	Compare match E
0F1h		GPT6_CMPF	Compare match F
0F2h		GPT6_OVF	Overflow
0F3h		GPT6_UDF	Underflow
0F4h		GPT6_ADTRGA	A/D converter start request A
0F5h		GPT6_ADTRGB	A/D converter start request B
0F6h	GPT32E7	GPT7_CCMPA	Compare match A
0F7h		GPT7_CCMPB	Compare match B
0F8h		GPT7_CMPC	Compare match C
0F9h		GPT7_CMPD	Compare match D
0FAh		GPT7_CMPE	Compare match E
0FBh		GPT7_CMPF	Compare match F
0FCh		GPT7_OVF	Overflow
0FDh		GPT7_UDF	Underflow
0FEh		GPT7_ADTRGA	A/D converter start request A
0FFh		GPT7_ADTRGB	A/D converter start request B
100h	GPT328	GPT8_CCMPA	Compare match A
101h		GPT8_CCMPB	Compare match B
102h		GPT8_CMPC	Compare match C
103h		GPT8_CMPD	Compare match D
104h		GPT8_CMPE	Compare match E
105h		GPT8_CMPF	Compare match F
106h		GPT8_OVF	Overflow
107h		GPT8_UDF	Underflow
10Ah	GPT329	GPT9_CCMPA	Compare match A
10Bh		GPT9_CCMPB	Compare match B
10Ch		GPT9_CMPC	Compare match C
10Dh		GPT9_CMPD	Compare match D
10Eh		GPT9_CMPE	Compare match E
10Fh		GPT9_CMPF	Compare match F
110h		GPT9_OVF	Overflow
111h		GPT9_UDF	Underflow
114h	GPT3210	GPT10_CCMPA	Compare match A
115h		GPT10_CCMPB	Compare match B
116h		GPT10_CMPC	Compare match C
117h		GPT10_CMPD	Compare match D
118h		GPT10_CMPE	Compare match E
119h		GPT10_CMPF	Compare match F
11Ah		GPT10_OVF	Overflow
11Bh		GPT10_UDF	Underflow

Table 19.3 ELSRn.ELS位中设置的事件信号名称与信号编号之间的关联（4个，共7个）

事件编号	中断请求源	Name	Description
0ECh	GPT32E6	GPT6_CCMPA	比较匹配A
0EDh		GPT6_CCMPB	比较匹配B
0EEh		GPT6_CMPC	比较匹配C
0EFh		GPT6_CMPD	比较匹配D
0F0h		GPT6_CMPE	比较匹配E
0F1h		GPT6_CMPF	比较匹配F
0F2h		GPT6_OVF	Overflow
0F3h		GPT6_UDF	Underflow
0F4h		GPT6_ADTRGA	AD转换器启动请求A
0F5h		GPT6_ADTRGB	AD转换器启动请求B
0F6h	GPT32E7	GPT7_CCMPA	比较匹配A
0F7h		GPT7_CCMPB	比较匹配B
0F8h		GPT7_CMPC	比较匹配C
0F9h		GPT7_CMPD	比较匹配D
0FAh		GPT7_CMPE	比较匹配E
0FBh		GPT7_CMPF	比较匹配F
0FCh		GPT7_OVF	Overflow
0FDh		GPT7_UDF	Underflow
0FEh		GPT7_ADTRGA	AD转换器启动请求A
0FFh		GPT7_ADTRGB	AD转换器启动请求B
100h	GPT328	GPT8_CCMPA	比较匹配A
101h		GPT8_CCMPB	比较匹配B
102h		GPT8_CMPC	比较匹配C
103h		GPT8_CMPD	比较匹配D
104h		GPT8_CMPE	比较匹配E
105h		GPT8_CMPF	比较匹配F
106h		GPT8_OVF	Overflow
107h		GPT8_UDF	Underflow
10Ah	GPT329	GPT9_CCMPA	比较匹配A
10Bh		GPT9_CCMPB	比较匹配B
10Ch		GPT9_CMPC	比较匹配C
10Dh		GPT9_CMPD	比较匹配D
10Eh		GPT9_CMPE	比较匹配E
10Fh		GPT9_CMPF	比较匹配F
110h		GPT9_OVF	Overflow
111h		GPT9_UDF	Underflow
114h	GPT3210	GPT10_CCMPA	比较匹配A
115h		GPT10_CCMPB	比较匹配B
116h		GPT10_CMPC	比较匹配C
117h		GPT10_CMPD	比较匹配D
118h		GPT10_CMPE	比较匹配E
119h		GPT10_CMPF	比较匹配F
11Ah		GPT10_OVF	Overflow
11Bh		GPT10_UDF	Underflow

Table 19.3 Association between event signal names set in ELSRn.ELS bits and signal numbers (5 of 7)

Event number	Interrupt request source	Name	Description
11Eh	GPT3211	GPT11_CCMPA	Compare match A
11Fh		GPT11_CCMPB	Compare match B
120h		GPT11_CMPC	Compare match C
121h		GPT11_CMPD	Compare match D
122h		GPT11_CMPE	Compare match E
123h		GPT11_CMPF	Compare match F
124h		GPT11_OVF	Overflow
125h		GPT11_UDF	Underflow
128h	GPT3212	GPT12_CCMPA	Compare match A
129h		GPT12_CCMPB	Compare match B
12Ah		GPT12_CMPC	Compare match C
12Bh		GPT12_CMPD	Compare match D
12Ch		GPT12_CMPE	Compare match E
12Dh		GPT12_CMPF	Compare match F
12Eh		GPT12_OVF	Overflow
12Fh		GPT12_UDF	Underflow
132h	GPT3213	GPT13_CCMPA	Compare match A
133h		GPT13_CCMPB	Compare match B
134h		GPT13_CMPC	Compare match C
135h		GPT13_CMPD	Compare match D
136h		GPT13_CMPE	Compare match E
137h		GPT13_CMPF	Compare match F
138h		GPT13_OVF	Overflow
139h		GPT13_UDF	Underflow
150h	GPT	GPT_UVWEDGE	UVW edge event
165h	Ethernet Controller	ETHER_RISE0	Pulse output timer 0 rising edge detection
166h		ETHER_RISE1	Pulse output timer 1 rising edge detection
167h		ETHER_RISE2	Pulse output timer 2 rising edge detection
168h		ETHER_RISE3	Pulse output timer 3 rising edge detection
169h		ETHER_RISE4	Pulse output timer 4 rising edge detection
16Ah		ETHER_RISE5	Pulse output timer 5 rising edge detection
16Bh		ETHER_FALL0	Pulse output timer 0 falling edge detection
16Ch		ETHER_FALL1	Pulse output timer 1 falling edge detection
16Dh		ETHER_FALL2	Pulse output timer 2 falling edge detection
16Eh		ETHER_FALL3	Pulse output timer 3 falling edge detection
16Fh		ETHER_FALL4	Pulse output timer 4 falling edge detection
170h		ETHER_FALL5	Pulse output timer 5 falling edge detection
174h	SCI0	SCI0_RXI *4	Receive data full
175h		SCI0_TXI *4	Transmit data empty
176h		SCI0_TEI	Transmit end
177h		SCI0_ERI *4	Receive error
178h		SCI0_AM	Address match event

Table 19.3 ELSRn.ELS位中设置的事件信号名称与信号编号之间的关联（5个，共7个）

事件编号	中断请求源	Name	Description
11Eh	GPT3211	GPT11_CCMPA	比较匹配A
11Fh		GPT11_CCMPB	比较匹配B
120h		GPT11_CMPC	比较匹配C
121h		GPT11_CMPD	比较匹配D
122h		GPT11_CMPE	比较匹配E
123h		GPT11_CMPF	比较匹配F
124h		GPT11_OVF	Overflow
125h		GPT11_UDF	Underflow
128h	GPT3212	GPT12_CCMPA	比较匹配A
129h		GPT12_CCMPB	比较匹配B
12Ah		GPT12_CMPC	比较匹配C
12Bh		GPT12_CMPD	比较匹配D
12Ch		GPT12_CMPE	比较匹配E
12Dh		GPT12_CMPF	比较匹配F
12Eh		GPT12_OVF	Overflow
12Fh		GPT12_UDF	Underflow
132h	GPT3213	GPT13_CCMPA	比较匹配A
133h		GPT13_CCMPB	比较匹配B
134h		GPT13_CMPC	比较匹配C
135h		GPT13_CMPD	比较匹配D
136h		GPT13_CMPE	比较匹配E
137h		GPT13_CMPF	比较匹配F
138h		GPT13_OVF	Overflow
139h		GPT13_UDF	Underflow
150h	GPT	GPT_UVWEDGE	UVW边缘事件
165h	以太网控制器	ETHER_RISE0	脉冲输出定时器0上升沿检测
166h		ETHER_RISE1	脉冲输出定时器1上升沿检测
167h		ETHER_RISE2	脉冲输出定时器2上升沿检测
168h		ETHER_RISE3	脉冲输出定时器3上升沿检测
169h		ETHER_RISE4	脉冲输出定时器4上升沿检测
16Ah		ETHER_RISE5	脉冲输出定时器5上升沿检测
16Bh		ETHER_FALL0	脉冲输出定时器0下降沿检测
16Ch		ETHER_FALL1	脉冲输出定时器1下降沿检测
16Dh		ETHER_FALL2	脉冲输出定时器2下降沿检测
16Eh		ETHER_FALL3	脉冲输出定时器3下降沿检测
16Fh		ETHER_FALL4	脉冲输出定时器4下降沿检测
170h		ETHER_FALL5	脉冲输出定时器5下降沿检测
174h	SCI0	SCI0_RXI *4	接收数据已满
175h		SCI0_TXI *4	传输数据为空
176h		SCI0_TEI	发射端
177h		SCI0_ERI *4	接收错误
178h		SCI0_AM	地址匹配事件

Table 19.3 Association between event signal names set in ELSRn.ELS bits and signal numbers (6 of 7)

Event number	Interrupt request source	Name	Description
17Ah	SCI1	SCI1_RXI *4	Receive data full
17Bh		SCI1_TXI *4	Transmit data empty
17Ch		SCI1_TEI	Transmit end
17Dh		SCI1_ERI *4	Receive error
17Eh		SCI1_AM	Address match event
180h	SCI2	SCI2_RXI *4	Receive data full
181h		SCI2_TXI *4	Transmit data empty
182h		SCI2_TEI	Transmit end
183h		SCI2_ERI *4	Receive error
184h		SCI2_AM	Address match event
186h	SCI3	SCI3_RXI *4	Receive data full
187h		SCI3_TXI *4	Transmit data empty
188h		SCI3_TEI	Transmit end
189h		SCI3_ERI *4	Receive error
18Ah		SCI3_AM	Address match event
18Ch	SCI4	SCI4_RXI *4	Receive data full
18Dh		SCI4_TXI *4	Transmit data empty
18Eh		SCI4_TEI	Transmit end
18Fh		SCI4_ERI *4	Receive error
190h		SCI4_AM	Address match event
192h	SCI5	SCI5_RXI *4	Receive data full
193h		SCI5_TXI *4	Transmit data empty
194h		SCI5_TEI	Transmit end
195h		SCI5_ERI *4	Receive error
196h		SCI5_AM	Address match event
198h	SCI6	SCI6_RXI *4	Receive data full
199h		SCI6_TXI *4	Transmit data empty
19Ah		SCI6_TEI	Transmit end
19Bh		SCI6_ERI *4	Receive error
19Ch		SCI6_AM	Address match event
19Eh	SCI7	SCI7_RXI *4	Receive data full
19Fh		SCI7_TXI *4	Transmit data empty
1A0h		SCI7_TEI	Transmit end
1A1h		SCI7_ERI *4	Receive error
1A2h		SCI7_AM	Address match event
1A4h	SCI8	SCI8_RXI *4	Receive data full
1A5h		SCI8_TXI *4	Transmit data empty
1A6h		SCI8_TEI	Transmit end
1A7h		SCI8_ERI *4	Receive error
1A8h		SCI8_AM	Address match event
1AAh	SCI9	SCI9_RXI *4	Receive data full
1ABh		SCI9_TXI *4	Transmit data empty
1ACh		SCI9_TEI	Transmit end
1ADh		SCI9_ERI *4	Receive error
1AEh		SCI9_AM	Address match event

Table 19.3 在ELSRn.ELS位中设置的事件信号名称与信号编号之间的关联（6个，共7个）

事件编号	中断请求源	Name	Description
17Ah	SCI1	SCI1_RXI *4	接收数据已满
17Bh		SCI1_TXI *4	传输数据为空
17Ch		SCI1_TEI	发射端
17Dh		SCI1_ERI *4	接收错误
17Eh		SCI1_AM	地址匹配事件
180h	SCI2	SCI2_RXI *4	接收数据已满
181h		SCI2_TXI *4	传输数据为空
182h		SCI2_TEI	发射端
183h		SCI2_ERI *4	接收错误
184h		SCI2_AM	地址匹配事件
186h	SCI3	SCI3_RXI *4	接收数据已满
187h		SCI3_TXI *4	传输数据为空
188h		SCI3_TEI	发射端
189h		SCI3_ERI *4	接收错误
18Ah		SCI3_AM	地址匹配事件
18Ch	SCI4	SCI4_RXI *4	接收数据已满
18Dh		SCI4_TXI *4	传输数据为空
18Eh		SCI4_TEI	发射端
18Fh		SCI4_ERI *4	接收错误
190h		SCI4_AM	地址匹配事件
192h	SCI5	SCI5_RXI *4	接收数据已满
193h		SCI5_TXI *4	传输数据为空
194h		SCI5_TEI	发射端
195h		SCI5_ERI *4	接收错误
196h		SCI5_AM	地址匹配事件
198h	SCI6	SCI6_RXI *4	接收数据已满
199h		SCI6_TXI *4	传输数据为空
19Ah		SCI6_TEI	发射端
19Bh		SCI6_ERI *4	接收错误
19Ch		SCI6_AM	地址匹配事件
19Eh	SCI7	SCI7_RXI *4	接收数据已满
19Fh		SCI7_TXI *4	传输数据为空
1A0h		SCI7_TEI	发射端
1A1h		SCI7_ERI *4	接收错误
1A2h		SCI7_AM	地址匹配事件
1A4h	SCI8	SCI8_RXI *4	接收数据已满
1A5h		SCI8_TXI *4	传输数据为空
1A6h		SCI8_TEI	发射端
1A7h		SCI8_ERI *4	接收错误
1A8h		SCI8_AM	地址匹配事件
1AAh	SCI9	SCI9_RXI *4	接收数据已满
1ABh		SCI9_TXI *4	传输数据为空
1ACh		SCI9_TEI	发射端
1ADh		SCI9_ERI *4	接收错误
1AEh		SCI9_AM	地址匹配事件

Table 19.3 Association between event signal names set in ELSRn.ELS bits and signal numbers (7 of 7)

Event number	Interrupt request source	Name	Description
1BCh	SPI0	SPI0_SPRI	Receive data full
1BDh		SPI0_SPTI	Transmit data empty
1BEh		SPI0_SPII	Idle
1BFh		SPI0_SPEI	Receive error
1C0h		SPI0_SPTEND	Transmit end
1C1h	SPI1	SPI1_SPRI	Receive data full
1C2h		SPI1_SPTI	Transmit data empty
1C3h		SPI1_SPII	Idle
1C4h		SPI1_SPEI	Receive error
1C5h		SPI1_SPTEND	Transmit end

Note 1. Only pulse (edge detection) is supported.
Note 2. ELSR8 to ELSR11, ELSR14 to ELSR17, and ELSR18 can select this event.
Note 3. This event can occur in Snooze mode.
Note 4. This event is not supported in FIFO mode.

19.3 Operation

19.3.1 Relation between Interrupt Handling and Event Linking

Event number for an event link is the same as that for the associated interrupt source. For information on generating event signals, see the explanation in the chapter for each event source module.

19.3.2 Linking Events

When an event occurs and that event is already set as a trigger in the Event Link Setting Register (ELSRn), the associated module is activated. The operation of the module must be set up in advance. Table 19.4 lists the operations of modules when an event occurs.

Table 19.4 Module operations when event occurs

Module	Operations when event occurs
GPT	• Start counting • Stop counting • Clear counting • Up counting • Down counting • Input capture.
ADC12	Start A/D conversion
DAC12	Start D/A conversion
I/O ports	• Change pin output based on the EORR (reset) or EOSR (set) • Latch pin state to EIDR • The following ports can be used for the ELC: PORT 1 PORT 2 PORT 3 PORT 4.
CTSU	Start measurement operation
DTC	Start DTC data transfer

19.3.3 Example Procedure for Linking Events

To link events:

1. Set the operation of the module for which an event is to be linked.
2. Set the appropriate ELSRn register for the module to be linked.

Table 19.3 ELSRn.ELS位中设置的事件信号名称与信号编号之间的关联（7个中的7个）

事件编号	中断请求源	Name	Description
1BCh	SPI0	SPI0_SPRI	接收数据已满
1BDh		SPI0_SPTI	传输数据为空
1BEh		SPI0_SPII	Idle
1BFh		SPI0_SPEI	接收错误
1C0h		SPI0_SPTEND	发射端
1C1h	SPI1	SPI1_SPRI	接收数据已满
1C2h		SPI1_SPTI	传输数据为空
1C3h		SPI1_SPII	Idle
1C4h		SPI1_SPEI	接收错误
1C5h		SPI1_SPTEND	发射端

Note 1. 仅支持脉冲（边缘检测）。
Note 2. ELSR8到ELSR11、ELSR14到ELSR17和ELSR18可以选择此事件。
Note 3. 此事件可以在贪睡模式下发生。
Note 4. FIFO模式不支持此事件。

19.3 Operation

19.3.1 中断处理和事件链接的关系

事件链接的事件编号与关联中断源的事件编号相同。有关生成事件信号的信息，请参阅每个事件源模块的章节中的说明。

19.3.2 链接事件

当事件发生并且该事件已在事件链接设置寄存器(ELSRn)中设置为触发器时，将激活相关模块。模块的操作必须提前设置好。表19.4列出了事件发生时模块的操作。

Table 19.4 事件发生时的模块操作

Module	事件发生时的操作
GPT	开始计数 停止计数 清除计数 递增计数 递减计数 输入捕获。
ADC12	开始AD转换
DAC12	开始DA转换
I/O ports	根据EORR（复位）或EOSR（设置）更改引脚输出 将引脚状态锁定为EIDR 以下端口可用于ELC：PORT1PORT2PORT3PORT4。
CTSU	开始测量操作
DTC	开始DTC数据传输

19.3.3 链接事件的示例过程

链接事件：

1. 设置要链接事件的模块的操作。
2. 为要链接的模块设置适当的ELSRn寄存器。

3. Set the ELCR.ELCON bit to 1 to enable linkage of all events.
4. Configure the module from which an event is output and activate the module. The link between the two modules is now active.
5. To stop event linkage of modules individually, set 000000000b in the ELSRn.ELS[8:0] bits associated with the modules. To stop linkage of all events, set the ELCR.ELCON bit to 0.

If the event link output from the RTC is to be used, set the ELC after the RTC is set, for example, for initialization and time settings. Unintended events can be generated if the RTC settings are made after the ELC settings.

19.4 Usage Notes

19.4.1 Linking DMAC or DTC Transfer End Signals as Events

When linking the DMAC or DTC transfer end signals as events, do not set the same peripheral module as the DMAC or DTC transfer destination and event link destination. If set, the peripheral module might be started before DMAC or DTC transfer to the peripheral module is complete.

19.4.2 Setting Clocks

To link events, you must enable the ELC and the related modules. The modules cannot operate if the related modules are in the module-stop state or in low power modes in which the module is stopped (Software Standby mode or Deep Software Standby mode). Some modules can perform in Snooze mode. For more information, see Table 19.3 and section 11, Low Power Modes.

19.4.3 Settings for the Module-Stop Function

The Module Stop Control Register C (MSTPCRC) can enable or disable ELC operation. The ELC is initially stopped after reset. Releasing the module-stop state enables access to the registers. For more information, see Table 19.3 and section 11, Low Power Modes. The ELCON bit must be set to 0 before disabling ELC operation using the Module Stop Control Register.

19.4.4 ELC Delay Time

In Figure 19.2, module A uses ELC and accesses module B through the ELC. There is a delay time in the ELC module between module A and module B. See Table 19.5.

If the clock domains in both module A and module B are the same, the delay time is 0. But, if the clock domains in module A and B are different, ELC module has some delay. The time delay is defined by the slower clock frequency between module A and module B clocks.

Table 19.5 ELC delay time

Clock domain	Clock frequency	ELC delay time
clock_A = clock_B	clock_A = clock_B	0 cycle
clock_A ≠ clock_B	clock_A = clock_B	1 cycle to 2 cycles
	clock_A > clock_B	1 cycle to 2 cycles of B
	clock_A < clock_B	1 cycle to 2 cycles of A

3. 将ELCR.ELCON位设置为1以启用所有事件的链接。
4. 配置输出事件的模块并激活该模块。两个模块之间的链接现在处于活动状态。
5. 要单独停止模块的事件链接，请在与模块关联的ELSRn.ELS[8:0]位中设置000000000b。要停止所有事件的链接，请将ELCR.ELCON位设置为0。

如果要使用RTC的事件链接输出，请在设置RTC后设置ELC，例如用于初始化和时间设置。如果在ELC设置之后进行RTC设置，则可能会生成意外事件。

19.4 使用说明

19.4.1 将DMAC或DTC传输结束信号作为事件链接

将DMAC或DTC传输结束信号作为事件链接时，请勿将外设模块设置为DMAC或DTC传输目标和事件链接目标。如果设置，则外围模块可能会在DMAC或DTC传输到外围模块完成之前启动。

19.4.2 设置时钟

要链接事件，您必须启用ELC和相关模块。如果相关模块处于模块停止状态或模块停止的低功耗模式（软件待机模式或深度软件待机模式），则模块无法运行。某些模块可以在贪睡模式下执行。有关详细信息，请参阅表19.3和第11节，低功耗模式。

19.4.3 模块停止功能的设置

模块停止控制寄存器C(MSTPCRC)可以启用或禁用ELC操作。ELC在复位后最初停止。释放模块停止状态可以访问寄存器。有关详细信息，请参阅表19.3和第11节，低功耗模式。在使用模块停止控制寄存器禁用ELC操作之前，必须将ELCON位设置为0。

19.4.4 ELC延迟时间

在图19.2中，模块A使用ELC并通过ELC访问模块B。模块A和模块B之间的ELC模块有一个延迟时间。见表19.5。

如果模块A和模块B中的时钟域相同，则延迟时间为0。但是，如果模块A和B中的时钟域不同，ELC模块会有一些延迟。时间延迟由模块A和模块B时钟之间较慢的时钟频率定义。

Table 19.5 ELC延迟时间

时钟域	时钟频率	ELC延迟时间
clock_A = clock_B	clock_A = clock_B	0 cycle
clock_A ≠ clock_B	clock_A = clock_B	1个周期到2个周期
	clock_A > clock_B	B的1个周期到2个周期
	clock_A < clock_B	A的1个周期到2个周期

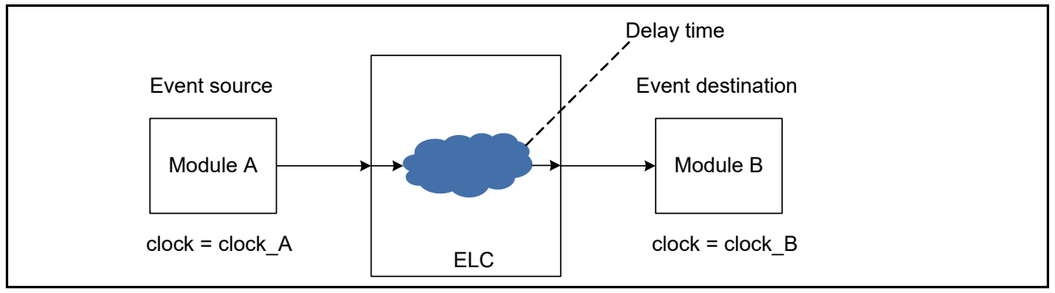


Figure 19.2 ELC delay time

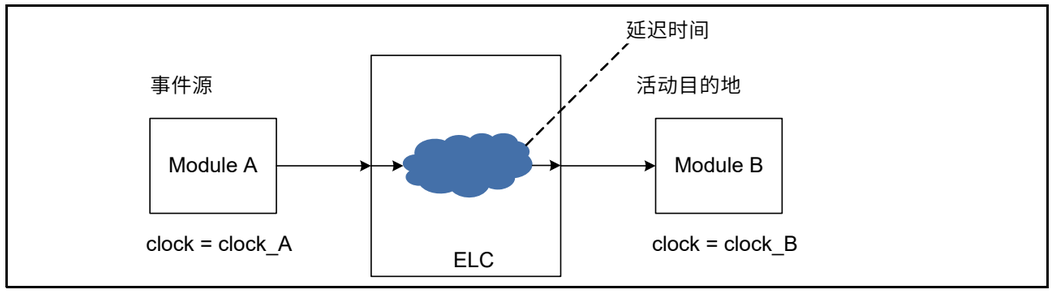


Figure 19.2 ELC延迟时间

20. I/O Ports

20.1 Overview

The I/O port pins operate as general I/O port pins, I/O pins for peripheral modules, interrupt input pins, analog I/O, port group function for the ELC, or bus control pins. All pins operate as input pins immediately after a reset, and pin functions are switched by register settings. You can specify the associated I/O ports and peripheral modules for each pin in the registers.

Figure 20.1 shows a connection diagram for the I/O port registers. The configuration of the I/O ports differs depending on the package. Table 20.1 lists the I/O port specifications by package, and Table 20.2 lists the port functions.

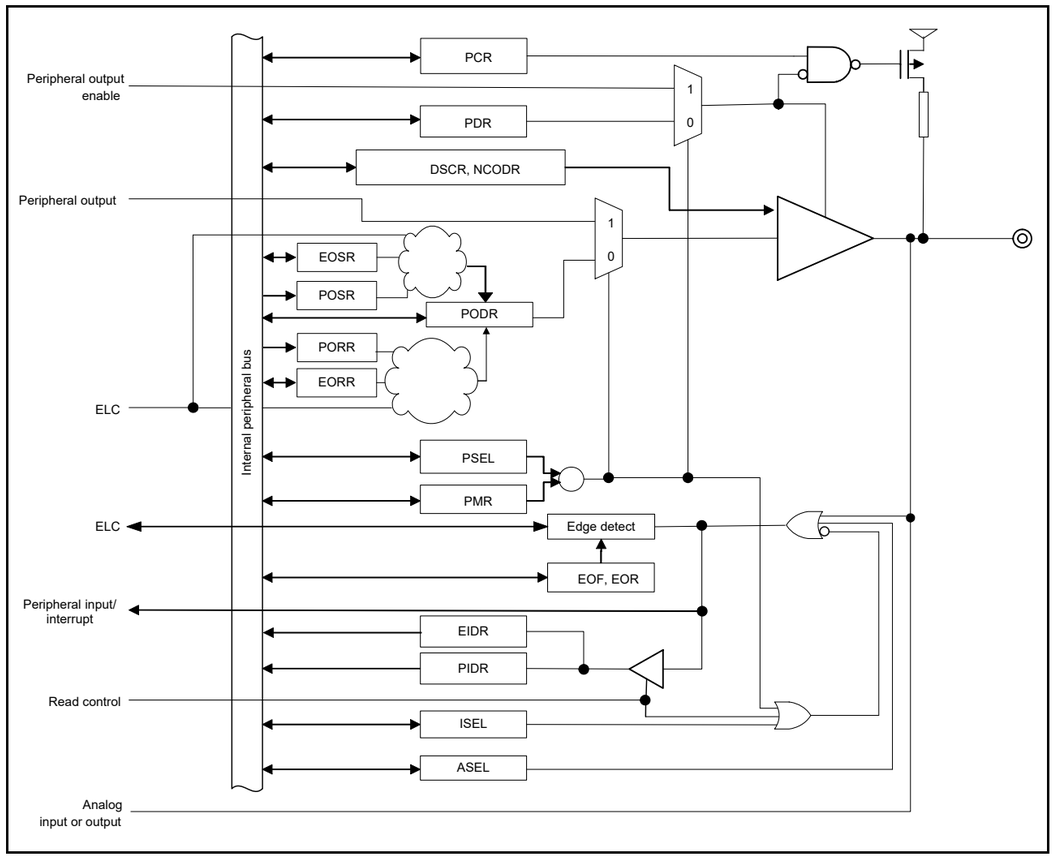


Figure 20.1 Connection diagram for I/O port registers

Note: Figure 20.1 shows a basic port configuration. The configuration differs depending on the ports.

20. I/O Ports

20.1 Overview

IO端口引脚用作通用IO端口引脚、外围模块的IO引脚、中断输入引脚、模拟IO、ELC的端口组功能或总线控制引脚。所有引脚在复位后立即作为输入引脚工作，引脚功能通过寄存器设置进行切换。您可以为寄存器中的每个引脚指定关联的IO端口和外围模块。

图20.1显示了IO端口寄存器的连接图。IO端口的配置因封装而异。表20.1按封装列出了IO端口规格，表20.2列出了端口功能。

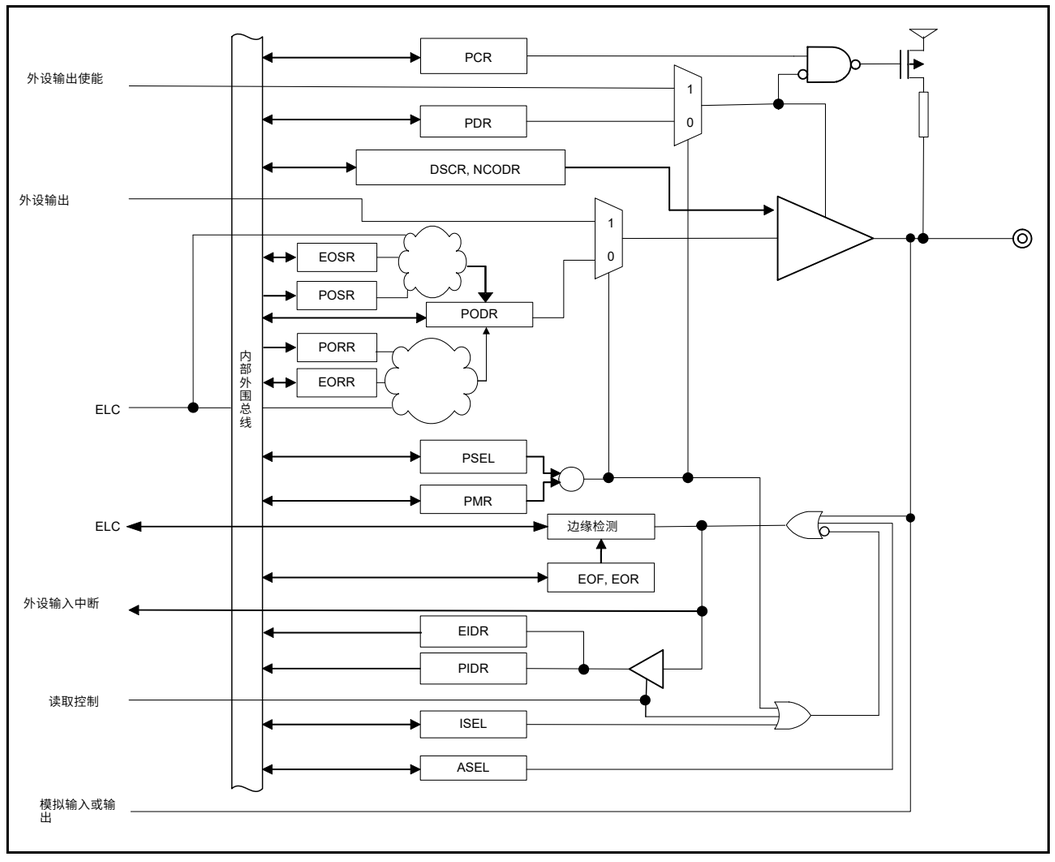


Figure 20.1 IO端口寄存器的连接图

Note: 图20.1显示了一个基本的端口配置。配置因端口而异。

Table 20.1 I/O port specifications

Port	Package 176 pins	Number of pins	Package 144 pins, 145 pins	Number of pins	Package 100 pins	Number of pins
PORT0	P000 to P010, P014, P015	13	P000 to P009, P014, P015	12	P000 to P008, P014, P015	11
PORT1	P100 to P115	16	P100 to P115	16	P100 to P115	16
PORT2	P200 to P214	15	P200 to P214	15	P200, P201, P205 to P214	12
PORT3	P300 to P315	16	P300 to P313	14	P300 to P307	8
PORT4	P400 to P415	16	P400 to P415	16	P400 to P415	16
PORT5	P500 to P508, P511 to P513	12	P500 to P506, P508, P511, P512	10	P500 to P504, P508	6
PORT6	P600 to P615	16	P600 to P605, P608 to P614	13	P600 to P602, P608 to P610	6
PORT7	P700 to P708	9	P700 to P705, P708 to P713	12	P708	1
PORT8	P800 to P806	7	P800, P801	2	N/A	0
PORT9	P900, P901, P905 to P908	6	N/A	0	N/A	0
PORTA	PA00, PA01, PA08 to PA10	5	N/A	0	N/A	0
PORTB	PB00, PB01	2	N/A	0	N/A	0
	Total pins	133	Total pins	110	Total pins	76

Table 20.2 I/O port functions

Port	Port name	Input pull-up	Open-drain output	Drive capacity switching	5-V tolerant
PORT0	P000 to P007	-	-	-	-
	P008 to P010, P014, P015	✓	✓	-	-
PORT1	P100 to P115	✓	✓	Low, middle, high	-
PORT2	P200	✓	-	-	-
	P201	✓	✓	-	-
	P202 to P204, P207 to P214	✓	✓	Low, middle, high	-
	P205, P206	✓	✓	Low, middle, high	✓
PORT3	P300 to P315	✓	✓	Low, middle, high	-
PORT4	P400, P401, P407 to P415	✓	✓	Low, middle, high	✓
	P402 to P406	✓	✓	Low, middle, high	-
PORT5	P500 to P508, P513	✓	✓	Low, middle, high	-
	P511, P512	✓	✓	Low, middle, high	✓
PORT6	P600 to P615*1	✓	✓	Low, middle, high	-
PORT7	P700 to P707	✓	✓	Low, middle, high	-
	P708 to P713	✓	✓	Low, middle, high	✓
PORT8	P800 to P806	✓	✓	Low, middle, high	-
PORT9	P900, P901, P905 to P908	✓	✓	Low, middle, high	-
PORTA	PA00, PA01, PA08 to PA10	✓	✓	Low, middle, high	-
PORTB	PB00	✓	✓	Low, middle, high	-
	PB01	✓	✓	Low, middle, high	✓

✓: Available

Table 20.1 IO端口规格

Port	Package 176 pins	引脚数	Package 144 pins, 145 pins	引脚数	Package 100 pins	引脚数
PORT0	P000 to P010, P014, P015	13	P000 to P009, P014, P015	12	P000 to P008, P014, P015	11
PORT1	P100 to P115	16	P100 to P115	16	P100 to P115	16
PORT2	P200 to P214	15	P200 to P214	15	P200, P201, P205 to P214	12
PORT3	P300 to P315	16	P300 to P313	14	P300 to P307	8
PORT4	P400 to P415	16	P400 to P415	16	P400 to P415	16
PORT5	P500 to P508, P511 to P513	12	P500 to P506, P508, P511, P512	10	P500 to P504, P508	6
PORT6	P600 to P615	16	P600 to P605, P608 to P614	13	P600 to P602, P608 to P610	6
PORT7	P700 to P708	9	P700 to P705, P708 to P713	12	P708	1
PORT8	P800 to P806	7	P800, P801	2	N/A	0
PORT9	P900, P901, P905 to P908	6	N/A	0	N/A	0
PORTA	PA00, PA01, PA08 to PA10	5	N/A	0	N/A	0
PORTB	PB00, PB01	2	N/A	0	N/A	0
	总针数	133	总针数	110	总针数	76

Table 20.2 IO口功能

Port	端口名称	Input pull-up	Open-drain output	驱动容量切换	5-V tolerant
PORT0	P000 to P007	-	-	-	-
	P008 to P010, P014, P015	✓	✓	-	-
PORT1	P100 to P115	✓	✓	低、中、高	-
PORT2	P200	✓	-	-	-
	P201	✓	✓	-	-
	P202 to P204, P207 to P214	✓	✓	低、中、高	-
	P205, P206	✓	✓	低、中、高	✓
PORT3	P300 to P315	✓	✓	低、中、高	-
PORT4	P400, P401, P407 to P415	✓	✓	低、中、高	✓
	P402 to P406	✓	✓	低、中、高	-
PORT5	P500 to P508, P513	✓	✓	低、中、高	-
	P511, P512	✓	✓	低、中、高	✓
PORT6	P600 to P615*1	✓	✓	低、中、高	-
PORT7	P700 to P707	✓	✓	低、中、高	-
	P708 to P713	✓	✓	低、中、高	✓
PORT8	P800 to P806	✓	✓	低、中、高	-
PORT9	P900, P901, P905 to P908	✓	✓	低、中、高	-
PORTA	PA00, PA01, PA08 to PA10	✓	✓	低、中、高	-
PORTB	PB00	✓	✓	低、中、高	-
	PB01	✓	✓	低、中、高	✓

✓: Available

Note 1. When P602 is set to EBCLK/SDCLK (PmnPFS.PSEL[4:0] are set to 01011b), the drive capacity of P602 is set high.

20.2 Register Descriptions

20.2.1 Port Control Register 1 (PCNTR1/PODR/PDR)

Address(es): PORT0.PCNTR1 4004 0000h, PORT1.PCNTR1 4004 0020h, PORT2.PCNTR1 4004 0040h, PORT3.PCNTR1 4004 0060h, PORT4.PCNTR1 4004 0080h, PORT5.PCNTR1 4004 00A0h, PORT6.PCNTR1 4004 00C0h, PORT7.PCNTR1 4004 00E0h, PORT8.PCNTR1 4004 0100h, PORT9.PCNTR1 4004 0120h, PORTA.PCNTR1 4004 0140h, PORTB.PCNTR1 4004 0160h

PORT0.PODR 4004 0000h, PORT1.PODR 4004 0020h, PORT2.PODR 4004 0040h, PORT3.PODR 4004 0060h, PORT4.PODR 4004 0080h, PORT5.PODR 4004 00A0h, PORT6.PODR 4004 00C0h, PORT7.PODR 4004 00E0h, PORT8.PODR 4004 0100h, PORT9.PODR 4004 0120h, PORTA.PODR 4004 0140h, PORTB.PODR 4004 0160h

PORT0.PDR 4004 0002h, PORT1.PDR 4004 0022h, PORT2.PDR 4004 0042h, PORT3.PDR 4004 0062h, PORT4.PDR 4004 0082h, PORT5.PDR 4004 00A2h, PORT6.PDR 4004 00C2h, PORT7.PDR 4004 00E2h, PORT8.PDR 4004 0102h, PORT9.PDR 4004 0122h, PORTA.PDR 4004 0142h, PORTB.PDR 4004 0162h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	PODR15	PODR14	PODR13	PODR12	PODR11	PODR10	PODR09	PODR08	PODR07	PODR06	PODR05	PODR04	PODR03	PODR02	PODR01	PODR00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PDR15	PDR14	PDR13	PDR12	PDR11	PDR10	PDR09	PDR08	PDR07	PDR06	PDR05	PDR04	PDR03	PDR02	PDR01	PDR00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b15 to b0	PDRn	Pmn Direction	0: Input (functions as an input pin) 1: Output (functions as an output pin).	R/W
b31 to b16	PODRn	Pmn Output Data	0: Low output 1: High output.	R/W

m = 0 to 9, A, B
n = 00 to 15

The Port Control Register 1 is a 32-bit and 16-bit read/write register that controls port direction and port output data.

The PCNTR1 specifies the port direction and the output data, and is accessed in 32-bit units. The PDRn (bits [15:0] in PCNTR1) and PODRn (bits [31:16] in PCNTR1) respectively, are accessed in 16-bit units.

The PDRn bits select the input or output direction for individual pins on the associated port when the pins are configured as general I/O pins. Each pin on port m is associated with a PORTm.PCNTR1.PDRn bit. The I/O direction can be specified in 1-bit units. Bits associated with non-existent pins are reserved. The write value should be 0. P000 to P007 and P200 are input only, so PORT0.PCNTR1.PDR00-PDR07 and PORT2.PCNTR1.PDR00 are reserved. The PDRn bit in the PORTm.PCNTR1 register serves the same function as the PDR bit in the PFS.PmnPFS register.

The PODRn bits hold data to be output from the general I/O pins. Bits associated with non-existent pins are reserved. The write value should be 0. P000 to P007 and P200 are input only, so PORT0.PCNTR1.PODR00-PODR07 and PORT2.PCNTR1.PODR00 are reserved. Writes to P000 to P007 and P200 have no effect. The PODRn bit in the PORTm.PCNTR1 register serves the same function as the PODR bit in the PFS.PmnPFS register.

Note 1. 当P602设置为EBCLKSDCLK （PmnPFS.PSEL[4:0]设置为01011b）时，P602的驱动能力设置为高。

20.2 注册说明

20.2.1 端口控制寄存器1(PCNTR1PODRPDR)

Address(es): PORT0.PCNTR1 4004 0000h, PORT1.PCNTR1 4004 0020h, PORT2.PCNTR1 4004 0040h, PORT3.PCNTR1 4004 0060h, PORT4.PCNTR1 4004 0080h, PORT5.PCNTR1 4004 00A0h, PORT6.PCNTR1 4004 00C0h, PORT7.PCNTR1 4004 00E0h, PORT8.PCNTR1 4004 0100h, PORT9.PCNTR1 4004 0120h, PORTA.PCNTR1 4004 0140h, PORTB.PCNTR1 4004 0160h

PORT0.PODR 4004 0000h, PORT1.PODR 4004 0020h, PORT2.PODR 4004 0040h, PORT3.PODR 4004 0060h, PORT4.PODR 4004 0080h, PORT5.PODR 4004 00A0h, PORT6.PODR 4004 00C0h, PORT7.PODR 4004 00E0h, PORT8.PODR 4004 0100h, PORT9.PODR 4004 0120h, PORTA.PODR 4004 0140h, PORTB.PODR 4004 0160h

PORT0.PDR 4004 0002h, PORT1.PDR 4004 0022h, PORT2.PDR 4004 0042h, PORT3.PDR 4004 0062h, PORT4.PDR 4004 0082h, PORT5.PDR 4004 00A2h, PORT6.PDR 4004 00C2h, PORT7.PDR 4004 00E2h, PORT8.PDR 4004 0102h, PORT9.PDR 4004 0122h, PORTA.PDR 4004 0142h, PORTB.PDR 4004 0162h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	PODR15	PODR14	PODR13	PODR12	PODR11	PODR10	PODR09	PODR08	PODR07	PODR06	PODR05	PODR04	PODR03	PODR02	PODR01	PODR00
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PDR15	PDR14	PDR13	PDR12	PDR11	PDR10	PDR09	PDR08	PDR07	PDR06	PDR05	PDR04	PDR03	PDR02	PDR01	PDR00
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b15 to b0	PDRn	Pmn Direction	0：输入（用作输入引脚）1：输出（用作输出引脚）。	R/W
b31 to b16	PODRn	Pmn输出数据	0：低输出1：高输出。	R/W

m = 0 to 9, A, B
n = 00 to 15

端口控制寄存器1是一个32位和16位读写寄存器，用于控制端口方向和端口输出数据。

PCNTR1指定端口方向和输出数据，并以32位为单位进行访问。PDRn（位[15:0]在PCNTR1)和PODRn（PCNTR1中的位[31:16]）分别以16位为单位进行访问。

当引脚配置为通用IO引脚时，PDRn位选择相关端口上各个引脚的输入或输出方向。端口m上的每个引脚都与一个PORTm.PCNTR1.PDRn位相关联。可以以1位为单位指定IO方向。与不存在的引脚相关的位被保留。写入值应为0。P000到P007和P200仅为输入，因此保留PORT0.PCNTR1.PDR00-PDR07和PORT2.PCNTR1.PDR00。PORTm.PCNTR1寄存器中的PDRn位与PFS.PmnPFS寄存器中的PDR位具有相同的功能。

PODRn位保存要从通用IO引脚输出的数据。与不存在的引脚相关的位被保留。
写入值应为0。P000到P007和P200仅为输入，因此保留PORT0.PCNTR1.PODR00-PODR07和PORT2.PCNTR1.PODR00。写入P000到P007和P200无效。在PODRn位
PORTm.PCNTR1寄存器的功能与PFS.PmnPFS寄存器中的PODR位相同。

20.2.2 Port Control Register 2 (PCNTR2/EIDR/PIDR)

Address(es): PORT0.PCNTR2 4004 0004h, PORT1.PCNTR2 4004 0024h, PORT2.PCNTR2 4004 0044h, PORT3.PCNTR2 4004 0064h, PORT4.PCNTR2 4004 0084h, PORT5.PCNTR2 4004 00A4h, PORT6.PCNTR2 4004 00C4h, PORT7.PCNTR2 4004 00E4h, PORT8.PCNTR2 4004 0104h, PORT9.PCNTR2 4004 0124h, PORTA.PCNTR2 4004 0144h, PORTB.PCNTR2 4004 0164h

PORT1.EIDR 4004 0024h, PORT2.EIDR 4004 0044h, PORT3.EIDR 4004 0064h, PORT4.EIDR 4004 0084h

PORT0.PIDR 4004 0006h, PORT1.PIDR 4004 0026h, PORT2.PIDR 4004 0046h, PORT3.PIDR 4004 0066h, PORT4.PIDR 4004 0086h, PORT5.PIDR 4004 00A6h, PORT6.PIDR 4004 00C6h, PORT7.PIDR 4004 00E6h, PORT8.PIDR 4004 0106h, PORT9.PIDR 4004 0126h, PORTA.PIDR 4004 0146h, PORTB.PIDR 4004 0166h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	EIDR15	EIDR14	EIDR13	EIDR12	EIDR11	EIDR10	EIDR09	EIDR08	EIDR07	EIDR06	EIDR05	EIDR04	EIDR03	EIDR02	EIDR01	EIDR00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PIDR15	PIDR14	PIDR13	PIDR12	PIDR11	PIDR10	PIDR09	PIDR08	PIDR07	PIDR06	PIDR05	PIDR04	PIDR03	PIDR02	PIDR01	PIDR00
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b15 to b0	PIDRn	Pmn State	0: Low level 1: High level.	R
b31 to b16	EIDRn	Port Event Input Data*1	When an ELC_PORTx occurs: 0: Low input 1: High input.	R

m = 0 to 9, A, B
n = 00 to 15
x = 1 to 4

Note 1. Supported for PORT1 to PORT4.

The Port Control Register 2 (PCNTR2/EIDR/PIDR) allows read access to the Pmn state and the port event input data using 32-bit or 16-bit access.

The PCNTR2 specifies the Pmn state and the port event input data, and is accessed in 32-bit units. The PIDRn (bits [15:0] in PCNTR2) and EIDRn (bits [31:16] in PCNTR2) respectively, are accessed in 16-bit units. Bits associated with non-existent pins are reserved. Reserved bits are read as undefined.

The PIDRn bits reflect individual pin states of the port, regardless of the values set in PmnPFS.PMR and PORTm.PCNTR1.PDRn. The PIDRn bit in the PORTm.PCNTR2 register serves the same function as the PIDR bit in the PFS.PmnPFS register.

A pin state cannot be reflected in PIDRn when one of the following functions is enabled:

- Main clock oscillator (MOSC)
- CS area controller (CSC)
- Analog function (ASEL = 1)
- Capacitive Touch Sensing Unit (CTSU)
- USB 2.0 Full-Speed (USBFS) module.

The EIDRn bits latch a pin state when an ELC_PORTx signal occurs. Pin states can only be input to EIDRn when PmnPFS.PMR and PORTm.PCNTR1.PDRn are 0. When the PmnPFS.ASEL bit is set to 1, the associated pin state is not reflected in EIDRn.

20.2.2 端口控制寄存器2(PCNTR2EIDRPIDR)

Address(es): PORT0.PCNTR2 4004 0004h, PORT1.PCNTR2 4004 0024h, PORT2.PCNTR2 4004 0044h, PORT3.PCNTR2 4004 0064h, PORT4.PCNTR2 4004 0084h, PORT5.PCNTR2 4004 00A4h, PORT6.PCNTR2 4004 00C4h, PORT7.PCNTR2 4004 00E4h, PORT8.PCNTR2 4004 0104h, PORT9.PCNTR2 4004 0124h, PORTA.PCNTR2 4004 0144h, PORTB.PCNTR2 4004 0164h

PORT1.EIDR 4004 0024h, PORT2.EIDR 4004 0044h, PORT3.EIDR 4004 0064h, PORT4.EIDR 4004 0084h

PORT0.PIDR 4004 0006h, PORT1.PIDR 4004 0026h, PORT2.PIDR 4004 0046h, PORT3.PIDR 4004 0066h, PORT4.PIDR 4004 0086h, PORT5.PIDR 4004 00A6h, PORT6.PIDR 4004 00C6h, PORT7.PIDR 4004 00E6h, PORT8.PIDR 4004 0106h, PORT9.PIDR 4004 0126h, PORTA.PIDR 4004 0146h, PORTB.PIDR 4004 0166h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	EIDR15	EIDR14	EIDR13	EIDR12	EIDR11	EIDR10	EIDR09	EIDR08	EIDR07	EIDR06	EIDR05	EIDR04	EIDR03	EIDR02	EIDR01	EIDR00
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PIDR15	PIDR14	PIDR13	PIDR12	PIDR11	PIDR10	PIDR09	PIDR08	PIDR07	PIDR06	PIDR05	PIDR04	PIDR03	PIDR02	PIDR01	PIDR00
重置后的值:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b15 to b0	PIDRn	Pmn State	0：低电平1 ：高电平。	R
b31 to b16	EIDRn	端口事件输入数据*1	当ELC_PORTx发生时：0：低 输入1：高输入。	R

m = 0 to 9, A, B
n = 00 to 15
x = 1 to 4

Note 1. 支持PORT1到PORT4。

端口控制寄存器2(PCNTR2EIDRPIDR)允许使用32位或16位访问对Pmn状态和端口事件输入数据进行读取访问。

PCNTR2指定Pmn状态和端口事件输入数据，并以32位为单位进行访问。PIDRn（PCNTR2中的位[15:0]）和EIDRn（PCNTR2中的位[31:16]）分别以16位为单位进行访问。与不存在的引脚相关的位被保留。保留位被读取为未定义。

PIDRn位反映端口的各个引脚状态，无论PmnPFS.PMR和PORTm.PCNTR1.PDRn。PORTm.PCNTR2寄存器中的PIDRn位与PFS.PmnPFS register.

当启用以下功能之一时，引脚状态无法反映在PIDRn中：

- 主时钟振荡器(MOSC)
- CS区域控制器(CSC)
- 模拟功能(ASEL=1)
- 电容式触控感应单元(CTSU)
- USB2.0全速(USBFS)模块。

当ELC_PORTx信号出现时，EIDRn位锁存引脚状态。引脚状态只能输入到EIDRn时PmnPFS.PMR和PORTm.PCNTR1.PDRn为0。当PmnPFS.ASEL位设置为1时，相关引脚状态不会反映在EIDRn中。

20.2.3 Port Control Register 3 (PCNTR3/PORR/POSR)

Address(es): PORT0.PCNTR3 4004 0008h, PORT1.PCNTR3 4004 0028h, PORT2.PCNTR3 4004 0048h, PORT3.PCNTR3 4004 0068h, PORT4.PCNTR3 4004 0088h, PORT5.PCNTR3 4004 00A8h, PORT6.PCNTR3 4004 00C8h, PORT7.PCNTR3 4004 00E8h, PORT8.PCNTR3 4004 0108h, PORT9.PCNTR3 4004 0128h, PORTA.PCNTR3 4004 0148h, PORTB.PCNTR3 4004 0168h

PORT0.PORR 4004 0008h, PORT1.PORR 4004 0028h, PORT2.PORR 4004 0048h, PORT3.PORR 4004 0068h, PORT4.PORR 4004 0088h, PORT5.PORR 4004 00A8h, PORT6.PORR 4004 00C8h, PORT7.PORR 4004 00E8h, PORT8.PORR 4004 0108h, PORT9.PORR 4004 0128h, PORTA.PORR 4004 0148h, PORTB.PORR 4004 0168h

PORT0.POSR 4004 000Ah, PORT1.POSR 4004 002Ah, PORT2.POSR 4004 004Ah, PORT3.POSR 4004 006Ah, PORT4.POSR 4004 008Ah, PORT5.POSR 4004 00AAh, PORT6.POSR 4004 00CAh, PORT7.POSR 4004 00EAh, PORT8.POSR 4004 010Ah, PORT9.POSR 4004 012Ah, PORTA.POSR 4004 014Ah, PORTB.POSR 4004 016Ah

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	PORR 15	PORR 14	PORR 13	PORR 12	PORR 11	PORR 10	PORR 09	PORR 08	PORR 07	PORR 06	PORR 05	PORR 04	PORR 03	PORR 02	PORR 01	PORR 00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	POSR 15	POSR 14	POSR 13	POSR 12	POSR 11	POSR 10	POSR 09	POSR 08	POSR 07	POSR 06	POSR 05	POSR 04	POSR 03	POSR 02	POSR 01	POSR 00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b15 to b0	POSRn	Pmn Output Set	0: No effect on output 1: High output.	W
b31 to b16	PORRn	Pmn Output Reset	0: No effect on output 1: Low output.	W

m = 0 to 9, A, B

n = 00 to 15

The Port Control Register 3 (PCNTR3/PORR/POSR) is a 32-bit and 16-bit write register that controls the setting or resetting of the port output data.

The PCNTR3 controls the setting or resetting of the port output data, and is accessed in 32-bit units. The POSRn (bits [15:0] in PCNTR3) and PORRn (bits [31:16] in PCNTR3) respectively, are accessed in 16-bit units.

POSR changes PODR when set by a software write. For example, for P100, when PORT1.PCNTR3.POSR00 is 1, PORT1.PCNTR1.PODR00 outputs 1. Bits associated with non-existent pins are reserved. The write value should always be 0. P000 to P007 and P200 are input only, so PORT0.PCNTR3.POSR00-07 and PORT2.PCNTR3.POSR00 are reserved.

PORR changes PODR when reset by a software write. For example, for P100, when PORT1.PCNTR3.PORR00 is 1, PORT1.PCNTR1.PODR00 outputs 0. Bits associated with non-existent pins are reserved. The write value should always be 0. P000 to P007 and P200 are input only, so PORT0.PCNTR3.PORR00-07 and PORT2.PCNTR3.PORR00 are reserved.

Note: When EORRn or EOSRn is set, writing is prohibited to PODRn, PORRn, and POSRn.
Note: PORRn and POSRn should not be set at the same time.

20.2.3 端口控制寄存器3(PCNTR3PORRPOSR)

Address(es): PORT0.PCNTR3 4004 0008h, PORT1.PCNTR3 4004 0028h, PORT2.PCNTR3 4004 0048h, PORT3.PCNTR3 4004 0068h, PORT4.PCNTR3 4004 0088h, PORT5.PCNTR3 4004 00A8h, PORT6.PCNTR3 4004 00C8h, PORT7.PCNTR3 4004 00E8h, PORT8.PCNTR3 4004 0108h, PORT9.PCNTR3 4004 0128h, PORTA.PCNTR3 4004 0148h, PORTB.PCNTR3 4004 0168h

PORT0.PORR 4004 0008h, PORT1.PORR 4004 0028h, PORT2.PORR 4004 0048h, PORT3.PORR 4004 0068h, PORT4.PORR 4004 0088h, PORT5.PORR 4004 00A8h, PORT6.PORR 4004 00C8h, PORT7.PORR 4004 00E8h, PORT8.PORR 4004 0108h, PORT9.PORR 4004 0128h, PORTA.PORR 4004 0148h, PORTB.PORR 4004 0168h

PORT0.POSR 4004 000Ah, PORT1.POSR 4004 002Ah, PORT2.POSR 4004 004Ah, PORT3.POSR 4004 006Ah, PORT4.POSR 4004 008Ah, PORT5.POSR 4004 00AAh, PORT6.POSR 4004 00CAh, PORT7.POSR 4004 00EAh, PORT8.POSR 4004 010Ah, PORT9.POSR 4004 012Ah, PORTA.POSR 4004 014Ah, PORTB.POSR 4004 016Ah

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	PORR 15	PORR 14	PORR 13	PORR 12	PORR 11	PORR 10	PORR 09	PORR 08	PORR 07	PORR 06	PORR 05	PORR 04	PORR 03	PORR 02	PORR 01	PORR 00
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	POSR 15	POSR 14	POSR 13	POSR 12	POSR 11	POSR 10	POSR 09	POSR 08	POSR 07	POSR 06	POSR 05	POSR 04	POSR 03	POSR 02	POSR 01	POSR 00
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b15 to b0	POSRn	Pmn输出设置	0：对输出无影响1： 高输出。	W
b31 to b16	PORRn	Pmn输出复位	0：对输出无影响1： 低输出。	W

m = 0 to 9, A, B

n = 00 to 15

端口控制寄存器3(PCNTR3PORRPOSR)是一个32位和16位写寄存器，用于控制端口输出数据的设置或复位。

PCNTR3控制端口输出数据的设置或复位，并以32位为单位进行访问。POSRn（PCNTR3中的位[15:0]）和PORRn（PCNTR3中的位[31:16]）分别以16位为单位进行访问。

POSR在通过软件写入设置时改变PODR。例如，对于P100，当PORT1.PCNTR3.POSR00为1时，PORT1.PCNTR1.PODR00输出1。与不存在的引脚相关的位被保留。写入值应始终为0。P000到P007和P200仅为输入，因此保留PORT0.PCNTR3.POSR00-07和PORT2.PCNTR3.POSR00。

PORR在通过软件写入复位时改变PODR。例如，对于P100，当PORT1.PCNTR3.PORR00为1时，PORT1.PCNTR1.PODR00输出0。与不存在的引脚相关的位被保留。写入值应始终为0。P000至P007和P200仅为输入，因此保留PORT0.PCNTR3.PORR00-07和PORT2.PCNTR3.PORR00。

Note: 当设置EORRn或EOSRn时，禁止写入PODRn、PORRn和POSRn。
Note: PORRn和POSRn不应同时设置。

20.2.4 Port Control Register 4 (PCNTR4/EORR/EOSR)

Address(es): PORT1.PCNTR4 4004 002Ch, PORT2.PCNTR4 4004 004Ch, PORT3.PCNTR4 4004 006Ch, PORT4.PCNTR4 4004 008Ch
PORT1.EORR 4004 002Ch, PORT2.EORR 4004 004Ch, PORT3.EORR 4004 006Ch, PORT4.EORR 4004 008Ch
PORT1.EOSR 4004 002Eh, PORT2.EOSR 4004 004Eh, PORT3.EOSR 4004 006Eh, PORT4.EOSR 4004 008Eh

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	EORR 15	EORR 14	EORR 13	EORR 12	EORR 11	EORR 10	EORR 09	EORR 08	EORR 07	EORR 06	EORR 05	EORR 04	EORR 03	EORR 02	EORR 01	EORR 00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	EOSR 15	EOSR 14	EOSR 13	EOSR 12	EOSR 11	EOSR 10	EOSR 09	EOSR 08	EOSR 07	EOSR 06	EOSR 05	EOSR 04	EOSR 03	EOSR 02	EOSR 01	EOSR 00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b15 to b0	EOSRn	Pmn Event Output Set	When an ELC_PORTx signal occurs: 0: No effect on output 1: High output.	R/W
b31 to b16	EORRn	Pmn Event Output Reset	When an ELC_PORTx signal occurs: 0: No effect on output 1: Low output.	R/W

m = 1 to 4
n = 00 to 15
x = 1 to 4

Port Control Register 4 (PCNTR4/EORR/EOSR) is a 32-bit and 16-bit read/write register that controls the setting or resetting of the port output data by event input from the ELC.

The PCNTR4 controls the setting or resetting of the port output data by event input from the ELC, and is accessed in 32-bit units. The EOSRn (bits [15:0] in PCNTR4) and EORRn (bits [31:16] in PCNTR4) respectively, are accessed in 16-bit units.

EOSR changes PODR when set because an ELC_PORTx signal occurs. For example, for P100, if PORT1.PCNTR4.EOSR00 is set to 1 when the ELC_PORTx occurs, PORT1.PCNTR1.PODR00 outputs 1. Bits associated with non-existent pins are reserved. The write value should always be 0. P000 to P007 and P200 are input only, so PORT0.PCNTR4.EOSR00-07 and PORT2.PCNTR4.EOSR00 are reserved.

EORR changes PODR when reset because an ELC_PORTx signal occurs. For example, for P100, if PORT1.PCNTR4.EORR00 is set to 1 when the ELC_PORTx occurs, PORT1.PCNTR1.PODR00 outputs 0. Bits associated with non-existent pins are reserved. The write value should always be 0. P000 to P007 and P200 are input only, so PORT0.PCNTR4.EORR00-07 and PORT2.PCNTR4.EORR00 are reserved.

Note: When EORRn or EOSRn is set, writing is prohibited to PODRn, PORRn, and POSRn.
Note: EORRn and EOSRn should not be set at the same time.

20.2.4 端口控制寄存器4(PCNTR4EORREOSR)

Address(es): PORT1.PCNTR4 4004 002Ch, PORT2.PCNTR4 4004 004Ch, PORT3.PCNTR4 4004 006Ch, PORT4.PCNTR4 4004 008Ch
PORT1.EORR 4004 002Ch, PORT2.EORR 4004 004Ch, PORT3.EORR 4004 006Ch, PORT4.EORR 4004 008Ch
PORT1.EOSR 4004 002Eh, PORT2.EOSR 4004 004Eh, PORT3.EOSR 4004 006Eh, PORT4.EOSR 4004 008Eh

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	EORR 15	EORR 14	EORR 13	EORR 12	EORR 11	EORR 10	EORR 09	EORR 08	EORR 07	EORR 06	EORR 05	EORR 04	EORR 03	EORR 02	EORR 01	EORR 00
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	EOSR 15	EOSR 14	EOSR 13	EOSR 12	EOSR 11	EOSR 10	EOSR 09	EOSR 08	EOSR 07	EOSR 06	EOSR 05	EOSR 04	EOSR 03	EOSR 02	EOSR 01	EOSR 00
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b15 to b0	EOSRn	Pmn事件输出集	当ELC_PORTx信号出现时：0：对输出没有影响1：高输出。	R/W
b31 to b16	EORRn	Pmn事件输出复位	当ELC_PORTx信号发生时：0：对输出没有影响1：低输出。	R/W

m = 1 to 4
n = 00 to 15
x = 1 to 4

端口控制寄存器4(PCNTR4EORREOSR)是一个32位和16位读写寄存器，通过来自ELC的事件输入来控制端口输出数据的设置或复位。

PCNTR4通过来自ELC的事件输入来控制端口输出数据的设置或复位，并以32位为单位进行访问。分别以16位为单位访问EOSRn（PCNTR4中的位[15:0]）和EORRn（PCNTR4中的位[31:16]）。

EOSR在设置时会更改PODR，因为发生ELC_PORTx信号。例如，对于P100，如果当ELC_PORTx发生时，PORT1.PCNTR4.EOSR00设置为1，PORT1.PCNTR1.PODR00输出1。与不存在的引脚相关的位被保留。写入值应始终为0。P000到P007和P200仅为输入，因此保留PORT0.PCNTR4.EOSR00-07和PORT2.PCNTR4.EOSR00。

EORR会在复位时更改PODR，因为发生ELC_PORTx信号。例如，对于P100，如果当ELC_PORTx发生时，PORT1.PCNTR4.EORR00设置为1，PORT1.PCNTR1.PODR00输出0。与不存在的引脚相关的位被保留。写入值应始终为0。P000到P007和P200仅为输入，因此保留PORT0.PCNTR4.EORR00-07和PORT2.PCNTR4.EORR00。

Note: 当设置EORRn或EOSRn时，禁止写入PODRn、PORRn和POSRn。
Note: EORRn和EOSRn不应同时设置。

20.2.5 Port mn Pin Function Select Register (PmnPFS/PmnPFS_HA/PmnPFS_BY) (m = 0 to 9, A, B; n = 00 to 15)

Address(es): PFS.P000PFS 4004 0800h to PFS.P015PFS 4004 083Ch, PFS.P100PFS 4004 0840h to PFS.P115PFS 4004 087Ch, PFS.P200PFS 4004 0880h to PFS.P214PFS 4004 08B8h, PFS.P300PFS 4004 08C0h to PFS.P315PFS 4004 08FCh, PFS.P400PFS 4004 0900h to PFS.P415PFS 4004 093Ch, PFS.P500PFS 4004 0940h to PFS.P513PFS 4004 0974h, PFS.P600PFS 4004 0980h to PFS.P615PFS 4004 09BCh, PFS.P700PFS 4004 09C0h to PFS.P713PFS 4004 09F4h, PFS.P800PFS 4004 0A00h to PFS.P806PFS 4004 0A18h, PFS.P900PFS 4004 0A40h to PFS.P908PFS 4004 0A60h, PFS.PA00PFS 4004 0A80h to PFS.PA10PFS 4004 0AA8h, PFS.PB00PFS 4004 0AC0h to PFS.PB01PFS 4004 0AC4h

PFS.P000PFS_HA 4004 0802h to PFS.P015PFS_HA 4004 083Eh, PFS.P100PFS_HA 4004 0842h to PFS.P115PFS_HA 4004 087Eh, PFS.P200PFS_HA 4004 0882h to PFS.P214PFS_HA 4004 08BAh, PFS.P300PFS_HA 4004 08C2h to PFS.P315PFS_HA 4004 08FEh, PFS.P400PFS_HA 4004 0902h to PFS.P415PFS_HA 4004 093Eh, PFS.P500PFS_HA 4004 0942h to PFS.P513PFS_HA 4004 0976h, PFS.P600PFS_HA 4004 0982h to PFS.P615PFS_HA 4004 09BEh, PFS.P700PFS_HA 4004 09C2h to PFS.P713PFS_HA 4004 09F6h, PFS.P800PFS_HA 4004 0A02h to PFS.P806PFS_HA 4004 0A1Ah, PFS.P900PFS_HA 4004 0A42h to PFS.P908PFS_HA 4004 0A62h, PFS.PA00PFS_HA 4004 0A82h to PFS.PA10PFS_HA 4004 0AAAh, PFS.PB00PFS_HA 4004 0AC2h to PFS.PB01PFS_HA 4004 0AC6h

PFS.P000PFS_BY 4004 0803h to PFS.P015PFS_BY 4004 083Fh, PFS.P100PFS_BY 4004 0843h to PFS.P115PFS_BY 4004 087Fh, PFS.P200PFS_BY 4004 0883h to PFS.P214PFS_BY 4004 08BBh, PFS.P300PFS_BY 4004 08C3h to PFS.P315PFS_BY 4004 08FFh, PFS.P400PFS_BY 4004 0903h to PFS.P415PFS_BY 4004 093Fh, PFS.P500PFS_BY 4004 0943h to PFS.P513PFS_BY 4004 0977h, PFS.P600PFS_BY 4004 0983h to PFS.P615PFS_BY 4004 09BFh, PFS.P700PFS_BY 4004 09C3h to PFS.P713PFS_BY 4004 09F7h, PFS.P800PFS_BY 4004 0A03h to PFS.P806PFS_BY 4004 0A1Bh, PFS.P900PFS_BY 4004 0A43h to PFS.P908PFS_BY 4004 0A63h, PFS.PA00PFS_BY 4004 0A83h to PFS.PA10PFS_BY 4004 0AABh, PFS.PB00PFS_BY 4004 0AC3h to PFS.PB01PFS_BY 4004 0AC7h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	PSEL[4:0]					—	—	—	—	—	—	—	PMR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0*2

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ASEL	ISEL	EOF	EOR	DSCR[1:0]		—	—	—	NCODR	—	PCR	—	PDR	PIDR	PODR
Value after reset:	0*2	0	0	0	0	0*2	0	0	0	0	0	0*2	0	0	x	0

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b0	PODR	Port Output Data	0: Low output 1: High output.	R/W
b1	PIDR	Pmn State	0: Low level 1: High level.	R
b2	PDR	Port Direction	0: Input (functions as an input pin) 1: Output (functions as an output pin).	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	PCR	Pull-up Control	0: Disable input pull-up 1: Enable input pull-up.	R/W
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6	NCODR	N-Channel Open-Drain Control	0: CMOS output 1: NMOS open-drain output.	R/W
b9 to b7	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b11, b10	DSCR[1:0]	Port Drive Capability	b11 b10 0 0: Low drive 0 1: Middle drive 1 0: Setting prohibited 1 1: High drive.	R/W
b13, b12	EOF/EOR	Event on Falling/Event on Rising*1	b13 b12 0 0: Don't care 0 1: Detect rising edge 1 0: Detect falling edge 1 1: Detect both edges.	R/W
b14	ISEL	IRQ Input Enable	0: Not used as IRQn input pin 1: Used as IRQn input pin.	R/W
b15	ASEL	Analog Input Enable	0: Not used as analog pin 1: Used as analog pin.	R/W
b16	PMR	Port Mode Control	0: Used as general I/O pin 1: Used as I/O port for peripheral functions.	R/W

20.2.5 端口mn引脚功能选择寄存器(PmnPFSPmnPFS_HAPmnPFS_BY)(m=0到9 A B;n =00到15)

Address(es): PFS.P000PFS 4004 0800h to PFS.P015PFS 4004 083Ch, PFS.P100PFS 4004 0840h to PFS.P115PFS 4004 087Ch, PFS.P200PFS 4004 0880h to PFS.P214PFS 4004 08B8h, PFS.P300PFS 4004 08C0h to PFS.P315PFS 4004 08FCh, PFS.P400PFS 4004 0900h to PFS.P415PFS 4004 093Ch, PFS.P500PFS 4004 0940h to PFS.P513PFS 4004 0974h, PFS.P600PFS 4004 0980h to PFS.P615PFS 4004 09BCh, PFS.P700PFS 4004 09C0h to PFS.P713PFS 4004 09F4h, PFS.P800PFS 4004 0A00h to PFS.P806PFS 4004 0A18h, PFS.P900PFS 4004 0A40h to PFS.P908PFS 4004 0A60h, PFS.PA00PFS 4004 0A80h to PFS.PA10PFS 4004 0AA8h, PFS.PB00PFS 4004 0AC0h to PFS.PB01PFS 4004 0AC4h

PFS.P000PFS_HA 4004 0802h to PFS.P015PFS_HA 4004 083Eh, PFS.P100PFS_HA 4004 0842h to PFS.P115PFS_HA 4004 087Eh, PFS.P200PFS_HA 4004 0882h to PFS.P214PFS_HA 4004 08BAh, PFS.P300PFS_HA 4004 08C2h to PFS.P315PFS_HA 4004 08FEh, PFS.P400PFS_HA 4004 0902h to PFS.P415PFS_HA 4004 093Eh, PFS.P500PFS_HA 4004 0942h to PFS.P513PFS_HA 4004 0976h, PFS.P600PFS_HA 4004 0982h to PFS.P615PFS_HA 4004 09BEh, PFS.P700PFS_HA 4004 09C2h to PFS.P713PFS_HA 4004 09F6h, PFS.P800PFS_HA 4004 0A02h to PFS.P806PFS_HA 4004 0A1Ah, PFS.P900PFS_HA 4004 0A42h to PFS.P908PFS_HA 4004 0A62h, PFS.PA00PFS_HA 4004 0A82h to PFS.PA10PFS_HA 4004 0AAAh, PFS.PB00PFS_HA 4004 0AC2h to PFS.PB01PFS_HA 4004 0AC6h

PFS.P000PFS_BY 4004 0803h to PFS.P015PFS_BY 4004 083Fh, PFS.P100PFS_BY 4004 0843h to PFS.P115PFS_BY 4004 087Fh, PFS.P200PFS_BY 4004 0883h to PFS.P214PFS_BY 4004 08BBh, PFS.P300PFS_BY 4004 08C3h to PFS.P315PFS_BY 4004 08FFh, PFS.P400PFS_BY 4004 0903h to PFS.P415PFS_BY 4004 093Fh, PFS.P500PFS_BY 4004 0943h to PFS.P513PFS_BY 4004 0977h, PFS.P600PFS_BY 4004 0983h to PFS.P615PFS_BY 4004 09BFh, PFS.P700PFS_BY 4004 09C3h to PFS.P713PFS_BY 4004 09F7h, PFS.P800PFS_BY 4004 0A03h to PFS.P806PFS_BY 4004 0A1Bh, PFS.P900PFS_BY 4004 0A43h to PFS.P908PFS_BY 4004 0A63h, PFS.PA00PFS_BY 4004 0A83h to PFS.PA10PFS_BY 4004 0AABh, PFS.PB00PFS_BY 4004 0AC3h to PFS.PB01PFS_BY 4004 0AC7h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	PSEL[4:0]					—	—	—	—	—	—	—	PMR
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0*2

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ASEL	ISEL	EOF	EOR	DSCR[1:0]		—	—	—	NCODR	—	PCR	—	PDR	PIDR	PODR
重置后的值:	0*2	0	0	0	0	0*2	0	0	0	0	0	0*2	0	0	x	0

x: Undefined

Bit	Symbol	位名称	Description	R/W
b0	PODR	端口输出数据	0：低输出1： 高输出。	R/W
b1	PIDR	Pmn State	0：低电平1 ：高电平。	R
b2	PDR	港口方向	0：输入（用作输入引脚）1：输出（ 用作输出引脚）。	R/W
b3	—	Reserved	该位读取为0。写入值应为0。	R/W
b4	PCR	Pull-up Control	0：禁止输入上拉1：使 能输入上拉。	R/W
b5	—	Reserved	该位读取为0。写入值应为0。	R/W
b6	NCODR	N-Channel Open-Drain Control	0: CMOS output 1: NMOS open-drain output.	R/W
b9 to b7	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b11, b10	DSCR[1:0]	端口驱动能力	b11b1000：低驱动01： 中驱动10：禁止设置11 ：高驱动。	R/W
b13, b12	EOF/EOR	坠落事件 Rising*1	b13b1200：无关01：检 测上升沿10：检测下降沿 11：检测两个沿。	R/W
b14	ISEL	IRQ输入使能	0：不用作IRQn输入引脚1： 用作IRQn输入引脚。	R/W
b15	ASEL	模拟输入使能	0：不用作模拟引脚1：用 作模拟引脚。	R/W
b16	PMR	端口模式控制	0：用作通用IO引脚1：用作外围功能的IO 端口。	R/W

Bit	Symbol	Bit name	Description	R/W
b23 to b17	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b28 to b24	PSEL[4:0]	Peripheral Select	These bits select the peripheral function. For individual pin functions, see the associated tables in this chapter.	R/W
b31 to b29	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: P011PFS to P013PFS, P509PFS, P510PFS, P902PFS to P904PFS, and PA02PFS to PA07PFS for 32-bit, 16-bit, and 8-bit access are not available.
Note 1. Supported for PORT1 to PORT4.
Note 2. The initial value of P000 to P007, P108, P109, P110, P201 and P300 is not 0000_0000h.
P000 to P007 is 0000_8000h, P108 is 0001_0410h, P109 is 0001_0400h, P110 is 0001_0010h, P201 is 0000_0010h, and P300 is 0001_0010h.

The Port mn Pin Function Select Register (PmnPFS/PmnPFS_HA/PmnPFS_BY) is a 32-bit, 16-bit, and 8-bit read/write control register that selects the port mn pin function, and is accessed in 32-bit units. PmnPFS_HA (bits [15:0] in PmnPFS) is accessed in 16-bit units. PmnPFS_BY (bits [7:0]) is accessed in 8-bit units.

The PDR/PIDR/PODR bits serve the same function as the PCNTR. When these bits are read, the PCNTR value is read.

The PCR bit enables or disables an input pull-up resistor on the individual port pins. When a pin is in the input state with the associated bit in PmnPFS.PCR set to 1, the pull-up resistor connected to the pin is enabled. When a pin is set as an external bus pin, a general port output pin, or a peripheral function output pin, the pull-up resistor for the pin is disabled regardless of the PCR setting. The pull-up resistor is also disabled in the reset state. Bits associated with non-existent pins are reserved. The write value should be 0.

The NCODR bit specifies the output type for the port pins. Bits associated with non-existent pins are reserved. Reserved bits are read as 0. The write value should be 0.

The DSCR bit switches the drive capacity of the port. If the drive capacity of a pin is fixed, the associated bit is read/write, but the drive capacity cannot be changed. Bits associated with non-existent pins are reserved. The write value should be 0.

The EOR and EOF bits select the edge detection method for the port group input signal. These bits support rising, falling, or both edge detections. When the EOR and EOF bits are set to 01b, 10b, or 11b, the input enable of the I/O cell is asserted. Following that, the event pulse is input from the external pin, and the GPIO outputs the event pulse to the ELC. Bits associated with non-existent pins are reserved. The write value should be 0.

The ISEL bit specifies IRQ input pins. This setting can be used in combination with the peripheral functions, although an IRQn (external pin interrupt) of the same number must only be enabled for one pin.

The ASEL bit specifies analog pins. When a pin is set to analog pin by this bit:

1. Specify it as a general I/O port with the Port Mode Control bit (PmnPFS.PMR).
2. Disable the pull-up resistor with the Pull-up Control bit (PmnPFS.PCR).
3. Specify the input in the Port Direction bit (PmnPFS.PDR). The pin state cannot be read at this point. The PmnPFS register is protected by the Write-Protect Register (PWPR). Release write-protect before modifying the register.

The ISEL bit for an unspecified IRQn is reserved. The ASEL bit for an unspecified analog I/O pin is reserved.

The PMR bit specifies the port pin function. Bits associated with non-existent pins are reserved. The write value should be 0.

The PSEL[4:0] bits assign the peripheral function.

For details on the peripheral settings for each product, see section 20.6, Peripheral Select Settings for each Product.

Bit	Symbol	位名称	Description	R/W
b23 to b17	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b28 to b24	PSEL[4:0]	外设选择	这些位选择外设功能。对于各个引脚功能，请参见本章中的相关表格。	R/W
b31 to b29	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note: P011PFS到P013PFS、P509PFS、P510PFS、P902PFS到P904PFS和PA02PFS到PA07PFS用于32位、16位和8位访问不可用。

Note 1. 支持PORT1到PORT4。
Note 2. P000到P007、P108、P109、P110、P201和P300的初始值不是0000_0000h。
P000至P007为0000_8000h，P108为0001_0410h，P109为0001_0400h，P110为0001_0010h，P201为0000_0010h，以及P300 is 0001_0010h.

端口mn引脚功能选择寄存器(PmnPFSPmnPFS_HAPmnPFS_BY)是一个32位、16位和8位读写控制寄存器，用于选择端口mn引脚功能，并以32位为单位进行访问。PmnPFS_HA（PmnPFS中的位[15:0]）以16位为单位进行访问。PmnPFS_BY（位[7:0]）以8位为单位进行访问。

PDRPIDRPODR位的功能与PCNTR相同。读取这些位时，将读取PCNTR值。

PCR位启用或禁用各个端口引脚上的输入上拉电阻。当引脚处于输入状态且PmnPFS.PCR中的相关位设置为1时，连接到该引脚的上拉电阻被启用。当引脚设置为外部总线引脚、通用端口输出引脚或外围功能输出引脚时，无论PCR设置如何，该引脚的上拉电阻都被禁用。上拉电阻在复位状态下也被禁用。与不存在的引脚相关的位被保留。写入值应为0。

NCODR位指定端口引脚的输出类型。与不存在的引脚相关的位被保留。保留位读取为0。写入值应为0。

DSCR位切换端口的驱动能力。如果某个管脚的驱动能力是固定的，则对应的位是读写，但驱动能力不能改变。与不存在的引脚相关的位被保留。写入值应为0。

EOR和EOF位选择端口组输入信号的边沿检测方法。这些位支持上升沿、下降沿或两个边沿检测。当EOR和EOF位设置为01b、10b或11b时，IO单元的输入使能有效。随后，事件脉冲从外部引脚输入，GPIO将事件脉冲输出到ELC。与不存在的引脚相关的位被保留。写入值应为0。

ISEL位指定IRQ输入引脚。此设置可以与外围功能结合使用，尽管
相同编号的IRQn（外部引脚中断）只能为一个引脚启用。

ASEL位指定模拟引脚。当通过该位将引脚设置为模拟引脚时：

1. 通过端口模式控制位(PmnPFS.PMR)将其指定为通用IO端口。
2. 使用上拉控制位(PmnPFS.PCR)禁用上拉电阻。
3. 在端口方向位(PmnPFS.PDR)中指定输入。此时无法读取引脚状态。PmnPFS寄存器受写保护寄存器(PWPR)保护。在修改寄存器之前释放写保护。

未指定的IRQn的ISEL位被保留。未指定的模拟IO引脚的ASEL位被保留。

PMR位指定端口引脚功能。与不存在的引脚相关的位被保留。写入值应为0。

PSEL[4:0]位分配外设功能。

有关每个产品的外设设置的详细信息，请参阅第20.6节，每个产品的外设选择设置。

20.2.6 Write-Protect Register (PWPR)

Address(es): PMISC.PWPR 4004 0D03h

	b7	b6	b5	b4	b3	b2	b1	b0
	B0WI	PFSWE	—	—	—	—	—	—
Value after reset:	1	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b5 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6	PFSWE	PmnPFS Register Write Enable	0: Writing to the PmnPFS register is disabled 1: Writing to the PmnPFS register is enabled.	R/W
b7	B0WI	PFSWE Bit Write Disable	0: Writing to the PFSWE bit is enabled 1: Writing to the PFSWE bit is disabled.	R/W

PFSWE bit (PmnPFS Register Write Enable)

Writing to the PmnPFS register is enabled only when the PFSWE bit is set to 1. You must first write 0 to the B0WI bit before setting PFSWE to 1.

B0WI bit (PFSWE Bit Write Disable)

Writing to the PFSWE bit is enabled only when the B0WI bit is set to 0.

20.2.7 Ethernet Control Register (PFENET)

Address(es): PMISC.PFENET 4004 0D00h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	PHYMODE0	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	PHYMODE0	Ethernet Mode Setting ch0	0: RMII mode (ETHERC channel 0) 1: MII mode (ETHERC channel 0).	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

PHYMODE0 bit (Ethernet Mode Setting ch0)

The PHYMODE0 bit specifies the PHY mode of ETHERC channel 0. Select the same mode as that specified in the pin function select bits (PmnPFS.PSEL[4:0]). When the signals for the RMII mode are specified in the PmnPFS.PSEL[4:0] bits, set the PHYMODE bit to 0 (RMII mode). When the signals for the MII mode are specified in the PmnPFS.PSEL[4:0] bits, set the PHYMODE bit to 1 (MII mode).

20.3 Operation

20.3.1 General I/O Ports

All pins except P000 to P007, P108 to P110, and P300 operate as general I/O ports after reset. General I/O ports are organized as 16 bits per port and can be accessed by port with the Port Control Registers (PCNTRn, where n = 1 to 4), or by individual pin with the Pin Function Select Registers. For details on these registers, see section 20, Register Descriptions.

20.2.6 Write-Protect Register (PWPR)

Address(es): PMISC.PWPR 4004 0D03h

	b7	b6	b5	b4	b3	b2	b1	b0
	B0WI	PFSWE	—	—	—	—	—	—
重置后的值：	1	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b5 to b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b6	PFSWE	PmnPFS寄存器写入Enable	0：禁止写入PmnPFS寄存器1：允许写入PmnPFS寄存器。	R/W
b7	B0WI	PFSWE位写入禁用	0：允许写入PFSWE位1：禁止写入PFSWE位。	R/W

PFSWE位（PmnPFS寄存器写使能）

仅当PFSWE位设置为1时才允许写入PmnPFS寄存器。您必须先将0写入B0WI位，然后再将PFSWE设置为1。

B0WI位（PFSWE位写入禁用）

仅当B0WI位设置为0时才允许写入PFSWE位。

20.2.7 以太网控制寄存器(PFENET)

Address(es): PMISC.PFENET 4004 0D00h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	PHYMODE0	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b3 to b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b4	PHYMODE0	以太网模式设置ch0	0：RMII模式（ETHERC通道0）1：MII模式（ETHERC通道0）。	R/W
b7 to b5	—	Reserved	这些位被读取为0。写入值应为0。	R/W

PHYMODE0位（以太网模式设置ch0）

PHYMODE0位指定ETHERC通道0的PHY模式。选择与引脚功能选择位(PmnPFS.PSEL[4:0])中指定的模式相同的模式。当在PmnPFS.PSEL[4:0]位中指定RMII模式的信号时，将PHYMODE位设置为0（RMII模式）。当在PmnPFS.PSEL[4:0]位中指定MII模式的信号时，将PHYMODE位设置为1（MII模式）。

20.3 Operation

20.3.1 通用IO端口

除P000到P007、P108到P110和P300之外的所有引脚在复位后都作为通用IO端口工作。通用IO端口组织为每个端口16位，可以通过端口控制寄存器（PCNTRn，其中n=1到4）通过端口访问，或通过引脚功能选择寄存器通过单个引脚访问。有关这些寄存器的详细信息，请参见第20节，寄存器说明。

Each port has the following bits:

- Port Direction bit (PDRn), which selects input or output direction
- Port Output Data bit (PODRn), which holds data for output
- Port Input Data bit (PIDRn), which indicates the pin state
- Event Input Data bit (EIDRn), which indicates the pin state when an ELC_PORT1, 2, 3, or 4 signal occurs
- Port Output Set bit (POSRn), which indicates the output value when a software write occurs
- Port Output Reset bit (PORRn), which indicates the output value when a software write occurs
- Event Output Set bit (EOSRn), which indicates the output value when an ELC_PORT1, 2, 3 or 4 signal occurs
- Event Output Reset bit (EORRn), which indicates the output value when an ELC_PORT1, 2, 3 or 4 signal occurs.

20.3.2 Port Function Select

The following port functions are available for configuring each pin:

- I/O configuration: Complementary or open-drain output, pull-up control, and drive strength
- General I/O port: Port direction, output data setting, and reading input data
- Alternate function: Configured function mapping to the pin.

Each pin is associated with a Pin Function Select register (PmnPFS), which includes the associated PODR, PIDR, and PDR bits. In addition, the PmnPFS register includes:

- PCR: Pull-up resistor control bit that turns the input pull-up MOS on or off
- NCODR: N-channel open-drain control bit that selects the output type for each pin
- DSCR: Drive capacity control bit that selects the drive capacity
- EOR: Event on rising bit used to detect rising edges on the port input
- EOF: Event on falling bit used to detect falling edges on the port input
- ISEL: IRQ input enable bit to specify an IRQ input pin
- ASEL: Analog input enable bit to specify an analog pin
- PMR: Port mode bit to specify the pin function of each port
- PSEL[4:0]: Port function select bits to select the associated peripheral function.

These configurations can be made by a single-register access to the Pin Function Select Register. For details, see section 20, Port mn Pin Function Select Register (PmnPFS/PmnPFS_HA/PmnPFS_BY) (m = 0 to 9, A, B; n = 00 to 15).

20.3.3 Port Group Function for the ELC

In the MCU, PORT1 to PORT4 are assigned for the port group function.

20.3.3.1 Behavior when ELC_PORT1, 2, 3, or 4 is input from the ELC

The MCU supports the two functions described in this section when an ELC_PORT1, 2, 3, or 4 signal comes from the ELC.

(1) Input to EIDR

For the GPI function (PDR = 0 and PMR = 0 in the PmnPFS register), when an ELC_PORT1, 2, 3, or 4 signal comes from the ELC, the input enable of the I/O cell is asserted, and data from the external pins are read into the EIDR bit.

For the GPO function (PDR = 1) or the peripheral mode (PMR = 1), 0 is input to the EIDR bit from the external pins.

每个端口都有以下位：

- 端口方向位(PDRn)，用于选择输入或输出方向
- 端口输出数据位(PODRn)，用于保存输出数据
- 端口输入数据位(PIDRn)，指示引脚状态
- 事件输入数据位(EIDRn)，指示发生ELC_PORT1、2、3或4信号时的引脚状态
- 端口输出设置位(POSRn)，表示发生软件写入时的输出值
- 端口输出复位位(PORRn)，指示发生软件写入时的输出值
- 事件输出设置位(EOSRn)，指示ELC_PORT1、2、3或4信号发生时的输出值
- 事件输出复位位(EORRn)，指示发生ELC_PORT1、2、3或4信号时的输出值。

20.3.2 端口功能选择

以下端口功能可用于配置每个引脚：

- IO配置：互补或开漏输出、上拉控制和驱动强度
- 通用IO口：端口方向、输出数据设置、读取输入数据
- 备用功能：配置的功能映射到引脚。

每个引脚都与一个引脚功能选择寄存器(PmnPFS)相关联，其中包括相关的PODR、PIDR和PDR位。此外，PmnPFS寄存器包括：

- PCR：上拉电阻控制位，用于打开或关闭输入上拉MOS
- NCODR：为每个引脚选择输出类型的N通道开漏控制位
- DSCR：选择驱动器容量的驱动器容量控制位
- EOR：上升位事件，用于检测端口输入的上升沿
- EOF：下降位事件，用于检测端口输入的下降沿
- ISEL：IRQ输入使能位，用于指定IRQ输入引脚
- ASEL：模拟输入使能位，用于指定模拟引脚
- PMR：端口模式位，指定每个端口的引脚功能
- PSEL[4:0]：端口功能选择位，用于选择相关的外设功能。

这些配置可以通过单个寄存器访问引脚功能选择寄存器来进行。有关详细信息，请参见第20节，端口mn引脚功能选择寄存器(PmnPFSPmnPFS_HAPmnPFS_BY)(m=0到9 A B;n=00到15)。

20.3.3 ELC的端口组功能

在MCU中，为端口组功能分配了PORT1到PORT4。

20.3.3.1 从ELC输入ELC_PORT1、2、3或4时的行为

当ELC_PORT1、2、3或4信号来自
ELC.

(1) 输入到EIDR

对于GPI功能（PmnPFS寄存器中的PDR=0和PMR=0），当ELC_PORT1、2、3或4信号来自ELC时，IO单元的输入使能有效，并且来自外部引脚的数据被读入EIDR位。

对于GPO功能(PDR=1)或外设模式(PMR=1)，0从外部引脚输入到EIDR位。

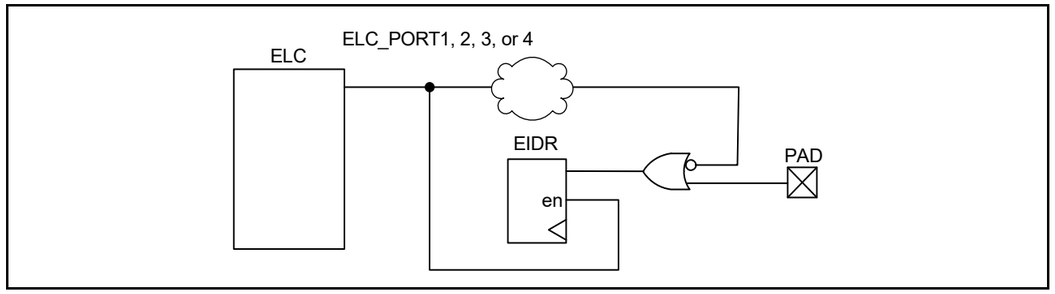


Figure 20.2 Event ports input data

(2) Output from PODR by EOSR/EORR

When an ELC_PORT1, 2, 3, or 4 signal occurs, the data is output from the PODR to the external pin based on the EOSR/EORR bit settings as follows:

- If EOSR is set to 1, when an ELC_PORT1, 2, 3, or 4 signal occurs, the PODR register outputs 1 to the external pin. Otherwise, when EOSR = 0, the PODR value is kept.
- If EORR is set to 1, when an ELC_PORT1, 2, 3, or 4 signal occurs, the PODR register outputs 0 to the external pin. Otherwise, when EORR = 0, the PODR value is kept.

See Figure 20.3.

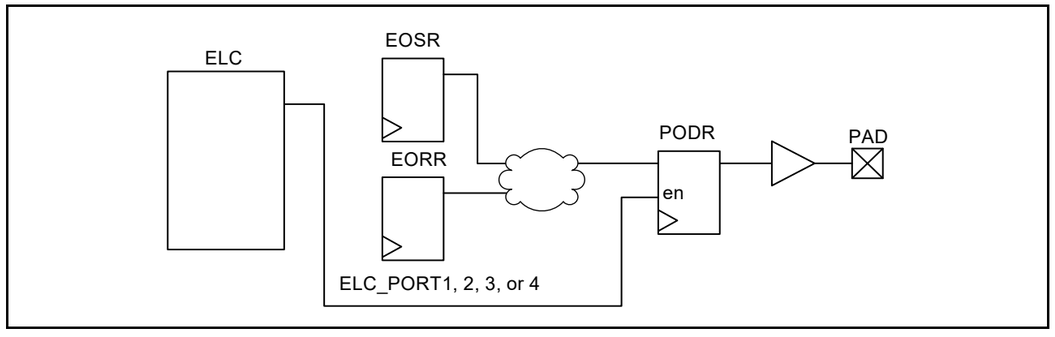


Figure 20.3 Event ports output data

20.3.3.2 Behavior when an event pulse is output to the ELC

To output the event pulse from the external pins to the ELC, set the EOR/EOF bits in the PmnPFS register. For details, see section 20.2.5, Port mn Pin Function Select Register (PmnPFS/PmnPFS_HA/PmnPFS_BY) (m = 0 to 9, A, B; n = 00 to 15). When the EOR/EOF bits are set, the input enable of the I/O cell is asserted.

Data from the external pin is the input. For example, for PORT1, when the data is input from P100 to P115, the data of those 16 pins is organized by OR logic. This data is formed into a one-shot pulse that goes to the ELC. The operation of PORT2 to PORT4 is the same.

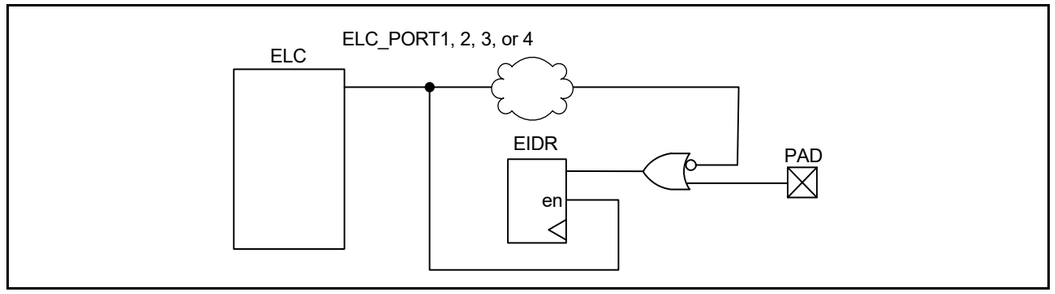


Figure 20.2 事件端口输入数据

(2) EOSREORR从PODR输出

当ELC_PORT1、2、3或4信号发生时，数据从PODR输出到基于外部引脚的EOSREORR位设置如下：

- 如果EOSR设置为1，当ELC_PORT1、2、3或4信号发生时，PODR寄存器输出1到外部引脚。否则，当EOSR=0时，保持PODR值。
- 如果EORR设置为1，则当ELC_PORT1、2、3或4信号发生时，PODR寄存器向外部引脚输出0。否则，当EORR=0时，保持PODR值。

请参见图20.3。

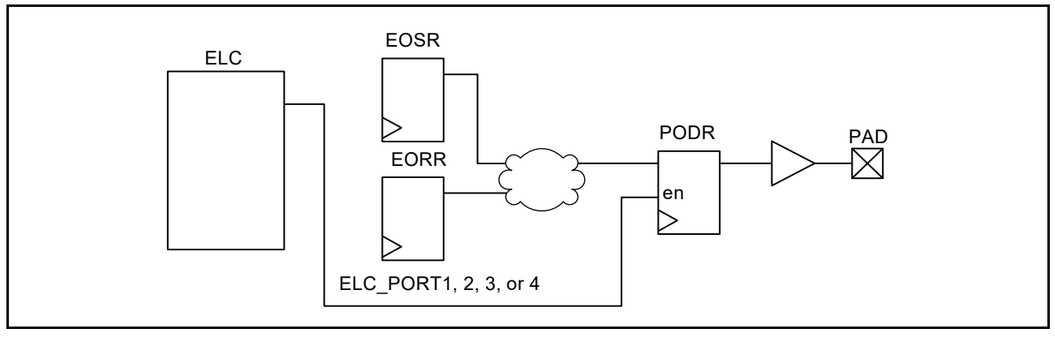


Figure 20.3 事件端口输出数据

20.3.3.2 事件脉冲输出到ELC时的行为

要将事件脉冲从外部引脚输出到ELC，请设置PmnPFS寄存器中的EOREOF位。有关详细信息，请参见第20.2.5节，端口mn引脚功能选择寄存器(PmnPFSPmnPFS_HAPmnPFS_BY)(m=0至9 A B;n=00至15)。当EOREOF位被置位时，IO单元的输入使能被断言。

来自外部引脚的数据是输入。例如，对于PORT1，当数据从P100输入到P115时，这16个引脚的数据由OR逻辑组织。该数据形成一个单次脉冲，该脉冲进入ELC。PORT2到PORT4的操作是一样的。

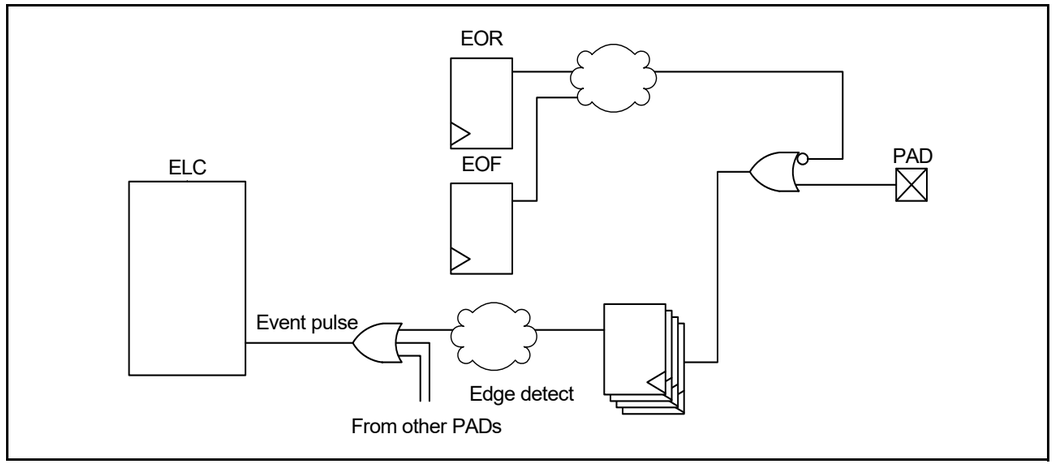


Figure 20.4 Generation of event pulse

20.4 Handling of Unused Pins

Table 20.3 shows how to handle unused pins.

Table 20.3 Handling of unused pins

Pin name	Handling when unused
MD	Use as a mode pin
RES	Connect to VCC through a resistor (pulling up)
USB_DP	Keep pin open
USB_DM	Keep pin open
P200/NMI	Connect to VCC through a resistor (pulling up)
EXTAL	When the main clock oscillator is not used, set the MOSCCR.MOSTP bit to 1 (general port P212). When this pin is not used as port P212, configure it in the same way as ports 1 to 9.
XTAL	When the main clock oscillator is not used, set the MOSCCR.MOSTP bit to 1 (general port P213). When the external clock is input to the EXTAL pin, the XTAL pin functions as P213. When this pin is not used as port P213, configure it in the same way as ports 1 to 9.
XCIN	Connect to VSS through a resistor (pulling down)
XCOUT	Keep pin open
P000 to P007	Connect to AVCC0 (pulled up) through a resistor or to AVSS0 (pulled down) through a resistor*1, *4
P008 to P010 P014 to P015	• If the direction is set to input (PCNTR1.PDRn = 0), connect the associated pin to AVCC0 (pulled up) through a resistor or to AVSS0 (pulled down) through a resistor*1 • If the direction is set to output (PCNTR1.PDRn = 1), release the pin*1
P1x to P9x PAx to PBx	• If the direction is set to input (PCNTR1.PDRn = 0), connect the associated pin to VCC (pulled up) through a resistor or to VSS (pulled down) through a resistor*1, *2 • If the direction is set to output (PCNTR1.PDRn = 1), release the pin*1, *3
VREFH0, VREFH	Connect to AVCC0
VREFL0, VREFL	Connect to AVSS0
USBHS_DP USBHS_DM USBHS_RREF	• Preconditions: AVCC_USBHS = VCC_USBHS: Connect to VCC AVSS_USBHS = PVSS_USBHS = VSS1_USBHS = VSS2_USBHS: Connect to VSS Set the module-stop state for USBHS (MSTPCRB.MSTPB12 = 1) • Processing details: USBHS_DP, USBHS_DM, and USBHS_RREF: Open.
VBATT	Connect to VCC or VSS.

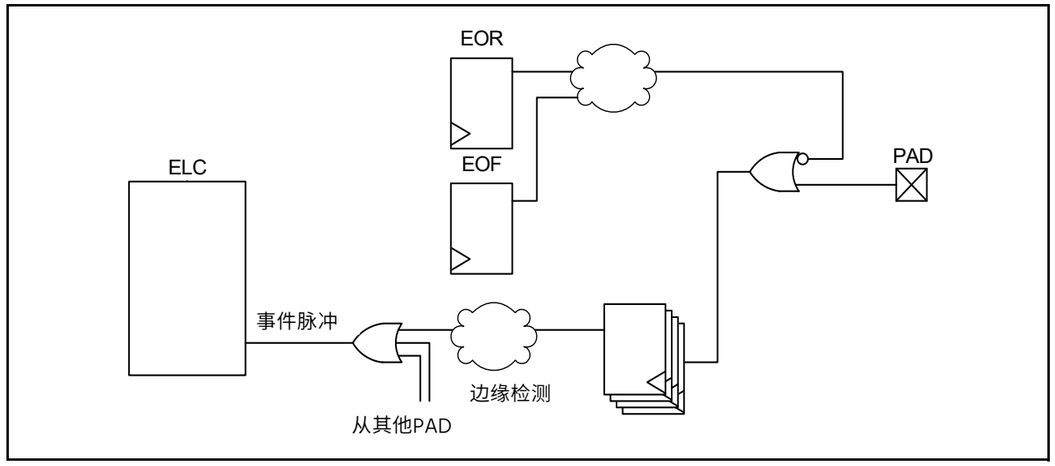


Figure 20.4 事件脉冲的产生

20.4 未使用引脚的处理

表20.3显示了如何处理未使用的引脚。

Table 20.3 处理未使用的引脚

引脚名称	未使用时的处理
MD	用作模式引脚
RES	通过一个电阻连接到VCC（上拉）
USB_DP	保持引脚打开
USB_DM	保持引脚打开
P200/NMI	通过一个电阻连接到VCC（上拉）
EXTAL	不使用主时钟振荡器时，将MOSCCR.MOSTP位设置为1（通用端口P212）。 当该管脚不作为端口P212使用时，配置方式与端口1到9相同。
XTAL	不使用主时钟振荡器时，将MOSCCR.MOSTP位设置为1（通用端口P213）。 当外部时钟输入到EXTAL引脚时，XTAL引脚起到P213的作用。当该管脚不作为端口P213使用时，配置方式与端口1到9相同。
XCIN	通过一个电阻连接到VSS（下拉）
XCOUT	保持引脚打开
P000 to P007	通过电阻连接到AVCC0（上拉）或通过电阻连接到AVSS0（下拉）*1、*4
P008 to P010 P014 to P015	如果方向设置为输入(PCNTR1.PDRn=0)，请将相关引脚通过电阻连接到AVCC0（上拉）或通过电阻连接到AVSS0（下拉）*1 如果方向设置为输出（PCNTR1.PDRn=1），释放引脚*1
P1x到P9xP Ax到PBx	如果方向设置为输入(PCNTR1.PDRn=0)，则将相关引脚通过电阻连接到VCC（上拉）或通过电阻连接到VSS（下拉）*1、*2 如果设置了方向输出（PCNTR1.PDRn=1），释放引脚*1，*3
VREFH0, VREFH	连接到AVCC0
VREFL0, VREFL	连接到AVSS0
USBHS_DP USBHS_DM USBHS_RREF	前提条件：AVCC_USBHS=VCC_USBHS：连接到VCC AVSS_USBHS=PVSS_USBHS=VSS1_USBHS=VSS2_USBHS：连接到VSS 设置USBHS的模块停止状态(MSTPCRB.MSTPB12=1) 处理细节：USBHS_DP、USBHS_DM和USBHS_RREF：打开。
VBATT	连接到VCC或VSS。

Note 1. Clear the PmnPFS.PMR, PmnPFS.ISEL, PmnPFS.PCR, and PmnPFS.ASEL bits to 0.
Note 2. P108, P110, P300 are recommended for pull up VCC (pulled up) through a resistor, because these pins are input pull-up enabled from the initial value (PmnPFS.PCR=1).
Note 3. P109 is recommended to be set as an output (PCNTR1.PDRn = 1) because this pin is output from the initial value.
Note 4. To reduce input leakage current of P003 and P007, set the P003PFS.ASEL and P007PFS.ASEL bits to 0.

20.5 Usage Notes

20.5.1 Procedure for Specifying the Pin Functions

To specify the I/O pin functions:

1. Clear the B0WI bit in the PWPR register. This enables writing to the PFSWE bit in the PWPR register.
2. Set 1 to the PFSWE bit in the PWPR register. This enables writing to the PmnPFS register.
3. Clear the port mode control in the PMR for the target pin to select the general I/O port.
4. Specify the I/O function for the pin through the PSEL[4:0] bit settings in the PmnPFS register.
5. Set the PMR bit to 1 as required to switch to the selected I/O function for the pin.
6. Clear the PFSWE bit in the PWPR register. This disables writing to the PmnPFS register.
7. Set 1 to the B0WI bit in the PWPR register. This disables writing to the PFSWE bit in the PWPR register.

20.5.2 Procedure for Using Port Group Input

To use the port group input (PORT1 to PORT4):

1. Set the ELSRx.ELS[8:0] bits to 0000 0000b to ignore unexpected pulses. For more information, see section 19, Event Link Controller (ELC).
2. Set the EOF/EOR bit of the PmnPFS register to specify the rising, falling, or both edge detections.
3. Execute a dummy read or wait for a short time, for example 100 ns. Ignoring of unexpected pulses depends on the initial value of the external pin.
4. Set the ELSRx.ELS[8:0] bits to enable the event signals.

20.5.3 Port Output Data Register (PODR) Summary

This register outputs data as follows:

1. Output 0 if PCNTR4.EORR is set to 1 when an ELC_PORT1, 2, 3, or 4 signal occurs.
2. Output 1 if PCNTR4.EOSR is set to 1 when an ELC_PORT1, 2, 3, or 4 signal occurs.
3. Output 0 if PCNTR3.PORR is set to 1.
4. Output 1 if PCNTR3.POSR is set to 1.
5. Output 0 or 1 because PCNTR1.PODR is set.
6. Output 0 or 1 because PmnPFS.PODR is set.

Numbers in this list correspond to the priority for writing to the PODR. For example, if 1. and 3. from the list occur at the same time, the higher priority event 1. is executed.

20.5.4 Notes on Using Analog Functions

To use an analog function, set the Port Mode Control bit (PMR) and Port Direction bit (PDR) to 0 so that the pin acts as a general input port. Next, set the Analog Input Enable bit (ASEL) in the Port mn Pin Function Select register (PmnPFS.ASEL) to 1.

20.5.5 I/O Buffer Specification

The P402, P403, and P404 can be used as the RTC input, AGT input, and other peripheral functions.

Table 20.4 lists the P402, P403, P404 specifications.

Note 1. 将PmnPFS.PMR、PmnPFS.ISEL、PmnPFS.PCR和PmnPFS.ASEL位清除为0。
Note 2. 推荐P108、P110、P300通过电阻上拉VCC（上拉），因为这些引脚从初始值（PmnPFS.PCR=1）开始输入上拉使能。

Note 3. 建议将P109设置为输出（PCNTR1.PDRn=1），因为该引脚是从初始值输出的。
Note 4. 要降低P003和P007的输入漏电流，请将P003PFS.ASEL和P007PFS.ASEL位设置为0。

20.5 使用说明

20.5.1 指定引脚功能的步骤

要指定IO引脚功能：

1. 将PWPR寄存器中的B0WI位清零。这允许写入PWPR寄存器中的PFSWE位。
2. 将PWPR寄存器中的PFSWE位设置为1。这允许写入PmnPFS寄存器。
3. 清除PMR中针对目标引脚的端口模式控制以选择通用IO端口。
4. 通过PmnPFS寄存器中的PSEL[4:0]位设置指定引脚的IO功能。
5. 根据需要将PMR位设置为1，以切换到为引脚选择的IO功能。
6. 将PWPR寄存器中的PFSWE位清零。这将禁止写入PmnPFS寄存器。
7. 将PWPR寄存器中的B0WI位设置为1。这将禁止写入PWPR寄存器中的PFSWE位。

20.5.2 使用端口组输入的过程

要使用端口组输入（PORT1到PORT4）：

1. 将ELSRx.ELS[8:0]位设置为00000000b以忽略意外脉冲。有关详细信息，请参阅第19节，事件链接控制器（ELC）。
2. 设置PmnPFS寄存器的EOFEOR位以指定上升沿、下降沿或两个边沿检测。
3. 执行虚拟读取或等待一小段时间，例如100ns。忽略意外脉冲取决于外部引脚的初始值。
4. 设置ELSRx.ELS[8:0]位以启用事件信号。

20.5.3 端口输出数据寄存器(PODR)摘要

该寄存器输出数据如下：

1. 如果在ELC_PORT1、2、3或4信号发生时PCNTR4.EORR设置为1，则输出0。
2. 如果出现ELC_PORT1、2、3或4信号时PCNTR4.EOSR设置为1，则输出1。
3. 如果PCNTR3.PORR设置为1，则输出0。
4. 如果PCNTR3.POSR设置为1，则输出1。
5. 输出0或1，因为PCNTR1.PODR已设置。
6. 输出0或1，因为PmnPFS.PODR已设置。

此列表中的数字对应于写入PODR的优先级。例如，如果列表中的1.和3.同时发生，则执行优先级较高的事件1.。

20.5.4 使用模拟功能的注意事项

要使用模拟功能，请将端口模式控制位(PMR)和端口方向位(PDR)设置为0，以便引脚用作通用输入端口。接下来，将端口mn引脚功能选择寄存器(PmnPFS.ASEL)中的模拟输入使能位(ASEL)设置为1。

20.5.5 IO缓冲器规格

P402、P403和P404可用作RTC输入、AGT输入和其他外围功能。

表20.4列出了P402、P403、P404规格。

Table 20.4 P402, P403, P404 specifications

I/O port	Functions: RTC and AGT			Functions: Other peripheral	
	RTC and AGT input enable register	RTC	AGT	Other peripheral enable register	CAC, GPT, CAN, SCI, SSIE, ETHERC (MII), ETHERC (RMII), SDHI, Interrupt, and PDC
P402	VBTICTLR .VCH0INEN	RTCIC0	AGTIO0 AGTIO1	P402PFS.PSEL and PMR	For details, see Table 20.13 Register settings for I/O pin functions on PORT4
P403	VBTICTLR .VCH1INEN	RTCIC1	AGTIO0 AGTIO1	P403PFS.PSEL and PMR	
P404	VBTICTLR .VCH2INEN	RTCIC2	—	P404PFS.PSEL and PMR	

These RTC and AGT inputs are controlled by the VBTICTLR register, which has the highest priority for selecting the RTC and AGT input functions. See Figure 20.5.

The VBTICTLR register is not initialized on reset. Therefore, when not using the RTC or AGT inputs, the associated bit of the VBTICTLR register must be set to 0 after reset.

For more information on the VBTICTLR register, see section 12.2.2, VBATT Input Control Register (VBTICTLR).

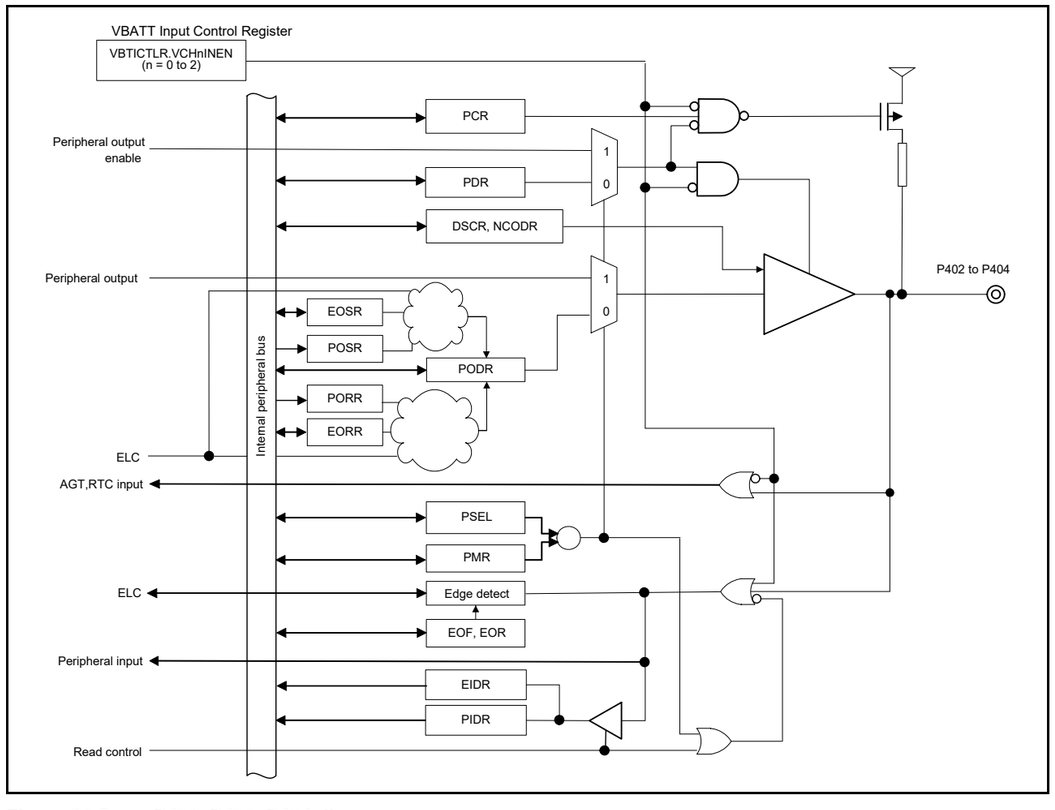


Figure 20.5 P402, P403, P404 diagram

Table 20.4 P402, P403, P404 specifications

I/O port	Functions: RTC and AGT			Functions: 其他周边	
	RTC和AGT输入使能寄存器	RTC	AGT	其他外设使能寄存器	CAC、GPT、CAN、SCI、SSIE、ETHERC(MII)、ETHERC(RMII)、SDHI、中断和PDC
P402	VBTICTLR .VCH0INEN	RTCIC0	AGTIO0 AGTIO1	P402PFS.PSEL and PMR	详见表20.13 PORT4上IO引脚功能的寄存器设置
P403	VBTICTLR .VCH1INEN	RTCIC1	AGTIO0 AGTIO1	P403PFS.PSEL and PMR	
P404	VBTICTLR .VCH2INEN	RTCIC2	—	P404PFS.PSEL and PMR	

这些RTC和AGT输入由VBTICTLR寄存器控制，该寄存器具有最高优先级来选择RTC和AGT输入功能。请参见图20.5。

VBTICTLR寄存器在复位时未初始化。因此，当不使用RTC或AGT输入时，VBTICTLR寄存器的相关位必须在复位后设置为0。

有关VBTICTLR寄存器的更多信息，请参见第12.2.2节，VBATT输入控制寄存器(VBTICTLR)。

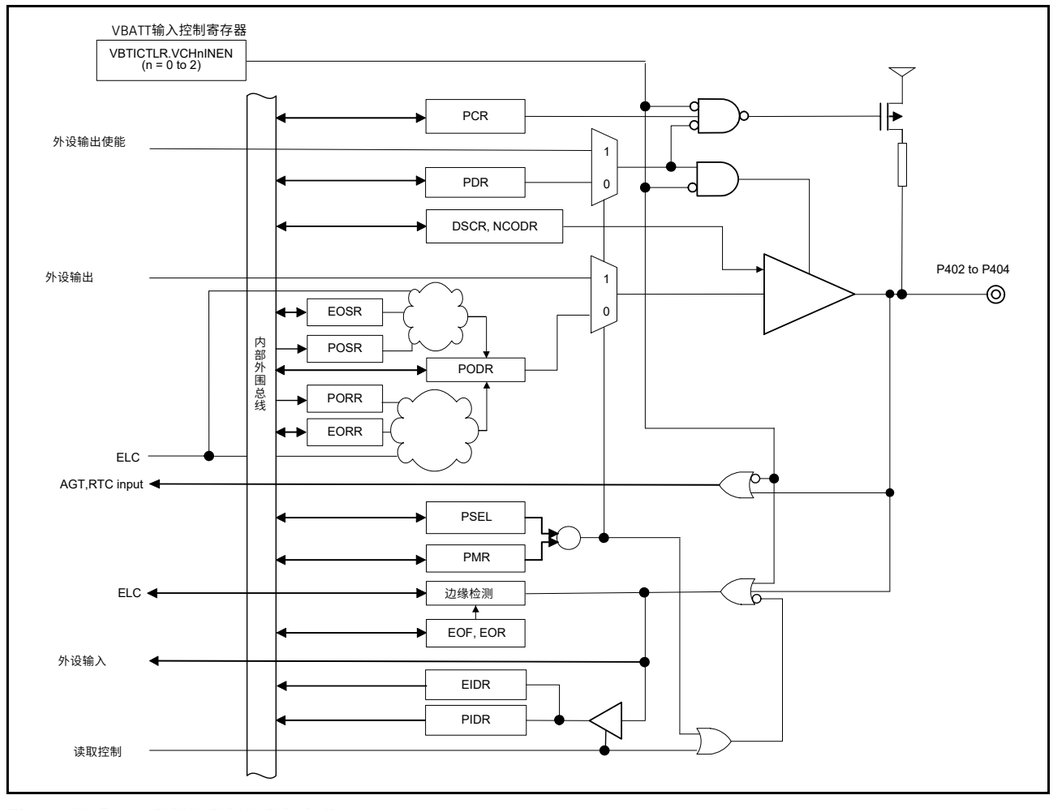


Figure 20.5 P402, P403, P404 diagram

20.6 Peripheral Select Settings for each Product

This section describes the pin function select configuration by the PmnPFS register. Some pin names have added _A, _B, and _C suffixes. When assigning IIC, SPI, SSIE, ETHERC, and SDHI functionality, select the functional pins having the same suffix. The other pins can be selected regardless of the suffix. Assigning the same function to two or more pins simultaneously is prohibited.

20.7 Notes on the PmnPFS Register Setting

(1) In the Port mn Pin Function Select register (PmnPFS), the PSEL bits must be set when the PMR bit of the target pin is 0. If the PSEL bits are set when the PMR bit is 1, unexpected edges might be input for the input function or unexpected pulses might be output to the external pin for the output function.

(2) Only the allowed values (functions) should be specified in the PSEL bits of PmnPFS. If a value that is not allowed for the register is specified, the correct operation is not guaranteed.

(3) A single function should not be assigned to multiple pins by the PmnPFS register.

(4) PORT0 and PORT5 have the analog functions such as A/D converter and D/A converter. When these pins are used as an analog function, to avoid loss of resolution, the PMR and PDR bits should be set to 0. After that, the ASEL bit should be set to 1.

(5) The initial value of the ASEL bit of P003 and P007 is 1. When these pins are not used as an analog function, to reduce the input leakage current, the ASEL bit should be set to 0.

Table 20.5 Register settings for I/O pin functions (PORT0)

PSEL[4:0] settings	Function	Pin							
		P000	P001	P002	P003	P004	P005	P006	P007
ASEL bit		AN000/ IVCMP2	AN001/ IVCMP2	AN002/ IVCMP2	PGAVSS000/ AN007	AN100/ IVCMP2	AN101/ IVCMP2	AN102/ IVCMP2	PGAVSS100/ AN107
ISEL bit		IRQ6-DS	IRQ7-DS	IRQ8-DS		IRQ9-DS	IRQ10-DS	IRQ11-DS	
DSCR[1:0] bits	Drive capacity control	-	-	-	-	-	-	-	-
NCODR bit	N-ch open-drain	-	-	-	-	-	-	-	-
PCR bit	Pull-up								
Number of pins	176 pins	✓	✓	✓	✓	✓	✓	✓	✓
	144 pins, 145 pins	✓	✓	✓	✓	✓	✓	✓	✓
	100 pins	✓	✓	✓	✓	✓	✓	✓	✓

✓: Available

Table 20.6 Register settings for I/O pin functions (PORT0)

PSEL[4:0] settings	Function	Pin				
		P008	P009	P010	P014	P015
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z				
ASEL bit		AN003	AN004	AN103	AN005/ AN105/ DA0/ IVREF3	AN006/ AN106/ DA1/ IVCMP1
ISEL bit		IRQ12-DS	IRQ13-DS	IRQ14-DS		IRQ13
DSCR[1:0] bits	Drive capacity control	*1	*1	*1	*1	*1
NCODR bit	N-ch open-drain	✓	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓	✓
Number of pins	176 pins	✓	✓	✓	✓	✓
	144 pins, 145 pins	✓	✓	-	✓	✓
	100 pins	✓	-	-	✓	✓

✓: Available

Note 1. The drive strength of this port cannot be controlled by PmnPFS.DSCR[1:0] bits.

20.6 每个产品的外设选择设置

本节介绍PmnPFS寄存器的引脚功能选择配置。一些引脚名称添加了_A、_B和_C后缀。分配IIC、SPI、SSIE、ETHERC和SDHI功能时，选择具有相同后缀的功能管脚。无论后缀如何，都可以选择其他引脚。禁止将相同的功能同时分配给两个或多个引脚。

20.7 PmnPFS寄存器设置注意事项

(1)在端口mn引脚功能选择寄存器(PmnPFS)中，当目标引脚的PMR位为0时，必须设置PSEL位。如果在PMR位为1时设置PSEL位，可能会输入意外边沿输入功能或意外脉冲可能会输出到输出功能的外部引脚。

(2)在PmnPFS的PSEL位中只应指定允许的值（功能）。如果指定了寄存器不允许的值，则不能保证正确操作。

(3)PmnPFS寄存器不应将单个功能分配给多个引脚。

(4)PORT0和PORT5具有AD转换器和DA转换器等模拟功能。当这些引脚用作模拟功能时，为避免分辨率损失，应将PMR和PDR位设置为0。之后，应将ASEL位设置为1。

(5)P003和P007的ASEL位初始值为1。当这些引脚不用作模拟功能时，为减少输入漏电流，应将ASEL位设置为0。

Table 20.5 IO引脚功能的寄存器设置(PORT0)

PSEL[4:0] settings	Function	Pin							
		P000	P001	P002	P003	P004	P005	P006	P007
ASEL bit		AN000/ IVCMP2	AN001/ IVCMP2	AN002/ IVCMP2	PGAVSS000/ AN007	AN100/ IVCMP2	AN101/ IVCMP2	AN102/ IVCMP2	PGAVSS100/ AN107
ISEL bit		IRQ6-DS	IRQ7-DS	IRQ8-DS		IRQ9-DS	IRQ10-DS	IRQ11-DS	
DSCR[1:0] bits	驱动容量控制	-	-	-	-	-	-	-	-
NCODR bit	N-ch open-drain	-	-	-	-	-	-	-	-
PCR bit	Pull-up								
引脚数	176 pins	✓	✓	✓	✓	✓	✓	✓	✓
	144 pins, 145 pins	✓	✓	✓	✓	✓	✓	✓	✓
	100 pins	✓	✓	✓	✓	✓	✓	✓	✓

✓: Available

Table 20.6 IO引脚功能的寄存器设置(PORT0)

PSEL[4:0] settings	Function	Pin				
		P008	P009	P010	P014	P015
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z				
ASEL bit		AN003	AN004	AN103	AN005/ AN105/ DA0/ IVREF3	AN006/ AN106/ DA1/ IVCMP1
ISEL bit		IRQ12-DS	IRQ13-DS	IRQ14-DS		IRQ13
DSCR[1:0] bits	驱动容量控制	*1	*1	*1	*1	*1
NCODR bit	N-ch open-drain	✓	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓	✓
引脚数	176 pins	✓	✓	✓	✓	✓
	144 pins, 145 pins	✓	✓	-	✓	✓
	100 pins	✓	-	-	✓	✓

✓: Available

Note 1. 此端口的驱动强度不能由PmnPFS.DSCR[1:0]位控制。

Table 20.7 Register settings for I/O pin functions (PORT1)

PSEL[4:0] settings	Function	Pin							
		P100	P101	P102	P103	P104	P105	P106	P107
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z							
00001b	AGT	AGTIO0	AGTEE0	AGTO0	—	—	—	AGTOB0	AGTOA0
00010b	GPT	GTETRGA	GTETRGB	GTOWLO	GTOWUP	GTETRGB	GTETRGA	—	—
00011b	GPT*2	GTIOC5B	GTIOC5A	GTIOC2B_A	GTIOC2A_A	GTIOC1B	GTIOC1A	GTIOC8B	GTIOC8A
00100b	SCI	RXD0/MISO0/ SCL0	TXD0/MOSI0/ SDA0	SCK0	CTS0_RTS0/ SS0	RXD8/MISO8/ SCL8	TXD8/MOSI8/ SDA8	SCK8	CTS8_RTS8/ SS8
00101b	SCI	SCK1	CTS1_RTS1/ SS1	—	—	—	—	—	—
00110b	SPI*1	MISOA_A	MOSIA_A	RSPCKA_A	SSLA0_A	SSLA1_A	SSLA2_A	SSLA3_A	—
00111b	IIC*1	SCL1_B	SDA1_B	—	—	—	—	—	
01000b	KINT	KR00	KR01	KR02	KR03	KR04	KR05	KR06	KR07
01010b	CAC/ADC12	—	—	ADTRG0	—	—	—	—	—
01011b	BUS	D00[A00/D00]/ DQ00	D01[A01/D01]/ DQ01	D02[A02/D02]/ DQ02	D03[A03/D03]/ DQ03	D04[A04/D04]/ DQ04	D05[A05/D05]/ DQ05	D06[A06/D06]/ DQ06	D07[A07/D07]/ DQ07
10000b	CAN	—	—	CRX0	CTX0	—	—	—	—
11001b	GLCDC	LCD_EXTCLK _A	LCD_CLK_A	LCD_TCON0_ A	LCD_TCON1_ A	LCD_TCON2_ A	LCD_TCON3_ A	LCD_DATA00_ A	LCD_DATA01_ A
ASEL bit		-	-	-	-	-	-	-	-
ISEL bit		IRQ2	IRQ1	-	-	IRQ1	IRQ0	-	-
DSCR[1:0] bits	Drive capacity control	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H
NCODR bit	N-ch open-drain	✓	✓	✓	✓	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓	✓	✓	✓	✓
Number of pins	176 pins	✓	✓	✓	✓	✓	✓	✓	✓
	144 pins, 145 pins	✓	✓	✓	✓	✓	✓	✓	✓
	100 pins	✓	✓	✓	✓	✓	✓	✓	✓

✓: Available
—: Setting prohibited

Note 1. Renesas recommends using pins that have a letter appended to their names, for instance “_A” or “_B”, to indicate group membership. For the interface, the AC portion of the electrical characteristics is measured for each group.
Note 2. There are two types of output buffer, middle drive and high drive. Renesas recommends using the same drive buffer for output skew spec (t_{GTISK}).

Table 20.7 IO引脚功能的寄存器设置(PORT1)

PSEL[4:0] settings	Function	Pin							
		P100	P101	P102	P103	P104	P105	P106	P107
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z							
00001b	AGT	AGTIO0	AGTEE0	AGTO0	—	—	—	AGTOB0	AGTOA0
00010b	GPT	GTETRGA	GTETRGB	GTOWLO	GTOWUP	GTETRGB	GTETRGA	—	—
00011b	GPT*2	GTIOC5B	GTIOC5A	GTIOC2B_A	GTIOC2A_A	GTIOC1B	GTIOC1A	GTIOC8B	GTIOC8A
00100b	SCI	RXD0/MISO0/ SCL0	TXD0/MOSI0/ SDA0	SCK0	CTS0_RTS0/ SS0	RXD8/MISO8/ SCL8	TXD8/MOSI8/ SDA8	SCK8	CTS8_RTS8/ SS8
00101b	SCI	SCK1	CTS1_RTS1/ SS1	—	—	—	—	—	—
00110b	SPI*1	MISOA_A	MOSIA_A	RSPCKA_A	SSLA0_A	SSLA1_A	SSLA2_A	SSLA3_A	—
00111b	IIC*1	SCL1_B	SDA1_B	—	—	—	—	—	
01000b	KINT	KR00	KR01	KR02	KR03	KR04	KR05	KR06	KR07
01010b	CAC/ADC12	—	—	ADTRG0	—	—	—	—	—
01011b	BUS	D00[A00/D00]/ DQ00	D01[A01/D01]/ DQ01	D02[A02/D02]/ DQ02	D03[A03/D03]/ DQ03	D04[A04/D04]/ DQ04	D05[A05/D05]/ DQ05	D06[A06/D06]/ DQ06	D07[A07/D07]/ DQ07
10000b	CAN	—	—	CRX0	CTX0	—	—	—	—
11001b	GLCDC	LCD_EXTCLK _A	LCD_CLK_A	LCD_TCON0_ A	LCD_TCON1_ A	LCD_TCON2_ A	LCD_TCON3_ A	LCD_DATA00_ A	LCD_DATA01_ A
ASEL bit		-	-	-	-	-	-	-	-
ISEL bit		IRQ2	IRQ1	-	-	IRQ1	IRQ0	-	-
DSCR[1:0] bits	驱动容量控制	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H
NCODR bit	N-ch open-drain	✓	✓	✓	✓	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓	✓	✓	✓	✓
引脚数	176 pins	✓	✓	✓	✓	✓	✓	✓	✓
	144 pins, 145 pins	✓	✓	✓	✓	✓	✓	✓	✓
	100 pins	✓	✓	✓	✓	✓	✓	✓	✓

:可用—:禁止设置

Note 1. 瑞萨电子建议使用名称后附有字母的引脚，例如"_A"或"_B"，以表示组成员身份。对于接口，测量每组电气特性的交流部分。
Note 2. 输出缓冲器有两种类型，中驱动和高驱动。Renesas建议使用相同的驱动缓冲器来实现输出偏斜规范(tGTISK)。

Table 20.8 Register settings for I/O pin functions (PORT1)

PSEL[4:0] settings	Function	Pin							
		P108	P109	P110	P111	P112	P113	P114	P115
00000b (value after reset)	Hi-Z/JTAG/SWD	TMS/SWDIO	TDO/SWO	TDI	Hi-Z				
00010b	GPT	GTOULO	GTOVUP	GTOVLO	—	—	—	—	—
00011b	GPT*2	GTIOC0B_A	GTIOC1A_A	GTIOC1B_A	GTIOC3A_A	GTIOC3B_A	GTIOC2A	GTIOC2B	GTIOC4A
00100b	SCI	—	—	CTS2_RTS2/ SS2	SCK2	TXD2/MOSI2/ SDA2	RXD2/MISO2/ SCL2	—	—
00101b	SCI	CTS9_RTS9/ SS9	TXD9/MOSI9/ SDA9	RXD9/MISO9/ SCL9	SCK9	SCK1	—	—	—
00110b	SPI*1	SSLB0_B	MOSIB_B	MISOB_B	RSPCKB_B	SSLB0_B	—	—	—
01001b	CLKOUT/ACMPHS/RTC	—	CLKOUT	VCOUT	—	—	—	—	—
01011b	BUS	—	—	—	A05	A04	A03	A02	A01
10000b	CAN	—	CTX1	CRX1	—	—	—	—	—
10010b	SSIE*1	—	—	—	—	SSIBCK0_B	SSILRCK0/SSI FS0_B	SSIRXD0_B	SSITXD0_B
11001b	GLCDC	—	—	—	LCD_DATA12_ A	LCD_DATA11_ A	LCD_DATA10_ A	LCD_DATA09_ A	LCD_DATA08_ A
ASEL bit		-	-	-	-	-	-	-	-
ISEL bit		-	-	IRQ3	IRQ4	-	-	-	-
DSCR[1:0] bits	Drive capacity control	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H
NCODR bit	N-ch open-drain	✓	✓	✓	✓	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓	✓	✓	✓	✓
Number of pins	176 pins	✓	✓	✓	✓	✓	✓	✓	✓
	144 pins, 145 pins	✓	✓	✓	✓	✓	✓	✓	✓
	100 pins	✓	✓	✓	✓	✓	✓	✓	✓

✓: Available
—: Setting prohibited

Note 1. Renesas recommends using pins that have a letter appended to their names, for instance “_A” or “_B”, to indicate group membership. For the interface, the AC portion of the electrical characteristics is measured for each group.
Note 2. There are two types of output buffer, middle drive and high drive. Renesas recommends using the same drive buffer for output skew spec (t_{GTISK}).

Table 20.8 IO引脚功能的寄存器设置(PORT1)

PSEL[4:0] settings	Function	Pin							
		P108	P109	P110	P111	P112	P113	P114	P115
00000b (value after reset)	Hi-Z/JTAG/SWD	TMS/SWDIO	TDO/SWO	TDI	Hi-Z				
00010b	GPT	GTOULO	GTOVUP	GTOVLO	—	—	—	—	—
00011b	GPT*2	GTIOC0B_A	GTIOC1A_A	GTIOC1B_A	GTIOC3A_A	GTIOC3B_A	GTIOC2A	GTIOC2B	GTIOC4A
00100b	SCI	—	—	CTS2_RTS2/ SS2	SCK2	TXD2/MOSI2/ SDA2	RXD2/MISO2/ SCL2	—	—
00101b	SCI	CTS9_RTS9/ SS9	TXD9/MOSI9/ SDA9	RXD9/MISO9/ SCL9	SCK9	SCK1	—	—	—
00110b	SPI*1	SSLB0_B	MOSIB_B	MISOB_B	RSPCKB_B	SSLB0_B	—	—	—
01001b	CLKOUT/ACMPHS/RTC	—	CLKOUT	VCOUT	—	—	—	—	—
01011b	BUS	—	—	—	A05	A04	A03	A02	A01
10000b	CAN	—	CTX1	CRX1	—	—	—	—	—
10010b	SSIE*1	—	—	—	—	SSIBCK0_B	SSILRCK0/SSI FS0_B	SSIRXD0_B	SSITXD0_B
11001b	GLCDC	—	—	—	LCD_DATA12_ A	LCD_DATA11_ A	LCD_DATA10_ A	LCD_DATA09_ A	LCD_DATA08_ A
ASEL bit		-	-	-	-	-	-	-	-
ISEL bit		-	-	IRQ3	IRQ4	-	-	-	-
DSCR[1:0] bits	驱动容量控制	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H
NCODR bit	N-ch open-drain	✓	✓	✓	✓	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓	✓	✓	✓	✓
引脚数	176 pins	✓	✓	✓	✓	✓	✓	✓	✓
	144 pins, 145 pins	✓	✓	✓	✓	✓	✓	✓	✓
	100 pins	✓	✓	✓	✓	✓	✓	✓	✓

:可用—:禁止设置

Note 1. 瑞萨电子建议使用名称后附有字母的引脚，例如“_A”或“_B”，以表示组成员身份。对于接口，测量每组电气特性的交流部分。
Note 2. 输出缓冲器有两种类型，中驱动和高驱动。Renesas建议使用相同的驱动缓冲器来实现输出偏斜规范(tGTISK)。

Table 20.9 Register settings for I/O pin functions (PORT2)

PSEL[4:0] settings	Function	Pin							
		P200*4	P201	P202	P203	P204	P205	P206	P207
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z							
00001b	AGT	—	—	—	—	AGTIO1	AGTO1	—	—
00010b	GPT	—	—	—	—	GTIW	GTIV	GTIU	—
00011b	GPT*2	—	—	GTIOC5B	GTIOC5A	GTIOC4B	GTIOC4A	—	—
00100b	SCI	—	—	SCK2	CTS2_RTS2/ SS2	SCK4	TXD4/MOSI4/ SDA4	RXD4/MISO4/ SCL4	—
00101b	SCI	—	—	RXD9/MISO9/ SCL9	TXD9/MOSI9/ SDA9	SCK9	CTS9_RTS9/ SS9	—	—
00110b	SPI*1	—	—	MISOB_A	MOSIB_A	RSPCKB_A	SSLB0_A	SSLB1_A	SSLB2_A
00111b	IIC*1	—	—	—	—	SCL0_B	SCL1_A	SDA1_A	—
01001b	CLKOUT/ACMPHS/RTC	—	—	—	—	—	CLKOUT	—	—
01010b	CAC/ADC12	—	—	—	—	CACREF	—	—	—
01011b	BUS	—	—	WR1/BC1	A19	A18	A16	WAIT	A17
01100b	CTSU	—	—	—	TSCAP	TS00	TSCAP	TS01	TS02
10000b	CAN	—	—	CRX0	CTX0	—	—	—	—
10001b	QSPI	—	—	—	—	—	—	—	QSSL
10010b	SSIE*1	—	—	—	—	SSIBCK1_A	SSILRCK1/SSI FS1_A	SSIDATA1_A	—
10011b	USBFS	—	—	—	—	USB_OVRCU RB-DS	USB_OVRCU RA-DS	USB_VBUSEN	—
10101b	SDHI*1	—	—	SD0DAT6_A	SD0DAT5_A	SD0DAT4_A	SD0DAT3_A	SD0DAT2_A	—
10110b	ETHERC (MII)	—	—	ET0_ERXD2	ET0_COL	ET0_RX_DV	ET0_WOL	ET0_LINKSTA	—
10111b	ETHERC (RMII)	—	—	—	—	—	ET0_WOL	ET0_LINKSTA	—
11001b	GLCDC	—	—	LCD_TCON3_ B	—	—	—	—	LCD_DATA23_ B
ASEL bit		-	-	-	-	-	-	-	-
ISEL bit		-	-	IRQ3-DS	IRQ2-DS	-	IRQ1-DS	IRQ0-DS	-
DSCR[1:0] bits	Drive capacity control	-	*3	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H
NCODR bit	N-ch open-drain	-	✓	✓	✓	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓	✓	✓	✓	✓
Number of pins	176 pins	✓	✓	✓	✓	✓	✓	✓	✓
	144 pins, 145 pins	✓	✓	✓	✓	✓	✓	✓	✓
	100 pins	✓	✓	-	-	-	✓	✓	✓

✓: Available
—: Setting prohibited

Note 1. Renesas recommends using pins that have a letter appended to their names, for instance “_A” or “_B”, to indicate group membership. For the interface, the AC portion of the electrical characteristics is measured for each group.
Note 2. There are two types of output buffer, middle drive and high drive. Renesas recommends using the same drive buffer for output skew spec (t_{GTISK}).
Note 3. The drive strength of this port cannot be controlled by PmnPFS.DSCR[1:0] bits.
Note 4. When using NMI pin interrupt, Port related registers setting are not required.

Table 20.9 IO引脚功能的寄存器设置(PORT2)

PSEL[4:0] settings	Function	Pin							
		P200*4	P201	P202	P203	P204	P205	P206	P207
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z							
00001b	AGT	—	—	—	—	AGTIO1	AGTO1	—	—
00010b	GPT	—	—	—	—	GTIW	GTIV	GTIU	—
00011b	GPT*2	—	—	GTIOC5B	GTIOC5A	GTIOC4B	GTIOC4A	—	—
00100b	SCI	—	—	SCK2	CTS2_RTS2/ SS2	SCK4	TXD4/MOSI4/ SDA4	RXD4/MISO4/ SCL4	—
00101b	SCI	—	—	RXD9/MISO9/ SCL9	TXD9/MOSI9/ SDA9	SCK9	CTS9_RTS9/ SS9	—	—
00110b	SPI*1	—	—	MISOB_A	MOSIB_A	RSPCKB_A	SSLB0_A	SSLB1_A	SSLB2_A
00111b	IIC*1	—	—	—	—	SCL0_B	SCL1_A	SDA1_A	—
01001b	CLKOUT/ACMPHS/RTC	—	—	—	—	—	CLKOUT	—	—
01010b	CAC/ADC12	—	—	—	—	CACREF	—	—	—
01011b	BUS	—	—	WR1/BC1	A19	A18	A16	WAIT	A17
01100b	CTSU	—	—	—	TSCAP	TS00	TSCAP	TS01	TS02
10000b	CAN	—	—	CRX0	CTX0	—	—	—	—
10001b	QSPI	—	—	—	—	—	—	—	QSSL
10010b	SSIE*1	—	—	—	—	SSIBCK1_A	SSILRCK1/SSI FS1_A	SSIDATA1_A	—
10011b	USBFS	—	—	—	—	USB_OVRCU RB-DS	USB_OVRCU RA-DS	USB_VBUSEN	—
10101b	SDHI*1	—	—	SD0DAT6_A	SD0DAT5_A	SD0DAT4_A	SD0DAT3_A	SD0DAT2_A	—
10110b	ETHERC (MII)	—	—	ET0_ERXD2	ET0_COL	ET0_RX_DV	ET0_WOL	ET0_LINKSTA	—
10111b	ETHERC (RMII)	—	—	—	—	—	ET0_WOL	ET0_LINKSTA	—
11001b	GLCDC	—	—	LCD_TCON3_ B	—	—	—	—	LCD_DATA23_ B
ASEL bit		-	-	-	-	-	-	-	-
ISEL bit		-	-	IRQ3-DS	IRQ2-DS	-	IRQ1-DS	IRQ0-DS	-
DSCR[1:0] bits	驱动容量控制	-	*3	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H
NCODR bit	N-ch open-drain	-	✓	✓	✓	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓	✓	✓	✓	✓
引脚数	176 pins	✓	✓	✓	✓	✓	✓	✓	✓
	144 pins, 145 pins	✓	✓	✓	✓	✓	✓	✓	✓
	100 pins	✓	✓	-	-	-	✓	✓	✓

:可用—:禁止设置

Note 1. 瑞萨电子建议使用名称后附有字母的引脚，例如”_A”或”_B”，以表示组成员身份。对于接口，测量每组电气特性的交流部分。
Note 2. 输出缓冲器有两种类型，中驱动和高驱动。Renesas建议使用相同的驱动缓冲器来实现输出偏斜规范(tGTISK)。
Note 3. 此端口的驱动强度不能由PmnPFS.DSCR[1:0]位控制。
Note 4. 使用NMI引脚中断时，不需要设置端口相关的寄存器。

Table 20.10 Register settings for I/O pin functions (PORT2)

PSEL[4:0] settings	Function	Pin						
		P208	P209	P210	P211	P212	P213	P214
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z						
00001b	AGT	—	—	—	—	AGTEE1	—	—
00010b	GPT	GTOVL0	GTOVUP	GTIW	GTIV	GTETRGD	GTETRGC	GTIU
00011b	GPT*2	—	—	—	—	GTIOC0B	GTIOC0A	—
00101b	SCI	—	—	—	—	RXD1/MISO1/ SCL1	TXD1/MOSI1/ SDA1	—
01010b	CAC/ADC12	—	—	—	—	—	ADTRG1	—
10001b	QSPI	QIO3	QIO2	QIO1	QIO0	—	—	QSPCLK
10101b	SDHI*1	SD0DAT0_B	SD0WP	SD0CD	SD0CMD_B	—	—	SD0CLK_B
10110b	ETHERC (MII)	ET0_LINKSTA	ET0_EXOUT	ET0_WOL	ET0_MDIO	—	—	ET0_MDC
10111b	ETHERC (RMII)	ET0_LINKSTA	ET0_EXOUT	ET0_WOL	ET0_MDIO	—	—	ET0_MDC
11001b	GLCDC	LCD_DATA18_ B	LCD_DATA19_ B	LCD_DATA20_ B	LCD_DATA21_ B	—	—	LCD_DATA22_ B
11010b	Trace (Debug)	TDATA3	TDATA2	TDATA1	TDATA0	—	—	TCLK
ASEL bit		-	-	-	-	-	-	-
ISEL bit		-	-	-	-	IRQ3	IRQ2	-
DSCR[1:0] bits	Drive capacity control	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H
NCODR bit	N-ch open-drain	✓	✓	✓	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓	✓	✓	✓
Number of pins	176 pins	✓	✓	✓	✓	✓	✓	✓
	144 pins, 145 pins	✓	✓	✓	✓	✓	✓	✓
	100 pins	✓	✓	✓	✓	✓	✓	✓

✓: Available
—: Setting prohibited

Note 1. Renesas recommends using pins that have a letter appended to their names, for instance “_A” or “_B”, to indicate group membership. For the interface, the AC portion of the electrical characteristics is measured for each group.
Note 2. There are two types of output buffer, middle drive and high drive. Renesas recommends using the same drive buffer for output skew spec (t_{GTISK}).

Table 20.10 IO引脚功能的寄存器设置(PORT2)

PSEL[4:0] settings	Function	Pin						
		P208	P209	P210	P211	P212	P213	P214
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z						
00001b	AGT	—	—	—	—	AGTEE1	—	—
00010b	GPT	GTOVL0	GTOVUP	GTIW	GTIV	GTETRGD	GTETRGC	GTIU
00011b	GPT*2	—	—	—	—	GTIOC0B	GTIOC0A	—
00101b	SCI	—	—	—	—	RXD1/MISO1/ SCL1	TXD1/MOSI1/ SDA1	—
01010b	CAC/ADC12	—	—	—	—	—	ADTRG1	—
10001b	QSPI	QIO3	QIO2	QIO1	QIO0	—	—	QSPCLK
10101b	SDHI*1	SD0DAT0_B	SD0WP	SD0CD	SD0CMD_B	—	—	SD0CLK_B
10110b	ETHERC (MII)	ET0_LINKSTA	ET0_EXOUT	ET0_WOL	ET0_MDIO	—	—	ET0_MDC
10111b	ETHERC (RMII)	ET0_LINKSTA	ET0_EXOUT	ET0_WOL	ET0_MDIO	—	—	ET0_MDC
11001b	GLCDC	LCD_DATA18_ B	LCD_DATA19_ B	LCD_DATA20_ B	LCD_DATA21_ B	—	—	LCD_DATA22_ B
11010b	Trace (Debug)	TDATA3	TDATA2	TDATA1	TDATA0	—	—	TCLK
ASEL bit		-	-	-	-	-	-	-
ISEL bit		-	-	-	-	IRQ3	IRQ2	-
DSCR[1:0] bits	驱动容量控制	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H
NCODR bit	N-ch open-drain	✓	✓	✓	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓	✓	✓	✓
引脚数	176 pins	✓	✓	✓	✓	✓	✓	✓
	144 pins, 145 pins	✓	✓	✓	✓	✓	✓	✓
	100 pins	✓	✓	✓	✓	✓	✓	✓

:可用—:禁止设置

Note 1. 瑞萨电子建议使用名称后附有字母的引脚，例如"_A"或"_B"，以表示组成员身份。对于接口，测量每组电气特性的交流部分。
Note 2. 输出缓冲器有两种类型，中驱动和高驱动。Renesas建议使用相同的驱动缓冲器来实现输出偏斜规范(tGTISK)。

Table 20.11 Register settings for I/O pin functions (PORT3)

PSEL[4:0] settings	Function	Pin							
		P300	P301	P302	P303	P304	P305	P306	P307
00000b (value after reset)	Hi-Z/JTAG/SWD	TCK/SWCLK	Hi-Z						
00001b	AGT	—	AGTIO0	—	—	—	—	—	—
00010b	GPT	—	GTOULO	GTOUUP	—	GTOWLO	GTOWUP	GTOULO	GTOUUP
00011b	GPT*2	GTIOC0A_A	GTIOC4B	GTIOC4A	GTIOC7B	GTIOC7A	—	—	—
00100b	SCI	—	RXD2/MISO2/ SCL2	TXD2/MOSI2/ SDA2	—	RXD6/MISO6/ SCL6	TXD6/MOSI6/ SDA6	SCK6	CTS6_RTS6/ SS6
00101b	SCI	—	CTS9_RTS9/ SS9	—	—	—	—	—	—
00110b	SPI*1	SSLB1_B	SSLB2_B	SSLB3_B	—	—	—	—	—
01011b	BUS	—	A06	A07	A08	A09	A10	A11	A12
10001b	QSPI	—	—	—	—	—	QSPCLK	QSSL	QIO0
11001b	GLCDC	—	LCD_DATA13_ A	LCD_DATA14_ A	LCD_DATA15_ A	LCD_DATA16_ A	LCD_DATA17_ A	LCD_DATA18_ A	LCD_DATA19_ A
ASEL bit		-	-	-	-	-	-	-	-
ISEL bit		-	IRQ6	IRQ5	-	IRQ9	IRQ8	-	-
DSCR[1:0] bits	Drive capacity control	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H
NCODR bit	N-ch open-drain	✓	✓	✓	✓	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓	✓	✓	✓	✓
Number of pins	176 pins	✓	✓	✓	✓	✓	✓	✓	✓
	144 pins, 145 pins	✓	✓	✓	✓	✓	✓	✓	✓
	100 pins	✓	✓	✓	✓	✓	✓	✓	✓

✓: Available

—: Setting prohibited

Note 1. Renesas recommends using pins that have a letter appended to their names, for instance “_A” or “_B”, to indicate group membership. For the interface, the AC portion of the electrical characteristics is measured for each group.

Note 2. There are two types of output buffer, middle drive and high drive. Renesas recommends using the same drive buffer for output skew spec (t_{GTISK}).

Table 20.11 IO引脚功能的寄存器设置(PORT3)

PSEL[4:0] settings	Function	Pin							
		P300	P301	P302	P303	P304	P305	P306	P307
00000b (value after reset)	Hi-Z/JTAG/SWD	TCK/SWCLK	Hi-Z						
00001b	AGT	—	AGTIO0	—	—	—	—	—	—
00010b	GPT	—	GTOULO	GTOUUP	—	GTOWLO	GTOWUP	GTOULO	GTOUUP
00011b	GPT*2	GTIOC0A_A	GTIOC4B	GTIOC4A	GTIOC7B	GTIOC7A	—	—	—
00100b	SCI	—	RXD2/MISO2/ SCL2	TXD2/MOSI2/ SDA2	—	RXD6/MISO6/ SCL6	TXD6/MOSI6/ SDA6	SCK6	CTS6_RTS6/ SS6
00101b	SCI	—	CTS9_RTS9/ SS9	—	—	—	—	—	—
00110b	SPI*1	SSLB1_B	SSLB2_B	SSLB3_B	—	—	—	—	—
01011b	BUS	—	A06	A07	A08	A09	A10	A11	A12
10001b	QSPI	—	—	—	—	—	QSPCLK	QSSL	QIO0
11001b	GLCDC	—	LCD_DATA13_ A	LCD_DATA14_ A	LCD_DATA15_ A	LCD_DATA16_ A	LCD_DATA17_ A	LCD_DATA18_ A	LCD_DATA19_ A
ASEL bit		-	-	-	-	-	-	-	-
ISEL bit		-	IRQ6	IRQ5	-	IRQ9	IRQ8	-	-
DSCR[1:0] bits	驱动容量控制	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H
NCODR bit	N-ch open-drain	✓	✓	✓	✓	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓	✓	✓	✓	✓
引脚数	176 pins	✓	✓	✓	✓	✓	✓	✓	✓
	144 pins, 145 pins	✓	✓	✓	✓	✓	✓	✓	✓
	100 pins	✓	✓	✓	✓	✓	✓	✓	✓

:可用一:禁止设置

Note 1. 瑞萨电子建议使用名称后附有字母的引脚，例如"_A"或"_B"，以表示组成员身份。对于接口，测量每组电气特性的交流部分。

Note 2. 输出缓冲器有两种类型，中驱动和高驱动。Renesas建议使用相同的驱动缓冲器来实现输出偏斜规范(tGTISK)。

Table 20.12 Register settings for I/O pin functions (PORT3)

PSEL[4:0] settings	Function	Pin							
		P308	P309	P310	P311	P312	P313	P314	P315
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z							
00001b	AGT	—	—	AGTEE1	AGTOB1	AGTOA1	—	—	—
00100b	SCI	—	—	—	—	—	—	—	RXD4
00101b	SCI	—	RXD3	TXD3	SCK3	CTS3_RTS3/ SS3	—	—	—
01010b	CAC/ADC12	—	—	—	—	—	—	ADTRG0	—
01011b	BUS	A13	A14	A15	CS2/RAS	CS3/CAS	A20	A21	A22
10001b	QSPI	QIO1	QIO2	QIO3	—	—	—	—	—
10101b	SDHI*1	—	—	—	—	—	SD0DAT7_A	—	—
10110b	ETHERC (MII)	—	—	—	—	—	ET0_ERXD3	—	—
11001b	GLCDC	LCD_DATA20_ A	LCD_DATA21_ A	LCD_DATA22_ A	LCD_DATA23_ A	—	LCD_TCON2_ B	LCD_TCON1_ B	LCD_TCON0_ B
ASEL bit		-	-	-	-	-	-	-	-
ISEL bit		-	-	-	-	-	-	-	-
DSCR[1:0] bits	Drive capacity control	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H
NCODR bit	N-ch open-drain	✓	✓	✓	✓	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓	✓	✓	✓	✓
Number of pins	176 pins	✓	✓	✓	✓	✓	✓	✓	✓
	144 pins, 145 pins	✓	✓	✓	✓	✓	✓	-	-
	100 pins	-	-	-	-	-	-	-	-

✓: Available
—: Setting prohibited

Note 1. Renesas recommends using pins that have a letter appended to their names, for instance “_A” or “_B”, to indicate group membership. For the interface, the AC portion of the electrical characteristics is measured for each group.

Table 20.12 IO引脚功能的寄存器设置(PORT3)

PSEL[4:0] settings	Function	Pin							
		P308	P309	P310	P311	P312	P313	P314	P315
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z							
00001b	AGT	—	—	AGTEE1	AGTOB1	AGTOA1	—	—	—
00100b	SCI	—	—	—	—	—	—	—	RXD4
00101b	SCI	—	RXD3	TXD3	SCK3	CTS3_RTS3/ SS3	—	—	—
01010b	CAC/ADC12	—	—	—	—	—	—	ADTRG0	—
01011b	BUS	A13	A14	A15	CS2/RAS	CS3/CAS	A20	A21	A22
10001b	QSPI	QIO1	QIO2	QIO3	—	—	—	—	—
10101b	SDHI*1	—	—	—	—	—	SD0DAT7_A	—	—
10110b	ETHERC (MII)	—	—	—	—	—	ET0_ERXD3	—	—
11001b	GLCDC	LCD_DATA20_ A	LCD_DATA21_ A	LCD_DATA22_ A	LCD_DATA23_ A	—	LCD_TCON2_ B	LCD_TCON1_ B	LCD_TCON0_ B
ASEL bit		-	-	-	-	-	-	-	-
ISEL bit		-	-	-	-	-	-	-	-
DSCR[1:0] bits	驱动容量控制	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H
NCODR bit	N-ch open-drain	✓	✓	✓	✓	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓	✓	✓	✓	✓
引脚数	176 pins	✓	✓	✓	✓	✓	✓	✓	✓
	144 pins, 145 pins	✓	✓	✓	✓	✓	✓	-	-
	100 pins	-	-	-	-	-	-	-	-

:可用—:禁止设置

Note 1. 瑞萨电子建议使用名称后附有字母的引脚，例如”_A”或”_B”，以表示组成员身份。对于接口，测量每组电气特性的交流部分。

Table 20.13 Register settings for I/O pin functions (PORT4)

PSEL[4:0] settings	Function	Pin							
		P400	P401	P402	P403	P404	P405	P406	P407
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z							
00001b	AGT	AGTIO1	—	—	—	—	—	—	AGTIO0
00010b	GPT	—	GTETRGA	—	—	—	—	—	—
00011b	GPT*3	GTIOC6A	GTIOC6B	—	GTIOC3A	GTIOC3B	GTIOC1A	GTIOC1B	—
00100b	SCI	SCK4	CTS4_RTS4/ SS4	—	—	—	—	—	CTS4_RTS4/ SS4
00101b	SCI	SCK7	TXD7/MOSI7/ SDA7	RXD7/MISO7/ SCL7	CTS7_RTS7/ SS7	—	—	—	—
00110b	SPI*2	—	—	—	—	—	—	SSLB3_C	SSLB3_A
00111b	IIC*2	SCL0_A	SDA0_A	—	—	—	—	—	SDA0_B
01001b	CLKOUT/ACMPHS/RTC	—	—	—	—	—	—	—	RTCOUT
01010b	CAC/ADC12	ADTRG1	—	CACREF	—	—	—	—	ADTRG0
01100b	CTSU	—	—	—	—	—	—	—	TS03
10000b	CAN	—	CTX0	CRX0	—	—	—	—	—
10010b	SSIE*2	AUDIO_CLK	—	AUDIO_CLK	SSIBCK0_A	SSILRCK0/SSIFS0_A	SSITXD0_A	SSIRXD0_A	—
10011b	USBFS	—	—	—	—	—	—	—	USB_VBUS
10101b	SDHI*2	—	—	—	SD1DAT7_B	SD1DAT6_B	SD1DAT5_B	SD1DAT4_B	—
10110b	ETHERC (MII)	ET0_WOL	ET0_MDC	ET0_MDIO	ET0_LINKSTA	ET0_EXOUT	ET0_TX_EN	ET0_RX_ER	ET0_EXOUT
10111b	ETHERC (RMII)*2	ET0_WOL	ET0_MDC	ET0_MDIO	ET0_LINKSTA	ET0_EXOUT	RMII0_TXD_EN_B	RMII0_TXD1_B	ET0_EXOUT
11000b	PDC	—	—	VSYNC	PIXD7	PIXD6	PIXD5	PIXD4	—
Don't-care	AGT, RTC	—	—	AGTIO0*1/ AGTIO1*1/ RTCIC0*1	AGTIO0*1/ AGTIO1*1/ RTCIC1*1	RTCIC2*1	—	—	—
ASEL bit		-	-	-	-	-	-	-	-
ISEL bit		IRQ0	IRQ5-DS	IRQ4-DS	-	-	-	-	-
DSCR[1:0] bits	Drive capacity control	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H
NCODR bit	N-ch open-drain	✓	✓	✓	✓	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓	✓	✓	✓	✓
Number of pins	176 pins	✓	✓	✓	✓	✓	✓	✓	✓
	144 pins, 145 pins	✓	✓	✓	✓	✓	✓	✓	✓
	100 pins	✓	✓	✓	✓	✓	✓	✓	✓

✓: Available
—: Setting prohibited

Note 1. To use this pin function, set the associated pin as a general input (set the PmnPFS.PDR and PmnPFS.PMR bits to 0).
Note 2. Renesas recommends using pins that have a letter appended to their names, for instance "_A" or "_B", to indicate group membership. For the interface, the AC portion of the electrical characteristics is measured for each group.
Note 3. There are two types of output buffer, middle drive and high drive. Renesas recommends using the same drive buffer for output skew spec (t_{GTISK}).

Table 20.13 IO引脚功能的寄存器设置(PORT4)

PSEL[4:0] settings	Function	Pin							
		P400	P401	P402	P403	P404	P405	P406	P407
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z							
00001b	AGT	AGTIO1	—	—	—	—	—	—	AGTIO0
00010b	GPT	—	GTETRGA	—	—	—	—	—	—
00011b	GPT*3	GTIOC6A	GTIOC6B	—	GTIOC3A	GTIOC3B	GTIOC1A	GTIOC1B	—
00100b	SCI	SCK4	CTS4_RTS4/ SS4	—	—	—	—	—	CTS4_RTS4/ SS4
00101b	SCI	SCK7	TXD7/MOSI7/ SDA7	RXD7/MISO7/ SCL7	CTS7_RTS7/ SS7	—	—	—	—
00110b	SPI*2	—	—	—	—	—	—	SSLB3_C	SSLB3_A
00111b	IIC*2	SCL0_A	SDA0_A	—	—	—	—	—	SDA0_B
01001b	CLKOUT/ACMPHS/RTC	—	—	—	—	—	—	—	RTCOUT
01010b	CAC/ADC12	ADTRG1	—	CACREF	—	—	—	—	ADTRG0
01100b	CTSU	—	—	—	—	—	—	—	TS03
10000b	CAN	—	CTX0	CRX0	—	—	—	—	—
10010b	SSIE*2	AUDIO_CLK	—	AUDIO_CLK	SSIBCK0_A	SSILRCK0/SSIFS0_A	SSITXD0_A	SSIRXD0_A	—
10011b	USBFS	—	—	—	—	—	—	—	USB_VBUS
10101b	SDHI*2	—	—	—	SD1DAT7_B	SD1DAT6_B	SD1DAT5_B	SD1DAT4_B	—
10110b	ETHERC (MII)	ET0_WOL	ET0_MDC	ET0_MDIO	ET0_LINKSTA	ET0_EXOUT	ET0_TX_EN	ET0_RX_ER	ET0_EXOUT
10111b	ETHERC (RMII)*2	ET0_WOL	ET0_MDC	ET0_MDIO	ET0_LINKSTA	ET0_EXOUT	RMII0_TXD_EN_B	RMII0_TXD1_B	ET0_EXOUT
11000b	PDC	—	—	VSYNC	PIXD7	PIXD6	PIXD5	PIXD4	—
Don't-care	AGT, RTC	—	—	AGTIO0*1/ AGTIO1*1/ RTCIC0*1	AGTIO0*1/ AGTIO1*1/ RTCIC1*1	RTCIC2*1	—	—	—
ASEL bit		-	-	-	-	-	-	-	-
ISEL bit		IRQ0	IRQ5-DS	IRQ4-DS	-	-	-	-	-
DSCR[1:0] bits	驱动容量控制	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H
NCODR bit	N-ch open-drain	✓	✓	✓	✓	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓	✓	✓	✓	✓
引脚数	176 pins	✓	✓	✓	✓	✓	✓	✓	✓
	144 pins, 145 pins	✓	✓	✓	✓	✓	✓	✓	✓
	100 pins	✓	✓	✓	✓	✓	✓	✓	✓

:可用—:禁止设置

Note 1. 要使用此引脚功能，请将相关引脚设置为通用输入（将PmnPFS.PDR和PmnPFS.PMR位设置为0）。
Note 2. 瑞萨电子建议使用名称后附有字母的引脚，例如"_A"或"_B"，以表示组成员身份。对于接口，测量每组电气特性的交流部分。
Note 3. 输出缓冲器有两种类型，中驱动和高驱动。Renesas建议使用相同的驱动缓冲器来实现输出偏斜规范(tGTISK)。

Table 20.14 Register settings for I/O pin functions (PORT4)

PSEL[4:0] settings	Function	Pin							
		P408	P409	P410	P411	P412	P413	P414	P415
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z							
00001b	AGT	—	—	AGTOB1	AGTOA1	AGTEE1	—	—	—
00010b	GPT	GTOWLO	GTOWUP	GTOVLO	GTOVUP	GTOULO	GTOUUP	—	—
00011b	GPT*2	GTIOC10B	GTIOC10A	GTIOC9B	GTIOC9A	—	—	GTIOC0B	GTIOC0A
00100b	SCI	—	—	RXD0/MISO0/ SCL0	TXD0/MOSI0/ SDA0	SCK0	CTS0_RTS0/ SS0	—	—
00101b	SCI	RXD3/MISO3/ SCL3	TXD3/MOSI3/ SDA3	SCK3	CTS3_RTS3/ SS3	—	—	—	—
00110b	SPI*1	—	—	MISOA_B	MOSIA_B	RSPCKA_B	SSLA0_B	SSLA1_B	SSLA2_B
00111b	IIC*1	SCL0_B	—	—	—	—	—	—	—
01100b	CTSU	TS04	TS05	TS06	TS07	TS08	TS09	TS10	TS11
10011b	USBFS	USB_ID	USB_EXICEN	—	—	—	—	—	USB_VBUSEN
10100b	USBHS	USBHS_ID	USBHS_EXIC EN	—	—	—	—	—	—
10101b	SDHI*1	—	—	SD0DAT1_A	SD0DAT0_A	SD0CMD_A	SD0CLK_A	SD0WP	SD0CD
10110b	ETHERC (MII)	ET0_CRS	ET0_RX_CLK	ET0_ERXD0	ET0_ERXD1	ET0_ETXD0	ET0_ETXD1		ET0_TX_EN
10111b	ETHERC (RMII)*1	RMII0_CRS_DV_A	RMII0_RX_ER_A	RMII0_RXD1_A	RMII0_RXD0_A	REF50CK0_A	RMII0_TXD0_A	RMII0_TXD1_A	RMII0_TXD_EN_A
11000b	PDC	PIXCLK	HSYNC	PIXD0	PIXD1	PIXD2	PIXD3	PIXD4	PIXD5
ASEL bit		-	-	-	-	-	-	-	-
ISEL bit		IRQ7	IRQ6	IRQ5	IRQ4	-	-	IRQ9	IRQ8
DSCR[1:0] bits	Drive capacity control	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H
NCODR bit	N-ch open-drain	✓	✓	✓	✓	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓	✓	✓	✓	✓
Number of pins	176 pins	✓	✓	✓	✓	✓	✓	✓	✓
	144 pins, 145 pins	✓	✓	✓	✓	✓	✓	✓	✓
	100 pins	✓	✓	✓	✓	✓	✓	✓	✓

✓: Available
—: Setting prohibited

Note 1. Renesas recommends using pins that have a letter appended to their names, for instance “_A” or “_B”, to indicate group membership. For the interface, the AC portion of the electrical characteristics is measured for each group.
Note 2. There are two types of output buffer, middle drive and high drive. Renesas recommends using the same drive buffer for output skew spec (t_{GTISK}).

Table 20.14 IO引脚功能的寄存器设置(PORT4)

PSEL[4:0] settings	Function	Pin							
		P408	P409	P410	P411	P412	P413	P414	P415
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z							
00001b	AGT	—	—	AGTOB1	AGTOA1	AGTEE1	—	—	—
00010b	GPT	GTOWLO	GTOWUP	GTOVLO	GTOVUP	GTOULO	GTOUUP	—	—
00011b	GPT*2	GTIOC10B	GTIOC10A	GTIOC9B	GTIOC9A	—	—	GTIOC0B	GTIOC0A
00100b	SCI	—	—	RXD0/MISO0/ SCL0	TXD0/MOSI0/ SDA0	SCK0	CTS0_RTS0/ SS0	—	—
00101b	SCI	RXD3/MISO3/ SCL3	TXD3/MOSI3/ SDA3	SCK3	CTS3_RTS3/ SS3	—	—	—	—
00110b	SPI*1	—	—	MISOA_B	MOSIA_B	RSPCKA_B	SSLA0_B	SSLA1_B	SSLA2_B
00111b	IIC*1	SCL0_B	—	—	—	—	—	—	—
01100b	CTSU	TS04	TS05	TS06	TS07	TS08	TS09	TS10	TS11
10011b	USBFS	USB_ID	USB_EXICEN	—	—	—	—	—	USB_VBUSEN
10100b	USBHS	USBHS_ID	USBHS_EXIC EN	—	—	—	—	—	—
10101b	SDHI*1	—	—	SD0DAT1_A	SD0DAT0_A	SD0CMD_A	SD0CLK_A	SD0WP	SD0CD
10110b	ETHERC (MII)	ET0_CRS	ET0_RX_CLK	ET0_ERXD0	ET0_ERXD1	ET0_ETXD0	ET0_ETXD1		ET0_TX_EN
10111b	ETHERC (RMII)*1	RMII0_CRS_DV_A	RMII0_RX_ER_A	RMII0_RXD1_A	RMII0_RXD0_A	REF50CK0_A	RMII0_TXD0_A	RMII0_TXD1_A	RMII0_TXD_EN_A
11000b	PDC	PIXCLK	HSYNC	PIXD0	PIXD1	PIXD2	PIXD3	PIXD4	PIXD5
ASEL bit		-	-	-	-	-	-	-	-
ISEL bit		IRQ7	IRQ6	IRQ5	IRQ4	-	-	IRQ9	IRQ8
DSCR[1:0] bits	驱动容量控制	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H
NCODR bit	N-ch open-drain	✓	✓	✓	✓	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓	✓	✓	✓	✓
引脚数	176 pins	✓	✓	✓	✓	✓	✓	✓	✓
	144 pins, 145 pins	✓	✓	✓	✓	✓	✓	✓	✓
	100 pins	✓	✓	✓	✓	✓	✓	✓	✓

:可用—:禁止设置

Note 1. 瑞萨电子建议使用名称后附有字母的引脚，例如“_A”或“_B”，以表示组成员身份。对于接口，测量每组电气特性的交流部分。
Note 2. 输出缓冲器有两种类型，中驱动和高驱动。Renesas建议使用相同的驱动缓冲器来实现输出偏斜规范(tGTISK)。

Table 20.15 Register settings for I/O pin functions (PORT5)

PSEL[4:0] settings	Function	Pin							
		P500	P501	P502	P503	P504	P505	P506	P507
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z							
00001b	AGT	AGTOA0	AGTOB0	—	—	—	—	—	—
00010b	GPT	GTIU	GTIV	GTIW	GTETRGC	GTETRGD	—	—	—
00011b	GPT*2	GTIOC11A	GTIOC11B	GTIOC12A	GTIOC12B	GTIOC13A	GTIOC13B	—	—
00100b	SCI	—	—	—	CTS6_RTS6/ SS6	SCK6	RXD6/MISO6/ SCL6	TXD6/MOSI6/ SDA6	—
00101b	SCI	—	TXD5/MOSI5/ SDA5	RXD5/MISO5/ SCL5	SCK5	CTS5_RTS5/S S5	—	—	CTS5_RTS5/ SS5
01011b	BUS	—	—	—	—	ALE	—	—	—
10001b	QSPI	QSPCLK	QSSL	QIO0	QIO1	QIO2	QIO3	—	—
10011b	USBFS	USB_VBUSEN	USB_OVRCU RA	USB_OVRCU RB	USB_EXICEN	USB_ID	—	—	—
10101b	SDHI*1	SD1CLK_A	SD1CMD_A	SD1DAT0_A	SD1DAT1_A	SD1DAT2_A	SD1DAT3_A	SD1CD	SD1WP_A
ASEL bit		AN016/ IVREF0	AN116/ IVREF1	AN017/ IVCMP0	AN117	AN018	AN118	AN019	AN119
ISEL bit		-	IRQ11	IRQ12	-	-	IRQ14	IRQ15	-
DSCR[1:0] bits	Drive capacity control	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H
NCODR bit	N-ch open-drain	✓	✓	✓	✓	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓	✓	✓	✓	✓
Number of pins	176 pins	✓	✓	✓	✓	✓	✓	✓	✓
	144 pins, 145 pins	✓	✓	✓	✓	✓	✓	✓	-
	100 pins	✓	✓	✓	✓	✓	-	-	-

✓: Available
—: Setting prohibited

Note 1. Renesas recommends using pins that have a letter appended to their names, for instance “_A” or “_B”, to indicate group membership. For the interface, the AC portion of the electrical characteristics is measured for each group.
Note 2. There are two types of output buffer, middle drive and high drive. Renesas recommends using the same drive buffer for output skew spec (t_{GTISK}).

Table 20.15 IO引脚功能的寄存器设置(PORT5)

PSEL[4:0] settings	Function	Pin							
		P500	P501	P502	P503	P504	P505	P506	P507
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z							
00001b	AGT	AGTOA0	AGTOB0	—	—	—	—	—	—
00010b	GPT	GTIU	GTIV	GTIW	GTETRGC	GTETRGD	—	—	—
00011b	GPT*2	GTIOC11A	GTIOC11B	GTIOC12A	GTIOC12B	GTIOC13A	GTIOC13B	—	—
00100b	SCI	—	—	—	CTS6_RTS6/ SS6	SCK6	RXD6/MISO6/ SCL6	TXD6/MOSI6/ SDA6	—
00101b	SCI	—	TXD5/MOSI5/ SDA5	RXD5/MISO5/ SCL5	SCK5	CTS5_RTS5/S S5	—	—	CTS5_RTS5/ SS5
01011b	BUS	—	—	—	—	ALE	—	—	—
10001b	QSPI	QSPCLK	QSSL	QIO0	QIO1	QIO2	QIO3	—	—
10011b	USBFS	USB_VBUSEN	USB_OVRCU RA	USB_OVRCU RB	USB_EXICEN	USB_ID	—	—	—
10101b	SDHI*1	SD1CLK_A	SD1CMD_A	SD1DAT0_A	SD1DAT1_A	SD1DAT2_A	SD1DAT3_A	SD1CD	SD1WP_A
ASEL bit		AN016/ IVREF0	AN116/ IVREF1	AN017/ IVCMP0	AN117	AN018	AN118	AN019	AN119
ISEL bit		-	IRQ11	IRQ12	-	-	IRQ14	IRQ15	-
DSCR[1:0] bits	驱动容量控制	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H
NCODR bit	N-ch open-drain	✓	✓	✓	✓	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓	✓	✓	✓	✓
引脚数	176 pins	✓	✓	✓	✓	✓	✓	✓	✓
	144 pins, 145 pins	✓	✓	✓	✓	✓	✓	✓	-
	100 pins	✓	✓	✓	✓	✓	-	-	-

:可用—:禁止设置

Note 1. 瑞萨电子建议使用名称后附有字母的引脚，例如"_A"或"_B"，以表示组成员身份。对于接口，测量每组电气特性的交流部分。
Note 2. 输出缓冲器有两种类型，中驱动和高驱动。Renesas建议使用相同的驱动缓冲器来实现输出偏斜规范(tGTISK)。

Table 20.16 Register settings for I/O pin functions (PORT5)

PSEL[4:0] settings	Function	Pin			
		P508	P511	P512	P513
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z			
00010b	GPT	—	—	—	—
00011b	GPT*1	—	GTIOC0B	GTIOC0A	—
00100b	SCI	SCK6	RXD4/MISO4/SCL4	TXD4/MOSI4/SDA4	—
00101b	SCI	SCK5	—	—	RXD5
00111b	IIC	—	SDA2	SCL2	—
10000b	CAN	—	CRX1	CTX1	—
11000b	PDC	—	PCKO	VSYNC	—
11001b	GLCDC	—	—	—	LCD_DATA16_B
ASEL bit		AN020	-	-	-
ISEL bit		-	IRQ15	IRQ14	-
DSCR[1:0] bits	Drive capacity control	L/M/H	L/M/H	L/M/H	L/M/H
NCODR bit	N-ch open-drain	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓
Number of pins	176 pins	✓	✓	✓	✓
	144 pins, 145 pins	✓	✓	✓	-
	100 pins	✓	-	-	-

✓: Available
—: Setting prohibited

Note 1. There are two types of output buffer, middle drive and high drive. Renesas recommends using the same drive buffer for output skew spec (t_{GTISK}).

Table 20.16 IO引脚功能的寄存器设置(PORT5)

PSEL[4:0] settings	Function	Pin			
		P508	P511	P512	P513
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z			
00010b	GPT	—	—	—	—
00011b	GPT*1	—	GTIOC0B	GTIOC0A	—
00100b	SCI	SCK6	RXD4/MISO4/SCL4	TXD4/MOSI4/SDA4	—
00101b	SCI	SCK5	—	—	RXD5
00111b	IIC	—	SDA2	SCL2	—
10000b	CAN	—	CRX1	CTX1	—
11000b	PDC	—	PCKO	VSYNC	—
11001b	GLCDC	—	—	—	LCD_DATA16_B
ASEL bit		AN020	-	-	-
ISEL bit		-	IRQ15	IRQ14	-
DSCR[1:0] bits	驱动容量控制	L/M/H	L/M/H	L/M/H	L/M/H
NCODR bit	N-ch open-drain	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓
引脚数	176 pins	✓	✓	✓	✓
	144 pins, 145 pins	✓	✓	✓	-
	100 pins	✓	-	-	-

:可用—:禁止设置

Note 1. 输出缓冲器有两种类型，中驱动和高驱动。Renesas建议使用相同的驱动缓冲器来实现输出偏斜规范(tGTISK)。

Table 20.17 Register settings for I/O pin functions (PORT6)

PSEL[4:0] settings	Function	Pin							
		P600	P601	P602	P603	P604	P605	P606	P607
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z							
00011b	GPT*1	GTIOC6B	GTIOC6A	GTIOC7B	GTIOC7A	GTIOC8B	GTIOC8A	—	—
00100b	SCI	—	—	—	—	—	—	CTS8_RTS8/ SS8	RXD8
00101b	SCI	SCK9	RXD9	TXD9	CTS9_RTS9/ SS9	—	—	—	—
01001b	CLKOUT/ACMPHS/RTC	CLKOUT	—	—	—	—	—	RTCOUT	—
01010b	CAC/ADC12	CACREF	—	—	—	—	—	—	—
01011b	BUS	RD	WR/ WR0/ DQM00	EBCLK/ SDCLK	D13[A13/D13]/ DQ13	D12[A12/D12]/ DQ12	D11[A11/D11]/ DQ11	—	—
11001b	GLCDC	LCD_DATA02_A	LCD_DATA03_A	LCD_DATA04_A	—	—	—	LCD_DATA03_B	LCD_DATA04_B
ASEL bit		-	-	-	-	-	-	-	-
ISEL bit		-	-	-	-	-	-	-	-
DSCR[1:0] bits	Drive capacity control	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H
NCODR bit	N-ch open-drain	✓	✓	✓	✓	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓	✓	✓	✓	✓
Number of pins	176 pins	✓	✓	✓	✓	✓	✓	✓	✓
	144 pins, 145 pins	✓	✓	✓	✓	✓	✓	-	-
	100 pins	✓	✓	✓	-	-	-	-	-

✓: Available

—: Setting prohibited

Note 1. There are two types of output buffer, middle drive and high drive. Renesas recommends using the same drive buffer for output skew spec (t_{GTISK}).

Table 20.17 IO引脚功能的寄存器设置(PORT6)

PSEL[4:0] settings	Function	Pin							
		P600	P601	P602	P603	P604	P605	P606	P607
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z							
00011b	GPT*1	GTIOC6B	GTIOC6A	GTIOC7B	GTIOC7A	GTIOC8B	GTIOC8A	—	—
00100b	SCI	—	—	—	—	—	—	CTS8_RTS8/ SS8	RXD8
00101b	SCI	SCK9	RXD9	TXD9	CTS9_RTS9/ SS9	—	—	—	—
01001b	CLKOUT/ACMPHS/RTC	CLKOUT	—	—	—	—	—	RTCOUT	—
01010b	CAC/ADC12	CACREF	—	—	—	—	—	—	—
01011b	BUS	RD	WR/ WR0/ DQM00	EBCLK/ SDCLK	D13[A13/D13]/ DQ13	D12[A12/D12]/ DQ12	D11[A11/D11]/ DQ11	—	—
11001b	GLCDC	LCD_DATA02_A	LCD_DATA03_A	LCD_DATA04_A	—	—	—	LCD_DATA03_B	LCD_DATA04_B
ASEL bit		-	-	-	-	-	-	-	-
ISEL bit		-	-	-	-	-	-	-	-
DSCR[1:0] bits	驱动容量控制	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H
NCODR bit	N-ch open-drain	✓	✓	✓	✓	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓	✓	✓	✓	✓
引脚数	176 pins	✓	✓	✓	✓	✓	✓	✓	✓
	144 pins, 145 pins	✓	✓	✓	✓	✓	✓	-	-
	100 pins	✓	✓	✓	-	-	-	-	-

:可用一:禁止设置

Note 1. 输出缓冲器有两种类型，中驱动和高驱动。Renesas建议使用相同的驱动缓冲器来实现输出偏斜规范(tGTISK)。

Table 20.18 Register settings for I/O pin functions (PORT6)

PSEL[4:0] settings	Function	Pin							
		P608	P609	P610	P611	P612	P613	P614	P615
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z							
00011b	GPT*1	GTIOC4B	GTIOC5A	GTIOC5B	—	—	—	—	—
00101b	SCI	—	—	—	CTS7_RTS7/ SS7	SCK7	TXD7	RXD7	—
01001b	CLKOUT/ACMPHS/RTC	—	—	—	CLKOUT	—	—	—	—
01010b	CAC/ADC12	—	—	—	CACREF	—	—	—	—
01011b	BUS	A00/BC0/ DQM1	CS1/CKE	CS0/WE	SDCS	D08[A08/D08]/ DQ08	D09[A09/D09]/ DQ09	D10[A10/D10]/ DQ10	—
10000b	CAN	—	CTX1	CRX1	—	—	—	—	—
11001b	GLCDC	LCD_DATA07_A	LCD_DATA06_A	LCD_DATA05_A	—	—	—	—	LCD_DATA10_B
ASEL bit		-	-	-	-	-	-	-	-
ISEL bit		-	-	-	-	-	-	-	-
DSCR[1:0] bits	Drive capacity control	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H
NCODR bit	N-ch open-drain	✓	✓	✓	✓	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓	✓	✓	✓	✓
Number of pins	176 pins	✓	✓	✓	✓	✓	✓	✓	✓
	144 pins, 145 pins	✓	✓	✓	✓	✓	✓	✓	-
	100 pins	✓	✓	✓	-	-	-	-	-

✓: Available
—: Setting prohibited

Note 1. There are two types of output buffer, middle drive and high drive. Renesas recommends using the same drive buffer for output skew spec (t_{GTISK}).

Table 20.18 IO引脚功能的寄存器设置(PORT6)

PSEL[4:0] settings	Function	Pin							
		P608	P609	P610	P611	P612	P613	P614	P615
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z							
00011b	GPT*1	GTIOC4B	GTIOC5A	GTIOC5B	—	—	—	—	—
00101b	SCI	—	—	—	CTS7_RTS7/ SS7	SCK7	TXD7	RXD7	—
01001b	CLKOUT/ACMPHS/RTC	—	—	—	CLKOUT	—	—	—	—
01010b	CAC/ADC12	—	—	—	CACREF	—	—	—	—
01011b	BUS	A00/BC0/ DQM1	CS1/CKE	CS0/WE	SDCS	D08[A08/D08]/ DQ08	D09[A09/D09]/ DQ09	D10[A10/D10]/ DQ10	—
10000b	CAN	—	CTX1	CRX1	—	—	—	—	—
11001b	GLCDC	LCD_DATA07_A	LCD_DATA06_A	LCD_DATA05_A	—	—	—	—	LCD_DATA10_B
ASEL bit		-	-	-	-	-	-	-	-
ISEL bit		-	-	-	-	-	-	-	-
DSCR[1:0] bits	驱动容量控制	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H
NCODR bit	N-ch open-drain	✓	✓	✓	✓	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓	✓	✓	✓	✓
引脚数	176 pins	✓	✓	✓	✓	✓	✓	✓	✓
	144 pins, 145 pins	✓	✓	✓	✓	✓	✓	✓	-
	100 pins	✓	✓	✓	-	-	-	-	-

:可用一:禁止设置

Note 1. 输出缓冲器有两种类型，中驱动和高驱动。Renesas建议使用相同的驱动缓冲器来实现输出偏斜规范(tGTISK)。

Table 20.19 Register settings for I/O pin functions (PORT7)

PSEL[4:0] settings	Function	Pin							
		P700	P701	P702	P703	P704	P705	P706	P707
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z							
00001b	AGT	—	—	—	—	AGTO0	AGTIO0	—	—
00011b	GPT*2	GTIOC5A	GTIOC5B	GTIOC6A	GTIOC6B	—	—	—	—
00101b	SCI	—	—	—	—	—	—	RXD3/MISO3/SCL3	TXD3/MOSI3/SDA3
00110b	SPI*1	MISOB_C	MOSIB_C	RSPCKB_C	SSLB0_C	SSLB1_C	SSLB2_C	—	—
01001b	CLKOUT/ACMPHS/RTC	—	—	—	VCOUT	—	—	—	—
10000b	CAN	—	—	—	—	CTX0	CRX0	—	—
10100b	USBHS	—	—	—	—	—	—	USBHS_OVRCURB	USBHS_OVRCURA
10101b	SDHI*1	SD1DAT3_B	SD1DAT2_B	SD1DAT1_B	SD1DAT0_B	SD1CLK_B	SD1CMD_B	SD1CD_B	SD1WP_B
10110b	ETHERC (MII)	ET0_ETXD1	ET0_ETXD0	ET0_ERXD1	ET0_ERXD0	ET0_RX_CLK	ET0_CRS	—	—
10111b	ETHERC (RMII)*1	RMII0_TXD0_B	REF50CK0_B	RMII0_RXD0_B	RMII0_RXD1_B	RMII0_RX_ER_B	RMII0_CRS_DV_B	—	—
11000b	PDC	PIXD3	PIXD2	PIXD1	PIXD0	HSYNC	PIXCLK	—	—
ASEL bit		-	-	-	-	-	-	-	-
ISEL bit		-	-	-	-	-	-	IRQ7	IRQ8
DSCR[1:0] bits	Drive capacity control	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H
NCODR bit	N-ch open-drain	✓	✓	✓	✓	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓	✓	✓	✓	✓
Number of pins	176 pins	✓	✓	✓	✓	✓	✓	✓	✓
	144 pins, 145 pins	✓	✓	✓	✓	✓	✓	-	-
	100 pins	-	-	-	-	-	-	-	-

✓: Available
—: Setting prohibited

Note 1. Renesas recommends using pins that have a letter appended to their names, for instance “_A” or “_B”, to indicate group membership. For the interface, the AC portion of the electrical characteristics is measured for each group.
Note 2. There are two types of output buffer, middle drive and high drive. Renesas recommends using the same drive buffer for output skew spec (t_{GTISK}).

Table 20.19 IO引脚功能的寄存器设置(PORT7)

PSEL[4:0] settings	Function	Pin							
		P700	P701	P702	P703	P704	P705	P706	P707
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z							
00001b	AGT	—	—	—	—	AGTO0	AGTIO0	—	—
00011b	GPT*2	GTIOC5A	GTIOC5B	GTIOC6A	GTIOC6B	—	—	—	—
00101b	SCI	—	—	—	—	—	—	RXD3/MISO3/SCL3	TXD3/MOSI3/SDA3
00110b	SPI*1	MISOB_C	MOSIB_C	RSPCKB_C	SSLB0_C	SSLB1_C	SSLB2_C	—	—
01001b	CLKOUT/ACMPHS/RTC	—	—	—	VCOUT	—	—	—	—
10000b	CAN	—	—	—	—	CTX0	CRX0	—	—
10100b	USBHS	—	—	—	—	—	—	USBHS_OVRCURB	USBHS_OVRCURA
10101b	SDHI*1	SD1DAT3_B	SD1DAT2_B	SD1DAT1_B	SD1DAT0_B	SD1CLK_B	SD1CMD_B	SD1CD_B	SD1WP_B
10110b	ETHERC (MII)	ET0_ETXD1	ET0_ETXD0	ET0_ERXD1	ET0_ERXD0	ET0_RX_CLK	ET0_CRS	—	—
10111b	ETHERC (RMII)*1	RMII0_TXD0_B	REF50CK0_B	RMII0_RXD0_B	RMII0_RXD1_B	RMII0_RX_ER_B	RMII0_CRS_DV_B	—	—
11000b	PDC	PIXD3	PIXD2	PIXD1	PIXD0	HSYNC	PIXCLK	—	—
ASEL bit		-	-	-	-	-	-	-	-
ISEL bit		-	-	-	-	-	-	IRQ7	IRQ8
DSCR[1:0] bits	驱动容量控制	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H
NCODR bit	N-ch open-drain	✓	✓	✓	✓	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓	✓	✓	✓	✓
引脚数	176 pins	✓	✓	✓	✓	✓	✓	✓	✓
	144 pins, 145 pins	✓	✓	✓	✓	✓	✓	-	-
	100 pins	-	-	-	-	-	-	-	-

:可用—:禁止设置

Note 1. 瑞萨电子建议使用名称后附有字母的引脚，例如“_A”或“_B”，以表示组成员身份。对于接口，测量每组电气特性的交流部分。
Note 2. 输出缓冲器有两种类型，中驱动和高驱动。Renesas建议使用相同的驱动缓冲器来实现输出偏斜规范(tGTISK)。

Table 20.20 Register settings for I/O pin functions (PORT7)

PSEL[4:0] settings	Function	Pin					
		P708	P709	P710	P711	P712	P713
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z					
00001b	AGT	—	—	—	AGTEE0	AGTOB0	AGTOA0
00011b	GPT*2	—	—	—	—	GTIOC2B	GTIOC2A
00101b	SCI	RXD1/MISO1/ SCL1	TXD1/MOSI1/ SDA1	SCK1	CTS1_RTS1/ SS1	—	—
00110b	SPI*1	SSLA3_B	—	—	—	—	—
01010b	CAC/ADC12	CACREF	—	—	—	—	—
01100b	CTSU	TS12	TS13	TS14	TS15	TS16	TS17
10010b	SSIE	AUDIO_CLK	—	—	—	—	—
10110b	ETHERC (MII)	ET0_ETXD3	ET0_ETXD2	ET0_TX_ER	ET0_TX_CLK	—	—
11000b	PDC	PCKO	—	—	—	—	—
ASEL bit		-	-	-	-	-	-
ISEL bit		IRQ11	IRQ10	-	-	-	-
DSCR[1:0] bits	Drive capacity control	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H
NCODR bit	N-ch open-drain	✓	✓	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓	✓	✓
Number of pins	176 pins	✓	-	-	-	-	-
	144 pins, 145 pins	✓	✓	✓	✓	✓	✓
	100 pins	✓	-	-	-	-	-

✓: Available
—: Setting prohibited

Note 1. Renesas recommends using pins that have a letter appended to their names, for instance “_A” or “_B”, to indicate group membership. For the interface, the AC portion of the electrical characteristics is measured for each group.
Note 2. There are two types of output buffer, middle drive and high drive. Renesas recommends using the same drive buffer for output skew spec (t_{GTISK}).

Table 20.20 IO引脚功能的寄存器设置(PORT7)

PSEL[4:0] settings	Function	Pin					
		P708	P709	P710	P711	P712	P713
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z					
00001b	AGT	—	—	—	AGTEE0	AGTOB0	AGTOA0
00011b	GPT*2	—	—	—	—	GTIOC2B	GTIOC2A
00101b	SCI	RXD1/MISO1/ SCL1	TXD1/MOSI1/ SDA1	SCK1	CTS1_RTS1/ SS1	—	—
00110b	SPI*1	SSLA3_B	—	—	—	—	—
01010b	CAC/ADC12	CACREF	—	—	—	—	—
01100b	CTSU	TS12	TS13	TS14	TS15	TS16	TS17
10010b	SSIE	AUDIO_CLK	—	—	—	—	—
10110b	ETHERC (MII)	ET0_ETXD3	ET0_ETXD2	ET0_TX_ER	ET0_TX_CLK	—	—
11000b	PDC	PCKO	—	—	—	—	—
ASEL bit		-	-	-	-	-	-
ISEL bit		IRQ11	IRQ10	-	-	-	-
DSCR[1:0] bits	驱动容量控制	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H
NCODR bit	N-ch open-drain	✓	✓	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓	✓	✓
引脚数	176 pins	✓	-	-	-	-	-
	144 pins, 145 pins	✓	✓	✓	✓	✓	✓
	100 pins	✓	-	-	-	-	-

:可用—:禁止设置

Note 1. 瑞萨电子建议使用名称后附有字母的引脚，例如“_A”或“_B”，以表示组成员身份。对于接口，测量每组电气特性的交流部分。
Note 2. 输出缓冲器有两种类型，中驱动和高驱动。Renesas建议使用相同的驱动缓冲器来实现输出偏斜规范(tGTISK)。

Table 20.21 Register settings for I/O pin functions (PORT8)

PSEL[4:0] settings	Function	Pin						
		P800	P801	P802	P803	P804	P805	P806
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z						
00101b	SCI	—	—	—	—	—	TXD5	—
01011b	BUS	D14[A14/D14]/DQ14	D15[A15/D15]/DQ15	—	—	—	—	—
10101b	SDHI*1	—	SD1DAT4_A	SD1DAT5_A	SD1DAT6_A	SD1DAT7_A	—	—
11001b	GLCDC	—	—	LCD_DATA02_B	LCD_DATA01_B	LCD_DATA00_B	LCD_DATA17_B	LCD_EXTCLK_B
ASEL bit		-	-	-	-	-	-	-
ISEL bit		-	-	-	-	-	-	-
DSCR[1:0] bits	Drive capacity control	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H
NCODR bit	N-ch open-drain	✓	✓	✓	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓	✓	✓	✓
Number of pins	176 pins	✓	✓	✓	✓	✓	✓	✓
	144 pins, 145 pins	✓	✓	-	-	-	-	-
	100 pins	-	-	-	-	-	-	-

✓: Available
—: Setting prohibited

Note 1. Renesas recommends using pins that have a letter appended to their names, for instance “_A” or “_B”, to indicate group membership. For the interface, the AC portion of the electrical characteristics is measured for each group.

Table 20.22 Register settings for I/O pin functions (PORT9)

PSEL[4:0] settings	Function	Pin				
		P900	P901	P905	P906	P907
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z				
00001b	AGT	—	AGTIO1	—	—	—
00011b	GPT*1	—	—	GTIOC13B	GTIOC13A	GTIOC12B
00100b	SCI	TXD4	SCK4	—	—	—
01011b	BUS	A23	—	CS4	CS5	CS6
11001b	GLCDC	LCD_CLK_B	LCD_DATA15_B	LCD_DATA11_B	LCD_DATA12_B	LCD_DATA13_B
ASEL bit		-	-	-	-	-
ISEL bit		-	-	-	-	-
DSCR[1:0] bits	Drive capacity control	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H
NCODR bit	N-ch open-drain	✓	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓	✓
Number of pins	176 pins	✓	✓	✓	✓	✓
	144 pins, 145 pins	-	-	-	-	-
	100 pins	-	-	-	-	-

✓: Available
—: Setting prohibited

Note 1. There are two types of output buffer, middle drive and high drive. Renesas recommends using the same drive buffer for output skew spec (t_{GTISK}).

Table 20.21 IO引脚功能的寄存器设置(PORT8)

PSEL[4:0] settings	Function	Pin						
		P800	P801	P802	P803	P804	P805	P806
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z						
00101b	SCI	—	—	—	—	—	TXD5	—
01011b	BUS	D14[A14/D14]/DQ14	D15[A15/D15]/DQ15	—	—	—	—	—
10101b	SDHI*1	—	SD1DAT4_A	SD1DAT5_A	SD1DAT6_A	SD1DAT7_A	—	—
11001b	GLCDC	—	—	LCD_DATA02_B	LCD_DATA01_B	LCD_DATA00_B	LCD_DATA17_B	LCD_EXTCLK_B
ASEL bit		-	-	-	-	-	-	-
ISEL bit		-	-	-	-	-	-	-
DSCR[1:0] bits	驱动容量控制	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H
NCODR bit	N-ch open-drain	✓	✓	✓	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓	✓	✓	✓
引脚数	176 pins	✓	✓	✓	✓	✓	✓	✓
	144 pins, 145 pins	✓	✓	-	-	-	-	-
	100 pins	-	-	-	-	-	-	-

:可用—:禁止设置

Note 1. 瑞萨电子建议使用名称后附有字母的引脚，例如“_A”或“_B”，以表示组成员身份。对于接口，测量每组电气特性的交流部分。

Table 20.22 IO引脚功能的寄存器设置(PORT9)

PSEL[4:0] settings	Function	Pin				
		P900	P901	P905	P906	P907
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z				
00001b	AGT	—	AGTIO1	—	—	—
00011b	GPT*1	—	—	GTIOC13B	GTIOC13A	GTIOC12B
00100b	SCI	TXD4	SCK4	—	—	—
01011b	BUS	A23	—	CS4	CS5	CS6
11001b	GLCDC	LCD_CLK_B	LCD_DATA15_B	LCD_DATA11_B	LCD_DATA12_B	LCD_DATA13_B
ASEL bit		-	-	-	-	-
ISEL bit		-	-	-	-	-
DSCR[1:0] bits	驱动容量控制	L/M/H	L/M/H	L/M/H	L/M/H	L/M/H
NCODR bit	N-ch open-drain	✓	✓	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓	✓	✓
引脚数	176 pins	✓	✓	✓	✓	✓
	144 pins, 145 pins	-	-	-	-	-
	100 pins	-	-	-	-	-

:可用—:禁止设置

Note 1. 输出缓冲器有两种类型，中驱动和高驱动。Renesas建议使用相同的驱动缓冲器来实现输出偏斜规范(tGTISK)。

Table 20.23 Register settings for I/O pin functions (PORT9)

PSEL[4:0] settings	Function	Pin
		P908
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z
00011b	GPT*1	GTIOC12A
01011b	BUS	CS7
11001b	GLCDC	LCD_DATA14_B
ASEL bit		-
ISEL bit		-
DSCR[1:0] bits	Drive capacity control	L/M/H
NCODR bit	N-ch open-drain	✓
PCR bit	Pull-up	✓
Number of pins	176 pins	✓
	144 pins, 145 pins	-
	100 pins	-

✓: Available
—: Setting prohibited

Note 1. There are two types of output buffer, middle drive and high drive. Renesas recommends using the same drive buffer for output skew spec (t_{GTISK}).

Table 20.24 Register settings for I/O pin functions (PORTA)

PSEL[4:0] settings	Function	Pin	
		PA00	PA01
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z	
00100b	SCI	TXD8	SCK8
11001b	GLCDC	LCD_DATA05_B	LCD_DATA06_B
ASEL bit		-	-
ISEL bit		-	-
DSCR[1:0] bits	Drive capacity control	L/M/H	L/M/H
NCODR bit	N-ch open-drain	✓	✓
PCR bit	Pull-up	✓	✓
Number of pins	176 pins	✓	✓
	144 pins, 145 pins	-	-
	100 pins	-	-

✓: Available
—: Setting prohibited

Table 20.23 IO引脚功能的寄存器设置(PORT9)

PSEL[4:0] settings	Function	Pin
		P908
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z
00011b	GPT*1	GTIOC12A
01011b	BUS	CS7
11001b	GLCDC	LCD_DATA14_B
ASEL bit		-
ISEL bit		-
DSCR[1:0] bits	驱动容量控制	L/M/H
NCODR bit	N-ch open-drain	✓
PCR bit	Pull-up	✓
引脚数	176 pins	✓
	144 pins, 145 pins	-
	100 pins	-

:可用—:禁止设置

Note 1. 输出缓冲器有两种类型，中驱动和高驱动。Renesas建议使用相同的驱动缓冲器来实现输出偏斜规范(tGTISK)。

Table 20.24 IO引脚功能的寄存器设置(PORTA)

PSEL[4:0] settings	Function	Pin	
		PA00	PA01
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z	
00100b	SCI	TXD8	SCK8
11001b	GLCDC	LCD_DATA05_B	LCD_DATA06_B
ASEL bit		-	-
ISEL bit		-	-
DSCR[1:0] bits	驱动容量控制	L/M/H	L/M/H
NCODR bit	N-ch open-drain	✓	✓
PCR bit	Pull-up	✓	✓
引脚数	176 pins	✓	✓
	144 pins, 145 pins	-	-
	100 pins	-	-

:可用—:禁止设置

Table 20.25 Register settings for I/O pin functions (PORTA)

PSEL[4:0] settings	Function	Pin		
		PA08	PA09	PA10
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z		
11001b	GLCDC	LCD_DATA09_B	LCD_DATA08_B	LCD_DATA07_B
ASEL bit		-	-	-
ISEL bit		-	-	-
DSCR[1:0] bits	Drive capacity control	L/M/H	L/M/H	L/M/H
NCODR bit	N-ch open-drain	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓
Number of pins	176 pins	✓	✓	✓
	144 pins, 145 pins	-	-	-
	100 pins	-	-	-

✓: Available
—: Setting prohibited

Table 20.26 Register settings for I/O pin functions (PORTB)

PSEL[4:0] settings	Function	Pin	
		PB00	PB01
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z	
00101b	SCI	SCK3	CTS3_RTS3/ SS3
10100b	USBHS	USBHS_VBUSEN	USBHS_VBUS
ASEL bit		-	-
ISEL bit		-	-
DSCR[1:0] bits	Drive capacity control	L/M/H	L/M/H
NCODR bit	N-ch open-drain	✓	✓
PCR bit	Pull-up	✓	✓
Number of pins	176 pins	✓	✓
	144 pins, 145 pins	-	-
	100 pins	-	-

✓: Available
—: Setting prohibited

Table 20.25 IO引脚功能的寄存器设置(PORTA)

PSEL[4:0] settings	Function	Pin		
		PA08	PA09	PA10
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z		
11001b	GLCDC	LCD_DATA09_B	LCD_DATA08_B	LCD_DATA07_B
ASEL bit		-	-	-
ISEL bit		-	-	-
DSCR[1:0] bits	驱动容量控制	L/M/H	L/M/H	L/M/H
NCODR bit	N-ch open-drain	✓	✓	✓
PCR bit	Pull-up	✓	✓	✓
引脚数	176 pins	✓	✓	✓
	144 pins, 145 pins	-	-	-
	100 pins	-	-	-

:可用—:禁止设置

Table 20.26 IO引脚功能的寄存器设置(PORTB)

PSEL[4:0] settings	Function	Pin	
		PB00	PB01
00000b (value after reset)	Hi-Z/JTAG/SWD	Hi-Z	
00101b	SCI	SCK3	CTS3_RTS3/ SS3
10100b	USBHS	USBHS_VBUSEN	USBHS_VBUS
ASEL bit		-	-
ISEL bit		-	-
DSCR[1:0] bits	驱动容量控制	L/M/H	L/M/H
NCODR bit	N-ch open-drain	✓	✓
PCR bit	Pull-up	✓	✓
引脚数	176 pins	✓	✓
	144 pins, 145 pins	-	-
	100 pins	-	-

:可用—:禁止设置

21. Key Interrupt Function (KINT)

21.1 Overview

A key interrupt (KEY_INTKR) can be generated by setting the Key Return Mode Register (KRM) and inputting a rising or falling edge on the key interrupt input pins, KR0 to KR7.

Table 21.1 shows the pin assignment for key interrupt detection, Table 21.2 shows the function configuration, and Figure 21.1 shows a block diagram.

Table 21.1 Assignment of key interrupt detection pins

Key Interrupt Mode Control n (n = 0 to 7)	Description
KRM0	Controls KR00 signal in 1-bit units
KRM1	Controls KR01 signal in 1-bit units
KRM2	Controls KR02 signal in 1-bit units
KRM3	Controls KR03 signal in 1-bit units
KRM4	Controls KR04 signal in 1-bit units
KRM5	Controls KR05 signal in 1-bit units
KRM6	Controls KR06 signal in 1-bit units
KRM7	Controls KR07 signal in 1-bit units

Table 21.2 Configuration of key interrupt function

Parameter	Configuration
Input	KR00 to KR07
Control registers	Key Return Control Register (KRCTL) Key Return Mode Register (KRM) Key Return Flag Register (KRF)

21. 按键中断功能(KINT)

21.1 Overview

按键中断(KEY_INTKR)可通过设置按键返回模式寄存器(KRM)并在按键中断输入引脚KR0至KR7上输入上升沿或下降沿来产生。

表21.1显示按键中断检测的引脚分配，表21.2显示功能配置，图21.1显示框图。

Table 21.1 按键中断检测引脚的分配

按键中断模式控制n（n=0到7）	Description
KRM0	以1位为单位控制KR00信号
KRM1	以1位为单位控制KR01信号
KRM2	以1位为单位控制KR02信号
KRM3	以1位为单位控制KR03信号
KRM4	以1位为单位控制KR04信号
KRM5	以1位为单位控制KR05信号
KRM6	以1位为单位控制KR06信号
KRM7	以1位为单位控制KR07信号

Table 21.2 按键中断功能配置

Parameter	Configuration
Input	KR00 to KR07
控制寄存器	密钥返回控制寄存器(KRCTL) 密钥返回模式寄存器(KRM) 密钥返回标志寄存器(KRF)

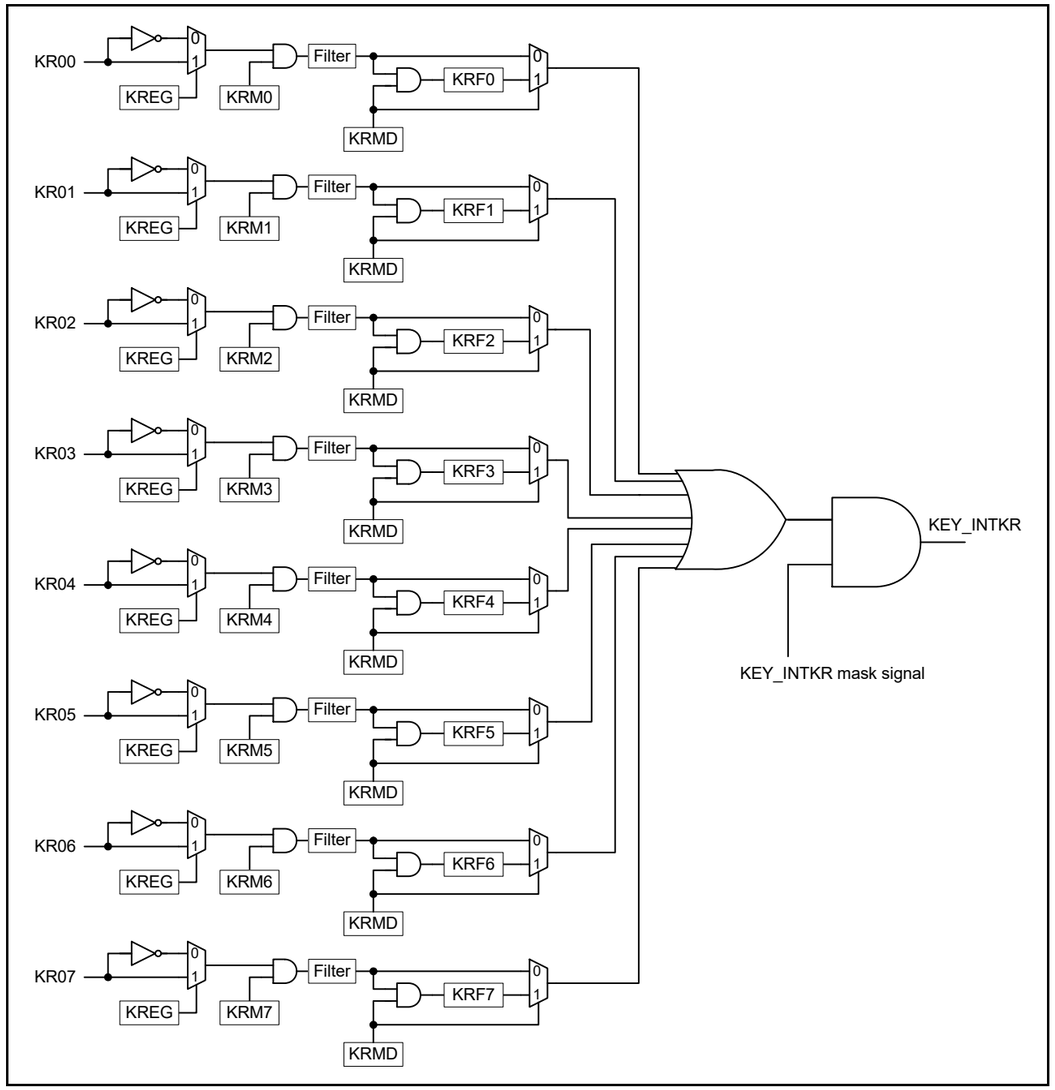


Figure 21.1 Key interrupt block diagram

All key return factors are merged by OR gate. The key interrupt KEY_INTKR is the output of the AND gate to mask merged key return factor by KEY_INTKR mask signal. When using KRFn (KRMD = 1), KEY_INTKR mask signal is used as the output mask that is asserted by clearing KRFn.

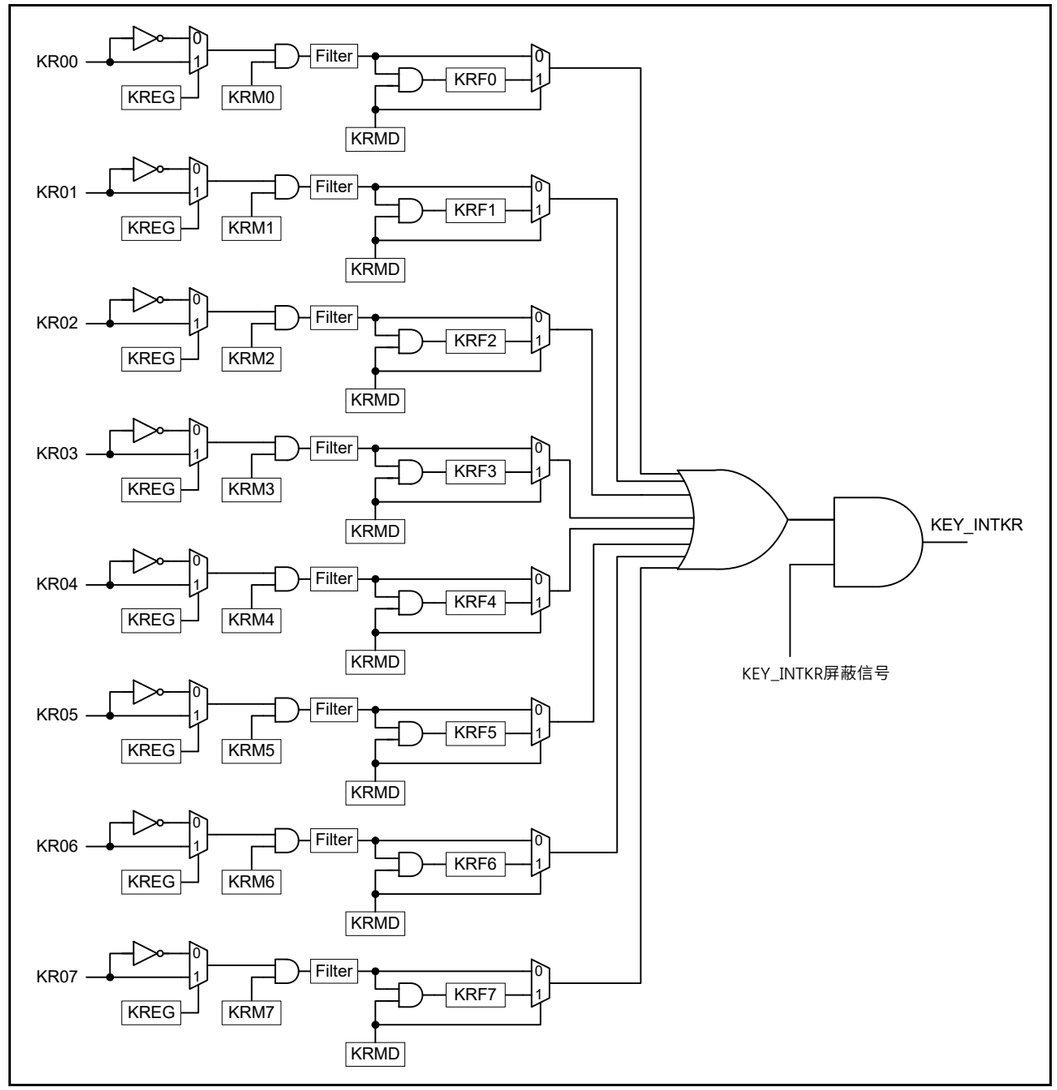


Figure 21.1 按键中断框图

所有关键的回报因素都由或门合并。键中断KEY_INTKR是与门的输出，用于通过KEY_INTKR屏蔽信号屏蔽合并的键返回因子。使用KRFn(KRMD=1)时，KEY_INTKR屏蔽信号用作通过清除KRFn来断言的输出屏蔽。

21.2 Register Descriptions

21.2.1 Key Return Control Register (KRCTL)

Address(es): KINT.KRCTL 4008 0000h

	b7	b6	b5	b4	b3	b2	b1	b0
	KRMD	—	—	—	—	—	—	KREG
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	KREG	Detection Edge Selection (KR00 to KR07)	0: Falling edge 1: Rising edge.	R/W
b6 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	KRMD	Usage of Key Interrupt Flags (KRF0 to KRF7)	0: Do not use key interrupt flags 1: Use key interrupt flags.	R/W

The KRCTL register controls the usage of the key interrupt flags, KRF0 to KRF7, and sets the detection edge.

21.2.2 Key Return Flag Register (KRF)

Address(es): KINT.KRF 4008 0004h

	b7	b6	b5	b4	b3	b2	b1	b0
	KRF7	KRF6	KRF5	KRF4	KRF3	KRF2	KRF1	KRF0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	KRFn	Key Interrupt Flag n	0: No key interrupt detected 1: Key interrupt detected.	R/W

n = 0 to 7

Note: When KRMD = 0, setting the KRFn bit to 1 is prohibited.
When setting the KRFn bit to 1, the KRFn value does not change. To clear the KRFn bit, confirm the target bit is 1 before writing 0 to the bit, then write 1 to the other bits.

The KRF register controls the key interrupt flags, KRF0 to KRF7.

21.2.3 Key Return Mode Register (KRM)

Address(es): KINT.KRM 4008 0008h

	b7	b6	b5	b4	b3	b2	b1	b0
	KRM7	KRM6	KRM5	KRM4	KRM3	KRM2	KRM1	KRM0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	KRMn	Key Interrupt Mode Control n	0: No key interrupt signal detected 1: Key interrupt signal detected.	R/W

n = 0 to 7

21.2 注册说明

21.2.1 密钥返回控制寄存器(KRCTL)

Address(es): KINT.KRCTL 4008 0000h

	b7	b6	b5	b4	b3	b2	b1	b0
	KRMD	—	—	—	—	—	—	KREG
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	KREG	检测边缘选择（KR00至KR07）	0：下降沿1：上升沿。	R/W
b6 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b7	KRMD	按键中断标志（KRF0到KRF7）的使用	0：不使用按键中断标志1：使用按键中断标志。	R/W

KRCTL寄存器控制按键中断标志KRF0到KRF7的使用，并设置检测沿。

21.2.2 密钥返回标志寄存器(KRF)

Address(es): KINT.KRF 4008 0004h

	b7	b6	b5	b4	b3	b2	b1	b0
	KRF7	KRF6	KRF5	KRF4	KRF3	KRF2	KRF1	KRF0
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b7 to b0	KRFn	按键中断标志n	0：未检测到按键中断1：检测到按键中断。	R/W

n = 0 to 7

Note: 当KRMD=0时，禁止将KRFn位设置为1。
将KRFn位设置为1时，KRFn值不变。要清除KRFn位，在向该位写入0之前确认目标位为1，然后向其他位写入1。

KRF寄存器控制关键中断标志，KRF0到KRF7。

21.2.3 密钥返回模式寄存器(KRM)

Address(es): KINT.KRM 4008 0008h

	b7	b6	b5	b4	b3	b2	b1	b0
	KRM7	KRM6	KRM5	KRM4	KRM3	KRM2	KRM1	KRM0
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b7 to b0	KRMn	按键中断模式控制n	0：未检测到按键中断信号1：检测到按键中断信号。	R/W

n = 0 to 7

Note: The on-chip pull-up resistors can be applied by setting the pull-up function for the associated key interrupt input pin. For more information, see section 20, I/O Ports.
Key interrupts can be assigned in the PmnPFS.PSEL bits. For more information, see section 20, I/O Ports.
An interrupt is generated when the target bit in the KRM register is set while a low level (KREG = 0) or a high level (KREG = 1) is being input to the key interrupt input pin. To ignore this interrupt, set the KRM register after disabling the interrupt handling.

The KRM register sets the key interrupt mode.

21.3 Operation

21.3.1 Operation When Not Using Key Interrupt Flag (KRMD = 0)

A key interrupt (KEY_INTKR) is generated when the valid edge specified in the KREG bit is input to a key interrupt pin, KR00 to KR07. To identify the channel to which the valid edge is input, read the port register and check the port level after the key interrupt (KEY_INTKR) is generated.

The KEY_INTKR signal changes based on the input level of the key interrupt input pin, KR00 to KR07.

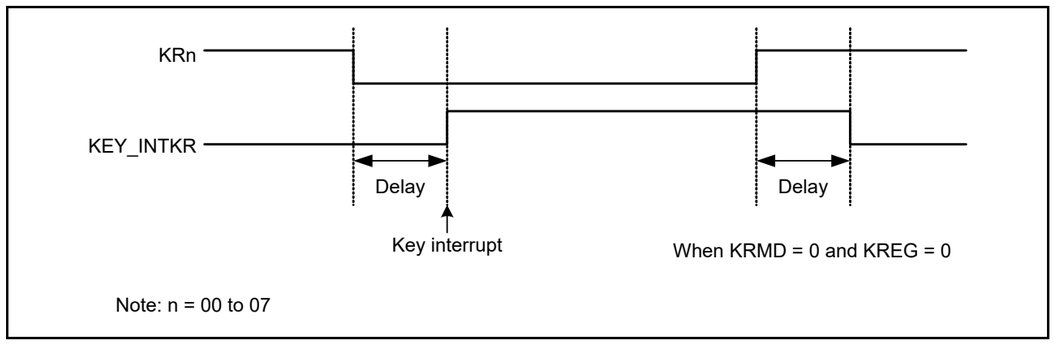


Figure 21.2 Operation of KEY_INTKR signal when a key interrupt is input to a single channel

Figure 21.3 shows the operation when a valid edge is input to multiple key interrupt input pins. The KEY_INTKR signal is set while a low level is being input to one pin (when KREG = 0). Therefore, even if a falling edge is input to another pin in this period, a key interrupt (KEY_INTKR) is not generated again. See [1] in Figure 21.3.

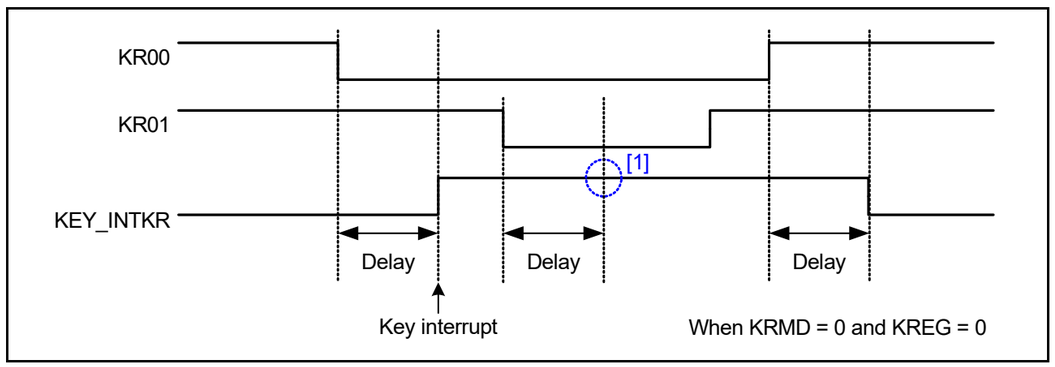


Figure 21.3 Operation of KEY_INTKR signal when key interrupts are input to multiple channels

21.3.2 Operation When Using the Key Interrupt Flags (KRMD = 1)

A key interrupt (KEY_INTKR) is generated when the valid edge specified in the KREG bit is input to a key interrupt pin, KR00 to KR07. To identify the channels to which the valid edge is input, read the Key Return Flag Register (KRF) after the key interrupt (KEY_INTKR) is generated. If the KRMD bit is set to 1, clear the KEY_INTKR signal by clearing the associated bit in the KRF register.

Note: 可以通过设置相关按键中断输入引脚的上拉功能来应用片上上拉电阻。有关详细信息，请参阅第20节，IO端口。可以在PmnPFS.PSEL位中分配键中断。有关详细信息，请参阅第20节，IO端口。

当低电平(KREG=0)或高电平(KREG=1)被输入到按键中断输入引脚时，如果KRM寄存器中的目标位被置位，就会产生中断。要忽略此中断，请在禁用中断处理后设置KRM寄存器。

KRM寄存器设置按键中断模式。

21.3 Operation

21.3.1 不使用按键中断标志(KRMD=0)时的操作

当KREG位中指定的有效边沿输入到按键中断引脚时，将产生按键中断(KEY_INTKR)，KR00至KR07。要识别输入有效边沿的通道，读取端口寄存器并在按键中断（KEY_INTKR）产生后检查端口电平。

KEY_INTKR信号根据按键中断输入引脚KR00至KR07的输入电平而变化。

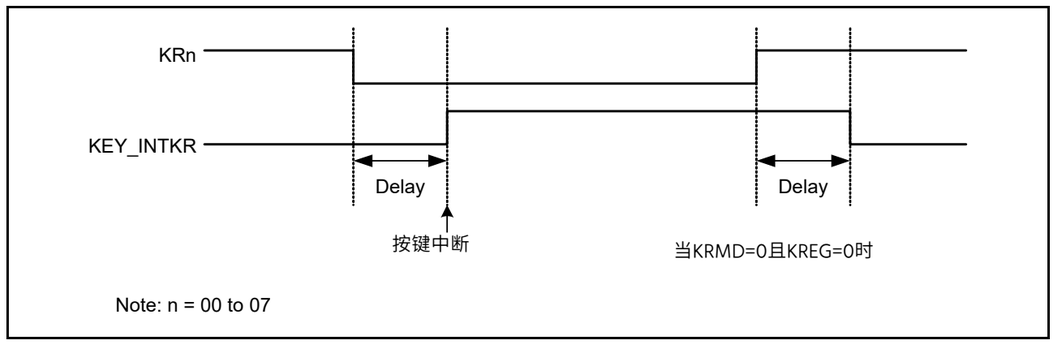


Figure 21.2 按键中断输入到单通道时KEY_INTKR信号的操作

图21.3显示了向多个按键中断输入引脚输入有效边沿时的操作。KEY_INTKR信号在低电平输入到一个引脚时设置（当KREG=0时）。因此，即使在此期间向另一个引脚输入下降沿，也不会再次产生按键中断（KEY_INTKR）。参见图21.3中的[1]。

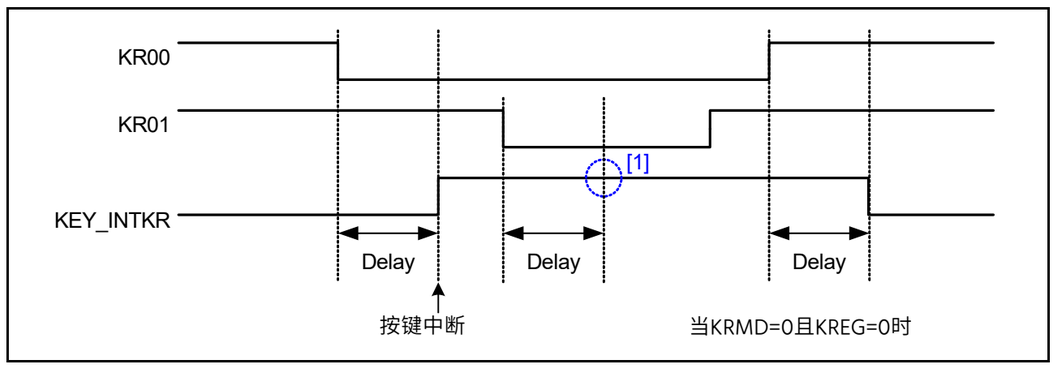


Figure 21.3 按键中断输入到多个通道时KEY_INTKR信号的操作

21.3.2 使用按键中断标志(KRMD=1)时的操作

当KREG位中指定的有效边沿输入到按键中断引脚KR00至KR07时，将产生按键中断(KEY_INTKR)。要识别输入有效边沿的通道，请在生成按键中断(KEY_INTKR)后读取按键返回标志寄存器(KRF)。如果KRMD位设置为1，则通过清除KRF寄存器中的相关位来清除KEY_INTKR信号。

As Figure 21.4 shows, only one interrupt is generated each time a falling edge is input to one channel, that is, when KREG = 0, regardless of whether the KRFn bit is cleared before or after a rising edge is input.

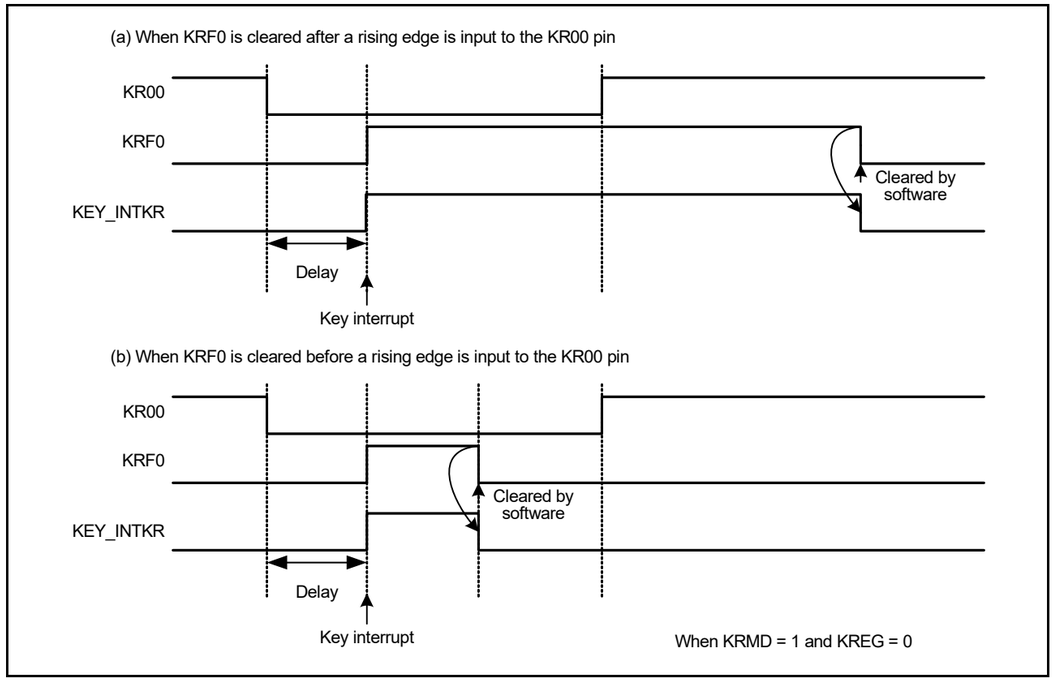


Figure 21.4 Basic operation of KEY_INTKR signal when key interrupt flag is used

The operation when a valid edge is input to multiple key interrupt input pins is shown in Figure 21.5. A falling edge is also input to the KR01 and KR05 pins after a falling edge is input to the KR00 pin (when KREG = 0). The KRF1 bit is set when the KRF0 bit is cleared. A key interrupt is generated 1 PCLKB clock cycle, after the KRF0 bit is cleared. See [1] in Figure 21.5.

Also, after a falling edge is input to the KR05 pin, the KRF5 bit is set. The KRF1 bit is cleared at time [2] in the figure. A key interrupt is generated 1 PCLKB clock cycle, after the KRF1 bit is cleared. See [3] in the figure. It is therefore possible to generate a key interrupt when a valid edge is input to multiple channels.

如图21.4所示，每次下降沿输入到一个通道时，只产生一个中断，即当KREG=0，无论KRFn位是在输入上升沿之前还是之后清零。

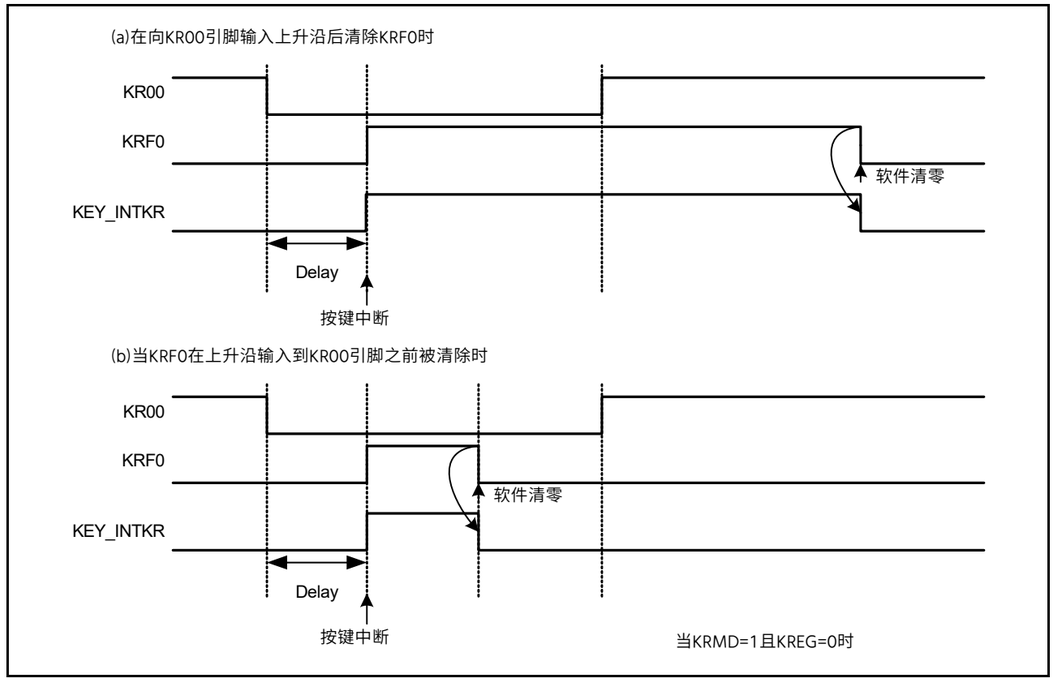


Figure 21.4 使用按键中断标志时KEY_INTKR信号的基本操作

有效边沿输入到多个按键中断输入引脚时的操作如图21.5所示。在向KR00引脚输入下降沿之后（当KREG=0时），也会向KR01和KR05引脚输入一个下降沿。当KRF0位被清零时，KRF1位被置位。在KRF0位清零后，1个PCLKB时钟周期产生一个按键中断。请参见图21.5中的[1]。

此外，在向KR05引脚输入下降沿后，KRF5位被置位。KRF1位在图中的时间[2]处被清除。在KRF1位清零后，1个PCLKB时钟周期产生一个按键中断。见图[3]。因此，当有效边沿输入到多个通道时，可能会产生按键中断。

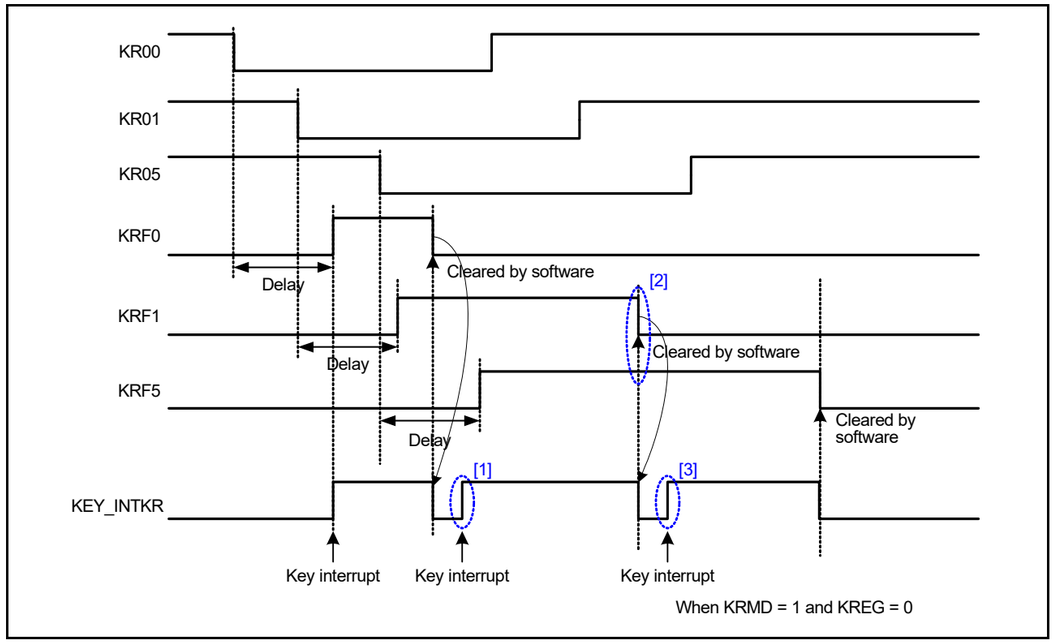


Figure 21.5 Operation of KEY_INTKR signal when key interrupts are input to multiple channels

21.4 Usage Notes

- If KEY_INTKR is used as the Snooze request, the KRMD bit must be set to 0.
- If KEY_INTKR is used as the interrupt source for returning to Normal mode from Snooze mode and Software Standby mode, the KRMD bit must be set to 1.
- When the Key Interrupt function (KINT) is assigned to a pin, this pin input is always enabled in Software Standby mode, and if the pin level changes, the associated KRFn flag can be set. Therefore, a key interrupt might occur on canceling Software Standby mode.

To ignore changes to the key interrupt pin during a software standby, clear the associated KRM bit before entering Software Standby mode. After canceling Software Standby mode, you must clear KRFn before the associated KRM bit can be set.

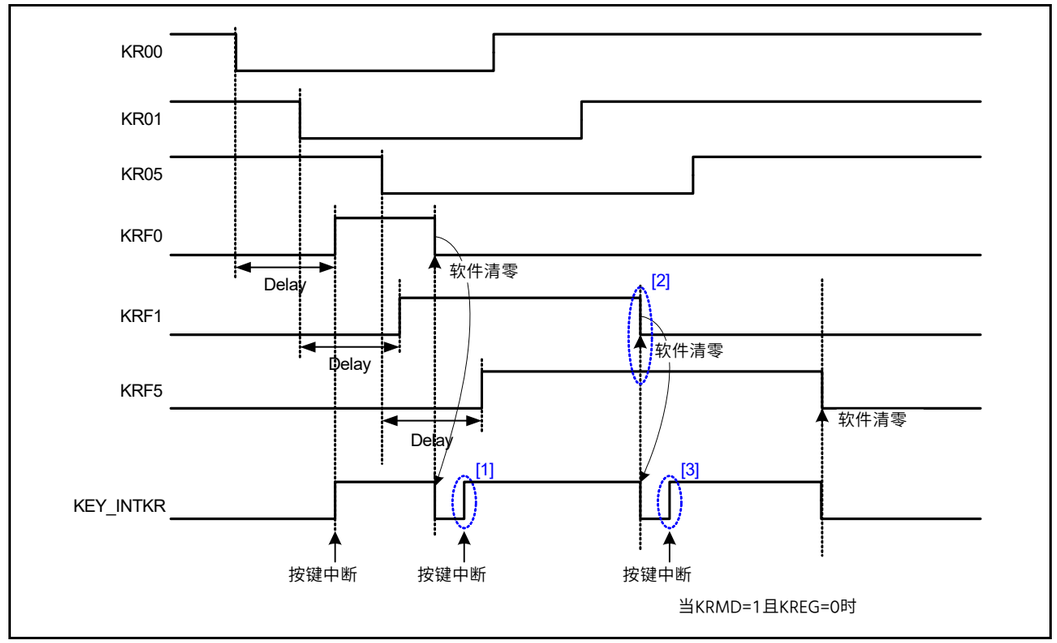


Figure 21.5 按键中断输入到多个通道时KEY_INTKR信号的操作

21.4 使用说明

- 如果KEY_INTKR用作贪睡请求，则KRMD位必须设置为0。
- 如果KEY_INTKR用作从贪睡模式和软件返回正常模式的中断源
  待机模式下，KRMD位必须设置为1。
- 当按键中断功能(KINT)分配给某个引脚时，该引脚输入始终在软件待机模式下启用，如果引脚电平发生变化，则可以设置相关的KRFn标志。因此，取消软件待机模式时可能会发生按键中断。

要在软件待机期间忽略对键中断引脚的更改，请在进入之前清除相关的KRM位
软件待机模式。取消软件待机模式后，必须先清除KRFn，然后才能设置相关的KRM位。

22. Port Output Enable for GPT (POEG)

22.1 Overview

Use the Port Output Enable for GPT (POEG) function to place the General PWM Timer (GPT) output pins in the output-disable state in one of the following ways:

- Input level detection of the GTETRGn (n = A, B, C, D) pins
- Output-disable request from the GPT
- Comparator interrupt request detection
- Oscillation stop detection of the clock generation circuit
- Register settings.

The GTETRGn (n = A, B, C, D) pins can also be used as GPT external trigger input pins.

Table 22.1 lists the POEG specifications, Figure 22.1 shows a block diagram, and Table 22.2 lists the input pins.

Table 22.1 POEG specifications

Parameter	Specifications
Output-disable control through input level detection	The GPT output pins can be disabled when a GTETRGn rising edge or high level is sampled after polarity and filter selection
Output-disable request from the GPT	• When the GTIOCA pin and the GTIOCB pin are driven to an active level simultaneously, the GPT generates an output-disable request to the POEG.Through reception of these requests, the POEG can control whether the GTIOCA and GTIOCB pins are output-disabled. • GPT output pins can be set to be disabled when the GPT output pins detect a dead time error.
Output-disable control through comparator (ACMPHS) interrupt detection	The GPT output pins can be disabled when an interrupt request is generated by a change in the output results of any of the comparators
Output-disable control through oscillation stop detection	The GPT output pins can be disabled when oscillation of the clock generation circuit stops
Output-disable control by software (registers)	The GPT output pins can be disabled by modifying the register settings
Interrupt	• Allows output-disable control by input level detection • Allows output-disable requests from the GPT or ACMPHS.
External trigger output to the GPT (count start, count stop, count clear, up-count, down-count, or input capture function)	The GTETRGn signals can be output to the GPT after polarity and filter selection
Noise filtering	• Three times sampling for every PCLKB/1, PCLKB/8, PCLKB/32, or PCLKB/128 can be set for any of the input pins GTETRGn • Positive or negative polarity can be selected for any of the input pins, GTETRGn • Signal state after polarity and filter selection can be monitored.

22. GPT(POEG)的端口输出使能

22.1 Overview

使用PortOutputEnableforGPT(POEG)功能可通过以下方式之一将通用PWM定时器(GPT)输出引脚置于输出禁用状态：

- GTETRn(n=A B C D)引脚的输入电平检测
- 来自GPT的输出禁用请求
- 比较器中断请求检测
- 时钟发生电路的振荡停止检测
- 注册设置。

GTETRn(n=A B C D)引脚也可用作GPT外部触发输入引脚。

表22.1列出了POEG规范，图22.1显示了框图，表22.2列出了输入引脚。

Table 22.1 POEG specifications

Parameter	Specifications
通过输入电平检测进行输出禁用控制	在极性和滤波器选择后采样GTETRn上升沿或高电平时，可以禁用GPT输出引脚
来自GPT的输出禁用请求	当GTIOCA引脚和GTIOCB引脚被驱动为有效电平时 同时，GPT向POEG产生一个输出禁止请求。通过接收这些请求，POEG可以控制GTIOCA和GTIOCB引脚是否禁止输出。 当GPT输出引脚检测到死区时间错误时，可以将GPT输出引脚设置为禁用。
通过比较器(ACMPHS)中断检测进行输出禁用控制	当任何比较器的输出结果发生变化而产生中断请求时，可以禁用GPT输出引脚
通过振荡停止检测进行输出禁用控制	当时钟生成电路的振荡停止时，可以禁用GPT输出引脚
通过软件（寄存器）进行输出禁用控制	可以通过修改寄存器设置来禁用GPT输出引脚
Interrupt	允许通过输入电平检测进行输出禁用控制 允许来自GPT或ACMPHS的输出禁用请求。
到GPT的外部触发输出（计数开始、计数停止、计数清除、递增计数、递减计数或输入捕捉功能）	GTETRn信号可在极性和滤波器选择后输出到GPT
噪声过滤	可以为任何输入引脚GTETRGn设置每个PCLKB1、PCLKB8、PCLKB32或PCLKB128的三次采样 可以为任何输入引脚GTETRGn选择正极性或负极性 极性后的信号状态可以监控过滤器的选择。

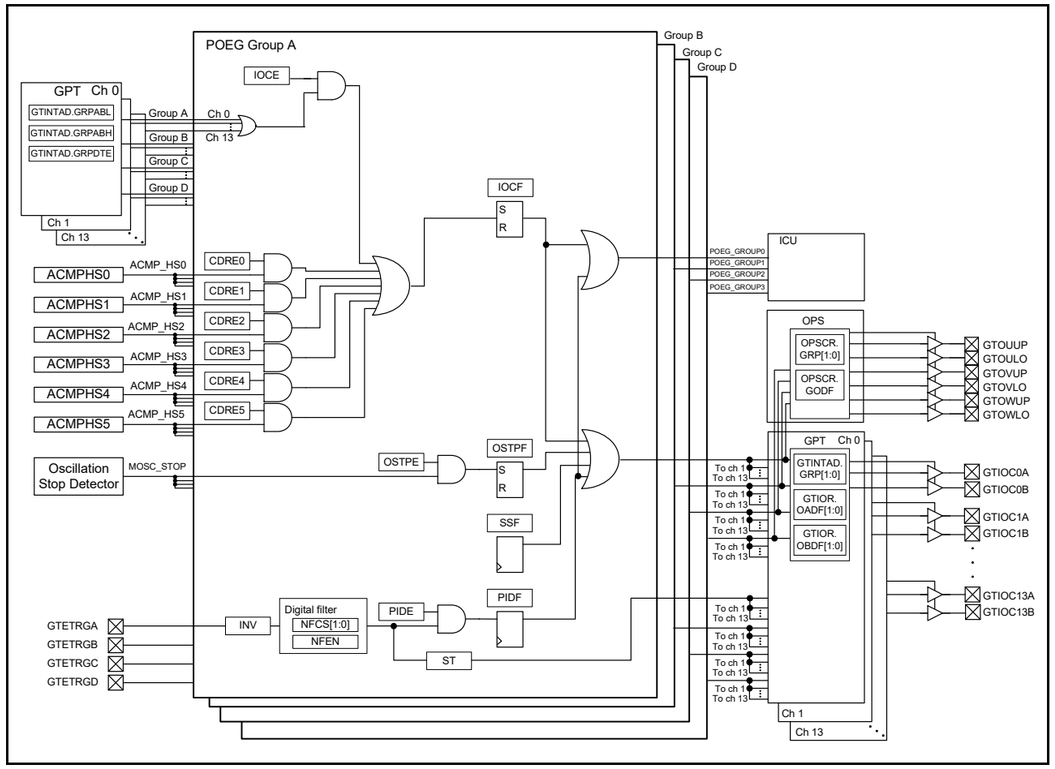


Figure 22.1 POEG block diagram

Table 22.2 POEG input pins

Pin name	I/O	Description
GTETRGA	Input	GPT output pin output-disable request signal and GPT external trigger input pin A
GTETRGB	Input	GPT output pin output-disable request signal and GPT external trigger input pin B
GTETRGC	Input	GPT output pin output-disable request signal and GPT external trigger input pin C
GTETRGD	Input	GPT output pin output-disable request signal and GPT external trigger input pin D

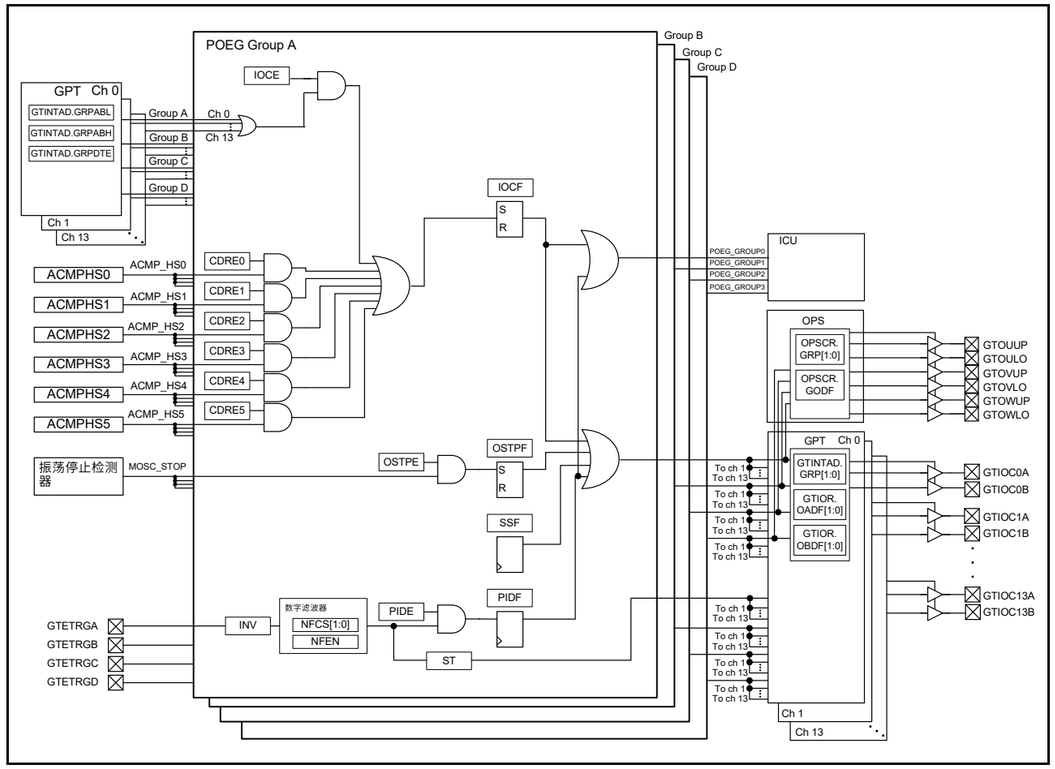


Figure 22.1 POEG框图

Table 22.2 POEG输入引脚

引脚名称	I/O	Description
GTETRGA	Input	GPT输出引脚输出禁止请求信号和GPT外部触发输入引脚A
GTETRGB	Input	GPT输出引脚输出禁止请求信号和GPT外部触发输入引脚B
GTETRGC	Input	GPT输出引脚输出禁止请求信号和GPT外部触发输入引脚C
GTETRGD	Input	GPT输出引脚输出禁止请求信号和GPT外部触发输入引脚D

22.2 Register Descriptions

22.2.1 POEG Group n Setting Register (POEGGn) (n = A to D)

Address(es): POEG.POEGGA 4004 2000h, POEG.POEGGB 4004 2100h, POEG.POEGGC 4004 2200h, POEG.POEGGD 4004 2300h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	NFCS[1:0]		NFEN	INV	—	—	—	—	—	—	—	—	—	—	—	ST
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	CDRE5	CDRE4	CDRE3	CDRE2	CDRE1	CDRE0	—	OSTPE	IOCE	PIDE	SSF	OSTPF	IOCF	PIDF
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	PIDF	Port Input Detection Flag	0: No output-disable request from the GTETRGn pin occurred 1: Output-disable request from the GTETRGn pin occurred.	R(/W)*1
b1	IOCF	Detection Flag for GPT or ACMPHS Output-Disable Request	0: No output-disable request from GPT disable request or comparator interrupt occurred 1: Output-disable request from GPT disable request or comparator interrupt occurred.	R(/W)*1
b2	OSTPF	Oscillation Stop Detection Flag	0: No output-disable request from oscillation stop detection occurred 1: Output-disable request from oscillation stop detection occurred.	R(/W)*1
b3	SSF	Software Stop Flag	0: No output-disable request from software occurred 1: Output-disable request from software occurred.	R/W
b4	PIDE	Port Input Detection Enable	0: Output-disable requests from the GTETRGn pins disabled 1: Output-disable requests from the GTETRGn pins enabled.	R/W*2
b5	IOCE	Enable for GPT Output-Disable Request	0: Output-disable requests from GPT disable request disabled 1: Output-disable requests from GPT disable request enabled.	R/W*2
b6	OSTPE	Oscillation Stop Detection Enable	0: Output-disable requests from oscillation stop detection disabled 1: Output-disable requests from oscillation stop detection enabled.	R/W*2
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b8	CDRE0	ACMP_HS0 Enable	0: Comparator 0 disable requests disabled 1: Comparator 0 disable requests enabled.	R/W*2
b9	CDRE1	ACMP_HS1 Enable	0: Comparator 1 disable requests disabled 1: Comparator 1 disable requests enabled.	R/W*2
b10	CDRE2	ACMP_HS2 Enable	0: Comparator 2 disable requests disabled 1: Comparator 2 disable requests enabled.	R/W*2
b11	CDRE3	ACMP_HS3 Enable	0: Comparator 3 disable requests disabled 1: Comparator 3 disable requests enabled.	R/W*2
b12	CDRE4	ACMP_HS4 Enable	0: Comparator 4 disable requests disabled 1: Comparator 4 disable requests enabled.	R/W*2
b13	CDRE5	ACMP_HS5 Enable	0: Comparator 5 disable requests disabled 1: Comparator 5 disable requests enabled.	R/W*2
b15, b14	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b16	ST	GTETRGn Input Status Flag	0: GTETRGn input after filtering was 0 1: GTETRGn input after filtering was 1.	R
b27 to b17	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b28	INV	GTETRGn Input Reverse	0: Input GTETRGn as-is 1: Input GTETRGn reversed.	R/W
b29	NFEN	Noise Filter Enable	0: Noise filtering disabled 1: Noise filtering enabled.	R/W

22.2 注册说明

22.2.1 POEG组n设置寄存器(POEGGn)(n=A到D)

Address(es): POEG.POEGGA 4004 2000h, POEG.POEGGB 4004 2100h, POEG.POEGGC 4004 2200h, POEG.POEGGD 4004 2300h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	NFCS[1:0]		NFEN	INV	—	—	—	—	—	—	—	—	—	—	—	ST
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	CDRE5	CDRE4	CDRE3	CDRE2	CDRE1	CDRE0	—	OSTPE	IOCE	PIDE	SSF	OSTPF	IOCF	PIDF
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	PIDF	端口输入检测标志	0：未发生来自GTETRn引脚的输出禁止请求1：发生了来自GTETRn引脚的输出禁止请求。	R(/W)*1
b1	IOCF	GPT或ACMPHS输出禁用检测标志 Request	0：没有来自GPT禁止请求或比较器中断的输出禁止请求1：来自GPT禁止请求或比较器中断的输出禁止请求。	R(/W)*1
b2	OSTPF	振荡停止检测 Flag	0：未发生振荡停止检测的输出禁止请求1：发生了振荡停止检测的输出禁止请求。	R(/W)*1
b3	SSF	软件停止标志	0：没有来自软件的输出禁止请求1：有来自软件的输出禁止请求。	R/W
b4	PIDE	端口输入检测启用	0：禁止来自GTETRn引脚的输出禁止请求1：允许来自GTETRn引脚的输出禁止请求。	R/W*2
b5	IOCE	启用GPT输出禁用请求	0：禁用来自GPT的输出禁用请求禁用请求1：启用来自GPT禁用请求的输出禁用请求。	R/W*2
b6	OSTPE	振荡停止检测 Enable	0：禁止来自振荡停止检测的输出禁止请求1：允许来自振荡停止检测的输出禁止请求。	R/W*2
b7	—	Reserved	该位读取为0。写入值应为0。	R/W
b8	CDRE0	ACMP_HS0 Enable	0：比较器0禁用请求禁用1：比较器0禁用请求启用。	R/W*2
b9	CDRE1	ACMP_HS1 Enable	0：比较器1禁用请求禁用1：比较器1禁用请求启用。	R/W*2
b10	CDRE2	ACMP_HS2 Enable	0：比较器2禁用请求禁用1：比较器2禁用请求启用。	R/W*2
b11	CDRE3	ACMP_HS3 Enable	0：比较器3禁用请求禁用1：比较器3禁用请求启用。	R/W*2
b12	CDRE4	ACMP_HS4 Enable	0：比较器4禁用请求禁用1：比较器4禁用请求启用。	R/W*2
b13	CDRE5	ACMP_HS5 Enable	0：比较器5禁用请求禁用1：比较器5禁用请求启用。	R/W*2
b15, b14	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b16	ST	GTETRn输入状态标志	0：滤波后的GTETRn输入为01：滤波后的GTETRn输入为1。	R
b27 to b17	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b28	INV	GTETRn输入反向	0：按原样输入GTETRn1：输入GTETRn反转。	R/W
b29	NFEN	噪声过滤器启用	0：禁用噪声过滤1：启用噪声过滤。	R/W

Bit	Symbol	Bit name	Description	R/W
b31, b30	NFCS[1:0]	Noise Filter Clock Select	b1 b0 0 0: GTETRGn pin input level sampled three times every PCLKB 0 1: GTETRGn pin input level sampled three times every PCLKB/8 1 0: GTETRGn pin input level sampled three times every PCLKB/32 1 1: GTETRGn pin input level sampled three times every PCLKB/128.	R/W

Note 1. Only 0 can be written, to clear the flag.
Note 2. Can be modified only once after a reset.

The POEGGA to POEGGD registers control the output-disable state of the GPT pins, interrupts, and the external trigger input to the GPT. In the descriptions, POEGGn represents all of the POEGGA to POEGGD registers.

22.3 Output-Disable Control Operation

If any of the following conditions is satisfied, the GTIOCxA, GTIOCxB, and the 3-phase PWM output for BLDC motor control pins can be set to output-disable:

- Input level or edge detection of the GTETRGn pins
  When POEGGn.PIDE is 1, the POEGGn.PIDF flag is set to 1.
- Output-disable request from the GPT
  When POEGGn.IOCE is 1, the POEGGn.IOCF flag is set to 1 if the disable request is enabled in the GTINTAD register. The GTINTAD.GRPDTE, GTINTAD.GRPABH, and GTINTAD.GRPABL settings apply to the group selected in the GPT registers GTINTAD.GRP[1:0] and OPSCR.GRP[1:0].
- Comparator (ACMPHS) interrupt request detection
  Comparator interrupt detection is activated when any of the POEGGn.CDRE[5:0] registers is 1. When the associated comparator interrupt is generated, the GPT output pins are disabled. POEGGn.IOCF indicates the detection status.
- Oscillation stop detection for the clock generation circuit
  When POEGGn.OSTPE is 1, the POEGGn.OSTPF flag is set to 1.
- SSF bit setting
  When POEGGn.SSF is set to 1, the PWM output is disabled.

The output-disable state is controlled in the GPT. The output-disable of the GTIOCxA and GTIOCxB pins is set in the GTINTAD.GRP[1:0], GTIOR.OADF[1:0], and GTIOR.OBDF[1:0] bits in GPTx. The output-disable of the 3-phase PWM output for BLDC motor control pins is set in the OPSCR.GRP[1:0] bits and OPSCR.GODF bit in GPT_OPS.

22.3.1 Pin Input Level Detection Operation

If the input conditions set in POEGGn.PIDE, POEGGn.NFCS[1:0], POEGGn.NFEN, and POEGGn.INV occur on the GTETRGn pins, the GPT output pins are output-disabled.

22.3.1.1 Digital filter

Figure 22.2 shows high level detection by the digital filter. When a high level associated with the POEGGn.INV polarity setting is detected three times consecutively with the sampling clock selected in POEGGn.NFCS[1:0] and POEGGn.NFEN, the detected level is recognized as high, and the GPT output pins are output-disabled. If even one low level is detected during this interval, the detected level is not recognized as high. In addition, in an interval where the sampling clock is not being output, changes of the levels on the GTETRGn pins are ignored.

Bit	Symbol	位名称	Description	R/W
b31, b30	NFCS[1:0]	噪声滤波器时钟选择	b1b000：GTETRn引脚输入电平每PCLKB采样3次01：GTETRn引脚输入电平每PCLKB采样3次810：GTETRn引脚输入电平每PCLKB采样3次3211：GTETRn引脚输入电平采样3次每个PCLKB128。	R/W

Note 1. 只能写入0，以清除标志。
Note 2. 重置后只能修改一次。

POEGGA到POEGGD寄存器控制GPT引脚的输出禁用状态、中断和GPT的外部触发输入。在描述中，POEGGn代表所有的POEGGA到POEGGD寄存器。

22.3 输出禁用控制操作

如果满足以下任一条件，则GTIOCxA、GTIOCxB和BLDC电机控制引脚的3相PWM输出可设置为输出禁用：

- GTETRn引脚的输入电平或边沿检测
  当POEGGn.PIDE为1时，POEGGn.PIDF标志设置为1。
- 来自GPT的输出禁用请求
  当POEGGn.IOCE为1时，如果在GTINTAD寄存器中启用了禁用请求，则POEGGn.IOCF标志设置为1。GTINTAD.GRPDTE、GTINTAD.GRPABH和GTINTAD.GRPABL设置适用于在GPT寄存器GTINTAD.GRP[1:0]和OPSCR.GRP[1:0]中选择的组。
- 比较器(ACMPHS)中断请求检测
  当任何POEGGn.CDRE[5:0]寄存器为1时，比较器中断检测被激活。当相关的比较器中断产生时，GPT输出引脚被禁用。POEGGn.IOCF指示检测状态。
- 时钟发生电路的振荡停止检测
  当POEGGn.OSTPE为1时，POEGGn.OSTPF标志设置为1。
- SSF位设置
  当POEGGn.SSF设置为1时，PWM输出被禁用。

输出禁用状态由GPT控制。GTIOCxA和GTIOCxB引脚的输出禁用设置在GPTx中的GTINTAD.GRP[1:0]、GTIOR.OADF[1:0]和GTIOR.OBDF[1:0]位。BLDC电机控制引脚的3相PWM输出的输出禁用在GPT_OPS中的OPSCR.GRP[1:0]位和OPSCR.GODF位中设置。

22.3.1 引脚输入电平检测操作

如果在POEGGn.PIDE、POEGGn.NFCS[1:0]、POEGGn.NFEN和POEGGn.INV中设置的输入条件发生在GTETRn引脚，GPT输出引脚输出禁用。

22.3.1.1 数字滤波器

图22.2显示了数字滤波器的高电平检测。当在POEGGn.NFCS[1:0]和POEGGn.NFEN中选择的采样时钟连续3次检测到与POEGGn.INV极性设置相关的高电平时，检测到的电平被识别为高电平，并且GPT输出引脚为输出禁用。如果在此间隔期间甚至检测到一个低电平，则检测到的电平不会被识别为高电平。此外，在不输出采样时钟的时间间隔内，GTETRn引脚上的电平变化将被忽略。

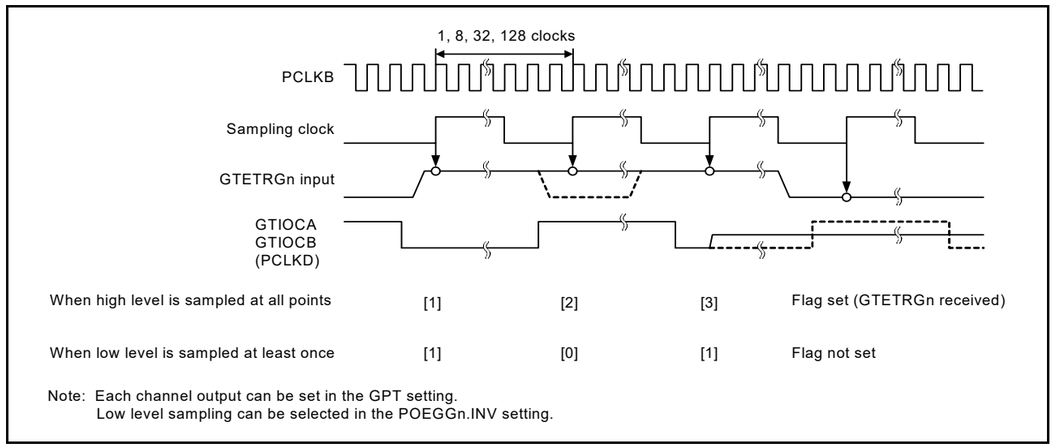


Figure 22.2 Example of digital filter operation

22.3.2 Output-Disable Requests from the GPT

For details on this operation, see the description of GTIOC Pin Output Negate Control in section 23, General PWM Timer (GPT).

22.3.3 Comparator Interrupt Detection

If POEGGn.CDRE[5:0] is 1 when an associated comparator interrupt request is generated, the GPT output pins are output-disabled for each group. The status flag is POEGGn.IOCF, which is shared with GPT output-disable detection.

22.3.4 Output-Disable Control Using Detection of Stopped Oscillation

When the oscillation stop detection function in the clock generation circuit detects stopped oscillation while POEGGn.OSTPE is 1, the GPT output pins are output-disabled for each group.

22.3.5 Output-Disable Control Using Registers

The GPT output pins can be directly controlled by writing to the Software Stop flag, POEGGn.SSF.

22.3.6 Release from Output-Disable

To release the GPT output pins placed in the output-disable state, either return them to their initial state with a reset or clear all of the following flags:

- POEGGn.PIDF
- POEGGn.IOCF
- POEGGn.OSTPF
- POEGGn.SSF.

Writing 0 to the POEGGn.PIDF flag is ignored (the flag is not cleared) if the external input pins, GTETRGn, are not disabled and the POEGGn.ST bit is not set to 0.

Writing 0 to the POEGGn.IOCF flag is valid (the flag is cleared) only if all of the GTST.DTEF, GTST.OABHF, and GTST.OABLF flags in the GPT are set to 0.

Writing 0 to the POEGGn.OSTPF flag is ignored (the flag is not cleared) if the OSTDSR.OSTDF flag in the clock generation circuit is not set to 0. In addition, when the flag set and release occur at the same time, the flag set takes precedence.

Figure 22.3 shows the release timing for output-disable. The output-disable is released at the beginning of the next count cycle of the GPT after the flag is cleared.

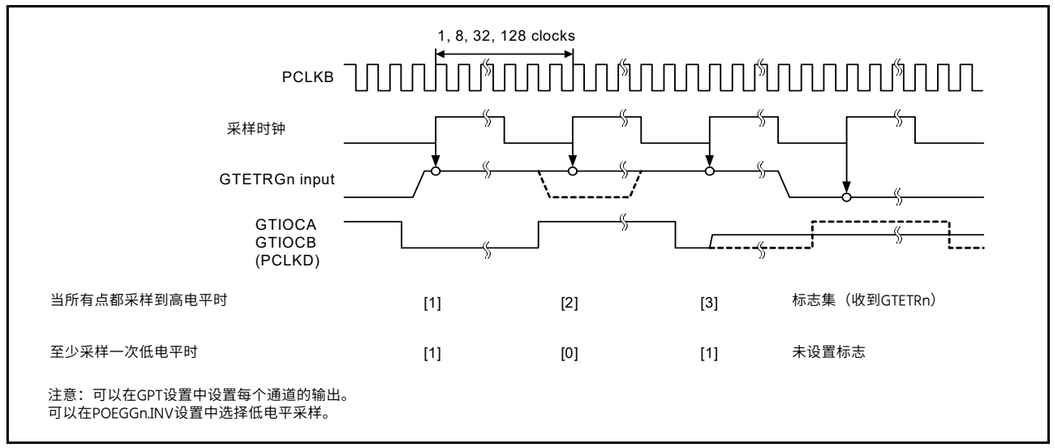


Figure 22.2 数字滤波器操作示例

22.3.2 来自GPT的输出禁用请求

有关此操作的详细信息，请参见第23节通用PWM中GTIOC引脚输出负控制的描述
Timer (GPT).

22.3.3 比较器中断检测

如果在产生相关比较器中断请求时POEGGn.CDRE[5:0]为1，则每个组的GPT输出引脚都禁止输出。状态标志是POEGGn.IOCF，它与GPT输出禁用检测共享。

22.3.4 使用停止振荡检测的输出禁用控制

当时钟发生电路中的振荡停止检测功能检测到停止振荡时
POEGGn.OSTPE为1，每组的GPT输出引脚输出禁用。

22.3.5 使用寄存器的输出禁用控制

GPT输出引脚可以通过写入软件停止标志POEGGn.SSF来直接控制。

22.3.6 从输出禁用释放

要释放处于输出禁用状态的GPT输出引脚，可以通过复位将它们返回到初始状态，或者清除以下所有标志：

- POEGGn.PIDF
- POEGGn.IOCF
- POEGGn.OSTPF
- POEGGn.SSF.

如果外部输入引脚GTETRn未禁用且POEGGn.ST位未设置为0，则忽略向POEGGn.PIDF标志写入0（该标志未清除）。

仅当所有GTST.DTEF、GTST.OABHF和
GPT中的GTST.OABLF标志设置为0。

如果时钟生成电路中的OSTDSR.OSTDF标志未设置为0，则忽略向POEGGn.OSTPF标志写入0（该标志不被清除）。此外，当标志设置和释放同时发生时，标志集优先。

图22.3显示了输出禁用的释放时序。标志清零后，在GPT的下一个计数周期开始时，输出禁用被释放。

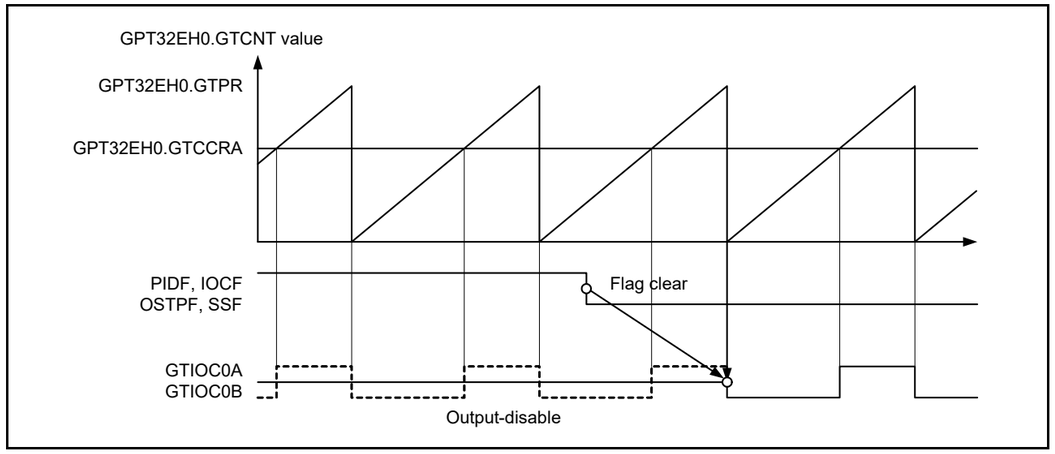


Figure 22.3 Output-disable release timing for GPT pin outputs

22.4 Interrupt Sources

The POEG generates an interrupt request when triggered by these sources:

- Output-disable control by input level detection
- Output-disable request from the GPT
- Comparator interrupt request detection.

Table 22.3 lists the conditions for interrupt requests.

Table 22.3 Interrupt sources and conditions

Interrupt source	Symbol	Associated flag	Trigger conditions
POEG group A interrupt	POEG_GROUP0	POEGGA.IOCF	An output-disable request from a GPT disable request occurred
			An output-disable request from a comparator interrupt occurred
		POEGGA.PIDF	An output-disable request from the GTETRGA pin occurred
POEG group B interrupt	POEG_GROUP1	POEGGB.IOCF	An output-disable request from a GPT disable request occurred
			An output-disable request from a comparator interrupt occurred
		POEGGB.PIDF	An output-disable request from the GTETRGB pin occurred
POEG group C interrupt	POEG_GROUP2	POEGGC.IOCF	An output-disable request from a GPT disable request occurred
			An output-disable request from a comparator interrupt occurred
		POEGGC.PIDF	An output-disable request from the GTETRGC pin occurred
POEG group D interrupt	POEG_GROUP3	POEGGD.IOCF	An output-disable request from a GPT disable request occurred
			An output-disable request from a comparator interrupt occurred
		POEGGD.PIDF	An output-disable request from the GTETRGD pin occurred

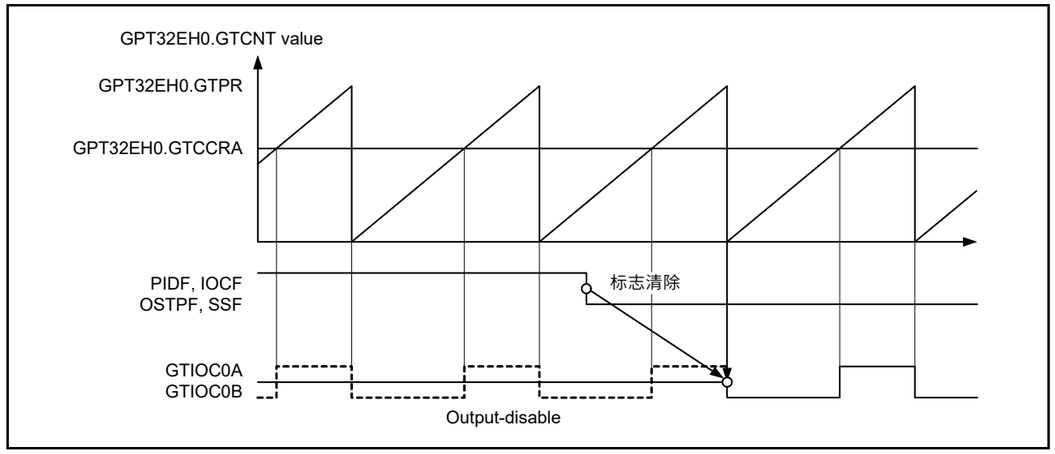


Figure 22.3 GPT引脚输出的输出禁用释放时序

22.4 中断源

当这些源触发时，POEG会产生一个中断请求：

- 通过输入电平检测进行输出禁用控制
- 来自GPT的输出禁用请求
- 比较器中断请求检测。

表22.3列出了中断请求的条件。

Table 22.3 中断源和条件

中断源	Symbol	相关标志	触发条件
POEGA组中断	POEG_GROUP0	POEGGA.IOCF	发生了来自GPT禁用请求的输出禁用请求
			发生了来自比较器中断的输出禁用请求
		POEGGA.PIDF	发生了来自GTETRGA引脚的输出禁用请求
POEGB组中断	POEG_GROUP1	POEGGB.IOCF	发生了来自GPT禁用请求的输出禁用请求
			发生了来自比较器中断的输出禁用请求
		POEGGB.PIDF	发生来自GTETRGB引脚的输出禁用请求
POEGC组中断	POEG_GROUP2	POEGGC.IOCF	发生了来自GPT禁用请求的输出禁用请求
			发生了来自比较器中断的输出禁用请求
		POEGGC.PIDF	发生了来自GTETRGC引脚的输出禁用请求
POEGD组中断	POEG_GROUP3	POEGGD.IOCF	发生了来自GPT禁用请求的输出禁用请求
			发生了来自比较器中断的输出禁用请求
		POEGGD.PIDF	发生来自GTETRGD引脚的输出禁用请求

22.5 External Trigger Output to the GPT

The POEG outputs the GTETRGn signals as the GPT operation trigger signal for the following:

- Count start
- Count stop
- Count clear
- Up-count
- Down-count
- Input capture.

For the POEGGn.INV polarity setting signal, when the same level is input three times continuously with the sampling clock selected in POEGGn.NFCS[1:0] and POEGGn.NFEN, that value is output. Set the control registers the same as for the input level detection operation described in section 22.3.1, Pin Input Level Detection Operation. The state after filtering can be monitored in POEGGn.ST.

Figure 22.4 shows the output timing of an external trigger to the GPT.

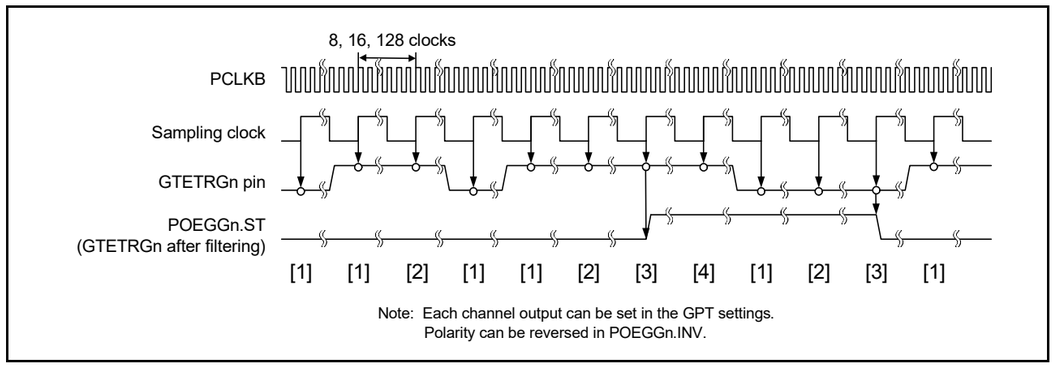


Figure 22.4 Output timing of external trigger to GPT

22.6 Usage Notes

22.6.1 Transition to Software Standby Mode

When using the POEG, do not invoke Software Standby mode. In this mode, the POEG stops and therefore output-disable of the pins cannot be controlled.

22.6.2 Specifying Pins Associated with the GPT

The POEG controls output-disable only when a pin is associated with the GPT in the PmnPFS.PMR and PmnPFS.PSEL settings. When the pin is specified as a general I/O pin, the POEG does not perform output-disable control.

22.5 到GPT的外部触发输出

POEG输出GTETRn信号作为GPT操作触发信号，用于以下用途：

- 计数开始
- 计数停止
- 清点数
- Up-count
- Down-count
- 输入捕获。

对于POEGGn.INV极性设置信号，当在POEGGn.NFCS[1:0]和POEGGn.NFEN中选择的采样时钟连续输入相同电平3次时，输出该值。将控制寄存器设置为与第22.3.1节“引脚输入电平检测操作”中描述的输入电平检测操作相同。过滤后的状态可以在POEGGn.ST中监控。

图22.4显示了外部触发到GPT的输出时序。

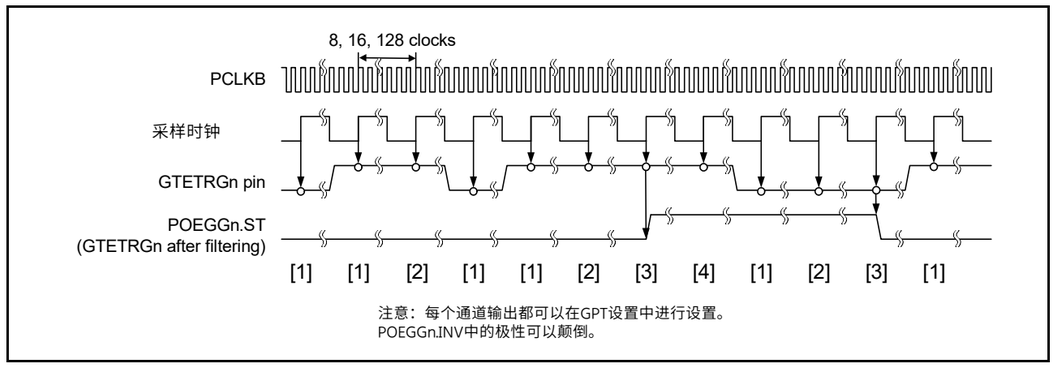


Figure 22.4 外部触发到GPT的输出时序

22.6 使用说明

22.6.1 过渡到软件待机模式

使用POEG时，请勿调用软件待机模式。在此模式下，POEG停止，因此无法控制引脚的输出禁用。

22.6.2 指定与GPT关联的引脚

仅当引脚与PmnPFS.PMR和PmnPFS.PSEL设置中的GPT关联时，POEG才控制输出禁用。当引脚指定为通用IO引脚时，POEG不执行输出禁用控制。

23. General PWM Timer (GPT)

23.1 Overview

The General PWM Timer (GPT) is a 32-bit timer with six GPT32 channels, four GPT32E channels, and four GPT32EH channels. PWM waveforms can be generated by controlling the up-counter, down-counter, or the up- and down-counter. The GPT can also be used as a general-purpose timer.

Table 23.1 lists the GPT specifications, Table 23.2 shows the GPT functions, Figure 23.1 shows a block diagram, Figure 23.2 shows the correspondence between the GPT channels and module names, and Table 23.3 lists the I/O pins.

Table 23.1 GPT specifications

Parameter	Specifications
Functions	• 32 bits × 14 channels • Up-counting or down-counting (saw waves) or up/down-counting (triangle waves) for each counter • Clock sources independently selectable for each channel • Two I/O pins per channel • Two output compare/input capture registers per channel • For the two output compare/input capture registers of each channel, four registers are provided as buffer registers and are capable of operating as comparison registers when buffering is not in use. • In output compare operation, buffer switching can be at crests or troughs, enabling the generation of laterally asymmetric PWM waveforms • Registers for setting up frame cycles in each channel (with capability for generating interrupts at overflow or underflow) • Generation of dead times in PWM operation • Synchronous starting, stopping, and clearing counters for arbitrary channels • Starting, stopping, and clearing up/down counters in response to a maximum of eight ELC events • Starting, stopping, and clearing up/down counters in response to input level comparison • Starting, stopping, and clearing up/down counters in response to a maximum of four external triggers • Output pin disable function by dead time error and detected short-circuits between output pins • A/D converter start triggers can be generated • PWM waveform for controlling brushless DC motors can be generated • Compare match A to F event, overflow/underflow event, and input UVW edge event can be output to the ELC • Enables the noise filter for input capture and input UVW • Bus clock: PCLKA • Core clock: PCLKD • Frequency ratio: PCLKA:PCLKD = 1:N (N = 1/2/4/8/16/32/64).

Table 23.2 GPT functions (1 of 2)

Parameter	GPT32EH, GPT32E	GPT32
Count clock	PCLKD PCLKD/4 PCLKD/16 PCLKD/64 PCLKD/256 PCLKD/1024	PCLKD PCLKD/4 PCLKD/16 PCLKD/64 PCLKD/256 PCLKD/1024
Output compare/input capture registers (GTCCR)	GTCCRA GTCCRB	GTCCRA GTCCRB
Compare/buffer registers	GTCCRC GTCCRD GTCCRE GTCCRF	GTCCRC GTCCRD GTCCRE GTCCRF
Cycle setting register	GTPR	GTPR
Cycle setting buffer registers	GTPBR GTPDBR	GTPBR
I/O pins	GTIOCA GTIOCB	GTIOCA GTIOCB

23. 通用PWM定时器(GPT)

23.1 Overview

通用PWM定时器(GPT)是一个32位定时器，具有六个GPT32通道、四个GPT32E通道和四个GPT32EH通道。PWM波形可以通过控制加计数器、减计数器或加减计数器来产生。GPT也可以用作通用定时器。

表23.1列出了GPT规格，表23.2列出了GPT功能，图23.1给出了框图，图23.2给出了GPT通道和模块名称的对应关系，表23.3列出了IO引脚。

Table 23.1 GPT specifications

Parameter	Specifications
Functions	32位×14通道 每个计数器的递增计数或递减计数（锯齿波）或递增递减计数（三角波） 每条通道可独立选择时钟源 每条通道两个IO引脚 两个输出比较输入捕捉每个通道的寄存器 对于每个通道的两个输出比较输入捕捉寄存器，提供四个寄存器作为缓冲寄存器，并且能够在不使用缓冲时作为比较寄存器操作。 在输出比较操作中，缓冲器切换可以在波峰或波谷，从而产生横向不对称的PWM波形 用于在每个通道中设置帧周期的寄存器（具有在上溢或下溢时产生中断的能力） 产生死区时间PWM操作 同步启动、停止和清除任意通道的计数器 启动、停止和清除递减计数器以响应最多8个ELC事件 启动、停止和清除递减计数器以响应输入电平比较 响应最多四个外部触发启动、停止和清除递减计数器 通过死区时间错误和检测到输出引脚之间的短路禁用输出引脚功能 可以生成AD转换器启动触发 用于控制无刷直流的PWM波形可以生成电机 比较匹配A到F事件、上溢下溢事件和输入UVW边缘事件可以输出到ELC启用输入捕获和输入UVW的噪声滤波器总线时钟：PCLKA内核时钟：PCLKD频率比：PCLKA:PCLKD=1:N(N=1248163264)。

Table 23.2 GPT函数(1of2)

Parameter	GPT32EH, GPT32E	GPT32
计数时钟	PCLKD PCLKD/4 PCLKD/16 PCLKD/64 PCLKD/256 PCLKD/1024	PCLKD PCLKD/4 PCLKD/16 PCLKD/64 PCLKD/256 PCLKD/1024
输出比较输入捕捉寄存器(GTCCR)	GTCCRA GTCCRB	GTCCRA GTCCRB
Compare/buffer registers	GTCCRC GTCCRD GTCCRE GTCCRF	GTCCRC GTCCRD GTCCRE GTCCRF
周期设定寄存器	GTPR	GTPR
循环设置缓冲寄存器	GTPBR GTPDBR	GTPBR
I/O pins	GTIOCA GTIOCB	GTIOCA GTIOCB

Table 23.2 GPT functions (2 of 2)

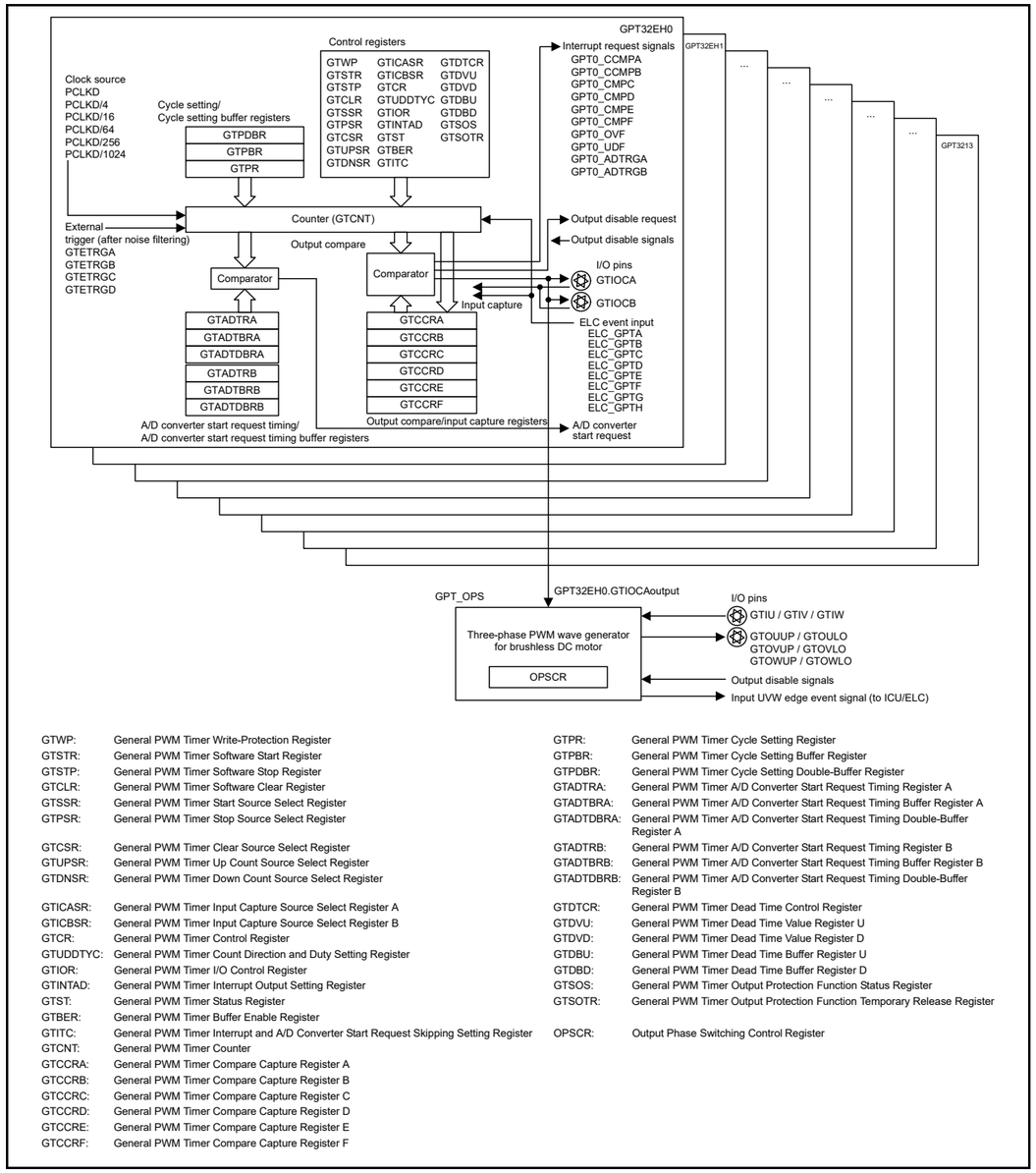
Parameter		GPT32EH, GPT32E	GPT32
External trigger input pin*1		GTETRGA GTETRGB GTETRGC GTETRGD	GTETRGA GTETRGB GTETRGC GTETRGD
Counter clear sources		GTPR register compare match, input capture, input pin status, ELC event input, and GTETRGn (n = A, B, C, D) pin input	GTPR register compare match, input capture, input pin status, ELC event input, and GTETRGn (n = A, B, C, D) pin input
Compare match output	Low output	Available	Available
	High output	Available	Available
	Toggle output	Available	Available
Input capture function		Available	Available
Automatic addition of dead time		Available	Available (no dead time buffer)
PWM mode		Available	Available
Phase count function		Available	Available
Buffer operation		Double buffer	Double buffer
One-shot operation		Available	Available
DTC activation		All the interrupt sources	All the interrupt sources
A/D converter start trigger		Compare match of GTADTRA or GTADTRB	-
Brushless DC motor control function		Available	Available
Interrupt sources		10 sources • GTCCRA compare match/input capture (GPTn_CCMPA) • GTCCRB compare match/input capture (GPTn_CCMPB) • GTCCRC compare match (GPTn_CMPC) • GTCCRD compare match (GPTn_CMPD) • GTCCRE compare match (GPTn_CMPCE) • GTCCRF compare match (GPTn_CMPF) • GTADTRA compare match (GPTn_ADTRGA) • GTADTRB compare match (GPTn_ADTRGB) • GTCNT overflow (GTPR compare match) (GPTn_OVF) • GTCNT underflow (GPTn_UDF)	8 sources • GTCCRA compare match/input capture (GPTn_CCMPA) • GTCCRB compare match/input capture (GPTn_CCMPB) • GTCCRC compare match (GPTn_CMPC) • GTCCRD compare match (GPTn_CMPD) • GTCCRE compare match (GPTn_CMPE) • GTCCRF compare match (GPTn_CMPF) • GTCNT overflow (GTPR compare match) (GPTn_OVF) • GTCNT underflow (GPTn_UDF)
Interrupt skipping function		Skips GTCNT overflows (GTPR compare match) (GPTn_OVF)/ GTCNT underflow (GPTn_UDF) interrupts (with interlocking function for other interrupts or A/D conversion requests).	-
Event linking (ELC) function		Available	Available
Noise filtering function		Available	Available

Note 1. GTRETRGn connects to GPT through the POEG module. Therefore, to use the GPT function, supply the POEG clock by clearing the MSTPD14 bit.

Table 23.2 GPT功能（2个中的2个）

Parameter		GPT32EH, GPT32E	GPT32
外部触发输入引脚*1		GTETRGA GTETRGB GTETRGC GTETRGD	GTETRGA GTETRGB GTETRGC GTETRGD
反清源		GTPR寄存器比较匹配、输入捕捉、输入引脚状态、ELC事件输入和GTETRn(n=A B C D)引脚输入	GTPR寄存器比较匹配、输入捕捉、输入引脚状态、ELC事件输入和GTETRn(n=A B C D)引脚输入
比较匹配输出	低输出	Available	Available
	高输出	Available	Available
	切换输出	Available	Available
输入捕捉功能		Available	Available
自动添加死区时间		Available	可用（无死区时间缓冲区）
PWM mode		Available	Available
相位计数功能		Available	Available
缓冲操作		双缓冲	双缓冲
One-shot operation		Available	Available
DTC activation		所有中断源	所有中断源
AD转换器启动触发		比较GTADTRA的匹配或GTADTRB	-
直流无刷电机控制功能		Available	Available
中断源		10个来源 GTCCRA比较匹配输入捕获(GPTn_CCMPA) GTCCRB比较匹配输入捕获(GPTn_CCMPB) GTCCRC比较匹配(GPTn_CMPC) GTCCRD比较匹配(GPTn_CMPD) GTCCRE比较匹配(GPTn_CMPCE) GTCCRF比较匹配(GPTn_CMPF) GTADTRA比较匹配(GPTn_ADTRGA) GTADTRB比较匹配(GPTn_ADTRGB) GTCNT上溢(GTPR比较匹配)(GPTn_OVF) GTCNT下溢(GPTn_UDF)	8个源 GTCCRA比较匹配输入捕获(GPTn_CCMPA) GTCCRB比较匹配输入捕获(GPTn_CCMPB) GTCCRC比较匹配(GPTn_CMPC) GTCCRD比较匹配(GPTn_CMPD) GTCCRE比较匹配(GPTn_CMPE) GTCCRF比较匹配(GPTn_CMPF) GTCNT上溢（GTPR比较匹配）（GPTn_OVF） GTCNT下溢（GPTn_UDF）
中断跳跃功能		跳过GTCNT上溢（GTPR比较匹配）（GPTn_OVF）GTCNT下溢（GPTn_UDF）中断（具有其他中断或AD转换请求的互锁功能）。	-
事件链接(ELC)功能		Available	Available
噪音过滤功能		Available	Available

Note 1. GTRETRGn通过POEG模块连接到GPT。因此，要使用GPT功能，通过清除MSTPD14位来提供POEG时钟。



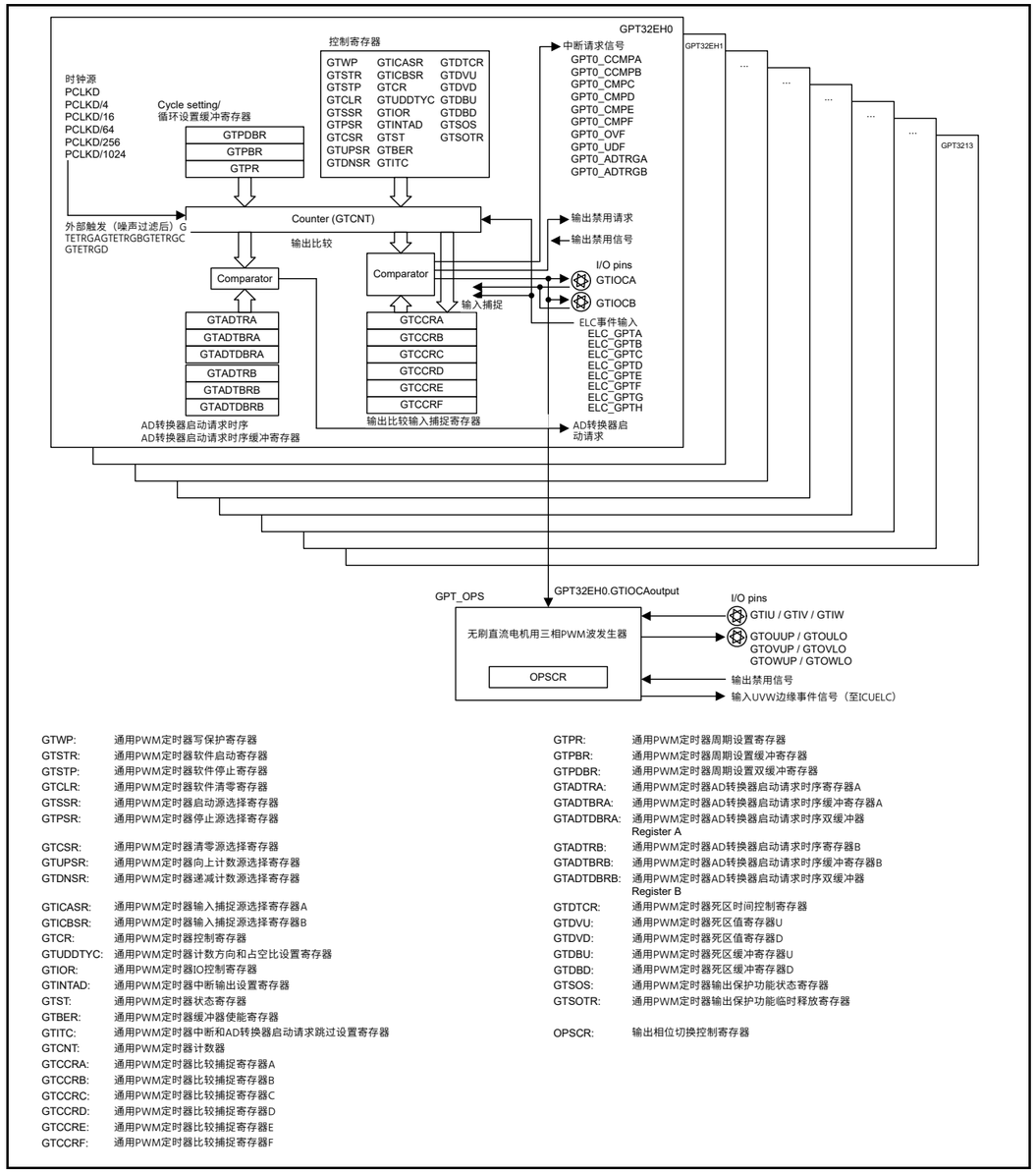
GTWP: General PWM Timer Write-Protection Register
GTSTR: General PWM Timer Software Start Register
GTSTP: General PWM Timer Software Stop Register
GTCLR: General PWM Timer Software Clear Register
GTSSR: General PWM Timer Start Source Select Register
GTPSR: General PWM Timer Stop Source Select Register
GTCSR: General PWM Timer Clear Source Select Register
GTUPSR: General PWM Timer Up Count Source Select Register
GTDNSR: General PWM Timer Down Count Source Select Register
GTICASR: General PWM Timer Input Capture Source Select Register A
GTICBSR: General PWM Timer Input Capture Source Select Register B
GTCR: General PWM Timer Control Register
GTUDDTYC: General PWM Timer Count Direction and Duty Setting Register
GTIOR: General PWM Timer I/O Control Register
GTINTAD: General PWM Timer Interrupt Output Setting Register
GTST: General PWM Timer Status Register
GTBER: General PWM Timer Buffer Enable Register
GTITC: General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register
GTCNT: General PWM Timer Counter
GTCCRA: General PWM Timer Compare Capture Register A
GTCCRB: General PWM Timer Compare Capture Register B
GTCCRC: General PWM Timer Compare Capture Register C
GTCCRD: General PWM Timer Compare Capture Register D
GTCCRE: General PWM Timer Compare Capture Register E
GTCCRF: General PWM Timer Compare Capture Register F

GTPR: General PWM Timer Cycle Setting Register
GTPBR: General PWM Timer Cycle Setting Buffer Register
GTPDBR: General PWM Timer Cycle Setting Double-Buffer Register
GTADTRA: General PWM Timer A/D Converter Start Request Timing Register A
GTADTBRA: General PWM Timer A/D Converter Start Request Timing Buffer Register A
GTADTDBRA: General PWM Timer A/D Converter Start Request Timing Double-Buffer Register A
GTADTRB: General PWM Timer A/D Converter Start Request Timing Register B
GTADTBRB: General PWM Timer A/D Converter Start Request Timing Buffer Register B
GTADTDBRB: General PWM Timer A/D Converter Start Request Timing Double-Buffer Register B
GTDTCR: General PWM Timer Dead Time Control Register
GTDVU: General PWM Timer Dead Time Value Register U
GTDVD: General PWM Timer Dead Time Value Register D
GTDBU: General PWM Timer Dead Time Buffer Register U
GTDBD: General PWM Timer Dead Time Buffer Register D
GTSOS: General PWM Timer Output Protection Function Status Register
GTSOTR: General PWM Timer Output Protection Function Temporary Release Register

OPSCR: Output Phase Switching Control Register

Figure 23.1 GPT block diagram

Figure 23.2 shows an example using multiple GPTs.



GTWP: 通用PWM定时器写保护寄存器
GTSTR: 通用PWM定时器软件启动寄存器
GTSTP: 通用PWM定时器软件停止寄存器
GTCLR: 通用PWM定时器软件清零寄存器
GTSSR: 通用PWM定时器启动源选择寄存器
GTPSR: 通用PWM定时器停止源选择寄存器
GTCSR: 通用PWM定时器清零源选择寄存器
GTUPSR: 通用PWM定时器向上计数源选择寄存器
GTDNSR: 通用PWM定时器递减计数源选择寄存器
GTICASR: 通用PWM定时器输入捕捉源选择寄存器A
GTICBSR: 通用PWM定时器输入捕捉源选择寄存器B
GTCR: 通用PWM定时器控制寄存器
GTUDDTYC: 通用PWM定时器计数方向和占空比设置寄存器
GTIOR: 通用PWM定时器IO控制寄存器
GTINTAD: 通用PWM定时器中断输出设置寄存器
GTST: 通用PWM定时器状态寄存器
GTBER: 通用PWM定时器缓冲器使能寄存器
GTITC: 通用PWM定时器中断和AD转换器启动请求跳过设置寄存器
GTCNT: 通用PWM定时器计数器
GTCCRA: 通用PWM定时器比较捕捉寄存器A
GTCCRB: 通用PWM定时器比较捕捉寄存器B
GTCCRC: 通用PWM定时器比较捕捉寄存器C
GTCCRD: 通用PWM定时器比较捕捉寄存器D
GTCCRE: 通用PWM定时器比较捕捉寄存器E
GTCCRF: 通用PWM定时器比较捕捉寄存器F

GTPR: 通用PWM定时器周期设置寄存器
GTPBR: 通用PWM定时器周期设置缓冲寄存器
GTPDBR: 通用PWM定时器周期设置双缓冲寄存器
GTADTRA: 通用PWM定时器AD转换器启动请求时序寄存器A
GTADTBRA: 通用PWM定时器AD转换器启动请求时序缓冲寄存器A
GTADTDBRA: 通用PWM定时器AD转换器启动请求时序双缓冲器 Register A
GTADTRB: 通用PWM定时器AD转换器启动请求时序寄存器B
GTADTBRB: 通用PWM定时器AD转换器启动请求时序缓冲寄存器B
GTADTDBRB: 通用PWM定时器AD转换器启动请求时序双缓冲器 Register B
GTDTCR: 通用PWM定时器死区时间控制寄存器
GTDVU: 通用PWM定时器死区值寄存器U
GTDVD: 通用PWM定时器死区值寄存器D
GTDBU: 通用PWM定时器死区缓冲寄存器U
GTDBD: 通用PWM定时器死区缓冲寄存器D
GTSOS: 通用PWM定时器输出保护功能状态寄存器
GTSOTR: 通用PWM定时器输出保护功能临时释放寄存器

OPSCR: 输出相位切换控制寄存器

Figure 23.1 GPT框图

图23.2显示了使用多个GPT的示例。

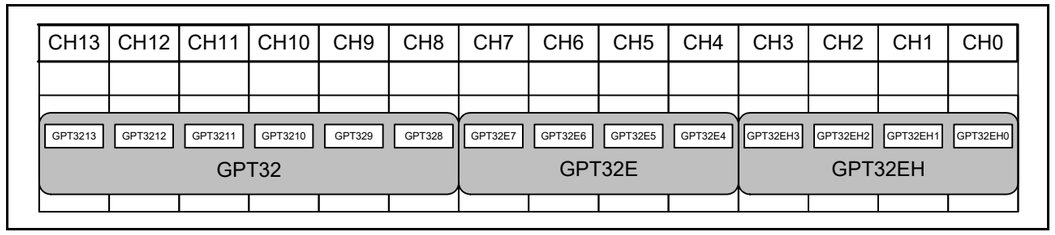


Figure 23.2 Correspondence between GPT channels and module names

Table 23.3 GPT I/O pins (1 of 2)

Channel	Pin name	I/O	Function
Shared	GTETRGA	Input	External trigger input pin A (after noise filtering)
	GTETRGB	Input	External trigger input pin B (after noise filtering)
	GTETRGC	Input	External trigger input pin C (after noise filtering)
	GTETRGD	Input	External trigger input pin D (after noise filtering)
GPT32EH0	GTIOC0A	I/O	GTCCRA register input capture input/output compare output/PWM output pin
	GTIOC0B	I/O	GTCCRB register input capture input/output compare output/PWM output pin
GPT32EH1	GTIOC1A	I/O	GTCCRA register input capture input/output compare output/PWM output pin
	GTIOC1B	I/O	GTCCRB register input capture input/output compare output/PWM output pin
GPT32EH2	GTIOC2A	I/O	GTCCRA register input capture input/output compare output/PWM output pin
	GTIOC2B	I/O	GTCCRB register input capture input/output compare output/PWM output pin
GPT32EH3	GTIOC3A	I/O	GTCCRA register input capture input/output compare output/PWM output pin
	GTIOC3B	I/O	GTCCRB register input capture input/output compare output/PWM output pin
GPT32E4	GTIOC4A	I/O	GTCCRA register input capture input/output compare output/PWM output pin
	GTIOC4B	I/O	GTCCRB register input capture input/output compare output/PWM output pin
GPT32E5	GTIOC5A	I/O	GTCCRA register input capture input/output compare output/PWM output pin
	GTIOC5B	I/O	GTCCRB register input capture input/output compare output/PWM output pin
GPT32E6	GTIOC6A	I/O	GTCCRA register input capture input/output compare output/PWM output pin
	GTIOC6B	I/O	GTCCRB register input capture input/output compare output/PWM output pin
GPT32E7	GTIOC7A	I/O	GTCCRA register input capture input/output compare output/PWM output pin
	GTIOC7B	I/O	GTCCRB register input capture input/output compare output/PWM output pin
GPT328	GTIOC8A	I/O	GTCCRA register input capture input/output compare output/PWM output pin
	GTIOC8B	I/O	GTCCRB register input capture input/output compare output/PWM output pin
GPT329	GTIOC9A	I/O	GTCCRA register input capture input/output compare output/PWM output pin
	GTIOC9B	I/O	GTCCRB register input capture input/output compare output/PWM output pin
GPT3210	GTIOC10A	I/O	GTCCRA register input capture input/output compare output/PWM output pin
	GTIOC10B	I/O	GTCCRB register input capture input/output compare output/PWM output pin
GPT3211	GTIOC11A	I/O	GTCCRA register input capture input/output compare output/PWM output pin
	GTIOC11B	I/O	GTCCRB register input capture input/output compare output/PWM output pin
GPT3212	GTIOC12A	I/O	GTCCRA register input capture input/output compare output/PWM output pin
	GTIOC12B	I/O	GTCCRB register input capture input/output compare output/PWM output pin
GPT3213	GTIOC13A	I/O	GTCCRA register input capture input/output compare output/PWM output pin
	GTIOC13B	I/O	GTCCRB register input capture input/output compare output/PWM output pin

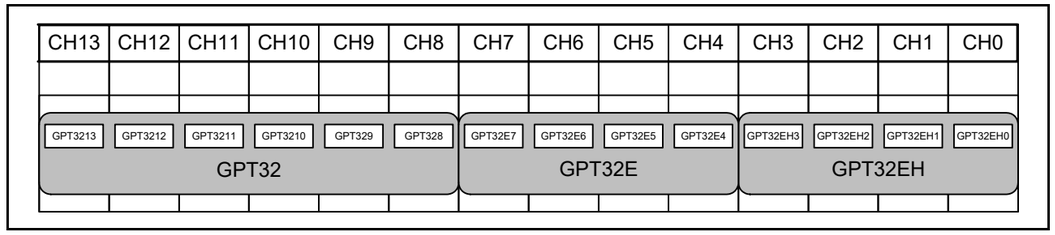


Figure 23.2 GPT通道与模块名称的对应关系

Table 23.3 GPTIO引脚（2个中的1个）

Channel	引脚名称	I/O	Function
Shared	GTETRGA	Input	外部触发输入引脚A（噪声过滤后）
	GTETRGB	Input	外部触发输入引脚B（噪声过滤后）
	GTETRGC	Input	外部触发输入引脚C（噪声过滤后）
	GTETRGD	Input	外部触发输入引脚D（噪声过滤后）
GPT32EH0	GTIOC0A	I/O	GTCCRA寄存器输入捕捉输入输出比较输出PWM输出引脚
	GTIOC0B	I/O	GTCCRB寄存器输入捕捉输入输出比较输出PWM输出引脚
GPT32EH1	GTIOC1A	I/O	GTCCRA寄存器输入捕捉输入输出比较输出PWM输出引脚
	GTIOC1B	I/O	GTCCRB寄存器输入捕捉输入输出比较输出PWM输出引脚
GPT32EH2	GTIOC2A	I/O	GTCCRA寄存器输入捕捉输入输出比较输出PWM输出引脚
	GTIOC2B	I/O	GTCCRB寄存器输入捕捉输入输出比较输出PWM输出引脚
GPT32EH3	GTIOC3A	I/O	GTCCRA寄存器输入捕捉输入输出比较输出PWM输出引脚
	GTIOC3B	I/O	GTCCRB寄存器输入捕捉输入输出比较输出PWM输出引脚
GPT32E4	GTIOC4A	I/O	GTCCRA寄存器输入捕捉输入输出比较输出PWM输出引脚
	GTIOC4B	I/O	GTCCRB寄存器输入捕捉输入输出比较输出PWM输出引脚
GPT32E5	GTIOC5A	I/O	GTCCRA寄存器输入捕捉输入输出比较输出PWM输出引脚
	GTIOC5B	I/O	GTCCRB寄存器输入捕捉输入输出比较输出PWM输出引脚
GPT32E6	GTIOC6A	I/O	GTCCRA寄存器输入捕捉输入输出比较输出PWM输出引脚
	GTIOC6B	I/O	GTCCRB寄存器输入捕捉输入输出比较输出PWM输出引脚
GPT32E7	GTIOC7A	I/O	GTCCRA寄存器输入捕捉输入输出比较输出PWM输出引脚
	GTIOC7B	I/O	GTCCRB寄存器输入捕捉输入输出比较输出PWM输出引脚
GPT328	GTIOC8A	I/O	GTCCRA寄存器输入捕捉输入输出比较输出PWM输出引脚
	GTIOC8B	I/O	GTCCRB寄存器输入捕捉输入输出比较输出PWM输出引脚
GPT329	GTIOC9A	I/O	GTCCRA寄存器输入捕捉输入输出比较输出PWM输出引脚
	GTIOC9B	I/O	GTCCRB寄存器输入捕捉输入输出比较输出PWM输出引脚
GPT3210	GTIOC10A	I/O	GTCCRA寄存器输入捕捉输入输出比较输出PWM输出引脚
	GTIOC10B	I/O	GTCCRB寄存器输入捕捉输入输出比较输出PWM输出引脚
GPT3211	GTIOC11A	I/O	GTCCRA寄存器输入捕捉输入输出比较输出PWM输出引脚
	GTIOC11B	I/O	GTCCRB寄存器输入捕捉输入输出比较输出PWM输出引脚
GPT3212	GTIOC12A	I/O	GTCCRA寄存器输入捕捉输入输出比较输出PWM输出引脚
	GTIOC12B	I/O	GTCCRB寄存器输入捕捉输入输出比较输出PWM输出引脚
GPT3213	GTIOC13A	I/O	GTCCRA寄存器输入捕捉输入输出比较输出PWM输出引脚
	GTIOC13B	I/O	GTCCRB寄存器输入捕捉输入输出比较输出PWM输出引脚

Table 23.3 GPT I/O pins (2 of 2)

Channel	Pin name	I/O	Function
GPT_OPS	GTIU	Input	Hall sensor input pin U
	GTIV	Input	Hall sensor input pin V
	GTIW	Input	Hall sensor input pin W
	GTOUUP	Output	3-phase PWM output for BLDC motor control (positive U-phase)
	GTOULO	Output	3-phase PWM output for BLDC motor control (negative U-phase)
	GTOVUP	Output	3-phase PWM output for BLDC motor control (positive V-phase)
	GTOVLO	Output	3-phase PWM output for BLDC motor control (negative V-phase)
	GTOWUP	Output	3-phase PWM output for BLDC motor control (positive W-phase)
	GTOWLO	Output	3-phase PWM output for BLDC motor control (negative W-phase)

23.2 Register Descriptions

Table 23.4 lists the registers in the GPT.

Table 23.4 GPT registers (1 of 2)

Module symbol	Register name	Register symbol	Reset value	Address (m = 0 to 13)	Access size	GPT32EH/ GPT32E	GPT32
GPT32EHm (m = 0 to 3) GPT32Em (m = 4 to 7) GPT32m (m = 8 to 13)	General PWM Timer Write Protection Register	GTWP	0000_0000h	4007 8000h + 0100h × m	32	✓	✓
	General PWM Timer Software Start Register	GTSTR	0000_0000h	4007 8004h + 0100h × m	32	✓	✓
	General PWM Timer Software Stop Register	GTSTP	FFFF_FFFFh	4007 8008h + 0100h × m	32	✓	✓
	General PWM Timer Software Clear Register	GTCLR	0000_0000h	4007 800Ch + 0100h × m	32	✓	✓
	General PWM Timer Start Source Select Register	GTSSR	0000_0000h	4007 8010h + 0100h × m	32	✓	✓
	General PWM Timer Stop Source Select Register	GTPSR	0000_0000h	4007 8014h + 0100h × m	32	✓	✓
	General PWM Timer Clear Source Select Register	GTCSR	0000_0000h	4007 8018h + 0100h × m	32	✓	✓
	General PWM Timer Up Count Source Select Register	GTUPSR	0000_0000h	4007 801Ch + 0100h × m	32	✓	✓
	General PWM Timer Down Count Source Select Register	GTDNSR	0000_0000h	4007 8020h + 0100h × m	32	✓	✓
	General PWM Timer Input Capture Source Select Register A	GTICASR	0000_0000h	4007 8024h + 0100h × m	32	✓	✓
	General PWM Timer Input Capture Source Select Register B	GTICBSR	0000_0000h	4007 8028h + 0100h × m	32	✓	✓
	General PWM Timer Control Register	GTCR	0000_0000h	4007 802Ch + 0100h × m	32	✓	✓
	General PWM Timer Count Direction and Duty Setting Register	GTUDDTYC	0000_0001h	4007 8030h + 0100h × m	32	✓	✓
	General PWM Timer I/O Control Register	GTIOR	0000_0000h	4007 8034h + 0100h × m	32	✓	✓
	General PWM Timer Interrupt Output Setting Register	GTINTAD	0000_0000h	4007 8038h + 0100h × m	32	✓	(✓)*1
	General PWM Timer Status Register	GTST	0000_8000h	4007 803Ch + 0100h × m	32	✓	(✓)*1
	General PWM Timer Buffer Enable Register	GTBER	0000_0000h	4007 8040h + 0100h × m	32	✓	(✓)*1
GPT32EHm (m = 0 to 3) GPT32Em (m = 4 to 7)	General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register	GTITC	0000_0000h	4007 8044h + 0100h × m	32	✓	-

Table 23.3 GPTIO引脚（2个中的2个）

Channel	引脚名称	I/O	Function
GPT_OPS	GTIU	Input	霍尔传感器输入引脚U
	GTIV	Input	霍尔传感器输入引脚V
	GTIW	Input	霍尔传感器输入引脚W
	GTOUUP	Output	用于BLDC电机控制的3相PWM输出（正U相）
	GTOULO	Output	用于BLDC电机控制的3相PWM输出（负U相）
	GTOVUP	Output	用于BLDC电机控制的3相PWM输出（正V相）
	GTOVLO	Output	用于BLDC电机控制的3相PWM输出（负V相）
	GTOWUP	Output	用于BLDC电机控制的3相PWM输出（正W相）
	GTOWLO	Output	用于BLDC电机控制的3相PWM输出（负W相）

23.2 注册说明

表23.4列出了GPT中的寄存器。

Table 23.4 GPT寄存器(1of2)

模块符号	注册名称	注册符号	重置值	地址（m=0到13）	访问大小	GPT32EH/ GPT32E	GPT32
GPT32EHm (m = 0 to 3) GPT32Em (m = 4 to 7) GPT32m (m = 8 to 13)	通用PWM定时器写保护登记册	GTWP	0000_0000h	4007 8000h + 0100h × m	32	✓	✓
	通用PWM定时器软件启动Register	GTSTR	0000_0000h	4007 8004h + 0100h × m	32	✓	✓
	通用PWM定时器软件停止Register	GTSTP	FFFF_FFFFh	4007 8008h + 0100h × m	32	✓	✓
	通用PWM定时器软件清零Register	GTCLR	0000_0000h	4007 800Ch + 0100h × m	32	✓	✓
	通用PWM定时器启动源选择注册	GTSSR	0000_0000h	4007 8010h + 0100h × m	32	✓	✓
	通用PWM定时器停止源选择注册	GTPSR	0000_0000h	4007 8014h + 0100h × m	32	✓	✓
	通用PWM定时器清零源选择注册	GTCSR	0000_0000h	4007 8018h + 0100h × m	32	✓	✓
	通用PWM定时器向上计数源选择寄存器	GTUPSR	0000_0000h	4007 801Ch + 0100h × m	32	✓	✓
	通用PWM定时器递减计数源选择寄存器	GTDNSR	0000_0000h	4007 8020h + 0100h × m	32	✓	✓
	通用PWM定时器输入捕捉源选择寄存器A	GTICASR	0000_0000h	4007 8024h + 0100h × m	32	✓	✓
	通用PWM定时器输入捕捉源选择寄存器B	GTICBSR	0000_0000h	4007 8028h + 0100h × m	32	✓	✓
	通用PWM定时器控制Register	GTCR	0000_0000h	4007 802Ch + 0100h × m	32	✓	✓
	通用PWM定时器计数方向和占空比设置寄存器	GTUDDTYC	0000_0001h	4007 8030h + 0100h × m	32	✓	✓
	通用PWM定时器IO控制Register	GTIOR	0000_0000h	4007 8034h + 0100h × m	32	✓	✓
	通用PWM定时器中断输出设置寄存器	GTINTAD	0000_0000h	4007 8038h + 0100h × m	32	✓	(✓)*1
	通用PWM定时器状态Register	GTST	0000_8000h	4007 803Ch + 0100h × m	32	✓	(✓)*1
	通用PWM定时器缓冲器使能Register	GTBER	0000_0000h	4007 8040h + 0100h × m	32	✓	(✓)*1
GPT32EHm (m = 0 to 3) GPT32Em (m = 4 to 7)	通用PWM定时器中断和AD转换器启动请求跳过设置寄存器	GTITC	0000_0000h	4007 8044h + 0100h × m	32	✓	-

Table 23.4 GPT registers (2 of 2)

Module symbol	Register name	Register symbol	Reset value	Address (m = 0 to 13)	Access size	GPT32EH/ GPT32E	GPT32
GPT32EHm (m = 0 to 3) GPT32Em (m = 4 to 7) GPT32m (m = 8 to 13)	General PWM Timer Counter	GTCNT	0000_0000h	4007 8048h + 0100h × m	32	✓	✓
	General PWM Timer Compare Capture Register A	GTCCRA	FFFF_FFFFh	4007 804Ch + 0100h × m	32	✓	✓
	General PWM Timer Compare Capture Register B	GTCCRB	FFFF_FFFFh	4007 8050h + 0100h × m	32	✓	✓
	General PWM Timer Compare Capture Register C	GTCCRC	FFFF_FFFFh	4007 8054h + 0100h × m	32	✓	✓
	General PWM Timer Compare Capture Register E	GTCCRE	FFFF_FFFFh	4007 8058h + 0100h × m	32	✓	✓
	General PWM Timer Compare Capture Register D	GTCCRD	FFFF_FFFFh	4007 805Ch + 0100h × m	32	✓	✓
	General PWM Timer Compare Capture Register F	GTCCRF	FFFF_FFFFh	4007 8060h + 0100h × m	32	✓	✓
	General PWM Timer Cycle Setting Register	GTPR	FFFF_FFFFh	4007 8064h + 0100h × m	32	✓	✓
	General PWM Timer Cycle Setting Buffer Register	GTPBR	FFFF_FFFFh	4007 8068h + 0100h × m	32	✓	✓
GPT32EHm (m = 0 to 3) GPT32Em (m = 4 to 7)	General PWM Timer Cycle Setting Double-Buffer Register	GTPDBR	FFFF_FFFFh	4007 806Ch + 0100h × m	32	✓	-
	A/D Converter Start Request Timing Register A	GTADTRA	FFFF_FFFFh	4007 8070h + 0100h × m	32	✓	-
	A/D Converter Start Request Timing Buffer Register A	GTADTBRA	FFFF_FFFFh	4007 8074h + 0100h × m	32	✓	-
	A/D Converter Start Request Timing Double-Buffer Register A	GTADTDBRA	FFFF_FFFFh	4007 8078h + 0100h × m	32	✓	-
	A/D Converter Start Request Timing Register B	GTADTRB	FFFF_FFFFh	4007 807Ch + 0100h × m	32	✓	-
	A/D Converter Start Request Timing Buffer Register B	GTADTBRB	FFFF_FFFFh	4007 8080h + 0100h × m	32	✓	-
	A/D Converter Start Request Timing Double-Buffer Register B	GTADTDBRB	FFFF_FFFFh	4007 8084h + 0100h × m	32	✓	-
GPT32EHm (m = 0 to 3) GPT32Em (m = 4 to 7) GPT32m (m = 8 to 13)	General PWM Timer Dead Time Control Register	GTDTCR	0000_0000h	4007 8088h + 0100h × m	32	✓	(✓)*1
	General PWM Timer Dead Time Value Register U	GTDVU	FFFF_FFFFh	4007 808Ch + 0100h × m	32	✓	✓
GPT32EHm (m = 0 to 3) GPT32Em (m = 4 to 7)	General PWM Timer Dead Time Value Register D	GTDVD	FFFF_FFFFh	4007 8090h + 0100h × m	32	✓	-
	General PWM Timer Dead Time Buffer Register U	GTDBU	FFFF_FFFFh	4007 8094h + 0100h × m	32	✓	-
	General PWM Timer Dead Time Buffer Register D	GTDBD	FFFF_FFFFh	4007 8098h + 0100h × m	32	✓	-
	General PWM Timer Output Protection Function Status Register	GTSOS	0000_0000h	4007 809Ch + 0100h × m	32	✓	-
	General PWM Timer Output Protection Function Temporary Release Register	GTSOTR	0000_0000h	4007 80A0h + 0100h × m	32	✓	-
GPT_OPS	Output Phase Switching Control Register	OPSCR	0000_0000h	4007 8FF0h	32	✓	✓

Note 1. Some functions are reduced from GPT32EH/GPT32E.

Table 23.4 GPT寄存器（2个中的2个）

模块符号	注册名称	注册符号	重置值	地址（m=0到13）	访问大小	GPT32EH/ GPT32E	GPT32
GPT32EHm (m = 0 to 3) GPT32Em (m = 4 to 7) GPT32m (m = 8 to 13)	通用PWM定时器计数器	GTCNT	0000_0000h	4007 8048h + 0100h × m	32	✓	✓
	通用PWM定时器比较捕获寄存器A	GTCCRA	FFFF_FFFFh	4007 804Ch + 0100h × m	32	✓	✓
	通用PWM定时器比较捕获寄存器B	GTCCRB	FFFF_FFFFh	4007 8050h + 0100h × m	32	✓	✓
	通用PWM定时器比较捕获寄存器C	GTCCRC	FFFF_FFFFh	4007 8054h + 0100h × m	32	✓	✓
	通用PWM定时器比较捕获寄存器E	GTCCRE	FFFF_FFFFh	4007 8058h + 0100h × m	32	✓	✓
	通用PWM定时器比较捕获寄存器D	GTCCRD	FFFF_FFFFh	4007 805Ch + 0100h × m	32	✓	✓
	通用PWM定时器比较捕获寄存器F	GTCCRF	FFFF_FFFFh	4007 8060h + 0100h × m	32	✓	✓
	通用PWM定时器周期设置Register	GTPR	FFFF_FFFFh	4007 8064h + 0100h × m	32	✓	✓
	通用PWM定时器周期设置缓冲寄存器	GTPBR	FFFF_FFFFh	4007 8068h + 0100h × m	32	✓	✓
GPT32EHm (m = 0 to 3) GPT32Em (m = 4 to 7)	通用PWM定时器周期设置Double-Buffer Register	GTPDBR	FFFF_FFFFh	4007 806Ch + 0100h × m	32	✓	-
	AD转换器启动请求时序Register A	GTADTRA	FFFF_FFFFh	4007 8070h + 0100h × m	32	✓	-
	AD转换器启动请求时序缓冲寄存器A	GTADTBRA	FFFF_FFFFh	4007 8074h + 0100h × m	32	✓	-
	AD转换器启动请求时序Double-Buffer Register A	GTADTDBRA	FFFF_FFFFh	4007 8078h + 0100h × m	32	✓	-
	AD转换器启动请求时序Register B	GTADTRB	FFFF_FFFFh	4007 807Ch + 0100h × m	32	✓	-
	AD转换器启动请求时序缓冲寄存器B	GTADTBRB	FFFF_FFFFh	4007 8080h + 0100h × m	32	✓	-
	AD转换器启动请求时序Double-Buffer Register B	GTADTDBRB	FFFF_FFFFh	4007 8084h + 0100h × m	32	✓	-
GPT32EHm (m = 0 to 3) GPT32Em (m = 4 to 7) GPT32m (m = 8 to 13)	通用PWM定时器死区时间控制寄存器	GTDTCR	0000_0000h	4007 8088h + 0100h × m	32	✓	(✓)*1
	通用PWM定时器死区时间值寄存器U	GTDVU	FFFF_FFFFh	4007 808Ch + 0100h × m	32	✓	✓
GPT32EHm (m = 0 to 3) GPT32Em (m = 4 to 7)	通用PWM定时器死区时间值寄存器D	GTDVD	FFFF_FFFFh	4007 8090h + 0100h × m	32	✓	-
	通用PWM定时器死区时间缓冲寄存器U	GTDBU	FFFF_FFFFh	4007 8094h + 0100h × m	32	✓	-
	通用PWM定时器死区时间缓冲寄存器D	GTDBD	FFFF_FFFFh	4007 8098h + 0100h × m	32	✓	-
	通用PWM定时器输出保护功能状态寄存器	GTSOS	0000_0000h	4007 809Ch + 0100h × m	32	✓	-
	通用PWM定时器输出保护功能临时释放寄存器	GTSOTR	0000_0000h	4007 80A0h + 0100h × m	32	✓	-
GPT_OPS	输出相位切换控制Register	OPSCR	0000_0000h	4007 8FF0h	32	✓	✓

Note 1. 从GPT32EHGPT32E减少了一些功能。

23.2.1 General PWM Timer Write-Protection Register (GTWP)

Address(es): GPT32EHm.GTWP 4007 8000h + 0100h × m (m = 0 to 3)
GPT32Em.GTWP 4007 8000h + 0100h × m (m = 4 to 7)
GPT32m.GTWP 4007 8000h + 0100h × m (m = 8 to 13)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PRKEY[7:0]								—	—	—	—	—	—	—	WP
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	WP	Register Write Disable	0: Enable writes to the affected registers 1: Disable writes to the affected registers.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15 to b8	PRKEY[7:0]	GTWP Key Code	When A5h is written to these bits, writing to the WP bit is permitted. These bits are read as 0.	R/W
b31 to b16	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

To prevent accidental changes, the GTWP register enables or disables writing to registers. The following is a list of write enabled or disabled registers:
GTSSR, GTPSR, GTCSR, GTUPSR, GTDNSR, GTICASR, GTICBSR, GTCR, GTUDDTYC, GTIOR, GTINTAD, GTST, GTBER, GTITC, GTCNT, GTCCRA, GTCCRB, GTCCRC, GTCCRD, GTCCRE, GTCCRF, GTPR, GTPBR, GTPDBR, GTADTRA, GTADTBRA, GTADTDBRA, GTADTRB, GTADTBRB, GTADTDBRB, GTDTCR, GTDVU, GTDVD, GTDBU, GTDBD, GTSOS, GTSOTR.

23.2.2 General PWM Timer Software Start Register (GTSTR)

Address(es): GPT32EHm.GTSTR 4007 8004h + 0100h × m (m = 0 to 3)
GPT32Em.GTSTR 4007 8004h + 0100h × m (m = 4 to 7)
GPT32m.GTSTR 4007 8004h + 0100h × m (m = 8 to 13)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	CSTRT 13	CSTRT 12	CSTRT 11	CSTRT 10	CSTRT 9	CSTRT 8	CSTRT 7	CSTRT 6	CSTRT 5	CSTRT 4	CSTRT 3	CSTRT 2	CSTRT 1	CSTRT 0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The GTSTR starts the GTCNT counter operation for each channel n, where n = 0 to 13.

The GTSTR bit number represents the channel number. The GTSTR register is shared by all of the channels. The GTCNT counter starts for the channel associated with the GTSTR bit where 1 is written. Writing 0 has no effect on the status of the GTCNT counter and the value of GTSTR register. For the association between the GTSTR bit number and a channel number, see Figure 23.2.

CSTRTn bit (Channel n GTCNT Count Start) (n = 0 to 13)

The CSTRTn bit starts channel n of the GTCNT counter operation. Writing to the GTSTR.CSTRTn bit (n = 0 to 13) has no effect unless the GPTm.GTSSR.CSTRT bit is set to 1 (for GPT32EH, m = EH0 to EH3, for GPT32E, m = E4 to E7, for GPT32, m = 8 to 13).

23.2.1 通用PWM定时器写保护寄存器(GTWP)

Address(es): GPT32EHm.GTWP 4007 8000h + 0100h × m (m = 0 to 3)
GPT32Em.GTWP 4007 8000h + 0100h × m (m = 4 to 7)
GPT32m.GTWP 4007 8000h + 0100h × m (m = 8 to 13)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PRKEY[7:0]								—	—	—	—	—	—	—	WP
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	WP	寄存器写禁用	0：允许写入受影响的寄存器1：禁止写入 受影响的寄存器。	R/W
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b15 to b8	PRKEY[7:0]	GTWP密钥代码	当A5h写入这些位时，允许写入WP位。这些位读为0。	R/W
b31 to b16	—	Reserved	这些位被读取为0。写入值应为0。	R/W

为防止意外更改，GTWP寄存器启用或禁用对寄存器的写入。以下是写启用或禁用寄存器的列表：
GTSSR, GTPSR, GTCSR, GTUPSR, GTDNSR, GTICASR, GTICBSR, GTCR, GTUDDTYC, GTIOR, GTINTAD, GTST, GTBER, GTITC, GTCNT, GTCCRA, GTCCRB, GTCCRC, GTCCRD, GTCCRE, GTCCRF, GTPR, GTPBR, GTPDBR, GTADTRA, GTADTBRA, GTADTDBRA, GTADTRB, GTADTBRB, GTADTDBRB, GTDTCR, GTDVU, GTDVD, GTDBU, GTDBD, GTSOS, GTSOTR.

23.2.2 通用PWM定时器软件启动寄存器(GTSTR)

Address(es): GPT32EHm.GTSTR 4007 8004h + 0100h × m (m = 0 to 3)
GPT32Em.GTSTR 4007 8004h + 0100h × m (m = 4 to 7)
GPT32m.GTSTR 4007 8004h + 0100h × m (m = 8 to 13)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	CSTRT 13	CSTRT 12	CSTRT 11	CSTRT 10	CSTRT 9	CSTRT 8	CSTRT 7	CSTRT 6	CSTRT 5	CSTRT 4	CSTRT 3	CSTRT 2	CSTRT 1	CSTRT 0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

GTSTR启动每个通道n的GTCNT计数器操作，其中n=0到13。

GTSTR位号代表通道号。GTSTR寄存器由所有通道共享。这
GTCNT计数器为与写入1的GTSTR位关联的通道启动。写0对GTCNT计数器的状态和GTSTR寄存器的值没有影响
。关于GTSTR位号和通道号之间的关联，请参见图23.2。

CSTRTn位（通道nGTCNT计数开始）（n=0至13）

CSTRTn位启动GTCNT计数器操作的通道n。除非GPTm.GTSSR.CSTRT位设置为1，否则写入GTSTR.CSTRTn位（n=0到13）无效（对于GPT32EH，m=EH0到EH3，对于GPT32E，m=E4到E7，对于GPT32 m=8到13）。

Read data shows the counter status of each channel (GTCR.CST bit). Zero means the counter is stopped and 1 means the counter is running.

23.2.3 General PWM Timer Software Stop Register (GTSTP)

Address(es): GPT32EHm.GTSTP 4007 8008h + 0100h × m (m = 0 to 3)
GPT32Em.GTSTP 4007 8008h + 0100h × m (m = 4 to 7)
GPT32m.GTSTP 4007 8008h + 0100h × m (m = 8 to 13)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	CSTOP 13	CSTOP 12	CSTOP 11	CSTOP 10	CSTOP 9	CSTOP 8	CSTOP 7	CSTOP 6	CSTOP 5	CSTOP 4	CSTOP 3	CSTOP 2	CSTOP 1	CSTOP 0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

The GTSTP register stops the GTCNT counter operation for each channel n, where n = 0 to 13.

The GTSTP bit number represents the channel number. The GTSTP register is shared by all of the channels. The GTCNT counter stops for the channel associated with the GTSTP bit in which 1 is written. Writing 0 has no effect on the status of GTCNT counter and the value of GTSTP register. For the association between the GTSTP bit number and a channel number, see Figure 23.2.

CSTOPn bit (Channel n GTCNT Count Stop) (n = 0 to 13)

The CSTOPn bit stops channel n of the GTCNT counter operation. Writing to the GTSTP.CSTOPn bit (n = 0 to 13) has no effect unless the GPTm.GTPSR.CSTOP bit is set to 1 (for GPT32EH, m = EH0 to EH3, for GPT32E, m = E4 to E7, for GPT32, m = 8 to 13).

Read data shows the counter status of each channel (invert of the GTCR.CST bit). Zero means the counter is running and 1 means the counter stops.

23.2.4 General PWM Timer Software Clear Register (GTCLR)

Address(es): GPT32EHm.GTCLR 4007 800Ch + 0100h × m (m = 0 to 3)
GPT32Em.GTCLR 4007 800Ch + 0100h × m (m = 4 to 7)
GPT32m.GTCLR 4007 800Ch + 0100h × m (m = 8 to 13)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	CCLR 13	CCLR 12	CCLR 11	CCLR 10	CCLR 9	CCLR 8	CCLR 7	CCLR 6	CCLR 5	CCLR 4	CCLR 3	CCLR 2	CCLR 1	CCLR 0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

GTCLR is a write-only register that clears the GTCNT counter operation for each channel n, where n = 0 to 13.

The GTCLR bit number represents the channel number. The GTCLR register is shared by all of the channels. The GTCNT counter is cleared for the channel associated with the GTCLR bit number where 1 is written. Writing 0 has no effect on the status of the GTCNT counter. For the association between the GTCLR bit number and a channel number, see Figure 23.2.

CCLRn bit (Channel n GTCNT Count Clear) (n = 0 to 13)

Channel n of the GTCNT counter value is cleared on writing 1 to the CCLRn bit. This bit is read as 0.

读取数据显示每个通道的计数器状态（GTCR.CST位）。零表示计数器停止，1表示计数器正在运行。

23.2.3 通用PWM定时器软件停止寄存器(GTSTP)

Address(es): GPT32EHm.GTSTP 4007 8008h + 0100h × m (m = 0 to 3)
GPT32Em.GTSTP 4007 8008h + 0100h × m (m = 4 to 7)
GPT32m.GTSTP 4007 8008h + 0100h × m (m = 8 to 13)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	CSTOP 13	CSTOP 12	CSTOP 11	CSTOP 10	CSTOP 9	CSTOP 8	CSTOP 7	CSTOP 6	CSTOP 5	CSTOP 4	CSTOP 3	CSTOP 2	CSTOP 1	CSTOP 0
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

GTSTP寄存器停止每个通道n的GTCNT计数器操作，其中n=0到13。

GTSTP位号代表通道号。GTSTP寄存器由所有通道共享。GTCNT计数器停止与写入1的GTSTP位关联的通道。写0对GTCNT计数器的状态和GTSTP寄存器的值没有影响。GTSTP比特编号与通道编号的关系见图23.2。

CSTOPn位（通道nGTCNT计数停止）（n=0到13）

CSTOPn位停止GTCNT计数器操作的通道n。除非GPTm.GTPSR.CSTOP位设置为1，否则写入GTSTP.CSTOPn位（n=0到13）无效（对于GPT32EH，m=EH0到EH3，对于GPT32E，m=E4到E7，对于GPT32 m=8到13）。

读取数据显示每个通道的计数器状态（反转GTCR.CST位）。零表示计数器正在运行，1表示计数器停止。

23.2.4 通用PWM定时器软件清零寄存器(GTCLR)

Address(es): GPT32EHm.GTCLR 4007 800Ch + 0100h × m (m = 0 to 3)
GPT32Em.GTCLR 4007 800Ch + 0100h × m (m = 4 to 7)
GPT32m.GTCLR 4007 800Ch + 0100h × m (m = 8 to 13)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	CCLR 13	CCLR 12	CCLR 11	CCLR 10	CCLR 9	CCLR 8	CCLR 7	CCLR 6	CCLR 5	CCLR 4	CCLR 3	CCLR 2	CCLR 1	CCLR 0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

GTCLR是一个只写寄存器，用于清除每个通道n的GTCNT计数器操作，其中n=0到13。

GTCLR位号代表通道号。GTCLR寄存器由所有通道共享。这
与写入1的GTCLR位号相关的通道的GTCNT计数器清零。写0对GTCNT计数器的状态没有影响。GTCLR位号和通道号之间的关联，见图23.2。

CCLRn位（通道nGTCNT计数清除）（n=0至13）

GTCNT计数器值的通道n在向CCLRn位写入1时被清除。该位读为0。

23.2.5 General PWM Timer Start Source Select Register (GTSSR)

Address(es): GPT32EHm.GTSSR 4007 8010h + 0100h × m (m = 0 to 3)
GPT32Em.GTSSR 4007 8010h + 0100h × m (m = 4 to 7)
GPT32m.GTSSR 4007 8010h + 0100h × m (m = 8 to 13)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	CSTRT	—	—	—	—	—	—	—	SSELCH	SSELCG	SSELCF	SSELCE	SSELCD	SSELCC	SSELCB	SSELCA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SSCBFAH	SSCBFAL	SSCBRAH	SSCBRAL	SSCAFBH	SSCAFBL	SSCARBH	SSCARBL	SSGTRGDF	SSGTRGDR	SSGTRGCF	SSGTRGCR	SSGTRGBF	SSGTRGBR	SSGTRGAF	SSGTRGAR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	SSGTRGAR	GTETRGA Pin Rising Input Source Counter Start Enable	0: Disable counter start on the rising edge of GTETRGA input 1: Enable counter start on the rising edge of GTETRGA input.	R/W
b1	SSGTRGAF	GTETRGA Pin Falling Input Source Counter Start Enable	0: Disable counter start on the falling edge of GTETRGA input 1: Enable counter start on the falling edge of GTETRGA input.	R/W
b2	SSGTRGBR	GTETRGB Pin Rising Input Source Counter Start Enable	0: Disable counter start on the rising edge of GTETRGB input 1: Enable counter start on the rising edge of GTETRGB input.	R/W
b3	SSGTRGBF	GTETRGB Pin Falling Input Source Counter Start Enable	0: Disable counter start on the falling edge of GTETRGB input 1: Enable counter start on the falling edge of GTETRGB input.	R/W
b4	SSGTRGCR	GTETRGC Pin Rising Input Source Counter Start Enable	0: Disable counter start on the rising edge of GTETRGC input 1: Enable counter start on the rising edge of GTETRGC input.	R/W
b5	SSGTRGCF	GTETRGC Pin Falling Input Source Counter Start Enable	0: Disable counter start on the falling edge of GTETRGC input 1: Enable counter start on the falling edge of GTETRGC input	R/W
b6	SSGTRGDR	GTETRGD Pin Rising Input Source Counter Start Enable	0: Disable counter start on the rising edge of GTETRGD input 1: Enable counter start on the rising edge of GTETRGD input.	R/W
b7	SSGTRGDF	GTETRGD Pin Falling Input Source Counter Start Enable	0: Disable counter start on the falling edge of GTETRGD input 1: Enable counter start on the falling edge of GTETRGD input.	R/W
b8	SSCARBL	GTIOCA Pin Rising Input during GTIOCB Value Low Source Counter Start Enable	0: Disable counter start on the rising edge of GTIOCA input when GTIOCB input is 0 1: Enable counter start on the rising edge of GTIOCA input when GTIOCB input is 0.	R/W
b9	SSCARBH	GTIOCA Pin Rising Input during GTIOCB Value High Source Counter Start Enable	0: Disable counter start on the rising edge of GTIOCA input when GTIOCB input is 1 1: Enable counter start on the rising edge of GTIOCA input when GTIOCB input is 1.	R/W
b10	SSCAFBL	GTIOCA Pin Falling Input during GTIOCB Value Low Source Counter Start Enable	0: Disable counter start on the falling edge of GTIOCA input when GTIOCB input is 0 1: Enable counter start on the falling edge of GTIOCA input when GTIOCB input is 0.	R/W

23.2.5 通用PWM定时器启动源选择寄存器(GTSSR)

Address(es): GPT32EHm.GTSSR 4007 8010h + 0100h × m (m = 0 to 3)
GPT32Em.GTSSR 4007 8010h + 0100h × m (m = 4 to 7)
GPT32m.GTSSR 4007 8010h + 0100h × m (m = 8 to 13)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	CSTRT	—	—	—	—	—	—	—	SSELCH	SSELCG	SSELCF	SSELCE	SSELCD	SSELCC	SSELCB	SSELCA
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SSCBFAH	SSCBFAL	SSCBRAH	SSCBRAL	SSCAFBH	SSCAFBL	SSCARBH	SSCARBL	SSGTRGDF	SSGTRGDR	SSGTRGCF	SSGTRGCR	SSGTRGBF	SSGTRGBR	SSGTRGAF	SSGTRGAR
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	SSGTRGAR	GTETRGA引脚上升输入源计数器启动启用	0：禁止在GTETRGA输入的上升沿启动计数器1：使能在GTETRGA输入的上升沿启动计数器。	R/W
b1	SSGTRGAF	GTETRGA引脚下降输入源计数器启动启用	0：禁止在GTETRGA输入的下降沿启动计数器1：使能在GTETRGA输入的下降沿启动计数器。	R/W
b2	SSGTRGBR	GTETRGB引脚上升输入源计数器启动启用	0：禁止在GTETRGB输入的上升沿启动计数器1：使能在GTETRGB输入的上升沿启动计数器。	R/W
b3	SSGTRGBF	GTETRGB引脚下降输入源计数器启动启用	0：禁止在GTETRGB输入的下降沿启动计数器1：使能在GTETRGB输入的下降沿启动计数器。	R/W
b4	SSGTRGCR	GTETRGC引脚上升沿输入源计数器启动启用	0：禁止在GTETRGC输入的上升沿启动计数器1：使能在GTETRGC输入的上升沿启动计数器。	R/W
b5	SSGTRGCF	GTETRGC引脚下降输入源计数器启动启用	0：禁止在GTETRGC输入的下降沿启动计数器1：使能在GTETRGC输入的下降沿启动计数器	R/W
b6	SSGTRGDR	GTETRGD引脚上升输入源计数器启动启用	0：禁止在GTETRGD输入的上升沿启动计数器1：使能在GTETRGD输入的上升沿启动计数器。	R/W
b7	SSGTRGDF	GTETRGD引脚下降输入源计数器启动启用	0：禁止在GTETRGD输入的下降沿启动计数器1：使能在GTETRGD输入的下降沿启动计数器。	R/W
b8	SSCARBL	GTIOCA引脚上升期间输入GTIOCB价值低来源计数器启动启用	0：当GTIOCB输入为0时，禁止在GTIOCA输入的上升沿启动计数器1：当GTIOCB输入为0时，使能在GTIOCA输入的上升沿启动计数器。	R/W
b9	SSCARBH	GTIOCA引脚上升期间输入GTIOCB价值高来源计数器启动启用	0：当GTIOCB输入为1时，禁止在GTIOCA输入上升沿启动计数器1：当GTIOCB输入为1时，使能在GTIOCA输入上升沿启动计数器。	R/W
b10	SSCAFBL	GTIOCA引脚下降期间输入GTIOCB价值低来源计数器启动启用	0：当GTIOCB输入为0时，禁止在GTIOCA输入的下降沿启动计数器1：当GTIOCB输入为0时，使能在GTIOCA输入的下降沿启动计数器。	R/W

Bit	Symbol	Bit name	Description	R/W
b11	SSCAFBH	GTIOCA Pin Falling Input during GTIOCB Value High Source Counter Start Enable	0: Disable counter start on the falling edge of GTIOCA input when GTIOCB input is 1 1: Enable counter start on the falling edge of GTIOCA input when GTIOCB input is 1.	R/W
b12	SSCBRAL	GTIOCB Pin Rising Input during GTIOCA Value Low Source Counter Start Enable	0: Disable counter start on the rising edge of GTIOCB input when GTIOCA input is 0 1: Enable counter start on the rising edge of GTIOCB input when GTIOCA input is 0.	R/W
b13	SSCBRAH	GTIOCB Pin Rising Input during GTIOCA Value High Source Counter Start Enable	0: Disable counter start on the rising edge of GTIOCB input when GTIOCA input is 1 1: Enable counter start on the rising edge of GTIOCB input when GTIOCA input is 1.	R/W
b14	SSCBFAL	GTIOCB Pin Falling Input during GTIOCA Value Low Source Counter Start Enable	0: Disable counter start on the falling edge of GTIOCB input when GTIOCA input is 0 1: Enable counter start on the falling edge of GTIOCB input when GTIOCA input is 0.	R/W
b15	SSCBFAH	GTIOCB Pin Falling Input during GTIOCA Value High Source Counter Start Enable	0: Disable counter start on the falling edge of GTIOCB input when GTIOCA input is 1 1: Enable counter start on the falling edge of GTIOCB input when GTIOCA input is 1.	R/W
b16	SSELCA	ELC_GPTA Event Source Counter Start Enable	0: Disable counter start on ELC_GPTA event input 1: Enable counter start on ELC_GPTA event input.	R/W
b17	SSELCB	ELC_GPTB Event Source Counter Start Enable	0: Disable counter start on ELC_GPTB event input 1: Enable counter start on ELC_GPTB event input.	R/W
b18	SSELCC	ELC_GPTC Event Source Counter Start Enable	0: Disable counter start on ELC_GPTC event input 1: Enable counter start on ELC_GPTC event input.	R/W
b19	SSELCD	ELC_GPTD Event Source Counter Start Enable	0: Disable counter start on ELC_GPTD event input 1: Enable counter start on ELC_GPTD event input.	R/W
b20	SSELCE	ELC_GPTE Event Source Counter Start Enable	0: Disable counter start on ELC_GPTE event input 1: Enable counter start on ELC_GPTE event input.	R/W
b21	SSELCF	ELC_GPTF Event Source Counter Start Enable	0: Disable counter start on ELC_GPTF event input 1: Enable counter start on ELC_GPTF event input.	R/W
b22	SSELCG	ELC_GPTG Event Source Counter Start Enable	0: Disable counter start on ELC_GPTG event input 1: Enable counter start on ELC_GPTG event input.	R/W
b23	SSELCH	ELC_GPTH Event Source Counter Start Enable	0: Disable counter start on ELC_GPTH event input 1: Enable counter start on ELC_GPTH event input.	R/W
b30 to b24	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b31	CSTRT	Software Source Counter Start Enable	0: Disable counter start by the GTSTR register 1: Enable counter start by the GTSTR register.	R/W

The GTSSR register sets the source to start the GTCNT counter.

SSGTRGAR bit (GTETRGA Pin Rising Input Source Counter Start Enable)

The SSGTRGAR bit enables or disables GTCNT counter start on the rising edge of the GTETRGA pin input.

SSGTRGAF bit (GTETRGA Pin Falling Input Source Counter Start Enable)

The SSGTRGAF bit enables or disables GTCNT counter start on the falling edge of the GTETRGA pin input.

SSGTRGBR bit (GTETRGB Pin Rising Input Source Counter Start Enable)

The SSGTRGBR bit enables or disables GTCNT counter start on the rising edge of the GTETRGB pin input.

SSGTRGBF bit (GTETRGB Pin Falling Input Source Counter Start Enable)

The SSGTRGBF bit enables or disables GTCNT counter start on the falling edge of the GTETRGB pin input.

SSGTRGCR bit (GTETRGC Pin Rising Input Source Counter Start Enable)

The SSGTRGCR bit enables or disables GTCNT counter start on the rising edge of the GTETRGC pin input.

Bit	Symbol	位名称	Description	R/W
b11	SSCAFBH	GTIOCA引脚下降期间输入GTIOCB价值高来源计数器启动启用	0：当GTIOCB输入为1时，禁止在GTIOCA输入的下降沿启动计数器1：当GTIOCB输入为1时，使能在GTIOCA输入的下降沿启动计数器。	R/W
b12	SSCBRAL	GTIOCB引脚上升期间输入GTIOCA价值低来源计数器启动启用	0：当GTIOCA输入为0时，禁止在GTIOCB输入的上升沿启动计数器1：当GTIOCA输入为0时，使能在GTIOCB输入的上升沿启动计数器。	R/W
b13	SSCBRAH	GTIOCB引脚上升期间输入GTIOCA价值高来源计数器启动启用	0：当GTIOCA输入为1时，禁止在GTIOCB输入的上升沿启动计数器1：当GTIOCA输入为1时，使能在GTIOCB输入的上升沿启动计数器。	R/W
b14	SSCBFAL	在GTIOCB引脚下降输入GTIOCA价值低来源计数器启动启用	0：当GTIOCA输入为0时，禁止在GTIOCB输入的下降沿启动计数器1：当GTIOCA输入为0时，使能在GTIOCB输入的下降沿启动计数器。	R/W
b15	SSCBFAH	在GTIOCB引脚下降输入GTIOCA价值高来源计数器启动启用	0：当GTIOCA输入为1时，禁止在GTIOCB输入的下降沿启动计数器1：当GTIOCA输入为1时，使能在GTIOCB输入的下降沿启动计数器。	R/W
b16	SSELCA	ELC_GPTA事件源计数器启动启用	0：在ELC_GPTA事件输入上禁用计数器启动1：在ELC_GPTA事件输入上启用计数器启动。	R/W
b17	SSELCB	ELC_GPTB事件源计数器启动启用	0：在ELC_GPTB事件输入上禁用计数器启动1：在ELC_GPTB事件输入上启用计数器启动。	R/W
b18	SSELCC	ELC_GPTC事件源计数器启动启用	0：在ELC_GPTC事件输入上禁用计数器启动1：在ELC_GPTC事件输入上启用计数器启动。	R/W
b19	SSELCD	ELC_GPTD事件源计数器启动启用	0：在ELC_GPTD事件输入上禁用计数器启动1：在ELC_GPTD事件输入上启用计数器启动。	R/W
b20	SSELCE	ELC_GPTE事件源计数器启动启用	0：在ELC_GPTE事件输入上禁用计数器启动1：在ELC_GPTE事件输入上启用计数器启动。	R/W
b21	SSELCF	ELC_GPTF事件源计数器启动启用	0：在ELC_GPTF事件输入上禁用计数器启动1：在ELC_GPTF事件输入上启用计数器启动。	R/W
b22	SSELCG	ELC_GPTG事件源计数器启动启用	0：在ELC_GPTG事件输入上禁用计数器启动1：在ELC_GPTG事件输入上启用计数器启动。	R/W
b23	SSELCH	ELC_GPTH事件源计数器启动启用	0：在ELC_GPTH事件输入上禁用计数器启动1：在ELC_GPTH事件输入上启用计数器启动。	R/W
b30 to b24	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b31	CSTRT	软件源计数器启动Enable	0：禁止由GTSTR寄存器启动计数器1：使能由GTSTR寄存器启动计数器。	R/W

GTSSR寄存器设置启动GTCNT计数器的源。

SSGTRGAR位（GTETRGA引脚上升沿输入源计数器启动使能）

SSGTRGAR位启用或禁用GTCNT计数器在GTETRGA引脚输入的上升沿启动。

SSGTRGAF位（GTETRGA引脚下降输入源计数器启动使能）

SSGTRGAF位启用或禁用GTCNT计数器在GTETRGA引脚输入的下降沿启动。

SSGTRGBR位（GTETRGB引脚上升输入源计数器启动使能）

SSGTRGBR位在GTETRGB引脚输入的上升沿启用或禁用GTCNT计数器启动。

SSGTRGBF位（GTETRGB引脚下降输入源计数器启动使能）

SSGTRGBF位在GTETRGB引脚输入的下降沿启用或禁用GTCNT计数器启动。

SSGTRGCR位（GTETRGC引脚上升沿输入源计数器启动使能）

SSGTRGCR位启用或禁用GTCNT计数器在GTETRGC引脚输入的上升沿启动。

SSGTRGCF bit (GTETRGC Pin Falling Input Source Counter Start Enable)

The SSGTRGCF bit enables or disables GTCNT counter start on the falling edge of the GTETRGC pin input.

SSGTRGDR bit (GTETRGD Pin Rising Input Source Counter Start Enable)

The SSGTRGDR bit enables or disables GTCNT counter start on the rising edge of the GTETRGD pin input.

SSGTRGDF bit (GTETRGD Pin Falling Input Source Counter Start Enable)

The SSGTRGDF bit enables or disables GTCNT counter start on the falling edge of the GTETRGD pin input.

SSCARBL bit (GTIOCA Pin Rising Input during GTIOCB Value Low Source Counter Start Enable)

The SSCARBL bit enables or disables GTCNT counter start on the rising edge of the GTIOCA pin input when the GTIOCB input is 0.

SSCARBH bit (GTIOCA Pin Rising Input during GTIOCB Value High Source Counter Start Enable)

The SSCARBH bit enables or disables GTCNT counter start on the rising edge of the GTIOCA pin input when the GTIOCB input is 1.

SSCAFBL bit (GTIOCA Pin Falling Input during GTIOCB Value Low Source Counter Start Enable)

The SSCAFBL bit enables or disables GTCNT counter start on the falling edge of the GTIOCA pin input when the GTIOCB input is 0.

SSCAFBH bit (GTIOCA Pin Falling Input during GTIOCB Value High Source Counter Start Enable)

The SSCAFBH bit enables or disables GTCNT counter start on the falling edge of the GTIOCA pin input when the GTIOCB input is 1.

SSCBRAL bit (GTIOCB Pin Rising Input during GTIOCA Value Low Source Counter Start Enable)

The SSCBRAL bit enables or disables GTCNT counter start on the rising edge of the GTIOCB pin input when the GTIOCA input is 0.

SSCBRAH bit (GTIOCB Pin Rising Input during GTIOCA Value High Source Counter Start Enable)

The SSCBRAH bit enables or disables GTCNT counter start on the rising edge of the GTIOCB pin input when the GTIOCA input is 1.

SSCBFAL bit (GTIOCB Pin Falling Input during GTIOCA Value Low Source Counter Start Enable)

The SSCBFAL bit enables or disables GTCNT counter start on the falling edge of the GTIOCB pin input when the GTIOCA input is 0.

SSCBFAH bit (GTIOCB Pin Falling Input during GTIOCA Value High Source Counter Start Enable)

The SSCBFAH bit enables or disables GTCNT counter start on the falling edge of the GTIOCB pin input when the GTIOCA input is 1.

SSELCm bit (ELC_GPTm Event Source Counter Start Enable) (m = A to H)

The SSELCm bit enables or disables GTCNT counter start on the ELC_GPTm event input.

CSTRT bit (Software Source Counter Start Enable)

The CSTRT bit enables or disables GTCNT counter start by the GTSTR register.

SSGTRGCF位（GTETRGC引脚下降输入源计数器启动使能）

SSGTRGCF位使能或禁止GTCNT计数器在GTETRGC引脚输入的下降沿启动。

SSGTRGDR位（GTETRGD引脚上升沿输入源计数器启动使能）

SSGTRGDR位启用或禁用GTCNT计数器在GTETRGD引脚输入的上升沿启动。

SSGTRGDF位（GTETRGD引脚下降输入源计数器启动使能）

SSGTRGDF位启用或禁用GTCNT计数器在GTETRGD引脚输入的下降沿启动。

SSCARBL位（GTIOCB值低电平期间的GTIOCA引脚上升沿输入源计数器启动使能）

SSCARBL位启用或禁用GTCNT计数器在GTIOCA引脚输入的上升沿启动，当GTIOCB输入为0。

SSCARBH位（GTIOCB值高源计数器启动启用期间GTIOCA引脚上升沿输入）

SSCARBH位启用或禁用GTCNT计数器在GTIOCA引脚输入的上升沿启动，当GTIOCB输入为1。

SSCAFBL位（GTIOCB值低源计数器启动启用期间的GTIOCA引脚下降输入）

SSCAFBL位启用或禁用GTCNT计数器在GTIOCA引脚输入的下降沿启动，当GTIOCB输入为0。

SSCAFBH位（GTIOCB值高源计数器启动启用期间GTIOCA引脚下降输入）

SSCAFBH位启用或禁用GTCNT计数器在GTIOCA引脚输入的下降沿启动，当GTIOCB输入为1。

SSCBRAL位（GTIOCA值低源计数器启动启用期间GTIOCB引脚上升沿输入）

SSCBRAL位启用或禁用GTCNT计数器在GTIOCB引脚输入的上升沿启动，当GTIOCA输入为0。

SSCBRAH位（GTIOCA值高源计数器启动启用期间的GTIOCB引脚上升沿输入）

SSCBRAH位启用或禁用GTCNT计数器在GTIOCB引脚输入的上升沿启动，当GTIOCA输入为1。

SSCBFAL位（GTIOCA值低源计数器启动启用期间的GTIOCB引脚下降输入）

SSCBFAL位启用或禁用GTCNT计数器在GTIOCB引脚输入的下降沿启动，当GTIOCA输入为0。

SSCBFAH位（GTIOCA值高源计数器启动启用期间GTIOCB引脚下降输入）

SSCBFAH位启用或禁用GTCNT计数器在GTIOCB引脚输入的下降沿启动，当GTIOCA输入为1。

SSELCm位（ELC_GPTm事件源计数器启动启用）（m=A到H）

SSELCm位在ELC_GPTm事件输入上启用或禁用GTCNT计数器启动。

CSTRT位（软件源计数器启动使能）

CSTRT位启用或禁用由GTSTR寄存器启动的GTCNT计数器。

23.2.6 General PWM Timer Stop Source Select Register (GTPSR)

Address(es): GPT32EHm.GTPSR 4007 8014h + 0100h × m (m = 0 to 3)
GPT32Em.GTPSR 4007 8014h + 0100h × m (m = 4 to 7)
GPT32m.GTPSR 4007 8014h + 0100h × m (m = 8 to 13)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	CSTOP	—	—	—	—	—	—	—	PSELCH	PSELCG	PSELCF	PSELCE	PSELCD	PSELCC	PSELCB	PSELCA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PSCBFAH	PSCBFAL	PSCBRAH	PSCBRAL	PSCAFBH	PSCAFBL	PSCARBH	PSCARBL	PSGTRGDF	PSGTRGDR	PSGTRGCF	PSGTRGCR	PSGTRGBF	PSGTRGBR	PSGTRGAF	PSGTRGAR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	PSGTRGAR	GTETRGA Pin Rising Input Source Counter Stop Enable	0: Disable counter stop on the rising edge of GTETRGA input 1: Enable counter stop on the rising edge of GTETRGA input.	R/W
b1	PSGTRGAF	GTETRGA Pin Falling Input Source Counter Stop Enable	0: Disable counter stop on the falling edge of GTETRGA input 1: Enable counter stop on the falling edge of GTETRGA input.	R/W
b2	PSGTRGBR	GTETRGB Pin Rising Input Source Counter Stop Enable	0: Disable counter stop on the rising edge of GTETRGB input 1: Enable counter stop on the rising edge of GTETRGB input.	R/W
b3	PSGTRGBF	GTETRGB Pin Falling Input Source Counter Stop Enable	0: Disable counter stop on the falling edge of GTETRGB input 1: Enable counter stop on the falling edge of GTETRGB input.	R/W
b4	PSGTRGCR	GTETRGC Pin Rising Input Source Counter Stop Enable	0: Disable counter stop on the rising edge of GTETRGC input 1: Enable counter stop on the rising edge of GTETRGC input.	R/W
b5	PSGTRGCF	GTETRGC Pin Falling Input Source Counter Stop Enable	0: Disable counter stop on the falling edge of GTETRGC input 1: Enable counter stop on the falling edge of GTETRGC input.	R/W
b6	PSGTRGDR	GTETRGD Pin Rising Input Source Counter Stop Enable	0: Disable counter stop on the rising edge of GTETRGD input 1: Enable counter stop on the rising edge of GTETRGD input.	R/W
b7	PSGTRGDF	GTETRGD Pin Falling Input Source Counter Stop Enable	0: Disable counter stop on the falling edge of GTETRGD input 1: Enable counter stop on the falling edge of GTETRGD input.	R/W
b8	PSCARBL	GTIOCA Pin Rising Input during GTIOCB Value Low Source Counter Stop Enable	0: Disable counter stop on the rising edge of GTIOCA input when GTIOCB input is 0 1: Enable counter stop on the rising edge of GTIOCA input when GTIOCB input is 0.	R/W
b9	PSCARBH	GTIOCA Pin Rising Input during GTIOCB Value High Source Counter Stop Enable	0: Disable counter stop on the rising edge of GTIOCA input when GTIOCB input is 1 1: Enable counter stop on the rising edge of GTIOCA input when GTIOCB input is 1.	R/W
b10	PSCAFBL	GTIOCA Pin Falling Input during GTIOCB Value Low Source Counter Stop Enable	0: Disable counter stop on the falling edge of GTIOCA input when GTIOCB input is 0 1: Enable counter stop on the falling edge of GTIOCA input when GTIOCB input is 0.	R/W

23.2.6 通用PWM定时器停止源选择寄存器(GTPSR)

Address(es): GPT32EHm.GTPSR 4007 8014h + 0100h × m (m = 0 to 3)
GPT32Em.GTPSR 4007 8014h + 0100h × m (m = 4 to 7)
GPT32m.GTPSR 4007 8014h + 0100h × m (m = 8 to 13)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	CSTOP	—	—	—	—	—	—	—	PSELCH	PSELCG	PSELCF	PSELCE	PSELCD	PSELCC	PSELCB	PSELCA
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PSCBFAH	PSCBFAL	PSCBRAH	PSCBRAL	PSCAFBH	PSCAFBL	PSCARBH	PSCARBL	PSGTRGDF	PSGTRGDR	PSGTRGCF	PSGTRGCR	PSGTRGBF	PSGTRGBR	PSGTRGAF	PSGTRGAR
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	PSGTRGAR	GTETRGA引脚上升输入源计数器停止启用	0：在GTETRGA输入的上升沿禁止计数器停止1：在GTETRGA输入的上升沿使能计数器停止。	R/W
b1	PSGTRGAF	GTETRGA引脚下降输入源计数器停止启用	0：在GTETRGA输入的下降沿禁用计数器停止1：在GTETRGA输入的下降沿启用计数器停止。	R/W
b2	PSGTRGBR	GTETRGB引脚上升输入源计数器停止启用	0：在GTETRGB输入上升沿禁止计数器停止1：在GTETRGB输入上升沿使能计数器停止。	R/W
b3	PSGTRGBF	GTETRGB引脚下降输入源计数器停止启用	0：在GTETRGB输入的下降沿禁用计数器停止1：在GTETRGB输入的下降沿启用计数器停止。	R/W
b4	PSGTRGCR	GTETRGC引脚上升沿输入源计数器停止启用	0：在GTETRGC输入的上升沿禁止计数器停止1：在GTETRGC输入的上升沿使能计数器停止。	R/W
b5	PSGTRGCF	GTETRGC引脚下降输入源计数器停止启用	0：在GTETRGC输入的下降沿禁用计数器停止1：在GTETRGC输入的下降沿启用计数器停止。	R/W
b6	PSGTRGDR	GTETRGD引脚上升输入源计数器停止启用	0：在GTETRGD输入的上升沿禁止计数器停止1：在GTETRGD输入的上升沿使能计数器停止。	R/W
b7	PSGTRGDF	GTETRGD引脚下降输入源计数器停止启用	0：在GTETRGD输入的下降沿禁止计数器停止1：在GTETRGD输入的下降沿使能计数器停止。	R/W
b8	PSCARBL	GTIOCA引脚上升期间输入GTIOCB价值低来源计数器停止启用	0：当GTIOCB输入为0时，在GTIOCA输入上升沿禁止计数器停止1：当GTIOCB输入为0时，在GTIOCA输入上升沿使能计数器停止。	R/W
b9	PSCARBH	GTIOCA引脚上升期间输入GTIOCB价值高来源计数器停止启用	0：当GTIOCB输入为1时，在GTIOCA输入上升沿禁止计数器停止1：当GTIOCB输入为1时，在GTIOCA输入上升沿使能计数器停止。	R/W
b10	PSCAFBL	GTIOCA引脚下降期间输入GTIOCB价值低来源计数器停止启用	0：当GTIOCB输入为0时，在GTIOCA输入下降沿禁止计数器停止1：当GTIOCB输入为0时，在GTIOCA输入下降沿使能计数器停止。	R/W

Bit	Symbol	Bit name	Description	R/W
b11	PSCAFBH	GTIOCA Pin Falling Input during GTIOCB Value High Source Counter Stop Enable	0: Disable counter stop on the falling edge of GTIOCA input when GTIOCB input is 1 1: Enable counter stop on the falling edge of GTIOCA input when GTIOCB input is 1.	R/W
b12	PSCBRAL	GTIOCB Pin Rising Input during GTIOCA Value Low Source Counter Stop Enable	0: Disable counter stop on the rising edge of GTIOCB input when GTIOCA input is 0 1: Enable counter stop on the rising edge of GTIOCB input when GTIOCA input is 0.	R/W
b13	PSCBRAH	GTIOCB Pin Rising Input during GTIOCA Value High Source Counter Stop Enable	0: Disable counter stop on the rising edge of GTIOCB input when GTIOCA input is 1 1: Enable counter stop on the rising edge of GTIOCB input when GTIOCA input is 1.	R/W
b14	PSCBFAL	GTIOCB Pin Falling Input during GTIOCA Value Low Source Counter Stop Enable	0: Disable counter stop on the falling edge of GTIOCB input when GTIOCA input is 0 1: Enable counter stop on the falling edge of GTIOCB input when GTIOCA input is 0	R/W
b15	PSCBFAH	GTIOCB Pin Falling Input during GTIOCA Value High Source Counter Stop Enable	0: Disable counter stop on the falling edge of GTIOCB input when GTIOCA input is 1 1: Enable counter stop on the falling edge of GTIOCB input when GTIOCA input is 1	R/W
b16	PSELCA	ELC_GPTA Event Source Counter Stop Enable	0: Disable counter stop on ELC_GPTA event input 1: Enable counter stop on ELC_GPTA event input.	R/W
b17	PSELCB	ELC_GPTB Event Source Counter Stop Enable	0: Disable counter stop on ELC_GPTB event input 1: Enable counter stop on ELC_GPTB event input.	R/W
b18	PSELCC	ELC_GPTC Event Source Counter Stop Enable	0: Disable counter stop on ELC_GPTC event input 1: Enable counter stop on ELC_GPTC event input.	R/W
b19	PSELCD	ELC_GPTD Event Source Counter Stop Enable	0: Disable counter stop on ELC_GPTD event input 1: Enable counter stop on ELC_GPTD event input.	R/W
b20	PSELCE	ELC_GPTE Event Source Counter Stop Enable	0: Disable counter stop on ELC_GPTE event input 1: Enable counter stop on ELC_GPTE event input.	R/W
b21	PSELCF	ELC_GPTF Event Source Counter Stop Enable	0: Disable counter stop on ELC_GPTF event input 1: Enable counter stop on ELC_GPTF event input.	R/W
b22	PSELCG	ELC_GPTG Event Source Counter Stop Enable	0: Disable counter stop on ELC_GPTG event input 1: Enable counter stop on ELC_GPTG event input.	R/W
b23	PSELCH	ELC_GPTH Event Source Counter Stop Enable	0: Disable counter stop on ELC_GPTH event input 1: Enable counter stop on ELC_GPTH event input.	R/W
b30 to b24	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b31	CSTOP	Software Source Counter Stop Enable	0: Disable counter stop by the GTSTP register 1: Enable counter stop by the GTSTP register.	R/W

The GTPSR register sets the source to stop the GTCNT counter.

PSGTRGAR bit (GTETRGA Pin Rising Input Source Counter Stop Enable)

The PSGTRGAR bit enables or disables GTCNT counter stop on the rising edge of the GTETRGA pin input.

PSGTRGAF bit (GTETRGA Pin Falling Input Source Counter Stop Enable)

The PSGTRGAF bit enables or disables GTCNT counter stop on the falling edge of the GTETRGA pin input.

PSGTRGBR bit (GTETRGB Pin Rising Input Source Counter Stop Enable)

The PSGTRGBR bit enables or disables GTCNT counter stop on the rising edge of the GTETRGB pin input.

PSGTRGBF bit (GTETRGB Pin Falling Input Source Counter Stop Enable)

The PSGTRGBF bit enables or disables GTCNT counter stop on the falling edge of the GTETRGB pin input.

PSGTRGCR bit (GTETRGC Pin Rising Input Source Counter Stop Enable)

The PSGTRGCR bit enables or disables GTCNT counter stop on the rising edge of the GTETRGC pin input.

Bit	Symbol	位名称	Description	R/W
b11	PSCAFBH	GTIOCA引脚下降期间输入GTIOCB价值高来源计数器停止启用	0：当GTIOCB输入为1时，在GTIOCA输入下降沿禁止计数器停止1：当GTIOCB输入为1时，在GTIOCA输入下降沿使能计数器停止。	R/W
b12	PSCBRAL	GTIOCB引脚上升期间输入GTIOCA价值低来源计数器停止启用	0：当GTIOCA输入为0时，在GTIOCB输入上升沿禁止计数器停止1：当GTIOCA输入为0时，在GTIOCB输入上升沿使能计数器停止。	R/W
b13	PSCBRAH	GTIOCB引脚上升期间输入GTIOCA价值高来源计数器停止启用	0：当GTIOCA输入为1时，在GTIOCB输入上升沿禁止计数器停止1：当GTIOCA输入为1时，在GTIOCB输入上升沿使能计数器停止。	R/W
b14	PSCBFAL	在GTIOCB引脚下降输入GTIOCA价值低来源计数器停止启用	0：当GTIOCA输入为0时，在GTIOCB输入的下降沿禁止计数器停止1：当GTIOCA输入为0时，在GTIOCB输入的下降沿使能计数器停止	R/W
b15	PSCBFAH	在GTIOCB引脚下降输入GTIOCA价值高来源计数器停止启用	0：当GTIOCA输入为1时，在GTIOCB输入下降沿禁止计数器停止1：当GTIOCA输入为1时，在GTIOCB输入下降沿使能计数器停止	R/W
b16	PSELCA	ELC_GPTA事件源计数器停止启用	0：在ELC_GPTA事件输入上禁用计数器停止1：在ELC_GPTA事件输入上启用计数器停止。	R/W
b17	PSELCB	ELC_GPTB事件源计数器停止启用	0：在ELC_GPTB事件输入上禁用计数器停止1：在ELC_GPTB事件输入上启用计数器停止。	R/W
b18	PSELCC	ELC_GPTC事件源计数器停止启用	0：在ELC_GPTC事件输入上禁用计数器停止1：在ELC_GPTC事件输入上启用计数器停止。	R/W
b19	PSELCD	ELC_GPTD事件源计数器停止启用	0：在ELC_GPTD事件输入上禁用计数器停止1：在ELC_GPTD事件输入上启用计数器停止。	R/W
b20	PSELCE	ELC_GPTE事件源计数器停止启用	0：在ELC_GPTE事件输入上禁用计数器停止1：在ELC_GPTE事件输入上启用计数器停止。	R/W
b21	PSELCF	ELC_GPTF事件源计数器停止启用	0：在ELC_GPTF事件输入上禁用计数器停止1：在ELC_GPTF事件输入上启用计数器停止。	R/W
b22	PSELCG	ELC_GPTG事件源计数器停止启用	0：在ELC_GPTG事件输入上禁用计数器停止1：在ELC_GPTG事件输入上启用计数器停止。	R/W
b23	PSELCH	ELC_GPTH事件源计数器停止启用	0：在ELC_GPTH事件输入上禁用计数器停止1：在ELC_GPTH事件输入上启用计数器停止。	R/W
b30 to b24	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b31	CSTOP	软件源计数器停止Enable	0：通过GTSTP寄存器禁止计数器停止1：通过GTSTP寄存器使能计数器停止。	R/W

GTPSR寄存器设置停止GTCNT计数器的源。

PSGTRGAR位（GTETRGA引脚上升沿输入源计数器停止使能）

PSGTRGAR位在GTETRGA引脚输入的上升沿启用或禁用GTCNT计数器停止。

PSGTRGAF位（GTETRGA引脚下降输入源计数器停止使能）

PSGTRGAF位在GTETRGA引脚输入的下降沿启用或禁用GTCNT计数器停止。

PSGTRGBR位（GTETRGB引脚上升输入源计数器停止使能）

PSGTRGBR位在GTETRGB引脚输入的上升沿启用或禁用GTCNT计数器停止。

PSGTRGBF位（GTETRGB引脚下降输入源计数器停止使能）

PSGTRGBF位在GTETRGB引脚输入的下降沿启用或禁用GTCNT计数器停止。

PSGTRGCR位（GTETRGC引脚上升沿输入源计数器停止使能）

PSGTRGCR位在GTETRGC引脚输入的上升沿启用或禁用GTCNT计数器停止。

PSGTRGCF bit (GTETRGC Pin Falling Input Source Counter Stop Enable)

The PSGTRGCF bit enables or disables GTCNT counter stop on the falling edge of the GTETRGC pin input.

PSGTRGDR bit (GTETRGD Pin Rising Input Source Counter Stop Enable)

The PSGTRGDR bit enables or disables GTCNT counter stop on the rising edge of the GTETRGD pin input.

PSGTRGDF bit (GTETRGD Pin Falling Input Source Counter Stop Enable)

The PSGTRGDF bit enables or disables GTCNT counter stop on the falling edge of the GTETRGD pin input.

PSCARBL bit (GTIOCA Pin Rising Input during GTIOCB Value Low Source Counter Stop Enable)

The PSCARBL bit enables or disables GTCNT counter stop on the rising edge of the GTIOCA pin input when the GTIOCB input is 0.

PSCARBH bit (GTIOCA Pin Rising Input during GTIOCB Value High Source Counter Stop Enable)

The PSCARBH bit enables or disables GTCNT counter stop on the rising edge of the GTIOCA pin input when the GTIOCB input is 1.

PSCAFBL bit (GTIOCA Pin Falling Input during GTIOCB Value Low Source Counter Stop Enable)

The PSCAFBL bit enables or disables GTCNT counter stop on the falling edge of the GTIOCA pin input when the GTIOCB input is 0.

PSCAFBH bit (GTIOCA Pin Falling Input during GTIOCB Value High Source Counter Stop Enable)

The PSCAFBH bit enables or disables GTCNT counter stop on the falling edge of the GTIOCA pin input when the GTIOCB input is 1.

PSCBRAL bit (GTIOCB Pin Rising Input during GTIOCA Value Low Source Counter Stop Enable)

The PSCBRAL bit enables or disables GTCNT counter stop on the rising edge of the GTIOCB pin input when the GTIOCA input is 0.

PSCBRAH bit (GTIOCB Pin Rising Input during GTIOCA Value High Source Counter Stop Enable)

The PSCBRAH bit enables or disables GTCNT counter stop on the rising edge of the GTIOCB pin input when the GTIOCA input is 1.

PSCBFAL bit (GTIOCB Pin Falling Input during GTIOCA Value Low Source Counter Stop Enable)

The PSCBFAL bit enables or disables GTCNT counter stop on the falling edge of the GTIOCB pin input when the GTIOCA input is 0.

PSCBFAH bit (GTIOCB Pin Falling Input during GTIOCA Value High Source Counter Stop Enable)

The PSCBFAH bit enables or disables GTCNT counter stop on the falling edge of the GTIOCB pin input when the GTIOCA input is 1.

PSELCm bit (ELC_GPTm Event Source Counter Stop Enable) (m = A to H)

The PSELCm bit enables or disables GTCNT counter stop on the ELC_GPTm event input.

CSTOP bit (Software Source Counter Stop Enable)

The CSTOP bit enables or disables GTCNT counter stop by the GTSTP register.

PSGTRGCF位（GTETRGC引脚下降输入源计数器停止使能）

PSGTRGCF位在GTETRGC引脚输入的下降沿启用或禁用GTCNT计数器停止。

PSGTRGDR位（GTETRGD引脚上升输入源计数器停止使能）

PSGTRGDR位在GTETRGD引脚输入的上升沿启用或禁用GTCNT计数器停止。

PSGTRGDF位（GTETRGD引脚下降输入源计数器停止使能）

PSGTRGDF位在GTETRGD引脚输入的下降沿启用或禁用GTCNT计数器停止。

PSCARBL位（GTIOCB值低源计数器停止使能期间GTIOCA引脚上升沿输入）

PSCARBL位在GTIOCA引脚输入的上升沿启用或禁用GTCNT计数器停止，当GTIOCB输入为0。

PSCARBH位（GTIOCB值高源计数器停止使能期间GTIOCA引脚上升沿输入）

PSCARBH位在GTIOCA引脚输入的上升沿启用或禁用GTCNT计数器停止，当GTIOCB输入为1。

PSCAFBL位（GTIOCB值低源计数器停止使能期间GTIOCA引脚下降输入）

PSCAFBL位在GTIOCA引脚输入的下降沿启用或禁用GTCNT计数器停止，当GTIOCB输入为0。

PSCAFBH位（GTIOCB值高源计数器停止使能期间GTIOCA引脚下降输入）

PSCAFBH位在GTIOCA引脚输入的下降沿启用或禁用GTCNT计数器停止，当GTIOCB输入为1。

PSCBRAL位（GTIOCA值低源计数器停止使能期间GTIOCB引脚上升沿输入）

PSCBRAL位在GTIOCB引脚输入的上升沿启用或禁用GTCNT计数器停止，当GTIOCA输入为0。

PSCBRAH位（GTIOCA值高源计数器停止使能期间GTIOCB引脚上升沿输入）

PSCBRAH位在GTIOCB引脚输入的上升沿启用或禁用GTCNT计数器停止，当GTIOCA输入为1。

PSCBFAL位（GTIOCA值低源计数器停止使能期间GTIOCB引脚下降输入）

PSCBFAL位在GTIOCB引脚输入的下降沿启用或禁用GTCNT计数器停止，当GTIOCA输入为0。

PSCBFAH位（GTIOCA值高源计数器停止使能期间GTIOCB引脚下降输入）

PSCBFAH位在GTIOCB引脚输入的下降沿启用或禁用GTCNT计数器停止，当GTIOCA输入为1。

PSELCm位（ELC_GPTm事件源计数器停止使能）（m=A到H）

PSELCm位启用或禁用ELC_GPTm事件输入上的GTCNT计数器停止。

CSTOP位（软件源计数器停止使能）

CSTOP位通过GTSTP寄存器启用或禁用GTCNT计数器停止。

23.2.7 General PWM Timer Clear Source Select Register (GTCSR)

Address(es): GPT32EHm.GTCSR 4007 8018h + 0100h × m (m = 0 to 3)
GPT32Em.GTCSR 4007 8018h + 0100h × m (m = 4 to 7)
GPT32m.GTCSR 4007 8018h + 0100h × m (m = 8 to 13)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	CCLR	—	—	—	—	—	—	—	CSELCH	CSELCG	CSELCF	CSELCE	CSELCD	CSELCC	CSELCB	CSELCA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CSCBFAH	CSCBFAL	CSCBRAH	CSCBRAL	CSCAFBH	CSCAFBL	CSCARBH	CSCARBL	CSGTRGDF	CSGTRGDR	CSGTRGCF	CSGTRGCR	CSGTRGBF	CSGTRGBR	CSGTRGAF	CSGTRGAR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	CSGTRGAR	GTETRGA Pin Rising Input Source Counter Clear Enable	0: Disable counter clear on the rising edge of GTETRGA input 1: Enable counter clear on the rising edge of GTETRGA input.	R/W
b1	CSGTRGAF	GTETRGA Pin Falling Input Source Counter Clear Enable	0: Disable counter clear on the falling edge of GTETRGA input 1: Enable counter clear on the falling edge of GTETRGA input.	R/W
b2	CSGTRGBR	GTETRGB Pin Rising Input Source Counter Clear Enable	0: Disable counter clear on the rising edge of GTETRGB input 1: Enable counter clear on the rising edge of GTETRGB input.	R/W
b3	CSGTRGBF	GTETRGB Pin Falling Input Source Counter Clear Enable	0: Disable counter clear on the falling edge of GTETRGB input 1: Enable counter clear on the falling edge of GTETRGB input.	R/W
b4	CSGTRGCR	GTETRGC Pin Rising Input Source Counter Clear Enable	0: Disable counter clear on the rising edge of GTETRGC input 1: Enable counter clear on the rising edge of GTETRGC input.	R/W
b5	CSGTRGCF	GTETRGC Pin Falling Input Source Counter Clear Enable	0: Disable counter clear on the falling edge of GTETRGC input 1: Enable counter clear on the falling edge of GTETRGC input.	R/W
b6	CSGTRGDR	GTETRGD Pin Rising Input Source Counter Clear Enable	0: Disable counter clear on the rising edge of GTETRGD input 1: Enable counter clear on the rising edge of GTETRGD input.	R/W
b7	CSGTRGDF	GTETRGD Pin Falling Input Source Counter Clear Enable	0: Disable counter clear on the falling edge of GTETRGD input 1: Enable counter clear on the falling edge of GTETRGD input.	R/W
b8	CSCARBL	GTIOCA Pin Rising Input during GTIOCB Value Low Source Counter Clear Enable	0: Disable counter clear on the rising edge of GTIOCA input when GTIOCB input is 0 1: Enable counter clear on the rising edge of GTIOCA input when GTIOCB input is 0.	R/W
b9	CSCARBH	GTIOCA Pin Rising Input during GTIOCB Value High Source Counter Clear Enable	0: Disable counter clear on the rising edge of GTIOCA input when GTIOCB input is 1 1: Enable counter clear on the rising edge of GTIOCA input when GTIOCB input is 1.	R/W
b10	CSCAFBL	GTIOCA Pin Falling Input during GTIOCB Value Low Source Counter Clear Enable	0: Disable counter clear on the falling edge of GTIOCA input when GTIOCB input is 0 1: Enable counter clear on the falling edge of GTIOCA input when GTIOCB input is 0.	R/W

23.2.7 通用PWM定时器清零源选择寄存器(GTCSR)

Address(es): GPT32EHm.GTCSR 4007 8018h + 0100h × m (m = 0 to 3)
GPT32Em.GTCSR 4007 8018h + 0100h × m (m = 4 to 7)
GPT32m.GTCSR 4007 8018h + 0100h × m (m = 8 to 13)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	CCLR	—	—	—	—	—	—	—	CSELCH	CSELCG	CSELCF	CSELCE	CSELCD	CSELCC	CSELCB	CSELCA
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CSCBFAH	CSCBFAL	CSCBRAH	CSCBRAL	CSCAFBH	CSCAFBL	CSCARBH	CSCARBL	CSGTRGDF	CSGTRGDR	CSGTRGCF	CSGTRGCR	CSGTRGBF	CSGTRGBR	CSGTRGAF	CSGTRGAR
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	CSGTRGAR	GTETRGA引脚上升输入源计数器清除启用	0：在GTETRGA输入的上升沿禁止计数器清零1：在GTETRGA输入的上升沿使能计数器清零。	R/W
b1	CSGTRGAF	GTETRGA引脚下降输入源计数器清除启用	0：禁止在GTETRGA输入的下降沿清除计数器1：使能在GTETRGA输入的下降沿清除计数器。	R/W
b2	CSGTRGBR	GTETRGB引脚上升输入源计数器清除启用	0：在GTETRGB输入的上升沿禁止计数器清零1：在GTETRGB输入的上升沿使能计数器清零。	R/W
b3	CSGTRGBF	GTETRGB引脚下降输入源计数器清除启用	0：在GTETRGB输入的下降沿禁止计数器清零1：在GTETRGB输入的下降沿使能计数器清零。	R/W
b4	CSGTRGCR	GTETRGC引脚上升沿输入源计数器清除启用	0：在GTETRGC输入的上升沿禁止计数器清除1：在GTETRGC输入的上升沿使能计数器清除。	R/W
b5	CSGTRGCF	GTETRGC引脚下降输入源计数器清除启用	0：在GTETRGC输入的下降沿禁止计数器清零1：在GTETRGC输入的下降沿使能计数器清零。	R/W
b6	CSGTRGDR	GTETRGD引脚上升输入源计数器清除启用	0：在GTETRGD输入的上升沿禁止计数器清除1：在GTETRGD输入的上升沿使能计数器清除。	R/W
b7	CSGTRGDF	GTETRGD引脚下降输入源计数器清除启用	0：禁止在GTETRGD输入的下降沿清除计数器1：使能在GTETRGD输入的下降沿清除计数器。	R/W
b8	CSCARBL	GTIOCA引脚上升期间输入GTIOCB价值低来源计数器清除启用	0：当GTIOCB输入为0时，在GTIOCA输入的上升沿禁止计数器清零1：当GTIOCB输入为0时，在GTIOCA输入的上升沿使能计数器清零。	R/W
b9	CSCARBH	GTIOCA引脚上升期间输入GTIOCB价值高来源计数器清除启用	0：当GTIOCB输入为1时，在GTIOCA输入上升沿禁止计数器清零1：当GTIOCB输入为1时，在GTIOCA输入上升沿使能计数器清零。	R/W
b10	CSCAFBL	GTIOCA引脚下降期间输入GTIOCB价值低来源计数器清除启用	0：当GTIOCB输入为0时，在GTIOCA输入的下降沿禁止计数器清零1：当GTIOCB输入为0时，在GTIOCA输入的下降沿使能计数器清零。	R/W

Bit	Symbol	Bit name	Description	R/W
b11	CSCAFBH	GTIOCA Pin Falling Input during GTIOCB Value High Source Counter Clear Enable	0: Disable counter clear on the falling edge of GTIOCA input when GTIOCB input is 1 1: Enable counter clear on the falling edge of GTIOCA input when GTIOCB input is 1.	R/W
b12	CSCBRAL	GTIOCB Pin Rising Input during GTIOCA Value Low Source Counter Clear Enable	0: Disable counter clear on the rising edge of GTIOCB input when GTIOCA input is 0 1: Enable counter clear on the rising edge of GTIOCB input when GTIOCA input is 0.	R/W
b13	CSCBRAH	GTIOCB Pin Rising Input during GTIOCA Value High Source Counter Clear Enable	0: Disable counter clear on the rising edge of GTIOCB input when GTIOCA input is 1 1: Enable counter clear on the rising edge of GTIOCB input when GTIOCA input is 1.	R/W
b14	CSCBFAL	GTIOCB Pin Falling Input during GTIOCA Value Low Source Counter Clear Enable	0: Disable counter clear on the falling edge of GTIOCB input when GTIOCA input is 0 1: Enable counter clear on the falling edge of GTIOCB input when GTIOCA input is 0.	R/W
b15	CSCBFAH	GTIOCB Pin Falling Input during GTIOCA Value High Source Counter Clear Enable	0: Disable counter clear on the falling edge of GTIOCB input when GTIOCA input is 1 1: Enable counter clear on the falling edge of GTIOCB input when GTIOCA input is 1.	R/W
b16	CSELCA	ELC_GPTA Event Source Counter Clear Enable	0: Disable counter clear on ELC_GPTA event input 1: Enable counter clear on ELC_GPTA event input.	R/W
b17	CSELCB	ELC_GPTB Event Source Counter Clear Enable	0: Disable counter clear on ELC_GPTB event input 1: Enable counter clear on ELC_GPTB event input.	R/W
b18	CSELCC	ELC_GPTC Event Source Counter Clear Enable	0: Disable counter clear on ELC_GPTC event input 1: Enable counter clear on ELC_GPTC event input.	R/W
b19	CSELCD	ELC_GPTD Event Source Counter Clear Enable	0: Disable counter clear on ELC_GPTD event input 1: Enable counter clear on ELC_GPTD event input.	R/W
b20	CSELCE	ELC_GPTE Event Source Counter Clear Enable	0: Disable counter clear on ELC_GPTE event input 1: Enable counter clear on ELC_GPTE event input.	R/W
b21	CSELCF	ELC_GPTF Event Source Counter Clear Enable	0: Disable counter clear on ELC_GPTF event input 1: Enable counter clear on ELC_GPTF event input.	R/W
b22	CSELCG	ELC_GPTG Event Source Counter Clear Enable	0: Disable counter clear on ELC_GPTG event input 1: Enable counter clear on ELC_GPTG event input.	R/W
b23	CSELCH	ELC_GPTH Event Source Counter Clear Enable	0: Disable counter clear on ELC_GPTH event input 1: Enable counter clear on ELC_GPTH event input.	R/W
b30 to b24	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b31	CCLR	Software Source Counter Clear Enable	0: Disable counter clear by the GTCLR register 1: Enable counter clear by the GTCLR register.	R/W

GTCSR sets the source to clear the GTCNT counter.

CSGTRGAR bit (GTETRGA Pin Rising Input Source Counter Clear Enable)

The CSGTRGAR bit enables or disables GTCNT counter clear on the rising edge of the GTETRGA pin input.

CSGTRGAF bit (GTETRGA Pin Falling Input Source Counter Clear Enable)

The CSGTRGAF bit enables or disables GTCNT counter clear on the falling edge of the GTETRGA pin input.

CSGTRGBR bit (GTETRGB Pin Rising Input Source Counter Clear Enable)

The CSGTRGBR bit enables or disables GTCNT counter clear on the rising edge of the GTETRGB pin input.

CSGTRGBF bit (GTETRGB Pin Falling Input Source Counter Clear Enable)

The CSGTRGBF bit enables or disables GTCNT counter clear on the falling edge of the GTETRGB pin input.

CSGTRGCR bit (GTETRGC Pin Rising Input Source Counter Clear Enable)

The CSGTRGCR bit enables or disables GTCNT counter clear on the rising edge of the GTETRGC pin input.

Bit	Symbol	位名称	Description	R/W
b11	CSCAFBH	GTIOCA引脚下降期间输入GTIOCB价值高来源计数器清除启用	0：当GTIOCB输入为1时，在GTIOCA输入的下降沿禁止计数器清零1：当GTIOCB输入为1时，在GTIOCA输入的下降沿使能计数器清零。	R/W
b12	CSCBRAL	GTIOCB引脚上升期间输入GTIOCA价值低来源计数器清除启用	0：当GTIOCA输入为0时，在GTIOCB输入的上升沿禁止计数器清零1：当GTIOCA输入为0时，在GTIOCB输入的上升沿使能计数器清零。	R/W
b13	CSCBRAH	GTIOCB引脚上升期间输入GTIOCA价值高来源计数器清除启用	0：当GTIOCA输入为1时，在GTIOCB输入的上升沿禁止计数器清零1：当GTIOCA输入为1时，在GTIOCB输入的上升沿使能计数器清零。	R/W
b14	CSCBFAL	在GTIOCB引脚下降输入GTIOCA价值低来源计数器清除启用	0：当GTIOCA输入为0时，在GTIOCB输入的下降沿禁止计数器清零1：当GTIOCA输入为0时，在GTIOCB输入的下降沿使能计数器清零。	R/W
b15	CSCBFAH	在GTIOCB引脚下降输入GTIOCA价值高来源计数器清除启用	0：当GTIOCA输入为1时，在GTIOCB输入的下降沿禁止计数器清零1：当GTIOCA输入为1时，在GTIOCB输入的下降沿使能计数器清零。	R/W
b16	CSELCA	ELC_GPTA事件源计数器清除启用	0：在ELC_GPTA事件输入上禁用计数器清除1：在ELC_GPTA事件输入上启用计数器清除。	R/W
b17	CSELCB	ELC_GPTB事件源计数器清除启用	0：在ELC_GPTB事件输入上禁用计数器清除1：在ELC_GPTB事件输入上启用计数器清除。	R/W
b18	CSELCC	ELC_GPTC事件源计数器清除启用	0：在ELC_GPTC事件输入上禁用计数器清除1：在ELC_GPTC事件输入上启用计数器清除。	R/W
b19	CSELCD	ELC_GPTD事件源计数器清除启用	0：在ELC_GPTD事件输入上禁用计数器清除1：在ELC_GPTD事件输入上启用计数器清除。	R/W
b20	CSELCE	ELC_GPTE事件源计数器清除启用	0：在ELC_GPTE事件输入上禁用计数器清除1：在ELC_GPTE事件输入上启用计数器清除。	R/W
b21	CSELCF	ELC_GPTF事件源计数器清除启用	0：在ELC_GPTF事件输入上禁用计数器清除1：在ELC_GPTF事件输入上启用计数器清除。	R/W
b22	CSELCG	ELC_GPTG事件源计数器清除启用	0：在ELC_GPTG事件输入上禁用计数器清除1：在ELC_GPTG事件输入上启用计数器清除。	R/W
b23	CSELCH	ELC_GPTH事件源计数器清除启用	0：在ELC_GPTH事件输入上禁用计数器清除1：在ELC_GPTH事件输入上启用计数器清除。	R/W
b30 to b24	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b31	CCLR	软件源计数器清零Enable	0：禁止通过GTCLR寄存器清除计数器1：允许通过GTCLR寄存器清除计数器。	R/W

GTCSR设置源以清除GTCNT计数器。

CSGTRGAR位（GTETRGA引脚上升沿输入源计数器清零使能）

CSGTRGAR位在GTETRGA引脚输入的上升沿启用或禁用GTCNT计数器清零。

CSGTRGAF位（GTETRGA引脚下降输入源计数器清零使能）

CSGTRGAF位在GTETRGA引脚输入的下降沿启用或禁用GTCNT计数器清零。

CSGTRGBR位（GTETRGB引脚上升沿输入源计数器清零使能）

CSGTRGBR位在GTETRGB引脚输入的上升沿启用或禁用GTCNT计数器清零。

CSGTRGBF位（GTETRGB引脚下降输入源计数器清零使能）

CSGTRGBF位在GTETRGB引脚输入的下降沿启用或禁用GTCNT计数器清零。

CSGTRGCR位（GTETRGC引脚上升沿输入源计数器清零使能）

CSGTRGCR位在GTETRGC引脚输入的上升沿启用或禁用GTCNT计数器清零。

CSGTRGCF bit (GTETRGC Pin Falling Input Source Counter Clear Enable)

The CSGTRGCF bit enables or disables GTCNT counter clear on the falling edge of the GTETRGC pin input.

CSGTRGDR bit (GTETRGD Pin Rising Input Source Counter Clear Enable)

The CSGTRGDR bit enables or disables GTCNT counter clear on the rising edge of the GTETRGD pin input.

CSGTRGDF bit (GTETRGD Pin Falling Input Source Counter Clear Enable)

The CSGTRGDF bit enables or disables GTCNT counter clear on the falling edge of the GTETRGD pin input.

CSCARBL bit (GTIOCA Pin Rising Input during GTIOCB Value Low Source Counter Clear Enable)

The CSCARBL bit enables or disables GTCNT counter clear on the rising edge of the GTIOCA pin input when the GTIOCB input is 0.

CSCARBH bit (GTIOCA Pin Rising Input during GTIOCB Value High Source Counter Clear Enable)

The CSCARBH bit enables or disables GTCNT counter clear on the rising edge of the GTIOCA pin input when the GTIOCB input is 1.

CSCAFBL bit (GTIOCA Pin Falling Input during GTIOCB Value Low Source Counter Clear Enable)

The CSCAFBL bit enables or disables GTCNT counter clear on the falling edge of the GTIOCA pin input when the GTIOCB input is 0.

CSCAFBH bit (GTIOCA Pin Falling Input during GTIOCB Value High Source Counter Clear Enable)

The CSCAFBH bit enables or disables GTCNT counter clear on the falling edge of the GTIOCA pin input when the GTIOCB input is 1.

CSCBRAL bit (GTIOCB Pin Rising Input during GTIOCA Value Low Source Counter Clear Enable)

The CSCBRAL bit enables or disables GTCNT counter clear on the rising edge of the GTIOCB pin input when the GTIOCA input is 0.

CSCBRAH bit (GTIOCB Pin Rising Input during GTIOCA Value High Source Counter Clear Enable)

The CSCBRAH bit enables or disables GTCNT counter clear on the rising edge of the GTIOCB pin input when the GTIOCA input is 1.

CSCBFAL bit (GTIOCB Pin Falling Input during GTIOCA Value Low Source Counter Clear Enable)

The CSCBFAL bit enables or disables GTCNT counter clear on the falling edge of the GTIOCB pin input when the GTIOCA input is 0.

CSCBFAH bit (GTIOCB Pin Falling Input during GTIOCA Value High Source Counter Clear Enable)

The CSCBFAH bit enables or disables GTCNT counter clear on the falling edge of the GTIOCB pin input when the GTIOCA input is 1.

CSELCm bit (ELC_GPTm Event Source Counter Clear Enable) (m = A to H)

The CSELCm bit enables or disables GTCNT counter clear on the ELC_GPTm event input.

CCLR bit (Software Source Counter Clear Enable)

The CCLR bit enables or disables GTCNT counter clear by the GTCLR register.

CSGTRGCF位（GTETRGC引脚下降输入源计数器清零使能）

CSGTRGCF位在GTETRGC引脚输入的下降沿启用或禁用GTCNT计数器清零。

CSGTRGDR位（GTETRGD引脚上升沿输入源计数器清零使能）

CSGTRGDR位在GTETRGD引脚输入的上升沿启用或禁用GTCNT计数器清零。

CSGTRGDF位（GTETRGD引脚下降输入源计数器清零使能）

CSGTRGDF位在GTETRGD引脚输入的下降沿启用或禁用GTCNT计数器清零。

CSCARBL位（在GTIOCB值低源计数器清除启用期间GTIOCA引脚上升输入）

CSCARBL位在GTIOCA引脚输入的上升沿启用或禁用GTCNT计数器清零，当GTIOCB输入为0。

CSCARBH位（GTIOCB值高电平期间的GTIOCA引脚上升沿输入源计数器清零使能）

CSCARBH位在GTIOCA引脚输入的上升沿启用或禁用GTCNT计数器清零，当GTIOCB输入为1。

CSCAFBL位（GTIOCB值低源计数器清除启用期间GTIOCA引脚下降输入）

CSCAFBL位在GTIOCA引脚输入的下降沿启用或禁用GTCNT计数器清零，当GTIOCB输入为0。

CSCAFBH位（在GTIOCB值高源计数器清除启用期间GTIOCA引脚下降输入）

CSCAFBH位在GTIOCA引脚输入的下降沿启用或禁用GTCNT计数器清零，当GTIOCB输入为1。

CSCBRAL位（GTIOCA值低源计数器清除启用期间GTIOCB引脚上升沿输入）

CSCBRAL位在GTIOCB引脚输入的上升沿启用或禁用GTCNT计数器清零，当GTIOCA输入为0。

CSCBRAH位（GTIOCA值高源计数器清除启用期间GTIOCB引脚上升沿输入）

CSCBRAH位在GTIOCB引脚输入的上升沿启用或禁用GTCNT计数器清零，当GTIOCA输入为1。

CSCBFAL位（GTIOCA值低源计数器清除启用期间GTIOCB引脚下降输入）

CSCBFAL位在GTIOCB引脚输入的下降沿启用或禁用GTCNT计数器清零，当GTIOCA输入为0。

CSCBFAH位（GTIOCA值高源计数器清零启用期间的GTIOCB引脚下降输入）

CSCBFAH位在GTIOCB引脚输入的下降沿启用或禁用GTCNT计数器清零，当GTIOCA输入为1。

CSELCm位（ELC_GPTm事件源计数器清除启用）（m=A到H）

CSELCm位启用或禁用ELC_GPTm事件输入上的GTCNT计数器清零。

CCLR位（软件源计数器清除使能）

CCLR位启用或禁用由GTCLR寄存器清除的GTCNT计数器。

23.2.8 General PWM Timer Up Count Source Select Register (GTUPSR)

Address(es): GPT32EHm.GTUPSR 4007 801Ch + 0100h × m (m = 0 to 3)
GPT32Em.GTUPSR 4007 801Ch + 0100h × m (m = 4 to 7)
GPT32m.GTUPSR 4007 801Ch + 0100h × m (m = 8 to 13)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	USELCH	USELCG	USELCF	USELCE	USELCD	USELCC	USELCB	USELCA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	USCBFAH	USCBFAL	USCBRAH	USCBRAL	USCAFBH	USCAFBL	USCARBH	USCARBL	USGTRGDF	USGTRGDR	USGTRGCF	USGTRGCR	USGTRGBF	USGTRGBR	USGTRGAF	USGTRGAR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	USGTRGAR	GTETRGA Pin Rising Input Source Counter Count Up Enable	0: Disable counter count up on the rising edge of GTETRGA input 1: Enable counter count up on the rising edge of GTETRGA input.	R/W
b1	USGTRGAF	GTETRGA Pin Falling Input Source Counter Count Up Enable	0: Disable counter count up on the falling edge of GTETRGA input 1: Enable counter count up on the falling edge of GTETRGA input.	R/W
b2	USGTRGBR	GTETRGB Pin Rising Input Source Counter Count Up Enable	0: Disable counter count up on the rising edge of GTETRGB input 1: Enable counter count up on the rising edge of GTETRGB input.	R/W
b3	USGTRGBF	GTETRGB Pin Falling Input Source Counter Count Up Enable	0: Disable counter count up on the falling edge of GTETRGB input 1: Enable counter count up on the falling edge of GTETRGB input.	R/W
b4	USGTRGCR	GTETRGC Pin Rising Input Source Counter Count Up Enable	0: Disable counter count up on the rising edge of GTETRGC input 1: Enable counter count up on the rising edge of GTETRGC input.	R/W
b5	USGTRGCF	GTETRGC Pin Falling Input Source Counter Count Up Enable	0: Disable counter count up on the falling edge of GTETRGC input 1: Enable counter count up on the falling edge of GTETRGC input.	R/W
b6	USGTRGDR	GTETRGD Pin Rising Input Source Counter Count Up Enable	0: Disable counter count up on the rising edge of GTETRGD input 1: Enable counter count up on the rising edge of GTETRGD input.	R/W
b7	USGTRGDF	GTETRGD Pin Falling Input Source Counter Count Up Enable	0: Disable counter count up on the falling edge of GTETRGD input 1: Enable counter count up on the falling edge of GTETRGD input.	R/W
b8	USCARBL	GTIOCA Pin Rising Input during GTIOCB Value Low Source Counter Count Up Enable	0: Disable counter count up on the rising edge of GTIOCA input when GTIOCB input is 0 1: Enable counter count up on the rising edge of GTIOCA input when GTIOCB input is 0.	R/W
b9	USCARBH	GTIOCA Pin Rising Input during GTIOCB Value High Source Counter Count Up Enable	0: Disable counter count up on the rising edge of GTIOCA input when GTIOCB input is 1 1: Enable counter count up on the rising edge of GTIOCA input when GTIOCB input is 1.	R/W
b10	USCAFBL	GTIOCA Pin Falling Input during GTIOCB Value Low Source Counter Count Up Enable	0: Disable counter count up on the falling edge of GTIOCA input when GTIOCB input is 0 1: Enable counter count up on the falling edge of GTIOCA input when GTIOCB input is 0.	R/W

23.2.8 通用PWM定时器向上计数源选择寄存器(GTUPSR)

Address(es): GPT32EHm.GTUPSR 4007 801Ch + 0100h × m (m = 0 to 3)
GPT32Em.GTUPSR 4007 801Ch + 0100h × m (m = 4 to 7)
GPT32m.GTUPSR 4007 801Ch + 0100h × m (m = 8 to 13)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	USELCH	USELCG	USELCF	USELCE	USELCD	USELCC	USELCB	USELCA
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	USCBFAH	USCBFAL	USCBRAH	USCBRAL	USCAFBH	USCAFBL	USCARBH	USCARBL	USGTRGDF	USGTRGDR	USGTRGCF	USGTRGCR	USGTRGBF	USGTRGBR	USGTRGAF	USGTRGAR
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	USGTRGAR	GTETRGA引脚上升输入源计数器计数启用	0：在GTETRGA输入的上升沿禁止计数器向上计数1：在GTETRGA输入的上升沿使能计数器向上计数。	R/W
b1	USGTRGAF	GTETRGA引脚下降输入源计数器计数启用	0：在GTETRGA输入的下降沿禁止计数器向上计数 1：在GTETRGA输入的下降沿使能计数器向上计数 。	R/W
b2	USGTRGBR	GTETRGB引脚上升输入源计数器计数启用	0：在GTETRGB输入的上升沿禁止计数器向上计数1：在GTETRGB输入的上升沿使能计数器向上计数。	R/W
b3	USGTRGBF	GTETRGB引脚下降输入源计数器计数启用	0：在GTETRGB输入的下降沿禁止计数器向上计数 1：在GTETRGB输入的下降沿使能计数器向上计数 。	R/W
b4	USGTRGCR	GTETRGC引脚上升沿输入源计数器计数启用	0：在GTETRGC输入的上升沿禁止计数器向上计数1：在GTETRGC输入的上升沿使能计数器向上计数。	R/W
b5	USGTRGCF	GTETRGC引脚下降输入源计数器计数启用	0：在GTETRGC输入的下降沿禁止计数器向上计数 1：在GTETRGC输入的下降沿使能计数器向上计数 。	R/W
b6	USGTRGDR	GTETRGD引脚上升输入源计数器计数启用	0：在GTETRGD输入的上升沿禁止计数器向上计数1：在GTETRGD输入的上升沿使能计数器向上计数。	R/W
b7	USGTRGDF	GTETRGD引脚下降输入源计数器计数启用	0：在GTETRGD输入的下降沿禁止计数器向上计数 1：在GTETRGD输入的下降沿使能计数器向上计数 。	R/W
b8	USCARBL	GTIOCA引脚上升期间输入GTIOCB价值低来源计数器计数启用	0：当GTIOCB输入为0时，在GTIOCA输入上升沿禁止计数器向上计数1：当GTIOCB输入为0时，在GTIOCA输入上升沿使能计数器向上计数。	R/W
b9	USCARBH	GTIOCA引脚上升期间输入GTIOCB价值高来源计数器计数启用	0：当GTIOCB输入为1时，在GTIOCA输入上升沿禁止计数器向上计数1：当GTIOCB输入为1时，在GTIOCA输入上升沿使能计数器向上计数。	R/W
b10	USCAFBL	GTIOCA引脚下降期间输入GTIOCB价值低来源计数器计数启用	0：当GTIOCB输入为0时，在GTIOCA输入的下降沿禁止计数器向上计数1：当GTIOCB输入为0时，在GTIOCA输入的下降沿使能计数器向上计数。	R/W

Bit	Symbol	Bit name	Description	R/W
b11	USCAFBH	GTIOCA Pin Falling Input during GTIOCB Value High Source Counter Count Up Enable	0: Disable counter count up on the falling edge of GTIOCA input when GTIOCB input is 1 1: Enable counter count up on the falling edge of GTIOCA input when GTIOCB input is 1.	R/W
b12	USCBRAL	GTIOCB Pin Rising Input during GTIOCA Value Low Source Counter Count Up Enable	0: Disable counter count up on the rising edge of GTIOCB input when GTIOCA input is 0 1: Enable counter count up on the rising edge of GTIOCB input when GTIOCA input is 0.	R/W
b13	USCBRAH	GTIOCB Pin Rising Input during GTIOCA Value High Source Counter Count Up Enable	0: Disable counter count up on the rising edge of GTIOCB input when GTIOCA input is 1 1: Enable counter count up on the rising edge of GTIOCB input when GTIOCA input is 1.	R/W
b14	USCBFAL	GTIOCB Pin Falling Input during GTIOCA Value Low Source Counter Count Up Enable	0: Disable counter count up on the falling edge of GTIOCB input when GTIOCA input is 0 1: Enable counter count up on the falling edge of GTIOCB input when GTIOCA input is 0.	R/W
b15	USCBFAH	GTIOCB Pin Falling Input during GTIOCA Value High Source Counter Count Up Enable	0: Disable counter count up on the falling edge of GTIOCB input when GTIOCA input is 1 1: Enable counter count up on the falling edge of GTIOCB input when GTIOCA input is 1.	R/W
b16	USELCA	ELC_GPTA Event Source Counter Count Up Enable	0: Disable counter count up on ELC_GPTA event input 1: Enable counter count up on ELC_GPTA event input.	R/W
b17	USELCB	ELC_GPTB Event Source Counter Count Up Enable	0: Disable counter count up on ELC_GPTB event input 1: Enable counter count up on ELC_GPTB event input.	R/W
b18	USELCC	ELC_GPTC Event Source Counter Count Up Enable	0: Disable counter count up on ELC_GPTC event input 1: Enable counter count up on ELC_GPTC event input.	R/W
b19	USELCD	ELC_GPTD Event Source Counter Count Up Enable	0: Disable counter count up on ELC_GPTD event input 1: Enable counter count up on ELC_GPTD event input.	R/W
b20	USELCE	ELC_GPTE Event Source Counter Count Up Enable	0: Disable counter count up on ELC_GPTE event input 1: Enable counter count up on ELC_GPTE event input.	R/W
b21	USELCF	ELC_GPTF Event Source Counter Count Up Enable	0: Disable counter count up on ELC_GPTF event input 1: Enable counter count up on ELC_GPTF event input.	R/W
b22	USELCG	ELC_GPTG Event Source Counter Count Up Enable	0: Disable counter count up on ELC_GPTG event input 1: Enable counter count up on ELC_GPTG event input.	R/W
b23	USELCH	ELC_GPTH Event Source Counter Count Up Enable	0: Disable counter count up on ELC_GPTH event input 1: Enable counter count up on ELC_GPTH event input.	R/W
b31 to b24	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The GTUPSR register sets the source to count up the GTCNT counter.

When at least one bit in the GTUPSR register is set to 1, the GTCNT counter is counted up by the source that is set to 1 in this register. In this case, GTCR.TPCS has no effect.

USGTRGAR bit (GTETRGA Pin Rising Input Source Counter Count Up Enable)

The USGTRGAR bit enables or disables GTCNT counter count up on the rising edge of the GTETRGA pin input.

USGTRGAF bit (GTETRGA Pin Falling Input Source Counter Count Up Enable)

The USGTRGAF bit enables or disables GTCNT counter count up on the falling edge of the GTETRGA pin input.

USGTRGBR bit (GTETRGB Pin Rising Input Source Counter Count Up Enable)

The USGTRGBR bit enables or disables GTCNT counter count up on the rising edge of the GTETRGB pin input.

USGTRGBF bit (GTETRGB Pin Falling Input Source Counter Count Up Enable)

The USGTRGBF bit enables or disables GTCNT counter count up on the falling edge of the GTETRGB pin input.

USGTRGCR bit (GTETRGC Pin Rising Input Source Counter Count Up Enable)

The USGTRGCR bit enables or disables GTCNT counter count up on the rising edge of the GTETRGC pin input.

Bit	Symbol	位名称	Description	R/W
b11	USCAFBH	GTIOCA引脚下降期间输入GTIOCB价值高来源计数器计数启用	0：当GTIOCB输入为1时，在GTIOCA输入的下降沿禁止计数器向上计数1：当GTIOCB输入为1时，在GTIOCA输入的下降沿使能计数器向上计数。	R/W
b12	USCBRAL	GTIOCB引脚上升期间输入GTIOCA价值低来源计数器计数启用	0：当GTIOCA输入为0时，在GTIOCB输入的上升沿禁止计数器向上计数1：当GTIOCA输入为0时，在GTIOCB输入的上升沿使能计数器向上计数。	R/W
b13	USCBRAH	GTIOCB引脚上升期间输入GTIOCA价值高来源计数器计数启用	0：当GTIOCA输入为1时，在GTIOCB输入上升沿禁止计数器向上计数1：当GTIOCA输入为1时，在GTIOCB输入上升沿使能计数器向上计数。	R/W
b14	USCBFAL	在GTIOCB引脚下降输入GTIOCA价值低来源计数器计数启用	0：当GTIOCA输入为0时，在GTIOCB输入的下降沿禁止计数器向上计数1：当GTIOCA输入为0时，在GTIOCB输入的下降沿使能计数器向上计数。	R/W
b15	USCBFAH	在GTIOCB引脚下降输入GTIOCA价值高来源计数器计数启用	0：当GTIOCA输入为1时，在GTIOCB输入下降沿禁止计数器向上计数1：当GTIOCA输入为1时，在GTIOCB输入下降沿使能计数器向上计数。	R/W
b16	USELCA	ELC_GPTA事件源计数器计数启用	0：在ELC_GPTA事件输入上禁用计数器向上计数1：在ELC_GPTA事件输入上启用计数器向上计数。	R/W
b17	USELCB	ELC_GPTB事件源计数器计数启用	0：在ELC_GPTB事件输入上禁用计数器向上计数1：在ELC_GPTB事件输入上启用计数器向上计数。	R/W
b18	USELCC	ELC_GPTC事件源计数器计数启用	0：在ELC_GPTC事件输入上禁用计数器向上计数1：在ELC_GPTC事件输入上启用计数器向上计数。	R/W
b19	USELCD	ELC_GPTD事件源计数器计数启用	0：在ELC_GPTD事件输入上禁用计数器向上计数1：在ELC_GPTD事件输入上启用计数器向上计数。	R/W
b20	USELCE	ELC_GPTE事件源计数器计数启用	0：在ELC_GPTE事件输入上禁用计数器向上计数1：在ELC_GPTE事件输入上启用计数器向上计数。	R/W
b21	USELCF	ELC_GPTF事件源计数器计数启用	0：在ELC_GPTF事件输入上禁用计数器向上计数1：在ELC_GPTF事件输入上启用计数器向上计数。	R/W
b22	USELCG	ELC_GPTG事件源计数器计数启用	0：在ELC_GPTG事件输入上禁用计数器向上计数1：在ELC_GPTG事件输入上启用计数器向上计数。	R/W
b23	USELCH	ELC_GPTH事件源计数器计数启用	0：在ELC_GPTH事件输入上禁用计数器向上计数1：在ELC_GPTH事件输入上启用计数器向上计数。	R/W
b31 to b24	—	Reserved	这些位被读取为0。写入值应为0。	R/W

GTUPSR寄存器设置源以向上计数GTCNT计数器。

当GTUPSR寄存器中的至少一位设置为1时，GTCNT计数器由该寄存器中设置为1的源进行计数。在这种情况下，GTCR.TPCS无效。

USGTRGAR位（GTETRGA引脚上升沿输入源计数器向上计数使能）

USGTRGAR位在GTETRGA引脚输入的上升沿启用或禁用GTCNT计数器向上计数。

USGTRGAF位（GTETRGA引脚下降输入源计数器向上计数使能）

USGTRGAF位在GTETRGA引脚输入的下降沿启用或禁用GTCNT计数器向上计数。

USGTRGBR位（GTETRGB引脚上升输入源计数器向上计数使能）

USGTRGBR位在GTETRGB引脚输入的上升沿启用或禁用GTCNT计数器向上计数。

USGTRGBF位（GTETRGB引脚下降输入源计数器向上计数使能）

USGTRGBF位在GTETRGB引脚输入的下降沿启用或禁用GTCNT计数器向上计数。

USGTRGCR位（GTETRGC引脚上升沿输入源计数器向上计数使能）

USGTRGCR位在GTETRGC引脚输入的上升沿启用或禁用GTCNT计数器向上计数。

USGTRGCF bit (GTETRGC Pin Falling Input Source Counter Count Up Enable)

The USGTRGCF bit enables or disables GTCNT counter count up on the falling edge of the GTETRGC pin input.

USGTRGDR bit (GTETRGD Pin Rising Input Source Counter Count Up Enable)

The USGTRGDR bit enables or disables GTCNT counter count up on the rising edge of the GTETRGD pin input.

USGTRGDF bit (GTETRGD Pin Falling Input Source Counter Count Up Enable)

The USGTRGDF bit enables or disables GTCNT counter count up on the falling edge of the GTETRGD pin input.

USCARBL bit (GTIOCA Pin Rising Input during GTIOCB Value Low Source Counter Count Up Enable)

The USCARBL bit enables or disables GTCNT counter count up on the rising edge of the GTIOCA pin input when GTIOCB input is 0.

USCARBH bit (GTIOCA Pin Rising Input during GTIOCB Value High Source Counter Count Up Enable)

The USCARBH bit enables or disables GTCNT counter count up on the rising edge of the GTIOCA pin input when the GTIOCB input is 1.

USCAFBL bit (GTIOCA Pin Falling Input during GTIOCB Value Low Source Counter Count Up Enable)

The USCAFBL bit enables or disables GTCNT counter count up on the falling edge of the GTIOCA pin input when the GTIOCB input is 0.

USCAFBH bit (GTIOCA Pin Falling Input during GTIOCB Value High Source Counter Count Up Enable)

The USCAFBH bit enables or disables GTCNT counter count up on the falling edge of the GTIOCA pin input when the GTIOCB input is 1.

USCBRAL bit (GTIOCB Pin Rising Input during GTIOCA Value Low Source Counter Count Up Enable)

The USCBRAL bit enables or disables GTCNT counter count up on the rising edge of the GTIOCB pin input when the GTIOCA input is 0.

USCBRAH bit (GTIOCB Pin Rising Input during GTIOCA Value High Source Counter Count Up Enable)

The USCBRAH bit enables or disables GTCNT counter count up on the rising edge of the GTIOCB pin input when the GTIOCA input is 1.

USCBFAL bit (GTIOCB Pin Falling Input during GTIOCA Value Low Source Counter Count Up Enable)

The USCBFAL bit enables or disables GTCNT counter count up on the falling edge of the GTIOCB pin input when the GTIOCA input is 0.

USCBFAH bit (GTIOCB Pin Falling Input during GTIOCA Value High Source Counter Count Up Enable)

The USCBFAH bit enables or disables GTCNT counter count up on the falling edge of the GTIOCB pin input when the GTIOCA input is 1.

USELCm bit (ELC_GPTm Event Source Counter Count Up Enable) (m = A to H)

The USELCm bit enables or disables GTCNT counter count up on the ELC_GPTm event input.

USGTRGCF位（GTETRGC引脚下降输入源计数器向上计数使能）

USGTRGCF位在GTETRGC引脚输入的下降沿启用或禁用GTCNT计数器向上计数。

USGTRGDR位（GTETRGD引脚上升沿输入源计数器向上计数使能）

USGTRGDR位在GTETRGD引脚输入的上升沿启用或禁用GTCNT计数器向上计数。

USGTRGDF位（GTETRGD引脚下降输入源计数器向上计数使能）

USGTRGDF位在GTETRGD引脚输入的下降沿启用或禁用GTCNT计数器向上计数。

USCARBL位（GTIOCB值低源计数器向上计数启用期间的GTIOCA引脚上升沿输入）

USCARBL位在GTIOCA引脚输入的上升沿启用或禁用GTCNT计数器向上计数，当GTIOCB输入为0。

USCARBH位（GTIOCB值高电平源计数器向上计数启用期间的GTIOCA引脚上升沿输入）

USCARBH位在GTIOCA引脚输入的上升沿启用或禁用GTCNT计数器向上计数，当GTIOCB输入为1。

USCAFBL位（GTIOCB值低源计数器向上计数启用期间的GTIOCA引脚下降输入）

USCAFBL位在GTIOCA引脚输入的下降沿启用或禁用GTCNT计数器向上计数，当GTIOCB输入为0。

USCAFBH位（GTIOCB值高源计数器向上计数启用期间的GTIOCA引脚下降输入）

USCAFBH位在GTIOCA引脚输入的下降沿启用或禁用GTCNT计数器向上计数，当GTIOCB输入为1。

USCBRAL位（GTIOCA值低源计数器向上计数启用期间的GTIOCB引脚上升输入）

USCBRAL位在GTIOCB引脚输入的上升沿启用或禁用GTCNT计数器向上计数，当GTIOCA输入为0。

USCBRAH位（GTIOCA值高源计数器向上计数启用期间的GTIOCB引脚上升沿输入）

USCBRAH位在GTIOCB引脚输入的上升沿启用或禁用GTCNT计数器向上计数，当GTIOCA输入为1。

USCBFAL位（GTIOCA值低源计数器向上计数启用期间的GTIOCB引脚下降输入）

USCBFAL位在GTIOCB引脚输入的下降沿启用或禁用GTCNT计数器向上计数，当GTIOCA输入为0。

USCBFAH位（GTIOCA值高源计数器向上计数启用期间GTIOCB引脚下降输入）

USCBFAH位在GTIOCB引脚输入的下降沿启用或禁用GTCNT计数器向上计数，当GTIOCA输入为1。

USELCm位（ELC_GPTm事件源计数器向上计数启用）（m=A到H）

USELCm位启用或禁用ELC_GPTm事件输入上的GTCNT计数器向上计数。

23.2.9 General PWM Timer Down Count Source Select Register (GTDNSR)

Address(es): GPT32EHm.GTDNSR 4007 8020h + 0100h × m (m = 0 to 3)
GPT32Em.GTDNSR 4007 8020h + 0100h × m (m = 4 to 7)
GPT32m.GTDNSR 4007 8020h + 0100h × m (m = 8 to 13)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	DSELCH	DSELCG	DSELCF	DSELCE	DSELCD	DSELCC	DSELCB	DSELCA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	DSCBFAH	DSCBFAL	DSCBRAH	DSCBRAL	DSCAFBH	DSCAFBL	DSCARBH	DSCARBL	DSGTRGDF	DSGTRGDR	DSGTRGCF	DSGTRGCR	DSGTRGBF	DSGTRGBR	DSGTRGAF	DSGTRGAR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	DSGTRGAR	GTETRGA Pin Rising Input Source Counter Count Down Enable	0: Disable counter count down on the rising edge of GTETRGA input 1: Enable counter count down on the rising edge of GTETRGA input.	R/W
b1	DSGTRGAF	GTETRGA Pin Falling Input Source Counter Count Down Enable	0: Disable counter count down on the falling edge of GTETRGA input 1: Enable counter count down on the falling edge of GTETRGA input.	R/W
b2	DSGTRGBR	GTETRGB Pin Rising Input Source Counter Count Down Enable	0: Disable counter count down on the rising edge of GTETRGB input 1: Enable counter count down on the rising edge of GTETRGB input.	R/W
b3	DSGTRGBF	GTETRGB Pin Falling Input Source Counter Count Down Enable	0: Disable counter count down on the falling edge of GTETRGB input 1: Enable counter count down on the falling edge of GTETRGB input.	R/W
b4	DSGTRGCR	GTETRGC Pin Rising Input Source Counter Count Down Enable	0: Disable counter count down on the rising edge of GTETRGC input 1: Enable counter count down on the rising edge of GTETRGC input.	R/W
b5	DSGTRGCF	GTETRGC Pin Falling Input Source Counter Count Down Enable	0: Disable counter count down on the falling edge of GTETRGC input 1: Enable counter count down on the falling edge of GTETRGC input.	R/W
b6	DSGTRGDR	GTETRGD Pin Rising Input Source Counter Count Down Enable	0: Disable counter count down on the rising edge of GTETRGD input 1: Enable counter count down on the rising edge of GTETRGD input.	R/W
b7	DSGTRGDF	GTETRGD Pin Falling Input Source Counter Count Down Enable	0: Disable counter count down on the falling edge of GTETRGD input 1: Enable counter count down on the falling edge of GTETRGD input.	R/W
b8	DSCARBL	GTIOCA Pin Rising Input during GTIOCB Value Low Source Counter Count Down Enable	0: Disable counter count down on the rising edge of GTIOCA input when GTIOCB input is 0 1: Enable counter count down on the rising edge of GTIOCA input when GTIOCB input is 0.	R/W
b9	DSCARBH	GTIOCA Pin Rising Input during GTIOCB Value High Source Counter Count Down Enable	0: Disable counter count down on the rising edge of GTIOCA input when GTIOCB input is 1 1: Enable counter count down on the rising edge of GTIOCA input when GTIOCB input is 1.	R/W
b10	DSCAFBL	GTIOCA Pin Falling Input during GTIOCB Value Low Source Counter Count Down Enable	0: Disable counter count down on the falling edge of GTIOCA input when GTIOCB input is 0 1: Enable counter count down on the falling edge of GTIOCA input when GTIOCB input is 0.	R/W

23.2.9 通用PWM定时器递减计数源选择寄存器(GTDNSR)

Address(es): GPT32EHm.GTDNSR 4007 8020h + 0100h × m (m = 0 to 3)
GPT32Em.GTDNSR 4007 8020h + 0100h × m (m = 4 to 7)
GPT32m.GTDNSR 4007 8020h + 0100h × m (m = 8 to 13)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	DSELCH	DSELCG	DSELCF	DSELCE	DSELCD	DSELCC	DSELCB	DSELCA
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	DSCBFAH	DSCBFAL	DSCBRAH	DSCBRAL	DSCAFBH	DSCAFBL	DSCARBH	DSCARBL	DSGTRGDF	DSGTRGDR	DSGTRGCF	DSGTRGCR	DSGTRGBF	DSGTRGBR	DSGTRGAF	DSGTRGAR
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	DSGTRGAR	GTETRGA引脚上升输入源计数器倒计时启用	0：在GTETRGA输入的上升沿禁用计数器减计数1：在GTETRGA输入的上升沿启用计数器减计数。	R/W
b1	DSGTRGAF	GTETRGA引脚下降输入源计数器倒计时启用	0：在GTETRGA输入的下降沿禁用计数器减计数1：在GTETRGA输入的下降沿启用计数器减计数。	R/W
b2	DSGTRGBR	GTETRGB引脚上升输入源计数器倒计时启用	0：在GTETRGB输入的上升沿禁用计数器减计数1：在GTETRGB输入的上升沿启用计数器减计数。	R/W
b3	DSGTRGBF	GTETRGB引脚下降输入源计数器倒计时启用	0：在GTETRGB输入的下降沿禁用计数器减计数1：在GTETRGB输入的下降沿启用计数器减计数。	R/W
b4	DSGTRGCR	GTETRGC引脚上升沿输入源计数器倒计时启用	0：在GTETRGC输入的上升沿禁止计数器向下计数1：在GTETRGC输入的上升沿使能计数器向下计数。	R/W
b5	DSGTRGCF	GTETRGC引脚下降输入源计数器倒计时启用	0：在GTETRGC输入的下降沿禁用计数器减计数1：在GTETRGC输入的下降沿启用计数器减计数。	R/W
b6	DSGTRGDR	GTETRGD引脚上升输入源计数器倒计时启用	0：在GTETRGD输入的上升沿禁止计数器向下计数1：在GTETRGD输入的上升沿使能计数器向下计数。	R/W
b7	DSGTRGDF	GTETRGD引脚下降输入源计数器倒计时启用	0：在GTETRGD输入的下降沿禁用计数器减计数1：在GTETRGD输入的下降沿启用计数器减计数。	R/W
b8	DSCARBL	GTIOCA引脚上升期间输入GTIOCB值低源计数器倒计时启用	0：当GTIOCB输入为0时，在GTIOCA输入上升沿禁止计数器减计数1：当GTIOCB输入为0时，在GTIOCA输入上升沿使能计数器减计数。	R/W
b9	DSCARBH	GTIOCA引脚上升期间输入GTIOCB值高源计数器倒计时启用	0：当GTIOCB输入为1时，在GTIOCA输入上升沿禁止计数器减计数1：当GTIOCB输入为1时，在GTIOCA输入上升沿使能计数器减计数。	R/W
b10	DSCAFBL	GTIOCA引脚下降期间输入GTIOCB值低源计数器倒计时启用	0：当GTIOCB输入为0时，在GTIOCA输入下降沿禁止计数器减计数1：当GTIOCB输入为0时，在GTIOCA输入下降沿使能计数器减计数。	R/W

Bit	Symbol	Bit name	Description	R/W
b11	DSCAFBH	GTIOCA Pin Falling Input during GTIOCB Value High Source Counter Count Down Enable	0: Disable counter count down on the falling edge of GTIOCA input when GTIOCB input is 1 1: Enable counter count down on the falling edge of GTIOCA input when GTIOCB input is 1.	R/W
b12	DSCBRAL	GTIOCB Pin Rising Input during GTIOCA Value Low Source Counter Count Down Enable	0: Disable counter count down on the rising edge of GTIOCB input when GTIOCA input is 0 1: Enable counter count down on the rising edge of GTIOCB input when GTIOCA input is 0.	R/W
b13	DSCBRAH	GTIOCB Pin Rising Input during GTIOCA Value High Source Counter Count Down Enable	0: Disable counter count down on the rising edge of GTIOCB input when GTIOCA input is 1 1: Enable counter count down on the rising edge of GTIOCB input when GTIOCA input is 1.	R/W
b14	DSCBFAL	GTIOCB Pin Falling Input during GTIOCA Value Low Source Counter Count Down Enable	0: Disable counter count down on the falling edge of GTIOCB input when GTIOCA input is 0 1: Enable counter count down on the falling edge of GTIOCB input when GTIOCA input is 0.	R/W
b15	DSCBFAH	GTIOCB Pin Falling Input during GTIOCA Value High Source Counter Count Down Enable	0: Disable counter count down on the falling edge of GTIOCB input when GTIOCA input is 1 1: Enable counter count down on the falling edge of GTIOCB input when GTIOCA input is 1.	R/W
b16	DSELCA	ELC_GPTA Event Source Counter Count Down Enable	0: Disable counter count down on ELC_GPTA event input 1: Enable counter count down on ELC_GPTA event input.	R/W
b17	DSELCB	ELC_GPTB Event Source Counter Count Down Enable	0: Disable counter count down on ELC_GPTB event input 1: Enable counter count down on ELC_GPTB event input.	R/W
b18	DSELCC	ELC_GPTC Event Source Counter Count Down Enable	0: Disable counter count down on ELC_GPTC event input 1: Enable counter count down on ELC_GPTC event input.	R/W
b19	DSELCD	ELC_GPTD Event Source Counter Count Down Enable	0: Disable counter count down on ELC_GPTD event input 1: Enable counter count down on ELC_GPTD event input.	R/W
b20	DSELCE	ELC_GPTE Event Source Counter Count Down Enable	0: Disable counter count down on ELC_GPTE event input 1: Enable counter count down on ELC_GPTE event input.	R/W
b21	DSELCF	ELC_GPTF Event Source Counter Count Down Enable	0: Disable counter count down on ELC_GPTF event input 1: Enable counter count down on ELC_GPTF event input.	R/W
b22	DSELCG	ELC_GPTG Event Source Counter Count Down Enable	0: Disable counter count down on ELC_GPTG event input 1: Enable counter count down on ELC_GPTG event input.	R/W
b23	DSELCH	ELC_GPTH Event Source Counter Count Down Enable	0: Disable counter count down on ELC_GPTH event input 1: Enable counter count down on ELC_GPTH event input.	R/W
b31 to b24	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The GTDNSR register sets the source to count down the GTCNT counter.

When at least one bit in the GTDNSR register is set to 1, the GTCNT counter is counted up by the source that is set to 1 in this register. In this case, GTCR.TPCS has no effect.

DSGTRGAR bit (GTETRGA Pin Rising Input Source Counter Count Down Enable)

The DSGTRGAR bit enables or disables GTCNT counter count down on the rising edge of the GTETRGA pin input.

DSGTRGAF bit (GTETRGA Pin Falling Input Source Counter Count Down Enable)

The DSGTRGAF bit enables or disables GTCNT counter count down on the falling edge of the GTETRGA pin input.

DSGTRGBR bit (GTETRGB Pin Rising Input Source Counter Count Down Enable)

The DSGTRGBR bit enables or disables GTCNT counter count down on the rising edge of the GTETRGB pin input.

DSGTRGBF bit (GTETRGB Pin Falling Input Source Counter Count Down Enable)

The DSGTRGBF bit enables or disables GTCNT counter count down on the falling edge of the GTETRGB pin input.

DSGTRGCR bit (GTETRGC Pin Rising Input Source Counter Count Down Enable)

The DSGTRGCR bit enables or disables GTCNT counter count down on the rising edge of the GTETRGC pin input.

Bit	Symbol	位名称	Description	R/W
b11	DSCAFBH	GTIOCA引脚下降期间输入GTIOCB值高源计数器倒计时启用	0：当GTIOCB输入为1时，在GTIOCA输入下降沿禁止计数器减计数1：当GTIOCB输入为1时，在GTIOCA输入下降沿使能计数器减计数。	R/W
b12	DSCBRAL	GTIOCB引脚上升期间输入GTIOCA值低源计数器倒计时启用	0：当GTIOCA输入为0时，在GTIOCB输入上升沿禁止计数器减计数1：当GTIOCA输入为0时，在GTIOCB输入上升沿使能计数器减计数。	R/W
b13	DSCBRAH	GTIOCB引脚上升期间输入GTIOCA值高源计数器倒计时启用	0：当GTIOCA输入为1时，在GTIOCB输入上升沿禁止计数器减计数1：当GTIOCA输入为1时，在GTIOCB输入上升沿使能计数器减计数。	R/W
b14	DSCBFAL	在GTIOCB引脚下降输入GTIOCA值低源计数器倒计时启用	0：当GTIOCA输入为0时，在GTIOCB输入的下降沿禁止计数器减计数1：当GTIOCA输入为0时，在GTIOCB输入的下降沿使能计数器减计数。	R/W
b15	DSCBFAH	在GTIOCB引脚下降输入GTIOCA值高源计数器倒计时启用	0：当GTIOCA输入为1时，在GTIOCB输入的下降沿禁止计数器向下计数1：当GTIOCA输入为1时，在GTIOCB输入的下降沿使能计数器向下计数。	R/W
b16	DSELCA	ELC_GPTA事件源计数器倒计时启用	0：在ELC_GPTA事件输入上禁用计数器递减计数1：在ELC_GPTA事件输入上启用计数器递减计数。	R/W
b17	DSELCB	ELC_GPTB事件源计数器倒计时启用	0：在ELC_GPTB事件输入上禁用计数器递减计数1：在ELC_GPTB事件输入上启用计数器递减计数。	R/W
b18	DSELCC	ELC_GPTC事件源计数器倒计时启用	0：在ELC_GPTC事件输入上禁用计数器递减计数1：在ELC_GPTC事件输入上启用计数器递减计数。	R/W
b19	DSELCD	ELC_GPTD事件源计数器倒计时启用	0：在ELC_GPTD事件输入上禁用计数器递减计数1：在ELC_GPTD事件输入上启用计数器递减计数。	R/W
b20	DSELCE	ELC_GPTE事件源计数器倒计时启用	0：在ELC_GPTE事件输入上禁用计数器递减计数1：在ELC_GPTE事件输入上启用计数器递减计数。	R/W
b21	DSELCF	ELC_GPTF事件源计数器倒计时启用	0：在ELC_GPTF事件输入上禁用计数器递减计数1：在ELC_GPTF事件输入上启用计数器递减计数。	R/W
b22	DSELCG	ELC_GPTG事件源计数器倒计时启用	0：在ELC_GPTG事件输入上禁用计数器递减计数1：在ELC_GPTG事件输入上启用计数器递减计数。	R/W
b23	DSELCH	ELC_GPTH事件源计数器倒计时启用	0：在ELC_GPTH事件输入上禁用计数器递减计数1：在ELC_GPTH事件输入上启用计数器递减计数。	R/W
b31 to b24	—	Reserved	这些位被读取为0。写入值应为0。	R/W

GTDNSR寄存器设置源以对GTCNT计数器进行递减计数。

当GTDNSR寄存器中的至少一位设置为1时，GTCNT计数器由该寄存器中设置为1的源进行计数。在这种情况下，GTCR.TPCS无效。

DSGTRGAR位（GTETRGA引脚上升沿输入源计数器倒计时使能）

DSGTRGAR位在GTETRGA引脚输入的上升沿启用或禁用GTCNT计数器倒计时。

DSGTRGAF位（GTETRGA引脚下降输入源计数器倒计时使能）

DSGTRGAF位在GTETRGA引脚输入的下降沿启用或禁用GTCNT计数器倒计时。

DSGTRGBR位（GTETRGB引脚上升输入源计数器倒计时使能）

DSGTRGBR位在GTETRGB引脚输入的上升沿启用或禁用GTCNT计数器倒计时。

DSGTRGBF位（GTETRGB引脚下降输入源计数器倒计时使能）

DSGTRGBF位在GTETRGB引脚输入的下降沿启用或禁用GTCNT计数器倒计时。

DSGTRGCR位（GTETRGC引脚上升输入源计数器倒计时使能）

DSGTRGCR位在GTETRGC引脚输入的上升沿启用或禁用GTCNT计数器倒计时。

DSGTRGCF bit (GTETRGC Pin Falling Input Source Counter Count Down Enable)

The DSGTRGCF bit enables or disables GTCNT counter count down on the falling edge of the GTETRGC pin input.

DSGTRGDR bit (GTETRGD Pin Rising Input Source Counter Count Down Enable)

The DSGTRGDR bit enables or disables GTCNT counter count down on the rising edge of the GTETRGD pin input.

DSGTRGDF bit (GTETRGD Pin Falling Input Source Counter Count Down Enable)

The DSGTRGDF bit enables or disables GTCNT counter count down on the falling edge of the GTETRGD pin input.

DSCARBL bit (GTIOCA Pin Rising Input during GTIOCB Value Low Source Counter Count Down Enable)

The DSCARBL bit enables or disables GTCNT counter count down on the rising edge of the GTIOCA pin input when the GTIOCB input is 0.

DSCARBH bit (GTIOCA Pin Rising Input during GTIOCB Value High Source Counter Count Down Enable)

The DSCARBH bit enables or disables GTCNT counter count down on the rising edge of the GTIOCA pin input when the GTIOCB input is 1.

DSCAFBL bit (GTIOCA Pin Falling Input during GTIOCB Value Low Source Counter Count Down Enable)

The DSCAFBL bit enables or disables GTCNT counter count down on the falling edge of the GTIOCA pin input when the GTIOCB input is 0.

DSCAFBH bit (GTIOCA Pin Falling Input during GTIOCB Value High Source Counter Count Down Enable)

The DSCAFBH bit enables or disables GTCNT counter count down on the falling edge of the GTIOCA pin input when the GTIOCB input is 1.

DSCBRAL bit (GTIOCB Pin Rising Input during GTIOCA Value Low Source Counter Count Down Enable)

The DSCBRAL bit enables or disables GTCNT counter count down on the rising edge of the GTIOCB pin input when the GTIOCA input is 0.

DSCBRAH bit (GTIOCB Pin Rising Input during GTIOCA Value High Source Counter Count Down Enable)

The DSCBRAH bit enables or disables GTCNT counter count down on the rising edge of the GTIOCB pin input when the GTIOCA input is 1.

DSCBFAL bit (GTIOCB Pin Falling Input during GTIOCA Value Low Source Counter Count Down Enable)

The DSCBFAL bit enables or disables GTCNT counter count down on the falling edge of the GTIOCB pin input when the GTIOCA input is 0.

DSCBFAH bit (GTIOCB Pin Falling Input during GTIOCA Value High Source Counter Count Down Enable)

The DSCBFAH bit enables or disables GTCNT counter count down on the falling edge of the GTIOCB pin input when the GTIOCA input is 1.

DSELCm bit (ELC_GPTm Event Source Counter Count Down Enable) (m = A to H)

The DSELCm bit enables or disables GTCNT counter count down on the ELC_GPTm event input.

DSGTRGCF位（GTETRGC引脚下降输入源计数器倒计时使能）

DSGTRGCF位在GTETRGC引脚输入的下降沿启用或禁用GTCNT计数器倒计时。

DSGTRGDR位（GTETRGD引脚上升输入源计数器倒计时使能）

DSGTRGDR位在GTETRGD引脚输入的上升沿启用或禁用GTCNT计数器倒计时。

DSGTRGDF位（GTETRGD引脚下降输入源计数器倒计时使能）

DSGTRGDF位在GTETRGD引脚输入的下降沿启用或禁用GTCNT计数器倒计时。

DSCARBL位（GTIOCB值低源计数器倒计时期间GTIOCA引脚上升沿输入Enable）

当GTIOCB输入为0时，DSCARBL位在GTIOCA引脚输入的上升沿启用或禁用GTCNT计数器倒计时。

DSCARBH位（GTIOCB值高电平期间的GTIOCA引脚上升沿输入源计数器向下计数Enable）

当GTIOCB输入为1时，DSCARBH位在GTIOCA引脚输入的上升沿启用或禁用GTCNT计数器递减计数。

DSCAFBL位（GTIOCB值低源计数器向下计数期间GTIOCA引脚下降输入Enable）

当GTIOCB输入为0时，DSCAFBL位在GTIOCA引脚输入的下降沿启用或禁用GTCNT计数器倒计时。

DSCAFBH位（GTIOCB值高源计数器倒计时期间GTIOCA引脚下降输入Enable）

当GTIOCB输入为1时，DSCAFBH位在GTIOCA引脚输入的下降沿启用或禁用GTCNT计数器倒计时。

DSCBRAL位（GTIOCA值低源计数器向下计数期间GTIOCB引脚上升沿输入Enable）

当GTIOCA输入为0时，DSCBRAL位在GTIOCB引脚输入的上升沿启用或禁用GTCNT计数器递减计数。

DSCBRAH位（GTIOCA值高源计数器倒计时期间GTIOCB引脚上升沿输入Enable）

当GTIOCA输入为1时，DSCBRAH位在GTIOCB引脚输入的上升沿启用或禁用GTCNT计数器倒计时。

DSCBFAL位（GTIOCA值低源计数器倒计时期间GTIOCB引脚下降输入Enable）

当GTIOCA输入为0时，DSCBFAL位在GTIOCB引脚输入的下降沿启用或禁用GTCNT计数器倒计时。

DSCBFAH位（GTIOCA值高源计数器倒计时期间GTIOCB引脚下降输入Enable）

当GTIOCA输入为1时，DSCBFAH位在GTIOCB引脚输入的下降沿启用或禁用GTCNT计数器倒计时。

DSELCm位（ELC_GPTm事件源计数器倒计时启用）（m=A到H）

DSELCm位启用或禁用ELC_GPTm事件输入上的GTCNT计数器倒计时。

23.2.10 General PWM Timer Input Capture Source Select Register A (GTICASR)

Address(es): GPT32EHm.GTICASR 4007 8024h + 0100h × m (m = 0 to 3)
GPT32Em.GTICASR 4007 8024h + 0100h × m (m = 4 to 7)
GPT32m.GTICASR 4007 8024h + 0100h × m (m = 8 to 13)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	ASELCH	ASELCG	ASELCF	ASELCE	ASELCD	ASELCC	ASELCB	ASELCA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ASCBFAH	ASCBFAL	ASCBRAH	ASCBRAL	ASCAFBH	ASCAFBL	ASCARBH	ASCARBL	ASGTRGDF	ASGTRGDR	ASGTRGCF	ASGTRGCR	ASGTRGBF	ASGTRGBR	ASGTRGAF	ASGTRGAR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	ASGTRGAR	GTETRGA Pin Rising Input Source GTCCRA Input Capture Enable	0: Disable GTCCRA input capture on the rising edge of GTETRGA input 1: Enable GTCCRA input capture on the rising edge of GTETRGA input.	R/W
b1	ASGTRGAF	GTETRGA Pin Falling Input Source GTCCRA Input Capture Enable	0: Disable GTCCRA input capture on the falling edge of GTETRGA input 1: Enable GTCCRA input capture on the falling edge of GTETRGA input.	R/W
b2	ASGTRGBR	GTETRGB Pin Rising Input Source GTCCRA Input Capture Enable	0: Disable GTCCRA input capture on the rising edge of GTETRGB input 1: Enable GTCCRA input capture on the rising edge of GTETRGB input.	R/W
b3	ASGTRGBF	GTETRGB Pin Falling Input Source GTCCRA Input Capture Enable	0: Disable GTCCRA input capture on the falling edge of GTETRGB input 1: Enable GTCCRA input capture on the falling edge of GTETRGB input.	R/W
b4	ASGTRGCR	GTETRGC Pin Rising Input Source GTCCRA Input Capture Enable	0: Disable GTCCRA input capture on the rising edge of GTETRGC input 1: Enable GTCCRA input capture on the rising edge of GTETRGC input.	R/W
b5	ASGTRGCF	GTETRGC Pin Falling Input Source GTCCRA Input Capture Enable	0: Disable GTCCRA input capture on the falling edge of GTETRGC input 1: Enable GTCCRA input capture on the falling edge of GTETRGC input.	R/W
b6	ASGTRGDR	GTETRGD Pin Rising Input Source GTCCRA Input Capture Enable	0: Disable GTCCRA input capture on the rising edge of GTETRGD input 1: Enable GTCCRA input capture on the rising edge of GTETRGD input.	R/W
b7	ASGTRGDF	GTETRGD Pin Falling Input Source GTCCRA Input Capture Enable	0: Disable GTCCRA input capture on the falling edge of GTETRGD input 1: Enable GTCCRA input capture on the falling edge of GTETRGD input.	R/W
b8	ASCARBL	GTIOCA Pin Rising Input during GTIOCB Value Low Source GTCCRA Input Capture Enable	0: Disable GTCCRA input capture on the rising edge of GTIOCA input when GTIOCB input is 0 1: Enable GTCCRA input capture on the rising edge of GTIOCA input when GTIOCB input is 0.	R/W
b9	ASCARBH	GTIOCA Pin Rising Input during GTIOCB Value High Source GTCCRA Input Capture Enable	0: Disable GTCCRA input capture on the rising edge of GTIOCA input when GTIOCB input is 1 1: Enable GTCCRA input capture on the rising edge of GTIOCA input when GTIOCB input is 1.	R/W
b10	ASCAFBL	GTIOCA Pin Falling Input during GTIOCB Value Low Source GTCCRA Input Capture Enable	0: Disable GTCCRA input capture on the falling edge of GTIOCA input when GTIOCB input is 0 1: Enable GTCCRA input capture on the falling edge of GTIOCA input when GTIOCB input is 0.	R/W

23.2.10 通用PWM定时器输入捕捉源选择寄存器A(GTICASR)

Address(es): GPT32EHm.GTICASR 4007 8024h + 0100h × m (m = 0 to 3)
GPT32Em.GTICASR 4007 8024h + 0100h × m (m = 4 to 7)
GPT32m.GTICASR 4007 8024h + 0100h × m (m = 8 to 13)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	ASELCH	ASELCG	ASELCF	ASELCE	ASELCD	ASELCC	ASELCB	ASELCA
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ASCBFAH	ASCBFAL	ASCBRAH	ASCBRAL	ASCAFBH	ASCAFBL	ASCARBH	ASCARBL	ASGTRGDF	ASGTRGDR	ASGTRGCF	ASGTRGCR	ASGTRGBF	ASGTRGBR	ASGTRGAF	ASGTRGAR
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	ASGTRGAR	GTETRGA引脚上升输入源 GTCCRA输入捕捉使能	0：在GTETRGA输入的上升沿禁用GTCCRA输入捕捉1：在GTETRGA输入的上升沿启用GTCCRA输入捕捉。	R/W
b1	ASGTRGAF	GTETRGA引脚下降输入源 GTCCRA输入捕捉使能	0：在GTETRGA输入的下降沿禁用GTCCRA输入捕捉1：在GTETRGA输入的下降沿启用GTCCRA输入捕捉。	R/W
b2	ASGTRGBR	GTETRGB引脚上升输入源 GTCCRA输入捕捉使能	0：在GTETRGB输入的上升沿禁用GTCCRA输入捕捉1：在GTETRGB输入的上升沿启用GTCCRA输入捕捉。	R/W
b3	ASGTRGBF	GTETRGB引脚下降输入源 GTCCRA输入捕捉使能	0：在GTETRGB输入的下降沿禁用GTCCRA输入捕捉1：在GTETRGB输入的下降沿启用GTCCRA输入捕捉。	R/W
b4	ASGTRGCR	GTETRGC引脚上升沿输入源 GTCCRA输入捕捉使能	0：在GTETRGC输入的上升沿禁用GTCCRA输入捕捉1：在GTETRGC输入的上升沿启用GTCCRA输入捕捉。	R/W
b5	ASGTRGCF	GTETRGC引脚下降输入源 GTCCRA输入捕捉使能	0：在GTETRGC输入的下降沿禁用GTCCRA输入捕捉1：在GTETRGC输入的下降沿启用GTCCRA输入捕捉。	R/W
b6	ASGTRGDR	GTETRGD引脚上升输入源 GTCCRA输入捕捉使能	0：在GTETRGD输入的上升沿禁用GTCCRA输入捕捉1：在GTETRGD输入的上升沿启用GTCCRA输入捕捉。	R/W
b7	ASGTRGDF	GTETRGD引脚下降输入源 GTCCRA输入捕捉使能	0：在GTETRGD输入的下降沿禁用GTCCRA输入捕捉1：在GTETRGD输入的下降沿启用GTCCRA输入捕捉。	R/W
b8	ASCARBL	GTIOCB值低源期间的GTIOCA引脚上升输入 GTCCRA输入捕捉使能	0：当GTIOCB输入为0时，在GTIOCA输入上升沿禁用GTCCRA输入捕捉1：当GTIOCB输入为0时，在GTIOCA输入上升沿启用GTCCRA输入捕捉。	R/W
b9	ASCARBH	GTIOCB值高源期间的GTIOCA引脚上升输入 GTCCRA输入捕捉使能	0：当GTIOCB输入为1时，在GTIOCA输入上升沿禁用GTCCRA输入捕捉1：当GTIOCB输入为1时，在GTIOCA输入上升沿启用GTCCRA输入捕捉。	R/W
b10	ASCAFBL	GTIOCA引脚下降期间输入 GTIOCB价值低来源 GTCCRA输入捕捉使能	0：当GTIOCB输入为0时，在GTIOCA输入下降沿禁用GTCCRA输入捕捉1：当GTIOCB输入为0时，在GTIOCA输入下降沿启用GTCCRA输入捕捉。	R/W

Bit	Symbol	Bit name	Description	R/W
b11	ASCAFBH	GTIOCA Pin Falling Input during GTIOCB Value High Source GTCCRA Input Capture Enable	0: Disable GTCCRA input capture on the falling edge of GTIOCA input when GTIOCB input is 1 1: Enable GTCCRA input capture on the falling edge of GTIOCA input when GTIOCB input is 1.	R/W
b12	ASCBRAL	GTIOCB Pin Rising Input during GTIOCA Value Low Source GTCCRA Input Capture Enable	0: Disable GTCCRA input capture on the rising edge of GTIOCB input when GTIOCA input is 0 1: Enable GTCCRA input capture on the rising edge of GTIOCB input when GTIOCA input is 0.	R/W
b13	ASCBRAH	GTIOCB Pin Rising Input during GTIOCA Value High Source GTCCRA Input Capture Enable	0: Disable GTCCRA input capture on the rising edge of GTIOCB input when GTIOCA input is 1 1: Enable GTCCRA input capture on the rising edge of GTIOCB input when GTIOCA input is 1.	R/W
b14	ASCBFAL	GTIOCB Pin Falling Input during GTIOCA Value Low Source GTCCRA Input Capture Enable	0: Disable GTCCRA input capture on the falling edge of GTIOCB input when GTIOCA input is 0 1: Enable GTCCRA input capture on the falling edge of GTIOCB input when GTIOCA input is 0.	R/W
b15	ASCBFAH	GTIOCB Pin Falling Input during GTIOCA Value High Source GTCCRA Input Capture Enable	0: Disable GTCCRA input capture on the falling edge of GTIOCB input when GTIOCA input is 1 1: Enable GTCCRA input capture on the falling edge of GTIOCB input when GTIOCA input is 1.	R/W
b16	ASELCA	ELC_GPTA Event Source GTCCRA Input Capture Enable	0: Disable GTCCRA input capture on ELC_GPTA event input 1: Enable GTCCRA input capture on ELC_GPTA event input.	R/W
b17	ASELCB	ELC_GPTB Event Source GTCCRA Input Capture Enable	0: Disable GTCCRA input capture on ELC_GPTB event input 1: Enable GTCCRA input capture on ELC_GPTB event input.	R/W
b18	ASELCC	ELC_GPTC Event Source GTCCRA Input Capture Enable	0: Disable GTCCRA input capture on ELC_GPTC event input 1: Enable GTCCRA input capture on ELC_GPTC event input.	R/W
b19	ASELCD	ELC_GPTD Event Source GTCCRA Input Capture Enable	0: Disable GTCCRA input capture on ELC_GPTD event input 1: Enable GTCCRA input capture on ELC_GPTD event input.	R/W
b20	ASELCE	ELC_GPTE Event Source GTCCRA Input Capture Enable	0: Disable GTCCRA input capture on ELC_GPTE event input 1: Enable GTCCRA input capture on ELC_GPTE event input.	R/W
b21	ASELCF	ELC_GPTF Event Source GTCCRA Input Capture Enable	0: Disable GTCCRA input capture on ELC_GPTF event input 1: Enable GTCCRA input capture on ELC_GPTF event input.	R/W
b22	ASELCG	ELC_GPTG Event Source GTCCRA Input Capture Enable	0: Disable GTCCRA input capture on ELC_GPTG event input 1: Enable GTCCRA input capture on ELC_GPTG event input.	R/W
b23	ASELCH	ELC_GPTH Event Source GTCCRA Input Capture Enable	0: Disable GTCCRA input capture on ELC_GPTH event input 1: Enable GTCCRA input capture on ELC_GPTH event input.	R/W
b31 to b24	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The GTICASR register sets the source of input capture for GTCCRA.

ASGTRGAR bit (GTETRGA Pin Rising Input Source GTCCRA Input Capture Enable)

The ASGTRGAR bit enables or disables input capture for GTCCRA on the rising edge of the GTETRGA pin input.

Bit	Symbol	位名称	Description	R/W
b11	ASCAFBH	GTIOCA引脚下降期间输入GTIOCB价值高来源GTCCRA输入捕捉使能	0：当GTIOCB输入为1时，在GTIOCA输入的下降沿禁用GTCCRA输入捕捉1：当GTIOCB输入为1时，在GTIOCA输入的下降沿启用GTCCRA输入捕捉。	R/W
b12	ASCBRAL	GTIOCA值低源期间的GTIOCB引脚上升输入GTCCRA输入捕捉使能	0：当GTIOCA输入为0时，在GTIOCB输入上升沿禁止GTCCRA输入捕捉1：当GTIOCA输入为0时，在GTIOCB输入上升沿启用GTCCRA输入捕捉。	R/W
b13	ASCBRAH	GTIOCA值高源期间的GTIOCB引脚上升输入GTCCRA输入捕捉使能	0：当GTIOCA输入为1时，在GTIOCB输入上升沿禁用GTCCRA输入捕捉1：当GTIOCA输入为1时，在GTIOCB输入上升沿启用GTCCRA输入捕捉。	R/W
b14	ASCBFAL	在GTIOCB引脚下降输入GTIOCA价值低来源GTCCRA输入捕捉使能	0：当GTIOCA输入为0时，在GTIOCB输入的下降沿禁止GTCCRA输入捕捉1：在GTIOCA输入为0时，在GTIOCB输入的下降沿启用GTCCRA输入捕捉。	R/W
b15	ASCBFAH	在GTIOCB引脚下降输入GTIOCA价值高来源GTCCRA输入捕捉使能	0：当GTIOCA输入为1时，在GTIOCB输入下降沿禁用GTCCRA输入捕捉1：当GTIOCA输入为1时，在GTIOCB输入下降沿启用GTCCRA输入捕捉。	R/W
b16	ASELCA	ELC_GPTA事件源GTCCRA输入捕捉使能	0：在ELC_GPTA事件输入上禁用GTCCRA输入捕捉1：在ELC_GPTA事件输入上启用GTCCRA输入捕捉。	R/W
b17	ASELCB	ELC_GPTB事件源GTCCRA输入捕捉使能	0：在ELC_GPTB事件输入上禁用GTCCRA输入捕捉1：在ELC_GPTB事件输入上启用GTCCRA输入捕捉。	R/W
b18	ASELCC	ELC_GPTC事件源GTCCRA输入捕捉使能	0：在ELC_GPTC事件输入上禁用GTCCRA输入捕捉1：在ELC_GPTC事件输入上启用GTCCRA输入捕捉。	R/W
b19	ASELCD	ELC_GPTD事件源GTCCRA输入捕捉使能	0：在ELC_GPTD事件输入上禁用GTCCRA输入捕捉1：在ELC_GPTD事件输入上启用GTCCRA输入捕捉。	R/W
b20	ASELCE	ELC_GPTE事件源GTCCRA输入捕捉使能	0：在ELC_GPTE事件输入上禁用GTCCRA输入捕捉1：在ELC_GPTE事件输入上启用GTCCRA输入捕捉。	R/W
b21	ASELCF	ELC_GPTF事件源GTCCRA输入捕捉使能	0：在ELC_GPTF事件输入上禁用GTCCRA输入捕捉1：在ELC_GPTF事件输入上启用GTCCRA输入捕捉。	R/W
b22	ASELCG	ELC_GPTG事件源GTCCRA输入捕捉使能	0：在ELC_GPTG事件输入上禁用GTCCRA输入捕捉1：在ELC_GPTG事件输入上启用GTCCRA输入捕捉。	R/W
b23	ASELCH	ELC_GPTH事件源GTCCRA输入捕捉使能	0：在ELC_GPTH事件输入上禁用GTCCRA输入捕捉1：在ELC_GPTH事件输入上启用GTCCRA输入捕捉。	R/W
b31 to b24	—	Reserved	这些位被读取为0。写入值应为0。	R/W

GTICASR寄存器设置GTCCRA的输入捕捉源。

ASGTRGAR位（GTETRGA引脚上升沿输入源GTCCRA输入捕捉使能）

ASGTRGAR位在GTETRGA引脚输入的上升沿启用或禁用GTCCRA的输入捕捉。

ASGTRGAF bit (GTETRGA Pin Falling Input Source GTCCRA Input Capture Enable)

The ASGTRGAF bit enables or disables input capture for GTCCRA on the falling edge of the GTETRGA pin input.

ASGTRGBR bit (GTETRGB Pin Rising Input Source GTCCRA Input Capture Enable)

The ASGTRGBR bit enables or disables input capture for GTCCRA on the rising edge of the GTETRGB pin input.

ASGTRGBF bit (GTETRGB Pin Falling Input Source GTCCRA Input Capture Enable)

The ASGTRGBF bit enables or disables input capture for GTCCRA on the falling edge of the GTETRGB pin input.

ASGTRGCR bit (GTETRGC Pin Rising Input Source GTCCRA Input Capture Enable)

The ASGTRGCR bit enables or disables input capture for GTCCRA on the rising edge of the GTETRGC pin input.

ASGTRGCF bit (GTETRGC Pin Falling Input Source GTCCRA Input Capture Enable)

The ASGTRGCF bit enables or disables input capture for GTCCRA on the falling edge of the GTETRGC pin input.

ASGTRGDR bit (GTETRGD Pin Rising Input Source GTCCRA Input Capture Enable)

The ASGTRGDR bit enables or disables input capture for GTCCRA on the rising edge of the GTETRGD pin input.

ASGTRGDF bit (GTETRGD Pin Falling Input Source GTCCRA Input Capture Enable)

The ASGTRGDF bit enables or disables input capture for GTCCRA on the falling edge of the GTETRGD pin input.

ASCARBL bit (GTIOCA Pin Rising Input during GTIOCB Value Low Source GTCCRA Input Capture Enable)

The ASCARBL bit enables or disables input capture for GTCCRA on the rising edge of the GTIOCA pin input when the GTIOCB input is 0.

ASCARBH bit (GTIOCA Pin Rising Input during GTIOCB Value High Source GTCCRA Input Capture Enable)

The ASCARBH bit enables or disables input capture for GTCCRA on the rising edge of the GTIOCA pin input when the GTIOCB input is 1.

ASCAFBL bit (GTIOCA Pin Falling Input during GTIOCB Value Low Source GTCCRA Input Capture Enable)

The ASCAFBL bit enables or disables input capture for GTCCRA on the falling edge of the GTIOCA pin input when the GTIOCB input is 0.

ASCAFBH bit (GTIOCA Pin Falling Input during GTIOCB Value High Source GTCCRA Input Capture Enable)

The ASCAFBH bit enables or disables input capture for GTCCRA on the falling edge of the GTIOCA pin input when the GTIOCB input is 1.

ASCBRAL bit (GTIOCB Pin Rising Input during GTIOCA Value Low Source GTCCRA Input Capture Enable)

The ASCBRAL bit enables or disables input capture for GTCCRA on the rising edge of the GTIOCB pin input when the GTIOCA input is 0.

ASCBRAH bit (GTIOCB Pin Rising Input during GTIOCA Value High Source GTCCRA Input Capture Enable)

The ASCBRAH bit enables or disables input capture for GTCCRA on the rising edge of the GTIOCB pin input when the GTIOCA input is 1.

ASCBFAL bit (GTIOCB Pin Falling Input during GTIOCA Value Low Source GTCCRA Input Capture Enable)

The ASCBFAL bit enables or disables input capture for GTCCRA on the falling edge of the GTIOCB pin input when the GTIOCA input is 0.

ASGTRGAF位（GTETRGA引脚下降输入源GTCCRA输入捕捉使能）

ASGTRGAF位在GTETRGA引脚输入的下降沿启用或禁用GTCCRA的输入捕捉。

ASGTRGBR位（GTETRGB引脚上升沿输入源GTCCRA输入捕捉使能）

ASGTRGBR位在GTETRGB引脚输入的上升沿启用或禁用GTCCRA的输入捕捉。

ASGTRGBF位（GTETRGB引脚下降输入源GTCCRA输入捕捉使能）

ASGTRGBF位在GTETRGB引脚输入的下降沿启用或禁用GTCCRA的输入捕捉。

ASGTRGCR位（GTETRGC引脚上升沿输入源GTCCRA输入捕捉使能）

ASGTRGCR位在GTETRGC引脚输入的上升沿启用或禁用GTCCRA的输入捕捉。

ASGTRGCF位（GTETRGC引脚下降输入源GTCCRA输入捕捉使能）

ASGTRGCF位在GTETRGC引脚输入的下降沿启用或禁用GTCCRA的输入捕捉。

ASGTRGDR位（GTETRGD引脚上升沿输入源GTCCRA输入捕捉使能）

ASGTRGDR位在GTETRGD引脚输入的上升沿启用或禁用GTCCRA的输入捕捉。

ASGTRGDF位（GTETRGD引脚下降输入源GTCCRA输入捕捉使能）

ASGTRGDF位在GTETRGD引脚输入的下降沿启用或禁用GTCCRA的输入捕捉。

ASCARBL位（GTIOCB值低电平期间GTIOCA引脚上升沿输入源GTCCRA输入捕捉Enable）

ASCARBL位在GTIOCA引脚输入的上升沿启用或禁用GTCCRA的输入捕捉，当GTIOCB输入为0。

ASCARBH位（GTIOCB值高电平期间GTIOCA引脚的上升沿输入源GTCCRA输入捕捉Enable）

ASCARBH位在GTIOCA引脚输入的上升沿启用或禁用GTCCRA的输入捕捉，当GTIOCB输入为1。

ASCAFBL位（GTIOCB值低电平期间GTIOCA引脚下降输入源GTCCRA输入捕捉Enable）

ASCAFBL位在GTIOCA引脚输入的下降沿启用或禁用GTCCRA的输入捕捉，当GTIOCB输入为0。

ASCAFBH位（GTIOCB值高电平期间GTIOCA引脚下降输入源GTCCRA输入捕捉Enable）

当GTIOCB输入为1时，ASCAFBH位在GTIOCA引脚输入的下降沿启用或禁用GTCCRA的输入捕捉。

ASCBRAL位（GTIOCA值低电平期间GTIOCB引脚上升沿输入源GTCCRA输入捕捉Enable）

ASCBRAL位在GTIOCB引脚输入的上升沿启用或禁用GTCCRA的输入捕捉，当GTIOCA输入为0。

ASCBRAH位（GTIOCA值高电平期间GTIOCB引脚的上升沿输入源GTCCRA输入捕捉Enable）

ASCBRAH位在GTIOCB引脚输入的上升沿启用或禁用GTCCRA的输入捕捉，当GTIOCA输入为1。

ASCBFAL位（GTIOCA值低电平期间GTIOCB引脚下降输入源GTCCRA输入捕捉Enable）

ASCBFAL位在GTIOCB引脚输入的下降沿启用或禁用GTCCRA的输入捕捉，当GTIOCA输入为0。

ASCBFAH bit (GTIOCB Pin Falling Input during GTIOCA Value High Source GTCCRA Input Capture Enable)

The ASCBFAH bit enables or disables input capture for GTCCRA on the falling edge of the GTIOCB pin input when the GTIOCA input is 1.

ASELCm bit (ELC_GPTm Event Source Counter GTCCRA Input Capture Enable) (m = A to H)

The ASELCm bit enables or disables input capture for GTCCRA on the ELC_GPTm event input.

23.2.11 General PWM Timer Input Capture Source Select Register B (GTICBSR)

Address(es): GPT32EHm.GTICBSR 4007 8028h + 0100h × m (m = 0 to 3)
GPT32Em.GTICBSR 4007 8028h + 0100h × m (m = 4 to 7)
GPT32m.GTICBSR 4007 8028h + 0100h × m (m = 8 to 13)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	BSELCH	BSELCG	BSELCF	BSELCE	BSELCD	BSELCC	BSELCB	BSELCA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BSCBFAH	BSCBFAL	BSCBRAH	BSCBRAL	BSCAFBH	BSCAFBL	BSCARBH	BSCARBL	BSGTRGDF	BSGTRGDR	BSGTRGCF	BSGTRGCR	BSGTRGBF	BSGTRGBR	BSGTRGAF	BSGTRGAR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	BSGTRGAR	GTETRGA Pin Rising Input Source GTCCRB Input Capture Enable	0: Disable GTCCRB input capture on the rising edge of GTETRGA input 1: Enable GTCCRB input capture on the rising edge of GTETRGA input.	R/W
b1	BSGTRGAF	GTETRGA Pin Falling Input Source GTCCRB Input Capture Enable	0: Disable GTCCRB input capture on the falling edge of GTETRGA input 1: Enable GTCCRB input capture on the falling edge of GTETRGA input.	R/W
b2	BSGTRGBR	GTETRGB Pin Rising Input Source GTCCRB Input Capture Enable	0: Disable GTCCRB input capture on the rising edge of GTETRGB input 1: Enable GTCCRB input capture on the rising edge of GTETRGB input.	R/W
b3	BSGTRGBF	GTETRGB Pin Falling Input Source GTCCRB Input Capture Enable	0: Disable GTCCRB input capture on the falling edge of GTETRGB input 1: Enable GTCCRB input capture on the falling edge of GTETRGB input.	R/W
b4	BSGTRGCR	GTETRGC Pin Rising Input Source GTCCRB Input Capture Enable	0: Disable GTCCRB input capture on the rising edge of GTETRGC input 1: Enable GTCCRB input capture on the rising edge of GTETRGC input.	R/W
b5	BSGTRGCF	GTETRGC Pin Falling Input Source GTCCRB Input Capture Enable	0: Disable GTCCRB input capture on the falling edge of GTETRGC input 1: Enable GTCCRB input capture on the falling edge of GTETRGC input.	R/W
b6	BSGTRGDR	GTETRGD Pin Rising Input Source GTCCRB Input Capture Enable	0: Disable GTCCRB input capture on the rising edge of GTETRGD input 1: Enable GTCCRB input capture on the rising edge of GTETRGD input.	R/W
b7	BSGTRGDF	GTETRGD Pin Falling Input Source GTCCRB Input Capture Enable	0: Disable GTCCRB input capture on the falling edge of GTETRGD input 1: Enable GTCCRB input capture on the falling edge of GTETRGD input.	R/W

ASCBFAH位（GTIOCA值高电平期间GTIOCB引脚下降输入源GTCCRA输入捕捉Enable)

ASCBFAH位在GTIOCB引脚输入的下降沿启用或禁用GTCCRA的输入捕捉，当GTIOCA输入为1。

ASELCm位（ELC_GPTm事件源计数器GTCCRA输入捕捉使能）（m=A到H）

ASELCm位启用或禁用ELC_GPTm事件输入上GTCCRA的输入捕捉。

23.2.11 通用PWM定时器输入捕捉源选择寄存器B(GTICBSR)

Address(es): GPT32EHm.GTICBSR 4007 8028h + 0100h × m (m = 0 to 3)
GPT32Em.GTICBSR 4007 8028h + 0100h × m (m = 4 to 7)
GPT32m.GTICBSR 4007 8028h + 0100h × m (m = 8 to 13)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	BSELCH	BSELCG	BSELCF	BSELCE	BSELCD	BSELCC	BSELCB	BSELCA
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BSCBFAH	BSCBFAL	BSCBRAH	BSCBRAL	BSCAFBH	BSCAFBL	BSCARBH	BSCARBL	BSGTRGDF	BSGTRGDR	BSGTRGCF	BSGTRGCR	BSGTRGBF	BSGTRGBR	BSGTRGAF	BSGTRGAR
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	BSGTRGAR	GTETRGA引脚上升输入源GTCCRB输入捕捉使能	0：在GTETRGA输入的上升沿禁用GTCCRB输入捕捉1：在GTETRGA输入的上升沿启用GTCCRB输入捕捉。	R/W
b1	BSGTRGAF	GTETRGA引脚下降输入源GTCCRB输入捕捉使能	0：在GTETRGA输入的下降沿禁用GTCCRB输入捕捉1：在GTETRGA输入的下降沿启用GTCCRB输入捕捉。	R/W
b2	BSGTRGBR	GTETRGB引脚上升输入源GTCCRB输入捕捉使能	0：在GTETRGB输入的上升沿禁用GTCCRB输入捕捉1：在GTETRGB输入的上升沿启用GTCCRB输入捕捉。	R/W
b3	BSGTRGBF	GTETRGB引脚下降输入源GTCCRB输入捕捉使能	0：在GTETRGB输入的下降沿禁用GTCCRB输入捕捉1：在GTETRGB输入的下降沿启用GTCCRB输入捕捉。	R/W
b4	BSGTRGCR	GTETRGC引脚上升沿输入源GTCCRB输入捕捉使能	0：在GTETRGC输入的上升沿禁用GTCCRB输入捕捉1：在GTETRGC输入的上升沿启用GTCCRB输入捕捉。	R/W
b5	BSGTRGCF	GTETRGC引脚下降输入源GTCCRB输入捕捉使能	0：在GTETRGC输入的下降沿禁用GTCCRB输入捕捉1：在GTETRGC输入的下降沿启用GTCCRB输入捕捉。	R/W
b6	BSGTRGDR	GTETRGD引脚上升输入源GTCCRB输入捕捉使能	0：在GTETRGD输入的上升沿禁用GTCCRB输入捕捉1：在GTETRGD输入的上升沿启用GTCCRB输入捕捉。	R/W
b7	BSGTRGDF	GTETRGD引脚下降输入源GTCCRB输入捕捉使能	0：在GTETRGD输入的下降沿禁用GTCCRB输入捕捉1：在GTETRGD输入的下降沿启用GTCCRB输入捕捉。	R/W

Bit	Symbol	Bit name	Description	R/W
b8	BSCARBL	GTIOCA Pin Rising Input during GTIOCB Value Low Source GTCCRB Input Capture Enable	0: Disable GTCCRB input capture on the rising edge of GTIOCA input when GTIOCB input is 0 1: Enable GTCCRB input capture on the rising edge of GTIOCA input when GTIOCB input is 0.	R/W
b9	BSCARBH	GTIOCA Pin Rising Input during GTIOCB Value High Source GTCCRB Input Capture Enable	0: Disable GTCCRB input capture on the rising edge of GTIOCA input when GTIOCB input is 1 1: Enable GTCCRB input capture on the rising edge of GTIOCA input when GTIOCB input is 1.	R/W
b10	BSCAFBL	GTIOCA Pin Falling Input during GTIOCB Value Low Source GTCCRB Input Capture Enable	0: Disable GTCCRB input capture on the falling edge of GTIOCA input when GTIOCB input is 0 1: Enable GTCCRB input capture on the falling edge of GTIOCA input when GTIOCB input is 0.	R/W
b11	BSCAFBH	GTIOCA Pin Falling Input during GTIOCB Value High Source GTCCRB Input Capture Enable	0: Disable GTCCRB input capture on the falling edge of GTIOCA input when GTIOCB input is 1 1: Enable GTCCRB input capture on the falling edge of GTIOCA input when GTIOCB input is 1.	R/W
b12	BSCBRAL	GTIOCB Pin Rising Input during GTIOCA Value Low Source GTCCRB Input Capture Enable	0: Disable GTCCRB input capture on the rising edge of GTIOCB input when GTIOCA input is 0 1: Enable GTCCRB input capture on the rising edge of GTIOCB input when GTIOCA input is 0.	R/W
b13	BSCBRAH	GTIOCB Pin Rising Input during GTIOCA Value High Source GTCCRB Input Capture Enable	0: Disable GTCCRB input capture on the rising edge of GTIOCB input when GTIOCA input is 1 1: Enable GTCCRB input capture on the rising edge of GTIOCB input when GTIOCA input is 1.	R/W
b14	BSCBFAL	GTIOCB Pin Falling Input during GTIOCA Value Low Source GTCCRB Input Capture Enable	0: Disable GTCCRB input capture on the falling edge of GTIOCB input when GTIOCA input is 0 1: Enable GTCCRB input capture on the falling edge of GTIOCB input when GTIOCA input is 0.	R/W
b15	BSCBFAH	GTIOCB Pin Falling Input during GTIOCA Value High Source GTCCRB Input Capture Enable	0: Disable GTCCRB input capture on the falling edge of GTIOCB input when GTIOCA input is 1 1: Enable GTCCRB input capture on the falling edge of GTIOCB input when GTIOCA input is 1.	R/W
b16	BSELCA	ELC_GPTA Event Source GTCCRB Input Capture Enable	0: Disable GTCCRB input capture on ELC_GPTA event input 1: Enable GTCCRB input capture on ELC_GPTA event input.	R/W
b17	BSELCB	ELC_GPTB Event Source GTCCRB Input Capture Enable	0: Disable GTCCRB input capture on ELC_GPTB event input 1: Enable GTCCRB input capture on ELC_GPTB event input.	R/W
b18	BSELCC	ELC_GPTC Event Source GTCCRB Input Capture Enable	0: Disable GTCCRB input capture on ELC_GPTC event input 1: Enable GTCCRB input capture on ELC_GPTC event input.	R/W
b19	BSELCD	ELC_GPTD Event Source GTCCRB Input Capture Enable	0: Disable GTCCRB input capture on ELC_GPTD event input 1: Enable GTCCRB input capture on ELC_GPTD event input.	R/W
b20	BSELCE	ELC_GPTE Event Source GTCCRB Input Capture Enable	0: Disable GTCCRB input capture on ELC_GPTE event input 1: Enable GTCCRB input capture on ELC_GPTE event input.	R/W
b21	BSELCF	ELC_GPTF Event Source GTCCRB Input Capture Enable	0: Disable GTCCRB input capture on ELC_GPTF event input 1: Enable GTCCRB input capture on ELC_GPTF event input.	R/W
b22	BSELCG	ELC_GPTG Event Source GTCCRB Input Capture Enable	0: Disable GTCCRB input capture on ELC_GPTG event input 1: Enable GTCCRB input capture on ELC_GPTG event input.	R/W

Bit	Symbol	位名称	Description	R/W
b8	BSCARBL	GTIOCB值低源期间的GTIOCA引脚上升输入 GTCCRB输入捕捉使能	0：当GTIOCB输入为0时，在GTIOCA输入上升沿禁用GTCCRB输入捕捉1：当GTIOCB输入为0时，在GTIOCA输入上升沿启用GTCCRB输入捕捉。	R/W
b9	BSCARBH	GTIOCB值高源期间的GTIOCA引脚上升输入 GTCCRB输入捕捉使能	0：当GTIOCB输入为1时，在GTIOCA输入上升沿禁止GTCCRB输入捕捉1：当GTIOCB输入为1时，在GTIOCA输入上升沿使能GTCCRB输入捕捉。	R/W
b10	BSCAFBL	GTIOCA引脚下降期间输入 GTIOCB价值低来源 GTCCRB输入捕捉使能	0：当GTIOCB输入为0时，在GTIOCA输入下降沿禁用GTCCRB输入捕捉1：当GTIOCB输入为0时，在GTIOCA输入下降沿启用GTCCRB输入捕捉。	R/W
b11	BSCAFBH	GTIOCA引脚下降期间输入 GTIOCB价值高来源 GTCCRB输入捕捉使能	0：当GTIOCB输入为1时，在GTIOCA输入下降沿禁止GTCCRB输入捕捉1：当GTIOCB输入为1时，在GTIOCA输入下降沿使能GTCCRB输入捕捉。	R/W
b12	BSCBRAL	GTIOCA值低源期间的GTIOCB引脚上升输入 GTCCRB输入捕捉使能	0：当GTIOCA输入为0时，在GTIOCB输入上升沿禁用GTCCRB输入捕捉1：在GTIOCA输入为0时，在GTIOCB输入上升沿启用GTCCRB输入捕捉。	R/W
b13	BSCBRAH	GTIOCA值高源期间的GTIOCB引脚上升输入 GTCCRB输入捕捉使能	0：当GTIOCA输入为1时，在GTIOCB输入上升沿禁用GTCCRB输入捕捉1：当GTIOCA输入为1时，在GTIOCB输入上升沿启用GTCCRB输入捕捉。	R/W
b14	BSCBFAL	在GTIOCB引脚下降输入 GTIOCA价值低来源 GTCCRB输入捕捉使能	0：当GTIOCA输入为0时，在GTIOCB输入下降沿禁止GTCCRB输入捕捉1：当GTIOCA输入为0时，在GTIOCB输入下降沿使能GTCCRB输入捕捉。	R/W
b15	BSCBFAH	在GTIOCB引脚下降输入 GTIOCA价值高来源 GTCCRB输入捕捉使能	0：当GTIOCA输入为1时，在GTIOCB输入下降沿禁用GTCCRB输入捕捉1：当GTIOCA输入为1时，在GTIOCB输入下降沿启用GTCCRB输入捕捉。	R/W
b16	BSELCA	ELC_GPTA事件源 GTCCRB输入捕捉使能	0：在ELC_GPTA事件输入上禁用GTCCRB输入捕捉1：在ELC_GPTA事件输入上启用GTCCRB输入捕捉。	R/W
b17	BSELCB	ELC_GPTB事件源 GTCCRB输入捕捉使能	0：在ELC_GPTB事件输入上禁用GTCCRB输入捕捉1：在ELC_GPTB事件输入上启用GTCCRB输入捕捉。	R/W
b18	BSELCC	ELC_GPTC事件源 GTCCRB输入捕捉使能	0：在ELC_GPTC事件输入上禁用GTCCRB输入捕捉1：在ELC_GPTC事件输入上启用GTCCRB输入捕捉。	R/W
b19	BSELCD	ELC_GPTD事件源 GTCCRB输入捕捉使能	0：在ELC_GPTD事件输入上禁用GTCCRB输入捕捉1：在ELC_GPTD事件输入上启用GTCCRB输入捕捉。	R/W
b20	BSELCE	ELC_GPTE事件源 GTCCRB输入捕捉使能	0：在ELC_GPTE事件输入上禁用GTCCRB输入捕捉1：在ELC_GPTE事件输入上启用GTCCRB输入捕捉。	R/W
b21	BSELCF	ELC_GPTF事件源 GTCCRB输入捕捉使能	0：在ELC_GPTF事件输入上禁用GTCCRB输入捕捉1：在ELC_GPTF事件输入上启用GTCCRB输入捕捉。	R/W
b22	BSELCG	ELC_GPTG事件源 GTCCRB输入捕捉使能	0：在ELC_GPTG事件输入上禁用GTCCRB输入捕捉1：在ELC_GPTG事件输入上启用GTCCRB输入捕捉。	R/W

Bit	Symbol	Bit name	Description	R/W
b23	BSELCH	ELC_GPTH Event Source GTCCRB Input Capture Enable	0: Disable GTCCRB input capture on ELC_GPTH event input 1: Enable GTCCRB input capture on ELC_GPTH event input.	R/W
b31 to b24	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The GTICBSR register sets the source of input capture for GTCCRB.

BSGTRGAR bit (GTETRGA Pin Rising Input Source GTCCRB Input Capture Enable)

The BSGTRGAR bit enables or disables input capture for GTCCRB on the rising edge of the GTETRGA pin input.

BSGTRGAF bit (GTETRGA Pin Falling Input Source GTCCRB Input Capture Enable)

The BSGTRGAF bit enables or disables input capture for GTCCRB on the falling edge of the GTETRGA pin input.

BSGTRGBR bit (GTETRGB Pin Rising Input Source GTCCRB Input Capture Enable)

The BSGTRGBR bit enables or disables input capture for GTCCRB on the rising edge of the GTETRGB pin input.

BSGTRGBF bit (GTETRGB Pin Falling Input Source GTCCRB Input Capture Enable)

The BSGTRGBF bit enables or disables input capture for GTCCRB on the falling edge of the GTETRGB pin input.

BSGTRGCR bit (GTETRGC Pin Rising Input Source GTCCRB Input Capture Enable)

The BSGTRGCR bit enables or disables input capture for GTCCRB on the rising edge of the GTETRGC pin input.

BSGTRGCF bit (GTETRGC Pin Falling Input Source GTCCRB Input Capture Enable)

The BSGTRGCF bit enables or disables input capture for GTCCRB on the falling edge of the GTETRGC pin input.

BSGTRGDR bit (GTETRGD Pin Rising Input Source GTCCRB Input Capture Enable)

The BSGTRGDR bit enables or disables input capture for GTCCRB on the rising edge of the GTETRGD pin input.

BSGTRGDF bit (GTETRGD Pin Falling Input Source GTCCRB Input Capture Enable)

The BSGTRGDF bit enables or disables input capture for GTCCRB on the falling edge of the GTETRGD pin input.

BSCARBL bit (GTIOCA Pin Rising Input during GTIOCB Value Low Source GTCCRB Input Capture Enable)

The BSCARBL bit enables or disables input capture for GTCCRB on the rising edge of the GTIOCA pin input when the GTIOCB input is 0.

BSCARBH bit (GTIOCA Pin Rising Input during GTIOCB Value High Source GTCCRB Input Capture Enable)

The BSCARBH bit enables or disables input capture for GTCCRB on the rising edge of the GTIOCA pin input when the GTIOCB input is 1.

BSCAFBL bit (GTIOCA Pin Falling Input during GTIOCB Value Low Source GTCCRB Input Capture Enable)

The BSCAFBL bit enables or disables input capture for GTCCRB on the falling edge of the GTIOCA pin input when the GTIOCB input is 0.

BSCAFBH bit (GTIOCA Pin Falling Input during GTIOCB Value High Source GTCCRB Input Capture Enable)

The BSCAFBH bit enables or disables input capture for GTCCRB on the falling edge of the GTIOCA pin input when the GTIOCB input is 1.

BSCBRAL bit (GTIOCB Pin Rising Input during GTIOCA Value Low Source GTCCRB Input Capture Enable)

The BSCBRAL bit enables or disables input capture for GTCCRB on the rising edge of the GTIOCB pin input when the

Bit	Symbol	位名称	Description	R/W
b23	BSELCH	ELC_GPTH事件源GTCCRB输入捕捉使能	0：在ELC_GPTH事件输入上禁用GTCCRB输入捕捉1：在ELC_GPTH事件输入上启用GTCCRB输入捕捉。	R/W
b31 to b24	—	Reserved	这些位被读取为0。写入值应为0。	R/W

GTICBSR寄存器设置GTCCRB的输入捕捉源。

BSGTRGAR位（GTETRGA引脚上升沿输入源GTCCRB输入捕捉使能）

BSGTRGAR位在GTETRGA引脚输入的上升沿启用或禁用GTCCRB的输入捕捉。

BSGTRGAF位（GTETRGA引脚下降输入源GTCCRB输入捕捉使能）

BSGTRGAF位在GTETRGA引脚输入的下降沿启用或禁用GTCCRB的输入捕捉。

BSGTRGBR位（GTETRGB引脚上升沿输入源GTCCRB输入捕捉使能）

BSGTRGBR位在GTETRGB引脚输入的上升沿启用或禁用GTCCRB的输入捕捉。

BSGTRGBF位（GTETRGB引脚下降输入源GTCCRB输入捕捉使能）

BSGTRGBF位在GTETRGB引脚输入的下降沿启用或禁用GTCCRB的输入捕捉。

BSGTRGCR位（GTETRGC引脚上升沿输入源GTCCRB输入捕捉使能）

BSGTRGCR位在GTETRGC引脚输入的上升沿启用或禁用GTCCRB的输入捕捉。

BSGTRGCF位（GTETRGC引脚下降输入源GTCCRB输入捕捉使能）

BSGTRGCF位在GTETRGC引脚输入的下降沿启用或禁用GTCCRB的输入捕捉。

BSGTRGDR位（GTETRGD引脚上升沿输入源GTCCRB输入捕捉使能）

BSGTRGDR位在GTETRGD引脚输入的上升沿启用或禁用GTCCRB的输入捕捉。

BSGTRGDF位（GTETRGD引脚下降输入源GTCCRB输入捕捉使能）

BSGTRGDF位在GTETRGD引脚输入的下降沿启用或禁用GTCCRB的输入捕捉。

BSCARBL位（GTIOCB值低电平期间GTIOCA引脚上升沿输入源GTCCRB输入捕捉Enable）

BSCARBL位在GTIOCA引脚输入的上升沿启用或禁用GTCCRB的输入捕捉，当GTIOCB输入为0。

BSCARBH位（GTIOCB值高电平期间GTIOCA引脚的上升沿输入源GTCCRB输入捕捉Enable）

BSCARBH位在GTIOCA引脚输入的上升沿启用或禁用GTCCRB的输入捕捉，当GTIOCB输入为1。

BSCAFBL位（GTIOCB值低电平期间GTIOCA引脚下降输入源GTCCRB输入捕捉Enable）

BSCAFBL位在GTIOCA引脚输入的下降沿启用或禁用GTCCRB的输入捕捉，当GTIOCB输入为0。

BSCAFBH位（GTIOCB值高电平期间GTIOCA引脚下降输入源GTCCRB输入捕捉Enable）

BSCAFBH位在GTIOCA引脚输入的下降沿启用或禁用GTCCRB的输入捕捉，当GTIOCB输入为1。

BSCBRAL位（GTIOCA值低电平期间GTIOCB引脚上升沿输入源GTCCRB输入捕捉Enable）

BSCBRAL位在GTIOCB引脚输入的上升沿启用或禁用GTCCRB的输入捕捉，当

GTIOCA input is 0.

BSCBRAH bit (GTIOCB Pin Rising Input during GTIOCA Value High Source GTCCRB Input Capture Enable)

The BSCBRAH bit enables or disables input capture for GTCCRB on the rising edge of the GTIOCB pin input when the GTIOCA input is 1.

BSCBFAL bit (GTIOCB Pin Falling Input during GTIOCA Value Low Source GTCCRB Input Capture Enable)

The BSCBFAL bit enables or disables input capture for GTCCRB on the falling edge of the GTIOCB pin input when the GTIOCA input is 0.

BSCBFAH bit (GTIOCB Pin Falling Input during GTIOCA Value High Source GTCCRB Input Capture Enable)

The BSCBFAH bit enables or disables input capture for GTCCRB on the falling edge of the GTIOCB pin input when the GTIOCA input is 1.

BSELCm bit (ELC_GPTm Event Source Counter GTCCRB Input Capture Enable) (m = A to H)

The BSELCm bit enables or disables input capture for GTCCRB on the ELC_GPTm event input.

23.2.12 General PWM Timer Control Register (GTCR)

Address(es): GPT32EHm.GTCR 4007 802Ch + 0100h × m (m = 0 to 3)
GPT32Em.GTCR 4007 802Ch + 0100h × m (m = 4 to 7)
GPT32m.GTCR 4007 802Ch + 0100h × m (m = 8 to 13)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	TPCS[2:0]			—	—	—	—	—	MD[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CST
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	CST	Count Start	0: Stop count operation 1: Perform count operation.	R/W
b15 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b18 to b16	MD[2:0]	Mode Select	b18 b16 0 0 0: Saw-wave PWM mode (single buffer or double buffer possible) 0 0 1: Saw-wave one-shot pulse mode (fixed buffer operation) 0 1 0: Setting prohibited 0 1 1: Setting prohibited 1 0 0: Triangle-wave PWM mode 1 (32-bit transfer at trough) (single buffer or double buffer possible) 1 0 1: Triangle-wave PWM mode 2 (32-bit transfer at crest and trough) (single buffer or double buffer possible) 1 1 0: Triangle-wave PWM mode 3 (64-bit transfer at trough) (fixed buffer operation) 1 1 1: Setting prohibited.	R/W
b23 to b19	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

GTIOCA输入为0。

BSCBRAH位（GTIOCA值高电平期间GTIOCB引脚的上升沿输入源GTCCRB输入捕捉Enable）

BSCBRAH位在GTIOCB引脚输入的上升沿启用或禁用GTCCRB的输入捕捉，当GTIOCA输入为1。

BSCBFAL位（GTIOCA值低电平期间GTIOCB引脚下降输入源GTCCRB输入捕捉Enable）

BSCBFAL位在GTIOCB引脚输入的下降沿启用或禁用GTCCRB的输入捕捉，当GTIOCA输入为0。

BSCBFAH位（GTIOCA值高电平期间GTIOCB引脚下降输入源GTCCRB输入捕捉Enable）

BSCBFAH位在GTIOCB引脚输入的下降沿启用或禁用GTCCRB的输入捕捉，当GTIOCA输入为1。

BSELCm位（ELC_GPTm事件源计数器GTCCRB输入捕捉使能）（m=A到H）

BSELCm位启用或禁用ELC_GPTm事件输入上GTCCRB的输入捕捉。

23.2.12 通用PWM定时器控制寄存器(GTCR)

Address(es): GPT32EHm.GTCR 4007 802Ch + 0100h × m (m = 0 to 3)
GPT32Em.GTCR 4007 802Ch + 0100h × m (m = 4 to 7)
GPT32m.GTCR 4007 802Ch + 0100h × m (m = 8 to 13)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	TPCS[2:0]			—	—	—	—	—	MD[2:0]		
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CST
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	CST	计数开始	0：停止计数操作1：进行计数操作。	R/W
b15 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b18 to b16	MD[2:0]	模式选择	b18b16000：Saw-wavePWM模式（单缓冲或双缓冲均可）001：Saw-waveone-shot脉冲模式（固定缓冲操作）010：设置禁止011：设置禁止100：三角波PWM模式1（波谷32位传输）（可单缓冲器或双缓冲器）101：三角波PWM模式2（波峰和波谷32位传输）（单缓冲器或双缓冲器可能）110：三角波PWM模式3（波谷64位传输）（固定缓冲操作）111：禁止设置。	R/W
b23 to b19	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Bit	Symbol	Bit name	Description	R/W
b26 to b24	TPCS[2:0]	Timer Prescaler Select	b26 b24 0 0 0: PCLKD/1 0 0 1: PCLKD/4 0 1 0: PCLKD/16 0 1 1: PCLKD/64 1 0 0: PCLKD/256 1 0 1: PCLKD/1024.	R/W
b31 to b27	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The GTCR register controls GTCNT.

CST bit (Count Start)

The CST bit controls the GTCNT counter start and stop.

[Setting conditions]

- GTSTR value in which the channel number associated with the bit number is set to 1 with the GTSSR.CSTRT bit being 1
- The ELC event input or the GTIOCA/GTIOCB/GTETRGn port input event enabled by GTSSR as the counter start source occurs
- 1 is written by software directly.

[Clearing conditions]

- GTSTP value in which the channel number associated with the bit number is set to 1 with the GTSSR.CSTOP bit being 1.
- The ELC event input or the GTIOCA/GTIOCB/GTETRGn port input event enabled by GTSSR as the counter stop source occurs
- 0 is written by software directly.

MD[2:0] bits (Mode Select)

The MD[2:0] bits select the GPT operating mode. The MD[2:0] bits must be set while the GTCNT operation is stopped.

TPCS[2:0] bits (Timer Prescaler Select)

The TPCS[2:0] bits select the clock for GTCNT. A clock prescaler can be selected independently for each channel. The TPCS[2:0] bits must be set while the GTCNT operation is stopped.

23.2.13 General PWM Timer Count Direction and Duty Setting Register (GTUDDTYC)

Address(es): GPT32EHm.GTUDDTYC 4007 8030h + 0100h × m (m = 0 to 3)
GPT32Em.GTUDDTYC 4007 8030h + 0100h × m (m = 4 to 7)
GPT32m.GTUDDTYC 4007 8030h + 0100h × m (m = 8 to 13)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	OBDTYR	OBDTYF	OBDTY[1:0]		—	—	—	—	OADTYR	OADTYF	OADTY[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	UDF	UD
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Bit name	Description	R/W
b0	UD	Count Direction Setting	0: GTCNT counts down 1: GTCNT counts up.	R/W

Bit	Symbol	位名称	Description	R/W
b26 to b24	TPCS[2:0]	定时器预分频器选择	b26 b24 0 0 0: PCLKD/1 0 0 1: PCLKD/4 0 1 0: PCLKD/16 0 1 1: PCLKD/64 1 0 0: PCLKD/256 1 0 1: PCLKD/1024.	R/W
b31 to b27	—	Reserved	这些位被读取为0。写入值应为0。	R/W

GTCR寄存器控制GTCNT。

CST位（计数开始）

CST位控制GTCNT计数器的启动和停止。

[Setting conditions]

- GTSTR值，其中与位号关联的通道号设置为1，GTSSR.CSTRT位为1
- 发生由GTSSR作为计数器启动源启用的ELC事件输入或GTIOCAGTIOCBGTETRn端口输入事件
- 1由软件直接编写。

[Clearing conditions]

- GTSTP值，其中与位号关联的通道号设置为1，GTSSR.CSTOP位为1。
- 发生由GTSSR作为计数器停止源启用的ELC事件输入或GTIOCAGTIOCBGTETRn端口输入事件
- 0由软件直接写入。

MD[2:0]位（模式选择）

MD[2:0]位选择GPT操作模式。当GTCNT操作停止时，必须设置MD[2:0]位。

TPCS[2:0]位（定时器预分频器选择）

TPCS[2:0]位选择GTCNT的时钟。可为每个通道独立选择时钟预分频器。这
当GTCNT操作停止时，必须设置TPCS[2:0]位。

23.2.13 通用PWM定时器计数方向和占空比设置寄存器(GTUDDTYC)

Address(es): GPT32EHm.GTUDDTYC 4007 8030h + 0100h × m (m = 0 to 3)
GPT32Em.GTUDDTYC 4007 8030h + 0100h × m (m = 4 to 7)
GPT32m.GTUDDTYC 4007 8030h + 0100h × m (m = 8 to 13)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	OBDTYR	OBDTYF	OBDTY[1:0]		—	—	—	—	OADTYR	OADTYF	OADTY[1:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	UDF	UD
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	位名称	Description	R/W
b0	UD	计数方向设置	0：GTCNT向下计数1： GTCNT向上计数。	R/W

Bit	Symbol	Bit name	Description	R/W
b1	UDF	Forcible Count Direction Setting	0: Do not force setting 1: Force setting.	R/W
b15 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b17, 16	OADTY[1:0]	GTIOCA Output Duty Setting	b17 b16 0 x: GTIOCA pin duty depends on compare match 1 0: GTIOCA pin duty = 0% 1 1: GTIOCA pin duty = 100%.	R/W
b18	OADTYF	Forcible GTIOCA Output Duty Setting	0: Do not force setting 1: Force setting.	R/W
b19	OADTYR	GTIOCA Output Value Selecting after Releasing 0%/100% Duty Setting	0: Apply output value set in 0%/100% duty to GTIOA[3:2] function after releasing 0%/100% duty setting 1: Apply masked compare match output value to GTIOA[3:2] function after releasing 0%/100% duty setting.	R/W
b23 to b20	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b25, b24	OBDTY[1:0]	GTIOCB Output Duty Setting	b25 b24 0 x: GTIOCB pin duty depends on compare match 1 0: GTIOCB pin duty = 0% 1 1: GTIOCB pin duty = 100%.	R/W
b26	OBDTYF	Forcible GTIOCB Output Duty Setting	0: Do not force setting 1: Force setting.	R/W
b27	OBDTYR	GTIOCB Output Value Selecting after Releasing 0%/100% Duty Setting	0: Apply output value set in 0%/100% duty to GTIOB[3:2] function after releasing 0%/100% duty setting 1: Apply masked compare match output value to GTIOB[3:2] function after releasing 0%/100% duty setting.	R/W
b31 to b28	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

x: Don't care

The GTUDDTYC register sets the direction in which GTCNT counts (up-counting or down-counting) and sets the duty of GTIOCA/GTIOCB pin output.

Count direction in saw-wave mode

When the UD value is set to 0 during up-counting, the count direction changes at an overflow (the timing synchronous with count clock after the GTCNT value becomes the GTPR value). When the UD value is set to 1 during down-counting, the count direction changes at an underflow (the timing synchronous with count clock after the GTCNT value becomes 0).

When the UD value changes from 1 to 0 with the UDF bit being 0 and while counting is stopped, the counter starts up-counting and the count direction changes at an overflow (the timing synchronous with count clock after the GTCNT value becomes GTPR value). When the UD value changes from 0 to 1 with the UDF bit being 0 and while counting is stopped, the counter starts down-counting and the count direction changes at an underflow (the timing synchronous with count clock after the GTCNT value becomes 0).

When the UDF bit is set to 1 while counting is stopped, the UD bit value is reflected in the count direction when counting starts.

Count direction in triangle-wave mode

When the UD value changes during counting, the count direction does not change. When the UD value changes while the UDF bit is 0 and counting is stopped, the change is not reflected in the count direction when counting starts.

When the UDF bit is set to 1 while counting is stopped, the UD value is reflected in the count direction when counting starts.

UD bit (Count Direction Setting)

The UD bit sets the count direction for GTCNT, either up-counting or down-counting.

UDF bit (Forcible Count Direction Setting)

The UDF bit forcibly sets the count direction when GTCNT starts operation as the UD value. Only write 0 to this bit during counter operation. When 1 is written to UDF while counting is stopped, return UDF to 0 before counting starts.

Bit	Symbol	位名称	Description	R/W
b1	UDF	强制计数方向 Setting	0：不强制设置1：强制设置。	R/W
b15 to b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b17, 16	OADTY[1:0]	GTIOCA输出占空比设置	b17b160x：GTIOCA引脚占空比取决于比较匹配10：GTIOCA引脚占空比=0%11：GTIOCA引脚占空比=100%。	R/W
b18	OADTYF	强制GTIOCA输出占空比 Setting	0：不强制设置1：强制设置。	R/W
b19	OADTYR	解除0%100%占空比设置后GTIOCA输出值选择	0：在释放0%100%占空比设置后将0%100%占空比中设置的输出值应用到GTIOA[3:2]功能1：在释放0%100%后将屏蔽比较匹配输出值应用到GTIOA[3:2]功能职责设置。	R/W
b23 to b20	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b25, b24	OBDTY[1:0]	GTIOCB输出占空比设置	b25b240x：GTIOCB引脚占空比取决于比较匹配10：GTIOCB引脚占空比=0%11：GTIOCB引脚占空比=100%。	R/W
b26	OBDTYF	强制GTIOCB输出占空比 Setting	0：不强制设置1：强制设置。	R/W
b27	OBDTYR	解除0%100%占空比设置后GTIOCB输出值选择	0：在释放0%100%duty设置后将0%100%duty中设置的输出值应用到GTIOB[3:2]功能1：在释放0%100%后将屏蔽比较匹配输出值应用到GTIOB[3:2]功能职责设置。	R/W
b31 to b28	—	Reserved	这些位被读取为0。写入值应为0。	R/W

x：不关心GTUDDTYC寄存器设置GTCNT计数的方向（向上计数或向下计数）并设置GTIOCAGTIOCB引脚输出的占空比。

锯波模式下的计数方向

如果在向上计数期间将UD值设置为0，则计数方向会在溢出时发生变化（GTCNT值变为GTPR值后与计数时钟同步的时序）。在递减计数期间将UD值设置为1时，计数方向会在下溢（GTCNT值变为0后与计数时钟同步的时序）下发生变化。

当UDF位为0且UD值从1变为0且计数停止时，计数器开始向上计数，并且计数方向在溢出时改变（GTCNT值变为GTPR值后与计数时钟同步的时序）。当UDF位为0且UD值从0变为1且计数停止时，计数器开始递减计数并且计数方向在下溢时改变（GTCNT值变为0后与计数时钟同步的时序）。

当计数停止时UDF位设置为1时，UD位值在计数开始时反映在计数方向上。

三角波模式下的计数方向

计数过程中UD值变化时，计数方向不变。当UD值改变而UDF位为0时停止计数，计数开始时变化不反映在计数方向上。

当计数停止时UDF位设置为1时，UD值在计数开始时反映在计数方向上。

UD位（计数方向设置）

UD位设置GTCNT的计数方向，向上计数或向下计数。

UDF位（强制计数方向设置）

当GTCNT开始操作时，UDF位将计数方向强制设置为UD值。仅在计数器操作期间向该位写入0。当计数停止时向UDF写入1时，在计数开始前将UDF恢复为0。

Output duty in saw-wave mode

When the OADTY/OBDTY value changes during up-counting, the duty is reflected at an overflow (GTCNT = GTPR). When the OADTY/OBDTY value changes during down-counting, the duty is reflected at an underflow (GTCNT = 0).

When the OADTY/OBDTY value changes to 1 with the OADTYF/OBDTYF bit being 0 and while counting is stopped, the output duty is not reflected at starting counter operation. When the count direction is up, the output duty is reflected at an overflow (GTCNT = GTPR). When the count direction is down, the output duty is reflected at an underflow (GTCNT = 0).

When the OADTY/OBDTY value changes to 0 with the OADTYF/OBDTYF bit being 1 and while counting is stopped, the output duty is reflected at starting counter operation.

Output duty in triangle-wave mode

When the OADTY/OBDTY value changes during counting, the duty is reflected at an underflow. When the OADTY/OBDTY value changes to 1 with the OADTYF/OBDTYF bit being 0 and while counting is stopped, the output duty is not reflected at starting counter operation. The output duty is reflected at an underflow.

When the OADTY/OBDTY value changes to 0 with the OADTYF/OBDTYF bit being 1 and while counting is stopped, the output duty is reflected at starting counter operation.

OmDTY[1:0] bits (GTIOCm Output Duty Setting) (m = A, B)

The OmDTY[1:0] bits set the output duty of the GTIOCm pin to either 0%, 100%, or compare match control.

OmDTYF bit (Forcible GTIOCm Output Duty Setting) (m = A, B)

The OmDTYF bit forcibly sets the output duty cycle to the OmDTY setting. Set this bit to 0 during counter operation. When OmDTYF bit is set to 1 while counting is stopped, return OmDTYF to 0 until the first period ends after the counter starts.

OmDTYR bit (GTIOCm Output Value Selecting after Releasing 0%/100% Duty Setting) (m = A, B)

The OmDTYR bits select the value that is the object of output retained or toggled at cycle end, when the control changes from 0%/100% duty setting to compare match for GTIOCm pin and GTIOR.GTIOm[3:2] are set to 00b (output retained at cycle end) or GTIOR.GTIOm[3:2] are set to 11b (output toggled at cycle end).

While the duty 0%/100% setting operation is running, the compare match operation continues inside the GPT32. When the OmDTYR bit is set to 1, the GTIOCm pin is in the output state selected by the GTIOR.GTIOm [3:2] bit at the end of the cycle in the compare match operation.

23.2.14 General PWM Timer I/O Control Register (GTIOR)

Address(es): GPT32EHm.GTIOR 4007 8034h + 0100h × m (m = 0 to 3)
GPT32Em.GTIOR 4007 8034h + 0100h × m (m = 4 to 7)
GPT32m.GTIOR 4007 8034h + 0100h × m (m = 8 to 13)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	NFCSB[1:0]		NFBEN	—	—	OBDF[1:0]		OBE	OBHLD	OBDFLT	—	GTIOB[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	NFCSA[1:0]		NFAEN	—	—	OADF[1:0]		OAE	OAHLD	OADFLT	—	GTIOA[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b4 to b0	GTIOA[4:0]	GTIOCA Pin Function Select	See Table 23.5.	R/W
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6	OADFLT	GTIOCA Pin Output Value Setting at the Count Stop	0: Output low on GTIOCA pin when counting is stopped 1: Output high on GTIOCA pin when counting is stopped.	R/W

锯波模式下的输出占空比

当OADTYOBDTY值在递增计数期间发生变化时，占空比反映在溢出处(GTCNT=GTPR)。
当向下计数期间OADTYOBDTY值发生变化时，占空比反映为下溢(GTCNT=0)。

当OADTYFOBDTYF位为0且OADTYOBDTY值变为1并且计数停止时，输出占空比不会反映在开始计数器操作时。当计数方向向上时，输出占空比反映在溢出处(GTCNT=GTPR)。当计数方向向下时，输出占空比反映为下溢(GTCNT=0)。

当OADTYOBDTY值变为0且OADTYFOBDTYF位为1且计数停止时，输出占空比反映在开始计数器操作时。

三角波模式下的输出占空比

当计数期间OADTYOBDTY值发生变化时，占空比反映为下溢。当。。。的时候
OADTYOBDTY值在OADTYFOBDTYF位为0时变为1，当计数停止时，输出占空比不会反映在开始计数器操作时。输出占空比反映在下溢处。

当OADTYOBDTY值变为0且OADTYFOBDTYF位为1且计数停止时，输出占空比反映在开始计数器操作时。

OmDTY[1:0]位（GTIOCm输出占空比设置）（m=A，B）

OmDTY[1:0]位将GTIOCm引脚的输出占空比设置为0%、100%或比较匹配控制。

OmDTYF位（强制GTIOCm输出占空比设置）（m=A，B）

OmDTYF位强制将输出占空比设置为OmDTY设置。在计数器操作期间将此位设置为0。
如果在停止计数时将OmDTYF位设置为1，则将OmDTYF恢复为0，直到计数器开始后第一个周期结束。

OmDTYR位（释放0%100%占空比设置后选择GTIOCm输出值）（m=A、B）

当控制从0%100%占空比设置更改为GTIOCm引脚的比较匹配且GTIOR.GTIOm[3:2]设置为00b时，OmDTYR位选择作为输出对象在周期结束时保留或切换的值（输出在循环结束时保留）或GTIOR.GTIOm[3:2]设置为11b（输出在循环结束时切换）。

在运行占空比0%100%设置操作时，比较匹配操作在GPT32内部继续进行。当OmDTYR位设置为1时，GTIOCm引脚在比较匹配操作的周期结束时处于由GTIOR.GTIOm[3:2]位选择的输出状态。

23.2.14 通用PWM定时器IO控制寄存器(GTIOR)

Address(es): GPT32EHm.GTIOR 4007 8034h + 0100h × m (m = 0 to 3)
GPT32Em.GTIOR 4007 8034h + 0100h × m (m = 4 to 7)
GPT32m.GTIOR 4007 8034h + 0100h × m (m = 8 to 13)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	NFCSB[1:0]		NFBEN	—	—	OBDF[1:0]		OBE	OBHLD	OBDFLT	—	GTIOB[4:0]				
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	NFCSA[1:0]		NFAEN	—	—	OADF[1:0]		OAE	OAHLD	OADFLT	—	GTIOA[4:0]				
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b4 to b0	GTIOA[4:0]	GTIOCA引脚功能选择	见表23.5。	R/W
b5	—	Reserved	该位读取为0。写入值应为0。	R/W
b6	OADFLT	GTIOCA引脚输出值在计数停止处设置	0：计数停止时GTIOCA引脚输出低电平1：计数停止时GTIOCA引脚输出高电平。	R/W

Bit	Symbol	Bit name	Description	R/W
b7	OAHLD	GTIOCA Pin Output Setting at the Start/Stop Count	0: Set GTIOCA pin output level on counting start and stop based on the register setting. 1: Retain GTIOCA pin output level on counting start and stop.	R/W
b8	OAE	GTIOCA Pin Output Enable	0: Disable output 1: Enable output.	R/W
b10, b9	OADF[1:0]	GTIOCA Pin Disable Value Setting	b10 b9 0 0: Prohibit output disable 0 1: Set GTIOCA pin to Hi-Z on output disable 1 0: Set GTIOCA pin to 0 on output disable 1 1: Set GTIOCA pin to 1 on output disable.	R/W
b12, b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b13	NFAEN	Noise Filter A Enable	0: Disable noise filter for GTIOCA pin 1: Enable noise filter for GTIOCA pin.	R/W
b15, b14	NFCSA[1:0]	Noise Filter A Sampling Clock Select	b15 b14 0 0: PCLKD/1 0 1: PCLKD/4 1 0: PCLKD/16 1 1: PCLKD/64.	R/W
b20 to b16	GTIOB[4:0]	GTIOCB Pin Function Select	See Table 23.5.	R/W
b21	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b22	OBDFLT	GTIOCB Pin Output Value Setting at the Count Stop	0: Output low on GTIOCB pin when counting is stopped 1: Output high on GTIOCB pin when counting is stopped.	R/W
b23	OBHLD	GTIOCB Pin Output Setting at the Start/Stop Count	0: Set GTIOCB pin output level on counting start and stop based on the register setting 1: Retain GTIOCB pin output level on counting start and stop.	R/W
b24	OBE	GTIOCB Pin Output Enable	0: Disable output 1: Enable output.	R/W
b26, b25	OBDF[1:0]	GTIOCB Pin Disable Value Setting	b26 b25 0 0: Prohibit output disable 0 1: Set GTIOCB pin to Hi-Z on output disable 1 0: Set GTIOCB pin to 0 on output disable 1 1: Set GTIOCB pin to 1 on output disable.	R/W
b28, b27	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b29	NFBEN	Noise Filter B Enable	0: Disable noise filter for GTIOCB pin 1: Enable noise filter for GTIOCB pin.	R/W
b31, b30	NFCSB[1:0]	Noise Filter B Sampling Clock Select	b31 b30 0 0: PCLKD/1 0 1: PCLKD/4 1 0: PCLKD/16 1 1: PCLKD/64.	R/W

The GTIOR register sets the functions of the GTIOCA and GTIOCB pins.

GTIOA[4:0] bits (GTIOCA Pin Function Select)

The GTIOA[4:0] bits select the GTIOCA pin function. For details, see Table 23.5.

OADFLT bit (GTIOCA Pin Output Value Setting at the Count Stop)

The OADFLT bit selects whether the GTIOCA pin outputs high or low when counting is stopped.

OAHLD bit (GTIOCA Pin Output Setting at the Start/Stop Count)

The OAHLD bit specifies whether the GTIOCA pin output level is retained or the level depends on the register setting when counting is started or stopped.

[When the OAHLD bit is set to 0]

- The value specified in the GTIOA[4] bit is output when counting starts
- The value specified in the OADFLT bit is output when counting stops
- If the OADFLT bit is modified while counting is stopped, the new value is immediately reflected in the output.

Bit	Symbol	位名称	Description	R/W
b7	OAHLD	开始停止计数时的GTIOCA引脚输出设置	0：根据寄存器设置在计数开始和停止时设置GTIOCA引脚输出电平。1：在计数开始和停止时保持GTIOCA引脚输出电平。	R/W
b8	OAE	GTIOCA引脚输出使能	0：禁用输出1： 启用输出。	R/W
b10, b9	OADF[1:0]	GTIOCA引脚禁用值 Setting	b10b900：禁止输出禁用01：在输出禁用时将GTIOCA引脚设置为Hi-Z10：在输出禁用时将GTIOCA引脚设置为011：在输出禁用时将GTIOCA引脚设置为1。	R/W
b12, b11	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b13	NFAEN	噪声滤波器A启用	0：禁用GTIOCA引脚的噪声滤波器1 ：启用GTIOCA引脚的噪声滤波器。	R/W
b15, b14	NFCSA[1:0]	噪声滤波器A采样时钟 Select	b15 b14 0 0: PCLKD/1 0 1: PCLKD/4 1 0: PCLKD/16 1 1: PCLKD/64.	R/W
b20 to b16	GTIOB[4:0]	GTIOCB引脚功能选择	见表23.5。	R/W
b21	—	Reserved	该位读取为0。写入值应为0。	R/W
b22	OBDFLT	GTIOCB引脚输出值 在计数停止处设置	0：计数停止时GTIOCB引脚输出低电平1：计数停止时GTIOCB引脚输出高电平。	R/W
b23	OBHLD	开始停止计数时的GTIOCB引脚输出设置	0：根据寄存器设置设置GTIOCB引脚在计数开始和停止时的输出电平1：在计数开始和停止时保持GTIOCB引脚输出电平。	R/W
b24	OBE	GTIOCB引脚输出使能	0：禁用输出1： 启用输出。	R/W
b26, b25	OBDF[1:0]	GTIOCB引脚禁用值 Setting	b26b2500：禁止输出禁用01：在输出禁用时将GTIOCB引脚设置为Hi-Z10：在输出禁用时将GTIOCB引脚设置为011：在输出禁用时将GTIOCB引脚设置为1。	R/W
b28, b27	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b29	NFBEN	噪声滤波器B启用	0：禁用GTIOCB引脚的噪声滤波器1 ：启用GTIOCB引脚的噪声滤波器。	R/W
b31, b30	NFCSB[1:0]	噪声滤波器B采样时钟 Select	b31 b30 0 0: PCLKD/1 0 1: PCLKD/4 1 0: PCLKD/16 1 1: PCLKD/64.	R/W

GTIOR寄存器设置GTIOCA和GTIOCB引脚的功能。

GTIOA[4:0]位（GTIOCA引脚功能选择）

GTIOA[4:0]位选择GTIOCA引脚功能。详见表23.5。

OADFLT位（计数停止时GTIOCA引脚输出值设置）

OADFLT位选择当计数停止时GTIOCA引脚输出高电平还是低电平。

OAHLD位（开始停止计数时GTIOCA引脚输出设置）

OAHLD位指定当计数开始或停止时是否保留GTIOCA引脚输出电平或电平取决于寄存器设置。

[OAHLD位设置为0时]

- 计数开始时输出GTIOA[4]位中指定的值
- 计数停止时输出OADFLT位中指定的值
- 如果在停止计数时修改了OADFLT位，则新值会立即反映在输出中。

[When the OAHLD bit is set to 1]

- The output is retained when counting starts or stops.

OAE bit (GTIOCA Pin Output Enable)

The OAE bit disables or enables the GTIOCA pin output.

When GTCCRA register is used as the input capture register (at least one bit in the GTICASR register is set to 1), the GTIOCA pin does not output regardless of the OAE bit value.

OADF[1:0] bits (GTIOCA Pin Disable Value Setting)

The OADF[1:0] bits select the output value of GTIOCA pin when an output disable request occurs.

NFAEN bit (Noise Filter A Enable)

The NFAEN bit disables or enables the noise filter for input from the GTIOCA pin. Because changing the value of the bit might lead to internal generation of an unexpected edge, select the output compare function for the relevant pin in the GTIOR register before doing so.

NFCSA[1:0] bits (Noise Filter A Sampling Clock Select)

The NFCSA[1:0] bits set the sampling interval for the noise filter of the GTIOCA pin. When setting these bits, wait for 2 cycles of the selected sampling interval before setting the input capture function.

GTIOB[4:0] bits (GTIOCB Pin Function Select)

The GTIOB[4:0] bits select the GTIOCB pin function. For details, see Table 23.5.

OBDFLT bit (GTIOCB Pin Output Value Setting at the Count Stop)

The OBDFLT bit sets whether the GTIOCB pin outputs high or low when counting is stopped.

OBHLD bit (GTIOCB Pin Output Setting at the Start/Stop Count)

The OBHLD bit specifies whether the GTIOCB pin output level is retained or the level depends on the register setting when counting is started or stopped.

[When the OBHLD bit is set to 0]

- The value specified in bit [4] of the GTIOB[4:0] bits is output when counting starts
- The value specified in the OBDFLT bit is output when counting stops
- If the OBDFLT bit is modified while counting is stopped, the new value is immediately reflected in the output.

[When the OBHLD bit is set to 1]

- The output is retained when counting starts or stops.

OBE bit (GTIOCB Pin Output Enable)

The OBE bit disables or enables the GTIOCB pin output.

When GTCCRB register is used as the input capture register (at least one bit in GTICBSR register is set to 1), the GTIOCB pin does not output regardless of the OBE bit value.

OBDF[1:0] bits (GTIOCB Pin Disable Value Setting)

The OBDF[1:0] bits select the output value of GTIOCB pin when an output disable request occurs.

NFBEN bit (Noise Filter B Enable)

The NFBEN bit disables or enables the noise filter for input from the GTIOCB pin. Because changing the value of the bit might lead to the internal generation of an unexpected edge, select the output compare function for the relevant pin in the GTIOR register before doing so.

NFCSB[1:0] bits (Noise Filter B Sampling Clock Select)

The NFCSB[1:0] bits set the sampling interval for the noise filter of the GTIOCB pin. When setting these bits, wait for 2

[OAHLD位设置为1时]

- 当计数开始或停止时，输出保持不变。

OAE位（GTIOCA引脚输出使能）

OAE位禁用或启用GTIOCA引脚输出。

当GTCCRA寄存器用作输入捕捉寄存器时（GTICASR寄存器中至少有一位设置为1），
无论OAE位值如何，GTIOCA引脚都不输出。

OADF[1:0]位（GTIOCA引脚禁用值设置）

当输出禁用请求发生时，OADF[1:0]位选择GTIOCA引脚的输出值。

NFAEN位（噪声滤波器A使能）

NFAEN位禁用或启用来自GTIOCA引脚的输入的噪声滤波器。由于更改该位的值可能会导致内部产生意外边沿，因此在执行此操作之前，请在GTIOR寄存器中为相关引脚选择输出比较功能。

NFCSA[1:0]位（噪声滤波器A采样时钟选择）

NFCSA[1:0]位设置GTIOCA引脚噪声滤波器的采样间隔。设置这些位时，请等待所选采样间隔的2个周期，然后再设置输入捕捉功能。

GTIOB[4:0]位（GTIOCB引脚功能选择）

GTIOB[4:0]位选择GTIOCB引脚功能。详见表23.5。

OBDFLT位（计数停止时GTIOCB引脚输出值设置）

OBDFLT位设置当计数停止时GTIOCB引脚输出高电平还是低电平。

OBHLD位（开始停止计数时GTIOCB引脚输出设置）

OBHLD位指定当计数开始或停止时是保留GTIOCB引脚输出电平还是电平取决于寄存器设置。

[OBHLD位设置为0时]

- 计数开始时输出GTIOB[4:0]位的位[4]中指定的值
- 计数停止时输出OBDFLT位中指定的值
- 如果在停止计数时修改了OBDFLT位，则新值会立即反映在输出中。

[OBHLD位设置为1时]

- 当计数开始或停止时，输出保持不变。

OBE位（GTIOCB引脚输出使能）

OBE位禁用或启用GTIOCB引脚输出。

当GTCCRB寄存器用作输入捕捉寄存器时（GTICBSR寄存器中至少有一位设置为1），
无论OBE位值如何，GTIOCB引脚都不输出。

OBDF[1:0]位（GTIOCB引脚禁用值设置）

当输出禁用请求发生时，OBDF[1:0]位选择GTIOCB引脚的输出值。

NFBEN位（噪声滤波器B启用）

NFBEN位禁用或启用来自GTIOCB引脚的输入的噪声滤波器。因为更改位的值可能会导致内部产生意外边沿，所以在此之前选择GTIOR寄存器中相关引脚的输出比较功能。

NFCSB[1:0]位（噪声滤波器B采样时钟选择）

NFCSB[1:0]位设置GTIOCB引脚噪声滤波器的采样间隔。设置这些位时，等待2

cycles of the selected sampling interval before setting the input capture function.

Table 23.5 Settings of GTIOA[4:0] and GTIOB[4:0] bits

GTIOA/GTIOB[4:0] bits					Function		
b4	b3	b2	b1	b0	b4	b3, b2	b1, b0
0	0	0	0	0	Set initial output low	Retain output at cycle end	Retain output at GTCCRA/GTCCRB compare match
0	0	0	0	1			Output low at GTCCRA/GTCCRB compare match
0	0	0	1	0			Output high at GTCCRA/GTCCRB compare match
0	0	0	1	1			Toggle output at GTCCRA/GTCCRB compare match
0	0	1	0	0		Output low at cycle end	Retain output at GTCCRA/GTCCRB compare match
0	0	1	0	1			Output low at GTCCRA/GTCCRB compare match
0	0	1	1	0			Output high at GTCCRA/GTCCRB compare match
0	0	1	1	1			Toggle output at GTCCRA/GTCCRB compare match
0	1	0	0	0		Output high at cycle end	Retain output at GTCCRA/GTCCRB compare match
0	1	0	0	1			Output low at GTCCRA/GTCCRB compare match
0	1	0	1	0			Output high at GTCCRA/GTCCRB compare match
0	1	0	1	1			Toggle output at GTCCRA/GTCCRB compare match
0	1	1	0	0		Toggle output at cycle end	Retain output at GTCCRA/GTCCRB compare match
0	1	1	0	1			Output low at GTCCRA/GTCCRB compare match
0	1	1	1	0			Output high at GTCCRA/GTCCRB compare match
0	1	1	1	1			Toggle output at GTCCRA/GTCCRB compare match
1	0	0	0	0	Set initial output high	Retain output at cycle end	Retain output at GTCCRA/GTCCRB compare match
1	0	0	0	1			Output low at GTCCRA/GTCCRB compare match
1	0	0	1	0			Output high at GTCCRA/GTCCRB compare match
1	0	0	1	1			Toggle output at GTCCRA/GTCCRB compare match
1	0	1	0	0		Output low at cycle end	Retain output at GTCCRA/GTCCRB compare match
1	0	1	0	1			Output low at GTCCRA/GTCCRB compare match
1	0	1	1	0			Output high at GTCCRA/GTCCRB compare match
1	0	1	1	1			Toggle output at GTCCRA/GTCCRB compare match
1	1	0	0	0		Output high at cycle end	Retain output at GTCCRA/GTCCRB compare match
1	1	0	0	1			Output low at GTCCRA/GTCCRB compare match
1	1	0	1	0			Output high at GTCCRA/GTCCRB compare match
1	1	0	1	1			Toggle output at GTCCRA/GTCCRB compare match
1	1	1	0	0		Toggle output at cycle end	Retain output at GTCCRA/GTCCRB compare match
1	1	1	0	1			Output low at GTCCRA/GTCCRB compare match
1	1	1	1	0			Output high at GTCCRA/GTCCRB compare match
1	1	1	1	1			Toggle output at GTCCRA/GTCCRB compare match

Note 1. The cycle end means an overflow (GTCNT is changed from GTPR to 0 in up-counting) or underflow (GTCNT is changed from 0 to GTPR in down-counting). In this case, the GTCNT counter is cleared for saw waves and for the trough (GTCNT is changed from 0 to 1) for triangle waves.

Note 2. When the timing of a cycle end and the timing of a GTCCRA/GTCCRB compare match are the same in a compare-match operation, the b3 and b2 settings are given priority in saw-wave PWM mode, and the b1 and b0 settings are given priority in any other mode.

Note 3. In event count operation where at least one bit in GTUPSR or GTDNSR is set to 1, the setting of b3 and b2 is ignored.

在设置输入捕捉功能之前选定的采样间隔的周期。

Table 23.5 GTIOA[4:0]和GTIOB[4:0]位的设置

GTIOA/GTIOB[4:0] bits					Function		
b4	b3	b2	b1	b0	b4	b3, b2	b1, b0
0	0	0	0	0	将初始输出设置为低	在循环结束时保留输出	在GTCCRAGTCCRB比较匹配时保留输出
0	0	0	0	1			GTCCRAGTCCRB比较匹配时输出低
0	0	0	1	0			GTCCRAGTCCRB比较匹配时输出高
0	0	0	1	1			在GTCCRAGTCCRB比较匹配时切换输出
0	0	1	0	0		循环结束时输出低	在GTCCRAGTCCRB比较匹配时保留输出
0	0	1	0	1			GTCCRAGTCCRB比较匹配时输出低
0	0	1	1	0			GTCCRAGTCCRB比较匹配时输出高
0	0	1	1	1			在GTCCRAGTCCRB比较匹配时切换输出
0	1	0	0	0		循环结束时输出高	在GTCCRAGTCCRB比较匹配时保留输出
0	1	0	0	1			GTCCRAGTCCRB比较匹配时输出低
0	1	0	1	0			GTCCRAGTCCRB比较匹配时输出高
0	1	0	1	1			在GTCCRAGTCCRB比较匹配时切换输出
0	1	1	0	0		在循环结束时切换输出	在GTCCRAGTCCRB比较匹配时保留输出
0	1	1	0	1			GTCCRAGTCCRB比较匹配时输出低
0	1	1	1	0			GTCCRAGTCCRB比较匹配时输出高
0	1	1	1	1			在GTCCRAGTCCRB比较匹配时切换输出
1	0	0	0	0	将初始输出设置为高	在循环结束时保留输出	在GTCCRAGTCCRB比较匹配时保留输出
1	0	0	0	1			GTCCRAGTCCRB比较匹配时输出低
1	0	0	1	0			GTCCRAGTCCRB比较匹配时输出高
1	0	0	1	1			在GTCCRAGTCCRB比较匹配时切换输出
1	0	1	0	0		循环结束时输出低	在GTCCRAGTCCRB比较匹配时保留输出
1	0	1	0	1			GTCCRAGTCCRB比较匹配时输出低
1	0	1	1	0			GTCCRAGTCCRB比较匹配时输出高
1	0	1	1	1			在GTCCRAGTCCRB比较匹配时切换输出
1	1	0	0	0		循环结束时输出高	在GTCCRAGTCCRB比较匹配时保留输出
1	1	0	0	1			GTCCRAGTCCRB比较匹配时输出低
1	1	0	1	0			GTCCRAGTCCRB比较匹配时输出高
1	1	0	1	1			在GTCCRAGTCCRB比较匹配时切换输出
1	1	1	0	0		在循环结束时切换输出	在GTCCRAGTCCRB比较匹配时保留输出
1	1	1	0	1			GTCCRAGTCCRB比较匹配时输出低
1	1	1	1	0			GTCCRAGTCCRB比较匹配时输出高
1	1	1	1	1			在GTCCRAGTCCRB比较匹配时切换输出

Note 1. 循环结束意味着上溢（向上计数时GTCNT从GTPR变为0）或下溢（向下计数时GTCNT从0变为GTPR）。在这种情况下，对于锯齿波和波谷（GTCNT从0变为1）清除三角波的GTCNT计数器。

Note 2. 在比较匹配操作中，当周期结束的时序和GTCCRAGTCCRB比较匹配的时序相同时，在锯齿波PWM模式下，b3和b2设置优先，b1和b0设置优先在任何其他模式下。

Note 3. 在GTUPSR或GTDNSR中至少一位设置为1的事件计数操作中，忽略b3和b2的设置。

23.2.15 General PWM Timer Interrupt Output Setting Register (GTINTAD)

Address(es): GPT32EHm.GTINTAD 4007 8038h + 0100h × m (m = 0 to 3)
GPT32Em.GTINTAD 4007 8038h + 0100h × m (m = 4 to 7)
GPT32m.GTINTAD 4007 8038h + 0100h × m (m = 8 to 13)

- GPT32EH, GPT32E

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	GRPABL	GRPABH	GRPDTE	—	—	GRP[1:0]		—	—	—	—	ADTRBDEN	ADTRBUEN	ADTRADEN	ADTRAUEN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

- GPT32

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	GRPABL	GRPABH	—	—	—	GRP[1:0]		—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b15 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b16	ADTRAUEN	GTADTRA Compare Match (Up-Counting) A/D Converter Start Request Enable	0: Disable A/D converter start request 1: Enable A/D converter start request.	R/W
b17	ADTRADEN	GTADTRA Compare Match (Down-Counting) A/D Converter Start Request Enable	0: Disable A/D converter start request 1: Enable A/D converter start request.	R/W
b18	ADTRBUEN	GTADTRB Compare Match (Up-Counting) A/D Converter Start Request Enable	0: Disable A/D converter start request 1: Enable A/D converter start request.	R/W
b19	ADTRBDEN	GTADTRB Compare Match (Down-Counting) A/D Converter Start Request Enable	0: Disable A/D converter start request 1: Enable A/D converter start request.	R/W
b23 to b20	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b25, b24	GRP[1:0]	Output Disable Source Select	b25 b24 0 0: Select Group A output disable request 0 1: Select Group B output disable request 1 0: Select Group C output disable request 1 1: Select Group D output disable request.	R/W
b27, b26	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b28	GRPDTE	Dead Time Error Output Disable Request Enable	0: Disable dead time error output disable request 1: Enable dead time error output disable request.	R/W
b29	GRPABH	Same Time Output Level High Disable Request Enable	0: Disable same time output level high disable request 1: Enable same time output level high disable request.	R/W
b30	GRPABL	Same Time Output Level Low Disable Request Enable	0: Disable same time output level low disable request 1: Enable same time output level low disable request.	R/W
b31	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

GTINTAD enables or disables interrupt requests, A/D converter start requests, and output disable requests.

23.2.15 通用PWM定时器中断输出设置寄存器(GTINTAD)

Address(es): GPT32EHm.GTINTAD 4007 8038h + 0100h × m (m = 0 to 3)
GPT32Em.GTINTAD 4007 8038h + 0100h × m (m = 4 to 7)
GPT32m.GTINTAD 4007 8038h + 0100h × m (m = 8 to 13)

- GPT32EH, GPT32E

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	GRPABL	GRPABH	GRPDTE	—	—	GRP[1:0]		—	—	—	—	ADTRBDEN	ADTRBUEN	ADTRADEN	ADTRAUEN
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

- GPT32

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	GRPABL	GRPABH	—	—	—	GRP[1:0]		—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b15 to b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b16	ADTRAUEN	GTADTRA比较匹配（上计数)AD转换器启动请求Enable	0：禁用AD转换器启动请求1：启用AD转换器启动请求。	R/W
b17	ADTRADEN	GTADTRA比较匹配（下计数)AD转换器启动请求Enable	0：禁用AD转换器启动请求1：启用AD转换器启动请求。	R/W
b18	ADTRBUEN	GTADTRB比较匹配（向上计数)AD转换器启动请求Enable	0：禁用AD转换器启动请求1：启用AD转换器启动请求。	R/W
b19	ADTRBDEN	GTADTRB比较匹配（下计数)AD转换器启动请求Enable	0：禁用AD转换器启动请求1：启用AD转换器启动请求。	R/W
b23 to b20	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b25, b24	GRP[1:0]	输出禁用源选择	b25b2400：选择A组输出禁用请求01：选择B组输出禁用请求10：选择C 组输出禁用请求11：选择D组输出禁用请求。	R/W
b27, b26	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b28	GRPDTE	死区时间错误输出禁用请求启用	0：禁用死区错误输出禁用请求1：启用死区错误输出禁用请求。	R/W
b29	GRPABH	同时输出电平高禁用请求启用	0：禁用同时输出电平高禁用请求1：启用同时输出电平高禁用请求。	R/W
b30	GRPABL	同时输出电平低禁用请求启用	0：禁用同时输出电平低禁用请求1：启用同时输出电平低禁用请求。	R/W
b31	—	Reserved	该位读取为0。写入值应为0。	R/W

GTINTAD启用或禁用中断请求、AD转换器启动请求和输出禁用请求。

ADTRAUEN bit (GTADTRA Compare Match (Up-Counting) A/D Converter Start Request Enable)

The ADTRAUEN bit enables or disables A/D converter start requests generated by GTADTRA compare matches during GTCNT up-counting. Only GPT32EH and GPT32E have this bit. GPT32 does not have this bit.

ADTRADEN bit (GTADTRA Compare Match (Down-Counting) A/D Converter Start Request Enable)

The ADTRADEN bit enables or disables A/D converter start requests generated by GTADTRA compare matches during GTCNT down-counting. Only GPT32EH and GPT32E have this bit. GPT32 does not have this bit.

ADTRBUEN bit (GTADTRB Compare Match (Up-Counting) A/D Converter Start Request Enable)

The ADTRBUEN bit enables or disables A/D converter start requests generated by GTADTRB compare matches during GTCNT up-counting. Only GPT32EH and GPT32E have this bit. GPT32 does not have this bit.

ADTRBDEN bit (GTADTRB Compare Match (Down-Counting) A/D Converter Start Request Enable)

The ADTRBDEN bit enables or disables A/D converter start requests generated by GTADTRB compare matches during GTCNT down-counting. Only GPT32EH and GPT32E have this bit. GPT32 does not have this bit.

GRP[1:0] bits (Output Disable Source Select)

The GRP[1:0] bits select GTIOCA pin and GTIOCB pin output disable source. The output disable request to POEG outputs to the group which is selected by GRP[1:0] bits when dead time error, same time output level high or low occurs according to each output disable request enable bits.

GTST.ODF shows the request of output disable source group that is selected with the GRP[1:0] bits.

Set the GRP[1:0] bits when both GTIOR.OAE and GTIOR.OBE are 0.

GRPDTE bit (Dead Time Error Output Disable Request Enable)

The GRPDTE bit enables or disables dead time error output disable request. Only GPT32EH and GPT32E have this bit. GPT32 does not have this bit.

GRPABH bit (Same Time Output Level High Disable Request Enable)

The GRPABH bit enables or disables output disable request when GTIOCA pin and GTIOCB pin output 1 at the same time.

GRPABL bit (Same Time Output Level Low Disable Request Enable)

The GRPABL bit enables or disables output disable request when GTIOCA pin and GTIOCB pin output 0 at the same time.

ADTRAUEN位（GTADTRA比较匹配（向上计数）AD转换器启动请求使能）

ADTRAUEN位启用或禁用GTADTRA比较匹配期间生成的AD转换器启动请求GTCNT递增计数。只有GPT32EH和GPT32E有这个位。GPT32没有这个位。

ADTRADEN位（GTADTRA比较匹配（递减计数）AD转换器启动请求使能）

ADTRADEN位启用或禁用GTADTRA比较匹配期间生成的AD转换器启动请求GTCNT递减计数。只有GPT32EH和GPT32E有这个位。GPT32没有这个位。

ADTRBUEN位（GTADTRB比较匹配（向上计数）AD转换器启动请求使能）

ADTRBUEN位启用或禁用由GTADTRB比较匹配期间生成的AD转换器启动请求GTCNT递增计数。只有GPT32EH和GPT32E有这个位。GPT32没有这个位。

ADTRBDEN位（GTADTRB比较匹配（递减计数）AD转换器启动请求使能）

ADTRBDEN位启用或禁用GTADTRB比较匹配期间生成的AD转换器启动请求GTCNT递减计数。只有GPT32EH和GPT32E有这个位。GPT32没有这个位。

GRP[1:0]位（输出禁用源选择）

GRP[1:0]位选择GTIOCA引脚和GTIOCB引脚输出禁用源。当死区时间错误时，对POEG的输出禁用请求输出到由GRP[1:0]位选择的组，同时根据每个输出禁用请求启用位出现输出电平高或低。

GTST.ODF显示了使用GRP[1:0]位选择的输出禁用源组的请求。

当GTIOR.OAE和GTIOR.OBE都为0时，设置GRP[1:0]位。

GRPDTE位（死区错误输出禁用请求启用）

GRPDTE位启用或禁用死区错误输出禁用请求。只有GPT32EH和GPT32E有这个位。GPT32没有这个位。

GRPABH位（同时输出电平高禁用请求启用）

当GTIOCA引脚和GTIOCB引脚同时输出1时，GRPABH位启用或禁用输出禁用请求。

GRPABL位（同时输出电平低禁用请求启用）

当GTIOCA引脚和GTIOCB引脚同时输出0时，GRPABL位启用或禁用输出禁用请求。

23.2.16 General PWM Timer Status Register (GTST)

Address(es): GPT32EHm.GTST 4007 803Ch + 0100h × m (m = 0 to 3)
GPT32Em.GTST 4007 803Ch + 0100h × m (m = 4 to 7)
GPT32m.GTST 4007 803Ch + 0100h × m (m = 8 to 13)

- GPT32EH, GPT32E

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	OABLF	OABHF	DTEF	—	—	—	ODF	—	—	—	—	ADTRBDF	ADTRBUF	ADTRADF	ADTRAUF
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TUCF	—	—	—	—	ITCNT[2:0]			TCFPU	TCFPO	TCFF	TCFE	TCFD	TCFC	TCFB	TCFA
Value after reset:	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

- GPT32

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	OABLF	OABHF	—	—	—	—	ODF	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TUCF	—	—	—	—	—	—	—	TCFPU	TCFPO	TCFF	TCFE	TCFD	TCFC	TCFB	TCFA
Value after reset:	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	TCFA	Input Capture/Compare Match Flag A	0: No input capture/compare match of GTCCRA occurred 1: Input capture/compare match of GTCCRA occurred.	R/(W)*1
b1	TCFB	Input Capture/Compare Match Flag B	0: No input capture/compare match of GTCCRB occurred 1: Input capture/compare match of GTCCRB occurred.	R/(W)*1
b2	TCFC	Input Compare Match Flag C	0: No compare match of GTCCRC occurred 1: Compare match of GTCCRC occurred.	R/(W)*1
b3	TCFD	Input Compare Match Flag D	0: No compare match of GTCCRD occurred 1: Compare match of GTCCRD occurred.	R/(W)*1
b4	TCFE	Input Compare Match Flag E	0: No compare match of GTCCRE occurred 1: Compare match of GTCCRE occurred.	R/(W)*1
b5	TCFF	Input Compare Match Flag F	0: No compare match of GTCCRF occurred 1: Compare match of GTCCRF occurred.	R/(W)*1
b6	TCFPO	Overflow Flag	0: No overflow (crest) occurred 1: Overflow (crest) occurred.	R/(W)*1
b7	TCFPU	Underflow Flag	0: No underflow (trough) occurred 1: Underflow (trough) occurred.	R/(W)*1
b10 to b8	ITCNT[2:0]	GPTn_OVF/GPTn_UDF Interrupt Skipping Count Counter	Counter for counting the number of times a timer interrupt is skipped.	R
b14 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15	TUCF	Count Direction Flag	0: GTCNT counter is counting down 1: GTCNT counter is counting up.	R
b16	ADTRAUF	GTADTRA Compare Match (Up-Counting) A/D Converter Start Request Flag	0: No compare match of GTADTRA at up-counting occurred 1: A compare match of GTADTRA at up-counting occurred.	R/(W)*1
b17	ADTRADF	GTADTRA Compare Match (Down-Counting) A/D Converter Start Request Flag	0: No compare match of GTADTRA at down-counting occurred 1: A compare match of GTADTRA at down-counting occurred.	R/(W)*1

23.2.16 通用PWM定时器状态寄存器(GTST)

Address(es): GPT32EHm.GTST 4007 803Ch + 0100h × m (m = 0 to 3)
GPT32Em.GTST 4007 803Ch + 0100h × m (m = 4 to 7)
GPT32m.GTST 4007 803Ch + 0100h × m (m = 8 to 13)

- GPT32EH, GPT32E

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	OABLF	OABHF	DTEF	—	—	—	ODF	—	—	—	—	ADTRBDF	ADTRBUF	ADTRADF	ADTRAUF
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TUCF	—	—	—	—	ITCNT[2:0]			TCFPU	TCFPO	TCFF	TCFE	TCFD	TCFC	TCFB	TCFA
重置后的值:	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

- GPT32

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	OABLF	OABHF	—	—	—	—	ODF	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TUCF	—	—	—	—	—	—	—	TCFPU	TCFPO	TCFF	TCFE	TCFD	TCFC	TCFB	TCFA
重置后的值:	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	TCFA	输入捕捉比较匹配 Flag A	0：未发生GTCCRA的输入捕捉比较匹配1：发生GTCCRA的输入捕捉比较匹配。	R/(W)*1
b1	TCFB	输入捕捉比较匹配 Flag B	0：未发生GTCCRB的输入捕捉比较匹配1：发生GTCCRB的输入捕捉比较匹配。	R/(W)*1
b2	TCFC	输入比较匹配标志C	0：未发生GTCCRC比较匹配1：发生GTCCRC比较匹配。	R/(W)*1
b3	TCFD	输入比较匹配标志D	0：未发生GTCCRD比较匹配1：发生GTCCRD比较匹配。	R/(W)*1
b4	TCFE	输入比较匹配标志E	0：未发生GTCCRE比较匹配1：发生GTCCRE比较匹配。	R/(W)*1
b5	TCFF	输入比较匹配标志F	0：未发生GTCCRF比较匹配1：发生GTCCRF比较匹配。	R/(W)*1
b6	TCFPO	溢出标志	0：未发生溢出（波峰）1：发生溢出（波峰）。	R/(W)*1
b7	TCFPU	Underflow Flag	0：未发生下溢（谷）1：发生下溢（谷）。	R/(W)*1
b10 to b8	ITCNT[2:0]	GPTn_OVFGPTn_UDF中断跳过计数 Counter	用于计算跳过定时器中断次数的计数器。	R
b14 to b11	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b15	TUCF	计数方向标志	0：GTCNT计数器向下计数1：GTCNT计数器向上计数。	R
b16	ADTRAUF	GTADTRA比较匹配（向上计数）AD转换器启动请求标志	0：在递增计数时没有发生GTADTRA的比较匹配1：在递增计数时发生了GTADTRA的比较匹配。	R/(W)*1
b17	ADTRADF	GTADTRA比较匹配（递减计数）AD转换器启动请求标志	0：在递减计数时没有发生GTADTRA的比较匹配1：在递减计数时发生了GTADTRA的比较匹配。	R/(W)*1

Bit	Symbol	Bit name	Description	R/W
b18	ADTRBUF	GTADTRB Compare Match (Up-Counting) A/D Converter Start Request Flag	0: No compare match of GTADTRB at up-counting occurred 1: A compare match of GTADTRB at up-counting occurred.	R/(W)*1
b19	ADTRBDF	GTADTRB Compare Match (Down-Counting) A/D Converter Start Request Flag	0: No compare match of GTADTRB at down-counting occurred 1: A compare match of GTADTRB at down-counting occurred.	R/(W)*1
b23 to b20	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b24	ODF	Output Disable Flag	0: No output disable request occurred 1: Output disable request occurred.	R
b27 to b25	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b28	DTEF	Dead Time Error Flag	0: No dead time error occurred 1: Dead time error occurred.	R
b29	OABHF	Same Time Output Level High Flag	0: GTIOCA pin and GTIOCB pin did not output 1 at the same time 1: GTIOCA pin and GTIOCB pin output 1 at the same time.	R
b30	OABLF	Same Time Output Level Low Flag	0: GTIOCA pin and GTIOCB pin did not output 0 at the same time 1: GTIOCA pin and GTIOCB pin output 0 at the same time.	R
b31	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Note 1. Only 0 can be written to this bit. Do not write 1.

The GTST register indicates the status of the GPT.

TCFA flag (Input Capture/Compare Match Flag A)

The TCFS flag indicates the status for the input capture or compare match of GTCCRA.

[Setting conditions]

- GTCNT = GTCCRA when the GTCCRA register functions as a compare match register
- GTCNT counter value is transferred to GTCCRA by the input capture signal when the GTCCRA register functions as an input capture register.

[Clearing condition]

- 0 is written to this flag.

TCFB flag (Input Capture/Compare Match Flag B)

The TCFB flag indicates the status for the input capture or compare match of GTCCRB.

[Setting conditions]

- GTCNT = GTCCRB when the GTCCRB register functions as a compare match register
- GTCNT counter value is transferred to GTCCRB by the input capture signal when the GTCCRB register function as an input capture register.

[Clearing condition]

- 0 is written to this flag.

TCFC flag (Input Compare Match Flag C)

The TCFC flag indicates the status for the compare match of GTCCRC.

[Setting condition]

- GTCNT = GTCCRC

[Clearing condition]

- 0 is written to this flag.

[Not comparing condition]

Bit	Symbol	位名称	Description	R/W
b18	ADTRBUF	GTADTRB比较匹配（向上计数）AD转换器启动请求标志	0：在递增计数时没有发生GTADTRB的比较匹配1：在递增计数时发生了GTADTRB的比较匹配。	R/(W)*1
b19	ADTRBDF	GTADTRB比较匹配（递减计数）AD转换器启动请求标志	0：在向下计数时没有发生GTADTRB的比较匹配1：在向下计数时发生了GTADTRB的比较匹配。	R/(W)*1
b23 to b20	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b24	ODF	输出禁用标志	0：未发生输出禁止请求1：发生输出禁止请求。	R
b27 to b25	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b28	DTEF	死区错误标志	0：未发生死区错误1：发生死区错误。	R
b29	OABHF	同时输出电平高Flag	0：GTIOCA引脚和GTIOCB引脚不同时输出11：GTIOCA引脚和GTIOCB引脚同时输出1。	R
b30	OABLF	同时输出电平低Flag	0：GTIOCA引脚和GTIOCB引脚不同时输出01：GTIOCA引脚和GTIOCB引脚同时输出0。	R
b31	—	Reserved	该位读取为0。写入值应为0。	R/W

Note 1. 该位只能写入0。不要写1。

GTST寄存器指示GPT的状态。

TCFA标志（输入捕捉比较匹配标志A）

TCFS标志指示GTCCRA的输入捕获或比较匹配的状态。

[Setting conditions]

- 当GTCCRA寄存器用作比较匹配寄存器时GTCNT=GTCCRA
- 当GTCCRA寄存器用作输入捕捉寄存器时，GTCNT计数器值通过输入捕捉信号传送到GTCCRA。

[Clearing condition]

- 0写入该标志。

TCFB标志（输入捕捉比较匹配标志B）

TCFB标志指示GTCCRB的输入捕获或比较匹配的状态。

[Setting conditions]

- 当GTCCRB寄存器用作比较匹配寄存器时GTCNT=GTCCRB
- 当GTCCRB寄存器用作输入捕捉寄存器时，GTCNT计数器值通过输入捕捉信号传送到GTCCRB。

[Clearing condition]

- 0写入该标志。

TCFC标志（输入比较匹配标志C）

TCFC标志指示GTCCRC比较匹配的状态。

[Setting condition]

- GTCNT = GTCCRC

[Clearing condition]

- 0写入该标志。

[Not comparing condition]

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)
- GTBER.CCRA[1:0] = 01b, 10b, 11b (GTCCRC performs buffer operation).

TCFD flag (Input Compare Match Flag D)

The TCFD flag indicates the status for the compare match of GTCCRD.

[Setting condition]

- GTCNT = GTCCRD

[Clearing condition]

- 0 is written to this flag.

[Not comparing condition]

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)
- GTBER.CCRA[1:0] = 10b, 11b (GTCCRD performs buffer operation).

TCFE flag (Input Compare Match Flag E)

The TCFE flag indicates the status for the compare match of GTCCRE.

[Setting condition]

- GTCNT = GTCCRE

[Clearing condition]

- 0 is written to this flag.

[Not comparing condition]

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)
- GTBER.CCRB[1:0] = 01b, 10b, 11b (GTCCRE performs buffer operation).

TCFF flag (Input Compare Match Flag F)

The TCFF flag indicates the status for the compare match of GTCCRF.

[Setting condition]

- GTCNT = GTCCRF

[Clearing condition]

- 0 is written to this flag.

[Not comparing condition]

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)
- GTBER.CCRB[1:0] = 10b, 11b (GTCCRF performs buffer operation).

TCFPO flag (Overflow Flag)

The TCFPO flag indicates when an overflow or a crest has occurred.

[Setting conditions]

- In saw-wave mode, an overflow (GTCNT changes from GTPR to 0 in up-counting) has occurred
- In triangle-wave mode, a crest (GTCNT changes from GTPR to GTPR-1) has occurred

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)
- GTBER.CCRA[1:0]=01b 10b 11b（GTCCRC执行缓冲操作）。

TCFD标志（输入比较匹配标志D）

TCFD标志指示GTCCRD比较匹配的状态。

[Setting condition]

- GTCNT = GTCCRD

[Clearing condition]

- 0写入该标志。

[Not comparing condition]

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)
- GTBER.CCRA[1:0]=10b 11b（GTCCRD执行缓冲操作）。

TCFE标志（输入比较匹配标志E）

TCFE标志指示GTCCRE比较匹配的状态。

[Setting condition]

- GTCNT = GTCCRE

[Clearing condition]

- 0写入该标志。

[Not comparing condition]

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)
- GTBER.CCRB[1:0]=01b 10b 11b（GTCCRE执行缓冲操作）。

TCFF标志（输入比较匹配标志F）

TCFF标志表示GTCCRF比较匹配的状态。

[Setting condition]

- GTCNT = GTCCRF

[Clearing condition]

- 0写入该标志。

[Not comparing condition]

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)
- GTBER.CCRB[1:0]=10b 11b（GTCCRF执行缓冲操作）。

TCFPO标志（溢出标志）

TCFPO标志指示何时发生溢出或波峰。

[Setting conditions]

- 在锯齿波模式下，发生了溢出（GTCNT在递增计数中从GTPR变为0）
- 在三角波模式下，出现波峰（GTCNT从GTPR变为GTPR-1）

- In counting by hardware sources, an overflow (GTCNT changes from GTPR to 0 in up-counting) has occurred.

[Clearing condition]

- 0 is written to this flag.

TCFPU flag (Underflow Flag)

The TCFPU flag indicates when an underflow or a trough has occurred.

[Setting conditions]

- In saw-wave mode, an underflow (GTCNT changes from 0 to GTPR in down-counting) has occurred
- In triangle-wave mode, a trough (GTCNT changes from 0 to 1) has occurred
- In counting by hardware sources, an underflow (GTCNT changes from 0 to GTPR in down-counting) has occurred.

[Clearing condition]

- 0 is written to this flag.

ITCNT[2:0] bits (GPTn_OVF/GPTn_UDF Interrupt Skipping Count Counter)

When the GPTn_OVF/GPTn_UDF (n = 0 to 7) interrupt skipping function is used (the GTITC.IVTC[1:0] bits are set to a value other than 00b), the counter in the ITCNT[2:0] bits increments by 1 every time the GPTn_OVF/GPTn_UDF interrupt source that is selected in GTITC.IVTC[1:0] is generated.

Only GPT32EH and GPT32E have these bits. GPT32 does not have these bits.

[Clearing conditions]

- The GPTn_OVF/GPTn_UDF interrupt skipping function is not used (GTITC.IVTT[2:0] is 000b when GTITC.IVTC[1:0] is 00b)
- The GPTn_OVF/GPTn_UDF interrupt skipping count matches the specified count (ITCNT[2:0] matches the skipping count specified in GTITC.IVTT[2:0]).

TUCF flag (Count Direction Flag)

The TUCF flag indicates the count direction of GTCNT. In event count operation, this flag is set to 1 in up-counting and is set to 0 in down-counting.

ADTRAUF flag (GTADTRA Compare Match (Up-Counting) A/D Converter Start Request Flag)

The ADTRAUF is a status flag for the compare match of GTADTRA at up-counting.

[Setting condition]

- GTCNT = GTADTRA at up-counting.

[Clearing condition]

- 0 is written to this bit.

ADTRADF flag (GTADTRA Compare Match (Down-Counting) A/D Converter Start Request Flag)

The ADTRADF is a status flag for the compare match of GTADTRA at down-counting.

[Setting condition]

- GTCNT = GTADTRA at down-counting.

[Clearing condition]

- 0 is written to this bit.

ADTRBUF flag (GTADTRB Compare Match (Up-Counting) A/D Converter Start Request Flag)

The ADTRBUF is a status flag for the compare match of GTADTRB at up-counting.

[Setting condition]

- GTCNT = GTADTRB at up-counting.

- 在硬件源的计数中，发生了溢出（GTCNT在递增计数中从GTPR变为0）。

[Clearing condition]

- 0写入该标志。

TCFPU flag (Underflow Flag)

TCFPU标志指示何时发生下溢或波谷。

[Setting conditions]

- 在锯齿波模式下，发生下溢（向下计数时GTCNT从0变为GTPR）
- 在三角波模式下，出现了一个波谷（GTCNT从0变为1）
- 在硬件源的计数中，发生了下溢（向下计数时GTCNT从0变为GTPR）。

[Clearing condition]

- 0写入该标志。

ITCNT[2:0]位（GPTn_OVFGPTn_UDF中断跳过计数计数器）

当使用GPTn_OVFGPTn_UDF(n=0to7)中断跳过功能时（GTITC.IVTC[1:0]位设置为00b以外的值），ITCNT[2:0]位中的计数器递增每次在GTITC.IVTC[1:0]中选择的GPTn_OVFGPTn_UDF中断源产生时为1。

只有GPT32EH和GPT32E有这些位。GPT32没有这些位。

[Clearing conditions]

- 不使用GPTn_OVFGPTn_UDF中断跳过功能（GTITC.IVTT[2:0]为000b时GTITC.IVTC[1:0] is 00b)
- GPTn_OVFGPTn_UDF中断跳过计数与指定计数匹配（ITCNT[2:0]与GTITC.IVTT[2:0]中指定的跳过计数匹配）。

TUCF标志（计数方向标志）

TUCF标志表示GTCNT的计数方向。在事件计数操作中，该标志在向上计数时设置为1，在向下计数时设置为0。

ADTRAUF标志（GTADTRA比较匹配（向上计数）AD转换器启动请求标志）

ADTRAUF是向上计数时GTADTRA比较匹配的状态标志。

[Setting condition]

- GTCNT = GTADTRA at up-counting.

[Clearing condition]

- 0写入该位。

ADTRADF标志（GTADTRA比较匹配（递减计数）AD转换器启动请求标志）

ADTRADF是向下计数时GTADTRA比较匹配的状态标志。

[Setting condition]

- GTCNT = GTADTRA at down-counting.

[Clearing condition]

- 0写入该位。

ADTRBUF标志（GTADTRB比较匹配（向上计数）AD转换器启动请求标志）

ADTRBUF是在递增计数时GTADTRB比较匹配的状态标志。

[Setting condition]

- GTCNT = GTADTRB at up-counting.

[Clearing condition]

- 0 is written to this bit.

ADTRBDF flag (GTADTRB Compare Match (Down-Counting) A/D Converter Start Request Flag)

The ADTRBDF is a status flag for the compare match of GTADTRB at down-counting.

[Setting condition]

- GTCNT = GTADTRB at down-counting.

[Clearing condition]

- 0 is written to this bit.

ODF flag (Output Disable Flag)

The ODF flag shows the request of the output disable source group that is selected in the GRP[1:0] bits. When output is disabled, an output disable control is not released within the same cycle in which an output disable request is negated. It is released in the next cycle.

DTEF flag (Dead Time Error Flag)

The DTEF flag indicates that the timer output toggle point after the automatic addition of dead time has exceeded the timer cycle.

DTEF returns to 0 when the timer output toggle point after the automatic addition of dead time is back within the cycle. DTEF is read only. Writing 0 to clear the flag is not allowed.

[Setting condition]

- The timer output toggle point after the automatic addition of dead time has exceeded the timer cycle.
  For triangle wave in up-counting: GTCCRA - GTDVU ≤ 0
  For triangle wave in down-counting: GTCCRA - GTDVD < 0
  For saw-wave one-shot pulse mode in up-counting:
  GTCCRA - GTDVU < 0 or GTCCRA + GTDVD > GTPR
  For saw-wave one-shot pulse mode in down-counting:
  GTCCRA + GTDVU > GTPR or GTCCRA - GTDVD < 0

[Clearing condition]

- The timer output toggle point after the automatic addition of dead time is within the timer cycle.
  Only GPT32EH and GPT32E have this flag. GPT32 does not have this flag.
  GPT32 has the automatic dead time setting function but it does not generate dead time error.

OABHF flag (Same Time Output Level High Flag)

The OABHF flag indicates that the GTIOCA pin and the GTIOCB pin output 1 at the same time.

When the GTIOCA pin or GTIOCB pin outputs 0, OABHF returns to 0. OABHF is read only. Writing 0 to clear the flag is not allowed. When an interrupt by the OABHF flag is enabled (GTINTAD.GRPABH = 1), the OABHF flag is output to the POEG as an output disable request.

[Setting condition]

- GTIOCA pin and GTIOCB pin output 1 at the same time when both the OAE and OBE bits are set to 1.

[Clearing conditions]

- GTIOCA pin output value is different from GTIOCB pin output value when both the OAE and OBE bits are set to 1
- GTIOCA pin and GTIOCB pin output 0 at the same time when both the OAE and OBE bits are set to 1
- Either the OAE bit or OBE bit is set to 0.

OABLF flag (Same Time Output Level Low Flag)

The OABLF flag indicates that the GTIOCA pin and the GTIOCB pin output 0 at the same time.

When the GTIOCA pin or GTIOCB pin outputs 1, OABLF returns to 0. OABLF is read only. Writing 0 to clear the flag

[Clearing condition]

- 0写入该位。

ADTRBDF标志（GTADTRB比较匹配（递减计数）AD转换器启动请求标志）

ADTRBDF是向下计数时GTADTRB比较匹配的状态标志。

[Setting condition]

- GTCNT = GTADTRB at down-counting.

[Clearing condition]

- 0写入该位。

ODF标志（输出禁用标志）

ODF标志显示在GRP[1:0]位中选择的输出禁用源组的请求。当输出禁用时，输出禁用控制不会在输出禁用请求被否定的同一周期内释放。它在下一个周期中发布。

DTEF标志（死区错误标志）

DTEF标志表示自动添加死区时间后的定时器输出切换点已超过定时器周期。

当自动添加死区时间后的定时器输出切换点回到循环内时，DTEF将返回0。
DTEF是只读的。不允许写入0来清除标志。

[Setting condition]

- 自动添加死区时间后的定时器输出切换点已超过定时器周期。
  对于递增计数中的三角波：GTCCRAGTDVU≤0
  对于向下计数中的三角波：GTCCRAGTDVD<0对于向上计数中的锯波单次脉冲模式：
  GTCCRAGTDVU<0或GTCCRA+GTDVD>GTPR对于向下计数中的锯波单次脉冲模式：
  GTCCRA + GTDVU > GTPR or GTCCRA - GTDVD < 0

[Clearing condition]

- 自动添加死区时间后的定时器输出切换点在定时器周期内。
  只有GPT32EH和GPT32E有这个标志。GPT32没有这个标志。
  GPT32具有自动死区时间设置功能，但不会产生死区时间错误。

OABHF标志（同时输出电平高标志）

OABHF标志表示GTIOCA引脚和GTIOCB引脚同时输出1。

当GTIOCA引脚或GTIOCB引脚输出0时，OABHF返回0。OABHF为只读。不允许写入0来清除标志。当启用OABHF标志的中断时(GTINTAD.GRPABH=1)，OABHF标志作为输出禁用请求输出到POEG。

[Setting condition]

- 当OAE和OBE位都设置为1时，GTIOCA引脚和GTIOCB引脚同时输出1。

[Clearing conditions]

- 当OAE和OBE位都设置为1时，GTIOCA引脚输出值与GTIOCB引脚输出值不同
- 当OAE和OBE位都设置为1时，GTIOCA引脚和GTIOCB引脚同时输出0
- OAE位或OBE位设置为0。

OABLF标志（同时输出电平低标志）

OABLF标志表示GTIOCA引脚和GTIOCB引脚同时输出0。

当GTIOCA引脚或GTIOCB引脚输出1时，OABLF返回0。OABLF为只读。写入0清除标志

is not allowed. When an interrupt by the OABLF flag is enabled (GTINTAD.GRPABL = 1), the OABLF flag is output to the POEG as an output disable request.

[Setting condition]

- GTIOCA pin and GTIOCB pin output 0 at the same time when both the OAE and OBE bits are set to 1.

[Clearing conditions]

- GTIOCA pin output value is different from GTIOCB pin output value when both the OAE and OBE bits are set to 1
- GTIOCA pin and GTIOCB pin output 1 at the same time when both the OAE and OBE bits are set to 1
- Either the OAE bit or OBE bit is set to 0.

The compare-target signals to generate the OABHF/OABLF flags are the compare match outputs (PWM outputs) signals before they are masked by the output disable function. When the output disable state is active, a compare match is performed continuously in the GPT and the OABHF/OABLF flags are updated according to with the result of the compared values.

23.2.17 General PWM Timer Buffer Enable Register (GTBER)

Address(es): GPT32EHm.GTBER 4007 8040h + 0100h × m (m = 0 to 3)
GPT32Em.GTBER 4007 8040h + 0100h × m (m = 4 to 7)
GPT32m.GTBER 4007 8040h + 0100h × m (m = 8 to 13)

- GPT32EH, GPT32E

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	ADTDB	ADTTB[1:0]		—	ADTDA	ADTTA[1:0]		—	CCRSWT	PR[1:0]		CCRB[1:0]		CCRA[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	BD[3]	BD[2]	BD[1]	BD[0]
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

- GPT32

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—		—	—	—		—	CCRSWT	PR[1:0]		CCRB[1:0]		CCRA[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	BD[1]	BD[0]
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	BD[0]	GTCCR Buffer Operation Disable	0: Enable buffer operation 1: Disable buffer operation.	R/W
b1	BD[1]	GTPR Buffer Operation Disable		R/W
b2	BD[2]	GTADTR Buffer Operation Disable		R/W
b3	BD[3]	GTDV Buffer Operation Disable		R/W
b15 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b17, b16	CCRA[1:0]	GTCCRA Buffer Operation	b17 b16 0 0: No buffer operation 0 1: Single buffer operation (GTCCRA ↔ GTCCRC) 1 x: Double buffer operation (GTCCRA ↔ GTCCRC ↔ GTCCRD).	R/W

不被允许。当启用OABLF标志的中断时（GTINTAD.GRPABL=1），OABLF标志作为输出禁用请求输出到POEG。

[Setting condition]

- 当OAE和OBE位都设置为1时，GTIOCA引脚和GTIOCB引脚同时输出0。

[Clearing conditions]

- 当OAE和OBE位都设置为1时，GTIOCA引脚输出值与GTIOCB引脚输出值不同
- 当OAE和OBE位都设置为1时，GTIOCA引脚和GTIOCB引脚同时输出1
- OAE位或OBE位设置为0。

生成OABHFOABLF标志的比较目标信号是比较匹配输出（PWM输出）信号，在它们被输出禁用功能屏蔽之前。当输出禁用状态激活时，在GPT中连续执行比较匹配，并根据比较值的结果更新OABHFOABLF标志。

23.2.17 通用PWM定时器缓冲器使能寄存器(GTBER)

Address(es): GPT32EHm.GTBER 4007 8040h + 0100h × m (m = 0 to 3)
GPT32Em.GTBER 4007 8040h + 0100h × m (m = 4 to 7)
GPT32m.GTBER 4007 8040h + 0100h × m (m = 8 to 13)

- GPT32EH, GPT32E

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	ADTDB	ADTTB[1:0]		—	ADTDA	ADTTA[1:0]		—	CCRSWT	PR[1:0]		CCRB[1:0]		CCRA[1:0]	
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	BD[3]	BD[2]	BD[1]	BD[0]
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

- GPT32

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—		—	—	—		—	CCRSWT	PR[1:0]		CCRB[1:0]		CCRA[1:0]	
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	BD[1]	BD[0]
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	BD[0]	GTCCR缓冲区操作禁用	0：启用缓冲操作1：禁用缓冲操作。	R/W
b1	BD[1]	GTPR缓冲区操作禁用		R/W
b2	BD[2]	GTADTR缓冲区操作禁用		R/W
b3	BD[3]	GTDV缓冲区操作禁用		R/W
b15 to b4	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b17, b16	CCRA[1:0]	GTCCRA缓冲区操作	b17b1600：无缓存操作01：单缓存操作（GTCCRA↔GTCCRC）1x：双缓存操作（GTCCRA↔GTCCRC↔GTCCRD）。	R/W

Bit	Symbol	Bit name	Description	R/W
b19, b18	CCRB[1:0]	GTCCRB Buffer Operation	b19 b18 0 0: No buffer operation 0 1: Single buffer operation (GTCCRB ↔ GTCCRE) 1 x: Double buffer operation (GTCCRB ↔ GTCCRE ↔ GTCCRF).	R/W
b21, b20	PR[1:0]	GTPR Buffer Operation	b21 b20 0 0: No buffer operation 0 1: Single buffer operation (GTPBR → GTPR) 1 x: Double buffer operation (GTPDBR → GTPBR → GTPR).	R/W
b22	CCRSWT	GTCCRA and GTCCRB Forcible Buffer Operation	Writing 1 to this bit forces a buffer transfer of GTCCRA and GTCCRB. This bit automatically returns to 0 after 1 is written. This bit is read as 0.	R/W
b23	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b25, b24	ADTTA[1:0]	GTADTRA Buffer Transfer Timing Select	• Triangle waves b25 b24 0 0: No transfer 0 1: Transfer at crest 1 0: Transfer at trough 1 1: Transfer at both crest and trough. • Saw waves b25 b24 0 0: No transfer Values other than 0 0: Transfer on underflow (during down-counting) or on overflow (during up-counting).	R/W
b26	ADTDA	GTADTRA Double Buffer Operation	0: Single buffer operation (GTADTBRA → GTADTRA) 1: Double buffer operation (GTADTDBRA → GTADTBRA → GTADTDRA).	R/W
b27	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b29, b28	ADTTB[1:0]	GTADTRB Buffer Transfer Timing Select	• Triangle waves b29 b28 0 0: No transfer 0 1: Transfer at crest 1 0: Transfer at trough 1 1: Transfer at both crest and trough. • Saw waves b29 b28 0 0: No transfer Values other than 0 0: Transfer on underflow (in down-counting) or on overflow (in up-counting).	R/W
b30	ADTDB	GTADTRB Double Buffer Operation	0: Single buffer operation (GTADTBRB → GTADTRB) 1: Double buffer operation (GTADTDBRB → GTADTBRB → GTADTDRB).	R/W
b31	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

The GTBER register provides settings for the buffer operation and must be set while the GTCNT operation is stopped.

BD[0] bit (GTCCR Buffer Operation Disable)

The BD[0] bit disables buffer operation using GTCCRA, GTCCRC, and GTCCRD combined and buffer operation using GTCCRB, GTCCRE, and GTCCRF combined.

When GTDTCR.TDE is 1, even if BD[0] is set to 0, GTCCRB does not perform buffer operation. The GTCCRB register is automatically set to a compare match value for a negative-phase waveform with dead time.

BD[1] bit (GTPR Buffer Operation Disable)

The BD[1] bit disables buffer operation using GTPR, GTPBR, and GTPDBR combined.

BD[2] bit (GTADTR Buffer Operation Disable)

The BD[2] bit disables buffer operation using GTADTRA, GTADTBRA, and GTADTDBRA combined and buffer operation using GTADTRB, GTADTBRB, and GTADTDBRB combined. In event count operation, this bit is not available and the GTADTR buffer operation is not performed. Only GPT32EH and GPT32E have this bit. GPT32 does

Bit	Symbol	位名称	Description	R/W
b19, b18	CCRB[1:0]	GTCCRB缓冲区操作	b19b1800：无缓冲操作01：单缓冲操作（GTCCRB↔GTCCRE）1x：双缓冲操作（GTCCRB↔GTCCRE↔GTCCRF）。	R/W
b21, b20	PR[1:0]	GTPR缓冲区操作	b21b2000：无缓冲操作01：单缓冲操作（GTPBR→GTPR）1x：双缓冲操作（GTPDBR→GTPBR→GTPR）。	R/W
b22	CCRSWT	GTCCRA和GTCCRB强制缓冲操作	向该位写入1会强制GTCCRA和GTCCRB进行缓冲区传输。该位在写入1后自动返回0。该位读为0。	R/W
b23	—	Reserved	该位读取为0。写入值应为0。	R/W
b25, b24	ADTTA[1:0]	GTADTRA缓冲区传输时序Select	三角波b25b2400：无转移01：在波峰转移10：在波谷转移11：在波峰和波谷转移。 锯齿波b25b2400：无传输0以外的值0：在下溢（向下计数期间）或在溢出时（向上计数期间）传输。	R/W
b26	ADTDA	GTADTRA双缓冲操作	0：单缓冲操作（GTADTBRA→GTADTRA）1：双缓冲操作（GTADTBRA→GTADTBRA→GTADTDRA）。	R/W
b27	—	Reserved	该位读取为0。写入值应为0。	R/W
b29, b28	ADTTB[1:0]	GTADTRB缓冲区传输时序Select	三角波b29b2800：无转移01：在波峰转移10：在波谷转移11：在波峰和波谷转移。 锯齿波b29b2800：不传输0以外的值0：在下溢（向下计数）或溢出（向上计数）时传输。	R/W
b30	ADTDB	GTADTRB双缓冲操作	0：单缓冲操作（GTADTBRB→GTADTRB）1：双缓冲操作（GTADTDBRB→GTADTBRB→GTADTDRB）。	R/W
b31	—	Reserved	该位读取为0。写入值应为0。	R/W

GTBER寄存器为缓冲操作提供设置，并且必须在GTCNT操作停止时设置。

BD[0]位（GTCCR缓冲区操作禁用）

BD[0]位禁用使用GTCCRA、GTCCRC和GTCCRD组合的缓冲区操作以及使用GTCCRB、GTCCRE和GTCCRF相结合。

当GTDTCR.TDE为1时，即使BD[0]设置为0，GTCCRB也不进行缓冲操作。GTCCRB寄存器自动设置为具有死区时间的负相位波形的比较匹配值。

BD[1]位（GTPR缓冲区操作禁用）

BD[1]位禁用使用GTPR、GTPBR和GTPDBR组合的缓冲区操作。

BD[2]位（GTADTR缓冲区操作禁用）

BD[2]位禁用使用GTADTRA、GTADTBRA和GTADTBRA组合的缓冲区操作以及使用GTADTRB、GTADTBRB和GTADTDBRB组合的缓冲区操作。在事件计数操作中，该位不可用且不执行GTADTR缓冲区操作。只有GPT32EH和GPT32E有这个位。GPT32可以

not have this bit.

BD[3] bit (GTDV Buffer Operation Disable)

The BD[3] bit disables buffer operation using GTDVU and GTDBU combined and buffer operation using GTDVD and GTDBD combined.

When the GTDTCR.TDFER bit is set to 1, even if BD[3] is set to 0, buffer operation is not performed and the GTDVD value is set as a value of GTDVU automatically. In event count operation, this bit is not available and the GTDV buffer operation is not performed. Only GPT32EH and GPT32E have this bit. GPT32 does not have this bit.

CCRA[1:0] bits (GTCCRA Buffer Operation)

The CCRA[1:0] bits set buffer operation using GTCCRA, GTCCRC, and GTCCRD combined. When buffer operation is restricted by the operating mode set in GTCR, the GTCR setting is given priority.*1

CCRB[1:0] bits (GTCCRB Buffer Operation)

The CCRB[1:0] bits set buffer operation using GTCCRB, GTCCRE, and GTCCRF combined. When buffer operation is restricted by the operating mode set in GTCR, the GTCR setting is given priority.*1

PR[1:0] bits (GTPR Buffer Operation)

The PR[1:0] bits set buffer operation using GTPR, GTPBR, and GTPDBR combined. GPT32 does not have the PR[1] bit. Only single buffer operation setting by PR[0] bit is available for GPT32.

CCRSWT bit (GTCCRA and GTCCRB Forcible Buffer Operation)

Writing 1 to the CCRSWT bit forcibly performs a buffer transfer of GTCCRA and GTCCRB. This bit automatically returns to 0 after 1 is written. This bit is read as 0 and is only valid when counting is stopped with a compare match operation specified.

ADTTA[1:0] bits (GTADTRA Buffer Transfer Timing Select)

The ADTTA[1:0] bits set the transfer timing for buffer operation of GTADTRA, GTADTBRA, and GTADTDBRA. These bits are not available in event count operation. Only GPT32EH and GPT32E have these bits. GPT32 does not have these bits.

ADTDA bit (GTADTRA Double Buffer Operation)

The ADTDA bit sets buffer operation using GTADTRA, GTADTBRA, and GTADTDBRA combined. This bit is not available in event count operation. Only GPT32EH and GPT32E have this bit. GPT32 does not have this bit.

ADTTB[1:0] bits (GTADTRB Buffer Transfer Timing Select)

The ADTTB[1:0] bits set the transfer timing for buffer operation of GTADTRB, GTADTBRB, and GTADTDBRB. These bits are not available in event count operation. Only GPT32EH and GPT32E have these bits. GPT32 does not have these bits.

ADTDB bit (GTADTRB Double Buffer Operation)

The ADTDB bit sets buffer operation using GTADTRB, GTADTBRB, and GTADTDBRB combined. This bit is not available in event count operation. Only GPT32EH and GPT32E have this bit. GPT32 does not have this bit.

Note 1. The buffer operation mode is fixed in saw-wave one-shot pulse mode or triangle-wave PWM mode 3 (64-bit transfer at trough).

没有这个位。

BD[3]位（GTDV缓冲区操作禁用）

BD[3]位禁用使用GTDVU和GTDBU组合的缓冲区操作以及使用GTDVD和
GTDBD combined.

当GTDTCR.TDFER位设置为1时，即使BD[3]设置为0，也不执行缓冲操作，并且GTDVD值自动设置为GTDVU的值。在事件计数操作中，该位不可用且不执行GTDV缓冲区操作。只有GPT32EH和GPT32E有这个位。GPT32没有这个位。

CCRA[1:0]位（GTCCRA缓冲区操作）

CCRA[1:0]位使用GTCCRA、GTCCRC和GTCCRD组合设置缓冲区操作。当缓冲操作受到GTCR中设置的操作模式限制时，GTCR设置优先。*1

CCRB[1:0]位（GTCCRB缓冲区操作）

CCRB[1:0]位使用GTCCRB、GTCCRE和GTCCRF组合设置缓冲区操作。当缓冲操作受到GTCR中设置的操作模式限制时，GTCR设置优先。*1

PR[1:0]位（GTPR缓冲区操作）

PR[1:0]位设置使用GTPR、GTPBR和GTPDBR组合的缓冲区操作。GPT32没有PR[1]位。GPT32只能通过PR[0]位设置单个缓冲区操作。

CCRSWT位（GTCCRA和GTCCRB强制缓冲操作）

向CCRSWT位写入1强制执行GTCCRA和GTCCRB的缓冲区传输。该位在写入1后自动返回0。该位读为0，仅当计数停止并指定比较匹配操作时才有效。

ADTTA[1:0]位（GTADTRA缓冲区传输时序选择）

ADTTA[1:0]位设置GTADTRA、GTADTBRA和GTADTBRA的缓冲区操作的传输时序。
这些位在事件计数操作中不可用。只有GPT32EH和GPT32E有这些位。GPT32没有这些位。

ADTDA位（GTADTRA双缓冲器操作）

ADTDA位设置使用GTADTRA、GTADTBRA和GTADTBRA组合的缓冲区操作。该位在事件计数操作中不可用。
只有GPT32EH和GPT32E有这个位。GPT32没有这个位。

ADTTB[1:0]位（GTADTRB缓冲区传输时序选择）

ADTTB[1:0]位设置GTADTRB、GTADTBRB和GTADTDRBB的缓冲区操作的传输时序。
这些位在事件计数操作中不可用。只有GPT32EH和GPT32E有这些位。GPT32没有这些位。

ADTDB位（GTADTRB双缓冲操作）

ADTDB位使用GTADTRB、GTADTBRB和GTADTDRBB组合设置缓冲区操作。该位在事件计数操作中不可用。
只有GPT32EH和GPT32E有这个位。GPT32没有这个位。

注1.缓冲操作模式固定为锯齿波单次脉冲模式或三角波PWM模式3（64位低谷传输）。

23.2.18 General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register (GTITC)

Address(es): GPT32EHm.GTITC 4007 8044h + 0100h × m (m = 0 to 3)
GPT32Em.GTITC 4007 8044h + 0100h × m (m = 4 to 7)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	ADTBL	—	ADTAL	—	IVTT[2:0]			IVTC[1:0]		ITLF	ITLE	ITLD	ITLC	ITLB	ITLA
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	ITLA	GTCCRA Compare Match/Input Capture Interrupt Link	0: Do not link with GPTn_OVF/GPTn_UDF interrupt skipping function 1: Link with GPTn_OVF/GPTn_UDF interrupt skipping function.	R/W
b1	ITLB	GTCCRB Compare Match/Input Capture Interrupt Link	0: Do not link with GPTn_OVF/GPTn_UDF interrupt skipping function 1: Link with GPTn_OVF/GPTn_UDF interrupt skipping function.	R/W
b2	ITLC	GTCCRC Compare Match Interrupt Link	0: Do not link with GPTn_OVF/GPTn_UDF interrupt skipping function 1: Link with GPTn_OVF/GPTn_UDF interrupt skipping function.	R/W
b3	ITLD	GTCCRD Compare Match Interrupt Link	0: Do not link with GPTn_OVF/GPTn_UDF interrupt skipping function 1: Link with GPTn_OVF/GPTn_UDF interrupt skipping function.	R/W
b4	ITLE	GTCCRE Compare Match Interrupt Link	0: Do not link with GPTn_OVF/GPTn_UDF interrupt skipping function 1: Link with GPTn_OVF/GPTn_UDF interrupt skipping function.	R/W
b5	ITLF	GTCCRF Compare Match Interrupt Link	0: Do not link with GPTn_OVF/GPTn_UDF interrupt skipping function 1: Link with GPTn_OVF/GPTn_UDF interrupt skipping function.	R/W
b7, b6	IVTC[1:0]	GPTn_OVF/GPTn_UDF Interrupt Skipping Function Select	b7 b6 0 0: Do not perform skipping 0 1: Count and skip both overflow and underflow for saw waves and crest for triangle waves 1 0: Count and skip both overflow and underflow for saw waves and trough for triangle waves 1 1: Count and skip both overflow and underflow for saw waves and both crest and trough for triangle waves.	R/W
b10 to b8	IVTT[2:0]	GPTn_OVF/GPTn_UDF Interrupt Skipping Count Select	b10 b8 0 0 0: No skipping 0 0 1: Skipping count of 1 0 1 0: Skipping count of 2 0 1 1: Skipping count of 3 1 0 0: Skipping count of 4 1 0 1: Skipping count of 5 1 1 0: Skipping count of 6 1 1 1: Skipping count of 7.	R/W
b11	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

23.2.18 通用PWM定时器中断和AD转换器启动请求跳过设置寄存器(GTITC)

Address(es): GPT32EHm.GTITC 4007 8044h + 0100h × m (m = 0 to 3)
GPT32Em.GTITC 4007 8044h + 0100h × m (m = 4 to 7)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	ADTBL	—	ADTAL	—	IVTT[2:0]			IVTC[1:0]		ITLF	ITLE	ITLD	ITLC	ITLB	ITLA
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	ITLA	GTCCRA Compare Match/Input 捕获中断链接	0：不与GPTn_OVFGPTn_UDF中断跳过功能联动1：与GPTn_OVFGPTn_UDF中断跳过功能联动。	R/W
b1	ITLB	GTCCRB Compare Match/Input 捕获中断链接	0：不与GPTn_OVFGPTn_UDF中断跳过功能联动1：与GPTn_OVFGPTn_UDF中断跳过功能联动。	R/W
b2	ITLC	GTCCRC比较匹配中断 Link	0：不与GPTn_OVFGPTn_UDF中断跳过功能联动1：与GPTn_OVFGPTn_UDF中断跳过功能联动。	R/W
b3	ITLD	GTCCRD比较匹配中断 Link	0：不与GPTn_OVFGPTn_UDF中断跳过功能联动1：与GPTn_OVFGPTn_UDF中断跳过功能联动。	R/W
b4	ITLE	GTCCRE比较匹配中断 Link	0：不与GPTn_OVFGPTn_UDF中断跳过功能联动1：与GPTn_OVFGPTn_UDF中断跳过功能联动。	R/W
b5	ITLF	GTCCRF比较匹配中断 Link	0：不与GPTn_OVFGPTn_UDF中断跳过功能联动1：与GPTn_OVFGPTn_UDF中断跳过功能联动。	R/W
b7, b6	IVTC[1:0]	GPTn_OVF/GPTn_UDF Interrupt 跳过功能选择	b7b600：不执行跳过01：计数并跳过锯齿波的上溢和下溢以及三角波的波峰10：计数并跳过锯齿波的上溢和下溢以及三角波的波谷11：计数并跳过跳过锯齿波的上溢和下溢以及三角波的波峰和波谷。	R/W
b10 to b8	IVTT[2:0]	GPTn_OVF/GPTn_UDF Interrupt 跳过计数选择	b10b8000：不跳过001：跳过计数1010：跳过计数2011：跳过计数3100：跳过计数4101：跳过计数5110：跳过计数6111：跳过计数7。	R/W
b11	—	Reserved	该位读取为0。写入值应为0。	R/W

Bit	Symbol	Bit name	Description	R/W
b12	ADTAL	GTADTRA A/D Converter Start Request Link	0: Do not link with GPTn_OVF/GPTn_UDF interrupt skipping function 1: Link with GPTn_OVF/GPTn_UDF interrupt skipping function.	R/W
b13	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b14	ADTBL	GTADTRB A/D Converter Start Request Link	0: Do not link with GPTn_OVF/GPTn_UDF interrupt skipping function 1: Link with GPTn_OVF/GPTn_UDF interrupt skipping function.	R/W
b31 to b15	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The GTITC register sets the skipping function for the GTCNT counter overflow (GTPR compare match) interrupt (GPTn_OVF) and underflow interrupt (GPTn_UDF). It also specifies whether to link other interrupts and A/D converter start requests with the GPTn_OVF/GPTn_UDF interrupt skipping function. The output disable request to POEG cannot be linked with the GPTn_OVF/GPTn_UDF interrupt skipping function. This register is not available in event count operation. Only GPT32EH and GPT32E have this register. GPT32 does not have this register and it is read as 0.

ITLA bit (GTCCRA Compare Match/Input Capture Interrupt Link)

The ITLA bit specifies whether to link the GTCCRA compare match/input capture interrupt (GTCIA) with the GPTn_OVF/GPTn_UDF interrupt skipping function.

ITLB bit (GTCCRB Compare Match/Input Capture Interrupt Link)

The ITLB bit specifies whether to link the GTCCRB compare match/input capture interrupt (GTCIB) with the GPTn_OVF/GPTn_UDF interrupt skipping function.

ITLC bit (GTCCRC Compare Match Interrupt Link)

The ITLC bit specifies whether to link the GTCCRC compare match interrupt (GTCIC) with the GPTn_OVF/GPTn_UDF interrupt skipping function.

ITLD bit (GTCCRD Compare Match Interrupt Link)

The ITLD bit specifies whether to link the GTCCRD compare match interrupt (GTCID) with the GPTn_OVF/GPTn_UDF interrupt skipping function.

ITLE bit (GTCCRE Compare Match Interrupt Link)

The ITLE bit specifies whether to link the GTCCRE compare match interrupt (GTCIE) with the GPTn_OVF/GPTn_UDF interrupt skipping function.

ITLF bit (GTCCRF Compare Match Interrupt Link)

The ITLF bit specifies whether to link the GTCCRF compare match interrupt (GTCIF) with the GPTn_OVF/GPTn_UDF interrupt skipping function.

IVTC[1:0] bits (GPTn_OVF/GPTn_UDF Interrupt Skipping Function Select)

The IVTC[1:0] bits set the skipping function for the GTPR compare match (GTCNT overflow) interrupt (GPTn_OVF) and GTCNT counter underflow interrupt (GPTn_UDF).

IVTT[2:0] bits (GPTn_OVF/GPTn_UDF Interrupt Skipping Count Select)

The IVTT[2:0] bits set the skipping count for the GTPR compare match (GTCNT overflow) interrupt (GPTn_OVF) and GTCNT counter underflow interrupt (GPTn_UDF). When modifying the IVTT[2:0] bits, first set the IVTC[1:0] bits to 00b.

ADTAL bit (GTADTRA A/D Converter Start Request Link)

The ADTAL bit specifies whether to link the GTADTRA A/D converter start request with GPTn_OVF/GPTn_UDF interrupt skipping function.

Bit	Symbol	位名称	Description	R/W
b12	ADTAL	GTADTRAAD转换器启动请求链接	0：不与GPTn_OVFGPTn_UDF中断跳过功能联动1：与GPTn_OVFGPTn_UDF中断跳过功能联动。	R/W
b13	—	Reserved	该位读取为0。写入值应为0。	R/W
b14	ADTBL	GTADTRBAD转换器启动请求链接	0：不与GPTn_OVFGPTn_UDF中断跳过功能联动1：与GPTn_OVFGPTn_UDF中断跳过功能联动。	R/W
b31 to b15	—	Reserved	这些位被读取为0。写入值应为0。	R/W

GTITC寄存器设置GTCNT计数器溢出（GTPR比较匹配）中断（GPTn_OVF）和下溢中断（GPTn_UDF）的跳过功能。它还指定是否将其他中断和AD转换器启动请求与GPTn_OVFGPTn_UDF中断跳过功能联系起来。对POEG的输出禁用请求不能与GPTn_OVFGPTn_UDF中断跳过函数链接。该寄存器在事件计数操作中不可用。只有GPT32EH和GPT32E有这个寄存器。GPT32没有这个寄存器，读为0。

ITLA位（GTCCRA比较匹配输入捕捉中断链接）

ITLA位指定是否将GTCCRA比较匹配输入捕捉中断(GTCIA)与GPTn_OVFGPTn_UDF中断跳过函数。

ITLB位（GTCCRB比较匹配输入捕捉中断链接）

ITLB位指定是否将GTCCRB比较匹配输入捕捉中断(GTCIB)与GPTn_OVFGPTn_UDF中断跳过函数。

ITLC位（GTCCRC比较匹配中断链接）

ITLC位指定是否将GTCCRC比较匹配中断(GTCIC)与GPTn_OVFGPTn_UDF中断跳过函数。

ITLD位（GTCCRD比较匹配中断链接）

ITLD位指定是否将GTCCRD比较匹配中断(GTCID)与GPTn_OVFGPTn_UDF中断跳过函数。

ITLE位（GTCCRE比较匹配中断链接）

ITLE位指定是否将GTCCRE比较匹配中断(GTCIE)与GPTn_OVFGPTn_UDF中断跳过函数。

ITLF位（GTCCRF比较匹配中断链接）

ITLF位指定是否将GTCCRF比较匹配中断(GTCIF)与GPTn_OVFGPTn_UDF中断跳过功能链接。

IVTC[1:0]位（GPTn_OVFGPTn_UDF中断跳过功能选择）

IVTC[1:0]位设置GTPR比较匹配（GTCNT上溢）中断（GPTn_OVF）和GTCNT计数器下溢中断（GPTn_UDF）的跳过功能。

IVTT[2:0]位（GPTn_OVFGPTn_UDF中断跳过计数选择）

IVTT[2:0]位设置GTPR比较匹配（GTCNT上溢）中断（GPTn_OVF）和GTCNT计数器下溢中断（GPTn_UDF）的跳过计数。修改IVTT[2:0]位时，首先将IVTC[1:0]位设置为00b。

ADTAL位（GTADTRAAD转换器启动请求链接）

ADTAL位指定是否将GTADTRAAD转换器启动请求与GPTn_OVFGPTn_UDF中断跳过功能联系起来。

ADTBL bit (GTADTRB A/D Converter Start Request Link)

The ADTBL bit specifies whether to link the GTADTRB A/D converter start request with GPTn_OVF/GPTn_UDF interrupt skipping function.

23.2.19 General PWM Timer Counter (GTCNT)

Address(es): GPT32EHm.GTCNT 4007 8048h + 0100h × m (m = 0 to 3)
GPT32Em.GTCNT 4007 8048h + 0100h × m (m = 4 to 7)
GPT32m.GTCNT 4007 8048h + 0100h × m (m = 8 to 13)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

GTCNT is a 32-bit read/write counter and can only be written to after counting stops. GTCNT must be accessed in 32-bit units. Access in 8-bit/16-bit units is prohibited. GTCNT must be set within the range of 0 ≤ GTCNT ≤ GTPR.

23.2.20 General PWM Timer Compare Capture Register n (GTCCRn) (n = A to F)

Address(es): GPT32EHm.GTCCRA 4007 804Ch + 0100h × m (m = 0 to 3)
GPT32Em.GTCCRA 4007 804Ch + 0100h × m (m = 4 to 7)
GPT32m.GTCCRA 4007 804Ch + 0100h × m (m = 8 to 13)
GPT32EHm.GTCCRB 4007 8050h + 0100h × m (m = 0 to 3)
GPT32Em.GTCCRB 4007 8050h + 0100h × m (m = 4 to 7)
GPT32m.GTCCRB 4007 8050h + 0100h × m (m = 8 to 13)
GPT32EHm.GTCCRC 4007 8054h + 0100h × m (m = 0 to 3)
GPT32Em.GTCCRC 4007 8054h + 0100h × m (m = 4 to 7)
GPT32m.GTCCRC 4007 8054h + 0100h × m (m = 8 to 13)
GPT32EHm.GTCCRE 4007 8058h + 0100h × m (m = 0 to 3)
GPT32Em.GTCCRE 4007 8058h + 0100h × m (m = 4 to 7)
GPT32m.GTCCRE 4007 8058h + 0100h × m (m = 8 to 13)
GPT32EHm.GTCCRD 4007 805Ch + 0100h × m (m = 0 to 3)
GPT32Em.GTCCRD 4007 805Ch + 0100h × m (m = 4 to 7)
GPT32m.GTCCRD 4007 805Ch + 0100h × m (m = 8 to 13)
GPT32EHm.GTCCRF 4007 8060h + 0100h × m (m = 0 to 3)
GPT32Em.GTCCRF 4007 8060h + 0100h × m (m = 4 to 7)
GPT32m.GTCCRF 4007 8060h + 0100h × m (m = 8 to 13)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

GTCCRn registers are read/write registers.

GTCCRA and GTCCRB are registers used for both output compare and input capture.

GTCCRC and GTCCRE are compare match registers that can also function as buffer registers for GTCCRA and GTCCRB.

GTCCRD and GTCCRF are compare match registers that can also function as buffer registers for GTCCRC and GTCCRE (double-buffer registers for GTCCRA and GTCCRB).

ADTBL位（GTADTRBAD转换器启动请求链接）

ADTBL位指定是否将GTADTRBAD转换器启动请求与GPTn_OVFGPTn_UDF中断跳过功能链接。

23.2.19 通用PWM定时器计数器(GTCNT)

Address(es): GPT32EHm.GTCNT 4007 8048h + 0100h × m (m = 0 to 3)
GPT32Em.GTCNT 4007 8048h + 0100h × m (m = 4 to 7)
GPT32m.GTCNT 4007 8048h + 0100h × m (m = 8 to 13)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

GTCNT是一个32位读写计数器，只能在计数停止后写入。GTCNT必须以32位单元访问。禁止以8位16位为单位进行访问。GTCNT必须设置在0≤GTCNT≤GTPR的范围内。

23.2.20 通用PWM定时器比较捕捉寄存器n(GTCCRn)(n=AtoF)

Address(es): GPT32EHm.GTCCRA 4007 804Ch + 0100h × m (m = 0 to 3)
GPT32Em.GTCCRA 4007 804Ch + 0100h × m (m = 4 to 7)
GPT32m.GTCCRA 4007 804Ch + 0100h × m (m = 8 to 13)
GPT32EHm.GTCCRB 4007 8050h + 0100h × m (m = 0 to 3)
GPT32Em.GTCCRB 4007 8050h + 0100h × m (m = 4 to 7)
GPT32m.GTCCRB 4007 8050h + 0100h × m (m = 8 to 13)
GPT32EHm.GTCCRC 4007 8054h + 0100h × m (m = 0 to 3)
GPT32Em.GTCCRC 4007 8054h + 0100h × m (m = 4 to 7)
GPT32m.GTCCRC 4007 8054h + 0100h × m (m = 8 to 13)
GPT32EHm.GTCCRE 4007 8058h + 0100h × m (m = 0 to 3)
GPT32Em.GTCCRE 4007 8058h + 0100h × m (m = 4 to 7)
GPT32m.GTCCRE 4007 8058h + 0100h × m (m = 8 to 13)
GPT32EHm.GTCCRD 4007 805Ch + 0100h × m (m = 0 to 3)
GPT32Em.GTCCRD 4007 805Ch + 0100h × m (m = 4 to 7)
GPT32m.GTCCRD 4007 805Ch + 0100h × m (m = 8 to 13)
GPT32EHm.GTCCRF 4007 8060h + 0100h × m (m = 0 to 3)
GPT32Em.GTCCRF 4007 8060h + 0100h × m (m = 4 to 7)
GPT32m.GTCCRF 4007 8060h + 0100h × m (m = 8 to 13)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

GTCCRn寄存器是读写寄存器。

GTCCRA和GTCCRB是用于输出比较和输入捕捉的寄存器。

GTCCRC和GTCCRE是比较匹配寄存器，也可以用作GTCCRA的缓冲寄存器和GTCCRB.

GTCCRD和GTCCRF是比较匹配寄存器，也可以用作GTCCRC的缓冲寄存器和GTCCRE（GTCCRA和GTCCRB的双缓冲寄存器）。

23.2.21 General PWM Timer Cycle Setting Register (GTPR)

Address(es): GPT32EHm.GTPR 4007 8064h + 0100h × m (m = 0 to 3)
GPT32Em.GTPR 4007 8064h + 0100h × m (m = 4 to 7)
GPT32m.GTPR 4007 8064h + 0100h × m (m = 8 to 13)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

GTPR is a read/write register that sets the maximum count value of GTCNT. For saw waves, the value of (GTPR + 1) is the cycle. For triangle waves, the value of (GTPR value × 2) is the cycle.

23.2.22 General PWM Timer Cycle Setting Buffer Register (GTPBR)

Address(es): GPT32EHm.GTPBR 4007 8068h + 0100h × m (m = 0 to 3)
GPT32Em.GTPBR 4007 8068h + 0100h × m (m = 4 to 7)
GPT32m.GTPBR 4007 8068h + 0100h × m (m = 8 to 13)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

GTPBR is a read/write register that functions as a buffer register for GTPR.

23.2.23 General PWM Timer Cycle Setting Double-Buffer Register (GTPDBR)

Address(es): GPT32EHm.GTPDBR 4007 806Ch + 0100h × m (m = 0 to 3)
GPT32Em.GTPDBR 4007 806Ch + 0100h × m (m = 4 to 7)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

GTPDBR is a 32-bit read/write register that functions as a buffer register for GTPBR (double-buffer register for GTPR). Only GPT32EH and GPT32E have this register. GPT32 does not have this register. This register is read with the value after reset.

23.2.21 通用PWM定时器周期设置寄存器(GTPR)

Address(es): GPT32EHm.GTPR 4007 8064h + 0100h × m (m = 0 to 3)
GPT32Em.GTPR 4007 8064h + 0100h × m (m = 4 to 7)
GPT32m.GTPR 4007 8064h + 0100h × m (m = 8 to 13)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

GTPR是一个读写寄存器，设置GTCNT的最大计数值。对于锯齿波，(GTPR+1)的值就是周期。对于三角波，（GTPR值 2）的值就是周期。

23.2.22 通用PWM定时器周期设置缓冲寄存器(GTPBR)

Address(es): GPT32EHm.GTPBR 4007 8068h + 0100h × m (m = 0 to 3)
GPT32Em.GTPBR 4007 8068h + 0100h × m (m = 4 to 7)
GPT32m.GTPBR 4007 8068h + 0100h × m (m = 8 to 13)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

GTPBR是一个读写寄存器，用作GTPR的缓冲寄存器。

23.2.23 通用PWM定时器周期设置双缓冲寄存器(GTPDBR)

Address(es): GPT32EHm.GTPDBR 4007 806Ch + 0100h × m (m = 0 to 3)
GPT32Em.GTPDBR 4007 806Ch + 0100h × m (m = 4 to 7)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

GTPDBR是一个32位读写寄存器，用作GTPBR的缓冲寄存器（GTPR的双缓冲寄存器）。
只有GPT32EH和GPT32E有这个寄存器。GPT32没有这个寄存器。用复位后的值读取该寄存器。

23.2.24 A/D Converter Start Request Timing Register n (GTADTRn) (n = A, B)

Address(es): GPT32EHm.GTADTRA 4007 8070h + 0100h × m (m = 0 to 3)
GPT32Em.GTADTRA 4007 8070h + 0100h × m (m = 4 to 7)

GPT32EHm.GTADTRB 4007 807Ch + 0100h × m (m = 0 to 3)
GPT32Em.GTADTRB 4007 807Ch + 0100h × m (m = 4 to 7)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

The GTADTRn registers are 32-bit read/write registers that set the timing of A/D converter start request generation. When the GTADTRn value matches the GTCNT counter value, an A/D converter start request is generated. GTADTRn must be accessed in 32-bit units. Access in 8-bit/16-bit units is prohibited. Only GPT32EH and GPT32E have this register. GPT32 does not have this register. This register is read with the value after reset.

23.2.25 A/D Converter Start Request Timing Buffer Register n (GTADTBRn) (n = A, B)

Address(es): GPT32EHm.GTADTBRA 4007 8074h + 0100h × m (m = 0 to 3)
GPT32Em.GTADTBRA 4007 8074h + 0100h × m (m = 4 to 7)

GPT32EHm.GTADTBRB 4007 8080h + 0100h × m (m = 0 to 3)
GPT32Em.GTADTBRB 4007 8080h + 0100h × m (m = 4 to 7)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

The GTADTBRn registers are 32-bit read/write registers that function as buffer registers for GTADTRn. GTADTBRn must be accessed in 32-bit units. Access in 8-bit/16-bit units is prohibited. Only GPT32EH and GPT32E have this register. GPT32 does not have this register. This register is read with the value after reset.

23.2.24 AD转换器启动请求时序寄存器n(GTADTRn)(n=A B)

Address(es): GPT32EHm.GTADTRA 4007 8070h + 0100h × m (m = 0 to 3)
GPT32Em.GTADTRA 4007 8070h + 0100h × m (m = 4 to 7)

GPT32EHm.GTADTRB 4007 807Ch + 0100h × m (m = 0 to 3)
GPT32Em.GTADTRB 4007 807Ch + 0100h × m (m = 4 to 7)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

GTADTRn寄存器是32位读写寄存器，用于设置AD转换器启动请求生成的时序。
当GTADTRn值与GTCNT计数器值匹配时，将产生AD转换器启动请求。GTADTRn必须以32位单元访问。禁止以8位16位为单位进行访问。只有GPT32EH和GPT32E有这个寄存器。GPT32没有这个寄存器。用复位后的值读取该寄存器。

23.2.25 AD转换器启动请求时序缓冲寄存器n(GTADTBRn)(n=A B)

Address(es): GPT32EHm.GTADTBRA 4007 8074h + 0100h × m (m = 0 to 3)
GPT32Em.GTADTBRA 4007 8074h + 0100h × m (m = 4 to 7)

GPT32EHm.GTADTBRB 4007 8080h + 0100h × m (m = 0 to 3)
GPT32Em.GTADTBRB 4007 8080h + 0100h × m (m = 4 to 7)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

GTADTRn寄存器是32位读写寄存器，用作GTADTRn的缓冲寄存器。GTADTBRn必须以32位单元访问。禁止以8位16位为单位进行访问。只有GPT32EH和GPT32E有这个寄存器。GPT32没有这个寄存器。用复位后的值读取该寄存器。

23.2.26 A/D Converter Start Request Timing Double-Buffer Register n (GTADTDBRn) (n = A, B)

Address(es): GPT32EHm.GTADTDBRA 4007 8078h + 0100h × m (m = 0 to 3)
GPT32Em.GTADTDBRA 4007 8078h + 0100h × m (m = 4 to 7)

GPT32EHm.GTADTDBRB 4007 8084h + 0100h × m (m = 0 to 3)
GPT32Em.GTADTDBRB 4007 8084h + 0100h × m (m = 4 to 7)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

The GTADTDBRn registers are 32-bit read/write registers that function as buffer registers for GTADTBRn (double-buffer registers for GTADTR). GTADTDBRn must be accessed in 32-bit units. Access in 8-bit/16-bit units is prohibited. Only GPT32EH and GPT32E have this register. GPT32 does not have this register. This register is read with the value after reset.

23.2.27 General PWM Timer Dead Time Control Register (GTDTCR)

Address(es): GPT32EHm.GTDTCR 4007 8088h + 0100h × m (m = 0 to 3)
GPT32Em.GTDTCR 4007 8088h + 0100h × m (m = 4 to 7)
GPT32m.GTDTCR 4007 8088h + 0100h × m (m = 8 to 13)

• GPT32EH, GPT32E

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	TDFER	—	—	TDBDE	TDBUE	—	—	—	TDE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

• GPT32

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TDE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	TDE	Negative-Phase Waveform Setting	0: Set GTCCRB without using GTDVU and GTDVD 1: Use GTDVU and GTDVD to set the compare match value for negative-phase waveform with dead time automatically in GTCCRB.	R/W
b3 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	TDBUE	GTDVU Buffer Operation Enable	0: Disable GTDVU buffer operation 1: Enable GTDVU buffer operation.	R/W

23.2.26 AD转换器启动请求时序双缓冲寄存器n(GTADTDBRn)(n=A B)

Address(es): GPT32EHm.GTADTDBRA 4007 8078h + 0100h × m (m = 0 to 3)
GPT32Em.GTADTDBRA 4007 8078h + 0100h × m (m = 4 to 7)

GPT32EHm.GTADTDBRB 4007 8084h + 0100h × m (m = 0 to 3)
GPT32Em.GTADTDBRB 4007 8084h + 0100h × m (m = 4 to 7)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

GTADTDBRn寄存器是32位读写寄存器，用作GTADTBRn的缓冲寄存器（GTADTR的双缓冲寄存器）。GTADTDBRn必须以32位单元访问。禁止以8位16位为单位进行访问。只有GPT32EH和GPT32E有这个寄存器。GPT32没有这个寄存器。用复位后的值读取该寄存器。

23.2.27 通用PWM定时器死区控制寄存器(GTDTCR)

Address(es): GPT32EHm.GTDTCR 4007 8088h + 0100h × m (m = 0 to 3)
GPT32Em.GTDTCR 4007 8088h + 0100h × m (m = 4 to 7)
GPT32m.GTDTCR 4007 8088h + 0100h × m (m = 8 to 13)

• GPT32EH, GPT32E

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	TDFER	—	—	TDBDE	TDBUE	—	—	—	TDE
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

• GPT32

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TDE
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	TDE	负相位波形设置	0：不使用GTDVU和GTDVD设置GTCCRB1：使用GTDVU和GTDVD在GTCCRB中自动设置带死区时间的负相波形的比较匹配值。	R/W
b3 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b4	TDBUE	GTDVU缓冲区操作使能	0：禁止GTDVU缓冲操作1：使能GTDVU缓冲操作。	R/W

Bit	Symbol	Bit name	Description	R/W
b5	TDBDE	GTDVD Buffer Operation Enable	0: Disable GTDVD buffer operation 1: Enable GTDVD buffer operation.	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	TDFER	GTDVD Setting	0: Set GTDVU and GTDVD separately 1: Automatically set the value written to GTDVU to GTDVD.	R/W
b31 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The GTDTCR register enables automatic setting of a compare match value for negative-phase waveform with dead time.

GPT32EH, GPT32E and GPT32 have dead time control function. GPT32 does not have the dead time buffer function and only GTDVU register is used for setting dead time value.

TDE bit (Negative-Phase Waveform Setting)

The TDE bit specifies whether to use GTDVU and GTDVD. When GTDVU and GTDVD are used, the compare match value for a negative-phase waveform with dead time obtained by the compare match value of a positive-phase waveform (GTCCRA) and the dead time value (GTDVU and GTDVD) is automatically set in GTCCRB.

The TDE bit setting is ignored in saw-wave PWM mode, and automatic setting does not take place.

The GTCCRB value is automatically set and has the following upper and lower limit values. If the obtained GTCCRB value is not within the upper or lower limit, the following limit value is set in GTCCRB and the GTST.DTEF flag is set to 1. However, in triangle waves, when the obtained GTCCRB value exceeds the upper limit value, the GTST.DTEF flag is set to 0.

- Triangle waves
  Upper limit value: GTPR – 1
  Lower limit value: 1 in up-counting, 0 in down-counting
- Saw-wave one-shot pulse mode
  Upper limit value: GTPR
  Lower limit value: 0.

TDBUE bit (GTDVU Buffer Operation Enable)

The TDBUE bit enables buffer operation with GTDVU and GTDBU combined. The buffer transfer timing is the trough for triangle waves, and an overflow or underflow for saw waves.

Only GPT32EH and GPT32E have this bit. GPT32 does not have this bit.

TDBDE bit (GTDVD Buffer Operation Enable)

The TDBDE bit enables buffer operation with GTDVD and GTDBD combined. The buffer transfer timing is the trough for triangle waves, and an overflow or underflow for saw waves. When this bit and the TDFER bit are set to 1 simultaneously, the TDFER bit setting is given priority.

Only GPT32EH and GPT32E have this bit. GPT32 does not have this bit.

TDFER bit (GTDVD Setting)

The TDFER bits selects whether or not the value written to GTDVU is also set to GTDVD automatically.

Only GPT32EH and GPT32E have this bit. GPT32 does not have this bit.

Bit	Symbol	位名称	Description	R/W
b5	TDBDE	GTDVD缓冲区操作使能	0：禁用GTDVD缓冲操作1：启用GT DVD缓冲操作。	R/W
b7, b6	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b8	TDFER	GTDVD Setting	0：分别设置GTDVU和GTDVD1：自动将写入GTDVU的值设置为GTDVD。	R/W
b31 to b9	—	Reserved	这些位被读取为0。写入值应为0。	R/W

GTDTCR寄存器可以自动设置带死区时间的负相波形的比较匹配值。

GPT32EH、GPT32E和GPT32具有死区时间控制功能。GPT32没有死区缓冲功能，只有GTDVU寄存器用于设置死区值。

TDE位（负相位波形设置）

TDE位指定是否使用GTDVU和GTDVD。使用GTDVU和GTDVD时，通过正相波形的比较匹配值(GTCCRA)和死区时间值(GTDVU和GTDVD)获得的带死区时间的负相波形的比较匹配值自动设置在GTCCRB.

TDE位设置在锯齿波PWM模式下被忽略，并且不会进行自动设置。

GTCCRB值是自动设置的，具有以下上下限值。如果获得的GTCCRB值不在上限或下限内，则在GTCCRB中设置以下限值并将GTST.DTEF标志设置为1。但是，在三角波中，当获得的GTCCRB值超过上限值时，GTST.DTEF标志设置为0。

- 三角波
  上限值：GTPR　1
  下限值：加1，减0
- 锯波单发脉冲模式
  上限值：GTPR
  下限值：0。

TDBUE位（GTDVU缓冲区操作使能）

TDBUE位使　　能结合GTDVU和GTDBU的缓冲器操作。缓冲传输时间是三角波的波谷，锯齿波的上溢或下溢。

只有GPT32EH和GPT32E有这个位。GPT32没有这个位。

TDBDE位（GTDVD缓冲区操作使能）

TDBDE位使能结合GTDVD和GTDBD的缓冲操作。缓冲传输时间是三角波的波谷，锯齿波的上溢或下溢。当该位和TDFER位同时设置为1时，TDFER位设置优先。

只有GPT32EH和GPT32E有这个位。GPT32没有这个位。

TDFER位（GTDVD设置）

TDFER位选择写入GTDVU的值是否也自动设置为GTDVD。

只有GPT32EH和GPT32E有这个位。GPT32没有这个位。

23.2.28 General PWM Timer Dead Time Value Register n (GTDVn) (n = U, D)

Address(es): GPT32EHm.GTDVU 4007 808Ch + 0100h x m (m = 0 to 3)
GPT32Em.GTDVU 4007 808Ch + 0100h x m (m = 4 to 7)
GPT32m.GTDVU 4007 808Ch + 0100h x m (m = 8 to 13)
GPT32EHm.GTDVD 4007 8090h + 0100h x m (m = 0 to 3)
GPT32Em.GTDVD 4007 8090h + 0100h x m (m = 4 to 7)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

GTDVn is a 32-bit read/write register that sets the dead time for generating PWM waveforms with dead time. GTDVU is used for up-counting and GTDVD is used for down-counting.

Setting a GTDVn value greater than or equal to GTPR is prohibited. Dead time setting beyond the cycle is prohibited. The compare match value set by the automatic dead time setting function for a negative waveform can be confirmed by reading from GTCCRB.

When GTDVn is used, writing to GTCCRB is not allowed. When this register is set to 0, waveforms without dead time are output. GTDVn must be accessed in 32-bit units. Access in 8-bit/16-bit units is prohibited. The way to rewrite GTDVn differs by GPT channel number.

GPT32EH0 to GPT32EH3 and GPT32E4 to GPT32E7

When GTDVn buffer operation is enabled, GTDBn can be written at anytime. GTDBn is transferred to GTDVn at the cycle end. When GTDVn buffer operation is disabled, stop the GPT using the CST bit in the GTCR register before changing GTDVn to a new value.

GPT328 to GPT3213

While the GPT is running, changing the GTDVU values is prohibited. To change GTDVU to a new value, stop the GPT with the CST bit in the GTCR register.

Only GPT32EH and GPT32E have the GTDVD register. GPT32 does not have the GTDVD register. This register is read with the value after reset.

23.2.29 General PWM Timer Dead Time Buffer Register n (GTDBn) (n = U, D)

Address(es): GPT32EHm.GTDBU 4007 8094h + 0100h × m (m = 0 to 3)
GPT32Em.GTDBU 4007 8094h + 0100h × m (m = 4 to 7)

GPT32EHm.GTDBD 4007 8098h + 0100h × m (m = 0 to 3)
GPT32Em.GTDBD 4007 8098h + 0100h × m (m = 4 to 7)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

GTDBn is a 32-bit read/write register that functions as a buffer register for GTDVn.

Only GPT32EH and GPT32E have this register. GPT32 does not have this register. This register is read with the value after reset.

23.2.28 通用PWM定时器死区值寄存器n(GTDVn)(n=U D)

Address(es): GPT32EHm.GTDVU 4007 808Ch + 0100h x m (m = 0 to 3)
GPT32Em.GTDVU 4007 808Ch + 0100h x m (m = 4 to 7)
GPT32m.GTDVU 4007 808Ch + 0100h x m (m = 8 to 13)
GPT32EHm.GTDVD 4007 8090h + 0100h x m (m = 0 to 3)
GPT32Em.GTDVD 4007 8090h + 0100h x m (m = 4 to 7)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

GTDVn是一个32位读写寄存器，用于设置死区时间，以生成带死区时间的PWM波形。GTDVU用于递增计数，GTDVD用于递减计数。

禁止将GTDVn值设置为大于或等于GTPR。禁止设置超出周期的死区时间。
通过读取GTCCRB可以确认负波形的自动死区时间设置功能设置的比较匹配值。

使用GTDVn时，不允许写入GTCCRB。当该寄存器设置为0时，输出无死区时间的波形。GTDVn必须以32位单元访问。禁止以8位16位为单位进行访问。重写GTDVn的方式因GPT通道号而异。

GPT32EH0到GPT32EH3和GPT32E4到GPT32E7

当GTDVn缓冲区操作使能时，可以随时写入GTDBn。GTDBn在循环结束时转移到GTDVn。当GTDVn缓冲操作被禁用时，在将GTDVn更改为新值之前，使用GTCR寄存器中的CST位停止GPT。

GPT328 to GPT3213

在GPT运行时，禁止更改GTDVU值。要将GTDVU更改为新值，请使用GTCR寄存器中的CST位停止GPT。

只有GPT32EH和GPT32E有GTDVD寄存器。GPT32没有GTDVD寄存器。用复位后的值读取该寄存器。

23.2.29 通用PWM定时器死区缓冲寄存器n(GTDBn)(n=U D)

Address(es): GPT32EHm.GTDBU 4007 8094h + 0100h × m (m = 0 to 3)
GPT32Em.GTDBU 4007 8094h + 0100h × m (m = 4 to 7)

GPT32EHm.GTDBD 4007 8098h + 0100h × m (m = 0 to 3)
GPT32Em.GTDBD 4007 8098h + 0100h × m (m = 4 to 7)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

GTDBn是一个32位读写寄存器，用作GTDVn的缓冲寄存器。

只有GPT32EH和GPT32E有这个寄存器。GPT32没有这个寄存器。用复位后的值读取该寄存器。

23.2.30 General PWM Timer Output Protection Function Status Register (GTSOS)

Address(es): GPT32EHm.GTSOS 4007 809Ch + 0100h x m (m = 0 to 3)
GPT32Em.GTSOS 4007 809Ch + 0100h × m (m = 4 to 7)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SOS[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	SOS[1:0]	Output Protection Function Status	b1 b0 0 0: Normal operation 0 1: Protected state (set GTCCRA = 0 during transfer at trough or crest) 1 0: Protected state (set GTCCRA ≥ GTPR during transfer at trough) 1 1: Protected state (set GTCCRA ≥ GTPR during transfer at crest).	R
b31 to b2	—	Reserved	These bits are read as 0. Writing to these bits is ignored.	R

GTSOS is a status register that indicates the status of the output protection function. The output protection function is enabled only when the dead time is automatically set (GTDTCR.TDE bit = 1) in triangle-wave mode.

Only GPT32EH and GPT32E have this register. GPT32 does not have this register. This register is read as 0000_0000h.

SOS[1:0] bits (Output Protection Function Status)

The SOS[1:0] bits indicate the status of the output protection function in triangle-wave PWM mode.

23.2.31 General PWM Timer Output Protection Function Temporary Release Register (GTSOTR)

Address(es): GPT32EHm.GTSOTR 4007 80A0h + 0100h x m (m = 0 to 3)
GPT32Em.GTSOTR 4007 80A0h + 0100h × m (m = 4 to 7)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SOTR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	SOTR	Output Protection Function Temporary Release	0: Do not release protected state 1: Release protected state.	R/W
b31 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The GTSOTR register temporarily releases the protected state of GTIOCB pin output when output protection is set. The protected state can be released only when GTSOS.SOS[1:0] bits = 10b (protected state in which GTCCRA ≥ GTPR has occurred during transfer at trough). The protected state cannot be released in any other case.

23.2.30 通用PWM定时器输出保护功能状态寄存器(GTSOS)

Address(es): GPT32EHm.GTSOS 4007 809Ch + 0100h x m (m = 0 to 3)
GPT32Em.GTSOS 4007 809Ch + 0100h × m (m = 4 to 7)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SOS[1:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b1, b0	SOS[1:0]	输出保护功能状态	b1b000：正常运行01：保护状态（在波谷或波峰转移期间设置GTCCRA=0）10：保护状态（在波谷转移期间设置GTCCRA≥GTPR）11：保护状态（在波谷或波峰转移期间设置GTCCRA≥GTPR）在波峰转移）。	R
b31 to b2	—	Reserved	这些位被读取为0。写入这些位被忽略。	R

GTSOS是一个状态寄存器，指示输出保护功能的状态。只有在三角波模式下自动设置死区时间（GTDTCR.TDE位=1）时，才会启用输出保护功能。

只有GPT32EH和GPT32E有这个寄存器。GPT32没有这个寄存器。该寄存器读为0000_0000h。

SOS[1:0]位（输出保护功能状态）

SOS[1:0]位指示三角波PWM模式下输出保护功能的状态。

23.2.31 通用PWM定时器输出保护功能临时释放寄存器(GTSOTR)

Address(es): GPT32EHm.GTSOTR 4007 80A0h + 0100h x m (m = 0 to 3)
GPT32Em.GTSOTR 4007 80A0h + 0100h × m (m = 4 to 7)

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SOTR
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	SOTR	输出保护功能 临时释放	0：不解除保护状态1：解除保护状态。	R/W
b31 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

当设置输出保护时，GTSOTR寄存器暂时解除GTIOCB引脚输出的保护状态。仅当GTSOS.SOS[1:0]位=10b时才能解除保护状态（在低谷传输期间发生GTCCRA≥GTPR的保护状态）。在任何其他情况下都不能释放受保护的状态。

Only GPT32EH and GPT32E have this register. GPT32 does not have this register. This register is read as 0000_0000h.

SOTR bit (Output Protection Function Temporary Release)

The SOTR bit specifies whether to temporarily release the protected state of the GTIOCB pin output in an output protected state. When the SOTR bit is set to 1, the output protection function is canceled from the first trough. When the SOTR bit is set to 0, output protection resumes from the first trough.

23.2.32 Output Phase Switching Control Register (OPSCR)

Address(es): GPT_OPS.OPSCR 4007 8FF0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	NFCS[1:0]		NFEN	—	—	GODF	GRP[1:0]		—	—	ALIGN	—	INV	N	P	FB
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	EN	—	W	V	U	—	WF	VF	UF
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	UF	Input Phase Soft Setting	These bits set the input phase from the software settings. Setting these bits is valid when the OPSCR.FB bit = 1.	R/W
b1	VF			R/W
b2	WF			R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	U	Input U-Phase Monitor	These bits monitor the state of the input phase: OPSCR.FB = 0: External input monitoring by PCLKD OPSCR.FB = 1: Software settings (UF/VF/WF).	R
b5	V	Input V-Phase Monitor		R
b6	W	Input W-Phase Monitor		R
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b8	EN	Enable-Phase Output Control	0: Do not output (Hi-Z on external pin) 1: Output.*1	R/W
b15 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b16	FB	External Feedback Signal Enable	This bit selects the input phase from the software settings or external input: 0: Select the external input 1: Select the software settings (OPSCR.UF, VF, WF).	R/W
b17	P	Positive-Phase Output (P) Control	0: Output level signal 1: Output PWM signal (PWM of GPT32EH0).	R/W
b18	N	Negative-Phase Output (N) Control	0: Output level signal 1: Output PWM signal (PWM of GPT32EH0).	R/W
b19	INV	Invert-Phase Output Control	0: Output positive logic (active-high) 1: Output negative logic (active-low).	R/W
b20	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b21	ALIGN	Input Phase Alignment	0: Align input phase to PCLKD 1: Align input phase to PWM.	R/W
b23, b22	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b25, b24	GRP[1:0]	Output Disabled Source Selection	b25 b24 0 0: Select Group A output disable source 0 1: Select Group B output disable source 1 0: Select Group C output disable source 1 1: Select Group D output disable source.	R/W
b26	GODF	Group Output Disable Function	0: Ignore this bit function 1: Clear the OPSCR.EN bit on group disable.*1	R/W
b28, b27	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

只有GPT32EH和GPT32E有这个寄存器。GPT32没有这个寄存器。该寄存器读为0000_0000h。

SOTR位（输出保护功能临时释放）

SOTR位指定是否在输出保护状态下暂时解除GTIOCB引脚输出的保护状态。当SOTR位设置为1时，输出保护功能从第一个波谷取消。当SOTR位设置为0时，输出保护从第一个波谷恢复。

23.2.32 输出相位切换控制寄存器(OPSCR)

Address(es): GPT_OPS.OPSCR 4007 8FF0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	NFCS[1:0]		NFEN	—	—	GODF	GRP[1:0]		—	—	ALIGN	—	INV	N	P	FB
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	EN	—	W	V	U	—	WF	VF	UF
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	UF	输入相位软设置	这些位通过软件设置设置输入相位。 当OPSCR.FB位=1时，设置这些位有效。	R/W
b1	VF			R/W
b2	WF			R/W
b3	—	Reserved	该位读取为0。写入值应为0。	R/W
b4	U	输入U相监视器	这些位监控输入相位的状态：OPSCR.FB=0：通过PCLKD监控外部输入 OPSCR.FB=1：软件设置（UFVFWF）。	R
b5	V	输入V相监视器		R
b6	W	输入W相监视器		R
b7	—	Reserved	该位读取为0。写入值应为0。	R/W
b8	EN	使能相输出控制	0：不输出（外部引脚上的Hi-Z）1： 输出。*1	R/W
b15 to b9	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b16	FB	外部反馈信号使能	该位从软件设置或外部输入中选择输入相位：0：选择外部输入1：选择软件设置（OPSCR.UF、VF、WF）。	R/W
b17	P	正相输出(P)控制	0：输出电平信号1：输出PWM信号（GPT32EH0的PWM）。	R/W
b18	N	负相输出(N)控制	0：输出电平信号1：输出PWM信号（GPT32EH0的PWM）。	R/W
b19	INV	反相输出控制	0：输出正逻辑（高电平有效）1：输 出负逻辑（低电平有效）。	R/W
b20	—	Reserved	该位读取为0。写入值应为0。	R/W
b21	ALIGN	输入相位对齐	0：将输入相位与PCLKD对齐1 ：将输入相位与PWM对齐。	R/W
b23, b22	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b25, b24	GRP[1:0]	输出禁用源选择	b25b2400：选择A组输出禁用源01：选择B 组输出禁用源10：选择C 组输出禁用源11： 选择D组输出禁用源。	R/W
b26	GODF	组输出禁用功能	0：忽略该位功能1：在组禁用时清除OPSCR.EN 位。*1	R/W
b28, b27	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Bit	Symbol	Bit name	Description	R/W
b29	NFEN	External Input Noise Filter Enable	0: Do not use a noise filter on the external input 1: Use a noise filter on the external input.	R/W
b31, b30	NFCS[1:0]	External Input Noise Filter Clock Selection	Noise filter sampling clock setting of the external input: b31 b30 0 0: PCLKD/1 0 1: PCLKD/4 1 0: PCLKD/16 1 1: PCLKD/64.	R/W

Note 1. When OPSCR.GODF = 1 and the signal value selected by the OPSCR.GRP bit is high, the OPSCR.EN bit is cleared to 0.

The OPSCR register sets the output of the signal waveform required for brushless DC motor control.

UF, VF, WF bits (Input Phase Soft Setting)

The UF, VF, and WF bits set the input phase from the software settings. When OPSCR.FB bit = 1, these bits are valid. The set value of the UF/VF/WF bits take the place of the U/V/W external inputs.

U, V, W bits (Input Phase Monitor)

When OPSCR.FB bit = 0, external inputs that are synchronized by PCLKD are monitored by the U, V, and W bits. When OPSCR.FB bit = 1, the OPSCR.U, OPSCR.V, and OPSCR.W bits can read the OPSCR.UF, OPSCR.VF, and OPSCR.WF bits.

EN bit (Enable-Phase Output Control)

The EN bit controls the output enable signal output phase (positive phase/reverse phase).

When OPSCR.EN bit = 1, the signal waveform is output.

When OPSCR.EN bit = 0, first set OPSCR.FB, OPSCR.UF/VF/WF (software setting is selected), OPSCR.P/N, OPSCR.INV, OPSCR.RV, OPSCR.ALIGN, OPSCR.GRP, OPSCR.GODF, OPSCR.NFEN, and OPSCR.NFCS. Then, set this bit to 1. Also, when OPSCR.GODF = 1 and the signal value selected by the OPSCR.GRP bit is high, the OPSCR.EN bit is cleared to 0.

FB bit (External Feedback Signal Enable)

The FB bit selects the input phase from the software settings (OPSCR.UF, VF, WF) and external input such as a Hall element.

P bit (Positive-Phase Output (P) Control)

The P bit selects the level signal output or PWM signal output for the positive-phase output (GTOUUP pin, GTOVUP pin, GTOWUP pin).

N bit (Negative-Phase Output (N) Control)

The N bit selects the level signal output or PWM signal output for the negative-phase output (GTOULO pin, GTOVLO pin, GTOWLO pin).

INV bit (Invert-Phase Output Control)

The INV bit selects either positive logic (active-high) output or negative logic (active-low) output for the output phase.

ALIGN bit (Input Phase Alignment)

The ALIGN bit selects PCLKD or PWM for the sampling of the input phase (input phase is specified in the OPSCR.FB bit).

When OPSCR.ALIGN bit = 0, input phase is aligned to PCLKD.

Note: When PWM output is selected (OPSCR.P/N = 1) and the PCLKD input phase is aligned, the PWM pulse might be short-pulsed.

Note: When OPSCR.ALIGN bit = 1, input phase is aligned with PWM output.

Bit	Symbol	位名称	Description	R/W
b29	NFEN	外部输入噪声滤波器启用	0：外部输入不使用噪声滤波器1：外部输入使用噪声滤波器。	R/W
b31, b30	NFCS[1:0]	外部输入噪声滤波器时钟Selection	外部输入的噪声滤波器采样时钟设置：b31b3000：PCLKD101：PCLKD410：PCLKD1611：PCLKD64。	R/W

Note 1. 当OPSCR.GODF=1且OPSCR.GRP位选择的信号值为高时，OPSCR.EN位清零。

OPSCR寄存器设置无刷直流电机控制所需的信号波形输出。

UF VF WF位（输入相位软设置）

UF、VF和WF位通过软件设置设置输入相位。当OPSCR.FB位=1时，这些位有效。
UFVFWF位的设定值代替了UVW外部输入。

U V W位（输入相位监视器）

当OPSCR.FB位=0时，由PCLKD同步的外部输入由U、V和W位监控。当OPSCR.FB位=1时，OPSCR.U、OPSCR.V和OPSCR.W位可以读取OPSCR.UF、OPSCR.VF和OPSCR.WF位。

EN位（使能相位输出控制）

EN位控制输出使能信号的输出相位（正相反相）。

当OPSCR.EN位=1时，输出信号波形。

当OPSCR.EN位=0时，首先设置OPSCR.FB、OPSCR.UFVFWF（选择软件设置）、OPSCR.PN、OPSCR.INV、OPSCR.RV、OPSCR.ALIGN、OPSCR.GRP、OPSCR.GODF、OPSCR.NFEN和OPSCR.NFCS。然后，将此位设置为1。此外，当OPSCR.GODF=1且OPSCR.GRP位选择的信号值为高时，OPSCR.EN位清零。

FB位（外部反馈信号使能）

FB位从软件设置（OPSCR.UF、VF、WF）和霍尔元件等外部输入中选择输入相位。

P位（正相输出（P）控制）

P位选择正相输出（GTOUUP引脚、GTOVUP引脚、GTOWUP引脚）的电平信号输出或PWM信号输出。

N位（负相输出（N）控制）

N位选择电平信号输出或负相输出（GTOULO引脚、GTOVLO引脚、GTOWLO引脚）的PWM信号输出。

INV位（反相输出控制）

INV位为输出相位选择正逻辑（高电平有效）输出或负逻辑（低电平有效）输出。

ALIGN位（输入相位对齐）

ALIGN位选择PCLKD或PWM对输入相位进行采样（输入相位在OPSCR.FB位中指定）。

当OPSCR.ALIGN位=0时，输入相位与PCLKD对齐。

Note: WhenPWMoutputisselected(OPSCR.PN=1)andthePCLKDinputphaseisaligned thePWMpulsemightbeshort-pulsed.

Note: 当OPSCR.ALIGN位=1时，输入相位与PWM输出对齐。

GRP[1:0] bits (Output Disabled Source Selection)

The GRP[1:0] bits select the output disable source (A to D).

GODF bit (Group Output Disable Function)

When the GODF bit = 1 and signal value selected by the OPSCR.GRP bit is high, the OPSCR.EN bit is cleared to 0.
When the GODF bit = 0, the bit is ignored.

NFEN bit (External Input Noise Filter Enable)

The NFEN bit selects the noise filter for external input.

When OPSCR.NFEN = 0, a noise filter is not used for the external input.

When OPSCR.NFEN = 1, a noise filter is used for the external input.

Note: When this bit is switched, because an unintentional internal edge occurs, first set the OPSCR.EN bit to 0.

NFCS[1:0] bits (External Input Noise Filter Clock Selection)

The NFCS[1:0] bits select the clock for the external input noise filter. When the OPSCR.NFEN bit = 1, noise filter sampling clock setting for external input is enabled.

Note: After setting the NFCS[1:0] bits, wait 2 cycles of the selected sampling clock, then set OPSCR.EN to 1.

23.3 Operation

23.3.1 Basic Operation

Each channel has a 32-bit timer that performs a periodic count operation using the count clock and hardware sources. The count function provides both up-counting and down-counting. The GTPR register controls the count cycle. When the GTCNT counter value matches the value in GTCCRA or GTCCRB, the output from the associated pin GTIOCA or GTIOCB can be changed. GTCCRA or GTCCRB can be used as an input capture register with hardware resources.

GTCCRC and GTCCRD can function as buffer registers for GTCCRA. GTCCRE and GTCCRF can function as buffer registers for GTCCRB.

23.3.1.1 Counter operation

(1) Counter start and stop

The counter of each channel starts the count operation when GTCR.CST is set to 1. The GTCR.CST bit value is changed by following sources:

- Writing to GTCR register
- Writing 1 to the bit in GTSTR associated with the GPT channel number when the GTSSR.CSTRT bit is set to 1
- Writing 1 to the bit in GTSTP associated with the GPT channel number when the GTPSR.CSTOP bit is set to 1
- The hardware source selected in the GTSSR register
- The hardware source selected in the GTPSR register.

(2) Periodic count operation in up-counting by count clock

The GTCNT counter in each channel starts up-counting when the associated GTCR.CST bit is set to 1 with the GTUPSR and GTDNSR registers set to 0000 0000h. When the GTCNT value changes from the GTPR value to 0 (overflow), the GTST.TCFPO flag is set to 1. When GTCNT overflows, up-counting resumes from 0000 0000h.

Figure 23.3 shows an example of a periodic count operation in up-counting.

GRP[1:0]位（输出禁用源选择）

GRP[1:0]位选择输出禁用源（A到D）。

GODF位（组输出禁用功能）

当GODF位=1且OPSCR.GRP位选择的信号值为高时，OPSCR.EN位清零。
当GODF位=0时，该位被忽略。

NFEN位（外部输入噪声滤波器使能）

NFEN位选择外部输入的噪声滤波器。

当OPSCR.NFEN=0时，外部输入不使用噪声滤波器。

当OPSCR.NFEN=1时，噪声滤波器用于外部输入。

Note: 切换该位时，由于出现意外的内部边沿，首先将OPSCR.EN位设置为0。

NFCS[1:0]位（外部输入噪声滤波器时钟选择）

NFCS[1:0]位选择外部输入噪声滤波器的时钟。当OPSCR.NFEN位=1时，外部输入的噪声滤波器采样时钟设置使能。

Note: 设置NFCS[1:0]位后，等待所选采样时钟的2个周期，然后将OPSCR.EN设置为1。

23.3 Operation

23.3.1 基本操作

每个通道都有一个32位定时器，它使用计数时钟和硬件源执行周期性计数操作。计数功能提供向上计数和向下计数。GTPR寄存器控制计数周期。当GTCNT计数器值与GTCCRA或GTCCRB中的值匹配时，可以更改相关引脚GTIOCA或GTIOCB的输出。GTCCRA或GTCCRB可用作具有硬件资源的输入捕捉寄存器。

GTCCRC和GTCCRD可以作为GTCCRA的缓冲寄存器。GTCCRE和GTCCRF可以作为GTCCRB的缓冲寄存器。

23.3.1.1 计数器操作

(1) 计数器启动和停止

当GTCR.CST设置为1时，每个通道的计数器开始计数操作。GTCR.CST位的值由以下来源改变：

- 写入GTCR寄存器
- 当GTSSR.CSTRT位设置为1时，将1写入GTSTR中与GPT通道号相关的位
- 当GTPSR.CSTOP位设置为1时，将1写入GTSTP中与GPT通道号相关联的位
- GTSSR寄存器中选择的硬件源
- 在GTPSR寄存器中选择的硬件源。

(2) 计数时钟递增计数中的周期计数操作

当相关的GTCR.CST位设置为1且GTUPSR和GTDNSR寄存器设置为00000000h时，每个通道中的GTCNT计数器开始向上计数。当GTCNT值从GTPR值变为0（溢出）时，GTST.TCFPO标志设置为1。当GTCNT溢出时，向上计数从00000000h恢复。

图23.3显示了递增计数中周期性计数操作的示例。

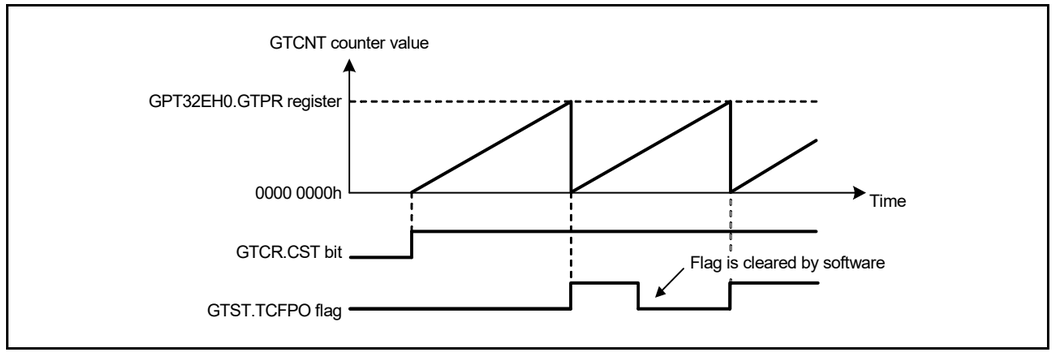


Figure 23.3 Example of periodic count operation in up-counting by the count clock

Figure 23.4 shows an example setting for periodic count operation in up-counting.

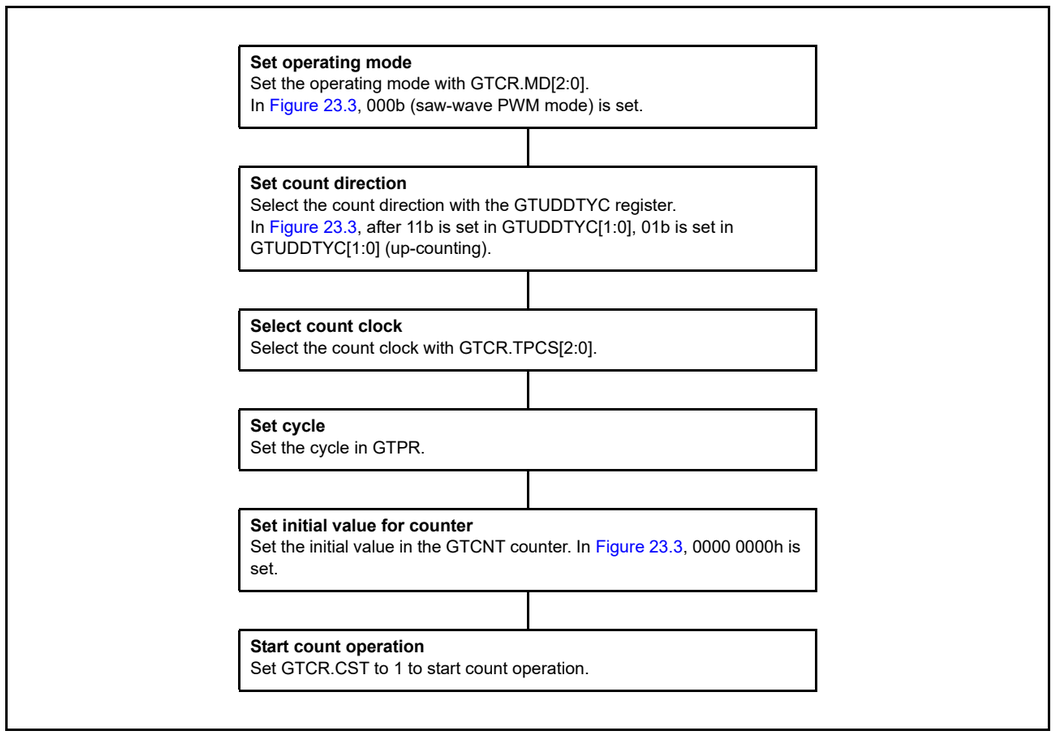


Figure 23.4 Example setting for a periodic count operation in up-counting by the count clock

(3) Periodic count operation in down-counting by count clock

The GTCNT counter in each channel can perform down-counting by setting GTUDDTYC.UD with the GTUPSR and GTDNSR registers set to 0000 0000h. When GTCNT changes from 0 to the GTPR value (underflow), GTST.TCFPU is set to 1. When the GTCNT counter underflows, down-counting resumes from the GTPR value.

Figure 23.5 shows an example of periodic count operation in down-counting by the count clock.

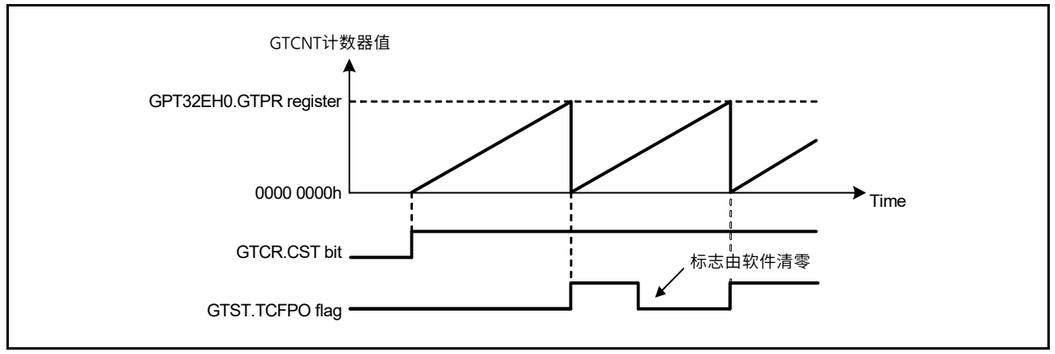


Figure 23.3 计数时钟递增计数中的周期计数操作示例

图23.4显示了递增计数中周期性计数操作的示例设置。

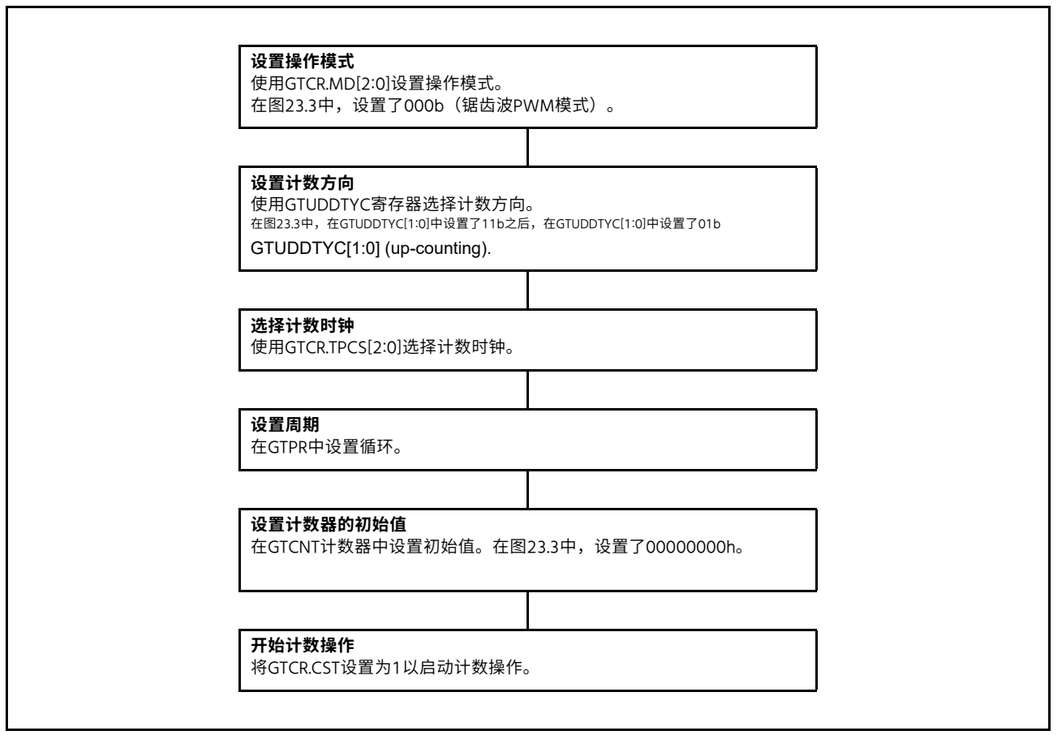


Figure 23.4 计数时钟递增计数中周期性计数操作的示例设置

(3) 计数时钟递减计数中的周期计数操作

每个通道中的GTCNT计数器可以通过使用GTUPSR设置GTUDDTYC.UD和GTDNSR寄存器设置为00000000h。当GTCNT从0变为GTPR值（下溢）时，GTST.TCFPU设置为1。当GTCNT计数器下溢时，从GTPR值开始向下计数。

图23.5显示了计数时钟递减计数中周期性计数操作的示例。

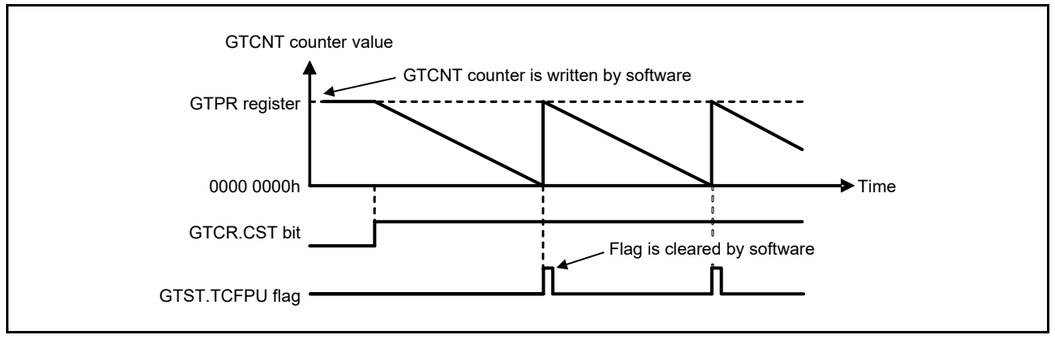


Figure 23.5 Example of periodic count operation in down-counting by the count clock

Figure 23.6 shows an example setting for periodic count operation in down-counting by the count clock.

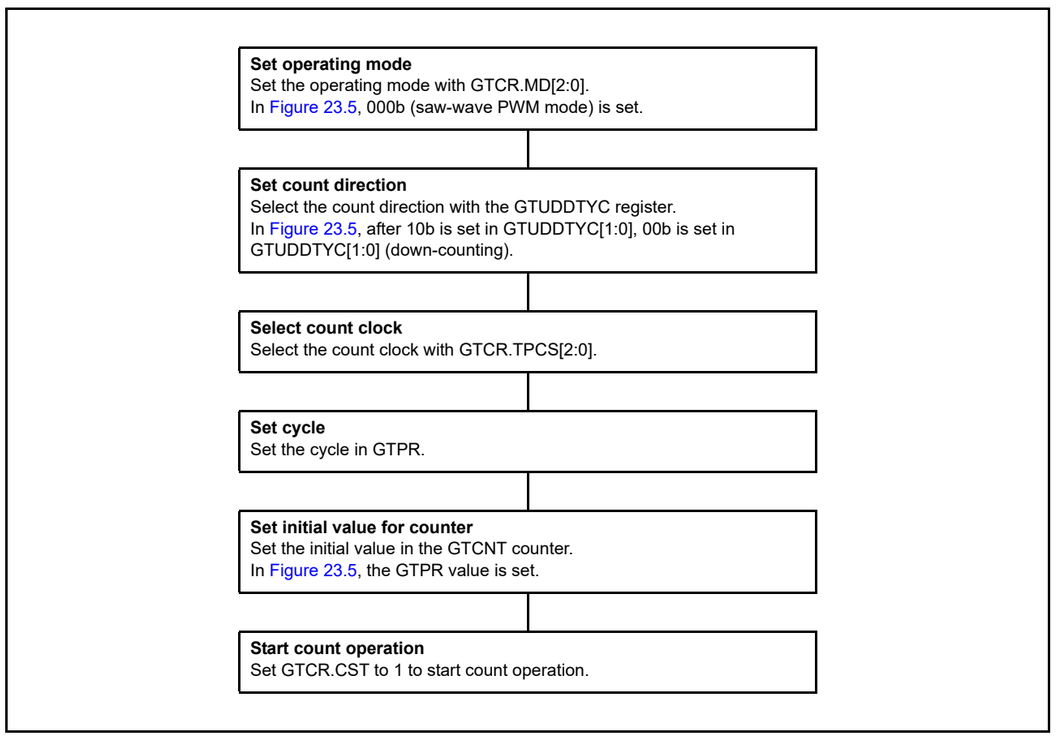


Figure 23.6 Example setting for periodic count operation in down-counting by count clock

(4) Event count operation in up-counting using hardware sources

The GTCNT counter in each channel can perform up-counting using hardware sources as set in GTUPSR.

When GTUPSR is set to enable, the count clock selected in GTCR.TPCS[2:0] and the count direction selected in GTUDDTYC.UD are ignored. If up-counting and down-counting using hardware sources occur at the same time, the GTCNT counter value does not change. The overflow behavior for up-counting using hardware sources is the same as for up-counting by the count clock.

When GTCR.CST bit is set to 1 to count up using hardware sources, the count operation is enabled. After GTCR.CST is set to 1, the counter cannot count up for 1 clock cycle as specified in GTCR.TPCS[2:0] because the count operation is

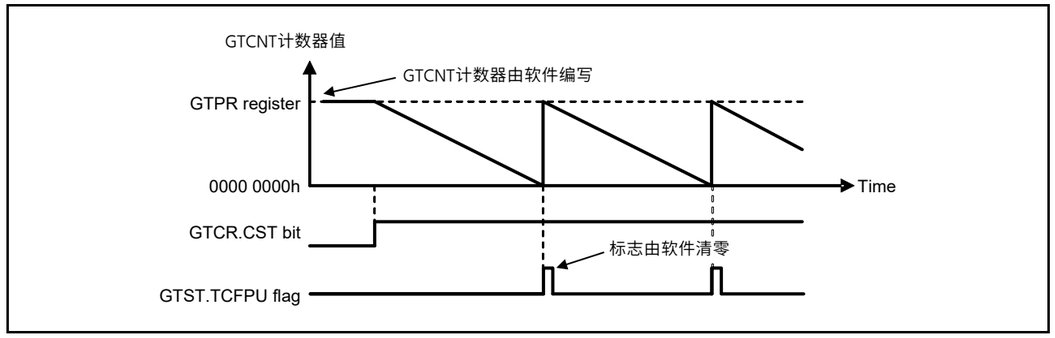


Figure 23.5 计数时钟递减计数中的周期计数操作示例

图23.6显示了计数时钟递减计数中周期性计数操作的示例设置。

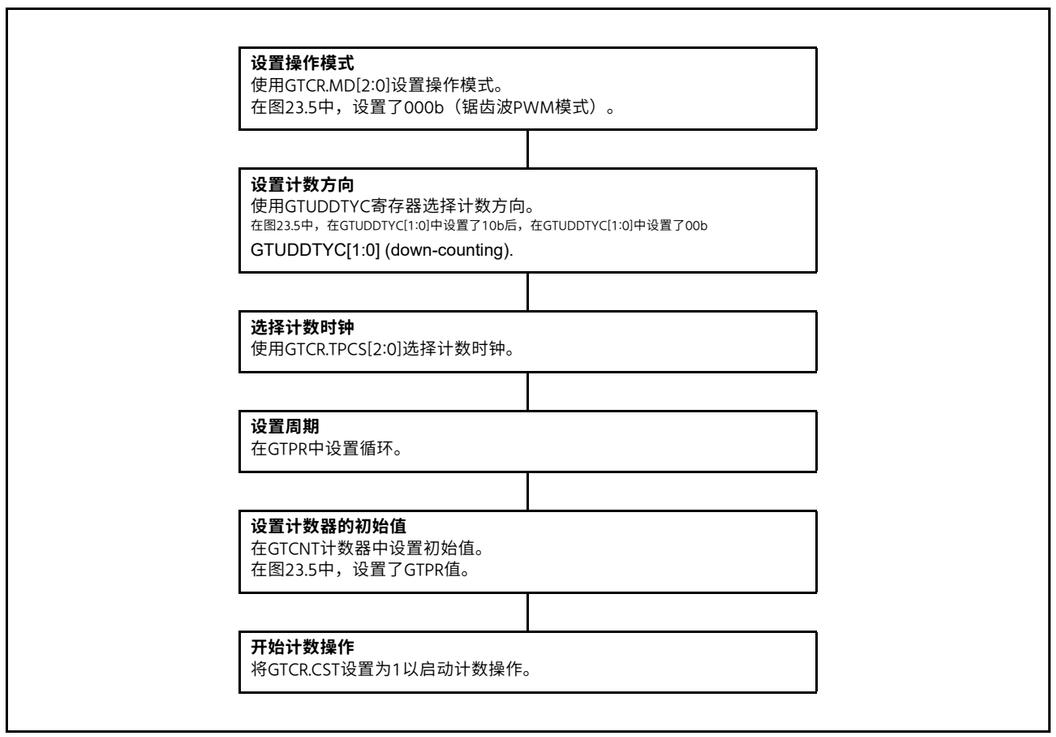


Figure 23.6 计数时钟递减计数中的周期计数操作设置示例

(4) 使用硬件源的递增计数中的事件计数操作

每个通道中的GTCNT计数器可以使用GTUPSR中设置的硬件源执行递增计数。

当GTUPSR设置为使能时，在GTCR.TPCS[2:0]中选择的计数时钟和在GTUDDTYC.UD被忽略。如果同时使用硬件源进行向上计数和向下计数，则GTCNT计数器值不会改变。使用硬件源进行向上计数的溢出行为与使用计数时钟进行向上计数的溢出行为相同。

当GTCR.CST位设置为1以使用硬件源进行计数时，计数操作被启用。GTCR.CST设置为1后，计数器不能按GTCR.TPCS[2:0]中的规定向上计数1个时钟周期，因为计数操作是

synchronized by the count clock selected in GTCR.TPCS[2:0]. Set GTCR.TPCS[2:0] to 000b to count up with a 1 PCLKD delay after GTCR.CST is set to 1.

Figure 23.7 shows an example of a periodic count operation in up-counting by a hardware source (rising edge of GTETRGA pin).

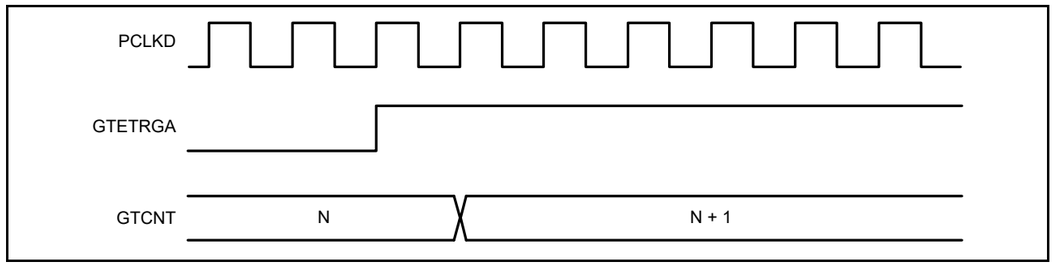


Figure 23.7 Example of periodic count operation in up-counting using hardware sources

Figure 23.8 shows an example setting for periodic count operation in up-counting by a hardware source.

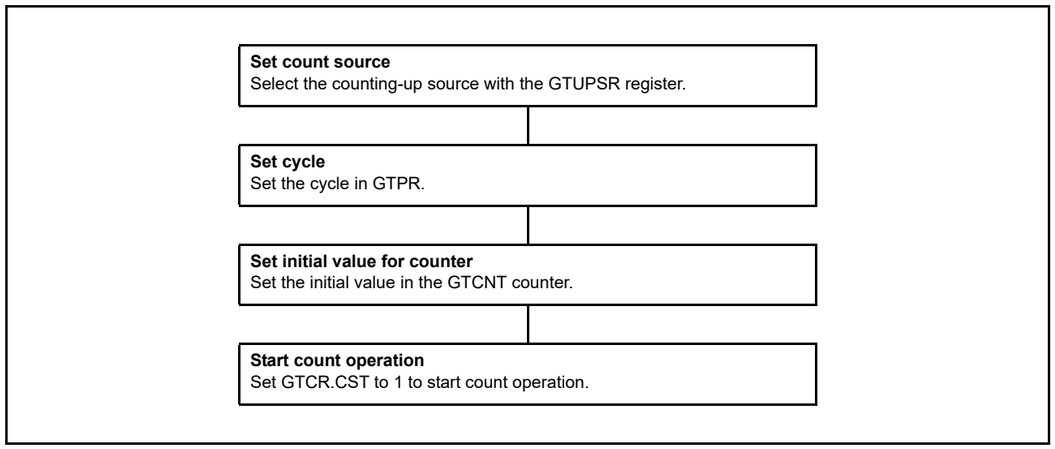


Figure 23.8 Example setting for an event count operation in up-counting using hardware sources

(5) Event count operation in down-counting using hardware sources

The GTCNT counter in each channel can perform down-counting using hardware sources set in the GTDNSR register.

When GTDNSR is set to enable, the count clock selected in GTCR.TPCS[2:0] and the count direction selected in GTUDDTYC.UD are ignored. If up-counting and down-counting using hardware sources occur at the same time, GTCNT counter value does not change. The underflow behavior for down-counting using hardware sources is the same as for down-counting by the count clock.

When GTCR.CST bit is set to 1 to count down using hardware sources, the count operation is enabled. After GTCR.CST is set to 1, the counter cannot count down for 1 clock cycle as specified in GTCR.TPCS[2:0] because the count operation is synchronized with the count clock selected by GTCR.TPCS[2:0]. Set GTCR.TPCS[2:0] to 000b to count down with a 1 PCLKD delay after GTCR.CST is set to 1.

Figure 23.9 shows an example of a periodic count operation in down-counting by a hardware source (rising edge of GTETRGA pin).

由GTCR.TPCS[2:0]中选择的计数时钟同步。将GTCR.TPCS[2:0]设置为000b以在GTCR.CST设置为1后以1个PCLKD延迟向上计数。

图23.7显示了硬件源递增计数中的周期性计数操作的示例（上升沿GTETRGA pin).

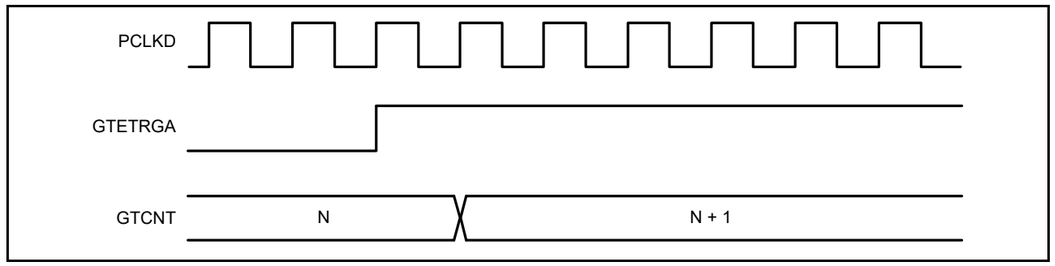


Figure 23.7 使用硬件源进行递增计数的周期性计数操作示例

图23.8显示了硬件源递增计数中周期性计数操作的示例设置。

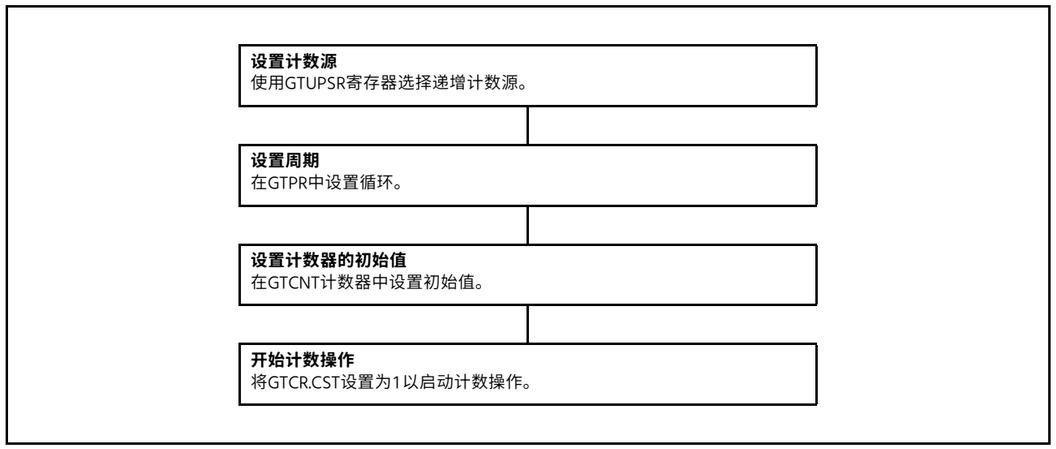


Figure 23.8 使用硬件源的递增计数中的事件计数操作设置示例

(5) 使用硬件源的递减计数中的事件计数操作

每个通道中的GTCNT计数器可以使用GTDNSR寄存器中设置的硬件源进行递减计数。

当GTDNSR设置为使能时，在GTCR.TPCS[2:0]中选择的计数时钟和在GTUDDTYC.UD中选择的计数方向被忽略。如果同时发生使用硬件源的递增计数和递减计数，
GTCNT计数器值不会改变。使用硬件源向下计数的下溢行为与使用计数时钟向下计数的相同。

当GTCR.CST位设置为1以使用硬件源进行递减计数时，启用计数操作。GTCR.CST设置为1后，计数器无法按照GTCR.TPCS[2:0]中的规定倒计时1个时钟周期，因为计数操作与GTCR.TPCS[2:0]选择的计数时钟同步。将GTCR.TPCS[2:0]设置为000b以在GTCR.CST设置为1后以1个PCLKD延迟递减计数。

图23.9显示了一个由硬件源进行递减计数的周期性计数操作示例（上升沿GTETRGA pin).

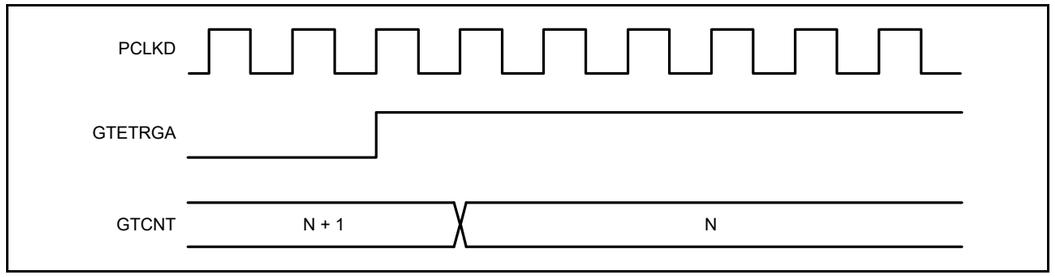


Figure 23.9 Example of event count operation in down-counting using hardware sources

Figure 23.10 shows an example setting for a periodic count operation in down-counting using a hardware source.

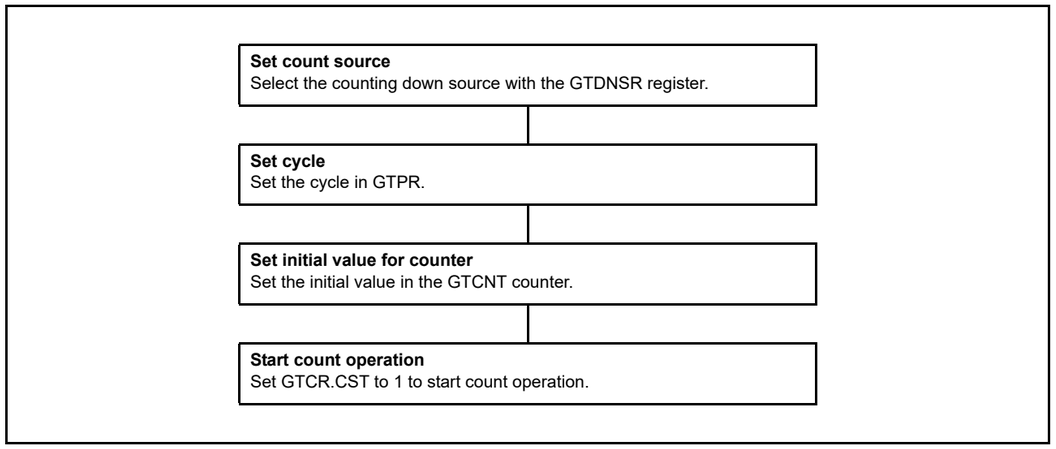


Figure 23.10 Example setting for an event count operation in down-counting using hardware sources

(6) Counter clear operation

The counter of each channel is cleared by following sources:

- Writing 0 to GTCNT register
- Writing 1 to the bit in GTCLR associated with the GPT channel number when the GTCSR.CCLR bit is set to 1
- The hardware source selected in GTCSR register.

Writing to the GTCNT register is prohibited during count operation. The GTCNT counter can be cleared both by writing 1 to the GTCLR and by the clear request of hardware sources, whether GTCNT is counting (GTCR.CST = 1) or not (GTCR.CST = 0).

For saw waves selected by setting GTCR.MD[2:0] and the count direction flag showing down-counting (GTST.TUCF = 0), the GTCNT register is set to the value of the GTPR register when writing 1 to the GTCLR register or when clearing by hardware sources is performed. When not in saw wave mode and down-counting, the GTCNT register is set to 0 when writing 1 to the GTCLR register and when clearing by hardware sources is performed.

In event count operation when at least 1 bit in GTUPSR or GTDNSR is set to 1, after clear sources occur, both writing to GTCLR register and clearing by hardware sources are performed immediately, synchronized with PCLKD. If other settings are used, clear is synchronized with the counter clock selected in GTCR.TPCS[2:0].

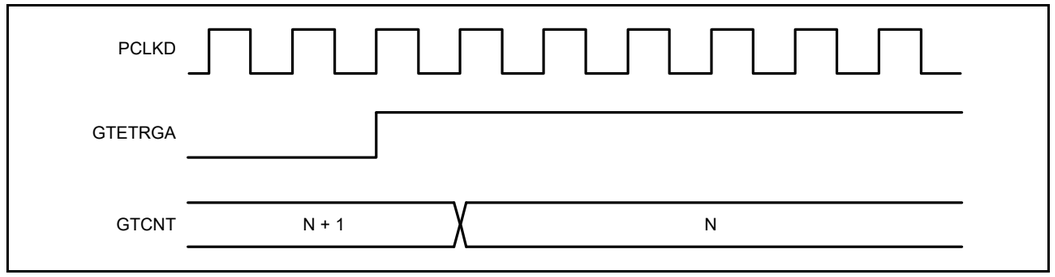


Figure 23.9 使用硬件源递减计数中的事件计数操作示例

图23.10显示了使用硬件源进行递减计数中的周期性计数操作的示例设置。

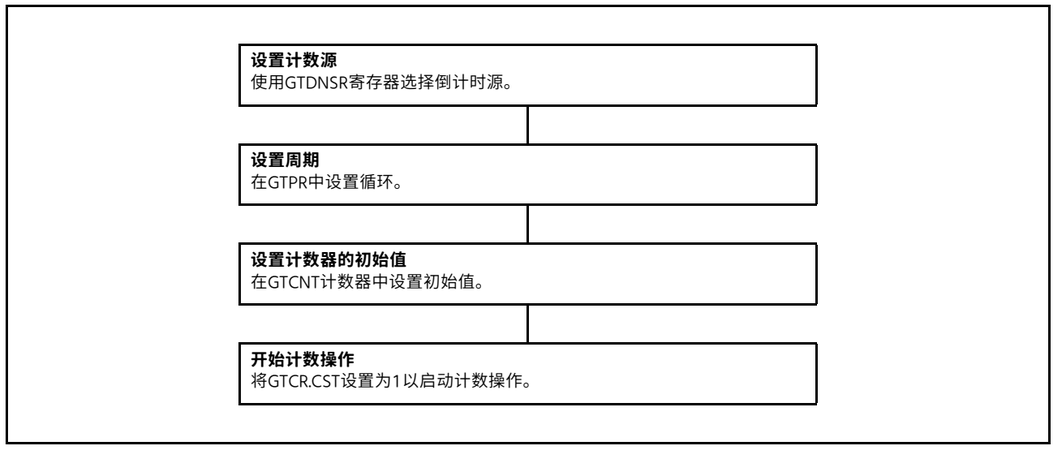


Figure 23.10 使用硬件源的递减计数中的事件计数操作设置示例

(6) 计数器清零操作

每个通道的计数器由以下来源清零：

- 将0写入GTCNT寄存器
- 当GTCSR.CCLR位设置为1时，将1写入GTCLR中与GPT通道号相关的位
- 在GTCSR寄存器中选择的硬件源。

计数操作期间禁止写入GTCNT寄存器。GTCNT计数器可以通过向GTCLR写入1和硬件源的清除请求来清除，无论GTCNT正在计数（GTCR.CST=1）还是不计数（GTCR.CST=0）。

对于通过设置GTCR.MD[2:0]和显示递减计数的计数方向标志(GTST.TUCF=0)选择的锯齿波，当向GTCLR寄存器写入1时，GTCNT寄存器设置为GTPR寄存器的值或执行硬件源清除时。当不处于锯齿波模式和递减计数时，当向GTCLR寄存器写入1并执行硬件源清零时，GTCNT寄存器设置为0。

在事件计数操作中，当GTUPSR或GTDNSR中至少有1位设置为1时，清除源发生后，两者都写入GTCLR寄存器和硬件源的清除立即执行，与PCLKD同步。如果使用其他设置，则清除与GTCR.TPCS[2:0]中选择的计数器时钟同步。

23.3.1.2 Waveform output by compare match

Compare match means that the GTCNT counter value matches the value of GTCCRA or GTCCRB. When a compare match occurs, the compare match flag is generated synchronously with the count clock, including the event count. At the same time the GPT can output low, high, or toggle output from the associated GTIOCA or GTIOCB output pin. In addition, the GTIOCA or GTIOCB pin output can be low, high, or toggle at the cycle end, which is determined by GTPR.

The cycle end is:

- For saw waves in up-counting — when GTCNT changes from the GTPR value to 0 (overflow)
- For saw waves in down-counting — when GTCNT changes from 0 to the GTPR value (underflow)
- For saw waves — when the GTCNT counter is cleared
- For triangle waves — when the GTCNT changes from 0 to 1 (trough).

(1) Low output and high output

Figure 23.11 shows an example of low output and high output operation by a compare match of GTCCRA and GTCCRB.

In this example, the GPT32EH0.GTCNT counter performs up-counting, and settings are made so that high is output from the GTIOC0A pin by a GPT32EH0.GTCCRA compare match, and low is output from the GTOC0B pin by a GPT32EH0.GTCCRB compare match. The pin level does not change when the specified level and pin level match.

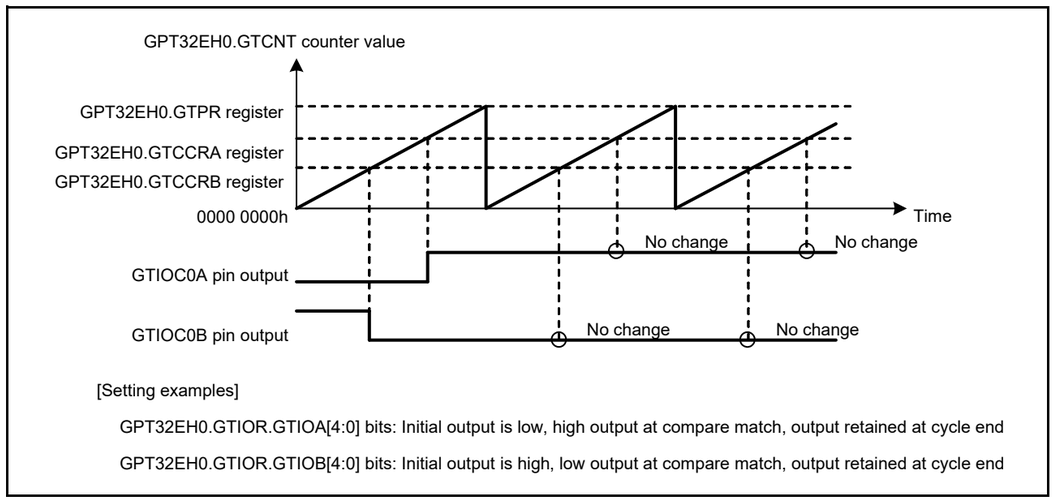


Figure 23.11 Example of low output and high output operation

Figure 23.12 shows an example setting for low output and high output operation.

23.3.1.2 比较匹配的波形输出

比较匹配意味着GTCNT计数器值与GTCCRA或GTCCRB的值匹配。当比较匹配发生时，比较匹配标志与计数时钟同步生成，包括事件计数。同时，GPT可以从相关的GTIOCA或GTIOCB输出引脚输出低、高或切换输出。此外，GTIOCA或GTIOCB引脚输出可以在周期结束时为低、高或翻转，这由GTPR确定。

循环结束为：

- 对于向上计数中的锯齿波——当GTCNT从GTPR值变为0（溢出）时
- 对于向下计数中的锯齿波——当GTCNT从0变为GTPR值时（下溢）
- 对于锯齿波——当GTCNT计数器清零时
- 对于三角波——当GTCNT从0变为1（波谷）时。

(1) 低输出和高输出

图23.11显示了通过GTCCRA和比较匹配的低输出和高输出操作示例
GTCCRB.

在本例中，GPT32EH0.GTCNT计数器进行递增计数，设置为通过GPT32EH0.GTCCRA比较匹配从GTIOC0A引脚输出高电平，通过GPT32EH0.GTCCRB比较匹配从GTOC0B引脚输出低电平.当指定电平和引脚电平匹配时，引脚电平不会改变。

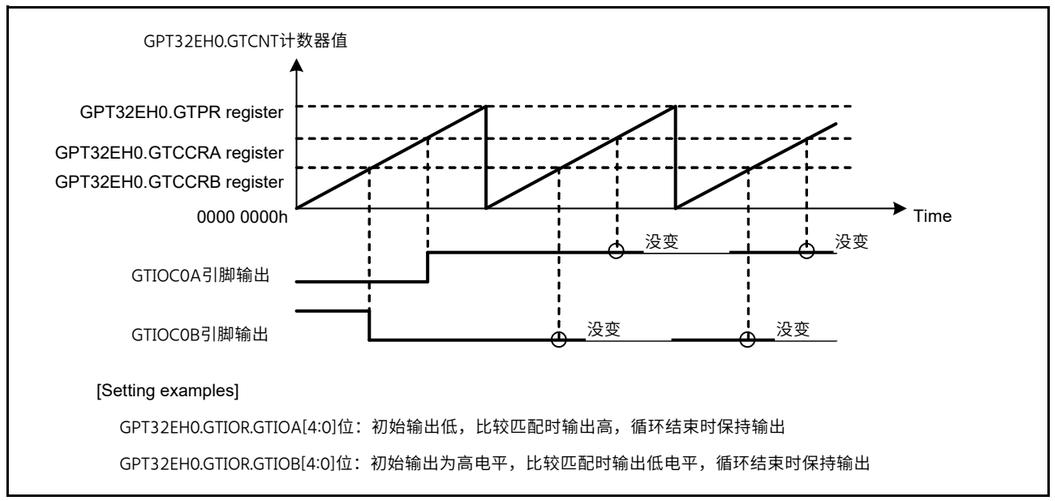
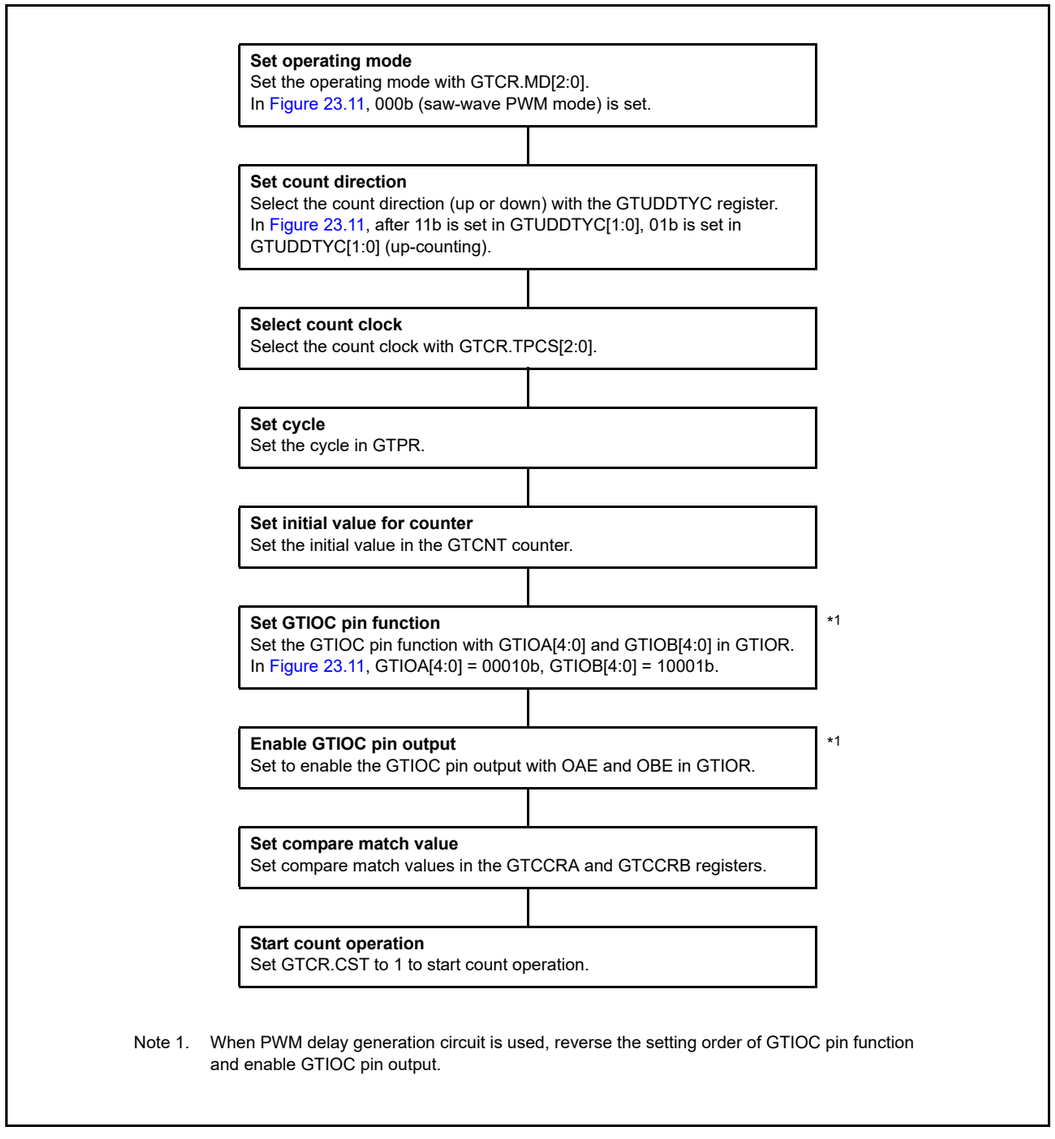


Figure 23.11 低输出和高输出操作示例

图23.12显示了低输出和高输出操作的示例设置。



Note 1. When PWM delay generation circuit is used, reverse the setting order of GTIOC pin function and enable GTIOC pin output.

Figure 23.12 Example setting for low output and high output operation

(2) Toggled output

Figure 23.13 and Figure 23.14 show examples of toggled output operation by compare matches of GTCCRA and GTCCRB. In Figure 23.13, the GPT32EH0.GTCNT counter performs up-counting, and settings are made so that the GTIOC0A pin output by a GPT32EH0.GTCCRA compare match and GTIOC0B pin output by a GPT32EH0.GTCCRB compare match are toggled.

In Figure 23.14, the GPT32EH0.GTCNT counter performs up-counting, and settings are made so that the GTIOC0A output is toggled by a compare match of GPT32EH0.GTCCRA and the GTIOC0B output is toggled at the cycle end.

Note 1. 当使用PWM延迟产生电路时，将GTIOC引脚功能的设置顺序颠倒，使能GTIOC引脚输出。

Figure 23.12 低输出和高输出操作的示例设置

(2) Toggled output

图23.13和图23.14显示了通过比较匹配GTCCRA和
GTCCRB。在图23.13中，GPT32EH0.GTCNT计数器执行递增计数，并进行设置以使
GPT32EH0.GTCCRA比较匹配的GTIOC0A引脚输出和GPT32EH0.GTCCRB比较匹配的GTIOC0B引脚输出被切换。

在图23.14中，GPT32EH0.GTCNT计数器执行递增计数，并进行设置，以便通过GPT32EH0.GTCCRA的比较匹配来切换GTIOC0A输出，并在周期结束时切换GTIOC0B输出。

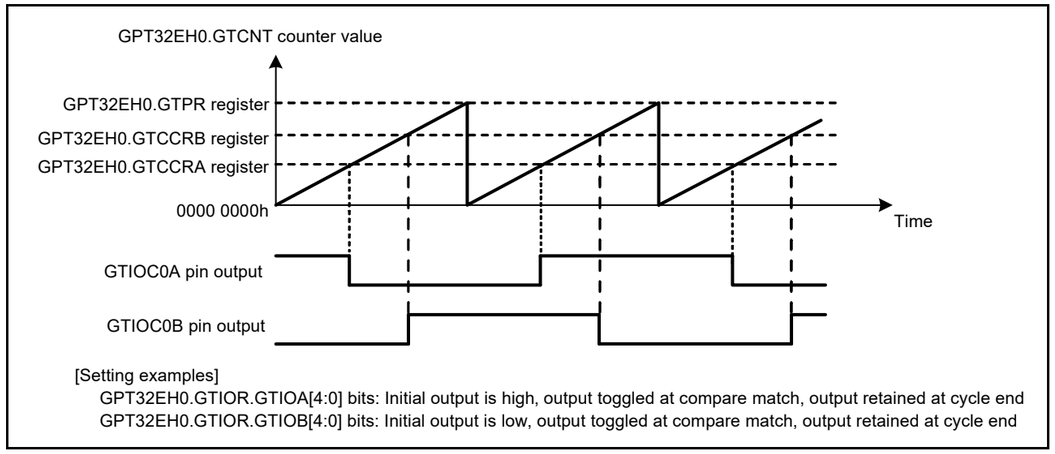


Figure 23.13 Example of toggled output operation (1)

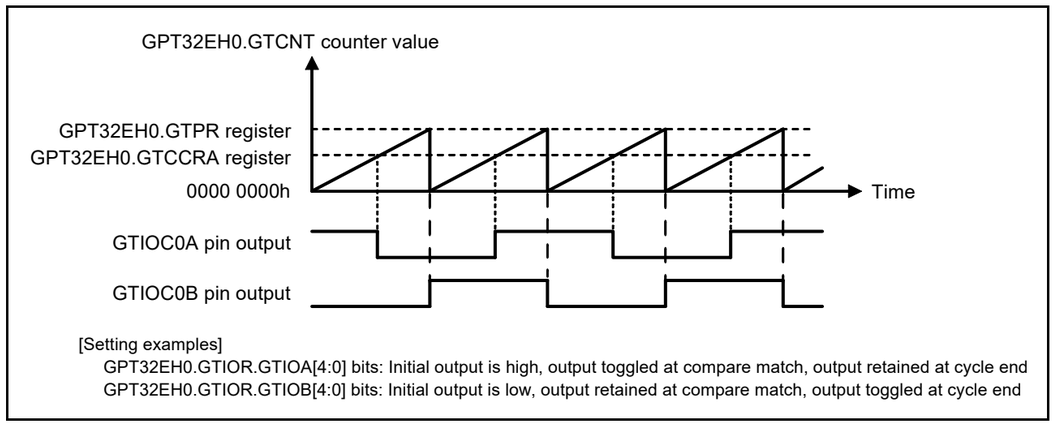


Figure 23.14 Example of toggled output operation (2)

Figure 23.15 shows an example setting for toggled output operation.

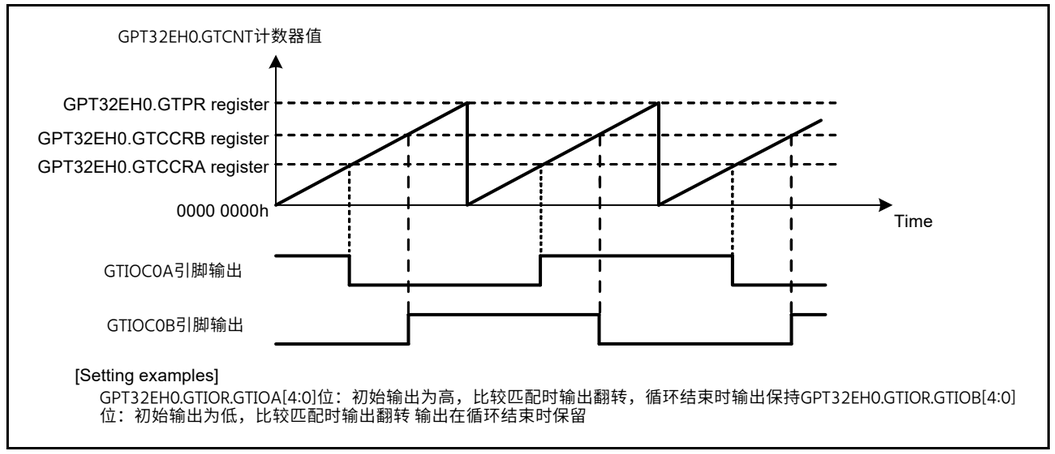


Figure 23.13 切换输出操作示例(1)

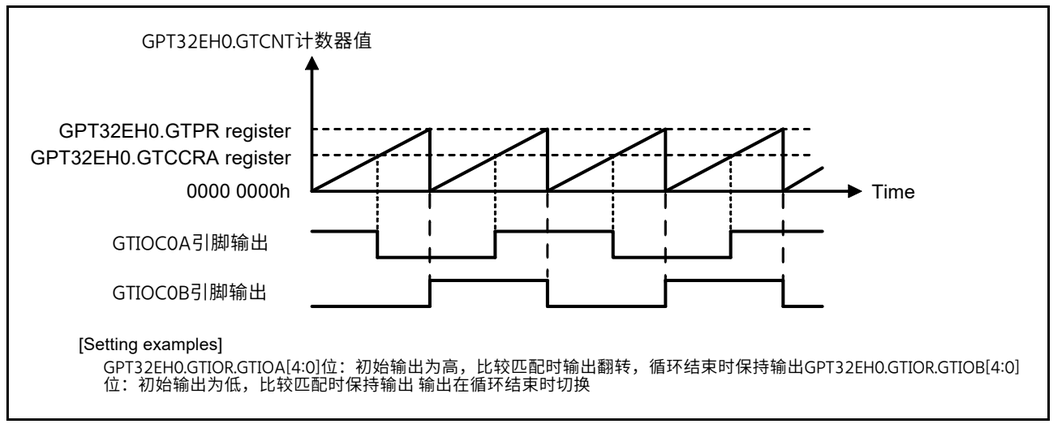
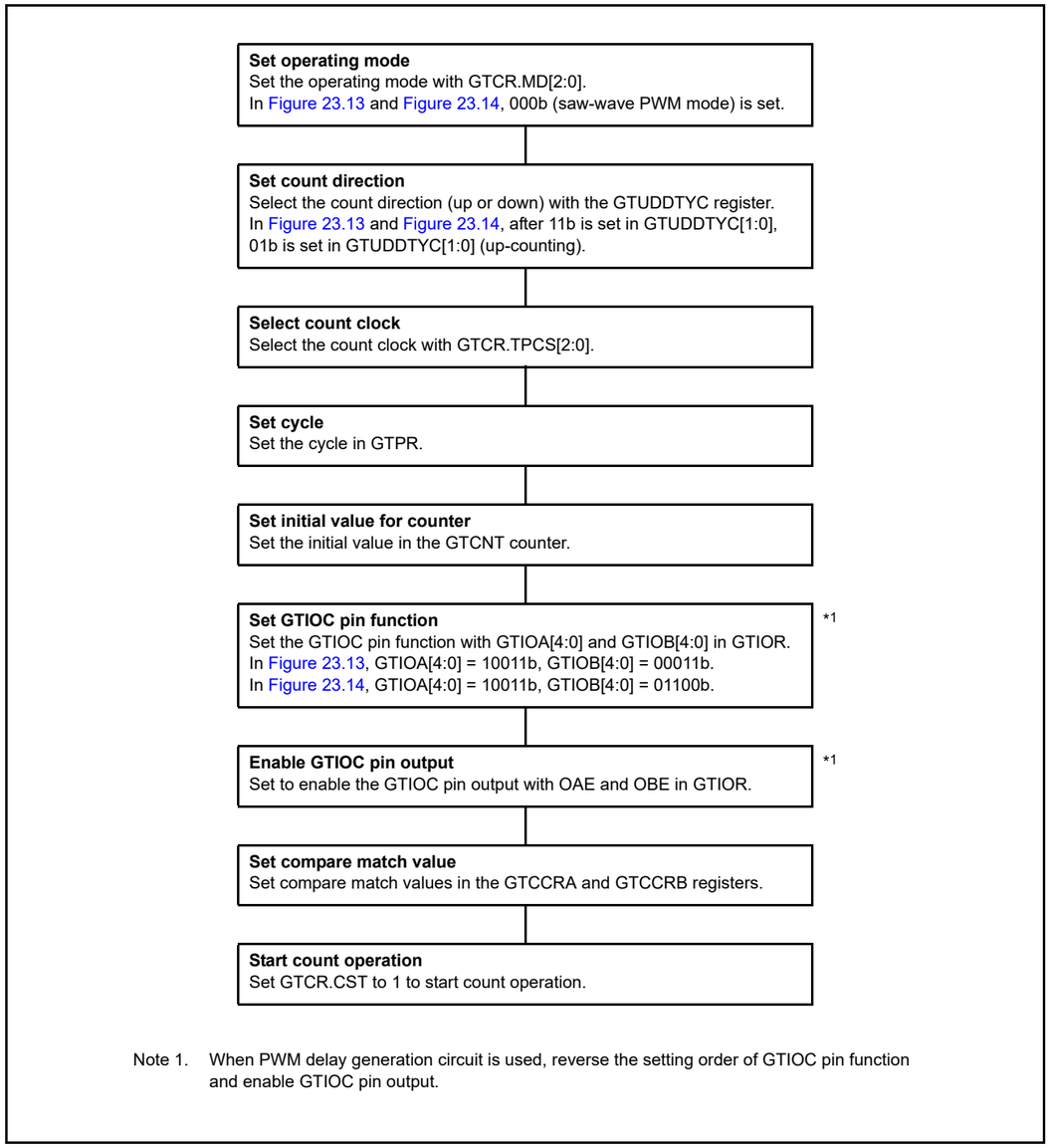


Figure 23.14 切换输出操作示例(2)

图23.15显示了切换输出操作的示例设置。



Note 1. When PWM delay generation circuit is used, reverse the setting order of GTIOC pin function and enable GTIOC pin output.

Figure 23.15 Example setting for toggled output operation

23.3.1.3 Input capture function

The GTCNT counter value can be transferred to either GTCCRA or GTCCRB on detection of the hardware source that is set in GTICASR and GTICBSR.

Figure 23.16 shows an example of the input capture function.

In this example, the GPT32EH0.GTCNT counter performs up-counting by the count clock, and settings are made so that an input capture is performed to GTICCRA at both edges of the GTIOC0A input pin and to GTICCRB on the rising edge of the GTIOC0B input pin.

Note 1. 当使用PWM延迟产生电路时，将GTIOC引脚功能的设置顺序颠倒，使能GTIOC引脚输出。

Figure 23.15 切换输出操作的示例设置

23.3.1.3 输入捕捉功能

在检测到在GTICASR和GTICBSR中设置的硬件源时，可以将GTCNT计数器值传输到GTCCRA或GTCCRB。

图23.16显示了输入捕获函数的示例。

在本例中，GPT32EH0.GTCNT计数器通过计数时钟进行递增计数，并设置为在GTIOC0A输入引脚的两个边沿对GTICCRA进行输入捕捉，在GTIOC0B输入的上升沿对GTICCRB进行输入捕捉别针。

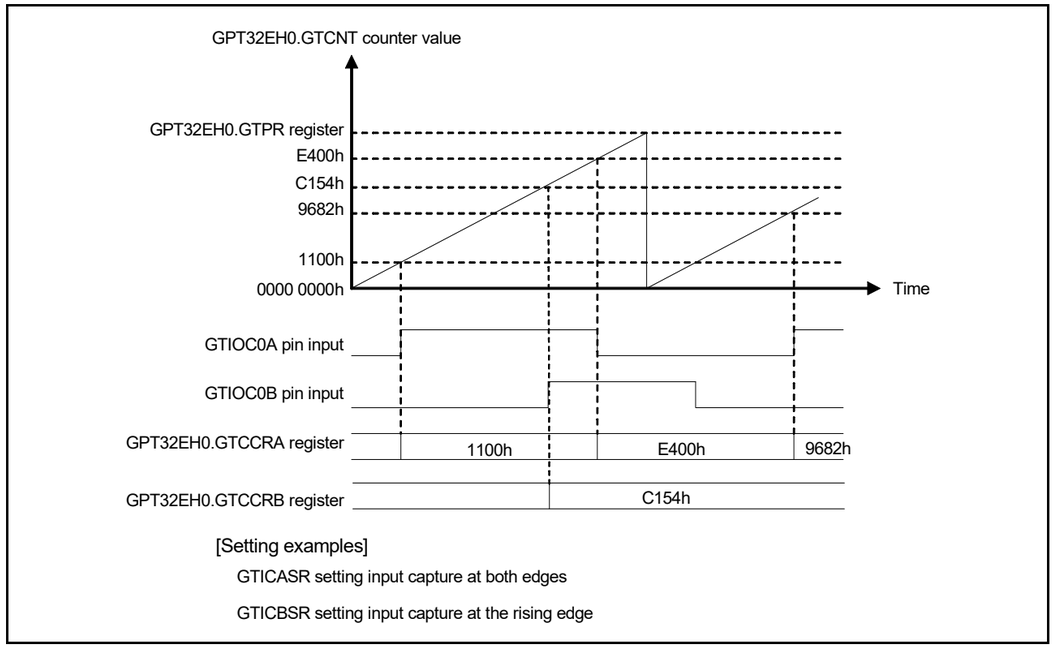


Figure 23.16 Example of input capture operation

Figure 23.17 shows an example setting for an input capture operation with count operation by the count clock.

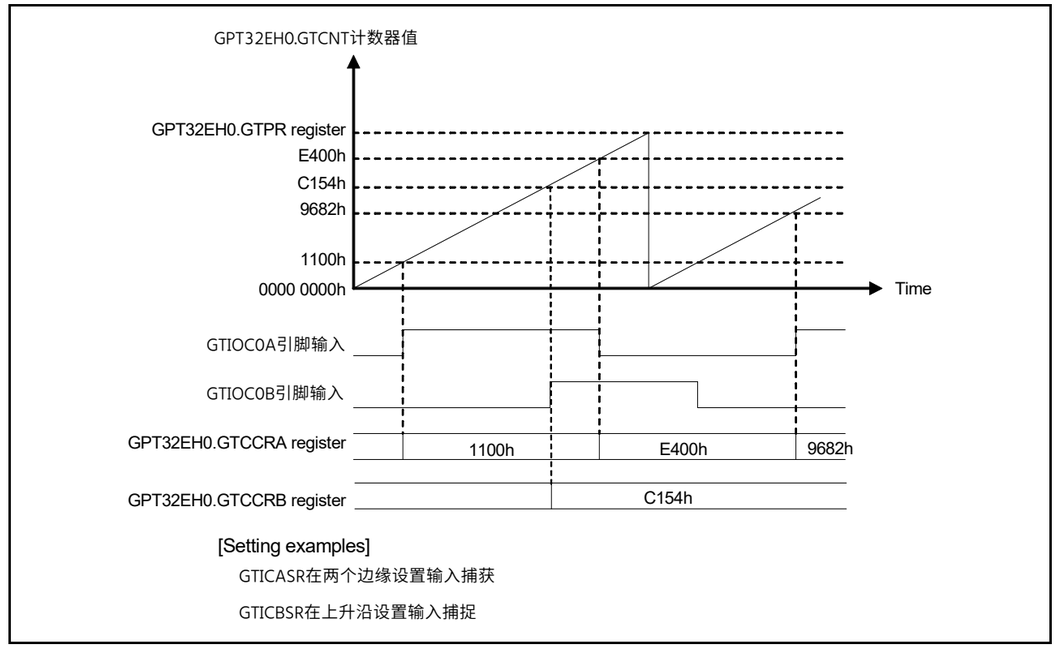


Figure 23.16 输入捕捉操作示例

图23.17显示了通过计数时钟进行计数操作的输入捕捉操作的示例设置。

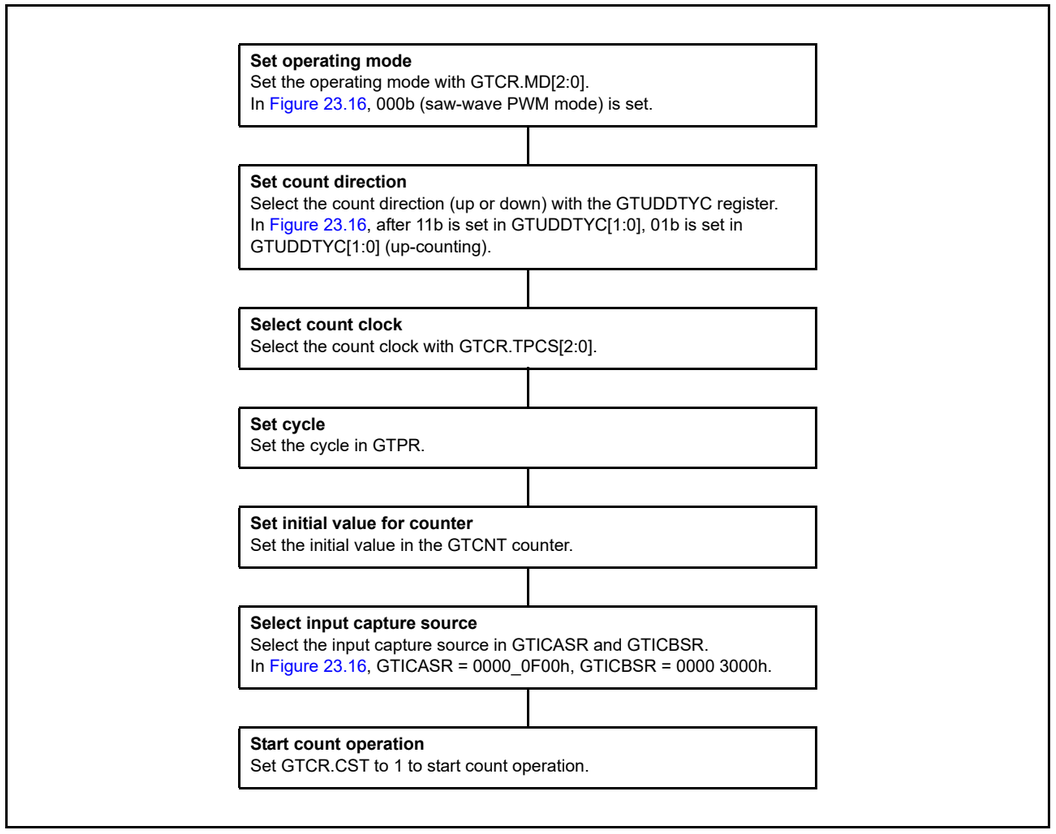


Figure 23.17 Example setting for input capture operation

23.3.2 Buffer Operation

The following buffer operations can be set with GTBER:

- GTPR, GTPBR, and GTPDBR
- GTCCRA, GTCCRC, and GTCCRD
- GTCCRB, GTCCRE, and GTCCRF
- GTADTRA, GTADTBRA, and GTADTDBRA
- GTADTRB, GTADTBRB, and GTADTDBRB.

The following buffer operations can be set with GTDTCR:

- GTDVU and GTDBU
- GTDVU and GTDBD.

23.3.2.1 GTPR register buffer operation

GTPBR can function as a buffer register for GTPR, and GTPDBR can function as a buffer register for GTPBR (double-buffer register for GTPR). The buffer transfer is performed at an overflow (during up-counting) or an underflow (during down-counting) in saw-wave mode or in event count, and at a trough in triangle-wave mode.

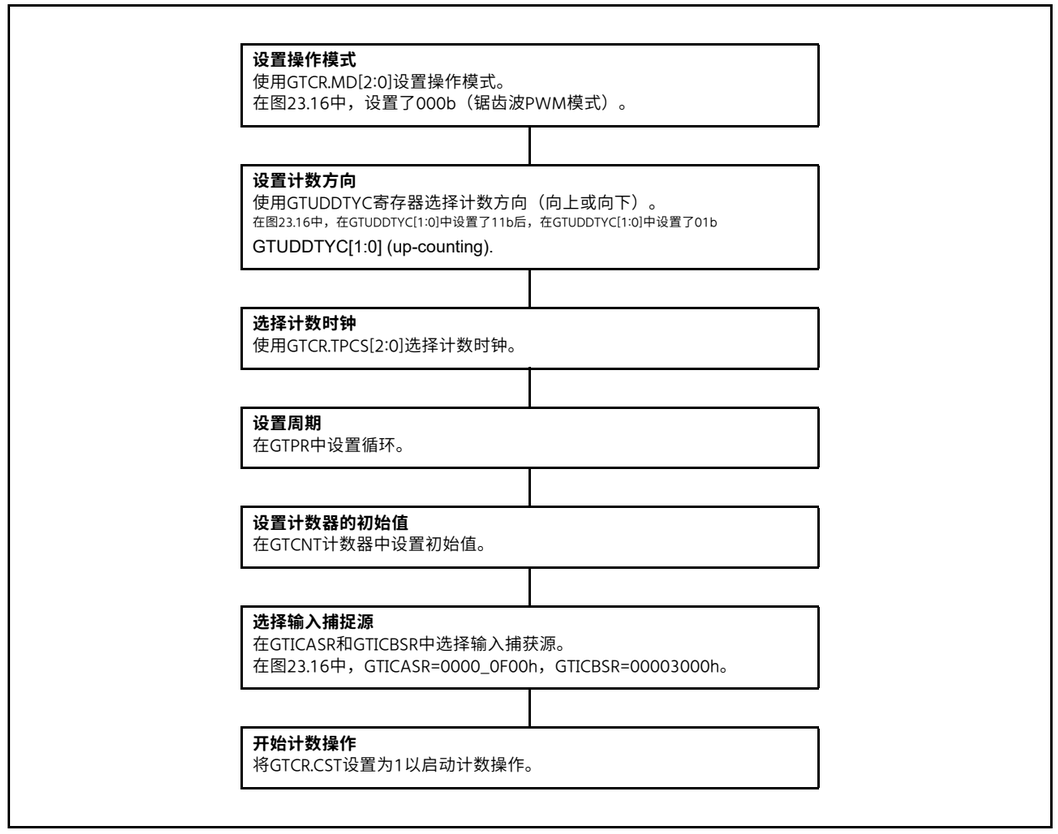


Figure 23.17 输入捕捉操作的示例设置

23.3.2 缓冲操作

可以使用GTBER设置以下缓冲区操作：

- GTPR, GTPBR, and GTPDBR
- GTCCRA, GTCCRC, and GTCCRD
- GTCCRB, GTCCRE, and GTCCRF
- GTADTRA, GTADTBRA, and GTADTDBRA
- GTADTRB, GTADTBRB, and GTADTDBRB.

可以使用GTDTCR设置以下缓冲区操作：

- GTDVU and GTDBU
- GTDVU and GTDBD.

23.3.2.1 GTPR寄存器缓冲操作

GTPBR可以作为GTPR的缓冲寄存器，GTPDBR可以作为GTPBR的缓冲寄存器（GTPR的双缓冲寄存器）。缓冲区传输在锯齿波模式或事件计数中的上溢（向上计数期间）或下溢（向下计数期间）以及三角波模式的波谷处执行。

In saw-wave mode or in event count, the buffer transfer is performed when the following counter clear operations occur during counting:

- Clear by hardware sources (the clear source is selected in GTCSR[23:0])
- Clear by software (when GTCSR.CCLR bit is 1 and GTCLR[n] bit is set to 1, n = channel number).

To set GTPR to function as double buffer, set GTBER.PR[1:0] to 10b or 11b. To set GTPR to not function as a buffer, set GTBER.PR[1:0] to 00b.

Figure 23.18 to Figure 23.20 show examples of GTPR buffer operation, and Figure 23.21 shows an example setting for GTPR buffer operation.

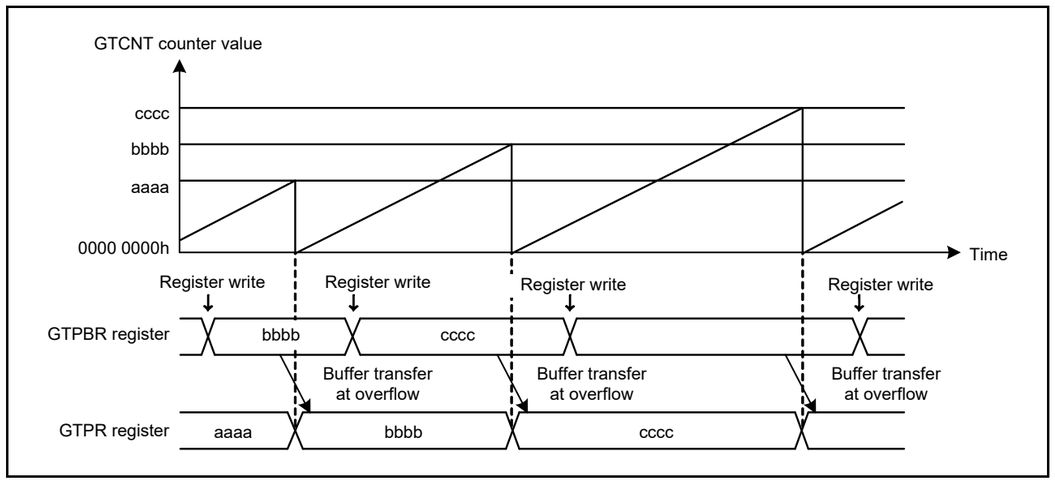


Figure 23.18 Example of GTPR buffer operation with saw waves in up-counting

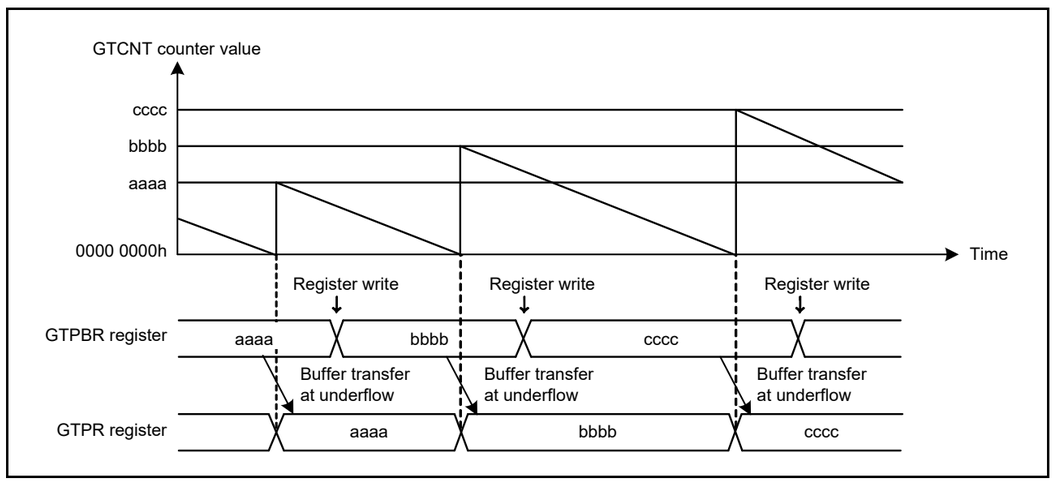


Figure 23.19 Example of GTPR buffer operation with saw waves in down-counting

在锯齿波模式或事件计数中，当计数期间发生以下计数器清零操作时，将执行缓冲区传输：

- 通过硬件源清除（清除源在GTCSR[23:0]中选择）
- 由软件清零（当GTCSR.CCLR位为1且GTCLR[n]位设置为1时，n=通道号）。

要将GTPR设置为双缓冲区，请将GTBER.PR[1:0]设置为10b或11b。要将GTPR设置为不用作缓冲区，请设置GTBER.PR[1:0] to 00b.

图23.18至图23.20显示了GTPR缓冲区操作的示例，图23.21显示了示例设置GTPR缓冲区操作。

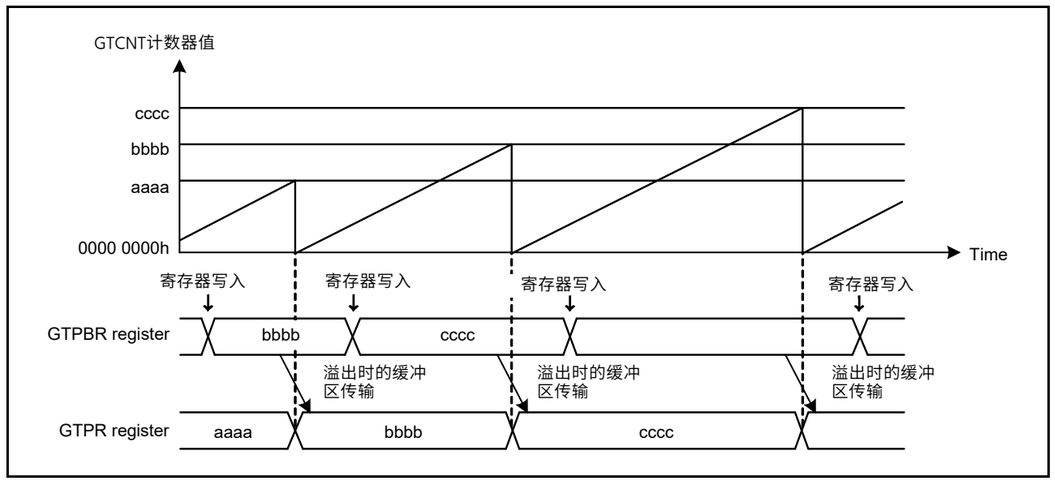


Figure 23.18 GTPR缓冲区操作示例，在向上计数中使用锯齿波

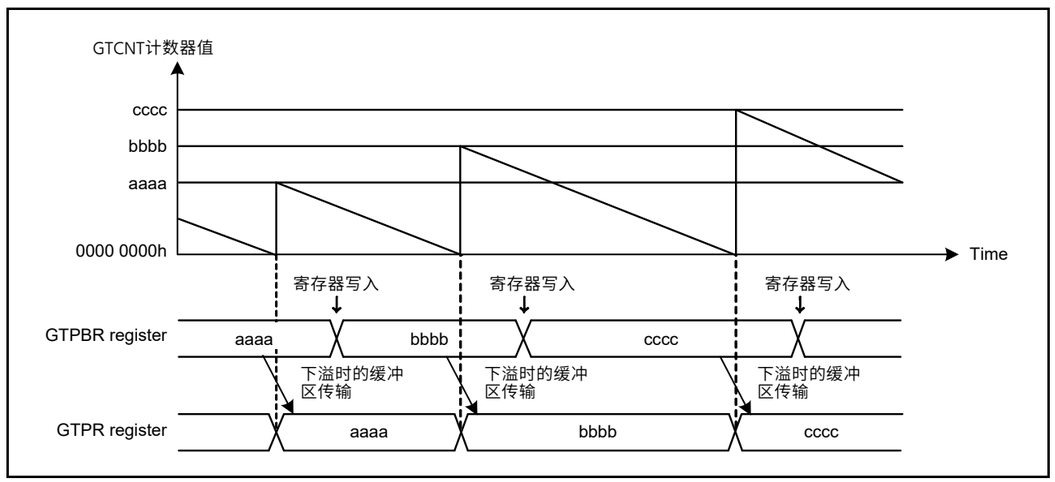


Figure 23.19 向下计数中锯波的GTPR缓冲区操作示例

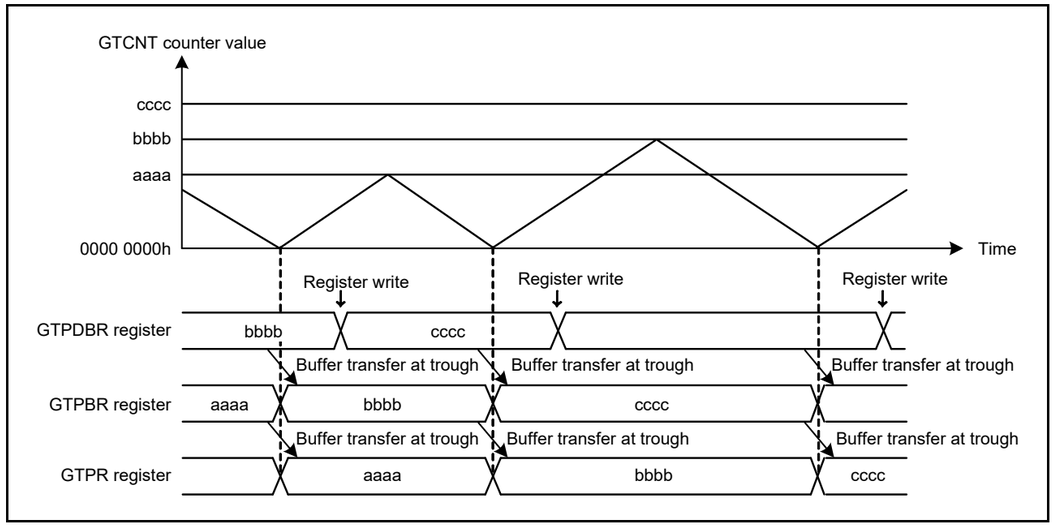


Figure 23.20 Example of GTPR double buffer operation with triangle waves

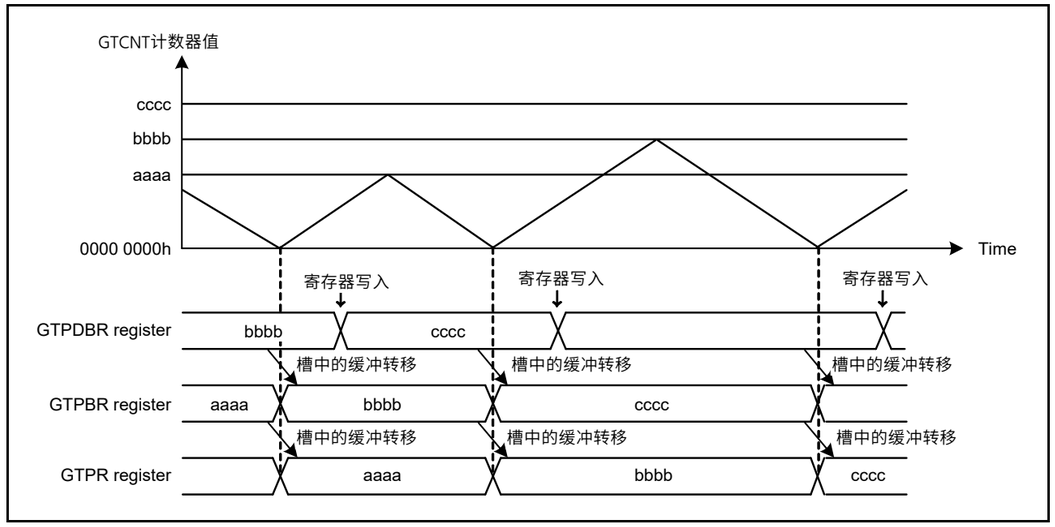


Figure 23.20 使用三角波的GTPR双缓冲操作示例

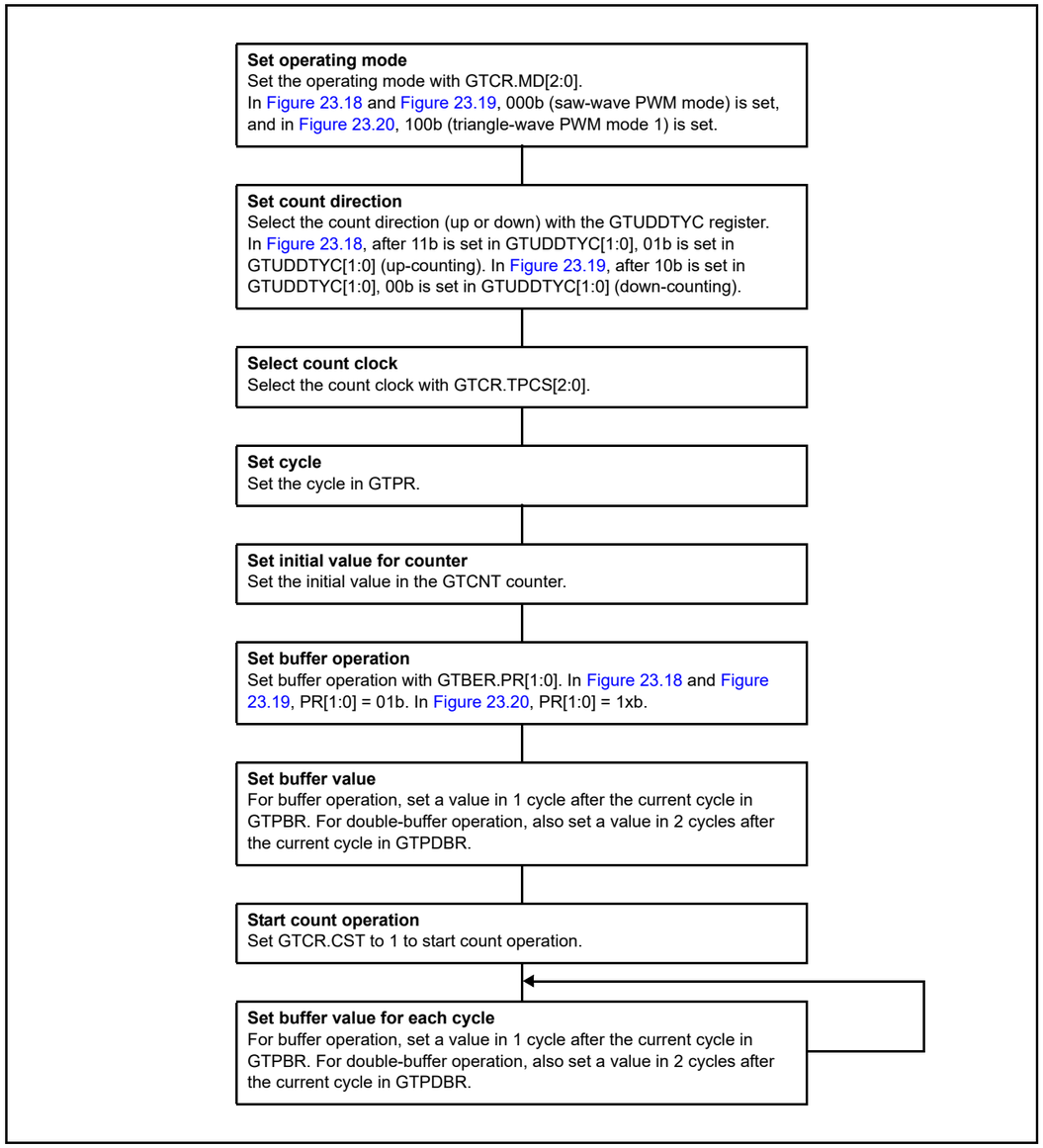


Figure 23.21 Example setting for GTPR buffer operation

23.3.2.2 Buffer operation for GTCCRA and GTCCRB

GTCCRC can function as the GTCCRA buffer register and GTCCRD can function as the GTCCRC buffer register (double-buffer register for GTCCRA). Similarly, GTCCRE can function as the GTCCRB buffer register and GTCCRF can function as the GTCCRE buffer register (double-buffer register for GTCCRB).

To set GTCCRA or GTCCRB to function as a double buffer, set GTBER.CCRA[1:0] or GTBER.CCRB[1:0] to 10b or 11b. For single-buffer operation, set GTBER.CCRA[1:0] or GTBER.CCRB[1:0] to 01b. To set GTCCRA or GTCCRB to not function as a buffer, set GTBER.CCRA[1:0] or GTBER.CCRB[1:0] to 00b.

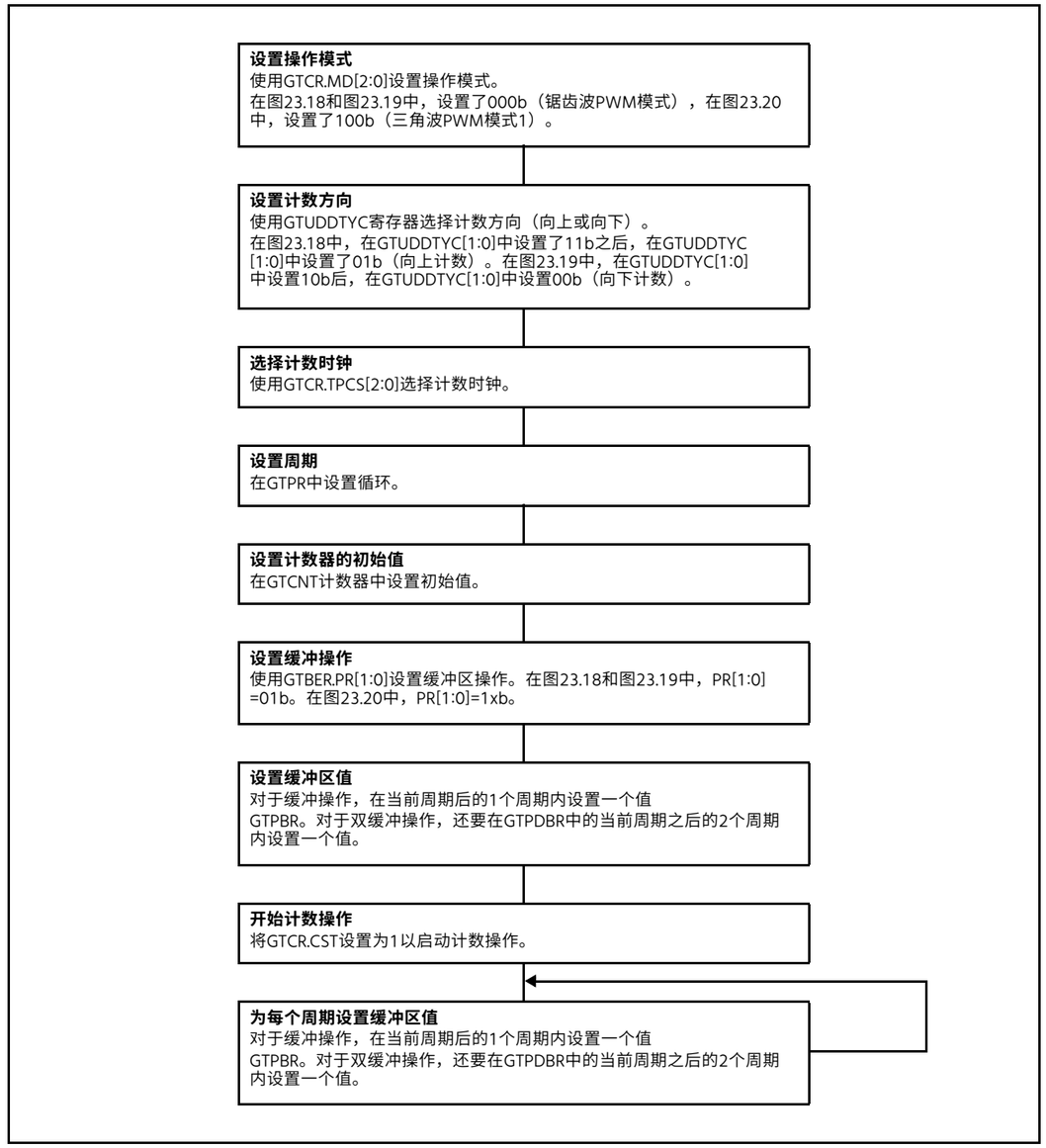


Figure 23.21 GTPR缓冲区操作的示例设置

23.3.2.2 GTCCRA和GTCCRB的缓冲操作

GTCCRC可以作为GTCCRA缓冲寄存器，GTCCRD可以作为GTCCRC缓冲寄存器（GTCCRA的双缓冲寄存器）。同样，GTCCRE可以作为GTCCRB缓冲寄存器，GTCCRF可以作为GTCCRE缓冲寄存器（GTCCRB的双缓冲寄存器）。

要将GTCCRA或GTCCRB设置为双缓冲区，请将GTBER.CCRA[1:0]或GTBER.CCRB[1:0]设置为10b或11b。对于单缓冲区操作，将GTBER.CCRA[1:0]或GTBER.CCRB[1:0]设置为01b。要将GTCCRA或GTCCRB设置为不用作缓冲区，请将GTBER.CCRA[1:0]或GTBER.CCRB[1:0]设置为00b。

(1) When GTCCRA or GTCCRB functions as an output compare register

Buffer transfer occurs in the following situations:

- Buffer transfer by overflow or underflow
  Buffer transfer is performed at an overflow (during up-counting) or an underflow (during down-counting) in saw-wave mode or in event count operation. In triangle-wave mode, buffer transfer is performed at a trough (triangle-wave PWM mode 1) or a crest and trough (triangle-wave PWM mode 2).
- Buffer transfer by counter clear
  In saw-wave mode or in event count operation, during counting, buffer transfer (which is the same as an overflow during up-counting or an underflow during down-counting) is performed by the counter clear sources the same as shown in section 23.3.2.1, GTPR register buffer operation. In triangle-wave mode, buffer transfer is not performed by the counter clear.
- Forcible buffer transfer
  When GTBER.CCRSWT bit is set to 1 while the count operation is stopped, the GTCCRA and the GTCCRB register buffer transfer is performed forcibly in saw-wave mode, in event count operation and in triangle-wave mode. Additionally, buffer transfer from the GTCCRD register to temporary register A and from the GTCCRF register to temporary register B are performed in saw-wave 1 shot pulse mode or triangle-wave PWM mode 3.

Figure 23.22 to Figure 23.24 show examples of GTCCRA and GTCCRB buffer operation and Figure 23.25 shows an example setting for GTCCRA and GTCCRB buffer operation.

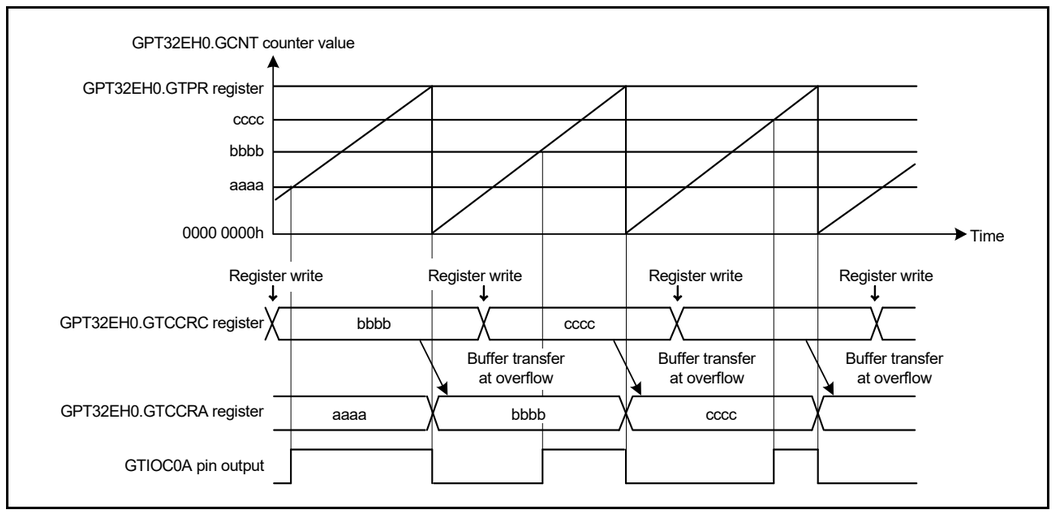


Figure 23.22 Example of GTCCRA and GTCCRB buffer operation with output compare, saw waves in up-counting, high output at GTCCRA compare match, and low output at cycle end

(1) 当GTCCRA或GTCCRB用作输出比较寄存器时

缓冲区传输发生在以下情况：

- 通过上溢或下溢进行缓冲区传输
  在锯齿波模式或事件计数操作中，在溢出（向上计数期间）或下溢（向下计数期间）时执行缓冲区传输。在三角波模式中，缓冲区传输在波谷（三角波PWM模式1）或波峰和波谷（三角波PWM模式2）处执行。
- 通过计数器清除缓冲区传输
  在锯齿波模式或事件计数操作中，在计数期间，缓冲区传输（与向上计数期间的溢出或向下计数期间的下溢相同）由计数器清零源执行，如第23.3节所示.2.1、GTPR寄存器缓冲操作。在三角波模式下，计数器清零不执行缓冲区传输。
- 强制缓冲转移
  当GTBER.CCRSWT位在计数操作停止时设置为1时，在锯齿波模式、事件计数操作和三角波模式下强制执行GTCCRA和GTCCRB寄存器缓冲传输。此外，从GTCCRD寄存器到临时寄存器A和从GTCCRF寄存器到临时寄存器B的缓冲区传输是在锯齿波1发射脉冲模式或三角波PWM模式3中执行的。

图23.22至图23.24显示了GTCCRA和GTCCRB缓冲操作的示例，图23.25显示了GTCCRA和GTCCRB缓冲操作的示例设置。

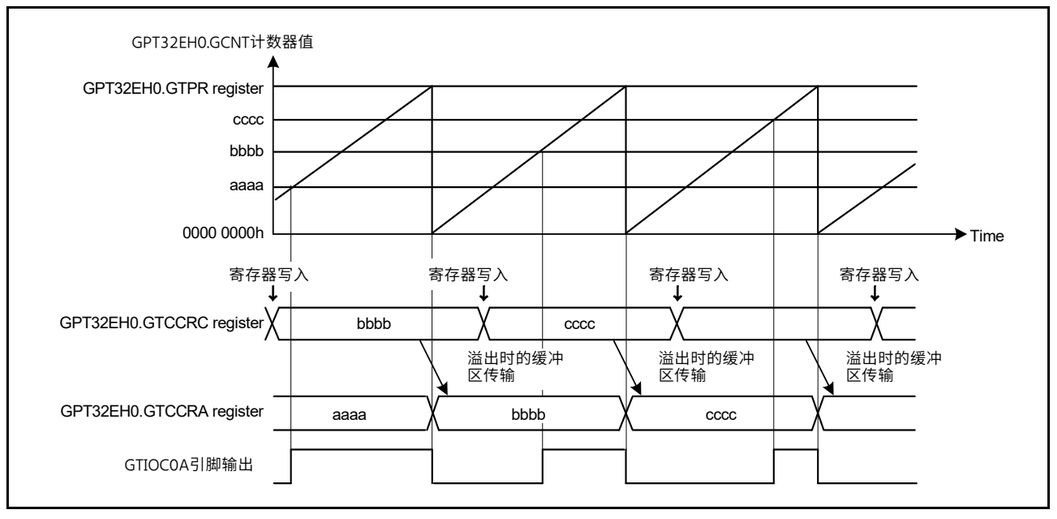


Figure 23.22 GTCCRA和GTCCRB缓冲器操作示例，输出比较、递增计数中的锯齿波、GTCCRA比较匹配时的高输出和周期结束时的低输出

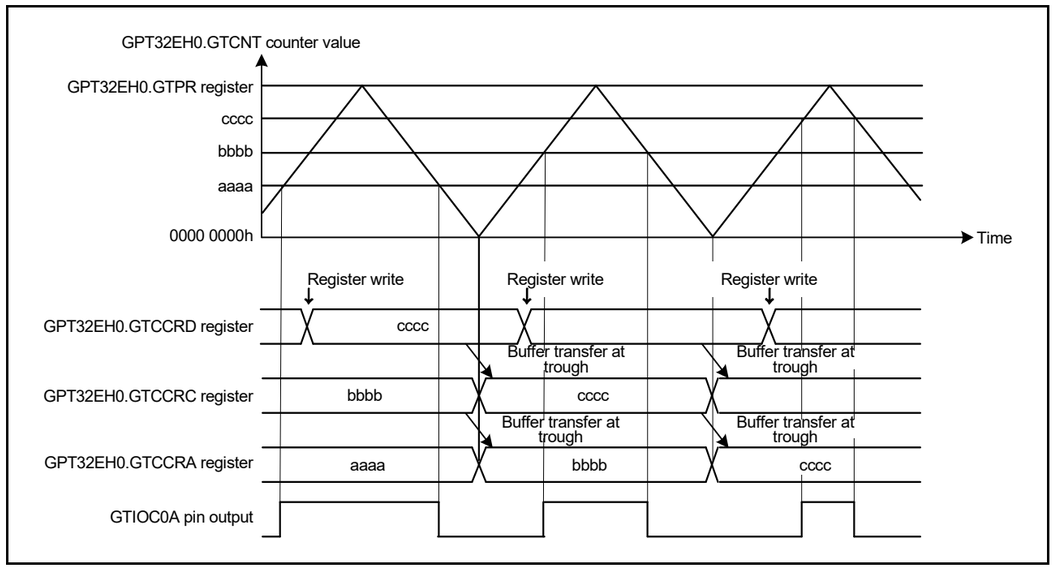


Figure 23.23 Example of GTCCRA and GTCCRB double buffer operation with output compare, triangle waves, buffer operation at trough, output toggled at GTCCRA compare match, and output retained at cycle end

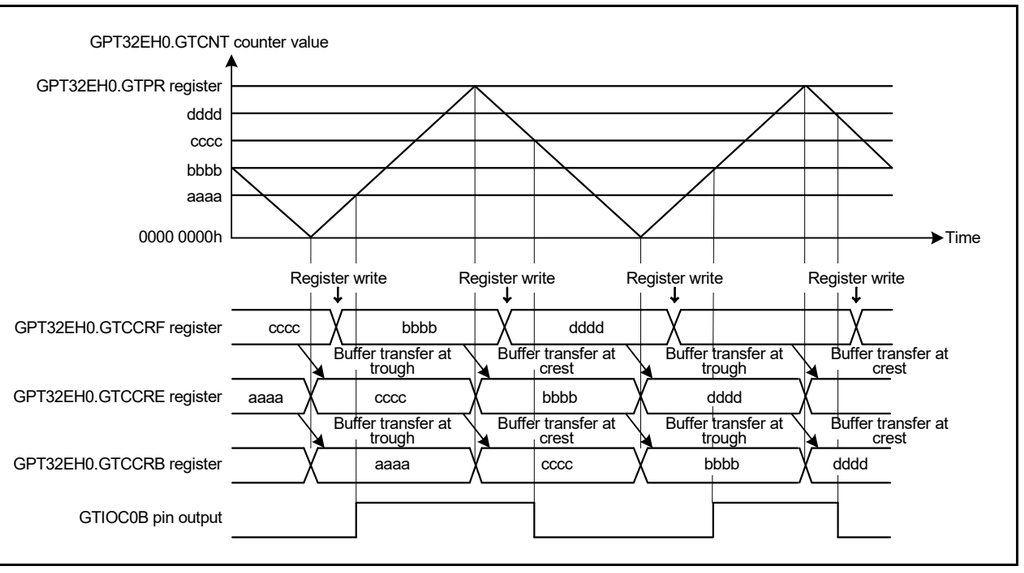


Figure 23.24 Example of GTCCRA and GTCCRB double buffer operation with output compare, triangle waves, buffer operation at both troughs and crests, output toggled at GTCCRB compare match, and output retained at cycle end

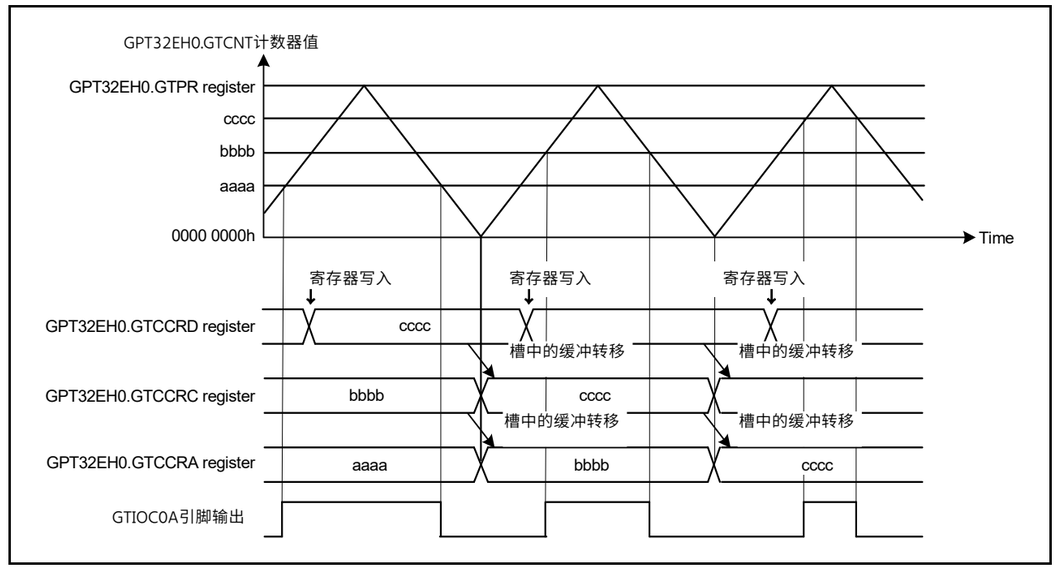


Figure 23.23 GTCCRA和GTCCRB双缓冲操作示例，输出比较、三角波、波谷缓冲操作、GTCCRA比较匹配时切换输出、循环结束时保留输出

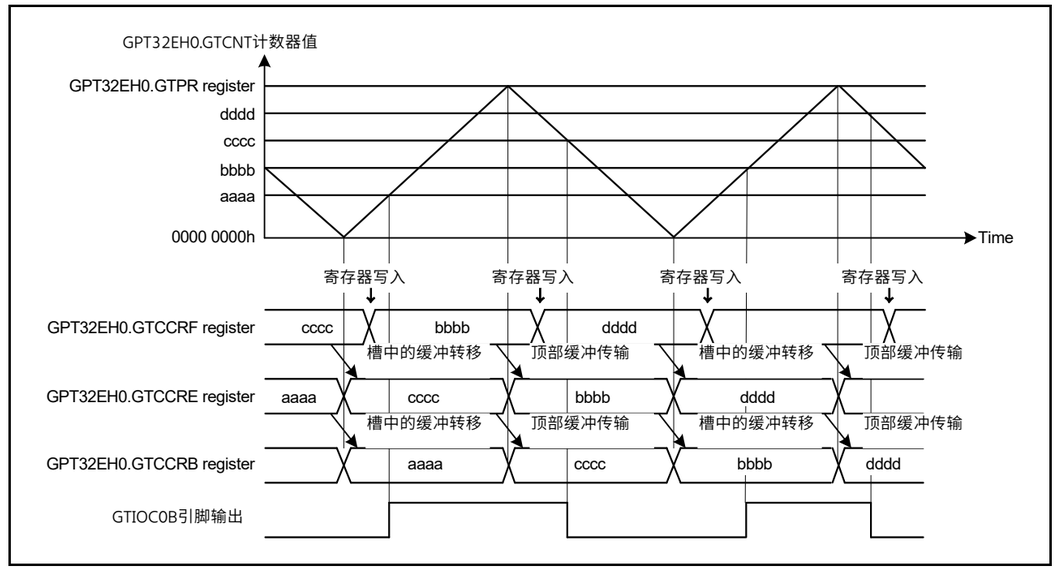
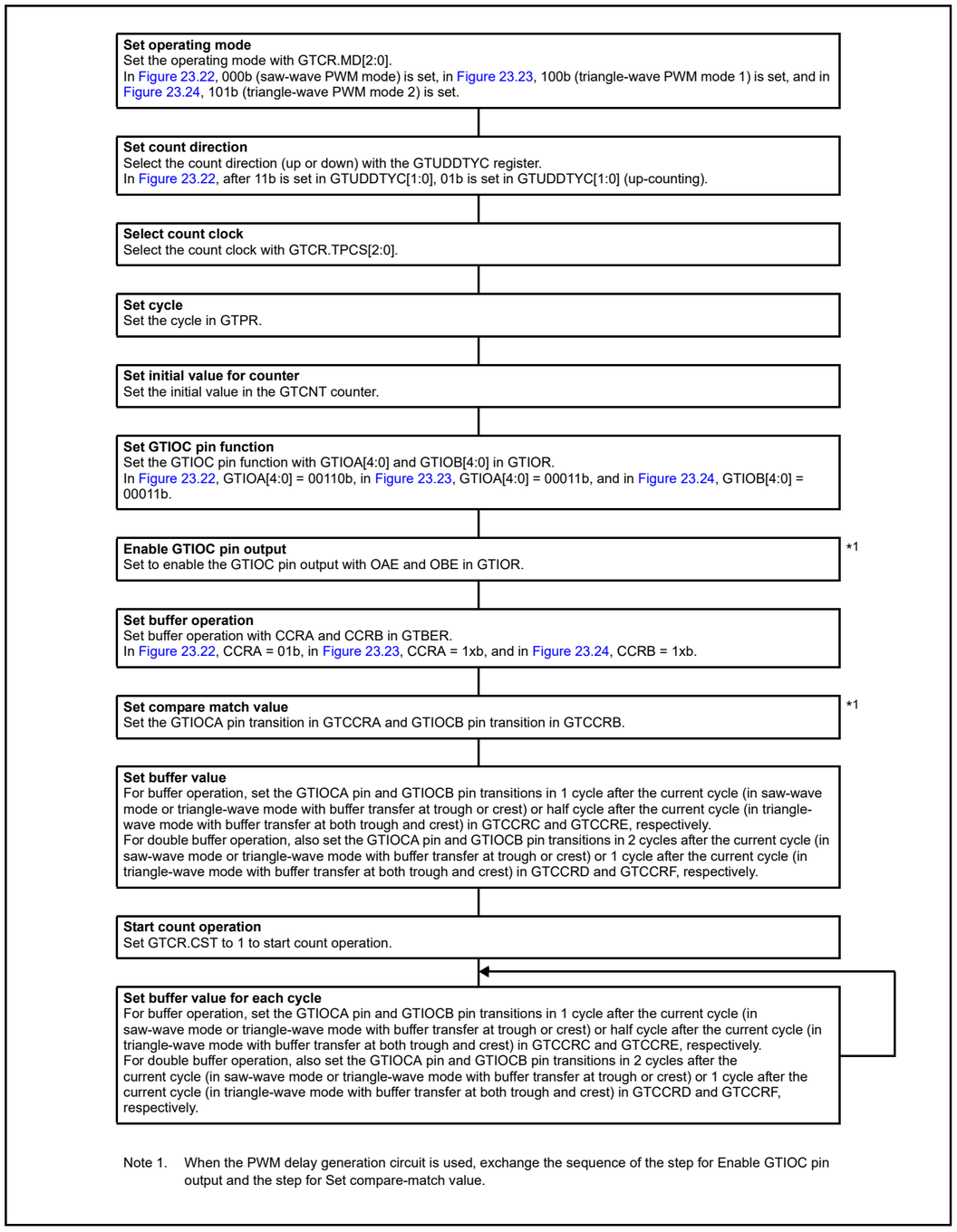


Figure 23.24 GTCCRA和GTCCRB双缓冲操作示例，输出比较、三角波、波谷和波峰缓冲操作、在GTCCRB比较匹配时切换输出以及在周期结束时保留输出



Note 1. When the PWM delay generation circuit is used, exchange the sequence of the step for Enable GTIOC pin output and the step for Set compare-match value.

Figure 23.25 Example setting for GTCCRA and GTCCRB buffer operation with output compare

Note 1. 当使用PWM延迟产生电路时，交换EnableGTIOCpinoutput的step和Setcompare-matchvalue的step。

Figure 23.25 带输出比较的GTCCRA和GTCCRB缓冲区操作设置示例

(2) When GTCCRA or GTCCRB functions as an input capture register

When an input capture is generated, the GTCNT counter value is transferred to GTCCRA and GTCCRB and the stored GTCCRA and GTCCRB register values are transferred to the buffer registers. In input capture operation, the buffer transfer is not performed by the counter clear.

Figure 23.26 and Figure 23.27 show examples of GTCCRA and GTCCRB buffer operation and Figure 23.28 shows an example setting for GTCCRA and GTCCRB buffer operation.

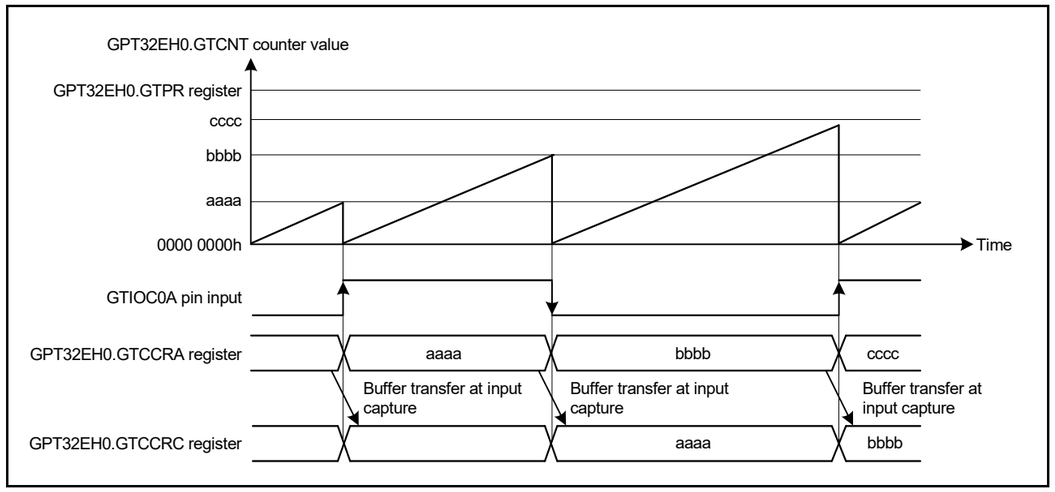


Figure 23.26 Example of GTCCRA and GTCCRB buffer operation with input capture at both edges of GTIOC0A input, saw waves in up-counting, and GTCNT counter cleared at both edges of GTIOC0A input

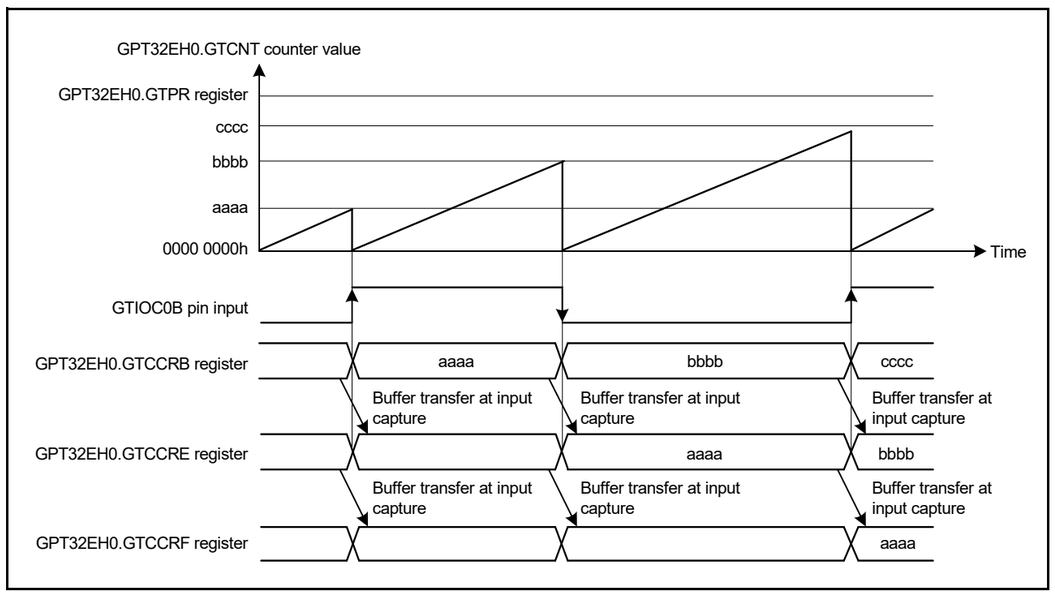


Figure 23.27 Example of GTCCRA and GTCCRB double buffer operation with input capture at both edges of GTIOC0B input, saw waves in up-counting, and GTCNT counter cleared at both edges of GTIOC0B input

(2) 当GTCCRA或GTCCRB用作输入捕捉寄存器时

当产生输入捕捉时，GTCNT计数器值被传送到GTCCRA和GTCCRB并存储GTCCRA和GTCCRB寄存器值被传送到缓冲寄存器。在输入捕捉操作中，缓冲区传输不是由计数器清零来执行的。

图23.26和图23.27显示了GTCCRA和GTCCRB缓冲操作的示例，图23.28显示了GTCCRA和GTCCRB缓冲操作的示例设置。

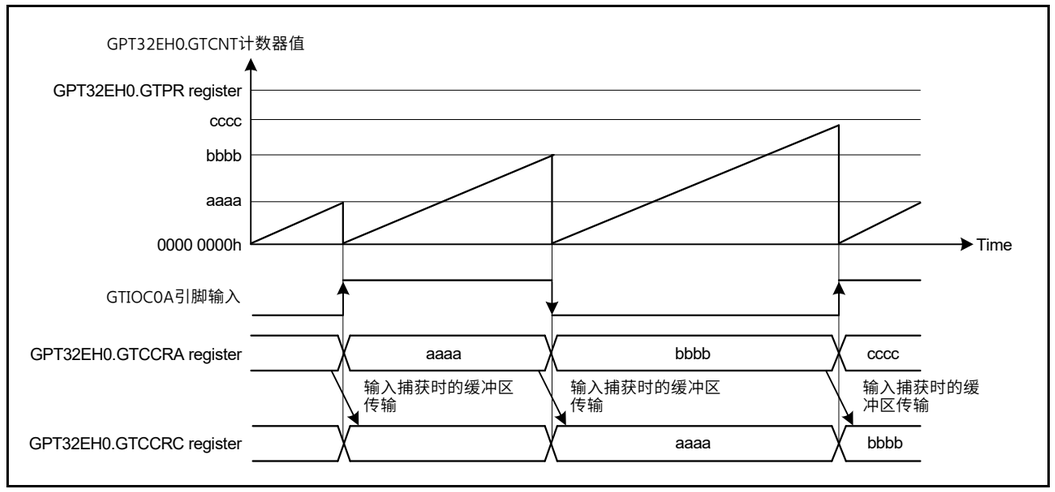


Figure 23.26 GTCCRA和GTCCRB缓冲器操作示例，在GTIOC0A输入的两个边沿进行输入捕获，在向上计数时看到锯齿波，并且在GTIOC0A输入的两个边沿清除GTCNT计数器

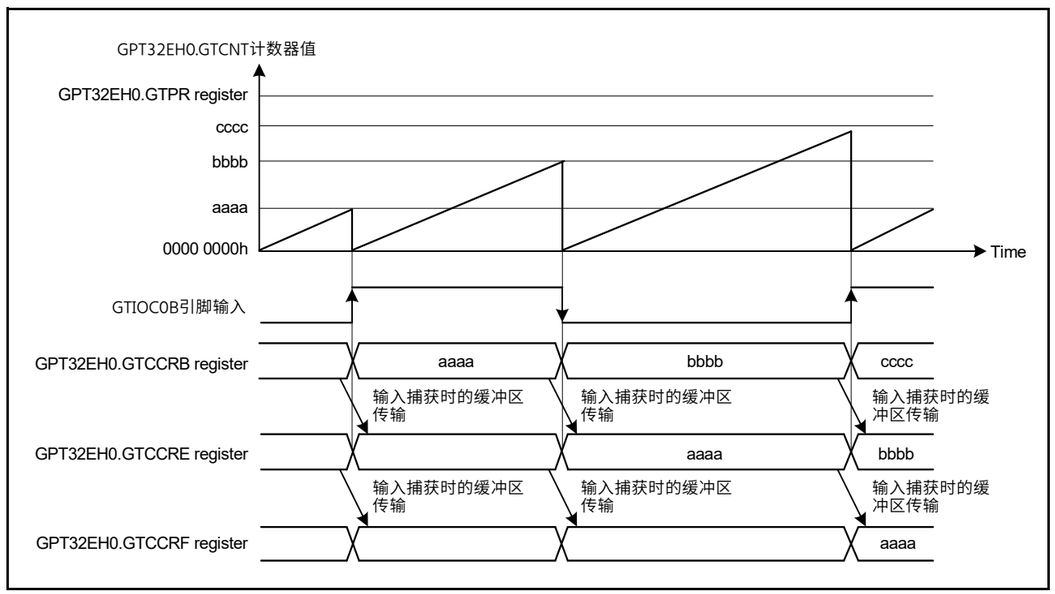


Figure 23.27 GTCCRA和GTCCRB双缓冲操作示例，在两个边沿进行输入捕获GTIOC0B输入，递增计数中的锯齿波，并且GTCNT计数器在GTIOC0B input

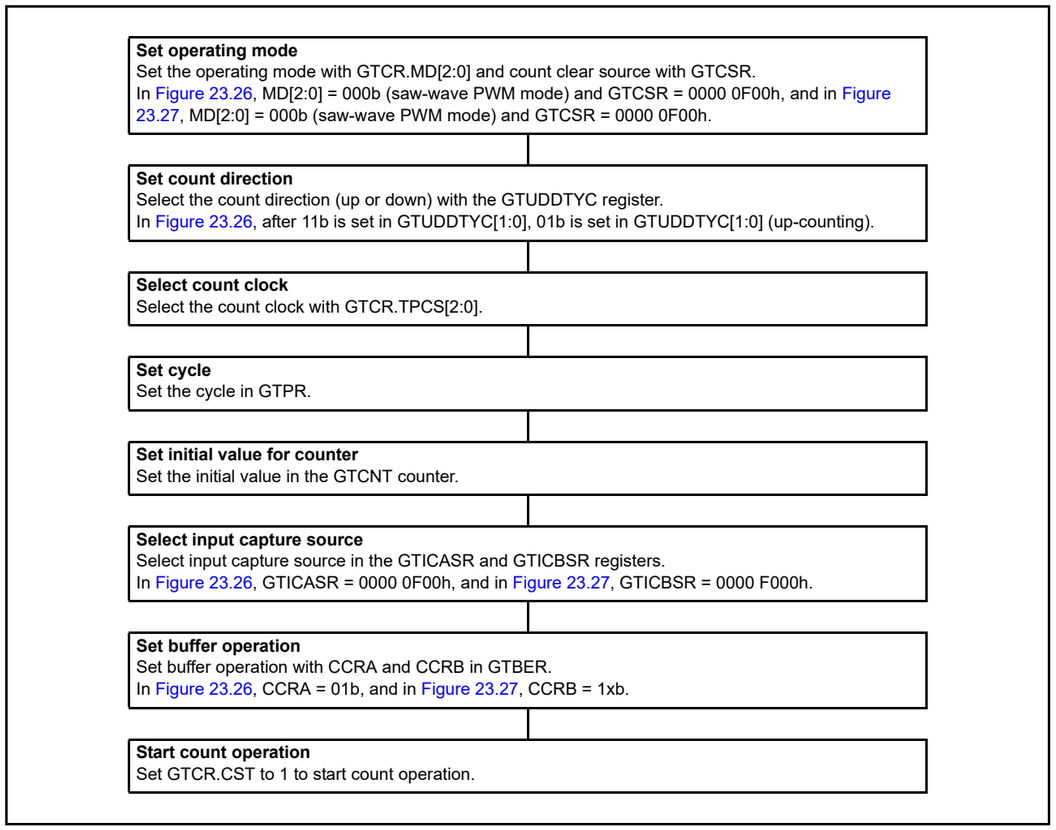


Figure 23.28 Example setting for GTCCRA and GTCCRB buffer operation with input capture

23.3.2.3 Buffer operation for GTADTRA and GTADTRB

GTADTBRA can function as the GTADTRA buffer register and GTADTDBRA can function as the GTADTBRA buffer register (double-buffer register for GTADTRA). Similarly, GTADTBRB can function as the GTADTRB buffer register and GTADTDBRB can function as the GTADTBRB buffer register (double-buffer register for GTADTRB).

To set GTADTRA or GTADTRB to function as a double buffer, set GTBER.ADTDA or GTBER.ADTDB to 1. For single buffer operation, set GTBER.ADTDA or GTBER.ADTDB to 0. To set GTADTRA or GTADTRB to not function as a buffer, set GTBER.ADTTA[1:0] or GTBER.ADTTB[1:0] to 00b.

The buffer transfer timing can be set with the GTBER.ADTTA[1:0] bits. For saw waves, overflows (during up-counting) or underflows (during down-counting) can be selected. For triangle waves, crests are selected when GTBER.ADTTA[1:0] = 01b, troughs are selected when GTBER.ADTTA[1:0] = 10b, and both crests and troughs are selected when GTBER.ADTTA[1:0] = 11b.

Figure 23.29 to Figure 23.31 show examples of GTADTRA and GTADTRB buffer operation and Figure 23.32 shows an example setting for GTDTRA and GTADTRB buffer operation.

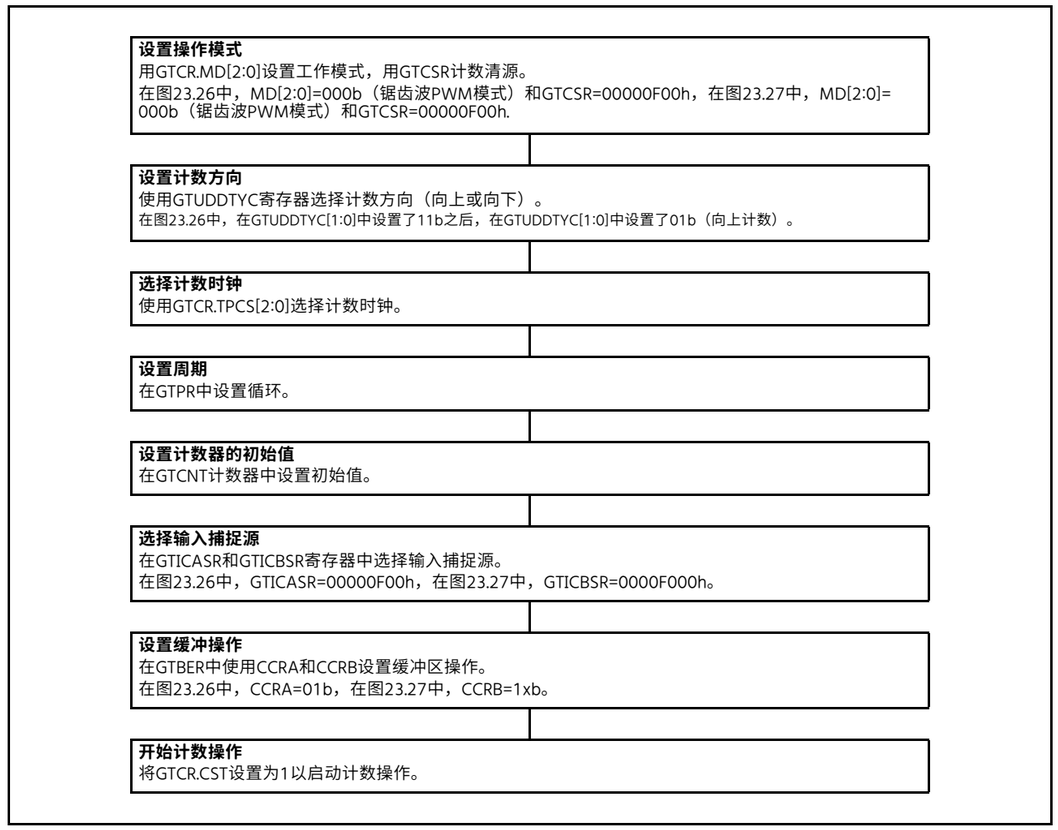


Figure 23.28 带输入捕获的GTCCRA和GTCCRB缓冲区操作设置示例

23.3.2.3 GTADTRA和GTADTRB的缓冲操作

GTADTBRA可以用作GTADTRA缓冲寄存器，GTADTBRA可以用作GTADTBRA缓冲寄存器（GTADTRA的双缓冲寄存器）。同样，GTADTBRB可以作为GTADTRB缓冲寄存器，GTADTDRBB可以作为GTADTBRB缓冲寄存器（GTADTRB的双缓冲寄存器）。

要将GTADTRA或GTADTRB设置为双缓冲区，请将GTBER.ADTDA或GTBER.ADTDB设置为1。对于单缓冲区操作，将GTBER.ADTDA或GTBER.ADTDB设置为0。要将GTADTRA或GTADTRB设置为不作为缓冲区，将GTBER.ADTTA[1:0]或GTBER.ADTTB[1:0]设置为00b。

可以使用GTBER.ADTTA[1:0]位设置缓冲区传输时序。对于锯齿波，可以选择上溢（向上计数期间）或下溢（向下计数期间）。对于三角波，当GTBER.ADTTA[1:0]=01b时选择波峰，当GTBER.ADTTA[1:0]=10b时选择波谷，当GTBER.ADTTA[1:0]时选择波峰和波谷=11b。

图23.29至图23.31显示了GTADTRA和GTADTRB缓冲操作的示例，图23.32显示了GTDTRA和GTADTRB缓冲操作的示例设置。

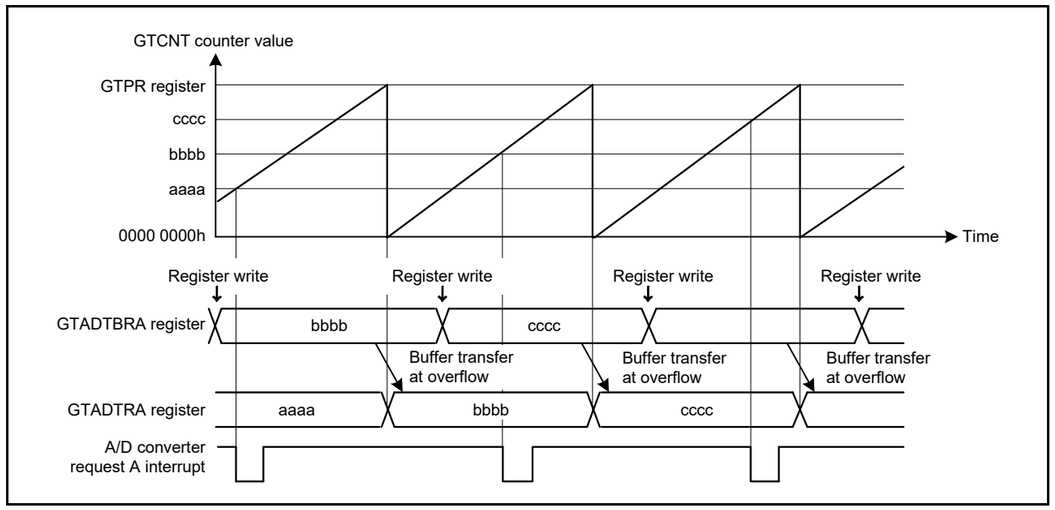


Figure 23.29 Example of GTADTRA and GTADTRB buffer operation with saw waves in up-counting and A/D converter start request interrupt generated by up-counting

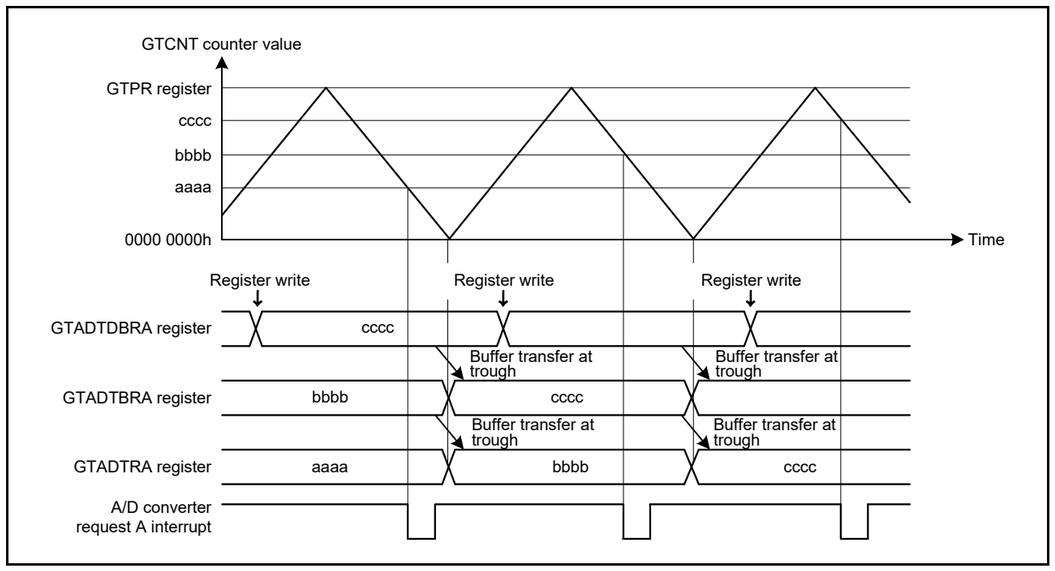


Figure 23.30 Example of GTADTRA and GTADTRB double buffer operation with triangle waves, buffer transfer at troughs, and A/D converter start request interrupt generated by down-counting

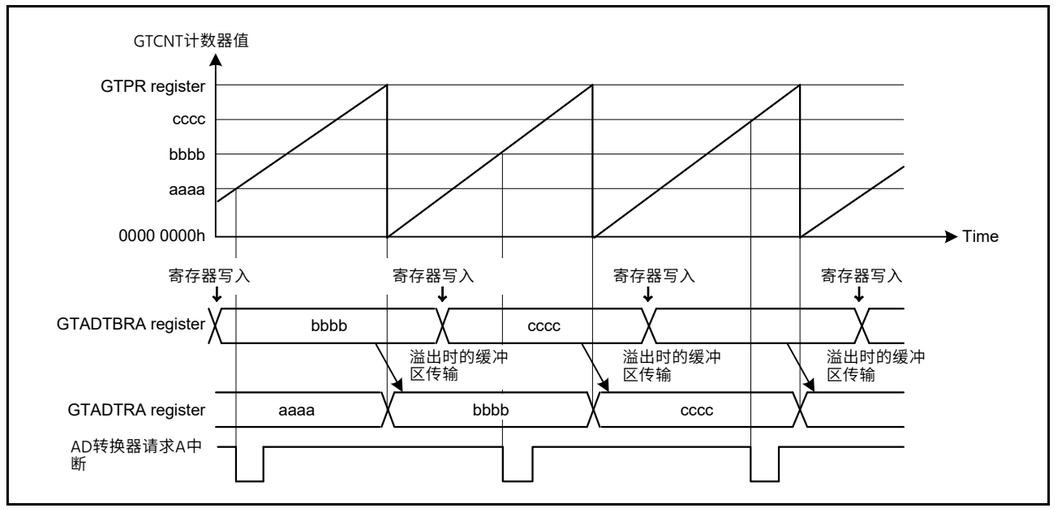


Figure 23.29 GTADTRA和GTADTRB缓冲器操作示例，在递增计数中使用锯齿波和递增计数产生的AD转换器启动请求中断

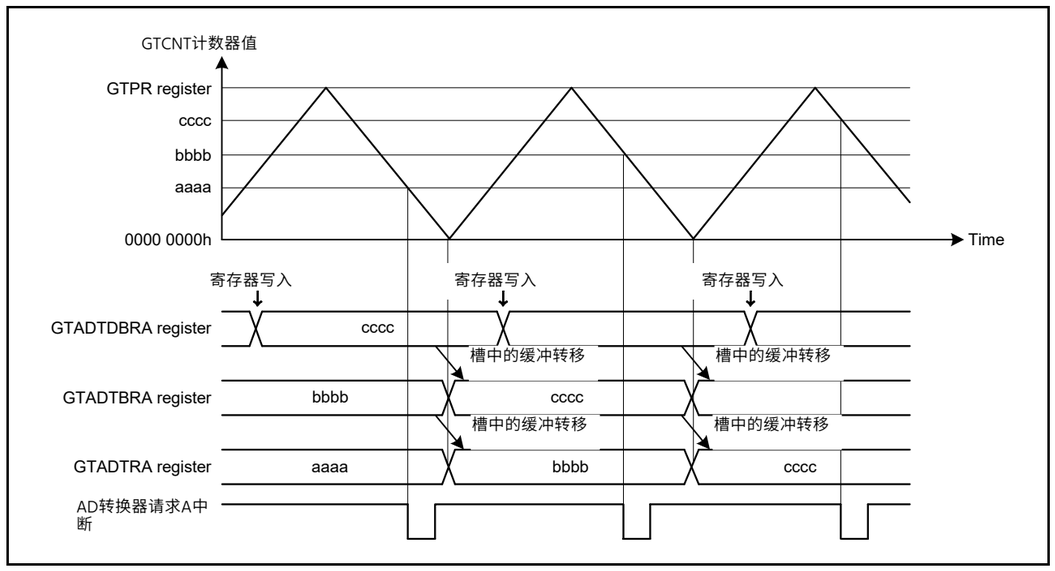


Figure 23.30 三角波的GTADTRA和GTADTRB双缓冲操作示例，波谷处的缓冲传输，以及由递减计数产生的AD转换器启动请求中断

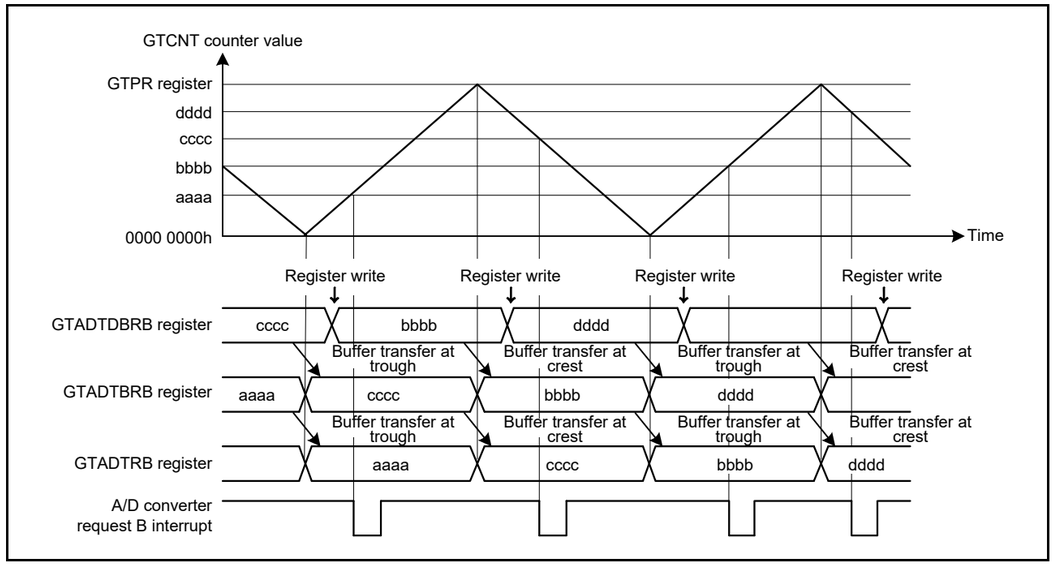


Figure 23.31 Example of GTADTRA and GTADTRB double buffer operation with triangle waves, buffer transfer at both troughs and crests, and A/D converter start request interrupt generated by both up- and down-counting

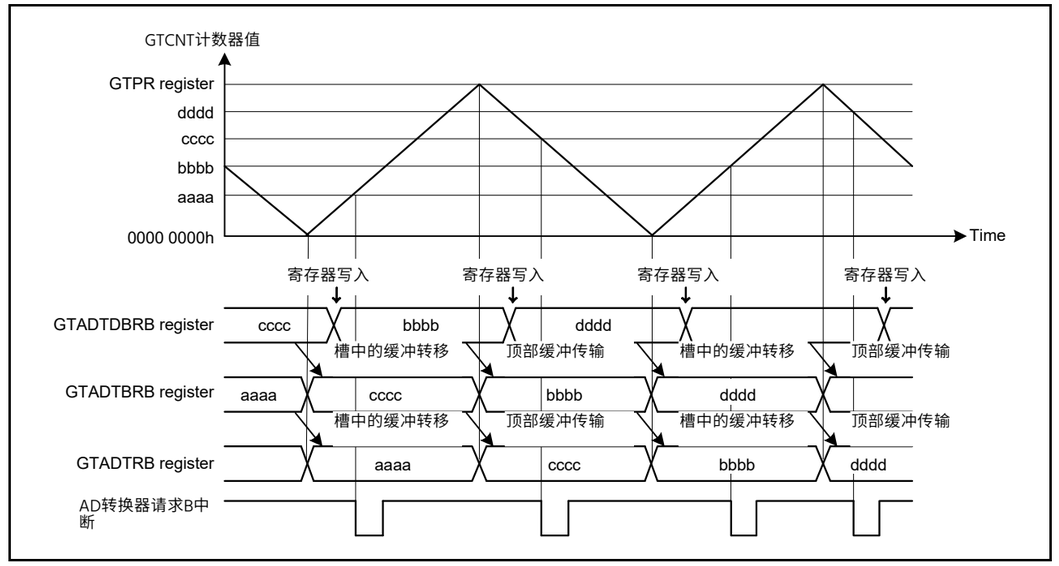


Figure 23.31 三角波的GTADTRA和GTADTRB双缓冲操作示例，波谷和波峰的缓冲传输，以及由加减计数产生的AD转换器启动请求中断

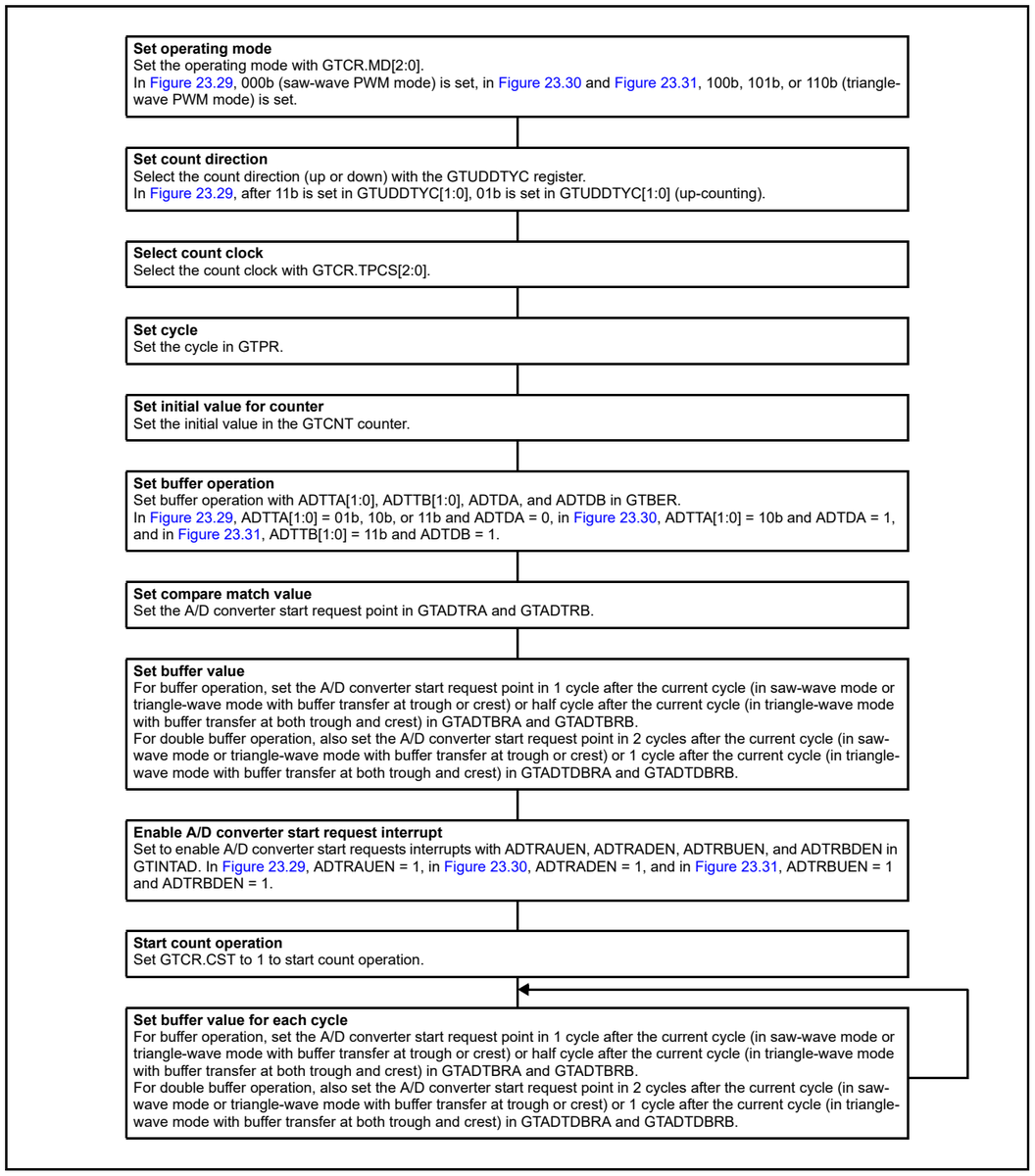


Figure 23.32 Example setting for GTADTRA and GTADTRB buffer operation

23.3.3 PWM Output Operating Mode

The GPT can output PWM waveforms to the GTIOCA or GTIOCB pin by a compare match between the GTCNT counter and GTCCRA or GTCCRB. By setting GTDTCR, GTDVU, and GTDVD, the compare match value for a negative-phase waveform with dead time can automatically be set to GTCCRB.

23.3.3.1 Saw-wave PWM mode

In saw-wave PWM mode, GTCNT performs saw-wave (half-wave) operation by setting the cycle in GTPR. A PWM

Figure 23.32 GTADTRA和GTADTRB缓冲操作的示例设置

23.3.3 PWM输出工作模式

通过GTCNT计数器与GTCCRA或GTCCRB之间的比较匹配，GPT可以将PWM波形输出到GTIOCA或GTIOCB引脚。通过设置GTDTCR、GTDVU和GTDVD，可以自动将带死区时间的负相波形的比较匹配值设置为GTCCRB。

23.3.3.1 Saw-wave PWM mode

在锯齿波PWM模式下，GTCNT通过在GTPR中设置周期来执行锯齿波（半波）操作。一个脉宽调制

waveform is output to the GTIOCA or GTIOCB pin when a GTCCRA or GTCCRB compare match occurs. The pin output value can be selected from low output, high output, or toggle output separately for a compare match and for the cycle end according to the GTIOR setting.

Figure 23.33 shows an example of saw-wave PWM mode operation, and Figure 23.34 shows an example setting for saw-wave PWM mode.

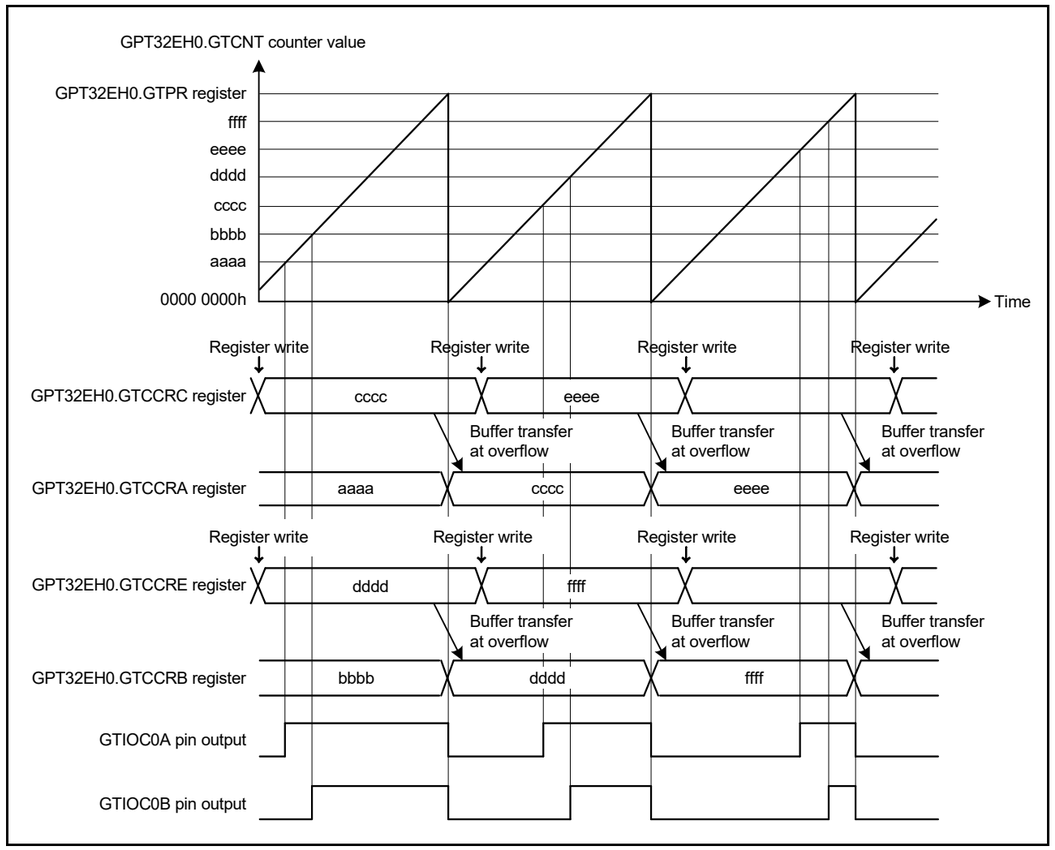


Figure 23.33 Example of saw-wave PWM mode operation with up-counting, buffer operation, high output at GTCCRA/GTCCRB compare match, and low output at cycle end

当GTCCRA或GTCCRB比较匹配发生时，波形输出到GTIOCA或GTIOCB引脚。引脚输出值可以根据GTIOR设置分别从低输出、高输出或切换输出中选择，用于比较匹配和循环结束。

图23.33显示了锯波PWM模式操作的示例，图23.34显示了锯波PWM模式的示例设置。

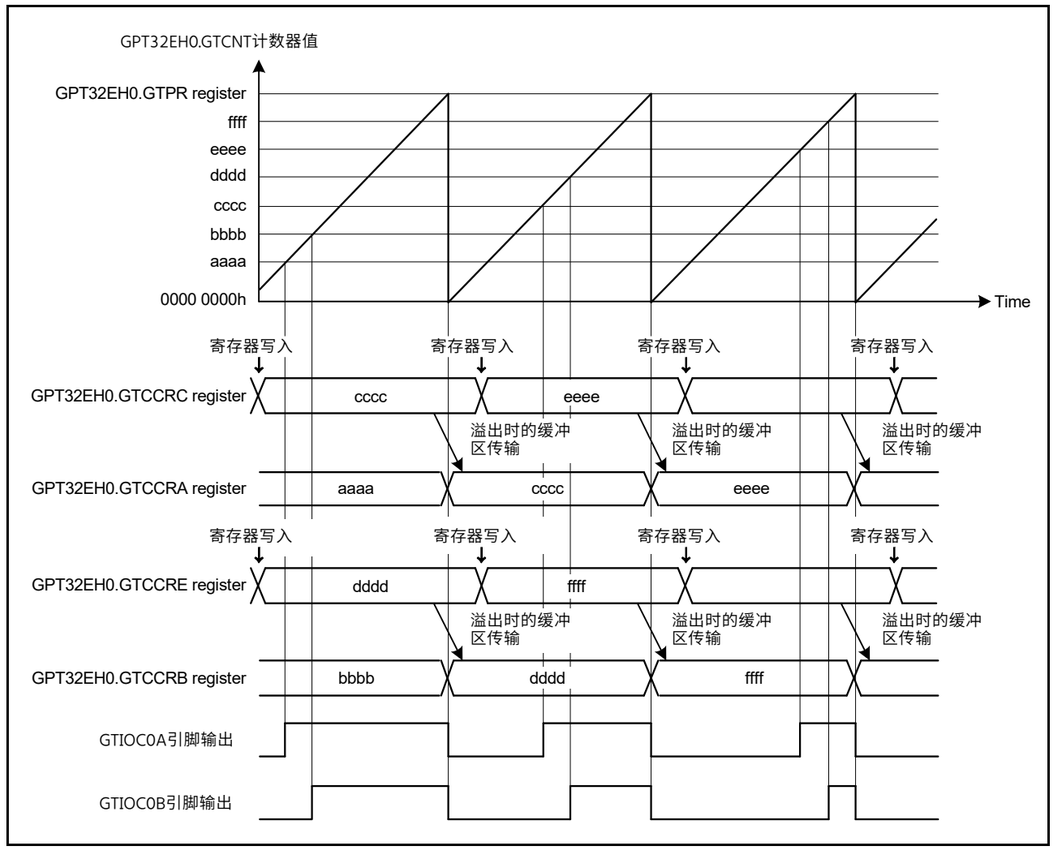
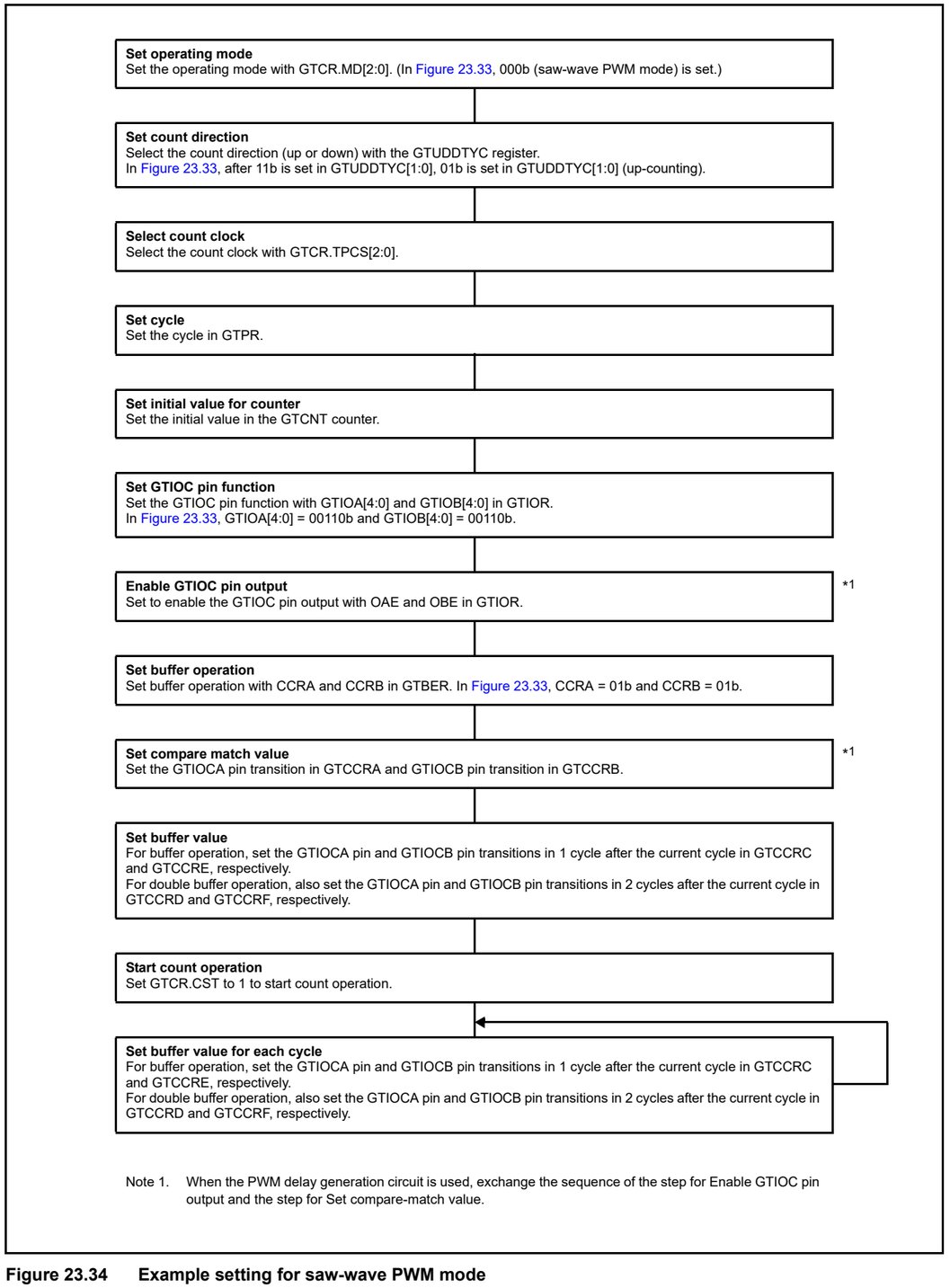
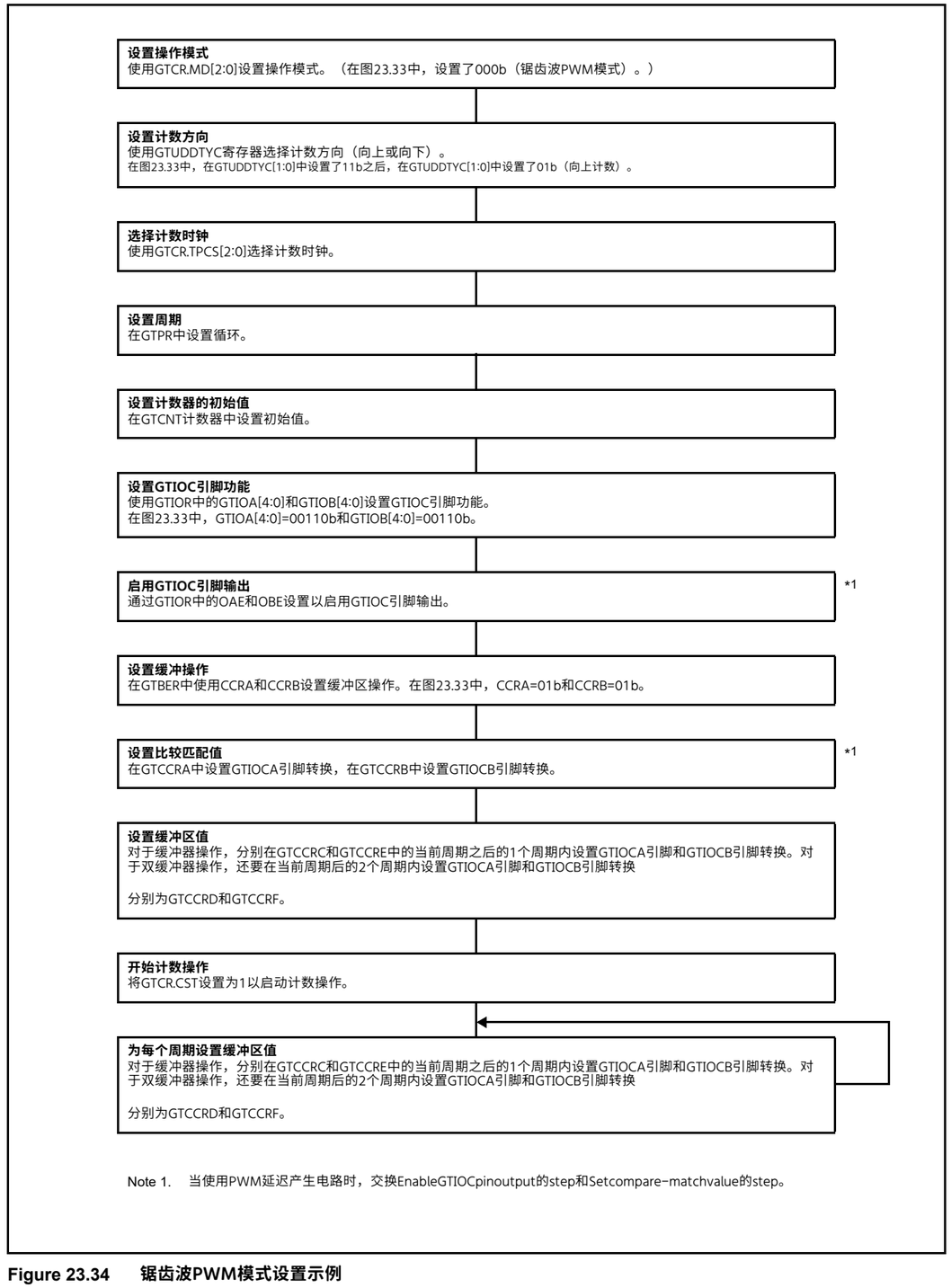


Figure 23.33 具有递增计数、缓冲操作、高输出的锯齿波PWM模式操作示例 GTCCRAGTCCRB比较匹配，循环结束时输出低



Note 1. When the PWM delay generation circuit is used, exchange the sequence of the step for Enable GTIOC pin output and the step for Set compare-match value.

Figure 23.34 Example setting for saw-wave PWM mode



Note 1. 当使用PWM延迟产生电路时，交换EnableGTIOCpinoutput的step和Setcompare-matchvalue的step。

Figure 23.34 锯齿波PWM模式设置示例

23.3.3.2 Saw-wave one-shot pulse mode

The saw-wave one-shot pulse mode is a mode in which the cycle is set in GTPR. The GTCNT counter performs saw-wave (half-wave) operation and a PWM waveform is output to the GTIOCA or GTIOCB pin at a compare match of GTCCRA or GTCCRB with buffer operation fixed.

Buffer operation in saw-wave one-shot pulse mode is different from the usual buffer operation. Buffer transfer is performed from:

- GTCCRC to GTCCRA at the cycle end
- GTCCRE to GTCCRB at the cycle end
- GTCCRD to temporary register A at the cycle end
- GTCCRF to temporary register B at the cycle end
- Temporary register A to GTCCRA at a GTCCRA compare match
- Temporary register B to GTCCRB at a GTCCRB compare match.

The pin output value can be selected from low output, high output, or toggle output separately for a compare match and the cycle end according to the GTIOR setting. When the GTBER.CCRSWT bit is set to 1 while the count operation is stopped, the buffer is transferred forcibly from the GTCCRD register to temporary register A and from the GTCCRF register to temporary register B. By setting GTDTCR, GTDVU, and GTDVD, a compare match value for a negative-phase waveform with dead time can automatically be set to GTCCRB.

Figure 23.35 shows an example of saw-wave one-shot pulse mode operation, and Figure 23.36 shows an example setting for saw-wave one-shot pulse mode.

23.3.3.2 锯波单发脉冲模式

锯齿波单发脉冲模式是在GTPR中设置周期的模式。GTCNT计数器执行锯齿波（半波）操作，并且在GTCCRA或GTCCRB的比较匹配时将PWM波形输出到GTIOCA或GTIOCB引脚，且缓冲器操作固定。

锯波单次脉冲模式中的缓冲操作不同于通常的缓冲操作。缓冲区传输从以下位置执行：

- 循环结束时GTCCRC到GTCCRA
- 循环结束时GTCCRE到GTCCRB
- GTCCRD在循环结束时到临时寄存器A
- GTCCRF在循环结束时到临时寄存器B
- 在GTCCRA比较匹配时将临时寄存器A发送到GTCCRA
- 在GTCCRB比较匹配时，临时寄存器B到GTCCRB。

引脚输出值可以根据GTIOR设置分别从低输出、高输出或切换输出中选择，以进行比较匹配和循环结束。当在计数操作停止时GTBER.CCRSWT位设置为1时，缓冲区被强制从GTCCRD寄存器传送到临时寄存器A，并从GTCCRF寄存器传送到临时寄存器B。通过设置GTDTCR、GTDVU和GTDVD，a带有死区时间的负相位波形的比较匹配值可以自动设置为GTCCRB。

图23.35显示了锯齿波单次脉冲模式操作的示例，图23.36显示了锯齿波单次脉冲模式设置的示例。

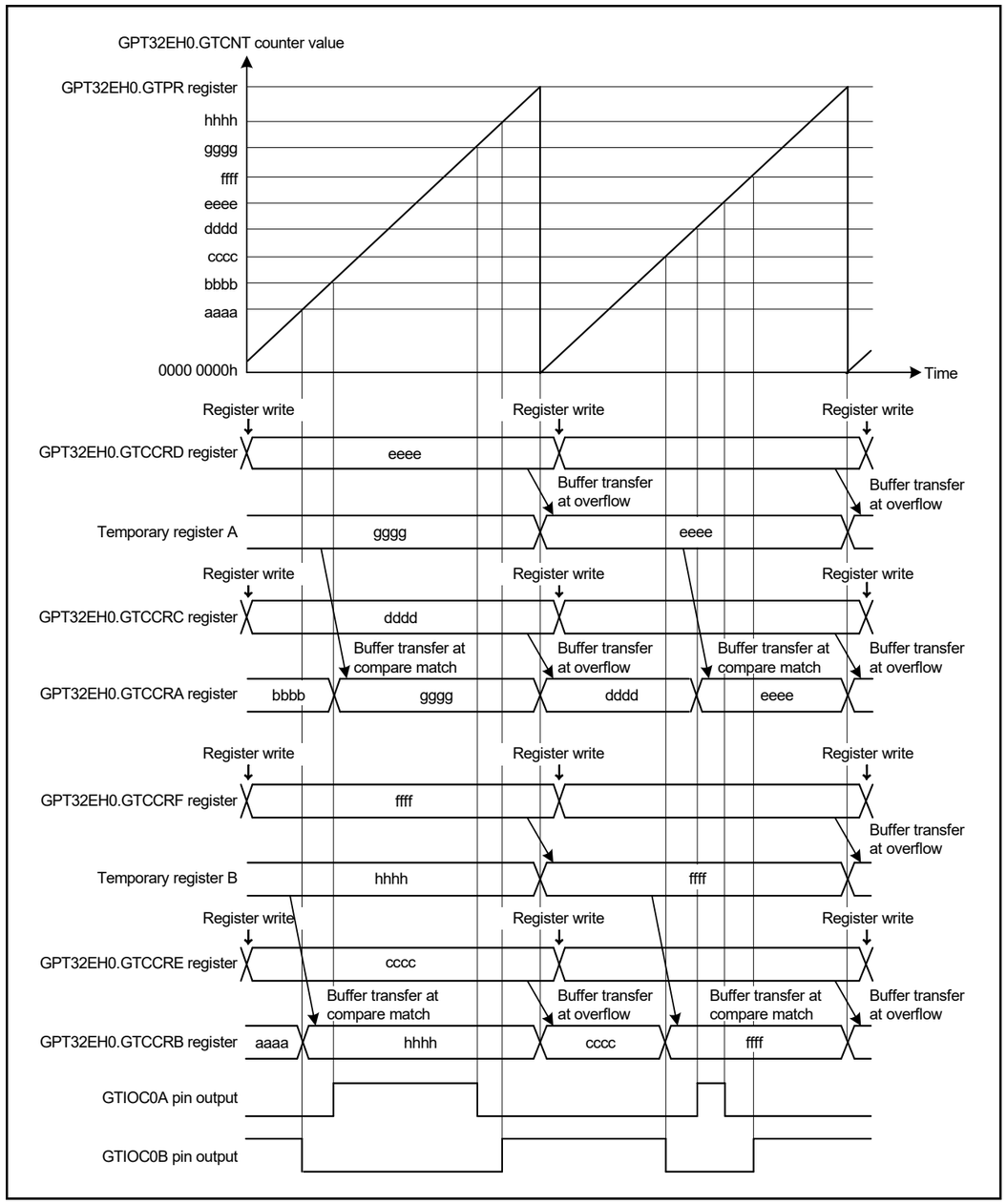


Figure 23.35 Example of saw-wave one-shot pulse mode operation with up-counting, low output from the GTIOC0A pin and high output from the GTIOC0B pin at count start, output toggled at GTCCRA/GTCCRB compare match, and output retained at cycle end

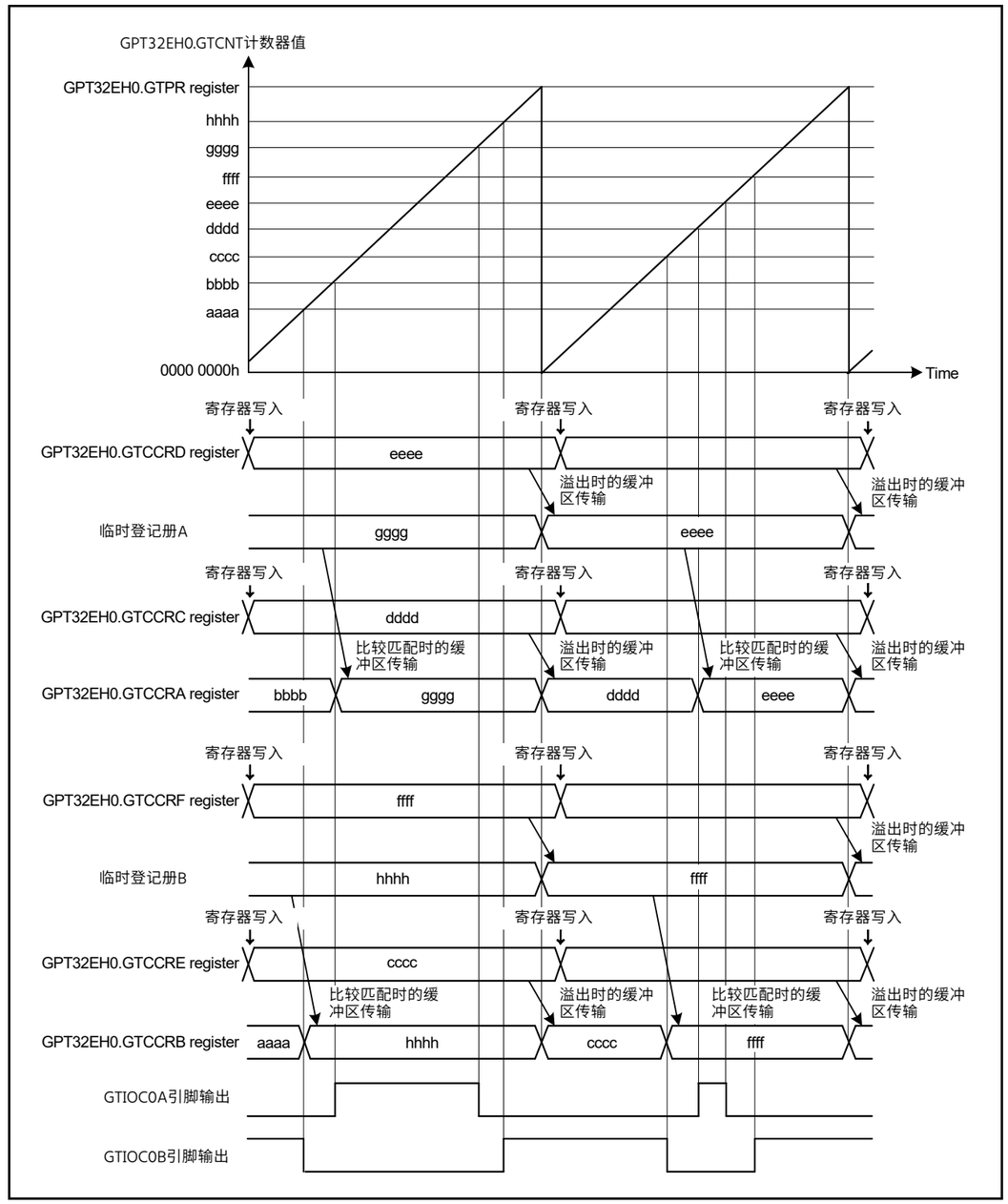
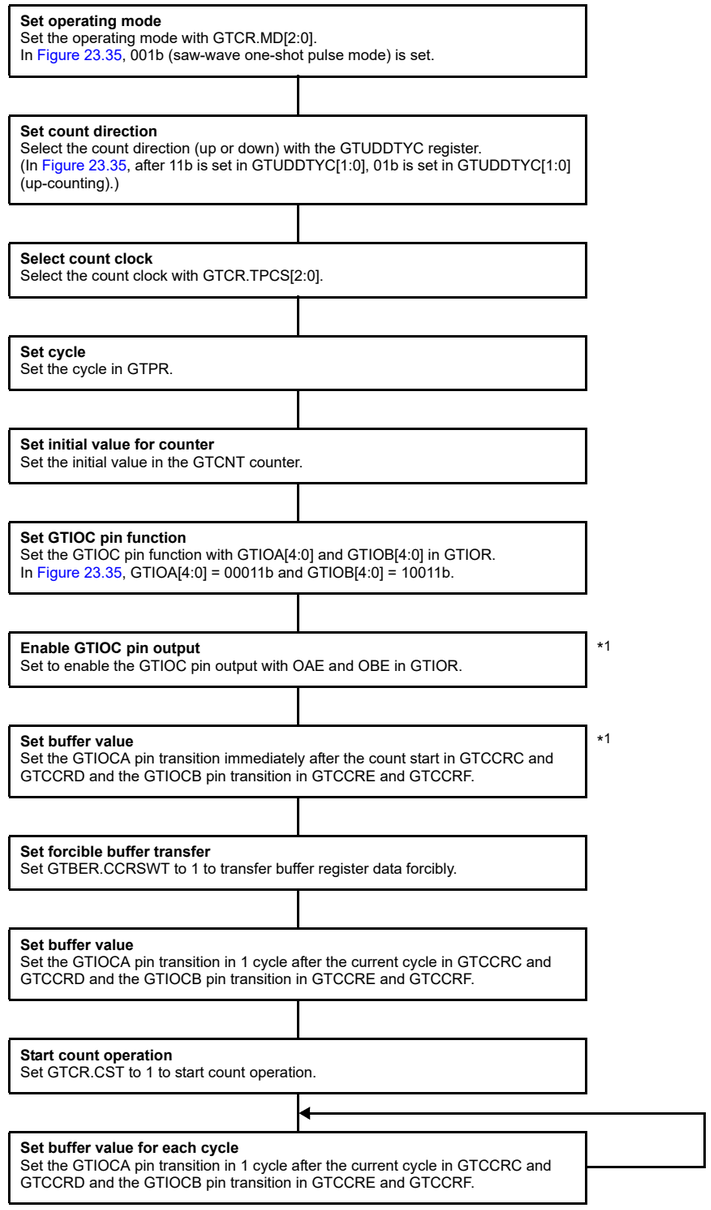
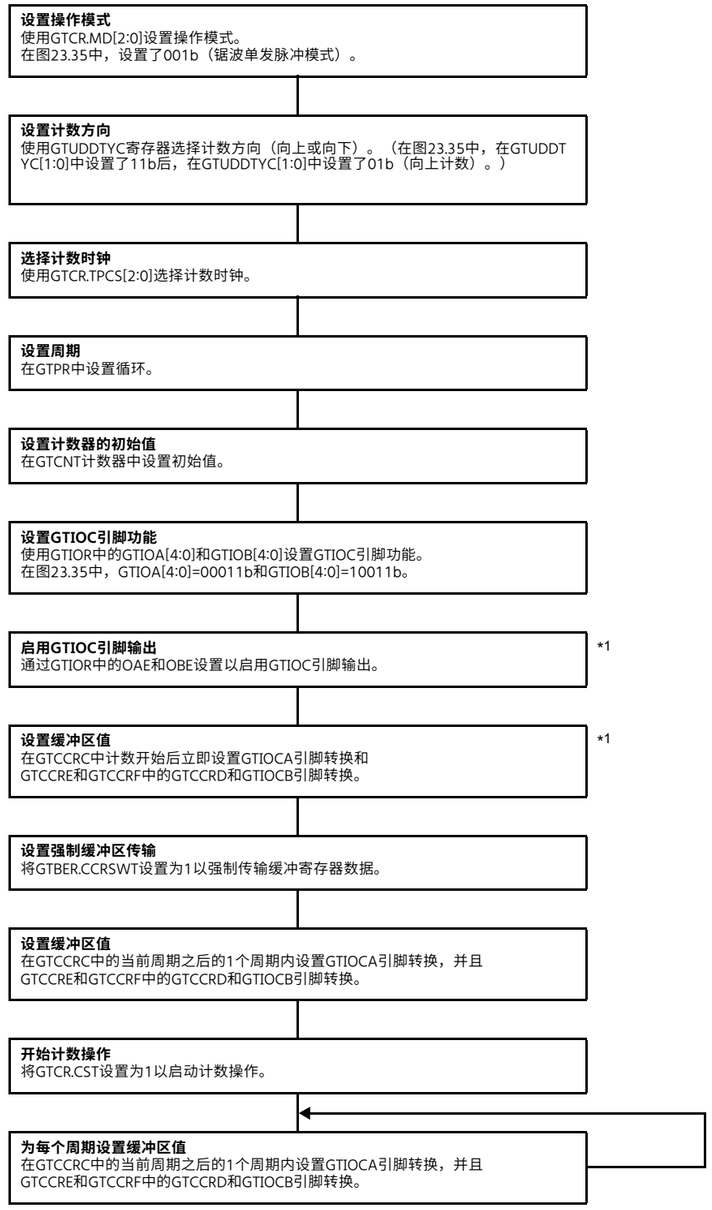


Figure 23.35 具有递增计数、低输出的锯齿波单次脉冲模式操作示例 GTIOC0A引脚和GTIOC0B引脚在计数开始时的高电平输出，输出在 GTCCRAGTCCRB比较匹配，并在循环结束时保留输出



Note 1. When the PWM delay generation circuit is used, exchange the sequence of the step for Enable GTIOC pin output and the step for Set buffer value.

Figure 23.36 Example setting for saw-wave one-shot pulse mode



Note 1. 当使用PWM延迟产生电路时，交换EnableGTIOCpinoutput的step和Setbuffervalue的step。

Figure 23.36 锯波单发脉冲模式设置示例

23.3.3.3 Triangle-wave PWM mode 1 (32-bit transfer at trough)

The triangle-wave PWM mode 1 is a mode in which the cycle is set in GTPR. The GTCNT counter performs triangle-wave (full-wave) operation, and a PWM waveform is output to the GTIOCA or GTIOCB pin when a GTCCRA or GTCCRB compare match occurs. Buffer transfer is performed at the trough. The pin output value can be selected from low output, high output, or toggle output separately for a compare match and for the cycle end based on the GTIOR setting.

By setting GTDTCR, GTDVU, and GTDVD, a compare match value for a negative-phase waveform with dead time can automatically be set to GTCCRB.

Figure 23.37 shows an example of a triangle-wave PWM mode 1 operation, and Figure 23.38 shows an example setting for a triangle-wave PWM mode 1.

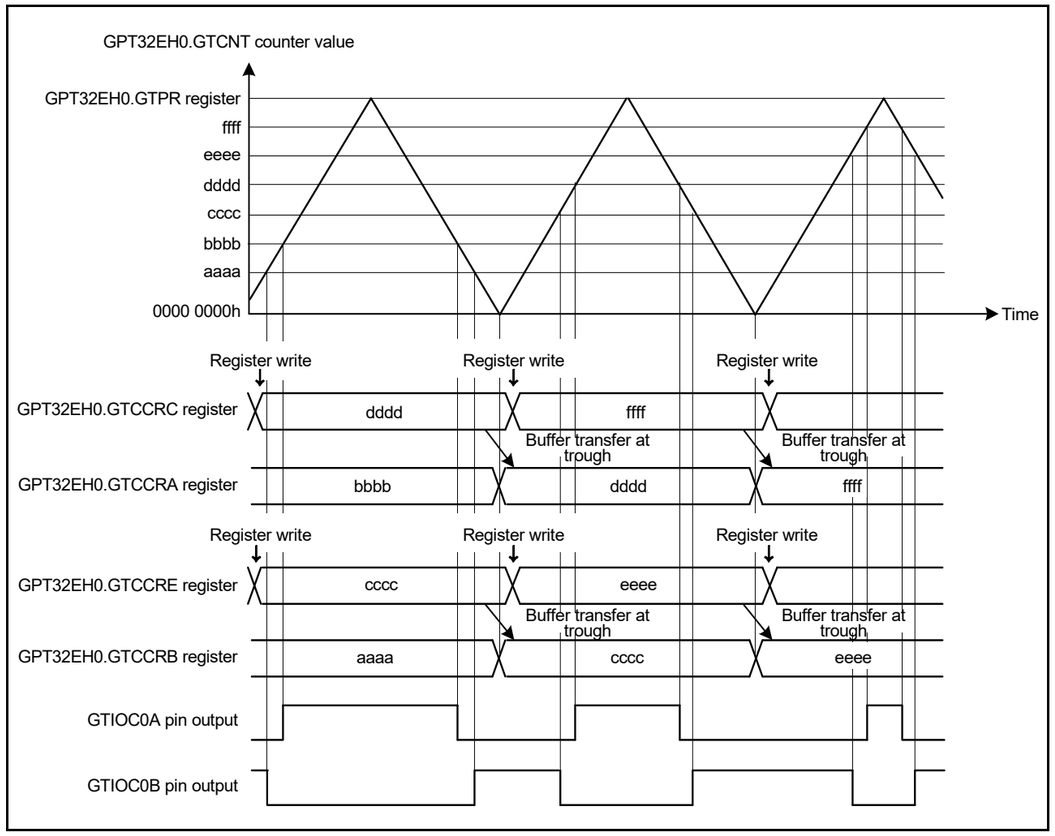


Figure 23.37 Example of triangle-wave PWM mode 1 operation with buffer operation, low output from the GTIOC0A pin and high output from the GTIOC0B pin at count start, output toggled at GTCCRA/GTCCRB register compare match, and output retained at cycle end

23.3.3.3 三角波PWM模式1（波谷32位传输）

三角波PWM模式1是在GTPR中设定周期的模式。GTCNT计数器执行三角波（全波）操作，当发生GTCCRA或GTCCRB比较匹配时，PWM波形将输出到GTIOCA或GTIOCB引脚。在槽中进行缓冲转移。引脚输出值可以根据GTIOR设置分别从低输出、高输出或切换输出中选择，用于比较匹配和循环结束。

通过设置GTDTCR、GTDVU和GTDVD，可以自动将带死区时间的负相位波形的比较匹配值设置为GTCCRB。

图23.37显示了三角波PWM模式1操作的示例，图23.38显示了三角波PWM模式1的示例设置。

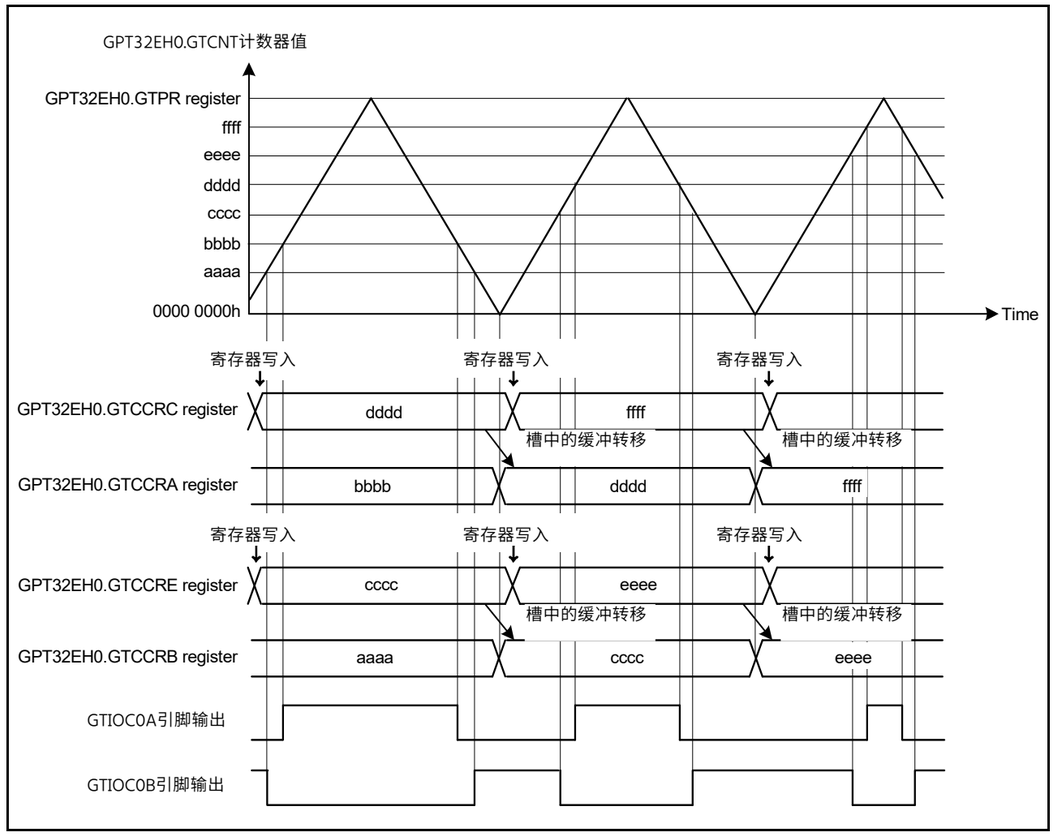
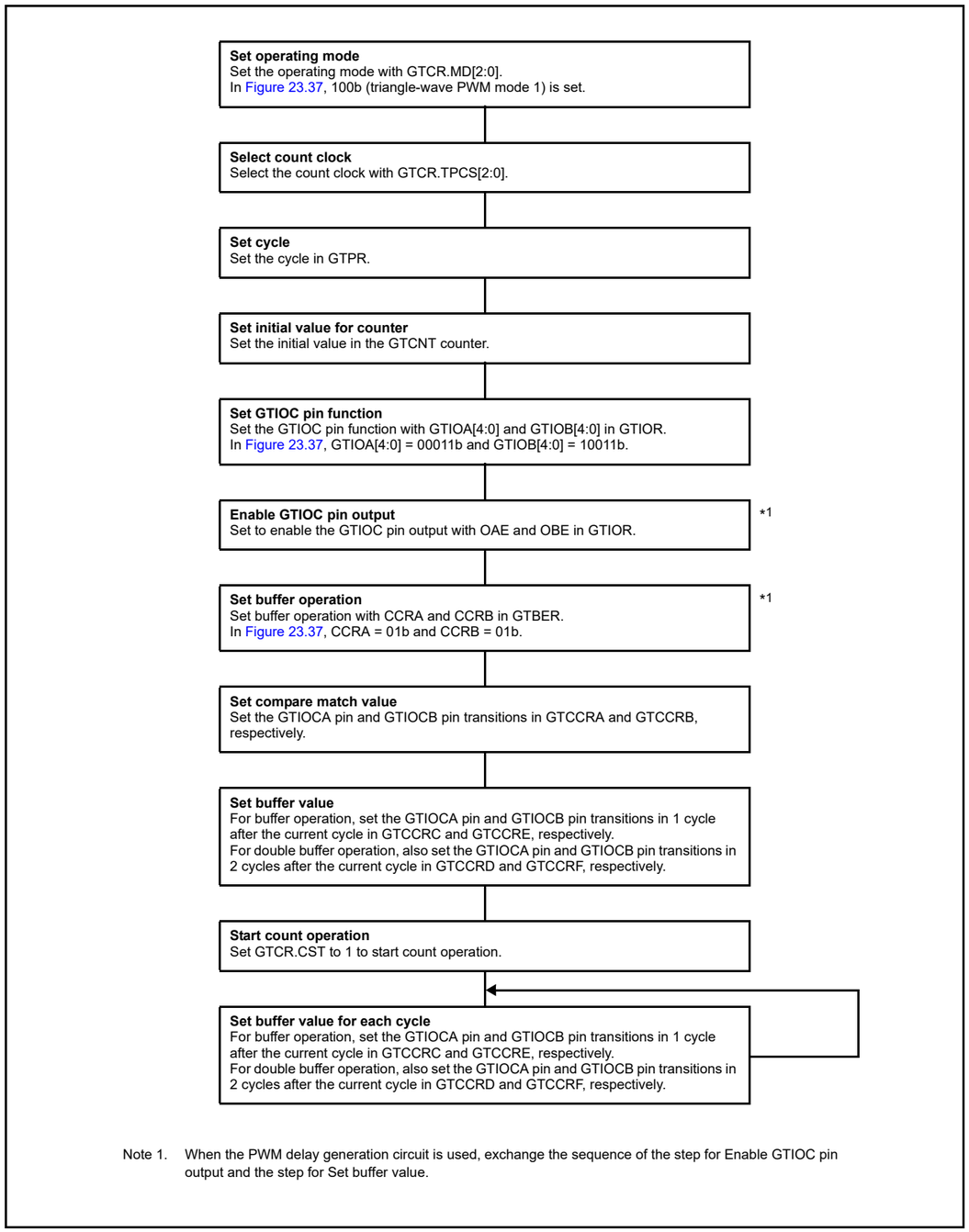
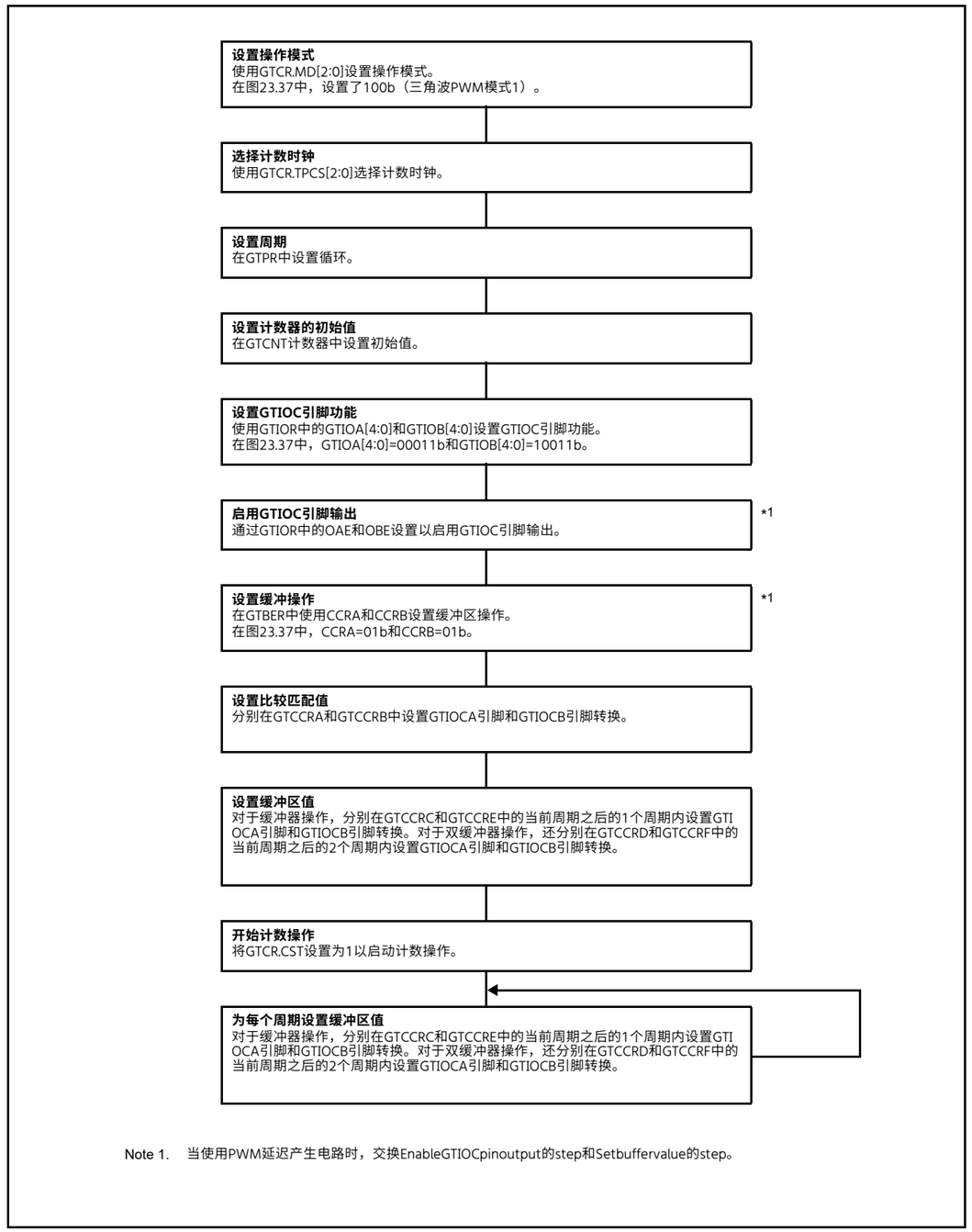


Figure 23.37 带缓冲操作的三角波PWM模式1操作示例，从GTIOC0A引脚和GTIOC0B引脚在计数开始时的高电平输出，输出在GTCCRAGTCCRB寄存器比较匹配，并在循环结束时保留输出



Note 1. When the PWM delay generation circuit is used, exchange the sequence of the step for Enable GTIOC pin output and the step for Set buffer value.

Figure 23.38 Example setting for triangle-wave PWM mode 1



Note 1. 当使用PWM延迟产生电路时，交换EnableGTIOCpinoutput的step和Setbuffervalue的step。

Figure 23.38 三角波PWM模式1的设置示例

23.3.3.4 Triangle-wave PWM mode 2 (32-bit transfer at crest and trough)

Similarly to triangle-wave PWM mode 1, in triangle-wave PWM mode 2 the cycle is set in GTPR. The GTCNT counter performs triangle-wave (full-wave) operation, and a PWM waveform is output to the GTIOCA or GTIOCB pin when a GTCCRA or GTCCRB compare match occurs. The buffer transfer is performed at both crests and troughs. The pin output value can be selected from low output, high output, or toggle output separately for a compare match and for the cycle end based on the GTIOR setting.

By setting GTDTCR, GTDVU, and GTDVD, a compare match value for a negative-phase waveform with dead time can automatically be set to GTCCRB.

Figure 23.39 shows an example of triangle-wave PWM mode 2 operation, and Figure 23.40 shows an example setting for triangle-wave PWM mode 2.

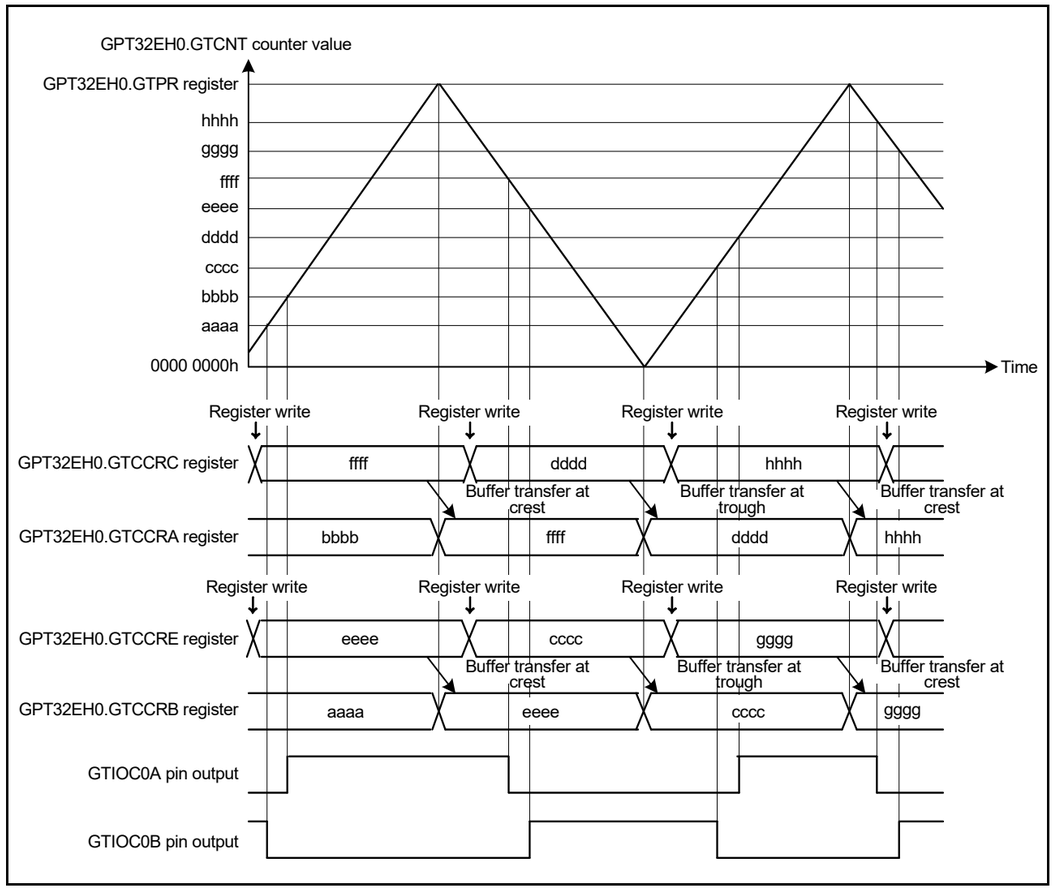


Figure 23.39 Example of triangle-wave PWM mode 2 operation with buffer operation, low output from the GTIOC0A pin and high output from the GTIOC0B pin at count start, output toggled at GTCCRA/GTCCRB compare match, and output retained at cycle end

23.3.3.4 三角波PWM模式2（波峰和波谷32位传输）

与三角波PWM模式1类似，在三角波PWM模式2中，周期在GTPR中设置。GTCNT计数器执行三角波（全波）操作，当发生GTCCRA或GTCCRB比较匹配时，PWM波形将输出到GTIOCA或GTIOCB引脚。缓冲转移在波峰和波谷进行。引脚输出值可以根据GTIOR设置分别从低输出、高输出或切换输出中选择，用于比较匹配和循环结束。

通过设置GTDTCR、GTDVU和GTDVD，可以自动将带死区时间的负相位波形的比较匹配值设置为GTCCRB。

图23.39显示了三角波PWM模式2操作的示例，图23.40显示了三角波PWM模式2的示例设置。

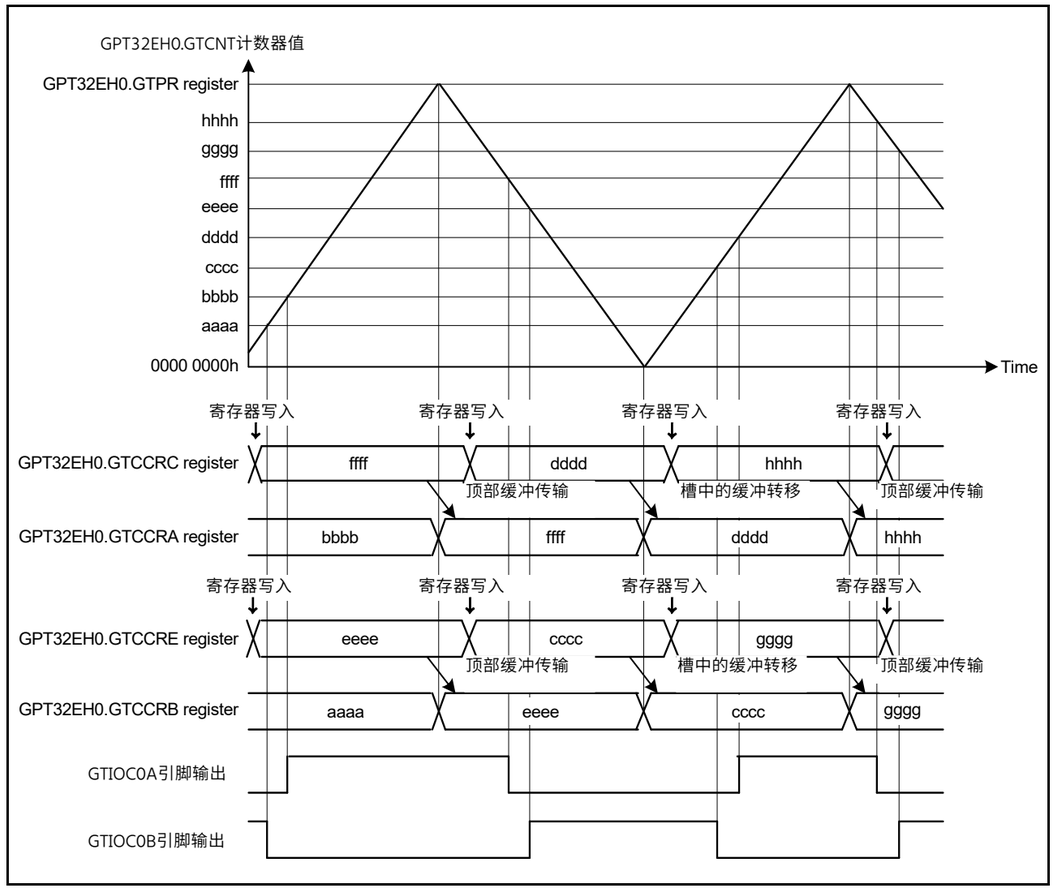
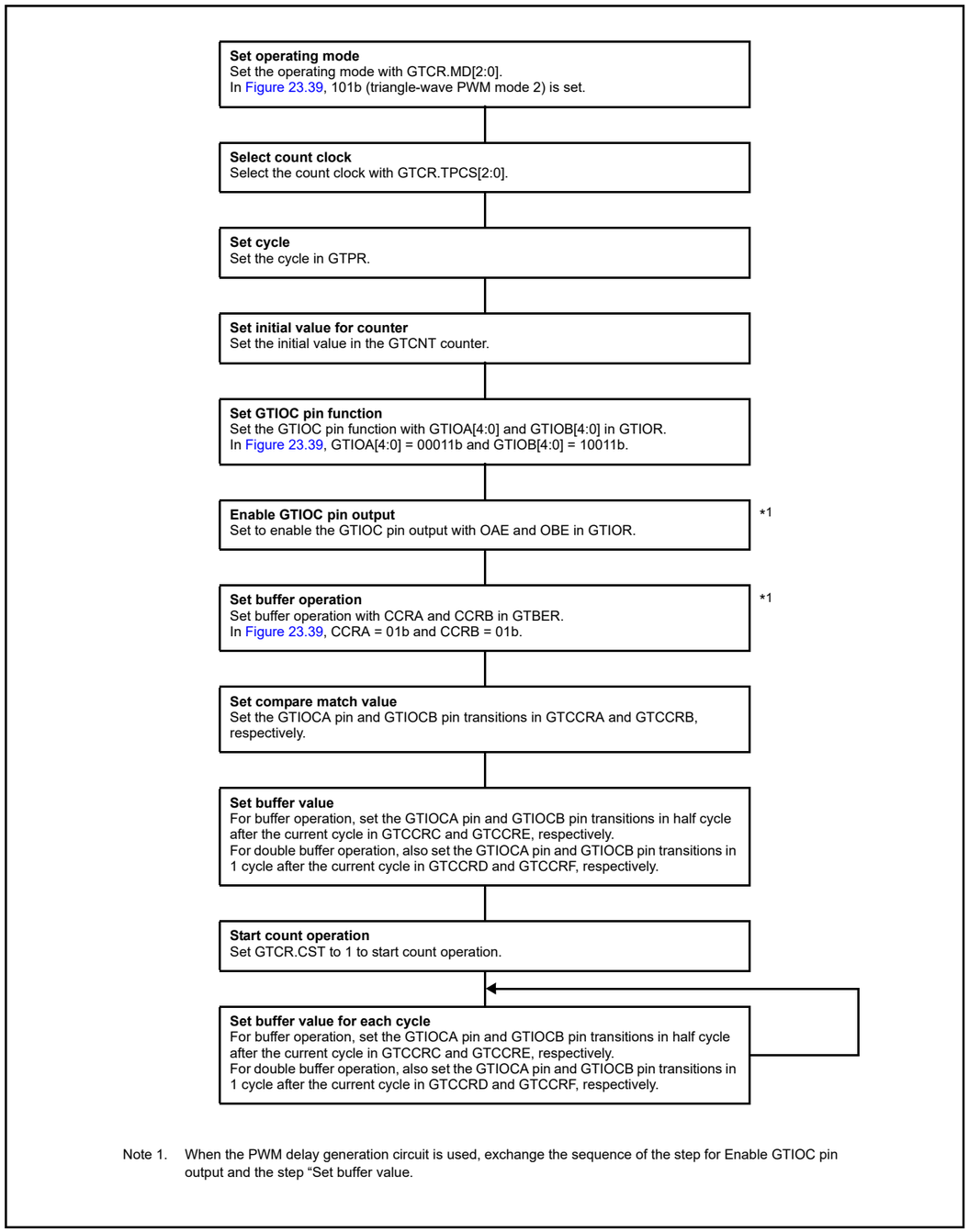
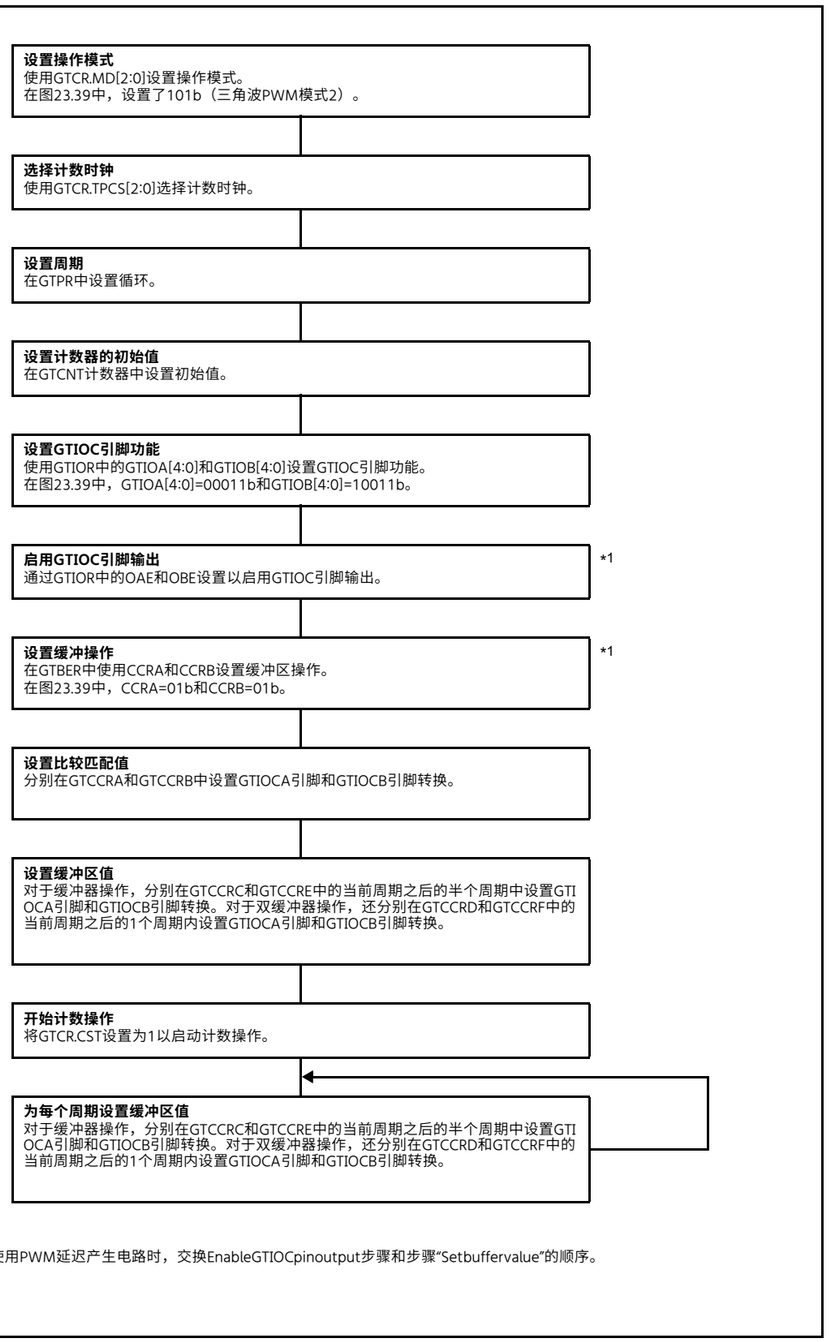


Figure 23.39 带缓冲操作的三角波PWM模式2操作示例，从GTIOC0A引脚和GTIOC0B引脚在计数开始时的高电平输出，输出在GTCCRAGTCCRB比较匹配，并在循环结束时保留输出



Note 1. When the PWM delay generation circuit is used, exchange the sequence of the step for Enable GTIOC pin output and the step “Set buffer value.

Figure 23.40 Example setting for triangle-wave PWM mode 2



Note 1. 当使用PWM延迟产生电路时，交换EnableGTIOCpinoutput步骤和步骤“Setbuffervalue”的顺序。

Figure 23.40 三角波PWM模式2的设置示例

23.3.3.5 Triangle-wave PWM mode 3 (64-bit transfer at trough)

The triangle-wave PWM mode 3 is a mode in which the cycle is set in GTPR. The GTCNT counter performs triangle-wave (full-wave) operation and a PWM waveform is output to the GTIOCA or GTIOCB pin at a compare match of GTCCRA or GTCCRB with buffer operation fixed. Buffer operation in triangle-wave PWM mode 3 is different from the usual buffer operation. Buffer transfer is performed from:

- GTCCRC to GTCCRA at the trough
- GTCCRE to GTCCRB at the trough
- GTCCRD to temporary register A at the trough
- GTCCRF to temporary register B at the trough
- Temporary register A to GTCCRA at the crest
- Temporary register B to GTCCRB at the crest.

The pin output value can be selected from low output, high output, or toggle output separately for a compare match and for the cycle end based on the GTIOR setting. By setting GTDTCR, GTDVU, and GTDVD, a compare match value for a negative-phase waveform with dead time can automatically be set to GTCCRB.

Figure 23.41 shows an example of triangle-wave PWM mode 3 operation, and Figure 23.42 shows an example setting for triangle-wave PWM mode 3.

23.3.3.5 三角波PWM模式3（波谷64位传输）

三角波PWM模式3是在GTPR中设定周期的模式。GTCNT计数器执行三角波（全波）操作，并且在GTCCRA或GTCCRB的比较匹配且缓冲器操作固定时，PWM波形输出到GTIOCA或GTIOCB引脚。三角波PWM模式3中的缓冲操作与通常的缓冲操作不同。缓冲区传输从以下位置执行：

- GTCCRC到GTCCRA在低谷
- GTCCRE到GTCCRB在低谷
- GTCCRD到谷底临时寄存器A
- GTCCRF到波谷临时寄存器B
- 顶部GTCCRA的临时注册A
- 在顶部的GTCCRB临时寄存器B。

引脚输出值可以根据GTIOR设置分别从低输出、高输出或切换输出中选择，用于比较匹配和循环结束。通过设置GTDTCR、GTDVU和GTDVD，可以自动将带死区时间的负相位波形的比较匹配值设置为GTCCRB。

图23.41显示了三角波PWM模式3操作的示例，图23.42显示了三角波PWM模式3的示例设置。

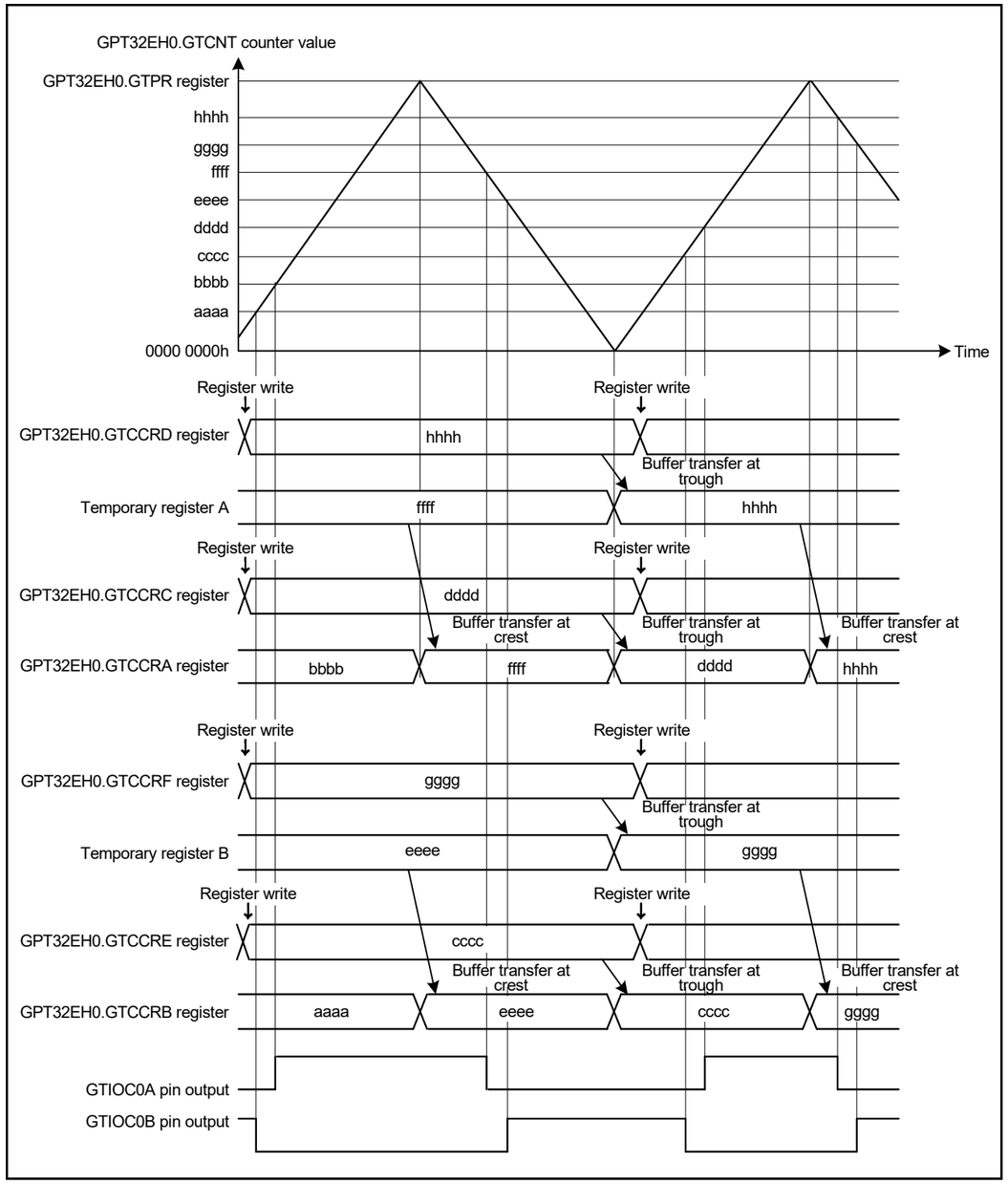


Figure 23.41 **Example of triangle-wave PWM mode 3 operation with low output from the GTIOC0A pin and high output from the GTIOC0B pin at count start, output toggled at GTCCRA/GTCCRB compare match, and output retained at cycle end**

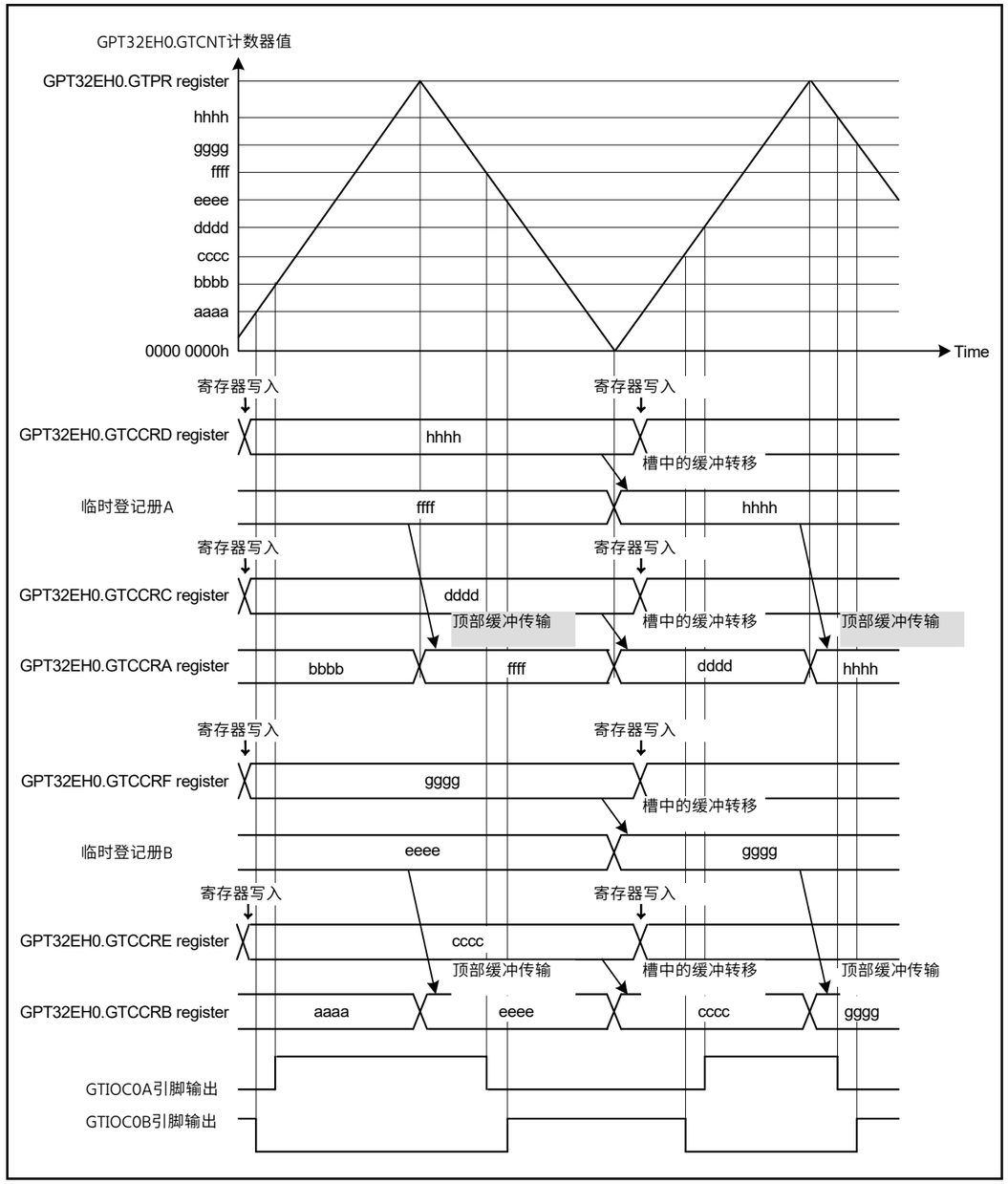
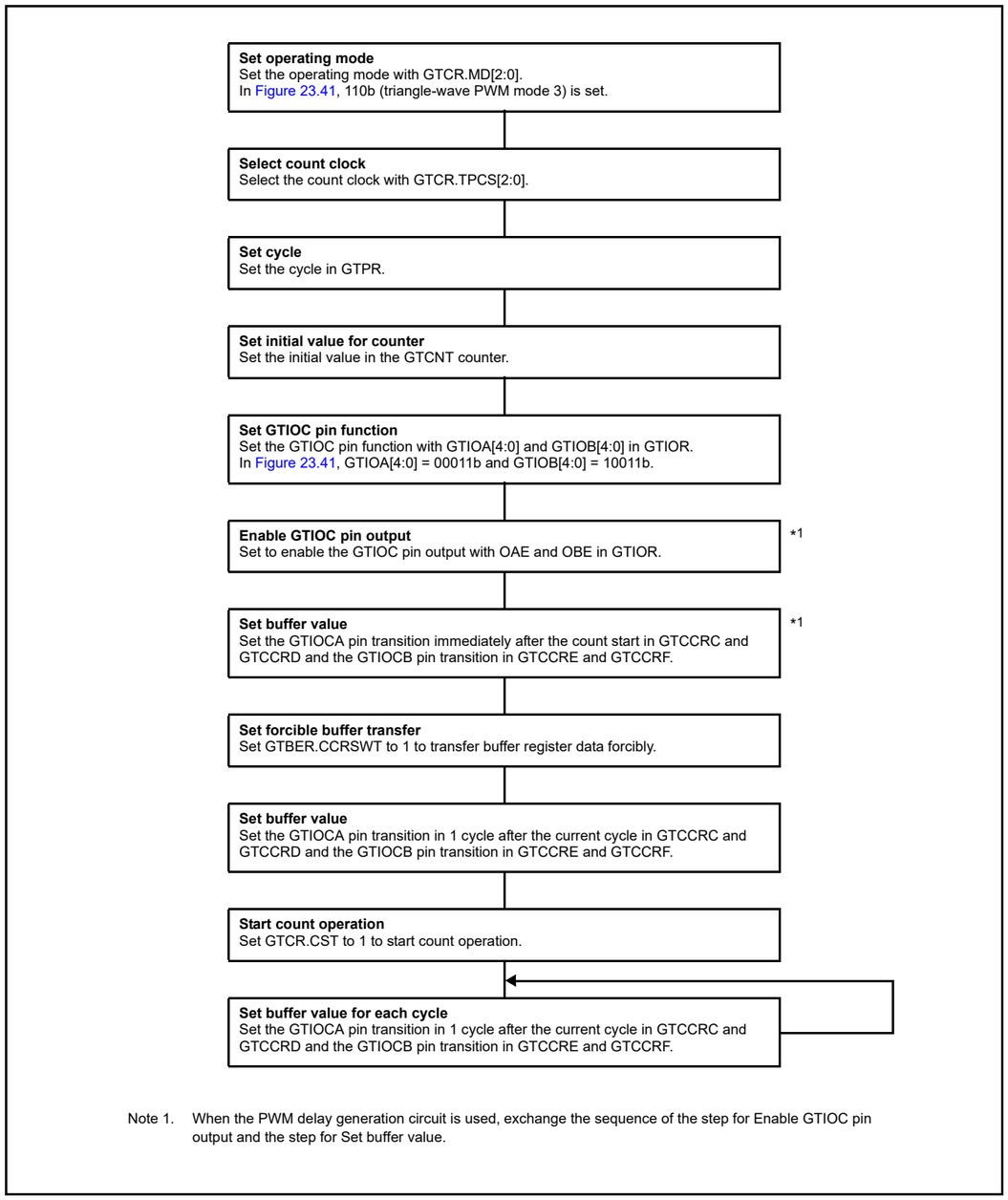


Figure 23.41 **三角波PWM模式3操作示例，计数开始时GTIOC0A引脚输出低电平，GTIOC0B引脚输出高电平，在GTCCRAGTCCRB比较匹配时切换输出，在周期结束时保持输出**

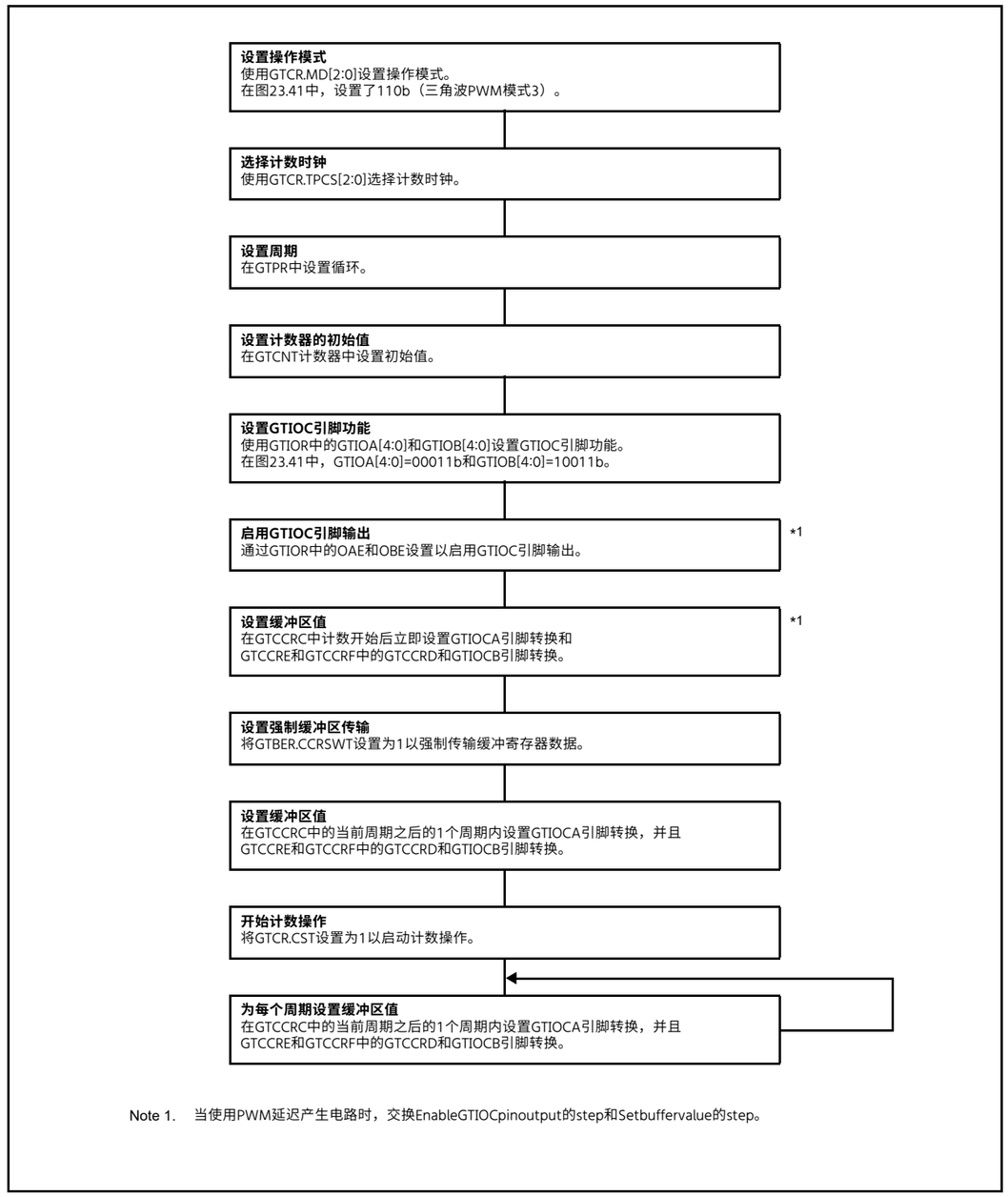


Note 1. When the PWM delay generation circuit is used, exchange the sequence of the step for Enable GTIOC pin output and the step for Set buffer value.

Figure 23.42 Example setting for triangle-wave PWM mode 3

23.3.4 Automatic Dead Time Setting Function

By setting GTDTCR, a compare match value for a negative waveform with dead time obtained by a compare match value for a positive waveform (GTCCRA value) and specified dead time values (GTDVU and GTDVD values) can automatically be set to GTCCRB. The automatic dead time setting function can be used in saw-wave one-shot pulse mode and all the triangle PWM modes.



Note 1. 当使用PWM延迟产生电路时，交换EnableGTIOCpinoutput的step和Setbuffervalue的step。

Figure 23.42 三角波PWM模式3的设置示例

23.3.4 自动死区时间设置功能

通过设置GTDTCR，通过正波形的比较匹配值（GTCCRA值）和指定的死区时间值（GTDVU和GTDVD值）获得的负波形与死区时间的比较匹配值可以自动设置为GTCCRB。自动死区时间设置功能可用于锯齿波一次性脉冲模式和所有三角PWM模式。

Dead time can be separately set for the first half and second half of a waveform. Dead time for the transition in the first half of a negative waveform is set in GTDVU and that in the second half is set in GTDVD. The same dead time can also be set for the first and second halves by setting the GTDTCR.TDFER bit to 1.

GTDBU can be used as a buffer register of GTDVU, and GTDBD can be used as a buffer register of GTDVD. Buffer transfer is performed at a GTCNT overflow (during up-counting), an underflow (during down-counting), or at a GTCNT counter clear for saw waves and at the trough for triangle waves.

The compare match value set by automatic dead time setting function can be confirmed by reading from GTCCRB. Writing to GTCCRB is prohibited when the automatic dead time setting function is used.

Dead time setting beyond the cycle is prohibited. When a dead time error occurs, the compare match values for positive and negative waveforms are adjusted to generate the waveforms with the dead time as shown in Table 23.6. The adjusted value for the negative waveform is set for GTCCRB automatically. The adjusted value for the positive waveform is used as internal signal and not set for GTCCRA.

In saw-wave one-shot pulse mode, when the adjusted value is beyond the cycle or the adjusted waveform toggle points are in disorder, the complementarity of the waveforms is not guaranteed.

In triangle-wave mode, when the dead time is beyond the cycle by setting the value GTCCR = 0 or GTCCRA ≥ GTPR for GTCCRA, the output protection function keeps the level of output. For details, see section 23.8.4, Output Protection Function for GTIOC Pin Output. When the GTCCRA is GTCCRA ≥ GTPR + GTDVn, GTPR-1 is set for GTCCRB as the upper limit value. The automatic dead time value setting to GTCCRB is performed at the next clock cycle count when registers used for calculating the automatic dead time value are updated.

The way to rewrite GTDVn differs by GPT channel number.

Table 23.6 Compare match value after adjusting for dead time error

PWM output operating mode	Count direction	First half/ Second half	Condition of dead time error	Compare match value after adjusting	
				Positive waveform	Negative waveform
Saw-wave one-shot pulse mode	Up	First half	GTCCRA - GTDVU < 0	GTDVU	0
		Second half	GTCCRA + GTDVD > GTPR	GTPR - GTDVD	GTPR
	Down	First half	GTCCRA + GTDVU > GTPR	GTPR - GTDVU	GTPR
		Second half	GTCCRA - GTDVD < 0	GTDVD	0
Triangle-wave PWM mode 1/2/3	Up	First half	GTCCRA - GTDVU ≤ 0	GTDVU + 1	1
	Down	Second half	GTCCRA - GTDVD < 0	GTDVD	0

GPT32EH0 to GPT32EH3 and GPT32E4 to GPT32E7

When GTDVn buffer operation is enabled, GTDBn can be written at anytime. GTDBn is transferred to GTDVn at the cycle end.

When GTDVn buffer operation is disabled, stop the GPT using the CST bit in the GTCR register before changing GTDVn to a new value.

GPT328 to GPT3213

While GPT is running, changing the GTDVU values is prohibited. To change GTDVU to a new value, first stop the GPT using the CST bit in the GTCR register.

Figure 23.43 to Figure 23.46 show examples of automatic dead time setting function operation for GPT32EH and GPT32E. Figure 23.47 and Figure 23.48 show the setting examples.

可以为波形的前半部分和后半部分分别设置死区时间。在GTDVU中设置负波形前半部分的过渡的死区时间，在GTDVD中设置后半部分的过渡时间。通过将GTDTCR.TDFER位设置为1，也可以为前半部分和后半部分设置相同的死区时间。

GTDBU可以作为GTDVU的缓冲寄存器，GTDBD可以作为GTDVD的缓冲寄存器。在GTCNT上溢（向上计数期间）、下溢（向下计数期间）或GTCNT计数器清除锯齿波和三角波波谷时执行缓冲区传输。

自动死区时间设置功能设置的比较匹配值可以通过读取GTCCRB来确认。
使用自动死区时间设置功能时，禁止写入GTCCRB。

禁止设置超出周期的死区时间。当出现死区时间错误时，调整正负波形的比较匹配值以生成具有死区时间的波形，如表23.6所示。负波形的调整值自动为GTCCRB设置。正波形的调整值用作内部信号，而不是为GTCCRA设置的。

在锯齿波单发脉冲模式下，当调整值超出周期或调整后的波形切换点混乱时，波形的互补性无法保证。

在三角波模式下，当通过设置GTCCRA=0或GTCCRA≥GTCCRA的值使死区时间超出周期时，输出保护功能保持输出电平。有关详细信息，请参见第23.8.4节，GTIOC引脚输出的输出保护功能。当GTCCRA为GTCCRA≥GTPR+GTDVn时，将GTPR-1设置为GTCCRB作为上限值。当用于计算自动死区时间值的寄存器被更新时，在下一个时钟周期计数时执行GTCCRB的自动死区时间值设置。

重写GTDVn的方式因GPT通道号而异。

Table 23.6 调整死区时间误差后比较匹配值

PWM输出工作模式	计数方向	First half/ 下半场	死区时间错误的条件	调整后比较匹配值	
				正波形	负波形
锯波单发脉冲模式	Up	上半场	GTCCRA - GTDVU < 0	GTDVU	0
		下半场	GTCCRA + GTDVD > GTPR	GTPR - GTDVD	GTPR
	Down	上半场	GTCCRA + GTDVU > GTPR	GTPR - GTDVU	GTPR
		下半场	GTCCRA - GTDVD < 0	GTDVD	0
Triangle-wave PWM mode 1/2/3	Up	上半场	GTCCRA - GTDVU ≤ 0	GTDVU + 1	1
	Down	下半场	GTCCRA - GTDVD < 0	GTDVD	0

GPT32EH0到GPT32EH3和GPT32E4到GPT32E7

当GTDVn缓冲区操作使能时，可以随时写入GTDBn。GTDBn在循环结束时转移到GTDVn。

当GTDVn缓冲器操作被禁用时，在更改之前使用GTCR寄存器中的CST位停止GPT
GTDVn到一个新值。

GPT328 to GPT3213

在GPT运行时，禁止更改GTDVU值。要将GTDVU更改为新值，首先使用GTCR寄存器中的CST位停止GPT。

图23.43至图23.46显示了GPT32EH和自动死区时间设置功能操作示例
GPT32E。图23.47和图23.48显示了设置示例。

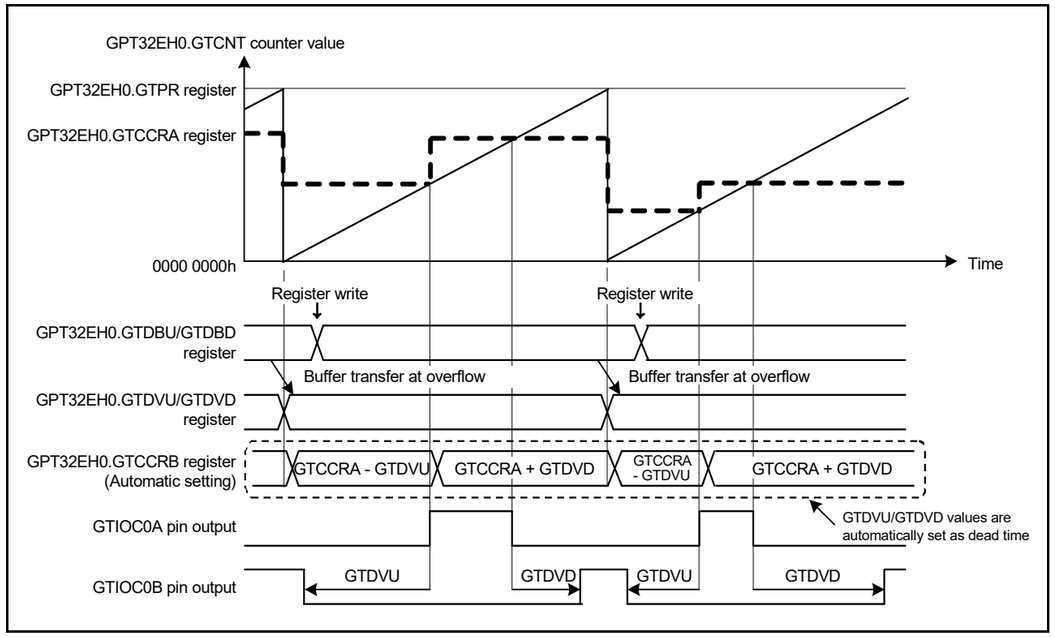


Figure 23.43 Example of automatic dead time setting function operation with saw-wave one-shot pulse mode, up-counting, GTDVU and GTDVD set to buffer operation, and active-high

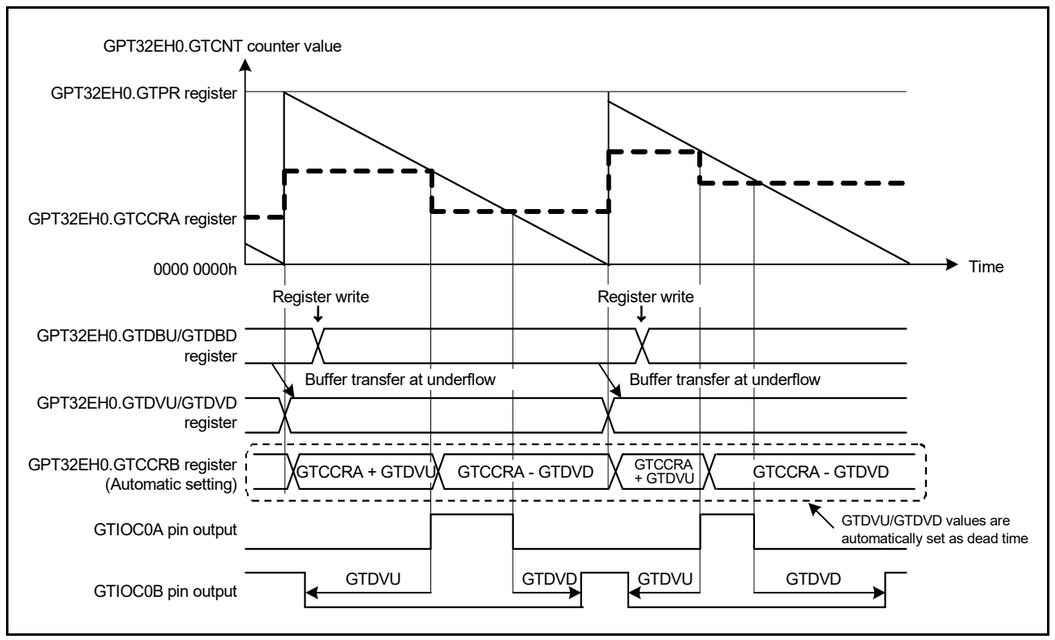


Figure 23.44 Example of automatic dead time setting function operation with saw-wave one-shot pulse mode, down-counting, GTDVU and GTDVD set to buffer operation, and active-high

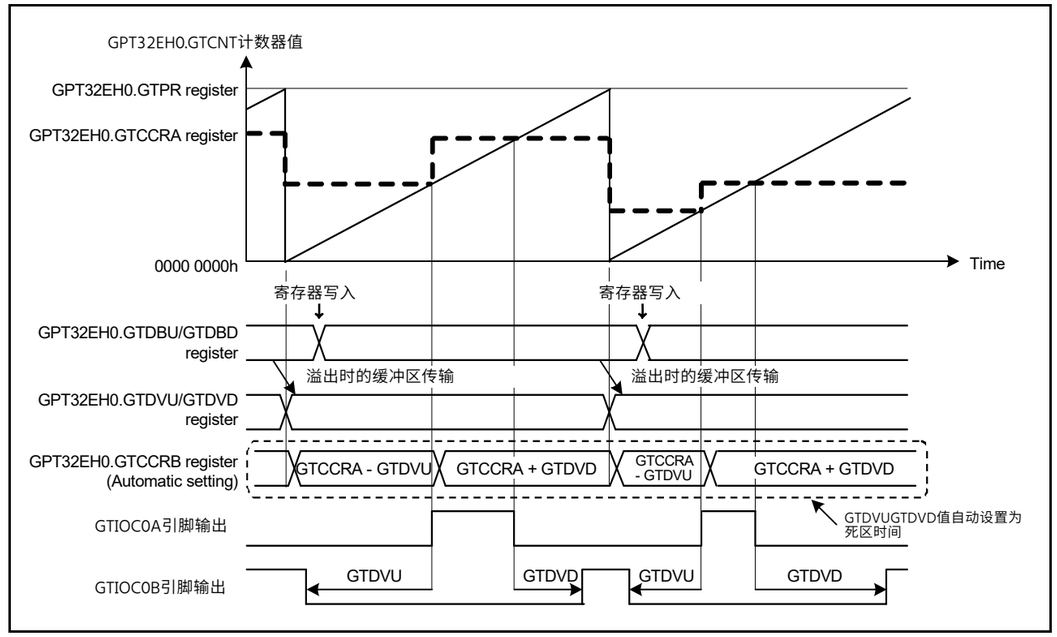


Figure 23.43 自动死区时间设置功能操作示例，锯齿波单次脉冲模式、递增计数、GTDVU和GTDVD设置为缓冲操作以及高电平有效

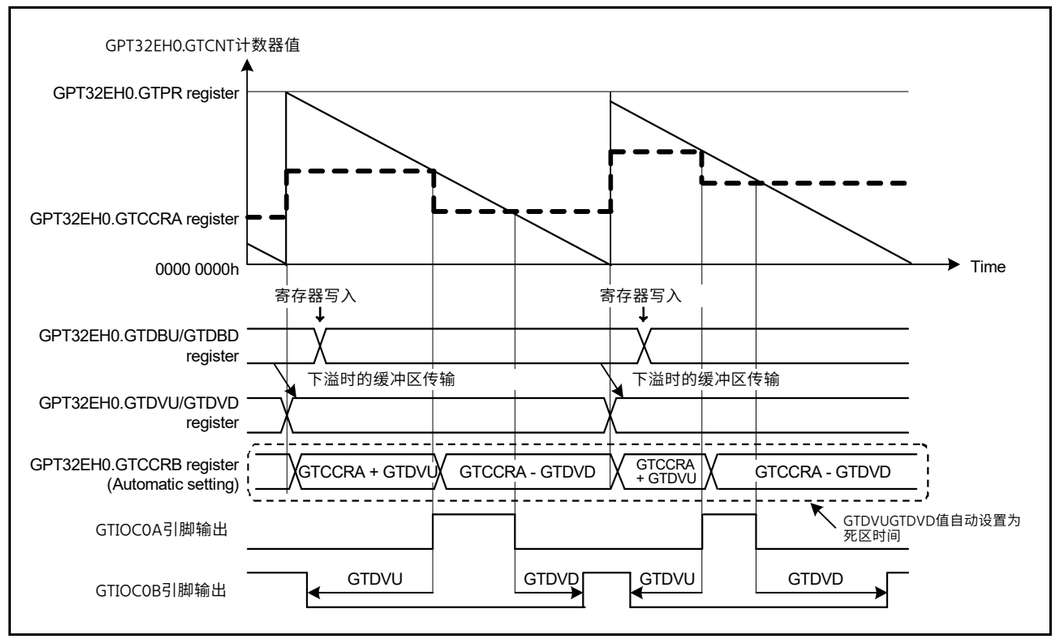


Figure 23.44 自动死区时间设置功能操作示例，锯齿波单次脉冲模式、递减计数、GTDVU和GTDVD设置为缓冲操作以及高电平有效

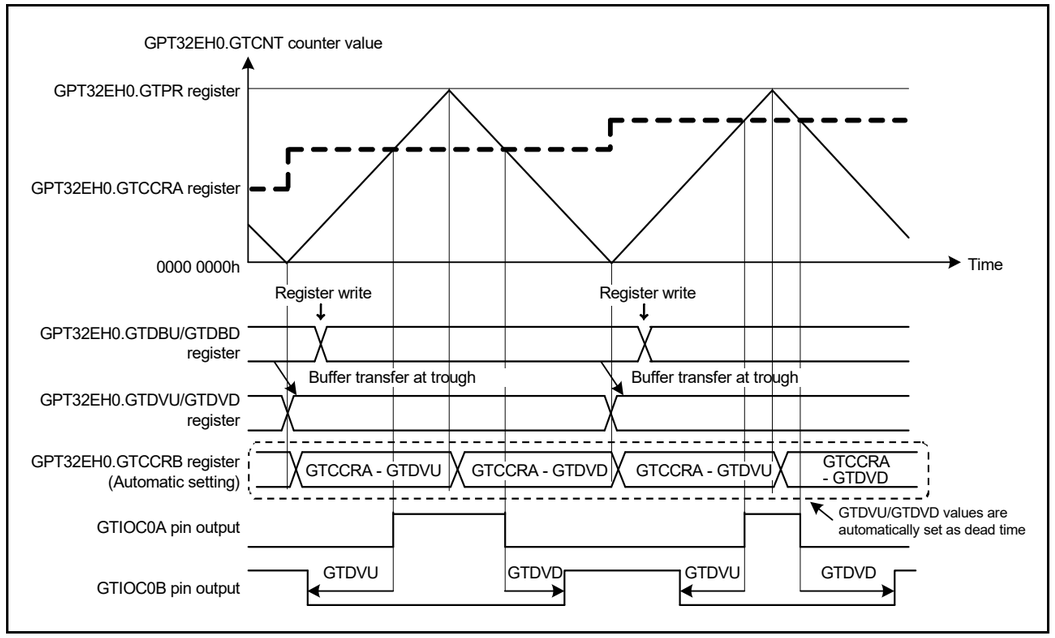


Figure 23.45 Example of automatic compare-match value setting function with dead time with triangle-wave PWM mode 1, GTDVU and GTDVD set to buffer operation, active-high

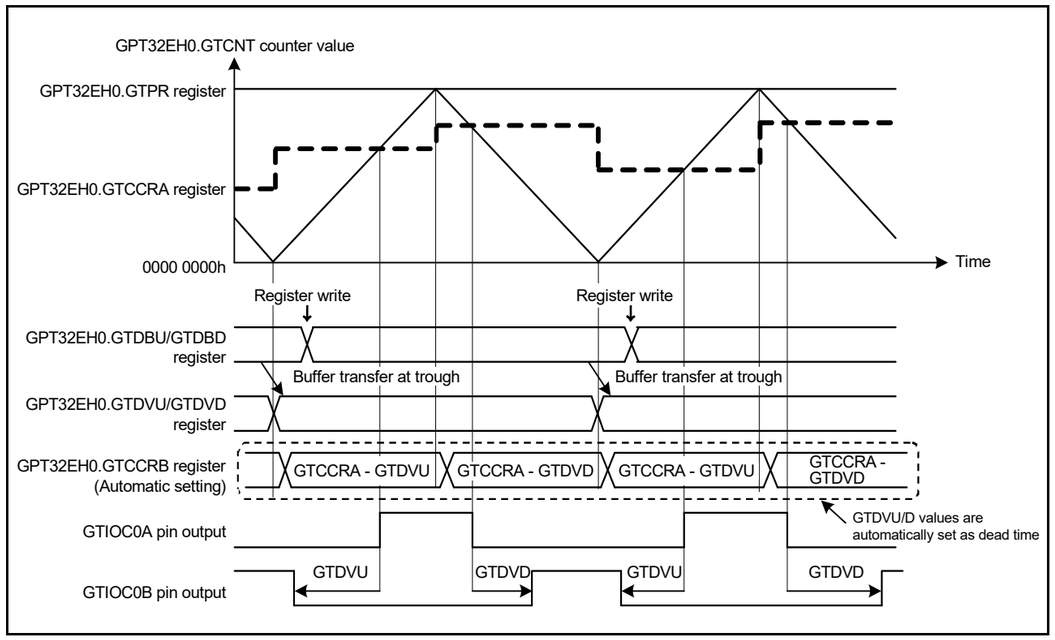


Figure 23.46 Example of automatic compare-match value setting function with dead time, with triangle-wave PWM mode 2 or 3, GTDVU and GTDVD set to buffer operation, and active-high

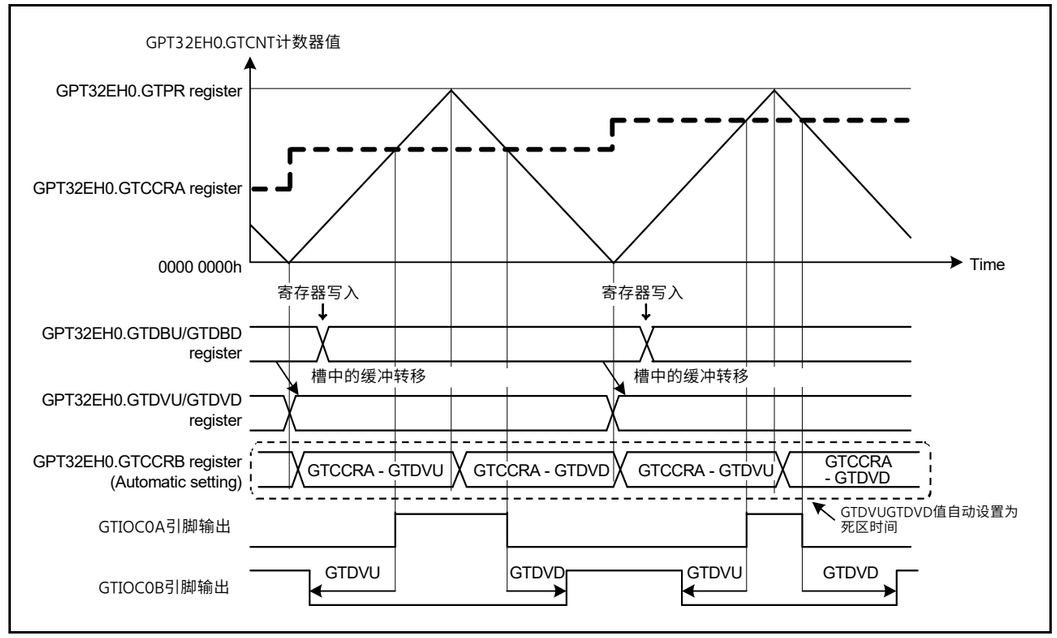


Figure 23.45 三角波带死区时间的自动比较匹配值设置功能示例
PWM模式1，GTDVU和GTDVD设置为缓冲操作，高电平有效

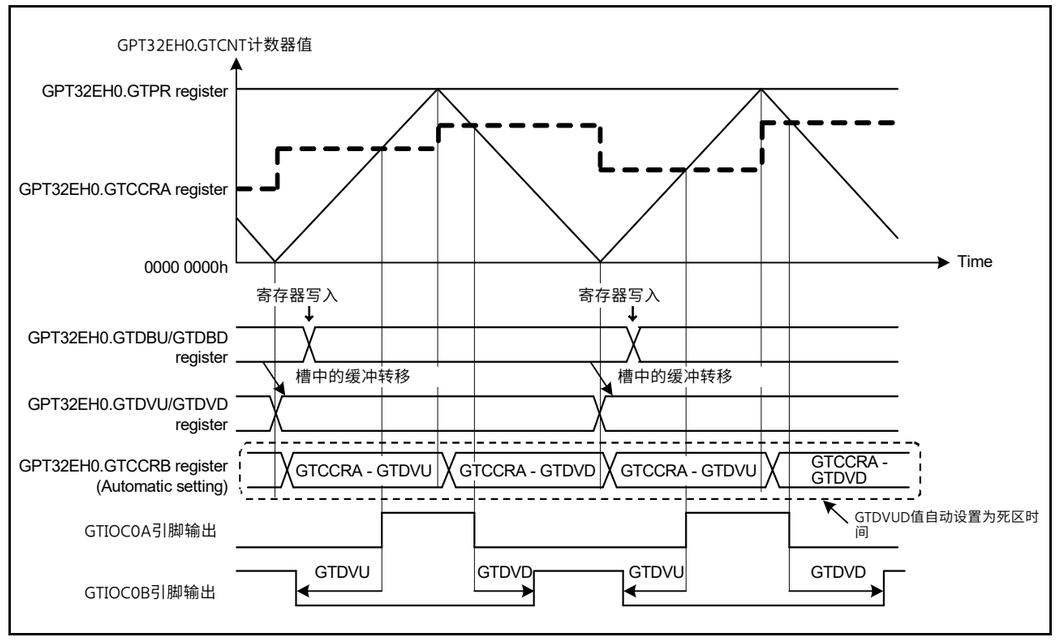
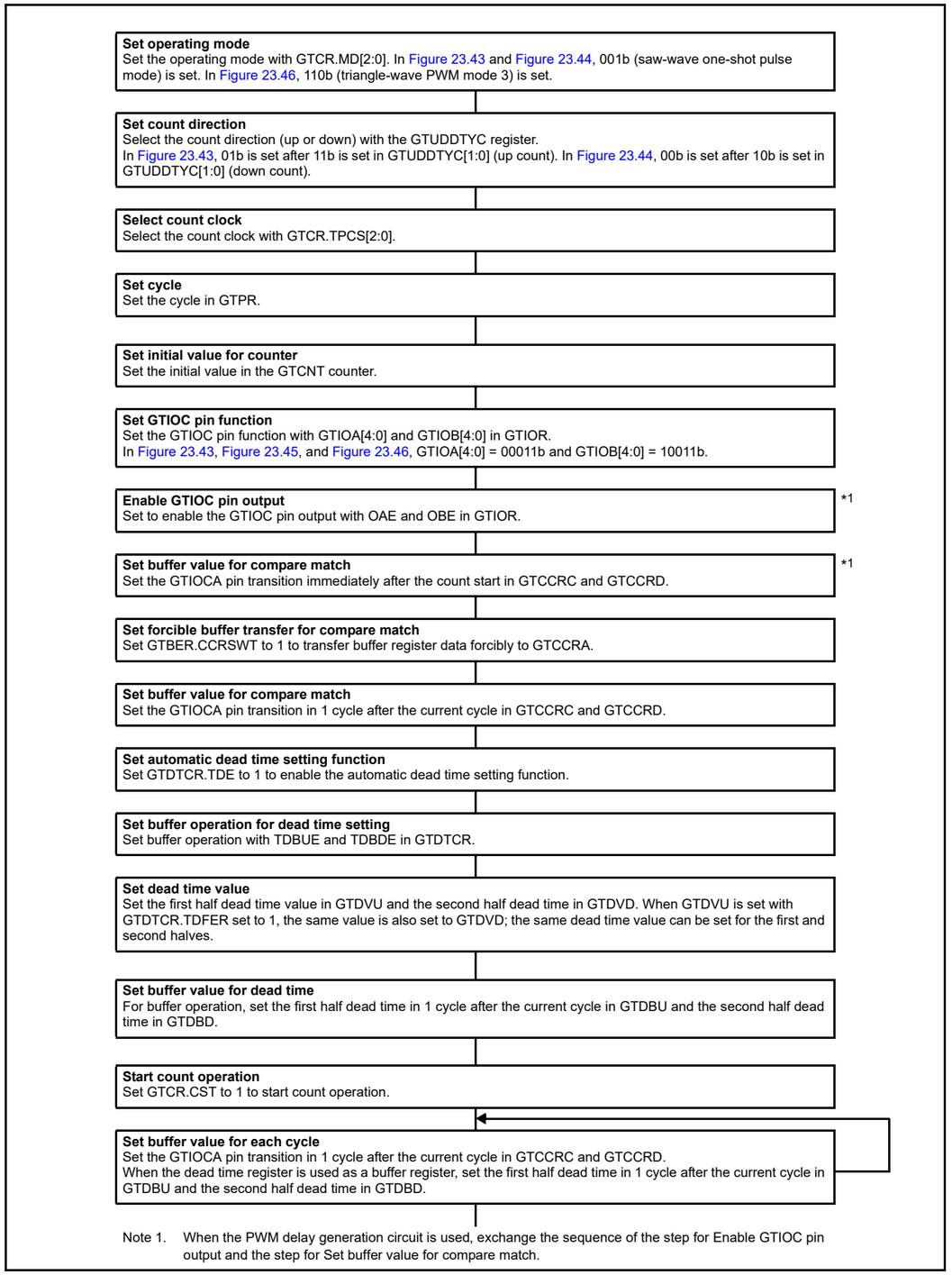
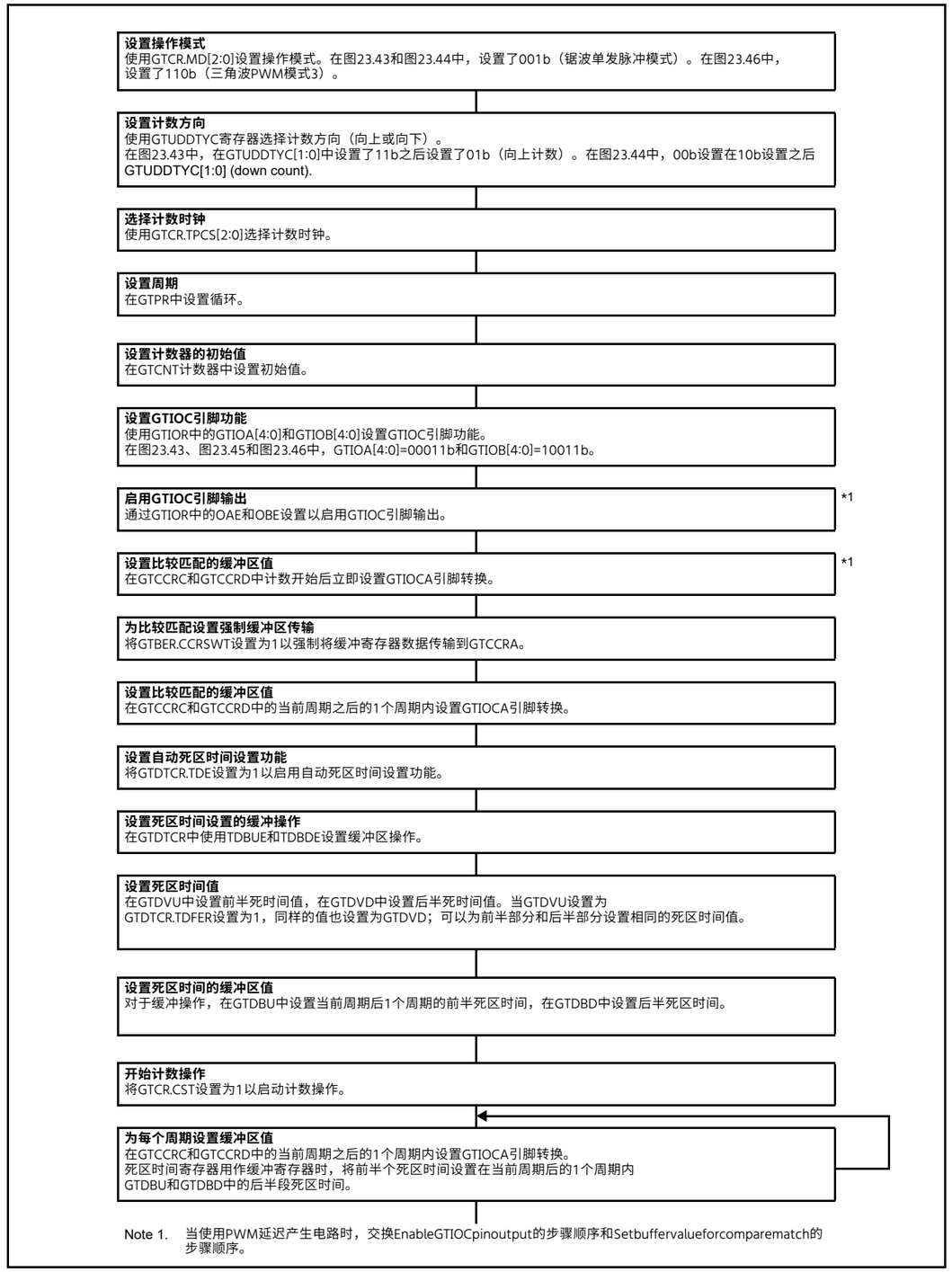


Figure 23.46 带死区时间的自动比较匹配值设置功能示例，带三角波
PWM模式2或3，GTDVU和GTDVD设置为缓冲操作，高电平有效



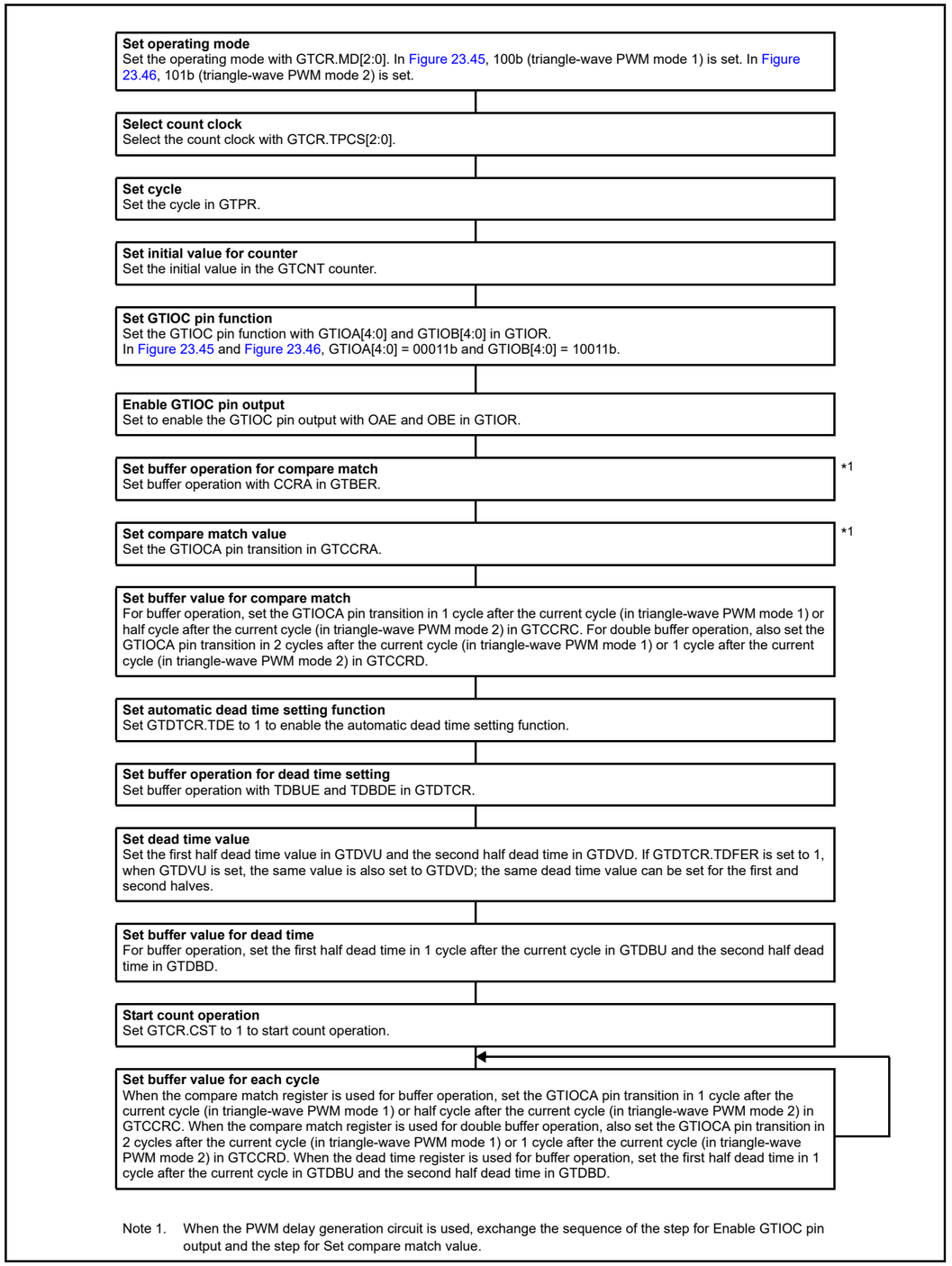
Note 1. When the PWM delay generation circuit is used, exchange the sequence of the step for Enable GTIOC pin output and the step for Set buffer value for compare match.

Figure 23.47 Example setting for automatic dead time setting function with saw-wave one-shot pulse mode, and triangle-wave PWM mode 3



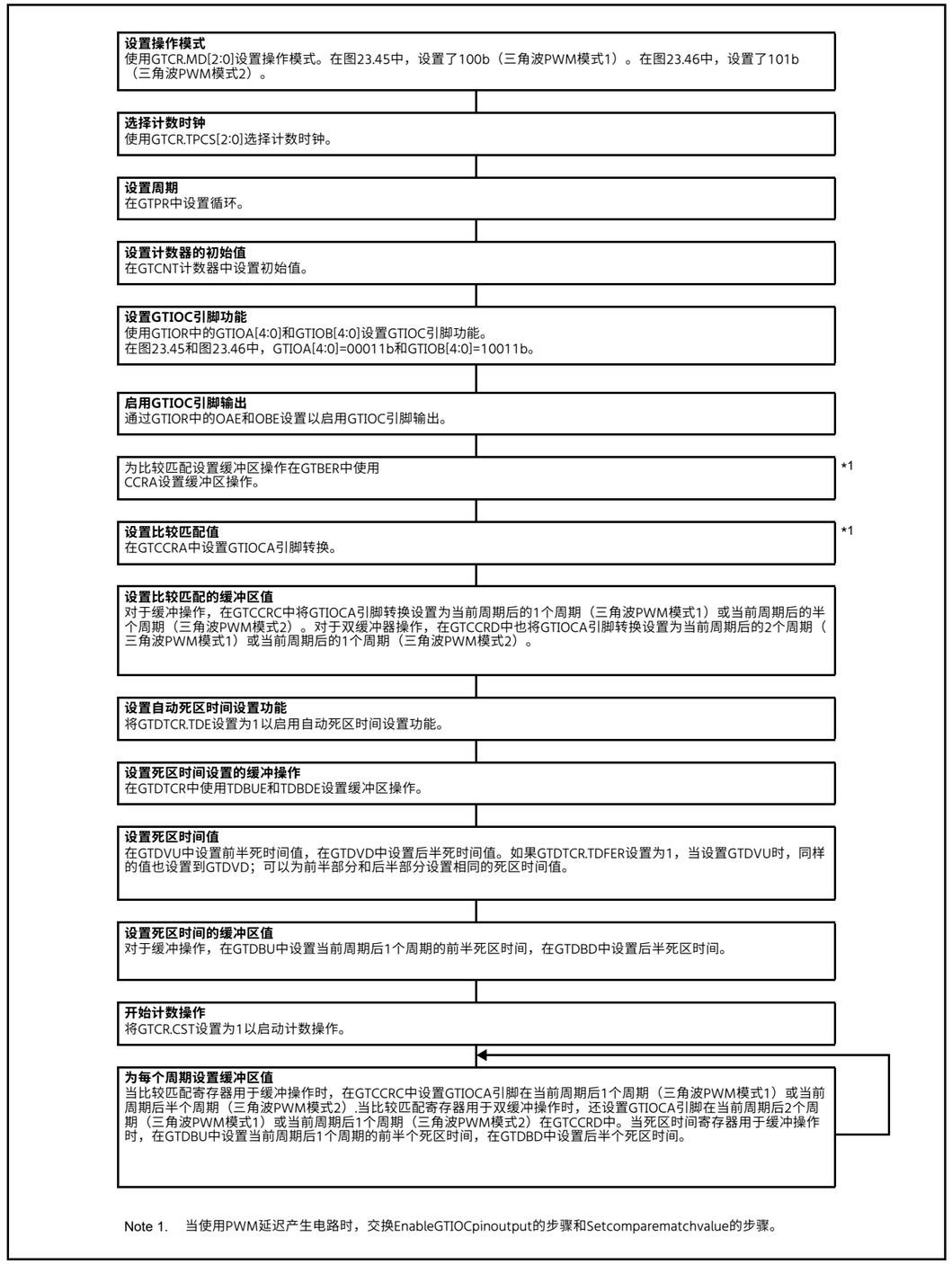
Note 1. 当使用PWM延迟产生电路时，交换EnableGTIOCpinoutput的步骤顺序和Setbuffervalueforcomparematch的步骤顺序。

Figure 23.47 锯齿波一次性脉冲模式和三角波PWM模式的自动死区时间设置功能示例3



Note 1. When the PWM delay generation circuit is used, exchange the sequence of the step for Enable GTIOC pin output and the step for Set compare match value.

Figure 23.48 Example setting for automatic dead time setting function with triangle-wave PWM mode 1 or 2



Note 1. 当使用PWM延迟产生电路时，交换EnableGTIOCpinoutput的步骤和Setcomparematchvalue的步骤。

Figure 23.48 三角波PWM模式1或2的自动死区时间设置功能设置示例

23.3.5 Count Direction Changing Function

The count direction of the GTCNT counter can be changed by modifying the UD bit in GTUDDTYC.

In saw-wave mode, if the UD bit in GTUDDTYC is modified during count operation, the count direction is changed at an overflow (when modified during up-counting) or an underflow (when modified during down-counting). If the GTUDDTYC.UD bit is modified while the count operation is stopped and the GTUDDTYC.UDF bit is 0, the GTUDDTYC.UD bit modification is not reflected at the start of counting and the count direction is changed at an overflow or an underflow. If the UDF bit is set to 1 while the count operation is stopped, the GTUDDTYC.UD bit value at that time is reflected at the start of counting.

In triangle-wave mode, the count direction does not change when the UD bit in GTUDDTYC is modified during the count operation. Similarly, when the GTUDDTYC.UD bit is modified while the count operation is stopped and GTUDDTYC.UDF bit is 0, the GTUDDTYC.UD bit value is not reflected to the count operation. If the GTUDDTYC.UDF bit is set to 1 while the count operation is stopped, the GTUDDTYC.UD bit value at that time is reflected at the start of counting.

If the count direction changes during a saw-wave count operation, the GTPR value after the start of up-counting is reflected to the count cycle during up-counting and the GTPR value before the start of down-counting is reflected during down-counting.

Figure 23.49 shows an example of count direction changing function operation.

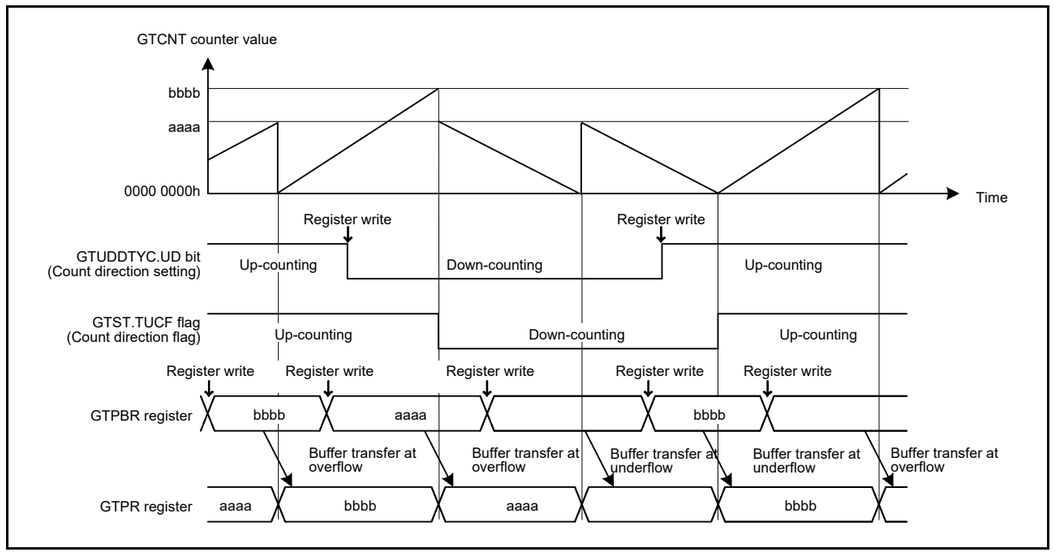


Figure 23.49 Example of count direction changing function operation during buffer operation

23.3.6 Function of Output Duty 0% and 100%

The output duty of the GTIOCA pin and the GTIOCB pin are set to 0% or 100% by changing the GTUDDTYC.OADTY bit or GTUDDTYC.OBDTY bit.

In saw-wave mode, if the GTUDDTYC.OADTY bit or the GTUDDTYC.OBDTY bit is modified during the count operation, the output duty setting is reflected at an overflow (when modified during up-counting) or an underflow (when modified during down-counting). If the GTUDDTYC.OADTY bit or the GTUDDTYC.OBDTY bit is modified while the count operation is stopped and the GTUDDTYC.OADTYF or the GTUDDTYC.OBDTYF bit is 0, the output duty modification is not reflected at the start of counting. The output duty changes at an overflow or an underflow. If the GTUDDTYC.OADTYF or the GTUDDTYC.OBDTYF bit is set to 1 while the count operation is stopped, the GTUDDTYC.OADTY bit or the GTUDDTYC.OBDTY bit value at that time is reflected at the start of counting.

In triangle-wave mode, if the GTUDDTYC.OADTY bit or the GTUDDTYC.OBDTY bit is modified during the count operation, the output duty setting is reflected at an underflow.

23.3.5 计数方向改变功能

GTCNT计数器的计数方向可以通过修改GTUDDTYC中的UD位来改变。

在锯齿波模式下，如果在计数操作期间修改GTUDDTYC中的UD位，则计数方向会在溢出（在向上计数期间修改时）或下溢（在向下计数期间修改时）改变。如果在计数操作停止且GTUDDTYC.UDF位为0时修改GTUDDTYC.UD位，则

GTUDDTYC.UD位修改不会反映在计数开始时，计数方向会在上溢或下溢时改变。如果在计数操作停止时UDF位设置为1，则此时的GTUDDTYC.UD位值将反映在计数开始时。

在三角波模式下，在计数操作期间修改GTUDDTYC中的UD位不会改变计数方向。类似地，当在计数操作停止且GTUDDTYC.UDF位为0时修改GTUDDTYC.UD位时，GTUDDTYC.UD位的值不会反映到计数操作中。如果

计数操作停止时GTUDDTYC.UDF位设置为1，此时的GTUDDTYC.UD位值反映在计数开始时。

如果在锯齿波计数操作期间计数方向发生变化，则加计数开始后的GTPR值在加计数时反映到计数周期，减计数开始前的GTPR值在减计数时反映.

图23.49显示了计数方向改变功能操作的示例。

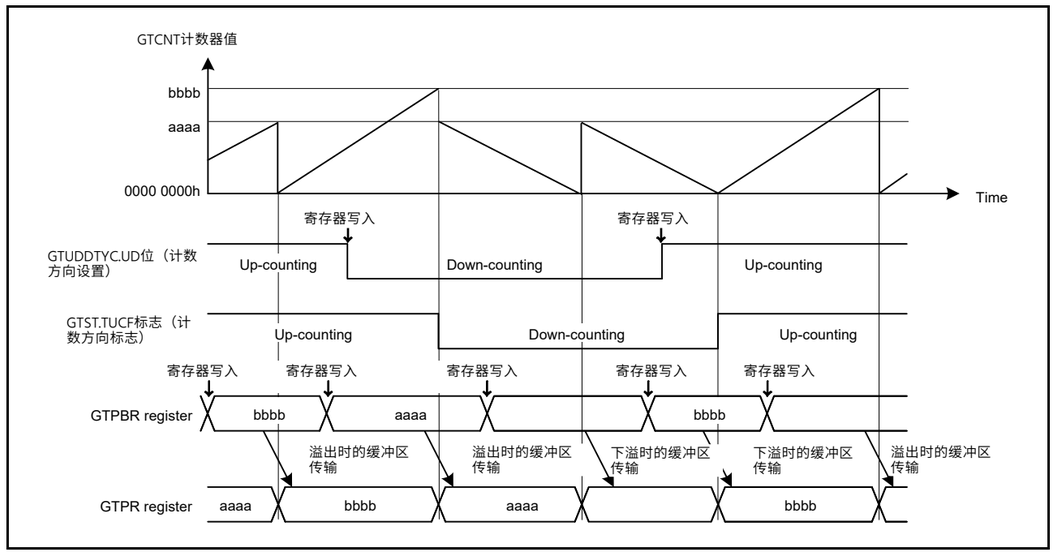


Figure 23.49 缓冲动作时的计数方向变更功能动作示例

23.3.6 输出占空比0%和100%的功能

GTIOCA引脚和GTIOCB引脚的输出占空比通过更改GTUDDTYC.OADTY位或GTUDDTYC.OBDTY位设置为0%或100%。

在锯齿波模式下，如果在计数操作期间修改GTUDDTYC.OADTY位或GTUDDTYC.OBDTY位，则输出占空比设置反映在溢出（在向上计数期间修改时）或下溢（在向下期间修改时-数数）。如果在计数操作停止且GTUDDTYC.OADTYF或GTUDDTYC.OBDTYF位为0时修改GTUDDTYC.OADTY位或GTUDDTYC.OBDTY位，则在计数开始时不反映输出占空比修改。输出占空比在上溢或下溢时发生变化。如果在计数操作停止时GTUDDTYC.OADTYF或GTUDDTYC.OBDTYF位设置为1，则

GTUDDTYC.OADTY位或当时的GTUDDTYC.OBDTY位值反映在计数开始时。

在三角波模式下，如果在计数操作期间修改GTUDDTYC.OADTY位或GTUDDTYC.OBDTY位，则输出占空比设置会反映在下溢处。

If the GTUDDTYC.OADTY bit or the GTUDDTYC.OBDTY bit is modified while the count operation is stopped and the GTUDDTYC.OADTYF or the GTUDDTYC.OBDTYF bit is 0, the output duty modification is not reflected at the start of counting. The output duty changes at an underflow. If the GTUDDTYC.OADTY bit or the GTUDDTYC.OBDTY bit is modified while the count operation is stopped and the GTUDDTYC.OADTYF or the GTUDDTYC.OBDTYF bit is 1, the output duty modification is reflected at the start of counting.

In performing 0%/100% duty operation, GPT internally continues to:

- Perform compare match operation
- Set compare match flag
- Output interrupt
- Perform buffer operation.

When the control is changed from 0% or 100% duty setting to compare match, the output value of GTIOCA pin at cycle end is decided by GTIOR.GTIOA[3:2] and GTUDDTYC.OADTYR. The output value of GTIOCB pin at cycle end is decided by GTIOR.GTIOB[3:2] and GTUDDTYC.OBDTYR.

When GTIOR.GTIOA[3:2] and GTIOR.GTIOB[3:2] are set to 01b, the output pins output low at cycle end. When GTIOR.GTIOA[3:2] and GTIOR.GTIOB[3:2] are set to 10b, the output pins output high at cycle end.

GTUDDTYC.OADTYR selects the value that is the object of output retained/toggled at cycle end, when GTIOR.GTIOm[3:2] are set to 00b (output retained at cycle end) or when GTIOR.GTIOm[3:2] are set to 11b (output toggled at cycle end). Table 23.7 shows the values of GTIOCA/GTIOCB pin output at cycle end.

Table 23.7 Output values after releasing 0% or 100% duty setting (m = A, B)

GTIOR.GTIOm[3:2]	Compare match value at cycle end masked by 0% or 100% duty setting	GTUDDTYC.OmDTYR in duty 0% setting		GTUDDTYC.OmDTYR in duty 100% setting	
		0	1	0	1
00 (output retained at cycle end)	0	0	0	1	0
	1	0	1	1	1
01 (low output at cycle end)	-	0	0	0	0
10 (high output at cycle end)	-	1	1	1	1
11 (output toggled at cycle end)	0	1	1	0	1
	1	1	0	0	0

Figure 23.50 shows an example of output duty 0% and 100% function operation.

如果在计数操作停止且GTUDDTYC.OADTYF或GTUDDTYC.OBDTYF位为0时修改GTUDDTYC.OADTY位或GTUDDTYC.OBDTY位，则在计数开始时不反映输出占空比修改。输出占空比在下溢时发生变化。如果GTUDDTYC.OADTY位或GTUDDTYC.OBDTY位在计数操作停止且GTUDDTYC.OADTYF或

GTUDDTYC.OBDTYF位为1，输出占空比修改反映在计数开始。

在执行0%100%占空比操作时，GPT在内部继续：

- 执行比较匹配操作
- 设置比较匹配标志
- 输出中断
- 执行缓冲操作。

当控制从0%或100%占空比设置更改为比较匹配时，循环结束时GTIOCA引脚的输出值由GTIOR.GTIOA[3:2]和GTUDDTYC.OADTYR决定。周期结束时GTIOCB引脚的输出值由GTIOR.GTIOB[3:2]和GTUDDTYC.OBDTYR决定。

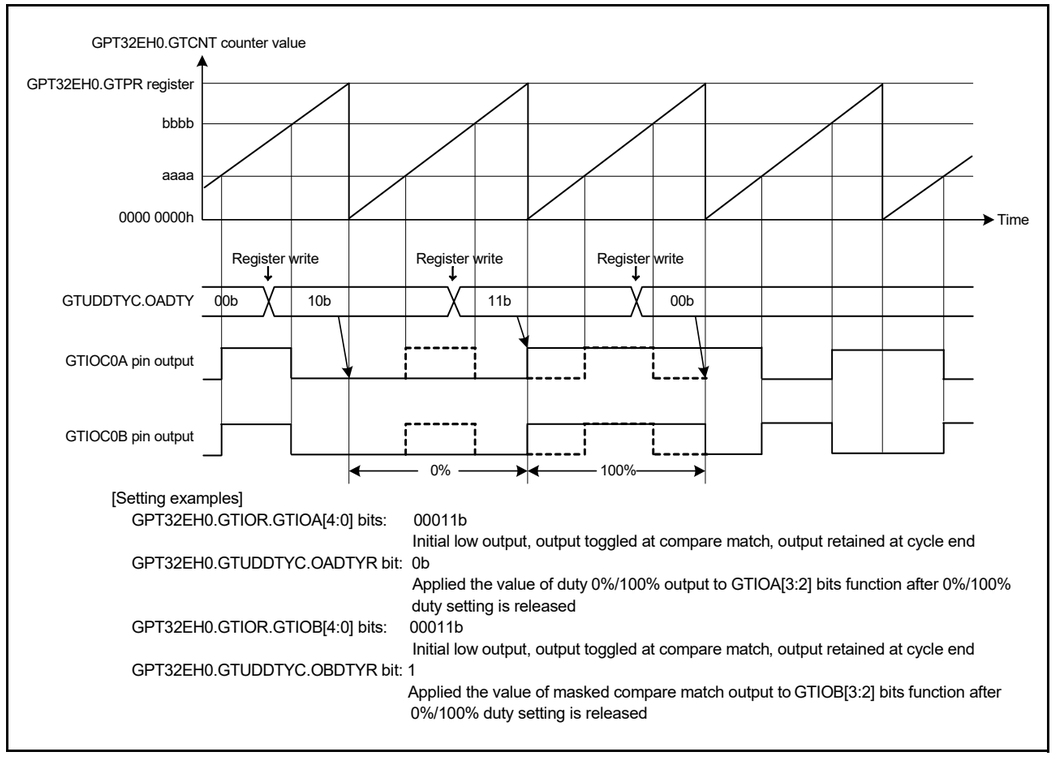
当GTIOR.GTIOA[3:2]和GTIOR.GTIOB[3:2]设置为01b时，输出引脚在周期结束时输出低电平。什么时候GTIOR.GTIOA[3:2]和GTIOR.GTIOB[3:2]设置为10b，输出引脚在周期结束时输出高电平。

GTUDDTYC.OADTYR选择在循环结束时作为输出保持切换的对象的值，当GTIOR.GTIOm[3:2]设置为00b（输出在循环结束时保留）或GTIOR.GTIOm[3:2]设置为11b（输出在循环结束时切换）。表23.7显示了循环结束时GTIOCAGTIOCB引脚输出的值。

Table 23.7 释放0%或100%占空比设置后的输出值(m=A B)

GTIOR.GTIOm[3:2]	比较被0%或100%占空比设置屏蔽的循环结束时的匹配值	GTUDDTYC.OmDTYR在占空比0%设置		GTUDDTYC.OmDTYR占空比100%设置	
		0	1	0	1
00（循环结束时保留输出）	0	0	0	1	0
	1	0	1	1	1
01（循环结束时输出低）	-	0	0	0	0
10（循环结束时的高输出）	-	1	1	1	1
11（循环结束时切换输出）	0	1	1	0	1
	1	1	0	0	0

图23.50显示了输出占空比0%和100%功能操作的示例。



[Setting examples]

GPT32EH0.GTIOR.GTIOA[4:0] bits: 00011b
Initial low output, output toggled at compare match, output retained at cycle end

GPT32EH0.GTUDDTYC.OADTYR bit: 0b
Applied the value of duty 0%/100% output to GTIOA[3:2] bits function after 0%/100% duty setting is released

GPT32EH0.GTIOR.GTIOB[4:0] bits: 00011b
Initial low output, output toggled at compare match, output retained at cycle end

GPT32EH0.GTUDDTYC.OBDTYR bit: 1
Applied the value of masked compare match output to GTIOB[3:2] bits function after 0%/100% duty setting is released

Figure 23.50 Example of output duty 0% and 100% functions

23.3.7 Hardware Count Start/Count Stop and Clear Operation

The GTCNT counter can be started, stopped, or cleared by the following hardware sources:

- External trigger input
- ELC event input
- GTIOCA/GTIOCB pin input.

23.3.7.1 Hardware start operation

The GTCNT counter can be started by selecting a hardware source using GTSSR.

Figure 23.51 shows an example of a count start operation by a hardware source. Figure 23.52 shows the setting example.

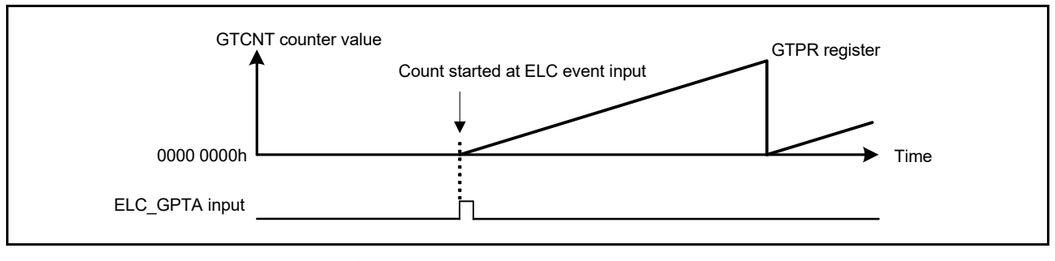
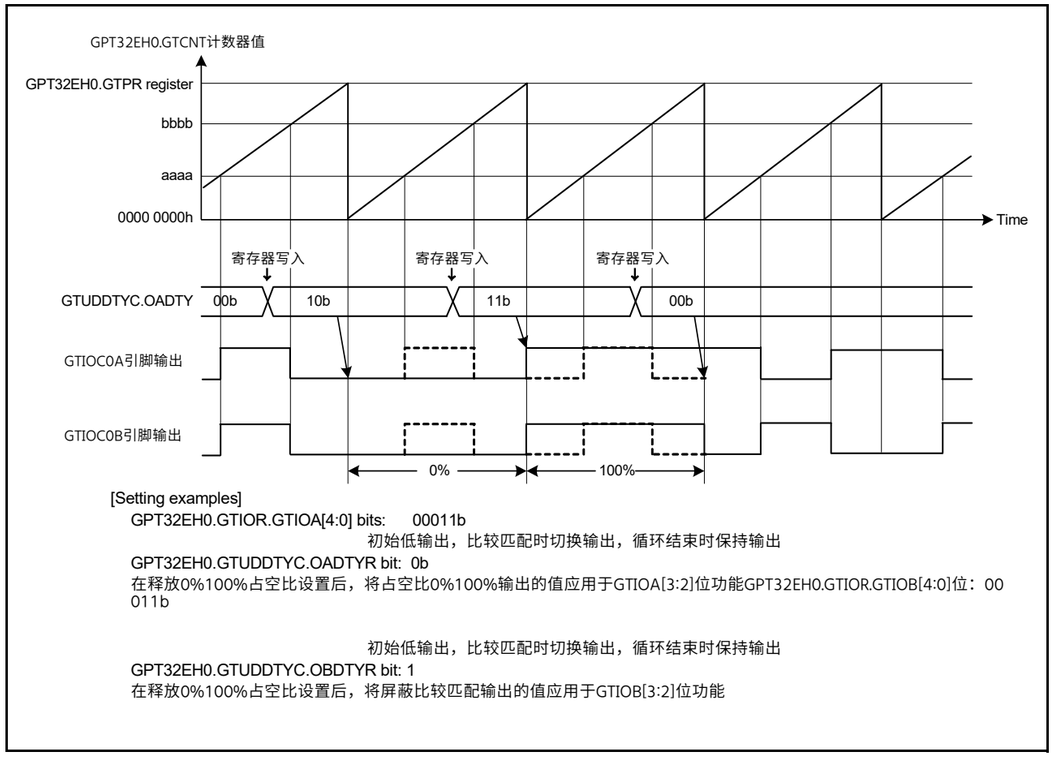


Figure 23.51 Example of count start operation by hardware source, started at the input of the signal from ELC_GPTA



[Setting examples]

GPT32EH0.GTIOR.GTIOA[4:0] bits: 00011b
初始低输出，比较匹配时切换输出，循环结束时保持输出

GPT32EH0.GTUDDTYC.OADTYR bit: 0b
在释放0%100%占空比设置后，将占空比0%100%输出的值应用于GTIOA[3:2]位功能GPT32EH0.GTIOR.GTIOB[4:0]位：00011b

初始低输出，比较匹配时切换输出，循环结束时保持输出

GPT32EH0.GTUDDTYC.OBDTYR bit: 1
在释放0%100%占空比设置后，将屏蔽比较匹配输出的值应用于GTIOB[3:2]位功能

Figure 23.50 输出占空比0%和100%功能示例

23.3.7 硬件计数开始计数停止和清除操作

GTCNT计数器可以由以下硬件源启动、停止或清除：

- 外部触发输入
- ELC事件输入
- GTIOCAGTIOCB引脚输入。

23.3.7.1 硬件启动操作

GTCNT计数器可以通过使用GTSSR选择硬件源来启动。

图23.51显示了一个硬件源的计数开始操作示例。图23.52显示了设置示例。

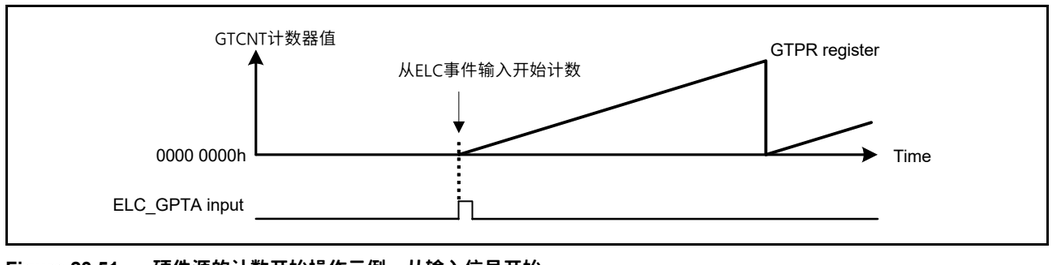


Figure 23.51 硬件源的计数开始操作示例，从输入信号开始ELC_GPTA

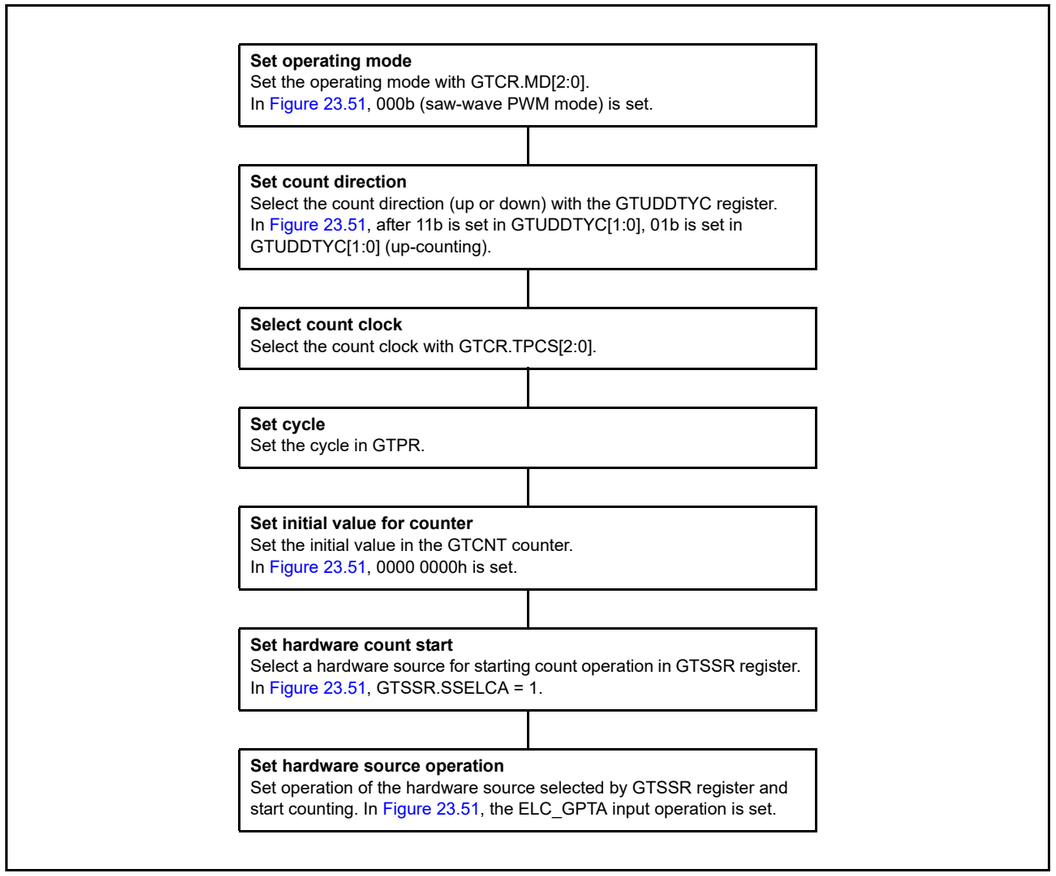


Figure 23.52 Example setting for count start operation by a hardware source

23.3.7.2 Hardware stop operation

The GTCNT counter can be stopped by selecting a hardware source using GTPSR. Figure 23.53 shows an example of a count stop operation by a hardware source. Figure 23.54 shows the setting example. In this example, the count operation stops and restarts at the edge of the ELC event input.

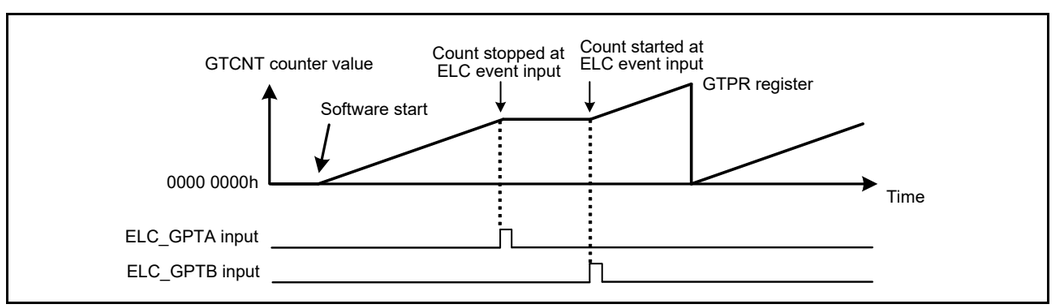


Figure 23.53 Example of count stop operation by hardware source started by software, stopped at ELC_GPTA input, and restarted at ELC_GPTB input

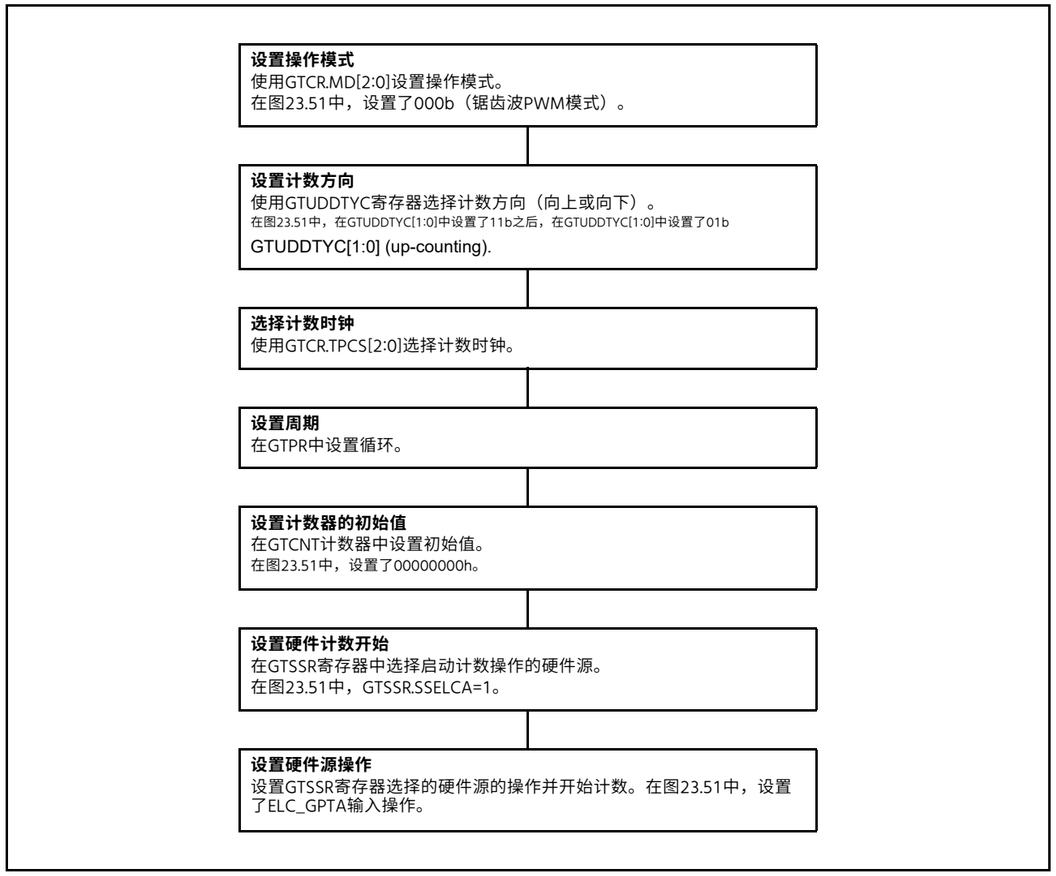


Figure 23.52 硬件源的计数开始操作设置示例

23.3.7.2 硬件停止操作

GTCNT计数器可以通过使用GTPSR选择硬件源来停止。图23.53显示了一个硬件源的计数停止操作示例。图23.54显示了设置示例。在本例中，计数操作在ELC事件输入的边沿停止并重新开始。

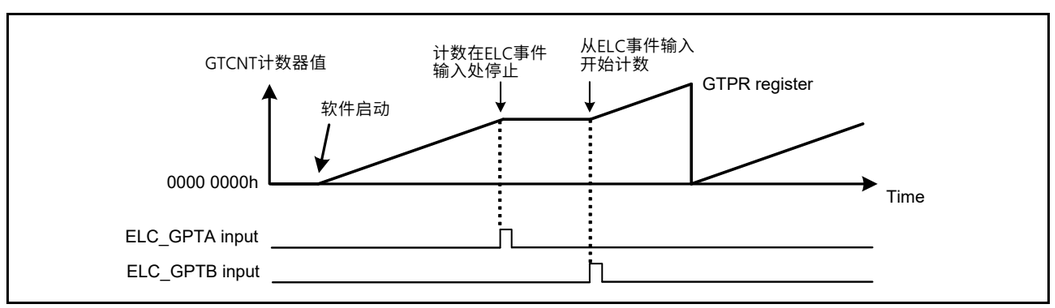


Figure 23.53 由软件启动、在ELC_GPTA输入处停止、在ELC_GPTB输入处重新启动的硬件源的计数停止操作示例

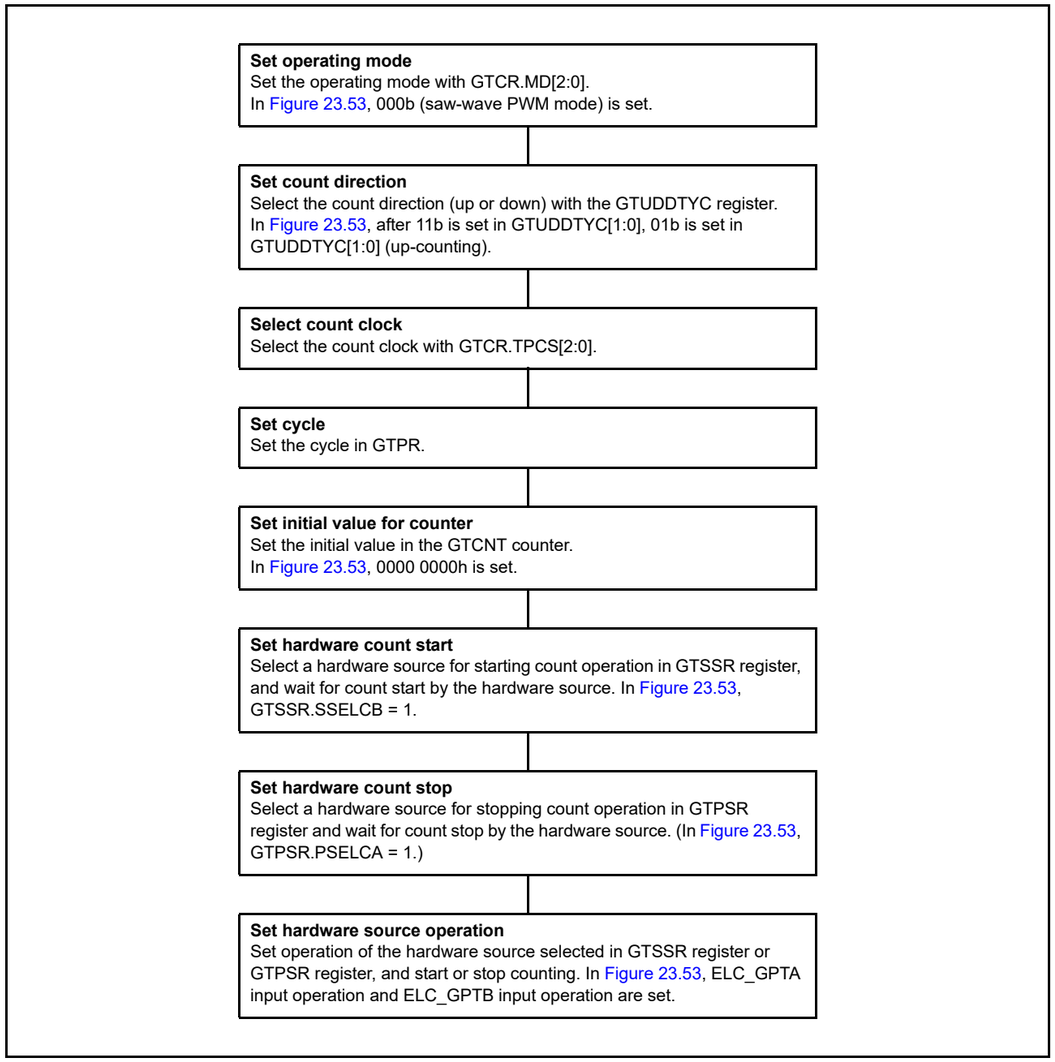


Figure 23.54 Example setting for count stop operation by a hardware source

Figure 23.55 shows an example of a count start/stop operation by a hardware source. Figure 23.56 shows the setting example. In this example, the counter operates during the high-level periods of the external trigger input GTETRGA.

Figure 23.54 硬件源的计数停止操作设置示例

图23.55显示了一个硬件源的计数开始停止操作示例。图23.56显示了设置示例。在本例中，计数器在外部触发输入GTETRGA的高电平期间运行。

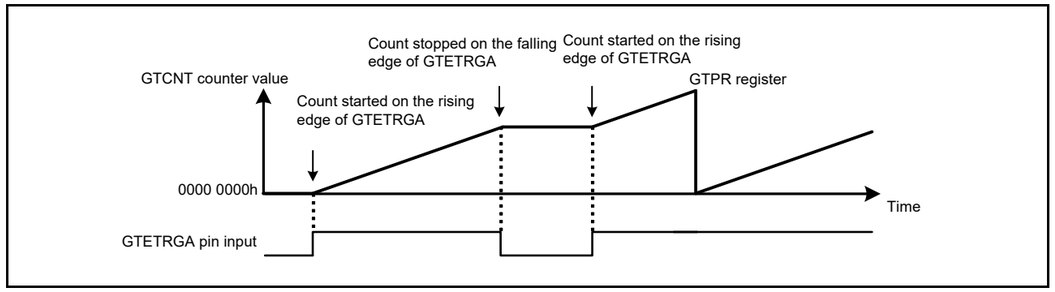


Figure 23.55 Example of count start/stop operation by hardware source, started on the rising edge of the GTETRGA pin input and stopped on the falling edge of the GTETRGA pin input

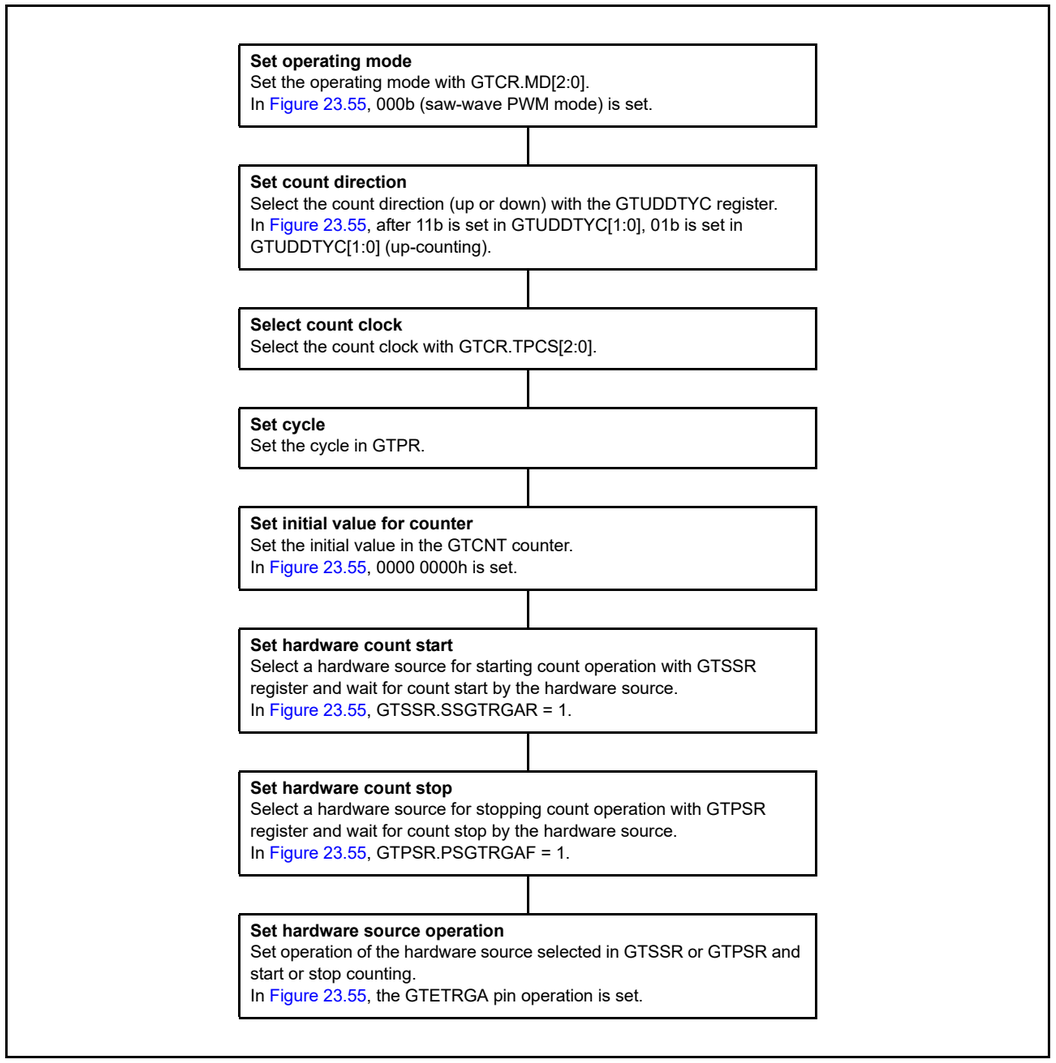


Figure 23.56 Example setting for count start/stop operation by a hardware source

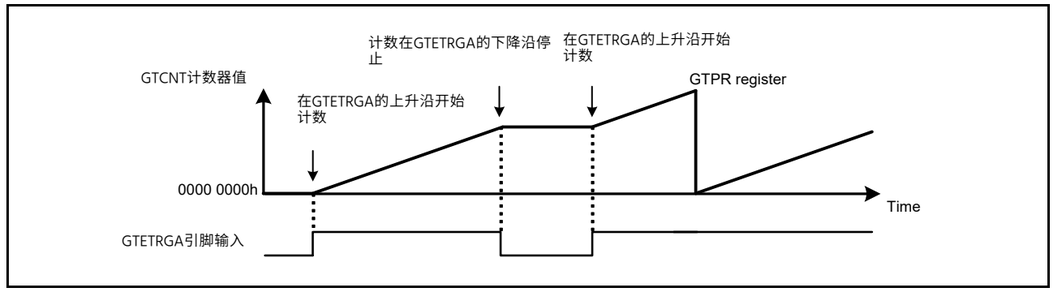


Figure 23.55 硬件源的计数开始停止操作示例，在上升沿开始GTETRGA引脚输入并在GTETRGA引脚输入的下降沿停止

Figure 23.56 硬件源的计数开始停止操作设置示例

23.3.7.3 Hardware clear operation

The GTCNT counter can be cleared by selecting a hardware source using GTCSR. The GPTn_OVF/GPTn_UDF (n = 0 to 13) interrupt (overflow/underflow interrupt) is not generated when the GTCNT counter is cleared by a hardware source or by software.

Figure 23.57 and Figure 23.58 show examples of the GTCNT counter clearing operation by a hardware source. Figure 23.59 shows the setting example. In this example, the GTCNT counter starts at the edge of the ELC_GPTA input, and the counter stops/clears at the edge of the ELC_GPTB input.

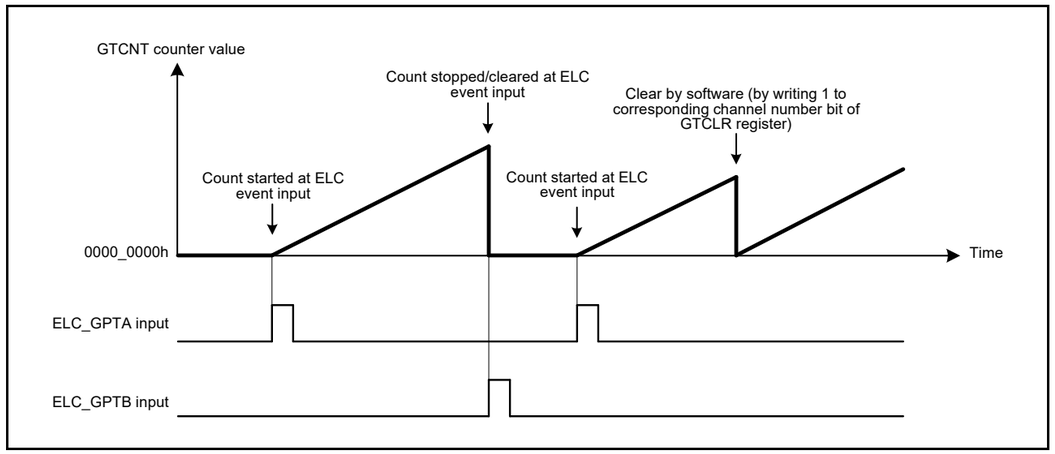


Figure 23.57 Examples of count clearing operation by hardware source with saw wave up-counting, started at ELC_GPTA input, and stopped/cleared at ELC_GPTB input

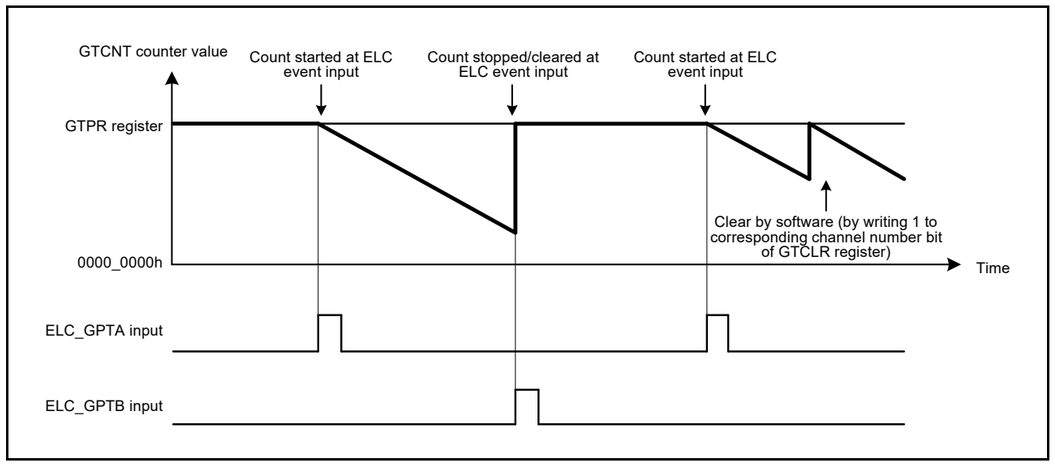


Figure 23.58 Examples of count clearing operation by hardware source with saw wave down-counting, started at ELC_GPTA input, and stopped/cleared at ELC_GPTB input

23.3.7.3 硬件清除操作

GTCNT计数器可以通过使用GTCSR选择硬件源来清除。GPTn_OVFGPTn_UDF（n=0到13）中断（溢出下溢中断）不会在GTCNT计数器被硬件源或软件清零时产生。

图23.57和图23.58显示了通过硬件源清除GTCNT计数器操作的示例。图23.59显示了设置示例。在本例中，GTCNT计数器在ELC_GPTA输入的边沿开始，计数器在ELC_GPTB输入的边沿停止并清零。

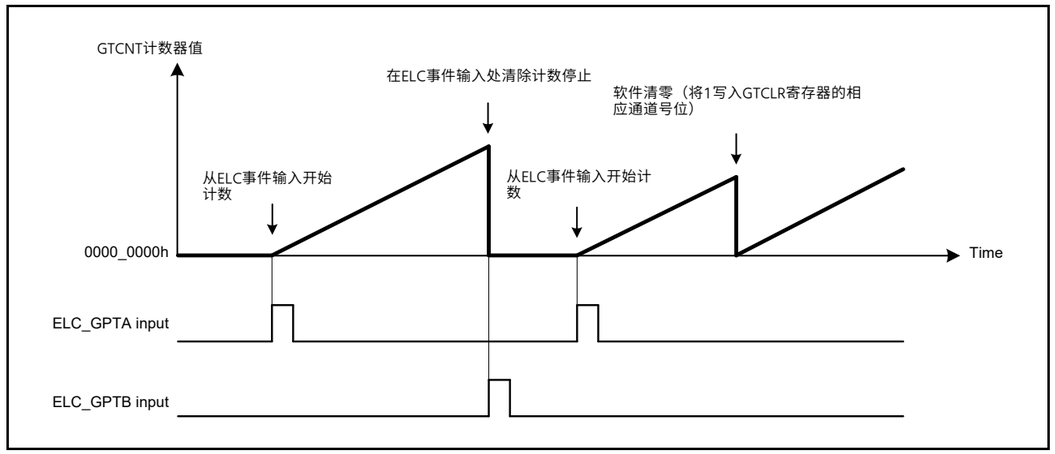


Figure 23.57 使用锯波递增计数的硬件源的计数清除操作示例，开始于ELC_GPTA输入，并在ELC_GPTB输入处停止清除

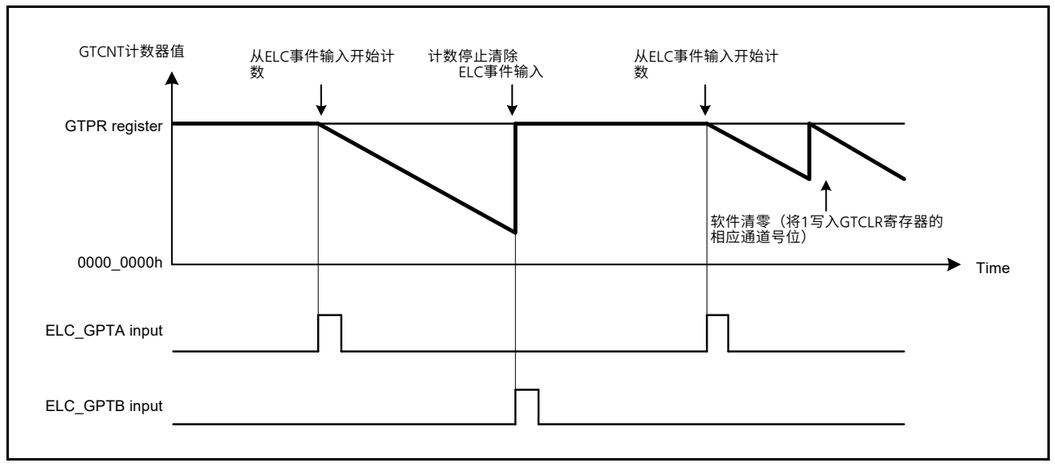


Figure 23.58 使用锯波递减计数的硬件源的计数清除操作示例，在ELC_GPTA输入处开始，在ELC_GPTB输入处停止清除

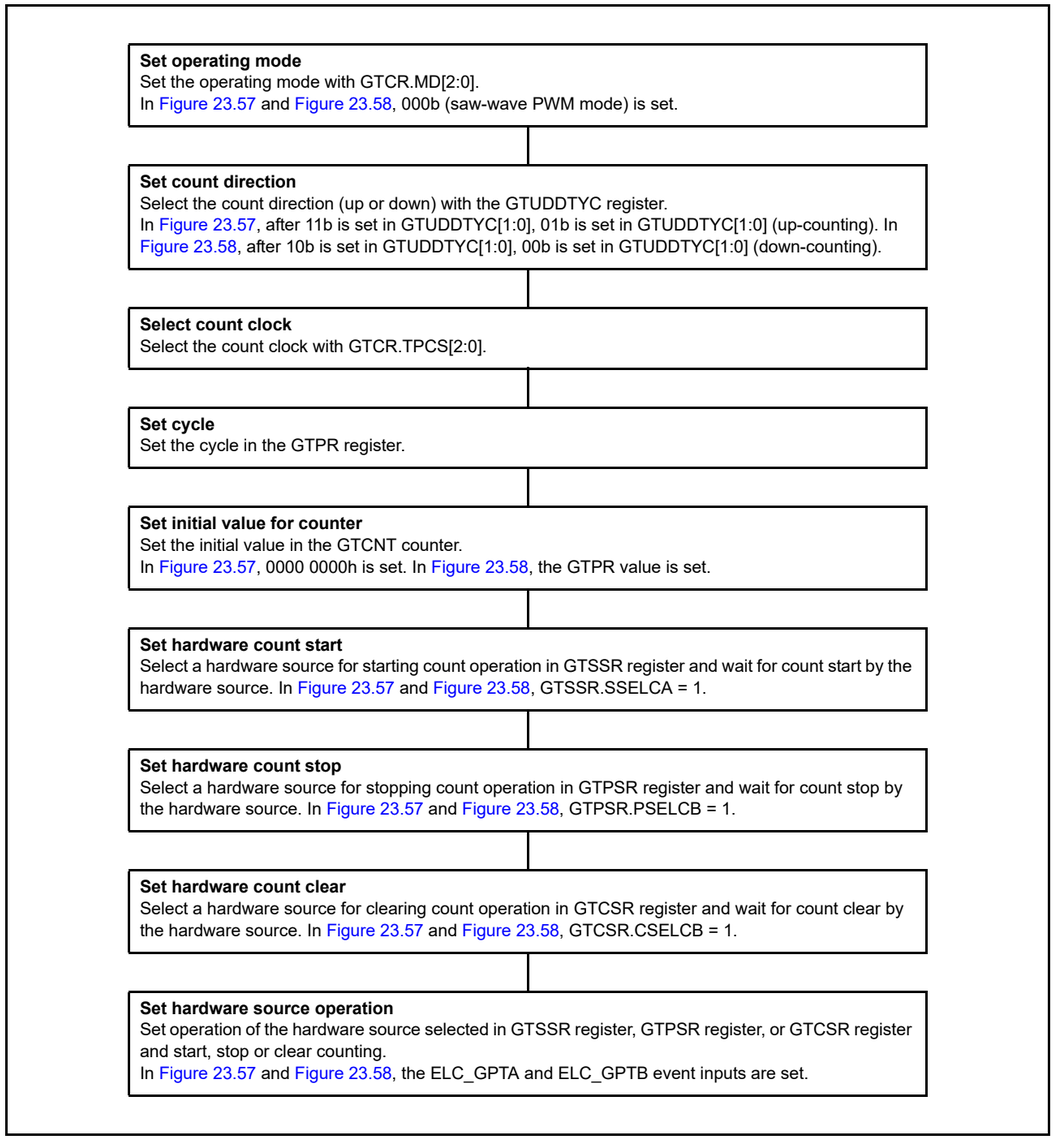


Figure 23.59 Example setting for count clearing operation by a hardware source

The GPTn_OVF/GPTn_UDF (n = 0 to 13) interrupt (overflow/underflow interrupt) is not generated when the counter is cleared by a hardware source or by software.

Figure 23.60 shows the relationship between the counter clearing by a hardware source and the GPTn_OVF (n = 0 to 13) interrupt.

Figure 23.59 通过硬件源进行计数清除操作的示例设置

GPTn_OVFGPTn_UDF（n=0到13）中断（溢出下溢中断）不会在计数器被硬件源或软件清零时产生。

图23.60显示了通过硬件源清除计数器和GPTn_OVF（n=0到13）中断之间的关系。

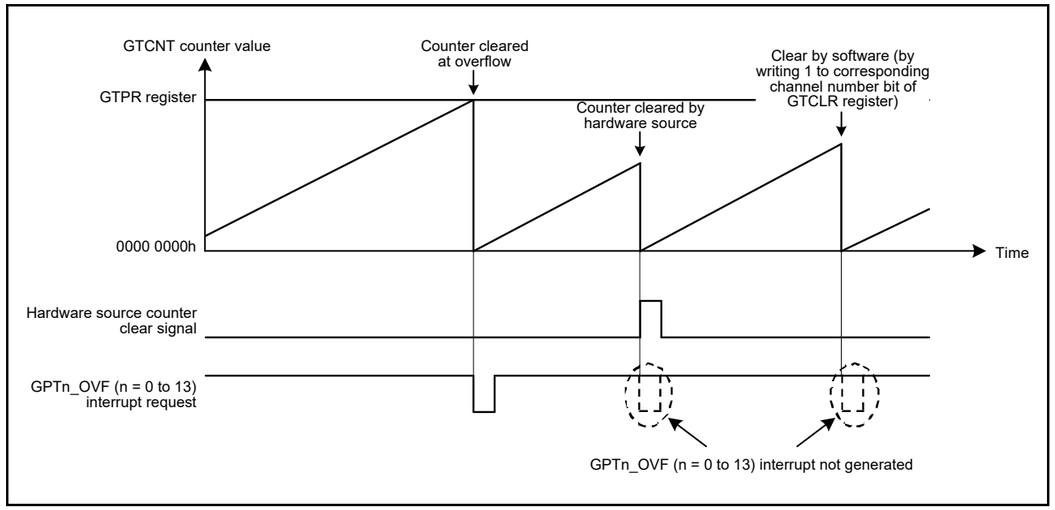


Figure 23.60 Relationship between counter clearing by hardware source and GPTn_OVF (n = 0 to 13) interrupt

23.3.8 Synchronized Operation

Synchronized operation on channels such as a synchronized start, stop, and clear operation can be performed.

23.3.8.1 Synchronized operation by software

The GTCNT counters can be started, stopped, and cleared on multiple channels by setting the associated GTSTR, GTSTP, or GTCLR bits simultaneously to 1.

Count start with a phase difference is possible by setting the initial value in the GTCNT counter and setting the associated GTSTR bits simultaneously to 1.

Figure 23.61 shows an example of a simultaneous start, stop, and clear by software. Figure 23.62 shows an example of phase start operation by software.

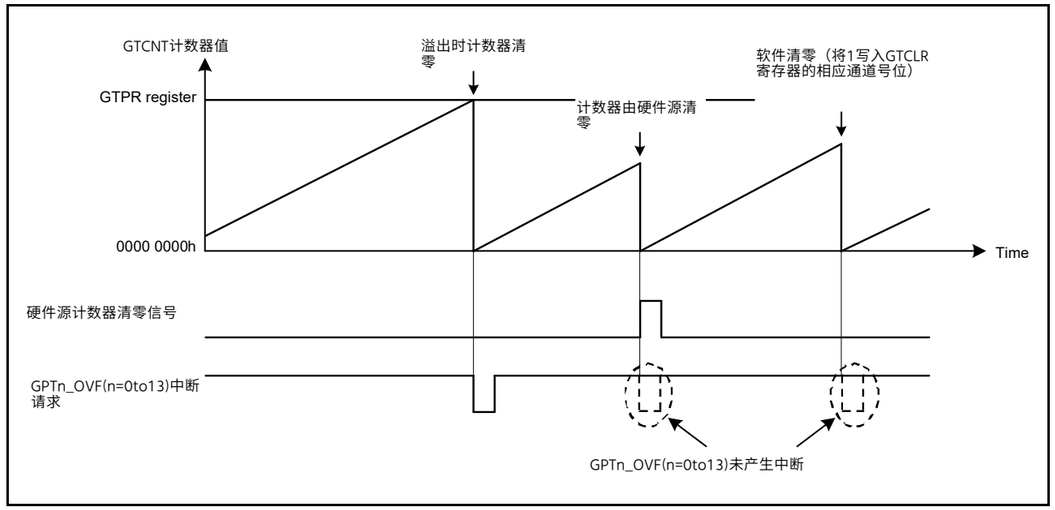


Figure 23.60 硬件源计数器清零与GPTn_OVF(n=0to13)中断的关系

23.3.8 同步操作

可以对通道进行同步操作，例如同步启动、停止和清除操作。

23.3.8.1 软件同步操作

通过设置相关的GTSTR，可以在多个通道上启动、停止和清除GTCNT计数器，GTSTP或GTCLR位同时为1。

通过在GTCNT计数器中设置初始值并同时将相关的GTSTR位设置为1，可以从相位差开始计数。

图23.61显示了通过软件同时启动、停止和清除的示例。图23.62显示了通过软件进行相位启动操作的示例。

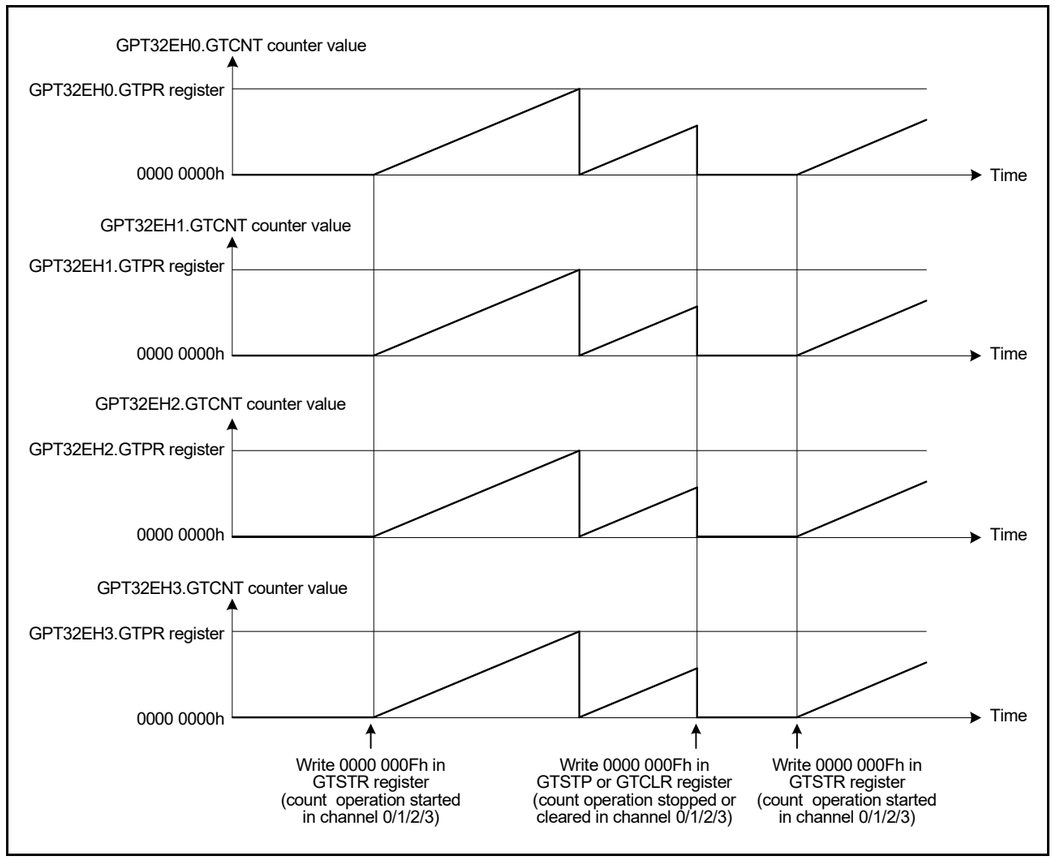


Figure 23.61 Example of a simultaneous start, stop, and clear by software, with the same count cycle (GTPR register value)

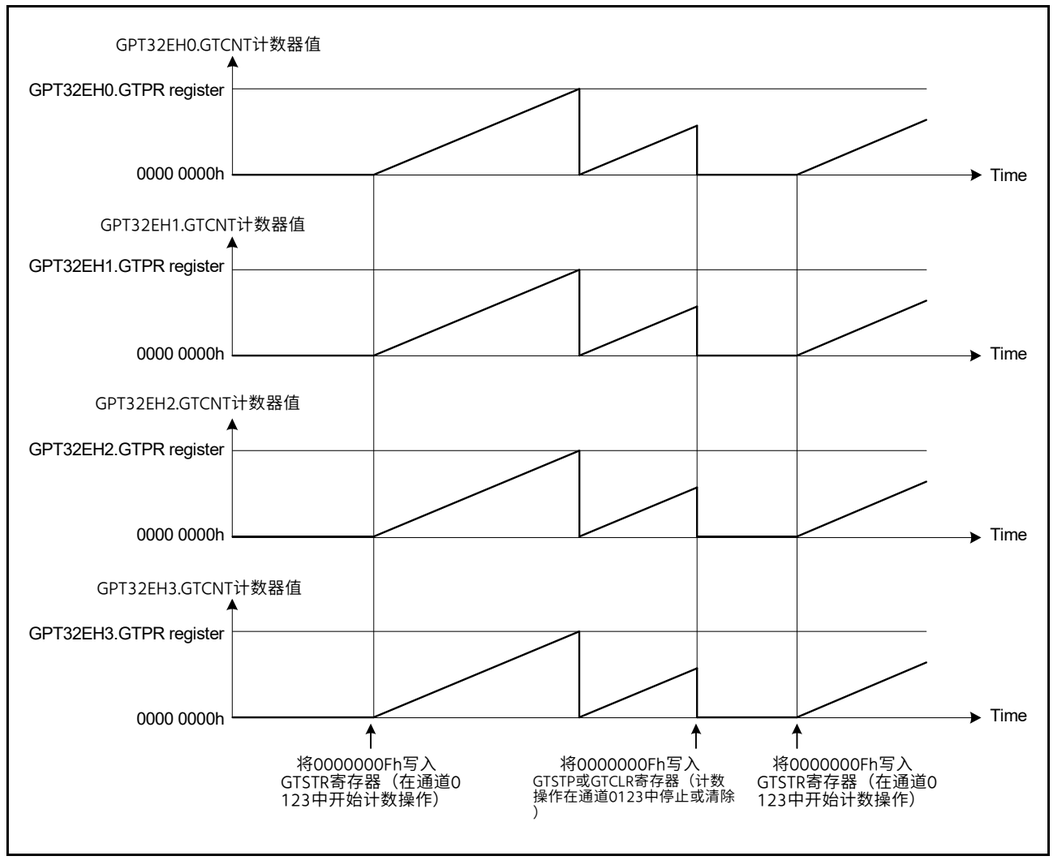


Figure 23.61 通过软件同时启动、停止和清除的示例，具有相同的计数周期（GTPR寄存器值）

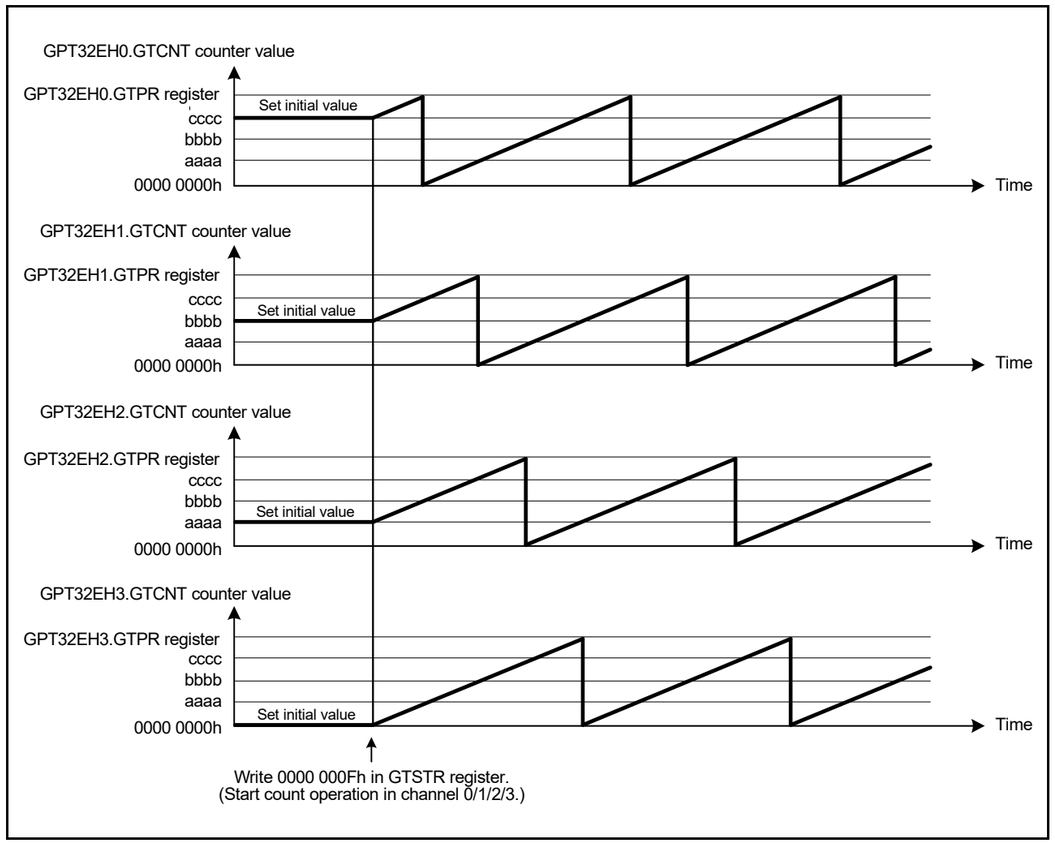


Figure 23.62 Example of software phase start with the same count cycle (GTPR register value)

23.3.8.2 Synchronized operation by hardware

The GTCNT counters can be started simultaneously by the following hardware sources:

- External trigger input
- ELC event input.

Figure 23.63 shows an example of a simultaneous start, stop, and clear operation by a hardware source. Figure 23.64 shows the setting example.

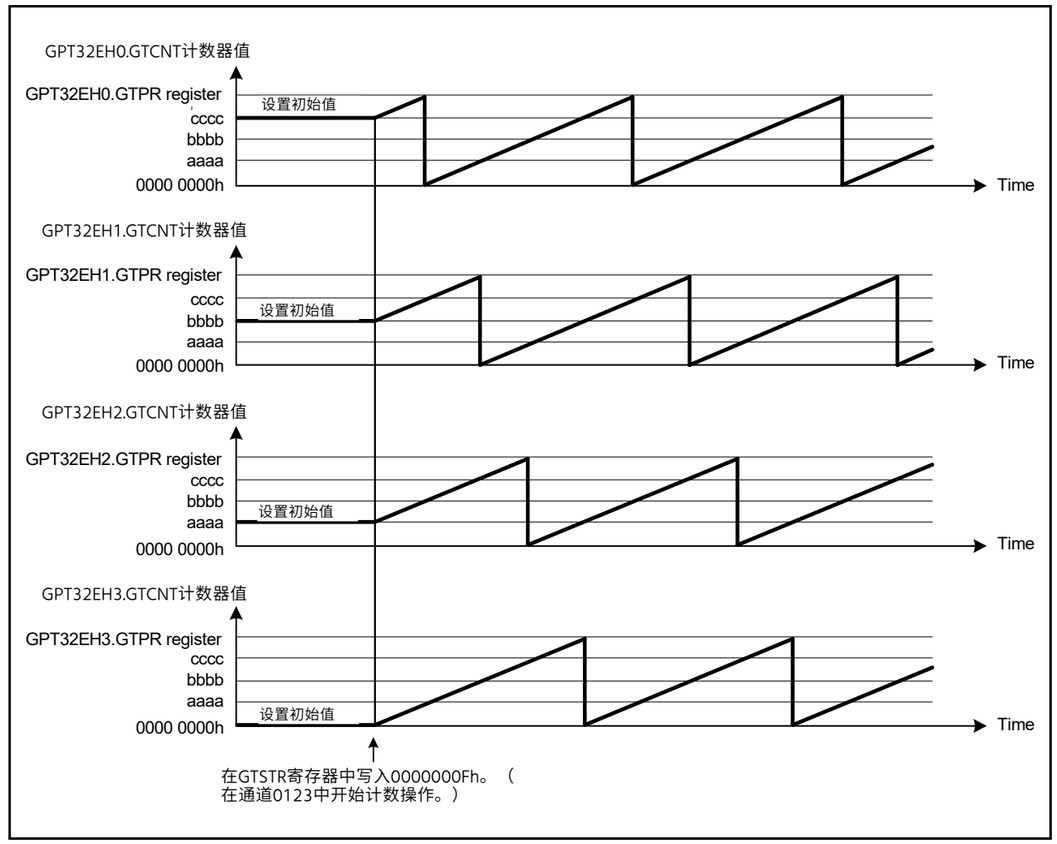


Figure 23.62 以相同计数周期开始的软件阶段示例（GTPR寄存器值）

23.3.8.2 硬件同步操作

GTCNT计数器可以由以下硬件源同时启动：

- 外部触发输入
- ELC事件输入。

图23.63显示了一个硬件源同时启动、停止和清除操作的示例。图23.64显示了设置示例。

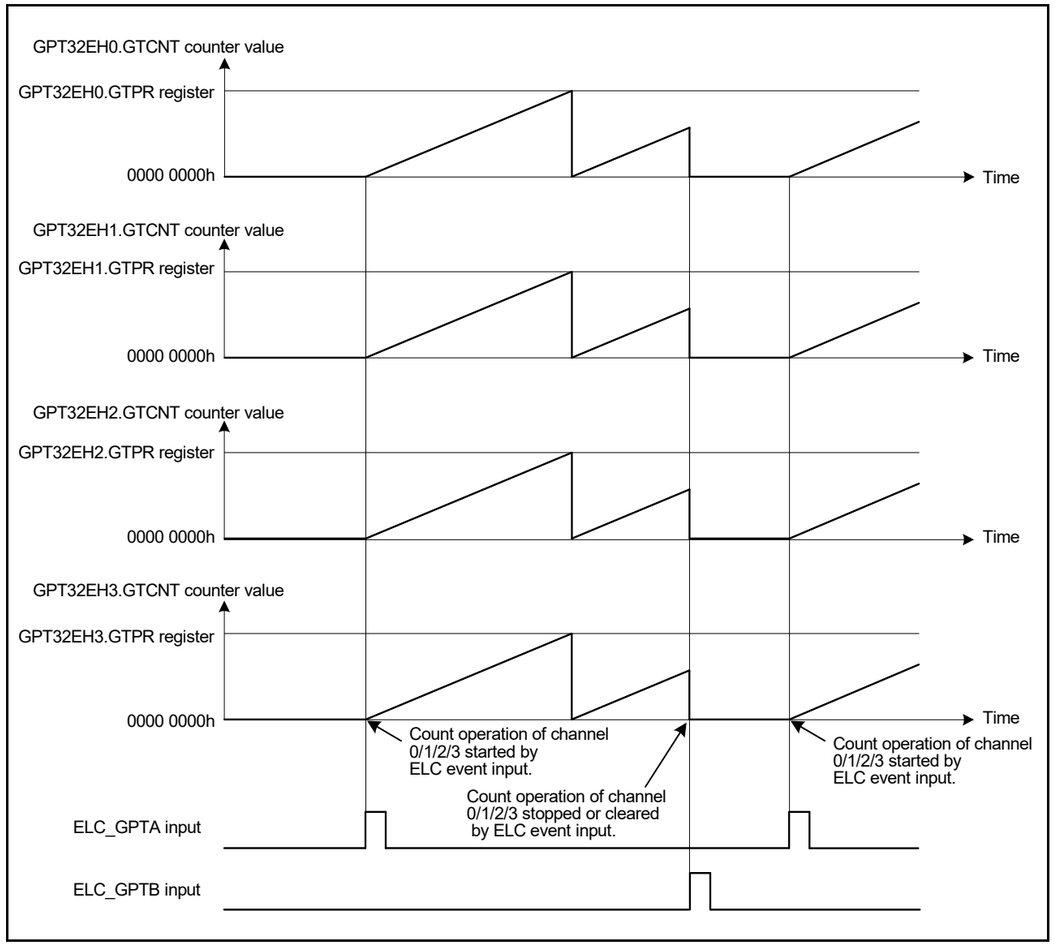


Figure 23.63 Example of a simultaneous start, stop, and clear by hardware source with the same count cycle (GTPR register value)

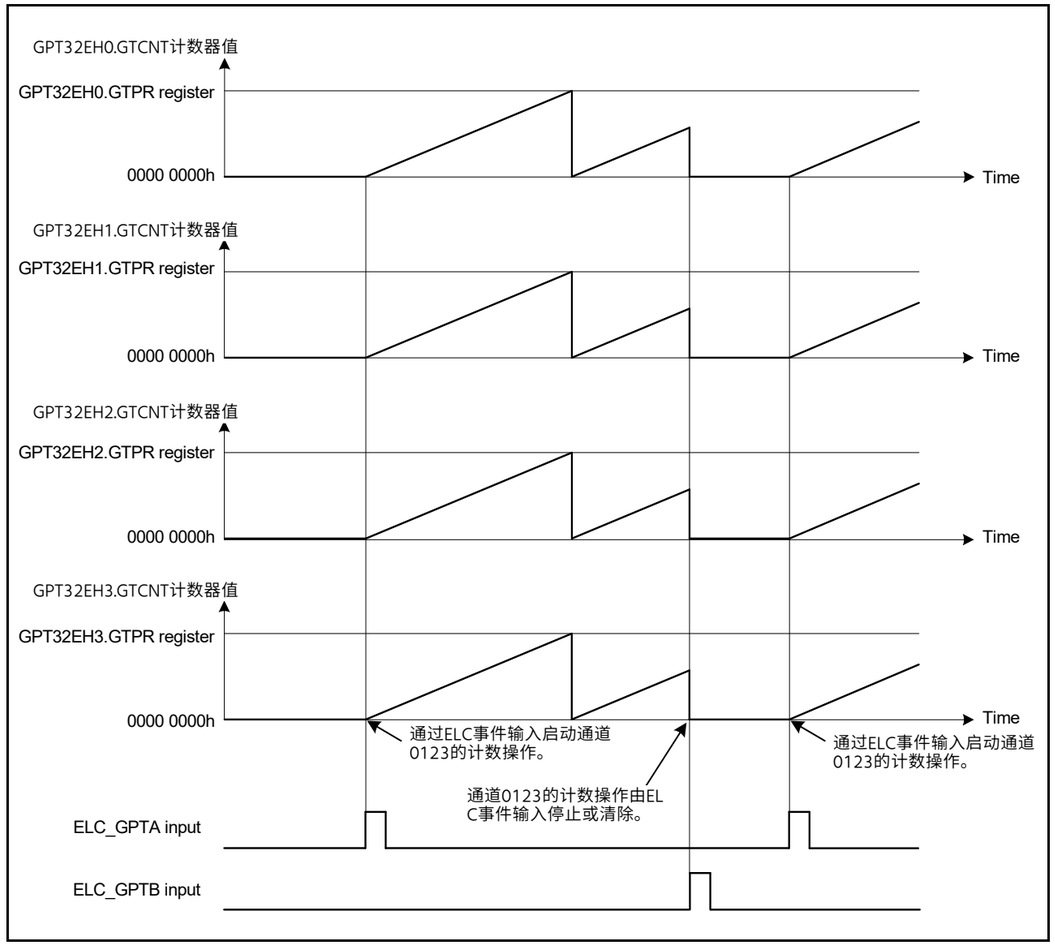


Figure 23.63 具有相同计数周期（GTPR寄存器值）的硬件源同时启动、停止和清除的示例

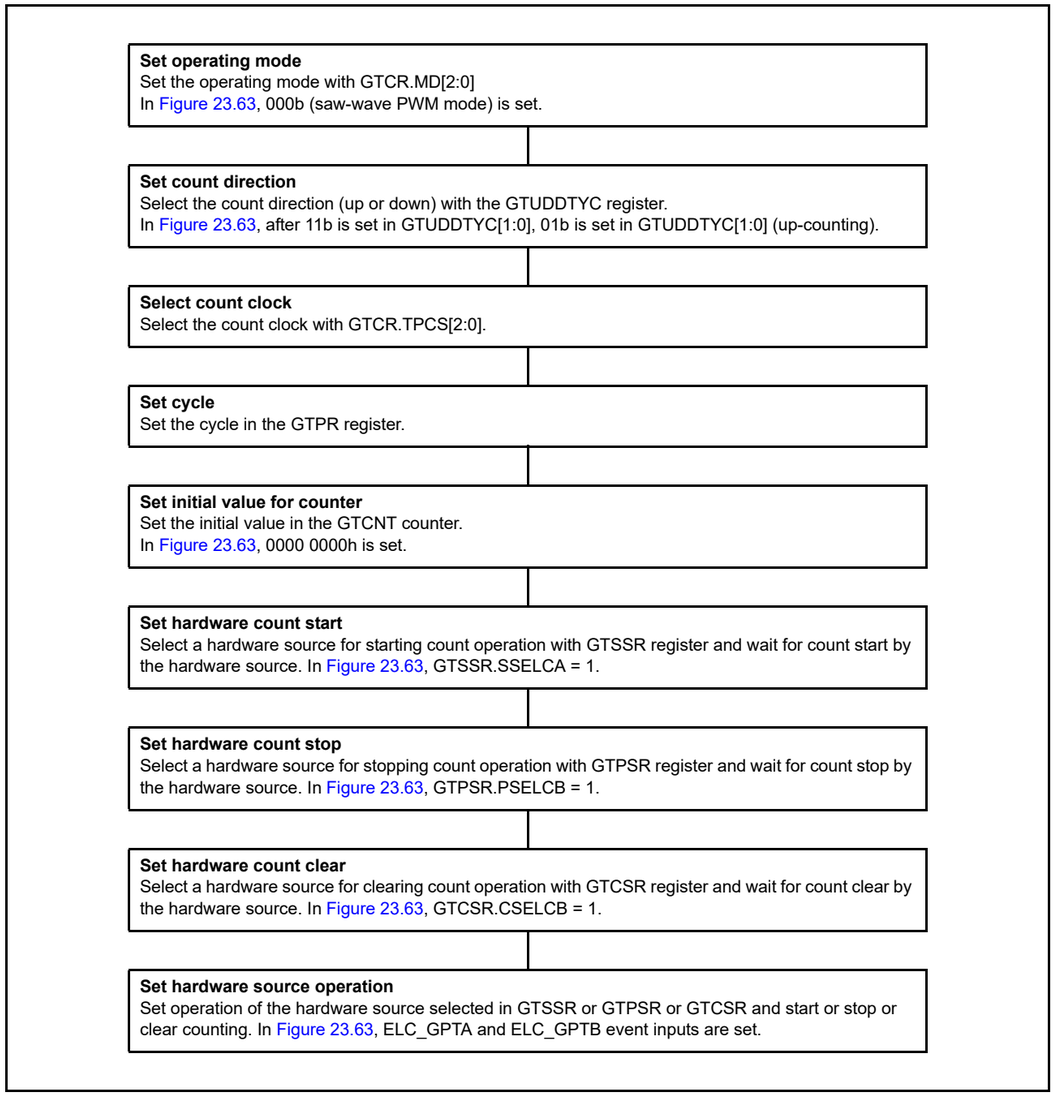


Figure 23.64 Example setting for simultaneous start by hardware source

23.3.9 PWM Output Operation Examples

(1) Synchronized PWM output

The GPT outputs 28 phases of linked PWM waveforms for a maximum of 14 channels by multiple GPTs.

Figure 23.65 shows an example in which four channels perform synchronized operation in saw-wave PWM mode and eight phases of PWM waveforms are output. The GTIOCA is set so that it outputs low as the initial value, high at a GTCCRA compare match, and low at the cycle end. The GTIOCB is set so that it outputs low as the initial value, high at a GTCCRB compare match, and low at the cycle end.

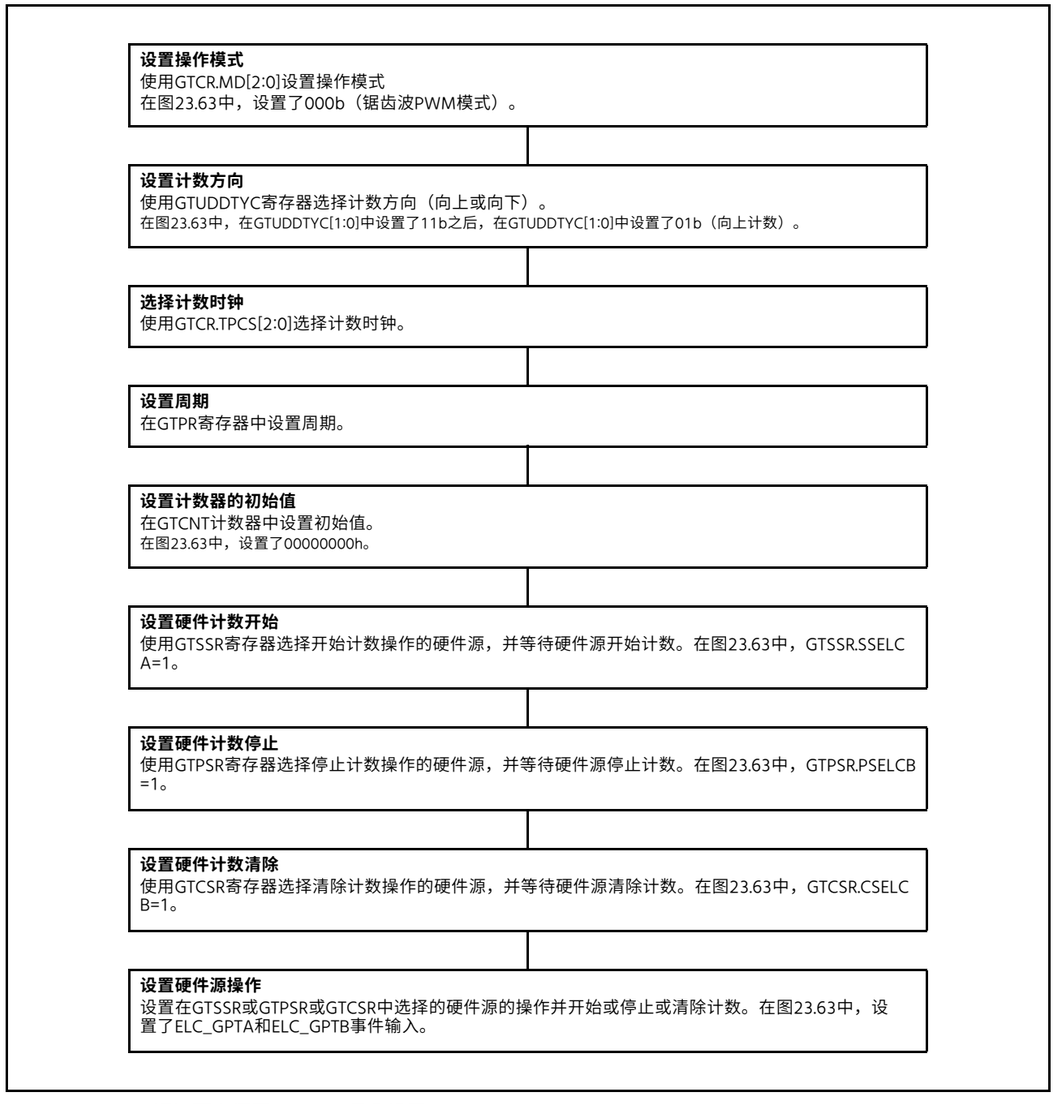


Figure 23.64 通过硬件源同时启动的示例设置

23.3.9 PWM输出操作示例

(1) 同步PWM输出

GPT通过多个GPT为最多14个通道输出28相链接的PWM波形。

图23.65显示了一个示例，其中4个通道在锯齿波PWM模式下执行同步操作并输出8相PWM波形。GTIOCA设置为输出低作为初始值，在GTCCRA比较匹配时输出高，在循环结束时输出低。GTIOCB设置为输出低作为初始值，在GTCCRB比较匹配时输出高，在循环结束时输出低。

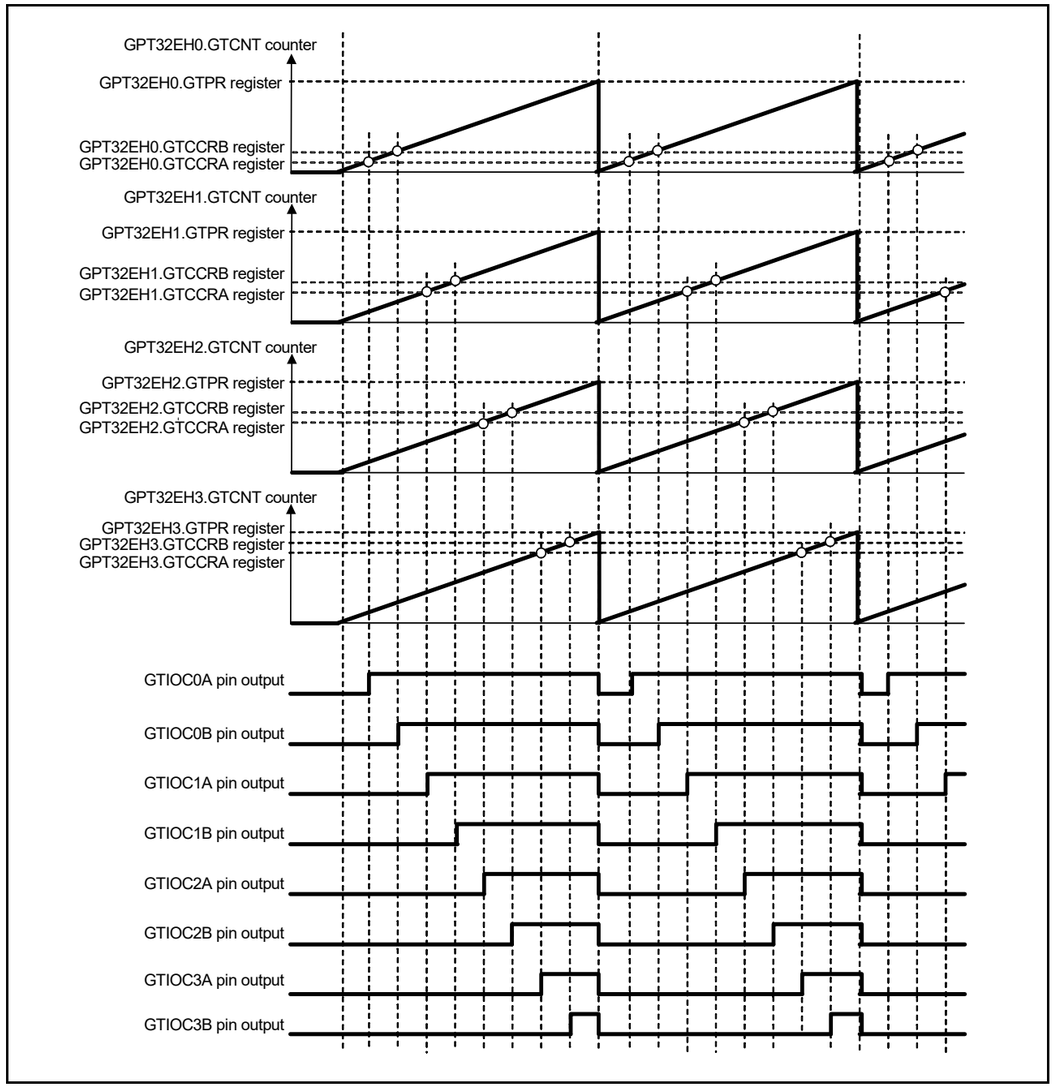


Figure 23.65 Example of synchronized PWM output

(2) 3-phase saw-wave complementary PWM output

Figure 23.66 shows an example in which three channels perform synchronized operation in saw-wave PWM mode and 3-phase complementary PWM waveforms are output. The GTIOCA pin is set so that it outputs low as the initial value, high at a GTCCRA compare match, and low at the cycle end. The GTIOCB pin is set so that it outputs high as the initial value, low at a GTCCRB compare match, and high at the cycle end.

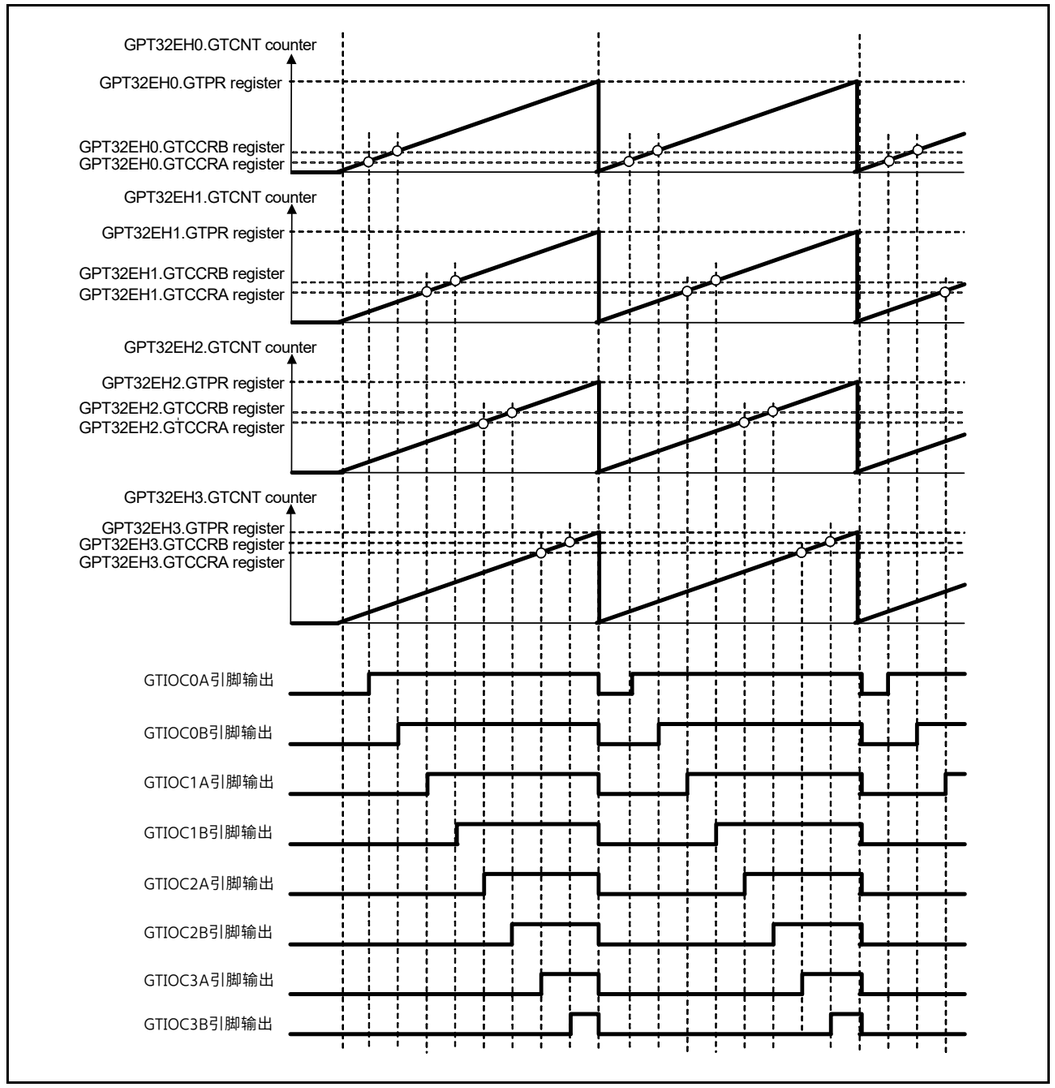


Figure 23.65 同步PWM输出示例

(2) 三相锯齿波互补PWM输出

图23.66显示了一个示例，其中三个通道在锯齿波PWM模式下执行同步操作并输出三相互补PWM波形。GTIOCA引脚设置为输出低作为初始值，在GTCCRA比较匹配时输出高，在循环结束时输出低。GTIOCB引脚设置为输出高作为初始值，在GTCCRB比较匹配时输出低，在周期结束时输出高。

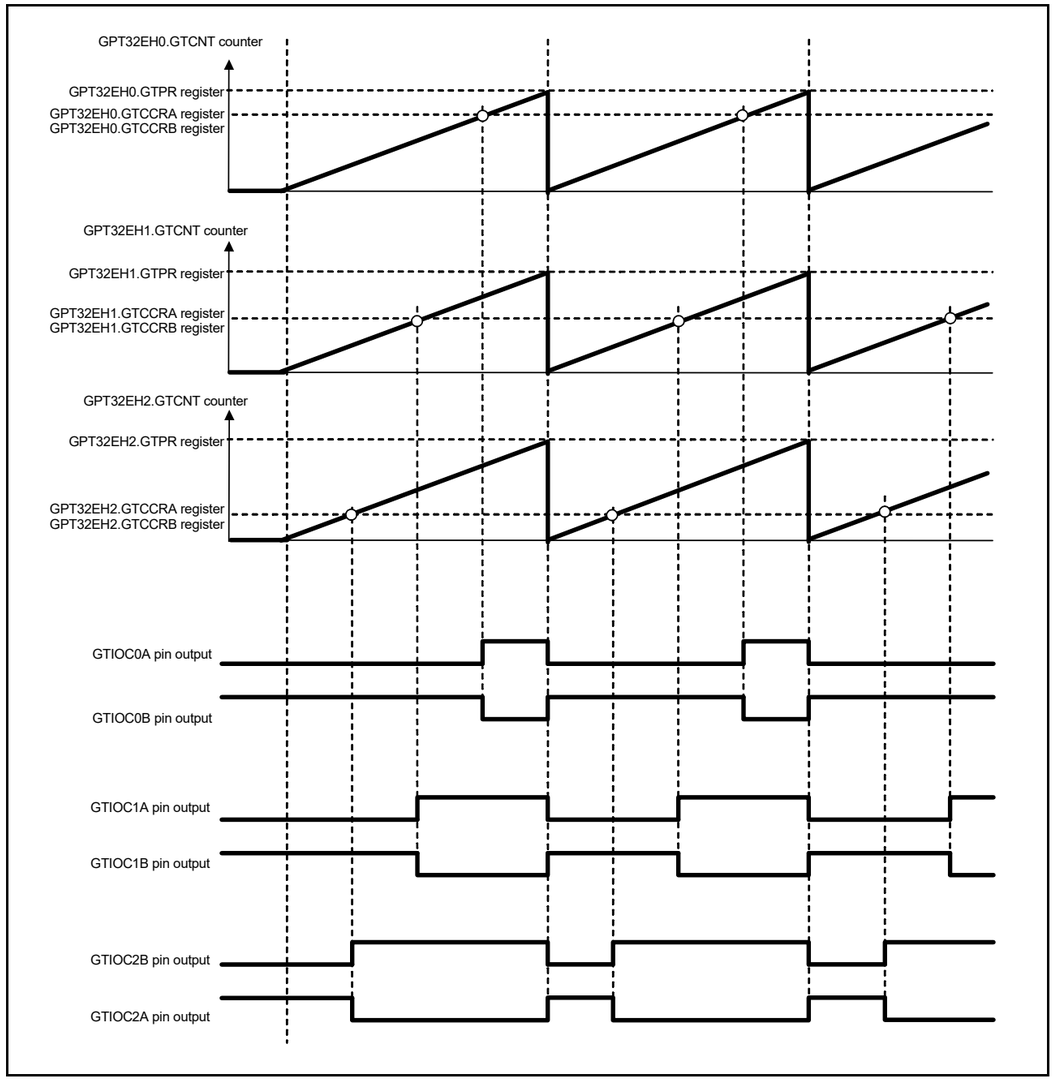


Figure 23.66 Example of 3-phase saw-wave complementary PWM output

(3) 3-phase saw-wave complementary PWM output with automatic dead time setting

Figure 23.67 shows an example in which three channels perform synchronized operation in saw-wave one-shot pulse mode with automatic dead time setting and 3-phase complementary PWM waveforms are output. The GTIOCA pin is set so that it outputs low as the initial value, toggles the output at a GTCCRA compare match, and retains the output at the cycle end. The GTIOCB pin is set so that it outputs high as the initial value, toggles the output at a GTCCRB compare match, and retains the output at the cycle end.

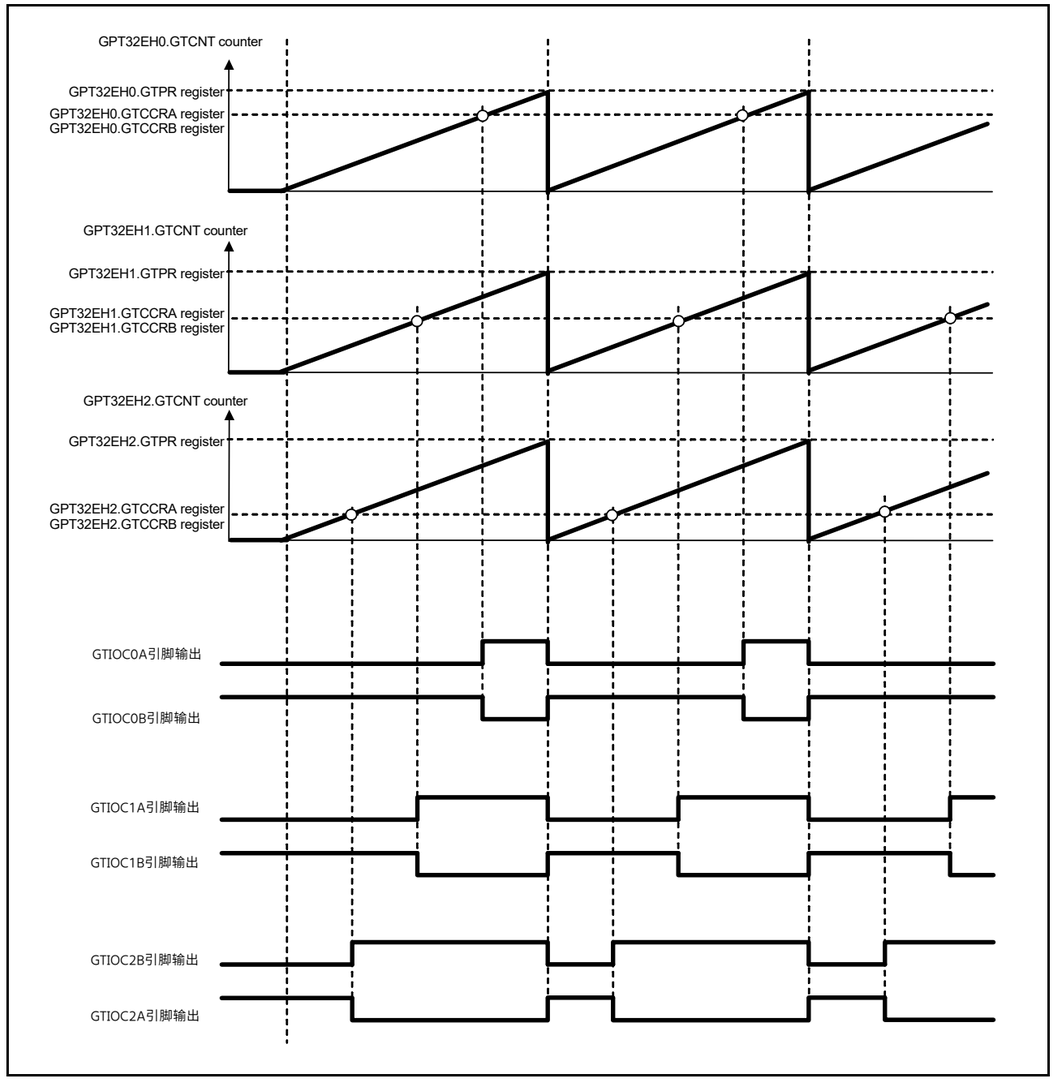


Figure 23.66 三相锯齿波互补PWM输出示例

(3) 具有自动死区时间设置的三相锯齿波互补PWM输出

图23.67显示了一个示例，其中三个通道在具有自动死区时间设置的锯齿波一次性脉冲模式下执行同步操作并输出三相互补PWM波形。GTIOCA引脚设置为输出低作为初始值，在GTCCRA比较匹配时切换输出，并在周期结束时保持输出。GTIOCB引脚设置为输出高电平作为初始值，在GTCCRB比较匹配时切换输出，并在周期结束时保持输出。

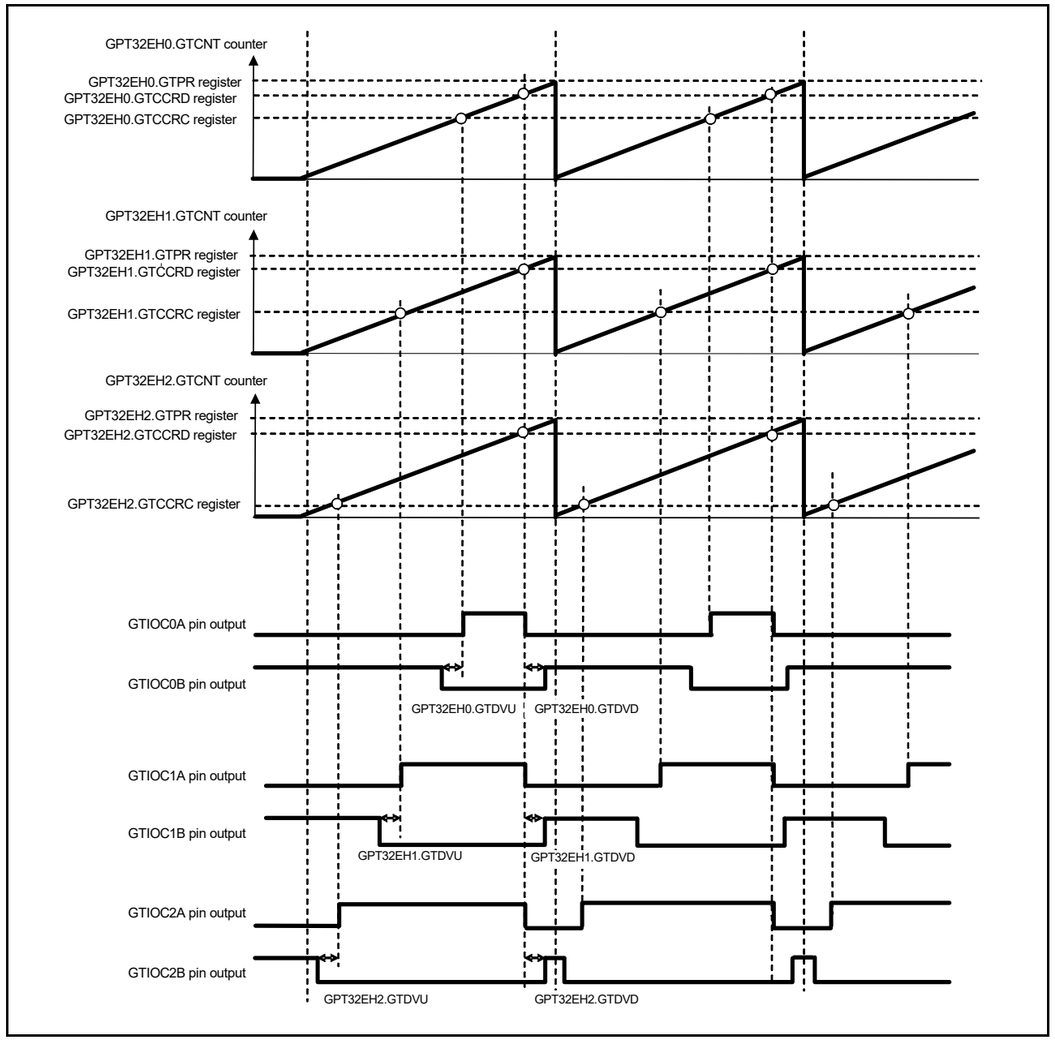


Figure 23.67 Example of 3-phase saw-wave complementary PWM output with automatic dead time setting

(4) 3-phase triangle-wave complementary PWM output

Figure 23.68 shows an example in which three channels perform synchronized operation in triangle-wave PWM mode 1 and 3-phase complementary PWM waveforms are output. The GTIOCA pin is set so that it outputs low as the initial value, toggles the output at a GTCCRA compare match, and retains the output at the cycle end. The GTIOCB pin is set so that it outputs high as the initial value, toggles the output at a GTCCRB compare match, and retains the output at the cycle end.

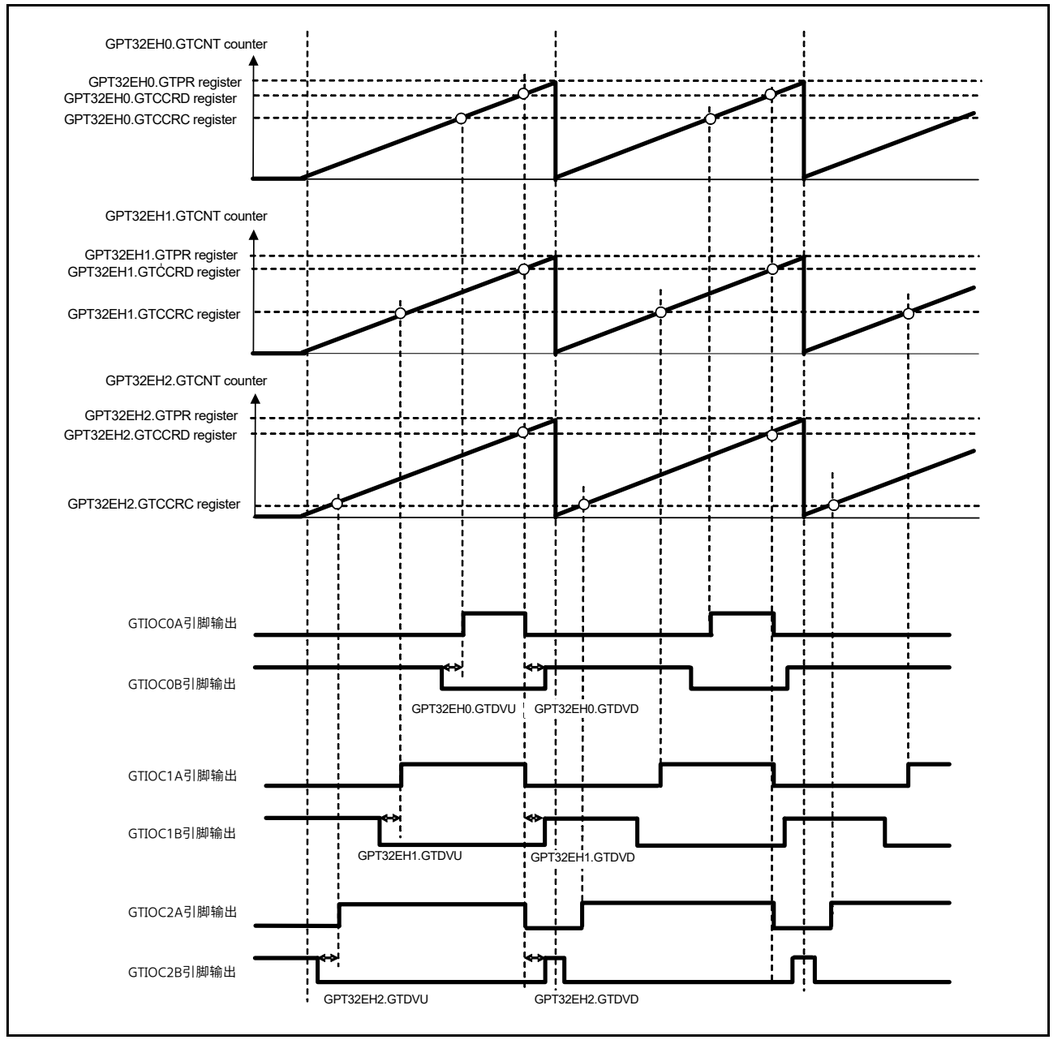


Figure 23.67 具有自动死区时间设置的三相锯齿波互补PWM输出示例

(4) 三相三角波互补PWM输出

图23.68显示了一个示例，其中三个通道在三角波PWM模式1中执行同步操作并输出三相互补PWM波形。GTIOCA引脚设置为输出低作为初始值，在GTCCRA比较匹配时切换输出，并在周期结束时保持输出。GTIOCB引脚设置为输出高电平作为初始值，在GTCCRB比较匹配时切换输出，并在周期结束时保持输出。

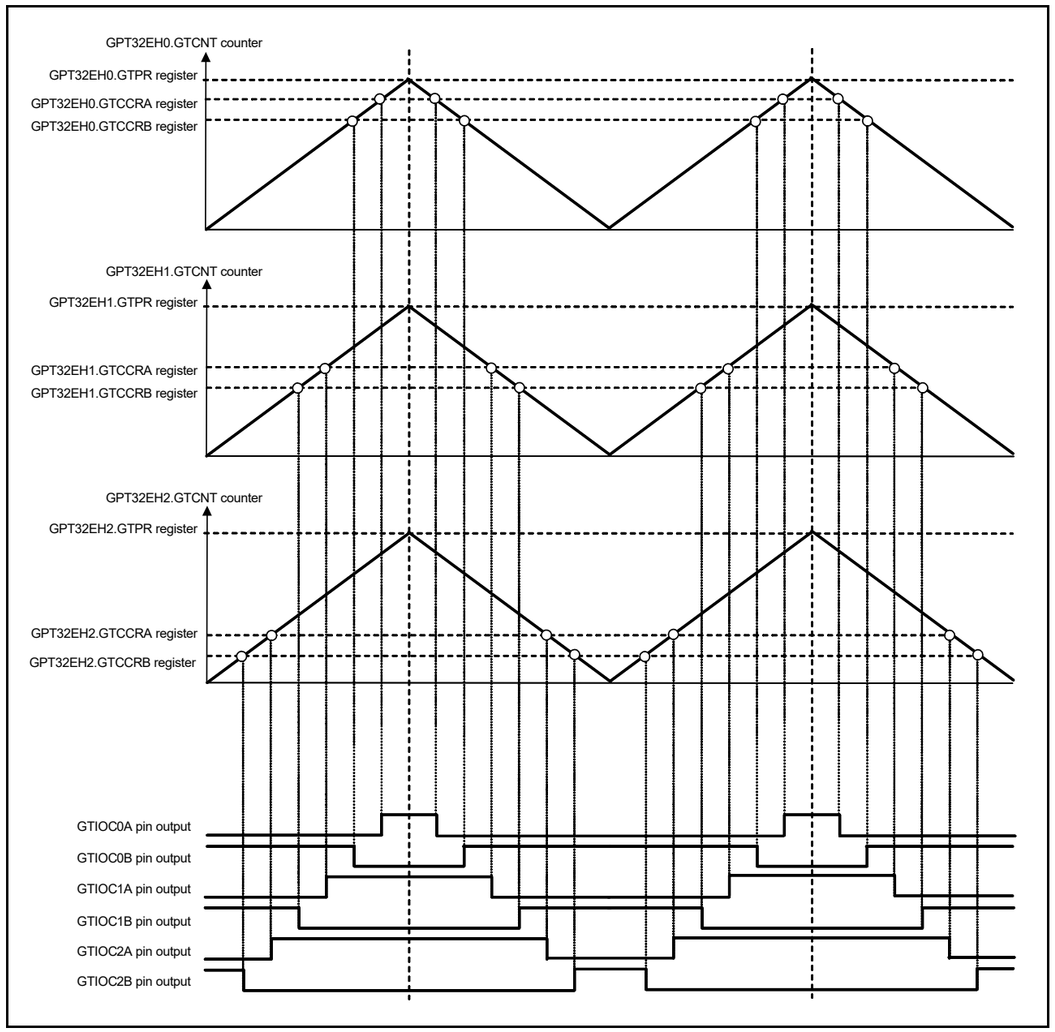


Figure 23.68 Example of 3-phase triangle-wave complementary PWM output

(5) 3-phase triangle-wave complementary PWM output with automatic dead time setting

Figure 23.69 shows an example in which three channels perform synchronized operation in triangle-wave PWM mode 1 with automatic dead time setting and 3-phase complementary PWM waveforms are output. The GTIOCA pin is set so that it outputs low as the initial value, toggles the output at a GTCCRA compare match, and retains the output at the cycle end. The GTIOCB pin is set so that it outputs high as the initial value, toggles the output at a GTCCRB compare match, and retains the output at the cycle end.

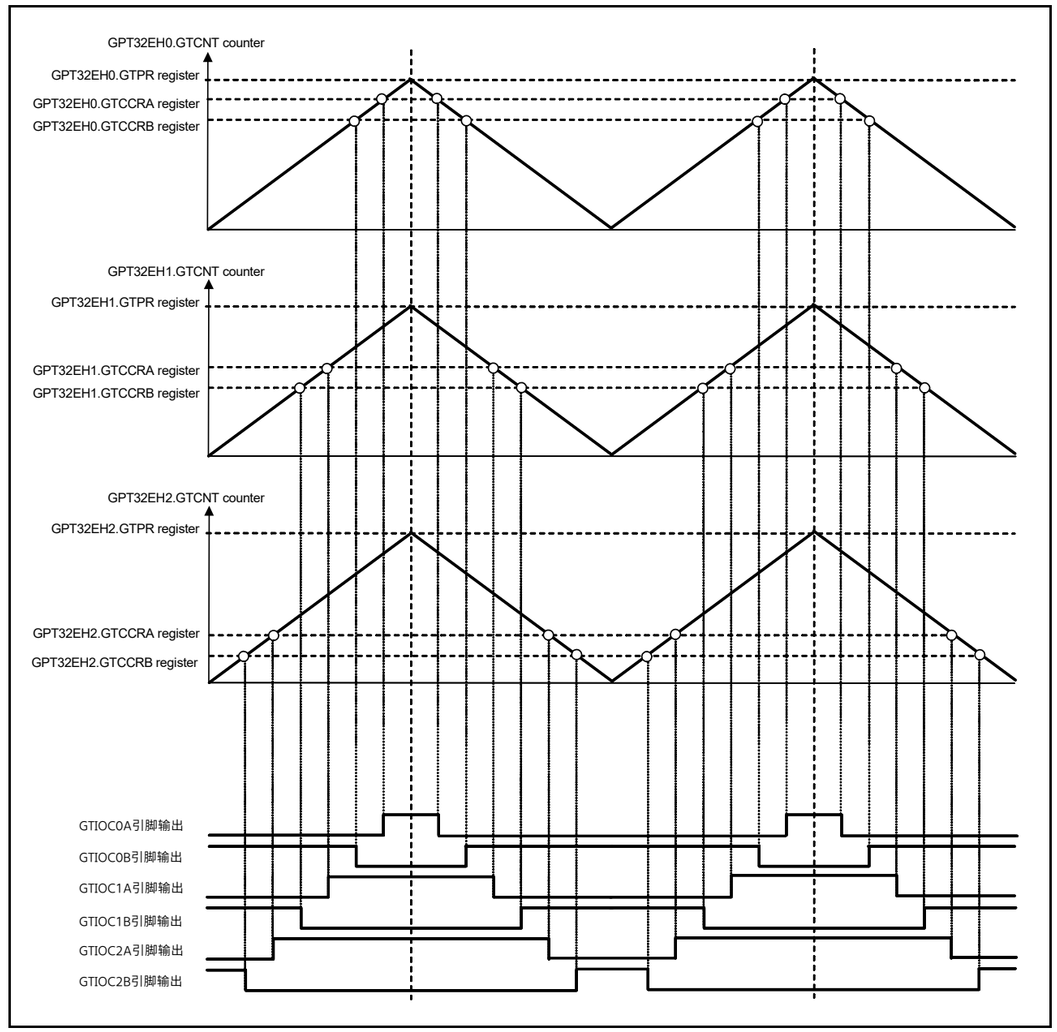


Figure 23.68 三相三角波互补PWM输出示例

(5) 具有自动死区时间设置的三相三角波互补PWM输出

图23.69显示了一个示例，其中三个通道在三角波PWM模式1下执行同步操作，自动设置死区时间并输出三相互补PWM波形。GTIOCA引脚设置为输出低电平作为初始值，在GTCCRA比较匹配时切换输出，并在周期结束时保持输出。GTIOCB引脚设置为输出高电平作为初始值，在GTCCRB比较匹配时切换输出，并在周期结束时保持输出。

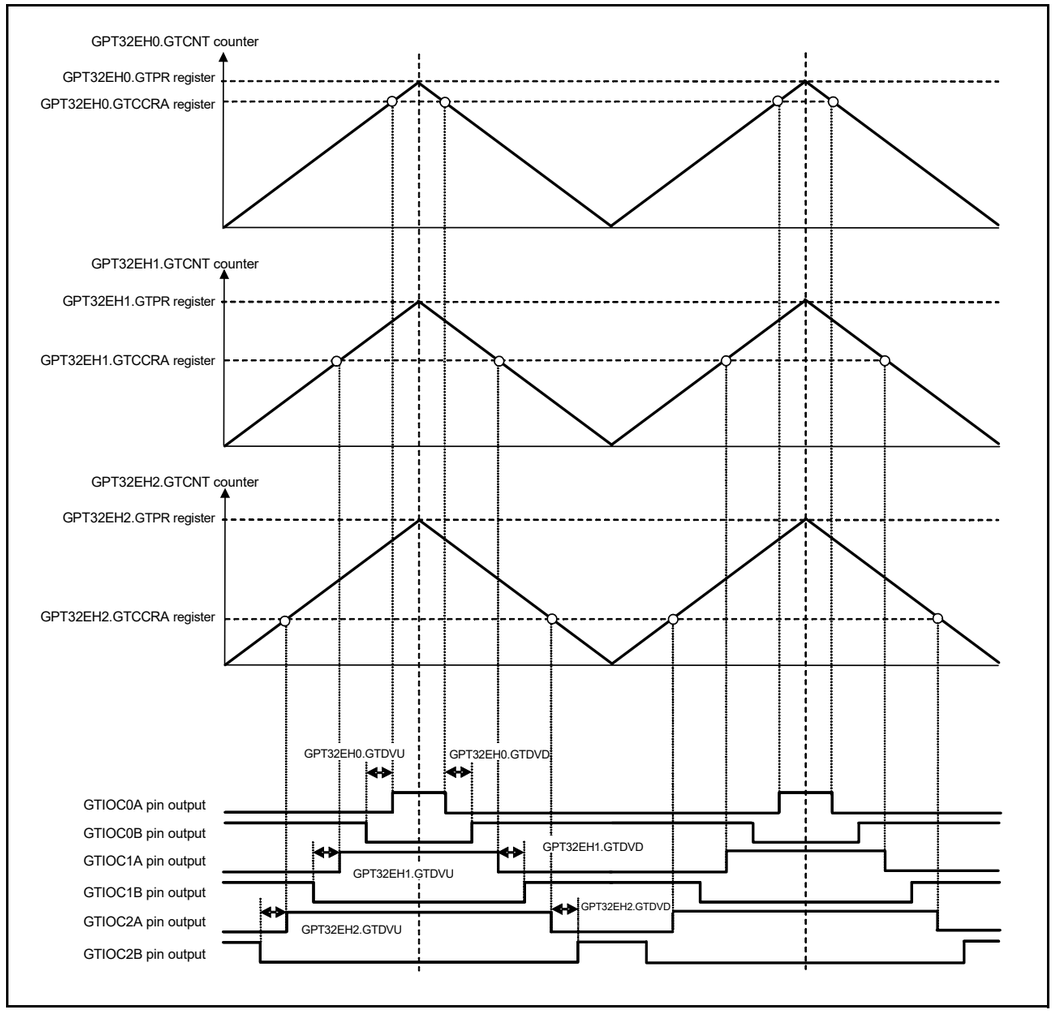


Figure 23.69 Example of 3-phase triangle-wave complementary PWM output with automatic dead time setting

(6) 3-phase asymmetric triangle-wave complementary PWM output with automatic dead time setting

Figure 23.70 shows an example in which three channels perform synchronized operation in triangle-wave PWM mode 3 with automatic dead time setting and 3-phase complementary PWM waveforms are output. The GTIOCA is set so that it outputs low as the initial value, toggles the output at a GTCCRA compare match, and retains the output at the cycle end. The GTIOCB is set so that it outputs high as the initial value, toggles the output at a GTCCRB compare match, and retains the output at the cycle end.

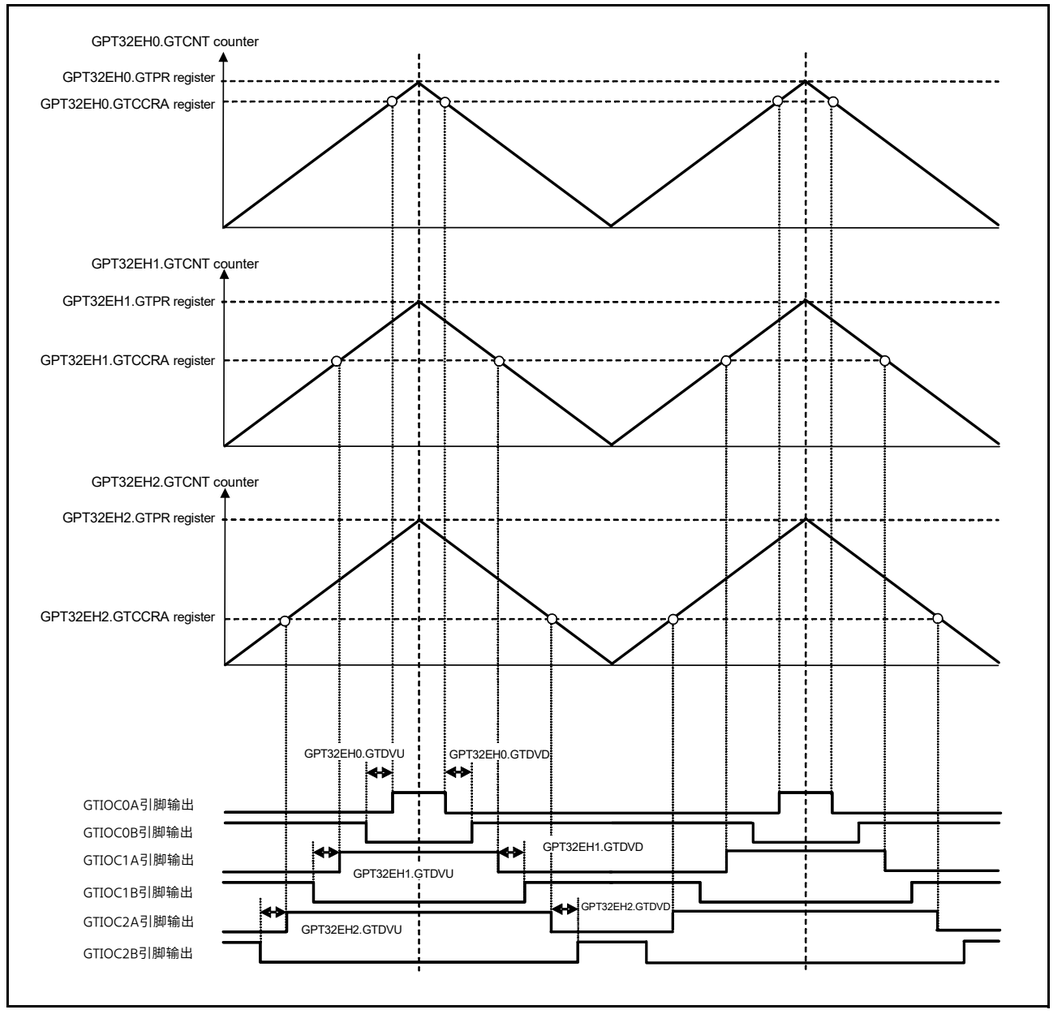


Figure 23.69 具有自动死区时间设置的三相三角波互补PWM输出示例

(6) 具有自动死区时间设置的三相不对称三角波互补PWM输出

图23.70显示了一个示例，其中三个通道在三角波PWM模式3下执行同步操作，自动设置死区时间并输出三相互补PWM波形。GTIOCA设置为输出低作为初始值，在GTCCRA比较匹配时切换输出，并在循环结束时保留输出。GTIOCB设置为输出高电平作为初始值，在GTCCRB比较匹配时切换输出，并在循环结束时保留输出。

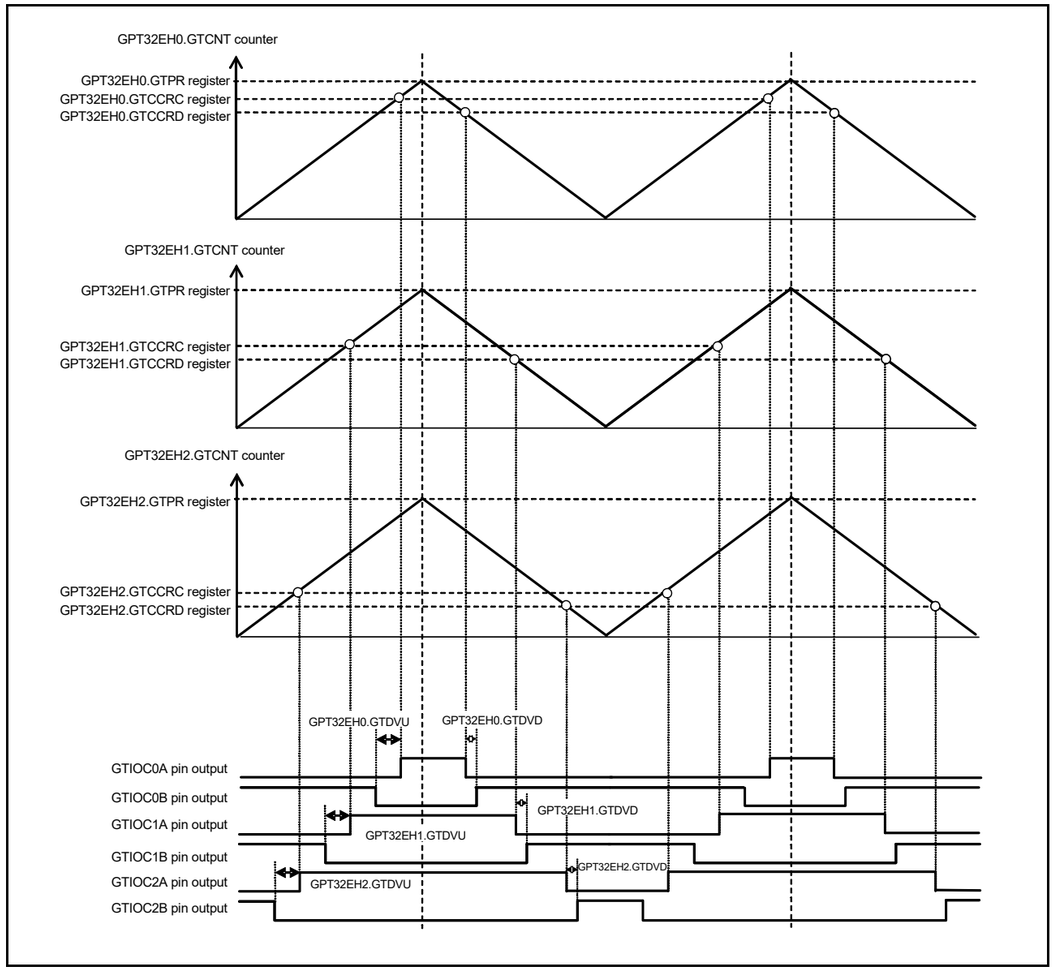


Figure 23.70 Example of 3-phase asymmetric triangle-wave complementary PWM output with automatic dead time setting

23.3.10 Phase Counting Function

The phase difference between the GTIOCA and GTIOCB pin inputs is detected and the associated GTCNT counts up or counts down. The detectable phase difference is available in any combination with the relationship between the edge and the level of GTIOCA and GTIOCB pin inputs being set in the GTUPSR and GTDNSR registers. For details on count operation, see section 23.3.1.1, Counter operation.

Figure 23.71 to Figure 23.80 show phase counting modes 1 to 5. Table 23.8 to Table 23.17 show conditions of up-counting or down-counting and lists settings for the GTUPSR and GTDNSR registers.

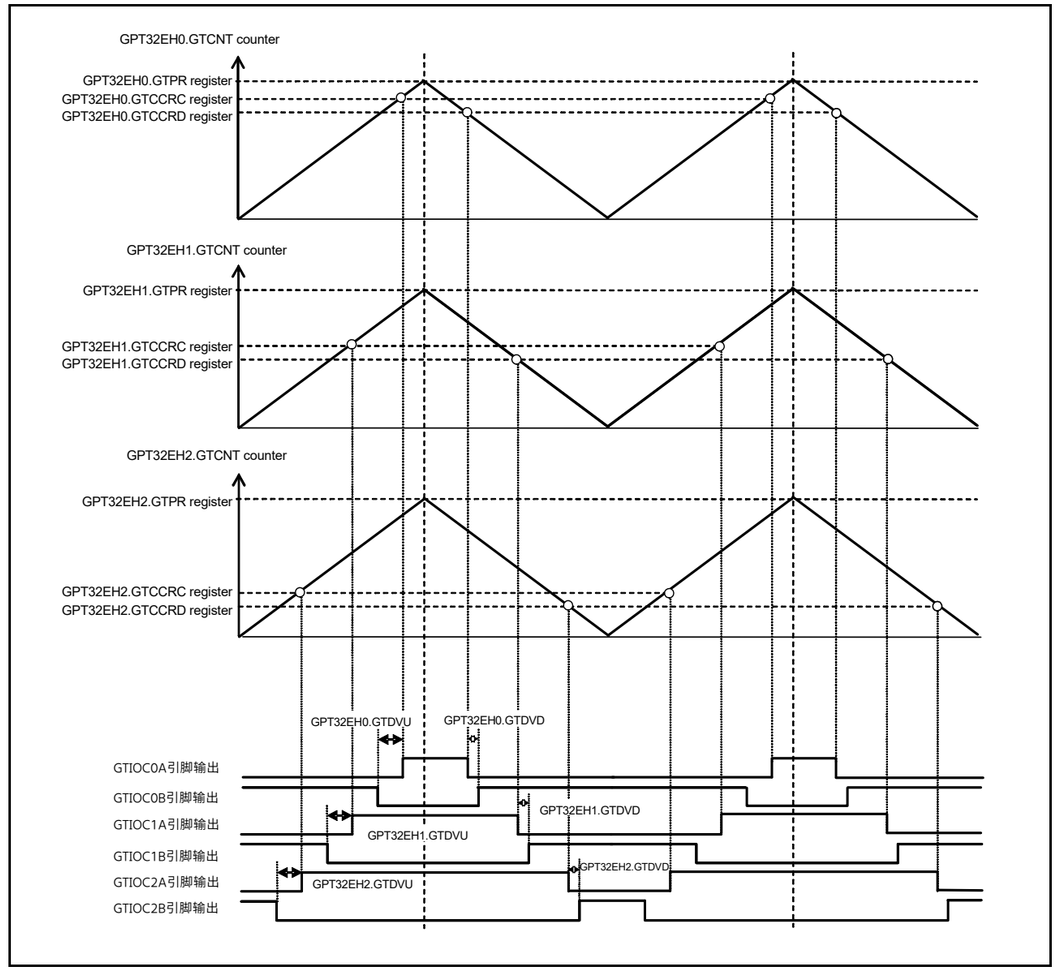


Figure 23.70 具有自动死区时间设置的三相不对称三角波互补PWM输出示例

23.3.10 相位计数功能

检测到GTIOCA和GTIOCB引脚输入之间的相位差，并且相关的GTCNT向上计数或向下计数。可检测的相位差可与在GTUPSR和GTDNSR寄存器中设置的GTIOCA和GTIOCB引脚输入的边沿和电平之间的关系任意组合。有关计数操作的详细信息，请参阅第23.3.1.1节，计数器操作。

图23.71至图23.80显示了相位计数模式1至5。表23.8至表23.17显示了向上计数或向下计数的条件，并列出了GTUPSR和GTDNSR寄存器的设置。

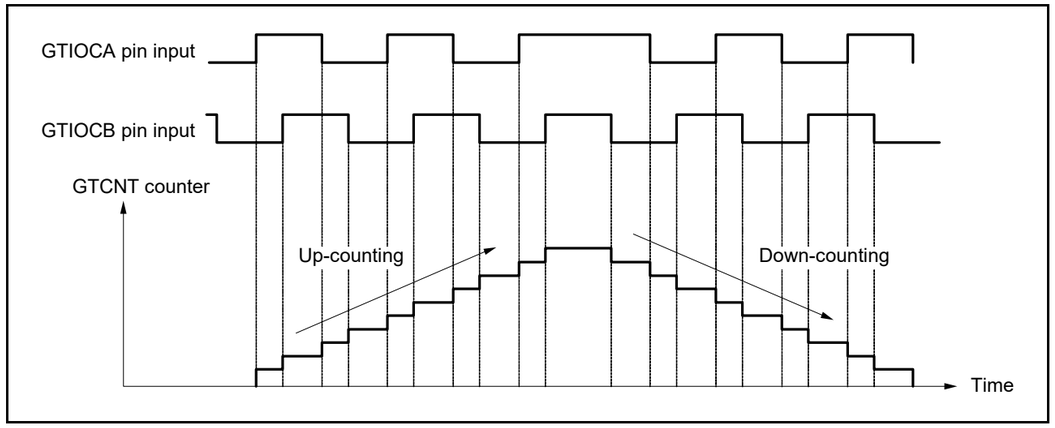


Figure 23.71 Example of phase counting mode 1

Table 23.8 Conditions of up-counting and down-counting in phase counting mode 1

GTIOCA pin input	GTIOCB pin input	Operation	Register setting
high	↑	Up-counting	GTUPSR = 0000 6900h GTDNSR = 0000 9600h
low	↓		
↑	low		
↓	high		
high	↓	Down-counting	
low	↑		
↑	high		
↓	low		

↑ : Rising edge

↓ : Falling edge

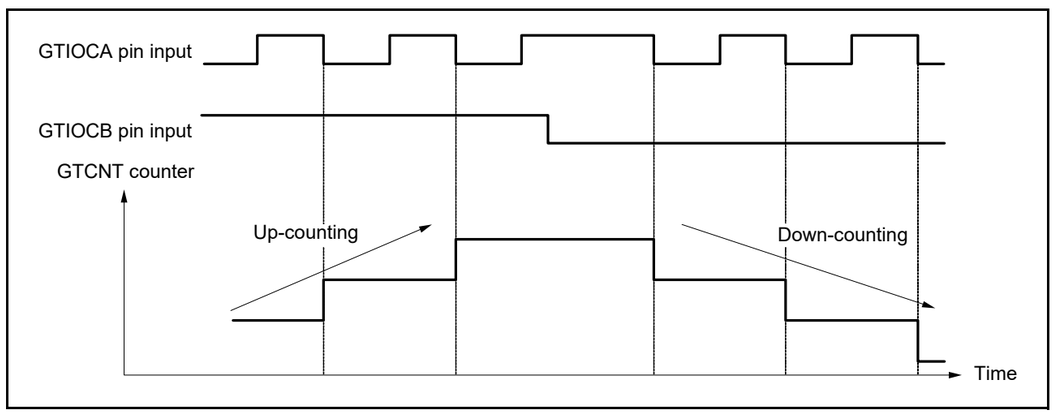


Figure 23.72 Example of phase counting mode 2 (A)

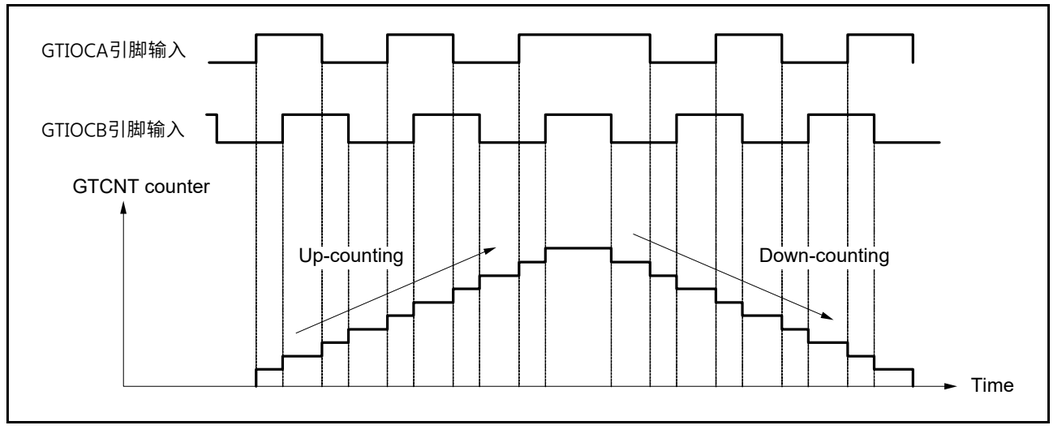


Figure 23.71 相位计数模式示例1

Table 23.8 相位计数方式的加减计数条件1

GTIOCA引脚输入	GTIOCB引脚输入	Operation	注册设置
high	↑	Up-counting	GTUPSR = 0000 6900h GTDNSR = 0000 9600h
low	↓		
↑	low		
↓	high		
high	↓	Down-counting	
low	↑		
↑	high		
↓	low		

↑ :上升沿

↓ :下降沿

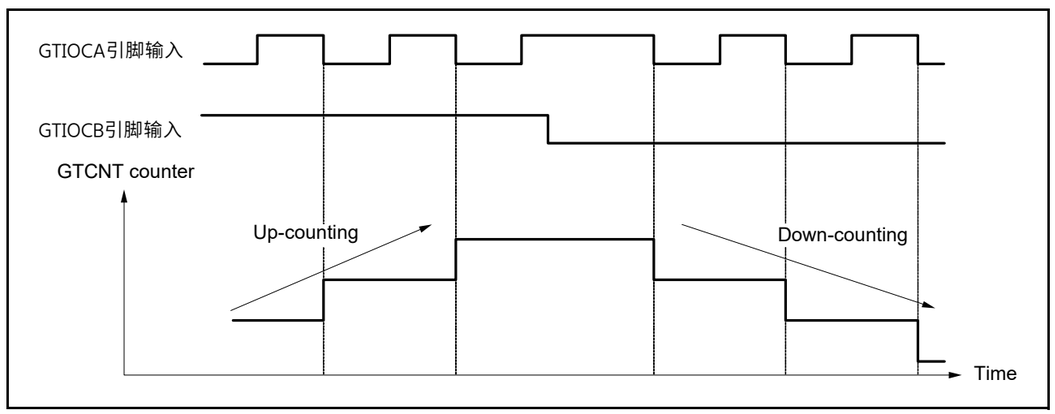


Figure 23.72 相位计数模式示例2(A)

Table 23.9 Conditions of up-counting and down-counting in phase counting mode 2 (A)

GTIOCA pin input	GTIOCB pin input	Operation	Register setting
high	↑	Don't care	GTUPSR = 0000 0800h GTDNSR = 0000 0400h
low	↓		
↑	low		
↓	high	Up-counting	
high	↓	Don't care	
low	↑		
↑	high		
↓	low	Down-counting	

↑ : Rising edge

↓ : Falling edge

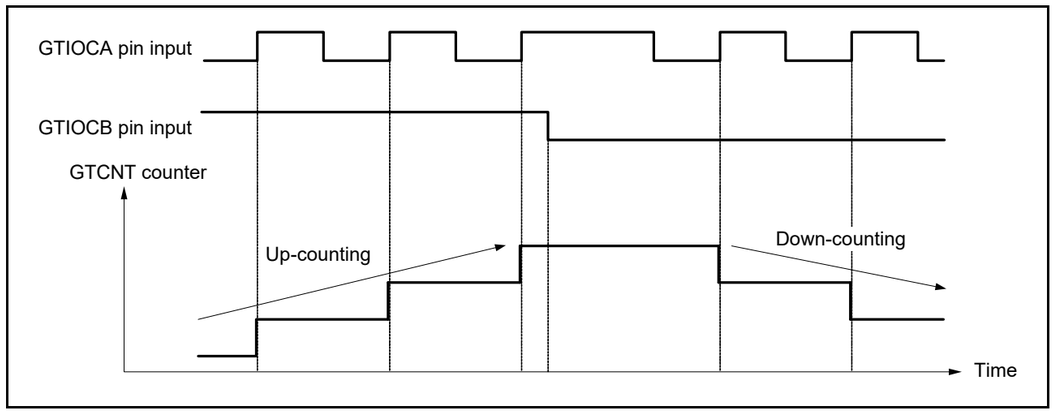


Figure 23.73 Example of phase counting mode 2 (B)

Table 23.10 Conditions of up-counting and down-counting in phase counting mode 2 (B)

GTIOCA pin input	GTIOCB pin input	Operation	Register setting
high	↑	Don't care	GTUPSR = 0000 0200h GTDNSR = 0000 0100h
low	↓		
↑	low	Down-counting	
↓	high	Don't care	
high	↓		
low	↑		
↑	high	Up-counting	
↓	low	Don't care	

↑ : Rising edge

↓ : Falling edge

Table 23.9 相位计数模式2(A)的加减计数条件

GTIOCA引脚输入	GTIOCB引脚输入	Operation	注册设置
high	↑	Don't care	GTUPSR = 0000 0800h GTDNSR = 0000 0400h
low	↓		
↑	low		
↓	high	Up-counting	
high	↓	Don't care	
low	↑		
↑	high		
↓	low	Down-counting	

↑ :上升沿

↓ :下降沿

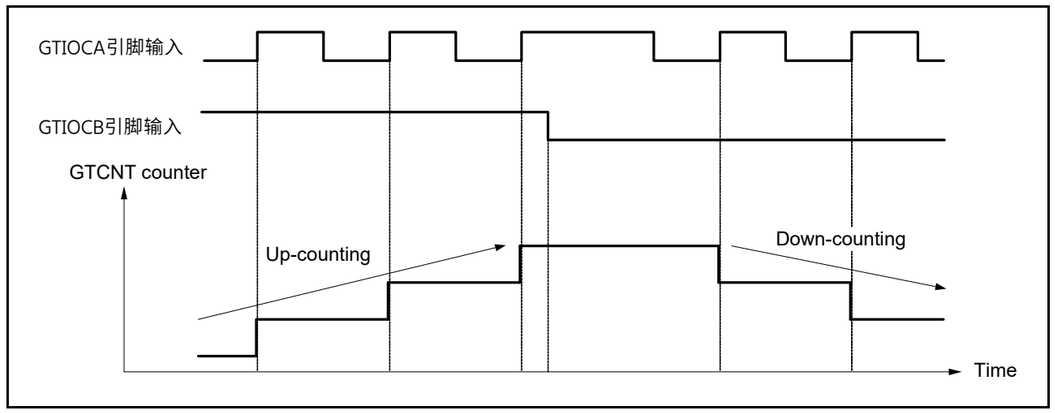


Figure 23.73 相位计数模式示例2(B)

Table 23.10 相位计数模式2(B)的加减计数条件

GTIOCA引脚输入	GTIOCB引脚输入	Operation	注册设置
high	↑	Don't care	GTUPSR = 0000 0200h GTDNSR = 0000 0100h
low	↓		
↑	low	Down-counting	
↓	high	Don't care	
high	↓		
low	↑		
↑	high	Up-counting	
↓	low	Don't care	

↑ :上升沿

↓ :下降沿

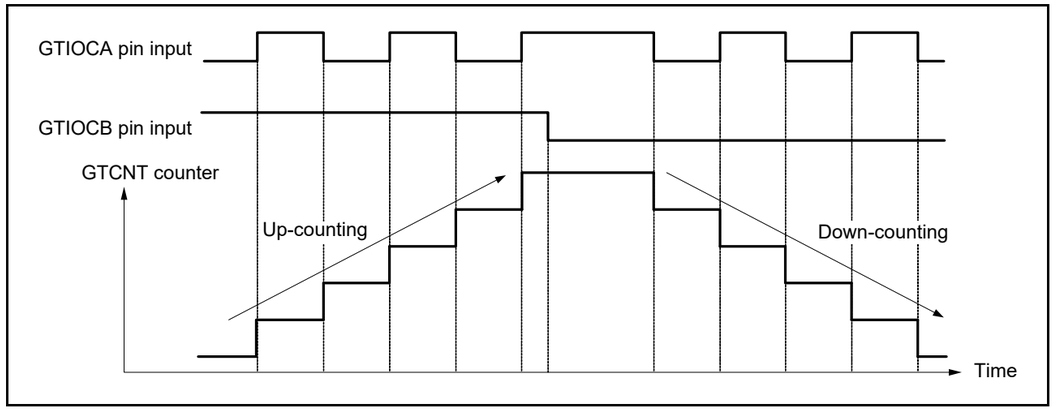


Figure 23.74 Example of phase counting mode 2 (C)

Table 23.11 Conditions of up-counting and down-counting in phase counting mode 2 (C)

GTIOCA pin input	GTIOCB pin input	Operation	Register setting
high	↑	Don't care	GTUPSR = 0000 0A00h GTDNSR = 0000 0500h
low	↓		
↑	low	Down-counting	
↓	high	Don't care	
low	↑		
↑	high	Up-counting	
↓	low	Down-counting	

↑ : Rising edge

↓ : Falling edge

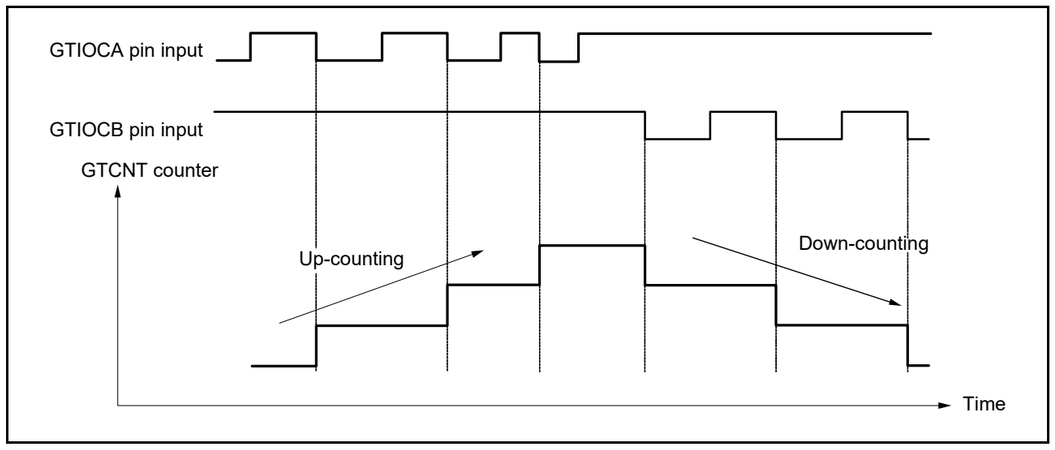


Figure 23.75 Example of phase counting mode 3 (A)

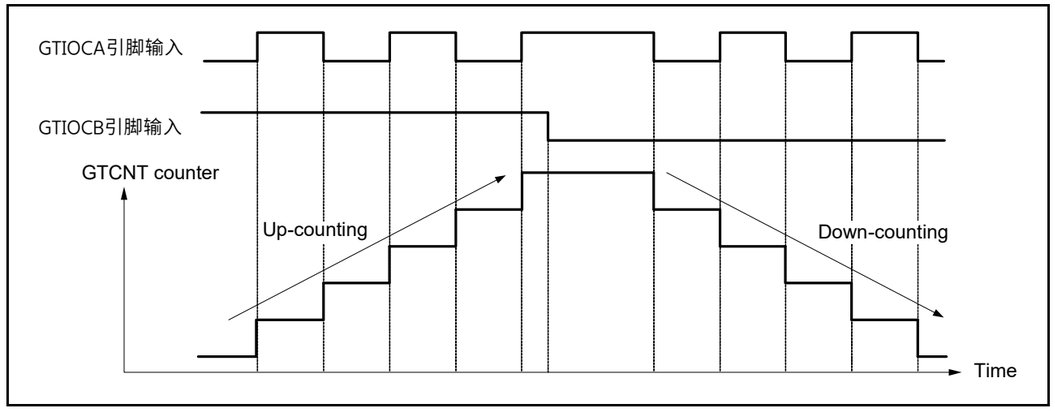


Figure 23.74 相位计数模式示例2(C)

Table 23.11 相位计数模式2（C）的加减计数条件

GTIOCA引脚输入	GTIOCB引脚输入	Operation	注册设置
high	↑	Don't care	GTUPSR = 0000 0A00h GTDNSR = 0000 0500h
low	↓		
↑	low	Down-counting	
↓	high	Don't care	
low	↑		
↑	high	Up-counting	
↓	low	Down-counting	

↑ :上升沿

↓ :下降沿

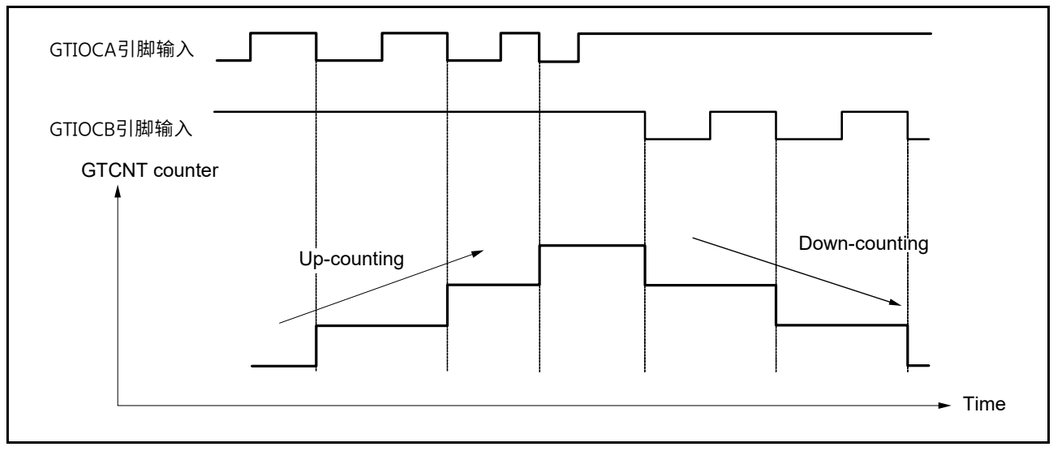


Figure 23.75 相位计数模式示例3(A)

Table 23.12 Conditions of up-counting and down-counting in phase counting mode 3 (A)

GTIOCA pin input	GTIOCB pin input	Operation	Register setting
high	↑	Don't care	GTUPSR = 0000 0800h GTDNSR = 0000 8000h
low	↓		
↑	low		
↓	high	Up-counting	
high	↓	Down-counting	
low	↑	Don't care	
↑	high		
↓	low		

↑ : Rising edge

↓ : Falling edge

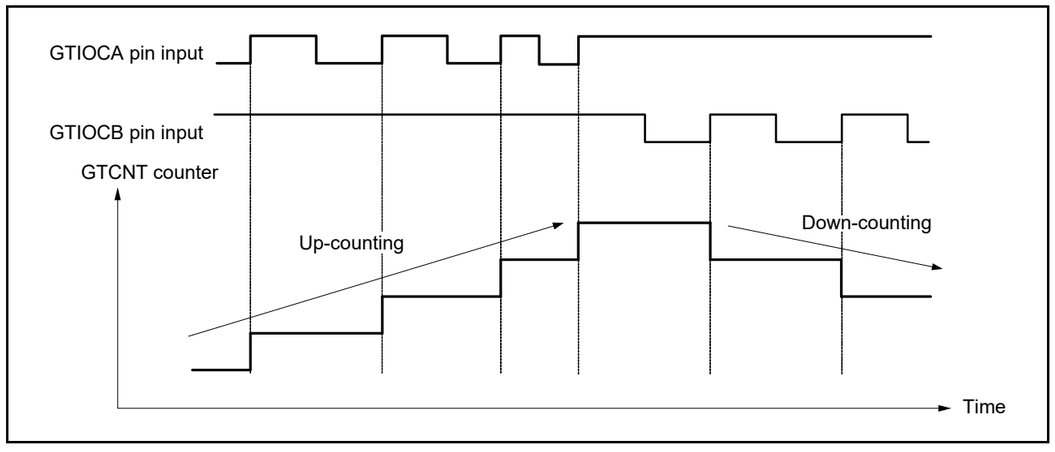


Figure 23.76 Example of phase counting mode 3 (B)

Table 23.13 Conditions of up-counting and down-counting in phase counting mode 3 (B)

GTIOCA pin input	GTIOCB pin input	Operation	Register setting
high	↑	Down-counting	GTUPSR = 0000 0200h GTDNSR = 0000 2000h
low	↓	Don't care	
↑	low		
↓	high		
high	↓		
low	↑		
↑	high	Up-counting	
↓	low	Don't care	

↑ : Rising edge

↓ : Falling edge

Table 23.12 相位计数模式3(A)加减计数条件

GTIOCA引脚输入	GTIOCB引脚输入	Operation	注册设置
high	↑	Don't care	GTUPSR = 0000 0800h GTDNSR = 0000 8000h
low	↓		
↑	low		
↓	high	Up-counting	
high	↓	Down-counting	
low	↑	Don't care	
↑	high		
↓	low		

↑ :上升沿

↓ :下降沿

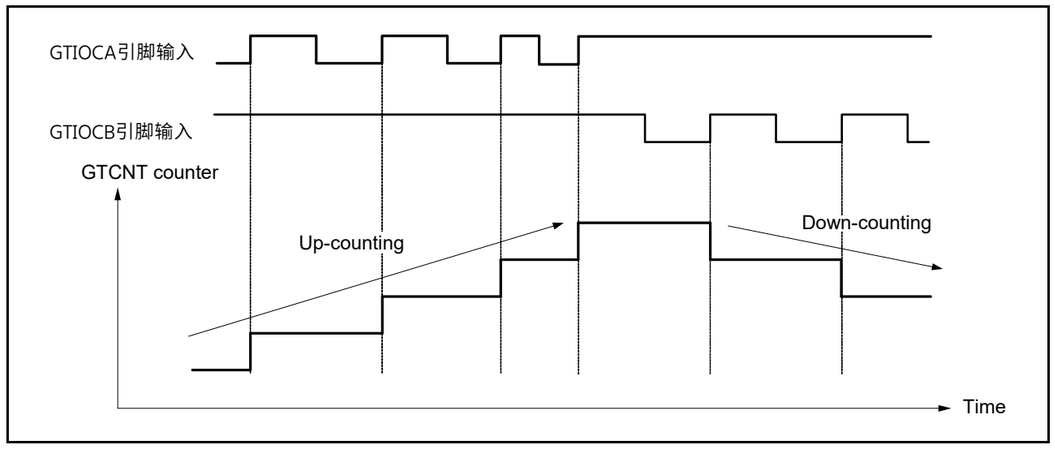


Figure 23.76 相位计数模式示例3(B)

Table 23.13 相位计数模式3(B)的加减计数条件

GTIOCA引脚输入	GTIOCB引脚输入	Operation	注册设置
high	↑	Down-counting	GTUPSR = 0000 0200h GTDNSR = 0000 2000h
low	↓	Don't care	
↑	low		
↓	high		
high	↓		
low	↑		
↑	high	Up-counting	
↓	low	Don't care	

↑ :上升沿

↓ :下降沿

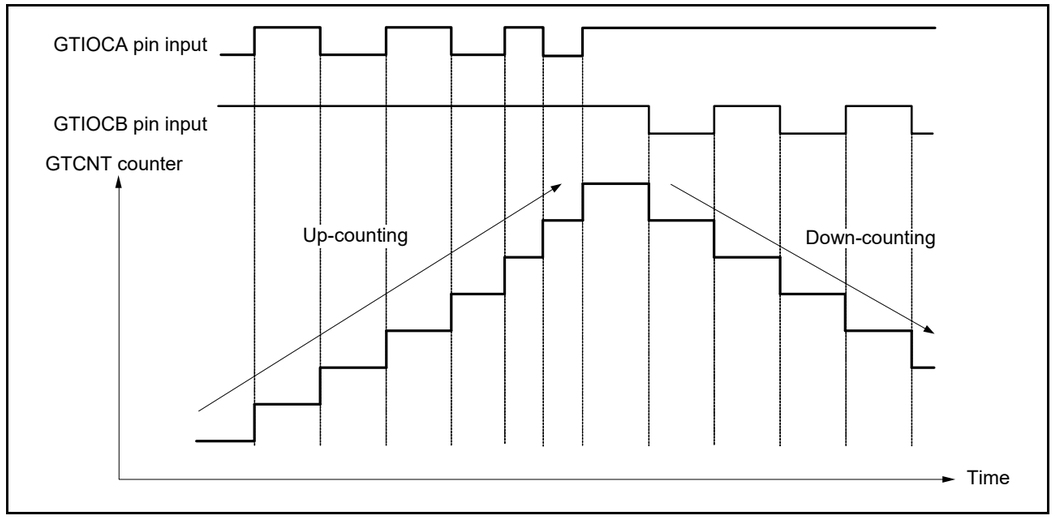


Figure 23.77 Example of phase counting mode 3 (C)

Table 23.14 Conditions of up-counting and down-counting in phase counting mode 3 (C)

GTIOCA pin input	GTIOCB pin input	Operation	Register setting
high	↑	Down-counting	GTUPSR = 0000 0A00h GTDNSR = 0000 A000h
low	↓	Don't care	
↑	low		
↓	high	Up-counting	
high	↓	Down-counting	
low	↑	Don't care	
↑	high	Up-counting	
↓	low	Don't care	

↑ : Rising edge

↓ : Falling edge

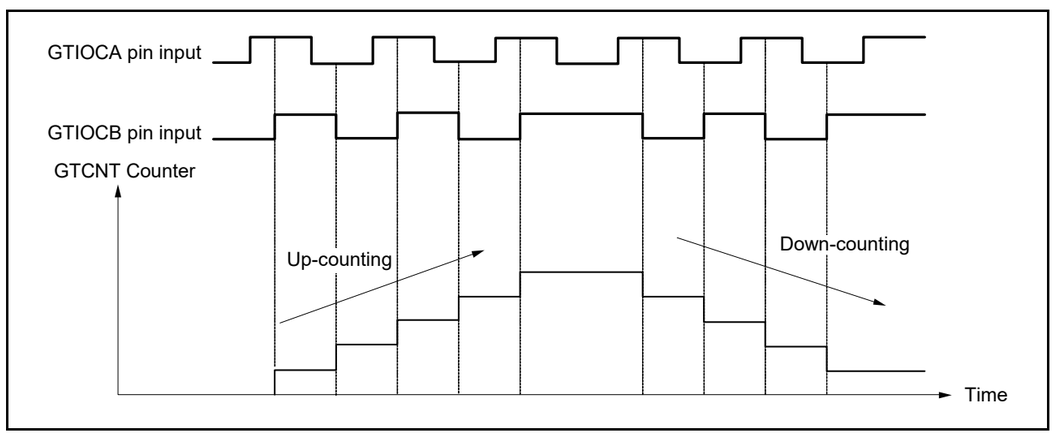


Figure 23.78 Example of phase counting mode 4

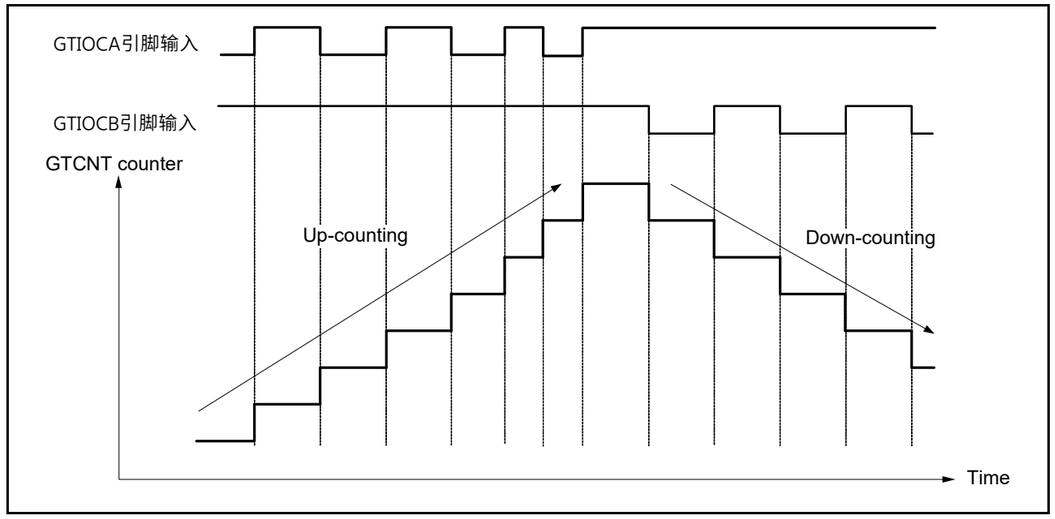


Figure 23.77 相位计数模式示例3(C)

Table 23.14 相位计数模式3(C)的加减计数条件

GTIOCA引脚输入	GTIOCB引脚输入	Operation	注册设置
high	↑	Down-counting	GTUPSR = 0000 0A00h GTDNSR = 0000 A000h
low	↓	Don't care	
↑	low		
↓	high	Up-counting	
high	↓	Down-counting	
low	↑	Don't care	
↑	high	Up-counting	
↓	low	Don't care	

↑ :上升沿

↓ :下降沿

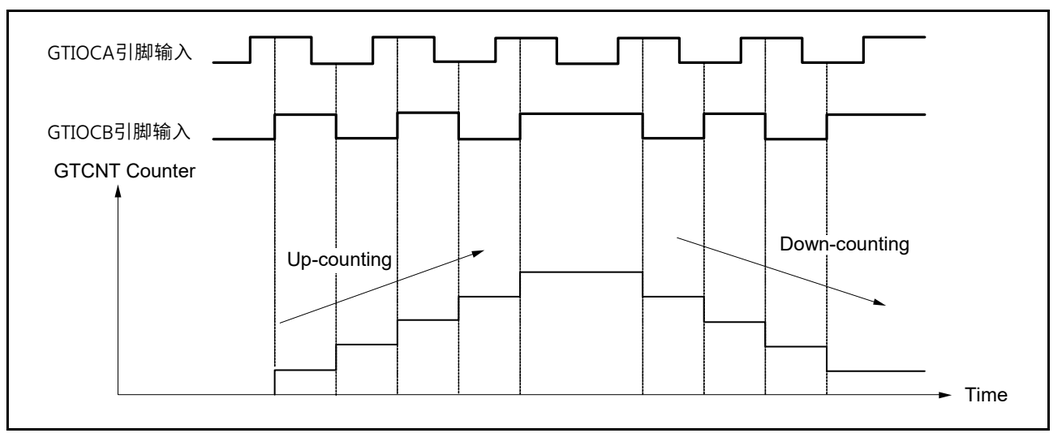


Figure 23.78 相位计数模式示例4

Table 23.15 Conditions of up-counting and down-counting in phase counting mode 4

GTIOCA pin input	GTIOCB pin input	Operation	Register setting
high	↑	Up-counting	GTUPSR = 0000 6000h GTDNSR = 0000 9000h
low	↓		
↑	low	Don't care	
↓	high		
high	↓	Down-counting	
low	↑		
↑	high	Don't care	
↓	low		

↑ : Rising edge

↓ : Falling edge

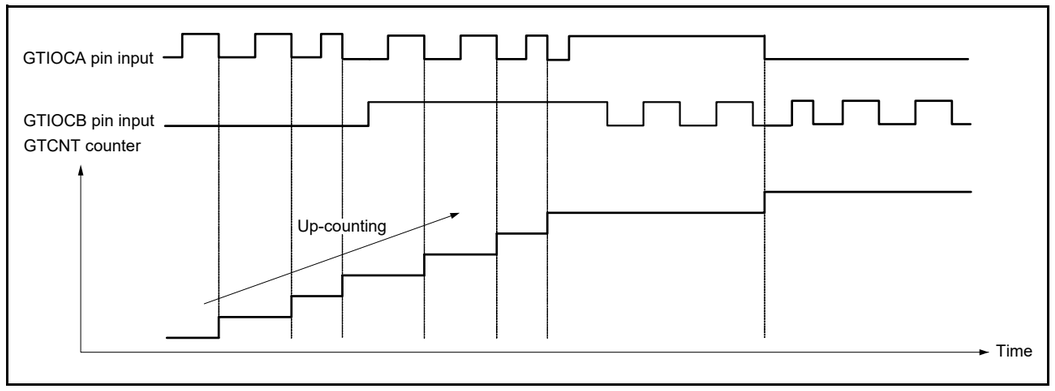


Figure 23.79 Example of phase counting mode 5 (A)

Table 23.16 Conditions of up-counting and down-counting in phase counting mode 5 (A)

GTIOCA pin input	GTIOCB pin input	Operation	Register setting
high	↑	Don't care	GTUPSR = 0000 0C00h GTDNSR = 0000 0000h
low	↓		
↑	low		
↓	high	Up-counting	
high	↓	Don't care	
low	↑		
↑	high		
↓	low	Up-counting	

↑ : Rising edge

↓ : Falling edge

Table 23.15 相位计数方式4加减计数条件

GTIOCA引脚输入	GTIOCB引脚输入	Operation	注册设置
high	↑	Up-counting	GTUPSR = 0000 6000h GTDNSR = 0000 9000h
low	↓		
↑	low	Don't care	
↓	high		
high	↓	Down-counting	
low	↑		
↑	high	Don't care	
↓	low		

↑ :上升沿

↓ :下降沿

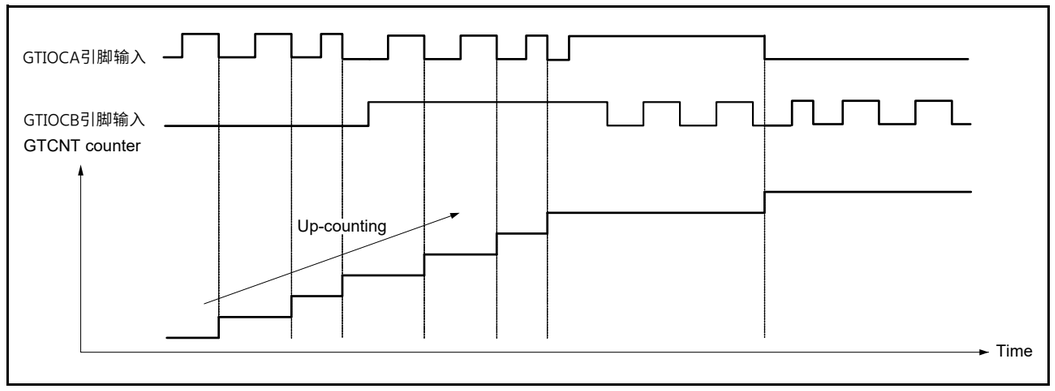


Figure 23.79 相位计数模式示例5(A)

Table 23.16 相位计数模式5(A)加减计数条件

GTIOCA引脚输入	GTIOCB引脚输入	Operation	注册设置
high	↑	Don't care	GTUPSR = 0000 0C00h GTDNSR = 0000 0000h
low	↓		
↑	low		
↓	high	Up-counting	
high	↓	Don't care	
low	↑		
↑	high		
↓	low	Up-counting	

↑ :上升沿

↓ :下降沿

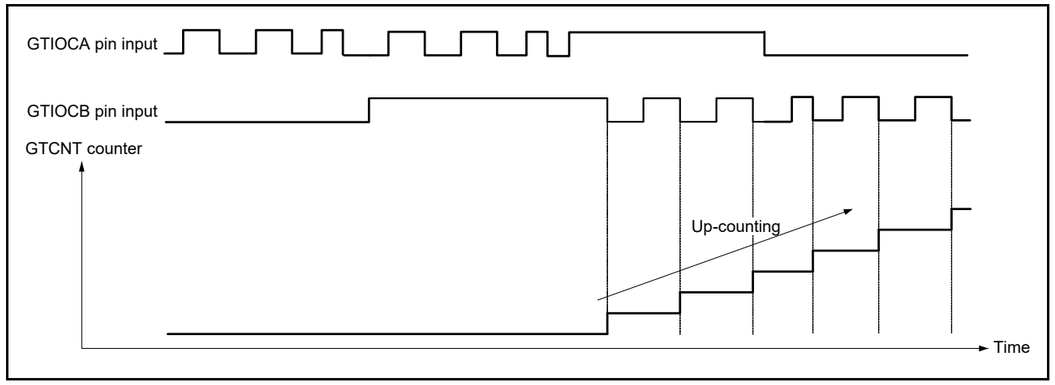


Figure 23.80 Example of phase counting mode 5 (B)

Table 23.17 Conditions of up-counting and down-counting in phase counting mode 5 (B)

GTIOCA pin input	GTIOCB pin input	Operation	Register setting
high	↑	Don't care	GTUPSR = 0000 0C00h GTDNSR = 0000 0000h
low	↓	Up-counting	
↑	low	Don't care	
↓	high		
high	↓	Up-counting	
low	↑	Don't care	
↑	high		
↓	low		

↑ : Rising edge

↓ : Falling edge

23.3.11 Output Phase Switching (GPT_OPS)

GPT_OPS provides a function for easy control of brushless DC motor operation using the Output Phase Switching Control Register (OPSCR).

GPT_OPS outputs a PWM signal to be used for chopper control or level signal for each phase (U-positive phase/negative phase, V-positive phase/negative phase, W-positive phase/negative phase) of the 6-phase motor control. This function uses a soft setting value (OPSCR.UF, VF, WF) set by software or external signals detected by the Hall element, a PWM waveform of GPT32EH0.GTIOCA.

Figure 23.81 shows the GPT_OPS control flow conceptual diagram.

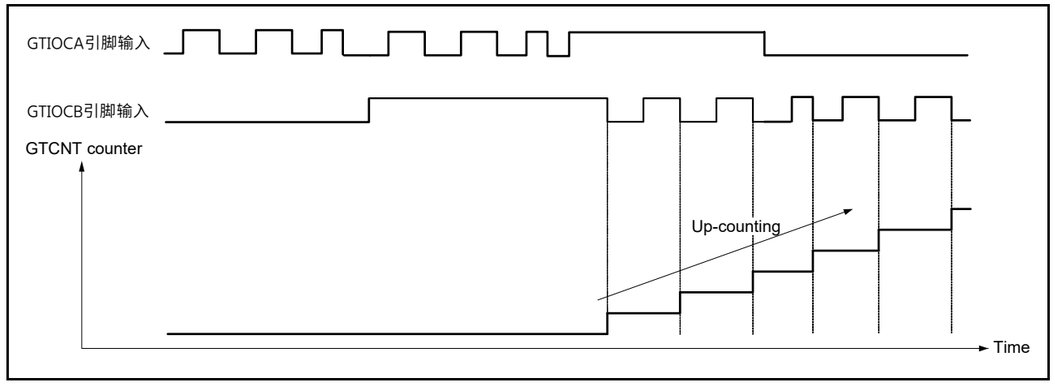


Figure 23.80 相位计数模式示例5(B)

Table 23.17 相位计数模式5(B)的加减计数条件

GTIOCA引脚输入	GTIOCB引脚输入	Operation	注册设置
high	↑	Don't care	GTUPSR = 0000 0C00h GTDNSR = 0000 0000h
low	↓	Up-counting	
↑	low	Don't care	
↓	high		
high	↓	Up-counting	
low	↑	Don't care	
↑	high		
↓	low		

↑ :上升沿

↓ :下降沿

23.3.11 输出相位切换(GPT_OPS)

GPT_OPS提供使用输出相位切换轻松控制无刷直流电机运行的功能
控制寄存器(OPSCR)。

GPT_OPS输出用于斩波控制的PWM信号或6相电机控制的每一相（U正相负相、V正相负相、W正相负相）的电平信号。该功能使用软件设置的软设置值（OPSCR.UF、VF、WF）或霍尔元件检测到的外部信号，GPT32EH0.GTIOCA的PWM波形。

图23.81显示了GPT_OPS控制流概念图。

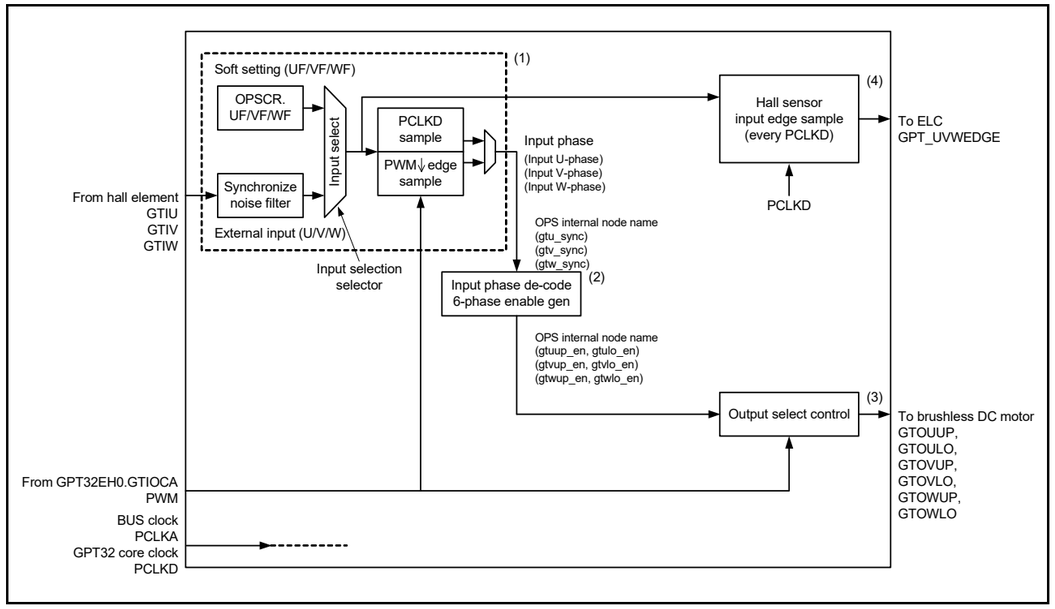


Figure 23.81 Conceptual diagram of GPT_OPS control flow

Figure 23.82 shows a 6-phase level signals output example of a GPT_OPS operation.

The GPT_UVWEDGE signal in Figure 23.82 is the Hall sensor input edge to ELC output.

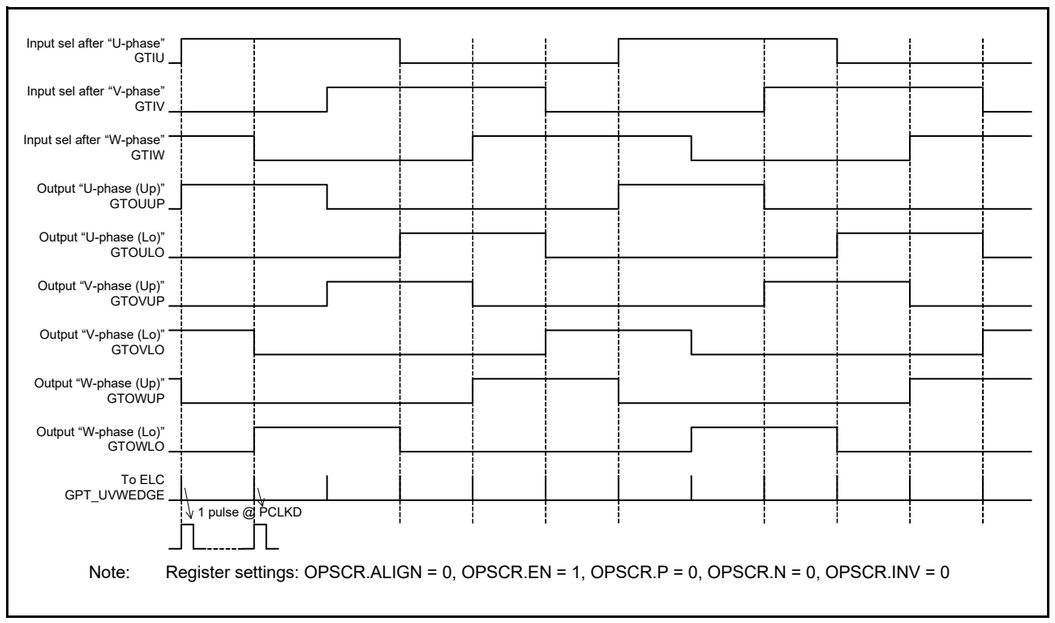


Figure 23.82 Example of 6-phase level output operation

Figure 23.83 shows a 6-phase PWM output example of a GPT_OPS operation (chopper control).

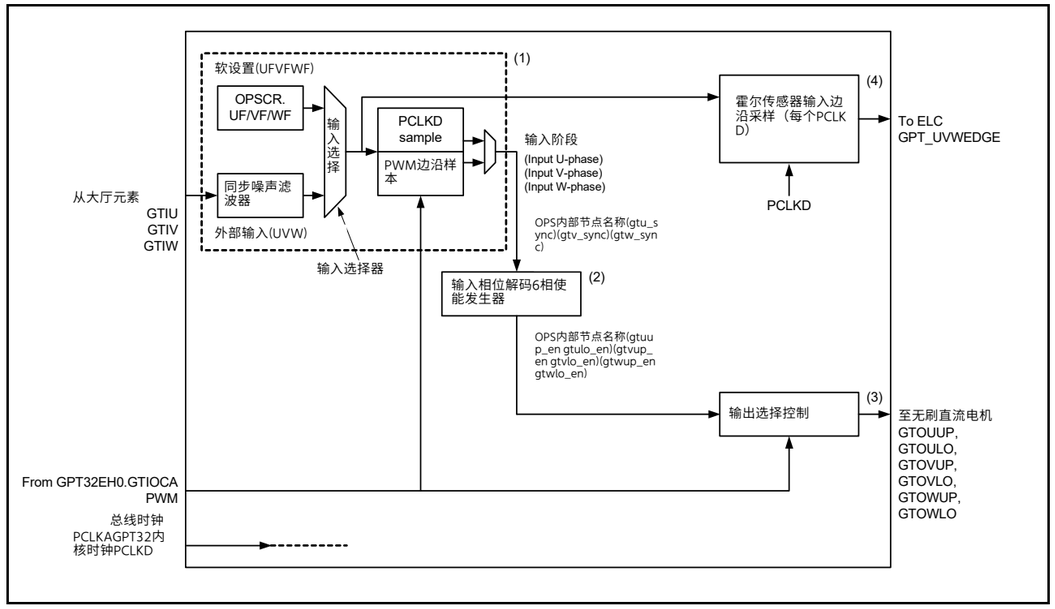


Figure 23.81 GPT_OPS控制流程概念图

图23.82显示了GPT_OPS操作的6相电平信号输出示例。

图23.82中的GPT_UVWEDGE信号是霍尔传感器输入边沿到ELC输出。

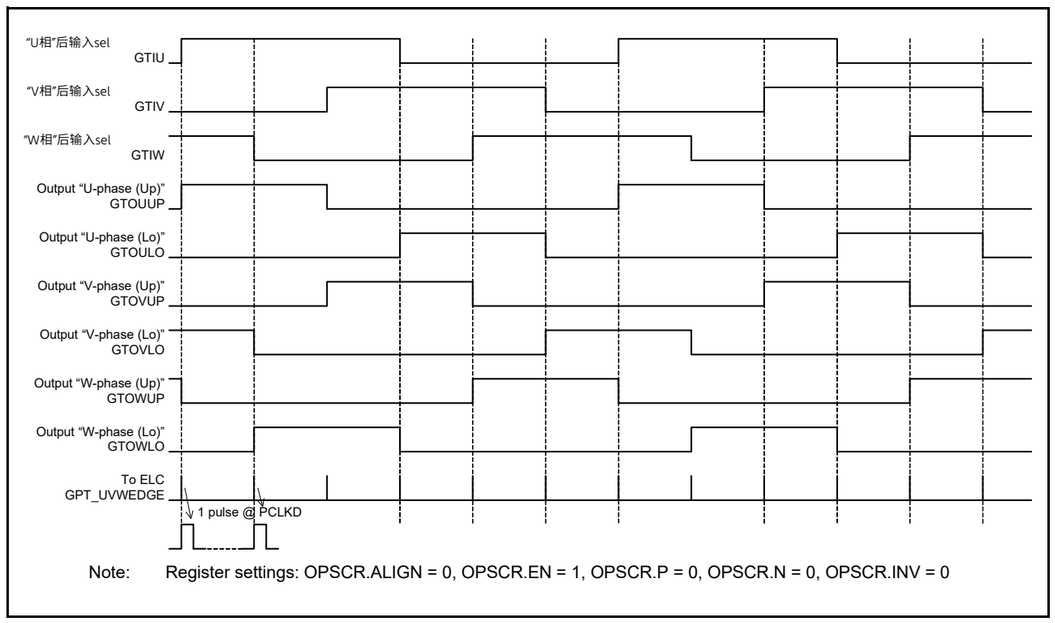
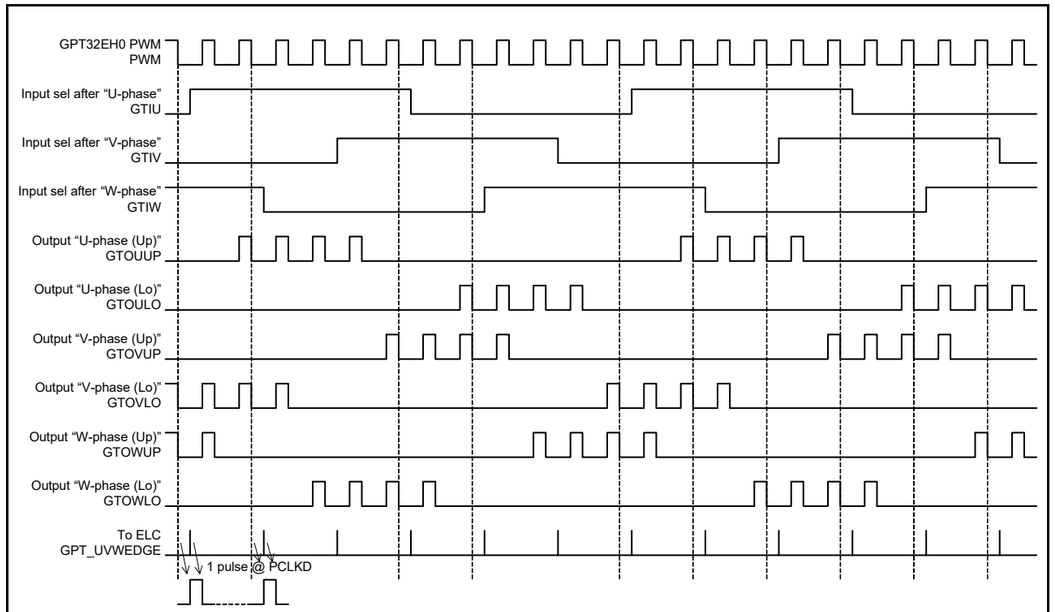


Figure 23.82 6相电平输出动作示例

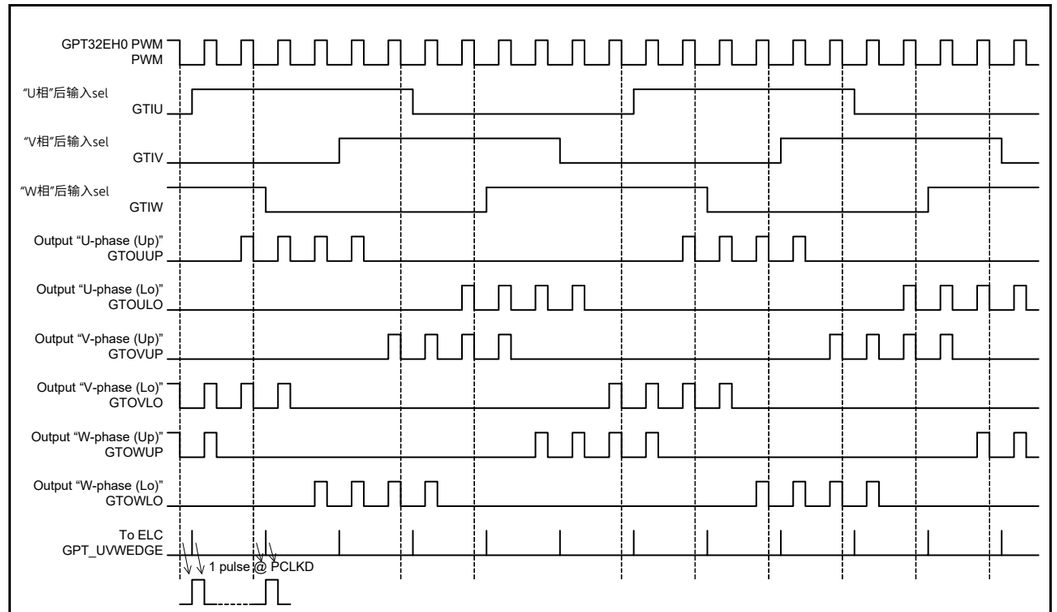
图23.83显示了GPT_OPS操作（斩波器控制）的6相PWM输出示例。



Note: Register settings: OPSCR.ALIGN = 1, OPSCR.EN = 1, OPSCR.P = 1, OPSCR.N = 1, OPSCR.INV = 0

Figure 23.83 Example of 6-phase PWM output operation with chopper control

Figure 23.84 shows an example of output disable control (6-phase PWM output operation).



Note: Register settings: OPSCR.ALIGN = 1, OPSCR.EN = 1, OPSCR.P = 1, OPSCR.N = 1, OPSCR.INV = 0

Figure 23.83 带斩波器控制的6相PWM输出操作示例

图23.84显示了输出禁用控制的示例（6相PWM输出操作）。

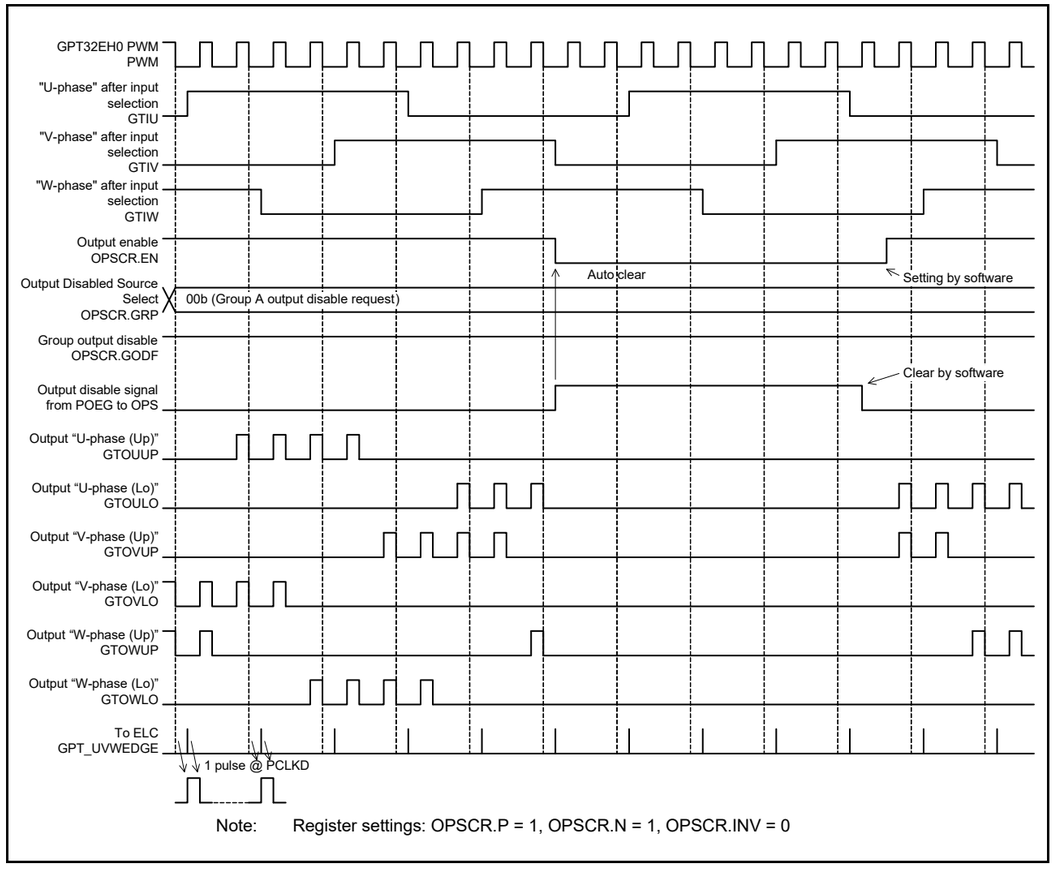


Figure 23.84 Example of group output disable control operation

23.3.11.1 Input selection and synchronization of external input signal

In the GPT_OPS control flow conceptual diagram shown in Figure 23.81, (1) is a selection of input phase from software settings and external input by the OPSCR.FB bit.

When OPSCR.FB bit = 0, select the external input. Enable the input signal after synchronization with the GPT core clock (PCLKD). After carrying out noise filtering (optional), set the external input to the input phase of PWM (PWM of GPT32EH0.GTIOCA) using falling edge sampling with OPSCR.ALIGN bit = 1.

When OPSCR.FB bit = 1, select the soft setting (OPSCR.UF, VF, WF) with the value of the input phase of PWM (PWM of GPT32EH0.GTIOCA) using falling edge sampling with OPSCR.ALIGN bit = 1.

When OPSCR.ALIGN bit = 0, GPT_OPS operates with the input phase of PCLKD synchronization with either OPSCR.FB bit = 0 or OPSCR.FB bit = 1. However, in some situations, the PWM pulse width of the output U/V/W phases (PWM output mode) of switch timing (just before or just after) is shortened.

Table 23.18 shows the input selection process and setting of associated OPSCR bits.

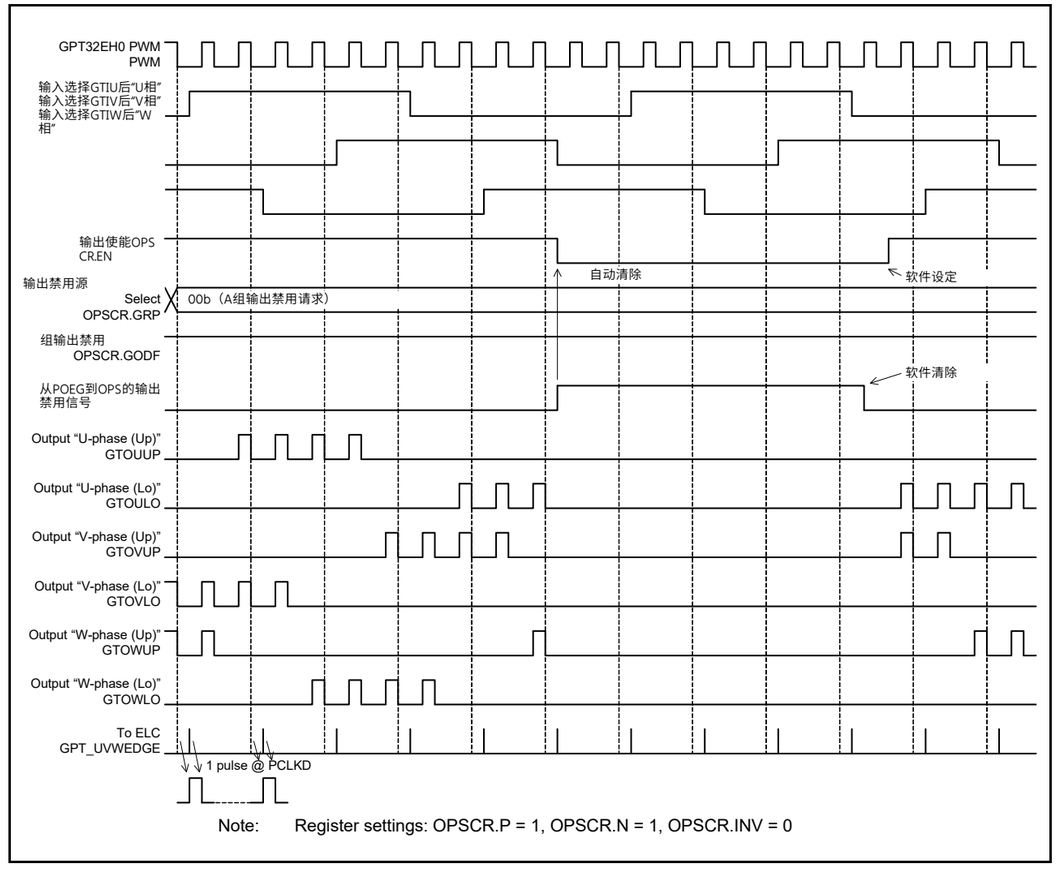


Figure 23.84 组输出禁用控制操作示例

23.3.11.1 外部输入信号的输入选择和同步

在图23.81所示的GPT_OPS控制流程概念图中，(1)是通过OPSCR.FB位从软件设置和外部输入中选择输入相位。

当OPSCR.FB位=0时，选择外部输入。与GPT内核时钟(PCLKD)同步后启用输入信号。执行噪声过滤（可选）后，使用OPSCR.ALIGN位=1的下降沿采样将外部输入设置为PWM的输入相位（GPT32EH0.GTIOCA的PWM）。

当OPSCR.FB位=1时，使用OPSCR.ALIGN位=1的下降沿采样，使用PWM（GPT32EH0.GTIOCA的PWM）的输入相位值选择软设置（OPSCR.UF、VF、WF）。

当OPSCR.ALIGN位=0时，GPT_OPS使用PCLKD同步的输入相位与任一OPSCR.FB位=0或OPSCR.FB位=1。但是，在某些情况下，开关时序（恰好之前或之后）的输出UVW相位（PWM输出模式）的PWM脉冲宽度会缩短。

表23.18显示了输入选择过程和相关OPSCR位的设置。

Table 23.18 Input selection processing method

OPSCR register		Selection of input phase sampling method (U/V/W-phase)	Synchronization input/output selection process (GPT_OPS internal node name)
FB bit	ALIGN bit		
0	1	External Input at PWM Falling Edge Sampling (PCLKD synchronization + falling edge sample)	“Input Phase” Input U-Phase (gtu_sync) Input V-Phase (gtv_sync) Input W-Phase (gtw_sync)
	0	External Input at PCLKD Synchronization Output (PCLKD synchronization + through mode)	
1	1	Software Settings at PWM Falling Edge Sampling (OPSCR.UF, VF, WF of falling edge sample)	
	0	Software Setting Value Selection (= OPSCR.UF/VF/WF value) (= PCLKD synchronization)	

23.3.11.2 Input sampling

The OPSCR.U, V, W bits indicate the PCLKD sampling results of the input selected by the OPSCR.FB bit.

When OPSCR.FB bit = 0 and after synchronization with the GPT core clock (PCLKD) and noise filtering (optional), OPSCR.U, V, W bits indicate the sampling results of the external input. When OPSCR.FB bit = 1, OPSCR.U, V, W bits have the value (OPSCR.UF, VF, WF) of the soft setting.

23.3.11.3 Input phase decode

In the GPT_OPS control flow conceptual diagram shown in Figure 23.81, (2) enables the 6-phase signals by decoding the input phase selected by the OPSCR.FB bit. The 6-phase enable signal is used for internal processing of GPT_OPS.

Table 23.19 shows the decode table of input phase.

Table 23.19 Decode table of input phase

Input phase (U/V/W) (GPT_OPS internal node name)			6-phase enable {U/V/W (Up/Lo)} by decoding input phase (GPT_OPS internal node name)					
Input U-phase	Input V-phase	Input W-phase	U-phase (Up)	U-phase (Lo)	V-phase (Up)	V-phase (Lo)	W-phase (Up)	W-phase (Lo)
(gtu_sync)	(gtv_sync)	(gtw_sync)	(gtuup_en)	(gtulo_en)	(gtvup_en)	(gtvlo_en)	(gtwup_en)	(gtwlo_en)
1	0	1	1	0	0	1	0	0
1	0	0	1	0	0	0	0	1
1	1	0	0	0	1	0	0	1
0	1	0	0	1	1	0	0	0
0	1	1	0	1	0	0	1	0
0	0	1	0	0	0	1	1	0
0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0

23.3.11.4 Output selection control

In the GPT_OPS control flow conceptual diagram in Figure 23.81, (3) represents the selection of the output waveform by setting the OPSCR register bit.

For output selection, the following bits are relevant:

- The OPSCR.EN bit controls whether to output the 6-phase output, or to stop
- The OPSCR.P and OPSCR.N bits can select from the level signal or PWM signal (chopper output) for the output phase
- The polarity of the output phase can be set to positive logic or negative logic by the OPSCR.INV bit.

Table 23.20 and Table 23.21 show the output selection control method using the OPSCR register bit.

Table 23.18 输入选择处理方法

OPSCR register		输入相位采样方式的选择（UVW−phase）	同步输入输出选择过程（GPT_OPS内部节点名）
FB bit	对齐位		
0	1	PWM下降沿采样的外部输入（PCLKD同步+下降沿采样）	“Input Phase” Input U-Phase (gtu_sync) Input V-Phase (gtv_sync) Input W-Phase (gtw_sync)
	0	PCLKD同步输出端的外部输入（PCLKD同步+直通模式）	
1	1	PWM下降沿采样的软件设置（下降沿采样的OPSCR.UF、VF、WF）	
	0	软件设置值选择（=OPSCR.UFVFWF值）（=PCLKD同步）	

23.3.11.2 输入采样

OPSCR.U、V、W位指示由OPSCR.FB位选择的输入的PCLKD采样结果。

当OPSCR.FB位=0并与GPT内核时钟(PCLKD)和噪声过滤（可选）同步后，
OPSCR.U、V、W位表示外部输入的采样结果。当OPSCR.FB位=1时，OPSCR.U、V、W位具有软设置的值（OPSCR.UF、VF、WF）。

23.3.11.3 输入相位解码

在图23.81所示的GPT_OPS控制流程概念图中，(2)通过解码OPSCR.FB位选择的输入相位来启用6相位信号。6相使能信号用于GPT_OPS的内部处理。

表23.19显示了输入相位的解码表。

Table 23.19 输入相位解码表

输入相位(UVW)（GPT_OPS内部节点名称）			6−phaseenable{UVW(UpLo) 通过解码输入相位（GPT_OPS内部节点名称）					
输入U相	输入V相	输入W相	U-phase (Up)	U-phase (Lo)	V-phase (Up)	V-phase (Lo)	W-phase (Up)	W-phase (Lo)
(gtu_sync)	(gtv_sync)	(gtw_sync)	(gtuup_en)	(gtulo_en)	(gtvup_en)	(gtvlo_en)	(gtwup_en)	(gtwlo_en)
1	0	1	1	0	0	1	0	0
1	0	0	1	0	0	0	0	1
1	1	0	0	0	1	0	0	1
0	1	0	0	1	1	0	0	0
0	1	1	0	1	0	0	1	0
0	0	1	0	0	0	1	1	0
0	0	0	0	0	0	0	0	0
1	1	1	0	0	0	0	0	0

23.3.11.4 输出选择控制

在图23.81的GPT_OPS控制流程概念图中，(3)表示通过设置OPSCR寄存器位来选择输出波形。

对于输出选择，以下位是相关的：

- OPSCR.EN位控制是输出6相输出，还是停止
- OPSCR.P和OPSCR.N位可以选择输出相位的电平信号或PWM信号（斩波器输出）
- 输出相位的极性可通过OPSCR.INV位设置为正逻辑或负逻辑。

表23.20和表23.21显示了使用OPSCR寄存器位的输出选择控制方法。

Table 23.20 Output selection control method (positive phase)

Enable-phase output control	Positive-phase output (P) control	Invert-phase output control	Output port name (positive phase = up) (output selection internal node allocation)	
OPSCR.EN bit	OPSCR.P bit	OPSCR.INV bit	GTOUUP GTOVUP GTOWUP	Mode
0	x	x	0	Output Stop (External pin: Hi-Z) GPT_OPS => 0 output
1	0	0	Level signal (gtuup_en) (gtvup_en) (gtwup_en)	Level Output Mode (Positive phase) (Positive logic)
1	0	1	Level signal (~gtuup_en) (~gtvup_en) (~gtwup_en)	Level Output Mode (Positive phase) (Negative logic)
1	1	0	PWM signal (PWM & gtuup_en) (PWM & gtvup_en) (PWM & gtwup_en)	PWM Output Mode (Positive phase) (Positive logic)
1	1	1	PWM signal (~(PWM & gtuup_en)) (~(PWM & gtvup_en)) (~(PWM & gtwup_en))	PWM Output Mode (Positive phase) (Negative logic)

Table 23.21 Output selection control method (negative phase)

Enable-phase output control	Negative-phase output (N) control	Invert-phase output control	Output port name (negative phase = Lo) (output selection internal node allocation)	
OPSCR.EN bit	OPSCR.N bit	OPSCR.INV bit	GTOULO GTOVLO GTOWLO	Mode
0	x	x	0	Output Stop (External pin: Hi-Z) GPT_OPS => 0 output
1	0	0	Level signal (gtulo_en) (gtvlo_en) (gtwlo_en)	Level Output Mode (Negative phase) (Positive logic)
1	0	1	Level signal (~gtulo_en) (~gtvlo_en) (~gtwlo_en)	Level Output Mode (Negative phase) (Negative logic)
1	1	0	PWM signal (PWM & gtulo_en) (PWM & gtvlo_en) (PWM & gtwlo_en)	PWM Output Mode (Negative phase) (Positive logic)
1	1	1	PWM signal (~(PWM & gtulo_en)) (~(PWM & gtvlo_en)) (~(PWM & gtwlo_en))	PWM Output Mode (Positive phase) (Negative logic)

23.3.11.5 Output selection control (group output disable function)

When OPSCR.GODF = 1 and the signal value selected by the OPSCR.GRP bit is high (output disable request), the GPT_OPS output pins are changed to Hi-Z asynchronously and the OPSCR.EN bit is set to 0 by the output disable request signal synchronized with PCLKD. For the return, set the OPSCR.EN to 1 after clearing the output disable request with software.

Table 23.20 输出选择控制方式（正相）

使能相位输出控制	正相输出(P)控制	反相输出控制	输出端口名称（正相=向上）（输出选择内部节点分配）	
OPSCR.EN bit	OPSCR.P bit	OPSCR.INV bit	GTOUUP GTOVUP GTOWUP	Mode
0	x	x	0	输出停止（外部引脚：Hi-Z）GPT_OPS=>0输出
1	0	0	电平信号(gtuup_en)(gtvup_en)(gtwup_en)	电平输出模式（正相）（正逻辑）
1	0	1	电平信号(~gtuup_en)(~gtvup_en)(~gtwup_en)	电平输出模式（正相）（负逻辑）
1	1	0	PWM signal (PWM & gtuup_en) (PWM & gtvup_en) (PWM & gtwup_en)	PWM输出模式（正相）（正逻辑）
1	1	1	PWM signal (~(PWM & gtuup_en)) (~(PWM & gtvup_en)) (~(PWM & gtwup_en))	PWM输出模式（正相）（负逻辑）

Table 23.21 输出选择控制方式（负相）

使能相位输出控制	负相输出(N)控制	反相输出控制	输出端口名称（负相=Lo）（输出选择内部节点分配）	
OPSCR.EN bit	OPSCR.N bit	OPSCR.INV bit	GTOULO GTOVLO GTOWLO	Mode
0	x	x	0	输出停止（外部引脚：Hi-Z）GPT_OPS=>0输出
1	0	0	电平信号(gtulo_en)(gtvlo_en)(gtwlo_en)	电平输出模式（负相）（正逻辑）
1	0	1	电平信号(~gtulo_en)(~gtvlo_en)(~gtwlo_en)	电平输出模式（负相）（负逻辑）
1	1	0	PWM signal (PWM & gtulo_en) (PWM & gtvlo_en) (PWM & gtwlo_en)	PWM输出模式（负相）（正逻辑）
1	1	1	PWM signal (~(PWM & gtulo_en)) (~(PWM & gtvlo_en)) (~(PWM & gtwlo_en))	PWM输出模式（负相）（负逻辑）

23.3.11.5 输出选择控制（组输出禁用功能）

当OPSCR.GODF=1且OPSCR.GRP位选择的信号值为高（输出禁用请求）时，GPT_OPS输出引脚异步更改为Hi-Z并且OPSCR.EN位由输出禁用设置为0请求信号与PCLKD同步。对于返回，请在用软件清除输出禁用请求后将OPSCR.EN设置为1。

The timing of OPSCR.EN bit cleared to 0 is 3 PCLKD cycles after generating the output disable request. To perform output disable control reliably, allow at least 4 PCLKD cycles after generating the output disable request (by clearing the output disable request flag in POEG) until the output disable request is terminated. For an example of the operation of group output disable control, see Figure 23.84.

23.3.11.6 Event Link Controller (ELC) output

In the GPT_OPS control flow conceptual diagram shown in Figure 23.81, (4) outputs the Hall sensor input signal edge to the ELC.

The Hall sensor input edge signal is the logical OR of the rising and falling edge signals of each U-phase/V-phase/W-phase input sampled at PCLKD. That is, if the high period of each of the U-phase/V-phase/W-phase input is short in duration, the Hall sensor edge input signal is not output at that time.

When OPSCR.FB bit = 0, the Hall sensor input edge signal is the logical OR of the edge signals of the external input phase sampled at PCLKD.

When OPSCR.FB bit = 1, the Hall sensor input edge signal is the logical OR of the edge of the soft setting (OPSCR.UF, VF, WF) sampled at PCLKD.

See Figure 23.82 to Figure 23.84 for examples of the output signal to the ELC.

OPSCR.EN位清零的时序是在产生输出禁用请求后的3个PCLKD周期。为了可靠地执行输出禁用控制，在生成输出禁用请求后（通过清除POEG中的输出禁用请求标志）至少允许4个PCLKD周期，直到输出禁用请求终止。组输出禁用控制的操作示例见图23.84。

23.3.11.6 事件链接控制器(ELC)输出

在图23.81所示的GPT_OPS控制流程概念图中，(4)将霍尔传感器输入信号沿输出到ELC。

霍尔传感器输入边沿信号是在PCLKD采样的每个U相V相W相输入的上升沿和下降沿信号的逻辑或。即，如果U相V相W相输入中的每一个的高电平时段持续时间短，则此时不输出霍尔传感器边沿输入信号。

当OPSCR.FB位=0时，霍尔传感器输入边沿信号是在PCLKD采样的外部输入相位边沿信号的逻辑或。

当OPSCR.FB位=1时，霍尔传感器输入边沿信号为软设置边沿的逻辑或(OPSCR.UF VF，WF）在PCLKD采样。

有关ELC的输出信号示例，请参见图23.82至图23.84。

23.3.11.7 GPT_OPS start operation setting flow

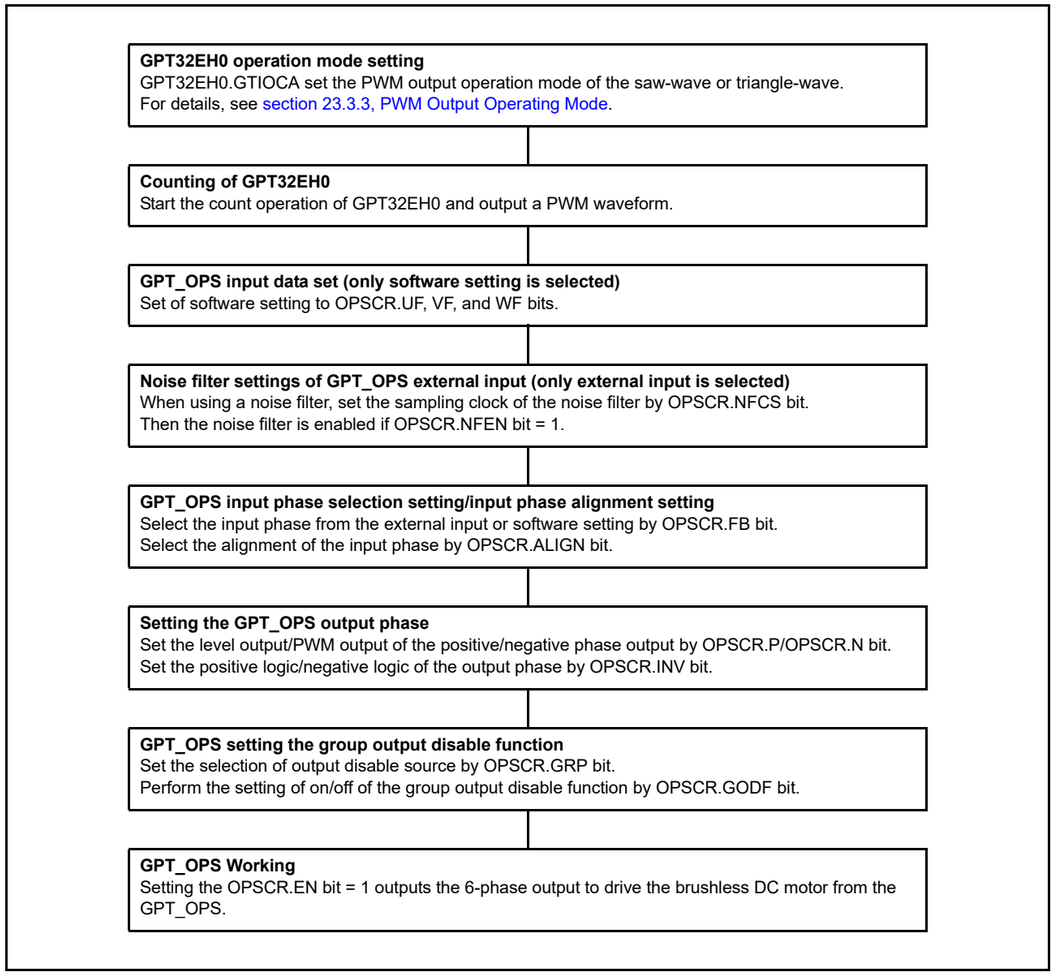


Figure 23.85 Example setting of GPT_OPS start operation

23.4 Interrupt Sources

23.4.1 Overview

The GPT provides the following interrupt sources:

- GTCCR input capture/compare match
- GTADTR compare match
- GTCNT counter overflow (GTPR compare match)/underflow.

Each interrupt source has its own status flag. When an interrupt source signal is generated, the associated status flag in GTST is set to 1. The associated status flag in GTST can be cleared by writing 0. If flag set and flag clear occur at the same time, flag clear takes priority over flag set. These flags are automatically updated by the internal state. Table 23.22 lists the GPT interrupt sources.

23.3.11.7 GPT_OPS启动操作设置流程

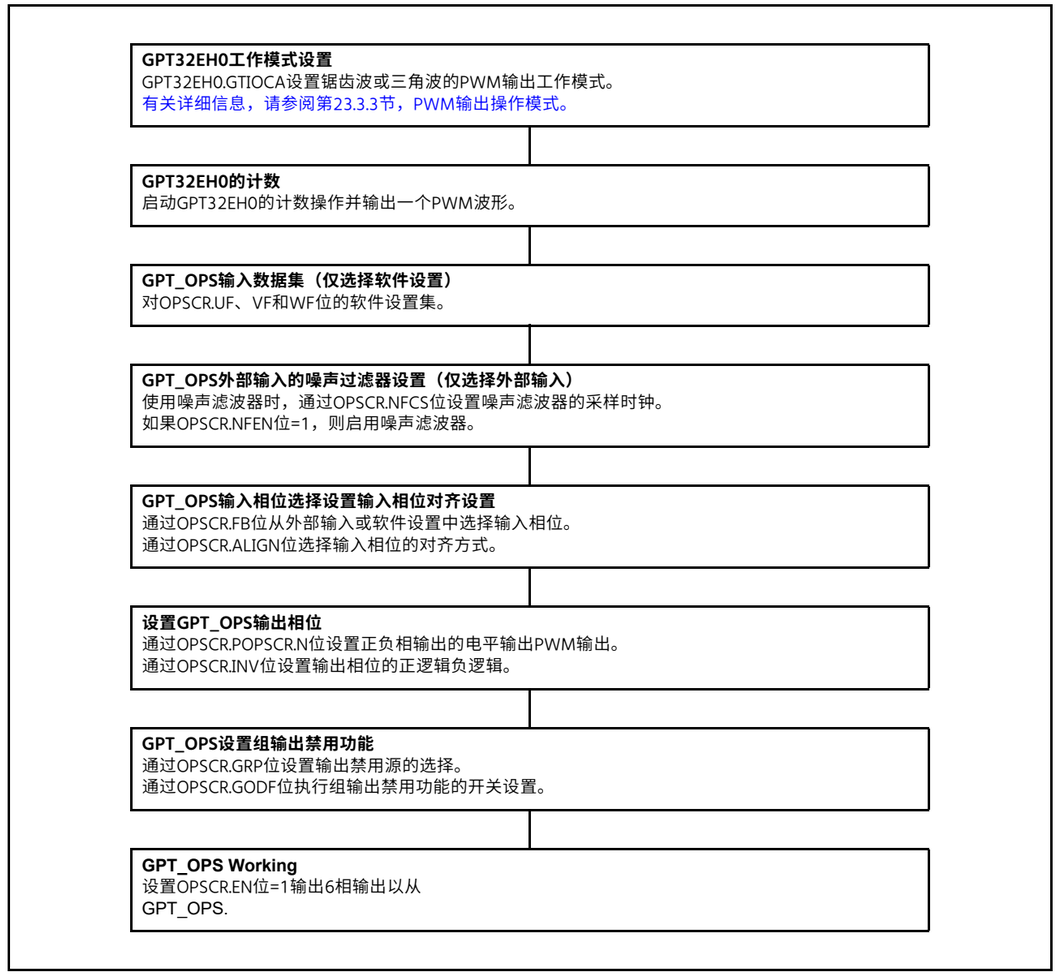


Figure 23.85 GPT_OPS启动操作的示例设置

23.4 中断源

23.4.1 Overview

GPT提供以下中断源：

- GTCCR输入捕获比较匹配
- GTADTR比较匹配
- GTCNT计数器上溢（GTPR比较匹配）下溢。

每个中断源都有自己的状态标志。当产生中断源信号时，GTST中的相关状态标志设置为1。GTST中的相关状态标志可以通过写入0来清除。如果标志设置和标志清除同时发生，则标志清除优先于标志放。这些标志由内部状态自动更新。表23.22列出了GPT中断源。

Table 23.22 Interrupt sources (1 of 4)

Channel	Name	Interrupt source	Interrupt flag	DMAC/DTC activation
0	GPT0_CCMPA	GPT32EH0.GTCCRA input capture/compare match	TCFA	Possible
	GPT0_CCMPB	GPT32EH0.GTCCRB input capture/compare match	TCFB	Possible
	GPT0_CMPC	GPT32EH0.GTCCRC compare match	TCFC	Possible
	GPT0_CMPD	GPT32EH0.GTCCRD compare match	TCFD	Possible
	GPT0_CMPE	GPT32EH0.GTCCRE compare match	TCFE	Possible
	GPT0_CMPF	GPT32EH0.GTCCRF compare match	TCFF	Possible
	GPT0_ADTRGA	GPT32EH0.GTADTRA compare match	ADTRAUF ADRTADF	Possible
	GPT0_ADTRGB	GPT32EH0.GTADTRB compare match	ADTRBUF ADRTBDF	Possible
	GPT0_OVF	GPT32EH0.GTCNT overflow (GPT32EH0.GTPR compare match)	TCFPO	Possible
	GPT0_UDF	GPT32EH0.GTCNT underflow	TCFPU	Possible
1	GPT1_CCMPA	GPT32EH1.GTCCRA input capture/compare match	TCFA	Possible
	GPT1_CCMPB	GPT32EH1.GTCCRB input capture/compare match	TCFB	Possible
	GPT1_CMPC	GPT32EH1.GTCCRC compare match	TCFC	Possible
	GPT1_CMPD	GPT32EH1.GTCCRD compare match	TCFD	Possible
	GPT1_CMPE	GPT32EH1.GTCCRE compare match	TCFE	Possible
	GPT1_CMPF	GPT32EH1.GTCCRF compare match	TCFF	Possible
	GPT1_ADTRGA	GPT32EH1.GTADTRA compare match	ADTRAUF ADRTADF	Possible
	GPT1_ADTRGB	GPT32EH1.GTADTRB compare match	ADTRBUF ADRTBDF	Possible
	GPT1_OVF	GPT32EH1.GTCNT overflow (GPT32EH1.GTPR compare match)	TCFPO	Possible
	GPT1_UDF	GPT32EH1.GTCNT underflow	TCFPU	Possible
2	GPT2_CCMPA	GPT32EH2.GTCCRA input capture/compare match	TCFA	Possible
	GPT2_CCMPB	GPT32EH2.GTCCRB input capture/compare match	TCFB	Possible
	GPT2_CMPC	GPT32EH2.GTCCRC compare match	TCFC	Possible
	GPT2_CMPD	GPT32EH2.GTCCRD compare match	TCFD	Possible
	GPT2_CMPE	GPT32EH2.GTCCRE compare match	TCFE	Possible
	GPT2_CMPF	GPT32EH2.GTCCRF compare match	TCFF	Possible
	GPT2_ADTRGA	GPT32EH2.GTCCRE compare match	ADTRAUF ADRTADF	Possible
	GPT2_ADTRGB	GPT32EH2.GTCCRF compare match	ADTRBUF ADRTBDF	Possible
	GPT2_OVF	GPT32EH2.GTCNT overflow (GPT32EH2.GTPR compare match)	TCFPO	Possible
	GPT2_UDF	GPT32EH2.GTCNT underflow	TCFPU	Possible

Table 23.22 中断源（4个中的1个）

Channel	Name	中断源	中断标志	DMAC/DTC activation
0	GPT0_CCMPA	GPT32EH0.GTCCRA输入捕捉比较匹配	TCFA	Possible
	GPT0_CCMPB	GPT32EH0.GTCCRB输入捕捉比较匹配	TCFB	Possible
	GPT0_CMPC	GPT32EH0.GTCCRC比较匹配	TCFC	Possible
	GPT0_CMPD	GPT32EH0.GTCCRD比较匹配	TCFD	Possible
	GPT0_CMPE	GPT32EH0.GTCCRE比较匹配	TCFE	Possible
	GPT0_CMPF	GPT32EH0.GTCCRF比较匹配	TCFF	Possible
	GPT0_ADTRGA	GPT32EH0.GTADTRA比较匹配	ADTRAUF ADRTADF	Possible
	GPT0_ADTRGB	GPT32EH0.GTADTRB比较匹配	ADTRBUF ADRTBDF	Possible
	GPT0_OVF	GPT32EH0.GTCNT溢出（GPT32EH0.GTPR比较匹配）	TCFPO	Possible
	GPT0_UDF	GPT32EH0.GTCNT underflow	TCFPU	Possible
1	GPT1_CCMPA	GPT32EH1.GTCCRA输入捕捉比较匹配	TCFA	Possible
	GPT1_CCMPB	GPT32EH1.GTCCRB输入捕捉比较匹配	TCFB	Possible
	GPT1_CMPC	GPT32EH1.GTCCRC比较匹配	TCFC	Possible
	GPT1_CMPD	GPT32EH1.GTCCRD比较匹配	TCFD	Possible
	GPT1_CMPE	GPT32EH1.GTCCRE比较匹配	TCFE	Possible
	GPT1_CMPF	GPT32EH1.GTCCRF比较匹配	TCFF	Possible
	GPT1_ADTRGA	GPT32EH1.GTADTRA比较匹配	ADTRAUF ADRTADF	Possible
	GPT1_ADTRGB	GPT32EH1.GTADTRB比较匹配	ADTRBUF ADRTBDF	Possible
	GPT1_OVF	GPT32EH1.GTCNT溢出（GPT32EH1.GTPR比较匹配）	TCFPO	Possible
	GPT1_UDF	GPT32EH1.GTCNT underflow	TCFPU	Possible
2	GPT2_CCMPA	GPT32EH2.GTCCRA输入捕捉比较匹配	TCFA	Possible
	GPT2_CCMPB	GPT32EH2.GTCCRB输入捕捉比较匹配	TCFB	Possible
	GPT2_CMPC	GPT32EH2.GTCCRC比较匹配	TCFC	Possible
	GPT2_CMPD	GPT32EH2.GTCCRD比较匹配	TCFD	Possible
	GPT2_CMPE	GPT32EH2.GTCCRE比较匹配	TCFE	Possible
	GPT2_CMPF	GPT32EH2.GTCCRF比较匹配	TCFF	Possible
	GPT2_ADTRGA	GPT32EH2.GTCCRE比较匹配	ADTRAUF ADRTADF	Possible
	GPT2_ADTRGB	GPT32EH2.GTCCRF比较匹配	ADTRBUF ADRTBDF	Possible
	GPT2_OVF	GPT32EH2.GTCNT溢出（GPT32EH2.GTPR比较匹配）	TCFPO	Possible
	GPT2_UDF	GPT32EH2.GTCNT underflow	TCFPU	Possible

Table 23.22 Interrupt sources (2 of 4)

Channel	Name	Interrupt source	Interrupt flag	DMAC/DTC activation
3	GPT3_CCMPA	GPT32EH3.GTCCRA input capture/compare match	TCFA	Possible
	GPT3_CCMPB	GPT32EH3.GTCCRB input capture/compare match	TCFB	Possible
	GPT3_CMPC	GPT32EH3.GTCCRC compare match	TCFC	Possible
	GPT3_CMPD	GPT32EH3.GTCCRD compare match	TCFD	Possible
	GPT3_CMPE	GPT32EH3.GTCCRE compare match	TCFE	Possible
	GPT3_CMPF	GPT32EH3.GTCCRF compare match	TCFF	Possible
	GPT3_ADTRGA	GPT32EH3.GTADTRA compare match	ADTRAUF ADRTADF	Possible
	GPT3_ADTRGB	GPT32EH3.GTADTRB compare match	ADTRBUF ADRTBDF	Possible
	GPT3_OVF	GPT32EH3.GTCNT overflow (GPT32EH3.GTPR compare match)	TCFPO	Possible
	GPT3_UDF	GPT32EH3.GTCNT underflow	TCFPU	Possible
4	GPT4_CCMPA	GPT32E4.GTCCRA input capture/compare match	TCFA	Possible
	GPT4_CCMPB	GPT32E4.GTCCRB input capture/compare match	TCFB	Possible
	GPT4_CMPC	GPT32E4.GTCCRC compare match	TCFC	Possible
	GPT4_CMPD	GPT32E4.GTCCRD compare match	TCFD	Possible
	GPT4_CMPE	GPT32E4.GTCCRE compare match	TCFE	Possible
	GPT4_CMPF	GPT32E4.GTCCRF compare match	TCFF	Possible
	GPT4_ADTRGA	GPT32E4.GTADTRA compare match	ADTRAUF ADRTADF	Possible
	GPT4_ADTRGB	GPT32E4.GTADTRB compare match	ADTRBUF ADRTBDF	Possible
	GPT4_OVF	GPT32E4.GTCNT overflow (GPT32E4.GTPR compare match)	TCFPO	Possible
	GPT4_UDF	GPT32E4.GTCNT underflow	TCFPU	Possible
5	GPT5_CCMPA	GPT32E5.GTCCRA input capture/compare match	TCFA	Possible
	GPT5_CCMPB	GPT32E5.GTCCRB input capture/compare match	TCFB	Possible
	GPT5_CMPC	GPT32E5.GTCCRC compare match	TCFC	Possible
	GPT5_CMPD	GPT32E5.GTCCRD compare match	TCFD	Possible
	GPT5_CMPE	GPT32E5.GTCCRE compare match	TCFE	Possible
	GPT5_CMPF	GPT32E5.GTCCRF compare match	TCFF	Possible
	GPT5_ADTRGA	GPT32E5.GTADTRA compare match	ADTRAUF ADRTADF	Possible
	GPT5_ADTRGB	GPT32E5.GTADTRB compare match	ADTRBUF ADRTBDF	Possible
	GPT5_OVF	GPT32E5.GTCNT overflow (GPT32E5.GTPR compare match)	TCFPO	Possible
	GPT5_UDF	GPT32E5.GTCNT underflow	TCFPU	Possible

Table 23.22 中断源（4个中的2个）

Channel	Name	中断源	中断标志	DMAC/DTC activation
3	GPT3_CCMPA	GPT32EH3.GTCCRA输入捕捉比较匹配	TCFA	Possible
	GPT3_CCMPB	GPT32EH3.GTCCRB输入捕捉比较匹配	TCFB	Possible
	GPT3_CMPC	GPT32EH3.GTCCRC比较匹配	TCFC	Possible
	GPT3_CMPD	GPT32EH3.GTCCRD比较匹配	TCFD	Possible
	GPT3_CMPE	GPT32EH3.GTCCRE比较匹配	TCFE	Possible
	GPT3_CMPF	GPT32EH3.GTCCRF比较匹配	TCFF	Possible
	GPT3_ADTRGA	GPT32EH3.GTADTRA比较匹配	ADTRAUF ADRTADF	Possible
	GPT3_ADTRGB	GPT32EH3.GTADTRB比较匹配	ADTRBUF ADRTBDF	Possible
	GPT3_OVF	GPT32EH3.GTCNT溢出（GPT32EH3.GTPR比较匹配）	TCFPO	Possible
	GPT3_UDF	GPT32EH3.GTCNT underflow	TCFPU	Possible
4	GPT4_CCMPA	GPT32E4.GTCCRA输入捕捉比较匹配	TCFA	Possible
	GPT4_CCMPB	GPT32E4.GTCCRB输入捕捉比较匹配	TCFB	Possible
	GPT4_CMPC	GPT32E4.GTCCRC比较匹配	TCFC	Possible
	GPT4_CMPD	GPT32E4.GTCCRD比较匹配	TCFD	Possible
	GPT4_CMPE	GPT32E4.GTCCRE比较匹配	TCFE	Possible
	GPT4_CMPF	GPT32E4.GTCCRF比较匹配	TCFF	Possible
	GPT4_ADTRGA	GPT32E4.GTADTRA比较匹配	ADTRAUF ADRTADF	Possible
	GPT4_ADTRGB	GPT32E4.GTADTRB比较匹配	ADTRBUF ADRTBDF	Possible
	GPT4_OVF	GPT32E4.GTCNT溢出（GPT32E4.GTPR比较匹配）	TCFPO	Possible
	GPT4_UDF	GPT32E4.GTCNT underflow	TCFPU	Possible
5	GPT5_CCMPA	GPT32E5.GTCCRA输入捕捉比较匹配	TCFA	Possible
	GPT5_CCMPB	GPT32E5.GTCCRB输入捕捉比较匹配	TCFB	Possible
	GPT5_CMPC	GPT32E5.GTCCRC比较匹配	TCFC	Possible
	GPT5_CMPD	GPT32E5.GTCCRD比较匹配	TCFD	Possible
	GPT5_CMPE	GPT32E5.GTCCRE比较匹配	TCFE	Possible
	GPT5_CMPF	GPT32E5.GTCCRF比较匹配	TCFF	Possible
	GPT5_ADTRGA	GPT32E5.GTADTRA比较匹配	ADTRAUF ADRTADF	Possible
	GPT5_ADTRGB	GPT32E5.GTADTRB比较匹配	ADTRBUF ADRTBDF	Possible
	GPT5_OVF	GPT32E5.GTCNT溢出（GPT32E5.GTPR比较匹配）	TCFPO	Possible
	GPT5_UDF	GPT32E5.GTCNT underflow	TCFPU	Possible

Table 23.22 Interrupt sources (3 of 4)

Channel	Name	Interrupt source	Interrupt flag	DMAC/DTC activation
6	GPT6_CCMPA	GPT32E6.GTCCRA input capture/compare match	TCFA	Possible
	GPT6_CCMPB	GPT32E6.GTCCRB input capture/compare match	TCFB	Possible
	GPT6_CMPC	GPT32E6.GTCCRC compare match	TCFC	Possible
	GPT6_CMPD	GPT32E6.GTCCRD compare match	TCFD	Possible
	GPT6_CMPE	GPT32E6.GTCCRE compare match	TCFE	Possible
	GPT6_CMPF	GPT32E6.GTCCRF compare match	TCFF	Possible
	GPT6_ADTRGA	GPT32E6.GTADTRA compare match	ADTRAUF ADRTADF	Possible
	GPT6_ADTRGB	GPT32E6.GTADTRB compare match	ADTRBUF ADRTBDF	Possible
	GPT6_OVF	GPT32E6.GTCNT overflow (GPT32E6.GTPR compare match)	TCFPO	Possible
	GPT6_UDF	GPT32E6.GTCNT underflow	TCFPU	Possible
7	GPT7_CCMPA	GPT32E7.GTCCRA input capture/compare match	TCFA	Possible
	GPT7_CCMPB	GPT32E7.GTCCRB input capture/compare match	TCFB	Possible
	GPT7_CMPC	GPT32E7.GTCCRC compare match	TCFC	Possible
	GPT7_CMPD	GPT32E7.GTCCRD compare match	TCFD	Possible
	GPT7_CMPE	GPT32E7.GTCCRE compare match	TCFE	Possible
	GPT7_CMPF	GPT32E7.GTCCRF compare match	TCFF	Possible
	GPT7_ADTRGA	GPT32E7.GTADTRA compare match	ADTRAUF ADRTADF	Possible
	GPT7_ADTRGB	GPT32E7.GTADTRB compare match	ADTRBUF ADRTBDF	Possible
	GPT7_OVF	GPT32E7.GTCNT overflow (GPT32E7.GTPR compare match)	TCFPO	Possible
	GPT7_UDF	GPT32E7.GTCNT underflow	TCFPU	Possible
8	GPT8_CCMPA	GPT328.GTCCRA input capture/compare match	TCFA	Possible
	GPT8_CCMPB	GPT328.GTCCRB input capture/compare match	TCFB	Possible
	GPT8_CMPC	GPT328.GTCCRC compare match	TCFC	Possible
	GPT8_CMPD	GPT328.GTCCRD compare match	TCFD	Possible
	GPT8_CMPE	GPT328.GTCCRE compare match	TCFE	Possible
	GPT8_CMPF	GPT328.GTCCRF compare match	TCFF	Possible
	GPT8_OVF	GPT328.GTCNT overflow (GPT328.GTPR compare match)	TCFPO	Possible
	GPT8_UDF	GPT328.GTCNT underflow	TCFPU	Possible
9	GPT9_CCMPA	GPT329.GTCCRA input capture/compare match	TCFA	Possible
	GPT9_CCMPB	GPT329.GTCCRB input capture/compare match	TCFB	Possible
	GPT9_CMPC	GPT329.GTCCRC compare match	TCFC	Possible
	GPT9_CMPD	GPT329.GTCCRD compare match	TCFD	Possible
	GPT9_CMPE	GPT329.GTCCRE compare match	TCFE	Possible
	GPT9_CMPF	GPT329.GTCCRF compare match	TCFF	Possible
	GPT9_OVF	GPT329.GTCNT overflow (GPT329.GTPR compare match)	TCFPO	Possible
	GPT9_UDF	GPT329.GTCNT underflow	TCFPU	Possible

Table 23.22 中断源（4个中的3个）

Channel	Name	中断源	中断标志	DMAC/DTC activation
6	GPT6_CCMPA	GPT32E6.GTCCRA输入捕捉比较匹配	TCFA	Possible
	GPT6_CCMPB	GPT32E6.GTCCRB输入捕捉比较匹配	TCFB	Possible
	GPT6_CMPC	GPT32E6.GTCCRC比较匹配	TCFC	Possible
	GPT6_CMPD	GPT32E6.GTCCRD比较匹配	TCFD	Possible
	GPT6_CMPE	GPT32E6.GTCCRE比较匹配	TCFE	Possible
	GPT6_CMPF	GPT32E6.GTCCRF比较匹配	TCFF	Possible
	GPT6_ADTRGA	GPT32E6.GTADTRA比较匹配	ADTRAUF ADRTADF	Possible
	GPT6_ADTRGB	GPT32E6.GTADTRB比较匹配	ADTRBUF ADRTBDF	Possible
	GPT6_OVF	GPT32E6.GTCNT溢出（GPT32E6.GTPR比较匹配）	TCFPO	Possible
	GPT6_UDF	GPT32E6.GTCNT underflow	TCFPU	Possible
7	GPT7_CCMPA	GPT32E7.GTCCRA输入捕捉比较匹配	TCFA	Possible
	GPT7_CCMPB	GPT32E7.GTCCRB输入捕捉比较匹配	TCFB	Possible
	GPT7_CMPC	GPT32E7.GTCCRC比较匹配	TCFC	Possible
	GPT7_CMPD	GPT32E7.GTCCRD比较匹配	TCFD	Possible
	GPT7_CMPE	GPT32E7.GTCCRE比较匹配	TCFE	Possible
	GPT7_CMPF	GPT32E7.GTCCRF比较匹配	TCFF	Possible
	GPT7_ADTRGA	GPT32E7.GTADTRA比较匹配	ADTRAUF ADRTADF	Possible
	GPT7_ADTRGB	GPT32E7.GTADTRB比较匹配	ADTRBUF ADRTBDF	Possible
	GPT7_OVF	GPT32E7.GTCNT溢出（GPT32E7.GTPR比较匹配）	TCFPO	Possible
	GPT7_UDF	GPT32E7.GTCNT underflow	TCFPU	Possible
8	GPT8_CCMPA	GPT328.GTCCRA输入捕捉比较匹配	TCFA	Possible
	GPT8_CCMPB	GPT328.GTCCRB输入捕捉比较匹配	TCFB	Possible
	GPT8_CMPC	GPT328.GTCCRC比较匹配	TCFC	Possible
	GPT8_CMPD	GPT328.GTCCRD比较匹配	TCFD	Possible
	GPT8_CMPE	GPT328.GTCCRE比较匹配	TCFE	Possible
	GPT8_CMPF	GPT328.GTCCRF比较匹配	TCFF	Possible
	GPT8_OVF	GPT328.GTCNT溢出（GPT328.GTPR比较匹配）	TCFPO	Possible
	GPT8_UDF	GPT328.GTCNT underflow	TCFPU	Possible
9	GPT9_CCMPA	GPT329.GTCCRA输入捕捉比较匹配	TCFA	Possible
	GPT9_CCMPB	GPT329.GTCCRB输入捕捉比较匹配	TCFB	Possible
	GPT9_CMPC	GPT329.GTCCRC比较匹配	TCFC	Possible
	GPT9_CMPD	GPT329.GTCCRD比较匹配	TCFD	Possible
	GPT9_CMPE	GPT329.GTCCRE比较匹配	TCFE	Possible
	GPT9_CMPF	GPT329.GTCCRF比较匹配	TCFF	Possible
	GPT9_OVF	GPT329.GTCNT溢出（GPT329.GTPR比较匹配）	TCFPO	Possible
	GPT9_UDF	GPT329.GTCNT underflow	TCFPU	Possible

Table 23.22 Interrupt sources (4 of 4)

Channel	Name	Interrupt source	Interrupt flag	DMAC/DTC activation
10	GPT10_CCMPA	GPT3210.GTCCRA input capture/compare match	TCFA	Possible
	GPT10_CCMPB	GPT3210.GTCCRB input capture/compare match	TCFB	Possible
	GPT10_CMPC	GPT3210.GTCCRC compare match	TCFC	Possible
	GPT10_CMPD	GPT3210.GTCCRD compare match	TCFD	Possible
	GPT10_CMPE	GPT3210.GTCCRE compare match	TCFE	Possible
	GPT10_CMPF	GPT3210.GTCCRF compare match	TCFF	Possible
	GPT10_OVF	GPT3210.GTCNT overflow (GPT3210.GTPR compare match)	TCFPO	Possible
	GPT10_UDF	GPT3210.GTCNT underflow	TCFPU	Possible
11	GPT11_CCMPA	GPT3211.GTCCRA input capture/compare match	TCFA	Possible
	GPT11_CCMPB	GPT3211.GTCCRB input capture/compare match	TCFB	Possible
	GPT11_CMPC	GPT3211.GTCCRC compare match	TCFC	Possible
	GPT11_CMPD	GPT3211.GTCCRD compare match	TCFD	Possible
	GPT11_CMPE	GPT3211.GTCCRE compare match	TCFE	Possible
	GPT11_CMPF	GPT3211.GTCCRF compare match	TCFF	Possible
	GPT11_OVF	GPT3211.GTCNT overflow (GPT3211.GTPR compare match)	TCFPO	Possible
	GPT11_UDF	GPT3211.GTCNT underflow	TCFPU	Possible
12	GPT12_CCMPA	GPT3212.GTCCRA input capture/compare match	TCFA	Possible
	GPT12_CCMPB	GPT3212.GTCCRB input capture/compare match	TCFB	Possible
	GPT12_CMPC	GPT3212.GTCCRC compare match	TCFC	Possible
	GPT12_CMPD	GPT3212.GTCCRD compare match	TCFD	Possible
	GPT12_CMPE	GPT3212.GTCCRE compare match	TCFE	Possible
	GPT12_CMPF	GPT3212.GTCCRF compare match	TCFF	Possible
	GPT12_OVF	GPT3212.GTCNT overflow (GPT3212.GTPR compare match)	TCFPO	Possible
	GPT12_UDF	GPT3212.GTCNT underflow	TCFPU	Possible
13	GPT13_CCMPA	GPT3213.GTCCRA input capture/compare match	TCFA	Possible
	GPT13_CCMPB	GPT3213.GTCCRB input capture/compare match	TCFB	Possible
	GPT13_CMPC	GPT3213.GTCCRC compare match	TCFC	Possible
	GPT13_CMPD	GPT3213.GTCCRD compare match	TCFD	Possible
	GPT13_CMPE	GPT3213.GTCCRE compare match	TCFE	Possible
	GPT13_CMPF	GPT3213.GTCCRF compare match	TCFF	Possible
	GPT13_OVF	GPT3213.GTCNT overflow (GPT3213.GTPR compare match)	TCFPO	Possible
	GPT13_UDF	GPT3213.GTCNT underflow	TCFPU	Possible

(1) GPTn_ADTRGA interrupt (n = 0 to 7)

When the GTCNT counter value matches with the GTADTRA register, an interrupt request is generated under the following conditions:

- In up-counting, the interrupt enable bit (ADTRAUEN) in the GTINTAD register is 1
- In down-counting, the interrupt enable bit (ADTRADEN) in the GTINTAD register is 1.

In event count operation, this interrupt request is not generated.

(2) GPTn_ADTRGB interrupt (n = 0 to 7)

When the GTCNT counter value matches with the GTADTRB register, an interrupt request is generated under the following conditions:

- In up-counting, the interrupt enable bit (ADTRBUEN) in the GTINTAD register is 1
- In down-counting, the interrupt enable bit (ADTRBDEN) in the GTINTAD register is 1.

Table 23.22 中断源（4个中的4个）

Channel	Name	中断源	中断标志	DMAC/DTC activation
10	GPT10_CCMPA	GPT3210.GTCCRA输入捕捉比较匹配	TCFA	Possible
	GPT10_CCMPB	GPT3210.GTCCRB输入捕捉比较匹配	TCFB	Possible
	GPT10_CMPC	GPT3210.GTCCRC比较匹配	TCFC	Possible
	GPT10_CMPD	GPT3210.GTCCRD比较匹配	TCFD	Possible
	GPT10_CMPE	GPT3210.GTCCRE比较匹配	TCFE	Possible
	GPT10_CMPF	GPT3210.GTCCRF比较匹配	TCFF	Possible
	GPT10_OVF	GPT3210.GTCNT溢出（GPT3210.GTPR比较匹配）	TCFPO	Possible
	GPT10_UDF	GPT3210.GTCNT underflow	TCFPU	Possible
11	GPT11_CCMPA	GPT3211.GTCCRA输入捕捉比较匹配	TCFA	Possible
	GPT11_CCMPB	GPT3211.GTCCRB输入捕捉比较匹配	TCFB	Possible
	GPT11_CMPC	GPT3211.GTCCRC比较匹配	TCFC	Possible
	GPT11_CMPD	GPT3211.GTCCRD比较匹配	TCFD	Possible
	GPT11_CMPE	GPT3211.GTCCRE比较匹配	TCFE	Possible
	GPT11_CMPF	GPT3211.GTCCRF比较匹配	TCFF	Possible
	GPT11_OVF	GPT3211.GTCNT溢出（GPT3211.GTPR比较匹配）	TCFPO	Possible
	GPT11_UDF	GPT3211.GTCNT underflow	TCFPU	Possible
12	GPT12_CCMPA	GPT3212.GTCCRA输入捕捉比较匹配	TCFA	Possible
	GPT12_CCMPB	GPT3212.GTCCRB输入捕捉比较匹配	TCFB	Possible
	GPT12_CMPC	GPT3212.GTCCRC比较匹配	TCFC	Possible
	GPT12_CMPD	GPT3212.GTCCRD比较匹配	TCFD	Possible
	GPT12_CMPE	GPT3212.GTCCRE比较匹配	TCFE	Possible
	GPT12_CMPF	GPT3212.GTCCRF比较匹配	TCFF	Possible
	GPT12_OVF	GPT3212.GTCNT溢出（GPT3212.GTPR比较匹配）	TCFPO	Possible
	GPT12_UDF	GPT3212.GTCNT underflow	TCFPU	Possible
13	GPT13_CCMPA	GPT3213.GTCCRA输入捕捉比较匹配	TCFA	Possible
	GPT13_CCMPB	GPT3213.GTCCRB输入捕捉比较匹配	TCFB	Possible
	GPT13_CMPC	GPT3213.GTCCRC比较匹配	TCFC	Possible
	GPT13_CMPD	GPT3213.GTCCRD比较匹配	TCFD	Possible
	GPT13_CMPE	GPT3213.GTCCRE比较匹配	TCFE	Possible
	GPT13_CMPF	GPT3213.GTCCRF比较匹配	TCFF	Possible
	GPT13_OVF	GPT3213.GTCNT溢出（GPT3213.GTPR比较匹配）	TCFPO	Possible
	GPT13_UDF	GPT3213.GTCNT underflow	TCFPU	Possible

(1) GPTn_ADTRGA中断（n=0到7）

当GTCNT计数器值与GTADTRA寄存器匹配时，会在以下条件下产生中断请求：

- 在递增计数中，GTINTAD寄存器中的中断使能位（ADTRAUEN）为1
- 在递减计数中，GTINTAD寄存器中的中断使能位（ADTRADEN）为1。

在事件计数操作中，不会产生此中断请求。

(2) GPTn_ADTRGB中断（n=0到7）

当GTCNT计数器值与GTADTRB寄存器匹配时，会在以下情况下产生中断请求：

- 在递增计数中，GTINTAD寄存器中的中断使能位（ADTRBUEN）为1
- 在递减计数中，GTINTAD寄存器中的中断使能位（ADTRBDEN）为1。

In event count operation, this interrupt request is not generated.

(3) GPTn_CCMPA interrupt (n = 0 to 13)

An interrupt request is generated under the following conditions:

- When the GTCCRA register functions as a compare match register, the GTCNT counter value matches with the GTCCRA register
- When the GTCCRA register functions as an input capture register, the input capture signal causes transfer of the GTCNT counter value to the GTCCRA register.

(4) GPTn_CCMPB interrupt (n = 0 to 13)

An interrupt request is generated under the following conditions:

- When the GTCCRB register functions as a compare match register, the GTCNT counter value matches with the GTCCRB register
- When the GTCCRB register functions as an input capture register, the input capture signal causes transfer of the GTCNT counter value to the GTCCRB register.

(5) GPTn_CMPC interrupt (n = 0 to 13)

An interrupt request is generated under the following condition:

- When the GTCCRC register functions as a compare match register, the GTCNT counter value matches with the GTCCRC register.

A compare match is not performed and an interrupt is not requested under the following conditions:

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)
- GTBER.CCRA[1:0] = 01b, 10b, 11b (buffer operation with the GTCCRC register).

(6) GPTn_CMPD interrupt (n = 0 to 13)

An interrupt request is generated under the following condition:

- When the GTCCRD register functions as a compare match register, the GTCNT counter value matches with the GTCCRD register.

A compare match is not performed and an interrupt is not requested under the following conditions:

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)
- GTBER.CCRA[1:0] = 10b, 11b (buffer operation with the GTCCRD register).

(7) GPTn_CMPE interrupt (n = 0 to 13)

An interrupt request is generated under the following condition:

- When the GTCCRE register functions as a compare match register, the GTCNT counter value matches with the GTCCRE register.

A compare match is not performed and an interrupt is not requested under the following conditions:

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)
- GTBER.CCRB[1:0] = 01b, 10b, 11b (buffer operation with the GTCCRE register).

(8) GPTn_CMPF interrupt (n = 0 to 13)

An interrupt request is generated under the following condition:

- When the GTCCRF register functions as a compare match register, the GTCNT counter value matches with the GTCCRF register.

在事件计数操作中，不会产生此中断请求。

(3) GPTn_CCMPA中断（n=0到13）

在以下情况下会产生中断请求：

- 当GTCCRA寄存器用作比较匹配寄存器时，GTCNT计数器值与GTCCRA register
- 当GTCCRA寄存器用作输入捕捉寄存器时，输入捕捉信号会导致GTCNT计数器值到GTCCRA寄存器。

(4) GPTn_CCMPB中断（n=0到13）

在以下情况下会产生中断请求：

- 当GTCCRB寄存器用作比较匹配寄存器时，GTCNT计数器值与GTCCRB register
- 当GTCCRB寄存器用作输入捕捉寄存器时，输入捕捉信号会导致GTCNT计数器值到GTCCRB寄存器。

(5) GPTn_CMPC中断（n=0到13）

在以下情况下会产生中断请求：

- 当GTCCRC寄存器用作比较匹配寄存器时，GTCNT计数器值与GTCCRC register.

在以下情况下不执行比较匹配并且不请求中断：

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)
- GTBER.CCRA[1:0]=01b 10b 11b（使用GTCCRC寄存器进行缓冲操作）。

(6) GPTn_CMPD中断（n=0到13）

在以下情况下会产生中断请求：

- 当GTCCRD寄存器用作比较匹配寄存器时，GTCNT计数器值与GTCCRD register.

在以下情况下不执行比较匹配并且不请求中断：

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)
- GTBER.CCRA[1:0]=10b 11b（使用GTCCRD寄存器进行缓冲操作）。

(7) GPTn_CMPE中断（n=0到13）

在以下情况下会产生中断请求：

- 当GTCCRE寄存器用作比较匹配寄存器时，GTCNT计数器值与GTCCRE register.

在以下情况下不执行比较匹配并且不请求中断：

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)
- GTBER.CCRB[1:0]=01b 10b 11b（使用GTCCRE寄存器进行缓冲操作）。

(8) GPTn_CMPF中断（n=0到13）

在以下情况下会产生中断请求：

- 当GTCCRF寄存器用作比较匹配寄存器时，GTCNT计数器值与GTCCRF register.

A compare match is not performed and an interrupt is not requested under the following conditions:

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)
- GTBER.CCRB[1:0] = 10b, 11b (buffer operation with the GTCCRF register).

(9) GPTn_OVF interrupt (n = 0 to 13)

An interrupt request is generated under the following conditions:

- In saw-wave mode, interrupt requests are enabled at overflows (when the GTCNT counter value changes from GTPR to 0 during up-counting)
- In triangle-wave mode, interrupt requests are enabled at crests (GTCNT changes from GTPR to GTPR-1)
- In counting by hardware sources, overflow (GTCNT changes from GTPR to 0 in up count) has occurred.

(10) GPTn_UDF interrupt (n = 0 to 13)

An interrupt request is generated under the following conditions:

- In saw-wave mode, interrupt requests are enabled at underflows (when the GTCNT counter value changes from 0 to GTPR during down-counting)
- In triangle-wave mode, interrupt requests are enabled at troughs (GTCNT changes from 0 to 1).
- In counting by hardware sources, underflow (GTCNT changes from 0 to GTPR in down count) has occurred.

Table 23.23 Interrupt signals, interrupt permission bits, and interrupt status flags

Interrupt signal	Interrupt permission bit	Interrupt status flag
GPTn_UDF	— *1	GTST[7] (TCFPU)
GPTn_OVF		GTST[6] (TCFPO)
GPTn_ADTRGB	GTINTAD[19] (ADTRBDEN) GTINTAD[18] (ADTRBUEN)	GTST[19] (ADTRBDF) GTST[18] (ADTRBUF)
GPTn_ADTRGA	GTINTAD[17] (ADTRADEN) GTINTAD[16] (ADTRAUEN)	GTST[17] (ADTRADF) GTST[16] (ADTRAUF)
GPTn_CMPF	— *1	GTST[5] (TCFF)
GPTn_CMPE		GTST[4] (TCFE)
GPTn_CMPD		GTST[3] (TCFD)
GPTn_CMPC		GTST[2] (TCFC)
GPTn_CCMPB		GTST[1] (TCFB)
GPTn_CCMPA		GTST[0] (TCFA)

Note 1. Interrupt is always permitted.

23.4.2 DMAC/DTC Activation

The DMAC and DTC can be activated by the interrupt in each channel. For details, see section 14, Interrupt Controller Unit (ICU), and section 18, Data Transfer Controller (DTC).

23.4.3 Interrupt and A/D Conversion Request Skipping Function

By setting the GTITC register, the GTCNT counter overflow (GTPR compare match) interrupt (GPTn_OVF) and underflow interrupt (GPTn_UDF) can be skipped. Other interrupts and A/D converter start request signals can be skipped in coordination with the GPTn_OVF/GPTn_UDF skipping function.

The interrupt request skipping function only depends on the setting of GTITC register and is independent of the setting of interrupt permission bits in the GTINTAD register.

When both troughs and crests are counted and skipped in triangle-wave mode, if the number of times of skipping is odd, GPTn_OVF/GPTn_UDF interrupt requests cannot be generated at troughs only or at crests only depending on the

在以下情况下不执行比较匹配并且不请求中断：

- GTCR.MD[2:0] = 001b (saw-wave one-shot pulse mode)
- GTCR.MD[2:0] = 110b (triangle-wave PWM mode 3)
- GTBER.CCRB[1:0]=10b 11b（使用GTCCRF寄存器进行缓冲操作）。

(9) GPTn_OVF中断（n=0到13）

在以下情况下会产生中断请求：

- 在锯齿波模式下，中断请求在溢出时启用（当GTCNT计数器值从向上计数期间GTPR为0）
- 在三角波模式下，在波峰处启用中断请求（GTCNT从GTPR变为GTPR-1）
- 在硬件源的计数中，发生了溢出（GTCNT在向上计数中从GTPR变为0）。

(10)GPTn_UDF中断（n=0到13）

在以下情况下会产生中断请求：

- 在锯齿波模式下，中断请求在下溢时启用（当GTCNT计数器值从0变为GTPR during down-counting)
- 在三角波模式下，中断请求在波谷处启用（GTCNT从0变为1）。
- 在硬件源的计数中，发生了下溢（向下计数时GTCNT从0变为GTPR）。

Table 23.23 中断信号、中断许可位和中断状态标志

中断信号	中断许可位	中断状态标志
GPTn_UDF	— *1	GTST[7] (TCFPU)
GPTn_OVF		GTST[6] (TCFPO)
GPTn_ADTRGB	GTINTAD[19] (ADTRBDEN) GTINTAD[18] (ADTRBUEN)	GTST[19] (ADTRBDF) GTST[18] (ADTRBUF)
GPTn_ADTRGA	GTINTAD[17] (ADTRADEN) GTINTAD[16] (ADTRAUEN)	GTST[17] (ADTRADF) GTST[16] (ADTRAUF)
GPTn_CMPF	— *1	GTST[5] (TCFF)
GPTn_CMPE		GTST[4] (TCFE)
GPTn_CMPD		GTST[3] (TCFD)
GPTn_CMPC		GTST[2] (TCFC)
GPTn_CCMPB		GTST[1] (TCFB)
GPTn_CCMPA		GTST[0] (TCFA)

Note 1. 总是允许中断。

23.4.2 DMAC/DTC Activation

DMAC和DTC可以通过每个通道中的中断来激活。有关详细信息，请参见第14节，中断控制器单元(ICU)和第18节，数据传输控制器(DTC)。

23.4.3 中断和AD转换请求跳过功能

通过设置GTITC寄存器，可以跳过GTCNT计数器溢出（GTPR比较匹配）中断（GPTn_OVF）和下溢中断（GPTn_UDF）。其他中断和AD转换器启动请求信号可以与GPTn_OVFGPTn_UDF跳过功能配合跳过。

中断请求跳过功能仅取决于GTITC寄存器的设置，与GTINTAD寄存器中中断允许位的设置无关。

三角波模式下波谷和波峰都计数跳越时，若跳越次数为奇数，
GPTn_OVFGPTn_UDF中断请求不能仅在波谷或仅在波峰产生，具体取决于

skipping counter start timing. To count both troughs and crests and generate the GPTn_OVF/GPTn_UDF interrupts at troughs only or crests only in triangle-wave mode, you must set an even number of skips.

Similarly, in saw-wave mode, when both overflows and underflows are counted and skipped with the count direction changed, GPTn_OVF interrupt requests cannot be generated on either overflows or underflows only. To count both overflows and underflows with the count direction changed and generate the GPTn_OVF/GPTn_UDF interrupts on either overflows or underflows only in saw wave mode, you must first check the skipping state.

Before changing the skipping count, you must release the skipping count setting (GTITC.IVTC[1:0] bits = 00b).

Figure 23.86 to Figure 23.91 show examples of skipping function operation.

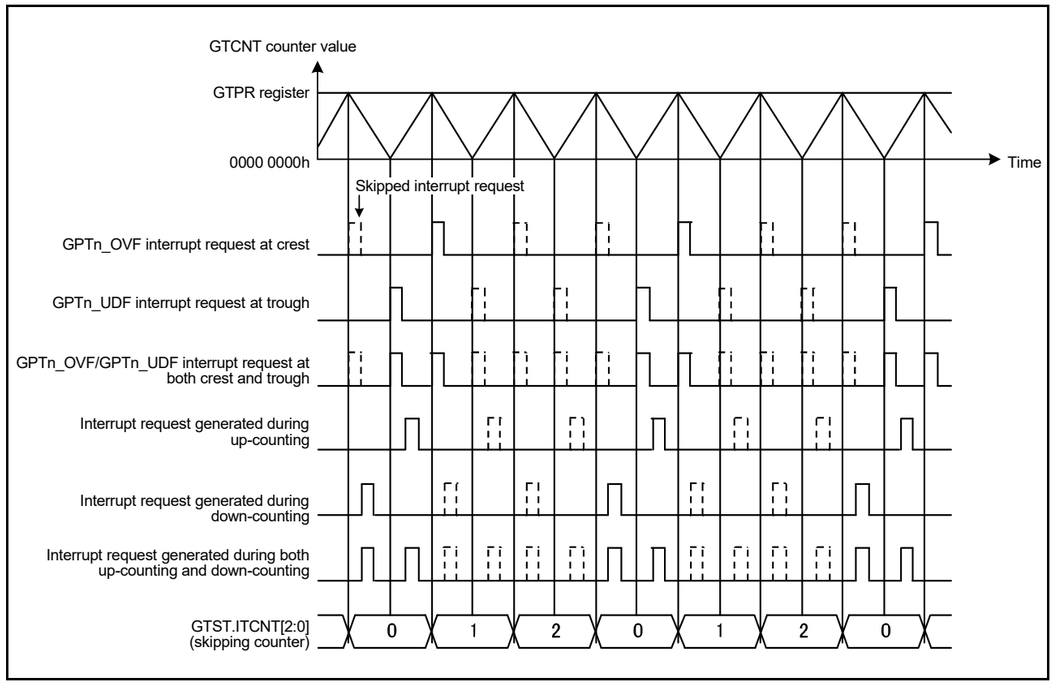


Figure 23.86 Example of interrupt skipping function operation with triangle waves, counting and skipping crests, and skipping count = 2

跳过计数器开始计时。要同时计算波谷和波峰，并在三角波模式下仅在波谷或波峰处生成GPTn_OVFGPTn_UDF中断，您必须设置偶数个跳过。

类似地，在锯齿波模式下，当计数方向改变同时计数和跳过上溢和下溢时，GPTn_OVF中断请求不能仅在上溢或下溢时产生。要在计数方向改变的情况下计算上溢和下溢，并仅在锯齿波模式下在上溢或下溢时生成GPTn_OVFGPTn_UDF中断，您必须首先检查跳过状态。

在更改跳过计数之前，您必须释放跳过计数设置（GTITC.IVTC[1:0]位=00b）。

图23.86至图23.91显示了跳过函数操作的示例。

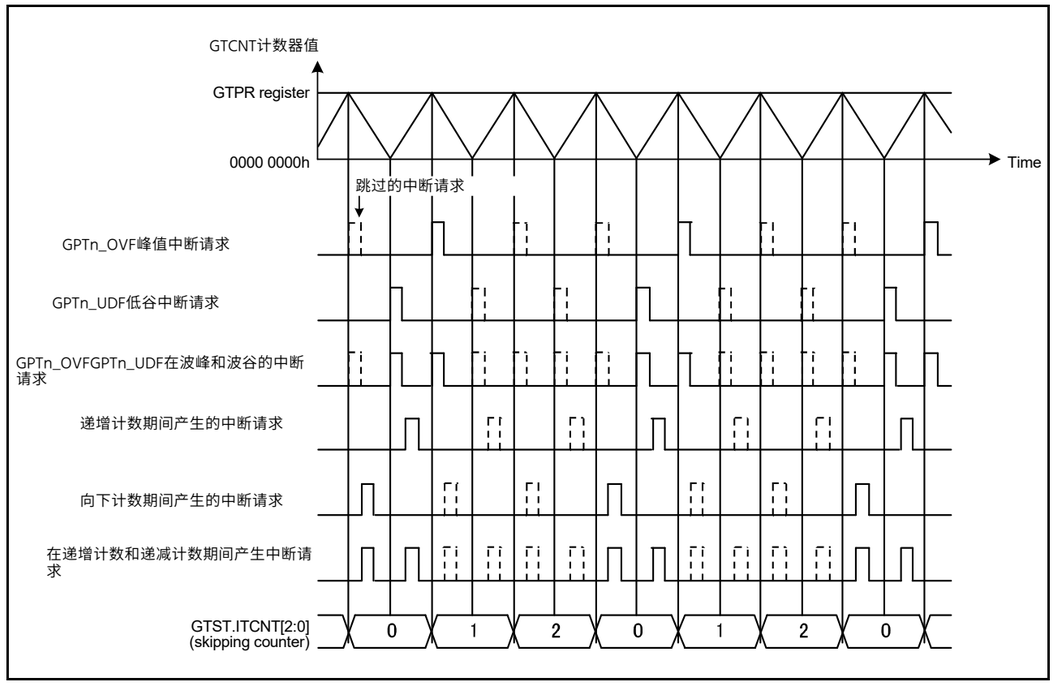


Figure 23.86 使用三角波、计数和跳过波峰以及跳过计数=2的中断跳过函数操作示例

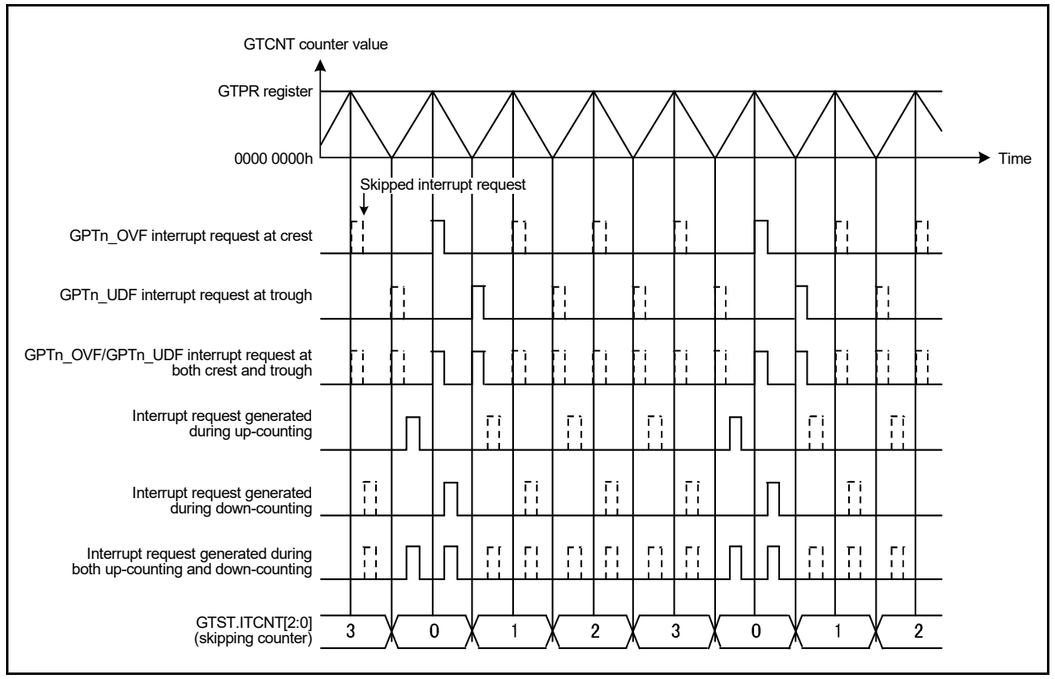


Figure 23.87 Example of interrupt skipping function operation with triangle waves, counting and skipping troughs, and skipping count = 3

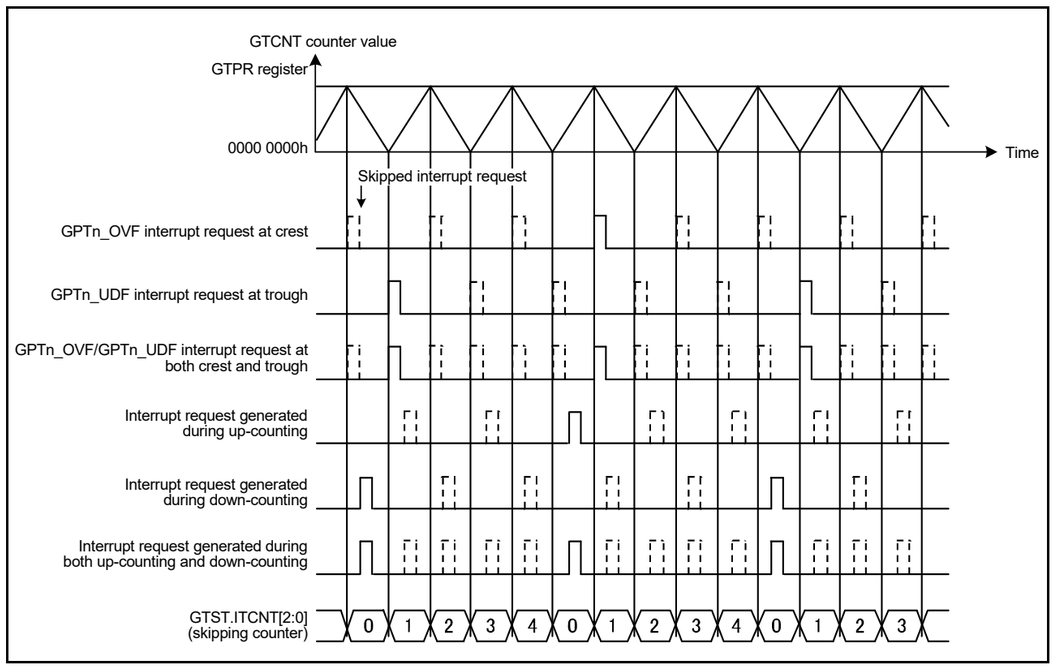


Figure 23.88 Example of interrupt skipping function operation with triangle waves, counting and skipping both troughs and crests, and skipping count = 4

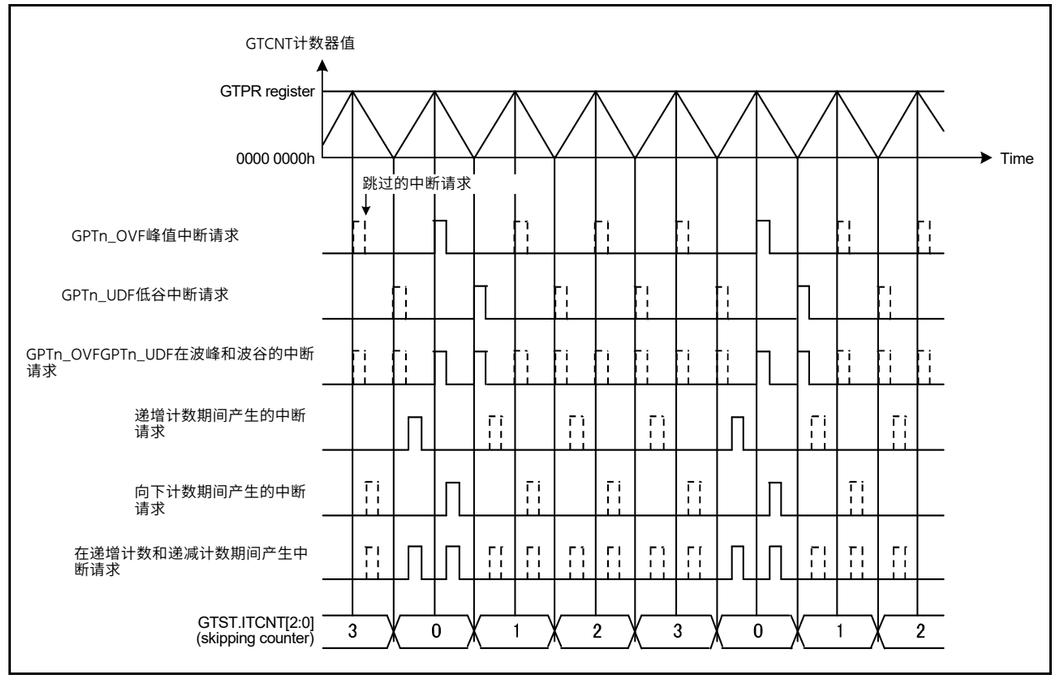


Figure 23.87 带有三角波的中断跳跃函数操作示例，计数和跳跃波谷，跳跃计数=3

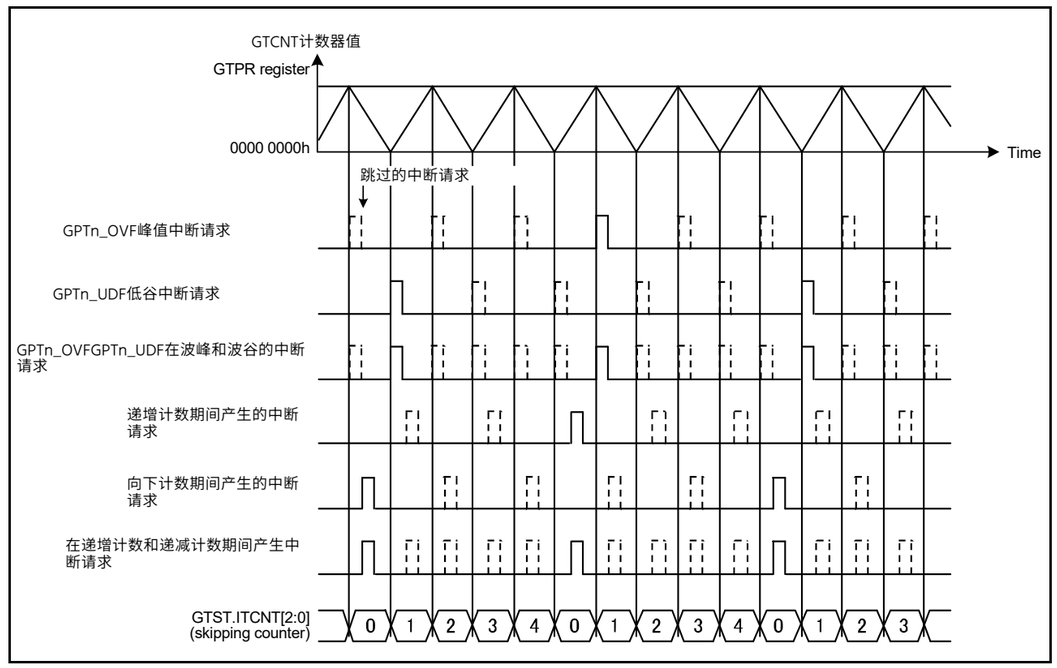


Figure 23.88 使用三角波的中断跳跃函数操作示例，计数和跳跃波谷和波峰，跳跃计数=4

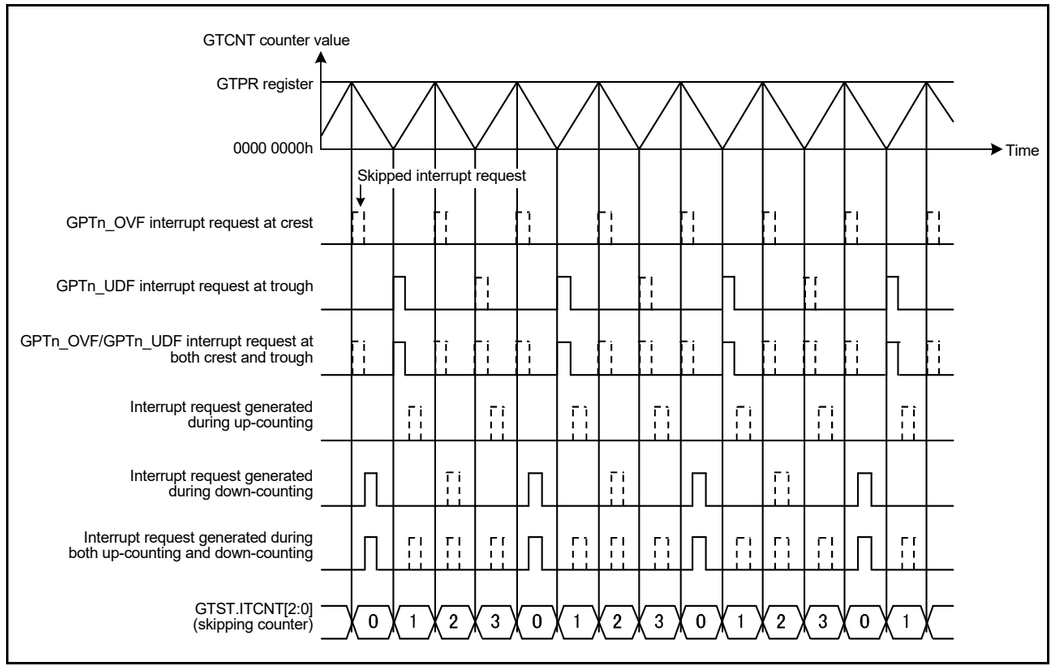


Figure 23.89 Example of interrupt skipping function operation with triangle waves, counting and skipping both troughs and crests, skipping count = 3, and skipping started at up-counting

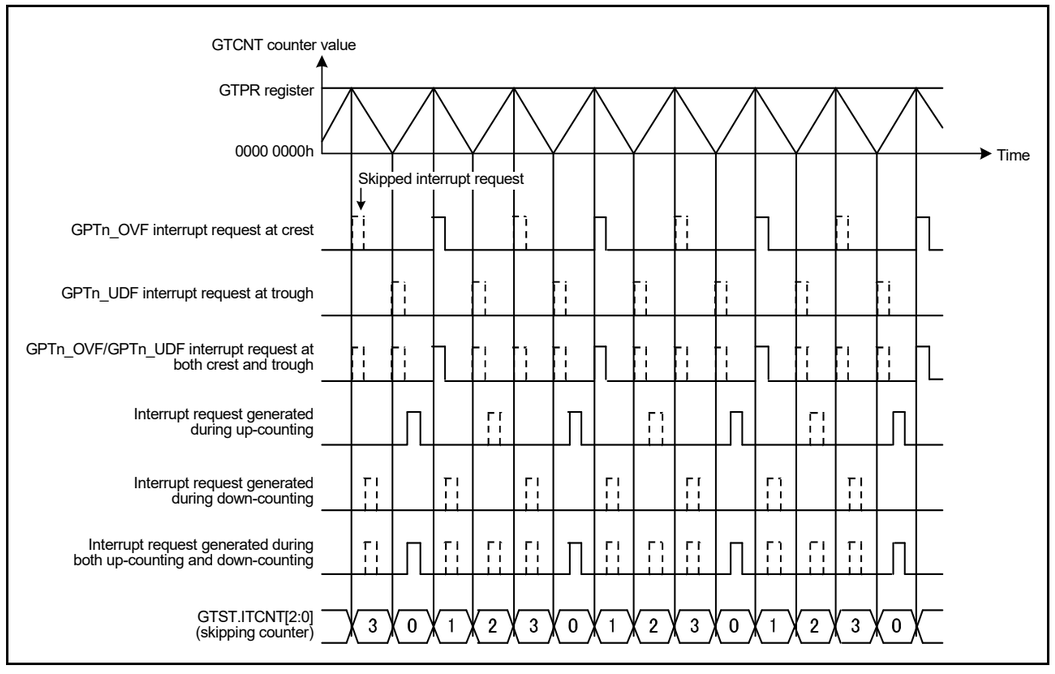


Figure 23.90 Example of interrupt skipping function operation with triangle waves, counting and skipping both troughs and crests, skipping count = 3, and skipping started at down-counting

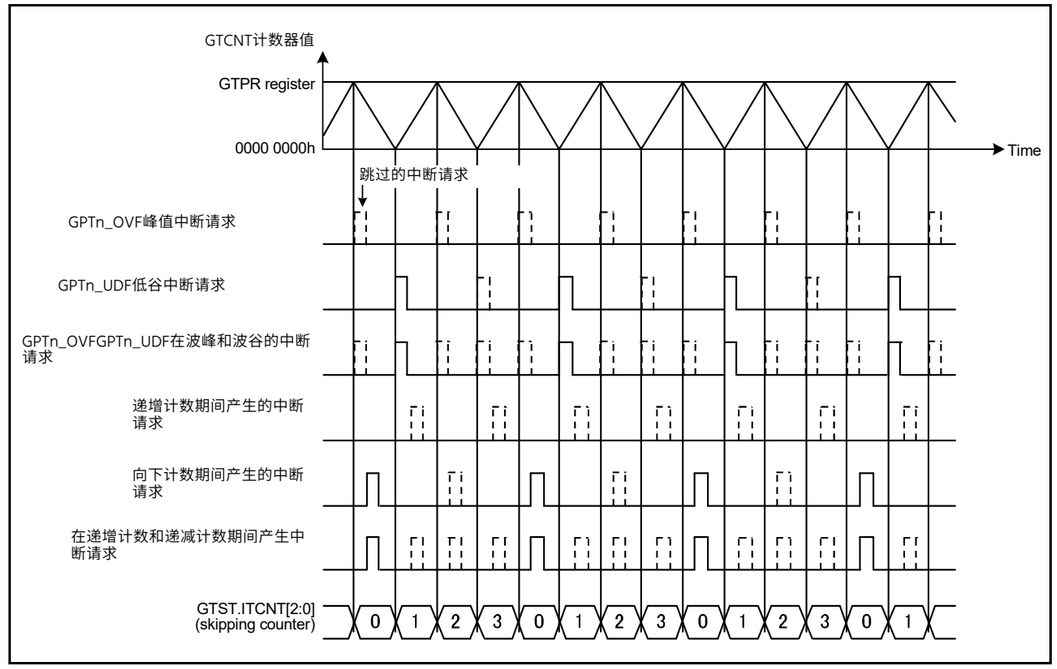


Figure 23.89 使用三角波的中断跳跃函数操作示例，计数和跳跃波谷和波峰，跳跃计数=3，跳跃从向上计数开始

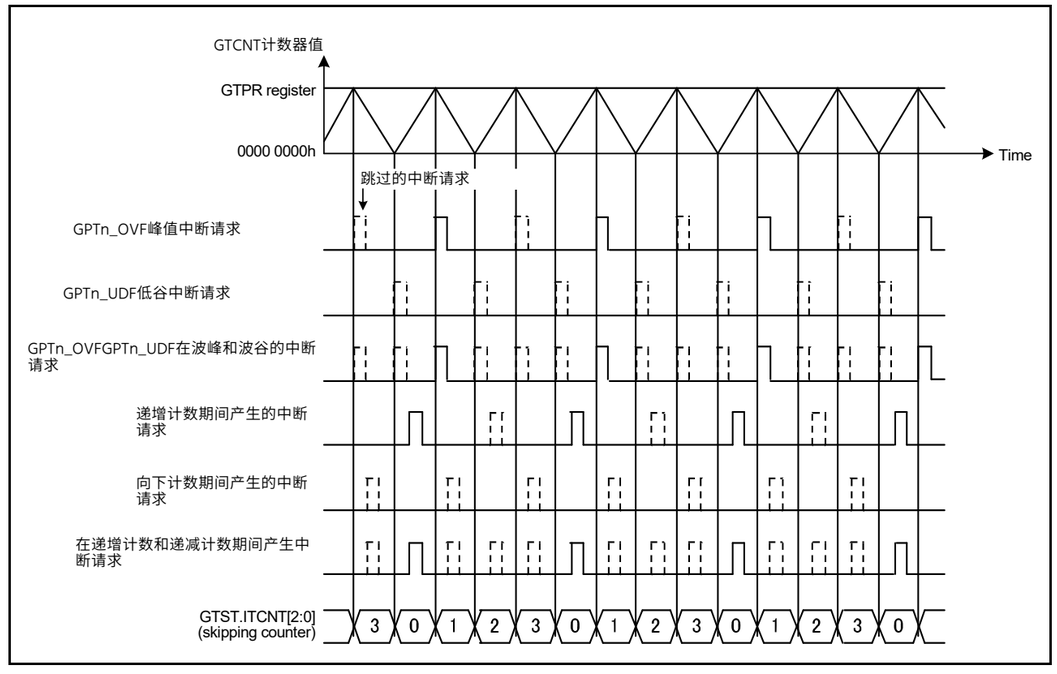


Figure 23.90 使用三角波的中断跳跃函数操作示例，计数和跳跃波谷和波峰，跳跃计数=3，跳跃从向下计数开始

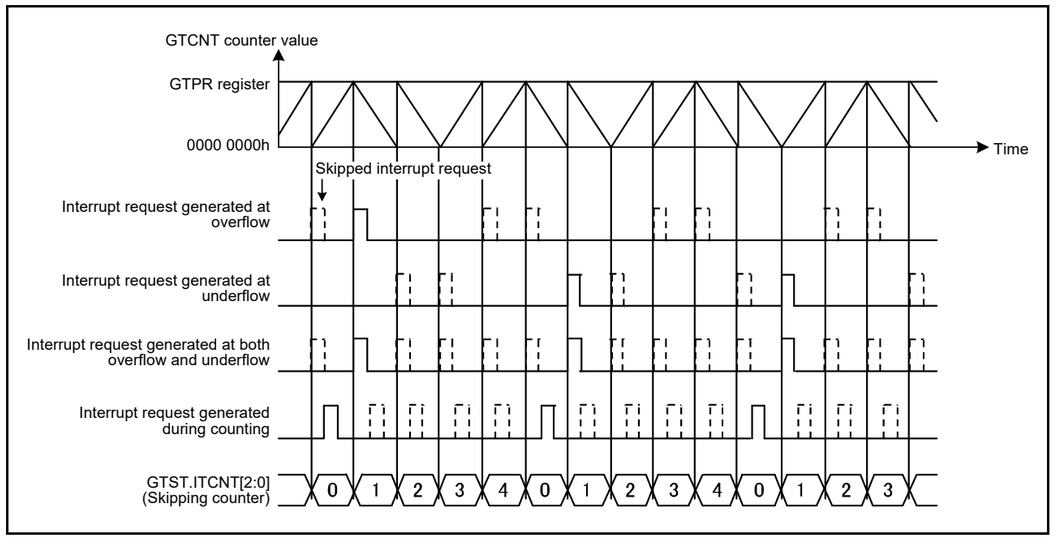


Figure 23.91 Example of interrupt skipping function operation with saw waves, operation with count direction changed, counting and skipping both overflows and underflows, and skipping count = 4

23.5 A/D Converter Start Request

An A/D converter start request can be issued at a compare match between the GTCNT counter and GTADTRA or GTADTRB, and up-counting only, down-counting only, or both up-counting and down-counting can be specified.

In event count operation, A/D converter start requests interrupt cannot be generated. An A/D converter start request does not direct output to the A/D converter module but results in output to ELC as event signals.

GTADTRA and GTADTRB each have two buffer registers. Buffer operation with GTADTRA combined with GTADTBRA and GTADTDBRA, and buffer operation with GTADTRB combined with GTADTBRB and GTADTDBRB can be performed.

Figure 23.92 shows an example of A/D converter start request operation, and Figure 23.93 shows an example setting for A/D converter start request operation.

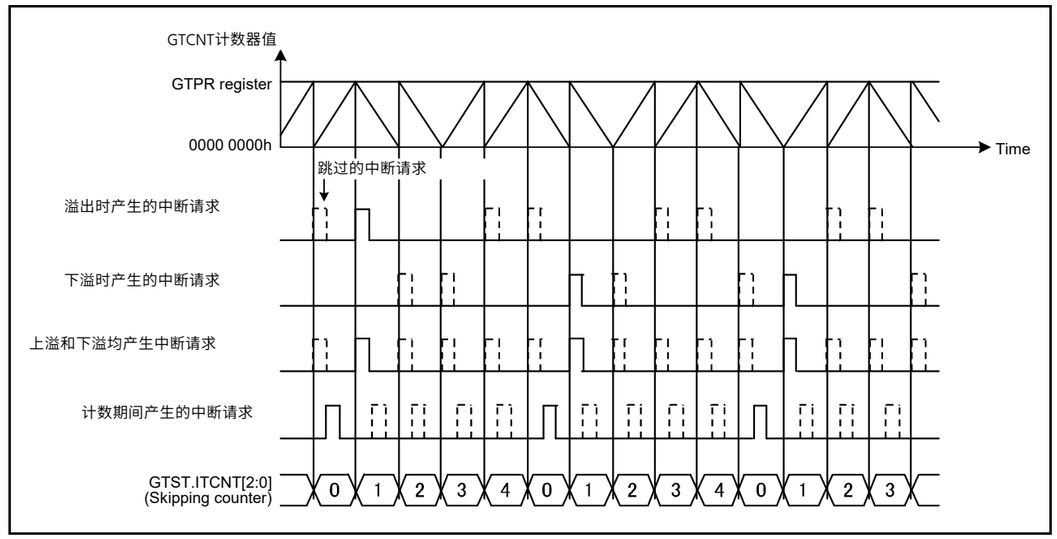


Figure 23.91 使用锯齿波的中断跳过功能操作示例，改变计数方向的操作，计数和跳过上溢和下溢，以及跳过计数=4

23.5 AD转换器启动请求

可以在GTCNT计数器与GTADTRA或GTADTRB之间的比较匹配时发出AD转换器启动请求，并且可以指定仅向上计数、仅向下计数或同时向上计数和向下计数。

在事件计数操作中，不能产生AD转换器启动请求中断。AD转换器启动请求不会直接输出到AD转换器模块，而是导致作为事件信号输出到ELC。

GTADTRA和GTADTRB各有两个缓冲寄存器。与GTADTRA相结合的缓冲操作GTADTBRA和GTADTBRA，以及将GTADTRB与GTADTBRB和可以执行GTADTDRBB。

图23.92显示AD转换器启动请求操作示例，图23.93显示示例设置AD转换器启动请求操作。

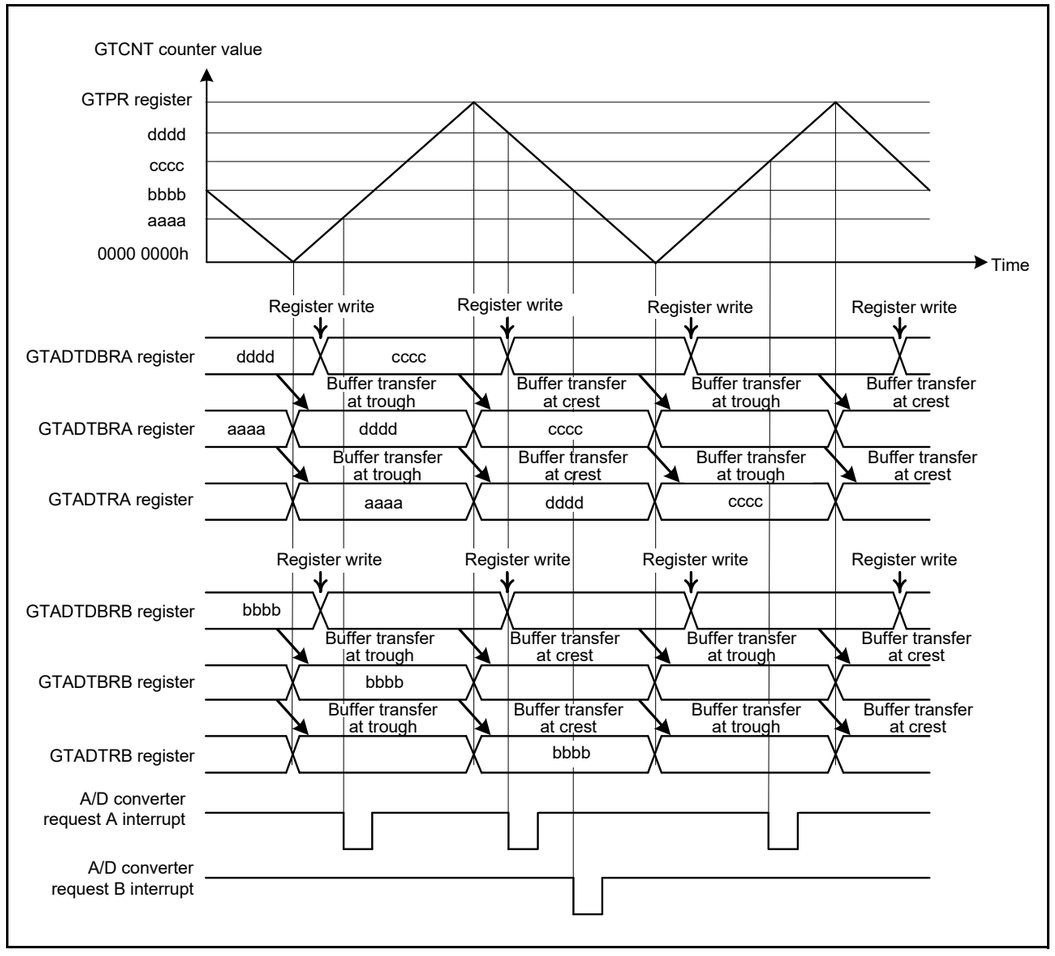


Figure 23.92 **Example of A/D converter start request timing operation with triangle waves, double buffer operation, buffer transfer at both troughs and crests, A/D converter start request interrupt by GTADTRA at both up-counting and down-counting, and A/D converter start request interrupt by GTADTRB at down-counting**

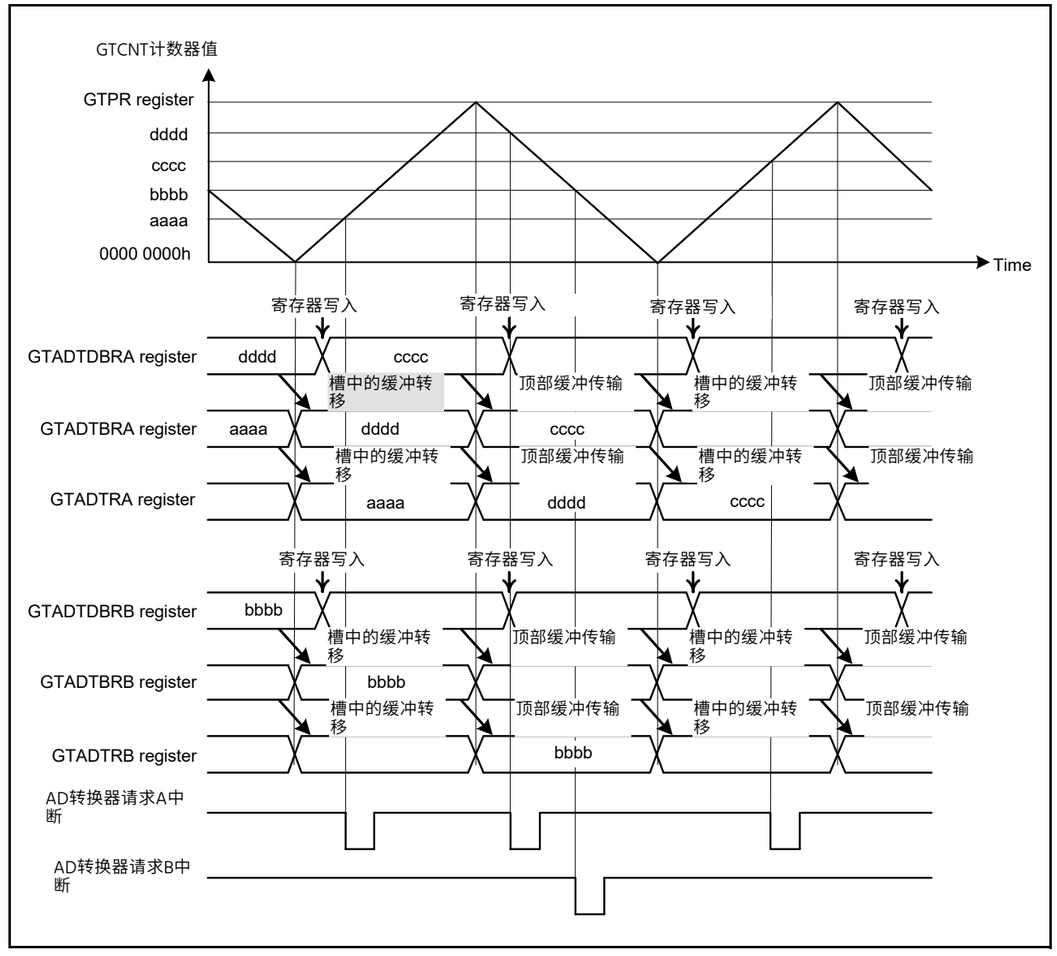


Figure 23.92 **带三角波的AD转换器启动请求时序操作示例、双缓冲操作、波谷和波峰的缓冲传输、递增计数和递减计数时GTADTRA的AD转换器启动请求中断以及AD转换器启动请求中断的示例**

GTADTRB at down-counting

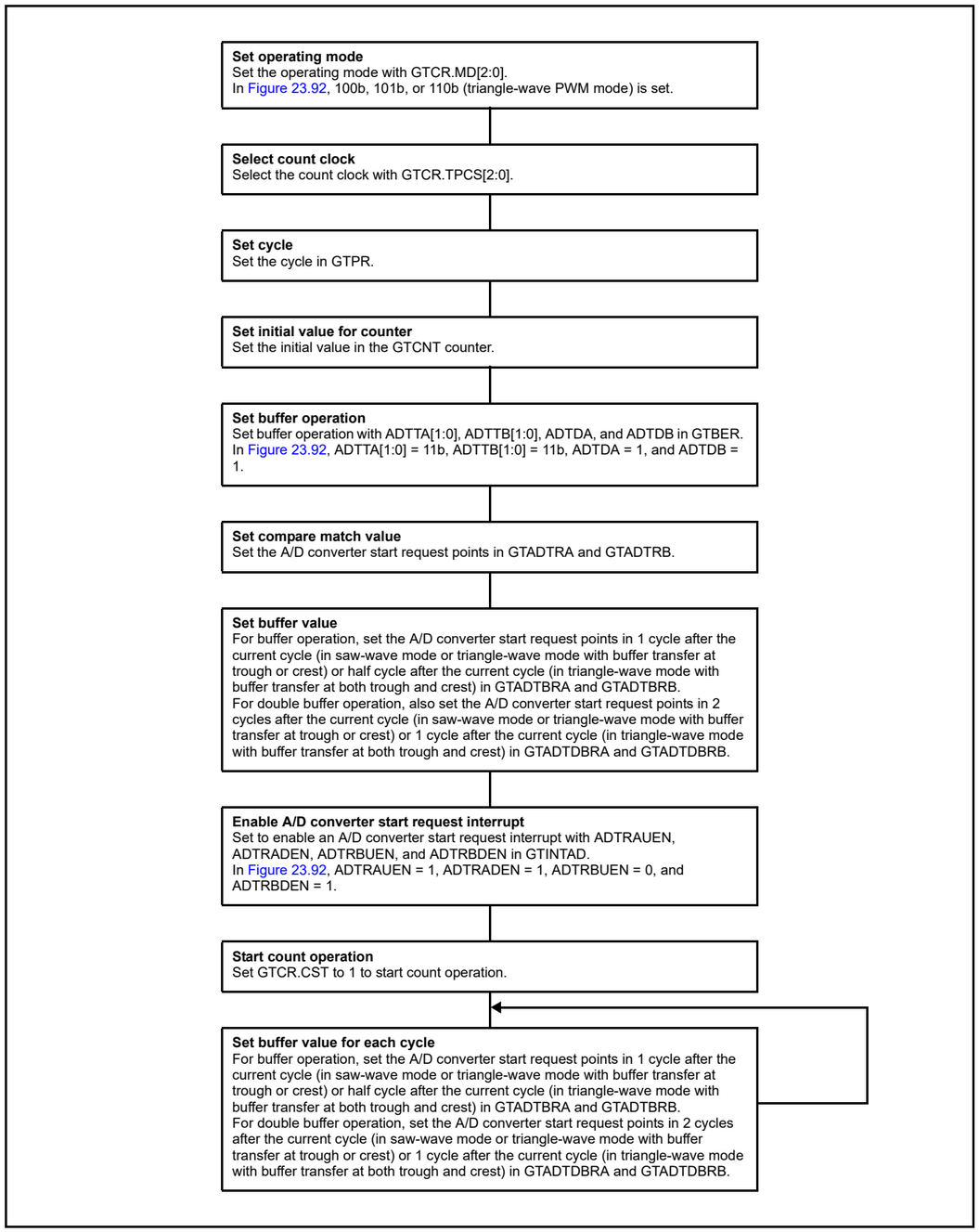


Figure 23.93 Example setting for A/D converter start request timing operation

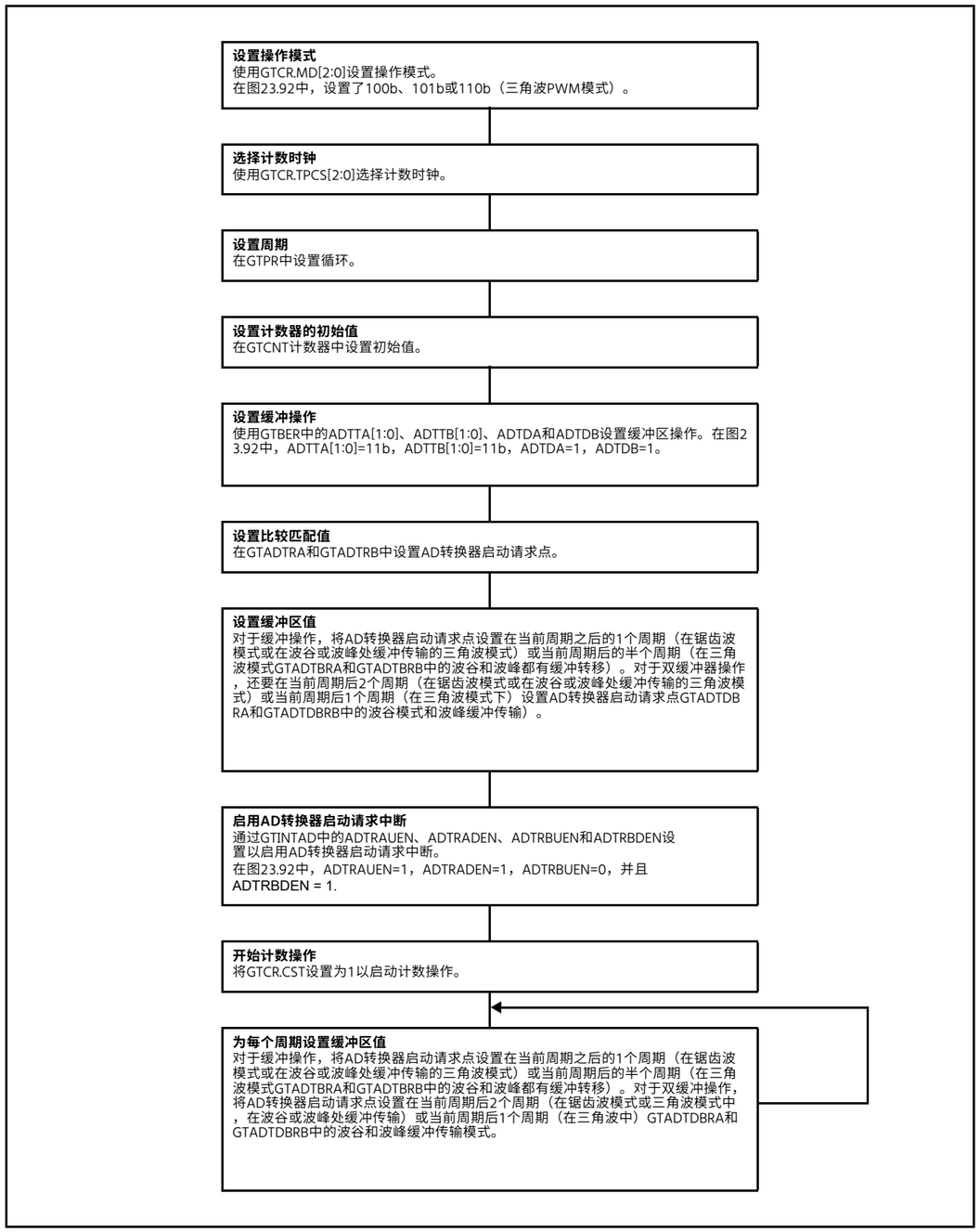


Figure 23.93 AD转换器启动请求时序操作的示例设置

23.6 Operations Linked by the ELC

23.6.1 Event Signal Output to the ELC

The GPT can perform operation linked with another module set in advance when its interrupt request signal is used as an event signal by the ELC.

A/D converter start requests can be enabled and disabled individually with each up-counting and down-counting for both interrupts and events output to ELC by enable bits of the interrupt request.

The GPT has the following ELC event signals:

- Generating of compare match A interrupt (GPTn_CCMPA (n = 0 to 13))
- Generating of compare match B interrupt (GPTn_CCMPB (n = 0 to 13))
- Generating of compare match C interrupt (GPTn_CMPC (n = 0 to 13))
- Generating of compare match D interrupt (GPTn_CMPD (n = 0 to 13))
- Generating of compare match E interrupt (GPTn_CMPE (n = 0 to 13))
- Generating of compare match F interrupt (GPTn_CMPF (n = 0 to 13))
- Generating of overflow interrupt (GPTn_OVF (n = 0 to 13))
- Generating of underflow interrupt (GPTn_UDF (n = 0 to 13))
- A/D converter start request A interrupt (GPTn_ADTRGA (n = 0 to 7))
- A/D converter start request B interrupt (GPTn_ADTRGB (n = 0 to 7)).

23.6.2 Event Signal Inputs from the ELC

The GPT can perform the following operations in response to a maximum of eight events from the ELC:

- Start counting, stop counting, clear counting
- Up-counting, down counting
- Input capture.

See section 23.3, Operation for detail on hardware resources.

23.7 Noise Filter Function

Each pin for use in input capture and Hall sensor input to the GPT is equipped with a noise filter. The noise filter samples input signals at the sampling clock and removes the pulses whose length is less than three sampling cycles.

The noise filter functionality includes enabling and disabling the noise filter for each pin and setting of the sampling clock for each channel.

Figure 23.94 shows the timing of noise filtering.

23.6 由ELC关联的操作

23.6.1 事件信号输出到ELC

当GPT的中断请求信号被ELC用作事件信号时，GPT可以执行与预先设置的另一个模块联动的操作。

D转换器启动请求可以通过中断请求的使能位分别启用和禁用，每次递增和递减中断和事件输出到ELC。

GPT具有以下ELC事件信号：

- 产生比较匹配A中断(GPTn_CCMPA(n=0to13))
- 产生比较匹配B中断(GPTn_CCMPB(n=0to13))
- 产生比较匹配C中断(GPTn_CMPC(n=0to13))
- 产生比较匹配D中断(GPTn_CMPD(n=0to13))
- 产生比较匹配E中断(GPTn_CMPE(n=0to13))
- 产生比较匹配F中断(GPTn_CMPF(n=0to13))
- 产生溢出中断(GPTn_OVF(n=0to13))
- 产生下溢中断(GPTn_UDF(n=0to13))
- AD转换器启动请求A中断(GPTn_ADTRGA(n=0to7))
- AD转换器启动请求B中断(GPTn_ADTRGB(n=0to7))。

23.6.2 来自ELC的事件信号输入

GPT最多可以执行以下操作以响应来自ELC的八个事件：

- 开始计数，停止计数，清除计数
- 递增计数、递减计数
- 输入捕获。

有关硬件资源的详细信息，请参见第23.3节，操作。

23.7 噪音过滤功能

用于GPT的输入捕捉和霍尔传感器输入的每个引脚都配备了噪声滤波器。噪声滤波器以采样时钟对输入信号进行采样，并去除长度小于三个采样周期的脉冲。

噪声过滤器功能包括为每个引脚启用和禁用噪声过滤器以及为每个通道设置采样时钟。

图23.94显示了噪声过滤的时序。

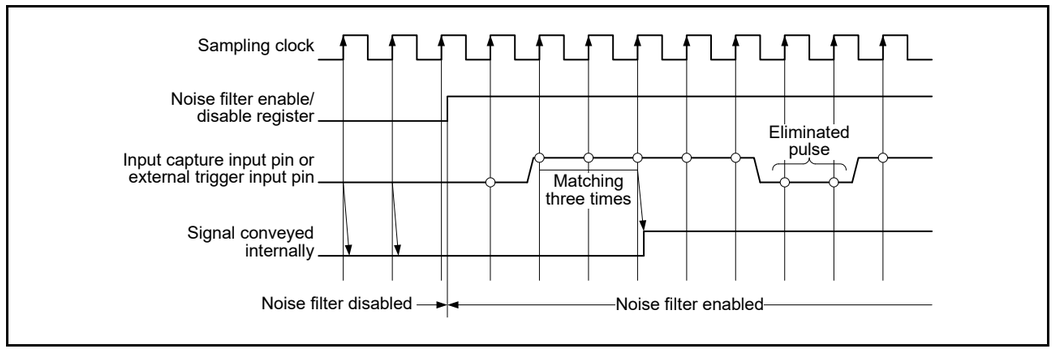


Figure 23.94 Timing of noise filtering

If noise filtering is enabled, the input capture operation or external trigger operation performs on the edges of the noise filtered signal after a delay of a sampling interval × 3 + PCLKD. This is caused by the noise filtering for the input capture input or external trigger operation.

23.8 Protection Function

23.8.1 Write-Protection for Registers

To prevent registers from being accidentally modified, registers can be write-protected in channel units by setting GTWP.WP. Write-protection can be set for the following registers:

GTSSR, GTPSR, GTCSR, GTUPSR, GTDNSR, GTICASR, GTICBSR, GTCR, GTUDDTYC, GTIOR, GTINTAD,GTST, GTBER, GTITC, GTCNT, GTCCRA, GTCCRB, GTCCRC, GTCCRD, GTCCRE, GTCCRF, GTPR, GTPBR, GTPDBR, GTADTRA, GTADTBRA, GTADTDBRA, GTADTRB, GTADTBRB, GTADTDBRB, GTDTCR, GTDVU, GTDVD, GTDBU, GTDBD, GTSOS, GTSOTR.

23.8.2 Disabling of Buffer Operation

If the timing of buffer register write is delayed in relative to the timing for the buffer transfer, buffer operation can be suspended with the GTBER.BD setting. Buffer transfer can be temporarily disabled even when a buffer transfer condition is generated during a buffer register write. This can be done by setting the associated GTBER.BD bit to 1 (buffer operation disabled) before a buffer register write and clearing the bit to 0 (buffer operation enabled) after completion of writing to all buffer registers. Figure 23.95 shows an example of operation for disabling buffer operation.

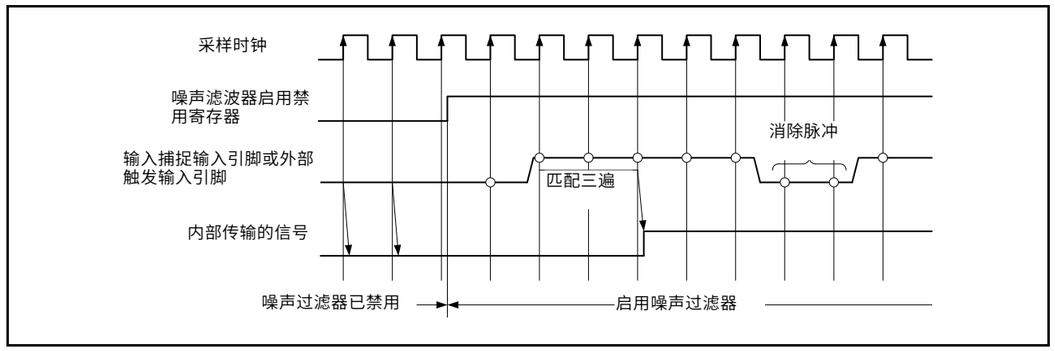


Figure 23.94 噪声过滤的时序

如果噪声过滤使能，输入捕捉操作或外部触发操作在经过一个采样间隔×3+PCLKD的延迟后在噪声过滤信号的边沿上执行。这是由输入捕捉输入或外部触发操作的噪声过滤引起的。

23.8 保护功能

23.8.1 寄存器的写保护

为了防止寄存器被意外修改，可以通过设置以通道为单位对寄存器进行写保护GTWP.WP。可以为以下寄存器设置写保护：

GTSSR, GTPSR, GTCSR, GTUPSR, GTDNSR, GTICASR, GTICBSR, GTCR, GTUDDTYC, GTIOR, GTINTAD,GTST, GTBER, GTITC, GTCNT, GTCCRA, GTCCRB, GTCCRC, GTCCRD, GTCCRE, GTCCRF, GTPR, GTPBR, GTPDBR, GTADTRA, GTADTBRA, GTADTDBRA, GTADTRB, GTADTBRB, GTADTDBRB, GTDTCR, GTDVU, GTDVD, GTDBU, GTDBD, GTSOS, GTSOTR.

23.8.2 禁用缓冲区操作

如果缓冲寄存器写入的时序相对于缓冲传输的时序延迟，则可以通过GTBER.BD设置暂停缓冲操作。即使在缓冲寄存器写入期间产生了缓冲传送条件，也可以暂时禁用缓冲传送。这可以通过在写入缓冲寄存器之前将相关的GTBER.BD位设置为1（禁用缓冲操作）并在完成对所有缓冲寄存器的写入后将该位清除为0（启用缓冲操作）来完成。图23.95显示了禁用缓冲区操作的操作示例。

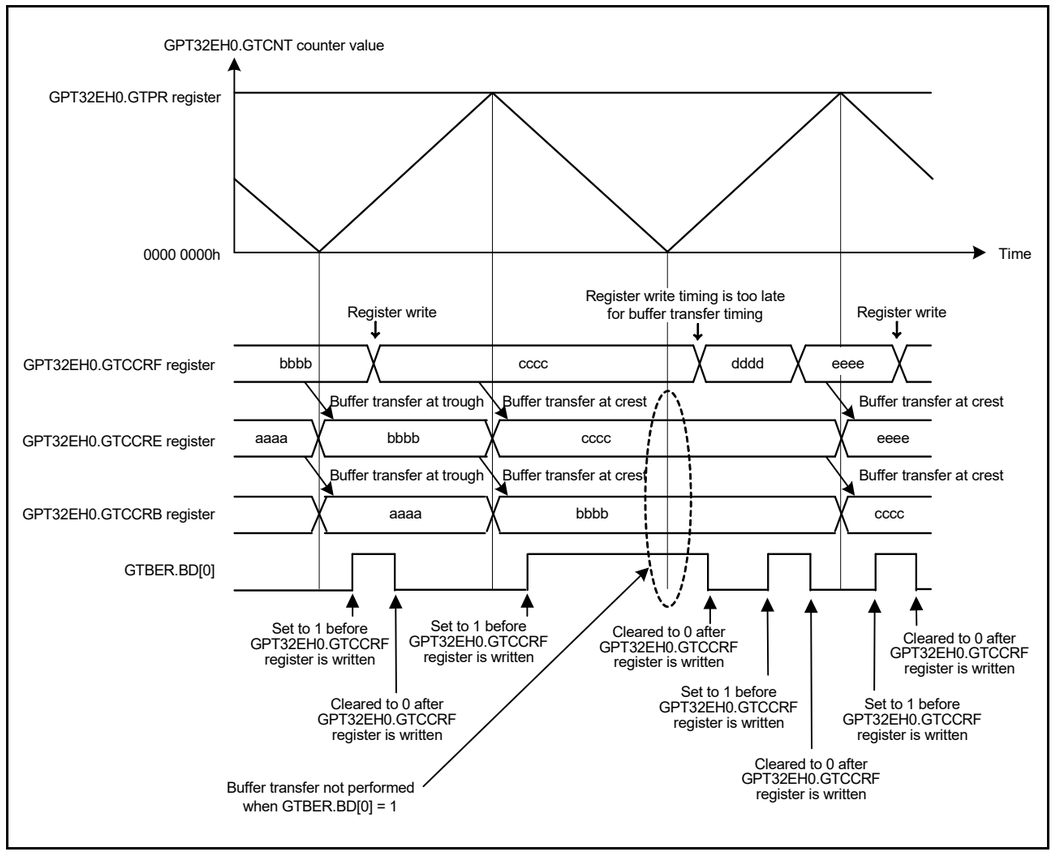


Figure 23.95 Example of operation for disabling buffer operation with triangle waves, double buffer operation, and buffer transfer at both troughs and crests

23.8.3 GTIOC Pin Output Negate Control

For protection from system failure, the output disable control that changes the GTIOC pin output value forcibly is provided for GTIOC pin output by the request of output disable from POEG.

When dead time error occurs or the GTIOCA pin output value is the same as the GTIOCB pin output value, output protection is required. The GPT detects this condition and generates output disable requests to POEG based on the settings in the output disable request permission bits, such as GTINTAD.GRPDTE, GTINTAD.GRPABH, and GTINTAD.GRPABL. After the POEG receives output disable requests from each channel and calculates external input using an OR operation, the POEG generates output disable requests to GPT.

One output disable signal (representing the shared output disable request signal of the GTIOCA pin and the GTIOCB pin) out of four output disable requests generated by the POEG is selected by setting GTINTAD.GRP[1:0]. The status of the selected disable output request is monitored by reading the GTST.ODF bit. The output level during output disable is based on the GTIOR.OADF[1:0] setting for the GTIOCA pin and the GTIOR.OBDF[1:0] setting for the GTIOCB pin.

The change to the output disable state is performed asynchronously by generating the output disable request from the POEG. The release of the output disable state is performed at end of cycle by terminating the output disable request. The timing of release of the output disable state is a minimum of 3 PCLKD cycles after terminating the output disable request. To perform output disable control reliably, allow at least 4 PCLKD cycles after generating the output disable request (by clearing the output disable request flag in POEG) until the output disable request is terminated.

When event count is performed or when the output disable state is to be released immediately without waiting for an end

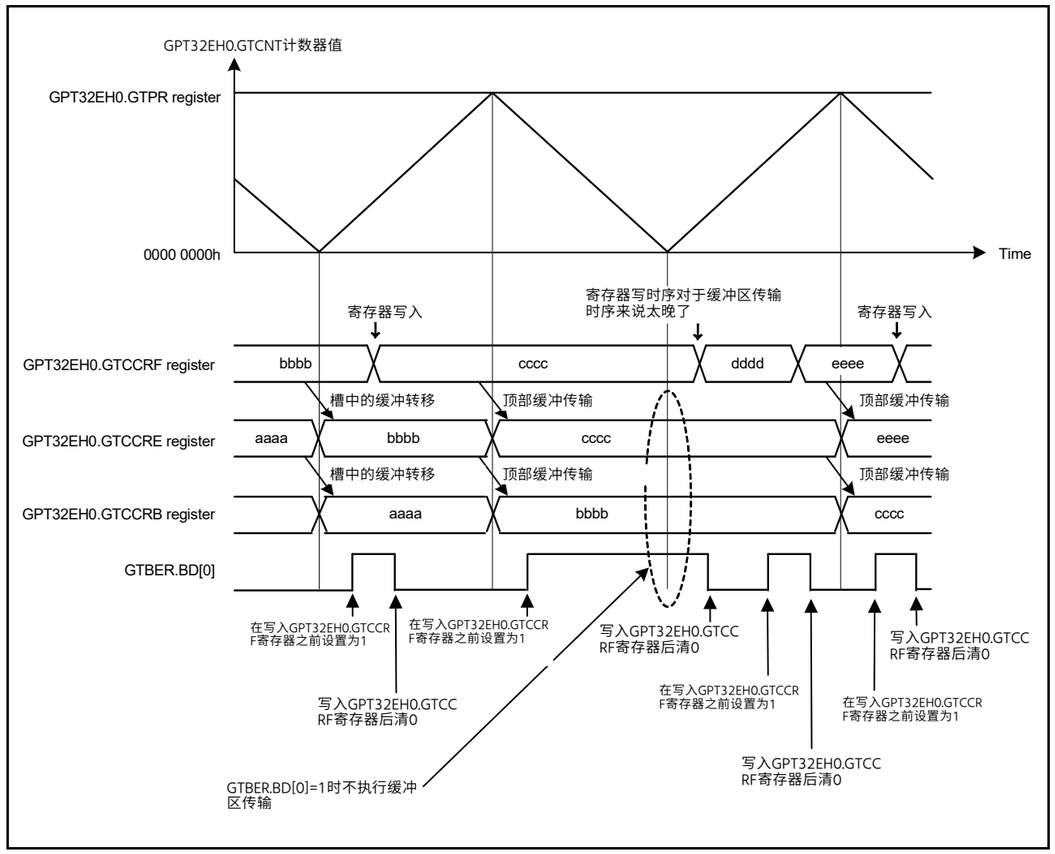


Figure 23.95 三角波缓冲操作、双缓冲操作、波谷和波峰缓冲转移的禁用操作示例

23.8.3 GTIOC引脚输出负控制

为防止系统故障，根据POEG的输出禁用请求，为GTIOC引脚输出提供强制改变GTIOC引脚输出值的输出禁用控制。

当发生死区错误或GTIOCA引脚输出值与GTIOCB引脚输出值相同时，需要输出保护。GPT检测到这种情况并根据输出禁用请求权限位中的设置（例如GTINTAD.GRPDTE、GTINTAD.GRPABH和GTINTAD.GRPABL）向POEG生成输出禁用请求。在POEG接收到来自每个通道的输出禁用请求并使用OR运算计算外部输入后，POEG向GPT生成输出禁用请求。

通过设置GTINTAD.GRP[1:0]，从POEG产生的四个输出禁止请求中选择一个输出禁止信号（代表GTIOCA引脚和GTIOCB引脚的共享输出禁止请求信号）。通过读取GTST.ODF位来监控所选禁用输出请求的状态。输出禁用期间的输出电平基于GTIOCA引脚的GTIOR.OADF[1:0]设置和GTIOCB引脚的GTIOR.OBDF[1:0]设置。

对输出禁用状态的更改是通过从
POEG。通过终止输出禁用请求，在循环结束时执行输出禁用状态的释放。输出禁用状态的释放时间是在终止输出禁用请求后至少3个PCLKD周期。为了可靠地执行输出禁用控制，在生成输出禁用请求后（通过清除POEG中的输出禁用请求标志）至少允许4个PCLKD周期，直到输出禁用请求终止。

执行事件计数或不等待结束而立即释放输出禁用状态时

of cycle, GTIOR.OADF[1:0] must be set to 00b (for GTIOCA pin) or GTIOR.OBDF[1:0] must be set to 00b (for GTIOCB pin).

Figure 23.96 shows an example of the GTIOC pin output disable control operation.

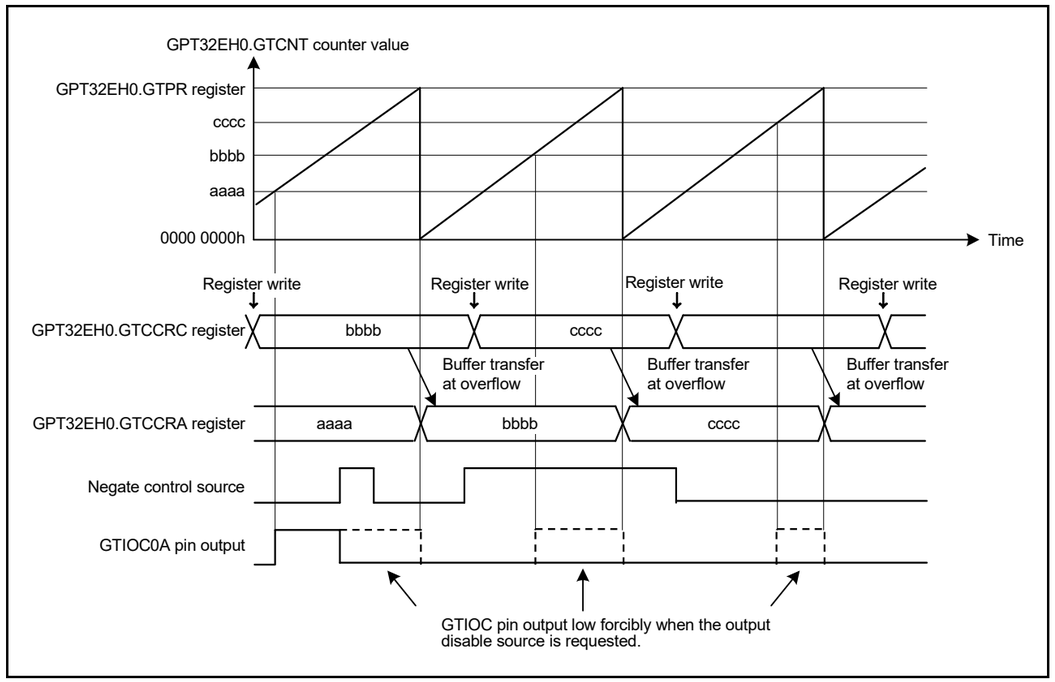


Figure 23.96 Example of GTIOC pin output disable control operation with saw-wave up-counting, buffer operation, active level 1, high output at GTCCRA compare match, low output at cycle end, and low output at output disable

23.8.4 Output Protection Function for GTIOC Pin Output

In preparation for incorrect settings of the GTCCRA register (settings outside the range of 0 < GTCCRA < GTPR), the output protection function for the GTIOC pin output (disabling function) is activated when the automatic dead time setting (GTDTCR.TDE = 1) is made in triangle-wave mode. The status of the output protection function can be read from GTSOS.SOS[1:0].

Figure 23.97 shows the output protection function state transition.

周期，GTIOR.OADF[1:0]必须设置为00b（对于GTIOCA引脚）或GTIOR.OBDF[1:0]必须设置为00b（对于GTIOCB引脚）。

图23.96显示了GTIOC引脚输出禁用控制操作的示例。

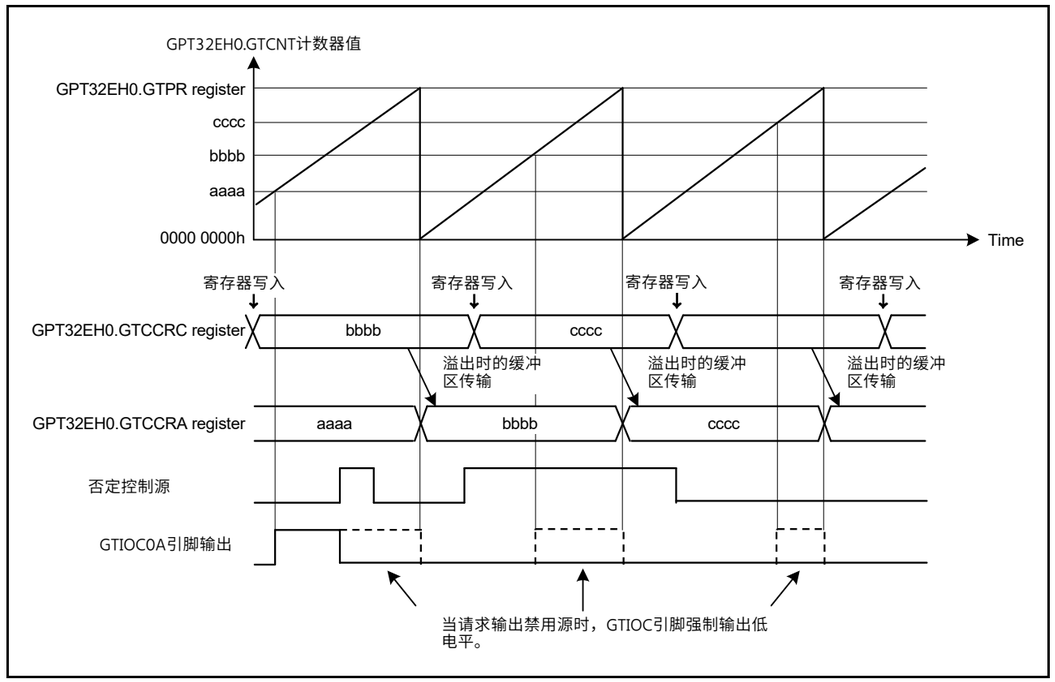


Figure 23.96 GTIOC引脚输出禁用控制操作示例，锯波递增计数、缓冲器操作、有效电平1、GTCCRA比较匹配时的高输出、周期结束时的低输出和输出禁用时的低输出

23.8.4 GTIOC引脚输出的输出保护功能

为防止GTCCRA寄存器的错误设置（设置超出0<GTCCRA<GTPR的范围），当自动死区时间设置(GTDTCR.TDE=1)时，将激活GTIOC引脚输出的输出保护功能（禁用功能）是在三角波模式下制作的。输出保护功能的状态可以从GTSOS.SOS[1:0]中读取。

图23.97显示了输出保护功能状态转换。

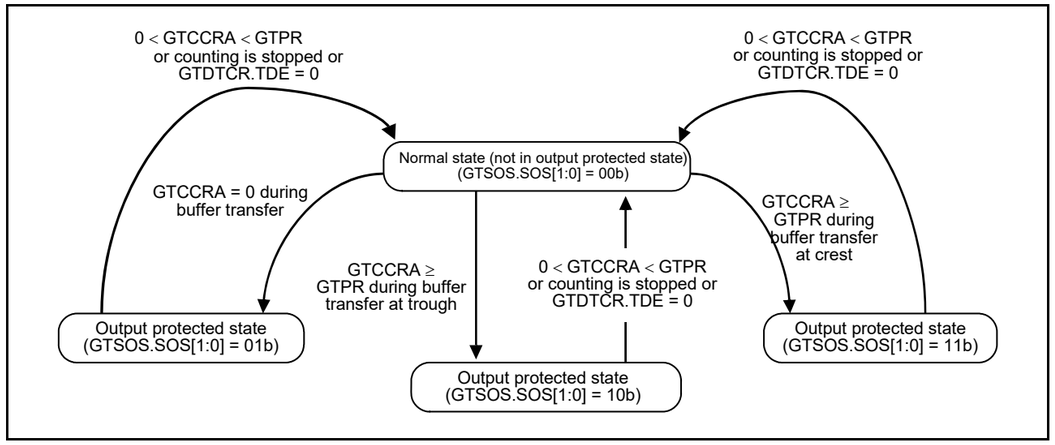
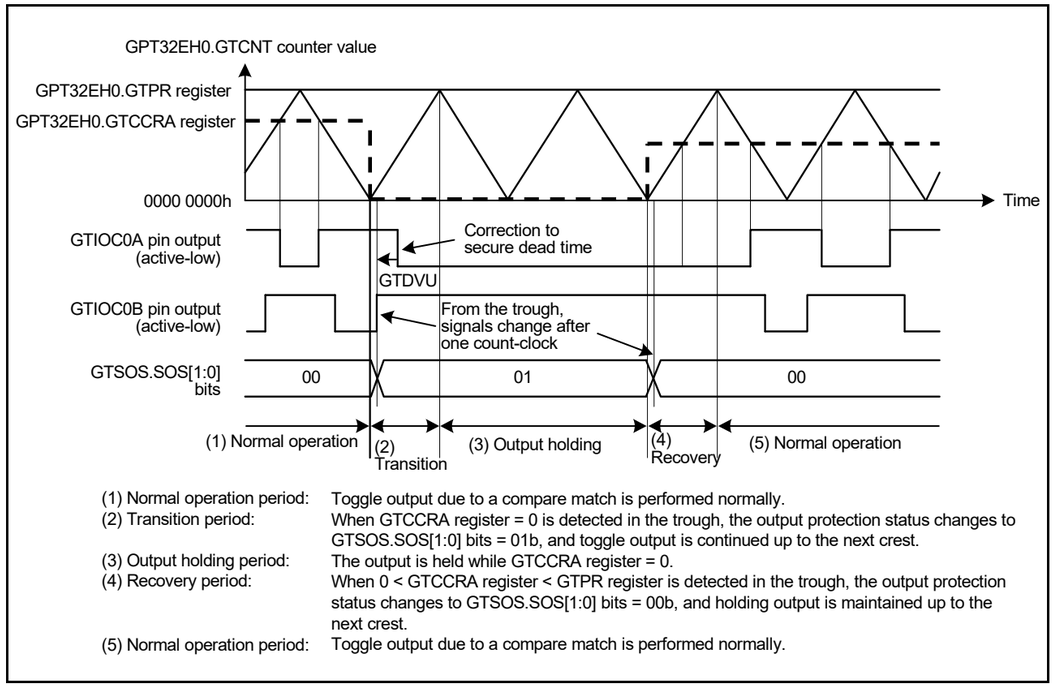


Figure 23.97 Output protection function

23.8.4.1 Output protection function when the GTCCRA register is set to 0 during buffer transfer

Figure 23.98 and Figure 23.99 show examples of output protection function operation when the GTCCRA register is set to 0 during buffer transfer at troughs, and Figure 23.100 and Figure 23.101 show examples when the GTCCRA register is set to 0 during buffer transfer at crests.



(1) Normal operation period: Toggle output due to a compare match is performed normally.
(2) Transition period: When GTCCRA register = 0 is detected in the trough, the output protection status changes to GTSOS.SOS[1:0] bits = 01b, and toggle output is continued up to the next crest.
(3) Output holding period: The output is held while GTCCRA register = 0.
(4) Recovery period: When 0 < GTCCRA register < GTPR register is detected in the trough, the output protection status changes to GTSOS.SOS[1:0] bits = 00b, and holding output is maintained up to the next crest.
(5) Normal operation period: Toggle output due to a compare match is performed normally.

Figure 23.98 Example of output protection operation when GTCCRA is set to 0 during buffer transfer at troughs, with 0 < GTCCRA < GTPR restored during buffer transfer at troughs, and active-low

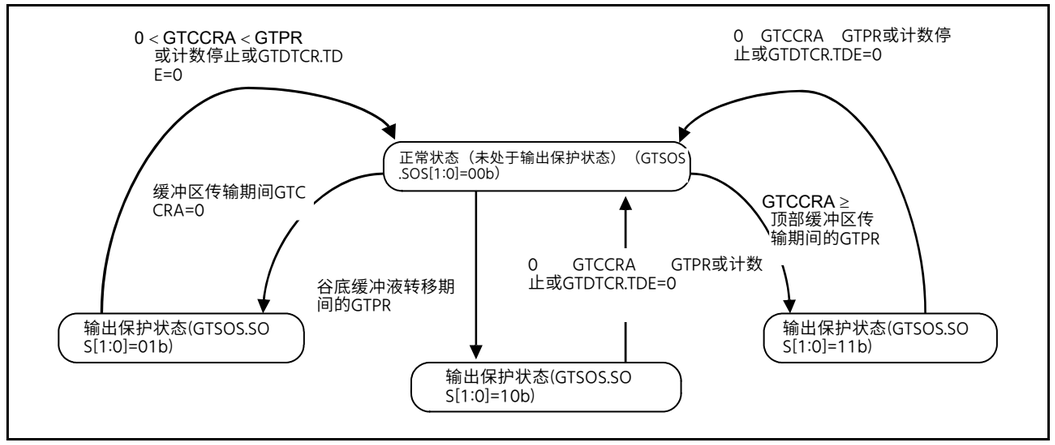
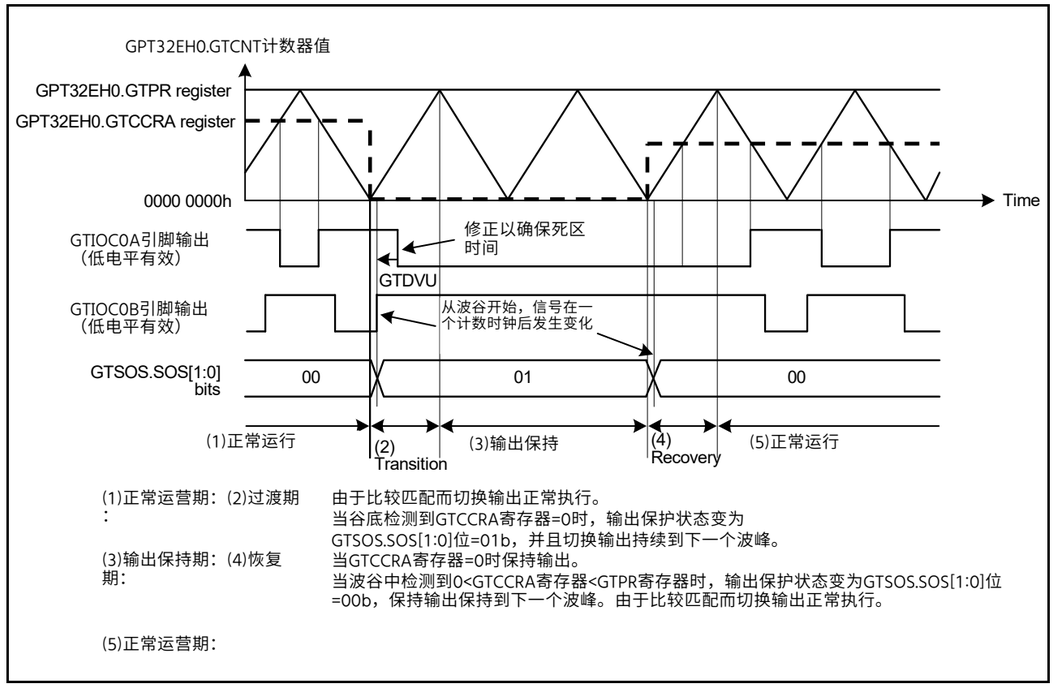


Figure 23.97 输出保护功能

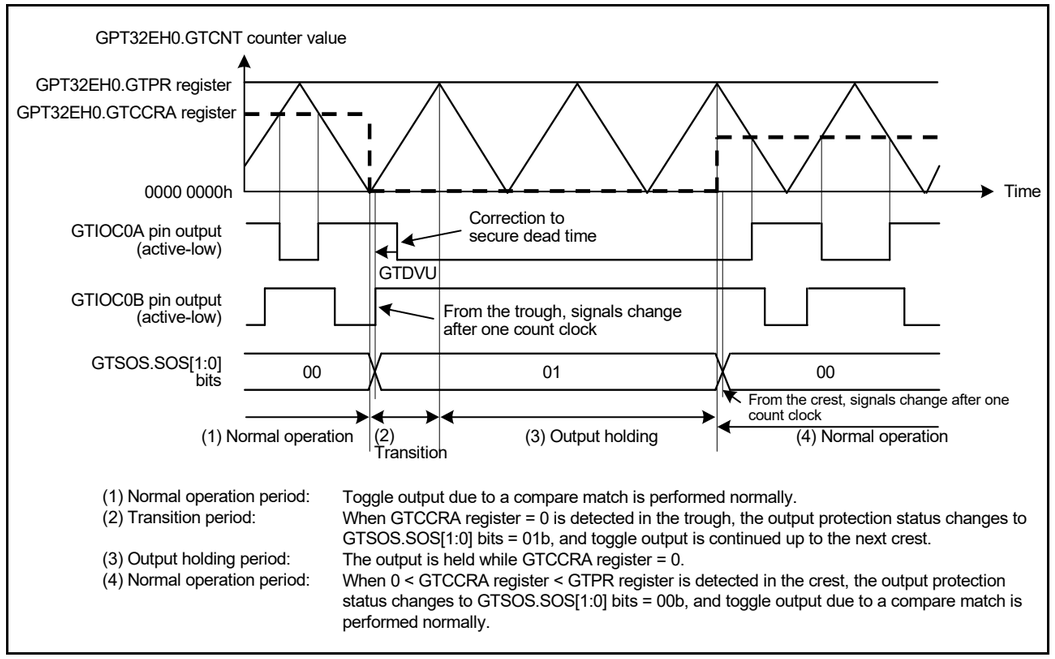
23.8.4.1 缓冲区传输期间GTCCRA寄存器设置为0时的输出保护功能

图23.98和图23.99显示了在波谷缓冲传输期间GTCCRA寄存器设置为0时的输出保护功能操作示例，图23.100和图23.101显示了在波峰缓冲传输期间GTCCRA寄存器设置为0的示例。



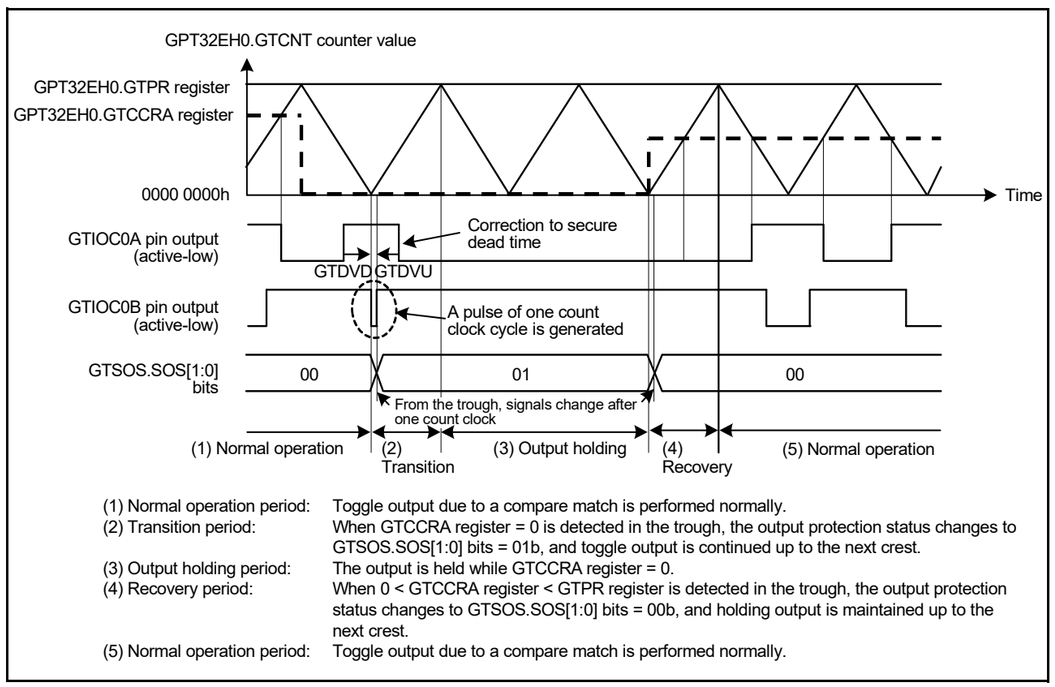
(1)正常运营期：(2)过渡期：由于比较匹配而切换输出正常执行。
当谷底检测到GTCCRA寄存器=0时，输出保护状态变为GTSOS.SOS[1:0]位=01b，并且切换输出持续到下一个波峰。
(3)输出保持期：(4)恢复期：当GTCCRA寄存器=0时保持输出。
当波谷中检测到0<GTCCRA寄存器<GTPR寄存器时，输出保护状态变为GTSOS.SOS[1:0]位=00b，保持输出保持到下一个波峰。由于比较匹配而切换输出正常执行。
(5)正常运营期：

Figure 23.98 输出保护操作示例，当GTCCRA在谷底缓冲区传输期间设置为0，0<GTCCRA<GTPR在谷底缓冲区传输期间恢复，低电平有效



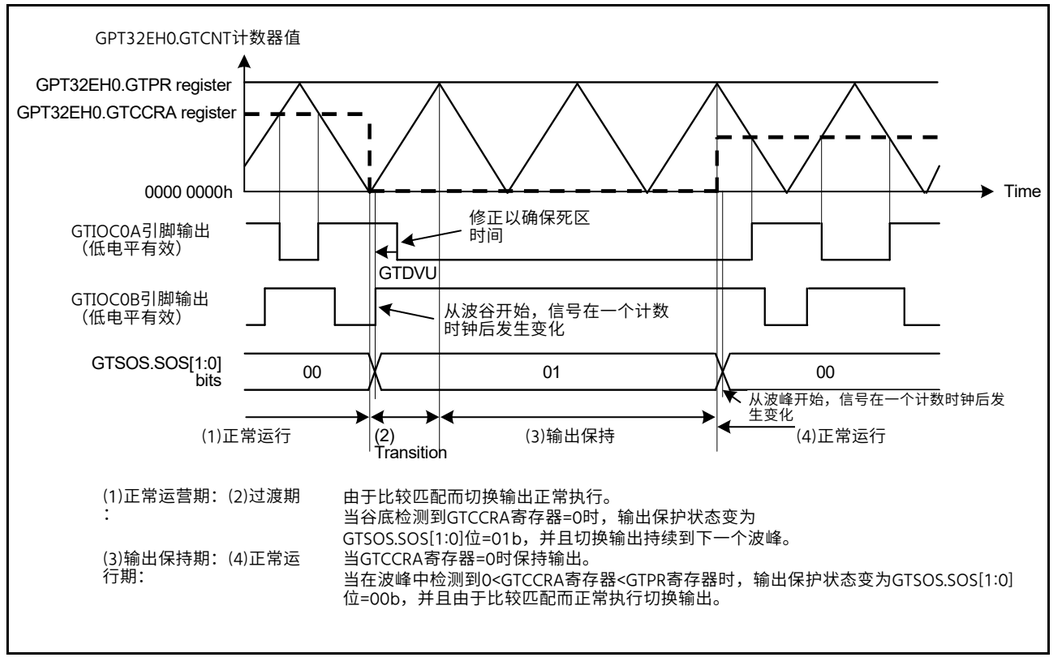
(1) Normal operation period: Toggle output due to a compare match is performed normally.
(2) Transition period: When GTCCRA register = 0 is detected in the trough, the output protection status changes to GTSOS.SOS[1:0] bits = 01b, and toggle output is continued up to the next crest.
(3) Output holding period: The output is held while GTCCRA register = 0.
(4) Normal operation period: When 0 < GTCCRA register < GTPR register is detected in the crest, the output protection status changes to GTSOS.SOS[1:0] bits = 00b, and toggle output due to a compare match is performed normally.

Figure 23.99 Example of output protection operation when GTCCRA is set to 0 during buffer transfer at troughs, with 0 < GTCCRA < GTPR restored during buffer transfer at crests, and active-low



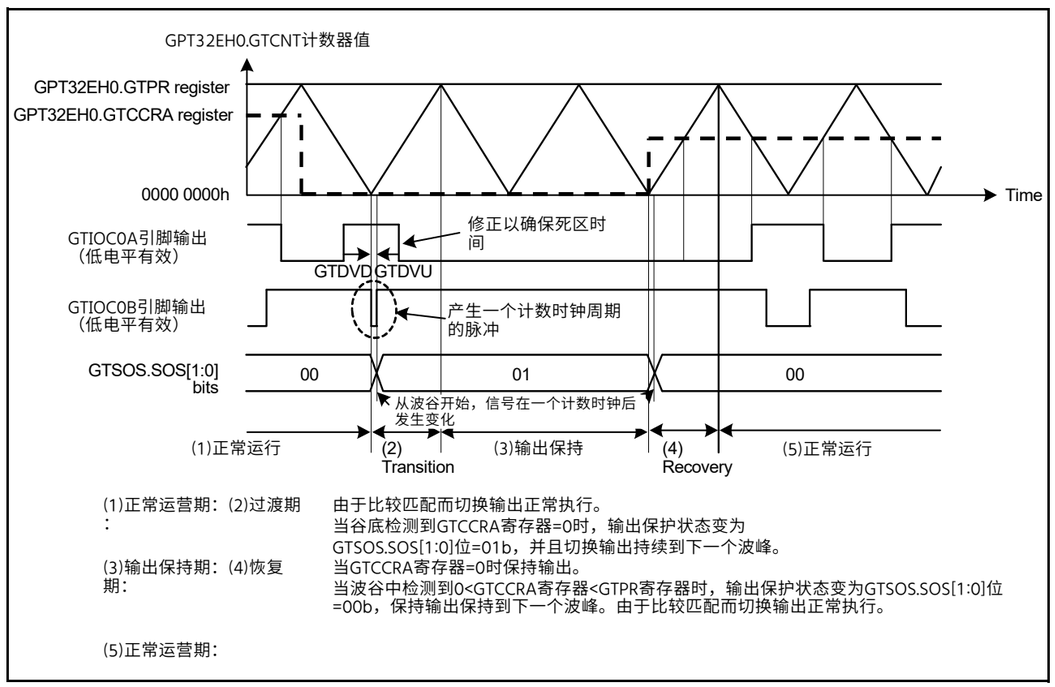
(1) Normal operation period: Toggle output due to a compare match is performed normally.
(2) Transition period: When GTCCRA register = 0 is detected in the trough, the output protection status changes to GTSOS.SOS[1:0] bits = 01b, and toggle output is continued up to the next crest.
(3) Output holding period: The output is held while GTCCRA register = 0.
(4) Recovery period: When 0 < GTCCRA register < GTPR register is detected in the trough, the output protection status changes to GTSOS.SOS[1:0] bits = 00b, and holding output is maintained up to the next crest.
(5) Normal operation period: Toggle output due to a compare match is performed normally.

Figure 23.100 Example of output protection operation when GTCCRA is set to 0 during buffer transfer at crests, with 0 < GTCCRA < GTPR restored during buffer transfer at troughs, and active-low



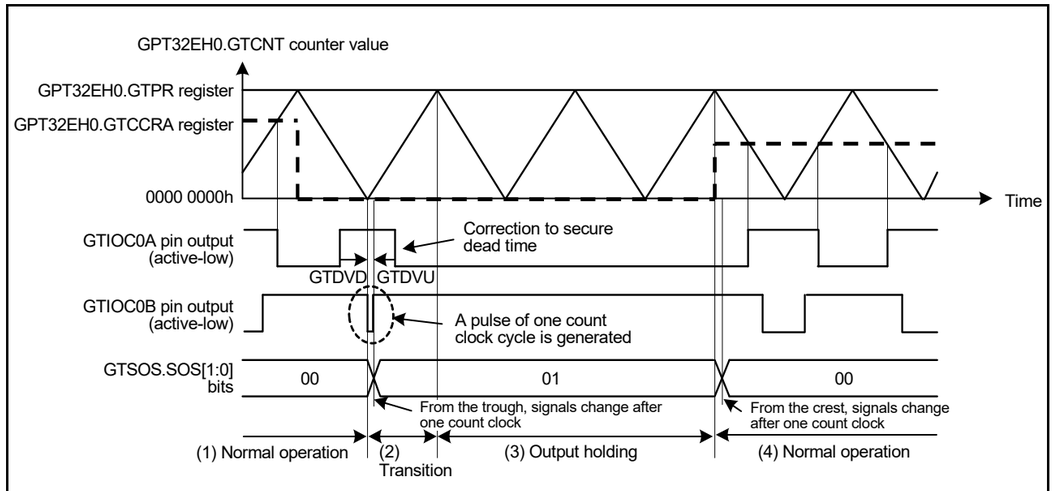
(1)正常运营期：(2)过渡期：由于比较匹配而切换输出正常执行。
当谷底检测到GTCCRA寄存器=0时，输出保护状态变为GTSOS.SOS[1:0]位=01b，并且切换输出持续到下一个波峰。
(3)输出保持期：(4)正常运行期：当GTCCRA寄存器=0时保持输出。
当在波峰中检测到0<GTCCRA寄存器<GTPR寄存器时，输出保护状态变为GTSOS.SOS[1:0]位=00b，并且由于比较匹配而正常执行切换输出。

Figure 23.99 输出保护操作示例，当GTCCRA在波谷缓冲传输期间设置为0，0<GTCCRA<GTPR在波峰缓冲传输期间恢复，低电平有效



(1)正常运营期：(2)过渡期：由于比较匹配而切换输出正常执行。
当谷底检测到GTCCRA寄存器=0时，输出保护状态变为GTSOS.SOS[1:0]位=01b，并且切换输出持续到下一个波峰。
(3)输出保持期：(4)恢复期：当GTCCRA寄存器=0时保持输出。
当波谷中检测到0<GTCCRA寄存器<GTPR寄存器时，输出保护状态变为GTSOS.SOS[1:0]位=00b，保持输出保持到下一个波峰。由于比较匹配而切换输出正常执行。
(5)正常运营期：

Figure 23.100 在波峰缓冲传输期间GTCCRA设置为0时输出保护操作示例，在波谷缓冲传输期间0<GTCCRA<GTPR恢复，低电平有效

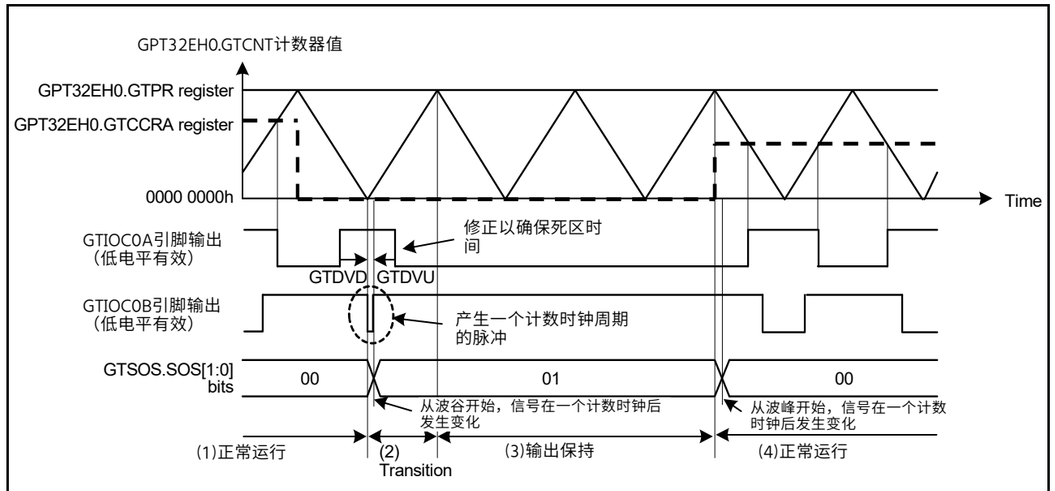


(1) Normal operation period: Toggle output due to a compare match is performed normally.
(2) Transition period: When GTCCRA register = 0 is detected in the trough, the output protection status changes to GTSOS.SOS[1:0] bits = 01b, and toggle output is continued up to the next crest.
(3) Output holding period: The output is held while GTCCRA register = 0.
(4) Normal operation period: When 0 < GTCCRA register < GTPR register Is detected in the crest, the output protection status changes to GTSOS.SOS[1:0] bits = 00b, and toggle output due to a compare match is performed normally.

Figure 23.101 Example of output protection operation when GTCCRA is set to 0 during buffer transfer at crests, with 0 < GTCCRA < GTPR restored during buffer transfer at crests, and active-low

23.8.4.2 Output protection function when GTCCRA ≥ GTPR is set during buffer transfer at troughs

Figure 23.102 and Figure 23.103 show examples of output protection function operation when GTCCRA ≥ GTPR is set during buffer transfer at troughs.

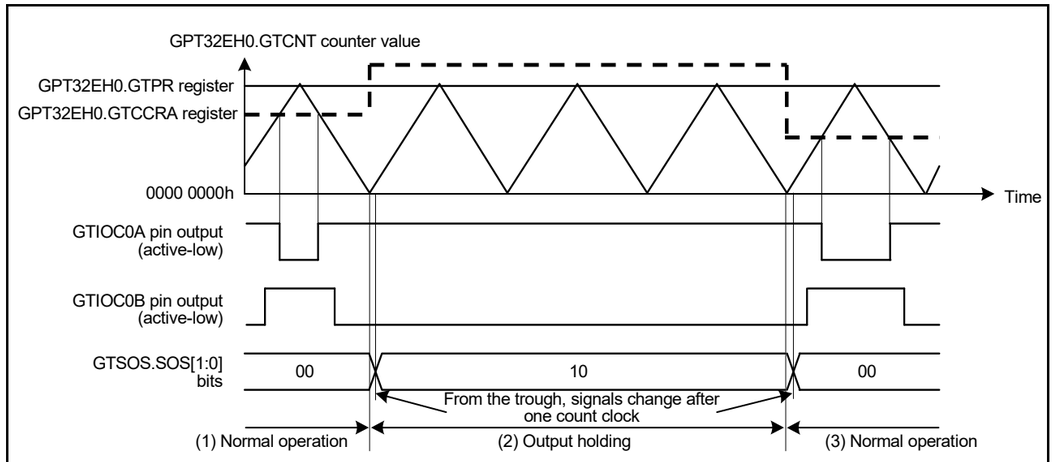


(1)正常运营期：(2)过渡期：由于比较匹配而切换输出正常执行。
当谷底检测到GTCCRA寄存器=0时，输出保护状态变为GTSOS.SOS[1:0]位=01b，并且切换输出持续到下一个波峰。
(3)输出保持期：(4)正常运行期：当GTCCRA寄存器=0时保持输出。
当在波峰中检测到0<GTCCRA寄存器<GTPR寄存器时，输出保护状态变为GTSOS.SOS[1:0]位=00b，并且由于比较匹配而正常执行切换输出。

Figure 23.101 峰值缓冲传输期间GTCCRA设置为0时的输出保护操作示例，0<GTCCRA<GTPR在峰值缓冲传输期间恢复，低电平有效

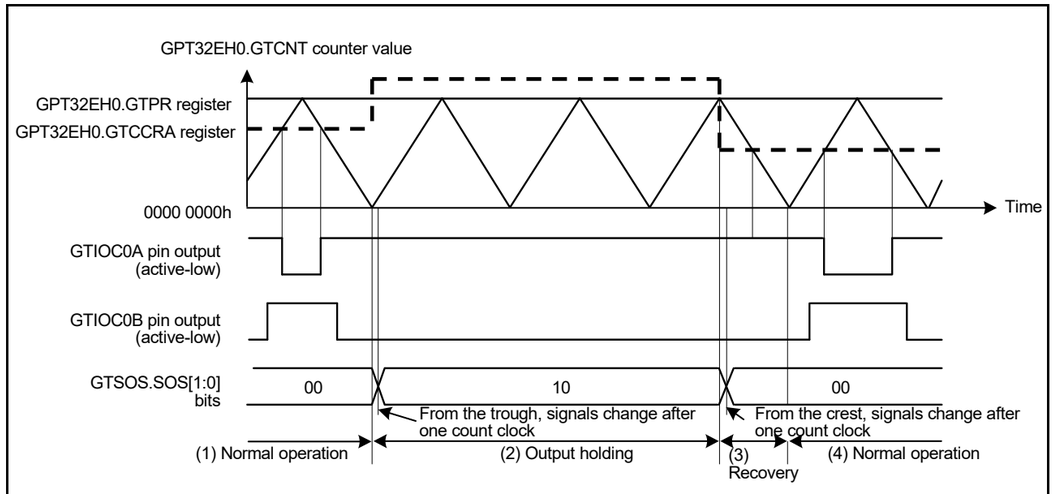
23.8.4.2 谷底缓冲转移时设定GTCCRA≥GTPR时的输出保护功能

图23.102和图23.103显示了在波谷缓冲传输期间设置GTCCRA≥GTPR时输出保护功能操作的示例。



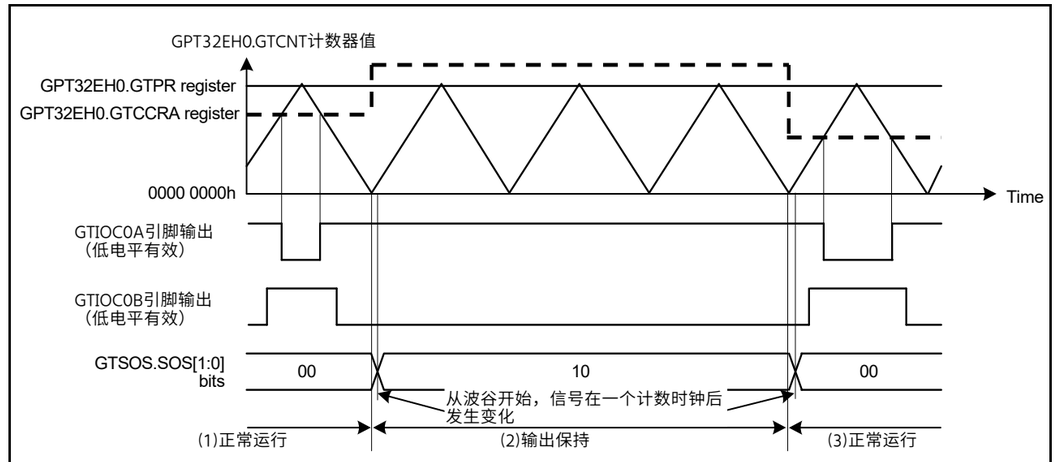
(1) Normal operation period: Toggle output due to a compare match is performed normally.
(2) Output holding period: When GTCCRA register ≥ GTPR register is detected in the trough, the output protection status changes to GTSOS.SOS[1:0] bits = 10b, and the output is held while GTCCRA register ≥ GTPR register.
(3) Normal operation period: When 0 < GTCCRA register < GTPR register is detected in the trough, the output protection status changes to GTSOS.SOS[1:0] bits = 00b, and toggle output due to a compare match is performed normally.

Figure 23.102 Example of output protection operation when GTCCRA ≥ GTPR is set during buffer transfer at troughs, with 0 < GTCCRA < GTPR restored during buffer transfer at troughs, and active-low



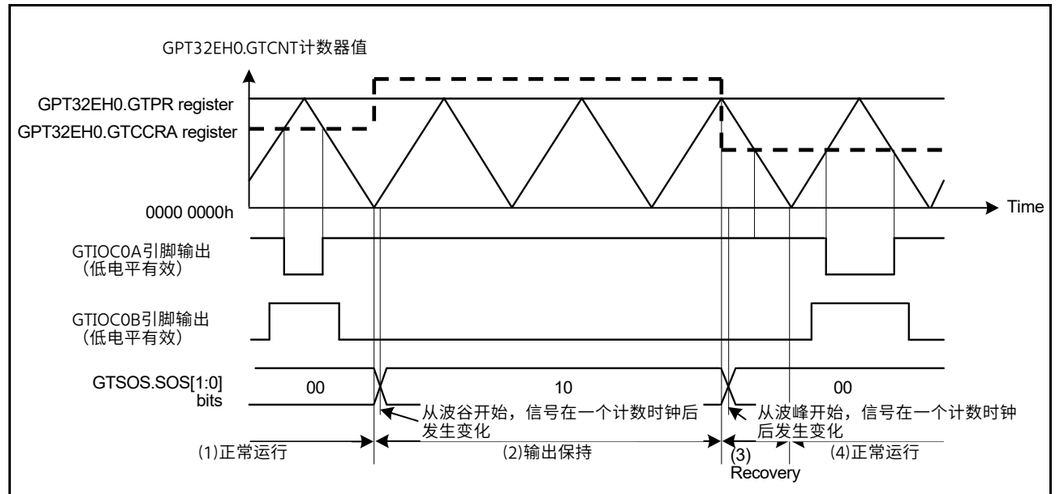
(1) Normal operation period: Toggle output due to a compare match is performed normally.
(2) Output holding period: When GTCCRA register ≥ GTPR register is detected in the trough, the output protection status changes to GTSOS.SOS[1:0] bits = 10b, and the output is held while GTCCRA register ≥ GTPR register.
(3) Recovery period: When 0 < GTCCRA register < GTPR register is detected in the crest, the output protection status changes to GTSOS.SOS[1:0] bits = 00b, and holding output is maintained up to the next trough.
(4) Normal operation period: Toggle output due to a compare match is performed normally.

Figure 23.103 Example of output protection operation when GTCCRA ≥ GTPR is set during buffer transfer at troughs, with 0 < GTCCRA < GTPR restored during buffer transfer at crests, and active-low



(1)正常运行期间：(2)输出保持期间：由于比较匹配而切换输出正常执行。
当检测到GTCCRA寄存器 GTPR寄存器处于波谷时，输出保护状态变为GTSOS.SOS[1:0]位=10b，并在GTCCRA寄存器 GTPR寄存器期间保持输出。当在谷中检测到0<GTCCRA寄存器<GTPR寄存器时，输出保护状态变为GTSOS.SOS[1:0]位=00b，并且由于比较匹配而正常执行切换输出。
(3)正常运营期：

Figure 23.102 输出保护操作示例，当GTCCRA≥GTPR在谷底缓冲区传输期间设置，0<GTCCRA<GTPR在谷底缓冲区传输期间恢复，低电平有效

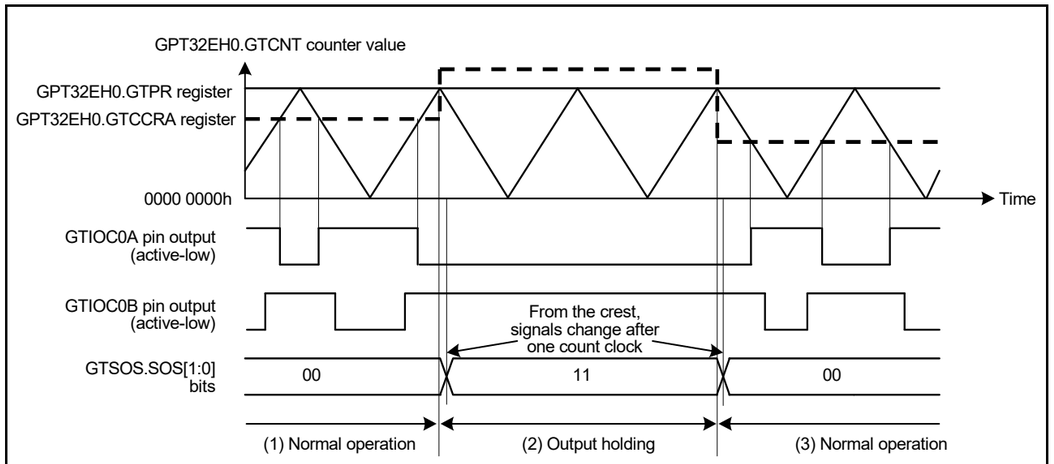


(1)正常运行期间：(2)输出保持期间：由于比较匹配而切换输出正常执行。
当检测到GTCCRA寄存器 GTPR寄存器处于波谷时，输出保护状态变为GTSOS.SOS[1:0]位=10b，并在GTCCRA寄存器 GTPR寄存器期间保持输出。当波峰检测到0<GTCCRA寄存器<GTPR寄存器时，输出保护状态变为GTSOS.SOS[1:0]位=00b，并保持输出保持到下一个波谷。由于比较匹配而切换输出正常执行。
(3) Recovery period:
(4)正常运营期：

Figure 23.103 谷底缓冲传输期间设置GTCCRA≥GTPR时输出保护操作示例，峰值缓冲传输期间0<GTCCRA<GTPR恢复，低电平有效

23.8.4.3 Output protection function when GTCCRA ≥ GTPR is set during buffer transfer at crests

Figure 23.104 and Figure 23.105 show examples of output protection function operation when GTCCRA ≥ GTPR is set during buffer transfer at crests.



(1) Normal operation period: Toggle output due to a compare match is performed normally.

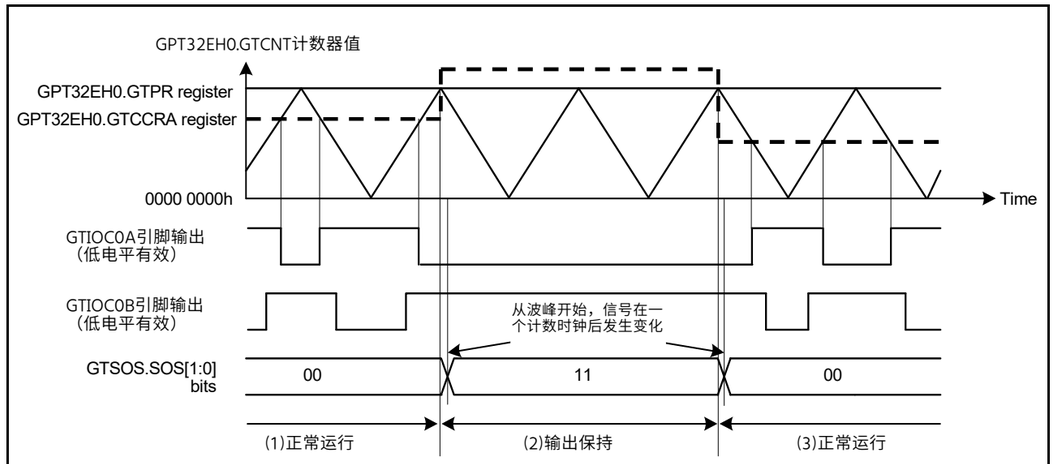
(2) Output holding period: When GTCCRA register ≥ GTPR register is detected in the crest, the output protection status changes to GTSOS.SOS[1:0] bits = 11b, and the output is held while GTCCRA register ≥ GTPR register.

(3) Normal operation period: When 0 < GTCCRA register < GTPR register is detected in the crest, the output protection status changes to GTSOS.SOS[1:0] bits = 00b, and toggle output due to a compare match is performed normally.

Figure 23.104 Example of output protection operation when GTCCRA ≥ GTPR is set during buffer transfer at crests, with 0 < GTCCRA < GTPR restored during buffer transfer at crests, and active-low

23.8.4.3 GTCCRA≥GTPR时的输出保护功能在波峰缓冲传输期间设置

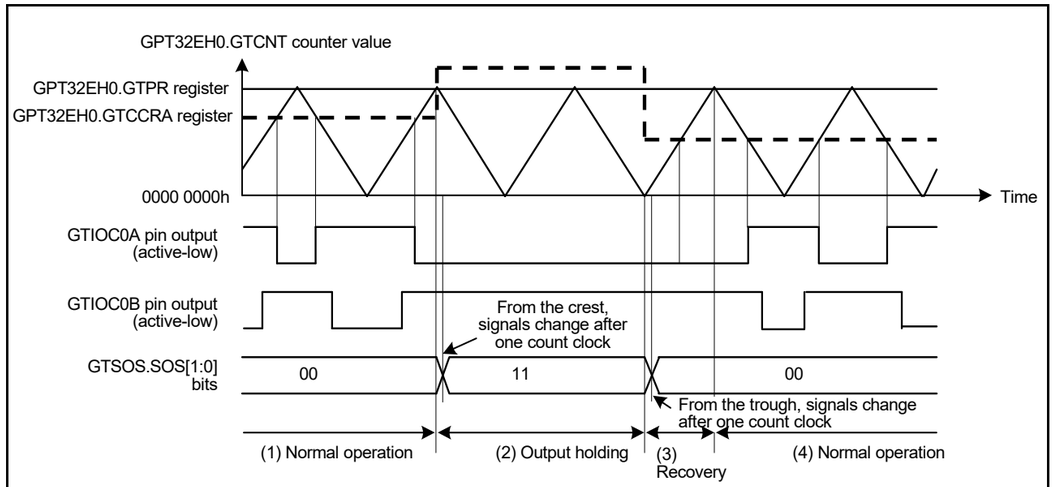
图23.104和图23.105显示了在峰值缓冲区传输期间设置GTCCRA≥GTPR时输出保护功能操作的示例。



(1)正常运行期间：(2)输出保持期间：由于比较匹配而切换输出正常执行。当在波峰中检测到GTCCRA寄存器　GTPR寄存器时，输出保护状态变为GTSOS.SOS[1:0]位=11b，并在GTCCRA寄存器　GTPR寄存器期间保持输出。当在波峰中检测到0<GTCCRA寄存器<GTPR寄存器时，输出保护状态变为GTSOS.SOS[1:0]位=00b，并且由于比较匹配而正常执行切换输出。

(3)正常运营期：

Figure 23.104 输出保护操作示例，当GTCCRA≥GTPR在波峰缓冲传输期间设置，0<GTCCRA<GTPR在波峰缓冲传输期间恢复，低电平有效



(1) Normal operation period: Toggle output due to a compare match is performed normally.
(2) Output holding period: When GTCCRA ≥ GTPR is detected in the crest, the output protection status changes to GTSOS.SOS[1:0] = 11b, and the output is held while GTCCRA ≥ GTPR.
(3) Recovery period: When 0 < GTCCRA < GTPR is detected in the trough, the output protection status changes to GTSOS.SOS[1:0] = 00b, and holding output is maintained up to the next crest.
(4) Normal operation period: Toggle output due to a compare match is performed normally.

Figure 23.105 Example of output protection function operation when GTCCRA ≥ GTPR is set during buffer transfer at crests, with 0 < GTCCRA < GTPR restored during buffer transfer at troughs, and active-low

23.8.4.4 Restricted specification of output protection function

The value of the GTCCRA register must be set within the range of (0 < GTCCRA < GTPR) at count start. If an incorrect value is set in the GTCCRA register during counting (a setting outside the range of 0 < GTCCRA < GTPR), the output protection function deactivates the level of one of the positive and negative outputs.

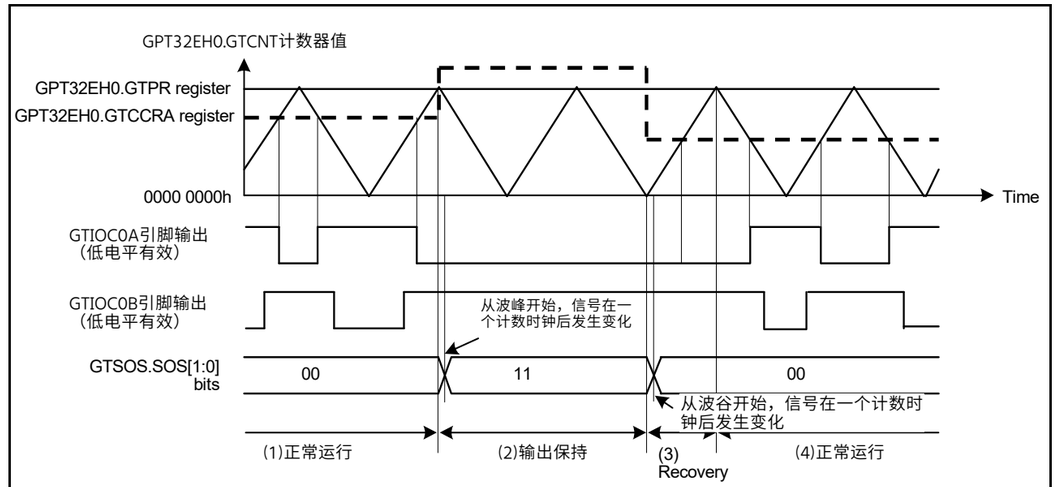
The function does not operate correctly if the following conditions are not satisfied:

- GTCCRA is 0 < GTCCRA < GTPR when counting starts
- The register conditions must be GTCCRA < GTPR + GTDVD - 1 during buffer transfer at crests
- When GTCCRA is greater than or equal to GTPR during buffer transfer at troughs, the register conditions must be GTCCRA > GTDVU + 1.

23.8.4.5 Temporary cancellation of output protection function

When the GTSOTR.SOTR bit is set to 1 with GTSOS.SOS[1:0] bits equal to 10b (showing output protection state by GTCCRA ≥ GTPR during buffer transfer at troughs), the output protection function for GTIOCB pin is temporarily canceled. GTSOS.SOS[1:0] bits retain the value of 10b even when the output protection function is canceled. When the SOTR bit is set to 0, the output protection function for GTIOCB pin resumes.

Figure 23.106 shows examples of temporary cancellation of output protection function operation when the GTCCRA ≥ GTPR is set during buffer transfer at troughs.



(1)正常运行期间：(2)输出保持期间：由于比较匹配而切换输出正常执行。当波峰检测到GTCCRA GTPR时，输出保护状态变为GTSOS.SOS[1:0]=11b，并且在GTCCRA GTPR时保持输出。
(3) Recovery period: 当波谷检测到0<GTCCRA<GTPR时，输出保护状态变为GTSOS.SOS[1:0]=00b，保持输出保持到下一个波峰。
(4)正常运营期：由于比较匹配而切换输出正常执行。

Figure 23.105 峰值缓冲传输期间设置GTCCRA≥GTPR时输出保护功能操作示例，在谷值缓冲传输期间0<GTCCRA <GTPR恢复，低电平有效

23.8.4.4 输出保护功能限制规格

GTCCRA寄存器的值必须在计数开始时设置在(0<GTCCRA<GTPR)的范围内。如果在计数期间在GTCCRA寄存器中设置了不正确的值（设置超出0<GTCCRA<GTPR的范围），则输出保护功能会禁用正输出和负输出之一的电平。

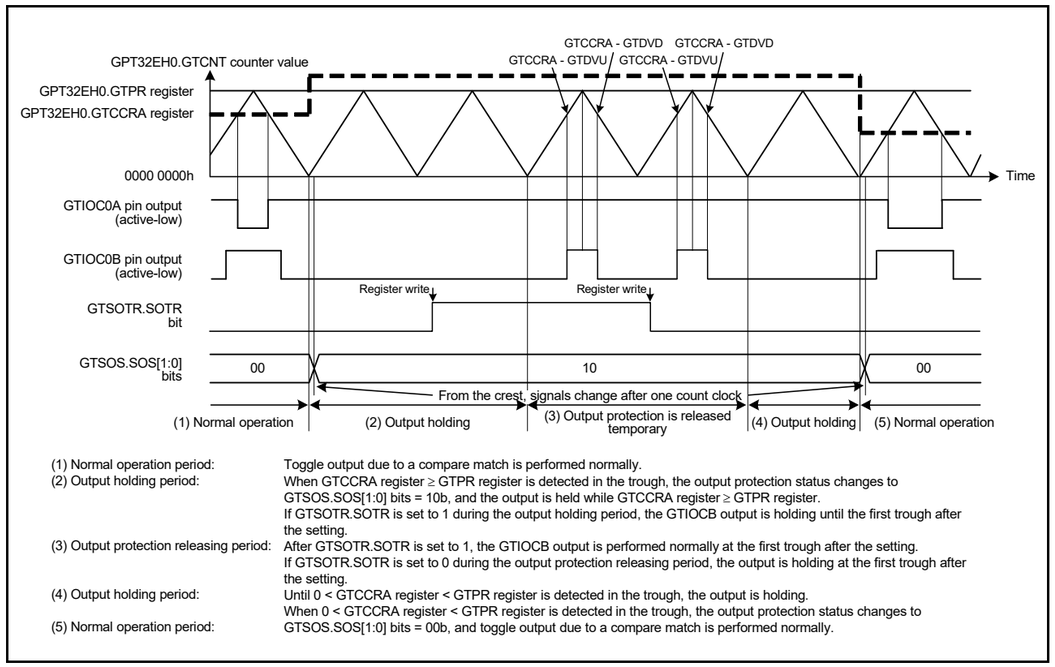
如果不满足以下条件，该功能将无法正常运行：

- 计数开始时GTCCRA为0<GTCCRA<GTPR
- 在波峰缓冲区传输期间，寄存器条件必须为GTCCRA<GTPR+GTDVD1
- 当谷底缓冲区传输期间GTCCRA大于或等于GTPR时，寄存器条件必须为 GTCCRA > GTDVU + 1.

23.8.4.5 输出保护功能暂时取消

当GTSOTR.SOTR位设置为1且GTSOS.SOS[1:0]位等于10b时（显示输出保护状态 GTCCRA≥GTPR在低谷缓冲传输期间），GTIOCB引脚的输出保护功能被暂时取消。即使取消了输出保护功能，GTSOS.SOS[1:0]位也保持10b的值。当SOTR位设置为0时，GTIOCB引脚的输出保护功能恢复。

图23.106显示了当GTCCRA≥时输出保护功能操作暂时取消的示例 GTPR在波谷的缓冲区传输期间设置。



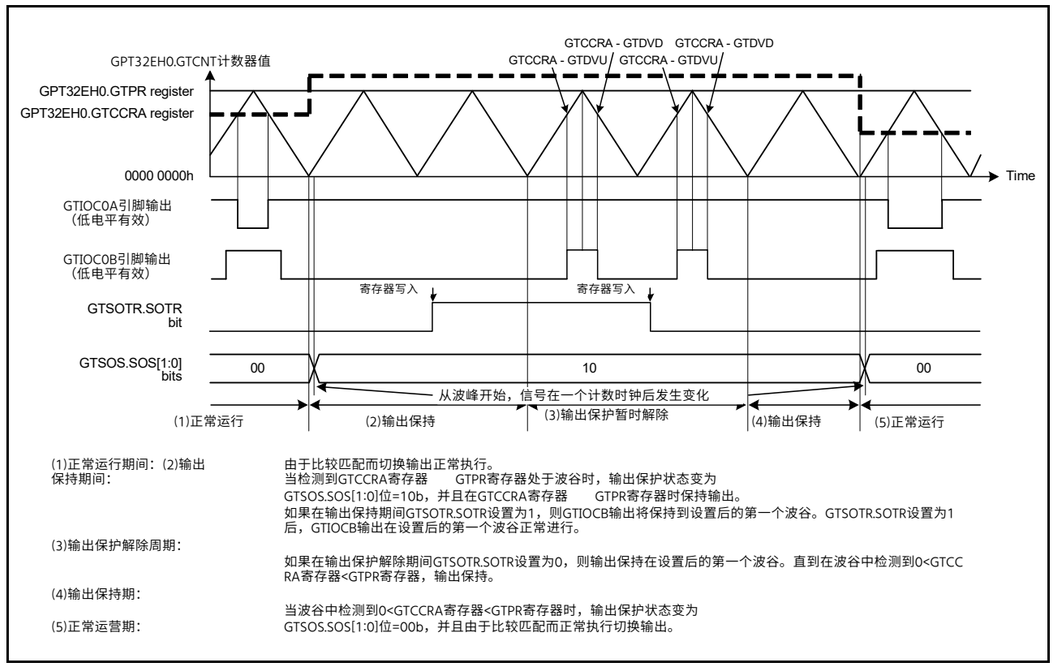
(1) Normal operation period: Toggle output due to a compare match is performed normally.
(2) Output holding period: When GTCCRA register ≥ GTPR register is detected in the trough, the output protection status changes to GTSOS.SOS[1:0] bits = 10b, and the output is held while GTCCRA register ≥ GTPR register.
If GTSOTR.SOTR is set to 1 during the output holding period, the GTIOCB output is holding until the first trough after the setting.
(3) Output protection releasing period: After GTSOTR.SOTR is set to 1, the GTIOCB output is performed normally at the first trough after the setting.
If GTSOTR.SOTR is set to 0 during the output protection releasing period, the output is holding at the first trough after the setting.
(4) Output holding period: Until 0 < GTCCRA register < GTPR register is detected in the trough, the output is holding.
When 0 < GTCCRA register < GTPR register is detected in the trough, the output protection status changes to
(5) Normal operation period: GTSOS.SOS[1:0] bits = 00b, and toggle output due to a compare match is performed normally.

Figure 23.106 Example of temporary cancellation of output protection function operation when GTCCRA ≥ GTPR is set during buffer transfer at troughs, with 0 < GTCCRA < GTPR restored during buffer transfer at troughs, and active-low

23.9 Initialization Method of Output Pins

23.9.1 Pin Settings after Reset

The GPT registers are initialized at reset. Start counting after selecting the port pin function with the PmnPFS register, setting GTIOR.OAE and GTIOR.OBE bits, and outputting the GPT function to external pins.



(1)正常运行期间：(2)输出保持期间：由于比较匹配而切换输出正常执行。
当检测到GTCCRA寄存器 GTPR寄存器处于波谷时，输出保护状态变为GTSOS.SOS[1:0]位=10b，并且在GTCCRA寄存器 GTPR寄存器时保持输出。
如果在输出保持期间GTSOTR.SOTR设置为1，则GTIOCB输出将保持到设置后的第一个波谷。GTSOTR.SOTR设置为1后，GTIOCB输出在设置后的第一个波谷正常进行。
(3)输出保护解除周期：
如果在输出保护解除期间GTSOTR.SOTR设置为0，则输出保持在设置后的第一个波谷。直到在波谷中检测到0<GTCCRA寄存器<GTPR寄存器，输出保持。
(4)输出保持期：
当波谷中检测到0<GTCCRA寄存器<GTPR寄存器时，输出保护状态变为
(5)正常运营期：GTSOS.SOS[1:0]位=00b，并且由于比较匹配而正常执行切换输出。

Figure 23.106 GTCCRA≥时输出保护功能动作暂时取消的例子
GTPR在波谷缓冲区传输期间设置，0<GTCCRA<GTPR在波谷缓冲区传输期间恢复，低电平有效

23.9 输出管脚的初始化方法

23.9.1 复位后的引脚设置

GPT寄存器在复位时被初始化。通过PmnPFS寄存器选择端口引脚功能，设置GTIOR.OAE和GTIOR.OBE位，并将GPT功能输出到外部引脚后开始计数。

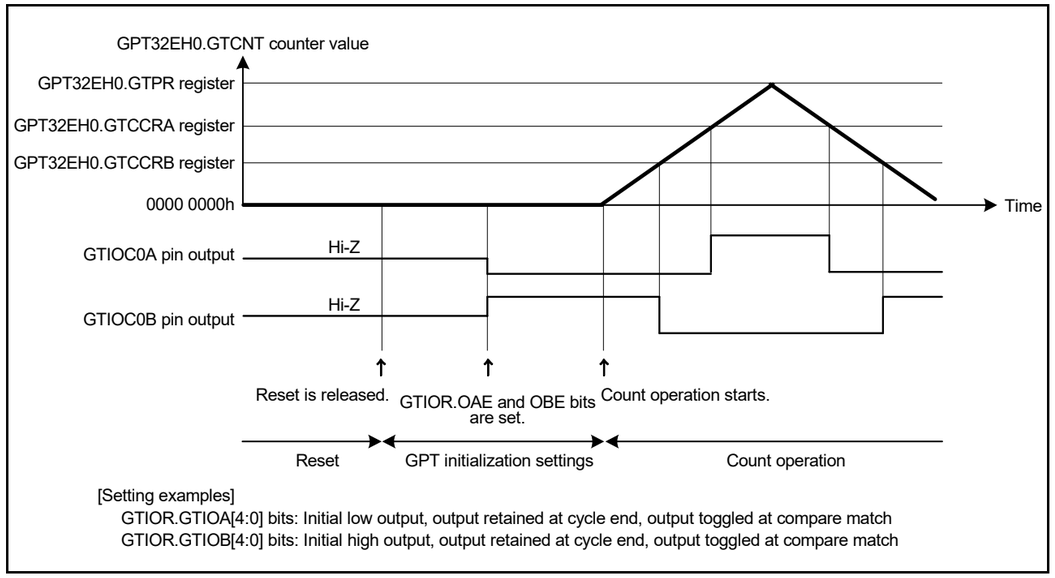


Figure 23.107 Example of pin settings after reset

23.9.2 Pin Initialization Caused by Error during Operation

If an error occurs during GPT operation, the following four types of pin processing can be performed before pin initialization:

- Set the OAHLD and OBHLD bits in GTIOR to 1 and retain the outputs at count stop
- Set the OAHLD and OBHLD bits in GTIOR to 0, specify arbitrary output values in OADFLT and OBDFLT in GTIOR, and output the arbitrary values on count stop
- Set the pin to output an arbitrary value as a general output port by setting the PDR, PODR, and PmnPFS registers of the I/O port in advance. Set the OAE and OBE bits in GTIOR to 0 and the control bit associated with the pin in the PmnPFS.PMR to 0 to allow arbitrary values to be output from the pin set as a general output port when an error occurs.
- Drive the output to a high impedance state using the POEG function.

When the automatic dead time setting is made, clear the GTDTCR.TDE bit to 0 after counting stops. When counting stops, only the values of registers that are changed by a GPT external source change. If counting resumes, operation continues from where it stopped. If counting stops, registers must be initialized before counting starts.

23.10 Usage Notes

23.10.1 Module-Stop Function Setting

The Module Stop Control Register can enable or disable GPT operation. The GPT module is initially stopped after reset. Releasing the module-stop state enables access to the registers. For details, see section 11, Low Power Modes.

23.10.2 GTCCRn Settings during Compare Match Operation (n = A to F)

(1) When automatic dead time setting is made in triangle-wave PWM mode

The GTCCRA register must satisfy the following conditions: GTDVU < GTCCRA, GTDVD < GTCCRA, and GTCCRA < GTPR.

When the setting of GTCCRA = 0 or GTCCRA ≥ GTPR is made during count operation, the output protection function is activated.

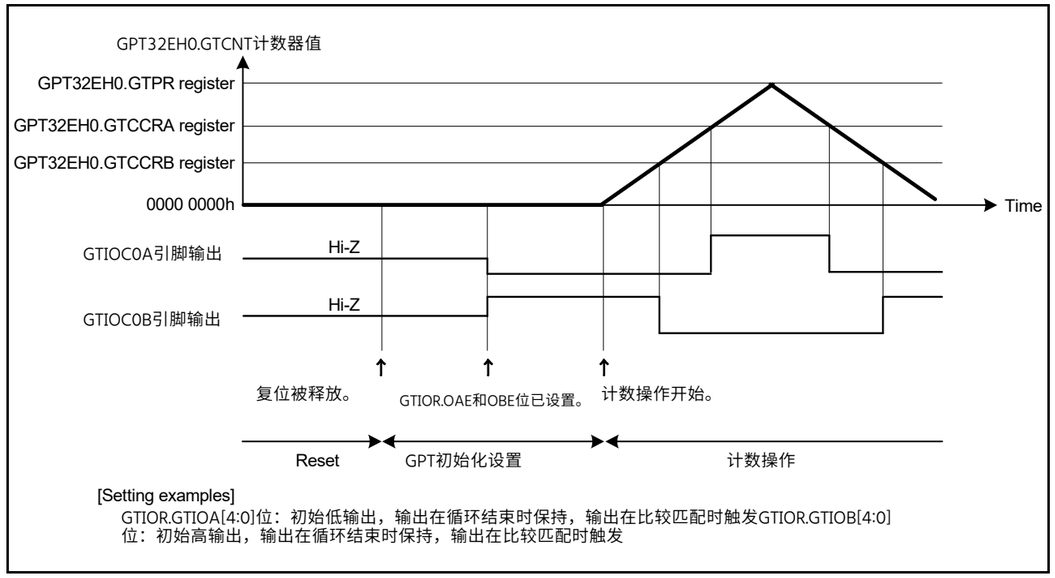


Figure 23.107 复位后的引脚设置示例

23.9.2 操作错误导致的引脚初始化

如果在GPT操作过程中发生错误，可以在引脚初始化之前进行以下四种引脚处理：

- 将GTIOR中的OAHLD和OBHLD位设置为1，并在计数停止时保留输出
- 将GTIOR中的OAHLD和OBHLD位设置为0，在OADFLT和OBDFLT中指定任意输出值GTIOR，并在计数停止时输出任意值
- 通过预先设置IO端口的PDR、PODR和PmnPFS寄存器，将引脚设置为输出任意值作为通用输出端口。将GTIOR中的OAE和OBE位设置为0，并将与PmnPFS.PMR中的引脚相关的控制位设置为0，以允许在发生错误时从设置为通用输出端口的引脚输出任意值。
- 使用POEG功能将输出驱动到高阻抗状态。

进行自动死区时间设置时，计数停止后将GTDTCR.TDE位清零。当计数停止时，只有被GPT外部源改变的寄存器的值会改变。如果计数恢复，则操作从停止处继续。如果计数停止，则必须在计数开始前初始化寄存器。

23.10 使用说明

23.10.1 模块停止功能设置

模块停止控制寄存器可以启用或禁用GPT操作。GPT模块在复位后最初停止。
释放模块停止状态可以访问寄存器。有关详细信息，请参阅第11节，低功耗模式。

23.10.2 比较匹配操作期间的GTCCRn设置（n=A到F）

(1) 在三角波PWM模式下进行自动死区时间设置时

GTCCRA寄存器必须满足以下条件：GTDVU<GTCCRA，GTDVD<GTCCRA，并且GTCCRA < GTPR.

当在计数操作期间设置GTCCRA=0或GTCCRA≥GTPR时，输出保护功能被激活。

However, the function does not operate correctly if the following conditions are not satisfied:

- GTCCRA is 0 < GTCCRA < GTPR when counting starts
- The register conditions must be GTCCRA < GTPR + GTDVD - 1 during buffer transfer at crests
- When GTCCRA is greater than or equal to GTPR during buffer transfer at troughs, the register conditions must be GTCCRA > GTDVU + 1.

For details, see section 23.8.4, Output Protection Function for GTIOC Pin Output.

(2) When automatic dead time setting is not made in triangle-wave PWM mode

The GTCCRA register must be set within the range of 0 < GTCCRA < GTPR. If GTCCRA = 0 or GTCCRA = GTPR is set, a compare match occurs within the cycle only when GTCCRA = 0 or GTCCRA = GTPR is satisfied. When GTCCRA > GTPR, no compare match occurs.

Similarly, GTCCRB must be set within the range of 0 < GTCCRB < GTPR. If GTCCRB = 0 or GTCCRB = GTPR is set, a compare match occurs within the cycle only when GTCCRB = 0 or GTCCRB = GTPR is satisfied. When GTCCRB > GTPR, no compare match occurs.

(3) When automatic dead time setting is made in saw-wave one-shot pulse mode

The GTCCRC and GTCCRD registers must be set to satisfy the following constraints. If the constraints are not satisfied, correct output waveforms with secured dead time might not be obtained:

- In up-counting: GTCCRC < GTCCRD, GTCCRC > GTDVU, GTCCRD < GTPR - GTDVD
- In down-counting: GTCCRC > GTCCRD, GTCCRC < GTPR - GTDVU, GTCCRD > GTDVD.

(4) When automatic dead time setting is not made in saw-wave one-shot pulse mode

The GTCCRC and GTCCRD registers must be set to satisfy the following constraints. If the constraints are not satisfied, two compare matches do not occur and pulse output cannot be performed:

- In up-counting: 0 < GTCCRC < GTCCRD < GTPR
- In down-counting: GTPR > GTCCRC > GTCCRD > 0.

Similarly, GTCCRE and GTCCRF must be set to satisfy the following constraints. If the constraints are not satisfied, two compare matches do not occur and pulse output cannot be performed:

- In up-counting: 0 < GTCCRE < GTCCRF < GTPR
- In down-counting: GTPR > GTCCRE > GTCCRF > 0.

(5) In saw-wave PWM mode

The GTCCRA register must be set with the range of 0 < GTCCRA < GTPR. If GTCCRA = 0 or GTCCRA = GTPR is set, a compare match occurs within the cycle only when GTCCRA = 0 or GTCCRA = GTPR is satisfied. If GTCCRA > GTPR is set, no compare match occurs.

Similarly, GTCCRB must be set with the range of 0 < GTCCRB < GTPR. If GTCCRB = 0 or GTCCRB = GTPR is set, a compare match occurs within the cycle only when GTCCRB = 0 or GTCCRB = GTPR is satisfied. If GTCCRB > GTPR is set, no compare match occurs.

23.10.3 Setting Range for the GTCNT Counter

The GTCNT counter register must be set with the range of 0 ≤ GTCNT ≤ GTPR.

23.10.4 Starting and Stopping the GTCNT Counter

The control timing of starting and stopping the GTCNT counter by the GTCR.CST bit synchronizes the count clock that is selected in GTCR.TPCS[2:0]. When GTCR.CST is updated, the GTCNT counter starts/stops after a count clock selected in GTCR.TPCS[2:0]. Therefore, an event generated before the GTCNT counter actually starts is ignored. On the other hand, there might be cases where an event is accepted or an interrupt occurs after GTCR.CST is set to 0.

但是，如果不满足以下条件，该功能将无法正常运行：

- 计数开始时GTCCRA为0<GTCCRA<GTPR
- 在波峰缓冲区传输期间，寄存器条件必须为GTCCRA<GTPR+GTDVD1
- 当谷底缓冲区传输期间GTCCRA大于或等于GTPR时，寄存器条件必须为 GTCCRA > GTDVU + 1.

有关详细信息，请参见第23.8.4节，GTIOC引脚输出的输出保护功能。

(2) 在三角波PWM模式下未进行自动死区时间设置时

GTCCRA寄存器必须设置在0<GTCCRA<GTPR的范围内。如果设置了GTCCRA=0或GTCCRA=GTPR，则仅当满足GTCCRA=0或GTCCRA=GTPR时，才会在周期内发生比较匹配。当GTCCRA>GTPR时，不发生比较匹配。

同样，GTCCRB必须设置在0<GTCCRB<GTPR的范围内。如果设置了GTCCRB=0或GTCCRB=GTPR，则仅当满足GTCCRB=0或GTCCRB=GTPR时，才会在周期内发生比较匹配。当GTCCRB>GTPR时，不发生比较匹配。

(3) 在锯波单发脉冲模式下进行自动死区时间设置时

GTCCRC和GTCCRD寄存器必须设置为满足以下约束。如果不满足约束条件，则可能无法获得具有安全死区时间的正确输出波形：

- In up-counting: GTCCRC < GTCCRD, GTCCRC > GTDVU, GTCCRD < GTPR - GTDVD
- In down-counting: GTCCRC > GTCCRD, GTCCRC < GTPR - GTDVU, GTCCRD > GTDVD.

(4) 在锯波单发脉冲模式下未进行自动死区时间设置时

GTCCRC和GTCCRD寄存器必须设置为满足以下约束。如果不满足约束条件，则不会发生两个比较匹配并且无法执行脉冲输出：

- In up-counting: 0 < GTCCRC < GTCCRD < GTPR
- In down-counting: GTPR > GTCCRC > GTCCRD > 0.

同样，必须设置GTCCRE和GTCCRF以满足以下约束。如果不满足约束条件，则不会发生两个比较匹配并且无法执行脉冲输出：

- In up-counting: 0 < GTCCRE < GTCCRF < GTPR
- In down-counting: GTPR > GTCCRE > GTCCRF > 0.

(5) 在锯齿波PWM模式下

GTCCRA寄存器必须设置为0<GTCCRA<GTPR。如果设置了GTCCRA=0或GTCCRA=GTPR，则仅当满足GTCCRA=0或GTCCRA=GTPR时，才会在周期内发生比较匹配。如果设置了GTCCRA>GTPR，则不会发生比较匹配。

类似地，GTCCRB必须设置在0<GTCCRB<GTPR的范围内。如果设置了GTCCRB=0或GTCCRB=GTPR，则仅当满足GTCCRB=0或GTCCRB=GTPR时，才会在周期内发生比较匹配。如果设置了GTCCRB>GTPR，则不会发生比较匹配。

23.10.3 GTCNT计数器的设置范围

GTCNT计数器寄存器的设置范围必须为0≤GTCNT≤GTPR。

23.10.4 启动和停止GTCNT计数器

通过GTCR.CST位启动和停止GTCNT计数器的控制时序与在GTCR.TPCS[2:0]中选择的计数时钟同步。当GTCR.CST更新时，GTCNT计数器在GTCR.TPCS[2:0]中选择的计数时钟后开始停止。因此，在GTCNT计数器实际启动之前生成的事件将被忽略。另一方面，在GTCR.CST设置为0之后，可能会接受事件或发生中断。

23.10.5 Priority Order of Each Event

(1) GTCNT register

Table 23.24 shows a priority order of events updating GTCNT register.

Table 23.24 Priority order of sources updating GTCNT

Source updating GTCNT	Priority order
Writing by CPU (Writing to GTCNT/GTCLR)	High ↑
Clear by hardware sources set in GTCSR	
Count up or down by hardware sources set in GTUPSR/GTDNSR	
Count operation	↓ Low

If up-counting and down-counting by hardware sources occur at the same time, the GTCNT counter value does not change. When there is a conflict between updating the GTCNT register and reading by the CPU, pre-update data is read.

(2) GTCR.CST bit

When there is a conflict between starting/stopping by hardware sources set in the GTSSR/GTPSR registers and writing by the CPU (writing to GTCR/GTSTR/GTSTP registers), writing by CPU has priority over starting/stopping by hardware sources.

When there is a conflict between starting by hardware sources set in the GTSSR register and stopping by hardware sources set in GTPSR register, the GTCR.CST bit value does not change. Where there is a conflict between updating the GTCR.CST bit and reading by the CPU, pre-update data is read.

(3) GTCCRn registers (n = A to F)

When there is a conflict between input capture/buffer transfer operation and writing to GTCCRn registers, writing to GTCCRn registers has priority over input capture/buffer transfer operation. When there is a conflict between input capture and writing to the counter register by the CPU or updating the counter register by hardware sources, the pre-update counter value is captured. Where there is a conflict between updating the GTCCRn registers and reading by the CPU, pre-update data is read.

(4) GTPR registers

When there is a conflict between buffer transfer operation and writing to the GTPR register, writing to GTPR register has priority over buffer transfer operation. When there is a conflict between updating GTPR register and reading by the CPU, pre-update data is read.

(5) GTADTRn registers (n = A, B)

When there is a conflict between buffer transfer operation and writing to the GTADTRn registers, writing to the GTADTRn registers has priority over buffer transfer operation. Where there is a conflict between updating GTADTRn registers and reading by the CPU, pre-update data is read.

(6) GTDVn registers (n = U, D)

When there is a conflict between buffer transfer operation and writing to GTDVn registers, writing to GTDVn registers has priority over buffer transfer operation. When there is a conflict between updating GTDVn registers and reading by the CPU, pre-update data is read.

23.10.5 每个事件的优先顺序

(1) GTCNT register

表23.24显示了更新GTCNT寄存器的事件的优先级顺序。

Table 23.24 更新GTCNT的源的优先顺序

源更新GTCNT	优先顺序
CPU写入（写入GTCNTGTCLR）	High ↑
由GTCSR中设置的硬件源清除	
通过GTUPSRGTDNSR中设置的硬件源进行向上或向下计数	
计数操作	↓ Low

如果硬件源的递增计数和递减计数同时发生，GTCNT计数器值不会改变。当更新GTCNT寄存器和CPU读取之间存在冲突时，会读取更新前的数据。

(2) GTCR.CST bit

当GTSSRGTPSR寄存器中设置的硬件源启动停止与CPU写入（写入GTCRGTSTRGTSTP寄存器）发生冲突时，CPU写入优先于硬件源启动停止。

当GTSSR寄存器中设置的硬件源启动和GTPSR寄存器中设置的硬件源停止之间存在冲突时，GTCR.CST位的值不会改变。如果更新GTCR.CST位与CPU读取之间存在冲突，则读取更新前的数据。

(3) GTCCRn寄存器（n=A到F）

当输入捕捉缓冲区传输操作和写入GTCCRn寄存器之间存在冲突时，写入GTCCRn寄存器优先于输入捕捉缓冲区传输操作。当输入捕获与CPU写入计数器寄存器或硬件源更新计数器寄存器之间存在冲突时，将捕获更新前的计数器值。如果更新GTCCRn寄存器和CPU读取之间存在冲突，则读取更新前的数据。

(4) GTPR registers

当缓冲区传输操作与写入GTPR寄存器之间存在冲突时，写入GTPR寄存器优先于缓冲区传输操作。当更新GTPR寄存器与CPU读取发生冲突时，读取更新前的数据。

(5) GTADTRn registers (n = A, B)

当缓冲区传输操作和写入GTADTRn寄存器之间存在冲突时，写入GTADTRn寄存器优先于缓冲区传输操作。如果更新GTADTRn寄存器与CPU读取之间存在冲突，则读取更新前的数据。

(6) GTDVn registers (n = U, D)

当缓冲区传输操作和写入GTDVn寄存器之间存在冲突时，写入GTDVn寄存器优先于缓冲区传输操作。当更新GTDVn寄存器和CPU读取之间存在冲突时，会读取更新前的数据。

24. PWM Delay Generation Circuit

24.1 Overview

The MCU has 4 channel delay circuits that can connect to the General PWM Timer (GPT). Table 24.1 lists the specifications for the PWM Delay Generation Circuit, Figure 24.1 shows a block diagram, and Table 24.2 lists the I/O pins.

Table 24.1 Specifications of the PWM Delay Generation Circuit

Parameter	Specifications
Function	The circuit can control the timing with which signals on the two PWM output pins for channel 0/1/2/3 rise and fall to an accuracy of up to 1/32 times the period of the GPT clock (PCLKD).

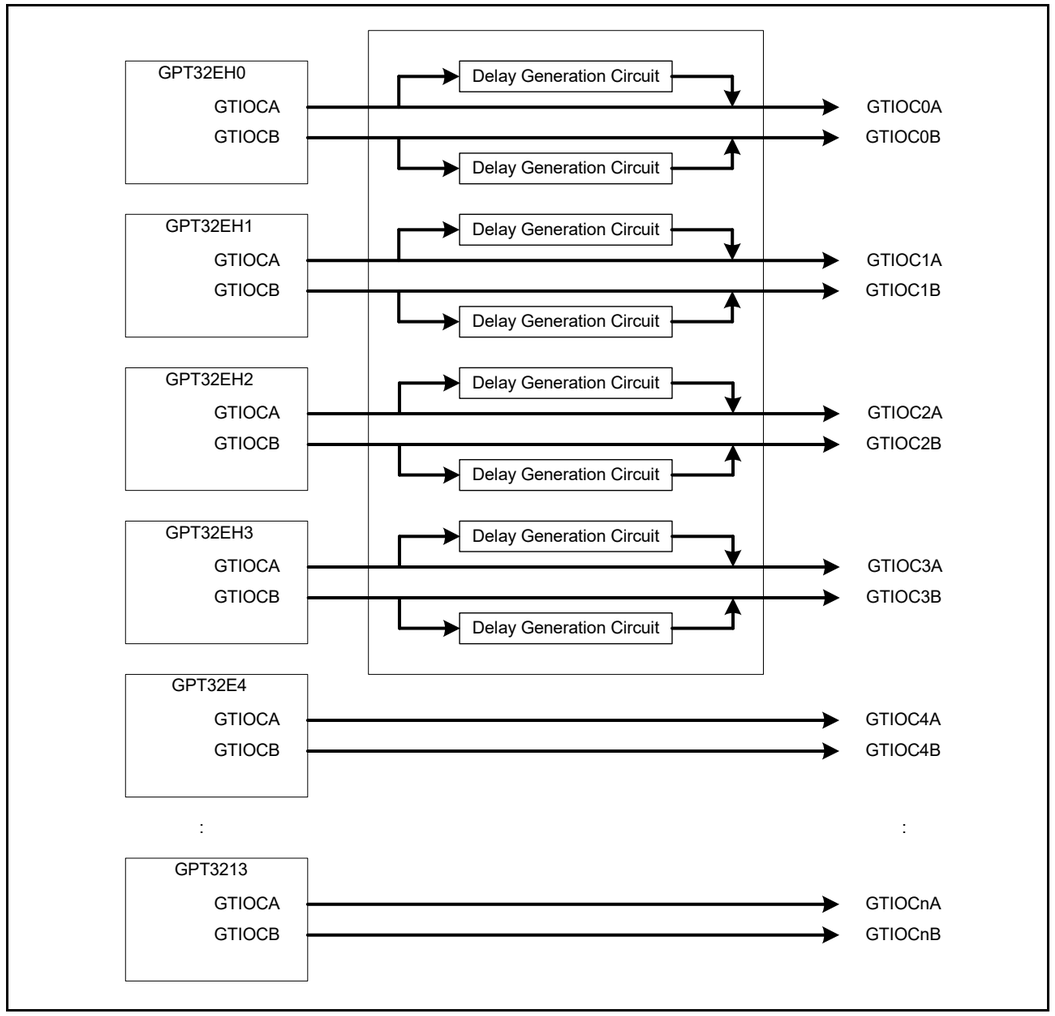


Figure 24.1 PWM delay generation circuit block diagram

24. PWM延迟产生电路

24.1 Overview

MCU有4个通道延迟电路，可以连接到通用PWM定时器(GPT)。表24.1列出了PWM延迟产生电路的规格，图24.1显示了框图，表24.2列出了IO引脚。

Table 24.1 PWM延迟发生电路的规格

Parameter	Specifications
Function	该电路可以控制通道0123的两个PWM输出引脚上的信号上升和下降的时序，精度高达GPT时钟(PCLKD)周期的132倍。

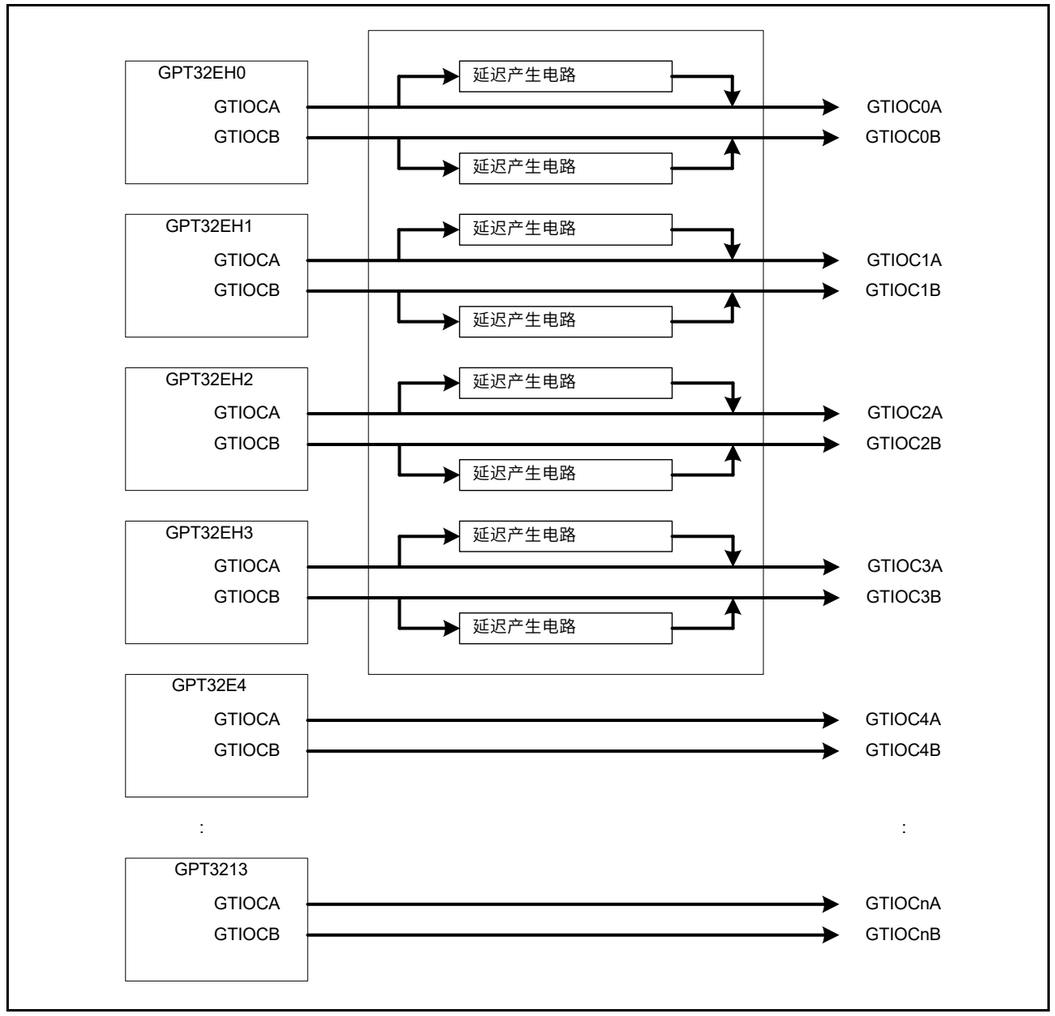


Figure 24.1 PWM延迟产生电路框图

Table 24.2 PWM delay generation circuit I/O pins

I/O pin	I/O	Function
GTIOC0A	Output	Delayed output of GTIOCA pin of GPT channel 0
GTIOC0B	Output	Delayed output of GTIOCB pin of GPT channel 0
GTIOC1A	Output	Delayed output of GTIOCA pin of GPT channel 1
GTIOC1B	Output	Delayed output of GTIOCB pin of GPT channel 1
GTIOC2A	Output	Delayed output of GTIOCA pin of GPT channel 2
GTIOC2B	Output	Delayed output of GTIOCB pin of GPT channel 2
GTIOC3A	Output	Delayed output of GTIOCA pin of GPT channel 3
GTIOC3B	Output	Delayed output of GTIOCB pin of GPT channel 3

24.2 Register Descriptions

24.2.1 PWM Output Delay Control Register (GTDLYCR)

Address(es): GPT_ODC.GTDLYCR 4007 B000h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DLYRST	DLLEN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	DLLEN	DLL Operation Enable	0: DLL operation disabled 1: DLL operation enabled.	R/W
b1	DLYRST	PWM Delay Generation Circuit Reset	0: Normal operation 1: Reset.	R/W
b15 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The GTDLYCR register controls the PWM delay generation circuit, which applies delays to the PWM outputs. GTDLYCR register can be written when register write protection is disabled (GPT32EH0.GTWP.WP = 0).

DLLEN bit (DLL Operation Enable)

The DLLEN bit selects whether the on-chip DLL in the PWM delay generation circuit is activated or not.

DLYRST bit (PWM Delay Generation Circuit Reset)

The DLYRST bit resets the internal state of the PWM delay generation circuit.

24.2.2 PWM Output Delay Control Register 2 (GTDLYCR2)

Address(es): GPT_ODC.GTDLYCR2 4007 B002h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	DLYEN3	DLYEN2	DLYEN1	DLYEN0	—	—	—	—	DLYBS3	DLYBS2	DLYBS1	DLYBS0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	DLYBS0	PWM Delay Generation Circuit bypass for channel 0	0: Delay generation circuit of channel 0 bypassed 1: Delay generation circuit of channel 0 not bypassed.	R/W

Table 24.2 PWM延迟产生电路IO引脚

I/O pin	I/O	Function
GTIOC0A	Output	GPT通道0的GTIOCA管脚延迟输出
GTIOC0B	Output	GPT通道0的GTIOCB管脚延迟输出
GTIOC1A	Output	GPT通道1的GTIOCA管脚延迟输出
GTIOC1B	Output	GPT通道1的GTIOCB管脚延迟输出
GTIOC2A	Output	GPT通道2的GTIOCA管脚延迟输出
GTIOC2B	Output	GPT通道2的GTIOCB管脚延迟输出
GTIOC3A	Output	GPT通道3的GTIOCA管脚延迟输出
GTIOC3B	Output	GPT通道3的GTIOCB管脚延迟输出

24.2 注册说明

24.2.1 PWM输出延迟控制寄存器(GTDLYCR)

Address(es): GPT_ODC.GTDLYCR 4007 B000h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DLYRST	DLLEN
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	DLLEN	DLL操作启用	0：禁用DLL操作1：启用DLL操作。	R/W
b1	DLYRST	PWM延迟产生电路Reset	0：正常运行1：复位。	R/W
b15 to b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W

GTDLYCR寄存器控制PWM延迟生成电路，该电路将延迟应用于PWM输出。
当寄存器写保护被禁用时（GPT32EH0.GTWP.WP=0），可以写入GTDLYCR寄存器。

DLLEN位（DLL操作使能）

DLLEN位选择是否激活PWM延迟产生电路中的片上DLL。

DLYRST位（PWM延迟产生电路复位）

DLYRST位复位PWM延迟产生电路的内部状态。

24.2.2 PWM输出延迟控制寄存器2(GTDLYCR2)

Address(es): GPT_ODC.GTDLYCR2 4007 B002h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	DLYEN3	DLYEN2	DLYEN1	DLYEN0	—	—	—	—	DLYBS3	DLYBS2	DLYBS1	DLYBS0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	DLYBS0	通道0的PWM延迟生成电路旁路	0：通道0的延时产生电路被旁路1：通道0的延时产生电路不被旁路。	R/W

Bit	Symbol	Bit name	Description	R/W
b1	DLYBS1	PWM Delay Generation Circuit bypass for channel 1	0: Delay generation circuit of channel 1 bypassed 1: Delay generation circuit of channel 1 not bypassed.	R/W
b2	DLYBS2	PWM Delay Generation Circuit bypass for channel 2	0: Delay generation circuit of channel 2 bypassed 1: Delay generation circuit of channel 2 not bypassed.	R/W
b3	DLYBS3	PWM Delay Generation Circuit bypass for channel 3	0: Delay generation circuit of channel 3 bypassed 1: Delay generation circuit of channel 3 not bypassed.	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	DLYEN0	PWM Delay Generation Circuit enable for channel 0	0: Delay generation circuit of channel 0 enabled 1: Delay generation circuit of channel 0 disabled.	R/W
b9	DLYEN1	PWM Delay Generation Circuit enable for channel 1	0: Delay generation circuit of channel 1 enabled 1: Delay generation circuit of channel 1 disabled.	R/W
b10	DLYEN2	PWM Delay Generation Circuit enable for channel 2	0: Delay generation circuit of channel 2 enabled 1: Delay generation circuit of channel 2 disabled.	R/W
b11	DLYEN3	PWM Delay Generation Circuit enable for channel 3	0: Delay generation circuit of channel 3 enabled 1: Delay generation circuit of channel 3 disabled.	R/W
b15 to b12	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The GTDLYCR2 register controls each channel of PWM delay generation circuit. GTDLYCR2 can be written when register write protection is disabled (GPT32EH0.GTWP.WP = 0).

DLYBSn (n = 0 to 3) bit (PWM Delay Generation Circuit Bypass for channel n)

The DLYBSn bit selects whether delays are applied to PWM output signals from the GTIOCnA and GTIOCnB pins (n = 0 to 3) by the PWM delay generation circuit or whether the circuit is bypassed.

A signal delayed in the PWM delay generation circuit is output 3 cycles of GPT operation clock (PCLKD) later than if it bypasses the PWM delay generation circuit.

DLYENn (n = 0 to 3) bit (PWM Delay Generation Circuit Enable for channel n)

The DLYENn bit selects whether channel n (n = 0 to 3) of PWM delay generation circuit is power on or off. If channel n of the PWM delay generation circuit is not used, set to 1.

Bit	Symbol	位名称	Description	R/W
b1	DLYBS1	通道1的PWM延迟生成电路旁路	0：通道1的延时产生电路被旁路1：通道1的延时产生电路不被旁路。	R/W
b2	DLYBS2	通道2的PWM延迟生成电路旁路	0：通道2的延迟产生电路被旁路1：通道2的延迟产生电路不被旁路。	R/W
b3	DLYBS3	通道3的PWM延迟生成电路旁路	0：通道3的延时产生电路被旁路1：通道3的延时产生电路不被旁路。	R/W
b7 to b4	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b8	DLYEN0	通道0的PWM延迟生成电路使能	0：启用通道0的延迟产生电路1：禁用通道0的延迟产生电路。	R/W
b9	DLYEN1	通道1的PWM延迟生成电路使能	0：通道1的延迟产生电路使能1：通道1的延迟产生电路禁止。	R/W
b10	DLYEN2	通道2的PWM延迟生成电路使能	0：启用通道2的延迟产生电路1：禁用通道2的延迟产生电路。	R/W
b11	DLYEN3	通道3的PWM延迟生成电路使能	0：通道3延时产生电路使能1：通道3延时产生电路禁止。	R/W
b15 to b12	—	Reserved	这些位被读取为0。写入值应为0。	R/W

GTDLYCR2寄存器控制PWM延迟产生电路的每个通道。当寄存器写保护被禁用时（GPT32EH0.GTWP.WP=0）可以写入GTDLYCR2。

DLYBSn（n=0到3）位（通道n的PWM延迟生成电路旁路）

DLYBSn位选择是否通过PWM延迟生成电路对来自GTIOCnA和GTIOCnB引脚（n=0至3）的PWM输出信号施加延迟，或者是否绕过该电路。

在PWM延迟发生电路中延迟的信号比绕过PWM延迟发生电路的信号晚3个GPT操作时钟(PCLKD)周期输出。

DLYENn（n=0到3）位（通道n的PWM延迟生成电路使能）

DLYENn位选择PWM延迟发生电路的通道n（n=0到3）是打开还是关闭。如果不使用PWM延迟发生电路的通道n，则设置为1。

24.2.3 GTIOCnA Rising Output Delay Register (GTDLYRnA) (n = 0 to 3)

Address(es): GPT_ODC.GTDLYR0A 4007 B018h, GPT_ODC.GTDLYR1A 4007 B01Ch, GPT_ODC.GTDLYR2A 4007 B020h, GPT_ODC.GTDLYR3A 4007 B024h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	DLY[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b4 to b0	DLY[4:0]	GTIOCnA Output Rising Edge Delay Setting	b4 b0 0 0 0 0 0: Delay on rising edges is not applied 0 0 0 0 1: Delay of 1/32 times PCLKD period applied 0 0 0 1 0: Delay of 2/32 times PCLKD period applied 0 0 0 1 1: Delay of 3/ 32 times PCLKD period applied 0 0 1 0 0: Delay of 4/ 32 times PCLKD period applied 0 0 1 0 1: Delay of 5/ 32 times PCLKD period applied 0 0 1 1 0: Delay of 6/ 32 times PCLKD period applied 0 0 1 1 1: Delay of 7/ 32 times PCLKD period applied 0 1 0 0 0: Delay of 8/ 32 times PCLKD period applied 0 1 0 0 1: Delay of 9/ 32 times PCLKD period applied 0 1 0 1 0: Delay of 10/ 32 times PCLKD period applied 0 1 0 1 1: Delay of 11/ 32 times PCLKD period applied 0 1 1 0 0: Delay of 12/ 32 times PCLKD period applied 0 1 1 0 1: Delay of 13/ 32 times PCLKD period applied 0 1 1 1 0: Delay of 14/ 32 times PCLKD period applied 0 1 1 1 1: Delay of 15/ 32 times PCLKD period applied 1 0 0 0 0: Delay of 16/ 32 times PCLKD period applied 1 0 0 0 1: Delay of 17/ 32 times PCLKD period applied 1 0 0 1 0: Delay of 18/ 32 times PCLKD period applied 1 0 0 1 1: Delay of 19/ 32 times PCLKD period applied 1 0 1 0 0: Delay of 20/ 32 times PCLKD period applied 1 0 1 0 1: Delay of 21/ 32 times PCLKD period applied 1 0 1 1 0: Delay of 22/ 32 times PCLKD period applied 1 0 1 1 1: Delay of 23/ 32 times PCLKD period applied 1 1 0 0 0: Delay of 24/ 32 times PCLKD period applied 1 1 0 0 1: Delay of 25/ 32 times PCLKD period applied 1 1 0 1 0: Delay of 26/ 32 times PCLKD period applied 1 1 0 1 1: Delay of 27/ 32 times PCLKD period applied 1 1 1 0 0: Delay of 28/ 32 times PCLKD period applied 1 1 1 0 1: Delay of 29/ 32 times PCLKD period applied 1 1 1 1 0: Delay of 30/ 32 times PCLKD period applied 1 1 1 1 1: Delay of 31/ 32 times PCLKD period applied.	R/W
b15 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The GTDLYRnA register sets a delay to be applied to rising edges of output signals on the GTIOCnA pin. On the timing for the transfer of settings, see section 24.3.2, Timing for Transfer of GTDLYRnA, GTLDYRnB, GTDLYFnA, and GTDLYFnB Register Settings.

GTDLYRnA can be written when register write protection is disabled (GPT32EHn.GTWP.WP = 0).

24.2.3 GTIOCnA上升沿输出延迟寄存器(GTDLYRnA)(n=0to3)

Address(es): GPT_ODC.GTDLYR0A 4007 B018h, GPT_ODC.GTDLYR1A 4007 B01Ch, GPT_ODC.GTDLYR2A 4007 B020h, GPT_ODC.GTDLYR3A 4007 B024h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	DLY[4:0]				
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b4 to b0	DLY[4:0]	GTIOCnA输出上升边沿延迟设置	b4b000000：不应用上升沿延迟00001：应用延迟132倍PCLKD周期00010：应用延迟232倍PCLKD周期00011：延迟332倍PCLKD周期应用00100：延迟432倍PCLKD周期应用00101：延迟532倍PCLKD周期应用00110：延迟632倍PCLKD周期应用00111：延迟732倍PCLKD周期01000：延迟832倍PCLKD周期01001：延迟932倍PCLKD周期01010：延迟10应用32倍PCLKD周期01011：延迟11应用32倍PCLKD周期01100：延迟12应用32倍PCLKD周期01101：延迟13应用32倍PCLKD周期01110：延迟1432倍PCLKD周期01111：延迟1532倍PCLKD周期10000：延迟1632倍PCLKD周期10001：延迟1732倍应用PCLKD周期10010：延迟1832倍PCLKD周期应用10011：延迟1932倍PCLKD周期应用10100：延迟2032倍PCLKD周期应用10101：延迟2132倍PCLKD周期应用10110:延迟2232倍PCLKD周期10111:延迟2332倍PCLKD周期11000:延迟2432倍PCLKD周期11001:延迟2532倍PCLKD周期应用11010：应用2632倍PCLKD周期的延迟11011：应用2732倍PCLKD周期的延迟11100：应用2832倍PCLKD周期的延迟11101：延迟2932倍PCLKD周期应用11110：延迟3032倍PCLKD周期应用11111：延迟3132倍PCLKD周期应用。	R/W
b15 to b5	—	Reserved	这些位被读取为0。写入值应为0。	R/W

GTDLYRnA寄存器设置延迟应用于GTIOCnA引脚上输出信号的上升沿。关于设置传送的时序，请参阅第24.3.2节，传送GTDLYRnA、GTLDYRnB、GTDLYFnA和GTDLYFnB寄存器设置的时序。

当寄存器写保护被禁用（GPT32EHn.GTWP.WP=0）时，可以写入GTDLYRnA。

24.2.4 GTIOCnA Falling Output Delay Register (GTDLYFnA) (n = 0 to 3)

Address(es): GPT_ODC.GTDLYF0A 4007 B028h, GPT_ODC.GTDLYF1A 4007 B02Ch, GPT_ODC.GTDLYF2A 4007 B030h, GPT_ODC.GTDLYF3A 4007 B034h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	DLY[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b4 to b0	DLY[4:0]	GTIOCnA Output Falling Edge Delay Setting	b4 b0 0 0 0 0 0: Delay on falling edges is not applied 0 0 0 0 1: Delay of 1/32 times PCLKD period applied 0 0 0 1 0: Delay of 2/32 times PCLKD period applied 0 0 0 1 1: Delay of 3/ 32 times PCLKD period applied 0 0 1 0 0: Delay of 4/ 32 times PCLKD period applied 0 0 1 0 1: Delay of 5/ 32 times PCLKD period applied 0 0 1 1 0: Delay of 6/ 32 times PCLKD period applied 0 0 1 1 1: Delay of 7/ 32 times PCLKD period applied 0 1 0 0 0: Delay of 8/ 32 times PCLKD period applied 0 1 0 0 1: Delay of 9/ 32 times PCLKD period applied 0 1 0 1 0: Delay of 10/ 32 times PCLKD period applied 0 1 0 1 1: Delay of 11/ 32 times PCLKD period applied 0 1 1 0 0: Delay of 12/ 32 times PCLKD period applied 0 1 1 0 1: Delay of 13/ 32 times PCLKD period applied 0 1 1 1 0: Delay of 14/ 32 times PCLKD period applied 0 1 1 1 1: Delay of 15/ 32 times PCLKD period applied 1 0 0 0 0: Delay of 16/ 32 times PCLKD period applied 1 0 0 0 1: Delay of 17/ 32 times PCLKD period applied 1 0 0 1 0: Delay of 18/ 32 times PCLKD period applied 1 0 0 1 1: Delay of 19/ 32 times PCLKD period applied 1 0 1 0 0: Delay of 20/ 32 times PCLKD period applied 1 0 1 0 1: Delay of 21/ 32 times PCLKD period applied 1 0 1 1 0: Delay of 22/ 32 times PCLKD period applied 1 0 1 1 1: Delay of 23/ 32 times PCLKD period applied 1 1 0 0 0: Delay of 24/ 32 times PCLKD period applied 1 1 0 0 1: Delay of 25/ 32 times PCLKD period applied 1 1 0 1 0: Delay of 26/ 32 times PCLKD period applied 1 1 0 1 1: Delay of 27/ 32 times PCLKD period applied 1 1 1 0 0: Delay of 28/ 32 times PCLKD period applied 1 1 1 0 1: Delay of 29/ 32 times PCLKD period applied 1 1 1 1 0: Delay of 30/ 32 times PCLKD period applied 1 1 1 1 1: Delay of 31/ 32 times PCLKD period applied.	R/W
b15 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The GTDLYFnA register sets a delay to be applied to falling edges of output signals on the GTIOCnA pin. On the timing for the transfer of settings, see section 24.3.2, Timing for Transfer of GTDLYRnA, GTLDYRnB, GTDLYFnA, and GTDLYFnB Register Settings.

GTDLYFnA can be written when register write protection is disabled (GPT32EHn.GTWP.WP = 0).

24.2.4 GTIOCnA下降输出延迟寄存器(GTDLYFnA)(n=0to3)

Address(es): GPT_ODC.GTDLYF0A 4007 B028h, GPT_ODC.GTDLYF1A 4007 B02Ch, GPT_ODC.GTDLYF2A 4007 B030h, GPT_ODC.GTDLYF3A 4007 B034h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	DLY[4:0]				
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b4 to b0	DLY[4:0]	GTIOCnA输出下降边沿延迟设置	b4b000000：不应用下降沿延迟00001：应用延迟132倍PCLKD周期00010：应用延迟232倍PCLKD周期00011：延迟332倍PCLKD周期应用00100：延迟432倍PCLKD周期应用00101：延迟532倍PCLKD周期应用00110：延迟632倍PCLKD周期应用00111：延迟732倍PCLKD周期01000：延迟832倍PCLKD周期01001：延迟932倍PCLKD周期01010：延迟10应用32倍PCLKD周期01011：延迟11应用32倍PCLKD周期01100：延迟12应用32倍PCLKD周期01101：延迟13应用32倍PCLKD周期01110：延迟1432倍PCLKD周期01111：延迟1532倍PCLKD周期10000：延迟1632倍PCLKD周期10001：延迟1732倍应用PCLKD周期10010：延迟1832次应用PCLKD周期10011：应用延迟1932倍PCLKD周期应用10100：应用延迟2032倍PCLKD周期10101：应用延迟2132倍PCLKD周期10110:延迟2232倍PCLKD周期10111:延迟2332倍PCLKD周期11000:延迟2432倍PCLKD周期11001:延迟2532倍PCLKD周期应用11010：应用2632倍PCLKD周期的延迟11011：应用2732倍PCLKD周期的延迟11100：应用2832倍PCLKD周期的延迟11101：延迟2932倍PCLKD周期应用11110：延迟3032倍PCLKD周期应用11111：延迟3132倍PCLKD周期应用。	R/W
b15 to b5	—	Reserved	这些位被读取为0。写入值应为0。	R/W

GTDLYFnA寄存器设置延迟应用于GTIOCnA引脚上输出信号的下降沿。关于设置传送的时序，请参阅第24.3.2节，传送GTDLYRnA、GTLDYRnB、GTDLYFnA和GTDLYFnB寄存器设置的时序。

当寄存器写保护被禁用（GPT32EHn.GTWP.WP=0）时，可以写入GTDLYFnA。

24.2.5 GTIOCnB Rising Output Delay Register (GTDLYRnB) (n = 0 to 3)

Address(es): GPT_ODC.GTDLYR0B 4007 B01Ah, GPT_ODC.GTDLYR1B 4007 B01Eh, GPT_ODC.GTDLYR2B 4007 B022h, GPT_ODC.GTDLYR3B 4007 B026h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	DLY[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b4 to b0	DLY[4:0]	GTIOCnB Output Rising Edge Delay Setting	b4 b0 0 0 0 0 0: Do not apply delay on rising edges is not applied 0 0 0 0 1: Delay of 1/32 times PCLKD period applied 0 0 0 1 0: Delay of 2/32 times PCLKD period applied 0 0 0 1 1: Delay of 3/ 32 times PCLKD period applied 0 0 1 0 0: Delay of 4/ 32 times PCLKD period applied 0 0 1 0 1: Delay of 5/ 32 times PCLKD period applied 0 0 1 1 0: Delay of 6/ 32 times PCLKD period applied 0 0 1 1 1: Delay of 7/ 32 times PCLKD period applied 0 1 0 0 0: Delay of 8/ 32 times PCLKD period applied 0 1 0 0 1: Delay of 9/ 32 times PCLKD period applied 0 1 0 1 0: Delay of 10/ 32 times PCLKD period applied 0 1 0 1 1: Delay of 11/ 32 times PCLKD period applied 0 1 1 0 0: Delay of 12/ 32 times PCLKD period applied 0 1 1 0 1: Delay of 13/ 32 times PCLKD period applied 0 1 1 1 0: Delay of 14/ 32 times PCLKD period applied 0 1 1 1 1: Delay of 15/ 32 times PCLKD period applied 1 0 0 0 0: Delay of 16/ 32 times PCLKD period applied 1 0 0 0 1: Delay of 17/ 32 times PCLKD period applied 1 0 0 1 0: Delay of 18/ 32 times PCLKD period applied 1 0 0 1 1: Delay of 19/ 32 times PCLKD period applied 1 0 1 0 0: Delay of 20/ 32 times PCLKD period applied 1 0 1 0 1: Delay of 21/ 32 times PCLKD period applied 1 0 1 1 0: Delay of 22/ 32 times PCLKD period applied 1 0 1 1 1: Delay of 23/ 32 times PCLKD period applied 1 1 0 0 0: Delay of 24/ 32 times PCLKD period applied 1 1 0 0 1: Delay of 25/ 32 times PCLKD period applied 1 1 0 1 0: Delay of 26/ 32 times PCLKD period applied 1 1 0 1 1: Delay of 27/ 32 times PCLKD period applied 1 1 1 0 0: Delay of 28/ 32 times PCLKD period applied 1 1 1 0 1: Delay of 29/ 32 times PCLKD period applied 1 1 1 1 0: Delay of 30/ 32 times PCLKD period applied 1 1 1 1 1: Delay of 31/ 32 times PCLKD period applied.	R/W
b15 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The GTDLYRnB register sets a delay to be applied to rising edges of output signals on the GTIOCnB pin. On the timing for the transfer of settings, see section 24.3.2, Timing for Transfer of GTDLYRnA, GTLDYRnB, GTDLYFnA, and GTDLYFnB Register Settings.

GTDLYRnB can be written when register write protection is disabled (GPT32EHn.GTWP.WP = 0).

24.2.5 GTIOCnB上升沿输出延迟寄存器(GTDLYRnB)(n=0to3)

Address(es): GPT_ODC.GTDLYR0B 4007 B01Ah, GPT_ODC.GTDLYR1B 4007 B01Eh, GPT_ODC.GTDLYR2B 4007 B022h, GPT_ODC.GTDLYR3B 4007 B026h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	DLY[4:0]				
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b4 to b0	DLY[4:0]	GTIOCnB输出上升边沿延迟设置	b4b000000：在上升沿不应用延迟不应用00001：应用132倍PCLKD周期的延迟00010：应用232倍PCLKD周期的延迟00011：延迟332倍PCLKD周期00100：延迟432倍PCLKD周期00101：延迟532倍PCLKD周期00110：延迟632倍PCLKD周期应用00111：延迟732倍PCLKD周期应用01000：延迟832倍PCLKD周期应用01001：延迟932倍PCLKD周期应用01010：延迟1032倍PCLKD周期01011：延迟1132倍PCLKD周期01100：延迟1232倍PCLKD周期01101：延迟1332倍PCLKD周期01110：延迟1432倍PCLKD周期01111：延迟1532倍PCLKD周期10000：延迟1632倍PCLKD周期10001：延迟1732次PCLKD周期应用10010：延迟1832倍PCLKD周期应用10011：延迟1932倍PCLKD周期应用10100：20延迟32倍PCLKD周期应用10101：21延迟32倍PCLKD周期应用10110：延迟2232倍PCLKD周期10111：延迟2332倍PCLKD周期11000：延迟2432倍PCLKD周期11001：延迟2532应用PCLKD周期11010：延迟26应用PCLKD周期32倍11011：延迟27应用PCLKD周期32倍11100：应用延迟2832倍PCLKD周期11101：延迟2932倍PCLKD周期11110：延迟3032倍PCLKD周期11111：延迟3132倍PCLKD周期。	R/W
b15 to b5	—	Reserved	这些位被读取为0。写入值应为0。	R/W

GTDLYRnB寄存器设置延迟应用于GTIOCnB引脚上输出信号的上升沿。关于设置传送的时序，请参阅第24.3.2节，传送GTDLYRnA、GTLDYRnB、GTDLYFnA和GTDLYFnB寄存器设置的时序。

当寄存器写保护被禁用（GPT32EHn.GTWP.WP=0）时，可以写入GTDLYRnB。

24.2.6 GTIOCnB Falling Output Delay Register (GTDLYFnB) (n = 0 to 3)

Address(es): GPT_ODC.GTDLYF0B 4007 B02Ah, GPT_ODC.GTDLYF1B 4007 B02Eh, GPT_ODC.GTDLYF2B 4007 B032h, GPT_ODC.GTDLYF3B 4007 B036h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	DLY[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b4 to b0	DLY[4:0]	GTIOCnB Output Falling Edge Delay Setting	b4 b0 0 0 0 0 0: Delay on falling edges is not applied 0 0 0 0 1: Delay of 1/32 times PCLKD period applied 0 0 0 1 0: Delay of 2/32 times PCLKD period applied 0 0 0 1 1: Delay of 3/ 32 times PCLKD period applied 0 0 1 0 0: Delay of 4/ 32 times PCLKD period applied 0 0 1 0 1: Delay of 5/ 32 times PCLKD period applied 0 0 1 1 0: Delay of 6/ 32 times PCLKD period applied 0 0 1 1 1: Delay of 7/ 32 times PCLKD period applied 0 1 0 0 0: Delay of 8/ 32 times PCLKD period applied 0 1 0 0 1: Delay of 9/ 32 times PCLKD period applied 0 1 0 1 0: Delay of 10/ 32 times PCLKD period applied 0 1 0 1 1: Delay of 11/ 32 times PCLKD period applied 0 1 1 0 0: Delay of 12/ 32 times PCLKD period applied 0 1 1 0 1: Delay of 13/ 32 times PCLKD period applied 0 1 1 1 0: Delay of 14/ 32 times PCLKD period applied 0 1 1 1 1: Delay of 15/ 32 times PCLKD period applied 1 0 0 0 0: Delay of 16/ 32 times PCLKD period applied 1 0 0 0 1: Delay of 17/ 32 times PCLKD period applied 1 0 0 1 0: Delay of 18/ 32 times PCLKD period applied 1 0 0 1 1: Delay of 19/ 32 times PCLKD period applied 1 0 1 0 0: Delay of 20/ 32 times PCLKD period applied 1 0 1 0 1: Delay of 21/ 32 times PCLKD period applied 1 0 1 1 0: Delay of 22/ 32 times PCLKD period applied 1 0 1 1 1: Delay of 23/ 32 times PCLKD period applied 1 1 0 0 0: Delay of 24/ 32 times PCLKD period applied 1 1 0 0 1: Delay of 25/ 32 times PCLKD period applied 1 1 0 1 0: Delay of 26/ 32 times PCLKD period applied 1 1 0 1 1: Delay of 27/ 32 times PCLKD period applied 1 1 1 0 0: Delay of 28/ 32 times PCLKD period applied 1 1 1 0 1: Delay of 29/ 32 times PCLKD period applied 1 1 1 1 0: Delay of 30/ 32 times PCLKD period applied 1 1 1 1 1: Delay of 31/ 32 times PCLKD period applied.	R/W
b15 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The GTDLYFnB register sets a delay to be applied to falling edges of output signals on the GTIOCnB pin. On the timing for the transfer of settings, see section 24.3.2, Timing for Transfer of GTDLYRnA, GTLDYRnB, GTDLYFnA, and GTDLYFnB Register Settings.

GTDLYFnB can be written when register write protection is disabled (GPT32EHn.GTWP.WP = 0).

24.3 Operation

24.3.1 Adjustments to the Timing of Rising and Falling Edges in PWM Waveforms

The timing of rising and falling edges in PWM waveforms which are output from the GTIOCnA and GTIOCnB pins, where n = channel number, can be delayed to an accuracy of 1/32 of the GPT operating clock (PCLKD) period.

If the timing of rising or falling edges in PWM waveforms output from the GTIOCnA and GTIOCnB pins must be adjusted, initialize the PWM generation circuit as shown in the procedure in Figure 24.2.

24.2.6 GTIOCnB下降输出延迟寄存器(GTDLYFnB)(n=0to3)

Address(es): GPT_ODC.GTDLYF0B 4007 B02Ah, GPT_ODC.GTDLYF1B 4007 B02Eh, GPT_ODC.GTDLYF2B 4007 B032h, GPT_ODC.GTDLYF3B 4007 B036h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	DLY[4:0]				
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b4 to b0	DLY[4:0]	GTIOCnB输出下降边沿延迟设置	b4b000000：不应用下降沿延迟00001：应用延迟132倍PCLKD周期00010：应用延迟232倍PCLKD周期00011：延迟332倍PCLKD周期应用00100：延迟432倍PCLKD周期应用00101：延迟532倍PCLKD周期应用00110：延迟632倍PCLKD周期应用00111：延迟732倍PCLKD周期01000：延迟832倍PCLKD周期01001：延迟932倍PCLKD周期01010：延迟10应用32倍PCLKD周期01011：延迟11应用32倍PCLKD周期01100：延迟12应用32倍PCLKD周期01101：延迟13应用32倍PCLKD周期01110：延迟1432倍PCLKD周期01111：延迟1532倍PCLKD周期10000：延迟1632倍PCLKD周期10001：延迟1732倍应用PCLKD周期10010：延迟1832次应用PCLKD周期10011：应用延迟1932倍PCLKD周期应用10100：应用延迟2032倍PCLKD周期10101：应用延迟2132倍PCLKD周期10110:延迟2232倍PCLKD周期10111:延迟2332倍PCLKD周期11000:延迟2432倍PCLKD周期11001:延迟2532倍PCLKD周期应用11010：应用2632倍PCLKD周期的延迟11011：应用2732倍PCLKD周期的延迟11100：应用2832倍PCLKD周期的延迟11101：延迟2932倍PCLKD周期应用11110：延迟3032倍PCLKD周期应用11111：延迟3132倍PCLKD周期应用。	R/W
b15 to b5	—	Reserved	这些位被读取为0。写入值应为0。	R/W

GTDLYFnB寄存器设置延迟应用于GTIOCnB引脚上输出信号的下降沿。关于设置传送的时序，请参阅第24.3.2节，传送GTDLYRnA、GTLDYRnB、GTDLYFnA和GTDLYFnB寄存器设置的时序。

当寄存器写保护被禁用（GPT32EHn.GTWP.WP=0）时，可以写入GTDLYFnB。

24.3 Operation

24.3.1 PWM波形上升沿和下降沿时序的调整

从GTIOCnA和GTIOCnB引脚输出的PWM波形的上升沿和下降沿时序（其中n=通道数）可以延迟到GPT工作时钟(PCLKD)周期的1×32的精度。

如果必须调整从GTIOCnA和GTIOCnB引脚输出的PWM波形的上升沿或下降沿时序，请按照图24.2中的步骤初始化PWM生成电路。

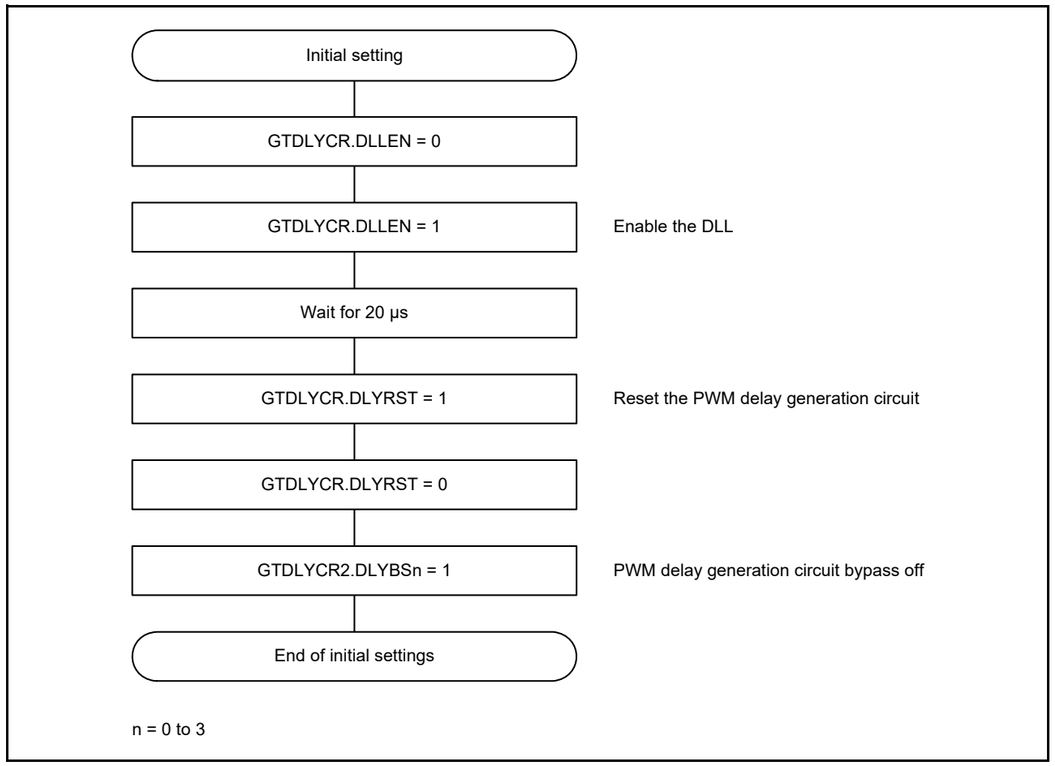


Figure 24.2 Example of initialization flow for the PWM delay generation circuit

In the PWM delay generation circuit, delay can be applied to rising and falling edges of the PWM output to an accuracy of 1/32 of the period of the GPT operation clock (PCLKD). This is described in section 23.3.3, PWM Output Operating Mode. Delays associated with the settings are reflected in the PWM output with the timing described in section 24.3.2, Timing for Transfer of GTDLYRnA, GTLDYRnB, GTDLYFnA, and GTDLYFnB Register Settings. Table 24.3 shows the association between the GTDLYRnA, GTLDYRnB, GTDLYFnA, and GTDLYFnB registers and the PWM outputs.

Table 24.3 Association between PWM output pins and delay setting registers

PWM output pin	Rising-edge delay setting register	Falling-edge delay setting register
GTIOC0A	GTDLYR0A	GTDLYF0A
GTIOC0B	GTDLYR0B	GTDLYF0B
GTIOC1A	GTDLYR1A	GTDLYF1A
GTIOC1B	GTDLYR1B	GTDLYF1B
GTIOC2A	GTDLYR2A	GTDLYF2A
GTIOC2B	GTDLYR2B	GTDLYF2B
GTIOC3A	GTDLYR3A	GTDLYF3A
GTIOC3B	GTDLYR3B	GTDLYF3B

When the PWM delay generation circuit is in use, the timing with which a PWM output signal rises and falls can be controlled to an accuracy of 1/32 of the period of the GPT operation clock (PCLKD). When this option is not in use, the period of the PWM output waveform is controlled to an accuracy of one period of the input clock for the timer counter, which is PCLKD. With the PWM delay generation circuit, the output can be controlled to an accuracy 32 times better. Additionally, the delay settings also control the periods at high and low level for the PWM waveform to the given accuracy. PWM delay generation circuit channels can be individually enabled or disabled.

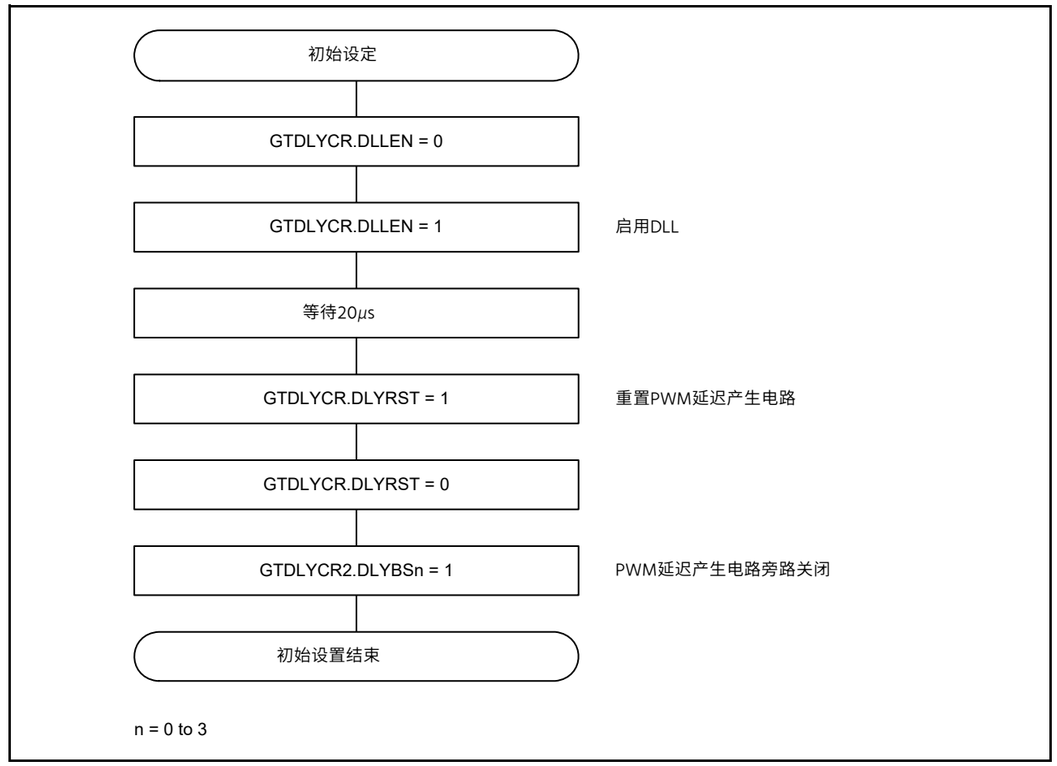


Figure 24.2 PWM延迟产生电路的初始化流程示例

在PWM延迟生成电路中，可以将延迟应用于PWM输出的上升沿和下降沿，精确到GPT操作时钟(PCLKD)周期的132。这在第23.3.3节“PWM输出操作模式”中进行了描述。与设置相关的延迟反映在PWM输出中，其时序在第24.3.2节“GTDLYRnA、GTLDYRnB、GTDLYFnA和GTDLYFnB寄存器设置的传输时序”中描述。表24.3显示了GTDLYRnA、GTLDYRnB、GTDLYFnA和GTDLYFnB寄存器与PWM输出之间的关联。

Table 24.3 PWM输出引脚和延迟设置寄存器之间的关联

PWM输出引脚	上升沿延迟设置寄存器	下降沿延迟设置寄存器
GTIOC0A	GTDLYR0A	GTDLYF0A
GTIOC0B	GTDLYR0B	GTDLYF0B
GTIOC1A	GTDLYR1A	GTDLYF1A
GTIOC1B	GTDLYR1B	GTDLYF1B
GTIOC2A	GTDLYR2A	GTDLYF2A
GTIOC2B	GTDLYR2B	GTDLYF2B
GTIOC3A	GTDLYR3A	GTDLYF3A
GTIOC3B	GTDLYR3B	GTDLYF3B

当使用PWM延迟产生电路时，PWM输出信号的上升和下降的时序可以控制在GPT操作时钟(PCLKD)周期的1×32的精度。不使用此选项时，PWM输出波形的周期被控制为定时器计数器输入时钟（即PCLKD）的一个周期的精度。使用PWM延迟产生电路，可以将输出控制精度提高32倍。此外，延迟设置还控制PWM波形的高电平和低电平周期，以达到给定的精度。PWM延迟生成电路通道可以单独启用或禁用。

24.3.2 Timing for Transfer of GTDLYRnA, GTLDYRnB, GTDLYFnA, and GTDLYFnB Register Settings

Settings for the GTDLYRnA, GTLDYRnB, GTDLYFnA, and GTDLYFnB registers are initially transferred to temporary registers, and then reflected in the delay on the GTIOCnA and GTIOCnB (n = 0 to 3) outputs. Transfer of the settings takes place on overflows (in up-counting) or underflows (in down-counting) for saw waves, and in the troughs of triangle waves.

Figure 24.3 and Figure 24.4 show examples of the operation of the GTDLYR0A and GTDLYF0A registers.

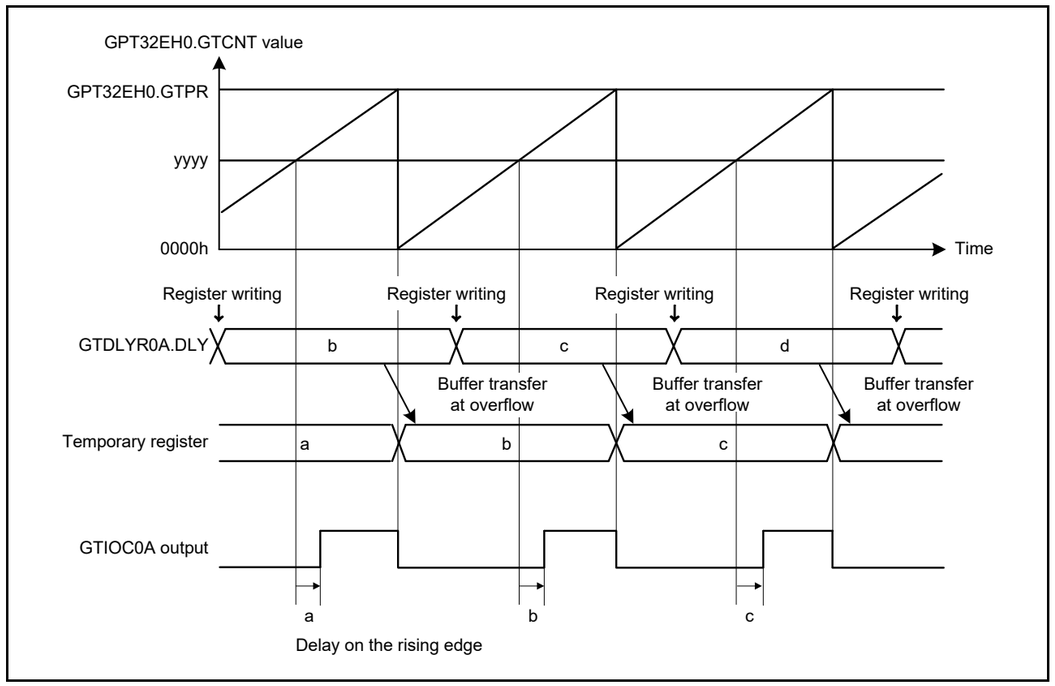


Figure 24.3 Example of GTLDYR0A register operation with PWM saw-wave generation

24.3.2 GTDLYRnA、GTLDYRnB、GTDLYFnA和GTDLYFnB的传输时间注册设置

GTDLYRnA、GTLDYRnB、GTDLYFnA和GTDLYFnB寄存器的设置最初传送到临时寄存器，然后反映在GTIOCnA和GTIOCnB（n=0到3）输出的延迟中。设置的传输发生在锯齿波的上溢（向上计数）或下溢（向下计数）以及三角波的波谷中。

图24.3和图24.4显示了GTDLYR0A和GTDLYF0A寄存器的操作示例。

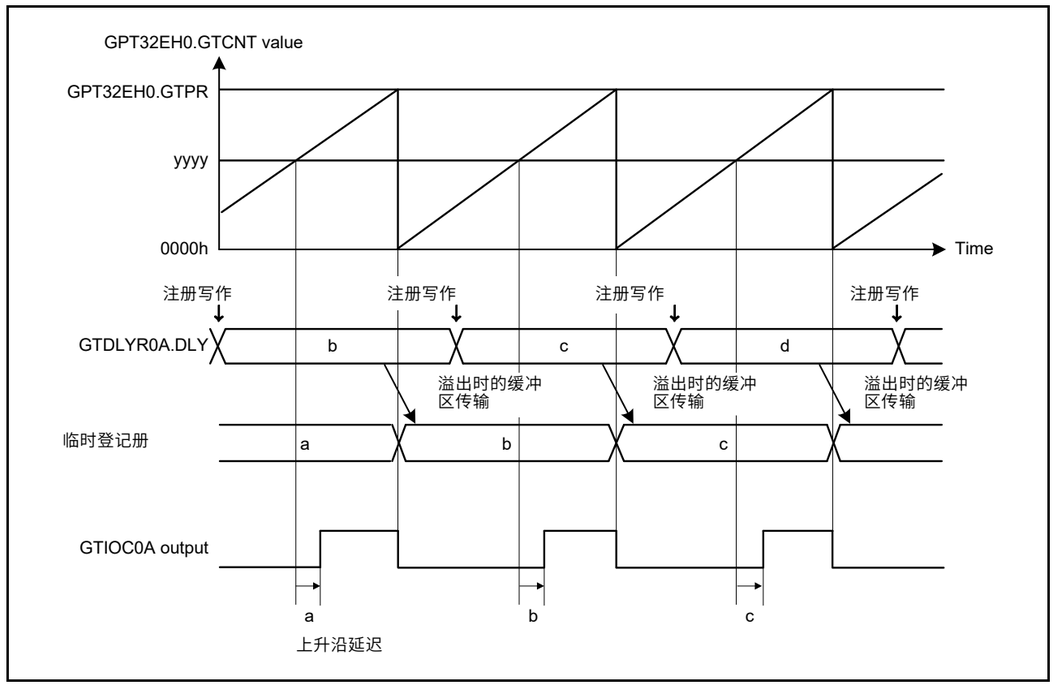


Figure 24.3 带有PWM锯齿波生成的GTLDYR0A寄存器操作示例

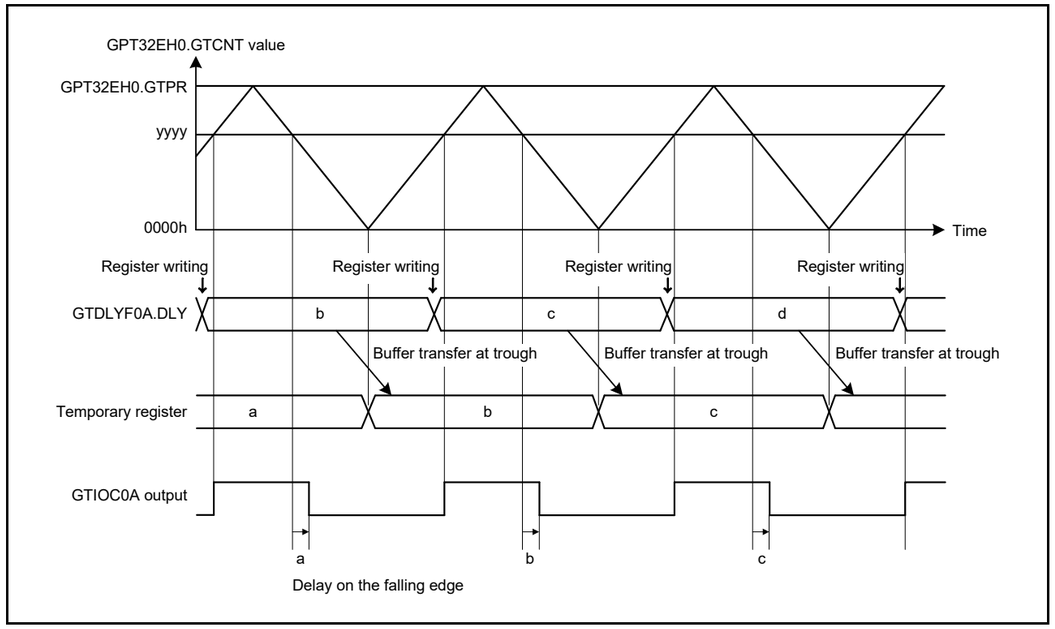


Figure 24.4 Example of GTLDYF0A register operation with PWM triangle-wave generation

24.4 Usage Notes

24.4.1 Settings for the Module-Stop Function

The Module Stop Control Register D (MSTPCRD) can enable or disable operation of the PWM delay generation circuit. The PWM delay generation circuit is initially stopped after reset. Releasing the module-stop state enables access to the registers. For details, see section 11, Low Power Modes.

24.4.2 Notes on Delay Settings for PWM Delay Generation Circuit

When the PWM delay generation circuit generates delays for a PWM output waveform and the waveform is toggled in response to compare-matches, do not change the settings for delay while the compare-match value is within the ranges listed in Table 24.4. This constraint applies to the GTDLYFnA, GTDLYRnA, GTDLFnB, and GTDLYRnB registers.

Table 24.4 Constraints on delay settings

Mode	Direction of counting	Compare-match value
Saw-wave mode	Up	GTPR - 2 or above
	Down	2 or below
Triangle-wave mode	Down	2 or below

Figure 24.5 shows an example of how the constraints apply to the timing of setting GTDLYFnA in saw-wave waveform one-shot pulse mode (counting up). Do not change the value set in GTDLYFnA while GTCCRD ≥ GTPR - 2.

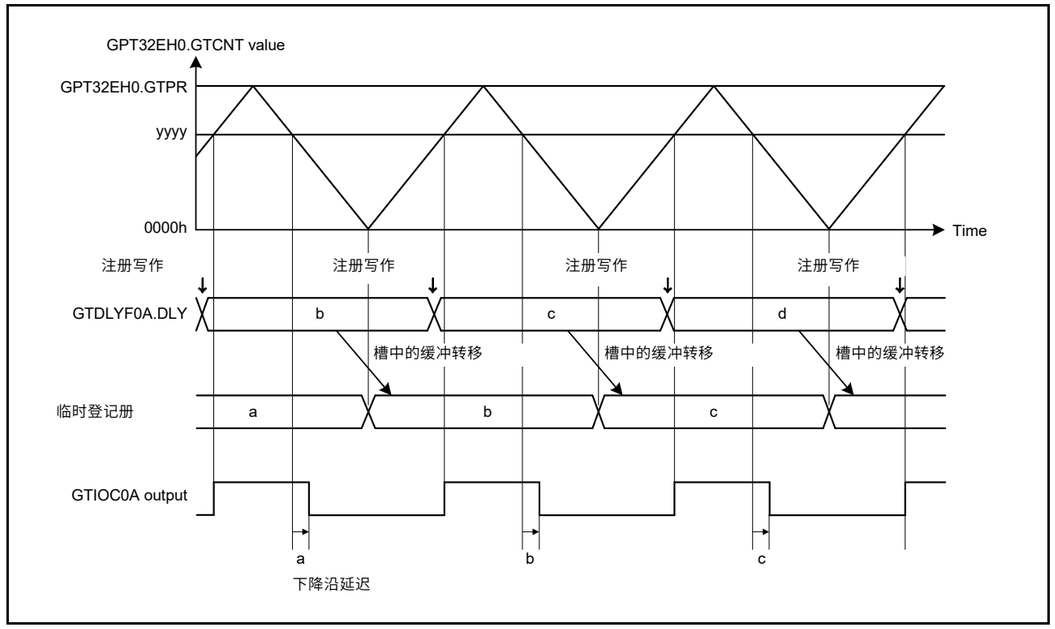


Figure 24.4 带有PWM三角波生成的GTLDYF0A寄存器操作示例

24.4 使用说明

24.4.1 模块停止功能的设置

模块停止控制寄存器D(MSTPCRD)可以启用或禁用PWM延迟生成电路的操作。PWM延迟产生电路在复位后最初停止。释放模块停止状态可以访问寄存器。有关详细信息，请参阅第11节，低功耗模式。

24.4.2 PWM延迟产生电路的延迟设置注意事项

当PWM延迟生成电路为PWM输出波形产生延迟并且波形响应比较匹配而切换时，当比较匹配值在表24.4中列出的范围内时，请勿更改延迟设置。此约束适用于GTDLYFnA、GTDLYRnA、GTDLFnB和GTDLYRnB寄存器。

Table 24.4 延迟设置的限制

Mode	计数方向	Compare-match value
Saw-wave mode	Up	GTPR2或以上
	Down	2或以下
Triangle-wave mode	Down	2或以下

图24.5显示了约束如何应用于在锯波波形单次脉冲模式（向上计数）中设置GTDLYFnA的时序的示例。当GTCCRD≥GTPR2时，请勿更改GTDLYFnA中设置的值。

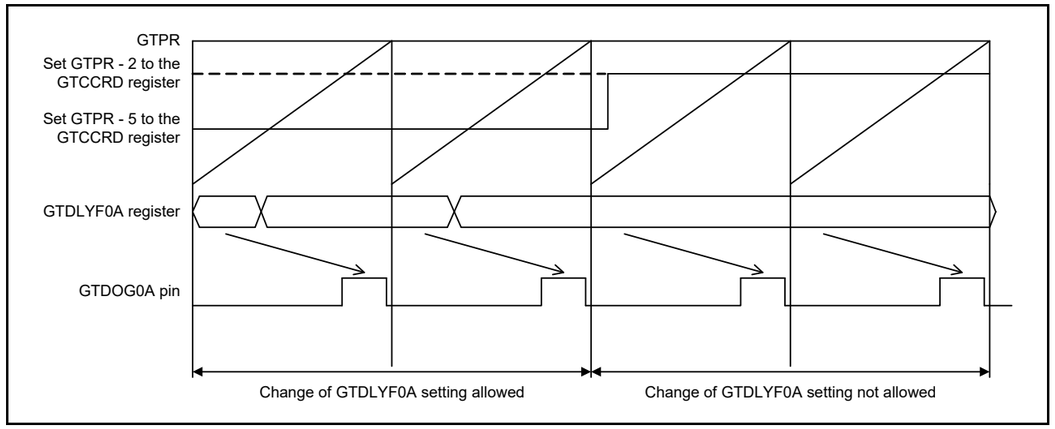


Figure 24.5 Constraints on the timing of GTDLYF0A register settings

Changing the values in the GTDLYFnA, GTDLYRnA, GTDLYFnB, and GTDLYRnB registers during periods where changes to settings are not allowed, might lead to faulty output waveforms such as shifts in the timing of output waveform transitions from the expected values.

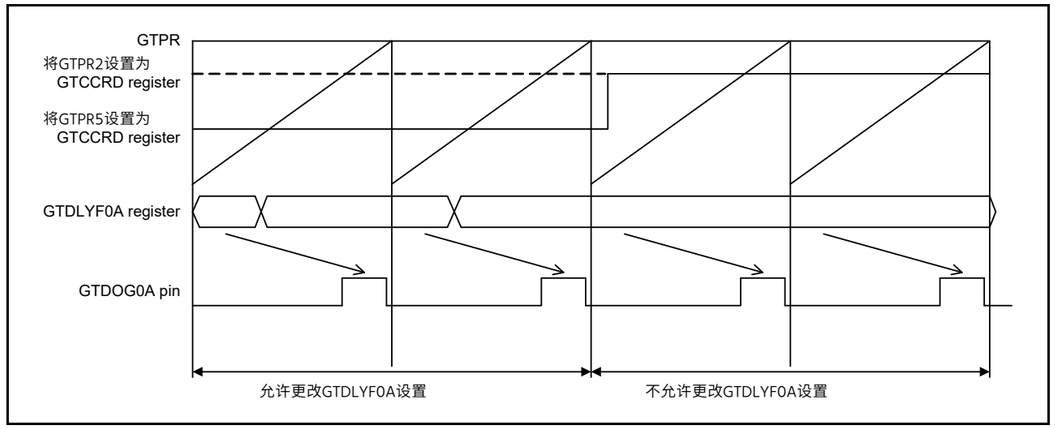


Figure 24.5 GTDLYF0A寄存器设置的时序约束

在不允许更改设置的期间更改GTDLYFnA、GTDLYRnA、GTDLYFnB和GTDLYRnB寄存器中的值可能会导致错误的输出波形，例如输出波形转换的时序偏离预期值。

25. Asynchronous General-Purpose Timer (AGT)

25.1 Overview

The Asynchronous General-Purpose Timer (AGT) is a 16-bit timer that can be used for pulse output, external pulse width or period measurement, and counting external events.

This 16-bit timer consists of a reload register and a down counter. The reload register and the down counter are allocated in the same address, and can be accessed with the AGT register.

Table 25.1 lists the AGT specifications, Figure 25.1 shows a block diagram, and Table 25.2 lists the I/O pins.

Table 25.1 AGT specifications

Parameter		Specifications
Operating modes	Timer mode	The count source is counted
	Pulse output mode	The count source is counted and the output is inverted at each timer underflow
	Event counter mode	An external event is counted
	Pulse width measurement mode	An external pulse width is measured
	Pulse period measurement mode	An external pulse period is measured
Count source (Operating clock)*2		PCLKB, PCLKB/2, PCLKB/8, AGTLCLK, AGTLCLK/2, AGTLCLK/4, AGTLCLK/8, AGTLCLK/16, AGTLCLK/32, AGTLCLK/64, AGTLCLK/128, AGTSCLK, AGTSCLK/2, AGTSCLK/4, AGTSCLK/8, AGTSCLK/16, AGTSCLK/32, AGTSCLK/64, AGTSCLK/128, or underflow signal of AGT0*1 selectable.
Interrupt/Event link function (Output)		• Underflow event signal or measurement complete event signal – When the counter underflows – When the measurement of the active width of the external input (AGTIO) is complete in pulse width measurement mode – When the set edge of the external input (AGTIO) is input in pulse period measurement mode • Compare match A event signal – When the values of AGT and AGTCMA matched (Compare match A function enabled) • Compare match B event signal – When the values of AGT and AGTCMB matched (Compare match B function enabled).
Selectable functions		• Compare match function One or two of the compare match A and B registers is selectable.

Note 1. AGT0 cannot use the AGT0 underflow signal. AGT1 connects directly with the underflow event signal from the AGT0 timer.
Note 2. Satisfy the frequency of the peripheral module clock (PCLKB) ≥ the frequency of the count source clock.

25. 异步通用定时器(AGT)

25.1 Overview

异步通用定时器(AGT)是一个16位定时器，可用于脉冲输出、外部脉冲宽度或周期测量以及外部事件计数。

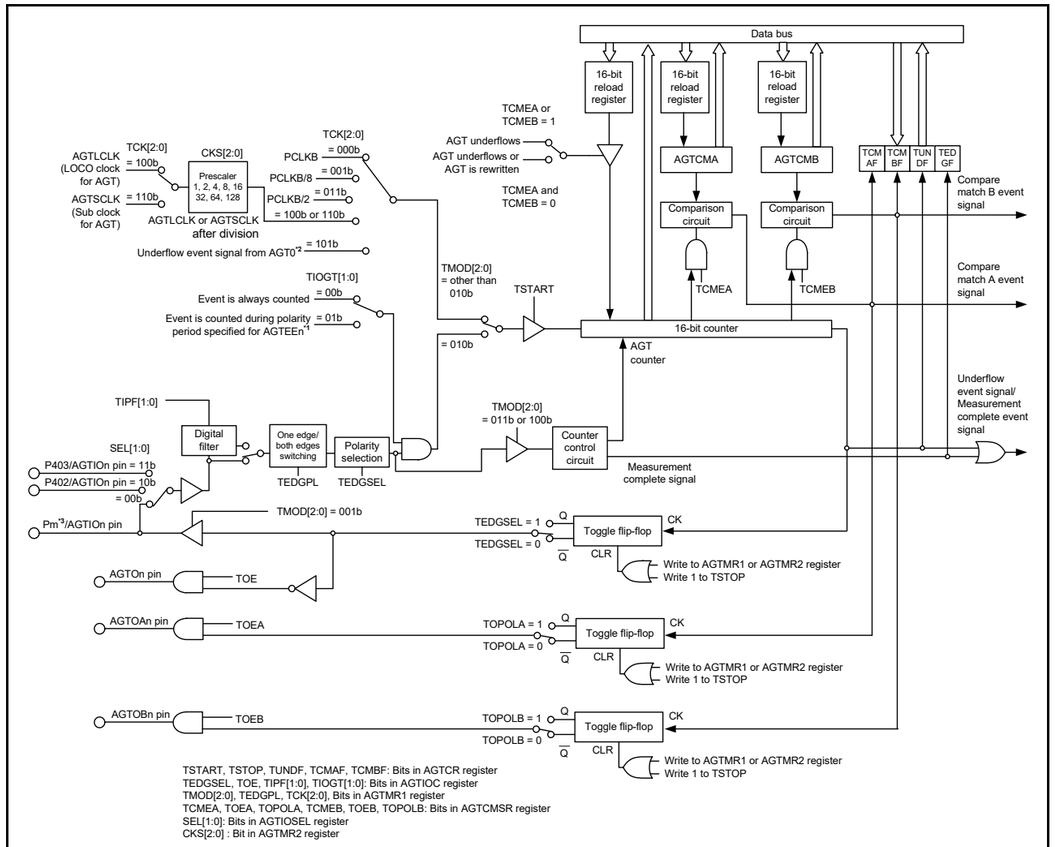
这个16位定时器由一个重载寄存器和一个递减计数器组成。重载寄存器和递减计数器分配在同一个地址，可以通过AGT寄存器访问。

表25.1列出了AGT规格，图25.1显示了框图，表25.2列出了IO引脚。

Table 25.1 AGT specifications

Parameter		Specifications
操作模式	定时器模式	计数源被计数
	脉冲输出方式	计数源被计数并在每次定时器下溢时反转输出
	事件计数器模式	计算外部事件
	脉宽测量模式	测量外部脉冲宽度
	脉冲周期测量模式	测量外部脉冲周　　期
计数源（工作时钟）*2		PCLKB, PCLKB/2, PCLKB/8, AGTLCLK, AGTLCLK/2, AGTLCLK/4, AGTLCLK/8, AGTLCLK/16, AGTLCLK/32, AGTLCLK/64, AGTLCLK/128, AGTSCLK, AGTSCLK/2, AGTSCLK/4, AGTSCLK/8, AGTSCLK/16, AGTSCLK32、AGTSCLK64、AGTSCLK128或AGT0*1的下溢信号可选。
中断事件链接功能（输出）		下溢事件信号或测量完成事件信号　当计数器下溢时　当外部输入(AGTIO)的有效宽度测量在脉冲宽度测量模式下完成时　当输入外部输入(AGTIO)的设置边沿时在脉冲周期测量模式　比较匹配A事件信号 当AGT和AGTCMA的值匹配时（启用比较匹配A功能）　比较匹配B事件信号 当AGT和AGTCMB的值匹配时（启用比较匹配B功能）。
可选择的功能		比较匹配功能 一个或两个比较匹配A和B寄存器是可选择的。

Note 1. AGT0不能使用AGT0下溢信号。AGT1直接与来自AGT0定时器的下溢事件信号相连。
Note 2. 满足外设模块时钟（PCLKB）的频率≥计数源时钟的频率。



Note 1. The polarity can be selected by the EEPS bit in the AGTISR register.
Note 2. AGT0 cannot use AGT underflow event. AGT1 uses the underflow of AGT0.
Note 3. m = 100, 301, 407, and 705 (AGT0), m = 204, 400, and 901 (AGT1).

Figure 25.1 AGT block diagram

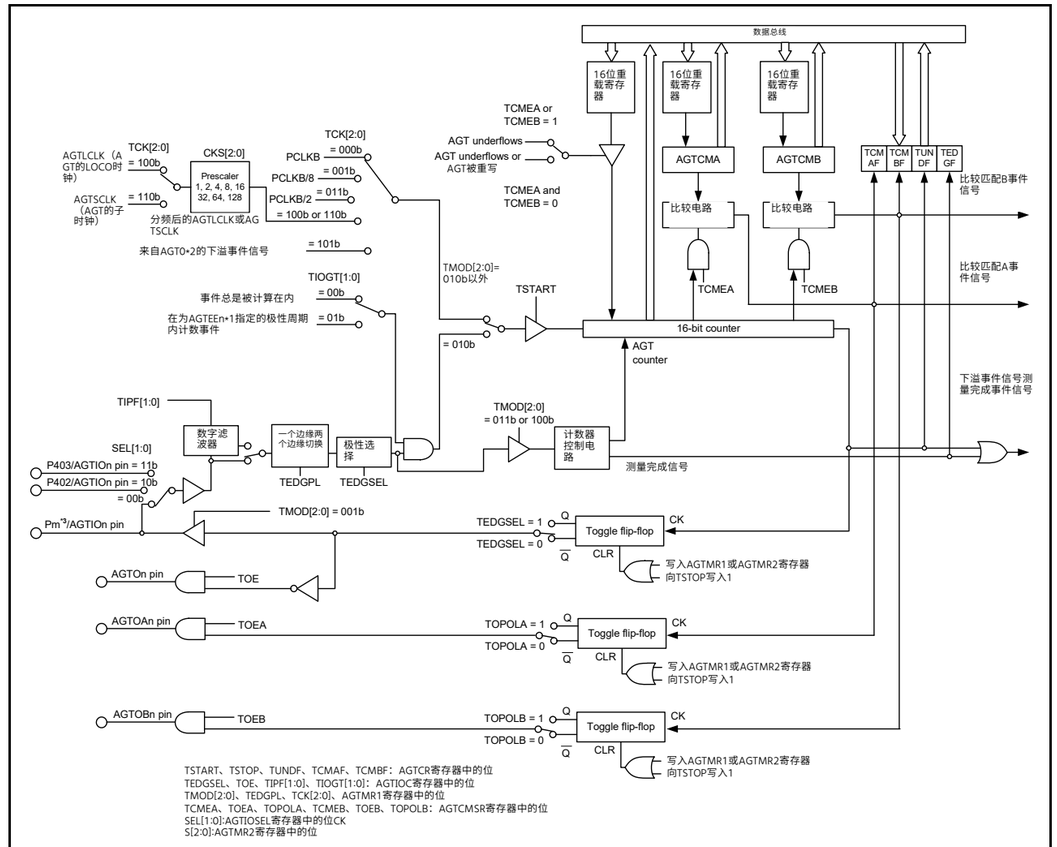
Table 25.2 AGT I/O pins

Pin name	I/O	Function
AGTEEn	Input	External event input for AGT
AGTIOn*1	Input*1/output	External event input and pulse output for AGT
AGTOn	Output	Pulse output for AGT
AGTOAn	Output	Output compare match A output for AGT
AGTOBn	Output	Output compare match B output for AGT

Note: Channel number (n = 0, 1).
Note 1. AGTIO can also be used in Deep Software Standby mode.

AGTIO can be controlled by the VBTICTLR register.

For more information, see section 12.2.2, VBATT Input Control Register (VBTICTLR) and section 20.5.5, I/O Buffer Specification.



注1.可以通过AGTISR寄存器中的EEPS位选择极性。注2.AGT0不能使用AGT下溢事件。AGT1使用AGT0的下溢。
注3.m=100、301、407和705(AGT0)，m=204、400和901(AGT1)。

Figure 25.1 AGT框图

Table 25.2 AGT I/O pins

引脚名称	I/O	Function
AGTEEn	Input	AGT的外部事件输入
AGTIOn*1	Input*1/output	AGT的外部事件输入和脉冲输出
AGTOn	Output	AGT的脉冲输出
AGTOAn	Output	输出比较匹配AGT的输出
AGTOBn	Output	AGT的输出比较匹配B输出

Note: 通道号(n=0 1)。
Note 1. AGTIO也可用于深度软件待机模式。

AGTIO可由VBTICTLR寄存器控制。

有关详细信息，请参阅第12.2.2节，VBATT输入控制寄存器(VBTICTLR)和第20.5.5节，IO缓冲区Specification.

25.2 Register Descriptions

25.2.1 AGT Counter Register (AGT)

Address(es): AGT0.AGT 4008 4000h, AGT1.AGT 4008 4100h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Description	Setting range	R/W
b15 to b0	16-bit counter and reload register *1, *2	0000h to FFFFh	R/W

Note 1. When 1 is written to the TSTOP bit in the AGTCR register, the 16-bit counter is forcibly stopped and set to FFFFh.
Note 2. When the TCK[2:0] bit setting in the AGTMR1 register is other than 001b (PCLKB/8) or 011b (PCLKB/2), if the AGT register is set to 0000h, a request signal to the ICU, the DTC, and the ELC is generated once immediately after the count starts. The AGTOn and AGTIOn outputs are toggled.
When the AGT register is set to 0000h in event counter mode, regardless of the value of bits TCK[2:0], a request signal to the ICU, the DTC, and the ELC is generated once immediately after the count starts.
In addition, the AGTOn output toggles even during a period other than the specified count period. When the AGT register is set to 0001h or more, a request signal is generated each time AGT underflows.

AGT is a 16-bit register. The write value is written to the reload register and the read value is read from the counter.

The states of the reload register and the counter change according to the TSTART bit in the AGTCR register and TCMEA/TCMEB bit in the AGTCMSR register. For details, see section 25.3.1, Reload Register and Counter Rewrite Operation. The AGT register can be set with a 16-bit memory manipulation instruction.

25.2.2 AGT Compare Match A Register (AGTCMA)

Address(es): AGT0.AGTCMA 4008 4002h, AGT1.AGTCMA 4008 4102h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Description	Setting range	R/W
b15 to b0	16-bit compare match A data is stored.*1	0000h to FFFFh	R/W

Note 1. Set the AGTCMA register to FFFFh when the compare match A is not used.

The AGTCMA register is a read/write register to set a value for compare match with the AGT counter. The states of the reload register and compare register A change according to the TSTART bit in the AGTCR register. For details, see section 25.3.2, Reload Register and Compare Register A/B Rewrite Operation. The AGTCMA register can be set by a 16-bit memory manipulation instruction.

25.2 注册说明

25.2.1 AGT计数器寄存器(AGT)

Address(es): AGT0.AGT 4008 4000h, AGT1.AGT 4008 4100h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Description	设定范围	R/W
b15 to b0	16位计数器和重载寄存器*1 *2	0000h to FFFFh	R/W

Note 1. 当AGTCR寄存器的TSTOP位写入1时，16位计数器被强制停止并设置为FFFFh。
Note 2. 当AGTMR1寄存器中的TCK[2:0]位设置不是001b(PCLKB8)或011b(PCLKB2)时，如果AGT寄存器设置为0000h，则向ICU、DTC和ELC在计数开始后立即生成一次。AGTOn和AGTIOn输出被切换。

当AGT寄存器在事件计数器模式下设置为0000h时，无论TCK[2:0]位的值如何，都会在计数开始后立即生成一次对ICU、DTC和ELC的请求信号。
此外，即使在指定计数周期以外的周期内，AGTOn输出也会切换。当AGT寄存器设置为0001h或更大时，每次AGT下溢时都会产生一个请求信号。

AGT是一个16位的寄存器。写入值写入重载寄存器，读取值从计数器中读取。

重载寄存器和计数器的状态根据AGTCR寄存器中的TSTART位和AGTCMSR寄存器中的TCMEATCMEB位。有关详细信息，请参阅第25.3.1节，重新加载寄存器和计数器重写手术。AGT寄存器可通过16位存储器操作指令进行设置。

25.2.2 AGT比较匹配A寄存器(AGTCMA)

Address(es): AGT0.AGTCMA 4008 4002h, AGT1.AGTCMA 4008 4102h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Description	设定范围	R/W
b15 to b0	16位比较匹配A数据被存储。*1	0000h to FFFFh	R/W

Note 1. 当不使用比较匹配A时，将AGTCMA寄存器设置为FFFFh。

AGTCMA寄存器是一个读写寄存器，用于设置与AGT计数器比较匹配的值。重载寄存器和比较寄存器A的状态根据AGTCR寄存器中的TSTART位而改变。有关详细信息，请参见第25.3.2节，重载寄存器和比较寄存器AB重写操作。AGTCMA寄存器可以通过16位存储器操作指令设置。

25.2.3 AGT Compare Match B Register (AGTCMB)

Address(es): AGT0.AGTCMB 4008 4004h, AGT1.AGTCMB 4008 4104h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Description	Setting range	R/W
b15 to b0	16-bit compare match B data is stored.*1	0000h to FFFFh	R/W

Note 1. Set the AGTCMB register to FFFFh when compare match B is not used.

The AGTCMB register is a read/write register to set a value for compare match with the AGT counter. The states of the reload register and compare register B change in accordance with the TSTART bit in the AGTCR register. For details, see section 25.3.2, Reload Register and Compare Register A/B Rewrite Operation. The AGTCMB register can be set by a 16-bit memory manipulation instruction.

25.2.4 AGT Control Register (AGTCR)

Address(es): AGT0.AGTCR 4008 4008h, AGT1.AGTCR 4008 4108h

	b7	b6	b5	b4	b3	b2	b1	b0
	TCMBF	TCMAF	TUNDF	TEDGF	—	TSTOP	TCSTF	TSTART
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	TSTART	AGT Count Start*2	0: Count stops 1: Count starts.	R/W
b1	TCSTF	AGT Count Status Flag*2	0: Count stopped 1: Count in progress.	R
b2	TSTOP	AGT Count Forced Stop*1	0: Writing is invalid 1: The count is forcibly stopped.	W
b3	—	Reserved	The read value is 0. The write value should be 0.	R/W
b4	TEDGF	Active Edge Judgment Flag	0: No active edge received 1: Active edge received.	R/(W)*3
b5	TUNDF	Underflow Flag	0: No underflow 1: Underflow.	R/(W)*3
b6	TCMAF	Compare Match A Flag	0: No match 1: Match.	R/(W)*3
b7	TCMBF	Compare Match B Flag	0: No match 1: Match.	R/(W)*3

Note 1. When 1 (count is forcibly stopped) is written to the TSTOP bit, the TSTART and TCSTF bits are initialized at the same time. The pulse output level is also initialized. The read value is 0.
Note 2. For information on using the TSTART and TCSTF bits, see section 25.4.1, Count Operation Start and Stop Control.
Note 3. Only 0 can be written to clear the flag.

TSTART bit (AGT Count Start)

The count operation is started by writing 1 to the TSTART bit and stopped by writing 0. When this bit is set to 1, the TCSTF bit is set to 1 (count in progress) in synchronization with the count source. Also, after 0 is written to the TSTART bit, the TCSTF bit is set to 0 (count stopped) in synchronization with the count source. For details, see section 25.4.1, Count Operation Start and Stop Control.

25.2.3 AGT比较匹配B寄存器(AGTCMB)

Address(es): AGT0.AGTCMB 4008 4004h, AGT1.AGTCMB 4008 4104h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Bit	Description	设定范围	R/W
b15 to b0	存储16位比较匹配B数据。*1	0000h to FFFFh	R/W

Note 1. 当不使用比较匹配B时，将AGTCMB寄存器设置为FFFFh。

AGTCMB寄存器是一个读写寄存器，用于设置与AGT计数器比较匹配的值。重载寄存器和比较寄存器B的状态根据AGTCR寄存器中的TSTART位变化。有关详细信息，请参见第25.3.2节，重载寄存器和比较寄存器AB重写操作。AGTCMB寄存器可以通过16位存储器操作指令设置。

25.2.4 AGT控制寄存器(AGTCR)

Address(es): AGT0.AGTCR 4008 4008h, AGT1.AGTCR 4008 4108h

	b7	b6	b5	b4	b3	b2	b1	b0
	TCMBF	TCMAF	TUNDF	TEDGF	—	TSTOP	TCSTF	TSTART
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	TSTART	AGT计数开始 *2	0：计数停止1 ：计数开始。	R/W
b1	TCSTF	AGT计数状态 Flag*2	0：计数停止1：计数进行中。	R
b2	TSTOP	AGT计数强制 Stop*1	0：写入无效1：强制停止计数。	W
b3	—	Reserved	读取值为0。写入值应为0。	R/W
b4	TEDGF	主动边缘判断 Flag	0：未收到有效边沿1：收到有效边沿。	R/(W)*3
b5	TUNDF	Underflow Flag	0: No underflow 1: Underflow.	R/(W)*3
b6	TCMAF	比较匹配标志	0：不匹配1 ：匹配。	R/(W)*3
b7	TCMBF	比较匹配B标志	0：不匹配1 ：匹配。	R/(W)*3

Note 1. 当1（强制停止计数）写入TSTOP位时，TSTART和TCSTF位同时初始化。
脉冲输出电平也被初始化。读取值为0。
Note 2. 有关使用TSTART和TCSTF位的信息，请参见第25.4.1节，计数操作开始和停止控制。
Note 3. 只能写入0来清除标志。

TSTART位（AGT计数开始）

通过向TSTART位写入1开始计数操作，通过写入0停止计数操作。当该位设置为1时，TCSTF位与计数源同步设置为1（正在进行计数）。此外，在TSTART位写入0后，TCSTF位与计数源同步设置为0（计数停止）。有关详细信息，请参见第25.4.1节，计数操作开始和停止控制。

TCSTF flag (AGT Count Status Flag)

The TCSTF flag indicates the AGT count status.

[Setting condition]

- When 1 is written to the TSTART bit (the TCSTF flag is set to 1 in synchronization with the count source).

[Clearing conditions]

- When 0 is written to the TSTART bit (the TCSTF flag is set to 0 in synchronization with the count source)
- When 1 is written to the TSTOP bit.

TSTOP bit (AGT Count Forced Stop)

When 1 is written to the TSTOP bit, the count is forcibly stopped. The read value is 0.

TEDGF flag (Active Edge Judgment Flag)

The TEDGF flag indicates that an active edge was detected.

[Setting condition]

- When the measurement of the active width of the external input (AGTIO) is complete in pulse width measurement mode.
- When the set edge of the external input (AGTIO) is input in pulse period measurement mode

[Clearing condition]

- When 0 is written to this flag by a program.

TUNDF flag (Underflow Flag)

The TUNDF flag indicates that the counter underflowed.

[Setting condition]

- When the counter underflows.

[Clearing condition]

- When 0 is written to this flag by software.

TCMAF flag (Compare Match A Flag)

The TCMAF flag indicates that compare match A was detected.

[Setting condition]

- When the value in the AGT register matches the value in the AGTCMA register.

[Clearing condition]

- When 0 is written to this flag by software.

TCMBF flag (Compare Match B Flag)

The TCMBF flag indicates that compare match B was detected.

[Setting condition]

- When the value in the AGT register matches the value in the AGTCMB register.

[Clearing condition]

- When 0 is written to this flag by software.

TCSTF标志（AGT计数状态标志）

TCSTF标志指示AGT计数状态。

[Setting condition]

- 当1写入TSTART位时（TCSTF标志设置为1与计数源同步）。

[Clearing conditions]

- 当0写入TSTART位时（TCSTF标志设置为0与计数源同步）
- 当1写入TSTOP位时。

TSTOP位（AGT计数强制停止）

向TSTOP位写入1时，强制停止计数。读取值为0。

TEDGF标志（活动边缘判断标志）

TEDGF标志表示检测到有效边沿。

[Setting condition]

- 在脉冲宽度测量模式下完成外部输入(AGTIO)的有效宽度测量时。
- 在脉冲周期测量模式下输入外部输入(AGTIO)的设置边沿时

[Clearing condition]

- 当程序向该标志写入0时。

TUNDF flag (Underflow Flag)

TUNDF标志指示计数器下溢。

[Setting condition]

- 当计数器下溢时。

[Clearing condition]

- 当软件向该标志写入0时。

TCMAF标志（比较匹配A标志）

TCMAF标志表示检测到比较匹配A。

[Setting condition]

- 当AGT寄存器中的值与AGTCMA寄存器中的值匹配时。

[Clearing condition]

- 当软件向该标志写入0时。

TCMBF标志（比较匹配B标志）

TCMBF标志表示检测到比较匹配B。

[Setting condition]

- 当AGT寄存器中的值与AGTCMB寄存器中的值匹配时。

[Clearing condition]

- 当软件向该标志写入0时。

25.2.5 AGT Mode Register 1 (AGTMR1)

Address(es): AGT0.AGTMR1 4008 4009h, AGT1.AGTMR1 4008 4109h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	TCK[2:0]			TEDGPL	TMOD[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	TMOD[2:0]	Operating Mode*3	b2 b0 0 0 0: Timer mode 0 0 1: Pulse output mode 0 1 0: Event counter mode 0 1 1: Pulse width measurement mode 1 0 0: Pulse period measurement mode. Other settings are prohibited.	R/W
b3	TEDGPL	Edge Polarity*4	0: Single-edge 1: Both-edge.	R/W
b6 to b4	TCK[2:0]	Count Source*1, *2, *5	b6 b4 0 0 0: PCLKB 0 0 1: PCLKB/8 0 1 1: PCLKB/2 1 0 0: Divided clock AGTLCLK specified in CKS[2:0] bits in AGTMR2 register 1 0 1: Underflow event signal from AGT0*6 1 1 0: Divided clock AGTSCLK specified in CKS[2:0] bits in AGTMR2 register. Other settings are prohibited.	R/W
b7	—	Reserved	The read value is 0. The write value should be 0.	R/W

Note: Write access to the AGTMR1 register initializes the output from the AGTOn, AGTIOn, AGTOAn and AGTOBn pins of the AGT (n = 0, 1). For details on the output level at initialization, see the description of section 25.2.7, AGT I/O Control Register (AGTIOC).

Note 1. When event counter mode is selected, the external input (AGTIOn) is selected as the count source regardless of the setting of TCK[2:0] bits.

Note 2. Do not switch count sources during count operation. Only switch count sources when both the TSTART and TCSTF bits in the AGTCR register are set to 0 (count is stopped).

Note 3. The operating mode can only be changed when the count is stopped while both the TSTART and TCSTF bits in the AGTCR register are set to 0 (count is stopped). Do not change the operating mode during count operation.

Note 4. The TEDGPL bit is enabled only in event counter mode.

Note 5. When running AGT in Software Standby and Deep Software Standby modes, set AGTSCLK or AGTLCLK (TCK[2:0] = 100b or 110b) as the count source.

Note 6. AGT0 cannot use AGT0 underflow (setting prohibited). AGT1 uses the underflow of AGT0.

25.2.5 AGT模式寄存器1(AGTMR1)

Address(es): AGT0.AGTMR1 4008 4009h, AGT1.AGTMR1 4008 4109h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	TCK[2:0]			TEDGPL	TMOD[2:0]		
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b2 to b0	TMOD[2:0]	Operating Mode*3	b2b0000：定时器模式001：脉冲输出模式010：事件计数器模式011：脉冲宽度测量模式100：脉冲周期测量模式。禁止其他设置。	R/W
b3	TEDGPL	Edge Polarity*4	0: Single-edge 1: Both-edge.	R/W
b6 to b4	TCK[2:0]	Count Source*1, *2, *5	b6b4000：PCLKB001：PCLKB8011：PCLKB2100：分频时钟AGTLCLK在AGTMR2寄存器的CKS[2:0]位中指定101：来自AGT0*的下溢事件信号6110：在AGTMR2寄存器的CKS[2:0]位中指定的分频时钟AGTSCLK。禁止其他设置。	R/W
b7	—	Reserved	读取值为0。写入值应为0。	R/W

Note: 对AGTMR1寄存器的写访问初始化AGT(n=0 1)的AGTOn、AGTIOn、AGTOAn和AGTOBn引脚的输出。有关初始化时输出电平的详细信息，请参见第25.2.7节AGTIO控制寄存器(AGTIOC)的描述。

Note 1. 选择事件计数器模式时，无论设置如何
TCK[2:0] bits.

Note 2. 请勿在计数操作期间切换计数源。只有在TSTART和TCSTF位都在
AGTCR寄存器设置为0（停止计数）。

Note 3. 只有在AGTCR寄存器中的TSTART和TCSTF位都设置为0（计数停止）时停止计数，才能更改操作模式。请勿在计数操作期间更改操作模式。

Note 4. TEDGPL位仅在事件计数器模式下启用。

Note 5. 在软件待机和深度软件待机模式下运行AGT时，将AGTSCLK或AGTLCLK(TCK[2:0]=100b或110b)设置为计数源。

Note 6. AGT0不能使用AGT0下溢（禁止设置）。AGT1使用AGT0的下溢。

25.2.6 AGT Mode Register 2 (AGTMR2)

Address(es): AGT0.AGTMR2 4008 400Ah, AGT1.AGTMR2 4008 410Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	LPM	—	—	—	—	CKS[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	CKS[2:0]	AGTSCLK/AGTLCLK Count Source Clock Frequency Division Ratio *1, *2, *3	b2 b0 0 0 0: 1/1 0 0 1: 1/2 0 1 0: 1/4 0 1 1: 1/8 1 0 0: 1/16 1 0 1: 1/32 1 1 0: 1/64 1 1 1: 1/128.	R/W
b6 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	LPM	Low Power Mode	0: Normal mode 1: Low-power mode.	R/W

Note 1. Do not rewrite CKS[2:0] during count operation. Only rewrite the CKS[2:0] bits when both the TSTART and TCSTF bits in the AGTCR register are set to 0 (count is stopped).
Note 2. When count source is AGTSCLK/AGTLCLK, the switch of CKS[2:0] is valid.
Note 3. Do not switch the TCK[2:0] bits in the AGTMR1 register when CKS[2:0] are not 000b. Switch the TCK[2:0] bits in the AGTMR1 register after CKS[2:0] are set to 000b, and wait for 1 cycle of the count source.

LPM bit (Low Power Mode)

The LPM bit sets the low power operation, which impacts access to certain AGT registers. Set 1 to operate in low power. When this bit is 1, access to the following registers is prohibited:

- AGT/AGTCMA/AGTCMB/AGTCR.

After this bit is switched from 1 to 0, the first access to the register is constrained as follows:

- AGT: Read AGT register twice. Only the second reading of data is valid.
- AGT, AGTCMA, AGTCMB, and AGTCR: Allow at least 2 cycles of the count source clock when writing to the register.

25.2.7 AGT I/O Control Register (AGTIOC)

Address(es): AGT0.AGTIOC 4008 400Ch, AGT1.AGTIOC 4008 410Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	TIOGT[1:0]		TIPF[1:0]		—	TOE	—	TEDGSEL
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	TEDGSEL	I/O Polarity Switch	Function varies depending on the operating mode. See Table 25.3 and Table 25.4. The TEDGSEL bit switches the AGTO output polarity and the AGTIO input/output edge and polarity. In pulse output mode, it only controls the polarity of AGTOn output and AGTIOn output. AGTOn output and AGTIOn output are initialized when the AGTMR1 register is written and the TSTOP bit in the AGTCR register is written with 1.	R/W

25.2.6 AGT模式寄存器2(AGTMR2)

Address(es): AGT0.AGTMR2 4008 400Ah, AGT1.AGTMR2 4008 410Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	LPM	—	—	—	—	CKS[2:0]		
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b2 to b0	CKS[2:0]	AGTSCLKAGTLCLK计数源时钟分频 Ratio *1, *2, *3	b2 b0 0 0 0: 1/1 0 0 1: 1/2 0 1 0: 1/4 0 1 1: 1/8 1 0 0: 1/16 1 0 1: 1/32 1 1 0: 1/64 1 1 1: 1/128.	R/W
b6 to b3	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b7	LPM	低功耗模式	0：正常模式1：低功耗模式。	R/W

Note 1. 在计数操作期间不要重写CKS[2:0]。只有当TSTART和TCSTF位都在AGTCR寄存器设置为0（停止计数）。
Note 2. 当计数源为AGTSCLKAGTLCLK时，CKS[2:0]的开关有效。
Note 3. 当CKS[2:0]不是000b时，不要切换AGTMR1寄存器中的TCK[2:0]位。在CKS[2:0]设置为000b后，切换AGTMR1寄存器中的TCK[2:0]位，并等待计数源的1个周期。

LPM位（低功耗模式）

LPM位设置低功耗操作，这会影响对某些AGT寄存器的访问。设置1以低功率运行。
该位为1时，禁止访问以下寄存器：

- AGT/AGTCMA/AGTCMB/AGTCR.

该位由1变为0后，对寄存器的第一次访问受到如下约束：

- AGT：读取AGT寄存器两次。只有第二次读取数据是有效的。
- AGT、AGTCMA、AGTCMB和AGTCR：写入寄存器时至少允许计数源时钟的2个周期。

25.2.7 AGTIO控制寄存器(AGTIOC)

Address(es): AGT0.AGTIOC 4008 400Ch, AGT1.AGTIOC 4008 410Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	TIOGT[1:0]		TIPF[1:0]		—	TOE	—	TEDGSEL
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	TEDGSEL	IO极性开关	功能因操作模式而异。见表25.3和 Table 25.4. TEDGSEL位切换AGTO输出极性和AGTIO输入输出边沿和极性。在脉冲输出模式下，它只控制AGTOn输出和AGTIon输出的极性。当写入AGTMR1寄存器并将AGTCR寄存器中的TSTOP位写入1时，初始化AGTOn输出和AGTIOn输出。	R/W

Bit	Symbol	Bit name	Description	R/W
b1	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b2	TOE	AGTOn Output Enable	0: AGTOn output disabled 1: AGTOn output enabled.	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b5, b4	TIPF[1:0]	Input Filter*3	b5 b4 0 0: No filter 0 1: Filter sampled at PCLKB 1 0: Filter sampled at PCLKB/8 1 1: Filter sampled at PCLKB/32. These bits specify the sampling frequency of the filter for the AGTIOn input. If the input to the AGTIOn pin is sampled and the value matches three successive times, that value is taken as the input value.	R/W
b7, b6	TIOGT[1:0]	Count Control*1,*2,*4	b7 b6 0 0: Event is always counted 0 1: Event is counted during polarity period specified for AGTEEn. Other settings are prohibited.	R/W

Note 1. When AGTEEn pin is used, the polarity to count an event can be selected with the EEPS bit in the AGTISR register.
Note 2. Bits TIOGT[1:0] are enabled only in event counter mode.
Note 3. When event counter mode operation is performed during Software Standby and Deep Software Standby modes, the digital filter function cannot be used.
Note 4. When using in Deep Software Standby mode, set TIOGT[1:0] = 00b (event is always counted).

Table 25.3 AGTIOn I/O edge and polarity switching

Operating mode	Function
Timer mode	Not used
Pulse output mode	0: Output is started at high (initialization level: high) 1: Output is started at low (initialization level: low).
Event counter mode	0: Count on rising edge 1: Count on falling edge.
Pulse width measurement mode	0: Low-level width is measured 1: High-level width is measured.
Pulse period measurement mode	0: Measure from one rising edge to the next rising edge 1: Measure from one falling edge to the next falling edge.

Table 25.4 AGTOn output polarity switching

Operating mode	Function
All modes	0: Output is started at low (initialization level: low) 1: Output is started at high (initialization level: high).

25.2.8 AGT Event Pin Select Register (AGTISR)

Address(es): AGT0.AGTISR 4008 400Dh, AGT1.AGTISR 4008 410Dh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	EEPS	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b2	EEPS	AGTEEn Polarity Selection	0: An event is counted during the low-level period 1: An event is counted during the high-level period.	R/W

Bit	Symbol	位名称	Description	R/W
b1	—	Reserved	该位读取为0。写入值应为0。	R/W
b2	TOE	AGTOn输出使能	0：禁用AGTOn输出1：启用AGTOn输出。	R/W
b3	—	Reserved	该位读取为0。写入值应为0。	R/W
b5, b4	TIPF[1:0]	Input Filter*3	b5b400：无滤波器01：滤波器在PCLKB1处采样0：滤波器在PCLKB8处采样11：滤波器在PCLKB32处采样。这些位指定AGTIOn输入的滤波器采样频率。如果对AGTIOn引脚的输入进行采样并且值连续匹配3次，则将该值作为输入值。	R/W
b7, b6	TIOGT[1:0]	Count Control*1,*2,*4	b7b600：始终计数事件01：在为AGTEEn指定的极性周期内计数事件。禁止其他设置。	R/W

Note 1. 当使用AGTEEn引脚时，可以通过AGTISR寄存器中的EEPS位选择计数事件的极性。
Note 2. 位TIOGT[1:0]仅在事件计数器模式下启用。
Note 3. 在软件待机和深度软件待机模式期间执行事件计数器模式操作时，不能使用数字滤波器功能。
Note 4. 在深度软件待机模式下使用时，设置TIOGT[1:0]=00b（始终计数事件）。

Table 25.3 AGTIOnIO边沿和极性切换

操作模式	Function
定时器模式	不曾用过
脉冲输出方式	0：高电平开始输出（初始化电平：高电平）1：低电平开始输出（初始化电平：低电平）。
事件计数器模式	0：上升沿计数1：下降沿计数。
脉宽测量模式	0：测量低电平宽度1：测量高电平宽度。
脉冲周期测量模式	0：从一个上升沿测量到下一个上升沿1：从一个下降沿测量到下一个下降沿。

Table 25.4 AGTOn输出极性切换

操作模式	Function
所有模式	0：低电平开始输出（初始化电平：低电平）1：高电平开始输出（初始化电平：高电平）。

25.2.8 AGT事件引脚选择寄存器(AGTISR)

Address(es): AGT0.AGTISR 4008 400Dh, AGT1.AGTISR 4008 410Dh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	EEPS	—	—
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b1, b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b2	EEPS	AGTEEn Polarity Selection	0：在低电平期间计数一个事件1：在高电平期间计数一个事件。	R/W

Bit	Symbol	Bit name	Description	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

25.2.9 AGT Compare Match Function Select Register (AGTCMSR)

Address(es): AGT0.AGTCMSR 4008 400Eh, AGT1.AGTCMSR 4008 410Eh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	TOPOLB	TOEB	TCMEB	—	TOPOLA	TOEA	TCMEA
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	TCMEA	Compare Match A Register Enable*1, *2	0: Compare match A register disabled 1: Compare match A register enabled.	R/W
b1	TOEA	AGTOAn Output Enable*1, *2	0: AGTOAn output disabled 1: AGTOAn output enabled.	R/W
b2	TOPOLA	AGTOAn Polarity Select*1, *2	0: AGTOAn output is started on low 1: AGTOAn output is started on high.	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	TCMEB	Compare Match B Register Enable*1, *2	0: Compare match B register disabled 1: Compare match B register enabled.	R/W
b5	TOEB	AGTOBn Output Enable*1, *2	0: AGTOBn output disabled 1: AGTOBn output enabled.	R/W
b6	TOPOLB	AGTOBn Polarity Select*1, *2	0: AGTOBn output is started on low 1: AGTOBn output is started on high.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Note 1. Do not rewrite the AGTCMSR register during a count operation. Only rewrite the AGTCMSR register when both the TSTART and TCSTF bits in the AGTCR register are set to 0 (count is stopped).
Note 2. Do not set 1 when in pulse width measurement mode or pulse period measurement mode.

25.2.10 AGT Pin Select Register (AGTIOSEL)

Address(es): AGT0.AGTIOSEL 4008 400Fh, AGT1.AGTIOSEL 4008 410Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	TIES	—	—	SEL[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	SEL[1:0]	AGTIO Pin Select*1,*3	b1 b0 0 0: Select Pm*2/AGTIO as AGTIO Pm/AGTIO can not be used as AGTIO input pin in Deep Software Standby mode. 0 1: Setting prohibited 1 0: Select P402/AGTIO as AGTIO P402/AGTIO can be used as AGTIO input pin in Deep Software Standby mode. P402/AGTIOn is input only. It cannot be used for output. 1 1: Select P403/AGTIO as AGTIO. P403/AGTIO can be used as AGTIO input pin in Deep Software Standby mode. P403/AGTIOn is input only. It cannot be used for output.	R/W
b3, b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Bit	Symbol	位名称	Description	R/W
b7 to b3	—	Reserved	这些位被读取为0。写入值应为0。	R/W

25.2.9 AGT比较匹配功能选择寄存器(AGTCSR)

Address(es): AGT0.AGTCMSR 4008 400Eh, AGT1.AGTCMSR 4008 410Eh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	TOPOLB	TOEB	TCMEB	—	TOPOLA	TOEA	TCMEA
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	TCMEA	比较比赛A Register Enable*1, *2	0：比较匹配A寄存器禁用1：比较匹配A寄存器启用。	R/W
b1	TOEA	AGTOAn Output Enable*1, *2	0：禁用AGTOAn输出1：启用AGTOAn输出。	R/W
b2	TOPOLA	AGTOAn Polarity Select*1, *2	0：AGTOAn输出从低电平开始1：AGTOAn输出从高电平开始。	R/W
b3	—	Reserved	该位读取为0。写入值应为0。	R/W
b4	TCMEB	比较比赛B Register Enable*1, *2	0：比较匹配B寄存器禁用1：比较匹配B寄存器启用。	R/W
b5	TOEB	AGTOBn Output Enable*1, *2	0：AGTOBn输出禁用1：AGTOBn输出使能。	R/W
b6	TOPOLB	AGTOBn Polarity Select*1, *2	0：AGTOBn输出从低电平开始1：AGTOBn输出从高电平开始。	R/W
b7	—	Reserved	该位读取为0。写入值应为0。	R/W

Note 1. 在计数操作期间不要重写AGCTMSR寄存器。仅当AGTCR寄存器中的TSTART和TCSTF位都设置为0（计数停止）时才重写AGTCMSR寄存器。
Note 2. 在脉冲宽度测量模式或脉冲周期测量模式下不要设置为1。

25.2.10 AGT引脚选择寄存器(AGTISEL)

Address(es): AGT0.AGTIOSEL 4008 400Fh, AGT1.AGTIOSEL 4008 410Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	TIES	—	—	SEL[1:0]	
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b1, b0	SEL[1:0]	AGTIO Pin Select*1,*3	b1b000：选择Pm*2AGTIO作为AGTIO PmAGTIO不能用作AGTIO输入引脚深度软件待机模式。01：禁止设置1 0：选择P402AGTIO作为AGTIO P402AGTIO可用作深度软件待机模式下的AGTIO输入引脚。P402AGTIOn仅为输入。它不能用于输出。11：选择P403AGTIO作为AGTIO。 P403AGTIO可用作深度软件待机模式下的AGTIO输入引脚。P403AGTION仅为输入。它不能用于输出。	R/W
b3, b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Bit	Symbol	Bit name	Description	R/W
b4	TIES	AGTIO Input Enable	0: External event input is disabled during Software Standby mode 1: External event input is enabled during Software Standby mode.	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. P402/AGTIO and P403/AGTIO can be used as external event input pins for the AGT in Deep Software Standby mode. Pm*2/AGTIO cannot be used as external event input pins for the AGT in Deep Software Standby mode. P402/AGTIO and P403/AGTIO are input only.
When Pm/AGTIO is selected, you must set the Port mn Pin Function Select (PmnPFS) register. See section 20, I/O Ports.
Note 2. m = 100, 301, 407, and 705 (AGT0), m = 204, 400, and 901 (AGT1).
Note 3. When P402/AGTIO and P403/AGTIO are selected, you must set the VBTICTLR register. See section 12, Battery Backup Function.

The AGTIOSEL register sets the AGTIO pin when using the AGTIO in Deep Software Standby mode and Software Standby mode. The AGTIOSEL register can be set with an 8-bit memory manipulation instruction.

SEL[1:0] bits (AGTIO Pin Select*1,*3)

The SEL[1:0] bits select the AGTIO pin function.

TIES bit (AGTIO Input Enable)

The TIES bit enables or disables an external event input.

25.3 Operation

25.3.1 Reload Register and Counter Rewrite Operation

Regardless of the operating mode, the timing of the rewrite operation to the reload register and the counter differs depending on the value of the TSTART bit in the AGTCR register and of the TCMEA or TCMEB bit in the AGTCMSR register. When the TSTART bit is 0 (count stops), the count value is directly written to the reload register and the counter. When the TSTART bit is 1 (count starts) and the TCMEA bit and TCMEB bit are 0 (compare match A/B registers are invalid), the value is written to the reload register in synchronization with the count source, and then to the counter in synchronization with the next count source. When the TSTART bit is 1 (count starts) and the TCMEA bit or TCMEB bit is 1 (compare match A register or compare match B register is valid), the value is written to the reload register in synchronization with the count source, and then to the counter in synchronization with the underflow of the counter.

Figure 25.2 and Figure 25.3 show the timing of rewrite operation with TSTART bit value and TCMEA/TCMEB bit value.

Bit	Symbol	位名称	Description	R/W
b4	TIES	AGTIO输入使能	0：在软件待机模式下禁用外部事件输入1：在软件待机模式下启用外部事件输入。	R/W
b7 to b5	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. P402AGTIO和P403AGTIO可用作深度软件待机模式下AGT的外部事件输入引脚。
Pm*2AGTIO不能用作深度软件待机模式下AGT的外部事件输入引脚。P402AGTIO和P403AGTIO仅为输入。

选择PMAGTIO后，必须设置端口MNPIN函数选择（PMNPFS）寄存器。请参阅第20节，IO端口。
Note 2. m = 100, 301, 407, and 705 (AGT0), m = 204, 400, and 901 (AGT1).
Note 3. WhenP402AGTIOandP403AGTIOareselected youmustsettheVBTICTLRregister.请参阅第12节，备用电池Function.

在深度软件待机模式和软件中使用AGTIO时，AGTIOSEL寄存器设置AGTIO引脚待机模式。AGTIOSEL寄存器可以使用8位存储器操作指令进行设置。

SEL[1:0]位(AGTIO引脚选择*1 *3)

SEL[1:0]位选择AGTIO引脚功能。

TIES位（AGTIO输入使能）

TIES位启用或禁用外部事件输入。

25.3 Operation

25.3.1 重载寄存器和计数器重写操作

无论操作模式如何，对重载寄存器和计数器的重写操作的时序根据AGTCR寄存器中的TSTART位和AGTCMSR寄存器中的TCMEA或TCMEB位的值而有所不同。当TSTART位为0（计数停止）时，计数值直接写入重载寄存器和计数器。当TSTART位为1（计数开始）且TCMEA位和TCMEB位为0（比较匹配AB寄存器无效）时，将值与计数源同步写入重载寄存器，然后同步写入计数器与下一个计数源。当TSTART位为1（计数开始）且TCMEA位或TCMEB位为1（比较匹配A寄存器或比较匹配B寄存器有效）时，该值与计数源同步写入重载寄存器，然后与计数器的下溢同步到计数器。

图25.2和图25.3显示了使用TSTART位值和TCMEATCMEB位值进行重写操作的时序。

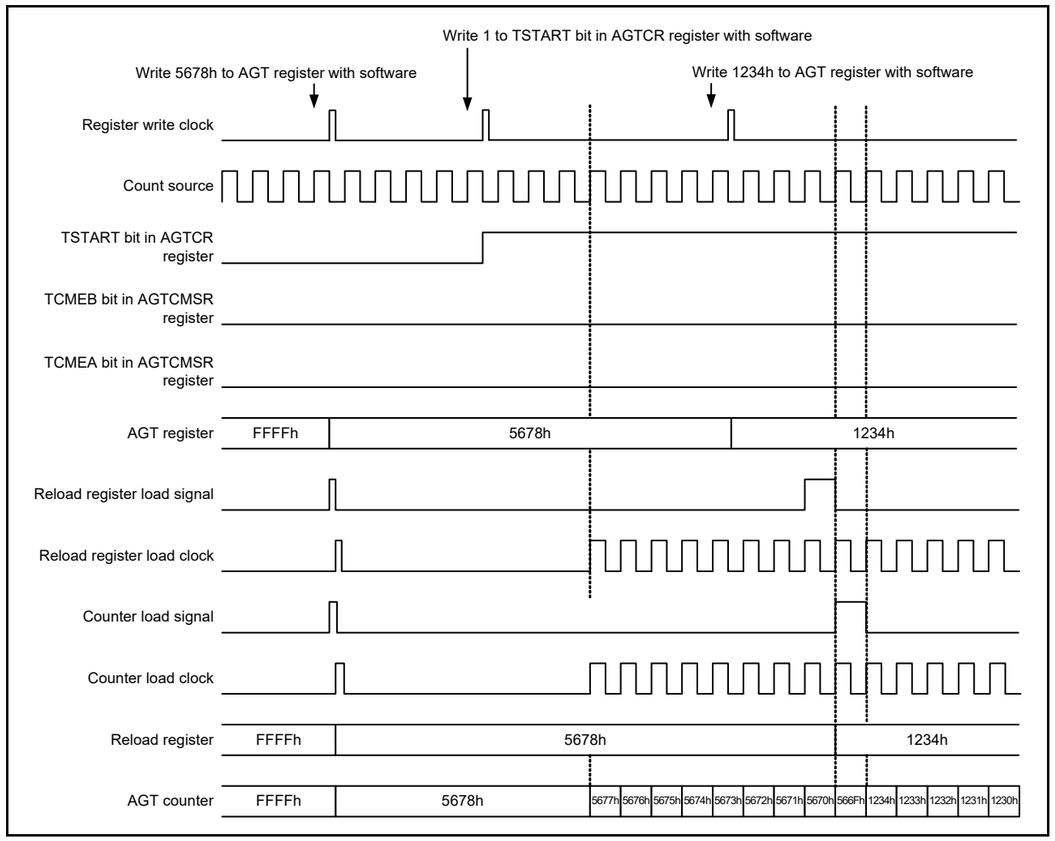


Figure 25.2 Timing of rewrite operation with TSTART bit value and TCMEA and TCMEB bit value when compare match register A and B are invalid

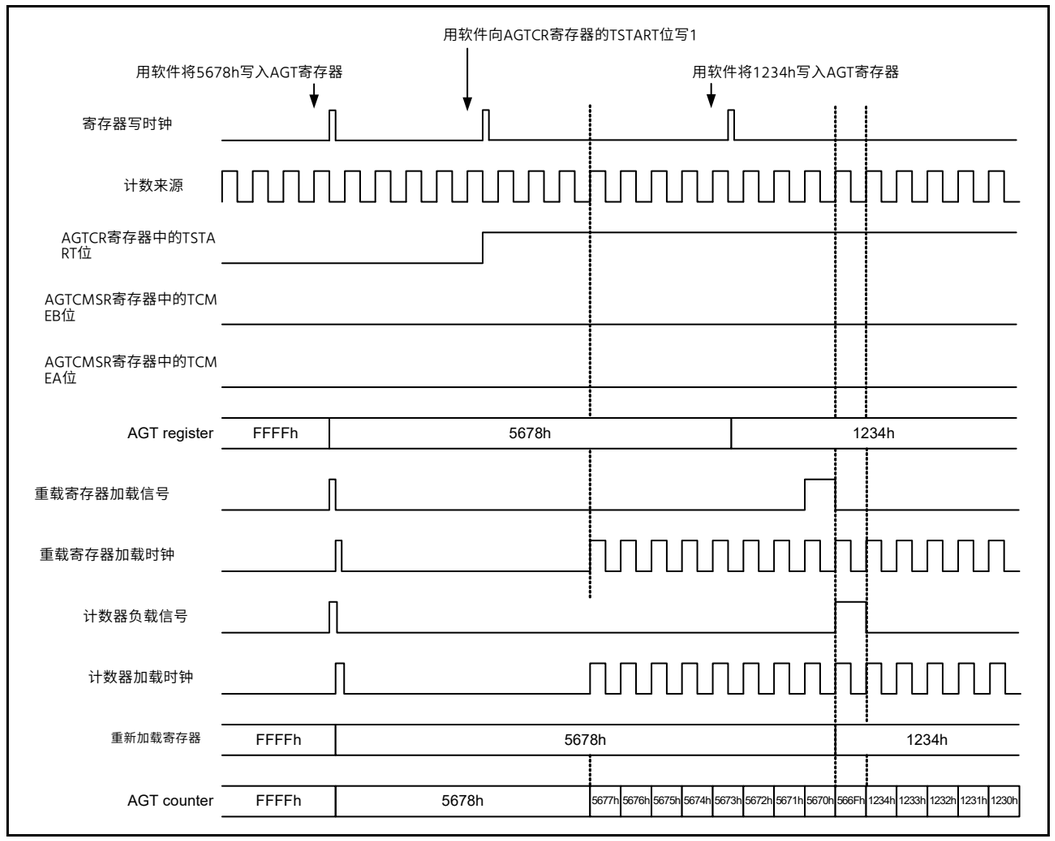


Figure 25.2 比较匹配寄存器A和B无效时用TSTART位值和TCMEA和TCMEB位值重写操作的时序

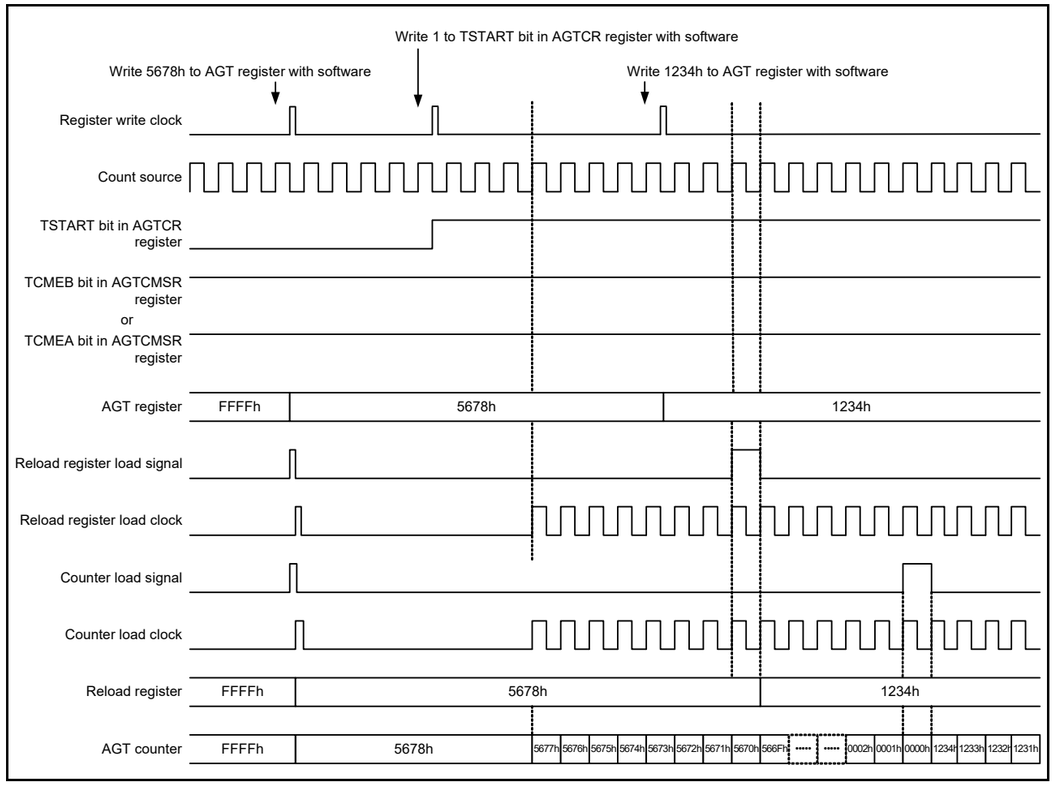


Figure 25.3 Timing of rewrite operation with TSTART bit value and TCMEA or TCMEB bit value when compare match register A or B is valid

25.3.2 Reload Register and Compare Register A/B Rewrite Operation

Regardless of the operating mode, the timing of the rewrite operation to compare register A/B depends on the value of the TSTART bit in the AGTCR register. When the TSTART bit is 0 (count stops), the count value is directly written to the reload register and compare register A/B. When the TSTART bit is 1 (count starts), the value is written to the reload register in synchronization with the count source, and then to the compare register in synchronization with the underflow of the counter.

Figure 25.4 shows the timing of rewrite operation with TSTART bit value for compare register A. Compare register B is of the same timing as compare register A.

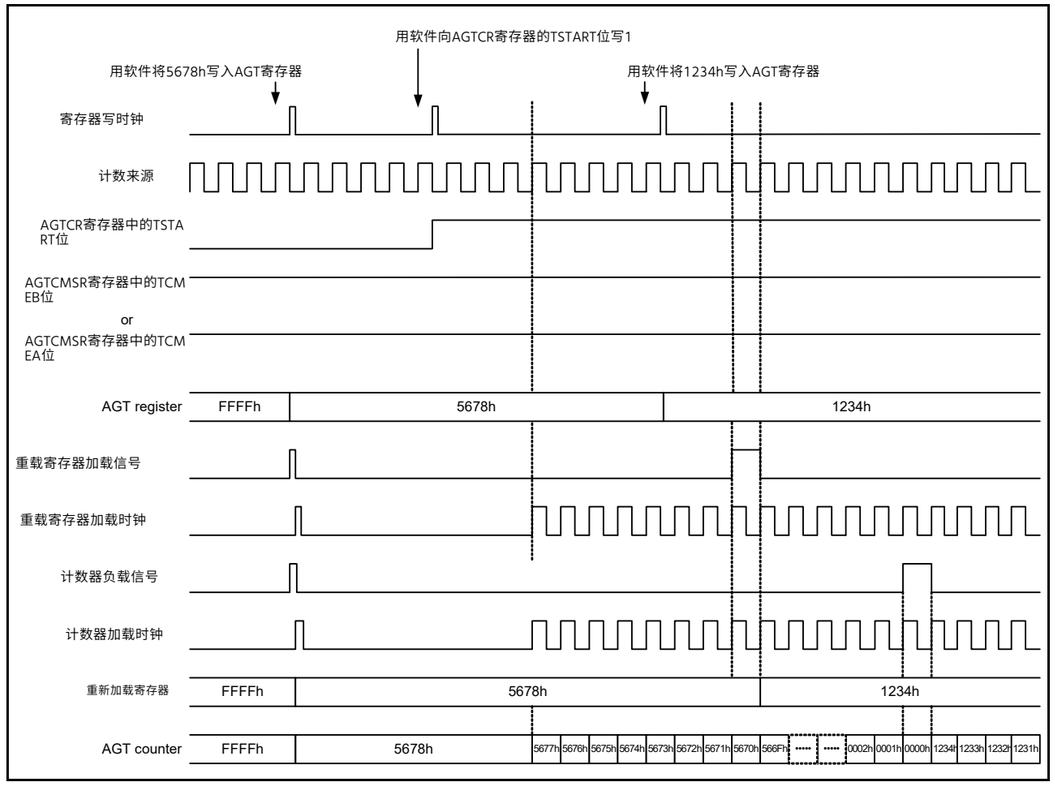


Figure 25.3 比较匹配寄存器A或B有效时TSTART位值和TCMEA或TCMEB位值的重写操作时序

25.3.2 重载寄存器和比较寄存器AB重写操作

不管操作模式如何，对比较寄存器AB的重写操作的时序取决于AGTCR寄存器中TSTART位的值。当TSTART位为0（计数停止）时，将计数值直接写入重载寄存器和比较寄存器AB。当TSTART位为1（开始计数）时，将值同步写入重载寄存器计数源，然后与计数器的下溢同步到比较寄存器。

图25.4显示了比较寄存器A的TSTART位值的重写操作时序。比较寄存器B与比较寄存器A的时序相同。

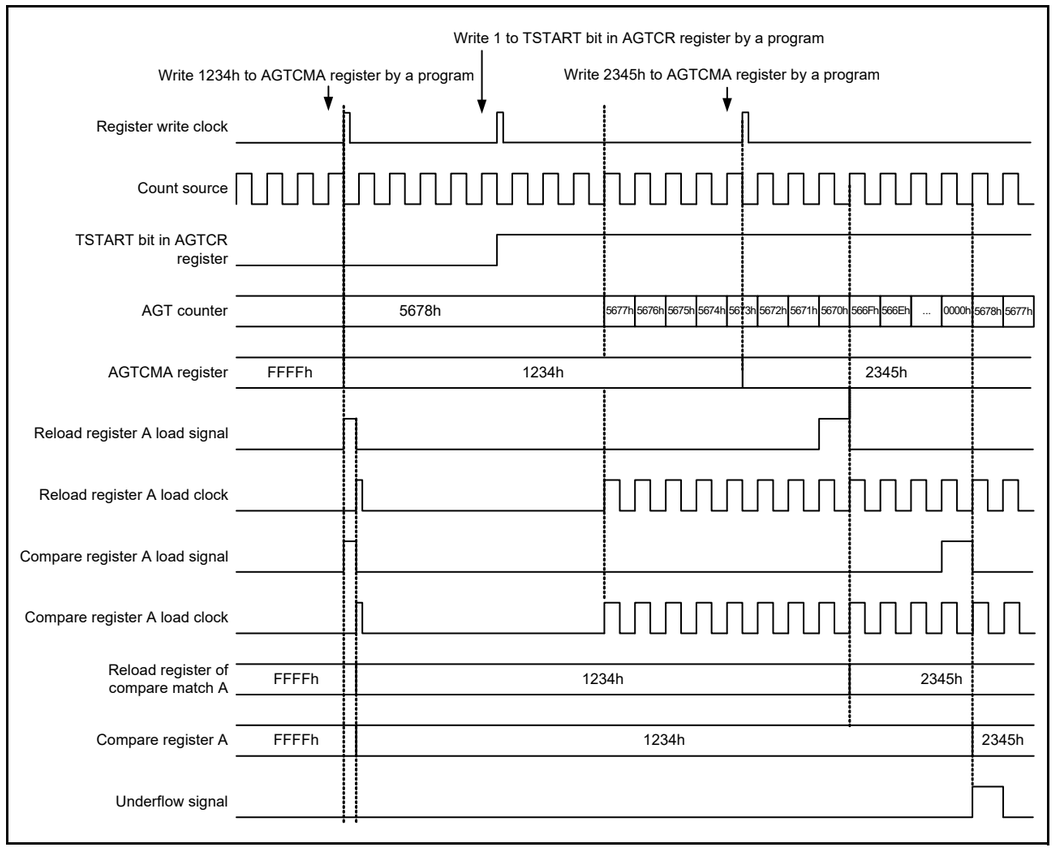


Figure 25.4 Timing of rewrite operation with TSTART bit value for compare register A

25.3.3 Timer Mode

In timer mode, the AGT counter is decremented by the count source selected in bits TCK[2:0] in the AGTMR1 register. In timer mode, the count value is decremented by 1 on each rising edge of the count source. When the count value reaches 0000h and the next count source is input, an underflow occurs and an interrupt request is generated.

Figure 25.5 shows the operation example in timer mode.

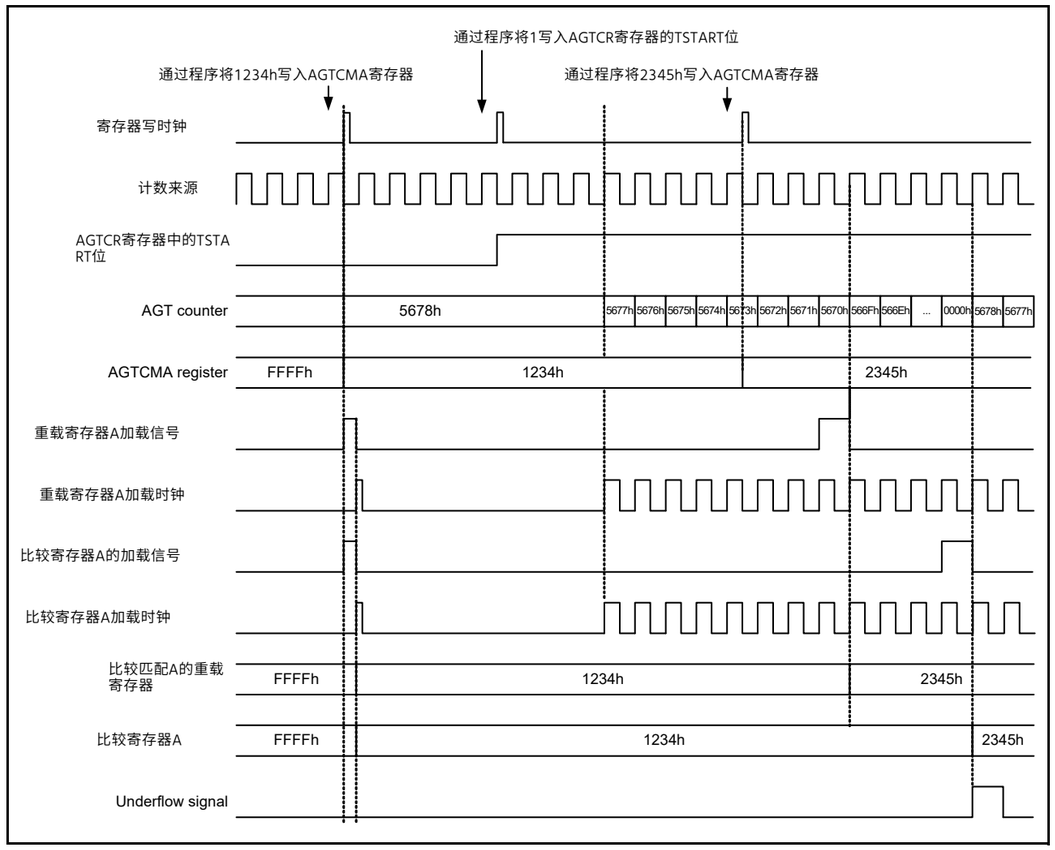


Figure 25.4 比较寄存器A的TSTART位值的重写操作时序

25.3.3 定时器模式

在定时器模式下，AGT计数器按AGTMR1寄存器的TCK[2:0]位中选择的计数源递减。
在定时器模式下，计数值在计数源的每个上升沿减1。当计数值达到0000h并输入下一个计数源时，发生下溢并产生中断请求。

图25.5显示了定时器模式下的操作示例。

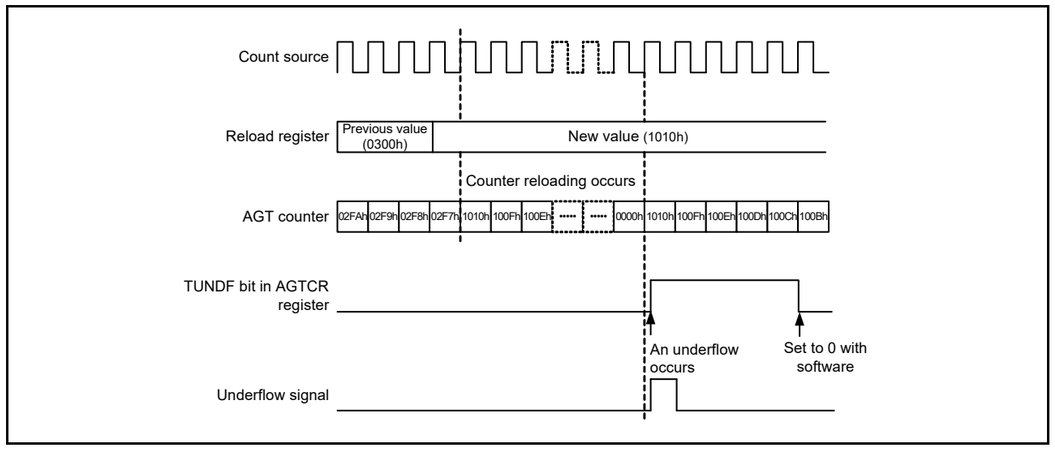


Figure 25.5 Operation example in timer mode

25.3.4 Pulse Output Mode

In pulse output mode, the counter is decremented by the count source selected in TCK[2:0] bits in the AGTMR1 register, and the output level of pins AGTIOn and AGTOn pin inverted each time an underflow occurs.

In pulse output mode, the count value is decremented by 1 on each rising edge of the count source. When the count value reaches 0000h and the next count source is input, an underflow occurs and an interrupt request is generated. In addition, a pulse can be output from the AGTIOn and AGTOn pins. The output level is inverted each time an underflow occurs. The pulse output from the AGTOn pin can be stopped with the TOE bit in the AGTIOC register. The output level can be selected with the TEDGSEL bit in the AGTIOC register.

Figure 25.6 shows the operation example in pulse output mode.

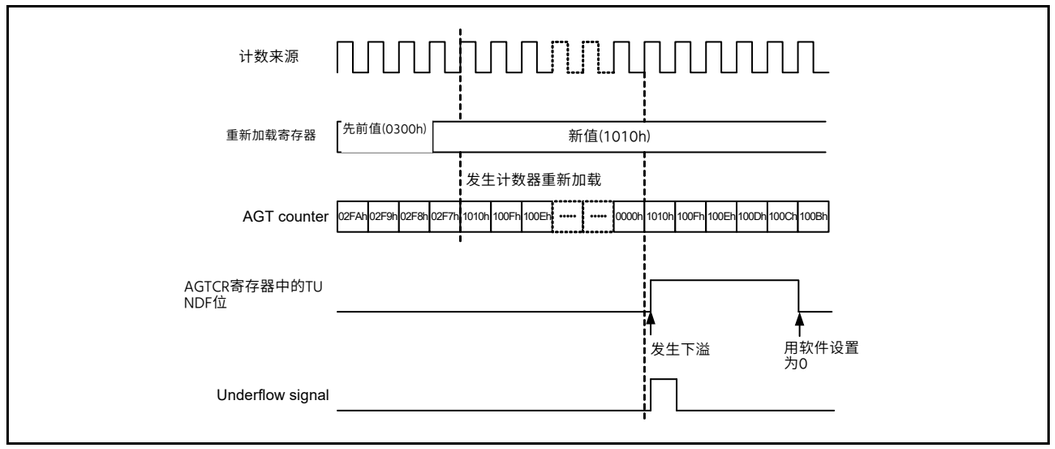


Figure 25.5 定时器模式下的操作示例

25.3.4 脉冲输出方式

在脉冲输出模式下，计数器由AGTMR1寄存器的TCK[2:0]位中选择的计数源递减，每次发生下溢时，引脚AGTIOn和AGTOn引脚的输出电平反转。

在脉冲输出模式下，计数值在计数源的每个上升沿减1。当计数值达到0000h并输入下一个计数源时，发生下溢并产生中断请求。此外，可以从AGTIOn和AGTOn引脚输出脉冲。每次发生下溢时，输出电平都会反转。AGTOn引脚的脉冲输出可通过AGTIOC寄存器中的TOE位停止。可以通过AGTIOC寄存器中的TEDGSEL位选择输出电平。

图25.6显示了脉冲输出模式下的操作示例。

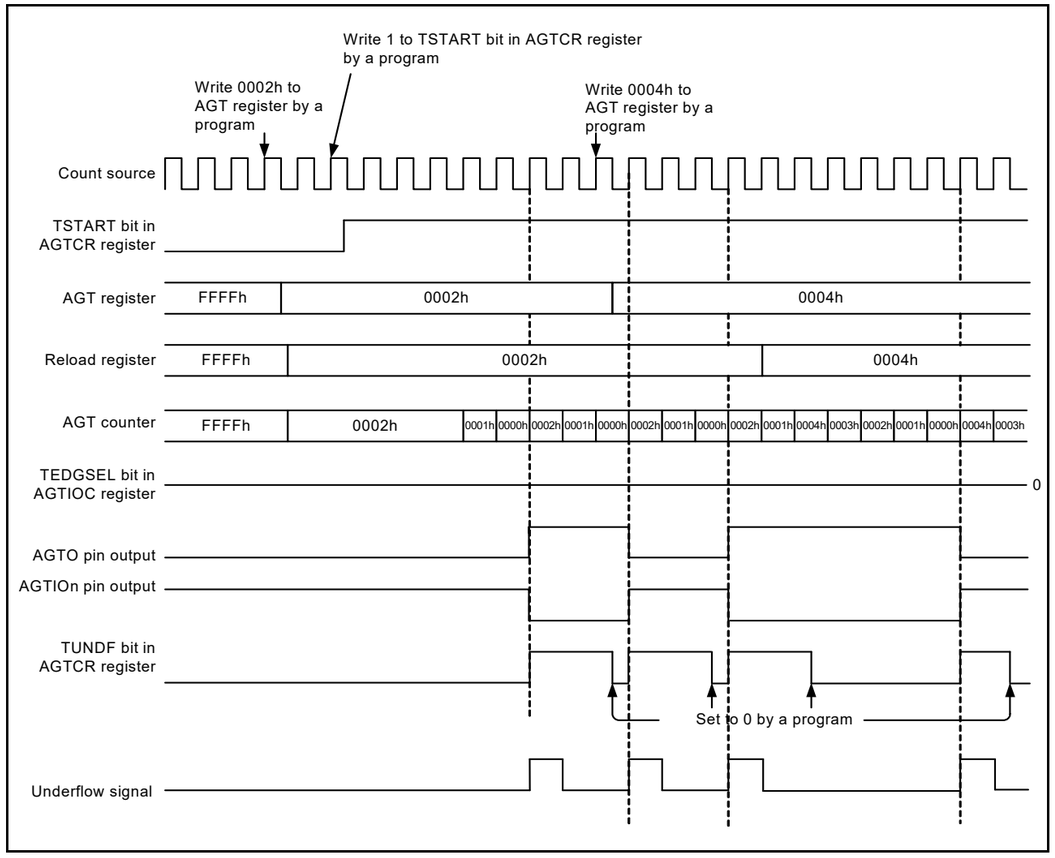


Figure 25.6 Operation example in pulse output mode

25.3.5 Event Counter Mode

In event counter mode, the counter is decremented by an external event signal input to the AGTIOn pin. Various periods for counting events can be set with the TIOGT[1:0] bits in the AGTIOC and AGTISR registers. In addition, the filter function for the AGTIOn input can be specified with bits TIPF[1:0] in the AGTIOC register. The output from the AGTOn pin can be toggled even in event counter mode.

Figure 25.7 shows the operation example in event counter mode.

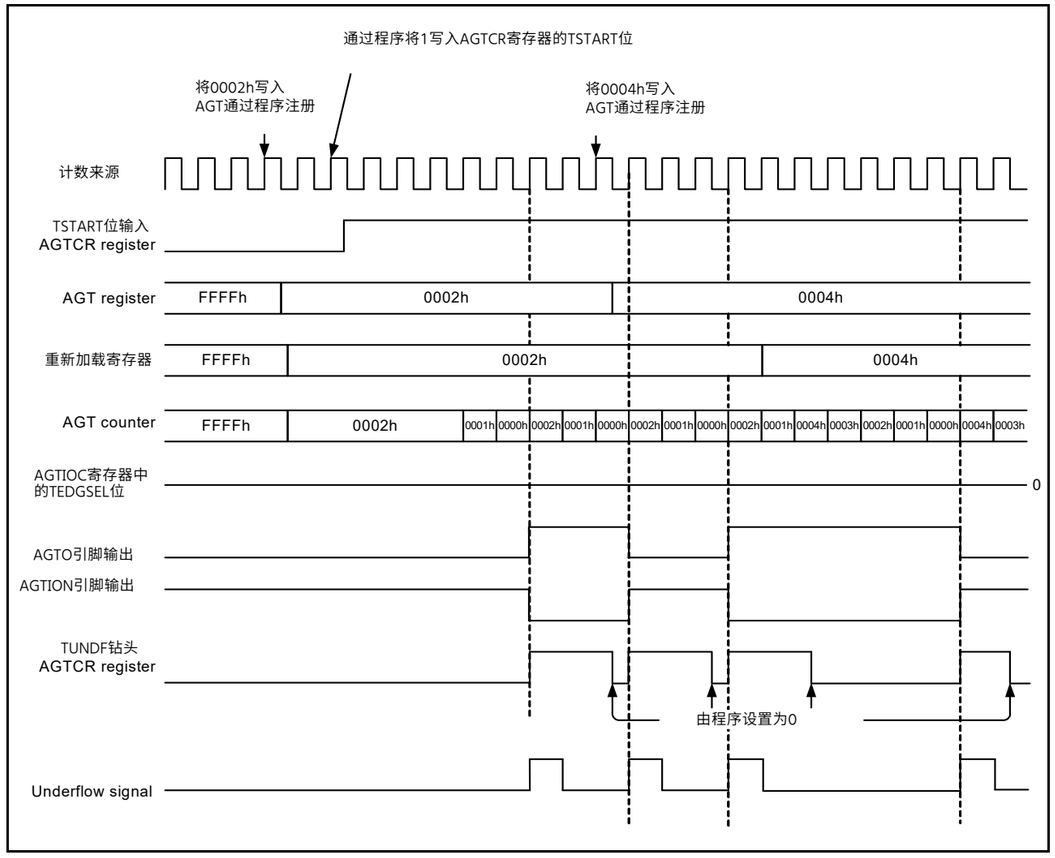


Figure 25.6 脉冲输出模式的动作示例

25.3.5 事件计数器模式

在事件计数器模式下，计数器由输入到AGTIOn引脚的外部事件信号递减。可以使用AGTIOC和AGTISR寄存器中的TIOGT[1:0]位设置计数事件的各种周期。此外，可以使用AGTIOC寄存器中的位TIPF[1:0]指定AGTIOn输入的过滤器功能。即使在事件计数器模式下，也可以切换AGTOn引脚的输出。

图25.7显示了事件计数器模式下的操作示例。

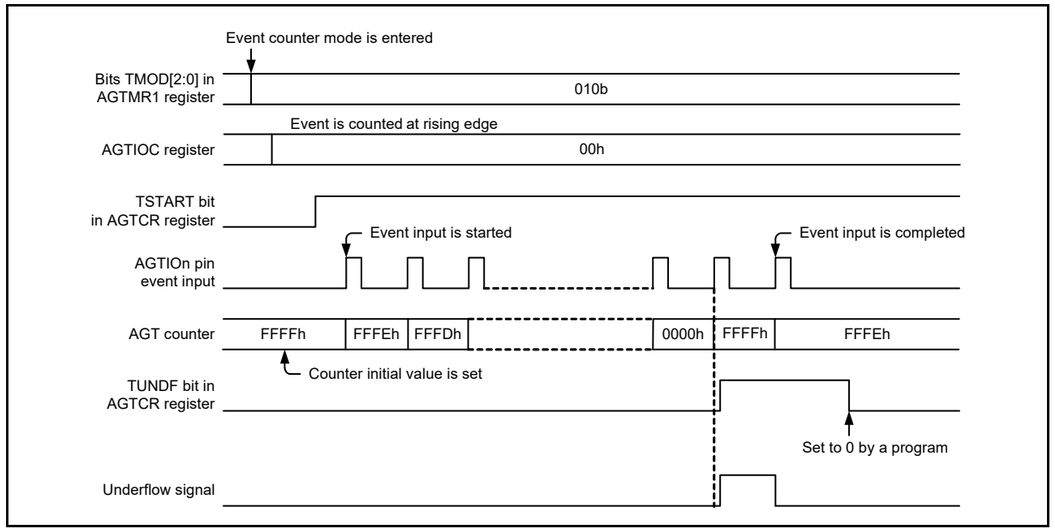


Figure 25.7 Operation example 1 in event counter mode

Figure 25.8 shows an operation example for counting during the specified period in event counter mode (bits TIOGT[1:0] in the AGTIOC register are set to 01b).

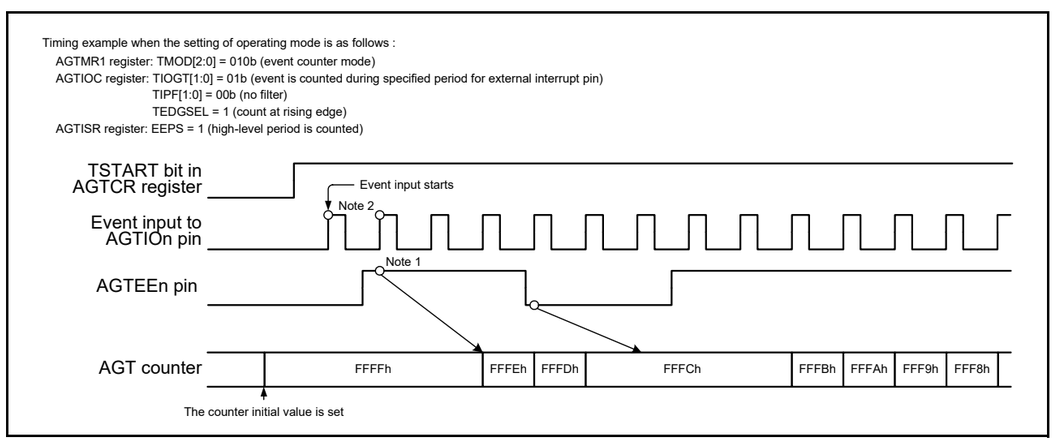


Figure 25.8 Operation example 2 in event counter mode

Note 1. To control synchronization, there is a delay of 2 cycles of the count source until count operation is affected. It is also possible that the count start timing is shifted by 1 cycle because of the phase difference between the AGTEEn and the sampling clock.

Note 2. Count operation can be performed for 2 cycles of the count source immediately after the count starts, depending on the previous state before the count stops.
To disable the count for 2 cycles immediately after the count starts, write 1 to the TSTOP bit in the AGTCR register to initialize the internal circuit, and then complete the operation settings before starting the count operation.

25.3.6 Pulse Width Measurement Mode

In pulse width measurement mode, the pulse width of an external signal input to the AGTIOn pin is measured. When the level specified in the TEDGSEL bit in the AGTIOC register is input to the AGTIOn pin, the counter is decremented by

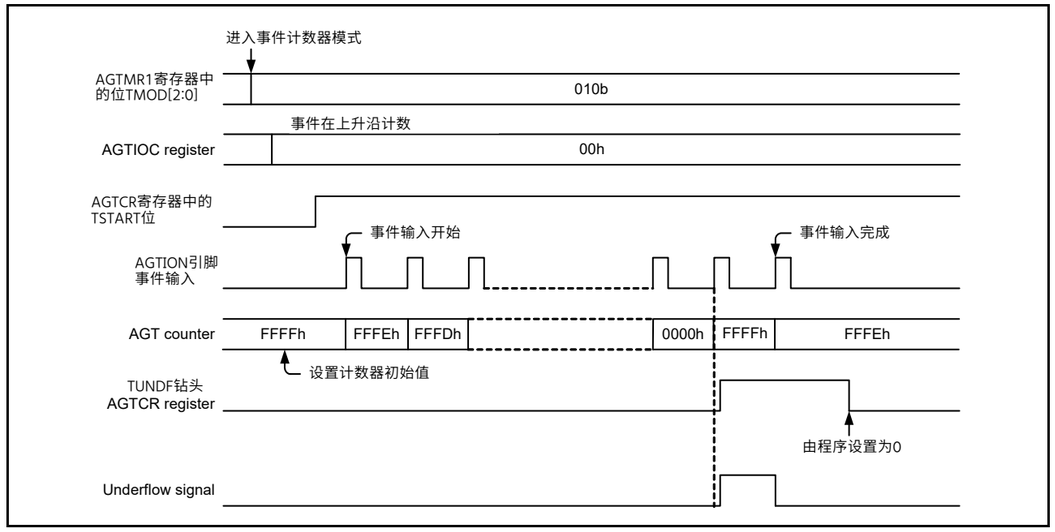


Figure 25.7 事件计数器模式下的操作示例1

图25.8显示了在事件计数器模式（位AGTIOC寄存器中的TIOGT[1:0]设置为01b）。

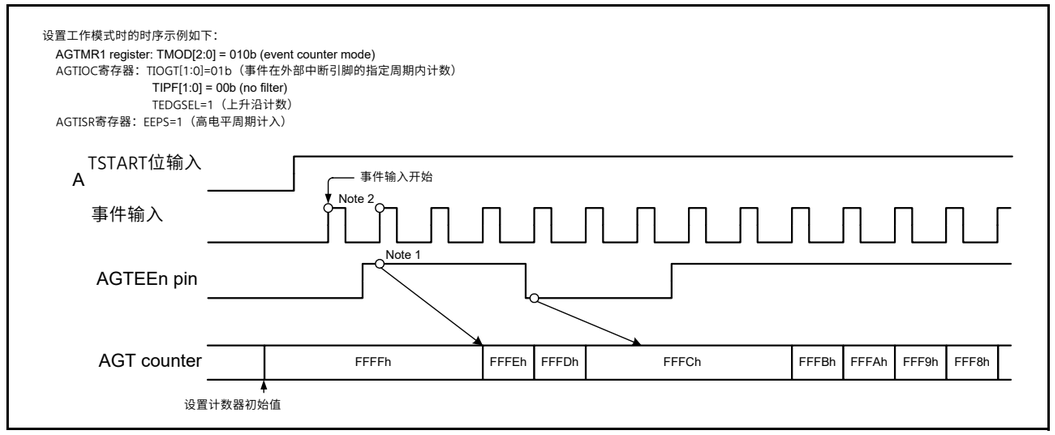


Figure 25.8 事件计数器模式下的操作示例2

注1.为了控制同步，计数源有2个周期的延迟，直到计数操作受到影响。由于AGTEEn和采样时钟之间的相位差，计数开始时间也可能偏移1个周期。

注2.根据计数停止前的状态，在计数开始后立即可以对计数源执行2个周期的计数操作。要在计数开始后立即禁止计数2个周期，将1写入AGTCR寄存器的TSTOP位以初始化内部电路，然后在开始计数操作之前完成操作设置。

25.3.6 脉冲宽度测量模式

在脉冲宽度测量模式下，测量输入到AGTIOn引脚的外部信号的脉冲宽度。当AGTIOC寄存器的TEDGSEL位指定的电平输入到AGTIOn引脚时，计数器递减

the count source selected by TCK[2:0] bits in the AGTMR1 register. When the specified level on the AGTIOn pin ends, the counter is stopped, the TEDGF bit in the AGTCR register is set to 1 (active edge received), and an interrupt request is generated. The measurement of pulse width data is performed by reading the count value while the counter is stopped. Also, when the counter underflows during measurement, the TUNDF bit in the AGTCR register is set to 1 and an interrupt request is generated.

Figure 25.9 shows the operation example in pulse width measurement mode.

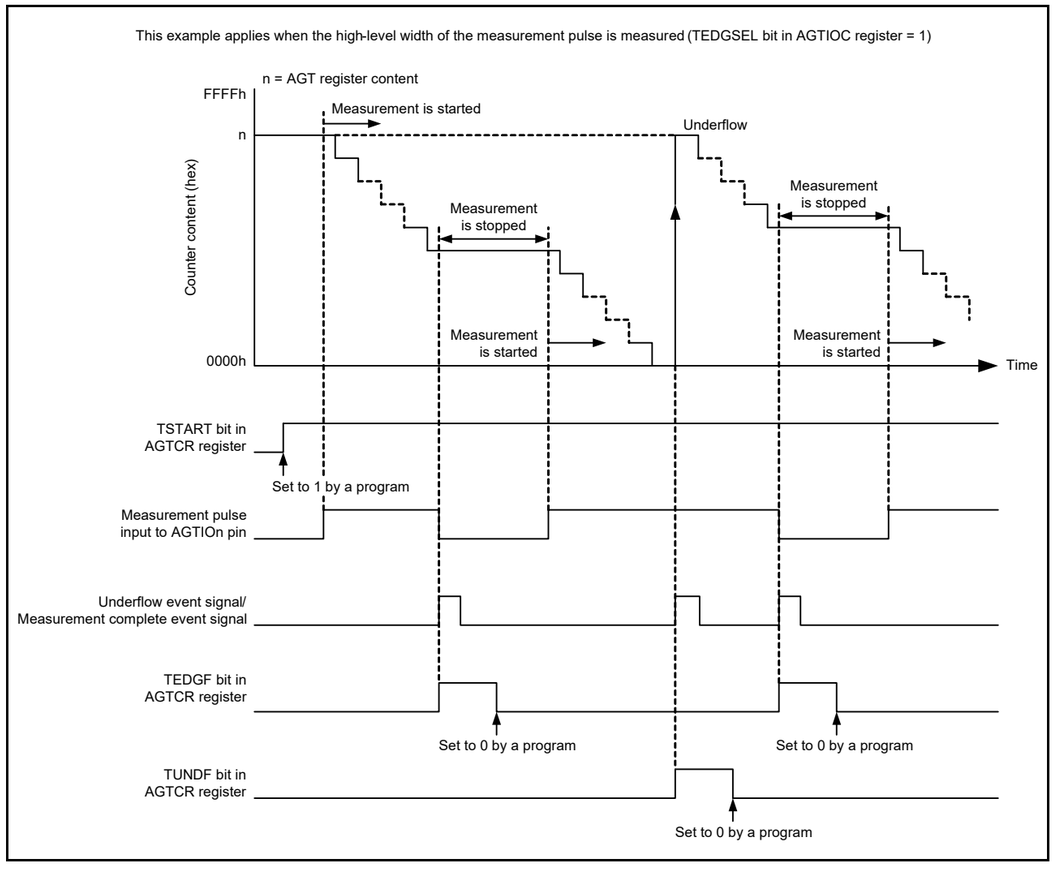


Figure 25.9 Operation example in pulse width measurement mode

25.3.7 Pulse Period Measurement Mode

In pulse period measurement mode, the pulse period of an external signal input to the AGTIOn pin is measured. The counter is decremented by the count source selected with bits TCK[2:0] in the AGTMR1 register. When a pulse with the level specified in the TEDGSEL bit in the AGTIOC register is input to the AGTIOn pin, the count value is transferred to the read-out buffer on the rising edge of the count source. The value in the reload register is loaded to the counter at the next rising edge. Simultaneously, the TEDGF bit in the AGTCR register is set to 1 (active edge received) and an interrupt request is generated. The read-out buffer (AGT register) is read at this time and the difference from the reload value (see section 25.4.5, How to Calculate Event Number, Pulse Width, and Pulse Period) is the period data of the input pulse. The period data is retained until the read-out buffer is read. When the counter underflows, the TUNDF bit in the AGTCR register is set to 1 (underflow) and an interrupt request is generated.

Figure 25.10 shows the operation example in pulse period measurement mode.

Only input pulses with a period longer than twice the period of the count source are measured. Also, the low-level and high-level widths must both be longer than the period of the count source. If a pulse period shorter than these conditions

由AGTMR1寄存器中的TCK[2:0]位选择的计数源。当AGTIOn引脚上的指定电平结束时，计数器停止，AGTCR寄存器中的TEDGF位设置为1（接收到有效沿），并产生中断请求。通过在计数器停止时读取计数值来执行脉冲宽度数据的测量。此外，当测量期间计数器下溢时，AGTCR寄存器中的TUNDF位设置为1，并产生中断请求。

图25.9显示了脉宽测量模式下的操作示例。

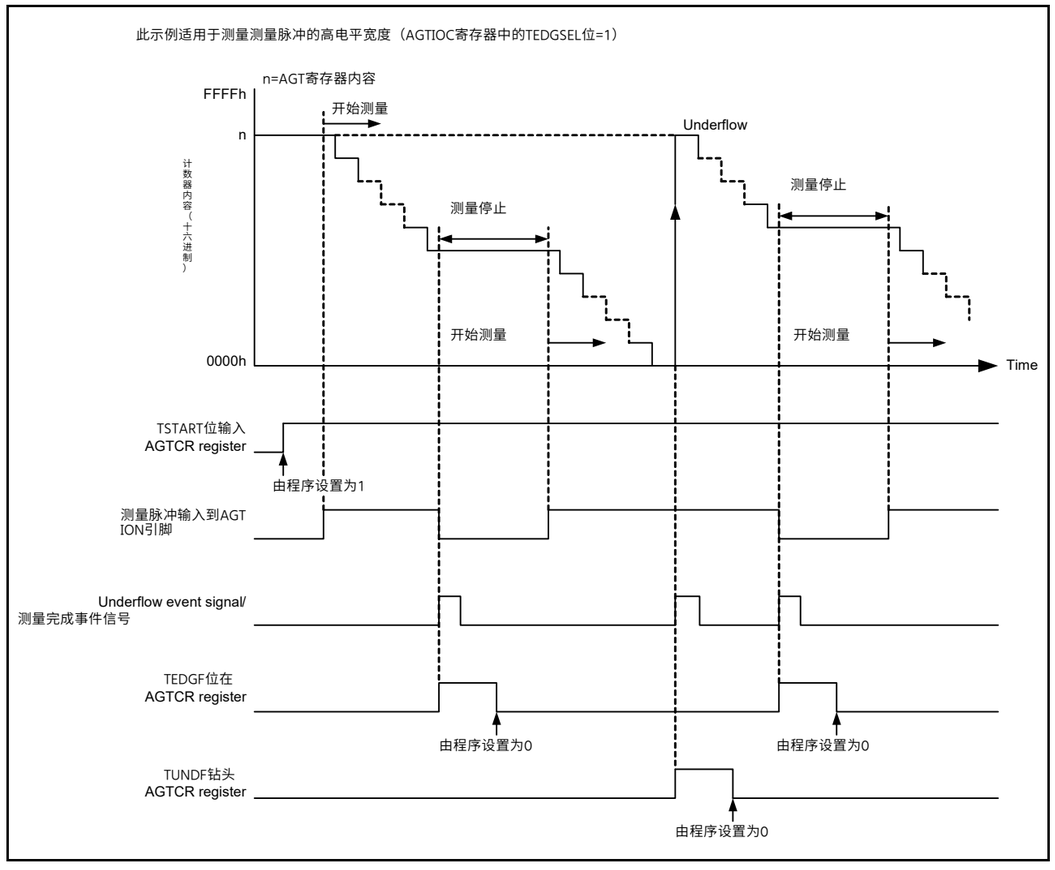


Figure 25.9 脉宽测量模式下的操作示例

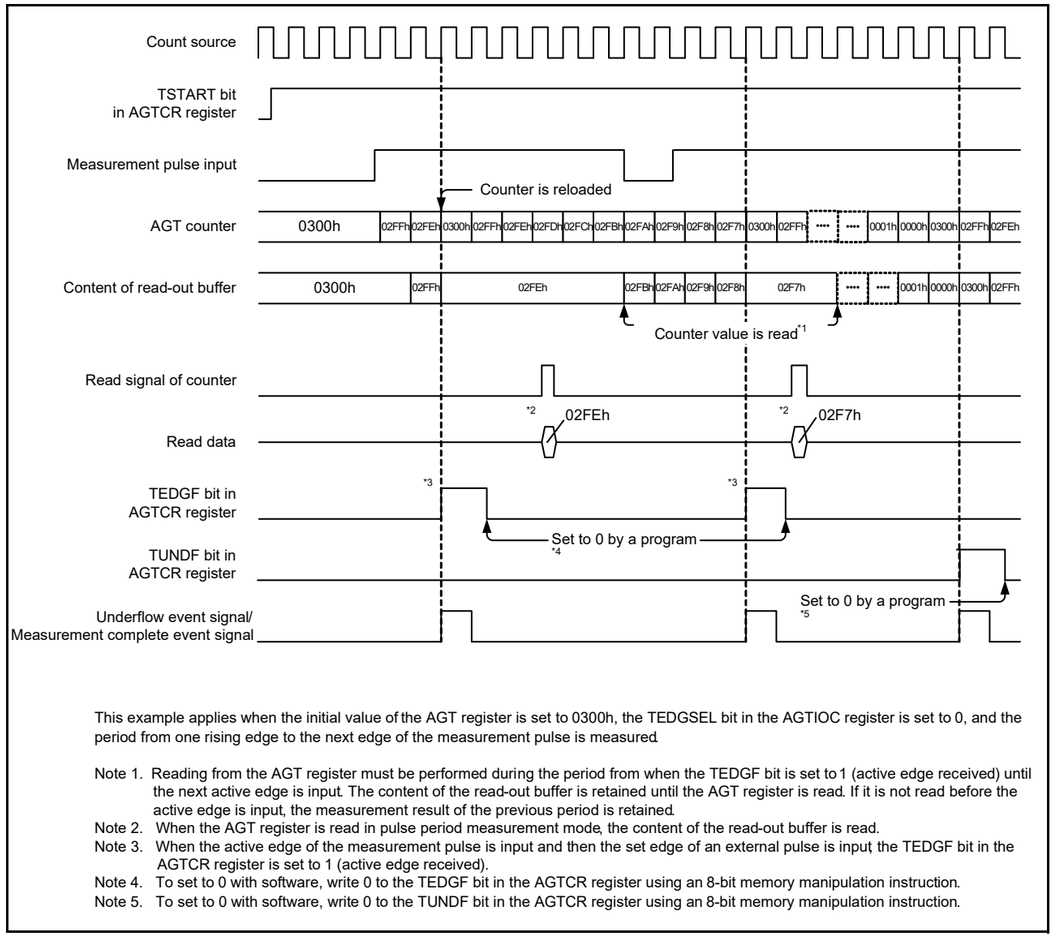
25.3.7 脉冲周期测量模式

在脉冲周期测量模式下，测量输入到AGTIOn引脚的外部信号的脉冲周期。计数器由AGTMR1寄存器中的TCK[2:0]位选择的计数源递减。当AGTIOC寄存器的TEDGSEL位指定电平的脉冲输入到AGTIOn引脚时，计数值在计数源的上升沿传送到读出缓冲器。重载寄存器中的值在下一个上升沿加载到计数器。同时，AGTCR寄存器中的TEDGF位设置为1（接收到有效边沿）并产生中断请求。此时读取读出缓冲区（AGT寄存器），与重载值的差值（参见第25.4.5节，如何计算事件数、脉冲宽度和脉冲周期）是输入脉冲的周期数据。周期数据被保留，直到读出缓冲器被读取。当计数器下溢时，AGTCR寄存器中的TUNDF位设置为1（下溢）并产生中断请求。

图25.10显示了脉冲周期测量模式下的操作示例。

仅测量周期长于计数源周期两倍的输入脉冲。此外，低电平和高电平宽度都必须长于计数源的周期。如果脉冲周期短于这些条件

is input, the input might be ignored.



This example applies when the initial value of the AGT register is set to 0300h, the TEDGSEL bit in the AGTIOC register is set to 0, and the period from one rising edge to the next edge of the measurement pulse is measured.

Note 1. Reading from the AGT register must be performed during the period from when the TEDGF bit is set to 1 (active edge received) until the next active edge is input. The content of the read-out buffer is retained until the AGT register is read. If it is not read before the active edge is input, the measurement result of the previous period is retained.
Note 2. When the AGT register is read in pulse period measurement mode, the content of the read-out buffer is read.
Note 3. When the active edge of the measurement pulse is input and then the set edge of an external pulse is input the TEDGF bit in the AGTCR register is set to 1 (active edge received).
Note 4. To set to 0 with software, write 0 to the TEDGF bit in the AGTCR register using an 8-bit memory manipulation instruction.
Note 5. To set to 0 with software, write 0 to the TUNDF bit in the AGTCR register using an 8-bit memory manipulation instruction.

Figure 25.10 Operation example in pulse period measurement mode

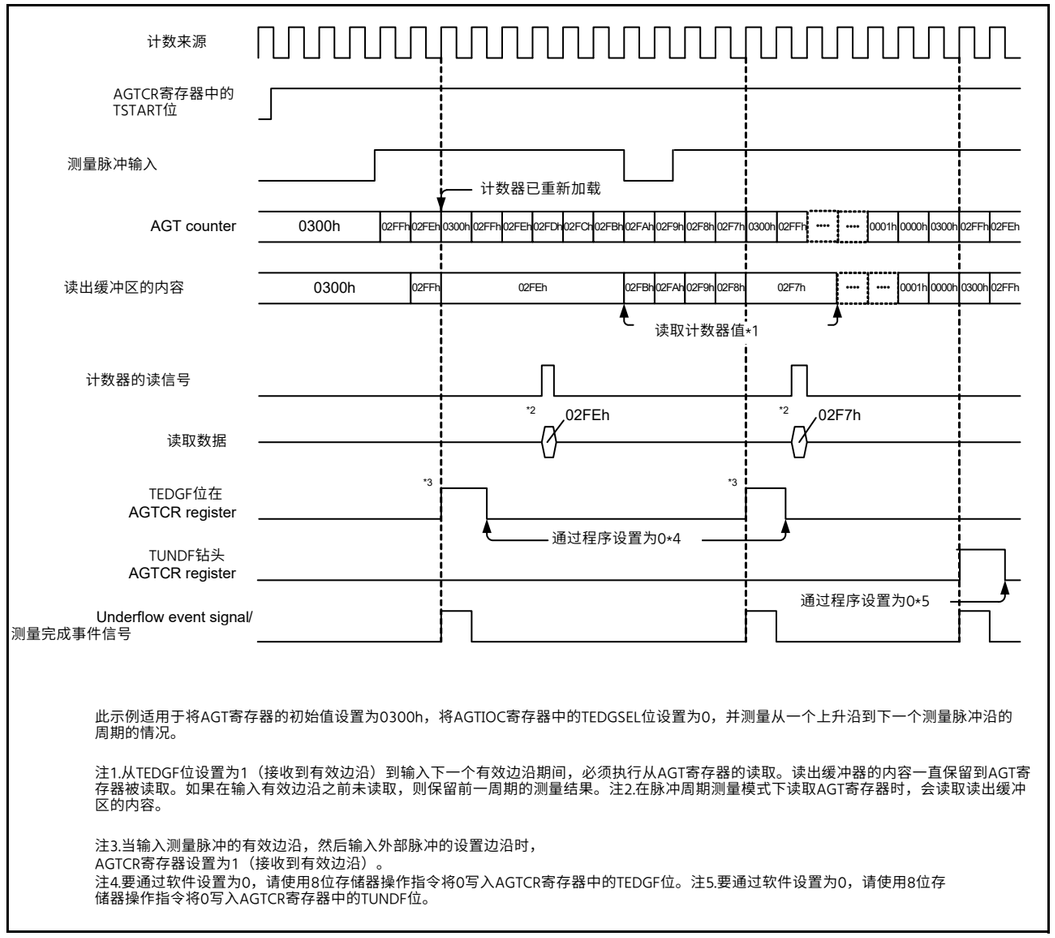
25.3.8 Compare Match Function

The compare match function detects matches between the content of the AGTCMA or AGTCMB register and the content of the AGT register. This function is enabled when the TCMEA bit or the TCMEB bit in the AGTCMSR register is 1 (compare match A register or compare match B register is valid). The counter is decremented by the count source selected in bits TCK[2:0] in the AGTMR1 register, and when the values of AGT and AGTCMA or AGTCMB match, the TCMAF/TCMBF bit in the AGTCR register is set to 1 (match), and an interrupt request is generated.

When compare match function is enabled, the timing of the rewrite operation to the reload register and the counter differs. See section 25.3.1, Reload Register and Counter Rewrite Operation for details. In addition, the output level of the AGTOAn and AGTOBn pins is inverted by the match and by the underflow. The output level can be selected with the TOPOLA or TOPOLB bit in the AGTCMSR register.

Figure 25.11 shows the operation example in compare match mode.

是输入，输入可能会被忽略。



此示例适用于将AGT寄存器的初始值设置为0300h，将AGTIOC寄存器中的TEDGSEL位设置为0，并测量从一个上升沿到下一个测量脉冲沿的周期的情况。

注1.从TEDGF位设置为1（接收到有效边沿）到输入下一个有效边沿期间，必须执行从AGT寄存器的读取。读出缓冲器的内容一直保留到AGT寄存器被读取。如果在输入有效边沿之前未读取，则保留前一周期的测量结果。注2.在脉冲周期测量模式下读取AGT寄存器时，会读取读出缓冲区的内容。

注3.当输入测量脉冲的有效边沿，然后输入外部脉冲的设置边沿时，
AGTCR寄存器设置为1（接收到有效边沿）。
注4.要通过软件设置为0，请使用8位存储器操作指令将0写入AGTCR寄存器中的TEDGF位。注5.要通过软件设置为0，请使用8位存储器操作指令将0写入AGTCR寄存器中的TUNDF位。

Figure 25.10 脉冲周期测量模式下的操作示例

25.3.8 比较匹配函数

比较匹配功能检测AGTCMA或AGTCMB寄存器的内容与AGT寄存器的内容是否匹配。当AGTCMSR寄存器中的TCMEA位或TCMEB位为1（比较匹配A寄存器或比较匹配B寄存器有效）时，该功能被使能。计数器按AGTMR1寄存器的TCK[2:0]位选择的计数源递减，当AGT与AGTCMA或AGTCMB的值匹配时，AGTCR寄存器中的TCMAFTCMBF位设置为1（匹配），并产生中断请求。

当比较匹配功能启用时，对重载寄存器和计数器的重写操作的时序不同。有关详细信息，请参见第25.3.1节，重载寄存器和计数器重写操作。此外，AGTOAn和AGTOBn引脚的输出电平通过匹配和下溢反转。输出电平可以选择与

AGTCMSR寄存器中的TOPOLA或TOPOLB位。

图25.11显示了比较匹配模式下的操作示例。

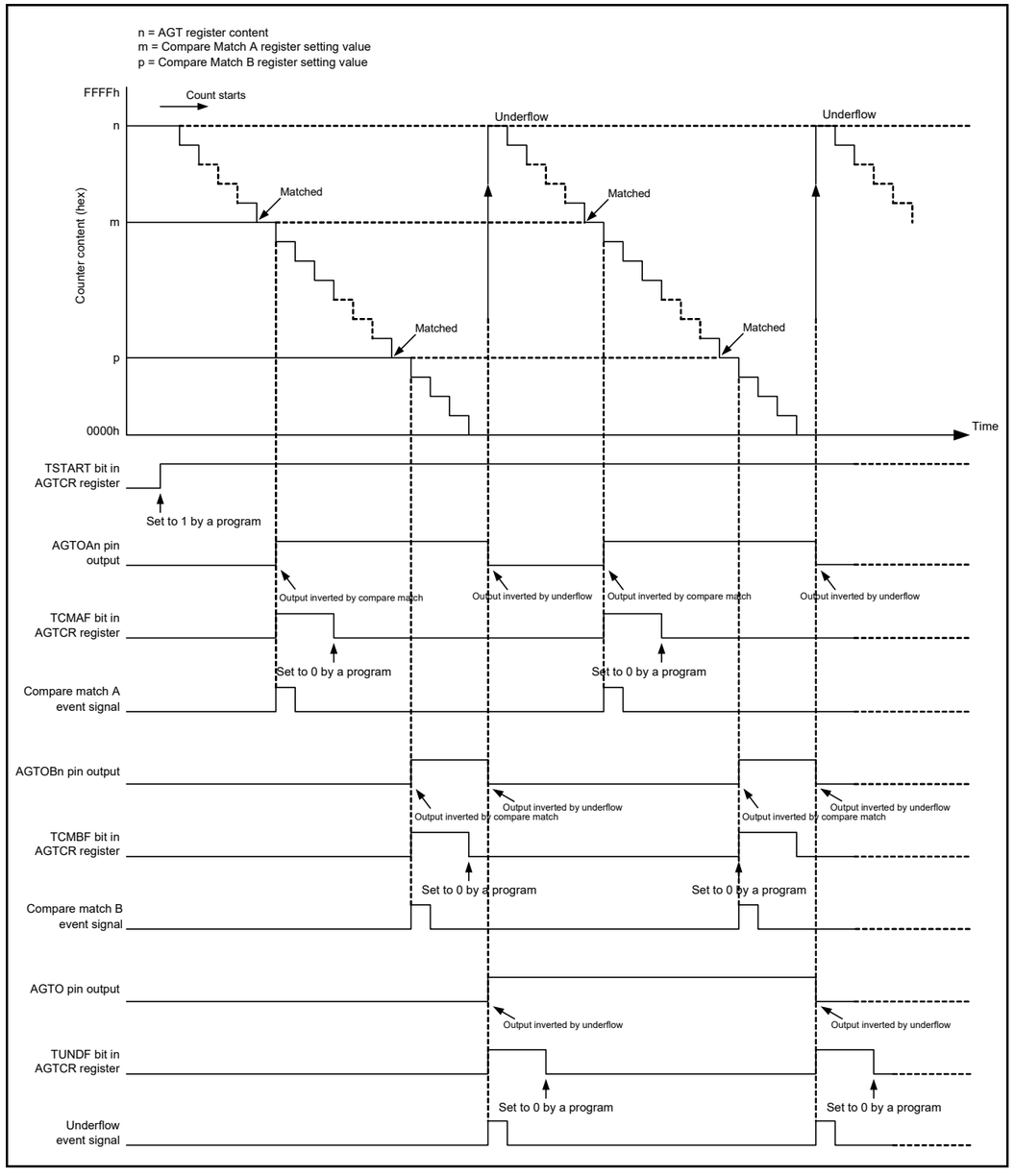


Figure 25.11 Operation example in compare match mode (TOPOLA = 0, TOPOLB = 0)

25.3.9 Output Settings for Each Mode

Table 25.5 to Table 25.8 list the states of pins AGTOn, AGTIOn, AGTOAn, and AGTOBn in each mode.

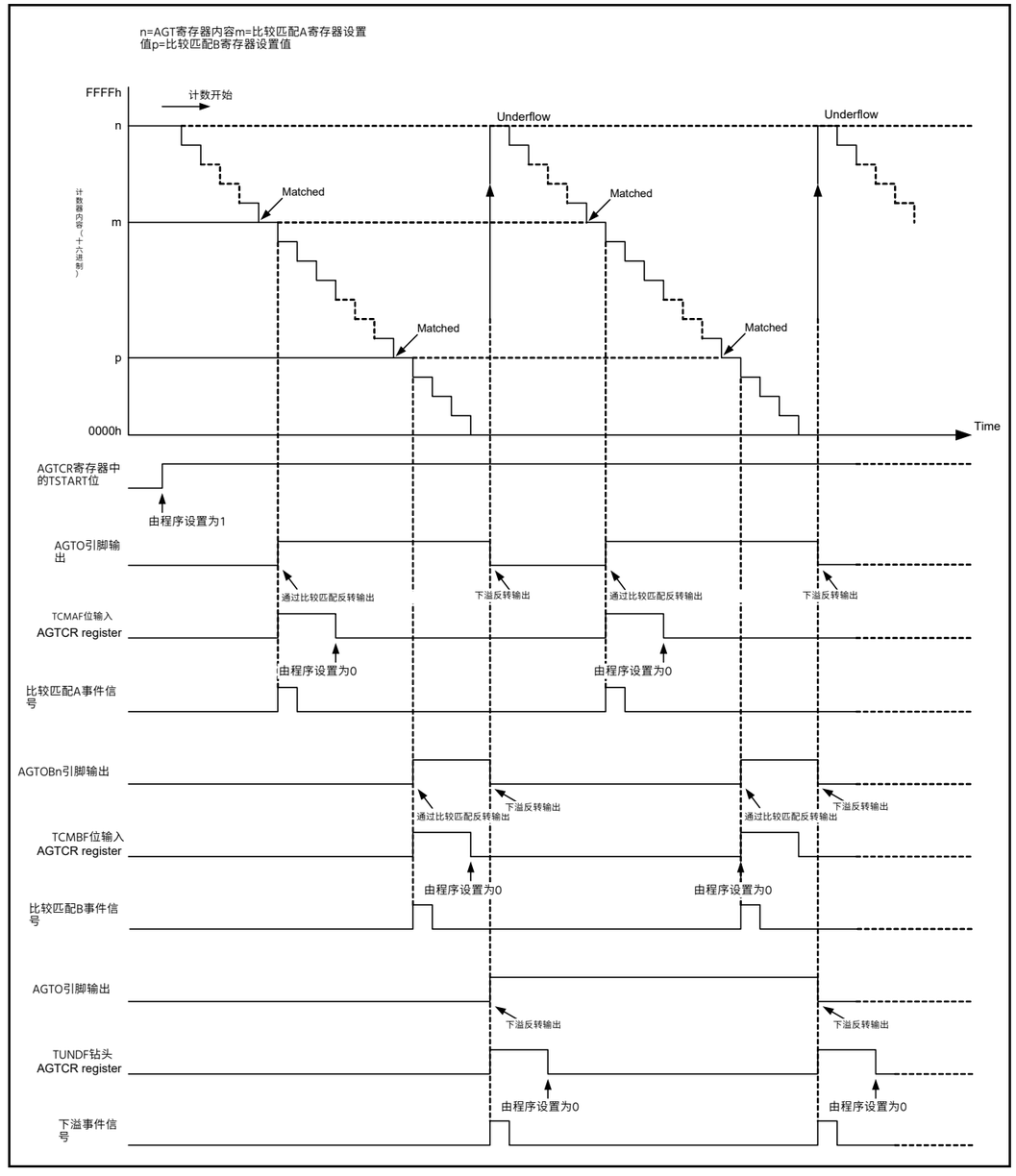


Figure 25.11 比较匹配模式下的操作示例(TOPOLA=0 TOPOLB=0)

25.3.9 每种模式的输出设置

表25.5至表25.8列出了每种模式下引脚AGTOn、AGTIOn、AGTOAn和AGTOBn的状态。

Table 25.5 AGTOn pin setting

Operating mode	AGTIOC register		AGTOn pin output
	TOE bit	TEDGSEL bit	
All modes	1	1	Inverted output
		0	Normal output
	0	0 or 1	Output disabled

Table 25.6 AGTIOn pin setting

Operating mode	AGTIOC register	AGTIOn pin I/O
	TEDGSEL bit	
Timer mode	0 or 1	Input (not used)
Pulse output mode	1	Normal output
	0	Inverted output
Event counter mode	0 or 1	Input
Pulse width measurement mode		
Pulse period measurement mode		

Table 25.7 AGTOAn pin setting

Operating mode	AGTCMSR register		AGTOAn pin output
	TOEA bit	TOPOLA bit	
Timer mode	1	1	Inverted output
		0	Normal output
	0	0 or 1	Output disabled (not used)
Pulse output mode	1	1	Inverted output
		0	Normal output
	0	0 or 1	Output disabled (not used)
Event counter mode	1	1	Inverted output
		0	Normal output
	0	0 or 1	Output disabled (not used)
Pulse width measurement mode	0	0	Prohibited
Pulse period measurement mode			

Table 25.8 AGTOBn pin setting (1 of 2)

Operating mode	AGTCMSR register		AGTOBn pin output
	TOEB bit	TOPOLB bit	
Timer mode	1	1	Inverted output
		0	Normal output
	0	0 or 1	Output disabled (not used)
Pulse output mode	1	1	Inverted output
		0	Normal output
	0	0 or 1	Output disabled (not used)

Table 25.5 AGTOn引脚设置

操作模式	AGTIOC register		AGTOn引脚输出
	脚趾位	TEDGSEL bit	
所有模式	1	1	反相输出
		0	正常输出
	0	0 or 1	输出禁用

Table 25.6 AGTIOn引脚设置

操作模式	AGTIOC register	AGTIOn pin I/O
	TEDGSEL bit	
定时器模式	0 or 1	Input (not used)
脉冲输出方式	1	正常输出
	0	反相输出
事件计数器模式	0 or 1	Input
脉宽测量模式		
脉冲周期测量模式		

Table 25.7 AGTO引脚设置

操作模式	AGTCMSR register		AGTO引脚输出
	TOEA bit	TOPOLA bit	
定时器模式	1	1	反相输出
		0	正常输出
	0	0 or 1	输出禁用（未使用）
脉冲输出方式	1	1	反相输出
		0	正常输出
	0	0 or 1	输出禁用（未使用）
事件计数器模式	1	1	反相输出
		0	正常输出
	0	0 or 1	输出禁用（未使用）
脉宽测量模式	0	0	Prohibited
脉冲周期测量模式			

Table 25.8 AGTOBn引脚设置(1of2)

操作模式	AGTCMSR register		AGTOBn引脚输出
	TOEB bit	TOPOLB bit	
定时器模式	1	1	反相输出
		0	正常输出
	0	0 or 1	输出禁用（未使用）
脉冲输出方式	1	1	反相输出
		0	正常输出
	0	0 or 1	输出禁用（未使用）

Table 25.8 AGTOBn pin setting (2 of 2)

Operating mode	AGTCMSR register TOEB bit	TOPOLB bit	AGTOBn pin output
Event counter mode	1	1	Inverted output
		0	Normal output
	0	0 or 1	Output disabled (not used)
Pulse width measurement mode	0	0	Prohibited
Pulse period measurement mode			

25.3.10 Standby Mode

The AGT can operate in Software Standby and Deep Software Standby modes. Set it to Software Standby mode or Deep Software Standby mode with count operation start (TSTART = 1, TCSTF = 1).

Table 25.9 and Table 25.10 show the settings that can be used in Software Standby and Deep Software Standby modes.

Table 25.9 Usable settings for AGT0 in Software Standby and Deep Software Standby modes

Operating mode	TCK[2:0] bits of AGTMR1 register	Operating clock	Resurgence factor of CPU
Timer mode	100b or 110b	AGTLCLK or AGTSCLK	—
Pulse output mode	100b or 110b	AGTLCLK or AGTSCLK	—
Event counter mode	- (Invalid)	AGTIOn	—
Pulse width measurement mode	100b or 110b	AGTLCLK or AGTSCLK	—
Pulse period measurement mode	100b or 110b	AGTLCLK or AGTSCLK	—

Table 25.10 Usable settings AGT1 in Software Standby and Deep Software Standby modes

Operating mode	TCK[2:0] bits of AGTMR1 register	Operating clock	Resurgence factor of CPU
Timer mode	100b or 110b or 101b *1	AGTLCLK or AGTSCLK or AGT0 underflow	• Underflow • Compare match A/B
Pulse output mode	100b or 110b or 101b *1	AGTLCLK or AGTSCLK or AGT0 underflow	• Underflow • Compare match A/B
Event counter mode	- (Invalid)	AGTIOn	• Underflow • Compare match A/B
Pulse width measurement mode	100b or 110b or 101b *1	AGTLCLK or AGTSCLK or AGT0 underflow	• Underflow • Active edge
Pulse period measurement mode	100b or 110b or 101b *1	AGTLCLK or AGTSCLK or AGT0 underflow	• Underflow • Active edge

Note: Release of Software Standby mode or Deep Software Standby mode is only AGT1.
Note 1. Only when AGT0 operates in Table 25.9.

25.3.11 Interrupt Sources

The AGT has three interrupt sources described in Table 25.11.

Table 25.8 AGTOBn引脚设置（2个中的2个）

操作模式	AGTCMSR register TOEB bit	TOPOLB bit	AGTOBn引脚输出
事件计数器模式	1	1	反相输出
		0	正常输出
	0	0 or 1	输出禁用（未使用）
脉宽测量模式	0	0	Prohibited
脉冲周期测量模式			

25.3.10 待机模式

AGT可以在软件待机和深度软件待机模式下运行。将其设置为软件待机模式或深度计数操作开始的软件待机模式（TSTART=1，TCSTF=1）。

表25.9和表25.10显示了可在软件待机和深度软件待机模式下使用的设置。

Table 25.9 软件待机和深度软件待机模式下AGT0的可用设置

操作模式	AGTMR1寄存器的TCK[2:0]位	工作时钟	中兴因子 CPU
定时器模式	100b or 110b	AGTLCLK or AGTSCLK	—
脉冲输出方式	100b or 110b	AGTLCLK or AGTSCLK	—
事件计数器模式	- (Invalid)	AGTIOn	—
脉宽测量模式	100b or 110b	AGTLCLK or AGTSCLK	—
脉冲周期测量模式	100b or 110b	AGTLCLK or AGTSCLK	—

Table 25.10 软件待机和深度软件待机模式下的可用设置AGT1

操作模式	AGTMR1寄存器的TCK[2:0]位	工作时钟	中兴因子 CPU
定时器模式	100b or 110b or 101b *1	AGTLCLK or AGTSCLK or AGT0 underflow	下溢 比较匹配AB
脉冲输出方式	100b or 110b or 101b *1	AGTLCLK or AGTSCLK or AGT0 underflow	下溢 比较匹配AB
事件计数器模式	- (Invalid)	AGTIOn	下溢 比较匹配AB
脉宽测量模式	100b or 110b or 101b *1	AGTLCLK or AGTSCLK or AGT0 underflow	下溢 活动边沿
脉冲周期测量模式	100b or 110b or 101b *1	AGTLCLK or AGTSCLK or AGT0 underflow	下溢 活动边沿

Note: 软件待机模式或深度软件待机模式的释放只有AGT1。
注1.仅当AGT0在表25.9中运行时。

25.3.11 中断源

AGT具有表25.11中描述的三个中断源。

Table 25.11 AGT interrupt sources

Name	Interrupt source	DMAC/DTC activation
AGTn_AGTI	• When the counter underflows • When measurement of the active width of the external input (AGTIO) is completed in pulse width measurement mode • When the set edge of the external input (AGTIO) is input in pulse period measurement mode.	Possible
AGTn_AGTCMAI	When the values of AGT and AGTCMA match	Possible
AGTn_AGTCMBI	When the values of AGT and AGTCMB match	Possible

Note: Channel number (n = 0 or 1).

25.3.12 Event Signal Output to ELC

The AGT uses the Event Link Controller (ELC) to perform a link operation to a specified module using the interrupt request signal as the event signal. The AGT outputs compare match A, compare match B, and underflow/measurement complete signals as event signals. For details, see section 19, Event Link Controller (ELC).

25.4 Usage Notes

25.4.1 Count Operation Start and Stop Control

- When the operating mode (see Table 25.1) is set to other than the event counter mode, or the count source is set to other than AGT0 underflow (TCK[2:0] = 101b)
  - After 1 (count starts) is written to the TSTART bit in the AGTCR register while the count is stopped, the TCSTF flag in the AGTCR register remains 0 (count stops) for 3 cycles of the count source. Do not access the registers associated with AGT*1 other than the TCSTF flag until this bit is set to 1 (count in progress).
  - After 0 (count stops) is written to the TSTART bit during a count operation, the TCSTF flag remains 1 for 3 cycles of the count source. When the TCSTF flag is set to 0, the count stops. Do not access the registers associated with AGT*1 other than the TCSTF flag until this bit is set to 0.
  - Clear the interrupt register before changing the TSTART bit from 0 to 1. See section 14, Interrupt Controller Unit (ICU) for details.

Note 1. Registers associated with AGT: AGT, AGTCMA, AGTCMB, AGTCR, AGTMR1, AGTMR2, AGTIOC, AGTISR, and AGTCMSR.

- When the operating mode (see Table 25.1) is set to event counter mode, or the count source is set to AGT0 underflow (TCK[2:0] = 101b)
  - After 1 (count starts) is written to the TSTART bit in the AGTCR register while the count is stopped, the TCSTF bit in the AGTCR register remains 0 (count stops) for 2 cycles of the PCLKB. Do not access the registers associated with AGT*1 other than the TCSTF bit until this bit is set to 1 (count in progress).
  - After 0 (count stops) is written to the TSTART bit during a count operation, the TCSTF bit remains 1 for 2 cycles of the PCLKB. When the TCSTF bit is set to 0, the count is stopped. Do not access the registers associated with AGT*1 other than the TCSTF bit until this bit is set to 0.
  - Clear the interrupt register before changing the TSTART bit from 0 to 1. See section 14, Interrupt Controller Unit (ICU) for details.

Note 1. Registers associated with AGT: AGT, AGTCMA, AGTCMB, AGTCR, AGTMR1, AGTMR2, AGTIOC, AGTISR, and AGTCMSR.

25.4.2 Access to Counter Register

When the TSTART and TCSTF bits in the AGTCR register are both 1 (count starts), allow at least 3 cycles of the count source clock between writes when writing to the AGT register successively.

Table 25.11 AGT中断源

Name	中断源	DMAC/DTC activation
AGTn_AGTI	当计数器下溢时 当在脉冲宽度测量模式下完成外部输入(AGTIO)的有效宽度测量时 当在脉冲周期测量模式下输入外部输入(AGTIO)的设置边沿时。	Possible
AGTn_AGTCMAI	当AGT和AGTCMA的值匹配时	Possible
AGTn_AGTCMBI	当AGT和AGTCMB的值匹配时	Possible

Note: 通道号（n=0或1）。

25.3.12 事件信号输出到ELC

AGT使用事件链接控制器(ELC)使用中断请求信号作为事件信号执行到指定模块的链接操作。AGT输出比较匹配A、比较匹配B和下溢测量完成信号作为事件信号。有关详细信息，请参阅第19节，事件链接控制器(ELC)。

25.4 使用说明

25.4.1 计数操作启动和停止控制

- 当操作模式（见表25.1）设置为非事件计数器模式，或计数源设置为非AGT0下溢时（TCK[2:0]=101b）
  - 在计数停止期间将1（计数开始）写入AGTCR寄存器中的TSTART位后，AGTCR寄存器中的TCSTF标志在计数源的3个周期内保持为0（计数停止）。在此位设置为1（正在进行计数）之前，不要访问与AGT*1相关的寄存器，而不是TCSTF标志。
  - 在计数操作期间将0（计数停止）写入TSTART位后，TCSTF标志在计数源的3个周期内保持为1。当TCSTF标志设置为0时，计数停止。在此位设置为0之前，请勿访问与AGT*1相关的寄存器，而不是TCSTF标志。
  - 在将TSTART位从0更改为1之前清除中断寄存器。参见第14节，中断控制器单位(ICU)了解详情。

注1.与AGT相关的寄存器：AGT、AGTCMA、AGTCMB、AGTCR、AGTMR1、AGTMR2、AGTIOC、AGTISR和AGTCMSR。

- 当工作模式（见表25.1）设置为事件计数器模式，或计数源设置为AGT0下溢时（TCK[2:0]=101b）
  - 在停止计数的同时将1（计数开始）写入AGTCR寄存器中的TSTART位后，AGTCR寄存器中的TCSTF位在PCLKB的2个周期内保持为0（计数停止）。不要访问除TCSTF位之外的与AGT*1关联的寄存器，直到该位设置为1（正在进行计数）。
  - 在计数操作期间将0（计数停止）写入TSTART位后，TCSTF位在PCLKB的2个周期内保持为1。当TCSTF位设置为0时，停止计数。在此位设置为0之前，请勿访问与AGT*1相关的寄存器，而不是TCSTF位。
  - 在将TSTART位从0更改为1之前清除中断寄存器。参见第14节，中断控制器单位(ICU)了解详情。

注1.与AGT相关的寄存器：AGT、AGTCMA、AGTCMB、AGTCR、AGTMR1、AGTMR2、AGTIOC、AGTISR和AGTCMSR。

25.4.2 访问计数器寄存器

当AGTCR寄存器中的TSTART和TCSTF位都为1（计数开始）时，连续写入AGT寄存器时，在两次写入之间至少允许计数源时钟的3个周期。

25.4.3 When Changing Mode

The registers associated with AGT operating mode (AGTMR1, AGTMR2, AGTIOC, AGTISR, AGTCMSR and AGTIOC) can be changed only when the count is stopped with both the TSTART and TCSTF bits set to 0 (count stops). Do not change these registers during count operation.

When the registers associated with AGT operating mode are changed, the values of bits TEDGF, TUNDF, TCMAF and TCMBF are undefined. Before starting the count, write 0 to the following bits:

- TEDGF (no active edge received)
- TUNDF (no underflow)
- TCMAF (no match)
- TCMBF (no match).

25.4.4 Digital Filter

When using the digital filter, do not start the timer operation for 5 cycles of the digital filter clock after setting bits TIPF[1:0] and when the TEDGSEL bit in the AGTIOC register changes.

25.4.5 How to Calculate Event Number, Pulse Width, and Pulse Period

- In event counter mode, event number is expressed mathematically as follows:
  Event number = initial value of counter [AGT register] - counter value of active event end
- In pulse width measurement mode, pulse width is expressed mathematically as follows:
  Pulse width = counter value of stopping measurement - counter value of next stopping measurement
- In pulse period measurement mode, input pulse period is expressed mathematically as follows:
  Period of input pulse = (initial value of counter [AGT register] - reading value of the read-out buffer) + 1

25.4.6 When Count Is Forcibly Stopped by TSTOP Bit

After the counter is forcibly stopped by the TSTOP bit in the AGTCR register, do not access the following I/O registers for 1 cycle of the count source:

- AGT
- AGTCMA
- AGTCMB
- AGTCR
- AGTMR1
- AGTMR2.

25.4.7 When Selecting AGT0 Underflow as the Count Source

Operate the AGT according to the procedures described in this section when selecting the underflow signal of AGT as the count source.

(1) Procedure for starting operation

1. Set AGT0 and AGT1.
2. Start the count operation of AGT1.
3. Start the count operation of AGT0.

(2) Procedure for stopping operation

1. Stop the count operation of AGT0.
2. Stop the count operation of AGT1.
3. Stop the count source clock of AGT1 (write 000b in the AGT1.AGTMR1.TCK[2:0] bits).

25.4.3 更改模式时

与AGT操作模式相关的寄存器（AGTMR1、AGTMR2、AGTIOC、AGTISR、AGTCMSR和只有在TSTART和TCSTF位都设置为0（计数停止）的情况下停止计数时才能更改AGTIOC）。在计数操作期间不要更改这些寄存器。

当与AGT工作模式相关的寄存器发生变化时，TEDGF、TUNDF、TCMAF和TCMBF未定义。在开始计数之前，将0写入以下位：

- TEDGF（未收到有效边沿）
- TUNDF (no underflow)
- TCMAF (no match)
- TCMBF (no match).

25.4.4 数字滤波器

使用数字滤波器时，设置位后在数字滤波器时钟的5个周期内不要启动定时器操作TIPF[1:0]以及AGTIOC寄存器中的TEDGSEL位发生变化时。

25.4.5 如何计算事件编号、脉冲宽度和脉冲周期

- 在事件计数器模式下，事件编号以数学方式表示如下：
  事件编号=计数器的初始值[AGT寄存器]活动事件结束的计数器值
- 在脉冲宽度测量模式下，脉冲宽度在数学上表示如下：
  脉冲宽度=停止测量的计数器值下一个停止测量的计数器值
- 在脉冲周期测量模式下，输入脉冲周期在数学上表示如下：
  输入脉冲周期=（计数器初始值[AGT寄存器]读出缓冲器的读取值）+1

25.4.6 当计数被TSTOP位强制停止时

计数器被AGTCR寄存器中的TSTOP位强制停止后，在计数源的1个周期内不要访问以下IO寄存器：

- AGT
- AGTCMA
- AGTCMB
- AGTCR
- AGTMR1
- AGTMR2.

25.4.7 选择AGT0下溢作为计数源时

选择AGT的下溢信号作为计数源时，请按照本节所述的步骤操作AGT。

(1) 开始运行的步骤

1. 设置AGT0和AGT1。
2. 启动AGT1的计数操作。
3. 启动AGT0的计数操作。

(2) 停止运行的步骤

1. 停止AGT0的计数操作。
2. 停止AGT1的计数操作。
3. 停止AGT1的计数源时钟（在AGT1.AGTMR1.TCK[2:0]位中写入000b）。

25.4.8 Reset of I/O Register

The I/O register of the AGT is not initialized by some types of resets. For details, see section 6, Resets.

25.4.9 When Selecting PCLKB, PCLKB/8, or PCLKB/2 as the Count Source

When a reset is generated, the operation of the AGT cannot be guaranteed. Set the registers associated with AGT again.

25.4.10 When Selecting AGTSCLK or AGTLCLK as the Count Source

The MSTPD2 bit in the MSTPCRD register must be set to 1 except when accessing the AGT1 registers. The MSTPD3 bit in the MSTPCRD register must be set to 1 except when accessing the AGT0 registers. When a reset occurs while MSTPD2 or MSTPD3 bit is 0, the operation of AGT1 or AGT0 cannot be guaranteed. Set the registers associated with AGT again.

25.4.11 When Switching Source Clock

When switching a clock source by changing SCKSCR.CKSEL[2:0], the clock output from the selector stops for 4 cycles of the switched clock. Therefore, when using the AGTIOn, AGTEEn, or both input as external event input, the clock source should not be switched. If switching the clock source while using the external event input, extend the input pulse width by 4 clock cycles of the switched source clock cycles.

25.4.8 IO寄存器的复位

AGT的IO寄存器不会被某些类型的复位初始化。有关详细信息，请参阅第6节，重置。

25.4.9 选择PCLKB、PCLKB8或PCLKB2作为计数源时

当产生复位时，不能保证AGT的操作。再次设置与AGT关联的寄存器。

25.4.10 选择AGTSCLK或AGTLCLK作为计数源时

除了访问AGT1寄存器时，MSTPCRD寄存器中的MSTPD2位必须设置为1。除了访问AGT0寄存器时，MSTPCRD寄存器中的MSTPD3位必须设置为1。当MSTPD2或MSTPD3位为0时发生复位时，不能保证AGT1或AGT0的操作。设置相关的寄存器

AGT again.

25.4.11 切换源时钟时

当通过改变SCKSCR.CKSEL[2:0]来切换时钟源时，选择器的时钟输出在切换时钟的4个周期内停止。因此，当使用AGTIOn、AGTEEn或两者输入作为外部事件输入时，不应切换时钟源。如果在使用外部事件输入时切换时钟源，请将输入脉冲宽度延长4个切换源时钟周期的时钟周期。

26. Realtime Clock (RTC)

26.1 Overview

The RTC has two counting modes, calendar count mode and binary count mode, that are used by switching register settings. For calendar count mode, the RTC has a 100 year calendar from 2000 to 2099 and automatically adjusts dates for leap years. For binary count mode, the RTC counts seconds and retains the information as a serial value. Binary count mode can be used for calendars other than the Gregorian (Western) calendar.

The sub-clock oscillator or LOCO can be selected as the count source of the time counters. The RTC uses a 128-Hz clock acquired by dividing the count source by a prescaler. Year, month, date, day-of-week, a.m./p.m. (in 12-hour mode), hour, minute, second, or 32-bit binary is counted by 1/128 second.

Table 26.1 lists the RTC specifications, Figure 26.1 shows a block diagram, and Table 26.2 lists the I/O pins.

Table 26.1 RTC specifications

Parameter	Specifications
Count mode	Calendar count mode/binary count mode
Count source*1	Sub-clock oscillator (XCIN) or LOCO
Clock and calendar functions	• Calendar count mode Year, month, date, day of week, hour, minute, second are counted, BCD display 12 hours/24 hours mode switching function 30 seconds adjustment function (a number less than 30 is rounded down to 00 seconds, and 30 seconds or more are rounded up to 1 minute) Automatic adjustment function for leap years • Binary count mode Count seconds in 32 bits, binary display • Shared by both modes Start/stop function The sub-second digit is displayed in binary units (1 Hz, 2 Hz, 4 Hz, 8 Hz, 16 Hz, 32 Hz, or 64 Hz) Clock error correction function Clock (1-Hz/64-Hz) output.
Interrupts	• Alarm interrupt (RTC_ALM) As an alarm interrupt condition, selectable for comparison with the following: Calendar count mode: Year, month, date, day-of-week, hour, minute, or second can be selected Binary count mode: Each bit of the 32-bit binary counter • Periodic interrupt (RTC_PRD) 2 seconds, 1 second, 1/2 second, 1/4 second, 1/8 second, 1/16 second, 1/32 second, 1/64 second, 1/128 second, or 1/256 second can be selected as an interrupt period • Carry interrupt (RTC_CUP) An interrupt is generated at either of the following conditions: - When a carry from the 64-Hz counter to the second counter is generated - When the 64-Hz counter is changed and the R64CNT register is read at the same time • Return from Software Standby mode or Deep Software Standby mode can be performed by an alarm interrupt or periodic interrupt.
Time capture function	• Times can be captured when the edge of the time capture event input pin is detected. For every event input, month, date, hour, minute, and second are captured or the 32-bit binary counter value is captured.
Event link function	Periodic event output (RTC_PRD)

Note 1. The frequency of the peripheral module clock (PCLKB) must be ≥ the frequency of the count source clock.

26. 实时时钟(RTC)

26.1 Overview

RTC有两种计数模式，日历计数模式和二进制计数模式，通过切换寄存器设置使用。对于日历计数模式，RTC有一个从2000年到2099年的100年日历，并自动调整闰年的日期。对于二进制计数模式，RTC会计算秒数并将信息保留为序列值。二进制计数模式可用于公历（西方）以外的日历。

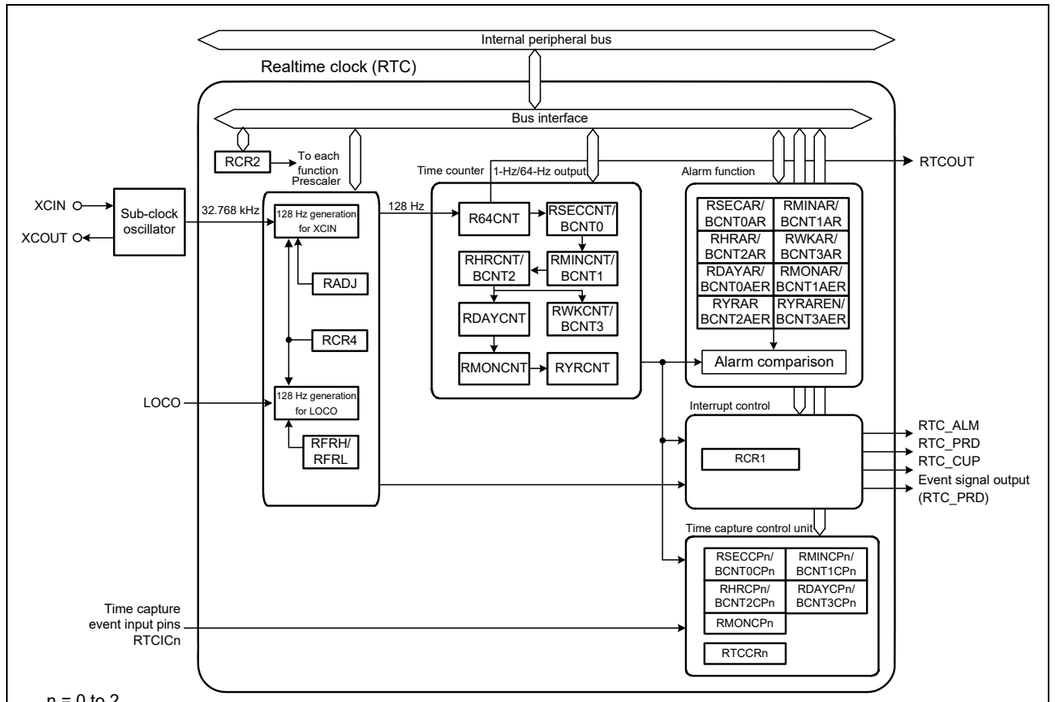
可以选择子时钟振荡器或LOCO作为时间计数器的计数源。RTC使用一个128-Hz时钟，通过预分频器将计数源分频获得。年、月、日、星期、上午、下午（在12小时模式下）时、分、秒或32位二进制按1128秒计数。

表26.1列出了RTC规范，图26.1显示了框图，表26.2列出了IO引脚。

Table 26.1 RTC specifications

Parameter	Specifications
计数模式	日历计数模式二进制计数模式
Count source*1	副时钟振荡器(XCIN)或LOCO
时钟和日历功能	日历计数模式 年、月、日、星期、时、分、秒计数，BCD显示12小时24小时模式切换功能30秒调整功能（小于30的数字向下舍入为00秒，大于等于30秒为四舍五入到1分钟）闰年自动调整功能 二进制计数模式 以32位计数秒，二进制显示 两种模式共享 启动停止功能 亚秒数字以二进制单位显示（1Hz、2Hz、4Hz、8Hz、16Hz、32Hz或64Hz） 时钟纠错功能 时钟(1-Hz64-Hz)输出。
Interrupts	报警中断(RTC_ALM) 作为报警中断条件，可选择用于与以下比较： 日历计数模式：可选择年、月、日、星期、小时、分钟或秒 二进制计数模式：32位二进制计数器的每一位 周期性中断(RTC_PRD) 可以选择2秒、1秒、12秒、14秒、18秒、116秒、132秒、164秒、1128秒或1256秒作为中断周期 进位中断（RTC_CUP） 在以下任一情况下会产生中断：当从64-Hz计数器到第二个计数器产生进位时当64-Hz计数器改变并同时读取R64CNT寄存器时 从软件待机模式返回或深度软件待机模式可以通过警报中断或周期性中断来执行。
时间捕捉功能	当检测到时间捕捉事件输入引脚的边沿时，可以捕捉时间。 对于每个事件输入，都会捕获月、日、小时、分钟和秒，或者捕获32位二进制计数器值。
事件链接功能	周期性事件输出(RTC_PRD)

Note 1. 外围模块时钟(PCLKB)的频率必须是 计数源时钟的频率。

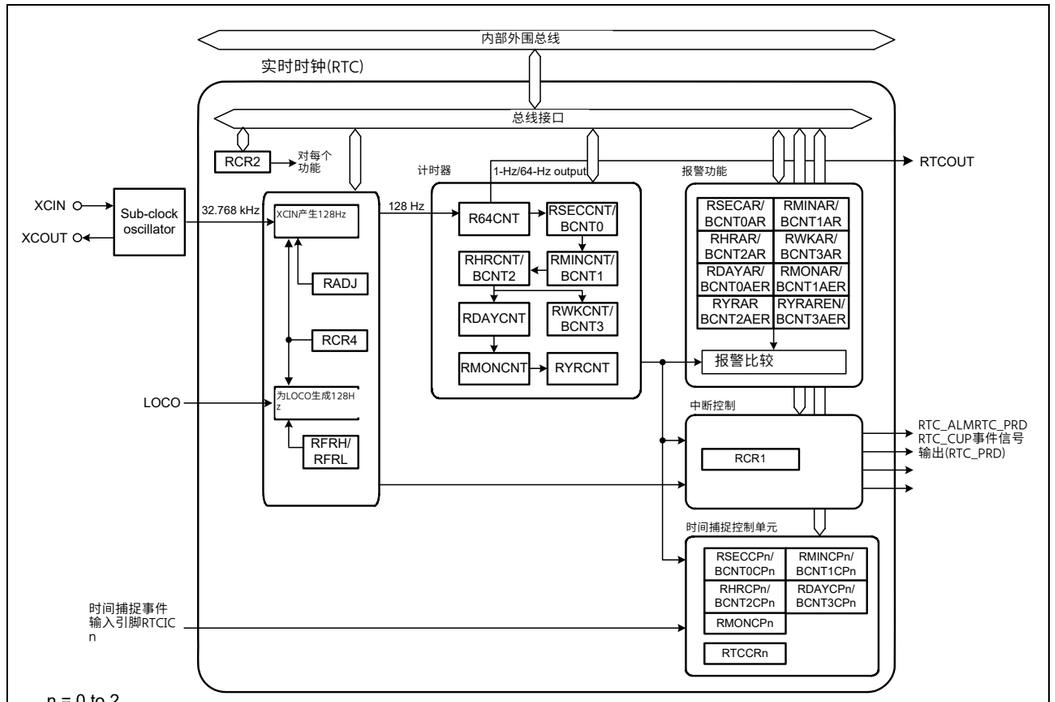


R64CNT:	64-Hz counter	RFRH/RFRL:	Frequency Register
RSECCNT/BCNT0:	Second Counter/Binary Counter 0	RMINAR/BCNT1AR:	Minute Alarm Register/Binary Counter 1 Alarm Register
RMINCNT/BCNT1:	Minute Counter/Binary Counter 1	RHRAR/BCNT2AR:	Hour Alarm Register/Binary Counter 2 Alarm Register
RHRCNT/BCNT2:	Hour Counter/Binary Counter 2	RWKAR/BCNT3AR:	Day-of-week Alarm Register/Binary Counter 3 Alarm Register
RWKCNT/BCNT3:	Day-of-week Counter/Binary Counter 3	RDAYAR/BCNT0AER:	Date Alarm Register/Binary Counter 0 Alarm Enable Register
RDAYCNT:	Date Counter	RMONAR/BCNT1AER:	Month Alarm Register/Binary Counter 1 Alarm Enable Register
RMONCNT:	Month Counter	RYRAR/BCNT2AER:	Year Alarm Register/Binary Counter 2 Alarm Enable Register
RYRCNT:	Year Counter	RYRAREN/BCNT3AER:	Year Alarm Enable Register/Binary Counter 3 Alarm Enable Register
RCR1:	Rtc Control Register 1	RTCCRn:	Time Capture Control Register n
RCR2:	Rtc Control Register 2	RSECCPn/BCNT0CPn:	Second Capture Register n/bcnt0 Capture Register n
RCR4:	Rtc Control Register 4	RMINCPn/BCNT1CPn:	Minute Capture Register n/bcnt1 Capture Register n
RADJ:	Time Error Adjustment Register	RHRCPn/BCNT2CPn:	Hour Capture Register n/bcnt2 Capture Register n
RSECAR/BCNT0AR:	Second Alarm Register/binary Counter 0 Alarm Register	RDAYCPn/BCNT3CPn:	Date Capture Register n/bcnt3 Capture Register n
		RMONCPn:	Month Capture Register n

Figure 26.1 RTC block diagram

Table 26.2 RTC pin configuration

Pin name	I/O	Function
XCIN	Input	Connect a 32.768-kHz crystal to these pins
XCOUT	Output	
RTCOUT	Output	This pin is used to output a 1-Hz/64-Hz waveform, but not in Deep Software Standby mode
RTCIC0	Input	Time capture event input pins. RTCIC0 to RTCIC2 can be controlled by the VBTICTLR register. For more information, see section 12, Battery Backup Function and section 20, I/O Ports.
RTCIC1	Input	
RTCIC2	Input	



R64CNT:	64-Hz counter	RFRH/RFRL:	频率寄存器
RSECCNT/BCNT0:	第二个计数器二进制计数器0	RMINAR/BCNT1AR:	分钟报警寄存器二进制计数器1报警寄存器
RMINCNT/BCNT1:	分计数器二进制计数器1	RHRAR/BCNT2AR:	小时报警寄存器二进制计数器2报警寄存器
RHRCNT/BCNT2:	小时计数器二进制计数器2	RWKAR/BCNT3AR:	星期报警寄存器二进制计数器3报警寄存器
RWKCNT/BCNT3:	Day-of-week Counter/Binary Counter 3	RDAYAR/BCNT0AER:	日期报警寄存器二进制计数器0报警使能寄存器
RDAYCNT:	日期计数器	RMONAR/BCNT1AER:	月报警寄存器二进制计数器1报警使能寄存器
RMONCNT:	月计数器	RYRAR/BCNT2AER:	年报警寄存器二进制计数器2报警使能寄存器
RYRCNT:	年计数器	RYRARENBCNT3AER:	年闹钟使能寄存器二进制计数器3闹钟使能Register
RCR1:	Rtc控制寄存器1	RTCCRn:	时间捕捉控制寄存器n
RCR2:	Rtc控制寄存器2	RSECCPn/BCNT0CPn:	第二个捕捉寄存器nbcnt0捕捉寄存器n
RCR4:	Rtc控制寄存器4	RMINCPn/BCNT1CPn:	分钟捕捉寄存器nbcnt1捕捉寄存器n
RADJ:	时间误差调整寄存器	RHRCPn/BCNT2CPn:	小时捕捉寄存器nbcnt2捕捉寄存器n
RSCARBCNT0AR:	第二个报警寄存器二进制计数器0报警寄存器	RDAYCPn/BCNT3CPn:	日期捕捉寄存器nbcnt3捕捉寄存器n
		RMONCPn:	月捕获寄存器n

Figure 26.1 实时时钟框图

Table 26.2 RTC引脚配置

引脚名称	I/O	Function
XCIN	Input	将32.768kHz晶振连接到这些引脚
XCOUT	Output	
RTCOUT	Output	此引脚用于输出1-Hz64-Hz波形，但不在深度软件待机模式下
RTCIC0	Input	时间捕捉事件输入引脚。 RTCIC0至RTCIC2可由VBTICTLR寄存器控制。 有关详细信息，请参阅第12节，电池备份功能和第20节，IO端口。
RTCIC1	Input	
RTCIC2	Input	

26.2 Register Descriptions

Write or read from the RTC registers as described in section 26.6.5, Notes on Writing to and Reading from Registers.

If the value in an RTC register after a reset is given as x (undefined bits) in the list, it is not initialized by a reset. When RTC enters the reset state or a low power consumption state during counting operations, for example while the RCR2.START bit is 1, the year, month, day of the week, date, hours, minutes, seconds, and 64-Hz counters continue to operate.

Note: A reset generated while writing to a register might destroy the register value. In addition, do not allow the chip to enter Software Standby mode or Deep Software Standby mode immediately after setting any of these registers. For details, see section 26.6.4, Transitions to Low Power Modes after Setting Registers.

26.2.1 64-Hz Counter (R64CNT)

Address(es): RTC.R64CNT 4004 4000h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	F1HZ	F2HZ	F4HZ	F8HZ	F16HZ	F32HZ	F64HZ
Value after reset:	0	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b0	F64HZ	64 Hz	Indicates the state between 1 Hz and 64 Hz of the sub-second digit	R
b1	F32HZ	32 Hz		R
b2	F16HZ	16 Hz		R
b3	F8HZ	8 Hz		R
b4	F4HZ	4 Hz		R
b5	F2HZ	2 Hz		R
b6	F1HZ	1 Hz		R
b7	—	Reserved	This bit is read as 0.	R

The R64CNT counter is used in both calendar count mode and in binary count mode. The 64-Hz counter (R64CNT) generates the period for a second by counting up periods of the 128-Hz clock. The state in the sub-second range can be confirmed by reading this counter.

This counter is cleared to 00h by an RTC software reset or an execution of a 30-second adjustment. To read this counter, follow the procedure in section 26.3.5, Reading 64-Hz Counter and Time.

26.2.2 Second Counter (RSECCNT)/Binary Counter 0 (BCNT0)

(1) In calendar count mode

Address(es): RTC.RSECCNT 4004 4002h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	SEC10[2:0]			SEC1[3:0]			
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b3 to b0	SEC1[3:0]	1-Second Count	Counts from 0 to 9 every second. When a carry is generated, 1 is added to the tens place.	R/W

26.2 注册说明

写入或读取RTC寄存器，如第26.6.5节“写入和读取寄存器的注意事项”中所述。

如果复位后RTC寄存器中的值在列表中以x（未定义位）的形式给出，则它不会被复位初始化。当RTC在计数操作期间进入复位状态或低功耗状态时，例如当
RCR2.START位为1，年、月、星期、日期、小时、分钟、秒和64-Hz计数器继续工作。

Note: 写入寄存器时产生的复位可能会破坏寄存器值。此外，不要让芯片在设置这些寄存器后立即进入软件待机模式或深度软件待机模式。有关详细信息，请参阅第26.6.4节，设置寄存器后转换到低功耗模式。

26.2.1 64-Hz Counter (R64CNT)

Address(es): RTC.R64CNT 4004 4000h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	F1HZ	F2HZ	F4HZ	F8HZ	F16HZ	F32HZ	F64HZ
重置后的值：	0	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b0	F64HZ	64 Hz	指示亚秒数位1Hz到64Hz之间的状态	R
b1	F32HZ	32 Hz		R
b2	F16HZ	16 Hz		R
b3	F8HZ	8 Hz		R
b4	F4HZ	4 Hz		R
b5	F2HZ	2 Hz		R
b6	F1HZ	1 Hz		R
b7	—	Reserved	该位读为0。	R

R64CNT计数器用于日历计数模式和二进制计数模式。64-Hz计数器(R64CNT)通过向上计数128-Hz时钟的周期来生成一秒的周期。亚秒范围内的状态可以通过读取该计数器来确认。

通过RTC软件复位或执行30秒调整，该计数器清零。要读取此计数器，请按照第26.3.5节，读取64-Hz计数器和时间中的程序进行操作。

26.2.2 第二个计数器(RSECCNT)二进制计数器0(BCNT0)

(1) 在日历计数模式下

Address(es): RTC.RSECCNT 4004 4002h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	SEC10[2:0]			SEC1[3:0]			
重置后的值：	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b3 to b0	SEC1[3:0]	1-Second Count	每秒从0计数到9。产生进位时，十位加1。	R/W

Bit	Symbol	Bit name	Description	R/W
b6 to b4	SEC10[2:0]	10-Second Count	Counts from 0 to 5 for 60-second counting.	R/W
b7	—	Reserved	Set this bit to 0. It is read as the set value.	R/W

The RSECCNT counter sets and counts the BCD-coded second value. It counts the carries generated once per second in the 64-Hz counter.

The setting range is decimal 00 to 59. The RTC does not operate normally if any other value is set. Before writing to this register, be sure to stop the count operation using the START bit in RCR2.

To read this counter, follow the procedure in section 26.3.5, Reading 64-Hz Counter and Time.

(2) In binary count mode

Address(es): RTC.BCNT0 4004 4002h

	b7	b6	b5	b4	b3	b2	b1	b0
	BCNT[7:0]							
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

BCNT0 is a read/write 32-bit binary counter b7 to b0 that performs count operation by a carry generated for each second of the 64-Hz counter. Before writing to this register, you must stop the count operation using the START bit in RCR2. To read this counter, follow the procedure in section 26.3.5, Reading 64-Hz Counter and Time.

26.2.3 Minute Counter (RMINCNT)/Binary Counter 1 (BCNT1)

(1) In calendar count mode

Address(es): RTC.RMINCNT 4004 4004h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	MIN10[2:0]			MIN1[3:0]			
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b3 to b0	MIN1[3:0]	1-Minute Count	Counts from 0 to 9 every minute. When a carry is generated, 1 is added to the tens place.	R/W
b6 to b4	MIN10[2:0]	10-Minute Count	Counts from 0 to 5 for 60-minute counting.	R/W
b7	—	Reserved	Set this bit to 0. It is read as the set value.	R/W

The RMINCNT counter sets and counts the BCD-coded minute value. It counts the carries generated once every minute in the second counter.

A value from 00 through 59 (in BCD) can be specified. If a value outside of this range is specified, the RTC does not operate correctly. Before writing to this register, be sure to stop the count operation using the START bit in RCR2. To read this counter, follow the procedure in section 26.3.5, Reading 64-Hz Counter and Time.

Bit	Symbol	位名称	Description	R/W
b6 to b4	SEC10[2:0]	10-Second Count	从0到5计数60秒。	R/W
b7	—	Reserved	将此位设置为0。它作为设置值读取。	R/W

RSECCNT计数器设置并计算BCD编码的第二个值。它对64-Hz计数器中每秒生成一次的进位进行计数。

设置范围为十进制00到59。如果设置任何其他值，RTC将无法正常工作。在写入该寄存器之前，请务必使用RCR2中的START位停止计数操作。

要读取此计数器，请按照第26.3.5节，读取64-Hz计数器和时间中的程序进行操作。

(2) 二进制计数模式

Address(es): RTC.BCNT0 4004 4002h

	b7	b6	b5	b4	b3	b2	b1	b0
	BCNT[7:0]							
重置后的值:	x	x	x	x	x	x	x	x

x: Undefined

BCNT0是一个读写32位二进制计数器b7到b0，它通过为64-Hz计数器的每一秒生成的进位执行计数操作。在写入该寄存器之前，您必须使用RCR2中的START位停止计数操作。要读取此计数器，请按照第26.3.5节，读取64-Hz计数器和时间中的程序进行操作。

26.2.3 分钟计数器(RMINCNT)二进制计数器1(BCNT1)

(1) 在日历计数模式下

Address(es): RTC.RMINCNT 4004 4004h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	MIN10[2:0]			MIN1[3:0]			
重置后的值:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b3 to b0	MIN1[3:0]	1-Minute Count	每分钟从0数到9。产生进位时，十位加1。	R/W
b6 to b4	MIN10[2:0]	10-Minute Count	从0到5计数60分钟。	R/W
b7	—	Reserved	将此位设置为0。它作为设置值读取。	R/W

RMINCNT计数器设置并计算BCD编码的分钟值。它对第二个计数器中每分钟产生一次的进位进行计数。

可以指定从00到59的值（以BCD表示）。如果指定的值超出此范围，则RTC将无法正确运行。在写入该寄存器之前，请务必使用RCR2中的START位停止计数操作。要读取此计数器，请按照第26.3.5节，读取64-Hz计数器和时间中的程序进行操作。

(2) In binary count mode

Address(es): RTC.BCNT1 4004 4004h

	b7	b6	b5	b4	b3	b2	b1	b0
	BCNT[15:8]							
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

BCNT1 is a read/write 32-bit binary counter b15 to b8 that performs count operation by a carry generated for each second of the 64-Hz counter. Before writing to this register, be sure to stop the count operation using the START bit in RCR2. To read this counter, follow the procedure in section 26.3.5, Reading 64-Hz Counter and Time.

26.2.4 Hour Counter (RHRCNT)/Binary Counter 2 (BCNT2)

(1) In calendar count mode

Address(es): RTC.RHRCNT 4004 4006h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	PM	HR10[1:0]		HR1[3:0]			
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b3 to b0	HR1[3:0]	1-Hour Count	Counts from 0 to 9 once per hour. When a carry is generated, 1 is added to the tens place.	R/W
b5, b4	HR10[1:0]	10-Hour Count	Counts from 0 to 2 once per carry from the ones place.	R/W
b6	PM	PM	AM/PM select for time counter setting. 0: AM 1: PM.	R/W
b7	—	Reserved	Set this bit to 0. It is read as the set value.	R/W

The RHRCNT counter sets and counts the BCD-coded hour value. It counts the carries generated once per hour in the minute counter. The specifiable time differs based on the setting in the hours mode bit (RCR2.HR24):

- When the RCR2.HR24 bit is 0 — from 00 to 11 (in BCD)
- When the RCR2.HR24 bit is 1 — from 00 to 23 (in BCD).

If a value outside of this range is specified, the RTC does not operate correctly. Before writing to this register, be sure to stop the count operation using the START bit in RCR2. The PM bit is only enabled when the RCR2.HR24 bit is 0. Otherwise, the setting in the PM bit has no effect. To read this counter, follow the procedure in section 26.3.5, Reading 64-Hz Counter and Time.

(2) In binary count mode

Address(es): RTC.BCNT2 4004 4006h

	b7	b6	b5	b4	b3	b2	b1	b0
	BCNT[23:16]							
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

BCNT2 is a read/write 32-bit binary counter b23 to b16 that performs count operation by a carry generated for each second of the 64-Hz counter. Before writing to this register, be sure to stop the count operation using the START bit in

(2) 二进制计数模式

Address(es): RTC.BCNT1 4004 4004h

	b7	b6	b5	b4	b3	b2	b1	b0
	BCNT[15:8]							
重置后的值：	x	x	x	x	x	x	x	x

x: Undefined

BCNT1是一个读写32位二进制计数器b15到b8，它通过为64-Hz计数器的每一秒生成的进位执行计数操作。在写入该寄存器之前，请务必使用RCR2中的START位停止计数操作。要读取此计数器，请按照第26.3.5节，读取64-Hz计数器和时间中的程序进行操作。

26.2.4 小时计数器(RHRCNT)二进制计数器2(BCNT2)

(1) 在日历计数模式下

Address(es): RTC.RHRCNT 4004 4006h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	PM	HR10[1:0]		HR1[3:0]			
重置后的值：	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b3 to b0	HR1[3:0]	1-Hour Count	每小时从0数到9次。产生进位时，十位加1。	R/W
b5, b4	HR10[1:0]	10-Hour Count	每次从个位进行一次从0计数到2。	R/W
b6	PM	PM	AMPM选择时间计数器设置。0：上午 1：下午。	R/W
b7	—	Reserved	将此位设置为0。它作为设置值读取。	R/W

RHRCNT计数器设置并计算BCD编码的小时值。它在分钟计数器中计算每小时生成一次的进位。可指定的时间因小时模式位(RCR2.HR24)中的设置而异：

- 当RCR2.HR24位为0时——从00到11（以BCD表示）
- 当RCR2.HR24位为1时—从00到23（以BCD表示）。

如果指定的值超出此范围，则RTC将无法正确运行。在写入该寄存器之前，请务必使用RCR2中的START位停止计数操作。仅当RCR2.HR24位为0时才启用PM位。否则，PM位中的设置无效。要读取此计数器，请按照第26.3.5节，读取64-Hz计数器和时间中的程序进行操作。

(2) 二进制计数模式

Address(es): RTC.BCNT2 4004 4006h

	b7	b6	b5	b4	b3	b2	b1	b0
	BCNT[23:16]							
重置后的值：	x	x	x	x	x	x	x	x

x: Undefined

BCNT2是一个读写32位二进制计数器b23到b16，它通过为64-Hz计数器的每一秒生成的进位执行计数操作。在写入该寄存器之前，请务必使用START位停止计数操作

RCR2. To read this counter, follow the procedure in section 26.3.5, Reading 64-Hz Counter and Time.

26.2.5 Day-of-Week Counter (RWKCNT)/Binary Counter 3 (BCNT3)

(1) In calendar count mode

Address(es): RTC.RWKCNT 4004 4008h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	DAYW[2:0]		
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b2 to b0	DAYW[2:0]	Day-of-Week Counting	b2 b0 0 0 0: Sunday 0 0 1: Monday 0 1 0: Tuesday 0 1 1: Wednesday 1 0 0: Thursday 1 0 1: Friday 1 1 0: Saturday 1 1 1: Setting prohibited.	R/W
b7 to b3	—	Reserved	Set these bits to 0. They are read as the set value.	R/W

The RWKCNT counter sets and counts in the coded day-of-week value. It counts the carries generated once per day in the hour counter. A value from 0 through 6 can be specified. If a value outside of this range is specified, the RTC does not operate correctly. Before writing to this register, be sure to stop the count operation using the START bit in RCR2. To read this counter, follow the procedure in section 26.3.5, Reading 64-Hz Counter and Time.

(2) In binary count mode

Address(es): RTC.BCNT3 4004 4008h

	b7	b6	b5	b4	b3	b2	b1	b0
	BCNT[31:24]							
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

BCNT3 is a read/write 32-bit binary counter b31 to b24 that performs count operation by a carry generated for each second of the 64-Hz counter. Before writing to this register, be sure to stop the count operation using the START bit in RCR2. To read this counter, follow the procedure in section 26.3.5, Reading 64-Hz Counter and Time.

RCR2。要读取此计数器，请按照第26.3.5节，读取64-Hz计数器和时间中的程序进行操作。

26.2.5 星期计数器(RWKCNT)二进制计数器3(BCNT3)

(1) 在日历计数模式下

Address(es): RTC.RWKCNT 4004 4008h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	DAYW[2:0]		
重置后的值：	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b2 to b0	DAYW[2:0]	Day-of-Week Counting	b2b0000：星期日001： 星期一010：星期二011： 星期三100：星期四101： 星期五110：星期六111： 禁止设置。	R/W
b7 to b3	—	Reserved	将这些位设置为0。它们作为设置值读取。	R/W

RWKCNT计数器在编码的星期值中设置和计数。它计算小时计数器中每天生成一次的进位。可以指定从0到6的值。如果指定的值超出此范围，则RTC将无法正确运行。在写入该寄存器之前，请务必使用RCR2中的START位停止计数操作。要读取此计数器，请按照第26.3.5节，读取64-Hz计数器和时间中的程序进行操作。

(2) 二进制计数模式

Address(es): RTC.BCNT3 4004 4008h

	b7	b6	b5	b4	b3	b2	b1	b0
	BCNT[31:24]							
重置后的值：	x	x	x	x	x	x	x	x

x: Undefined

BCNT3是一个读写32位二进制计数器b31到b24，它通过为64-Hz计数器的每一秒生成的进位执行计数操作。在写入该寄存器之前，请务必使用RCR2中的START位停止计数操作。要读取此计数器，请按照第26.3.5节，读取64-Hz计数器和时间中的程序进行操作。

26.2.6 Day Counter (RDAYCNT)

Address(es): RTC.RDAYCNT 4004 400Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	DATE10[1:0]		DATE1[3:0]			
Value after reset:	0	0	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b3 to b0	DATE1[3:0]	1-Day Count	Counts from 0 to 9 once per day. When a carry is generated, 1 is added to the tens place.	R/W
b5, b4	DATE10[1:0]	10-Day Count	Counts from 0 to 3 once per carry from the ones place	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The RDAYCNT counter is used in calendar count mode to set and count the BCD-coded date value. It counts the carries generated once per day in the hour counter. The count operation depends on the month and whether the year is a leap year. Leap years are determined according to whether the year counter (RYRCNT) value is divisible by 400, 100, and 4.

A value from 01 through 31 (in BCD) can be specified. If a value outside of this range is specified, the RTC does not operate correctly. When specifying a value, the range of specifiable days depends on the month and whether the year is a leap year. Before writing to this register, be sure to stop the count operation using the START bit in RCR2. To read this counter, follow the procedure in section 26.3.5, Reading 64-Hz Counter and Time.

26.2.7 Month Counter (RMONCNT)

Address(es): RTC.RMONCNT 4004 400Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	MON10	MON1[3:0]			
Value after reset:	0	0	0	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b3 to b0	MON1[3:0]	1-Month Count	Counts from 0 to 9 once per month. When a carry is generated, 1 is added to the tens place.	R/W
b4	MON10	10-Month Count	Counts from 0 to 1 once per carry from the ones place.	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The RMONCNT counter is used in calendar count mode to set and count the BCD-coded month value. It counts the carries generated once per month in the date counter.

A value from 01 through 12 (in BCD) can be specified. If a value outside of this range is specified, the RTC does not operate correctly. Before writing to this register, be sure to stop the count operation using the START bit in RCR2. To read this counter, follow the procedure in section 26.3.5, Reading 64-Hz Counter and Time.

26.2.6 日计数器(RDAYCNT)

Address(es): RTC.RDAYCNT 4004 400Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	DATE10[1:0]		DATE1[3:0]			
重置后的值:	0	0	x	x	x	x	x	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b3 to b0	DATE1[3:0]	1-Day Count	每天从0数到9次。产生进位时，十位加1。	R/W
b5, b4	DATE10[1:0]	10-Day Count	每次从个位进位从0计数到3	R/W
b7, b6	—	Reserved	这些位被读取为0。写入值应为0。	R/W

RDAYCNT计数器用于日历计数模式以设置和计数BCD编码的日期值。它计算小时计数器中每天生成一次的进位。计数操作取决于月份以及年份是否为闰年。闰年根据年份计数器(RYRCNT)值是否可被400、100和4整除来确定。

可以指定从01到31的值（以BCD表示）。如果指定的值超出此范围，则RTC将无法正确运行。指定值时，可指定天数的范围取决于月份以及年份是否为闰年。在写入该寄存器之前，请务必使用RCR2中的START位停止计数操作。要读取此计数器，请按照第26.3.5节，读取64-Hz计数器和时间中的程序进行操作。

26.2.7 月计数器(RMONCNT)

Address(es): RTC.RMONCNT 4004 400Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	MON10	MON1[3:0]			
重置后的值:	0	0	0	x	x	x	x	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b3 to b0	MON1[3:0]	1-Month Count	每月从0数到9次。产生进位时，十位加1。	R/W
b4	MON10	10-Month Count	每次从个位进位从0到1计数一次。	R/W
b7 to b5	—	Reserved	这些位被读取为0。写入值应为0。	R/W

RMONCNT计数器用于日历计数模式以设置和计数BCD编码的月份值。它在日期计数器中计算每月生成一次的进位。

可以指定从01到12的值（以BCD表示）。如果指定的值超出此范围，则RTC将无法正确运行。在写入该寄存器之前，请务必使用RCR2中的START位停止计数操作。要读取此计数器，请按照第26.3.5节，读取64-Hz计数器和时间中的程序进行操作。

26.2.8 Year Counter (RYRCNT)

Address(es): RTC.RYRCNT 4004 400Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	YR10[3:0]				YR1[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b3 to b0	YR1[3:0]	1-Year Count	Counts from 0 to 9 once per year. When a carry is generated, 1 is added to the tens place.	R/W
b7 to b4	YR10[3:0]	10-Year Count	Counts from 0 to 9 once per carry from ones place. When a carry is generated in the tens place, 1 is added to the hundreds place.	R/W
b15 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The RYRCNT counter is used in calendar count mode to set and count the BCD-coded year value. It counts the carries generated once per year in the month counter.

A value from 00 through 99 (in BCD) can be specified. If a value outside of this range is specified, the RTC does not operate correctly. Before writing to this register, be sure to stop the count operation using the START bit in RCR2. To read this counter, follow the procedure in section 26.3.5, Reading 64-Hz Counter and Time.

26.2.9 Second Alarm Register (RSECAR)/Binary Counter 0 Alarm Register (BCNT0AR)

(1) In calendar count mode

Address(es): RTC.RSECAR 4004 4010h

	b7	b6	b5	b4	b3	b2	b1	b0
	ENB	SEC10[2:0]			SEC1[3:0]			
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b3 to b0	SEC1[3:0]	1 Second	Value for the ones place of seconds.	R/W
b6 to b4	SEC10[2:0]	10 Seconds	Value for the tens place of seconds.	R/W
b7	ENB	ENB	0: The register value is not compared with the RSECCNT counter value 1: The register value is compared with the RSECCNT counter value.	R/W

RSECAR is an alarm register associated with the BCD-coded second counter RSECCNT. When the ENB bit is set to 1, the RSECAR value is compared with the RSECCNT value. From the following alarm registers, only those selected with the ENB bits set to 1 are compared with the associated counters:

- RSECAR
- RMINAR
- RHRAR
- RWKAR
- RDAYAR
- RMONAR

26.2.8 年计数器(RYRCNT)

Address(es): RTC.RYRCNT 4004 400Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	YR10[3:0]				YR1[3:0]			
重置后的值:	0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b3 to b0	YR1[3:0]	1-Year Count	每年从0数到9次。产生进位时，十位加1。	R/W
b7 to b4	YR10[3:0]	10-Year Count	每次从一个地方进行一次从0到9计数。当十位产生进位时，百位加1。	R/W
b15 to b8	—	Reserved	这些位被读取为0。写入值应为0。	R/W

RYRCNT计数器在日历计数模式下用于设置和计数BCD编码的年份值。它计算月份计数器中每年生成一次的进位。

可以指定从00到99（BCD格式）的值。如果指定的值超出此范围，则RTC将无法正确运行。在写入该寄存器之前，请务必使用RCR2中的START位停止计数操作。要读取此计数器，请按照第26.3.5节，读取64-Hz计数器和时间中的程序进行操作。

26.2.9 第二个报警寄存器(RSECAR)二进制计数器0报警寄存器(BCNT0AR)

(1) 在日历计数模式下

Address(es): RTC.RSECAR 4004 4010h

	b7	b6	b5	b4	b3	b2	b1	b0
	ENB	SEC10[2:0]			SEC1[3:0]			
重置后的值:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b3 to b0	SEC1[3:0]	1 Second	以秒为单位的值。	R/W
b6 to b4	SEC10[2:0]	10 Seconds	十位秒的值。	R/W
b7	ENB	ENB	0：寄存器值不与RSECCNT计数器值比较1：寄存器值与RSECCNT计数器值比较。	R/W

RSCAR是与BCD编码的第二个计数器RSECCNT相关的警报寄存器。当ENB位设置为1时，RSCAR值与RSECCNT值进行比较。从以下报警寄存器中，只有选择ENB位设置为1的报警寄存器与相关计数器进行比较：

- RSECAR
- RMINAR
- RHRAR
- RWKAR
- RDAYAR
- RMONAR

- RYRAREN.

When all the respective values match, the IR flag associated with the RTC_ALM interrupt is set to 1. RSECAR values from 00 through 59 (in BCD) can be specified. If a value outside of this range is specified, the RTC does not operate correctly. This register is cleared to 00h by an RTC software reset.

(2) In binary count mode

Address(es): RTC.BCNT0AR 4004 4010h

	b7	b6	b5	b4	b3	b2	b1	b0
	BCNTAR[7:0]							
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

BCNT0AR is a read/write alarm register associated with the 32-bit binary counter b7 to b0. This register is cleared to 00h by an RTC software reset.

26.2.10 Minute Alarm Register (RMINAR)/Binary Counter 1 Alarm Register (BCNT1AR)

(1) In calendar count mode

Address(es): RTC.RMINAR 4004 4012h

	b7	b6	b5	b4	b3	b2	b1	b0
	ENB	MIN10[2:0]			MIN1[3:0]			
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b3 to b0	MIN1[3:0]	1 Minute	Value for the ones place of minutes	R/W
b6 to b4	MIN10[2:0]	10 Minutes	Value for the tens place of minutes	R/W
b7	ENB	ENB	0: The register value is not compared with the RMINCNT counter value 1: The register value is compared with the RMINCNT counter value.	R/W

RMINAR is an alarm register associated with the BCD-coded minute counter RMINCNT. When the ENB bit is set to 1, the RMINAR value is compared with the RMINCNT value. From the following alarm registers, only those selected with the ENB bits set to 1 are compared with the associated counters:

- RSECAR
- RMINAR
- RHRAR
- RWKAR
- RDAYAR
- RMONAR
- RYRAREN.

When all the respective values match, the IR flag associated with the RTC_ALM interrupt is set to 1. RMINAR values from 00 through 59 (in BCD) can be specified. If a value outside of this range is specified, the RTC does not operate correctly. This register is cleared to 00h by an RTC software reset.

- RYRAREN.

当所有各自的值都匹配时，与RTC_ALM中断相关的IR标志设置为1。可以指定从00到59（以BCD表示）的RSCAR值。如果指定的值超出此范围，则RTC将无法正确运行。该寄存器通过RTC软件复位清零。

(2) 二进制计数模式

Address(es): RTC.BCNT0AR 4004 4010h

	b7	b6	b5	b4	b3	b2	b1	b0
	BCNTAR[7:0]							
重置后的值：	x	x	x	x	x	x	x	x

x: Undefined

BCNT0AR是一个与32位二进制计数器b7到b0相关的读写警报寄存器。该寄存器通过RTC软件复位清零。

26.2.10 分钟报警寄存器(RMINAR)二进制计数器1报警寄存器(BCNT1AR)

(1) 在日历计数模式下

Address(es): RTC.RMINAR 4004 4012h

	b7	b6	b5	b4	b3	b2	b1	b0
	ENB	MIN10[2:0]			MIN1[3:0]			
重置后的值：	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b3 to b0	MIN1[3:0]	1 Minute	分钟个位数的值	R/W
b6 to b4	MIN10[2:0]	10 Minutes	十位分值	R/W
b7	ENB	ENB	0：寄存器值不与RMINCNT计数器值比较1：寄存器值与RMINCNT计数器值比较。	R/W

RMINAR是一个与BCD编码的分钟计数器RMINCNT相关的报警寄存器。当ENB位设置为1时，将RMINAR值与RMINCNT值进行比较。从以下报警寄存器中，只有选择ENB位设置为1的报警寄存器与相关计数器进行比较：

- RSECAR
- RMINAR
- RHRAR
- RWKAR
- RDAYAR
- RMONAR
- RYRAREN.

当所有各自的值都匹配时，与RTC_ALM中断相关的IR标志设置为1。可以指定从00到59（以BCD表示）的RMINAR值。如果指定的值超出此范围，则RTC将无法正确运行。该寄存器通过RTC软件复位清零。

(2) In binary count mode

Address(es): RTC.BCNT1AR 4004 4012h

	b7	b6	b5	b4	b3	b2	b1	b0
	BCNTAR[15:8]							
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

BCNT1AR is a read/write alarm register associated with the 32-bit binary counter from b15 to b8. This register is cleared to 00h by an RTC software reset.

26.2.11 Hour Alarm Register (RHRAR)/Binary Counter 2 Alarm Register (BCNT2AR)

(1) In calendar count mode

Address(es): RTC.RHRAR 4004 4014h

	b7	b6	b5	b4	b3	b2	b1	b0
	ENB	PM	HR10[1:0]		HR1[3:0]			
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b3 to b0	HR1[3:0]	1 Hour	Value for the ones place of hours	R/W
b5, b4	HR10[1:0]	10 Hours	Value for the tens place of hours	R/W
b6	PM	PM	Time alarm setting: 0: AM 1: PM.	R/W
b7	ENB	ENB	0:The register value is not compared with the RHRCNT counter value 1: The register value is compared with the RHRCNT counter value.	R/W

RHRAR is an alarm register associated with the BCD-coded hour counter RHRCNT. When the ENB bit is set to 1, the RHRAR value is compared with the RHRCNT value. From the following alarm registers, only those selected with the ENB bits set to 1 are compared with the associated counters:

- RSECAR
- RMINAR
- RHRAR
- RWKAR
- RDAYAR
- RMONAR
- RYRAREN.

When all the respective values match, the IR flag associated with the RTC_ALM interrupt is set to 1. The specifiable time differs according to the setting in the hours mode bit (RCR2.HR24):

- When the RCR2.HR24 bit is 0 — From 00 to 11 (in BCD)
- When the RCR2.HR24 bit is 1 — From 00 to 23 (in BCD).

If a value outside of this range is specified, the RTC does not operate correctly. When the RCR2.HR24 bit is 0, be sure to set the PM bit. When the RCR2.HR24 bit is 1, the setting in the PM bit has no effect. This register is cleared to 00h by an RTC software reset.

(2) 二进制计数模式

Address(es): RTC.BCNT1AR 4004 4012h

	b7	b6	b5	b4	b3	b2	b1	b0
	BCNTAR[15:8]							
重置后的值：	x	x	x	x	x	x	x	x

x: Undefined

BCNT1AR是一个读写报警寄存器，与从b15到b8的32位二进制计数器相关联。该寄存器通过RTC软件复位清零。

26.2.11 小时报警寄存器(RHRAR)二进制计数器2报警寄存器(BCNT2AR)

(1) 在日历计数模式下

Address(es): RTC.RHRAR 4004 4014h

	b7	b6	b5	b4	b3	b2	b1	b0
	ENB	PM	HR10[1:0]		HR1[3:0]			
重置后的值：	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b3 to b0	HR1[3:0]	1 Hour	几个小时的价值	R/W
b5, b4	HR10[1:0]	10 Hours	数十小时的价值	R/W
b6	PM	PM	时间报警设置：0 ：上午1：下午。	R/W
b7	ENB	ENB	0：寄存器值不与RHRCNT计数器值比较1：寄存器值与RHRCNT计数器值比较。	R/W

RHRAR是一个与BCD编码的小时计数器RHRCNT相关的警报寄存器。当ENB位设置为1时，RHRAR值与RHRCNT值进行比较。从下面的报警寄存器中，只有那些选择与
设置为1的ENB位与相关计数器进行比较：

- RSECAR
- RMINAR
- RHRAR
- RWKAR
- RDAYAR
- RMONAR
- RYRAREN.

当所有各自的值都匹配时，与RTC_ALM中断相关的IR标志设置为1。可指定的时间根据小时模式位(RCR2.HR24)中的设置而有所不同：

- 当RCR2.HR24位为0时—从00到11（以BCD表示）
- 当RCR2.HR24位为1时—从00到23（以BCD表示）。

如果指定的值超出此范围，则RTC将无法正确运行。当RCR2.HR24位为0时，请务必设置PM位。当RCR2.HR24位为1时，PM位中的设置无效。该寄存器通过RTC软件复位清零。

(2) In binary count mode

Address(es): RTC.BCNT2AR 4004 4014h

	b7	b6	b5	b4	b3	b2	b1	b0
	BCNTAR[23:16]							
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

BCNT2AR is a read/write alarm register associated with the 32-bit binary counter b23 to b16. This register is cleared to 00h by an RTC software reset.

26.2.12 Day-of-Week Alarm Register (RWKAR)/Binary Counter 3 Alarm Register (BCNT3AR)

(1) In calendar count mode

Address(es): RTC.RWKAR 4004 4016h

	b7	b6	b5	b4	b3	b2	b1	b0
	ENB	—	—	—	—	DAYW[2:0]		
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b2 to b0	DAYW[2:0]	Day-of-Week Setting	b2 b0 0 0 0: Sunday 0 0 1: Monday 0 1 0: Tuesday 0 1 1: Wednesday 1 0 0: Thursday 1 0 1: Friday 1 1 0: Saturday 1 1 1: Setting prohibited.	R/W
b6 to b3	—	Reserved	Set these bits to 0. They are read as the set value.	R/W
b7	ENB	ENB	0: The register value is not compared with the RWKCNT counter value 1: The register value is compared with the RWKCNT counter value.	R/W

RWKAR is an alarm register associated with the coded day-of-week counter RWKCNT. When the ENB bit is set to 1, the RWKAR value is compared with the RWKCNT value. From the following alarm registers, only those selected with the ENB bits set to 1 are compared with the associated counters:

- RSECAR
- RMINAR
- RHRAR
- RWKAR
- RDAYAR
- RMONAR
- RYRAREN.

When all the respective values all match, the IR flag associated with the RTC_ALM interrupt is set to 1. RWKAR values from 0 through 6 (in BCD) can be specified. If a value outside of this range is specified, the RTC does not operate correctly. This register is cleared to 00h by an RTC software reset.

(2) 二进制计数模式

Address(es): RTC.BCNT2AR 4004 4014h

	b7	b6	b5	b4	b3	b2	b1	b0
	BCNTAR[23:16]							
重置后的值：	x	x	x	x	x	x	x	x

x: Undefined

BCNT2AR是与32位二进制计数器b23至b16相关的读写警报寄存器。该寄存器通过RTC软件复位清零。

26.2.12 星期报警寄存器(RWKAR)二进制计数器3报警寄存器(BCNT3AR)

(1) 在日历计数模式下

Address(es): RTC.RWKAR 4004 4016h

	b7	b6	b5	b4	b3	b2	b1	b0
	ENB	—	—	—	—	DAYW[2:0]		
重置后的值：	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b2 to b0	DAYW[2:0]	Day-of-Week Setting	b2b0000：星期日001： 星期一010：星期二011： 星期三100：星期四101： 星期五110：星期六111： 禁止设置。	R/W
b6 to b3	—	Reserved	将这些位设置为0。它们作为设置值读取。	R/W
b7	ENB	ENB	0：寄存器值不与RWKCNT计数器值比较1：寄存器值与RWKCNT计数器值比较。	R/W

RWKAR是与编码的星期计数器RWKCNT相关的警报寄存器。当ENB位设置为1时，RWKAR值与RWKCNT值进行比较。从以下报警寄存器中，只有选择ENB位设置为1的报警寄存器与相关计数器进行比较：

- RSECAR
- RMINAR
- RHRAR
- RWKAR
- RDAYAR
- RMONAR
- RYRAREN.

当所有各自的值都匹配时，与RTC_ALM中断相关的IR标志设置为1。可以指定从0到6（以BCD表示）的RWKAR值。如果指定的值超出此范围，则RTC将无法正确运行。该寄存器通过RTC软件复位清零。

(2) In binary count mode

Address(es): RTC.BCNT3AR 4004 4016h

	b7	b6	b5	b4	b3	b2	b1	b0
	BCNTAR[31:24]							
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

BCNT3AR is a read/write alarm register associated with the 32-bit binary counter b31 to b24. This register is cleared to 00h by an RTC software reset.

26.2.13 Date Alarm Register (RDAYAR)/Binary Counter 0 Alarm Enable Register (BCNT0AER)

(1) In calendar count mode

Address(es): RTC.RDAYAR 4004 4018h

	b7	b6	b5	b4	b3	b2	b1	b0
	ENB	—	DATE10[1:0]		DATE1[3:0]			
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b3 to b0	DATE1[3:0]	1 Day	Value for the ones place of days	R/W
b5, b4	DATE10[1:0]	10 Days	Value for the tens place of days	R/W
b6	—	Reserved	Set this bit to 0. It is read as the set value.	R/W
b7	ENB	ENB	0: The register value is not compared with the RDAYCNT counter value 1: The register value is compared with the RDAYCNT counter value.	R/W

RDAYAR is an alarm register associated with the BCD-coded date counter RDAYCNT. When the ENB bit is set to 1, the RDAYAR value is compared with the RDAYCNT value. From the following alarm registers, only those selected with the ENB bits set to 1 are compared with the associated counters:

- RSECAR
- RMINAR
- RHRAR
- RWKAR
- RDAYAR
- RMONAR
- RYRAREN.

When all the respective values match, the IR flag associated with the RTC_ALM interrupt is set to 1. RDAYAR values from 01 through 31 (in BCD) can be specified. If a value outside of this range is specified, the RTC does not operate correctly. This register is cleared to 00h by an RTC software reset.

(2) 二进制计数模式

Address(es): RTC.BCNT3AR 4004 4016h

	b7	b6	b5	b4	b3	b2	b1	b0
	BCNTAR[31:24]							
重置后的值：	x	x	x	x	x	x	x	x

x: Undefined

BCNT3AR是与32位二进制计数器b31至b24相关的读写警报寄存器。该寄存器通过RTC软件复位清零。

26.2.13 日期报警寄存器(RDAYAR)二进制计数器0报警使能寄存器(BCNT0AER)

(1) 在日历计数模式下

Address(es): RTC.RDAYAR 4004 4018h

	b7	b6	b5	b4	b3	b2	b1	b0
	ENB	—	DATE10[1:0]		DATE1[3:0]			
重置后的值：	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b3 to b0	DATE1[3:0]	1 Day	几天的地方的价值	R/W
b5, b4	DATE10[1:0]	10 Days	十位天的价值	R/W
b6	—	Reserved	将此位设置为0。它作为设置值读取。	R/W
b7	ENB	ENB	0：寄存器值不与RDAYCNT计数器值比较1：寄存器值与RDAYCNT计数器值比较。	R/W

RDAYAR是一个与BCD编码日期计数器RDAYCNT相关的报警寄存器。当ENB位设置为1时，将RDAYAR值与RDAYCNT值进行比较。从下面的报警寄存器中，只有那些选择与
设置为1的ENB位与相关计数器进行比较：

- RSECAR
- RMINAR
- RHRAR
- RWKAR
- RDAYAR
- RMONAR
- RYRAREN.

当所有各自的值都匹配时，与RTC_ALM中断相关的IR标志设置为1。可以指定从01到31（以BCD表示）的RDAYAR值。如果指定的值超出此范围，则RTC将无法正确运行。该寄存器通过RTC软件复位清零。

(2) In binary count mode

Address(es): RTC.BCNT0AER 4004 4018h

	b7	b6	b5	b4	b3	b2	b1	b0
	ENB[7:0]							
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

BCNT0AER is a read/write register for setting the alarm enable associated with the 32-bit binary counter b7 to b0. The binary counter (BCNT[31:0]) associated with the ENB[31:0] bits that are set to 1 is compared with the binary alarm register (BCNTAR[31:0]) and, when all match, the IR flag associated with the RTC_ALM interrupt becomes 1. This register is cleared to 00h by an RTC software reset.

26.2.14 Month Alarm Register (RMONAR)/Binary Counter 1 Alarm Enable Register (BCNT1AER)

(1) In calendar count mode

Address(es): RTC.RMONAR 4004 401Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	ENB	—	—	MON10	MON1[3:0]			
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b3 to b0	MON1[3:0]	1 Month	Value for the ones place of months	R/W
b4	MON10	10 Months	Value for the tens place of months	R/W
b6, b5	—	Reserved	Set these bits to 0. They are read as the set value.	R/W
b7	ENB	ENB	0: The register value is not compared with the RMONCNT counter value 1: The register value is compared with the RMONCNT counter value.	R/W

RMONAR is an alarm register associated with the BCD-coded month counter RMONCNT. When the ENB bit is set to 1, the RMONAR value is compared with the RMONCNT value. From the following alarm registers, only those selected with the ENB bits set to 1 are compared with the associated counters:

- RSECAR
- RMINAR
- RHRAR
- RWKAR
- RDAYAR
- RMONAR
- RYRAREN.

When all the respective values match, the IR flag associated with the RTC_ALM interrupt is set to 1. RMONAR values from 01 through 12 (in BCD) can be specified. If a value outside of this range is specified, the RTC does not operate correctly. This register is cleared to 00h by an RTC software reset.

(2) 二进制计数模式

Address(es): RTC.BCNT0AER 4004 4018h

	b7	b6	b5	b4	b3	b2	b1	b0
	ENB[7:0]							
重置后的值：	x	x	x	x	x	x	x	x

x: Undefined

BCNT0AER是一个读写寄存器，用于将与32位二进制计数器b7关联的警报使能设置为b0。与设置为1的ENB[31:0]位相关的二进制计数器(BCNT[31:0])与二进制报警寄存器(BCNTAR[31:0])进行比较，当全部匹配时，IR标志与RTC_ALM中断相关联的值变为1。该寄存器通过RTC软件复位清零为00h。

26.2.14 月份闹钟寄存器(RMONAR)二进制计数器1闹钟启用寄存器(BCNT1AER)

(1) 在日历计数模式下

Address(es): RTC.RMONAR 4004 401Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	ENB	—	—	MON10	MON1[3:0]			
重置后的值：	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b3 to b0	MON1[3:0]	1 Month	月份个位数的值	R/W
b4	MON10	10 Months	十位月份的值	R/W
b6, b5	—	Reserved	将这些位设置为0。它们作为设置值读取。	R/W
b7	ENB	ENB	0：寄存器值不与RMONCNT计数器值比较1：寄存器值与RMONCNT计数器值比较。	R/W

RMONAR是一个与BCD编码月份计数器RMONCNT相关的报警寄存器。当ENB位设置为1时，RMONAR值与RMONCNT值进行比较。从以下报警寄存器中，只有选择ENB位设置为1的报警寄存器与相关计数器进行比较：

- RSECAR
- RMINAR
- RHRAR
- RWKAR
- RDAYAR
- RMONAR
- RYRAREN.

当所有各自的值都匹配时，与RTC_ALM中断相关的IR标志设置为1。可以指定从01到12（以BCD表示）的RMONAR值。如果指定的值超出此范围，则RTC将无法正确运行。该寄存器通过RTC软件复位清零。

(2) In binary count mode

Address(es): RTC.BCNT1AER 4004 401Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	ENB[15:8]							
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

BCNT1AER is a read/write register for setting the alarm enable associated with the 32-bit binary counter b15 to b8. The binary counter (BCNT[31:0]) associated with the ENB[31:0] bits that are set to 1 is compared with the binary alarm register (BCNTAR[31:0]) and, when all match, the IR flag associated with the RTC_ALM interrupt is set to 1. This register is cleared to 00h by an RTC software reset.

26.2.15 Year Alarm Register (RYRAR)/Binary Counter 2 Alarm Enable Register (BCNT2AER)

(1) In calendar count mode

Address(es): RTC.RYRAR 4004 401Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	YR10[3:0]				YR1[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b3 to b0	YR1[3:0]	1 Year	Value for the ones place of years	R/W
b7 to b4	YR10[3:0]	10 Years	Value for the tens place of years	R/W
b15 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

RYRAR is an alarm register associated with the BCD-coded year counter RYRCNT. RYRAR values from 00 through 99 (in BCD) can be specified. If a value outside of this range is specified, the RTC does not operate correctly. This register is cleared to 0000h by an RTC software reset.

(2) In binary count mode

Address(es): RTC.BCNT2AER 4004 401Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	ENB[23:16]							
Value after reset:	0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x

x: Undefined

BCNT2AER is a read/write register for setting the alarm enable associated with the 32-bit binary counter b23 to b16. The binary counter (BCNT[31:0]) associated with the ENB[31:0] bits that are set to 1 is compared with the binary alarm register (BCNTAR[31:0]) and, when all match, the IR flag associated with the RTC_ALM interrupt is set to 1. This register is cleared to 0000h by an RTC software reset.

(2) 二进制计数模式

Address(es): RTC.BCNT1AER 4004 401Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	ENB[15:8]							
重置后的值：	x	x	x	x	x	x	x	x

x: Undefined

BCNT1AER是一个读写寄存器，用于设置与32位二进制计数器b15到b8相关的警报使能。与设置为1的ENB[31:0]位相关的二进制计数器(BCNT[31:0])与二进制报警寄存器(BCNTAR[31:0])进行比较，当全部匹配时，IR标志与RTC_ALM中断相关的设置为1。该寄存器通过RTC软件复位清零为00h。

26.2.15 年报警寄存器(RYRAR)二进制计数器2报警使能寄存器(BCNT2AER)

(1) 在日历计数模式下

Address(es): RTC.RYRAR 4004 401Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	YR10[3:0]				YR1[3:0]			
重置后的值：	0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b3 to b0	YR1[3:0]	1 Year	年个地方的价值	R/W
b7 to b4	YR10[3:0]	10 Years	数十年的价值	R/W
b15 to b8	—	Reserved	这些位被读取为0。写入值应为0。	R/W

RYRAR是一个与BCD编码年份计数器RYRCNT相关联的警报寄存器。可以指定从00到99（BCD格式）的RYRAR值。如果指定的值超出此范围，则RTC将无法正确运行。该寄存器通过RTC软件复位清零为0000h。

(2) 二进制计数模式

Address(es): RTC.BCNT2AER 4004 401Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	ENB[23:16]							
重置后的值：	0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x

x: Undefined

BCNT2AER是一个读写寄存器，用于设置与32位二进制计数器b23到b16相关的警报使能。与设置为1的ENB[31:0]位相关的二进制计数器(BCNT[31:0])与二进制报警寄存器(BCNTAR[31:0])进行比较，当全部匹配时，IR标志与RTC_ALM中断相关的设置为1。该寄存器通过RTC软件复位清零为0000h。

26.2.16 Year Alarm Enable Register (RYRAREN)/Binary Counter 3 Alarm Enable Register (BCNT3AER)

(1) In calendar count mode

Address(es): RTC.RYRAREN 4004 401Eh

	b7	b6	b5	b4	b3	b2	b1	b0
	ENB	—	—	—	—	—	—	—
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b6 to b0	—	Reserved	Set these bits to 0. They are read as the set value.	R/W
b7	ENB	ENB	0: The register value is not compared with the RYRCNT counter value 1: The register value is compared with the RYRCNT counter value.	R/W

When the ENB bit in RYRAREN is set to 1, the RYRAR value is compared with the RYRCNT value. From the following alarm registers, only those selected with the ENB bits set to 1 are compared with the associated counters:

- RSECAR
- RMINAR
- RHRAR
- RWKAR
- RDAYAR
- RMONAR
- RYRAREN.

When all the respective values match, the IR flag associated with the RTC_ALM interrupt is set to 1. This register is cleared to 00h by an RTC software reset.

(2) In binary count mode

Address(es): RTC.BCNT3AER 4004 401Eh

	b7	b6	b5	b4	b3	b2	b1	b0
	ENB[31:24]							
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

BCNT3AER is a read/write register for setting the alarm enable associated with the 32-bit binary counter b31 to b24. The binary counter (BCNT[31:0]) associated with the ENB[31:0] bits that are set to 1 is compared with the binary alarm register (BCNTAR[31:0]) and, when all match, the IR flag associated with the RTC_ALM interrupt is set to 1. This register is cleared to 00h by an RTC software reset.

26.2.16 年报警使能寄存器(RYRAREN)二进制计数器3报警使能 Register (BCNT3AER)

(1) 在日历计数模式下

Address(es): RTC.RYRAREN 4004 401Eh

	b7	b6	b5	b4	b3	b2	b1	b0
	ENB	—	—	—	—	—	—	—
重置后的值：	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b6 to b0	—	Reserved	将这些位设置为0。它们作为设置值读取。	R/W
b7	ENB	ENB	0：寄存器值不与RYRCNT计数器值比较1：寄存器值与RYRCNT计数器值比较。	R/W

当RYRAREN中的ENB位设置为1时，RYRAR值与RYRCNT值进行比较。从以下报警寄存器中，只有选择ENB位设置为1的报警寄存器与相关计数器进行比较：

- RSECAR
- RMINAR
- RHRAR
- RWKAR
- RDAYAR
- RMONAR
- RYRAREN.

当所有各自的值都匹配时，与RTC_ALM中断相关的IR标志设置为1。该寄存器通过RTC软件复位清零为00h。

(2) 二进制计数模式

Address(es): RTC.BCNT3AER 4004 401Eh

	b7	b6	b5	b4	b3	b2	b1	b0
	ENB[31:24]							
重置后的值：	x	x	x	x	x	x	x	x

x: Undefined

BCNT3AER是一个读写寄存器，用于设置与32位二进制计数器b31至b24相关的警报使能。与设置为1的ENB[31:0]位相关的二进制计数器(BCNT[31:0])与二进制报警寄存器(BCNTAR[31:0])进行比较，当全部匹配时，IR标志与RTC_ALM中断相关的设置为1。该寄存器通过RTC软件复位清零为00h。

26.2.17 RTC Control Register 1 (RCR1)

Address(es): RTC.RCR1 4004 4022h

	b7	b6	b5	b4	b3	b2	b1	b0
	PES[3:0]				RTCOS	PIE	CIE	AIE
Value after reset:	x	x	x	x	0	x	0	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b0	AIE	Alarm Interrupt Enable	0: An alarm interrupt request is disabled 1: An alarm interrupt request is enabled.	R/W
b1	CIE	Carry Interrupt Enable	0: A carry interrupt request is disabled 1: A carry interrupt request is enabled.	R/W
b2	PIE	Periodic Interrupt Enable	0: A periodic interrupt request is disabled 1: A periodic interrupt request is enabled.	R/W
b3	RTCOS	RTCOUT Output Select	0: RTCOUT outputs 1 Hz 1: RTCOUT outputs 64 Hz.	R/W
b7 to b4	PES[3:0]	Periodic Interrupt Select	b7 b4 0 1 1 0: Generate periodic interrupt every 1/256 second*1 0 1 1 1: Generate periodic interrupt every 1/128 second 1 0 0 0: Generate periodic interrupt every 1/64 second 1 0 0 1: Generate periodic interrupt every 1/32 second 1 0 1 0: Generate periodic interrupt every 1/16 second 1 0 1 1: Generate periodic interrupt every 1/8 second 1 1 0 0: Generate periodic interrupt every 1/4 second 1 1 0 1: Generate periodic interrupt every 1/2 second 1 1 1 0: Generate periodic interrupt every 1 second 1 1 1 1: Generate periodic interrupt every 2 seconds. Other settings: No periodic interrupts are generated.	R/W

Note 1. When LOCO is selected (RCR4.RCKSEL = 1) while PES[3:0] = 0110b, a periodic interrupt is generated every 1/128 second.

The RCR1 register is used in both calendar count mode and in binary count mode. Bits AIE, PIE, and PES[3:0] are updated synchronously with the count source. When the RCR1 register is modified, check that all the bits are updated before proceeding.

AIE bit (Alarm Interrupt Enable)

The AIE bit enables or disables alarm interrupt requests.

If the times indicated in the counters and alarm settings match in Deep Software Standby mode, the MCU returns from the mode regardless of the AIE bit value.

CIE bit (Carry Interrupt Enable)

The CIE bit enables or disables interrupt requests when a carry to the RSECCNT/BCNT0 register occurs, or when a carry to the 64-Hz counter (R64CNT) occurs while reading the 64-Hz counter.

PIE bit (Periodic Interrupt Enable)

The PIE bit enables or disabled a periodic interrupt.

If the periods indicated in the counters and PES[3:0] settings match in Deep Software Standby mode, the MCU returns from the mode regardless of the PIE bit value.

RTCOS bit (RTCOUT Output Select)

The RTCOS bit selects the RTCOUT output period. The RTCOS bit must be rewritten while the count operation is stopped (the RCR2.START bit is 0) and the RTCOUT output is disabled (the RCR2.RTCOE bit is 0). When RTCOUT is output to an external pin, the RCR2.RTCOE bit must be enabled. For details on controlling the I/O ports, see section 20.5.1, Procedure for Specifying the Pin Functions.

26.2.17 RTC控制寄存器1(RCR1)

Address(es): RTC.RCR1 4004 4022h

	b7	b6	b5	b4	b3	b2	b1	b0
	PES[3:0]				RTCOS	PIE	CIE	AIE
重置后的值：	x	x	x	x	0	x	0	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b0	AIE	报警中断使能	0：禁止报警中断请求1：允许报警中断请求。	R/W
b1	CIE	进位中断使能	0：禁止进位中断请求1：使能进位中断请求。	R/W
b2	PIE	周期性中断使能	0：禁用周期性中断请求1：启用周期性中断请求。	R/W
b3	RTCOS	RTCOUT输出选择	0: RTCOUT outputs 1 Hz 1: RTCOUT outputs 64 Hz.	R/W
b7 to b4	PES[3:0]	周期性中断选择	b7b40110：每1256秒产生周期性中断*10111：每1128秒产生周期性中断1000：每164秒产生周期性中断1001：每1产生周期性中断32秒1010：每1秒产生周期中断16秒1011：每18秒产生周期中断1100：每14秒产生周期中断1101：每12秒产生周期中断1110：每1秒产生周期性中断1111：每2秒产生周期性中断。其他设置：不产生周期性中断。	R/W

Note 1. WhenLOCOisselected(RCR4.RCKSEL=1)whilePES[3:0]=0110b aperiodicinterruptisgeneratedevery1128second.

RCR1寄存器用于日历计数模式和二进制计数模式。AIE、PIE和PES[3:0]位与计数源同步更新。修改RCR1寄存器时，在继续之前检查所有位是否都已更新。

AIE位（报警中断使能）

AIE位启用或禁用警报中断请求。

如果计数器和警报设置中指示的时间在深度软件待机模式下匹配，则无论AIE位值如何，MCU都会从该模式返回。

CIE位（进位中断使能）

当发生对RSECCNTBCNT0寄存器的进位，或在读取64-Hz计数器时发生对64-Hz计数器(R64CNT)的进位时，CIE位启用或禁用中断请求。

PIE位（周期性中断使能）

PIE位启用或禁用周期性中断。

如果计数器中指示的周期和PES[3:0]设置在深度软件待机模式下匹配，则无论PIE位值如何，MCU都会从该模式返回。

RTCOS位（RTCOUT输出选择）

RTCOS位选择RTCOUT输出周期。当计数操作停止（RCR2.START位为0）且RTCOUT输出禁用（RCR2.RTCOE位为0）时，必须重写RTCOS位。当RTCOUT输出到外部引脚时，必须使能RCR2.RTCOE位。有关控制IO端口的详细信息，请参见第20.5.1节，指定引脚功能的过程。

PES[3:0] bits (Periodic Interrupt Select)

The PES[3:0] bits specify the period for the periodic interrupt. A periodic interrupt is generated with the period specified in these bits.

26.2.18 RTC Control Register 2 (RCR2)

(1) In calendar count mode

Address(es): RTC.RCR2 4004 4024h

	b7	b6	b5	b4	b3	b2	b1	b0
	CNTMD	HR24	AADJP	AADJE	RTCOE	ADJ30	RESET	START
Value after reset:	x	x	x	x	0	0	0	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b0	START	Start	0: Prescaler and time counter are stopped 1: Prescaler and time counter operate normally.	R/W
b1	RESET	RTC Software Reset	• In writing 0: Invalid (writing 0 has no effect) 1: The prescaler and the target registers for RTC software reset *1 are initialized. • In reading 0: Normal time operation in progress, or RTC software reset has completed 1: RTC software reset in progress.	R/W
b2	ADJ30	30-Second Adjustment	• In writing 0: Invalid (writing 0 has no effect) 1: 30-second adjustment is executed. • In reading 0: Normal time operation in progress, or 30-second adjustment has completed 1: 30-second adjustment in progress.	R/W
b3	RTCOE	RTCOUT Output Enable	0: RTCOUT output is disabled 1: RTCOUT output is enabled.	R/W
b4	AADJE	Automatic Adjustment Enable*2	0: Automatic adjustment is disabled 1: Automatic adjustment is enabled.	R/W
b5	AADJP	Automatic Adjustment Period Select*2	0: The RADJ.ADJ[5:0] setting value is adjusted from the count value of the prescaler every minute 1: The RADJ.ADJ[5:0] setting value is adjusted from the count value of the prescaler every 10 seconds.	R/W
b6	HR24	Hours Mode	0: RTC operates in 12-hour mode 1: RTC operates in 24-hour mode.	R/W
b7	CNTMD	Count Mode Select	0: Calendar count mode 1: Binary count mode.	R/W

Note 1. R64CNT, RSECAR/BCNT0AR, RMINAR/BCNT1AR, RHRAR/BCNT2AR, RWKAR/BCNT3AR, RDAYAR/BCNT0AER, RMONAR/BCNT1AER, RYRAR/BCNT2AER, RYRAREN/BCNT3AER, RADJ, RTCCRy, RSECCPy/BCNT0CPy, RMINCPy/BCNT1CPy, RHRCPy/BCNT2CPy, RDAYCPy/BCNT3CPy, RMONCPy, RCR2.ADJ30, RCR2.AADJE, RCR2.AADJP.
Note 2. When LOCO is selected, the setting of this bit is disabled.

The RCR2 register is related to hours mode, automatic adjustment function, enabling RTCOUT output, 30-second adjustment, RTC software reset, and controlling count operation.

START bit (Start)

The START bit stops or restarts the prescaler or time counter operation. This bit is updated in synchronization with the next cycle of the count source. When the START bit is modified, check that the bit is updated before proceeding.

PES[3:0]位（周期性中断选择）

PES[3:0]位指定周期性中断的周期。以这些位中指定的周期生成周期性中断。

26.2.18 RTC控制寄存器2(RCR2)

(1) 在日历计数模式下

Address(es): RTC.RCR2 4004 4024h

	b7	b6	b5	b4	b3	b2	b1	b0
	CNTMD	HR24	AADJP	ADJ	RTCOE	ADJ30	复位	开始
重置后的值：	x	x	x	x	0	0	0	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b0	START	Start	0：预分频器和时间计数器停止1：预分频器和时间计数器正常运行。	R/W
b1	RESET	RTC软件复位	写入0：无效（写入0无效）1：预分频器和RTC软件复位的目标寄存器*1被初始化。 读取中0：正常时间操作正在进行，或RTC软件复位已完成1：RTC软件复位正在进行。	R/W
b2	ADJ30	30-Second Adjustment	Inwriting0：无效（写入0无效）1：执行30秒调整。 读数中0：正在进行正常时间操作，或30秒调整已完成1：正在进行30秒调整。	R/W
b3	RTCOE	RTCOUT输出使能	0：禁用RTCOUT输出1：启用RTCOUT输出。	R/W
b4	AADJE	自动调整启用*2	0：禁用自动调整1：启用自动调整。	R/W
b5	AADJP	自动调整期Select*2	0：RADJ.ADJ[5:0]设置值每分钟根据预分频器的计数值调整1：RADJ.ADJ[5:0]设置值每10秒根据预分频器的计数值调整一次。	R/W
b6	HR24	小时模式	0：RTC以12小时模式运行1：RTC以24小时模式运行。	R/W
b7	CNTMD	计数模式选择	0：日历计数模式1：二进制计数模式。	R/W

Note 1. R64CNT, RSECAR/BCNT0AR, RMINAR/BCNT1AR, RHRAR/BCNT2AR, RWKAR/BCNT3AR, RDAYAR/BCNT0AER, RMONAR/BCNT1AER, RYRAR/BCNT2AER, RYRAREN/BCNT3AER, RADJ, RTCCRy, RSECCPy/BCNT0CPy, RMINCPy/BCNT1CPy, RHRCPy/BCNT2CPy, RDAYCPy/BCNT3CPy, RMONCPy, RCR2.ADJ30, RCR2.AADJE, RCR2.AADJP.
Note 2. 选择Loco时，该位的设置将被禁用。

RCR2寄存器与小时模式、自动调整功能、启用RTCOUT输出、30秒调整、RTC软件复位和控制计数操作有关。

开始位（开始）

START位停止或重新启动预分频器或时间计数器操作。该位与计数源的下一个周期同步更新。修改START位后，请在继续之前检查该位是否已更新。

RESET bit (RTC Software Reset)

The RESET bit initializes the prescaler and registers to be reset by RTC software.

When 1 is written to the RESET bit, initialization starts in synchronization with the count source. When the initialization is complete, the RESET bit is automatically set to 0. Check that this bit is 0 before proceeding.

ADJ30 bit (30-Second Adjustment)

The ADJ30 bit is for 30-second adjustment.

When 1 is written to the ADJ30 bit, the RSECCNT value of 30 seconds or less is rounded down to 00 second and the value of 30 seconds or more is rounded up to 1 minute.

The 30-second adjustment is performed in synchronization with the count source. When 1 is written to this bit, the ADJ30 bit is automatically set to 0 after the 30-second adjustment is complete. If 1 is written to the ADJ30 bit, check that the bit is 0 before proceeding. When the 30-second adjustment is performed, the prescaler and R64CNT are also reset. The ADJ30 bit is cleared to 0 by an RTC software reset.

RTCOE bit (RTCOUT Output Enable)

The RTCOE bit enables output of a 1-Hz/64-Hz clock signal from the RTCOUT pin.

Use the START bit to stop counting before changing the value of the RTCOE bit. Do not stop counting (write 0 to the START bit) and change the value of the RTCOE bit at the same time.

When RTCOUT is to be output from an external pin, enable the RTCOE bit and set up the port control for the pin.

AADJE bit (Automatic Adjustment Enable*2)

The AADJE bit controls (enables or disables) automatic adjustment.

Set the plus-minus bits (RADJ.PMADJ[1:0]) to 00b (adjustment is not performed) before changing the value of the AADJE bit.

The AADJE bit is cleared to 0 by an RTC software reset.

AADJP bit (Automatic Adjustment Period Select*2)

The AADJP bit selects the automatic-adjustment period.

Set the plus-minus bits (RADJ.PMADJ[1:0]) to 00b (adjustment is not performed) before changing the value of the AADJP bit.

The AADJP bit is cleared to 0 by an RTC software reset.

HR24 bit (Hours Mode)

The HR24 bit specifies whether the RTC operates in 12- or 24-hour mode.

Use the START bit to stop counting before changing the value of the HR24 bit. Do not stop counting (write 0 to the START bit) and change the value of the HR24 bit at the same time.

CNTMD bit (Count Mode Select)

The CNTMD bit specifies whether the RTC count mode operates in calendar count mode or in binary count mode.

When setting the count mode, execute an RTC software reset and start again from the initial settings. This bit is updated synchronously with the count source, and its value is fixed before the RTC software reset is complete.

For details on initial settings, see section 26.3.1, Outline of Initial Settings of Registers after Power On.

RESET位（RTC软件复位）

RESET位初始化预分频器和寄存器以由RTC软件复位。

向RESET位写入1时，初始化与计数源同步开始。初始化完成后，RESET位自动设置为0。在继续之前检查该位是否为0。

ADJ30位（30秒调整）

ADJ30位用于30秒调整。

向ADJ30位写入1时，30秒以下的RSECCNT值向下舍入为00秒，30秒以上的值向上舍入为1分钟。

30秒调整与计数源同步进行。当1写入该位时，
30秒调整完成后，ADJ30位自动设置为0。如果将1写入ADJ30位，请在继续之前检查该位是否为0。当执行30秒调整时，预分频器和R64CNT也被复位。RTC软件复位将ADJ30位清零。

RTCOE位（RTCOUT输出使能）

RTCOE位使能从RTCOUT引脚输出1-Hz64-Hz时钟信号。

在更改RTCOE位的值之前，使用START位停止计数。不要停止计数（将0写入START位）并同时更改RTCOE位的值。

当RTCOUT要从外部引脚输出时，使能RTCOE位并设置引脚的端口控制。

ADJE位（自动调整使能*2）

AADJE位控制（启用或禁用）自动调整。

在更改
AADJE bit.

通过RTC软件复位将ADJE位清零。

AADJP位（自动调整周期选择*2）

AADJP位选择自动调整周期。

在更改
AADJP bit.

AADJP位通过RTC软件复位清零。

HR24位（小时模式）

HR24位指定RTC是在12小时还是24小时模式下运行。

在更改HR24位的值之前，使用START位停止计数。不要停止计数（将0写入START位）并同时更改HR24位的值。

CNTMD位（计数模式选择）

CNTMD位指定RTC计数模式是在日历计数模式还是二进制计数模式下运行。

设置计数模式时，执行RTC软件复位并从初始设置重新开始。该位与计数源同步更新，其值在RTC软件复位完成前固定。

有关初始设置的详细信息，请参阅第26.3.1节“通电后寄存器初始设置概述”。

(2) In binary count mode

Address(es): RTC.RCR2 4004 4024h

	b7	b6	b5	b4	b3	b2	b1	b0
	CNTMD	—	AADJP	AADJE	RTCOE	—	RESET	START
Value after reset:	x	x	x	x	0	0	0	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b0	START	Start	0: The 32-bit binary counter, 64-Hz counter, and prescaler are stopped 1: The 32-bit binary counter, 64-Hz counter, and prescaler are in normal operation.	R/W
b1	RESET	RTC Software Reset	• In writing 0: Invalid (writing 0 has no effect) 1: The prescaler and the target registers for RTC software reset*1 are initialized. • In reading 0: Normal time operation in progress, or RTC software reset has completed 1: RTC software reset in progress.	R/W
b2	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b3	RTCOE	RTCOUT Output Enable	0: RTCOUT output is disabled 1: RTCOUT output is enabled.	R/W
b4	AADJE	Automatic Adjustment Enable*2	0: Automatic adjustment is disabled 1: Automatic adjustment is enabled.	R/W
b5	AADJP	Automatic Adjustment Period Select*2	0: Add or subtract RADJ.ADJ [5:0] bits from prescaler count value every 32 seconds 1: Add or subtract RADJ.ADJ [5:0] bits from prescaler count value every 8 seconds.	R/W
b6	—	Reserved	This bit is undefined. The write value should be 0.	R/W
b7	CNTMD	Count Mode Select	0: Calendar count mode 1: Binary count mode.	R/W

Note 1. R64CNT, RSECAR/BCNT0AR, RMINAR/BCNT1AR, RHRAR/BCNT2AR, RWKAR/BCNT3AR, RDAYAR/BCNT0AER, RMONAR/BCNT1AER, RYRAR/BCNT2AER, RYRAREN/BCNT3AER, RADJ, RTCCRy, RSECCPy/BCNT0CPy, RMINCPy/BCNT1CPy, RHRCPy/BCNT2CPy, RDAYCPy/BCNT3CPy, RMONCPy, RCR2.ADJ30, RCR2.AADJE, RCR2.AADJP.
Note 2. When LOCO is selected, the setting of this bit is disabled.

START bit (Start)

The START bit stops or restarts the prescaler or counter (clock) operation. The bit is updated in synchronization with the count source. When the START bit is modified, check that the bit is updated before proceeding.

RESET bit (RTC Software Reset)

The RESET bit initializes the prescaler and registers to be reset by RTC software.

When 1 is written to this bit, initialization starts in synchronization with the count source. When the initialization is complete, the RESET bit is automatically set to 0. When 1 is written to the RESET bit, check that the bit is 0 before proceeding.

RTCOE bit (RTCOUT Output Enable)

The RTCOE bit enables output of a 1-Hz/64-Hz clock signal from the RTCOUT pin.

Use the START bit to stop counting before changing the value of the RTCOE bit. Do not stop counting (write 0 to the START bit) and change the value of the RTCOE bit at the same time. When an RTCOUT signal is to be output from an external pin, enable the port control in addition to setting this bit.

(2) 二进制计数模式

Address(es): RTC.RCR2 4004 4024h

	b7	b6	b5	b4	b3	b2	b1	b0
	CNTMD	—	AADJP	AADJE	RTCOE	—	复位开始	
重置后的值：	x	x	x	x	0	0	0	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b0	START	Start	0：32位二进制计数器、64-Hz计数器和预分频器停止1：32位二进制计数器、64-Hz计数器和预分频器正常运行。	R/W
b1	RESET	RTC软件复位	写入0：无效（写入0无效）1：预分频器和RTC软件复位的目标寄存器*1被初始化。 读取中0：正常时间操作正在进行，或RTC软件复位已完成1：RTC软件复位正在进行。	R/W
b2	—	Reserved	该位读取为0。写入值应为0。	R/W
b3	RTCOE	RTCOUT输出使能	0：禁用RTCOUT输出1：启用RTCOUT输出。	R/W
b4	AADJE	自动调整启用 *2	0：禁用自动调整1：启用自动调整	R/W
b5	AADJP	自动调整期 Select*2	0：每32秒从预分频器计数值加或减RADJ.ADJ[5:0]位1：每8秒从预分频器计数值加或减RADJ.ADJ[5:0]位。	R/W
b6	—	Reserved	该位未定义。写入值应为0。	R/W
b7	CNTMD	计数模式选择	0：日历计数模式1：二进制计数模式。	R/W

Note 1. R64CNT, RSECAR/BCNT0AR, RMINAR/BCNT1AR, RHRAR/BCNT2AR, RWKAR/BCNT3AR, RDAYAR/BCNT0AER, RMONAR/BCNT1AER, RYRAR/BCNT2AER, RYRAREN/BCNT3AER, RADJ, RTCCRy, RSECCPy/BCNT0CPy, RMINCPy/BCNT1CPy, RHRCPy/BCNT2CPy, RDAYCPy/BCNT3CPy, RMONCPy, RCR2.ADJ30, RCR2.AADJE, RCR2.AADJP.
Note 2. 选择Loco时，该位的设置将被禁用。

开始位（开始）

START位停止或重新启动预分频器或计数器（时钟）操作。该位与计数源同步更新。修改START位后，请在继续之前检查该位是否已更新。

RESET位（RTC软件复位）

RESET位初始化预分频器和寄存器以由RTC软件复位。

当向该位写入1时，初始化与计数源同步开始。初始化完成后，RESET位自动设置为0。当向RESET位写入1时，在继续之前检查该位是否为0。

RTCOE位（RTCOUT输出使能）

RTCOE位使能从RTCOUT引脚输出1-Hz64-Hz时钟信号。

在更改RTCOE位的值之前，使用START位停止计数。不要停止计数（将0写入START位）并同时更改RTCOE位的值。当要从外部引脚输出RTCOUT信号时，除了设置该位外，还启用端口控制。

AADJE bit (Automatic Adjustment Enable)

The AADJE bit controls (enables or disables) automatic adjustment.

Set the plus-minus bits (RADJ.PMADJ[1:0]) to 00b (adjustment is not performed) before changing the value of the AADJE bit. The AADJE bit is cleared to 0 by an RTC software reset.

AADJP bit (Automatic Adjustment Period Select)

The AADJP bit selects the automatic-adjustment period.

Correction period can be selected from 32 second units or 8 second units in binary count mode.

Set the plus-minus bits (RADJ.PMADJ[1:0]) to 00b (adjustment is not performed) before changing the value of the AADJP bit. The AADJP bit is cleared to 0 by an RTC software reset.

CNTMD bit (Count Mode Select)

The CNTMD bit specifies whether the RTC count mode operates in calendar count mode or in binary count mode.

When setting the count mode, execute an RTC software reset and start again from the initial settings. This bit is updated synchronously with the count source, and its value is fixed before the RTC software reset is complete.

For details on initial settings, see section 26.3.1, Outline of Initial Settings of Registers after Power On.

26.2.19 RTC Control Register 4 (RCR4)

Address(es): RTC.RCR4 4004 4028h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	RCKSEL
Value after reset:	0	0	0	0	0	0	0	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b0	RCKSEL	Count Source Select	0: Sub-clock oscillator is selected 1: LOCO is selected.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The RCR4 register selects the count source and is used in both calendar count mode and binary count mode.

When the RCKSEL bit is set to 0, the time is counted with the sub-clock oscillator. When the bit is set to 1, the time is counted with LOCO.

RCKSEL bit (Count Source Select)

The RCKSEL bit selects the count source from the sub-clock oscillator and LOCO.

The count source must be selected only once before specifying the initial settings of the RTC registers at power on.

ADJE位（自动调整使能）

AADJE位控制（启用或禁用）自动调整。

在更改
ADJE位。通过RTC软件复位将ADJE位清零。

AADJP位（自动调整周期选择）

AADJP位选择自动调整周期。

在二进制计数模式下，校正周期可以从32秒单位或8秒单位中选择。

在更改
AADJP位。AADJP位通过RTC软件复位清零。

CNTMD位（计数模式选择）

CNTMD位指定RTC计数模式是在日历计数模式还是二进制计数模式下运行。

设置计数模式时，执行RTC软件复位并从初始设置重新开始。该位与计数源同步更新，其值在RTC软件复位完成前固定。

有关初始设置的详细信息，请参阅第26.3.1节“通电后寄存器初始设置概述”。

26.2.19 RTC控制寄存器4(RCR4)

Address(es): RTC.RCR4 4004 4028h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	RCKSEL
重置后的值：	0	0	0	0	0	0	0	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b0	RCKSEL	计数源选择	0：选择副时钟振荡器1：选择LOCO。	R/W
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

RCR4寄存器选择计数源，用于日历计数模式和二进制计数模式。

当RCKSEL位设置为0时，时间由副时钟振荡器计数。当该位设置为1时，时间以LOCO计数。

RCKSEL位（计数源选择）

RCKSEL位从副时钟振荡器和LOCO中选择计数源。

在上电时指定RTC寄存器的初始设置之前，必须只选择一次计数源。

26.2.20 Frequency Register (RFRH/RFRL)

Address(es): RTC.RFRH.4004 402Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RFC16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b0	RFC16	Reserved	Write 0 before writing to the RFRL register after a cold start	R/W
b15 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Address(es): RTC.RFRL.4004 402Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RFC[15:0]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b15 to b0	RFC[15:0]	Frequency Comparison Value	Write 00FFh to this register when using the LOCO	R/W

RFRL is a register for controlling the prescaler when LOCO is selected.

The RTC time counter operates on a 128-Hz clock signal as the base clock. Therefore, when LOCO is selected, LOCO is divided by the prescaler to generate a 128-Hz clock signal. Set the frequency comparison value in the RFC[15:0] bits to generate a 128-Hz clock from the LOCO frequency. Before writing to RFC[15:0] after a cold start, write 0000h to the RFRH register.

A value from 0007h through 01FFh can be specified as the frequency comparison value. If a value outside of this range is specified, the RTC does not operate correctly. Before writing to this register, be sure to stop the count operation through the setting of the START bit in RCR2. The operating frequency of the peripheral module clock and the LOCO should be such that the peripheral module clock is ≥ to the LOCO.

Calculation method of frequency comparison value:

RFC[15:0] = (LOCO clock frequency) / 128 - 1

When the LOCO frequency is 32.768 kHz, the RFRL register should be set to 00FFh.

26.2.20 频率寄存器(RFRHRFRL)

Address(es): RTC.RFRH.4004 402Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RFC16
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b0	RFC16	Reserved	冷启动后写入RFRL寄存器前写入0	R/W
b15 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Address(es): RTC.RFRL.4004 402Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RFC[15:0]															
重置后的值:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b15 to b0	RFC[15:0]	频率比较 Value	使用LOCO时将00FFh写入该寄存器	R/W

RFRL是一个寄存器，用于在选择LOCO时控制预分频器。

RTC时间计数器以128-Hz时钟信号作为基本时钟运行。Therefore whenLOCOisselected LOCOisdividedbytheprescalertogeneratea128-Hzclocksignal设置RFC[15:0]位中的频率比较值以从LOCO频率生成128-Hz时钟。在冷启动后写入RFC[15:0]之前，将0000h写入RFRH寄存器。

可以将0007h到01FFh的值指定为频率比较值。如果指定的值超出此范围，则RTC将无法正确运行。在写入该寄存器之前，请务必通过设置RCR2中的START位来停止计数操作。外围模块时钟和LOCO的工作频率应使外围模块时钟与LOCO相差 。

频率比较值的计算方法：

RFC[15:0] = (LOCO clock frequency) / 128 - 1

当LOCO频率为32.768kHz时，RFRL寄存器应设置为00FFh。

26.2.21 Time Error Adjustment Register (RADJ)

Address(es): RTC.RADJ 4004 402Eh

	b7	b6	b5	b4	b3	b2	b1	b0
	PMADJ[1:0]		ADJ[5:0]					
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b5 to b0	ADJ[5:0]	Adjustment Value	These bits specify the adjustment value from the prescaler	R/W
b7, b6	PMADJ[1:0]	Plus-Minus	b7 b6 0 0: Adjustment is performed 0 1: Adjustment is performed by the addition to the prescaler 1 0: Adjustment is performed by the subtraction from the prescaler 1 1: Setting prohibited.	R/W

Adjustment is performed by the addition to or subtraction from the prescaler. If the automatic adjustment enable (RCR2.AADJE) bit is 0, adjustment is performed when writing to the RADJ. If the RCR2.AADJE bit is 1, adjustment is performed in the interval specified in the automatic adjustment period select (RCR2.AADJP) bit.

The current adjustment by software (disabling automatic adjustment) might be invalid if the following adjustment value is specified within 320 cycles of the count source after the register setting. To perform adjustment consecutively, wait for 320 cycles or more of the count source after the register setting, then specify the next adjustment value.

RADJ is updated in synchronization with the count source. When RADJ is modified, check that all the bits are updated before continuing with more processing. This register is cleared to 00h by an RTC software reset. The setting of this register is enabled only when the sub-clock oscillator is selected. When LOCO is selected, adjustment is not performed.

ADJ[5:0] bits (Adjustment Value)

The ADJ[5:0] bits specify the adjustment value (number of sub-clock cycles) from the prescaler.

PMADJ[1:0] bits (Plus-Minus)

The PMADJ[1:0] bits select whether the clock is set ahead or back depending on the error-adjustment value set in the ADJ[5:0] bits.

26.2.22 Time Capture Control Register y (RTCCRy) (y = 0 to 2)

Address(es): RTC.RTCCR0 4004 4040h, RTC.RTCCR1 4004 4042h, RTC.RTCCR2 4004 4044h

	b7	b6	b5	b4	b3	b2	b1	b0
	TCEN	—	TCNF[1:0]		—	TCST	TCCT[1:0]	
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b1, b0	TCCT[1:0]	Time Capture Control	b1 b0 0 0: No event is detected 0 1: Rising edge is detected 1 0: Falling edge is detected 1 1: Both edges are detected.	R/W
b2	TCST	Time Capture Status	0: No event is detected 1: An event is detected.*1	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

26.2.21 时间误差调整寄存器(RADJ)

Address(es): RTC.RADJ 4004 402Eh

	b7	b6	b5	b4	b3	b2	b1	b0
	PMADJ[1:0]		ADJ[5:0]					
重置后的值：	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b5 to b0	ADJ[5:0]	调整值	这些位指定来自预分频器的调整值	R/W
b7, b6	PMADJ[1:0]	Plus-Minus	b7b600：进行调整01：通过预分频器1的加法进行调整0：通过预分频器1的减法进行调整1：禁止设置。	R/W

通过对预分频器进行加法或减法进行调整。如果自动调整使能(RCR2.AADJE)位为0，则在写入RADJ时执行调整。如果RCR2.AADJE位为1，则在自动调整周期选择(RCR2.AADJP)位指定的间隔内执行调整。

如果在寄存器设置后的计数源的320个周期内指定了以下调整值，则通过软件进行的当前调整（禁用自动调整）可能无效。要连续执行调整，请在寄存器设置后等待计数源的320个或更多周期，然后指定下一个调整值。

RADJ与计数源同步更新。修改RADJ后，在继续进行更多处理之前检查所有位是否已更新。该寄存器通过RTC软件复位清零。该寄存器的设置仅在选择了副时钟振荡器时启用。选择LOCO时，不进行调整。

ADJ[5:0]位（调整值）

ADJ[5:0]位指定来自预分频器的调整值（子时钟周期数）。

PMADJ[1:0] bits (Plus-Minus)

PMADJ[1:0]位根据在
ADJ[5:0] bits.

26.2.22 时间捕捉控制寄存器y(RTCCRy)(y=0to2)

Address(es): RTC.RTCCR0 4004 4040h, RTC.RTCCR1 4004 4042h, RTC.RTCCR2 4004 4044h

	b7	b6	b5	b4	b3	b2	b1	b0
	TCEN	—	TCNF[1:0]		—	TCST	TCCT[1:0]	
重置后的值：	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b1, b0	TCCT[1:0]	时间捕捉控制	b1b000：未检测到事件01：检测到上升沿10：检测到下降沿 11：检测到两个沿。	R/W
b2	TCST	时间捕捉状态	0：未检测到事件1：检测到事件。*1	R/W
b3	—	Reserved	该位读取为0。写入值应为0。	R/W

Bit	Symbol	Bit name	Description	R/W
b5, b4	TCNF[1:0]	Time Capture Noise Filter Control	b5 b4 0 0: Turn noise filter off 0 1: Setting prohibited 1 0: Turn noise filter on (count source) 1 1: Turn noise filter on (count source by divided by 32).	R/W
b6	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b7	TCEN	Time Capture Event Input Pin Enable	0: The RTCICn pin is disabled as the time capture event input 1: The RTCICn pin is enabled as the time capture event input (n = 0 to 2).	R/W

Note 1. Indicates that an event is detected. Writing 1 to this bit has no effect. Writing 0 sets this bit to 0.

The RTCCRy register is used both in calendar count mode and in binary count mode. RTCCR0, RTCCR1, and RTCCR2 control the RTCIC0, RTCIC1, and RTCIC2 pins, respectively.

RTCCRy is updated in synchronization with the count source. When RTCCRy is modified, check that all the bits except the TCST bit are updated before continuing with more processing. This register is cleared to 00h by an RTC software reset. When RTCICn is used as the time capture pin, VBTICTLR.VCHnIEN (n = 0 to 2) must be set to 1. For more information, see section 12, Battery Backup Function.

TCCT[1:0] bits (Time Capture Control)

The TCCT[1:0] bits control the edge detection of the time capture event input pins, RTCIC0, RTCIC1, and RTCIC2. The detection edge is selectable. The TCCT[1:0] bits must be set while the VBTICTLR.VCHnIEN bit is 1.

TCST bit (Time Capture Status)

The TCST bit indicates that an event on the time capture event input pins, RTCIC0, RTCIC1, and RTCIC2, was detected. When the TCST bit is 0, no event is detected. When the TCST bit is 1, this bit indicates that an event was detected on the associated pin and the capture register is valid. When multiple events are detected, the capture time for the first event is retained.

If an event is detected while the count operation is stopped (the RCR2.START bit is 0), the captured value is not guaranteed. In this case, set the TCST bit to 0 to delete the captured value. Writing 0 sets the TCST bit to 0. Writing any value other than 0 has no effect.

Set the TCST bit while the TCCT[1:0] bits are 00b (no event is detected). The TCST bit is set to 0 in synchronization with the count source. When the TCST bit is set to 0, check that the bit is updated before continuing with additional processing.

TCNF[1:0] bits (Time Capture Noise Filter Control)

The TCNF[1:0] bits control the noise filter of the time capture event input pins (RTCIC0, RTCIC1, and RTCIC2).

When the noise filter is on, the count source divided by 1 or divided by 32 is selectable. In this case, when the input level on the time capture event input pin matches three consecutive times at the set sampling period, the input level is determined.

Set the TCNF[1:0] bits while the TCCT[1:0] bits are 00b (no event is detected). When the noise filter is used, set the TCNF[1:0] bits, wait for 3 cycles of the specified sampling period, and then set the TCCT[1:0] bits. Set the TCNF[1:0] bits when the VBTICTLR.VCHnIEN bit is 1.

TCEN bit (Time Capture Event Input Pin Enable)

The TCEN bit enables or disables the time capture event input pins RTCIC0, RTCIC1, and RTCIC2. When the functions of the time capture event input pins are multiplexed, set VBTICTLR first. If the TCEN bit is set to 0, also set the TCCT[1:0] bits to 00b.

Bit	Symbol	位名称	Description	R/W
b5, b4	TCNF[1:0]	时间捕捉噪声过滤器控制	b5b400：关闭噪声滤波器01：设置禁止10：打开噪声滤波器（计数源）11：打开噪声滤波器（计数源除以32） 。	R/W
b6	—	Reserved	该位读取为0。写入值应为0。	R/W
b7	TCEN	时间捕捉事件输入引脚使能	0：禁止RTCICn引脚作为时间捕捉事件输入1：使能RTCICn引脚作为时间捕捉事件输入（n=0到2）。	R/W

Note 1. 表示检测到事件。向该位写入1无效。写入0将该位设置为0。

RTCCry寄存器用于日历计数模式和二进制计数模式。RTCCR0、RTCCR1和RTCCR2分别控制RTCIC0、RTCIC1和RTCIC2引脚。

RTCCRy与计数源同步更新。修改RTCCRy后，请检查除TCST位之外的所有位是否都已更新，然后再继续进行更多处理。该寄存器通过RTC软件复位清零。当RTCICn用作时间捕捉引脚时，VBTICTLR.VCHnIEN(n=0to2)必须设置为1。有关详细信息，请参阅第12节，电池备份功能。

TCCT[1:0]位（时间捕捉控制）

TCCT[1:0]位控制时间捕捉事件输入引脚RTCIC0、RTCIC1和RTCIC2的边沿检测。检测边缘是可选的。当VBTICTLR.VCHnIEN位为1时，必须设置TCCT[1:0]位。

TCST位（时间捕捉状态）

TCST位指示检测到时间捕捉事件输入引脚RTCIC0、RTCIC1和RTCIC2上的事件。当TCST位为0时，未检测到任何事件。当TCST位为1时，该位表示在相关引脚上检测到事件并且捕捉寄存器有效。当检测到多个事件时，将保留第一个事件的捕获时间。

如果在计数操作停止时检测到事件（RCR2.START位为0），则不能保证捕获的值。在这种情况下，将TCST位设置为0以删除捕获的值。写入0会将TCST位设置为0。写入0以外的任何值均无效。

当TCCT[1:0]位为00b（未检测到事件）时，设置TCST位。TCST位与计数源同步设置为0。当TCST位设置为0时，在继续进行其他处理之前检查该位是否已更新。

TCNF[1:0]位（时间捕捉噪声滤波器控制）

TCNF[1:0]位控制时间捕捉事件输入引脚（RTCIC0、RTCIC1和RTCIC2）的噪声滤波器。

当噪声滤波器打开时，计数源除以1或除以32是可选的。在这种情况下，当时间捕捉事件输入引脚上的输入电平在设置的采样周期内连续匹配3次时，确定输入电平。

当TCCT[1:0]位为00b（未检测到事件）时，设置TCNF[1:0]位。使用噪声滤波器时，设置TCNF[1:0]位，等待指定采样周期的3个周期，然后设置TCCT[1:0]位。当VBTICTLR.VCHnIEN位为1时，设置TCNF[1:0]位。

TCEN位（时间捕捉事件输入引脚使能）

TCEN位启用或禁用时间捕捉事件输入引脚RTCIC0、RTCIC1和RTCIC2。当时间捕捉事件输入引脚的功能复用时，首先设置VBTICTLR。如果TCEN位设置为0，也将TCCT[1:0]位设置为00b。

26.2.23 Second Capture Register y (RSECCPy) (y = 0 to 2)/BCNT0 Capture Register y (BCNT0CPy) (y = 0 to 2)

(1) In calendar count mode

Address(es): RTC.RSECCP0 4004 4052h, RTC.RSECCP1 4004 4062h, RTC.RSECCP2 4004 4072h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	SEC10[2:0]			SEC1[3:0]			
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b3 to b0	SEC1[3:0]	1-Second Capture	Capture value for the ones place of seconds	R
b6 to b4	SEC10[2:0]	10-Second Capture	Capture value for the tens place of seconds	R
b7	—	Reserved	This bit is read as 0 after an RTC software reset	R

RSECCPy is a read-only register that captures the RSECCNT value when a time capture event is detected.

The event detection times detected by the RTCIC0, RTCIC1, and RTCIC2 pins are stored in the RSECCP0, RSECCP1, and RSECCP2 registers, respectively. This register is cleared to 00h by an RTC software reset. Before reading from this register, be sure to stop the time capture event detection using the RTCCRy.TCCT[1:0] bits.

(2) In binary count mode

Address(es): RTC.BCNT0CP0 4004 4052h, RTC.BCNT0CP1 4004 4062h, RTC.BCNT0CP2 4004 4072h

	b7	b6	b5	b4	b3	b2	b1	b0
	BCNTCPy[7:0]							
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

BCNT0CPy is a read-only register that captures the BCNT0 value when a time capture event is detected. The event detection times detected by the RTCIC0, RTCIC1, and RTCIC2 pins are stored in the BCNT0CP0, BCNT0CP1, and BCNT0CP2 registers, respectively.

This register is cleared to 00h by an RTC software reset. Before reading from this register, be sure to stop the time capture event detection using the RTCCRy.TCCT[1:0] bits.

26.2.24 Minute Capture Register y (RMINCPy) (y = 0 to 2)/BCNT1 Capture Register y (BCNT1CPy) (y = 0 to 2)

(1) In calendar count mode

Address(es): RTC.RMINCP0 4004 4054h, RTC.RMINCP1 4004 4064h, RTC.RMINCP2 4004 4074h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	MIN10[2:0]			MIN1[3:0]			
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b3 to b0	MIN1[3:0]	1-Minute Capture	Capture value for the ones place of minutes	R

26.2.23 第二个捕捉寄存器y(RSECPy)(y=0到2)BCNT0捕捉寄存器y(BCNT0CPy)(y=0到2)

(1) 在日历计数模式下

Address(es): RTC.RSECCP0 4004 4052h, RTC.RSECCP1 4004 4062h, RTC.RSECCP2 4004 4072h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	SEC10[2:0]			SEC1[3:0]			
重置后的值:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b3 to b0	SEC1[3:0]	1-Second Capture	捕获秒个位的值	R
b6 to b4	SEC10[2:0]	10-Second Capture	十位秒的捕获值	R
b7	—	Reserved	在RTC软件复位后，该位被读取为0	R

RSECCpy是一个只读寄存器，当检测到时间捕捉事件时，它会捕捉RSECCNT值。

RTCIC0、RTIC1和RTCIC2引脚检测到的事件检测时间分别存储在RSCCP0、RSCCP1和RSCCP2寄存器中。该寄存器通过RTC软件复位清零。在读取该寄存器之前，请务必使用RTCCRy.TCCT[1:0]位停止时间捕捉事件检测。

(2) 二进制计数模式

Address(es): RTC.BCNT0CP0 4004 4052h, RTC.BCNT0CP1 4004 4062h, RTC.BCNT0CP2 4004 4072h

	b7	b6	b5	b4	b3	b2	b1	b0
	BCNTCPy[7:0]							
重置后的值:	x	x	x	x	x	x	x	x

x: Undefined

BCNT0CPy是一个只读寄存器，当检测到时间捕捉事件时，它会捕捉BCNT0的值。RTCIC0、RTCIC1和RTCIC2引脚检测到的事件检测时间分别存储在BCNT0CP0、BCNT0CP1和BCNT0CP2寄存器中。

该寄存器通过RTC软件复位清零。在读取该寄存器之前，请务必使用RTCCRy.TCCT[1:0]位停止时间捕捉事件检测。

26.2.24 分钟捕捉寄存器y(RMINCPy)(y=0到2)BCNT1捕捉寄存器y(BCNT1CPy)(y=0到2)

(1) 在日历计数模式下

Address(es): RTC.RMINCP0 4004 4054h, RTC.RMINCP1 4004 4064h, RTC.RMINCP2 4004 4074h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	MIN10[2:0]			MIN1[3:0]			
重置后的值:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b3 to b0	MIN1[3:0]	1-Minute Capture	捕获分钟个位的值	R

Bit	Symbol	Bit name	Description	R/W
b6 to b4	MIN10[2:0]	10-Minute Capture	Capture value for the tens place of minutes	R
b7	—	Reserved	This bit is read as 0 after an RTC software reset	R

RMINCPy is a read-only register that captures the RMINCNT value when a time capture event is detected.

The event detection times detected by the RTCIC0, RTCIC1, and RTCIC2 pins are stored in the RMINCP0, RMINCP1, and RMINCP2 registers, respectively.

This register is cleared to 00h by an RTC software reset. Before reading from this register, be sure to stop the time capture event detection using the RTCCRy.TCCT[1:0] bits.

(2) In binary count mode

Address(es): RTC.BCNT1CP0 4004 4054h, RTC.BCNT1CP1 4004 4064h, RTC.BCNT1CP2 4004 4074h

	b7	b6	b5	b4	b3	b2	b1	b0
	BCNTCPy[15:8]							
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

BCNT1CPy is a read-only register that captures the BCNT1 value when a time capture event is detected.

The event detection times detected by the RTCIC0, RTCIC1, and RTCIC2 pins are stored in the BCNT1CP0, BCNT1CP1, and BCNT1CP2 registers, respectively.

This register is cleared to 00h by an RTC software reset. Before reading from this register, you must stop the time capture event detection using the RTCCRy.TCCT[1:0] bits.

26.2.25 Hour Capture Register y (RHRCPy) (y = 0 to 2)/BCNT2 Capture Register y (BCNT2CPy) (y = 0 to 2)

(1) In calendar count mode

Address(es): RTC.RHRCP0 4004 4056h, RTC.RHRCP1 4004 4066h, RTC.RHRCP2 4004 4076h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	PM	HR10[1:0]		HR1[3:0]			
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b3 to b0	HR1[3:0]	1-Hour Capture	Capture value for the ones place of hours	R
b5, b4	HR10[1:0]	10-Hour Capture	Capture value for the tens place of hours	R
b6	PM	PM	0: AM 1: PM.	R
b7	—	Reserved	This bit is read as 0 after an RTC software reset.	R

RHRCPy is a read-only register that captures the RHRCNT value when a time capture event is detected.

The event detection times detected by the RTCIC0, RTCIC1, and RTCIC2 pins are stored in the RHRCP0, RHRCP1, and RHRCP2 registers, respectively. The PM bit is only enabled when the RCR2.HR24 bit is 0 (in 12-hour mode).

This register is cleared to 00h by an RTC software reset. Before reading from this register, be sure to stop the time capture event detection using the RTCCRy.TCCT[1:0] bits.

Bit	Symbol	位名称	Description	R/W
b6 to b4	MIN10[2:0]	10-Minute Capture	十位分钟的捕获值	R
b7	—	Reserved	在RTC软件复位后，该位被读取为0	R

RMINCPy是一个只读寄存器，它在检测到时间捕捉事件时捕捉RMINCNT值。

RTCIC0、RTCIC1和RTCIC2引脚检测到的事件检测时间分别存储在RMINCP0、RMINCP1和RMINCP2寄存器中。

该寄存器通过RTC软件复位清零。在读取该寄存器之前，请务必使用RTCCRy.TCCT[1:0]位停止时间捕捉事件检测。

(2) 二进制计数模式

Address(es): RTC.BCNT1CP0 4004 4054h, RTC.BCNT1CP1 4004 4064h, RTC.BCNT1CP2 4004 4074h

	b7	b6	b5	b4	b3	b2	b1	b0
	BCNTCPy[15:8]							
重置后的值：	x	x	x	x	x	x	x	x

x: Undefined

BCNT1CPy是一个只读寄存器，它在检测到时间捕捉事件时捕捉BCNT1值。

RTCIC0、RTCIC1和RTCIC2引脚检测到的事件检测时间存储在BCNT1CP0、分别是BCNT1CP1和BCNT1CP2寄存器。

该寄存器通过RTC软件复位清零。在读取该寄存器之前，您必须使用RTCCRy.TCCT[1:0]位停止时间捕捉事件检测。

26.2.25 小时捕捉寄存器y(RHRCPy)(y=0to2)BCNT2CaptureRegistery(BCNT2CPy)(y=0to2)

(1) 在日历计数模式下

Address(es): RTC.RHRCP0 4004 4056h, RTC.RHRCP1 4004 4066h, RTC.RHRCP2 4004 4076h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	PM	HR10[1:0]		HR1[3:0]			
重置后的值：	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b3 to b0	HR1[3:0]	1-Hour Capture	为几个小时的地方捕获价值	R
b5, b4	HR10[1:0]	10-Hour Capture	捕捉数十小时的价值	R
b6	PM	PM	0: AM 1: PM.	R
b7	—	Reserved	在RTC软件复位后，该位被读取为0。	R

RHRCPy是一个只读寄存器，它在检测到时间捕捉事件时捕捉RHRCNT值。

RTCIC0、RTCIC1和RTCIC2引脚检测到的事件检测时间存储在RHRCP0、RHRCP1和RHRCP2寄存器，分别。PM位仅在RCR2.HR24位为0时启用（在12小时模式下）。

该寄存器通过RTC软件复位清零。在读取该寄存器之前，请务必使用RTCCRy.TCCT[1:0]位停止时间捕捉事件检测。

(2) In binary count mode

Address(es): RTC.BCNT2CP0 4004 4056h, RTC.BCNT2CP1 4004 4066h, RTC.BCNT2CP2 4004 4076h

	b7	b6	b5	b4	b3	b2	b1	b0
	BCNTCPy[23:16]							
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

BCNT2CPy is a read-only register that captures the BCNT2 value when a time capture event is detected.

The event detection times detected by the RTCIC0, RTCIC1, and RTCIC2 pins are stored in the BCNT2CP0, BCNT2CP1, and BCNT2CP2 registers, respectively.

This register is cleared to 00h by an RTC software reset. Before reading from this register, be sure to stop the time capture event detection using the RTCCRy.TCCT[1:0] bits.

26.2.26 Date Capture Register y (RDAYCPy) (y = 0 to 2)/BCNT3 Capture Register y (BCNT3CPy) (y = 0 to 2)

(1) In calendar count mode:

Address(es): RTC.RDAYCP0 4004 405Ah, RTC.RDAYCP1 4004 406Ah, RTC.RDAYCP2 4004 407Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	DATE10[1:0]		DATE1[3:0]			
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b3 to b0	DATE1[3:0]	1-Day Capture	Capture value for the ones place of days	R
b5, b4	DATE10[1:0]	10-Day Capture	Capture value for the tens place of days	R
b7, b6	—	Reserved	These bits are read as 0 after an RTC software reset	R

RDAYCPy is a read-only register that captures the RDAYCNT value when a time capture event is detected.

The event detection times detected by the RTCIC0, RTCIC1, and RTCIC2 pins are stored in the RDAYCP0, RDAYCP1, and RDAYCP2 registers, respectively.

This register is cleared to 00h by an RTC software reset. Before reading from this register, be sure to stop the time capture event detection using the RTCCRy.TCCT[1:0] bits.

(2) In binary count mode

Address(es): RTC.BCNT3CP0 4004 405Ah, RTC.BCNT3CP1 4004 406Ah, RTC.BCNT3CP2 4004 407Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	BCNTCPy[31:24]							
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

BCNT3CPy is a read-only register that captures the BCNT3 value when a time capture event is detected.

The event detection times detected by the RTCTC0, RTCTC1, and RTCTC2 pins are stored in the BCNT3CP0, BCNT3CP1, and BCNT3CP2 registers, respectively.

This register is cleared to 00h by an RTC software reset. Before reading from this register, you must stop the time capture

(2) 二进制计数模式

Address(es): RTC.BCNT2CP0 4004 4056h, RTC.BCNT2CP1 4004 4066h, RTC.BCNT2CP2 4004 4076h

	b7	b6	b5	b4	b3	b2	b1	b0
	BCNTCPy[23:16]							
重置后的值：	x	x	x	x	x	x	x	x

x: Undefined

BCNT2CPy是一个只读寄存器，它在检测到时间捕捉事件时捕捉BCNT2值。

RTCIC0、RTCIC1和RTCIC2引脚检测到的事件检测时间存储在BCNT2CP0、分别是BCNT2CP1和BCNT2CP2寄存器。

该寄存器通过RTC软件复位清零。在读取该寄存器之前，请务必使用RTCCRy.TCCT[1:0]位停止时间捕捉事件检测。

26.2.26 数据捕捉寄存器y(RDAYCPy)(y=0to2)BCNT3CaptureRegistery(BCNT3CPy)(y=0to2)

(1) 在日历计数模式下：

Address(es): RTC.RDAYCP0 4004 405Ah, RTC.RDAYCP1 4004 406Ah, RTC.RDAYCP2 4004 407Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	DATE10[1:0]		DATE1[3:0]			
重置后的值：	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b3 to b0	DATE1[3:0]	1-Day Capture	捕获天数的价值	R
b5, b4	DATE10[1:0]	10-Day Capture	十天的捕获值	R
b7, b6	—	Reserved	这些位在RTC软件复位后被读取为0	R

RDAYCPy是一个只读寄存器，在检测到时间捕捉事件时捕捉RDAYCNT值。

RTCIC0、RTCIC1和RTCIC2引脚检测到的事件检测时间分别存储在RDAYCP0、RDAYCP1和RDAYCP2寄存器中。

该寄存器通过RTC软件复位清零。在读取该寄存器之前，请务必使用RTCCRy.TCCT[1:0]位停止时间捕捉事件检测。

(2) 二进制计数模式

Address(es): RTC.BCNT3CP0 4004 405Ah, RTC.BCNT3CP1 4004 406Ah, RTC.BCNT3CP2 4004 407Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	BCNTCPy[31:24]							
重置后的值：	x	x	x	x	x	x	x	x

x: Undefined

BCNT3CPy是一个只读寄存器，它在检测到时间捕捉事件时捕捉BCNT3值。

RTCTC0、RTCTC1和RTCTC2引脚检测到的事件检测时间存储在BCNT3CP0、分别是BCNT3CP1和BCNT3CP2寄存器。

该寄存器通过RTC软件复位清零。在读取该寄存器之前，您必须停止时间捕捉

event detection using the RTCCRy.TCCT[1:0] bits.

26.2.27 Month Capture Register y (RMONCPy) (y = 0 to 2)

(1) In calendar count mode:

Address(es): RTC.RMONCP0 4004 405Ch, RTC.RMONCP1 4004 406Ch, RTC.RMONCP2 4004 407Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	MON10	MON1[3:0]			
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b3 to b0	MON1[3:0]	1-Month Capture	Capture value for the ones place of months	R
b4	MON10	10-Month Capture	Capture value for the tens place of months	R
b7 to b5	—	Reserved	These bits are read as 0	R

RMONCPy is a read-only register that captures the RMONCNT value when a time capture event is detected.

The event detection times detected by the RTCIC0, RTCIC1, and RTCIC2 pins are stored in the RMONCP0, RMONCP1, and RMONCP2 registers, respectively.

This register is cleared to 00h by an RTC software reset. Before reading from this register, you must stop the time capture event detection using the RTCCRy.TCCT[1:0] bits.

26.3 Operation

26.3.1 Outline of Initial Settings of Registers after Power On

After the power is turned on, perform the initial settings for the clock setting, count mode setting, time error adjustment, time setting, alarm, interrupt, and time capture control register.

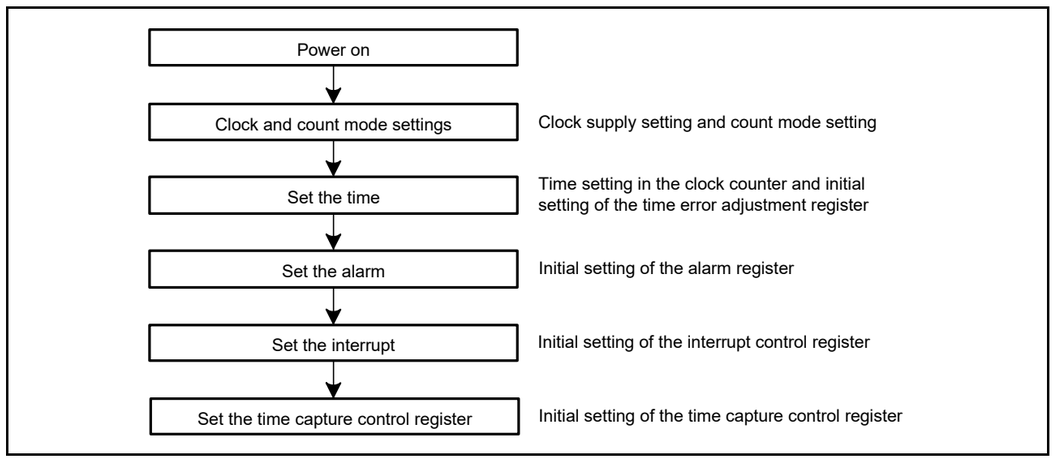


Figure 26.2 Outline of initial settings after a power on

使用RTCCRy.TCCT[1:0]位进行事件检测。

26.2.27 月份捕捉寄存器y(RMONCPy)(y=0to2)

(1) 在日历计数模式下：

Address(es): RTC.RMONCP0 4004 405Ch, RTC.RMONCP1 4004 406Ch, RTC.RMONCP2 4004 407Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	MON10	MON1[3:0]			
重置后的值：	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b3 to b0	MON1[3:0]	1-Month Capture	捕获月份的某个地方的价值	R
b4	MON10	10-Month Capture	捕获十个月的价值	R
b7 to b5	—	Reserved	这些位被读为0	R

RMONCPy是一个只读寄存器，它在检测到时间捕捉事件时捕捉RMONCNT值。

RTCIC0、RTCIC1和RTCIC2引脚检测到的事件检测时间存储在RMONCP0、分别是RMONCP1和RMONCP2寄存器。

该寄存器通过RTC软件复位清零。在读取该寄存器之前，您必须使用RTCCRy.TCCT[1:0]位停止时间捕捉事件检测。

26.3 Operation

26.3.1 上电后寄存器的初始设置概要

上电后，对时钟设置、计数模式设置、时间误差调整、时间设置、闹钟、中断、时间捕捉控制寄存器进行初始设置。

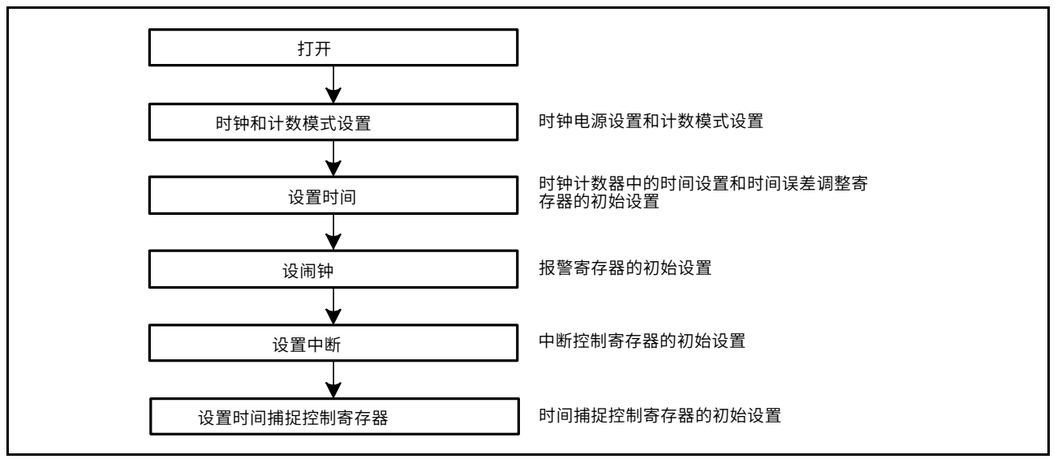
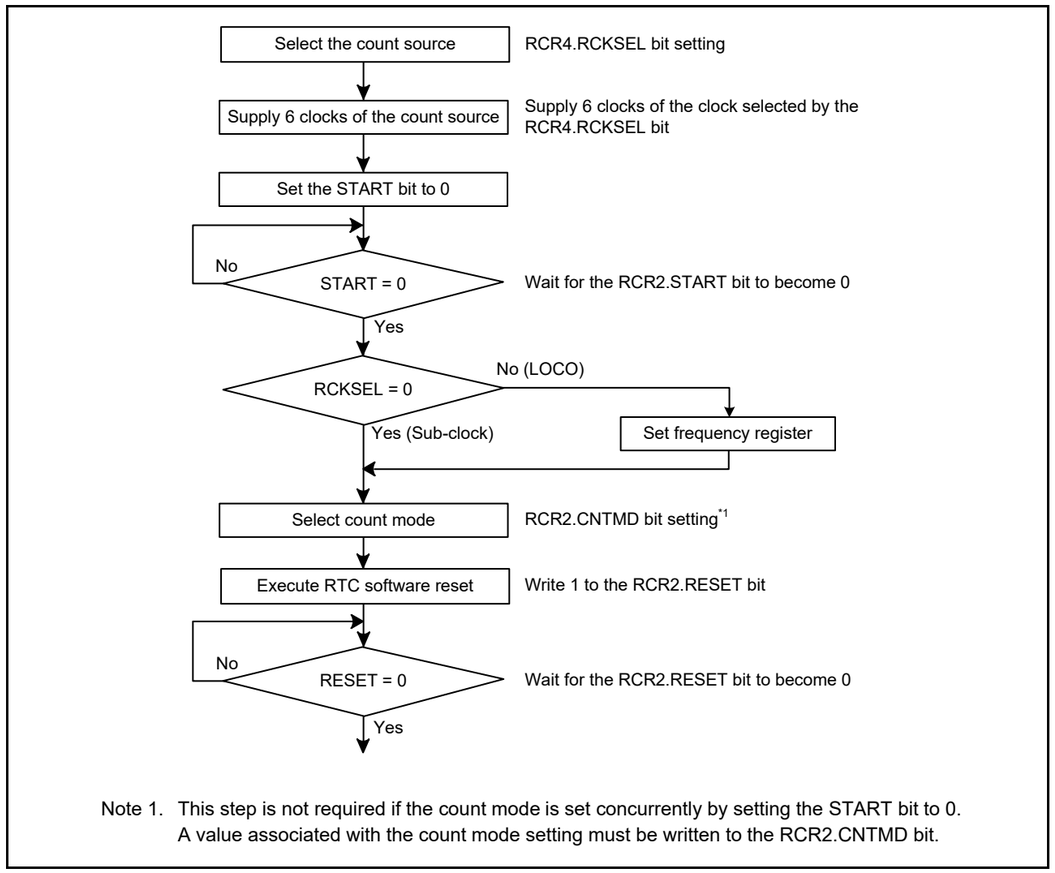


Figure 26.2 通电后的初始设定概要

26.3.2 Clock and Count Mode Setting Procedure

Figure 26.3 shows how to set the clock and the count mode.



Note 1. This step is not required if the count mode is set concurrently by setting the START bit to 0. A value associated with the count mode setting must be written to the RCR2.CNTMD bit.

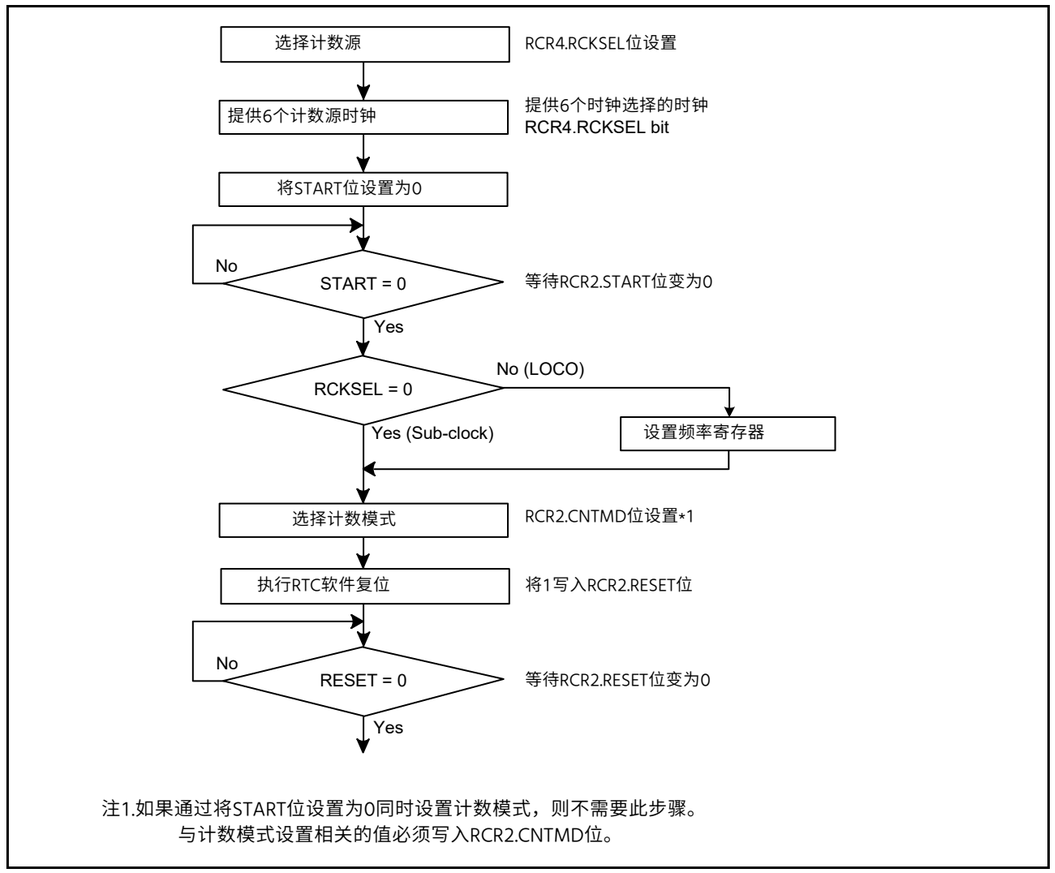
Figure 26.3 Clock and count mode setting procedure

26.3.3 Setting the Time

Figure 26.4 shows how to set the time.

26.3.2 时钟和计数模式设置程序

图26.3显示了如何设置时钟和计数模式。

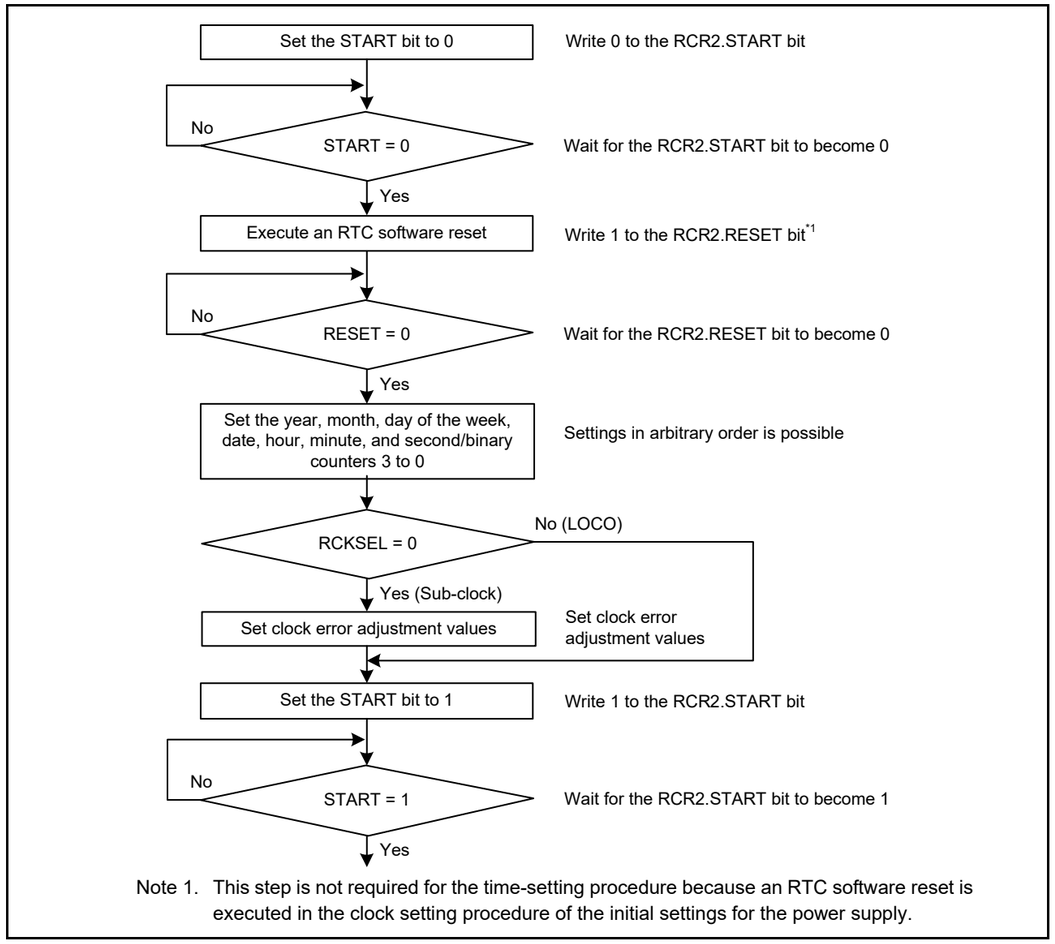


注1.如果通过将START位设置为0同时设置计数模式，则不需要此步骤。
与计数模式设置相关的值必须写入RCR2.CNTMD位。

Figure 26.3 时钟和计数模式设置程序

26.3.3 设置时间

图26.4显示了如何设置时间。



Note 1. This step is not required for the time-setting procedure because an RTC software reset is executed in the clock setting procedure of the initial settings for the power supply.

Figure 26.4 Setting the time

26.3.4 30-Second Adjustment

Figure 26.5 shows how to execute a 30-second adjustment.

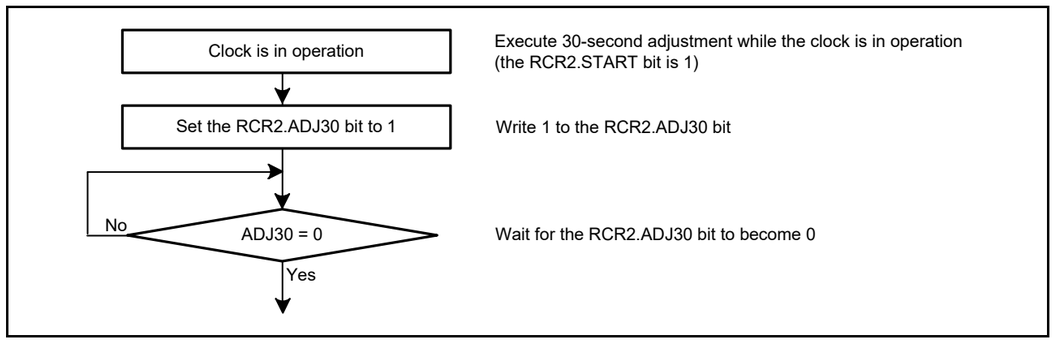
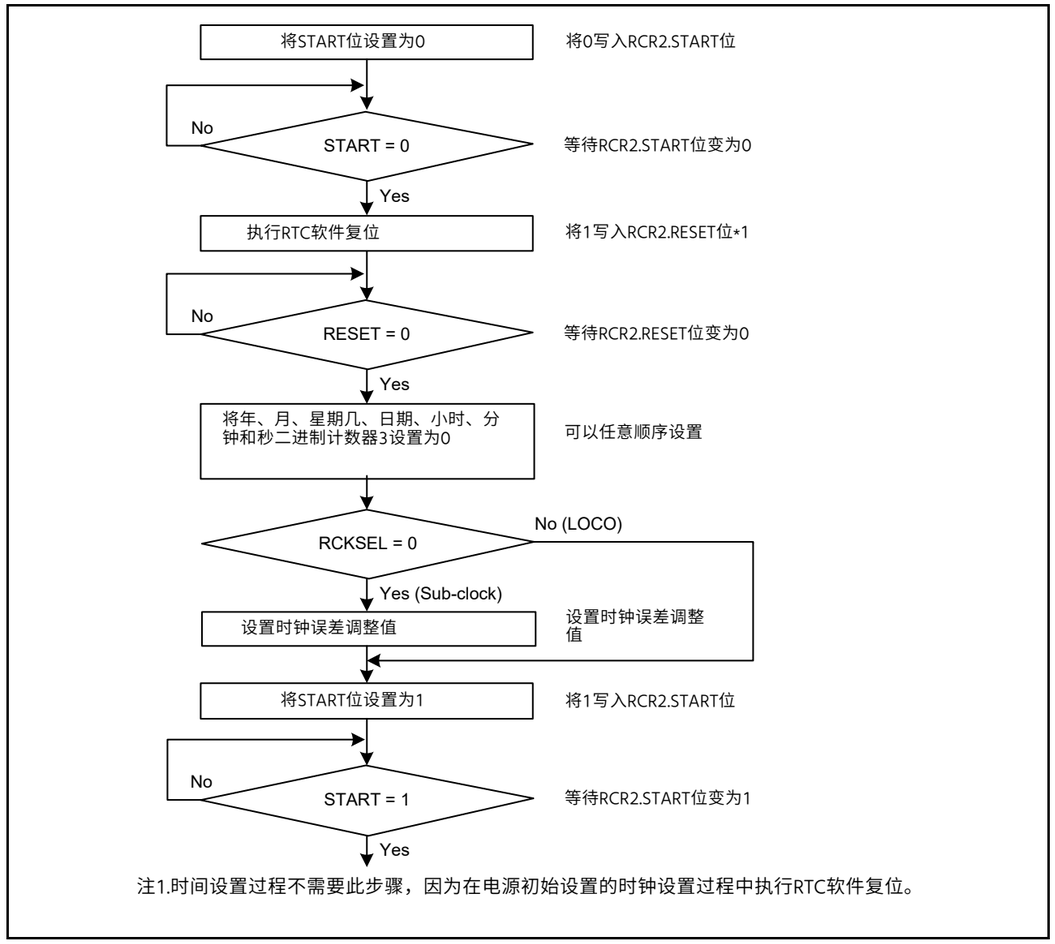


Figure 26.5 30-second adjustment



注1.时间设置过程不需要此步骤，因为在电源初始设置的时钟设置过程中执行RTC软件复位。

Figure 26.4 设定时间

26.3.4 30-Second Adjustment

图26.5显示了如何执行30秒的调整。

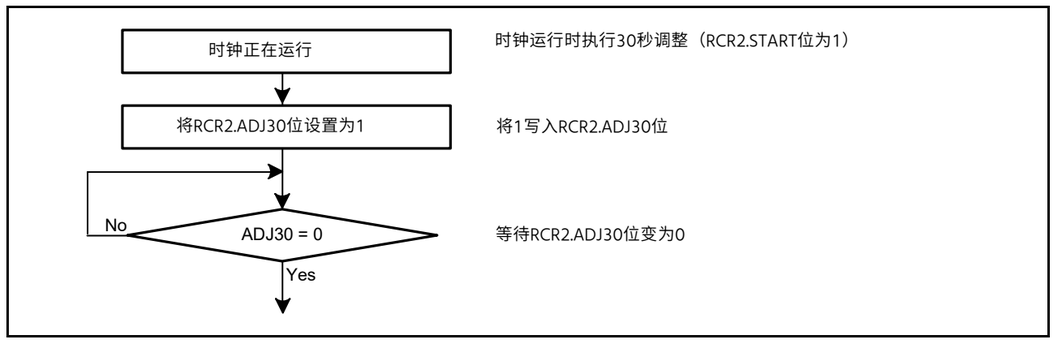


Figure 26.5 30-second adjustment

26.3.5 Reading 64-Hz Counter and Time

Figure 26.6 shows how to read a 64-Hz counter and time.

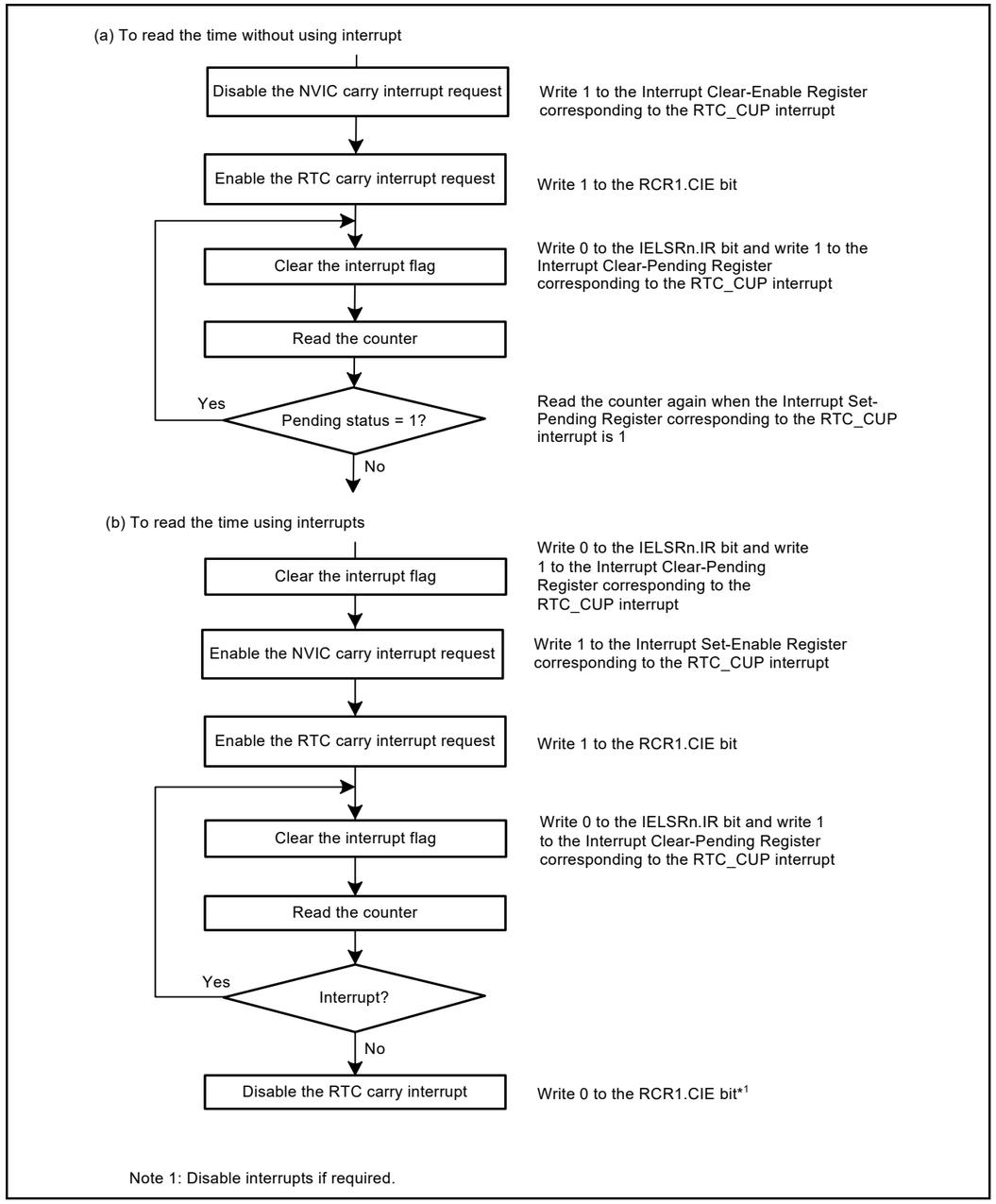


Figure 26.6 Reading time

If a carry occurs while the 64-Hz counter and time are being read, the correct time is not obtained, therefore they must be read again. The procedure for reading the time without using interrupts is shown in (a) in Figure 26.6, and the procedure using carry interrupts is shown in (b). To keep the program simple, Renesas recommends using method (a) in most cases.

26.3.5 读取64-Hz计数器和时间

图26.6显示了如何读取64-Hz计数器和时间。

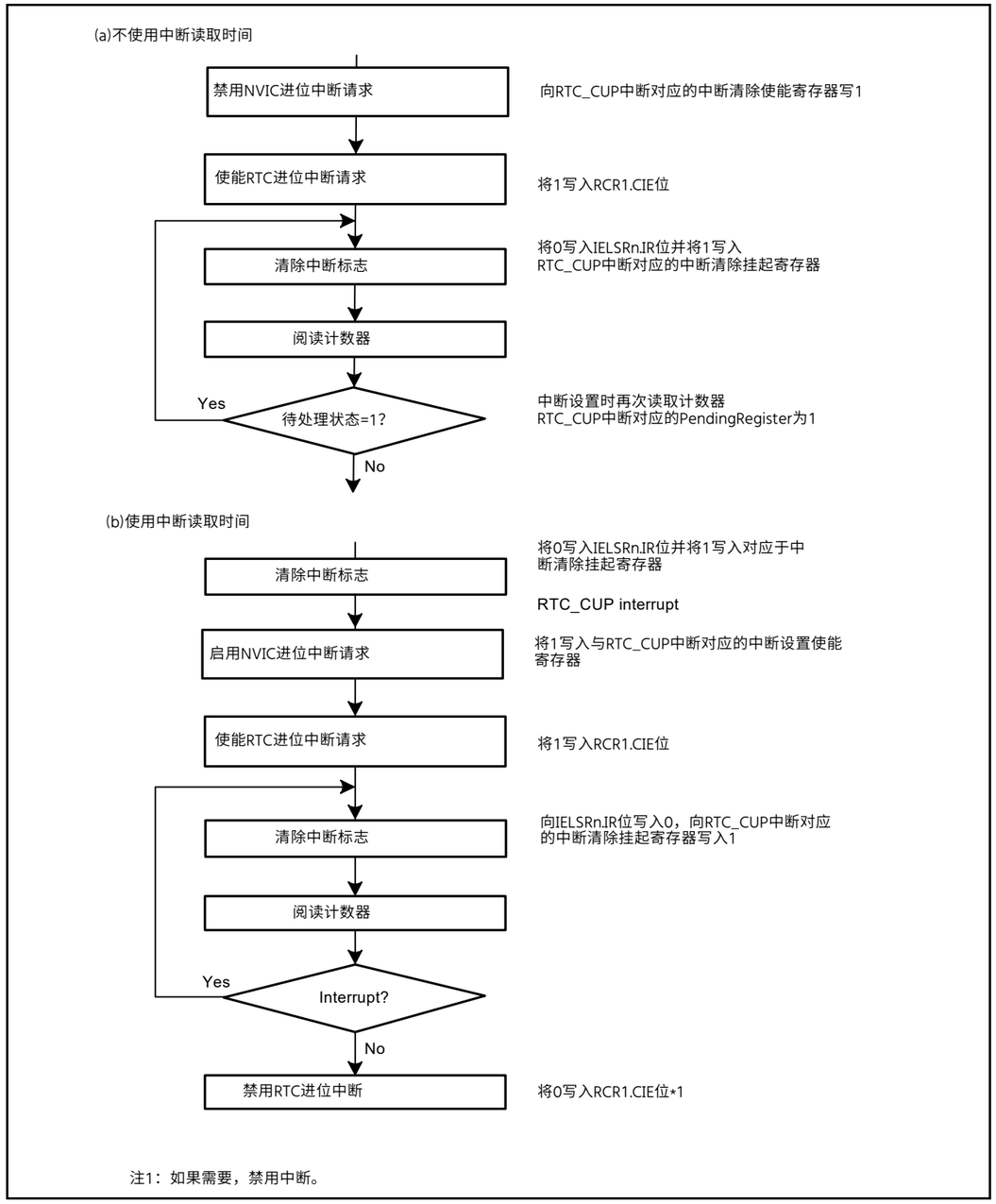


Figure 26.6 阅读时间

如果在读取64-Hz计数器和时间时发生进位，则无法获得正确的时间，因此必须再次读取它们。不使用中断读取时间的过程如图26.6(a)所示，使用进位中断的过程如图26.6所示。为保持程序简单，瑞萨推荐在大多数情况下使用方法(a)。

26.3.6 Alarm Function

Figure 26.7 shows how to use the alarm function.

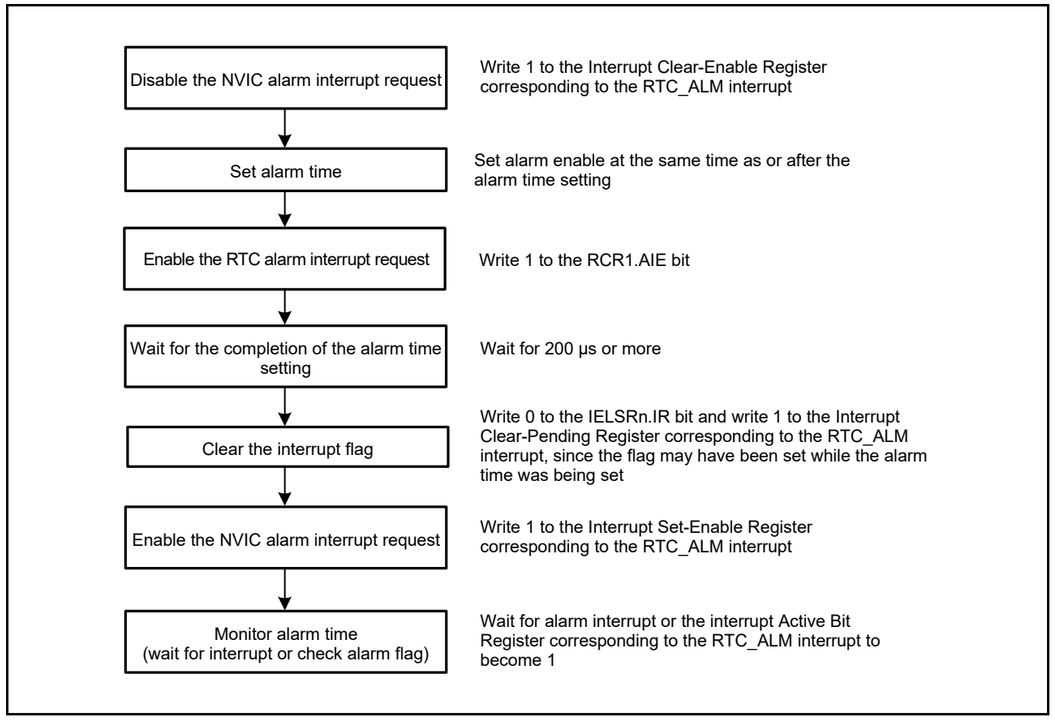


Figure 26.7 Using the alarm function

In calendar count mode, an alarm can be generated by any one of year, month, date, day-of-week, hour, minute or second, or any combination of those. Write 1 to the ENB bit in the alarm registers involved in the alarm setting, and set the alarm time in the lower bits. Write 0 to the ENB bit in registers not involved in the alarm setting.

In binary count mode, an alarm can be generated in any bit combination of 32 bits. Write 1 to the ENB bit of the alarm enable register associated with the target bit of the alarm, and set the alarm time in the alarm register. For bits that are not the target of the alarm, write 0 to the ENB bit of the alarm enable register.

When the counter and the alarm time match, the IELSRn.IR bit and Interrupt Set-Pending/Clear-Pending Register associated with the RTC_ALM interrupt are set to 1. Alarm detection can be confirmed by reading the interrupt Set-Pending Register associated with the RTC_ALM interrupt, but an interrupt should be used in most cases. If 1 is set in the Interrupt Set-Enable Register associated with the RTC_ALM interrupt, an alarm interrupt is generated in the event of the alarm, enabling the alarm to be detected.

Writing 0 sets the IELSRn.IR bit associated with the RTC_ALM interrupt to 0. If interrupt is enabled, the Interrupt Set-Pending/Clear-Pending Register associated with the RTC_ALM interrupt is cleared automatically after exiting the interrupt handler. Otherwise, write 1 to the Interrupt Clear-Pending Register associated with the RTC_ALM interrupt to clear it.

When the counter and the alarm time match in a low power state, the MCU returns from the low power state. In Deep Software Standby mode, the MCU returns from the Deep Software Standby mode even when the alarm interrupt request is disabled.

26.3.7 Procedure for Disabling Alarm Interrupt

Figure 26.8 shows the procedure for disabling the enabled alarm interrupt request.

26.3.6 报警功能

图26.7显示了如何使用报警功能。

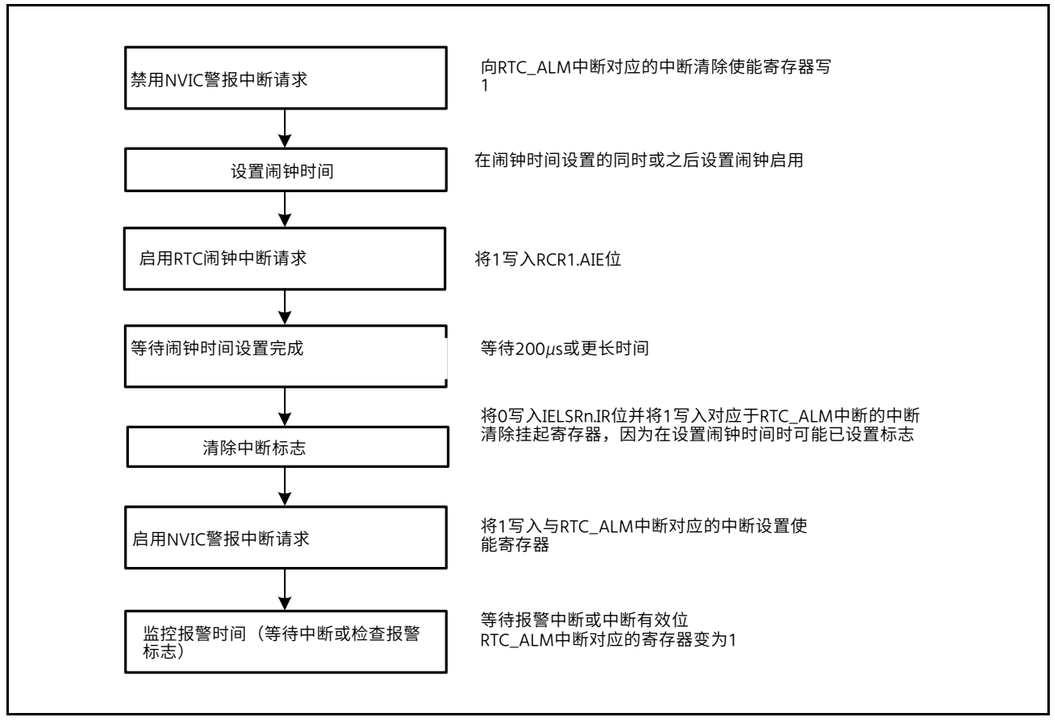


Figure 26.7 使用报警功能

在日历计数模式下，可以通过年、月、日、星期、小时、分钟或秒中的任何一个或它们的任意组合来生成警报。将1写入涉及闹钟设置的闹钟寄存器的ENB位，并在低位设置闹钟时间。将0写入与报警设置无关的寄存器中的ENB位。

在二进制计数模式下，可以以32位的任意位组合产生报警。将1写入与闹钟目标位相关的闹钟使能寄存器的ENB位，并在闹钟寄存器中设置闹钟时间。对于不是警报目标的位，将0写入警报使能寄存器的ENB位。

当计数器和闹钟时间匹配时，与RTC_ALM中断相关的IELSRn.IR位和中断设置挂起清除挂起寄存器设置为1。可以通过读取与RTC_ALM中断相关的中断设置挂起寄存器来确认报警检测，但在大多数情况下应该使用中断。如果在与RTC_ALM中断相关的中断设置使能寄存器中设置为1，则在发生警报时会产生警报中断，从而能够检测到警报。

写入0会将与RTC_ALM中断关联的IELSRn.IR位设置为0。如果启用中断，则与RTC_ALM中断关联的InterruptSetPendingClear-Pending寄存器会在退出中断处理程序后自动清除。否则，将1写入与RTC_ALM中断相关的中断清除挂起寄存器以将其清除。

当计数器和闹钟时间在低功耗状态下匹配时，MCU从低功耗状态返回。在深软件待机模式，即使警报中断请求被禁用，MCU也会从深度软件待机模式返回。

26.3.7 禁用警报中断的步骤

图26.8显示了禁用启用的警报中断请求的过程。

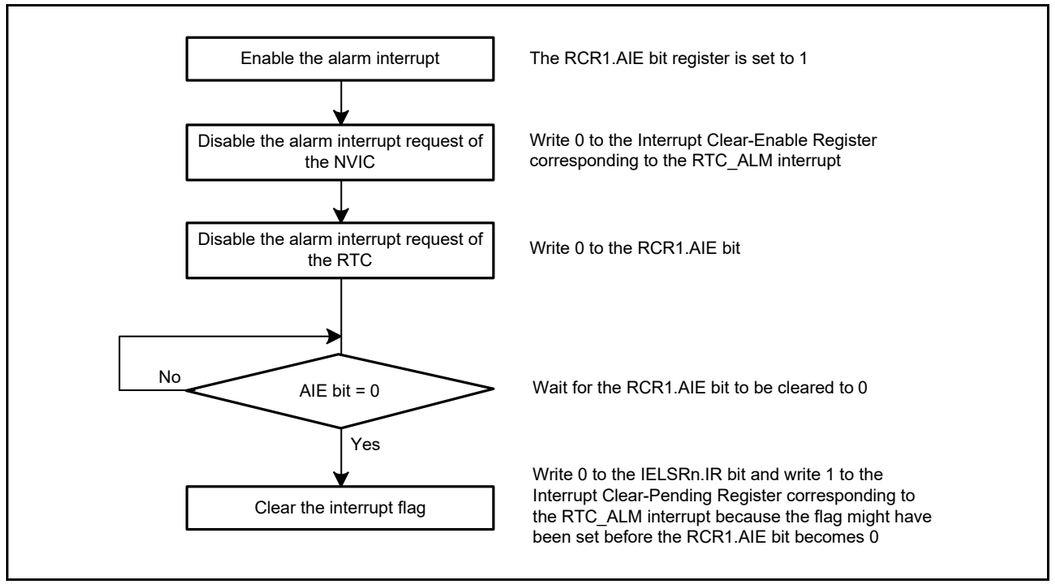


Figure 26.8 Procedure for disabling alarm interrupt request

26.3.8 Time Error Adjustment Function

The time error adjustment function is used to correct errors, running fast or slow, in the time caused by variation in the precision of oscillation by the sub-clock oscillator. Because 32,768 cycles of the sub-clock oscillator constitute 1 second of operation when the sub-clock oscillator is selected, the clock runs fast if the sub-clock frequency is high and slow if the sub-clock frequency is low.

The time error adjustment functions include:

- Automatic adjustment
- Adjustment by software.

Use the RCR2.AADJE bit to select automatic adjustment or adjustment by software.

26.3.8.1 Automatic adjustment

Enable automatic adjustment by setting the RCR2.AADJE bit to 1. Automatic adjustment is the addition or subtraction of the value counted by the prescaler to or from the value in the RADJ register every time the adjustment period selected by the RCR2.AADJP bit elapses.

(1) Example 1: Sub-clock oscillator running at 32.769 kHz

(a) Adjustment procedure

When the sub-clock oscillator is running at 32.769 kHz, 1 second elapses every 32,769 clock cycles. The RTC is meant to run at 32,768 clock cycles, so the clock runs fast by 1 clock cycle every second. The time on the clock is fast by 60 clock cycles per minute, so adjustment can take the form of setting the clock back by 60 cycles every minute.

Register settings: (when RCR2.CNTMD = 0)

- RCR2.AADJP = 0 (adjustment every minute)
- RADJ.PMADJ[1:0] = 10b (adjustment is performed by the subtraction from the prescaler)
- RADJ.ADJ[5:0] = 60 (3Ch).

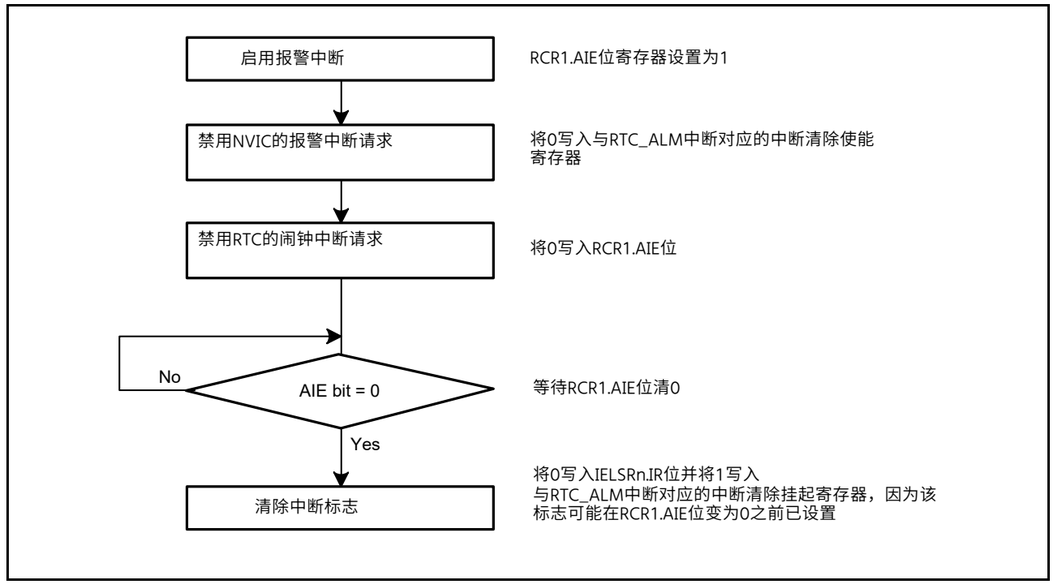


Figure 26.8 禁用报警中断请求的步骤

26.3.8 时间误差调整功能

时间误差调整功能用于校正子时钟振荡器振荡精度变化引起的时间误差，运行速度快或慢。由于在选择子时钟振荡器时，子时钟振荡器的32 768个周期构成1秒的运行时间，因此如果子时钟频率高，则时钟运行快，如果子时钟频率低，则时钟运行慢。

时间误差调整功能包括：

- 自动调整
- 通过软件调整。

使用RCR2.AADJE位选择自动调整或软件调整。

26.3.8.1 自动调整

通过将RCR2.AADJE位设置为1来启用自动调整。自动调整是每次经过RCR2.AADJP位选择的调整周期时，将预分频器计数的值与RADJ寄存器中的值相加或相减。

(1) 示例1：运行在32.769kHz的子时钟振荡器

(a) 调整程序

当副时钟振荡器以32.769kHz运行时，每32 769个时钟周期经过1秒。RTC旨在以32 768个时钟周期运行，因此时钟以每秒1个时钟周期的速度运行。时钟上的时间每分钟快60个时钟周期，因此调整可以采取将时钟每分钟调回60个周期的形式。

Register settings: (when RCR2.CNTMD = 0)

- RCR2.AADJP = 0 (adjustment every minute)
- RADJ.PMADJ[1:0]=10b（通过预分频器的减法进行调整）
- RADJ.ADJ[5:0] = 60 (3Ch).

(2) Example 2: Sub-clock oscillator running at 32.766 kHz

(a) Adjustment procedure

When the sub-clock oscillator is running at 32.766 kHz, 1 second elapses every 32,766 clock cycles. The RTC is meant to run at 32,768 clock cycles, so the clock runs slow by 2 clock cycles every second. The time on the clock is slow by 20 clock cycles every 10 seconds, so adjustment can take the form of setting the clock forward by 20 cycles every 10 seconds.

Register settings: (when RCR2.CNTMD = 0)

- RCR2.AADJP = 1 (adjustment every 10 seconds)
- RADJ.PMADJ[1:0] = 01b (adjustment is performed by the addition to the prescaler)
- RADJ.ADJ[5:0] = 20 (14h).

(3) Example 3: Sub-clock oscillator running at 32.764 kHz

(a) Adjustment procedure

At 32.764 kHz, 1 second elapses on 32,764 clock cycles. Because the RTC operates for 32,768 clock cycles as 1 second, the clock is delayed for 4 clock cycles per second. In 8 seconds, the delay is 32 clock cycles, therefore correction can be made by advancing the clock 32 clock cycles every 8 seconds.

Register settings when the RCR2.CNTMD bit is 1

- RCR2.AADJP = 1 (adjustment every 8 seconds)
- RADJ.PMADJ[1:0] = 01b (adjustment is performed by the addition to the prescaler)
- RADJ.ADJ[5:0] = 32 (20h).

26.3.8.2 Adjustment by software

Enable adjustment by software by setting the RCR2.AADJE bit to 0. Adjustment by software is the addition or subtraction of the value counted by the prescaler to or from the value in the RADJ register on execution of a write instruction to the RADJ register.

(1) Example 1: Sub-clock oscillator running at 32.769 kHz

(a) Adjustment procedure

When the sub-clock oscillator is running at 32.769 kHz, 1 second elapses every 32,769 clock cycles. The RTC is meant to run at 32,768 clock cycles, so the clock runs fast by one clock cycle every second. The time on the clock is fast by one clock cycle per second, so adjustment can take the form of setting the clock back by 1 cycle every second.

(b) Register settings

- RADJ.PMADJ[1:0] = 10b (adjustment is performed by the subtraction from the prescaler)
- RADJ.ADJ[5:0] = 1 (01h).
  This is written to the RADJ register once per 1-second interrupt.

26.3.8.3 Procedure for changing the mode of adjustment

When changing the mode of adjustment, change the value of the AADJE bit in RCR2 after setting the RADJ.PMADJ[1:0] bits to 00b (adjustment is not performed).

To change adjustment by software to automatic adjustment:

1. Set the RADJ.PMADJ[1:0] bits to 00b (adjustment is not performed).
2. Set the RCR2.AADJE bit to 1 (automatic adjustment is enabled).
3. Use the RCR2.AADJP bit to select the period of adjustment.
4. In RADJ, set the PMADJ[1:0] bits for addition or subtraction and the ADJ[5:0] bits to the value for use in time error adjustment.

(2) 示例2：以32.766kHz运行的子时钟振荡器

(a) 调整程序

当副时钟振荡器以32.766kHz运行时，每32 766个时钟周期经过1秒。RTC旨在以32 768个时钟周期运行，因此时钟每秒运行2个时钟周期。时钟上的时间每10秒慢20个时钟周期，因此调整可以采取将时钟每10秒向前20个周期的形式。

Register settings: (when RCR2.CNTMD = 0)

- RCR2.AADJP = 1 (adjustment every 10 seconds)
- RADJ.PMADJ[1:0]=01b（通过加到预分频器进行调整）
- RADJ.ADJ[5:0] = 20 (14h).

(3) 示例3：以32.764kHz运行的子时钟振荡器

(a) 调整程序

在32.764kHz时，32 764个时钟周期经过1秒。由于RTC以1秒为单位运行32 768个时钟周期，因此时钟每秒延迟4个时钟周期。在8秒内，延迟为32个时钟周期，因此可以通过每8秒将时钟提前32个时钟周期来进行校正。

RCR2.CNTMD位为1时的寄存器设置

- RCR2.AADJP = 1 (adjustment every 8 seconds)
- RADJ.PMADJ[1:0]=01b（通过加到预分频器进行调整）
- RADJ.ADJ[5:0] = 20 (14h).

26.3.8.2 软件调整

通过将RCR2.AADJE位设置为0来启用软件调整。软件调整是在对RADJ寄存器执行写指令时，将预分频器计数的值与RADJ寄存器中的值相加或相减。

(1) 示例1：运行在32.769kHz的子时钟振荡器

(a) 调整程序

当副时钟振荡器以32.769kHz运行时，每32 769个时钟周期经过1秒。RTC旨在以32 768个时钟周期运行，因此时钟以每秒一个时钟周期的速度运行。时钟上的时间每秒快一个时钟周期，因此调整可以采取将时钟每秒调回一个周期的形式。

(b) 注册设置

- RADJ.PMADJ[1:0]=10b（通过预分频器的减法进行调整）
- RADJ.ADJ[5:0] = 1 (01h).
  每1秒中断一次将其写入RADJ寄存器。

26.3.8.3 更改调整模式的步骤

改变调节方式时，设置好后改变RCR2中ADJE位的值
RADJ.PMADJ[1:0]位到00b（不执行调整）。

将软件调整改为自动调整：

1. 将RADJ.PMADJ[1:0]位设置为00b（不执行调整）。
2. 将RCR2.AADJE位设置为1（启用自动调整）。
3. 使用RCR2.AADJP位选择调整周期。
4. 在RADJ中，将PMADJ[1:0]位设置为加法或减法，并将ADJ[5:0]位设置为用于时间误差调整的值。

To change automatic adjustment to adjustment by software:

1. Set the RADJ.PMADJ[1:0] bits to 00b (adjustment is not performed).
2. Set the RCR2.AADJE bit to 0 (adjustment by software is enabled).
3. Proceed with the adjustment by setting the RADJ.PMADJ[1:0] bits for addition or subtraction and the RADJ.ADJ[5:0] bits to the value for use in time error adjustment at the wanted time. After that, the time is adjusted every time a value is written to the RADJ register.

26.3.8.4 Procedure for stopping adjustment

Stop the adjustment by setting the RADJ.PMADJ[1:0] bits to 00b (adjustment is not performed).

26.3.8.5 Capturing the time

The RTC is capable of storing the month, date, hour, minute and second/binary counters 3 to 0 by detecting an edge of a signal on a time capture event input pin.

A noise filter can also be used on a time capture event input pin. If the noise filter is enabled, the TCST bit is set to 1 when the input level on the pin matches three times.

The noise filter can be switched on or off for each of the time capture event input pins. Set VBTICTLR.VCHnIEN (n = 0 to 2) to 1 to enable the RTCICn input. Operation when the noise filter is off is shown in Figure 26.9 and operation when the noise filter is on is shown in Figure 26.10.

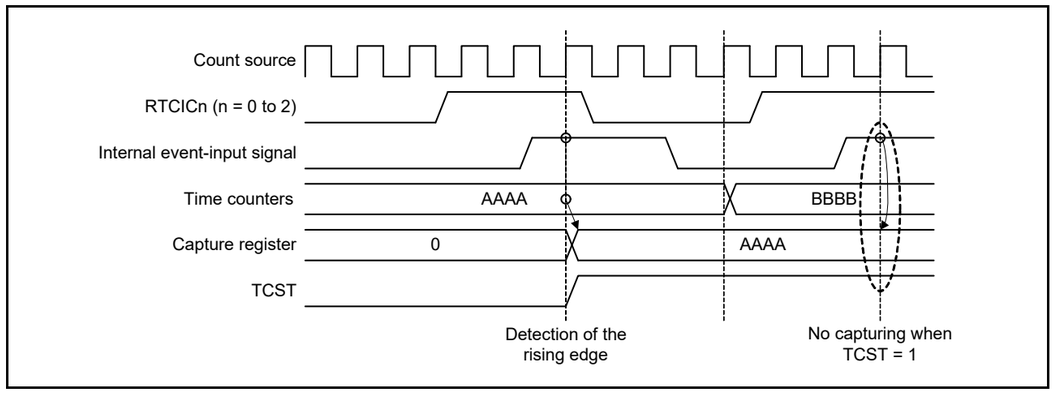


Figure 26.9 Timing of a time capture operation with the filter off

将自动调整更改为软件调整：

1. 将RADJ.PMADJ[1:0]位设置为00b（不执行调整）。
2. 将RCR2.AADJE位设置为0（启用软件调整）。
3. 通过设置RADJ.PMADJ[1:0]位进行加法或减法以及RADJ.ADJ[5:0]位用于在所需时间进行时间误差调整的值。之后，每次将值写入RADJ寄存器时都会调整时间。

26.3.8.4 停止调整的步骤

通过将RADJ.PMADJ[1:0]位设置为00b来停止调整（不执行调整）。

26.3.8.5 捕捉时间

RTC能够通过检测时间捕捉事件输入引脚上的信号沿来存储月、日、小时、分钟和秒二进制计数器3到0。

噪声滤波器也可用于时间捕捉事件输入引脚。如果启用了噪声滤波器，则当引脚上的输入电平匹配3次时，TCST位设置为1。

可以为每个时间捕捉事件输入引脚打开或关闭噪声滤波器。将VBTICTLR.VCHnIEN（n=0到2）设置为1以启用RTCICn输入。噪声滤波器关闭时的操作如图26.9所示，噪声滤波器打开时的操作如图26.10所示。

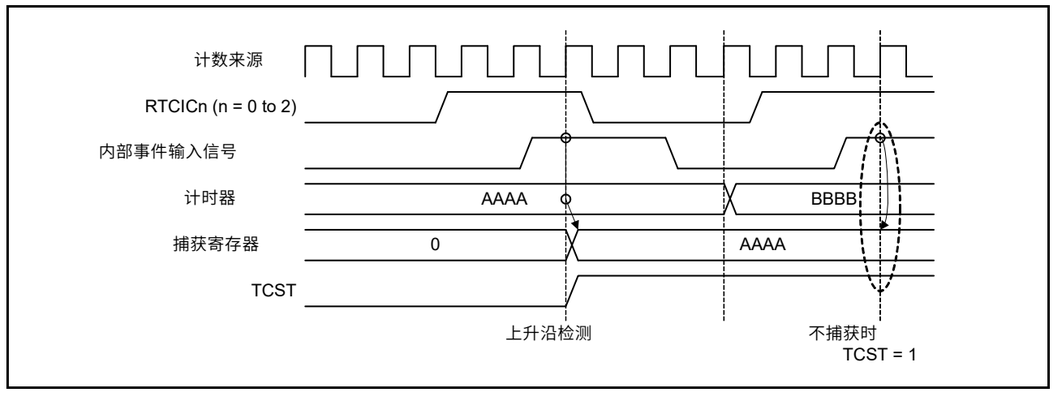


Figure 26.9 过滤器关闭的时间捕获操作的时序

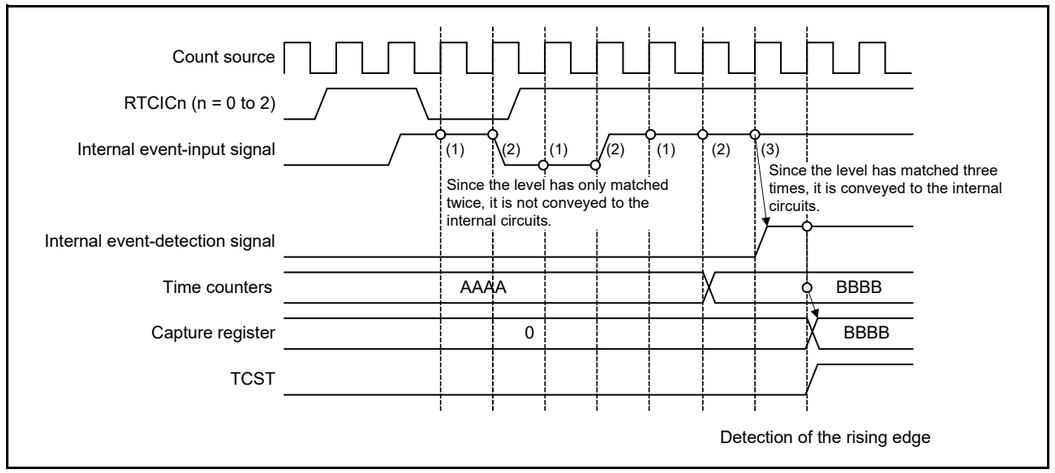


Figure 26.10 Timing of a time capture operation with the filter on

26.4 Interrupt Sources

The RTC has three interrupt sources and are listed in Table 26.3.

Table 26.3 RTC interrupt sources

Name	Interrupt source
RTC_ALM	Alarm interrupt
RTC_PRD	Periodic interrupt
RTC_CUP	Carry interrupt

(1) Alarm interrupt (RTC_ALM)

This interrupt is generated based on the result of comparison between the alarm registers and RTC counters. For details, see section 26.3.6, Alarm Function.

Because there is a possibility that the interrupt flag might be set to 1 when the settings of the alarm registers match the clock counters, wait for the alarm time settings to be confirmed and clear the IELSRn.IR bit and the interrupt Set-Pending Register associated with the RTC_ALM interrupt to 0 again after modifying values of the alarm registers. After the interrupt flag for the alarm interrupt is set to 1 and the state is returned to non-matching of the alarm registers and clock counters, the flag is not set again until there is another match or the values of the alarm registers are modified again.

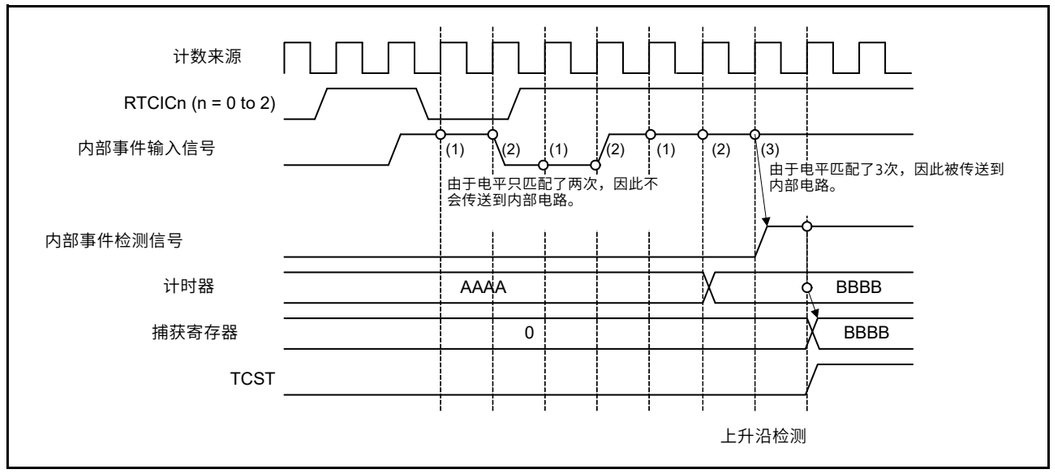


Figure 26.10 开启滤波器的时间捕获操作的时序

26.4 中断源

RTC具有三个中断源，列于表26.3中。

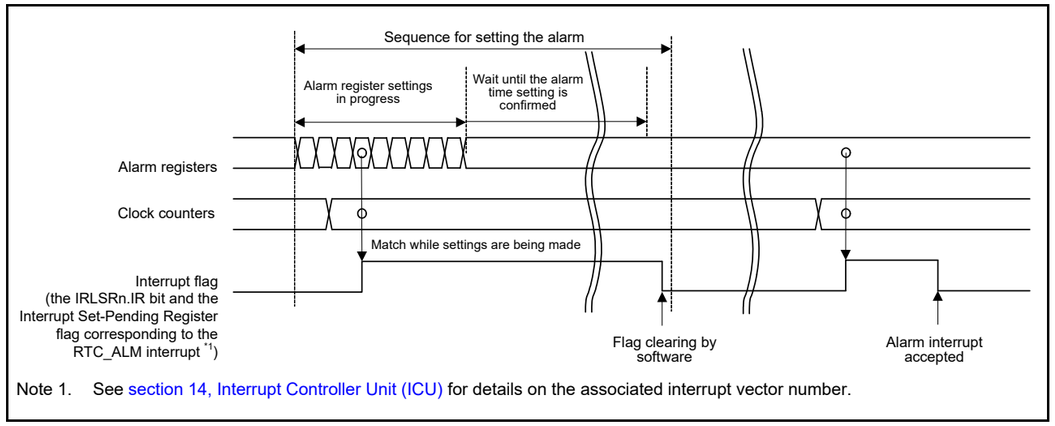
Table 26.3 RTC中断源

Name	中断源
RTC_ALM	报警中断
RTC_PRD	周期性中断
RTC_CUP	进位中断

(1) 闹钟中断(RTC_ALM)

该中断是根据闹钟寄存器和RTC计数器的比较结果产生的。有关详细信息，请参见第26.3.6节，报警功能。

因为当闹钟寄存器的设置与时钟计数器匹配时中断标志可能被设置为1，请等待闹钟时间设置被确认并清除IELSRn.IR位和与修改闹钟寄存器的值后，RTC_ALM中断再次为0。报警中断的中断标志置1后，状态返回到报警寄存器和时钟计数器不匹配，直到再次匹配或再次修改报警寄存器的值时才重新设置该标志.



Note 1. See section 14, Interrupt Controller Unit (ICU) for details on the associated interrupt vector number.

Figure 26.11 Timing diagram for the alarm interrupt (RTC_ALM)

(2) Periodic interrupt (RTC_PRD)

This interrupt is generated at intervals of 2 seconds, 1 second, 1/2 second, 1/4 second, 1/8 second, 1/16 second, 1/32 second, 1/64 second, 1/128 second, or 1/256 second. The interrupt interval can be selected through the RCR1.PES[3:0] bits.

(3) Carry interrupt (RTC_CUP)

This interrupt is generated when a carry to the second counter/binary counter 0 occurred or a carry to the R64CNT counter occurred during read access to the 64-Hz counter.

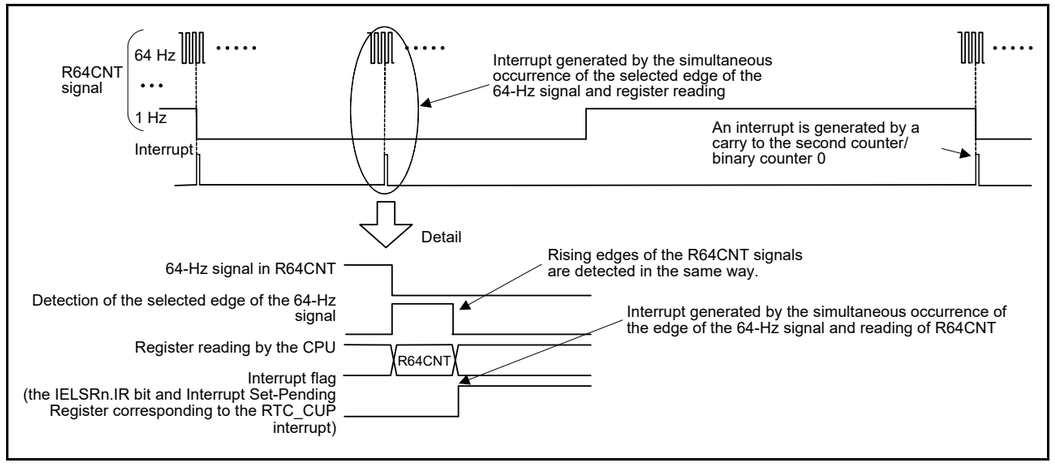


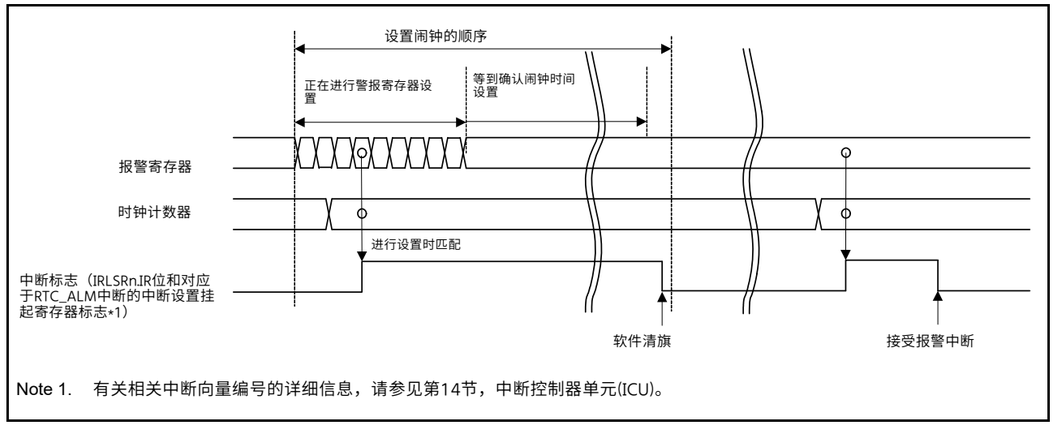
Figure 26.12 Timing diagram for the carry interrupt (RTC_CUP)

26.5 Event Link Output

The RTC generates periodic event output (RTC_PRD) event signal for the Event Link Controller (ELC) that can be used to initiate operations by other modules selected in advance.

The periodic event signal is output at the interval selected from 1/256, 1/128, 1/64, 1/32, 1/16, 1/8, 1/4, 1/2, 1, and 2 seconds by setting the RCR1.PES[3:0] bits.

The event generation period immediately after the event generation is selected is not guaranteed.



Note 1. 有关相关中断向量编号的详细信息，请参见第14节，中断控制器单元(ICU)。

Figure 26.11 闹钟中断(RTC_ALM)的时序图

(2) 周期性中断(RTC_PRD)

此中断以2秒、1秒、12秒、14秒、18秒、116秒、132秒、164秒、1128秒或1256秒的间隔生成。可以通过RCR1.PES[3:0]位选择中断间隔。

(3) 进位中断(RTC_CUP)

当第二个计数器二进制计数器0的进位发生或在对64-Hz计数器的读访问期间发生对R64CNT计数器的进位时，将产生此中断。

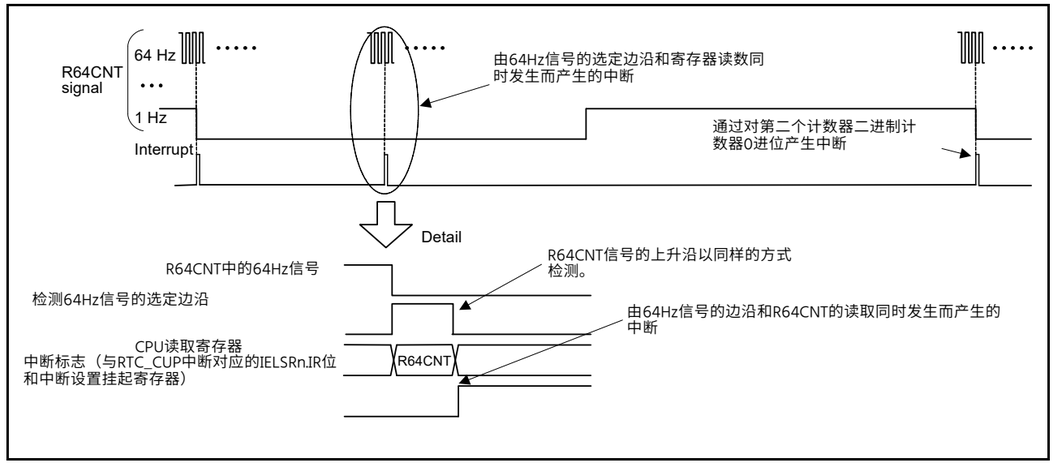


Figure 26.12 进位中断(RTC_CUP)的时序图

26.5 事件链接输出

RTC为事件链接控制器(ELC)生成周期性事件输出(RTC_PRD)事件信号，该信号可用于启动预先选择的其他模块的操作。

通过设置RCR1.PES[3:0，以从1256、1128、164、132、116、18、14、12、1和2秒中选择的间隔输出周期性事件信号]位。

不保证选择事件生成后的事件生成周期。

Note: If event linking from the RTC is used, only set the ELC after setting the RTC, for example initialization and time settings. Setting the RTC after the ELC can lead to output of unexpected event signals.

26.5.1 Interrupt Handling and Event Linking

The RTC has a bit to enable or disable periodic interrupts. An interrupt request signal is output for the CPU when an interrupt source is generated while the associated enable bit is enabled.

In contrast, an event link output signal is sent to other modules as an event signal through the ELC when an interrupt source is generated, regardless of the setting of the associated interrupt enable bit.

Note: Although alarm and periodic interrupts can still be output during Software Standby mode or Deep Software Standby mode, the periodic event signals for the ELC are not output.

26.6 Usage Notes

26.6.1 Register Writing during Counting

The following registers must not be written to during counting, that is, while the RCR2.START bit is 1:

- RSECCNT/BCNT0
- RMINCNT/BCNT1
- RHRCNT/BCNT2
- RDAYCNT
- RWKCNT/BCNT3
- RMONCNT
- RYRCNT
- RCR1.RTCOS
- RCR2.RTCOE
- RCR2.HR24
- RFRL.

The counter must be stopped before writing to any of these registers.

26.6.2 Use of Periodic Interrupts

The procedure for using periodic interrupts is shown in Figure 26.13.

The generation and period of the periodic interrupt can be changed by setting the RCR1.PES[3:0] bits. However, because the prescaler R64CNT and RSECCNT/BCNT0 are used to generate interrupts, the interrupt period is not guaranteed immediately after setting the RCR1.PES[3:0] bits. In addition, any of the following operation can affect the interrupt period:

- Stopping/restarting or resetting counter operation
- Reset by RTC software
- 30-second adjustment by changing the RCR2 value.

When the time error adjustment function is used, the interrupt generation period after adjustment is added or subtracted based on the adjustment value.

Note: 如果使用来自RTC的事件链接，请仅在设置RTC后设置ELC，例如初始化和时间设置。在ELC之后设置RTC会导致意外事件信号的输出。

26.5.1 中断处理和事件链接

RTC有一个位来启用或禁用周期性中断。当相应的使能位使能时产生中断源时，将向CPU输出中断请求信号。

相反，当产生中断源时，事件链接输出信号作为事件信号通过ELC发送到其他模块，而不管相关中断使能位的设置如何。

Note: 虽然在软件待机模式或深度软件期间仍然可以输出警报和周期性中断
待机模式下，不输出ELC的周期性事件信号。

26.6 使用说明

26.6.1 计数期间的寄存器写入

计数期间不得写入以下寄存器，即RCR2.START位为1时：

- RSECCNT/BCNT0
- RMINCNT/BCNT1
- RHRCNT/BCNT2
- RDAYCNT
- RWKCNT/BCNT3
- RMONCNT
- RYRCNT
- RCR1.RTCOS
- RCR2.RTCOE
- RCR2.HR24
- RFRL.

在写入任何这些寄存器之前，必须停止计数器。

26.6.2 使用周期性中断

使用周期性中断的过程如图26.13所示。

可以通过设置RCR1.PES[3:0]位来更改周期性中断的产生和周期。但是，因为预分频器R64CNT和RSECCNTBCNT0用于产生中断，所以在设置RCR1.PES[3:0]位后不能立即保证中断周期。此外，以下任何操作都会影响中断周期：

- 停止重新启动或重置计数器操作
- 通过RTC软件复位
- 通过更改RCR2值进行30秒调整。

使用时间误差调整功能时，根据调整值加减调整后的中断产生周期。

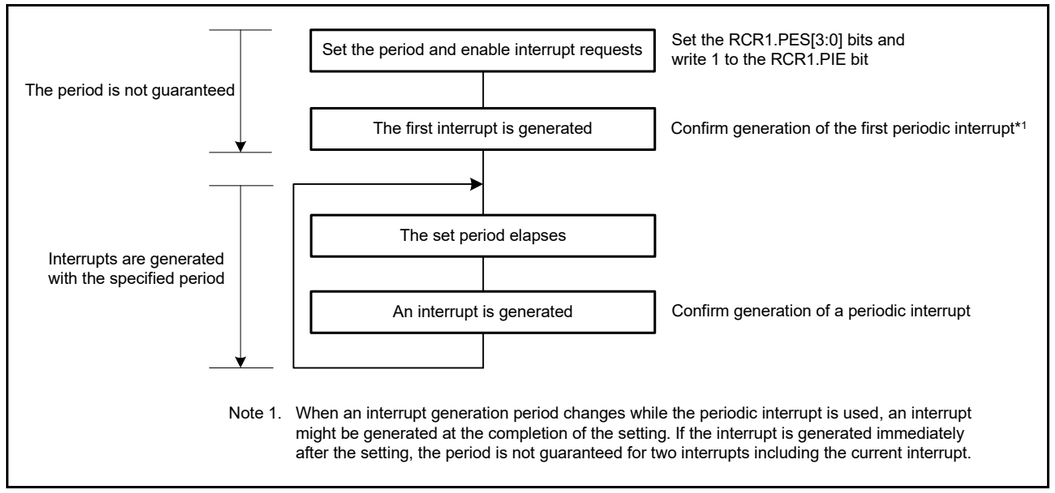


Figure 26.13 Using the periodic interrupt function

26.6.3 RTCOUT (1-Hz/64-Hz) Clock Output

Stopping/restarting or resetting counter operation, reset by RTC software, and the 30-second adjustment by changing the RCR2 value affects the period of RTCOUT (1-Hz/64-Hz) output. When the time error adjustment function is used, the period of RTCOUT (1-Hz/64-Hz) output after adjustment is added or subtracted based on the adjustment value.

26.6.4 Transitions to Low Power Modes after Setting Registers

A transition to a low power state (Software Standby mode, Deep Software Standby mode, or battery backup) during a write to an RTC register might corrupt the value in the register. After setting the register, confirm that the setting is in place before initiating a transition to a low power state.

26.6.5 Notes on Writing to and Reading from Registers

- When reading a counter register such as the second counter after writing to the counter register, follow the procedure in section 26.3.5, Reading 64-Hz Counter and Time
- The value written to the count registers, alarm registers, year alarm enable register, bits RCR2.AADJE, AADJP, and HR24, RCR4 register, or frequency register is reflected when four read operations are performed after writing
- The values written to the RCR1.CIE, RCR1.RTCOS, and RCR2.RTCOE bits can be read immediately after writing
- To read the value from the timer counter after return from a reset, Software Standby mode, Deep Software Standby mode, or the battery backup state, wait for 1/128 second while the clock is operating (RCR2.START bit is 1)
- After a reset is generated, write to the RTC register after 6 cycles of the count source clock elapse.

26.6.6 Changing the Count Mode

When changing the count mode (calendar/binary), set the RCR2.START bit to 0, stop the counting operation, then restart it from the initial setting. For details on the initial setting, see section 26.3.1, Outline of Initial Settings of Registers after Power On.

26.6.7 Initialization Procedure when the RTC Is Not To Be Used

Registers in the RTC are not initialized by a reset. Depending on the initial state, the generation of an unintentional interrupt request or operation of the counter might lead to increased power consumption.

For applications that do not require a realtime clock, initialize the registers by following the initialization procedure shown in Figure 26.14.

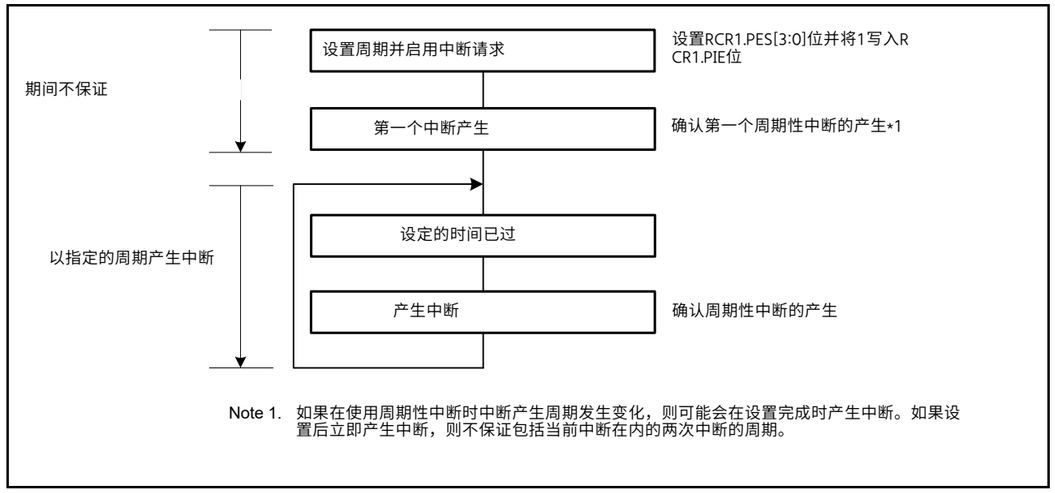


Figure 26.13 使用周期性中断功能

26.6.3 RTCOUT(1-Hz64-Hz)时钟输出

停止重新启动或重置计数器操作，通过RTC软件重置，并通过更改30秒调整RCR2值影响RTCOUT(1-Hz64-Hz)输出的周期。使用时间误差调整功能时，调整后的RTCOUT（1-Hz64-Hz）输出的周期根据调整值加减。

26.6.4 设置寄存器后转换到低功耗模式

在写入RTC寄存器期间转换到低功耗状态（软件待机模式、深度软件待机模式或电池备份）可能会损坏寄存器中的值。设置寄存器后，在开始转换到低功耗状态之前确认设置到位。

26.6.5 关于写入和读取寄存器的注意事项

- 在写入计数器寄存器后读取计数器寄存器（例如第二个计数器）时，请按照第26.3.5节中的步骤，读取64-Hz计数器和时间
- 写入计数寄存器、闹钟寄存器、年份闹钟启用寄存器、位RCR2.AADJE、AADJP和HR24、RCR4寄存器或频率寄存器在写后进行四次读操作时反映
- 写入RCR1.CIE、RCR1.RTCOS和RCR2.RTCOE位的值可在写入后立即读取
- 要在从复位、软件待机模式、深度软件待机模式或电池备份状态返回后从定时器计数器读取值，请在时钟运行时等待1128秒（RCR2.START位为1）
- 产生复位后，在经过6个计数源时钟周期后写入RTC寄存器。

26.6.6 更改计数模式

更改计数模式（日历二进制）时，将RCR2.START位设置为0，停止计数操作，然后从初始设置重新启动。有关初始设置的详细信息，请参阅第26.3.1节“通电后寄存器初始设置概述”。

26.6.7 不使用RTC时的初始化程序

RTC中的寄存器不会因复位而初始化。根据初始状态，意外中断请求的生成或计数器的操作可能会导致功耗增加。

对于不需要实时时钟的应用程序，按照图26.14所示的初始化过程初始化寄存器。

Alternatively, when the sub-clock oscillator is not used as the system clock or realtime clock, the counter can be stopped by writing 0 (subclock oscillator is selected) to the RCR4.RCKSEL bit and stopping the sub-clock oscillator. To stop the sub-clock oscillator, write 1 to the SOSCCR.SOSTP bit.

For details on the setting of the SOSCCR.SOSTP bit, see section 9, Clock Generation Circuit.

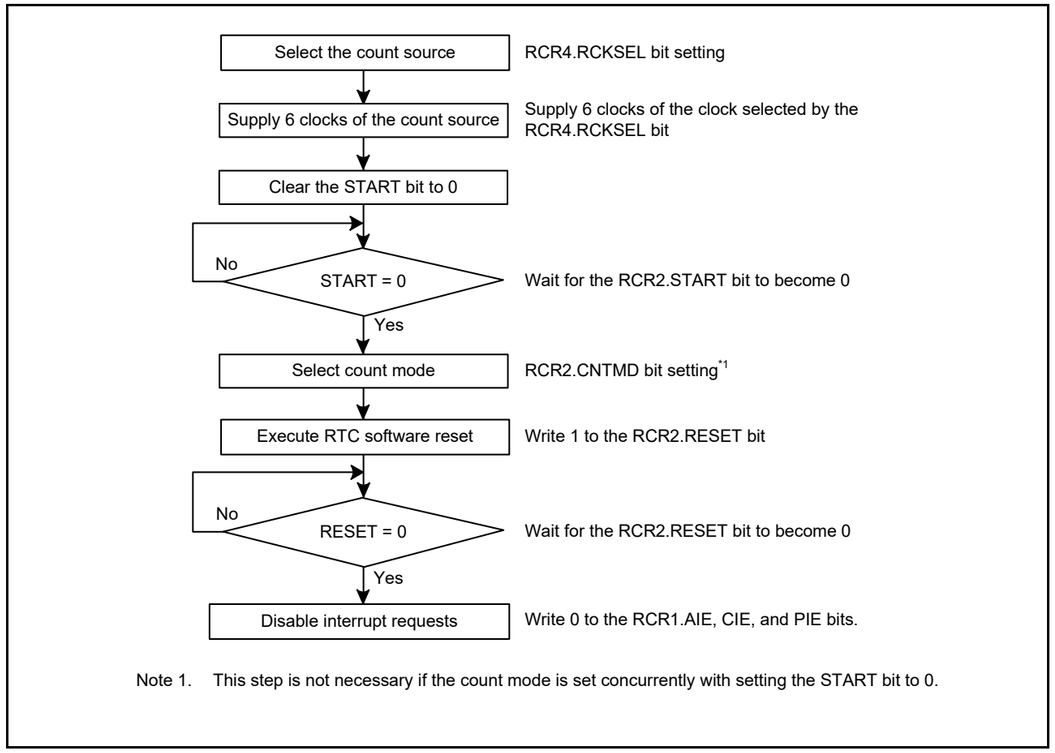


Figure 26.14 Initialization procedure

26.6.8 When Switching Source Clock

When switching a clock source by changing SCKSCR.CKSEL[2:0], the clock output from the selector stops for 4 cycles of the switched clock. If the RTC periodical interrupt or RTC periodical event output was generated at this time, the interrupt or event is invalid.

或者，当副时钟振荡器不用作系统时钟或实时时钟时，可以通过向RCR4.RCKSEL位写入0（选择副时钟振荡器）并停止副时钟振荡器来停止计数器。要停止副时钟振荡器，将1写入SOSCCR.SOSTP位。

有关SOSCCR.SOSTP位设置的详细信息，请参见第9节，时钟生成电路。

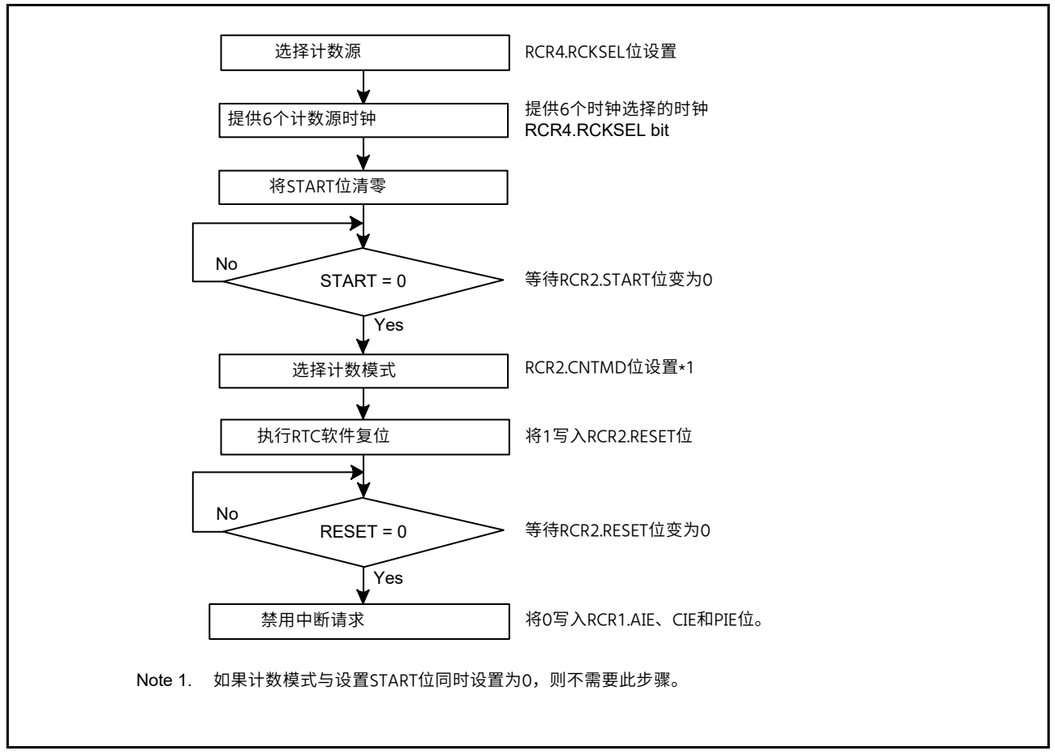


Figure 26.14 初始化程序

26.6.8 切换源时钟时

当通过改变SCKSCR.CKSEL[2:0]来切换时钟源时，选择器的时钟输出在切换时钟的4个周期内停止。如果此时产生了RTC周期性中断或RTC周期性事件输出，则该中断或事件无效。

27. Watchdog Timer (WDT)

27.1 Overview

The Watchdog Timer (WDT) is a 14-bit down-counter and can be used to reset the MCU when the counter underflows because the system has run out of control and become unable to refresh the WDT. In addition, the WDT can be used to generate a non-maskable interrupt or an underflow interrupt. The refresh-permitted period can be set to refresh the counter and to detect when the system runs out of control.

Table 27.1 lists the WDT specifications and Figure 27.1 shows a block diagram.

Table 27.1 WDT specifications

Parameter	Specifications
Count source	Peripheral clock (PCLKB)
Clock division ratio	Division by 4, 64, 128, 512, 2,048, or 8,192
Counter operation	Counting down using a 14-bit down-counter
Conditions for starting the counter	• Auto start mode: Counting automatically starts after a reset, or after an underflow or refresh error occurs • Register start mode: Counting is started with a refresh by writing to the WDTRR register.
Conditions for stopping the counter	• Reset (the down-counter and other registers return to their initial values) • A counter underflows or a refresh error is generated.
Window function	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods)
WDT reset sources	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error).
Non-maskable interrupt/interrupt sources	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error).
Reading of the counter value	The down-counter value can be read by the WDTSR register
Event link function (output)	• Down-counter underflow event output • Refresh error event output.
Output signal (internal signal)	• Reset output • Interrupt request output • Sleep-mode count stop control output.

27. 看门狗定时器(WDT)

27.1 Overview

看门狗定时器(WDT)是一个14位递减计数器，可用于在计数器下溢时复位MCU，因为系统已经失控并且无法刷新WDT。此外，WDT可用于产生不可屏蔽中断或下溢中断。可以设置刷新允许周期来刷新计数器并检测系统何时失控。

表27.1列出了WDT规范，图27.1显示了框图。

Table 27.1 WDT specifications

Parameter	Specifications
计数来源	外设时钟(PCLKB)
时钟分频比	除以4、64、128、512、2 048或8 192
计数器操作	使用14位递减计数器进行递减计数
启动计数器的条件	自动启动模式：在复位后或发生下溢或刷新错误后自动开始计数 寄存器启动模式：通过写入WDTRR寄存器以刷新开始计数。
停止计数器的条件	复位（递减计数器和其他寄存器返回其初始值） 计数器下溢或产生刷新错误。
窗口功能	可以指定窗口开始和结束位置（允许刷新和禁止刷新期间）
WDT复位源	递减计数器下溢 在允许刷新的时间之外刷新（刷新错误）。
Non-maskable interrupt/interrupt sources	递减计数器下溢 在允许刷新的时间之外刷新（刷新错误）。
读取计数器值	递减计数器的值可以通过WDTSR寄存器读取
事件链接功能（输出）	递减计数器下溢事件输出 刷新错误事件输出。
输出信号（内部信号）	复位输出 中断请求输出 睡眠模式计数停止控制输出。

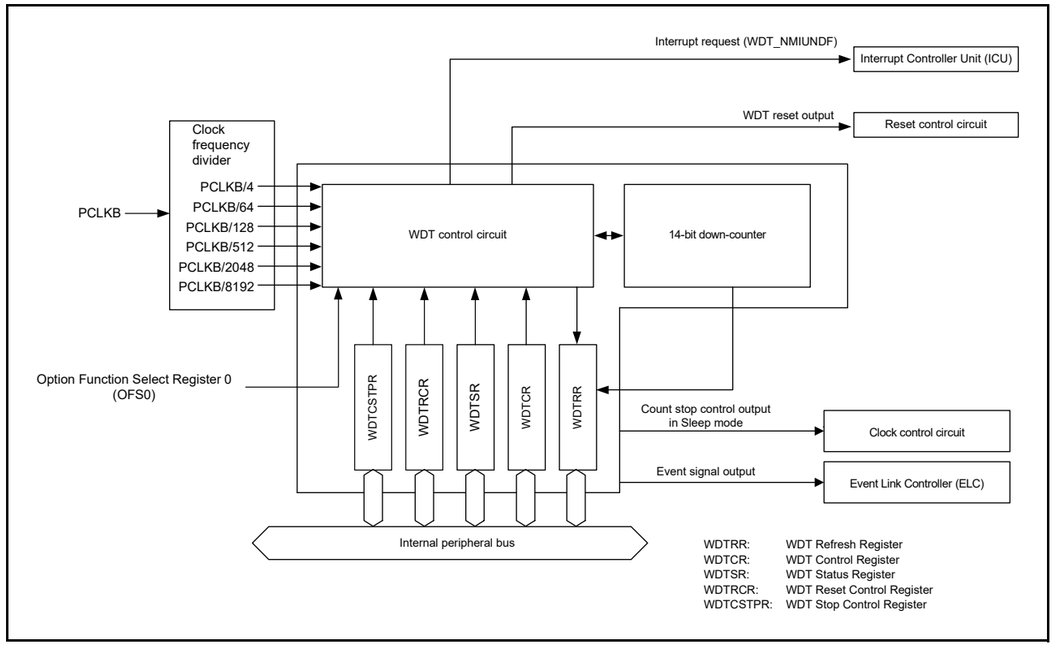


Figure 27.1 WDT block diagram

27.2 Register Descriptions

27.2.1 WDT Refresh Register (WDTRR)

Address(es): WDT.WDTRR 4004 4200h

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1

Bit	Description	R/W
b7 to b0	The down-counter is refreshed by writing 00h and then writing FFh to this register	R/W

The WDTRR register refreshes the down-counter of the WDT.

The down-counter of the WDT is refreshed by writing 00h and then writing FFh to WDTRR (refresh operation) within the refresh-permitted period.

After the down-counter is refreshed, it starts counting down from the value selected in the WDT Timeout Period Select bits (OFS0.WDTTOPS[1:0]) in Option Function Select Register 0 in auto start mode. In register start mode, counting down starts from the value selected in the Timeout Period Select bits (WDTCR.TOPS[1:0]) in the WDT Control Register.

When 00h is written, the read value is 00h. When a value other than 00h is written, the read value is FFh. For details on the refresh operation, see section 27.3.3, Refresh Operation.

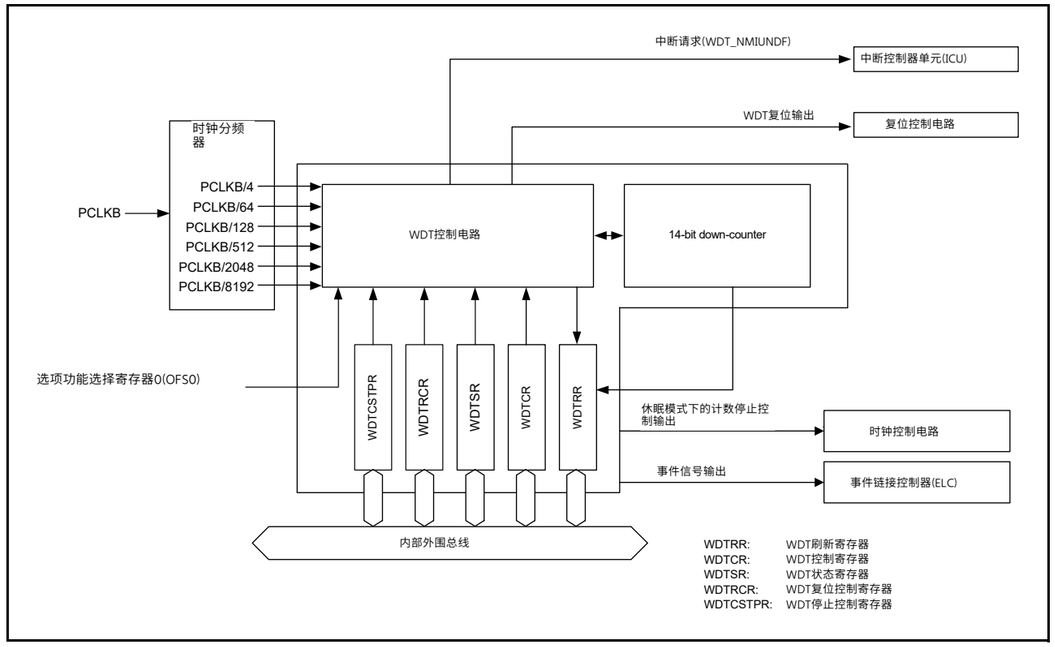


Figure 27.1 看门狗框图

27.2 注册说明

27.2.1 WDT刷新寄存器(WDTRR)

Address(es): WDT.WDTRR 4004 4200h

	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	1	1	1	1	1	1	1	1

Bit	Description	R/W
b7 to b0	通过写入00h然后将FFh写入该寄存器来刷新递减计数器	R/W

WDTRR寄存器刷新WDT的递减计数器。

WDT的递减计数器通过写入00h进行刷新，然后在允许刷新期间将FFh写入WDTRR（刷新操作）。

递减计数器刷新后，在自动启动模式下，它从选项功能选择寄存器0中的WDT超时周期选择位(OFS0.WDTTOPS[1:0])中选择的值开始递减计数。在寄存器启动模式下，倒计时从WDT控制寄存器的超时周期选择位(WDTCR.TOPS[1:0])中选择的值开始。

写入00h时，读取值为00h。写入00h以外的值时，读取值为FFh。有关刷新操作的详细信息，请参阅第27.3.3节，刷新操作。

27.2.2 WDT Control Register (WDTCR)

Address(es): WDT.WDTCR 4004 4202h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	RPSS[1:0]		—	—	RPES[1:0]		CKS[3:0]				—	—	TOPS[1:0]	
Value after reset:	0	0	1	1	0	0	1	1	1	1	1	1	0	0	1	1

Bit	Symbol	Bit name	Description	R/W
b1, b0	TOPS[1:0]	Timeout Period Select	b1 b0 0 0: 1,024 cycles (03FFh) 0 1: 4,096 cycles (0FFFh) 1 0: 8,192 cycles (1FFFh) 1 1: 16,384 cycles (3FFFh).	R/W
b3, b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7 to b4	CKS[3:0]	Clock Division Ratio Select	b7 b4 0 0 0 1: PCLKB/4 0 1 0 0: PCLKB/64 1 1 1 1: PCLKB/128 0 1 1 0: PCLKB/512 0 1 1 1: PCLKB/2048 1 0 0 0: PCLKB/8192. Other settings are prohibited.	R/W
b9, b8	RPES[1:0]	Window End Position Select	b9 b8 0 0: 75% 0 1: 50% 1 0: 25% 1 1: 0% (do not specify window end position).	R/W
b11, b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b13, b12	RPSS[1:0]	Window Start Position Select	b13 b12 0 0: 25% 0 1: 50% 1 0: 75% 1 1: 100% (do not specify window start position).	R/W
b15, b14	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Some constraints apply to writes to the WDTCR register. For details, see section 27.3.2, Controlling Writes to the WDTCR, WDTRCR, and WDTCSTPR Registers.

In auto start mode, the settings in the WDTCR register are disabled, and the settings in Option Function Select Register 0 (OFS0) are enabled. The settings for the WDTCR register can also be made for the OFS0 register. For details, see section 27.3.7, Associations between Option Function Select Register 0 (OFS0) and WDT Registers.

TOPS[1:0] bits (Timeout Period Select)

The TOPS[1:0] bits select the timeout period, the period until the down-counter underflows, from 1,024, 4,096, 8,192, and 16,384 cycles, taking the divided clock specified in the CKS[3:0] bits as 1 cycle. After the down-counter is refreshed, the combination of the CKS[3:0] and TOPS[1:0] bits determines the number of PCLKB cycles until the counter underflows.

Table 27.2 lists the relationship between the CKS[3:0] and TOPS[1:0] bit settings, the timeout period, and the number of PCLKB cycles.

27.2.2 WDT控制寄存器(WDTCR)

Address(es): WDT.WDTCR 4004 4202h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	RPSS[1:0]		—	—	RPES[1:0]		CKS[3:0]				—	—	TOPS[1:0]	
重置后的值：	0	0	1	1	0	0	1	1	1	1	1	1	0	0	1	1

Bit	Symbol	位名称	Description	R/W
b1, b0	TOPS[1:0]	超时时间选择	b1 b0 0 0: 1,024 cycles (03FFh) 0 1: 4,096 cycles (0FFFh) 1 0: 8,192 cycles (1FFFh) 1 1: 16,384 cycles (3FFFh).	R/W
b3, b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b7 to b4	CKS[3:0]	时钟分频比选择	b7b40001:PCLKB40100:PCLKB641111:PCLKB1280110:PCLKB5120111:PCLKB20481000:PCLKB8192。禁止其他设置。	R/W
b9, b8	RPES[1:0]	窗口结束位置选择	b9b800：75%01：50%10：25%11：0%（不指定窗口结束位置）。	R/W
b11, b10	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b13, b12	RPSS[1:0]	窗口起始位置选择	b13b1200:25%01:50%10:75%11:100%（不指定窗口起始位置）。	R/W
b15, b14	—	Reserved	这些位被读取为0。写入值应为0。	R/W

一些限制适用于写入WDTCR寄存器。有关详细信息，请参阅第27.3.2节，控制对WDTCR、WDTRCR和WDTCSTPR寄存器。

在自动启动模式下，WDTCR寄存器中的设置被禁用，而选项功能选择寄存器0(OFS0)中的设置被启用。WDTCR寄存器的设置也可以对OFS0寄存器进行。有关详细信息，请参阅第27.3.7节，选项功能选择寄存器0(OFS0)和WDT寄存器之间的关联。

TOPS[1:0]位（超时周期选择）

TOPS[1:0]位从1 024、4 096、8 192和16 384个周期中选择超时周期，即递减计数器下溢之前的周期，将CKS[3:0]位中指定的分频时钟作为1个周期.向下计数器刷新后，CKS[3:0]和TOPS[1:0]位的组合决定了PCLKB周期数，直到计数器下溢。

表27.2列出了CKS[3:0]和TOPS[1:0]位设置、超时时间和
PCLKB cycles.

Table 27.2 Timeout period settings

CKS[3:0] bits				TOPS[1:0] bits		Clock division ratio	Timeout period (number of cycles)	PCLKB clock cycles
b7	b6	b5	b4	b1	b0			
0	0	0	1	0	0	PCLKB/4	1,024	4,096
				0	1		4,096	16,384
				1	0		8,192	32,768
				1	1		16,384	65,536
0	1	0	0	0	0	PCLKB/64	1,024	65,536
				0	1		4,096	262,144
				1	0		8,192	524,288
				1	1		16,384	1,048,576
1	1	1	1	0	0	PCLKB/128	1,024	131,072
				0	1		4,096	524,288
				1	0		8,192	1,048,576
				1	1		16,384	2,097,152
0	1	1	0	0	0	PCLKB/512	1,024	524,288
				0	1		4,096	2,097,152
				1	0		8,192	4,194,304
				1	1		16,384	8,388,608
0	1	1	1	0	0	PCLKB/2048	1,024	2,097,152
				0	1		4,096	8,388,608
				1	0		8,192	16,777,216
				1	1		16,384	33,554,432
1	0	0	0	0	0	PCLKB/8192	1,024	8,388,608
				0	1		4,096	33,554,432
				1	0		8,192	67,108,864
				1	1		16,384	134,217,728

CKS[3:0] bits (Clock Division Ratio Select)

The CKS[3:0] bits specify the division ratio of the clock used for the down-counter. The division ratio can be selected from the peripheral clock (PCLKB) divided by 4, 64, 128, 512, 2048, and 8192. Combined with the TOPS[1:0] bit setting, this allows the WDT to be configured to a count period between 4,096 and 134,217,728 cycles of the PCLKB clock.

RPES[1:0] bits (Window End Position Select)

The RPES[1:0] bits specify the window end position that indicates the refresh-permitted period. 75%, 50%, 25%, or 0% of the timeout period can be selected for the window end position. Set the window end position to a value less than the value for the window start position (window start position > window end position). If the window end position is greater than the window start position, only the window start position setting is enabled.

RPSS[1:0] bits (Window Start Position Select)

The RPSS[1:0] bits specify the window start position that indicates the refresh-permitted period. 100%, 75%, 50%, or 25% of the timeout period can be selected for the window start position. Set the window start position to a value greater than the value for the window end position. If the window start position is set to a value less than or equal to the window end position, the window end position is set to 0%.

Table 27.3 lists the counter values for the window start and end positions, and Figure 27.2 shows the refresh-permitted period set in the RPSS[1:0], RPES[1:0], and TOPS[1:0] bits.

Table 27.2 超时时间设置

CKS[3:0] bits				TOPS[1:0] bits		时钟分频比	超时时间（周期数）	PCLKB时钟周期
b7	b6	b5	b4	b1	b0			
0	0	0	1	0	0	PCLKB/4	1,024	4,096
				0	1		4,096	16,384
				1	0		8,192	32,768
				1	1		16,384	65,536
0	1	0	0	0	0	PCLKB/64	1,024	65,536
				0	1		4,096	262,144
				1	0		8,192	524,288
				1	1		16,384	1,048,576
1	1	1	1	0	0	PCLKB/128	1,024	131,072
				0	1		4,096	524,288
				1	0		8,192	1,048,576
				1	1		16,384	2,097,152
0	1	1	0	0	0	PCLKB/512	1,024	524,288
				0	1		4,096	2,097,152
				1	0		8,192	4,194,304
				1	1		16,384	8,388,608
0	1	1	1	0	0	PCLKB/2048	1,024	2,097,152
				0	1		4,096	8,388,608
				1	0		8,192	16,777,216
				1	1		16,384	33,554,432
1	0	0	0	0	0	PCLKB/8192	1,024	8,388,608
				0	1		4,096	33,554,432
				1	0		8,192	67,108,864
				1	1		16,384	134,217,728

CKS[3:0]位（时钟分频比选择）

CKS[3:0]位指定用于递减计数器的时钟的分频比。分频比可以从外设时钟(PCLKB)除以4、64、128、512、2048和8192中选择。结合TOPS[1:0]位设置，这允许将WDT配置为计数PCLKB时钟周期在4 096到134 217 728个周期之间。

RPES[1:0]位（窗口结束位置选择）

RPES[1:0]位指定指示刷新允许周期的窗口结束位置。可以为窗口结束位置选择75%、50%、25%或0%的超时时间。将窗口结束位置设置为小于窗口起始位置的值（窗口起始位置>窗口结束位置）。如果窗口结束位置大于窗口起始位置，则仅启用窗口起始位置设置。

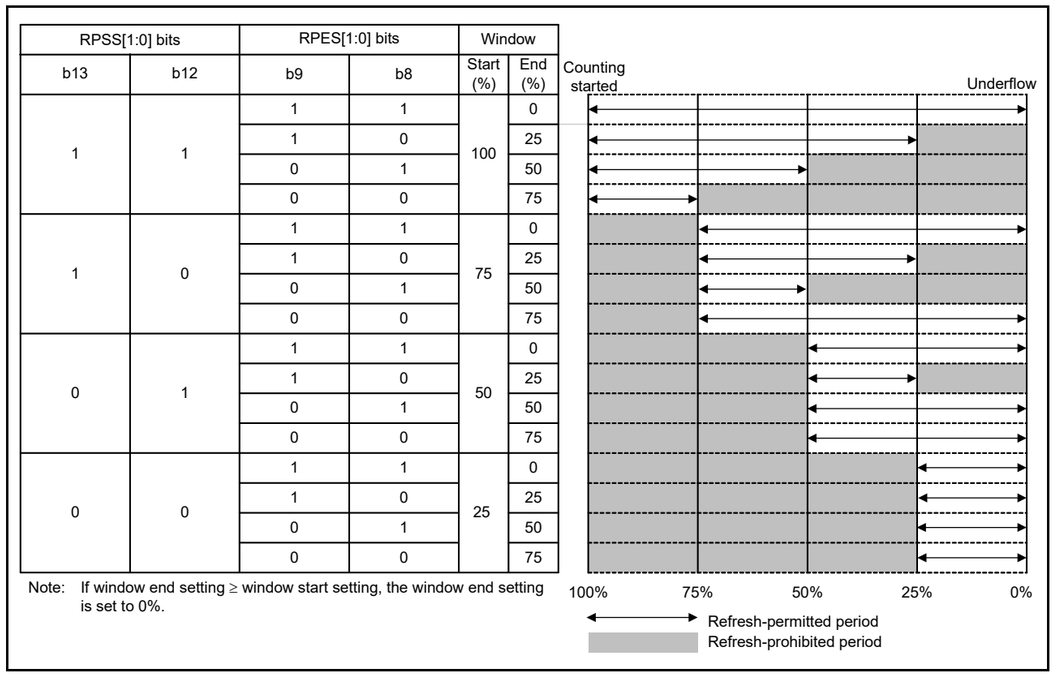
RPSS[1:0]位（窗口起始位置选择）

RPSS[1:0]位指定指示允许刷新周期的窗口起始位置。窗口起始位置可选择100%、75%、50%或25%的超时时间。将窗口开始位置设置为大于窗口结束位置的值。如果窗口开始位置设置为小于或等于窗口结束位置的值，则窗口结束位置设置为0%。

表27.3列出了窗口开始和结束位置的计数器值，图27.2显示了在RPSS[1:0]、RPES[1:0]和TOPS[1:0]位中设置的允许刷新周期。

Table 27.3 Relationship between the timeout period and window start and end counter values

TOPS[1:0] bits		Timeout period		Window start and end counter value			
		Cycles	Counter value	100%	75%	50%	25%
0	0	1024	03FFh	03FFh	02FFh	01FFh	00FFh
0	1	4096	0FFFh	0FFFh	0BFFh	07FFh	03FFh
1	0	8192	1FFFh	1FFFh	17FFh	0FFFh	07FFh
1	1	16384	3FFFh	3FFFh	2FFFh	1FFFh	0FFFh

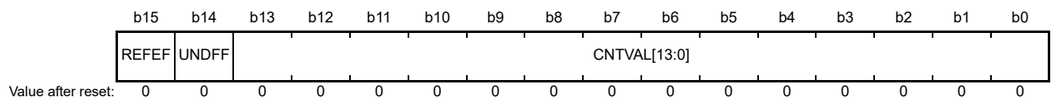


Note: If window end setting ≥ window start setting, the window end setting is set to 0%.

Figure 27.2 RPSS[1:0] and RPES[1:0] bit settings and refresh-permitted period

27.2.3 WDT Status Register (WDTSR)

Address(es): WDT.WDTSR 4004 4204h

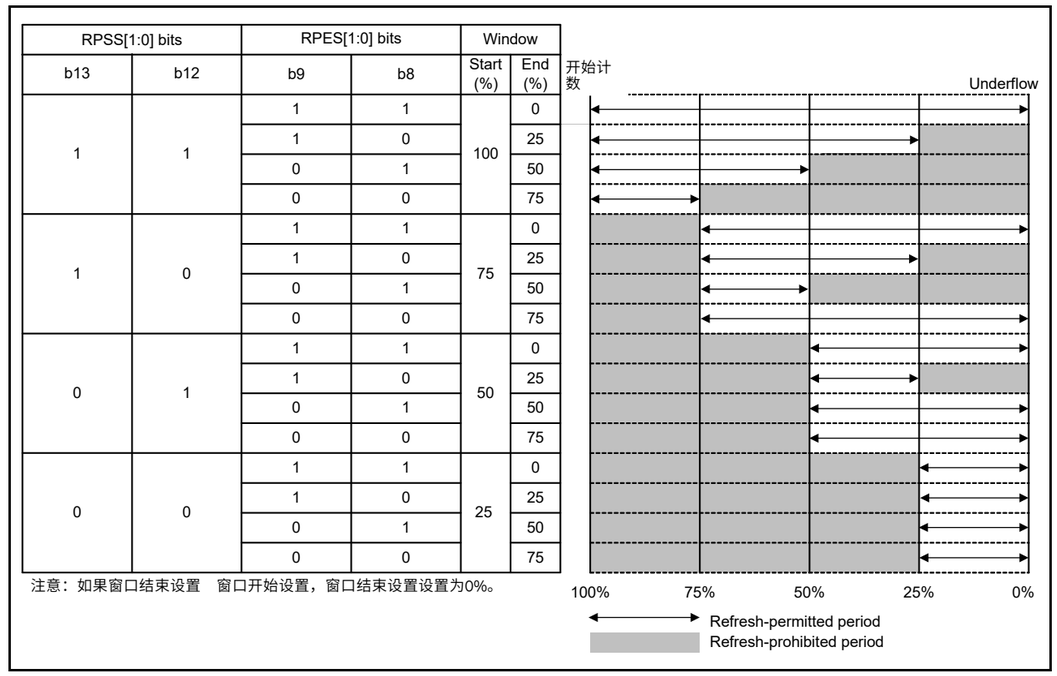


Bit	Symbol	Bit name	Description	R/W
b13 to b0	CNTVAL[13:0]	Down-Counter Value	Value counted by the down-counter	R
b14	UNDFF	Underflow Flag	0: No underflow occurred 1: Underflow occurred.	R(/W) *1
b15	REFEF	Refresh Error Flag	0: No refresh error occurred 1: Refresh error occurred.	R(/W) *1

Note 1. Only 0 can be written to clear the flag.

Table 27.3 超时时间与窗口开始和结束计数器值之间的关系

TOPS[1:0] bits		超时时间		窗口开始和结束计数器值			
		Cycles	计数器值	100%	75%	50%	25%
0	0	1024	03FFh	03FFh	02FFh	01FFh	00FFh
0	1	4096	0FFFh	0FFFh	0BFFh	07FFh	03FFh
1	0	8192	1FFFh	1FFFh	17FFh	0FFFh	07FFh
1	1	16384	3FFFh	3FFFh	2FFFh	1FFFh	0FFFh

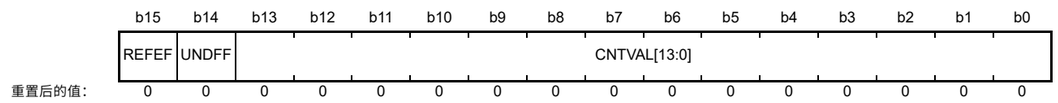


注意：如果窗口结束设置 窗口开始设置，窗口结束设置设置为0%。

Figure 27.2 RPSS[1:0]和RPES[1:0]位设置和允许刷新周期

27.2.3 WDT状态寄存器(WDTSR)

Address(es): WDT.WDTSR 4004 4204h



Bit	Symbol	位名称	Description	R/W
b13 to b0	CNTVAL[13:0]	Down-Counter Value	递减计数器计数的值	R
b14	UNDFF	Underflow Flag	0：未发生下溢1：发生下溢。	R(/W) *1
b15	REFEF	刷新错误标志	0：未发生刷新错误1：发生刷新错误。	R(/W) *1

Note 1. 只能写入0来清除标志。

CNTVAL[13:0] bits (Down-Counter Value)

Read the CNTVAL[13:0] bits to confirm the value of the down-counter. The read value might differ from the actual count by 1.

UNDFF flag (Underflow Flag)

Read the UNDFF flag to confirm whether an underflow occurred in the down-counter. A value of 1 indicates that the down-counter underflowed. Write 0 to the flag to set the value to 0. Writing 1 has no effect.

Clearing of the UNDFF flag takes (N+1) PCLKB cycles. In addition, clearing of the flag is ignored for (N+1) PCLKB cycles after an underflow. N is specified in the WDTCR.CKS[3:0] bits as follows:

- When WDTCR.CKS[3:0] = 0001b, N = 4
- When WDTCR.CKS[3:0] = 0100b, N = 64
- When WDTCR.CKS[3:0] = 1111b, N = 128
- When WDTCR.CKS[3:0] = 0110b, N = 512
- When WDTCR.CKS[3:0] = 0111b, N = 2048
- When WDTCR.CKS[3:0] = 1000b, N = 8192.

REFEF flag (Refresh Error Flag)

Read the REFEF flag to confirm whether a refresh error occurred, indicating that a refresh operation was performed during a prohibited period. A value of 1 indicates that a refresh error occurred. Write 0 to the flag to set the value to 0. Writing 1 has no effect.

Clearing of the REFEF flag takes (N+1) PCLKB cycles. In addition, clearing of the flag is ignored for (N+1) PCLKB cycles after a refresh error. N is specified in the WDTCR.CKS[3:0] bits as follows:

- When WDTCR.CKS[3:0] = 0001b, N = 4
- When WDTCR.CKS[3:0] = 0100b, N = 64
- When WDTCR.CKS[3:0] = 1111b, N = 128
- When WDTCR.CKS[3:0] = 0110b, N = 512
- When WDTCR.CKS[3:0] = 0111b, N = 2048
- When WDTCR.CKS[3:0] = 1000b, N = 8192

27.2.4 WDT Reset Control Register (WDTRCR)

Address(es): WDT.WDTRCR 4004 4206h

	b7	b6	b5	b4	b3	b2	b1	b0
	RSTIRQS	—	—	—	—	—	—	—
Value after reset:	1	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b6 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	RSTIRQS	Reset Interrupt Request Select	0: Non-maskable interrupt request or interrupt request output is enabled 1: Reset output is enabled.	R/W

Some constraints apply to writes to the WDTRCR register. For details, see section 27.3.2, Controlling Writes to the WDTCR, WDTRCR, and WDTCSTPR Registers.

In auto start mode, the WDTRCR register settings are disabled, and the settings in Option Function Select Register 0 (OFS0) are enabled. The settings for the WDTCR register can also be made for the OFS0 register. For details, see section

CNTVAL[13:0]位（递减计数器值）

读取CNTVAL[13:0]位以确认递减计数器的值。读取的值可能与实际计数相差1。

UNDFF flag (Underflow Flag)

读取UNDFF标志以确认递减计数器中是否发生下溢。值1表示递减计数器下溢。将0写入标志以将值设置为0。写入1无效。

清除UNDFF标志需要(N+1)个PCLKB周期。此外，在下溢后的(N+1)个PCLKB周期内忽略标志的清除。N在WDTCR.CKS[3:0]位中指定如下：

- When WDTCR.CKS[3:0] = 0001b, N = 4
- When WDTCR.CKS[3:0] = 0100b, N = 64
- When WDTCR.CKS[3:0] = 1111b, N = 128
- When WDTCR.CKS[3:0] = 0110b, N = 512
- When WDTCR.CKS[3:0] = 0111b, N = 2048
- When WDTCR.CKS[3:0] = 1000b, N = 8192.

REFEF标志（刷新错误标志）

读取REFEF标志，确认是否发生刷新错误，表示在禁止期间进行了刷新操作。值1表示发生了刷新错误。将0写入标志以将值设置为0。写入1无效。

清除REFEF标志需要(N+1)个PCLKB周期。此外，在刷新错误后的(N+1)个PCLKB周期内，标志的清除将被忽略。N在WDTCR.CKS[3:0]位中指定如下：

- When WDTCR.CKS[3:0] = 0001b, N = 4
- When WDTCR.CKS[3:0] = 0100b, N = 64
- When WDTCR.CKS[3:0] = 1111b, N = 128
- When WDTCR.CKS[3:0] = 0110b, N = 512
- When WDTCR.CKS[3:0] = 0111b, N = 2048
- When WDTCR.CKS[3:0] = 1000b, N = 8192

27.2.4 WDT复位控制寄存器(WDTRCR)

Address(es): WDT.WDTRCR 4004 4206h

	b7	b6	b5	b4	b3	b2	b1	b0
	RSTIRQS	—	—	—	—	—	—	—
重置后的值：	1	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b6 to b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b7	RSTIRQS	复位中断请求选择	0：使能不可屏蔽中断请求或中断请求输出1：使能复位输出。	R/W

一些限制适用于写入WDTRCR寄存器。有关详细信息，请参阅第27.3.2节，控制对WDTCR、WDTRCR和WDTCSTPR寄存器。

在自动启动模式下，WDTRCR寄存器设置被禁用，而选项功能选择寄存器0(OFS0)中的设置被启用。WDTCR寄存器的设置也可以对OFS0寄存器进行。有关详细信息，请参阅部分

27.3.7, Associations between Option Function Select Register 0 (OFS0) and WDT Registers.

27.2.5 WDT Count Stop Control Register (WDTCSTPR)

Address(es): WDT.WDTCSTPR 4004 4208h

	b7	b6	b5	b4	b3	b2	b1	b0
	SLCSTP	—	—	—	—	—	—	—
Value after reset:	1	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b6 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	SLCSTP	Sleep-Mode Count Stop Control	0: Count stop is disabled 1: Count is stopped when transition to Sleep mode.	R/W

The WDTCSTPR register controls whether to stop the WDT counter in a low power mode. Some constraints apply to writes to the WDTCSTPR register. For details, see section 27.3.2, Controlling Writes to the WDTCR, WDTRCR, and WDTCSTPR Registers.

In auto start mode, the WDTCSTPR register settings are disabled, and the settings in Option Function Select register 0 (OFS0) are enabled. The settings for the WDTCSTPR register can also be made for the OFS0 register. For details, see section 27.3.7, Associations between Option Function Select Register 0 (OFS0) and WDT Registers.

SLCSTP bit (Sleep-Mode Count Stop Control)

The SLCSTP bit selects whether to stop counting when transition to Sleep mode.

27.2.6 Option Function Select Register 0 (OFS0)

For information on the OFS0 register, see section 27.3.7, Associations between Option Function Select Register 0 (OFS0) and WDT Registers.

27.3 Operation

27.3.1 Count Operation in Each Start Mode

The WDT has two start modes:

- Auto start mode, in which counting automatically starts after a release from the reset state
- Register start mode, in which counting is started with a refresh by writing to the register.

In auto start mode, counting automatically starts after release from the reset state in accordance with the settings in Option Function Select Register 0 (OFS0) in the flash.

In register start mode, counting starts with a refresh by writing to the register after the respective registers are set after a release from the reset state.

Select auto start mode or register start mode by setting the WDT Start Mode Select bit (OFS0.WDTSTRT) in the OFS0 register. When the auto start mode is selected, the settings in the WDT Control Register (WDTCR), WDT Reset Control Register (WDTRCR), and WDT Count Stop Control Register (WDTCSTPR) are disabled, and the settings in the OFS0 register are enabled. When the register start mode is selected, the OFS0 register settings are disabled, and the settings in the WDT Control Register (WDTCR), WDT Reset Control Register (WDTRCR), and WDT Count Stop Control Register (WDTCSTPR) are enabled.

27.3.1.1 Register start mode

When the WDT Start Mode Select bit (OFS0.WDTSTRT) is 1, register start mode is selected and the WDT Control Register (WDTCR), WDT Reset Control Register (WDTRCR), and WDT Count Stop Control Register (WDTCSTPR) are enabled.

27.3.7，选项功能选择寄存器0(OFS0)和WDT寄存器之间的关联。

27.2.5 WDT计数停止控制寄存器(WDTCSTPR)

Address(es): WDT.WDTCSTPR 4004 4208h

	b7	b6	b5	b4	b3	b2	b1	b0
	SLCSTP	—	—	—	—	—	—	—
重置后的值：	1	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b6 to b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b7	SLCSTP	睡眠模式计数停止控制	0：禁止计数停止1：转换到睡眠模式时停止计数。	R/W

WDTCSTPR寄存器控制是否在低功耗模式下停止WDT计数器。一些限制适用于写入WDTCSTPR寄存器。有关详细信息，请参见第27.3.2节，控制对WDTCR、WDTRCR和WDTCSTPR寄存器的写入。

在自动启动模式下，WDTCSTPR寄存器设置被禁用，而选项功能选择寄存器0(OFS0)中的设置被启用。也可以对OFS0寄存器进行WDTCSTPR寄存器的设置。有关详细信息，请参阅第27.3.7节，选项功能选择寄存器0(OFS0)和WDT寄存器之间的关联。

SLCSTP位（休眠模式计数停止控制）

SLCSTP位选择在转换到休眠模式时是否停止计数。

27.2.6 选项功能选择寄存器0(OFS0)

有关OFS0寄存器的信息，请参见第27.3.7节，选项功能选择寄存器0(OFS0)和WDT寄存器之间的关联。

27.3 Operation

27.3.1 每种启动模式下的计数操作

WDT有两种启动模式：

- 自动启动模式，从复位状态释放后自动开始计数
- 寄存器启动模式，在这种模式下，通过写入寄存器来启动计数。

在自动启动模式下，从复位状态释放后，按照
选项功能选择闪存中的寄存器0(OFS0)。

在寄存器启动模式中，在从复位状态释放后，在设置各个寄存器后，通过写入寄存器来开始计数。

通过设置OFS0寄存器中的WDT启动模式选择位(OFS0.WDTSTRT)来选择自动启动模式或寄存器启动模式。选择自动启动模式后，WDT控制寄存器（WDTCR）中的设置，WDTRESET控制寄存器（WDTRCR）和WDT计数停止控制寄存器（WDTCSTPR）被禁用，并启用OFS0寄存器中的设置。选择寄存器启动模式后，禁用了OFS0寄存器设置，并在WDT控制寄存器（WDTCR）中的设置，WDTRESETCONTROL寄存器（WDTRCR）和WDTCountCountStopControl寄存器（WDTCSTPR）启用。

27.3.1.1 注册启动模式

当WDT启动模式选择位(OFS0.WDTSTRT)为1时，选择寄存器启动模式并且WDT控制
使能寄存器(WDTCR)、WDT复位控制寄存器(WDTRCR)和WDT计数停止控制寄存器(WDTCSTPR)。

After the reset state is released, set the following to Sleep mode in the WDTCSTPR register:

- Clock division ratio
- Window start and end positions
- Timeout period in the WDTCR register
- Reset output or interrupt request output in the WDTRCR register
- Counter stop control during transitions to Sleep mode in the WDTCSTPR register.

Refresh the down-counter to start counting down from the value set in the Timeout Period Select bits (WDTCR.TOPS[1:0]).

Thereafter, as long as the counter is refreshed in the refresh-permitted period, the value in the counter is reset each time the counter is refreshed and down-counting continues. The WDT does not output the reset signal as long as counting continues. However, if the down-counter underflows because the down-counter cannot be refreshed due to a program runaway, or if a refresh error occurs because the counter was refreshed outside the refresh-permitted period, the WDT outputs a reset signal or a non-maskable interrupt request/interrupt request (WDT_NMIUNDF). Reset output or interrupt request output can be selected in the WDT Reset Interrupt Request Select bit (WDTRCR.RSTIRQS). Non-maskable interrupt request or interrupt request can be selected in the WDT Underflow/Refresh Error Interrupt Enable bit (NMIER.WDTEN).

Figure 27.3 shows an example of operation under the following conditions:

- Register start mode (OFS0.WDTSTRT = 1)
- Reset output is enabled (WDTRCR.RSTIRQS = 1)
- The window start position is 75% (WDTCR.RPSS[1:0] = 10b)
- The window end position is 25% (WDTCR.RPES[1:0] = 10b).

释放复位状态后，在WDTCSTPR寄存器中将以下内容设置为休眠模式：

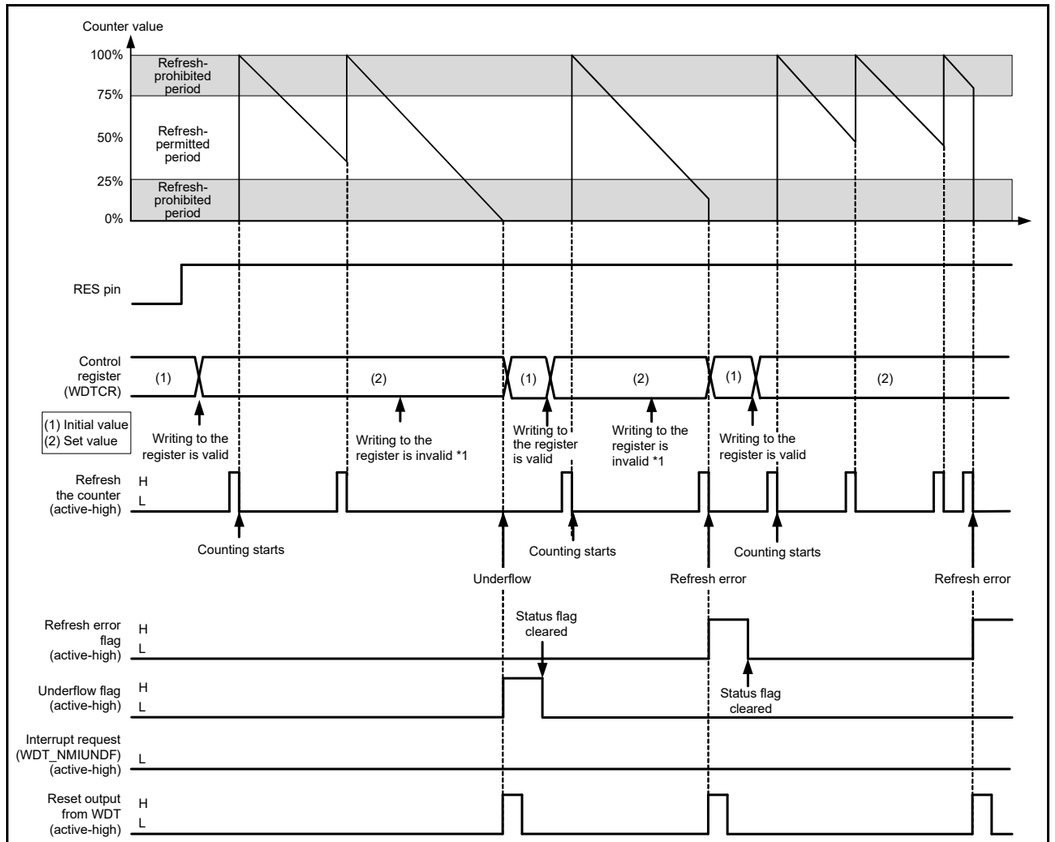
- 时钟分频比
- 窗口开始和结束位置
- WDTCR寄存器中的超时时间
- WDTRCR寄存器中的复位输出或中断请求输出
- 在WDTCSTPR寄存器中转换到休眠模式期间的计数器停止控制。

刷新递减计数器以从超时周期选择位(WDTCR.TOPS[1:0])中设置的值开始递减计数。

此后，只要在可刷新期间刷新计数器，每次刷新计数器时计数器中的值都会被重置，并继续递减计数。只要继续计数，WDT就不会输出复位信号。但是，如果由于程序失控导致递减计数器无法刷新而导致递减计数器下溢，或者由于计数器在刷新允许时间之外刷新而发生刷新错误，则WDT输出复位信号或非可屏蔽中断请求中断请求(WDT_NMIUNDF)。可以在WDT复位中断请求选择位(WDTRCR.RSTIRQS)中选择复位输出或中断请求输出。可以在WDT下溢刷新错误中断　　允许位(NMIER.WDTEN)中选择不可屏蔽的中断请求或中断请求。

图27.3显示了以下条件下的操作示例：

- 寄存器启动模式（OFS0.WDTSTRT=1）
- 使能复位输出(WDTRCR.RSTIRQS=1)
- 窗口起始位置为75%(WDTCR.RPSS[1:0]=10b)
- 窗口结束位置为25%(WDTCR.RPES[1:0]=10b)。



Note 1. See section 27.3.2, Controlling Writes to the WDTCR, WDTRCR, and WDTCSTPR Registers.

Figure 27.3 Operation example in register start mode

27.3.1.2 Auto start mode

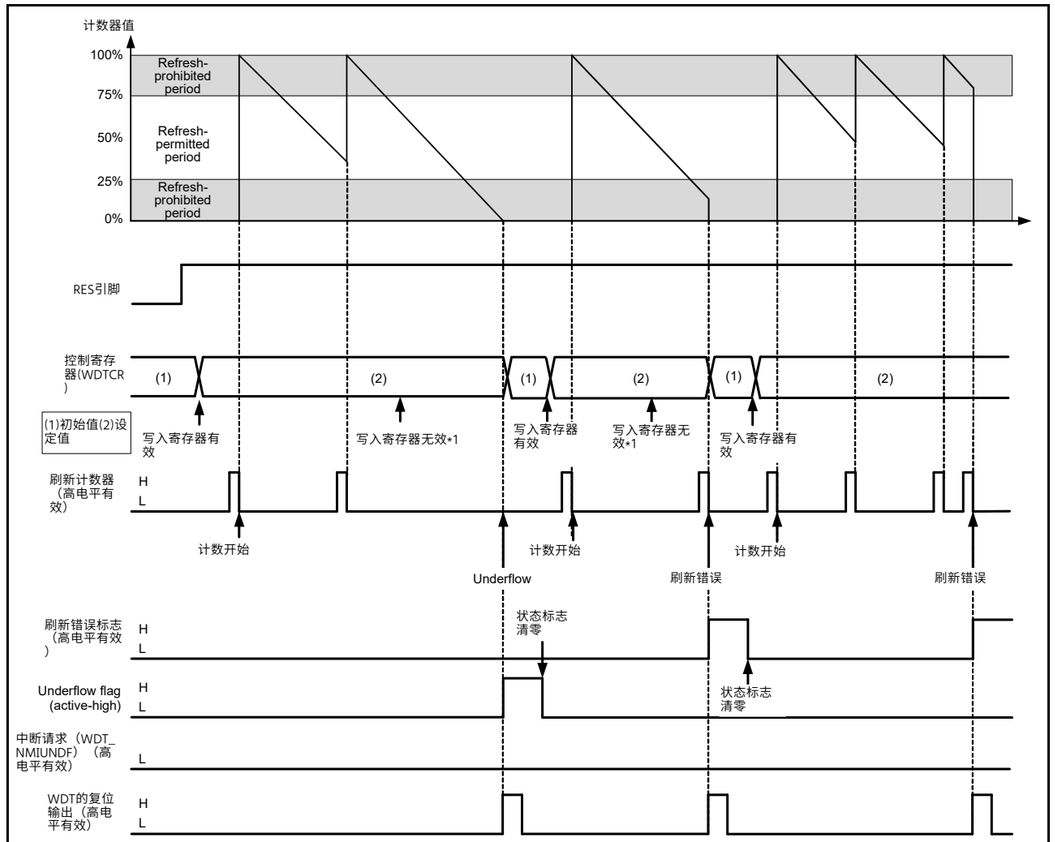
When the WDT Start Mode Select bit (OFS0.WDTSTRT) in the Option Function Select Register 0 (OFS0) is 0, auto start mode is selected. The WDT Control Register (WDTCR), WDT Reset Control Register (WDTRCR), and WDT Count Stop Control Register (WDTCSTPR) are disabled while the settings in the OFS0 register are enabled.

Within the reset state, the following values in Option Function Select register 0 (OFS0) are set in the WDT registers:

- Clock division ratio
- Window start and end positions
- Timeout period
- Reset output or interrupt request
- Counter stop control on transition to Sleep mode.

When the reset state is released, the down-counter automatically starts counting down from the value set in the WDT Timeout Period Select bits (OFS0.WDTTOPS[1:0]).

Thereafter, as long as the counter is refreshed in the refresh-permitted period, the value in the counter is reset each time the counter is refreshed and down-counting continues. The WDT does not output the reset signal as long as the counting continues. However, if the down-counter underflows because refreshing of the down-counter is not possible due to a runaway program or if a refresh error occurs due to refreshing outside the refresh-permitted period, the WDT asserts the



注1.请参见第27.3.2节，控制对WDTCR、WDTRCR和WDTCSTPR寄存器的写入。

Figure 27.3 寄存器启动模式下的操作示例

27.3.1.2 自动启动模式

当WDT启动模式选择位置（OFS0.WDTSTRT）中的选项功能选择寄存器0（OFS0）为0时，选择了自动启动模式。WDT控制寄存器(WDTCR)、WDT复位控制寄存器(WDTRCR)和WDT计数停止控制寄存器(WDTCSTPR)被禁用，而OFS0寄存器中的设置被启用。

在复位状态下，选项功能选择寄存器0(OFS0)中的以下值在WDT寄存器中设置：

- 时钟分频比
- 窗口开始和结束位置
- 超时时间
- 复位输出或中断请求
- 转换到睡眠模式时的计数器停止控制。

当复位状态解除时，递减计数器自动从WDT中设置的值开始递减计数
超时周期选择位(OFS0.WDTTOPS[1:0])。

此后，只要在可刷新期间刷新计数器，每次刷新计数器时计数器中的值都会被重置，并继续递减计数。只要继续计数，WDT就不会输出复位信号。但是，如果由于程序失控而无法刷新递减计数器导致递减计数器下溢，或者由于刷新允许刷新时间之外的刷新而发生刷新错误，则WDT断言

reset signal or non-maskable interrupt request/interrupt request (WDT_NMIUNDF).

After the reset signal or non-maskable interrupt request/interrupt request is generated, the counter reloads the timeout period after counting for 1 cycle. The value of the timeout period is set in the down-counter and counting restarts.

Reset output or interrupt request output can be selected in the WDT Reset Interrupt Request Select bit (OFS0.WDTRSTIRQS). Non-maskable interrupt request or interrupt request can be selected in the WDT Underflow/Refresh Error Interrupt Enable bit (NMIER.WDTEN).

Figure 27.4 shows an example of operation (non-maskable interrupt) under the following conditions:

- Auto start mode (OFS0.WDTSTRT = 0)
- Non-maskable interrupt request output is enabled (OFS0.WDTRSTIRQS = 0)
- The window start position is 75% (WDTCR.RPSS[1:0] = 10b)
- The window end position is 25% (WDTCR.RPES[1:0] = 10b).

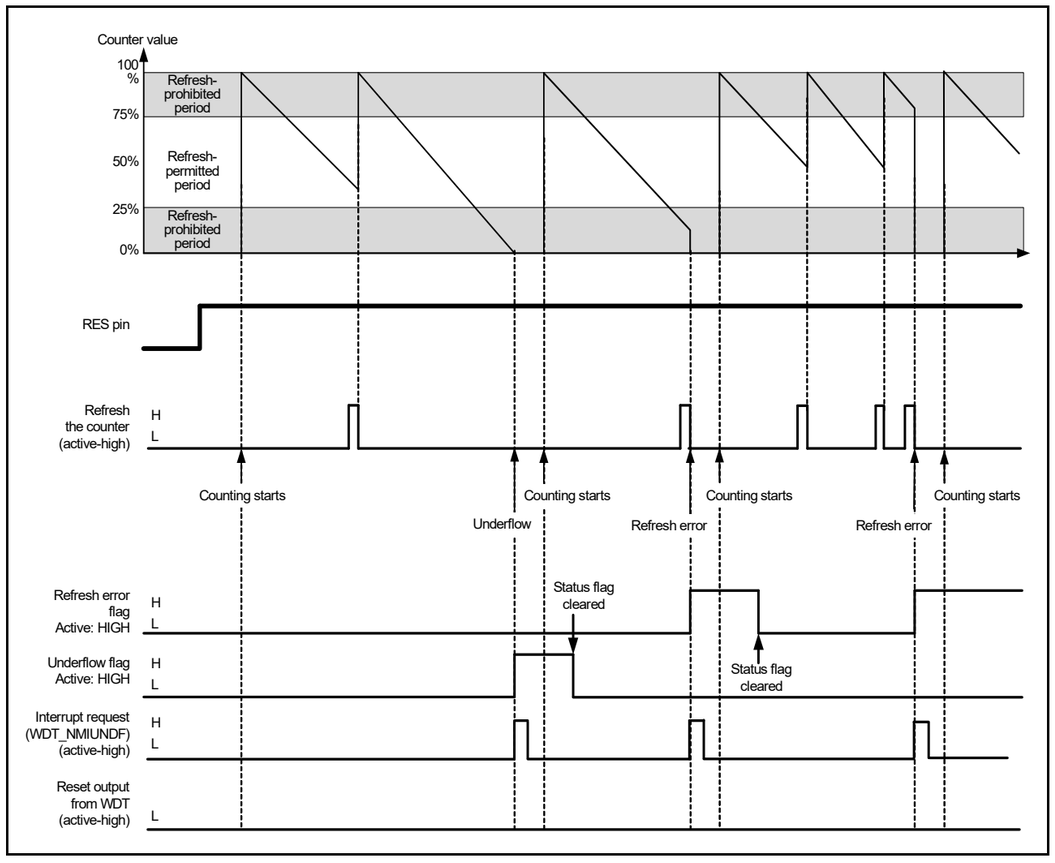


Figure 27.4 Operation example in auto start mode

27.3.2 Controlling Writes to the WDTCR, WDTRCR, and WDTCSTPR Registers

Writing to the WDT Control Register (WDTCR), WDT Reset Control Register (WDTRCR), or WDT Count Stop Control Register (WDTCSTPR) is possible once between the release from the reset state and the first refresh operation.

After a refresh (counting starts) or a write to WDTCR, WDTRCR or WDTCSTPR, the protection signal in the WDT becomes 1 to protect WDTCR, WDTRCR and WDTCSTPR against subsequent write attempts. This protection is released by the reset source of the WDT. With other reset sources, the protection is not released.

复位信号或不可屏蔽中断请求中断请求(WDT_NMIUNDF)。

复位信号或不可屏蔽中断请求中断请求产生后，计数器在计数1个周期后重新加载超时周期。超时时间的值在递减计数器中设置并重新开始计数。

可以在WDT复位中断请求选择位(OFS0.WDTRSTIRQS)中选择复位输出或中断请求输出。可以在WDT下溢刷新错误中断　　允许位(NMIER.WDTEN)中选择不可屏蔽的中断请求或中断请求。

图27.4显示了以下条件下的操作示例（不可屏蔽中断）：

- 自动启动模式（OFS0.WDTSTRT=0）
- 使能不可屏蔽中断请求输出(OFS0.WDTRSTIRQS=0)
- 窗口起始位置为75%(WDTCR.RPSS[1:0]=10b)
- 窗口结束位置为25%(WDTCR.RPES[1:0]=10b)。

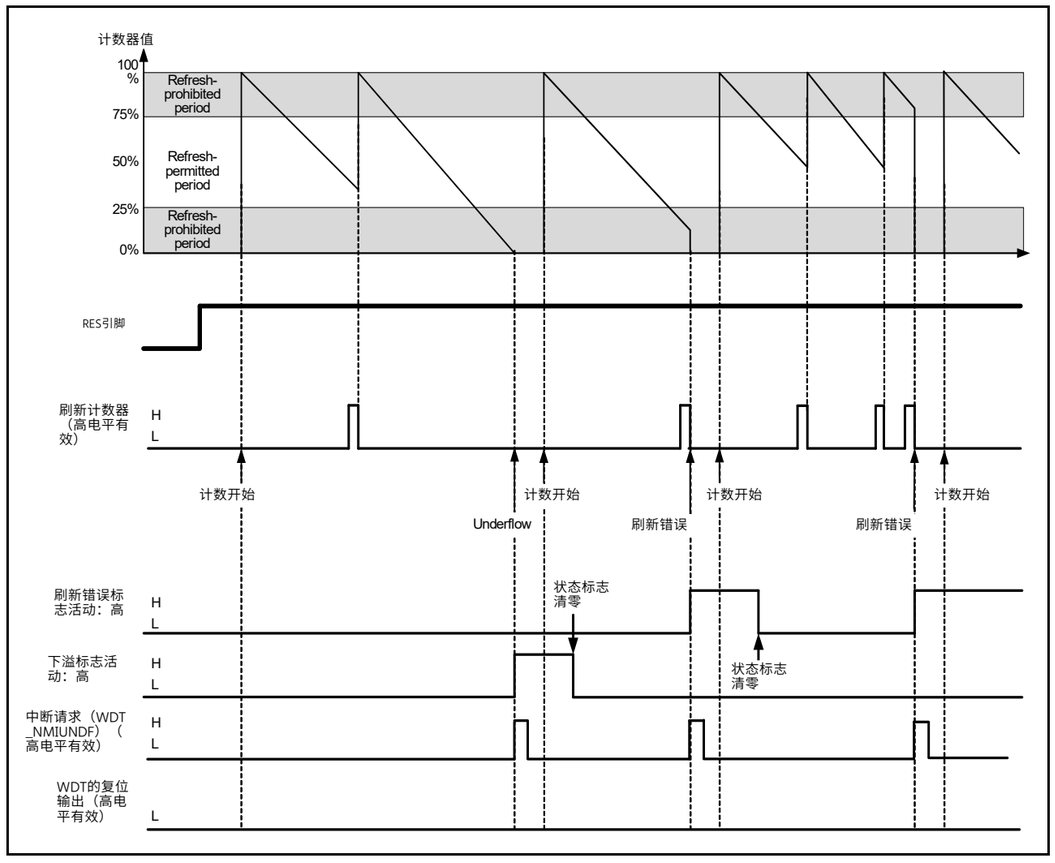


Figure 27.4 自动启动模式下的操作示例

27.3.2 控制对WDTCR、WDTRCR和WDTCSTPR寄存器的写入

写入WDT控制寄存器(WDTCR)、WDT复位控制寄存器(WDTRCR)或WDT计数停止控制寄存器(WDTCSTPR)在从复位状态释放到第一次刷新操作之间是可能的。

在刷新（计数开始）或写入WDTCR、WDTRCR或WDTCSTPR后，WDT中的保护信号变为1，以保护WDTCR、WDTRCR和WDTCSTPR免受后续写入尝试。该保护由WDT的复位源解除。使用其他复位源时，不会解除保护。

Figure 27.5 shows control waveforms produced in response to writing to the WDTCR.

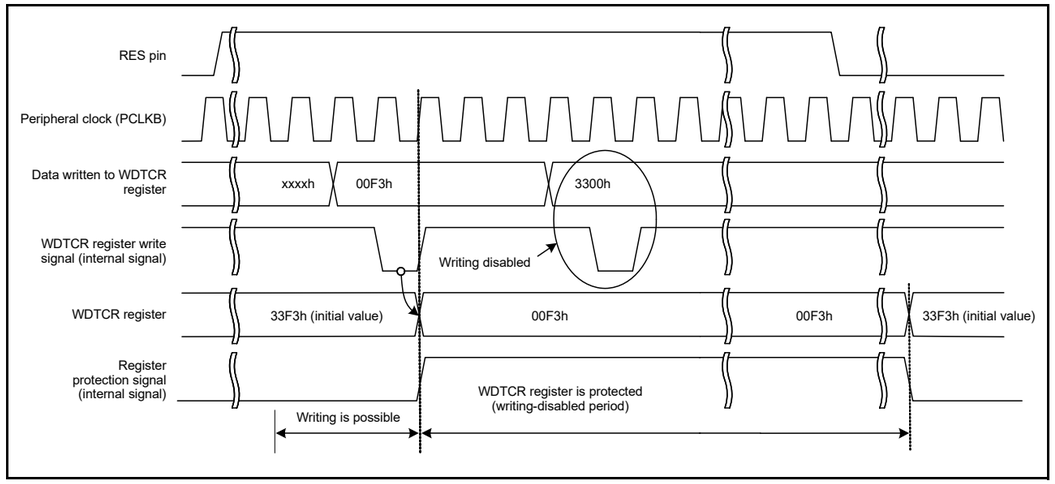


Figure 27.5 Control waveforms produced in response to writes to the WDTCR register

27.3.3 Refresh Operation

The down-counter is refreshed by writing the values 00h and FFh to the WDT Refresh Register (WDTRR). If a value other than FFh is written after 00h, the down-counter is not refreshed. After an invalid value is written, correct refreshing resumes by writing 00h and FFh to the WDTRR register.

When a register other than WDTRR is accessed or WDTRR is read between writing 00h and writing FFh to WDTRR, correct refreshing is performed.

Writing to refresh the counter must be performed within the refresh-permitted period and whether this is done is determined by writing FFh. For this reason, correct refreshing is performed even when 00h is written outside the refresh-permitted period.

[Example write sequences that are valid for refreshing the counter]

- 00h → FFh
- 00h (n-1th time) → 00h (nth time) → FFh
- 00h → access to another register or read from WDTRR → FFh.

[Example write sequences that are invalid for refreshing the counter]

- 23h (a value other than 00h) → FFh
- 00h → 54h (a value other than FFh)
- 00h→ AAh (00h and a value other than FFh) → FFh.

After FFh is written to the WDT Refresh Register (WDTRR), refreshing the down-counter requires up to 4 cycles of the signal for counting. To meet this requirement, complete writing FFh to WDTRR 4 count cycles before the down-counter underflows.

Figure 27.6 shows the WDT refresh-operation waveforms when the clock division ratio = PCLKB/64.

图27.5显示了响应写入WDTCR产生的控制波形。

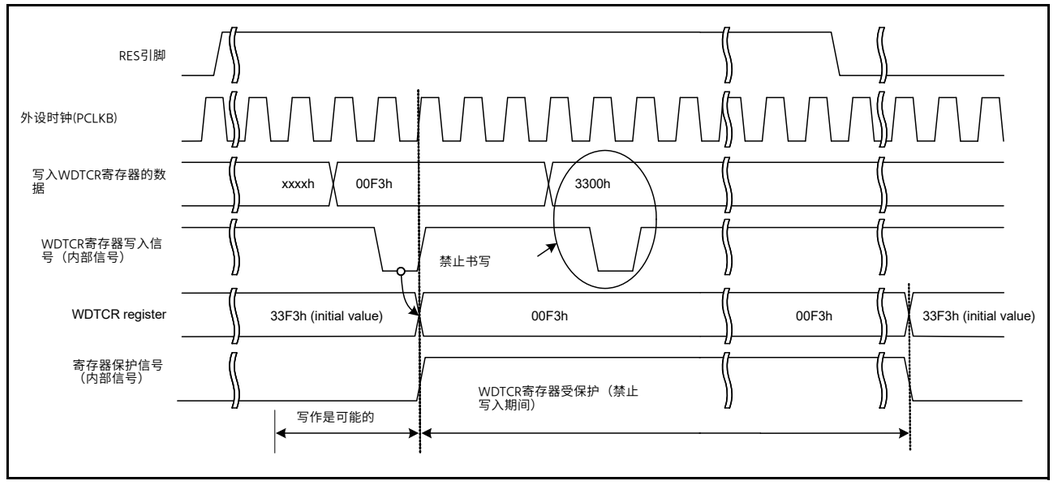


Figure 27.5 响应写入WDTCR寄存器而产生的控制波形

27.3.3 刷新操作

通过将值00h和FFh写入WDT刷新寄存器(WDTRR)来刷新递减计数器。如果在00h之后写入FFh以外的值，则不刷新递减计数器。写入无效值后，通过将00h和FFh写入WDTRR寄存器来恢复正确刷新。

在写入00h到写入FFh到WDTRR之间访问WDTRR以外的寄存器或读取WDTRR时，执行正确的刷新。

刷新计数器的写入必须在允许刷新的周期内执行，是否执行由写入FFh确定。因此，即使在允许刷新期间之外写入00h，也会执行正确的刷新。

[对刷新计数器有效的示例写入序列]

- 00h → FFh
- 00h (n-1th time) → 00h (nth time) → FFh
- 00h→访问另一个寄存器或从WDTRR→FFh读取。

[对刷新计数器无效的示例写入序列]

- 23h（00h以外的值）→FFh
- 00h→54h（FFh以外的值）
- 00h→AAh（00h和FFh以外的值）→FFh。

将FFh写入WDT刷新寄存器(WDTRR)后，刷新递减计数器最多需要4个信号周期进行计数。为满足此要求，请在递减计数器下溢之前的4个计数周期内将FFh写入WDTRR。

图27.6显示了时钟分频比=PCLKB64时的WDT刷新操作波形。

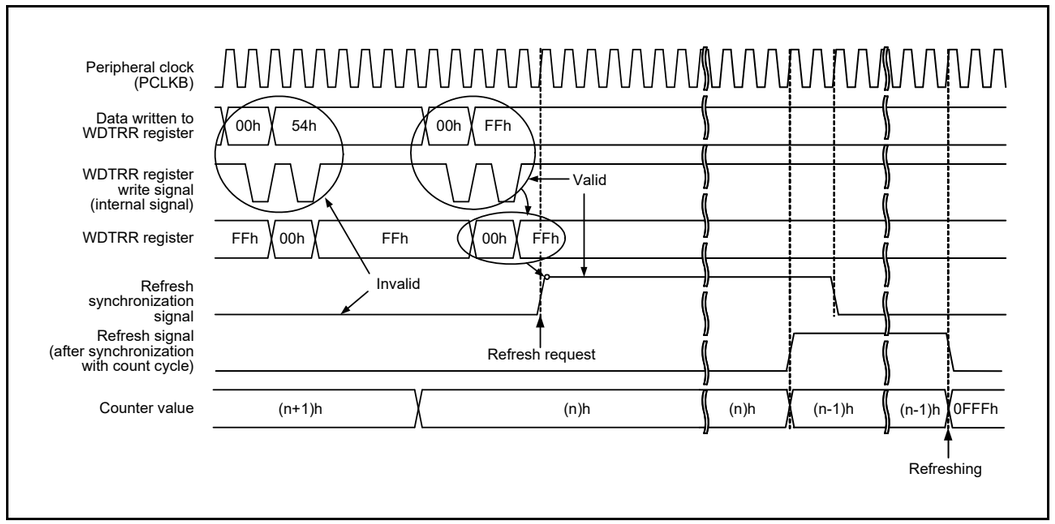


Figure 27.6 WDT refresh operation waveforms when WDTCR.CKS[3:0] = 0100b and WDTCR.TOPS[1:0] = 01b

27.3.4 Reset Output

When the Reset Interrupt Request Select bit (WDTRCR.RSTIRQS) is set to 1 in register start mode, or when the WDT Reset Interrupt Request Select bit (OFS0.WDTRSTIRQS) in the Option Function Select Register 0 (OFS0) is set to 1 in auto start mode, a reset signal is output for 1 cycle count when an underflow in the down-counter or a refresh error occurs.

In register start mode, the down-counter is initialized (all bits set to 0) and stopped in that state after output of a reset signal. After the reset state is released and the program is restarted, the counter is set up and counting down starts again with a refresh. In auto start mode, counting down starts automatically after the reset state is released.

27.3.5 Interrupt Sources

When the Reset Interrupt Request Select bit (WDTRCR.RSTIRQS) is set to 0 in register start mode or when the WDT Reset Interrupt Request Select bit (OFS0.WDTRSTIRQS) in Option Function Select Register 0 (OFS0) is set to 0 in auto start mode, an interrupt signal (WDT_NMIUNDF) is generated when an underflow in the counter or a refresh error occurs. This interrupt can be used as a non-maskable interrupt or an interrupt. For details, see section 14, Interrupt Controller Unit (ICU).

Table 27.4 WDT interrupt sources

Name	Interrupt source	DTC activation	DMAC activation
WDT_NMIUNDF	• Down-counter underflow • Refresh error	Not possible	Not possible

27.3.6 Reading the Down-Counter Value

The WDT stores the counter value in the down-counter value bits (WDTSR.CNTVAL[13:0]) of the WDT Status Register. Check these bits to obtain the counter value.

Figure 27.7 shows the processing for reading the WDT down-counter value when the clock division ratio = PCLKB/64.

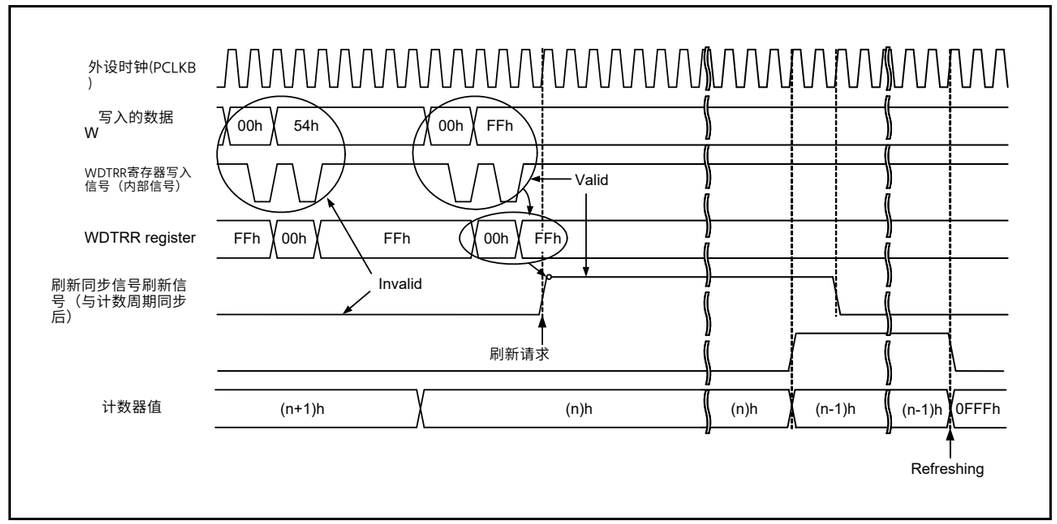


Figure 27.6 WDTCR.CKS[3:0]=0100b和WDTCR.TOPS[1:0]=01b时的WDT刷新操作波形

27.3.4 复位输出

当重置中断请求选择位（wdtrcr.rstirqs）在寄存器开始模式下设置为1，或者在wdtrepreptinterrupt请求中选择位（ofs0.wdtrstirqs）在选项函数函数选择寄存器0（OFS0）中设置为1in在自动启动模式下，当递减计数器下溢或发生刷新错误时，会在1个周期计数内输出复位信号。

在寄存器启动模式下，递减计数器被初始化（所有位设置为0）并在输出复位信号后停止在该状态。复位状态解除并重新启动程序后，计数器设置并通过刷新重新开始倒计时。在自动启动模式下，复位状态解除后自动开始倒计时。

27.3.5 中断源

当在寄存器启动模式下复位中断请求选择位(WDTRCR.RSTIRQS)设置为0或WDT
选项功能选择寄存器0(OFS0)中的复位中断请求选择位(OFS0.WDTRSTIRQS)在自动启动模式下设置为0，当计数器下溢或发生刷新错误时会产生中断信号(WDT_NMIUNDF)。此中断可用作不可屏蔽中断或中断。有关详细信息，请参阅第14节，中断控制器单元(ICU)。

Table 27.4 WDT中断源

Name	中断源	DTC activation	DMAC activation
WDT_NMIUNDF	递减计数器下溢 刷新错误	不可能	不可能

27.3.6 读取递减计数器值

WDT将计数器值存储在WDT状态的递减计数器值位(WDTSR.CNTVAL[13:0])中
登记。检查这些位以获得计数器值。

图27.7显示了在时钟分频比=PCLKB64时读取WDT递减计数器值的过程。

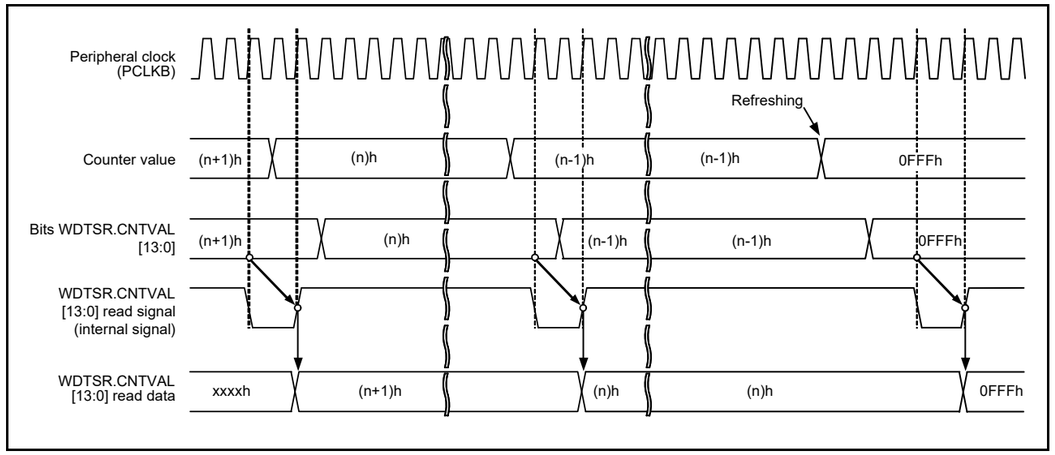


Figure 27.7 Processing for reading WDT down-counter value when WDTCR.CKS[3:0] = 0100b and WDTCR.TOPS[1:0] = 01b

27.3.7 Associations between Option Function Select Register 0 (OFS0) and WDT Registers

Table 27.5 lists the associations between Option Function Select register 0 (OFS0), used in auto start mode, and the registers used in register start mode. Do not change the OFS0 register settings during WDT operation. For details on Option Function Select register 0 (OFS0), see section 7, Option Function Select Register 0 (OFS0).

Table 27.5 Association between Option Function Select register 0 (OFS0) and the WDT registers

Control target	Function	OFS0 register (enabled in auto start mode) OFS0.WDTSTRT = 0	WDT registers (enabled in register start mode) OFS0.WDTSTRT = 1
Down-counter	Timeout period select	OFS0.WDTTOPS[1:0]	WDTCR.TOPS[1:0]
	Clock division ratio select	OFS0.WDTCKS[3:0]	WDTCR.CKS[3:0]
	Window start position select	OFS0.WDTRPSS[1:0]	WDTCR.RPSS[1:0]
	Window end position select	OFS0.WDTRPES[1:0]	WDTCR.RPES[1:0]
Reset output or interrupt request output	Reset output or interrupt request output select	OFS0.WDTRSTIRQS	WDTRCR.RSTIRQS
Count stop	Sleep-mode count stop control	OFS0.WDTSTPCTL	WDTCSTPR.SLCSTP

27.4 Link Operation by ELC

The WDT is capable of a link operation for the previously specified module when interrupt request signal is used as an event signal by the ELC. The event signal is output by the counter underflow or refresh error.

An event signal is output regardless of the setting in the WDTRCR.RSTIRQS bit in register start mode or the OFS0.WDTRSTIRQS bit in auto start mode. An event signal can also be output when the next interrupt source is generated while the Refresh Error Flag (WDTSR.REFEF) or Underflow Flag (WDTSR.UNDFF) is 1. For details, see section 19, Event Link Controller (ELC).

27.5 Usage Notes

27.5.1 Restrictions on the ICU Event Link Setting Register n (IELSRn) Setting

Setting 47h to the ICU Event Link Setting Register n (IELSRn.IELS[8:0] bits) is prohibited when enabling the WDT reset assertion (OFS0.WDTRSTIRQS = 1 or WDTRCR.RSTIRQS = 1) or when enabling the event link operation (47h is set to ELSRm.ELS[8:0]).

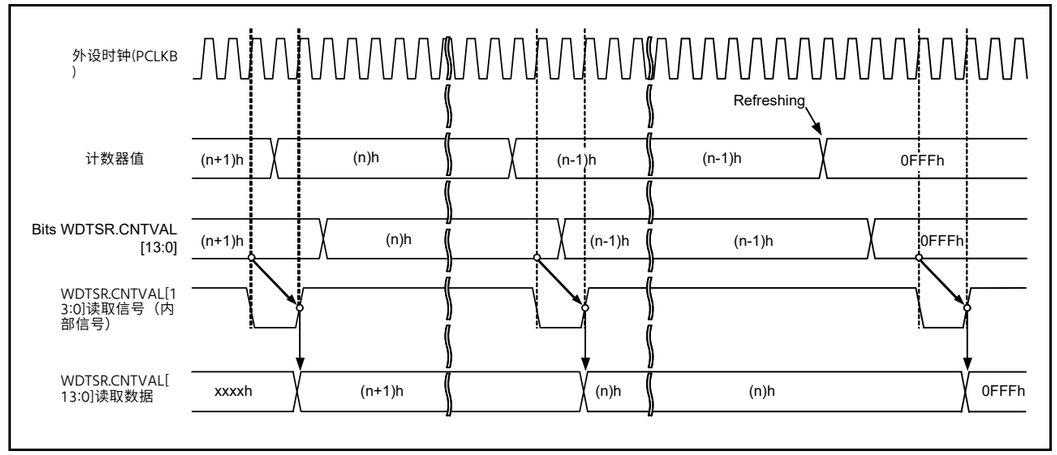


Figure 27.7 当WDTCR.CKS[3:0]=0100b和WDTCR.TOPS[1:0] = 01b

27.3.7 选项功能选择寄存器0(OFS0)和WDT之间的关联Registers

表27.5列出了用于自动启动模式的选项功能选择寄存器0(OFS0)和用于寄存器启动模式的寄存器之间的关联。请勿在WDT操作期间更改OFS0寄存器设置。有关选项功能选择寄存器0(OFS0)的详细信息，请参见第7节，选项功能选择寄存器0(OFS0)。

Table 27.5 选项功能选择寄存器0(OFS0)和WDT寄存器之间的关联

控制目标	Function	OFS0寄存器（在自动启动模式下启用）OFS0.WDTSTRT=0	WDT寄存器（在寄存器启动模式下启用）OFS0.WDTSTRT=1
Down-counter	超时时间选择	OFS0.WDTTOPS[1:0]	WDTCR.TOPS[1:0]
	时钟分频比选择	OFS0.WDTCKS[3:0]	WDTCR.CKS[3:0]
	窗口起始位置选择	OFS0.WDTRPSS[1:0]	WDTCR.RPSS[1:0]
	窗口结束位置选择	OFS0.WDTRPES[1:0]	WDTCR.RPES[1:0]
复位输出或中断请求输出	复位输出或中断请求输出选择	OFS0.WDTRSTIRQS	WDTCR.RSTIRQS
计数停止	睡眠模式计数停止控制	OFS0.WDTSTPCTL	WDTCSTPR.SLCSTP

27.4 ELC的链接操作

当ELC将中断请求信号用作事件信号时，WDT能够对先前指定的模块进行链接操作。事件信号由计数器下溢或刷新错误输出。

无论寄存器启动模式下的WDTRCR.RSTIRQS位的设置如何，都会输出事件信号。
自动启动模式下的OFS0.WDTRSTIRQS位。当刷新错误标志(WDTSR.REFEF)或下溢标志(WDTSR.UNDFF)为1时，也可以在产生下一个中断源时输出事件信号。有关详细信息，请参阅第19节，事件链接控制器(ELC)。

27.5 使用说明

27.5.1 ICU事件链接设置寄存器n(IELSRn)设置的限制

当启用WDT复位断言（OFS0.WDTRSTIRQS=1或WDTRCR.RSTIRQS=1）或启用事件链接操作（47h设置为ELSRm.ELS[8:0]）。

28. Independent Watchdog Timer (IWDT)

28.1 Overview

The Independent Watchdog Timer (IWDT) is a 14-bit down counter that must be serviced periodically to prevent counter underflow. The IWDT can be used to reset the MCU or to generate a non-maskable interrupt or an underflow interrupt. Because the timer operates using an independent, dedicated clock source, it is particularly useful in returning the MCU to a known state as a failsafe mechanism when the system runs out of control. The IWDT can be triggered automatically by a reset, underflow, refresh error, or a refresh of the count value in the registers.

The IWDT functions differ from those of the WDT as follows:

- The divided IWDT-dedicated clock (IWDTCLK) is used as the count source (not affected by PCLKB)
- IWDT does not support the register start mode
- When transitioning to a low power mode (excluding Deep Software Standby mode), the OFS0.IWDTSTPCTL bit can be used to select whether to stop the counter or not.

Table 28.1 lists the IWDT specifications and Figure 28.1 shows a block diagram.

Table 28.1 IWDT specifications

Parameter	Specifications
Count source*1	IWDT-dedicated clock (IWDTCLK)
Clock division ratio	Division by 1, 16, 32, 64, 128, or 256
Counter operation	Counting down using a 14-bit down-counter
Condition for starting the counter	• Counting automatically starts after a reset
Conditions for stopping the counter	• Reset (the down-counter and other registers return to their initial values) • A counter underflows or a refresh error is generated (and counting restarts automatically)
Window function	Window start and end positions can be specified (refresh-permitted and refresh-prohibited periods)
IWDT reset sources	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)
Non-maskable interrupt/interrupt sources	• Down-counter underflows • Refreshing outside the refresh-permitted period (refresh error)
Reading of the counter value	The down-counter value can be read by the IWDTSR register
Event link function (output)	• Down-counter underflow event output • Refresh error event output
Output signal (internal signal)	• Reset output • Interrupt request output • Sleep-mode count stop control output
Auto start mode	Configurable to the following triggers: • Clock frequency division ratio after a reset (OFS0.IWDTCKS[3:0] bits) • Timeout period of the IWDT (OFS0.IWDTTOPS[1:0] bits) • Window start position in the IWDT (OFS0.IWDTRPSS[1:0] bits) • Window end position in the IWDT (OFS0.IWDTRPES[1:0] bits) • Reset output or interrupt request output (OFS0.IWDTRSTIRQS bit) • Down-count stop function on transition to Sleep mode, Software Standby mode, or Snooze mode (OFS0.IWDTSTPCTL bit)

Note 1. This must satisfy the frequency of the peripheral module clock (PCLKB) ≥ 4 × (the frequency of the count clock source after division).

To use the IWDT, you must supply the IWDT-dedicated clock (IWDTCLK). The bus interface and registers operate with PCLKB, and the 14-bit counter and control circuits operate with IWDTCLK.

28. 独立看门狗定时器(IWDT)

28.1 Overview

独立看门狗定时器(IWDT)是一个14位递减计数器，必须定期对其进行服务以防止计数器下溢。IWDT可用于复位MCU或产生不可屏蔽中断或下溢中断。由于定时器使用独立的专用时钟源运行，因此当系统失控时，它在将MCU作为故障保护机制返回到已知状态时特别有用。IWDT可以通过复位、下溢、刷新错误或寄存器中的计数值的刷新来自动触发。

IWDT的功能与WDT的不同之处如下：

- 分频的IWDT专用时钟（IWDTCLK）用作计数源（不受PCLKB影响）
- IWDT不支持寄存器启动模式
- 当转换到低功耗模式（不包括深度软件待机模式）时，OFS0.IWDTSTPCL位可用于选择是否停止计数器。

表28.1列出了IWDT规范，图28.1显示了框图。

Table 28.1 IWDT specifications

Parameter	Specifications
Count source*1	IWDT-dedicated clock (IWDTCLK)
时钟分频比	除以1、16、32、64、128或256
计数器操作	使用14位递减计数器进行递减计数
启动计数器的条件	复位后自动开始计数
停止计数器的条件	复位（递减计数器和其他寄存器恢复到初始值） 计数器下溢或产生刷新错误（计数自动重新开始）
窗口功能	可以指定窗口开始和结束位置（允许刷新和禁止刷新期间）
IWDT复位源	递减计数器下溢 在允许刷新的时间之外刷新（刷新错误）
Non-maskable interrupt/interrupt sources	递减计数器下溢 在允许刷新的时间之外刷新（刷新错误）
读取计数器值	递减计数器的值可以通过IWDTSR寄存器读取
事件链接功能（输出）	递减计数器下溢事件输出 刷新错误事件输出
输出信号（内部信号）	复位输出 中断请求输出 睡眠模式计数停止控制输出
自动启动模式	可配置为以下触发器： 复位后的时钟分频比（OFS0.IWDTCKS[3:0]位） IWDT的超时周期（OFS0.IWDTTOPS[1:0]位） IWDT中的窗口开始位置（OFS0.IWDTRPSS[1:0]位） IWDT中的窗口结束位置（OFS0.IWDTRPES[1:0]位） 复位输出或中断请求输出（OFS0.IWDTRSTIRQS位） 向下计数停止功能在转换到睡眠模式、软件待机模式或贪睡模式（OFS0.IWDTSTPCL位）

Note 1. 这必须满足外围模块时钟(PCLKB)的频率 4×(分频后的计数时钟源的频率)。

要使用IWDT，您必须提供IWDT专用时钟(IWDTCLK)。总线接口和寄存器操作PCLKB、14位计数器和控制电路使用IWDTCLK工作。

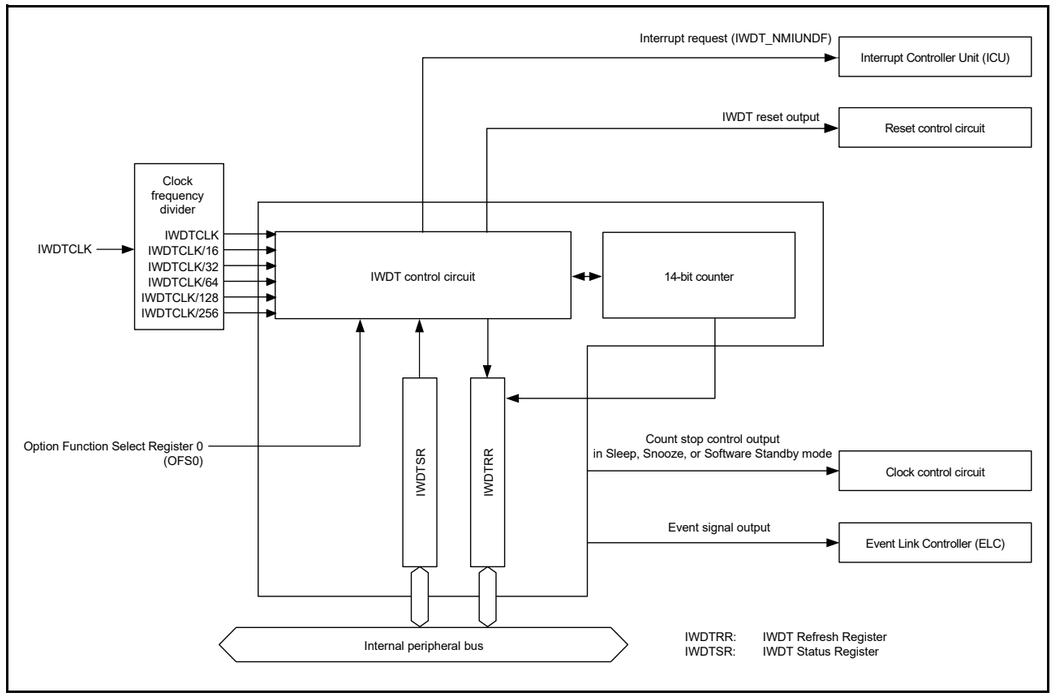


Figure 28.1 IWDT block diagram

28.2 Register Descriptions

28.2.1 IWDT Refresh Register (IWDTRR)

Address(es): IWDT.IWDTRR 4004 4400h

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1

Bit	Description	R/W
b7 to b0	The down-counter is refreshed by writing 00h and then writing FFh to this register.	R/W

The IWDTRR register refreshes the down-counter of the IWDT. The down-counter of the IWDT is refreshed by writing 00h and then writing FFh to IWDTRR (refresh operation) within the refresh-permitted period. After the counter is refreshed, it starts counting down from the value selected in the IWDT Timeout Period Select bits (OFS0.IWDTTOPS[1:0]) in Option Function Select Register 0 (OFS0).

When 00h is written, the read value is 00h. When a value other than 00h is written, the read value is FFh. For details on the refresh operation, see section 28.3.2, Refresh Operation.

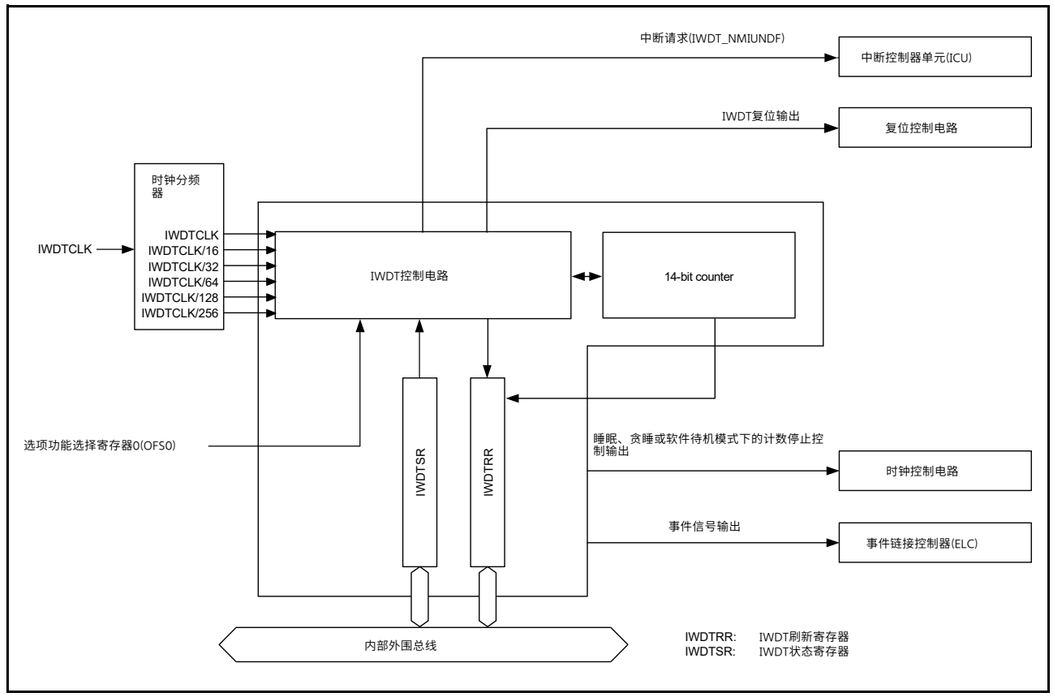


Figure 28.1 IWDT框图

28.2 注册说明

28.2.1 IWDT刷新寄存器(IWDTRR)

Address(es): IWDT.IWDTRR 4004 4400h

	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	1	1	1	1	1	1	1	1

Bit	Description	R/W
b7 to b0	通过写入00h然后将FFh写入该寄存器来刷新递减计数器。	R/W

IWDTRR寄存器刷新IWDT的递减计数器。IWDT的递减计数器通过写入00h进行刷新，然后在允许刷新期间将FFh写入IWDTRR（刷新操作）。计数器刷新后，它从选项功能选择寄存器0(OFS0)的IWDT超时周期选择位(OFS0.IWDTTOPS[1:0])中选择的值开始递减计数。

写入00h时，读取值为00h。写入00h以外的值时，读取值为FFh。有关刷新操作的详细信息，请参阅第28.3.2节，刷新操作。

28.2.2 IWDT Status Register (IWDTSR)

Address(es): IWDT.IWDTSR 4004 4404h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	REFEF	UNDFF	CNTVAL[13:0]													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b13 to b0	CNTVAL[13:0]	Counter Value	Value counted by the down-counter	R
b14	UNDFF	Underflow Flag	0: No underflow occurred 1: Underflow occurred.	R/(W)*1
b15	REFEF	Refresh Error Flag	0: No refresh error occurred 1: Refresh error occurred.	R/(W)*1

Note 1. Only 0 can be written to clear the flag.

CNTVAL[13:0] bits (Counter Value)

Read the CNTVAL[13:0] bits to confirm the value of the down-counter. The read value might differ from the actual count by 1.

UNDFF flag (Underflow Flag)

Read the UNDFF flag to confirm whether an underflow occurred in the counter. A value of 1 indicates that the down-counter underflowed. Write 0 to the flag to set the value to 0. Writing 1 has no effect.

Clearing of the UNDFF flag takes (N+2) IWDTCLK cycles and 2 PCLKB cycles. In addition, clearing of the flag is ignored for (N+2) IWDTCLK cycles after an underflow. N is specified in the IWDTCKS[3:0] bits as follows:

- When IWDTCKS[3:0] = 0000b, N = 1
- When IWDTCKS[3:0] = 0010b, N = 16
- When IWDTCKS[3:0] = 0011b, N = 32
- When IWDTCKS[3:0] = 0100b, N = 64
- When IWDTCKS[3:0] = 1111b, N = 128
- When IWDTCKS[3:0] = 0101b, N = 256

REFEF flag (Refresh Error Flag)

Read the REFEF flag to confirm whether a refresh error occurred, indicating that a refresh operation was performed during a prohibited period. A value of 1 indicates that a refresh error occurred. Write 0 to the flag to set the value to 0. Writing 1 has no effect.

Clearing of the REFEF flag takes (N+2) IWDTCLK cycles and 2 PCLKB cycles. In addition, clearing of the flag is ignored for (N+2) IWDTCLK cycles after a refresh error. N is specified in the IWDTCKS[3:0] bits as follows:

- When IWDTCKS[3:0] = 0000b, N = 1
- When IWDTCKS[3:0] = 0010b, N = 16
- When IWDTCKS[3:0] = 0011b, N = 32
- When IWDTCKS[3:0] = 0100b, N = 64
- When IWDTCKS[3:0] = 1111b, N = 128
- When IWDTCKS[3:0] = 0101b, N = 256.

28.2.2 IWDT状态寄存器(IWDTSR)

Address(es): IWDT.IWDTSR 4004 4404h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	REFEF	UNDFF	CNTVAL[13:0]													
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b13 to b0	CNTVAL[13:0]	计数器值	递减计数器计数的值	R
b14	UNDFF	Underflow Flag	0：未发生下溢1：发生下溢。	R/(W)*1
b15	REFEF	刷新错误标志	0：未发生刷新错误1：发生刷新错误。	R/(W)*1

Note 1. 只能写入0来清除标志。

CNTVAL[13:0]位（计数器值）

读取CNTVAL[13:0]位以确认递减计数器的值。读取的值可能与实际计数相差1。

UNDFF flag (Underflow Flag)

读取UNDFF标志以确认计数器是否发生下溢。值1表示递减计数器下溢。将0写入标志以将值设置为0。写入1无效。

清除UNDFF标志需要(N+2)个IWDTCLK周期和2个PCLKB周期。此外，在下溢后的(N+2)个IWDTCLK周期内忽略标志的清除。N在IWDTCKS[3:0]位中指定如下：

- When IWDTCKS[3:0] = 0000b, N = 1
- When IWDTCKS[3:0] = 0010b, N = 16
- When IWDTCKS[3:0] = 0011b, N = 32
- When IWDTCKS[3:0] = 0100b, N = 64
- When IWDTCKS[3:0] = 1111b, N = 128
- When IWDTCKS[3:0] = 0101b, N = 256

REFEF标志（刷新错误标志）

读取REFEF标志，确认是否发生刷新错误，表示在禁止期间进行了刷新操作。值1表示发生了刷新错误。将0写入标志以将值设置为0。写入1无效。

清除REFEF标志需要(N+2)个IWDTCLK周期和2个PCLKB周期。此外，在刷新错误后的(N+2)个IWDTCLK周期内，标志的清除将被忽略。N在IWDTCKS[3:0]位中指定如下：

- When IWDTCKS[3:0] = 0000b, N = 1
- When IWDTCKS[3:0] = 0010b, N = 16
- When IWDTCKS[3:0] = 0011b, N = 32
- When IWDTCKS[3:0] = 0100b, N = 64
- When IWDTCKS[3:0] = 1111b, N = 128
- When IWDTCKS[3:0] = 0101b, N = 256.

28.2.3 Option Function Select Register 0 (OFS0)

For information on Option Function Select Register 0 (OFS0), see section 7.2.1, Option Function Select Register 0 (OFS0).

IWDTTOPS[1:0] bits (IWDT Timeout Period Select)

The IWDTTOPS[1:0] bits select the timeout period, the period until the down-counter underflows, from 128, 512, 1024, or 2048 cycles, taking the divided clock specified in the IWDTCKS[3:0] bits as 1 cycle. After the down-counter is refreshed, the combination of the IWDTCKS[3:0] and IWDTTOPS[1:0] bits determines the number of IWDTCLK cycles until the counter underflows.

Table 28.2 lists the relationship between the IWDTCKS[3:0] and IWDTTOPS[1:0] bit settings, the timeout period, and the number of IWDTCLK cycles.

Table 28.2 Timeout period settings

IWDTCKS[3:0] bits				IWDTTOPS[1:0] bits		Clock division ratio	Timeout period (number of cycles)	IWDTCLK cycles
b7	b6	b5	b4	b1	b0			
0	0	0	0	0	0	IWDTCLK	128	128
				0	1		512	512
				1	0		1,024	1,024
				1	1		2,048	2,048
0	0	1	0	0	0	IWDTCLK/16	128	2,048
				0	1		512	8,192
				1	0		1,024	16,384
				1	1		2,048	32,768
0	0	1	1	0	0	IWDTCLK/32	128	40,96
				0	1		512	16,384
				1	0		1,024	32,768
				1	1		2,048	65,536
0	1	0	0	0	0	IWDTCLK/64	128	8,192
				0	1		512	32,768
				1	0		1,024	65,536
				1	1		2,048	131,072
1	1	1	1	0	0	IWDTCLK/128	128	16,384
				0	1		512	65,536
				1	0		1,024	131,072
				1	1		2,048	262,144
0	1	0	1	0	0	IWDTCLK/256	128	32,768
				0	1		512	131,072
				1	0		1,024	262,144
				1	1		2,048	5242,88

IWDTCKS[3:0] bits (IWDT-Dedicated Clock Frequency Division Ratio Select)

The IWDTCKS[3:0] bits specify the division ratio of the clock used for the down-counter. The division ratio can be selected from the IWDT-dedicated clock (IWDTCLK) divided by 1, 16, 32, 64, 128, and 256. Combined with the IWDTTOPS[1:0] bit setting, this allows the IWDT to be configured to a count period between 128 and 524288 IWDTCLK cycles.

IWDTRPES[1:0] bits (IWDT Window End Position Select)

The IWDTRPES[1:0] bits specify the window end position that indicates the refresh-permitted period. 75%, 50%, 25%, or 0% of the timeout period can be selected for the window end position. Set the window end position to a value less than

28.2.3 选项功能选择寄存器0(OFS0)

有关选项功能选择寄存器0(OFS0)的信息，请参阅第7.2.1节，选项功能选择寄存器0(OFS0)。

IWDTTOPS[1:0]位（IWDT超时周期选择）

IWDTTOPS[1:0]位从128、512、1024或2048个周期中选择超时周期，直到递减计数器下溢的周期，将IWDTCKS[3:0]位中指定的分频时钟作为1个周期.向下计数器刷新后，IWDTCKS[3:0]和IWDTTOPS[1:0]位的组合决定了在计数器下溢之前的IWDTCLK周期数。

表28.2列出了IWDTCKS[3:0]和IWDTTOPS[1:0]位设置、超时周期和IWDTCLK周期数之间的关系。

Table 28.2 超时时间设置

IWDTCKS[3:0] bits				IWDTTOPS[1:0] bits		时钟分频比	超时时间（周期数）	IWDTCLK cycles
b7	b6	b5	b4	b1	b0			
0	0	0	0	0	0	IWDTCLK	128	128
				0	1		512	512
				1	0		1,024	1,024
				1	1		2,048	2,048
0	0	1	0	0	0	IWDTCLK/16	128	2,048
				0	1		512	8,192
				1	0		1,024	16,384
				1	1		2,048	32,768
0	0	1	1	0	0	IWDTCLK/32	128	40,96
				0	1		512	16,384
				1	0		1,024	32,768
				1	1		2,048	65,536
0	1	0	0	0	0	IWDTCLK/64	128	8,192
				0	1		512	32,768
				1	0		1,024	65,536
				1	1		2,048	131,072
1	1	1	1	0	0	IWDTCLK/128	128	16,384
				0	1		512	65,536
				1	0		1,024	131,072
				1	1		2,048	262,144
0	1	0	1	0	0	IWDTCLK/256	128	32,768
				0	1		512	131,072
				1	0		1,024	262,144
				1	1		2,048	5242,88

IWDTCKS[3:0]位（IWDT专用时钟分频比选择）

IWDTCKS[3:0]位指定用于递减计数器的时钟分频比。分频比可以从IWDT专用时钟(IWDTCLK)除以1、16、32、64、128和256中选择。结合IWDTTOPS[1:0]位设置，这允许将IWDT配置为128到524288之间的计数周期

IWDTCLK cycles.

IWDTRPES[1:0]位（IWDT窗口结束位置选择）

IWDTRPES[1:0]位指定指示刷新允许周期的窗口结束位置。可以为窗口结束位置选择75%、50%、25%或0%的超时时间。将窗口结束位置设置为小于

the window start position (window start position > window end position). If the window end position is greater than the window start position, only the window start position setting is enabled.

IWDTRPSS[1:0] bits (IWDT Window Start Position Select)

The IWDTRPSS[1:0] bits specify the window start position that indicates the refresh-permitted period. 100%, 75%, 50%, or 25% of the timeout period can be selected for the window start position. Set the window start position to a value greater than the window end position. If the window start position is less than or equal to the window end position, the window end position is set to 0%.

Table 28.3 lists the counter values for the window start and end positions, and Figure 28.2 shows the refresh-permitted period set in the IWDTRPSS[1:0], IWDTRPES[1:0], and IWDTTOPS[1:0] bits.

Table 28.3 Relationship between the timeout period and window start and end counter values

IWDTTOPS[1:0] bits		Timeout period		Window start and end counter value			
b1	b0	Cycles	Counter value	100%	75%	50%	25%
0	0	128	007Fh	007Fh	005Fh	003Fh	001Fh
0	1	512	01FFh	01FFh	017Fh	00FFh	007Fh
1	0	1,024	03FFh	03FFh	02FFh	01FFh	00FFh
1	1	2,048	07FFh	07FFh	05FFh	03FFh	01FFh

IWDTRPSS[1:0] bits		IWDTRPES[1:0] bits		Window	
b13	b12	b9	b8	Start (%)	End (%)
1	1	1	1	100	0
		1	0		25
		0	1		50
		0	0		75
1	0	1	1	75	0
		1	0		25
		0	1		50
		0	0		75
0	1	1	1	50	0
		1	0		25
		0	1		50
		0	0		75
0	0	1	1	25	0
		1	0		25
		0	1		50
		0	0		75

Note: If window end setting ≥ window start setting, the window end setting is set to 0%.

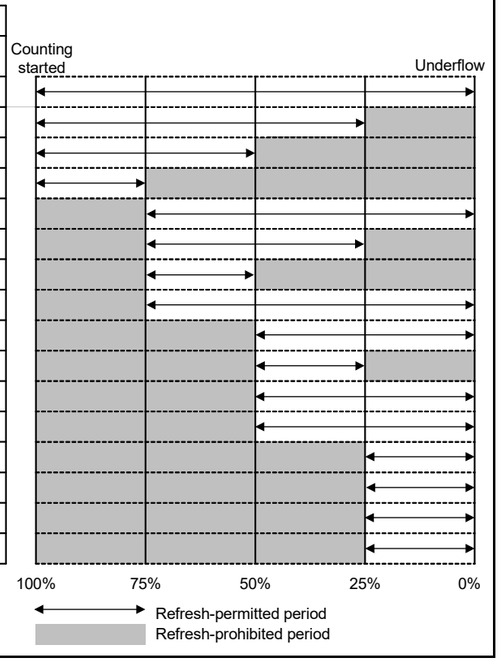


Figure 28.2 IWDTRPSS[1:0] and IWDTRPES[1:0] bit settings and refresh-permitted period

IWDTRSTIRQS bit (IWDT Reset Interrupt Request Select)

The IWDTRSTIRQS bit specifies the behavior when an underflow or a refresh error occurs. Setting 1 selects reset output. Setting 0 selects non-maskable interrupt or interrupt.

IWDTSTPCTL bit (IWDT Stop Control)

The IWDTSTPCTL bit controls whether to stop counting on transition to Sleep, Snooze, or Software Standby mode.

窗口起始位置（窗口起始位置>窗口结束位置）。如果窗口结束位置大于窗口起始位置，则仅启用窗口起始位置设置。

IWDTRPSS[1:0]位（IWDT窗口起始位置选择）

IWDTRPSS[1:0]位指定指示刷新允许周期的窗口起始位置。窗口起始位置可选择100%、75%、50%或25%的超时时间。将窗口开始位置设置为大于窗口结束位置的值。如果窗口开始位置小于或等于窗口结束位置，则窗口结束位置设置为0%。

表28.3列出了窗口开始和结束位置的计数器值，图28.2显示了在IWDTRPSS[1:0]、IWDTRPES[1:0]和IWDTTOPS[1:0]位中设置的允许刷新周期。

Table 28.3 超时时间与窗口开始和结束计数器值之间的关系

IWDTTOPS[1:0] bits		超时时间		窗口开始和结束计数器值			
b1	b0	Cycles	计数器值	100%	75%	50%	25%
0	0	128	007Fh	007Fh	005Fh	003Fh	001Fh
0	1	512	01FFh	01FFh	017Fh	00FFh	007Fh
1	0	1,024	03FFh	03FFh	02FFh	01FFh	00FFh
1	1	2,048	07FFh	07FFh	05FFh	03FFh	01FFh

IWDTRPSS[1:0] bits		IWDTRPES[1:0] bits		Window	
b13	b12	b9	b8	Start (%)	End (%)
1	1	1	1	100	0
		1	0		25
		0	1		50
		0	0		75
1	0	1	1	75	0
		1	0		25
		0	1		50
		0	0		75
0	1	1	1	50	0
		1	0		25
		0	1		50
		0	0		75
0	0	1	1	25	0
		1	0		25
		0	1		50
		0	0		75

注意：如果窗口结束设置　窗口开始设置，窗口结束设置设置为0%。

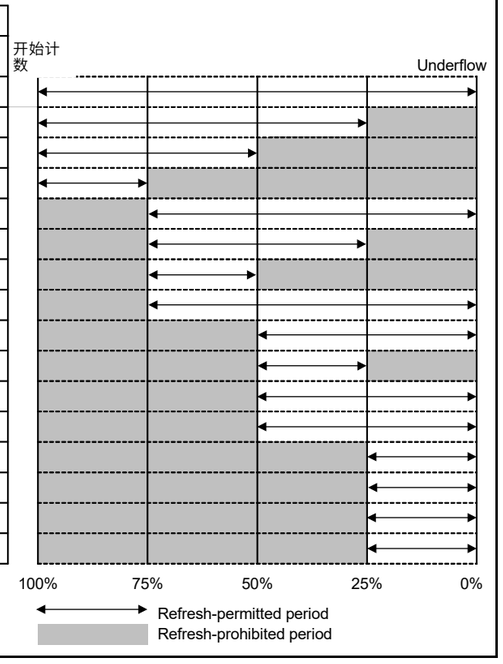


Figure 28.2 IWDTRPSS[1:0]和IWDTRPES[1:0]位设置和允许刷新周期

IWDTRSTIRQS位（IWDT复位中断请求选择）

IWDTRSTIRQS位指定发生下溢或刷新错误时的行为。设置1选择复位输出。设置0选择不可屏蔽中断或中断。

IWDTSTPCTL位（IWDT停止控制）

IWDTSTPCTL位控制在转换到休眠、贪睡或软件待机模式时是否停止计数。

28.3 Operation

28.3.1 Auto Start Mode

When the IWDT Start Mode Select bit (OFS0.IWDTSTRT) is 0, auto start mode is selected. Otherwise, the IWDT is disabled.

Within the reset state, the following values in Option Function Select Register 0 (OFS0) are set in the IWDT registers:

- Clock division ratio
- Window start and end positions
- Timeout period
- Reset output or interrupt request
- Counter stop control on transition to the low power modes.

When the reset state is released, the down-counter automatically starts counting down from the value set in the IWDT Timeout Period Select bits (OFS0.IWDTTOPS[1:0]).

After that, as long as the program continues normal operation and the counter is refreshed within the refresh-permitted period, the value in the counter is reset each time the counter is refreshed and down-counting continues. The IWDT does not output the reset signal as long as this procedure continues. However, if the counter underflows because the program crashes, or because a refresh error occurs when an attempt is made to refresh outside the refresh-permitted period, the IWDT asserts the reset signal or non-maskable interrupt request/interrupt request (IWDT_NMIUNDF).

After the reset signal or non-maskable interrupt request/interrupt request is generated, the counter reloads the timeout period after counting for 1 cycle, and restarts the count. Reset output or interrupt request output can be selected in the IWDT Reset Interrupt Request Select bit (OFS0.IWDTRSTIRQS). Non-maskable interrupt request or interrupt request can be selected in the IWDT Underflow/Refresh Error Interrupt Enable bit (NMIER.IWDTEN).

Figure 28.3 shows an example of operation under the following conditions:

- Auto start mode (OFS0.IWDTSTRT = 0)
- Non-maskable interrupt request output is enabled (OFS0.IWDTRSTIRQS = 0)
- The window start position is 75% (OFS0.IWDTRPSS[1:0] = 10b)
- The window end position is 25% (OFS0.IWDTRPES[1:0] = 10b).

28.3 Operation

28.3.1 自动启动模式

当IWDT启动模式选择位(OFS0.IWDTSTRT)为0时，选择自动启动模式。否则，禁用IWDT。

在复位状态下，选项功能选择寄存器0(OFS0)中的以下值在IWDT寄存器中设置：

- 时钟分频比
- 窗口开始和结束位置
- 超时时间
- 复位输出或中断请求
- 转换到低功耗模式时的计数器停止控制。

复位状态解除后，递减计数器自动从IWDT中设置的值开始递减计数
超时周期选择位(OFS0.IWDTOPS[1:0])。

之后，只要程序继续正常运行，并且在允许刷新的时间内刷新计数器，每次刷新计数器并继续递减计数时，计数器中的值都会被复位。只要此过程继续，IWDT就不会输出复位信号。但是，如果由于程序崩溃或由于在刷新允许周期之外尝试刷新时发生刷新错误而导致计数器下溢，则IWDT将置位复位信号或不可屏蔽中断请求中断请求(IWDT_NMIUNDF)。

复位信号或不可屏蔽中断请求中断请求产生后，计数器在计数1个周期后重新加载超时周期，重新开始计数。可以在IWDT复位中断请求选择位(OFS0.IWDTRSTIRQS)中选择复位输出或中断请求输出。可以在IWDT下溢刷新错误中断　　允许位(NMIER.IWDTEN)中选择不可屏蔽的中断请求或中断请求。

图28.3显示了以下条件下的操作示例：

- 自动启动模式（OFS0.IWDTSTRT=0）
- 使能不可屏蔽中断请求输出(OFS0.IWDTRSTIRQS=0)
- 窗口起始位置为75%(OFS0.IWDTRPSS[1:0]=10b)
- 窗口结束位置为25%(OFS0.IWDTRPES[1:0]=10b)。

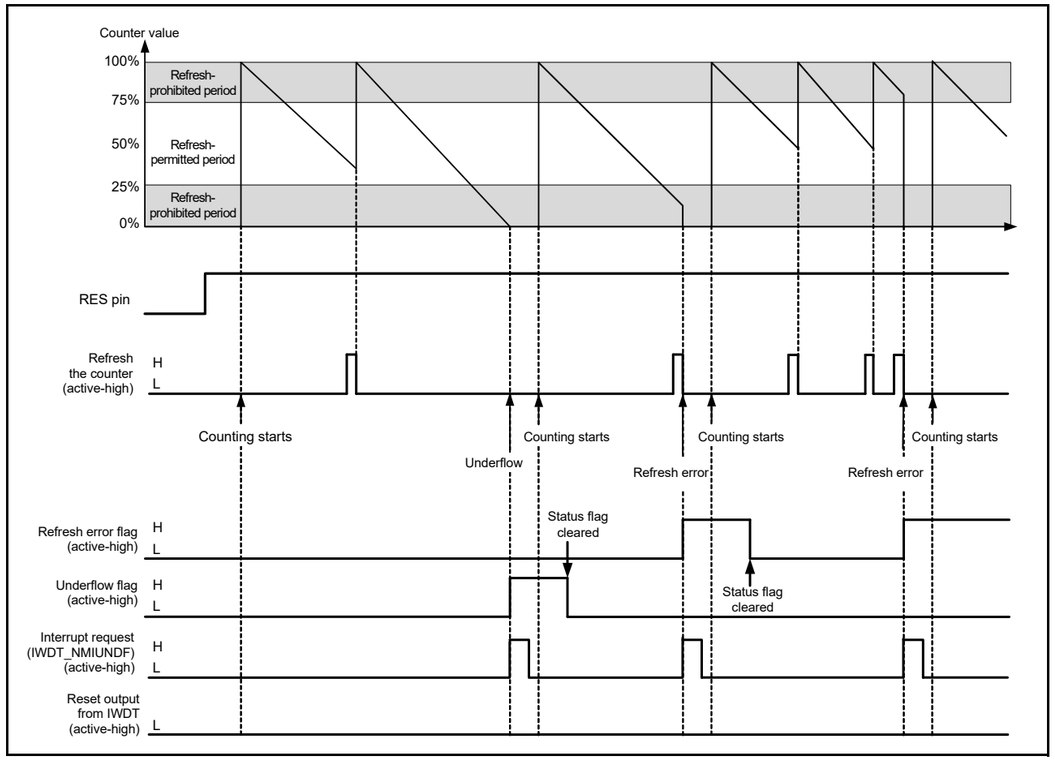


Figure 28.3 Operation example in auto start mode

28.3.2 Refresh Operation

The down-counter is refreshed by writing the values 00h and FFh to the IWDT Refresh Register (IWDTRR). If a value other than FFh is written after 00h, the down-counter is not refreshed. If an invalid value is written, correct refreshing resumes on a write of 00h and FFh to the IWDTRR register.

When writes are made in the order of 00h (first time) → 00h (second time), and if FFh is written after that, the writing order 00h → FFh is satisfied. Writes of 00h (n-1th time) → 00h (nth time) → FFh are valid, and the refresh is performed correctly. Even when the first value written before 00h is not 00h, correct refreshing is performed as long as the operation contains the write sequence of 00h → FFh.

Correct refreshing is also performed when a register other than IWDTRR is accessed or IWDTRR is read between writing 00h and writing FFh to IWDTRR. Writes to refresh the counter must be made within the refresh-permitted period, and this is determined by the FFh write. For this reason, correct refreshing is performed even when 00h is written outside the refresh-permitted period.

[Example write sequences that are valid for refreshing the counter]

- 00h → FFh
- 00h (n-1th time) → 00h (nth time) → FFh
- 00h → access to another register or read from IWDTRR → FFh.

[Example write sequences that are invalid for refreshing the counter]

- 23h (a value other than 00h) → FFh
- 00h → 54h (a value other than FFh)
- 00h → AAh (00h and a value other than FFh) → FFh.

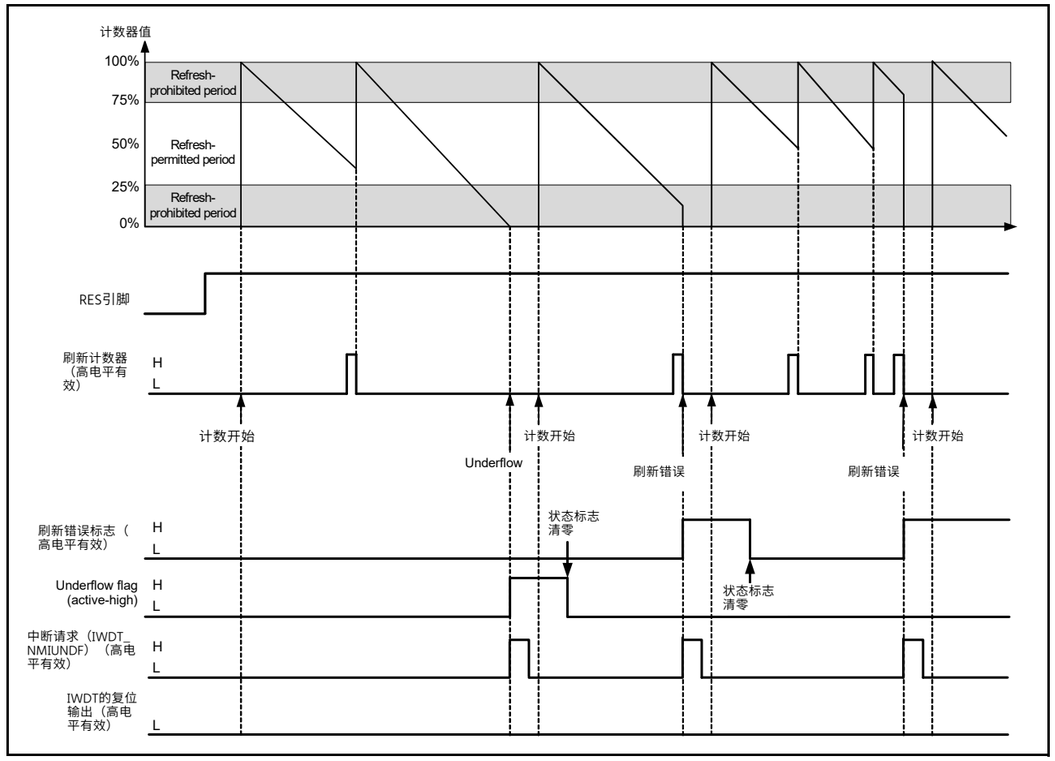


Figure 28.3 自动启动模式下的操作示例

28.3.2 刷新操作

通过将值00h和FFh写入IWDT刷新寄存器(IWDTRR)来刷新递减计数器。如果在00h之后写入FFh以外的值，则不刷新递减计数器。如果写入无效值，则在将00h和FFh写入IWDTRR寄存器时会恢复正确刷新。

当以00h（第一次）→00h（第二次）的顺序进行写入时，如果在此之后写入FFh，则满足写入顺序00h→FFh。00h（第n-1次）→00h（第n次）→FFh的写入有效，刷新正确。即使在00h之前写入的第一个值不是00h，只要操作包含00h→FFh的写入序列，就会执行正确的刷新。

当访问IWDTRR以外的寄存器或在写入00h和将FFh写入IWDTRR之间读取IWDTRR时，也会执行正确刷新。刷新计数器的写操作必须在允许刷新的时间内进行，这由FFh写操作决定。因此，即使在刷新允许期间之外写入00h，也会执行正确的刷新。

[对刷新计数器有效的示例写入序列]

- 00h → FFh
- 00h (n-1th time) → 00h (nth time) → FFh
- 00h→访问另一个寄存器或从IWDTRR→FFh读取。

[对刷新计数器无效的示例写入序列]

- 23h（00h以外的值）→FFh
- 00h→54h（FFh以外的值）
- 00h→AAh(00h和FFh以外的值)→FFh。

After FFh is written to the IWDT Refresh Register (IWDTRR), refreshing the down-counter requires up to 4 cycles of the signal for counting (the IWDT-dedicated clock frequency division ratio select bits (OFS0.IWDTCKS[3:0]) determine how many cycles of the IWDT-dedicated clock (IWDTCLK) make up 1 counting cycle). To meet this requirement, complete writing FFh to IWDTRR 4 count cycles before the end of the refresh-permitted period or a counter underflow. The value of the counter can be checked in the counter bits (IWDTSR.CNTVAL[13:0]).

[Example refreshing timings]

- When the window start position is set to 1FFFh, even if 00h is written to IWDTRR before 1FFFh is reached (at 2002h, for example), refreshing occurs if FFh is written to IWDTRR after the value of the IWDTSR.CNTVAL[13:0] bits reaches 1FFFh.
- When the window end position is set to 1FFFh, refreshing occurs if 2003h (four count cycles before 1FFFh) or a greater value is read from the IWDTSR.CNTVAL[13:0] bits immediately after a write of 00h → FFh to IWDTRR.
- When the refresh-permitted period continues until count 0000h, refreshing can be performed immediately before an underflow. In this case, if 0003h (four count cycles before an underflow) or a greater value is read from the IWDTSR.CNTVAL[13:0] bits immediately after a write of 00h → FFh to IWDTRR, no underflow occurs and refreshing is performed.

Figure 28.4 shows the IWDT refresh-operation waveforms when PCLKB > IWDTCLK and the clock division ratio is IWDTCLK.

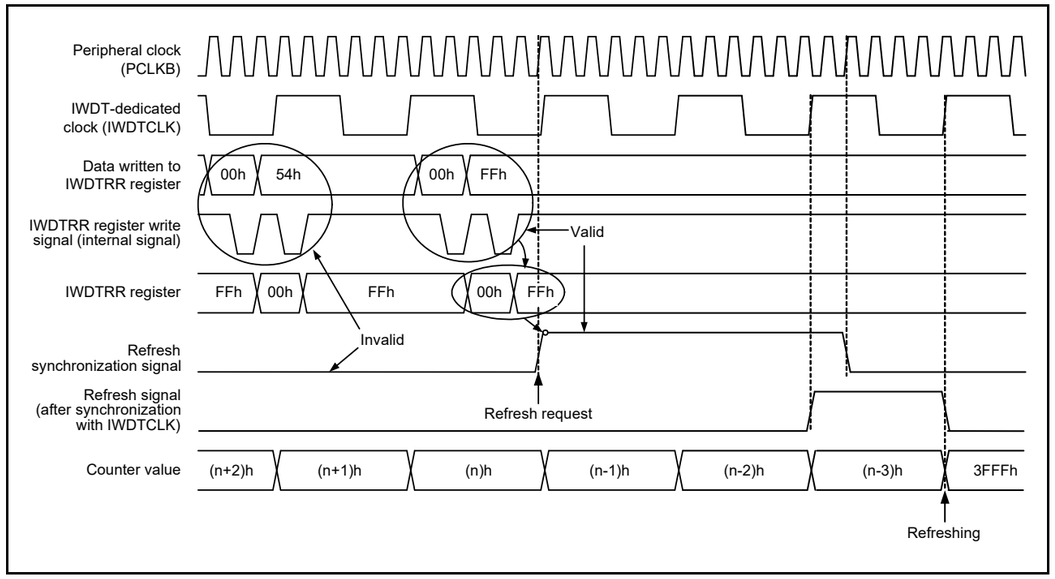


Figure 28.4 IWDT refresh operation waveforms when OFS0.IWDTCKS[3:0] = 0000b and OFS0.IWDTTOPS[1:0] = 11b

28.3.3 Status Flags

The refresh error (IWDTSR.REFEF) and underflow (IWDTSR.UNDFF) flags retain the source of the reset signal output from the IWDT or the source of the interrupt request from the IWDT. After a release from the reset state or interrupt request generation, read the IWDTSR.REFEF and UNDFF flags to check for the reset or interrupt source. For each flag, writing 0 clears the bit and writing 1 has no effect.

Leaving the status flags unchanged does not affect operation. If the flags are not cleared on the next reset or interrupt request from the IWDT, the earlier reset or interrupt source is cleared and the new reset or interrupt source is written. After 0 is written to each flag, up to 3 IWDTCLK cycles and 2 PCLKB cycles are required before the value is reflected.

将FFh写入IWDT刷新寄存器(IWDTRR)后，刷新递减计数器需要最多4个周期的计数信号（IWDT专用时钟分频比选择位(OFS0.IWDTCKS[3:0])确定IWDT专用时钟(IWDTCLK)的多少个周期构成1个计数周期）。为满足此要求，请在刷新允许周期结束或计数器下溢之前4个计数周期将FFh写入IWDTRR。可以在计数器位(IWDTSR.CNTVAL[13:0])中检查计数器的值。

[Example refreshing timings]

- 当窗口起始位置设置为1FFFh时，即使在到达1FFFh之前（例如在2002h）将00h写入IWDTRR，如果在IWDTSR.CNTVAL[13:0]的值之后将FFh写入IWDTRR，也会发生刷新位达到1FFFh。
- 当窗口结束位置设置为1FFFh时，如果在将00h→FFh写入IWDTRR后立即从IWDTSR.CNTVAL[13:0]位读取2003h（1FFFh之前的四个计数周期）或更大的值，则会发生刷新。
- 当刷新允许周期持续到计数0000h时，可以在下溢之前立即执行刷新。在这种情况下，如果在将00h→FFh写入IWDTRR后立即从IWDTSR.CNTVAL[13:0]位读取0003h（下溢之前的四个计数周期）或更大的值，则不会发生下溢并执行刷新。

图28.4显示了当PCLKB>IWDTCLK并且时钟分频比为时的IWDT刷新操作波形
IWDTCLK.

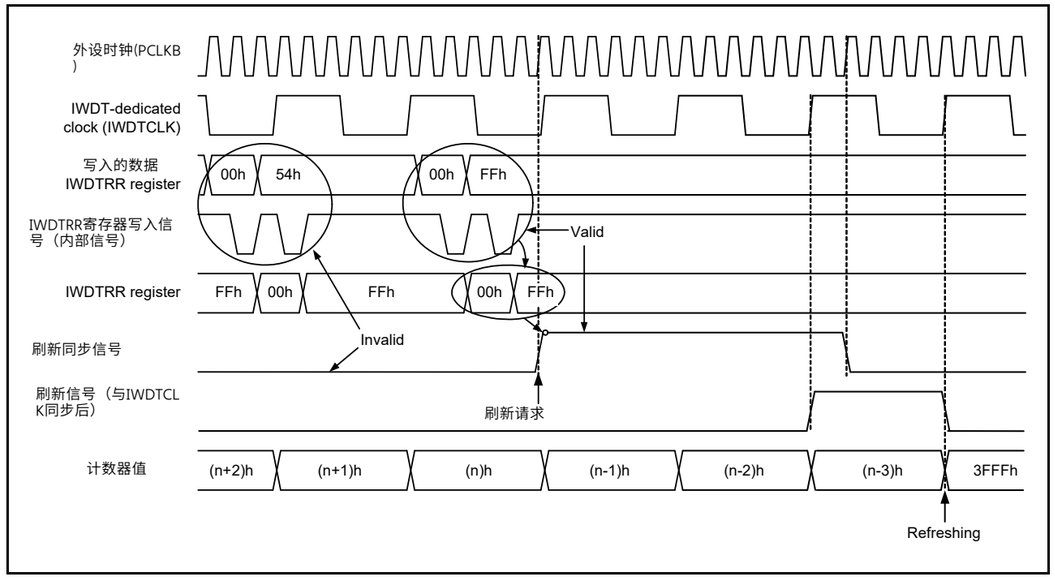


Figure 28.4 当OFS0.IWDTCKS[3:0]=0000b且OFS0.IWDTCKS[1:0]=11b时的IWDT刷新操作波形

28.3.3 状态标志

刷新错误(IWDTSR.REFEF)和下溢(IWDTSR.UNDFF)标志保留IWDT的复位信号输出源或IWDT的中断请求源。从复位状态释放或产生中断请求后，读取IWDTSR.REFEF和UNDFF标志以检查复位或中断源。对于每个标志，写入0清除该位，写入1无效。

保持状态标志不变不会影响操作。如果在IWDT发出的下一次复位或中断请求时未清除标志，则清除较早的复位或中断源并写入新的复位或中断源。将0写入每个标志后，最多需要3个IWDTCLK周期和2个PCLKB周期才能反映该值。

28.3.4 Reset Output

When the IWDT Reset Interrupt Request Select bit (OFS0.IWDTRSTIRQS) in Option Function Select Register 0 (OFS0) is set to 1, a reset signal is output when an underflow in the down-counter or a refresh error occurs. Counting down starts automatically after the reset output.

28.3.5 Interrupt Sources

When the IWDT Reset Interrupt Request Select bit (OFS0.IWDTRSTIRQS) in Option Function Select Register 0 (OFS0) is set to 0, an interrupt signal (IWDT_NMIUNDF) is generated when an underflow in the counter or a refresh error occurs. This interrupt can be used as a non-maskable interrupt or an interrupt. For details, see section 14, Interrupt Controller Unit (ICU).

Table 28.4 IWDT interrupt source

Name	Interrupt source	DTC activation	DMAC activation
IWDT_NMIUNDF	• Down-counter underflow • Refresh error	Not possible	Not possible

28.3.6 Reading the Down-Counter Value

Because the counter is the IWDT-dedicated clock (IWDTCLK), the counter value cannot be read directly. The IWDT synchronizes the counter value with the peripheral clock (PCLKB) and stores it in the down-counter value bits (IWDTSR.CNTVAL[13:0]) of the IWDT Status register. Check these bits to obtain the counter value indirectly. Reading the counter value requires multiple PCLKB clock cycles (up to four clock cycles), and the read counter value might differ from the actual counter value by a value of one count.

Figure 28.5 shows the processing for reading the IWDT counter value when PCLKB > IWDTCLK and the clock division ratio is IWDTCLK.

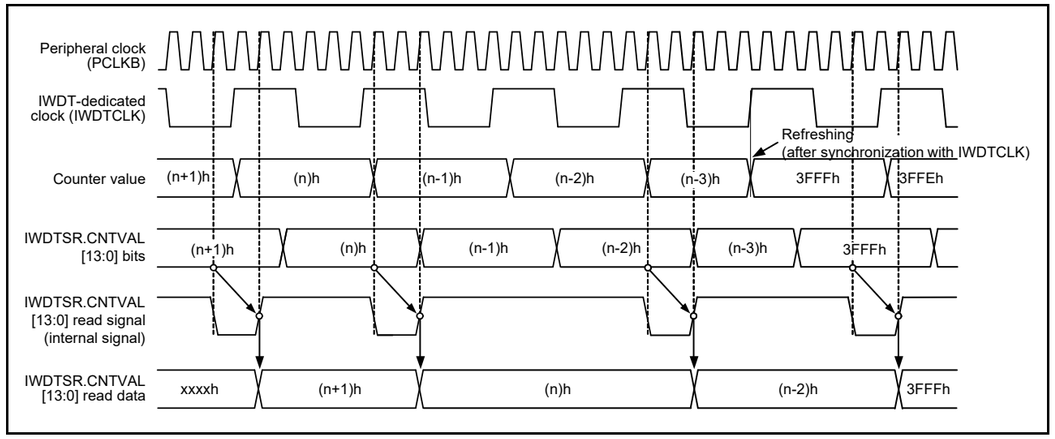


Figure 28.5 Processing for reading IWDT counter value when OFS0.IWDTCKS[3:0] = 0000b and OFS0.IWDTTOPS[1:0] = 11b

28.4 Output to the Event Link Controller (ELC)

The IWDT is capable of link operation for a specified module when the interrupt request signal is used as an event signal by the ELC. The event signal is output by the counter underflow or refresh error.

An event signal is output regardless of the setting in the OFS0.WDTRSTIRQS bit. An event signal can also be output when the next interrupt source is generated while the Refresh Error Flag (IWDTSR.REFEF) or Underflow Flag (IWDTSR.UNDFF) is 1. For details, see section 19, Event Link Controller (ELC).

28.3.4 复位输出

当IWDT重置中断请求选择位置（OFS0.IWDTRSTIRQS）在选项函数选择寄存器0（OFS0）中的BIT（OFS0）设置为1时，当下部访问中的下流或刷新错误发生时，将输出重置信号。复位输出后自动开始倒计时。

28.3.5 中断源

当IWDT重置中断请求选择位置（OFS0.IWDTRSTIRQS）中的选项功能选择寄存器0（OFS0）设置为0时，当计数器中的下流或刷新错误时，会生成中断信号（IWDT_NMIUNDF）。此中断可用作不可屏蔽中断或中断。有关详细信息，请参阅第14节，中断控制器单元(ICU)。

Table 28.4 IWDT中断源

Name	中断源	DTC activation	DMAC activation
IWDT_NMIUNDF	递减计数器下溢 刷新错误	不可能	不可能

28.3.6 读取递减计数器值

因为计数器是IWDT专用时钟（IWDTCLK），所以无法直接读取计数器值。IWDT将计数器值与外设时钟(PCLKB)同步，并将其存储在IWDT状态寄存器的递减计数器值位(IWDTSR.CNTVAL[13:0])中。检查这些位以间接获得计数器值。读取计数器值需要多个PCLKB时钟周期（最多四个时钟周期），并且读取的计数器值可能与实际计数器值相差一个计数值。

图28.5显示了当PCLKB>IWDTCLK并且时钟分频比为IWDTCLK时读取IWDT计数器值的处理。

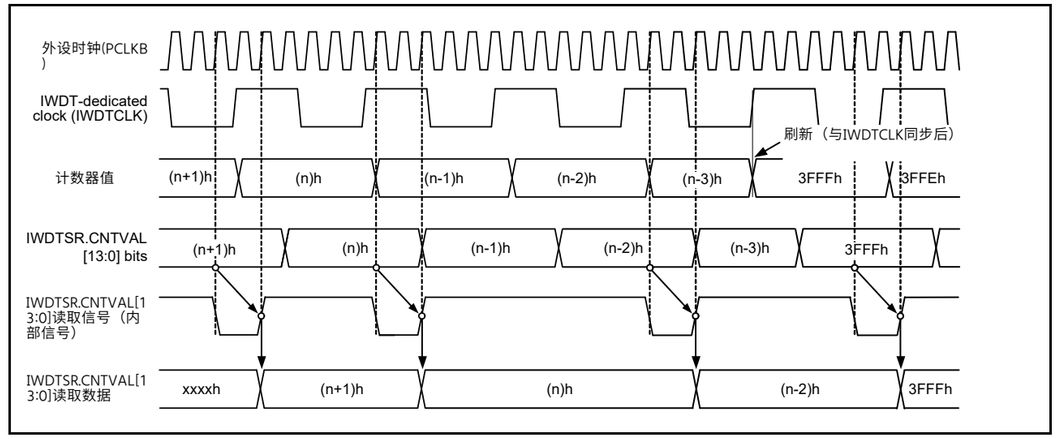


Figure 28.5 当OFS0.IWDTCKS[3:0]=0000b和时读取IWDT计数器值的处理 OFS0.IWDTTOPS[1:0] = 11b

28.4 输出到事件链接控制器(ELC)

当中断请求信号被ELC用作事件信号时，IWDT能够对指定模块进行链接操作。事件信号由计数器下溢或刷新错误输出。

无论OFS0.WDTRSTIRQS位的设置如何，都会输出事件信号。当刷新错误标志(IWDTSR.REFEF)或下溢标志(IWDTSR.UNDFF)为1时，也可以在产生下一个中断源时输出事件信号。有关详细信息，请参阅第19节，事件链接控制器(ELC)。

28.5 Usage Notes

28.5.1 Refresh Operations

While configuring the refresh time, consider variations in the range of errors given the accuracy of PCLKB and IWDTCLK. Set values that ensure refreshing is possible.

28.5.2 Constraints on the Clock Division Ratio Setting

Satisfy the following required frequency of the peripheral module clock (PCLKB):

PCLKB ≥ 4 × (the frequency of the count clock source after division).

28.5 使用说明

28.5.1 刷新操作

在配置刷新时间时，考虑到给定PCLKB精度和误差范围的变化IWDTCLK。设置确保可以刷新的值。

28.5.2 时钟分频比设置的约束

满足以下所需的外围模块时钟（PCLKB）频率：

PCLKB 4 （分频后计数时钟源的频率）。

29. Ethernet MAC Controller (ETHERC)

29.1 Overview

The MCU provides a one-channel Ethernet Controller (ETHERC) compliant with the Ethernet or IEEE802.3 Media Access Control (MAC) layer protocol. ETHERC channel has one channel of the MAC layer interface. Connecting the MCU to the physical layer LSI (PHY-LSI) allows transmission and reception of frames compliant with the Ethernet/IEEE802.3 standard. The ETHERC is connected through the Ethernet PTP Controller (EPTPC) to the Ethernet DMA Controller (EDMAC), so data can be transferred without using the CPU. When the EPTPC is not used, bypass the EPTPC by setting the bypass registers in the EPTPC. See section 30.2.79, Bypass 1588 Module Register (BYPASS).

Table 29.1 lists the ETHERC specifications, Figure 29.1 shows the configuration, and Table 29.2 lists the I/O pins. Figure 29.2 and Figure 29.3 show examples connections of the MCU to an external PHY-LSI.

Table 29.1 ETHERC specifications

Parameter	Specifications
Number of channels	One channel
Protocol	Flow control compliant with IEEE802.3x
Data transmission/reception	Frames compliant with the Ethernet/IEEE802.3 standard can be transmitted and received
Bit rate	Supports 10 Mbps and 100 Mbps
Operation modes	Supports full-duplex and half-duplex modes
Interfaces	Media Independent Interface (MII), Reduced Media Independent Interface (RMII), compliant with the IEEE802.3u standard
Functions	Magic Packet™ detection, Wake-on-LAN (WOL) signal output

29. 以太网MAC控制器(ETHERC)

29.1 Overview

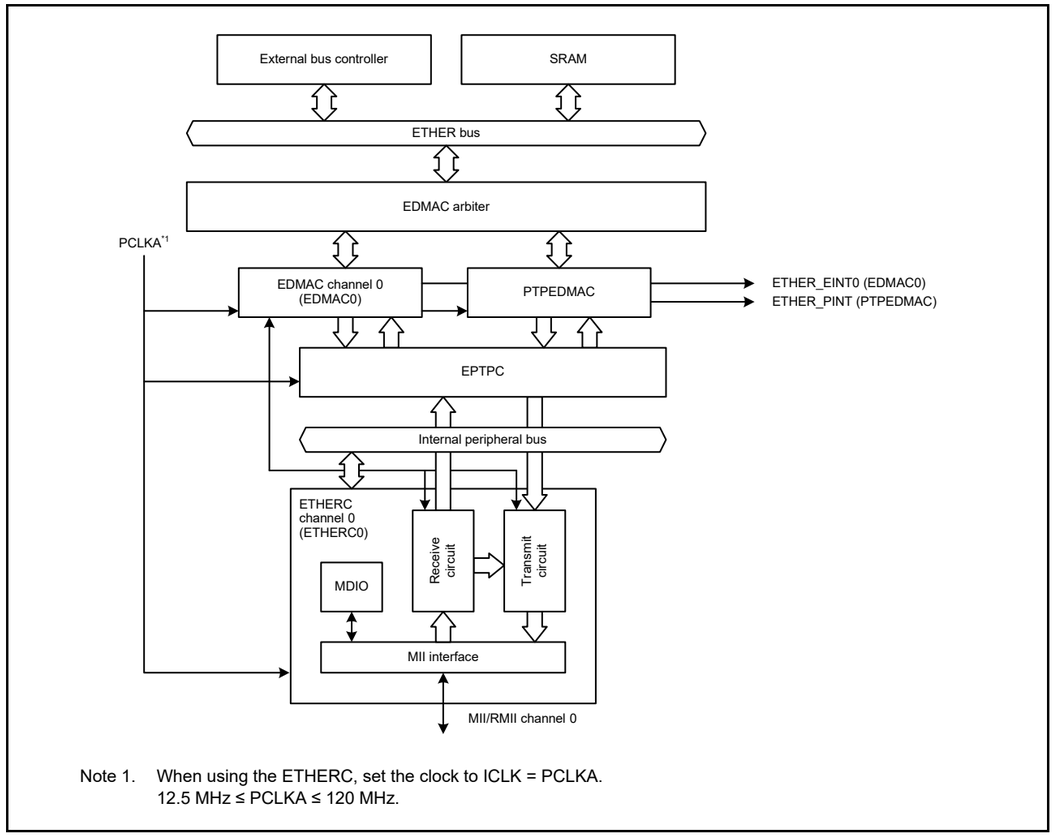
MCU提供符合以太网或IEEE802.3媒体访问控制(MAC)层协议的单通道以太网控制器(ETHERC)。ETHERC通道有一个MAC层接口通道。将MCU连接到物理层LSI(PHY-LSI)允许发送和接收符合以太网的帧

IEEE802.3标准。ETHERC通过以太网PTP控制器(EPTPC)连接到以太网DMA控制器(EDMAC)，因此可以在不使用CPU的情况下传输数据。不使用EPTPC时，绕过
EPTPC通过设置EPTPC中的旁路寄存器。请参阅第30.2.79节，绕过1588模块寄存器(BYPASS)。

表29.1列出了ETHERC规范，图29.1显示了配置，表29.2列出了IO引脚。
图29.2和图29.3显示了MCU与外部PHY-LSI的连接示例。

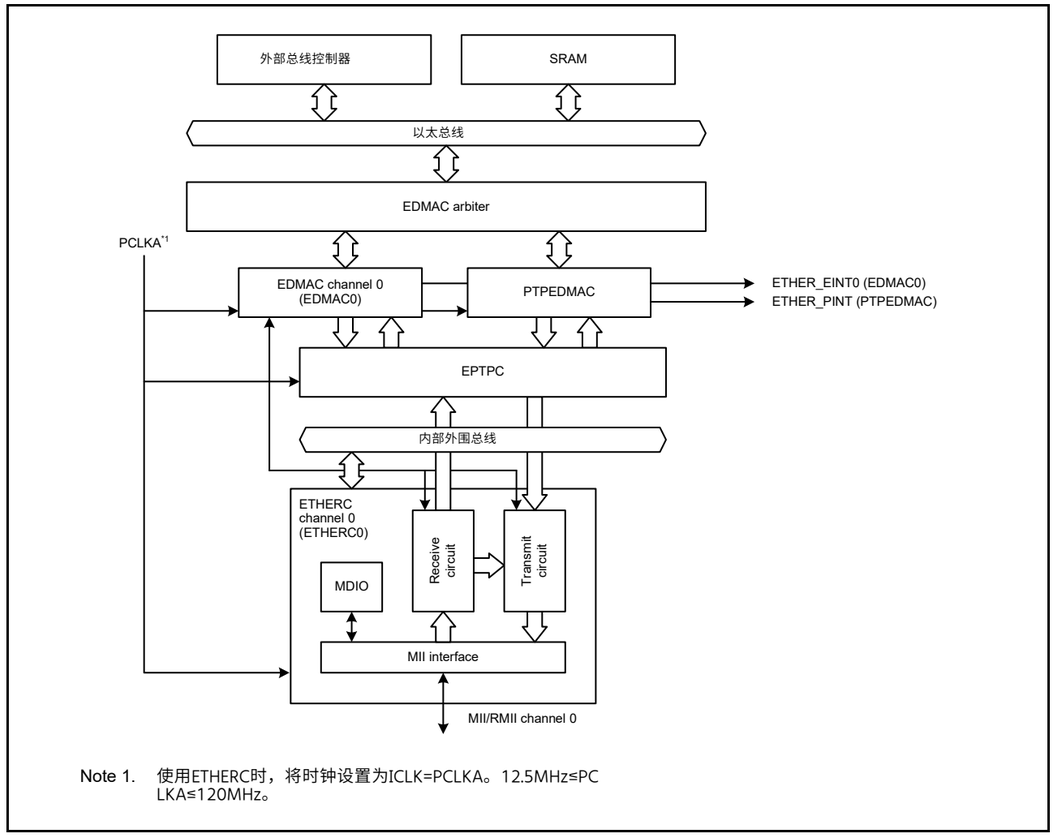
Table 29.1 ETHERC specifications

Parameter	Specifications
通道数	一个频道
Protocol	符合IEEE802.3x的流量控制
Data transmission/reception	可以发送和接收符合以太网IEEE802.3标准的帧
比特率	支持10Mbps和100Mbps
操作模式	支持全双工和半双工模式
Interfaces	媒体独立接口(MII)、精简媒体独立接口(RMII)，符合IEEE802.3u标准
Functions	MagicPacketTM检测、Wake-on-LAN(WOL)信号输出



Note 1. When using the ETHERC, set the clock to ICLK = PCLKA.
12.5 MHz ≤ PCLKA ≤ 120 MHz.

Figure 29.1 ETHERC configuration



Note 1. 使用ETHERC时，将时钟设置为ICLK=PCLKA。12.5MHz≤PC
LKA≤120MHz。

Figure 29.1 ETHERC configuration

Table 29.2 ETHERC I/O pins

Operating mode	Pin name	I/O	Description
MII	ET0_TX_CLK *1	Input	Transmit clock Timing reference signal for outputting the ET0_TX_EN, ET0_ETXD3 to ET0_ETXD0, and ET0_TX_ER signals.
	ET0_RX_CLK *1	Input	Receive clock Timing reference signal for inputting the ET0_RX_DV, ET0_ERXD3 to ET0_ERXD0, and ET0_RX_ER signals.
	ET0_TX_EN *1	Output	Transmit data valid This signal indicates that valid transmit data was output on pins ET0_ETXD3 to ET0_ETXD0.
	ET0_ETXD3 to ET0_ETXD0 *1	Output	4-bit transmit data
	ET0_TX_ER *1	Output	Transmit error This signal notifies the PHY-LSI that an error occurred during transmission.
	ET0_RX_DV *1	Input	Receive data valid This signal indicates that valid receive data is on pins ET0_ERXD3 to ET0_ERXD0.
	ET0_ERXD3 to ET0_ERXD0 *1	Input	4-bit receive data
	ET0_RX_ER *1	Input	Receive error This signal indicates that there is an error in a frame that is being transferred from the PHY-LSI to the ETHERC.
	ET0_CRS *1	Input	Carrier sense
	ET0_COL *1	Input	Collision detection signal
	ET0_MDC *1	Output	Management data clock Reference clock signal for transfer of information on the ET0_MDIO pin.
	ET0_MDIO *1	I/O	Management data Input/Output Bidirectional data signal for exchanging management data with the PHY-LSI.
	ET0_LINKSTA	Input	Link status input from the PHY-LSI
	ET0_EXOUT	Output	General output pin
	ET0_WOL	Output	Wake-on-LAN. This signal indicates that a Magic Packet was received.
RMII	REF50CK0 *2	Input	Reference clock Timing reference signal for the RMII0_TXD_EN, RMII0_TXD1 to RMII0_TXD0, RMII0_CRS_DV, RMII0_RXD1 to RMII0_RXD0, and RMII0_RX_ER pins.
	RMII0_TXD_EN *2	Output	Transmit data valid This signal indicates that valid transmit data was output on the RMII0_TXD1 and RMII0_TXD0 pins.
	RMII0_TXD1 to RMII0_TXD0 *2	Output	2-bit transmit data
	RMII0_CRS_DV *2	Input	Carrier sense/receive data valid This signal indicates that valid receive data is on the RMII0_RXD1 and RMII0_RXD0 pins.
	RMII0_RXD1 to RMII0_RXD0 *2	Input	2-bit receive data
	RMII0_RX_ER *2	Input	Receive error This signal indicates that there is an error in a frame that is being transferred from the PHY-LSI to the ETHERC. See the note in section 29.5.2, Input to RMII0_RX_ER Pin while RMII Is Selected.
	ET0_MDC *2	Output	Management data clock Reference clock signal for transfer of information on the ET0_MDIO pin
	ET0_MDIO *2	I/O	Management data Input/Output Bidirectional data signal for exchanging management data with the PHY-LSI.
	ET0_LINKSTA	Input	Link status input from the PHY-LSI.
	ET0_EXOUT	Output	General output pin
	ET0_WOL	Output	Wake-on-LAN. This signal indicates that a Magic Packet was received.

Table 29.2 ETHERC I/O pins

操作模式	引脚名称	I/O	Description
MII	ET0_TX_CLK *1	Input	发送时钟 将ET0_TX_EN、ET0_ETXD3输出到的时序参考信号 ET0_ETXD0和ET0_TX_ER信号。
	ET0_RX_CLK *1	Input	接收时钟 将ET0_RX_DV、ET0_ERXD3输入到 ET0_ERXD0和ET0_RX_ER信号。
	ET0_TX_EN *1	Output	传输数据有效 该信号表示在ET0_ETXD3到ET0_ETXD0引脚上输出了有效的发送数据。
	ET0_ETXD3 to ET0_ETXD0 *1	Output	4位传输数据
	ET0_TX_ER *1	Output	传输错误 该信号通知PHY-LSI在传输过程中发生了错误。
	ET0_RX_DV *1	Input	接收数据有效 该信号表明有效的接收数据在引脚ET0_ERXD3到 ET0_ERXD0.
	ET0_ERXD3 to ET0_ERXD0 *1	Input	4位接收数据
	ET0_RX_ER *1	Input	接收错误 该信号表示从PHY-LSI传输到ETHERC的帧中存在错误。
	ET0_CRS *1	Input	载体感
	ET0_COL *1	Input	碰撞检测信号
	ET0_MDC *1	Output	管理数据时钟 用于在ET0_MDIO引脚上传输信息的参考时钟信号。
	ET0_MDIO *1	I/O	管理数据输入输出 用于与PHY-LSI交换管理数据的双向数据信号。
	ET0_LINKSTA	Input	来自PHY-LSI的链路状态输入
	ET0_EXOUT	Output	通用输出引脚
	ET0_WOL	Output	局域网唤醒。该信号表示收到了一个魔术包。
RMII	REF50CK0 *2	Input	参考时钟 RMII0_TXD_EN、RMII0_TXD1的时序参考信号 RMII0_TXD0、RMII0_CRS_DV、RMII0_RXD1至RMII0_RXD0，以及 RMII0_RX_ER pins.
	RMII0_TXD_EN *2	Output	传输数据有效 该信号表明在RMII0_TXD1和RMII0_TXD0引脚上输出了有效的发送数据。
	RMII0_TXD1 to RMII0_TXD0 *2	Output	2位传输数据
	RMII0_CRS_DV *2	Input	载波侦听接收数据有效 该信号表示有效的接收数据在RMII0_RXD1上，并且 RMII0_RXD0 pins.
	RMII0_RXD1 to RMII0_RXD0 *2	Input	2位接收数据
	RMII0_RX_ER *2	Input	接收错误 该信号表示从PHY-LSI传输到ETHERC的帧中存在错误。请参阅第29.5.2节“选择RMII时输入到RMII0_RX_ER引脚”中的注释。
	ET0_MDC *2	Output	管理数据时钟 用于在ET0_MDIO引脚上传输信息的参考时钟信号
	ET0_MDIO *2	I/O	管理数据输入输出 用于与PHY-LSI交换管理数据的双向数据信号。
	ET0_LINKSTA	Input	来自PHY-LSI的链路状态输入。
	ET0_EXOUT	Output	通用输出引脚
	ET0_WOL	Output	局域网唤醒。该信号表示收到了一个魔术包。

Note 1. MII signal compliant with IEEE802.3u.
Note 2. RMII signal compliant with IEEE802.3u.

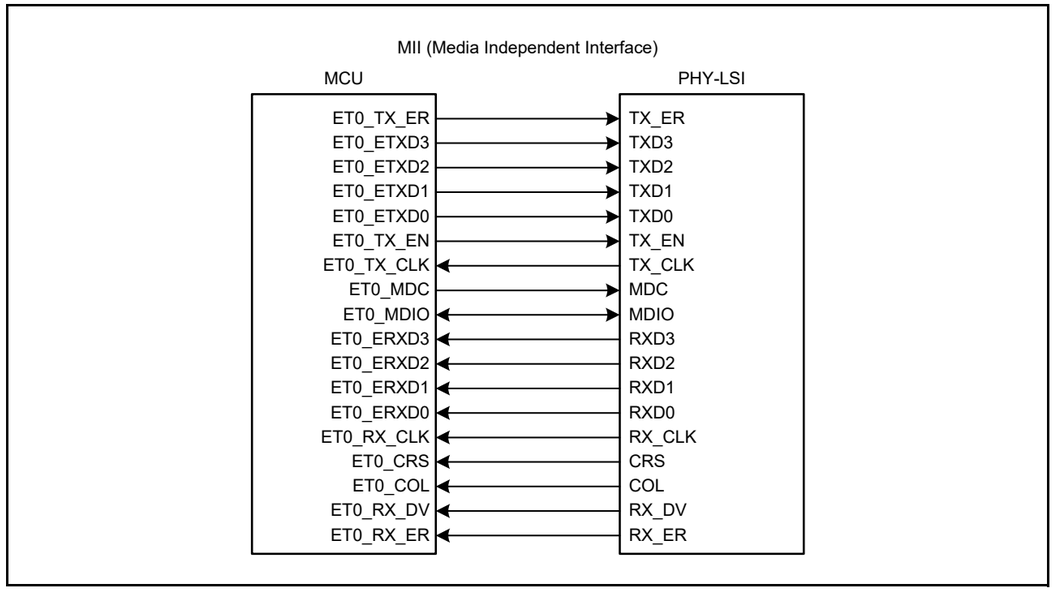


Figure 29.2 Example of connection with PHY-LSI for MII

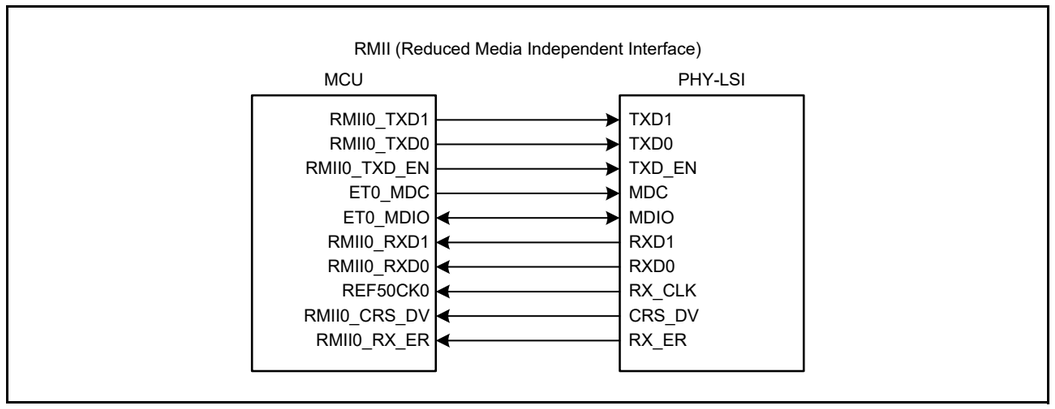


Figure 29.3 Example of connection with PHY-LSI for RMII

Note 1. 符合IEEE802.3u的MII信号。
Note 2. RMII信号符合IEEE802.3u。

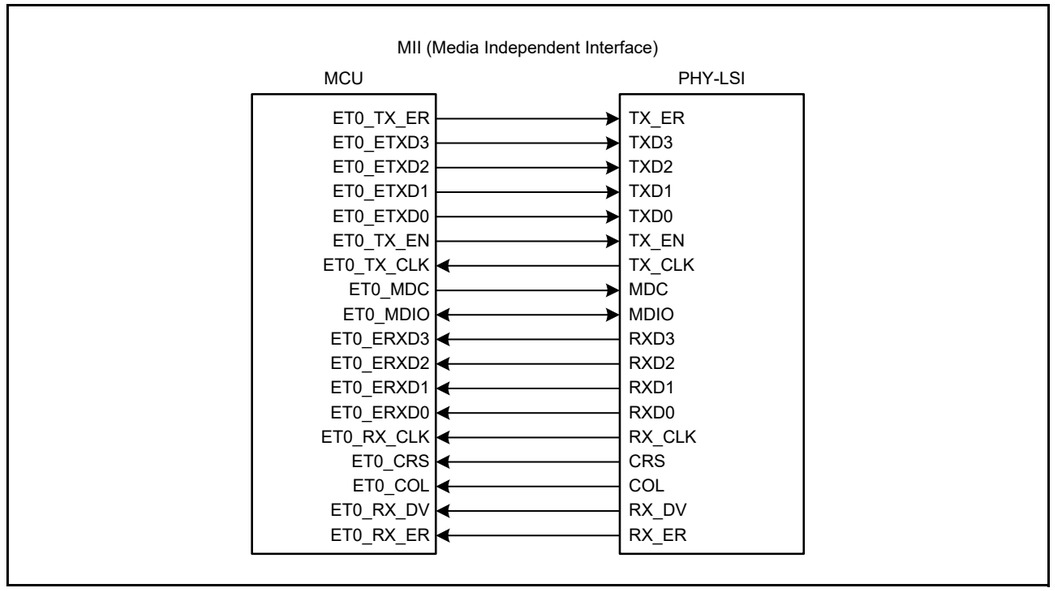


Figure 29.2 与MII用PHY-LSI的连接示例

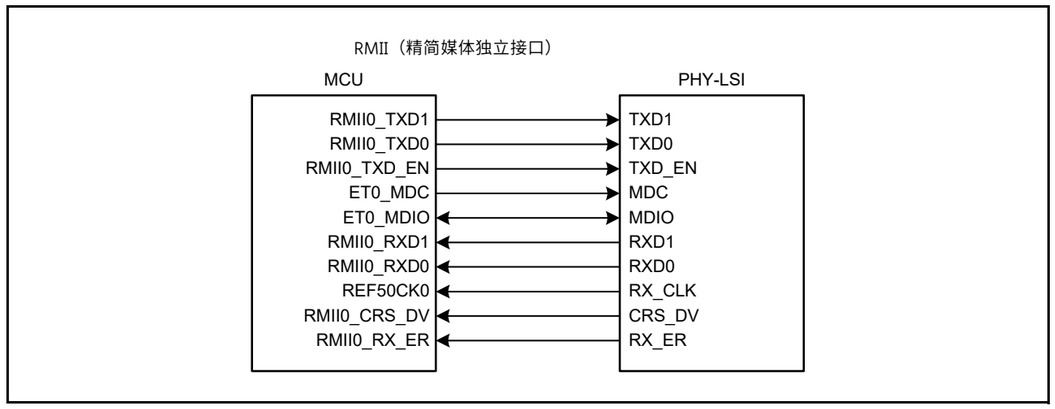


Figure 29.3 用于RMII的PHY-LSI连接示例

29.2 Register Descriptions

29.2.1 ETHERC Mode Register (ECMR)

Address(es): ETHERC0.ECMR 4006 4100h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	TPC	ZPF	PFR	RXF	TXF
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	PRCEF	—	—	MPDE	—	—	RE	TE	—	ILB	RTM	DM	PRM
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	PRM	Promiscuous Mode	0: Disable promiscuous mode 1: Enable promiscuous mode.	R/W
b1	DM	Duplex Mode	0: Half-duplex mode 1: Full-duplex mode.	R/W
b2	RTM	Bit Rate	0: 10 Mbps 1: 100 Mbps.	R/W
b3	ILB	Internal Loopback Mode	0: Perform normal data transmission or reception 1: Loop data back in the ETHERC when full-duplex mode is selected.	R/W
b4	—	Reserved	The read value is 0. The write value should be 0.	R/W
b5	TE	Transmission Enable	0: Disable transmit function 1: Enable transmit function.	R/W
b6	RE	Reception Enable	0: Disable receive function 1: Enable receive function.	R/W
b8, b7	—	Reserved	The read value is 0. The write value should be 0.	R/W
b9	MPDE	Magic Packet Detection Enable	0: Disable Magic Packet detection 1: Enable Magic Packet detection.	R/W
b11, b10	—	Reserved	The read value is 0. The write value should be 0.	R/W
b12	PRCEF	CRC Error Frame Receive Mode	0: Notify EDMAC of a CRC error 1: Do not notify EDMAC of a CRC error.	R/W
b15 to b13	—	Reserved	The read value is 0. The write value should be 0.	R/W
b16	TXF	Transmit Flow Control Operating Mode	0: Disable automatic PAUSE frame transmission (PAUSE frame is not automatically transmitted) 1: Enable automatic PAUSE frame transmission (PAUSE frame is automatically transmitted as required).	R/W
b17	RXF	Receive Flow Control Operating Mode	0: Disable PAUSE frame detection 1: Enable PAUSE frame detection.	R/W
b18	PFR	PAUSE Frame Receive Mode	0: Do not transfer PAUSE frame to the EDMAC 1: Transfer PAUSE frame to the EDMAC.	R/W
b19	ZPF	0 Time PAUSE Frame Enable	0: Do not use PAUSE frames that contain a pause_time parameter of 0 1: Use PAUSE frames that contains a pause_time parameter of 0.	R/W
b20	TPC	PAUSE Frame Transmit	0: Transmit PAUSE frame even during a PAUSE period 1: Do not transmit PAUSE frame during a PAUSE period.	R/W
b31 to b21	—	Reserved	The read value is 0. The write value should be 0.	R/W

The ECMR register controls ETHERC operation. Except for the TE and RE bits, set the bits in this register during initialization after a reset. When rewriting this register outside the initialization process, set the EDMAC0.EDMR.SWR bit to 1 to reset the EDMAC and ETHERC, then set this register again.

29.2 注册说明

29.2.1 ETHERC模式寄存器(ECMR)

Address(es): ETHERC0.ECMR 4006 4100h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	TPC	ZPF	PFR	RXF	TXF
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	PRCEF	—	—	MPDE	—	—	RE	TE	—	ILB	RTM	DM	PRM
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	PRM	混杂模式	0：禁用混杂模式1：启用混杂模式。	R/W
b1	DM	双工模式	0: Half-duplex mode 1: Full-duplex mode.	R/W
b2	RTM	比特率	0: 10 Mbps 1: 100 Mbps.	R/W
b3	ILB	内部环回模式	0：执行正常的数据发送或接收1：选择全双工模式时，在ETHERC中环回数据。	R/W
b4	—	Reserved	读取值为0。写入值应为0。	R/W
b5	TE	传输使能	0：关闭发送功能1：开启发送功能。	R/W
b6	RE	接收启用	0：关闭接收功能1：开启接收功能。	R/W
b8, b7	—	Reserved	读取值为0。写入值应为0。	R/W
b9	MPDE	魔术包检测 Enable	0：禁用魔包检测1：启用魔包检测。	R/W
b11, b10	—	Reserved	读取值为0。写入值应为0。	R/W
b12	PRCEF	CRC错误帧接收 Mode	0：通知EDMACCRC错误1：不通知EDMACCRC错误。	R/W
b15 to b13	—	Reserved	读取值为0。写入值应为0。	R/W
b16	TXF	传输流控制 操作模式	0：禁用自动PAUSE帧传输（不自动传输PAUSE帧）1：启用自动PAUSE帧传输（PAUSE帧根据需要自动发送）。	R/W
b17	RXF	接收流控制 操作模式	0：禁用PAUSE帧检测1：启用PAUSE帧检测。	R/W
b18	PFR	PAUSE帧接收模式	0：不向EDMAC传输PAUSE帧1：向EDMAC传输PAUSE帧。	R/W
b19	ZPF	0时间PAUSE帧启用	0：不使用包含pause_time参数的PAUSE帧 01：使用包含pause_time参数为0的PAUSE帧。	R/W
b20	TPC	PAUSE帧发送	0：即使在PAUSE期间也发送PAUSE帧1：在PAUSE期间不发送PAUSE帧。	R/W
b31 to b21	—	Reserved	读取值为0。写入值应为0。	R/W

ECMR寄存器控制ETHERC操作。除TE和RE位外，在复位后初始化期间设置此寄存器中的位。在初始化过程之外重写该寄存器时，将EDMAC0.EDMR.SWR位设置为1以复位EDMAC和ETHERC，然后再次设置该寄存器。

PRM bit (Promiscuous Mode)

When the PRM bit is set to 1, the ETHERC operates in promiscuous mode, where all Ethernet frames are received. In promiscuous mode, the ETHERC receives all valid frames regardless of whether the address matches the destination or broadcast address and regardless of the multicast bit setting.

RTM bit (Bit Rate)

The RTM bit sets the bit rate when the RMII is selected.

ILB bit (Internal Loopback Mode)

When the ILB bit is set to 1, transmit frames can be looped back in the MCU. Set the DM bit to 1 (full-duplex mode) to perform a loopback test.

TE bit (Transmission Enable)

When the TE bit is set to 1, the ETHERC transmit function is enabled. When the TE bit is set to 0, the transmit function is disabled after the frame being processed is completely transmitted.

RE bit (Reception Enable)

When the RE bit is set to 1, the ETHERC receive function is enabled. When the RE bit is set to 0, the receive function is disabled after the frame being processed is completely received.

PRCEF bit (CRC Error Frame Receive Mode)

When the PRCEF bit is set to 1, the EDMAC is not notified that a CRC error has occurred even when the error is detected in a receive frame. Accordingly, the EDMAC0.EESR.CERF flag and RFS0 bit in receive descriptor 0 (RD0) do not become 1.

ZPF bit (0 Time PAUSE Frame Enable)

When the ZPF bit is 1, a PAUSE frame with a pause_time parameter of 0 is transmitted when a PAUSE frame transmit request is canceled before the PAUSE time of the previously transmitted PAUSE frame has elapsed. After the PAUSE frame containing the pause_time parameter of 0 is received, the ETHERC is ready for transmission.

When the ZPF bit is 0, even if the PAUSE frame transmit request from the receive FIFO is canceled, the next PAUSE frame is not transmitted until the PAUSE time of the previously transmitted PAUSE frame has elapsed. When a PAUSE frame containing a pause_time parameter of 0 is received, it is discarded.

PRM位（混杂模式）

当PRM位设置为1时，ETHERC以混杂模式运行，其中接收所有以太网帧。在混杂模式下，ETHERC接收所有有效帧，无论地址是否匹配目标地址或广播地址，也无论多播位设置如何。

RTM位（比特率）

选择RMII时，RTM位设置了比特率。

ILB位（内部环回模式）

当ILB位设置为1时，发送帧可以在MCU中环回。将DM位设置为1（全双工模式）以执行环回测试。

TE位（传输使能）

当TE位设置为1时，使能ETHERC发送功能。当TE位设置为0时，正在处理的帧发送完毕后，发送功能被禁用。

RE位（接收使能）

当RE位设置为1时，使能ETHERC接收功能。当RE位设置为0时，接收功能在正在处理的帧被完全接收后被禁用。

PRCEF位（CRC错误帧接收模式）

当PRCEF位设置为1时，即使在接收帧中检测到错误，也不通知EDMAC发生CRC错误。因此，接收描述符0(RD0)中的EDMAC0.EESR.CERF标志和RFS0位不会变为1。

ZPF位（0时间暂停帧使能）

当ZPF位为1时，如果在先前发送的PAUSE帧的PAUSE时间过去之前取消PAUSE帧发送请求，则发送一个pause_time参数为0的PAUSE帧。在接收到包含pause_time参数为0的PAUSE帧后，ETHERC准备好传输。

当ZPF位为0时，即使来自接收FIFO的PAUSE帧发送请求被取消，直到前一个发送的PAUSE帧的PAUSE时间过去后，下一个PAUSE帧才会发送。当接收到包含pause_time参数为0的PAUSE帧时，将其丢弃。

29.2.2 Receive Frame Maximum Length Register (RFLR)

Address(es): ETHERC0.RFLR 4006 4108h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	RFL[11:0]											
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b11 to b0	RFL[11:0]	Receive Frame Maximum Length	The set value becomes the maximum frame length. The minimum value that can be set is 1,518 bytes, and the maximum value that can be set is 2,048 bytes. Values less than 1,518 bytes are regarded as 1,518 bytes, and values larger than 2,048 bytes are regarded as 2,048 bytes.	R/W
b31 to b12	—	Reserved	The read value is 0. The write value should be 0.	R/W

The RFLR register specifies the maximum frame length that can be received by the MCU. Set the length in bytes. Do not rewrite this register while the ECMR.RE bit is 1 (receive function enabled).

RFL[11:0] bits (Receive Frame Maximum Length)

The RFL[11:0] bits set the frame length to be checked. The frame length is the number of bytes in a field, extending from the destination address to the frame check sequence [FCS] of the received frame. When this length exceeds the RFL[11:0] bit value, the EDMAC is notified of a frame-too-long error, and the excess data is discarded.

29.2.2 接收帧最大长度寄存器(RFLR)

Address(es): ETHERC0.RFLR 4006 4108h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	RFL[11:0]											
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b11 to b0	RFL[11:0]	接收帧最大值 Length	设定值成为最大帧长。可设置的最小值为1 518字节，可设置的最大值为2 048字节。小于1 518字节的值被视为1 518字节，大于2 048字节的值被视为2 048字节。	R/W
b31 to b12	—	Reserved	读取值为0。写入值应为0。	R/W

RFLR寄存器指定MCU可以接收的最大帧长度。以字节为单位设置长度。当ECMR.RE位为1（启用接收功能）时不要重写该寄存器。

RFL[11:0]位（接收帧最大长度）

RFL[11:0]位设置要检查的帧长度。帧长度是一个字段中的字节数，从目标地址延伸到接收帧的帧校验序列[FCS]。当此长度超过RFL[11:0]位值时，EDMAC会收到帧太长错误的通知，并丢弃多余的数据。

29.2.3 ETHERC Status Register (ECSR)

Address(es): ETHERC0.ECSR 4006 4110h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	BFR	PSRTO	—	LCHNG	MPD	ICD
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	ICD	False Carrier Detect Flag	0: PHY-LSI has not detected a false carrier on the line 1: PHY-LSI detected a false carrier on the line.	R/W *1
b1	MPD	Magic Packet Detect Flag	0: Magic Packet not detected 1: Magic Packet detected.	R/W *1
b2	LCHNG	Link Signal Change Flag	0: Change in the ET0_LINKSTA signal not detected 1: Change in the ET0_LINKSTA signal detected (high to low, or low to high).	R/W *1
b3	—	Reserved	The read value is 0. The write value should be 0.	R/W
b4	PSRTO	PAUSE Frame Retransmit Over Flag	0: PAUSE frame retransmit count has not reached the upper limit 1: PAUSE frame retransmit count reached the upper limit.	R/W *1
b5	BFR	Continuous Broadcast Frame Reception Flag	0: Continuous reception of broadcast frames not detected 1: Continuous reception of broadcast frames detected.	R/W *1
b31 to b6	—	Reserved	The read value is 0. The write value should be 0.	R/W

Note 1. Write 1 to clear the flag.

The ECSR register indicates the status of the ETHERC. When any flag in the ECSR register is set to 1 while the associated bit in the ECSIPR register is 1 (interrupt enabled), the EDMAC0.EESR.ECI flag is set to 1.

ICD flag (False Carrier Detect Flag)

The ICD flag indicates that the PHY-LSI has detected a false carrier on the line. The flag is set to 1 when a receive error signal shown in Figure 29.11 is received from the PHY-LSI. The information might not be correct when signals input from the PHY-LSI change faster than software recognizes the change. Check the timing of the PHY-LSI.

LCHNG flag (Link Signal Change Flag)

The LCHNG flag indicates that the ET0_LINKSTA signal input from the PHY-LSI has changed from high to low, or from low to high. Check the PSR.LMON flag for the current link status. See section 29.5.1, Preventing the LCHNG Flag from Erroneously Setting to 1 for more information.

PSRTO flag (PAUSE Frame Retransmit Over Flag)

The PSRTO flag indicates that the number of retransmissions reached the value set in the TPAUSER register when retransmitting a PAUSE frame while automatic PAUSE frame transmission is enabled.

29.2.3 ETHERC状态寄存器(ECSR)

Address(es): ETHERC0.ECSR 4006 4110h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	BFR	PSRTO	—	LCHNG	MPD	ICD
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	ICD	错误载波检测标志	0：PHY-LSI未检测到线路上的虚假载波1：PHY-LSI检测到线路上的虚假载波。	R/W *1
b1	MPD	魔术包检测标志	0：未检测到魔术包1：检测到魔术包。	R/W *1
b2	LCHNG	链路信号变化标志	0：未检测到ET0_LINKSTA信号变化1：检测到ET0_LINKSTA信号变化（从高到低，或从低到高）。	R/W *1
b3	—	Reserved	读取值为0。写入值应为0。	R/W
b4	PSRTO	暂停帧重传过旗	0：PAUSE帧重传计数未达到上限1：PAUSE帧重传计数达到上限。	R/W *1
b5	BFR	连续广播帧接收标志	0：未检测到连续接收广播帧1：检测到连续接收广播帧。	R/W *1
b31 to b6	—	Reserved	读取值为0。写入值应为0。	R/W

Note 1. 写1清除标志。

ECSR寄存器指示ETHERC的状态。当ECSR寄存器中的任何标志设置为1且ECSIPR寄存器中的相关位为1（允许中断）时，EDMAC0.EESR.ECI标志设置为1。

ICD标志（假载波检测标志）

ICD标志表示PHY-LSI检测到线路上的错误载波。当从PHY-LSI接收到图29.11所示的接收错误信号时，该标志设置为1。当来自PHY-LSI的信号输入变化快于软件识别变化的速度时，该信息可能不正确。检查PHY-LSI的时序。

LCHNG标志（链路信号变化标志）

LCHNG标志表示从PHY-LSI输入的ET0_LINKSTA信号已由高变为低，或由低变为高。检查当前链接状态的PSR.LMON标志。有关详细信息，请参阅第29.5.1节，防止LCHNG标志错误地设置为1。

PSRTO标志（暂停帧重传标志）

PSRTO标志表示在启用自动PAUSE帧传输时重传PAUSE帧时重传次数达到TPAUSER寄存器中设置的值。

29.2.4 ETHERC Interrupt Enable Register (ECSIPR)

Address(es): ETHERC0.ECSIPR 4006 4118h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	BFSIPR	PSRTOIP	—	LCHNGIP	MPDIP	ICDIP
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	ICDIP	False Carrier Detect Interrupt Enable	0: Disable interrupt notification 1: Enable interrupt notification.	R/W
b1	MPDIP	Magic Packet Detect Interrupt Enable	0: Disable interrupt notification 1: Enable interrupt notification.	R/W
b2	LCHNGIP	LINK Signal Change Interrupt Enable	0: Disable interrupt notification 1: Enable interrupt notification.	R/W
b3	—	Reserved	The read value is 0. The write value should be 0.	R/W
b4	PSRTOIP	PAUSE Frame Retransmit Over Interrupt Enable	0: Disable interrupt notification 1: Enable interrupt notification.	R/W
b5	BFSIPR	Continuous Broadcast Frame Reception Interrupt Enable	0: Disable interrupt notification 1: Enable interrupt notification.	R/W
b31 to b6	—	Reserved	The read value is 0. The write value should be 0.	R/W

The ECSIPR register selects whether to notify the EDMAC of the status indicated in the ECSR register. Each bit is associated with the flag with the same bit number in the ECSR register.

29.2.4 ETHERC中断使能寄存器(ECSIPR)

Address(es): ETHERC0.ECSIPR 4006 4118h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	BFSIPR	PSRTOIP	—	LCHNGIP	MPDIP	ICDIP
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	ICDIP	假载波检测中断使能	0：禁用中断通知1：启用中断通知。	R/W
b1	MPDIP	魔术包检测中断使能	0：禁用中断通知1：启用中断通知。	R/W
b2	LCHNGIP	LINK信号变化中断使能	0：禁用中断通知1：启用中断通知。	R/W
b3	—	Reserved	读取值为0。写入值应为0。	R/W
b4	PSRTOIP	PAUSE帧重传结束中断使能	0：禁用中断通知1：启用中断通知。	R/W
b5	BFSIPR	连续广播帧接收中断使能	0：禁用中断通知1：启用中断通知。	R/W
b31 to b6	—	Reserved	读取值为0。写入值应为0。	R/W

ECSIPR寄存器选择是否将ECSR寄存器中指示的状态通知EDMAC。每个位都与ECSR寄存器中具有相同位号的标志相关联。

29.2.5 PHY Interface Register (PIR)

Address(es): ETHERC0.PIR 4006 4120h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	MDI	MDO	MMD	MDC
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	x	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	MDC	MII/RMII Management Data Clock	This value is output from the ET0_MDC pin to supply the management data clock to the MII or RMII.	R/W
b1	MMD	MII/RMII Management Mode	0: Read 1: Write.	R/W
b2	MDO	MII/RMII Management Data-Out	This value is output from the ET0_MDIO pin when the MMD bit is 1 (write), and not when MMD is 0 (read).	R/W
b3	MDI	MII/RMII Management Data-In	This bit indicates the level of the ET0_MDIO pin. The write value should be 0.	R
b31 to b4	—	Reserved	The read value is 0. The write value should be 0.	R/W

The PIR register accesses registers in the PHY-LSI through the MII or RMII. The management clock and management data are controlled by software. See section 29.3.4, Accessing the MII and RMII Registers for details on accessing the MII and RMII registers.

29.2.6 PHY Status Register (PSR)

Address(es): ETHERC0.PSR 4006 4128h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	LMON
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	x

Bit	Symbol	Bit name	Description	R/W
b0	LMON	ET0_LINKSTA Pin Status Flag	The link status can be read by connecting the link signal output from the PHY-LSI to the ET0_LINKSTA pin. For details on the polarity, see the specifications of the connected PHY-LSI.	R
b31 to b1	—	Reserved	The read value is 0.	R

The PSR register monitors interface signals from the PHY-LSI.

29.2.5 PHY接口寄存器(PIR)

Address(es): ETHERC0.PIR 4006 4120h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	MDI	MDO	MMD	MDC
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	x	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	MDC	MII/RMII Management 数据时钟	该值从ET0_MDC引脚输出，为MII或RMII提供管理数据时钟。	R/W
b1	MMD	MII/RMII Management Mode	0：读取1 ：写入。	R/W
b2	MDO	MII/RMII Management Data-Out	该值在MMD位为1（写入）时从ET0_MDIO引脚输出，而不是在MMD为0（读取）时输出。	R/W
b3	MDI	MII/RMII Management Data-In	该位指示ET0_MDIO引脚的电平。写入值应为0。	R
b31 to b4	—	Reserved	读取值为0。写入值应为0。	R/W

PIR寄存器通过MII或RMII访问PHY-LSI中的寄存器。管理时钟和管理数据由软件控制。有关访问MII和RMII寄存器的详细信息，请参见第29.3.4节，访问MII和RMII寄存器。

29.2.6 PHY状态寄存器(PSR)

Address(es): ETHERC0.PSR 4006 4128h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	LMON
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	x

Bit	Symbol	位名称	Description	R/W
b0	LMON	ET0_LINKSTA Pin 状态标志	链接状态可以通过连接从输出的链接信号读取PHY-LSI连接到ET0_LINKSTA引脚。有关极性的详细信息，请参阅所连接的PHY-LSI的规格。	R
b31 to b1	—	Reserved	读取值为0。	R

PSR寄存器监视来自PHY-LSI的接口信号。

29.2.7 Random Number Generation Counter Upper Limit Setting Register (RDMLR)

Address(es): ETHERC0.RDMLR 4006 4140h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	RMD[19:16]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RMD[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b19 to b0	RMD[19:0]	Random Number Generation Counter	00000h: Normal operation 00001h to FFFFFh: Setting prohibited.	R/W
b31 to b20	—	Reserved	The read value is 0. The write value should be 0.	R/W

The RDMLR register specifies the maximum value for the counter used in the random number generator. Do not rewrite this register while the ECMR.TE bit is 1 (transmit function enabled) or while the ECMR.RE bit is 1 (receive function enabled).

29.2.8 Interpacket Gap Register (IPGR)

Address(es): ETHERC0.IPGR 4006 4150h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	IPG[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0

Bit	Symbol	Bit name	Description	R/W
b4 to b0	IPG[4:0]	Interpacket Gap	00h: 16 bit times 01h: 20 bit times : : 14h: 96 bit times (initial value) : : 1Fh: 140 bit times.	R/W
b31 to b5	—	Reserved	The read value is 0. The write value should be 0.	R/W

The IPGR register specifies the interpacket gap (IPG) value. Do not rewrite this register while the ECMR.TE bit is 1 (transmit function enabled) or while the ECMR.RE bit is 1 (receive function enabled). See section 29.3.6, Adjusting Transmission Efficiency by Changing the IPG for details on the IPG.

29.2.7 随机数生成计数器上限设置寄存器(RDMLR)

Address(es): ETHERC0.RDMLR 4006 4140h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	RMD[19:16]			
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RMD[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b19 to b0	RMD[19:0]	随机数生成 Counter	00000h：正常运行00001h至FFFFFh ：禁止设置。	R/W
b31 to b20	—	Reserved	读取值为0。写入值应为0。	R/W

RDMLR寄存器指定随机数发生器中使用的计数器的最大值。当ECMR.TE位为1（启用发送功能）或ECMR.RE位为1（启用接收功能）时，请勿重写此寄存器。

29.2.8 包间间隙寄存器(IPGR)

Address(es): ETHERC0.IPGR 4006 4150h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	IPG[4:0]				
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0

Bit	Symbol	位名称	Description	R/W
b4 to b0	IPG[4:0]	Interpacket Gap	00h:16位时间01h:20位时间:: 14h:96位时间（初始值）::1F h:140位时间。	R/W
b31 to b5	—	Reserved	读取值为0。写入值应为0。	R/W

IPGR寄存器指定包间间隙(IPG)值。当ECMR.TE位为1（启用发送功能）或ECMR.RE位为1（启用接收功能）时，请勿重写此寄存器。有关IPG的详细信息，请参见第29.3.6节，通过更改IPG调整传输效率。

29.2.9 Automatic PAUSE Frame Register (APR)

Address(es): ETHERC0.APR 4006 4154h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	AP[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b15 to b0	AP[15:0]	Automatic PAUSE Time Setting	These bits set the value of the pause_time parameter for PAUSE frames that are automatically transmitted. Transmission is not performed until the set value multiplied by 512 bit times has elapsed.	R/W
b31 to b16	—	Reserved	The read value is 0. The write value should be 0.	R/W

The APR register specifies the PAUSE time for PAUSE frames that are automatically transmitted. The value set in the APR register is used for the pause_time parameter of the PAUSE frame. Do not rewrite this register while the ECMR.TE bit is 1 (transmit function enabled) or while the ECMR.RE bit is 1 (receive function enabled).

29.2.10 Manual PAUSE Frame Register (MPR)

Address(es): ETHERC0.MPR 4006 4158h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MP[15:0]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Bit	Symbol	Bit name	Description	R/W
b15 to b0	MP[15:0]	Manual PAUSE Time Setting	These bits set the value of the pause_time parameter for PAUSE frames that are manually transmitted. Transmission is not performed until the set value multiplied by 512 bit times has elapsed. The read value is undefined.	W
b31 to b16	—	Reserved	The read value is 0. The write value should be 0.	W

The MPR register specifies the PAUSE time for PAUSE frames that are manually transmitted. The value set in the MPR register is used for the pause_time parameter of the PAUSE frame. When a value is set to this register, a PAUSE frame is transmitted. Rewrite this register while the ECMR.TE bit is 1 (transmit function enabled).

29.2.9 自动暂停帧寄存器(APR)

Address(es): ETHERC0.APR 4006 4154h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	AP[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b15 to b0	AP[15:0]	自动暂停时间设定	这些位为自动传输的PAUSE帧设置pause_time参数的值。在设定值乘以512位时间之前，不执行传输。	R/W
b31 to b16	—	Reserved	读取值为0。写入值应为0。	R/W

APR寄存器指定自动发送的暂停帧的暂停时间。中设置的值
APR寄存器用于PAUSE帧的pause_time参数。当ECMR.TE位为1（启用发送功能）或ECMR.RE位为1（启用接收功能）时，请勿重写此寄存器。

29.2.10 手动暂停帧寄存器(MPR)

Address(es): ETHERC0.MPR 4006 4158h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MP[15:0]															
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Bit	Symbol	位名称	Description	R/W
b15 to b0	MP[15:0]	手动暂停时间 Setting	这些位为手动传输的PAUSE帧设置pause_time参数的值。在设定值乘以512位时间之前，不执行传输。读取值未定义。	W
b31 to b16	—	Reserved	读取值为0。写入值应为0。	W

MPR寄存器指定手动发送的暂停帧的暂停时间。MPR寄存器中设置的值用于PAUSE帧的pause_time参数。当一个值被设置到这个寄存器时，一个暂停帧被发送。当ECMR.TE位为1（启用发送功能）时重写该寄存器。

29.2.11 Received PAUSE Frame Counter (RFCF)

Address(es): ETHERC0.RFCF 4006 4160h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	RPAUSE[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	RPAUSE[7:0]	Received PAUSE Frame Count	Number of received PAUSE frames.	R
b31 to b8	—	Reserved	The read value is 0.	R

The RFCF register is a counter that indicates the number of received PAUSE frames. The counter is reset after this register is read.

29.2.12 PAUSE Frame Retransmit Count Setting Register (TPAUSER)

Address(es): ETHERC0.TPAUSER 4006 4164h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TPAUSE[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b15 to b0	TPAUSE[15:0]	Automatic PAUSE Frame Retransmit Setting	0000h: Number of retransmissions is unlimited 0001h: Maximum number of retransmissions is 1 : : FFFFh: Maximum number of retransmissions is 65,535.	R/W
b31 to b16	—	Reserved	The read value is 0. The write value should be 0.	R/W

The TPAUSER register selects the maximum number of times a PAUSE frame is automatically transmitted. Do not rewrite this register while the ECMR.TE bit is 1 (transmit function enabled).

29.2.11 接收暂停帧计数器(RFCF)

Address(es): ETHERC0.RFCF 4006 4160h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	RPAUSE[7:0]							
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b7 to b0	RPAUSE[7:0]	接收暂停帧计数	接收到的暂停帧数。	R
b31 to b8	—	Reserved	读取值为0。	R

RFCF寄存器是一个计数器，用于指示接收到的PAUSE帧的数量。读取该寄存器后计数器复位。

29.2.12 PAUSE帧重传计数设置寄存器(TPAUSER)

Address(es): ETHERC0.TPAUSER 4006 4164h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TPAUSE[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b15 to b0	TPAUSE[15:0]	自动暂停帧重传 Setting	0000h：重发次数不受限制0001h：最大重发次数为1::FFFFh：最大重发次数为65 535。	R/W
b31 to b16	—	Reserved	读取值为0。写入值应为0。	R/W

TPAUSER寄存器选择自动发送PAUSE帧的最大次数。当ECMR.TE位为1（启用发送功能）时不要重写该寄存器。

29.2.13 PAUSE Frame Retransmit Counter (TPAUSECR)

Address(es): ETHERC0.TPAUSECR 4006 4168h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	TXP[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	TXP[7:0]	PAUSE Frame Retransmit Count	Number of times a PAUSE frame was retransmitted.	R
b31 to b8	—	Reserved	The read value is 0.	R

The TPAUSECR register is a counter that indicates the number of times a PAUSE frame was automatically retransmitted. The counter is reset after this register is read.

29.2.14 Broadcast Frame Receive Count Setting Register (BCFRR)

Address(es): ETHERC0.BCFRR 4006 416Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BCF[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b15 to b0	BCF[15:0]	Broadcast Frame Continuous Receive Count Setting	0000h: Number of receptions is unlimited 0001h: Receive 1 frame. : : FFFFh: Receive 65,535 frames.	R/W
b31 to b16	—	Reserved	The read value is 0. The write value should be 0.	R/W

The BCFRR register specifies the number of times broadcast frames can be received continuously. When the number of received frames exceeds the BCF[15:0] bit value, the excess broadcast frames are discarded. Do not rewrite this register while the EMCR.RE bit is 1 (receive function enabled).

29.2.13 暂停帧重传计数器(TPAUSECR)

Address(es): ETHERC0.TPAUSECR 4006 4168h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	TXP[7:0]							
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b7 to b0	TXP[7:0]	暂停帧 重传计数	重传PAUSE帧的次数。	R
b31 to b8	—	Reserved	读取值为0。	R

TPAUSECR寄存器是一个计数器，指示暂停帧自动重传的次数。读取该寄存器后计数器复位。

29.2.14 广播帧接收计数设置寄存器(BCFRR)

Address(es): ETHERC0.BCFRR 4006 416Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BCF[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b15 to b0	BCF[15:0]	广播帧连续 接收计数设置	0000h：接收次数不受限制0001h：接收1帧。::FFFFh：接收65 535帧。	R/W
b31 to b16	—	Reserved	读取值为0。写入值应为0。	R/W

BCFRR寄存器指定可以连续接收广播帧的次数。当接收到的帧数超过BCF[15:0]位值时，多余的广播帧将被丢弃。当EMCR.RE位为1（启用接收功能）时，请勿重写此寄存器。

29.2.15 MAC Address Upper Bit Register (MAHR)

Address(es): ETHERC0.MAHR 4006 41C0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b31 to b0	MAHR[31:0]	MAC Address Upper Bit	See the description following this table	R/W

The MAHR register specifies the upper 32 bits ([47:16]) of the 48-bit MAC address. For example, if the MAC address is 01-23-45-67-89-AB, set the register to 0123 4567h.

Set the MAHR register during initialization after a reset. Do not rewrite this register while the ECMR.TE bit is 1 (transmit function enabled) or while the ECMR.RE bit is 1 (receive function enabled). When rewriting this register, set the EDMAC0.EDMR.SWR bit to 1 to reset the EDMAC and ETHERC, then set this register again.

29.2.16 MAC Address Lower Bit Register (MALR)

Address(es): ETHERC0.MALR 4006 41C8h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MALR[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b15 to b0	MALR[15:0]	MAC Address Lower Bit	These bits set the lower 16 bits of the MAC address	R/W
b31 to b16	—	Reserved	The read value is 0. The write value should be 0.	R/W

The MALR register specifies the lower 16 bits of the 48-bit MAC address. For example, if the MAC address is 01-23-45-67-89-AB, set the register to 0000 89ABh.

Set the MALR register during initialization after a reset. Do not rewrite this register while the ECMR.TE bit is 1 (transmit function enabled) or while the ECMR.RE bit is 1 (receive function enabled). When rewriting this register, set the EDMAC0.EDMR.SWR bit to 1 to reset the EDMAC and ETHERC, then set this register again.

29.2.15 MAC地址高位寄存器(MAHR)

Address(es): ETHERC0.MAHR 4006 41C0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b31 to b0	MAHR[31:0]	MAC地址高位	请参阅此表后面的说明	R/W

MAHR寄存器指定48位MAC地址的高32位([47:16])。例如，如果MAC地址为01-23-45-67-89-AB，则将寄存器设置为01234567h。

在复位后初始化期间设置MAHR寄存器。当ECMR.TE位为1（启用发送功能）或ECMR.RE位为1（启用接收功能）时，请勿重写此寄存器。重写该寄存器时，将EDMAC0.EDMR.SWR位设置为1以复位EDMAC和ETHERC，然后再次设置该寄存器。

29.2.16 MAC地址低位寄存器（MALR）

Address(es): ETHERC0.MALR 4006 41C8h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MALR[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b15 to b0	MALR[15:0]	MAC地址低位	这些位设置MAC地址的低16位	R/W
b31 to b16	—	Reserved	读取值为0。写入值应为0。	R/W

MALR寄存器指定48位MAC地址的低16位。例如，如果MAC地址为01-23-4567-89-AB，则将寄存器设置为000089ABh。

在复位后初始化期间设置MALR寄存器。当ECMR.TE位为1（启用发送功能）或ECMR.RE位为1（启用接收功能）时，请勿重写此寄存器。重写该寄存器时，将EDMAC0.EDMR.SWR位设置为1以复位EDMAC和ETHERC，然后再次设置该寄存器。

29.2.17 Transmit Retry Over Counter Register (TROCR)

Address(es): ETHERC0.TROCR 4006 41D0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b31 to b0	TROCR[31:0]	Transmit Retry Over Counter	See the description following this table	R/W

The TROCR register is a counter that indicates the number of frames that failed to be retransmitted. The register is incremented by 1 when a frame fails to be retransmitted 15 times. The counter stops when the register value becomes FFFF FFFFh. Writing any value to the TROCR register clears the counter value to 0.

29.2.18 Late Collision Detect Counter Register (CDCR)

Address(es): ETHERC0.CDCR 4006 41D4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b31 to b0	CDCR[31:0]	Late Collision Detect Counter	See the description following this table	R/W

The CDCR register is a counter that indicates the number of late collisions that are detected after transmission starts. When the register value becomes FFFF FFFFh, the counter stops. Writing any value to the CDCR register clears the counter value to 0.

29.2.17 发送重试计数器寄存器(TROCR)

Address(es): ETHERC0.TROCR 4006 41D0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b31 to b0	TROCR[31:0]	传输重试 Counter	请参阅此表后面的说明	R/W

TROCR寄存器是一个计数器，用于指示重传失败的帧数。当一帧重传15次失败时，寄存器加1。当寄存器值变为FFFFFFFFh时，计数器停止。向TR OCR寄存器写入任何值都会将计数器值清除为0。

29.2.18 后期碰撞检测计数器寄存器(CDCR)

Address(es): ETHERC0.CDCR 4006 41D4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b31 to b0	CDCR[31:0]	后期碰撞检测 Counter	请参阅此表后面的说明	R/W

CDCR寄存器是一个计数器，用于指示在传输开始后检测到的后期冲突数。当寄存器值变为FFFFFFFFh时，计数器停止。向CDCR寄存器写入任何值都会将计数器值清零。

29.2.19 Lost Carrier Counter Register (LCCR)

Address(es): ETHERC0.LCCR 4006 41D8h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b31 to b0	LCCR[31:0]	Lost Carrier Counter	See the description following this table	R/W

The LCCR register is a counter that indicates the number of times a loss of carrier is detected during frame transmission. When the register value becomes FFFF FFFFh, the counter stops. Writing any value to the LCCR register clears the counter value to 0.

29.2.20 Carrier Not Detect Counter Register (CNDCR)

Address(es): ETHERC0.CNDCR 4006 41DCh

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b31 to b0	CNDCR[31:0]	Carrier Not Detect Counter	See the description following this table	R/W

The CNDCR register is a counter that indicates the number of times a carrier is not detected during preamble transmission. When the register value becomes FFFF FFFFh, the counter stops. Writing any value to the CNDCR register clears the counter value to 0.

29.2.19 丢失载波计数器寄存器(LCCR)

Address(es): ETHERC0.LCCR 4006 41D8h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b31 to b0	LCCR[31:0]	遗失承运人柜台	请参阅此表后面的说明	R/W

LCCR寄存器是一个计数器，用于指示在帧传输期间检测到载波丢失的次数。
当寄存器值变为FFFFFFFFh时，计数器停止。向LCCR寄存器写入任何值都会将计数器值清零。

29.2.20 载波未检测计数器寄存器(CNDCR)

Address(es): ETHERC0.CNDCR 4006 41DCh

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b31 to b0	CNDCR[31:0]	未检测到运营商 Counter	请参阅此表后面的说明	R/W

CNDCR寄存器是一个计数器，指示在前导码传输期间未检测到载波的次数。当寄存器值变为FFFFFFFFh时，计数器停止。向CNDCR寄存器写入任何值都会将计数器值清除为0。

29.2.21 CRC Error Frame Receive Counter Register (CEFCR)

Address(es): ETHERC0.CEFCR 4006 41E4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b31 to b0	CEFCR[31:0]	CRC Error Frame Receive Counter	See the description following this table	R/W

The CEFCR register is a counter that indicates the number of received frames in which a CRC error was detected. When the register value becomes FFFF FFFFh, the counter stops. Writing any value to the CEFCR register clears the counter value to 0.

29.2.22 Frame Receive Error Counter Register (FRECR)

Address(es): ETHERC0.FRECR 4006 41E8h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b31 to b0	FRECR[31:0]	Frame Receive Error Counter	See the description following this table	R/W

The FRECR register is a counter that indicates the number of times a frame receive error has occurred. The PHY-LSI notifies the ETHERC of the frame receive error using the ET0_RX_ER pin. The FRECR register increments each time the ET0_RX_ER pin goes high. When the register value becomes FFFF FFFFh, the counter stops. Writing any value to the FRECR register clears the counter value to 0.

29.2.21 CRC错误帧接收计数器寄存器(CEFCR)

Address(es): ETHERC0.CEFCR 4006 41E4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b31 to b0	CEFCR[31:0]	CRC错误帧接收计数器	请参阅此表后面的说明	R/W

CEFCR寄存器是一个计数器，用于指示检测到CRC错误的接收帧数。当寄存器值变为FFFFFFFFh时，计数器停止。向CEFCR寄存器写入任何值都会将计数器值清零。

29.2.22 帧接收错误计数器寄存器(FRECR)

Address(es): ETHERC0.FRECR 4006 41E8h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b31 to b0	FRECR[31:0]	帧接收错误Counter	请参阅此表后面的说明	R/W

FRECR寄存器是一个计数器，用于指示帧接收错误发生的次数。PHY-LSI使用ET0_RX_ER引脚将帧接收错误通知ETHERC。每次ET0_RX_ER引脚变高时，FRECR寄存器都会递增。当寄存器值变为FFFFFFFFh时，计数器停止。向FRECR寄存器写入任何值都会将计数器值清零。

29.2.23 Too-Short Frame Receive Counter Register (TSFRCR)

Address(es): ETHERC0.TSFRCR 4006 41ECh

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	TSFRCR[31:16]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TSFRCR[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b31 to b0	TSFRCR[31:0]	Too-Short Frame Receive Counter	See the description following this table	R/W

The TSFRCR register is a counter that indicates the number of times a short frame that is shorter than 64 bytes was received. When the register value becomes FFFF FFFFh, the counter stops. Writing any value to the TSFRCR register clears the counter value to 0.

29.2.24 Too-Long Frame Receive Counter Register (TLFRCR)

Address(es): ETHERC0.TLFRCR 4006 41F0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	TLFRCR[31:16]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TLFRCR[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b31 to b0	TLFRCR[31:0]	Too-Long Frame Receive Counter	See the description following this table	R/W

The TLFRCR register is a counter that indicates the number of times a long frame that is longer than the RFLR register value was received. When the register value becomes FFFF FFFFh, the counter stops. Writing any value to the TLFRCR register clears the counter value to 0.

Note: The TLFRCR register does not increment when a frame is received with an alignment error. In this case, the RFCR register increments.

29.2.23 过短帧接收计数器寄存器(TSFRCR)

Address(es): ETHERC0.TSFRCR 4006 41ECh

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	TSFRCR[31:16]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TSFRCR[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b31 to b0	TSFRCR[31:0]	帧接收过短 Counter	请参阅此表后面的说明	R/W

TSFRCR寄存器是一个计数器，用于指示接收到短于64字节的短帧的次数。当寄存器值变为FFFFFFFFh时，计数器停止。向TSFRCR寄存器写入任何值都会将计数器值清除为0。

29.2.24 过长帧接收计数器寄存器(TLFRCR)

Address(es): ETHERC0.TLFRCR 4006 41F0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	TLFRCR[31:16]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TLFRCR[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

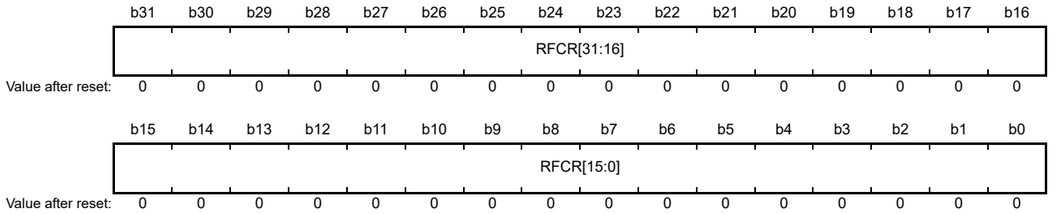
Bit	Symbol	位名称	Description	R/W
b31 to b0	TLFRCR[31:0]	帧接收过长 Counter	请参阅此表后面的说明	R/W

TLFRCR寄存器是一个计数器，用于指示接收到长于RFLR寄存器值的长帧的次数。当寄存器值变为FFFFFFFFh时，计数器停止。向TLFRCR寄存器写入任何值都会将计数器值清零。

Note: 当接收到有对齐错误的帧时，TLFRCR寄存器不会增加。在这种情况下，RFCR寄存器递增。

29.2.25 Received Alignment Error Frame Counter Register (RFCR)

Address(es): ETHERC0.RFCR 4006 41F4h

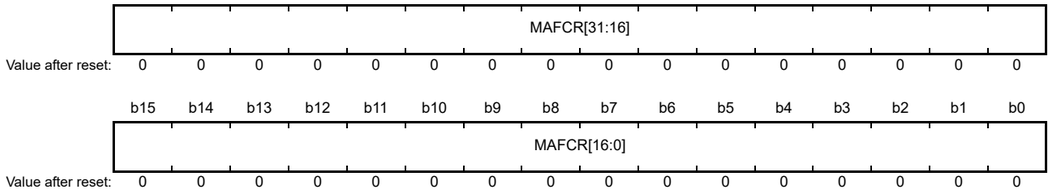


Bit	Symbol	Bit name	Description	R/W
b31 to b0	RFCR[31:0]	Received Alignment Error Frame Counter	See the description following this table	R/W

The RFCR register is a counter that indicates the number of times a frame was received with an alignment error, meaning that it is not an integral number of octets. When the register value becomes FFFF FFFFh, the counter stops. Writing any value to the RFCR register clears the counter value to 0.

29.2.26 Multicast Address Frame Receive Counter Register (MAFCR)

Address(es): ETHERC0.MAFCR 4006 41F8h

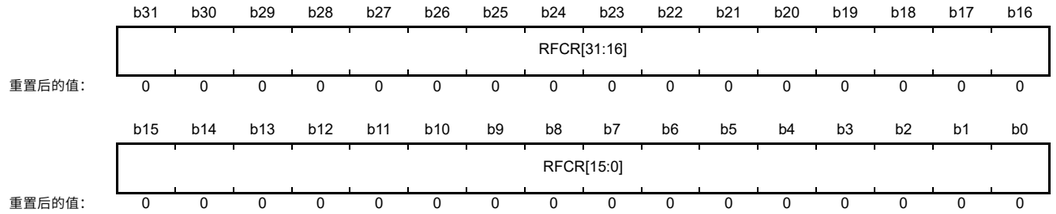


Bit	Symbol	Bit name	Description	R/W
b31 to b0	MAFCR[31:0]	Multicast Address Frame Receive Counter	See the description following this table	R/W

The MAFCR register is a counter that indicates the number of times a frame with the multicast address set was received. When the register value becomes FFFF FFFFh, the counter stops. Writing any value to the MAFCR register clears the counter value to 0.

29.2.25 接收对齐错误帧计数器寄存器(RFCR)

Address(es): ETHERC0.RFCR 4006 41F4h

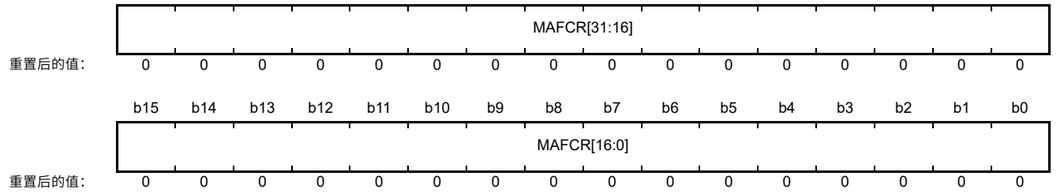


Bit	Symbol	位名称	Description	R/W
b31 to b0	RFCR[31:0]	收到对齐错误帧计数器	请参阅此表后面的说明	R/W

RFCR寄存器是一个计数器，指示接收到的帧出现对齐错误的次数，这意味着它不是八位字节的整数。当寄存器值变为FFFFFFFFh时，计数器停止。向RFCR寄存器写入任何值都会将计数器值清除为0。

29.2.26 多播地址帧接收计数器寄存器(MAFCR)

Address(es): ETHERC0.MAFCR 4006 41F8h



Bit	Symbol	位名称	Description	R/W
b31 to b0	MAFCR[31:0]	组播地址帧接收计数器	请参阅此表后面的说明	R/W

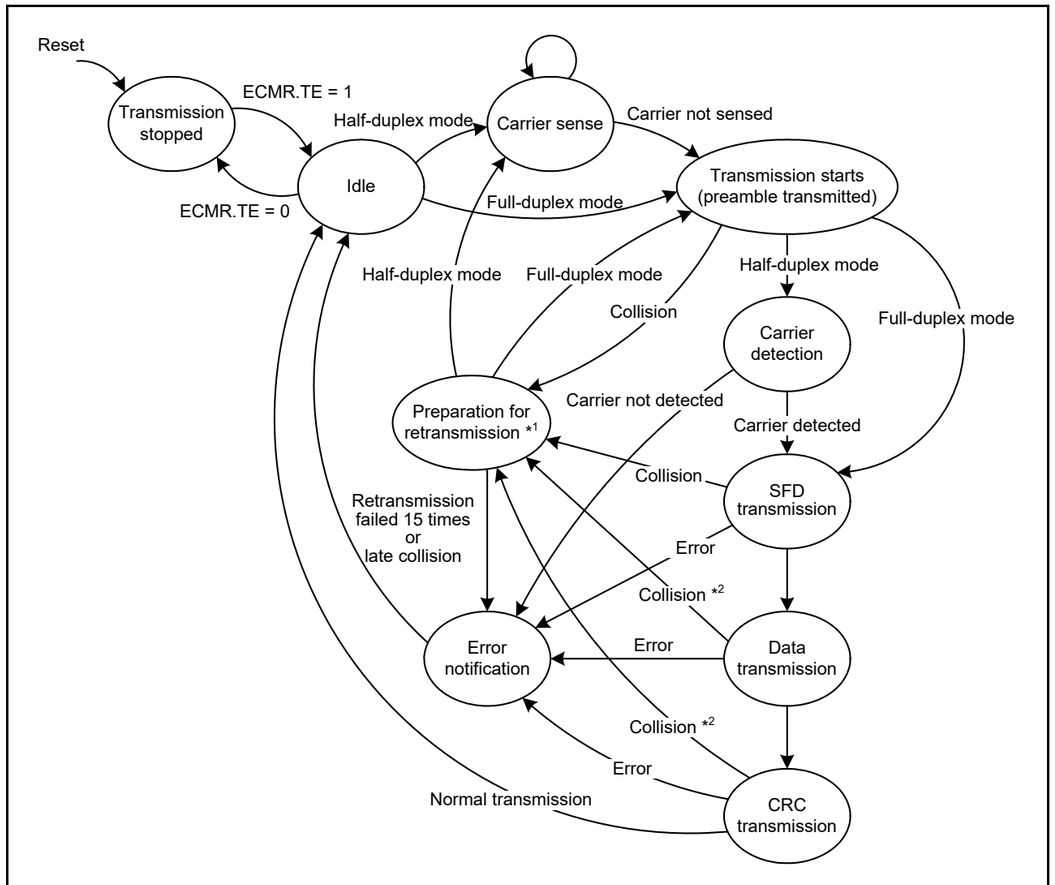
MAFCR寄存器是一个计数器，用于指示接收到设置了多播地址的帧的次数。
当寄存器值变为FFFFFFFFh时，计数器停止。向MAFCR寄存器写入任何值都会将计数器值清除为0。

29.3 Operation

This section provides an overview of the ETHERC operations. The ETHERC supports flow control compliant with IEEE802.3x, and can transmit and receive PAUSE frames. When using the ETHERC, set the clock to ICLK = PCLKA beforehand.

29.3.1 Transmission

The ETHERC transmitter assembles transmit data into a frame and outputs it to the MII or RMII when a transmit request is received from the EDMAC. The frame transmitted through the MII or RMII is transmitted on the line by the PHY-LSI. Figure 29.4 shows the state transitions of the ETHERC transmitter.



Note 1. Preparation for retransmission after a collision is detected includes transmitting a jam signal and adjusting transmission time intervals using the backoff algorithm.

Note 2. Preparation for retransmission is performed only when a collision is detected within 512 bit times after preamble transmission starts. When a collision is detected after 512 bit times, only a jam signal is transmitted and processing using the backoff algorithm is not performed.

Figure 29.4 ETHERC transmitter state transitions

The ETHERC transmitter state transitions are as follows:

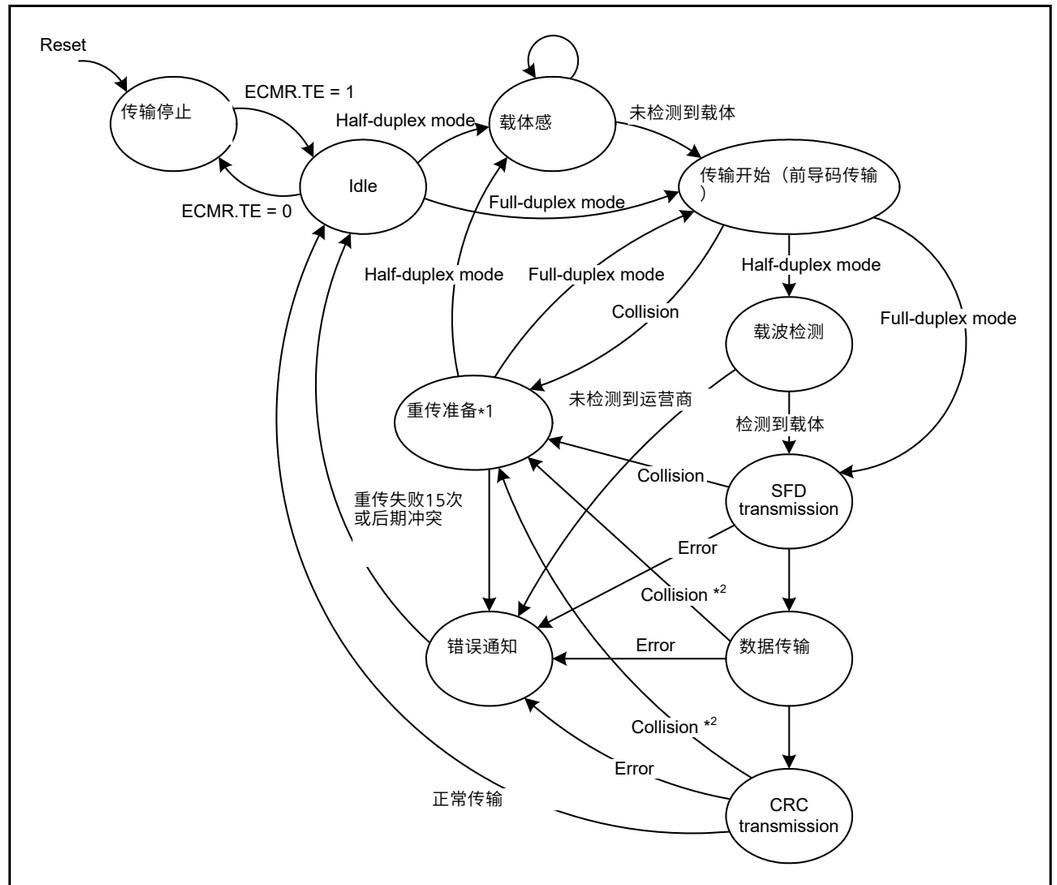
1. When the ECMR.TE bit is set to 1, the ETHERC enters the transmit idle state.
2. When a transmit request is received from the EDMAC, the ETHERC enters the carrier sense state. The ETHERC waits for the interpacket gap and then transmits a preamble to the MII or RMII. When full-duplex mode is selected,

29.3 Operation

本节概述了ETHERC操作。ETHERC支持符合以下标准的流量控制
IEEE802.3x，可收发PAUSE帧。使用ETHERC时，请预先将时钟设置为ICLK=PCLKA。

29.3.1 Transmission

当收到来自EDMAC的发送请求时，ETHERC发送器将发送数据组合成一个帧并将其输出到MII或RMII。通过MII或RMII传输的帧由PHY-LSI在线路上传输。图29.4显示了ETHERC发送器的状态转换。



Note 1. 检测到冲突后的重传准备包括传输阻塞信号和使用退避算法调整传输时间间隔。

Note 2. 只有在前导码传输开始后的512比特时间内检测到冲突时，才执行重传准备。当在512位时间后检测到冲突时，仅传输阻塞信号，并且不执行使用退避算法的处理。

Figure 29.4 ETHERC发送器状态转换

ETHERC发送器状态转换如下：

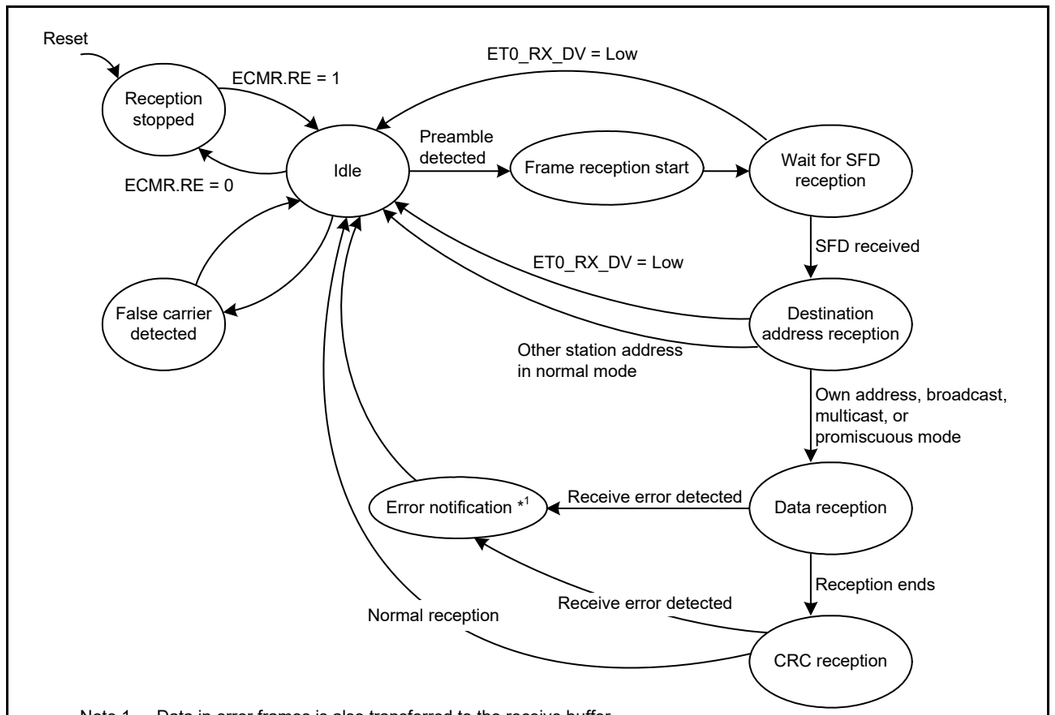
1. 当ECMR.TE位设置为1时，ETHERC进入发送空闲状态。
2. 当收到来自EDMAC的发送请求时，ETHERC进入载波侦听状态。ETHERC等待包间间隙，然后将前同步码发送到MII或RMII。Whenfull-duplexmodeisselected

carrier sensing is not required, so the ETHERC transmits a preamble immediately after receiving a transmit request from the EDMAC.

3. The ETHERC transmits the Start Frame Delimiter (SFD), transmit data, and CRC sequentially. When the transmission completes successfully, the ETHERC notifies the EDMAC of successful completion, and the EDMAC sets the EDMAC0.EESR.TC flag to 1. When a late collision or loss of carrier is detected during data transmission, the ETHERC stops the transmission and notifies the EDMAC of the error.
4. After the time specified as the interpacket gap has elapsed, the ETHERC enters the idle state and continues transmission when transmit data remains.

29.3.2 Reception

The ETHERC receiver separates the frame input from the MII or RMII into the preamble, SFD, receive data, and CRC, and transmits only the receive data (destination address, source address, type/length, data/LLC). Figure 29.5 shows the state transitions of the ETHERC receiver.



Note 1. Data in error frames is also transferred to the receive buffer.

Figure 29.5 ETHERC receiver state transitions

The ETHERC receiver state transitions are as follows:

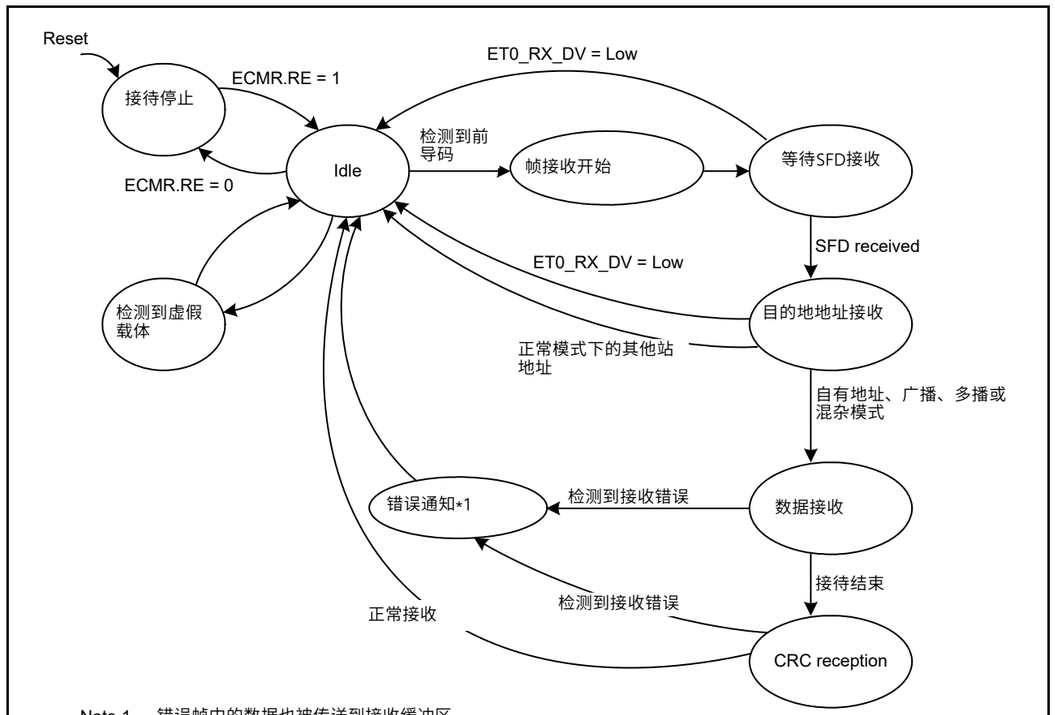
1. When the ECMR.RE bit is set to 1, the ETHERC enters the receive idle state.
2. When the SFD following the preamble of the receive packet is detected, the ETHERC starts reception. If the received SFD is invalid, the ETHERC discards the frame.
3. In normal mode, the ETHERC starts data reception when the destination address of the receive frame is the address of the MCU or the receive frame is a broadcast or multicast frame. In promiscuous mode, the ETHERC starts data reception regardless of the receive frame type.
4. After receiving data from the MII or RMII, the ETHERC performs a CRC check. The ETHERC notifies the EDMAC of the CRC check result. After the received data is transferred to the receive buffer, the CRC check result

不需要载波侦听，因此ETHERC在收到来自EDMAC的发送请求后立即发送前导码。

3. ETHERC依次传输起始帧定界符(SFD)、传输数据和CRC。当传输成功完成时，ETHERC通知EDMAC成功完成，EDMAC将EDMAC0.EESR.TC标志设置为1。当在数据传输过程中检测到延迟冲突或载波丢失时，ETHERC停止传输并通知错误的EDMAC。
4. 在指定为包间间隙的时间过去后，ETHERC进入空闲状态并在传输数据剩余时继续传输。

29.3.2 Reception

ETHERC接收器将从MII或RMII输入的帧分离为前导码、SFD、接收数据和CRC，并仅发送接收数据（目标地址、源地址、类型长度、数据LLC）。图29.5显示了ETHERC接收器的状态转换。



Note 1. 错误帧中的数据也被传送到接收缓冲区。

Figure 29.5 ETHERC接收器状态转换

ETHERC接收器状态转换如下：

1. 当ECMR.RE位设置为1时，ETHERC进入接收空闲状态。
2. 当检测到接收数据包前导码之后的SFD时，ETHERC开始接收。如果接收到的SFD无效，则ETHERC丢弃该帧。
3. 在正常模式下，当接收帧的目的地址是MCU的地址或接收帧是广播或组播帧时，ETHERC开始数据接收。在混杂模式下，无论接收帧类型如何，ETHERC都会开始数据接收。
4. 从MII或RMII接收数据后，ETHERC执行CRC校验。ETHERC通知CRC校验结果的EDMAC。接收到的数据传送到接收缓冲区后，CRC校验结果

is written back to the receive descriptor as status. The result is also reflected in the EDMAC0.EESR.CERF flag.

5. When the ECMR.RE bit is 1 after one frame is received, the ETHERC prepares to receive the next frame.

29.3.3 Frame Timing

29.3.3.1 MII frame timing

Figure 29.6 to Figure 29.11 show the MII frame timing.

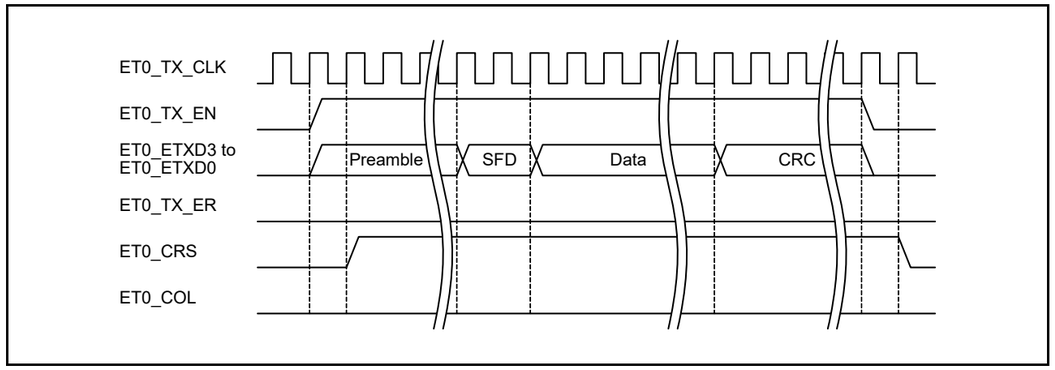


Figure 29.6 MII frame transmit timing during normal transmission

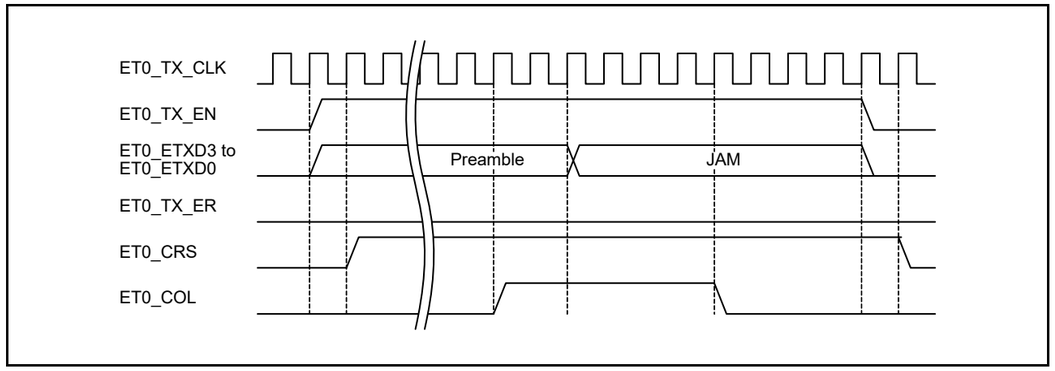


Figure 29.7 MII frame transmit timing when a collision occurs

被写回接收描述符作为状态。结果也反映在EDMAC0.EESR.CERF标志中。

5. 当接收到一帧后ECMR.RE位为1时，ETHERC准备接收下一帧。

29.3.3 帧时序

29.3.3.1 MII帧时序

图29.6至图29.11显示了MII帧时序。

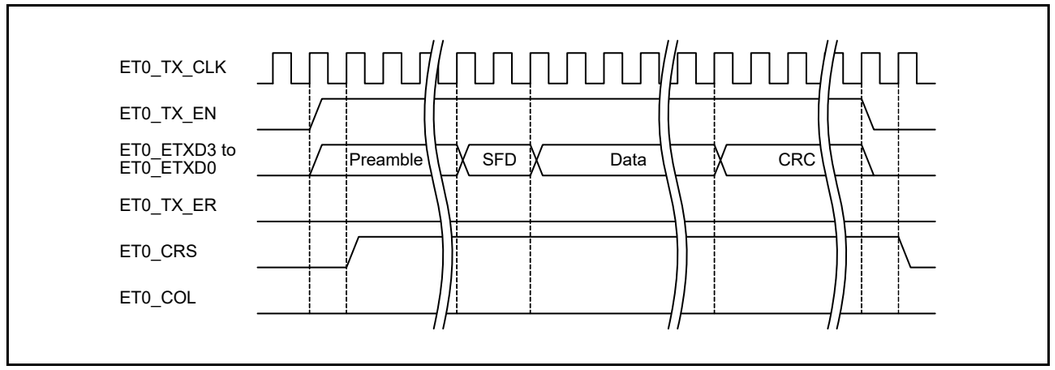


Figure 29.6 正常传输期间的MII帧传输时序

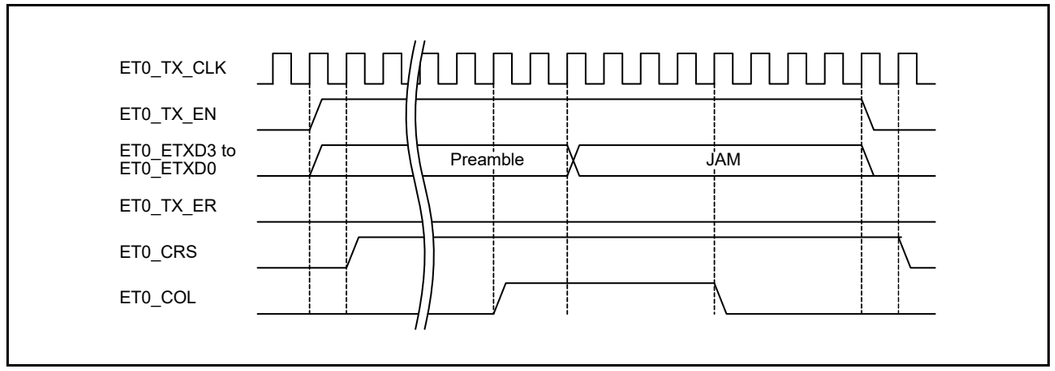


Figure 29.7 发生冲突时的MII帧发送时序

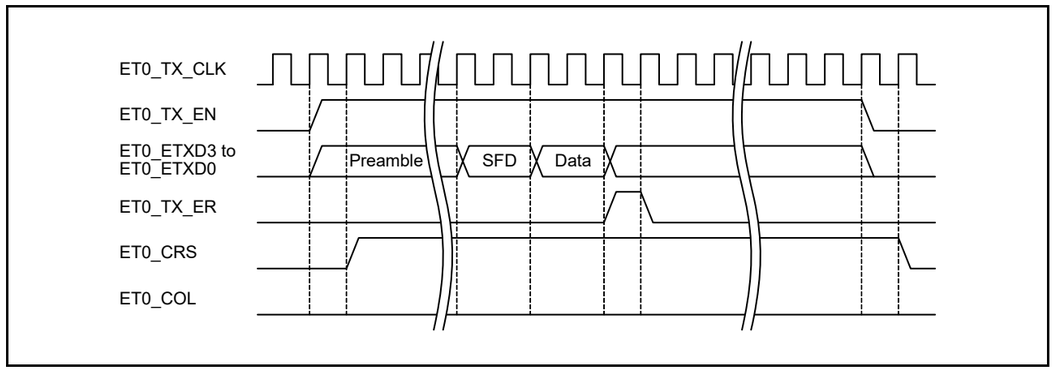


Figure 29.8 MII frame transmit timing when a transmit error occurs

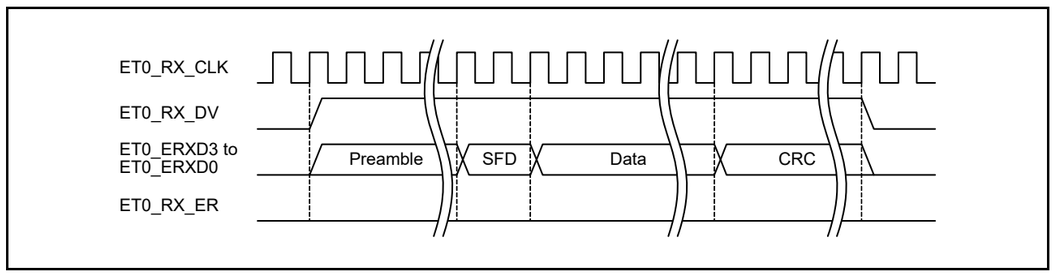


Figure 29.9 MII frame receive timing during normal reception

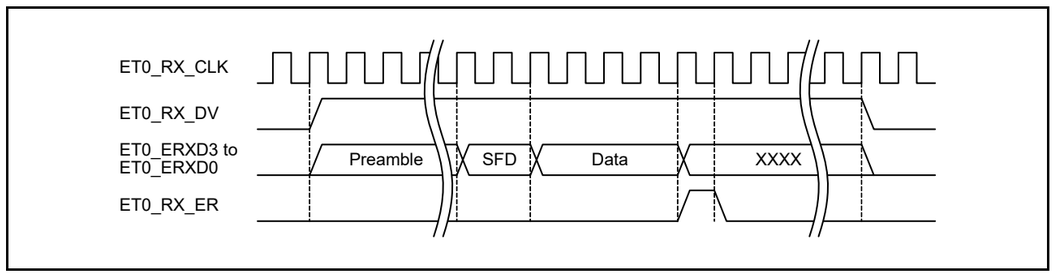


Figure 29.10 MII frame receive timing for receive error notification

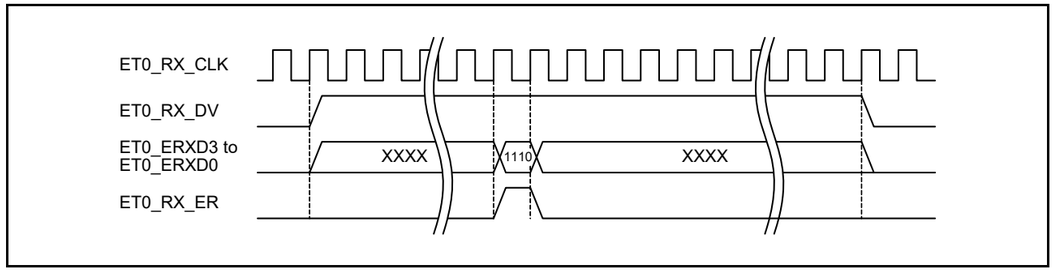


Figure 29.11 MII frame receive timing for false carrier notification

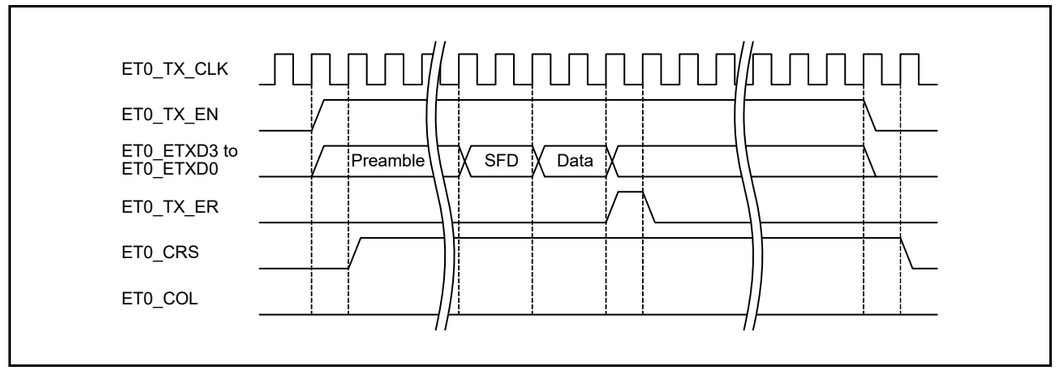


Figure 29.8 发生传输错误时的MII帧传输时序

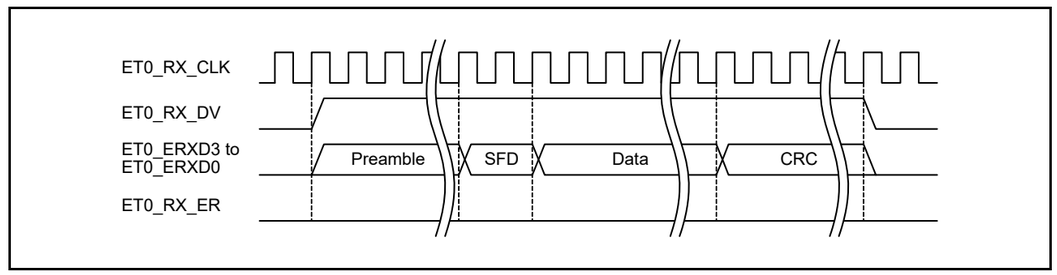


Figure 29.9 正常接收期间的MII帧接收时序

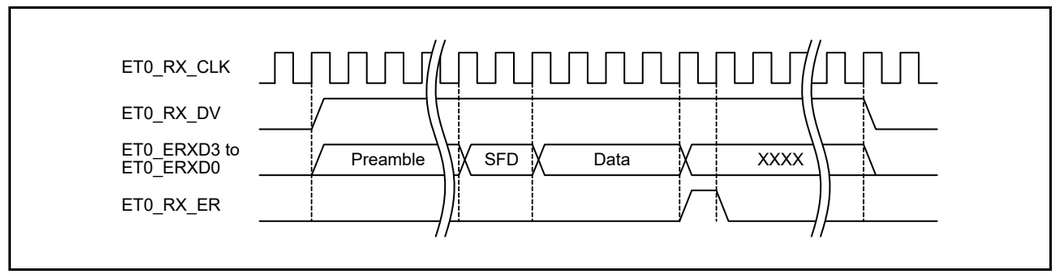


Figure 29.10 接收错误通知的MII帧接收时序

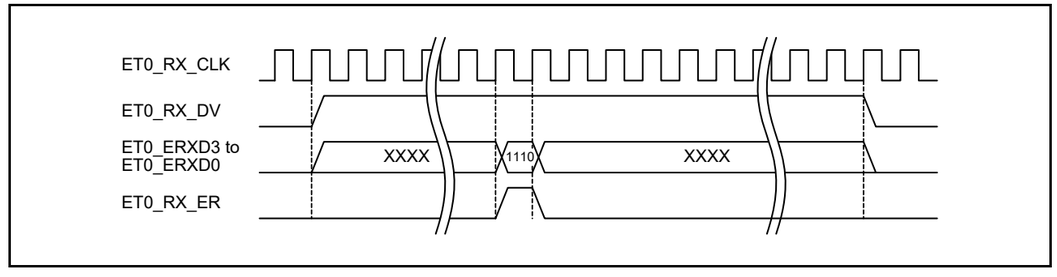


Figure 29.11 错误载波通知的MII帧接收时序

29.3.3.2 RMII frame timing

Figure 29.12 to Figure 29.14 show the RMII frame timing.

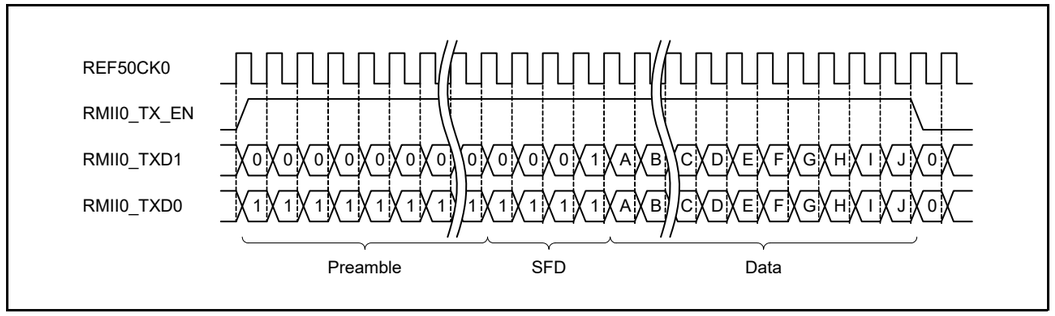


Figure 29.12 RMII frame transmit timing during normal transmission

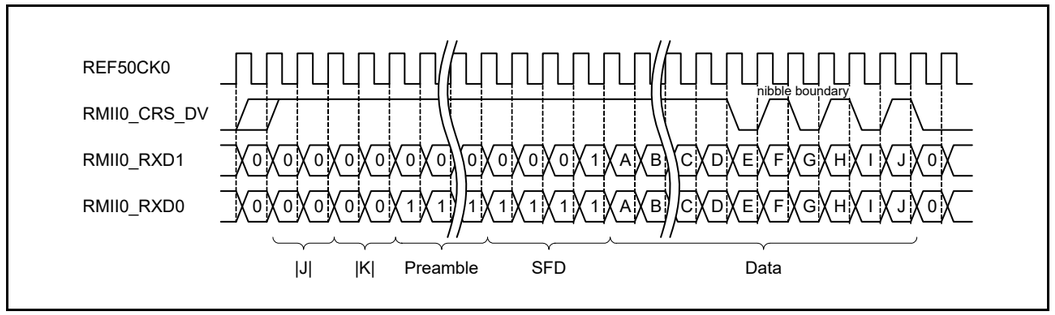


Figure 29.13 RMII frame receive timing during normal reception

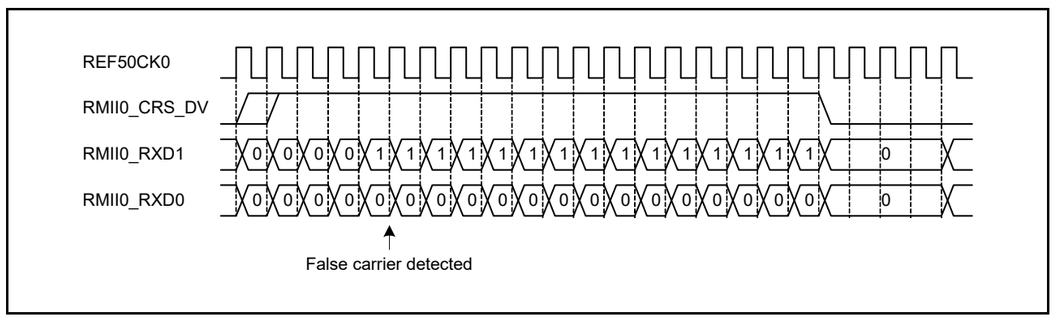


Figure 29.14 RMII frame receive timing when a false carrier is detected

29.3.3.2 RMII帧时序

图29.12至图29.14显示了RMII帧时序。

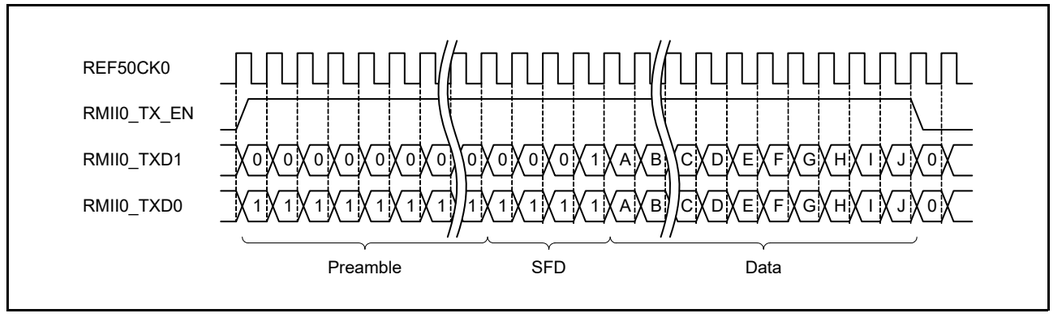


Figure 29.12 正常传输期间的RMII帧传输时序

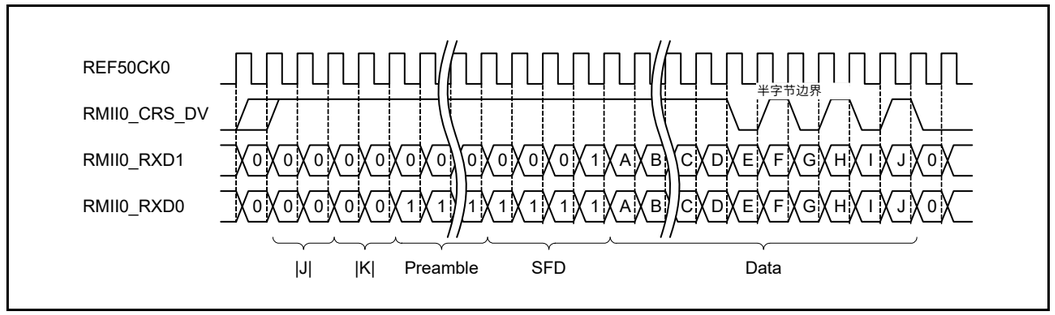


Figure 29.13 正常接收期间的RMII帧接收时序

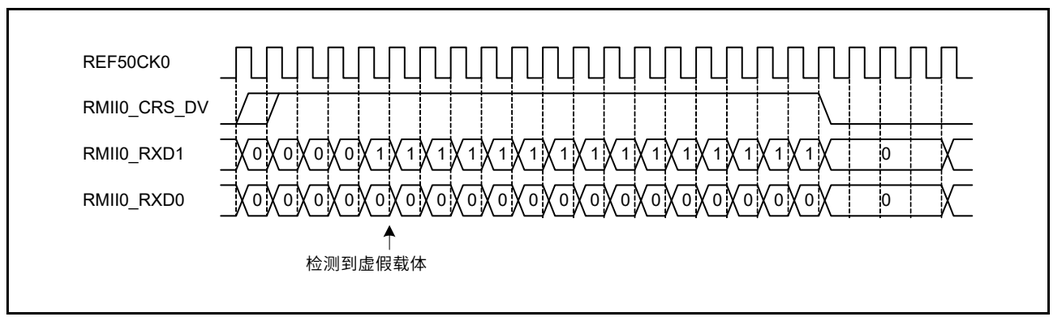


Figure 29.14 检测到错误载波时的RMII帧接收时序

29.3.4 Accessing the MII and RMII Registers

Use the PIR register to access the MII and RMII registers in the PHY-LSI. Serial data in the MII and RMII management frame format is transmitted and received through the ET0_MDC and ET0_MDIO pins controlled by software.

29.3.4.1 MII and RMII management frame format

Table 29.3 lists the MII and RMII management frame formats.

Table 29.3 MII and RMII management frame formats

Access type		MII and RMII management frame							
	Parameter	PRE	ST	OP	PHYAD	REGAD	TA	DATA	IDLE
	Number of bits	32	2	2	5	5	2	16	1
Read		1...1	01	10	00001	RRRRR	Z0	DDDDDDDDDDDDDDDD	Z
Write		1...1	01	01	00001	RRRRR	10	DDDDDDDDDDDDDDDD	Z

Note: PRE (preamble): Send 32 consecutive 1s.
ST (start of frame): Send 01b.
OP (operation code): Send 10b for read or 01b for write.
PHYAD (PHY address): Up to 32 PHY-LSIs can be connected to one MAC. PHY-LSIs are selected with these 5 bits. When the PHY-LSI address is 1, send 00001b.
REGAD (register address): One register is selected from up to 32 registers in the PHY-LSI. When the register address is 1, send 00001b.
TA (turnaround): Use 2-bit turnaround time to avoid contention between the register address and data during a read operation. Send 10b during a write operation. Release the bus for 1 bit during a read operation (Z is output).
(This is indicated as Z0 because 0 is output from the PHY-LSI on the next clock cycle.)
DATA (data): 16-bit data. Sequentially send or receive starting from the MSB.
IDLE (IDLE condition): Wait time before inputting the next MII or RMII management format. Release the bus during a write operation (Z is output). No control is required, because a bus was already released during a read operation.

29.3.4.2 MII and RMII register access procedure

Access to the MII and RMII registers includes writing data in 1-bit units, reading data in 1-bit units, and releasing the bus. Figure 29.15 to Figure 29.18 show examples of the MII and RMII register access timing. The access timing differs with the PHY-LSI type.

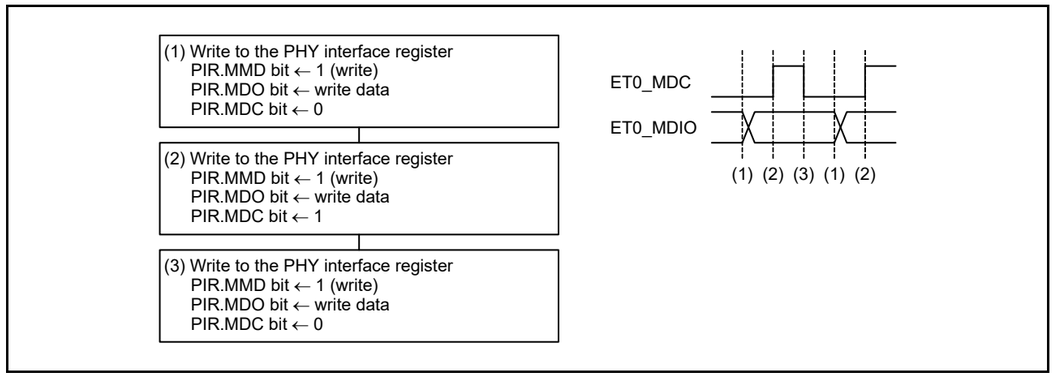


Figure 29.15 1-bit data write flow

29.3.4 访问MII和RMII寄存器

使用PIR寄存器访问PHY-LSI中的MII和RMII寄存器。MII和RMII管理帧格式的串行数据通过软件控制的ET0_MDC和ET0_MDIO引脚发送和接收。

29.3.4.1 MII和RMII管理帧格式

表29.3列出了MII和RMII管理帧格式。

Table 29.3 MII和RMII管理帧格式

访问类型		MII和RMII管理框架							
	Parameter	PRE	ST	OP	PHYAD	REGAD	TA	DATA	IDLE
	位数	32	2	2	5	5	2	16	1
Read		1...1	01	10	00001	RRRRR	Z0	DDDDDDDDDDDDDDDD	Z
Write		1...1	01	01	00001	RRRRR	10	DDDDDDDDDDDDDDDD	Z

Note: PRE（前导码）：发送32个连续的1。
ST（帧开始）：发送01b。
OP（操作码）：发送10b读或01b写。
PHYAD（PHY地址）：一个MAC最多可以连接32个PHY-LSI。使用这5位选择PHY-LSI。当。。。的时候
PHY-LSI地址为1，发送00001b。
REGAD（寄存器地址）：从PHY-LSI的最多32个寄存器中选择一个寄存器。当寄存器地址为1时，发送00001b。TA（周转）：使用2位周转时间来避免读取操作期间寄存器地址和数据之间的争用。

在写操作期间发送10b。在读操作期间释放总线1位（Z为输出）。（这表示为Z0，因为在下一个时钟周期从PHY-LSI输出0。）DATA（数据）：16位数据。从MSB开始顺序发送或接收。

IDLE（IDLE条件）：输入下一个MII或RMII管理格式前的等待时间。在写操作期间释放总线（Z为输出）。不需要控制，因为在读取操作期间总线已被释放。

29.3.4.2 MII和RMII寄存器访问过程

对MII和RMII寄存器的访问包括以1位为单位写入数据、以1位为单位读取数据以及释放总线。图29.15至图29.18显示了MII和RMII寄存器访问时序的示例。访问时序因PHY-LSI类型而异。

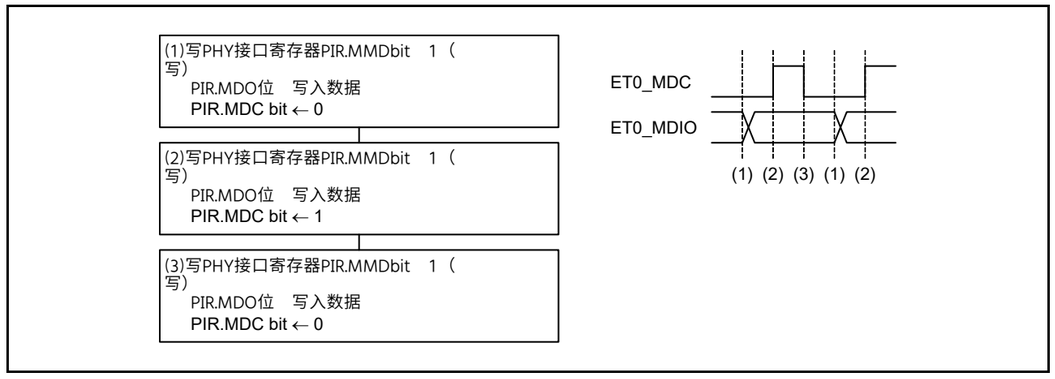


Figure 29.15 1位数据写入流程

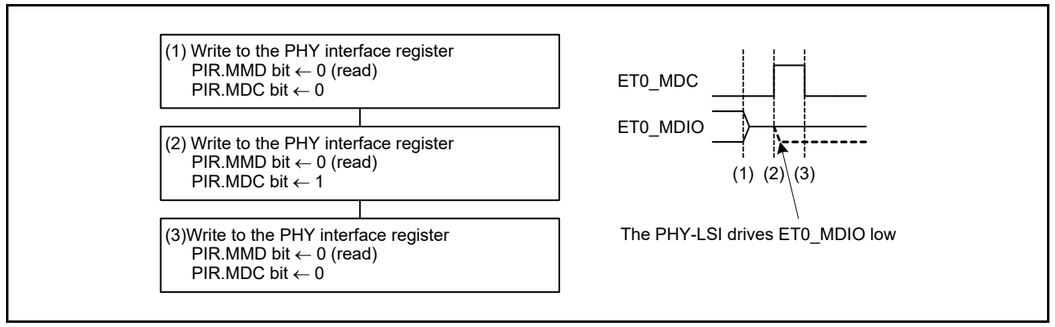


Figure 29.16 Bus release flow, with TA in read operation in Table 29.3

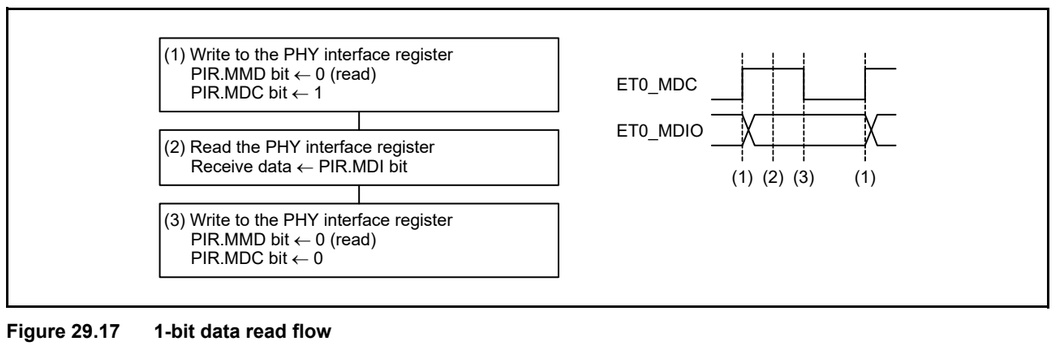


Figure 29.17 1-bit data read flow

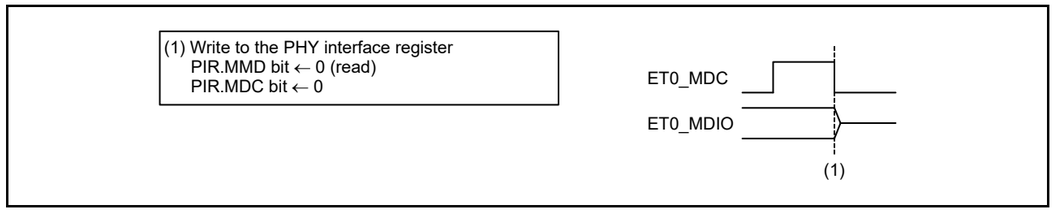


Figure 29.18 Bus release flow, with IDLE in write operation in Table 29.3

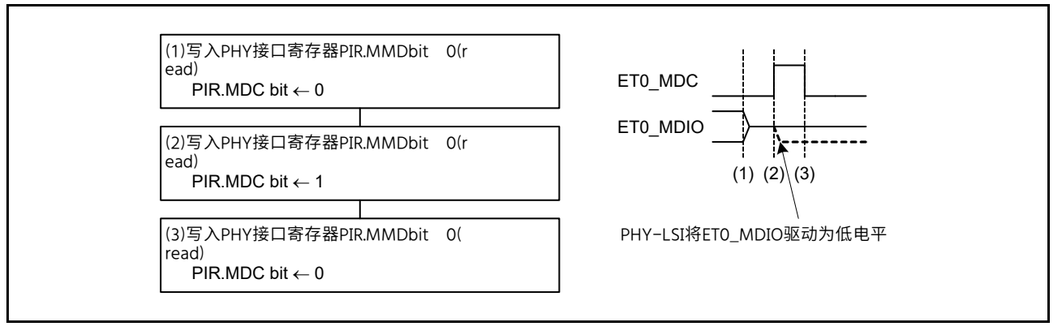


Figure 29.16 总线释放流程，TA在读操作中见表29.3

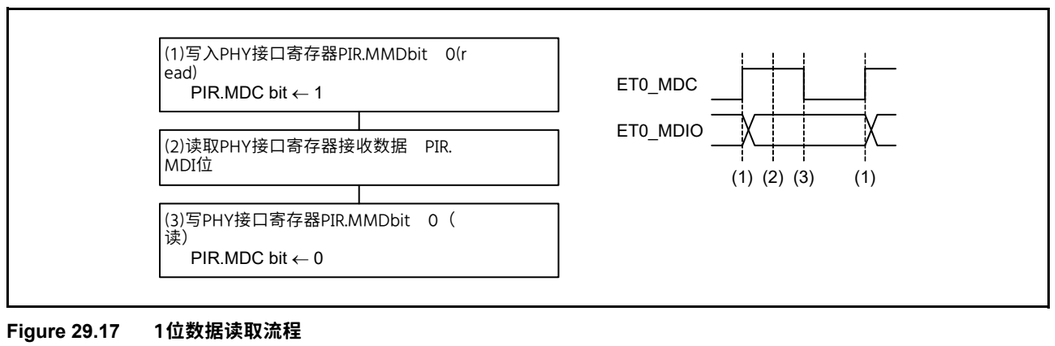


Figure 29.17 1位数据读取流程

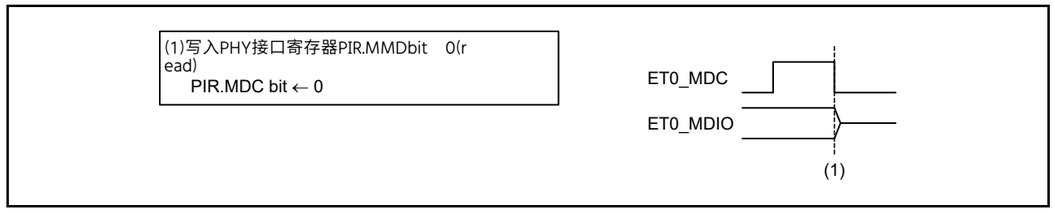


Figure 29.18 总线释放流程，IDLE写操作见表29.3

29.3.5 Magic Packet Detection

The ETHERC supports Wake-on-LAN (WOL). WOL is a function to detect a Magic Packet transmitted from a host device or other device and wake the MCU from a low power mode such as Sleep. When the ETHERC detects a Magic Packet, it outputs high on the ET0_WOL pin. Write 1 to the EDMAC0.EDMR.SWR bit to drive the ET0_WOL pin low.

Because a Magic Packet is transmitted in broadcast mode, it is received regardless of the destination MAC address selected in the format. The ETHERC outputs high on the ET0_WOL pin only when the destination MAC address matches its own MAC address. See the technical documentation provided by Advanced Micro Devices, Inc., for details on the Magic Packet.

To use WOL in the MCU, use the procedure in the following example:

1. Configure the ICU to disable ETHER_EINT0 interrupt requests.
2. Set the ECMR.MPDE bit to 1 to enable Magic Packet detection, and set the ECMR.RE bit to 1 to enable reception.
3. Set the ECSIPR.MPDIP bit to 1 to enable notification of Magic Packet detection interrupts.
4. Set the EDMAC0.EESIPR.ECIIP bit to 1 to enable ETHERC status register source interrupts.
5. Configure the ICU to enable ETHER_EINT0 interrupt requests.
6. Change the CPU operating mode to Sleep mode or place unused peripherals in the module-stop state, as required.
7. When a Magic Packet is detected, an interrupt request is sent to the CPU. High is output on the ET0_WOL pin to notify peripheral devices that the Magic Packet was detected.

29.3.5.1 Constraints on Magic Packet detection

The ETHERC receives packets, including broadcast packets, even when waiting to receive a Magic Packet. This means that receive data might already be stored in the receive FIFO of the EDMAC when a Magic Packet is detected. Also, flags in the ECSR and EDMAC0.EESR registers might have changed. When returning to normal operation after detecting a Magic Packet, set the EDMAC0.EDMR.SWR bit to 1 to reset the ETHERC and EDMAC.

29.3.6 Adjusting Transmission Efficiency by Changing the IPG

The IPG is a non-transmit period between transmit frames. The ETHERC can change the value of the IPG to increase or decrease transmission efficiency based on the value set in the IPGR register. Typical values are specified in the IEEE802.3 standard. When changing the setting, confirm that all devices in the same network operate normally.

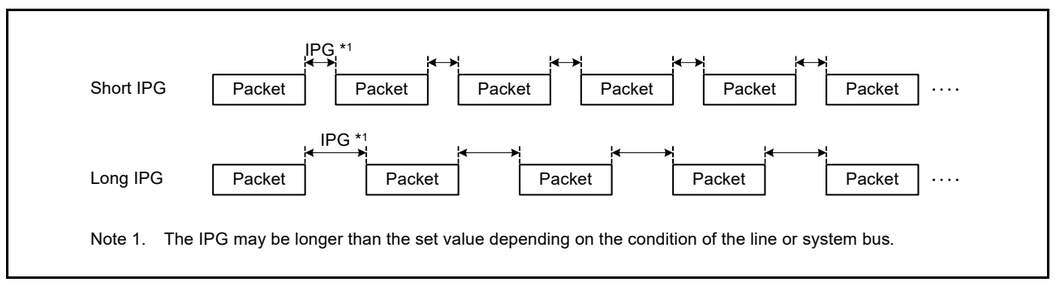


Figure 29.19 Differences in transmission efficiency based on changes in the IPG

29.3.5 魔术包检测

ETHERC支持网络唤醒(WOL)。WOL是一种检测从主机设备或其他设备发送的魔术包并将MCU从低功耗模式（例如睡眠）唤醒的功能。当ETHERC检测到一个魔术包时，它在ET0_WOL引脚上输出高电平。将1写入EDMAC0.EDMR.SWR位以将ET0_WOL引脚驱动为低电平。

因为MagicPacket以广播模式传输，所以无论格式中选择的目标MAC地址如何，都会接收到它。仅当目标MAC地址与其自己的MAC地址匹配时，ETHERC才会在ET0_WOL引脚上输出高电平。有关MagicPacket的详细信息，请参阅AdvancedMicroDevices Inc.提供的技术文档。

要在MCU中使用WOL，请使用以下示例中的过程：

1. 将ICU配置为禁用ETHER_EINT0中断请求。
2. 将ECMR.MPDE位设置为1以启用魔术包检测，并将ECMR.RE位设置为1以启用接收。
3. 将ECSIPR.MPDIP位设置为1以启用魔术包检测中断通知。
4. 将EDMAC0.EESIPR.ECIIP位设置为1以启用ETHERC状态寄存器源中断。
5. 配置ICU以启用ETHER_EINT0中断请求。
6. 根据需要，将CPU操作模式更改为睡眠模式或将未使用的外设置于模块停止状态。
7. 当检测到MagicPacket时，会向CPU发送中断请求。ET0_WOL引脚上输出高电平以通知外围设备检测到魔术包。

29.3.5.1 魔术包检测的约束

ETHERC接收数据包，包括广播数据包，即使在等待接收魔术数据包时也是如此。这意味着当检测到魔术包时，接收数据可能已经存储在EDMAC的接收FIFO中。此外，ECSR和EDMAC0.EESR寄存器中的标志可能已更改。检测到魔术包后返回正常操作时，将EDMAC0.EDMR.SWR位设置为1以复位ETHERC和EDMAC。

29.3.6 改变IPG调整传输效率

IPG是传输帧之间的非传输周期。ETHERC可以根据IPGR寄存器中设置的值改变IPG的值来提高或降低传输效率。典型值在IEEE802.3标准中指定。更改设置时，请确认同一网络中的所有设备都正常运行。

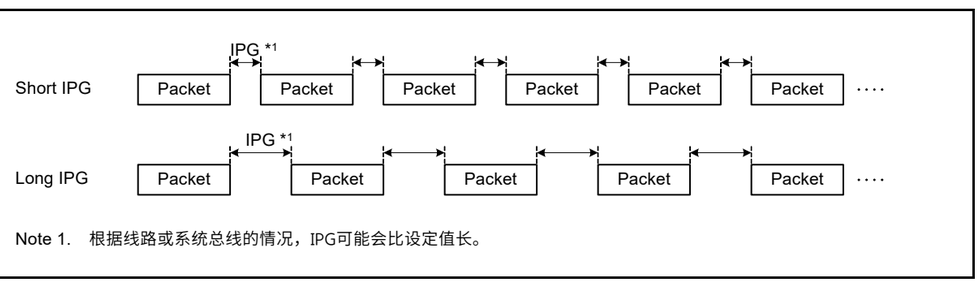


Figure 29.19 基于IPG变化的传输效率差异

29.3.7 Flow Control

The ETHERC can perform flow control compliant with IEEE802.3x in full-duplex mode, and the receiver and transmitter can be set independently. PAUSE frames can be transmitted automatically or manually.

29.3.7.1 Automatic PAUSE frame transmission

When the ECMR.TXF bit is set to 1, automatic PAUSE frame transmission is enabled. A PAUSE frame is automatically transmitted by a PAUSE frame transmit request from the EDMAC. The APR.AP[15:0] bit value is used for the pause_time parameter of the PAUSE frame.

When a PAUSE frame is transmitted, if the EDMAC is still requesting PAUSE frame transmission after the PAUSE time elapses, a PAUSE frame is transmitted again. The maximum number of PAUSE frame retransmissions can be set in the TPAUSER.TPAUSE[15:0] bits. If the maximum number of retransmissions is reached, subsequent PAUSE frames are not transmitted.

Figure 29.20 shows the procedure for setting up automatic PAUSE frame transmission.

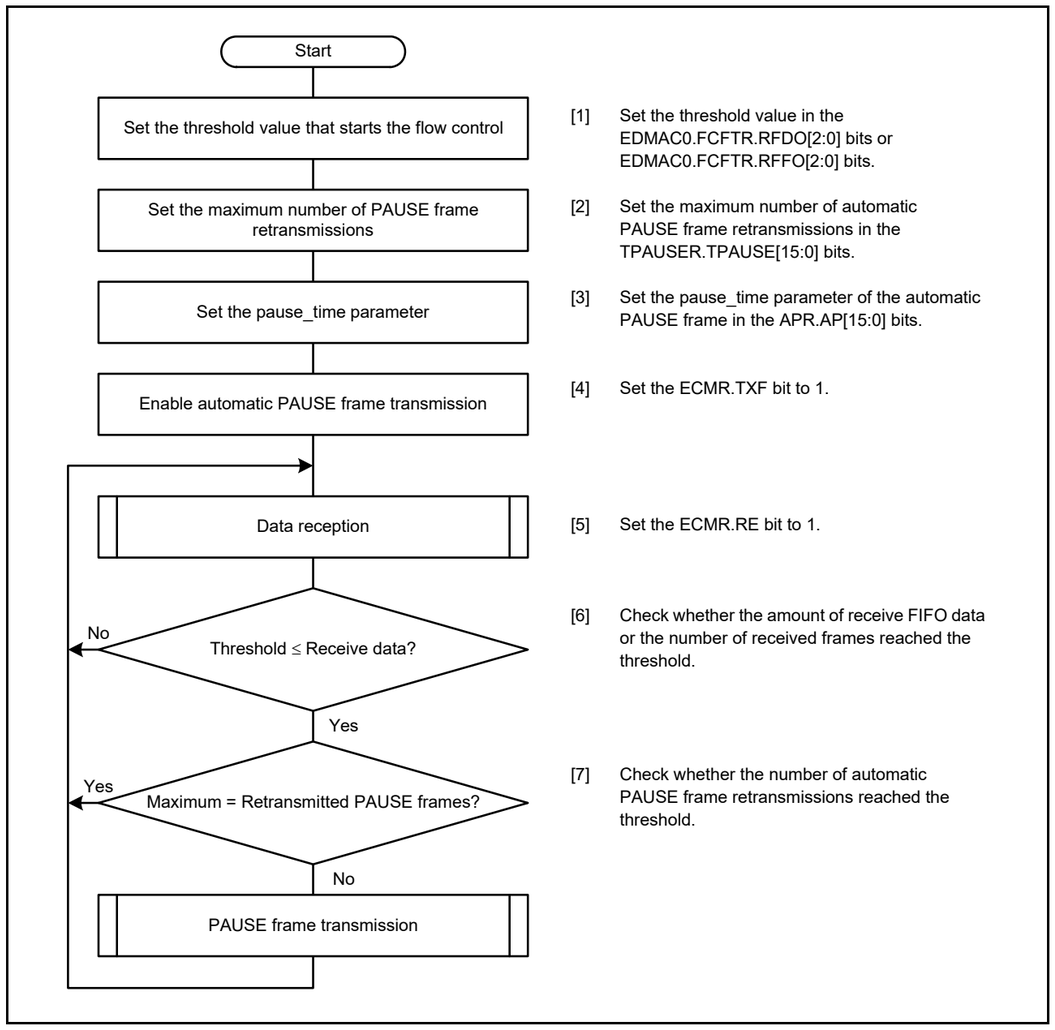


Figure 29.20 Example procedure for setting up automatic PAUSE frame transmission

29.3.7 流量控制

ETHERC可以在全双工模式下进行符合IEEE802.3x的流量控制，接收端和发送端可以独立设置。PAUSE帧可以自动或手动传输。

29.3.7.1 自动暂停帧传输

当ECMR.TXF位设置为1时，启用自动暂停帧传输。PAUSE帧由来自EDMAC的PAUSE帧发送请求自动发送。APR.AP[15:0]位值用于PAUSE帧的pause_time参数。

当发送暂停帧时，如果在暂停时间过去后EDMAC仍在请求暂停帧发送，则再次发送暂停帧。PAUSE帧重传的最大次数可以在TPAUSER.TPAUSE[15:0]位中设置。如果达到最大重传次数，则不传输后续PAUSE帧。

图29.20显示了设置自动暂停帧传输的过程。

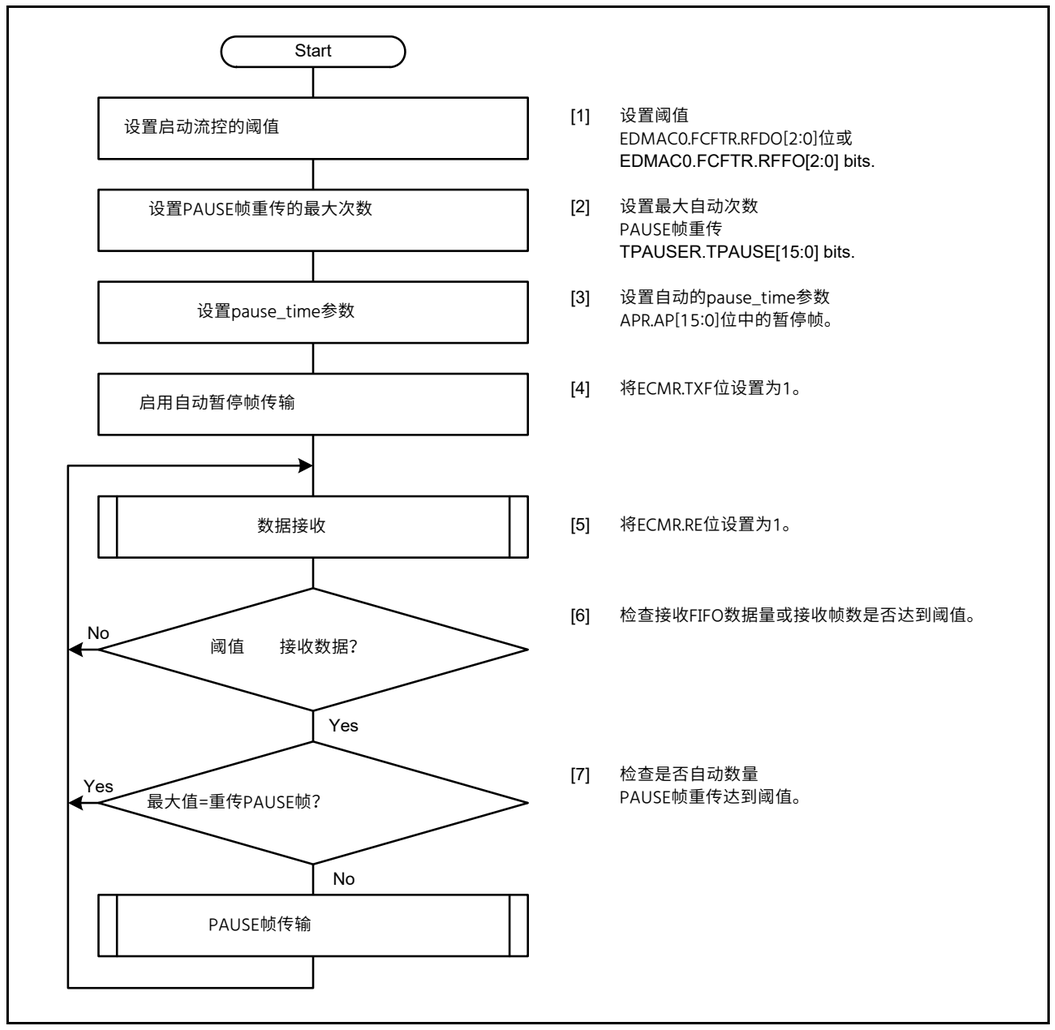


Figure 29.20 设置自动暂停帧传输的示例过程

29.3.7.2 Manual PAUSE frame transmission

A PAUSE frame can be manually transmitted at any time. When the software writes the pause_time parameter of the PAUSE frame to the MPR.MP[15:0] bits, the ETHERC transmits a PAUSE frame once. To transmit a PAUSE frame more than once, write to the MPR.MP[15:0] bits for each transmission.

29.3.7.3 PAUSE frame reception

When the ECMR.RXF bit is set to 1, PAUSE frame detection is enabled. After a PAUSE frame is received, the ETHERC completes transmission of the current frame and waits for the PAUSE time of the received PAUSE frame to elapse before it can transmit the next frame. The ETHERC also increments the RFCF.RPAUSE[7:0] bit value.

However, while waiting for the PAUSE time to elapse, if a PAUSE frame that contains a pause_time parameter of 0 is received and the ECMR.ZPF bit is 1, the ETHERC becomes ready to transmit immediately.

29.4 Interrupts

When a flag in the ECSR register sets to 1 and the associated bit in the ECSIPR register is 1, the ETHERC notifies the EDMAC of the interrupt source status. After receiving the notification, the EDMAC sets the EDMAC0.EESR.ECI flag to 1. When the EDMAC0.EESIPR.ECIIP bit is 1, the EDMAC sends an ETHER_EINT0 interrupt request to the CPU. For details, see section 31, Ethernet DMA Controller (EDMAC).

29.5 Usage Notes

29.5.1 Preventing the LCHNG Flag from Erroneously Setting to 1

The ECSR.LCHNG flag might set to 1 even when the input level of the ET0_LINKSTA pin remains the same. In this case, high is input to the ET0_LINKSTA pin when setting the PFS.PmnPFS register to assign the ET0_LINKSTA signal to a port or when releasing the ETHERC and EDMAC software reset using the EDMAC0.EDMR.SWR bit. The ECSR.LCHNG flag sets to 1 because the ET0_LINKSTA signal in the ETHERC is fixed low regardless of the input level to the external pin if the MPC does not assign the ET0_LINKSTA signal or during an ETHERC and EDMAC software reset.

To avoid erroneously generating a link signal change interrupt, clear the ECSR.LCHNG flag, and then set the ECSIPR.LCHNGIP bit to 1.

29.5.2 Input to RMII0_RX_ER Pin while RMII Is Selected

When the width of a reception error signal received from the PHY-LSI is only 1 cycle of the REF50CK0 clock (50 MHz) while the RMII is selected, the signal is not recognized as an error signal.

29.5.3 Processing when Erroneous Frame Is Detected

If an erroneous frame is detected due to a corrupted frame or noise in the external circuit when the ETHERC and EPTPC are receiving data, subsequent normal frames might not be received properly.

Reset the EDMAC, ETHERC, and EPTPC after an erroneous frame is detected. Then, wait for the required number of cycles before setting communications again.

When set to bypass EPTPC, you do not need to reset the processing. See section 30.2.79, Bypass 1588 Module Register (BYPASS).

(1) Detecting an erroneous frame

An erroneous frame can be detected by reading the INFABT flag in the SYNFP Status Register (SYSR) of EPTPCn. Even when the EPTPCn is not used but only the EDMACn and ETHERCn are used to receive and transmit standard Ethernet frames, read the INFABT flag to detect an erroneous frame (n = 0).

(2) Resetting after detection of an erroneous frame

When the EPTPCn.SYSR.INFABT flag becomes 1, reset EPTPCn, EDMACn, and ETHERCn according to the channel. Then wait for the required number of cycles before setting the registers. Even when the EPTPCn is not used but only the EDMACn and ETHERCn are used to receive and transmit standard Ethernet frames, reset the EPTPCn and the registers. In this case, you do not need to reset PTPEDMAC. The following steps show the resetting procedure where n = 0:

29.3.7.2 手动暂停帧传输

PAUSE帧可以随时手动发送。当软件将PAUSE帧的pause_time参数写入MPR.MP[15:0]位时，ETHERC发送一次PAUSE帧。要多次传输PAUSE帧，请在每次传输时写入MPR.MP[15:0]位。

29.3.7.3 暂停帧接收

当ECMR.RXF位设置为1时，启用PAUSE帧检测。接收到PAUSE帧后，ETHERC完成当前帧的传输，并等待接收到的PAUSE帧的PAUSE时间过去，然后才能传输下一帧。ETHERC还会增加RFCF.RPAUSE[7:0]位的值。

然而，在等待PAUSE时间过去时，如果接收到包含pause_time参数为0的PAUSE帧并且ECMR.ZPF位为1，则ETHERC立即准备好发送。

29.4 Interrupts

当ECSR寄存器中的标志设置为1并且ECSIPR寄存器中的相关位为1时，ETHERC通知EDMAC中断源状态。EDMAC收到通知后，将EDMAC0.EESR.ECI标志设置为1。当EDMAC0.EESIPR.ECIIP位为1时，EDMAC向CPU发送ETHER_EINT0中断请求。有关详细信息，请参阅第31节，以太网DMA控制器(EDMAC)。

29.5 使用说明

29.5.1 防止LCHNG标志错误设置为1

即使ET0_LINKSTA引脚的输入电平保持不变，ECSR.LCHNG标志也可能设置为1。在这种情况下，当设置PFS.PmnPFS寄存器以将ET0_LINKSTA信号分配给端口或使用EDMAC0.EDMR.SWR位释放ETHERC和EDMAC软件复位时，ET0_LINKSTA引脚输入高电平。ECSR.LCHNG标志设置为1，因为如果MPC未分配ET0_LINKSTA信号或在ETHERC和EDMAC软件复位期间，无论外部引脚的输入电平如何，ETHERC中的ET0_LINKSTA信号都固定为低。

为避免错误地生成链接信号更改中断，请清除ECSR.LCHNG标志，然后设置ECSIPR.LCHNGIP位为1。

29.5.2 选择RMII时输入到RMII0_RX_ER引脚

选择RMII时，如果从PHY-LSI接收到的接收错误信号的宽度仅为REF50CK0时钟(50MHz)的1个周期，则该信号不会被识别为错误信号。

29.5.3 检测到错误帧时的处理

如果在ETHERC和EPTPC接收数据时，由于帧损坏或外部电路中的噪声而检测到错误帧，则可能无法正确接收后续正常帧。

在检测到错误帧后重置EDMAC、ETHERC和EPTPC。然后，在再次设置通信之前等待所需的周期数。

当设置为绕过EPTPC时，您不需要重置处理。请参阅第30.2.79节，绕过1588模块寄存器(BYPASS)。

(1) 检测错误帧

可以通过读取EPTPCn的SYNFP状态寄存器(SYSR)中的INFABT标志来检测错误帧。即使不使用EPTPCn而仅使用EDMACn和ETHERCn来接收和发送标准
以太网帧，读取INFABT标志以检测错误帧(n=0)。

(2) 检测到错误帧后重置

当EPTPCn.SYSR.INFABT标志变为1时，根据通道复位EPTPCn、EDMACn和ETHERCn。然后在设置寄存器之前等待所需的周期数。即使不使用EPTPCn，而仅使用EDMACn和ETHERCn来接收和发送标准以太网帧，也要复位EPTPCn和寄存器。

在这种情况下，您不需要重置PTPEDMAC。以下步骤显示了n=0时的重置过程：

1. Set the EPTPC_CFG.PTRSTR.RESET bit to 1 (reset the EPTPCn through software).
2. Set the EDMACn.EDMR.SWR bit to 1 (reset the EDMACn and ETHERCn through software).
3. Wait for at least 64 cycles of the peripheral module clock (PCLKA). This step is necessary to initialize EDMACn and ETHERCn. Use a software loop or timer to wait for at least 64 PCLKA cycles.
4. Set the EPTPC_CFG.PTRSTR.RESET bit to 0 (release the EPTPCn reset).
5. Reset communications.
6. Set the EDMACn, ETHERCn, PTPEDMAC, and EPTPCn registers to enable communications.

29.5.4 Collision Occurrence in Half-Duplex Mode

Transmission might start and communication might collide within 21 clock cycles (50 MHz) from reception in half-duplex mode.

1. 将EPTPC_CFG.PTRSTR.RESET位设置为1（通过软件复位EPTPCn）。
2. 将EDMACn.EDMR.SWR位设置为1（通过软件复位EDMACn和ETHERCn）。
3. 等待至少64个外围模块时钟(PCLKA)周期。这一步是初始化EDMACn和ETHERCn所必需的。使用软件循环或定时器等待至少64个PCLKA周期。
4. 将EPTPC_CFG.PTRSTR.RESET位设置为0（释放EPTPCn复位）。
5. 重置通讯。
6. 设置EDMACn、ETHERCn、PTPEDMAC和EPTPCn寄存器以启用通信。

29.5.4 半双工模式下的冲突发生

在半双工模式下，从接收开始的21个时钟周期(50MHz)内，传输可能会开始并且通信可能会发生冲突。

30. Ethernet PTP Controller (EPTPC)

30.1 Overview

The MCU provides an on-chip Precision Time Protocol (PTP) module for the Ethernet Controller (EPTPC). The module applies the PTP as defined in version 2 of the IEEE 1588-2008 standard to handle timing and synchronization between devices. The EPTPC is composed of a Synchronization Frame Processing unit (SYNFP0) and a Statistical Time Correction Algorithm unit (STCA).

The EPTPC is used in combination with the on-chip Ethernet Controller (ETHERC) and the DMA Controller for the PTP Ethernet Controller (PTPEDMAC). When the EPTPC is not used, you can bypass it by setting the bypass registers in the EPTPC. See section 30.2.79, Bypass 1588 Module Register (BYPASS).

Table 30.1 lists the EPTPC specifications, and Figure 30.1 shows the configuration.

Table 30.1 EPTPC specifications

Parameter	Specifications
Protocol	Compliant with the Precision Time Protocol (PTP) defined in IEEE 1588.
Synchronization Frame Processing unit (SYNFP0)	• Transmission and reception of PTP messages as a master or slave • Support for clock device: - Ordinary clock (OC) • Calculation of meanPathDelay and offsetFromMaster as defined in IEEE 1588 • Capable of generating a master clock • Hardware filtering of received multicast packets with a MAC address • Capable of hardware filtering with the type of PTP message • Support for PTP message frames in layer 4 (IPv4 and UDP) and layer 2 (Ethernet frames) • Can be used as a normal Ethernet port when time synchronization is not in use
Statistical Time Correction Algorithm unit (STCA)	• Frequency of the clock supplied to the Statistical Time Correction Algorithm unit is selectable as 20, 25, 50, or 100 MHz • In slave operation, the synchronized state can be indicated by the offsetFromMaster value staying below a threshold specified in advance or calculated statistically from collected positive and negative gradient values (worst-10 acquisition) • Local clock counter holds corrected time information obtained from a master clock • STCA clock can be used as the clock source for generating pulse signals from pulse output timer m (m = 0 to 5) • Peripheral modules such as GPT can be started or stopped on the edge of pulses synchronized with the master clock in response to interrupt requests by the pulse output timer or the output of event signals to the ELC
Interrupt sources	ETHER_MINT interrupt: • Requested when the state of the individual modules is changed • Requested on rising edges of the pulse signal generated by the pulse output timer. ETHER_IPLS interrupt: • Requested on rising or falling edges of the pulse signal generated by the previously selected pulse output timer group • Can be requested on every edge or only once
Event linking	• Event signal is output to the ELC on a rising or falling edge of the pulse signal generated by the pulse output timer • Event signal can be output on every edge or only once

30. 以太网PTP控制器(EPTPC)

30.1 Overview

MCU为以太网控制器(EPTPC)提供片上精确时间协议(PTP)模块。该模块应用IEEE1588-2008标准第2版中定义的PTP来处理设备之间的定时和同步。EPTPC由同步帧处理单元（SYNFP0）和统计时间校正算法单元（STCA）组成。

EPTPC与片上以太网控制器(ETHERC)和用于PTP以太网控制器(PTPEDMAC)的DMA控制器结合使用。不使用EPTPC时，可以通过在
EPTPC。请参阅第30.2.79节，绕过1588模块寄存器(BYPASS)。

表30.1列出了EPTPC规格，图30.1显示了配置。

Table 30.1 EPTPC specifications

Parameter	Specifications
Protocol	符合IEEE1588中定义的精确时间协议(PTP)。
同步帧 处理单元(SYNFP0)	作为主机或从机发送和接收PTP消息 支持时钟设备：普通时钟(OC) 计算IEEE1588中定义的meanPathDelay和offsetFromMaster 能够生成主时钟 使用MAC地址 能够对PTP消息类型进行硬件过滤 支持第4层（IPv4和UDP）和第2层（以太网帧）中的PTP消息帧 在不使用时间同步时可用作普通以太网端口
统计时间 校正算法单元(STCA)	提供给StatisticalTimeCorrectionAlgorithm单元的时钟频率可选择为20、25、50或100MHz 在从属操作中，可以通过offsetFromMaster值保持在预先指定的阈值以下或统计计算来指示同步状态从收集的正负梯度值（最差10采集）本地时钟计数器保存从主时钟获得的校正时间信息STCA时钟可用作时钟源，用于从脉冲输出定时器m（m=0到5） GPT等外围模块可以在与主时钟同步的脉冲沿启动或停止，以响应脉冲输出定时器的中断请求或向ELC输出事件信号
中断源	ETHER_MINT中断： 当各个模块的状态改变时请求 在脉冲输出定时器产生的脉冲信号的上升沿请求。ETHER_IPLS中断： 在先前选择的脉冲输出定时器组生成的脉冲信号的上升沿或下降沿请求 可以在每个沿或仅一次请求
事件链接	事件信号在脉冲输出定时器产生的脉冲信号的上升沿或下降沿输出到ELC 事件信号可以在每个沿输出或仅输出一次

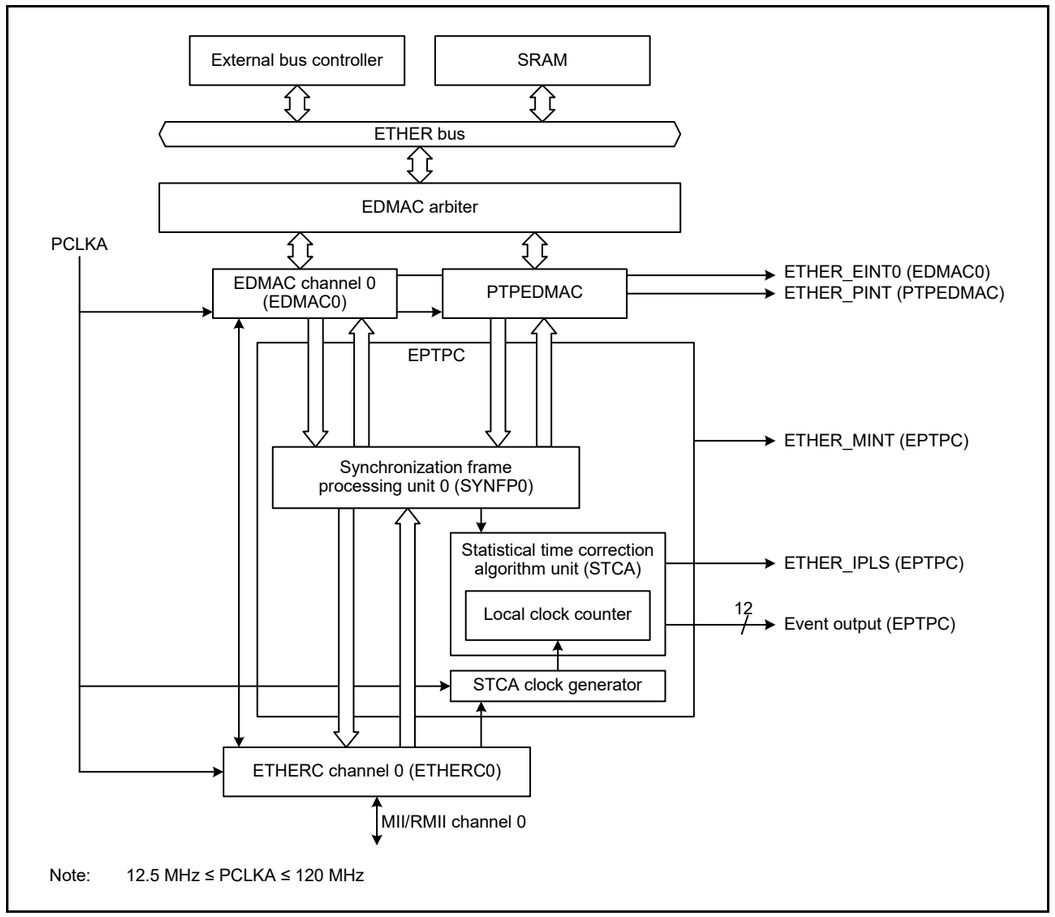


Figure 30.1 EPTPC configuration

In this section, individual channels might not be mentioned in the overall descriptions of modules that have multiple channels. Table 30.2 lists examples of the notation.

Table 30.2 Notation examples

Module name	Channel	Meaning
SYNFP module	One channel	Synchronization processing unit 0 (SYNFP0)
Pulse output timer m	m = 0 to 5	Pulse output timer channels 0 to 5

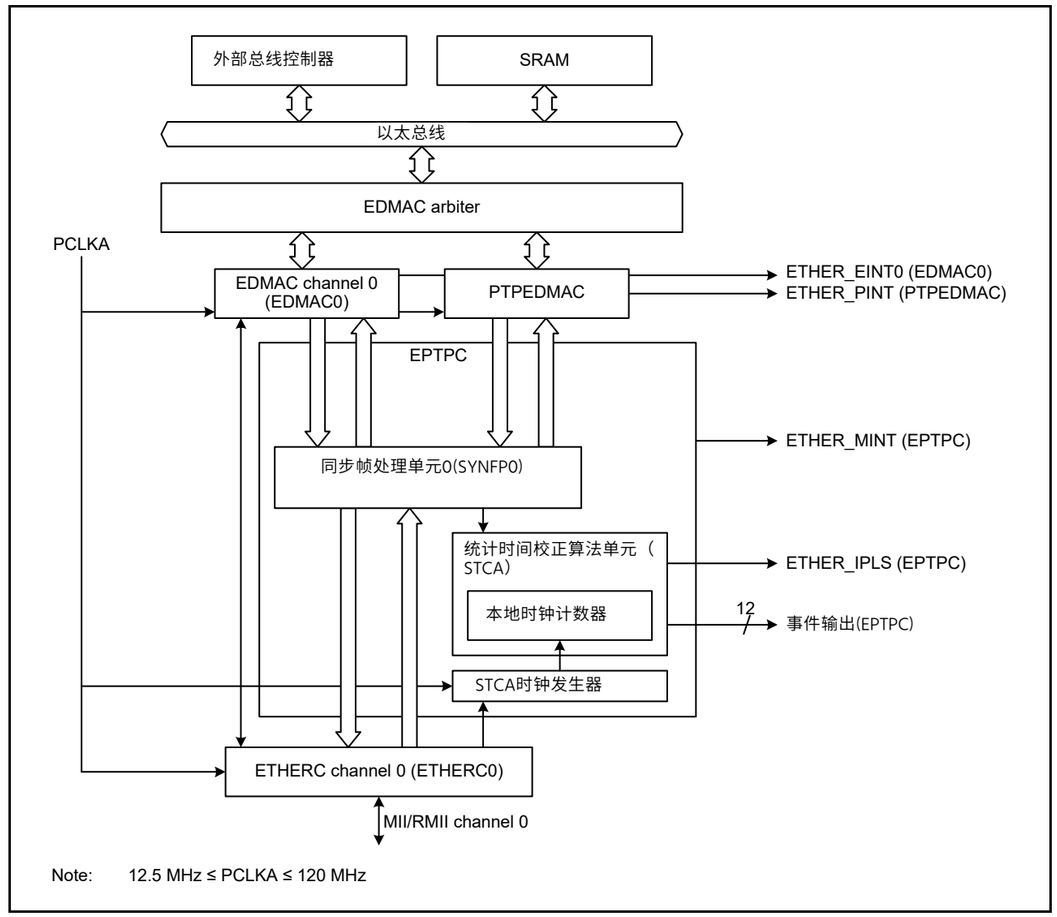


Figure 30.1 EPTPC configuration

在本节中，在对具有多个通道的模块的整体描述中可能不会提及单个通道。表30.2列出了该符号的示例。

Table 30.2 符号示例

模块名称	Channel	Meaning
SYNFP module	一个频道	同步处理单元0(SYNFP0)
脉冲输出定时器m	m = 0 to 5	脉冲输出定时器通道0到5

30.1.1 Combination of Clock Device and Ethernet Port

The EPTPC supports operation as one type of clock device:

- Ordinary clock (OC)

In addition, it supports both end-to-end (E2E) and peer-to-peer (P2P) operation. Table 30.3 lists the available combinations for usage of Ethernet ports 0.

Table 30.3 Combination of clock devices and Ethernet ports

Clock device	Ethernet port 0	
No control by EPTPC	PTP packets are not handled	
Ordinary clock (OC) Only Ethernet port 0 is used for handling PTP packets	Master	End-to-end (E2E)
		Peer-to-peer (P2P)
	Slave	E2E
		P2P

30.1.2 Frame Format of PTP Messages

The frame format of PTP messages can be selected from the four types by setting the FORM0 and FORM1 bits in the SYNFP Frame Format Setting Register (SYFORMR). Figure 30.2 shows the PTP message formats for transmission and reception by the EPTPC.

Ethernet header			Ethernet data
Destination MAC address	Source MAC address	Type	PTP messages

Ethernet header			Ethernet data		
Destination MAC address	Source MAC address	Length	LLC	SNAP	PTP messages

Ethernet header			Ethernet data		
Destination MAC address	Source MAC address	Type	IP header	UDP header	UDP data
					PTP messages

Ethernet header			Ethernet data				
Destination MAC address	Source MAC address	Length	LLC	SNAP	IP header	UDP header	UDP data
							PTP messages

Figure 30.2 Frame format of PTP messages

The EPTPC module is capable of transmitting PTP messages. When it sends a PTP message, multicast addresses as defined in IEEE 1588 are normally specified as the destination MAC address and IP address, depending on the type of PTP message to be sent. In addition, when a PTP message is encapsulated for use with UDP, the port number must also be specified in accordance with the message type, as stipulated in IEEE 1588.

Table 30.4 provides a summary of the information required to specify the Ethernet frame format for PTP messages.

30.1.1 时钟设备和以太网端口的组合

EPTPC支持作为一种时钟设备运行：

- 普通时钟(OC)

此外，它支持端到端(E2E)和点对点(P2P)操作。表30.3列出了以太网端口0的可用组合。

Table 30.3 时钟设备和以太网端口的组合

时钟装置	以太网端口0	
不受EPTPC控制	不处理PTP数据包	
普通时钟(OC) 仅以太网端口0用于处理PTP数据包	Master	End-to-end (E2E)
		Peer-to-peer (P2P)
	Slave	E2E
		P2P

30.1.2 PTP消息的帧格式

PTP消息的帧格式可以通过设置FORM0和FORM1位从四种类型中选择SYNFP帧格式设置寄存器(SYFORMR)。图30.2显示了EPTPC发送和接收的PTP消息格式。

以太网头			以太网数据
目标MAC地址	Source MAC地址	Type	PTP messages

以太网头			以太网数据		
目标MAC地址	MAC地址长度		LLC	SNAP	PTP messages

以太网头			以太网数据		
目标MAC地址	Source MAC地址	Type	IP头	UDP header	UDP data
					PTP messages

以太网头			以太网数据				
目标MAC地址	MAC地址长度		LLC	SNAP	IP头	UDP header	UDP data
							PTP messages

Figure 30.2 PTP消息的帧格式

EPTPC模块能够传输PTP消息。当它发送PTP消息时，IEEE1588中定义的多播地址通常指定为目标MAC地址和IP地址，具体取决于要发送的PTP消息的类型。此外，当PTP消息被封装用于UDP时，还必须按照IEEE1588的规定，根据消息类型指定端口号。

表30.4提供了为PTP消息指定以太网帧格式所需的信息摘要。

Table 30.4 PTP message types for multicast and information for specifying the Ethernet frame format

PTP message type			IEEE802.3 frame format (SYFORMR.FORM0 bit = 1)		Ethernet II frame format (SYFORMR.FORM0 bit = 0)		UDP port number*1
			MAC address	IP address	MAC address	Ethertype	
PTP-primary	Event messages	Sync	01-00-5E-00-01-81	224.0.1.129	01-1B-19-00-00-00	88F7h	319
		Delay_Req					
PTP-pdelay		Pdelay_Req	01-00-5E-00-00-6B	224.0.0.107	01-80-C2-00-00-0E		
		Pdelay_Resp					
	General messages	Pdelay_Resp_Follow_Up					320
PTP-primary		Announce	01-00-5E-00-01-81	224.0.1.129	01-1B-19-00-00-00		
		Follow_Up					
		Delay_Resp					
		Signaling					
		Management					

Note 1. The port number must be specified only when a PTP message is encapsulated for use with UDP, when the SYFORMR.FORM1 bit = 1.

30.1.3 PTP Message Type and Processing Details

Table 30.5 and Table 30.6 give details on EPTPC processing for receiving and transmitting PTP messages.

Table 30.5 Processing of PTP messages received by the EPTPC

Message type	Message	The EPTPC...
Event	Sync	Calculates the value of offsetFromMaster if twoStepFlag in flagField is FALSE
	Delay_Req	Responds to Delay_Resp
	Pdelay_Req	Responds to Pdelay_Resp
	Pdelay_Resp	Calculates the value of meanPathDelay if twoStepFlag in flagField is FALSE
General	Announce	—
	Follow_Up	Calculates the value of offsetFromMaster if twoStepFlag in flagField of the most recently received Sync message was TRUE and the value of meanPathDelay is fixed
	Delay_Resp	Calculates the value of meanPathDelay
	Pdelay_Resp_Follow_Up	Calculates the value of meanPathDelay if twoStepFlag in flagField of the most recently received Pdelay_Resp message was TRUE
	Management	—
	Signaling	—

Table 30.6 Processing of PTP messages to be transmitted by the EPTPC (1 of 2)

Message type	Message	The EPTPC...
Event	Sync	Transmits sync messages at the fixed interval specified in the SYTLIR.SYNC[7:0] bits
	Delay_Req	Proceeds with transmission with an interval from 0 to twice the interval set in the SYTLIR.DREQ[7:0] bits and determined by a random number
	Pdelay_Req	Transmits Pdelay_Req messages at the fixed interval specified in the SYTLIR.DREQ[7:0] bits
	Pdelay_Resp	Transmits responses to Pdelay_Req

Table 30.4 用于多播的PTP消息类型和用于指定以太网帧格式的信息

PTP消息类型			IEEE802.3帧格式（SYFORMR.FORM0位=1）		以太网II帧格式（SYFORMR.FORM0位=0）		UDP端口号*1
			MAC地址	IP地址	MAC地址	Ethertype	
PTP-primary	事件消息	Sync	01-00-5E-00-01-81	224.0.1.129	01-1B-19-00-00-00	88F7h	319
		Delay_Req					
PTP-pdelay		Pdelay_Req	01-00-5E-00-00-6B	224.0.0.107	01-80-C2-00-00-0E		
		Pdelay_Resp					
	一般信息	Pdelay_Resp_Follow_Up					320
PTP-primary		Announce	01-00-5E-00-01-81	224.0.1.129	01-1B-19-00-00-00		
		Follow_Up					
		Delay_Resp					
		Signaling					
		Management					

Note 1. 仅当PTP消息被封装以用于UDP时，当SYFORMR.FORM1位=1时，才必须指定端口号。

30.1.3 PTP消息类型和处理详细信息

表30.5和表30.6给出了关于接收和发送PTP消息的EPTPC处理的详细信息。

Table 30.5 处理EPTPC收到的PTP消息

消息类型	Message	The EPTPC...
Event	Sync	如果flagField中的twoStepFlag为FALSE，则计算offsetFromMaster的值
	Delay_Req	响应Delay_Resp
	Pdelay_Req	响应Pdelay_Resp
	Pdelay_Resp	如果flagField中的twoStepFlag为FALSE，则计算meanPathDelay的值
General	Announce	—
	Follow_Up	如果最近收到的Sync消息的flagField中的twoStepFlag为TRUE，并且meanPathDelay的值固定，则计算offsetFromMaster的值
	Delay_Resp	计算meanPathDelay的值
	Pdelay_Resp_Follow_Up	如果最近收到的Pdelay_Resp消息的flagField中的twoStepFlag为TRUE，则计算meanPathDelay的值
	Management	—
	Signaling	—

Table 30.6 处理由EPTPC传输的PTP消息（1of2）

消息类型	Message	The EPTPC...
Event	Sync	以SYTLIR.SYNC[7:0]位中指定的固定间隔发送同步消息
	Delay_Req	以0到2倍的间隔进行传输 SYTLIR.DREQ[7:0]位，由随机数确定
	Pdelay_Req	以SYTLIR.DREQ[7:0]位中指定的固定间隔发送Pdelay_Req消息
	Pdelay_Resp	将响应传输到Pdelay_Req

Table 30.6 Processing of PTP messages to be transmitted by the EPTPC (2 of 2)

Message type	Message	The EPTPC...
General	Announce	Transmits Announce messages at the fixed interval specified in the SYTLIR.ANCE[7:0] bits
	Follow_Up	—
	Delay_Resp	Transmits responses to Delay_Req
	Pdelay_Resp_Follow_Up	—
	Management	—
	Signaling	—

30.2 Register Descriptions

30.2.1 ETHER_MINT Interrupt Source Status Register (MIESR)

Address(es): EPTPC.MIESR 4006 5000h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	CYC5	CYC4	CYC3	CYC2	CYC1	CYC0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SY0	ST
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	ST	STCA Status Flag	0: No change in the state of the STCA unit 1: A change in the state of the STCA unit.	R
b1	SY0	SYNFP0 Status Flag	0: No change in the state of the SYNFP0 unit 1: A change in the state of the SYNFP0 unit.	R
b15 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b16	CYC0	Pulse Output Timer 0 Rising Edge Detection Flag	0: Rising edge not detected on the periodic pulse signal from pulse output timer 0 1: Rising edge detected on the periodic pulse signal from pulse output timer 0.	R/W*1
b17	CYC1	Pulse Output Timer 1 Rising Edge Detection Flag	0: Rising edge not detected on the periodic pulse signal from pulse output timer 1 1: A Rising edge detected on the periodic pulse signal from pulse output timer 1.	R/W*1
b18	CYC2	Pulse Output Timer 2 Rising Edge Detection Flag	0: Rising edge not detected on the periodic pulse signal from pulse output timer 2 1: A Rising edge detected on the periodic pulse signal from pulse output timer 2.	R/W*1
b19	CYC3	Pulse Output Timer 3 Rising Edge Detection Flag	0: Rising edge not detected on the periodic pulse signal from pulse output timer 3 1: A Rising edge detected on the periodic pulse signal from pulse output timer 3.	R/W*1
b20	CYC4	Pulse Output Timer 4 Rising Edge Detection Flag	0: Rising edge not detected on the periodic pulse signal from pulse output timer 4 1: A Rising edge detected on the periodic pulse signal from pulse output timer 4.	R/W*1
b21	CYC5	Pulse Output Timer 5 Rising Edge Detection Flag	0: Rising edge not detected on the periodic pulse signal from pulse output timer 5 1: A Rising edge detected on the periodic pulse signal from pulse output timer 5.	R/W*1

Table 30.6 处理由EPTPC传输的PTP消息(2of2)

消息类型 Message type	Message	The EPTPC...
General	Announce	以SYTLIR.ANCE[7:0]位中指定的固定间隔发送Announce消息
	Follow_Up	—
	Delay_Resp	将响应传输到Delay_Req
	Pdelay_Resp_Follow_Up	—
	Management	—
	Signaling	—

30.2 注册说明

30.2.1 ETHER_MINT中断源状态寄存器(MIESR)

Address(es): EPTPC.MIESR 4006 5000h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	CYC5	CYC4	CYC3	CYC2	CYC1	CYC0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SY0	ST
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	ST	STCA状态标志	0：STCA单元的状态没有变化1：STCA单元的状态有变化。	R
b1	SY0	SYNFP0状态标志	0：SYNFP0单元的状态没有变化1：SYNFP0单元的状态有变化。	R
b15 to b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b16	CYC0	脉冲输出定时器0上升边缘检测标志	0：未检测到来自脉冲输出定时器0的周期脉冲信号的上升沿1：检测到来自脉冲输出定时器0的周期脉冲信号的上升沿。	R/W*1
b17	CYC1	脉冲输出定时器1上升边缘检测标志	0：未检测到来自脉冲输出定时器1的周期脉冲信号的上升沿1：检测到来自脉冲输出定时器1的周期脉冲信号的上升沿。	R/W*1
b18	CYC2	脉冲输出定时器2上升边缘检测标志	0：未检测到来自脉冲输出定时器2的周期脉冲信号的上升沿1：检测到来自脉冲输出定时器2的周期脉冲信号的上升沿。	R/W*1
b19	CYC3	脉冲输出定时器3上升边缘检测标志	0：未检测到来自脉冲输出定时器3的周期脉冲信号的上升沿1：检测到来自脉冲输出定时器3的周期脉冲信号的上升沿。	R/W*1
b20	CYC4	脉冲输出定时器4上升边缘检测标志	0：未检测到来自脉冲输出定时器4的周期脉冲信号的上升沿1：检测到来自脉冲输出定时器4的周期脉冲信号的上升沿。	R/W*1
b21	CYC5	脉冲输出定时器5上升边缘检测标志	0：未检测到来自脉冲输出定时器5的周期脉冲信号的上升沿1：检测到来自脉冲输出定时器5的周期脉冲信号的上升沿。	R/W*1

Bit	Symbol	Bit name	Description	R/W
b31 to b22	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Writing 1 clears the flag. Writing 0 does not affect the flag value.

The MIESR register indicates changes in the states of the STCA and SYNFP0 units, which act as ETHER_MINT interrupt sources, and enables the detection of rising edges on pulse output timers m (m = 0 to 5). For more the ETHER_MINT interrupt, see section 30.4, Interrupts.

ST flag (STCA Status Flag)

The ST flag indicates changes in the state of the STCA unit.

[Setting condition]

- A change in the state of a flag in the STSR register for which notification is enabled in the STIPR register.

[Clearing conditions]

When any of the following conditions is met:

- The flags in the STSR register are all 0
- The bits in the STIPR register are all 0
- A bit is set to 1 in the STIPR register, but the associated flag in the STSR register is 0.

SY0 flag (SYNFP0 Status Flag)

The SY0 flag indicates changes in the state of the SYNFP0 unit.

[Setting condition]

- A change in the state of a flag in the SYSR register for which notification is enabled in the SYIPR register.

[Clearing conditions]

When any of the following conditions is met:

- The flags in the SYSR register are all 0
- The bits in the SYIPR register are all 0
- A bit is set to 1 in the SYIPR register, but the associated flag in the SYSR register is 0.

CYCm flag (Pulse Output Timer m Rising Edge Detection Flag)

The CYCm flag indicates detection of a rising edge on the periodic pulse signal produced by the associated pulse output timer m (m = 0 to 5).

[Setting condition]

- Detection of a rising edge on the periodic pulse signal produced by a pulse output timer for which notification is enabled in the MITSELR register.

[Clearing condition]

- 1 is written to this flag.
  After the flag is cleared to 0, it is set to 1 again on detection of a rising edge on the periodic pulse signal from the associated pulse output timer.

Bit	Symbol	位名称	Description	R/W
b31 to b22	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 写1清除标志。写入0不影响标志值。

MIESR寄存器指示STCA和SYNFP0单元的状态变化，它们充当ETHER_MINT中断源，并启用脉冲输出定时器m（m=0到5）上的上升沿检测。有关ETHER_MINT中断的更多信息，请参阅第30.4节，中断。

ST标志（STCA状态标志）

ST标志指示STCA单元状态的变化。

[Setting condition]

- STSR寄存器中标志状态的变化，在STIPR寄存器中启用通知。

[Clearing conditions]

当满足以下任一条件时：

- STSR寄存器中的标志全为0
- STIPR寄存器中的位全为0
- STIPR寄存器中的某个位设置为1，但STSR寄存器中的相关标志为0。

SY0标志（SYNFP0状态标志）

SY0标志指示SYNFP0单元状态的变化。

[Setting condition]

- SYSR寄存器中标志状态的变化，在SIIPR寄存器中启用通知。

[Clearing conditions]

当满足以下任一条件时：

- SYSR寄存器中的标志位全为0
- SYIPR寄存器中的位全为0
- SYIPR寄存器中的某个位设置为1，但SYSR寄存器中的相关标志为0。

CYCm标志（脉冲输出定时器m上升沿检测标志）

CYCm标志表示检测到由相关脉冲输出定时器m（m=0到5）产生的周期性脉冲信号的上升沿。

[Setting condition]

- 检测脉冲输出定时器产生的周期性脉冲信号的上升沿，在MITSELR寄存器中启用通知。

[Clearing condition]

- 1写入该标志。标志清除为0后，在检测到来自相关脉冲输出定时器的周期脉冲信号的上升沿时再次设置为1。

30.2.2 ETHER_MINT Interrupt Request Enable Register (MIEIPR)

Address(es): EPTPC.MIEIPR 4006 5004h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	CYC5	CYC4	CYC3	CYC2	CYC1	CYC0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SY0	ST
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	ST	STCA Status Interrupt Request Enable	0: Disable generation of ETHER_MINT interrupt requests by the STCA status flag 1: Enable generation of ETHER_MINT interrupt requests by the STCA status flag.	R/W
b1	SY0	SYNFP0 Status Interrupt Request Enable	0: Disable generation of ETHER_MINT interrupt requests by the SYNFP0 status flag 1: Enable generation of ETHER_MINT interrupt requests by the SYNFP0 status flag.	R/W
b15 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b16	CYC0	Pulse Output Timer 0 Rising Edge Detection Interrupt Request Enable	0: Disable generation of ETHER_MINT interrupt requests on detection of a rising edge of pulse output timer 0 1: Enable generation of ETHER_MINT interrupt requests on detection of a rising edge of pulse output timer 0.	R/W
b17	CYC1	Pulse Output Timer 1 Rising Edge Detection Interrupt Request Enable	0: Disable generation of ETHER_MINT interrupt requests on detection of a rising edge of pulse output timer 1 1: Enable generation of ETHER_MINT interrupt requests on detection of a rising edge of pulse output timer 1.	R/W
b18	CYC2	Pulse Output Timer 2 Rising Edge Detection Interrupt Request Enable	0: Disable generation of ETHER_MINT interrupt requests on detection of a rising edge of pulse output timer 2 1: Enable generation of ETHER_MINT interrupt requests on detection of a rising edge of pulse output timer 2.	R/W
b19	CYC3	Pulse Output Timer 3 Rising Edge Detection Interrupt Request Enable	0: Disable generation of ETHER_MINT interrupt requests on detection of a rising edge of pulse output timer 3 1: Enable generation of ETHER_MINT interrupt requests on detection of a rising edge of pulse output timer 3.	R/W
b20	CYC4	Pulse Output Timer 4 Rising Edge Detection Interrupt Request Enable	0: Disable generation of ETHER_MINT interrupt requests on detection of a rising edge of pulse output timer 4 1: Enable generation of ETHER_MINT interrupt requests on detection of a rising edge of pulse output timer 4.	R/W
b21	CYC5	Pulse Output Timer 5 Rising Edge Detection Interrupt Request Enable	0: Disable generation of ETHER_MINT interrupt requests on detection of a rising edge of pulse output timer 5 1: Enable generation of ETHER_MINT interrupt requests on detection of a rising edge of pulse output timer 5.	R/W
b31 to b22	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The MIEIPR register enables or disables the generation of ETHER_MINT interrupt requests when ETHER_MINT interrupt source conditions are satisfied.

30.2.2 ETHER_MINT中断请求使能寄存器(MIEIPR)

Address(es): EPTPC.MIEIPR 4006 5004h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	CYC5	CYC4	CYC3	CYC2	CYC1	CYC0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SY0	ST
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	ST	STCA状态中断请求启用	0：通过STCA状态标志禁止产生ETHER_MINT中断请求1：通过STCA状态标志允许产生ETHER_MINT中断请求。	R/W
b1	SY0	SYNFP0状态中断请求启用	0：通过SYNFP0状态标志禁止产生ETHER_MINT中断请求1：通过SYNFP0状态标志允许产生ETHER_MINT中断请求。	R/W
b15 to b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b16	CYC0	脉冲输出定时器0上升边缘检测中断请求启用	0：在检测到脉冲输出定时器0的上升沿时禁止产生ETHER_MINT中断请求1：在检测到脉冲输出定时器0的上升沿时允许产生ETHER_MINT中断请求。	R/W
b17	CYC1	脉冲输出定时器1上升边缘检测中断请求启用	0：在检测到脉冲输出定时器1的上升沿时禁止产生ETHER_MINT中断请求1：在检测到脉冲输出定时器1的上升沿时允许产生ETHER_MINT中断请求。	R/W
b18	CYC2	脉冲输出定时器2上升边缘检测中断请求启用	0：在检测到脉冲输出定时器2的上升沿时禁止产生ETHER_MINT中断请求1：在检测到脉冲输出定时器2的上升沿时允许产生ETHER_MINT中断请求。	R/W
b19	CYC3	脉冲输出定时器3上升边缘检测中断请求启用	0：在检测到脉冲输出定时器3的上升沿时禁止产生ETHER_MINT中断请求1：在检测到脉冲输出定时器3的上升沿时允许产生ETHER_MINT中断请求。	R/W
b20	CYC4	脉冲输出定时器4上升边缘检测中断请求启用	0：在检测到脉冲输出定时器4的上升沿时禁止产生ETHER_MINT中断请求1：在检测到脉冲输出定时器4的上升沿时允许产生ETHER_MINT中断请求。	R/W
b21	CYC5	脉冲输出定时器5上升边缘检测中断请求启用	0：在检测到脉冲输出定时器5的上升沿时禁止产生ETHER_MINT中断请求1：在检测到脉冲输出定时器5的上升沿时允许产生ETHER_MINT中断请求。	R/W
b31 to b22	—	Reserved	这些位被读取为0。写入值应为0。	R/W

当ETHER_MINT中断源条件满足时，MIEIPR寄存器启用或禁用ETHER_MINT中断请求的生成。

30.2.3 ELC Output/ETHER_IPLS Interrupt Request Permission Register (ELIPPR)

Address(es): EPTPC.ELIPPR 4006 5010h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	PLSN	—	—	—	—	—	—	—	PLSP
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	CYCN5	CYCN4	CYCN3	CYCN2	CYCN1	CYCN0	—	—	CYCP5	CYCP4	CYCP3	CYCP2	CYCP1	CYCP0
Value after reset:	0	0	1	1	1	1	1	1	0	0	1	1	1	1	1	1

Bit	Symbol	Bit name	Description	R/W
b0	CYCP0	Pulse Output Timer 0 Rising Edge Detection Event Output Enable	0: Do not output rising edges of pulse output timer 0 to the ELC as event signals 1: Output rising edges of pulse output timer 0 to the ELC as event signals.	R/W
b1	CYCP1	Pulse Output Timer 1 Rising Edge Detection Event Output Enable	0: Do not output rising edges of pulse output timer 1 to the ELC as event signals 1: Output rising edges of pulse output timer 1 to the ELC as event signals.	R/W
b2	CYCP2	Pulse Output Timer 2 Rising Edge Detection Event Output Enable	0: Do not output rising edges of pulse output timer 2 to the ELC as event signals 1: Output rising edges of pulse output timer 2 to the ELC as event signals.	R/W
b3	CYCP3	Pulse Output Timer 3 Rising Edge Detection Event Output Enable	0: Do not output rising edges of pulse output timer 3 to the ELC as event signals 1: Output rising edges of pulse output timer 3 to the ELC as event signals.	R/W
b4	CYCP4	Pulse Output Timer 4 Rising Edge Detection Event Output Enable	0: Do not output rising edges of pulse output timer 4 to the ELC as event signals 1: Output rising edges of pulse output timer 4 to the ELC as event signals.	R/W
b5	CYCP5	Pulse Output Timer 5 Rising Edge Detection Event Output Enable	0: Do not output rising edges of pulse output timer 5 to the ELC as event signals 1: Rising edges of the signal from pulse output timer 5 to the ELC as event signals.	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	CYCN0	Pulse Output Timer 0 Falling Edge Detection Event Output Enable	0: Do not output falling edges of pulse output timer 0 to the ELC as event signals 1: Output falling edges of pulse output timer 0 to the ELC as event signals.	R/W
b9	CYCN1	Pulse Output Timer 1 Falling Edge Detection Event Output Enable	0: Do not output falling edges of pulse output timer 1 to the ELC as event signals 1: Output falling edges of pulse output timer 1 to the ELC as event signals.	R/W
b10	CYCN2	Pulse Output Timer 2 Falling Edge Detection Event Output Enable	0: Do not output falling edges of pulse output timer 2 to the ELC as event signals 1: Output falling edges of pulse output timer 2 to the ELC as event signals.	R/W
b11	CYCN3	Pulse Output Timer 3 Falling Edge Detection Event Output Enable	0: Do not output falling edges of pulse output timer 3 to the ELC as event signals 1: Output falling edges of pulse output timer 3 to the ELC as event signals.	R/W

30.2.3 ELC输出ETHER_IPLS中断请求许可寄存器(ELIPPR)

Address(es): EPTPC.ELIPPR 4006 5010h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	PLSN	—	—	—	—	—	—	—	PLSP
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	CYCN5	CYCN4	CYCN3	CYCN2	CYCN1	CYCN0	—	—	CYCP5	CYCP4	CYCP3	CYCP2	CYCP1	CYCP0
重置后的值:	0	0	1	1	1	1	1	1	0	0	1	1	1	1	1	1

Bit	Symbol	位名称	Description	R/W
b0	CYCP0	脉冲输出定时器0上升沿检测事件输出 Enable	0：不将脉冲输出定时器0的上升沿作为事件信号输出到ELC1：将脉冲输出定时器0的上升沿作为事件信号输出到ELC。	R/W
b1	CYCP1	脉冲输出定时器1上升沿检测事件输出 Enable	0：不将脉冲输出定时器1的上升沿作为事件信号输出到ELC1：将脉冲输出定时器1的上升沿作为事件信号输出到ELC。	R/W
b2	CYCP2	脉冲输出定时器2上升沿检测事件输出 Enable	0：不将脉冲输出定时器2的上升沿作为事件信号输出到ELC1：将脉冲输出定时器2的上升沿作为事件信号输出到ELC。	R/W
b3	CYCP3	脉冲输出定时器3上升沿检测事件输出 Enable	0：不将脉冲输出定时器3的上升沿作为事件信号输出到ELC1：将脉冲输出定时器3的上升沿作为事件信号输出到ELC。	R/W
b4	CYCP4	脉冲输出定时器4上升沿检测事件输出 Enable	0：不将脉冲输出定时器4的上升沿作为事件信号输出到ELC1：将脉冲输出定时器4的上升沿作为事件信号输出到ELC。	R/W
b5	CYCP5	脉冲输出定时器5上升沿检测事件输出 Enable	0：不将脉冲输出定时器5的上升沿作为事件信号输出到ELC1：脉冲输出定时器5的信号上升沿作为事件信号输出到ELC。	R/W
b7, b6	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b8	CYCN0	脉冲输出定时器0下降沿检测事件输出 Enable	0：不将脉冲输出定时器0的下降沿作为事件信号输出到ELC1：将脉冲输出定时器0的下降沿作为事件信号输出到ELC。	R/W
b9	CYCN1	脉冲输出定时器1下降沿检测事件输出 Enable	0：不将脉冲输出定时器1的下降沿作为事件信号输出到ELC1：将脉冲输出定时器1的下降沿作为事件信号输出到ELC。	R/W
b10	CYCN2	脉冲输出定时器2下降沿检测事件输出 Enable	0：不将脉冲输出定时器2的下降沿作为事件信号输出到ELC1：将脉冲输出定时器2的下降沿作为事件信号输出到ELC。	R/W
b11	CYCN3	脉冲输出定时器3下降沿检测事件输出 Enable	0：不将脉冲输出定时器3的下降沿作为事件信号输出到ELC1：将脉冲输出定时器3的下降沿作为事件信号输出到ELC。	R/W

Bit	Symbol	Bit name	Description	R/W
b12	CYCN4	Pulse Output Timer 4 Falling Edge Detection Event Output Enable	0: Do not output falling edges of pulse output timer 4 to the ELC as event signals 1: Output falling edges of pulse output timer 4 to the ELC as event signals.	R/W
b13	CYCN5	Pulse Output Timer 5 Falling Edge Detection Event Output Enable	0: Do not output falling edges of pulse output timer 5 to the ELC as event signals 1: Output falling edges of pulse output timer 5 to the ELC as event signals.	R/W
b15, b14	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b16	PLSP	Pulse Output Timer Rising Edge Detection ETHER_IPLS Interrupt Request Enable	0: Disable ETHER_IPLS interrupt requests triggered by rising edges of signals from the selected pulse output timer 1: Enable ETHER_IPLS interrupt requests triggered by rising edges of signals from the selected pulse output timer.	R/W
b23 to b17	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b24	PLSN	Pulse Output Timer Falling Edge Detection ETHER_IPLS Interrupt Request Enable	0: Disable ETHER_IPLS interrupt requests triggered by falling edges of signals from the selected pulse output timer 1: Enable ETHER_IPLS interrupt requests triggered by falling edges of signals from the selected pulse output timer.	R/W
b31 to b25	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The ELIPPR register determines whether rising and falling edges of the periodic pulse signals produced by pulse output timers m are output as event signals to the ELC. The register also enables or disables ETHER_IPLS interrupts triggered by rising or falling edges of signals from the pulse output timer selected in the IPTSELR register.

Peripheral modules such as the GPT can be controlled with the clock synchronized by the PTP by using the ELC linking function to set a periodic pulse generated by pulse output timer m as a trigger for operations of the peripheral module.

The ELIPACR register can be used to set up the one-time-only output of event signals to the ELC or of ETHER_IPLS interrupt requests. For more on the ETHER_IPLS interrupt, see section 30.4, Interrupts.

30.2.4 ELC Output/ETHER_IPLS Interrupt Permission Automatic Clearing Register (ELIPACR)

Address(es): EPTPC.ELIPACR 4006 5014h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	PLSN	—	—	—	—	—	—	—	PLSP
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	CYCN5	CYCN4	CYCN3	CYCN2	CYCN1	CYCN0	—	—	CYCP5	CYCP4	CYCP3	CYCP2	CYCP1	CYCP0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	CYCP0	ELIPPR.CYCP0 Bit Automatic Clearing	0: Disable automatic clearing of enable bit for output of rising edges of pulse output timer 0 1: Enable automatic clearing of enable bit for output of rising edges of pulse output timer 0.	R/W
b1	CYCP1	ELIPPR.CYCP1 Bit Automatic Clearing	0: Disable automatic clearing of enable bit for output of rising edges of pulse output timer 1 1: Enable automatic clearing of enable bit for output of rising edges of pulse output timer 1.	R/W
b2	CYCP2	ELIPPR.CYCP2 Bit Automatic Clearing	0: Disable automatic clearing of enable bit for output of rising edges of pulse output timer 2 1: Enable automatic clearing of enable bit for output of rising edges of pulse output timer 2.	R/W

Bit	Symbol	位名称	Description	R/W
b12	CYCN4	脉冲输出定时器4下降沿检测事件输出 Enable	0：不将脉冲输出定时器4的下降沿作为事件信号输出到ELC1：将脉冲输出定时器4的下降沿作为事件信号输出到ELC。	R/W
b13	CYCN5	脉冲输出定时器5下降沿检测事件输出 Enable	0：不将脉冲输出定时器5的下降沿作为事件信号输出到ELC1：将脉冲输出定时器5的下降沿作为事件信号输出到ELC。	R/W
b15, b14	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b16	PLSP	脉冲输出定时器上升边缘检测ETHER_IPLS中断请求使能	0：禁用由所选脉冲输出定时器的信号上升沿触发的ETHER_IPLS中断请求1：启用由所选脉冲输出定时器的信号上升沿触发的ETHER_IPLS中断请求。	R/W
b23 to b17	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b24	PLSN	脉冲输出定时器下降边缘检测ETHER_IPLS中断请求使能	0：禁用由来自所选脉冲输出定时器的信号下降沿触发的ETHER_IPLS中断请求1：启用由来自所选脉冲输出定时器的信号下降沿触发的ETHER_IPLS中断请求。	R/W
b31 to b25	—	Reserved	这些位被读取为0。写入值应为0。	R/W

ELIPPR寄存器决定脉冲输出定时器m产生的周期脉冲信号的上升沿和下降沿是否作为事件信号输出到ELC。该寄存器还启用或禁用由来自IPTSELR寄存器中选择的脉冲输出定时器的信号的上升沿或下降沿触发的ETHER_IPLS中断。

GPT等外围模块可以通过PTP同步的时钟进行控制，方法是使用ELC链接功能将脉冲输出定时器m产生的周期脉冲设置为外围模块操作的触发器。

ELIPACR寄存器可用于设置事件信号到ELC或ETHER_IPLS中断请求的一次性输出。有关ETHER_IPLS中断的更多信息，请参阅第30.4节，中断。

30.2.4 ELC输出ETHER_IPLS中断许可自动清除寄存器(ELIPACR)

Address(es): EPTPC.ELIPACR 4006 5014h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	PLSN	—	—	—	—	—	—	—	PLSP
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	CYCN5	CYCN4	CYCN3	CYCN2	CYCN1	CYCN0	—	—	CYCP5	CYCP4	CYCP3	CYCP2	CYCP1	CYCP0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	CYCP0	ELIPPR.CYCP0位自动Clearing	0：禁止自动清除脉冲输出定时器0上升沿输出使能位1：使能自动清除脉冲输出定时器0上升沿输出使能位。	R/W
b1	CYCP1	ELIPPR.CYCP1位自动Clearing	0：禁止自动清除脉冲输出定时器1上升沿输出使能位1：使能自动清除脉冲输出定时器1上升沿输出使能位。	R/W
b2	CYCP2	ELIPPR.CYCP2位自动Clearing	0：禁止自动清除脉冲输出定时器2上升沿输出使能位1：使能自动清除脉冲输出定时器2上升沿输出使能位。	R/W

Bit	Symbol	Bit name	Description	R/W
b3	CYCP3	ELIPPR.CYCP3 Bit Automatic Clearing	0: Disable automatic clearing of enable bit for output of rising edges of pulse output timer 3 1: Enable automatic clearing of enable bit for output of rising edges of pulse output timer 3.	R/W
b4	CYCP4	ELIPPR.CYCP4 Bit Automatic Clearing	0: Disable automatic clearing of enable bit for output of rising edges of pulse output timer 4 1: Enable automatic clearing of enable bit for output of rising edges of pulse output timer 4.	R/W
b5	CYCP5	ELIPPR.CYCP5 Bit Automatic Clearing	0: Disable automatic clearing of enable bit for output of rising edges of pulse output timer 5 1: Enable automatic clearing of enable bit for output of rising edges of pulse output timer 5.	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	CYCN0	ELIPPR.CYCN0 Bit Automatic Clearing	0: Disable automatic clearing of enable bit for output of falling edges of pulse output timer 0 1: Enable automatic clearing of enable bit for output of falling edges of pulse output timer 0.	R/W
b9	CYCN1	ELIPPR.CYCN1 Bit Automatic Clearing	0: Disable automatic clearing of enable bit for output of falling edges of pulse output timer 1 1: Enable automatic clearing of enable bit for output of falling edges of pulse output timer 1.	R/W
b10	CYCN2	ELIPPR.CYCN2 Bit Automatic Clearing	0: Disable automatic clearing of enable bit for output of falling edges of pulse output timer 2 1: Enable automatic clearing of enable bit for output of falling edges of pulse output timer 2.	R/W
b11	CYCN3	ELIPPR.CYCN3 Bit Automatic Clearing	0: Disable automatic clearing of enable bit for output of falling edges of pulse output timer 3 1: Enable automatic clearing of enable bit for output of falling edges of pulse output timer 3.	R/W
b12	CYCN4	ELIPPR.CYCN4 Bit Automatic Clearing	0: Disable automatic clearing of enable bit for output of falling edges of pulse output timer 4 1: Enable automatic clearing of enable bit for output of falling edges of pulse output timer 4.	R/W
b13	CYCN5	ELIPPR.CYCN5 Bit Automatic Clearing	0: Disable automatic clearing of enable bit for output of falling edges of pulse output timer 5 1: Enable automatic clearing of enable bit for output of falling edges of pulse output timer 5.	R/W
b15, b14	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b16	PLSP	ELIPPR.PLSP Bit Automatic Clearing	0: Disable automatic clearing of enable bit for ETHER_IPLS interrupt requests on detection of rising edges of the pulse output timer 1: Enable automatic clearing of enable bit for ETHER_IPLS interrupt requests on detection of rising edges of the pulse output timer.	R/W
b23 to b17	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b24	PLSN	ELIPPR.PLSN Bit Automatic Clearing	0: Disable automatic clearing of enable bit for ETHER_IPLS interrupt requests on detection of falling edges of the pulse output timer 1: Enable automatic clearing of enable bit for ETHER_IPLS interrupt requests on detection of falling edges of the pulse output timer.	R/W
b31 to b25	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The ELIPACR register enables one-time output of each event to the ELC or each ETHER_IPLS interrupt request triggered by detecting edges of the periodic pulses of pulse output timer m. Normally, an event is output to the ELC or an ETHER_IPLS interrupt request is generated on each edge of the periodic pulses of pulse output timer m while the associated bit in the ELIPPR register is 1 (enabled). When a bit in the ELIPPR register is 1 while the associated bit in the ELIPACR register is also 1, the bit in the ELIPPR register automatically clears to 0 when the event signal for the ELC or ETHER_IPLS interrupt request is generated. For more on the ETHER_IPLS interrupt, see section 30.4, Interrupts.

Bit	Symbol	位名称	Description	R/W
b3	CYCP3	ELIPPR.CYCP3位自动Clearing	0：禁止自动清除脉冲输出定时器3上升沿输出使能位1：使能脉冲输出定时器3上升沿输出使能位自动清除。	R/W
b4	CYCP4	ELIPPR.CYCP4位自动Clearing	0：禁止自动清除脉冲输出定时器4上升沿输出使能位1：使能自动清除脉冲输出定时器4上升沿输出使能位。	R/W
b5	CYCP5	ELIPPR.CYCP5位自动Clearing	0：禁止自动清除脉冲输出定时器5上升沿输出使能位1：使能自动清除脉冲输出定时器5上升沿输出使能位。	R/W
b7, b6	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b8	CYCN0	ELIPPR.CYCN0位自动Clearing	0：禁止自动清除脉冲输出定时器0下降沿输出使能位1：使能脉冲输出定时器0下降沿输出使能位自动清除。	R/W
b9	CYCN1	ELIPPR.CYCN1位自动Clearing	0：禁止自动清除脉冲输出定时器1下降沿输出使能位1：使能自动清除脉冲输出定时器1下降沿输出使能位。	R/W
b10	CYCN2	ELIPPR.CYCN2位自动Clearing	0：禁止自动清除脉冲输出定时器2下降沿输出使能位1：使能自动清除脉冲输出定时器2下降沿输出使能位。	R/W
b11	CYCN3	ELIPPR.CYCN3位自动Clearing	0：禁止自动清除脉冲输出定时器3下降沿输出使能位1：使能脉冲输出定时器3下降沿输出使能位自动清除。	R/W
b12	CYCN4	ELIPPR.CYCN4位自动Clearing	0：禁止自动清除脉冲输出定时器4下降沿输出使能位1：使能自动清除脉冲输出定时器4下降沿输出使能位。	R/W
b13	CYCN5	ELIPPR.CYCN5位自动Clearing	0：禁止自动清除脉冲输出定时器5下降沿输出使能位1：使能自动清除脉冲输出定时器5下降沿输出使能位。	R/W
b15, b14	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b16	PLSP	ELIPPR.PLSP位自动Clearing	0：禁止在检测到脉冲输出定时器的上升沿时自动清除ETHER_IPLS中断请求的使能位1：使能在检测到脉冲输出定时器的上升沿时自动清除ETHER_IPLS中断请求的使能位。	R/W
b23 to b17	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b24	PLSN	ELIPPR.PLSN位自动Clearing	0：禁止在检测到脉冲输出定时器的下降沿时自动清除ETHER_IPLS中断请求的使能位1：使能在检测到脉冲输出定时器的下降沿时自动清除ETHER_IPLS中断请求的使能位。	R/W
b31 to b25	—	Reserved	这些位被读取为0。写入值应为0。	R/W

ELIPACR寄存器允许将每个事件一次性输出到ELC或通过检测脉冲输出定时器m的周期性脉冲的边沿触发的每个ETHER_IPLS中断请求。通常，当ELIPPR寄存器中的相关位为1（启用）时，在脉冲输出定时器m的周期脉冲的每个边沿上都会向ELC输出一个事件或一个ETHER_IPLS中断请求。当ELIPPR寄存器中的某个位为1且ELIPACR寄存器中的相关位也为1时，ELIPPR寄存器中的位会在ELC或

ETHER_IPLS中断请求产生。有关ETHER_IPLS中断的更多信息，请参阅第30.4节，中断。

30.2.5 STCA Status Register (STSR)

Address(es): EPTPC.STSR 4006 5040h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	W10D	SYNTOUT	—	SYNCOUT	SYNC
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	SYNC	Synchronized State Detection Flag	0: Synchronization not detected 1: Synchronization detected.	R/W*1
b1	SYNCOUT	Synchronization Loss Detection Flag	0: Loss of synchronization not detected 1: Loss of synchronization detected.	R/W*1
b2	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b3	SYNTOUT	Sync Message Reception Timeout Detection Flag	0: Sync message reception timeout not detected 1: Sync message reception timeout detected.	R/W*1
b4	W10D	Worst 10 Acquisition Completion Flag	0: Ten worst values not acquired yet 1: Ten worst values acquired.	R/W*1
b31 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: When the SYNSTARTR.STR bit is 0, the value of the associated flag stays the same.
Note 1. Writing 1 clears the flag. Writing 0 does not affect the flag value.

The STSR register indicates the state of the STCA module.

SYNC flag (Synchronized State Detection Flag)

The SYNC flag indicates that synchronization has occurred more than the number of times specified in the STMR.SYTH[3:0] bits in succession when the STMR.ALEN0 bit is 1. When the STMR.ALEN0 bit is 0, the SYNC flag is not set to 1 even if synchronization has occurred more than the specified number of times in succession.

SYNCOUT flag (Synchronization Loss Detection Flag)

The SYNCOUT flag indicates that loss of synchronization has occurred more than the number of times specified in the STMR.DVTH[3:0] bits in succession when the STMR.ALEN0 bit is 1. Because the time is not synchronized immediately after time synchronization is started (when the SYNSTARTR.STR bit is set to 1), SYNCOUT is set to 1 regardless of the STMR.ALEN0 bit setting. When using the SYNTOUT flag, set the SYNTOUT flag to 0 immediately after starting time synchronization.

When the STMR.ALEN0 bit is 0, the SYNCOUT flag is not set to 1 even if loss of synchronization occurs more than the specified number of times in succession after time synchronization starts and the SYNTOUT flag is immediately set to 0.

SYNTOUT flag (Sync Message Reception Timeout Detection Flag)

The SYNTOUT flag indicates that a Sync message was not received during the period specified in the SYNTOR register when the STMR.ALEN1 bit is 1. The SYNTOUT flag is set to 1 immediately after time synchronization is started (when the SYNSTARTR.STR bit is set to 1) when no Sync message is received after the EPTPC starts. When using the SYNTOUT flag, set the SYNTOUT flag to 0 immediately after starting time synchronization.

W10D flag (Worst 10 Acquisition Completion Flag)

The W10D flag indicates that acquisition of the worst 10 values is complete.

30.2.5 STCA状态寄存器(STSR)

Address(es): EPTPC.STSR 4006 5040h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	W10D	SYNTOUT	—	SYNCOUT	SYNC
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	SYNC	同步状态检测Flag	0：未检测到同步1：检测到同步。	R/W*1
b1	SYNCOUT	同步丢失检测Flag	0：未检测到同步丢失1：检测到同步丢失。	R/W*1
b2	—	Reserved	该位读取为0。写入值应为0。	R/W
b3	SYNTOUT	同步消息接收超时检测标志	0：未检测到同步消息接收超时1：检测到同步消息接收超时。	R/W*1
b4	W10D	最差10次收购完成标志	0：尚未获取10个最差值1：已获取10个最差值。	R/W*1
b31 to b5	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note: 当SYNSTARTR.STR位为0时，相关标志的值保持不变。
Note 1. 写1清除标志。写入0不影响标志值。

STSR寄存器指示STCA模块的状态。

SYNC标志（同步状态检测标志）

SYNC标志表示当STMR.ALEN0位为1时，同步发生的次数连续超过STMR.SYTH[3:0]位中指定的次数。当STMR.ALEN0位为0时，SYNC标志为即使同步已连续发生超过指定次数，也不会设置为1。

SYNCOUT标志（同步丢失检测标志）

SYNCOUT标志表示同步丢失发生的次数超过了在
当STMR.ALEN0位为1时，STMR.DVTH[3:0]位连续。因为在时间同步开始后（当SYNSTARTR.STR位设置为1时）时间不会立即同步，所以SYNCOUT设置为1无论STMR.ALEN0位设置如何。使用SYNTOUT标志时，在开始时间同步后立即将SYNTOUT标志设置为0。

当STMR.ALEN0位为0时，即使在时间同步开始后连续发生超过指定次数的同步丢失，SYNCOUT标志也不设置为1，并且SYNTOUT标志立即设置为0。

SYNTOUT标志（同步消息接收超时检测标志）

SYNTOUT标志表示当STMR.ALEN1位为1时，在SYNTOR寄存器中指定的时间段内没有接收到同步消息。在时间同步开始后（当设置SYNSTARTR.STR位时，SYNTOUT标志立即设置为1到1)当EPTPC启动后没有收到Sync消息时。使用SYNTOUT标志时，在开始时间同步后立即将SYNTOUT标志设置为0。

W10D标志（最差10次采集完成标志）

W10D标志表示已完成最差10个值的采集。

30.2.6 STCA Status Notification Enable Register (STIPR)

Address(es): EPTPC.STIPR 4006 5044h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	W10D	SYNTOUT	—	SYNCOUT	SYNC
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	SYNC	SYNC Status Notification Enable	0: Disable notification of the STSR.SYNC state 1: Enable notification of the STSR.SYNC state.	R/W
b1	SYNCOUT	SYNCOUT Status Notification Enable	0: Disable notification of the STSR.SYNCOUT state 1: Enable notification of the STSR.SYNCOUT state.	R/W
b2	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b3	SYNTOUT	SYNTOUT Status Notification Enable	0: Disable notification of the STSR.SYNTOUT state 1: Enable notification of the STSR.SYNTOUT state.	R/W
b4	W10D	W10D Status Notification Enable	0: Disable notification of the STSR.W10D state 1: Enable notification of the STSR.W10D state.	R/W
b31 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The STIPR register specifies whether the MIESR.ST flag does or does not reflect changes in the state of the STCA module.

30.2.7 STCA Clock Frequency Setting Register (STCFR)

Address(es): EPTPC.STCFR 4006 5050h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	STCF[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	STCF[1:0]	STCA Clock Frequency	b1 b0 0 0: 20 MHz 0 1: 25 MHz 1 0: 50 MHz 1 1: 100 MHz.	R/W
b31 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Set this register before starting the EDMAC, ETHERC, or PTPEDMAC. Do not change the settings during operations.

The STCFR register specifies the frequency of the clock source for the STCA module (STCA clock). The setting in this register must be set to the same frequency as that selected in the STCSELR register.

30.2.6 STCA状态通知启用寄存器(STIPR)

Address(es): EPTPC.STIPR 4006 5044h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	W10D	SYNTOUT	—	SYNCOUT	SYNC
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	SYNC	同步状态通知 Enable	0：禁用STSR.SYNC状态通知1：启用STSR.SYNC状态通知。	R/W
b1	SYNCOUT	SYNCOUT状态通知 Enable	0：禁用STSR.SYNCOUT状态通知1：启用STSR.SYNCOUT状态通知。	R/W
b2	—	Reserved	该位读取为0。写入值应为0。	R/W
b3	SYNTOUT	SYNTOUT状态通知 Enable	0：禁用STSR.SYNTOUT状态通知1：启用STSR.SYNTOUT状态通知。	R/W
b4	W10D	W10D状态通知 Enable	0：禁用STSR.W10D状态通知1：启用STSR.W10D状态通知。	R/W
b31 to b5	—	Reserved	这些位被读取为0。写入值应为0。	R/W

STIPR寄存器指定MIESR.ST标志是否反映STCA模块状态的变化。

30.2.7 STCA时钟频率设置寄存器(STCFR)

Address(es): EPTPC.STCFR 4006 5050h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	STCF[1:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b1, b0	STCF[1:0]	STCA时钟频率	b1 b0 0 0: 20 MHz 0 1: 25 MHz 1 0: 50 MHz 1 1: 100 MHz.	R/W
b31 to b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note: 在启动EDMAC、ETHERC或PTPEDMAC之前设置该寄存器。请勿在操作期间更改设置。

STCFR寄存器指定STCA模块的时钟源频率（STCA时钟）。该寄存器中的设置必须设置为与STCSELR寄存器中选择的频率相同的频率。

STCF[1:0] bits (STCA Clock Frequency)

The STCF[1:0] bits select the frequency of the STCA clock. To enable synchronous control in compliance with IEEE 1588, the STCA clock frequency must be specified as 20, 25, 50, or 100 MHz. Operation is not guaranteed if the frequency selected in these bits differs from the clock frequency actually input to the STCA module.

30.2.8 STCA Operating Mode Register (STMR)

Address(es): EPTPC.STMR 4006 5054h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	ALEN1	ALEN0	—	—	—	—	DVTH[3:0]				SYTH[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	W10S	—	CMOD	—	—	—	—	—	WINT[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	WINT[7:0]	Worst 10 Acquisition Time	00h: Do not acquire the worst 10 values 01h: Sync message reception: 1 time : FFh: Sync message reception: 255 times.	R/W
b12 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b13	CMOD	Time Synchronization Correction Mode	0: Mode 1 1: Mode 2.	R/W
b14	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b15	W10S	Worst 10 Acquisition Control Select	0: Start measurement by hardware and use the value acquired in the PW10VR or MW10R register as the filtering limit 1: Start measurement using the GETW10R.GW10 bit and use the value set in the PLIMITR or MLIMITR register as the filtering limit.	R/W
b19 to b16	SYTH[3:0]	Synchronized State Detection Threshold Setting	0h: None *1 1h: 1 time : Fh: 15 times.	R/W
b23 to b20	DVTH[3:0]	Synchronization Loss Detection Threshold Setting	0h: None *2 1h: 1 time : Fh: 15 times.	R/W
b27 to b24	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b28	ALEN0	Alarm Detection Enable 0	0: Disable STSR.SYNC or SYNCOUT flag from setting to 1 on detection of synchronization or loss of synchronization 1: Enable STSR.SYNC or SYNCOUT flag to set to 1 on detection of synchronization or loss of synchronization.	R/W
b29	ALEN1	Alarm Detection Enable 1	0: Disable STSR.SYNTOUT flag from setting to 1 on detection of the Sync message reception timeout interrupt 1: Enable STSR.SYNTOUT flag to set to 1 on detection of the Sync message reception timeout interrupt.	R/W
b31, b30	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. The STSR.SYNC flag is not set to 1 regardless of the ALEN0 bit setting.
Note 2. The STSR.SYNCOUT flag is not set to 1 regardless of the ALEN0 bit setting.

The STMR register specifies the operating mode of the STCA module.

STCF[1:0]位（STCA时钟频率）

STCF[1:0]位选择STCA时钟的频率。要启用符合IEEE1588的同步控制，STCA时钟频率必须指定为20、25、50或100MHz。如果在这些位中选择的频率与实际输入到STCA模块的时钟频率不同，则无法保证操作。

30.2.8 STCA操作模式寄存器(STMR)

Address(es): EPTPC.STMR 4006 5054h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	ALEN1	ALEN0	—	—	—	—	DVTH[3:0]				SYTH[3:0]			
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	W10S	—	CMOD	—	—	—	—	—	WINT[7:0]							
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b7 to b0	WINT[7:0]	最差的10次采集时间	00h：不获取最差的10个值01h：同步消息接收：1次 ：FFh：同步信息接收：255次。	R/W
b12 to b8	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b13	CMOD	时间同步校正模式	0: Mode 1 1: Mode 2.	R/W
b14	—	Reserved	该位读取为0。写入值应为0。	R/W
b15	W10S	最差的10个采集控制Select	0：通过硬件开始测量，使用PW10VR或MW10R寄存器中获取的值作为过滤限值1：使用GETW10R.GW10位开始测量，使用PLIMITR或MLIMITR寄存器中设置的值作为过滤限值。	R/W
b19 to b16	SYTH[3:0]	同步状态检测阈值设置	0h：无*11h：1次 : Fh: 15 times.	R/W
b23 to b20	DVTH[3:0]	同步丢失检测阈值设置	0h：无*21h：1次 : Fh: 15 times.	R/W
b27 to b24	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b28	ALEN0	报警检测使能0	0：在检测到同步或同步丢失时禁用STSR.SYNC或SYNCOUT标志设置为11：在检测到同步或同步丢失时启用STSR.SYNC或SYNCOUT标志设置为1。	R/W
b29	ALEN1	报警检测使能1	0：在检测到同步消息接收超时中断时禁止STSR.SYNTOUT标志设置为11：在检测到同步消息接收超时中断时启用STSR.SYNTOUT标志设置为1。	R/W
b31, b30	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 无论ALEN0位设置如何，STSR.SYNC标志都不会设置为1。
Note 2. 无论ALEN0位设置如何，STSR.SYNCOUT标志都不会设置为1。

STMR寄存器指定STCA模块的工作模式。

WINT[7:0] bits (Worst 10 Acquisition Time)

The WINT[7:0] bits set the time for acquiring the worst 10 gradients (the number of times Sync messages are received). Renesas recommends setting the number of Sync message receptions to 32 or more in most cases.

CMOD bit (Time Synchronization Correction Mode)

Mode 1 or mode 2 can be selected in the CMOD bit to correct the local time information when the EPTPC operates as a slave clock. Select the appropriate mode for your system configuration. Table 30.7 provides a summary of the two correction modes.

Table 30.7 Correction mode features

Correction mode	Function	Features	Notes
Mode 1	Mode for correcting the counter every Sync message reception by using the current offsetFromMaster. Operation is in mode 1 after the start of correction, then shifts to the specified mode.	The time information of the master clock is set as the local time information at a specific time.	Synchronization is not guaranteed if calculating offsetFromMaster is not possible, for example if packets are temporarily being discarded because of a failure of communications.
Mode 2	In mode 2, the gradient value calculated from offsetFromMaster (worst-10 control) is retained and used in correcting the local time information so that it approximates the time information of the master clock.	Even when calculating offsetFromMaster is not possible, a certain level of synchronization can be guaranteed in this mode, because the counter is still corrected from the gradient information.	Establishing synchronization takes longer.

W10S bit (Worst 10 Acquisition Control Select)

The W10S bit selects the value used for measuring and filtering the worst 10 gradients. When this bit is set to 0, the values acquired in the PW10VRU, PW10VRM, and PW10VRL registers and the MW10RU, MW10RM, and MW10RL registers are used as the limit for the filter. When the bit is set to 1, the values set in the PLIMITRU, PLIMITRM, and PLIMITRL registers and the MLIMITRU, MLIMITRM, and MLIMITRL registers are used as the limit for the filter.

SYTH[3:0] bits (Synchronized State Detection Threshold Setting)

The SYTH[3:0] bits specify the number of consecutive times that a value should fall within the thresholds set in registers SYNTDBRU and SYNTDBRL, to be considered as a synchronized state. When the ALEN0 bit is 1, the STSR.SYNCOUT flag becomes 1.

DVTH[3:0] bits (Synchronization Loss Detection Threshold Setting)

The DVTH[3:0] bits specify a value for the number of consecutive times the offsetFromMaster value must exceed the specified thresholds for the STCA module to detect loss of synchronization. The thresholds are specified in the SYNTDARU and SYNTDARL registers. When the ALEN0 bit is 1, the STSR.SYNCOUT flag is set to 1 on loss of synchronization detection.

ALEN0 bit (Alarm Detection Enable 0)

When the ALEN0 bit is 1, the STSR.SYNC or SYNCOUT flag is set to 1 on detection of synchronization or loss of synchronization. When this bit is 0, the SYNC or SYNCOUT flag is not set to 1 even if synchronization or loss of synchronization is detected.

ALEN1 bit (Alarm Detection Enable 1)

When the ALEN1 bit is 1, the STSR.SYNTOUT flag is set to 1 if a Sync message is not received within the time specified in the SYNTOR register. When this bit is 0, the SYNTOUT flag is not set to 1 even if a reception timeout occurs.

WINT[7:0]位（最差10次采集时间）

WINT[7:0]位设置获取最差10个梯度的时间（接收同步消息的次数）。
Renesas建议在大多数情况下将同步消息接收数设置为32或更多。

CMOD位（时间同步校正模式）

当EPTPC作为从时钟运行时，可以在CMOD位中选择模式1或模式2来校正本地时间信息。为您的系统配置选择适当的模式。表30.7总结了两种校正模式。

Table 30.7 校正模式功能

校正模式	Function	Features	Notes
Mode 1	通过使用当前的offsetFromMaster来纠正每次接收Sync消息的计数器的模式。校正开始后运行在模式1，然后切换到指定模式。	主时钟的时间信息被设置为特定时间的本地时间信息。	如果无法计算offsetFromMaster，则无法保证同步，例如，如果由于通信失败而暂时丢弃数据包。
Mode 2	在模式2中，从offsetFromMaster（worst-10控制）计算的梯度值被保留并用于校正本地时间信息，使其接近主时钟的时间信息。	即使在无法计算offsetFromMaster的情况下，在这种模式下也可以保证一定程度的同步，因为计数器仍然根据梯度信息进行校正。	建立同步需要更长的时间。

W10S位（最差10采集控制选择）

W10S位选择用于测量和过滤最差10个梯度的值。当该位设置为0时，在PW10VRU、PW10VRM和PW10VRL寄存器以及MW10RU、MW10RM和MW10RL寄存器中获取的值用作滤波器的限值。当该位设置为1时，在PLIMITRU、PLIMITRM和PLIMITRL寄存器以及MLIMITRU、MLIMITRM和MLIMITRL寄存器中设置的值用作过滤器的限制。

SYTH[3:0]位（同步状态检测阈值设置）

SYTH[3:0]位指定值应落在寄存器中设置的阈值内的连续次数
SYNTDBRU和SYNTDBRL，被视为同步状态。当ALEN0位为1时，
STSR.SYNCOUT标志变为1。

DVTH[3:0]位（同步丢失检测阈值设置）

DVTH[3:0]位指定offsetFromMaster值必须超过STCA模块检测同步丢失的指定阈值的连续次数的值。阈值在SYNTDARU和SYNTDARL寄存器中指定。当ALEN0位为1时，STSR.SYNCOUT标志在同步丢失检测时设置为1。

ALEN0位（报警检测使能0）

当ALEN0位为1时，STSR.SYNC或SYNCOUT标志在检测到同步或同步丢失时设置为1。当该位为0时，即使检测到同步或同步丢失，SYNC或SYNCOUT标志也不会设置为1。

ALEN1位（报警检测使能1）

当ALEN1位为1时，如果在SYNTOR寄存器中指定的时间内未接收到同步消息，则STSR.SYNTOUT标志设置为1。当该位为0时，即使发生接收超时，SYNTOUT标志也不会设置为1。

30.2.9 Sync Message Reception Timeout Register (SYNTOR)

Address(es): EPTPC.SYNTOR 4006 5058h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b31 to b0	—	—	If no Sync message is received within 1024 × n (ns), where n is the SYNTOR setting, a timeout for reception of Sync messages occurs, and the STSR.SYNTOUT flag is set to 1.	R/W

The SYNTOR register specifies the timeout period for reception of Sync messages. The timeout period is 1024 times the SYNTOR setting, in nanoseconds. If no Sync message is received within the period specified in these bits, a timeout is detected. When the SYNTOR register is 0, the STSR.SYNTOUT flag is not set to 1.

30.2.10 ETHER_IPLS Interrupt Request Timer Select Register (IPTSELR)

Address(es): EPTPC.IPTSELR 4006 5060h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	IPTSEL5	IPTSEL4	IPTSEL3	IPTSEL2	IPTSEL1	IPTSEL0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	IPTSEL0	Pulse Output Timer 0 Select	0: Pulse output timer 0 not selected as a source for ETHER_IPLS interrupt requests 1: Pulse output timer 0 selected as a source for ETHER_IPLS interrupt requests.	R/W
b1	IPTSEL1	Pulse Output Timer 1 Select	0: Pulse output timer 1 not selected as a source for ETHER_IPLS interrupt requests 1: Pulse output timer 1 selected as a source for ETHER_IPLS interrupt requests.	R/W
b2	IPTSEL2	Pulse Output Timer 2 Select	0: Pulse output timer 2 not selected as a source for ETHER_IPLS interrupt requests 1: Pulse output timer 2 selected as a source for ETHER_IPLS interrupt requests.	R/W
b3	IPTSEL3	Pulse Output Timer 3 Select	0: Pulse output timer 3 not selected as a source for ETHER_IPLS interrupt requests 1: Pulse output timer 3 selected as a source for ETHER_IPLS interrupt requests.	R/W
b4	IPTSEL4	Pulse Output Timer 4 Select	0: Pulse output timer 4 not selected as a source for ETHER_IPLS interrupt requests 1: Pulse output timer 4 selected as a source for ETHER_IPLS interrupt requests.	R/W

30.2.9 同步消息接收超时寄存器(SYNTOR)

Address(es): EPTPC.SYNTOR 4006 5058h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b31 to b0	—	—	如果在1024×n(ns)内没有接收到Sync消息，其中n是SYNTOR设置，则接收Sync消息会发生超时，并且STSR.SYNTOUT标志设置为1。	R/W

SYNTOR寄存器指定接收同步消息的超时时间。超时时间是SYNTOR设置的1024倍，以纳秒为单位。如果在这些位指定的时间段内没有收到同步消息，则检测到超时。当SYNTOR寄存器为0时，STSR.SYNTOUT标志不设置为1。

30.2.10 ETHER_IPLS中断请求定时器选择寄存器(IPTSELR)

Address(es): EPTPC.IPTSELR 4006 5060h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	IPTSEL5	IPTSEL4	IPTSEL3	IPTSEL2	IPTSEL1	IPTSEL0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	IPTSEL0	脉冲输出定时器0选择	0：未选择脉冲输出定时器0作为ETHER_IPLS中断请求的源1：选择脉冲输出定时器0作为ETHER_IPLS中断请求的源。	R/W
b1	IPTSEL1	脉冲输出定时器1选择	0：未选择脉冲输出定时器1作为ETHER_IPLS中断请求的源1：选择脉冲输出定时器1作为ETHER_IPLS中断请求的源。	R/W
b2	IPTSEL2	脉冲输出定时器2选择	0：未选择脉冲输出定时器2作为ETHER_IPLS中断请求的源1：选择脉冲输出定时器2作为ETHER_IPLS中断请求的源。	R/W
b3	IPTSEL3	脉冲输出定时器3选择	0：未选择脉冲输出定时器3作为ETHER_IPLS中断请求的源1：选择脉冲输出定时器3作为ETHER_IPLS中断请求的源。	R/W
b4	IPTSEL4	脉冲输出定时器4选择	0：未选择脉冲输出定时器4作为ETHER_IPLS中断请求的源1：选择脉冲输出定时器4作为ETHER_IPLS中断请求的源。	R/W

Bit	Symbol	Bit name	Description	R/W
b5	IPTSEL5	Pulse Output Timer 5 Select	0: Pulse output timer 5 not selected as a source for ETHER_IPLS interrupt requests 1: Pulse output timer 5 selected as a source for ETHER_IPLS interrupt requests.	R/W
b31 to b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The IPTSELR register selects the pulse output timers that generate ETHER_IPLS interrupt requests. Each pulse output timer m (m = 0 to 5) takes the clock signal from the STCA as its clock source and produces pulses with a specified period and duty cycle. An ETHER_IPLS interrupt is requested on rising edges if the ELIPPR.PLSP bit is set to 1 and on falling edges if the PLSN bit in the same register is set to 1. When multiple channels are selected in this register, the interrupt request signal becomes the logical OR of the interrupt requests from the selected channels. For more on the ETHER_IPLS interrupt, see section 30.4, Interrupts.

30.2.11 ETHER_MINT Interrupt Request Timer Select Register (MITSELR)

Address(es): EPTPC.MITSELR 4006 5064h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	MINTEN5	MINTEN4	MINTEN3	MINTEN2	MINTEN1	MINTEN0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	MINTEN0	Pulse Output Timer 0 ETHER_MINT Interrupt Output Enable	0: Do not reflect rising edges of pulse output timer 0 on MIESR.CYC0 flag as ETHER_MINT interrupt source 1: Reflect rising edges of pulse output timer 0 on MIESR.CYC0 flag as ETHER_MINT interrupt source.	R/W
b1	MINTEN1	Pulse Output Timer 1 ETHER_MINT Interrupt Output Enable	0: Do not reflect rising edges of pulse output timer 1 on MIESR.CYC1 flag as ETHER_MINT interrupt source 1: Reflect rising edges of pulse output timer 1 on MIESR.CYC1 flag as ETHER_MINT interrupt source.	R/W
b2	MINTEN2	Pulse Output Timer 2 ETHER_MINT Interrupt Output Enable	0: Do not reflect rising edges of pulse output timer 2 on MIESR.CYC2 flag as ETHER_MINT interrupt source 1: Reflect rising edges of pulse output timer 2 on MIESR.CYC2 flag as ETHER_MINT interrupt source.	R/W
b3	MINTEN3	Pulse Output Timer 3 ETHER_MINT Interrupt Output Enable	0: Do not reflect rising edges of pulse output timer 3 on MIESR.CYC3 flag as ETHER_MINT interrupt source 1: Reflect rising edges of pulse output timer 3 on MIESR.CYC3 flag as ETHER_MINT interrupt source.	R/W
b4	MINTEN4	Pulse Output Timer 4 ETHER_MINT Interrupt Output Enable	0: Do not reflect rising edges of pulse output timer 4 on MIESR.CYC4 flag as ETHER_MINT interrupt source 1: Reflect rising edges of pulse output timer 4 on MIESR.CYC4 flag as ETHER_MINT interrupt source.	R/W
b5	MINTEN5	Pulse Output Timer 5 ETHER_MINT Interrupt Output Enable	0: Do not reflect rising edges of pulse output timer 5 on MIESR.CYC5 flag as ETHER_MINT interrupt source 1: Reflect rising edges of pulse output timer 5 on MIESR.CYC5 flag as ETHER_MINT interrupt source.	R/W
b31 to b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The MITSELR register selects pulse output timers that generate ETHER_MINT interrupt requests. Each pulse output timer m (m = 0 to 5) takes the clock signal from the STCA as its clock source and produces pulses with a specified period and duty cycle. An ETHER_MINT interrupt is requested on rising edges of the pulse signal from the associated pulse output timer m if the setting of the MIEIPR.CYCm bit is 1. For more on the ETHER_MINT interrupt, see section 30.4,

Bit	Symbol	位名称	Description	R/W
b5	IPTSEL5	脉冲输出定时器5选择	0：未选择脉冲输出定时器5作为ETHER_IPLS中断请求的源1：选择脉冲输出定时器5作为ETHER_IPLS中断请求的源。	R/W
b31 to b6	—	Reserved	这些位被读取为0。写入值应为0。	R/W

IPTSELR寄存器选择产生ETHER_IPLS中断请求的脉冲输出定时器。每个脉冲输出定时器m（m=0到5）以来自STCA的时钟信号作为其时钟源，并产生具有指定周期和占空比的脉冲。如果ELIPPR.PLSP位设置为1，则在上升沿请求ETHER_IPLS中断；如果同一寄存器中的PLSN位设置为1，则在下降沿请求ETHER_IPLS中断。当在该寄存器中选择多个通道时，中断请求信号变为来自所选通道的中断请求的逻辑或。有关ETHER_IPLS中断的更多信息，请参阅第30.4节，中断。

30.2.11 ETHER_MINT中断请求定时器选择寄存器(MITSELR)

Address(es): EPTPC.MITSELR 4006 5064h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	MINTEN5	MINTEN4	MINTEN3	MINTEN2	MINTEN1	MINTEN0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	MINTEN0	脉冲输出定时器0 ETHER_MINT Interrupt 输出使能	0：不将MIESR.CYC0标志上的脉冲输出定时器0的上升沿反映为ETHER_MINT中断源1：将MIESR.CYC0标志上的脉冲输出定时器0的上升沿反映为ETHER_MINT中断源。	R/W
b1	MINTEN1	脉冲输出定时器1 ETHER_MINT Interrupt 输出使能	0：不将MIESR.CYC1标志上的脉冲输出定时器1的上升沿反映为ETHER_MINT中断源1：将MIESR.CYC1标志上的脉冲输出定时器1的上升沿反映为ETHER_MINT中断源。	R/W
b2	MINTEN2	脉冲输出定时器2 ETHER_MINT Interrupt 输出使能	0：不将MIESR.CYC2标志上的脉冲输出定时器2的上升沿反映为ETHER_MINT中断源1：将MIESR.CYC2标志上的脉冲输出定时器2的上升沿反映为ETHER_MINT中断源。	R/W
b3	MINTEN3	脉冲输出定时器3 ETHER_MINT Interrupt 输出使能	0：不将脉冲输出定时器3的上升沿反映在MIESR.CYC3标志上作为ETHER_MINT中断源1：将脉冲输出定时器3的上升沿反映在MIESR.CYC3标志上作为ETHER_MINT中断源。	R/W
b4	MINTEN4	脉冲输出定时器4 ETHER_MINT Interrupt 输出使能	0：不将MIESR.CYC4标志上的脉冲输出定时器4的上升沿反映为ETHER_MINT中断源1：将MIESR.CYC4标志上的脉冲输出定时器4的上升沿反映为ETHER_MINT中断源。	R/W
b5	MINTEN5	脉冲输出定时器5 ETHER_MINT Interrupt 输出使能	0：不将脉冲输出定时器5的上升沿反映在MIESR.CYC5标志上作为ETHER_MINT中断源1：将脉冲输出定时器5的上升沿反映在MIESR.CYC5标志上作为ETHER_MINT中断源。	R/W
b31 to b6	—	Reserved	这些位被读取为0。写入值应为0。	R/W

MITSELR寄存器选择产生ETHER_MINT中断请求的脉冲输出定时器。每个脉冲输出定时器m（m=0到5）以来自STCA的时钟信号作为其时钟源，并产生具有指定周期和占空比的脉冲。如果MIEIPR.CYCm位设置为1，则在来自相关脉冲输出定时器m的脉冲信号的上升沿请求ETHER_MINT中断。有关ETHER_MINT中断的更多信息，请参见第30.4节，

Interrupts.

30.2.12 ELC Output Timer Select Register (ELTSELR)

Address(es): EPTPC.ELTSELR 4006 5068h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	ELTDIS5	ELTDIS4	ELTDIS3	ELTDIS2	ELTDIS1	ELTDIS0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	ELTDIS0	Pulse Output Timer 0 Event Generation Disable	0: Use pulse output timer 0 for generating event signals for the ELC 1: Do not use pulse output timer 0 for generating event signals for the ELC.	R/W
b1	ELTDIS1	Pulse Output Timer 1 Event Generation Disable	0: Use pulse output timer 1 for generating event signals for the ELC 1: Do not use pulse output timer 1 for generating event signals for the ELC.	R/W
b2	ELTDIS2	Pulse Output Timer 2 Event Generation Disable	0: Use pulse output timer 2 for generating event signals for the ELC 1: Do not use pulse output timer 2 for generating event signals for the ELC.	R/W
b3	ELTDIS3	Pulse Output Timer 3 Event Generation Disable	0: Use pulse output timer 3 for generating event signals for the ELC 1: Do not use pulse output timer 3 for generating event signals for the ELC.	R/W
b4	ELTDIS4	Pulse Output Timer 4 Event Generation Disable	0: Use pulse output timer 4 for generating event signals for the ELC 1: Do not use pulse output timer 4 for generating event signals for the ELC.	R/W
b5	ELTDIS5	Pulse Output Timer 5 Event Generation Disable	0: Use pulse output timer 5 for generating event signals for the ELC 1: Do not use pulse output timer 5 for generating event signals for the ELC.	R/W
b31 to b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The ELTSELR register selects the pulse output timers that output event signals to the ELC. Each pulse output timer m (m = 0 to 5) takes the clock signal from the STCA as its clock source and produces pulses with a specified period and duty cycle. An event signal is output to the ELC on rising edges if the ELIPPR.CYCPm bit is set to 1 and on falling edges if the CYCNm bit in the same register is set to 1. For more on output of event signals to the ELC, see section 30.4, Interrupts.

Interrupts.

30.2.12 ELC输出定时器选择寄存器(ELTSELR)

Address(es): EPTPC.ELTSELR 4006 5068h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	ELTDIS5	ELTDIS4	ELTDIS3	ELTDIS2	ELTDIS1	ELTDIS0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	ELTDIS0	脉冲输出定时器0事件代禁用	0：使用脉冲输出定时器0为ELC生成事件信号1：不要使用脉冲输出定时器0为ELC生成事件信号。	R/W
b1	ELTDIS1	脉冲输出定时器1事件代禁用	0：使用脉冲输出定时器1为ELC生成事件信号1：不要使用脉冲输出定时器1为ELC生成事件信号。	R/W
b2	ELTDIS2	脉冲输出定时器2事件代禁用	0：使用脉冲输出定时器2为ELC生成事件信号1：不要使用脉冲输出定时器2为ELC生成事件信号。	R/W
b3	ELTDIS3	脉冲输出定时器3事件代禁用	0：使用脉冲输出定时器3为ELC生成事件信号1：不要使用脉冲输出定时器3为ELC生成事件信号。	R/W
b4	ELTDIS4	脉冲输出定时器4事件代禁用	0：使用脉冲输出定时器4为ELC生成事件信号1：不要使用脉冲输出定时器4为ELC生成事件信号。	R/W
b5	ELTDIS5	脉冲输出定时器5事件代禁用	0：使用脉冲输出定时器5为ELC生成事件信号1：不要使用脉冲输出定时器5为ELC生成事件信号。	R/W
b31 to b6	—	Reserved	这些位被读取为0。写入值应为0。	R/W

ELTSELR寄存器选择向ELC输出事件信号的脉冲输出定时器。每个脉冲输出定时器m（m=0到5）以来自STCA的时钟信号作为其时钟源，并产生具有指定周期和占空比的脉冲。如果ELIPPR.CYCPm位设置为1，则在上升沿向ELC输出事件信号；如果同一寄存器中的CYCNm位设置为1，则在下降沿向ELC输出事件信号。有关向ELC输出事件信号的更多信息，请参阅第30.4节，中断。

30.2.13 Time Synchronization Channel Select Register (STCHSELR)

Address(es): EPTPC.STCHSELR 4006 506Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SYSEL
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	SYSEL	Timer Information Input Select	0: Use time information from the SYNFP0 module 1: Setting prohibited.	R/W
b31 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The STCHSELR register selects the time information input to the STCA module.

30.2.14 Slave Time Synchronization Start Register (SYNSTARTR)

Address(es): EPTPC.SYNSTARTR 4006 5080h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	STR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	STR	Slave Time Synchronization Control	0: Stop slave time synchronization 1: Start slave time synchronization.	R/W
b31 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The SYNSTARTR register starts or stops time synchronization. This register is used when the EPTPC is operating as a slave node.

30.2.13 时间同步通道选择寄存器(STCHSELR)

Address(es): EPTPC.STCHSELR 4006 506Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SYSEL
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	SYSEL	定时器信息输入选择	0：使用来自SYNFP0模块的时间信息1：禁止设置。	R/W
b31 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

STCHSELR寄存器选择输入到STCA模块的时间信息。

30.2.14 从机时间同步启动寄存器(SYNSTARTR)

Address(es): EPTPC.SYNSTARTR 4006 5080h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	STR
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	STR	从机时间同步 Control	0：停止从机对时1：启动从机对时。	R/W
b31 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

SYNSTARTR寄存器启动或停止时间同步。该寄存器在EPTPC作为从节点运行时使用。

30.2.15 Local Clock Counter Initial Value Load Directive Register (LCIVLDR)

Address(es): EPTPC.LCIVLDR 4006 5084h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	LOAD
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	LOAD	Local Clock Counter Initial Value Load Directive	0: Do not load initial value to the local clock counter 1: Load initial value to the local clock counter.	W*1
b31 to b1	—	Reserved	The write value should be 0.	W

Note 1. Do not change the value of this bit while the SYNSTARTR.STR bit is 1.

The LCIVLDR register specifies the value in the LCIVRU, LCIVRM, and LCIVRL registers as the initial value of the local clock counter.

30.2.16 Synchronization Loss Detection Threshold Register (SYNTDARU, SYNTDARL)

Address(es): EPTPC.SYNTDARU 4006 5090h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b31 to b0	—	—	These bits specify the upper-order 32 bits of the threshold for detection of loss of synchronization.	R/W

Address(es): EPTPC.SYNTDARL 4006 5094h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

30.2.15 本地时钟计数器初始值加载指令寄存器(LCIVLDR)

Address(es): EPTPC.LCIVLDR 4006 5084h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	LOAD
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	LOAD	本地时钟计数器初始值 价值加载指令	0：不加载初始值到本地时钟计数器1：加载初始值 到本地时钟计数器。	W*1
b31 to b1	—	Reserved	写入值应为0。	W

Note 1. 当SYNSTARTR.STR位为1时不要更改该位的值。

LCIVLDR寄存器指定LCIVRU、LCIVRM和LCIVRL寄存器中的值作为本地时钟计数器的初始值。

30.2.16 同步丢失检测阈值寄存器(SYNTDARU SYNTDARL)

Address(es): EPTPC.SYNTDARU 4006 5090h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b31 to b0	—	—	这些位指定用于检测同步丢失的阈值的高位32位。	R/W

Address(es): EPTPC.SYNTDARL 4006 5094h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b31 to b0	—	—	These bits specify the lower-order 32 bits of the threshold for detection of loss of synchronization.	R/W

The SYNTDARU and SYNTDARL registers specify the threshold value for offsetFromMaster to be used in determining loss of synchronization. When setting a threshold value, write the upper-order 32 bits to SYNTDARU and the lower-order 32 bits to SYNTDARL, in that order and in consecutive operations. If the offsetFromMaster value exceeds the value specified in SYNTDARU and SYNTDARL, a loss of synchronization is detected. Set the value in SYNTDARU and SYNTDARL in nanoseconds. SYNTDARU and SYNTDARL are not used when the device is operating as a master clock.

30.2.17 Synchronization Detection Threshold Register (SYNTDBRU, SYNTDBRL)

Address(es): EPTPC.SYNTDBRU 4006 5098h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b31 to b0	—	—	These bits specify the upper-order 32 bits of the threshold for detection of synchronization.	R/W

Address(es): EPTPC.SYNTDBRL 4006 509Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b31 to b0	—	—	These bits specify the lower-order 32 bits of the threshold for detection of synchronization.	R/W

The SYNTDBRU and SYNTDBRL registers specify the threshold value for offsetFromMaster to be used in determining synchronization. When setting a threshold value, write the upper-order 32 bits to SYNTDBRU and the lower-order 32 bits to SYNTDBRL, in that order and in consecutive operations. If the offsetFromMaster value is less than the value specified in SYNTDBRU and SYNTDBRL, synchronization is detected. Set the value in SYNTDBRU and SYNTDBRL in nanoseconds. SYNTDBRU and SYNTDBRL are not used when the device is operating as a master clock.

Bit	Symbol	位名称	Description	R/W
b31 to b0	—	—	这些位指定用于检测同步丢失的阈值的低32位。	R/W

SYNTDARU和SYNTDARL寄存器指定offsetFromMaster的阈值，用于确定同步丢失。设置阈值时，将高位32位写入SYNTDARU，将低位32位写入SYNTDARL，按顺序和连续操作。如果offsetFromMaster值超过SYNTDARU和SYNTDARL中指定的值，则检测到同步丢失。以纳秒为单位设置SYNTDARU和SYNTDARL中的值。当器件作为主时钟运行时，不使用SYNTDARU和SYNTDARL。

30.2.17 同步检测阈值寄存器(SYNTDBRU SYNTDBRL)

Address(es): EPTPC.SYNTDBRU 4006 5098h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b31 to b0	—	—	这些位指定用于检测同步的阈值的高位32位。	R/W

Address(es): EPTPC.SYNTDBRL 4006 509Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b31 to b0	—	—	这些位指定用于检测同步的阈值的低32位。	R/W

SYNTDBRU和SYNTDBRL寄存器指定用于确定同步的offsetFromMaster的阈值。设置阈值时，将高位32位写入SYNTDBRU，将低位32位写入SYNTDBRL，顺序和连续操作。如果offsetFromMaster值小于SYNTDBRU和SYNTDBRL中指定的值，则检测到同步。以纳秒为单位设置SYNTDBRU和SYNTDBRL中的值。当设备作为主时钟运行时，不使用SYNTDBRU和SYNTDBRL。

30.2.18 Local Clock Counter Initial Value Register (LCIVRU, LCIVRM, LCIVRL)

Address(es): EPTPC.LCIVRU 4006 50B0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b15 to b0	—	—	These bits specify the upper-order 16 bits of the integer portion of the initial value for the local clock counter.	R/W
b31 to b16	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Address(es): EPTPC.LCIVRM 4006 50B4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b31 to b0	—	—	These bits specify the lower-order 32 bits of the integer portion of the initial value for the clock counter.	R/W

Address(es): EPTPC.LCIVRL 4006 50B8h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b31 to b0	—	—	These bits specify the fractional portion of the initial value of the clock counter in nanoseconds.	R/W

30.2.18 本地时钟计数器初始值寄存器(LCIVRU LCIVRM LCIVRL)

Address(es): EPTPC.LCIVRU 4006 50B0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b15 to b0	—	—	这些位指定本地时钟计数器初始值整数部分的高16位。	R/W
b31 to b16	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Address(es): EPTPC.LCIVRM 4006 50B4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b31 to b0	—	—	这些位指定时钟计数器初始值整数部分的低32位。	R/W

Address(es): EPTPC.LCIVRL 4006 50B8h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b31 to b0	—	—	这些位指定时钟计数器初始值的小数部分（以纳秒为单位）。	R/W

The LCIVRU, LCIVRM, and LCIVRL registers specify the initial value in seconds of the clock counter. When setting an initial value, write the upper-order 16 bits of the integer portion to LCIVRU, the lower-order 32 bits of the integer portion to LCIVRM, and the fractional portion in nanoseconds to LCIVRL, in that order and in consecutive operations.

The value in these registers can be used as the initial value of the local clock counter. When setting these register values in the local clock counter, set the LCIVLDR.LOAD bit to 1.

(1) Example

When 2.000000025 (s) is set as the initial value, write the following values to the registers:

- LCIVRU: 0000_0000h
- LCIVRM: 0000_0002h
- LCIVRL: 0000_0019h.

30.2.19 Worst 10 Acquisition Directive Register (GETW10R)

Address(es): EPTPC.GETW10R 4006 5124h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	GW10
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	GW10	Worst 10 Acquisition Directive	0: Do not acquire the worst 10 values 1: Start acquiring the worst 10 values.	R/W*1
b31 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Do not set this bit to 1 while the STMR.W10S bit is 0.

Software uses the GETW10R register to start calculation of gradient values for use in selecting the worst 10 values. A gradient value is the amount by which the timer counter of a slave is incremented when a given interval elapses. Setting the GW10 bit to 1 while the value of the STMR.W10S bit is 1 selects calculation of a gradient value by the EPTPC each time it receives a Sync message. Gradient values are calculated the number of times specified in the STMR.WINT[7:0] bits. The GW10 bit clears to 0 on completion of this number of calculations. The GETW10R register is not used when the device is operating as a master clock.

LCIVRU、LCIVRM和LCIVRL寄存器指定时钟计数器的初始值（以秒为单位）。设置初始值时，将整数部分的高16位写入LCIVRU，将整数部分的低32位写入LCIVRM，将小数部分（以纳秒为单位）写入LCIVRL，按此顺序和连续操作。

这些寄存器中的值可以作为本地时钟计数器的初始值。在本地时钟计数器中设置这些寄存器值时，将LCIVLDR.LOAD位设置为1。

(1) Example

当2.000000025(s)设置为初始值时，将以下值写入寄存器：

- LCIVRU: 0000_0000h
- LCIVRM: 0000_0002h
- LCIVRL: 0000_0019h.

30.2.19 最差10采集指令寄存器(GETW10R)

Address(es): EPTPC.GETW10R 4006 5124h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	GW10
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	GW10	最差10项采购指令	0：不获取最差的10个值1：开始获取最差的10个值。	R/W*1
b31 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 当STMR.W10S位为0时，请勿将此位设置为1。

软件使用GETW10R寄存器开始计算梯度值，用于选择最差的10个值。梯度值是在给定时间间隔过去时从站的计时器计数器增加的量。将GW10位设置为1，而STMR.W10S位的值为1，选择EPTPC每次接收同步消息时计算梯度值。梯度值按STMR.WINT[7:0]位中指定的次数计算。完成此次数的计算后，GW10位清除为0。当器件作为主时钟运行时，不使用GETW10R寄存器。

30.2.20 Positive Gradient Limit Register (PLIMITRU, PLIMITRM, PLIMITRL)

Address(es): EPTPC.PLIMITRU 4006 5128h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b30 to b0	—	—	These bits specify the upper-order 31 bits of the limit for the positive gradient.	R/W
b31	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Address(es): EPTPC.PLIMITRM 4006 512Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b31 to b0	—	—	These bits specify the middle-order 32 bits of the limit for the positive gradient.	R/W

Address(es): EPTPC.PLIMITRL 4006 5130h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b31 to b0	—	—	These bits specify the lower-order 32 bits of the limit for the positive gradient.	R/W

30.2.20 正梯度限制寄存器(PLIMITRU PLIMITRM PLIMITRL)

Address(es): EPTPC.PLIMITRU 4006 5128h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b30 to b0	—	—	这些位指定正梯度限制的高31位。	R/W
b31	—	Reserved	该位读取为0。写入值应为0。	R/W

Address(es): EPTPC.PLIMITRM 4006 512Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b31 to b0	—	—	这些位指定正梯度限制的中间32位。	R/W

Address(es): EPTPC.PLIMITRL 4006 5130h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b31 to b0	—	—	这些位指定正梯度限制的低32位。	R/W

The PLIMITRU, PLIMITRM, and PLIMITRL registers specify an upper limit on the gradient (= positive gradient) used in time synchronization. When setting the upper limit, write to the registers consecutively in the order of PLIMITRU, PLIMITRM, PLIMITRL. Gradients that exceed the value specified in these registers are not used in time synchronization. These registers are not used when the device is operating as a master clock. The registers are valid while the STMR.CMOD and W10S bits are 1.

Use the following expression to calculate the gradient value to be set in the registers:

PLIMITRU, PLIMITRM, and PLIMITRL register values = A (s)/T (s) × 2^{32}

A: Time (s) by which the slave local clock counter advances during the interval between received Sync messages

T: Actual time (s) between received Sync messages

For example, if the interval between Sync messages is 0.5 seconds and the local clock counter advances by 0.7 seconds during that time, and this is to be set as the limit, then the setting for PLIMITR = 0.7/0.5 × 2^{32} = 6 012 954 214 = 1 6666 6666h, and the settings for the individual registers are as follows:

- PLIMITRU = 0000_0000h
- PLIMITRM = 0000_0001h
- PLIMITRL = 6666_6666h.

The minimum setting depends on the STCA clock frequency as the clock source for counting by the local clock counter. For example, if the STCA clock frequency is 50 MHz, then the minimum allowable setting for PLIMITRU, PLIMITRM, and PLIMITRL = (1/50 (MHz)) (s)/0.5 (s) × 2^{32} = 172 = ACh, and the settings for the individual registers are as follows:

- PLIMITRU = 0000_0000h
- PLIMITRM = 0000_0000h
- PLIMITRL = 0000_00ACh.

The gradient limit values to be set are valid when time synchronization correction mode is mode 2 (STMR.CMOD is 1) and the gradient is controlled by software (STMR.W10S is 1).

30.2.21 Negative Gradient Limit Register (MLIMITRU, MLIMITRM, MLIMITRL)

Address(es): EPTPC.MLIMITRU 4006 5134h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b30 to b0	—	—	These bits specify the upper-order 31 bits of the limit for the negative gradient.	R/W
b31	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

PLIMITRU、PLIMITRM和PLIMITRL寄存器指定时间同步中使用的梯度（=正梯度）的上限。设置上限时，按PLIMITRU、PLIMITRM、PLIMITRL的顺序连续写入寄存器。超过这些寄存器中指定值的梯度不用于时间同步。当器件作为主时钟运行时，不使用这些寄存器。当STMR.CMOD和W10S位为1时，寄存器有效。

使用以下表达式计算要在寄存器中设置的梯度值：

PLIMITRU、PLIMITRM和PLIMITRL寄存器值=A(s)T(s)×232

A：从本地时钟计数器在接收到的同步消息之间的间隔内前进的时间（秒）

T：接收到的同步消息之间的实际时间（秒）

例如，如果Sync消息之间的间隔为0.5秒，并且在此期间本地时钟计数器提前0.7秒，并且将其设置为限制，则设置PLIMITR=0.70.5×232=6012954214=166666666h，各个寄存器的设置如下：

- PLIMITRU = 0000_0000h
- PLIMITRM = 0000_0001h
- PLIMITRL = 6666_6666h.

最小设置取决于作为本地时钟计数器计数的时钟源的STCA时钟频率。例如，如果STCA时钟频率为50MHz，则PLIMITRU、PLIMITRM和PLIMITRL的最小允许设置=(150(MHz))(s)0.5(s)×232=172=ACh，并且设置个人登记册如下：

- PLIMITRU = 0000_0000h
- PLIMITRM = 0000_0000h
- PLIMITRL = 0000_00ACh.

当时间同步校正模式为模式2（STMR.CMOD为1）且梯度由软件控制（STMR.W10S为1）时，要设置的梯度限制值有效。

30.2.21 负梯度限制寄存器(MLIMITRU MLIMITRM MLIMITRL)

Address(es): EPTPC.MLIMITRU 4006 5134h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b30 to b0	—	—	这些位指定负梯度限制的高31位。	R/W
b31	—	Reserved	该位读取为0。写入值应为0。	R/W

Address(es): EPTPC.MLIMITRM 4006 5138h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b31 to b0	—	—	These bits specify the middle-order 32 bits of the limit for the negative gradient.	R/W

Address(es): EPTPC.MLIMITRL 4006 513Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b31 to b0	—	—	These bits specify the lower-order 32 bits of the limit for the negative gradient.	R/W

The MLIMITRU, MLIMITRM, and MLIMITRL registers specify a lower limit on the gradient (= negative gradient) used in time synchronization. Use a two's complement value to set the lower limit. When setting the lower limit, write to the registers consecutively in the order of MLIMITRU, MLIMITRM, MLIMITRL. Gradients that are less than the value specified in these registers are not used in time synchronization. These registers are not used when the device is operating as a master clock. The registers are valid while the STMR.CMOD and W10S bits are 1.

The procedure for setting the value, and the minimum value that can be set, are the same as for the PLIMITRU, PLIMITRM, and PLIMITRL registers.

Address(es): EPTPC.MLIMITRM 4006 5138h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b31 to b0	—	—	这些位指定负梯度限制的中间32位。	R/W

Address(es): EPTPC.MLIMITRL 4006 513Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b31 to b0	—	—	这些位指定负梯度限制的低32位。	R/W

MLIMITRU、MLIMITRM和MLIMITRL寄存器指定时间同步中使用的梯度（=负梯度）的下限。使用二进制补码值设置下限。设置下限时，按MLIMITRU、MLIMITRM、MLIMITRL的顺序连续写入寄存器。小于这些寄存器中指定值的梯度不用于时间同步。当器件作为主时钟运行时，不使用这些寄存器。当STMR.CMOD和W10S位为1时，寄存器有效。

设置值的过程，以及可以设置的最小值，与PLIMITRU相同，
PLIMITRM和PLIMITRL寄存器。

30.2.22 Statistical Information Retention Control Register (GETINFOR)

Address(es): EPTPC.GETINFOR 4006 5140h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	INFO
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	INFO	Information Retention Control	When written: 0: No effect 1: Information is retained. When read: 0: Information retention is complete 1: Processing for information retention is in progress. After information fetching is directed, values of some statistical information read before completion of information fetching are not guaranteed.	R/W
b31 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The GETINFOR register controls retention of the following statistical information:

- LCCVRU, LCCVRM, and LCCVRL registers
- PW10VRU, PW10VRM, and PW10VRL registers
- MW10RU, MW10RM, and MW10RL registers.

The only value that is writable to the INFO bit is 1. When setting a value in the PW10VRU, PW10VRM, and PW10VRL registers, or the MW10RU, MW10RM, and MW10RL registers, only set the INFO bit to 1 while the STMR.W10S bit is 1. If the INFO bit is set to 1 before acquisition of the worst 10 values is complete, the information retained in the PW10VRU, PW10VRM, and PW10VRL registers and MW10RU, MW10RM, and MW10RL registers is not guaranteed to be correct. Use the GETW10R.GW10 bit to confirm that acquisition is completed before setting the INFO bit to 1. The INFO bit automatically returns to 0 on completion of information fetching.

30.2.23 Local Clock Counter (LCCVRU, LCCVRM, LCCVRL)

Address(es): EPTPC.LCCVRU 4006 5170h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b15 to b0	—	—	These bits indicate the upper-order 16 bits of the integer portion of the value of the local clock counter.	R
b31 to b16	—	Reserved	These bits are read as 0.	R

30.2.22 统计信息保留控制寄存器(GETINFOR)

Address(es): EPTPC.GETINFOR 4006 5140h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	INFO
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	INFO	信息保留控制	写入时：0：无效1：保留信息。读取时：0：信息保留完成1：信息保留处理正在进行中。定向获取信息后，在获取信息完成之前读取的一些统计信息的值是无法保证的。	R/W
b31 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

GETINFOR寄存器控制以下统计信息的保留：

- LCCVRU、LCCVRM和LCCVRL寄存器
- PW10VRU、PW10VRM和PW10VRL寄存器
- MW10RU、MW10RM和MW10RL寄存器。

可写入INFO位的唯一值是1。在PW10VRU、PW10VRM和PW10VRL寄存器或MW10RU、MW10RM和MW10RL寄存器中设置值时，仅将INFO位设置为1，而STMR.W10S位为1。如果在获取最差10个值之前将INFO位设置为1，则不能保证PW10VRU、PW10VRM和PW10VRL寄存器以及MW10RU、MW10RM和MW10RL寄存器中保留的信息是正确的。在将INFO位设置为1之前，使用GETW10R.GW10位确认采集已完成。信息获取完成后，INFO位自动返回0。

30.2.23 本地时钟计数器（LCCVRU、LCCVRM、LCCVRL）

Address(es): EPTPC.LCCVRU 4006 5170h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b15 to b0	—	—	这些位指示本地时钟计数器值的整数部分的高16位。	R
b31 to b16	—	Reserved	这些位读为0。	R

Address(es): EPTPC.LCCVRM 4006 5174h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b31 to b0	—	—	These bits indicate the lower-order 32 bits of the integer portion of the value in the local clock counter.	R

Address(es): EPTPC.LCCVRL 4006 5178h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b31 to b0	—	—	These bits indicate the fractional portion of the value in the local clock counter (in nanoseconds).	R

The LCCVRU, LCCVRM, and LCCVRL registers indicate the value of the local clock counter. When the GETINFOR.INFO bit is set to 1, the value of the local clock counter at that time is stored in these registers as follows:

- LCCVRU: Upper-order 16 bits of the integer portion in seconds
- LCCVRM: Lower-order 32 bits of the integer portion in seconds
- LCCVRL: Fractional portion in nanoseconds.

For example, if the local time information is 14:25, 44 seconds, 10 milliseconds, 23 microseconds, and 39 nanoseconds, the registers have 14 × 3600 + 25 × 60 + 44 = 51944 (s) = 0000_0000_CAE8h as the setting of the upper-order 48 bits and $10 \times 10^6 + 23 \times 10^3 + 39 = 10023039$ (ns) = 0098_F07Fh as the setting of the lower-order 32 bits.

Address(es): EPTPC.LCCVRM 4006 5174h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b31 to b0	—	—	这些位指示本地时钟计数器中值的整数部分的低32位。	R

Address(es): EPTPC.LCCVRL 4006 5178h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b31 to b0	—	—	这些位指示本地时钟计数器中值的小数部分（以纳秒为单位）。	R

LCCVRU、LCCVRM和LCCVRL寄存器指示本地时钟计数器的值。当。。。的时候GETINFOR.INFO位设置为1，此时本地时钟计数器的值存储在这些寄存器中，如下所示：

- LCCVRU：整数部分的高16位，单位为秒
- LCCVRM：整数部分的低32位，以秒为单位
- LCCVRL：以纳秒为单位的小数部分。

例如，如果本地时间信息为14:25、44秒、10毫秒、23微秒和39纳秒，则寄存器有14×3600+25×60+44=51944(s)=0000_0000_CAE8h作为高位48位和10×106+23×103+39=10023039(ns)=0098_F07Fh作为低位32位的设置。

30.2.24 Positive Gradient Worst 10 Value Register (PW10VRU, PW10VRM, PW10VRL)

Address(es): EPTPC.PW10VRU 4006 5210h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b31 to b0	—	—	These bits indicate the upper-order 32 bits of the positive gradient value.	R

Address(es): EPTPC.PW10VRM 4006 5214h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b31 to b0	—	—	These bits indicate the middle-order 32 bits of the positive gradient value.	R

Address(es): EPTPC.PW10VRL 4006 5218h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b31 to b0	—	—	These bits indicate the lower-order 32 bits of the positive gradient value.	R

30.2.24 正梯度最差10值寄存器（PW10VRU、PW10VRM、PW10VRL）

Address(es): EPTPC.PW10VRU 4006 5210h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b31 to b0	—	—	这些位表示正梯度值的高32位。	R

Address(es): EPTPC.PW10VRM 4006 5214h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b31 to b0	—	—	这些位表示正梯度值的中间32位。	R

Address(es): EPTPC.PW10VRL 4006 5218h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b31 to b0	—	—	这些位表示正梯度值的低32位。	R

The PW10VRU, PW10VRM, and PW10VRL registers indicate the worst 10 of the positive gradient values. When the GETINFOR.INFO bit is set to 1, the worst 10 values at that time are stored in these registers. The format of the worst 10 gradients stored in the registers is the same as for the PLIMITRU, PLIMITRM, and PLIMITRL registers. See the PLIMITR register descriptions. The PW10VRU, PW10VRM, and PW10VRL registers are not used when the device is used as a master clock.

30.2.25 Negative Gradient Worst 10 Value Register (MW10RU, MW10RM, MW10RL)

Address(es): EPTPC.MW10RU 4006 52D0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b31 to b0	—	—	These bits indicate the upper-order 32 bits of the negative gradient value.	R

Address(es): EPTPC.MW10RM 4006 52D4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b31 to b0	—	—	These bits indicate the middle-order 32 bits of the negative gradient value.	R

Address(es): EPTPC.MW10RL 4006 52D8h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PW10VRU、PW10VRM和PW10VRL寄存器指示正梯度值中最差的10个。当。。。的时候GETINFOR.INFO位设置为1，当时最差的10个值存储在这些寄存器中。存储在寄存器中的最差10个梯度的格式与PLIMITRU、PLIMITRM和PLIMITRL寄存器的格式相同。请参阅PLMITR寄存器说明。当器件用作主时钟时，不使用PW10VRU、PW10VRM和PW10VRL寄存器。

30.2.25 负梯度最差10值寄存器（MW10RU、MW10RM、MW10RL）

Address(es): EPTPC.MW10RU 4006 52D0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b31 to b0	—	—	这些位表示负梯度值的高32位。	R

Address(es): EPTPC.MW10RM 4006 52D4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b31 to b0	—	—	这些位表示负梯度值的中间32位。	R

Address(es): EPTPC.MW10RL 4006 52D8h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b31 to b0	—	—	These bits indicate the lower-order 32 bits of the negative gradient value.	R

The MW10RU, MW10RM, and MW10RL registers indicate the worst 10 of the negative gradient values. When the GETINFOR.INFO bit is set to 1, the worst 10 value at that time is stored in these registers. The format of the worst 10 gradients stored in the registers is the same as for the MLIMITRU, MLIMITRM, and MLIMITRL registers. See the MLIMITR register descriptions. The MW10RU, MW10RM, and MW10RL registers are not used when the device is used as a master clock.

30.2.26 Timer Start Time Setting Register m (TMSTTRUm, TMSTTRLm) (m = 0 to 5)

Address(es): EPTPC.TMSTTRU0 4006 5300h, EPTPC.TMSTTRU1 4006 5310h, EPTPC.TMSTTRU2 4006 5320h, EPTPC.TMSTTRU3 4006 5330h, EPTPC.TMSTTRU4 4006 5340h, EPTPC.TMSTTRU5 4006 5350h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b31 to b0	—	—	These bits specify the upper-order 32 bits of the start time of the pulse output timer in nanoseconds.	R/W

Address(es): EPTPC.TMSTTRL0 4006 5304h, EPTPC.TMSTTRL1 4006 5314h, EPTPC.TMSTTRL2 4006 5324h, EPTPC.TMSTTRL3 4006 5334h EPTPC.TMSTTRL4 4006 5344h, EPTPC.TMSTTRL5 4006 5354h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b31 to b0	—	—	These bits specify the lower-order 32 bits of the start time of the pulse output timer in nanoseconds.	R/W

The TMSTTRUm and TMSTTRLm register specify the start time of pulse output timer m. Set the start time of pulse output timer m (64 bits) in nanoseconds. Although the setting is in nanoseconds, the start time of pulse output timer m depends on the resolution of the STCA clock. For example, if the STCA clock is running at 50 MHz, 1 cycle takes 20 ns, so the time at which the timer starts might differ from the time set in these registers by up to 20 ns. When writing to the registers, write values consecutively in the order of TMSTTRUm, TMSTTRLm, while the TMSTARTR.ENm bit is 0. The format for setting times in these registers differs from that described in section 30.2.23, Local Clock Counter (LCCVRU, LCCVRM, LCCVRL).

Bit	Symbol	位名称	Description	R/W
b31 to b0	—	—	这些位表示负梯度值的低32位。	R

MW10RU、MW10RM和MW10RL寄存器指示负梯度值中最差的10个。当GETINFOR.INFO位设置为1时，此时最差的10值将存储在这些寄存器中。存储在寄存器中的最差10个梯度的格式与MLIMITRU、MLIMITRM和MLIMITRL寄存器的格式相同。请参阅MLIMITR寄存器说明。当器件用作主时钟时，不使用MW10RU、MW10RM和MW10RL寄存器。

30.2.26 定时器启动时间设置寄存器m(TMSTTRUm TMSTTRLm)(m=0to5)

Address(es): EPTPC.TMSTTRU0 4006 5300h, EPTPC.TMSTTRU1 4006 5310h, EPTPC.TMSTTRU2 4006 5320h, EPTPC.TMSTTRU3 4006 5330h, EPTPC.TMSTTRU4 4006 5340h, EPTPC.TMSTTRU5 4006 5350h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b31 to b0	—	—	这些位指定脉冲输出定时器开始时间的高32位，单位为纳秒。	R/W

Address(es): EPTPC.TMSTTRL0 4006 5304h, EPTPC.TMSTTRL1 4006 5314h, EPTPC.TMSTTRL2 4006 5324h, EPTPC.TMSTTRL3 4006 5334h EPTPC.TMSTTRL4 4006 5344h, EPTPC.TMSTTRL5 4006 5354h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b31 to b0	—	—	这些位指定脉冲输出定时器开始时间的低32位，单位为纳秒。	R/W

TMSTTRUm和TMSTTRLm寄存器指定脉冲输出定时器m的启动时间。以纳秒为单位设置脉冲输出定时器m（64位）的开始时间。虽然设置单位为纳秒，但脉冲输出定时器m的启动时间取决于STCA时钟的分辨率。例如，如果STCA时钟以50MHz运行，则1个周期需要20ns，因此定时器启动的时间可能与这些寄存器中设置的时间相差最多20ns。写入寄存器时，按TMSTTRUm、TMSTTRLm的顺序连续写入值，同时TMSTARTR.ENm位为0。这些寄存器中设置时间的格式与第30.2.23节，本地时钟计数器（LCCVRU，LCCVRM，LCCVRL）。

30.2.27 Timer Cycle Setting Register m (TMCYCRm) (m = 0 to 5)

Address(es): EPTPC.TMCYCR0 4006 5308h, EPTPC.TMCYCR1 4006 5318h, EPTPC.TMCYCR2 4006 5328h, EPTPC.TMCYCR3 4006 5338h EPTPC.TMCYCR4 4006 5348h, EPTPC.TMCYCR5 4006 5358h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—														
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b29 to b0	—	—	These bits specify the cycle of the pulse output timer in nanoseconds. Set a value that is equivalent to at least 4 cycles of the STCA clock.	R/W
b31, b30	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The TMCYCRm registers specify the period of the output signal generated by the associated pulse output timer m. Set a value in nanoseconds that is equivalent to at least 4 cycles of the STCA clock while the value of the TMSTARTR.ENm bit is 0. Although the setting is in nanoseconds, the period of the output signal generated by pulse output timer m and the time at which the timer starts depend on the period of the STCA clock. For example, if the STCA clock is running at 50 MHz, 1 cycle takes 20 ns, so the clock source for counting by pulse output timer m might differ from the period set in these registers by up to 19 ns. The SYNFP module handles calculations to correct this difference.

For example, if the setting for the timer period is 81 ns and the STCA clock is running at 50 MHz, the only available settings close to the actual timer period are for 80 or 100 ns. By setting the timer period in the SYNFP module to 80 ns for 19 and to 100 ns for 1 of every 20 cycles, the average period can be adjusted to 81 ns.

$$(80\ (\text{ns}) \times 19 + 100\ (\text{ns}) \times 1)/20 = 81\ (\text{ns})$$

The minimum value that can be set in a TMCYCRm register is 4 cycles of the STCA clock. For example, if the STCA clock is running at 50 MHz, the minimum setting corresponds to 80 ns. Timer operation is not guaranteed if a value set in one of these registers is less than this value.

30.2.28 Timer Pulse Width Setting Register m (TMPLSRm) (m = 0 to 5)

Address(es): EPTPC.TMPLSR0 4006 530Ch, EPTPC.TMPLSR1 4006 531Ch, EPTPC.TMPLSR2 4006 532Ch, EPTPC.TMPLSR3 4006 533Ch, EPTPC.TMPLSR4 4006 534Ch, EPTPC.TMPLSR5 4006 535Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b28 to b0	—	—	These bits specify the high-level width of the pulse signal from the timer in nanoseconds. Set a value that is equivalent to at least 2 cycles of the STCA clock.	R/W
b31 to b29	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

30.2.27 定时器周期设置寄存器m(TMCYCRm)(m=0to5)

Address(es): EPTPC.TMCYCR0 4006 5308h, EPTPC.TMCYCR1 4006 5318h, EPTPC.TMCYCR2 4006 5328h, EPTPC.TMCYCR3 4006 5338h EPTPC.TMCYCR4 4006 5348h, EPTPC.TMCYCR5 4006 5358h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—														
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b29 to b0	—	—	这些位以纳秒为单位指定脉冲输出定时器的周期。设置一个等于至少4个STCA时钟周期的值。	R/W
b31, b30	—	Reserved	这些位被读取为0。写入值应为0。	R/W

TMCYCRm寄存器指定由相关脉冲输出定时器m生成的输出信号的周期。当TMSTARTR.ENm位的值为0时，设置一个以纳秒为单位的值，该值相当于STCA时钟的至少4个周期。虽然设置以纳秒为单位，但脉冲输出定时器m产生的输出信号的周期和定时器启动的时间取决于STCA时钟的周期。例如，如果STCA时钟以50MHz运行，则1个周期需要20ns，因此脉冲输出定时器m计数的时钟源可能与这些寄存器中设置的周期相差最多19ns。SYNFP模块处理计算以纠正这种差异。

例如，如果定时器周期设置为81ns，并且STCA时钟运行在50MHz，则接近实际定时器周期的唯一可用设置是80或100ns。通过将SYNFP模块中的定时器周期设置为19个80ns和每20个周期中的1个100ns，可以将平均周期调整为81ns。

$$(80\ (\text{ns}) \times 19 + 100\ (\text{ns}) \times 1)/20 = 81\ (\text{ns})$$

可以在TMCYCRm寄存器中设置的最小值是STCA时钟的4个周期。例如，如果STCA时钟以50MHz运行，则最小设置对应于80ns。如果这些寄存器之一中设置的值小于该值，则不能保证定时器操作。

30.2.28 定时器脉冲宽度设置寄存器m(TMPLSRm)(m=0to5)

Address(es): EPTPC.TMPLSR0 4006 530Ch, EPTPC.TMPLSR1 4006 531Ch, EPTPC.TMPLSR2 4006 532Ch, EPTPC.TMPLSR3 4006 533Ch, EPTPC.TMPLSR4 4006 534Ch, EPTPC.TMPLSR5 4006 535Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—													
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b28 to b0	—	—	这些位指定来自定时器的脉冲信号的高电平宽度（以纳秒为单位）。设置一个等于至少2个STCA时钟周期的值。	R/W
b31 to b29	—	Reserved	这些位被读取为0。写入值应为0。	R/W

The TMPLSRm registers specify the high-level width of the output signal generated by the associated pulse output timer m. When the TMSTARTR.ENm bit is 0, set a value corresponding to a time no shorter than 2 cycles of the STCA clock in nanoseconds. Although the setting is in nanoseconds, the high-level width of the signal from the timer depends on the period of the STCA clock. The method for correcting the high-level width of the signal from the timer is the same as that for correcting the timer periods set in the TMCYCRm register.

The upper-order 3 bits of the TMPLSRm register are reserved. These bits are read as 000b. When writing, write 000b to these bits.

30.2.29 Timer Start Register (TMSTARTR)

Address(es): EPTPC.TMSTARTR 4006 537Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	EN5	EN4	EN3	EN2	EN1	EN0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	EN0	Pulse Output Timer 0 Start	0: Stop pulse output timer 0 1: Start pulse output timer 0.	R/W
b1	EN1	Pulse Output Timer 1 Start	0: Stop pulse output timer 1 1: Start pulse output timer 1.	R/W
b2	EN2	Pulse Output Timer 2 Start	0: Stop pulse output timer 2 1: Start pulse output timer 2.	R/W
b3	EN3	Pulse Output Timer 3 Start	0: Stop pulse output timer 3 1: Start pulse output timer 3.	R/W
b4	EN4	Pulse Output Timer 4 Start	0: Stop pulse output timer 4 1: Start pulse output timer 4.	R/W
b5	EN5	Pulse Output Timer 5 Start	0: Stop pulse output timer 5 1: Start pulse output timer 5.	R/W
b31 to b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The TMSTARTR register starts and stops the pulse output timers.

TMPLSRm寄存器指定由相关脉冲输出定时器m生成的输出信号的高电平宽度。当TMSTARTR.ENm位为0时，设置一个对应于时间不短于STCA时钟的2个周期（以纳秒为单位）的值。虽然设置以纳秒为单位，但来自定时器的信号的高电平宽度取决于STCA时钟的周期。校正定时器信号高电平宽度的方法与校正TMCYCRm寄存器中设置的定时器周期的方法相同。

TMPLSRm寄存器的高3位被保留。这些位被读取为000b。写入时，将000b写入这些位。

30.2.29 定时器启动寄存器(TMSTARTR)

Address(es): EPTPC.TMSTARTR 4006 537Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	EN5	EN4	EN3	EN2	EN1	EN0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	EN0	脉冲输出定时器0启动	0：停止脉冲输出定时器01 ：启动脉冲输出定时器0。	R/W
b1	EN1	脉冲输出定时器1启动	0：停止脉冲输出定时器11 ：启动脉冲输出定时器1。	R/W
b2	EN2	脉冲输出定时器2启动	0：停止脉冲输出定时器21 ：启动脉冲输出定时器2。	R/W
b3	EN3	脉冲输出定时器3启动	0：停止脉冲输出定时器31 ：启动脉冲输出定时器3。	R/W
b4	EN4	脉冲输出定时器4启动	0：停止脉冲输出定时器41 ：启动脉冲输出定时器4。	R/W
b5	EN5	脉冲输出定时器5启动	0：停止脉冲输出定时器51 ：启动脉冲输出定时器5。	R/W
b31 to b6	—	Reserved	这些位被读取为0。写入值应为0。	R/W

TMSTARTR寄存器启动和停止脉冲输出定时器。

30.2.30 SYNFP Status Register (SYSR)

Address(es): EPTPC0.SYSR 4006 5800h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	GENDN	RESDN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	INFABT	—	RECLP	—	—	—	—	—	DRQOVR	INTDEV	DRPTO	—	MPDUD	INTCHG	OFMUD
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	OFMUD	offsetFromMaster Value Update Flag	0: offsetFromMaster value not updated 1: offsetFromMaster value updated.	R/W*1
b1	INTCHG	Receive logMessageInterval Value Change Detection Flag	0: Received logMessageInterval value did not change 1: Received logMessageInterval value changed.	R/W*1
b2	MPDUD	meanPathDelay Value Update Flag	0: meanPathDelay value not updated 1: meanPathDelay value updated.	R/W*1
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	DRPTO	Delay_Resp/Pdelay_Resp Reception Timeout Detection Flag	0: No Delay_Resp/Pdelay_Resp timeout occurred 1: Delay_Resp/Pdelay_Resp timeout occurred.	R/W*1
b5	INTDEV	Receive logMessageInterval Value Out-of-Range Flag	0: Received logMessageInterval value is within the range 1: Received logMessageInterval value is out of the range.	R/W*1
b6	DRQOVR	Delay_Req Reception FIFO Overflow Detection Flag	0: Received Delay_Req did not cause the reception FIFO to overflow 1: Received Delay_Req caused the reception FIFO to overflow.	R/W*1
b11 to b7	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b12	RECLP	Loop Reception Detection Flag	0: Received message did not return through a loop 1: Received message returned through a loop.	R/W*1
b13	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b14	INFABT	Control Information Abnormality Detection Flag	0: No abnormality in control information 1: Abnormality in control information.	R/W*1
b15	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b16	RESDN	Response Stop Completion Detection Flag	0: Stopping responses not completed 1: Stopping responses completed.	R/W*1
b17	GENDN	Generation Stop Completion Detection Flag	0: Stopping generation not completed 1: Stopping generation completed.	R/W*1
b23 to b18	—	Reserved	These bits are read as undefined. The write value should be 0.	R/W
b31 to b24	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Writing 1 clears the flag. Writing 0 does not affect the flag value.

The SYSR register indicates the state of the SYNFP module.

OFMUD flag (offsetFromMaster Value Update Flag)

The OFMUD flag indicates that the value of offsetFromMaster was updated.

INTCHG flag (Receive logMessageInterval Value Change Detection Flag)

The INTCHG flag indicates that the logMessageInterval value of the Delay_Resp, Sync or Announce message differs from the previously received value.

30.2.30 SYNFP状态寄存器(SYSR)

Address(es): EPTPC0.SYSR 4006 5800h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	GENDN	RESDN
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	INFABT	—	RECLP	—	—	—	—	—	DRQOVR	INTDEV	DRPTO	—	MPDUD	INTCHG	OFMUD
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	OFMUD	offsetFromMaster值更新标志	0：offsetFromMaster值未更新1：offsetFromMaster值已更新。	R/W*1
b1	INTCHG	接收logMessageInterval值变化检测标志	0：接收到的logMessageInterval值没有改变1：接收到的logMessageInterval值改变了。	R/W*1
b2	MPDUD	meanPathDelay值更新标志	0：meanPathDelay值未更新1：meanPathDelay值已更新。	R/W*1
b3	—	Reserved	该位读取为0。写入值应为0。	R/W
b4	DRPTO	Delay_Resp/Pdelay_Resp接收超时检测Flag	0：未发生Delay_RespPdelay_Resp超时1：发生Delay_RespPdelay_Resp超时。	R/W*1
b5	INTDEV	Receive logMessageInterval值超出范围标志	0：接收到的logMessageInterval值在范围内1：接收到的logMessageInterval值超出范围。	R/W*1
b6	DRQOVR	Delay_Req Reception FIFO溢出检测标志	0：接收到Delay_Req没有导致接收FIFO溢出1：接收到Delay_Req导致接收FIFO溢出。	R/W*1
b11 to b7	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b12	RECLP	循环接收检测Flag	0：接收到的消息没有通过循环返回1：接收到的消息通过循环返回。	R/W*1
b13	—	Reserved	该位读取为0。写入值应为0。	R/W
b14	INFABT	控制信息异常检测标志	0：控制信息无异常1：控制信息异常。	R/W*1
b15	—	Reserved	该位读取为0。写入值应为0。	R/W
b16	RESDN	响应停止完成检测标志	0：未完成停止响应1：已完成停止响应。	R/W*1
b17	GENDN	发电停止完成检测标志	0：停止生成未完成1：停止生成完成。	R/W*1
b23 to b18	—	Reserved	这些位被读取为未定义。写入值应为0。	R/W
b31 to b24	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 写1清除标志。写入0不影响标志值。

SYSR寄存器指示SYNFP模块的状态。

OFMUD标志（offsetFromMaster值更新标志）

OFMUD标志表示offsetFromMaster的值已更新。

INTCHG标志（接收logMessageInterval值变化检测标志）

INTCHG标志指示Delay_Resp、Sync或Announce消息的logMessageInterval值与先前接收的值不同。

MPDUD flag (meanPathDelay Value Update Flag)

The MPDUD flag indicates that the value of meanPathDelay was updated.

DRPTO flag (Delay_Resp/Pdelay_Resp Reception Timeout Detection Flag)

The DRPTO flag indicates that a Delay_Resp or Pdelay_Resp message was not received within the period set in the RSTOUTR register.

INTDEV flag (Receive logMessageInterval Value Out-of-Range Flag)

The INTDEV flag indicates that a Delay_Resp message was received with a logMessageInterval value outside the range, -7 to +6.

DRQOVR flag (Delay_Req Reception FIFO Overflow Detection Flag)

The DRQOVR flag indicates that the FIFO buffer for storing information from received Delay_Req messages holds 32 or more entries.

RECLP flag (Loop Reception Detection Flag)

The RECLP flag indicates that the value of the sourcePortIdentity field in a received PTP message matches the local PortIdentity as set in the SYCIDRU, SYCIDRL, and SYPNUMR registers.

INFABT flag (Control Information Abnormality Detection Flag)

The INFABT flag indicates that the control information includes a mismatch. If an erroneous frame is detected because of a corrupted frame or noise in the external circuit when the ETHERC and EPTPC are receiving data, subsequent normal frames might not be received properly.

Reset the EDMAC, ETHERC, and EPTPC after an erroneous frame is detected. Then, wait for the required number of cycles before setting communications again.

- Detecting an erroneous frame

  To detect an erroneous frame, read the INFABT flag in the SYNFP Status Register (SYSR) of EPTPC0. An INFABT flag is provided for EPTPC0.
  When the EPTPC0 is not used and only the EDMAC0 and ETHERC0 are used to receive and transmit standard Ethernet frames, read the INFABT flag to detect an erroneous frame.

- Resetting after detection of an erroneous flag

  When the EPTPC0.SYSR.INFABT flag is set to 1, reset the EPTPC0 and ETHERC0, and then wait for the required number of cycles before setting the registers.
  When the EPTPC0 is not used and only the EDMAC0 and ETHERC0 are used to receive and transmit standard Ethernet frames, reset the EPTPC0 and the registers. In this case, resetting PTPEDMAC is not required.
  To reset the EPTPC0 and the registers:

  a. Set the EPTPC_CFG.PTRSTR.RESET bit to 1 (reset the EPTPC0 by software).
  b. Set the EDMAC0.EDMR.SWR bit to 1 (reset the EDMAC0 and ETHERC0 by software).
  c. Use a software loop or timer to wait for at least 64 cycles of the peripheral module clock, PCLKA. This step is necessary to initialize EDMAC0 and ETHERC0.
  d. Set the EPTPC_CFG.PTRSTR.RESET bit to 0 (release the EPTPC0 reset).
  e. Reset communications by setting the EDMAC0, ETHERC0, PTPEDMAC, and EPTPC0 registers to enable communications.

RESDN flag (Response Stop Completion Detection Flag)

The RESDN flag indicates the end of processing for transmission of a Delay_Resp or Pdelay_Resp as response messages when the handling of a received Delay_Req or Pdelay_Req by the SYNFP module is disabled in the SYRFL1R or SYRVLDR register.

MPDUD标志（meanPathDelay值更新标志）

MPDUD标志表明meanPathDelay的值已更新。

DRPTO标志（Delay_RespPdelay_Resp接收超时检测标志）

DRPTO标志表明延迟_Resp或Pdelay_Resp消息在设置的周期内没有收到。
RSTOUTR register.

INTDEV标志（接收logMessageInterval值超出范围标志）

INTDEV标志指示接收到的Delay_Resp消息的logMessageInterval值超出了-7到+6的范围。

DRQOVR标志（Delay_Req接收FIFO溢出检测标志）

DRQOVR标志指示用于存储来自接收到的Delay_Req消息的信息的FIFO缓冲区包含32个或更多条目。

RECLP标志（循环接收检测标志）

RECLP标志表示接收到的PTP消息中的sourcePortIdentity字段的值与本地
在SYCIDRU、SYCIDRL和SYPNUMR寄存器中设置的PortIdentity。

INFABT标志（控制信息异常检测标志）

INFABT标志指示控制信息包括不匹配。如果在ETHERC和EPTPC接收数据时，由于帧损坏或外部电路中的噪声而检测到错误帧，则可能无法正确接收后续正常帧。

在检测到错误帧后重置EDMAC、ETHERC和EPTPC。然后，在再次设置通信之前等待所需的周期数。

- 检测错误帧

  要检测错误帧，请读取EPTPC0的SYNFP状态寄存器(SYSR)中的INFABT标志。一个
  为EPTPC0提供了INFABT标志。
  不使用EPTPC0仅使用EDMAC0和ETHERC0接收和发送标准时
  以太网帧，读取INFABT标志以检测错误帧。

- 检测到错误标志后重置

  当EPTPC0.SYSR.INFABT标志设置为1时，复位EPTPC0和ETHERC0，然后在设置寄存器之前等待所需的周期数。不使用EPTPC0仅使用EDMAC0和ETHERC0接收和发送标准时

  以太网帧，复位EPTPC0和寄存器。在这种情况下，不需要重置PTPEDMAC。
  复位EPTPC0和寄存器：a．将EPTPC_CFG.PTRSTR.RESET位设置为1（通过软件复位EPTPC0）。

  湾。将EDMAC0.EDMR.SWR位设置为1（通过软件复位EDMAC0和ETHERC0）。

  C。使用软件循环或定时器等待外设模块时钟PCLKA的至少64个周期。这一步是初始化EDMAC0和ETHERC0所必需的。

  d。将EPTPC_CFG.PTRSTR.RESET位设置为0（释放EPTPC0复位）。

  e.通过设置EDMAC0、ETHERC0、PTPEDMAC和EPTPC0寄存器来复位通信以启用通信。

RESDN标志（响应停止完成检测标志）

当在SYRFL1R或SYRVLDR寄存器中禁用SYNFP模块对接收到的Delay_Req或Pdelay_Req的处理时，RESDN标志指示作为响应消息发送Delay_Resp或Pdelay_Resp的处理结束。

GENDN flag (Generation Stop Completion Detection Flag)

The GENDN flag indicates the end of processing for transmission of messages of a type disabled in the SYTRENR or SYRVLDR register.

30.2.31 SYNFP Status Notification Enable Register (SYIPR)

Address(es): EPTPC0.SYIPR 4006 5804h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	GENDN	RESDN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	INFABT	—	RECLP	—	—	—	—	—	DRQOVR	INTDEV	DRPTO	—	MPDUD	INTCHG	OFMUD
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	OFMUD	SYSR.OFMUD Status Notification Enable	0: Disable notification of the SYSR.OFMUD state 1: Enable notification of the SYSR.OFMUD state.	R/W
b1	INTCHG	SYSR.INTCHG Status Notification Enable	0: Disable notification of the SYSR.INTCHG state 1: Enable notification of the SYSR.INTCHG state.	R/W
b2	MPDUD	SYSR.MPDUD Status Notification Enable	0: Disable notification of the SYSR.MPDUD state 1: Enable notification of the SYSR.MPDUD state.	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	DRPTO	SYSR.DRPTO Status Notification Enable	0: Disable notification of the SYSR.DRPTO state 1: Enable notification of the SYSR.DRPTO state.	R/W
b5	INTDEV	SYSR.INTDEV Status Notification Enable	0: Disable notification of the SYSR.INTDEV state 1: Enable notification of the SYSR.INTDEV state.	R/W
b6	DRQOVR	SYSR.DRQOVR Status Notification Enable	0: Disable notification of the SYSR.DRQOVR state 1: Enable notification of the SYSR.DRQOVR state.	R/W
b11 to b7	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b12	RECLP	SYSR.RECLP Status Notification Enable	0: Disable notification of the SYSR.RECLP state 1: Enable notification of the SYSR.RECLP state.	R/W
b13	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b14	INFABT	SYSR.INFABT Status Notification Enable	0: Disable notification of the SYSR.INFABT state 1: Enable notification of the SYSR.INFABT state.	R/W
b15	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b16	RESDN	SYSR.RESDN Status Notification Enable	0: Disable notification of the SYSR.RESDN state 1: Enable notification of the SYSR.RESDN state.	R/W
b17	GENDN	SYSR.GENDN Status Notification Enable	0: Disable notification of the SYSR.GENDN state 1: Enable notification of the SYSR.GENDN state.	R/W
b23 to b18	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b31 to b24	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The SYIPR register specifies whether the MIESR.SY0 flag reflects changes in the state of the SYNFP0 module.

GENDN标志（生成停止完成检测标志）

GENDN标志指示SYTRENR中禁用的类型的消息传输处理结束或
SYRVLDR register.

30.2.31 SYNFP状态通知使能寄存器(SYIPR)

Address(es): EPTPC0.SYIPR 4006 5804h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	GENDN	RESDN
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	INFABT	—	RECLP	—	—	—	—	—	DRQOVR	INTDEV	DRPTO	—	MPDUD	INTCHG	OFMUD
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	OFMUD	SYSR.OFMUD Status 通知启用	0：禁用SYSR.OFMUD状态通知1：启用SYSR.OFMUD状态通知。	R/W
b1	INTCHG	SYSR.INTCHG Status 通知启用	0：禁用SYSR.INTCHG状态通知1：启用SYSR.INTCHG状态通知。	R/W
b2	MPDUD	SYSR.MPDUD Status 通知启用	0：禁用SYSR.MPDUD状态通知1：启用SYSR.MPDUD状态通知。	R/W
b3	—	Reserved	该位读取为0。写入值应为0。	R/W
b4	DRPTO	SYSR.DRPTO Status 通知启用	0：禁用SYSR.DRPTO状态通知1：启用SYSR.DRPTO状态通知。	R/W
b5	INTDEV	SYSR.INTDEV Status 通知启用	0：禁用SYSR.INTDEV状态通知1：启用SYSR.INTDEV状态通知。	R/W
b6	DRQOVR	SYSR.DRQOVR Status 通知启用	0：禁用SYSR.DRQOVR状态通知1：启用SYSR.DRQOVR状态通知。	R/W
b11 to b7	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b12	RECLP	SYSR.RECLP Status 通知启用	0：禁用SYSR.RECLP状态通知1：启用SYSR.RECLP状态通知。	R/W
b13	—	Reserved	该位读取为0。写入值应为0。	R/W
b14	INFABT	SYSR.INFABT Status 通知启用	0：禁用SYSR.INFABT状态通知1：启用SYSR.INFABT状态通知。	R/W
b15	—	Reserved	该位读取为0。写入值应为0。	R/W
b16	RESDN	SYSR.RESDN Status 通知启用	0：禁用SYSR.RESDN状态通知1：启用SYSR.RESDN状态通知。	R/W
b17	GENDN	SYSR.GENDN Status 通知启用	0：禁用SYSR.GENDN状态通知1：启用SYSR.GENDN状态通知。	R/W
b23 to b18	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b31 to b24	—	Reserved	这些位被读取为0。写入值应为0。	R/W

SYIPR寄存器指定MIESR.SY0标志是否反映SYNFP0模块状态的变化。

30.2.32 SYNFP MAC Address Register (SYMACRU, SYMACRL)

Address(es): EPTPC0.SYMACRU 4006 5810h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b23 to b0	—	—	These bits specify the upper-order 24 bits of the local MAC address.	R/W
b31 to b24	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Address(es): EPTPC0.SYMACRL 4006 5814h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b23 to b0	—	—	These bits specify the lower-order 24 bits of the local MAC address.	R/W
b31 to b24	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The SYMACRU and SYMACRL registers specify the local MAC address for Ethernet ports 0. Set these registers before starting the EDMAC, ETHERC, or PTPEDMAC. Do not change the settings while the EPTPC is operating.

30.2.32 SYNFPMAC地址寄存器(SYMACRU SYMACRL)

Address(es): EPTPC0.SYMACRU 4006 5810h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—								
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b23 to b0	—	—	这些位指定本地MAC地址的高24位。	R/W
b31 to b24	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Address(es): EPTPC0.SYMACRL 4006 5814h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—								
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b23 to b0	—	—	这些位指定本地MAC地址的低24位。	R/W
b31 to b24	—	Reserved	这些位被读取为0。写入值应为0。	R/W

SYMACRU和SYMACRL寄存器指定以太网端口0的本地MAC地址。在启动EDMAC、ETHERC或PTPEDMAC之前设置这些寄存器。请勿在EPTPC运行时更改设置。

30.2.33 SYNFP LLC-CTL Value Register (SYLLCCTLR)

Address(es): EPTPC0.SYLLCCTLR 4006 5818h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	CTL[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bit	Symbol	Bit name	Description	R/W
b7 to b0	CTL[7:0]	LLC-CTL Field	These bits specify the value used for the control field in the LLC sublayer when generating IEEE802.3 frames.	R/W
b31 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The SYLLCCTLR register specifies the control field (LLC-CTL) value of LLC frames generated by the SYNFP module. Set this register before starting the EDMAC, ETHERC, or PTPEDMAC. Do not change the settings while the EPTPC is operating.

30.2.34 SYNFP Local IP Address Register (SYIPADDRR)

Address(es): EPTPC0.SYIPADDRR 4006 581Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b31 to b0	—	—	These bits specify the local IP address.	R/W

The SYIPADDRR register specifies the local IP address for Ethernet port 0. Set the SYIPADDRR register before starting the EDMAC, ETHERC, or PTPEDMAC. Do not change the settings while the EPTPC is operating.

30.2.33 SYNFPLLC-CTL值寄存器(SYLLCCTLR)

Address(es): EPTPC0.SYLLCCTLR 4006 5818h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	CTL[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bit	Symbol	位名称	Description	R/W
b7 to b0	CTL[7:0]	LLC-CTL Field	这些位指定在生成IEEE802.3帧时用于LLC子层中的控制字段的值。	R/W
b31 to b8	—	Reserved	这些位被读取为0。写入值应为0。	R/W

SYLLCCTLR寄存器指定由SYNFP模块生成的LLC帧的控制字段(LLC-CTL)值。在启动EDMAC、ETHERC或PTPEDMAC之前设置该寄存器。请勿在EPTPC运行时更改设置。

30.2.34 SYNFP本地IP地址寄存器(SYIPADDRR)

Address(es): EPTPC0.SYIPADDRR 4006 581Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b31 to b0	—	—	这些位指定本地IP地址。	R/W

SYIPADDRR寄存器指定以太网端口0的本地IP地址。在启动EDMAC、ETHERC或PTPEDMAC之前设置SYIPADDRR寄存器。请勿在EPTPC运行时更改设置。

30.2.35 SYNFP Specification Version Setting Register (SYSPVRR)

Address(es): EPTPC0.SYSPVRR 4006 5840h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	TRSP[3:0]				VER[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	VER[3:0]	versionPTP Field Value	These bits specify the versionPTP field value of the PTP v2 header. When a message is received, this value is compared with the versionPTP field of the received frame. In generating messages, the value is used for the versionPTP field of the frame to be transmitted. Set these bits to 0010b (PTP v2).	R/W
b7 to b4	TRSP[3:0]	transportSpecific Field Value	These bits specify the transportSpecific field value of the PTP v2 header. When a message is received, this value is compared with the transportSpecific field of the received frame. In generating messages, the value is used for the transportSpecific field of the frame to be transmitted. Set these bits to 0000b (IEEE 1588).	R/W
b31 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The SYSPVRR register specifies the transportSpecific and versionPTP field values of the PTP v2 message header. Do not change the settings while reception or transmission of PTP messages is enabled.

30.2.36 SYNFP Domain Number Setting Register (SYDOMR)

Address(es): EPTPC0.SYDOMR 4006 5844h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	DNUM[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	DNUM[7:0]	domainNumber Field Value Setting	These bits specify the domainNumber field value of the PTP v2 header. When a message is received, this value is compared with the domainNumber field of the received frame as a condition for PTP reception processing. In generating messages, the value is used for the domainNumber field of the frame to be transmitted.	R/W
b31 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

30.2.35 SYNFP规范版本设置寄存器(SYSPVRR)

Address(es): EPTPC0.SYSPVRR 4006 5840h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	TRSP[3:0]				VER[3:0]			
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bit	Symbol	位名称	Description	R/W
b3 to b0	VER[3:0]	versionPTP字段值	这些位指定PTPv2标头的versionPTP字段值。当接收到消息时，将该值与接收帧的versionPTP字段进行比较。在生成消息时，该值用于要传输的帧的versionPTP字段。将这些位设置为0010b(PTPv2)。	R/W
b7 to b4	TRSP[3:0]	运输特定字段值	这些位指定PTPv2标头的传输特定字段值。当接收到消息时，将该值与接收帧的transportSpecific字段进行比较。在生成消息时，该值用于要传输的帧的transportSpecific字段。将这些位设置为0000b(IEEE1588)。	R/W
b31 to b8	—	Reserved	这些位被读取为0。写入值应为0。	R/W

SYSPVRR寄存器指定PTPv2消息头的transportSpecific和versionPTP字段值。在启用PTP消息的接收或传输时不要更改设置。

30.2.36 SYNFP域号设置寄存器(SYDOMR)

Address(es): EPTPC0.SYDOMR 4006 5844h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	DNUM[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b7 to b0	DNUM[7:0]	domainNumber字段值设置	这些位指定PTPv2标头的domainNumber字段值。当接收到消息时，将该值与接收帧的domainNumber字段进行比较，作为PTP接收处理的条件。在生成消息时，该值用于要传输的帧的domainNumber字段。	R/W
b31 to b8	—	Reserved	这些位被读取为0。写入值应为0。	R/W

The SYDOMR register specifies the domainNumber field value of the PTP v2 message header. Do not change the settings while reception or transmission of PTP messages is enabled.

30.2.37 Announce Message Flag Field Setting Register (ANFR)

Address(es): EPTPC0.ANFR 4006 5850h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	FLAG14	FLAG13	—	—	FLAG10	—	FLAG8	—	—	FLAG5	FLAG4	FLAG3	FLAG2	FLAG1	FLAG0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	FLAG0	leap61	This bit specifies the logical value of the leap61 member of timePropertiesDS. 0: Set leap61 to FALSE 1: Set leap61 to TRUE.	R/W
b1	FLAG1	leap59	This bit specifies the logical value of the leap59 member of timePropertiesDS. 0: Set leap59 to FALSE 1: Set leap59 to TRUE.	R/W
b2	FLAG2	currentUtcOffsetValid	This bit specifies the logical value of the currentUtcOffsetValid member of timePropertiesDS. 0: Set currentUtcOffsetValid to FALSE 1: Set currentUtcOffsetValid to TRUE.	R/W
b3	FLAG3	ptpTimescale	This bit specifies the logical value of the ptpTimescale member of timePropertiesDS. 0: Set ptpTimescale to FALSE 1: Set ptpTimescale to TRUE.	R/W
b4	FLAG4	timeTraceable	This bit specifies the logical value of the timeTraceable member of timePropertiesDS. 0: Set timeTraceable to FALSE 1: Set timeTraceable to TRUE.	R/W
b5	FLAG5	frequencyTraceable	This bit specifies the logical value of the frequencyTraceable member of timePropertiesDS. 0: Set frequencyTraceable to FALSE 1: Set frequencyTraceable to TRUE.	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	FLAG8	alternateMasterFlag	0: Set alternateMasterFlag to FALSE 1: Set alternateMasterFlag to TRUE.	R/W
b9	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b10	FLAG10	unicastFlag	0: Set unicastFlag to FALSE 1: Set unicastFlag to TRUE.	R/W
b12, b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b13	FLAG13	PTP profile Specific 1	0: Set PTP profile Specific 1 to FALSE 1: Set PTP profile Specific 1 to TRUE.	R/W
b14	FLAG14	PTP profile Specific 2	0: Set PTP profile Specific 2 to FALSE 1: Set PTP profile Specific 2 to TRUE.	R/W
b31 to b15	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The ANFR register specifies the flagField section of the header when the SYNFP module is to generate an Announce message. The values specified in this register are only reflected in the SYNFP module after the SYRVLDR.ANUP bit is set to 1.

SYDOMR寄存器指定PTPv2消息头的domainNumber字段值。在启用PTP消息的接收或传输时不要更改设置。

30.2.37 宣布消息标志字段设置寄存器(ANFR)

Address(es): EPTPC0.ANFR 4006 5850h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	FLAG14	FLAG13	—	—	FLAG10	—	FLAG8	—	—	FLAG5	FLAG4	FLAG3	FLAG2	FLAG1	FLAG0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	FLAG0	leap61	该位指定timePropertiesDS的leap61成员的逻辑值。0：将leap61设置为FALSE1：将leap61设置为TRUE。	R/W
b1	FLAG1	leap59	该位指定timePropertiesDS的leap59成员的逻辑值。0：将leap59设置为FALSE1：将leap59设置为TRUE。	R/W
b2	FLAG2	currentUtcOffsetValid	该位指定timePropertiesDS的currentUtcOffsetValid成员的逻辑值。0：将currentUtcOffsetValid设置为FALSE1：将currentUtcOffsetValid设置为TRUE。	R/W
b3	FLAG3	ptpTimescale	该位指定timePropertiesDS的ptpTimescale成员的逻辑值。0：将ptpTimescale设置为FALSE1：将ptpTimescale设置为TRUE。	R/W
b4	FLAG4	timeTraceable	该位指定timePropertiesDS的timeTraceable成员的逻辑值。0：将timeTraceable设置为FALSE1：将timeTraceable设置为TRUE。	R/W
b5	FLAG5	frequencyTraceable	该位指定timePropertiesDS的frequencyTraceable成员的逻辑值。0：将frequencyTraceable设置为FALSE1：将frequencyTraceable设置为TRUE。	R/W
b7, b6	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b8	FLAG8	alternateMasterFlag	0：将alternateMasterFlag设置为FALSE1：将alternateMasterFlag设置为TRUE。	R/W
b9	—	Reserved	该位读取为0。写入值应为0。	R/W
b10	FLAG10	unicastFlag	0：将unicastFlag设置为FALSE1：将unicastFlag设置为TRUE。	R/W
b12, b11	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b13	FLAG13	PTP配置文件特定1	0：将PTP配置文件特定1设置为FALSE1：将PTP配置文件特定1设置为TRUE。	R/W
b14	FLAG14	PTP配置文件特定2	0：将PTP配置文件特定2设置为FALSE1：将PTP配置文件特定2设置为TRUE。	R/W
b31 to b15	—	Reserved	这些位被读取为0。写入值应为0。	R/W

当SYNFP模块要生成Announce消息时，ANFR寄存器指定标头的flagField部分。此寄存器中指定的值仅在SYRVLDR.ANUP位设置为1后反映在SYNFP模块中。

30.2.38 Sync Message Flag Field Setting Register (SYNFR)

Address(es): EPTPC0.SYNFR 4006 5854h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	FLAG14	FLAG13	—	—	FLAG10	FLAG9	FLAG8	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	FLAG8	alternateMasterFlag	0: Set alternateMasterFlag to FALSE 1: Set alternateMasterFlag to TRUE.	R/W
b9	FLAG9	twoStepFlag	Set this bit to 0 (FALSE).	R/W
b10	FLAG10	unicastFlag	0: Set unicastFlag to FALSE 1: Set unicastFlag to TRUE.	R/W
b12, b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b13	FLAG13	PTP profile Specific 1	0: Set PTP profile Specific 1 to FALSE 1: Set PTP profile Specific 1 to TRUE.	R/W
b14	FLAG14	PTP profile Specific 2	0: Set PTP profile Specific 2 to FALSE 1: Set PTP profile Specific 2 to TRUE.	R/W
b31 to b15	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The SYNFR register specifies the flagField section of the header when the SYNFP module is to generate a Sync message. The values specified in this register are only reflected in the SYNFP module after the SYRVLDR.STUP bit is set to 1.

30.2.39 Delay_Req Message Flag Field Setting Register (DYRQFR)

Address(es): EPTPC0.DYRQFR 4006 5858h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	FLAG14	FLAG13	—	—	FLAG10	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b9 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b10	FLAG10	unicastFlag	0: Set unicastFlag to FALSE 1: Set unicastFlag to TRUE.	R/W
b12, b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b13	FLAG13	PTP profile Specific 1	0: Set PTP profile Specific 1 to FALSE. 1: Set PTP profile Specific 1 to TRUE.	R/W

30.2.38 同步消息标志字段设置寄存器(SYNFR)

Address(es): EPTPC0.SYNFR 4006 5854h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	FLAG14	FLAG13	—	—	FLAG10	FLAG9	FLAG8	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b7 to b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b8	FLAG8	alternateMasterFlag	0：将alternateMasterFlag设置为FALSE1 ：将alternateMasterFlag设置为TRUE。	R/W
b9	FLAG9	twoStepFlag	将此位设置为0(FALSE)。	R/W
b10	FLAG10	unicastFlag	0：将unicastFlag设置为FALSE1 ：将unicastFlag设置为TRUE。	R/W
b12, b11	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b13	FLAG13	PTP配置文件特定1	0：将PTP配置文件特定1设置为FALSE1：将 PTP配置文件特定1设置为TRUE。	R/W
b14	FLAG14	PTP配置文件特定2	0：将PTP配置文件特定2设置为FALSE1：将 PTP配置文件特定2设置为TRUE。	R/W
b31 to b15	—	Reserved	这些位被读取为0。写入值应为0。	R/W

当SYNFP模块要生成同步消息时，SYNFR寄存器指定标头的flagField部分。此寄存器中指定的值仅在SYRVLDR.STUP位设置为1后反映在SYNFP模块中。

30.2.39 Delay_Req消息标志字段设置寄存器(DYRQFR)

Address(es): EPTPC0.DYRQFR 4006 5858h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	FLAG14	FLAG13	—	—	FLAG10	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b9 to b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b10	FLAG10	unicastFlag	0：将unicastFlag设置为FALSE1 ：将unicastFlag设置为TRUE。	R/W
b12, b11	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b13	FLAG13	PTP配置文件特定1	0：将PTP配置文件特定1设置为FALSE。1： 将PTP配置文件特定1设置为TRUE。	R/W

Bit	Symbol	Bit name	Description	R/W
b14	FLAG14	PTP profile Specific 2	0: Set PTP profile Specific 2 to FALSE. 1: Set PTP profile Specific 2 to TRUE.	R/W
b31 to b15	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The DYRQFR register specifies the flagField section of the header when the SYNFP module is to generate a Delay_Req or Pdelay_Req message. The values specified in this register are only reflected in the SYNFP module after the SYRVLDR.STUP bit is set to 1.

30.2.40 Delay_Resp Message Flag Field Setting Register (DYRPFR)

Address(es): EPTPC0.DYRPFR 4006 585Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	FLAG14	FLAG13	—	—	FLAG10	FLAG9	FLAG8	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	FLAG8	alternateMasterFlag*1	0: Set alternateMasterFlag to FALSE 1: Set alternateMasterFlag to TRUE.	R/W
b9	FLAG9	twoStepFlag*2	Set this bit to 0 (FALSE).	R/W
b10	FLAG10	unicastFlag	0: Set unicastFlag to FALSE 1: Set unicastFlag to TRUE.	R/W
b12, b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b13	FLAG13	PTP profile Specific 1	0: Set PTP profile Specific 1 to FALSE 1: Set PTP profile Specific 1 to TRUE.	R/W
b14	FLAG14	PTP profile Specific 2	0: Set PTP profile Specific 2 to FALSE 1: Set PTP profile Specific 2 to TRUE.	R/W
b31 to b15	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. This bit is reserved for Pdelay_Resp messages. Set the bit to 0.
Note 2. This bit is reserved for Delay_Resp messages.

The DYRPFR register specifies the flagField section of the header when the SYNFP module is to generate a Delay_Resp or Pdelay_Resp message. The values specified in this register are only reflected in the SYNFP module after the SYRVLDR.STUP bit is set to 1. Do not change the settings in this register while transmission of Delay_Resp or Pdelay_Resp messages is enabled. After disabling this transmission processing, do not change the settings in this register until the SYSR.RESDN flag sets to 1.

Bit	Symbol	位名称	Description	R/W
b14	FLAG14	PTP配置文件特定2	0：将PTP配置文件特定2设置为FALSE。1： 将PTP配置文件特定2设置为TRUE。	R/W
b31 to b15	—	Reserved	这些位被读取为0。写入值应为0。	R/W

当SYNFP模块要生成Delay_Req或Pdelay_Req消息时，DYRQFR寄存器指定标头的flagField部分。此寄存器中指定的值仅在SYRVLDR.STUP位设置为1后反映在SYNFP模块中。

30.2.40 Delay_Resp消息标志字段设置寄存器(DYRPFR)

Address(es): EPTPC0.DYRPFR 4006 585Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	FLAG14	FLAG13	—	—	FLAG10	FLAG9	FLAG8	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b7 to b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b8	FLAG8	alternateMasterFlag*1	0：将alternateMasterFlag设置为FALSE1 ：将alternateMasterFlag设置为TRUE。	R/W
b9	FLAG9	twoStepFlag*2	将此位设置为0(FALSE)。	R/W
b10	FLAG10	unicastFlag	0：将unicastFlag设置为FALSE1 ：将unicastFlag设置为TRUE。	R/W
b12, b11	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b13	FLAG13	PTP配置文件特定1	0：将PTP配置文件特定1设置为FALSE1：将 PTP配置文件特定1设置为TRUE。	R/W
b14	FLAG14	PTP配置文件特定2	0：将PTP配置文件特定2设置为FALSE1：将 PTP配置文件特定2设置为TRUE。	R/W
b31 to b15	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 该位为Pdelay_Resp消息保留。将该位设置为0。
Note 2. 该位为Delay_Resp消息保留。

当SYNFP模块要生成Delay_Resp或Pdelay_Resp消息时，DYRPFR寄存器指定标头的flagField部分。此寄存器中指定的值仅在SYRVLDR.STUP位设置为1后反映在SYNFP模块中。请勿在传输Delay_Resp或

Pdelay_Resp消息已启用。禁用此发送处理后，请勿更改此寄存器中的设置，直到SYSR.RESDN标志设置为1。

30.2.41 SYNFP Local Clock ID Register (SYCIDRU, SYCIDRL)

Address(es): EPTPC0.SYCIDRU 4006 5860h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b31 to b0	—	—	These bits specify the upper-order 32 bits of the clock-ID of the local port.	R/W

Address(es): EPTPC0.SYCIDRL 4006 5864h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b31 to b0	—	—	These bits specify the lower-order 32 bits of the clock-ID of the local port.	R/W

The SYCIDR register specifies the clock-ID of the local port. The clock-ID is used for the clockIdentity section in the sourcePortIdentity field of the header when the SYNFP module is to generate a PTP message. When a PTP message is received, the value in these registers is compared with the clockIdentity section in the sourcePortIdentity field of the PTP message to determine whether the message is one that was transmitted by your application. Renesas recommends making this setting the same as the value of portDS.portIdentity.clockIdentity in most cases.

Do not change the settings in these registers while reception or transmission of PTP messages is enabled.

30.2.41 SYNFP本地时钟ID寄存器(SYCIDRU SYCIDRL)

Address(es): EPTPC0.SYCIDRU 4006 5860h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b31 to b0	—	—	这些位指定本地端口时钟ID的高32位。	R/W

Address(es): EPTPC0.SYCIDRL 4006 5864h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b31 to b0	—	—	这些位指定本地端口时钟ID的低32位。	R/W

SYCIDR寄存器指定本地端口的时钟ID。当SYNFP模块要生成PTP消息时，clock-ID用于header的sourcePortIdentity字段中的clockIdentity部分。当接收到PTP消息时，会将这些寄存器中的值与PTP消息的sourcePortIdentity字段中的clockIdentity部分进行比较，以确定该消息是否是由您的应用程序发送的消息。Renesas建议在大多数情况下将此设置与portDS.portIdentity.clockIdentity的值相同。

当启用PTP消息的接收或发送时，请勿更改这些寄存器中的设置。

30.2.42 SYNFP Local Port Number Register (SYPNUMR)

Address(es): EPTPC0.SYPNUMR 4006 5868h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PNUM[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b15 to b0	PNUM[15:0]	Local Port Number Setting	These bits specify the port number of the local port.	R/W
b31 to b16	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The SYPNUMR register specifies the port number of the local port. This register is used for the portNumber section in the sourcePortIdentity field of the header when the SYNFP module is to generate a PTP message. When a PTP message is received, the value in this register is compared with the portNumber section in the sourcePortIdentity field of the PTP message to determine whether the message is one that was transmitted by the local device. Renesas recommends making this setting the same as the value of portDS.portIdentity.portNumber in most cases.

Do not change the settings in this register while reception or transmission of PTP messages is enabled.

30.2.43 SYNFP Register Value Load Directive Register (SYRVLDR)

Address(es): EPTPC0.SYRVLDR 4006 5880h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	ANUP	STUP	BMUP
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	BMUP	BMC Update	When this bit is set to 1, the SYNFP module simultaneously reflects values of registers storing the information that identifies MasterClock.	W
b1	STUP	State Update	When this bit is set to 1, the SYNFP module simultaneously reflects register values for PTP message reception and transmission.	W
b2	ANUP	Announce Message Generation Information Update	When this bit is set to 1, the Announce message generation block simultaneously reflects register values required for generating Announce messages.	W
b31 to b3	—	Reserved	The write value should be 0.	W

The SYRVLDR register simultaneously updates multiple register values in the SYNFP module.

BMUP bit (BMC Update)

When the BMUP bit is set to 1, the SYNFP module simultaneously reflects the values of the following registers that store the information that identifies MasterClock:

30.2.42 SYNFP本地端口号寄存器(SYPNUMR)

Address(es): EPTPC0.SYPNUMR 4006 5868h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PNUM[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b15 to b0	PNUM[15:0]	本地端口号设置	这些位指定本地端口的端口号。	R/W
b31 to b16	—	Reserved	这些位被读取为0。写入值应为0。	R/W

SYPNUMR寄存器指定本地端口的端口号。当SYNFP模块要生成PTP消息时，此寄存器用于标头的sourcePortIdentity字段中的portNumber部分。当接收到PTP消息时，将该寄存器中的值与PTP消息的sourcePortIdentity字段中的portNumber部分进行比较，以确定该消息是否是由本地设备发送的消息。Renesas建议在大多数情况下将此设置与portDS.portIdentity.portNumber的值相同。

当启用PTP消息的接收或发送时，请勿更改此寄存器中的设置。

30.2.43 SYNFP寄存器值加载指令寄存器(SYRVLDR)

Address(es): EPTPC0.SYRVLDR 4006 5880h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	ANUP	STUP	BMUP
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	BMUP	BMC Update	当该位设置为1时，SYNFP模块同时反映存储识别MasterClock信息的寄存器的值。	W
b1	STUP	状态更新	当该位设置为1时，SYNFP模块同时反映PTP消息接收和发送的寄存器值。	W
b2	ANUP	发布消息 代信息 Update	当该位设置为1时，Announce消息生成块同时反映生成Announce消息所需的寄存器值。	W
b31 to b3	—	Reserved	写入值应为0。	W

SYRVLDR寄存器同时更新SYNFP模块中的多个寄存器值。

BMUP位（BMC更新）

当BMUP位设置为1时，SYNFP模块同时反映以下存储识别MasterClock信息的寄存器的值：

- MTCIDU and MTCIDL registers
- MTPID register.

STUP bit (State Update)

When the STUP bit is set to 1, the SYNFP module simultaneously reflects the values of the following registers and bits for PTP message reception and transmission:

- SYNFR register
- DYRQFR register
- SYTLIR.DREQ[7:0] bits
- RSTOUTR register
- SYRFL1R register
- SYRFL2R register
- SYTRENR register.

ANUP bit (Announce Message Generation Information Update)

When the ANUP bit is set to 1, the Announce message generation block simultaneously reflects the values of the following registers and bits required for generating Announce messages:

- ANFR register
- SYTLIR.ANCE[7:0] bits
- GMPR register
- GMCQR register
- GMIDRU and GMIDRL registers
- CUOTSR register
- SRR register.

30.2.44 SYNFP Reception Filter Register 1 (SYRFL1R)

Address(es): EPTPC0.SYRFL1R 4006 5890h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	PDFUP2	—	PDFUP0	—	PDRP2	—	PDRP0	—	PDRQ2	—	PDRQ0	—	DRP2	—	DRP0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	DRQ2	—	DRQ0	—	FUP2	—	FUP0	—	SYNC2	—	SYNC0	—	—	—	ANCE0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	ANCE0	Announce Message Processing	0: Do not transfer messages to the PTPEDMAC 1: Transfer messages to the PTPEDMAC.	R/W
b3 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	SYNC0	Sync Message Processing	0: Do not transfer messages to the PTPEDMAC 1: Transfer messages to the PTPEDMAC.	R/W
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6	SYNC2	Sync Message Processing	0: Do not process messages in the SYNFP 1: Process messages in the SYNFP.	R/W

- MTCIDU和MTCIDL寄存器
- MTPID register.

STUP位（状态更新）

当STUP位设置为1时，SYNFP模块同时反映以下寄存器和位的值用于PTP消息的接收和发送：

- SYNFR register
- DYRQFR register
- SYTLIR.DREQ[7:0] bits
- RSTOUTR register
- SYRFL1R register
- SYRFL2R register
- SYTRENR register.

ANUP位（宣布消息生成信息更新）

当ANUP位设置为1时，Announce消息生成模块同时反映生成Announce消息所需的以下寄存器和位的值：

- ANFR register
- SYTLIR.ANCE[7:0] bits
- GMPR register
- GMCQR register
- GMIDRU和GMIDRL寄存器
- CUOTSR register
- SRR register.

30.2.44 SYNFP接收过滤器寄存器1(SYRFL1R)

Address(es): EPTPC0.SYRFL1R 4006 5890h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	PDFUP2	—	PDFUP0	—	PDRP2	—	PDRP0	—	PDRQ2	—	PDRQ0	—	DRP2	—	DRP0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	DRQ2	—	DRQ0	—	FUP2	—	FUP0	—	SYNC2	—	SYNC0	—	—	—	ANCE0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	ANCE0	宣布消息处理	0：不向PTPEDMAC传输消息1：向PTPEDMAC传输消息。	R/W
b3 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b4	SYNC0	同步消息处理	0：不向PTPEDMAC传输消息1：向PTPEDMAC传输消息。	R/W
b5	—	Reserved	该位读取为0。写入值应为0。	R/W
b6	SYNC2	同步消息处理	0：不处理SYNFP中的消息1：处理SYNFP中的消息。	R/W

Bit	Symbol	Bit name	Description	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b8	FUP0	Follow_Up Message Processing	0: Do not transfer messages to the PTPEDMAC 1: Transfer messages to the PTPEDMAC.	R/W
b9	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b10	FUP2	Follow_Up Message Processing	0: Do not process messages in the SYNFP 1: Process messages in the SYNFP.	R/W
b11	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b12	DRQ0	Delay_Req Message Processing	0: Do not transfer messages to the PTPEDMAC 1: Transfer messages to the PTPEDMAC.	R/W
b13	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b14	DRQ2	Delay_Req Message Processing	0: Do not process messages in the SYNFP 1: Process messages in the SYNFP.	R/W
b15	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b16	DRP0	Delay_Resp Message Processing	0: Do not transfer messages to the PTPEDMAC 1: Transfer messages to the PTPEDMAC.	R/W
b17	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b18	DRP2	Delay_Resp Message Processing	0: Do not process messages in the SYNFP 1: Process messages in the SYNFP.	R/W
b19	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b20	PDRQ0	Pdelay_Req Message Processing	0: Do not transfer messages to the PTPEDMAC 1: Transfer messages to the PTPEDMAC.	R/W
b21	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b22	PDRQ2	Pdelay_Req Message Processing	0: Do not process messages in the SYNFP 1: Process messages in the SYNFP.	R/W
b23	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b24	PDRP0	Pdelay_Resp Message Processing	0: Do not transfer messages to the PTPEDMAC 1: Transfer messages to the PTPEDMAC.	R/W
b25	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b26	PDRP2	Pdelay_Resp Message Processing	0: Do not process messages in the SYNFP 1: Process messages in the SYNFP.	R/W
b27	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b28	PDFUP0	Pdelay_Resp_Follow_Up Message Processing	0: Do not transfer messages to the PTPEDMAC 1: Transfer messages to the PTPEDMAC.	R/W
b29	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b30	PDFUP2	Pdelay_Resp_Follow_Up Message Processing	0: Do not process messages in the SYNFP 1: Process messages in the SYNFP.	R/W
b31	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

The SYRFL1R register specifies filtering for the reception of PTP messages. Multiple bits corresponding to different types of messages can be set to 1. Setting all bits for a type of message to 0 leads to all messages of the given type being discarded. The values specified in this register are only reflected in the SYNFP module after the SYRVLDR.STUP bit is set to 1.

Bit	Symbol	位名称	Description	R/W
b7	—	Reserved	该位读取为0。写入值应为0。	R/W
b8	FUP0	Follow_Up消息处理	0：不向PTPEDMAC传输消息1：向PTPEDMAC传输消息。	R/W
b9	—	Reserved	该位读取为0。写入值应为0。	R/W
b10	FUP2	Follow_Up消息处理	0：不处理SYNFP中的消息1：处理SYNFP中的消息。	R/W
b11	—	Reserved	该位读取为0。写入值应为0。	R/W
b12	DRQ0	Delay_Req消息处理	0：不向PTPEDMAC传输消息1：向PTPEDMAC传输消息。	R/W
b13	—	Reserved	该位读取为0。写入值应为0。	R/W
b14	DRQ2	Delay_Req消息处理	0：不处理SYNFP中的消息1：处理SYNFP中的消息。	R/W
b15	—	Reserved	该位读取为0。写入值应为0。	R/W
b16	DRP0	Delay_Resp消息处理	0：不向PTPEDMAC传输消息1：向PTPEDMAC传输消息。	R/W
b17	—	Reserved	该位读取为0。写入值应为0。	R/W
b18	DRP2	Delay_Resp消息处理	0：不处理SYNFP中的消息1：处理SYNFP中的消息。	R/W
b19	—	Reserved	该位读取为0。写入值应为0。	R/W
b20	PDRQ0	Pdelay_Req消息处理	0：不向PTPEDMAC传输消息1：向PTPEDMAC传输消息。	R/W
b21	—	Reserved	该位读取为0。写入值应为0。	R/W
b22	PDRQ2	Pdelay_Req消息处理	0：不处理SYNFP中的消息1：处理SYNFP中的消息。	R/W
b23	—	Reserved	该位读取为0。写入值应为0。	R/W
b24	PDRP0	Pdelay_Resp消息处理	0：不向PTPEDMAC传输消息1：向PTPEDMAC传输消息。	R/W
b25	—	Reserved	该位读取为0。写入值应为0。	R/W
b26	PDRP2	Pdelay_Resp消息处理	0：不处理SYNFP中的消息1：处理SYNFP中的消息。	R/W
b27	—	Reserved	该位读取为0。写入值应为0。	R/W
b28	PDFUP0	Pdelay_Resp_Follow_Up Message Processing	0：不向PTPEDMAC传输消息1：向PTPEDMAC传输消息。	R/W
b29	—	Reserved	该位读取为0。写入值应为0。	R/W
b30	PDFUP2	Pdelay_Resp_Follow_Up Message Processing	0：不处理SYNFP中的消息1：处理SYNFP中的消息。	R/W
b31	—	Reserved	该位读取为0。写入值应为0。	R/W

SYRFL1R寄存器指定对PTP消息接收的过滤。可以将对应于不同类型消息的多个位设置为1。将一种消息类型的所有位设置为0会导致给定类型的所有消息都被丢弃。此寄存器中指定的值仅在SYRVLDR.STUP位设置为1后反映在SYNFP模块中。

30.2.45 SYNFP Reception Filter Register 2 (SYRFL2R)

Address(es): EPTPC0.SYRFL2R 4006 5894h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	ILL0	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	SIG0	—	—	—	MAN0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	MAN0	Management Message Processing Setting	0: Do not transfer messages to the PTPEDMAC 1: Transfer messages to the PTPEDMAC.	R/W
b3 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	SIG0	Signaling Message Processing Setting	0: Do not transfer messages to the PTPEDMAC 1: Transfer messages to the PTPEDMAC.	R/W
b27 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b28	ILL0	Illegal Message Processing Setting*1	0: Do not transfer messages to the PTPEDMAC 1: Transfer messages to the PTPEDMAC.	R/W
b31 to b29	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. PTP messages other than PTP v2 messages and messages of undefined type are handled as illegal messages.

The SYRFL2R register specifies filtering for the reception of PTP messages. Multiple bits corresponding to different types of messages can be set to 1. Setting all bits for a type of message to 0 leads to all messages of the given type being discarded. The values specified in this register are only reflected in the SYNFP module after the SYRVLDR.STUP bit is set to 1.

30.2.46 SYNFP Transmission Enable Register (SYTRENR)

Address(es): EPTPC0.SYTRENR 4006 5898h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	PDRQ	—	—	—	DRQ	—	—	—	SYNC	—	—	—	ANCE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	ANCE	Announce Message Transmission Enable	0: Do not transmit Announce messages 1: Transmit Announce messages.	R/W
b3 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	SYNC	Sync Message Transmission Enable	0: Do not transmit Sync messages 1: Transmit Sync messages.	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	DRQ	Delay_Req Message Transmission Enable	0: Do not transmit Delay_Req messages 1: Transmit Delay_Req messages.	R/W

30.2.45 SYNFP接收过滤器寄存器2(SYRFL2R)

Address(es): EPTPC0.SYRFL2R 4006 5894h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	ILL0	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	SIG0	—	—	—	MAN0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	MAN0	管理讯息 加工设定	0：不向PTPEDMAC传输消息1：向PTPEDMAC 传输消息。	R/W
b3 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b4	SIG0	信令消息处理设置	0：不向PTPEDMAC传输消息1：向PTPEDMAC 传输消息。	R/W
b27 to b5	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b28	ILL0	非法消息处理 Setting*1	0：不向PTPEDMAC传输消息1：向PTPEDMAC 传输消息。	R/W
b31 to b29	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. PTPv2消息以外的PTP消息和未定义类型的消息将作为非法消息处理。

SYRFL2R寄存器指定过滤PTP消息的接收。可以将对应于不同类型消息的多个位设置为1。将一种消息类型的所有位设置为0会导致给定类型的所有消息都被丢弃。此寄存器中指定的值仅在SYRVLDR.STUP位设置为1后反映在SYNFP模块中。

30.2.46 SYNFP传输使能寄存器(SYTRENR)

Address(es): EPTPC0.SYTRENR 4006 5898h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	PDRQ	—	—	—	DRQ	—	—	—	SYNC	—	—	—	ANCE
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	ANCE	宣布消息传输启用	0：不发送Announce消息1：发送Anno unce消息。	R/W
b3 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b4	SYNC	同步消息传输 Enable	0：不发送同步消息1：发送同步消 息。	R/W
b7 to b5	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b8	DRQ	Delay_Req消息传输 使能	0：不发送Delay_Req消息1：发送Delay_ Req消息。	R/W

Bit	Symbol	Bit name	Description	R/W
b11 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b12	PDRQ	Pdelay_Req Message Transmission Enable	0: Do not transmit Pdelay_Req messages 1: Transmit Pdelay_Req messages.	R/W
b31 to b13	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The SYTRENR register enables or disables transmission of PTP messages. Do not set the PDRQ and DRQ bits to 1 at the same time. Operation is not guaranteed when both bits are set to 1. The values specified in this register are only reflected in the SYNFP module after the SYRVLDR.STUP bit is set to 1.

30.2.47 Master Clock ID Register (MTCIDU, MTCIDL)

Address(es): EPTPC0.MTCIDU 4006 58A0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b31 to b0	—	—	These bits specify the upper-order 32 bits of the clock-ID of the master clock.	R/W

Address(es): EPTPC0.MTCIDL 4006 58A4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b31 to b0	—	—	These bits specify the lower-order 32 bits of the clock-ID of the master clock.	R/W

The MTCIDU and MTCIDL registers specify the clock-ID of the master clock for synchronization. The value specified in these registers is only reflected in the SYNFP module after the SYRVLDR.BMUP bit is set to 1.

Bit	Symbol	位名称	Description	R/W
b11 to b9	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b12	PDRQ	Pdelay_Req Message 传输使能	0：不发送Pdelay_Req消息1：发送Pdelay _Req消息。	R/W
b31 to b13	—	Reserved	这些位被读取为0。写入值应为0。	R/W

SYTRENR寄存器启用或禁用PTP消息的传输。不要同时将PDRQ和DRQ位设置为1。当两个位都设置为1时，不能保证操作。此寄存器中指定的值仅在SYRVLDR.STUP位设置为1后反映在SYNFP模块中。

30.2.47 主时钟ID寄存器(MTCIDU MTCIDL)

Address(es): EPTPC0.MTCIDU 4006 58A0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b31 to b0	—	—	这些位指定主时钟的时钟ID的高32位。	R/W

Address(es): EPTPC0.MTCIDL 4006 58A4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b31 to b0	—	—	这些位指定主时钟的时钟ID的低32位。	R/W

MTCIDU和MTCIDL寄存器指定用于同步的主时钟的时钟ID。这些寄存器中指定的值仅在SYRVLDR.BMUP位设置为1后反映在SYNFP模块中。

30.2.48 Master Clock Port Number Register (MTPID)

Address(es): EPTPC0.MTPID 4006 58A8h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PNUM[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b15 to b0	PNUM[15:0]	Master Clock Port Number Setting	These bits specify the port number of the master clock.	R/W
b31 to b16	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The MTPID register specifies the port number of the master clock for synchronization. The value specified in this register is only reflected in the SYNFP module after the SYRVLDR.BMUP bit is set to 1. In normal usage, set the value of parentDS.parentPortIdentity.portNumber in this register.

30.2.49 SYNFP Transmission Interval Setting Register (SYTLIR)

Address(es): EPTPC0.SYTLIR 4006 58C0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	DREQ[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SYNC[7:0]								ANCE[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Bit name	Description	R/W
b7 to b0	ANCE[7:0]	Announce Message Transmission Interval Setting	These bits set the interval for the transmission of Announce messages.	R/W
b15 to b8	SYNC[7:0]	Sync Message Transmission Interval Setting	These bits set the interval for the transmission of Sync messages. The setting is also placed in the logMessageInterval field of transmitted Sync messages.	R/W
b23 to b16	DREQ[7:0]	Delay_Req Transmission Interval Average Value/ Pdelay_Req Transmission Interval Setting	The bits set the average interval for the transmission of Delay_Req messages and the interval for the transmission of Pdelay_Req messages.The setting is also placed in the logMessageInterval field of Delay_Resp messages.	R/W
b31 to b24	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The SYTLIR register specifies the interval for the transmission of messages generated by the SYNFP module. The setting is an integer logarithm in base 2 (log2(x)) and determines a value x in seconds. In other words, the interval for transmission is 2^n (s), where n is the setting. The available settings are from -7 (F9h) to +6 (06h).

Examples:

- If the setting is 06h, then the interval for transmission is $2^6 = 64$ (s)
- If the setting is 00h, then the interval for transmission is $2^0 = 1$ (s)

30.2.48 主时钟端口号寄存器(MTPID)

Address(es): EPTPC0.MTPID 4006 58A8h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PNUM[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b15 to b0	PNUM[15:0]	主时钟端口号 Setting	这些位指定主时钟的端口号。	R/W
b31 to b16	—	Reserved	这些位被读取为0。写入值应为0。	R/W

MTPID寄存器指定用于同步的主时钟的端口号。此寄存器中指定的值仅在SYRVLDR.BMUP位设置为1后反映在SYNFP模块中。正常使用时，设置此寄存器中parentDS.parentPortIdentity.portNumber的值。

30.2.49 SYNFP传输间隔设置寄存器(SYTLIR)

Address(es): EPTPC0.SYTLIR 4006 58C0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	DREQ[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SYNC[7:0]								ANCE[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	位名称	Description	R/W
b7 to b0	ANCE[7:0]	发布消息 传输间隔设置	这些位设置Announce消息的传输间隔。	R/W
b15 to b8	SYNC[7:0]	同步消息传输 间隔设置	这些位设置同步消息的传输间隔。该设置也放置在传输的同步消息的logMessageInterval字段中。	R/W
b23 to b16	DREQ[7:0]	Delay_Req传输间隔平均值 Pdelay_Req Transmission 间隔设置	这些位设置传输延迟请求消息的平均间隔和传输的间隔 Pdelay_Req消息。该设置也放置在Delay_Resp消息的log MessageInterval字段中。	R/W
b31 to b24	—	Reserved	这些位被读取为0。写入值应为0。	R/W

SYTLIR寄存器指定传输由SYNFP模块生成的消息的时间间隔。该设置是一个以2为底的整数对数(log2(x))，并以秒为单位确定值x。换言之，传输的间隔是2n(s)，其中n是设置。可用设置从-7(F9h)到+6(06h)。

Examples:

- 如果设置为06h，则传输间隔为26=64(s)
- 如果设置为00h，则传输间隔为20=1(s)

- If the setting is FFh, then the interval for transmission is 2^{-1} = 0.5 (s) = 500 (ms)
- If the setting is F9h, then the interval for transmission is 2^{-7} = 0.0078125 (s) = 7.8125 (ms).

The value specified in the ANCE[7:0] bits is only reflected in the SYNFP module after the SYRVLDR.ANUP bit is set to 1. The values specified in the DREQ[7:0] and SYNC[7:0] bits are only reflected in the SYNFP module after the SYRVLDR.STUP bit is set to 1.

30.2.50 SYNFP Received logMessageInterval Value Indication Register (SYRLIR)

Address(es): EPTPC0.SYRLIR 4006 58C4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	DRESP[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SYNC[7:0]								ANCE[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	ANCE[7:0]	Announce Message logMessageInterval Field Indication Flag	These bits indicate the logMessageInterval field value of a received Announce message.	R
b15 to b8	SYNC[7:0]	Sync Message logMessageInterval Field Indication Flag	These bits indicate the logMessageInterval field value of a received Sync message.	R
b23 to b16	DRESP[7:0]	Delay_Resp Message logMessageInterval Field Indication Flag	These bits indicate the logMessageInterval field value of a received Delay_Resp message.	R
b31 to b24	—	Reserved	These bits are read as 0.	R

The SYRLIR register indicates the logMessageInterval field values of received PTP messages.

30.2.51 offsetFromMaster Value Register (OFMRU, OFMRL)

Address(es): EPTPC0.OFMRU 4006 58C8h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b31 to b0	—	—	These bits indicate the upper-order 32 bits of the calculated offsetFromMaster value.	R

- 如果设置为FFh，则传输间隔为2−1=0.5(s)=500(ms)
- 如果设置为F9h，则传输间隔为2−7=0.0078125(s)=7.8125(ms)。

ANCE[7:0]位中指定的值仅在SYRVLDR.ANUP位设置为1后反映在SYNFP模块中。DREQ[7:0]和SYNC[7:0]位中指定的值是仅在SYRVLDR.STUP位设置为1后反映在SYNFP模块中。

30.2.50 SYNFP接收到的logMessageInterval值指示寄存器(SYRLIR)

Address(es): EPTPC0.SYRLIR 4006 58C4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	DRESP[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SYNC[7:0]								ANCE[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b7 to b0	ANCE[7:0]	公告消息logMessageInterval字段指示标志	这些位指示接收到的Announce消息的logMessageInterval字段值。	R
b15 to b8	SYNC[7:0]	同步消息logMessageInterval字段指示标志	这些位指示接收到的同步消息的logMessageInterval字段值。	R
b23 to b16	DRESP[7:0]	Delay_Resp消息logMessageInterval字段指示标志	这些位指示接收到的Delay_Resp消息的logMessageInterval字段值。	R
b31 to b24	—	Reserved	这些位读为0。	R

SYRLIR寄存器指示接收到的PTP消息的logMessageInterval字段值。

30.2.51 offsetFromMaster值寄存器(OFMRU OFMRL)

Address(es): EPTPC0.OFMRU 4006 58C8h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b31 to b0	—	—	这些位指示计算出的offsetFromMaster值的高32位。	R

Address(es): EPTPC0.OFMRL 4006 58CCh

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b31 to b0	—	—	These bits indicate the lower-order 32 bits of the calculated offsetFromMaster value.	R

The OFMRU and OFMRL registers indicate the calculated offsetFromMaster value. The value is expressed as a two's complement in nanoseconds. The numeric representation differs from that of the offsetFromMaster member of the current data set (currentDS), as shown in the following note. For reads, access the registers in the order of OFMRU, OFMRL.

Note 1. The value of currentDS.offsetFromMaster is multiplied by 2^{16}. Example: 2.5 (ns) = 0000_0000_0002_8000h

30.2.52 meanPathDelay Value Register (MPDRU, MPDRL)

Address(es): EPTPC0.MPDRU 4006 58D0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b31 to b0	—	—	These bits indicate the upper-order 32 bits of the calculated meanPathDelay value.	R

Address(es): EPTPC0.MPDRL 4006 58D4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Address(es): EPTPC0.OFMRL 4006 58CCh

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b31 to b0	—	—	这些位指示计算出的offsetFromMaster值的低32位。	R

OFMRU和OFMRL寄存器指示计算出的offsetFromMaster值。该值表示为以纳秒为单位的二进制补码。数字表示与当前数据集(currentDS)的offsetFromMaster成员的表示不同，如下面的注释所示。对于读取，按OFMRU、OFMRL的顺序访问寄存器。

注1.currentDS.offsetFromMaster的值乘以216。示例：2.5(ns)=0000_0000_0002_8000h

30.2.52 meanPathDelay值寄存器(MPDRU MPDRL)

Address(es): EPTPC0.MPDRU 4006 58D0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b31 to b0	—	—	这些位表示计算出的meanPathDelay值的高32位。	R

Address(es): EPTPC0.MPDRL 4006 58D4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b31 to b0	—	—	These bits indicate the lower-order 32 bits of the calculated meanPathDelay value.	R

The MPDRU and MPDRL registers indicate the calculated meanPathDelay value. The value is expressed as a two's complement in nanoseconds. The numeric representation differs from that of the meanPathDelay member of the current data set (currentDS), as shown in the following note. For reads, access the registers in the order of MPDRU, MPDRL.

Note 1. The value of currentDS.meanPathDelay is multiplied by 2^{16}. Example: 2.5 (ns) = 0000_0000_0002_8000h

30.2.53 grandmasterPriority Field Setting Register (GMPR)

Address(es): EPTPC0.GMPR 4006 58E0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	GMPR1[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	GMPR2[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	GMPR2[7:0]	grandmasterPriority2 Field Value Setting	These bits specify the value of the grandmasterPriority2 fields of Announce messages.	R/W
b15 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b23 to b16	GMPR1[7:0]	grandmasterPriority1 Field Value Setting	These bits specify the value of the grandmasterPriority1 fields of Announce messages.	R/W
b31 to b24	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The GMPR register specifies the grandmasterPriority1 and grandmasterPriority2 field values of Announce messages generated by the SYNFP module. The values specified in this register are only reflected in the SYNFP module after the SYRVLDR.ANUP bit is set to 1.

Bit	Symbol	位名称	Description	R/W
b31 to b0	—	—	这些位表示计算出的meanPathDelay值的低32位。	R

MPDRU和MPDRL寄存器指示计算出的meanPathDelay值。该值表示为以纳秒为单位的二进制补码。数字表示与当前数据集(currentDS)的meanPathDelay成员的表示不同，如下面的注释所示。对于读取，按MPDRU、MPDRL的顺序访问寄存器。

注1.currentDS.meanPathDelay的值乘以216。示例：2.5(ns)=0000_0000_0002_8000h

30.2.53 grandmasterPriority字段设置寄存器(GMPR)

Address(es): EPTPC0.GMPR 4006 58E0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	GMPR1[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	GMPR2[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b7 to b0	GMPR2[7:0]	grandmasterPriority2字段值设置	这些位指定GrandmasterPriority2字段的值发布消息。	R/W
b15 to b8	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b23 to b16	GMPR1[7:0]	grandmasterPriority1字段值设置	这些位指定GrandmasterPriority1字段的值发布消息。	R/W
b31 to b24	—	Reserved	这些位被读取为0。写入值应为0。	R/W

GMPR寄存器指定SYNFP模块生成的Announce消息的grandmasterPriority1和grandmasterPriority2字段值。此寄存器中指定的值仅在SYRVLDR.ANUP位设置为1后反映在SYNFP模块中。

30.2.54 grandmasterClockQuality Field Setting Register (GMCQR)

Address(es): EPTPC0.GMCQR 4006 58E4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b31 to b0	—	—	These bits specify the value of the grandmasterClockQuality fields of Announce messages. The associations between bits and the grandmasterClockQuality fields is as follows: b31 to b24: clockClass b23 to b16: clockAccuracy b15 to b0: offsetScaledLogVariance.	R/W

The GMCQR register specifies the grandmasterClockQuality field value of Announce messages generated by the SYNFP module. The value specified in the GMCQR register is only reflected in the SYNFP module after the SYRVLDR.ANUP bit is set to 1.

30.2.55 grandmasterIdentity Field Setting Register (GMIDRU, GMIDRL)

Address(es): EPTPC0.GMIDRU 4006 58E8h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b31 to b0	—	—	These bits specify the upper-order 32 bits of the value of the grandmasterIdentity fields of Announce messages.	R/W

Address(es): EPTPC0.GMIDRL 4006 58ECh

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

30.2.54 grandmasterClockQuality字段设置寄存器(GMCQR)

Address(es): EPTPC0.GMCQR 4006 58E4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b31 to b0	—	—	这些位指定Announce消息的grandmasterClockQuality字段的值。位和grandmasterClockQuality字段之间的关联如下：b31到b24：clockClassb23到b16：clockAccuracyb15到b0：offsetScaledLogVariance。	R/W

GMCQR寄存器指定由Announce消息生成的grandmasterClockQuality字段值SYNFP模块。GMCQR寄存器中指定的值仅在SYNFP模块中反映SYRVLDR.ANUP位设置为1。

30.2.55 grandmasterIdentity字段设置寄存器(GMIDRU GMIDRL)

Address(es): EPTPC0.GMIDRU 4006 58E8h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b31 to b0	—	—	这些位指定Announce消息的grandmasterIdentity字段值的高32位。	R/W

Address(es): EPTPC0.GMIDRL 4006 58ECh

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b31 to b0	—	—	These bits specify the lower-order 32 bits of the value of the grandmasterIdentity fields of Announce messages.	R/W

The GMIDRU and GMIDRL registers specify the grandmasterIdentity field value of Announce messages generated by the SYNFP module. The value specified in these registers is only reflected in the SYNFP module after the SYRVLDR.ANUP bit is set to 1.

30.2.56 currentUtcOffset/timeSource Field Setting Register (CUOTSR)

Address(es): EPTPC0.CUOTSR 4006 58F0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	CUTO[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	TSRC[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	TSRC[7:0]	timeSource Field Setting	These bits specify the value of the timeSource fields of Announce messages.	R/W
b15 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b31 to b16	CUTO[15:0]	currentUtcOffset Field Setting	These bits specify the value of the currentUtcOffset fields of Announce messages.	R/W

The CUOTSR register specifies the currentUtcOffset and timeSource field values of Announce messages generated by the SYNFP module. The values specified in this register are only reflected in the SYNFP module after the SYRVLDR.ANUP bit is set to 1.

30.2.57 stepsRemoved Field Setting Register (SRR)

Address(es): EPTPC0.SRR 4006 58F4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SRMV[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b15 to b0	SRMV[15:0]	stepsRemoved Field Value Setting	These bits specify the value of the stepsRemoved fields of Announce messages.	R/W
b31 to b16	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The SRR register specifies the stepsRemoved field value of Announce messages generated by the SYNFP module. The value specified in this register is only reflected in the SYNFP module after the SYRVLDR.ANUP bit is set to 1.

Bit	Symbol	位名称	Description	R/W
b31 to b0	—	—	这些位指定Announce消息的grandmasterIdentity字段值的低32位。	R/W

GMIDRU和GMIDRL寄存器指定SYNFP模块生成的Announce消息的grandmasterIdentity字段值。这些寄存器中指定的值仅在SYRVLDR.ANUP位设置为1后反映在SYNFP模块中。

30.2.56 currentUtcOffsettimeSource字段设置寄存器(CUOTSR)

Address(es): EPTPC0.CUOTSR 4006 58F0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	CUTO[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	TSRC[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b7 to b0	TSRC[7:0]	timeSource字段设置	这些位指定Announce消息的timeSource字段的值。	R/W
b15 to b8	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b31 to b16	CUTO[15:0]	currentUtcOffset字段设置	这些位指定的currentUtcOffset字段的值发布消息。	R/W

CUOTSR寄存器指定SYNFP模块生成的Announce消息的currentUtcOffset和timeSource字段值。此寄存器中指定的值仅在SYRVLDR.ANUP位设置为1后反映在SYNFP模块中。

30.2.57 stepsRemoved字段设置寄存器(SRR)

Address(es): EPTPC0.SRR 4006 58F4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SRMV[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b15 to b0	SRMV[15:0]	stepsRemoved字段值设置	这些位指定stepsRemoved字段的值发布消息。	R/W
b31 to b16	—	Reserved	这些位被读取为0。写入值应为0。	R/W

SRR寄存器指定SYNFP模块生成的Announce消息的stepsRemoved字段值。该寄存器中指定的值仅在SYRVLDR.ANUP位设置为1后反映在SYNFP模块中。

30.2.58 PTP-primary Message Destination MAC Address Setting Register (PPMACRU, PPMACRL)

Address(es): EPTPC0.PPMACRU 4006 5900h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	1	1	0	1	1	0	0	0	1	1	0	0	1

Bit	Symbol	Bit name	Description	R/W
b23 to b0	—	—	These bits specify the upper-order 24 bits of the destination MAC address for PTP-primary messages.	R/W
b31 to b24	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Address(es): EPTPC0.PPMACRL 4006 5904h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b23 to b0	—	—	These bits specify the lower-order 24 bits of the destination MAC address for PTP-primary messages.	R/W
b31 to b24	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The PPMACRU and PPMACRL registers specify the destination MAC address for PTP-primary messages. In normal usage, set 01:1B:19:00:00:00 in these registers. The value is used in the destination MAC address field when generating an Ethernet frame for a PTP-primary message. It is also used as a determining condition for received frames carrying PTP messages. Set these registers before starting the EDMAC, ETHERC, or PTPEDMAC. Do not change the settings while the EPTPC is operating.

30.2.58 PTP-primaryMessageDestinationMACAddressSettingRegister(PPMACRU PPMACRL)

Address(es): EPTPC0.PPMACRU 4006 5900h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—								
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值:	0	0	0	1	1	0	1	1	0	0	0	1	1	0	0	1

Bit	Symbol	位名称	Description	R/W
b23 to b0	—	—	这些位指定目标的高24位 PTP主要消息的MAC地址。	R/W
b31 to b24	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Address(es): EPTPC0.PPMACRL 4006 5904h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—								
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b23 to b0	—	—	这些位指定目标的低24位 PTP主要消息的MAC地址。	R/W
b31 to b24	—	Reserved	这些位被读取为0。写入值应为0。	R/W

PPMACRU和PPMACRL寄存器指定PTP主要消息的目标MAC地址。在正常使用中，在这些寄存器中设置01:1B:19:00:00:00。当为PTP主要消息生成以太网帧时，该值用于目标MAC地址字段。它也被用作接收帧携带PTP消息的确定条件。在启动EDMAC、ETHERC或PTPEDMAC之前设置这些寄存器。请勿在EPTPC运行时更改设置。

30.2.59 PTP-pdelay Message MAC Address Setting Register (PDMACRU, PDMACRL)

Address(es): EPTPC0.PDMACRU 4006 5908h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	0	0	0	0	0	0	0	1	1	0	0	0	0	1	0

Bit	Symbol	Bit name	Description	R/W
b23 to b0	—	—	These bits specify the upper-order 24 bits of the destination MAC address for PTP-pdelay messages.	R/W
b31 to b24	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Address(es): EPTPC0.PDMACRL 4006 590Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0

Bit	Symbol	Bit name	Description	R/W
b23 to b0	—	—	These bits specify the lower-order 24 bits of the destination MAC address for PTP-pdelay messages.	R/W
b31 to b24	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The PDMACRU and PDMACRL registers specify the destination MAC address for PTP-pdelay messages. In normal usage, set 01:80:C2:00:00:0E in these registers. This value is used in the destination MAC address field when generating frames carrying PTP-pdelay messages in the Ethernet format. It is also used as a determining condition for received frames carrying PTP messages. Set these registers before starting the EDMAC, ETHERC, or PTPEDMAC. Do not change the settings while the EPTPC is operating.

30.2.59 PTP-pdelay消息MAC地址设置寄存器(PDMACRU PDMACRL)

Address(es): EPTPC0.PDMACRU 4006 5908h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—								
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值:	1	0	0	0	0	0	0	0	1	1	0	0	0	0	1	0

Bit	Symbol	位名称	Description	R/W
b23 to b0	—	—	这些位指定目标的高24位 PTP-pdelay消息的MAC地址。	R/W
b31 to b24	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Address(es): EPTPC0.PDMACRL 4006 590Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—								
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0

Bit	Symbol	位名称	Description	R/W
b23 to b0	—	—	这些位指定目标的低24位 PTP-pdelay消息的MAC地址。	R/W
b31 to b24	—	Reserved	这些位被读取为0。写入值应为0。	R/W

PDMACRU和PDMACRL寄存器指定PTP-pdelay消息的目标MAC地址。在正常使用中，在这些寄存器中设置01:80:C2:00:00:0E。当生成携带以太网格式的PTP-pdelay消息的帧时，此值用于目标MAC地址字段。它也被用作接收帧携带PTP消息的确定条件。在启动EDMAC、ETHERC或PTPEDMAC之前设置这些寄存器。请勿在EPTPC运行时更改设置。

30.2.60 PTP Message Ethertype Setting Register (PETYPER)

Address(es): EPTPC0.PETYPER 4006 5910h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TYPE[15:0]															
Value after reset:	1	0	0	0	1	0	0	0	1	1	1	1	0	1	1	1

Bit	Symbol	Bit name	Description	R/W
b15 to b0	TYPE[15:0]	PTP Message Ethertype Value Setting	These bits specify the Ethertype field value for frames in the Ethernet II format.	R/W
b31 to b16	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The PETYPER register specifies the Ethertype field for frames carrying the PTP messages. In normal usage, set 0000_88F7h in this register. This value is used in the Ethertype field when generating frames carrying PTP messages in the Ethernet II format. It is also used as a determining condition for received frames carrying PTP messages. Set these registers before starting the EDMAC, ETHERC, or PTPEDMAC. Do not change the settings while the EPTPC is operating.

30.2.61 PTP-primary Message Destination IP Address Setting Register (PPIPR)

Address(es): EPTPC0.PPIPR 4006 5920h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1

Bit	Symbol	Bit name	Description	R/W
b31 to b0	—	—	These bits specify the destination IP address for PTP-primary messages.	R/W

The PPIPR register specifies the destination IP address for PTP messages. In normal usage, set E000_0181h (224.0.1.129) in this register. This value is used in the destination IP address field when generating frames carrying PTP-primary messages in the IPv4 format. The lower-order 23 bits are also used in the destination MAC address field for Ethernet frames. The value is also used as a determining condition for received frames carrying PTP messages. Set this register before starting the EDMAC, ETHERC, or PTPEDMAC. Do not change the settings while the EPTPC is operating.

30.2.60 PTP消息以太网类型设置寄存器(PETYPER)

Address(es): EPTPC0.PETYPER 4006 5910h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TYPE[15:0]															
重置后的值:	1	0	0	0	1	0	0	0	1	1	1	1	0	1	1	1

Bit	Symbol	位名称	Description	R/W
b15 to b0	TYPE[15:0]	PTP消息以太网类型值 Setting	这些位指定Ethertype字段值的帧在以太网II格式。	R/W
b31 to b16	—	Reserved	这些位被读取为0。写入值应为0。	R/W

PETYPER寄存器为携带PTP消息的帧指定Ethertype字段。正常使用时，在该寄存器中设置0000_88F7h。当生成携带以太网II格式的PTP消息的帧时，该值用于Ethertype字段。它也被用作接收帧携带PTP消息的确定条件。在启动EDMAC、ETHERC或PTPEDMAC之前设置这些寄存器。请勿在EPTPC运行时更改设置。

30.2.61 PTP-primaryMessageDestinationIPAddressSettingRegister(PPIPR)

Address(es): EPTPC0.PPIPR 4006 5920h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值:	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值:	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0	1

Bit	Symbol	位名称	Description	R/W
b31 to b0	—	—	这些位指定PTP主要消息的目标IP地址。	R/W

PPIPR寄存器指定PTP消息的目标IP地址。正常使用时，在此寄存器中设置E000_0181h(224.0.1.129)。当生成携带IPv4格式的PTPprimary消息的帧时，此值用于目标IP地址字段。低23位也用于以太网帧的目标MAC地址字段。该值也作为接收帧携带PTP消息的判断条件。在启动EDMAC、ETHERC或PTPEDMAC之前设置该寄存器。请勿在EPTPC运行时更改设置。

30.2.62 PTP-pdelay Message Destination IP Address Setting Register (PDIPR)

Address(es): EPTPC0.PDIPR 4006 5924h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	1	1	0	1	0	1	1

Bit	Symbol	Bit name	Description	R/W
b31 to b0	—	—	These bits specify the destination IP address for PTP-pdelay messages.	R/W

The PDIPR register specifies the destination IP address for PTP-pdelay messages. In normal usage, set E000_006Bh (224.0.0.107) in this register. The value is used in the destination IP address field when generating frames carrying PTP-pdelay messages in the IPv4 format. The lower-order 23 bits are also used in the destination MAC address field for Ethernet frames. The value is also used as a determining condition for received frames carrying PTP messages. Set this register before starting the EDMAC, ETHERC, or PTPEDMAC. Do not change the settings while the EPTPC is operating.

30.2.63 PTP Event Message TOS Setting Register (PETOSR)

Address(es): EPTPC0.PETOSR 4006 5928h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	EVTO[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	EVTO[7:0]	PTP Event Message TOS Field Value Setting	These bits specify the value of the TOS field within the IPv4 headers of PTP event messages.	R/W
b31 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The PETOSR register specifies the TOS (type of service) field value within the IPv4 headers of PTP event messages. Set this register before starting the EDMAC, ETHERC, or PTPEDMAC. Do not change the settings while the EPTPC is operating.

30.2.62 PTP-pdelay消息目的地IP地址设置寄存器(PDIPR)

Address(es): EPTPC0.PDIPR 4006 5924h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值:	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值:	0	0	0	0	0	0	0	0	0	1	1	0	1	0	1	1

Bit	Symbol	位名称	Description	R/W
b31 to b0	—	—	这些位指定PTP-pdelay消息的目标IP地址。	R/W

PDIPR寄存器指定PTP-pdelay消息的目标IP地址。正常使用时，在该寄存器中设置E000_006Bh(224.0.0.107)。当生成携带IPv4格式的PTPpdelay消息的帧时，该值用于目标IP地址字段。低23位也用于以太网帧的目标MAC地址字段。该值也作为接收帧携带PTP消息的判断条件。在启动EDMAC、ETHERC或PTPEDMAC之前设置该寄存器。请勿在EPTPC运行时更改设置。

30.2.63 PTP事件消息TOS设置寄存器(PETOSR)

Address(es): EPTPC0.PETOSR 4006 5928h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	EVTO[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b7 to b0	EVTO[7:0]	PTP事件消息服务条款字段值设置	这些位指定PTP事件消息的IPv4标头内的TOS字段的值。	R/W
b31 to b8	—	Reserved	这些位被读取为0。写入值应为0。	R/W

PETOSR寄存器指定PTP事件消息的IPv4标头中的TOS（服务类型）字段值。在启动EDMAC、ETHERC或PTPEDMAC之前设置该寄存器。请勿在EPTPC运行时更改设置。

30.2.64 PTP general Message TOS Setting Register (PGTOSR)

Address(es): EPTPC0.PGTOSR 4006 592Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	GETO[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	GETO[7:0]	PTP general Message TOS Field Value Setting	These bits specify the value of the TOS field within the IPv4 headers of PTP general messages.	R/W
b31 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The PGTOSR register specifies the TOS (type of service) field value within the IPv4 headers of PTP general messages. Set this register before starting the EDMAC, ETHERC, or PTPEDMAC. Do not change the settings while the EPTPC is operating.

30.2.65 PTP-primary Message TTL Setting Register (PPTTLR)

Address(es): EPTPC0.PPTTLR 4006 5930h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	PRTL[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	PRTL[7:0]	PTP-primary Message TTL Field Value Setting	These bits specify the value of the TTL field within the IPv4 headers of PTP-primary messages.	R/W
b31 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The PPTTLR register specifies the TTL (time to live) field value within the IPv4 headers of PTP-primary messages. Set this register before starting the EDMAC, ETHERC, or PTPEDMAC. Do not change the settings while the EPTPC is operating.

30.2.64 PTP通用消息TOS设置寄存器(PGTOSR)

Address(es): EPTPC0.PGTOSR 4006 592Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	GETO[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b7 to b0	GETO[7:0]	PTP通用消息服务条款字段值设置	这些位指定PTP通用消息的IPv4标头内的TOS字段的值。	R/W
b31 to b8	—	Reserved	这些位被读取为0。写入值应为0。	R/W

PGTOSR寄存器指定PTP通用消息的IPv4标头中的TOS（服务类型）字段值。在启动EDMAC、ETHERC或PTPEDMAC之前设置该寄存器。请勿在EPTPC运行时更改设置。

30.2.65 PTP-primaryMessageTTL设置寄存器(PPTLR)

Address(es): EPTPC0.PPTTLR 4006 5930h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	PRTL[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b7 to b0	PRTL[7:0]	PTP-primary Message TTL字段值设置	这些位指定PTP主要消息的IPv4标头内的TTL字段的值。	R/W
b31 to b8	—	Reserved	这些位被读取为0。写入值应为0。	R/W

PPTLR寄存器指定PTP主要消息的IPv4标头中的TTL（生存时间）字段值。在启动EDMAC、ETHERC或PTPEDMAC之前设置该寄存器。请勿在EPTPC运行时更改设置。

30.2.66 PTP-pdelay Message TTL Setting Register (PDTTLR)

Address(es): EPTPC0.PDTTLR 4006 5934h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	PDTL[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Bit name	Description	R/W
b7 to b0	PDTL[7:0]	PTP-pdelay Message TTL Field Value	These bits specify the value of the TTL field within the IPv4 headers of PTP-pdelay messages.	R/W
b31 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The PDTTLR register specifies the TTL field value within the IPv4 headers of PTP-pdelay messages. Set this register before starting the EDMAC, ETHERC, or PTPEDMAC. Do not change the settings while the EPTPC is operating.

30.2.67 PTP Event Message UDP Destination Port Number Setting Register (PEUDPR)

Address(es): EPTPC0.PEUDPR 4006 5938h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	EVUPT[15:0]															
Value after reset:	0	0	0	0	0	0	0	1	0	0	1	1	1	1	1	1

Bit	Symbol	Bit name	Description	R/W
b15 to b0	EVUPT[15:0]	PTP Event Message Destination Port Number Setting	These bits specify the value of the destination port number field within the UDP headers of PTP event messages.	R/W
b31 to b16	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The PEUDPR register specifies the destination port number field value within the UDP headers of PTP event messages. In normal usage, set 013Fh (319) in this register. Set this register before starting the EDMAC, ETHERC, or PTPEDMAC. Do not change the settings while the EPTPC is operating.

30.2.66 PTP-pdelay消息TTL设置寄存器(PDTTLR)

Address(es): EPTPC0.PDTTLR 4006 5934h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	PDTL[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	位名称	Description	R/W
b7 to b0	PDTL[7:0]	PTP-pdelay Message TTL 字段值	这些位指定PTP-pdelay消息的IPv4标头中的TTL字段的值。	R/W
b31 to b8	—	Reserved	这些位被读取为0。写入值应为0。	R/W

PDTTLR寄存器指定PTP-pdelay消息的IPv4标头中的TTL字段值。在启动EDMAC、ETHERC或PTPEDMAC之前设置该寄存器。请勿在EPTPC运行时更改设置。

30.2.67 PTP事件消息UDP目标端口号设置寄存器(PEUDPR)

Address(es): EPTPC0.PEUDPR 4006 5938h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	EVUPT[15:0]															
重置后的值:	0	0	0	0	0	0	0	1	0	0	1	1	1	1	1	1

Bit	Symbol	位名称	Description	R/W
b15 to b0	EVUPT[15:0]	PTP事件消息目的端口号 Setting	这些位指定PTP事件消息的UDP标头内的目标端口号字段的值。	R/W
b31 to b16	—	Reserved	这些位被读取为0。写入值应为0。	R/W

PEUDPR寄存器指定PTP事件消息的UDP标头中的目标端口号字段值。
正常使用时，在此寄存器中设置013Fh(319)。在启动EDMAC、ETHERC或PTPEDMAC。请勿在EPTPC运行时更改设置。

30.2.68 PTP general Message UDP Destination Port Number Setting Register (PGUDPR)

Address(es): EPTPC0.PGUDPR 4006 593Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	GEUPT[15:0]															
Value after reset:	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b15 to b0	GEUPT[15:0]	PTP general Message Destination Port Number	These bits specify the value of the destination port number field within the UDP headers of PTP general messages.	R/W
b31 to b16	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The PGUDPR register specifies the destination port number field value within the UDP headers of PTP general messages. In normal usage, set 0140h (320) in this register. Set this register before starting the EDMAC, ETHERC, or PTPEDMAC. Do not change the settings while the EPTPC is operating.

30.2.69 Frame Reception Filter Setting Register (FFLTR)

Address(es): EPTPC0.FFLTR 4006 5940h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	EXTPRM
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	ENB	PRT	SEL
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	SEL	Receive MAC Address Select*1	These bits select how filtering is handled when multicast frames other than PTP messages are received. b2 b0 0 0: Disable filtering (receive all multicast frames) 0 0: Disable filtering (receive all multicast frames) 0 1: Disable filtering (receive all multicast frames) 0 1: Disable filtering (receive all multicast frames) 1 0: Do not receive multicast frames 1 0: Do not receive multicast frames 1 1: Only receive multicast frames matching the MAC address setting in FMAC0RU and FMAC0RL 1 1: Only receive multicast frames matching the MAC address setting in FMAC1RU and FMAC1RL.	R/W
b1	PRT	Frame Reception Enable*1		R/W
b2	ENB	Reception Filter Enable*1		R/W
b15 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b16	EXTPRM	Extended Promiscuous Mode Setting	0: Normal operation (receive unicast frames addressed to the EPTPC, filter PTP frames, filter multicast frames, and receive all broadcast frames) 1: Extended promiscuous mode (receive all frames).	R/W

30.2.68 PTP通用消息UDP目标端口号设置寄存器(PGUDPR)

Address(es): EPTPC0.PGUDPR 4006 593Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	GEUPT[15:0]															
重置后的值:	0	0	0	0	0	0	0	1	0	1	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b15 to b0	GEUPT[15:0]	PTP通用消息 目的端口号	这些位指定PTP通用消息的UDP标头中的目标端口号字段的值。	R/W
b31 to b16	—	Reserved	这些位被读取为0。写入值应为0。	R/W

PGUDPR寄存器指定PTP通用消息的UDP报头中的目标端口号字段值。正常使用时，在该寄存器中设置0140h(320)。在启动EDMAC、ETHERC或PTPEDMAC之前设置该寄存器。请勿在EPTPC运行时更改设置。

30.2.69 帧接收过滤器设置寄存器(FFLTR)

Address(es): EPTPC0.FFLTR 4006 5940h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	EXTPRM
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	ENB	PRT	SEL
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	SEL	接收MAC地址 Select*1	这些位选择在接收到PTP消息以外的多播帧时如何处理过滤。b2 b0 0 0: 禁用过滤（接收所有组播帧） 0 0: 禁用过滤（接收所有组播帧） 0 1: 禁用过滤（接收所有组播帧） 0 1: 禁用过滤（接收所有组播帧） 1 0: 不接收多播帧 1 0: 不接收组播帧 1 1: 只接收与FMAC0RU和FMAC0RL中的MAC地址设置匹配的组播帧 1 1: 只接收与FMAC1RU和FMAC1RL中的MAC地址设置匹配的组播帧。	R/W
b1	PRT	帧接收启用*1		R/W
b2	ENB	接收过滤器启用*1		R/W
b15 to b3	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b16	EXTPRM	扩展混杂模式 Setting	0: 正常操作（接收发往EPTPC的单播帧，过滤PTP帧，过滤组播帧，接收所有广播帧）1: 扩展混杂模式（接收所有帧）。	R/W

Bit	Symbol	Bit name	Description	R/W
b31 to b17	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. The setting in these bits is only valid when the EXTPRM bit is 0.

The FFLTR register switches extended promiscuous mode on or off and selects how filtering is handled when multicast frames other than PTP messages are received. To enable the filter for the reception of multicast frames other than PTP messages, set the ENB, PRT, and SEL bits to 110b or 111b. Frames passed by the filter are then transferred by EDMAC0.

Set this register before starting the EDMAC, ETHERC, or PTPEDMAC. Do not change the settings while the EPTPC is operating.

30.2.70 Frame Reception Filter MAC Address 0 Setting Register (FMAC0RU, FMAC0RL)

Address(es): EPTPC0.FMAC0RU 4006 5960h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b23 to b0	—	—	These bits specify the upper-order 24 bits of the destination MAC address for received multicast frames.	R/W
b31 to b24	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Address(es): EPTPC0.FMAC0RL 4006 5964h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b23 to b0	—	—	These bits specify the lower-order 24 bits of the destination MAC address for received multicast frames.	R/W
b31 to b24	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The FMAC0RU and FMAC0RL registers specify the MAC address for filtering during the reception of multicast frames other than PTP messages. Set this register before starting the EDMAC, ETHERC, or PTPEDMAC. Do not change the settings while the EPTPC is operating.

Bit	Symbol	位名称	Description	R/W
b31 to b17	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 这些位的设置仅在EXTPRM位为0时有效。

FFLTR寄存器打开或关闭扩展混杂模式，并选择在接收到PTP消息以外的多播帧时如何处理过滤。要启用过滤器以接收PTP消息以外的多播帧，请将ENB、PRT和SEL位设置为110b或111b。过滤器通过的帧然后由EDMAC0传输。

在启动EDMAC、ETHERC或PTPEDMAC之前设置该寄存器。请勿在EPTPC运行时更改设置。

30.2.70 帧接收过滤器MAC地址0设置寄存器(FMAC0RU FMAC0RL)

Address(es): EPTPC0.FMAC0RU 4006 5960h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—								
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b23 to b0	—	—	这些位指定目标的高24位 接收到的多播帧的MAC地址。	R/W
b31 to b24	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Address(es): EPTPC0.FMAC0RL 4006 5964h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—								
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b23 to b0	—	—	这些位指定目标的低24位 接收到的多播帧的MAC地址。	R/W
b31 to b24	—	Reserved	这些位被读取为0。写入值应为0。	R/W

FMAC0RU和FMAC0RL寄存器指定MAC地址，以便在接收PTP消息以外的多播帧期间进行过滤。在启动EDMAC、ETHERC或PTPEDMAC之前设置该寄存器。请勿在EPTPC运行时更改设置。

30.2.71 Frame Reception Filter MAC Address 1 Setting Register (FMAC1RU, FMAC1RL)

Address(es): EPTPC0.FMAC1RU 4006 5968h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b23 to b0	—	—	These bits specify the upper-order 24 bits of the destination MAC address for received multicast frames.	R/W
b31 to b24	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Address(es): EPTPC0.FMAC1RL 4006 596Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b23 to b0	—	—	These bits specify the lower-order 24 bits of the destination MAC address for received multicast frames.	R/W
b31 to b24	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The FMAC1RU and FMAC1RL registers specify the MAC address for filtering during the reception of multicast frames other than PTP messages. Set this register before starting the EDMAC, ETHERC, or PTPEDMAC. Do not change the settings while the EPTPC is operating.

30.2.71 帧接收过滤器MAC地址1设置寄存器(FMAC1RU FMAC1RL)

Address(es): EPTPC0.FMAC1RU 4006 5968h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—								
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b23 to b0	—	—	这些位指定目标的高24位 接收到的多播帧的MAC地址。	R/W
b31 to b24	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Address(es): EPTPC0.FMAC1RL 4006 596Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—								
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b23 to b0	—	—	这些位指定目标的低24位 接收到的多播帧的MAC地址。	R/W
b31 to b24	—	Reserved	这些位被读取为0。写入值应为0。	R/W

FMAC1RU和FMAC1RL寄存器指定MAC地址，以便在接收PTP消息以外的多播帧期间进行过滤。在启动EDMAC、ETHERC或PTPEDMAC之前设置该寄存器。请勿在EPTPC运行时更改设置。

30.2.72 Asymmetric Delay Setting Register (DASYMRU, DASYMRL)

Address(es): EPTPC0.DASYMRU 4006 59C0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b15 to b0	—	—	These bits specify the upper-order 16 bits of the asymmetric delay value. Set them to 0000h in this MCU.	R/W
b31 to b16	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Address(es): EPTPC0.DASYMRL 4006 59C4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b31 to b0	—	—	These bits specify the lower-order 32 bits of the asymmetric delay value. Set them to 0000_0000h in this MCU.	R/W

The DASYMRU and DASYMRL registers specify the asymmetric delay value (delayAsymmetry). Set the registers DASYMRU and DASYMRL to 0000_0000h in this MCU.

30.2.72 非对称延迟设置寄存器(DASYMRU DASYMRL)

Address(es): EPTPC0.DASYMRU 4006 59C0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b15 to b0	—	—	这些位指定非对称延迟值的高16位。在此MCU中将它们设置为0000h。	R/W
b31 to b16	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Address(es): EPTPC0.DASYMRL 4006 59C4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

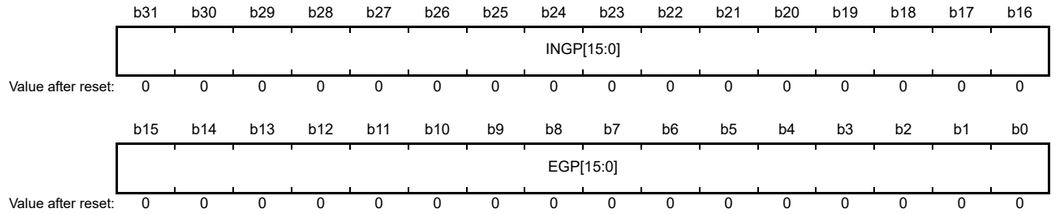
	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b31 to b0	—	—	这些位指定非对称延迟值的低32位。在此MCU中将它们设置为0000_0000h。	R/W

DASYMRU和DASYMRL寄存器指定非对称延迟值(delayAsymmetry)。设置寄存器此MCU中的DASYMRU和DASYMRL到0000_0000h。

30.2.73 Timestamp Latency Setting Register (TSLATR)

Address(es): EPTPC0.TSLATR 4006 59C8h



Bit	Symbol	Bit name	Description	R/W
b15 to b0	EGP[15:0]	Output Port Timestamp Latency Setting	These bits specify the timestamp latency (ns) for the output ports.	R/W
b31 to b16	INGP[15:0]	Input Port Timestamp Latency Setting	These bits specify the timestamp latency (ns) for the input ports.	R/W

The TSLATR register specifies the amount of latency in timestamp acquisition in nanoseconds. Do not change the settings while reception or transmission of PTP messages is enabled.

EGP[15:0] bits (Output Port Timestamp Latency Setting)

Set the EGP[15:0] bits to the fixed values listed in Table 30.8 for the target system. The timestamp latency differs with the link transfer rate (100 or 10 Mbps) and the frequency of the STCA clock (20, 25, 50, or 100 MHz).

Table 30.8 EGP[15:0] bit settings (ns)

Link transfer rate		STCA clock frequency 20 MHz	25 MHz	50 MHz	100 MHz
MII	100 Mbps	590	625	695	730
	10 Mbps	7430	7465	7535	7570
RMII	100 Mbps	770	805	875	910
	10 Mbps	9230	9265	9335	9370

INGP[15:0] bits (Input Port Timestamp Latency Setting)

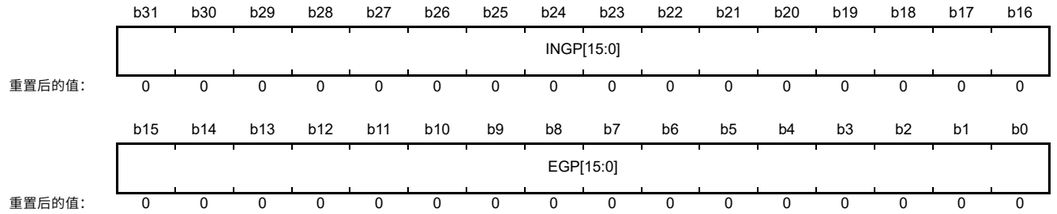
Set the INGP[15:0] bits to the fixed values listed in Table 30.9 for the target system. The timestamp latency differs with the link transfer rate (100 or 10 Mbps) and the frequency of the STCA clock (20, 25, 50, or 100 MHz).

Table 30.9 INGP[15:0] bit settings (ns)

Link transfer rate		STCA clock frequency 20 MHz	25 MHz	50 MHz	100 MHz
MII	100 Mbps	980	945	875	840
	10 Mbps	8180	8145	8075	8015
RMII	100 Mbps	1060	1025	955	920
	10 Mbps	8980	8945	8875	8815

30.2.73 时间戳延迟设置寄存器(TSLATR)

Address(es): EPTPC0.TSLATR 4006 59C8h



Bit	Symbol	位名称	Description	R/W
b15 to b0	EGP[15:0]	输出端口时间戳延迟设置	这些位指定输出端口的时间戳延迟(ns)。	R/W
b31 to b16	INGP[15:0]	输入端口时间戳延迟Setting	这些位指定输入端口的时间戳延迟(ns)。	R/W

TSLATR寄存器指定时间戳采集的延迟量（以纳秒为单位）。在启用PTP消息的接收或传输时不要更改设置。

EGP[15:0]位（输出端口时间戳延迟设置）

将目标系统的EGP[15:0]位设置为表30.8中列出的固定值。时间戳延迟因链路传输速率（100或10Mbps）和STCA时钟频率（20、25、50或100MHz）而异。

Table 30.8 EGP[15:0]位设置(ns)

链接传输率		STCA时钟频率 20 MHz	25 MHz	50 MHz	100 MHz
MII	100 Mbps	590	625	695	730
	10 Mbps	7430	7465	7535	7570
RMII	100 Mbps	770	805	875	910
	10 Mbps	9230	9265	9335	9370

INGP[15:0]位（输入端口时间戳延迟设置）

将IGP[15:0]位设置为目标系统的表30.9中列出的固定值。时间戳延迟因链路传输速率（100或10Mbps）和STCA时钟频率（20、25、50或100MHz）而异。

Table 30.9 INGP[15:0]位设置(ns)

链接传输率		STCA时钟频率 20 MHz	25 MHz	50 MHz	100 MHz
MII	100 Mbps	980	945	875	840
	10 Mbps	8180	8145	8075	8015
RMII	100 Mbps	1060	1025	955	920
	10 Mbps	8980	8945	8875	8815

30.2.74 SYNFP Operation Setting Register (SYCONFR)

Address(es): EPTPC0.SYCONFR 4006 59CCh

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FILDIS
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	SBDIS	—	—	—	—	TCYC[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	TCYC[7:0]	PTP Message Transmission Interval Setting	These bits specify the time from the completion of one transmission to the start of the next in transmission clock cycles. A value n in these bits means that a transmission interval of n cycles is secured. No interval is secured if the setting is 00h. Recommended setting: 28h (40 cycles).	R/W
b11 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b12	SBDIS	Sync Message Transmission Bandwidth Securing Disable	0: Enable securing of the bandwidth for the transmission of SYNC messages (give lower priority to transfers by the EDMAC) 1: Disable securing of the bandwidth for the transmission of SYNC messages (give higher priority to transfers by the EDMAC).	R/W
b15 to b13	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b16	FILDIS	Receive Message domainNumber Filter Disable	0: Include comparison with the domainNumber field in the filtering conditions for the reception of PTP messages 1: Do not include comparison with the domainNumber field in the filtering conditions for the reception of PTP messages.	R/W
b31 to b17	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The SYCONFR register controls operation of the SYNFP module. Set this register before starting the EDMAC, ETHERC, or PTPEDMAC. Do not change the settings while the EPTPC is operating.

TCYC[7:0] bits (PTP Message Transmission Interval Setting)

The TCYC[7:0] bits specify a wait time between packets to secure a fixed transmission delay. The setting defines the interval from input of the transmission completed signal from the ETHERC to output of the next transmission request as a number of cycles of the transmission clock, which runs at 2.5 MHz if the link transfer rate is 10 Mbps and 25 MHz if the rate is 100 Mbps.

SBDIS bit (Sync Message Transmission Bandwidth Securing Disable)

The SBDIS bit disables securing of bandwidth to increase accuracy of the interval for the transmission of SYNC messages.

FILDIS bit (Receive Message domainNumber Filter Disable)

The FLDIS bit selects whether or not to include comparison with the domainNumber field in the filtering conditions for the reception of PTP messages.

30.2.74 SYNFP操作设置寄存器(SYCONFR)

Address(es): EPTPC0.SYCONFR 4006 59CCh

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FILDIS
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	SBDIS	—	—	—	—	TCYC[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b7 to b0	TCYC[7:0]	PTP Message 传输间隔 Setting	这些位指定从一个传输完成到下一个传输时钟周期开始的时间。这些比特中的值n意味着保证了n个周期的传输间隔。如果设置为00h，则不保证间隔。 Recommended setting: 28h (40 cycles).	R/W
b11 to b8	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b12	SBDIS	同步消息传输带宽保护禁用	0：启用SYNC消息传输的带宽保护（赋予EDMAC传输较低的优先级）1：禁用SYNC消息传输的带宽保护（赋予EDMAC传输更高的优先级）。	R/W
b15 to b13	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b16	FILDIS	接收消息域号码过滤器禁用	0：在PTP消息接收的过滤条件中包含与domainNumber字段的比较 1：在PTP消息的接收过滤条件中不包含与domainNumber字段的比较。	R/W
b31 to b17	—	Reserved	这些位被读取为0。写入值应为0。	R/W

SYCONFR寄存器控制SYNFP模块的操作。在启动EDMAC之前设置该寄存器，ETHERC或PTPEDMAC。请勿在EPTPC运行时更改设置。

TCYC[7:0]位（PTP消息传输间隔设置）

TCYC[7:0]位指定数据包之间的等待时间，以确保固定的传输延迟。该设置定义了从ETHERC输入传输完成信号到输出下一个传输请求的间隔，作为传输时钟的周期数，如果链路传输速率为10Mbps，则以2.5MHz运行，如果链路传输速率为25MHz，则以25MHz运行。速率为100Mbps。

SBDIS位（同步消息传输带宽保护禁用）

SBDIS位禁用带宽保护以提高SYNC消息传输间隔的准确性。

FILDIS位（接收消息域编号过滤器禁用）

FLDIS位选择是否在接收PTP消息的过滤条件中包括与domainNumber字段的比较。

30.2.75 SYNFP Frame Format Setting Register (SYFORMR)

Address(es): EPTPC0.SYFORMR 4006 59D0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FORM1	FORM0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	FORM0	Ethernet Frame Format Setting	0: Ethernet II frame format 1: IEEE802.3 frame format.	R/W
b1	FORM1	Ethernet/UDP Encapsulation	0: PTP directly over Ethernet 1: PTP over UDP/IPv4.	R/W
b31 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The SYFORMR register specifies the format for frame generation by the SYNFP module. Set this register before starting the EDMAC, ETHERC, or PTPEDMAC. Do not change the settings while the EPTPC is operating.

30.2.76 Response Message Reception Timeout Register (RSTOUTR)

Address(es): EPTPC0.RSTOUTR 4006 59D4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b31 to b0	—	Response Message Reception Timeout Time Setting	If no response message is received within n × 1024 (ns), where n is the setting in these bits, a timeout is detected.	R/W

The RSTOUTR register specifies the time for detection of a timeout during the reception of PTP response messages (Delay_Resp and Pdelay_Resp). If no Delay_Resp or Pdelay_Resp message is received within the time specified in this register after transmission of a Delay_Req or Pdelay_Req message, the SYSR.DRPTO flag is set to 1. The value specified in this register is only reflected in the SYNFP module after the SYRVLDR.STUP bit is set to 1.

30.2.75 SYNFP帧格式设置寄存器(SYFORMR)

Address(es): EPTPC0.SYFORMR 4006 59D0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FORM1	FORM0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	FORM0	以太网帧格式设置	0：以太网II帧格式1：IEEE802.3帧格式。	R/W
b1	FORM1	Ethernet/UDP Encapsulation	0：直接通过以太网的PTP1 ：通过UDPIPv4的PTP。	R/W
b31 to b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W

SYFORMR寄存器指定SYNFP模块生成帧的格式。在启动EDMAC、ETHERC或PTPEDMAC之前设置该寄存器。请勿在EPTPC运行时更改设置。

30.2.76 响应消息接收超时寄存器(RSTOUTR)

Address(es): EPTPC0.RSTOUTR 4006 59D4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b31 to b0	—	响应消息接收 超时时间设置	如果在n×1024(ns)内没有收到响应消息，其中n是这些位中的设置，则检测到超时。	R/W

RSTOUTR寄存器指定在接收PTP响应消息（Delay_Resp和Pdelay_Resp）期间检测超时的时间。如果在发送Delay_Req或Pdelay_Req消息后，在此寄存器中指定的时间内没有接收到Delay_Resp或Pdelay_Resp消息，则SYSR.DRPTO标志设置为1。此寄存器中指定的值仅在SYRVLDR之后反映在SYNFP模块中.STUP位设置为1。

30.2.77 PTP Reset Register (PTRSTR)

Address(es): EPTPC_CFG.PTRSTR 4006 4500h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RESET
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	RESET	EPTPC Software Reset	0: Do not reset the EPTPC 1: Reset the EPTPC.*1	R/W
b31 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Do not access the EPTPC-related registers other than this register while a software reset is being issued.

The PTRSTR register resets the EPTPC. It takes 64 cycles of the peripheral module clock (PCLKA) until initialization of the EPTPC is complete. After the RESET bit is set to 1, wait for 64 PCLKA cycles before clearing its value to 0.

30.2.78 STCA Clock Select Register (STCSELR)

Address(es): EPTPC_CFG.STCSELR 4006 4504h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	SCLKSEL[2:0]			—	—	—	—	—	SCLKDIV[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	SCLKDIV[2:0]	PCLKA Clock Frequency Division	b2 b0 0 0 1: 1 0 1 0: 1/2 0 1 1: 1/3 1 0 0: 1/4 1 0 1: 1/5 1 1 0: 1/6. Other settings are prohibited.	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b10 to b8	SCLKSEL[2:0]	STCA Clock Select	b10 b8 0 0 0: Use PCLKA clock divided by 1 to 6 0 1 0: Input clock from the REF50CK0 pin. Other settings are prohibited.	R/W
b31 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The STCSELR register selects the STCA clock signal for the EPTPC. Set this register before starting the EDMAC, ETHERC, or PTPEDMAC. Do not change the settings while the EPTPC is operating.

30.2.77 PTP复位寄存器(PTRSTR)

Address(es): EPTPC_CFG.PTRSTR 4006 4500h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RESET
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	RESET	EPTPC软件复位	0：不复位EPTPC1：复位EPTPC。*1	R/W
b31 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 发出软件复位时，请勿访问该寄存器以外的EPTPC相关寄存器。

PTRSTR寄存器复位EPTPC。外围模块时钟(PCLKA)的64个周期直到EPTPC的初始化完成。在RESET位设置为1后，等待64个PCLKA周期后将其值清零。

30.2.78 STCA时钟选择寄存器(STCSELR)

Address(es): EPTPC_CFG.STCSELR 4006 4504h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	SCLKSEL[2:0]			—	—	—	—	—	SCLKDIV[2:0]		
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0

Bit	Symbol	位名称	Description	R/W
b2 to b0	SCLKDIV[2:0]	PCLKA时钟分频	b2 b0 0 0 1: 1 0 1 0: 1/2 0 1 1: 1/3 1 0 0: 1/4 1 0 1: 1/5 10:16.禁止其他设置。	R/W
b7 to b3	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b10 to b8	SCLKSEL[2:0]	STCA时钟选择	b10 b8 0 0 0：使用PCLKA时钟除以1到6 10：来自REF50CK0引脚的输入时钟。禁止其他设置。	R/W
b31 to b11	—	Reserved	这些位被读取为0。写入值应为0。	R/W

STCSELR寄存器为EPTPC选择STCA时钟信号。在启动EDMAC之前设置该寄存器，ETHERC或PTPEDMAC。请勿在EPTPC运行时更改设置。

SCLKDIV[2:0] bits (PCLKA Clock Frequency Division)

The SCLKDIV[2:0] bits select the division ratio of PCLKA. When the setting of the SCLKSEL[2:0] bits is 000b, the frequency-divided PCLKA is used as the STCA clock signal.

SCLKSEL[2:0] bits (STCA Clock Select)

The SCLKSEL[2:0] bits select the STCA clock signal for use in the EPTPC.

30.2.79 Bypass 1588 Module Register (BYPASS)

Address(es): EPTPC_CFG.BYPASS 4006 4508h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	BYPASS0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	BYPASS0	Bypass1588 module for Ether 0ch	0: Use 1588 module for Ether channel 0 1: Bypass 1588 module for Ether channel 0.	R/W
b31 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Do not access the BYPASS register while the Ether module is in operation. When the EPTPC is not used, bypass it by setting the BYPASS register.

30.3 Operation

After release from the reset state, the EPTPC is set to not receive (analyze) or transmit (generate) PTP messages, so it has no effect on the transmission or reception of frames by the ETHERC and EDMAC at that time. The EPTPC registers must be configured to transmit and receive PTP messages for the ETHERC and EDMAC to be able to use packet filtering by MAC address in the SYNFP module.

Figure 30.3 shows a block diagram of the modules involved in frame transfer.

SCLKDIV[2:0]位（PCLKA时钟分频）

SCLKDIV[2:0]位选择PCLKA的分频比。当SCLKSEL[2:0]位设置为000b时，分频PCLKA用作STCA时钟信号。

SCLKSEL[2:0]位（STCA时钟选择）

SCLKSEL[2:0]位选择用于EPTPC的STCA时钟信号。

30.2.79 绕过1588模块寄存器(BYPASS)

Address(es): EPTPC_CFG.BYPASS 4006 4508h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	BYPASS0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	BYPASS0	用于Ether0ch的Bypass1588模块	0：Ether通道0使用1588模块1：Ether通道0绕过1588模块。	R/W
b31 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note: 在以太模块运行时不要访问BYPASS寄存器。当不使用EPTPC时，通过设置BYPASS寄存器绕过它。

30.3 Operation

从复位状态释放后，EPTPC被设置为不接收（分析）或发送（生成）PTP消息，因此对当时的ETHERC和EDMAC发送或接收帧没有影响。必须将EPTPC寄存器配置为发送和接收PTP消息，以便ETHERC和EDMAC能够使用SYNFP模块中的MAC地址进行数据包过滤。

图30.3显示了帧传输中涉及的模块的框图。

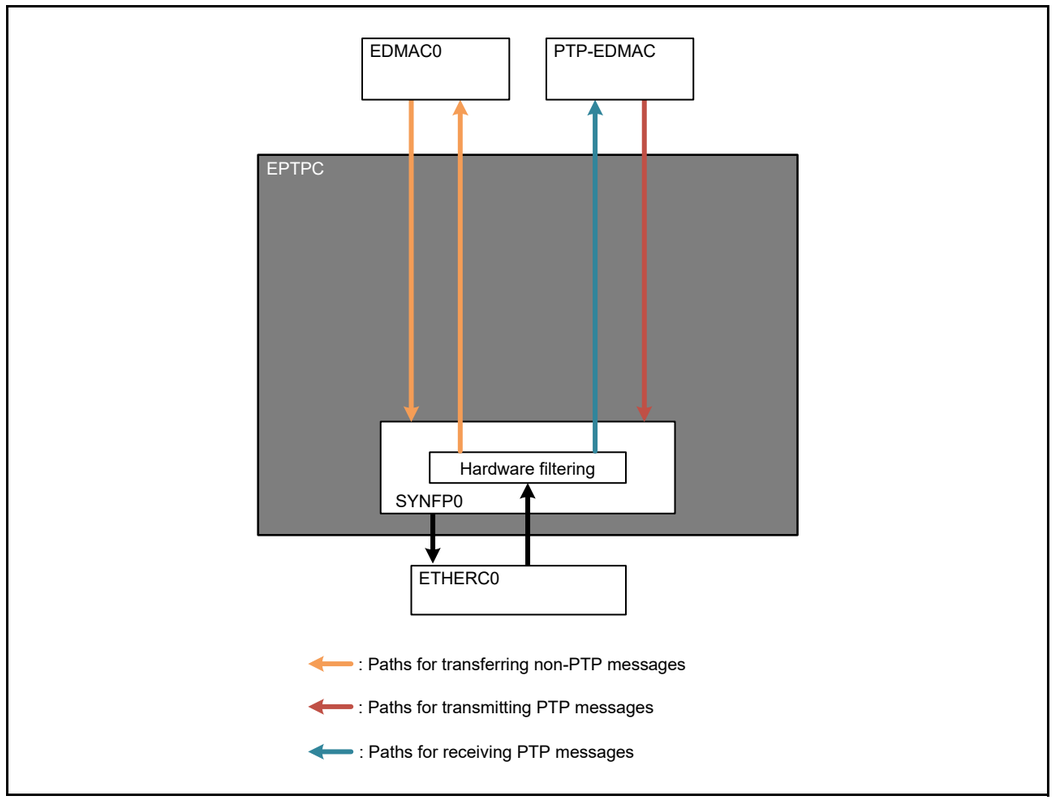


Figure 30.3 Block diagram of the modules involved in frame transfers

30.3.1 Transmission and Reception of Non-PTP Messages

The EPTPC operates in extended promiscuous mode when the FFLTR.EXTPRM bit setting is 1. In this mode, all frames received by the Ethernet ports are transferred to the EDMAC without filtering. The EPTPC operates in normal mode when the FFLTR.EXTPRM bit setting is 0. In this mode, the SYNFP module applies its hardware filtering function to filter frames received by the Ethernet ports.

The EPTPC and EDMAC transfer received unicast frames if they are for the given node.

Operation when multicast frames are received can be selected from the following: frames are transferred to the EDMAC, frames are not transferred to the EDMAC, or frames are transferred to the EDMAC only when the address matches the specified MAC address.

The EPTPC transfers received broadcast frames to the EDMAC for the receiving Ethernet port.

30.3.2 Paths for the Transfer of Non-PTP Messages

Messages received through the Ethernet port are transferred to the EDMAC. Figure 30.4 is a diagram of paths for the transmission and reception of non-PTP messages.

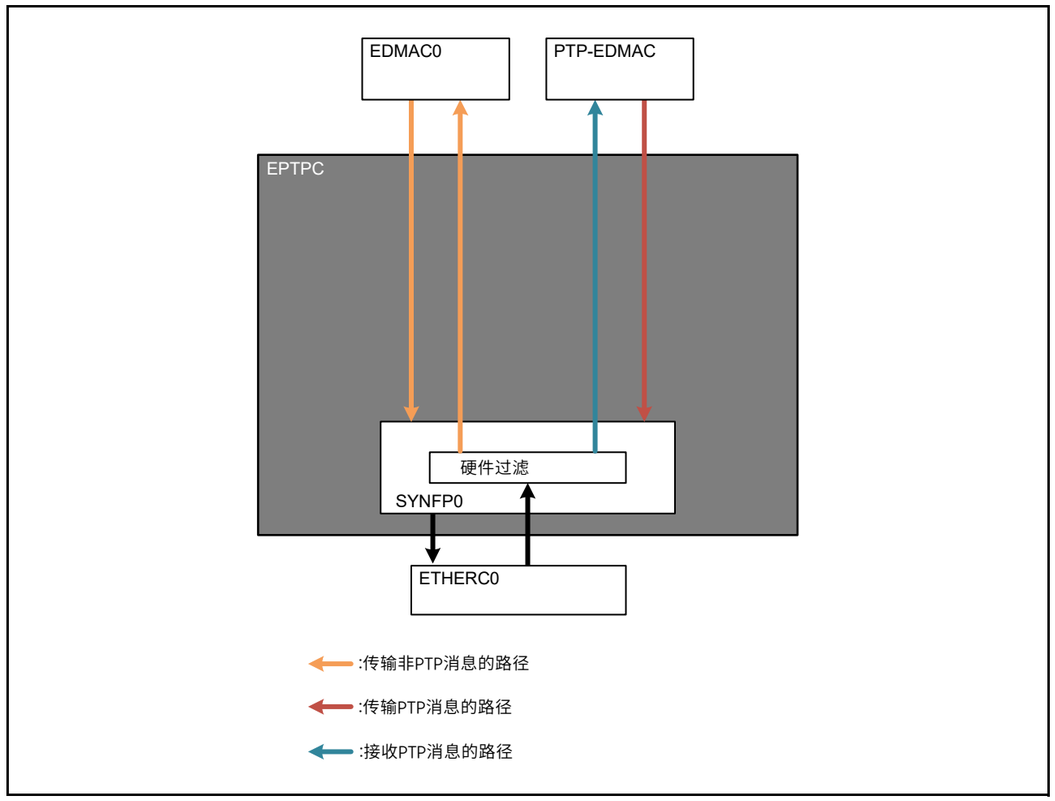


Figure 30.3 涉及帧传输的模块框图

30.3.1 非PTP消息的传输和接收

当FFLTR.EXTPRM位设置为1时，EPTPC在扩展混杂模式下运行。在这种模式下，以太网端口接收到的所有帧都被传输到EDMAC而不进行过滤。当FFLTR.EXTPRM位设置为0时，EPTPC在正常模式下运行。在这种模式下，SYNFP模块应用其硬件过滤功能来过滤以太网端口接收到的帧。

EPTPC和EDMAC传输接收到的单播帧，如果它们是给定节点的。

接收到多播帧时的操作可以从以下选择：将帧传输到EDMAC，不将帧传输到EDMAC，或仅当地址与指定的MAC地址匹配时才将帧传输到EDMAC。

EPTPC将接收到的广播帧传输到接收以太网端口的EDMAC。

30.3.2 非PTP消息的传输路径

通过以太网端口接收的消息被传输到EDMAC。图30.4是发送和接收非PTP消息的路径图。

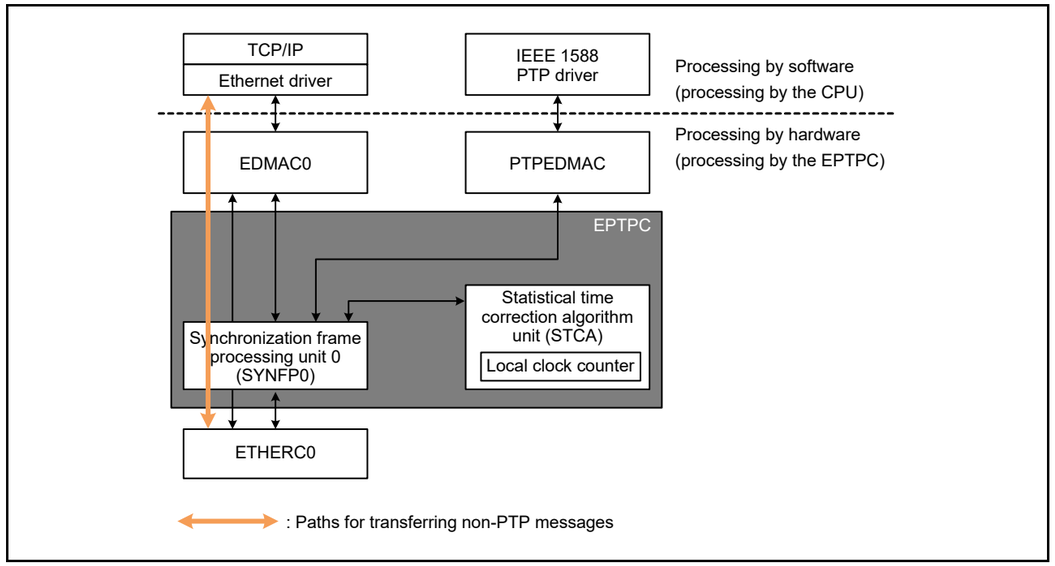


Figure 30.4 Paths for the transmission and reception of non-PTP messages

30.3.3 Transmission and Reception of PTP Messages

The EPTPC hardware automatically handles analysis and extraction of fields from received PTP messages, and generation and transmission of PTP messages. However, the software must still handle the transmission of certain PTP messages. Table 30.10 shows the specifications for control over the transmission and reception of the different PTP message types.

Table 30.10 Control over the transmission and reception of PTP messages

Message type	Message	OC (Ordinary Clock)	
		Master	Slave
Event	Sync	Generation (automatic)	Reception (automatic)
	Delay_Req	Generation (automatic)	Reception (automatic)
	Pdelay_Req	Generation and reception (automatic)	Generation and reception (automatic)
	Pdelay_Resp	Generation and reception (automatic)	Generation and reception (automatic)
General	Announce	Generation (automatic)	Reception (software)
	Follow_Up	—*1	Reception (automatic)
	Delay_Resp	Packet generation	Reception (automatic)
	Pdelay_Resp_Follow_Up	—*1	Reception (automatic)
	Management	Transmission and reception (software)	
	Signaling	Transmission and reception (software)	

Note 1. Control is not required as the clock for this is a one-step clock.

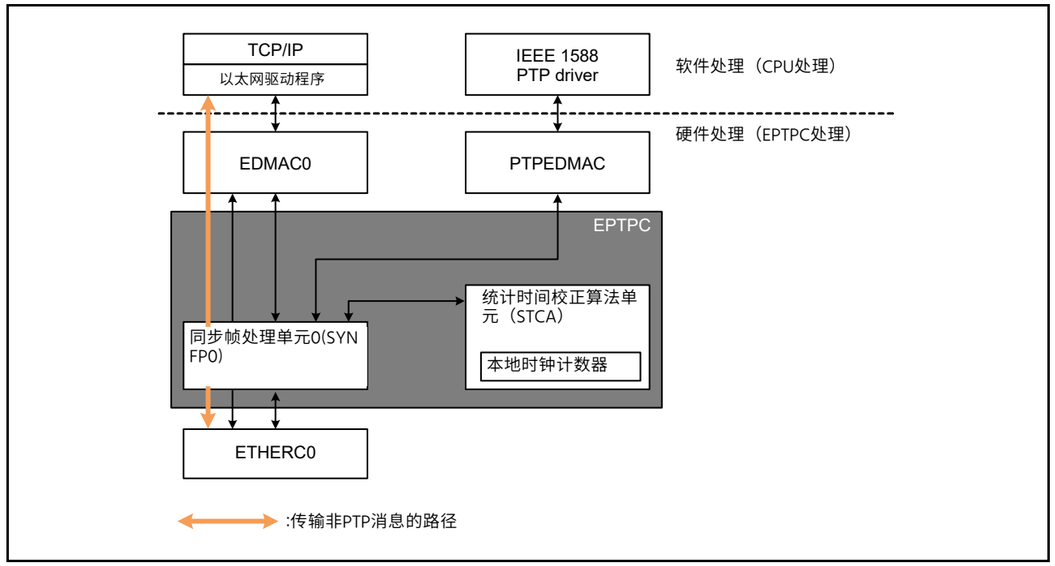


Figure 30.4 非PTP消息的传输和接收路径

30.3.3 PTP消息的发送和接收

EPTPC硬件自动处理接收到的PTP消息中的字段分析和提取，以及PTP消息的生成和传输。但是，该软件仍必须处理某些PTP消息的传输。表30.10显示了控制不同PTP消息类型的发送和接收的规范。

Table 30.10 控制PTP消息的传输和接收

消息类型	Message	OC (Ordinary Clock)	
		Master	Slave
Event	Sync	Generation (automatic)	Reception (automatic)
	Delay_Req	Generation (automatic)	Reception (automatic)
	Pdelay_Req	生成和接收（自动）	生成和接收（自动）
	Pdelay_Resp	生成和接收（自动）	生成和接收（自动）
General	Announce	Generation (automatic)	Reception (software)
	Follow_Up	—*1	Reception (automatic)
	Delay_Resp	数据包生成	Reception (automatic)
	Pdelay_Resp_Follow_Up	—*1	Reception (automatic)
	Management	传输和接收（软件）	
	Signaling	传输和接收（软件）	

Note 1. 不需要控制，因为它的时钟是单步时钟。

30.3.4 Paths for the Transfer of PTP Messages

Transfer paths for the PTP messages differ based on whether transfer requires processing by software or is automatically processed by hardware.

30.3.4.1 Paths for the transfer of PTP messages requiring processing by software

Figure 30.5 shows the paths for the transfer of PTP messages where transfer requires software processing. The figure shows paths for all message, clock-type, and process combinations for which “(software)” is indicated in Table 30.10.

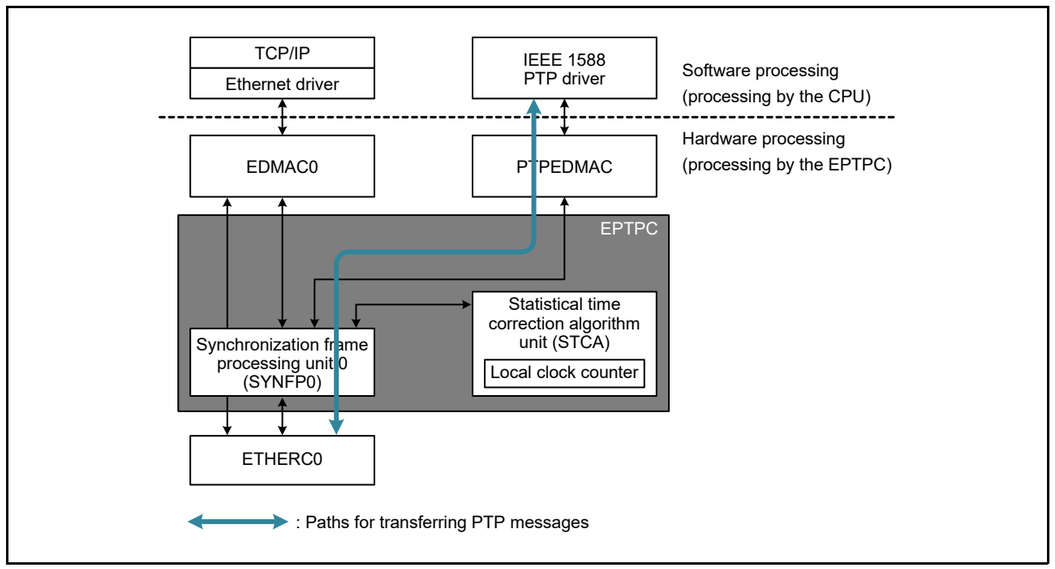


Figure 30.5 Paths for the transfer of PTP messages requiring software processing

30.3.4.2 Paths for the transfer of PTP messages handled automatically by hardware

For PTP messages for which the hardware automatically handles the processing, the SYNFP modules handle transmission and reception.

(1) Generation of and response to PTP messages by hardware

Figure 30.6 shows the transfer paths in the automatic generation of and response to PTP messages by the SYNFP module. The paths in the figure are used for the “Generation (automatic)”, “Reception (automatic)”, and “Generation and reception (automatic)” operations indicated in Table 30.10.

30.3.4 PTP消息的传输路径

PTP消息的传输路径根据传输是需要软件处理还是由硬件自动处理而有所不同。

30.3.4.1 需要软件处理的PTP消息的传输路径

图30.5显示了PTP消息的传输路径，其中传输需要软件处理。该图显示了表30.10中指示“（软件）”的所有消息、时钟类型和进程组合的路径。

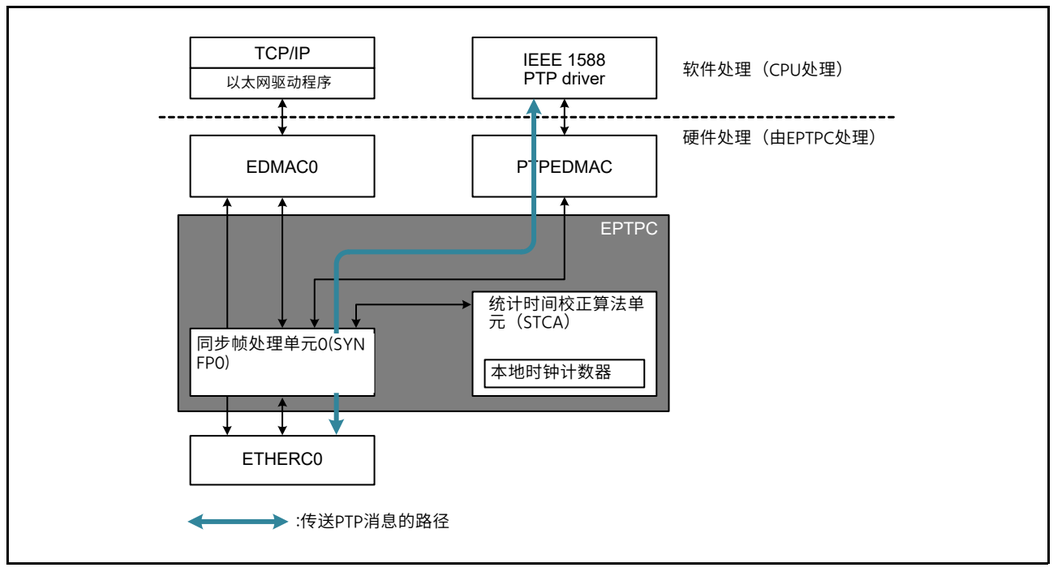


Figure 30.5 需要软件处理的PTP消息的传输路径

30.3.4.2 由硬件自动处理的PTP消息传输路径

对于硬件自动处理的PTP消息，SYNFP模块处理传输和接收。

(1) 通过硬件生成和响应PTP消息

图30.6显示了SYNFP模块自动生成和响应PTP消息的传输路径。图中的路径用于表30.10所示的“生成（自动）”、“接收（自动）”和“生成和接收（自动）”操作。

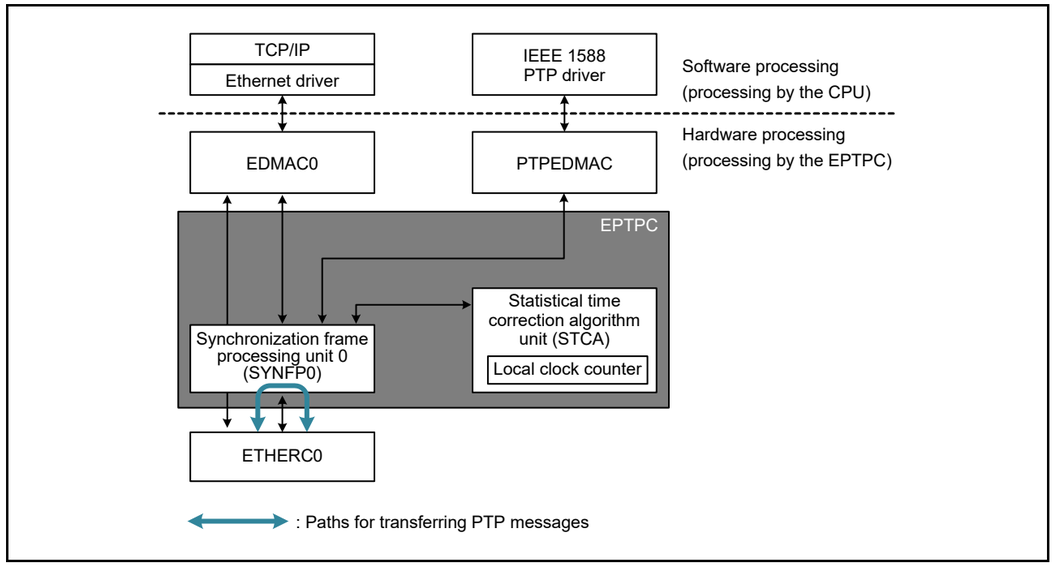


Figure 30.6 Paths for the generation of and response to PTP messages by hardware

30.3.5 Clock Devices

The EPTPC can operate as the clock devices defined in IEEE 1588.

30.3.5.1 End-to-End (E2E)

(1) Master

PTP messages are transmitted and received as described in Table 30.11 in operation as an end-to-end (E2E) master.

Table 30.11 Processing of PTP messages by an E2E master

Message type	Message	The EPTPC...
Event	Sync	Transmits Sync messages at the fixed interval specified in the SYTLIR.SYNC[7:0] bits.
	Delay_Req	When this message is received, transmits a Delay_Resp message in response.
	Pdelay_Req	—
	Pdelay_Resp	—
General	Announce	Transmits Announce messages at the fixed interval specified in the SYTLIR.ANCE[7:0] bits.
	Follow_Up	—
	Delay_Resp	Transmits this as the response to a received Delay_Req messages.
	Pdelay_Resp_Follow_Up	—
	Management	Transmits and receives Management messages by software through the PTPEDMAC.
	Signaling	Transmits and receives Signaling messages by software through the PTPEDMAC.

(2) Slave

PTP messages are transmitted and received as described in Table 30.12 in operation as an E2E slave, and the calculated offsetFromMaster is used to correct the local time information.

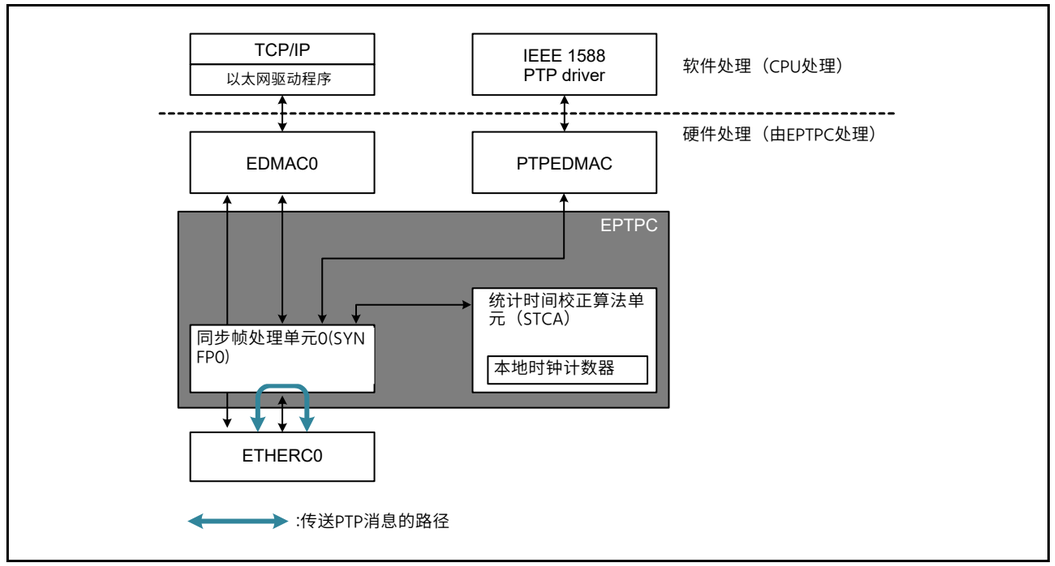


Figure 30.6 硬件生成和响应PTP消息的路径

30.3.5 时钟设备

EPTPC可以作为IEEE1588中定义的时钟设备运行。

30.3.5.1 End-to-End (E2E)

(1) Master

PTP消息的发送和接收如表30.11中所述，作为端到端(E2E)主机运行。

Table 30.11 E2E主站对PTP消息的处理

消息类型	Message	The EPTPC...
Event	Sync	以SYTLIR.SYNC[7:0]位中指定的固定间隔发送同步消息。
	Delay_Req	当收到此消息时，发送一个Delay_Resp消息作为响应。
	Pdelay_Req	—
	Pdelay_Resp	—
General	Announce	以SYTLIR.ANCE[7:0]位中指定的固定间隔发送Announce消息。
	Follow_Up	—
	Delay_Resp	将此作为对接收到的Delay_Req消息的响应传输。
	Pdelay_Resp_Follow_Up	—
	Management	软件通过PTPEDMAC发送和接收管理消息。
	Signaling	软件通过PTPEDMAC发送和接收信令消息。

(2) Slave

PTP消息的发送和接收如表30.12中所述，作为E2E从站运行，计算出的offsetFromMaster用于校正本地时间信息。

Table 30.12 Processing of PTP messages by an E2E slave

Message type	Message	The EPTPC...
Event	Sync	Calculates the offsetFromMaster value when this message is received if twoStepFlag in flagField was FALSE (1-step clock).
	Delay_Req	Transmits Delay_Req messages at random intervals from 0 to the time specified in the SYTLIR.DREQ[7:0] bits × 2.
	Pdelay_Req	—
	Pdelay_Resp	—
General	Announce	Transmits Announce messages by software through the PTPEDMAC.
	Follow_Up	Calculates the offsetFromMaster value when this message is received if twoStepFlag in flagField of the most recently received Sync message was TRUE (two-step clock).
	Delay_Resp	Calculates the meanPathDelay value when this message is received.
	Pdelay_Resp_Follow_Up	—
	Management	Transmits and receives Management messages by software through the PTPEDMAC.
	Signaling	Transmits and receives Signaling messages by software through the PTPEDMAC.

30.3.5.2 Peer-to-Peer (P2P)

(1) Master

PTP messages are transmitted and received as described in Table 30.13 in operation as a Peer-to-Peer (P2P) master.

Table 30.13 Processing of PTP messages by a P2P master

Packet type	Message	The EPTPC...
Event	Sync	Transmits timestamps for transmission at the fixed interval specified in the SYTLIR.SYNC[7:0] bits.
	Delay_Req	—
	Pdelay_Req	• Transmits Pdelay_Req messages at the fixed interval specified in the SYTLIR.DREQ[7:0] bits • Transmits a Pdelay_Resp message in response when this message is received.
	Pdelay_Resp	• Transmits this as the response to a received Pdelay_Req message • Calculates the meanPathDelay value when this message is received if twoStepFlag in flagField was FALSE (one-step clock).
General	Announce	Transmits Announce messages at the fixed interval specified in the SYTLIR.ANCE[7:0] bits.
	Follow_Up	—
	Delay_Resp	—
	Pdelay_Resp_Follow_Up	Calculates the meanPathDelay value when this message is received if twoStepFlag in flagField of the most recently received Pdelay_Resp message was TRUE (two-step clock).
	Management	Transmits Management messages by software through the PTPEDMAC.
	Signaling	Transmits and receives Signaling messages by software through the PTPEDMAC.

(2) Slave

PTP messages are transmitted and received as described in Table 30.14 in operation as a P2P slave, and the calculated offsetFromMaster is used to correct the local time information.

Table 30.12 E2E从站对PTP消息的处理

消息类型	Message	The EPTPC...
Event	Sync	如果flagField中的twoStepFlag为FALSE（1步时钟），则在收到此消息时计算offsetFromMaster值。
	Delay_Req	以从0到指定时间的随机间隔发送Delay_Req消息 SYTLIR.DREQ[7:0] bits × 2.
	Pdelay_Req	—
	Pdelay_Resp	—
General	Announce	软件通过PTPEDMAC传输Announce消息。
	Follow_Up	如果最近收到的Sync消息的flagField中的twoStepFlag为TRUE（两步时钟），则在收到此消息时计算offsetFromMaster值。
	Delay_Resp	收到此消息时计算meanPathDelay值。
	Pdelay_Resp_Follow_Up	—
	Management	软件通过PTPEDMAC发送和接收管理消息。
	Signaling	软件通过PTPEDMAC发送和接收信令消息。

30.3.5.2 Peer-to-Peer (P2P)

(1) Master

PTP消息的发送和接收如表30.13中所述，作为点对点(P2P)主机运行。

Table 30.13 P2P主机处理PTP消息

数据包类型	Message	The EPTPC...
Event	Sync	以指定的固定间隔传输时间戳以进行传输 SYTLIR.SYNC[7:0] bits.
	Delay_Req	—
	Pdelay_Req	以SYTLIR.DREQ[7:0]位中指定的固定间隔发送Pdelay_Req消息 当收到此消息时，发送Pdelay_Resp消息作为响应。
	Pdelay_Resp	将此作为对接收到的Pdelay_Req消息的响应进行传输 如果flagField中的twoStepFlag为FALSE（单步时钟），则计算收到此消息时的meanPathDelay值。
General	Announce	以SYTLIR.ANCE[7:0]位中指定的固定间隔发送Announce消息。
	Follow_Up	—
	Delay_Resp	—
	Pdelay_Resp_Follow_Up	如果最近收到的Pdelay_Resp消息的flagField中的twoStepFlag为TRUE（两步时钟），则计算收到此消息时的meanPathDelay值。
	Management	通过PTPEDMAC由软件传输管理消息。
	Signaling	软件通过PTPEDMAC传输信令消息。

(2) Slave

PTP消息的发送和接收如表30.14所述，作为P2P从设备运行，计算出的offsetFromMaster用于校正本地时间信息。

Table 30.14 Processing of PTP messages by a P2P slave

Packet type	Message	The EPTPC...
Event	Sync	Calculates the offsetFromMaster value when this message is received if twoStepFlag in flagField was FALSE (1-step clock).
	Delay_Req	—
	Pdelay_Req	• Transmits Pdelay_Req messages at the fixed interval specified in the SYTLIR.DREQ[7:0] bits • Transmits a Pdelay_Resp message in response when this message is received.
	Pdelay_Resp	• Transmits this as the response to a received Pdelay_Req messages • Calculates the meanPathDelay value when this message is received if twoStepFlag in flagField was FALSE (one-step clock).
General	Announce	Transmits Announce messages by software through the PTPEDMAC.
	Follow_Up	Calculates the offsetFromMaster value when this message is received if twoStepFlag in flagField of the most recently received Sync message was TRUE (two-step clock).
	Delay_Resp	—
	Pdelay_Resp_Follow_Up	Calculates the meanPathDelay value when this message is received if twoStepFlag in flagField of the most recently received Pdelay_Resp message was TRUE (2-step clock).
	Management	Transmits and receives Management messages by software through the PTPEDMAC.
	Signaling	Transmits and receives Signaling messages by software through the PTPEDMAC.

30.3.5.3 Ordinary Clock (OC)

PTP messages are transmitted and received through one Ethernet port in operation as an ordinary clock. An ordinary clock operates as the grand master clock or as a slave clock in the master-slave hierarchy. For operation as an E2E master, E2E slave, P2P master, or P2P slave, see the following sections:

- section 30.3.7, Operation as an E2E Master
- section 30.3.8, Operation as an E2E Slave
- section 30.3.10, Operation as a P2P Master
- section 30.3.11, Operation as a P2P Slave.

30.3.6 EPTPC Initialization

Transmitting and receiving PTP messages requires the settings in the EPTPC registers listed in Table 30.15. Set the registers associated with the Ethernet port used. Also set the registers listed in Table 30.16 if UDP and IPv4 are used for the frame format of the PTP messages.

Table 30.15 Registers requiring settings for EPTPC initialization (1 of 2)

Register name	Settings	Description
STCFR	Example: 0000_0002h	The value of 50 MHz is given as an example. Three other settings are also available.
SYCONFR	Example: 0000_0028h	The setting differs with the type of PTP clock operation.
SYMACRU, SYMACRL	As wanted	—
SYSPVRR	0000_0002h	transportSpecific and version fields
SYDOMR	As wanted	—
SYCIDRU, SYCIDRL	As wanted	—
SYPNUMR	0000_0001h	If the PTP clock operates as an OC, the setting is 0000_0001h.
PPMACRU, PPMACRL	01:1B:19:00:00:00	MAC address for PTP-primary messages
PDMACRU, PDMACRL	01:80:C2:00:00:0E	MAC address for PTP-pdelay messages
DASYMRU, DASYMRL	0000_0000h	—
TSLATR	As wanted	Depends on the link transfer rate and STCA clock frequency

Table 30.14 P2P从站处理PTP消息

数据包类型	Message	The EPTPC...
Event	Sync	如果flagField中的twoStepFlag为FALSE（1步时钟），则在收到此消息时计算offsetFromMaster值。
	Delay_Req	—
	Pdelay_Req	以SYTLIR.DREQ[7:0]位中指定的固定间隔发送Pdelay_Req消息 当收到此消息时，发送Pdelay_Resp消息作为响应。
	Pdelay_Resp	将此作为对接收到的Pdelay_Req消息的响应进行传输 如果flagField中的twoStepFlag为FALSE（单步时钟），则计算收到此消息时的meanPathDelay值。
General	Announce	软件通过PTPEDMAC传输Announce消息。
	Follow_Up	如果最近收到的Sync消息的flagField中的twoStepFlag为TRUE（两步时钟），则在收到此消息时计算offsetFromMaster值。
	Delay_Resp	—
	Pdelay_Resp_Follow_Up	如果最近收到的Pdelay_Resp消息的flagField中的twoStepFlag为TRUE（2步时钟），则计算收到此消息时的meanPathDelay值。
	Management	软件通过PTPEDMAC发送和接收管理消息。
	Signaling	软件通过PTPEDMAC发送和接收信令消息。

30.3.5.3 普通时钟(OC)

PTP消息通过一个以太网端口作为普通时钟进行传输和接收。普通时钟作为主时钟或主从层次结构中的从时钟运行。对于作为E2E主站、E2E从站、P2P主站或P2P从站的操作，请参阅以下部分：

- 第30.3.7节，作为E2E主站操作
- 第30.3.8节，作为E2E从站操作
- 第30.3.10节，作为P2P主机操作
- 第30.3.11节，作为P2P从站操作。

30.3.6 EPTPC Initialization

发送和接收PTP消息需要在表30.15中列出的EPTPC寄存器中进行设置。设置与使用的以太网端口相关的寄存器。如果UDP和IPv4用于PTP消息的帧格式，还要设置表30.16中列出的寄存器。

Table 30.15 需要设置EPTPC初始化的寄存器(1of2)

注册名称	Settings	Description
STCFR	Example: 0000_0002h	以50MHz的值为例。还可以使用其他三种设置。
SYCONFR	Example: 0000_0028h	该设置因PTP时钟操作的类型而异。
SYMACRU, SYMACRL	随心所欲	—
SYSPVRR	0000_0002h	transportSpecific和版本字段
SYDOMR	随心所欲	—
SYCIDRU, SYCIDRL	随心所欲	—
SYPNUMR	0000_0001h	如果PTP时钟作为OC运行，则设置为0000_0001h。
PPMACRU, PPMACRL	01:1B:19:00:00:00	PTP主要消息的MAC地址
PDMACRU, PDMACRL	01:80:C2:00:00:0E	PTP-pdelay消息的MAC地址
DASYMRU, DASYMRL	0000_0000h	—
TSLATR	随心所欲	取决于链路传输速率和STCA时钟频率

Table 30.15 Registers requiring settings for EPTPC initialization (2 of 2)

Register name	Settings	Description
SYFORMR	As wanted	Four settings are available.
SYLLCCTLR	0000_0003h	LLC-CTL field value for Ethernet frames
PETYPER	0000_88F7h	Ethertype for PTP messages

Table 30.16 Registers requiring additional settings when UDP or IPv4 is used

Register name	Settings	Description
SYIPADDRR	As wanted	Local IP address
PETOSR	As wanted	Set the highest allowable traffic class selector codepoint as the value for the differentiated service (DS) field.
PGTOSR	As wanted	—
PPTTLR	As wanted	TTL field value for PTP-primary messages
PEUDPR	0000_013Fh	UDP port number for event messages
PGUDPR	0000_0140h	UDP port number for general messages
PDIPR	0000_006Bh	IP address for PTP-pdelay messages
PDTTLR	0000_0001h	TTL field value for PTP-pdelay messages

In operation as an OC, set registers as shown in Figure 30.7 to transfer received Announce, Management, and Signaling messages to the PTPEDMAC.

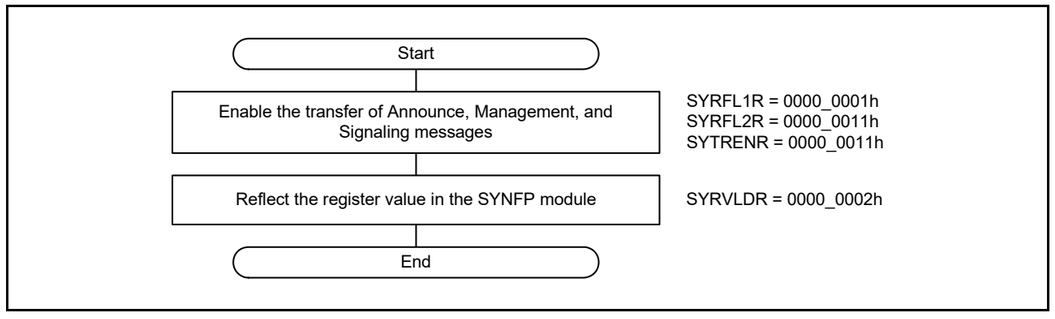


Figure 30.7 Shared settings for PTP devices

30.3.7 Operation as an E2E Master

30.3.7.1 Preparatory setting

Table 30.17 lists the registers for use in operation as an E2E master. When the EPTPC operates as an OC, set the initial value of the time information in advance. See section 30.2.18, Local Clock Counter Initial Value Register (LCIVRU, LCIVRM, LCIVRL) for this value. To reflect the value set in these registers, you must set the SYRVLDR.STUP or ANUP bit to 1.

Table 30.17 Registers used in E2E master operation (1 of 2)

Register name	SYRVLDR register bits used for loading direction	Settings	Description
SYNFR	STUP	0000_0000h	flagField for Sync messages
SYTLIR	STUP ANUP	Example: 0000_0001h	Delay_Resp: 1 s Sync: 1 s Announce: 2 s
ANFR	ANUP	0000_0000h	flagField for Announce messages
GMPR	ANUP	As wanted	—

Table 30.15 需要设置EPTPC初始化的寄存器(2of2)

注册名称	Settings	Description
SYFORMR	随心所欲	有四种设置可用。
SYLLCCTLR	0000_0003h	以太网帧的LLC-CTL字段值
PETYPER	0000_88F7h	PTP消息的以太网类型

Table 30.16 使用UDP或IPv4时需要额外设置的寄存器

注册名称	Settings	Description
SYIPADDRR	随心所欲	本地IP地址
PETOSR	随心所欲	将允许的最高流量类别选择器代码点设置为区分服务(DS)字段的值。
PGTOSR	随心所欲	—
PPTTLR	随心所欲	PTP主要消息的TTL字段值
PEUDPR	0000_013Fh	事件消息的UDP端口号
PGUDPR	0000_0140h	一般消息的UDP端口号
PDIPR	0000_006Bh	PTP-pdelay消息的IP地址
PDTTLR	0000_0001h	PTP-pdelay消息的TTL字段值

在作为OC运行时，如图30.7所示设置寄存器以将接收到的Announce、Management和Signaling消息传输到PTP EDMAC。

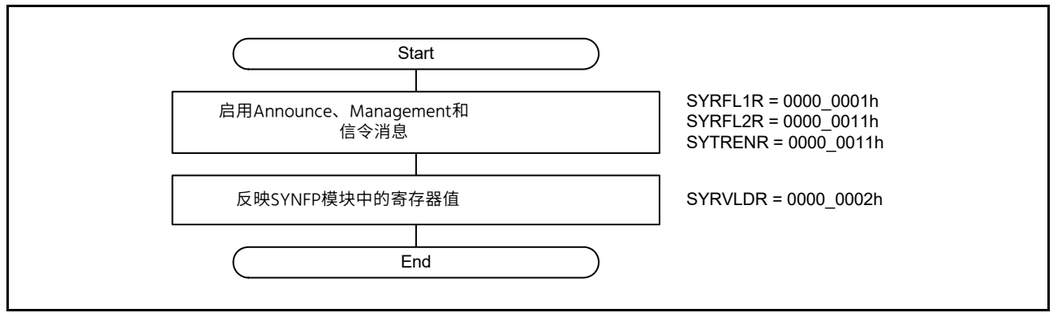


Figure 30.7 PTP设备的共享设置

30.3.7 作为E2E主站操作

30.3.7.1 预备设置

表30.17列出了作为E2E主机运行时使用的寄存器。当EPTPC作为OC运行时，请预先设置时间信息的初始值。有关该值，请参见第30.2.18节，本地时钟计数器初始值寄存器（LCIVRU、LCIVRM、LCIVRL）。要反映这些寄存器中设置的值，您必须设置SYRVLDR.STUP或

ANUP位为1。

Table 30.17 E2E主机操作中使用的寄存器(1of2)

注册名称	用于加载方向的SYRVLDR寄存器位	Settings	Description
SYNFR	STUP	0000_0000h	同步消息的标志字段
SYTLIR	STUP ANUP	Example: 0000_0001h	Delay_Resp: 1 s Sync: 1 s Announce: 2 s
ANFR	ANUP	0000_0000h	公告消息的标志字段
GMPR	ANUP	随心所欲	—

Table 30.17 Registers used in E2E master operation (2 of 2)

Register name	SYRVLDR register bits used for loading direction	Settings	Description
GMCQR	ANUP	As wanted	—
GMIDRU, GMIDRL	ANUP	As wanted	—
CUOTSR	ANUP	As wanted	timeSource: Internal Oscillator
SRR	ANUP	As wanted	• If the EPTPC operates as a master, set this register to 0000_0000h • If the EPTPC operates as a slave, set this register to the StepsRemoved field value of Announce messages received by the slave plus one
SYRFL1R	STUP	0000_4001h	Enables the processing of Delay_Req messages by the SYNFP module
SYRFL2R	STUP	0000_0011h	Enables the transfer of Signaling and Management messages to the PTPEDMAC
SYTRENR	STUP	0000_0011h	Enables the transmission of Sync and Announce messages

30.3.7.2 Procedure for starting operations

Figure 30.8 shows the procedure for settings to start operation as an E2E master.

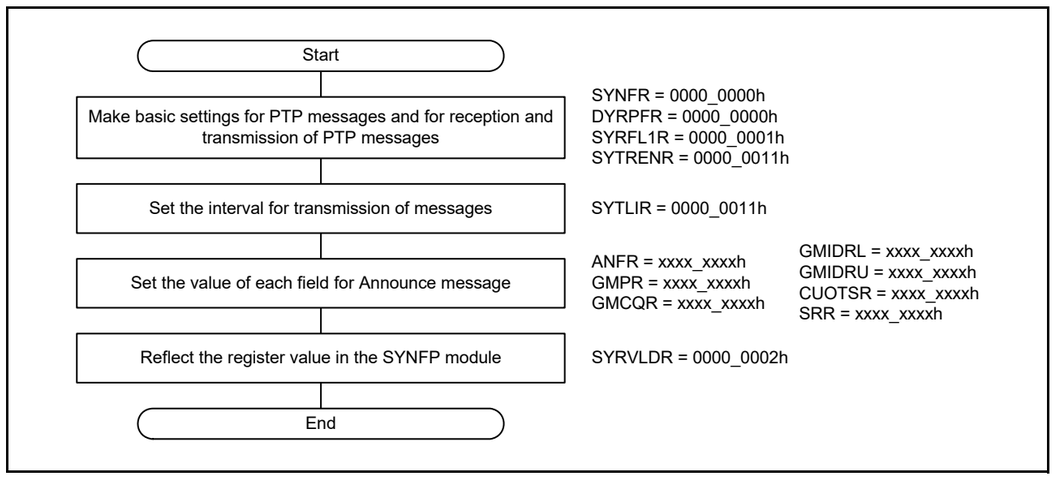


Figure 30.8 Procedure for starting operation as an E2E master

30.3.7.3 Procedure for changing the settings

Increases in the frequency of receiving Delay_Req messages caused by network conditions might lead to an overflow of the FIFO buffer that receives the Delay_Req messages. In such cases, change the value of the logMessageInterval field of Delay_Resp messages so that the slave sending the Delay_Req messages lengthens the interval between the messages. Figure 30.9 shows the procedure for changing the value of the logMessageInterval field.

Table 30.17 E2E主机操作中使用的寄存器(2of2)

注册名称	用于加载方向的SYRVLDR寄存器位	Settings	Description
GMCQR	ANUP	随心所欲	—
GMIDRU, GMIDRL	ANUP	随心所欲	—
CUOTSR	ANUP	随心所欲	timeSource：内部振荡器
SRR	ANUP	随心所欲	如果EPTPC作为主机运行，则将此寄存器设置为0000_0000h 如果EPTPC作为从机运行，则将此寄存器设置为从机收到的Announcemessages的StepsRemoved字段值加一
SYRFL1R	STUP	0000_4001h	启用对Delay_Req消息的处理 SYNFP module
SYRFL2R	STUP	0000_0011h	允许将信令和管理消息传输到PTPEDMAC
SYTRENR	STUP	0000_0011h	启用同步和公告消息的传输

30.3.7.2 开始操作的程序

图30.8显示了作为E2E主机开始操作的设置过程。

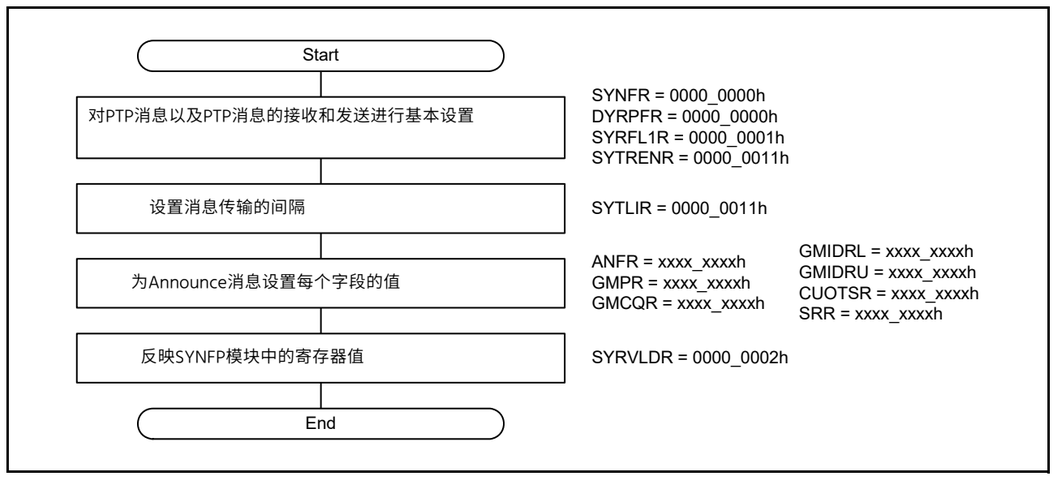


Figure 30.8 开始作为E2E主站运行的步骤

30.3.7.3 更改设置的步骤

网络条件导致接收Delay_Req消息的频率增加可能导致接收Delay_Req消息的FIFO缓冲区溢出。在这种情况下，请更改Delay_Resp消息的logMessageInterval字段的值，以使发送Delay_Req消息的从站延长消息之间的间隔。图30.9显示了更改logMessageInterval字段值的过程。

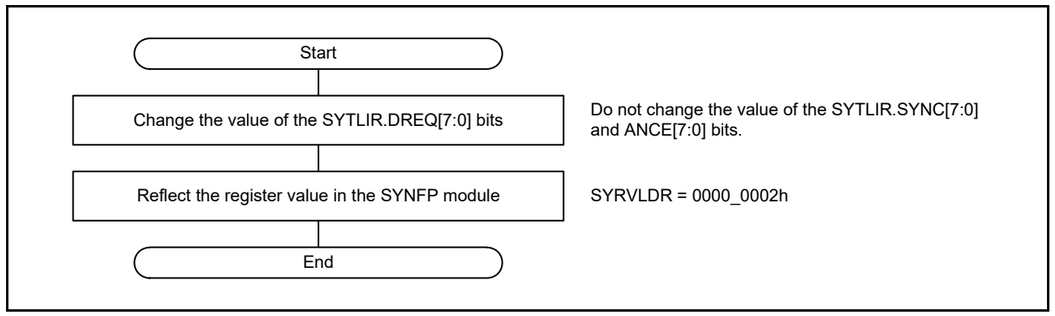


Figure 30.9 Procedure for changing the value of the logMessageInterval Field for Delay_Resp messages

30.3.7.4 Procedure for stopping operations

Figure 30.10 shows the procedure for stopping operation as an E2E master. To confirm that the operation is completely stopped, read the SYSR.GENDN and RESDN flags to check that generation of messages and sending of responses are completely stopped.

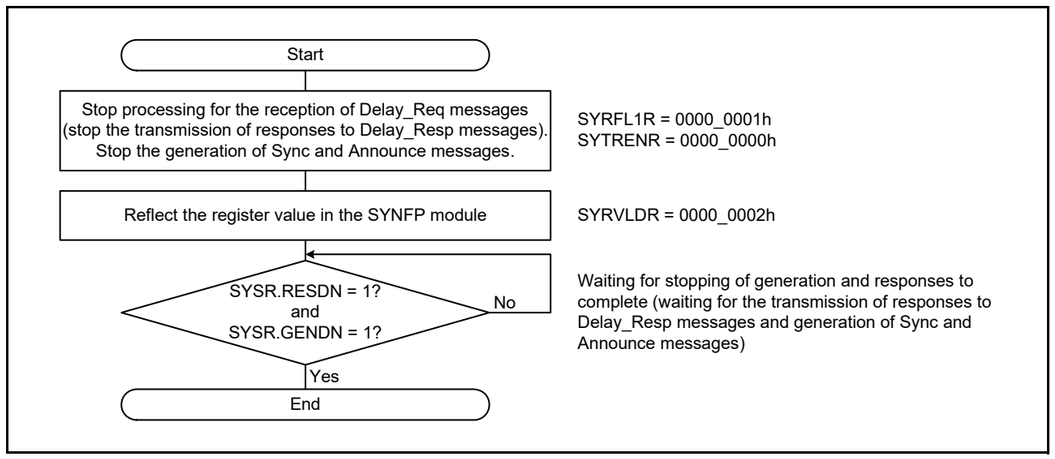


Figure 30.10 Procedure for stopping operation as an E2E master

30.3.8 Operation as an E2E Slave

30.3.8.1 Preparatory settings

Table 30.18 lists the registers for use in operation as an E2E slave. To reflect the value set in the register in SYNFP operations, you must set the SYRVLDR.STUP, ANUP, or BMUP bit to 1.

Table 30.18 Registers used in E2E slave operation (1 of 2)

Register name	SYRVLDR register bits used for loading direction	Settings	Description
MTCID	BMUP	As wanted	clockIdentity value of the master clock that provides synchronization
MTPID	BMUP	As wanted	portNumber value of the master clock that provides synchronization
SYTLIR	ANUP BMUP	Example: 0000_0000h	Delay_Resp: 1 s*1

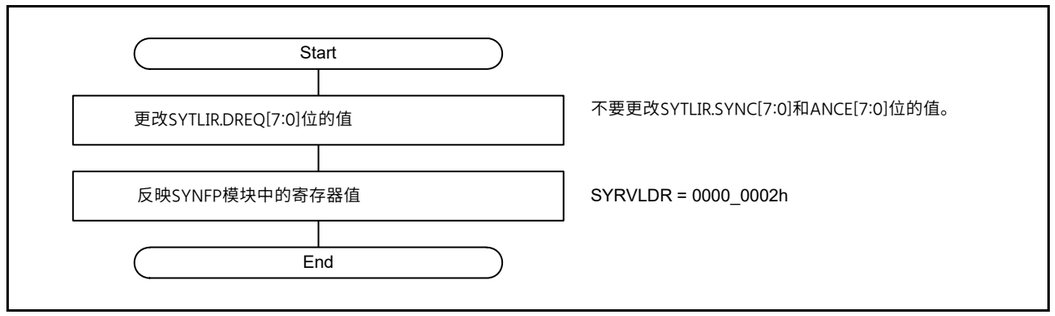


Figure 30.9 更改Delay_Resp消息的logMessageInterval字段值的过程

30.3.7.4 停止操作的程序

图30.10显示了作为E2E主站停止操作的过程。要确认操作完全停止，请阅读SYSR.GENDN和RESDN标志以检查消息的生成和响应的发送是否完全停止。

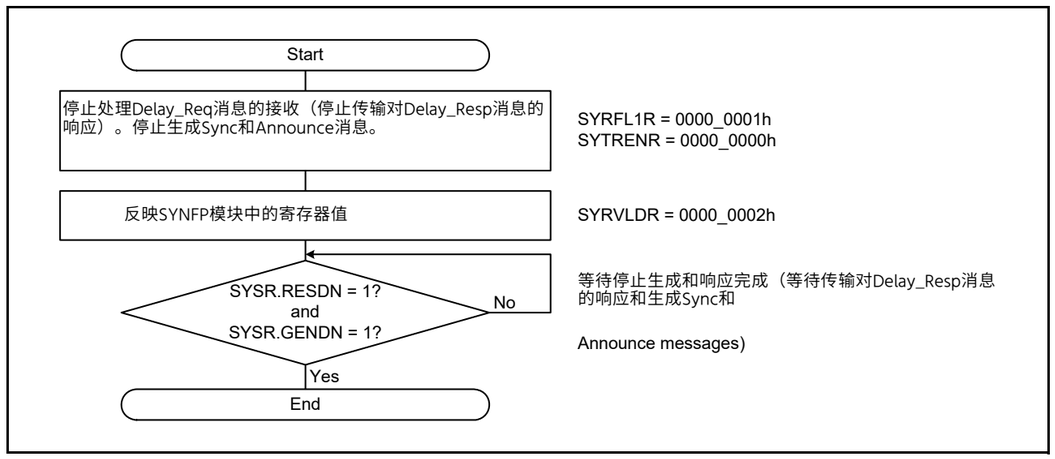


Figure 30.10 停止作为E2E主站运行的步骤

30.3.8 作为E2E从站运行

30.3.8.1 准备设置

表30.18列出了用作E2E从机的寄存器。要在SYNFP操作中反映寄存器中设置的值，您必须将SYRVLDR.STUP、ANUP或BMUP位设置为1。

Table 30.18 E2E从机操作中使用的寄存器(1of2)

注册名称	用于加载方向的SYRVLDR寄存器位	Settings	Description
MTCID	BMUP	随心所欲	提供同步的主时钟的clockIdentity值
MTPID	BMUP	随心所欲	portNumber提供同步的主时钟的值
SYTLIR	ANUP BMUP	Example: 0000_0000h	Delay_Resp: 1 s*1

Table 30.18 Registers used in E2E slave operation (2 of 2)

Register name	SYRVLDR register bits used for loading direction	Settings	Description
RSTOUTR	STUP	As wanted	—
SYNTOR	—	As wanted	—
SYRFL1R	STUP	0004_0441h	Enables reception of Delay_Resp, Follow_Up, and Sync messages and transfer of Announce messages to the PTPEDMAC
SYRFL2R	STUP	0000_0011h	Enables transfer of Signaling and Management messages to the PTPEDMAC
SYTRENR	STUP	0000_0100h	Enables the generation of Delay_Req messages

Note 1. During the reception of Delay_Resp messages by an E2E slave, the SYTLIR.DREQ[7:0] bits must be adjusted if the value of the SYRLIR.DRESP[7:0] flags is to be altered. The SYTLIR.DREQ[7:0] bits specify a value in the range from -7 to +6. Set the SYTLIR.DREQ[7:0] bits to -7 if the value indicated in the SYRLIR.DRESP[7:0] flags is less than or equal to -8 and to 6 if the value indicated in the SYRLIR.DRESP[7:0] flags is greater than or equal to 7.

30.3.8.2 Procedure for starting operations

Figure 30.11 shows the procedure for settings to start operation as an E2E slave.

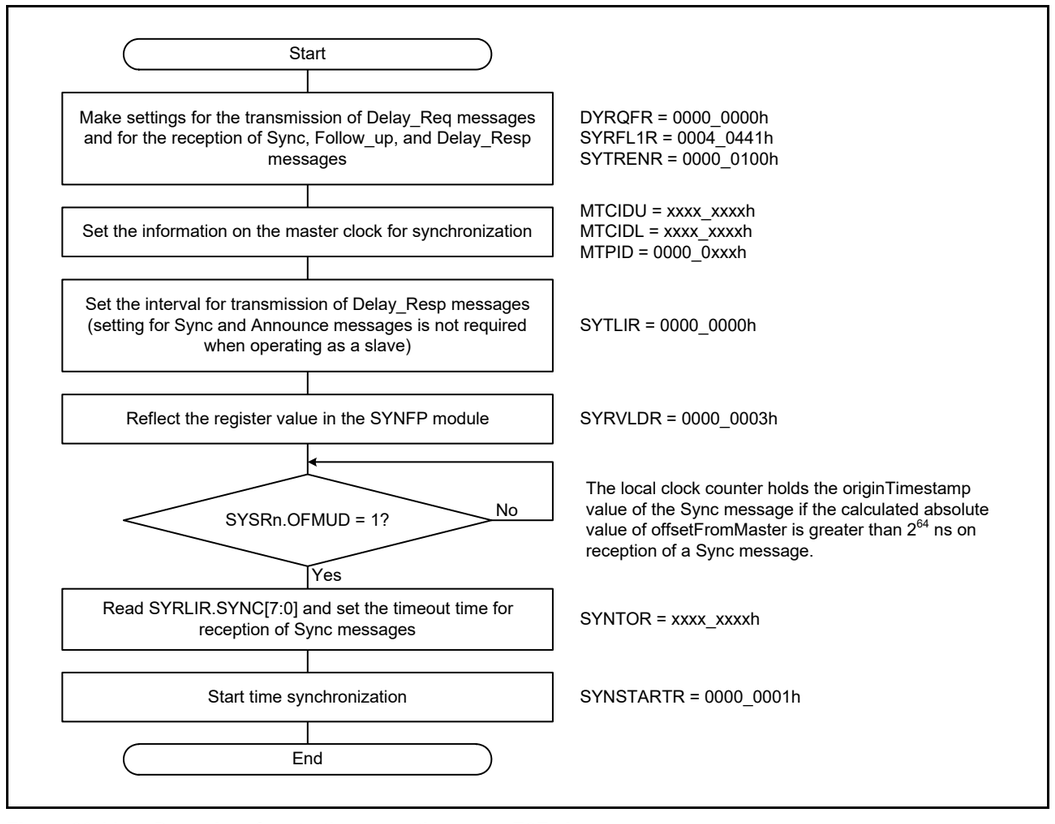


Figure 30.11 Procedure for starting operation as an E2E slave

Table 30.18 E2E从机操作中使用的寄存器(2of2)

注册名称	用于加载方向的SYRVLDR寄存器位	Settings	Description
RSTOUTR	STUP	随心所欲	—
SYNTOR	—	随心所欲	—
SYRFL1R	STUP	0004_0441h	允许接收Delay_Resp、Follow_Up和Sync消息并将Announce消息传输到PTPEDMAC
SYRFL2R	STUP	0000_0011h	允许将信令和管理消息传输到PTPEDMAC
SYTRENR	STUP	0000_0100h	启用Delay_Req消息的生成

Note 1. 在E2E从站接收Delay_Resp消息期间，如果要更改SYRLIR.DRESP[7:0]标志的值，则必须调整SYTLIR.DREQ[7:0]位。SYTLIR.DREQ[7:0]位指定范围从-7到+6的值。如果SYRLIR.DRESP[7:0]标志中指示的值小于或等于-8，则将SYTLIR.DREQ[7:0]位设置为-7，如果SYRLIR.DRESP[中指示的值，则设置为67:0]flags大于或等于7。

30.3.8.2 开始操作的程序

图30.11显示了作为E2E从站启动操作的设置过程。

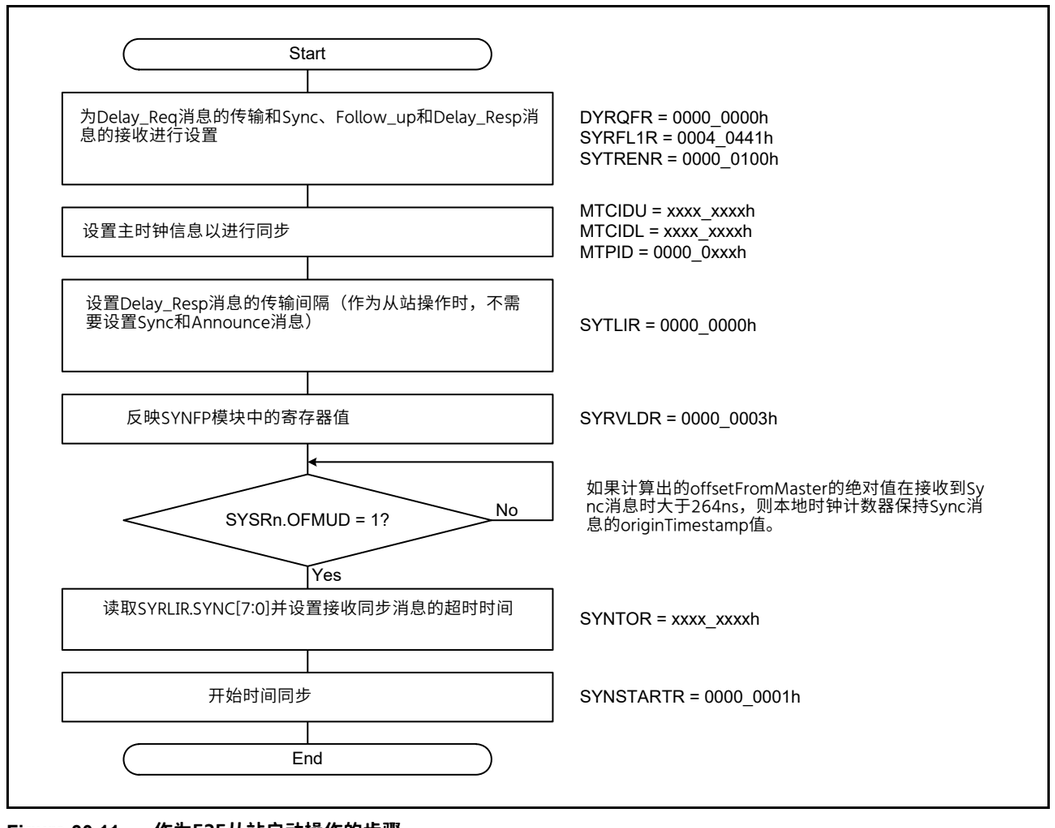


Figure 30.11 作为E2E从站启动操作的步骤

30.3.8.3 Procedure for changing the settings

IEEE 1588 stipulates that the average interval for the transmission of Delay_Req messages must be adjusted in response to changes in the value of the logMessageInterval field of received Delay_Resp messages. The EPTPC sets the SYSR.INTCHG flag to 1 if the logMessageInterval value of a received message differs from that of the previous message. When this happens, the application must set the SYTLIR.DREQ[7:0] bits to the value in the SYRLIR.DRESP[7:0] bits. The SYTLIR.DREQ[7:0] bits specify a value in the range from -7 to +6. Set the SYTLIR.DREQ[7:0] bits to -7 if the value indicated in the SYRLIR.DRESP[7:0] flags is less than or equal to -8 and to 6 if the value indicated in the SYRLIR.DRESP[7:0] bits is greater than or equal to 7.

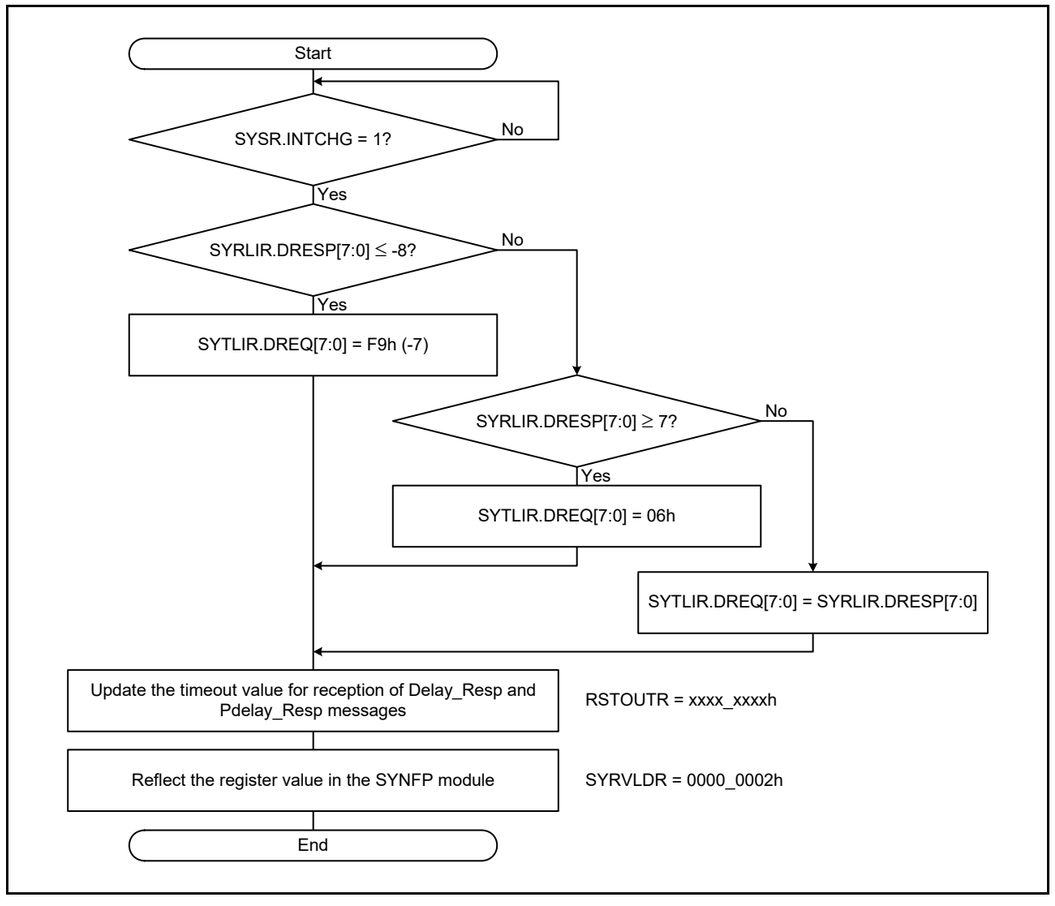


Figure 30.12 Procedure for changing the transmission interval for Delay_Req messages

30.3.8.4 Procedure for stopping operations

Figure 30.13 shows the procedure for stopping operation as an E2E slave. To confirm that operation as an E2E slave is completely stopped, read the SYSR.GENDN flag to check that generation is completely stopped.

30.3.8.3 更改设置的步骤

IEEE1588规定，必须根据接收到的Delay_Resp消息的logMessageInterval字段值的变化来调整传输Delay_Req消息的平均间隔。如果接收到的消息的logMessageInterval值与前一个消息的值不同，则EPTPC将SYSR.INTCHG标志设置为1。发生这种情况时，应用程序必须将SYTLIR.DREQ[7:0]位设置为SYRLIR.DRESP[7:0]位中的值。SYTLIR.DREQ[7:0]位指定范围从-7到+6的值。设置

如果SYRLIR.DRESP[7:0]标志中指示的值小于或等于-8，则SYTLIR.DREQ[7:0]位为-7；如果SYRLIR.DRESP[7]中指示的值，则为6：0]位大于等于7。

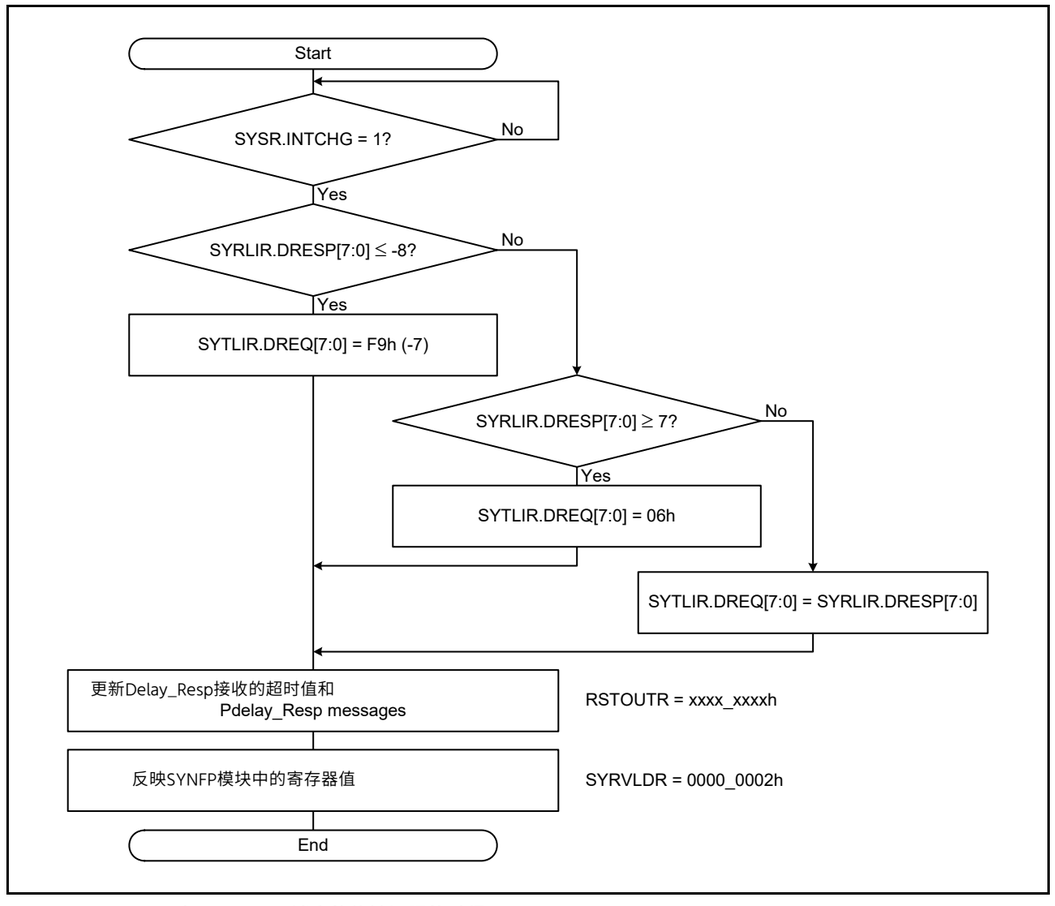


Figure 30.12 更改Delay_Req消息的传输间隔的过程

30.3.8.4 停止操作的程序

图30.13显示了作为E2E从站停止操作的过程。要确认作为E2E从站的操作已完全停止，请读取SYSR.GENDN标志以检查生成是否已完全停止。

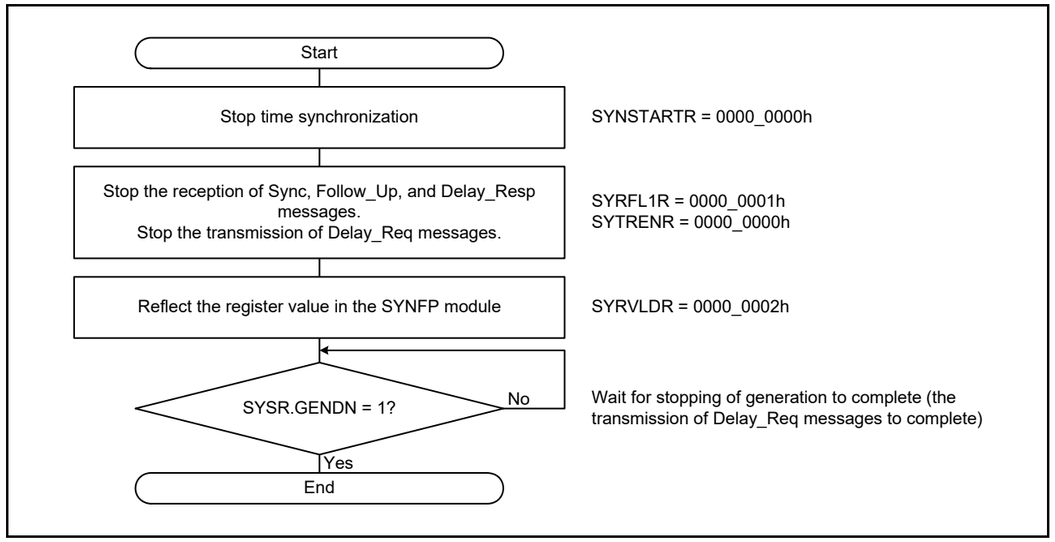


Figure 30.13 Procedure for stopping operation as an E2E slave

30.3.9 P2P Operation (Shared by Master and Slave)

Table 30.19 lists the registers for use in P2P operation. When the EPTPC is to be operated with P2P protocol, the SYNFP module handles the processing of PTP-pdelay messages regardless of whether operation is as a master or slave. The interval for Pdelay_Req transmission and the parameters for monitoring of Pdelay_Resp messages must be set at the same time.

Table 30.19 Registers for use in P2P operation

Register name	SYRVLDR register bits used for loading direction	Settings	Description
MTCID	BMUP	As wanted	clockIdentity value of the synchronized master clock
MTPID	BMUP	As wanted	portNumber value of the synchronized master clock
SYTLIR	ANUP STUP	0000_0000h	Announce: — Sync: — Pdelay_Req: 1 s
RSTOUTR	STUP	As wanted	—
SYRFL1R	STUP	4440_0001h	Enables the reception of Pdelay_Req, Pdelay_Resp, and Pdelay_Resp_Follow_Up messages and the transfer of Announce messages to the PTPEDMAC
SYRFL2R	STUP	0000_0011h	Enables the transfer of Signaling and Management messages to the PTPEDMAC
SYTRENR	STUP	0000_1000h	Enables the generation of Pdelay_Req messages

30.3.9.1 Procedure for starting operations

Figure 30.14 shows the procedure for starting P2P operation (sending and receiving PTP-pdelay messages).

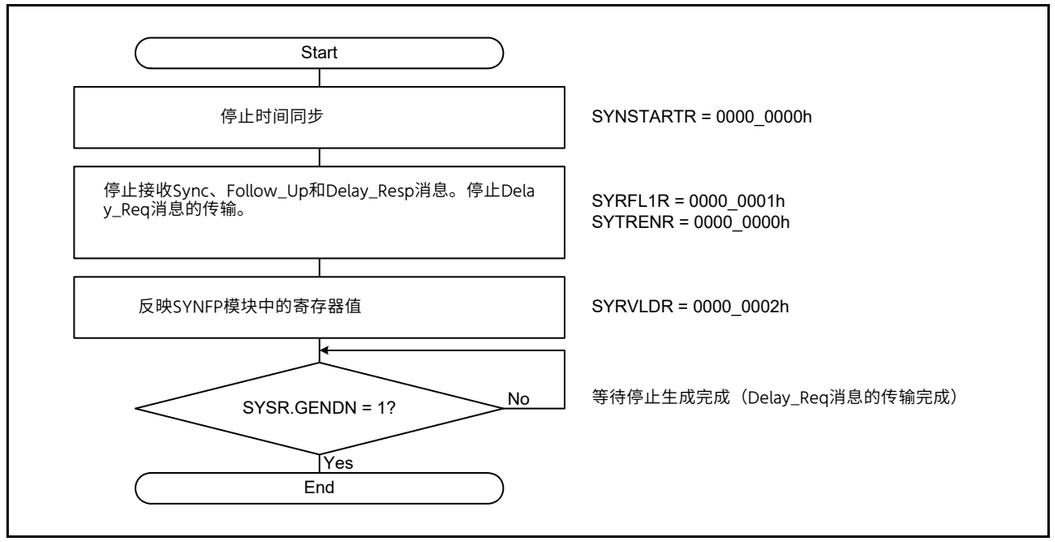


Figure 30.13 停止作为E2E从站运行的步骤

30.3.9 P2P操作（主从共享）

表30.19列出了用于P2P操作的寄存器。当EPTPC以P2P协议运行时，无论是作为主机还是从机，SYNFP模块都会处理PTP-pdelay消息的处理。Pdelay_Req传输的时间间隔和Pdelay_Resp消息的监控参数必须同时设置。

Table 30.19 用于P2P操作的寄存器

注册名称	用于加载方向的SYRVLDR寄存器位	Settings	Description
MTCID	BMUP	随心所欲	同步主时钟的clockIdentity值
MTPID	BMUP	随心所欲	portNumber同步主时钟的值
SYTLIR	ANUP STUP	0000_0000h	Announce: — Sync: — Pdelay_Req: 1 s
RSTOUTR	STUP	随心所欲	—
SYRFL1R	STUP	4440_0001h	启用Pdelay_Req、Pdelay_Resp和Pdelay_Resp_Follow_Up消息和传输向PTPEDMAC发布消息
SYRFL2R	STUP	0000_0011h	允许将信令和管理消息传输到PTPEDMAC
SYTRENR	STUP	0000_1000h	启用Pdelay_Req消息的生成

30.3.9.1 开始操作的程序

图30.14显示了启动P2P操作（发送和接收PTP-pdelay消息）的过程。

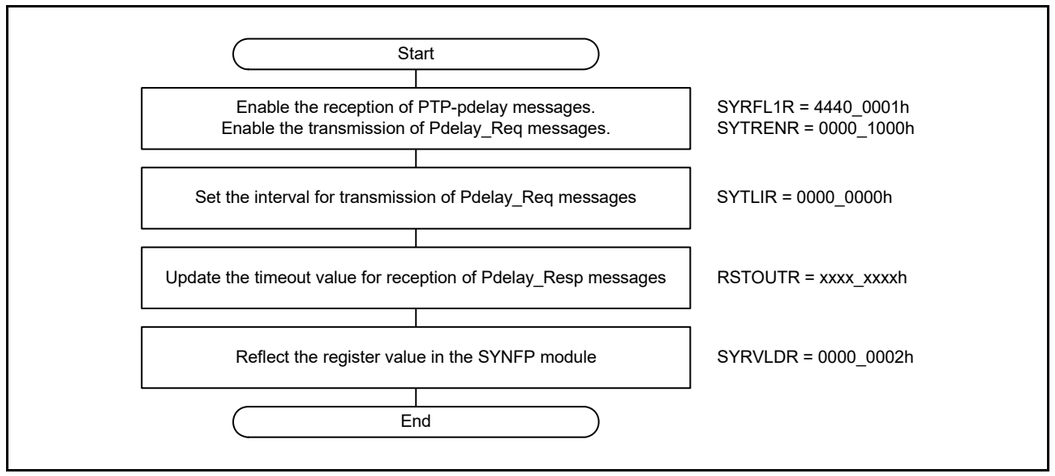


Figure 30.14 Procedure for starting P2P operation

30.3.9.2 Procedure for stopping operations

Figure 30.15 shows the procedure for stopping P2P operation (sending and receiving PTP-pdelay messages).

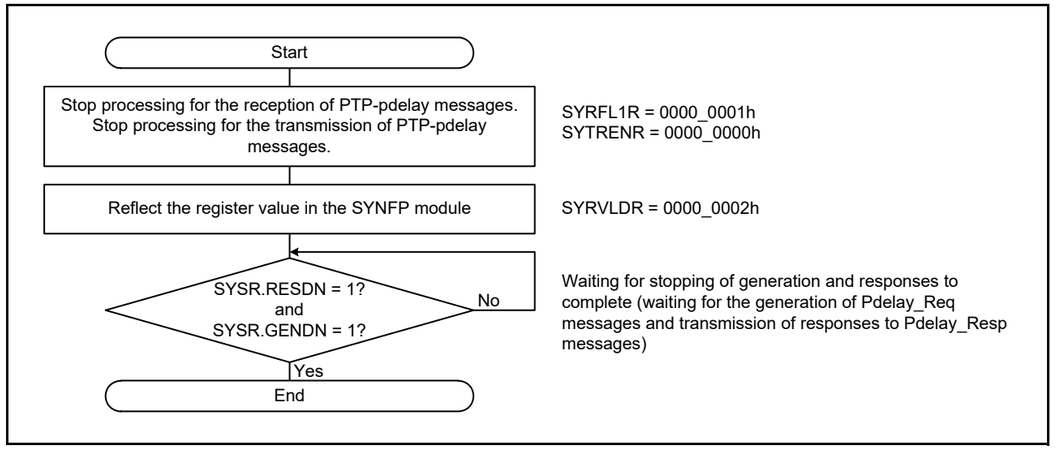


Figure 30.15 Procedure for stopping P2P operation

30.3.10 Operation as a P2P Master

Table 30.20 lists the registers for use in operation as a P2P master. When the EPTPC operates as an OC or BC using both ports as masters, set the initial value of the time information in advance as required. See section 30.2.18, Local Clock Counter Initial Value Register (LCIVRU, LCIVRM, LCIVRL) for this value.

Table 30.20 Registers used in P2P master operation (1 of 2)

Register name	SYRVLDR register bits used for loading direction	Settings	Description
SYCONFR	—	0000_0028h	—
ANFR	ANUP	0000_0000h	flagField for Announce messages
SYNFR	STUP	0000_0000h	flagField for Sync messages

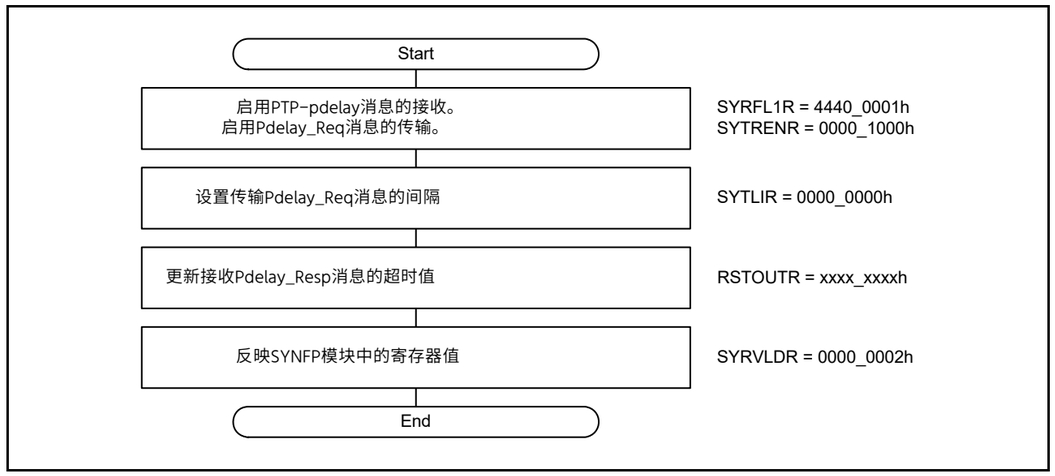


Figure 30.14 开始P2P操作的步骤

30.3.9.2 停止操作的程序

图30.15显示了停止P2P操作（发送和接收PTP-pdelay消息）的过程。

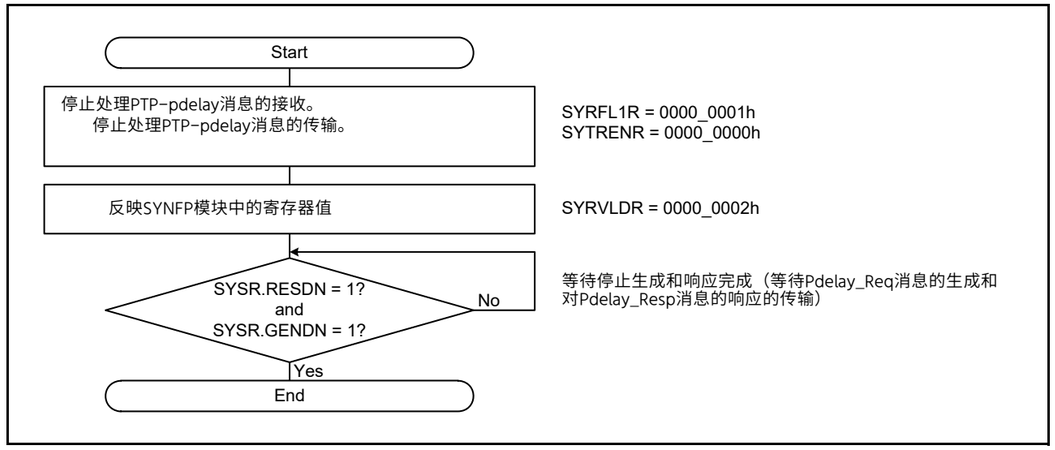


Figure 30.15 停止P2P操作的程序

30.3.10 作为P2P主机操作

表30.20列出了用作P2P主机的寄存器。当EPTPC作为OC或BC使用两个端口作为主机时，请根据需要预先设置时间信息的初始值。有关该值，请参见第30.2.18节，本地时钟计数器初始值寄存器（LCIVRU、LCIVRM、LCIVRL）。

Table 30.20 P2P主机操作中使用的寄存器(1of2)

注册名称	用于加载方向的SYRVLDR寄存器位	Settings	Description
SYCONFR	—	0000_0028h	—
ANFR	ANUP	0000_0000h	公告消息的标志字段
SYNFR	STUP	0000_0000h	同步消息的标志字段

Table 30.20 Registers used in P2P master operation (2 of 2)

Register name	SYRVLDR register bits used for loading direction	Settings	Description
SYTLIR	ANUP STUP	Example: 0000_0001h	Announce: 2 s Sync: 1 s Pdelay_Req: 1 s
GMPR	ANUP	As wanted	Grandmaster Priority1 and Priority2
GMCQR	ANUP	As wanted	Grandmaster Quality
GMIDR	ANUP	As wanted	Grandmaster Identity
CUOTSR	ANUP	As wanted	currentUtcOffset, timeSource
SRR	ANUP	As wanted	StepsRemoved
RSTOUTR	STUP	As wanted	—
SYRFL1R	STUP	4440_0000h	Enables the reception of Pdelay_Req, Pdelay_Resp, and Pdelay_Resp_Follow_Up messages
SYRFL2R	STUP	0000_0011h	Enables the transfer of Signaling and Management messages to the PTPEDMAC
SYTRENR	STUP	0000_1011h	Enables the transmission of Pdelay_Req, Sync, and Announce messages

30.3.10.1 Procedure for starting operations

When transmission of Sync and Announce messages is started during P2P operation (sending and receiving PTP-pdelay messages), the EPTPC operates as a P2P master. Figure 30.16 shows the procedure for starting operation as a P2P master.

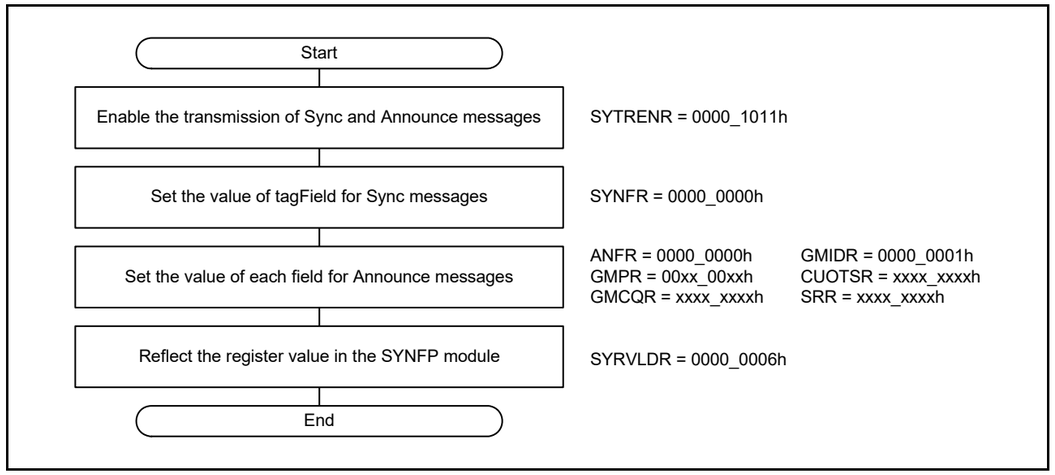


Figure 30.16 Procedure for starting operation as a P2P master

30.3.10.2 Procedure for stopping operations

Figure 30.17 shows the procedure for stopping the transmission of Sync and Announce messages to stop operation as a P2P master.

Table 30.20 P2P主机操作中使用的寄存器(2of2)

注册名称	用于加载方向的SYRVLDR寄存器位	Settings	Description
SYTLIR	ANUP STUP	Example: 0000_0001h	Announce: 2 s Sync: 1 s Pdelay_Req: 1 s
GMPR	ANUP	随心所欲	宗师优先级1和优先级2
GMCQR	ANUP	随心所欲	大师品质
GMIDR	ANUP	随心所欲	宗师身份
CUOTSR	ANUP	随心所欲	currentUtcOffset, timeSource
SRR	ANUP	随心所欲	StepsRemoved
RSTOUTR	STUP	随心所欲	—
SYRFL1R	STUP	4440_0000h	启用Pdelay_Req、Pdelay_Resp和Pdelay_Resp_Follow_Up messages
SYRFL2R	STUP	0000_0011h	允许将信令和管理消息传输到PTPEDMAC
SYTRENR	STUP	0000_1011h	启用Pdelay_Req、Sync和发布消息

30.3.10.1 开始操作的程序

在P2P操作（发送和接收PTP-pdelay消息）期间开始传输Sync和Announce消息时，EPTPC将作为P2P主机运行。图30.16显示了作为P2P主机开始操作的过程。

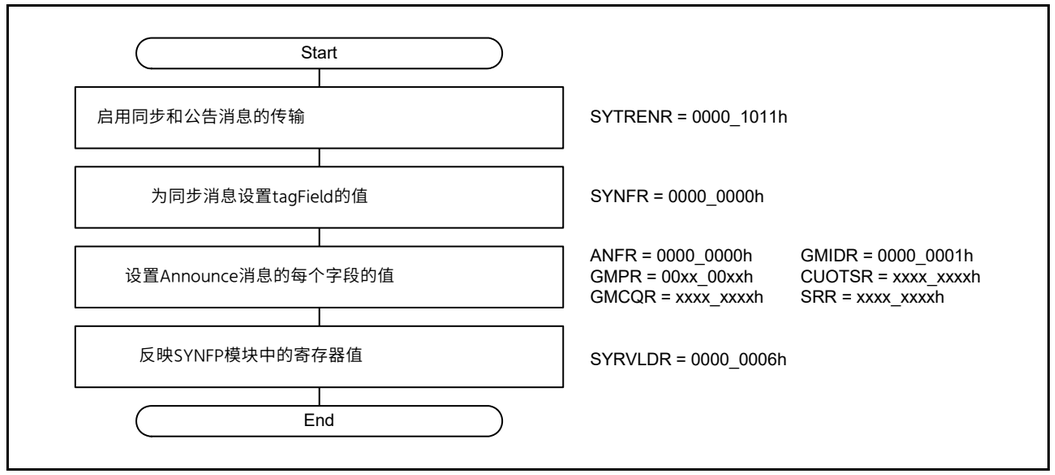


Figure 30.16 作为P2P主机开始操作的步骤

30.3.10.2 停止操作的程序

图30.17显示了停止传输Sync和Announce消息以停止操作的过程
P2P master.

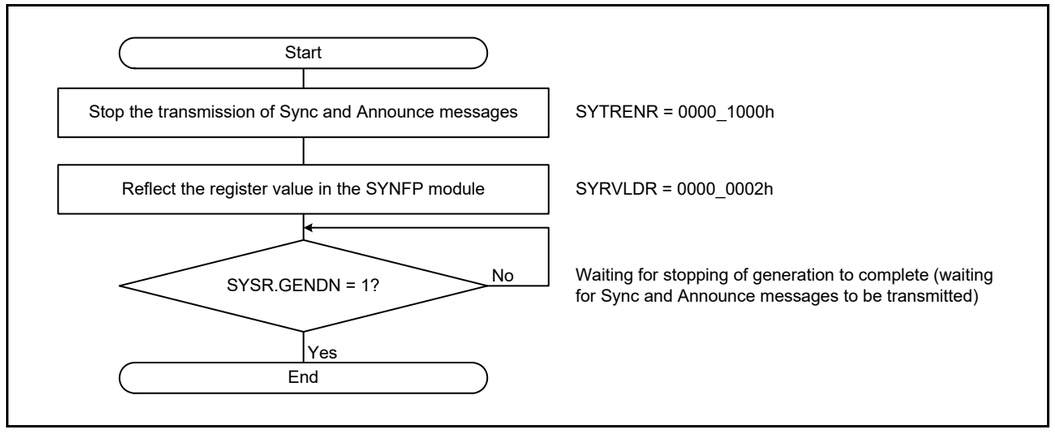


Figure 30.17 Procedure for stopping operation as a P2P master

30.3.11 Operation as a P2P Slave

Table 30.21 lists the registers for use in operation as a P2P slave. Setting a SYNFP module to receive Sync messages and Follow_Up messages during P2P operation results in operation as a P2P slave. Information on the master clock for synchronization must be specified.

Table 30.21 Registers used in P2P slave operation

Register name	SYRVLDR register bits used for loading direction	Settings	Description
MTCID	BMUP	As wanted	clockIdentity value of the synchronized master clock
MTPID	BMUP	As wanted	portNumber value of the synchronized master clock
RSTOUTR	STUP	As wanted	—
SYRFL1R	STUP	4440_0441h	Enables the reception of Pdelay_Req, Pdelay_Resp, Pdelay_Resp_Follow_Up, Follow_Up, and Sync messages and the transfer of Announce messages to the PTPEDMAC

30.3.11.1 Procedure for starting operations

Figure 30.18 shows the procedure for making the additional settings for shifting to slave operation during P2P operation (sending and receiving PTP-pdelay messages).

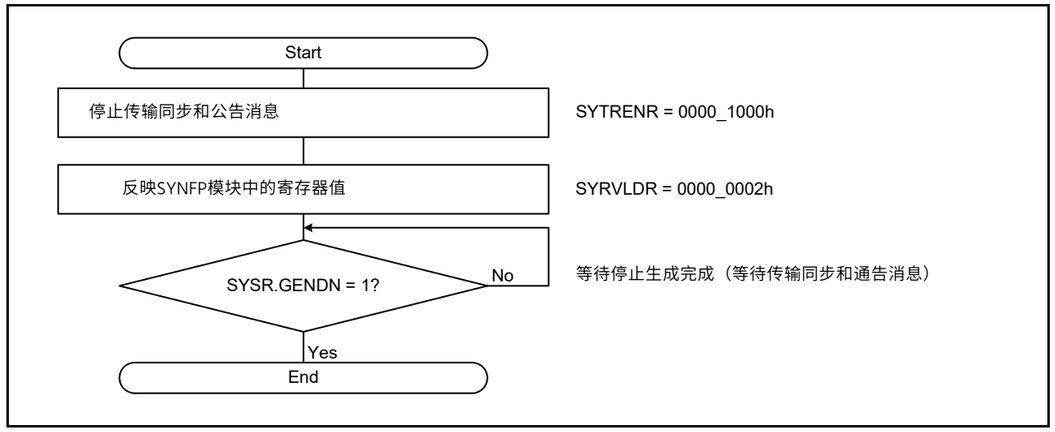


Figure 30.17 作为P2P主机停止操作的步骤

30.3.11 作为P2P从站运行

表30.21列出了用作P2P从机的寄存器。设置SYNFP模块以接收同步消息和P2P操作期间的Follow_Up消息导致作为P2P从站操作。必须指定用于同步的主时钟信息。

Table 30.21 P2P从机操作中使用的寄存器

注册名称	用于加载方向的SYRVLDR寄存器位	Settings	Description
MTCID	BMUP	随心所欲	同步主时钟的clockIdentity值
MTPID	BMUP	随心所欲	portNumber同步主时钟的值
RSTOUTR	STUP	随心所欲	—
SYRFL1R	STUP	4440_0441h	启用Pdelay_Req、Pdelay_Resp、Pdelay_Resp_Follow_Up、Follow_Up和Sync消息以及Announce消息到PTPEDMAC的传输

30.3.11.1 开始操作的程序

图30.18显示了在P2P操作（发送和接收PTP-pdelay消息）期间进行附加设置以转移到从操作的过程。

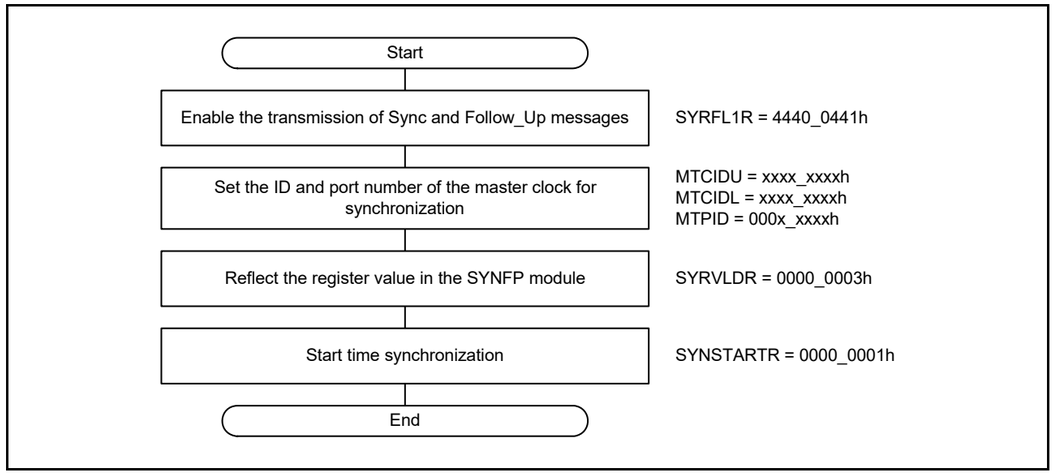


Figure 30.18 Procedure for starting operation as a P2P slave

30.3.11.2 Procedure for stopping operations

Figure 30.19 shows the procedure for stopping the reception of Sync and Follow_Up messages to stop operation as a P2P slave.

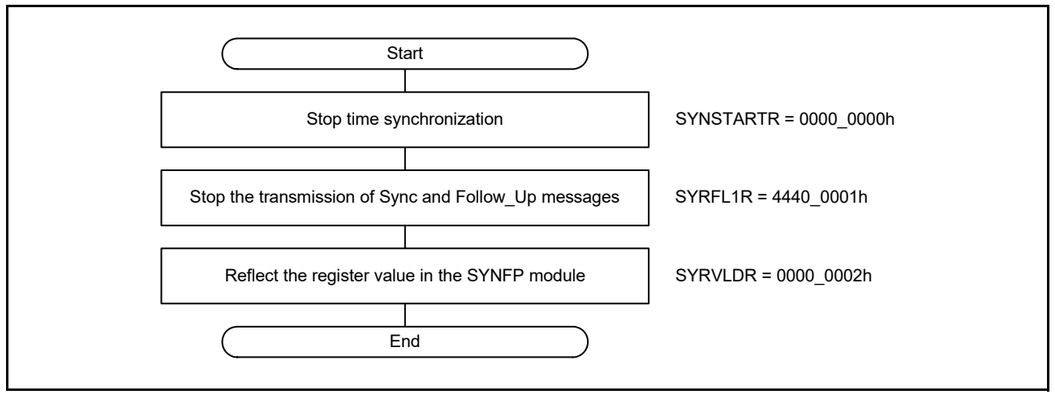


Figure 30.19 Procedure for stopping operation as a P2P slave

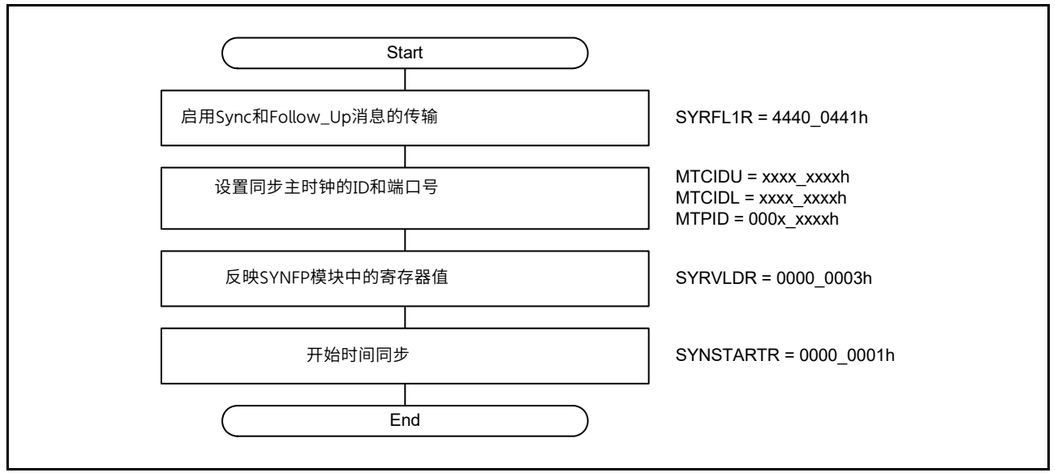


Figure 30.18 作为P2P从站启动操作的步骤

30.3.11.2 停止操作的程序

图30.19显示了停止接收Sync和Follow_Up消息以停止作为P2P从站操作的过程。

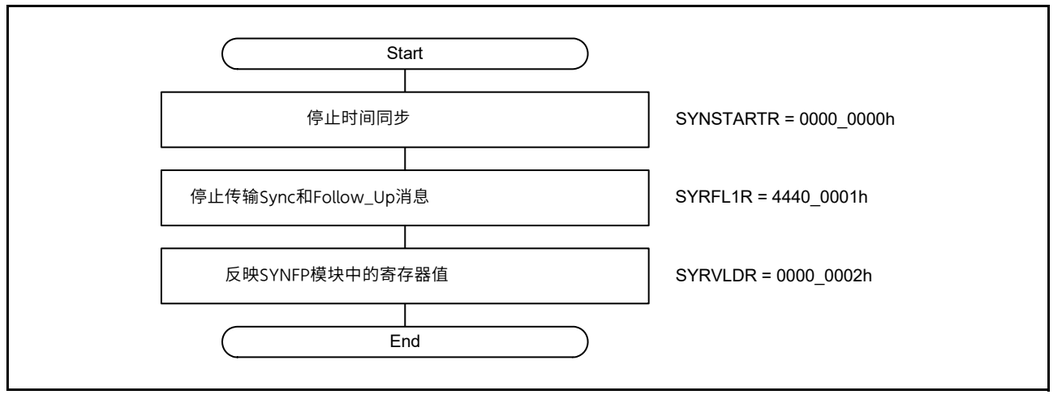


Figure 30.19 停止作为P2P从站运行的步骤

30.3.12 Monitoring of Received Messages

30.3.12.1 Reception of announce messages

The EPTPC does not detect timeouts during the reception of Announce messages. To detect timeouts, monitor the reception of Announce messages by software.

30.3.12.2 Reception of sync messages

The STSR.SYNTOUT flag is set to 1 when a timeout occurs during the reception of a Sync message while correcting time synchronization.

The SYSR.OFMUD flag is set to 1 when a Sync message is received, regardless of whether time synchronization is being corrected. Accordingly, the reception of Sync messages is detectable by referencing this flag even when the correction of time synchronization stops because a timeout occurs during the reception of a Sync message.

30.3.12.3 Reception of Delay_Resp and Pdelay_Resp messages

The SYSR.DRPTO flag is set to 1 when a timeout occurs during the reception of a Delay_Resp message after the transmission of a Delay_Req message while operating as an E2E slave, or when a timeout occurs during the reception of a Pdelay_Resp message after the transmission of a Pdelay_Req message while operating as a P2P.

The SYSR.MPDUD flag is set to 1 when a Delay_Resp or Pdelay_Resp message is received, so the reception of these messages is still detectable when a timeout occurs during reception.

30.3.13 Correcting Time Synchronization

A slave detects differences in the clock gradient relative to the master clock. The offsetFromMaster values calculated using the standard IEEE 1588 algorithm are used to calculate the clock gradient, so the result includes elements of network fluctuation that are not frequency differences. The EPTPC has a worst-10 function to eliminate fluctuations caused by network load and other dynamic conditions. With these functions, the time is corrected from the calculated gradient difference values and results of correction are obtained as shown in Figure 30.21.

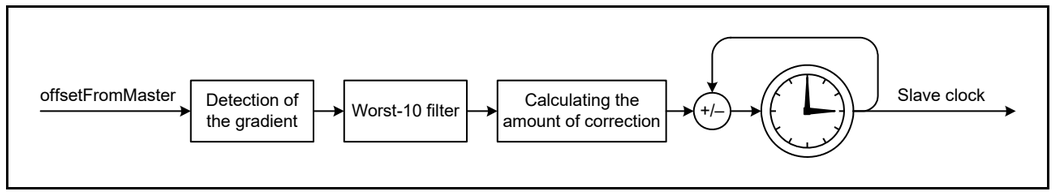


Figure 30.20 Configuration of the time correction circuit

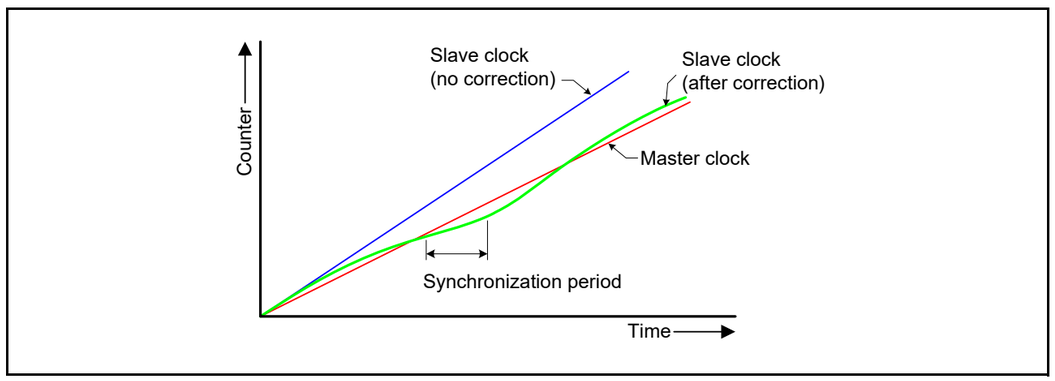


Figure 30.21 Overview of time correction

30.3.12 监控收到的消息

30.3.12.1 接收公告信息

EPTPC在接收Announce消息期间不检测超时。要检测超时，请监控软件对Announce消息的接收。

30.3.12.2 接收同步消息

当在纠正时间同步时接收同步消息期间发生超时时，STSR.SYNTOUT标志设置为1。

当接收到同步消息时，SYSR.OFMUD标志设置为1，无论时间同步是否正在被纠正。因此，即使在时间同步的校正由于在接收同步消息期间发生超时而停止时，也可以通过参考该标志来检测同步消息的接收。

30.3.12.3 接收Delay_Resp和Pdelay_Resp消息

SYSR.DRPTO标志设置为1，当在作为E2E从机运行时发送Delay_Req消息后接收Delay_Resp消息期间发生超时时，或者当在传输后接收Pdelay_Resp消息期间发生超时时作为P2P操作时的Pdelay_Req消息。

当接收到Delay_Resp或Pdelay_Resp消息时，SYSR.MPDUD标志设置为1，因此当接收期间发生超时时，仍可检测到这些消息的接收。

30.3.13 校正时间同步

从设备检测时钟梯度相对于主时钟的差异。使用标准IEEE1588算法计算的offsetFromMaster值用于计算时钟梯度，因此结果包括不是频率差异的网络波动元素。EPTPC具有最差10功能，可消除由网络负载和其他动态条件引起的波动。使用这些函数，根据计算出的梯度差值校正时间，并获得校正结果，如图30.21所示。

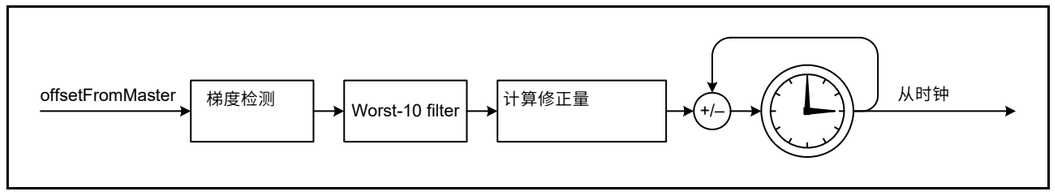


Figure 30.20 时间校正电路的构成

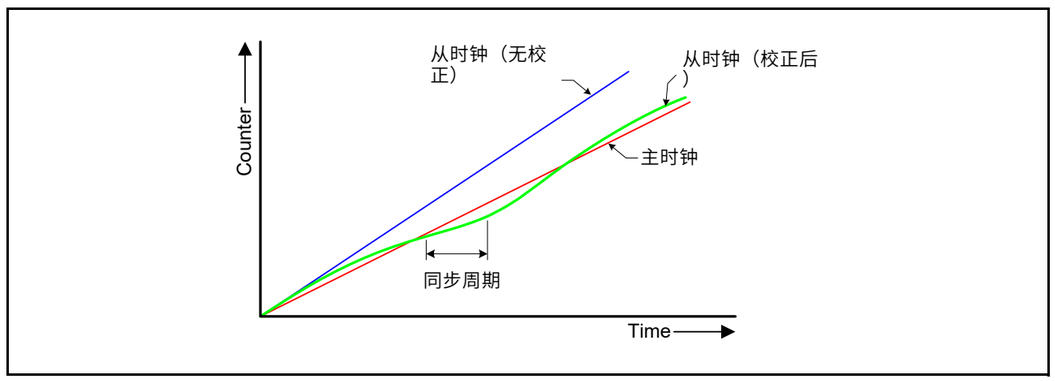


Figure 30.21 时间校正概述

30.3.13.1 Determining synchronization and loss of synchronization

Loss of synchronization is detected if the absolute value of offsetFromMaster reaches or exceeds the value specified in the SYNTDARU or SYNTDARL register. Synchronization is considered maintained if the absolute value of offsetFromMaster is less than the absolute values of the synchronization detection threshold registers, SYNTDBRU and SYNTDBRL.

The STSR.SYNCOUT flag is set to 1 when synchronization is lost, and the SYNC flags is set to 1 when synchronization is obtained. Hysteresis can be obtained by setting the threshold registers to appropriate different values. In addition, the STMR.DVTH[3:0] and SYTH[3:0] bits can be used to set the consecutive number of times detection must occur for the determination of synchronization and loss of synchronization.

For systems in which control must be aborted if synchronization is lost because of fluctuations in network conditions, set the SYNTDARU and SYNTDARL registers to low values and set the number of times detection is required to trigger a loss of synchronization to one. In systems where these conditions do not apply, set the SYNTDARU and SYNTDARL registers and the number of times detection is required to large values.

Figure 30.22 shows an example of a situation where synchronization is lost and regained. In this example, the number of consecutive times detection is required is three for both synchronization and loss of synchronization.

Note: The setting of the STSR.SYNCOUT flag is 1 when time synchronization starts, even if the condition for determining loss of synchronization is not satisfied at this stage. For this reason, detection of loss of synchronization must be ignored immediately after time synchronization starts.

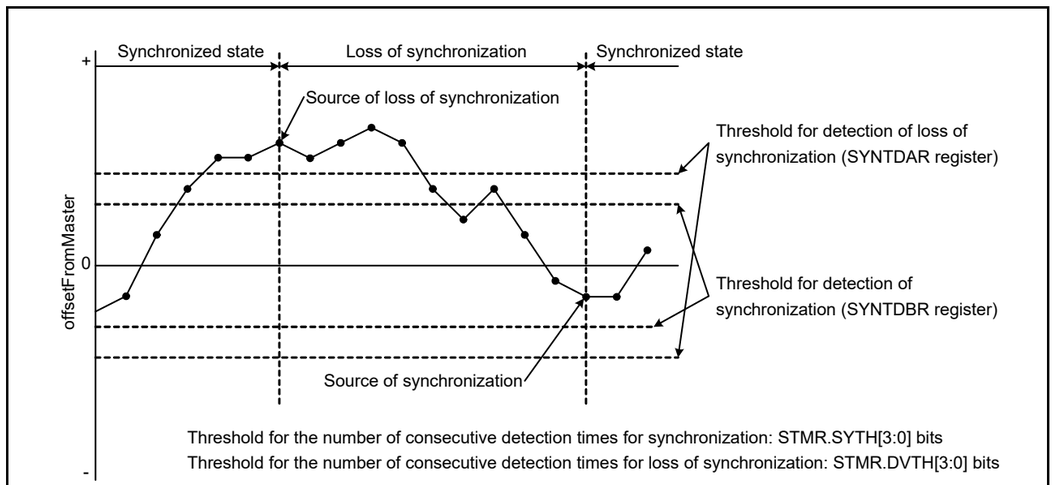


Figure 30.22 Example of a situation where synchronization is lost and regained, when the number of consecutive detections is set to three in the STMR.DVTH[3:0] and SYTH[3:0] bits

30.3.13.2 Worst-10 function

The worst-10 function is used to impose limits on exceedingly large and small values among the calculated values for clock gradient differences. These values are collected by observing the transfer over a specified interval, and threshold values to impose limits are extracted from the observed values. Fluctuations in network conditions must be considered in addition to clock errors, and differences in both the positive and negative directions are collected, as shown in Figure 30.23.

The function selects the largest gradient values from the collected values for positive and negative gradient differences, orders them from first to tenth (worst to tenth worst), and uses the tenth worst as a threshold value. Fluctuations in the time kept by a slave clock can be suppressed by continually overwriting the tenth worst value with new values large enough to exceed the threshold. Periodic collections of gradient values can also be made for updating the threshold values during operations or for using the method of setting threshold values from previously measured results.

30.3.13.1 确定同步和同步丢失

如果offsetFromMaster的绝对值达到或超过SYNTDARU或SYNTDARL寄存器中指定的值，则检测到同步丢失。如果offsetFromMaster的绝对值小于同步检测阈值寄存器SYNTDBRU和SYNTDBRL的绝对值，则认为保持同步。

STSR.SYNCOUT标志在同步丢失时设置为1，而SYNC标志在获得同步时设置为1。可以通过将阈值寄存器设置为适当的不同值来获得滞后。此外，STMR.DVTH[3:0]和SYTH[3:0]位可用于设置必须发生的连续检测次数，以确定同步和同步丢失。

对于如果由于网络条件波动而失去同步而必须中止控制的系统，请将SYNTDARU和SYNTDARL寄存器设置为低值，并将触发同步丢失所需的检测次数设置为1。在不适用这些条件的系统中，将SYNTDARU和SYNTDARL寄存器以及需要检测的次数设置为较大的值。

图30.22显示了同步丢失和重新获得的情况的示例。在本例中，同步和失步都需要连续检测3次。

Note: 当时间同步开始时，STSR.SYNCOUT标志的设置为1，即使在此阶段不满足确定同步丢失的条件。因此，必须在时间同步开始后立即忽略同步丢失的检测。

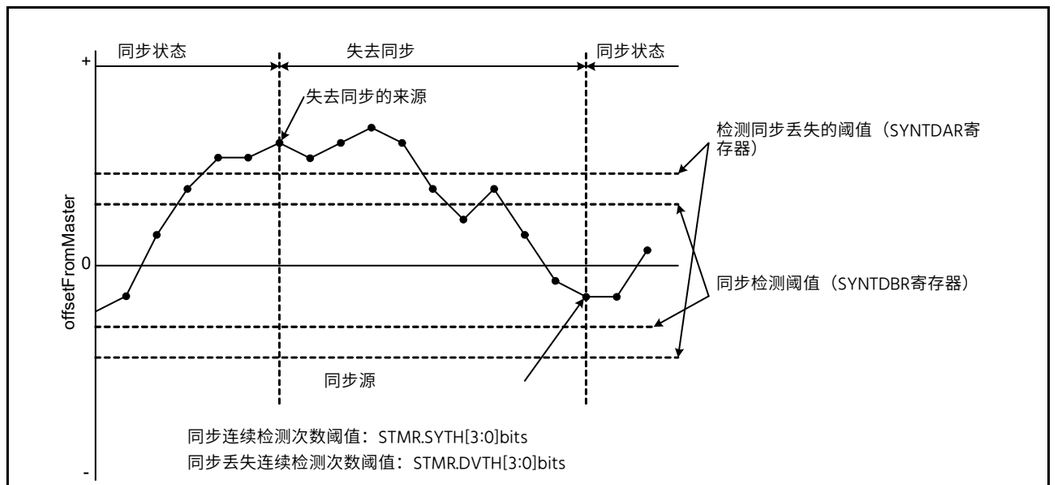


Figure 30.22 当STMR.DVTH[3:0]和SYTH[3:0]位中的连续检测数设置为3时，同步丢失和重新获得的情况示例

30.3.13.2 Worst-10 function

最差10函数用于对时钟梯度差的计算值中的极大值和极小值施加限制。这些值是通过在指定的时间间隔内观察传输来收集的，并且从观察值中提取施加限制的阈值。除了时钟误差外，还必须考虑网络条件的波动，收集正负两个方向的差异，如图30.23所示。

该函数从收集的正负梯度差值中选择最大的梯度值，将它们从第一个到第十个（最差到第十个最差）排序，并使用第十个最差作为阈值。从时钟保持的时间波动可以通过用大到足以超过阈值的新值连续覆盖第十个最差值来抑制。梯度值的定期收集也可以用于在操作期间更新阈值或使用根据先前测量结果设置阈值的方法。

However, while fluctuations in the time kept by a slave clock can be suppressed by the valid filtering of values for gradient difference (collecting the worst 10 values and using the tenth worst), this slows down the following of time kept by a master clock.

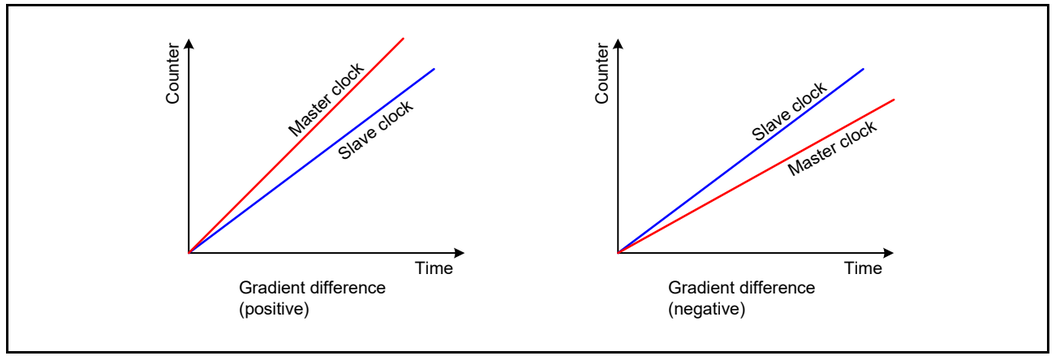


Figure 30.23 Overview of gradient differences

30.3.13.3 Collecting differences in clock gradient and extracting the worst ten values

During slave operation, the EPTPC can calculate the offsetFromMaster values from received messages and calculate gradient differences between the local clock (acting as a slave clock) and master clock from those values. Specifically, the worst ten values are extracted from the sets of collected values for gradient difference. Either automatic filtering by the hardware or software-triggered filtering can be designated for acquisition of the sets of the worst 10 values. Figure 30.24 gives an overview of the collection of gradient difference values.

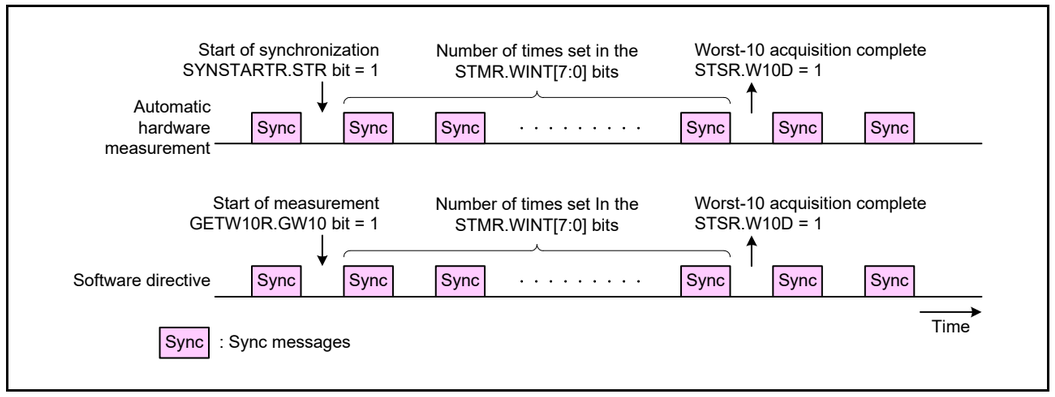


Figure 30.24 Overview of the collection of gradient difference values

(1) Collecting gradient differences and extracting the worst ten values by hardware

The EPTPC automatically collects the gradient difference values by hardware if the STMR.W10S bit is 0.

When the SYNSTARTR.STR bit is set to 1 (starting slave time synchronization), the EPTPC collects gradient difference values for the number of times set in the STMR.WINT[7:0] bits. When the collection of gradient difference values is finished, the tenth largest values on the positive and negative sides are stored as the tenth worst values in the PW10VRU, PW10VRM, and PW10VRL registers and the MW10RU, MW10RM, and MW10RL registers. When acquisition of the worst 10 values completes, the STSR.W10D flag sets to 1. Filtering of gradient difference values by using the stored tenth worst values then proceeds automatically.

If the number of times set in the STMR.WINT[7:0] bits is less than ten, the double of the best of the collected values on the positive side is stored in the PW10VRU, PW10VRM, and PW10VRL registers. The half of the best of the collected values on the negative side is stored in the MW10RU, MW10RM, and MW10RL registers.

然而，虽然从时钟保持的时间波动可以通过梯度差值的有效过滤（收集最差的10个值并使用第十个最差的值）来抑制，但这会减慢主时钟保持的时间跟踪。

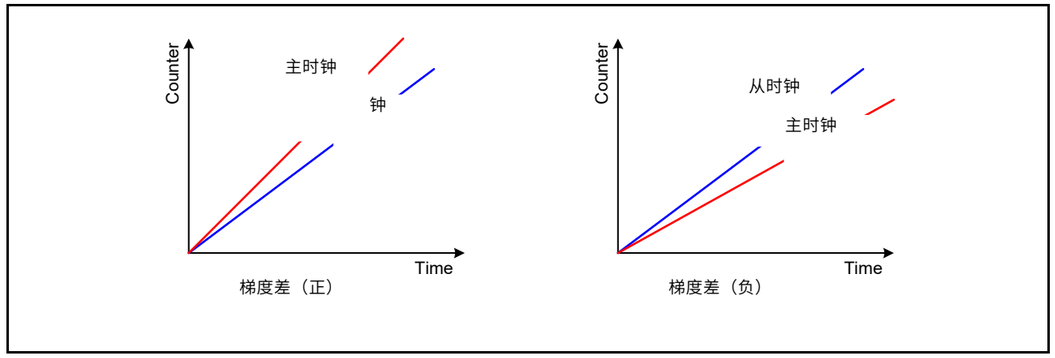


Figure 30.23 梯度差异概述

30.3.13.3 收集时钟梯度的差异并提取最差的十个值

在从属操作期间，EPTPC可以根据接收到的消息计算offsetFromMaster值，并根据这些值计算本地时钟（充当从属时钟）和主时钟之间的梯度差。具体而言，从梯度差的收集值集中提取最差的十个值。可以指定硬件自动过滤或软件触发过滤来获取最差的10个值的集合。图30.24给出了梯度差值集合的概览。

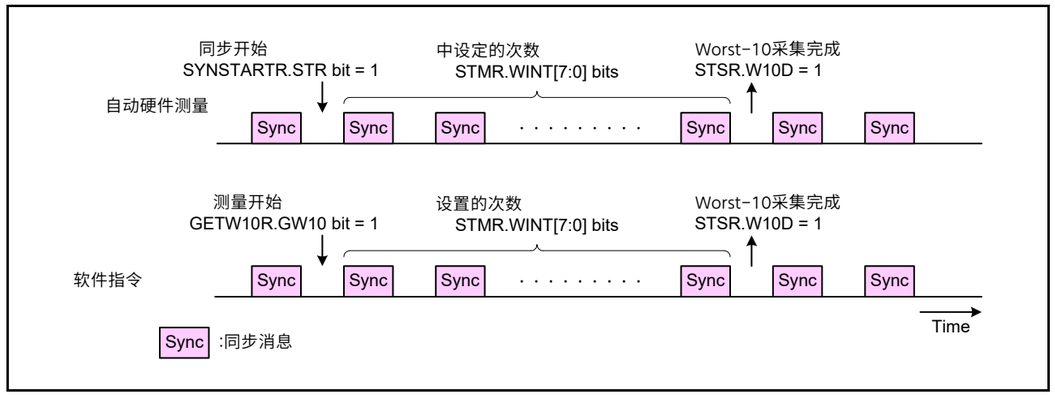


Figure 30.24 梯度差值收集概述

(1) 收集梯度差异并通过硬件提取最差的十个值

如果STMR.W10S位为0，EPTPC会通过硬件自动收集梯度差值。

当SYNSTARTR.STR位设置为1（启动从属时间同步）时，EPTPC收集在STMR.WINT[7:0]位中设置的次数的梯度差值。梯度差值采集完成后，正负侧第10个最大值作为第10个最差值存储在PW10VRU、PW10VRM和PW10VRL寄存器和MW10RU、MW10RM和MW10RL寄存器中。当最差10个值的采集完成时，STSR.W10D标志设置为1。然后使用存储的第10个最差值过滤梯度差值，然后自动进行。

如果在STMR.WINT[7:0]位中设置的次数小于10，则正侧收集的最佳值的两倍存储在PW10VRU、PW10VRM和PW10VRL寄存器中。负侧收集的最佳值的一半存储在MW10RU、MW10RM和MW10RL寄存器中。

(2) Collecting gradient differences and extracting the worst ten values by software

The EPTPC collects gradient difference values by software if the STMR.W10S bit is 1.

When the GETW10R.GW10 bit is set to 1 after time synchronization starts, the EPTPC collects gradient difference values for the number of times set in the STMR.WINT[7:0] bits. When the collection of gradient difference values is finished, the tenth largest values on the positive and negative sides are stored as the tenth worst values in the PW10VRU, PW10VRM, and PW10VRL registers and the MW10RU, MW10RM, and MW10RL registers. When acquisition of the worst 10 values completes, the STSR.W10D flag is set to 1.

Because filtering of gradient difference values proceeds with the values set in the PLIMITRU, PLIMITRM, and PLIMITRL registers as the upper filtering limits and the MLIMITRU, MLIMITRM, and MLIMITRL registers as the lower filtering limit, you must write the values stored in the PW10VRU, PW10VRM, and PW10VRL registers to PLIMITRU, PLIMITRM, and PLIMITRL, and write the values stored in the MW10RU, MW10RM, and MW10RL registers to MLIMITRU, MLIMITRM, and MLIMITRL.

If the number of times set in the STMR.WINT[7:0] bits is less than ten, the double of the best of the collected values on the positive is stored in the PW10VRU, PW10VRM, and PW10VRL registers. The half of the best of the collected values on the negative side is stored in the MW10RU, MW10RM, and MW10RL registers.

(2) 通过软件收集梯度差异并提取最差的十个值

如果STMR.W10S位为1，EPTPC通过软件收集梯度差值。

当GETW10R.GW10位在时间同步开始后设置为1时，EPTPC将收集STMR.WINT[7:0]位中设置的次数的梯度差值。梯度差值采集完成后，正负侧第10个最大值作为第10个最差值存储在PW10VRU、PW10VRM和PW10VRL寄存器和MW10RU、MW10RM和MW10RL寄存器中。当最差10个值的采集完成时，STSR.W10D标志设置为1。

因为梯度差值的过滤使用PLIMITRU、PLIMITRM和PLIMITRL寄存器作为滤波上限，MLIMITRU、MLIMITRM和MLIMITRL寄存器作为滤波下限，必须将PW10VRU、PW10VRM和PW10VRL寄存器中存储的值写入PLIMITRU、PLIMITRM和PLIMITRL，并将存储的值写入MW10RU、MW10RM和MW10RL寄存器中的MLIMITRU、MLIMITRM和MLIMITRL。

如果在STMR.WINT[7:0]位中设置的次数小于10，则正极上收集到的最佳值的两倍存储在PW10VRU、PW10VRM和PW10VRL寄存器中。负侧收集的最佳值的一半存储在MW10RU、MW10RM和MW10RL寄存器中。

The flow in Figure 30.25 shows an example of the procedure for software-triggered acquisition of the worst 10 values.

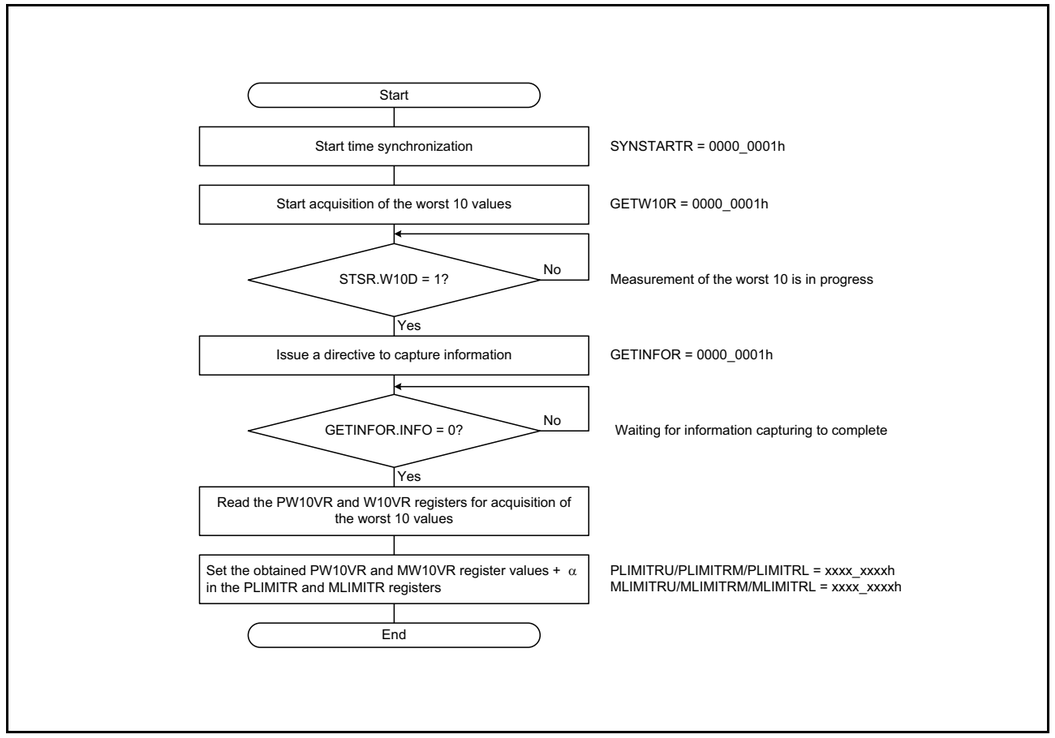


Figure 30.25 Example procedure for software-triggered acquisition of the worst 10 values

30.3.14 Local Clock Counter

The local clock counter retains the synchronized time information. The counter starts counting from 0 after the ETHERC is released from the module-stop state or the EPTPC is released from the software reset state. The local clock counter can then be set to any value. Figure 30.26 shows the procedure for setting the initial value in the local clock counter.

The time information kept by the local clock counter is also readable. Figure 30.27 shows the procedure for reading the time information kept by the local clock counter.

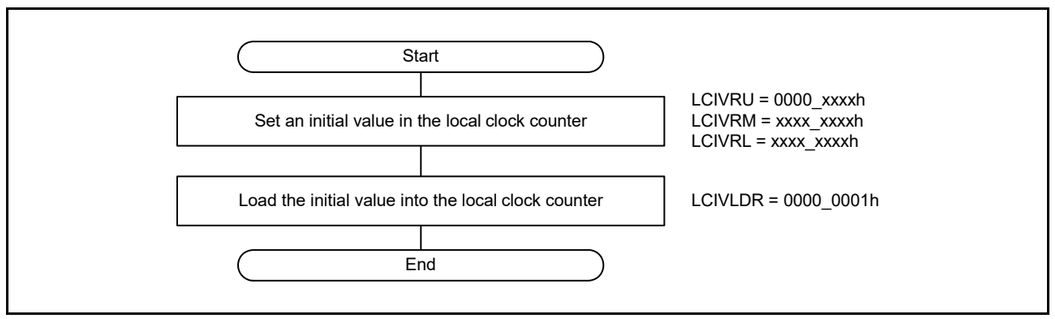


Figure 30.26 Procedure for setting a new initial value in the local clock counter

图30.25中的流程显示了软件触发采集最差10个值的过程示例。

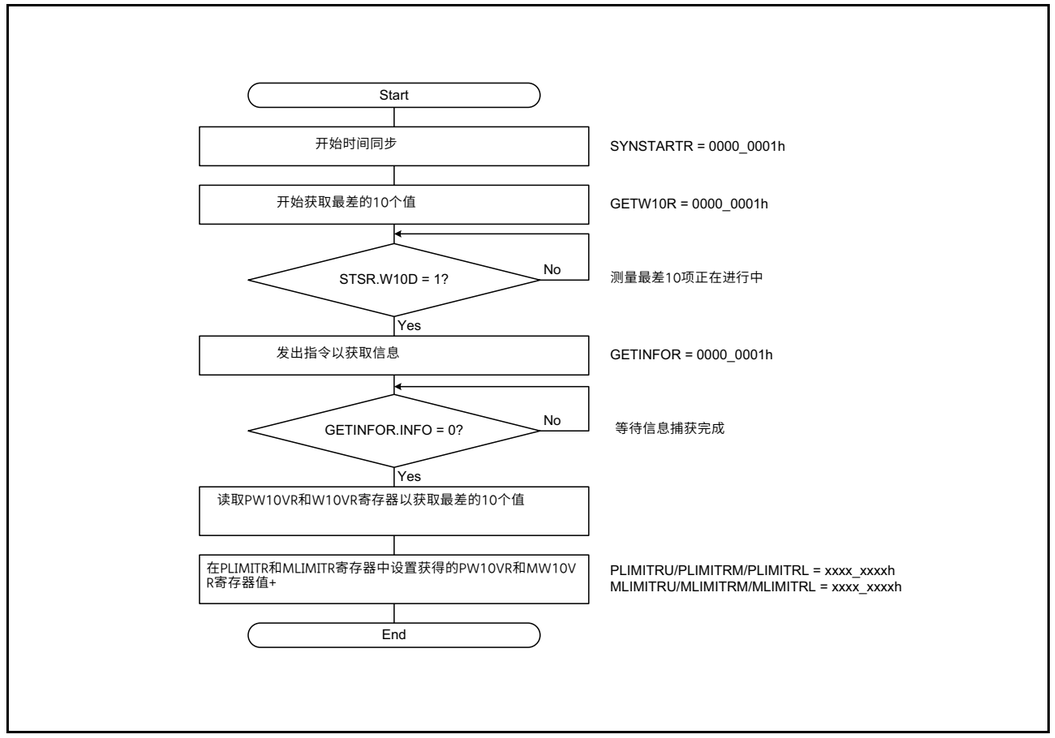


Figure 30.25 软件触发采集最差10个值的示例程序

30.3.14 本地时钟计数器

本地时钟计数器保留同步的时间信息。ETHERC从模块停止状态释放或EPTPC从软件复位状态释放后，计数器从0开始计数。然后可以将本地时钟计数器设置为任何值。图30.26显示了在本地时钟计数器中设置初始值的过程。

本地时钟计数器保存的时间信息也是可读的。图30.27显示了读取本地时钟计数器保存的时间信息的过程。

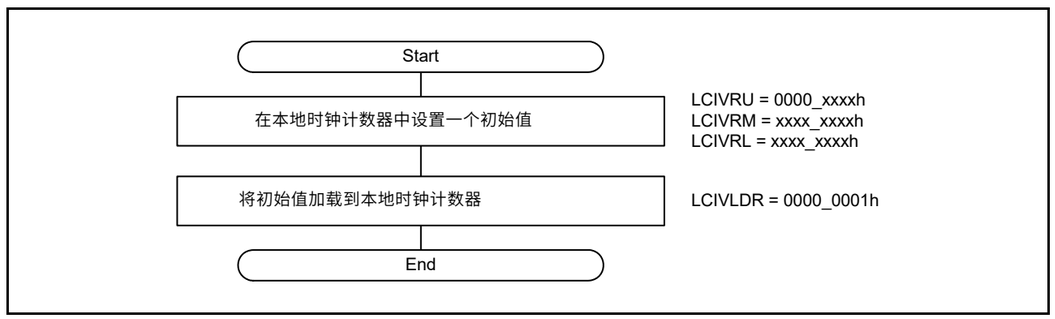


Figure 30.26 在本地时钟计数器中设置新初始值的过程

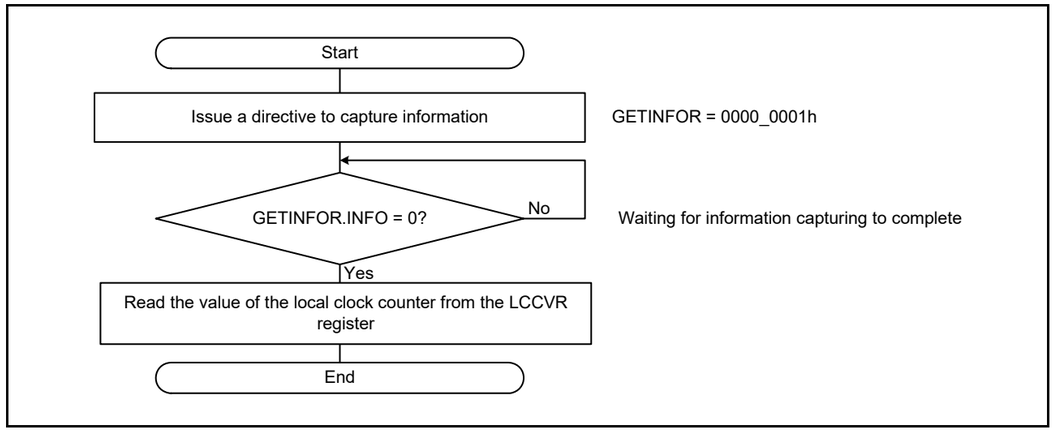


Figure 30.27 Procedure for reading the time kept by the local clock counter

30.3.15 Pulse Output Timer

The STCA module of the EPTPC incorporates six timers (pulse output timers 0 to 5) that operate independently of each other. The pulse output timers produce periodic pulses, and the rising or falling edges of these pulses can be used as interrupt requests or output to the ELC as event signals. The time at which a pulse output timer starts operating (t_{start}), and the period (t_c) and pulse width (t_w) of the output pulses, can be specified.

Figure 30.28 shows the timing of pulse output timer operation, and Table 30.22 lists the constraints on the settings.

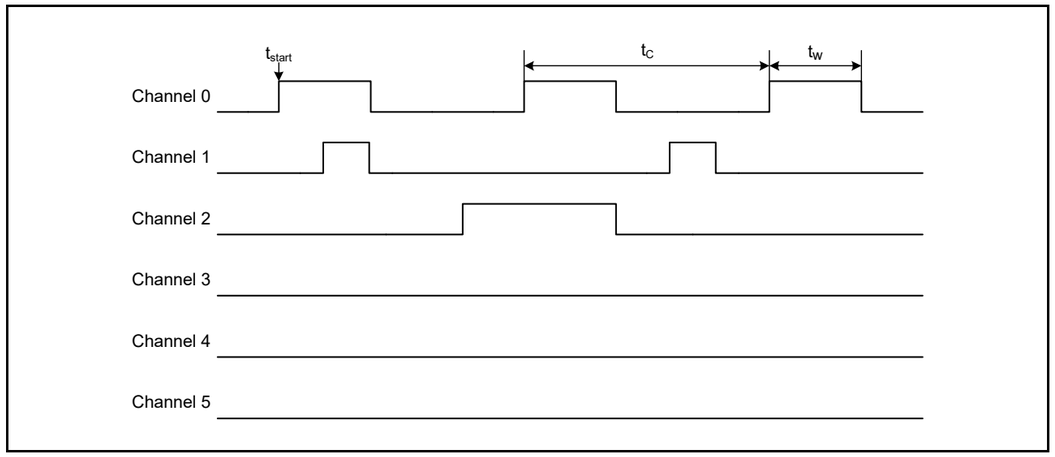


Figure 30.28 Time at which a pulse output timer starts operating

Table 30.22 Constraints on the values that can be specified for a pulse output timer (1 of 2)

Parameter	Constraints
Cycle (t_C)	From 4 cycles of the STCA clock to 1 s
Resolution of the cycle	Set in nanoseconds However, the timing of rising edges is rounded by the period of the system clock (50 ns, 40 ns, 20 ns, or 10 ns).
Pulse width (t_w)	From 2 cycles of the STCA clock to 500 ms

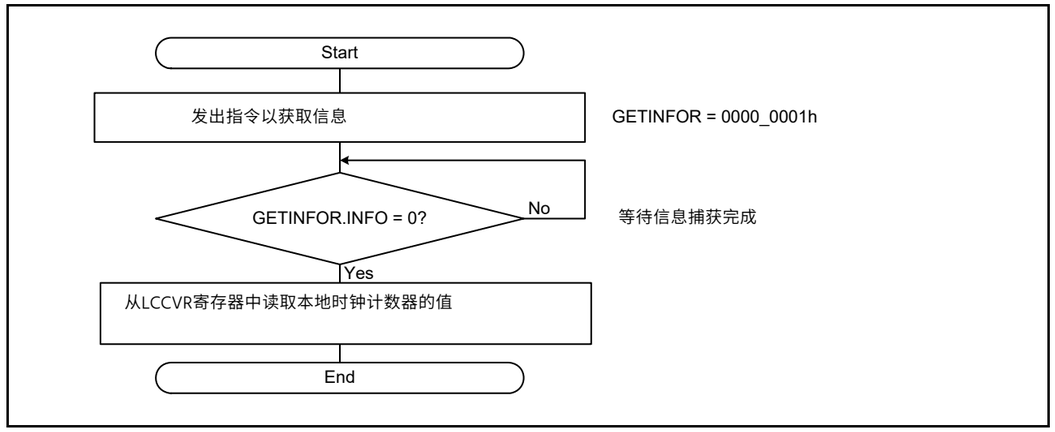


Figure 30.27 读取本地时钟计数器保持的时间的过程

30.3.15 脉冲输出定时器

EPTPC的STCA模块包含六个相互独立运行的定时器（脉冲输出定时器0到5）。脉冲输出定时器产生周期性脉冲，这些脉冲的上升沿或下降沿可用作中断请求或作为事件信号输出到ELC。可以指定脉冲输出定时器开始工作的时间(tstart)，以及输出脉冲的周期(tc)和脉冲宽度(tw)。

图30.28显示了脉冲输出定时器操作的时序，表30.22列出了设置的限制条件。

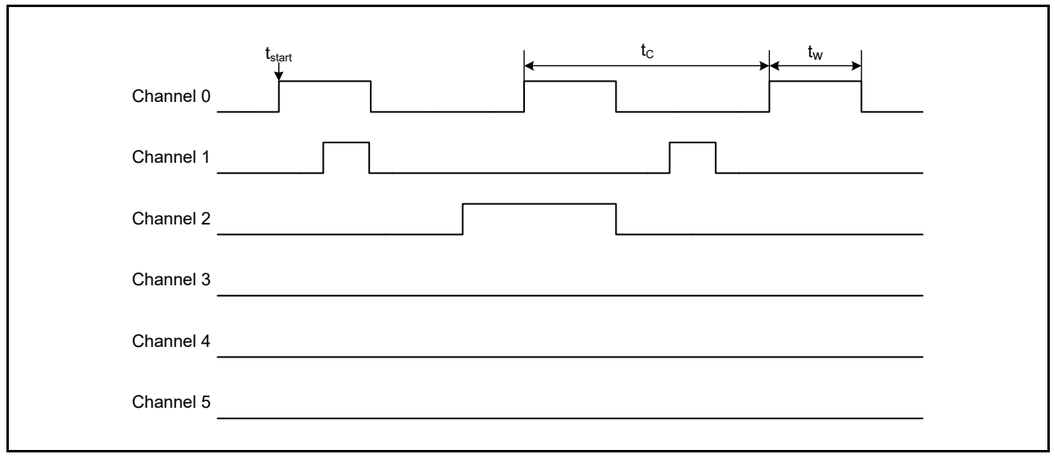


Figure 30.28 脉冲输出定时器开始工作的时间

Table 30.22 可以为脉冲输出定时器指定的值的限制（1of2）

Parameter	Constraints
Cycle (t_C)	从STCA时钟的4个周期到1s
循环分辨率	以纳秒为单位设置 但是，上升沿的时序会按系统时钟的周期（50ns、40ns、20ns或10ns）四舍五入。
脉冲宽度(tw)	从STCA时钟的2个周期到500ms

Table 30.22 Constraints on the values that can be specified for a pulse output timer (2 of 2)

Parameter	Constraints
Resolution of the pulse width	Set in nanoseconds However, the timing of falling edges is rounded by the period of the system clock (50 ns, 40 ns, 20 ns, or 10 ns).

30.3.15.1 Procedure for setting a pulse output timer

Figure 30.29 shows the procedure for setting a pulse output timer.

Note: A timer does not produce periodic pulses if the time set in the TMSTTRUm and TMSTTRLm registers (m = 0 to 5) has elapsed. Set the time for a pulse output timer to start at a later time than that when the timer is set.

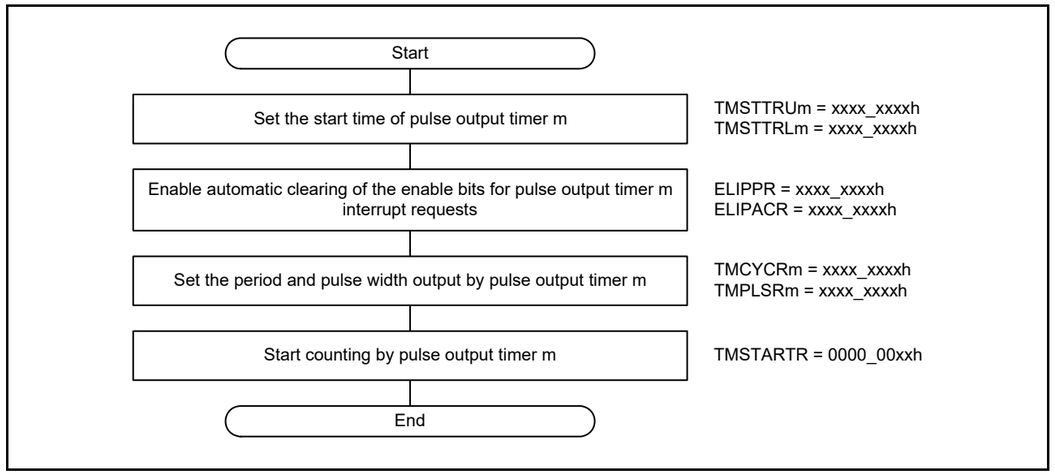


Figure 30.29 Procedure for setting a pulse output timer

30.3.15.2 Output of periodic pulses as interrupt requests or event signals

ETHER_MINT interrupt requests, ETHER_IPLS interrupt requests, or event output signals for the ELC can be generated on detection of rising or falling edges of the periodic pulses from the pulse output timer. The detection edge and the pulse output timer used are configurable, and automatic clearing of enable bits for the ETHER_IPLS interrupt or event output can be set. Make the required settings before setting the TMSTARTR.ENm bit to 1 (starting pulse output timer m).

(1) ETHER_MINT interrupt request

ETHER_MINT interrupt requests can be generated on rising edges of the periodic pulses from the pulse output timers. They cannot be generated on falling edges. Select the pulse output timers for generating these requests in the MITSELR.MINTENm bits. Automatic clearing of the enable bits for ETHER_MINT interrupt requests is not available.

(2) ETHER_IPLS interrupt request

ETHER_IPLS interrupt requests can be generated on either rising or falling edges of the periodic pulses from the pulse output timers. Select the pulse output timers for generating these requests in the IPTSELR.IPTSELm bits. Setting the ELIPACR.PLSP or PLSN bit enables automatic clearing of the enable bits for ETHER_IPLS interrupt requests.

(3) Output of event signals to the ELC

Event signals can be output to the ELC on either rising or falling edges of the periodic pulses from the pulse output timers. Select the pulse output timers for event signal output and the valid edge in the ELIPPR.CYCPm or CYCNm bits. Setting the ELIPACR.CYCPm or CYCNm bits enables automatic clearing of the event output enable bits.

Table 30.22 可以为脉冲输出定时器指定的值的限制（2个中的2个）

Parameter	Constraints
脉冲宽度的分辨率	以纳秒为单位设置 但是，下降沿的时序会按系统时钟的周期（50ns、40ns、20ns或10ns）四舍五入。

30.3.15.1 设置脉冲输出定时器的步骤

图30.29显示了设置脉冲输出定时器的过程。

Note: 如果TMSTTRUm和TMSTTRLm寄存器（m=0到5）中设置的时间已过，则定时器不会产生周期性脉冲。将脉冲输出定时器的启动时间设置为比定时器设置的时间晚。

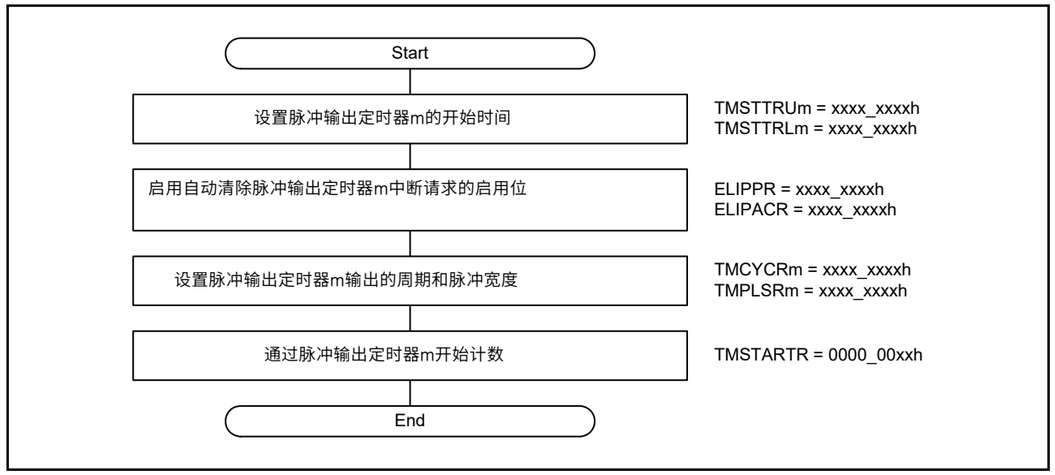


Figure 30.29 设置脉冲输出定时器的步骤

30.3.15.2 输出周期性脉冲作为中断请求或事件信号

ETHER_MINT中断请求、ETHER_IPLS中断请求或ELC的事件输出信号可以在检测到来自脉冲输出定时器的周期性脉冲的上升沿或下降沿时生成。使用的检测边沿和脉冲输出定时器是可配置的，并且可以设置ETHER_IPLS中断或事件输出的使能位的自动清除。在将TMSTARTR.ENm位设置为1（启动脉冲输出定时器m）之前进行所需的设置。

(1) ETHER_MINT中断请求

ETHER_MINT中断请求可以在来自脉冲输出定时器的周期性脉冲的上升沿产生。它们不能在下降沿生成。选择脉冲输出定时器以在

MITSELR.MINTENm位。无法自动清除ETHER_MINT中断请求的启用位。

(2) ETHER_IPLS中断请求

ETHER_IPLS中断请求可以在来自脉冲输出定时器的周期性脉冲的上升沿或下降沿产生。在IPTSELR.IPTSELm位中选择用于生成这些请求的脉冲输出定时器。设置ELIPACR.PLSP或PLSN位可以自动清除ETHER_IPLS中断请求的启用位。

(3) 向ELC输出事件信号

事件信号可以在脉冲输出定时器的周期脉冲的上升沿或下降沿输出到ELC。在ELIPPR.CYCPm或CYCNm位中选择事件信号输出的脉冲输出定时器和有效边沿。设置ELIPACR.CYCPm或CYCNm位可以自动清除事件输出使能位。

30.3.16 Priority Control in Transmission

30.3.16.1 Arbitration

Contention between multiple requests for the transmission of messages by the SYNFP module are arbitrated in the order of priority shown in Table 30.23.

Table 30.23 Priority for message transmission arbitration

Transmission message	Priority order	Remark
Sync	1 Highest priority	—
Delay_Req, Pdelay_Req	2	There is no device type that simultaneously transmits Delay_Req and Pdelay_Req messages
Delay_Resp, Pdelay_Resp	3	There is no device type that simultaneously transmits Delay_Resp and Pdelay_Resp messages
Announce	4	—
Messages to be transmitted from the PTPEDMAC	5	—
Messages to be transmitted from the EDMAC0	6	—

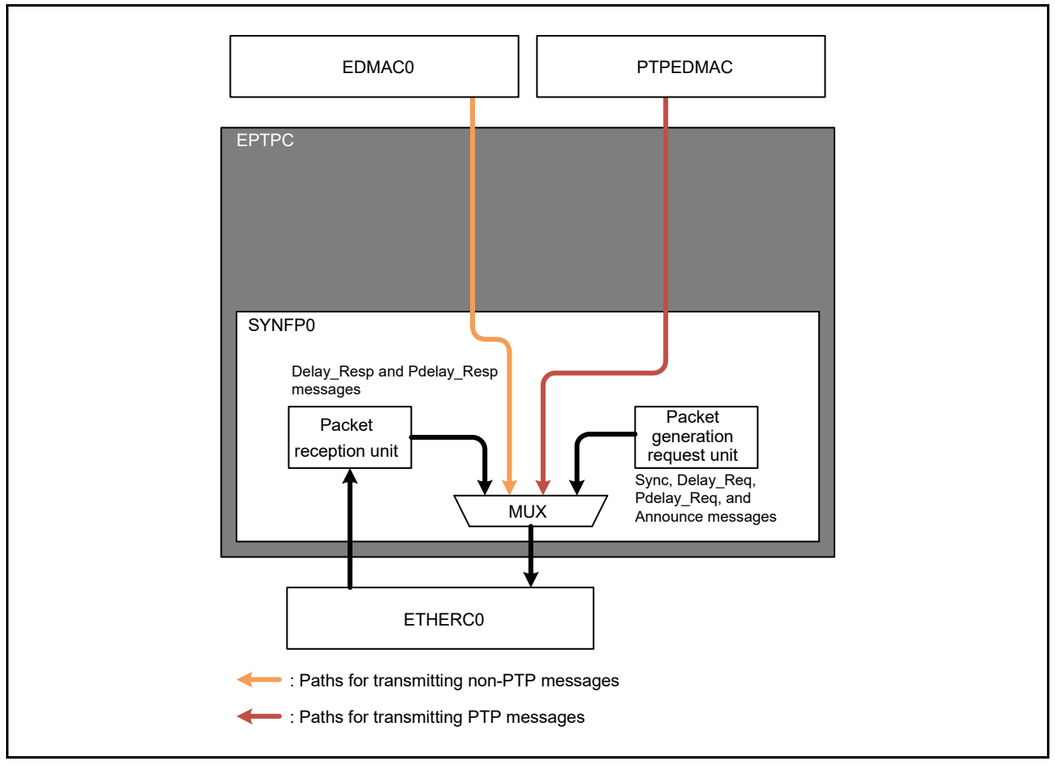


Figure 30.30 Arbitration in message transmission

30.3.16.2 Securing bandwidth for the transmission of sync messages

The EPTPC secures bandwidth for the transmission of Sync messages, and is capable of handling transmission at very precise intervals.

If the transmission of a Sync message at a fixed interval proceeds at the same time that transmission by the PTPEDMAC,

30.3.16 传输优先控制

30.3.16.1 Arbitration

SYNFP模块的多个消息传输请求之间的争用按照表30.23中所示的优先级顺序进行仲裁。

Table 30.23 消息传输仲裁的优先级

传送讯息	优先顺序	Remark
Sync	1 最高优先级	—
Delay_Req, Pdelay_Req	2	没有同时传输的设备类型 Delay_Req和Pdelay_Req消息
Delay_Resp, Pdelay_Resp	3	没有同时传输的设备类型 Delay_Resp和Pdelay_Resp消息
Announce	4	—
要从 PTPEDMAC	5	—
要从EDMAC0传输的消息	6	—

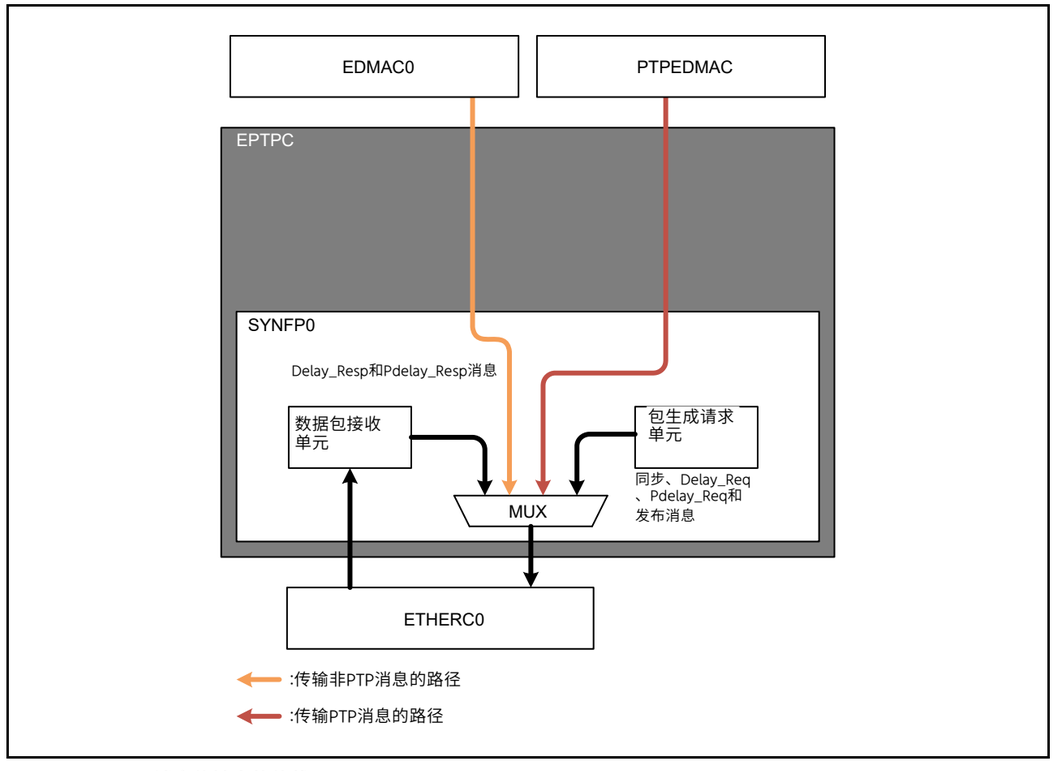


Figure 30.30 消息传输中的仲裁

30.3.16.2 确保传输同步消息的带宽

EPTPC为同步消息的传输确保带宽，并且能够以非常精确的间隔处理传输。

如果Sync消息以固定间隔的传输与PTPEDMAC的传输同时进行，

because transmission of the Sync message proceeds when the other processing is complete, the interval for transmission is no longer fixed. Securing bandwidth for the transmission of Sync messages limits the transmission of messages from EDMAC0 and the PTPEDMAC, allowing Sync message transmission to be handled without fluctuations. To disable securing of bandwidth for Sync message transmission, set the SYCONFR.SBDIS bit to 1.

Figure 30.31 gives a schematic view of securing bandwidth for the transmission of Sync messages.

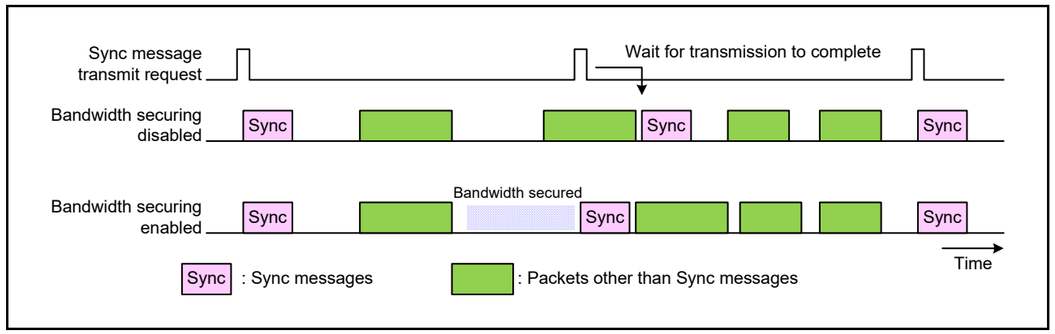


Figure 30.31 Securing of bandwidth for Sync message transmission

30.3.16.3 Securing of transmission interval

In the transmission of messages by the ETHERC, if there is a fixed delay from the time of a request for transmission to the time of transmission on the MII of Ethernet port 0, PTP message timestamps can be used for accurately obtaining the size of the delay during slave operation. However, for continuous transfer where processing of messages to wait for inter-packet gap times is required, delay times might fluctuate.

To enable the ETHERC to secure the reliability of timestamp values, specify an interval for frame transmission in the SYCONFR.TCYC[7:0] bits to control the interval between the completion of transmission and the next request for transmission. This avoids the effects of inter-packet gap times and a fixed delay for transmission.

30.4 Interrupts

The EPTPC provides the ETHER_MINT and ETHER_IPLS interrupt requests. Figure 30.32 shows the relationship between the two interrupt requests. Figure 30.33 shows the details on interrupt requests of the pulse output timer.

因为当其他处理完成时同步消息的传输继续，传输间隔不再是固定的。确保同步消息传输的带宽限制了来自EDMAC0和PTPEDMAC的消息传输，从而允许处理同步消息传输而不会出现波动。要禁用同步消息传输的带宽保护，请将SYCONFR.SBDIS位设置为1。

图30.31给出了为Sync消息的传输确保带宽的示意图。

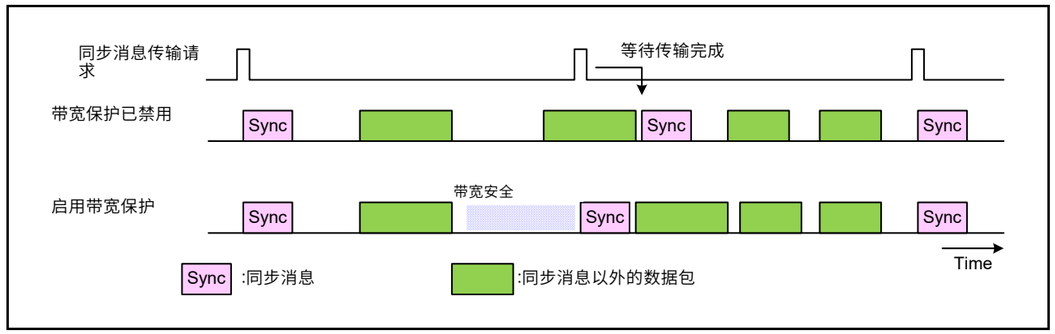


Figure 30.31 确保同步消息传输的带宽

30.3.16.3 确保传输间隔

在ETHERC传输消息时，如果从请求传输的时间到以太网端口0的MII上传输的时间之间存在固定的延迟，则可以使用PTP消息时间戳来准确获取延迟的大小在从属操作期间。但是，对于需要处理消息以等待包间间隙时间的连续传输，延迟时间可能会波动。

为了使ETHERC能够确保时间戳值的可靠性，请在SYCONFR.TCYC[7:0]位控制传输完成和下一次传输请求之间的间隔。这避免了包间间隙时间和传输的固定延迟的影响。

30.4 Interrupts

EPTPC提供ETHER_MINT和ETHER_IPLS中断请求。图30.32显示了两个中断请求之间的关系。图30.33显示了脉冲输出定时器的中断请求的详细信息。

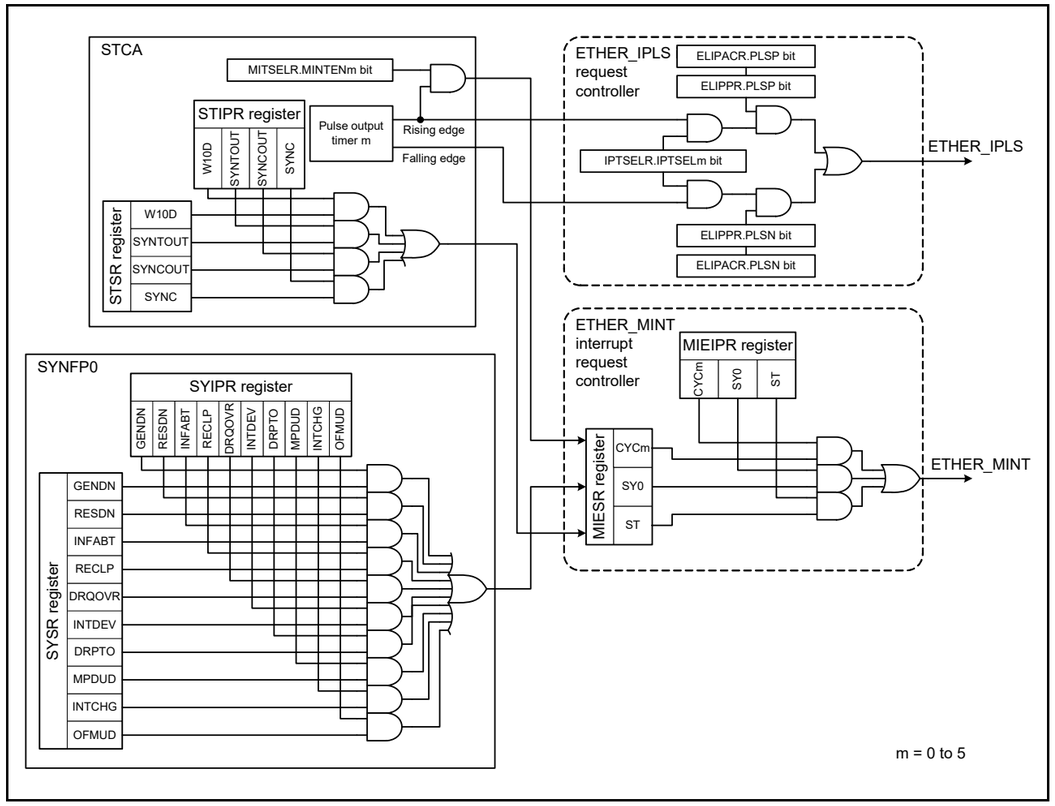


Figure 30.32 ETHER_MINT and ETHER_IPLS interrupt requests

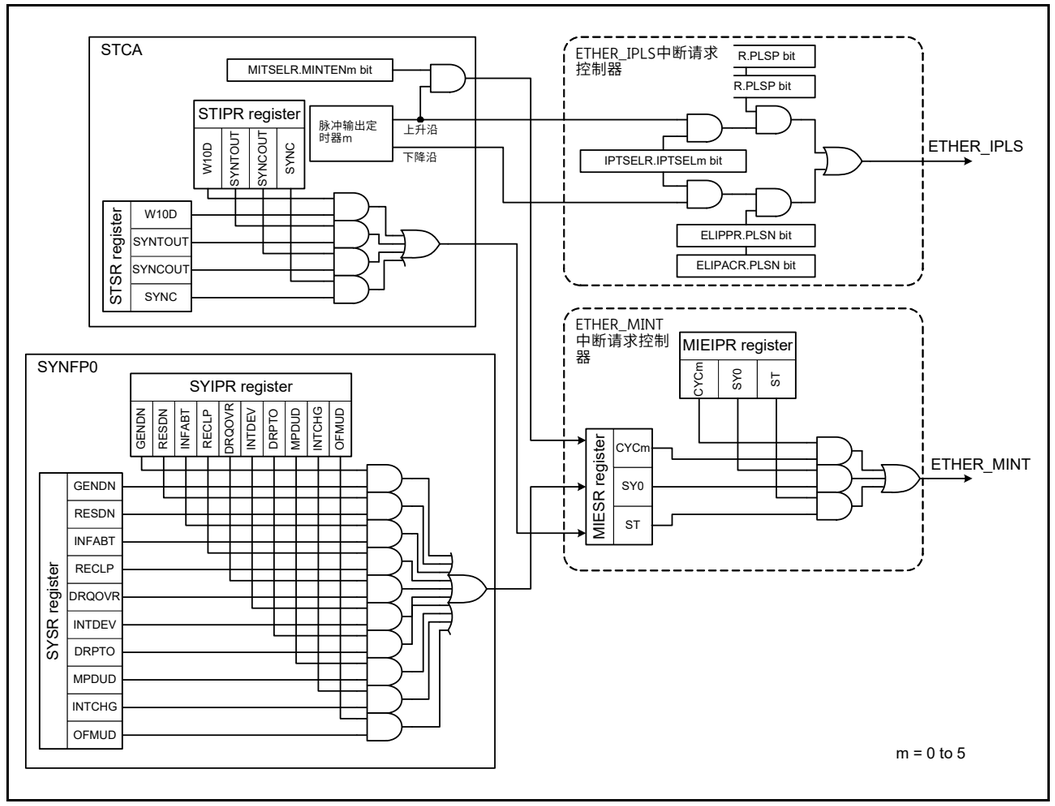


Figure 30.32 ETHER_MINT和ETHER_IPLS中断请求

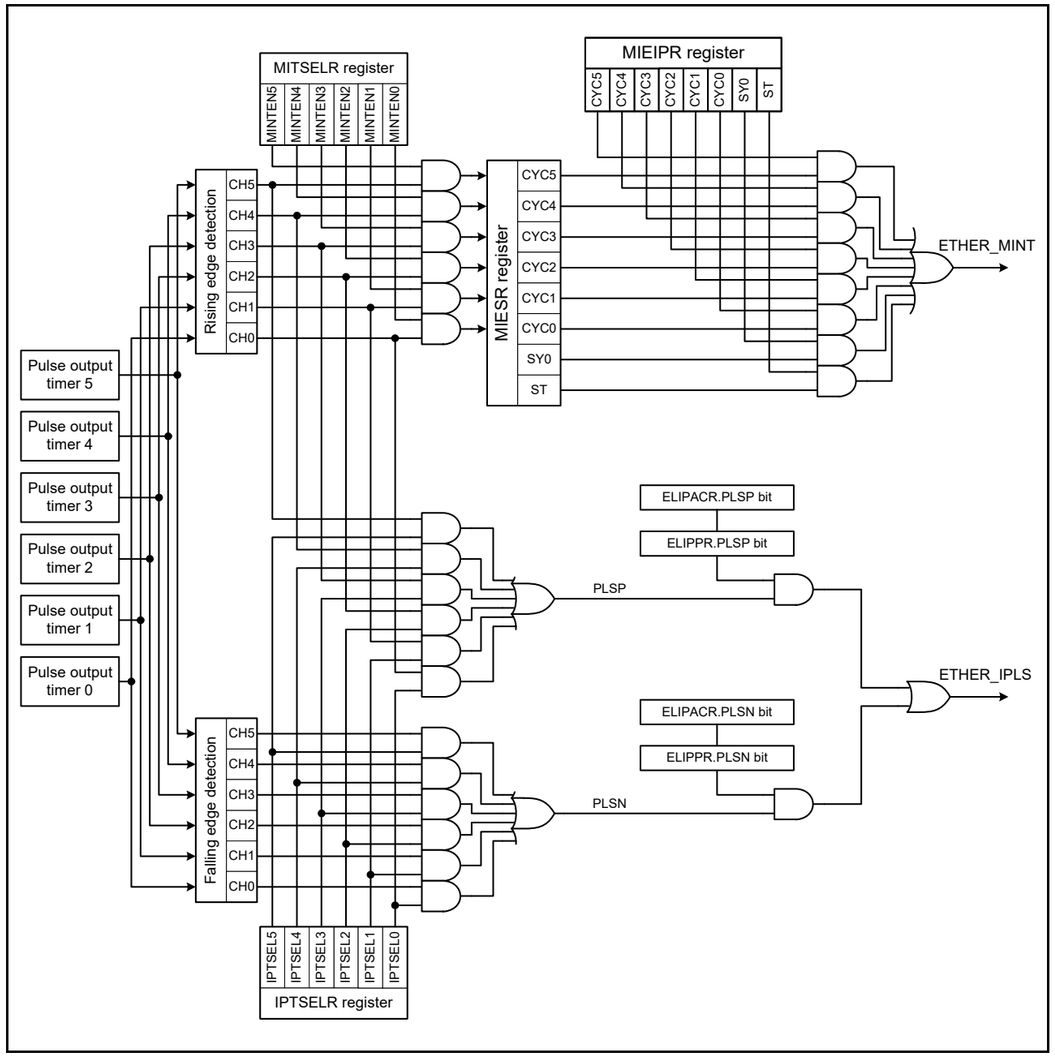


Figure 30.33 Details on interrupt requests of the pulse output timer

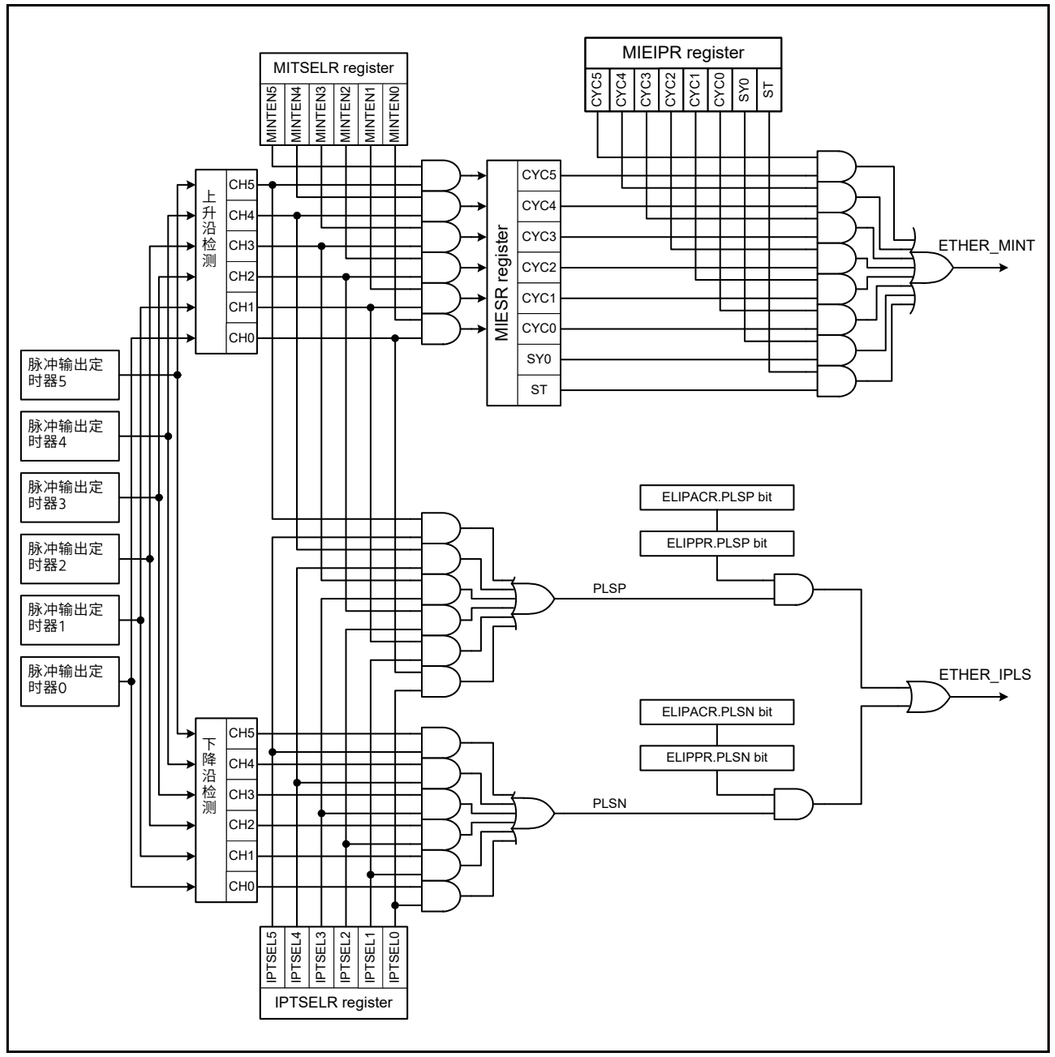


Figure 30.33 脉冲输出定时器的中断请求详情

30.5 Event Link (Output)

The EPTPC can output an event to the ELC by detecting the rising or falling edge of the pulse from the pulse output timer. Figure 30.34 shows the relationship between the pulse output timer and the ELC.

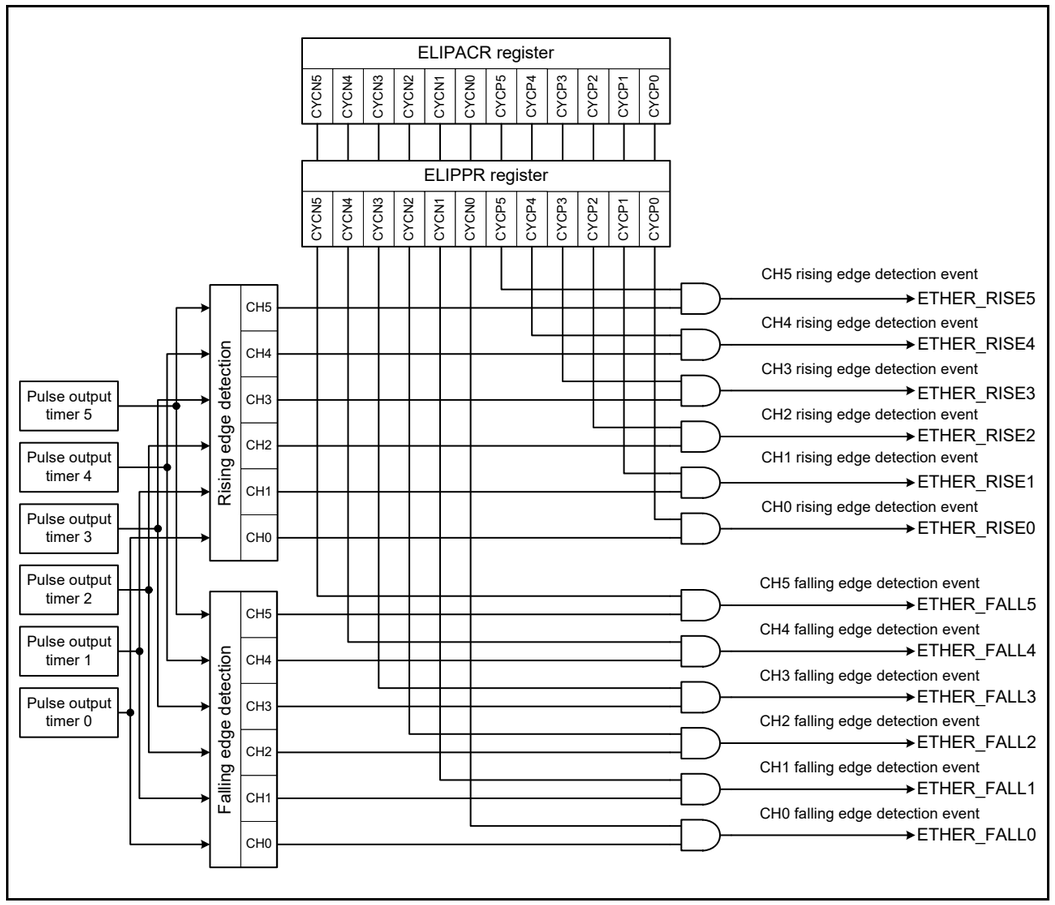


Figure 30.34 Relationship between the pulse output timer and the ELC

30.5 事件链接（输出）

EPTPC可以通过检测来自脉冲输出定时器的脉冲的上升沿或下降沿来向ELC输出事件。图30.34显示了脉冲输出定时器和ELC之间的关系。

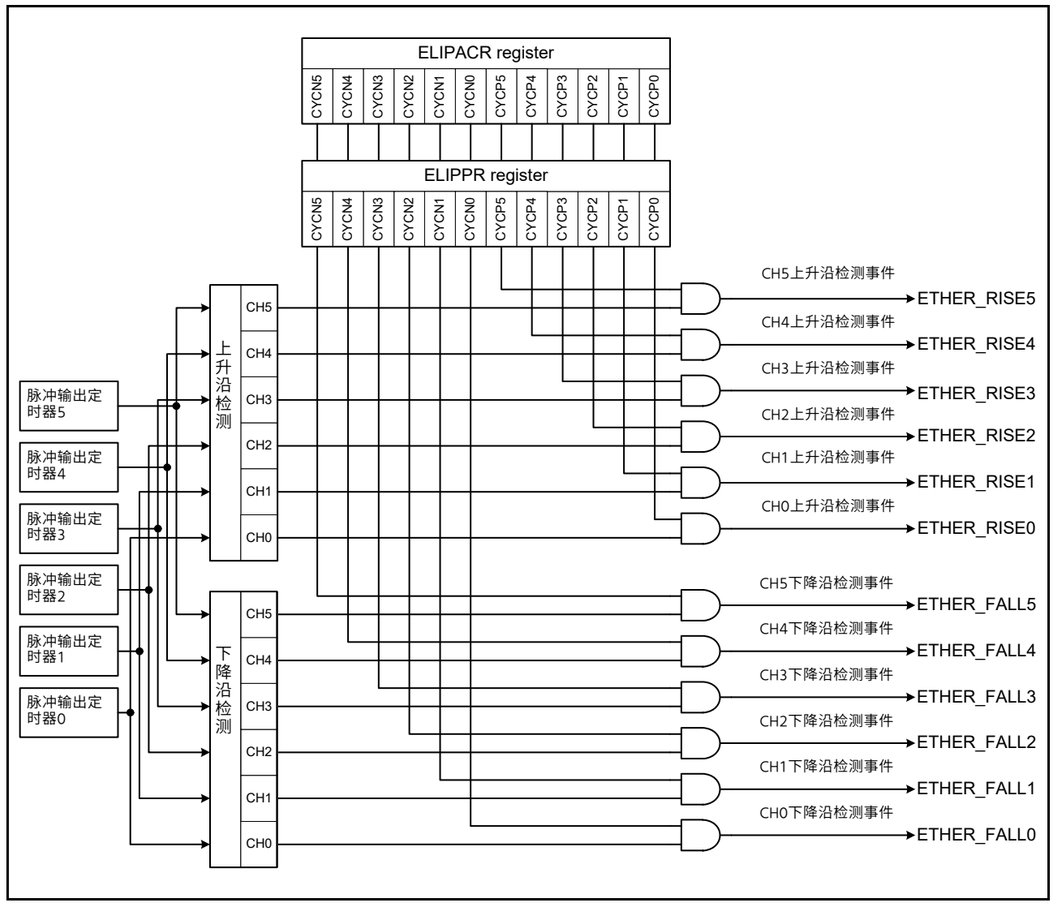


Figure 30.34 脉冲输出定时器与ELC的关系

30.6 Usage Notes

30.6.1 Constraints on Register Access

When the EPTPC and PTPEDMAC operations are enabled (MSTPCRB.MSTPB13 = 0), some registers in the EPTPC become inaccessible depending on the setting combination of the MSTPCRB.MSTPB15 bit and EPTPC bypass bit (BYPASS.BYPASS0 bit). Table 30.24 to Table 30.25 summarize the constraints on access to the registers.

Table 30.24 Constraints on register access when no channels are bypassed (BYPASS.BYPASS0 = 0)

Constraints on register access				
Ethernet port usage	Allocation of register addresses for access			
MSTPB15 setting (EMACC0 and EDMAC0)	4006 4500h to 4006 45FFh	4006 5000h to 4006 503Fh	4006 5040h to 4006 53FFh (STCA)	4006 5800h to 4006 5BFFh (SYNFP0)
0	Accessible	Accessible	Accessible	Accessible
1	Accessible	Access prohibited	Access prohibited	Access prohibited

Table 30.25 Constraints on register access when channel 0 is bypassed (BYPASS.BYPASS0 = 1)

Constraints on register access				
Ethernet port usage	Allocation of register addresses for access			
MSTPB15 setting (ETHERC0 and EDMAC0)	4006 4500h to 4006 45FFh	4006 5000h to 4006 503Fh	4006 5040h to 4006 53FFh (STCA)	4006 5800h to 4006 5BFFh (SYNFP0)
0	Accessible	Access prohibited	Access prohibited	Access prohibited
1	Accessible	Access prohibited	Access prohibited	Access prohibited

Note: Access to an access-prohibited register can lead to a bus timeout error. If a bus timeout error occurs, set the PTRSTR.RESET bit to 1 to reset the EPTPC by software.

30.6.2 Wait Cycles for Register Access

Access to registers in the EPTPC involves the arbitration of different clock signals, specifically the peripheral module clock signal (PCLKA), the STCA clock signal, and the MII clock signals such as TX_CLK. Accordingly, the number of wait cycles for register access differs depending on the combination of the frequency settings for these clock signals.

Table 30.26 gives examples of numbers of wait cycles for different combinations. Add 1 to 2 cycles to these values to obtain the number of access cycles.

Table 30.26 Wait cycles for register access when the STCA clock is 20 MHz

	STCA clock = 20 MHz							
	Peripheral module clock PCLKA = 120 MHz				Peripheral module clock PCLKA = 20 MHz			
	MII clock 25 MHz (100 Mbps)		MII clock 2.5 MHz (10 Mbps)		MII clock 25 MHz (100 Mbps)		MII clock 2.5 MHz (10 Mbps)	
Address range	Read	Write	Read	Write	Read	Write	Read	Write
4006 4500h to 4006 45FFh	2	2	2	2	2	2	2	2
4006 5000h to 4006 503Fh	4	4	4	4	4	4	4	4
4006 5040h to 4006 53FFh (STCA)	7	27 to 41*1	7	27 to 41*1	7	15 to 17*1	7	15 to 17*1
4006 5800h to 4006 5BFFh (SYNFP0)	8	23 to 33*2	8	111 to 209*2	8	15 to 17*2	8	31 to 49*2

Note 1. The number of wait cycles in access to the STCA-related registers (W_{STCA}) can be calculated to the following range from the periods of the peripheral module clock ($t_{c(PCLKA)}$) and STCA clock ($t_{c(STCA)}$).
Minimum value of W_{STCA} = Int ($t_{c(STCA)}/t_{c(PCLKA)}$) × 2 + 15 ($t_{c(PCLKA)} \leq t_{c(STCA)}$)

30.6 使用说明

30.6.1 注册访问的限制

当EPTPC和PTPEDMAC操作被启用(MSTPCRB.MSTPB13=0)时，根据MSTPCRB.MSTPB15位和EPTPC旁路位(BYPASS.BYPASS0位)的设置组合，EPTPC中的一些寄存器变得不可访问。表30.24至表30.25总结了对寄存器访问的限制。

Table 30.24 未绕过任何通道时的寄存器访问限制(BYPASS.BYPASS0=0)

注册访问的限制				
以太网端口使用情况	为访问分配寄存器地址			
MSTPB15设置（EMACC0和EDMAC0）	4006 4500h to 4006 45FFh	4006 5000h to 4006 503Fh	4006 5040h to 4006 53FFh (STCA)	4006 5800h to 4006 5BFFh (SYNFP0)
0	Accessible	Accessible	Accessible	Accessible
1	Accessible	禁止访问	禁止访问	禁止访问

Table 30.25 绕过通道0时的寄存器访问限制(BYPASS.BYPASS0=1)

注册访问的限制				
以太网端口使用情况	为访问分配寄存器地址			
MSTPB15设置（ETHERC0和EDMAC0）	4006 4500h to 4006 45FFh	4006 5000h to 4006 503Fh	4006 5040h to 4006 53FFh (STCA)	4006 5800h to 4006 5BFFh (SYNFP0)
0	Accessible	禁止访问	禁止访问	禁止访问
1	Accessible	禁止访问	禁止访问	禁止访问

Note: 访问禁止访问的寄存器会导致总线超时错误。如果发生总线超时错误，将PTRSTR.RESET位设置为1以通过软件复位EPTPC。

30.6.2 寄存器访问的等待周期

EPTPC中寄存器的访问涉及到不同时钟信号的仲裁，具体是外设模块时钟信号（PCLKA）、STCA时钟信号和TX_CLK等MII时钟信号。因此，寄存器访问的等待周期数取决于这些时钟信号的频率设置的组合。

表30.26给出了不同组合的等待周期数示例。将这些值加上1到2个周期以获得访问周期数。

Table 30.26 STCA时钟为20MHz时寄存器访问的等待周期

	STCA clock = 20 MHz							
	外设模块时钟PCLKA=120MHz				外设模块时钟PCLKA=20MHz			
	MII clock 25 MHz (100 Mbps)		MII clock 2.5 MHz (10 Mbps)		MII clock 25 MHz (100 Mbps)		MII clock 2.5 MHz (10 Mbps)	
地址范围	Read	Write	Read	Write	Read	Write	Read	Write
4006 4500h to 4006 45FFh	2	2	2	2	2	2	2	2
4006 5000h to 4006 503Fh	4	4	4	4	4	4	4	4
4006 5040h to 4006 53FFh (STCA)	7	27 to 41*1	7	27 to 41*1	7	15 to 17*1	7	15 to 17*1
4006 5800h to 4006 5BFFh (SYNFP0)	8	23 to 33*2	8	111 to 209*2	8	15 to 17*2	8	31 to 49*2

Note 1. 访问STCA相关寄存器的等待周期数(WSTCA)可以从外围模块时钟(tc(PCLKA))和STCA时钟(tc(STCA))的周期计算到以下范围。WSTCA的最小值

= 15 ($t_{c(PCLKA)} > t_{c(STCA)}$)

Maximum value of W_{STCA} = Int ($t_{c(STCA)}/t_{c(PCLKA)}$) × 4 + 17 ($t_{c(PCLKA)} \leq t_{c(STCA)}$)

= 17 ($t_{c(PCLKA)} > t_{c(STCA)}$)

- Int(A) is the calculation of the largest integer not greater than A.
- This calculation assumes that the CPU clock and peripheral module clock have the same periods.

For example, if the frequency of the peripheral module clock is 120 MHz and that of the STCA clock is 1/6 that of the peripheral module clock (= 20 MHz),

Minimum value of W_{STCA} = Int (50 [ns]/8.3 [ns]) × 2 + 15 = 27, and

Maximum value of W_{STCA} = Int (50 [ns]/8.3 [ns]) × 4 + 17 = 41.

If REF50CK0 is used as the STCA clock, the frequency of the STCA clock is 25 MHz.

Note 2. The number of wait cycles in access to the SYNFP-related registers (W_{SYNF}) can be calculated to the following range from the periods of the peripheral module clock ($t_{c(PCLKA)}$) and MII clock ($t_{c(MII)}$).

Minimum value of W_{SYNF} = Int ($t_{c(MII)}/t_{c(PCLKA)}$) × 2 + 15 ($t_{c(PCLKA)} \leq t_{c(MII)}$)

= 15 ($t_{c(PCLKA)} > t_{c(MII)}$)

Maximum value of W_{SYNF} = Int ($t_{c(MII)}/t_{c(PCLKA)}$) × 4 + 17 ($t_{c(PCLKA)} \leq t_{c(MII)}$)

= 17 ($t_{c(PCLKA)} > t_{c(MII)}$)

- Int(A) is the calculation of the largest integer not greater than A.
- This calculation assumes that the CPU clock and peripheral module clock have the same periods.

For example, if the frequency of the peripheral module clock is 120 MHz and the transmission rate is 10 Mbps (so the MII clock is running at 2.5 MHz),

Minimum value of W_{SYNF} = Int (400 [ns]/8.3 [ns]) × 2 + 15 = 111, and

Maximum value of W_{SYNF} = Int (400 [ns]/8.3 [ns]) × 4 + 17 = 209.

= 15 (t > t)

WSTCA的最大值=Int(tc(STCA)tc(PCLKA))×4+17(tc(PCLKA) tc(STCA))=17(tc(PCLKA)>tc(STCA))•Int(A)是不大于A的最大整数的计算。•该计算假设CPU时钟和外围模块时钟具有相同的周期。

例如，如果外围模块时钟频率为120MHz，STCA时钟频率为外围模块时钟频率的16(=20MHz)，则WSTCA的最小值

=整数(50[ns]8.3[ns])×2+15=27，并且

WSTCA的最大值=Int(50[ns]8.3[ns])×4+17=41。如果使用REF50CK0作为STCA时钟，则STCA时钟的频率为25MHz。

Note 2. 访问SYNFP相关寄存器的等待周期数(WSYNF)可以从外围模块时钟(tc(PCLKA))和MII时钟(tc(MII))的周期计算到以下范围。WSYNF的最小值

= 15 (t > t)

WSYNF的最大值=Int(tc(MII)tc(PCLKA))×4+17(tc(PCLKA) tc(MII))=17(tc(PCLKA)>tc(MII))•Int(A)是不大于A的最大整数的计算。•该计算假设CPU时钟和外围模块时钟具有相同的周期。

例如，如果外围模块时钟的频率为120MHz，传输速率为10Mbps（因此MII时钟运行在2.5MHz），

WSYNF的最小值 =整数(400[ns]8.3[ns])×2+15=111，并且

WSYNF的最大值 = Int (400 [ns]/8.3 [ns]) × 4 + 17 = 209.

31. Ethernet DMA Controller (EDMAC)

31.1 Overview

The MCU provides two channels for the Ethernet DMA Controller (EDMAC), one channel for the Ethernet Controller (ETHERC) and one channel for the Ethernet PTP Controller (EPTPC). EDMAC0 controls data transmission and reception for ETHERC0. The PTPEDMAC controls data transmission and reception for ETHERC0 based on the EPTPC settings.

The EDMAC controls most of the transmit and receive buffer management for communications. This reduces the load on the CPU and allows efficient data transmission and reception. The data transfers are controlled according to the information referred to as descriptors, in memory.

Table 31.1 lists the EDMAC specifications and Figure 31.1 shows the configuration. Figure 31.2 shows the configuration of descriptors and transmit and receive buffers in memory.

Table 31.1 EDMAC specifications

Parameter	Specifications
Data transmission and reception	• Controls data transmission and reception according to descriptors • Supports single buffer frame transmission and reception (1 buffer per frame) and multi-buffer frame transmission and reception (multiple buffers per frame)
Functions	• Minimizes system bus occupancy time using block transfer (32-byte units) • Writes back the transmit or receive frame state to descriptors • Inserts padding in receive data
Module-stop function	Module-stop state can be set to reduce power consumption

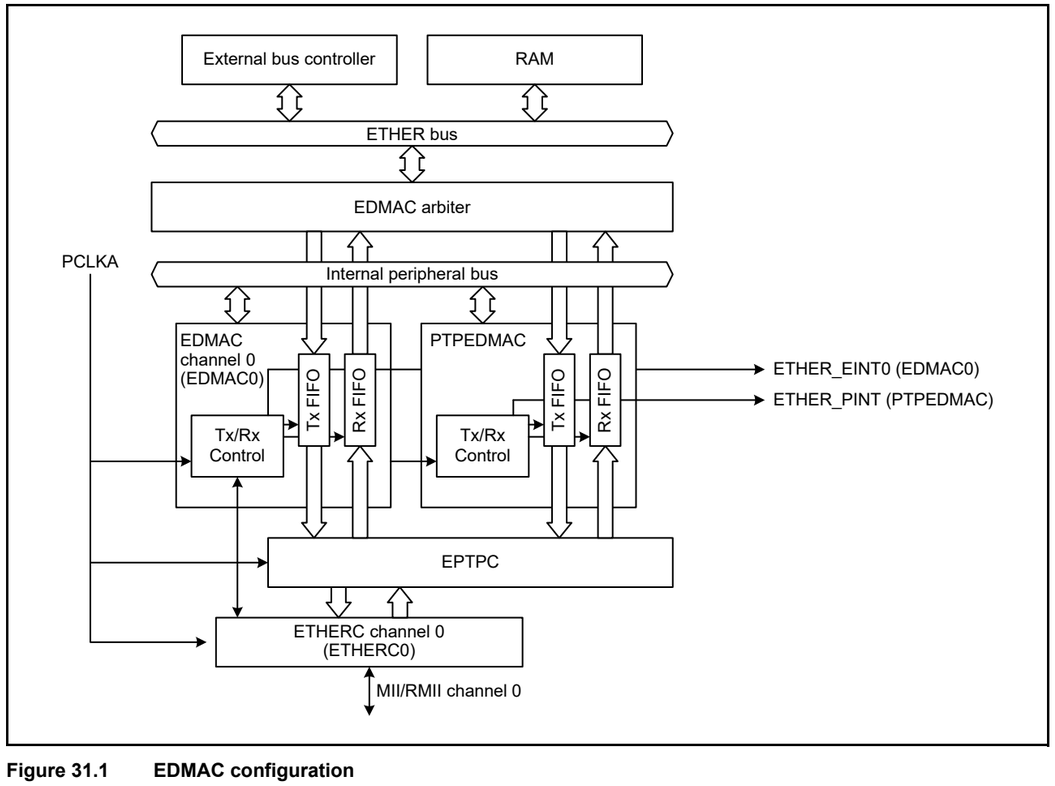


Figure 31.1 EDMAC configuration

31. 以太网DMA控制器(EDMAC)

31.1 Overview

MCU为以太网DMA控制器(EDMAC)提供两个通道，一个为以太网控制器(ETHERC)提供一个通道，一个为以太网PTP控制器(EPTPC)提供一个通道。EDMAC0控制ETHERC0的数据传输和接收。PTPEDMAC根据EPTPC设置控制ETHERC0的数据传输和接收。

EDMAC控制大部分用于通信的发送和接收缓冲区管理。这减少了CPU的负载并允许高效的数据传输和接收。数据传输是根据内存中称为描述符的信息进行控制的。

表31.1列出了EDMAC规范，图31.1显示了配置。图31.2显示了内存中描述符以及发送和接收缓冲区的配置。

Table 31.1 EDMAC specifications

Parameter	Specifications
数据传输和接收	根据描述符控制数据发送和接收 支持单缓冲区帧发送和接收（每帧1个缓冲区）和多缓冲区帧发送和接收（每帧多个缓冲区）
Functions	使用块传输（32字节单位）最小化系统总线占用时间 将发送或接收帧状态写回描述符 在接收数据中插入填充
Module-stop function	可设置模块停止状态以降低功耗

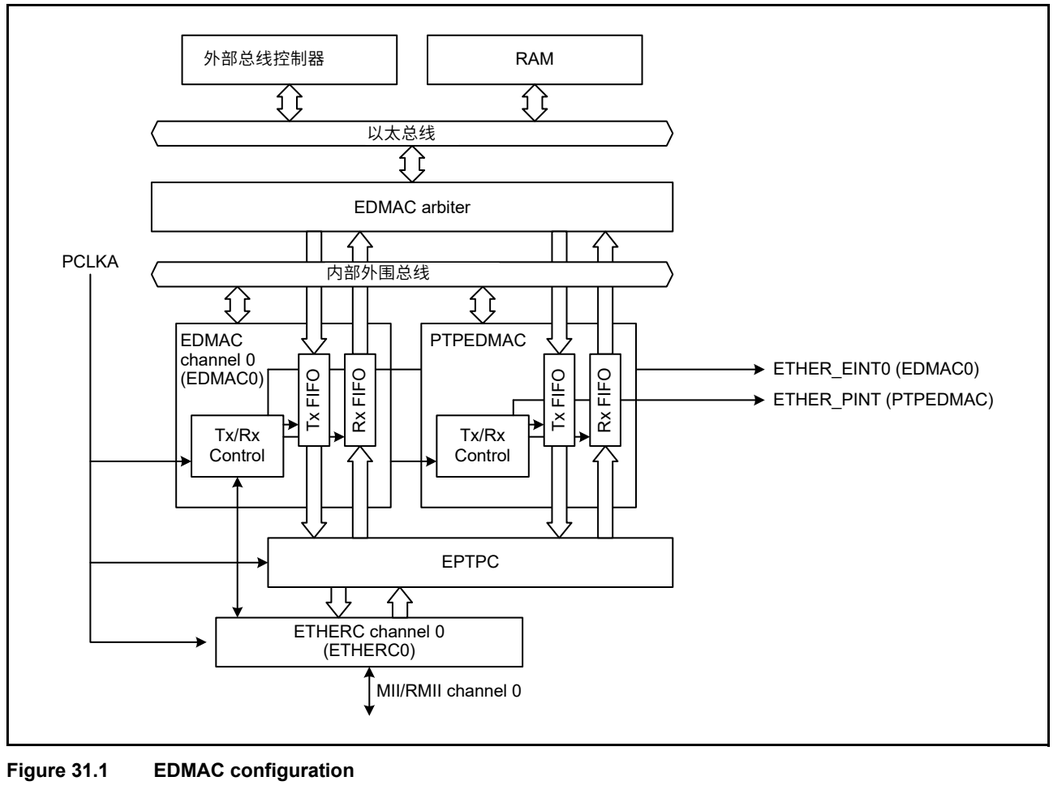


Figure 31.1 EDMAC configuration

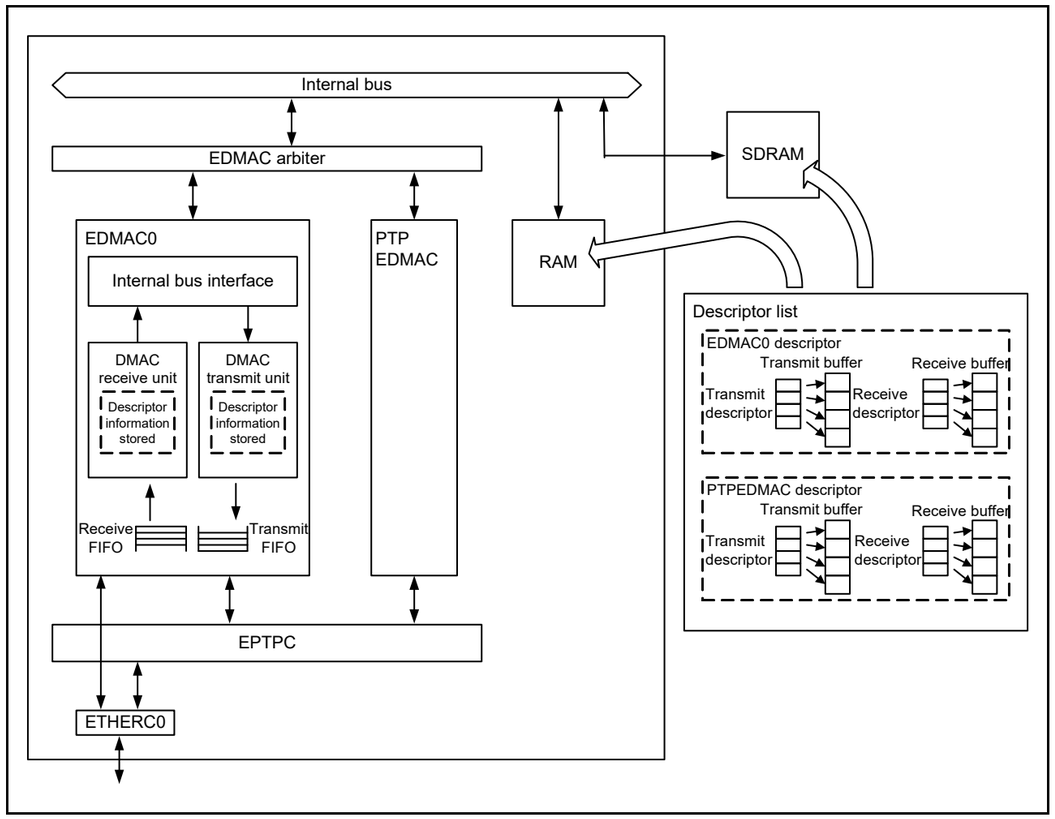


Figure 31.2 Configuration of descriptors and transmit and receive buffers in memory

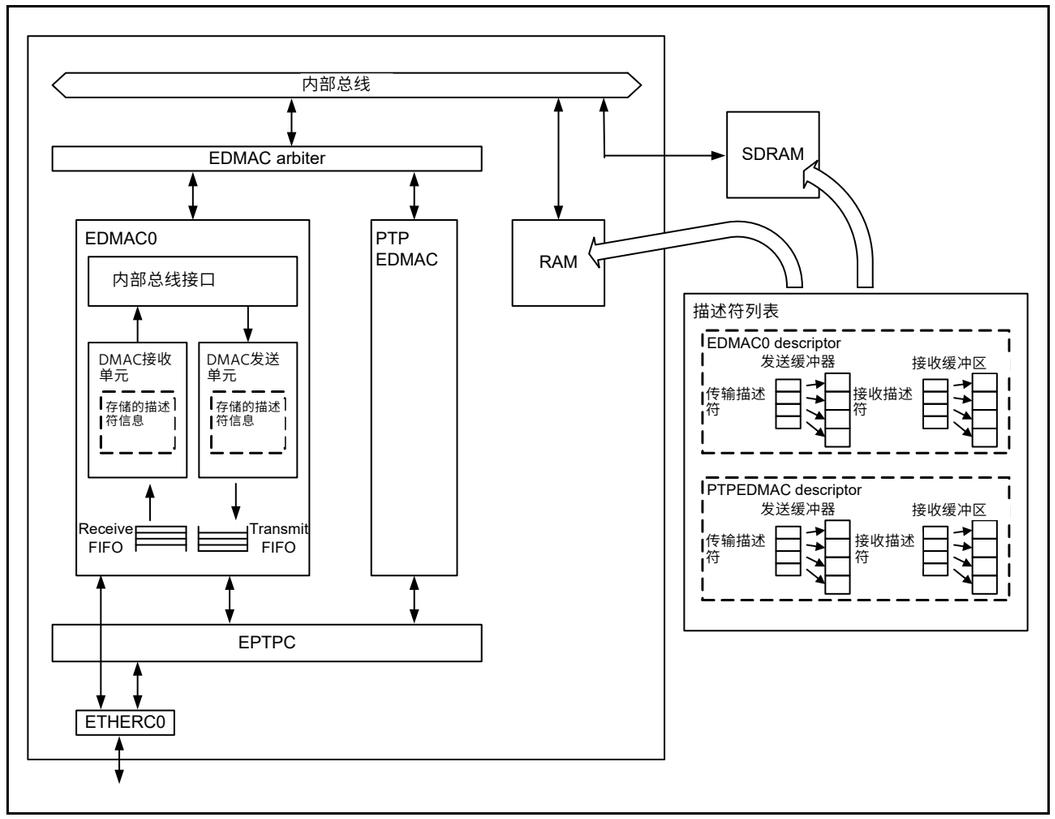


Figure 31.2 在内存中配置描述符和发送和接收缓冲区

31.2 Register Descriptions

31.2.1 EDMAC Mode Register (EDMR)

Address(es): EDMAC0.EDMR 4006 4000h, PTPEDMAC.EDMR 4006 4400h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	DE	DL[1:0]		—	—	—	SWR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	SWR	Software Reset	When 1 is written, the associated channels of the EDMAC and ETHERC are reset. Note: The ETHERC is not reset for the PTPEDMAC. The TDLAR, RDLAR, RMFCR, TFUCR, and RFOCR registers are not reset with this bit.The read value is 0.	R/W
b3 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b5, b4	DL[1:0]	Transmit/Receive Descriptor Length	b5 b4 0 0: 16 bytes 0 1: 32 bytes 1 0: 64 bytes 1 1: 16 bytes.	R/W
b6	DE	Big Endian Mode/Little Endian Mode*1	0: Big endian mode 1: Little endian mode.	R/W
b31 to b7	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. This setting applies to data for the transmit and receive buffers. It does not apply to transmit and receive descriptors and registers.

The EDMR register controls EDMAC operation. Set the EDMR register during initialization process after a reset. When rewriting this register outside of the initialization process, set the SWR bit to 1 to reset the EDMAC and ETHERC, and then set this register again. If the ETHERC and EDMAC are reset during data transmission or reception, abnormal data might be sent on the line. Do not rewrite this register while the ETHERC transmit or receive function is enabled. It takes 64 cycles of the peripheral module clock (PCLKA) to initialize the ETHERC and EDMAC. Complete the initialization before accessing registers in the ETHERC and EDMAC.

31.2 注册说明

31.2.1 EDMAC模式寄存器(EDMR)

Address(es): EDMAC0.EDMR 4006 4000h, PTPEDMAC.EDMR 4006 4400h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	DE	DL[1:0]		—	—	—	SWR
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	SWR	软件复位	当写入1时，EDMAC的相关通道和 ETHERC被重置。 注意：不会为PTPEDMAC重置ETHERC。 TDLAR、RDLAR、RMFCR、TFUCR和RFOCR寄存器不会用该位复位。读取值为0。	R/W
b3 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b5, b4	DL[1:0]	Transmit/Receive Descriptor Length	b5 b4 0 0: 16 bytes 0 1: 32 bytes 1 0: 64 bytes 1 1: 16 bytes.	R/W
b6	DE	Big Endian Mode/Little Endian Mode*1	0：大端模式1：小端 模式。	R/W
b31 to b7	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 此设置适用于发送和接收缓冲区的数据。它不适用于发送和接收描述符和寄存器。

EDMR寄存器控制EDMAC操作。在复位后的初始化过程中设置EDMR寄存器。在初始化过程之外重写该寄存器时，将SWR位设置为1以复位EDMAC和ETHERC，然后再次设置该寄存器。如果ETHERC和EDMAC在数据传输或接收过程中被复位，可能会在线路上发送异常数据。在启用ETHERC发送或接收功能时不要重写该寄存器。初始化ETHERC和EDMAC需要64个外围模块时钟(PCLKA)周期。在访问ETHERC和EDMAC中的寄存器之前完成初始化。

31.2.2 EDMAC Transmit Request Register (EDTRR)

Address(es): EDMAC0.EDTRR 4006 4008h, PTPEDMAC.EDTRR 4006 4408h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	TR	Transmit Request	When 1 is written, the EDMAC reads the associated descriptor and transmits frames where the TD0.TACT bit is 1. The TR bit clears to 0 after all the valid frames are transmitted. Writing 0 to this bit has no effect.	R/W
b31 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The EDTRR register controls EDMAC transmission. After the EDMAC transmits one frame, it reads the next descriptor. When the TD0.TACT bit in the descriptor is 1, the EDMAC continues transmission. When the TD0.TACT bit is 0, the EDMAC sets the TR bit to 0 and stops transmission.

31.2.3 EDMAC Receive Request Register (EDRRR)

Address(es): EDMAC0.EDRRR 4006 4010h, PTPEDMAC.EDRRR 4006 4410h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	RR	Receive Request	0: Disable the receive function*1 1: Read receive descriptor and enable the receive function.	R/W
b31 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. If the receive function is disabled during frame reception, write-back to the receive descriptor is not performed successfully. Subsequent pointers for reading a receive descriptor become abnormal and the EDMAC cannot operate normally. In this case, to enable the EDMAC receive function again, execute a software reset by setting the EDMR.SWR bit to 1.
To disable the EDMAC receive function without resetting the EDMAC, set the ETHERC0.ECMR.RE bit to 0. After the EDMAC completes reception and write-back to the receive descriptor is confirmed, set the RR bit to 0.

The EDRRR register controls EDMAC reception. When the RR bit sets to 1, the EDMAC reads the receive descriptor. When the RD0.RACT bit is 1, the EDMAC waits for a receive request from the ETHERC. When the EDMAC has received data for the receive buffer size, it reads the next descriptor and waits to receive a frame. If the RD0.RACT bit is 0, the EDMAC sets the RR bit to 0 and stops reception.

31.2.2 EDMAC发送请求寄存器(EDTRR)

Address(es): EDMAC0.EDTRR 4006 4008h, PTPEDMAC.EDTRR 4006 4408h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TR
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	TR	发送请求	写入1时，EDMAC读取相关描述符并发送TD0.TACT位为1的帧。发送完所有有效帧后，TR位清零。向该位写入0无效。	R/W
b31 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

EDTRR寄存器控制EDMAC传输。EDMAC传输一帧后，读取下一个描述符。
当描述符中的TD0.TACT位为1时，EDMAC继续传输。当TD0.TACT位为0时，EDMAC将TR位设置为0并停止传输。

31.2.3 EDMAC接收请求寄存器(EDRRR)

Address(es): EDMAC0.EDRRR 4006 4010h, PTPEDMAC.EDRRR 4006 4410h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RR
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	RR	接收请求	0：关闭接收功能*11：读取接收描述符，开启接收功能。	R/W
b31 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 如果在帧接收期间禁用接收功能，则无法成功执行对接收描述符的回写。
后续读取接收描述符的指针异常，EDMAC不能正常工作。在这种情况下，要再次启用EDMAC接收功能，通过将EDMR.SWR位设置为1来执行软件复位。要禁用EDMAC接收功能而不重置EDMAC，请将ETHERC0.ECMR.RE位设置为0。EDMAC完成接收并确认回写到接收描述符，将RR位设置为0。

EDRRR寄存器控制EDMAC接收。当RR位设置为1时，EDMAC读取接收描述符。
当RD0.RACT位为1时，EDMAC等待来自ETHERC的接收请求。当EDMAC接收到接收缓冲区大小的数据时，它会读取下一个描述符并等待接收帧。如果RD0.RACT位为0，则EDMAC将RR位设置为0并停止接收。

31.2.4 Transmit Descriptor List Start Address Register (TDLAR)

Address(es): EDMAC0.TDLAR 4006 4018h, PTPEDMAC.TDLAR 4006 4418h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b31 to b0	—	—	These bits specify the start address of the transmit descriptor list. Set the start address according to the descriptor length selected in the EDMR.DL[1:0] bits. • 16-byte boundary: Lower 4 bits = 0000b • 32-byte boundary: Lower 5 bits = 00000b • 64-byte boundary: Lower 6 bits = 000000b.	R/W

The TDLAR register specifies the start address of the transmit descriptor list. Align each descriptor on the associated boundary to the descriptor length selected in the EDMR.DL[1:0] bits. Do not rewrite the TDLAR register during transmission. Rewrite the TDLAR register while the EDTRR.TR bit is 0.

31.2.5 Receive Descriptor List Start Address Register (RDLAR)

Address(es): EDMAC0.RDLAR 4006 4020h, PTPEDMAC.RDLAR 4006 4420h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b31 to b0	—	—	The start address of the receive descriptor list is set. Set the start address according to the descriptor length selected in the EDMR.DL[1:0] bits. • 16-byte boundary: Lower 4 bits = 0000b • 32-byte boundary: Lower 5 bits = 00000b • 64-byte boundary: Lower 6 bits = 000000b.	R/W

The RDLAR register specifies the start address of the receive descriptor list. Allocate each descriptor on the associated boundary to the descriptor length selected in the EDMR.DL[1:0] bits. Do not rewrite the RDLAR register during reception. Rewrite the RDLAR register while the EDRRR.RR bit is 0.

31.2.4 发送描述符列表起始地址寄存器(TDLAR)

Address(es): EDMAC0.TDLAR 4006 4018h, PTPEDMAC.TDLAR 4006 4418h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b31 to b0	—	—	这些位指定发送描述符列表的起始地址。根据在EDMR.DL[1:0]位中选择的描述符长度设置起始地址。 16字节边界：低4位=0000b 32字节边界：低5位=00000b 64字节边界：低6位=000000b。	R/W

TDLAR寄存器指定发送描述符列表的起始地址。将相关边界上的每个描述符与在EDMR.DL[1:0]位中选择的描述符长度对齐。发送期间不要重写TDLAR寄存器。在EDTRR.TR位为0时重写TDLAR寄存器。

31.2.5 接收描述符列表起始地址寄存器(RDLAR)

Address(es): EDMAC0.RDLAR 4006 4020h, PTPEDMAC.RDLAR 4006 4420h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b31 to b0	—	—	设置接收描述符列表的起始地址。根据在EDMR.DL[1:0]位中选择的描述符长度设置起始地址。 16字节边界：低4位=0000b 32字节边界：低5位=00000b 64字节边界：低6位=000000b。	R/W

RDLAR寄存器指定接收描述符列表的起始地址。将相关边界上的每个描述符分配给在EDMR.DL[1:0]位中选择的描述符长度。接收期间不要重写RDLAR寄存器。在EDRRR.RR位为0时重写RDLAR寄存器。

31.2.6 ETHERC/EDMAC Status Register (EDMAC0.EESR)

Address(es): EDMAC0.EESR 4006 4028h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	TWB	—	—	—	TABT	RABT	RFCOF	ADE	ECI	TC	TDE	TFUF	FR	RDE	RFOF
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	CND	DLC	CD	TRO	RMAF	—	—	RRF	RTLF	RTSF	PRE	CERF
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	CERF	CRC Error Flag	0: CRC error not detected 1: CRC error detected.	R/W
b1	PRE	PHY-LSI Receive Error Flag	0: PHY-LSI receive error not detected 1: PHY-LSI receive error detected.	R/W
b2	RTSF	Frame-Too-Short Error Flag	0: Frame-too-short error not detected 1: Frame-too-short error detected.	R/W
b3	RTLF	Frame-Too-Long Error Flag	0: Frame-too-long error not detected 1: Frame-too-long error detected.	R/W
b4	RRF	Alignment Error Flag	0: Alignment error not detected 1: Alignment error detected.	R/W
b6, b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	RMAF	Multicast Address Frame Receive Flag	0: Multicast address frame not received 1: Multicast address frame received.	R/W
b8	TRO	Transmit Retry Over Flag	0: Transmit retry-over condition not detected 1: Transmit retry-over condition detected.	R/W
b9	CD	Late Collision Detect Flag	0: Late collision not detected 1: Late collision detected during frame transmission.	R/W
b10	DLC	Loss of Carrier Detect Flag	0: Loss of carrier not detected 1: Loss of carrier detected during frame transmission.	R/W
b11	CND	Carrier Not Detect Flag	0: Carrier detected when transmission started 1: Carrier not detected during preamble transmission.	R/W
b15 to b12	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b16	RFOF	Receive FIFO Overflow Flag	0: No overflow occurred 1: Overflow occurred.	R/W
b17	RDE	Receive Descriptor Empty Flag	0: EDMAC detected that the receive descriptor valid bit (RD0.RACT) is 1 1: EDMAC detected that the receive descriptor valid bit (RD0.RACT) is 0.	R/W
b18	FR	Frame Receive Flag	0: Frame not received 1: Frame received and update of the receive descriptor is complete.	R/W
b19	TFUF	Transmit FIFO Underflow Flag	0: No underflow occurred 1: Underflow occurred.	R/W
b20	TDE	Transmit Descriptor Empty Flag	0: EDMAC detected that the transmit descriptor valid bit (TD0.TACT) is 1 1: EDMAC detected that the transmit descriptor valid bit (TD0.TACT) is 0.	R/W
b21	TC	Frame Transfer Complete Flag	0: Transfer not complete or no transfer requested 1: All frames indicated in the transmit descriptor were completely transferred to the transmit FIFO.	R/W

31.2.6 ETHERCEDMAC状态寄存器(EDMAC0.EESR)

Address(es): EDMAC0.EESR 4006 4028h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	TWB	—	—	—	TABT	RABT	RFCOF	ADE	ECI	TC	TDE	TFUF	FR	RDE	RFOF
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	CND	DLC	CD	TRO	RMAF	—	—	RRF	RTLF	RTSF	PRE	CERF
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	CERF	CRC错误标志	0：未检测到CRC错误1： 检测到CRC错误。	R/W
b1	PRE	PHY-LSI接收错误标志	0：未检测到PHY-LSI接收错误1：检 测到PHY-LSI接收错误。	R/W
b2	RTSF	帧太短错误标志	0：未检测到帧太短错误1：检测到帧 太短错误。	R/W
b3	RTLF	帧过长错误标志	0：未检测到帧过长错误1：检测到 帧过长错误。	R/W
b4	RRF	对齐错误标志	0：未检测到对齐错误1：检测 到对齐错误。	R/W
b6, b5	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b7	RMAF	组播地址帧接收 Flag	0：未收到组播地址帧1：收到组播地址 帧。	R/W
b8	TRO	发送重试标志	0：未检测到发送重试条件1：检测到发送重 试条件。	R/W
b9	CD	后期碰撞检测标志	0：未检测到后期冲突1：在帧传输期间检测到后期 冲突。	R/W
b10	DLC	载波检测标志丢失	0：未检测到载波丢失1：在帧传输过程中检测到载波 丢失。	R/W
b11	CND	运营商未检测标志	0：传输开始时检测到载波1：前导传输期间未检测到 载波。	R/W
b15 to b12	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b16	RFOF	接收FIFO溢出标志	0：未发生溢出1：发生 溢出。	R/W
b17	RDE	接收描述符空标志	0：EDMAC检测到接收描述符有效位（RD0.RACT）为11 ：EDMAC检测到接收描述符有效位（RD0.RACT）为0。	R/W
b18	FR	帧接收标志	0：未接收到帧1：接收到帧并且接收描述符的更新完成。	R/W
b19	TFUF	发送FIFO下溢标志	0：未发生下溢1：发生 下溢。	R/W
b20	TDE	发送描述符空标志	0：EDMAC检测到发送描述符有效位（TD0.TACT）为11 ：EDMAC检测到发送描述符有效位（TD0.TACT）为0。	R/W
b21	TC	帧传输完成标志	0：传输未完成或未请求传输1：传输描述符中指示的 所有帧都已完全传输到传输FIFO。	R/W

Bit	Symbol	Bit name	Description	R/W
b22	ECI	ETHERC Status Register Source Flag	0: ETHERC status interrupt source not detected 1: ETHERC status interrupt source detected.	R*1
b23	ADE	Address Error Flag	0: Invalid memory address not detected (normal operation) 1: Invalid memory address detected.*2	R/W
b24	RFCOF	Receive Frame Counter Overflow Flag	0: Receive frame counter did not overflow 1: Receive frame counter overflowed.	R/W
b25	RABT	Receive Abort Detect Flag	0: Frame reception not aborted or no reception requested 1: Frame reception aborted.	R/W
b26	TABT	Transmit Abort Detect Flag	0: Frame transmission not aborted or no transmission requested. 1: Frame transmission aborted.	R/W
b29 to b27	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b30	TWB	Write-Back Complete Flag	0: Write-back not complete or no transmission requested 1: Write-back to the transmit descriptor completed.	R/W
b31	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Note 1. The ECI flag is read-only. When the source in the ETHERC0.ECSR register is cleared, the ECI flag is also cleared.
Note 2. When an address error is detected, the EDMAC halts the process. To resume operation, set the EDMR.SWR bit to 1 (resetting the EDMAC and ETHERC), and then reconfigure the EDMAC and ETHERC.

The EDMAC0.EESR register indicates the ETHERC and EDMAC communication status. Each flag in the EESR register can be output as an interrupt request signal (ETHER_EINT0) from the EDMAC. Writing 1 clears all of the flags except ECI to 0. Writing 0 does not affect any of the flag values. The interrupt sources are enabled by setting the associated bits in the EDMAC0.EESIPR register.

CERF flag (CRC Error Flag)

The CERF flag sets to 1 when an error is detected while checking the frame check sequence (FCS) field of the receive frame.

PRE flag (PHY-LSI Receive Error Flag)

The PRE flag indicates that the RX_ER signal output from the PHY-LSI is high.

RTSF flag (Frame-Too-Short Error Flag)

The RTSF flag indicates that a received frame is less than 64 bytes.

RTLF flag (Frame-Too-Long Error Flag)

The RTLF flag indicates that a received frame is greater than the upper limit of the receive frame length set in the ETHERC0.RFLR register. The excess data is discarded.

RRF flag (Alignment Error Flag)

The RRF flag indicates that a frame is not an integral number of octets. The last word that is not an integral number of octets is not transferred.

RMAF flag (Multicast Address Frame Receive Flag)

The RMAF flag indicates that a multicast frame was received.

TRO flag (Transmit Retry Over Flag)

The TRO flag indicates that a collision occurred again during the 15th retry of frame transmission.

CD flag (Late Collision Detect Flag)

The CD flag indicates that a late collision was detected during frame transmission.

DLC flag (Loss of Carrier Detect Flag)

The DLC flag indicates that a loss of carrier was detected during frame transmission.

Bit	Symbol	位名称	Description	R/W
b22	ECI	ETHERC状态寄存器源 Flag	0：未检测到ETHERC状态中断源1：检测到ETHERC状态中断源。	R*1
b23	ADE	地址错误标志	0：未检测到无效内存地址（正常操作）1：检测到无效内存地址。*2	R/W
b24	RFCOF	接收帧计数器溢出 Flag	0：接收帧计数器未溢出1：接收帧计数器溢出。	R/W
b25	RABT	接收中止检测标志	0：未中止帧接收或未请求接收1：中止帧接收。	R/W
b26	TABT	发送中止检测标志	0：帧传输未中止或未请求传输。1：帧传输中止。	R/W
b29 to b27	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b30	TWB	回写完成标志	0：回写未完成或未请求传输1：对传输描述符的回写完成。	R/W
b31	—	Reserved	该位读取为0。写入值应为0。	R/W

Note 1. ECI标志是只读的。当ETHERC0.ECSR寄存器中的源被清除时，ECI标志也被清除。
Note 2. 当检测到地址错误时，EDMAC会停止该过程。要恢复操作，请将EDMR.SWR位设置为1（重置EDMAC和ETHERC），然后重新配置EDMAC和ETHERC。

EDMAC0.EESR寄存器指示ETHERC和EDMAC通信状态。EESR寄存器中的每个标志都可以作为中断请求信号（ETHER_EINT0）从EDMAC输出。写入1会将除ECI之外的所有标志清除为0。写入0不会影响任何标志值。通过设置EDMAC0.EESIPR寄存器中的相关位来启用中断源。

CERF标志（CRC错误标志）

当在检查接收帧的帧校验序列(FCS)字段时检测到错误时，CERF标志设置为1。

PRE标志（PHY-LSI接收错误标志）

PRE标志表示从PHY-LSI输出的RX_ER信号为高电平。

RTSF标志（Frame-Too-ShortErrorFlag）

RTSF标志表示接收到的帧小于64字节。

RTLF标志（帧过长错误标志）

RTLF标志表示接收到的帧大于设置的接收帧长度的上限ETHERC0.RFLR寄存器。多余的数据被丢弃。

RRF标志（对齐错误标志）

RRF标志表明一个帧不是整数个八位字节。不是整数八位字节的最后一个字不被传送。

RMAF标志（组播地址帧接收标志）

RMAF标志指示接收到多播帧。

TRO标志（传输重试结束标志）

TRO标志表示在第15次帧传输重试期间再次发生冲突。

CD标志（后期碰撞检测标志）

CD标志表示在帧传输期间检测到后期冲突。

DLC标志（丢失载波检测标志）

DLC标志表示在帧传输期间检测到载波丢失。

CND flag (Carrier Not Detect Flag)

The CND flag sets to 1 when a carrier is not detected during preamble transmission.

RFOF flag (Receive FIFO Overflow Flag)

The RFOF flag indicates that the receive FIFO overflowed during frame reception.

RDE flag (Receive Descriptor Empty Flag)

The RDE flag indicates that the read receive descriptor is invalid. When this flag sets to 1, set the RD0.RACT bit in the receive descriptor to 1 and set the EDRRR.RR bit to 1 to resume reception.

FR flag (Frame Receive Flag)

The FR flag indicates that a frame was received and the receive descriptor was updated. The FR flag sets to 1 every time a frame is received.

TFUF flag (Transmit FIFO Underflow Flag)

The TFUF flag indicates that no data remains in the transmit FIFO during frame transmission. Incomplete data is sent to the line.

TDE flag (Transmit Descriptor Empty Flag)

The TDE flag indicates that the TD0.TACT bit of the transmit descriptor is 0 while the previous transmit descriptor indicates that the frame is not complete (TD0.TFP[1:0] bits are 10b or 00b) in multi-buffer frame transmission. As a result, an incomplete frame might be sent.

When this flag sets to 1, perform a software reset and then set the EDTRR.TR bit to 1 to resume transmission. Transmission starts from the address stored in the TDLAR register.

TC flag (Frame Transfer Complete Flag)

The TC flag indicates that all the data specified in the transmit descriptor was transmitted from the ETHERC. This flag sets to 1 when one frame was transmitted in single-buffer frame transmission or when the last data of a frame is transmitted in multi-buffer frame transmission and the TD0.TACT bit in the next transmit descriptor is 0. After frame transmission is complete, the EDMAC writes the transfer status back to the descriptor.

ECI flag (ETHERC Status Register Source Flag)

The ECI flag sets to 1 when an interrupt request is generated by the ETHERC.ECSR register.

ADE flag (Address Error Flag)

The ADE flag indicates that the memory address that the EDMAC tried to use for transfer is invalid.

RFCOF flag (Receive Frame Counter Overflow Flag)

The RFCOF flag indicates that the next frame reception started while the number of frames stored in the receive FIFO reached the maximum number of frames (16 frames). The received frame is discarded while the RFCOF flag is 1.

RABT flag (Receive Abort Detect Flag)

The RABT flag indicates that the ETHERC aborted frame reception because of a CRC error, PHY-LSI receive error, frame-too-short error, frame-too-long error, or other error.

TABT flag (Transmit Abort Detect Flag)

The TABT flag indicates that the ETHERC aborted frame transmission because of transmit retry over, loss of carrier, no carrier detection, or other error.

TWB flag (Write-Back Complete Flag)

The TWB flag indicates the EDMAC completed writing back to the descriptor after frame transmission. This flag sets to 1 after each frame transmission when the TRIMD.TIM bit is 0. It only sets to 1 when the TRIMD.TIS bit is 1.

CND标志（载波未检测标志）

当在前导码传输期间未检测到载波时，CND标志设置为1。

RFOF标志（接收FIFO溢出标志）

RFOF标志表示接收FIFO在帧接收期间溢出。

RDE标志（接收描述符空标志）

RDE标志指示读取的接收描述符无效。当该标志设置为1时，将接收描述符中的RD0.RACT位设置为1，并将EDRRR.RR位设置为1以恢复接收。

FR标志（帧接收标志）

FR标志表示接收到一个帧并且接收描述符已更新。每次接收到一帧时，FR标志设置为1。

TFUF标志（发送FIFO下溢标志）

TFUF标志表示在帧传输期间没有数据保留在传输FIFO中。不完整的数据被发送到线路。

TDE标志（传输描述符空标志）

TDE标志表示发送描述符的TD0.TACT位为0，而前一个发送描述符表示在多缓冲区帧传输中该帧未完成（TD0.TFP[1:0]位为10b或00b）。因此，可能会发送不完整的帧。

当该标志设置为1时，执行软件复位，然后将EDTRR.TR位设置为1以恢复传输。
传输从存储在TDLAR寄存器中的地址开始。

TC标志（帧传输完成标志）

TC标志表示发送描述符中指定的所有数据都是从ETHERC发送的。当在单缓冲帧传输中传输一帧或在多缓冲帧传输中传输一帧的最后一个数据并且下一个传输描述符中的TD0.TACT位为0时，此标志设置为1。完成后，EDMAC将传输状态写回描述符。

ECI标志（ETHERC状态寄存器源标志）

当ETHERC.ECSR寄存器产生中断请求时，ECI标志设置为1。

ADE标志（地址错误标志）

ADE标志表示EDMAC尝试用于传输的内存地址无效。

RFCOF标志（接收帧计数器溢出标志）

RFCOF标志表示在接收FIFO中存储的帧数达到最大帧数（16帧）时开始下一帧接收。当RFCOF标志为1时，接收到的帧被丢弃。

RABT标志（接收中止检测标志）

RABT标志指示ETHERC由于CRC错误、PHY-LSI接收错误、帧太短错误、帧太长错误或其他错误而中止帧接收。

TABT标志（发送中止检测标志）

TABT标志指示ETHERC由于传输重试、载波丢失、未检测到载波或其他错误而中止帧传输。

TWB标志（回写完成标志）

TWB标志表示EDMAC在帧传输后完成写回描述符。当TRIMD.TIM位为0时，此标志在每帧传输后设置为1。仅当TRIMD.TIS位为1时设置为1。

31.2.7 PTP/EDMAC Status Register (PTPEDMAC.EESR)

Address(es): PTPEDMAC.EESR 4006 4428h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	TWB	—	—	—	TABT	—	RFCOF	ADE	—	TC	TDE	TFUF	FR	RDE	RFOF
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	MACE	—	—	—	PVER	TYPE[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	TYPE[3:0]	PTP v2 Message Type Flag	b3 b0 0 0 0 0: Sync 0 0 0 1: Delay_Req 0 0 1 0: Pdelay_Req 0 0 1 1: Pdelay_Resp 1 0 0 0: Follow_Up 1 0 0 1: Delay_Resp 1 0 1 0: Pdelay_Resp_Follow_Up 1 0 1 1: Announce 1 1 0 0: Signaling 1 1 0 1: Management. Other settings are reserved.	R/W
b4	PVER	PTP v2 Packet Flag	0: Current packet is not a PTP v2 packet 1: Current packet is a PTP v2 packet.	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	MACE	MAC Address Mismatch Flag	0: Source MAC address of transmit frame data matches the set value 1: Source MAC address of transmit frame data does not match the set value.	R/W
b15 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b16	RFOF	Receive FIFO Overflow Flag	0: No overflow occurred 1: Overflow occurred.	R/W
b17	RDE	Receive Descriptor Empty Flag	0: EDMAC detected that the receive descriptor valid bit (RD0.RACT) is 1 1: EDMAC detected that the receive descriptor valid bit (RD0.RACT) is 0.	R/W
b18	FR	Frame Receive Flag	0: Frame not received 1: Frame received and receive descriptor updated.	R/W
b19	TFUF	Transmit FIFO Underflow Flag	0: No underflow occurred 1: Underflow occurred.	R/W
b20	TDE	Transmit Descriptor Empty Flag	0: EDMAC detected that the transmit descriptor valid bit (TD0.TACT) is 1 1: EDMAC detected that the transmit descriptor valid bit (TD0.TACT) is 0.	R/W
b21	TC	Frame Transfer Complete Flag	0: Transfer not complete or transfer not requested 1: All frames indicated in the transmit descriptor were completely transferred to the transmit FIFO.	R/W
b22	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b23	ADE	Address Error Flag	0: Invalid memory address not detected (normal operation) 1: Invalid memory address detected.*1	R/W
b24	RFCOF	Receive Frame Counter Overflow Flag	0: Receive frame counter did not overflow 1: Receive frame counter overflowed.	R/W
b25	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

31.2.7 PTPEDMAC状态寄存器(PTPEDMAC.EESR)

Address(es): PTPEDMAC.EESR 4006 4428h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	TWB	—	—	—	TABT	—	RFCOF	ADE	—	TC	TDE	TFUF	FR	RDE	RFOF
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	MACE	—	—	—	PVER	TYPE[3:0]			
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b3 to b0	TYPE[3:0]	PTPv2消息类型标志	b3b00000：Sync0001：Delay_Req0010：Pdelay_Req0011：Pdelay_Resp1000：Follow_Up1001：Delay_Resp1010：Pdelay_Resp_Follow_Up1011：通告1100：信令1101：管理。保留其他设置。	R/W
b4	PVER	PTPv2数据包标志	0：当前数据包不是PTPv2数据包1：当前数据包是PTPv2数据包。	R/W
b7 to b5	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b8	MACE	MAC地址不匹配标志	0：发送帧数据的源MAC地址与设定值匹配1：发送帧数据的源MAC地址与设定值不匹配。	R/W
b15 to b9	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b16	RFOF	接收FIFO溢出标志	0：未发生溢出1：发生溢出。	R/W
b17	RDE	接收描述符空标志	0：EDMAC检测到接收描述符有效位（RD0.RACT）为11：EDMAC检测到接收描述符有效位（RD0.RACT）为0。	R/W
b18	FR	帧接收标志	0：未接收到帧1：接收到帧并更新接收描述符。	R/W
b19	TFUF	发送FIFO下溢标志	0：未发生下溢1：发生下溢。	R/W
b20	TDE	发送描述符空标志	0：EDMAC检测到发送描述符有效位（TD0.TACT）为11：EDMAC检测到发送描述符有效位（TD0.TACT）为0。	R/W
b21	TC	帧传输完成标志	0：传输未完成或未请求传输1：传输描述符中指示的所有帧都已完全传输到传输FIFO。	R/W
b22	—	Reserved	该位读取为0。写入值应为0。	R/W
b23	ADE	地址错误标志	0：未检测到无效内存地址（正常操作）1：检测到无效内存地址。*1	R/W
b24	RFCOF	接收帧计数器溢出Flag	0：接收帧计数器未溢出1：接收帧计数器溢出。	R/W
b25	—	Reserved	该位读取为0。写入值应为0。	R/W

Bit	Symbol	Bit name	Description	R/W
b26	TABT	Transmit Abort Detect Flag	0: Frame transmission not aborted or transmission not requested 1: Frame transmission aborted.	R/W
b29 to b27	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b30	TWB	Write-Back Complete Flag	0: Write-back not complete or transmission not requested 1: Write-back to the transmit descriptor completed.	R/W
b31	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Note 1. When an address error is detected, the EDMAC halts the process. To resume operation, set the EDMR.SWR bit to 1 (resetting the EDMAC and ETHERC), and then reconfigure the EDMAC and ETHERC.

The PTPEDMAC.EESR register indicates the PTPEDMAC communication status. Each flag in the EESR register can be output as an interrupt request signal (ETHER_PINT) from the PTPEDMAC. Writing 1 clears the flags to 0. Writing 0 does not affect the flag values. All of the interrupt sources, except for the TYPE[3:0] flag, are enabled by setting the associated bits in the PTPEDMAC.EESIPR register.

TYPE[3:0] flags (PTP v2 Message Type Flag)

The TYPE[3:0] flags indicate the type of received PTP message.

PVER flag (PTP v2 Packet Flag)

The PVER flag indicates whether the received packet is a PTP v2 packet.

MACE flag (MAC Address Mismatch Flag)

The MACE flag indicates that the source MAC address is different from the set value.

RFOF flag (Receive FIFO Overflow Flag)

The RFOF flag indicates that the receive FIFO overflowed during frame reception.

RDE flag (Receive Descriptor Empty Flag)

The RDE flag indicates that the read receive descriptor is invalid. When this flag sets to 1, set the RD0.RACT bit in the receive descriptor to 1 and set the EDRRR.RR bit to 1 to resume reception.

FR flag (Frame Receive Flag)

The FR flag indicates that a frame was received and the receive descriptor was updated. The FR flag sets to 1 every time a frame is received.

TFUF flag (Transmit FIFO Underflow Flag)

The TFUF flag indicates that no data remains in the transmit FIFO during frame transmission. Incomplete data is sent to the line.

TDE flag (Transmit Descriptor Empty Flag)

The TDE flag indicates that the TD0.TACT bit of the transmit descriptor is 0 while the previous transmit descriptor indicates that the frame is not complete (TD0.TFP[1:0] bits are 10b or 00b) in multi-buffer frame transmission. As a result, an incomplete frame might be sent.

When this flag sets to 1, perform a software reset and then set the EDTRR.TR bit to 1 to resume transmission. Transmission starts from the address stored in the TDLAR register.

TC flag (Frame Transfer Complete Flag)

The TC flag indicates that all the data specified in the transmit descriptor was transmitted from the ETHERC. This flag sets to 1 when one frame is transmitted in single-buffer frame transmission or when the last data of a frame is transmitted in multi-buffer frame transmission and the TD0.TACT bit in the next transmit descriptor is 0. After frame transmission is complete, the PTPEDMAC writes the transfer status back to the descriptor.

ADE flag (Address Error Flag)

The ADE flag indicates that the memory address that the PTPEDMAC tried to use for transfer is invalid.

Bit	Symbol	位名称	Description	R/W
b26	TABT	发送中止检测标志	0：未中止帧传输或未请求传输1：中止帧传输。	R/W
b29 to b27	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b30	TWB	回写完成标志	0：未完成回写或未请求传输1：已完成对传输描述符的回写。	R/W
b31	—	Reserved	该位读取为0。写入值应为0。	R/W

Note 1. 当检测到地址错误时，EDMAC会停止该过程。要恢复操作，请将EDMR.SWR位设置为1（重置EDMAC和ETHERC），然后重新配置EDMAC和ETHERC。

PTPEDMAC.EESR寄存器指示PTPEDMAC通信状态。EESR寄存器中的每个标志都可以作为来自PTPEDMAC的中断请求信号(ETHER_PINT)输出。写入1会将标志清除为0。写入0不会影响标志值。除TYPE[3:0]标志外，所有中断源都通过设置PTPEDMAC.EESIPR寄存器中的相关位来启用。

TYPE[3:0]标志（PTPv2消息类型标志）

TYPE[3:0]标志指示接收到的PTP消息的类型。

PVER标志（PTPv2数据包标志）

PVER标志指示接收到的数据包是否是PTPv2数据包。

MACE标志（MAC地址不匹配标志）

MACE标志表示源MAC地址与设置值不同。

RFOF标志（接收FIFO溢出标志）

RFOF标志表示接收FIFO在帧接收期间溢出。

RDE标志（接收描述符空标志）

RDE标志指示读取的接收描述符无效。当该标志设置为1时，将接收描述符中的RD0.RACT位设置为1，并将EDRRR.RR位设置为1以恢复接收。

FR标志（帧接收标志）

FR标志表示接收到一个帧并且接收描述符已更新。每次接收到一帧时，FR标志设置为1。

TFUF标志（发送FIFO下溢标志）

TFUF标志表示在帧传输期间没有数据保留在传输FIFO中。不完整的数据被发送到线路。

TDE标志（传输描述符空标志）

TDE标志表示发送描述符的TD0.TACT位为0，而前一个发送描述符表示在多缓冲区帧传输中该帧未完成（TD0.TFP[1:0]位为10b或00b）。因此，可能会发送不完整的帧。

当该标志设置为1时，执行软件复位，然后将EDTRR.TR位设置为1以恢复传输。
传输从存储在TDLAR寄存器中的地址开始。

TC标志（帧传输完成标志）

TC标志表示发送描述符中指定的所有数据都是从ETHERC发送的。当在单缓冲帧传输中传输一帧或在多缓冲帧传输中传输一帧的最后一个数据并且下一个传输描述符中的TD0.TACT位为0时，此标志设置为1。完成后，PTPEDMAC将传输状态写回描述符。

ADE标志（地址错误标志）

ADE标志指示PTPEDMAC尝试用于传输的内存地址无效。

RFCOF flag (Receive Frame Counter Overflow Flag)

The RFCOF flag indicates that the next frame reception started while the number of frames stored in the receive FIFO reached the maximum number of frames (16 frames). Received frames are discarded while the RFCOF flag is 1.

TABT flag (Transmit Abort Detect Flag)

The TABT flag indicates that the ETHERC aborted frame transmission because of transmit retry over, loss of carrier, no carrier detection, or other error.

TWB flag (Write-Back Complete Flag)

The TWB flag indicates that the PTPEDMAC completed writing back to the descriptor after frame transmission. This flag sets to 1 after each frame transmission when the TRIMD.TIM bit is 0. It only sets to 1 when the TRIMD.TIS bit is 1.

RFCOF标志（接收帧计数器溢出标志）

RFCOF标志表示在接收FIFO中存储的帧数达到最大帧数（16帧）时开始下一帧接收。RFCOF标志为1时丢弃接收的帧。

TABT标志（发送中止检测标志）

TABT标志指示ETHERC由于传输重试、载波丢失、未检测到载波或其他错误而中止帧传输。

TWB标志（回写完成标志）

TWB标志表明PTPEDMAC在帧传输后完成了对描述符的写回。当TRIMD.TIM位为0时，此标志在每帧传输后设置为1。仅当TRIMD.TIS位为1时设置为1。

31.2.8 ETHERC/EDMAC Status Interrupt Enable Register (EDMAC0.EESIPR)

Address(es): EDMAC0.EESIPR 4006 4030h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	TWBIP	—	—	—	TABTIP	RABTIP	RFCOFIP	ADEIP	ECIIP	TCIP	TDEIP	TFUFIP	FRIP	RDEIP	RFOFIP
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	CNDIP	DLCIP	CDIP	TROIP	RMAFIP	—	—	RRFIP	RTLFIP	RTSFIP	PREIP	CERFIP
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	CERFIP	CRC Error Interrupt Request Enable	0: Disable CRC error interrupt requests 1: Enable CRC error interrupt requests.	R/W
b1	PREIP	PHY-LSI Receive Error Interrupt Request Enable	0: Disable PHY-LSI receive error interrupt requests 1: Enable PHY-LSI receive error interrupt requests.	R/W
b2	RTSFIP	Frame-Too-Short Error Interrupt Request Enable	0: Disable frame-too-short error interrupt requests 1: Enable frame-too-short error interrupt requests.	R/W
b3	RTLFIP	Frame-Too-Long Error Interrupt Request Enable	0: Disable frame-too-long error interrupt requests 1: Enable frame-too-long error interrupt requests.	R/W
b4	RRFIP	Alignment Error Interrupt Request Enable	0: Disable alignment error interrupt requests 1: Enable alignment error interrupt requests.	R/W
b6, b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	RMAFIP	Multicast Address Frame Receive Interrupt Request Enable	0: Disable multicast address frame receive interrupt requests 1: Enable multicast address frame receive interrupt requests.	R/W
b8	TROIP	Transmit Retry Over Interrupt Request Enable	0: Disable transmit retry over interrupt requests 1: Enable transmit retry over interrupt requests.	R/W
b9	CDIP	Late Collision Detect Interrupt Request Enable	0: Disable late collision detected interrupt requests 1: Enable late collision detected interrupt requests.	R/W
b10	DLCIP	Loss of Carrier Detect Interrupt Request Enable	0: Disable loss of carrier detected interrupt requests 1: Enable loss of carrier detected interrupt requests.	R/W
b11	CNDIP	Carrier Not Detect Interrupt Request Enable	0: Disable carrier not detected interrupt requests 1: Enable carrier not detected interrupt requests.	R/W
b15 to b12	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b16	RFOFIP	Receive FIFO Overflow Interrupt Request Enable	0: Disable overflow interrupt requests 1: Enable overflow interrupt requests.	R/W
b17	RDEIP	Receive Descriptor Empty Interrupt Request Enable	0: Disable receive descriptor empty interrupt requests 1: Enable receive descriptor empty interrupt requests.	R/W
b18	FRIP	Frame Receive Interrupt Request Enable	0: Disable frame reception interrupt requests 1: Enable frame reception interrupt requests.	R/W
b19	TFUFIP	Transmit FIFO Underflow Interrupt Request Enable	0: Disable underflow interrupt requests 1: Enable underflow interrupt requests.	R/W
b20	TDEIP	Transmit Descriptor Empty Interrupt Request Enable	0: Disable transmit descriptor empty interrupt requests 1: Enable transmit descriptor empty interrupt requests.	R/W
b21	TCIP	Frame Transfer Complete Interrupt Request Enable	0: Disable frame transmission complete interrupt requests 1: Enable frame transmission complete interrupt requests.	R/W
b22	ECIIP	ETHERC Status Register Source Interrupt Request Enable	0: Disable ETHERC status interrupt requests 1: Enable ETHERC status interrupt requests.	R/W

31.2.8 ETHERCEDMAC状态中断使能寄存器(EDMAC0.EESIPR)

Address(es): EDMAC0.EESIPR 4006 4030h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	TWBIP	—	—	—	TABTIP	RABTIP	RFCOFIP	ADEIP	ECIIP	TCIP	TDEIP	TFUFIP	FRIP	RDEIP	RFOFIP
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	CNDIP	DLCIP	CDIP	TROIP	RMAFIP	—	—	RRFIP	RTLFIP	RTSFIP	PREIP	CERFIP
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	CERFIP	CRC错误中断请求使能	0：禁用CRC错误中断请求1：启用CRC错误中断请求。	R/W
b1	PREIP	PHY-LSI接收错误中断请求Enable	0：禁止PHY-LSI接收错误中断请求1：使能PHY-LSI接收错误中断请求。	R/W
b2	RTSFIP	帧太短错误中断请求Enable	0：禁用帧太短错误中断请求1：启用帧太短错误中断请求。	R/W
b3	RTLFIP	帧过长错误中断请求Enable	0：禁用帧过长错误中断请求1：启用帧过长错误中断请求。	R/W
b4	RRFIP	对齐错误中断请求启用	0：禁用对齐错误中断请求1：启用对齐错误中断请求。	R/W
b6, b5	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b7	RMAFIP	组播地址帧接收中断请求使能	0：禁止组播地址帧接收中断请求1：使能组播地址帧接收中断请求。	R/W
b8	TROIP	通过中断请求发送重试Enable	0：禁止发送重试中断请求1：启用发送重试中断请求。	R/W
b9	CDIP	后期冲突检测中断请求Enable	0：禁用后期冲突检测中断请求1：启用后期冲突检测中断请求。	R/W
b10	DLCIP	载波检测中断请求丢失Enable	0：禁用检测到载波丢失中断请求1：启用检测到载波丢失中断请求。	R/W
b11	CNDIP	运营商未检测到中断请求Enable	0：禁用未检测到载波中断请求1：启用未检测到载波中断请求。	R/W
b15 to b12	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b16	RFOFIP	接收FIFO溢出中断请求Enable	0：禁止溢出中断请求1：使能溢出中断请求。	R/W
b17	RDEIP	接收描述符空中断请求启用	0：禁用接收描述符空中断请求1：启用接收描述符空中断请求。	R/W
b18	FRIP	帧接收中断请求使能	0：禁止帧接收中断请求1：允许帧接收中断请求。	R/W
b19	TFUFIP	发送FIFO下溢中断请求启用	0：禁止下溢中断请求1：允许下溢中断请求。	R/W
b20	TDEIP	发送描述符空中断请求启用	0：禁止发送描述符空中断请求1：使能发送描述符空中断请求。	R/W
b21	TCIP	帧传输完成中断请求启用	0：禁止帧发送完成中断请求1：允许帧发送完成中断请求。	R/W
b22	ECIIP	ETHERC状态寄存器源中断请求启用	0：禁止ETHERC状态中断请求1：使能ETHERC状态中断请求。	R/W

Bit	Symbol	Bit name	Description	R/W
b23	ADEIP	Address Error Interrupt Request Enable	0: Disable address error interrupt requests 1: Enable address error interrupt requests.	R/W
b24	RFCOFIP	Receive Frame Counter Overflow Interrupt Request Enable	0: Disable receive frame counter overflow interrupt requests 1: Enable receive frame counter overflow interrupt requests.	R/W
b25	RABTIP	Receive Abort Detect Interrupt Request Enable	0: Disable receive abort detected interrupt requests 1: Enable receive abort detected interrupt requests.	R/W
b26	TABTIP	Transmit Abort Detect Interrupt Request Enable	0: Disable transmit abort detected interrupt requests 1: Enable transmit abort detected interrupt requests.	R/W
b29 to b27	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b30	TWBIP	Write-Back Complete Interrupt Request Enable	0: Disable write-back complete interrupt requests 1: Enable write-back complete interrupt requests.	R/W
b31	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

The EDMAC0.EESIPR register enables interrupt requests associated with bits in the EDMAC0.EESR register. When a bit in this register is 1, the associated interrupt request is enabled.

Bit	Symbol	位名称	Description	R/W
b23	ADEIP	地址错误中断请求使能	0：禁止地址错误中断请求1：允许地址错误中断请求。	R/W
b24	RFCOFIP	接收帧计数器溢出中断请求使能	0：禁止接收帧计数器溢出中断请求1：使能接收帧计数器溢出中断请求。	R/W
b25	RABTIP	接收中止检测中断请求Enable	0：禁用接收中止检测到中断请求1：启用接收中止检测到中断请求。	R/W
b26	TABTIP	发送中止检测中断请求Enable	0：禁止发送中止检测到中断请求1：使能发送中止检测到中断请求。	R/W
b29 to b27	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b30	TWBIP	回写完成中断请求Enable	0：禁止回写完成中断请求1：使能回写完成中断请求。	R/W
b31	—	Reserved	该位读取为0。写入值应为0。	R/W

EDMAC0.EESIPR寄存器启用与EDMAC0.EESR寄存器中的位相关的中断请求。当该寄存器中的某个位为1时，相关的中断请求被使能。

31.2.9 PTP/EDMAC Status Interrupt Enable Register (PTPEDMAC.EESIPR)

Address(es): PTPEDMAC.EESIPR 4006 4430h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	TWBIP	—	—	—	TABTIP	—	RFCOFIP	ADEIP	—	TCIP	TDEIP	TFUFIP	FRIP	RDEIP	RFOFIP
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	MACEIP	—	—	—	PVERIP	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	—	Reserved	The read value is 0. The write value should be 0.	R/W
b4	PVERIP	PTP v2 Packet Receive Interrupt Request Enable	0: Disable PTP v2 packet receive interrupt requests 1: Enable PTP v2 packet receive interrupt requests.	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	MACEIP	MAC Address Mismatch Interrupt Request Enable	0: Disable interrupt requests generated when the source MAC address of transmit frame data does not match the set value 1: Enable interrupt requests generated when the source MAC address of transmit frame data does not match the set value.	R/W
b15 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b16	RFOFIP	Receive FIFO Overflow Interrupt Request Enable	0: Disable overflow interrupt requests 1: Enable overflow interrupt requests.	R/W
b17	RDEIP	Receive Descriptor Empty Interrupt Request Enable	0: Disable receive descriptor empty interrupt requests 1: Enable receive descriptor empty interrupt requests.	R/W
b18	FRIP	Frame Receive Interrupt Request Enable	0: Disable frame receive interrupt requests 1: Enable frame receive interrupt requests.	R/W
b19	TFUFIP	Transmit FIFO Underflow Interrupt Request Enable	0: Disable underflow interrupt requests 1: Enable underflow interrupt requests.	R/W
b20	TDEIP	Transmit Descriptor Empty Interrupt Request Enable	0: Disable transmit descriptor empty interrupt requests 1: Enable transmit descriptor empty interrupt requests.	R/W
b21	TCIP	Frame Transfer Complete Interrupt Request Enable	0: Disable frame transmission complete interrupt requests 1: Enable frame transmission complete interrupt requests.	R/W
b22	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b23	ADEIP	Address Error Interrupt Request Enable	0: Disable address error interrupt requests 1: Enable address error interrupt requests.	R/W
b24	RFCOFIP	Receive Frame Counter Overflow Interrupt Request Enable	0: Disable receive frame counter overflow interrupt requests 1: Enable receive frame counter overflow interrupt requests.	R/W
b25	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b26	TABTIP	Transmit Abort Detect Interrupt Request Enable	0: Disable transmit abort detect interrupt requests 1: Enable transmit abort detect interrupt requests.	R/W
b29 to b27	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b30	TWBIP	Write-Back Complete Interrupt Request Enable	0: Disable write-back complete interrupt requests 1: Enable write-back complete interrupt requests.	R/W
b31	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

The PTPEDMAC.EESIPR register enables interrupt requests associated with bits in the PTPEDMAC.EESR register. When a bit in this register is 1, the associated interrupt request is enabled.

31.2.9 PTPEDMAC状态中断使能寄存器(PTPEDMAC.EESIPR)

Address(es): PTPEDMAC.EESIPR 4006 4430h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	TWBIP	—	—	—	TABTIP	—	RFCOFIP	ADEIP	—	TCIP	TDEIP	TFUFIP	FRIP	RDEIP	RFOFIP
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	MACEIP	—	—	—	PVERIP	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b3 to b0	—	Reserved	读取值为0。写入值应为0。	R/W
b4	PVERIP	PTPv2数据包接收中断请求启用	0：禁用PTPv2数据包接收中断请求1：启用PTPv2数据包接收中断请求。	R/W
b7 to b5	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b8	MACEIP	MAC地址不匹配中断请求启用	0：禁止发送帧数据的源MAC地址与设定值不匹配时产生的中断请求1：使能发送帧数据的源MAC地址与设定值不匹配时产生的中断请求。	R/W
b15 to b9	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b16	RFOFIP	接收FIFO溢出中断请求启用	0：禁止溢出中断请求1：使能溢出中断请求。	R/W
b17	RDEIP	接收描述符空中断请求启用	0：禁用接收描述符空中断请求1：启用接收描述符空中断请求。	R/W
b18	FRIP	帧接收中断请求Enable	0：禁止帧接收中断请求1：允许帧接收中断请求。	R/W
b19	TFUFIP	发送FIFO下溢中断请求启用	0：禁止下溢中断请求1：允许下溢中断请求。	R/W
b20	TDEIP	发送描述符空中断请求启用	0：禁止发送描述符空中断请求1：使能发送描述符空中断请求。	R/W
b21	TCIP	帧传输完成中断请求启用	0：禁止帧发送完成中断请求1：允许帧发送完成中断请求。	R/W
b22	—	Reserved	该位读取为0。写入值应为0。	R/W
b23	ADEIP	地址错误中断请求使能	0：禁止地址错误中断请求1：允许地址错误中断请求。	R/W
b24	RFCOFIP	接收帧计数器溢出中断请求使能	0：禁止接收帧计数器溢出中断请求1：使能接收帧计数器溢出中断请求。	R/W
b25	—	Reserved	该位读取为0。写入值应为0。	R/W
b26	TABTIP	发送中止检测中断请求启用	0：禁止发送中止检测中断请求1：使能发送中止检测中断请求。	R/W
b29 to b27	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b30	TWBIP	回写完成中断请求Enable	0：禁止回写完成中断请求1：使能回写完成中断请求。	R/W
b31	—	Reserved	该位读取为0。写入值应为0。	R/W

PTPEDMAC.EESIPR寄存器启用与PTPEDMAC.EESR寄存器中的位相关的中断请求。
当该寄存器中的某个位为1时，相关的中断请求被使能。

31.2.10 ETHERC/EDMAC Transmit/Receive Status Copy Enable Register (EDMAC0.TRSCER)

Address(es): EDMAC0.TRSCER 4006 4038h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	RMAFCE	—	—	RRFCE	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	RRFCE	RRF Flag Copy Enable	0: Reflect the EESR.RRF flag status in the RD0.RFE bit of the receive descriptor 1: Do not reflect the EESR.RRF flag status in the RD0.RFE bit of the receive descriptor.	R/W
b6, b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	RMAFCE	RMAF Flag Copy Enable	0: Reflect the EESR.RMAF flag status in the RD0.RFE bit of the receive descriptor 1: Do not reflect the EESR.RMAF flag status in the RD0.RFE bit of the receive descriptor.	R/W
b31 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The EDMAC0.TRSCER register selects whether the receive status indicated in the EDMAC0.EESR.RMAF and RRF flags is reflected in the RFE bit of the receive descriptor as a summary. The bits in this register are associated with bits in the EESR register that have the same number. When the RMAFCE or RRFCE bit is set to 0, the associated receive status is reflected in the RFE bit. When the RMAFCE or RRFCE bit is set to 1, the associated receive status is not reflected.

31.2.10 ETHERCEDMAC发送接收状态复制使能寄存器(EDMAC0.TRSCER)

Address(es): EDMAC0.TRSCER 4006 4038h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	RMAFCE	—	—	RRFCE	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b3 to b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b4	RRFCE	RRF标志复制启用	0：在接收描述符的RD0.RFE位中反映EESR.RRF标志状态1：在接收描述符的RD0.RFE位中不反映EESR.RRF标志状态。	R/W
b6, b5	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b7	RMAFCE	RMAF标志复制启用	0：在接收描述符的RD0.RFE位中反映EESR.RMAF标志状态1：在接收描述符的RD0.RFE位中不反映EESR.RMAF标志状态。	R/W
b31 to b8	—	Reserved	这些位被读取为0。写入值应为0。	R/W

EDMAC0.TRSCER寄存器选择是否将EDMAC0.EESR.RMAF和RRF标志中指示的接收状态作为摘要反映在接收描述符的RFE位中。该寄存器中的位与EESR寄存器中具有相同编号的位相关联。当RMAFCE或RRFCE位设置为0时，相关的接收状态反映在RFE位中。当RMAFCE或RRFCE位设置为1时，不反映相关的接收状态。

31.2.11 Missed-Frame Counter Register (RMFCR)

Address(es): EDMAC0.RMFCR 4006 4040h, PTPEDMAC.RMFCR 4006 4440h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MFC[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b15 to b0	MFC[15:0]	Missed-Frame Counter	These bits indicate the number of frames that are discarded and not transferred to the receive buffer during reception.	R/W
b31 to b16	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The RMFCR register indicates that the number of frames that could not be stored in the receive FIFO and so were discarded during reception. When the receive FIFO overflows, it stops receiving data, and the rest of frames are discarded. At the same time, the RMFCR register value is incremented. When the RMFCR register value reaches FFFFh, count-up is halted. Writing any value to the RMFCR register clears the counter value to 0.

For frames that are not completely received, after data in the receive FIFO is transferred to the receive buffer, the RACT bit in the receive descriptor 0 (RD0) clears to 0 (descriptor disabled), the RFS9 bit sets to 1 (receive FIFO overflowed), and the EDMAC0.EESR.RFOF or PTPEDMAC.EESR.RFOF flag sets to 1 (overflow detected).

31.2.11 漏帧计数器寄存器(RMFCR)

Address(es): EDMAC0.RMFCR 4006 4040h, PTPEDMAC.RMFCR 4006 4440h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MFC[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b15 to b0	MFC[15:0]	Missed-Frame Counter	这些位指示在接收期间被丢弃且未传输到接收缓冲区的帧数。	R/W
b31 to b16	—	Reserved	这些位被读取为0。写入值应为0。	R/W

RMFCR寄存器指示无法存储在接收FIFO中并因此在接收期间被丢弃的帧数。当接收FIFO溢出时，它停止接收数据，其余帧被丢弃。同时，RMFCR寄存器值递增。当RMFCR寄存器值达到FFFFh时，停止向上计数。向RMFCR寄存器写入任何值都会将计数器值清零。

对于未完全接收的帧，接收FIFO中的数据传输到接收缓冲区后，接收描述符0（RD0）中的RACT位清为0（描述符禁用），RFS9位设置为1（接收FIFO溢出），并且EDMAC0.EESR.RFOF或PTPEDMAC.EESR.RFOF标志设置为1（检测到溢出）。

31.2.12 Transmit FIFO Threshold Register (TFTR)

Address(es): EDMAC0.TFTR 4006 4048h, PTPEDMAC.TFTR 4006 4448h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	TFT[10:0]										
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b10 to b0	TFT[10:0]	Transmit FIFO Threshold	000h: Store-and-forward mode 001h to 00Ch: Setting prohibited 00Dh to 200h: The threshold is the set value multiplied by 4. Example: 00Dh: 52 bytes 040h: 256 bytes 100h: 1024 bytes 200h: 2048 bytes 201h to 7FFh: Setting prohibited.	R/W
b31 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: When starting transmission before one frame data is completely written, take care to prevent an underflow. To prevent a transmit underflow, Renesas recommends using the initial value (store-and-forward mode).

The TFTR register specifies the transmit FIFO threshold at which the first transmission starts. The actual threshold is the set value multiplied by 4.

The ETHERC starts transmission when the amount of data in the transmit FIFO exceeds the number of bytes set in this register, when the transmit FIFO is full, or when one frame of data is completely written. Set the TFTR register while the EDTRR.TR bit is 0.

31.2.12 发送FIFO阈值寄存器(TFTR)

Address(es): EDMAC0.TFTR 4006 4048h, PTPEDMAC.TFTR 4006 4448h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	TFT[10:0]										
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b10 to b0	TFT[10:0]	发送FIFO阈值	000h：存储转发模式001h至00Ch：禁止设置00Dh至200h：阈值是设置值乘以4示例：00Dh：52字节040h：256字节100h：1024字节200h：2048字节201h至7FFh：禁止设置。	R/W
b31 to b11	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note: 在完全写入一帧数据之前开始传输时，请注意防止下溢。为防止发送下溢，瑞萨推荐使用初始值（存储转发模式）。

TFTR寄存器指定第一次发送开始时的发送FIFO阈值。实际阈值是设定值乘以4。

当发送FIFO中的数据量超过此寄存器中设置的字节数、发送FIFO已满或一帧数据被完全写入时，ETHERC开始发送。当EDTRR.TR位为0时设置TFTR寄存器。

31.2.13 FIFO Depth Register (FDR)

Address(es): EDMAC0.FDR 4006 4050h, PTPEDMAC.FDR 4006 4450h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	TFD[4:0]					—	—	—	RFD[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b4 to b0	RFD[4:0]	Receive FIFO Depth	b4 b0 01111: 4096 bytes. Other settings are prohibited.	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b12 to b8	TFD[4:0]	Transmit FIFO Depth	b12 b8 00111: 2048 bytes. Other settings are prohibited.	R/W
b31 to b13	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The FDR register specifies the transmit and receive FIFO depths. Set this register to 0000_070Fh before starting transmission and reception.

31.2.14 Receive Method Control Register (RMCR)

Address(es): EDMAC0.RMCR 4006 4058h, PTPEDMAC.RMCR 4006 4458h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RNR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	RNR	Receive Request Reset	0: EDRRR.RR bit (receive request bit) is cleared to 0 when one frame is received 1: EDRRR.RR bit (receive request bit) is not cleared to 0 when one frame is received.	R/W
b31 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The RMCR register specifies how to control the EDRRR.RR bit when receiving a frame. When the RNR bit is 0, the EDRRR.RR bit clears to 0 when one frame is received, so it must be set to 1 by software to receive the subsequent frame. When the RNR bit is 1, the EDRRR.RR bit does not clear to 0 when one frame is received, and the EDMAC reads the next receive descriptor and continues frame reception. Renesas recommends setting the RNR bit to 1 when receiving data continuously. Set the RMCR register while the EDRRR.RR bit is 0.

31.2.13 FIFO深度寄存器(FDR)

Address(es): EDMAC0.FDR 4006 4050h, PTPEDMAC.FDR 4006 4450h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	TFD[4:0]					—	—	—	RFD[4:0]				
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b4 to b0	RFD[4:0]	接收FIFO深度	b4b001111：4096字节。禁止其他设置。	R/W
b7 to b5	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b12 to b8	TFD[4:0]	发送FIFO深度	b12b800111：2048字节。禁止其他设置。	R/W
b31 to b13	—	Reserved	这些位被读取为0。写入值应为0。	R/W

FDR寄存器指定发送和接收FIFO深度。在开始发送和接收之前将此寄存器设置为0000_070Fh。

31.2.14 接收方法控制寄存器(RMCR)

Address(es): EDMAC0.RMCR 4006 4058h, PTPEDMAC.RMCR 4006 4458h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RNR
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	RNR	接收请求重置	0：当接收一帧时，EDRRR.RR位（接收请求位）清零1：当接收一帧时，EDRRR.RR位（接收请求位）不清零。	R/W
b31 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

RMCR寄存器指定接收帧时如何控制EDRRR.RR位。当RNR位为0时，
EDRRR.RR位在接收到一帧后清为0，因此必须通过软件设置为1才能接收后续帧。
当RNR位为1时，接收到一帧时EDRRR.RR位不清为0，EDMAC读取下一个接收描述符并继续帧接收。Renesas建议在连续接收数据时将RNR位设置为1。当EDRRR.RR位为0时设置RMCR寄存器。

31.2.15 Transmit FIFO Underflow Counter (TFUCR)

Address(es): EDMAC0.TFUCR 4006 4064h, PTPEDMAC.TFUCR 4006 4464h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	UNDER[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b15 to b0	UNDER[15:0]	Transmit FIFO Underflow Count	These bits indicate how many times the transmit FIFO underflows. The counter stops when the counter value reaches FFFFh.	R/W
b31 to b16	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The TFUCR register indicates how many times the transmit FIFO underflows. Writing any value to the TFUCR register clears the counter value to 0.

31.2.16 Receive FIFO Overflow Counter (RFOCR)

Address(es): EDMAC0.RFOCR 4006 4068h, PTPEDMAC.RFOCR 4006 4468h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	OVER[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b15 to b0	OVER[15:0]	Receive FIFO Overflow Count	These bits indicate how many times the receive FIFO overflows. The counter stops when the counter value reaches FFFFh.	R/W
b31 to b16	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The RFOCR register indicates how many times the receive FIFO overflows. Writing any value to the RFOCR register clears the counter value to 0.

31.2.15 发送FIFO下溢计数器(TFUCR)

Address(es): EDMAC0.TFUCR 4006 4064h, PTPEDMAC.TFUCR 4006 4464h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	UNDER[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b15 to b0	UNDER[15:0]	发送FIFO下溢计数	这些位指示发送FIFO下溢的次数。当计数器值达到FFFFh时，计数器停止。	R/W
b31 to b16	—	Reserved	这些位被读取为0。写入值应为0。	R/W

TFUCR寄存器指示发送FIFO下溢的次数。向TFUCR寄存器写入任何值都会将计数器值清零。

31.2.16 接收FIFO溢出计数器(RFOCR)

Address(es): EDMAC0.RFOCR 4006 4068h, PTPEDMAC.RFOCR 4006 4468h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	OVER[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b15 to b0	OVER[15:0]	接收FIFO溢出计数	这些位指示接收FIFO溢出的次数。 当计数器值达到FFFFh时，计数器停止。	R/W
b31 to b16	—	Reserved	这些位被读取为0。写入值应为0。	R/W

RFOCR寄存器指示接收FIFO溢出的次数。向RFOCR寄存器写入任何值都会将计数器值清零。

31.2.17 Independent Output Signal Setting Register (IOSR)

Address(es): EDMAC0.IOSR 4006 406Ch, PTPEDMAC.IOSR 4006 446Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ELB
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	ELB	External Loopback Mode	0: Output low on the ET0_EXOUT pin 1: Output high on the ET0_EXOUT pin.	R/W
b31 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The IOSR register selects the output level of the ETHERC external output pin (ET0_EXOUT) in external loopback mode. The ELB bit value is output on the ET0_EXOUT pin, which can be used to set loopback mode for the PHY-LSI. To use the loopback function of the PHY-LSI through this register, you must connect the PHY-LSI to the ET0_EXOUT pin.

31.2.17 独立输出信号设置寄存器（IOSR）

Address(es): EDMAC0.IOSR 4006 406Ch, PTPEDMAC.IOSR 4006 446Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ELB
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	ELB	外部环回模式	0：ET0_EXOUT引脚输出低电平1：ET0_EXOUT引脚输出高电平。	R/W
b31 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

IOSR寄存器选择外部环回模式下ETHERC外部输出引脚(ET0_EXOUT)的输出电平。ELB位值在ET0_EXOUT引脚上输出，可用于设置PHY-LSI的环回模式。要通过该寄存器使用PHY-LSI的环回功能，您必须将PHY-LSI连接到ET0_EXOUT引脚。

31.2.18 Flow Control Start FIFO Threshold Setting Register (FCFTR)

Address(es): EDMAC0.FCFTR 4006 4070h, PTPEDMAC.FCFTR 4006 4470h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	RFFO[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	RFDO[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bit	Symbol	Bit name	Description	R/W
b2 to b0	RFDO[2:0]	Receive FIFO Data PAUSE Output Threshold	b2 b0 0 0 0:When 224 (256 to 32) bytes of data is stored in the receive FIFO 0 0 1:When 480 (512 to 32) bytes of data is stored in the receive FIFO : 1 1 0:When 1760 (1792 to 32) bytes of data is stored in the receive FIFO 1 1 1:When 2016 (2048 to 32) bytes of data is stored in the receive FIFO.	R/W
b15 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b18 to b16	RFFO[2:0]	Receive FIFO Frame PAUSE Output Threshold	b18 b16 0 0 0:When 2 receive frames are stored in the receive FIFO 0 0 1:When 4 receive frames are stored in the receive FIFO 0 1 0:When 6 receive frames are stored in the receive FIFO : 1 1 0:When 14 receive frames are stored in the receive FIFO 1 1 1:When 16 receive frames are stored in the receive FIFO.	R/W
b31 to b19	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The FCFTR register specifies the ETHERC flow control. Set the threshold to automatically transmit a PAUSE frame. The threshold can be set using the data size (RFDO[2:0] bits) and the number of frames (RFFO[2:0] bits) stored in the receive FIFO. Flow control starts when the stored data size or the number of stored frames reaches its threshold.

31.2.18 流控制启动FIFO阈值设置寄存器(FCFTR)

Address(es): EDMAC0.FCFTR 4006 4070h, PTPEDMAC.FCFTR 4006 4470h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	RFFO[2:0]		
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	RFDO[2:0]		
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bit	Symbol	位名称	Description	R/W
b2 to b0	RFDO[2:0]	接收FIFO数据暂停输出Threshold	b2b0000：接收FIFO中存储224（256到32）字节数据时001：接收FIFO中存储480（512到32）字节数据时：110：当1760（1792到32)字节的数据存储在接收FIFO111：当2016(2048到32)字节的数据存储在接收FIFO中时。	R/W
b15 to b3	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b18 to b16	RFFO[2:0]	接收FIFO帧暂停输出Threshold	b18b16000：当接收FIFO中存储2个接收帧时001：当接收FIFO中存储4个接收帧时010：当接收FIFO中存储6个接收帧时：110：当接收FIFO中存储14个接收帧111：当接收FIFO中存储16个接收帧时。	R/W
b31 to b19	—	Reserved	这些位被读取为0。写入值应为0。	R/W

FCFTR寄存器指定ETHERC流控制。设置阈值以自动发送PAUSE帧。可以使用存储在接收FIFO中的数据大小（RFDO[2:0]位）和帧数（RFFO[2:0]位）来设置阈值。当存储的数据大小或存储的帧数达到其阈值时，流量控制开始。

31.2.19 Receive Data Padding Insert Register (RPADIR)

Address(es): EDMAC0.RPADIR 4006 4078h, PTPEDMAC.RPADIR 4006 4478h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PADS[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	PADR[5:0]					
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b5 to b0	PADR[5:0]	Padding Slot	00h: Insert padding at the head of received data 01h: Insert padding between the 1st and 2nd bytes of received data : 3Eh: Insert padding between the 62nd and 63rd bytes of received data 3Fh: Insert padding between the 63rd and 64th bytes of received data.	R/W
b15 to b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b17, b16	PADS[1:0]	Padding Size	b17b16 0 0: Do not insert padding 0 1: Insert 1 byte 1 0: Insert 2 bytes 1 1: Insert 3 bytes.	R/W
b31 to b18	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The RPADIR register specifies insertion of padding for received data. The padding value is 00h. Set the EDMR.SWR bit to 1 to reset before rewriting the PRADIR register.

31.2.19 接收数据填充插入寄存器(RPADIR)

Address(es): EDMAC0.RPADIR 4006 4078h, PTPEDMAC.RPADIR 4006 4478h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PADS[1:0]	
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	PADR[5:0]					
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b5 to b0	PADR[5:0]	填充槽	00h：在接收数据的开头插入填充01h：在接收数据的第1和第2字节之间插入填充：3Eh：在接收数据的第62和第63字节之间插入填充3Fh：在接收数据的第63和第64字节之间插入填充.	R/W
b15 to b6	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b17, b16	PADS[1:0]	填充尺寸	b17b1600：不插入填充01：插入1个字节10：插入2个字节11：插入3个字节。	R/W
b31 to b18	—	Reserved	这些位被读取为0。写入值应为0。	R/W

RPADIR寄存器指定为接收到的数据插入填充。填充值是00h。在重写PRADIR寄存器之前，将EDMR.SWR位设置为1以复位。

31.2.20 Transmit Interrupt Setting Register (TRIMD)

Address(es): EDMAC0.TRIMD 4006 407Ch, PTPEDMAC.TRIMD 4006 447Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	TIM	—	—	—	TIS
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	TIS	Transmit Interrupt Enable	0: Disable transmit interrupts 1: Enable transmit Interrupts. Set the EESR.TWB flag to 1 in the mode selected in the TIM bit to report an interrupt.	R/W
b3 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	TIM	Transmit Interrupt Mode	0: Select transmission complete interrupt mode, where an interrupt occurs when a frame is transmitted 1: Select write-back complete interrupt mode, where an interrupt occurs when write-back to the transmit descriptor is complete while the TWBI bit is 1.	R/W
b31 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The TRIMD register specifies the transmit interrupt mode and enables or disables transmit interrupts. When the condition selected in this register is satisfied, the EESR.TWB flag sets to 1, and an interrupt request is output when the EESIPR.TWBIP bit is 1.

31.2.21 Receive Buffer Write Address Register (RBWAR)

Address(es): EDMAC0.RBWAR 4006 40C8h, PTPEDMAC.RBWAR 4006 44C8h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The RBWAR register indicates the last address that the EDMAC wrote data to when writing to the receive buffer. Check the contents of this register to identify which address in the receive buffer the EDMAC is writing data to. The address that the EDMAC is outputting to the receive buffer might not match the read value of the RBWAR register during data reception. The RBWAR register is read-only. Do not write to this register.

31.2.20 发送中断设置寄存器(TRIMD)

Address(es): EDMAC0.TRIMD 4006 407Ch, PTPEDMAC.TRIMD 4006 447Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	TIM	—	—	—	TIS
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	TIS	发送中断使能	0：禁用发送中断1：启用发送中断。在TIM位选择的模式下将EESR.TWB标志设置为1以报告中断。	R/W
b3 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b4	TIM	发送中断模式	0：选择发送完成中断模式，发送一帧时发生中断1：选择回写完成中断模式，当TWBI位为1时，发送描述符的写回完成时发生中断。	R/W
b31 to b5	—	Reserved	这些位被读取为0。写入值应为0。	R/W

TRIMD寄存器指定发送中断模式并启用或禁用发送中断。当满足此寄存器中选择的条件时，EESR.TWB标志设置为1，并且当ESIPR.TWBIP位为1时输出中断请求。

31.2.21 接收缓冲区写地址寄存器(RBWAR)

Address(es): EDMAC0.RBWAR 4006 40C8h, PTPEDMAC.RBWAR 4006 44C8h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RBWAR寄存器指示EDMAC在写入接收缓冲区时写入数据的最后一个地址。检查该寄存器的内容以确定EDMAC正在向接收缓冲区中的哪个地址写入数据。在数据接收期间，EDMAC输出到接收缓冲区的地址可能与RBWAR寄存器的读取值不匹配。RBWAR寄存器是只读的。不要写入该寄存器。

31.2.22 Receive Descriptor Fetch Address Register (RDFAR)

Address(es): EDMAC0.RDFAR 4006 40CCh, PTPEDMAC.RDFAR 4006 44CCh

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The RDFAR register indicates the start address of the last fetched receive descriptor when the EDMAC is fetching descriptor information from the receive descriptor. Check the contents of this register to identify which receive descriptor information the EDMAC is using for active processing. The address of the receive descriptor that the EDMAC is fetching might not match the read value of the RDFAR register during data reception. The RDFAR register is read-only. Do not write to this register.

31.2.23 Transmit Buffer Read Address Register (TBRAR)

Address(es): EDMAC0.TBRAR 4006 40D4h, PTPEDMAC.TBRAR 4006 44D4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The TBRAR register indicates the last address that the EDMAC read data from when reading data from the transmit buffer. Check the contents of this register to identify which address in the transmit buffer the EDMAC is reading from. The address that the EDMAC is outputting to the transmit buffer might not match the read value of the TBRAR register. The TBRAR register is read-only. Do not write to this register.

31.2.22 接收描述符获取地址寄存器(RDFAR)

Address(es): EDMAC0.RDFAR 4006 40CCh, PTPEDMAC.RDFAR 4006 44CCh

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

当EDMAC从接收描述符中获取描述符信息时，RDFAR寄存器指示最后获取的接收描述符的起始地址。检查该寄存器的内容以确定EDMAC正在使用哪些接收描述符信息进行主动处理。EDMAC正在获取的接收描述符的地址可能与数据接收期间RDFAR寄存器的读取值不匹配。RDFAR寄存器是只读的。不要写入该寄存器。

31.2.23 发送缓冲区读取地址寄存器(TBRAR)

Address(es): EDMAC0.TBRAR 4006 40D4h, PTPEDMAC.TBRAR 4006 44D4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

TBRAR寄存器指示EDMAC从发送缓冲区读取数据时读取数据的最后地址。检查该寄存器的内容以确定EDMAC正在从发送缓冲区中的哪个地址读取。EDMAC输出到发送缓冲区的地址可能与TBRAR寄存器的读取值不匹配。

TBRAR寄存器是只读的。不要写入该寄存器。

31.2.24 Transmit Descriptor Fetch Address Register (TDFAR)

Address(es): EDMAC0.TDFAR 4006 40D8h, PTPEDMAC.TDFAR 4006 44D8h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The TDFAR register indicates the start address of the last fetched transmit descriptor when the EDMAC is fetching descriptor information from the transmit descriptor. Check the contents of this register to identify which transmit descriptor information the EDMAC is using for active processing. The address of transmit descriptor that the EDMAC fetches might not match the read value of the TDFAR register. The TDFAR is read only. Do not write to this register.

31.2.24 发送描述符获取地址寄存器(TDFAR)

Address(es): EDMAC0.TDFAR 4006 40D8h, PTPEDMAC.TDFAR 4006 44D8h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

当EDMAC从发送描述符中获取描述符信息时，TDFAR寄存器指示最后获取的发送描述符的起始地址。检查该寄存器的内容以确定EDMAC正在使用哪些传输描述符信息进行主动处理。EDMAC获取的发送描述符地址可能与TDFAR寄存器的读取值不匹配。TDFAR是只读的。不要写入该寄存器。

31.3 Operation

The EDMAC transfers data according to the information written in the descriptor. Two descriptors are provided: transmit and receive. A descriptor includes the buffer size, address, and transmit or receive status. The EDMAC transmits or receives data continuously by using sequentially arranged descriptors.

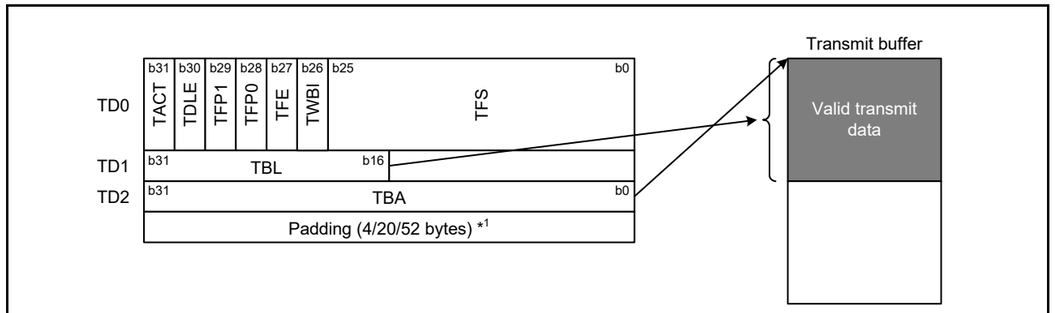
31.3.1 Descriptor Lists and Data Buffers

To transfer data using the EDMAC, create the transmit and receive descriptor lists in memory, set the start address of the transmit descriptor list in the TDLAR register, and set the start address of the receive descriptor list in the RDLAR register. Also, transmit and receive buffers associated with each descriptor are required.

Align the descriptor list on the appropriate address boundary according to the descriptor length set in the EDMR.DL[1:0] bits. The transmit buffer can be aligned on a word boundary, halfword boundary, or byte boundary. When the valid transmit buffer size is 16 bytes or less, align it on a 32-byte boundary. Align the receive buffer on a 32-byte boundary. Set different addresses for the transmit and receive descriptors and buffers for EDMAC0 and the PTPEDMAC.

31.3.1.1 Transmit descriptor

Figure 31.3 shows the relationship between a transmit descriptor and transmit buffer. A transmit descriptor consists of TD0 to TD2. The transmit frame and transmit buffer configuration can be specified as one buffer per frame (single-buffer frame transmission) or multiple buffers per frame (multi-buffer frame transmission) by setting the transmit descriptor.



Note 1. The padding size is determined by the descriptor length (16/32/64 bytes).

Figure 31.3 Relationship between transmit descriptor and transmit buffer

31.3 Operation

EDMAC根据描述符中写入的信息传输数据。提供了两个描述符：发送和接收。描述符包括缓冲区大小、地址和发送或接收状态。EDMAC通过使用顺序排列的描述符连续发送或接收数据。

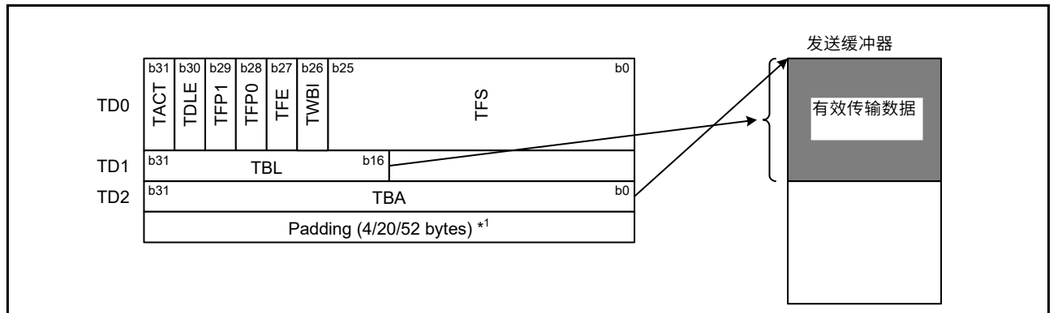
31.3.1 描述符列表和数据缓冲区

要使用EDMAC传输数据，在内存中创建发送和接收描述符列表，在TDLAR寄存器中设置发送描述符列表的起始地址，在RDLAR寄存器中设置接收描述符列表的起始地址。此外，还需要与每个描述符关联的发送和接收缓冲区。

根据在EDMR.DL[1:0]位中设置的描述符长度将描述符列表对齐在适当的地址边界上。发送缓冲区可以在字边界、半字边界或字节边界上对齐。当有效发送缓冲区大小为16字节或更少时，将其对齐在32字节边界上。在32字节边界上对齐接收缓冲区。为EDMAC0和PTPEDMAC的发送和接收描述符和缓冲区设置不同的地址。

31.3.1.1 传输描述符

图31.3显示了发送描述符和发送缓冲区之间的关系。发送描述符由TD0到TD2组成。通过设置传输描述符，可以将传输帧和传输缓冲区配置指定为每帧一个缓冲区（单缓冲区帧传输）或每帧多个缓冲区（多缓冲区帧传输）。



Note 1. 填充大小由描述符长度（163264字节）确定。

Figure 31.3 发送描述符和发送缓冲区的关系

(1) Transmit descriptor 0 (TD0)

Bit	Symbol	Bit name	Description	R/W
b25 to b0	TFS	Transmit Frame Status	Set all bits to 0 when creating a descriptor. After write-back, the bits indicate the following: • For EDMAC0: TFS25 to TFS9: Reserved TFS8: Transmit abort was detected (value is equivalent to the EESR.TABT flag) TFS7 to TFS4: Reserved TFS3: No carrier was detected (value is equivalent to the EESR.CND flag) TFS2: Loss of carrier was detected (value is equivalent to the EESR.DLC flag) TFS1: Late collision during transmission was detected (value is equivalent to the EESR.CD flag) TFS0: Transmit retry over (value is equivalent to the EESR.TRO flag). When a bit sets to 1, it indicates that the associated error occurred during frame transmission. When any of the TFS bits sets to 1, the TFE bit also sets to 1. When any of bits TFS3 to TFS0 sets to 1, TFS8 also sets to 1. • For the PTPEDMAC: TFS25 to TFS9: Reserved TFS8: Transmit abort was detected (value is equivalent to the EESR.TABT flag) TFS7 to TFS1: Reserved TFS0: The transmission source MAC address of the transmit frame data did not match the set value (value is equivalent to the EESR.MACE flag). When a bit sets to 1, it indicates that the associated error occurred during frame transmission. When any of the TFS bits sets to 1, the TFE bit also sets to 1. When TFS0 sets to 1, TFS8 also sets to 1.	R/W
b26	TWBI	Write-Back Complete Interrupt Enable	0: Do not generate interrupt when write-back to this descriptor is complete 1: Generate interrupt when write-back to this descriptor is complete.	R/W
b27	TFE	Transmit Frame Error	0: Frame transmission is successfully complete 1: Error occurred during frame transmission (transmission aborted).	R/W
b29, b28	TFP[1:0]	Transmit Frame Position	b29 b28 0 0: Transmit buffer indicated in this descriptor is the middle of a transmit frame (frame information is incomplete) 0 1: Transmit buffer indicated in this descriptor is the end of a transmit frame (frame information is complete) 1 0: Transmit buffer indicated in this descriptor is the head of a transmit frame (frame information is incomplete) 1 1: Transmit buffer indicated in this descriptor is all of a transmit frame (one buffer per frame).	R/W
b30	TDLE	Transmit Descriptor List End	When this bit is 1, it indicates that this descriptor is the last in the descriptor list.	R/W
b31	TACT	Transmit Descriptor Valid	This bit indicates that this descriptor is valid.	R/W

Note: Bits for write-back are underlined.

TD0 specifies the transmit frame settings and indicates the status after transmission.

TFE bit (Transmit Frame Error)

When the TFE bit is 1, it indicates that any of the TFS bits is 1.

TFP[1:0] bits (Transmit Frame Position)

The TFP[1:0] bits indicate which part of a transmit frame corresponds to the transmit buffer indicated in this descriptor. The TFP[1:0] and TD1.TBL bit settings must be logically consistent in the previous and next descriptors.

(1) 发送描述符0(TD0)

Bit	Symbol	位名称	Description	R/W
b25 to b0	TFS	发送帧状态	创建描述符时将所有位设置为0。回写后，这些位指示以下内容： 对于EDMAC0：TFS25到TFS9：保留 TFS8：检测到发送中止（值相当于EESR.TABT flag) TFS7到TFS4：保留 TFS3：未检测到载波（值相当于EESR.CND标志）TFS2：检测到载波丢失（值相当于EESR.DLC flag) TFS1：在传输过程中检测到后期冲突（值相当于EESR.CD标志）TFS0：传输重试结束（值相当于EESR.TRO标志）。当某个位设置为1时，表示在帧传输期间发生了相关错误。当任何TFS位设置为1时，TFE位也设置为1。当任何位TFS3到TFS0设置为1时，TFS8也设置为1。 对于PTPEDMAC：TFS25到TFS9：保留 TFS8：检测到发送中止（值相当于EESR.TABT flag) TFS7到TFS1：保留 TFS0：发送帧数据的发送源MAC地址与设定值不匹配（值相当于EESR.MACE标志）。 当某个位设置为1时，表示在帧传输期间发生了相关错误。当任何TFS位设置为1时，TFE位也设置为1。当TFS0设置为1时，TFS8也设置为1。	R/W
b26	TWBI	Write-Back Complete 中断使能	0：回写该描述符完成时不产生中断1：回写该描述符完成时产生中断。	R/W
b27	TFE	传输帧错误	0：帧传输成功完成1：帧传输过程中发生错误（传输中止）。	R/W
b29, b28	TFP[1:0]	发送帧位置	b29b2800：此描述符中指示的传输缓冲区是传输帧的中间（帧信息不完整）01：此描述符中指示的传输缓冲区是传输帧的结尾（帧信息完整）10：传输此描述符中指示的缓冲区是传输帧的头部（帧信息不完整）11：此描述符中指示的传输缓冲区是一个传输帧的全部（每帧一个缓冲区）。	R/W
b30	TDLE	传输描述符列表结束	当该位为1时，表示该描述符是描述符列表中的最后一个。	R/W
b31	TACT	传输描述符有效	该位指示该描述符有效。	R/W

Note: 用于回写的位带有下划线。

TD0指定传输帧设置并指示传输后的状态。

TFE位（发送帧错误）

当TFE位为1时，表示任何TFS位为1。

TFP[1:0]位（发送帧位置）

TFP[1:0]位指示发送帧的哪一部分对应于该描述符中指示的发送缓冲区。
TFP[1:0]和TD1.TBL位设置在前一个和下一个描述符中必须在逻辑上一致。

TACT bit (Transmit Descriptor Valid)

The TACT bit indicates that this descriptor is valid. The TACT bit is set to 1 by software. This bit clears to 0 when the transmit frame is transferred or when the transmission is aborted.

(2) Transmit descriptor 1 (TD1)

Bit	Symbol	Bit name	Description	R/W
b15 to b0	—	Reserved	The read value is 0. The write value should be 0.	R/W
b31 to b16	TBL	Transmit Buffer Length	Specifies the valid byte length of the associated transmit buffer. Set a value equal to or greater than 1.	R/W

TD1 specifies the valid byte length of the transmit buffer.

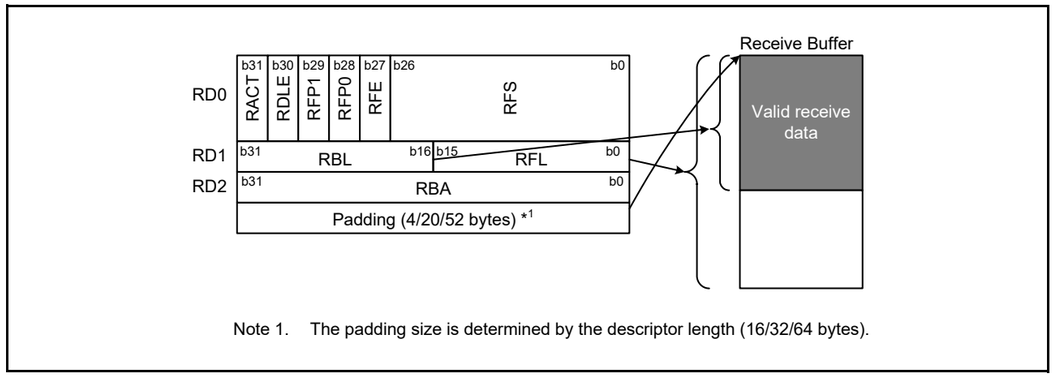
(3) Transmit descriptor 2 (TD2)

Bit	Symbol	Bit name	Description	R/W
b31 to b0	TBA	Transmit Buffer Address	Specifies the start address of the transmit buffer. When the TD1.TBL bit value is 1 to 16 bytes, align it on a 32-byte boundary.	R/W

TD2 specifies the start address of the transmit buffer.

31.3.1.2 Receive descriptor

Figure 31.4 shows the relationship between a receive descriptor and receive buffer. The receive frame and receive buffer configuration can be specified as one buffer per frame (single-buffer frame transmission) or multiple buffers per frame (multi-buffer frame transmission) by setting the receive descriptor. If the receive buffer length (RBL) is set to 0, operation indicated in the descriptor is not guaranteed.



Note 1. The padding size is determined by the descriptor length (16/32/64 bytes).

Figure 31.4 Relationship between receive descriptor and receive buffer

TACT位（发送描述符有效）

TACT位指示该描述符是有效的。TACT位由软件设置为1。当传输帧被传输或传输被中止时，该位清零。

(2) 传输描述符1(TD1)

Bit	Symbol	位名称	Description	R/W
b15 to b0	—	Reserved	读取值为0。写入值应为0。	R/W
b31 to b16	TBL	发送缓冲区长度	指定相关传输缓冲区的有效字节长度。设置一个等于或大于1的值。	R/W

TD1指定发送缓冲区的有效字节长度。

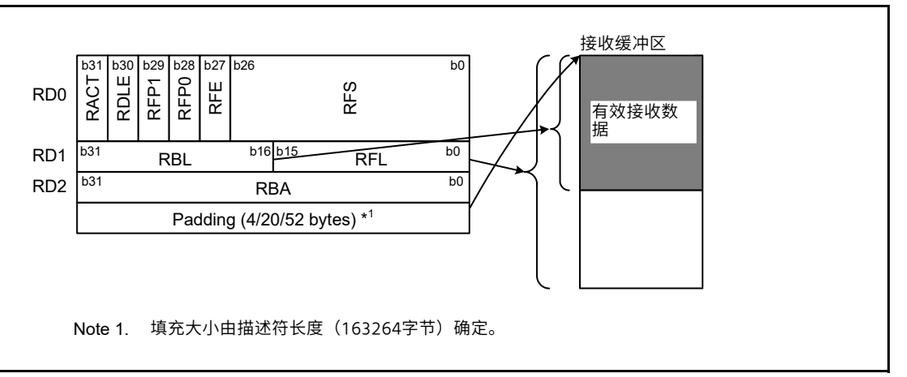
(3) 传输描述符2(TD2)

Bit	Symbol	位名称	Description	R/W
b31 to b0	TBA	发送缓冲区地址	指定发送缓冲区的起始地址。当TD1.TBL位值为1到16字节时，将其对齐在32字节边界上。	R/W

TD2指定发送缓冲区的起始地址。

31.3.1.2 接收描述符

图31.4显示了接收描述符和接收缓冲区之间的关系。通过设置接收描述符，可以将接收帧和接收缓冲区配置指定为每帧一个缓冲区（单缓冲区帧传输）或每帧多个缓冲区（多缓冲区帧传输）。如果接收缓冲区长度(RBL)设置为0，则无法保证描述符中指示的操作。



Note 1. 填充大小由描述符长度（163264字节）确定。

Figure 31.4 接收描述符和接收缓冲区的关系

(1) Receive descriptor 0 (RD0)

Bit	Symbol	Bit name	Description	R/W
b26 to b0	RFS	Receive Frame Status	Set all bits to 0 when creating a descriptor. After write-back, the bits indicate the following: • For EDMAC0: RFS26 to RFS10: Reserved RFS9: Receive FIFO overflow (value is equivalent to the EESR.RFOF flag) RFS8: Receive abort was detected (value is equivalent to the EESR.RABT flag) RFS7: Multicast address frame was received (value is equivalent to the EESR.RMAF flag) RFS6 and RFS5: Reserved RFS4: Alignment error was detected (value is equivalent to the EESR.RRF flag) RFS3: Frame-too-long error (value is equivalent to the EESR.RTLF flag) RFS2: Frame-too-short error (value is equivalent to the EESR.RTSF flag) RFS1: PHY-LSI receive error (value is equivalent to the EESR.PRE flag) RFS0: CRC error (value is equivalent to the EESR.CERF flag). When a bit sets to 1, it indicates that the associated error occurred during frame reception. When any of the RFS bits sets to 1, the RFE bit also sets to 1. (Set the TRSCER register to select whether bits RFS7 and RFS4 are reflected in the RFE bit.) When any of bits RFS3 to RFS0 sets to 1, RFS8 also sets to 1. • For the PTPEDMAC: RFS26 to RFS10: Reserved RFS9: Receive FIFO overflow (value is equivalent to the EESR.RFOF flag) RFS8: Reserved RFS4: PTPV2 packet was received (value is equivalent to the EESR.PVER flag) (The PTPEDMAC can only receive PTP packets. If a non-PTP packet is received, the packet is not transferred to the PTPEDAC, and it is discarded.) RFS3 to RFS0: Type of the received PTP message (value is equivalent to the EESR.TYPE[3:0] flags). Each bit indicates the status of the received frame.	R/W
b27	RFE	Receive Frame Error	• For EDMAC0: 0: No error occurred in the received frame 1: Error occurred in the received frame. • For the PTPEDMAC: Reserved.	R/W
b29, b28	RFP[1:0]	Receive Frame Position	b29 b28 0 0: Receive buffer indicated in this descriptor is the middle of a receive frame (frame information is incomplete) 0 1: Receive buffer indicated in this descriptor is the end of a receive frame (frame information is complete) 1 0: Receive buffer indicated in this descriptor is the head of a receive frame (frame information is incomplete) 1 1: Receive buffer indicated in this descriptor is all of a receive frame (one buffer per frame).	R/W
b30	RDLE	Receive Descriptor List End	When this bit is 1, it indicates that this descriptor is the last in the descriptor list.	R/W
b31	RACT	Receive Descriptor Valid	Indicates that this descriptor is valid.	R/W

Note: Bits for write-back are underlined.

RD0 indicates the receive frame status.

RFE bit (Receive Frame Error)

When the RFE bit is 1, it indicates that any of the RFS bits is 1. Set the TRSCER register to select whether the RFS7 and RFS4 bits of EDMAC0 are reflected in the RFE bit.

RFP[1:0] bits (Receive Frame Position)

The RFP[1:0] bits indicate which part of a receive frame corresponds to the receive buffer indicated in this descriptor.

(1) 接收描述符0(RD0)

Bit	Symbol	位名称	Description	R/W
b26 to b0	RFS	接收帧 Status	创建描述符时将所有位设置为0。回写后，这些位指示以下内容： 对于EDMAC0：RFS26到RFS 10：保留 RFS9：接收FIFO溢出（值相当于EESR.RFOF标志） RFS8：检测到接收中止（值等同于EESR.RABT标志） RFS7：收到多播地址帧（值相当于 EESR.RMAF flag) RFS6和RFS5：保留 RFS4：检测到对齐错误（值等同于EESR.RRF标志） RFS3：帧过长错误（值相当于EESR.RTLF标志）RFS2：帧过短错误（值相当于EESR.RTSF标志）RFS1：PHY-LSI接收错误（值相当于EESR.PRE标志） RFS0：CRC错误（值相当于EESR.CERF标志）。 当某个位设置为1时，表示在帧接收期间发生了相关错误。当任何RFS位设置为1时，RFE位也设置为1。（设置TRSCER寄存器以选择位RFS7和RFS4是否反映在RFE位中。）当任何位RFS3至RFS0设置为1时，RFS8也设置为1。 对于PTPEDMAC：RFS26到R FS10：保留 RFS9：接收FIFO溢出（值相当于EESR.RFOF标志） RFS8: Reserved RFS4:PTPV2packetwasreceived（值相当于EESR.PVER标志）（PTPEDMAC只能接收PTP数据包，如果接收到非PTP数据包，则该数据包不会传输到PTPEDAC，会被丢弃。）RFS3到RFS0：接收到的PTP消息的类型（值相当于 EESR.TYPE[3:0] flags). 每个位表示接收帧的状态。	R/W
b27	RFE	接收帧错误	对于EDMAC0：0：接收帧中没有发生错误1：接收帧中发生错误。 对于PTPEDMAC：保留 。	R/W
b29, b28	RFP[1:0]	接收帧 Position	b29b2800：此描述符中指示的接收缓冲区是接收帧的中间（帧信息不完整）01：此描述符中指示的接收缓冲区是接收帧的结尾（帧信息完整）10：接收此描述符中指示的缓冲区是接收帧的头部（帧信息不完整）11：此描述符中指示的接收缓冲区是一个接收帧的全部（每帧一个缓冲区）。	R/W
b30	RDLE	接收描述符列表结束	当该位为1时，表示该描述符是描述符列表中的最后一个。	R/W
b31	RACT	接收描述符 Valid	表示此描述符有效。	R/W

Note: 用于回写的位带有下划线。

RD0指示接收帧状态。

RFE位（接收帧错误）

当RFE位为1时，表示任何一个RFS位为1。设置TRSCER寄存器以选择是否RFS7和EDMAC0的RFS4位反映在RFE位中。

RFP[1:0]位（接收帧位置）

RFP[1:0]位指示接收帧的哪一部分对应于该描述符中指示的接收缓冲区。

RACT bit (Receive Descriptor Valid)

The RACT bit indicates that this descriptor is valid. The RACT bit is set to 1 by software. This bit clears to 0 when all data is transferred to the receive buffer indicated in RD2 or when the receive buffer becomes full.

(2) Receive descriptor 1 (RD1)

Bit	Symbol	Bit name	Description	R/W
b15 to b0	RFL	Receive Frame Length	Specifies the length (number of bytes) of the receive frame stored in the buffer. This does not include the number of bytes for padding set in the RPADIR register. These bits are written back to the descriptor associated with the end of a frame.	R/W
b31 to b16	RBL	Receive Buffer Length	Specifies the byte length of the associated receive buffer. Set an integral multiple of 32 as the buffer length.	R/W

Note: Bits for write-back are underlined.

RD1 specifies the receive buffer length. When reception is complete, the receive frame length is written back.

(3) Receive descriptor 2 (RD2)

Bit	Symbol	Bit name	Description	R/W
b31 to b0	RBA	Receive Buffer Address	Specifies the start address of the receive buffer. Align the buffer address on a 32-byte boundary.	R/W

RD2 specifies the start address of the receive buffer.

RACT位（接收描述符有效）

RACT位指示该描述符是有效的。RACT位由软件设置为1。当所有数据传输到RD2中指示的接收缓冲区或接收缓冲区已满时，该位清0。

(2) 接收描述符1(RD1)

Bit	Symbol	位名称	Description	R/W
b15 to b0	RFL	接收帧 Length	指定存储在缓冲区中的接收帧的长度（字节数）。这不包括RPADIR寄存器中设置的填充字节数。这些位被写回与帧结束相关的描述符。	R/W
b31 to b16	RBL	接收缓冲区长度	指定相关接收缓冲区的字节长度。设置32的整数倍作为缓冲区长度。	R/W

Note: 用于回写的位带有下划线。

RD1指定接收缓冲区长度。当接收完成时，接收帧长度被写回。

(3) 接收描述符2(RD2)

Bit	Symbol	位名称	Description	R/W
b31 to b0	RBA	接收缓冲区 Address	指定接收缓冲区的起始地址。在32字节边界上对齐缓冲区地址。	R/W

RD2指定接收缓冲区的起始地址。

31.3.2 Transmission

When the EDTRR.TR bit is set to 1 while the ETHERC0.ECMR.TE bit is 1, the EDMAC reads the descriptor following the previously used descriptor in the transmit descriptor list (or the descriptor indicated in the TDLAR register after a reset). When the TACT bit is 1 in the transmit descriptor (TD0), the EDMAC sequentially reads transmit data from the start address of the transmit buffer indicated in transmit descriptor 2 (TD2) and transfers it to the ETHERC through the transmit FIFO. The ETHERC creates a transmit frame and starts transmission to the MII or RMII. When all data indicated in the TD1.TBL bit is transferred, write-back is performed based on the TD0.TFP[1:0] bit setting as follows:

- When the TD0.TFP[1:0] bits are 00b or 10b (frame is incomplete), the TD0.TACT bit is written back
- When the TD0.TFP[1:0] bits are 01b or 11b (frame is complete), the TD0.TACT, TD0.TFS, and TD0.TFE bits are written back.

When the TD0.TACT bit in the read descriptor is 1, the EDMAC continues reading descriptors and transmit frames. When the TD0.TACT bit in the read descriptor is 0, the EDMAC sets the EDTRR.TR bit to 0 and stops transmission.

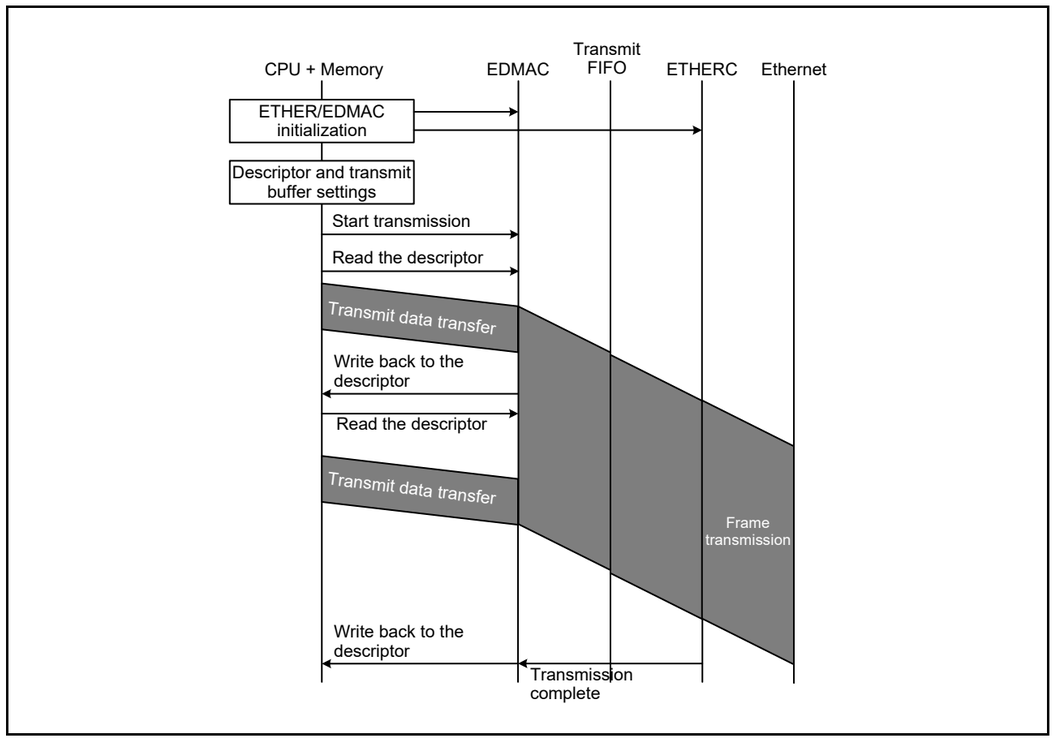


Figure 31.5 Example of transmission flow

31.3.2 Transmission

当EDTRR.TR位设置为1而ETHERC0.ECMR.TE位为1时，EDMAC读取发送描述符列表中先前使用的描述符之后的描述符（或复位后TDLAR寄存器中指示的描述符）。当发送描述符(TD0)中的TACT位为1时，EDMAC从发送描述符2(TD2)中指示的发送缓冲区的起始地址顺序读取发送数据，并通过发送FIFO将其传输到ETHERC。ETHERC创建一个传输帧并开始传输到MII或RMII。当传输TD1.TBL位中指示的所有数据时，将根据TD0.TFP[1:0]位设置执行回写，如下所示：

- 当TD0.TFP[1:0]位为00b或10b（帧不完整）时，回写TD0.TACT位
- 当TD0.TFP[1:0]位为01b或11b（帧完成）时，TD0.TACT、TD0.TFS和TD0.TFE位被写回。

当读取描述符中的TD0.TACT位为1时，EDMAC继续读取描述符并发送帧。当读描述符中的TD0.TACT位为0时，EDMAC将EDTRR.TR位设置为0并停止传输。

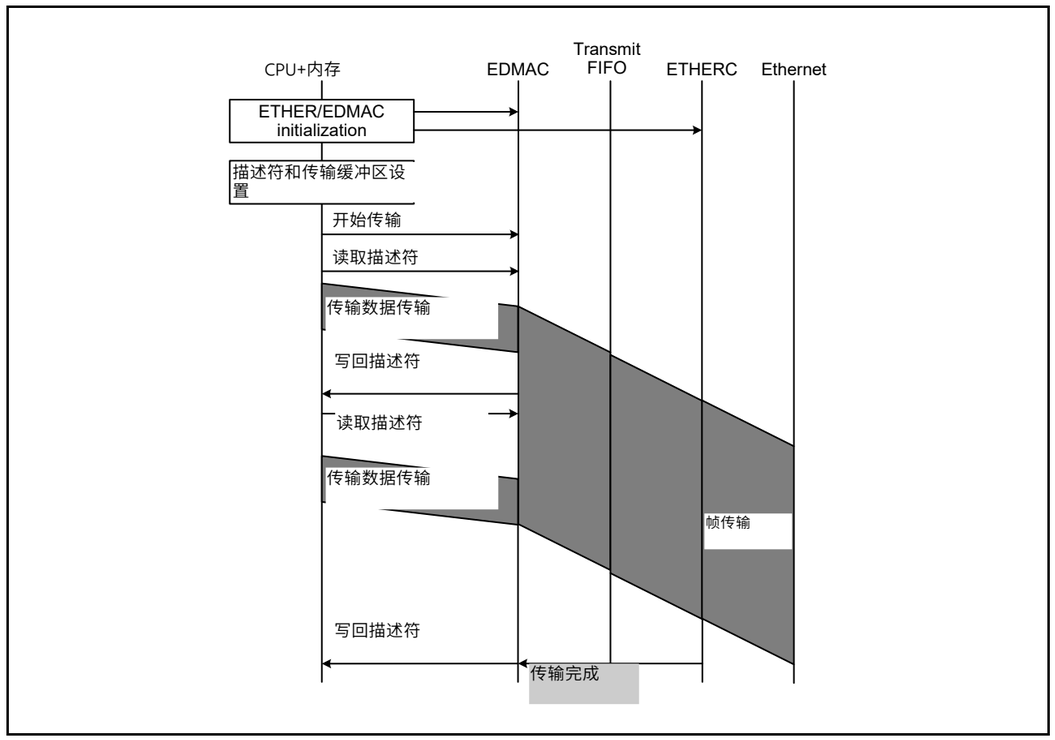


Figure 31.5 传输流程示例

31.3.3 Reception

When the EDRRR.RR bit is set to 1 while the ETHERC0.ECMR.RE bit is 1, the EDMAC reads the receive descriptor following the previously used descriptor (or the descriptor indicated in the RDLAR register after a reset) and then waits for reception. When the RD0.RACT bit is 1, if the data stored in the receive FIFO is 32 bytes or more, or if the end byte of the frame is stored in the receive buffer, the EDMAC transfers data from the receive FIFO to the receive buffer indicated in receive descriptor 2 (RD2).

If the data length of the received frame is longer than the buffer length set in the RBL bit in receive descriptor 1 (RD1), the EDMAC writes back 10b or 00b to the RD0.RFP[1:0] bits and 0 to the RD0.RACT bit when the receive buffer becomes full, and then the EDMAC reads the next data. After that, the EDMAC transfers data to another receive buffer.

When the frame reception is complete or when the frame reception is aborted by an error, the EDMAC writes back 11b or 01b to the RD0.RFP[1:0] bits, 0 to the RD0.RACT bit, and the receive frame length to the RD1.RFL bit. When the RMCR.RNR bit is 1, the EDMAC reads the next descriptor and waits for reception. When the RNR bit is 0, the EDMAC sets the EDRRR.RR bit to 0 and stops reception.

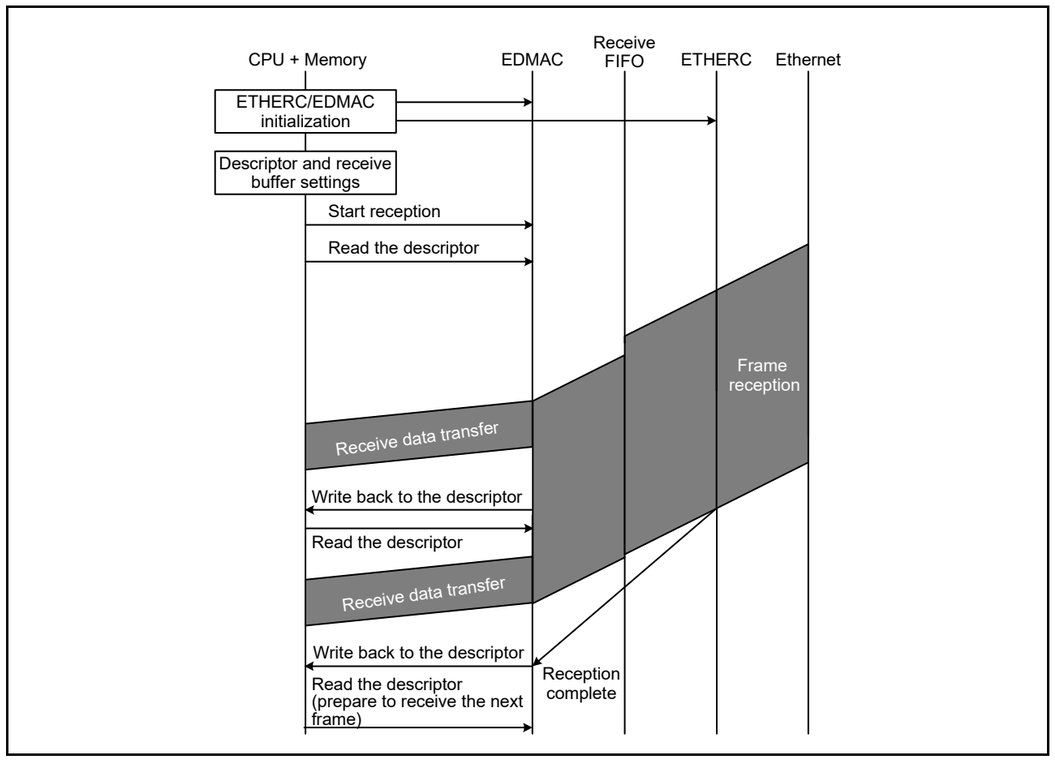


Figure 31.6 Example of reception flow

31.3.3 Reception

当EDRRR.RR位设置为1而ETHERC0.ECMR.RE位为1时，EDMAC读取先前使用的描述符（或复位后RDLAR寄存器中指示的描述符）之后的接收描述符，然后等待接收.当RD0.RACT位为1时，如果存储在接收FIFO中的数据为32字节或更多，或者如果帧的结束字节存储在接收缓冲区中，则EDMAC将数据从接收FIFO传输到接收缓冲区在接收描述符2(RD2)中指示。

如果接收帧的数据长度大于接收描述符1(RD1)中RBL位中设置的缓冲区长度，则EDMAC将10b或00b写回RD0.RFP[1:0]位，并将0写回RD0.RACT位当接收缓冲器变满时，EDMAC读取下一个数据。之后，EDMAC将数据传输到另一个接收缓冲区。

当帧接收完成或帧接收因错误而中止时，EDMAC将11b或01b写回RD0.RFP[1:0]位，将0写回RD0.RACT位，并将接收帧长度写入RD1.RFL位。当RMCR.RNR位为1时，EDMAC读取下一个描述符并等待接收。当RNR位为0时，EDMAC将EDRRR.RR位设置为0并停止接收。

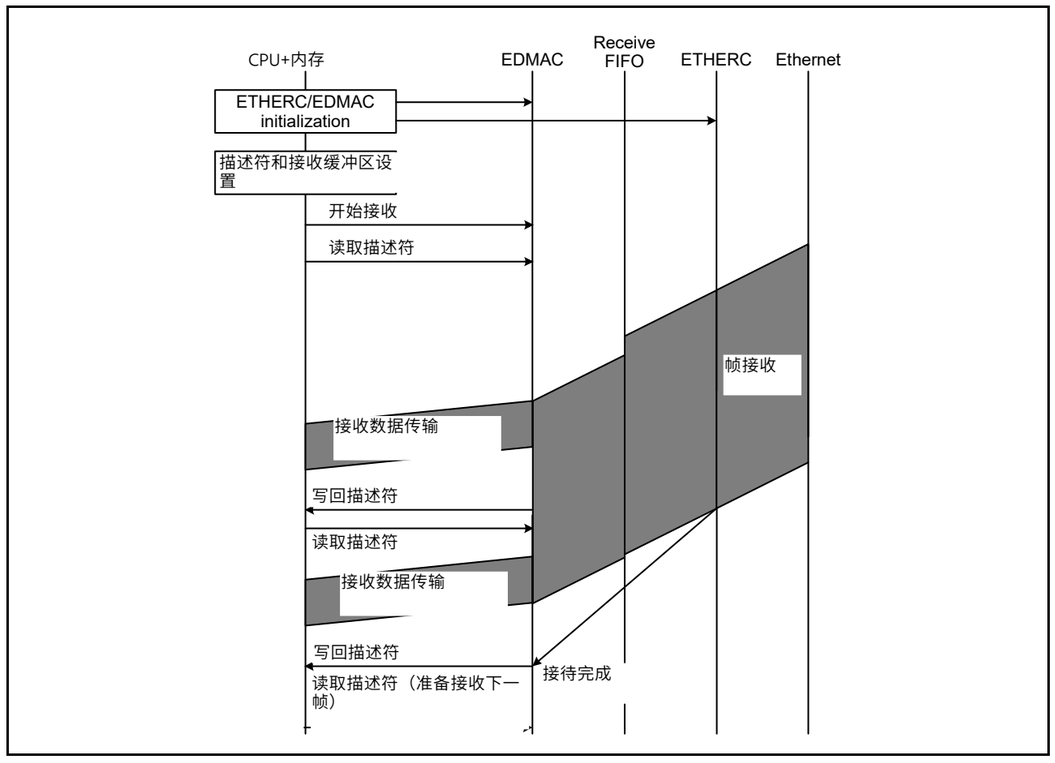


Figure 31.6 接收流程示例

31.3.4 Multi-Buffer Frame Transmission

31.3.4.1 Error processing while transmitting multi-buffer frame

If an error occurs during multi-buffer frame transmission, the EDMAC performs the processing shown in Figure 31.7. In the figure, when the TACT bit of transmit descriptor 0 (TD0) is 0, the descriptor indicates that all data in the buffer is successfully transmitted. When the TACT bit is 1, the descriptor indicates that data in the buffer is not yet transmitted. If a frame transmit error*1 occurs in the head or middle of the frame while the TD0.TACT bit is 1, the EDMAC stops data transmission from the transmit FIFO and EDMAC data transfer, and sets the TD0.TACT bit to 0.

After that, the EDMAC reads the next descriptor to see if the descriptor indicates the middle of the frame (TD0.TFP[1:0] bits are 00b) or the end of the frame (TD0.TFP[1:0] bits are 01b). When the descriptor indicates the middle of the frame, the EDMAC sets the TD0.TACT bit to 0 and reads the next descriptor. When the descriptor indicates the end of the frame, in addition to setting the TD0.TACT bit to 0, the EDMAC also writes back to the TD0.TFE and TD0.TFS bits.

After an error occurs, data in the buffer is not transmitted until write-back to the descriptor for the end of the frame. When the associated transmit error interrupt is enabled in the EESIPR register, an interrupt request is generated immediately after write-back to the descriptor for the end of the frame.

Note 1. For EDMAC0, a transmit retry-over condition, late collision, or loss of carrier is detected, or a carrier is not detected. For the PTPEDMAC, the MAC address does not match the set value.

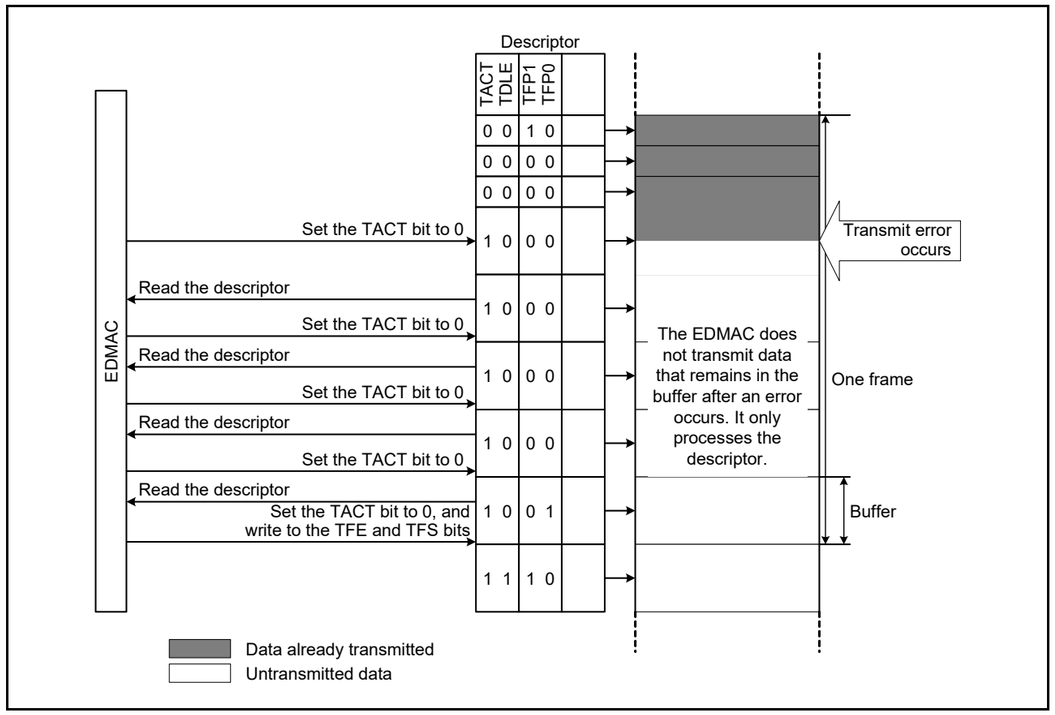


Figure 31.7 EDMAC operation after transmit error occurs

31.3.4 多缓冲区帧传输

31.3.4.1 传输多缓冲帧时的错误处理

如果在多缓冲帧传输过程中发生错误，EDMAC将执行图31.7所示的处理。图中，当发送描述符0（TD0）的TACT位为0时，描述符表示缓冲区中的所有数据都发送成功。当TACT位为1时，描述符指示缓冲区中的数据尚未传输。如果在TD0.TACT位为1时在帧的头部或中间发生帧发送错误*1，则EDMAC停止来自发送FIFO的数据传输和EDMAC数据传输，并将TD0.TACT位设置为0。

之后，EDMAC读取下一个描述符，看描述符是表示帧中间（TD0.TFP[1:0]位为00b）还是帧结束（TD0.TFP[1:0]位为01b)。当描述符指示帧的中间时，EDMAC将TD0.TACT位设置为0并读取下一个描述符。当描述符指示帧结束时，除了将TD0.TACT位设置为0外，EDMAC还写回TD0.TFE和TD0.TFS位。

发生错误后，缓冲区中的数据不会传输，直到写回帧结束的描述符。
当在ESIPR寄存器中使能相关的发送错误中断时，在帧结束写回描述符后立即生成中断请求。

注1.对于EDMAC0，检测到传输重试条件、延迟冲突或载波丢失，或未检测到载波。对于PTPEDMAC，MAC地址与设定值不匹配。

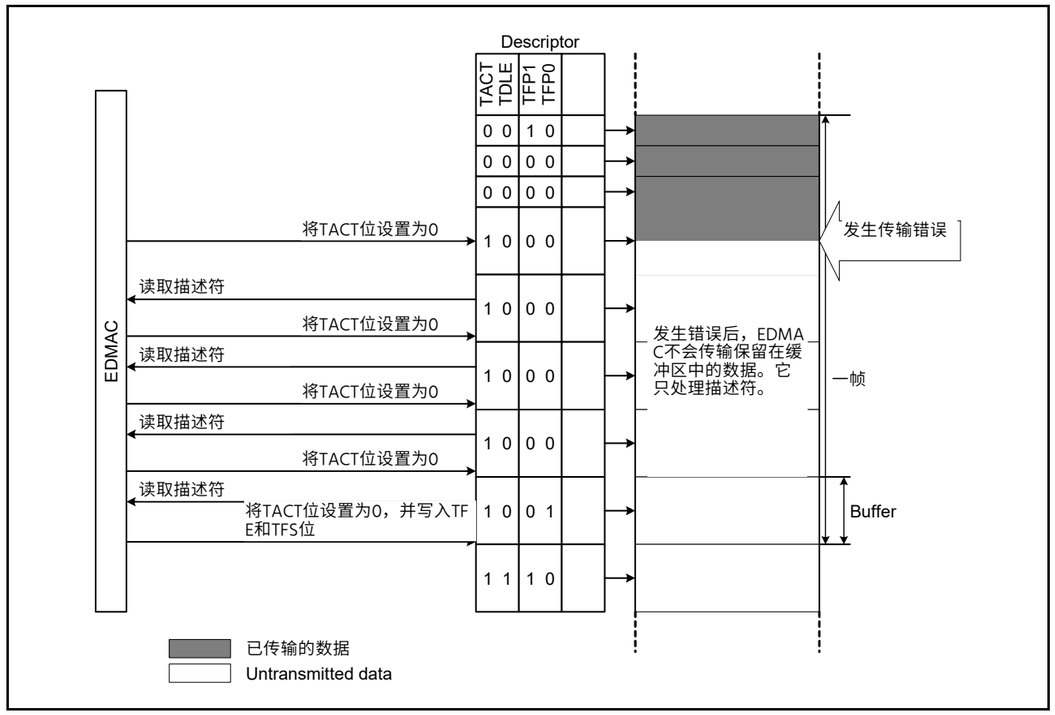


Figure 31.7 发生传输错误后的EDMAC操作

31.3.4.2 Error processing while receiving multi-buffer frame

If an error occurs during multi-buffer frame reception, the EDMAC performs the processing shown in Figure 31.8. In the figure, when the RACT bit of receive descriptor 0 (RD0) is 0, the descriptor indicates that data was successfully received in the buffer. When the RACT bit is 1, the descriptor indicates that data is not yet received in the buffer. If a frame receive error*1 occurs, the EDMAC stops receiving new data, but it transfers data that is already stored in the receive FIFO to the receive buffer.

When the receive buffer becomes full during transfer, the EDMAC sets the RACT bit to 0 and the RFP[1:0] bits to 10b or 00b and reads the next descriptor. After all data in the receive FIFO is transferred, the EDMAC writes back the status to the descriptor.

When the associated receive error interrupt is enabled in the EESIPR register, an interrupt request is generated immediately after write-back to the descriptor. When there is a request to receive a new frame, the EDMAC continues reception using the descriptor following the descriptor where the error occurred.

Note 1. For EDMAC0, a CRC error, PHY-LSI receive error, frame-too-short error, frame-too-long error, or alignment error is detected. For the PTPEDMAC, a parity error is detected.

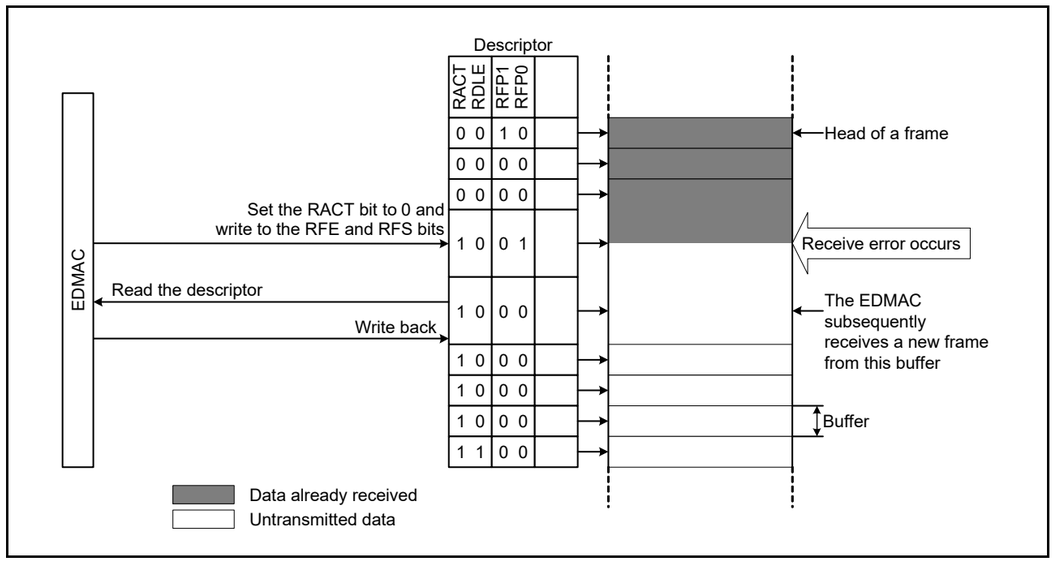


Figure 31.8 EDMAC operation after receive error occurs

31.3.4.2 接收多缓冲帧时的错误处理

如果在多缓冲区帧接收过程中发生错误，EDMAC将执行图31.8所示的处理。图中，当接收描述符0（RD0）的RACT位为0时，描述符表示缓冲区成功接收到数据。当RACT位为1时，描述符指示缓冲区中尚未接收到数据。如果发生帧接收错误*1，EDMAC将停止接收新数据，但会将已存储在接收FIFO中的数据传输到接收缓冲区。

当接收缓冲区在传输过程中变满时，EDMAC将RACT位设置为0，并将RFP[1:0]位设置为10b或00b并读取下一个描述符。接收FIFO中的所有数据传输完毕后，EDMAC将状态写回描述符。

当在ESIPR寄存器中启用相关的接收错误中断时，在写回描述符后立即生成中断请求。当有接收新帧的请求时，EDMAC使用发生错误的描述符之后的描述符继续接收。

注1.对于EDMAC0，检测到CRC错误、PHY-LSI接收错误、帧太短错误、帧太长错误或对齐错误。对于PTPEDMAC，检测到奇偶校验错误。

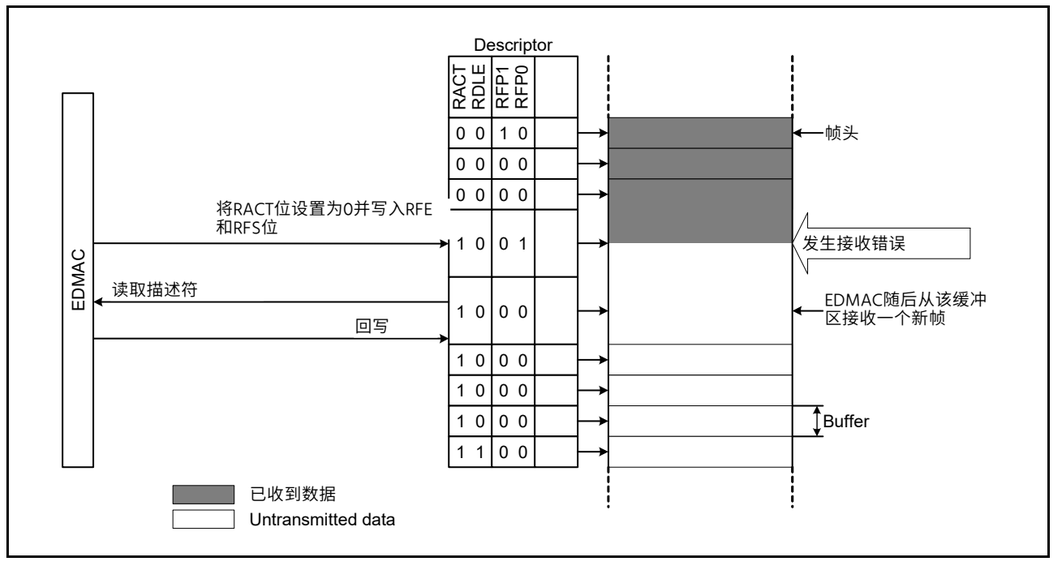


Figure 31.8 发生接收错误后的EDMAC操作

31.3.5 EDMAC Channel Priority

This section describes the priority of the two EDMAC channels (EDMAC0, PTPEDMAC). Each time transfer of one channel is complete, that channel takes the lowest priority. This operation is shown in Figure 31.9. After a reset, the priority is EDMAC0 > PTPEDMAC.

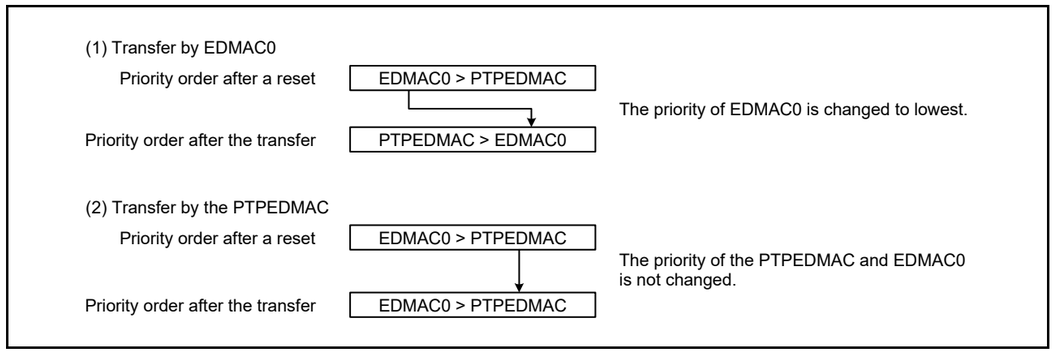


Figure 31.9 Channel priority order

Figure 31.10 shows the change in the channel priority order when transfer requests are concurrently generated to EDMAC0 and the PTPEDMAC.

The operations in the figure are as follows:

1. Transfer requests are concurrently sent to EDMAC0.
2. The EDMAC0 starts a transfer.
3. After EDMAC0 ends the transfer, the priority of EDMAC0 is changed to the lowest.
4. Transfer requests are concurrently sent to EDMAC0 and the PTPEDMAC.
5. Because PTPEDMAC has higher priority than the EDMAC0 at this time, PTPEDMAC starts a transfer and the EDMAC0 waits.
6. After PTPEDMAC ends the transfer, the priority of PTPEDMAC is changed to the lowest.
7. EDMAC0 starts a transfer.
8. After the EDMAC0 ends the transfer, the priority of EDMAC0 is changed to the lowest.

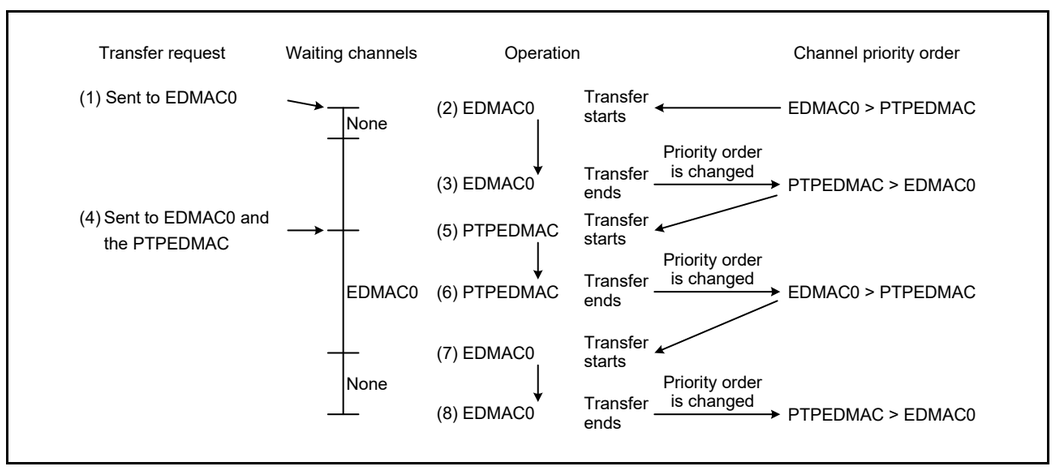


Figure 31.10 Example of channel priority order change

31.3.5 EDMAC通道优先级

本节介绍两个EDMAC通道（EDMAC0、PTPEDMAC）的优先级。每次完成一个通道的传输时，该通道的优先级最低。该操作如图31.9所示。复位后，优先级为EDMAC0>PTPEDMAC。

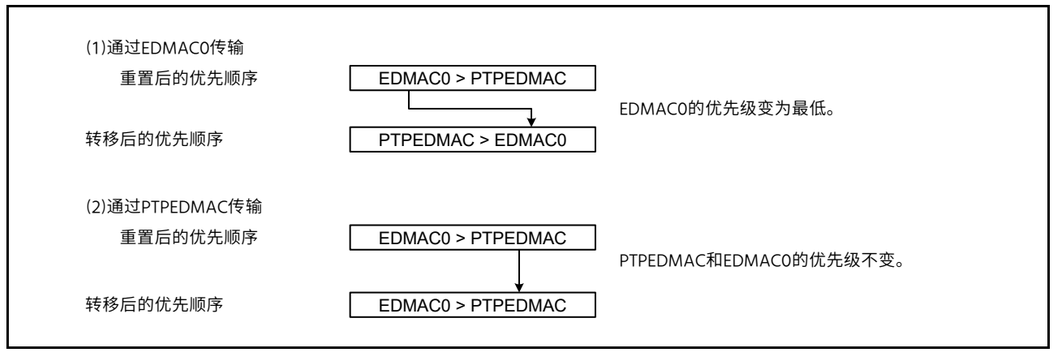


Figure 31.9 频道优先顺序

图31.10显示了同时生成传输请求时通道优先级顺序的变化EDMAC0和PTPEDMAC。

图中的操作如下：

1. 传输请求同时发送到EDMAC0。
2. EDMAC0开始传输。
3. EDMAC0结束传输后，EDMAC0的优先级变为最低。
4. 传输请求同时发送到EDMAC0和PTPEDMAC。
5. 由于此时PTPEDMAC的优先级高于EDMAC0，因此PTPEDMAC开始传输，并且EDMAC0 waits.
6. PTPEDMAC结束传输后，PTPEDMAC的优先级变为最低。
7. EDMAC0开始传输。
8. EDMAC0结束传输后，EDMAC0的优先级变为最低。

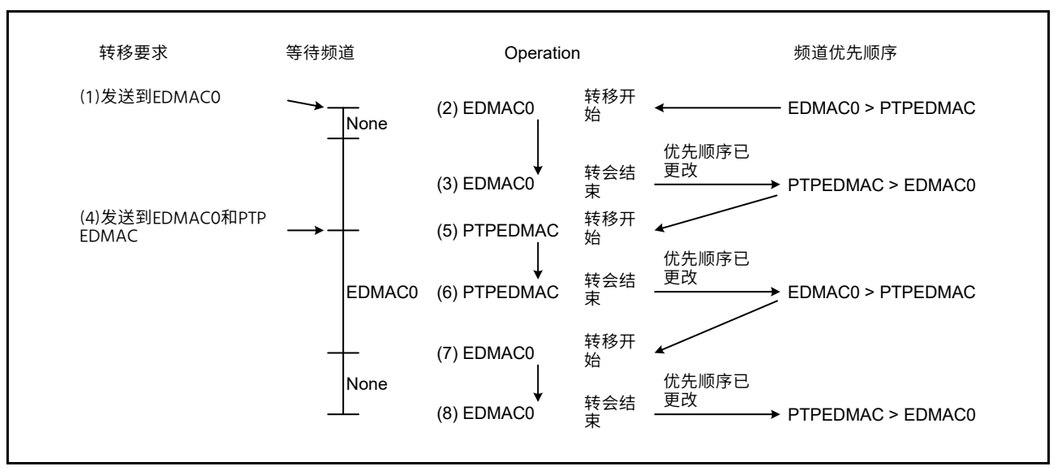


Figure 31.10 频道优先顺序更改示例

31.4 Interrupts

When any of the status flags in the EESR register sets to 1 while the associated interrupt request enable bit in the EESIPR register is 1, EDMAC0 issues an ETHER_EINT0 interrupt request or the PTPEDMAC issues an ETHER_PINT interrupt request to the CPU.

31.5 Usage Notes

31.5.1 Settings for the Module-Stop Function

The following bits in Module Stop Control Register B (MSTPCRB) enable or disable EDMAC module operation:

- The MSTPB15 bit in enables or disables ETHERC0 and EDMAC0 operation
- The MSTPCRB.MSTPB13 bit enables or disables EPTPC and PTPEDMAC operation.

The modules are initially stopped after reset. Releasing the module-stop state enables access to the registers. For details, see section 11, Low Power Modes.

Note: When EPTPC and PTPEDMAC operation is enabled (MSTPB13 = 0), some registers in the EPTPC module become inaccessible depending on the combination of the MSTPB15 bit and EPTPC bypass bit (BYPASS.BYPASS0) settings. See section 30.6.1, Constraints on Register Access.

31.5.2 Stopping the EDMAC during Operation

When stopping EDMAC operation by using a Sleep instruction or the module-stop function while the EDMAC is running, confirm that the EDTRR.TR and EDRRR.RR bits are 0. If the EDMAC is stopped while the EDTRR.TR or EDRRR.RR bit is 1, the data for the frame that is being transmitted or received might not be complete, and EDMAC operation after exiting Sleep mode or the module-stop state is not guaranteed.

31.4 Interrupts

当EESR寄存器中的任何状态标志设置为1而ESIPR寄存器中的相关中断请求使能位为1时，EDMAC0向CPU发出ETHER_EINT0中断请求或PTPEDMAC向CPU发出ETHER_PINT中断请求。

31.5 使用说明

31.5.1 模块停止功能的设置

模块停止控制寄存器B(MSTPCRB)中的以下位启用或禁用EDMAC模块操作：

- MSTPB15位启用或禁用ETHERC0和EDMAC0操作
- MSTPCRB.MSTPB13位启用或禁用EPTPC和PTPEDMAC操作。

模块在复位后最初停止。释放模块停止状态可以访问寄存器。有关详细信息，请参阅第11节，低功耗模式。

Note: 当EPTPC和PTPEDMAC操作使能(MSTPB13=0)时，EPTPC模块中的某些寄存器变得不可访问，具体取决于MSTPB15位和EPTPC旁路位(BYPASS.BYPASS0)设置的组合。请参阅第30.6.1节，寄存器访问限制。

31.5.2 在运行期间停止EDMAC

在EDMAC运行时使用休眠指令或模块停止功能停止EDMAC操作时，请确认EDTRR.TR和EDRRR.RR位为0。如果在EDTRR.TR或EDRRR.RR位时停止EDMAC为1，正在发送或接收的帧的数据可能不完整，并且无法保证退出休眠模式或模块停止状态后的EDMAC操作。

32. USB 2.0 Full-Speed Module (USBFS)

32.1 Overview

The MCU provides a USB 2.0 Full-Speed module (USBFS) that operates as a host or device controller compliant with the Universal Serial Bus (USB) specification revision 2.0. The host controller supports USB 2.0 full-speed and low-speed transfers, and the device controller supports USB 2.0 full-speed transfers. The USBFS has an internal USB transceiver and supports all of the transfer types defined in the USB 2.0 specification.

The USBFS has FIFO buffer for data transfers, providing a maximum of 10 pipes. Any endpoint number can be assigned to pipes 1 to 9, based on the peripheral devices or the communication requirements for your system.

Table 32.1 lists the USBFS specifications, Figure 32.1 shows a block diagram, and Table 32.2 lists the I/O pins.

Table 32.1 USBFS specifications

Parameter	Specifications
Features	• USB Device Controller (UDC) and USB 2.0 transceiver supporting host controller, device controller, and On-The-Go (OTG) functions (one channel) • Host and device controller can be switched by software • Self-power or bus power mode selectable.
	Host controller features: • Full-speed transfer (12 Mbps) and low-speed transfer (1.5 Mbps) • Automatic scheduling for SOF and packet transmissions • Programmable intervals for isochronous and interrupt transfers • Communications with multiple peripheral devices connected through a single hub.
	Device controller features: • Full-speed transfer (12 Mbps)*1 • Control transfer stage control function • Auto response function for SET_ADDRESS request • SOF interpolation.
Supported transfer types	• Control transfer • Bulk transfer • Interrupt transfer • Isochronous transfer.
Pipe configuration	• FIFO buffer for USB communication • Up to 10 pipes selectable, including the Default Control Pipe (DCP) • Pipes 1 to 9 assignable to any endpoint number.
	Transfer conditions specifiable for each pipe: • Pipe 0: Control transfer with 64-byte single buffer • Pipes 1 and 2: Selectable to bulk transfer with 64-byte double buffer or isochronous transfer with 256-byte double buffer • Pipes 3 to 5: Bulk transfer with 64-byte double buffer • Pipes 6 to 9: Interrupt transfer with 64-byte single buffer.
Other features	• Reception end function using transaction count • Function that changes the BRDY interrupt event notification timing (BFRE) • Automatic clearing of the FIFO buffer after the data for the pipe specified in the DnFIFO port (n = 0, 1) is read (DCLRM) • NAK setting function for response PID generated on transfer end (SHTNAK) • On-chip pull-up and pull-down resistors for D+ and D-.
Module-stop function	Module-stop state can be set to reduce power consumption

Note 1. Low-speed transfer (1.5 Mbps) is not supported.

32. USB2.0全速模块(USBFS)

32.1 Overview

MCU提供USB2.0全速模块(USBFS)，可作为主机或设备控制器运行，符合通用串行总线(USB)规范修订版2.0。主机控制器支持USB2.0全速和低速传输，设备控制器支持USB2.0全速传输。USBFS有一个内部USB收发器，支持USB2.0规范中定义的所有传输类型。

USBFS具有用于数据传输的FIFO缓冲区，最多提供10个管道。根据外围设备或系统的通信要求，可以将任何端点编号分配给管道1到9。

表32.1列出了USBFS规范，图32.1显示了框图，表32.2列出了IO引脚。

Table 32.1 USBFS specifications

Parameter	Specifications
Features	USB设备控制器(UDC)和USB2.0收发器，支持主机控制器、设备控制器和On-The-Go(OTG)功能（一个通道） 主机和设备控制器可以通过软件切换 自供电或总线供电模式可选择的。
	主机控制器特性： 全速传输(12Mbps)和低速传输(1.5Mbps) SOF和数据包传输的自动调度 同步和中断传输的可编程间隔 与通过单个集线器连接的多个外围设备进行通信。
	设备控制器特性： 全速传输(12Mbps)*1 控制传输级控制功能 设备状态控制功能 SET_ADDRESS请求的自动响应功能 SOF插值。
支持的传输类型	控制传输 批量传输 中断传输 同步传输。
管道配置	用于USB通信的FIFO缓冲区 最多可选择10个管道，包括默认控制管道(DCP) 管道1到9可分配给任何端点编号。
	可为每个管道指定传输条件： 管道0：使用64字节单缓冲区进行控制传输 管道1和2：可选择使用64字节双缓冲区 进行批量传输或使用256字节双缓冲区 进行同步传输 管道3到5：使用64字节双缓冲区 的批量传输 管道6到9：使用64字节单缓冲区的中断传输。
其它功能	使用事务计数的接收结束功能 更改BRDY中断事件通知时序(BFRE)的功能 读取DnFIFO端口(n=0 1)中指定管道的数据后自动清除FIFO缓冲区(DCLRM) NAK设置功能，用于在传输结束时生成的响应PID(SHTNAK) D+和D-的片上上拉和下拉电阻。
Module-stop function	可设置模块停止状态以降低功耗

Note 1. 不支持低速传输(1.5Mbps)。

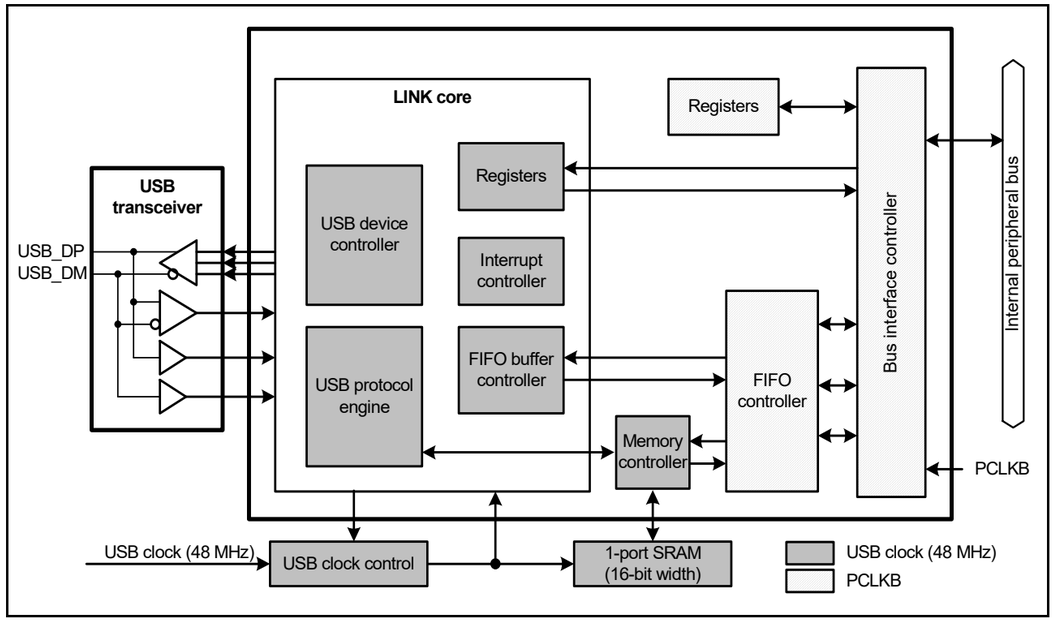


Figure 32.1 USBFS block diagram

Table 32.2 USBFS pin configuration

Port	Pin name	I/O	Function
USBFS	USB_DP	I/O	D+ I/O for the on-chip USB transceiver. Must be connected to the D+ data line of the USB bus.
	USB_DM	I/O	D- I/O pin for the on-chip USB transceiver. Must be connected to the D- data line of the USB bus.
	USB_VBUS	Input	USB cable connection monitor pin. Must be connected to VBUS signal on the USB bus. VBUS pin status (connected or disconnected) can be detected when the USBFS is a device controller.*1
	USB_EXICEN	Output	Low-power control signal for the OTG power supply IC
	USB_VBUSEN	Output	VBUS (5 V) enable signal for the external power supply IC
	USB_OVRCURA USB_OVRCURB	Input	Overcurrent pins for USBFS. Must be connected to external overcurrent detection signals. When the OTG power supply chip is connected, must be connected to the VBUS comparator signals.
	USB_ID	Input	Must be connected to MicroAB connector ID input signal in OTG mode
Shared	VCC_USB	Input	USB transceiver input supply voltage
	VSS_USB	Input	USB ground pin

Note 1. P407 is 5-V tolerant.

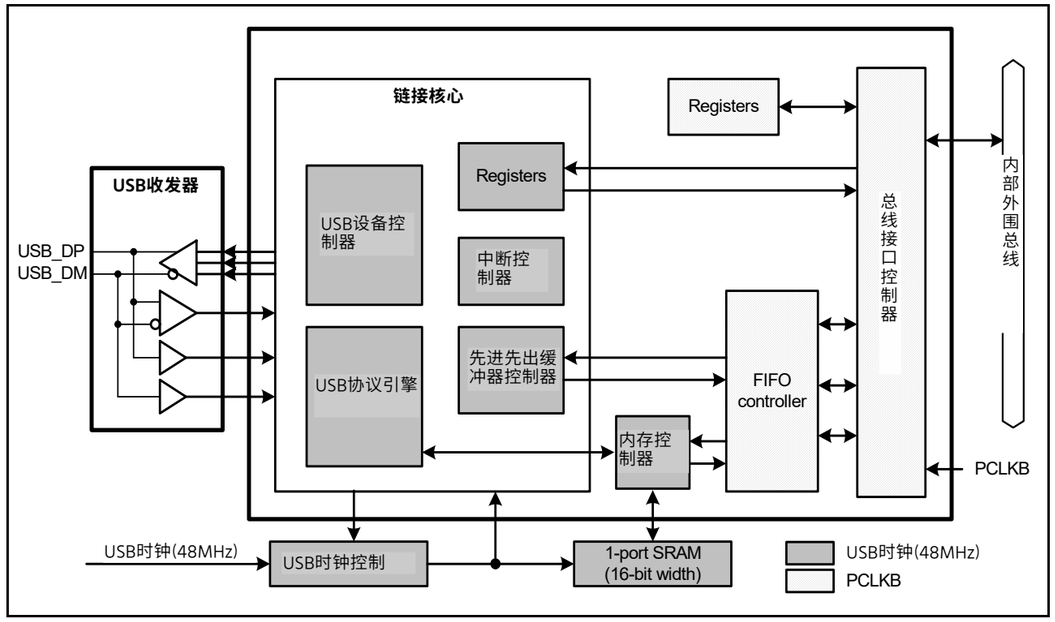


Figure 32.1 USBFS框图

Table 32.2 USBFS引脚配置

Port	引脚名称	I/O	Function
USBFS	USB_DP	I/O	D+IO用于片上USB收发器。 必须连接到USB总线的D+数据线。
	USB_DM	I/O	用于片上USB收发器的DIO引脚。 必须连接到USB总线的Ddata线。
	USB_VBUS	Input	USB电缆连接监视器引脚。 必须连接到USB总线上的VBUS信号。当USBFS为设备控制器时，可以检测VBUS引脚状态（连接或断开）。*1
	USB_EXICEN	Output	OTG电源IC的低功耗控制信号
	USB_VBUSEN	Output	外部电源IC的VBUS(5V)使能信号
	USB_OVRCURA USB_OVRCURB	Input	USBFS的过流引脚。 必须连接外部过流检测信号。当OTG供电芯片接上时，必须接上VBUS比较器信号。
	USB_ID	Input	OTG模式下必须连接MicroAB连接器ID输入信号
Shared	VCC_USB	Input	USB收发器输入电源电压
	VSS_USB	Input	USB接地引脚

Note 1. P407可耐受5V。

32.2 Register Descriptions

32.2.1 System Configuration Control Register (SYSCFG)

Address(es): USBFS.SYSCFG 4009 0000h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	SCKE	—	—	—	DCFM	DRPD	DPRPU	—	—	—	USBE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	USBE	USBFS Operation Enable	0: Disable 1: Enable.	R/W
b3, b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	DPRPU	D+ Line Resistor Control	0: Disable line pull-up 1: Enable line pull-up.	R/W
b5	DRPD	D+/D- Line Resistor Control	0: Disable line pull-down 1: Enable line pull-down.	R/W
b6	DCFM	Controller Function Select	0: Select device controller 1: Select host controller.	R/W
b9 to b7	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b10	SCKE	USB Clock Enable	0: Stop clock supply to the USBFS 1: Enable clock supply to the USBFS.	R/W
b15 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: After writing 1 to the SCKE bit, read it to confirm that it is set to 1.

USBE bit (USBFS Operation Enable)

The USBE bit enables or disables operation of the USBFS.

Changing the USBE bit from 1 to 0 initializes the bits listed in Table 32.3. Only change this bit while the SCKE bit is 1. In host controller mode, this bit must be set to 1 after setting the DRPD bit to 1, eliminating SYSSTS0.LNST[1:0] flag chattering, and confirming that the USB bus state is stable.

Table 32.3 Registers initialized by writing 0 to the SYSCFG.USBE bit

Selected function	Register	Bit	Remarks
Device controller	SYSSTS0	LNST[1:0]	Value is saved in host controller mode
	DVSTCTR0	RHST[2:0]	-
	INTSTS0	DVSQ[2:0]	Value is saved in host controller mode
	USBADDR	USBADDR[6:0]	Value is saved in host controller mode
	USBREQ	BREQUEST[7:0], BMREQUESTTYPE[7:0]	Value is saved in host controller mode
	USBVAL	WVALUE[15:0]	Value is saved in host controller mode
	USBINDX	WINDEX[15:0]	Value is saved in host controller mode
	USBLENG	WLENTUH[15:0]	Value is saved in host controller mode
Host controller	DVSTCTR0	RHST[2:0]	-
	FRMNUM	FRNM[10:0]	Value is saved in device controller mode

DPRPU bit (D+ Line Resistor Control)

The DPRPU bit enables or disables pulling up the D+ line in device controller mode.

When the DPRPU bit is set to 1 in device controller mode, the USBFS pulls up the D+ line to notify the USB host that it

32.2 注册说明

32.2.1 系统配置控制寄存器(SYSCFG)

Address(es): USBFS.SYSCFG 4009 0000h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	SCKE	—	—	—	DCFM	DRPD	DPRPU	—	—	—	USBE
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	USBE	USBFS操作启用	0：禁用1 ：启用。	R/W
b3, b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b4	DPRPU	D+线路电阻控制	0：禁用线路上拉1： 启用线路上拉。	R/W
b5	DRPD	D+DLine电阻控制	0：禁用线路下拉1：启 用线路下拉。	R/W
b6	DCFM	控制器功能选择	0：选择设备控制器1：选 择主机控制器。	R/W
b9 to b7	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b10	SCKE	USB时钟使能	0：停止向USBFS提供时钟1：使能向 USBFS提供时钟。	R/W
b15 to b11	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note: 将1写入SCKE位后，读取它以确认其设置为1。

USBE位（USBFS操作使能）

USBE位启用或禁用USBFS的操作。

将USBE位从1更改为0会初始化表32.3中列出的位。仅在SCKE位为1时更改该位。在主机控制器模式下，必须在将DRPD位设置为1后将该位设置为1，消除SYSSTS0.LNST[1:0]标志抖动，并确认USB总线状态是稳定的。

Table 32.3 通过向SYSCFG.USBE位写入0来初始化寄存器

所选功能	Register	Bit	Remarks
设备控制器	SYSSTS0	LNST[1:0]	值以主机控制器模式保存
	DVSTCTR0	RHST[2:0]	-
	INTSTS0	DVSQ[2:0]	值以主机控制器模式保存
	USBADDR	USBADDR[6:0]	值以主机控制器模式保存
	USBREQ	BREQUEST[7:0], BMREQUESTTYPE[7:0]	值以主机控制器模式保存
	USBVAL	WVALUE[15:0]	值以主机控制器模式保存
	USBINDX	WINDEX[15:0]	值以主机控制器模式保存
	USBLENG	WLENTUH[15:0]	值以主机控制器模式保存
主机控制器	DVSTCTR0	RHST[2:0]	-
	FRMNUM	FRNM[10:0]	值保存在设备控制器模式中

DPRPU位（D+线路电阻控制）

DPRPU位启用或禁用在设备控制器模式下上拉D+线。

当DPRPU位在设备控制器模式下设置为1时，USBFS将D+线上拉以通知USB主机它

attached. Changing the DPRPU bit from 1 to 0 releases the pull-up, thereby notifying the USB host that it detached.

Set this bit to 1 in device controller mode and to 0 in host controller mode.

DRPD bit (D+/D- Line Resistor Control)

The DRPD bit enables or disables pulling down D+ and D- lines in host controller mode.

Set this bit to 1 in host controller mode and to 0 in device controller mode.

DCFM bit (Controller Function Select)

The DCFM bit selects the host or device function of the USBFS.

Only change this bit when the DPRPU and DRPD bits are both 0.

SCKE bit (USB Clock Enable)

The SCKE bit stops or enables the 48-MHz clock supply to the USBFS.

When this bit is 0, only SYSCFG is permitted to be read from and written to; the other registers related to the USB should not be read from or written to.

32.2.2 System Configuration Status Register 0 (SYSSTS0)

Address(es): USBFS.SYSSTS0 4009 0004h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	OVCMON[1:0]		—	—	—	—	—	—	—	HTACT	SOFEA	—	—	IDMON	LNST[1:0]	
Value after reset:	0*1	0*1	0	0	0	0	0	0	0	0	0	0	0	0*1	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	LNST[1:0]	USB Data Line Status Monitor	Indicates the status of the USB data lines, see Table 32.4	R
b2	IDMON	External ID0 Input Pin Monitor	0: USB_ID pin is low 1: USB_ID pin is high.	R
b4, b3	—	Reserved	These bits are read as 0 and cannot be modified.	R
b5	SOFEA	Active Monitor When the Host Controller Is Selected	0: SOF output stopped 1: SOF output operating.	R
b6	HTACT	USB Host Sequencer Status Monitor	0: Host sequencer completely stopped 1: Host sequencer not completely stopped.	R
b13 to b7	—	Reserved	These bits are read as 0 and cannot be changed.	R
b15, b14	OVCMON[1:0]	External USB_OVRCURA/ USB_OVRCURB Input Pin Monitor	OVCMON[1] indicates the USB_OVRCURA pin status. OVCMON[0] indicates the USB_OVRCURB pin status.	R

Note 1. Depends on the status of the USB_OVRCURA, USB_OVRCURB, and USB_ID pins.

LNST[1:0] bits (USB Data Line Status Monitor)

The LNST[1:0] bits indicate the state of the USB data lines, D+ and D-. For details, see Table 32.4.

In device controller mode, read the LNST[1:0] bits after connection processing (SYSCFG.DPRPU bit = 1). In host controller mode, read them after enabling pull-down of the lines (SYSCFG.DRPD bit = 1).

Table 32.4 Status of the USB data bus lines (D+ and D-) (1 of 2)

LNST[1:0] bits	During full-speed operation	During low-speed operation
00b	SE0	SE0
01b	J-State	K-State
10b	K-State	J-State

随附的。将DPRPU位从1更改为0会释放上拉电阻，从而通知USB主机它已分离。

在设备控制器模式下将此位设置为1，在主机控制器模式下设置为0。

DRPD位（D+DLine电阻控制）

DRPD位在主机控制器模式下启用或禁用下拉D+和Dlines。

在主机控制器模式下将此位设置为1，在设备控制器模式下设置为0。

DCFM位（控制器功能选择）

DCFM位选择USBFS的主机或设备功能。

仅当DPRPU和DRPD位都为0时更改该位。

SCKE位（USB时钟使能）

SCKE位停止或启用向USBFS提供48MHz时钟。

该位为0时，只允许读写SYSCFG；不应读取或写入与USB相关的其他寄存器。

32.2.2 系统配置状态寄存器0(SYSSTS0)

Address(es): USBFS.SYSSTS0 4009 0004h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	OVCMON[1:0]		—	—	—	—	—	—	—	HTACT	SOFEA	—	—	IDMON	LNST[1:0]	
重置后的值：	0*1	0*1	0	0	0	0	0	0	0	0	0	0	0	0*1	0	0

Bit	Symbol	位名称	Description	R/W
b1, b0	LNST[1:0]	USB数据线状态监视器	指示USB数据线的状态，见表32.4	R
b2	IDMON	外部ID0输入引脚监视器	0：USB_ID引脚为低电平1： USB_ID引脚为高电平。	R
b4, b3	—	Reserved	这些位被读取为0并且不能被修改。	R
b5	SOFEA	主机时主动监控 选择控制器	0：SOF输出停止1：SOF 输出工作。	R
b6	HTACT	USB主机定序器状态 Monitor	0：主机定序器完全停止1：主机定序器未 完全停止。	R
b13 to b7	—	Reserved	这些位被读取为0并且不能更改。	R
b15, b14	OVCMON[1:0]	外部USB_OVRCURAUSB_O VRCURB输入引脚 Monitor	OVCMON[1]指示USB_OVRCURA引脚状态。OVCMON[0]指示USB_OVRCURB引脚状态。	R

Note 1. 取决于USB_OVRCURA、USB_OVRCURB和USB_ID引脚的状态。

LNST[1:0]位（USB数据线状态监视器）

LNST[1:0]位指示USB数据线D+和D−的状态。详见表32.4。

在设备控制器模式下，在连接处理后读取LNST[1:0]位（SYSCFG.DPRPU位=1）。在主机控制器模式下，在启用线路下拉后读取它们（SYSCFG.DRPD位=1）。

Table 32.4 USB数据总线的状态（D+和D−）（1of2）

LNST[1:0] bits	全速运行期间	低速运转时
00b	SE0	SE0
01b	J-State	K-State
10b	K-State	J-State

Table 32.4 Status of the USB data bus lines (D+ and D-) (2 of 2)

LNST[1:0] bits	During full-speed operation	During low-speed operation
11b	SE1	SE1

SOFEA bit (Active Monitor When the Host Controller Is Selected)

The SOFEA bit is used in host controller mode to check whether the output of the last SOF is complete when the USBFS is suspended because of a 0 setting to the DVSTCTR0.UACT bit.

In host controller mode, check that both the HTACT and SOFEA bits are 0 before setting the SYSCFG.USBE bit to 0 to stop the USBFS or setting the SYSCFG.SCKE bit to 0 to stop the clock signal supply during communication.

HTACT bit (USB Host Sequencer Status Monitor)

The HTACT bit is set to 0 when the host sequencer of the USBFS is completely stopped.

In host controller mode, check that the HTACT bit is 0 before setting the DVSTCTR0.UACT bit to 0 to place the USBFS in the suspended state or setting the SCKE bit to 0 to stop the clock signal supply during communication.

OVCMON[1:0] bits (External USB_OVRCURA/ USB_OVRCURB Input Pin Monitor)

The OVCMON[1:0] bits indicate the status of the overcurrent signals from an external power supply IC.

32.2.3 Device State Control Register 0 (DVSTCTR0)

Address(es): USBFS.DVSTCTR0 4009 0008h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	HNPBTOA	EXICEN	VBUSEN	WKUP	RWUPE	USBRST	RESUME	UACT	—	RHST[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	RHST[2:0]	USB Bus Reset Status	• In host controller mode: b2 b0 0 0 0:Communication speed indeterminate (powered state or no connection) 1 x x:USB bus reset in progress 0 0 1:Low-speed connection 0 1 0:Full-speed connection. • In device controller mode b2 b0 0 0 0: Communication speed indeterminate 0 0 1: USB bus reset in progress 0 1 0: USB bus reset in progress or full-speed connection.	R
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	UACT	USB Bus Enable	0: Disable downstream port (disable SOF transmission) 1: Enable downstream port (enable SOF transmission).	R/W
b5	RESUME	Resume Output	0: Do not output resume signal 1: Output resume signal.	R/W
b6	USBRST	USB Bus Reset Output	0: Do not output USB bus reset signal 1: Output USB bus reset signal.	R/W
b7	RWUPE	Wakeup Detection Enable	0: Disable downstream port remote wakeup 1: Enable downstream port remote wakeup.	R/W
b8	WKUP	Wakeup Output	0: Do not output remote wakeup signal 1: Output remote wakeup signal.	R/W
b9	VBUSEN	USB_VBUSEN Output Pin Control	0: Output low on external USB_VBUSEN pin 1: Output high on external USB_VBUSEN pin.	R/W
b10	EXICEN	USB_EXICEN Output Pin Control	0: Output low on external USB_EXICEN pin 1: Output high on external USB_EXICEN pin.	R/W

Table 32.4 USB数据总线的状态（D+和D−）（2之2）

LNST[1:0] bits	全速运行期间	低速运转时
11b	SE1	SE1

SOFEA位（选择主机控制器时的主动监视器）

SOFEA位在主机控制器模式下用于检查当USBFS因为DVSTCTR0.UACT位设置为0而暂停时最后一个SOF的输出是否完成。

在主机控制器模式下，在将SYSCFG.USBE位设置为0以停止USBFS或将SYSCFG.SCKE位设置为0以在通信期间停止时钟信号供应之前，请检查HTACT和SOFEA位是否都为0。

HTACT位（USB主机定序器状态监视器）

当USBFS的主机定序器完全停止时，HTACT位设置为0。

在主机控制器模式下，在将DVSTCTR0.UACT位设置为0以将USBFS置于挂起状态或将SCKE位设置为0以在通信期间停止时钟信号供应之前，请检查HTACT位是否为0。

OVCMON[1:0]位（外部USB_OVRCURAUSB_OVRCURB输入引脚监视器）

OVCMON[1:0]位指示来自外部电源IC的过流信号的状态。

32.2.3 设备状态控制寄存器0(DVSTCTR0)

Address(es): USBFS.DVSTCTR0 4009 0008h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	HNPBTOA	EXICEN	VBUSEN	WKUP	RWUPE	USBRST	RESUME	UACT	—	RHST[2:0]		
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b2 to b0	RHST[2:0]	USB总线复位状态	在主机控制器模式下：b2b0000：通信速度不确定（通电状态或无连接）1xx：USB总线复位正在进行中001：低速连接010：全速连接。 在设备控制器模式下b2b0000：通信速度不确定001：USB总线复位正在进行中010：USB总线复位正在进行或全速连接。	R
b3	—	Reserved	该位读取为0。写入值应为0。	R/W
b4	UACT	USB总线启用	0：禁用下行端口（禁用SOF传输）1：启用下行端口（启用SOF传输）。	R/W
b5	RESUME	恢复输出	0：不输出恢复信号1：输出恢复信号。	R/W
b6	USBRST	USB总线复位输出	0：不输出USB总线复位信号1：输出USB总线复位信号。	R/W
b7	RWUPE	唤醒检测启用	0：禁用下游端口远程唤醒1：启用下游端口远程唤醒。	R/W
b8	WKUP	唤醒输出	0：不输出远程唤醒信号1：输出远程唤醒信号。	R/W
b9	VBUSEN	USB_VBUSEN输出引脚控制	0：外部USB_VBUSEN引脚输出低电平1：外部USB_VBUSEN引脚输出高电平。	R/W
b10	EXICEN	USB_EXICEN输出引脚控制	0：外部USB_EXICEN引脚输出低电平1：外部USB_EXICEN引脚输出高电平。	R/W

Bit	Symbol	Bit name	Description	R/W
b11	HNPBTOA	Host Negotiation Protocol (HNP) Control	Use this bit when switching from device B to device A in OTG mode. If the HNPBTOA bit is 1, the internal function control remains in the Suspend state until the HNP processing ends even if SYSCFG.DPRPU = 0 or SYSCFG.DCFM = 1.	R/W
b15 to b12	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

x: Don't care

The USBFS controller does not support low-speed connections in device controller mode. When this value is read, abnormal connection processing must be executed in higher level application software.

RHST[2:0] bits (USB Bus Reset Status)

The RHST[2:0] bits indicate the status of the USB bus reset.

In host controller mode, writing 1 to the USBRST bit causes the RHST[2:0] bits to set to 100b. When 0 is written to the USBRST bit and the USBFS ends the SE0 state, the RHST[2:0] bits update to a new value.

In device controller mode, if the USBFS detects a USB bus reset, the RHST[2:0] bits indicate 010b if the DPRPU bit is 1, and a DVST interrupt is generated.

UACT bit (USB Bus Enable)

When set to 1 in host controller mode, the UACT bit enables USB bus operation by controlling SOF packet transmission to the USB bus in addition to data and reception. The USBFS starts SOF packet output within one frame period after the UACT bit is set to 1. When UACT is set to 0, the USBFS enters the idle state after the SOF packet output.

The USBFS sets the UACT bit to 0 on any of the following conditions:

- A DTCH interrupt is detected during communication (when UACT = 1)
- An EOFERR interrupt is detected during communication (when UACT = 1).

Always write 1 to the UACT bit at the end of the USB bus reset processing (writing 0 to the USBRST bit) or at the end of resume processing from the suspended state (writing 0 to the RESUME bit).

In device controller mode, always set this bit to 0.

RESUME bit (Resume Output)

The RESUME bit controls the resume signal output in host controller mode.

When this bit is set to 1, the USBFS drives the USB port to the K-state and outputs the resume signal. The USBFS sets the bit to 1 on detection of a remote wakeup signal while the RWUPE bit is 1 and in the USB Suspend state.

The USBFS continues outputting the K-state while the RESUME bit is 1, until the bit is cleared to 0 by software. The RESUME bit must be 1 (resume period) for the time defined in the USB 2.0 specification. Only set this bit to 1 while the interface is in the Suspend state. Write 1 to the UACT bit simultaneously with the end of the resume processing (writing 0 to the RESUME bit).

Always set this bit to 0 in device controller mode.

USBRST bit (USB Bus Reset Output)

The USBRST bit controls the output of the USB bus signal in host controller mode. When this bit set to 1, the USBFS drives the USB port to the SE0 state to reset the USB bus. The USBFS continues outputting SE0 while the USBRST bit is 1, until the bit is cleared to 0 by software. The USBRST bit must be 1 (USB bus reset period) for the time defined in the USB 2.0 specification. Writing 1 to the USBRST bit during communication (UACT bit = 1) or during resume processing (RESUME bit = 1) prevents the USBFS from starting USB bus reset processing until both the UACT and RESUME bits become 0. Write 1 to the UACT bit simultaneously with the end of the USB bus reset processing (writing 0 to the USBRST bit).

Always set this bit to 0 in device controller mode.

Bit	Symbol	位名称	Description	R/W
b11	HNPBTOA	主机协商协议(HNP) Control	在OTG模式下从设备B切换到设备A时使用该位。如果HNPBTOA位为1，即使SYSCFG.DPRPU=0或SYSCFG.DCFM=1，内部功能控制仍保持暂停状态直到HNP处理结束。	R/W
b15 to b12	—	Reserved	这些位被读取为0。写入值应为0。	R/W

x: Don't care

USBFS控制器不支持设备控制器模式下的低速连接。当读取此值时，必须在更高级别的应用软件中执行异常连接处理。

RHST[2:0]位（USB总线复位状态）

RHST[2:0]位指示USB总线复位的状态。

在主机控制器模式下，将1写入USBRST位会导致RHST[2:0]位设置为100b。当0被写入USBRST位和USBFS结束SE0状态，RHST[2:0]位更新为新值。

在设备控制器模式下，如果USBFS检测到USB总线复位，如果DPRPU位为1，则RHST[2:0]位指示010b，并产生DVST中断。

UACT位（USB总线使能）

在主机控制器模式下设置为1时，UACT位通过控制向USB总线发送SOF数据包以及数据和接收来启用USB总线操作。USBFS在UACT位设置为1后的一帧周期内开始SOF数据包输出。当UACT设置为0时，USBFS在SOF数据包输出后进入空闲状态。

USBFS在以下任何条件下将UACT位设置为0：

- 在通信期间检测到DTCH中断（当UACT=1时）
- 通信期间检测到EOFERR中断（当UACT=1时）。

在USB总线复位处理结束（将0写入USBRST位）或从挂起状态恢复处理结束（将0写入RESUME位）时，始终向UACT位写入1。

在设备控制器模式下，始终将此位设置为0。

RESUME位（恢复输出）

RESUME位控制主机控制器模式下的恢复信号输出。

当该位设置为1时，USBFS将USB端口驱动到K状态并输出恢复信号。当RWUPE位为1且处于USB挂起状态时，USBFS在检测到远程唤醒信号时将该位设置为1。

当RESUME位为1时，USBFS继续输出K状态，直到该位被软件清除为0。这在USB2.0规范中定义的时间内，RESUME位必须为1（恢复周期）。仅当接口处于挂起状态时将此位设置为1。在恢复处理结束的同时向UACT位写入1（向RESUME位写入0）。

在设备控制器模式下始终将此位设置为0。

USBRST位（USB总线复位输出）

USBRST位控制主机控制器模式下USB总线信号的输出。当该位设置为1时，USBFS将USB端口驱动到SE0状态以复位USB总线。当USBRST位为1时，USBFS继续输出SE0，直到该位被软件清零。在USB2.0规范中定义的时间内，USBRST位必须为1（USB总线复位周期）。在通信期间（UACT位=1）或恢复处理期间（RESUME位=1）向USBRST位写入1可防止USBFS开始USB总线复位处理，直到UACT和RESUME位都变为0。同时向UACT位写入1随着USB总线复位处理的结束（向USBRST位写入0）。

在设备控制器模式下始终将此位设置为0。

RWUPE bit (Wakeup Detection Enable)

The RWUPE bit enables or disables remote wakeup signals (resume signals) from downstream peripheral devices in host controller mode. When this bit is set to 1, the USBFS detects a remote wakeup signal (K-state for 2.5 µs) from a downstream peripheral device, and performs resume processing, driving the K-state. When the RWUPE bit is set to 0, the USBFS ignores remote wakeup signals (K-states) from peripheral devices connected to the USB port.

Do not stop the internal clock when the RWUPE bit is 1, even in the Suspend state (SYSCFG.SCKE bit must be set to 1).

Always set this bit to 0 in device controller mode.

WKUP bit (Wakeup Output)

The WKUP bit enables or disables remote wakeup signals (resume signals) to the USB bus in device controller mode.

The USBFS controls the output timing of the remote wakeup signals. When this bit is set to 1, the USBFS clears it to 0 after outputting the K-state for 10 ms. The USB 2.0 specification specifies that the USB bus idle state must be kept for 5 ms or longer before a remote wakeup signal is sent. If the USBFS writes 1 to the WKUP bit immediately after detecting the Suspend state, the K-state is output after 2 ms.

Only write 1 to the WKUP bit when the device is in the Suspend state (INTSTS0.DVSQ[2:0] bits = 1xxb) and the USB host enables the remote wakeup signal (RWUPE = 1). Do not stop the internal clock while this bit is 1, even in the Suspend state (SYSCFG.SCKE bit must be set to 1).

Always set this bit to 0 in host controller mode.

HNPBTOA bit (Host Negotiation Protocol (HNP) Control)

The HNPBTOA bit is used when switching from device B to device A while in OTG mode.

If the HNPBTOA bit is 1, the internal function control maintains the Suspend state until HNP processing ends, even if the SYSCFG.DPRPU bit is set to 0 or the SYSCFG.DCFM bit is set to 1. Resume interrupts (RESM) are not generated even if a falling edge of D+ is detected.

The HNP processing ends when a host attach event is detected, because of a pull-up by the initiating party, or the HNPBTOA bit is cleared to 0 by software because the HNP processing times out.

32.2.4 CFIFO Port Register (CFIFO/CFIFOL)
D0FIFO Port Register (D0FIFO/D0FIFOL)
D1FIFO Port Register (D1FIFO/D1FIFOL)

(1) When the MBW bit is 1

Address(es): USBFS.CFIFO 4009 0014h, USBFS.D0FIFO 4009 0018h, USBFS.D1FIFO 4009 001Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	FIFOPORT[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(2) When the MBW bit is 0

Address(es): USBFS.CFIFOL 4009 0014h, USBFS.D0FIFOL 4009 0018h, USBFS.D1FIFOL 4009 001Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	FIFOPORT[15:0]							
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b15 to b0	FIFOPORT[15:0]*1	FIFO Port	Read receive data from the FIFO buffer or write transmit data to the FIFO buffer by accessing these bits	R/W

RUPE位（唤醒检测使能）

在主机控制器模式下，RWUPE位启用或禁用来自下游外围设备的远程唤醒信号（恢复信号）。当该位设置为1时，USBFS检测到来自下游外围设备的远程唤醒信号（K状态持续2.5µs），并执行恢复处理，驱动K状态。当RHUPE位设置为0时，USBFS忽略来自连接到USB端口的外围设备的远程唤醒信号（K状态）。

当RHUPE位为1时不要停止内部时钟，即使处于挂起状态（SYSCFG.SCKE位必须设置为1）。

在设备控制器模式下始终将此位设置为0。

WKUP位（唤醒输出）

WKUP位在设备控制器模式下启用或禁用到USB总线的远程唤醒信号（恢复信号）。

USBFS控制远程唤醒信号的输出时序。当该位设置为1时，USBFS在输出K状态10ms后将其清除为0。USB2.0规范规定，在发送远程唤醒信号之前，USB总线空闲状态必须保持5ms或更长时间。如果USBFS在检测到Suspend状态后立即向WKUP位写入1，则在2ms后输出K-state。

仅当设备处于挂起状态（INTSTS0.DVSQ[2:0]位=1xxb）且USB主机使能远程唤醒信号（RWUPE=1）时，向WKUP位写入1。当该位为1时不要停止内部时钟，即使处于挂起状态（SYSCFG.SCKE位必须设置为1）。

在主机控制器模式下始终将此位设置为0。

HNPBTOA位（主机协商协议(HNP)控制）

在OTG模式下从设备B切换到设备A时使用HNPBTOA位。

如果HNPBTOA位为1，内部功能控制保持暂停状态直到HNP处理结束，即使SYSCFG.DPRPU位设置为0或SYSCFG.DCFM位设置为1。不产生恢复中断(RESM)即使检测到D+的下降沿。

当检测到主机连接事件时，HNP处理结束，因为发起方的上拉，或者由于HNP处理超时，HNPBTOA位由软件清零。

32.2.4 CFIFO端口寄存器(CFIFOCFIFOL)
D0FIFO端口寄存器(D0FIFOD0FIFOL)D1FIFO端口寄存器(D1FIFOD1FIFOL)

(1)MBW位为1时

Address(es): USBFS.CFIFO 4009 0014h, USBFS.D0FIFO 4009 0018h, USBFS.D1FIFO 4009 001Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	FIFOPORT[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

(2)MBW位为0时

Address(es): USBFS.CFIFOL 4009 0014h, USBFS.D0FIFOL 4009 0018h, USBFS.D1FIFOL 4009 001Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	FIFOPORT[15:0]							
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b15 to b0	FIFOPORT[15:0]*1	FIFO Port	通过访问这些位从FIFO缓冲区读取接收数据或将发送数据写入FIFO缓冲区	R/W

Note 1. The valid bits depend on the MBW settings (CFIFOSEL.MBW, D0FIFOSEL.MBW, and D1FIFOSEL.MBW) and BIGEND settings (CFIFOSEL.BIGEND, D0FIFOSEL.BIGEND, and D1FIFOSEL.BIGEND) in the associated port select register. See Table 32.5 and Table 32.6.

Three FIFO ports are available:

- CFIFO
- D0FIFO
- D1FIFO.

Each FIFO port is configured with:

- A port register (CFIFO, D0FIFO, or D1FIFO) that handles reading of data from the FIFO buffer and writing of data to the FIFO buffer
- A port select register (CFIFOSEL, D0FIFOSEL, or D1FIFOSEL) that selects the pipe assigned to the FIFO port
- A port control register (CFIFOCTR, D0FIFOCTR, or D1FIFOCTR).

Each FIFO port has the following constraints:

- Access to the FIFO buffer for DCP control transfers is through the CFIFO port
- Access to the FIFO buffer for DMA or DTC transfers is through the D0FIO or D1FIFO port
- The D0FIFO and D1FIFO ports can also be accessed by the CPU
- When using functions specific to the FIFO port, such as the DMA or DTC transfer function, you cannot change the pipe number selected in the CURPIPE[3:0] bits of the port select register
- Registers configuring a FIFO port do not affect other FIFO ports
- The same pipe must not be assigned to two or more FIFO ports
- There are two FIFO buffer states, one giving access rights to the CPU and the other to the serial interface engine (SIE). When the SIE has access rights, the FIFO buffer cannot be accessed by the CPU.

FIFOPORT[15:0] bits (FIFO Port)

When the FIFOPORT bit is accessed, the USBFS reads the received data from the FIFO buffer or writes the transmit data to the FIFO buffer. The FIFO port register can be accessed only when the FRDY bit in the associated port control register (CFIFOCTR, D0FIFOCTR, or D1FIFOCTR) is 1.

The valid bits in the FIFO port register depend on the MBW and BIGEND settings in the port select register (CFIFOSEL, D0FIFOSEL, or D1FIFOSEL). See Table 32.5 and Table 32.6.

Table 32.5 Endian operation in 16-bit access

CFIFOSEL.BIGEND bit D0FIFOSEL.BIGEND bit D1FIFOSEL.BIGEND bit	Bits [15:8]	Bits [7:0]
0	N + 1 data	N + 0 data
1	N + 0 data	N + 1 data

Table 32.6 Endian operation in 8-bit access

CFIFOSEL.BIGEND bit D0FIFOSEL.BIGEND bit D1FIFOSEL.BIGEND bit	Bits [15:8]	Bits [7:0]
0	Access prohibited*1	N + 0 data
1	Access prohibited*1	N + 0 data

Note 1. Writing to or reading from these areas is not allowed.

Note 1. 有效位取决于相关端口选择寄存器中的MBW设置（CFIFOSEL.MBW、D0FIFOSEL.MBW和D1FIFOSEL.MBW）和BIGEND设置（CFIFOSEL.BIGEND、D0FIFOSEL.BIGEND和D1FIFOSEL.BIGEND）。请参见表32.5和表32.6。

三个FIFO端口可用：

- CFIFO
- D0FIFO
- D1FIFO.

每个FIFO端口配置有：

- 处理从FIFO缓冲区读取数据和将数据写入FIFO缓冲区的端口寄存器（CFIFO、D0FIFO或D1FIFO）
- 选择分配给FIFO端口的管道的端口选择寄存器（CFIFOSEL、D0FIFOSEL或D1FIFOSEL）
- 端口控制寄存器（CFIFOCTR、D0FIFOCTR或D1FIFOCTR）。

每个FIFO端口具有以下约束：

- 通过CFIFO端口访问DCP控制传输的FIFO缓冲区
- 通过D0FIO或D1FIFO端口访问DMA或DTC传输的FIFO缓冲区
- CPU也可以访问D0FIFO和D1FIFO端口
- 当使用特定于FIFO端口的功能时，例如DMA或DTC传输功能，您无法更改在端口选择寄存器的CURPIPE[3:0]位中选择的管道编号
- 配置FIFO端口的寄存器不会影响其他FIFO端口
- 不得将同一管道分配给两个或多个FIFO端口
- 有两种FIFO缓冲区状态，一种授予CPU访问权限，另一种授予串行接口引擎(SIE)。当SIE有访问权限时，CPU不能访问FIFO缓冲区。

FIFOPORT[15:0]位（FIFO端口）

当访问FIFOPORT位时，USBFS从FIFO缓冲区读取接收数据或将发送数据写入FIFO缓冲区。只有当相关端口控制寄存器（CFIFOCTR、D0FIFOCTR或D1FIFOCTR）中的FRDY位为1时，才能访问FIFO端口寄存器。

FIFO端口寄存器中的有效位取决于端口选择寄存器（CFIFOSEL、D0FIFOSEL或D1FIFOSEL）中的MBW和BIGEND设置。请参见表32.5和表32.6。

Table 32.5 16位访问中的字节序操作

CFIFOSEL.BIGEND bit D0FIFOSEL.BIGEND bit D1FIFOSEL.BIGEND bit	Bits [15:8]	Bits [7:0]
0	N + 1 data	N + 0 data
1	N + 0 data	N + 1 data

Table 32.6 8位访问中的字节序操作

CFIFOSEL.BIGEND bit D0FIFOSEL.BIGEND bit D1FIFOSEL.BIGEND bit	Bits [15:8]	Bits [7:0]
0	禁止访问*1	N + 0 data
1	禁止访问*1	N + 0 data

Note 1. 不允许对这些区域进行写入或读取。

32.2.5 CFIFO Port Select Register (CFIFOSEL) D0FIFO Port Select Register (D0FIFOSEL) D1FIFO Port Select Register (D1FIFOSEL)

CFIFOSEL

Address(es): USBFS.CFIFOSEL 4009 0020h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RCNT	REW	—	—	—	MBW	—	BIGEND	—	—	ISEL	—	CURPIPE[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	CURPIPE[3:0]	CFIFO Port Access Pipe Specification	b3 b0 0 0 0 0: DCP (Default Control Pipe) 0 0 0 1: Pipe 1 0 0 1 0: Pipe 2 0 0 1 1: Pipe 3 0 1 0 0: Pipe 4 0 1 0 1: Pipe 5 0 1 1 0: Pipe 6 0 1 1 1: Pipe 7 1 0 0 0: Pipe 8 1 0 0 1: Pipe 9. Other settings are prohibited.	R/W
b4	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b5	ISEL	CFIFO Port Access Direction When DCP Is Selected	0: Select reading from the FIFO buffer 1: Select writing to the FIFO buffer.	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	BIGEND	CFIFO Port Endian Control	0: Little endian 1: Big endian.	R/W
b9	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b10	MBW	CFIFO Port Access Bit Width	0: 8-bit width 1: 16-bit width.	R/W
b13 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b14	REW	Buffer Pointer Rewind	0: Do not rewind buffer pointer 1: Rewind buffer pointer.	W*1
b15	RCNT	Read Count Mode	0: The DTLN[8:0] bits (CFIFOCTR.DTLN[8:0], D0FIFOCTR.DTLN[8:0], D1FIFOCTR.DTLN[8:0]) are cleared when all receive data is read from the CFIFO. In double buffer mode, the DTLN[8:0] value is cleared when all data is read from only a single plane. 1: The DTLN[8:0] bits are decremented each time the receive data is read from the CFIFO.	R/W

Note 1. Only 0 can be read.

Do not specify the same pipe number in the CURPIPE[3:0] bits in the CFIFOSEL, D0FIFOSEL, and D1FIFOSEL registers. When the CURPIPE[3:0] bits in the D0FIFOSEL and D1FIFOSEL registers are set to 0000b, no pipe is selected.

Do not change the pipe number while DMA or DTC transfer is enabled.

CURPIPE[3:0] bits (CFIFO Port Access Pipe Specification)

The CURPIPE[3:0] bits specify the pipe number to use for reading or writing data through the CFIFO port. After writing to these bits, read them to check that the written value agrees with the read value before proceeding to the next process. Do not set the same pipe number to the CURPIPE[3:0] bits in CFIFOSEL, D0FIFOSEL, and D1FIFOSEL.

32.2.5 CFIFO端口选择寄存器(CFIFOSEL) D0FIFO端口选择寄存器(D0FIFOSEL)D1FIFO端口选择寄存器(D1FIFOSEL)

CFIFOSEL

Address(es): USBFS.CFIFOSEL 4009 0020h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RCNT	REW	—	—	—	MBW	—	BIGEND	—	—	ISEL	—	CURPIPE[3:0]			
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b3 to b0	CURPIPE[3:0]	CFIFO端口访问管道规范	b3b00000：DCP（默认控制管道） 0001：管道10010：管道20011：管道30100：管道40101：管道50110：管道60111：管道71000：管道81001：管道9。禁止其他设置。	R/W
b4	—	Reserved	该位读取为0。写入值应为0。	R/W
b5	ISEL	CFIFO端口访问方向何时已选择DCP	0：选择从FIFO缓冲区读取1：选择写入FIFO缓冲区。	R/W
b7, b6	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b8	BIGEND	CFIFO端口字节序控制	0：小端1：大端。	R/W
b9	—	Reserved	该位读取为0。写入值应为0。	R/W
b10	MBW	CFIFO端口访问位宽	0: 8-bit width 1: 16-bit width.	R/W
b13 to b11	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b14	REW	缓冲区指针倒带	0：不倒回缓冲区指针1：倒回缓冲区指针。	W*1
b15	RCNT	读取计数模式	0：DTLN[8:0]位（CFIFOCTR.DTLN[8:0]，当从CFIFO读取所有接收数据时，D0FIFOCTR.DTLN[8:0]、D1FIFOCTR.DTLN[8:0])被清除。在双缓冲模式下，当仅从单个平面读取所有数据时，清除DTLN[8:0]值。1：每次从CFIFO读取接收数据时，DTLN[8:0]位递减。	R/W

Note 1. 只能读取0。

不要在CFIFOSEL、D0FIFOSEL和D1FIFOSEL寄存器的CURPIPE[3:0]位中指定相同的管道编号。当D0FIFOSEL和D1FIFOSEL寄存器中的CURPIPE[3:0]位设置为0000b时，不选择管道。

启用DMA或DTC传输时不要更改管道编号。

CURPIPE[3:0]位（CFIFO端口访问管道规范）

CURPIPE[3:0]位指定用于通过CFIFO端口读取或写入数据的管道编号。写入这些位后，读取它们以检查写入的值是否与读取的值一致，然后再进行下一个过程。不要为CFIFOSEL、D0FIFOSEL和D1FIFOSEL中的CURPIPE[3:0]位设置相同的管道编号。

During FIFO buffer access, even when an attempt is made to change the CURPIPE[3:0] setting, the current access setting is retained until access is complete.

ISEL bit (CFIFO Port Access Direction When DCP Is Selected)

After writing a new value to the ISEL bit with the DCP as the selected pipe, read the ISEL bit to check that the written value agrees with the read value before proceeding to the next process. Set the ISEL and CURPIPE[3:0] bits simultaneously.

MBW bit (CFIFO Port Access Bit Width)

The MBW bit specifies the bit width for accessing the CFIFO port.

When the selected pipe is receiving, set the CURPIPE[3:0] and MBW bits simultaneously. After a write to these bits starts a data read from the FIFO buffer, do not change the bits until all of the data is read. When reading the FIFO buffer, read with the access size set in MBW.

When the selected pipe is transmitting, the bit width cannot be changed from 8-bit to 16-bit while data is being written to the FIFO buffer.

An odd number of bytes can also be written through byte-access control even when 16-bit width is selected.

REW bit (Buffer Pointer Rewind)

The REW bit specifies whether to rewind the buffer pointer.

When the selected pipe is receiving, setting this bit to 1 while the FIFO buffer is being read allows re-reading of the FIFO buffer from the first data. In double buffering, this setting enables re-reading of the currently-read FIFO buffer plane from the first entry.

Do not set this bit to 1 while simultaneously changing the CURPIPE[3:0] bits. Before setting the REW bit to 1, be sure to check that the FRDY bit is 1.

To rewrite to the FIFO buffer from the first data for the transmitting pipe, use the BCLR bit.

D0FIFOSEL, D1FIFOSEL

Address(es): USBFS.D0FIFOSEL 4009 0028h, USBFS.D1FIFOSEL 4009 002Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RCNT	REW	DCLRM	DREQE	—	MBW	—	BIGEND	—	—	—	—	CURPIPE[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	CURPIPE[3:0]	FIFO Port Access Pipe Specification	b3 b0 0 0 0 0: No pipe specification 0 0 0 1: Pipe 1 0 0 1 0: Pipe 2 0 0 1 1: Pipe 3 0 1 0 0: Pipe 4 0 1 0 1: Pipe 5 0 1 1 0: Pipe 6 0 1 1 1: Pipe 7 1 0 0 0: Pipe 8 1 0 0 1: Pipe 9. Other settings are prohibited.	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	BIGEND	FIFO Port Endian Control	0: Little endian 1: Big endian.	R/W
b9	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b10	MBW	FIFO Port Access Bit Width	0: 8-bit width 1: 16-bit width.	R/W

在FIFO缓冲区访问期间，即使尝试更改CURPIPE[3:0]设置，当前访问设置也会保留，直到访问完成。

ISEL位（选择DCP时的CFIFO端口访问方向）

在以DCP作为选定管道的情况下将新值写入ISEL位后，读取ISEL位以检查写入的值是否与读取的值一致，然后再进行下一个过程。同时设置ISEL和CURPIPE[3:0]位。

MBW位（CFIFO端口访问位宽度）

MBW位指定访问CFIFO端口的位宽。

当所选管道正在接收时，同时设置CURPIPE[3:0]和MBW位。在写入这些位开始从FIFO缓冲区读取数据后，在读取所有数据之前不要更改这些位。读取FIFO缓冲区时，读取以MBW为单位设置的访问大小。

当所选管道正在传输时，位宽不能从8位更改为16位，同时数据正在写入FIFO缓冲区。

即使选择了16位宽度，也可以通过字节访问控制写入奇数个字节。

REW位（缓冲区指针倒带）

REW位指定是否倒回缓冲区指针。

当所选管道正在接收时，在读取FIFO缓冲区时将此位设置为1允许从第一个数据重新读取FIFO缓冲区。在双缓冲中，此设置允许从第一个条目重新读取当前读取的FIFO缓冲区平面。

请勿在同时更改CURPIPE[3:0]位时将此位设置为1。在将REW位设置为1之前，请务必检查FRDY位是否为1。

要从传输管道的第一个数据重写FIFO缓冲区，请使用BCLR位。

D0FIFOSEL, D1FIFOSEL

Address(es): USBFS.D0FIFOSEL 4009 0028h, USBFS.D1FIFOSEL 4009 002Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RCNT	REW	DCLRM	DREQE	—	MBW	—	BIGEND	—	—	—	—	CURPIPE[3:0]			
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b3 to b0	CURPIPE[3:0]	FIFO端口访问管道 Specification	b3b00000：无管道规格0001：管道10010：管道20011：管道30100：管道40101：管道50110：管道60111：管道71000：管道81001：管道9。禁止其他设置。	R/W
b7 to b4	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b8	BIGEND	FIFO端口字节序控制	0：小端1：大端。	R/W
b9	—	Reserved	该位读取为0。写入值应为0。	R/W
b10	MBW	FIFO端口访问位宽	0: 8-bit width 1: 16-bit width.	R/W

Bit	Symbol	Bit name	Description	R/W
b11	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b12	DREQE	DMA/DTC Transfer Request Enable	0: Disable DMA/DTC transfer request 1: Enable DMA/DTC transfer request.	R/W
b13	DCLRM	Auto Buffer Memory Clear Mode Accessed after Specified Pipe Data is Read	0: Disable auto buffer clear mode 1: Enable auto buffer clear mode.	R/W
b14	REW	Buffer Pointer Rewind	0: Do not rewind buffer pointer 1: Rewind buffer pointer.	R/W*1
b15	RCNT	Read Count Mode	0: Clear DTLN[8:0] bits in (CFIFOCTR.DTLN[8:0], D0FIFOCTR.DTLN[8:0], D1FIFOCTR.DTLN[8:0]) when all receive data is read from DnFIFO (after read of a single plane in double buffer mode) 1: Decrement DTLN[8:0] bits each time receive data is read from DnFIFO. n = 0, 1.	R/W

Note 1. Only 0 can be read.

The same pipe must not be specified in the CURPIPE[3:0] bits in the CFIFOSEL, D0FIFOSEL, and D1FIFOSEL registers. When the CURPIPE[3:0] bits in the D0FIFOSEL and D1FIFOSEL registers are set to 0000b, no pipe is selected. The pipe number must not be changed while DMA or DTC transfer is enabled.

CURPIPE[3:0] bits (FIFO Port Access Pipe Specification)

The CURPIPE[3:0] bits specify the pipe number to use for reading or writing data through the DnFIFO port. After writing to these bits, read them to check that the written value agrees with the read value before proceeding to the next process. Do not set the same pipe number to the CURPIPE[3:0] bits in CFIFOSEL, D0FIFOSEL, and D1FIFOSEL.

During FIFO buffer access, even when an attempt is made to change the CURPIPE[3:0] setting, the current access setting is retained until access is complete.

MBW bit (FIFO Port Access Bit Width)

The MBW bit specifies the bit width for accessing the DnFIFO port.

When the selected pipe is receiving, after a write to these bits starts a data read from the FIFO buffer, do not change the bits until all of the data is read. Set the CURPIPE[3:0] and MBW bits simultaneously. When reading the FIFO buffer, read with the access size set in MBW.

When the selected pipe is transmitting, the bit width cannot be changed from 8-bit to 16-bit while data is being written to the FIFO buffer.

An odd number of bytes can also be written through byte-access control even when 16-bit width is selected.

DREQE bit (DMA/DTC Transfer Request Enable)

The DREQE bit enables or disables issuing of DMA or DTC transfer requests. To enable DMA or DTC transfer requests, set this bit to 1 after setting the CURPIPE[3:0] bits. To change the CURPIPE[3:0] setting, first set this bit to 0.

DCLRM bit (Auto Buffer Memory Clear Mode Accessed after Specified Pipe Data is Read)

The DCLRM bit enables or disables automatic FIFO buffer clearing after data in the selected pipe is read.

When this bit is set to 1, on receiving a zero-length packet while the FIFO buffer assigned to the selected pipe is empty, or when reading of a received short packet is complete while the PIPECFG.BFRE bit is 1, the USBFS sets the BCLR bit in the FIFO port control register to 1.

When using the USBFS with the SOFCFG.BRDYM bit set to 1, set this bit to 0.

REW bit (Buffer Pointer Rewind)

The REW bit specifies whether to rewind the buffer pointer.

When the selected pipe is receiving, setting this bit to 1 while the FIFO buffer is being read allows re-reading of the FIFO buffer from the first data. In double buffering, this setting enables re-reading of the currently-read FIFO buffer plane

Bit	Symbol	位名称	Description	R/W
b11	—	Reserved	该位读取为0。写入值应为0。	R/W
b12	DREQE	DMADTC传输请求 Enable	0：禁用DMADTC传输请求1：启用DMADTC传输请求。	R/W
b13	DCLRM	自动缓冲存储器清除模式后访问 读取指定的管道数据	0：禁用自动缓冲区清除模式1： 启用自动缓冲区清除模式。	R/W
b14	REW	缓冲区指针倒带	0：不倒回缓冲区指针1：倒回 缓冲区指针。	R/W*1
b15	RCNT	读取计数模式	0：清除(CFIFOCTR.DTLN[8:0]中的DTLN[8:0]位， D0FIFOCTR.DTLN[8:0] D1FIFOCTR.DTLN[8:0])当从DnFIFO读取所有接收数据时（在双缓冲模式下读取单个平面后）1：每次递减DTLN[8:0]位接收数据从DnFIFO中读取。n=0 1。	R/W

Note 1. 只能读取0。

不能在CFIFOSEL、D0FIFOSEL和D1FIFOSEL寄存器的CURPIPE[3:0]位中指定相同的管道。当D0FIFOSEL和D1FIFOSEL寄存器中的CURPIPE[3:0]位设置为0000b时，不选择管道。启用DMA或DTC传输时，不得更改管道编号。

CURPIPE[3:0]位（FIFO端口访问管道规范）

CURPIPE[3:0]位指定用于通过DnFIFO端口读取或写入数据的管道编号。写入这些位后，读取它们以检查写入的值是否与读取的值一致，然后再进行下一个过程。不要为CFIFOSEL、D0FIFOSEL和D1FIFOSEL中的CURPIPE[3:0]位设置相同的管道编号。

在FIFO缓冲区访问期间，即使尝试更改CURPIPE[3:0]设置，当前访问设置也会保留，直到访问完成。

MBW位（FIFO端口访问位宽）

MBW位指定访问DnFIFO端口的位宽。

当所选管道正在接收时，在写入这些位后开始从FIFO缓冲区读取数据，在读取所有数据之前不要更改这些位。同时设置CURPIPE[3:0]和MBW位。读取FIFO缓冲区时，读取以MBW为单位设置的访问大小。

当所选管道正在传输时，位宽不能从8位更改为16位，同时数据正在写入FIFO缓冲区。

即使选择了16位宽度，也可以通过字节访问控制写入奇数个字节。

DREQE位（DMADTC传输请求使能）

DREQE位启用或禁用DMA或DTC传输请求的发出。要启用DMA或DTC传输请求，请在设置CURPIPE[3:0]位后将此位设置为1。要更改CURPIPE[3:0]设置，首先将该位设置为0。

DCLRM位（读取指定管道数据后访问的自动缓冲存储器清除模式）

在读取所选管道中的数据后，DCLRM位启用或禁用自动FIFO缓冲区清除。

当该位设置为1时，在分配给所选管道的FIFO缓冲区为空时接收到零长度数据包，或者当PIPECFG.BFRE位为1时完成读取接收到的短数据包时，USBFS设置FIFO端口控制寄存器中的BCLR位为1。

当使用SOFCFG.BRDYM位设置为1的USBFS时，将此位设置为0。

REW位（缓冲区指针倒带）

REW位指定是否倒回缓冲区指针。

当所选管道正在接收时，在读取FIFO缓冲区时将此位设置为1允许从第一个数据重新读取FIFO缓冲区。在双缓冲中，此设置允许重新读取当前读取的FIFO缓冲平面

from the first entry.

Do not set this bit to 1 while simultaneously changing the CURPIPE[3:0] bits. Before setting the bit to 1, be sure to check that the FRDY bit is 1.

To rewrite to the FIFO buffer from the first data for the transmitting pipe, use the BCLR bit.

RCNT bit (Read Count Mode)

The RCNT bit specifies the read mode for the value in the CFIFOCTR.DTLN bit. When accessing DnFIFO with the PIPECFG.BFRE bit set to 1, set the RCNT bit to 0.

32.2.6 CFIFO Port Control Register (CFIFOCTR) D0FIFO Port Control Register (D0FIFOCTR) D1FIFO Port Control Register (D1FIFOCTR)

Address(es): USBFS.CFIFOCTR 4009 0022h, USBFS.D0FIFOCTR 4009 002Ah, USBFS.D1FIFOCTR 4009 002Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BVAL	BCLR	FRDY	—	—	—	—	DTLN[8:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b8 to b0	DTLN[8:0]	Receive Data Length	Indicates the receive data length. The meaning of the values differs depending on the RCNT bit setting in the port select register. For details, see the description of the DTLN[8:0] bits.	R
b12 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b13	FRDY	FIFO Port Ready	0: FIFO port access disabled 1: FIFO port access enabled.	R
b14	BCLR	CPU Buffer Clear	0: No operation 1: Clear FIFO buffer on the CPU side.	R/W*1
b15	BVAL	Buffer Memory Valid Flag	0: Invalid (writing 0 has no effect) 1: Writing ended.	R/W

Note 1. Only 0 can be read.

The CFIFOCTR, D0FIFOCTR, and D1FIFOCTR registers correspond to the CFIFO, D0FIFO, and D1FIFO buffers.

DTLN[8:0] bits (Receive Data Length)

The DTLN[8:0] bits indicate the length of the receive data.

While the FIFO buffer is being read, the DTLN[8:0] bits indicate different values depending on the DnFIFOSEL.RCNT bit (n = 0, 1), as follows:

- RCNT = 0
  The USBFS sets the DTLN[8:0] bits to indicate the length of the receive data until the CPU or DMA/DTC has read all of the received data from a single FIFO buffer plane.
  While the PIPECFG.BFRE bit = 1, the USBFS retains the length of the receive data until the BCLR bit is set to 1, even after all the data is read.
- RCNT = 1
  The USBFS decrements the value indicated in the DTLN[8:0] bits each time data is read from the FIFO buffer. The value is decremented by 1 when MBW = 0, and by 2 when MBW = 1.
  The USBFS sets these bits to 0 when all the data is read from one FIFO buffer plane. In double buffer mode, if data is received in one FIFO buffer plane before all of the data is read from the other plane, the USBFS sets these bits to indicate the length of the receive data in the former plane when all of the data is read from the latter plane.

从第一个条目。

请勿在同时更改CURPIPE[3:0]位时将此位设置为1。在将该位设置为1之前，请务必检查FRDY位是否为1。

要从传输管道的第一个数据重写FIFO缓冲区，请使用BCLR位。

RCNT位（读取计数模式）

RCNT位指定CFIFOCTR.DTLN位中值的读取模式。当使用DnFIFO访问PIPECFG.BFRE位设置为1，将RCNT位设置为0。

32.2.6 CFIFO端口控制寄存器(CFIFOCTR) D0FIFO端口控制寄存器(D0FIFOCTR)D1FIFO端口控制寄存器(D1FIFOCTR)

Address(es): USBFS.CFIFOCTR 4009 0022h, USBFS.D0FIFOCTR 4009 002Ah, USBFS.D1FIFOCTR 4009 002Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BVAL	BCLR	FRDY	—	—	—	—	DTLN[8:0]								
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b8 to b0	DTLN[8:0]	接收数据长度	表示接收数据长度。 这些值的含义因端口选择寄存器中的RCNT位设置而异。有关详细信息，请参见DTLN[8:0]位的说明。	R
b12 to b9	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b13	FRDY	FIFO端口就绪	0：禁止FIFO端口访问1：使能FIFO端口访问。	R
b14	BCLR	CPU缓冲区清除	0：无操作1：清除CPU端的FIFO缓冲区。	R/W*1
b15	BVAL	缓冲存储器有效标志	0：无效（写入0无效）1：写入结束。	R/W

Note 1. 只能读取0。

CFIFOCTR、D0FIFOCTR和D1FIFOCTR寄存器对应于CFIFO、D0FIFO和D1FIFO缓冲区。

DTLN[8:0]位（接收数据长度）

DTLN[8:0]位指示接收数据的长度。

在读取FIFO缓冲区时，DTLN[8:0]位指示不同的值，具体取决于DnFIFOSEL.RCNT位(n=0 1)，如下所示：

- RCNT = 0
  USBFS设置DTLN[8:0]位以指示接收数据的长度，直到CPU或DMADTC从单个FIFO缓冲区平面读取所有接收数据。当PIPECFG.BFRE位=1时，USBFS将保留接收数据的长度，直到BCLR位设置为1，即使在读取所有数据之后也是如此。
- RCNT = 1
  每次从FIFO缓冲区读取数据时，USBFS都会递减DTLN[8:0]位中指示的值。当MBW=0时该值减1，当MBW=1时减2。当从一个FIFO缓冲区平面读取所有数据时，USBFS将这些位设置为0。在双缓冲区模式下，如果在一个FIFO缓冲区平面中的所有数据从另一个平面读取之前接收到数据，USBFS设置这些位以指示在读取所有数据时前一个平面中接收数据的长度从后一个平面。

FRDY bit (FIFO Port Ready)

The FRDY bit indicates whether the FIFO port can be accessed by the CPU or DMA/DTC.

In the following cases, the USBFS sets the FRDY bit to 1 but data cannot be read through the FIFO port because there is no data to be read:

- A zero-length packet is received when the FIFO buffer assigned to the selected pipe is empty
- A short packet is received and the data is completely read while the PIPECFG.BFRE bit = 1.

In these cases, set the BCLR bit to 1 to clear the FIFO buffer, and enable transmission and reception of the next data.

BCLR bit (CPU Buffer Clear)

Set the BCLR bit to 1 to clear the FIFO buffer on the CPU side for the selected pipe.

When double buffer mode is set for the FIFO buffer assigned to the selected pipe, the USBFS clears only one plane of the FIFO buffer even when both planes are read-enabled.

When the DCP is the selected pipe, setting the BCLR bit to 1 allows the USBFS to clear the FIFO buffer regardless of whether the CPU or SIE has access rights. To clear the buffer when the SIE has access rights, set the DCPCTR.PID[1:0] bits to 00b (NAK response) before setting the BCLR bit to 1.

When the selected pipe is transmitting, if 1 is written to the BVAL flag and the BCLR bit simultaneously, the USBFS clears the data that is already written, enabling transmission of a zero-length packet.

When the selected pipe is not the DCP, only write 1 to the BCLR bit while the FRDY bit in the FIFO port control register is 1 (set by the USBFS).

BVAL flag (Buffer Memory Valid Flag)

Set the BVAL flag to 1 when data is completely written to the FIFO buffer on the CPU side for the pipe selected in CURPIPE[3:0].

When the selected pipe is transmitting, set this flag to 1 in the following cases:

- To transmit a short packet, set this flag to 1 after data is written
- To transmit a zero-length packet, set this flag to 1 before data is written to the FIFO buffer.

The USBFS then switches the FIFO buffer from the CPU side to the SIE side, enabling transmission.

When data of the maximum packet size is written for the pipe in continuous transfer mode, the USBFS sets the BVAL flag to 1 and switches the FIFO buffer from the CPU side to the SIE side, enabling transmission.

Only write 1 to the BVAL flag while the FRDY bit is 1 (set by the USBFS). When the selected pipe is receiving, do not set the BVAL flag to 1.

32.2.7 Interrupt Enable Register 0 (INTENB0)

Address(es): USBFS.INTENB0 4009 0030h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	VBSE	RSME	SOFE	DVSE	CTRE	BEMPE	NRDYE	BRDYE	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	BRDYE	Buffer Ready Interrupt Enable	0: Disable interrupt request 1: Enable interrupt request.	R/W
b9	NRDYE	Buffer Not Ready Response Interrupt Enable	0: Disable interrupt request 1: Enable interrupt request.	R/W

FRDY位（FIFO端口就绪）

FRDY位指示FIFO端口是否可以被CPU或DMADTC访问。

在以下情况下，USBFS将FRDY位设置为1，但由于没有数据可读取，因此无法通过FIFO端口读取数据：

- 当分配给所选管道的FIFO缓冲区为空时，接收到零长度数据包
- 当PIPECFG.BFRE位=1时，接收到一个短数据包并完全读取数据。

在这些情况下，将BCLR位设置为1以清除FIFO缓冲区，并启用下一个数据的发送和接收。

BCLR位（CPU缓冲区清除）

将BCLR位设置为1以清除所选管道的CPU端的FIFO缓冲区。

当分配给所选管道的FIFO缓冲区设置为双缓冲区模式时，USBFS仅清除
即使两个平面都已启用读取，也有FIFO缓冲区。

当DCP为选定管道时，将BCLR位设置为1允许USBFS清除FIFO缓冲区，而不管CPU或SIE是否具有访问权限。要在SIE具有访问权限时清除缓冲区，请将DCPCTR.PID[1:0]位设置为00b（NAK响应），然后再将BCLR位设置为1。

当所选管道正在传输时，如果同时向BVAL标志和BCLR位写入1，则USBFS会清除已写入的数据，从而可以传输零长度数据包。

当所选管道不是DCP时，仅在FIFO端口控制寄存器中的frdy位为1（由USBF设置）时，仅将1个写入BCLR位。

BVAL标志（缓冲存储器有效标志）

当数据完全写入CPU端的FIFO缓冲区时，将BVAL标志设置为1，用于在CURPIPE[3:0]。

当所选管道正在传输时，在以下情况下将此标志设置为1：

- 要发送短数据包，请在写入数据后将此标志设置为1
- 要发送长度为零的数据包，请在将数据写入FIFO缓冲区之前将此标志设置为1。

然后USBFS将FIFO缓冲区从CPU端切换到SIE端，从而启用传输。

当在连续传输模式下为管道写入最大数据包大小的数据时，USBFS将BVAL标志设置为1，并将FIFO缓冲区从CPU侧切换到SIE侧，从而启用传输。

仅在FRDY位为1（由USBFS设置）时将1写入BVAL标志。当所选管道正在接收时，不要将BVAL标志设置为1。

32.2.7 中断使能寄存器0(INTENB0)

Address(es): USBFS.INTENB0 4009 0030h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	VBSE	RSME	SOFE	DVSE	CTRE	BEMPE	NRDYE	BRDYE	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b7 to b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b8	BRDYE	缓冲区就绪中断使能	0：禁止中断请求1：允许中断请求。	R/W
b9	NRDYE	缓冲区未就绪响应中断使能	0：禁止中断请求1：允许中断请求。	R/W

Bit	Symbol	Bit name	Description	R/W
b10	BEMPE	Buffer Empty Interrupt Enable	0: Disable interrupt request 1: Enable interrupt request.	R/W
b11	CTRE	Control Transfer Stage Transition Interrupt Enable*1	0: Disable interrupt request 1: Enable interrupt request.	R/W
b12	DVSE	Device State Transition Interrupt Enable*1	0: Disable interrupt request 1: Enable interrupt request.	R/W
b13	SOFE	Frame Number Update Interrupt Enable	0: Disable interrupt request 1: Enable interrupt request.	R/W
b14	RSME	Resume Interrupt Enable*1	0: Disable interrupt request 1: Enable interrupt request.	R/W
b15	VBSE	VBUS Interrupt Enable	0: Disable interrupt request 1: Enable interrupt request.	R/W

Note 1. The RSME, DVSE, and CTRE bits can only be set to 1 in device controller mode. Do not set these bits to 1 in host controller mode.

When a status flag in the INTSTS0 register sets to 1 and the associated interrupt request enable bit setting in the INTENB0 register is 1, the USBFS issues a USBFS interrupt request.

Regardless of the INTENB0 register setting, the status flag in the INTSTS0 register sets to 1 in response to a state change that satisfies the associated condition.

When an interrupt request enable bit in the INTENB0 register is switched from 0 to 1 while the associated status flag in the INTSTS0 register is set to 1, a USBFS interrupt is requested.

32.2.8 Interrupt Enable Register 1 (INTENB1)

Address(es): USBFS.INTENB1 4009 0032h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	OVRCRE	BCHGE	—	DTCHE	ATTCHE	—	—	—	—	EOFERRE	SIGNE	SACKE	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	SACKE	Setup Transaction Normal Response Interrupt Enable	0: Disable interrupt request 1: Enable interrupt request.	R/W
b5	SIGNE	Setup Transaction Error Interrupt Enable	0: Disable interrupt request 1: Enable interrupt request.	R/W
b6	EOFERRE	EOF Error Detection Interrupt Enable	0: Disable interrupt request 1: Enable interrupt request.	R/W
b10 to b7	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b11	ATTCHE	Connection Detection Interrupt Enable	0: Disable interrupt request 1: Enable interrupt request.	R/W
b12	DTCHE	Disconnection Detection Interrupt Enable	0: Disable interrupt request 1: Enable interrupt request.	R/W
b13	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b14	BCHGE	USB Bus Change Interrupt Enable	0: Disable interrupt request 1: Enable interrupt request.	R/W
b15	OVRCRE	Overcurrent Input Change Interrupt Enable	0: Disable interrupt request 1: Enable interrupt request.	R/W

Note: The bits in INTENB1 can only be set to 1 in host controller mode. Do not set these bits to 1 in device controller mode.

INTENB1 specifies the interrupt masks in host controller mode and for the setup transaction.

Bit	Symbol	位名称	Description	R/W
b10	BEMPE	缓冲区空中断使能	0：禁止中断请求1：允许中断请求。	R/W
b11	CTRE	控制传输阶段转换中断Enable*1	0：禁止中断请求1：允许中断请求。	R/W
b12	DVSE	设备状态转换中断启用*1	0：禁止中断请求1：允许中断请求。	R/W
b13	SOFE	帧号更新中断使能	0：禁止中断请求1：允许中断请求。	R/W
b14	RSME	恢复中断使能*1	0：禁止中断请求1：允许中断请求。	R/W
b15	VBSE	VBUS中断使能	0：禁止中断请求1：允许中断请求。	R/W

Note 1. RSME、DVSE和CTRE位只能在设备控制器模式下设置为1。不要在主机控制器模式下将这些位设置为1。

当INTSTS0寄存器中的状态标志设置为1并且相关的中断请求使能位设置在INTENB0寄存器为1，USBFS发出USBFS中断请求。

无论INTENB0寄存器设置如何，INTSTS0寄存器中的状态标志都会设置为1，以响应满足相关条件的状态变化。

当INTENB0寄存器中的中断请求使能位从0切换到1且INTSTS0寄存器中的相关状态标志设置为1时，请求USBFS中断。

32.2.8 中断使能寄存器1(INTENB1)

Address(es): USBFS.INTENB1 4009 0032h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	OVRCRE	BCHGE	—	DTCHE	ATTCHE	—	—	—	—	EOFERRE	SIGNE	SACKE	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b3 to b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b4	SACKE	设置事务正常响应中断使能	0：禁止中断请求1：允许中断请求。	R/W
b5	SIGNE	设置事务错误中断Enable	0：禁止中断请求1：允许中断请求。	R/W
b6	EOFERRE	EOF错误检测中断使能	0：禁止中断请求1：允许中断请求。	R/W
b10 to b7	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b11	ATTCHE	连接检测中断使能	0：禁止中断请求1：允许中断请求。	R/W
b12	DTCHE	断线检测中断Enable	0：禁止中断请求1：允许中断请求。	R/W
b13	—	Reserved	该位读取为0。写入值应为0。	R/W
b14	BCHGE	USB总线变化中断使能	0：禁止中断请求1：允许中断请求。	R/W
b15	OVRCRE	过流输入变化中断Enable	0：禁止中断请求1：允许中断请求。	R/W

Note: INTENB1中的位只能在主机控制器模式下设置为1。不要在设备控制器模式下将这些位设置为1。

INTENB1指定主机控制器模式和设置事务的中断掩码。

When a status flag in the INTSTS1 register sets to 1 and the associated interrupt request enable bit setting in the INTENB1 register is 1, the USBFS issues a USBFS interrupt request.

Regardless of the INTENB1 register setting, the status flag in the INTSTS1 register sets to 1 in response to a state change that satisfies the associated condition.

When an interrupt request enable bit in the INTENB1 register is switched from 0 to 1 while the associated status flag in the INTSTS1 register is set to 1, a USBFS interrupt is requested.

Do not enable interrupts in device controller mode.

32.2.9 BRDY Interrupt Enable Register (BRDYENB)

Address(es): USBFS.BRDYENB 4009 0036h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	PIPE9BRDYE	PIPE8BRDYE	PIPE7BRDYE	PIPE6BRDYE	PIPE5BRDYE	PIPE4BRDYE	PIPE3BRDYE	PIPE2BRDYE	PIPE1BRDYE	PIPE0BRDYE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	PIPE0BRDYE	BRDY Interrupt Enable for Pipe 0	0: Disable interrupt request 1: Enable interrupt request.	R/W
b1	PIPE1BRDYE	BRDY Interrupt Enable for Pipe 1	0: Disable interrupt request 1: Enable interrupt request.	R/W
b2	PIPE2BRDYE	BRDY Interrupt Enable for Pipe 2	0: Disable interrupt request 1: Enable interrupt request.	R/W
b3	PIPE3BRDYE	BRDY Interrupt Enable for Pipe 3	0: Disable interrupt request 1: Enable interrupt request.	R/W
b4	PIPE4BRDYE	BRDY Interrupt Enable for Pipe 4	0: Disable interrupt request 1: Enable interrupt request.	R/W
b5	PIPE5BRDYE	BRDY Interrupt Enable for Pipe 5	0: Disable interrupt request 1: Enable interrupt request.	R/W
b6	PIPE6BRDYE	BRDY Interrupt Enable for Pipe 6	0: Disable interrupt request 1: Enable interrupt request.	R/W
b7	PIPE7BRDYE	BRDY Interrupt Enable for Pipe 7	0: Disable interrupt request 1: Enable interrupt request.	R/W
b8	PIPE8BRDYE	BRDY Interrupt Enable for Pipe 8	0: Disable interrupt request 1: Enable interrupt request.	R/W
b9	PIPE9BRDYE	BRDY Interrupt Enable for Pipe 9	0: Disable interrupt request 1: Enable interrupt request.	R/W
b15 to b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The BRDYENB register enables or disables the INTSTS0.BRDY bit to be set to 1 when a BRDY interrupt is detected for each pipe.

When a status flag in the BRDYSTS register sets to 1 and the associated PIPEnBRDYE bit (n = 0 to 9) setting in the BRDYENB register is 1, the INTSTS0.BRDY flag sets to 1. In this case, if the BRDYE bit in INTENB0 is 1, the USBFS generates a BRDY interrupt request. While at least one PIPEnBRDY bit indicates 1, the USB generates the BRDY interrupt request when the associated interrupt request enable bit in the BRDYENB register is changed from 0 to 1 by software.

当INTSTS1寄存器中的状态标志设置为1并且相关的中断请求使能位设置在INTENB1寄存器为1，USBFS发出USBFS中断请求。

无论INTENB1寄存器设置如何，INTSTS1寄存器中的状态标志都会设置为1，以响应满足相关条件的状态更改。

当INTENB1寄存器中的中断请求使能位从0切换到1且INTSTS1寄存器中的相关状态标志设置为1时，请求USBFS中断。

不要在设备控制器模式下启用中断。

32.2.9 BRDY中断使能寄存器(BRDYENB)

Address(es): USBFS.BRDYENB 4009 0036h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	PIPE9BRDYE	PIPE8BRDYE	PIPE7BRDYE	PIPE6BRDYE	PIPE5BRDYE	PIPE4BRDYE	PIPE3BRDYE	PIPE2BRDYE	PIPE1BRDYE	PIPE0BRDYE
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	PIPE0BRDYE	管道0的BRDY中断使能	0：禁止中断请求1：允许中断请求。	R/W
b1	PIPE1BRDYE	管道1的BRDY中断使能	0：禁止中断请求1：允许中断请求。	R/W
b2	PIPE2BRDYE	管道2的BRDY中断启用	0：禁止中断请求1：允许中断请求。	R/W
b3	PIPE3BRDYE	管道3的BRDY中断启用	0：禁止中断请求1：允许中断请求。	R/W
b4	PIPE4BRDYE	管道4的BRDY中断启用	0：禁止中断请求1：允许中断请求。	R/W
b5	PIPE5BRDYE	管道5的BRDY中断启用	0：禁止中断请求1：允许中断请求。	R/W
b6	PIPE6BRDYE	管道6的BRDY中断启用	0：禁止中断请求1：允许中断请求。	R/W
b7	PIPE7BRDYE	管道7的BRDY中断启用	0：禁止中断请求1：允许中断请求。	R/W
b8	PIPE8BRDYE	管道8的BRDY中断启用	0：禁止中断请求1：允许中断请求。	R/W
b9	PIPE9BRDYE	管道9的BRDY中断启用	0：禁止中断请求1：允许中断请求。	R/W
b15 to b10	—	Reserved	这些位被读取为0。写入值应为0。	R/W

当检测到每个管道的BRDY中断时，BRDYENB寄存器启用或禁用INTSTS0.BRDY位以设置为1。

当BRDYSTS寄存器中的状态标志设置为1并且相关的PIPEnBRDYE位（n=0到9）设置在BRDYENB寄存器为1，INTSTS0.BRDY标志设置为1。这种情况下，如果INTENB0中的BRDYE位为1，则USBFS产生一个BRDY中断请求。当至少一个PIPEnBRDY位指示1时，当BRDYENB寄存器中相关的中断请求使能位由软件从0变为1时，USB产生BRDY中断请求。

32.2.10 NRDY Interrupt Enable Register (NRDYENB)

Address(es): USBFS.NRDYENB 4009 0038h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	PIPE9NRDYE	PIPE8NRDYE	PIPE7NRDYE	PIPE6NRDYE	PIPE5NRDYE	PIPE4NRDYE	PIPE3NRDYE	PIPE2NRDYE	PIPE1NRDYE	PIPE0NRDYE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	PIPE0NRDYE	NRDY Interrupt Enable for Pipe 0	0: Disable interrupt request 1: Enable interrupt request.	R/W
b1	PIPE1NRDYE	NRDY Interrupt Enable for Pipe 1	0: Disable interrupt request 1: Enable interrupt request.	R/W
b2	PIPE2NRDYE	NRDY Interrupt Enable for Pipe 2	0: Disable interrupt request 1: Enable interrupt request.	R/W
b3	PIPE3NRDYE	NRDY Interrupt Enable for Pipe 3	0: Disable interrupt request 1: Enable interrupt request.	R/W
b4	PIPE4NRDYE	NRDY Interrupt Enable for Pipe 4	0: Disable interrupt request 1: Enable interrupt request.	R/W
b5	PIPE5NRDYE	NRDY Interrupt Enable for Pipe 5	0: Disable interrupt request 1: Enable interrupt request.	R/W
b6	PIPE6NRDYE	NRDY Interrupt Enable for Pipe 6	0: Disable interrupt request 1: Enable interrupt request.	R/W
b7	PIPE7NRDYE	NRDY Interrupt Enable for Pipe 7	0: Disable interrupt request 1: Enable interrupt request.	R/W
b8	PIPE8NRDYE	NRDY Interrupt Enable for Pipe 8	0: Disable interrupt request 1: Enable interrupt request.	R/W
b9	PIPE9NRDYE	NRDY Interrupt Enable for Pipe 9	0: Disable interrupt request 1: Enable interrupt request.	R/W
b15 to b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The NRDYENB register enables or disables the INTSTS0.NRDY bit to be set to 1 when a NRDY interrupt is detected for each pipe.

When a status flag in the NRDYSTS register sets to 1 and the associated PIPEnNRDYE (n = 0 to 9) bit setting in the NRDYENB register is 1, the INTSTS0.NRDY flag sets to 1. In this case, if the NRDYE bit in INTENB0 is 1, the USBFS generates a NRDY interrupt request. While at least one PIPEnNRDY bit indicates 1, the USBFS generates the NRDY interrupt request when the associated interrupt request enable bit in the NRDYENB register is changed from 0 to 1 by software.

32.2.11 BEMP Interrupt Enable Register (BEMPENB)

Address(es): USBFS.BEMPENB 4009 003Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	PIPE9BEMPE	PIPE8BEMPE	PIPE7BEMPE	PIPE6BEMPE	PIPE5BEMPE	PIPE4BEMPE	PIPE3BEMPE	PIPE2BEMPE	PIPE1BEMPE	PIPE0BEMPE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	PIPE0BEMPE	BEMP Interrupt Enable for Pipe 0	0: Disable interrupt request 1: Enable interrupt request.	R/W
b1	PIPE1BEMPE	BEMP Interrupt Enable for Pipe 1	0: Disable interrupt request 1: Enable interrupt request.	R/W

32.2.10 NRDY中断使能寄存器(NRDYENB)

Address(es): USBFS.NRDYENB 4009 0038h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	PIPE9NRDYE	PIPE8NRDYE	PIPE7NRDYE	PIPE6NRDYE	PIPE5NRDYE	PIPE4NRDYE	PIPE3NRDYE	PIPE2NRDYE	PIPE1NRDYE	PIPE0NRDYE
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	PIPE0NRDYE	管道0的NRDY中断使能	0：禁止中断请求1：允许中断请求。	R/W
b1	PIPE1NRDYE	管道1的NRDY中断使能	0：禁止中断请求1：允许中断请求。	R/W
b2	PIPE2NRDYE	管道2的NRDY中断使能	0：禁止中断请求1：允许中断请求。	R/W
b3	PIPE3NRDYE	管道3的NRDY中断使能	0：禁止中断请求1：允许中断请求。	R/W
b4	PIPE4NRDYE	管道4的NRDY中断使能	0：禁止中断请求1：允许中断请求。	R/W
b5	PIPE5NRDYE	管道5的NRDY中断使能	0：禁止中断请求1：允许中断请求。	R/W
b6	PIPE6NRDYE	管道6的NRDY中断使能	0：禁止中断请求1：允许中断请求。	R/W
b7	PIPE7NRDYE	管道7的NRDY中断使能	0：禁止中断请求1：允许中断请求。	R/W
b8	PIPE8NRDYE	管道8的NRDY中断使能	0：禁止中断请求1：允许中断请求。	R/W
b9	PIPE9NRDYE	管道9的NRDY中断使能	0：禁止中断请求1：允许中断请求。	R/W
b15 to b10	—	Reserved	这些位被读取为0。写入值应为0。	R/W

当检测到每个管道的NRDY中断时，NRDYENB寄存器启用或禁用INTSTS0.NRDY位设置为1。

当NRDYSTS寄存器中的状态标志设置为1并且NRDYENB寄存器中相关的PIPEnNRDYE（n=0到9）位设置为1时，INTSTS0.NRDY标志设置为1。在这种情况下，如果INTENB0中的NRDYE位为1，USBFS产生一个NRDY中断请求。当至少一个PIPEnNRDY位指示1时，当NRDYENB寄存器中相关的中断请求使能位由软件从0变为1时，USBFS产生NRDY中断请求。

32.2.11 BEMP中断使能寄存器(BEMPENB)

Address(es): USBFS.BEMPENB 4009 003Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	PIPE9BEMPE	PIPE8BEMPE	PIPE7BEMPE	PIPE6BEMPE	PIPE5BEMPE	PIPE4BEMPE	PIPE3BEMPE	PIPE2BEMPE	PIPE1BEMPE	PIPE0BEMPE
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	PIPE0BEMPE	管道0的BEMP中断启用	0：禁止中断请求1：允许中断请求。	R/W
b1	PIPE1BEMPE	管道1的BEMP中断启用	0：禁止中断请求1：允许中断请求。	R/W

Bit	Symbol	Bit name	Description	R/W
b2	PIPE2BEMPE	BEMP Interrupt Enable for Pipe 2	0: Disable interrupt request 1: Enable interrupt request.	R/W
b3	PIPE3BEMPE	BEMP Interrupt Enable for Pipe 3	0: Disable interrupt request 1: Enable interrupt request.	R/W
b4	PIPE4BEMPE	BEMP Interrupt Enable for Pipe 4	0: Disable interrupt request 1: Enable interrupt request.	R/W
b5	PIPE5BEMPE	BEMP Interrupt Enable for Pipe 5	0: Disable interrupt request 1: Enable interrupt request.	R/W
b6	PIPE6BEMPE	BEMP Interrupt Enable for Pipe 6	0: Disable interrupt request 1: Enable interrupt request.	R/W
b7	PIPE7BEMPE	BEMP Interrupt Enable for Pipe 7	0: Disable interrupt request 1: Enable interrupt request.	R/W
b8	PIPE8BEMPE	BEMP Interrupt Enable for Pipe 8	0: Disable interrupt request 1: Enable interrupt request.	R/W
b9	PIPE9BEMPE	BEMP Interrupt Enable for Pipe 9	0: Disable interrupt request 1: Enable interrupt request.	R/W
b15 to b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The BEMPENB register enables or disables the INTSTS0.BEMP bit to be set to 1 when a BEMP interrupt is detected for each pipe.

When a status flag in the BEMPSTS register sets to 1 and the associated PIPEnBEMPE (n = 0 to 9) bit setting in the BEMPENB register is 1, the INTSTS0.BEMP flag sets to 1. In this case, if the BEMPE bit in INTENB0 is 1, the USBFS generates a BEMP interrupt request. While at least one PIPEnBEMP bit indicates 1, the USBFS generates the BEMP interrupt request when the associated interrupt request enable bit in the BEMPENB register is changed from 0 to 1 by software.

32.2.12 SOF Output Configuration Register (SOFCFG)

Address(es): USBFS.SOFCFG 4009 003Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	TRNENSEL	—	BRDYM	—	EDGESTS	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	EDGESTS	Edge Interrupt Output Status Monitor*1	Indicates 1 during the edge processing of an edge interrupt output signal.	R
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6	BRDYM	BRDY Interrupt Status Clear Timing	0: Clear BRDY flag by software 1: Clear BRDY flag by the USBFS through a data read from the FIFO buffer or data write to the FIFO buffer.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b8	TRNENSEL	Transaction-Enabled Time Select*1	0: Not low-speed communication 1: Low-speed communication.	R/W
b15 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Confirm that these bits are 0 before stopping the clock supply to the USBFS.

EDGESTS bit (Edge Interrupt Output Status Monitor)

The EDGESTS bit indicates 1 during the edge processing of an edge interrupt output signal. Confirm that this bit is 0 before stopping the clock supply to the USBFS.

Bit	Symbol	位名称	Description	R/W
b2	PIPE2BEMPE	管道2的BEMP中断启用	0：禁止中断请求1：允许中断请求。	R/W
b3	PIPE3BEMPE	管道3的BEMP中断启用	0：禁止中断请求1：允许中断请求。	R/W
b4	PIPE4BEMPE	管道4的BEMP中断启用	0：禁止中断请求1：允许中断请求。	R/W
b5	PIPE5BEMPE	管道5的BEMP中断启用	0：禁止中断请求1：允许中断请求。	R/W
b6	PIPE6BEMPE	管道6的BEMP中断启用	0：禁止中断请求1：允许中断请求。	R/W
b7	PIPE7BEMPE	管道7的BEMP中断启用	0：禁止中断请求1：允许中断请求。	R/W
b8	PIPE8BEMPE	管道8的BEMP中断启用	0：禁止中断请求1：允许中断请求。	R/W
b9	PIPE9BEMPE	管道9的BEMP中断启用	0：禁止中断请求1：允许中断请求。	R/W
b15 to b10	—	Reserved	这些位被读取为0。写入值应为0。	R/W

当检测到每个管道的BEMP中断时，BEMPENB寄存器启用或禁用INTSTS0.BEMP位设置为1。

当BEMPSTS寄存器中的状态标志设置为1并且BEMPENB寄存器中相关的PIPEnBEMPE（n=0到9）位设置为1时，INTSTS0.BEMP标志设置为1。在这种情况下，如果INTENB0中的BEMPE位为1，USBFS产生一个BEMP中断请求。当至少一个PIPEnBEMP位指示1时，当BEMPENB寄存器中相关的中断请求使能位由软件从0变为1时，USBFS产生BEMP中断请求。

32.2.12 SOF输出配置寄存器(SOFCFG)

Address(es): USBFS.SOFCFG 4009 003Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	TRNENSEL	—	BRDYM	—	EDGESTS	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b3 to b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b4	EDGESTS	边沿中断输出状态监视器*1	在边沿中断输出信号的边沿处理期间表示1。	R
b5	—	Reserved	该位读取为0。写入值应为0。	R/W
b6	BRDYM	BRDY中断状态清除时序	0：软件清除BRDY标志1：USBFS通过从FIFO缓冲区读取数据或向FIFO缓冲区写入数据清除BRDY标志。	R/W
b7	—	Reserved	该位读取为0。写入值应为0。	R/W
b8	TRNENSEL	Transaction-Enabled Time Select*1	0：非低速通讯1：低速通讯。	R/W
b15 to b9	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 在停止向USBFS提供时钟之前，请确认这些位为0。

EDGESTS位（边缘中断输出状态监视器）

在边沿中断输出信号的边沿处理期间，EDGESTS位指示1。在停止向USBFS提供时钟之前，请确认该位为0。

BRDYM bit (BRDY Interrupt Status Clear Timing)

The BRDYM bit specifies how the BRDY interrupt status flags for the pipes are cleared.

TRNENSEL bit (Transaction-Enabled Time Select)

When the USB port is in use for full- or low-speed communications, the TRNENSEL bit specifies the timing with which the USBFS issues tokens in a frame (transaction-enabled time).

Set this bit to 1 when a low-speed device is connected directly or through a hub. The bit is only valid in host controller mode. Set this bit to 0 in device controller mode.

32.2.13 Interrupt Status Register 0 (INTSTS0)

Address(es): USBFS.INTSTS0 4009 0040h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	VBINT	RESM	SOFR	DVST	CTRT	BEMP	NRDY	BRDY	VBSTS	DVSQ[2:0]			VALID	CTSQ[2:0]		
Value after reset:	0	0	0	0/1*1	0	0	0	0	0*2	0*3	0*3	0/1*3	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	CTSQ[2:0]	Control Transfer Stage	b2 b0 0 0 0: Idle or setup stage 0 0 1: Control read data stage 0 1 0: Control read status stage 0 1 1: Control write data stage 1 0 0: Control write status stage 1 0 1: Control write (no data) status stage 1 1 0: Control transfer sequence error.	R
b3	VALID	USB Request Reception	0: Setup packet not received 1: Setup packet received.	R/W*4
b6 to b4	DVSQ[2:0]	Device State	Indicates the device state. b6 b4 0 0 0: Powered state 0 0 1: Default state 0 1 0: Address state 0 1 1: Configured state 1 x x: Suspend state.	R
b7	VBSTS	VBUS Input Status	0: USB_VBUS pin is low 1: USB_VBUS pin is high.	R
b8	BRDY	Buffer Ready Interrupt Status	0: No BRDY interrupt occurred 1: BRDY interrupt occurred.	R
b9	NRDY	Buffer Not Ready Interrupt Status	0: No NRDY interrupt occurred 1: NRDY interrupt occurred.	R
b10	BEMP	Buffer Empty Interrupt Status	0: No BEMP interrupt occurred 1: BEMP interrupt occurred.	R
b11	CTRT	Control Transfer Stage Transition Interrupt Status*5	0: No control transfer stage transition interrupt occurred 1: Control transfer stage transition interrupt occurred.	R/W*4
b12	DVST	Device State Transition Interrupt Status*5	0: No device state transition interrupt occurred 1: Device state transition interrupt occurred.	R/W*4
b13	SOFR	Frame Number Refresh Interrupt Status	0: No SOF interrupt occurred 1: SOF interrupt occurred.	R/W*4
b14	RESM	Resume Interrupt Status*5,*6	0: No resume interrupt occurred 1: Resume interrupt occurred.	R/W*4
b15	VBINT	VBUS Interrupt Status*6	0: No VBUS interrupt occurred 1: VBUS interrupt occurred.	R/W*4

x: Don't care

BRDYM位（BRDY中断状态清除时序）

BRDYM位指定如何清除管道的BRDY中断状态标志。

TRNENSEL位（事务使能时间选择）

当USB端口用于全速或低速通信时，TRNENSEL位指定USBFS在帧中发出令牌的时间（事务启用时间）。

当低速设备直接或通过集线器连接时，将此位设置为1。该位仅在主机控制器模式下有效。在设备控制器模式下将此位设置为0。

32.2.13 中断状态寄存器0(INTSTS0)

Address(es): USBFS.INTSTS0 4009 0040h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	VBINT	RESM	SOFR	DVST	CTRT	BEMP	NRDY	BRDY	VBSTS	DVSQ[2:0]			VALID	CTSQ[2:0]		
重置后的值：	0	0	0	0/1*1	0	0	0	0	0*2	0*3	0*3	0/1*3	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b2 to b0	CTSQ[2:0]	控制转移阶段	b2b0000：空闲或设置阶段001：控制读取数据阶段010：控制读取状态阶段011：控制写入数据阶段100：控制写入状态阶段101：控制写入（无数据）状态阶段110：控制传输顺序错误。	R
b3	VALID	USB请求接收	0：未收到设置包1：收到设置包。	R/W*4
b6 to b4	DVSQ[2:0]	设备状态	指示设备状态。b6b4000：通电状态001：默认状态010：地址状态011：配置状态1xx：挂起状态。	R
b7	VBSTS	VBUS输入状态	0：USB_VBUS引脚为低电平1：USB_VBUS引脚为高电平。	R
b8	BRDY	缓冲区就绪中断状态	0：未发生BRDY中断1：发生BRDY中断。	R
b9	NRDY	缓冲区未就绪中断Status	0：未发生NRDY中断1：发生NRDY中断。	R
b10	BEMP	缓冲区空中断状态	0：未发生BEMP中断1：发生BEMP中断。	R
b11	CTRT	控制转移阶段转换中断状态 *5	0：未发生控制转移阶段转换中断1：发生控制转移阶段转换中断。	R/W*4
b12	DVST	设备状态转换中断状态 *5	0：未发生设备状态转换中断1：发生设备状态转换中断。	R/W*4
b13	SOFR	帧号刷新中断状态	0：未发生SOF中断1：发生SOF中断。	R/W*4
b14	RESM	恢复中断状态 *5,*6	0：未发生恢复中断1：发生恢复中断。	R/W*4
b15	VBINT	VBUS中断状态 *6	0：未发生VBUS中断1：发生VBUS中断。	R/W*4

x: Don't care

Note 1. The value is 0 when the MCU is reset and 1 after a USB bus reset.
Note 2. The value is 1 when the USB_VBUS pin is high and 0 when the USB_VBUS pin is low.
Note 3. The value is 000b when the MCU is reset and 001b after a USB bus reset.
Note 4. To clear the VBINT, RESM, SOFR, DVST, CTRT, or VALID bits, write 0 only to the bits to be cleared. Write 1 to the other bits. Do not write 0 to the status bits indicating 0.
Note 5. The status of the RESM, DVST, and CTRT bits are changed only in device controller mode. Set the associated interrupt enable bits to 0 (disabled) in host controller mode.
Note 6. The USBFS detects a change in the status indicated in the VBINT and RESM bits even while the clock supply is stopped (SCKE bit = 0), and it requests the interrupt when the associated interrupt request bit is 1. Enable the clock supply before clearing the status by software.

CTSQ[2:0] bits (Control Transfer Stage)

In host controller mode, the read value of the CTSQ[2:0] bits is invalid.

VALID bit (USB Request Reception)

In host controller mode, the read value of the VALID bit is invalid.

DVSQ[2:0] bits (Device State)

The DVSQ[2:0] bits are initialized by a USB bus reset. In host controller mode, the read value is invalid.

BRDY flag (Buffer Ready Interrupt Status)

The BRDY flag indicates the BRDY interrupt status.

The USBFS sets the BRDY bit to 1 when it detects a BRDY interrupt status (PIPEnBRDY = 1, n = 0 to 9) on at least one pipe for which BRDY interrupts are enabled (BRDYENB.PIPEnBRDYE = 1).

For the conditions that cause the PIPEnBRDY status to be asserted, see section 32.3.3.1, BRDY interrupt.

The USBFS sets the BRDY bit to 0 when the software writes 0 to all of the PIPEnBRDY bits associated with the PIPEnBRDYE bits that are set to 1. Writing 0 to the BRDY flag in the software does not clear the flag.

NRDY flag (Buffer Not Ready Interrupt Status)

The NRDY flag indicates the NRDY interrupt status.

The USBFS sets the NRDY bit to 1 when it detects a NRDY interrupt status (PIPEnNRDY = 1, n = 0 to 9) on at least one pipe for which NRDY interrupts are enabled (NRDYENB.PIPEnNRDYE = 1).

For the conditions that cause the PIPEnNRDY status to be asserted, see section 32.3.3.2, NRDY interrupt.

The USBFS sets the NRDY bit to 0 when the software writes 0 to all of the PIPEnNRDY bits associated with the PIPEnNRDYE bits that are set to 1. Writing 0 to the NRDY flag in the software does not clear the flag.

BEMP flag (Buffer Empty Interrupt Status)

The BEMP flag indicates the BEMP interrupt status.

The USBFS sets the BEMP bit to 1 when it detects a BEMP interrupt status (PIPEnBEMP = 1, n = 0 to 9) on at least one pipe for which BEMP interrupts are enabled (BEMPENB.PIPEnBEMPE = 1).

For the conditions that cause the PIPEnBEMP status to be asserted, see section 32.3.3.3, BEMP interrupt.

The USBFS sets the BEMP bit to 0 when the software writes 0 to all of the PIPEnBEMP bits associated with the PIPEnBEMPE bits that are set to 1. Writing 0 to the BEMP flag in the software does not clear the flag.

CTRT flag (Control Transfer Stage Transition Interrupt Status)

In device controller mode, the USBFS updates the value of the CTSQ[2:0] bits and sets the CTRT flag to 1 on detecting a transition in the control transfer stage. When a control transfer stage transition interrupt occurs, clear the CTRT flag before the USBFS detects the next control transfer stage transition.

Values read from the CTRT flag in host controller mode are invalid.

DVST flag (Device State Transition Interrupt Status)

In device controller mode, the USBFS updates the value of the DVSQ[2:0] bits and sets the DVST flag to 1 on detecting a change in the device state. When a device state transition interrupt occurs, clear the DVST flag before the USBFS

Note 1. MCU复位时为0，USB总线复位后为1。
Note 2. 当USB_VBUS引脚为高电平时值为1，当USB_VBUS引脚为低电平时值为0。
Note 3. MCU复位时值为000b，USB总线复位后值为001b。
Note 4. 要清除VBINT、RESM、SOFR、DVST、CTRT或VALID位，只需将0写入要清除的位。将1写入其他位。不要将0写入指示0的状态位。
Note 5. RESM、DVST和CTRT位的状态仅在设备控制器模式下更改。在主机控制器模式下，将相关的中断使能位设置为0（禁用）。
Note 6. USBFS检测到VBINT和RESM位指示的状态变化，即使在时钟供应停止（SCKE位=0）时，它也会在相关的中断请求位为1时请求中断。在清除时钟之前启用时钟供应软件状态。

CTSQ[2:0]位（控制传输阶段）

在主机控制器模式下，CTSQ[2:0]位的读取值无效。

有效位（USB请求接收）

在主机控制器模式下，VALID位的读取值无效。

DVSQ[2:0]位（设备状态）

DVSQ[2:0]位由USB总线复位初始化。在主机控制器模式下，读取的值无效。

BRDY标志（缓冲区就绪中断状态）

BRDY标志指示BRDY中断状态。

当USBFS在至少一个启用了BRDY中断(BRDYENB.PIPEnBRDYE=1)的管道上检测到BRDY中断状态(PIPEnBRDY=1 n=0到9)时，将BRDY位设置为1。

有关导致PIPEnBRDY状态被断言的条件，请参见第32.3.3.1节，BRDY中断。

当软件将0写入与
设置为1的PIPEnBRDYE位。在软件中将0写入BRDY标志不会清除该标志。

NRDY标志（缓冲区未就绪中断状态）

NRDY标志指示NRDY中断状态。

当USBFS在至少一个启用了NRDY中断(NRDYENB.PIPEnNRDYE=1)的管道上检测到NRDY中断状态(PIPEnNRDY=1 n=0到9)时，将NRDY位设置为1。

有关导致PIPEnNRDY状态被断言的条件，请参见第32.3.3.2节，NRDY中断。

USBFS将NRDY位设置为0，当软件将0写入与
设置为1的PIPEnNRDYE位。在软件中将0写入NRDY标志不会清除该标志。

BEMP标志（缓冲区空中断状态）

BEMP标志指示BEMP中断状态。

当USBFS在至少一个启用了BEMP中断(BEMPENB.PIPEnBEMPE=1)的管道上检测到BEMP中断状态(PIPEnBEMP=1 n=0到9)时，将BEMP位设置为1。

有关导致PIPEnBEMP状态被断言的条件，请参阅第32.3.3.3节，BEMP中断。

当软件将0写入与
PIPEnBEMPE位设置为1。在软件中将0写入BEMP标志不会清除该标志。

CTRT标志（控制传输阶段转换中断状态）

在设备控制器模式下，USBFS更新CTSQ[2:0]位的值，并在检测到控制传输阶段的转换时将CTRT标志设置为1。
当控制传输阶段转换中断发生时，在USBFS检测到下一个控制传输阶段转换之前清除CTRT标志。

在主机控制器模式下从CTRT标志读取的值无效。

DVST标志（设备状态转换中断状态）

在设备控制器模式下，USBFS更新DVSQ[2:0]位的值，并在检测到设备状态发生变化时将DVST标志设置为1。
当发生设备状态转换中断时，在USBFS之前清除DVST标志

detects the next device state transition.

Values read from the DVST flag in host controller mode are invalid.

SOFR flag (Frame Number Refresh Interrupt Status)

In host controller mode, the USBFS sets the SOFR flag to 1 on updating the frame number when the DVSTCTR0.UACT bit is set to 1 by software. A SOFR interrupt is detected every 1 ms.

In device controller mode, the USBFS sets the SOFR flag to 1 on updating the frame number. A frame number refresh interrupt is detected every 1 ms.

The USBFS can detect an SOFR interrupt through the internal interpolation function even when a corrupted SOF packet is received from the USB host.

RESM flag (Resume Interrupt Status)

In device controller mode, the USBFS sets the RESM flag to 1 on detecting the falling edge of the signal on the USB_DP pin in the Suspend state (DVSQ[2:0] = 1xxb). Values read from the RESM flag in host controller mode are invalid.

VBINT flag (VBUS Interrupt Status)

The USBFS sets the VBINT flag to 1 on detecting a level change (high to low or low to high) in the USB_VBUS pin input value. The USBFS sets the VBSTS flag to indicate the USB_VBUS pin input value. When a VBUS interrupt occurs, eliminate transient elements by reading the VBSTS flag at least three times through software processing and check that the values read are the same.

32.2.14 Interrupt Status Register 1 (INTSTS1)

Address(es): USBFS.INTSTS1 4009 0042h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	OVRCR	BCHG	—	DTCH	ATTCH	—	—	—	—	EOFERR	SIGN	SACK	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	SACK	Setup Transaction Normal Response Interrupt Status	0: No SACK interrupt occurred 1: SACK interrupt occurred.	R/W *1
b5	SIGN	Setup Transaction Error Interrupt Status	0: No SIGN interrupt occurred 1: SIGN interrupt occurred.	R/W *1
b6	EOFERR	EOF Error Detection Interrupt Status	0: No EOFERR interrupt occurred 1: EOFERR interrupt occurred.	R/W *1
b10 to b7	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b11	ATTCH	ATTCH Interrupt Status	0: No ATTCH interrupt occurred 1: ATTCH interrupt occurred.	R/W *1
b12	DTCH	USB Disconnection Detection Interrupt Status	0: No DTCH interrupt occurred 1: DTCH interrupt occurred.	R/W *1
b13	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b14	BCHG	USB Bus Change Interrupt Status*2	0: No BCHG interrupt occurred 1: BCHG interrupt occurred.	R/W *1
b15	OVRCR	Overcurrent Input Change Interrupt Status*2	0: No OVRCR interrupt occurred 1: OVRCR interrupt occurred.	R/W *1

Note 1. To clear the bits in INTSTS1, write 0 only to the bits to be cleared. Write 1 to the other bits.
Note 2. The USBFS detects a change in the status in the OVRCR or BCHG bit even when the clock supply is stopped (SYSCFG.SCKE = 0), and it requests the interrupt when the associated interrupt request bit is 1. Enable the clock supply (SYSCFG.SCKE = 1)

检测下一个设备状态转换。

在主机控制器模式下从DVST标志读取的值无效。

SOFR标志（帧号刷新中断状态）

在主机控制器模式下，当软件将DVSTCTR0.UACT位设置为1时，USBFS在更新帧号时将SOFR标志设置为1。每1 ms检测一次SOFR中断。

在设备控制器模式下，USBFS在更新帧号时将SOFR标志设置为1。每1ms检测一次帧号刷新中断。

即使从USB主机接收到损坏的SOF数据包，USBFS也可以通过内部插值功能检测SOFR中断。

RESM标志（恢复中断状态）

在设备控制器模式下，USBFS在检测到处于挂起状态(DVSQ[2:0]=1xxb)的USB_DP引脚上的信号下降沿时将RESM标志设置为1。在主机控制器模式下从RESM标志读取的值无效。

VBINT标志（VBUS中断状态）

USBFS在检测到USB_VBUS引脚输入值的电平变化（从高到低或从低到高）时将VBINT标志设置为1。USBFS设置VBSTS标志以指示USB_VBUS引脚输入值。当发生VBUS中断时，通过软件处理至少3次读取VBSTS标志来消除瞬态元素，并检查读取的值是否相同。

32.2.14 中断状态寄存器1(INTSTS1)

Address(es): USBFS.INTSTS1 4009 0042h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	OVRCR	BCHG	—	DTCH	ATTCH	—	—	—	—	EOFERR	SIGN	SACK	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b3 to b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b4	SACK	设置事务正常响应中断状态	0：未发生SACK中断1：发生SACK中断。	R/W *1
b5	SIGN	设置事务错误中断状态	0：未发生SIGN中断1：发生SIGN中断。	R/W *1
b6	EOFERR	EOF错误检测中断状态	0：没有EOFERR中断发生1：EOFERR中断发生。	R/W *1
b10 to b7	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b11	ATTCH	ATTCH中断状态	0：未发生ATTCH中断1：发生ATTCH中断。	R/W *1
b12	DTCH	USB断线检测中断Status	0：未发生DTCH中断1：发生DTCH中断。	R/W *1
b13	—	Reserved	该位读取为0。写入值应为0。	R/W
b14	BCHG	USB总线更改中断状态 *2	0：未发生BCHG中断1：发生BCHG中断。	R/W *1
b15	OVRCR	过流输入变化中断Status*2	0：未发生OVRCR中断1：发生OVRCR中断。	R/W *1

Note 1. 要清除INTSTS1中的位，只需将0写入要清除的位。将1写入其他位。
Note 2. 即使在停止提供时钟（SYSCFG.SCKE=0）时，USBFS也会检测到OVRCR或BCHG位的状态变化，并在相关的中断请求位为1时请求中断。启用时钟提供（SYSCFG.SCKE=1）

before clearing the status through the software. No other interrupts can be detected while the clock supply is stopped (SYSCFG.SCKE bit = 0).

INTSTS1 is used to confirm the status of each interrupt in host controller mode. Only enable the status change interrupts indicated in the bits in INTSTS1 in host controller mode.

SACK flag (Setup Transaction Normal Response Interrupt Status)

The SACK flag indicates the status of the setup transaction normal response interrupt in host controller mode.

The USBFS detects the SACK interrupt and sets this flag to 1 when an ACK response is returned from a peripheral device during the setup transactions issued by the USBFS. If the associated interrupt enable bit is set to 1 by software, the USBFS generates the interrupt.

Values read from the SACK flag in device controller mode are invalid.

SIGN flag (Setup Transaction Error Interrupt Status)

The SIGN flag indicates the status of setup transaction error interrupts in host controller mode.

The USBFS detects the SIGN interrupt and sets this flag to 1 when an ACK response is not returned from a peripheral device three consecutive times during the setup transactions issued by the USBFS. If the associated interrupt enable bit is set to 1 by software, the USBFS generates the interrupt.

The USBFS detects the SIGN interrupt when any of the following response conditions occur for three consecutive setup transactions:

- Timeout is detected by the USBFS when the peripheral device has returned no response
- A corrupted ACK packet is received
- A handshake other than ACK (NAK, NYET, or STALL) is received.

Values read from the SIGN flag in device controller mode are invalid.

EOFERR flag (EOF Error Detection Interrupt Status)

The EOFERR flag indicates the status of EOF error detection interrupts in host controller mode.

The USBFS detects the EOFERR interrupt and sets this flag to 1 on detecting that communication did not complete at the EOF2 timing defined in the USB 2.0 specification. If the associated interrupt enable bit is set to 1 by software, the USBFS generates the interrupt.

After detecting the EOFERR interrupt, the USBFS controls the hardware as follows, regardless of the associated interrupt enable bit setting:

- Sets the DVSTCTR0.UACT bit for the port in which the EOFERR interrupt was detected to 0
- Puts the port in which the EOFERR interrupt occurred into the idle state.

The software must terminate all pipes in which communications are being carried out and re-enumerate the USB port.

Values read from the EOFERR flag in device controller mode are invalid.

ATTCH flag (ATTCH Interrupt Status)

The ATTCH flag indicates the status of USB attach detection interrupts in host controller mode.

The USBFS detects the ATTCH interrupt and sets this flag to 1 on detecting a J- or K-state on the full- or low-speed signal level for 2.5 µs. If the associated interrupt enable bit is set to 1 by software, the USBFS generates the interrupt.

The USBFS detects the ATTCH interrupt on any of the following conditions.

- K-state, SE0, or SE1 changes to J-state, and J-state continues for 2.5 µs
- J-state, SE0, or SE1 changes to K-state, and K-state continues for 2.5 µs.

Values read from the ATTCH flag in device controller mode are invalid.

DTCH flag (USB Disconnection Detection Interrupt Status)

The DTCH flag indicates the status of USB disconnection detection interrupts in host controller mode.

在通过软件清除状态之前。停止提供时钟（SYSCFG.SCKE位=0）时，不会检测到其他中断。

INTSTS1用于确认主机控制器模式下每个中断的状态。仅在主机控制器模式下启用INTSTS1位中指示的状态更改中断。

SACK标志（设置事务正常响应中断状态）

SACK标志指示主机控制器模式下设置事务正常响应中断的状态。

在USBFS发出的设置事务期间，当外围设备返回ACK响应时，USBFS检测到SACK中断并将该标志设置为1。如果相关的中断使能位由软件设置为1，则USBFS产生中断。

在设备控制器模式下从SACK标志读取的值无效。

SIGN标志（设置事务错误中断状态）

SIGN标志指示主机控制器模式下设置事务错误中断的状态。

在USBFS发出的设置事务期间，如果外围设备连续3次没有返回ACK响应，则USBFS检测到SIGN中断并将该标志设置为1。如果相关的中断使能位由软件设置为1，则USBFS产生中断。

当三个连续的设置事务发生以下任何响应条件时，USBFS检测到SIGN中断：

- 当外围设备没有返回响应时，USBFS检测到超时
- 收到损坏的ACK数据包
- 收到除ACK（NAK、NYET或STALL）以外的握手。

在设备控制器模式下从SIGN标志读取的值无效。

EOFERR标志（EOF错误检测中断状态）

EOFERR标志指示主机控制器模式下EOF错误检测中断的状态。

USBFS检测到EOFERR中断，并在检测到通信未完成时将此标志设置为1
USB2.0规范中定义的EOF2时序。如果相关的中断使能位由软件设置为1，则
USBFS产生中断。

检测到EOFERR中断后，USBFS对硬件进行如下控制，而不考虑相关的中断使能位设置：

- 将检测到EOFERR中断的端口的DVSTCTR0.UACT位设置为0
- 将发生EOFERR中断的端口置于空闲状态。

软件必须终止正在执行通信的所有管道并重新枚举USB端口。

在设备控制器模式下从EOFERR标志读取的值无效。

ATTCH标志（ATTCH中断状态）

ATTCH标志指示主机控制器模式下USB连接检测中断的状态。

USBFS检测到ATTCH中断，并在检测到全速或低速信号电平上的JorK状态持续2.5µs时将此标志设置为1。如果相关的中断使能位由软件设置为1，则USBFS产生中断。

USBFS在以下任何条件下检测ATTCH中断。

- K-state、SE0或SE1变为J-state，J-state持续2.5µs
- J-state、SE0或SE1变为K-state，K-state持续2.5µs。

在设备控制器模式下从ATTCH标志读取的值无效。

DTCH标志（USB断线检测中断状态）

DTCH标志指示主机控制器模式下USB断开检测中断的状态。

The USBFS detects the DTCH interrupt and sets this flag to 1 on detecting a USB bus detach event. If the associated interrupt enable bit is set to 1 by software, the USBFS generates the interrupt.

The USBFS detects bus detach events based on the USB 2.0 specification.

After detecting the DTCH interrupt, the USBFS controls hardware as follows, regardless of the associated interrupt enable bit setting:

- Sets the DVSTCTR0.UACT bit for the port in which the DTCH interrupt was detected to 0
- Puts the port in which the DTCH interrupt occurred into the idle state.

The software must terminate all pipes in which communications are being carried out and invoke the wait state for attaching to the USB port (waiting for ATTCH interrupt generation).

Values read from the DTCH flag in device controller mode are invalid.

BCHG flag (USB Bus Change Interrupt Status)

The BCHG flag indicates the status of USB bus change interrupts in host controller mode.

The USBFS detects the BCHG interrupt and sets this flag to 1 when a change in the full- or low-speed signal level occurs on the USB port. This includes any change from J-state, K-state, or SE0 to J-state, K-state, or SE0. If the associated interrupt enable bit is set to 1 by software, the USBFS generates the interrupt.

The USBFS sets the LNST[1:0] flags to indicate the input state of the USB port. When a BCHG interrupt occurs, eliminate transient elements by repeat reading the LNST[1:0] flags by software until the same value is read at least three times.

Change in the USB bus state can be detected while the internal clock is stopped.

Values read from the BCHG flag in device controller mode are invalid.

OVRCR flag (Overcurrent Input Change Interrupt Status)

The OVRCR flag indicates the status of USB_OVRCURA and USB_OVRCURB input pin change interrupts.

The USBFS detects the OVRCR interrupt and sets this flag to 1 when a change (high to low or low to high) occurs in at least one of the input values to the USB_OVRCURA and USB_OVRCURB pins. If the associated interrupt enable bit is set to 1 by software, the USBFS generates the interrupt.

32.2.15 BRDY Interrupt Status Register (BRDYSTS)

Address(es): USBFS.BRDYSTS 4009 0046h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	PIPE9BRDY	PIPE8BRDY	PIPE7BRDY	PIPE6BRDY	PIPE5BRDY	PIPE4BRDY	PIPE3BRDY	PIPE2BRDY	PIPE1BRDY	PIPE0BRDY
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	PIPE0BRDY	BRDY Interrupt Status for Pipe 0*2	0: No BRDY interrupt occurred 1: BRDY interrupt occurred.	R/W *1
b1	PIPE1BRDY	BRDY Interrupt Status for Pipe 1*2	0: No BRDY interrupt occurred 1: BRDY interrupt occurred.	R/W *1
b2	PIPE2BRDY	BRDY Interrupt Status for Pipe 2*2	0: No BRDY interrupt occurred 1: BRDY interrupt occurred.	R/W *1
b3	PIPE3BRDY	BRDY Interrupt Status for Pipe 3*2	0: No BRDY interrupt occurred 1: BRDY interrupt occurred.	R/W *1
b4	PIPE4BRDY	BRDY Interrupt Status for Pipe 4*2	0: No BRDY interrupt occurred 1: BRDY interrupt occurred.	R/W *1
b5	PIPE5BRDY	BRDY Interrupt Status for Pipe 5*2	0: No BRDY interrupt occurred 1: BRDY interrupt occurred.	R/W *1

USBFS检测到DTCH中断并在检测到USB总线分离事件时将此标志设置为1。如果相关的中断使能位由软件设置为1，则USBFS产生中断。

USBFS根据USB2.0规范检测总线分离事件。

检测到DTCH中断后，USBFS对硬件进行如下控制，而不管相关的中断使能位设置如何：

- 将检测到DTCH中断的端口的DVSTCTR0.UACT位设置为0
- 将发生DTCH中断的端口置于空闲状态。

软件必须终止正在执行通信的所有管道并调用等待状态以连接到USB端口（等待ATTCH中断生成）。

在设备控制器模式下从DTCH标志读取的值无效。

BCHG标志（USB总线更改中断状态）

BCHG标志指示主机控制器模式下USB总线更改中断的状态。

当USB端口上发生全速或低速信号电平变化时，USBFS检测到BCHG中断并将该标志设置为1。这包括从J-state、K-state或SE0到J-state、K-state或SE0的任何更改。如果相关的中断使能位由软件设置为1，则USBFS产生中断。

USBFS设置LNST[1:0]标志以指示USB端口的输入状态。当发生BCHG中断时，通过软件重复读取LNST[1:0]标志来消除瞬态元素，直到至少读取相同的值3次。

当内部时钟停止时，可以检测到USB总线状态的变化。

在设备控制器模式下从BCHG标志读取的值无效。

OVRCR标志（过流输入变化中断状态）

OVRCR标志指示USB_OVRCURA和USB_OVRCURB输入引脚变化中断的状态。

当USB_OVRCURA和USB_OVRCURB引脚的至少一个输入值发生变化（从高到低或从低到高）时，USBFS检测到OVRCR中断并将该标志设置为1。如果相关的中断使能位由软件设置为1，则USBFS产生中断。

32.2.15 BRDY中断状态寄存器(BRDYSTS)

Address(es): USBFS.BRDYSTS 4009 0046h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	PIPE9BRDY	PIPE8BRDY	PIPE7BRDY	PIPE6BRDY	PIPE5BRDY	PIPE4BRDY	PIPE3BRDY	PIPE2BRDY	PIPE1BRDY	PIPE0BRDY
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	PIPE0BRDY	管道0*2的BRDY中断状态	0：未发生BRDY中断1：发生BRDY中断。	R/W *1
b1	PIPE1BRDY	管道1*2的BRDY中断状态	0：未发生BRDY中断1：发生BRDY中断。	R/W *1
b2	PIPE2BRDY	管道2*2的BRDY中断状态	0：未发生BRDY中断1：发生BRDY中断。	R/W *1
b3	PIPE3BRDY	管道3*2的BRDY中断状态	0：未发生BRDY中断1：发生BRDY中断。	R/W *1
b4	PIPE4BRDY	管道4*2的BRDY中断状态	0：未发生BRDY中断1：发生BRDY中断。	R/W *1
b5	PIPE5BRDY	管道5*2的BRDY中断状态	0：未发生BRDY中断1：发生BRDY中断。	R/W *1

Bit	Symbol	Bit name	Description	R/W
b6	PIPE6BRDY	BRDY Interrupt Status for Pipe 6*2	0: No BRDY interrupt occurred 1: BRDY interrupt occurred.	R/W *1
b7	PIPE7BRDY	BRDY Interrupt Status for Pipe 7*2	0: No BRDY interrupt occurred 1: BRDY interrupt occurred.	R/W *1
b8	PIPE8BRDY	BRDY Interrupt Status for Pipe 8*2	0: No BRDY interrupt occurred 1: BRDY interrupt occurred.	R/W *1
b9	PIPE9BRDY	BRDY Interrupt Status for Pipe 9*2	0: No BRDY interrupt occurred 1: BRDY interrupt occurred.	R/W *1
b15 to b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. When the SOFCFG.BRDYM bit is set to 0, to clear the status indicated in the bits in BRDYSTS, write 0 only to the bits to be cleared. Write 1 to the other bits.
Note 2. When the SOFCFG.BRDYM bit is set to 0, clear BRDY interrupts before accessing the FIFO.

32.2.16 NRDY Interrupt Status Register (NRDYSTS)

Address(es): USBFS.NRDYSTS 4009 0048h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	PIPE9NRDY	PIPE8NRDY	PIPE7NRDY	PIPE6NRDY	PIPE5NRDY	PIPE4NRDY	PIPE3NRDY	PIPE2NRDY	PIPE1NRDY	PIPE0NRDY
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	PIPE0NRDY	NRDY Interrupt Status for Pipe 0	0: No NRDY interrupt occurred 1: NRDY interrupt occurred.	R/W *1
b1	PIPE1NRDY	NRDY Interrupt Status for Pipe 1	0: No NRDY interrupt occurred 1: NRDY interrupt occurred.	R/W *1
b2	PIPE2NRDY	NRDY Interrupt Status for Pipe 2	0: No NRDY interrupt occurred 1: NRDY interrupt occurred.	R/W *1
b3	PIPE3NRDY	NRDY Interrupt Status for Pipe 3	0: No NRDY interrupt occurred 1: NRDY interrupt occurred.	R/W *1
b4	PIPE4NRDY	NRDY Interrupt Status for Pipe 4	0: No NRDY interrupt occurred 1: NRDY interrupt occurred.	R/W *1
b5	PIPE5NRDY	NRDY Interrupt Status for Pipe 5	0: No NRDY interrupt occurred 1: NRDY interrupt occurred.	R/W *1
b6	PIPE6NRDY	NRDY Interrupt Status for Pipe 6	0: No NRDY interrupt occurred 1: NRDY interrupt occurred.	R/W *1
b7	PIPE7NRDY	NRDY Interrupt Status for Pipe 7	0: No NRDY interrupt occurred 1: NRDY interrupt occurred.	R/W *1
b8	PIPE8NRDY	NRDY Interrupt Status for Pipe 8	0: No NRDY interrupt occurred 1: NRDY interrupt occurred.	R/W *1
b9	PIPE9NRDY	NRDY Interrupt Status for Pipe 9	0: No NRDY interrupt occurred 1: NRDY interrupt occurred.	R/W *1
b15 to b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. To clear the status indicated in the bits in NRDYSTS, write 0 only to the bits to be cleared. Write 1 to the other bits.

Bit	Symbol	位名称	Description	R/W
b6	PIPE6BRDY	管道6*2的BRDY中断状态	0：未发生BRDY中断1：发生BRDY中断。	R/W *1
b7	PIPE7BRDY	管道7*2的BRDY中断状态	0：未发生BRDY中断1：发生BRDY中断。	R/W *1
b8	PIPE8BRDY	管道8*2的BRDY中断状态	0：未发生BRDY中断1：发生BRDY中断。	R/W *1
b9	PIPE9BRDY	管道9*2的BRDY中断状态	0：未发生BRDY中断1：发生BRDY中断。	R/W *1
b15 to b10	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 当SOFCFG.BRDYM位设置为0时，要清除BRDYSTS中位指示的状态，只需将0写入要清除的位。将1写入其他位。
Note 2. 当SOFCFG.BRDYM位设置为0时，在访问FIFO之前清除BRDY中断。

32.2.16 NRDY中断状态寄存器(NRDYSTS)

Address(es): USBFS.NRDYSTS 4009 0048h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	PIPE9NRDY	PIPE8NRDY	PIPE7NRDY	PIPE6NRDY	PIPE5NRDY	PIPE4NRDY	PIPE3NRDY	PIPE2NRDY	PIPE1NRDY	PIPE0NRDY
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	PIPE0NRDY	管道0的NRDY中断状态	0：未发生NRDY中断1：发生NRDY中断。	R/W *1
b1	PIPE1NRDY	管道1的NRDY中断状态	0：未发生NRDY中断1：发生NRDY中断。	R/W *1
b2	PIPE2NRDY	管道2的NRDY中断状态	0：未发生NRDY中断1：发生NRDY中断。	R/W *1
b3	PIPE3NRDY	管道3的NRDY中断状态	0：未发生NRDY中断1：发生NRDY中断。	R/W *1
b4	PIPE4NRDY	管道4的NRDY中断状态	0：未发生NRDY中断1：发生NRDY中断。	R/W *1
b5	PIPE5NRDY	管道5的NRDY中断状态	0：未发生NRDY中断1：发生NRDY中断。	R/W *1
b6	PIPE6NRDY	管道6的NRDY中断状态	0：未发生NRDY中断1：发生NRDY中断。	R/W *1
b7	PIPE7NRDY	管道7的NRDY中断状态	0：未发生NRDY中断1：发生NRDY中断。	R/W *1
b8	PIPE8NRDY	管道8的NRDY中断状态	0：未发生NRDY中断1：发生NRDY中断。	R/W *1
b9	PIPE9NRDY	管道9的NRDY中断状态	0：未发生NRDY中断1：发生NRDY中断。	R/W *1
b15 to b10	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 要清除NRDYSTS中位中指示的状态，请仅将0写入要清除的位。将1写入其他位。

32.2.17 BEMP Interrupt Status Register (BEMPSTS)

Address(es): USBFS.BEMPSTS 4009 004Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	PIPE9BEMP	PIPE8BEMP	PIPE7BEMP	PIPE6BEMP	PIPE5BEMP	PIPE4BEMP	PIPE3BEMP	PIPE2BEMP	PIPE1BEMP	PIPE0BEMP
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	PIPE0BEMP	BEMP Interrupt Status for Pipe 0	0: No BEMP interrupt occurred 1: BEMP interrupt occurred.	R/W *1
b1	PIPE1BEMP	BEMP Interrupt Status for Pipe 1	0: No BEMP interrupt occurred 1: BEMP interrupt occurred.	R/W *1
b2	PIPE2BEMP	BEMP Interrupt Status for Pipe 2	0: No BEMP interrupt occurred 1: BEMP interrupt occurred.	R/W *1
b3	PIPE3BEMP	BEMP Interrupt Status for Pipe 3	0: No BEMP interrupt occurred 1: BEMP interrupt occurred.	R/W *1
b4	PIPE4BEMP	BEMP Interrupt Status for Pipe 4	0: No BEMP interrupt occurred 1: BEMP interrupt occurred.	R/W *1
b5	PIPE5BEMP	BEMP Interrupt Status for Pipe 5	0: No BEMP interrupt occurred 1: BEMP interrupt occurred.	R/W *1
b6	PIPE6BEMP	BEMP Interrupt Status for Pipe 6	0: No BEMP interrupt occurred 1: BEMP interrupt occurred.	R/W *1
b7	PIPE7BEMP	BEMP Interrupt Status for Pipe 7	0: No BEMP interrupt occurred 1: BEMP interrupt occurred.	R/W *1
b8	PIPE8BEMP	BEMP Interrupt Status for Pipe 8	0: No BEMP interrupt occurred 1: BEMP interrupt occurred.	R/W *1
b9	PIPE9BEMP	BEMP Interrupt Status for Pipe 9	0: No BEMP interrupt occurred 1: BEMP interrupt occurred.	R/W *1
b15 to b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. To clear the status indicated in the bits in BEMPSTS, write 0 only to the bits to be cleared. Write 1 to the other bits.

32.2.18 Frame Number Register (FRMNUM)

Address(es): USBFS.FRMNUM 4009 004Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	OVRN	CRCE	—	—	—	FRNM[10:0]										
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b10 to b0	FRNM[10:0]	Frame Number	Latest frame number.	R
b13 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b14	CRCE	Receive Data Error	0: No error occurred 1: Error occurred.	R/W*1
b15	OVRN	Overrun/Underrun Detection Status	0: No error occurred 1: Error occurred.	R/W*1

Note 1. To clear the status, write 0 only to the bits to be cleared. Write 1 to the other bits.

32.2.17 BEMP中断状态寄存器(BEMPSTS)

Address(es): USBFS.BEMPSTS 4009 004Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	PIPE9BEMP	PIPE8BEMP	PIPE7BEMP	PIPE6BEMP	PIPE5BEMP	PIPE4BEMP	PIPE3BEMP	PIPE2BEMP	PIPE1BEMP	PIPE0BEMP
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	PIPE0BEMP	管道0的BEMP中断状态	0：未发生BEMP中断1：发生BEMP中断。	R/W *1
b1	PIPE1BEMP	管道1的BEMP中断状态	0：未发生BEMP中断1：发生BEMP中断。	R/W *1
b2	PIPE2BEMP	管道2的BEMP中断状态	0：未发生BEMP中断1：发生BEMP中断。	R/W *1
b3	PIPE3BEMP	管道3的BEMP中断状态	0：未发生BEMP中断1：发生BEMP中断。	R/W *1
b4	PIPE4BEMP	管道4的BEMP中断状态	0：未发生BEMP中断1：发生BEMP中断。	R/W *1
b5	PIPE5BEMP	管道5的BEMP中断状态	0：未发生BEMP中断1：发生BEMP中断。	R/W *1
b6	PIPE6BEMP	管道6的BEMP中断状态	0：未发生BEMP中断1：发生BEMP中断。	R/W *1
b7	PIPE7BEMP	管道7的BEMP中断状态	0：未发生BEMP中断1：发生BEMP中断。	R/W *1
b8	PIPE8BEMP	管道8的BEMP中断状态	0：未发生BEMP中断1：发生BEMP中断。	R/W *1
b9	PIPE9BEMP	管道9的BEMP中断状态	0：未发生BEMP中断1：发生BEMP中断。	R/W *1
b15 to b10	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 要清除BEMPSTS中位中指示的状态，请仅将0写入要清除的位。将1写入其他位。

32.2.18 帧号寄存器(FRMNUM)

Address(es): USBFS.FRMNUM 4009 004Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	OVRN	CRCE	—	—	—	FRNM[10:0]										
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b10 to b0	FRNM[10:0]	帧号	最新帧号。	R
b13 to b11	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b14	CRCE	接收数据错误	0：未发生错误1：发生错误。	R/W*1
b15	OVRN	OverrunUnderrun检测状态	0：未发生错误1：发生错误。	R/W*1

Note 1. 要清除状态，只向要清除的位写入0。将1写入其他位。

FRNM[10:0] flags (Frame Number)

The USBFS sets the FRNM[10:0] flags to indicate the latest frame number, which is updated every 1 ms, when an SOF packet is issued or received.

CRCE flag (Receive Data Error)

The CRCE flag sets to 1 when a CRC error or bit stuffing error occurs during isochronous transfer. On detecting a CRC error in host controller mode, the USBFS generates an internal NRDY interrupt.

To clear the CRCE flag, write 0 to it while writing 1 to the other bits in the FRMNUM register.

OVRN flag (Overrun/Underrun Detection Status)

The OVRN flag sets to 1 when an overrun or underrun error occurs during isochronous transfer. To clear the flag, write 0 to it while writing 1 to the other bits in the FRMNUM register.

In host controller mode, the OVRN flag sets to 1 on any of the following conditions:

- For a transmitting isochronous pipe, the time to issue an OUT token comes before all of the transmit data is written to the FIFO buffer
- For a receiving isochronous pipe, the time to issue an IN token comes when no FIFO buffer planes are empty.

In device controller mode, the OVRN flag sets to 1 on any of the following conditions:

- For a transmitting isochronous pipe, the IN token is received before all of the transmit data is written to the FIFO buffer
- For a receiving isochronous pipe, the OUT token is received when no FIFO buffer planes are empty.

32.2.19 Device State Change Register (DVCHGR)

Address(es): USBFS.DVCHGR 4009 004Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	DVCHG	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b14 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15	DVCHG	Device State Change	0: Disable writes to the USBADDR.STSRECOV[3:0] and USBADDR.USBADDR[6:0] bits 1: Enable writes to the USBADDR.STSRECOV[3:0] and USBADDR.USBADDR[6:0] bits.	R/W

For details, see section 32.3.1.5, Release from deep software standby mode because of USB suspend/resume interrupts.

FRNM[10:0]标志（帧号）

USBFS设置FRNM[10:0]标志以指示最新的帧号，该帧号每1ms更新一次，当发出或接收SOF数据包时。

CRCE标志（接收数据错误）

当同步传输期间发生CRC错误或位填充错误时，CRCE标志设置为1。在主机控制器模式下检测到CRC错误时，USBFS会生成内部NRDY中断。

要清除CRCE标志，向其写入0，同时向FRMNUM寄存器中的其他位写入1。

OVRN标志（溢出欠载检测状态）

当同步传输期间发生溢出或欠载错误时，OVRN标志设置为1。要清除该标志，请向其写入0，同时向FRMNUM寄存器中的其他位写入1。

在主机控制器模式下，OVRN标志在以下任何条件下设置为1：

- 对于传输同步管道，发出OUT令牌的时间出现在所有传输数据写入FIFO缓冲区之前
- 对于接收同步管道，在没有FIFO缓冲区平面为空时发出IN令牌。

在设备控制器模式下，OVRN标志在以下任何条件下设置为1：

- 对于传输同步管道，在所有传输数据写入FIFO缓冲区之前接收到IN令牌
- 对于接收同步管道，当没有FIFO缓冲区平面为空时接收OUT令牌。

32.2.19 设备状态更改寄存器(DVCHGR)

Address(es): USBFS.DVCHGR 4009 004Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	DVCHG	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b14 to b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b15	DVCHG	设备状态更改	0：禁止写入USBADDR.STSRECOV[3:0]和USBADDR.USBADDR[6:0]位1：允许写入USBADDR.STSRECOV[3:0]和USBADDR.USBADDR[6:0]位。	R/W

有关详细信息，请参阅第32.3.1.5节，由于USB挂起恢复中断而从深度软件待机模式中释放。

32.2.20 USB Address Register (USBADDR)

Address(es): USBFS.USBADDR 4009 0050h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	STSRECOV[3:0]				—	USBADDR[6:0]						
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b6 to b0	USBADDR[6:0]	USB Address	In device controller mode, these bits indicate the USB address assigned by the host when the USBFS processed the SET_ADDRESS request successfully.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b11 to b8	STSRECOV[3:0]	Status Recovery	• Recovery in device controller mode b11 b8 1 0 0 1: Return to the full-speed state (bits DVSTCTR0.RHST[2:0] = 010b), bits INTSTS0.DVSQ[2:0] = 001b (default state) 1 0 1 0: Return to the full-speed state (bits DVSTCTR0.RHST[2:0] = 010b), bits INTSTS0.DVSQ[2:0] = 010b (address state) 1 0 1 1: Return to the full-speed state (bits DVSTCTR0.RHST[2:0] = 010b), bits INTSTS0.DVSQ[2:0] = 011b (configured state). Other settings are prohibited. • Recovery in host controller mode b11 b8 0 1 0 0: Return to the low-speed state (bits DVSTCTR0.RHST[2:0] = 001b) 1 0 0 0: Return to the full-speed state (bits DVSTCTR0.RHST[2:0] = 010b). Other settings are prohibited.	R/W
b15 to b12	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

USBADDR[6:0] bits (USB Address)

In device controller mode, the USBADDR[6:0] flags indicate the USB address received when the USBFS processed a SetAddress request successfully. The USBFS sets the USBADDR[6:0] bits to 00h on detecting a USB bus reset.

Writing to these bits is enabled while the DVCHGR.DVCHG bit is set to 1. On recovering from a USB power shut-off, the operation can resume from the USB address set before the software shut-off.

In host controller mode, the USBADDR[6:0] bits are invalid.

STSRECOV[3:0] bits (Status Recovery)

Use the STSRECOV[3:0] bits to resume the state of the internal sequencer on recovering from USB power shut-off. For details, see section 32.3.1.5, Release from deep software standby mode because of USB suspend/resume interrupts.

Writing to these bits is enabled while the DVCHGR.DVCHG bit is set to 1.

32.2.20 USB地址寄存器(USBADDR)

Address(es): USBFS.USBADDR 4009 0050h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	STSRECOV[3:0]				—	USBADDR[6:0]						
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b6 to b0	USBADDR[6:0]	USB地址	在设备控制器模式下，这些位指示USBFS成功处理SET_ADDRESS请求时主机分配的USB地址。	R/W
b7	—	Reserved	该位读取为0。写入值应为0。	R/W
b11 to b8	STSRECOV[3:0]	状态恢复	在设备控制器模式下恢复b11b81001：返回全速状态（位DVSTCTR0.RHST[2:0]=010b），位INTSTS0.DVSQ[2:0]=001b（默认状态）1010：返回全速状态（位DVSTCTR0.RHST[2:0]=010b），位INTSTS0.DVSQ[2:0]=010b（地址状态）1011：返回全速速度状态（位DVSTCTR0.RHST[2:0]=010b），位INTSTS0.DVSQ[2:0]=011b（配置状态）。禁止其他设置。 在主机控制器模式下恢复b11b80100：返回低速状态（位DVSTCTR0.RHST[2:0]=001b）1000：返回全速状态（位DVSTCTR0.RHST[2:0]=010b)。禁止其他设置。	R/W
b15 to b12	—	Reserved	这些位被读取为0。写入值应为0。	R/W

USBADDR[6:0]位（USB地址）

在设备控制器模式下，USBADDR[6:0]标志指示当USBFS处理一个SetAddress请求成功。USBFS在检测到USB总线复位时将USBADDR[6:0]位设置为00h。

当DVCHGR.DVCHG位设置为1时，允许写入这些位。从USB电源关闭恢复后，操作可以从软件关闭前设置的USB地址恢复。

在主机控制器模式下，USBADDR[6:0]位无效。

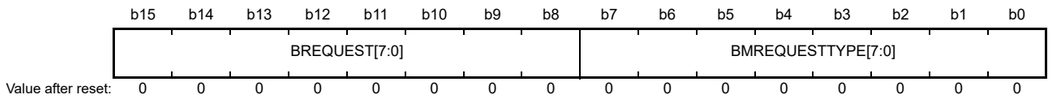
STSRECOV[3:0]位（状态恢复）

使用STSRECOV[3:0]位在从USB电源关闭恢复时恢复内部定序器的状态。有关详细信息，请参阅第32.3.1.5节，由于USB挂起恢复中断而从深度软件待机模式中释放。

当DVCHGR.DVCHG位设置为1时，可以写入这些位。

32.2.21 USB Request Type Register (USBREQ)

Address(es): USBFS.USBREQ 4009 0054h



Bit	Symbol	Bit name	Description	R/W
b7 to b0	BMREQUESTTYPE[7:0]	Request Type	USB request bmRequestType value	R/W *1
b15 to b8	BREQUEST[7:0]	Request	USB request bRequest value	R/W *1

Note 1. In device controller mode, these bits can be read, but writing to them has no effect. In host controller mode, these bits are both read/write bits.

USBREQ stores setup requests for control transfers.

In device controller mode, the USBREQ stores the received bRequest and bmRequestType values. In host controller mode, it sets to the bRequest and bmRequestType values to be transmitted.

USBREQ is initialized by a USB bus reset.

BMREQUESTTYPE[7:0] bits (Request Type)

The BMREQUESTTYPE[7:0] bits hold the bmRequestType value of USB requests.

- In host controller mode:
  Set these bits to the value of the USB request data in transmission setup transactions. Do not change the value of the bits while the DCPCTR.SUREQ bit is 1.
- In device controller mode:
  These bits indicate the value of the USB request data in reception setup transactions. Writing to the bits has no effect.

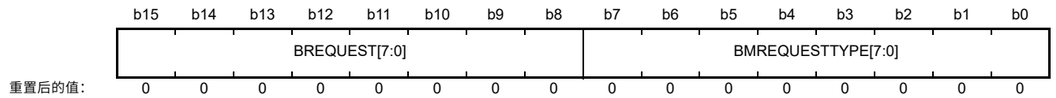
BREQUEST[7:0] bits (Request)

The BREQUEST[7:0] bits store bRequest value of the USB request.

- In host controller mode:
  Set these bits to the value of the USB request data in setup transmission transactions. Do not change the value of the bits while the DCPCTR.SUREQ bit is 1.
- In device controller mode:
  These bits indicate the value of the USB request data in reception setup transactions. Writing to the bits has no effect.

32.2.21 USB请求类型寄存器(USBREQ)

Address(es): USBFS.USBREQ 4009 0054h



Bit	Symbol	位名称	Description	R/W
b7 to b0	BMREQUESTTYPE[7:0]	请求类型	USB请求bmRequestType值	R/W *1
b15 to b8	BREQUEST[7:0]	Request	USB请求bRequest值	R/W *1

Note 1. 在设备控制器模式下，可以读取这些位，但写入它们无效。在主机控制器模式下，这些位都是读写位。

USBREQ存储控制传输的设置请求。

在设备控制器模式下，USBREQ存储接收到的bRequest和bmRequestType值。在主机控制器模式下，它设置为要传输的bRequest和bmRequestType值。

USBREQ由USB总线复位初始化。

BMREQUESTTYPE[7:0]位（请求类型）

BMREQUESTTYPE[7:0]位保存USB请求的bmRequestType值。

- 在主机控制器模式下：
  在传输设置事务中将这些位设置为USB请求数据的值。当DCPCTR.SUREQ位为1时，不要更改位的值。
- 在设备控制器模式下：
  这些位指示接收设置事务中USB请求数据的值。写入位无效。

BREQUEST[7:0]位（请求）

BREQUEST[7:0]位存储USB请求的bRequest值。

- 在主机控制器模式下：
  在设置传输事务中将这些位设置为USB请求数据的值。当DCPCTR.SUREQ位为1时，不要更改位的值。
- 在设备控制器模式下：
  这些位指示接收设置事务中USB请求数据的值。写入位无效。

32.2.22 USB Request Value Register (USBVAL)

Address(es): USBFS.USBVAL 4009 0056h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	WVALUE[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b15 to b0	WVALUE[15:0]	Value	USB request wValue value	R/W *1

Note 1. In device controller mode, these bits can be read, but writing to them has no effect. In host controller mode, these bits are both read/write bits.

In device controller mode, USBVAL stores the received wValue value. In host controller mode, it sets to the wValue value to be transmitted is set.

USBVAL is initialized by a USB bus reset.

WVALUE[15:0] bits (Value)

The WVALUE[15:0] bits store wValue value of the USB request.

- In host controller mode:
  Set these bits to the value of the wValue field in USB requests of transmission setup transactions. Do not change the value of the bits while the DCPCTR.SUREQ bit is 1.
- In device controller mode:
  These bits indicate the wValue value of USB requests in reception setup transactions. Writing to the bits has no effect.

32.2.23 USB Request Index Register (USBINDX)

Address(es): USBFS.USBINDX 4009 0058h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	WINDEX[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b15 to b0	WINDEX[15:0]	Index	USB request wIndex value	R/W *1

Note 1. In device controller mode, these bits can be read, but writing to them has no effect. In host controller mode, these bits are both read/write bits.

USBINDX stores setup requests for control transfers.

In device controller mode, it stores the received wIndex value. In host controller mode, it sets to the wIndex value to be transmitted.

USBINDX is initialized by a USB bus reset.

WINDEX[15:0] bits (Index)

The WINDEX[15:0] bits hold the wIndex value of a USB request.

32.2.22 USB请求值寄存器(USBVAL)

Address(es): USBFS.USBVAL 4009 0056h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	WVALUE[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b15 to b0	WVALUE[15:0]	Value	USB请求wValue值	R/W *1

Note 1. 在设备控制器模式下，可以读取这些位，但写入它们无效。在主机控制器模式下，这些位都是读写位。

在设备控制器模式下，USBVAL存储接收到的wValue值。在主机控制器模式下，它设置为要传输的wValue值。

USBVAL由USB总线复位初始化。

WVALUE[15:0]位（值）

WVALUE[15:0]位存储USB请求的wValue值。

- 在主机控制器模式下：
  将这些位设置为USB传输设置事务请求中wValue字段的值。当DCPCTR.SUREQ位为1时，不要更改位的值。
- 在设备控制器模式下：
  这些位指示接收设置事务中USB请求的wValue值。写入位无效。

32.2.23 USB请求索引寄存器(USBINDX)

Address(es): USBFS.USBINDX 4009 0058h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	WINDEX[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b15 to b0	WINDEX[15:0]	Index	USB请求wIndex值	R/W *1

Note 1. 在设备控制器模式下，可以读取这些位，但写入它们无效。在主机控制器模式下，这些位都是读写位。

USBINDX存储控制传输的设置请求。

在设备控制器模式下，它存储接收到的wIndex值。在主机控制器模式下，它设置为要传输的wIndex值。

USBINDX由USB总线复位初始化。

WINDEX[15:0]位（索引）

WINDEX[15:0]位保存USB请求的wIndex值。

- In host controller mode:
  Set these bits to the wIndex value in USB requests in transmission setup transactions. Do not change the value of the bits while the DCPCTR.SUREQ bit is 1.
- In device controller mode:
  These bits indicate the wIndex value in USB requests received in reception setup transactions. Writing to the bits has no effect.

32.2.24 USB Request Length Register (USBLENG)

Address(es): USBFS.USBLENG 4009 005Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	WLENTUH[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b15 to b0	WLENTUH[15:0]	Length	USB request wLength value	R/W*1

Note 1. In device controller mode, these bits can be read, but writing to them has no effect. In host controller mode, these bits are both read/write bits.

USBLENG stores setup requests for control transfers.

In device controller mode, the value of wLength that is received is stored. In host controller mode, the value of wLength to be transmitted is set.

USBLENG is initialized by a USB bus reset.

WLENTUH[15:0] bits (Length)

The WLENTUH[15:0] bits hold the wLength value of a USB request.

- In host controller mode:
  Set these bits to the wLength value in USB requests in transmission setup transactions. Do not change the value of the bits while the DCPCTR.SUREQ bit is 1.
- In device controller mode:
  These bits indicate the wLength value in USB requests received in reception setup transactions. Writing to the bits has no effect.

32.2.25 DCP Configuration Register (DCPCFG)

Address(es): USBFS.DCPCFG 4009 005Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	SHTNAK	—	—	DIR	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	DIR	Transfer Direction*1	0: Data receiving direction 1: Data transmitting direction.	R/W
b6, b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	SHTNAK	Pipe Disabled at End of Transfer*1	0: Keep pipe open after transfer ends 1: Disable pipe after transfer ends.	R/W

- 在主机控制器模式下：
  在传输设置事务中将这些位设置为USB请求中的wIndex值。当DCPCTR.SUREQ位为1时，不要更改位的值。
- 在设备控制器模式下：
  这些位指示在接收设置事务中收到的USB请求中的wIndex值。写入位无效。

32.2.24 USB请求长度寄存器(USBLENG)

Address(es): USBFS.USBLENG 4009 005Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	WLENTUH[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b15 to b0	WLENTUH[15:0]	Length	USB请求wLength值	R/W*1

Note 1. 在设备控制器模式下，可以读取这些位，但写入它们无效。在主机控制器模式下，这些位都是读写位。

USBLENG存储控制传输的设置请求。

在设备控制器模式下，存储接收到的wLength的值。在主机控制器模式下，设置要传输的wLength的值。

USBLENG由USB总线复位初始化。

WLENTUH[15:0]位（长度）

WLENTUH[15:0]位保存USB请求的wLength值。

- 在主机控制器模式下：
  在传输设置事务中将这些位设置为USB请求中的wLength值。当DCPCTR.SUREQ位为1时，不要更改位的值。
- 在设备控制器模式下：
  这些位指示在接收设置事务中收到的USB请求中的wLength值。写入位无效。

32.2.25 DCP配置寄存器(DCPCFG)

Address(es): USBFS.DCPCFG 4009 005Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	SHTNAK	—	—	DIR	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b3 to b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b4	DIR	转移方向 *1	0：数据接收方向1：数据发送方向。	R/W
b6, b5	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b7	SHTNAK	传输结束时禁用管道 *1	0：传输结束后保持管道打开1：传输结束后禁用管道。	R/W

Bit	Symbol	Bit name	Description	R/W
b15 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Only set this bit while the PID is NAK. Before setting this bit, check that the DCPCTR.PBUSY bit is 0, and then change the DCPCTR.PID[1:0] bits for the DCP from BUF to NAK. If the PID[1:0] bits are changed to NAK by the USBFS, checking the PBUSY bit through the software is not necessary.

DIR bit (Transfer Direction)

In host controller mode, the DIR bit sets the transfer direction of the data stage and status stage for control transfers. In device controller mode, set the DIR bit to 0.

SHTNAK bit (Pipe Disabled at End of Transfer)

The SHTNAK bit specifies whether to change PID to NAK on transfer end when the selected pipe is receiving. It is only valid when the selected pipe is receiving.

When the SHTNAK bit is 1, the USBFS changes the DCPCTR.PID[1:0] bits for the DCP to NAK on determining that a transfer has ended. The USBFS determines transfer end on the following condition:

- A short packet, including a zero-length packet, is successfully received.

32.2.26 DCP Maximum Packet Size Register (DCPMAXP)

Address(es): USBFS.DCPMAXP 4009 005Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	DEVSEL[3:0]				—	—	—	—	—	MXPS[6:0]						
Value after reset:	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b6 to b0	MXPS[6:0]	Maximum Packet Size*1	Maximum data payload specification (maximum packet size) for the DCP	R/W
b11 to b7	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15 to b12	DEVSEL[3:0]	Device Select*2	b15 b12 0 0 0 0: Address 0000b 0 0 0 1: Address 0001b 0 0 1 0: Address 0010b 0 0 1 1: Address 0011b 0 1 0 0: Address 0100b 0 1 0 1: Address 0101b. Other settings are prohibited.	R/W

Note 1. Only set the MXPS[6:0] bits while PID is NAK. Before setting these bits, check that the DCPCTR.PBUSY bit is 0, and then change the DCPCTR.PID[1:0] bits for the DCP from BUF to NAK. If the PID[1:0] bits are changed to NAK by the USBFS, checking the PBUSY bit through the software is not necessary. After the MXPS[6:0] bits are set and the DCP is set to the CURPIPE[3:0] bits in a port select register, clear the buffer by setting the BCLR bit in the port control register to 1.

Note 2. Only set the DEVSEL[3:0] bits while PID is NAK and the DCPCTR.SUREQ bit is 0. Before setting these bits, check that the DCPCTR.PBUSY bit is 0, and then change the DCPCTR.PID[1:0] bits for the DCP from BUF to NAK. If the PID[1:0] bits are changed to NAK by the USBFS, checking the PBUSY bit through the software is not necessary.

MXPS[6:0] bits (Maximum Packet Size)

The MXPS[6:0] bits specify the maximum data payload (maximum packet size) for the DCP. The initial value is 40h (64 bytes). Set the bits to a USB 2.0-compliant value. Do not write to the FIFO buffer or set PID = BUF while MXPS[6:0] is set to 0.

DEVSEL[3:0] bits (Device Select)

In host controller mode, the DEVSEL[3:0] bits specify the address of the target peripheral device for a control transfer. Set up the device address in the associated DEVADDn (n = 0 to 5) register first, and then set these bits to the corresponding value. To set the DEVSEL[3:0] bits to 0010b, for example, first set the address in the DEVADD2 register.

Bit	Symbol	位名称	Description	R/W
b15 to b8	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 仅在PID为NAK时设置该位。在设置该位之前，请检查DCPCTR.PBUSY位是否为0，然后将DCP的DCPCTR.PID[1:0]位从BUF更改为NAK。如果PID[1:0]位被USBFS更改为NAK，则检查
PBUSY位不需要通过软件。

DIR位（传输方向）

在主机控制器模式下，DIR位设置控制传输的数据阶段和状态阶段的传输方向。在设备控制器模式下，将DIR位设置为0。

SHTNAK位（传输结束时管道禁用）

SHTNAK位指定当所选管道正在接收时，是否在传输结束时将PID更改为NAK。仅在所选管道正在接收时有效。

当SHTNAK位为1时，USBFS在确定传输已结束时将DCPCR.PID[1:0]位更改为DCP为NAK。USBFS在以下条件下确定传输结束：

- 成功接收到一个短数据包，包括一个长度为零的数据包。

32.2.26 DCP最大数据包大小寄存器(DCPMAXP)

Address(es): USBFS.DCPMAXP 4009 005Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	DEVSEL[3:0]				—	—	—	—	—	MXPS[6:0]						
重置后的值：	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b6 to b0	MXPS[6:0]	最大数据包大小 *1	最大数据有效载荷规范（最大数据包大小） DCP	R/W
b11 to b7	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b15 to b12	DEVSEL[3:0]	设备选择 *2	b15b120000：地址0000b0 001：地址0001b0010：地 址0010b0011：地址0011b0 100：地址0100b0101：地 址0101b。禁止其他设置。	R/W

Note 1. 仅在PID为NAK时设置MXPS[6:0]位。在设置这些位之前，请检查DCPCTR.PBUSY位是否为0，然后将DCP的DCPCTR.PID[1:0]位从BUF更改为NAK。如果PID[1:0]位被USBFS更改为NAK，则无需通过软件检查PBUSY位。在设置MXPS[6:0]位并将DCP设置为端口选择寄存器中的CURPIPE[3:0]位后，通过将端口控制寄存器中的BCLR位设置为1来清除缓冲区。

Note 2. 仅在PID为NAK且DCPCTR.SUREQ位为0时设置DEVSEL[3:0]位。在设置这些位之前，请检查DCPCTR.PBUSY位是否为0，然后更改DCPCTR.PID[1:0]从BUF到NAK的DCP位。如果PID[1:0]位被USBFS更改为NAK，则无需通过软件检查PBUSY位。

MXPS[6:0]位（最大数据包大小）

MXPS[6:0]位指定DCP的最大数据有效载荷（最大数据包大小）。初始值为40h（64字节）。将这些位设置为符合USB2.0的值。当MXPS[6:0]设置为0时，不要写入FIFO缓冲区或设置PID=BUF。

DEVSEL[3:0]位（设备选择）

在主机控制器模式下，DEVSEL[3:0]位指定目标外围设备的地址以进行控制传输。首先在相关的DEVADDn（n=0到5）寄存器中设置设备地址，然后将这些位设置为相应的值。例如，要将DEVSEL[3:0]位设置为0010b，首先要设置DEVADD2寄存器中的地址。

In device controller mode, set these bits to 0000b.

32.2.27 DCP Control Register (DCPCTR)

Address(es): USBFS.DCPCTR 4009 0060h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BSTS	SUREQ	—	—	SUREQ CLR	—	—	SQCLR	SQSET	SQMON	PBUSY	—	—	CCPL	PID[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	PID[1:0]	Response PID	b1 b0 0 0: NAK response 0 1: BUF response (depends on the buffer state) 1 0: STALL response 1 1: STALL response.	R/W
b2	CCPL	Control Transfer End Enable	0: Disable control transfer completion 1: Enable control transfer completion.	R/W
b4, b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b5	PBUSY	Pipe Busy	0: DCP not used for the USB bus 1: DCP in use for the USB bus.	R
b6	SQMON	Sequence Toggle Bit Monitor	0: DATA0 1: DATA1.	R
b7	SQSET	Sequence Toggle Bit Set*2	Sets the sequence toggle bit in DCP transfers. 0: Invalid (writing 0 has no effect) 1: Set the expected value for the next transaction to DATA1. This bit is read as 0.	R/W*1
b8	SQCLR	Sequence Toggle Bit Clear*2	Clears the sequence toggle bit in DCP transfers. 0: Invalid (writing 0 has no effect) 1: Clear the expected value for the next transaction to DATA0. This bit is read as 0.	R/W*1
b10, b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b11	SUREQCLR	SUREQ Bit Clear	Clears the SUREQ bit in host controller mode. 0: Invalid (writing 0 has no effect) 1: Clear SUREQ to 0. This bit is read as 0.	R/W
b13, b12	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b14	SUREQ	Setup Token Transmission	Sets up token transmission in host controller mode. 0: Invalid (writing 0 has no effect) 1: Transmit setup packet.	R/W
b15	BSTS	Buffer Status	0: Buffer access disabled 1: Buffer access enabled.	R

Note 1. This bit is read as 0.
Note 2. Only set the SQSET and SQCLR bits while PID is NAK. Before setting these bits, check that the PBUSY bit is 0, and then change the PID[1:0] bits for the DCP from BUF to NAK. If the PID[1:0] bits are changed to NAK by the USBFS, checking the PBUSY bit through the software is not necessary.

PID[1:0] bits (Response PID)

The PID[1:0] bits control the USB response type during control transfers.

In host controller mode, to change the PID[1:0] setting from NAK to BUF:

- When the transmitting direction is set:

在设备控制器模式下，将这些位设置为0000b。

32.2.27 DCP控制寄存器(DCPCTR)

Address(es): USBFS.DCPCTR 4009 0060h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BSTS	SUREQ	—	—	SUREQ CLR	—	—	SQCLR	SQSET	SQMON	PBUSY	—	—	CCPL	PID[1:0]	
重置后的值：	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0

Bit	Symbol	位名称		Description	R/W
b1, b0	PID[1:0]	响应PID		b1b000：NAK响应01：BUF响应（取决于缓冲区状态）10：STALL响应11：STALL响应。	R/W
b2	CCPL	控制传输结束使能		0：禁用控制传输完成1：启用控制传输完成。	R/W
b4, b3	—	Reserved		这些位被读取为0。写入值应为0。	R/W
b5	PBUSY	管道忙		0：USB总线不使用DCP1：USB总线使用DCP。	R
b6	SQMON	序列切换位监视器		0: DATA0 1: DATA1.	R
b7	SQSET	序列切换位设置	*2	设置DCP传输中的序列切换位。0：无效（写0无效）1：将下一笔交易的期望值设置为DATA1。 该位读为0。	R/W*1
b8	SQCLR	序列切换位清除	*2	清除DCP传输中的序列切换位。0：无效（写0无效）1：清除下一笔交易的期望值到DATA0。 该位读为0。	R/W*1
b10, b9	—	Reserved		这些位被读取为0。写入值应为0。	R/W
b11	SUREQCLR	SUEQ位清零		在主机控制器模式下清除SUREQ位。0：无效（写0无效）1：将SUREQ清0。该位读为0。	R/W
b13, b12	—	Reserved		这些位被读取为0。写入值应为0。	R/W
b14	SUREQ	设置令牌传输		在主机控制器模式下设置令牌传输。0：无效（写0无效）1：发送设置包。	R/W
b15	BSTS	缓冲区状态		0：禁止缓冲区访问1：允许缓冲区访问。	R

Note 1. 该位读为0。
Note 2. 仅在PID为NAK时设置SQSET和SQCLR位。在设置这些位之前，请检查PBUSY位是否为0，然后将DCP的PID[1:0]位从BUF更改为NAK。如果PID[1:0]位被USBFS更改为NAK，则无需通过软件检查PBUSY位。

PID[1:0]位（响应PID）

PID[1:0]位在控制传输期间控制USB响应类型。

在主机控制器模式下，要将PID[1:0]设置从NAK更改为BUF：

- 设置传输方向时：

a. Write all of the transmit data to the FIFO buffer while the DVSTCTR0.UACT bit is 1 and PID is NAK.

b. Set PID[1:0] bits to 01b (BUF).
The USBFS then executes the OUT transaction.

- When the receiving direction is set:

a. Check that the FIFO buffer is empty (or empty the buffer) while the DVSTCTR0.UACT bit is 1 and PID is NAK.

b. Set PID[1:0] bits to 01b (BUF).
The USBFS then executes the IN transaction.

The USBFS changes the PID[1:0] setting as follows:

- When the PID[1:0] bits are set to BUF (01b) by software and the USBFS has received data exceeding MaxPacketSize, the USBFS sets the PID[1:0] to STALL (11b)
- When a reception error, such as a CRC error, is detected three times consecutively, the USBFS sets the PID[1:0] bits to NAK (00b)
- On receiving the STALL handshake, the USBFS sets PID[1:0] to STALL (11b).

In device controller mode, the USBFS changes the PID[1:0] setting as follows:

- On receiving a setup packet, the USBFS sets PID[1:0] to NAK (00b). The USBFS then sets the INTSTS0.VALID flag to 1, and the PID[1:0] setting cannot be changed until the software clears the VALID flag to 0.
- When the PID[1:0] bits are set to BUF (01b) by software and the USBFS has received data exceeding MaxPacketSize, the USBFS sets PID[1:0] to STALL (11b)
- On detecting a control transfer sequence error, the USBFS sets PID[1:0] to STALL (1xb)
- On detecting a USB bus reset, the USBFS sets PID[1:0] to NAK.

The USBFS does not check the PID[1:0] setting while processing a SET_ADDRESS request.

The PID[1:0] bits are initialized by a USB bus reset.

CCPL bit (Control Transfer End Enable)

In device controller mode, setting the CCPL bit to 1 enables the status stage of the control transfer to be completed. When the bit is set to 1 by software while the associated PID[1:0] bits are set to BUF, the USBFS completes the control transfer status stage.

During control read transfers, the USBFS transmits the ACK handshake in response to the OUT transaction from the USB host. During control write or no-data control transfers, it transmits the zero-length packet in response to the IN transaction from the USB host. On detecting a SET_ADDRESS request, the USBFS operates in auto response mode from the setup stage up to status stage completion regardless of the CCPL bit setting.

The USBFS changes the CCPL bit from 1 to 0 on receiving a new setup packet. The software cannot write 1 to the bit while the INTSTS0.VALID bit is 1. The bit is initialized by a USB bus reset.

In host controller mode, always write 0 to the CCPL bit.

PBUSY bit (Pipe Busy)

The PBUSY bit indicates whether DCP is used for the transaction when USBFS changes the PID[1:0] bits from BUF to NAK. The USBFS changes the PBUSY bit from 0 to 1 on start of a USB transaction for the selected pipe. It changes the PBUSY bit from 1 to 0 on completion of one transaction.

After PID is set to NAK by software, the value in the PBUSY bit indicates whether changes to pipe settings can proceed.

For details, see section 32.3.4.1, Pipe control register switching procedures.

SQMON bit (Sequence Toggle Bit Monitor)

The SQMON bit indicates the expected value of the sequence toggle bit for the next transaction during a DCP transfer.

The USBFS toggles the bit on normal completion of the transaction. It does not toggle the bit, however, when a DATA-PID mismatch occurs during a transfer in the receiving direction.

一个。当DVSTCTR0.UACT位为1且PID为NAK时，将所有发送数据写入FIFO缓冲区。

湾。将PID[1:0]位设置为01b(BUF)。
然后USBFS执行OUT事务。

- 设置接收方向时：

一个。在DVSTCTR0.UACT位为1且PID为NAK时检查FIFO缓冲区是否为空（或清空缓冲区）。

湾。将PID[1:0]位设置为01b(BUF)。
然后USBFS执行IN事务。

USBFS更改PID[1:0]设置如下：

- 当PID[1:0]位被软件设置为BUF(01b)并且USBFS接收到的数据超过MaxPacketSize，USBFS将PID[1:0]设置为STALL(11b)
- 当连续3次检测到接收错误（例如CRC错误）时，USBFS将PID[1:0]位设置为NAK(00b)
- 在接收到STALL握手时，USBFS将PID[1:0]设置为STALL(11b)。

在设备控制器模式下，USBFS将PID[1:0]设置更改如下：

- 接收到设置数据包后，USBFS将PID[1:0]设置为NAK(00b)。然后USBFS将INTSTS0.VALID标志设置为1，并且在软件将VALID标志清除为0之前无法更改PID[1:0]设置。
- 当PID[1:0]位被软件设置为BUF(01b)并且USBFS接收到的数据超过MaxPacketSize，USBFS将PID[1:0]设置为STALL(11b)
- 在检测到控制传输序列错误时，USBFS将PID[1:0]设置为STALL(1xb)
- 在检测到USB总线复位时，USBFS将PID[1:0]设置为NAK。

USBFS在处理SET_ADDRESS请求时不检查PID[1:0]设置。

PID[1:0]位由USB总线复位初始化。

CCPL位（控制传输结束使能）

在设备控制器模式下，将CCPL位设置为1可以完成控制传输的状态阶段。
当该位由软件设置为1且相关的PID[1:0]位设置为BUF时，USBFS完成控制传输状态阶段。

在控制读取传输期间，USBFS发送ACK握手以响应来自USB主机的OUT事务。在控制写入或无数据控制传输期间，它传输零长度数据包以响应来自USB主机的IN事务。在检测到SET_ADDRESS请求时，USBFS从设置阶段到状态阶段完成以自动响应模式运行，无论CCPL位设置如何。

USBFS在接收到新的设置数据包时将CCPL位从1更改为0。当INTSTS0.VALID位为1时，软件无法向该位写入1。该位由USB总线复位初始化。

在主机控制器模式下，始终将0写入CCPL位。

PBUSY位（管道忙）

PBUSY位指示当USBFS将PID[1:0]位从BUF更改为NAK时是否使用DCP进行事务处理。USBFS在所选管道的USB事务开始时将PBUSY位从0更改为1。它改变了
PBUSY位在一个事务完成时从1变为0。

在软件将PID设置为NAK后，PBUSY位中的值指示是否可以继续对管道设置进行更改。

详见32.3.4.1管道控制寄存器切换流程。

SQMON位（序列切换位监视器）

SQMON位指示DCP传输期间下一个事务的序列切换位的预期值。

USBFS在事务正常完成时切换该位。然而，它不会切换该位，当一个DATA
PID不匹配发生在接收方向的传输过程中。

In device controller mode, the USBFS sets the SQMON bit to 1 (specifies DATA1 as the expected value) on successful reception of the setup packet.

In device controller mode, the USBFS does not reference this bit during IN or OUT transactions at the status stage, and it does not toggle the bit on normal completion.

SQSET bit (Sequence Toggle Bit Set)

The SQSET bit specifies DATA1 as the expected value of the sequence toggle bit for the next transaction during a DCP transfer.

Do not set the SQCLR and SQSET bits to 1 simultaneously.

SQCLR bit (Sequence Toggle Bit Clear)

The SQCLR bit specifies DATA0 as the expected value of the sequence toggle bit for the next transaction during a DCP transfer. It is read as 0.

Do not set the SQCLR and SQSET bits to 1 simultaneously.

SUREQCLR bit (SUREQ Bit Clear)

In host controller mode, setting the SUREQCLR bit to 1 clears the SUREQ bit to 0. The bit is read as 0.

If transfer stops while the SUREQ bit is set to 1 in a setup transaction, set the SUREQCLR bit to 1 by software. This is not necessary at the end of a normal setup transaction, because the USBFS automatically clears the SUREQ bit to 0.

Only control the SUREQ bit through the SUREQCLR bit while the DVSTCTR0.UACT bit is 0. When UACT is 0, communication is halted or no transfer is occurring because a bus disconnection was detected.

In device controller mode, always write 0 to this bit.

SUREQ bit (Setup Token Transmission)

In host controller mode, setting the SUREQ bit to 1 triggers the USBFS to transmit the setup packet. After completing the setup transaction process, the USBFS generates either the SACK or SIGN interrupt and clears the SUREQ bit to 0. The USBFS also clears the SUREQ bit to 0 when the software sets the SUREQCLR bit to 1.

Before setting the SUREQ bit to 1, set the DCPMAXP.DEVSEL[3:0] bits, USBREQ, USBVAL, USBINDX, and USBLENG appropriately to transmit the target USB request in the setup transaction. Also check that the PID[1:0] bits for the DCP are set to NAK. After setting the SUREQ bit to 1, do not change the DCPMAXP.DEVSEL[3:0] bits, USBREQ, USBVAL, USBINDX, or USBLENG until the setup transaction is complete (SUREQ bit = 1). Write 1 to the SUREQ bit only when transmitting the setup token. Otherwise, write 0.

In device controller mode, always write 0 to this bit.

BSTS flag (Buffer Status)

The BSTS flag indicates the status of access to the DCP FIFO buffer. The meaning of this flag varies as follows depending on the CFIFOSEL.ISEL setting:

- When ISEL = 0, the bit indicates whether receive data can be read from the buffer
- When ISEL = 1, the bit indicates whether transmit data can be written to the buffer.

在设备控制器模式下，USBFS在成功接收到设置数据包时将SQMON位设置为1（指定DATA1作为预期值）。

在设备控制器模式下，USBFS在状态阶段的IN或OUT事务期间不引用该位，并且它不会在正常完成时切换该位。

SQSET位（序列切换位设置）

SQSET位将DATA1指定为DCP传输期间下一个事务的序列切换位的预期值。

不要同时将SQCLR和SQSET位设置为1。

SQCLR位（序列切换位清除）

SQCLR位将DATA0指定为DCP传输期间下一个事务的序列切换位的预期值。读为0。

不要同时将SQCLR和SQSET位设置为1。

SUREQCLR位（SUREQ位清零）

在主机控制器模式下，将SUREQCLR位设置为1会将SUREQ位清除为0。该位被读取为0。

如果在设置事务中将SUREQ位设置为1时传输停止，则通过软件将SUREQCLR位设置为1。这在正常设置事务结束时不是必需的，因为USBFS会自动将SUREQ位清除为0。

当DVSTCTR0.UACT位为0时，仅通过SUREQCLR位控制SUREQ位。当UACT为0时，由于检测到总线断开，通信停止或没有传输发生。

在设备控制器模式下，始终向该位写入0。

SUREQ位（设置令牌传输）

在主机控制器模式下，将SUREQ位设置为1会触发USBFS发送设置数据包。完成设置事务处理后，USBFS产生SACK或SIGN中断并将SUREQ位清零。当软件将SUREQCLR位设置为1时，USBFS也将SUREQ位清零。

在将SUREQ位设置为1之前，适当地设置DCPMAXP.DEVSEL[3:0]位、USBREQ、USBVAL、USBINDX和USBLENG以在设置事务中传输目标USB请求。还要检查DCP的PID[1:0]位是否设置为NAK。将SUREQ位设置为1后，在设置事务完成（SUREQ位=1）之前，不要更改DCPMAXP.DEVSEL[3:0]位、USBREQ、USBVAL、USBINDX或USBLENG。将1写入

仅在发送设置令牌时才使用SUEQ位。否则，写0。

在设备控制器模式下，始终向该位写入0。

BSTS标志（缓冲区状态）

BSTS标志指示访问DCPFIFO缓冲区的状态。根据CFIFOSEL.ISEL设置，该标志的含义如下：

- 当ISEL=0时，该位指示是否可以从缓冲区中读取接收数据
- 当ISEL=1时，该位指示是否可以将发送数据写入缓冲区。

32.2.28 Pipe Window Select Register (PIPESEL)

Address(es): USBFS.PIPESEL 4009 0064h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	PIPESEL[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	PIPESEL[3:0]	Pipe Window Select	b3 b0 0 0 0 0: No pipe selected 0 0 0 1: Pipe 1 0 0 1 0: Pipe 2 0 0 1 1: Pipe 3 0 1 0 0: Pipe 4 0 1 0 1: Pipe 5 0 1 1 0: Pipe 6 0 1 1 1: Pipe 7 1 0 0 0: Pipe 8 1 0 0 1: Pipe 9. Other settings are prohibited.	R/W
b15 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Set pipes 1 to 9 using the PIPESEL, PIPECFG, PIPEMAXP, PIPEPERI, PIPEnCTR, PIPEnTRE, and PIPEnTRN registers (n = 0 to 9).

After selecting the pipe in the PIPESEL register, pipe functions must be set in the associated PIPECFG, PIPEMAXP, and PIPEPERI registers. PIPEnCTR, PIPEnTRE, and PIPEnTRN can be set independently of the pipe selection in this register.

PIPESEL[3:0] bits (Pipe Window Select)

The PIPESEL[3:0] bits select the pipe number associated with the PIPECFG, PIPEMAXP, and PIPEPERI registers used for data writing and reading. Selecting a pipe number in the PIPESEL[3:0] bits allows writing to and reading from PIPECFG, PIPEMAXP, and PIPEPERI associated with the selected pipe number.

When PIPESEL[3:0] = 0000b, 0 is read from all of the bits in PIPECFG, PIPEMAXP, and PIPEPERI. Writing to these bits has no effect.

32.2.29 Pipe Configuration Register (PIPECFG)

Address(es): USBFS.PIPECFG 4009 0068h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TYPE[1:0]		—	—	—	BFRE	DBLB	—	SHTNAK	—	—	DIR	EPNUM[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	EPNUM[3:0]	Endpoint Number*1	Specifies the endpoint number for the selected pipe. Setting 0000b indicates that the pipe is not used.	R/W
b4	DIR	Transfer Direction*2,*3	0: Receiving direction 1: Transmitting direction.	R/W
b6, b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	SHTNAK	Pipe Disabled at End of Transfer*1	0: Continue pipe operation after transfer ends 1: Disable pipe after transfer ends.	R/W
b8	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

32.2.28 管道窗口选择寄存器(PIPESEL)

Address(es): USBFS.PIPESEL 4009 0064h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	PIPESEL[3:0]			
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b3 to b0	PIPESEL[3:0]	管道窗口选择	b3b00000：未选择管道000 1：管道10010：管道20011 ：管道30100：管道40101： 管道50110：管道60111：管 道71000：管道81001：管道 9。禁止其他设置。	R/W
b15 to b4	—	Reserved	这些位被读取为0。写入值应为0。	R/W

使用PIPESEL、PIPECFG、PIPEMAXP、PIPEPERI、PIPEnCTR、PIPEnTRE和PIPEnTRN寄存器（n=0到9）设置管道1到9。

在PIPESEL寄存器中选择管道后，必须在相关的PIPECFG、PIPEMAXP和PIPEPERI寄存器。PIPEnCTR、PIPEnTRE和PIPEnTRN可以独立于该寄存器中的管道选择进行设置。

PIPESEL[3:0]位（管道窗口选择）

PIPESEL[3:0]位选择与用于数据写入和读取的PIPECFG、PIPEMAXP和PIPEPERI寄存器相关的管道编号。在PIPESEL[3:0]位中选择一个管道编号允许写入和读取与所选管道编号相关的PIPECFG、PIPEMAXP和PIPEPERI。

当PIPESEL[3:0]=0000b时，从PIPECFG、PIPEMAXP和PIPEPERI中的所有位读取0。写入这些位无效。

32.2.29 管道配置寄存器(PIPECFG)

Address(es): USBFS.PIPECFG 4009 0068h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TYPE[1:0]		—	—	—	BFRE	DBLB	—	SHTNAK	—	—	DIR	EPNUM[3:0]			
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称		Description	R/W
b3 to b0	EPNUM[3:0]	端点编号	*1	指定选定管道的端点编号。 设置0000b表示不使用管道。	R/W
b4	DIR	转移方向	*2,*3	0：接收方向1：发送方 向。	R/W
b6, b5	—	Reserved		这些位被读取为0。写入值应为0。	R/W
b7	SHTNAK	传输结束时禁用管道	*1	0：传输结束后继续管道操作1：传输结束后 禁用管道。	R/W
b8	—	Reserved		该位读取为0。写入值应为0。	R/W

Bit	Symbol	Bit name	Description	R/W
b9	DBLB	Double Buffer Mode*2,*3	0: Single buffer 1: Double buffer.	R/W
b10	BFRE	BRDY Interrupt Operation Specification*2,*3	0: Generate BRDY interrupt on transmitting or receiving data 1: Generate BRDY interrupt on completion of reading data.	R/W
b13 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15, b14	TYPE[1:0]	Transfer Type*1	• Pipes 1 and 2 b15 b14 0 0: Pipe not used 0 1: Bulk transfer 1 0: Setting prohibited 1 1: Isochronous transfer. • Pipes 3 to 5 b15 b14 0 0: Pipe not used 0 1: Bulk transfer 1 0: Setting prohibited 1 1: Setting prohibited. • Pipes 6 to 9 b15 b14 0 0: Pipe not used 0 1: Setting prohibited 1 0: Interrupt transfer 1 1: Setting prohibited.	R/W

Note 1. Only set the TYPE[1:0], SHTNAK, and EPNUM[3:0] bits while PID is NAK. Before setting these bits, check that the PIPEnCTR.PBUSY bit is 0, and then change the PIPEnCTR.PID[1:0] bits from 01b (BUF) to 00b (NAK). If the PID[1:0] bits are changed to 00 (NAK) by the USBFS, checking the PBUSY bit through the software is not necessary.

Note 2. Only set the BFRE, DBLB, and DIR bits while PID is NAK and before the pipe is selected in the CURPIPE[3:0] bits in the port select register. Before setting these bits, check that the PIPEnCTR.PBUSY bit is 0, and then change the PIPEnCTR.PID[1:0] bits from 01b (BUF) to 00b (NAK). If the PID[1:0] bits are changed to 00 (NAK) by the USBFS, checking the PBUSY bit through the software is not necessary.

Note 3. To change the BFRE, DBLB, or DIR bits after completing USB communication on the selected pipe, in addition to the constraints described in Note 2, write 1 and 0 to the PIPEnCTR.ACLRM bit continuously through the software and clear the FIFO buffer assigned to the pipe.

PIPECFG specifies the transfer type, FIFO buffer access direction, and endpoint numbers for pipes 1 to 9. It also selects single or double buffer mode, and whether to continue or disable pipe operation at the end of transfer.

EPNUM[3:0] bits (Endpoint Number)

The EPNUM[3:0] bits specify the endpoint number for the selected pipe. Setting 0000b indicates the pipe not used.

Set these bits so that the combination of the DIR and EPNUM[3:0] settings is different from those for other pipes. The EPNUM[3:0] bits can be set to 0000b for all pipes.

DIR bit (Transfer Direction)

The DIR bit specifies the transfer direction for the selected pipe.

When the software sets this bit to 0, the USBFS uses the selected pipe for receiving. When the software sets this bit to 1, the USBFS uses the selected pipe for transmitting.

SHTNAK bit (Pipe Disabled at End of Transfer)

The SHTNAK bit specifies whether to change the PIPEnCTR.PID[1:0] bits to 00b (NAK) at the end of transfer when the selected pipe is set in the receiving direction. The bit is valid for pipes 1 to 5 in the receiving direction.

When the software sets this bit to 1 for a receiving pipe, the USBFS changes the associated PIPEnCTR.PID[1:0] bits to 00b (NAK) on determining the transfer end. The USBFS determines that the transfer has ended on the following conditions:

- A short packet data (including a zero-length packet) was successfully received

Bit	Symbol	位名称	Description	R/W
b9	DBLB	双缓冲模式 *2,*3	0：单缓冲区1： 双缓冲区。	R/W
b10	BFRE	BRDY中断操作 Specification*2,*3	0：发送或接收数据时产生BRDY中断1：读取数据完成时产生BRDY中断。	R/W
b13 to b11	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b15, b14	TYPE[1:0]	传输类型 *1	管道1和2b15b1400：管道未使用01：批量传输10：设置禁止11：同步传输。 管道3至5b15b1400：管道未使用01：批量传输10：禁止设置11：禁止设置。 管道6至9b15b1400：未使用管道01：禁止设置10：中断传输11：禁止设置。	R/W

Note 1. 仅在PID为NAK时设置TYPE[1:0]、SHTNAK和EPNUM[3:0]位。在设置这些位之前，请检查PIPEnCTR.PBUSY位为0，然后将PIPEnCTR.PID[1:0]位从01b(BUF)更改为00b(NAK)。如果PID[1:0]位被USBFS更改为00(NAK)，则无需通过软件检查PBUSY位。

Note 2. 仅在PID为NAK且在端口选择寄存器的CURPIPE[3:0]位中选择管道之前设置BFRE、DBLB和DIR位。在设置这些位之前，请检查PIPEnCTR.PBUSY位是否为0，然后将PIPEnCTR.PID[1:0]位从01b(BUF)更改为00b(NAK)。如果PID[1:0]位被USBFS更改为00(NAK)，则无需通过软件检查PBUSY位。

Note 3. 要在选定管道上完成USB通信后更改BFRE、DBLB或DIR位，除了注释2中描述的约束外，还可以通过软件连续向PIPEnCTR.ACLRM位写入1和0，并清除分配给管道。

PIPECFG指定管道1到9的传输类型、FIFO缓冲区访问方向和端点编号。它还选择单缓冲区或双缓冲区模式，以及在传输结束时是继续还是禁用管道操作。

EPNUM[3:0]位（端点编号）

EPNUM[3:0]位指定所选管道的端点号。设置0000b表示管道未使用。

设置这些位，以便DIR和EPNUM[3:0]设置的组合不同于其他管道的设置。这
对于所有管道，EPNUM[3:0]位可以设置为0000b。

DIR位（传输方向）

DIR位指定所选管道的传输方向。

当软件将此位设置为0时，USBFS使用所选管道进行接收。当软件将此位设置为1时，USBFS使用所选管道进行传输。

SHTNAK位（传输结束时管道禁用）

SHTNAK位指定当所选管道设置为接收方向时，是否在传输结束时将PIPEnCTR.PID[1:0]位更改为00b(NAK)。该位对接收方向的管道1到5有效。

当软件将该位设置为1用于接收管道时，USBFS在确定传输结束时将相关的PIPEnCTR.PID[1:0]位更改为00b(NAK)。USBFS在以下条件下确定传输已结束：

- 成功接收到一个短包数据（包括一个零长度包）

- The transaction counter is used and the number of packets specified for the transaction counter are successfully received.

DBLB bit (Double Buffer Mode)

The DBLB bit selects either single or double buffer mode for the FIFO buffer used by the selected pipe. The bit is valid for pipes 1 to 5.

BFRE bit (BRDY Interrupt Operation Specification)

The BFRE bit specifies the BRDY interrupt generation timing from the USBFS to the CPU for the selected pipe.

When the software sets the BFRE bit to 1 and the selected pipe is in the receiving direction, the USBFS detects the transfer completion and generates the BRDY interrupt on reading the packet.

When a BRDY interrupt is generated with this setting, the software must write 1 to the BCLR bit in the port control register. The FIFO buffer assigned to the selected pipe is not enabled for reception until 1 is written to the BCLR bit.

When the BFRE bit is set to 1 by software and the selected pipe is in the transmitting direction, the USBFS does not generate the BRDY interrupt. For details, see section 32.3.3.1, BRDY interrupt.

TYPE[1:0] bits (Transfer Type)

The TYPE[1:0] bits specify the transfer type for the pipe selected in the PIPESEL.PIPESEL[3:0] bits. Before setting PID to BUF and starting USB communication on the selected pipe, set the TYPE[1:0] bits to a value other than 00b.

32.2.30 Pipe Maximum Packet Size Register (PIPEMAXP)

Address(es): USBFS.PIPEMAXP 4009 006Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	DEVSEL[3:0]				—	—	—	MXPS[8:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0/1 *1	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b8 to b0	MXPS[8:0]	Maximum Packet Size*2	• Pipes 1 and 2 1 byte (001h) to 256 bytes (100h) • Pipes 3 to 5 8 bytes (008h), 16 bytes (010h), 32 bytes (020h), 64 bytes (040h) (Bits [8:7] and [2:0] not supported.) • Pipes 6 to 9 1 byte (001h) to 64 bytes (040h) (Bits [8:7] not supported.)	R/W
b11 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15 to b12	DEVSEL[3:0]	Device Select*3	b3 b0 0 0 0 0: Address 0000b 0 0 0 1: Address 0001b 0 0 1 0: Address 0010b 0 0 1 1: Address 0011b 0 1 0 0: Address 0100b 0 1 0 1: Address 0101b. Other settings are prohibited.	R/W

Note 1. The value of the MXPS[8:0] bits is 000h when no pipe is selected in the PIPESEL.PIPESEL[3:0] bits and 040h when a pipe is selected.

Note 2. Only set the MXPS[8:0] bits while PID is NAK and before the pipe is selected in the CURPIPE[3:0] bits in the port select register. Before setting these bits, check that the PIPEnCTR.PBUSY bit is 0, and then change the PIPEnCTR.PID[1:0] bits from 01b (BUF) to 00b (NAK). If the PID[1:0] bits are changed to 00 (NAK) by the USBFS, checking the PBUSY bit through the software is not necessary.

Note 3. Only set the DEVSEL[3:0] bits while PID is NAK. Before setting these bits, check that the PIPEnCTR.PBUSY bit is 0, and then change the PIPEnCTR.PID[1:0] bits from 01b (BUF) to 00b (NAK). If the PID[1:0] bits are changed to 00 (NAK) by the USBFS,

- 使用事务计数器并成功接收为事务计数器指定的数据包数量。

DBLB位（双缓冲模式）

DBLB位为所选管道使用的FIFO缓冲区选择单缓冲区模式或双缓冲区模式。该位对管道1到5有效。

BFRE位（BRDY中断操作规范）

BFRE位为所选管道指定从USBFS到CPU的BRDY中断生成时序。

当软件将BFRE位设置为1且所选管道处于接收方向时，USBFS检测到传输完成并在读取数据包时产生BRDY中断。

当使用该设置产生BRDY中断时，软件必须将1写入端口控制寄存器中的BCLR位。在将1写入BCLR位之前，分配给所选管道的FIFO缓冲区不会用于接收。

当BFRE位由软件设置为1且所选管道处于发送方向时，USBFS不会产生BRDY中断。有关详细信息，请参阅第32.3.3.1节，BRDY中断。

TYPE[1:0]位（传输类型）

TYPE[1:0]位指定在PIPESEL.PIPESEL[3:0]位中选择的管道的传输类型。在将PID设置为BUF并在所选管道上启动USB通信之前，请将TYPE[1:0]位设置为00b以外的值。

32.2.30 管道最大数据包大小寄存器(PIPEMAXP)

Address(es): USBFS.PIPEMAXP 4009 006Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	DEVSEL[3:0]				—	—	—	MXPS[8:0]								
重置后的值：	0	0	0	0	0	0	0	0	0	0/1 *1	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b8 to b0	MXPS[8:0]	最大数据包大小 *2	管道1和2 1字节(001h)到256字节(100h) 管道3到5 8字节(008h)、16字节(010h)、32字节(020h)、64字节(040h)（不支持位[8:7]和[2:0]。） 管道6到9 1字节(001h)到64字节(040h)（不支持位[8:7]。）	R/W
b11 to b9	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b15 to b12	DEVSEL[3:0]	设备选择 *3	b3b00000：地址0000b0001：地址0001b0010：地址0010b0011：地址0011b0100：地址0101b。禁止其他设置。	R/W

Note 1. 当在管道中选择未选择管道时，MXPS[8：0]位的值为000H。pipesel[3：0]位和选择管道时040H。

Note 2. 仅在PID为NAK且在端口选择寄存器的CURPIPE[3:0]位中选择管道之前设置MXPS[8:0]位。在设置这些位之前，请检查PIPEnCTR.PBUSY位是否为0，然后将PIPEnCTR.PID[1:0]位从01b(BUF)更改为00b(NAK)。如果PID[1:0]位被USBFS更改为00(NAK)，则无需通过软件检查PBUSY位。

Note 3. 仅在PID为NAK时设置DEVSEL[3:0]位。在设置这些位之前，请检查PIPEnCTR.PBUSY位是否为0，然后将PIPEnCTR.PID[1:0]位从01b(BUF)更改为00b(NAK)。如果PID[1:0]位被USBFS更改为00(NAK)，

checking the PBUSY bit through the software is not necessary.

PIPEMAXP specifies the maximum packet size for pipes 1 to 9.

MXPS[8:0] bits (Maximum Packet Size)

The MXPS[8:0] bits specify the maximum data payload (maximum packet size) for the selected pipe.

Set these bits to the appropriate value for each transfer type based on the USB 2.0 specification. When MXPS[8:0] = 0, do not write to the FIFO buffer or set PID to BUF. These writes have no effect.

DEVSEL[3:0] bits (Device Select)

In host controller mode, the DEVSEL[3:0] bits specify the address of the target device for USB communication. Set up the device address in the associated DEVADDn (n = 0 to 5) register first, and then set these bits to the corresponding value. To set the DEVSEL[3:0] bits to 0010b, for example, first set the address in the DEVADD2 register.

In device controller mode, set these bits to 0000b.

32.2.31 Pipe Cycle Control Register (PIPEPERI)

Address(es): USBFS.PIPEPERI 4009 006Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	IFIS	—	—	—	—	—	—	—	—	—	IITV[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	IITV[2:0] *1	Interval Error Detection Interval	Specifies the interval error detection timing for the selected pipe as the n-th power of 2 of the frame timing	R/W
b11 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b12	IFIS	Isochronous IN Buffer Flush	0: Do not flush buffer 1: Flush buffer.	R/W
b15 to b13	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Only set the IITV[2:0] bits while PID is NAK. Before setting these bits, check that the PBUSY bit is 0, and then change the PID[1:0] bits from 01b (BUF) to 00b (NAK). If the PID[1:0] bits are changed to 00 (NAK) by the USBFS, checking the PBUSY bit through the software is not necessary.

PIPEPERI selects whether the buffer is flushed or not when an interval error occurred during isochronous IN transfers, and sets the interval error detection interval for pipes 1 to 9.

IITV[2:0] bits (Interval Error Detection Interval)

To change the IITV[2:0] bits to another value after they are set and USB communication is performed, set the PIPEnCTR.PID[1:0] bits to 00b (NAK) and then set the PIPEnCTR.ACLRM bit to 1 to initialize the interval timer.

The IITV[2:0] bits are not provided for pipes 3 to 5. Write 000b to bit positions of the IITV[2:0] bits associated with pipes 3 to 5.

IFIS bit (Isochronous IN Buffer Flush)

The IFIS bit specifies whether to flush the buffer when the pipe selected in the PIPESEL.PIPESEL[3:0] bits is used for isochronous IN transfers.

In device controller mode when the selected pipe is for isochronous IN transfers, the USBFS automatically clears the FIFO buffer if the USBFS fails to receive the IN token from the USB host within the interval set in the IITV[2:0] bits in terms of frames.

When double buffering is specified (PIPECFG.DBLB = 1), the USBFS only clears the data in the previously used plane.

The USBFS clears the FIFO buffer on receiving the SOF packet immediately after the frame in which the USBFS

无需通过软件检查PBUSY位。

PIPEMAXP指定管道1到9的最大数据包大小。

MXPS[8:0]位（最大数据包大小）

MXPS[8:0]位指定所选管道的最大数据有效负载（最大数据包大小）。

根据USB2.0规范将这些位设置为每种传输类型的适当值。当MXPS[8:0]=0时，不要写入FIFO缓冲区或将PID设置为BUF。这些写入没有效果。

DEVSEL[3:0]位（设备选择）

在主机控制器模式下，DEVSEL[3:0]位指定USB通信的目标设备的地址。首先在相关的DEVADDn（n=0到5）寄存器中设置设备地址，然后将这些位设置为相应的值。例如，要将DEVSEL[3:0]位设置为0010b，首先要设置DEVADD2寄存器中的地址。

在设备控制器模式下，将这些位设置为0000b。

32.2.31 管道周期控制寄存器(PIPEPERI)

Address(es): USBFS.PIPEPERI 4009 006Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	IFIS	—	—	—	—	—	—	—	—	—	IITV[2:0]		
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b2 to b0	IITV[2:0] *1	间隔错误检测间隔	将所选管道的间隔错误检测时间指定为帧时间的2的n次方	R/W
b11 to b3	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b12	IFIS	同步IN缓冲区刷新	0：不刷新缓冲区1： 刷新缓冲区。	R/W
b15 to b13	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 仅在PID为NAK时设置IITV[2:0]位。在设置这些位之前，请检查PBUSY位是否为0，然后更改PID[1:0]位从01b(BUF)到00b(NAK)。如果PID[1:0]位被USBFS更改为00(NAK)，则无需通过软件检查PBUSY位。

PIPEPERI选择在同步IN传输期间发生间隔错误时是否刷新缓冲区，并设置管道1到9的间隔错误检测间隔。

IITV[2:0]位（间隔错误检测间隔）

要在设置IITV[2:0]位并在执行USB通信后将其更改为另一个值，请设置PIPEnCTR.PID[1:0]位为00b(NAK)，然后将PIPEnCTR.ACLRM位设置为1以初始化间隔定时器。

不为管道3到5提供IITV[2:0]位。将000b写入与管道3到5相关联的IITV[2:0]位的位位置。

IFIS位（同步IN缓冲区刷新）

IFIS位指定当在PIPESEL.PIPESEL[3:0]位中选择的管道用于同步IN传输时是否刷新缓冲区。

在设备控制器模式下，当所选管道用于同步IN传输时，USBFS会自动清除
如果USBFS未能在IITV[2:0]位（以帧为单位）设置的间隔内接收来自USB主机的IN令牌，则FIFO缓冲区。

当指定双缓冲时（PIPECFG.DBLB=1），USBFS只清除先前使用的平面中的数据。

USBFS在接收到SOF数据包的帧之后立即清除FIFO缓冲区

expected to receive the IN token. Even if the SOF packet is corrupted, the FIFO buffer is cleared at the time the SOF packet is expected to be received by using the internal interpolation function.

When the host controller function is selected, set this bit to 0. When the selected pipe is not for isochronous transfer, set this bit to 0.

32.2.32 PIPEn Control Register (PIPEnCTR) (n = 1 to 9)

PIPEnCTR (n = 1 to 5)

Address(es): USBFS.PIPE1CTR 4009 0070h, USBFS.PIPE2CTR 4009 0072h, USBFS.PIPE3CTR 4009 0074h, USBFS.PIPE4CTR 4009 0076h, USBFS.PIPE5CTR 4009 0078h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BSTS	INBUFM	—	—	—	ATREPM	ACLRM	SQCLR	SQSET	SQMON	PBUSY	—	—	—	PID[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	PID[1:0]	Response PID	b1 b0 0 0: NAK response 0 1: BUF response (depends buffer state) 1 0: STALL response 1 1: STALL response.	R/W
b4 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b5	PBUSY	Pipe Busy	0: Pipe n not in use for the transaction 1: Pipe n in use for the transaction.	R
b6	SQMON	Sequence Toggle Bit Confirmation	0: DATA0 1: DATA1.	R
b7	SQSET	Sequence Toggle Bit Set*2	Sets the sequence toggle bit for pipe n. 0: Invalid (writing 0 has no effect) 1: Set the expected value for the next transaction to DATA1. This bit is read as 0.	R/W*1
b8	SQCLR	Sequence Toggle Bit Clear*2	Clears the sequence toggle bit for pipe n. 0: Invalid (writing 0 has no effect) 1: Clear the expected value for the next transaction to DATA0. This bit is read as 0.	R/W*1
b9	ACLRM	Auto Buffer Clear Mode*3	0: Disable 1: Enable (initialize all buffers).	R/W
b10	ATREPM	Auto Response Mode*2	0: Disable auto response mode 1: Enable auto response mode.	R/W
b13 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b14	INBUFM	Transmit Buffer Monitor	0: No data to be transmitted is in the FIFO buffer 1: Data to be transmitted is in the FIFO buffer.	R
b15	BSTS	Buffer Status	0: Buffer access by the CPU disabled 1: Buffer access by the CPU enabled.	R

Note 1. Only 0 can be read.
Note 2. Only set the ATREPM bit or write 1 to the SQCLR or SQSET bit while PID is NAK. Before setting these bits, check that the PBUSY bit is 0, and then change the PID[1:0] bits from 01b (BUF) to 00b (NAK). If the PID[1:0] bits are changed to 00 (NAK) by the USBFS, checking the PBUSY bit through the software is not necessary.
Note 3. Only set the ACLRM bit while PID is NAK and before the pipe is selected in the CURPIPE[3:0] bits in the port select register. Before setting this bit, check that the PBUSY bit is 0, and then change the PID[1:0] bits from 01b (BUF) to 00b (NAK). If the PID[1:0] bits are changed to 00 (NAK) by the USBFS, checking the PBUSY bit through the software is not necessary.

PIPEnCTR can be set for any pipe selection in the PIPESEL register.

PID[1:0] bits (Response PID)

The PID[1:0] bits specify the response type for the next transaction on the selected pipe.

预计会收到IN令牌。即使SOF数据包损坏，FIFO缓冲区也会在预期接收SOF数据包时使用内部插值功能清除。

Whenthehostcontrollerfunctionisselected setthisbitto0.Whentheselectedpipeisnotforisochronoustransfer set thisbitto0.

32.2.32 PIPEn控制寄存器(PIPEnCTR)(n=1到9)

PIPEnCTR (n = 1 to 5)

Address(es): USBFS.PIPE1CTR 4009 0070h, USBFS.PIPE2CTR 4009 0072h, USBFS.PIPE3CTR 4009 0074h, USBFS.PIPE4CTR 4009 0076h, USBFS.PIPE5CTR 4009 0078h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BSTS	INBUFM	—	—	—	ATREPM	ACLRM	SQCLR	SQSET	SQMON	PBUSY	—	—	—	PID[1:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b1, b0	PID[1:0]	响应PID	b1b000：NAK响应01：BUF响应（取决于缓冲区状态）10：STALL响应11：STALL响应。	R/W
b4 to b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b5	PBUSY	管道忙	0：管道n未用于事务1：管道n正在用于事务。	R
b6	SQMON	序列切换位 Confirmation	0: DATA0 1: DATA1.	R
b7	SQSET	序列切换位设置 *2	设置管道n的序列切换位。0：无效（写0无效）1：将下一笔交易的期望值设置为DATA1。该位读为0。	R/W*1
b8	SQCLR	序列切换位 Clear*2	清除管道n的序列切换位。0：无效（写0无效）1：清除下一笔交易的期望值到DATA0。该位读为0。	R/W*1
b9	ACLRM	自动缓冲区清除模式 *3	0：禁用1：启用（初始化所有缓冲区）。	R/W
b10	ATREPM	自动响应模式 *2	0：禁用自动响应模式1：启用自动响应模式。	R/W
b13 to b11	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b14	INBUFM	发送缓冲区监视器	0：FIFO缓冲区中没有要发送的数据1：FIFO缓冲区中没有要发送的数据。	R
b15	BSTS	缓冲区状态	0：禁止CPU访问缓冲区1：允许CPU访问缓冲区。	R

Note 1. 只能读取0。
Note 2. PID为NAK时，仅设置ATREPM位或将1写入SQCLR或SQSET位。在设置这些位之前，请检查PBUSY位为0，然后将PID[1:0]位从01b(BUF)更改为00b(NAK)。如果PID[1:0]位被USBFS更改为00(NAK)，则无需通过软件检查PBUSY位。
Note 3. 仅在PID为NAK时以及在端口选择寄存器的CURPIPE[3:0]位中选择管道之前设置ACLRM位。在设置该位之前，请检查PBUSY位是否为0，然后将PID[1:0]位从01b(BUF)更改为00b(NAK)。如果PID[1:0]位由USBFS更改为00(NAK)，无需通过软件检查PBUSY位。

PIPEnCTR可以为PIPESEL寄存器中的任何管道选择设置。

PID[1:0]位（响应PID）

PID[1:0]位指定所选管道上下一个事务的响应类型。

The default PID[1:0] setting is NAK. Change the PID[1:0] setting to BUF to use the associated pipe for USB transfer. Table 32.7 and Table 32.8 show the basic operations of the USBFS (when there are no errors in the communication packets) based on the PID[1:0] bit setting.

After changing the PID[1:0] setting from BUF to NAK through the software during USB communication on the selected pipe, check that the PBUSY bit is 1 to see if USB transfer on the pipe has actually entered the NAK state. If the USBFS changes the PID[1:0] bits to NAK, checking the PBUSY bit through the software is not necessary.

The USBFS changes the PIPEnCTR.PID[1:0] setting in the following cases:

- The USBFS sets PID to NAK on recognizing completion of the transfer when the selected pipe is in the receiving direction and the PIPECFG.SHTNAK bit for the selected pipe is set to 1 by software
- The USBFS sets PID to STALL (11b) on receiving a data packet with a payload exceeding the maximum packet size of the selected pipe
- The USBFS sets PID to NAK on detecting a USB bus reset in device controller mode
- The USBFS sets PID to NAK on detecting a reception error, such as a CRC error, three consecutive times in host controller mode
- The USBFS sets PID to STALL (11b) on receiving the STALL handshake in host controller mode.

To specify the response type, set the PID[1:0] bits as follows:

- To transition from NAK (00b) to STALL, set 10b
- To transition from BUF (01b) to STALL, set 11b
- To transition from STALL (11b) to NAK, set 10b and then 00b
- To transition from STALL to BUF, transition to NAK and then BUF.

Table 32.7 Operation of the USBFS based on the PID[1:0] setting in host controller mode

PID[1:0] value	Transfer type	Transfer direction (DIR bit)	USBFS operation
00b (NAK)	Does not depend on the setting	Does not depend on the setting	Does not issue tokens
01b (BUF)	Bulk or interrupt	Does not depend on the setting	Issues tokens when the DVSTCTR0.UACT bit is 1 and the FIFO buffer associated with the selected pipe is ready for transmission and reception. Does not issue tokens when the DVSTCTR0.UACT bit is 0 or the FIFO buffer associated with the selected pipe is not ready for transmission or reception.
	Isochronous	Does not depend on the setting	Issues tokens regardless of the status of the FIFO buffer associated with the selected pipe.
10b (STALL) or 11b (STALL)	Does not depend on the setting	Does not depend on the setting	Does not issue tokens.

Table 32.8 Operation of the USBFS based on the PID[1:0] setting in device controller mode (1 of 2)

PID[1:0] value	Transfer type	Transfer direction (DIR bit)	USBFS operation
00b (NAK)	Bulk or interrupt	Does not depend on the setting	Returns NAK in response to the token from the USB host
	Isochronous	Does not depend on the setting	Returns nothing in response to the token from the USB host

默认PID[1:0]设置为NAK。将PID[1:0]设置更改为BUF以使用关联的管道进行USB传输。
表32.7和表32.8显示了基于PID[1:0]位设置的USBFS的基本操作（当通信数据包中没有错误时）。

在选定管道上进行USB通信期间，通过软件将PID[1:0]设置从BUF更改为NAK后，检查PBUSY位是否为1，以查看管道上的USB传输是否真正进入了NAK状态。如果USBFS将PID[1:0]位更改为NAK，则无需通过软件检查PBUSY位。

USBFS在以下情况下更改PIPEnCTR.PID[1:0]设置：

- 当所选管道处于接收方向并且所选管道的PIPECFG.SHTNAK位由软件设置为1时，USBFS在识别到传输完成时将PID设置为NAK
- USBFS在接收到有效载荷超过所选管道的最大数据包大小的数据包时将PID设置为STALL(11b)
- USBFS在设备控制器模式下检测到USB总线复位时将PID设置为NAK
- USBFS在主机控制器模式下连续3次检测到接收错误（例如CRC错误）时将PID设置为NAK
- USBFS在主机控制器模式下接收到STALL握手时将PID设置为STALL(11b)。

要指定响应类型，请按如下方式设置PID[1:0]位：

- 要从NAK(00b)转换到STALL，请设置10b
- 要从BUF(01b)转换到STALL，请设置11b
- 要从STALL(11b)转换到NAK，请设置10b，然后设置00b
- 要从STALL过渡到BUF，先过渡到NAK，然后再过渡到BUF。

Table 32.7 USBFS在主机控制器模式下基于PID[1:0]设置的操作

PID[1:0] value	传输类型	传输方向（DIR位）	USBFS operation
00b (NAK)	不依赖于设置	不依赖于设置	不发行代币
01b (BUF)	批量或中断	不依赖于设置	当DVSTCTR0.UACT位为1并且与所选管道关联的FIFO缓冲区已准备好进行发送和接收时，发出令牌。当DVSTCTR0.UACT位为0或 与所选管道关联的FIFO缓冲区尚未准备好进行发送或接收。
	Isochronous	不依赖于设置	无论与所选管道关联的FIFO缓冲区的状态如何，都会发出令牌。
10b (STALL) or 11b (STALL)	不依赖于设置	不依赖于设置	不发行代币。

Table 32.8 基于设备控制器模式下的PID[1:0]设置的USBFS操作（1of2）

PID[1:0] value	传输类型	传输方向（DIR位）	USBFS operation
00b (NAK)	批量或中断	不依赖于设置	返回NAK以响应来自USB主机的令牌
	Isochronous	不依赖于设置	响应来自USB主机的令牌，不返回任何内容

Table 32.8 Operation of the USBFS based on the PID[1:0] setting in device controller mode (2 of 2)

PID[1:0] value	Transfer type	Transfer direction (DIR bit)	USBFS operation
01b (BUF)	Bulk	Receiving direction (DIR = 0)	Receives data and returns ACK in response to the OUT token from the USB host if the FIFO buffer associated with the selected pipe is ready for reception
	Interrupt	Receiving direction (DIR = 0)	Receives data and returns ACK in response to the OUT token from the USB host if the FIFO buffer associated with the selected pipe is ready for reception
	Bulk or interrupt	Transmitting direction (DIR = 1)	Transmits data in response to the token from the USB host if the FIFO buffer associated with the selected pipe is ready for transmission. Otherwise, returns NAK.
	Isochronous	Receiving direction (DIR = 0)	Receives data in response to the OUT token from the USB host if the FIFO buffer associated with the selected pipe is ready for reception. Otherwise, discards the data.
	Isochronous	Transmitting direction (DIR = 1)	Transmits data in response to the token from the USB host if the associated FIFO buffer is ready for transmission. Otherwise, transmits a zero-length packet.
10b (STALL) or 11b (STALL)	Bulk or interrupt	Does not depend on the setting	Returns STALL in response to the token from the USB host
	Isochronous	Does not depend on the setting	Returns nothing in response to the token from the USB host

PBUSY bit (Pipe Busy)

The PBUSY bit indicates whether the selected pipe is being used for the current transaction.

The USBFS changes the PBUSY bit from 0 to 1 on start of the USB transaction for the selected pipe, and changes the PBUSY bit from 1 to 0 on completion of one transaction.

Reading the PBUSY bit by software after PID is set to NAK allows you to check whether changing the pipe setting is possible. For details, see section 32.3.4.1, Pipe control register switching procedures.

SQMON bit (Sequence Toggle Bit Confirmation)

The SQMON bit indicates the expected value of the sequence toggle bit for the next transaction of the selected pipe.

When the selected pipe is not the isochronous transfer type, the USBFS toggles the SQMON flag on successful completion of the transaction. However, the USBFS does not toggle the SQMON flag when a DATA-PID mismatch occurs during transfer in the receiving direction.

SQSET bit (Sequence Toggle Bit Set)

Setting the SQSET bit to 1 through the software causes the USBFS to set DATA1 as the expected value of the sequence toggle bit for the next transaction on the selected pipe. The USBFS clears the SQSET bit to 0.

SQCLR bit (Sequence Toggle Bit Clear)

Setting the SQCLR bit to 1 through the software causes the USBFS to clear the expected value of the sequence toggle bit for the next transaction on the selected pipe to DATA0. The USBFS clears the SQCLR bit to 0.

ACLRM bit (Auto Buffer Clear Mode)

The ACLRM bit enables or disables auto buffer clear mode for the selected pipe. To completely clear the data in the FIFO buffer allocated to the selected pipe, write 1 and then 0 to the ACLRM bit continuously.

Table 32.9 shows the data cleared by writing 1 and 0 to the ACLRM bit continuously and the cases in which this processing is required.

Table 32.9 Data cleared by the USBFS when ACLRM = 1 (1 of 2)

Number	Data cleared by setting the ACLRM bit	Situations requiring data clear
1	All data in the FIFO buffer allocated to the selected pipe (two FIFO buffers in double buffer mode)	When initializing the selected pipe

Table 32.8 基于设备控制器模式下的PID[1:0]设置的USBFS操作（2之2）

PID[1:0] value	传输类型	传输方向（DIR位）	USBFS operation
01b (BUF)	Bulk	接收方向(DIR=0)	如果与所选管道关联的FIFO缓冲区已准备好接收，则接收数据并返回ACK以响应来自USB主机的OUT令牌
	Interrupt	接收方向(DIR=0)	如果与所选管道关联的FIFO缓冲区已准备好接收，则接收数据并返回ACK以响应来自USB主机的OUT令牌
	批量或中断	发射方向(DIR=1)	传输数据以响应来自USB主机的令牌，如果与所选管道关联的FIFO缓冲区已准备好进行传输。否则，返回NAK。
	Isochronous	接收方向(DIR=0)	如果与所选管道关联的FIFO缓冲区已准备好接收，则接收数据以响应来自USB主机的OUT令牌。否则，丢弃数据。
	Isochronous	发射方向(DIR=1)	如果关联的FIFO缓冲区已准备好传输，则传输数据以响应来自USB主机的令牌。否则，发送零长度数据包。
10b (STALL) or 11b (STALL)	批量或中断	不依赖于设置	返回STALL以响应来自USB主机的令牌
	Isochronous	不依赖于设置	响应来自USB主机的令牌，不返回任何内容

PBUSY位（管道忙）

PBUSY位指示所选管道是否正在用于当前事务。

USBFS在所选管道的USB事务开始时将PBUSY位从0更改为1，并更改PBUSY位在一个事务完成时从1变为0。

在PID设置为NAK后，通过软件读取PBUSY位可以检查是否可以更改管道设置。详见32.3.4.1管道控制寄存器切换流程。

SQMON位（序列切换位确认）

SQMON位指示所选管道的下一个事务的序列切换位的预期值。

当所选管道不是同步传输类型时，USBFS在事务成功完成时切换SQMON标志。但是，当在接收方向的传输过程中发生DATA-PID不匹配时，USBFS不会切换SQMON标志。

SQSET位（序列切换位设置）

通过软件将SQSET位设置为1会导致USBFS将DATA1设置为所选管道上下一个事务的序列切换位的预期值。USBFS将SQSET位清0。

SQCLR位（序列切换位清除）

通过软件将SQCLR位设置为1会导致USBFS将所选管道上下一个事务的序列切换位的预期值清除为DATA0。USBFS将SQCLR位清0。

ACLRM位（自动缓冲区清除模式）

ACLRM位启用或禁用所选管道的自动缓冲区清除模式。彻底清除数据库中的数据FIFO缓冲区分配给所选管道，向ACLRM位连续写入1和0。

表32.9显示了通过向ACLRM位连续写入1和0来清除的数据以及需要进行此处理的情况。

Table 32.9 当ACLRM=1(1of2)时USBFS清除的数据

Number	通过设置ACLRM位清除数据	需要数据清楚的情况
1	FIFO缓冲区中的所有数据分配给选定的管道（两个双缓冲模式下的FIFO缓冲）	初始化选定管道时

Table 32.9 Data cleared by the USBFS when ACLRM = 1 (2 of 2)

Number	Data cleared by setting the ACLRM bit	Situations requiring data clear
2	Interval count value when the selected pipe is the isochronous transfer type	When resetting the interval count value
3	Internal flags related to the PIPECFG.BFRE bit	When changing the PIPECFG.BFRE setting
4	FIFO buffer toggle control	When changing the PIPECFG.DBLB setting
5	Internal flags related to the transaction count	When forcing the transaction count function to terminate

ATREPM bit (Auto Response Mode)

The ATREPM bit enables or disables auto response mode for the selected pipe.

This bit can be set to 1 in device controller mode when the selected pipe is the bulk transfer type. When the bit is set to 1, the USBFS responds to the token from the USB host as follows:

- When the selected pipe is set for bulk IN transfers (PIPECFG.TYPE[1:0] = 01b and PIPECFG.DIR = 1):
  a. When the ATREPM bit = 1 and PID = BUF, the USBFS transmits a zero-length packet in response to the IN token.
  b. The USBFS updates (allows toggling of) the sequence toggle bit (DATA-PID) each time the USBFS receives ACK from the USB host. In a single transaction, the IN token is received, a zero-length packet is transmitted, and then ACK is received. The USBFS does not generate the BRDY or BEMP interrupt.
- When the selected pipe is set for bulk OUT transfers (PIPECFG.TYPE[1:0] = 01b and PIPECFG.DIR = 0):

  When the ATREPM bit = 1 and PID = BUF, the USBFS returns NAK in response to the OUT token and generates an NRDY interrupt.

For USB communication in auto response mode, set the ATREPM bit to 1 while the FIFO buffer is empty. Do not write to the FIFO buffer during USB communication in auto response mode. When the selected pipe uses isochronous transfer, always set this bit to 0.

In host controller mode, always set the ATREPM bit to 0.

INBUFM bit (Transmit Buffer Monitor)

The INBUMFM bit indicates the FIFO buffer status for the selected pipe in the transmitting direction.

When the selected pipe is set in the transmitting direction (PIPECFG.DIR = 1), the USBFS sets this bit to 1 when the CPU or DMA/DTC completes writing data to at least one FIFO buffer plane.

The USBFS sets this bit to 0 when the USBFS completes transmission of the data from the FIFO buffer plane to which all the data is written. In double buffer mode (PIPECFG.DBLB = 1), the USBFS sets the INBUFM bit to 0 when the USBFS completes transmission of the data from the two FIFO buffer planes before the CPU or DMA/DTC completes writing data to one FIFO buffer plane.

The INBUFM bit indicates the same value as the BSTS bit when the selected pipe is in the receiving direction (PIPECFG.DIR = 0).

BSTS bit (Buffer Status)

The BSTS bit indicates the FIFO buffer status for the selected pipe.

The meaning of the BSTS bit depends on the PIPECFG.DIR, PIPECFG.BFRE, and DnFIFOSEL.DCLRM settings, as shown in Table 32.10.

Table 32.9 当ACLRM=1(2of2)时USBFS清除的数据

Number	通过设置ACLRM位清除数据	需要数据清楚的情况
2	选择管道为等时传输类型时的间隔计数值	重置间隔计数值时
3	与PIPECFG.BFRE位相关的内部标志	更改PIPECFG.BFRE设置时
4	FIFO缓冲区切换控制	更改PIPECFG.DBLB设置时
5	与事务计数相关的内部标志	强制事务计数函数终止时

ATREPM位（自动响应模式）

ATREPM位启用或禁用所选管道的自动响应模式。

当所选管道为批量传输类型时，该位可以在设备控制器模式下设置为1。当该位设置为1时，USBFS响应来自USB主机的令牌，如下所示：

- 当所选管道设置为批量IN传输时（PIPECFG.TYPE[1:0]=01b和PIPECFG.DIR=1）：

  一个。当ATREPM位=1且PID=BUF时，USBFS发送一个长度为零的数据包以响应IN令牌。

  湾。每次USBFS从USB主机接收到ACK时，USBFS都会更新（允许切换）序列切换位(DATA-PID)。在单个事务中，收到IN令牌，发送零长度数据包，然后收到ACK。USBFS不会产生BRDY或BEMP中断。

- 当所选管道设置为批量OUT传输时（PIPECFG.TYPE[1:0]=01b和PIPECFG.DIR=0）：

当ATREPM位=1且PID=BUF时，USBFS返回NAK以响应OUT令牌并产生NRDY中断。对于自动响应模式下的USB通信，当FIFO缓冲区为空时，将ATREPM位设置为1。在自动响应模式下的USB通信期间不要写入FIFO缓冲区。当所选管道使用同步传输时，始终将此位设置为0。

在主机控制器模式下，始终将ATREPM位设置为0。

INBUFM位（发送缓冲区监视器）

INBUMFM位指示发送方向上所选管道的FIFO缓冲区状态。

当所选管道设置为发送方向（PIPECFG.DIR=1）时，USBFS将该位设置为1，当CPU或DMADTC完成将数据写入至少一个FIFO缓冲平面。

当USBFS完成从写入所有数据的FIFO缓冲区平面传输数据时，USBFS将该位设置为0。在双缓冲模式(PIPECFG.DBLB=1)下，当USBFS在CPU或DMADTC完成将数据写入一个FIFO缓冲层之前完成从两个FIFO缓冲层的数据传输时，USBFS将INBUFM位设置为0。

当所选管道处于接收方向时（PIPECFG.DIR=0），INBUFM位指示与BSTS位相同的值。

BSTS位（缓冲区状态）

BSTS位指示所选管道的FIFO缓冲区状态。

BSTS位的含义取决于PIPECFG.DIR、PIPECFG.BFRE和DnFIFOSEL.DCLRM设置，如表32.10所示。

Table 32.10 BSTS bit operation

DIR value	BFRE value	DCLRM value	BSTS bit function
0	0	0	Sets to 1 when receive data can be read from the FIFO buffer, and clears to 0 on completion of data read
		1	Setting prohibited
	1	0	Sets to 1 when receive data can be read from the FIFO buffer, and clears to 0 when the software sets the BCLR bit in the port control register to 1 after the data read is complete
		1	Sets to 1 when receive data can be read from the FIFO buffer, and clears to 0 on completion of data read
1	0	0	Sets to 1 when transmit data can be written to the FIFO buffer, and clears to 0 on completion of data write
		1	Setting prohibited
	1	0	Setting prohibited
		1	Setting prohibited

PIPEnCTR (n = 6 to 9)

Address(es): USBFS.PIPE6CTR 4009 007Ah, USBFS.PIPE7CTR 4009 007Ch, USBFS.PIPE8CTR 4009 007Eh, USBFS.PIPE9CTR 4009 0080h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BSTS	—	—	—	—	—	ACLRM	SQCLR	SQSET	SQMON	PBUSY	—	—	—	PID[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	PID[1:0]	Response PID	b1 b0 0 0: NAK response 0 1: BUF response (depends on the buffer state) 1 0: STALL response 1 1: STALL response.	R/W
b4 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b5	PBUSY	Pipe Busy	0: Pipe n not in use for the transaction 1: Pipe n in use for the transaction.	R
b6	SQMON	Sequence Toggle Bit Confirmation	0: DATA0 1: DATA1.	R
b7	SQSET	Sequence Toggle Bit Set*2	Sets the sequence toggle bit for pipe n: 0: Invalid (writing 0 has no effect) 1: Set the expected value for the next transaction to DATA1. This bit is read as 0.	R/W *1
b8	SQCLR	Sequence Toggle Bit Clear*2	Clears the sequence toggle bit for pipe n: 0: Invalid (writing 0 has no effect) 1: Clear the expected value for the next transaction to DATA0. This bit is read as 0.	R/W *1
b9	ACLRM	Auto Buffer Clear Mode*3	0: Disable 1: Enable (all buffers initialized).	R/W
b14 to b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15	BSTS	Buffer Status	0: Buffer access disabled 1: Buffer access enabled.	R

Note 1. Only 0 can be read. Only 1 can be written.
Note 2. Only write 1 to the SQCLR or SQSET bit while PID is NAK. Before setting these bits, check that the PBUSY bit is 0, and then change the PID[1:0] bits from 01b (BUF) to 00b (NAK). If the PID[1:0] bits are changed to 00 (NAK) by the USBFS, checking the PBUSY bit through the software is not necessary.
Note 3. Only set the ACLRM bit while PID is NAK and before the pipe is selected in the CURPIPE[3:0] bits in the port select register. Before setting this bits, check that the PIPEnCTR.PBUSY bit is 0, and then change the PIPEnCTR.PID[1:0] bits from 01b (BUF)

Table 32.10 BSTS位操作

方向值	BFRE value	DCLRM value	BSTS位功能
0	0	0	当接收数据可以从FIFO缓冲区读取时设置为1，并在数据读取完成时清除为0
		1	禁止设定
	1	0	接收数据可以从FIFO缓冲区读取时设置为1，当数据读取完成后软件将端口控制寄存器中的BCLR位设置为1时清除为0
		1	当接收数据可以从FIFO缓冲区读取时设置为1，并在数据读取完成时清除为0
1	0	0	当发送数据可以写入FIFO缓冲区时设置为1，并在数据写入完成时清除为0
		1	禁止设定
	1	0	禁止设定
		1	禁止设定

PIPEnCTR (n = 6 to 9)

Address(es): USBFS.PIPE6CTR 4009 007Ah, USBFS.PIPE7CTR 4009 007Ch, USBFS.PIPE8CTR 4009 007Eh, USBFS.PIPE9CTR 4009 0080h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BSTS	—	—	—	—	—	ACLRM	SQCLR	SQSET	SQMON	PBUSY	—	—	—	PID[1:0]	
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b1, b0	PID[1:0]	响应PID	b1b000：NAK响应01：BUF响应（取决于缓冲区状态）10：STALL响应11：STALL响应。	R/W
b4 to b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b5	PBUSY	管道忙	0：管道n未用于事务1：管道n正在用于事务。	R
b6	SQMON	序列切换位 Confirmation	0: DATA0 1: DATA1.	R
b7	SQSET	序列切换位设置 *2	设置管道n的序列切换位：0：无效（写入0无效）1：将下一个事务的预期值设置为DATA1。该位读为0。	R/W *1
b8	SQCLR	序列切换位 Clear*2	清除管道n的序列切换位：0：无效（写入0无效）1：将下一个事务的预期值清除到DATA0。该位读为0。	R/W *1
b9	ACLRM	自动缓冲区清除模式 *3	0：禁用1：启用（所有缓冲区都已初始化）。	R/W
b14 to b10	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b15	BSTS	缓冲区状态	0：禁止缓冲区访问1：允许缓冲区访问。	R

Note 1. 只能读取0。只能写1个。
Note 2. PID为NAK时，仅向SQCLR或SQSET位写入1。在设置这些位之前，请检查PBUSY位是否为0，然后将PID[1:0]位从01b(BUF)更改为00b(NAK)。如果PID[1:0]位被USBFS更改为00(NAK)，则无需通过软件检查PBUSY位。

Note 3. 仅在PID为NAK时以及在端口选择寄存器的CURPIPE[3:0]位中选择管道之前设置ACLRM位。
在设置此位之前，请检查PIPEnCTR.PBUSY位是否为0，然后将PIPEnCTR.PID[1:0]位从01b(BUF)更改

to 00b (NAK). If the PID[1:0] bits are changed to 00 (NAK) by the USBFS, checking the PBUSY bit through the software is not necessary.

PID[1:0] bits (Response PID)

The PID[1:0] bits specify the response type for the next transaction of the selected pipe.

The default PID[1:0] setting is NAK. Change the PID[1:0] setting to BUF to use the associated pipe for USB transfer. Table 32.7 and Table 32.8 show the basic operation (when there are no errors in the transmitted and received packets) of the USBFS depending on the PID[1:0] setting.

After changing the PID[1:0] setting from BUF to NAK through the software during USB communication on the selected pipe, check that the PBUSY bit is 1 to see if USB transfer on the selected pipe has actually entered the NAK state. If the USBFS changes the PID[1:0] bits to NAK, checking the PBUSY bit through the software is not necessary.

The USBFS changes the PIPEnCTR.PID[1:0] setting in the following cases:

- The USBFS sets PID to STALL (11b) on receiving a data packet with a payload exceeding the maximum packet size of the selected pipe
- The USBFS sets PID to NAK on detecting a USB bus reset in device controller mode
- The USBFS sets PID to NAK on detecting a reception error, such as a CRC error, three consecutive times in host controller mode
- The USBFS sets PID to STALL (11b) on receiving the STALL handshake in host controller mode.

To specify each response type, set the PID[1:0] bits as follows:

- To transition from NAK (00b) to STALL, set 10b
- To transition from BUF (01b) to STALL, set 11b
- To transition from STALL (11b) to NAK, set 10b and then 00b
- To transition from STALL to BUF, transition to NAK and then BUF.

PBUSY bit (Pipe Busy)

The PBUSY bit indicates whether the selected pipe is being used for the current transaction.

The USBFS changes the PBUSY bit from 0 to 1 on start of the USB transaction for the selected pipe, and changes the PBUSY bit from 1 to 0 on completion of one transaction.

Reading the PBUSY bit by software after PID is set to NAK allows you to check whether changing the pipe setting is possible.

SQMON bit (Sequence Toggle Bit Confirmation)

The SQMON bit indicates the expected value of the sequence toggle bit for the next transaction of the selected pipe.

The USBFS toggles the SQMON bit on successful completion of the transaction. However, the USBFS does not toggle the SQMON bit when a DATA-PID mismatch occurs during transfer in the receiving direction.

SQSET bit (Sequence Toggle Bit Set)

Setting the SQSET bit to 1 through the software causes the USBFS to set DATA1 as the expected value of the sequence toggle bit for the next transaction on the selected pipe. The USBFS sets the SQSET bit to 0.

SQCLR bit (Sequence Toggle Bit Clear)

Setting the SQCLR bit to 1 through the software causes the USBFS to clear the expected value of the sequence toggle bit for the next transaction on the selected pipe to DATA0. The USBFS sets the SQCLR bit to 0.

ACLRM bit (Auto Buffer Clear Mode)

The ACLRM bit enables or disables auto buffer clear mode for the selected pipe. To completely clear the data in the FIFO buffer allocated to the selected pipe, write 1 and then 0 to the ACLRM bit continuously.

Table 32.11 shows the data cleared by writing 1 and 0 continuously to the ACLRM bit and the cases in which this processing is required.

到00b(NAK)。如果PID[1:0]位被USBFS更改为00(NAK)，则无需通过软件检查PBUSY位。

PID[1:0]位（响应PID）

PID[1:0]位指定所选管道的下一个事务的响应类型。

默认PID[1:0]设置为NAK。将PID[1:0]设置更改为BUF以使用关联的管道进行USB传输。
表32.7和表32.8显示了取决于PID[1:0]设置的USBFS的基本操作（在发送和接收的数据包中没有错误时）。

在选定管道上进行USB通信期间，通过软件将PID[1:0]设置从BUF更改为NAK后，检查PBUSY位是否为1，以查看选定管道上的USB传输是否真正进入了NAK状态。如果USBFS将PID[1:0]位更改为NAK，则无需通过软件检查PBUSY位。

USBFS在以下情况下更改PIPEnCTR.PID[1:0]设置：

- USBFS在接收到有效载荷超过所选管道的最大数据包大小的数据包时将PID设置为STALL(11b)
- USBFS在设备控制器模式下检测到USB总线复位时将PID设置为NAK
- USBFS在主机控制器模式下连续3次检测到接收错误（例如CRC错误）时将PID设置为NAK
- USBFS在主机控制器模式下接收到STALL握手时将PID设置为STALL(11b)。

要指定每种响应类型，请按如下方式设置PID[1:0]位：

- 要从NAK(00b)转换到STALL，请设置10b
- 要从BUF(01b)转换到STALL，请设置11b
- 要从STALL(11b)转换到NAK，请设置10b，然后设置00b
- 要从STALL过渡到BUF，先过渡到NAK，然后再过渡到BUF。

PBUSY位（管道忙）

PBUSY位指示所选管道是否正在用于当前事务。

USBFS在所选管道的USB事务开始时将PBUSY位从0更改为1，并更改
PBUSY位在一个事务完成时从1变为0。

在PID设置为NAK后，通过软件读取PBUSY位可以检查是否可以更改管道设置。

SQMON位（序列切换位确认）

SQMON位指示所选管道的下一个事务的序列切换位的预期值。

USBFS在事务成功完成时切换SQMON位。但是，当在接收方向的传输过程中发生DATA-PID不匹配时，USBFS不会触发SQMON位。

SQSET位（序列切换位设置）

通过软件将SQSET位设置为1会导致USBFS将DATA1设置为所选管道上下一个事务的序列切换位的预期值。USBFS将SQSET位设置为0。

SQCLR位（序列切换位清除）

通过软件将SQCLR位设置为1会导致USBFS将所选管道上下一个事务的序列切换位的预期值清除为DATA0。USBFS将SQCLR位设置为0。

ACLRM位（自动缓冲区清除模式）

ACLRM位启用或禁用所选管道的自动缓冲区清除模式。彻底清除数据库中的数据
FIFO缓冲区分配给所选管道，向ACLRM位连续写入1和0。

表32.11显示了通过向ACLRM位连续写入1和0来清除的数据以及需要进行此处理的情况。

Table 32.11 Data cleared by the USBFS when ACLRM = 1

Number	Data cleared by setting the ACLRM bit	Situations requiring data clear
1	All data in the FIFO buffer allocated to the selected pipe	When initializing the selected pipe
2	Interval count value when the selected pipe is the isochronous transfer type	When resetting the interval count value
3	Internal flags related to the PIPECFG.BFRE bit	When changing the PIPECFG.BFRE setting
4	Internal flags related to the transaction count	When forcing the transaction count function to terminate

BSTS bit (Buffer Status)

The BSTS bit indicates the FIFO buffer status for the selected pipe.

The meaning of the BSTS bit depends on the PIPECFG.DIR, PIPECFG.BFRE, and DnFIFOSEL.DCLRM settings, as shown in Table 32.10.

32.2.33 PIPEn Transaction Counter Enable Register (PIPEnTRE) (n = 1 to 5)

Address(es): USBFS.PIPE1TRE 4009 0090h, USBFS.PIPE2TRE 4009 0094h, USBFS.PIPE3TRE 4009 0098h, USBFS.PIPE4TRE 4009 009Ch, USBFS.PIPE5TRE 4009 00A0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	TRENB	TRCLR	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	TRCLR	Transaction Counter Clear	0: Invalid (writing 0 has no effect) 1: Clear counter value.	R/W
b9	TRENB	Transaction Counter Enable	0: Disable transaction counter 1: Enable transaction counter.	R/W
b15 to b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Set each bit in PIPEnTRE while PID is NAK. Before setting these bits after changing the PIPEnCTR.PID[1:0] bits for the selected pipe from BUF to NAK, check that the PIPEnCTR.PBUSY bit is 0. However, if the PID[1:0] bits are changed to NAK by the USBFS, checking the PBUSY bit through the software is not necessary.

TRCLR bit (Transaction Counter Clear)

When the TRCLR bit sets to 1, the USBFS clears the value of the transaction counter associated with the selected pipe and then sets the TRCLR bit to 0.

TRENB bit (Transaction Counter Enable)

The TRENB bit enables or disables the transaction counter.

For receiving pipes, setting the TRENB bit to 1 after setting the total number of the packets to be received in the PIPEnTRN.TRNCNT[15:0] bits through the software allows the USBFS to control hardware on having received the number of packets equal to the TRNCNT[15:0] setting, as follows:

- When the PIPECFG.SHTNAK bit is 1, the USBFS changes the PID bits to NAK for the associated pipe on having received the number of packets equal to the TRNCNT[15:0] setting
- When the PIPECFG.BFRE bit is 1, the USBFS asserts the BRDY interrupt on having received the number of packets equal to the TRNCNT[15:0] setting and then reading the last received data.

For transmitting pipes, set the TRENB bit to 0.

When the transaction counter is not used, set this bit to 0. When the transaction counter is used, set the TRNCNT[15:0] bits before setting this bit to 1. Set this bit to 1 before receiving the first packet to be counted by the transaction counter.

Table 32.11 ACLRM=1时USBFS清除的数据

Number	通过设置ACLRM位清除数据	需要数据清楚的情况
1	分配给所选管道的FIFO缓冲区中的所有数据	初始化选定管道时
2	选择管道为等时传输类型时的间隔计数值	重置间隔计数值时
3	与PIPECFG.BFRE位相关的内部标志	更改PIPECFG.BFRE设置时
4	与事务计数相关的内部标志	强制事务计数函数终止时

BSTS位（缓冲区状态）

BSTS位指示所选管道的FIFO缓冲区状态。

BSTS位的含义取决于PIPECFG.DIR、PIPECFG.BFRE和DnFIFOSEL.DCLRM设置，如表32.10所示。

32.2.33 PIPEn事务计数器使能寄存器(PIPEnTRE)(n=1到5)

Address(es): USBFS.PIPE1TRE 4009 0090h, USBFS.PIPE2TRE 4009 0094h, USBFS.PIPE3TRE 4009 0098h, USBFS.PIPE4TRE 4009 009Ch, USBFS.PIPE5TRE 4009 00A0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	TRENB	TRCLR	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b7 to b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b8	TRCLR	交易计数器清除	0：无效（写0无效）1：清除计数器值。	R/W
b9	TRENB	事务计数器启用	0：禁用事务计数器1：启用事务计数器。	R/W
b15 to b10	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note: 当PID为NAK时，设置PIPEnTRE中的每个位。在将所选管道的PIPEnCTR.PID[1:0]位从BUF更改为NAK之后设置这些位之前，请检查PIPEnCTR.PBUSY位是否为0。但是，如果PID[1:0]位更改为NAK通过USBFS，无需通过软件检查PBUSY位。

TRCLR位（事务计数器清零）

当TRCLR位设置为1时，USBFS清除与所选管道关联的事务计数器的值，然后将TRCLR位设置为0。

TRENB位（事务计数器使能）

TRENB位启用或禁用事务计数器。

对于接收管道，在设置接收管道的总包数后，将TRENB位设置为1
PIPEnTRN.TRNCNT[15:0]位通过软件允许USBFS在接收到等于TRNCNT[15:0]设置的数据包数量时控制硬件，如下所示：

- 当PIPECFG.SHTNAK位为1时，USBFS在接收到等于TRNCNT[15:0]设置的数据包数量时将关联管道的PID位更改为NAK
- 当PIPECFG.BFRE位为1时，USBFS在接收到等于TRNCNT[15:0]设置的数据包数量并读取最后接收到的数据时断言BRDY中断。

对于传输管道，将TRENB位设置为0。

当不使用事务计数器时，将该位设置为0。当使用事务计数器时，将该位设置为1之前设置TRNCNT[15:0]位。在接收第一个要计数的数据包之前将该位设置为1由交易柜台。

32.2.34 PIPEn Transaction Counter Register (PIPEnTRN) (n = 1 to 5)

Address(es): USBFS.PIPE1TRN 4009 0092h, USBFS.PIPE2TRN 4009 0096h, USBFS.PIPE3TRN 4009 009Ah, USBFS.PIPE4TRN 4009 009Eh, USBFS.PIPE5TRN 4009 00A2h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TRNCNT[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b15 to b0	TRNCNT[15:0]	Transaction Counter	When written to, this bit specifies the total packets (number of transactions) to be received by the selected pipe. When read from, when PIPEnTRE.TRENB is 0, this bit indicates the specified number of transactions. When PIPEnTRE.TRENB is 1, this bit indicates the current transaction count.	R/W

The PIPEnTRN registers retain their settings during a USB bus reset.

TRNCNT[15:0] bits (Transaction Counter)

The USBFS increments the value of the TRNCNT[15:0] bits by 1 when all of the following conditions are satisfied on receiving the packet:

- The PIPEnTRE.TRENB bit = 1
- (TRNCNT[15:0] set value ≠ current counter value + 1) on receiving the packet
- The payload of the received packet agrees with the PIPEMAXP.MXPS[8:0] setting.

The USBFS clears the value of the TRNCNT[15:0] bits to 0 when any of the following conditions are satisfied:

All of the following conditions are satisfied:

- The PIPEnTRE.TRENB bit = 1
- (TRNCNT[15:0] set value = current counter value + 1) on receiving the packet
- The payload of the received packet agrees with the PIPEMAXP.MXPS[8:0] setting.

Both of the following conditions are satisfied:

- The PIPEnTRE.TRENB bit = 1
- The USBFS received a short packet.

Both of the following conditions are satisfied:

- The PIPEnTRE.TRENB bit = 1
- The PIPEnTRE.TRCLR bit was set to 1 by software.

For transmitting pipes, set the TRNCNT[15:0] bits to 0. When the transaction counter is not used, set the TRNCNT[15:0] bits to 0.

Setting the number of transactions to be transferred to the TRNCNT[15:0] bits is only enabled when the PIPEnTRE.TRENB bit is 0. To set the number of transactions to be transferred, set the TRCLR bit to 1 to clear the current counter value before setting the PIPEnTRE.TRENB bit to 1.

32.2.34 PIPEn事务计数器寄存器(PIPEnTRN)(n=1到5)

Address(es): USBFS.PIPE1TRN 4009 0092h, USBFS.PIPE2TRN 4009 0096h, USBFS.PIPE3TRN 4009 009Ah, USBFS.PIPE4TRN 4009 009Eh, USBFS.PIPE5TRN 4009 00A2h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TRNCNT[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b15 to b0	TRNCNT[15:0]	交易柜台	写入时，该位指定所选管道要接收的总数据包（事务数）。读取时，当PIPEnTRE.TRENB为0时，该位指示指定的事务数。当PIPEnTRE.TRENB为1时，该位指示当前事务计数。	R/W

PIPEnTRN寄存器在USB总线复位期间保留其设置。

TRNCNT[15:0]位（事务计数器）

当接收到数据包时满足以下所有条件时，USBFS将TRNCNT[15:0]位的值加1：

- PIPEnTRE.TRENB位=1
- (TRNCNT[15:0]设定值≠当前计数器值+1)收到数据包
- 接收到的数据包的有效负载与PIPEMAXP.MXPS[8:0]设置一致。

当满足以下任一条件时，USBFS将TRNCNT[15:0]位的值清零：

满足以下所有条件：

- PIPEnTRE.TRENB位=1
- (TRNCNT[15:0]设置值=当前计数器值+1)接收数据包时
- 接收到的数据包的有效负载与PIPEMAXP.MXPS[8:0]设置一致。

满足以下两个条件：

- PIPEnTRE.TRENB位=1
- USBFS收到一个短数据包。

满足以下两个条件：

- PIPEnTRE.TRENB位=1
- PIPEnTRE.TRCLR位由软件设置为1。

对于传输管道，将TRNCNT[15:0]位设置为0。当不使用事务计数器时，将TRNCNT[15:0]位设置为0。

设置要传输到TRNCNT[15:0]位的事务数仅在PIPEnTRE.TRENB位为0。要设置要传输的事务数，请将TRCLR位设置为1以清除当前计数器值，然后再将PIPEnTRE.TRENB位设置为1。

32.2.35 Device Address n Configuration Register (DEVADDn) (n = 0 to 5)

Address(es): USBFS.DEVADD0 4009 00D0h, USBFS.DEVADD1 4009 00D2h, USBFS.DEVADD2 4009 00D4h, USBFS.DEVADD3 4009 00D6h, USBFS.DEVADD4 4009 00D8h, USBFS.DEVADD5 4009 00DAh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	USBSPD[1:0]		—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b5 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7, b6	USBSPD[1:0]	Transfer Speed of Communication Target Device	b7 b6 0 0: Do not use DEVADDn 0 1: Low-speed 1 0: Full-speed 1 1: Setting prohibited.	R/W
b15 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The DEVADDn register specifies the transfer speed of the peripheral device that is the communication target for pipes 0 to 9.

In host controller mode, set all DEVADDn bits before starting communication to any pipes. Only change the bits in DEVADDn when no valid pipes are using the bit settings. A valid pipe is defined as one that satisfies both of the following conditions:

- DEVADDn is selected in the DEVSEL[3:0] bits
- The PID[1:0] bits are set to BUF for the selected pipe, or the selected pipe is the DCP with the DCPCTR.SUREQ bit set to 1.

In device controller mode, set all bits in this register to 0.

USBSPD[1:0] bits (Transfer Speed of Communication Target Device)

The USBSPD[1:0] bits specify the USB transfer speed of the target peripheral device. Set these bits to 10b when a full-speed device is connected through the hub. In host controller mode, the USBFS generates packets based on the USBSPD[1:0] setting. In device controller mode, set these bits to 00b.

32.2.36 PHY Cross Point Adjustment Register (PHYSLEW)

Address(es): USBFS.PHYSLEW 4009 00F0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	x	0	x	x	0	0	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	SLEWF01	SLEWF00	SLEWR01	SLEWR00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b0	SLEWR00	Driver Cross Point Adjustment 00	0: Reserved 1: Host or device controller mode.	R/W
b1	SLEWR01	Driver Cross Point Adjustment 01	0: Host or device controller mode 1: Reserved.	R/W

32.2.35 器件地址n配置寄存器(DEVADDn)(n=0到5)

Address(es): USBFS.DEVADD0 4009 00D0h, USBFS.DEVADD1 4009 00D2h, USBFS.DEVADD2 4009 00D4h, USBFS.DEVADD3 4009 00D6h, USBFS.DEVADD4 4009 00D8h, USBFS.DEVADD5 4009 00DAh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	USBSPD[1:0]		—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b5 to b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b7, b6	USBSPD[1:0]	通讯传输速度 目标设备	b7b600：不使用DEVADDn 01：低速10：全速11：禁止设置。	R/W
b15 to b8	—	Reserved	这些位被读取为0。写入值应为0。	R/W

DEVADDn寄存器指定作为管道0到9的通信目标的外围设备的传输速度。

在主机控制器模式下，在开始与任何管道通信之前设置所有DEVADDn位。仅更改中的位DEVADDn当没有有效管道使用位设置时。有效管道被定义为同时满足以下两个条件的管道：

- DEVADDn在DEVSEL[3:0]位中选择
- 所选管道的PID[1:0]位设置为BUF，或者所选管道是DCPCTR.SUREQ位设置为1的DCP。

在设备控制器模式下，将此寄存器中的所有位设置为0。

USBSPD[1:0]位（通信目标设备的传输速度）

USBSPD[1:0]位指定目标外围设备的USB传输速度。当通过集线器连接全速设备时，将这些位设置为10b。在主机控制器模式下，USBFS根据USBSPD[1:0]设置生成数据包。在设备控制器模式下，将这些位设置为00b。

32.2.36 PHY交叉点调整寄存器（PHYSLEW）

Address(es): USBFS.PHYSLEW 4009 00F0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	x	0	x	x	0	0	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	SLEWF01	SLEWF00	SLEWR01	SLEWR00
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0

x: Undefined

Bit	Symbol	位名称	Description	R/W
b0	SLEWR00	司机交叉点 Adjustment 00	0：保留1：主机或设备控制器模式。	R/W
b1	SLEWR01	司机交叉点 Adjustment 01	0：主机或设备控制器模式1：保留。	R/W

Bit	Symbol	Bit name	Description	R/W
b2	SLEWF00	Driver Cross Point Adjustment 00	0: Reserved 1: Host or device controller mode.	R/W
b3	SLEWF01	Driver Cross Point Adjustment 01	0: Host or device controller mode 1: Reserved.	R/W
b15 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b17, b16	—	Reserved	The read value is undefined. The write value should be 0.	R/W
b19, b18	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b21, b20	—	Reserved	The read value is undefined. The write value should be 0.	R/W
b22	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b23	—	Reserved	The read value is undefined. The write value should be 0.	R/W
b31 to b24	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The PHYSLEW register adjusts the cross point of the driver. In both host and device controller modes, set this register before operating the controller.

32.2.37 Deep Software Standby USB Transceiver Control/Pin Monitor Register (DPUSR0R)

Address(es): USBFS.DPUSR0R 4009 0400h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	DVBSTS0	—	DOVCB0	DOVCA0	—	—	DM0	DP0
Value after reset:	0	0	0	0	0	0	0	0	x	0	x	x	0	0	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	FIXPHY0	DRPD0	—	RPUE0	SRPC0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b0	SRPC0	USB Single-ended Receiver Control	0: Disable input through DP and DM inputs 1: Enable input through DP and DM inputs.	R/W
b1	RPUE0*1	DP Pull-Up Resistor Control	0: Disable DP pull-up resistor 1: Enable DP pull-up resistor.	R/W
b2	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b3	DRPD0*1	D+/D- Pull-Down Resistor Control	0: Disable DP/DM pull-down resistor 1: Enable DP/DM pull-down resistor.	R/W
b4	FIXPHY0	USB Transceiver Output Fix	0: Fix outputs in Normal mode and on return from Deep Software Standby mode 1: Fix outputs on transition to Deep Software Standby mode.	R/W
b15 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b16	DP0	USB D+ Input	Indicates D+ input signal on the USBFS side	R
b17	DM0	USB D- Input	Indicates D- input signal on the USBFS side	R
b19, b18	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b20	DOVCA0	USB OVRCURA Input	Indicates OVRCURA input signal on the USBFS side	R
b21	DOVCB0	USB OVRCURB Input	Indicates OVRCURB input signal on the USBFS side	R
b22	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b23	DVBSTS0	USB VBUS Input	Indicates VBUS input signal on the USBFS side	R
b31 to b24	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Use this bit during operation in Deep Software Standby mode. For details, see section 32.3.1.5, Release from deep software

Bit	Symbol	位名称	Description	R/W
b2	SLEWF00	司机交叉点 Adjustment 00	0：保留1：主机或设备控制器模式。	R/W
b3	SLEWF01	司机交叉点 Adjustment 01	0：主机或设备控制器模式1：保留。	R/W
b15 to b4	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b17, b16	—	Reserved	读取值未定义。写入值应为0。	R/W
b19, b18	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b21, b20	—	Reserved	读取值未定义。写入值应为0。	R/W
b22	—	Reserved	该位读取为0。写入值应为0。	R/W
b23	—	Reserved	读取值未定义。写入值应为0。	R/W
b31 to b24	—	Reserved	这些位被读取为0。写入值应为0。	R/W

PHYSLEW寄存器调整驱动器的交叉点。在主机和设备控制器模式下，请在操作控制器之前设置此寄存器。

32.2.37 深度软件待机USB收发器控制引脚监控寄存器(DPUSR0R)

Address(es): USBFS.DPUSR0R 4009 0400h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	DVBSTS0	—	DOVCB0	DOVCA0	—	—	DM0	DP0
重置后的值：	0	0	0	0	0	0	0	0	x	0	x	x	0	0	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	FIXPHY0	DRPD0	—	RPUE0	SRPC0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

x: Undefined

Bit	Symbol	位名称	Description	R/W
b0	SRPC0	USB Single-ended 接收机控制	0：禁用通过DP和DM输入的输入1：启用通过DP和DM输入的输入。	R/W
b1	RPUE0*1	DP Pull-Up Resistor Control	0：禁用DP上拉电阻1：启用DP上拉电阻。	R/W
b2	—	Reserved	该位读取为0。写入值应为0。	R/W
b3	DRPD0*1	D+/D- Pull-Down Resistor Control	0：禁用DPDM下拉电阻1：启用DPDM下拉电阻。	R/W
b4	FIXPHY0	USB收发器输出 Fix	0：在正常模式和从深度软件待机模式返回时修复输出1：在转换到深度软件待机模式时修复输出。	R/W
b15 to b5	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b16	DP0	USBD+输入	指示USBFS侧的D+输入　　信号	R
b17	DM0	USB D- Input	指示USBFS侧的Dinput信号	R
b19, b18	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b20	DOVCA0	USBOVRCURA输入	指示USBFS侧的OVRCURA输入信号	R
b21	DOVCB0	USBOVRCURB输入	指示USBFS侧的OVRCURB输入信号	R
b22	—	Reserved	该位读取为0。写入值应为0。	R/W
b23	DVBSTS0	USBVBUS输入	指示USBFS侧的VBUS输入信号	R
b31 to b24	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 在深度软件待机模式下操作期间使用该位。有关详细信息，请参阅第32.3.1.5节，从深度软件发布

standby mode because of USB suspend/resume interrupts.

SRPC0 bit (USB Single-ended Receiver Control)

The SRPC0 bit controls the D+ and D- inputs of the USB transceiver. This bit is only valid when the FIXPHY0 bit is 1.

FIXPHY0 bit (USB Transceiver Output Fix)

The FIXPHY0 bit keeps the outputs of the USB transceiver disabled.

32.2.38 Deep Software Standby USB Suspend/Resume Interrupt Register (DPUSR1R)

Address(es): USBFS.DPUSR1R 4009 0404h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	DVBINT0	—	DOVRCRB0	DOVRCRA0	—	—	DMINT0	DPINT0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	DVBSE0	—	DOVRCRBE0	DOVRCRAE0	—	—	DMINTE0	DPINTE0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	DPINTE0	USB DP Interrupt Enable/Clear	0: Disable recovery from Deep Software Standby mode by DP input 1: Enable recovery from Deep Software Standby mode by DP input.	R/W
b1	DMINTE0	USB DM Interrupt Enable/Clear	0: Disable recovery from Deep Software Standby mode by DM input 1: Enable recovery from Deep Software Standby mode by DM input.	R/W
b3, b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	DOVRCRAE0	USB OVRCURA Interrupt Enable/Clear	0: Disable recovery from Deep Software Standby mode by OVRCURA input 1: Enable recovery from Deep Software Standby mode by OVRCURA input.	R/W
b5	DOVRCRBE0	USB OVRCURB Interrupt Enable/Clear	0: Disable recovery from Deep Software Standby mode by OVRCURB input 1: Enable recovery from Deep Software Standby mode by OVRCURB input.	R/W
b6	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b7	DVBSE0	USB VBUS Interrupt Enable/Clear	0: Disable recovery from Deep Software Standby mode by VBUS input 1: Enable recovery from Deep Software Standby mode by VBUS input.	R/W
b15 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b16	DPINT0	USB DP Interrupt Source Recovery	0: System has not recovered from Deep Software Standby mode 1: System recovered from Deep Software Standby mode because of DP.	R
b17	DMINT0	USB DM Interrupt Source Recovery	0: System has not recovered from Deep Software Standby mode 1: System recovered from Deep Software Standby mode because of DM input.	R
b19, b18	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b20	DOVRCRA0	USB OVRCURA Interrupt Source Recovery	0: System has not recovered from Deep Software Standby mode 1: System recovered from Deep Software Standby mode because of OVRCURA input.	R

待机模式因为USB暂停恢复中断。

SRPC0位（USB单端接收器控制）

SRPC0位控制USB收发器的D+和D-输入。该位仅在FIXPHY0位为1时有效。

FIXPHY0位（USB收发器输出修复）

FIXPHY0位保持禁用USB收发器的输出。

32.2.38 深度软件待机USB挂起恢复中断寄存器(DPUSR1R)

Address(es): USBFS.DPUSR1R 4009 0404h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	DVBINT0	—	DOVRCRB0	DOVRCRA0	—	—	DMINT0	DPINT0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	DVBSE0	—	DOVRCRBE0	DOVRCRAE0	—	—	DMINTE0	DPINTE0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	DPINTE0	USBDP中断 Enable/Clear	0：禁止通过DP输入从深度软件待机模式恢复1：允许通过DP输入从深度软件待机模式恢复。	R/W
b1	DMINTE0	USBDM中断 Enable/Clear	0：禁止通过DM输入从深度软件待机模式恢复1：通过DM输入启用从深度软件待机模式恢复。	R/W
b3, b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b4	DOVRCRAE0	USBOVRCURA中断 Enable/Clear	0：通过OVRCURA输入禁止从深度软件待机模式恢复1：通过OVRCURA输入允许从深度软件待机模式恢复。	R/W
b5	DOVRCRBE0	USBOVRCURB中断 Enable/Clear	0：禁用通过OVRCURB输入从深度软件待机模式恢复1：通过OVRCURB输入启用从深度软件待机模式恢复。	R/W
b6	—	Reserved	该位读取为0。写入值应为0。	R/W
b7	DVBSE0	USBVBUS中断 Enable/Clear	0：禁止通过VBUS输入从深度软件待机模式恢复1：使能通过VBUS输入从深度软件待机模式恢复。	R/W
b15 to b8	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b16	DPINT0	USBDP中断源 Recovery	0：系统尚未从深度软件待机模式中恢复1：系统由于DP从深度软件待机模式中恢复。	R
b17	DMINT0	USBDM中断源 Recovery	0：系统尚未从深度软件待机模式中恢复1：系统由于DM输入而从深度软件待机模式中恢复。	R
b19, b18	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b20	DOVRCRA0	USBOVRCURA中断源恢复	0：系统尚未从深度软件待机模式中恢复1：系统由于OVRCURA输入而从深度软件待机模式中恢复。	R

Bit	Symbol	Bit name	Description	R/W
b21	DOVRCRB0	USB OVRCURB Interrupt Source Recovery	0: System has not recovered from Deep Software Standby mode 1: System recovered from Deep Software Standby mode because of OVRCURB input.	R
b22	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b23	DVBINT0	USB VBUS Interrupt Source Recovery	0: System has not recovered from Deep Software Standby mode 1: System recovered from Deep Software Standby mode because of VBUS input.	R
b31 to b24	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

DPINTE0 bit (USB DP Interrupt Enable/Clear)

The DPINET0 bit enables or disables triggering of recovery from Deep Software Standby mode by the DP input of the USBFS. Writing 0 to this bit while the DPINT0 bit is 1 sets the DPINT0 bit to 0.

DMINTE0 bit (USB DM Interrupt Enable/Clear)

The DMINTE0 bit enables or disables triggering of recovery from Deep Software Standby mode by the DM input of the USBFS. Writing 0 to this bit while the DMINT0 bit is 1 clears the DMINTE0 bit to 0.

DOVRCRAE0 bit (USB OVRCURA Interrupt Enable/Clear)

The DOVRCRAE0 bit enables or disables triggering of recovery from Deep Software Standby mode by the OVRCURA input of the USBFS. Writing 0 to this bit while the DOVRCRA0 bit is 1 clears the DOVRCRAE0 bit to 0.

DOVRCRBE0 bit (USB OVRCURB Interrupt Enable/Clear)

The DOVRCRBE0 bit enables or disables triggering of recovery from Deep Software Standby mode by the OVRCURB input of the USBFS. Writing 0 to this bit while the DOVRCRB0 bit is 1 clears the DOVRCRB0 bit to 0.

DVBSE0 bit (USB VBUS Interrupt Enable/Clear)

The DVBSE0 bit enables or disables triggering of recovery from Deep Software Standby mode by the VBUS input of the USBFS. Writing 0 to this bit while the DVBINT0 bit is 1 clears the DVBINT0 bit to 0.

DPINT0 bit (USB DP Interrupt Source Recovery)

The DPINT0 bit indicates that the system has returned from Deep Software Standby mode because of the DP input of the USBFS. This recovery is only enabled when the DPINTE0 bit is 1. Writing 0 to the DPINTE0 bit while this bit is 1 clears this bit to 0.

DMINT0 bit (USB DM Interrupt Source Recovery)

The DMINT0 bit indicates that the system has returned from Deep Software Standby mode because of the DM input of the USBFS. This recovery is only enabled when the DMINTE0 bit is 1. Writing 0 to the DPINTE0 bit while this bit is 1 clears this bit to 0.

DOVRCRA0 bit (USB OVRCURA Interrupt Source Recovery)

The DOVRCRA0 bit indicates that the system has returned from Deep Software Standby mode because of the OVRCURA input of the USBFS. This recovery is only enabled when the DOVRCRAE0 bit is 1. Writing 0 to the DOVRCRAE0 bit while this bit is 1 clears this bit to 0.

DOVRCRB0 bit (USB OVRCURB Interrupt Source Recovery)

The DOVRCRB0 bit indicates that the system has returned from Deep Software Standby mode because of the OVRCURB input of the USBFS. This recovery is only enabled when the DOVRCRBE0 bit is 1. Writing 0 to the DOVRCRBE0 bit while this bit is 1 clears this bit to 0.

DVBINT0 bit (USB VBUS Interrupt Source Recovery)

The DVBINT0 bit indicates that the system has returned from Deep Software Standby mode because of the VBUS input of the USBFS. This recovery is only enabled when the DVBSE0 bit is 1. Writing 0 to the DVBSE0 bit while this bit is 1 clears this bit to 0.

Bit	Symbol	位名称	Description	R/W
b21	DOVRCRB0	USBOVRCURB中断源恢复	0：系统尚未从深度软件待机模式中恢复1：系统由于OVRCURB输入而从深度软件待机模式中恢复。	R
b22	—	Reserved	该位读取为0。写入值应为0。	R/W
b23	DVBINT0	USBVBUS中断源恢复	0：系统尚未从深度软件待机模式中恢复1：系统由于VBUS输入而从深度软件待机模式中恢复。	R
b31 to b24	—	Reserved	这些位被读取为0。写入值应为0。	R/W

DPINTE0位（USBDP中断使能清除）

DPINET0位启用或禁用触发从深度软件待机模式恢复由DP输入USBFS。当DPINT0位为1时向该位写入0会将DPINT0位设置为0。

DMINTE0位（USBDM中断使能清除）

DMINTE0位启用或禁用触发从深度软件待机模式恢复由DM输入USBFS。当DMINT0位为1时向该位写入0会将DMINTE0位清除为0。

DOVRCRAE0位（USBOVRCURA中断使能清除）

DOVRCRAE0位通过USBFS的OVRCURA输入启用或禁用从深度软件待机模式恢复的触发。当DOVRCRA0位为1时向该位写入0会将DOVRCRAE0位清除为0。

DOVRCRBE0位（USBOVRCURB中断使能清除）

DOVRCRBE0位通过USBFS的OVRCURB输入启用或禁用从深度软件待机模式恢复的触发。当DOVRCRB0位为1时向该位写入0会将DOVRCRB0位清除为0。

DVBSE0位（USBVBUS中断使能清除）

DVBSE0位通过VBUS输入启用或禁用从深度软件待机模式恢复的触发USBFS。当DVBINT0位为1时向该位写入0会将DVBINT0位清除为0。

DPINT0位（USBDP中断源恢复）

由于USBFS的DP输入，DPINT0位指示系统已从深度软件待机模式返回。此恢复仅在DPINTE0位为1时启用。当该位为1时向DPINTE0位写入0将该位清除为0。

DMINT0位（USBDM中断源恢复）

由于USBFS的DM输入，DMINT0位指示系统已从深度软件待机模式返回。此恢复仅在DMINTE0位为1时启用。当该位为1时将0写入DPINTE0位可将该位清除为0。

DOVRCRA0位（USBOVRCURA中断源恢复）

DOVRCRA0位指示系统已从深度软件待机模式返回，因为USBFS的OVRCURA输入。此恢复仅在DOVRCRAE0位为1时启用。将0写入DOVRCRAE0位当该位为1时将该位清除为0。

DOVRCRB0位（USBOVRCURB中断源恢复）

DOVRCRB0位指示系统已从深度软件待机模式返回，因为USBFS的OVRCURB输入。此恢复仅在DOVRCRBE0位为1时启用。将0写入DOVRCRBE0位当该位为1时将该位清除为0。

DVBINT0位（USBVBUS中断源恢复）

由于USBFS的VBUS输入，DVBINT0位指示系统已从深度软件待机模式返回。此恢复仅在DVBSE0位为1时启用。当该位为1时将0写入DVBSE0位可将该位清除为0。

32.3 Operation

32.3.1 System Control

This section describes register settings required for initializing the USBFS and controlling power consumption.

32.3.1.1 Setting data to the USBFS registers

Setting the SYSCFG.USBE bit to 1 after starting the clock supply (SYSCFG.SCKE bit = 1) enables and starts USBFS operation.

32.3.1.2 Selecting the controller function

The USBFS can operate as either a host or device controller.

Use the SYSCFG.DCFM bit to select one of these USBFS functions. The DCFM bit must be changed in the initial settings immediately after a reset or in the D+ pull-up-disabled state (SYSCFG.DPRPU bit = 0) and D+ and D- pull-down-disabled state (SYSCFG.DRPD bit = 0).

32.3.1.3 Controlling the USB data bus using resistors

The USBFS provides pull-up and pull-down resistors for the D+ and D- lines. Pull these lines up or down by setting the SYSCFG.DPRPU and DRPD bits.

In device controller mode, confirm that connection to the USB host is made, and then set the SYSCFG.DPRPU bit to 1 and pull up the D+ line (in full-speed communication).

When the SYSCFG.DPRPU bit is set to 0 during communication with a PC, the USBFS disables the pull-up resistor of the USB data line, thereby notifying the USB host of disconnection.

In host controller mode, set the SYSCFG.DRPD bit to 1 to pull down the D+ and D- lines.

Table 32.12 USB data bus resistor control

SYSCFG register settings		USB data bus control		
DRPD bit	DPRPU bit	D-	D+	Function
0	0	Open	Open	When resistors not used
0	1	Open	Pull-up	When operating as a device controller at full-speed
1	0	Pull-down	Pull-down	When operating as a host controller
1	1	—	—	Setting prohibited

32.3.1.4 Example external connection circuits

Figure 32.2 shows an example OTG connection in the self-powered system. The USBFS controls the pull-up resistor of the D+ line and the pull-down resistor of D+ and D- lines. Select pull-up and pull-down for the lines in the SYSCFG.DPRPU and SYSCFG.DRPD bits. In device controller mode, the pull-up resistor of USB data line is disabled if SYSCFG.DPRPU bit is set to 0 while communicating with the USB host. The USBFS can use this to notify the USB host of a device disconnect.

32.3 Operation

32.3.1 系统控制

本节介绍初始化USBFS和控制功耗所需的寄存器设置。

32.3.1.1 将数据设置到USBFS寄存器

启动时钟供应（SYSCFG.SCKE位=1）后将SYSCFG.USBE位设置为1启用并启动USBFS操作。

32.3.1.2 选择控制器功能

USBFS可以作为主机或设备控制器运行。

使用SYSCFG.DCFM位选择这些USBFS功能之一。DCFM位必须在复位后立即更改为初始设置或在D+上拉禁用状态（SYSCFG.DPRPU位=0）和D+和Dpulldown禁用状态（SYSCFG.DRPD位=0）。

32.3.1.3 使用电阻控制USB数据总线

USBFS为D+和Dlines提供上拉和下拉电阻。通过设置SYSCFG.DPRPU和DRPD位。

在设备控制器模式下，确认与USB主机的连接已建立，然后将SYSCFG.DPRPU位设置为1并拉高D+线（全速通信）。

当SYSCFG.DPRPU位在与PC通信期间设置为0时，USBFS禁用USB数据线的上拉电阻，从而通知USB主机断开连接。

在主机控制器模式下，将SYSCFG.DRPD位设置为1以拉低D+和Dlines。

Table 32.12 USB数据总线电阻控制

SYSCFG寄存器设置		USB数据总线控制		
DRPD bit	DPRPU bit	D-	D+	Function
0	0	Open	Open	不使用电阻时
0	1	Open	Pull-up	作为设备控制器全速运行时
1	0	Pull-down	Pull-down	作为主机控制器运行时
1	1	—	—	禁止设定

32.3.1.4 外部连接电路示例

图32.2显示了自供电系统中的示例OTG连接。USBFS控制D+线的上拉电阻和D+和Dlines的下拉电阻。为SYSCFG.DPRPU和SYSCFG.DRPD位中的线路选择上拉和下拉。在设备控制器模式下，如果在与USB主机通信时将SYSCFG.DPRPU位设置为0，则禁用USB数据线的上拉电阻。USBFS可以使用它来通知USB主机设备断开连接。

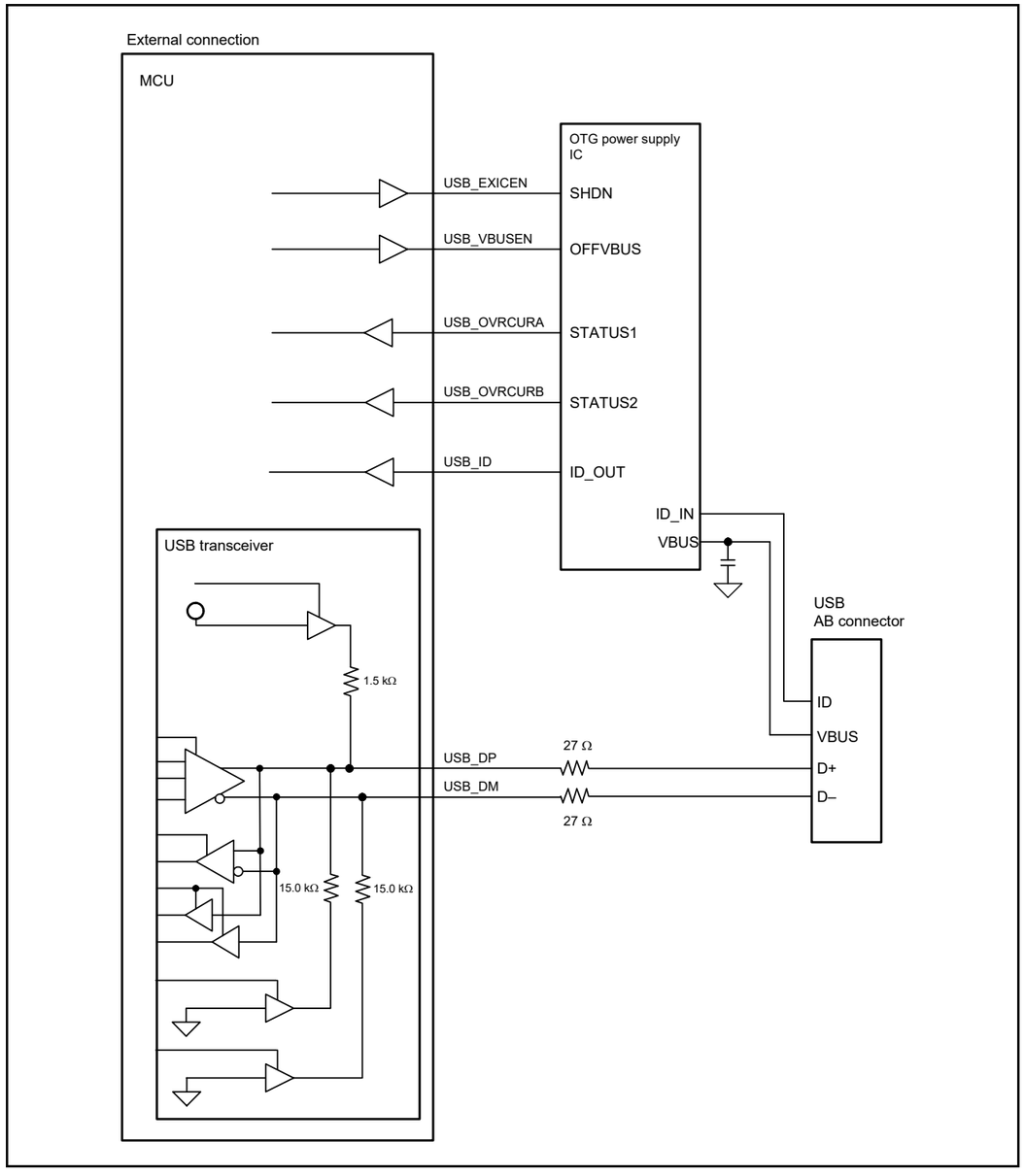


Figure 32.2 Example OTG connection in a self-powered system

Figure 32.3 shows an example device connection in a self-powered system.

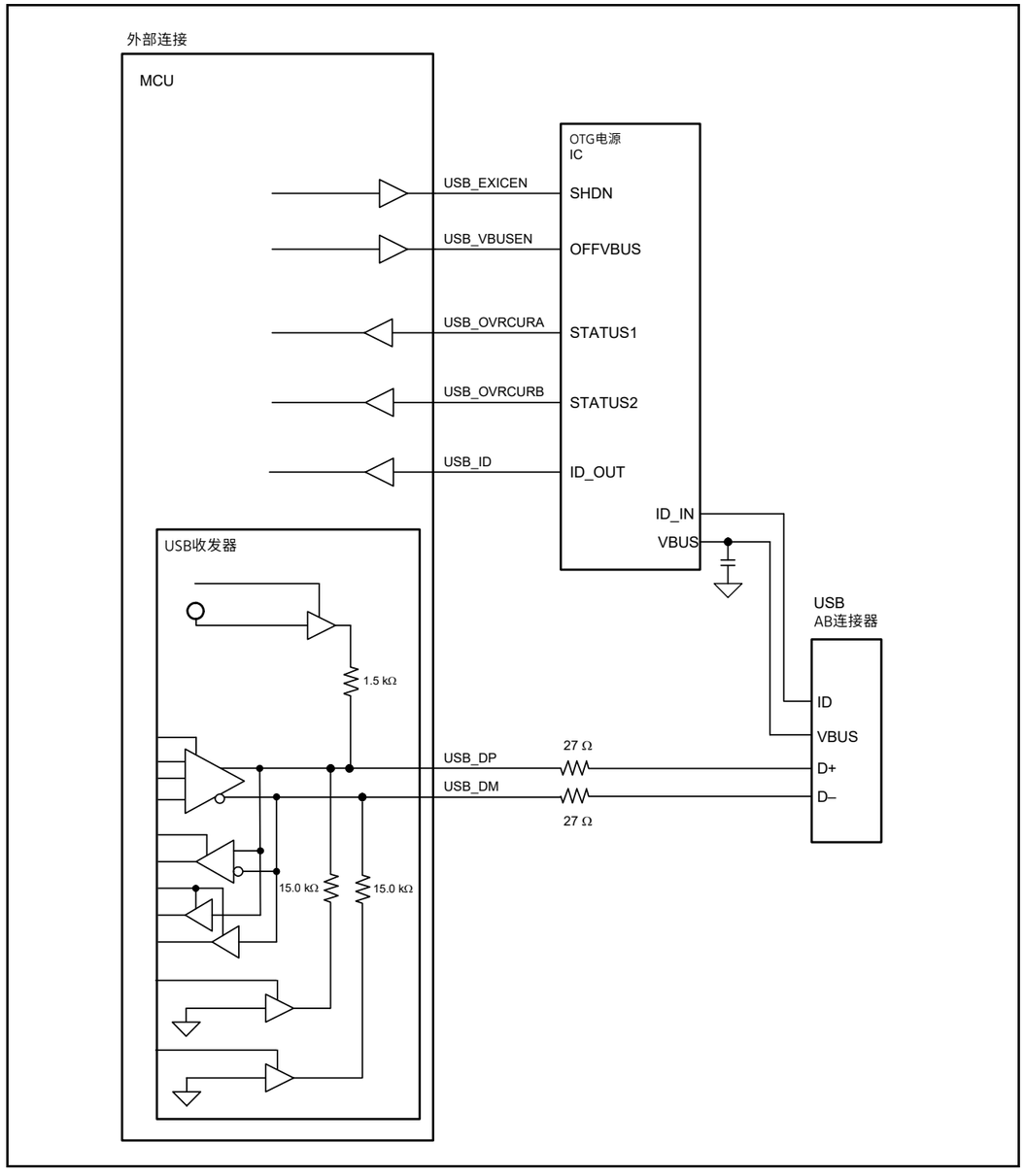
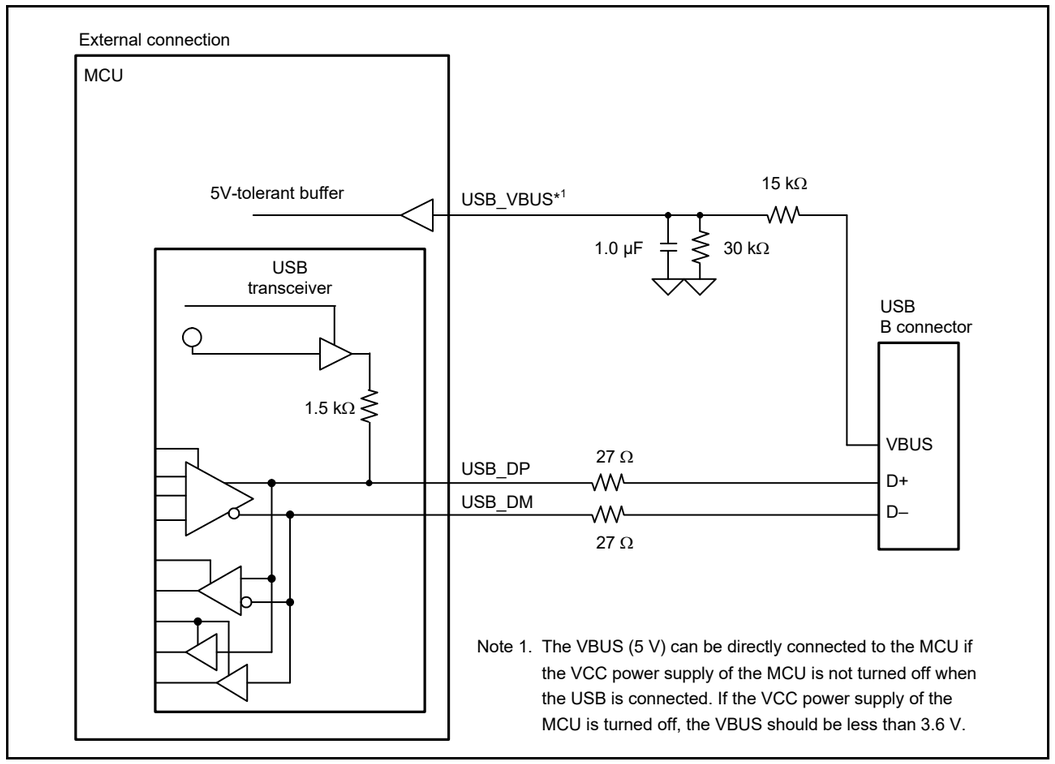


Figure 32.2 自供电系统中的示例OTG连接

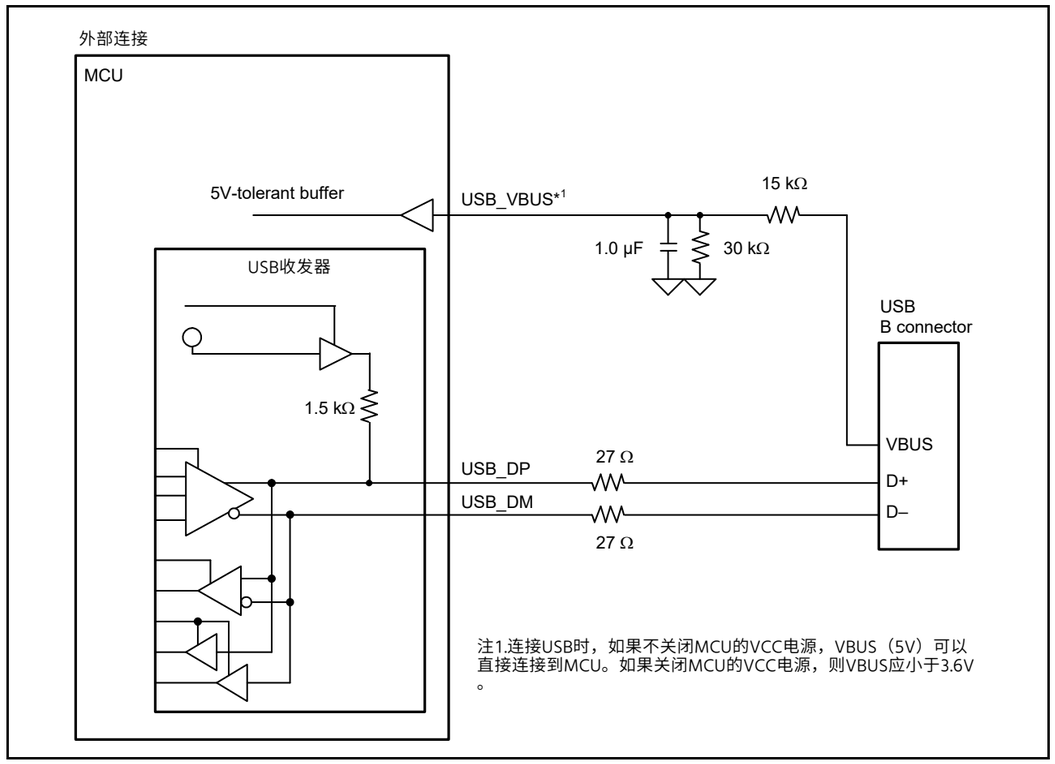
图32.3显示了自供电系统中的示例设备连接。



Note 1. The VBUS (5 V) can be directly connected to the MCU if the VCC power supply of the MCU is not turned off when the USB is connected. If the VCC power supply of the MCU is turned off, the VBUS should be less than 3.6 V.

Figure 32.3 Example device connection in a self-powered system

Figure 32.4 shows an example host connection.



注1.连接USB时，如果不关闭MCU的VCC电源，VBUS（5V）可以直接连接到MCU。如果关闭MCU的VCC电源，则VBUS应小于3.6V。

Figure 32.3 自供电系统中的示例设备连接

图32.4显示了一个示例主机连接。

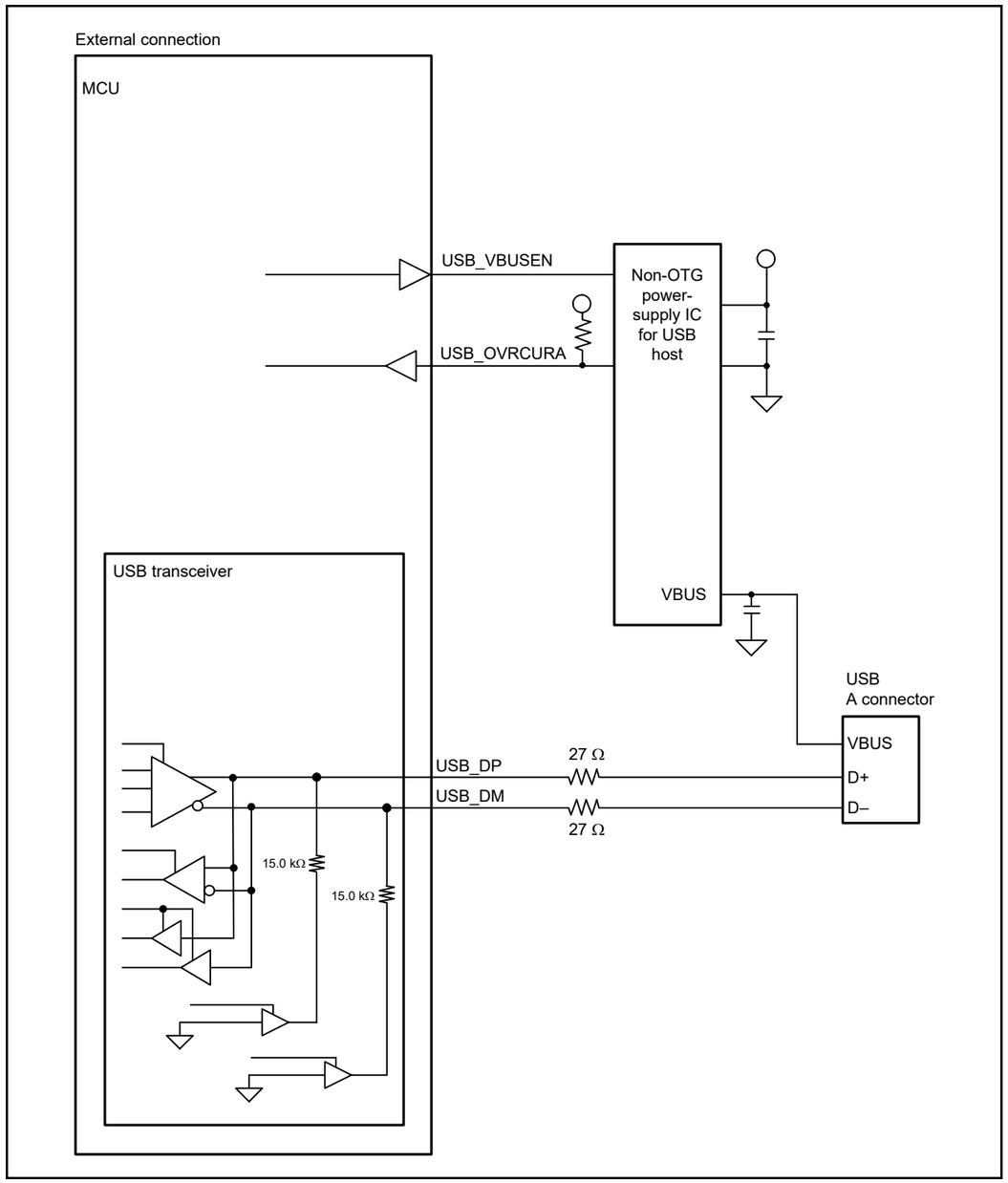


Figure 32.4 Example host connection

Figure 32.5 shows an example device connection in a bus-powered system.

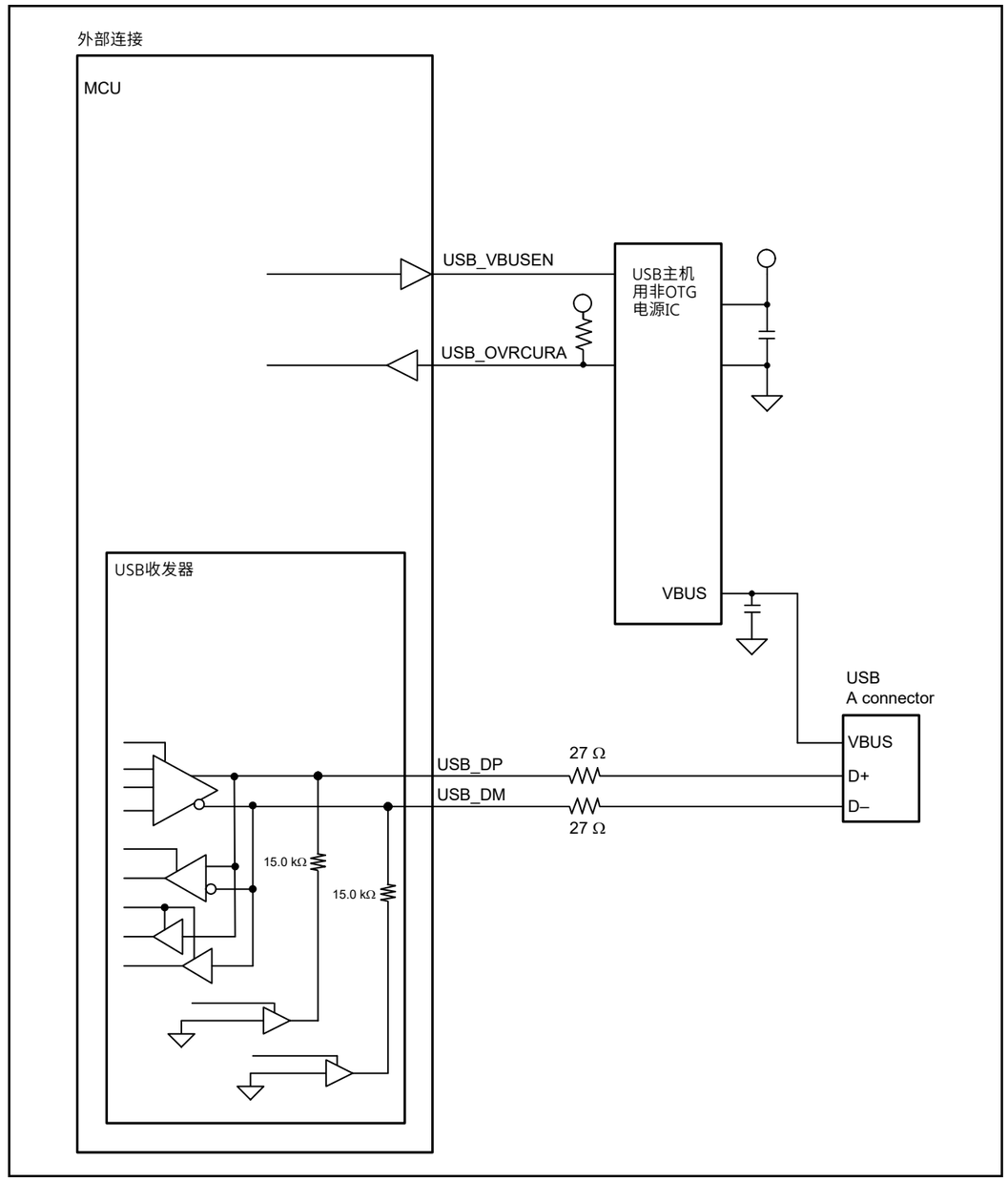


Figure 32.4 主机连接示例

图32.5显示了总线供电系统中的示例设备连接。

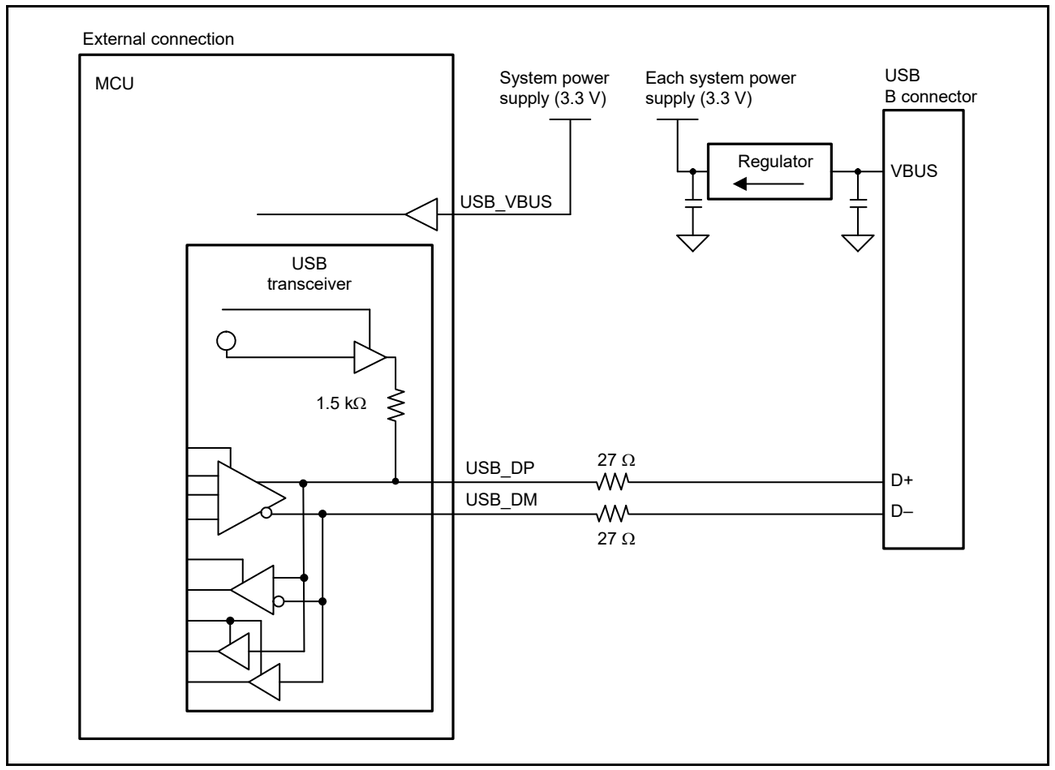


Figure 32.5 Example device connection in a bus-powered state

The examples of external circuits given in this section are simplified circuits, and their operation in every system is not guaranteed.

32.3.1.5 Release from deep software standby mode because of USB suspend/resume interrupts

Deep Software Standby mode can be canceled by a USB suspend/resume interrupt. USB suspend/resume interrupts are detected by the USB resume detecting unit, which controls and monitors the USB I/O pins to detect the interrupts.

Figure 32.6 shows a schematic diagram of the connection between the USB resume detecting unit and the USB I/O pins.

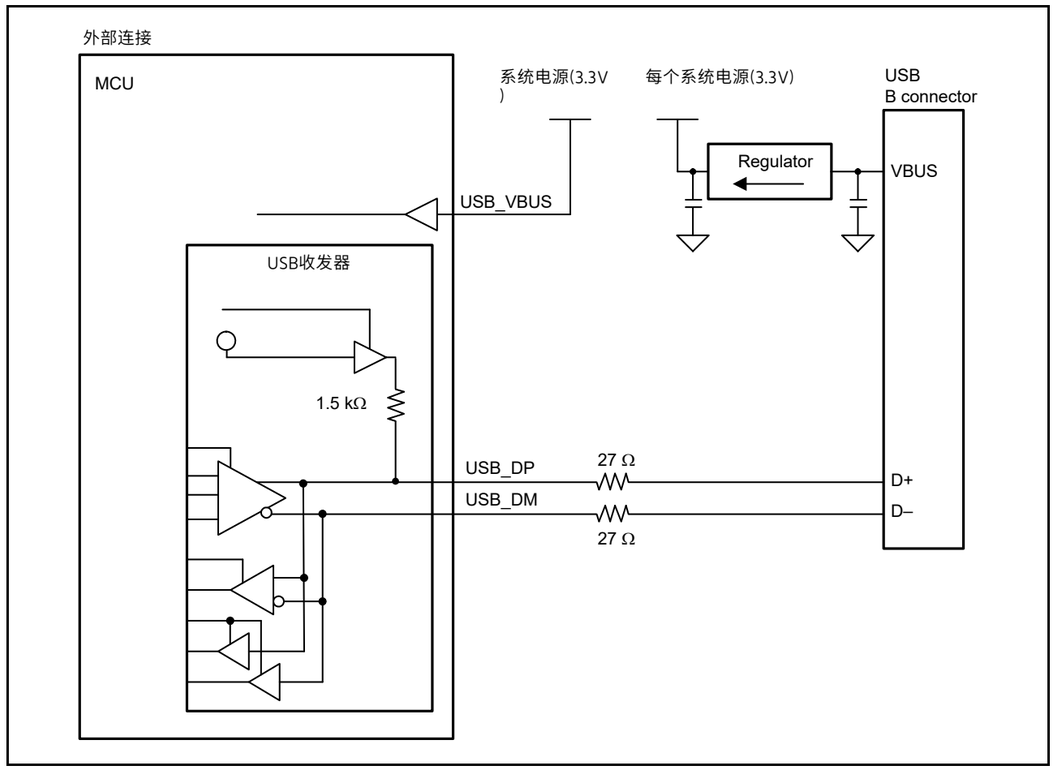


Figure 32.5 总线供电状态下的示例设备连接

本节中给出的外部电路示例是简化电路，不保证它们在每个系统中的操作。

32.3.1.5 由于USB挂起恢复中断而从深度软件待机模式中释放

深度软件待机模式可以通过USB挂起恢复中断来取消。USB暂停恢复中断由USB恢复检测单元检测，该单元控制和监视USBIO引脚以检测中断。

图32.6显示了USB恢复检测单元与USBIO引脚之间的连接示意图。

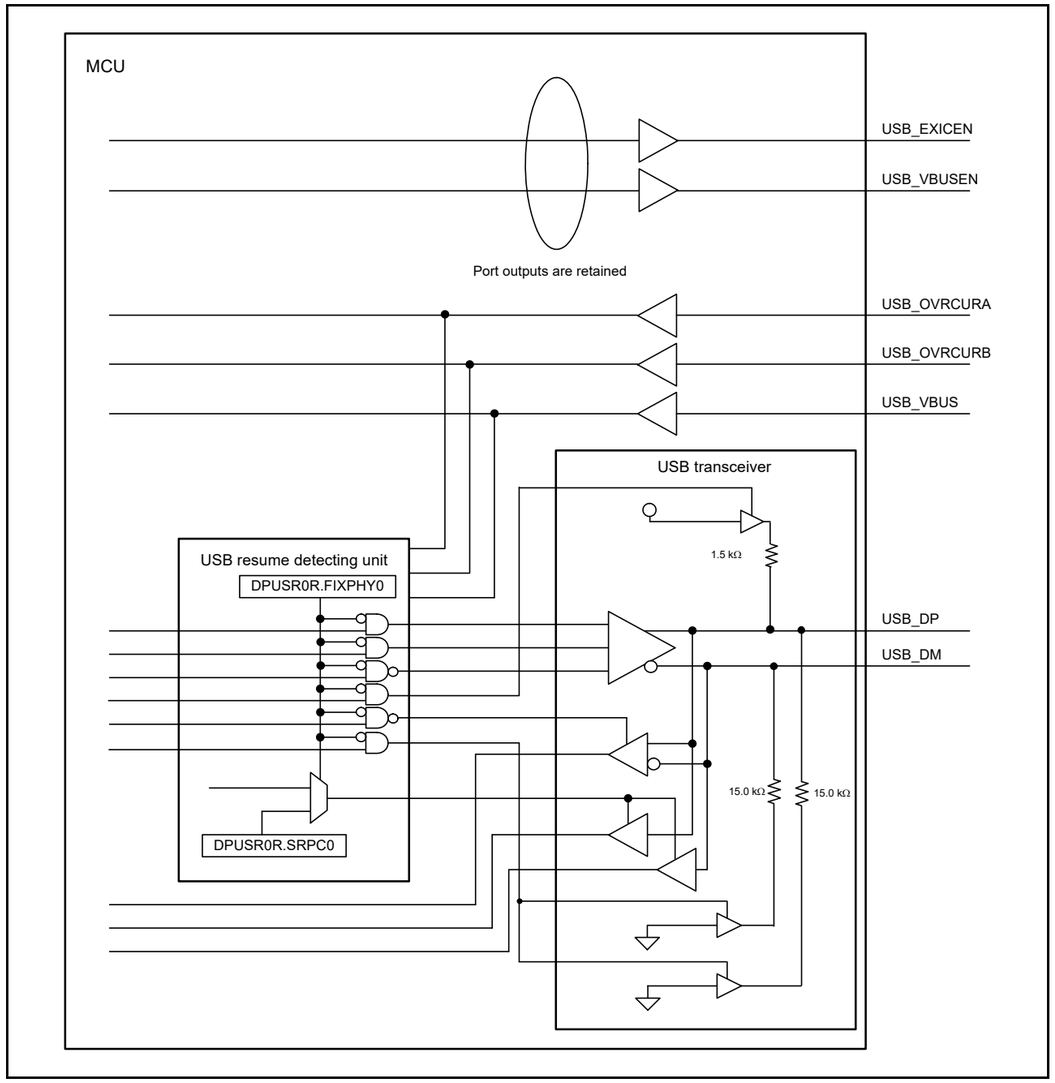


Figure 32.6 Connection between the USB resume detecting unit and the USB I/O pins

Table 32.13 shows the USB suspend and resume interrupt sources and their associated I/O pins.

Table 32.13 USB suspend and resume interrupt sources and their associated I/O pins

USB operating mode	Source	Pin name
Device, OTG	Resume	USB_DP
Host, OTG	Attach or detach	USB_DP, USB_DM
Device	Attach or detach	USB_VBUS
Host	Overcurrent detection	USB_OVRCURA
OTG	Overcurrent detection	USB_OVRCURA, USB_OVRCURB

Figure 32.7 shows the flow for setting the USBFS when entering Deep Software Standby mode from either host or device controller mode. Figure 32.8 shows the flow for setting the USBFS when canceling Deep Software Standby mode

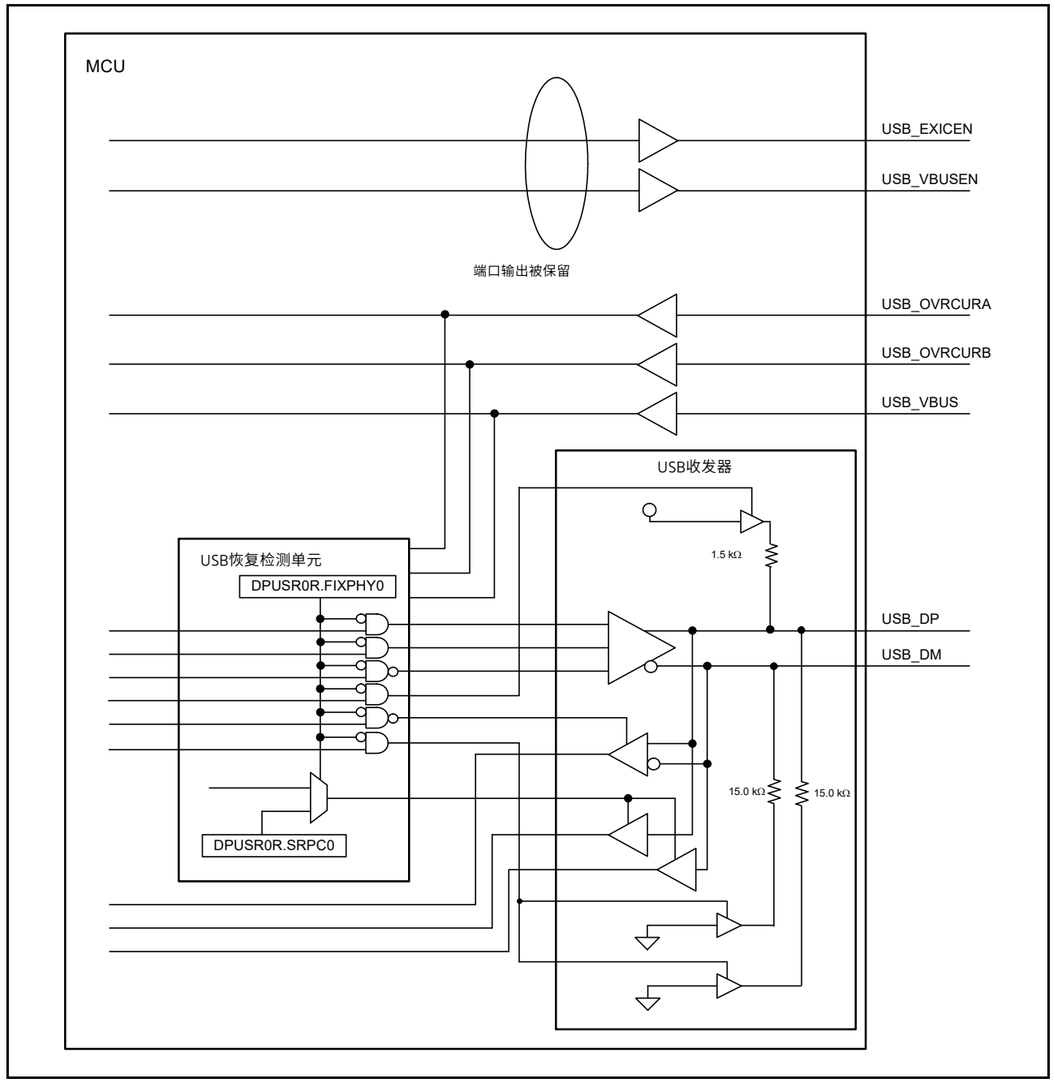


Figure 32.6 USB恢复检测单元与USBIO管脚的连接

表32.13显示了USB挂起和恢复中断源及其相关的IO引脚。

Table 32.13 USB挂起和恢复中断源及其相关的IO引脚

USB操作模式	Source	引脚名称
Device, OTG	Resume	USB_DP
Host, OTG	连接或分离	USB_DP, USB_DM
Device	连接或分离	USB_VBUS
Host	Overcurrent detection	USB_OVRCURA
OTG	Overcurrent detection	USB_OVRCURA, USB_OVRCURB

图32.7显示了从主机或设备控制器模式进入深度软件待机模式时设置USBFS的流程。图32.8显示了取消深度软件待机模式时设置USBFS的流程

from host controller mode. Figure 32.9 shows the flow for setting the USBFS when canceling Deep Software Standby mode from device controller mode.

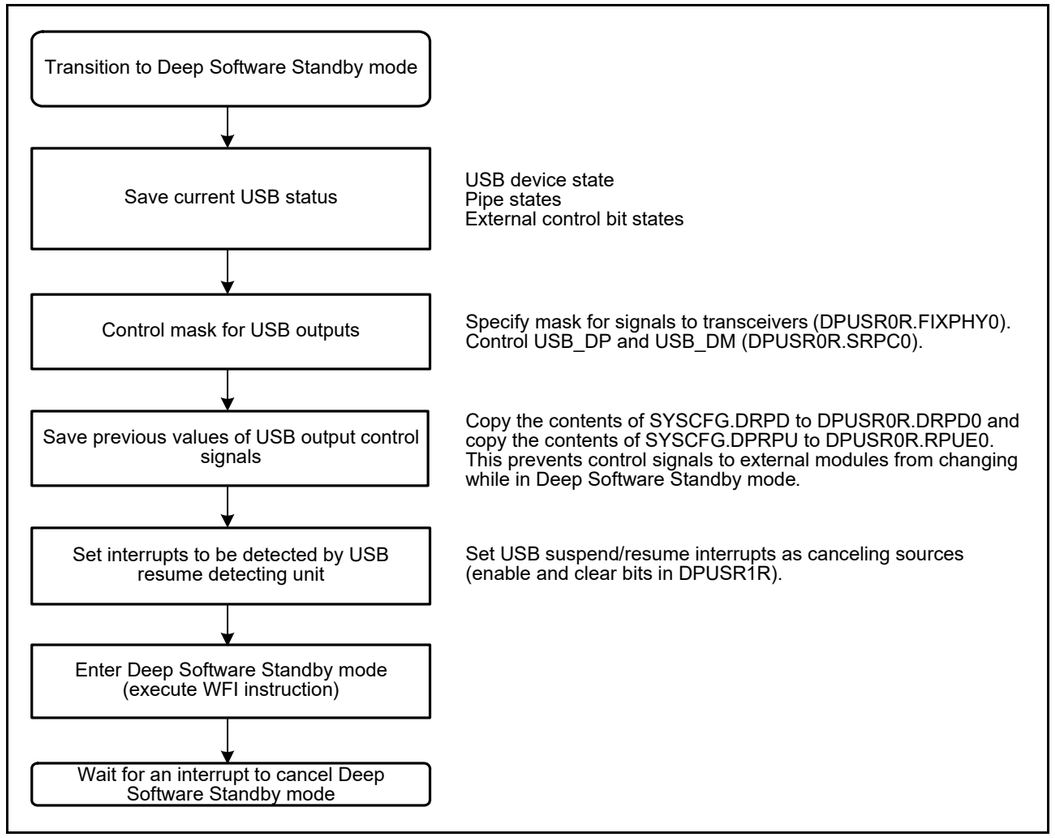


Figure 32.7 USBFS setup flow for transition to Deep Software Standby mode as host or device controller

从主机控制器模式。图32.9显示了从设备控制器模式取消深度软件待机模式时设置USBFS的流程。

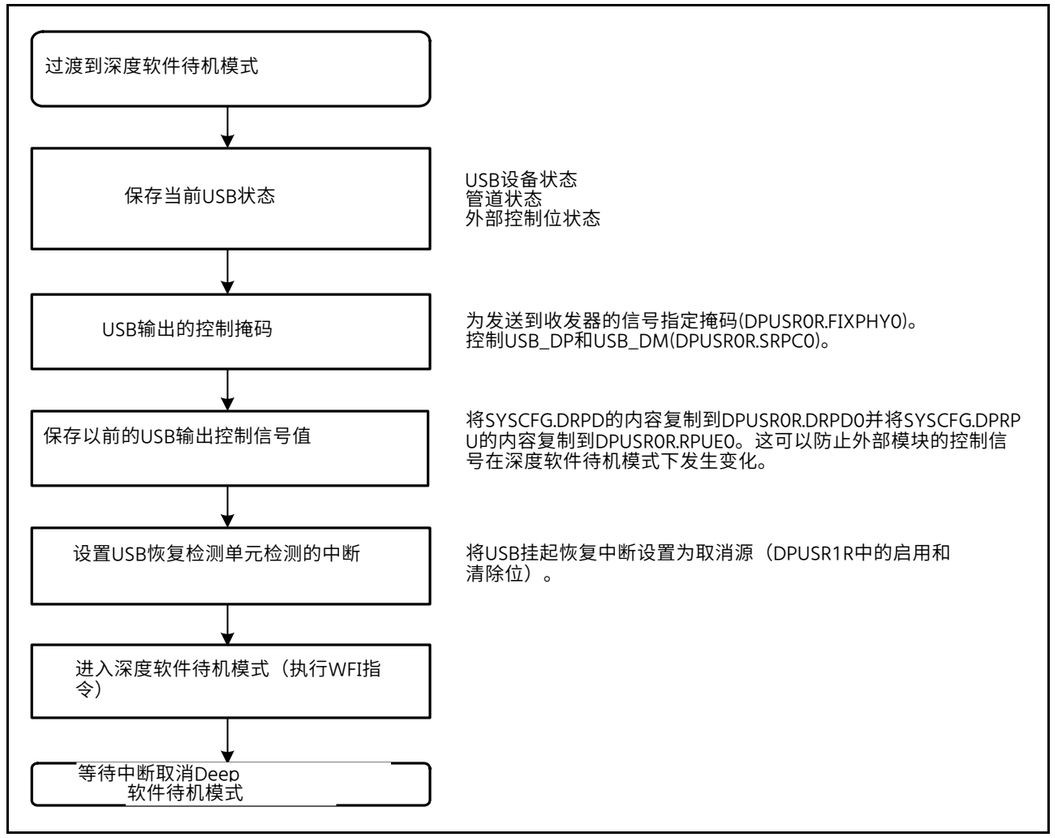


Figure 32.7 作为主机或设备控制器转换到深度软件待机模式的USBFS设置流程

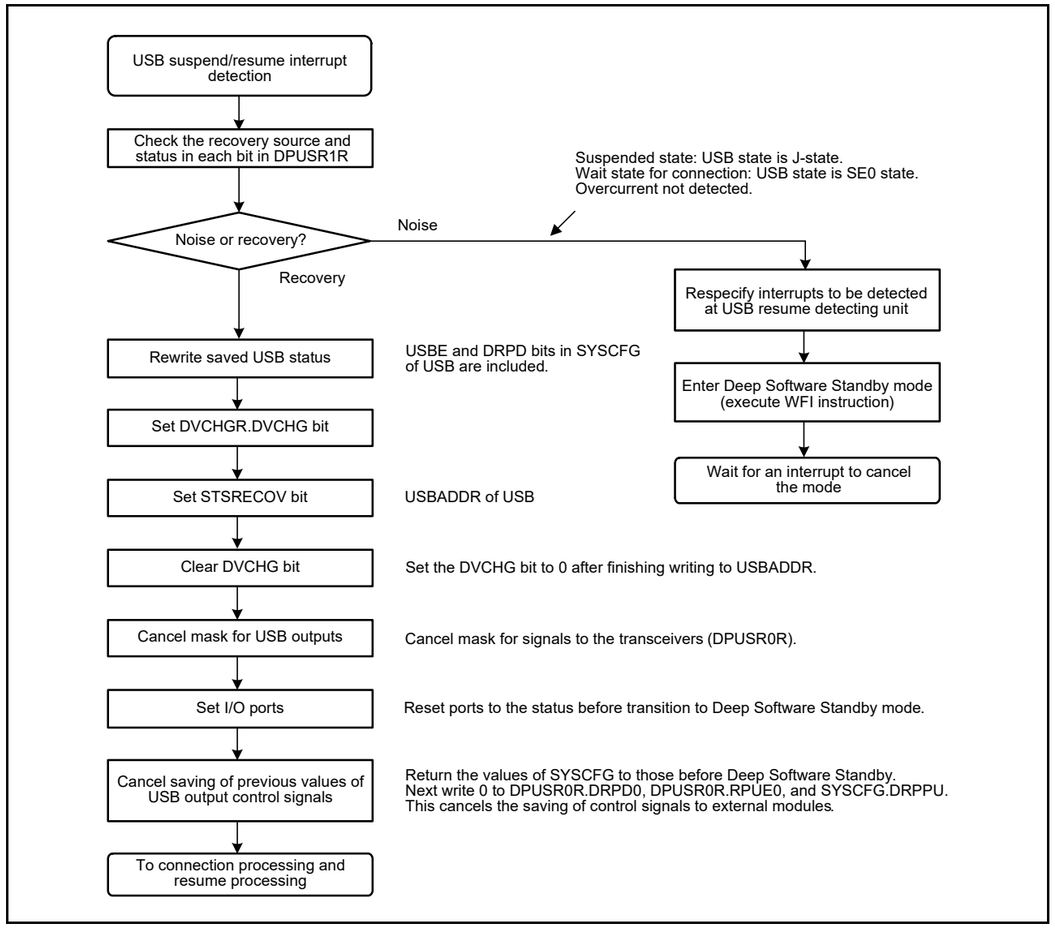


Figure 32.8 USBFS setup flow for canceling Deep Software Standby mode as host controller

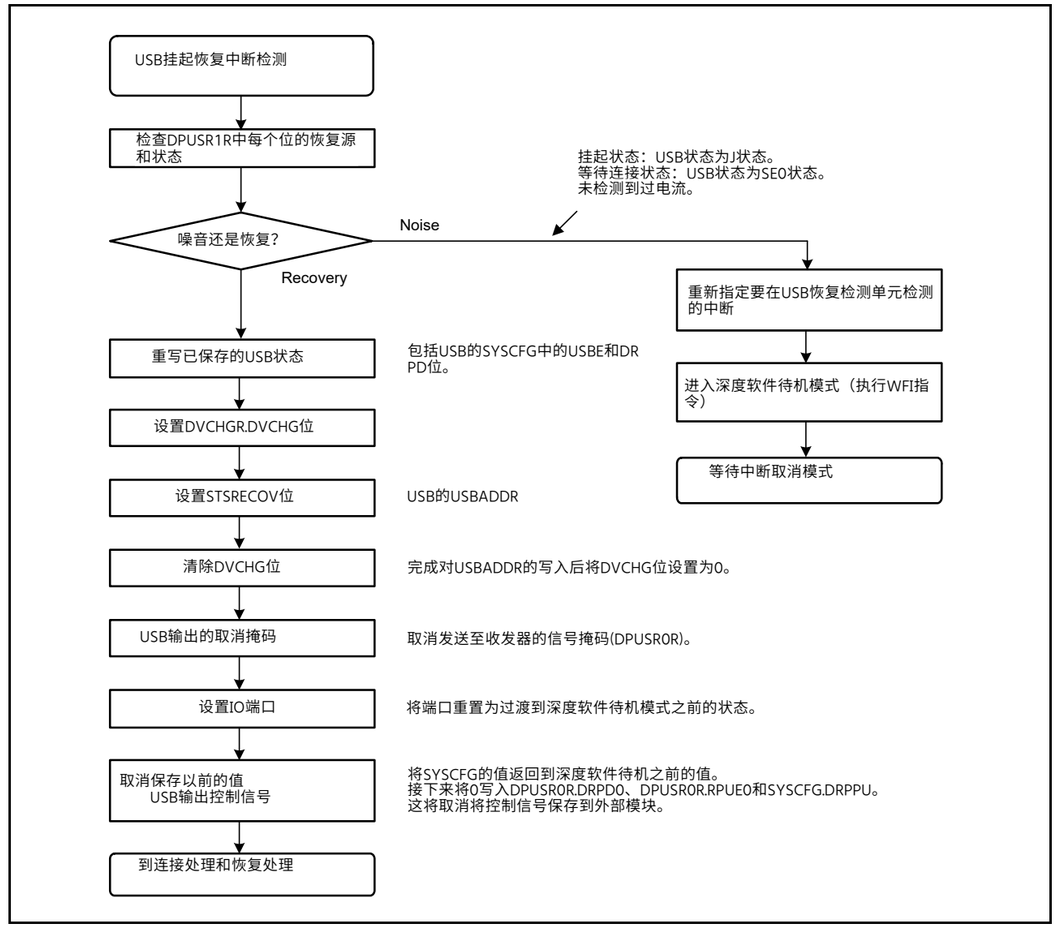


Figure 32.8 用于取消作为主机控制器的深度软件待机模式的USBFS设置流程

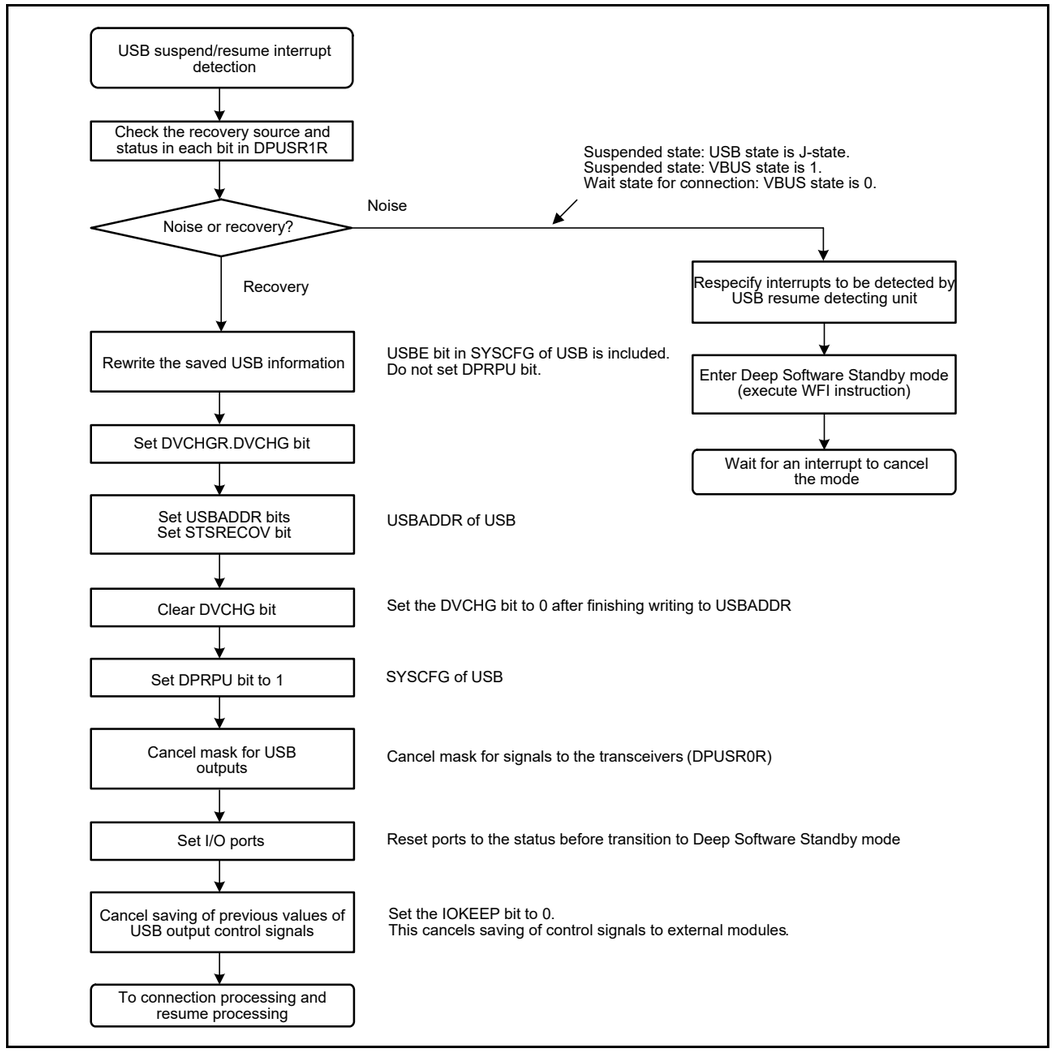


Figure 32.9 USBFS setup flow for canceling Deep Software Standby mode as device controller

32.3.2 Interrupts

Table 32.14 lists the interrupt sources in the USBFS. When an interrupt generation condition is satisfied and the interrupt output is enabled using the associated interrupt enable register, a USBFS interrupt request is issued to the Interrupt Controller Unit (ICU) and an USBFS interrupt is generated.

Table 32.14 Interrupt sources (1 of 3)

Bit to be set to 1	Name	Interrupt source	Applicable controller function	Status flag
VBINT	VBUS interrupt	• A change in the state of the USB_VBUS input pin was detected (low to high or high to low)	Host or device*1	INTSTS0.VBSTS

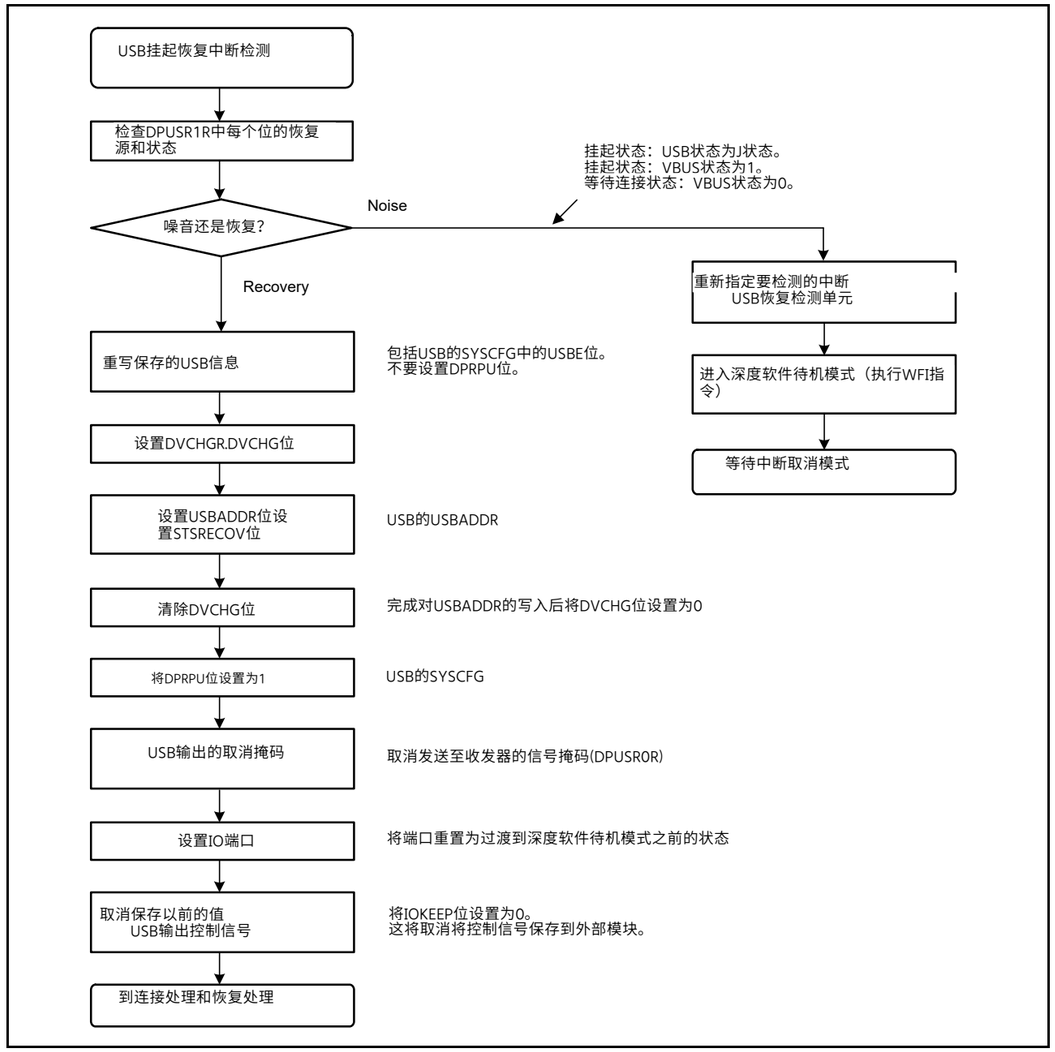


Figure 32.9 用于取消作为设备控制器的深度软件待机模式的USBFS设置流程

32.3.2 Interrupts

表32.14列出了USBFS中的中断源。当满足中断生成条件并使用相关的中断使能寄存器启用中断输出时，将向中断控制器单元(ICU)发出USBFS中断请求并生成USBFS中断。

Table 32.14 中断源(1of3)

要设置为1的位	Name	中断源	适用控制器功能	状态标志
VBINT	VBUS interrupt	检测到USB_VBUS输入引脚的状态变化（从低到高或从高到低）	主机或设备*1	INTSTS0.VBSTS

Table 32.14 Interrupt sources (2 of 3)

Bit to be set to 1	Name	Interrupt source	Applicable controller function	Status flag
RESM	Resume interrupt	• A change in the state of the USB bus was detected in the Suspend state (J-state to K-state or J-state to SE0)	Device	—
SOFR	Frame number update interrupt	In host controller mode: • An SOF packet with a different frame number was transmitted In device controller mode: • An SOF packet with a different frame number was received	Host or device	—
DVST	Device state transition interrupt	• One of the following device state transitions was detected: - USB bus reset was detected - Suspend state was detected - SET_ADDRESS request was received - SET_CONFIGURATION request was received	Device	INTSTS0.DVSQ[2:0]
CTRT	Control transfer stage transition interrupt	• A control transfer stage transition was detected because of one of the following: - Setup stage completed - Control write transfer status stage transition occurred - Control read transfer status stage transition occurred - Control transfer completed - Control transfer sequence error occurred.	Device	INTSTS0.CTSQ[2:0]
BEMP	Buffer empty interrupt	• The buffer is empty after all FIFO buffer data was transmitted • A packet larger than the maximum packet size was received	Host or device	BEMPSTS.PIPEnBEMP
NRDY	Buffer not ready interrupt	In host controller mode: • A STALL response was received from the peripheral device in response to the issued token • The response from the peripheral device in response to the issued token was not received successfully (no response three times consecutively or packet reception error three times consecutively) • An overrun or underrun error occurred during isochronous transfer In device controller mode: • NAK was returned for an IN or OUT token while the PID[1:0] bits were set to 01b (BUF) • A CRC error or bit stuffing error occurred during data reception in isochronous transfer • An overrun or underrun occurred during data reception in isochronous transfer	Host or device	NRDYSTS.PIPEnNRDY
BRDY	Buffer ready interrupt	• The buffer is ready (readable or writable state)	Host or device	BRDYSTS.PIPEnBRDY
OVRCR	Overcurrent input change interrupt	• USB_OVRCURA or USB_OVRCURB input pin state change was detected (low to high or high to low)	Host	INTSTS1.OVRCR
BCHG	Bus change interrupt	• USB bus state change was detected	Host or device	SYSSTS0.LNST[1:0]
DTCH	Disconnect detection during full-speed operation	• Peripheral device disconnect was detected in full-speed operation	Host	DVSTCTR0.RHST[2:0]
ATTCH	Device connect detection interrupt	• J-state or K-state was detected on the USB bus for 2.5 µs continuously This interrupt can be used to check whether peripheral devices are connected.	Host	—
EOFERR	EOF error detection interrupt	• An EOF error was detected for a peripheral device	Host	—

Table 32.14 中断源（2个，共3个）

要设置为1的位	Name	中断源	适用控制器功能	状态标志
RESM	恢复中断	在Suspend状态下检测到USB总线状态的变化（J状态到K状态或J状态到SE0）	Device	—
SOFR	帧号更新中断	在主机控制器模式下： 发送了具有不同帧号的SOF数据包在设备控制器模式下： 接收到了具有不同帧号的SOF数据包	主机或设备	—
DVST	设备状态转换中断	检测到以下设备状态转换之一：检测到USB总线复位检测到挂起状态收到SET_ADDRESS请求收到SET_CONFIGURATION请求	Device	INTSTS0.DVSQ[2:0]
CTRT	控制转移阶段转换中断	由于以下原因之一检测到控制传输阶段转换：设置阶段完成发生控制写入传输状态阶段转换发生控制读取传输状态阶段转换控制传输完成发生控制传输序列错误。	Device	INTSTS0.CTSQ[2:0]
BEMP	缓冲区空中断	发送完所有FIFO缓冲区数据后，缓冲区为空 接收到的数据包大于最大数据包大小	主机或设备	BEMPSTS.PIPEnBEMP
NRDY	缓冲区未就绪中断	在主机控制器模式下： 从外围设备接收到响应发出的令牌的STALL响应 未成功收到外围设备对发出的令牌的响应（连续3次无响应或3次数据包接收错误 同步传输期间发生溢出或欠载错误在设备控制器模式下： 当PID[1:0]位设置为01b(BUF)时，为IN或OUT令牌返回NAK CRC错误或位填充同步传输中的数据接收过程中发生错误 同步传输中的数据接收过程中发生溢出或欠载	主机或设备	NRDYSTS.PIPEnNRDY
BRDY	缓冲区就绪中断	缓冲区准备就绪（可读或可写状态）	主机或设备	BRDYSTS.PIPEnBRDY
OVRCR	过流输入变化中断	检测到USB_OVRCURA或USB_OVRCURB输入引脚状态变化（从低到高或从高到低）	Host	INTSTS1.OVRCR
BCHG	总线变化中断	检测到USB总线状态更改	主机或设备	SYSSTS0.LNST[1:0]
DTCH	全速运行时断线检测	在全速运行中检测到外围设备断开连接	Host	DVSTCTR0.RHST[2:0]
ATTCH	设备连接检测中断	连续2.5µs在USB总线上检测到J状态或K状态此中断可用于检查外围设备是否已连接。	Host	—
EOFERR	EOF错误检测中断	检测到外围设备的EOF错误	Host	—

Table 32.14 Interrupt sources (3 of 3)

Bit to be set to 1	Name	Interrupt source	Applicable controller function	Status flag
SACK	Setup normal interrupt	• A setup transaction normal response (ACK) was received	Host	—
SIGN	Setup error interrupt	• A setup transaction error (no response or ACK packet corruption) was detected three consecutive times	Host	—

Note 1. Although this interrupt can be generated in host controller mode, it is not usually used in this mode.

Figure 32.10 shows the circuits related to the USBFS interrupts.

Table 32.14 中断源（3个中的3个）

要设置为1的位	Name	中断源	适用控制器功能	状态标志
SACK	设置正常中断	收到设置事务正常响应(ACK)	Host	—
SIGN	设置错误中断	连续3次检测到设置事务错误（无响应或ACK数据包损坏）	Host	—

Note 1. 虽然在主机控制器模式下可以产生此中断，但通常不会在此模式下使用。

图32.10显示了与USBFS中断相关的电路。

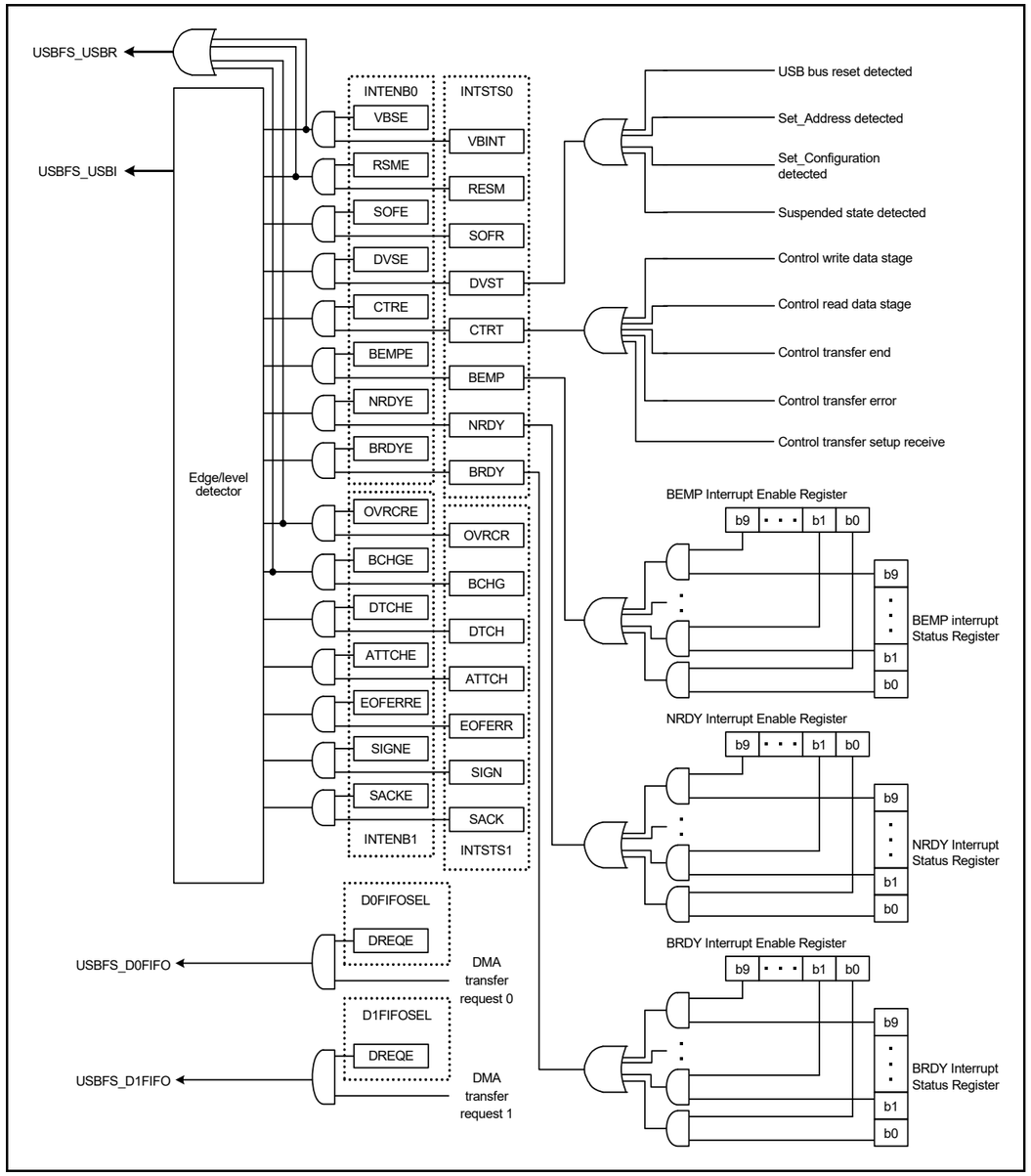


Figure 32.10 USBFS interrupt-related circuits

Table 32.15 shows the interrupts generated by the USBFS.

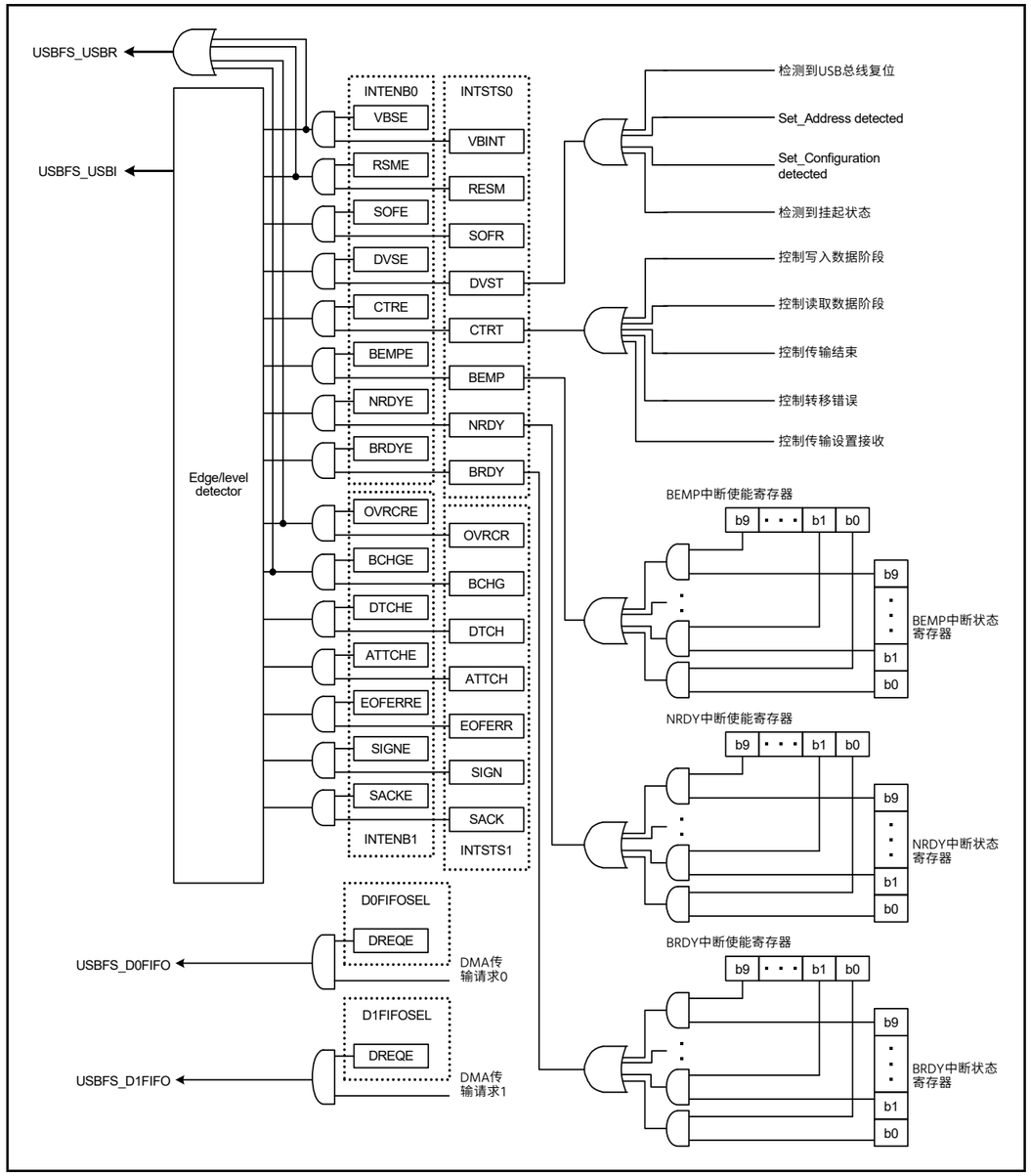


Figure 32.10 USBFS interrupt-related circuits

表32.15显示了USBFS产生的中断。

Table 32.15 USBFS interrupts

Interrupt name	Interrupt status flag	DTC activation	DMAC activation	Priority
USBFS_D0FIFO	DMA transfer request 0	Possible	Possible	High
USBFS_D1FIFO	DMA transfer request 1	Possible	Possible	
USBFS_USBI	VBUS interrupt, resume interrupt, frame number update interrupt, device state transition interrupt, control transfer stage transition interrupt, buffer empty interrupt, buffer not ready interrupt, buffer ready interrupt, overcurrent input change interrupt, bus change interrupt, disconnect detection interrupt during full-speed operation, device connect detection interrupt, EOF error detection interrupt, normal setup operation interrupt, and setup error interrupt	Not possible	Not possible	
USBFS_USBR	VBUS interrupt, resume interrupt, overcurrent input change interrupt, and bus change interrupt	Not possible	Not possible	—

Low

32.3.3 Interrupt Descriptions

32.3.3.1 BRDY interrupt

The BRDY interrupt is generated in both host and device controller modes. This section describes the conditions in which the USBFS sets the associated bit in BRDYSTS to 1. Under these conditions, the USBFS generates a BRDY interrupt if the software has set the bit in BRDYENB associated with the given pipe to 1 and the INTENB0.BRDYE bit to 1.

The conditions for generating and clearing the BRDY interrupt depend on the SOFCFG.BRDYM and PIPECFG.BFRE settings for each pipe as follows:

(1) When SOFCFG.BRDYM = 0 and PIPECFG.BFRE = 0

With these settings, the BRDY interrupt indicates that the FIFO port is accessible.

On any of the following conditions, the USBFS generates an internal BRDY interrupt request trigger and sets the BRDYSTS.PIPEnBRDY bit associated with the selected pipe to 1.

(a) For transmitting pipes

- When the DIR bit is changed from 0 to 1 by software
- When packet transmission is complete for a pipe while write-access from the CPU to the FIFO buffer for the pipe is disabled (when the BSTS bit is read as 0)
- When one FIFO buffer is empty on completion of writing data to the other FIFO buffer in double buffer mode
- No request trigger is generated until completion of writing data to the currently-written FIFO buffer even if transmission to the other FIFO buffer is complete
- When the hardware flushes the buffer of the pipe for isochronous transfers
- When 1 is written to the PIPEnCTR.ACLRM bit, which causes the FIFO buffer to transition from the write-disabled to write-enabled state.

No request trigger is generated for the DCP, that is, during data transmission for control transfers.

(b) For receiving pipes

- When packet reception is successfully complete, enabling the FIFO buffer to be read while read-access from the CPU to the FIFO buffer for the given pipe is disabled (when the BSTS bit is read as 0). No request trigger is generated for transactions in which a DATA-PID mismatch has occurred.
- When one FIFO buffer is read-enabled on completion of reading data from the other FIFO buffer in double buffer mode. No request trigger is generated until completion of reading data from the currently-read FIFO buffer, even if reception by the other FIFO buffer is complete.

In device controller mode, the BRDY interrupt is not generated in the status stage of control transfers. The PIPEnBRDY

Table 32.15 USBFS interrupts

中断名称	中断状态标志	DTC activation	DMAC activation	Priority
USBFS_D0FIFO	DMA传输请求0	Possible	Possible	High
USBFS_D1FIFO	DMA传输请求1	Possible	Possible	
USBFS_USBI	VBUS中断、恢复中断、帧号更新中断、设备状态转换中断、控制传输阶段转换中断、缓冲区空中断、缓冲区未就绪中断、缓冲区就绪中断、过流输入改变中断、总线改变中断、满时断开检测中断速度操作、设备连接检测中断、EOF错误检测中断、正常设置操作中断和设置错误中断	不可能	不可能	
USBFS_USBR	VBUS中断、恢复中断、过流输入变化中断、总线变化中断	不可能	不可能	—

Low

32.3.3 中断说明

32.3.3.1 BRDY interrupt

在主机和设备控制器模式下都会产生BRDY中断。本节介绍USBFS将BRDYSTS中的相关位设置为1的条件。在这些条件下，如果软件将BRDYENB中与给定管道相关的位设置为1并且INTENB0.BRDYE位，USBFS将生成BRDY中断为1。

产生和清除BRDY中断的条件取决于每个管道的SOFCFG.BRDYM和PIPECFG.BFRE设置，如下所示：

(1) 当SOFCFG.BRDYM=0且PIPECFG.BFRE=0时

通过这些设置，BRDY中断指示FIFO端口可访问。

在以下任何一种情况下，USBFS都会产生一个内部BRDY中断请求触发器并设置BRDYSTS.PIPEnBRDY位与所选管道相关联为1。

(a) 用于传输管道

- 当DIR位由软件从0变为1时
- 当管道的数据包传输完成而从CPU到管道的FIFO缓冲区的写访问被禁用时（当BSTS位被读取为0时）
- 双缓冲模式下，当一个FIFO缓冲区在完成向另一个FIFO缓冲区写入数据时为空时
- 直到完成向当前写入的FIFO缓冲区写入数据之前，不会生成请求触发，即使传输到另一个FIFO缓冲区已完成
- 当硬件刷新管道缓冲区以进行同步传输时
- 当1写入PIPEnCTR.ACLRM位时，这会导致FIFO缓冲区从写禁止状态转换为写使能状态。

没有为DCP生成请求触发，即在控制传输的数据传输期间。

(b) 用于接收管道

- 当数据包接收成功完成后，在从CPU到给定管道的FIFO缓冲区被禁用（当BSTS位被读取为0时）。对于发生DATA-PID不匹配的事务，不会生成请求触发器。
- 当一个FIFO缓冲区在双缓冲区模式下完成从另一个FIFO缓冲区读取数据后启用读取。在从当前读取的FIFO缓冲区读取数据完成之前，不会生成请求触发，即使其他FIFO缓冲区的接收已完成。

在设备控制器模式下，在控制传输的状态阶段不会产生BRDY中断。PIPEnBRDY

interrupt status of the selected pipe can be set to 0 by writing 0 to the associated PIPEnBRDY bit through software. In this case, the other PIPEnBRDY bit should be set to 1.

Clear the BRDY status before accessing the FIFO buffer.

(2) When SOFCFG.BRDYM = 0 and PIPECFG.BFRE = 1

With these settings, the USBFS generates a BRDY interrupt on completion of reading all data for a single transfer using the receiving pipe, and sets the bit in BRDYSTS associated with the pipe to 1.

On any of the following conditions, the USBFS determines that the last data for a single transfer was received.

- When a short packet including a zero-length packet is received
- When the PIPEn transaction counter register (PIPEnTRN) is used and the number of packets specified in the PIPEnTRN.TRNCNT[15:0] bits are completely received.

When the data is completely read after any of these conditions is satisfied, the USBFS determines that all data for a single transfer is completely read.

When a zero-length packet is received while the FIFO buffer is empty, the USBFS determines that all data for a single transfer is completely read when the FRDY bit in the FIFO port control register is 1 and the DTLN[8:0] bits are 0. In this case, to start the next transfer, write 1 to the BCLR bit in the associated port control register through the software. With these settings, the USBFS does not detect a BRDY interrupt for the transmitting pipe.

The PIPEnBRDY interrupt status of a pipe can be set to 0 by writing 0 to the associated BRDYSTS.PIPEnBRDY bit through the software. In this case, 1s must be written to the PIPEnBRDY bits for the other pipes.

In this mode, do not change the PIPECFG.BFRE bit setting until all data for a single transfer is processed. When it is necessary to change the PIPECFG.BFRE bit before completion of processing, all FIFO buffers for the pipe must be cleared using the PIPEnCTR.ACLRM bit.

(3) When SOFCFG.BRDYM = 1 and PIPECFG.BFRE = 0

With these settings, the BRDYSTS.PIPEnBRDY values are linked to the BSTS bit setting for each pipe. In other words, the BRDY interrupt status bits (PIPEnBRDY) are set to 1 or 0 by the USB depending on the FIFO buffer status.

(a) For transmitting pipes

The BRDY interrupt status bits are set to 1 when the FIFO buffer is ready for write access, and are set to 0 when it is not ready. The BRDY interrupt is not generated for the DCP in the transmitting direction even when it is ready for write access.

(b) For receiving pipes

The BRDY interrupt status bits set to 1 when the FIFO buffer is ready for read access, and set to 0 when all data is read (not ready for read access).

When a zero-length packet is received while the FIFO buffer is empty, the associated bit is set to 1 and the BRDY interrupt is continuously generated until the software writes 1 to BCLR. With this setting, the PIPEnBRDY bit cannot be set to 0 by software.

When the SOFCFG.BRDYM bit is set to 1, set the PIPECFG.BFRE bit for all pipes to 0.

Figure 32.11 shows the timing of BRDY interrupt generation.

通过软件将0写入相关的PIPEnBRDY位，可以将所选管道的中断状态设置为0。在这种情况下，其他PIPEnBRDY位应设置为1。

在访问FIFO缓冲区之前清除BRDY状态。

(2) 当SOFCFG.BRDYM=0且PIPECFG.BFRE=1时

使用这些设置，USBFS在完成使用接收管道读取单次传输的所有数据时生成BRDY中断，并将BRDYSTS中与管道关联的位设置为1。

在以下任何一种情况下，USBFS都会确定已接收到单次传输的最后一个数据。

- 当接收到包含零长度数据包的短数据包时
- 当使用PIPEn事务计数器寄存器(PIPEnTRN)并且在PIPEnTRN.TRNCNT[15:0]位被完全接收。

当满足其中任何一个条件后数据被完全读取时，USBFS确定单次传输的所有数据都被完全读取。

当FIFO缓冲区为空时接收到零长度数据包时，当FIFO端口控制寄存器中的FRDY位为1且DTLN[8:0]位为0.在这种情况下，要开始下一次传输，通过软件向相关端口控制寄存器中的BCLR位写入1。使用这些设置，USBFS不会检测到传输管道的BRDY中断。

通过软件将0写入相关的BRDYSTS.PIPEnBRDY位，可以将管道的PIPEnBRDY中断状态设置为0。在这种情况下，必须将1写入其他管道的PIPEnBRDY位。

在此模式下，在处理完单次传输的所有数据之前，不要更改PIPECFG.BFRE位设置。当需要在处理完成之前更改PIPECFG.BFRE位时，必须使用PIPEnCTR.ACLRM位清除管道的所有FIFO缓冲区。

(3) 当SOFCFG.BRDYM=1且PIPECFG.BFRE=0时

通过这些设置，BRDYSTS.PIPEnBRDY值链接到每个管道的BSTS位设置。换言之，BRDY中断状态位(PIPEnBRDY)由USB设置为1或0，具体取决于FIFO缓冲区状态。

(a) 用于传输管道

当FIFO缓冲区准备好进行写访问时，BRDY中断状态位设置为1，当它未准备好时设置为0。发送方向上的DCP不会产生BRDY中断，即使它已准备好进行写访问。

(b) 用于接收管道

当FIFO缓冲区准备好进行读取访问时，BRDY中断状态位设置为1，并在读取所有数据（未准备好进行读取访问）时设置为0。

当FIFO缓冲区为空时接收到零长度数据包时，相关位设置为1，并且持续产生BRDY中断，直到软件将1写入BCLR。使用此设置，PIPEnBRDY位不能通过软件设置为0。

当SOFCFG.BRDYM位设置为1时，将所有管道的PIPECFG.BFRE位设置为0。

图32.11显示了BRDY中断产生的时序。

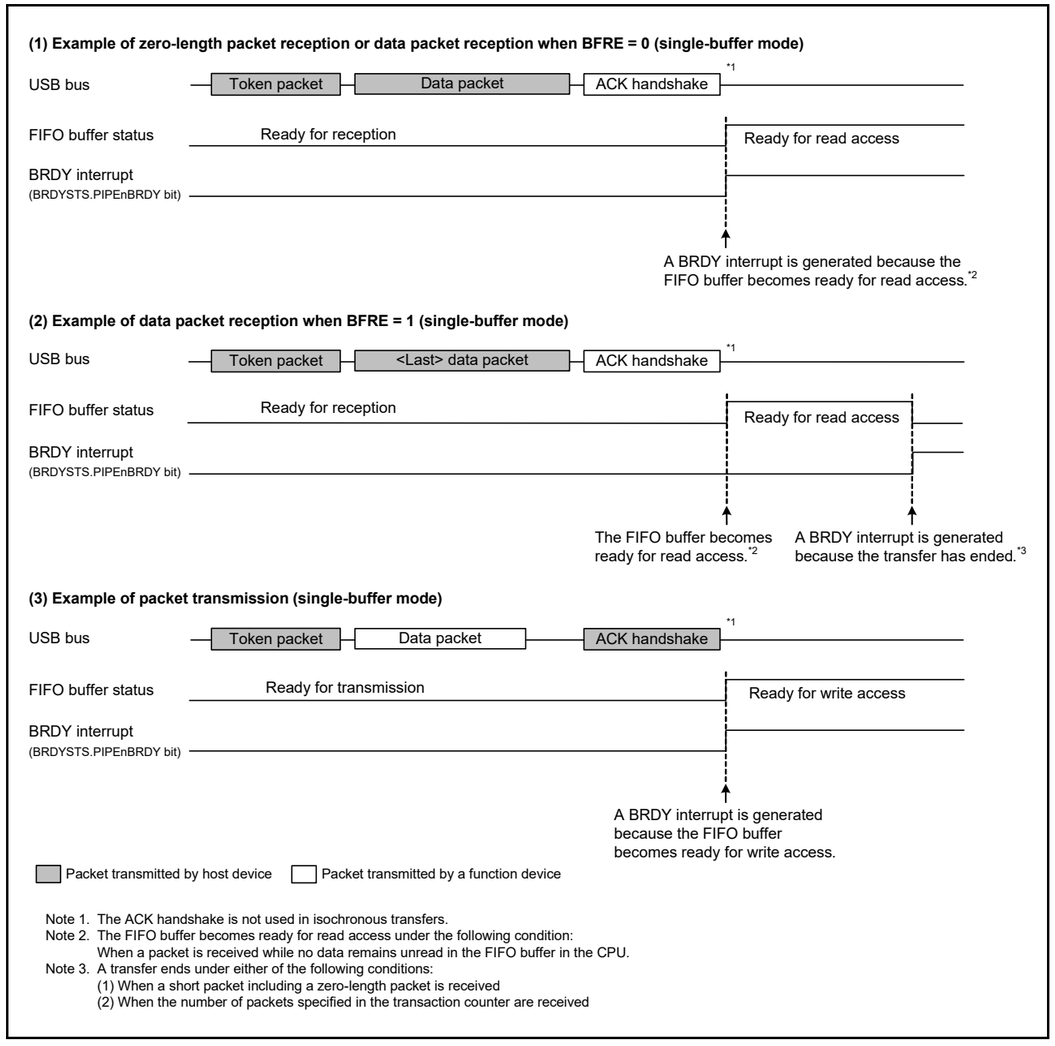


Figure 32.11 Timing of BRDY interrupt generation

The condition for clearing the INTSTS0.BRDY bit depends on the SOFCFG.BRDYM bit setting, as shown in Table 32.16.

Table 32.16 Conditions for clearing the BRDY bit

BRDYM bit	Condition for clearing BRDY bit
0	When all bits in BRDYSTS are set to 0 by software.
1	PIPEnBRDY when the BSTS bits for all pipes have cleared to 0.

32.3.3.2 NRDY interrupt

On generating an internal NRDY interrupt request for the pipe whose PID bits are set to BUF by software, the USBFS sets the associated PIPEnNRDY bit in NRDYSTS to 1. If the associated bit in NRDYENB is set to 1 by software, the USBFS sets the INTSTS0.NRDY bit to 1 and generates a USBFS interrupt.

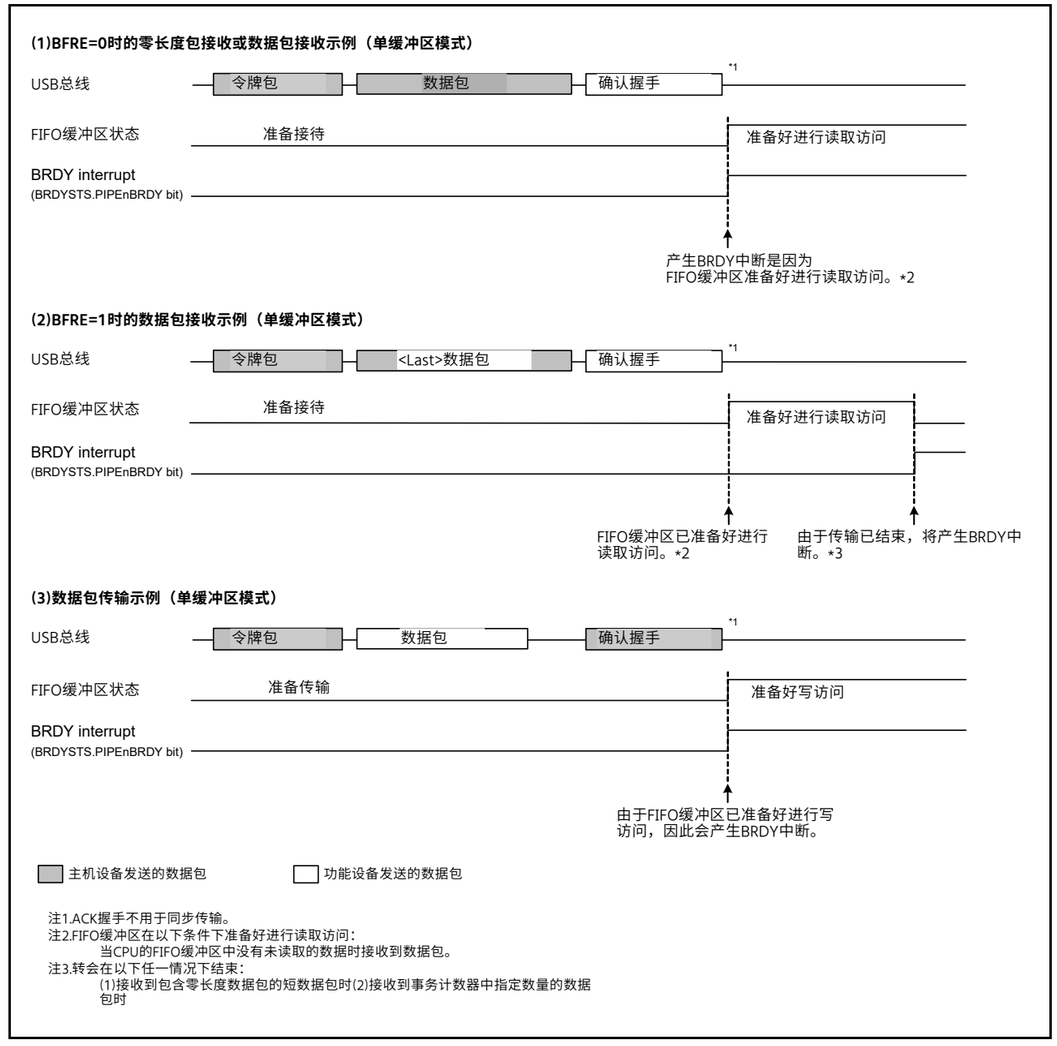


Figure 32.11 BRDY中断产生的时序

清除INTSTS0.BRDY位的条件取决于SOFCFG.BRDYM位设置，如表32.16所示。

Table 32.16 清除BRDY位的条件

BRDYM bit	清除BRDY位的条件
0	当BRDYSTS中的所有位由软件设置为0时。
1	当所有管道的BSTS位都被清除为0时，PIPEnBRDY。

32.3.3.2 NRDY interrupt

在为PID位由软件设置为BUF的管道生成内部NRDY中断请求时，USBFS将NRDYSTS中的相关PIPEnNRDY位设置为1。如果NRDYENB中的相关位由软件设置为1，则USBFS设置INTSTS0.NRDY位为1并产生USBFS中断。

This section describes the conditions in which the USBFS generates the internal NRDY interrupt request for a given pipe.

The internal NRDY interrupt request is not generated during setup transaction execution in host controller mode. During setup transactions in host controller mode, the SACK or SIGN interrupt is detected.

The internal NRDY interrupt request is not generated during status stage execution of the control transfer in device controller mode.

(1) In host controller mode

(a) For transmitting pipes

On any of the following conditions, the USBFS detects an NRDY interrupt:

- For isochronous transfer pipes, when the time to issue an OUT token comes while there is no data to be transmitted in the FIFO buffer. In this case, the USBFS transmits a zero-length packet following the OUT token and sets the associated NRDYSTS.PIPEnNRDY bit and the FRMNUM.OVRN bit to 1.
- During communications other than setup transactions on pipes not used for isochronous transfers, when any combination of the following two cases occur three consecutive times:
  - No response is returned from the peripheral device (when timeout is detected before detection of the handshake packet from the peripheral device
  - An error is detected in the packet from the peripheral device. In this case, the USBFS sets the associated PIPEnNRDY bit to 1 and changes the associated PID[1:0] setting for the pipe to NAK.
- During communications other than setup transactions, when the STALL handshake is received from the peripheral device. In this case, the USBFS sets the associated PIPEnNRDY bit to 1 and changes the PID[1:0] setting for the associated pipe to STALL (11b).

(b) For receiving pipes

- For isochronous transfer pipes, when the time to issue an IN token comes but there is no space available in the FIFO buffer. In this case, the USBFS discards the received data for the IN token and sets the PIPEnNRDY bit associated with the pipe and the OVRN bit to 1. When a packet error is detected in the received data for the IN token, the USBFS also sets the FRMNUM.CRCE bit to 1.
- For non-isochronous transfer pipes, when any combination of the following two cases occur three consecutive times:
  - No response is returned from the peripheral device for the IN token issued by the USBFS (when timeout is detected before detection of the DATA packet from the peripheral device)
  - An error is detected in the packet from the peripheral device. In this case, the USBFS sets the associated PIPEnNRDY bit to 1 and changes the associated PID[1:0] setting for the pipe to NAK.
- For isochronous transfer pipes, when no response is returned from the peripheral device for the IN token (when timeout is detected before detection of the DATA packet from the peripheral device) or an error is detected in the packet from the peripheral device. In this case, the USBFS sets the PIPEnNRDY bit associated with the pipe to 1. The PID[1:0] setting for the pipe is not changed.
- For isochronous transfer pipes, when a CRC error or a bit stuffing error is detected in the received data packet. In this case, the USBFS sets the PIPEnNRDY bit associated with the pipe and the CRCE bit to 1.
- When the STALL handshake is received. In this case, the USBFS sets the PIPEnNRDY bit associated with the pipe to 1 and changes the PID[1:0] setting for the associated pipe to STALL.

(2) In device controller mode

(a) For transmitting pipes

- When an IN token is received while there is no data to be transmitted in the FIFO buffer. In this case, the USBFS generates a NRDY interrupt request on reception of the IN token and sets the NRDYSTS.PIPEnNRDY bit to 1. For an isochronous transfer pipe in which an interrupt is generated, the USBFS transmits a zero-length packet and sets the FRMNUM.OVRN bit to 1.

本节描述USBFS为给定管道生成内部NRDY中断请求的条件。

内部NRDY中断请求在主控制器模式下的设置事务执行期间不会产生。在主机控制器模式下的设置事务期间，检测到SACK或SIGN中断。

在设备控制器模式下控制传输的状态阶段执行期间，不会产生内部NRDY中断请求。

(1) 在主机控制器模式下

(a) 用于传输管道

在以下任何一种情况下，USBFS都会检测到NRDY中断：

- 对于同步传输管道，当发出OUT令牌的时间到来时，FIFO缓冲区中没有要传输的数据。在这种情况下，USBFS在OUT令牌之后发送一个长度为零的数据包，并将相关的NRDYSTS.PIPEnNRDY位和FRMNUM.OVRN位设置为1。
- 在不用于同步传输的管道上的设置事务以外的通信期间，当以下两种情况的任意组合连续发生3次时：
  - 外围设备没有返回响应（当在检测到来自外围设备的握手包之前检测到超时时
  - 在来自外围设备的数据包中检测到错误。在这种情况下，USBFS设置关联的PIPEnNRDY位为1并将管道的相关PID[1:0]设置更改为NAK。
- 在设置事务以外的通信期间，当从外围设备接收到STALL握手时。在这种情况下，USBFS将相关的PIPEnNRDY位设置为1，并将相关管道的PID[1:0]设置更改为STALL(11b)。

(b) 用于接收管道

- 对于同步传输管道，当发出IN令牌的时间到来但FIFO缓冲区中没有可用空间时。在这种情况下，USBFS丢弃接收到的IN令牌数据，并将与管道关联的PIPEnNRDY位和OVRN位设置为1。当在接收到的IN令牌数据中检测到数据包错误时，USBFS也会设置FRMNUM.CRCE位为1。
- 对于非等时传输管道，当下列两种情况的任意组合连续出现3次时：
  - USBFS发出的IN令牌没有从外围设备返回响应（当在检测到来自外围设备的DATA包之前检测到超时时）
  - 在来自外围设备的数据包中检测到错误。在这种情况下，USBFS设置关联的PIPEnNRDY位为1并将管道的相关PID[1:0]设置更改为NAK。
- 对于同步传输管道，当外围设备没有返回对IN令牌的响应时（在检测到来自外围设备的DATA数据包之前检测到超时）或在来自外围设备的数据包中检测到错误。在这种情况下，USBFS将与管道关联的PIPEnNRDY位设置为1。管道的PID[1:0]设置不会更改。
- 对于同步传输管道，当在接收到的数据包中检测到CRC错误或位填充错误时。在这种情况下，USBFS将与管道关联的PIPEnNRDY位和CRCE位设置为1。
- 当收到STALL握手时。在这种情况下，USBFS将与管道关联的PIPEnNRDY位设置为1，并将关联管道的PID[1:0]设置更改为STALL。

(2) 在设备控制器模式下

(a) 用于传输管道

- 当FIFO缓冲区中没有要传输的数据时接收到IN令牌。在这种情况下，USBFS在接收到IN令牌时产生一个NRDY中断请求，并将NRDYSTS.PIPEnNRDY位设置为1。对于产生中断的同步传输管道，USBFS发送一个长度为零的数据包并将FRMNUM.OVRN位为1。

(b) For receiving pipes

- When an OUT token is received but there is no space available in the FIFO buffer. For an isochronous transfer pipe in which an interrupt is generated, the USBFS generates a NRDY interrupt request on reception of the OUT token and sets the PIPEnNRDY bit to 1 and OVRN bit to 1. For a non-isochronous transfer pipe in which an interrupt is generated, the USBFS generates a NRDY interrupt request when a NAK handshake is transferred after the data following the OUT token is received, and sets the PIPEnNRDY bit to 1. The NRDY interrupt request is not generated during retransmission because of a DATA-PID mismatch. In addition, the NRDY interrupt request is not generated if an error occurs in the DATA packet.
- For isochronous transfer pipes, when a token is not received successfully within an interval frame. In this case, the USBFS generates an NRDY interrupt request when the SOF is received, and sets the PIPEnNRDY bit to 1.

Figure 32.12 shows the timing of NRDY interrupt generation in device controller mode.

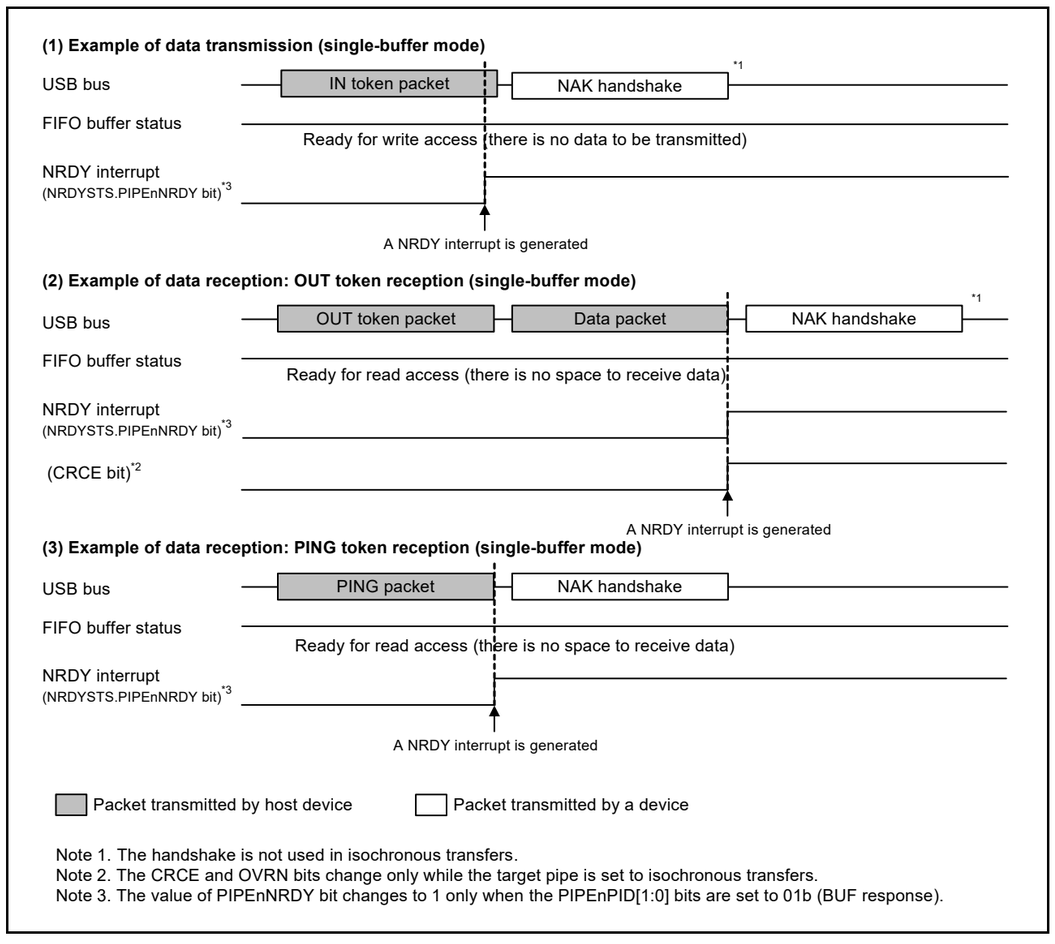


Figure 32.12 Timing of NRDY interrupt generation in device controller mode

32.3.3.3 BEMP interrupt

On detecting a BEMP interrupt for the pipe whose PID bits are set to BUF by software, the USBFS sets the associated BEMPSTS.PIPEnBEMP bit to 1. If the associated bit in BEMPENB is set to 1 by software, the USBFS sets the INTSTS0.BEMP bit to 1 and generates a USBFS interrupt. This section describes the conditions in which the USBFS generates an internal BEMP interrupt request.

(b) 用于接收管道

- 当接收到OUT令牌但FIFO缓冲区中没有可用空间时。对于产生中断的同步传输管道，USBFS在接收到OUT令牌时产生一个NRDY中断请求，并将PIPEnNRDY位设置为1，并将OVRN位设置为1。USBFS在接收到OUT令牌之后的数据后，在传输NAK握手时产生NRDY中断请求，并将PIPEnNRDY位设置为1。由于DATA-PID不匹配，重传期间不会产生NRDY中断请求。此外，如果DATA包发生错误，则不会产生NRDY中断请求。
- 对于同步传输管道，当在间隔帧内未成功接收到令牌时。在这种情况下，USBFS在接收到SOF时产生一个NRDY中断请求，并将PIPEnNRDY位设置为1。

图32.12显示了设备控制器模式下NRDY中断产生的时序。

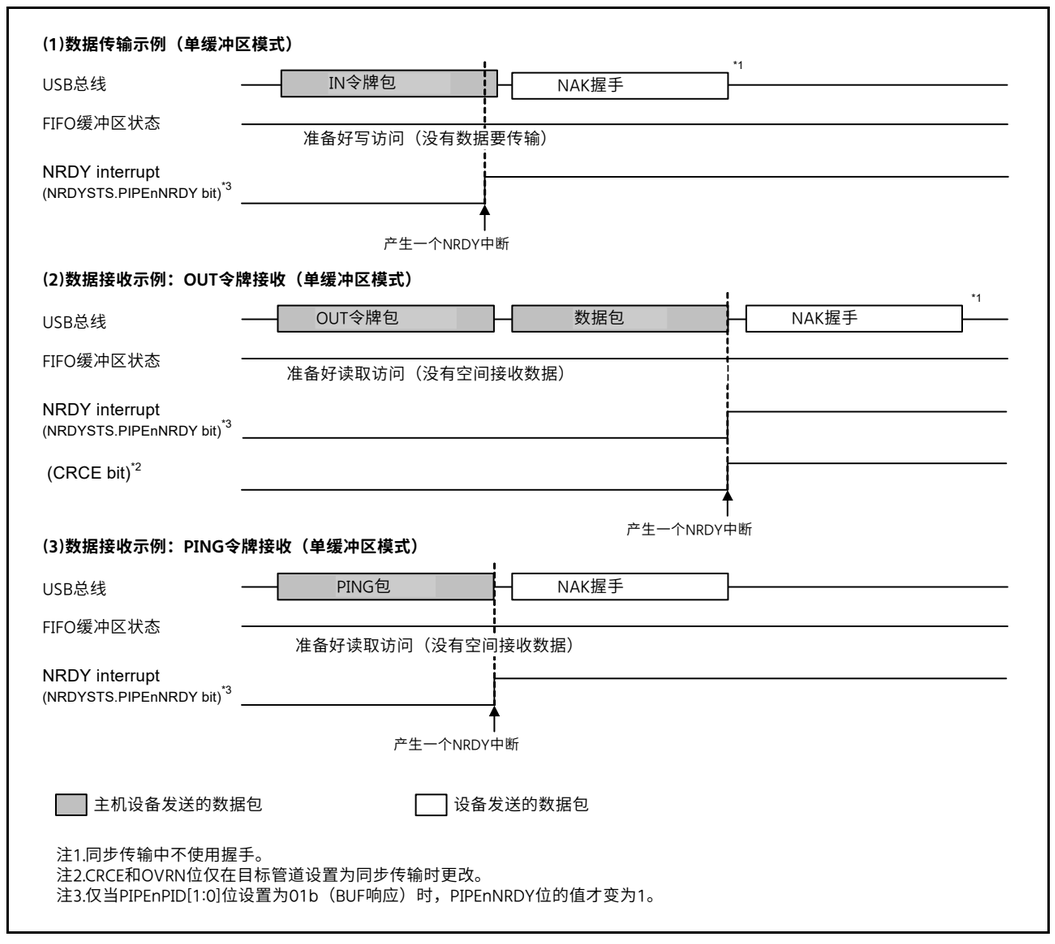


Figure 32.12 设备控制器模式下NRDY中断产生的时序

32.3.3.3 BEMP interrupt

在检测到PID位被软件设置为BUF的管道的BEMP中断时，USBFS将相关的BEMPSTS.PIPEnBEMP位设置为1。如果BEMPENB中的相关位被软件设置为1，USBFS将设置
INTSTS0.BEMP位为1并产生USBFS中断。本节介绍USBFS产生内部BEMP中断请求的条件。

(1) For transmitting pipes

When the FIFO buffer of the associated pipe is empty on completion of transmission, including zero-length packet transmission, and in single buffer mode, an internal BEMP interrupt request is generated simultaneously with the BRDY interrupt for a non-DCP pipe. The internal BEMP interrupt request is not generated in any of the following conditions:

- When the CPU or DMA/DTC has already started writing data to the FIFO buffer of the CPU on completion of transmitting data from one FIFO buffer in double buffer mode
- When the buffer is cleared (emptied) by setting the PIPEnCTR.ACLRM or the BCLR bit to 1 in the port control register
- When an IN transfer (zero-length packet transmission) is performed during the control transfer status stage in device controller mode.

(2) For receiving pipes

When a successfully-received data packet size exceeds the specified maximum packet size. In this case, the USBFS generates a BEMP interrupt request, sets the associated BEMPSTS.PIPEnBEMP bit to 1, discards the received data, and changes the associated PID[1:0] setting for the pipe to STALL (11b). The USBFS returns no response in host controller mode, and returns STALL response in device controller mode.

The internal BEMP interrupt request is not generated in any of the following conditions:

- When a CRC error or a bit stuffing error is detected in the received data
- When a setup transaction is being performed:
  - Writing 0 to the BEMPSTS.PIPEnBEMP bit clears the status
  - Writing 1 to the BEMPSTS.PIPEnBEMP bit has no effect.

Figure 32.13 shows the timing of BEMP interrupt generation in device controller mode.

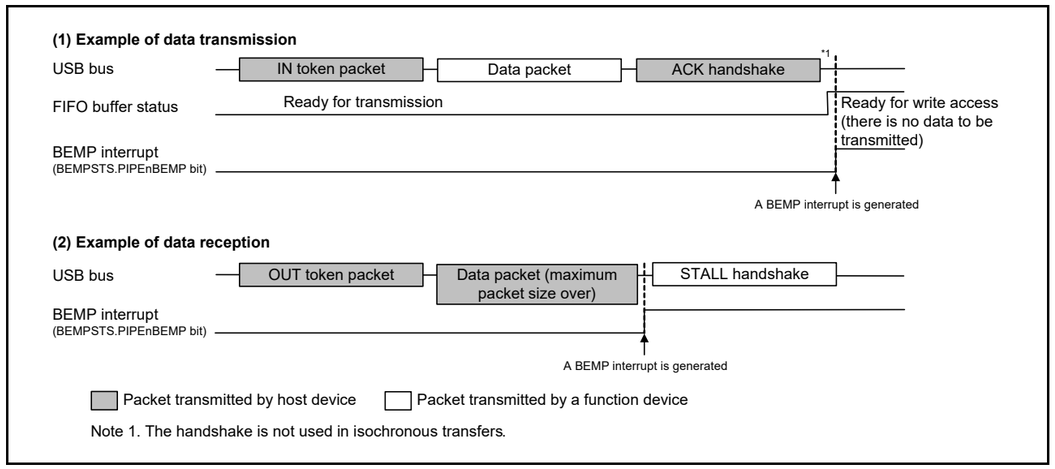


Figure 32.13 Timing of BEMP interrupt generation in device controller mode

32.3.3.4 Device state transition interrupt (device controller mode)

Figure 32.14 shows a diagram of the USBFS device state transitions. The USBFS controls device states and generates device state transition interrupts. However, recovery from the Suspend state (resume signal detection) is detected by means of the resume interrupt. Device state transition interrupts can be enabled or disabled independently in INTENB0. Devices whose states have changed can be checked in the INTSTS0.DVSQ[2:0] bits.

When a transition is made to the default state, a device state transition interrupt is generated after a USB bus reset is detected.

The USBFS controls device states, and device state transition interrupts can be generated, only in device controller

(1) 用于传输管道

当相关管道的FIFO缓冲区在传输完成时为空时，包括零长度数据包传输，并且在单缓冲区模式下，内部BEMP中断请求与非DCP管道的BRDY中断同时生成。在以下任何一种情况下都不会产生内部BEMP中断请求：

- 当CPU或DMADTC在双缓冲模式下从一个FIFO缓冲区完成数据传输后已经开始向CPU的FIFO缓冲区写入数据时
- 当通过将端口控制寄存器中的PIPEnCTR.ACLRM或BCLR位设置为1来清除（清空）缓冲区时
- 在设备控制器模式下的控制传输状态阶段执行IN传输（零长度数据包传输）时。

(2) 用于接收管道

当成功接收的数据包大小超过指定的最大包大小时。在这种情况下，USBFS生成一个BEMP中断请求，将相关的BEMPSTS.PIPEnBEMP位设置为1，丢弃接收到的数据，并将管道的相关PID[1:0]设置更改为STALL(11b)。USBFS在主机控制器模式下不返回响应，在设备控制器模式下返回STALL响应。

在以下任何一种情况下都不会产生内部BEMP中断请求：

- 在接收到的数据中检测到CRC错误或位填充错误时
- 执行设置事务时：
  - 将0写入BEMPSTS.PIPEnBEMP位可清除状态
  - 向BEMPSTS.PIPEnBEMP位写入1无效。

图32.13显示了设备控制器模式下BEMP中断产生的时序。

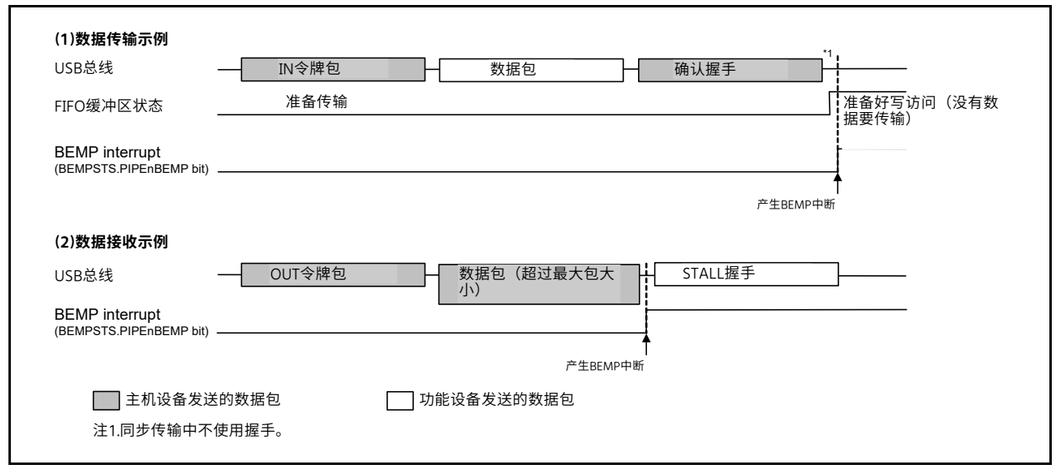


Figure 32.13 设备控制器模式下BEMP中断产生的时序

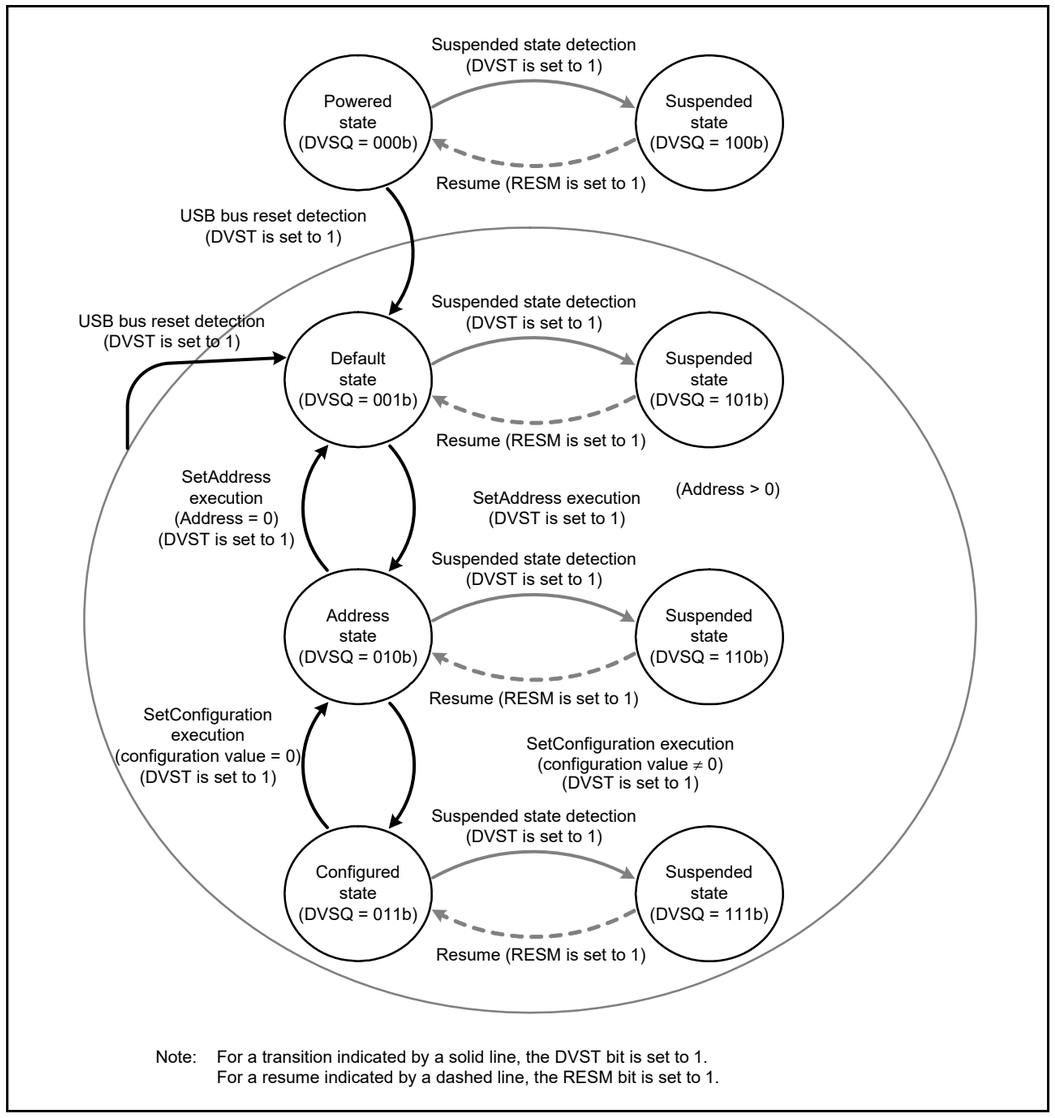
32.3.3.4 设备状态转换中断（设备控制器模式）

图32.14显示了USBFS设备状态转换的示意图。USBFS控制设备状态并产生设备状态转换中断。但是，从挂起状态的恢复（恢复信号检测）是通过恢复中断来检测的。可以在INTENB0中独立启用或禁用设备状态转换中断。可以在INTSTS0.DVSQ[2:0]位中检查状态已更改的设备。

当转换到默认状态时，检测到USB总线复位后会产生设备状态转换中断。

USBFS控制设备状态，只能在设备控制器中产生设备状态转换中断

mode.



Note: For a transition indicated by a solid line, the DVST bit is set to 1.
For a resume indicated by a dashed line, the RESM bit is set to 1.

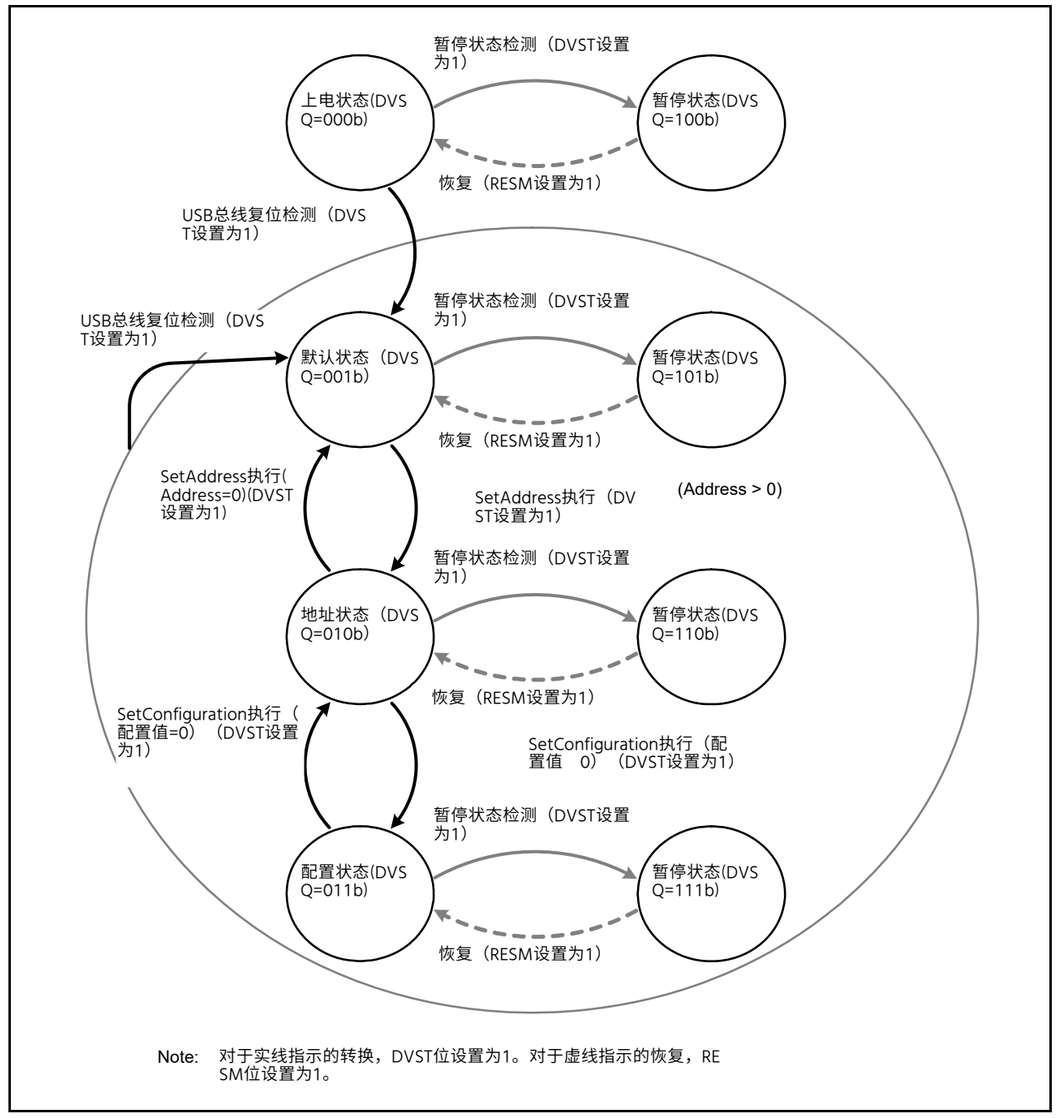
Figure 32.14 Device state transitions

32.3.3.5 Control transfer stage transition interrupt (device controller mode)

Figure 32.15 shows a diagram of the control transfer stage transitions of the USBFS. The USBFS controls the control transfer sequence and generates control transfer stage transition interrupts. Control transfer stage transition interrupts can be enabled or disabled independently in INTENB0. Transfer stages that have transitioned can be checked in the INTSTS0.CTSQ[2:0] bits.

Control transfer stage transition interrupts are generated only in device controller mode. This section describes control transfer sequence errors. If an error occurs, the DCPCTR.PID[1:0] bits are set to 1xb (STALL response).

mode.



Note: 对于实线指示的转换，DVST位设置为1。对于虚线指示的恢复，RESM位设置为1。

Figure 32.14 设备状态转换

32.3.3.5 控制转移阶段转换中断（设备控制器模式）

图32.15显示了USBFS的控制传输阶段转换图。USBFS控制控制传输序列并产生控制传输阶段转换中断。控制转移阶段转换中断可以在INTENB0中独立启用或禁用。可以在INTSTS0.CTSQ[2:0]位中检查已转换的传输阶段。

控制转移阶段转换中断仅在设备控制器模式下产生。本节描述控制传输序列错误。如果发生错误，则DCPCTR.PID[1:0]位设置为1xb（STALL响应）。

(1) Control read transfer errors

- An OUT token is received but no data is transferred in response to the IN token at the data stage
- An IN token is received at the status stage
- A data packet with DATAPID = DATA0 is received at the status stage.

(2) Control write transfer errors

- An IN token is received but no ACK is returned in response to the OUT token at the data stage
- A data packet with DATAPID = DATA0 is received as the first data packet at the data stage
- An OUT token is received at the status stage.

(3) Control write no data transfer errors

- An OUT token is received at the status stage.

At the control write transfer data stage, if the receive data length exceeds the wLength value of the USB request, it is not recognized as a control transfer sequence error. At the control read transfer status stage, packets other than zero-length packets are received by an ACK response and the transfer ends normally.

When a CTRT interrupt occurs in response to a sequence error (INTSTS0.CTRT = 1), the CTSQ[2:0] = 110b value is saved until the CTRT bit is set to 0, clearing the interrupt status. While CTSQ[2:0] = 110b is being saved, no CTRT interrupt for ending the setup stage is generated, even if a new USB request is received. The USBFS saves the setup stage completion status, and it generates a CTRT interrupt after the interrupt status is cleared by software.

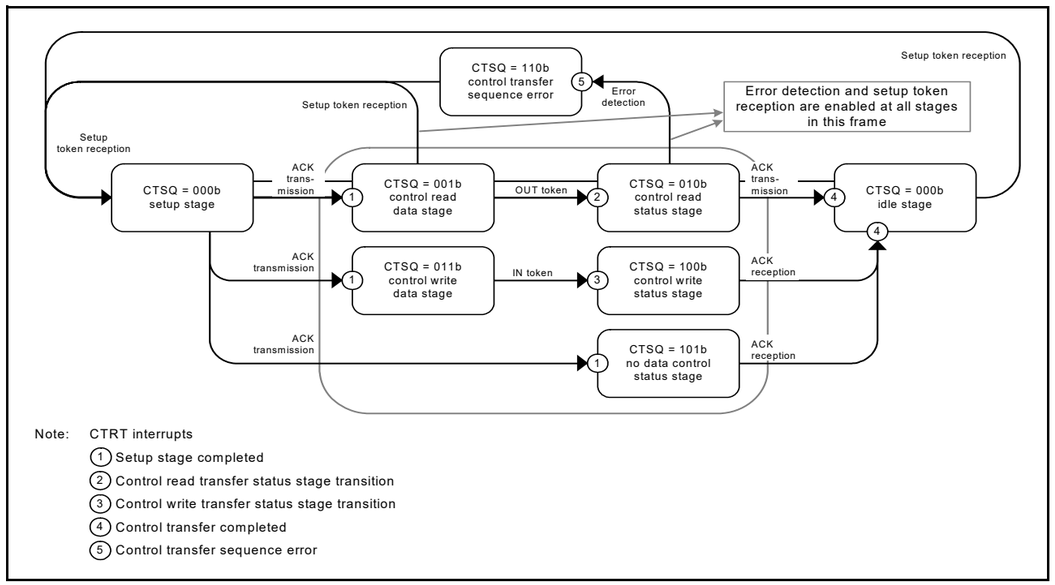


Figure 32.15 Control transfer stage transitions

32.3.3.6 Frame update interrupt

In host controller mode, an interrupt is generated when the frame number is updated.

In device controller mode, an SOFR interrupt is generated when the frame number is updated. The USBFS updates the frame number and generates an SOFR interrupt if it detects a new SOF packet during full-speed operation.

32.3.3.7 VBUS interrupt

When the USB_VBUS pin level changes, a VBUS interrupt is generated. The level of the USB_VBUS pin can be

(1) 控制读取传输错误

- 接收到OUT令牌，但在数据阶段没有响应IN令牌传输数据
- 在状态阶段收到一个IN令牌
- 在状态阶段接收到一个DATAPID=DATA0的数据包。

(2) 控制写入传输错误

- 在数据阶段接收到IN令牌但没有返回ACK以响应OUT令牌
- DATAPID=DATA0的数据包作为数据阶段的第一个数据包被接收
- 在状态阶段收到一个OUT令牌。

(3) 控制写入无数据传输错误

- 在状态阶段收到一个OUT令牌。

在控制写入传输数据阶段，如果接收数据长度超过USB请求的wLength值，则不被识别为控制传输序列错误。在控制读取传输状态阶段，除了零长度数据包之外的数据包被一个ACK响应接收并且传输正常结束。

当CTRT中断响应序列错误(INTSTS0.CTRT=1)时，将保存CTSQ[2:0]=110b值，直到CTRT位设置为0，清除中断状态。在保存CTSQ[2:0]=110b时，不会产生用于结束设置阶段的CTRT中断，即使收到新的USB请求也是如此。USBFS保存设置阶段完成状态，软件清除中断状态后产生CTRT中断。

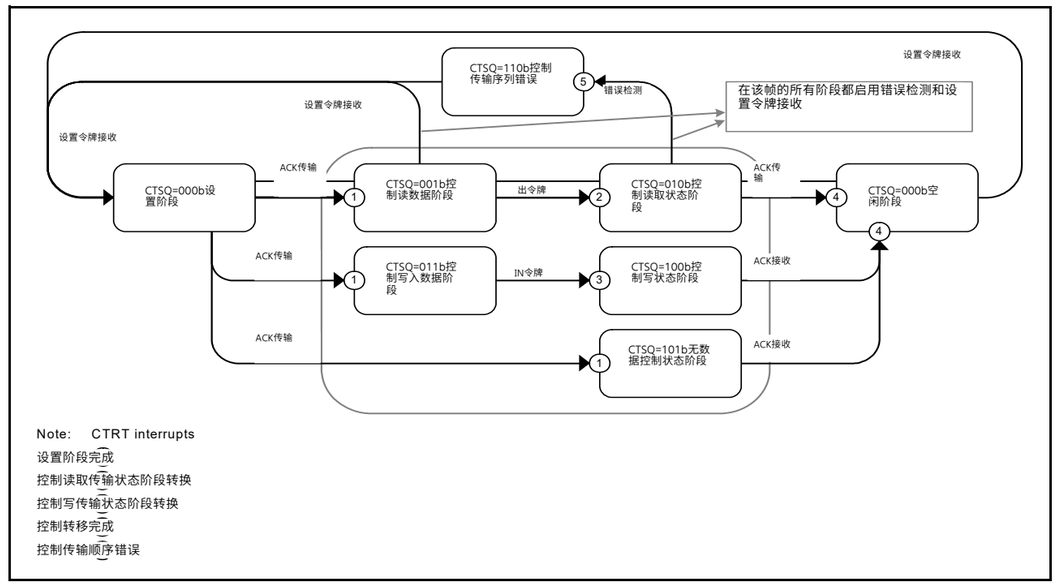


Figure 32.15 控制转移阶段转换

32.3.3.6 帧更新中断

在主机控制器模式下，更新帧号时会产生中断。

在设备控制器模式下，更新帧号时会产生SOFR中断。如果USBFS在全速运行期间检测到新的SOF数据包，则USBFS会更新帧号并生成SOFR中断。

32.3.3.7 VBUS interrupt

当USB_VBUS引脚电平改变时，会产生VBUS中断。USB_VBUS引脚的电平可以是

checked with the INTSTS0.VBSTS bit. Whether the host controller is connected or disconnected can be confirmed using the VBUS interrupt. If the system is activated with the host controller connected, the first VBUS interrupt is not generated, because there is no change in the USB_VBUS pin level.

32.3.3.8 Resume interrupt

In device controller mode, a resume interrupt is generated when the device state is the Suspend state and the USB bus state has changed (from J-state to K-state, or from J-state to SE0). Recovery from the Suspend state is detected by means of the resume interrupt.

In host controller mode, no resume interrupt is generated. Use the BCHG interrupt to detect a change in the USB bus state.

32.3.3.9 OVRCR interrupt

An OVRCR interrupt is generated when the USB_OVRCURA or USB_OVRCURB pin level has changed. The levels of the USB_OVRCURA and USB_OVRCURB pins can be checked in the SYSSTS0.OVCMON[1:0] flags. The external power supply IC can check whether overcurrent is detected using the OVRCR interrupt.

For OTG connections, the OVRCR interrupt allows you to check whether a change is detected in the VBUS comparator.

32.3.3.10 BCHG interrupt

A BCHG interrupt is generated when the USB bus state has changed. The BCHG interrupt can be used to detect whether a peripheral device is connected and can also be used to detect a remote wakeup in host controller mode. The BCHG interrupt is generated in both host and device controller modes.

32.3.3.11 DTCH interrupt

A DTCH interrupt occurs when a USB bus disconnect is detected in host controller mode. The USBFS detects bus disconnects in compliance with the USB 2.0 specification.

On interrupt detection, all pipes in which communications are being carried out for the relevant port must be terminated by software. The pipes enter the wait state for a bus connection to the port, waiting for an ATTCH interrupt to occur. Regardless of the value set in the associated interrupt enable bit, the USBFS hardware:

- Sets the DVSTCTR0.UACT bit for the port in which the DTCH interrupt is detected to 0
- Puts the port in which the DTCH interrupt occurred into the idle state.

32.3.3.12 SACK interrupt

A SACK interrupt is generated when an ACK response for the transmitted setup packet is received from the peripheral device in host controller mode. The SACK interrupt can be used to confirm that the setup transaction is successfully complete.

32.3.3.13 SIGN interrupt

A SIGN interrupt is generated when an ACK response for the transmitted setup packet is not correctly received from the peripheral device three consecutive times in host controller mode. The SIGN interrupt can be used to detect no ACK response transmitted from the peripheral device or corruption of an ACK packet.

32.3.3.14 ATTCH interrupt

An ATTCH interrupt is generated when J-state or K-state of the full-speed signal level is detected on the USB port for 2.5 µs in host controller mode. To be more specific, an ATTCH interrupt is detected on any of the following conditions:

- When K-state, SE0, or SE1 changes to J-state, and J-state continues 2.5 µs
- When J-state, SE0, or SE1 changes to K-state, and K-state continues 2.5 µs.

32.3.3.15 EOFERR interrupt

An EOFERR interrupt occurs when the USBFS detects that communication is not complete at the EOF2 timing defined in the USB 2.0 specification.

用INTSTS0.VBSTS位检查。主控制器是连接还是断开可以使用VBUS中断来确认。如果系统在连接主机控制器的情况下激活，则不会产生第一个VBUS中断，因为USB_VBUS引脚电平没有变化。

32.3.3.8 恢复中断

在设备控制器模式下，当设备状态为Suspend状态且USB总线状态发生变化（从J-state到K-state，或从J-state到SE0）时，会产生恢复中断。通过恢复中断检测从挂起状态的恢复。

在主机控制器模式下，不会产生恢复中断。使用BCHG中断来检测USB总线状态的变化。

32.3.3.9 OVRCR interrupt

当USB_OVRCURA或USB_OVRCURB引脚电平发生变化时，会产生OVRCR中断。USB_OVRCURA和USB_OVRCURB引脚的电平可以在SYSSTS0.OVCMON[1:0]标志中检查。外部电源IC可以使用OVRCR中断检查是否检测到过电流。

对于OTG连接，OVRCR中断允许您检查是否在VBUS比较器中检测到变化。

32.3.3.10 BCHG interrupt

当USB总线状态改变时会产生BCHG中断。BCHG中断可用于检测是否连接了外围设备，也可用于检测主机控制器模式下的远程唤醒。BCHG中断在主机和设备控制器模式下产生。

32.3.3.11 DTCH interrupt

当在主机控制器模式下检测到USB总线断开连接时，会发生DTCH中断。USBFS检测符合USB2.0规范的总线断开连接。

在检测到中断时，为相关端口执行通信的所有管道必须由软件终止。管道进入等待状态，等待总线连接到端口，等待ATTCH中断发生。无论相关中断使能位中设置的值如何，USBFS硬件：

- 将检测到DTCH中断的端口的DVSTCTR0.UACT位设置为0
- 将发生DTCH中断的端口置于空闲状态。

32.3.3.12 SACK中断

当在主机控制器模式下从外围设备接收到对发送的设置数据包的ACK响应时，将产生SACK中断。SACK中断可用于确认设置事务成功完成。

32.3.3.13 标志中断

在主机控制器模式下，如果连续三次未从外围设备正确接收到已发送的设置数据包的ACK响应，则会产生SIGN中断。SIGN中断可用于检测没有从外围设备发送的ACK响应或ACK数据包的损坏。

32.3.3.14 ATTCH interrupt

在主机控制器模式下，当在USB端口上检测到全速信号电平的J状态或K状态持续2.5µs时，将产生ATTCH中断。更具体地说，在以下任何条件下都会检测到ATTCH中断：

- 当K-state、SE0或SE1变为J-state时，J-state持续2.5μs
- 当J-state、SE0或SE1变为K-state时，K-state持续2.5μs。

32.3.3.15 EOFERR interrupt

当USBFS检测到在USB2.0规范中定义的EOF2时序未完成通信时，将发生EOFERR中断。

On interrupt detection, all pipes in which communications are being carried out for the relevant port must be terminated by software, and the port must be re-enumerated. Regardless of the value set in the associated interrupt enable bit, the USBFS hardware:

- Sets the DVSTCTR0.UACT bit for the port in which the EOFERR interrupt is detected to 0
- Puts the port in which the EOFERR interrupt is generated into the idle state.

32.3.4 Pipe Control

Table 32.17 lists the pipe settings for the USBFS. USB data transfer is performed through logical pipes that the software associates with endpoints. The USBFS provides 10 pipes that are used for data transfer. Set up the pipes based on your system specifications.

Table 32.17 Pipe settings

Register name	Bit name	Setting	Notes
DCPCFG PIPECFG	TYPE	Transfer type	Pipes 1 to 9: Settable
	BFRE	BRDY interrupt mode	Pipes 1 to 5: Settable
	DBLB	Double buffer select	Pipes 1 to 5: Settable
	DIR	Transfer direction select	IN or OUT settable
	EPNUM	Endpoint number	Pipes 1 to 9: Settable A value other than 0000b must be set when the pipe is used.
	SHTNAK	Selects disabled state for pipe when transfer ends	Pipes 1 and 2: Settable only for bulk transfers Pipes 3 to 5: Settable
DCPMAXP PIPEMAXP	DEVSEL	Device select	Referenced only in host controller mode.
	MXPS	Maximum packet size	Compliant with the USB 2.0 specification.
PIPEPERI	IFIS	Buffer flush	Pipes 1 and 2: Settable only for isochronous transfers Pipes 3 to 9: Setting disabled
	IITV	Interval counter	Pipes 1 and 2: Settable only for isochronous transfers Pipes 3 to 5: Setting disabled Pipes 6 to 9: Settable only in host controller mode
DCPCTR PIPEnCTR	BSTS	Buffer status	For the DCP, receive buffer status and transmit buffer status are switched with the ISEL bit.
	INBUFM	IN buffer monitor	Available only for pipes 1 to 5.
	SUREQ	Setup request	Settable only for the DCP and controlled in host controller mode
	SUREQCLR	SUREQ clear	Settable only for the DCP and controlled in host controller mode
	ATREPM	Auto response mode	Pipes 1 to 5: Settable only in device controller mode
	ACLRM	Auto buffer clear	Pipes 1 to 9: Settable
	SQCLR	Sequence clear	Clears the data toggle bit
	SQSET	Sequence set	Sets the data toggle bit
	SQMON	Sequence monitor	Monitors the data toggle bit
	PBUSY	Pipe busy status	-
	PID	Response PID	See section 32.3.4.6, Response PID.
PIPEnTRE	TRENB	Transaction counter enable	Pipes 1 to 5: Settable
	TRCLR	Current transaction counter clear	Pipes 1 to 5: Settable
PIPEnTRN	TRNCNT	Transaction counter	Pipes 1 to 5: Settable

32.3.4.1 Pipe control register switching procedures

The following bits in the pipe control registers can be changed only when USB communication is prohibited (PID = NAK).

Do not change the following registers and bits when USB communication is enabled (PID = BUF):

在检测到中断时，所有为相关端口执行通信的管道必须由软件终止，并且必须重新枚举该端口。无论相关中断使能位中设置的值如何，USBFS硬件：

- 将检测到EOFERR中断的端口的DVSTCTR0.UACT位设置为0
- 将产生EOFERR中断的端口置于空闲状态。

32.3.4 管道控制

表32.17列出了USBFS的管道设置。USB数据传输是通过软件与端点关联的逻辑管道执行的。USBFS提供了10个用于数据传输的管道。根据您的系统规格设置管道。

Table 32.17 管道设置

注册名称	位名称	Setting	Notes
DCPCFG PIPECFG	TYPE	传输类型	管道1至9：可设置
	BFRE	BRDY中断模式	管道1至5：可设置
	DBLB	双缓冲选择	管道1至5：可设置
	DIR	传输方向选择	输入或输出可设置
	EPNUM	端点编号	管道1至9：可设置 使用管道时，必须设置0000b以外的值。
	SHTNAK	传输结束时为管道选择禁用状态	管道1和2：仅可设置用于批量传输 管道3至5：可设置
DCPMAXP PIPEMAXP	DEVSEL	设备选择	仅在主机控制器模式下引用。
	MXPS	最大数据包大小	符合USB2.0规范。
PIPEPERI	IFIS	缓冲区刷新	管道1和2：仅可设置用于同步传输 管道3到9：设置禁用
	IITV	间隔计数器	管道1和2：仅可设置用于同步传输 管道3到5：禁用设置 管道6到9：仅在主机控制器模式下可设置
DCPCTR PIPEnCTR	BSTS	缓冲状态	对于DCP，接收缓冲器状态和发送缓冲器状态通过ISEL位切换。
	INBUFM	IN缓冲监视器	仅适用于管道1到5。
	SUREQ	设置请求	只能为DCP设置并在主机控制器模式下控制
	SUREQCLR	SUREQ clear	只能为DCP设置并在主机控制器模式下控制
	ATREPM	自动响应模式	管道1到5：仅在设备控制器模式下可设置
	ACLRM	自动缓冲区清除	管道1至9：可设置
	SQCLR	序列清晰	清除数据切换位
	SQSET	序列集	设置数据切换位
	SQMON	序列监视器	监控数据切换位
	PBUSY	管道繁忙状态	-
	PID	响应PID	请参阅第32.3.4.6节，响应PID。
PIPEnTRE	TRENB	事务计数器启用	管道1至5：可设置
	TRCLR	当前交易柜台清零	管道1至5：可设置
PIPEnTRN	TRNCNT	交易柜台	管道1至5：可设置

32.3.4.1 管道控制寄存器切换程序

只有当USB通信被禁止（PID=
NAK).

当启用USB通信(PID=BUF)时，请勿更改以下寄存器和位：

- Bits in DCPCFG and DCPMAXP
- SQCLR and SQSET bits in DCPCTR
- Bits in PIPECFG, PIPEMAXP, and PIPEPERI
- ATREPM, ACLRM, SQCLR, and SQSET bits in PIPEnCTR
- Bits in PIPEnTRE and PIPEnTRN.

To set these bits when USB communication is enabled (PID = BUF):

1. A request to change the bits in the pipe control register occurs.
2. Set the PID[1:0] bits associated with the pipe to NAK.
3. Wait until the associated PBUSY bit clears to 0.
4. Set the bits in the pipe control register.

The following bits in the pipe control registers can be changed only when the selected pipe information is not set in the CURPIPE[3:0] bits in CFIFOSEL, D0FIFOSEL, and D1FIFOSEL.

Do not set the following registers when the CURPIPE[3:0] bits are set:

- Bits in DCPCFG and DCPMAXP
- Bits in PIPECFG, PIPEMAXP and PIPEPERI.

To change pipe information, you must set the CURPIPE[3:0] bits in the port select registers to a pipe other than the one to be changed. For the DCP, the buffer must be cleared using the BCLR bit in the Port Control Register after the pipe information is changed.

32.3.4.2 Transfer types

The PIPECFG.TYPE[1:0] bits specify the following transfer types for each pipe:

- DCP: No setting is necessary (fixed at control transfer)
- Pipes 1 and 2: Set to bulk or isochronous transfer
- Pipes 3 to 5: Set to bulk transfer
- Pipes 6 to 9: Set to interrupt transfer.

32.3.4.3 Endpoint number

The PIPECFG.EPNUM[3:0] bits are used to set the endpoint number for each pipe. The DCP is fixed at endpoint 0. The other pipes can be set from endpoint 1 to 15.

- DCP: No setting is necessary (fixed at endpoint 0)
- Pipes 1 to 9: Select and set the endpoint numbers from 1 to 15 so that the combination of the PIPECFG.DIR and EPNUM[3:0] bits is unique.

32.3.4.4 Maximum packet size setting

Specify the maximum packet size for each pipe in the DCPMAXP.MXPS[6:0] and PIPEMAXP.MXPS[8:0] bits. The DCP and pipes 1 to 5 can be set to any of the maximum pipe sizes defined in the USB 2.0 specification. For pipes 6 to 9, the maximum packet size is 64 bytes. Set the maximum packet size as follows before starting a transfer (PID = BUF):

- DCP: Set to 8, 16, 32, or 64
- Pipes 1 to 5: Set to 8, 16, 32, or 64 for bulk transfers
- Pipes 1 and 2: Set between 1 and 256 for isochronous transfers
- Pipes 6 to 9: Set between 1 and 64.

32.3.4.5 Transaction counter for pipes 1 to 5 in the receiving direction

When the specified number of transactions is complete in the data packet receiving direction, the USBFS recognizes that

- DCPCFG和DCPMAXP中的位
- DCPCTR中的SQCLR和SQSET位
- PIPECFG、PIPEMAXP和PIPEPERI中的位
- PIPEnCTR中的ATREPM、ACLRM、SQCLR和SQSET位
- PIPEnTRE和PIPEnTRN中的位。

要在启用USB通信(PID=BUF)时设置这些位：

1. 发生更改管道控制寄存器中的位的请求。
2. 将与管道关联的PID[1:0]位设置为NAK。
3. 等到相关的PBUSY位清除为0。
4. 设置管道控制寄存器中的位。

管道控制寄存器中的以下位只有在所选管道信息未设置时才能更改CFIFOSEL、D0FIFOSEL和D1FIFOSEL中的CURPIPE[3:0]位。

设置CURPIPE[3:0]位时不要设置以下寄存器：

- DCPCFG和DCPMAXP中的位
- PIPECFG、PIPEMAXP和PIPEPERI中的位。

要更改管道信息，您必须将端口选择寄存器中的CURPIPE[3:0]位设置为要更改的管道以外的管道。对于DCP，必须在管道信息更改后使用端口控制寄存器中的BCLR位清除缓冲区。

32.3.4.2 传输类型

PIPECFG.TYPE[1:0]位为每个管道指定以下传输类型：

- DCP：无需设置（控制转移时固定）
- 管道1和2：设置为批量传输或同步传输
- 管道3到5：设置为批量传输
- 管道6到9：设置为中断传输。

32.3.4.3 端点编号

PIPECFG.EPNUM[3:0]位用于设置每个管道的端点编号。DCP固定在端点0。其他管道可以设置从端点1到15。

- DCP：无需设置（固定在端点0）
- 管道1到9：选择并设置从1到15的端点编号，以便PIPECFG.DIR和EPNUM[3:0]位是唯一的。

32.3.4.4 最大数据包大小设置

在DCPMAXP.MXPS[6:0]和PIPEMAXP.MXPS[8:0]位中指定每个管道的最大数据包大小。DCP和管道1到5可以设置为USB2.0规范中定义的任何最大管道尺寸。对于管道6到9，最大数据包大小为64字节。在开始传输之前设置最大数据包大小如下（PID=BUF）：

- DCP：设置为8、16、32或64
- 管道1到5：设置为8、16、32或64以进行批量传输
- 管道1和2：设置在1和256之间，用于同步传输
- 管道6到9：设置在1到64之间。

32.3.4.5 接收方向上管道1到5的事务计数器

当在数据包接收方向完成指定数量的事务时，USBFS识别

the transfer ended. Two transaction counters are provided: one is the PIPEnTRN register, which specifies the number of transactions to be executed, and the other is the current counter, which internally counts the number of executed transactions. If the PIPECFG.SHTNAK bit is set to 1, when the current counter value matches the specified number of transactions, the associated PIPEnCTR.PID[1:0] bits are set to NAK and the subsequent transfer is disabled. The transactions can be counted again from the beginning by initializing the current counter of the transaction counter function through the PIPEnTRE.TRCLR bit. The data read from PIPEnTRN differs depending on the PIPEnTRE.TRENB setting as follows:

- The TRENB bit = 0: Specified transaction counter value can be read
- The TRENB bit = 1: Current counter value indicating the internally counted number of executed transactions can be read.

The following constraints apply when working with the TRCLR bit:

- If the transactions are being counted and PID = BUF, the current counter cannot be cleared
- If there is any data left in the buffer, the current counter cannot be cleared.

32.3.4.6 Response PID

Specify the response PID for each pipe in the PID[1:0] bits in DCPCTR and PIPEnCTR. This section describes the USBFS operation with different response PID settings.

(1) Software response PID settings in host controller mode

Select the response PID to specify the execution of transactions as follows:

- NAK setting: Using pipes is disabled and no transactions are executed
- BUF setting: Transactions are executed based on the FIFO buffer state:
  - OUT direction: An OUT token is issued if the FIFO buffer contains transmit data.
  - IN direction: An IN token is issued if the FIFO buffer is not full and can receive data.
- STALL setting: Using pipes is disabled and no transactions are executed.

Note: Use the DCPCTR.SUREQ bit to execute setup transactions for the DCP.

(2) Software response PID settings in device controller mode

Select the response PID to respond as follows to transactions from the host:

- NAK setting: A NAK response is returned to all generated transactions
- BUF setting: A response is returned to transactions based on the FIFO buffer
- STALL setting: A STALL response is returned to all generated transactions.

Note: For setup transactions, an ACK response is always returned, regardless of the PID[1:0] bits setting, and the USB request is stored in the register.

Sections (3) and (4) describe situations in which the USBFS writes to the PID[1:0] bits because of specific transaction results.

(3) Hardware response PID settings in host controller mode

- NAK setting: PID = NAK is set in the following cases, and issuing of tokens is automatically stopped:
  - When a non-isochronous transfer is performed and an NRDY interrupt is generated (For details, see section 32.3.3.2, NRDY interrupt.)
  - If a short packet is received when the PIPECFG.SHTNAK bit is set to 1 for bulk transfers
  - If transaction counting ends when the SHTNAK bit is set to 1 for bulk transfers.
- BUF setting: The USBFS does not write this setting.

转移结束。提供了两个事务计数器：一个是PIPEnTRN寄存器，指定要执行的事务数，另一个是当前计数器，内部统计执行的事务数。如果PIPECFG.SHTNAK位设置为1，则当当前计数器值与指定的事务数匹配时，相关的PIPEnCTR.PID[1:0]位将设置为NAK，并禁用后续传输。通过PIPEnTRE.TRCLR位初始化事务计数器功能的当前计数器，事务可以从头开始重新计数。从PIPEnTRN读取的数据因PIPEnTRE.TRENB设置而异，如下所示：

- TRENB位=0：可以读取指定的事务计数器值
- TRENB位=1：可以读取表示内部计数的已执行事务数的当前计数器值。

使用TRCLR位时适用以下约束：

- 如果正在对事务进行计数且PID=BUF，则无法清除当前计数器
- 如果缓冲区中还有任何数据，则无法清除当前计数器。

32.3.4.6 响应PID

在DCPCTR和PIPEnCTR的PID[1:0]位中指定每个管道的响应PID。本节介绍具有不同响应PID设置的USBFS操作。

(1) 主机控制器模式下的软件响应PID设置

选择响应PID来指定事务的执行，如下所示：

- NAK设置：禁用使用管道并且不执行任何事务
- BUF设置：根据FIFO缓冲区状态执行事务：
  - OUT方向：如果FIFO缓冲区包含发送数据，则发出OUT令牌。
  - IN方向：如果FIFO缓冲区未满并且可以接收数据，则发出IN令牌。
- STALL设置：禁用使用管道并且不执行任何事务。

Note: 使用DCPCTR.SUREQ位执行DCP的设置事务。

(2) 设备控制器模式下的软件响应PID设置

选择响应PID以对来自主机的事务进行如下响应：

- NAK设置：向所有生成的事务返回NAK响应
- BUF设置：根据FIFO缓冲区向事务返回响应
- STALL设置：向所有生成的事务返回一个STALL响应。

Note: 对于设置事务，无论PID[1:0]位设置如何，始终返回ACK响应，并且USB请求存储在寄存器中。

第(3)和(4)节描述了USBFS由于特定事务结果而写入PID[1:0]位的情况。

(3) 主机控制器模式下的硬件响应PID设置

- NAK设置：PID=NAK在以下情况下设置，并且自动停止发行令牌：
  - 当执行非同步传输并产生NRDY中断时（详情请参阅第32.3.3.2节，NRDY中断。）
  - 如果在PIPECFG.SHTNAK位设置为1以进行批量传输时接收到短数据包
  - 如果在SHTNAK位设置为1以进行批量传输时事务计数结束。
- BUF设置：USBFS不写入此设置。

- STALL setting: PID = STALL is set in the following cases, and issuing of tokens is automatically stopped:
  - When STALL is received in response to a transmitted token
  - When a received data packet exceeds the maximum packet size.

(4) Hardware response PID settings in device controller mode

- NAK setting: PID = NAK is set in the following cases, and a NAK response is returned to transactions:
  - When the setup token is received normally (DCP only)
  - If transaction counting ends or a short packet is received when the PIPECFG.SHTNAK bit is set to 1 for bulk transfers.
- BUF setting: There is no BUF writing by the USBFS.
- STALL setting: PID = STALL is set in the following cases, and a STALL response is returned to transactions:
  - When a received data packet exceeds the maximum packet size
  - When a control transfer sequence error is detected (DCP only).

32.3.4.7 Data PID sequence bit

The USBFS automatically toggles the sequence bit in the data PID when data is transferred successfully in the control transfer data stage, bulk transfer, and interrupt transfer. The sequence bit of the next data PID to be transmitted can be confirmed with the SQMON bit in DCPCTR and PIPEnCTR. When data is transmitted, the sequence bit toggles on ACK handshake reception. When data is received, the sequence bit toggles on ACK handshake transmission. The SQCLR and SQSET bits in DCPCTR and PIPEnCTR registers can be used to change the data PID sequence bit.

In device controller mode when control transfers are used, the USBFS automatically sets the sequence bit for stage transitions. DATA1 is returned when the setup stage ends. The sequence bit is not referenced and PID = DATA1 is returned in the status stage. Therefore, no software settings are required. However, in host controller mode when control transfers are used, the sequence bit must be set by software for the stage transitions.

For ClearFeature requests for transmission or reception, the data PID sequence bit must be set by software in both host and device controller modes.

32.3.4.8 Response PID = NAK function

The USBFS provides a function for disabling pipe operation (PID response = NAK) when the final data packet of a transaction is received. The USBFS automatically distinguishes this based on reception of a short packet or the transaction counter. Enable this function by setting the PIPECFG.SHTNAK bit to 1.

When the double buffer mode is being used for the FIFO buffer, using this function enables reception of data packets in transfer units. If pipe operation is disabled, the software must enable the pipe again (PID response = BUF).

The response PID = NAK function can be used only for bulk transfers.

32.3.4.9 Auto response mode

For bulk transfer pipes (1 to 5), when the PIPEnCTR.ATREPM bit is set to 1, a transition is made to auto response mode. During an OUT transfer (PIPECFG.DIR = 0), OUT-NAK mode is invoked, and during an IN transfer (DIR = 1), null auto response mode is invoked.

32.3.4.10 OUT-NAK mode

For bulk OUT transfer pipes, NAK is returned in response to an OUT token, and an NRDY interrupt is output when the PIPEnCTR.ATREPM bit is set to 1. To transition from normal mode to OUT-NAK mode, specify OUT-NAK mode while pipe operation is disabled (PID[1:0] = 00b for NAK response). Next enable pipe operation (PID[1:0] = 01b for BUF response), on which OUT-NAK mode becomes valid. If an OUT token is received immediately before pipe operation is disabled, the token data is normally received, and an ACK is returned to the host.

To transition from OUT-NAK mode to normal mode, cancel OUT-NAK mode while pipe operation is disabled (NAK). Next enable pipe operation (BUF). In normal mode, reception of OUT data is enabled.

- STALL设置：PID=STALL在以下情况下设置，并且自动停止发行令牌：
  - 当接收到STALL以响应传输的令牌时
  - 当接收到的数据包超过最大包大小时。

(4) 设备控制器模式下的硬件响应PID设置

- NAK设置：PID=NAK在以下情况下设置，并向事务返回NAK响应：
  - 正常接收设置令牌时（仅DCP）
  - 如果在PIPECFG.SHTNAK位设置为1以进行批量传输时，事务计数结束或收到短数据包。
- BUF设置：USBFS没有写入BUF。
- STALL设置：PID=STALL在以下情况下设置，并向事务返回STALL响应：
  - 当接收到的数据包超过最大包大小时
  - 当检测到控制传输序列错误时（仅限DCP）。

32.3.4.7 数据PID序列位

当数据在控制传输数据阶段、批量传输和中断传输成功传输时，USBFS会自动切换数据PID中的序列位。下一个要发送的数据PID的序列位可以通过DCPCTR和PIPEnCTR中的SQMON位来确认。发送数据时，序列位在ACK握手接收时切换。当接收到数据时，序列位在ACK握手传输上切换。DCPCTR和PIPEnCTR寄存器中的SQCLR和SQSET位可用于更改数据PID序列位。

在使用控制传输的设备控制器模式下，USBFS自动设置阶段转换的序列位。DATA1在设置阶段结束时返回。不引用序列位，在状态阶段返回PID=DATA1。因此，不需要任何软件设置。但是，在使用控制传输的主机控制器模式下，必须由软件设置序列位以进行阶段转换。

对于发送或接收的ClearFeature请求，数据PID序列位必须由软件在主机和设备控制器模式下设置。

32.3.4.8 响应PID=NAK功能

USBFS提供了在接收到事务的最终数据包时禁用管道操作（PID响应=NAK）的功能。USBFS根据收到的短数据包或事务计数器自动区分这一点。通过将PIPECFG.SHTNAK位设置为1来启用此功能。

当FIFO缓冲区使用双缓冲区模式时，使用此功能可以接收以传输为单位的数据包。如果管道操作被禁用，软件必须再次启用管道（PID响应=BUF）。

响应PID=NAK函数只能用于批量传输。

32.3.4.9 自动响应模式

对于批量传输管道（1到5），当PIPEnCTR.ATREPM位设置为1时，将转换到自动响应模式。在OUT传输期间(PIPECFG.DIR=0)，将调用OUT-NAK模式，在IN传输期间(DIR=1)，将调用空自动响应模式。

32.3.4.10 OUT-NAK mode

对于批量OUT传输管道，NAK响应OUT令牌返回，并且当PIPEnCTR.ATREPM位设置为1时输出NRDY中断。要从正常模式转换到OUT-NAK模式，请指定OUT-NAK模式，同时管道操作被禁用（PID[1:0]=00b用于NAK响应）。接下来启用管道操作（PID[1:0]=01b用于BUF响应），此时OUT-NAK模式变为有效。如果在禁用管道操作之前立即收到OUT令牌，则正常接收令牌数据，并向主机返回ACK。

要从OUT-NAK模式转换到正常模式，请在禁用管道操作(NAK)时取消OUT-NAK模式。
接下来启用管道操作(BUF)。在正常模式下，可以接收OUT数据。

32.3.4.11 Null auto response mode

For bulk IN transfer pipes, zero-length packets are continuously transmitted when the PIPEnCTR.ATREPM bit is set to 1.

To transition from normal mode to null auto response mode, specify null auto response mode while pipe operation is disabled (response PID = NAK). Next enable pipe operation (response PID = BUF) on which null auto response mode becomes valid. Before setting null auto response mode, check that PIPEnCTR.INBUFM = 0, because the mode can be set only when the buffer is empty. If the INBUFM bit is 1, empty the buffer using the PIPEnCTR.ACLRM bit. Do not write data from the FIFO port while a transition to null auto response mode is being made.

To transition from null auto response mode to normal mode, keep pipe operation disabled (response PID = NAK) for the period of the zero-length packet transmission (about 10 µs) before canceling the null auto response mode. In normal mode, data can be written from the FIFO port, so packet transmission to the host is enabled by enabling pipe operation (response PID = BUF).

32.3.5 FIFO Buffer

The USBFS provides a FIFO buffer for data transfers, and it manages the memory area used for each pipe. The FIFO buffer has two states depending on whether the access right is assigned to the system (CPU side) or the USBFS (SIE side).

(1) Buffer status

Table 32.18 and Table 32.19 show the buffer status in the USBFS. The FIFO buffer status can be confirmed using the DCPCTR.BSTS and PIPEnCTR.INBUFM bits. The transfer direction for the FIFO buffer can be specified in either the PIPECFG.DIR or CFIFOSEL.ISEL bit (when DCP is selected).

The INBUFM bit is valid for pipes 0 to 5 in the transmitting direction.

When a transmitting pipe uses double buffering, the software can read the BSTS bit to monitor the FIFO buffer status on the CPU side and the INBUFM bit to monitor the FIFO buffer status on the SIE side. When write access to the FIFO port by the CPU or DMA/DTC is slow and the buffer empty status cannot be determined using the BEMP interrupt, the software can use the INBUFM bit to confirm the end of transmission.

Table 32.18 Buffer status indicated in the BSTS bit

ISEL or DIR	BSTS	FIFO buffer status
0 (receiving direction)	0	There is no received data, or data is being received. Reading from the FIFO port is disabled.
0 (receiving direction)	1	There is received data, or a zero-length packet is received. Reading from the FIFO port is allowed. When a zero-length packet is received, reading is not possible and the buffer must be cleared.
1 (transmitting direction)	0	Transmission has not completed. Writing to the FIFO port is disabled.
1 (transmitting direction)	1	Transmission is complete. CPU write is allowed.

Table 32.19 Buffer status indicated in the INBUFM bit

DIR	INBUFM	FIFO buffer status
0 (receiving direction)	Invalid	Invalid
1 (transmitting direction)	0	Transmission is complete. There is no data waiting to be transmitted.
1 (transmitting direction)	1	The FIFO port has written data to the buffer. There is data to be transmitted.

32.3.6 FIFO Buffer Clearing

Table 32.20 shows the methods for clearing the FIFO buffer. The FIFO buffer can be cleared using BCLR bit in the port control register, DnFIFOSEL.DCLRM, or the PIPEnCTR.ACLRM bit.

32.3.4.11 空自动响应模式

对于批量IN传输管道，当PIPEnCTR.ATREPM位设置为1时，将连续传输零长度数据包。

要从正常模式转换为空自动响应模式，请在禁用管道操作时指定空自动响应模式（响应PID=NAK）。接下来启用空自动响应模式有效的管道操作（响应PID=BUF）。在设置空自动响应模式之前，请检查PIPEnCTR.INBUFM=0，因为只有在缓冲区为空时才能设置模式。如果INBUFM位为1，则使用PIPEnCTR.ACLRM位清空缓冲区。在转换到空自动响应模式时，不要从FIFO端口写入数据。

要从空值自动响应模式转换到正常模式，在取消空值自动响应模式之前，在零长度数据包传输期间（约10µs）保持管道操作禁用（响应PID=NAK）。在正常模式下，可以从FIFO端口写入数据，因此通过启用管道操作（响应PID=BUF）来启用到主机的数据包传输。

32.3.5 FIFO Buffer

USBFS为数据传输提供FIFO缓冲区，并管理用于每个管道的内存区域。根据访问权限是分配给系统（CPU端）还是USBFS（SIE端），FIFO缓冲区有两种状态。

(1) 缓冲状态

表32.18和表32.19显示了USBFS中的缓冲区状态。FIFO缓冲区状态可以使用确认DCPCTR.BSTS和PIPEnCTR.INBUFM位。FIFO缓冲区的传输方向可以在任一pipecfg.dir或cfifosel.isel位（选择DCP时）。

INBUFM位对传输方向的管道0到5有效。

当传输管道使用双缓冲时，软件可以读取BSTS位来监控CPU侧的FIFO缓冲区状态，以及读取INBUFM位来监控SIE侧的FIFO缓冲区状态。当CPU或DMADTC对FIFO端口的写访问速度较慢且无法使用BEMP中断确定缓冲区空状态时，软件可以使用INBUFM位来确认传输结束。

Table 32.18 BSTS位中指示的缓冲区状态

ISEL或DIR	BSTS	FIFO缓冲区状态
0 (receiving direction)	0	没有接收到数据，或正在接收数据。 禁止从FIFO端口读取。
0 (receiving direction)	1	有接收数据，或接收到零长度数据包。 允许从FIFO端口读取。 当接收到零长度数据包时，无法读取，必须清除缓冲区。
1 (transmitting direction)	0	传输尚未完成。 禁止写入FIFO端口。
1 (transmitting direction)	1	传输完成。 允许CPU写入。

Table 32.19 INBUFM位中指示的缓冲区状态

DIR	INBUFM	FIFO缓冲区状态
0 (receiving direction)	Invalid	Invalid
1 (transmitting direction)	0	传输完成。 没有等待传输的数据。
1 (transmitting direction)	1	FIFO端口已将数据写入缓冲区。 有数据要传输。

32.3.6 FIFO缓冲区清除

表32.20显示了清除FIFO缓冲区的方法。可以使用端口控制寄存器中的BCLR位、DnFIFOSEL.DCLRM或PIPEnCTR.ACLRM位清除FIFO缓冲区。

Single or double buffering can be selected for pipes 1 to 5 in the PIPECFG.DBLB bit.

Table 32.20 Buffer clearing methods

FIFO buffer clearing mode	Clearing FIFO buffer on the CPU side	Mode for automatically clearing the FIFO buffer after reading the specified pipe data	Auto buffer clear mode for discarding all received packets
Register used	CFIFOCTR DnFIFOCTR	DnFIFOSEL	PIPEnCTR
Bit used	BCLR	DCLRM	ACLRM
Clearing condition	Cleared by writing 1	1: Mode valid 0: Mode invalid	1: Mode valid 0: Mode invalid

(1) Auto buffer clear mode function

The USBFS discards all received data packets if the PIPEnCTR.ACLRM bit is set to 1. If a correct data packet is received, the ACK response is returned to the host controller. The auto buffer clear mode function can only be set in the FIFO buffer reading direction.

Setting the ACLRM bit to 1 and then to 0 clears the FIFO buffer of the selected pipe regardless of the access direction. An access cycle of at least 100 ns is required for the internal hardware sequence processing between ACLRM = 1 and ACLRM = 0.

32.3.7 FIFO Port Functions

Table 32.21 shows the settings for the FIFO port functions. In write access, writing data until the maximum packet size is reached automatically enables transmission of the data. To enable transmission before the maximum packet size is reached, set the BVAL flag in the port control register to end writing. To send a zero-length packet, use the BCLR bit to clear the buffer, and then set the BVAL flag to end writing.

In reading, reception of new packets is automatically enabled when all data is read. Data cannot be read when a zero-length packet is received (DTLN[8:0] = 0), so the buffer must be cleared with the BCLR bit. The length of the receive data can be confirmed in the DTLN[8:0] bits in the port control register.

Table 32.21 FIFO port function settings

Register name	Bit name	Description
CFIFOSEL, DnFIFOSEL (n = 0, 1)	RCNT	Selects DTLN[8:0] read mode
	REW	FIFO buffer rewind (re-read, rewrite)
	DCLRM	Automatically clears receive data for a specified pipe after the data is read (only for DnFIFO)
	DREQE	Enables DMA/DTC transfers (only for DnFIFO)
	MBW	FIFO port access bit width
	BIGEND	Selects FIFO port endian
	ISEL	FIFO port access direction (only for DCP)
	CURPIPE	Selects the current pipe
CFIFOCTR, DnFIFOCTR (n = 0, 1)	BVAL	Ends writing to the FIFO buffer
	BCLR	Clears the FIFO buffer on the CPU side
	DTLN	Checks the length of receive data

(1) FIFO port selection

Table 32.22 shows the pipes that can be selected with the different FIFO ports. The pipe to be accessed must be selected in the CURPIPE[3:0] bits in the port select register. After the pipe is selected, the software must check whether the written value can be read correctly from the CURPIPE[3:0] bits. (If the previous pipe number is read, it indicates that the USBFS is modifying the pipe.) Next, the software checks that the FRDY bit in the port control register is 1.

In addition, the software must specify the bus width to be accessed in the MBW bit in the port select register. The FIFO buffer access direction conforms to the PIPECFG.DIR setting. For the DCP only, the ISEL bit in the port select register

可以在PIPECFG.DBLB位中为管道1到5选择单缓冲或双缓冲。

Table 32.20 缓冲区清除方法

FIFO缓冲区清除模式	清除FIFO缓冲区CPU端	读取指定管道数据后自动清除FIFO缓冲区的模式	自动缓冲区清除模式，用于丢弃所有接收到的数据包
注册使用	CFIFOCTR DnFIFOCTR	DnFIFOSEL	PIPEnCTR
使用的位	BCLR	DCLRM	ACLRM
清算条件	通过写1清除	1：模式有效0 ：模式无效	1：模式有效0 ：模式无效

(1) 自动缓冲清除模式功能

如果PIPEnCTR.ACLRM位设置为1，USBFS将丢弃所有接收到的数据包。如果接收到正确的数据包，则向主机控制器返回ACK响应。自动缓冲区清除模式功能只能在FIFO缓冲区读取方向设置。

无论访问方向如何，将ACLRM位设置为1，然后设置为0都会清除所选管道的FIFO缓冲区。ACLRM=1和之间的内部硬件序列处理需要至少100ns的访问周期
ACLRM = 0.

32.3.7 FIFO端口功能

表32.21显示了FIFO端口功能的设置。在写访问中，在达到最大数据包大小之前写入数据会自动启用数据传输。要在达到最大数据包大小之前启用传输，请设置端口控制寄存器中的BVAL标志以结束写入。要发送零长度数据包，请使用BCLR位清除缓冲区，然后设置BVAL标志以结束写入。

在读取中，当所有数据被读取时，自动启用新数据包的接收。接收到零长度数据包时（DTLN[8:0]=0）无法读取数据，因此必须使用BCLR位清除缓冲区。接收数据的长度可以在端口控制寄存器的DTLN[8:0]位中确认。

Table 32.21 FIFO端口功能设置

注册名称	位名称	Description
CFIFOSEL, DnFIFOSEL (n = 0, 1)	RCNT	选择DTLN[8:0]读取模式
	REW	FIFO缓冲区倒带（重新读取、重写）
	DCLRM	读取数据后自动清除指定管道的接收数据（仅适用于DnFIFO）
	DREQE	启用DMADTC传输（仅适用于DnFIFO）
	MBW	FIFO端口访问位宽
	BIGEND	选择FIFO端口字节序
	ISEL	FIFO端口访问方向（仅适用于DCP）
	CURPIPE	选择当前管道
CFIFOCTR, DnFIFOCTR (n = 0, 1)	BVAL	结束写入FIFO缓冲区
	BCLR	清除CPU端的FIFO缓冲区
	DTLN	检查接收数据的长度

(1) 先进先出端口选择

表32.22显示了可以使用不同FIFO端口选择的管道。必须在端口选择寄存器的CURPIPE[3:0]位中选择要访问的管道。选择管道后，软件必须检查是否可以从CURPIPE[3:0]位正确读取写入的值。（如果读取了之前的管道号，则表明USBFS正在修改管道。）接下来，软件检查端口控制寄存器中的FRDY位是否为1。

此外，软件必须在端口选择寄存器的MBW位中指定要访问的总线宽度。FIFO缓冲区访问方向符合PIPECFG.DIR设置。仅对于DCP，端口选择寄存器中的ISEL位

determines the direction.

Table 32.22 FIFO port access by pipe

Pipe	Access method	Ports that can be used
DCP	CPU access	CFIFO port register
Pipes 1 to 9	CPU access	• CFIFO port register • D0FIFO/D1FIFO port register
	DMA/DTC access	D0FIFO/D1FIFO port register

(2) REW bit

It is possible to temporarily stop access to a pipe currently being accessed, access a different pipe, and then continue processing for the first pipe again. The REW bit in the port select register is used for this processing.

If a pipe is selected in the CURPIPE[3:0] bits in the port select register with the REW bit set to 1, the pointer used for reading from and writing to the FIFO buffer is reset, and reading or writing can be carried out from the first byte. If a pipe is selected with 0 set for the REW bit, data can be read and written in continuation from the previous selection, without the pointer being reset.

To access the FIFO port, the software must check that the FRDY bit in the port control register is 1 after selecting a pipe.

32.3.8 DMA Transfers (D0FIFO and D1FIFO Ports)

(1) Overview of DMA transfers

For pipes 1 to 9, the FIFO port can be accessed using the DMAC. When buffer access for a pipe targeted for DMA transfer is enabled, a DMA transfer request is issued.

Select the unit of transfer to the FIFO port in the DnFIFOSEL.MBW bit, and select the pipe targeted for the DMA transfer in the DnFIFOSEL.CURPIPE[3:0] bits. Do not change the selected pipe during the DMA transfer.

(2) DnFIFO auto clear mode (D0FIFO and D1FIFO port reading direction)

If 1 is set in the DnFIFOSEL.DCLRM bit, the USBFS automatically clears the FIFO buffer of the selected pipe when reading of data from the FIFO buffer is complete.

Table 32.23 shows the packet reception and FIFO buffer clearing processing by software for each of the settings. As shown in the table, the buffer clearing conditions depend on the value set in the PIPECFG.BFRE bit. Using the DnFIFOSEL.DCLRM bit eliminates the need for the buffer to be cleared by software in any situation that requires buffer clearing. This enables DMA transfers without involving software.

The DnFIFO auto clear mode can only be set in the FIFO buffer reading direction.

Table 32.23 Packet reception and FIFO buffer clearing processing by software

Buffer status when packet is received	Register setting			
	DCLRM = 0		DCLRM = 1	
	BFRE = 0	BFRE = 1	BFRE = 0	BFRE = 1
Buffer full	No clearing required	No clearing required	No clearing required	No clearing required
Zero-length packet reception	Clearing required	Clearing required	No clearing required	No clearing required
Normal short packet reception	No clearing required	Clearing required	No clearing required	No clearing required
Transaction count end	No clearing required	Clearing required	No clearing required	No clearing required

32.3.9 Control Transfers Using the DCP

The DCP is used for data transfers in the control transfer data stage. The FIFO buffer of the DCP is a 64-byte single buffer with a fixed area for both control reads and control writes. The FIFO buffer can be accessed only through the CFIFO port.

决定方向。

Table 32.22 通过管道访问FIFO端口

Pipe	访问方法	可以使用的端口
DCP	CPU访问	CFIFO端口寄存器
管道1至9	CPU访问	CFIFO端口寄存器 D0FIFOD1FIFO端口寄存器
	DMA/DTC access	D0FIFOD1FIFO端口寄存器

(2) REW位

可以暂时停止对当前正在访问的管道的访问，访问不同的管道，然后再次继续处理第一个管道。端口选择寄存器中的REW位用于此处理。

如果在端口选择寄存器的CURPIPE[3:0]位中选择了一个管道，并且REW位设置为1，则用于读取和写入FIFO缓冲区的指针复位，可以进行读取或写入从第一个字节开始。如果在REW位设置为0的情况下选择管道，则可以从先前的选择继续读取和写入数据，而无需重置指针。

要访问FIFO端口，软件必须在选择管道后检查端口控制寄存器中的FRDY位是否为1。

32.3.8 DMA传输（D0FIFO和D1FIFO端口）

(1) DMA传输概述

对于管道1到9，可以使用DMAC访问FIFO端口。当启用以DMA传输为目标的管道的缓冲区访问时，将发出DMA传输请求。

在DnFIFOSEL.MBW位中选择传输到FIFO端口的单位，并在DnFIFOSEL.CURPIPE[3:0]位中选择DMA传输的目标管道。在DMA传输期间不要更改选定的管道。

(2) DnFIFO自动清除模式（D0FIFO和D1FIFO端口读取方向）

如果DnFIFOSEL.DCLRM位设置为1，USBFS会在从FIFO缓冲区读取数据完成时自动清除所选管道的FIFO缓冲区。

表32.23显示了针对每个设置通过软件进行的数据包接收和FIFO缓冲区清除处理。如表所示，缓冲区清除条件取决于PIPECFG.BFRE位中设置的值。使用DnFIFOSEL.DCLRM位无需在任何需要清除缓冲区的情况下通过软件清除缓冲区。这可以在不涉及软件的情况下实现DMA传输。

DnFIFO自动清除模式只能设置在FIFO缓冲区读取方向。

Table 32.23 通过软件进行数据包接收和FIFO缓冲区清除处理

收到数据包时的缓冲区状态	注册设置			
	DCLRM = 0		DCLRM = 1	
	BFRE = 0	BFRE = 1	BFRE = 0	BFRE = 1
缓冲区已满	无需清算	无需清算	无需清算	无需清算
零长度数据包接收	需要清算	需要清算	无需清算	无需清算
正常短包接收	无需清算	需要清算	无需清算	无需清算
交易计数结束	无需清算	需要清算	无需清算	无需清算

32.3.9 使用DCP进行控制传输

DCP用于控制传输数据阶段的数据传输。DCP的FIFO缓冲区是一个64字节的单缓冲区，具有用于控制读取和控制写入的固定区域。FIFO缓冲区只能通过CFIFO端口访问。

32.3.9.1 Control transfers in host controller mode

(1) Setup stage

The USQREQ, USBVAL, USBINDX, and USBLENG registers are used to transmit USB requests for setup transactions. Writing the setup packet data to the registers and then writing 1 to the DCPCTR.SUREQ bit transmits the specified data for the setup transaction. On completion of the transaction, the SUREQ bit clears to 0. Do not change these USB request registers while SUREQ = 1.

When an attached function device is detected, the software must issue the first setup transaction for the device using this sequence with the DCPMAXP.DEVSEL[3:0] bits cleared to 0 and the DEVADD0.USBSPD[1:0] bits set appropriately.

When an attached function device is shifted to the Address state, the software must issue setup transactions using this sequence with the assigned USB address set in the DEVSEL[3:0] bits and the bits in DEVADDn corresponding to the specified USB address set appropriately. For example, when PIPEMAXP.DEVSEL[3:0] = 0010b, make appropriate settings in DEVADD2. When PIPEMAXP.DEVSEL[3:0] = 0101b, make appropriate settings in DEVADD5.

When the setup transaction data is sent, an interrupt request is generated based on the response from the peripheral device (SIGN or SACK bit in INTSTS1). This interrupt request allows the software to check the setup transaction result.

A DATA0 data packet (USB request) for the setup transaction is always transmitted regardless of the status of the DCPCTR.SQMON bit.

(2) Data stage

The data stage is used to transfer data using the DCP FIFO buffer.

Before accessing the DCP FIFO buffer, specify the access direction in the CFIFOSEL.ISEL bit. Specify the transfer direction in the DCPCFG.DIR bit.

For the first data packet of the data stage, the data PID must be transferred as DATA1. Set data PID = DATA1 in the DCPCTR.SQSET bit and set the PID bits = BUF. Completion of data transfer is detected using the BRDY or BEMP interrupt.

For control write transfers, when the number of data bytes to be sent is an integer multiple of the maximum packet size, the software must send a zero-length packet at the end.

(3) Status stage

The status stage is used for zero-length packet data transfers in the reverse direction of the data stage. As in the data stage, data is transfered using the DCP FIFO buffer. Transactions are executed using the same procedure as the data stage.

Data packets in the status stage must be transmitted and received with the data PID set to DATA1 using the DCPCTR.SQSET bit.

When a zero-length packet is received, check the receive-data length in the CFIFOCTR.DTLN[8:0] bits after a BRDY interrupt is generated, and then clear the FIFO buffer using the BCLR bit.

32.3.9.2 Control transfers in device controller mode

(1) Setup stage

The USBFS sends an ACK response to a normal setup packet for the USBFS. The USBFS operates in the setup stage as follows:

On receiving a new setup packet, the USBFS sets the following bits:

- Sets the INTSTS0.VALID bit to 1
- Sets the DCPCTR.PID[1:0] bits to NAK
- Sets the DCPCTR.CCPL bit to 0.

When the USBFS receives a data packet following a setup packet, it stores the USB request parameters in USBREQ, USBVAL, USBINDX, and USBLENG.

Before performing the response processing for a control transfer, set the VALID flag to 0. When the VALID bit = 1, PID

32.3.9.1 主机控制器模式下的控制传输

(1) 设置阶段

USQREQ、USBVAL、USBINDX和USBLENG寄存器用于传输设置事务的USB请求。将设置数据包数据写入寄存器，然后向DCPCTR.SUREQ位写入1，以传输设置事务的指定数据。事务完成后，SUREQ位清除为0。在SUREQ=1时不要更改这些USB请求寄存器。

当检测到连接的功能器件时，软件必须使用此序列为器件发出第一个设置事务，其中DCPMAXP.DEVSEL[3:0]位清零，DEVADD0.USBSPD[1:0]位适当设置。

当连接的功能器件转移到地址状态时，软件必须使用此序列发出设置事务，其中指定的USB地址设置在DEVSEL[3:0]位中，并且DEVADDn中的位对应于指定的USB地址设置适当。例如，当PIPEMAXP.DEVSEL[3:0]=0010b时，在DEVADD2中进行适当的设置。当PIPEMAXP.DEVSEL[3:0]=0101b时，在DEVADD5中进行适当的设置。

发送设置事务数据时，根据外围设备的响应（INTSTS1中的SIGN或SACK位）生成中断请求。该中断请求允许软件检查设置事务结果。

一个DATA0数据包（USB请求）用于设置事务总是被传输，无论状态如何
DCPCTR.SQMON bit.

(2) 数据阶段

数据级用于使用DCPFIFO缓冲区传输数据。

在访问DCPFIFO缓冲区之前，请在CFIFOSEL.ISEL位中指定访问方向。在DCPCFG.DIR位中指定传输方向。

对于数据阶段的第一个数据包，数据PID必须作为DATA1传输。在DCPCTR.SQSET位中设置数据PID=DATA1，并设置PID位=BUF。使用BRDY或BEMP中断检测数据传输的完成。

对于控制写传输，当要发送的数据字节数是最大数据包大小的整数倍时，软件必须在最后发送一个长度为零的数据包。

(3) 状态阶段

状态阶段用于在数据阶段的相反方向上进行零长度分组数据传输。与数据阶段一样，使用DCPFIFO缓冲区传输数据。事务使用与数据阶段相同的过程执行。

状态阶段的数据包必须在数据PID设置为DATA1的情况下使用
DCPCTR.SQSET bit.

当接收到零长度数据包时，在产生BRDY中断后检查CFIFOCTR.DTLN[8:0]位中的接收数据长度，然后使用BCLR位清除FIFO缓冲区。

32.3.9.2 设备控制器模式下的控制传输

(1) 设置阶段

USBFS向USBFS的正常设置数据包发送ACK响应。USBFS在设置阶段运行如下：

在接收到新的设置数据包时，USBFS设置以下位：

- 将INTSTS0.VALID位设置为1
- 将DCPCTR.PID[1:0]位设置为NAK
- 将DCPCTR.CCPL位设置为0。

当USBFS在setup数据包之后接收到数据包时，它会将USB请求参数存储在USBREQ中，
USBVAL, USBINDX, and USBLENG.

在执行控制传输的响应处理之前，将VALID标志设置为0。当VALID位=1时，PID

= BUF cannot be set, and the data stage cannot be terminated.

Using the VALID bit function, the USBFS can suspend a request being processed when it receives a new USB request during a control transfer and return a response to the latest request.

In addition, the USBFS automatically detects the direction bit (bmRequestType bit [8]) and the request data length (wLength) in the received USB request. It distinguishes between control read transfers, control write transfers, and no-data control transfers, and it controls stage transitions. For an incorrect sequence, a sequence error occurs in the control transfer stage transition interrupt, and the interrupt is reported to the software. For a diagram of the stage control by the USBFS, see Figure 32.15.

(2) Data stage

The DCP must be used to execute data transfers for received USB requests. Before accessing the DCP FIFO buffer, specify the access direction in the CFIFOSEL.ISEL bit.

If the transfer data is larger than the size of the DCP FIFO buffer, execute the data transfer using the BRDY interrupt for control write transfers and the BEMP interrupt for control read transfers.

(3) Status stage

Control transfers are terminated by setting the DCPCTR.CCPL bit to 1 while the DCPCTR.PID[1:0] bits are set to BUF.

After this setting is made, the USBFS automatically executes the status stage based on the data transfer direction determined at the setup stage. The procedure is as follows:

- For control read transfers
  The USBFS receives a zero-length packet from the USB host and transmits an ACK response.
- For control write transfers and no-data control transfers
  The USBFS transmits a zero-length packet and receives an ACK response from the USB host.

(4) Control transfer auto response function

The USBFS automatically responds to a correct SET_ADDRESS request. If any of the following errors occurs in the SET_ADDRESS request, a response from the software is necessary.

- bmRequestType is not 00h: Any transfer other than a control write transfer
- wIndex is not 00h: Request error
- wLength is not 00h: Any transfer other than a no-data control transfer
- wValue is larger than 7Fh: Request error
- INTSTS0.DVSQ[2:0] are 011b (Configured state): Control transfer of a device state error.

For all requests other than the SET_ADDRESS request, a response is required from the corresponding software.

32.3.10 Bulk Transfers (Pipes 1 to 5)

The FIFO buffer usage (single/double buffer setting) is configurable for bulk transfers. The USBFS provides the following functions for bulk transfers:

- BRDY interrupt function (PIPECFG.BFRE bit), see section 32.3.3.1, (2) When SOFCFG.BRDYM = 0 and PIPECFG.BFRE = 1
- Transaction count function (PIPEnTRE.TRENB, TRCLR, and PIPEnTRN.TRNCNT[15:0] bits), see section 32.3.4.5, Transaction counter for pipes 1 to 5 in the receiving direction
- Response PID = NAK function (PIPECFG.SHTNAK bit), see section 32.3.4.8, Response PID = NAK function
- Auto response mode (PIPEnCTR.ATREPM bit), see section 32.3.4.9, Auto response mode.

32.3.11 Interrupt Transfers (Pipes 6 to 9)

In device controller mode, the USBFS performs interrupt transfers based on the timing dictated by the host controller.

In host controller mode, the software can set the timing for issuing tokens using the interval counter.

=BUF不能设置，数据阶段不能终止。

使用VALID位功能，USBFS可以在控制传输期间接收到新的USB请求时暂停正在处理的请求，并返回对最新请求的响应。

此外，USBFS会自动检测接收到的USB请求中的方向位（bmRequestTypebit[8]）和请求数据长度（wLength）。它区分控制读取传输、控制写入传输和无数据控制传输，并控制阶段转换。对于不正确的序列，在控制转移阶段转换中断中发生序列错误，并将中断报告给软件。有关USBFS的阶段控制图，请参见图32.15。

(2) 数据阶段

DCP必须用于执行接收到的USB请求的数据传输。在访问DCPFIFO缓冲区之前，请在CFIFOSEL.ISEL位中指定访问方向。

如果传输数据大于DCPFIFO缓冲区的大小，则使用控制写传输的BRDY中断和控制读传输的BEMP中断执行数据传输。

(3) 状态阶段

通过将DCPCTR.CCPL位设置为1而将DCPCTR.PID[1:0]位设置为BUF来终止控制传输。

完成此设置后，USBFS根据设置阶段确定的数据传输方向自动执行状态阶段。程序如下：

- 对于控制读取传输
  USBFS从USB主机接收零长度数据包并发送ACK响应。
- 用于控制写传输和无数据控制传输
  USBFS发送一个长度为零的数据包并接收来自USB主机的ACK响应。

(4) 控制转移自动响应功能

USBFS自动响应正确的SET_ADDRESS请求。如果出现以下任何错误
SET_ADDRESS请求，需要软件的响应。

- bmRequestType不是00h：控制写入传输以外的任何传输
- wIndex不是00h：请求错误
- wLength不是00h：除无数据控制传输之外的任何传输
- wValue大于7Fh：请求错误
- INTSTS0.DVSQ[2:0]为011b（已配置状态）：设备状态错误的控制传输。

对于除SET_ADDRESS请求之外的所有请求，都需要相应软件的响应。

32.3.10 批量传输（管道1到5）

FIFO缓冲区使用（单双缓冲区设置）可配置为批量传输。USBFS为批量传输提供以下功能：

- BRDY中断功能（PIPECFG.BFRE位），见第32.3.3.1节，(2)当SOFCFG.BRDYM=0且PIPECFG.BFRE = 1
- 事务计数函数（PIPEnTRE.TRENB、TRCLR和PIPEnTRN.TRNCNT[15:0]位），参见第32.3.4.5节，接收方向管道1到5的事务计数器
- 响应PID=NAK功能（PIPECFG.SHTNAK位），请参见第32.3.4.8节，响应PID=NAK功能
- 自动响应模式（PIPEnCTR.ATREPM位），请参见第32.3.4.9节，自动响应模式。

32.3.11 中断传输（管道6到9）

在设备控制器模式下，USBFS根据主机控制器规定的时序执行中断传输。

在主机控制器模式下，软件可以使用间隔计数器设置发布令牌的时间。

32.3.11.1 Interval counter for interrupt transfers in host controller mode

Specify the transaction interval for interrupt transfers in the PIPEPERI.IITV[2:0] bits. The USBFS issues interrupt transfer tokens based on this interval.

(1) Counter initialization

The USBFS initializes the interval counter under the following conditions:

- Power-on reset
  This initializes the IITV[2:0] bits.
- FIFO buffer initialization using the PIPEnCTR.ACLRM bit:
  This does not initialize the IITV[2:0] bits, but does initialize the count value. Setting the PIPEnCTR.ACLRM bit to 0 starts counting from the value set in IITV[2:0].

The interval counter is not initialized in the following case:

- USB bus reset or USB suspended
  The IITV[2:0] bits are not initialized. Setting 1 to the DVSTCTR0.UACT bit starts counting from the value saved before entering the USB bus reset state or USB suspend state.

(2) Operation when tokens cannot be transmitted or received even on token generation

No token is generated in the following cases even at token generation time. In these cases, the USBFS tries to execute the transaction in the next interval.

- When the PID is set to NAK or STALL
- When the FIFO buffer is full at token transmit time in the receiving (IN) direction
- When there is no data to be transmitted in the FIFO buffer at token transmit time in the transmitting (OUT) direction.

32.3.12 Isochronous Transfers (Pipes 1 and 2)

The USBFS provides the following functions for isochronous transfers:

- Notification of isochronous transfer error
- Interval counter specified in the PIPEPERI.IITV[2:0] bits
- Isochronous IN transfer data setup control (IDLY function)
- Isochronous IN transfer buffer flush function specified in the PIPEPERI.IFIS bit.

32.3.12.1 Error detection in isochronous transfers

The USBFS provides a function for detecting the errors described in this section, so that when errors occur in isochronous transfers, they can be controlled by software. Table 32.24 and Table 32.25 show the priority order for errors detected by the USBFS and the associated interrupts.

(a) PID errors

- The PID value of the received packet is invalid.

(b) CRC errors and bit stuffing errors

- A CRC error is found in a received packet or the bit stuffing is illegal.

(c) Maximum packet size exceeded

- The data size of the received packet exceeds the specified maximum packet size.

(d) Overrun and underrun errors

In host controller mode:

- The FIFO buffer is full at token transmit time in the IN (receiving) direction
- There is no data to be sent in the FIFO buffer at token transmit time in the OUT (transmitting) direction.

32.3.11.1 主机控制器模式下中断传输的间隔计数器

在PIPEPERI.IITV[2:0]位中指定中断传输的事务间隔。USBFS基于此间隔发出中断传输令牌。

(1) 计数器初始化

USBFS在以下条件下初始化间隔计数器：

- Power-on reset
  这将初始化IITV[2:0]位。
- 使用PIPEnCTR.ACLRM位初始化FIFO缓冲区：
  这不会初始化IITV[2:0]位，但会初始化计数值。将PIPEnCTR.ACLRM位设置为0从IITV[2:0]中设置的值开始计数。

在以下情况下不初始化间隔计数器：

- USB总线复位或USB挂起
  IITV[2:0]位未初始化。将DVSTCTR0.UACT位置1从进入USB总线复位状态或USB挂起状态之前保存的值开始计数。

(2) 即使在生成令牌时也无法发送或接收令牌时的操作

在以下情况下，即使在生成令牌时也不会生成令牌。在这些情况下，USBFS会尝试在下一个时间间隔执行事务。

- 当PID设置为NAK或STALL时
- 当FIFO缓冲区在接收(IN)方向的令牌传输时间已满时
- 在发送(OUT)方向的令牌发送时间，当FIFO缓冲区中没有要发送的数据时。

32.3.12 同步传输（管道1和2）

USBFS为同步传输提供以下功能：

- 同步传输错误通知
- 在PIPEPERI.IITV[2:0]位中指定的间隔计数器
- 同步IN传输数据设置控制（IDLY功能）
- 在PIPEPERI.IFIS位中指定的同步IN传输缓冲区刷新功能。

32.3.12.1 同步传输中的错误检测

USBFS提供了检测本节所述的错误的功能，以便在同步传输中发生错误时，可以通过软件进行控制。表32.24和表32.25显示了USBFS检测到的错误和相关中断的优先级顺序。

(a) PID错误

- 接收到的数据包的PID值无效。

(b) CRC错误和位填充错误

- 在收到的数据包中发现CRC错误或比特填充是非法的。

(c) 超出最大数据包大小

- 接收到的数据包的数据大小超过了指定的最大数据包大小。

(d) 溢出和欠载错误

在主机控制器模式下：

- FIFO缓冲区在IN（接收）方向的令牌发送时间已满
- 在OUT（发送）方向的令牌发送时，FIFO缓冲区中没有要发送的数据。

In device controller mode:

- There is no data to be sent in the FIFO buffer at token receive time in the IN (transmitting) direction
- The FIFO buffer is full at token receive time in the OUT (receiving) direction.

(e) Interval errors

In device controller mode, the following cases are treated as an interval error:

- Failure to receive an IN token in the interval frame during an isochronous IN transfer
- Failure to receive an OUT token in the interval frame during an isochronous OUT transfer.

Table 32.24 Error detection for token transmission and reception

Detection priority	Error	Generated interrupt and status
1	PID error	No interrupts are generated in either host or device controller mode (ignored as a corrupted packet)
2	CRC or bit stuffing error	No interrupts are generated in either host or device controller mode (ignored as a corrupted packet)
3	Overrun or underrun error	An NRDY interrupt is generated to set the FRMNUM.OVRN bit to 1 in both host and device controller modes. In device controller mode, a zero-length packet is transmitted in response to an IN token. No data packets are received in response to OUT token.
4	Interval error	An NRDY interrupt is generated in device controller mode. No interrupt is generated in host controller mode.

Table 32.25 Error detection for data packet reception

Detection priority	Error	Generated interrupt and status
1	PID error	No interrupts are generated (ignored as a corrupted packet)
2	CRC or bit stuffing error	An NRDY interrupt is generated and the FRMNUM.CRCE bit sets to 1 in both host and device controller modes
3	Maximum packet size exceeded error	A BEMP interrupt is generated and the PID[1:0] bits set to STALL in both host and device controller modes

32.3.12.2 DATA-PID

In device controller mode, the USBFS responds to a received PID as follows:

(1) IN direction

- DATA0: Transmitted as data packet PID
- DATA1: Not transmitted
- DATA2: Not transmitted
- mDATA: Not transmitted.

(2) OUT direction

- DATA0: Received normally as data packet PID
- DATA1: Received normally as data packet PID
- DATA2: Packets ignored
- mDATA: Packets ignored.

32.3.12.3 Interval counter

The isochronous transfer interval can be set in the PIPEPERI.IITV[2:0] bits. In device controller mode, the interval

在设备控制器模式下：

- 在IN（发送）方向的令牌接收时间，FIFO缓冲区中没有要发送的数据
- FIFO缓冲区在OUT（接收）方向上的令牌接收时间已满。

(e) 间隔错误

在设备控制器模式下，以下情况被视为间隔错误：

- 在同步IN传输期间未能在间隔帧中接收IN令牌
- 在同步OUT传输期间未能在间隔帧中接收OUT令牌。

Table 32.24 令牌发送和接收的错误检测

检测优先级	Error	产生的中断和状态
1	PID错误	在主机或设备控制器模式下都不会产生中断（被忽略为损坏的数据包）
2	CRC或位填充错误	在主机或设备控制器模式下都不会产生中断（被忽略为损坏的数据包）
3	溢出或欠载错误	在主机和设备控制器模式下，都会产生一个NRDY中断来将FRMNUM.OVRN位设置为1。在设备控制器模式下，发送一个零长度数据包以响应IN令牌。 没有接收到响应OUT令牌的数据包。
4	间隔误差	在设备控制器模式下会产生一个NRDY中断。在主机控制器模式下不产生中断。

Table 32.25 数据包接收错误检测

检测优先级	Error	产生的中断和状态
1	PID错误	不产生中断（作为损坏的数据包被忽略）
2	CRC或位填充错误	在主机和设备控制器模式下都会产生一个NRDY中断并且FRMNUM.CRCE位设置为1
3	超出最大数据包大小错误	在主机和设备控制器模式下都会产生BEMP中断并且PID[1:0]位设置为STALL

32.3.12.2 DATA-PID

在设备控制器模式下，USBFS响应接收到的PID如下：

(1) 在方向

- DATA0：作为数据包PID发送
- DATA1：未发送
- DATA2：未传输
- mDATA：未传输。

(2) 出方向

- DATA0：作为数据包PID正常接收
- DATA1：作为数据包PID正常接收
- DATA2：数据包被忽略
- mDATA：数据包被忽略。

32.3.12.3 间隔计数器

同步传输间隔可以在PIPEPERI.IITV[2:0]位中设置。在设备控制器模式下，间隔

counter enables the functions as shown in Table 32.26. In host controller mode, the USBFS generates the token issuance timing, and the interval counter operation is the same as that for interrupt transfers.

Table 32.26 Interval counter functions in device controller mode

Transfer direction	Function	Conditions for detection
IN	Transmit buffer flush	Failure to receive an IN token successfully in the interval frame during an isochronous IN transfer.
OUT	Notification of no reception of token	Failure to receive an OUT token successfully in the interval frame during an isochronous OUT transfer.

The interval count is performed when an SOF is received or for interpolated SOFs, so the isochronism can be maintained even if an SOF is corrupt. The frame interval can be set to 2^{IITV} frames.

(1) Counter initialization in device controller mode

The USBFS initializes the interval counter under the following conditions:

- Power-on reset
  This initializes the PIPEPERI.IITV[2:0] bits.
- FIFO buffer initialization using the ACLRM bit
  This does not initialize the IITV[2:0] bits, but does initialize the count value.

After the interval counter is initialized, the interval count starts under one of the following conditions when a packet is transferred successfully:

- An SOF is received after data is transmitted in response to an IN token when PID = BUF
- An SOF is received after data is received in response to an OUT token when PID = BUF.

The interval counter is not initialized in the following conditions:

- When the PID[1:0] bits are set to NAK or STALL
  This does not stop the interval timer. The USBFS attempts the transaction in the next interval.
- When the USB bus is reset or USBFS is suspended
  This does not initialize the IITV[2:0] bits. When an SOF is received, the interval counter starts counting from the value set before SOF was received.

(2) Interval counting and transfer control in host controller mode

The USBFS controls the interval between token issuance operations based on the PIPEPERI.IITV[2:0] bit settings. Specifically, the USBFS issues a token for a selected pipe once every 2^{IITV} frames.

The USBFS starts counting the token issuance interval at the frame following the frame in which the PID[1:0] bits are set to BUF by software.

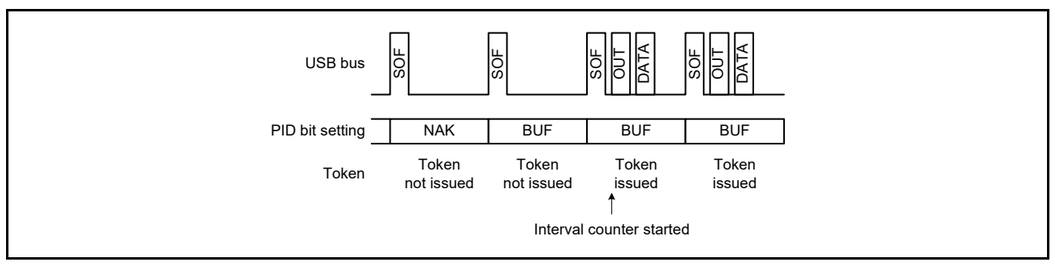


Figure 32.16 Token issuance when IITV = 0

计数器启用表32.26中所示的功能。在主机控制器模式下，USBFS产生令牌发布时序，间隔计数器操作与中断传输相同。

Table 32.26 设备控制器模式下的间隔计数器功能

转移方向	Function	检测条件
IN	发送缓冲区刷新	在同步IN传输期间未能在间隔帧中成功接收IN令牌。
OUT	未收到令牌的通知	在等时期间未能在间隔帧中成功接收OUT令牌 输出传输。

间隔计数在接收到SOF时执行或对插值SOF执行，因此即使SOF损坏也可以保持等时性。帧间隔可以设置为2个IITV帧。

(1) 设备控制器模式下的计数器初始化

USBFS在以下条件下初始化间隔计数器：

- Power-on reset
  这将初始化PIPEPERI.IITV[2:0]位。
- 使用ACLRM位初始化FIFO缓冲区
  这不会初始化IITV[2:0]位，但会初始化计数值。

间隔计数器初始化后，当数据包传输成功时，间隔计数在以下条件之一开始：

- 当PID=BUF时，响应IN令牌传输数据后收到SOF
- 当PID=BUF时，接收到响应于OUT令牌的数据后接收到SOF。

间隔计数器在以下情况下不会初始化：

- 当PID[1:0]位设置为NAK或STALL
  这不会停止间隔计时器。USBFS在下一个间隔尝试事务。
- 当USB总线复位或USBFS暂停时
  这不会初始化IITV[2:0]位。当接收到SOF时，间隔计数器从接收到SOF之前设置的值开始计数。

(2) 主机控制器模式下的间隔计数和传输控制

USBFS根据PIPEPERI.IITV[2:0]位设置控制令牌发布操作之间的间隔。
具体来说，USBFS每2个IITV帧为所选管道发布一次令牌。

USBFS在PID[1:0]位被软件设置为BUF的帧之后的帧开始计算令牌发布间隔。

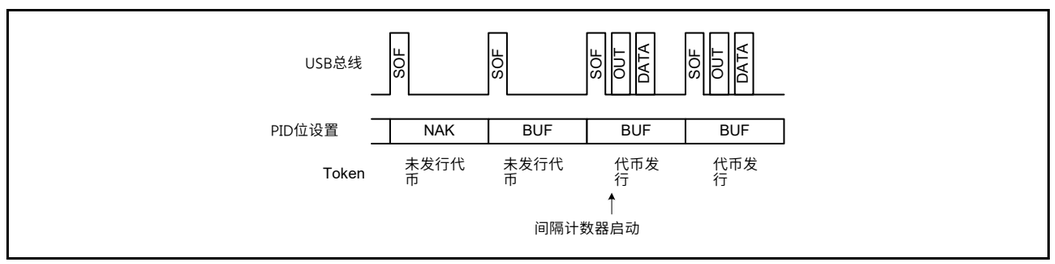


Figure 32.16 IITV=0时的代币发行

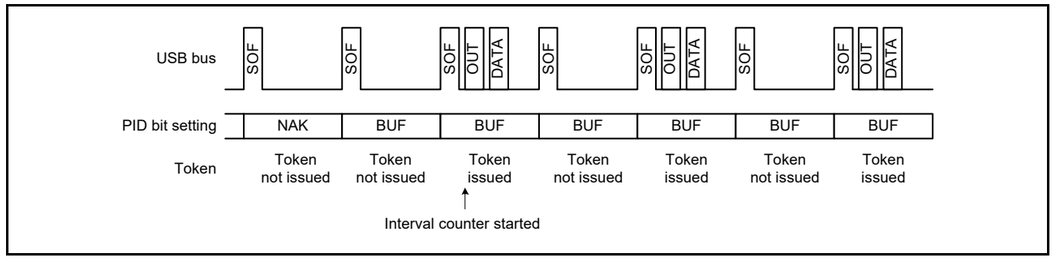


Figure 32.17 Token issuance when IITV = 1

When the selected pipe is set for isochronous transfers, the USBFS performs the following operation in addition to controlling the token issuance interval. The USBFS issues a token even when the NRDY interrupt generation condition is satisfied.

(a) When the selected pipe is for isochronous IN transfers

The USBFS generates an NRDY interrupt when the USBFS issues an IN token but does not successfully receive a packet from a peripheral device (no response or packet error).

The USBFS sets the FRMNUM.OVRN bit to 1, generating an NRDY interrupt, when the time to issue an IN token occurs while the USBFS cannot receive data because the FIFO buffer is full, because the CPU or DMAC/DTC is too slow in reading data from the FIFO buffer.

(b) When the selected pipe is for isochronous OUT transfers

The USBFS sets the OVRN bit to 1, generating an NRDY interrupt and transmitting a zero-length packet, when the time to issue an OUT token comes while there is no data to be transmitted in the FIFO buffer, or because the CPU or DMAC/DTC is too slow in writing data to the FIFO buffer.

The token issuance interval is reset on any of the following conditions:

- When the USBFS is reset through a reset pin
  This initializes the IITV[2:0] bits.
- When the PIPEnCTR.ACLRM bit is set to 1 by software.

(3) Interval counting and transfer control in device controller mode

(a) When the selected pipe is for isochronous OUT transfers

The USBFS generates an NRDY interrupt when it fails to receive a data packet within the interval set in the PIPEPERI.IITV[2:0] bits.

The USBFS also generates an NRDY interrupt when it fails to receive data because of a CRC error or other errors contained in the data packet or because the FIFO buffer is full.

The NRDY interrupt is generated on SOF packet reception. Even if the SOF packet is corrupted, internal interpolation allows the interrupt to be generated when the SOF packet is received. However, when the IITV bits are set to a value other than 0, the USBFS generates an NRDY interrupt on receiving an SOF packet for every interval after interval counting starts.

When the PID[1:0] bits are set to NAK by software after starting the interval timer, the USBFS does not generate an NRDY interrupt on receiving an SOF packet.

The timing for starting interval counting depend on the IITV[2:0] setting as follows:

- When the IITV[2:0] bits = 0:
  Interval counting starts at the next frame after the software changes the PID[1:0] bits of the selected pipe to BUF.
- When the IITV[2:0] bits ≠ 0:
  Interval counting starts on completion of successful reception of the first data packet after the PID[1:0] bits for the selected pipe are changed to BUF.

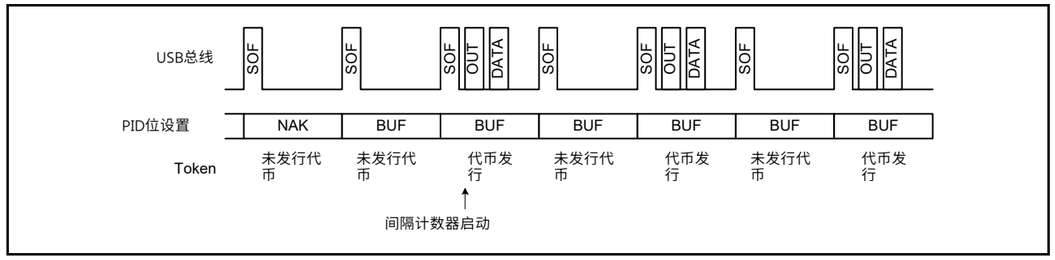


Figure 32.17 IITV=1时的代币发行

当所选管道设置为同步传输时，USBFS除了控制令牌发布间隔外，还执行以下操作。即使满足NRDY中断生成条件，USBFS也会发出令牌。

(a) 当所选管道用于同步IN传输时

当USBFS发出IN令牌但未成功接收到来自外围设备的数据包（无响应或数据包错误）时，USBFS会生成NRDY中断。

USBFS将FRMNUM.OVRN位设置为1，产生一个NRDY中断，此时发生发出IN令牌的时间，而USBFS无法接收数据，因为FIFO缓冲区已满，因为CPU或DMACDTC读取数据太慢从FIFO缓冲区。

(b) 当所选管道用于同步OUT传输时

USBFS将OVRN位设置为1，产生一个NRDY中断并发送一个长度为零的数据包，当发出OUT令牌的时间到来而FIFO缓冲区中没有要发送的数据时，或者因为CPU或DMACDTC将数据写入FIFO缓冲区太慢。

令牌发行间隔在以下任何条件下重置：

- 当USBFS通过复位引脚复位时
  这将初始化IITV[2:0]位。
- 当PIPEnCTR.ACLRM位由软件设置为1时。

(3) 设备控制器模式下的间隔计数和传输控制

(a) 当所选管道用于同步OUT传输时

当USBFS在设置的时间间隔内没有接收到数据包时，会产生一个NRDY中断。
PIPEPERI.IITV[2:0] bits.

当由于数据包中包含的CRC错误或其他错误或FIFO缓冲区已满而无法接收数据时，USBFS也会产生NRDY中断。

NRDY中断在SOF数据包接收时产生。即使SOF数据包损坏，内部插值也允许在接收到SOF数据包时产生中断。但是，当IITV位设置为0以外的值时，USBFS会在间隔计数开始后的每个间隔接收到SOF数据包时产生NRDY中断。

当PID[1:0]位在启动间隔定时器后由软件设置为NAK时，USBFS不会产生
接收到SOF数据包时的NRDY中断。

开始间隔计数的时间取决于IITV[2:0]设置，如下所示：

- 当IITV[2:0]位=0时：
  软件将所选管道的PID[1:0]位更改为BUF后，间隔计数从下一帧开始。
- 当IITV[2:0]位≠0时：
  在所选管道的PID[1:0]位更改为BUF后，成功接收第一个数据包后，间隔计数开始。

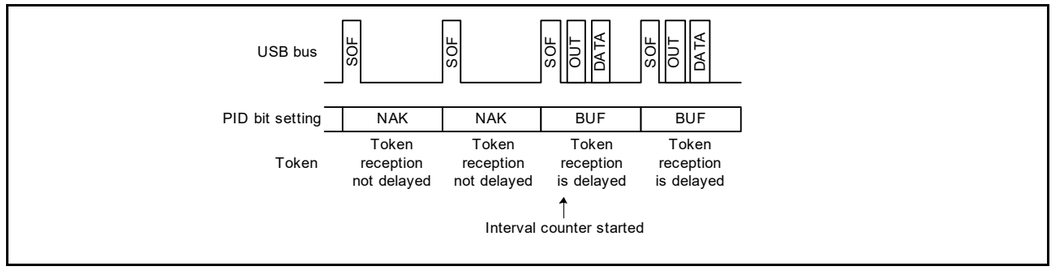


Figure 32.18 Relationship between frames and expected token reception when IITV[2:0] = 0

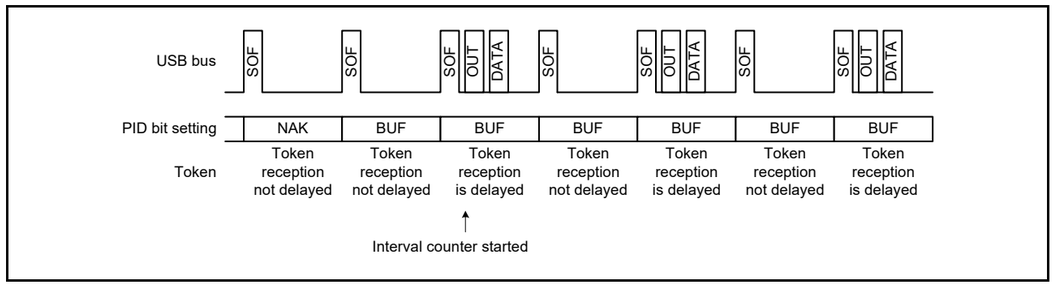


Figure 32.19 Relationship between frames and expected token reception when IITV[2:0] ≠ 0

(b) When the selected pipe is for isochronous IN transfers

The PIPEPERI.IFIS bit must be 1 for this use case. When IFIS = 0, the USBFS transmits a data packet in response to a received IN token regardless of the PIPEPERI.IITV[2:0] setting.

When IFIS is 1 and there is data to be transmitted in the FIFO buffer, the USBFS clears the FIFO buffer when it fails to receive an IN token in the frame at the interval set in the IITV[2:0] bits.

The USBFS also clears the FIFO buffer when it fails to receive an IN token successfully because of a bus error, such as a CRC error, contained in the IN token.

The FIFO buffer is cleared on SOF packet reception. Even if the SOF packet is corrupted, the internal interpolation allows the FIFO buffer to be cleared when the SOF packet is received.

The timing to start interval counting depends on the IITV[2:0] setting, as with OUT transfers.

The interval is counted on any of the following conditions in device controller mode:

- When a hardware reset is applied to the USBFS (which also sets the IITV[2:0] bits to 000b)
- When the PIPEnCTR.ACLRM bit is set to 1 by software
- When the USBFS detects a USB bus reset.

(4) Transmit data setup for isochronous transfers in device controller mode

With isochronous data transmission using the USBFS in device controller mode, after data is written to the FIFO buffer, a data packet can be transmitted in the first frame after the SOF packet is detected. This isochronous transfer transmit data setup function can identify the frame that started transmission.

When the double buffering is used, transmission is only enabled for the buffer where data writing was completed first, even after the data write to both buffers is complete. Accordingly, even if multiple IN tokens are received, only the one packet of FIFO buffer data is transmitted.

When the FIFO buffer is ready to transmit data when an IN token is received, the data is transferred and a normal response is returned. However, if the FIFO buffer cannot transmit data, a zero-length packet is transmitted and an underrun error occurs.

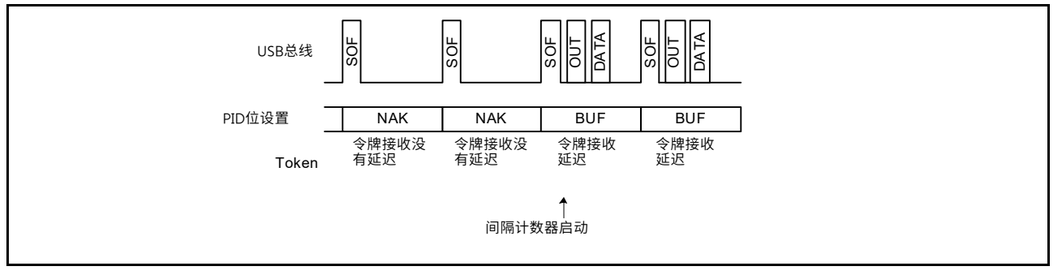


Figure 32.18 IITV[2:0]=0时帧与预期令牌接收之间的关系

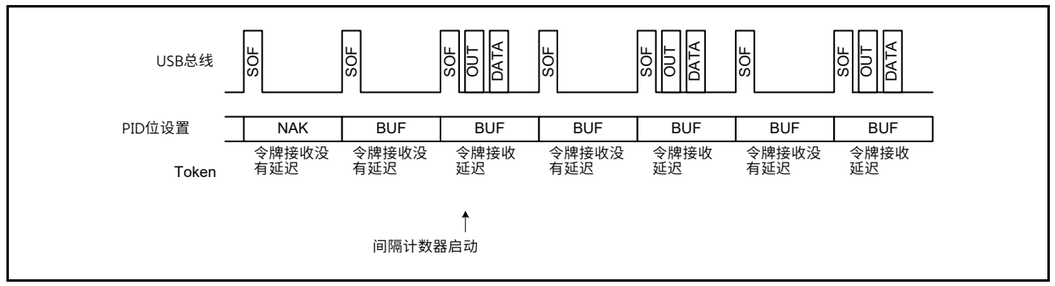


Figure 32.19 IITV[2:0]≠0时帧与预期令牌接收的关系

(b) 当所选管道用于同步IN传输时

对于此用例，PIPEPERI.IFIS位必须为1。当IFIS=0时，无论PIPEPERI.IITV[2:0]设置如何，USBFS都会发送一个数据包以响应接收到的IN令牌。

当IFIS为1且FIFO缓冲区中有数据要发送时，如果USBFS在IITV[2:0]位设置的时间间隔内未能接收到帧中的IN令牌，则清除FIFO缓冲区。

当USBFS由于总线错误（例如
CRC错误，包含在IN令牌中。

FIFO缓冲区在SOF数据包接收时被清除。即使SOF数据包损坏，内部插值也允许在接收到SOF数据包时清除FIFO缓冲区。

开始间隔计数的时间取决于IITV[2:0]设置，与OUT传输一样。

在设备控制器模式下，根据以下任何条件计算间隔：

- 当对USBFS应用硬件复位时（也将IITV[2:0]位设置为000b）
- 当PIPEnCTR.ACLRM位由软件设置为1时
- 当USBFS检测到USB总线复位时。

(4) 设备控制器模式下同步传输的传输数据设置

在设备控制器模式下使用USBFS进行同步数据传输，数据写入FIFO缓冲区后，可在检测到SOF包后的第一帧发送数据包。此同步传输传输数据设置功能可以识别开始传输的帧。

使用双缓冲时，仅对先完成数据写入的缓冲区启用传输，即使在两个缓冲区的数据写入完成后也是如此。因此，即使接收到多个IN令牌，也仅发送一包FIFO缓冲器数据。

当接收到IN令牌时，当FIFO缓冲区准备好传输数据时，将传输数据并返回正常响应。但是，如果FIFO缓冲区无法传输数据，则会传输零长度数据包并发生欠载错误。

Figure 32.20 shows an example transmission using the isochronous transfer transmission data setup function when IITV = 0 (every frame) is set.

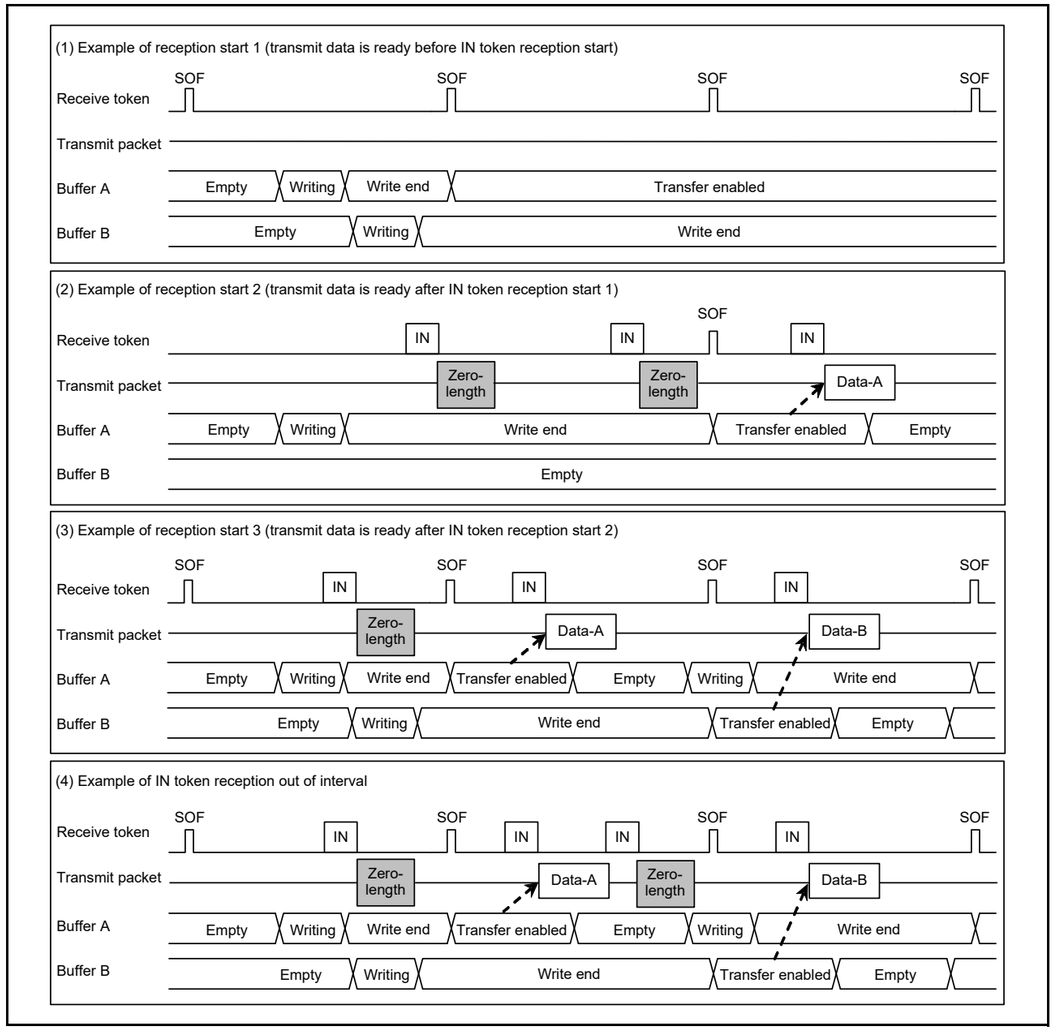


Figure 32.20 Example data setup operation

(5) Transmit buffer flush for isochronous transfers in device controller mode

In device controller mode during isochronous data transmission, if the USBFS receives an SOF packet for the next frame without receiving an IN token in the interval frame, it operates as if the IN token is corrupt and clears the buffer that is enabled for transmission, putting that buffer in the writing enabled state.

When double buffering is used and writing to both buffers is complete, the cleared FIFO buffer is assumed to be the one where the data was transmitted in the interval frame, and transmission is enabled for the FIFO buffer that was not cleared on SOF packet reception.

The timing of the buffer flush function depends on the PIPEPERI.IITV[2:0] setting as follows:

- When IITV = 0:
  The buffer flush operation starts from the first frame after the pipe is enabled.

图32.20显示了在设置IITV=0（每帧）时使用同步传输传输数据设置功能的示例传输。

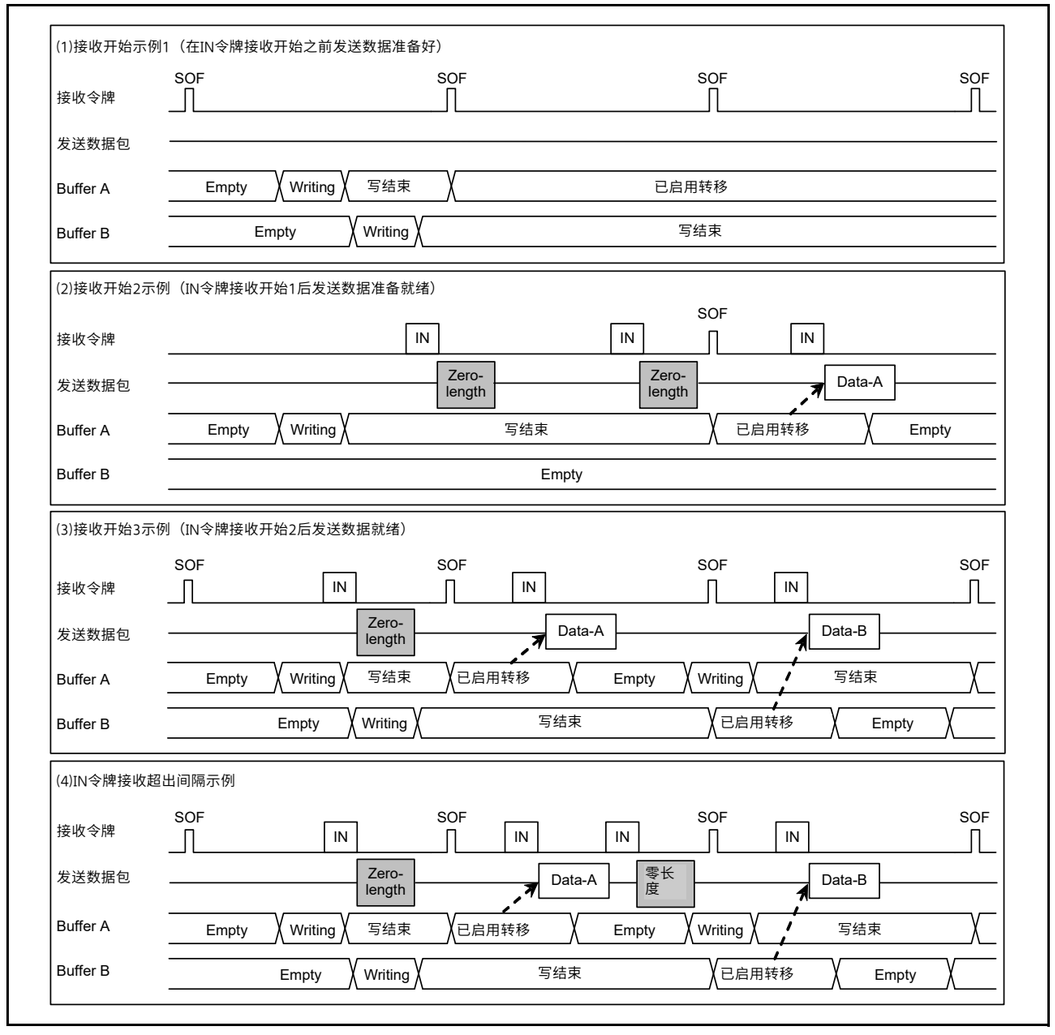


Figure 32.20 示例数据设置操作

(5) 设备控制器模式下同步传输的传输缓冲区刷新

在同步数据传输期间的设备控制器模式下，如果USBFS接收到下一帧的SOF数据包，而在间隔帧中没有接收到IN令牌，则它会像IN令牌损坏一样操作并清除启用传输的缓冲区，将该缓冲区处于写入启用状态。

当使用双缓冲并完成对两个缓冲区的写入时，已清除的FIFO缓冲区被假定为在间隔帧中传输数据的缓冲区，并为接收SOF数据包时未清除的FIFO缓冲区启用传输。

缓冲区刷新功能的时间取决于PIPEPERI.IITV[2:0]设置，如下所示：

- When IITV = 0:
  缓冲区刷新操作从启用管道后的第一帧开始。

- When IITV ≠ 0:
  The buffer flush operation starts after the first normal transaction.

Figure 32.21 shows an example buffer flush. When an unanticipated token is received before the interval frame, the USBFS sends the write data or a zero-length packet as an underrun error, depending on the data setup status.

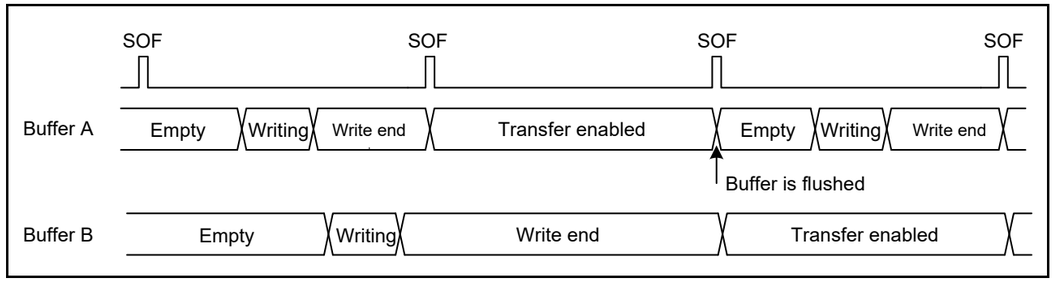


Figure 32.21 Example buffer flush operation

Figure 32.22 shows an example interval error occurrence. There are five types of interval errors, as shown in the figure. An interval error occurs at timing ①, and the buffer flush function is activated.

If an interval error occurs during an IN transfer, the buffer flush function is activated. If it occurs during an OUT transfer, an NRDY interrupt is generated. Use the FRMNUM.OVRN bit to distinguish between this and NRDY interrupts triggered by received packet errors and overrun errors.

For tokens that are shaded in the figure, responses are returned based on the FIFO buffer status.

- IN direction:
  - If the buffer is ready to transfer data, the data is transferred and a normal response is returned
  - If the buffer is not ready to transfer data, a zero-length packet is transmitted and an underrun error occurs.
- OUT direction:
  - If the buffer is ready to receive data, the data is received and a normal response is returned
  - If the buffer is not ready to receive data, the received data is discarded and an overrun error occurs.

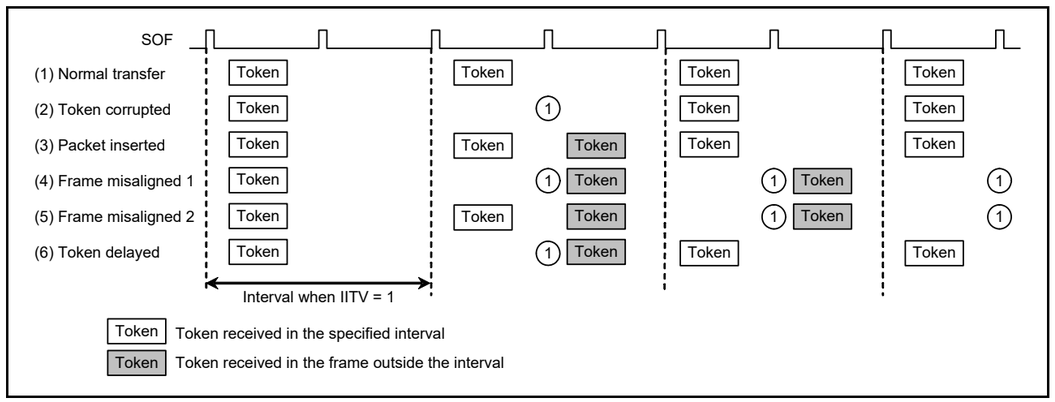


Figure 32.22 Example interval error occurrence when IITV = 1

32.3.13 SOF Interpolation Function

In device controller mode, if packet reception is disabled at intervals of 1 ms because the SOF packet is corrupted or missing, the USBFS interpolates the SOF. SOF interpolation begins when the USBE and SCKE bits in SYSCFG are set to 1 and an SOF packet is received.

- When IITV ≠ 0:
  缓冲区刷新操作在第一个正常事务之后开始。

图32.21显示了一个示例缓冲区刷新。当在间隔帧之前收到未预料到的令牌时，USBFS根据数据设置状态将写入数据或零长度数据包作为欠载错误发送。

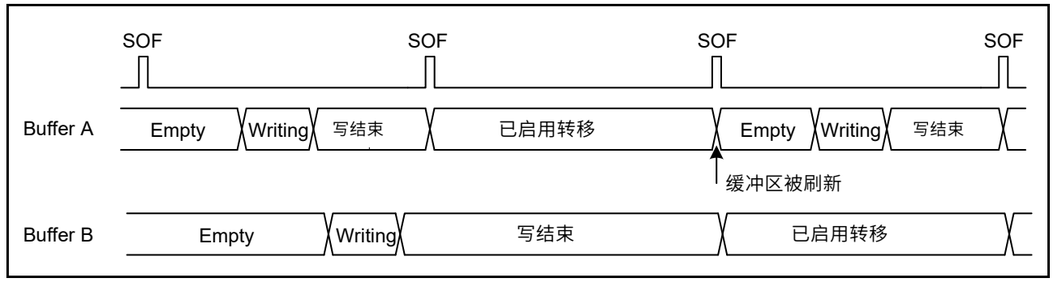


Figure 32.21 缓冲区刷新操作示例

图32.22显示了一个发生间隔错误的示例。如图所示，有五种区间误差。
定时出现间隔错误 ① 并且缓冲区刷新功能被激活。

如果在IN传输期间发生间隔错误，则会激活缓冲区刷新功能。如果它发生在OUT传输期间，则会产生NRDY中断。使用FRMNUM.OVRN位来区分此中断和由接收数据包错误和溢出错误触发的NRDY中断。

对于图中带阴影的令牌，根据FIFO缓冲区状态返回响应。

- IN direction:
  - 如果缓冲区准备好传输数据，则传输数据并返回正常响应
  - 如果缓冲区尚未准备好传输数据，则会传输零长度数据包并发生欠载错误。
- OUT direction:
  - 如果缓冲区准备好接收数据，则接收数据并返回正常响应
  - 如果缓冲区没有准备好接收数据，则丢弃接收到的数据并发生溢出错误。

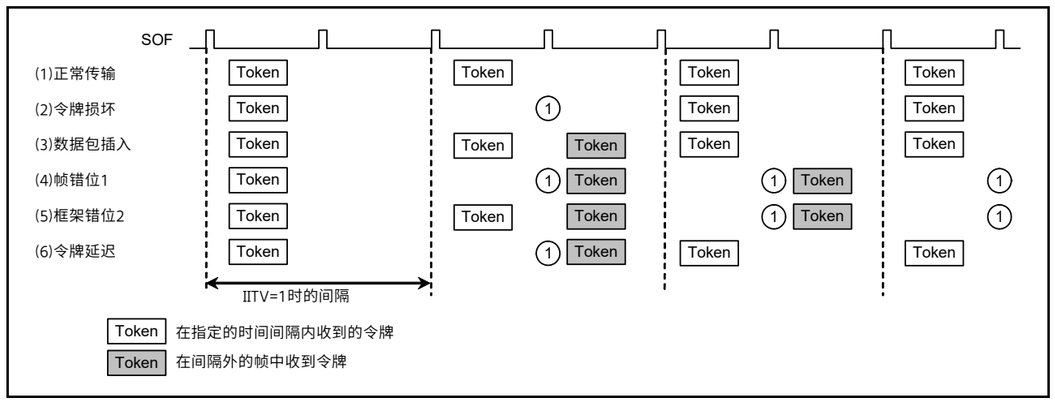


Figure 32.22 IITV=1时发生的示例间隔错误

32.3.13 SOF插值函数

在设备控制器模式下，如果由于SOF数据包损坏或丢失而每隔1ms禁用数据包接收，则USBFS会内插SOF。当SYSCFG中的USBE和SCKE位设置为1并且接收到SOF数据包时，SOF内插开始。

The interpolation function is initialized under the following conditions:

- MCU reset
- USB bus reset
- Suspend state detection.

The SOF interpolation operates as follows:

- The interpolation function is not activated until an SOF packet is received.
- When the first SOF packet is received, interpolation is performed by counting 1 ms on the 48-MHz internal clock
- When the second and subsequent SOF packets are received, interpolation is performed at the previous reception interval
- Interpolation is not performed in the Suspend state or on reception of a USB bus reset.

The USBFS supports the following functions controlled by SOF packet reception. These functions operate normally with SOF interpolation if the SOF packet is missing:

- Updating of the frame number
- SOFR interrupt timing
- Isochronous transfer interval count.

If an SOF packet is missing during full-speed operation, the FRMNUM.FRNM[10:0] bits are not updated.

32.3.14 Pipe Schedule

32.3.14.1 Conditions for generating transactions

In host controller mode and when the DVSTCTR0.UACT bit is set to 1, the USBFS generates transactions under the conditions shown in Table 32.27.

Table 32.27 Conditions for generating transactions

	Conditions for generation				
Transaction	**DIR**	**PID**	**IITV0**	**Buffer state**	**SUREQ**
Setup	—*1	—*1	—*1	—*1	1 setting
Control transfer data stage, status stage, bulk transfer	IN	BUF	Invalid	Receive area exists	—*1
	OUT	BUF	Invalid	Transmit data exists	—*1
Interrupt transfer	IN	BUF	Valid	Receive area exists	—*1
	OUT	BUF	Valid	Transmit data exists	—*1
Isochronous transfer	IN	BUF	Valid	*2	—*1
	OUT	BUF	Valid	*3	—*1

Note 1. An em dash (—) in the table indicates that the condition is unrelated to the generating of tokens. “Valid” indicates that, for interrupt transfers and isochronous transfers, a transaction is generated only in transfer frames that are based on the interval counter. “Invalid” indicates that a transaction is generated regardless of the interval counter.

Note 2. This indicates that a transaction is generated regardless of whether there is a receive area. If there is no receive area, however, the received data is discarded.

Note 3. This indicates that a transaction is generated regardless of whether there is any data to be transmitted. If there is no data to be transmitted, however, a zero-length packet is transmitted.

插值函数在以下条件下初始化：

- MCU reset
- USB总线复位
- 暂停状态检测。

SOF插值操作如下：

- 在接收到SOF数据包之前，不会激活插值功能。
- 当接收到第一个SOF数据包时，通过在48-MHz内部时钟上计数1ms来执行插值
- 当接收到第二个和随后的SOF数据包时，以先前的接收间隔执行插值
- 在挂起状态或接收到USB总线复位时不执行插值。

USBFS支持以下由SOF数据包接收控制的功能。这些功能正常运行
如果SOF数据包丢失，则SOF插值：

- 更新帧号
- SOFR中断时序
- 同步传输间隔计数。

如果在全速运行期间丢失SOF数据包，则不会更新FRMNUM.FRNM[10:0]位。

32.3.14 管道计划

32.3.14.1 产生交易的条件

在主机控制器模式下，当DVSTCTR0.UACT位设置为1时，USBFS在表32.27所示的条件下生成事务。

Table 32.27 产生交易的条件

	生成条件				
Transaction	**DIR**	**PID**	**IITV0**	**缓冲状态**	**SUREQ**
Setup	—*1	—*1	—*1	—*1	1 setting
控制传输数据阶段、状态阶段、批量传输	IN	BUF	Invalid	接收区存在	—*1
	OUT	BUF	Invalid	传输数据存在	—*1
中断传输	IN	BUF	Valid	接收区存在	—*1
	OUT	BUF	Valid	传输数据存在	—*1
Isochronous transfer	IN	BUF	Valid	*2	—*1
	OUT	BUF	Valid	*3	—*1

Note 1. 表中的破折号(—)表示该条件与令牌的生成无关。“有效”表示，对于中断传输和同步传输，事务仅在基于间隔计数器的传输帧中生成。“无效”表示无论间隔计数器如何都生成事务。

Note 2. 这表示不管是否有接收区域，都会产生一个事务。但是，如果没有接收区域，则丢弃接收到的数据。

Note 3. 这表明无论是否有任何数据要传输，都会生成一个事务。然而，如果没有要传输的数据，则传输零长度数据包。

32.3.14.2 Transfer schedule

This section describes the transfer scheduling within a frame of the USBFS. After the USBFS sends an SOF, the transfer is carried out in the following sequence:

1. Execution of periodic transfers:
   A pipe is searched for in the order of pipe 1 → pipe 2 → pipe 6 → pipe 7 → pipe 8 → pipe 9, and then if there is a pipe for which an isochronous or interrupt transfer transaction can be generated, the transaction is generated.
2. Setup transactions for control transfers:
   The DCP is checked, and if a setup transaction is possible, it is sent.
3. Execution of bulk transfers, control transfer data stages, and control transfer status stages:
   A pipe is searched for in the order of DCP → pipe 1 → pipe 2 → pipe 3 → pipe 4 → pipe 5, and then if there is a pipe for which a transaction for a bulk transfer, a control transfer data stage, or a control transfer status stage can be generated, the transaction is generated.
   When a transaction is generated, processing moves to the next pipe transaction regardless of whether the response from the peripheral device is ACK or NAK. If there is time for transfer within the frame, step 3 is repeated.

32.3.14.3 Enabling USB communication

Setting the DVSTCTR0.UACT bit to 1 initiates an SOF transmission, and transaction generation is enabled. Setting the UACT bit to 0 stops SOF transmission and the Suspend state is invoked. If the UACT setting is changed from 1 to 0, processing stops after the next SOF is sent.

32.4 Usage Notes

32.4.1 Settings for the Module-Stop State

USBFS operation can be disabled or enabled using Module Stop Control Register B (MSTPCRB). The USBFS is initially stopped after reset. Releasing the module-stop state enables access to the registers. For details, see section 11, Low Power Modes.

32.4.2 Clearing the Interrupt Status Register on Exiting Software Standby Mode

Because the input buffer is always enabled in Software Standby mode, an unexpected interrupt might occur under the following conditions:

- When the interrupt is enabled in Normal mode
- When the interrupt is disabled in Software Standby mode
- When the input level of the pin that cancels software standby is changed in Software Standby mode.

These conditions might cause the associated interrupt flag in the Interrupt Status Register to set unexpectedly. After the MCU exits the Software Standby mode, the unexpected interrupt might be sent to the interrupt controller. To avoid this, always clear the INTSTS0 and INTSTS1 registers in the canceling sequence.

32.4.3 Clearing the Interrupt Status Register after Setting Up the Port Function

The input buffer is disabled before the PmnPFS.PSEL and PmnPFS.PMR port is set up, so the internal signal is fixed high or low. The input buffer is enabled after the port is set so that the external pin state is propagated to the MCU. An unexpected interrupt might occur at this time, causing the VBINT and OVRCR bits in INTSTS0 and INTSTS1, or other interrupt status flags to set to 1. To avoid a malfunction, always clear the INTSTS0 and INTSTS1 registers after setting up the port.

32.3.14.2 转移时间表

本节介绍USBFS帧内的传输调度。USBFS发送SOF后，按以下顺序进行传输：

1. 执行定期转账：
   按照管道1 管道2 管道6 管道7 管道8 管道9的顺序搜索管道，然后如果存在可以生成等时或中断传输事务的管道，则生成事务.
2. 为控制转移设置交易：
   DCP被检查，如果设置事务是可能的，它被发送。
3. 批量传输、控制传输数据阶段和控制传输状态阶段的执行：
   管道按DCP 管道1 管道2 管道3 管道4 管道5的顺序搜索，然后如果存在要进行批量传输的事务、控制传输数据阶段或可以生成控制转移状态阶段，生成事务。生成事务时，无论来自外围设备的响应是ACK还是NAK，处理都会转移到下一个管道事务。如果帧内有时间进行传输，则重复步骤3。

32.3.14.3 启用USB通信

将DVSTCR0.UACT位设置为1启动SOF传输，并启用事务生成。设置UACT位为0停止SOF传输并调用暂停状态。如果UACT设置从1更改为0，则在发送下一个SOF后处理停止。

32.4 使用说明

32.4.1 模块停止状态的设置

可以使用模块停止控制寄存器B(MSTPCRB)禁用或启用USBFS操作。USBFS在复位后最初停止。释放模块停止状态可以访问寄存器。有关详细信息，请参阅第11节，低功耗模式。

32.4.2 退出软件待机模式时清除中断状态寄存器

由于在软件待机模式下始终启用输入缓冲区，因此在以下情况下可能会发生意外中断：

- 在正常模式下启用中断时
- 在软件待机模式下禁用中断时
- 当取消软件待机的引脚的输入电平在软件待机模式下发生变化时。

这些情况可能会导致中断状态寄存器中的相关中断标志意外设置。MCU退出软件待机模式后，可能会向中断控制器发送意外中断。为避免这种情况，请始终在取消序列中清除INTSTS0和INTSTS1寄存器。

32.4.3 设置端口功能后清除中断状态寄存器

在设置PmnPFS.PSEL和PmnPFS.PMR端口之前，输入缓冲器被禁用，因此内部信号固定为高电平或低电平。设置端口后启用输入缓冲器，以便将外部引脚状态传播到MCU。此时可能会发生意外中断，导致INTSTS0和INTSTS1中的VBINT和OVRCR位或其他中断状态标志设置为1。为避免故障，请在设置端口后始终清除INTSTS0和INTSTS1寄存器。

33. USB 2.0 High-Speed Module (USBHS)

33.1 Overview

The MCU provides a USB 2.0 High-Speed Module (USBHS) that operates as a host or a device controller compliant with the Universal Serial Bus (USB) Specification revision 2.0. The host controller supports USB 2.0 high-speed, full-speed, and low-speed transfers, and the device controller supports USB 2.0 high-speed and full-speed transfers. The USBHS has an internal USB transceiver and supports all of the transfer types defined in the USB 2.0 specification.

The USBHS has FIFO buffer for data transfers, providing a maximum of 10 pipes. Any endpoint number can be assigned to pipes 1 to 9, based on the peripheral devices or the communication requirements for your system.

Table 33.1 lists the USBHS specifications, Figure 33.1 shows a block diagram, and Table 33.2 lists the I/O pins.

Table 33.1 USBHS specifications

Parameter	Specifications
Features	• USB Device Controller (UDC) and USB 2.0 transceiver supporting host controller, device controller, and On-The-Go (OTG) functions • Software can switch between host and device controller modes.
	Host controller features: • High-speed transfer (480 Mbps), full-speed transfer (12 Mbps), and low-speed transfer (1.5 Mbps) • Automatic scheduling for SOF and packet transmissions • Programmable intervals for isochronous and interrupt transfers • Communications with multiple peripheral devices connected through a single hub.
	Device controller features: • High-speed transfer (480 Mbps) and full-speed transfer (12 Mbps) • Control transfer stage control function • Device state control function • Auto response function for SET_ADDRESS request • SOF complementation.
Supported transfer types	• Control transfer • Bulk transfer • Interrupt transfer • Isochronous transfer.
Pipe configuration	• FIFO buffer of up to 8.5 KB for USB communications • Up to 10 pipes selectable, including the default control pipe • Programmable pipe configurations • Pipes 1 to 9 assignable to any endpoint number.
	Transfer conditions specifiable for each pipe: • Pipe 0: Control transfer with 64-byte single buffer • Pipes 1 and 2: Bulk isochronous transfer continuous transfer mode with programmable buffer size up to 2 KB and optional double buffer • Pipes 3 to 5: Bulk transfer continuous transfer mode with programmable buffer size up to 2 KB and optional double buffer • Pipes 6 to 9: Interrupt transfer with 64-byte single buffer.
Other features	• Force-end transfer function using transaction count • Function that changes the BRDY interrupt event notification timing • Automatic clearing of the FIFO buffer after data for the pipe specified in the DnFIFO port (n = 0, 1) is read • NAK setting function for response PID generated on transfer end • On-chip pull-up and pull-down resistors for D+ and D- • Support for Link Power Management (LPM) ECN, including a new Sleep state (the L1 state) • Compliance with Battery Charging Class Specification Revision 1.2 • For power reduction, selectable classic-only mode (CL-only mode) in which operation is only USB 1.1-compliant

33. USB2.0高速模块(USBHS)

33.1 Overview

MCU提供USB2.0高速模块(USBHS)，可作为主机或设备控制器运行，符合通用串行总线(USB)规范2.0版。主机控制器支持USB2.0高速、全速和低速传输，设备控制器支持USB2.0高速和全速传输。USBHS具有内部USB收发器，并支持USB2.0规范中定义的所有传输类型。

USBHS具有用于数据传输的FIFO缓冲区，最多提供10个管道。根据外围设备或系统的通信要求，可以将任何端点编号分配给管道1到9。

表33.1列出了USBHS规范，图33.1显示了框图，表33.2列出了IO引脚。

Table 33.1 USBHS specifications

Parameter	Specifications
Features	USB设备控制器(UDC)和USB2.0收发器支持主机控制器、设备控制器和On-The-Go(OTG)功能 软件可以在主机和设备控制器模式之间切换。
	主机控制器特性： 高速传输(480Mbps)、全速传输(12Mbps)和低速传输(1.5Mbps) SOF和数据包传输的自动调度 同步和中断传输的可编程间隔 通信通过单个集线器连接多个外围设备。
	设备控制器特性： 高速传输（480Mbps）和全速传输（12Mbps） 控制传输阶段控制功能 设备状态控制功能 SET_ADDRESS请求的自动响应功能 SOF补充。
支持的传输类型	控制传输 批量传输 中断传输 同步传输。
管道配置	用于USB通信的高达8.5KB的FIFO缓冲区 最多可选择10个管道，包括默认控制管道 可编程管道配置 管道1到9可分配给任何端点编号。
	可为每个管道指定传输条件： 管道0：使用64字节单缓冲区进行控制传输 管道1和2：批量同步传输连续传输模式，可编程缓冲区大小高达2KB和可选的双缓冲区 管道3到5：批量传输连续传输模式，可编程缓冲区大小高达2KB，可选双缓冲区 管道6到9：使用64字节单缓冲区的中断传输。
其它功能	使用事务计数的强制结束传输功能 更改BRDY中断事件通知时序的功能 读取DnFIFO端口(n=0 1)中指定管道的数据后自动清除FIFO缓冲区 NAK设置功能传输结束时生成响应PID 用于D+和D的片上上拉和下拉电阻 支持链路电源管理(LPM)ECN，包括新的睡眠状态（L1状态） 符合电池充电类规范修订版1.2 为了降低功耗，可选择仅经典模式（仅CL模式），其中操作仅符合USB1.1标准

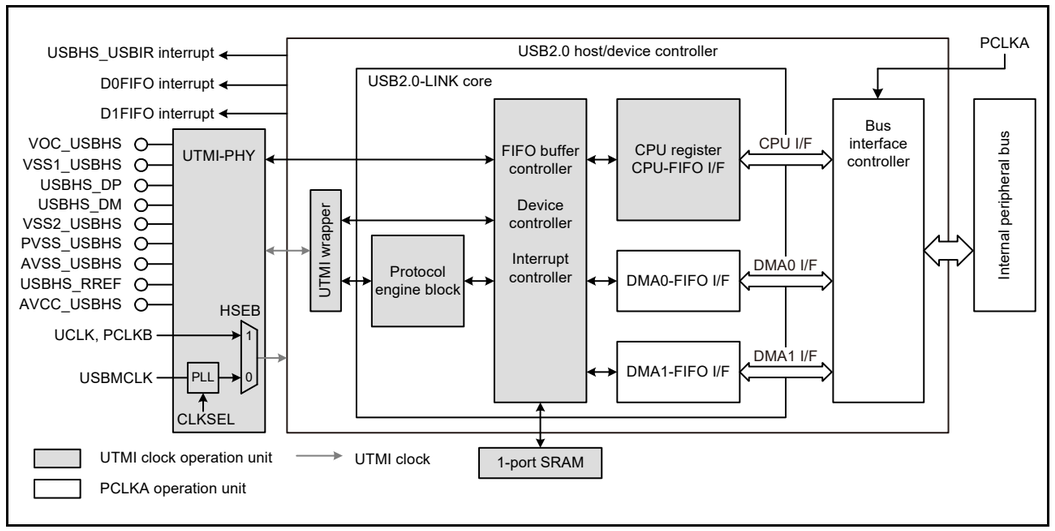


Figure 33.1 USBHS block diagram

Table 33.2 USBHS I/O pins

Pin name	I/O	Function
VCC_USBHS	Input	Power supply pin for the USBHS
VSS1_USBHS VSS2_USBHS	Input	Ground pin for the USBHS
AVCC_USBHS	Input	Analog power supply pin for the USBHS
AVSS_USBHS	Input	Analog ground pin for the USBHS Must be shorted to the PVSS_USBHS pin.
PVSS_USBHS	Input	PLL circuit ground pin for the USBHS Must be shorted to the AVSS_USBHS pin.
USBHS_RREF	I/O	Reference current source pin for the USBHS Must be connected to the AVSS_USBHS pin through a 2.2-kΩ (±1%) resistor.
USBHS_DP	I/O	Input/output pin for the D+ data line of the USB bus
USBHS_DM	I/O	Input/output pin for the D- data line of the USB bus
USBHS_EXICEN	Output	Must be connected to the OTG power supply IC
USBHS_ID	Input	Must be connected to the OTG power supply IC
USBHS_VBUSEN	Output	VBUS power supply enable pin for the USBHS
USBHS_OVRCURA/ USBHS_OVRCURB	Input	Overcurrent pin for the USBHS
USBHS_VBUS	Input	USB cable connection monitor input pin

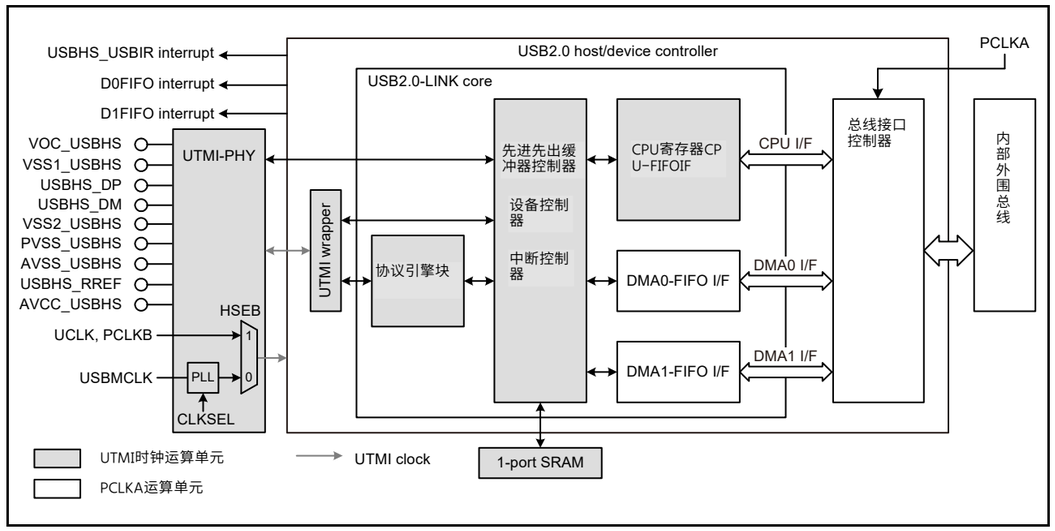


Figure 33.1 USBHS框图

Table 33.2 USBHS I/O pins

引脚名称	I/O	Function
VCC_USBHS	Input	USBHS的电源引脚
VSS1_USBHS VSS2_USBHS	Input	USBHS的接地引脚
AVCC_USBHS	Input	USBHS的模拟电源引脚
AVSS_USBHS	Input	USBHS的模拟接地引脚 必须短接到PVSS_USBHS引脚。
PVSS_USBHS	Input	USBHS的PLL电路接地引脚 必须短接到AVSS_USBHS引脚。
USBHS_RREF	I/O	USBHS的参考电流源引脚 必须通过2.2-kΩ(±1%)电阻连接到AVSS_USBHS引脚。
USBHS_DP	I/O	USB总线D+数据线的输入输出引脚
USBHS_DM	I/O	USB总线Ddata线的输入输出引脚
USBHS_EXICEN	Output	必须接OTG电源IC
USBHS_ID	Input	必须接OTG电源IC
USBHS_VBUSEN	Output	USBHS的VBUS电源使能引脚
USBHS_OVRCURA/ USBHS_OVRCURB	Input	USBHS的过流引脚
USBHS_VBUS	Input	USB线连接显示器输入引脚

33.2 Register Descriptions

33.2.1 System Configuration Control Register (SYSCFG)

Address(es): USBHS.SYSCFG 4006 0000h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	CNEN	HSE	DCFM	DRPD	DPRPU	—	—	—	USBE
Value after reset:	x	x	x	x	x	x	x	0	0	0	1	0	x	x	x	0

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b0	USBE	USBHS Operation Enable	0: Disable 1: Enable.	R/W
b3 to b1	—	Reserved	The read value is undefined. The write value should be 0.	R/W
b4	DPRPU	D+ Line Resistor Control	0: Disable line pull-up 1: Enable line pull-up.	R/W
b5	DRPD	D+/D- Line Resistor Control	0: Disable line pull-down 1: Enable line pull-down.	R/W
b6	DCFM	Controller Operation Select	0: Select device controller mode 1: Select host controller mode.	R/W
b7	HSE	High-Speed Operation Enable	0: Disable Device controller mode: full-speed Host controller mode: full- or low-speed. 1: Enable. The controller detects the communication speed.	R/W
b8	CNEN	Single-ended Receiver Enable	0: Disable 1: Enable.	R/W
b15 to b9	—	Reserved	The read value is undefined. The write value should be 0.	R/W

Writing to the SYSCFG register can proceed while the PHY clock is stopped. However, written values are only reflected in the SYSCFG register after the PHY clock is oscillating again.

USBE bit (USBHS Operation Enable)

The USBE bit enables or disables operation of USBHS.

Changing the USBE bit from 1 to 0 initializes the bits listed in Table 33.3. Only change this bit after specifying the input clock in the PHYSET.CLKSEL[1:0] bits and confirming that the PLLSTA.PLLLOCK flag is 1. In CL-only mode, change the USBE bit after setting the PHYSET.HSEB bit to 1. At that time, the UCLK must be set to 48 MHz and PCLKB must be set to 60 MHz. For the clock settings, see section 33.3.3, Supplying the Clock.

In host controller mode, always set this bit to 1 after setting the DRPD bit to 1, eliminating SYSSTS0.LNST[1:0] bit chattering, and confirming that the USB bus state is stable.

33.2 注册说明

33.2.1 系统配置控制寄存器(SYSCFG)

Address(es): USBHS.SYSCFG 4006 0000h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	CNEN	HSE	DCFM	DRPD	DPRPU	—	—	—	USBE
重置后的值：	x	x	x	x	x	x	x	0	0	0	1	0	x	x	x	0

x: Undefined

Bit	Symbol	位名称	Description	R/W
b0	USBE	USBHS操作使能	0：禁用1 ：启用。	R/W
b3 to b1	—	Reserved	读取值未定义。写入值应为0。	R/W
b4	DPRPU	D+线路电阻控制	0：禁用线路上拉1： 启用线路上拉。	R/W
b5	DRPD	D+DLine电阻控制	0：禁用线路下拉1：启 用线路下拉。	R/W
b6	DCFM	控制器操作选择	0：选择设备控制器模式1：选择 主机控制器模式。	R/W
b7	HSE	高速操作使能	0: Disable 设备控制器模式：全速 主机控制器模式：全速或低速。1：启用。 控制器检测通信速度。	R/W
b8	CNEN	单端接收器使能	0：禁用1 ：启用。	R/W
b15 to b9	—	Reserved	读取值未定义。写入值应为0。	R/W

当PHY时钟停止时，可以继续写入SYSCFG寄存器。但是，写入的值仅在PHY时钟再次振荡后才会反映在SYSCFG寄存器中。

USBE位（USBHS操作使能）

USBE位启用或禁用USBHS的操作。

将USBE位从1更改为0会初始化表33.3中列出的位。仅在PHYSET.CLKSEL[1:0]位中指定输入时钟并确认PLLSTA.PLLLOCK标志为1后更改该位。在CL-only模式下，将PHYSET.HSEB位设置为1后更改USBE位.那时，UCLK必须设置为48MHz，PCLKB必须设置为60MHz。有关时钟设置，请参阅第33.3.3节，提供时钟。

在主机控制器模式下，在将DRPD位设置为1后始终将此位设置为1，消除SYSSTS0.LNST[1:0]位抖动，并确认USB总线状态稳定。

Table 33.3 Bits initialized by writing SYSCFG.USBE = 0

Selected function	Register	Bit	Remarks
Device controller (DCFM = 0)	SYSSTS0	LNST[1:0]	Value is saved in host controller mode
	DVSTCTR0	RHST[2:0]	-
	PL1CTRL1	DVSQ[3:0]	Value is saved in host controller mode
	USBADDR	USBADDR[6:0]	Value is saved in host controller mode
	USBREQ	• BREQUEST[7:0] • BMREQUESTTYPE[7:0].	Value is saved in host controller mode
	USBVAL	WVALUE[15:0]	Value is saved in host controller mode
	USBINDX	WINDEX[15:0]	Value is saved in host controller mode
	USBLENG	WLENTUH[15:0]	Value is saved in host controller mode
Host controller (DCFM = 1)	DVSTCTR0	RHST[2:0]	-
	FRMNUM	FRNM[10:0]	Value is saved in device controller mode
	UFRMNUM	UFRNM[2:0]	Value is saved in device controller mode

DPRPU bit (D+ Line Resistor Control)

The DPRPU bit enables or disables pulling up the D+ line in device controller mode.

When the DPRPU bit is set to 1 in device controller mode, the USBHS pulls up the D+ line to notify the USB host that it attached. Changing the DPRPU bit from 1 to 0 releases the pull-up, thereby notifying the USB host that it detached.

Set this bit to 1 in device controller mode and to 0 in host controller mode.

DRPD bit (D+/D- Line Resistor Control)

The DRPD bit enables or disables pulling down D+ and D- lines in host controller mode.

Set this bit to 1 in host controller mode. Set it to 0 when OTG is not used in device controller mode.

DCFM bit (Controller Operation Select)

The DCFM bit selects the host or device function of the USBHS.

Only change this bit when the DPRPU and DRPD bits are both 0.

HSE bit (High-Speed Operation Enable)

The HSE bit enables or disables high-speed operation.

When this bit is 1, the USBHS operates in high- or full-speed based on the results of the reset handshake.

In host controller mode, setting this bit to 0 allows the USBHS to operate in low- or full-speed. If the DVSTCTR0.RHST[2:0] flags indicate that a low-speed device has attached, set the HSE bit to 0.

In host controller mode, setting this bit to 1 allows the USBHS to operate in high- or full-speed based on the results of the reset handshake. Change the HSE bit after detection of an attach event (ATTCH interrupt) and before the USB bus reset (when DVSTCTR0.USBRST = 1), or after detection of a detach event.

In device controller mode, setting this bit to 0 allows the USBHS to operate in full-speed. Setting the bit to 1 allows the USBHS to perform the reset handshake and then operate in high-speed or full-speed, based on the results.

In device controller mode, only change this bit when the DPRPU bit is 0.

CNEN bit (Single-ended Receiver Enable)

Setting the CNEN bit to 1 enables single-ended receiver operation and selects monitoring of the D+ and D- line states in the SYSSTS0.LNST[1:0] flags. Use this bit to prevent through-current damage that might otherwise be caused during single-ended receiver operation, where the terminals are floating while the USBHS is detached.

In host controller mode, set this bit to 1 after confirming that the PHY clock is being supplied. In device controller mode, set this bit to 1 when the VBUS is detected because of a VBUS interrupt, and set it to 0 when the VBUS line is removed.

Table 33.3 通过写入SYSCFG.USBE=0初始化的位

所选功能	Register	Bit	Remarks
设备控制器(DCFM=0)	SYSSTS0	LNST[1:0]	值以主机控制器模式保存
	DVSTCTR0	RHST[2:0]	-
	PL1CTRL1	DVSQ[3:0]	值以主机控制器模式保存
	USBADDR	USBADDR[6:0]	值以主机控制器模式保存
	USBREQ	• BREQUEST[7:0] • BMREQUESTTYPE[7:0].	值以主机控制器模式保存
	USBVAL	WVALUE[15:0]	值以主机控制器模式保存
	USBINDX	WINDEX[15:0]	值以主机控制器模式保存
	USBLENG	WLENTUH[15:0]	值以主机控制器模式保存
主机控制器(DCFM=1)	DVSTCTR0	RHST[2:0]	-
	FRMNUM	FRNM[10:0]	值保存在设备控制器模式中
	UFRMNUM	UFRNM[2:0]	值保存在设备控制器模式中

DPRPU位（D+线路电阻控制）

DPRPU位启用或禁用在设备控制器模式下上拉D+线。

当DPRPU位在设备控制器模式下设置为1时，USBHS拉高D+线以通知USB主机它已连接。将DPRPU位从1更改为0会释放上拉电阻，从而通知USB主机它已分离。

在设备控制器模式下将此位设置为1，在主机控制器模式下设置为0。

DRPD位（D+DLine电阻控制）

DRPD位在主机控制器模式下启用或禁用下拉D+和Dlines。

在主机控制器模式下将此位设置为1。在设备控制器模式下不使用OTG时将其设置为0。

DCFM位（控制器操作选择）

DCFM位选择USBHS的主机或设备功能。

仅当DPRPU和DRPD位都为0时更改该位。

HSE位（高速操作使能）

HSE位启用或禁用高速操作。

当该位为1时，USBHS根据复位握手的结果以高速或全速运行。

在主机控制器模式下，将该位设置为0允许USBHS以低速或全速运行。如果DVSTCTR0.RHST[2:0]标志表示已连接低速设备，将HSE位设置为0。

在主机控制器模式下，将此位设置为1允许USBHS根据复位握手的结果以高速或全速运行。在检测到附加事件（ATTCH中断）和USB总线复位之前（当DVSTCTR0.USBRST=1时）或检测到分离事件之后，更改HSE位。

在设备控制器模式下，将该位设置为0允许USBHS全速运行。将该位设置为1允许USBHS根据结果执行复位握手，然后以高速或全速运行。

在设备控制器模式下，仅当DPRPU位为0时更改该位。

CNEN位（单端接收器使能）

将CNEN位设置为1可启用单端接收器操作，并在SYSSTS0.LNST[1:0]标志中选择监视D+和Dline状态。使用该位可防止在单端接收器操作期间可能造成的直通电流损坏，其中在USBHS分离时端子处于浮动状态。

在主机控制器模式下，在确认提供PHY时钟后将该位设置为1。在设备控制器模式下，当由于VBUS中断而检测到VBUS时将该位设置为1，并在移除VBUS线时将其设置为0。

33.2.2 CPU Bus Wait Register (BUSWAIT)

Address(es): USBHS.BUSWAIT 4006 0002h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	BWAIT[3:0]			
Value after reset:	x	x	0	0	0	0	0	0	x	x	0	0	1	1	1	1

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b3 to b0	BWAIT[3:0]	CPU Bus Access Wait Specification	b3 b0 0 0 0 0: 0 waits (2 access cycles) : : 0 0 1 0: 2 waits (4 access cycles) : : 0 1 0 0: 4 waits (6 access cycles) : : 1 1 1 1: 15 waits (17 access cycles) (initial value).	R/W
b5, b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7, b6	—	Reserved	The read value is undefined. The write value should be 0.	R/W
b13 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15, b14	—	Reserved	The read value is undefined. The write value should be 0.	R/W

BWAIT[3:0] bits (CPU Bus Access Wait Specification)

The BWAIT[3:0] bits specify the wait time for access to the USBHS registers.

When accessing the registers at addresses in the range beginning at 4006 0004h, set the cycle time for consecutive access to at least 40.8 ns. The initial value is 1111b (17 cycles), but Renesas recommends that you satisfy this condition by setting the best wait time for the frequency of the CPU clock in your application.

This setting is the same as the wait time for accesses to the FIFO port register. The maximum speed of access to the FIFO port is as follows:

- MBW[1:0] = 10b (32-bit width): Maximum 60 MB/s
- MBW[1:0] = 01b (16-bit width): Maximum 30 MB/s
- MBW[1:0] = 00b (8-bit width): Maximum 15 MB/s

33.2.3 System Configuration Status Register (SYSSTS0)

Address(es): USBHS.SYSSTS0 4006 0004h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	OVCMON[1:0]		—	—	—	—	—	—	—	HTACT	SOFEA	—	—	IDMON	LNST[1:0]	
Value after reset:	x	x	x	x	x	x	x	x	x	0	0	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b1, b0	LNST[1:0]	USB Data Line Status Monitor Flag	Indicates the status of the USB data lines. See Table 33.4.	R
b2	IDMON	USBHS_ID Pin Monitor Flag	0: USBHS_ID pin is low 1: USBHS_ID pin is high.	R
b4, b3	—	Reserved	The read value is undefined.	R

33.2.2 CPU总线等待寄存器(BUSWAIT)

Address(es): USBHS.BUSWAIT 4006 0002h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	BWAIT[3:0]			
重置后的值：	x	x	0	0	0	0	0	0	x	x	0	0	1	1	1	1

x: Undefined

Bit	Symbol	位名称	Description	R/W
b3 to b0	BWAIT[3:0]	CPU总线访问等待 Specification	b3 b0 0 0 0 0：0等待（2个访问周期） : : 0 0 1 0：2次等待（4个访问周期） : : 0 1 0 0：4次等待（6个访问周期） : : 1 1 1 1：15次等待（17个访问周期）（初始值）。	R/W
b5, b4	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b7, b6	—	Reserved	读取值未定义。写入值应为0。	R/W
b13 to b8	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b15, b14	—	Reserved	读取值未定义。写入值应为0。	R/W

BWAIT[3:0]位（CPU总线访问等待规范）

BWAIT[3:0]位指定访问USBHS寄存器的等待时间。

当访问地址范围从40060004h开始的寄存器时，将连续访问的周期时间设置为至少40.8ns。初始值为1111b（17个周期），但瑞萨建议您通过在应用程序中为CPU时钟频率设置最佳等待时间来满足此条件。

该设置与访问FIFO端口寄存器的等待时间相同。访问FIFO端口的最大速度如下：

- MBW[1:0] = 10b (32-bit width): Maximum 60 MB/s
- MBW[1:0] = 01b (16-bit width): Maximum 30 MB/s
- MBW[1:0] = 00b (8-bit width): Maximum 15 MB/s

33.2.3 系统配置状态寄存器(SYSSTS0)

Address(es): USBHS.SYSSTS0 4006 0004h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	OVCMON[1:0]		—	—	—	—	—	—	—	HTACT	SOFEA	—	—	IDMON	LNST[1:0]	
重置后的值：	x	x	x	x	x	x	x	x	x	0	0	x	x	x	x	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b1, b0	LNST[1:0]	USB数据线状态监视器 Flag	指示USB数据线的状态。见表33.4。	R
b2	IDMON	USBHS_ID引脚监控标志	0：USBHS_ID引脚为低电平1 ：USBHS_ID引脚为高电平。	R
b4, b3	—	Reserved	读取值未定义。	R

Bit	Symbol	Bit name	Description	R/W
b5	SOFEA	SOF Active Monitor Flag While Host Controller Operation Is Selected	0: SOF output stopped 1: SOF output operating.	R
b6	HTACT	Host Sequencer Status Monitor Flag	0: Host sequencer stopped 1: Host sequencer operating.	R
b13 to b7	—	Reserved	The read value is undefined.	R
b15, b14	OVCMON[1:0]	External USBHS_OVRCURA/USBHS_OVRCURB Input Pin Monitor Flag	OVCMON[1] indicates the USBHS_OVRCURA pin status. OVCMON[0] indicates the USBHS_OVRCURB pin status.	R

LNST[1:0] flags (USB Data Line Status Monitor Flag)

The LNST[1:0] flags indicate the state of the USB data lines, D+ and D-. For details, see Table 33.4.

In device controller mode, read the LNST[1:0] flags after setting the SYSCFG.CNEN and SYSCFG.USBE bits to 1. In host controller mode, read them after setting the SYSCFG.DRPD bit to 1.

When you are checking hardware contacts for the battery charging function in device controller mode, read the LNST[1:0] flags after setting the SYSCFG.DRPD, SYSCFG.CNEN, and BCCTRL.IDPSRCE bits to 1. For details, see section 33.3.15, Battery charging detection processing.

Table 33.4 Status of USB data bus lines (D+ and D-)

LNST[1]	LNST[0]	Low-speed operation (host controller mode only)	Full-speed operation	High-speed operation	Chirp operation
0	0	SE0	SE0	Squelch	Squelch
0	1	K-State	J-State	Unsquelch	Chirp J
1	0	J-State	K-State	Invalid	Chirp K
1	1	SE1	SE1	Invalid	Invalid

Chirp: The reset handshake protocol is being executed when high-speed operation is enabled (HSE bit is 1).
Squelch: SE0 or idle state
Unsquelch: High-speed J-state or high-speed K-state
Chirp J: Chirp J-State
Chirp K: Chirp K-State

SOFEA flag (SOF Active Monitor Flag While Host Controller Operation Is Selected)

The SOFEA flag is used in host controller mode to check whether the output of the last SOF is complete when the USBHS is suspended because of a 0 setting to the DVSTCTR0.UACT bit.

In host controller mode, check that both the HTACT and SOFEA flags are 0 before setting the SYSCFG.USBE bit to 0 to stop the USBHS or setting the LPSTS.SUSPENDM bit to 0 to stop the clock signal supply during communication.

HTACT flag (Host Sequencer Status Monitor Flag)

The HTACT flag clears to 0 when the host sequencer of the USBHS is completely stopped.

In host controller mode, check that the HTACT flag is 0 before setting the DVSTCTR0.UACT bit to 0 to place the USBHS in the Suspend state or setting the LPSTS.SUSPENDM bit to 0 to stop the clock signal supply during communication.

OVCMON[1:0] flags (External USBHS_OVRCURA/USBHS_OVRCURB Input Pin Monitor Flag)

The OVCMON[1:0] flags indicate the status of the overcurrent signals from an external power supply IC.

Bit	Symbol	位名称	Description	R/W
b5	SOFEA	SOF主动监控标志，而主机控制器操作是 Selected	0：SOF输出停止1：SOF输出工作。	R
b6	HTACT	主机排序器状态监视器 Flag	0：主机定序器停止1：主机定序器运行。	R
b13 to b7	—	Reserved	读取值未定义。	R
b15, b14	OVCMON[1:0]	External USBHS_OVRCURAUSBHS_OVRCURB输入管脚监控标志	OVCMON[1]指示USBHS_OVRCURA引脚状态。OVCMON[0]指示USBHS_OVRCURB引脚状态。	R

LNST[1:0]标志（USB数据线状态监控标志）

LNST[1:0]标志指示USB数据线D+和D−的状态。详见表33.4。

在设备控制器模式下，将SYSCFG.CNEN和SYSCFG.USBE位设置为1后读取LNST[1:0]标志。在主机控制器模式下，将SYSCFG.DRPD位设置为1后读取它们。

在设备控制器模式下检查电池充电功能的硬件触点时，请阅读将SYSCFG.DRPD、SYSCFG.CNEN和BCCTRL.IDPSRCE位设置为1后的LNST[1:0]标志。有关详细信息，请参见第33.3.15节，电池充电检测处理。

Table 33.4 USB数据总线的状态（D+和D−）

LNST[1]	LNST[0]	低速运行（仅主机控制器模式）	Full-speed operation	High-speed operation	啁啾操作
0	0	SE0	SE0	Squelch	Squelch
0	1	K-State	J-State	Unsquelch	Chirp J
1	0	J-State	K-State	Invalid	Chirp K
1	1	SE1	SE1	Invalid	Invalid

Chirp: 当使能高速操作（HSE位为1）时，正在执行复位握手协议。
Squelch: SE0或空闲状态
Unsquelch: High-speed J-state or high-speed K-state
Chirp J: Chirp J-State
Chirp K: Chirp K-State

SOFEA标志（选择主机控制器操作时的SOF活动监视器标志）

SOFEA标志用于主机控制器模式，用于检查最后一个SOF的输出是否完成。
由于DVSTCTR0.UACT位设置为0，USBHS被挂起。

在主机控制器模式下，在将SYSCFG.USBE位设置为0以停止USBHS或将LPSTS.SUSPENDM位设置为0以在通信期间停止时钟信号供应之前，请检查HTACT和SOFEA标志是否为0。

HTACT标志（主机定序器状态监视器标志）

当USBHS的主机定序器完全停止时，HTACT标志清零。

在主机控制器模式下，在将DVSTCTR0.UACT位设置为0之前检查HTACT标志是否为0以放置USBHS处于Suspend状态或将LPSTS.SUSPENDM位设置为0以在通信期间停止时钟信号供应。

OVCMON[1:0]标志（外部USBHS_OVRCURAUSBHS_OVRCURB输入引脚监控标志）

OVCMON[1:0]标志指示来自外部电源IC的过流信号的状态。

33.2.4 PLL Status Register (PLLSTA)

Address(es): USBHS.PLLSTA 4006 0006h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PLLLOCK
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b0	PLLLOCK	PLL Lock Flag	0: PLL not locked 1: PLL locked.	R
b15 to b1	—	Reserved	The read value is undefined.	R

PLLLOCK flag (PLL Lock Flag)

The PLLLOCK flag indicates whether the USB-PHY internal PLL is locked. When not using CL-only mode, make sure that the PLL is locked before starting USB communication.

33.2.5 Device State Control Register 0 (DVSTCTR0)

Address(es): USBHS.DVSTCTR0 4006 0008h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	HNPBTOA	EXICEN	VBUSEN	WKUP	RWUPE	USBRST	RESUME	UACT	—	RHST[2:0]		
Value after reset:	x	x	x	x	0	0	0	0	0	0	0	0	x	0	0	0

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b2 to b0	RHST[2:0]	USB Bus Reset Status Flag	• Host controller mode b2 b0 0 0 0: Communication speed indeterminate (powered state or no connection) 1 x x: USB bus reset in progress 0 0 1: Low-speed connection 0 1 0: Full-speed connection 0 1 1: High-speed connection. x: Don't care • Device controller mode b2 b0 0 0 0: Communication speed indeterminate (powered state or no connection) 0 0 1: USB bus reset in progress or low-speed connection 0 1 0: USB bus reset in progress or full-speed connection 0 1 1: USB bus reset in progress or high-speed connection.	R
b3	—	Reserved	The read value is undefined. The write value should be 0.	R/W
b4	UACT	USB Bus Operation Enable for the Host Controller Operation	0: Disable downstream port (disable SOF or micro-SOF transmission) 1: Enable downstream port (enable SOF or micro-SOF transmission).	R/W
b5	RESUME	Resume Signal Output for the Host Controller Operation	0: Do not output resume signal 1: Output resume signal.	R/W
b6	USBRST	USB Bus Reset Output for the Host Controller Operation	0: Do not output USB bus reset signal 1: Output USB bus reset signal.	R/W

33.2.4 PLL状态寄存器(PLLSTA)

Address(es): USBHS.PLLSTA 4006 0006h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PLLLOCK
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	0

x: Undefined

Bit	Symbol	位名称	Description	R/W
b0	PLLLOCK	PLL锁定标志	0：PLL未锁定1： PLL锁定。	R
b15 to b1	—	Reserved	读取值未定义。	R

PLLLOCK标志（PLL锁定标志）

PLLLOCK标志指示USB-PHY内部PLL是否被锁定。不使用CL-only模式时，请确保在开始USB通信之前锁定PLL。

33.2.5 设备状态控制寄存器0(DVSTCTR0)

Address(es): USBHS.DVSTCTR0 4006 0008h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	HNPBTOA	EXICEN	VBUSEN	WKUP	RWUPE	USBRST	RESUME	UACT	—	RHST[2:0]		
重置后的值：	x	x	x	x	0	0	0	0	0	0	0	0	x	0	0	0

x: Undefined

Bit	Symbol	位名称	Description	R/W
b2 to b0	RHST[2:0]	USB总线复位状态标志	主机控制器模式b2 0 0 0：通讯速度不定（通电或无连接） 1 x x：正在进行USB总线复位 0 0 1: Low-speed connection 0 1 0: Full-speed connection 11：高速连接。x：无关 设备控制器模式b2 0 0 0：通讯速度不定（通电或无连接） 0 0 1：USB总线复位中或低速连接 0 1 0：USB总线复位中或全速连接 0 1 1：USB总线正在复位或高速连接。	R
b3	—	Reserved	读取值未定义。写入值应为0。	R/W
b4	UACT	主机控制器操作的USB总线操作使能	0：禁用下行端口（禁用SOF或micro-SOF传输）1：启用下行端口（启用SOF或micro-SOF传输）。	R/W
b5	RESUME	恢复信号输出为主机控制器操作	0：不输出恢复信号1：输出恢复信号。	R/W
b6	USBRST	USB总线复位输出为主机控制器操作	0：不输出USB总线复位信号1：输出USB总线复位信号。	R/W

Bit	Symbol	Bit name	Description	R/W
b7	RWUPE	Remote Wakeup Detection Enable for the Host Controller Operation	0: Disable downstream port remote wakeup 1: Enable downstream port remote wakeup.	R/W
b8	WKUP	Remote Wakeup Output for the Device Controller Operation	0: Do not output remote wakeup signal 1: Output remote wakeup signal.	R/W
b9	VBUSEN	USBHS_VBUSEN Output Pin Control	0: Output low on external USBHS_VBUSEN pin 1: Output high on external USBHS_VBUSEN pin.	R/W
b10	EXICEN	USBHS_EXICEN Output Pin Control	0: Output low on external USBHS_EXICEN pin 1: Output high on external USBHS_EXICEN pin.	R/W
b11	HNPBTOA	Host Negotiation Protocol (HNP) Control	Use this bit when switching from device B to device A in OTG mode. If the HNPBTOA bit is 1, the internal function control remains in the Suspend state until the HNP processing ends even if SYSCFG.DPRPU = 0 or SYSCFG.DCFM = 1 is set.	R/W
b15 to b12	—	Reserved	The read value is undefined. The write value should be 0.	R/W

RHST[2:0] flags (USB Bus Reset Status Flag)

The RHST[2:0] flags indicate the USB bus reset status.

In host controller mode, writing 1 to the USBRST bit causes the RHST[2:0] flags to set to 100b. When 0 is written to the USBRST bit and the USBHS ends the SE0 state, the RHST[2:0] flags update to a new value.

In device controller mode, if the USBHS detects a USB bus reset, the RHST[2:0] flags set to 010b if an attach event occurs while the DPRPU bit is 1, and a DVST interrupt is generated.

UACT bit (USB Bus Operation Enable for the Host Controller Operation)

When set to 1 in host controller mode, the UACT bit enables USB bus operation by controlling SOF packet transmission to the USB bus in addition to data and reception. The USBHS starts SOF packet output within one frame period after the this bit is set to 1. If UACT is set to 0, the USBHS enters the idle state after the SOF packet output.

The USBHS sets the bit to 0 on any of the following conditions:

- A DTCH interrupt is detected during communication (while UACT = 1)
- An EOFERR interrupt is detected during communication (while UACT = 1).

Always write 1 to the UACT bit at the end of the USB bus reset processing (on a 0 write to the USBRST bit) or at the end of resume processing from the Suspend state (on a 0 write to the RESUME bit).

The USBHS clears the UACT bit to 0 if it receives an ACK response to an LPM token while the HL1CTRL1.L1REQ bit is set to 1. The USBHS sets the UACT bit to 1 when it finishes resume processing from the L1 state.

In device controller mode, always set this bit to 0.

RESUME bit (Resume Signal Output for the Host Controller Operation)

The RESUME bit controls the resume signal output in host controller mode.When this bit is set to 1, the USBHS drives the USB port to the K-state and outputs the resume signal. The USBHS sets the bit to 1 on detection of a remote wakeup signal while the RWUPE bit is 1 and in the USB suspend state. The USBHS continues outputting the K-state while the RESUME bit is 1, until the bit is cleared to 0 by software. The RESUME bit must be 1 (= resume period) for the time defined in the USB 2.0 specification. Only set this bit to 1 while the interface is in the Suspend state. Write 1 to the UACT bit simultaneously with the end of the resume processing (0 write to the RESUME bit).

Setting the RESUME bit to 1 during transition to the L1 state allows the USBHS to drive the USB port to the K-state and output the resume signal. The USBHS clears the RESUME bit to 0 at the end of the resume period, the value set in the HL1CTRL2.HIRD[3:0] bits.

Always set this bit to 0 in device controller mode.

USBRST bit (USB Bus Reset Output for the Host Controller Operation)

The USBRST bit controls the output of the USB bus signal in host controller mode. When this bit set to 1, the USBHS drives the USB port to the SE0 state to reset the USB bus. The USBHS continues outputting SE0 while the USBRST bit is 1, until the bit is cleared to 0 by software. The USBRST bit must be 1 (= USB bus reset period) for the time defined in

Bit	Symbol	位名称	Description	R/W
b7	RWUPE	远程唤醒检测 启用主机控制器 Operation	0：禁用下游端口远程唤醒1：启用下游端口 远程唤醒。	R/W
b8	WKUP	远程唤醒输出为 设备控制器操作	0：不输出远程唤醒信号1：输出远程 唤醒信号。	R/W
b9	VBUSEN	USBHS_VBUSEN输出引脚 Control	0：外部USBHS_VBUSEN引脚输出低电平1：外部 USBHS_VBUSEN引脚输出高电平。	R/W
b10	EXICEN	USBHS_EXICEN输出引脚 Control	0：外部USBHS_EXICEN引脚输出低电平1：外部 USBHS_EXICEN引脚输出高电平。	R/W
b11	HNPBTOA	主机协商协议(HNP)控制	在OTG模式下从设备B切换到设备A时使用该位。如果HNPBTO A位为1，即使设置SYSCFG.DPRPU=0或SYSCFG.DCFM=1，内 部功能控制仍保持暂停状态直到HNP处理结束。	R/W
b15 to b12	—	Reserved	读取值未定义。写入值应为0。	R/W

RHST[2:0]标志（USB总线复位状态标志）

RHST[2:0]标志指示USB总线复位状态。

在主机控制器模式下，将1写入USBRST位会导致RHST[2:0]标志设置为100b。当0被写入USBRST位和USBHS结束SE0状态，RHST[2:0]标志更新为新值。

在设备控制器模式下，如果USBHS检测到USB总线复位，如果在DPRPU位为1时发生连接事件并产生DVST中断，则RHST[2:0]标志设置为010b。

UACT位（主机控制器操作的USB总线操作使能）

在主机控制器模式下设置为1时，UACT位通过控制向USB总线发送SOF数据包以及数据和接收来启用USB总线操作。USBHS在该位设置为1后的一帧周期内开始SOF数据包输出。如果UACT设置为0，则USBHS在SOF数据包输出后进入空闲状态。

USBHS在以下任何条件下将该位设置为0：

- 在通信期间检测到DTCH中断（当UACT=1时）
- 通信期间检测到EOFERR中断（当UACT=1时）。

在USB总线复位处理结束时（向USBRST位写入0）或从挂起状态恢复处理结束时（向RESUME位写入0），始终向UACT位写入1。

如果USBHS在HL1CTRL1.L1REQ位设置为1时接收到对LPM令牌的ACK响应，则将UACT位清除为0。USBHS在完成从L1状态恢复处理时将 UACT位设置为1。

在设备控制器模式下，始终将此位设置为0。

RESUME位（主机控制器操作的恢复信号输出）

RESUME位控制主机控制器模式下的恢复信号输出。当该位设置为1时，USBHS将USB端口驱动到K状态并输出恢复信号。当RUPE位为1且处于USB挂起状态时，USBHS在检测到远程唤醒信号时将该位设置为1。当RESUME位为1时，USBHS继续输出K状态，直到该位被软件清零。在USB2.0规范中定义的时间内，RESUME位必须为1（=恢复周期）。仅当接口处于挂起状态时将此位设置为1。在恢复处理结束的同时向UACT位写入1（向RESUME位写入0）。

在转换到L1状态期间将RESUME位设置为1允许USBHS将USB端口驱动到K状态并输出恢复信号。USBHS在恢复周期结束时将RE SUME位清除为0，该值在HL1CTRL2.HIRD[3:0]位中设置。

在设备控制器模式下始终将此位设置为0。

USBRST位（用于主机控制器操作的USB总线复位输出）

USBRST位控制主机控制器模式下USB总线信号的输出。当该位设置为1时，USBHS将USB端口驱动到SE0状态以复位USB总线。当USBRST位为1时，USBHS继续输出SE0，直到该位被软件清零。USBRST位在定义的时间内必须为1（=USB总线复位周期）

the USB 2.0 specification. Writing 1 to the USBRST bit during communication (UACT bit = 1) or during resume processing (RESUME bit = 1) prevents the USBHS from starting USB bus reset processing until both the UACT and RESUME bits clear to 0. Write 1 to the UACT bit simultaneously with the end of the USB bus reset processing (0 write to the USBRST bit).

Always set this bit to 0 in device controller mode.

RWUPE bit (Remote Wakeup Detection Enable for the Host Controller Operation)

The RWUPE bit enables or disables remote wakeup signals (resume signals) from downstream peripheral devices in host controller mode. When this bit is set to 1, the USBHS detects a remote wakeup signal (K-state for 2.5 µs) from a downstream peripheral device, and it performs resume processing, driving the K-state. When the RWUPE bit is set to 0, the USBHS ignores remote wakeup signals (K-states) from peripheral devices connected to the USB port.

Do not stop the PHY clock while the RWUPE bit is 1, even in the Suspend state (the LPSTS.SUSPENDM bit must be set to 1). Also, do not reset the USB bus (setting USBRST to 1) from the Suspend state. This is prohibited in the USB 2.0 specification.

The RWUPE bit is also used to enable or disable detection of a remote wakeup signal during transition to the L1 state.

Always set this bit to 0 in device controller mode.

WKUP bit (Remote Wakeup Output for the Device Controller Operation)

The WKUP bit enables or disables remote wakeup signals (resume signals) to the USB bus in device controller mode.

The USBHS controls the output timing of the remote wakeup signals. When this bit is set to 1, the USBHS clears it to 0 after outputting the K-state for 10 ms. The USB 2.0 specification dictates that the USB bus idle state must be maintained for 5 ms or longer before a remote wakeup signal is sent. If the USBHS writes 1 to the WKUP bit immediately after detecting the Suspend state, the K-state is output after 2 ms.

Only write 1 to the WKUP bit when the device is in the Suspend state (the PL1CTRL1.DVSQ[3:0] flags are 01xxb) and the USB host enables the remote wakeup signal (RWUPE = 1). Do not stop the PHY clock while this bit is 1, even in the Suspend state (the LPSTS.SUSPENDM bit must be set to 1).

If the WKUP bit is set to 1 during transition to the L1 state, the USBHS outputs the K-state for 50 µs and then clears the bit to 0. Before writing 1 to the bit during the L1 state, check that the PL1CTRL1.DVSQ[3:0] flags are 10xxb.

Always set this bit to 0 in host controller mode.

HNPBTOA bit (Host Negotiation Protocol (HNP) Control)

The HNPBTOA bit is used when switching from device B to device A while in OTG mode.

If the HNPBTOA bit is 1, the internal function control maintains the Suspend state until HNP processing ends, even if the SYSCFG.DPRPU bit is set to 0 or the SYSCFG.DCFM bit is set to 1. Resume interrupts (RESM) are not generated even if a falling edge of D+ is detected.

The HNP processing ends when a host attach event is detected, because of a pull-up by the initiating party, or the HNPBTOA bit is cleared to 0 by software because the HNP processing times out.

33.2.6 USB Test Mode Register (TESTMODE)

Address(es): USBHS.TESTMODE 4006 000Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	UTST[3:0]			
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	0	0	0	0

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b3 to b0	UTST[3:0]	Test Mode	These bits output the USB test signals. See Table 33.5.	R/W

USB2.0规范。在通信期间（UACT位=1）或恢复处理期间（RESUME位=1）向USBRST位写入1可防止USBHS启动USB总线复位处理，直到UACT和RESUME位都清零。向UACT位写入1同时结束USB总线复位处理（0写入USB RST位）。

在设备控制器模式下始终将此位设置为0。

RHUPE位（主机控制器操作的远程唤醒检测使能）

在主机控制器模式下，RWUPE位启用或禁用来自下游外围设备的远程唤醒信号（恢复信号）。当该位设置为1时，USBHS检测到来自下游外围设备的远程唤醒信号（K状态持续2.5µs），并执行恢复处理，驱动K状态。当RWUPE位设置为0时，USBHS忽略来自连接到USB端口的外围设备的远程唤醒信号（K状态）。

当RHUPE位为1时不要停止PHY时钟，即使处于挂起状态（LPSTS.SUSPENDM位必须设置为1）。此外，不要将USB总线（将USBRST设置为1）从挂起状态复位。这在USB2.0规范中是禁止的。

RWUPE位还用于在转换到L1状态期间启用或禁用远程唤醒信号的检测。

在设备控制器模式下始终将此位设置为0。

WKUP位（设备控制器操作的远程唤醒输出）

WKUP位在设备控制器模式下启用或禁用到USB总线的远程唤醒信号（恢复信号）。

USBHS控制远程唤醒信号的输出时序。当该位设置为1时，USBHS在输出K状态10ms后将其清除为0。USB2.0规范规定，在发送远程唤醒信号之前，USB总线空闲状态必须保持5ms或更长时间。如果USBHS在检测到Suspend状态后立即向WKUP位写入1，则在2ms后输出K状态。

仅当器件处于挂起状态（PL1CTRL1.DVSQ[3:0]标志为01xxb）且USB主机使能远程唤醒信号（RWUPE=1）时向WKUP位写入1。当该位为1时不要停止PHY时钟，即使处于挂起状态（LPSTS.SUSPENDM位必须设置为1）。

如果在转换到L1状态期间WKUP位设置为1，则USBHS输出K状态50µs，然后将该位清除为0。在L1状态期间向该位写入1之前，请检查PL1CTRL1.DVSQ[3:0]标志为10xxb。

在主机控制器模式下始终将此位设置为0。

HNPBTOA位（主机协商协议(HNP)控制）

在OTG模式下从设备B切换到设备A时使用HNPBTOA位。

如果HNPBTOA位为1，内部功能控制保持暂停状态直到HNP处理结束，即使SYSCFG.DPRPU位设置为0或SYSCFG.DCFM位设置为1。不产生恢复中断(RESM)即使检测到D+的下降沿。

当检测到主机连接事件时，HNP处理结束，因为发起方的上拉，或者
由于HNP处理超时，HNPBTOA位由软件清零。

33.2.6 USB测试模式寄存器(TESTMODE)

Address(es): USBHS.TESTMODE 4006 000Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	UTST[3:0]			
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	0	0	0	0

x: Undefined

Bit	Symbol	位名称	Description	R/W
b3 to b0	UTST[3:0]	测试模式	这些位输出USB测试信号。见表33.5。	R/W

Bit	Symbol	Bit name	Description	R/W
b15 to b4	—	Reserved	The read value is undefined. The write value should be 0.	R/W

UTST[3:0] bits (Test Mode)

Writing values to the UTST[3:0] bits allows the USBHS to output USB test signals in high-speed operation mode. Table 33.5 shows the test mode operation settings.

Table 33.5 Test mode operation settings

Test mode	UTST[3:0] bit setting	
	In device controller mode	In host controller mode
Normal operation	0000b	0000b
Test_J	0001b	1001b
Test_K	0010b	1010b
Test_SE0_NAK	0011b	1011b
Test_Packet	0100b	1100b
Test_Force_Enable	—	1101b
Reserved	0101b to 0111b	1110b to 1111b

Host controller mode

In host controller mode, these bits can be set after setting the SYSCFG.DRPD bit to 1. After the UTST[3:0] bits are set, the USBHS outputs waveforms to the USB port by setting the DVSTCTR0.UACT bit to 1. The USBHS also performs high-speed termination for the USB port by setting these bits in host controller mode.

To set the UTST[3:0] bits in host controller mode:

1. Reset the hardware.
2. Start supplying the PHY clock, and then set the LPSTS.SUSPENDM bit to 1.
3. Set the SYSCFG.DCFM and SYSCFG.DRPD bits to 1. (Setting the SYSCFG.HSE bit to 1 is not required.)
4. Set the SYSCFG.USBE bit to 1.
5. Set the UTST[3:0] bits based on the test requirements.
6. Set the DVSTCTR0.UACT bit to 1.

Assuming the initial steps (1) to (6) are already complete, to change the UTST[3:0] bits in host controller mode:

1. Set the DVSTCTR0.UACT and SYSCFG.USBE bits to 0.
2. Set the SYSCFG.USBE bit to 1.
3. Set the UTST[3:0] bits based on the test requirements.
4. Set the DVSTCTR0.UACT bit to 1.

When the UTST[3:0] bits are set to 1011b (Test_SE0_NAK), the USBHS does not output SOF packets to ports for which the DVSTCTR0.UACT bit is set to 1.

When the UTST[3:0] bits are set to 1101b (Test_Force_Enable), the USBHS outputs SOF packets to ports for which the DVSTCTR0.UACT bit is set to 1. In this test mode, the USBHS does not control the hardware related to attach detection, even if it detects a high-speed detach event (DTCH interrupt).

Before setting the UTST[3:0] bits, set the PID[1:0] bits of all pipe control registers to 00b (NAK response). To return to normal USB communication after setting a test mode, issue a hardware reset.

Device controller mode

In device controller mode, set these bits using a SetFeature request from the USB host during high-speed communication. The USBHS does not enter the Suspend state while these bits are 0001b to 0100b. To return to normal USB communication after setting a test mode, issue a hardware reset.

Bit	Symbol	位名称	Description	R/W
b15 to b4	—	Reserved	读取值未定义。写入值应为0。	R/W

UTST[3:0]位（测试模式）

将值写入UTST[3:0]位允许USBHS在高速操作模式下输出USB测试信号。表33.5显示了测试模式操作设置。

Table 33.5 测试模式操作设置

测试模式	UTST[3:0]位设置	
	在设备控制器模式下	在主机控制器模式下
普通手术	0000b	0000b
Test_J	0001b	1001b
Test_K	0010b	1010b
Test_SE0_NAK	0011b	1011b
Test_Packet	0100b	1100b
Test_Force_Enable	—	1101b
Reserved	0101b to 0111b	1110b to 1111b

主机控制器模式

在主机控制器模式下，可在将SYSCFG.DRPD位设置为1后设置这些位。设置UTST[3:0]位后，通过将DVSTCTR0.UACT位设置为1，USBHS将波形输出到USB端口。USBHS还通过在主机控制器模式下设置这些位来为USB端口执行高速端接。

在主机控制器模式下设置UTST[3:0]位：

1. 重置硬件。
2. 开始提供PHY时钟，然后将LPSTS.SUSPENDM位设置为1。
3. 将SYSCFG.DCFM和SYSCFG.DRPD位设置为1。（不需要将SYSCFG.HSE位设置为1。）
4. 将SYSCFG.USBE位设置为1。
5. 根据测试要求设置UTST[3:0]位。
6. 将DVSTCTR0.UACT位设置为1。

假设初始步骤(1)到(6)已经完成，在主机控制器模式下更改UTST[3:0]位：

1. 将DVSTCTR0.UACT和SYSCFG.USBE位设置为0。
2. 将SYSCFG.USBE位设置为1。
3. 根据测试要求设置UTST[3:0]位。
4. 将DVSTCTR0.UACT位设置为1。

当UTST[3:0]位设置为1011b(Test_SE0_NAK)时，USBHS不会将SOF数据包输出到DVSTCTR0.UACT位设置为1的端口。

当UTST[3:0]位设置为1101b(Test_Force_Enable)时，USBHS将SOF数据包输出到DVSTCTR0.UACT位设置为1的端口。在此测试模式下，USBHS不控制与连接检测，即使它检测到高速分离事件（DTCH中断）。

在设置UTST[3:0]位之前，将所有管道控制寄存器的PID[1:0]位设置为00b（NAK响应）。要在设置测试模式后返回正常USB通信，请发出硬件复位。

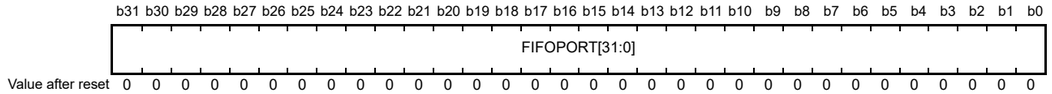
设备控制器模式

在设备控制器模式下，在高速通信期间使用来自USB主机的SetFeature请求设置这些位。当这些位为0001b至0100b时，USBHS不会进入暂停状态。要在设置测试模式后返回正常USB通信，请发出硬件复位。

33.2.7 CFIFO Port Register (CFIFO) D0FIFO Port Register (D0FIFO) D1FIFO Port Register (D1FIFO)

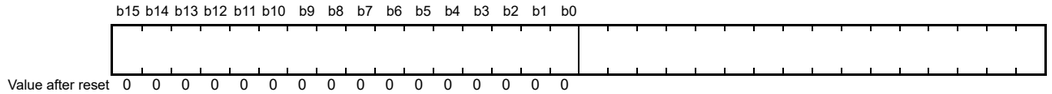
- Access in words

Address(es): USBHS.CFIFO 4006 0014h, USBHS.D0FIFO 4006 0018h, USBHS.D1FIFO 4006 001Ch



- Access in halfwords

Address(es): USBHS.CFIFOL 4006 0014h, USBHS.CFIFOH 4006 0016h, USBHS.D0FIFOL 4006 0018h, USBHS.D0FIFOH 4006 001Ah, USBHS.D1FIFOL 4006 001Ch, USBHS.D1FIFOH 4006 001Eh



- Access in bytes

Address(es): USBHS.CFIFOLL 4006 0014h, USBHS.CFIFOHH 4006 0017h, USBHS.D0FIFOLL 4006 0018h, USBHS.D0FIFOHH 4006 001Bh, USBHS.D1FIFOLL 4006 001Ch, USBHS.D1FIFOHH 4006 001Fh

Bit	Symbol	Bit name	Description	R/W
b31 to b0	FIFOPORT*1	FIFO Port	Read receive data from the FIFO buffer or write transmit data to the FIFO buffer by accessing these bits.	R/W

Note 1. The valid bits depend on the MBW[1:0] and BIGEND settings in the associated port selection register.

Three FIFO ports are provided:

- CFIFO
- D0FIFO
- D1FIFO.

Each FIFO port is configured with:

- A port register (CFIFO, D0FIFO, or D1FIFO) that handles reading of data from the FIFO buffer and writing of data to the FIFO buffer
- A port selection register (CFIFOSEL, D0FIFOSEL, or D1FIFOSEL) that selects the pipe assigned to the FIFO port
- A port control register (CFIFOCTR, D0FIFOCTR, or D1FIFOCTR).

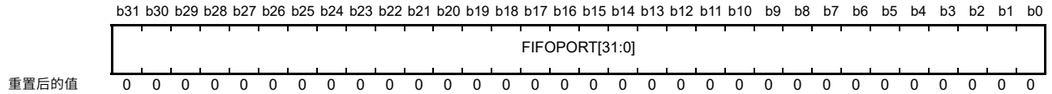
Each FIFO port has the following constraints:

- Access to the FIFO buffer for DCP control transfers is through the CFIFO port
- Access to the FIFO buffer for DMA or DTC transfers is through the D0FIFO or D1FIFO port
- The D0FIFO and D1FIFO ports can also be accessed by the CPU
- When using functions specific to the FIFO port, such as the DMA or DTC transfer function, you cannot change the pipe number selected in the CURPIPE[3:0] bits of the Port Selection Register
- Registers configuring one FIFO port do not affect other FIFO ports
- The same pipe must not be assigned to two or more FIFO ports

33.2.7 CFIFO端口寄存器(CFIFO) D0FIFO端口寄存器(D0FIFO)D1FIFO端口寄存器(D1FIFO)

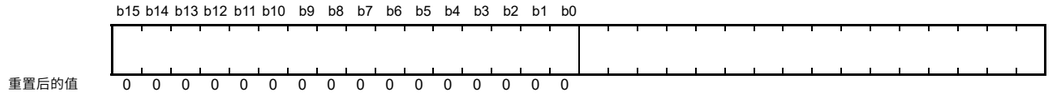
文字访问

Address(es): USBHS.CFIFO 4006 0014h, USBHS.D0FIFO 4006 0018h, USBHS.D1FIFO 4006 001Ch



半字访问

Address(es): USBHS.CFIFOL 4006 0014h, USBHS.CFIFOH 4006 0016h, USBHS.D0FIFOL 4006 0018h, USBHS.D0FIFOH 4006 001Ah, USBHS.D1FIFOL 4006 001Ch, USBHS.D1FIFOH 4006 001Eh



以字节为单位的访问

Address(es): USBHS.CFIFOLL 4006 0014h, USBHS.CFIFOHH 4006 0017h, USBHS.D0FIFOLL 4006 0018h, USBHS.D0FIFOHH 4006 001Bh, USBHS.D1FIFOLL 4006 001Ch, USBHS.D1FIFOHH 4006 001Fh

Bit	Symbol	位名称	Description	R/W
b31 to b0	FIFOPORT*1	FIFO Port	通过访问这些位从FIFO缓冲区读取接收数据或将发送数据写入FIFO缓冲区。	R/W

Note 1. 有效位取决于相关端口选择寄存器中的MBW[1:0]和BIGEND设置。

提供了三个FIFO端口：

- CFIFO
- D0FIFO
- D1FIFO.

每个FIFO端口配置有：

- 处理从FIFO缓冲区读取数据和将数据写入FIFO缓冲区的端口寄存器（CFIFO、D0FIFO或D1FIFO）
- 端口选择寄存器（CFIFOSEL、D0FIFOSEL或D1FIFOSEL），用于选择分配给FIFO端口的管道
- 端口控制寄存器（CFIFOCTR、D0FIFOCTR或D1FIFOCTR）。

每个FIFO端口具有以下约束：

- 通过CFIFO端口访问DCP控制传输的FIFO缓冲区
- 通过D0FIFO或D1FIFO端口访问DMA或DTC传输的FIFO缓冲区
- CPU也可以访问D0FIFO和D1FIFO端口
- 当使用特定于FIFO端口的功能时，例如DMA或DTC传输功能，您无法更改在端口选择寄存器的CURPIPE[3:0]位中选择的管道编号
- 配置一个FIFO端口的寄存器不会影响其他FIFO端口
- 不得将同一管道分配给两个或多个FIFO端口

- There are two FIFO buffer states, one giving access rights to the CPU and the other to the serial interface engine (SIE). When the SIE has access rights, the FIFO buffer cannot be accessed by the CPU.

FIFOPORT bit (FIFO Port)

When the FIFOPORT bit is accessed, the USBHS reads the received data from the FIFO buffer or writes the transmission data to the FIFO buffer. The FIFO port register can be accessed only when the FRDY flag in the associated port control register (CFIFOCTR, D0FIFOCTR, or D1FIFOCTR) is 1.

The valid bits in the FIFO port register depend on the MBW[1:0] and BIGEND settings in the port selection register (CFIFOSEL, D0FIFOSEL, or D1FIFOSEL). See Table 33.6 to Table 33.8.

Table 33.6 Endian operation in 32-bit access (MBW[1:0] = 10b)

BIGEND	CFIFO, D0FIFO, D1FIFO b31 to b24	CFIFO, D0FIFO, D1FIFO b23 to b16	CFIFO, D0FIFO, D1FIFO b15 to b8	CFIFO, D0FIFO, D1FIFO b7 to b0	Remarks
0	Located at N+3	Located at N+2	Located at N+1	Located at N+0	Transmit data is sent from the address N+0. Receive data is stored from the address N+0.
1	Located at N+0	Located at N+1	Located at N+2	Located at N+3	Transmission data is sent from the address N+3. Receive data is stored from the address N+3.

Table 33.7 Endian operation in 16-bit access (MBW[1:0] = 01b)

BIGEND	CFIFOL, D0FIFOL, D1FIFOL b15 to b8	CFIFOL, D0FIFOL, D1FIFOL b7 to b0	CFIFOH, D0FIFOH, D1FIFOH b15 to b8	CFIFOH, D0FIFOH, D1FIFOH b7 to b0	Remarks
0	Access prohibited*1		Located at N+1	Located at N+0	Transmit data is sent from the address N+0. Receive data is stored from the address N+0.
1	Located at N+0	Located at N+1	Access prohibited*1		Transmit data is sent from the address N+1. Receive data is stored from the address N+1.

Note 1. Writing to or reading from these areas is prohibited.

Table 33.8 Endian operation in 8-bit access (MBW[1:0] = 00b)

BIGEND	CFIFOLL, D1FIFOLL, D0FIFOLL	CFIFOHH, D1FIFOHH, D0FIFOHH
0	Access prohibited*1	Located at N+0
1	Located at N+0	Access prohibited*1

Note 1. Writing to or reading from these locations is prohibited.

- 有两种FIFO缓冲区状态，一种授予CPU访问权限，另一种授予串行接口引擎(SIE)。当SIE有访问权限时，CPU不能访问FIFO缓冲区。

FIFOPORT位（FIFO端口）

当访问FIFOPORT位时，USBHS从FIFO缓冲区读取接收数据或将发送数据写入FIFO缓冲区。只有当相关端口控制寄存器（CFIFOCTR、D0FIFOCTR或D1FIFOCTR）中的FRDY标志为1时，才能访问FIFO端口寄存器。

FIFO端口寄存器中的有效位取决于端口选择寄存器（CFIFOSEL、D0FIFOSEL或D1FIFOSEL）中的MBW[1:0]和BIGEND设置。见表33.6至表33.8。

Table 33.6 32位访问中的字节序操作(MBW[1:0]=10b)

BIGEND	CFIFO, D0FIFO, D1FIFO b31 to b24	CFIFO, D0FIFO, D1FIFO b23 to b16	CFIFO, D0FIFO, D1FIFO b15 to b8	CFIFO, D0FIFO, D1FIFO b7 to b0	Remarks
0	位于N+3	位于N+2	位于N+1	位于N+0	发送数据从地址N+0发送。 接收数据从地址N+0开始存储。
1	位于N+0	位于N+1	位于N+2	位于N+3	传输数据从地址N+3发送。 接收数据从地址N+3开始存储。

Table 33.7 16位访问中的字节序操作(MBW[1:0]=01b)

BIGEND	CFIFOL, D0FIFOL, D1FIFOL b15 to b8	CFIFOL, D0FIFOL, D1FIFOL b7 to b0	CFIFOH, D0FIFOH, D1FIFOH b15 to b8	CFIFOH, D0FIFOH, D1FIFOH b7 to b0	Remarks
0	Access prohibited*1		位于N+1	位于N+0	发送数据从地址N+0发送。 接收数据从地址N+0开始存储。
1	位于N+0	位于N+1	Access prohibited*1		发送数据从地址N+1发送。 接收数据从地址N+1开始存储。

Note 1. 禁止向这些区域写入或读取。

Table 33.8 8位访问中的字节序操作(MBW[1:0]=00b)

BIGEND	CFIFOLL, D1FIFOLL, D0FIFOLL	CFIFOHH, D1FIFOHH, D0FIFOHH
0	Access prohibited*1	位于N+0
1	位于N+0	Access prohibited*1

Note 1. 禁止向这些位置写入或读取。

33.2.8 CFIFO Port Selection Register (CFIFOSEL)

Address(es): USBHS.CFIFOSEL 4006 0020h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RCNT	REW	—	—	MBW[1:0]		—	BIGEND	—	—	ISEL	—	CURPIPE[3:0]			
Value after reset:	0	0	x	x	0	0	x	0	x	x	0	x	0	0	0	0

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b3 to b0	CURPIPE[3:0]	FIFO Port Access Pipe Specification	b3 b0 0 0 0 0: DCP (default control pipe) 0 0 0 1: Pipe 1 0 0 1 0: Pipe 2 0 0 1 1: Pipe 3 0 1 0 0: Pipe 4 0 1 0 1: Pipe 5 0 1 1 0: Pipe 6 0 1 1 1: Pipe 7 1 0 0 0: Pipe 8 1 0 0 1: Pipe 9. Other settings are prohibited.	R/W
b4	—	Reserved	The read value is undefined. The write value should be 0.	R/W
b5	ISEL	FIFO Port Access Direction when DCP Is Selected	0: Select reading from the FIFO buffer 1: Select writing to the FIFO buffer.	R/W
b7, b6	—	Reserved	The read value is undefined. The write value should be 0.	R/W
b8	BIGEND	FIFO Port Endian Control	0: Little endian 1: Big endian.	R/W
b9	—	Reserved	The read value is undefined. The write value should be 0.	R/W
b11, b10	MBW[1:0]	CFIFO Port Access Bit Width	b11 b10 0 0: 8-bit width 0 1: 16-bit width 1 0: 32-bit width 1 1: Setting prohibited.	R/W
b13, b12	—	Reserved	The read value is undefined. The write value should be 0.	R/W
b14	REW	Buffer Pointer Rewind	0: Do not rewind buffer pointer (Writing 0 has no effect.) 1: Rewind buffer pointer.	W
b15	RCNT	Read Count Mode	0: Clear DTLN[11:0] flags in the FIFO port control register to 000h when all receive data is read from CFIFO 1: Decrement DTLN[11:0] flags each time receive data is read from CFIFO.	R/W

Do not specify the same pipe number in the CURPIPE[3:0] bits in the CFIFOSEL, D0FIFOSEL, and D1FIFOSEL registers.

Do not change the pipe number while DMA or DTC transfer is enabled.

CURPIPE[3:0] bits (FIFO Port Access Pipe Specification)

The CURPIPE[3:0] bits specify the pipe number used to read or write data through the CFIFO port. After writing to these bits, read them to check that the written value agrees with the read value before proceeding to the next process. Do not set the same pipe number to the CURPIPE[3:0] bits in CFIFOSEL, D0FIFOSEL, and D1FIFOSEL.

During FIFO buffer access, the pipe specification is maintained until the access is complete, even if the software attempts to change the CURPIPE[3:0] setting. Access continues after the current value is written back to the CURPIPE[3:0] bits.

ISEL bit (FIFO Port Access Direction when DCP Is Selected)

After writing a new value to the ISEL bit while the DCP is the selected pipe, read this bit to check that the written value agrees with the read value before proceeding to the next process. Set the ISEL and CURPIPE[3:0] bits simultaneously.

33.2.8 CFIFO端口选择寄存器(CFIFOSEL)

Address(es): USBHS.CFIFOSEL 4006 0020h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RCNT	REW	—	—	MBW[1:0]		—	BIGEND	—	—	ISEL	—	CURPIPE[3:0]			
重置后的值：	0	0	x	x	0	0	x	0	x	x	0	x	0	0	0	0

x: Undefined

Bit	Symbol	位名称	Description	R/W
b3 to b0	CURPIPE[3:0]	FIFO端口访问管道 Specification	b3 b0 0 0 0 0: DCP (default control pipe) 0 0 0 1: Pipe 1 0 0 1 0: Pipe 2 0 0 1 1: Pipe 3 0 1 0 0: Pipe 4 0 1 0 1: Pipe 5 0 1 1 0: Pipe 6 0 1 1 1: Pipe 7 1 0 0 0: Pipe 8 01：管道9。禁止其他设置。	R/W
b4	—	Reserved	读取值未定义。写入值应为0。	R/W
b5	ISEL	选择DCP时的FIFO端口访问方向	0：选择从FIFO缓冲区读取1：选择写入FIFO缓冲区。	R/W
b7, b6	—	Reserved	读取值未定义。写入值应为0。	R/W
b8	BIGEND	FIFO端口字节序控制	0：小端1：大端。	R/W
b9	—	Reserved	读取值未定义。写入值应为0。	R/W
b11, b10	MBW[1:0]	CFIFO端口访问位宽	b11 b10 0 0: 8-bit width 0 1: 16-bit width 1 0: 32-bit width 1 1：禁止设置。	R/W
b13, b12	—	Reserved	读取值未定义。写入值应为0。	R/W
b14	REW	缓冲区指针倒带	0：不回退缓冲区指针（写入0无效。）1：回退缓冲区指针。	W
b15	RCNT	读取计数模式	0：当从CFIFO读取所有接收数据时，将FIFO端口控制寄存器中的DTLN[11:0]标志清零1：每次从CFIFO读取接收数据时，递减DTLN[11:0]标志。	R/W

不要在CFIFOSEL、D0FIFOSEL和D1FIFOSEL寄存器的CURPIPE[3:0]位中指定相同的管道编号。

启用DMA或DTC传输时不要更改管道编号。

CURPIPE[3:0]位（FIFO端口访问管道规范）

CURPIPE[3:0]位指定用于通过CFIFO端口读取或写入数据的管道号。写入这些位后，读取它们以检查写入的值是否与读取的值一致，然后再进行下一个过程。不要为CFIFOSEL、D0FIFOSEL和D1FIFOSEL中的CURPIPE[3:0]位设置相同的管道编号。

在FIFO缓冲区访问期间，管道规范一直保持到访问完成，即使软件尝试更改CURPIPE[3:0]设置。将当前值写回CURPIPE[3:0]位后继续访问。

ISEL位（选择DCP时的FIFO端口访问方向）

在DCP为选定管道时向ISEL位写入新值后，读取该位以检查写入的值是否与读取的值一致，然后再进行下一个过程。同时设置ISEL和CURPIPE[3:0]位。

BIGEND bit (FIFO Port Endian Control)

Use the BIGEND bit to set the byte endian order of the CFIFO port to be the same as that selected in the endian selection register (MDE).

MBW[1:0] bits (CFIFO Port Access Bit Width)

The MBW[1:0] bits specify the bit width for accessing the CFIFO port.

When the selected pipe is receiving, after a write to these bits starts a data read from the FIFO buffer, do not change the bits until all of the data is read. When reading the FIFO buffer, read with the access size set in MBW.

When the selected pipe is transmitting, set the CURPIPE[3:0] and MBW[1:0] bits simultaneously. The bit width cannot be changed from 8-bit to 16- or 32-bit, or from 16-bit to 32-bit while data is being written to the FIFO buffer.

An odd number of bytes can also be written through byte-access control even when 16- or 32-bit width is selected.

REW bit (Buffer Pointer Rewind)

The REW bit specifies whether or not to rewind the buffer pointer.

When the selected pipe is receiving, setting this bit to 1 while the FIFO buffer is being read allows re-reading of the FIFO buffer from the first data. In double-buffering when reading is already in progress, this setting enables reading either FIFO buffer from the first entry.

Do not set this bit to 1 while simultaneously changing the CURPIPE[3:0] bits. Before setting the bit to 1, always check that the FRDY flag is 1.

To rewrite to the FIFO buffer from the first data for the transmitting pipe, use the BCLR bit.

RCNT bit (Read Count Mode)

When the RCNT bit set to 0, the USBHS clears the CFIFOCTR.DTLN[11:0] flags to 0 on finishing reading all of the received data in the FIFO buffer assigned to the pipe specified in the CURPIPE[3:0] bits, or after reading a single plane in double buffer mode.

With this bit set to 1, the USBHS decrements the value in the CFIFOCTR.DTLN[11:0] flags each time it reads data received from the FIFO buffer assigned to the pipe specified in the CURPIPE[3:0] bits.

33.2.9 D0FIFO Port Selection Register (D0FIFOSEL) D1FIFO Port Selection Register (D1FIFOSEL)

Address(es): USBHS.D0FIFOSEL 4006 0028h, USBHS.D1FIFOSEL 4006 002Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RCNT	REW	DCLRM	DREQE	MBW[1:0]		—	BIGEND	—	—	—	—	CURPIPE[3:0]			
Value after reset:	0	0	0	0	0	0	x	0	x	x	x	x	0	0	0	0

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b3 to b0	CURPIPE[3:0]	FIFO Port Access Pipe Specification	b3 b0 0 0 0 0: No pipe specification 0 0 0 1: Pipe 1 0 0 1 0: Pipe 2 0 0 1 1: Pipe 3 0 1 0 0: Pipe 4 0 1 0 1: Pipe 5 0 1 1 0: Pipe 6 0 1 1 1: Pipe 7 1 0 0 0: Pipe 8 1 0 0 1: Pipe 9. Other settings are prohibited.	R/W
b7 to b4	—	Reserved	The read value is undefined. The write value should be 0.	R/W

BIGEND位（FIFO端口字节序控制）

使用BIGEND位将CFIFO端口的字节字节序设置为与在字节序选择寄存器(MDE)中选择的相同。

MBW[1:0]位（CFIFO端口访问位宽）

MBW[1:0]位指定访问CFIFO端口的位宽。

当所选管道正在接收时，在写入这些位后开始从FIFO缓冲区读取数据，在读取所有数据之前不要更改这些位。读取FIFO缓冲区时，读取以MBW为单位设置的访问大小。

当所选管道正在传输时，同时设置CURPIPE[3:0]和MBW[1:0]位。当数据写入FIFO缓冲区时，位宽不能从8位更改为16位或32位，或从16位更改为32位。

即使选择了16位或32位宽度，也可以通过字节访问控制写入奇数个字节。

REW位（缓冲区指针倒带）

REW位指定是否回绕缓冲区指针。

当所选管道正在接收时，在读取FIFO缓冲区时将此位设置为1允许从第一个数据重新读取FIFO缓冲区。在读取已经在进行时的双缓冲中，此设置允许从第一个条目读取任一FIFO缓冲区。

请勿在同时更改CURPIPE[3:0]位时将此位设置为1。在将该位设置为1之前，请始终检查FRDY标志是否为1。

要从传输管道的第一个数据重写FIFO缓冲区，请使用BCLR位。

RCNT位（读取计数模式）

当RCNT位设置为0时，USBHS在完成读取分配给CURPIPE[3:0]位指定的管道的FIFO缓冲区中的所有接收数据后，将CFIFOCTR.DTLN[11:0]标志清除为0，或在双缓冲模式下读取单个平面后。

该位设置为1时，USBHS每次读取从分配给CURPIPE[3:0]位指定的管道的FIFO缓冲区接收到的数据时都会递减CFIFOCTR.DTLN[11:0]标志中的值。

33.2.9 D0FIFO端口选择寄存器（D0FIFOSEL）D1FIFO端口选择寄存器（D1FIFOSEL）

Address(es): USBHS.D0FIFOSEL 4006 0028h, USBHS.D1FIFOSEL 4006 002Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RCNT	REW	DCLRM	DREQE	MBW[1:0]		—	BIGEND	—	—	—	—	CURPIPE[3:0]			
重置后的值：	0	0	0	0	0	0	x	0	x	x	x	x	0	0	0	0

x: Undefined

Bit	Symbol	位名称	Description	R/W
b3 to b0	CURPIPE[3:0]	FIFO端口访问管道 Specification	b3 b0 0 0 0 0：无管道规格 0 0 0 1: Pipe 1 0 0 1 0: Pipe 2 0 0 1 1: Pipe 3 0 1 0 0: Pipe 4 0 1 0 1: Pipe 5 0 1 1 0: Pipe 6 0 1 1 1: Pipe 7 1 0 0 0: Pipe 8 01：管道9。禁止其他设置。	R/W
b7 to b4	—	Reserved	读取值未定义。写入值应为0。	R/W

Bit	Symbol	Bit name	Description	R/W
b8	BIGEND	FIFO Port Endian Control	0: Little endian 1: Big endian.	R/W
b9	—	Reserved	The read value is undefined. The write value should be 0.	R/W
b11, b10	MBW[1:0]	FIFO Port Access Bit Width	b11 b10 0 0: 8-bit width 0 1: 16-bit width 1 0: 32-bit width 1 1: Setting prohibited.	R/W
b12	DREQE	DMA/DTC Transfer Request Enable	0: Disable DMA/DTC transfer request. 1: Enable DMA/DTC transfer request.	R/W
b13	DCLRM	Auto FIFO Buffer Clear Mode after Specified Pipe is Read	0: Disable auto buffer clear mode 1: Enable auto buffer clear mode.	R/W
b14	REW	Buffer Pointer Rewind	0: Do not rewind buffer pointer (writing 0 has no effect) 1: Rewind buffer pointer.	W
b15	RCNT	Read Count Mode	0: Clear DTLN[11:0] flags in the FIFO port control register to 000h when all receive data is read from DnFIFO (after read of a single plane in double buffer mode) 1: Decrement DTLN[11:0] flags each time receive data is read from DnFIFO. n = 0, 1.	R/W

Do not specify the same pipe number in the CURPIPE[3:0] bits in the CFIFOSEL, D0FIFOSEL, and D1FIFOSEL registers. When the CURPIPE[3:0] bits in the D0FIFOSEL and D1FIFOSEL registers are set to 0000b, no pipe is selected.

Do not change the pipe number while DMA or DTC transfer is enabled.

CURPIPE[3:0] bits (FIFO Port Access Pipe Specification)

The CURPIPE[3:0] bits specify the pipe number used to read or write data through the DnFIFO port. After writing to these bits, read them to check that the written value agrees with the read value before proceeding to the next process. Do not set the same pipe number to the CURPIPE[3:0] bits in CFIFOSEL, D0FIFOSEL, and D1FIFOSEL.

During FIFO buffer access, the pipe specification is maintained until the access is complete, even if the software attempts to change the CURPIPE[3:0] setting. Access continues after the current value is written back to the CURPIPE[3:0] bits.

BIGEND bit (FIFO Port Endian Control)

Use the BIGEND bit to set the byte endian order of the D0FIFO or D1FIFO port to be the same as that selected in the endian selection register (MDE).

MBW[1:0] bits (FIFO Port Access Bit Width)

The MBW[1:0] bits specify the bit width for accessing the DnFIFO port.

When the selected pipe is receiving, after a write to these bits starts a data read from the FIFO buffer, do not change the bits until all of the data is read. When reading the FIFO buffer, read with the access size set in MBW.

When the selected pipe is transmitting, set the CURPIPE[3:0] and MBW[1:0] bits simultaneously. The bit width cannot be changed from 8-bit to 16- or 32-bit, or from 16-bit to 32-bit while data is being written to the FIFO buffer.

An odd number of bytes can also be written through byte-access control even when 16- or 32-bit width is selected.

DREQE bit (DMA/DTC Transfer Request Enable)

The DREQE bit enables or disables issuing of DMA or DTC transfer requests. Only change the settings of DREQE bit when the CURPIPE[3:0] bits are 0000b.

To enable DMA or DTC transfer requests, set this bit to 1 after setting the CURPIPE[3:0] bits to 0000b, and then set the CURPIPE[3:0] bits to the PIPE number for the transfer.

DCLRM bit (Auto FIFO Buffer Clear Mode after Specified Pipe is Read)

The DCLRM bit enables or disables automatic FIFO buffer clearing after data in the selected pipe is read.

When this bit is set to 1, on receiving a zero-length packet while the FIFO buffer assigned to the selected pipe is empty,

Bit	Symbol	位名称	Description	R/W
b8	BIGEND	FIFO端口字节序控制	0：小端1：大端。	R/W
b9	—	Reserved	读取值未定义。写入值应为0。	R/W
b11, b10	MBW[1:0]	FIFO端口访问位宽	b11 b10 0 0: 8-bit width 0 1: 16-bit width 1 0: 32-bit width 1 1：禁止设置。	R/W
b12	DREQE	DMADTC传输请求Enable	0：禁用DMADTC传输请求。1：启用DMADTC传输请求。	R/W
b13	DCLRM	读取指定管道后自动FIFO缓冲区清除模式	0：禁用自动缓冲区清除模式1：启用自动缓冲区清除模式。	R/W
b14	REW	缓冲区指针倒带	0：不回退缓冲区指针（写0无效）1：回退缓冲区指针。	W
b15	RCNT	读取计数模式	0：当从DnFIFO读取所有接收数据时（在双缓冲模式下读取单个平面后），将FIFO端口控制寄存器中的DTLN[11:0]标志清零1：每次递减DTLN[11:0]标志接收数据从DnFIFO中读取。n=0 1。	R/W

不要在CFIFOSEL、D0FIFOSEL和D1FIFOSEL寄存器的CURPIPE[3:0]位中指定相同的管道编号。当D0FIFOSEL和D1FIFOSEL寄存器中的CURPIPE[3:0]位设置为0000b时，不选择管道。

启用DMA或DTC传输时不要更改管道编号。

CURPIPE[3:0]位（FIFO端口访问管道规范）

CURPIPE[3:0]位指定用于通过DnFIFO端口读取或写入数据的管道编号。写入这些位后，读取它们以检查写入的值是否与读取的值一致，然后再进行下一个过程。不要为CFIFOSEL、D0FIFOSEL和D1FIFOSEL中的CURPIPE[3:0]位设置相同的管道编号。

在FIFO缓冲区访问期间，管道规范一直保持到访问完成，即使软件尝试更改CURPIPE[3:0]设置。将当前值写回CURPIPE[3:0]位后继续访问。

BIGEND位（FIFO端口字节序控制）

使用BIGEND位将D0FIFO或D1FIFO端口的字节字节序设置为与在字节序选择寄存器(MDE)中选择的相同。

MBW[1:0]位（FIFO端口访问位宽）

MBW[1:0]位指定访问DnFIFO端口的位宽。

当所选管道正在接收时，在写入这些位后开始从FIFO缓冲区读取数据，在读取所有数据之前不要更改这些位。读取FIFO缓冲区时，读取以MBW为单位设置的访问大小。

当所选管道正在传输时，同时设置CURPIPE[3:0]和MBW[1:0]位。当数据写入FIFO缓冲区时，位宽不能从8位更改为16位或32位，或从16位更改为32位。

即使选择了16位或32位宽度，也可以通过字节访问控制写入奇数个字节。

DREQE位（DMADTC传输请求使能）

DREQE位启用或禁用DMA或DTC传输请求的发出。仅当CURPIPE[3:0]位为0000b时更改DREQE位的设置。

要启用DMA或DTC传输请求，请在将CURPIPE[3:0]位设置为0000b后将此位设置为1，然后将CURPIPE[3:0]位到用于传输的PIPE编号。

DCLRM位（读取指定管道后自动FIFO缓冲区清除模式）

在读取所选管道中的数据后，DCLRM位启用或禁用自动FIFO缓冲区清除。

当该位设置为1时，在分配给所选管道的FIFO缓冲区为空时接收到长度为零的数据包时，

or when reading of a received short packet is complete while the PIPECFG.BFRE bit is 1, the USBHS sets the BCLR bit in the FIFO port control register to 1.

When using the USBHS with the SOFCFG.BRDYM bit set to 1, set this bit to 0.

REW bit (Buffer Pointer Rewind)

The REW bit specifies whether or not to rewind the buffer pointer.

When the selected pipe is receiving, setting this bit to 1 while the FIFO buffer is being read allows re-reading of the FIFO buffer from the first data. In double-buffering when reading is already in progress, this setting enables reading either FIFO buffer from the first entry.

Do not set this bit to 1 while simultaneously changing the CURPIPE[3:0] bits. Before setting the bit to 1, always check that the FRDY flag is 1.

To rewrite to the FIFO buffer from the first data for the transmitting pipe, use the BCLR bit.

RCNT bit (Read Count Mode)

When the RCNT bit set to 0, the USBHS clears the DnFIFOCTR.DTLN[11:0] flags (n = 0, 1) to 0 on finishing reading all of the received data in the FIFO buffer assigned to the pipe specified in the CURPIPE[3:0] bits, or after reading a single plane in double buffer mode.

With this bit set to 1, the USBHS decrements the value in the CFIFOCTR.DTLN[11:0] flags each time it reads data received from the FIFO buffer assigned to the pipe specified in the CURPIPE[3:0] bits. When accessing DnFIFO with the PIPECFG.BFRE bit set to 1, set the RCNT bit to 0.

33.2.10 CFIFO Port Control Register (CFIFOCTR)
D0FIFO Port Control Register (D0FIFOCTR)
D1FIFO Port Control Register (D1FIFOCTR)

Address(es): USBHS.CFIFOCTR 4006 0022h, USBHS.D0FIFOCTR 4006 002Ah, USBHS.D1FIFOCTR 4006 002Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BVAL	BCLR	FRDY	—	DTLN[11:0]											
Value after reset:	0	0	0	x	0	0	0	0	0	0	0	0	0	0	0	0

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b11 to b0	DTLN[11:0]	Receive Data Length Flag	Receive data length The meaning of the values differs depending on the RCNT bit setting in the port selection register. For details, see the description of the DTLN[11:0] bits.	R
b12	—	Reserved	The read value is undefined. The write value should be 0.	R/W
b13	FRDY	FIFO Port Ready Flag	0: FIFO port access disabled 1: FIFO port access enabled.	R
b14	BCLR	CPU Buffer Clear	0: No operation 1: Clear FIFO buffer on the CPU side. Writing 0 to this bit has no effect. This bit is read as 0.	R/W
b15	BVAL	FIFO Buffer Valid Flag	0: Invalid (writing 0 has no effect) 1: Writing ended. Set this bit to 1 when data is completely written to the FIFO buffer on the CPU side for the selected pipe (CURPIPE[3:0] setting).	R/W

The CFIFOCTR, D0FIFOCTR, and D1FIFOCTR registers correspond to the CFIFO, D0FIFO, and D1FIFO buffers.

DTLN[11:0] flags (Receive Data Length Flag)

The DTLN[11:0] flags indicate the length of the receive data.

或者当PIPECFG.BFRE位为1时完成读取接收到的短数据包时，USBHS将FIFO端口控制寄存器中的BCLR位设置为1。

当使用SOFCFG.BRDYM位设置为1的USBHS时，将此位设置为0。

REW位（缓冲区指针倒带）

REW位指定是否回绕缓冲区指针。

当所选管道正在接收时，在读取FIFO缓冲区时将此位设置为1允许从第一个数据重新读取FIFO缓冲区。在读取已经在进行时的双缓冲中，此设置允许从第一个条目读取任一FIFO缓冲区。

请勿在同时更改CURPIPE[3:0]位时将此位设置为1。在将该位设置为1之前，请始终检查FRDY标志是否为1。

要从传输管道的第一个数据重写FIFO缓冲区，请使用BCLR位。

RCNT位（读取计数模式）

当RCNT位设置为0时，USBHS清除DnFIFOCTR.DTLN[11:0]标志(n=0 1)为0完成读取分配给CURPIPE中指定管道的FIFO缓冲区中的所有接收数据[3:0]位，或在双缓冲模式下读取单个平面后。

该位设置为1时，USBHS每次读取从分配给CURPIPE[3:0]位指定的管道的FIFO缓冲区接收到的数据时都会递减CFIFOCTR.DTLN[11:0]标志中的值。当PIPECFG.BFRE位设置为1访问DnFIFO时，将RCNT位设置为0。

33.2.10 CFIFO端口控制寄存器(CFIFOCTR)
D0FIFO端口控制寄存器(D0FIFOCTR)D1FIFO端口控制寄存器(D1FIFOCTR)

Address(es): USBHS.CFIFOCTR 4006 0022h, USBHS.D0FIFOCTR 4006 002Ah, USBHS.D1FIFOCTR 4006 002Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BVAL	BCLR	FRDY	—	DTLN[11:0]											
重置后的值：	0	0	0	x	0	0	0	0	0	0	0	0	0	0	0	0

x: Undefined

Bit	Symbol	位名称	Description	R/W
b11 to b0	DTLN[11:0]	接收数据长度标志	接收数据长度 这些值的含义因端口选择寄存器中的RCNT位设置而异。有关详细信息，请参见DTLN[11:0]位的说明。	R
b12	—	Reserved	读取值未定义。写入值应为0。	R/W
b13	FRDY	FIFO端口就绪标志	0：禁止FIFO端口访问1：使能FIFO端口访问。	R
b14	BCLR	CPU缓冲区清除	0：无操作1：清除CPU端的FIFO缓冲区。向该位写入0无效。该位读为0。	R/W
b15	BVAL	FIFO缓冲区有效标志	0：无效（写入0无效）1：写入结束。当数据完全写入所选管道的CPU端的FIFO缓冲区时，将此位设置为1（CURPIPE[3:0]设置）。	R/W

CFIFOCTR、D0FIFOCTR和D1FIFOCTR寄存器对应于CFIFO、D0FIFO和D1FIFO缓冲区。

DTLN[11:0]标志（接收数据长度标志）

DTLN[11:0]标志指示接收数据的长度。

While the FIFO buffer is being read, the DTLN[11:0] bits indicate different values depending on the DnFIFOSEL.RCNT bit (n = 0, 1), as follows:

- RCNT = 0:
  The USBHS sets the DTLN[11:0] flags to indicate the length of the receive data until the CPU or DMA/DTC has read all of the received data in the FIFO buffer (or until it has read a single plane in double buffer mode).
  While the PIPECFG.BFRE bit is 1, the USBHS retains the length of the receive data until the BCLR bit is set to 1, even after all the data is read.
- RCNT = 1:
  The USBHS decrements the value indicated in the DTLN[11:0] flags each time the CPU or DMA/DTC reads the receive data from the FIFO buffer. (The value is decremented by 1 when MBW[1:0] = 00b, by 2 when MBW[1:0] = 01b, and by 4 when MBW[1:0] = 10b.)
  The USBHS sets these flags to 0 when all the data is read from the FIFO buffer. In double buffer mode, if data is received in one FIFO buffer plane before all of the data is read from the other plane, the USBHS sets these bits to indicate the length of the receive data in the latter plane when all of the data is read from the former plane.
  When the RCNT bit is 1, reading the DTLN[11:0] flags while the FIFO buffer is being read returns the latest value within 150 ns after the FIFO port read cycle.

FRDY flag (FIFO Port Ready Flag)

The FRDY flag indicates whether the FIFO port can be accessed by the CPU or DMA/DTC.

In the following cases, the USBHS sets the FRDY flag to 1 but data cannot be read through the FIFO port because there is no data to be read:

- A zero-length packet is received when the FIFO buffer assigned to the selected pipe is empty
- A short packet is received and the data is completely read while the PIPECFG.BFRE bit is 1.

In these cases, set the BCLR bit to 1 to clear the FIFO buffer, and enable transmission and reception of the next data.

BCLR bit (CPU Buffer Clear)

Set the BCLR bit to 1 to clear the FIFO buffer on the CPU for the selected pipe.

When double buffer mode is set for the FIFO buffer assigned to the selected pipe, the USBHS clears only one plane of the FIFO buffer even when both planes are read-enabled.

When the DCP is the selected pipe, setting the BCLR bit to 1 allows the USBHS to clear both sets of FIFO buffers regardless of whether the CPU or SIE has access rights. To clear the buffer when the SIE has access rights, set the DCPCTR.PID[1:0] bits to 00b (NAK response) before setting the BCLR bit to 1.

When the selected pipe is not the DCP, only write 1 to the BCLR bit while the FRDY flag in the FIFO port control register is 1 (set by the USBHS).

BVAL bit (FIFO Buffer Valid Flag)

Set the BVAL bit to 1 when data is completely written to the FIFO buffer on the CPU for the pipe selected in CURPIPE[3:0].

When the selected pipe is transmitting, set this bit to 1 in the following cases:

- To transmit a short packet, set this bit to 1 after data is written
- To transmit a zero-length packet, set this bit to 1 before data is written to the FIFO buffer
- Set this bit to 1 after the specified number of data bytes is written for the pipe in continuous transfer mode, where the number is a natural integer multiple of the maximum packet size and less than the buffer size.

The USBHS then switches the FIFO buffer from the CPU side to the SIE side, enabling transmission.

When the selected pipe is in use for transmission, simultaneously setting the BVAL flag and the BCLR bit to 1 causes the USBHS to clear the data that is already written and enables transmission of a zero-length packet. When data of the maximum packet size is written for the pipe in non-continuous transfer mode, the USBHS sets this bit to 1 and switches the FIFO buffer from the CPU side to the SIE side, enabling transmission.

Only write 1 to the BVAL flag while the FRDY bit is 1 (set by the USBHS). When the selected pipe is receiving, do not

在读取FIFO缓冲区时，DTLN[11:0]位指示不同的值，具体取决于DnFIFOSEL.RCNT位(n=0 1)，如下所示：

- RCNT = 0:
  USBHS设置DTLN[11:0]标志以指示接收数据的长度，直到CPU或DMADTC已读取FIFO缓冲区中的所有接收数据（或直到它在双缓冲区模式下读取单个平面）.当PIPECFG.BFRE位为1时，USBHS将保留接收数据的长度，直到BCLR位设置为1，即使在读取所有数据之后也是如此。
- RCNT = 1:
  每次CPU或DMADTC从FIFO缓冲区读取接收数据时，USBHS都会递减DTLN[11:0]标志中指示的值。（当MBW[1:0]=00b时该值减1，当MBW[1:0]=01b时减2，当MBW[1:0]=10b时减4。）USBHS将这些标志设置为0当从FIFO缓冲区中读取所有数据时。在双缓冲模式下，如果在一个FIFO缓冲平面中的所有数据从另一个平面读取之前接收到数据，则USBHS设置这些位以指示在读取所有数据时后一个平面中接收数据的长度从前飞机。当RCNT位为1时，在读取FIFO缓冲区时读取DTLN[11:0]标志会在FIFO端口读取周期后150ns内返回最新值。

FRDY标志（FIFO端口就绪标志）

FRDY标志指示CPU或DMADTC是否可以访问FIFO端口。

在以下情况下，USBHS将FRDY标志设置为1，但由于没有数据可读取，因此无法通过FIFO端口读取数据：

- 当分配给所选管道的FIFO缓冲区为空时，接收到零长度数据包
- 当PIPECFG.BFRE位为1时，接收到一个短数据包并完全读取数据。

在这些情况下，将BCLR位设置为1以清除FIFO缓冲区，并启用下一个数据的发送和接收。

BCLR位（CPU缓冲区清除）

将BCLR位设置为1以清除CPU上所选管道的FIFO缓冲区。

当为分配给所选管道的FIFO缓冲区设置双缓冲区模式时，USBHS仅清除FIFO缓冲区的一个平面，即使两个平面都已启用读取。

当DCP为选定管道时，将BCLR位设置为1允许USBHS清除两组FIFO缓冲区，而不管CPU或SIE是否具有访问权限。要在SIE具有访问权限时清除缓冲区，请将DCPCTR.PID[1:0]位设置为00b（NAK响应），然后再将BCLR位设置为1。

当所选管道不是DCP时，仅在FIFO端口控制寄存器中的Frdy标志为1（由USBH设置）时，仅将1个写入BCLR位。

BVAL位（FIFO缓冲区有效标志）

当数据完全写入CPU上的FIFO缓冲区时，将BVAL位设置为1，用于
CURPIPE[3:0].

当所选管道正在传输时，在以下情况下将此位设置为1：

- 要发送短数据包，请在写入数据后将此位设置为1
- 要发送长度为零的数据包，请在将数据写入FIFO缓冲区之前将此位设置为1
- 在连续传输模式下为管道写入指定数量的数据字节后，将此位设置为1，其中该数字是最大数据包大小的自然整数倍，并且小于缓冲区大小。

然后USBHS将FIFO缓冲区从CPU侧切换到SIE侧，从而启用传输。

当所选管道用于传输时，同时将BVAL标志和BCLR位设置为1会导致USBHS清除已写入的数据并启用零长度数据包的传输。当在非连续传输模式下为管道写入最大数据包大小的数据时，USBHS将该位设置为1，并将FIFO缓冲区从CPU侧切换到SIE侧，从而启用传输。

仅在FRDY位为1（由USBHS设置）时将1写入BVAL标志。Whentheselectedpipeisreceiving donot

set the BVAL flag to 1.

33.2.11 Interrupt Enable Register 0 (INTENB0)

Address(es): USBHS.INTENB0 4006 0030h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	VBSE	RSME	SOFE	DVSE	CTRE	BEMPE	NRDYE	BRDYE	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b7 to b0	—	Reserved	The read value is undefined. The write value should be 0.	R/W
b8	BRDYE	Buffer Ready Interrupt Request Enable	0: Disable interrupt request 1: Enable interrupt request.	R/W
b9	NRDYE	Buffer Not Ready Response Interrupt Request Enable	0: Disable interrupt request 1: Enable interrupt request.	R/W
b10	BEMPE	Buffer Empty Interrupt Request Enable	0: Disable interrupt request 1: Enable interrupt request.	R/W
b11	CTRE	Control Transfer Stage Transition Interrupt Request Enable	0: Disable interrupt request 1: Enable interrupt request.	R/W
b12	DVSE	Device State Transition Interrupt Request Enable	0: Disable interrupt request 1: Enable interrupt request.	R/W
b13	SOFE	Frame Number Update Interrupt Request Enable	0: Disable interrupt request 1: Enable interrupt request.	R/W
b14	RSME	Resume Interrupt Request Enable	0: Disable interrupt request 1: Enable interrupt request.	R/W
b15	VBSE	VBUS Interrupt Request Enable	0: Disable interrupt request 1: Enable interrupt request.	R/W

Note: The RSME, DVSE, and CTRE bits can only be set to 1 in device controller mode. Do not set these bits to 1 in host controller mode.

When a status flag in the INTSTS0 register sets to 1 and the associated interrupt request enable bit setting in the INTENB0 register is 1, the USBHS issues a USBHS interrupt request.

Regardless of the INTENB0 register setting, the status flag in the INTSTS0 register sets to 1 in response to a state change that satisfies the associated condition.

When an interrupt request enable bit in the INTENB0 register is switched from 0 to 1 while the associated status flag in the INTSTS0 register is set to 1, a USBHS interrupt is requested.

将BVAL标志设置为1。

33.2.11 中断使能寄存器0(INTENB0)

Address(es): USBHS.INTENB0 4006 0030h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	VBSE	RSME	SOFE	DVSE	CTRE	BEMPE	NRDYE	BRDYE	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b7 to b0	—	Reserved	读取值未定义。写入值应为0。	R/W
b8	BRDYE	缓冲区就绪中断请求 Enable	0：禁止中断请求1：允许中断请求。	R/W
b9	NRDYE	缓冲区未就绪响应中断请求使能	0：禁止中断请求1：允许中断请求。	R/W
b10	BEMPE	缓冲区空中断请求 Enable	0：禁止中断请求1：允许中断请求。	R/W
b11	CTRE	控制转移阶段转换中断请求 Enable	0：禁止中断请求1：允许中断请求。	R/W
b12	DVSE	设备状态转换中断请求启用	0：禁止中断请求1：允许中断请求。	R/W
b13	SOFE	帧号更新中断请求启用	0：禁止中断请求1：允许中断请求。	R/W
b14	RSME	恢复中断请求 Enable	0：禁止中断请求1：允许中断请求。	R/W
b15	VBSE	VBUS中断请求使能	0：禁止中断请求1：允许中断请求。	R/W

Note: RSME、DVSE和CTRE位只能在设备控制器模式下设置为1。不要在主机控制器模式下将这些位设置为1。

当INTSTS0寄存器中的状态标志设置为1并且相关的中断请求使能位设置在INTENB0寄存器为1，USBHS发出USBHS中断请求。

无论INTENB0寄存器设置如何，INTSTS0寄存器中的状态标志都会设置为1，以响应满足相关条件的状态变化。

当INTENB0寄存器中的中断请求使能位从0切换到1且INTSTS0寄存器中的相关状态标志设置为1时，请求USBHS中断。

33.2.12 Interrupt Enable Register 1 (INTENB1)

Address(es): USBHS.INTENB1 4006 0032h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	OVRCRE	BCHGE	—	DTCHE	ATTCHE	—	L1RSMENDE	LPMENDE	—	EOFERRE	SIGNE	SACKE	—	—	—	PDDETINTE
Value after reset:	0	0	x	0	0	x	0	0	x	0	0	0	x	x	x	0

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b0	PDDETINTE	PDDETINT Detection Interrupt Request Enable	0: Disable interrupt request 1: Enable interrupt request.	R/W
b3 to b1	—	Reserved	The read value is undefined. The write value should be 0.	R/W
b4	SACKE	Setup Transaction Normal Response Interrupt Request Enable	0: Disable interrupt request 1: Enable interrupt request.	R/W
b5	SIGNE	Setup Transaction Error Interrupt Request Enable	0: Disable interrupt request 1: Enable interrupt request.	R/W
b6	EOFERRE	EOF Error Detection Interrupt Request Enable	0: Disable interrupt request 1: Enable interrupt request.	R/W
b7	—	Reserved	The read value is undefined. The write value should be 0.	R/W
b8	LPMENDE	LPM Transaction End Interrupt Request Enable	0: Disable interrupt request 1: Enable interrupt request.	R/W
b9	L1RSMENDE	L1 Resume End Interrupt Enable	0: Disable interrupt request 1: Enable interrupt request.	R/W
b10	—	Reserved	The read value is undefined. The write value should be 0.	R/W
b11	ATTCHE	Connection Detection Interrupt Request Enable	0: Disable interrupt request 1: Enable interrupt request.	R/W
b12	DTCHE	Disconnection Detection Interrupt Request Enable	0: Disable interrupt request 1: Enable interrupt request.	R/W
b13	—	Reserved	The read value is undefined. The write value should be 0.	R/W
b14	BCHGE	USB Bus Change Interrupt Request Enable	0: Disable interrupt request 1: Enable interrupt request.	R/W
b15	OVRCRE	OVRCRE Interrupt Request Enable	0: Disable interrupt request 1: Enable interrupt request.	R/W

When a status flag in the INTSTS1 register sets to 1 and the associated interrupt request enable bit setting in the INTENB1 register is 1, the USBHS issues a USBHS interrupt request.

Regardless of the INTENB1 register setting, the status flag in the INTSTS1 register sets to 1 in response to a state change that satisfies the associated condition.

When an interrupt request enable bit in the INTENB1 register is switched from 0 to 1 while the associated status flag in the INTSTS1 register is set to 1, a USBHS interrupt is requested.

33.2.12 中断使能寄存器1(INTENB1)

Address(es): USBHS.INTENB1 4006 0032h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	OVRCRE	BCHGE	—	DTCHE	ATTCHE	—	L1RSMENDE	LPMENDE	—	EOFERRE	SIGNE	SACKE	—	—	—	PDDETINTE
重置后的值：	0	0	x	0	0	x	0	0	x	0	0	0	x	x	x	0

x: Undefined

Bit	Symbol	位名称	Description	R/W
b0	PDDETINTE	PDDETINT检测中断请求启用	0：禁止中断请求1：允许中断请求。	R/W
b3 to b1	—	Reserved	读取值未定义。写入值应为0。	R/W
b4	SACKE	设置事务正常响应中断请求Enable	0：禁止中断请求1：允许中断请求。	R/W
b5	SIGNE	设置交易错误中断请求使能	0：禁止中断请求1：允许中断请求。	R/W
b6	EOFERRE	EOF错误检测中断请求启用	0：禁止中断请求1：允许中断请求。	R/W
b7	—	Reserved	读取值未定义。写入值应为0。	R/W
b8	LPMENDE	LPM事务结束中断请求启用	0：禁止中断请求1：允许中断请求。	R/W
b9	L1RSMENDE	L1恢复结束中断Enable	0：禁止中断请求1：允许中断请求。	R/W
b10	—	Reserved	读取值未定义。写入值应为0。	R/W
b11	ATTCHE	连接检测中断请求启用	0：禁止中断请求1：允许中断请求。	R/W
b12	DTCHE	断线检测中断请求使能	0：禁止中断请求1：允许中断请求。	R/W
b13	—	Reserved	读取值未定义。写入值应为0。	R/W
b14	BCHGE	USB总线变化中断请求启用	0：禁止中断请求1：允许中断请求。	R/W
b15	OVRCRE	OVRCRE中断请求Enable	0：禁止中断请求1：允许中断请求。	R/W

当INTSTS1寄存器中的状态标志设置为1并且相关的中断请求使能位设置在INTENB1寄存器为1，USBHS发出USBHS中断请求。

无论INTENB1寄存器设置如何，INTSTS1寄存器中的状态标志都会设置为1，以响应满足相关条件的状态更改。

当INTENB1寄存器中的中断请求使能位从0切换到1且INTSTS1寄存器中的相关状态标志设置为1时，请求USBHS中断。

33.2.13 BRDY Interrupt Enable Register (BRDYENB)

Address(es): USBHS.BRDYENB 4006 0036h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	PIPEBRDYE[9:0]									
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b9 to b0	PIPEBRDYE [9:0]	BRDY Interrupt Request Enable for Pipes [9:0]*1	0: Disable interrupt request 1: Enable interrupt request.	R/W
b15 to b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Each bit number corresponds to the same pipe number.

The BRDYENB register enables or disables the INTSTS0.BRDY bit to be set to 1 when a BRDY interrupt is detected for each pipe.

When a status flag in the BRDYSTS register sets to 1 and the associated PIPEBRDYEn (n = 9 to 0) bit setting in the BRDYENB register is 1, the INTSTS0.BRDY flag sets to 1. In this case, if the BRDYE bit in INTENB0 is 1, the USBHS generates a BRDY interrupt request. While at least one PIPEBRDYEn flag indicates 1, the INTSTS0.BRDY flag sets to 1 when the associated interrupt request enable bit in the BRDYENB register is changed from 0 to 1 by software.

33.2.14 NRDY Interrupt Enable Register (NRDYENB)

Address(es): USBHS.NRDYENB 4006 0038h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	PIPENRDYE[9:0]									
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b9 to b0	PIPENRDYE [9:0]	NRDY Interrupt Enable for Pipes [9:0]*1	0: Disable interrupt request 1: Enable interrupt request.	R/W
b15 to b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Each bit number corresponds to the same pipe number.

The NRDYENB register enables or disables the INTSTS0.NRDY bit to be set to 1 when a NRDY interrupt is detected for each pipe.

When a status flag in the NRDYSTS register sets to 1 and the associated PIPENRDYEn (n = 0 to 9) bit setting in the NRDYENB register is 1, the INTSTS0.NRDY flag sets to 1. In this case, if the NRDYE bit in INTENB0 is 1, the USBHS generates a NRDY interrupt request. While at least one PIPEBRDYEn flag indicates 1, the INTSTS0.NRDY flag sets to 1 when the associated interrupt request enable bit in the NRDYENB register is changed from 0 to 1 by software.

33.2.13 BRDY中断使能寄存器(BRDYENB)

Address(es): USBHS.BRDYENB 4006 0036h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	PIPEBRDYE[9:0]									
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b9 to b0	PIPEBRDYE [9:0]	管道[9:0]*1的BRDY中断请求启用	0：禁止中断请求1：允许中断请求。	R/W
b15 to b10	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 每个位号对应相同的管道号。

当检测到每个管道的BRDY中断时，BRDYENB寄存器启用或禁用INTSTS0.BRDY位以设置为1。

当BRDYSTS寄存器中的状态标志设置为1并且相关的PIPEBRDYEn（n=9到0）位设置BRDYENB寄存器为1，INTSTS0.BRDY标志置1。这种情况下，如果INTENB0中的BRDYE位为1，USBHS产生一个BRDY中断请求。虽然至少有一个PIPEBRDYEn标志指示1，但当BRDYENB寄存器中的相关中断请求使能位由软件从0变为1时，INTSTS0.BRDY标志设置为1。

33.2.14 NRDY中断使能寄存器(NRDYENB)

Address(es): USBHS.NRDYENB 4006 0038h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	PIPENRDYE[9:0]									
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b9 to b0	PIPENRDYE [9:0]	NRDY中断使能 Pipes [9:0]*1	0：禁止中断请求1：允许中断请求。	R/W
b15 to b10	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 每个位号对应相同的管道号。

当检测到每个管道的NRDY中断时，NRDYENB寄存器启用或禁用INTSTS0.NRDY位设置为1。

当NRDYSTS寄存器中的状态标志设置为1并且NRDYENB寄存器中相关的PIPENRDYEn(n=0到9)位设置为1时，INTSTS0.NRDY标志设置为1。在这种情况下，如果INTENB0中的NRDYE位为1，USBHS产生一个NRDY中断请求。虽然至少有一个PIPEBRDYEn标志指示1，但当NRDYENB寄存器中的相关中断请求使能位由软件从0变为1时，INTSTS0.NRDY标志设置为1。

33.2.15 BEMP Interrupt Enable Register (BEMPENB)

Address(es): USBHS.BEMPENB 4006 003Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	PIPEBEMPE[9:0]									
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b9 to b0	PIPEBEMPE [9:0]	BEMP Interrupt Enable for Pipes [9:0]*1	0: Disable interrupt request 1: Enable interrupt request.	R/W
b15 to b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Each bit number corresponds to the same pipe number.

The BEMPENB register enables or disables the INTSTS0.BEMP bit to be set to 1 when a BEMP interrupt is detected for each pipe.

When a status flag in the BEMPSTS register sets to 1 and the associated PIPEBEMPEn (n = 0 to 9) bit setting in the BEMPENB register is 1, the INTSTS0.BEMP flag sets to 1. In this case, if the BEMPE bit in INTENB0 is 1, the USBHS generates a BEMP interrupt request. While at least one PIPEBEMPEn flag indicates 1, the INTSTS0.BEMP flag sets to 1 when the associated interrupt request enable bit in the BEMPENB register is changed from 0 to 1 by software.

33.2.16 SOF Output Configuration Register (SOFCFG)

Address(es): USBHS.SOFCFG 4006 003Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	TRNEN SEL	—	BRDY M	INTL	EDGES TS	—	—	—	—
Value after reset:	x	x	x	x	x	x	x	0	x	0	0	0	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b3 to b0	—	Reserved	The read value is undefined. The write value should be 0.	R/W
b4	EDGESTS	Interrupt Edge Processing Status Flag*1	Indicates 1 during the edge processing of an edge interrupt output signal.	R
b5	INTL	Interrupt Output Sense Select*2	0: Edge detection 1: Level detection.	R/W
b6	BRDYM	PIPEBRDY Interrupt Status Clear Timing*3	0: Clear BRDY flag through software 1: Clear BRDY flag by the USBHS through a data read from the FIFO buffer or data write to the FIFO buffer.	R/W
b7	—	Reserved	The read value is undefined. The write value should be 0.	R/W
b8	TRNENSEL	Transaction-Enabled Time Select*4	0: Not low-speed communication 1: Low-speed communication.	R/W
b15 to b9	—	Reserved	The read value is undefined. The write value should be 0.	R/W

Note 1. Confirm that the EDGESTS flag is 0 before stopping the clock supply to the USBHS.
Note 2. When the INTL bit is set to 0, to stop the PHY clock (LPSTS.SUSPENDM = 0) after clearing the interrupt status, write 0 to the LPSTS.SUSPENDM bit after confirming that the EDGESTS flag is cleared to 0.
Note 3. When setting the BRDYM bit to 1, set the INTL bit to 1.
Note 4. The setting in the TRNENSEL bit is only valid in host controller mode. Even in host controller mode, the setting of this bit has no effect on the transaction-enabled time during high-speed communication.

33.2.15 BEMP中断使能寄存器(BEMPENB)

Address(es): USBHS.BEMPENB 4006 003Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	PIPEBEMPE[9:0]									
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b9 to b0	PIPEBEMPE [9:0]	BEMP中断使能 Pipes [9:0]*1	0：禁止中断请求1：允许中断请求。	R/W
b15 to b10	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 每个位号对应相同的管道号。

当检测到每个管道的BEMP中断时，BEMPENB寄存器启用或禁用INTSTS0.BEMP位设置为1。

当BEMPSTS寄存器中的状态标志设置为1并且相关的PIPEBEMPEn（n=0到9）位设置在BEMPENB寄存器为1，INTSTS0.BEMP标志置1。这种情况下，如果INTENB0中的BEMPE位为1，USBHS产生一个BEMP中断请求。虽然至少有一个PIPEBEMPEn标志指示1，但当BEMPENB寄存器中的相关中断请求使能位由软件从0变为1时，INTSTS0.BEMP标志设置为1。

33.2.16 SOF输出配置寄存器(SOFCFG)

Address(es): USBHS.SOFCFG 4006 003Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	TRNEN SEL	—	BRDY M	INTL	EDGES TS	—	—	—	—
重置后的值：	x	x	x	x	x	x	x	0	x	0	0	0	x	x	x	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b3 to b0	—	Reserved	读取值未定义。写入值应为0。	R/W
b4	EDGESTS	中断沿处理状态 Flag*1	在边沿中断输出信号的边沿处理期间表示1。	R
b5	INTL	中断输出检测选择 *2	0：边缘检测1： 电平检测。	R/W
b6	BRDYM	PIPEBRDY中断状态 明确时间 *3	0：通过软件清除BRDY标志1：USBHS通过从FIFO缓冲区读取数据或向FIFO缓冲区写入数据清除BRDY标志。	R/W
b7	—	Reserved	读取值未定义。写入值应为0。	R/W
b8	TRNENSEL	Transaction-Enabled Time Select*4	0：非低速通讯1：低速通讯。	R/W
b15 to b9	—	Reserved	读取值未定义。写入值应为0。	R/W

Note 1. 在停止向USBHS提供时钟之前，请确认EDGESTS标志为0。
Note 2. 当INTL位设置为0时，要在清除中断状态后停止PHY时钟(LPSTS.SUSPENDM=0)，将0写入确认EDGESTS标志清零后的LPSTS.SUSPENDM位。
Note 3. 将BRDYM位设置为1时，将INTL位设置为1。
Note 4. TRNENSEL位中的设置仅在主机控制器模式下有效。即使在主机控制器模式下，该位的设置也不会影响高速通信期间的事务使能时间。

EDGESTS flag (Interrupt Edge Processing Status Flag)

The EDGESTS flag indicates 1 during the edge processing of an edge interrupt output signal. Confirm that this flag is 0 before stopping the PHY clock.

BRDYM bit (PIPEBRDY Interrupt Status Clear Timing)

The BRDYM bit specifies how the BRDY interrupt status flags for the pipes are cleared.

TRNENSEL bit (Transaction-Enabled Time Select)

When the USB port is in use for full- or low-speed communications, the TRNENSEL bit specifies the timing with which the USBHS issues tokens in a frame (transaction-enabled time).

Set this bit to 1 when a low-speed device is connected directly or through a full-speed hub. The bit is only valid in host controller mode. Set this bit to 0 when the interface is in use as a device controller.

33.2.17 PHY Setting Register (PHYSET)

Address(es): USBHS.PHYSET 4006 003Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	HSEB	—	—	—	REPSTART	—	REPSEL[1:0]		—	—	CLKSEL[1:0]		CDPEN	—	PLLRESET	DIRPD
Value after reset:	x	x	x	x	0	x	0	0	x	x	1	1	0	x	1	1

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b0	DIRPD	Power-Down Control	0: Do not enter low power mode 1: Enter low power mode.	R/W
b1	PLLRESET	PLL Reset Control*1	0: Disable PLL reset control for UTMI_PHY 1: Enable PLL reset control for UTMI_PHY.	R/W
b2	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b3	CDPEN	Charging Downstream Port Enable	0: Disable downstream port charging 1: Enable downstream port charging.	R/W
b5, b4	CLKSEL[1:0]	Input System Clock Frequency	b5 b4 0 0: 12 MHz 0 1: Setting prohibited 1 0: 20 MHz 1 1: 24 MHz.	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b9, b8	REPSEL[1:0]	Terminating Resistance Adjustment Cycle	b9 b8 0 0: No cycle is set 0 1: Adjust terminating resistance at 16-second intervals 1 0: Adjust terminating resistance at 64-second intervals 1 1: Adjust terminating resistance at 128-second intervals.	R/W
b10	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b11	REPSTART	Forcibly Start Terminating Resistance Adjustment	0: Force terminating resistance adjustment to start 1: Do not force terminating resistance adjustment to start.	R/W
b14 to b12	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15	HSEB	CL-only mode	0: Disable CL-only mode 1: Enable CL-only mode.	R/W

Note 1. Because the value of the PLLRESET bit is 1 after a reset, changing the setting after release from the reset state is not required. Do not set the PLLRESET bit to 1 after setting the PLLRESET bit to 0. Operation is not guaranteed.

CLKSEL[1:0] bits (Input System Clock Frequency)

The CLKSEL[1:0] bits select the transfer clock source for the USBHS.

For the transfer clock generated in the USB-PHY internal PLL, these bits set the input clock frequency. To input the

EDGESTS标志（中断边缘处理状态标志）

EDGESTS标志在边沿中断输出信号的边沿处理期间指示为1。在停止PHY时钟之前确认该标志为0。

BRDYM位（PIPEBRDY中断状态清除时序）

BRDYM位指定如何清除管道的BRDY中断状态标志。

TRNENSEL位（事务使能时间选择）

当USB端口用于全速或低速通信时，TRNENSEL位指定USBHS在帧中发出令牌的时间（事务启用时间）。

当低速设备直接连接或通过全速集线器连接时，将此位设置为1。该位仅在主机控制器模式下有效。当接口用作设备控制器时，将此位设置为0。

33.2.17 PHY设置寄存器(PHYSET)

Address(es): USBHS.PHYSET 4006 003Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	HSEB	—	—	—	REPSTART	—	REPSEL[1:0]		—	—	CLKSEL[1:0]		CDPEN	—	PLLRESET	DIRPD
重置后的值：	x	x	x	x	0	x	0	0	x	x	1	1	0	x	1	1

x: Undefined

Bit	Symbol	位名称	Description	R/W
b0	DIRPD	Power-Down Control	0：不进入低功耗模式1：进入低功耗模式。	R/W
b1	PLLRESET	PLL Reset Control*1	0：禁用UTMI_PHY的PLL复位控制1：启用UTMI_PHY的PLL复位控制。	R/W
b2	—	Reserved	该位读取为0。写入值应为0。	R/W
b3	CDPEN	充电下游端口 Enable	0：禁用下行端口充电1：启用下行端口充电。	R/W
b5, b4	CLKSEL[1:0]	输入系统时钟频率	b5 b4 0 0: 12 MHz 0 1：禁止设置 1 0: 20 MHz 1 1: 24 MHz.	R/W
b7, b6	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b9, b8	REPSEL[1:0]	终止电阻调整周期	b9 b8 0 0：未设置周期 0 1：以16秒为间隔调整终端电阻 1 0：以64秒为间隔调整终端电阻 1 1：以128秒为间隔调整终端电阻。	R/W
b10	—	Reserved	该位读取为0。写入值应为0。	R/W
b11	REPSTART	强制开始终止阻力调整	0：强制启动终端电阻调整1：不强制启动终端电阻调整。	R/W
b14 to b12	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b15	HSEB	CL-only mode	0：禁用CL-only模式1：启用CL-only模式。	R/W

Note 1. 由于PLLRESET位的值在复位后为1，因此无需在从复位状态释放后更改设置。在将PLLRESET位设置为0后不要将PLLRESET位设置为1。不能保证操作。

CLKSEL[1:0]位（输入系统时钟频率）

CLKSEL[1:0]位选择USBHS的传输时钟源。

对于USB-PHY内部PLL中生成的传输时钟，这些位设置输入时钟频率。要输入

clock source from the EXTAL pin, the USB 2.0 clock specification must be strictly followed.

Writing to the CKSEL[1:0] bits is invalid in CL-only mode because the internal PLL is stopped (see the description for HSEB bit (CL-only mode)). For the clock settings, see section 33.3.3, Supplying the Clock.

HSEB bit (CL-only mode)

The HSEB bit selects whether the USBHS operates in CL-only mode. High-speed transfer by the USBHS requires the use of internal high-speed analog circuits including the PLL, clock, and data recovery (CDR) circuit in the USB-PHY block.

CL-only mode limits the transfer to the USB 1.1 specification (full- and low-speed transfer only). Power consumption can be reduced by stopping the internal PLL of the PHY module and other high-speed analog circuits.

In CL-only mode, the USBHS requires supply clocks of 48 MHz and 60 MHz, generated in the Clock Generation Circuit. For the clock supply method, see section 9, Clock Generation Circuit.

33.2.18 Interrupt Status Register 0 (INTSTS0)

Address(es): USBHS.INTSTS0 4006 0040h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	VBINT	RESM	SOFR	DVST	CTRT	BEMP	NRDY	BRDY	VBSTS	DVSQ[2:0]			VALID	CTSQ[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	x	0	0	0	0	0	0	0

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b2 to b0	CTSQ[2:0]	Control Transfer Stage Flag*1	b2 b0 0 0 0: Idle or setup stage 0 0 1: Control read data stage 0 1 0: Control read status stage 0 1 1: Control write data stage 1 0 0: Control write status stage 1 0 1: Control write (no data) status stage 1 1 0: Control transfer sequence error.	R
b3	VALID	USB Request Reception Flag*1	0: Setup packet not received 1: Setup packet received.	R/(W) *3
b6 to b4	DVSQ[2:0]	Device State*1	Indicates the device state. b6 b4 0 0 0: Powered state 0 0 1: Default state 0 1 0: Address state 0 1 1: Configured state 1 x x: Suspend state.	R
b7	VBSTS	VBUS Input Status Flag	0: USBHS_VBUS pin is low 1: USBHS_VBUS pin is high.	R
b8	BRDY	BRDY Interrupt Status Flag	0: No BRDY interrupt occurred 1: BRDY interrupt occurred.	R
b9	NRDY	NRDY Interrupt Status Flag	0: No NRDY interrupt occurred 1: NRDY interrupt occurred.	R
b10	BEMP	BEMP Interrupt Status Flag	0: No BEMP interrupt occurred 1: BEMP interrupt occurred.	R
b11	CTRT	Control Transfer Stage Transition Interrupt Status Flag*2	0: No control transfer stage transition interrupt occurred 1: Control transfer stage transition interrupt occurred.	R/(W) *3
b12	DVST	Device State Transition Interrupt Status Flag*2	0: No device state transition interrupt occurred 1: Device state transition interrupt occurred.	R/(W) *3
b13	SOFR	Frame Number Refresh Interrupt Status Flag	0: No SOF interrupt occurred 1: SOF interrupt occurred.	R/(W) *3

来自EXTAL引脚的时钟源，必须严格遵循USB2.0时钟规范。

在CL-only模式下写入CKSEL[1:0]位无效，因为内部PLL已停止（请参见HSEB位（仅限CL模式））。有关时钟设置，请参阅第33.3.3节，提供时钟。

HSEB位（仅CL模式）

HSEB位选择USBHS是否工作在CL-only模式。USBHS的高速传输需要使用内部高速模拟电路，包括USB-PHY模块中的PLL、时钟和数据恢复(CDR)电路。

仅CL模式将传输限制为USB1.1规范（仅限全低速传输）。通过停止PHY模块的内部PLL和其他高速模拟电路可以降低功耗。

在CL-only模式下，USBHS需要48MHz和60MHz的电源时钟，在时钟生成中生成电路。关于时钟提供方法，请参见第9节"时钟生成电路"。

33.2.18 中断状态寄存器0(INTSTS0)

Address(es): USBHS.INTSTS0 4006 0040h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	VBINT	RESM	SOFR	DVST	CTRT	BEMP	NRDY	BRDY	VBSTS	DVSQ[2:0]			VALID	CTSQ[2:0]		
重置后的值：	0	0	0	0	0	0	0	0	x	0	0	0	0	0	0	0

x: Undefined

Bit	Symbol	位名称	Description	R/W
b2 to b0	CTSQ[2:0]	控制转移阶段标志*1	b2 b0 0 0 0：空闲或设置阶段 0 0 1：控制读数据阶段 0 1 0：控制读状态阶段 0 1 1：控制写入数据阶段 1 0 0：控制写状态阶段 1 0 1：控制写入（无数据）状态阶段 1 1 0：控制传输顺序错误。	R
b3	VALID	USB请求接收标志*1	0：未收到设置包1：收到设置包。	R/(W) *3
b6 to b4	DVSQ[2:0]	Device State*1	指示设备状态。b6 0 0 0：上电状态 0 0 1：默认状态 0 1 0：地址状态 0 1 1：配置状态 1 x x：暂停状态。	R
b7	VBSTS	VBUS输入状态标志	0：USBHS_VBUS引脚为低电平1：USBHS_VBUS引脚为高电平。	R
b8	BRDY	BRDY中断状态标志	0：未发生BRDY中断1：发生BRDY中断。	R
b9	NRDY	NRDY中断状态标志	0：未发生NRDY中断1：发生NRDY中断。	R
b10	BEMP	BEMP中断状态标志	0：未发生BEMP中断1：发生BEMP中断。	R
b11	CTRT	控制转移阶段转换中断状态标志 *2	0：未发生控制转移阶段转换中断1：发生控制转移阶段转换中断。	R/(W) *3
b12	DVST	设备状态转换中断状态标志 *2	0：未发生设备状态转换中断1：发生设备状态转换中断。	R/(W) *3
b13	SOFR	帧号刷新中断状态标志	0：未发生SOF中断1：发生SOF中断。	R/(W) *3

Bit	Symbol	Bit name	Description	R/W
b14	RESM	Resume Interrupt Status Flag*2, *4	0: No resume interrupt occurred 1: Resume interrupt occurred.	R/(W) *3
b15	VBINT	VBUS Interrupt Status Flag*4	0: No VBUS interrupt occurred on detecting a change in the USBHS_VBUS pin 1: VBUS interrupt occurred on detecting a change in the USBHS_VBUS pin.	R/(W) *3

x: Don't care

Note 1. The CTSQ[2:0], VALID, and DVSQ[2:0] flags are only valid in device controller mode.
Note 2. The status of the CTRT, DVST, and RESM flags are changed only in device controller mode. Set the associated interrupt enable bits to 0 (disabled) in host controller mode.
Note 3. To clear the CTRT, DVST, SOFR, RESM, or VBINT flags, write 0 only to the flags to be cleared. Write 1 to the other flags. Do not write 0 to the status flags indicating 0.
Note 4. The USBHS detects a change in the status in the RESM or VBINT flag even while the clock supply is stopped (LPSTS.SUSPENDM = 0), and it requests the interrupt when the associated interrupt request bit is 1. Enable the clock supply before clearing the status by software.

BRDY flag (BRDY Interrupt Status Flag)

The BRDY flag indicates the BRDY interrupt state. For the conditions that cause the flag to be set, see section 33.2.13, BRDY Interrupt Enable Register (BRDYENB).

The USBHS clears the BRDY flag to 0 when 0 is written to the BRDYSTS.PIPEBRDYn (n = 0 to 9) flags for all pipes for which the BRDY interrupt is enabled (BRDYENB.PIPEBRDYEn bits). Writing 0 to the BRDY flag in the software does not clear the flag.

NRDY flag (NRDY Interrupt Status Flag)

The NRDY flag indicates the NRDY interrupt state. For the conditions that cause the flag to be set, see section 33.2.14, NRDY Interrupt Enable Register (NRDYENB).

The USBHS clears the NRDY flag to 0 when 0 is written to the NRDYSTS.PIPENRDYn (n = 0 to 9) flags for all pipes for which the NRDY interrupt is enabled (NRDYENB.PIPENRDYEn bits). Writing 0 to the NRDY flag in the software does not clear the flag.

BEMP flag (BEMP Interrupt Status Flag)

The BEMP indicates the BEMP interrupt state. For the conditions that cause the flag to be set, see section 33.2.15, BEMP Interrupt Enable Register (BEMPENB).

The USBHS clears the BEMP flag to 0 when 0 is written to the BEMPSTS.PIPEBEMPn (n = 0 to 9) flags for all pipes for which the BEMP interrupt is enabled (BEMPENB.PIPEBEMPEn bits). Writing 0 to the BEMP flag in the software does not clear the flag.

CTRT flag (Control Transfer Stage Transition Interrupt Status Flag)

In device controller mode, the USBHS updates the value of the CTSQ[2:0] bits and sets the CTRT flag to 1 on detecting a transition in the control transfer stage. When a control transfer stage transition interrupt occurs, clear the CTRT flag before the USBHS detects the next control transfer stage transition.

Values read from the CTRT flag in host controller mode are invalid.

DVST flag (Device State Transition Interrupt Status Flag)

In device controller mode, the USBHS updates the value of the PL1CTRL1.DVSQ[3:0] bits and sets the DVST flag to 1 on detecting a change in the device state. When a device state transition interrupt occurs, clear the DVST flag before the USBHS detects the next device state transition.

Values read from the DVST flag in host controller mode are invalid.

SOFR flag (Frame Number Refresh Interrupt Status Flag)

In host controller mode, the USBHS sets the SOFR flag to 1 on updating the frame number when the DVSTCTR0.UACT bit is set to 1 by software. An SOFR interrupt is detected every 1 ms.

In device controller mode, the USBHS sets the SOFR flag to 1 on updating the frame number. An SOFR interrupt is

Bit	Symbol	位名称	Description	R/W
b14	RESM	恢复中断状态 Flag*2, *4	0：未发生恢复中断1：发生恢复中断。	R/(W) *3
b15	VBINT	VBUS中断状态标志 *4	0：检测到USBHS_VBUS引脚变化时未发生VBUS中断1：检测到USBHS_VBUS引脚变化时发生VBUS中断。	R/(W) *3

x: Don't care

Note 1. CTSQ[2:0]、VALID和DVSQ[2:0]标志仅在设备控制器模式下有效。
Note 2. CTRT、DVST和RESM标志的状态仅在设备控制器模式下更改。在主机控制器模式下，将相关的中断使能位设置为0（禁用）。
Note 3. 要清除CTRT、DVST、SOFR、RESM或VBINT标志，只需将0写入要清除的标志。将1写入其他标志。不要将0写入指示0的状态标志。
Note 4. 即使在时钟供应停止时（LPSTS.SUSPENDM=0），USBHS也会检测到RESM或VBINT标志的状态变化，并在相关的中断请求位为1时请求中断。在清除软件状态。

BRDY标志（BRDY中断状态标志）

BRDY标志指示BRDY中断状态。有关导致设置标志的条件，请参阅第33.2.13节，BRDY中断使能寄存器(BRDYENB)。

当0写入BRDYSTS.PIPEBRDYn（n=0到9）标志时，USBHS将BRDY标志清除为0，用于所有启用了BRDY中断的管道（BRDYENB.PIPEBRDYEn位）。在软件中将0写入BRDY标志不会清除该标志。

NRDY标志（NRDY中断状态标志）

NRDY标志指示NRDY中断状态。有关导致设置标志的条件，请参阅第33.2.14节，NRDY中断使能寄存器(NRDYENB)。

当0写入所有启用了NRDY中断的管道（NRDYENB.PIPENRDYEn位）的NRDYSTS.PIPENRDYn（n=0到9）标志时，USBHS将NRDY标志清除为0。在软件中将0写入NRDY标志不会清除该标志。

BEMP标志（BEMP中断状态标志）

BEMP指示BEMP中断状态。有关导致设置标志的条件，请参阅第33.2.15节，BEMP中断使能寄存器(BEMPENB)。

当0写入所有启用了BEMP中断的管道（BEMPENB.PIPEBEMPEn位）的BEMPSTS.PIPEBEMPn（n=0到9）标志时，USBHS将BEMP标志清除为0。在软件中将0写入BEMP标志不会清除该标志。

CTRT标志（控制传输阶段转换中断状态标志）

在设备控制器模式下，USBHS更新CTSQ[2:0]位的值并将CTRT标志设置为1检测到控制传输阶段的转换。当控制传输阶段转换中断发生时，在USBHS检测到下一个控制传输阶段转换之前清除CTRT标志。

在主机控制器模式下从CTRT标志读取的值无效。

DVST标志（设备状态转换中断状态标志）

在设备控制器模式下，USBHS更新PL1CTRL1.DVSQ[3:0]位的值并将DVST标志设置为1，以检测设备状态的变化。当设备状态转换中断发生时，在USBHS检测到下一个设备状态转换之前清除DVST标志。

在主机控制器模式下从DVST标志读取的值无效。

SOFR标志（帧号刷新中断状态标志）

在主机控制器模式下，当DVSTCTR0.UACT位被软件设置为1时，USBHS在更新帧号时将SOFR标志设置为1。每1 ms检测一次SOFR中断。

在设备控制器模式下，USBHS在更新帧号时将SOFR标志设置为1。SOFR中断是

detected every 1 ms. The USBHS can detect an SOFR interrupt through the SOF complementation function even when a corrupted SOF packet is received from the USB host. See section 33.3.13, SOF Complementation Function.

RESM flag (Resume Interrupt Status Flag)

In device controller mode, the USBHS sets the RESM flag to 1 on detecting the falling edge of the signal on the USBHS_DP pin in the Suspend state (PL1CTRL1.DVSQ[3:0] = 01xxb).

Values read from the RESM flag in host controller mode are invalid.

VBINT flag (VBUS Interrupt Status Flag)

The USBHS sets the VBINT flag to 1 on detecting a level change (high to low or low to high) in the USBHS_VBUS pin input value. The USBHS sets the VBSTS flag to indicate the USBHS_VBUS pin input value. When a VBINT interrupt occurs, eliminate transient elements by reading the VBSTS flag at least three times through software processing and check that the values read are the same.

33.2.19 Interrupt Status Register 1 (INTSTS1)

Address(es): USBHS.INTSTS1 4006 0042h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	OVRCR	BCHG	—	DTCH	ATTCH	—	L1RSMEND	LPMEND	—	EOFERR	SIGN	SACK	—	—	—	PDDETINT
Value after reset:	0	0	x	0	0	x	0	0	x	0	0	0	x	x	x	0

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b0	PDDETINT	PDDET Detection Interrupt Status Flag*1	0: No PDDET interrupt occurred 1: PDDET interrupt occurred.	R/(W)*2
b3 to b1	—	Reserved	The read value is undefined. The write value should be 0.	R/W
b4	SACK	Setup Transaction Normal Response Interrupt Status Flag	0: No SACK interrupt occurred 1: SACK interrupt occurred.	R/(W)*2
b5	SIGN	Setup Transaction Error Interrupt Status Flag	0: No SIGN interrupt occurred 1: SIGN interrupt occurred.	R/(W)*2
b6	EOFERR	EOF Error Detection Interrupt Status Flag	0: No EOFERR interrupt occurred 1: EOFERR interrupt occurred.	R/(W)*2
b7	—	Reserved	The read value is undefined. The write value should be 0.	R/W
b8	LPMEND	LPM Transaction End Interrupt Status Flag	0: No LPMEND interrupt occurred 1: LPMEND interrupt occurred.	R/(W)*2
b9	L1RSMEND	L1 Resume End Interrupt Status Flag	0: No L1RSMEND interrupt occurred 1: L1RSMEND interrupt occurred.	R/(W)*2
b10	—	Reserved	The read value is undefined. The write value should be 0.	R/W
b11	ATTCH	USB Connection Detection Interrupt Status Flag	0: No ATTCH interrupt occurred 1: ATTCH interrupt occurred.	R/(W)*2
b12	DTCH	USB Disconnection Detection Interrupt Status Flag	0: No DTCH interrupt occurred. 1: DTCH interrupt occurred	R/(W)*2
b13	—	Reserved	The read value is undefined. The write value should be 0.	R/W
b14	BCHG	USB Bus Change Interrupt Status Flag*1	0: No BCHG interrupt occurred 1: BCHG interrupt occurred.	R/(W)*2
b15	OVRCR	OVRCR Interrupt Status Flag*1	0: No OVRCR interrupt occurred 1: OVRCR interrupt occurred.	R/(W)*2

Note: Only enable the status change interrupts indicated in the flags in INTSTS1 in host controller mode, except for the PDDET detection interrupt.

Note 1. The USBHS detects a change in the status in the PDDETINT, BCHG, or OVRCR flag even while the clock supply is stopped (LPSTS.SUSPENDM = 0), and it requests the interrupt when the associated interrupt request bit is 1. Enable the clock supply before clearing the status by software. No other interrupts can be detected while the clock supply is stopped (LPSTS.SUSPENDM = 0).

每1ms检测一次。即使从USB主机接收到损坏的SOF数据包，USBHS也可以通过SOF补充功能检测SOFR中断。请参阅第33.3.13节，SOF互补功能。

RESM标志（恢复中断状态标志）

在设备控制器模式下，USBHS在检测到信号的下降沿时将RE SM标志设置为1
USBHS_DP引脚处于挂起状态(PL1CTRL1.DVSQ[3:0]=01xxb)。

在主机控制器模式下从RESM标志读取的值无效。

VBINT标志（VBUS中断状态标志）

USBHS在检测到USBHS_VBUS引脚输入值的电平变化（从高到低或从低到高）时将VBINT标志设置为1。USBHS设置VBSTS标志以指示USBHS_VBUS引脚输入值。当发生VBINT中断时，通过软件处理至少3次读取VBSTS标志来消除瞬态元素，并检查读取的值是否相同。

33.2.19 中断状态寄存器1(INTSTS1)

Address(es): USBHS.INTSTS1 4006 0042h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	OVRCR	BCHG	—	DTCH	ATTCH	—	L1RSMEND	LPMEND	—	EOFERR	SIGN	SACK	—	—	—	PDDETINT
重置后的值：	0	0	x	0	0	x	0	0	x	0	0	0	x	x	x	0

x: Undefined

Bit	Symbol	位名称	Description	R/W
b0	PDDETINT	PDDET检测中断 Status Flag*1	0：未发生PDDET中断1：发生PDDET中断。	R/(W)*2
b3 to b1	—	Reserved	读取值未定义。写入值应为0。	R/W
b4	SACK	设置事务正常 响应中断状态标志	0：未发生SACK中断1：发生SACK中断。	R/(W)*2
b5	SIGN	设置事务错误 中断状态标志	0：未发生SIGN中断1：发生SIGN中断。	R/(W)*2
b6	EOFERR	EOF错误检测中断 状态标志	0：没有EOFERR中断发生1：EOFERR中断发生。	R/(W)*2
b7	—	Reserved	读取值未定义。写入值应为0。	R/W
b8	LPMEND	LPM事务结束中断 状态标志	0：未发生LPMEND中断1：发生LPMEND中断。	R/(W)*2
b9	L1RSMEND	L1恢复结束中断状态 Flag	0：未发生L1RSMEND中断1：发生L1RSMEND中断。	R/(W)*2
b10	—	Reserved	读取值未定义。写入值应为0。	R/W
b11	ATTCH	USB连接检测 中断状态标志	0：未发生ATTCH中断1：发生ATTCH中断。	R/(W)*2
b12	DTCH	USB断线检测 中断状态标志	0：未发生DTCH中断。1：发生DTCH中断	R/(W)*2
b13	—	Reserved	读取值未定义。写入值应为0。	R/W
b14	BCHG	USB总线变化中断 Status Flag*1	0：未发生BCHG中断1：发生BCHG中断。	R/(W)*2
b15	OVRCR	OVRCR中断状态标志*1	0：未发生OVRCR中断1：发生OVRCR中断。	R/(W)*2

Note: 仅在主机控制器模式下启用INTSTS1中标志指示的状态更改中断，PDDET检测中断除外。

Note 1. USBHS检测到PDDETINT、BCHG或OVRCR标志中的状态变化，即使在时钟供应停止(LPSTS.SUSPENDM=0)时，它也会在相关的中断请求位为1时请求中断。启用时钟供应在通过软件清除状态之前。停止提供时钟(LPSTS.SUSPENDM=0)时无法检测到其他中断。

Note 2. To clear the flags in INTSTS1, write 0 only to the flags to be cleared. Write 1 to the other bits.

PDDETINT flag (PDDET Detection Interrupt Status Flag*1)

The USBHS sets the PDDETINT flag to 1 on detecting a level change (high to low or low to high) in the PDDET pin input value. When the PDDETINT interrupt is generated, perform debouncing by reading the PDDETSTS flag at least three times through software processing and checking that the values read are the same.

SACK flag (Setup Transaction Normal Response Interrupt Status Flag)

The SACK flag indicates the status of the setup transaction normal response interrupt in host controller mode.

The USBHS detects the SACK interrupt and sets this bit to 1 when an ACK response is returned from a peripheral device during the setup transactions issued by the USBHS. If the associated interrupt enable bit is set to 1 by software, the USBHS generates the interrupt.

Values read from the SACK flag in device controller mode are invalid.

SIGN flag (Setup Transaction Error Interrupt Status Flag)

The SIGN flag indicates the status of setup transaction error interrupts in host controller mode.

The USBHS detects the SIGN interrupt and sets this bit to 1 when an ACK response is not returned from a peripheral device three consecutive times during the setup transactions issued by the USBHS. If the associated interrupt enable bit is set to 1 by software, the USBHS generates the interrupt.

The USBHS detects the SIGN interrupt when any of the following response conditions occur for three consecutive setup transactions:

- Timeout is detected by the USBHS when the peripheral device has returned no response
- A corrupted ACK packet is received
- A handshake other than ACK (NAK, NYET, or STALL) is received.

Values read from the SIGN flag in device controller mode are invalid.

EOFERR flag (EOF Error Detection Interrupt Status Flag)

The EOFERR flag indicates the status of EOF error detection interrupts in host controller mode.

The USBHS detects the EOFERR interrupt and sets this bit to 1 on detecting that communication did not complete at the EOF2 timing defined in the USB 2.0 specification. If the associated interrupt enable bit is set to 1 by software, the USBHS generates the interrupt.

After detecting the EOFERR interrupt, the USBHS controls the hardware as follows, regardless of the associated interrupt enable bit setting:

- Sets the DVSTCTR0.UACT bit for the port in which the EOFERR interrupt was detected to 0
- Puts the port in which the EOFERR interrupt occurred into the idle state.

The software must terminate all pipes in which communications are being carried out and re-enumerate the USB port.

Values read from the EOFERR flag in device controller mode are invalid.

LPMEND flag (LPM Transaction End Interrupt Status Flag)

The PLPMEND flag indicates the status of LPM transaction end interrupts in host controller mode.

When the HL1CTRL1.L1REQ bit sets to 1, the USBHS sends an LPM token. When the LPM transaction is ended because a response from the function device or a timeout is detected, the USBHS sets this flag to 1.

Values read from the LPMEND flag in device controller mode are invalid.

L1RSMEND flag (L1 Resume End Interrupt Status Flag)

The L1RSMEND flag indicates the status of L1 resume end interrupts in host controller mode.

When performing resume processing after transitioning to the L1 state because an ACK was received in response to an LPM token, the USBHS sets this flag to 1.

Note 2. 要清除INTSTS1中的标志，只需将0写入要清除的标志。将1写入其他位。

PDDETINT标志（PDDET检测中断状态标志*1）

USBHS在检测到PDDET引脚输入值的电平变化（从高到低或从低到高）时将PDDETINT标志设置为1。当产生PDDETINT中断时，通过软件处理至少3次读取PDDETSTS标志并检查读取的值是否相同来执行去抖动。

SACK标志（设置事务正常响应中断状态标志）

SACK标志指示主机控制器模式下设置事务正常响应中断的状态。

在USBHS发出的设置事务期间，当外围设备返回ACK响应时，USBHS检测到SACK中断并将该位设置为1。如果相关的中断使能位由软件设置为1，则USBHS产生中断。

在设备控制器模式下从SACK标志读取的值无效。

SIGN标志（设置事务错误中断状态标志）

SIGN标志指示主机控制器模式下设置事务错误中断的状态。

在USBHS发出的设置事务期间，如果外围设备连续3次没有返回ACK响应，则USBHS检测到SIGN中断并将该位设置为1。如果相关的中断使能位由软件设置为1，则USBHS产生中断。

当三个连续的设置事务发生以下任何响应条件时，USBHS检测到SIGN中断：

- 当外围设备没有返回响应时，USBHS检测到超时
- 收到损坏的ACK数据包
- 收到除ACK（NAK、NYET或STALL）以外的握手。

在设备控制器模式下从SIGN标志读取的值无效。

EOFERR标志（EOF错误检测中断状态标志）

EOFERR标志指示主机控制器模式下EOF错误检测中断的状态。

USBHS检测到EOFERR中断并在检测到通信未完成时将该位设置为1
USB2.0规范中定义的EOF2时序。如果相关的中断使能位由软件设置为1，则
USBHS产生中断。

检测到EOFERR中断后，USBHS对硬件进行如下控制，而不考虑相关的中断使能位设置：

- 将检测到EOFERR中断的端口的DVSTCTR0.UACT位设置为0
- 将发生EOFERR中断的端口置于空闲状态。

软件必须终止正在执行通信的所有管道并重新枚举USB端口。

在设备控制器模式下从EOFERR标志读取的值无效。

LPMEND标志（LPM事务结束中断状态标志）

PLPMEND标志指示主机控制器模式下LPM事务结束中断的状态。

当HL1CTRL1.L1REQ位设置为1时，USBHS发送一个LPM令牌。当LPM事务因检测到来自功能设备的响应或超时而结束时，USBHS将此标志设置为1。

在设备控制器模式下从LPMEND标志读取的值无效。

L1RSMEND标志（L1恢复结束中断状态标志）

L1RSMEND标志指示主机控制器模式下L1恢复结束中断的状态。

在转换到L1状态后执行恢复处理时，因为接收到ACK以响应
LPM令牌，USBHS将此标志设置为1。

Values read from the L1RSMEND flag in device controller mode are invalid.

ATTCH flag (USB Connection Detection Interrupt Status Flag)

The ATTCH flag indicates the status of USB attach detection interrupts in host controller mode.

The USBHS detects the ATTCH interrupt and sets this bit to 1 on detecting a J- or K-state on the full- or low-speed signal level for 2.5 µs. If the associated interrupt enable bit is set to 1 by software, the USBHS generates the interrupt.

The USBHS detects the ATTCH interrupt on any of the following conditions:

- K-state, SE0, or SE1 changes to J-state, and J-state continues for 2.5 µs
- J-state, SE0, or SE1 changes to K-state, and K-state continues for 2.5 µs.

Values read from the ATTCH flag in device controller mode are invalid.

DTCH flag (USB Disconnection Detection Interrupt Status Flag)

The DTCH flag indicates the status of USB detach detection interrupts in host controller mode.

The USBHS detects the DTCH interrupt and sets this bit to 1 on detecting a USB bus detach event. If the associated interrupt enable bit is set to 1 by software, the USBHS generates the interrupt.

The USBHS detects bus detach events based on the USB 2.0 specification.

After detecting the DTCH interrupt, the USBHS controls hardware as follows, regardless of the associated interrupt enable bit setting:

- Sets the DVSTCTR0.UACT bit for the port in which the DTCH interrupt was detected to 0
- Puts the port in which the DTCH interrupt occurred into the idle state.

The software must terminate all pipes in which communications are being carried out and invoke the wait state for attaching to the USB port (waiting for ATTCH interrupt generation).

Values read from the DTCH flag in device controller mode are invalid.

BCHG flag (USB Bus Change Interrupt Status Flag*1)

The BCHG flag indicates the status of USB bus change interrupts in host controller mode.

The USBHS detects the BCHG interrupt and sets this bit to 1 when a change in the full-speed signal level occurs on the USB port. This includes any change from J-state, K-state, or SE0 to J-state, K-state, or SE0. If the associated interrupt enable bit is set to 1 by software, the USBHS generates the interrupt.

The USBHS sets the SYSSTS0.LNST[1:0] flags to indicate the input state of the USB port. When a BCHG interrupt occurs, eliminate transient elements by repeat reading the LNST[1:0] bits by software until the same value is read at least three times.

Changes in the USB bus state can be detected while the PHY clock is stopped.

Values read from the BCHG flag in device controller mode are invalid.

OVRCR flag (OVRCR Interrupt Status Flag*1)

The OVRCR flag indicates the input status on the USBHS_OVCUR0A pin or changes on the USBHS_OVCUR0B pin. If the INTENB1.OVRCRE bit sets to 1, the USBHS requests the interrupt.

The USBHS sets the SYSSTS0.OVCMON[1:0] flags to indicate the input state of the USBHS_OVCUR0A and USBHS_OVCUR0B pins.

These pins allow overcurrent detection by software in host controller mode. To implement this function, connect the overcurrent signal from the external power supply IC that supplies VBUS to connected USB devices to the OVCUR0A or OVCUR0B pin. On detection of an OVRCR interrupt, eliminate transients by repeatedly reading the OVCMON[1:0] flags through the software until the same value is read at least three times.

在设备控制器模式下从L1RSMEND标志读取的值无效。

ATTCH标志（USB连接检测中断状态标志）

ATTCH标志指示主机控制器模式下USB连接检测中断的状态。

USBHS检测到ATTCH中断并在检测到全速或低速信号电平上的JorK状态持续2.5µs时将该位设置为1。如果相关的中断使能位由软件设置为1，则USBHS产生中断。

USBHS在以下任何条件下检测ATTCH中断：

- K-state、SE0或SE1变为J-state，J-state持续2.5µs
- J-state、SE0或SE1变为K-state，K-state持续2.5µs。

在设备控制器模式下从ATTCH标志读取的值无效。

DTCH标志（USB断线检测中断状态标志）

DTCH标志指示主机控制器模式下USB分离检测中断的状态。

USBHS检测到DTCH中断并在检测到USB总线分离事件时将该位设置为1。如果相关的中断使能位由软件设置为1，则USBHS产生中断。

USBHS根据USB2.0规范检测总线分离事件。

检测到DTCH中断后，USBHS对硬件进行如下控制，而不管相关的中断使能位设置如何：

- 将检测到DTCH中断的端口的DVSTCTR0.UACT位设置为0
- 将发生DTCH中断的端口置于空闲状态。

软件必须终止正在执行通信的所有管道并调用等待状态以连接到USB端口（等待ATTCH中断生成）。

在设备控制器模式下从DTCH标志读取的值无效。

BCHG标志（USB总线变化中断状态标志*1）

BCHG标志指示主机控制器模式下USB总线更改中断的状态。

当全速信号电平发生变化时，USBHS检测到BCHG中断并将该位设置为1。
USB端口。这包括从J-state、K-state或SE0到J-state、K-state或SE0的任何更改。如果相关的中断使能位由软件设置为1，则USBHS产生中断。

USBHS设置SYSSTS0.LNST[1:0]标志以指示USB端口的输入状态。当发生BCHG中断时，通过软件重复读取LNST[1:0]位来消除瞬态元素，直到至少读取3次相同的值。

当PHY时钟停止时，可以检测到USB总线状态的变化。

在设备控制器模式下从BCHG标志读取的值无效。

OVRCR标志（OVRCR中断状态标志*1）

OVRCR标志指示USBHS_OVCUR0A引脚上的输入状态或USBHS_OVCUR0B引脚上的变化。
如果INTENB1.OVRCRE位设置为1，则USBHS请求中断。

USBHS设置SYSSTS0.OVCMON[1:0]标志以指示USBHS_OVCUR0A的输入状态和
USBHS_OVCUR0B pins.

这些引脚允许在主机控制器模式下通过软件进行过流检测。要实现此功能，请将来自为所连接的USB设备提供VBUS的外部电源IC的过流信号连接到OVCUR0A或OVCUR0B引脚。在检测到OVRCR中断时，通过软件重复读取OVCMON[1:0]标志来消除瞬变，直到至少读取相同的值3次。

33.2.20 BRDY Interrupt Status Register (BRDYSTS)

Address(es): USBHS.BRDYSTS 4006 0046h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	PIPEBRDY[9:0]									
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b9 to b0	PIPEBRDY[9:0]	BRDY Interrupt Status Flag for Pipe[9:0]*1	0: No BRDY interrupt occurred 1: BRDY interrupt occurred.	R/(W) *2
b15 to b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Each bit number corresponds to the same pipe number.
Note 2. When the SOFCFG.BRDYM bit is set to 0, to clear the status indicated in the PIPEBRDY[9:0] flags, write 0 only to the bits to be cleared. Write 1 to the other bits.
When the SOFCFG.BRDYM bit is set to 0, clear BRDY interrupts before accessing the FIFO.

PIPEBRDY[9:0] flags (BRDY Interrupt Status Flag for Pipe[9:0])

When the BRDY interrupt is detected, the USBHS sets the associated bit in the PIPEBRDY[9:0] flags to 1. For details on BRDY interrupts, see section 33.3.6.1, BRDY interrupt.

33.2.21 NRDY Interrupt Status Register (NRDYSTS)

Address(es): USBHS.NRDYSTS 4006 0048h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	PIPENRDY[9:0]									
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b9 to b0	PIPENRDY[9:0]	NRDY Interrupt Status Flag for Pipe[9:0]*1	0: No NRDY interrupt occurred 1: NRDY interrupt occurred.	R/(W) *2
b15 to b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Each bit number corresponds to the same pipe number.
Note 2. To clear the status indicated in the PIPENRDY[9:0] flags, write 0 only to the bits to be cleared. Write 1 to the other bits.

PIPENRDY[9:0] flags (NRDY Interrupt Status Flag for Pipe[9:0])

If an internal NRDY interrupt is detected while the PID[1:0] bits in a pipe control register are 01b (BUF response), the USBHS sets the associated bit in the PIPENRDY[9:0] flags to 1. For details on NRDY interrupts, see section 33.3.6.2, NRDY interrupt.

33.2.20 BRDY中断状态寄存器(BRDYSTS)

Address(es): USBHS.BRDYSTS 4006 0046h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	PIPEBRDY[9:0]									
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b9 to b0	PIPEBRDY[9:0]	BRDY中断状态标志 Pipe[9:0]*1	0：未发生BRDY中断1：发生BRDY中断。	R/(W) *2
b15 to b10	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 每个位号对应相同的管道号。
Note 2. 当SOFCFG.BRDYM位设置为0时，要清除PIPEBRDY[9: 0]标志中指示的状态，只需将0写入要清除的位。将1写入其他位。当SOFCFG.BRDYM位设置为0时，在访问FIFO之前清除BRDY中断。

PIPEBRDY[9: 0]标志（管道[9:0]的BRDY中断状态标志）

当检测到BRDY中断时，USBHS将PIPEBRDY[9: 0]标志中的相关位设置为1。有关详细信息BRDY中断，请参阅第33.3.6.1节，BRDY中断。

33.2.21 NRDY中断状态寄存器(NRDYSTS)

Address(es): USBHS.NRDYSTS 4006 0048h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	PIPENRDY[9:0]									
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b9 to b0	PIPENRDY[9:0]	NRDY中断状态标志 Pipe[9:0]*1	0：未发生NRDY中断1：发生NRDY中断。	R/(W) *2
b15 to b10	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 每个位号对应相同的管道号。
Note 2. 要清除PIPENRDY[9: 0]标志中指示的状态，仅将0写入要清除的位。将1写入其他位。

PIPENRDY[9: 0]标志（管道[9:0]的NRDY中断状态标志）

如果在管道控制寄存器中的PID[1:0]位为01b（BUF响应）时检测到内部NRDY中断，则USBHS将PIPENRDY[9: 0]标志中的相关位设置为1。有关NRDY的详细信息中断，见第33.3.6.2节，NRDY interrupt.

33.2.22 BEMP Interrupt Status Register (BEMPSTS)

Address(es): USBHS.BEMPSTS 4006 004Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	PIPEBEMP[9:0]									
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b9 to b0	PIPEBEMP[9:0]	BEMP Interrupt Status Flag for Pipe[9:0]*1	0: No BEMP interrupt occurred 1: BEMP interrupt occurred.	R/(W) *2
b15 to b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Each bit number corresponds to the same pipe number.
Note 2. To clear the status indicated in the PIPEBEMP[9:0] flags, write 0 only to the bits to be cleared. Write 1 to the other bits.

PIPEBEMP[9:0] flags (BEMP Interrupt Status Flag for Pipe[9:0])

If an BEMP interrupt is detected while the PID[1:0] bits in a pipe control register are 01b (BUF response), the USBHS sets the associated bit in the PIPEBEMP[9:0] flags to 1. For details on BEMP interrupts, see section 33.3.6.3, BEMP interrupt.

33.2.23 Frame Number Register (FRMNUM)

Address(es): USBHS.FRMNUM 4006 004Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	OVRN	CRCE	—	—	—	FRNM[10:0]										
Value after reset:	0	0	x	x	x	0	0	0	0	0	0	0	0	0	0	0

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b10 to b0	FRNM[10:0]	Frame Number Flag	Latest frame number	R
b13 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b14	CRCE	CRC Error Detection Status Flag	0: No error occurred 1: Error occurred.	R/(W)
b15	OVRN	Overrun/Underrun Detection Status Flag	0: No error occurred 1: Error occurred.	R/(W)

Note: The OVRN flag is for debugging. Design the timing so that no overrun or underrun occurs in the system.

FRNM[10:0] flags (Frame Number Flag)

The USBHS sets the FRNM[10:0] flags to indicate the latest frame number, which is updated every 1 ms, when an SOF packet is issued or received.

CRCE flag (CRC Error Detection Status Flag)

The CRCE flag sets to 1 when a CRC error or bit stuffing error occurs during isochronous transfer. On detecting a CRC error, the USBHS generates an internal NRDY interrupt.

To clear the CRCE flag, write 0 to it while writing 1 to the other bits in the FRMNUM register.

OVRN flag (Overrun/Underrun Detection Status Flag)

The OVRN flag sets to 1 when an overrun or underrun error occurs during isochronous transfer. To clear the flag, write 0

33.2.22 BEMP中断状态寄存器(BEMPSTS)

Address(es): USBHS.BEMPSTS 4006 004Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	PIPEBEMP[9:0]									
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b9 to b0	PIPEBEMP[9:0]	BEMP中断状态标志 Pipe[9:0]*1	0：未发生BEMP中断1：发生BEMP中断。	R/(W) *2
b15 to b10	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 每个位号对应相同的管道号。
Note 2. 要清除PIPEBEMP[9:0]标志中指示的状态，请仅将0写入要清除的位。将1写入其他位。

PIPEBEMP[9:0]标志（管道[9:0]的BEMP中断状态标志）

如果在管道控制寄存器中的PID[1:0]位为01b（BUF响应）时检测到BEMP中断，则USBHS将PIPEBEMP[9:0]标志中的相关位设置为1。有关BEMP中断的详细信息，请参阅第33.3.6.3节，BEMP中断。

33.2.23 帧号寄存器(FRMNUM)

Address(es): USBHS.FRMNUM 4006 004Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	OVRN	CRCE	—	—	—	FRNM[10:0]										
重置后的值：	0	0	x	x	x	0	0	0	0	0	0	0	0	0	0	0

x: Undefined

Bit	Symbol	位名称	Description	R/W
b10 to b0	FRNM[10:0]	帧号标志	最新帧号	R
b13 to b11	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b14	CRCE	CRC错误检测状态 Flag	0：未发生错误1：发生错误。	R/(W)
b15	OVRN	Overrun/Underrun Detection 状态标志	0：未发生错误1：发生错误。	R/(W)

Note: OVRN标志用于调试。设计时序，使系统不会发生溢出或欠载。

FRNM[10:0]标志（帧号标志）

USBHS设置FRNM[10:0]标志以指示最新的帧号，该帧号每1ms更新一次，当发出或接收SOF数据包时。

CRCE标志（CRC错误检测状态标志）

当同步传输期间发生CRC错误或位填充错误时，CRCE标志设置为1。在检测到CRC错误时，USBHS产生一个内部NRDY中断。

要清除CRCE标志，向其写入0，同时向FRMNUM寄存器中的其他位写入1。

OVRN标志（溢出欠载检测状态标志）

当同步传输期间发生溢出或欠载错误时，OVRN标志设置为1。要清除标志，请写入0

to it while writing 1 to the other bits in the FRMNUM register.

In host controller mode, the OVRN flag sets to 1 on any of the following conditions:

- For a transmitting isochronous pipe, the time to issue an OUT token comes before all of the transmit data is written to the FIFO buffer
- For a receiving isochronous pipe, the time to issue an IN token comes when no FIFO buffer planes are empty.

In device controller mode, the OVRN flag sets to 1 on any of the following conditions:

- For a transmitting isochronous pipe, the IN token is received before all of the transmit data is written to the FIFO buffer
- For a receiving isochronous pipe, the OUT token is received when no FIFO buffer planes are empty.

33.2.24 µFrame Number Register (UFRMNUM)

Address(es): USBHS.UFRMNUM 4006 004Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	DVCHG	—	—	—	—	—	—	—	—	—	—	—	—	UFRNM[2:0]		
Value after reset:	0	x	x	x	x	x	x	x	x	x	x	x	x	0	0	0

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b2 to b0	UFRNM[2:0]	Microframe Number	Microframe number	R
b14 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15	DVCHG	Device State Change	0: Disable writes to the USBADDR.STSRECOV0[2:0] and USBADDR.USBADDR[6:0] bits 1: Enable writes to the USBADDR.STSRECOV0[2:0] and USBADDR.USBADDR[6:0] bits.	R/W

UFRNM[2:0] flags (Microframe Number)

The USBHS sets the UFRNM[2:0] flags to indicate the microframe number during high-speed operation. When not in high-speed operation, the USBHS sets these bits to 00h.

Read these bits repeatedly until the same value is read twice.

33.2.25 USB Address Register (USBADDR)

Address(es): USBHS.USBADDR 4006 0050h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	STSRECOV0[2:0]			—	USBADDR[6:0]						
Value after reset:	x	x	x	x	x	0	0	0	x	0	0	0	0	0	0	0

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b6 to b0	USBADDR[6:0]	USB Address Flag	In device controller mode, these flags indicate the USB address assigned by the host when the USBHS processed the SET_ADDRESS request successfully.	R
b7	—	Reserved	The read value is undefined. The write value should be 0.	R/W

将1写入FRMNUM寄存器中的其他位。

在主机控制器模式下，OVRN标志在以下任何条件下设置为1：

- 对于传输同步管道，发出OUT令牌的时间出现在所有传输数据写入FIFO缓冲区之前
- 对于接收同步管道，在没有FIFO缓冲区平面为空时发出IN令牌。

在设备控制器模式下，OVRN标志在以下任何条件下设置为1：

- 对于传输同步管道，在所有传输数据写入FIFO缓冲区之前接收到IN令牌
- 对于接收同步管道，当没有FIFO缓冲区平面为空时接收OUT令牌。

33.2.24 µFrame编号寄存器(UFRMNUM)

Address(es): USBHS.UFRMNUM 4006 004Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	DVCHG	—	—	—	—	—	—	—	—	—	—	—	—	UFRNM[2:0]		
重置后的值：	0	x	x	x	x	x	x	x	x	x	x	x	x	0	0	0

x: Undefined

Bit	Symbol	位名称	Description	R/W
b2 to b0	UFRNM[2:0]	Microframe Number	Microframe number	R
b14 to b3	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b15	DVCHG	设备状态更改	0：禁止写入USBADDR.STSRECOV0[2:0]和USBADDR.USBADDR[6:0]位1：允许写入USBADDR.STSRECOV0[2:0]和USBADDR.USBADDR[6:0]位。	R/W

UFRNM[2:0]标志（微帧号）

USBHS设置UFRNM[2:0]标志以指示高速操作期间的微帧数。当不处于高速操作时，USBHS将这些位设置为00h。

重复读取这些位，直到读取两次相同的值。

33.2.25 USB地址寄存器(USBADDR)

Address(es): USBHS.USBADDR 4006 0050h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	STSRECOV0[2:0]			—	USBADDR[6:0]						
重置后的值：	x	x	x	x	x	0	0	0	x	0	0	0	0	0	0	0

x: Undefined

Bit	Symbol	位名称	Description	R/W
b6 to b0	USBADDR[6:0]	USB地址标志	在设备控制器模式下，这些标志指示USBHS成功处理SET_ADDRESS请求时主机分配的USB地址。	R
b7	—	Reserved	读取值未定义。写入值应为0。	R/W

Bit	Symbol	Bit name	Description	R/W
b10 to b8	STSRECOV0[2:0]	Status Recovery	• Recovery in device controller mode b10 b8 0 0 1:Return to the full-speed connection and Default state 0 1 0:Return to the full-speed connection and Address state 0 1 1:Return to the full-speed connection and Configured state 1 0 0:Return to the suspend connection and Suspend state 1 0 1:Return to the high-speed connection and Default state 1 1 0:Return to the high-speed connection and Address state 1 1 1:Return to the high-speed connection and Configured state. Other settings are prohibited. • Recovery in host controller mode b10 b8 0 1 0:Return to the low-speed state (bits DVSTCTR0.RHST[2:0] = 001b) 1 0 0:Return to the full-speed state (bits DVSTCTR0.RHST[2:0] = 010b) 1 1 0:Return to the high-speed state (bits DVSTCTR0.RHST[2:0] = 011b). Other settings are prohibited.	R/W
b15 to b11	—	Reserved	The read value is undefined. The write value should be 0.	R/W

USBADDR[6:0] flags (USB Address Flag)

In device controller mode, the USBADDR[6:0] flags indicate the USB address received when the USBHS processed a SetAddress request successfully. The USBHS sets the USBADDR[6:0] bits to 00h on detecting a USB bus reset.

In host controller mode, the USBADDR[6:0] bits are invalid.

STSRECOV0[2:0] bits (Status Recovery)

Use the STSRECOV[3:0] bits to resume the state of the internal sequencer on recovering from USB power shut-off. For details, see section 33.3.17, Release from Deep Software Standby Mode Because of USB Suspend/Resume Interrupts.

Writing to these bits is enabled while the DVCHGR.DVCHG bit is set to 1.

33.2.26 USB Request Type Register (USBREQ)

Address(es): USBHS.USBREQ 4006 0054h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BREQUEST[7:0]								BMREQUESTTYPE[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	BMREQUESTTYPE[7:0]	Request Type	USB request bmRequestType value	R/W*1
b15 to b8	BREQUEST[7:0]	Request	USB request bRequest value	R/W*1

Note 1. In device controller mode, these bits can be read, but writing to them has no effect. In host controller mode, these bits are both read/write bits.

BMREQUESTTYPE[7:0] bits (Request Type)

The BMREQUESTTYPE[7:0] bits hold the bmRequestType value of USB requests.

- In host controller mode:
  Set these bits to the value of the USB request data in transmission setup transactions. Do not change the value of the bits while the DCPCTR.SUREQ bit is 1.
- In device controller mode:
  These bits indicate the value of the USB request data in reception setup transactions. Writing to the bits has no effect.

Bit	Symbol	位名称	Description	R/W
b10 to b8	STSRECOV0[2:0]	状态恢复	在设备控制器模式下恢复b10 0 01：返回全速连接和默认状态 0 10：返回全速连接和地址状态 0 11：返回全速连接和配置状态 1 00：返回挂起连接和挂起状态 1 01：返回高速连接和默认状态 1 10：返回高速连接和地址状态 111：返回高速连接和配置状态。禁止其他设置。 在主机控制器模式下恢复b10 0 10：返回低速状态（位DVSTCTR0.RHST[2:0]=001b） 1 00：返回全速状态（位DVSTCTR0.RHST[2:0]=010b） 110：返回高速状态（位DVSTCTR0.RHST[2:0]=011b）。禁止其他设置。	R/W
b15 to b11	—	Reserved	读取值未定义。写入值应为0。	R/W

USBADDR[6:0]标志（USB地址标志）

在设备控制器模式下，USBADDR[6:0]标志指示当USBHS处理一个SetAddress请求成功。USBHS在检测到USB总线复位时将USBADDR[6:0]位设置为00h。

在主机控制器模式下，USBADDR[6:0]位无效。

STSRECOV0[2:0]位（状态恢复）

使用STSRECOV[3:0]位在从USB电源关闭恢复时恢复内部定序器的状态。有关详细信息，请参阅第33.3.17节，由于USB挂起恢复中断而从深度软件待机模式中释放。

当DVCHGR.DVCHG位设置为1时，可以写入这些位。

33.2.26 USB请求类型寄存器(USBREQ)

Address(es): USBHS.USBREQ 4006 0054h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BREQUEST[7:0]								BMREQUESTTYPE[7:0]							
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b7 to b0	BMREQUESTTYPE[7:0]	请求类型	USB请求bmRequestType值	R/W*1
b15 to b8	BREQUEST[7:0]	Request	USB请求bRequest值	R/W*1

Note 1. 在设备控制器模式下，可以读取这些位，但写入它们无效。在主机控制器模式下，这些位都是读写位。

BMREQUESTTYPE[7:0]位（请求类型）

BMREQUESTTYPE[7:0]位保存USB请求的bmRequestType值。

- 在主机控制器模式下：
  在传输设置事务中将这些位设置为USB请求数据的值。当DCPCTR.SUREQ位为1时，不要更改位的值。
- 在设备控制器模式下：
  这些位指示接收设置事务中USB请求数据的值。写入位无效。

BREQUEST[7:0] bits (Request)

The BREQUEST[7:0] bits hold the bRequest value of USB requests.

- In host controller mode:
  Set these bits to the value of the USB request data in transmission setup transactions. Do not change the value of the bits while the DCPCTR.SUREQ bit is 1.
- In device controller mode:
  These bits indicate the value of the USB request data in reception setup transactions. Writing to the bits has no effect.

33.2.27 USB Request Value Register (USBVAL)

Address(es): USBHS.USBVAL 4006 0056h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	WVALUE[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b15 to b0	WVALUE[15:0]	Value	USB request wValue value	R/W*1

Note 1. In device controller mode, these bits are readable, but writing to them has no effect. In host controller mode, these bits are both read/write bits.

WVALUE[15:0] bits (Value)

The WVALUE[15:0] bits hold the wValue value of USB requests.

- In host controller mode:
  Set these bits to the wValue value for USB requests in transmission setup transactions. Do not change the value of the bits while the DCPCTR.SUREQ bit is 1.
- In device controller mode:
  These bits indicate the wValue value of USB requests in reception setup transactions. Writing to the bits has no effect.

33.2.28 USB Request Index Register (USBINDX)

Address(es): USBHS.USBINDX 4006 0058h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	WINDEX[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b15 to b0	WINDEX[15:0]	Index	USB request wIndex value	R/W*1

Note 1. In device controller mode, these bits are readable, but writing to them has no effect. In host controller mode, these bits are both read/write bits.

WINDEX[15:0] bits (Index)

The WINDEX[15:0] bits hold the wIndex value of USB requests.

- In host controller mode:
  Set these bits to the wIndex value of USB requests in transmission setup transactions. Do not change the value of

BREQUEST[7:0]位（请求）

BREQUEST[7:0]位保存USB请求的bRequest值。

- 在主机控制器模式下：
  在传输设置事务中将这些位设置为USB请求数据的值。当DCPCTR.SUREQ位为1时，不要更改位的值。
- 在设备控制器模式下：
  这些位指示接收设置事务中USB请求数据的值。写入位无效。

33.2.27 USB请求值寄存器(USBVAL)

Address(es): USBHS.USBVAL 4006 0056h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	WVALUE[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b15 to b0	WVALUE[15:0]	Value	USB请求wValue值	R/W*1

Note 1. 在设备控制器模式下，这些位是可读的，但写入它们没有效果。在主机控制器模式下，这些位都是读写位。

WVALUE[15:0]位（值）

WVALUE[15:0]位保存USB请求的wValue值。

- 在主机控制器模式下：
  将这些位设置为传输设置事务中USB请求的wValue值。当DCPCTR.SUREQ位为1时，不要更改位的值。
- 在设备控制器模式下：
  这些位指示接收设置事务中USB请求的wValue值。写入位无效。

33.2.28 USB请求索引寄存器(USBINDX)

Address(es): USBHS.USBINDX 4006 0058h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	WINDEX[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b15 to b0	WINDEX[15:0]	Index	USB请求wIndex值	R/W*1

Note 1. 在设备控制器模式下，这些位是可读的，但写入它们没有效果。在主机控制器模式下，这些位都是读写位。

WINDEX[15:0]位（索引）

WINDEX[15:0]位保存USB请求的wIndex值。

- 在主机控制器模式下：
  将这些位设置为传输设置事务中USB请求的wIndex值。不改变值

the bits while the DCPCTR.SUREQ bit is 1.

- In device controller mode:
  These bits indicate the wIndex value of USB requests received in reception setup transactions. Writing to the bits has no effect.

33.2.29 USB Request Length Register (USBLENG)

Address(es): USBHS.USBLENG 4006 005Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	WLENTUH[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b15 to b0	WLENTUH[15:0]	Length	USB request wLength value	R/W*1

Note 1. In device controller mode, these bits are readable, but writing to them has no effect. In host controller mode, these bits are both read/write bits.

WLENTUH[15:0] bits (Length)

The WLENTUH[15:0] bits hold the wLength value of USB requests.

- In host controller mode:
  Set the wLength value of USB requests in transmission setup transactions. Do not change the value of the bits while the DCPCTR.SUREQ bit is 1.
- In device controller mode:
  These bits indicate the wLength value of USB requests in reception setup transactions. Writing to the bits has no effect.

33.2.30 DCP Configuration Register (DCPCFG)

Address(es): USBHS.DCPCFG 4006 005Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	CNTMD	SHTNAK	—	—	DIR	—	—	—	—
Value after reset:	x	x	x	x	x	x	x	0	0	x	x	0	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b3 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	DIR	Transfer Direction	0: Data receiving direction 1: Data transmitting direction.	R/W
b6, b5	—	Reserved	The read value is undefined. The write value should be 0.	R/W
b7	SHTNAK	Pipe Blocking on End of Transfer	0: Keep pipe open after transfer ends 1: Disable pipe after transfer ends.	R/W
b8	CNTMD	Continuous Transfer Mode	0: Non-continuous transfer mode 1: Continuous transfer mode.	R/W
b15 to b9	—	Reserved	The read value is undefined. The write value should be 0.	R/W

Note 1. Only set the bits in this register while the PID is NAK. Before setting the bits, check that the DCPCTR.PBUSY bit is 0, and then change the DCPCTR.PID[1:0] bits for the DCP from BUF to NAK. If the PID[1:0] bits are changed to NAK by the USBHS, checking the PBUSY bit through software is not necessary.

DCPCTR.SUREQ位为1时的位。

- 在设备控制器模式下：
  这些位指示在接收设置事务中接收到的USB请求的wIndex值。写入位无效。

33.2.29 USB请求长度寄存器(USBLENG)

Address(es): USBHS.USBLENG 4006 005Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	WLENTUH[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b15 to b0	WLENTUH[15:0]	Length	USB请求wLength值	R/W*1

Note 1. 在设备控制器模式下，这些位是可读的，但写入它们没有效果。在主机控制器模式下，这些位都是读写位。

WLENTUH[15:0]位（长度）

WLENTUH[15:0]位保存USB请求的wLength值。

- 在主机控制器模式下：
  在传输设置事务中设置USB请求的wLength值。当DCPCTR.SUREQ位为1时，不要更改位的值。
- 在设备控制器模式下：
  这些位指示接收设置事务中USB请求的wLength值。写入位无效。

33.2.30 DCP配置寄存器(DCPCFG)

Address(es): USBHS.DCPCFG 4006 005Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	CNTMD	SHTNAK	—	—	DIR	—	—	—	—
重置后的值：	x	x	x	x	x	x	x	0	0	x	x	0	x	x	x	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b3 to b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b4	DIR	转移方向	0：数据接收方向1：数据发送方向。	R/W
b6, b5	—	Reserved	读取值未定义。写入值应为0。	R/W
b7	SHTNAK	管道末端堵塞 Transfer	0：传输结束后保持管道打开1：传输结束后禁用管道。	R/W
b8	CNTMD	连续传输模式	0：非连续传输模式1：连续传输模式。	R/W
b15 to b9	—	Reserved	读取值未定义。写入值应为0。	R/W

Note 1. 仅在PID为NAK时设置此寄存器中的位。在设置这些位之前，检查DCPCTR.PBUSY位是否为0，然后将DCP的DCPCTR.PID[1:0]位从BUF更改为NAK。如果PID[1:0]位被USBHS更改为NAK，则无需通过软件检查PBUSY位。

DIR bit (Transfer Direction)

In host controller mode, the DIR bit sets the transfer direction of the data stage and status stage for control transfers. In device controller mode, set the DIR bit to 0.

SHTNAK bit (Pipe Blocking on End of Transfer)

The SHTNAK bit specifies whether to change PID to NAK on transfer end when the selected pipe is receiving. It is only valid when the selected pipe is receiving.

When the SHTNAK bit is 1, the USBHS changes the DCPCTR.PID[1:0] bits for the DCP to NAK on determining that a transfer has ended. The USBHS determines transfer end on the following condition:

- A short packet, including a zero-length packet, is successfully received.

CNTMD bit (Continuous Transfer Mode)

The CNTMD bit indicates whether transfer through the default control pipe is in continuous transfer mode.

33.2.31 DCP Maximum Packet Size Register (DCPMAXP)

Address(es): USBHS.DCPMAXP 4006 005Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	DEVSEL[3:0]				—	—	—	—	—	MXPS[6:0]						
Value after reset:	0	0	0	0	x	x	x	x	x	1	0	0	0	0	0	0

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b6 to b0	MXPS[6:0]	Maximum Packet Size*1	Maximum data payload specification (maximum packet size) for the DCP	R/W
b11 to b7	—	Reserved	The read value is undefined. The write value should be 0.	R/W
b15 to b12	DEVSEL[3:0]	Device Select*2	b15 b12 0 0 0 0: Address 0000b 0 0 0 1: Address 0001b 0 0 1 0: Address 0010b 0 0 1 1: Address 0011b 0 1 0 0: Address 0100b 0 1 0 1: Address 0101b 0 1 1 0: Address 0110b 0 1 1 1: Address 0111b 1 0 0 0: Address 1000b 1 0 0 1: Address 1001b 1 0 1 0: Address 1010b Other settings are prohibited.	R/W

Note 1. Only set the MXPS[6:0] bits while PID is NAK. Before setting this bit, check that the CSSTS and PBUSY bits are 0, and then change the DCPCTR.PID[1:0] bits from 01b (BUF) to 00b (NAK), and the CFIFOSEL.CURPIPE[3:0] bits to 0000b. If the DCPCTR.PID[1:0] bits are changed to 00b (NAK) by the USBHS, checking the CSSTS and PBUSY bits through software is not necessary. After the MXPS[6:0] bits are set and the DCP is set to the CURPIPE[3:0] bits in a port select register, clear the buffer by setting the BCLR bit the port control register to 1.

Note 2. Only set the DEVSEL[3:0] bits while PID is NAK and the DCPCTR.SUREQ bits are 0. Before setting these bits, check that the CSSTS and PBUSY flags are 0, and then change the DCPCTR.PID[1:0] bits from 01b (BUF) to 00b (NAK), and the DCPCTR.SUREQ[3:0] bits to 0. If the DCPCTR.PID[1:0] bits are changed to 00b (NAK) by the USBHS, checking the CSSTS and PBUSY bits through software is not necessary.

MXPS[6:0] bits (Maximum Packet Size)

The MXPS[6:0] bits specify the maximum data payload (maximum packet size) for the DCP. The initial value is 40h (64 bytes). Set the bits to a USB 2.0-compliant value. Do not write to the FIFO buffer or set PID = BUF while MXPS[6:0] is set to 0.

DIR位（传输方向）

在主机控制器模式下，DIR位设置控制传输的数据阶段和状态阶段的传输方向。在设备控制器模式下，将DIR位设置为0。

SHTNAK位（传输结束时管道阻塞）

SHTNAK位指定当所选管道正在接收时，是否在传输结束时将PID更改为NAK。仅在所选管道正在接收时有效。

当SHTNAK位为1时，USBHS在确定传输已经结束时将DCPCR.PID[1:0]位更改为NAK。USBHS在以下条件下确定传输结束：

- 成功接收到一个短数据包，包括一个长度为零的数据包。

CNTMD位（连续传输模式）

CNTMD位指示通过默认控制管道的传输是否处于连续传输模式。

33.2.31 DCP最大数据包大小寄存器(DCPMAXP)

Address(es): USBHS.DCPMAXP 4006 005Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	DEVSEL[3:0]				—	—	—	—	—	MXPS[6:0]						
重置后的值：	0	0	0	0	x	x	x	x	x	1	0	0	0	0	0	0

x: Undefined

Bit	Symbol	位名称	Description	R/W
b6 to b0	MXPS[6:0]	最大数据包大小 *1	DCP的最大数据有效负载规范（最大数据包大小）	R/W
b11 to b7	—	Reserved	读取值未定义。写入值应为0。	R/W
b15 to b12	DEVSEL[3:0]	设备选择 *2	b15 b12 0 0 0 0: Address 0000b 0 0 0 1: Address 0001b 0 0 1 0: Address 0010b 0 0 1 1: Address 0011b 0 1 0 0: Address 0100b 0 1 0 1: Address 0101b 0 1 1 0: Address 0110b 0 1 1 1: Address 0111b 1 0 0 0: Address 1000b 1 0 0 1: Address 1001b 1 0 1 0: Address 1010b 禁止其他设置。	R/W

Note 1. 仅在PID为NAK时设置MXPS[6:0]位。在设置该位之前，检查CSSTS和PBUSY位是否为0，然后将DCPCTR.PID[1:0]位从01b(BUF)更改为00b(NAK)，以及CFIFOSEL.CURPIPE[3:0]位到0000b。如果DCPCTR.PID[1:0]位被USBHS更改为00b(NAK)，则无需通过软件检查CSSTS和PBUSY位。在设置MXPS[6:0]位并将DCP设置为端口选择寄存器中的CURPIPE[3:0]位后，通过将端口控制寄存器的BCLR位设置为1来清除缓冲区。

Note 2. 仅在PID为NAK且DCPCTR.SUREQ位为0时设置DEVSEL[3:0]位。在设置这些位之前，请检查CSSTS和PBUSY标志是否为0，然后更改DCPCTR.PID[1:0]从01b(BUF)到00b(NAK)的位，以及
DCPCTR.SUREQ[3:0]位为0。如果DCPCTR.PID[1:0]位被USBHS更改为00b(NAK)，则无需通过软件检查CSSTS和PBUSY位。

MXPS[6:0]位（最大数据包大小）

MXPS[6:0]位指定DCP的最大数据有效载荷（最大数据包大小）。初始值为40h（64字节）。将这些位设置为符合USB2.0的值。当MXPS[6:0]设置为0时，不要写入FIFO缓冲区或设置PID=BUF。

DEVSEL[3:0] bits (Device Select)

In host controller mode, the DEVSEL[3:0] bits specify the address of the target peripheral device for a control transfer. Set up the device address in the associated DEVADDm (m = 0 to A) register first, and then set these bits to the corresponding value. To set the DEVSEL[3:0] bits to 0010b, for example, first set the address in the DEVADD2 register.

In device controller mode, set these bits to 0000b.

33.2.32 DCP Control Register (DCPCTR)

Address(es): USBHS.DCPCTR 4006 0060h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BSTS	SUREQ	CSCLR	CSSTS	SUREQCLR	—	—	SQCLR	SQSET	SQMON	PBUSY	PINGE	—	CCPL	PID[1:0]	
Value after reset:	0	0	0	0	x	x	x	0	0	1	0	0	x	0	0	0

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b1, b0	PID[1:0]	Response PID	b1 b0 0 0: NAK response 0 1: BUF response (depends on buffer state) 1 0: STALL response 1 1: STALL response.	R/W
b2	CCPL	Control Transfer End Enable	0: Disable control transfer completion 1: Enable control transfer completion.	R/W
b3	—	Reserved	The read value is undefined. The write value should be 0.	R/W
b4	PINGE	PING Token Issue Enable*1	0: Disable PING token 1: Enable normal PING operation.	R/W
b5	PBUSY	Pipe Busy Flag	0: DCP not used for the USB bus 1: DCP in use for the USB bus.	R
b6	SQMON	Sequence Toggle Bit Monitor Flag	0: DATA0 1: DATA1.	R
b7	SQSET	Sequence Toggle Bit Set*1	Sets the sequence toggle bit in DCP transfers. 0: Invalid (writing 0 has no effect) 1: Set the expected value for the next transaction to DATA1. This bit is read as 0.	R/W
b8	SQCLR	Sequence Toggle Bit Clear*1	Clears the sequence toggle bit in DCP transfers. 0: Invalid (writing 0 has no effect) 1: Clear the expected value for the next transaction to DATA0. This bit is read as 0.	R/W
b10, b9	—	Reserved	The read value is undefined. The write value should be 0.	R/W
b11	SUREQCLR	SUREQ Bit Clear	Clears the SUREQ bit in host controller mode. 0: Invalid (writing 0 has no effect) 1: Clear SUREQ to 0. This bit is read as 0.	R/W
b12	CSSTS	CSSTS Status Flag	0: Start-split (SSPLIT) transaction, or processing for devices that are not using split transactions, in progress. 1: Complete-split (CSPLIT) transaction in progress.	R
b13	CSCLR	CSSTS Status Flag Clear	Clears the CSSTS flag in host controller mode for split transactions, resuming the next DCP transfer from SSPLIT. 0: Invalid (writing 0 has no effect) 1: Clear CSSTS to 0. This bit is read as 0.	R/W
b14	SUREQ	SETUP Token Transmission	Sets up token transmission in host controller mode. 0: Invalid (writing 0 has no effect) 1: Transmit setup packet.	R/W
b15	BSTS	Buffer Status Flag	0: Buffer access disabled 1: Buffer access enabled.	R

DEVSEL[3:0]位（设备选择）

在主机控制器模式下，DEVSEL[3:0]位指定目标外围设备的地址以进行控制传输。首先在相关的DEVADDm（m=0到A）寄存器中设置设备地址，然后将这些位设置为相应的值。例如，要将DEVSEL[3:0]位设置为0010b，首先要设置DEVADD2寄存器中的地址。

在设备控制器模式下，将这些位设置为0000b。

33.2.32 DCP控制寄存器(DCPCTR)

Address(es): USBHS.DCPCTR 4006 0060h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BSTS	SUREQ	CSCLR	CSSTS	SUREQCLR	—	—	SQCLR	SQSET	SQMON	PBUSY	PINGE	—	CCPL	PID[1:0]	
重置后的值：	0	0	0	0	x	x	x	0	0	1	0	0	x	0	0	0

x: Undefined

Bit	Symbol	位名称	Description	R/W
b1, b0	PID[1:0]	响应PID	b1 b0 0 0：NAK响应 0 1：BUF响应（取决于缓冲区状态） 1 0：停止响应 1 1：停止响应。	R/W
b2	CCPL	控制传输结束使能	0：禁用控制传输完成1：启用控制传输完成。	R/W
b3	—	Reserved	读取值未定义。写入值应为0。	R/W
b4	PINGE	PING令牌发布启用 *1	0：禁用PING令牌1：启用正常PING操作。	R/W
b5	PBUSY	管道忙标志	0：USB总线不使用DCP1：USB总线使用DCP。	R
b6	SQMON	序列切换位监视器 Flag	0: DATA0 1: DATA1.	R
b7	SQSET	序列切换位设置 *1	设置DCP传输中的序列切换位。0：无效（写0无效）1：将下一笔交易的期望值设置为DATA1。该位读为0。	R/W
b8	SQCLR	序列切换位清除 *1	清除DCP传输中的序列切换位。0：无效（写0无效）1：清除下一笔交易的期望值到DATA0。该位读为0。	R/W
b10, b9	—	Reserved	读取值未定义。写入值应为0。	R/W
b11	SUREQCLR	SUEQ位清零	在主机控制器模式下清除SUREQ位。0：无效（写0无效）1：将SUREQ清0。该位读为0。	R/W
b12	CSSTS	CSSTS状态标志	0：开始拆分(SSPLIT)事务，或正在处理未使用拆分事务的设备。1：完成拆分（CSPLIT）事务正在进行中。	R
b13	CSCLR	CSSTS状态标志清除	在主机控制器模式下清除CSSTS标志以进行拆分事务，从SSPLIT恢复下一次DCP传输。0：无效（写0无效）1：将CSSTS清0。该位读为0。	R/W
b14	SUREQ	SETUP令牌传输	在主机控制器模式下设置令牌传输。0：无效（写0无效）1：发送设置包。	R/W
b15	BSTS	缓冲区状态标志	0：禁止缓冲区访问1：允许缓冲区访问。	R

Note 1. Only set the SQSET, SQCLR, and PINGE bits while PID is NAK. Before setting these bits, check that the CSSTS and PBUSY bits are 0, and then change the DCPCTR.PID[1:0] bits from 01b (BUF) to 00b (NAK). If the DCPCTR.PID[1:0] bits are changed to 00b (NAK) by the USBHS, checking the CSSTS and PBUSY bits through the software is not necessary.

PID[1:0] bits (Response PID)

The PID[1:0] bits control the USB response type during control transfers.

In host controller mode, to change the PID[1:0] setting from NAK to BUF:

- When the transmitting direction is set:
  a. Write all of the transmit data to the FIFO buffer while the DVSTCTR0.UACT bit is 1 and PID is NAK.
  b. Set PID[1:0] bits to 01b (BUF).
  The USBHS then executes the OUT transaction (or PING transaction).
- When the receiving direction is set:
  c. Check that the FIFO buffer is empty (or empty the buffer) while the DVSTCTR0.UACT bit is 1 and PID is NAK.
  d. Set PID[1:0] bits to 01b (BUF).
  The USBHS then executes the IN transaction.

The USBHS changes the PID[1:0] setting as follows:

- When the PID[1:0] bits are set to BUF (01b) by software and the USBHS has received data exceeding MaxPacketSize, the USBHS sets PID[1:0] to STALL (11b)
- When a reception error, such as a CRC error, is detected three times consecutively, the USBHS sets PID[1:0] to NAK (00b)
- On receiving the STALL handshake, the USBHS sets PID[1:0] to STALL (11b).

In device controller mode, the USBHS changes the PID[1:0] setting as follows:

- On receiving a setup packet, the USBHS sets PID[1:0] to NAK (00b). The USBHS then sets the INTSTS0.VALID flag to 1, and the PID[1:0] setting cannot be changed until the software clears the VALID flag to 0.
- When the PID[1:0] bits are set to BUF (01b) by software and the USBHS has received data exceeding MaxPacketSize, the USBHS sets PID[1:0] to STALL (11b)
- On detecting a control transfer sequence error, the USBHS sets PID[1:0] to STALL (1xb)
- On detecting a USB bus reset, the USBHS sets PID[1:0] to NAK.

The USBHS does not check the PID[1:0] setting while processing a SET_ADDRESS request.

CCPL bit (Control Transfer End Enable)

In device controller mode, setting the CCPL bit to 1 enables the status stage of the control transfer to be completed. When the bit is set to 1 by software while the associated PID[1:0] bits are set to BUF, the USBHS completes the control transfer status stage.

During control read transfers, the USBHS transmits the ACK handshake in response to the OUT transaction from the USB host. During control write or no-data control transfers, it transmits the zero-length packet in response to the IN transaction from the USB host. On detecting a SET_ADDRESS request, the USBHS operates in auto response mode from the setup stage up to status stage completion regardless of the CCPL bit setting.

The USBHS changes the CCPL bit from 1 to 0 on receiving a new setup packet. The software cannot write 1 to the bit while the INTSTS0.VALID bit is 1. The bit is initialized by a USB bus reset.

In host controller mode, always write 0 to the CCPL bit.

PINGE bit (PING Token Issue Enable)

In host controller mode, when the software sets the PINGE bit to 1, the USBHS issues a PING token for transfer in the transmitting direction, which triggers the transfer to start. If an ACK handshake is detected in the PING transaction, the OUT transaction is executed in the next transaction. If a NAK or NYET handshake is detected in the OUT transaction, the PING transaction is executed in the next transaction.

Note 1. 仅在PID为NAK时设置SQSET、SQCLR和PINGE位。在设置这些位之前，请检查CSSTS和PBUSY位是否为0，然后将DCPCTR.PID[1:0]位从01b(BUF)更改为00b(NAK)。如果DCPCTR.PID[1:0]位被USBHS更改为00b(NAK)，则无需通过软件检查CSSTS和PBUSY位。

PID[1:0]位（响应PID）

PID[1:0]位在控制传输期间控制USB响应类型。

在主机控制器模式下，要将PID[1:0]设置从NAK更改为BUF：

- 设置传输方向时：
  一个。当DVSTCTR0.UACT位为1且PID为NAK时，将所有发送数据写入FIFO缓冲区。
  湾。将PID[1:0]位设置为01b(BUF)。
  然后USBHS执行OUT事务（或PING事务）。
- 设置接收方向时：
  C。在DVSTCTR0.UACT位为1且PID为NAK时检查FIFO缓冲区是否为空（或清空缓冲区）。
  d。将PID[1:0]位设置为01b(BUF)。
  然后USBHS执行IN事务。

USBHS将PID[1:0]设置更改如下：

- 当PID[1:0]位被软件设置为BUF(01b)并且USBHS接收到的数据超过MaxPacketSize，USBHS将PID[1:0]设置为STALL(11b)
- 当连续3次检测到接收错误（例如CRC错误）时，USBHS将PID[1:0]设置为NAK (00b)
- 在接收到STALL握手时，USBHS将PID[1:0]设置为STALL(11b)。

在设备控制器模式下，USBHS将PID[1:0]设置更改如下：

- 接收到设置数据包后，USBHS将PID[1:0]设置为NAK(00b)。然后USBHS将INTSTS0.VALID标志设置为1，并且在软件将VALID标志清除为0之前无法更改PID[1:0]设置。
- 当PID[1:0]位被软件设置为BUF(01b)并且USBHS接收到的数据超过MaxPacketSize，USBHS将PID[1:0]设置为STALL(11b)
- 在检测到控制传输序列错误时，USBHS将PID[1:0]设置为STALL(1xb)
- 在检测到USB总线复位时，USBHS将PID[1:0]设置为NAK。

USBHS在处理SET_ADDRESS请求时不检查PID[1:0]设置。

CCPL位（控制传输结束使能）

在设备控制器模式下，将CCPL位设置为1可以完成控制传输的状态阶段。
当该位由软件设置为1且相关的PID[1:0]位设置为BUF时，USBHS完成控制传输状态阶段。

在控制读取传输期间，USBHS发送ACK握手以响应来自USB主机的OUT事务。在控制写入或无数据控制传输期间，它传输零长度数据包以响应来自USB主机的IN事务。在检测到SET_ADDRESS请求时，USBHS从设置阶段到状态阶段完成以自动响应模式运行，无论CCPL位设置如何。

USBHS在接收到新的设置数据包时将CCPL位从1更改为0。当INTSTS0.VALID位为1时，软件无法向该位写入1。该位由USB总线复位初始化。

在主机控制器模式下，始终将0写入CCPL位。

PINGE位（PING令牌发布启用）

在主机控制器模式下，当软件将PINGE位设置为1时，USBHS会发出一个PING令牌以进行传输方向的传输，从而触发传输开始。如果在PING事务中检测到ACK握手，则在 下一个事务中执行OUT事务。如果在OUT事务中检测到NAK或NYET握手，则在 下一个事务中执行PING事务。

If the software sets this bit to 0, the USBHS issues no PING token for transfer in the transmitting direction. All transfers in the transmitting direction are executed in the OUT transaction.

PBUSY flag (Pipe Busy Flag)

The PBUSY bit indicates whether DCP is used for the transaction when USBHS changes the PID[1:0] bits from BUF to NAK. The USBHS changes the PBUSY flag from 0 to 1 on start of a USB transaction for the selected pipe. It changes the PBUSY flag from 1 to 0 on completion of one transaction.

After PID is set to NAK by software, the value in the PBUSY flag indicates whether changes to pipe settings can proceed.

For details, see section 33.3.7.1, Pipe control register switching procedures.

SQMON flag (Sequence Toggle Bit Monitor Flag)

The SQMON bit indicates the expected value of the sequence toggle bit for the next transaction during a DCP transfer.

The USBHS toggles the bit on normal completion of the transaction. It does not toggle the bit, however, when a DATA-PID mismatch occurs during a transfer in the receiving direction.

In device controller mode, the USBHS sets the SQMON bit to 1 (specifies DATA1 as the expected value) on successful reception of the setup packet.

In device controller mode, the USBHS does not reference this bit during IN or OUT transactions at the status stage, and it does not toggle the bit on normal completion.

SQSET bit (Sequence Toggle Bit Set)

The SQSET bit specifies DATA1 as the expected value of the sequence toggle bit for the next transaction during a DCP transfer.

Do not set the SQCLR and SQSET bits to 1 simultaneously.

SQCLR bit (Sequence Toggle Bit Clear)

The SQCLR bit specifies DATA0 as the expected value of the sequence toggle bit for the next transaction during a DCP transfer. It is read as 0.

Do not set the SQCLR and SQSET bits to 1 simultaneously.

SUREQCLR bit (SUREQ Bit Clear)

In host controller mode, setting the SUREQCLR bit to 1 clears the SUREQ bit to 0. The bit is read as 0.

If transfer stops while the SUREQ bit is set to 1 in a setup transaction, set the SUREQCLR bit to 1 through software. This is not necessary at the end of a normal setup transaction, because the USBHS automatically clears the SUREQ bit to 0.

Only control the SUREQ bit through the SUREQCLR bit while the DVSTCTR0.UACT bit is 0. When UACT is 0, communication is halted or no transfer is occurring because a bus disconnection was detected.

In device controller mode, always write 0 to the SUREQCLR bit.

CSSTS flag (CSSTS Status Flag)

In host controller mode, the CSSTS flag indicates the complete-split state in split transactions for pipes that are not isochronous. The USBHS sets the CSSTS flag to 1 at the beginning of a complete-split transaction and sets the flag back to 0 when it detects transaction completion.

Values read from the CSSTS flag in device controller mode are invalid.

CSCLR bit (CSSTS Status Flag Clear)

In host controller mode, setting the CSCLR bit to 1 clears the CSSTS bit to 0.

Set this bit to 1 through software when forcing the next transfer to restart from start-split in transfers using split transactions. This is not necessary at the end of a successful complete-split transaction in a normal split transaction, because the USBHS automatically clears the CSSTS flag to 0.

如果软件将此位设置为0，则USBHS不会发出PING令牌以进行传输方向的传输。发送方向的所有传输都在OUT事务中执行。

PBUSY标志（管道忙标志）

当USBHS将PID[1:0]位从BUF更改为
纳克。USBHS在所选管道的USB事务开始时将PBUSY标志从0更改为1。它在一个事务完成时将PBUSY标志从1更改为0。

软件将PID设置为NAK后，PBUSY标志中的值指示是否可以继续对管道设置进行更改。

详见33.3.7.1管道控制寄存器切换流程。

SQMON标志（序列切换位监视器标志）

SQMON位指示DCP传输期间下一个事务的序列切换位的预期值。

USBHS在事务正常完成时切换该位。然而，它不会切换该位，当一个DATA
PID不匹配发生在接收方向的传输过程中。

在设备控制器模式下，USBHS在成功接收到设置数据包时将SQMON位设置为1（指定DATA1作为预期值）。

在设备控制器模式下，USBHS在状态阶段的IN或OUT事务期间不参考该位，并且在正常完成时不切换该位。

SQSET位（序列切换位设置）

SQSET位将DATA1指定为DCP传输期间下一个事务的序列切换位的预期值。

不要同时将SQCLR和SQSET位设置为1。

SQCLR位（序列切换位清除）

SQCLR位将DATA0指定为DCP传输期间下一个事务的序列切换位的预期值。读为0。

不要同时将SQCLR和SQSET位设置为1。

SUREQCLR位（SUREQ位清零）

在主机控制器模式下，将SUREQCLR位设置为1会将SUREQ位清除为0。该位被读取为0。

如果在设置事务中将SUREQ位设置为1时传输停止，则通过软件将SUREQCLR位设置为1。
这在正常设置事务结束时不是必需的，因为USBHS会自动将SUREQ位清除为0。

当DVSTCTR0.UACT位为0时，仅通过SUREQCLR位控制SUREQ位。当UACT为0时，由于检测到总线断开，通信停止或没有传输发生。

在设备控制器模式下，始终将0写入SUREQCLR位。

CSSTS标志（CSSTS状态标志）

在主机控制器模式下，CSSTS标志指示非同步管道的拆分事务中的完全拆分状态。USBHS在完全拆分事务开始时将CSSTS标志设置为1，并在检测到事务完成时将该标志设置回0。

在设备控制器模式下从CSSTS标志读取的值无效。

CSCLR位（CSSTS状态标志清除）

在主机控制器模式下，将CSCLR位设置为1会将CSSTS位清零。

在使用拆分事务的传输中强制下一次传输从start-split重新启动时，通过软件将此位设置为1。在正常拆分事务中成功完成拆分事务结束时，这不是必需的，因为USBHS会自动将CSSTS标志清除为0。

Only control the CSSTS flag through the CSCLR bit while the DVSTCTR0.UACT bit is 0. When UACT is 0, communication is halted or no transfer is occurring because a port disconnection was detected. Writing 1 to this bit while the CSSTS flag is 0 has no effect; the flag remains 0.

In device controller mode, always write 0 to this bit.

SUREQ bit (SETUP Token Transmission)

In host controller mode, setting the SUREQ bit to 1 triggers the USBHS to transmit the setup packet. After completing the setup transaction process, the USBHS generates either the SACK or SIGN interrupt and clears the SUREQ bit to 0. The USBHS also clears the SUREQ bit to 0 when the software sets the SUREQCLR bit to 1.

Before setting the SUREQ bit to 1, set the DCPMAXP.DEVSEL[3:0] bits, USBREQ, USBVAL, USBINDX, and USBLENG appropriately to transmit the wanted USB request in the setup transaction. Also check that the PID[1:0] bits for the DCP are set to NAK. After setting the SUREQ bit to 1, do not change the DCPMAXP.DEVSEL[3:0] bits, USBREQ, USBVAL, USBINDX, or USBLENG until the setup transaction is complete (SUREQ bit = 1). Write 1 to the SUREQ bit only when transmitting the setup token. Otherwise, write 0.

In device controller mode, always write 0 to this bit.

BSTS flag (Buffer Status Flag)

The BSTS flag indicates the status of access to the DCP FIFO buffer. The meaning of this flag varies as follows depending on the CFIFOSEL.ISEL setting:

- When ISEL = 0, the bit indicates whether receive data can be read from the buffer
- When ISEL = 1, the bit indicates whether transmit data can be written to the buffer.

33.2.33 Pipe Window Select Register (PIPESEL)

Address(es): USBHS.PIPESEL 4006 0064h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	PIPESEL[3:0]			
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	0	0	0	0

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b3 to b0	PIPESEL[3:0]	Pipe Window Select	b3 b0 0 0 0 0: No pipe selected 0 0 0 1: Pipe 1 0 0 1 0: Pipe 2 0 0 1 1: Pipe 3 0 1 0 0: Pipe 4 0 1 0 1: Pipe 5 0 1 1 0: Pipe 6 0 1 1 1: Pipe 7 1 0 0 0: Pipe 8 1 0 0 1: Pipe 9. Other settings are prohibited.	R/W
b15 to b4	—	Reserved	The read value is undefined. The write value should be 0.	R/W

Set pipes 1 to 9 using the PIPESEL, PIPECFG, PIPEMAXP, PIPEPERI, PIPEnCTR, PIPEnTRE, and PIPEnTRN registers (n = 0 to 9).

After selecting the pipe in the PIPESEL register, pipe functions must be set in the associated PIPECFG, PIPEMAXP, and PIPEPERI registers. PIPEnCTR, PIPEnTRE, and PIPEnTRN can be set independently of the pipe selection in this register.

PIPESEL[3:0] bits (Pipe Window Select)

The PIPESEL[3:0] bits select the pipe number associated with the PIPECFG, PIPEMAXP, and PIPEPERI registers used

仅当DVSTCTR0.UACT位为0时，通过CSCLR位控制CSSTS标志。当UACT为0时，由于检测到端口断开，通信停止或不发生传输。CSSTS标志为0时向该位写入1无效；标志保持为0。

在设备控制器模式下，始终向该位写入0。

SUREQ位（SETUP令牌传输）

在主机控制器模式下，将SUREQ位设置为1会触发USBHS发送设置数据包。完成设置事务处理后，USBHS产生SACK或SIGN中断并将SUREQ位清零。当软件将SUREQCLR位设置为1时，USBHS也将SUREQ位清零。

在将SUREQ位设置为1之前，适当地设置DCPMAXP.DEVSEL[3:0]位、USBREQ、USBVAL、USBINDX和USBLENG以在设置事务中传输所需的USB请求。还要检查DCP的PID[1:0]位是否设置为NAK。将SUREQ位设置为1后，在设置事务完成（SUREQ位=1）之前，不要更改DCPMAXP.DEVSEL[3:0]位、USBREQ、USBVAL、USBINDX或USBLENG。将1写入

仅在发送设置令牌时才使用SUEQ位。否则，写0。

在设备控制器模式下，始终向该位写入0。

BSTS标志（缓冲区状态标志）

BSTS标志指示访问DCPFIFO缓冲区的状态。根据CFIFOSEL.ISEL设置，该标志的含义如下：

- 当ISEL=0时，该位指示是否可以从缓冲区中读取接收数据
- 当ISEL=1时，该位指示是否可以将发送数据写入缓冲区。

33.2.33 管道窗口选择寄存器(PIPESEL)

Address(es): USBHS.PIPESEL 4006 0064h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	PIPESEL[3:0]			
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	0	0	0	0

x: Undefined

Bit	Symbol	位名称	Description	R/W
b3 to b0	PIPESEL[3:0]	管道窗口选择	b3 b0 0 0 0 0：未选择管道 0 0 0 1: Pipe 1 0 0 1 0: Pipe 2 0 0 1 1: Pipe 3 0 1 0 0: Pipe 4 0 1 0 1: Pipe 5 0 1 1 0: Pipe 6 0 1 1 1: Pipe 7 1 0 0 0: Pipe 8 01：管道9。禁止其他设置。	R/W
b15 to b4	—	Reserved	读取值未定义。写入值应为0。	R/W

使用PIPESEL、PIPECFG、PIPEMAXP、PIPEPERI、PIPEnCTR、PIPEnTRE和PIPEnTRN寄存器（n=0到9）设置管道1到9。

在PIPESEL寄存器中选择管道后，必须在相关的PIPECFG、PIPEMAXP和PIPEPERI寄存器。PIPEnCTR、PIPEnTRE和PIPEnTRN可以独立于该寄存器中的管道选择进行设置。

PIPESEL[3:0]位（管道窗口选择）

PIPESEL[3:0]位选择与使用的PIPECFG、PIPEMAXP和PIPEPERI寄存器相关的管道编号

for data writing and reading. Selecting a pipe number in the PIPESEL[3:0] bits allows writing to and reading from PIPECFG, PIPEMAXP, and PIPEPERI associated with the selected pipe number.

When PIPESEL[3:0] = 0000b, 0 is read from all of the bits in PIPECFG, PIPEMAXP, and PIPEPERI. Writing to these bits has no effect.

33.2.34 Pipe Configuration Register (PIPECFG)

Address(es): USBHS.PIPECFG 4006 0068h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TYPE[1:0]		—	—	—	BFRE	DBLB	CNTMD	SHTNAK	—	—	DIR	EPNUM[3:0]			
Value after reset:	0	0	x	x	x	0	0	0	0	x	x	0	0	0	0	0

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b3 to b0	EPNUM[3:0]	Endpoint Number*1	Specifies the endpoint number for the selected pipe. Setting 0000b indicates the pipe is not used.	R/W
b4	DIR	Transfer Direction*2, *3	0: Receiving direction 1: Transmitting direction.	R/W
b6, b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	SHTNAK	Pipe Disabled at End of Transfer*1	0: Continue pipe operation after transfer ends 1: Disable pipe after transfer ends.	R/W
b8	CNTMD	Continuous Transfer Mode*2, *3	0: Discontinuous transfer mode 1: Continuous transfer mode.	R/W
b9	DBLB	Double Buffer Mode*2, *3	0: Single buffer 1: Double buffer.	R/W
b10	BFRE	BRDY Interrupt Operation Specification*2, *3	0: Generate BRDY interrupt on transmitting or receiving data 1: Generate BRDY interrupt on completion of reading data.	R/W
b13 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15, b14	TYPE[1:0]	Transfer Type*1	• Pipes 1 and 2 b15 b14 0 0: Pipe not used 0 1: Bulk transfer 1 0: Setting prohibited 1 1: Isochronous transfer. • Pipes 3 to 5 b15 b14 0 0: Pipe not used 0 1: Bulk transfer 1 0: Setting prohibited 1 1: Setting prohibited. • Pipes 6 to 9 b15 b14 0 0: Pipe not used 0 1: Setting prohibited 1 0: Interrupt transfer 1 1: Setting prohibited.	R/W

Note 1. Only set the TYPE[1:0], SHTNAK, and EPNUM[3:0] bits while PID is NAK. Before setting these bits, check that the PIPEnCTR.CSSTS and PIPEnCTR.PBUSY flags are 0, and then change the PIPEnCTR.PID[1:0] bits from 01b (BUF) to 00b (NAK). If the PIPEnCTR.PID[1:0] bits are changed to 00b (NAK) by the USBHS, checking the CSSTS and PBUSY flags through the software is not necessary.

Note 2. Only set the BFRE, DBLB, and DIR bits while PID is NAK and before the pipe is selected in the CURPIPE[3:0] bits in the port select register. Before setting these bits, check that the PIPEnCTR.CSSTS and PIPEnCTR.PBUSY flags are 0, and then change the PIPEnCTR.PID[1:0] bits from 01b (BUF) to 00b (NAK). If the PIPEnCTR.PID[1:0] bits are changed to 00b (NAK) by the USBHS, checking the PBUSY flag through the software is not necessary.

Note 3. To change the BFRE, DBLB, or DIR bit after completing USB communication on the selected pipe, in addition to the constraints described in note 2, write 1 and 0 to the PIPEnCTR.ACLRM bit continuously through software and clear the FIFO buffer

用于数据写入和读取。在PIPESEL[3:0]位中选择一个管道编号允许写入和读取与所选管道编号相关的PIPECFG、PIPEMAXP和PIPEPERI。

当PIPESEL[3:0]=0000b时，从PIPECFG、PIPEMAXP和PIPEPERI中的所有位读取0。写入这些位无效。

33.2.34 管道配置寄存器(PIPECFG)

Address(es): USBHS.PIPECFG 4006 0068h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TYPE[1:0]		—	—	—	BFRE	DBLB	CNTMD	SHTNAK	—	—	DIR	EPNUM[3:0]			
重置后的值：	0	0	x	x	x	0	0	0	0	x	x	0	0	0	0	0

x: Undefined

Bit	Symbol	位名称		Description	R/W
b3 to b0	EPNUM[3:0]	端点编号	*1	指定选定管道的端点编号。设置0000b表示不使用管道。	R/W
b4	DIR	转移方向	*2, *3	0：接收方向1：发送方向。	R/W
b6, b5	—	Reserved		这些位被读取为0。写入值应为0。	R/W
b7	SHTNAK	管道在结束时禁用Transfer*1		0：传输结束后继续管道操作1：传输结束后禁用管道。	R/W
b8	CNTMD	连续传输模式	*2, *3	0：不连续传输模式1：连续传输模式。	R/W
b9	DBLB	双缓冲模式	*2, *3	0：单缓冲区1：双缓冲区。	R/W
b10	BFRE	BRDY中断操作Specification*2, *3		0：发送或接收数据时产生BRDY中断1：读取数据完成时产生BRDY中断。	R/W
b13 to b11	—	Reserved		这些位被读取为0。写入值应为0。	R/W
b15, b14	TYPE[1:0]	传输类型	*1	管道1和2b15b14 0 0：未使用管道 0 1：批量传输 1 0：禁止设定 1 1: Isochronous transfer. 管道3至5b15b14 0 0：未使用管道 0 1：批量传输 1 0：禁止设定 1 1：禁止设置。 管道6至9b15b14 0 0：未使用管道 0 1：禁止设置 1 0：中断传输 1 1：禁止设置。	R/W

Note 1. 仅在PID为NAK时设置TYPE[1:0]、SHTNAK和EPNUM[3:0]位。在设置这些位之前，请检查PIPEnCTR.CSSTS和PIPEnCTR.PBUSY标志为0，然后将PIPEnCTR.PID[1:0]位从01b(BUF)更改为00b(NAK)。如果PIPEnCTR.PID[1:0]位被USBHS更改为00b(NAK)，则无需通过软件检查CSSTS和PBUSY标志。

Note 2. 仅在PID为NAK且在端口选择寄存器的CURPIPE[3:0]位中选择管道之前设置BFRE、DBLB和DIR位。在设置这些位之前，请检查PIPEnCTR.CSSTS和PIPEnCTR.PBUSY标志是否为0，然后将PIPEnCTR.PID[1:0]位从01b(BUF)更改为00b(NAK)。如果PIPEnCTR.PID[1:0]位被USBHS更改为00b(NAK)，则无需通过软件检查PBUSY标志。

Note 3. 要在选定管道上完成USB通信后更改BFRE、DBLB或DIR位，除了注释2中描述的约束外，通过软件连续向PIPEnCTR.ACLRM位写入1和0，并清除FIFO缓冲区

assigned to the pipe.

EPNUM[3:0] bit (Endpoint Number)

The EPNUM[3:0] bits specify the endpoint number for the selected pipe. Setting 0000b indicates the pipe not used.

Set these bits so that the combination of the DIR and EPNUM[3:0] settings is different from those for other pipes. (The EPNUM[3:0] bits can be set to 0000b for all pipes.)

DIR bit (Transfer Direction)

The DIR bit specifies the transfer direction for the selected pipe.

When the software sets this bit to 0, the USBHS uses the selected pipe for receiving. When the software sets this bit to 1, the USBHS uses the selected pipe for transmitting.

SHTNAK bit (Pipe Disabled at End of Transfer)

The SHTNAK bit specifies whether to change the PIPEnCTR.PID[1:0] bits to 00b (NAK) at the end of transfer when the selected pipe is set in the receiving direction. The bit is valid for pipes 1 to 5 in the receiving direction.

When the software sets this bit to 1 for a receiving pipe, the USBHS changes the associated PIPEnCTR.PID[1:0] bits to 00b (NAK) on determining the transfer end. The USBHS determines that the transfer has ended on the following conditions:

- Short packet data (including a zero-length packet) was successfully received
- The transaction counter is used and the number of packets specified for the transaction counter were successfully received.

CNTMD bit (Continuous Transfer Mode)

The CNTMD bit specifies whether to operate the selected pipe in continuous transfer mode. The bit is valid for pipes 1 to 5 of the bulk transfer type.

Based on this bit setting, the USBHS determines the completion of transmission or reception for the FIFO buffer allocated to the selected pipe as shown in Table 33.9.

Table 33.9 Relationship between the CNTMD setting and methods for determining completion of FIFO buffer transmission or reception

CNTMD bit setting	Methods for determining readable state and transmittable state
0	Condition for FIFO buffer readable state in receiving direction (DIR = 0): • The USBHS received one packet.
	Conditions for FIFO buffer transmittable state in transmitting direction (DIR = 1): When one of (1) or (2) of the following is satisfied: (1) Software (or DMAC/DTC) wrote data of the maximum packet size to the FIFO buffer. (2) Software (or DMAC/DTC) wrote data of the short packet size (including 0 bytes) to the FIFO buffer and set the BVAL flag in the port control register to 1.
1	Condition for FIFO buffer readable state in receiving direction (DIR = 0): (1) The byte count of data received in the FIFO buffer allocated to the selected pipe is equal to the allocated byte count ((BUFSIZE + 1) × 64). (2) The USBHS received a short packet, other than a zero-length packet. (3) The USBHS received a zero-length packet when data was already contained in the FIFO buffer allocated to the selected pipe. (4) Software received the number of packets specified for the transaction counter set for the selected pipe.
	Conditions for FIFO buffer transmittable state in transmitting direction (DIR = 1): When one of (1) to (3) of the following is satisfied. (1) The amount of data written by software (or DMAC/DTC) is equal to the size of the FIFO buffer allocated to the selected pipe. (2) The software (or DMAC/DTC) wrote data of smaller size than that of the FIFO buffer allocated to the selected pipe (including 0 bytes) and set the BVAL flag in the port control register to 1. (3) The software (or DMAC/DTC) wrote data of smaller size than that of one FIFO buffer allocated to the selected pipe (including 0 bytes) and asserted the DENDx_N signal on the last write.

分配给管道。

EPNUM[3:0]位（端点编号）

EPNUM[3:0]位指定所选管道的端点号。设置0000b表示管道未使用。

设置这些位，以便DIR和EPNUM[3:0]设置的组合不同于其他管道的设置。（这所有管道的EPNUM[3:0]位都可以设置为0000b。）

DIR位（传输方向）

DIR位指定所选管道的传输方向。

当软件将此位设置为0时，USBHS使用所选管道进行接收。当软件将该位设置为1时，USBHS使用选定的管道进行传输。

SHTNAK位（传输结束时管道禁用）

SHTNAK位指定当所选管道设置为接收方向时，是否在传输结束时将PIPEnCTR.PID[1:0]位更改为00b(NAK)。该位对接收方向的管道1到5有效。

当软件将该位设置为1用于接收管道时，USBHS在确定传输结束时将相关的PIPEnCTR.PID[1:0]位更改为00b(NAK)。USBHS在以下条件下确定传输已结束：

- 成功接收短包数据（包括零长度包）
- 使用事务计数器，并且成功接收到为事务计数器指定的数据包数。

CNTMD位（连续传输模式）

CNTMD位指定是否在连续传输模式下操作选定的管道。该位对批量传输类型的管道1到5有效。

根据该位设置，USBHS确定分配给所选管道的FIFO缓冲区的发送或接收是否完成，如表33.9所示。

Table 33.9 CNTMD设置与确定FIFO缓冲区发送或接收完成的方法之间的关系

CNTMD位设置	确定可读状态和可传输状态的方法
0	接收方向上FIFO缓冲区可读状态的条件（DIR=0）： USBHS接收到一个数据包。
	发送方向(DIR=1)的FIFO缓冲区可发送状态的条件： 当满足以下(1)或(2)之一时：(1)软件（或DMACDTC）将最大数据包大小的数据写入FIFO缓冲区。(2)软件（或DMACDTC）将短包大小（包括0字节）的数据写入FIFO缓冲区，并将端口控制寄存器中的BVAL标志设置为1。
1	接收方向（DIR=0）FIFO缓冲区可读状态的条件：（1）分配给所选管道的FIFO缓冲区中接收到的数据的字节数等于分配的字节数（（BUFSIZE+1）×64）。(2)USBHS接收到一个短数据包，而不是一个零长度数据包。(3)当数据已包含在分配给所选管道的FIFO缓冲区中时，USBHS接收到一个零长度数据包。(4)软件接收到为所选管道设置的事务计数器指定的数据包数量。
	发送方向(DIR=1)的FIFO缓冲区可发送状态的条件： 当满足以下（1）至（3）之一时。(1)软件（或DMACDTC）写入的数据量等于分配给所选管道的FIFO缓冲区的大小。(2)软件（或DMACDTC）写入比分配给所选管道的FIFO缓冲区更小的数据（包括0字节），并将端口控制寄存器中的BVAL标志设置为1。(3)软件（或DMACDTC）写入的数据小于分配给所选管道的一个FIFO缓冲区（包括0字节），并在最后一次写入时置位DENDx_N信号。

DBLB bit (Double Buffer Mode)

The DBLB bit selects either single or double buffer mode for the FIFO buffer used by the selected pipe. The bit is valid for pipes 1 to 5.

When the software sets this bit to 1, the USBHS allocates twice the FIFO buffer size specified in the PIPEBUF.BUFSIZE[5:0] bits for the selected pipe. The FIFO buffer size that the USBHS allocates to the selected pipe is as follows:

(BUFSIZE + 1) × 64 × (DBLB + 1) [bytes]

BFRE bit (BRDY Interrupt Operation Specification)

The BFRE bit specifies the BRDY interrupt generation timing from the USBHS to the CPU for the selected pipe.

When the software sets the BFRE bit to 1 and the selected pipe is in the receiving direction, the USBHS detects the transfer completion and generates the BRDY interrupt on reading the packet.

When a BRDY interrupt is generated with this setting, the software must write 1 to the BCLR bit in the port control register. The FIFO buffer assigned to the selected pipe is not enabled for reception until 1 is written to the BCLR bit.

When the BFRE bit is set to 1 by software and the selected pipe is in the transmitting direction, the USBHS does not generate the BRDY interrupt. For details, see section 33.3.6.1, BRDY interrupt.

TYPE[1:0] bits (Transfer Type)

The TYPE[1:0] bits specify the transfer type for the pipe selected in the PIPESEL.PIPESEL[3:0] bits. Before setting PID to BUF and starting USB communication on the selected pipe, set the TYPE[1:0] bits to a value other than 00b.

33.2.35 Pipe Buffer Register (PIPEBUF)

Address(es): USBHS.PIPEBUF 4006 006Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	BUFSIZE[4:0]					—	—	BUFNMB[7:0]							
Value after reset:	x	0	0	0	0	0	x	x	0	0	0	0	0	0	0	0

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b7 to b0	BUFNMB[7:0]	Buffer Number	Specifies the FIFO buffer number of the selected pipe (04h to 87h).	R/W
b9, b8	—	Reserved	The read value is undefined. The write value should be 0.	R/W
b14 to b10	BUFSIZE[4:0]	Buffer Size	00h: 64 bytes 01h: 128 bytes ... 1Fh: 2 KB.	R/W
b15	—	Reserved	The read value is undefined. The write value should be 0.	R/W

Note 1. Only set the bits in the PIPEBUF register while PID is NAK and before the pipe is selected in the CURPIPE[3:0] bits in the port select register. Before setting these bits, check that the PIPEnCTR.CSSTS and PIPEnCTR.PBUSY flags are 0, and then change the PIPEnCTR.PID[1:0] bits from 01b (BUF) to 00b (NAK). If the PIPEnCTR.PID[1:0] bits are changed to 00b (NAK) by the USBHS, checking the CSSTS and PBUSY flags through the software is not necessary.

BUFNMB[7:0] bits (Buffer Number)

The BUFNMB[7:0] bits specify the first block number of the FIFO buffer to be allocated to the selected pipe.

The USBHS allocates the FIFO buffer blocks to the selected pipe as follows:

Block number: BUFNMB to block number: BUFNMB + (BUFSIZE + 1) × (DBLB + 1) - 1

Set a value within the memory size range for these bits (0 [00h] to 8640 [87h] for 8.5 KB), while observing the following conditions:

DBLB位（双缓冲模式）

DBLB位为所选管道使用的FIFO缓冲区选择单缓冲区模式或双缓冲区模式。该位对管道1到5有效。

当软件将该位设置为1时，USBHS分配两倍于
所选管道的PIPEBUF.BUFSIZE[5:0]位。USBHS分配给所选管道的FIFO缓冲区大小如下：

(BUFSIZE + 1) × 64 × (DBLB + 1) [bytes]

BFRE位（BRDY中断操作规范）

BFRE位为所选管道指定从USBHS到CPU的BRDY中断生成时序。

当软件将BFRE位设置为1且所选管道处于接收方向时，USBHS检测到传输完成并在读取数据包时产生BRDY中断。

当使用该设置产生BRDY中断时，软件必须将1写入端口控制寄存器中的BCLR位。在将1写入BCLR位之前，分配给所选管道的FIFO缓冲区不会用于接收。

当BFRE位由软件设置为1且所选管道处于发送方向时，USBHS不会产生BRDY中断。有关详细信息，请参阅第33.3.6.1节，BRDY中断。

TYPE[1:0]位（传输类型）

TYPE[1:0]位指定在PIPESEL.PIPESEL[3:0]位中选择的管道的传输类型。在将PID设置为BUF并在所选管道上启动USB通信之前，请将TYPE[1:0]位设置为00b以外的值。

33.2.35 管道缓冲寄存器(PIPEBUF)

Address(es): USBHS.PIPEBUF 4006 006Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	BUFSIZE[4:0]					—	—	BUFNMB[7:0]							
重置后的值：	x	0	0	0	0	0	x	x	0	0	0	0	0	0	0	0

x: Undefined

Bit	Symbol	位名称	Description	R/W
b7 to b0	BUFNMB[7:0]	缓冲区号	指定所选管道的FIFO缓冲区编号（04h到87h）。	R/W
b9, b8	—	Reserved	读取值未定义。写入值应为0。	R/W
b14 to b10	BUFSIZE[4:0]	缓冲区大小	00h: 64 bytes 01h: 128 bytes ... 1Fh: 2 KB.	R/W
b15	—	Reserved	读取值未定义。写入值应为0。	R/W

Note 1. 仅在PID为NAK时以及在端口选择寄存器的CURPIPE[3:0]位中选择管道之前设置PIPEBUF寄存器中的位。在设置这些位之前，请检查PIPEnCTR.CSSTS和PIPEnCTR.PBUSY标志是否为0，然后将PIPEnCTR.PID[1:0]位从01b(BUF)更改为00b(NAK)。如果PIPEnCTR.PID[1:0]位被USBHS更改为00b(NAK)，则无需通过软件检查CSSTS和PBUSY标志。

BUFNMB[7:0]位（缓冲区编号）

BUFNMB[7:0]位指定要分配给所选管道的FIFO缓冲区的第一个块号。

USBHS将FIFO缓冲区块分配给所选管道，如下所示：

块号：BUFNMB到块号：BUFNMB+(BUFSIZE+1)×(DBLB+1)1

为这些位设置一个内存大小范围内的值（0[00h]到8640[87h]，对于8.5KB），同时遵守以下条件：

- 00h is for DCP only
- 04h is for pipe 6 only, but is available for other pipes when pipe 6 is not used. When pipe 6 is selected, writes to these bits are disabled. The USBHS automatically allocates 04h to the BUFNMB bits for pipe 6.
- 05h is for pipe 7 only, but is available for other pipes when pipe 7 is not used. When pipe 7 is selected, writes to these bits are disabled. The USBHS automatically allocates 05h to the BUFNMB bits for pipe 7.
- 06h is for pipe 8 only, but is available for other pipes when pipe 8 is not used. When pipe 8 is selected, writes to these bits are disabled. The USBHS automatically allocates 06h to the BUFNMB bits for pipe 8.
- 07h is for pipe 9 only, but is available for other pipes when pipe 9 is not used. When pipe 9 is selected, writes to these bits are disabled. The USBHS automatically allocates 07h to the BUFNMB bits for pipe 9.

BUFSIZE[4:0] bits (Buffer Size)

The BUFSIZE[4:0] bits specify the FIFO buffer size (number of blocks) to be allocated to the selected pipe. One block is 64 bytes.

When the software sets the DBLB bit to 1, the USBHS allocates twice the FIFO buffer size specified in these bits to the selected pipe. The DBLB = 1 setting is valid for pipes 1 to 5.

The USBHS allocates the FIFO buffer blocks to the selected pipe as follows:

(BUFSIZE + 1) × 64 × (DBLB + 1) [bytes]

Set the value within the following range:

- For pipes 1 to 5, set a value from 00h to 1Fh (up to 2 KB)
- For pipes 6 to 9, only set a value of 00h (64 bytes).

33.2.36 Pipe Maximum Packet Size Register (PIPEMAXP)

Address(es): USBHS.PIPEMAXP 4006 006Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	DEVSEL[3:0]				—	MXPS[10:0]										
Value after reset:	0	0	0	0	x	0	0	0	0	0	0	0	0	0	0	0

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b10 to b0	MXPS[10:0] *1, *2	Maximum Packet Size	• Pipes 1 and 2 1 byte (001h) to 1024 bytes (400h) • Pipes 3 to 5 8 bytes (008h), 16 bytes (010h), 32 bytes (020h), 64 bytes (040h), 512 bytes (200h) (Bits 2 to 0 not supported.) • Pipes 6 to 9 1 byte (001h) to 64 bytes (040h) (Bits 10 to 7 not supported.)	R/W
b11	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b15 to b12	DEVSEL[3:0] *3	Device Select	b15 b12 0 0 0 0: Address 0000b 0 0 0 1: Address 0001b ... 1 0 0 1: Address 1001b 1 0 1 0: Address 1010b 1011 to 1111: Reserved.	R/W

Note 1. The initial value of the MXPS[10:0] bits is 00h when no pipe is selected in the PIPESEL.PIPESEL[3:0] bits and 40h when a pipe is selected.

Note 2. Only set the MXPS[10:0] bits while PID is NAK and before the pipe is selected in the CURPIPE[3:0] bits in the port select register. Before setting these bits, check that the PIPEnCTR.CSSTS and PIPEnCTR.PBUSY flags are 0, and then change the

- 00h仅适用于DCP
- 04h仅适用于管道6，但在不使用管道6时可用于其他管道。选择管道6时，将这些位写入这些位。USBHS自动将04h分配给管道6的BUFNMB位。
- 05h仅适用于管道7，但在不使用管道7时可用于其他管道。选择管道7时，将这些位写入这些位。USBHS自动将05h分配给管道7的BUFNMB位。
- 06h仅适用于管道8，但在不使用管道8时可用于其他管道。选择管道8时，将这些位写入这些位。USBHS自动将06h分配给管道8的BUFNMB位。
- 07h仅适用于管道9，但在不使用管道9时可用于其他管道。选择管道9时，将这些位写入这些位。USBHS自动将07h分配给管道9的BUFNMB位。

BUFSIZE[4:0]位（缓冲区大小）

BUFSIZE[4:0]位指定要分配给所选管道的FIFO缓冲区大小（块数）。一个块是64字节。

当软件将DBLB位设置为1时，USBHS将这些位中指定的两倍FIFO缓冲区大小分配给所选管道。DBLB=1设置对管道1到5有效。

USBHS将FIFO缓冲区块分配给所选管道，如下所示：

(BUFSIZE + 1) × 64 × (DBLB + 1) [bytes]

将值设置在以下范围内：

- 对于管道1到5，设置一个从00h到1Fh的值（最大2KB）
- 对于管道6到9，仅设置值00h（64字节）。

33.2.36 管道最大数据包大小寄存器(PIPEMAXP)

Address(es): USBHS.PIPEMAXP 4006 006Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	DEVSEL[3:0]				—	MXPS[10:0]										
重置后的值：	0	0	0	0	x	0	0	0	0	0	0	0	0	0	0	0

x: Undefined

Bit	Symbol	位名称	Description	R/W
b10 to b0	MXPS[10:0] *1, *2	最大数据包大小	管道1和2 1字节(001h)到1024字节(400h) 管道3到5 8字节(008h)、16字节(010h)、32字节(020h)、64字节(040h)、512字节(200h)（不支持位2到0。） 管道6到9 1字节(001h)至64字节(040h)（不支持位10至7。）	R/W
b11	—	Reserved	该位读取为0。写入值应为0。	R/W
b15 to b12	DEVSEL[3:0] *3	设备选择	b15 b12 0 0 0 0: Address 0000b 0 0 0 1: Address 0001b ... 1 0 0 1: Address 1001b 10：地址1010b1011到111 1：保留。	R/W

Note 1. TheinitialvalueoftheMXPS[10:0]bitsis00hwhennopipeisselectedinthePIPESEL.PIPESEL[3:0]bitsand40hwhenapipeisselected.

Note 2. 仅在PID为NAK且在端口选择寄存器的CURPIPE[3:0]位中选择管道之前设置MXPS[10:0]位。在设置这些位之前，检查PIPEnCTR.CSSTS和PIPEnCTR.PBUSY标志是否为0，然后更改

PIPEnCTR.PID[1:0] bits from 01b (BUF) to 00b (NAK). If the PIPEnCTR.PID[1:0] bits are changed to 00b (NAK) by the USBHS, checking the CSSTS and PBUSY flags through the software is not necessary.

Note 3. Only set the DEVSEL[3:0] bits while PID is NAK and before the pipe is selected in the CURPIPE[3:0] bits in the port select register. Before setting these bits, check that the PIPEnCTR.CSSTS and PIPEnCTR.PBUSY flags are 0, and then change the PIPEnCTR.PID[1:0] bits from 01b (BUF) to 00b (NAK). If the PIPEnCTR.PID[1:0] bits are changed to 00b (NAK) by the USBHS, checking the PBUSY flag through the software is not necessary.

MXPS[10:0] bits (Maximum Packet Size)

The MXPS[10:0] bits specify the maximum data payload (maximum packet size) for the selected pipe.

Set these bits to the appropriate value for each transfer type based on the USB 2.0 specification. When MXPS[10:0] = 0, do not write to the FIFO buffer or set PID to BUF. These writes have no effect.

To communicate on an isochronous pipe using a split transaction, set the value in the MXPS[10:0] bits to 188 bytes or less.

DEVSEL[3:0] bits (Device Select)

In host controller mode, the DEVSEL[3:0] bits specify the address of the target device for USB communication. Set up the device address in the associated DEVADDm (m = 0 to A) register first, and then set these bits to the corresponding value. To set the DEVSEL[3:0] bits to 0010b, for example, first set the address in the DEVADD2 register.

In device controller mode, set these bits to 0000b.

33.2.37 Pipe Cycle Control Register (PIPEPERI)

Address(es): USBHS.PIPEPERI 4006 006Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	IFIS	—	—	—	—	—	—	—	—	—	IITV[2:0]		
Value after reset:	x	x	x	0	x	x	x	x	x	x	x	x	x	0	0	0

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b2 to b0	IITV[2:0]	Interval Error Detection Interval	Specifies the interval error detection timing for the selected pipe as the n-th power of 2 of the frame timing.	R/W
b11 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b12	IFIS	Isochronous IN Buffer Flush	0: Do not flush buffer 1: Flush buffer.	R/W
b15 to b13	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Only set the IITV[2:0] bits while PID is NAK. Before setting these bits, check that the PIPEnCTR.CSSTS and PIPEnCTR.PBUSY flags are 0, and then change the PIPEnCTR.PID[1:0] bits from 01b (BUF) to 00b (NAK). If the PIPEnCTR.PID[1:0] bits are changed to 00b (NAK) by the USBHS, checking the PBUSY flag through the software is not necessary.

PIPEPERI selects whether the buffer is flushed or not when an interval error occurred during isochronous IN transfers, and sets the interval error detection interval for pipes 1 to 9.

IITV[2:0] bits (Interval Error Detection Interval)

To change the IITV[2:0] bits to another value after they are set and USB communication is performed, set the PIPEnCTR.PID[1:0] bits to 00b (NAK) and then set the PIPEnCTR.ACLRM bit to 1 to initialize the interval timer.

The IITV[2:0] bits are not provided for pipes 3 to 5. Write 000b to bit positions of the IITV[2:0] bits associated with pipes 3 to 5.

IFIS bit (Isochronous IN Buffer Flush)

The IFIS bit specifies whether to flush the buffer when the pipe specified in the PIPESEL.PIPESEL[3:0] bits is used for isochronous IN transfers.

PIPEnCTR.PID[1:0]位从01b(BUF)到00b(NAK)。如果PIPEnCTR.PID[1:0]位被更改为00b(NAK)
USBHS，不需要通过软件检查CSSTS和PBUSY标志。

Note 3. 仅在PID为NAK且在端口选择寄存器的CURPIPE[3:0]位中选择管道之前设置DEVSEL[3:0]位。在设置这些位之前，请检查PIPEnCTR.CSSTS和PIPEnCTR.PBUSY标志是否为0，然后将PIPEnCTR.PID[1:0]位从01b(BUF)更改为00b(NAK)。如果PIPEnCTR.PID[1:0]位被更改为00b(NAK)
USBHS，不需要通过软件检查PBUSY标志。

MXPS[10:0]位（最大数据包大小）

MXPS[10:0]位指定所选管道的最大数据有效负载（最大数据包大小）。

根据USB2.0规范将这些位设置为每种传输类型的适当值。当MXPS[10:0]=0时，不要写入FIFO缓冲区或将PID设置为BUF。这些写入没有效果。

要使用拆分事务在同步管道上进行通信，请将MXPS[10:0]位中的值设置为188字节或更少。

DEVSEL[3:0]位（设备选择）

在主机控制器模式下，DEVSEL[3:0]位指定USB通信的目标设备的地址。首先在相关的DEVADDm（m=0到A）寄存器中设置设备地址，然后将这些位设置为相应的值。例如，要将DEVSEL[3:0]位设置为0010b，首先要设置DEVADD2寄存器中的地址。

在设备控制器模式下，将这些位设置为0000b。

33.2.37 管道周期控制寄存器(PIPEPERI)

Address(es): USBHS.PIPEPERI 4006 006Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	IFIS	—	—	—	—	—	—	—	—	—	IITV[2:0]		
重置后的值：	x	x	x	0	x	x	x	x	x	x	x	x	x	0	0	0

x: Undefined

Bit	Symbol	位名称	Description	R/W
b2 to b0	IITV[2:0]	间隔错误检测间隔	将所选管道的间隔错误检测时间指定为帧时间的2的n次方。	R/W
b11 to b3	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b12	IFIS	同步IN缓冲区刷新	0：不刷新缓冲区1： 刷新缓冲区。	R/W
b15 to b13	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 仅在PID为NAK时设置IITV[2:0]位。在设置这些位之前，请检查PIPEnCTR.CSSTS和PIPEnCTR.PBUSY标志为0，然后将PIPEnCTR.PID[1:0]位从01b(BUF)更改为00b(NAK)。如果PIPEnCTR.PID[1:0]位由USBHS更改为00b(NAK)，无需通过软件检查PBUSY标志。

PIPEPERI选择在同步IN传输期间发生间隔错误时是否刷新缓冲区，并设置管道1到9的间隔错误检测间隔。

IITV[2:0]位（间隔错误检测间隔）

要在设置IITV[2:0]位并在执行USB通信后将其更改为另一个值，请设置PIPEnCTR.PID[1:0]位为00b(NAK)，然后将PIPEnCTR.ACLRM位设置为1以初始化间隔定时器。

不为管道3到5提供IITV[2:0]位。将000b写入与管道3到5相关联的IITV[2:0]位的位位置。

IFIS位（同步IN缓冲区刷新）

IFIS位指定当PIPESEL.PIPESEL[3:0]位中指定的管道用于同步IN传输时是否刷新缓冲区。

In device controller mode when the selected pipe is for isochronous IN transfers, the USBHS automatically clears the FIFO buffer if the USBHS fails to receive the IN token from the USB host within the interval set in the IITV[2:0] bits in terms of frames.

When double buffering is specified (PIPECFG.DBLB = 1), the USBHS only clears the data in the previously used plane.

The USBHS clears the FIFO buffer on receiving the SOF packet immediately after the frame in which the USBHS expected to receive the IN token. Even if the SOF packet is corrupted, the FIFO buffer is cleared at the time the SOF packet is expected to be received by using the internal complementation function.

In host controller mode, set the IITV[2:0] bits to 000b.

Set the IITV[2:0] bits to 000b when the selected pipe is not used for isochronous transfers.

33.2.38 Pipe n Control Register (PIPEnCTR) (n = 1 to 9)

Address(es): USBHS.PIPE1CTR 4006 0070h, USBHS.PIPE2CTR 4006 0072h, USBHS.PIPE3CTR 4006 0074h, USBHS.PIPE4CTR 4006 0076h, USBHS.PIPE5CTR 4006 0078h, USBHS.PIPE6CTR 4006 007Ah, USBHS.PIPE7CTR 4006 007Ch, USBHS.PIPE8CTR 4006 007Eh, USBHS.PIPE9CTR 4006 0080h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BSTS	INBUFM	CSCLR	CSSTS	—	ATREPM	ACLRM	SQCLR	SQSET	SQMON	PBUSY	—	—	—	PID[1:0]	
Value after reset:	0	0	0	0	x	0	0	0	0	0	0	x	x	x	0	0

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b1, b0	PID[1:0]	Response PID	b1 b0 0 0: NAK response 0 1: BUF response (depends on buffer state) 1 0: STALL response 1 1: STALL response.	R/W
b4 to b2	—	Reserved	The read value is undefined. The write value should be 0.	R/W
b5	PBUSY	Pipe Busy Flag	0: Pipe n not in use for the transaction 1: Pipe n in use for the transaction.	R
b6	SQMON	Sequence Toggle Bit Monitor Flag	0: DATA0 1: DATA1.	R
b7	SQSET	Sequence Toggle Bit Set*1	Sets the sequence toggle bit for pipe n. 0: Invalid (writing 0 has no effect) 1: Set the expected value for the next transaction to DATA1. This bit is read as 0.	R/W
b8	SQCLR	Sequence Toggle Bit Clear*1	Clears the sequence toggle bit for pipe n. 0: Invalid (writing 0 has no effect) 1: Clear the expected value for the next transaction to DATA0. This bit is read as 0.	R/W
b9	ACLRM	Auto Buffer Clear Mode*2	0: Disable 1: Enable (initialize all buffers).	R/W
b10	ATREPM	Auto Response Mode*1, *3	0: Disable auto response mode 1: Enable auto response mode.	R/W
b11	—	Reserved	The read value is undefined. The write value should be 0.	R/W
b12	CSSTS	CSSTS Status Flag	0: Start-split (SSPLIT) transaction, or processing for devices that are not using split transactions, in progress. 1: Complete-split (CSPLIT) transaction in progress.	R
b13	CSCLR	CSPLIT Status Clear	Clears the CSSTS flag for pipe n. 0: Invalid (writing 0 has no effect) 1: Clear CSSTS to 0.	W
b14	INBUFM	Transmit Buffer Monitor Flag*3	0: No data to be transmitted is in the FIFO buffer 1: Data to be transmitted is in the FIFO buffer.	R
b15	BSTS	Buffer Status Flag	0: Buffer access disabled 1: Buffer access enabled.	R

在设备控制器模式下，当所选管道用于同步IN传输时，USBHS会自动清除
如果USBHS未能在IITV[2:0]位（以帧为单位）设置的间隔内接收来自USB主机的IN令牌，则FIFO缓冲区。

当指定双缓冲时（PIPECFG.DBLB=1），USBHS仅清除先前使用的平面中的数据。

在USBHS预期接收IN令牌的帧之后，USBHS在接收到SOF数据包后立即清除FIFO缓冲区。即使SOF数据包已损坏，FIFO缓冲区也会在预期接收SOF数据包时使用内部补充功能清除。

在主机控制器模式下，将IITV[2:0]位设置为000b。

当所选管道不用于同步传输时，将IITV[2:0]位设置为000b。

33.2.38 管道n控制寄存器(PIPEnCTR)(n=1到9)

Address(es): USBHS.PIPE1CTR 4006 0070h, USBHS.PIPE2CTR 4006 0072h, USBHS.PIPE3CTR 4006 0074h, USBHS.PIPE4CTR 4006 0076h, USBHS.PIPE5CTR 4006 0078h, USBHS.PIPE6CTR 4006 007Ah, USBHS.PIPE7CTR 4006 007Ch, USBHS.PIPE8CTR 4006 007Eh, USBHS.PIPE9CTR 4006 0080h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BSTS	INBUFM	CSCLR	CSSTS	—	ATREPM	ACLRM	SQCLR	SQSET	SQMON	PBUSY	—	—	—	PID[1:0]	
重置后的值:	0	0	0	0	x	0	0	0	0	0	0	x	x	x	0	0

x: Undefined

Bit	Symbol	位名称	Description	R/W
b1, b0	PID[1:0]	响应PID	b1 b0 0 0：NAK响应 0 1：BUF响应（取决于缓冲区状态） 1 0：停止响应 1 1：停止响应。	R/W
b4 to b2	—	Reserved	读取值未定义。写入值应为0。	R/W
b5	PBUSY	管道忙标志	0：管道n未用于事务1：管道n正在用于事务。	R
b6	SQMON	序列切换位监视器 Flag	0: DATA0 1: DATA1.	R
b7	SQSET	序列切换位设置 *1	设置管道n的序列切换位。0：无效（写0无效）1：将下一笔交易的期望值设置为DATA1。该位读为0。	R/W
b8	SQCLR	序列切换位清除 *1	清除管道n的序列切换位。0：无效（写0无效）1：清除下一笔交易的期望值到DATA0。该位读为0。	R/W
b9	ACLRM	自动缓冲区清除模式 *2	0：禁用1：启用（初始化所有缓冲区）。	R/W
b10	ATREPM	自动响应模式 *1, *3	0：禁用自动响应模式1：启用自动响应模式。	R/W
b11	—	Reserved	读取值未定义。写入值应为0。	R/W
b12	CSSTS	CSSTS状态标志	0：开始拆分(SSPLIT)事务，或正在处理未使用拆分事务的设备。1：完成拆分（CSPLIT）事务正在进行中。	R
b13	CSCLR	CSPLIT状态清除	清除管道n的CSSTS标志。0：无效（写0无效）1：清除CSSTS为0。	W
b14	INBUFM	发送缓冲区监控标志 *3	0：FIFO缓冲区中没有要发送的数据1：FIFO缓冲区中没有要发送的数据。	R
b15	BSTS	缓冲区状态标志	0：禁止缓冲区访问1：允许缓冲区访问。	R

Note 1. Only set the ATREPM bit while PID is NAK. Before setting this bit, check that the PIPEnCTR.CSSTS and PIPEnCTR.PBUSY flags are 0, and then change the PIPEnCTR.PID[1:0] bits from 01b (BUF) to 00b (NAK). If the PIPEnCTR.PID[1:0] bits are changed to 00b (NAK) by the USBHS, checking the PBUSY flag through the software is not necessary.
Note 2. Only set the ACLRM bit while PID is NAK and before the pipe is selected in the CURPIPE[3:0] bits in the port select register. Before setting this bit, check that the PIPEnCTR.CSSTS and PIPEnCTR.PBUSY flags are 0, and then change the PIPEnCTR.PID[1:0] bits from 01b (BUF) to 00b (NAK). If the PIPEnCTR.PID[1:0] bits are changed to 00b (NAK) by the USBHS, checking the PBUSY flag through the software is not necessary.
Note 3. The ATREPM bit and the INBUFM flag in the PIPE6CTR to PIPE9CTR registers are reserved. The read value is undefined. The write value must be 0.

PID[1:0] bits (Response PID)

The PID[1:0] bits specify the response type for the next transaction on the selected pipe.

The default PID[1:0] setting is NAK. Change the PID[1:0] setting to BUF to use the associated pipe for USB transfer. Table 33.10 and Table 33.11 show the basic operations of the USBHS (when there are no errors in the communication packets) based on the PID[1:0] bit setting.

After changing the PID[1:0] setting from BUF to NAK through the software during USB communication on the selected pipe, check that the PBUSY bit is 1 to see if USB transfer on the selected pipe has actually entered the NAK state. If the USBHS changes the PID[1:0] bits to NAK, checking the PBUSY bit through the software is not necessary.

The USBHS changes the PIPEnCTR.PID[1:0] setting in the following cases:

- The USBHS sets PID to NAK on recognizing completion of the transfer when the selected pipe is in the receiving direction and the PIPECFG.SHTNAK bit for the selected pipe is set to 1 by software
- The USBHS sets PID to STALL (11b) on receiving a data packet with a payload exceeding the maximum packet size of the selected pipe
- The USBHS sets PID to NAK on detecting a USB bus reset in device controller mode
- The USBHS sets PID to NAK on detecting a reception error, such as a CRC error, three consecutive times in host controller mode
- The USBHS sets PID to STALL (11b) on receiving the STALL handshake in host controller mode.

To specify the response type, set the PID[1:0] bits as follows:

- To transition from NAK (00b) to STALL, set 10b
- To transition from BUF (01b) to STALL, set 11b
- To transition from STALL (11b) to NAK, set 10b and then 00b
- To transition from STALL to BUF, set 00b (NAK) and then 01b (BUF).

Table 33.10 Operation of the USBHS based on the PIPEnCTR.PID[1:0] setting in host controller mode

PID[1:0] value	Transfer type (TYPE[1:0] value)	Transfer direction (DIR value)	USBHS operation
00b (NAK)	Does not depend on the setting	Does not depend on the setting	Does not issue tokens
01b (BUF)	Bulk or Interrupt	Does not depend on the setting	Issues tokens when the DVSTCTR0.UACT bit is 1 and the FIFO buffer associated with the selected pipe is ready for transmission and reception. Does not issue tokens when the DVSTCTR0.UACT bit is 0 or the FIFO buffer associated with the selected pipe is not ready for transmission or reception.
	Isochronous	Does not depend on the setting.	Issues tokens when the DVSTCTR0.UACT bit is 1, regardless of the state of the FIFO buffer associated with the selected pipe. Does not issue tokens when UACT = 0.
10b (STALL) or 11b (STALL)	Does not depend on the setting.	Does not depend on the setting.	Does not issue tokens.

Note 1. 仅在PID为NAK时设置ATREPM位。在设置该位之前，检查PIPEnCTR.CSSTS和PIPEnCTR.PBUSY标志是否为0，然后将PIPEnCTR.PID[1:0]位从01b(BUF)更改为00b(NAK)。如果PIPEnCTR.PID[1:0]位被USBHS更改为00b(NAK)，则无需通过软件检查PBUSY标志。

Note 2. 仅在PID为NAK时以及在端口选择寄存器的CURPIPE[3:0]位中选择管道之前设置ACLRM位。
在设置该位之前，检查PIPEnCTR.CSSTS和PIPEnCTR.PBUSY标志是否为0，然后更改PIPEnCTR.PID[1:0]位从01b(BUF)到00b(NAK)。如果PIPEnCTR.PID[1:0]位被更改为00b(NAK)USBHS，不需要通过软件检查PBUSY标志。
Note 3. PIPE6CTR到PIPE9CTR寄存器中的ATREPM位和INBUFM标志被保留。读取值未定义。
写入值必须为0。

PID[1:0]位（响应PID）

PID[1:0]位指定所选管道上下一个事务的响应类型。

默认PID[1:0]设置为NAK。将PID[1:0]设置更改为BUF以使用关联的管道进行USB传输。表33.10和表33.11显示了基于PID[1:0]位设置的USBHS的基本操作（通信数据包中没有错误时）。

在选定管道上进行USB通信期间，通过软件将PID[1:0]设置从BUF更改为NAK后，检查PBUSY位是否为1，以查看选定管道上的USB传输是否真正进入了NAK状态。如果USBHS将PID[1:0]位更改为NAK，则无需通过软件检查PBUSY位。

USBHS在以下情况下更改PIPEnCTR.PID[1:0]设置：

- 当所选管道处于接收方向并且所选管道的PIPECFG.SHTNAK位由软件设置为1时，USBHS在识别到传输完成时将PID设置为NAK
- USBHS将PID设置为STALL(11b)在接收到有效载荷超过所选管道的最大数据包大小的数据包时
- USBHS在设备控制器模式下检测到USB总线复位时将PID设置为NAK
- USBHS在主机控制器模式下连续3次检测到接收错误（例如CRC错误）时将PID设置为NAK
- USBHS在主机控制器模式下接收到STALL握手时将PID设置为STALL(11b)。

要指定响应类型，请按如下方式设置PID[1:0]位：

- 要从NAK(00b)转换到STALL，请设置10b
- 要从BUF(01b)转换到STALL，请设置11b
- 要从STALL(11b)转换到NAK，请设置10b，然后设置00b
- 要从STALL转换到BUF，请设置00b(NAK)，然后设置01b(BUF)。

Table 33.10 USBHS在主机控制器模式下基于PIPEnCTR.PID[1:0]设置的操作

PID[1:0] value	传输类型（TYPE[1:0]值）	传输方向（DIR值）	USBHS operation
00b (NAK)	不依赖于设置	不依赖于设置	不发行代币
01b (BUF)	批量或中断	不依赖于设置	当DVSTCTR0.UACT位为1并且与所选管道关联的FIFO缓冲区已准备好进行发送和接收时，发出令牌。当DVSTCTR0.UACT位为0或与所选管道关联的FIFO缓冲区未准备好进行发送或接收时，不发出令牌。
	Isochronous	不依赖于设置。	当DVSTCTR0.UACT位为1时发出令牌，无论与所选管道关联的FIFO缓冲区的状态如何。当UACT=0时不发行令牌。
10b (STALL) or 11b (STALL)	不依赖于设置。	不依赖于设置。	不发行代币。

Table 33.11 Operation of the USBHS based on the PIPEnCTR.PID[1:0] setting in device controller mode

PID[1:0] value	Transfer type (TYPE[1:0] value)	Transfer direction (DIR value)	USBHS operation
00b (NAK)	Bulk or Interrupt	Does not depend on the setting	Returns NAK in response to the token from the USB host
	Isochronous	Receiving direction (DIR = 0)	Returns nothing in response to the token from the USB host
		Transmitting direction (DIR = 1)	Transmits a zero-length packet in response to the token from the USB host
01b (BUF)	Bulk	Receiving direction (DIR = 0)	Receives data and returns ACK or NYET in response to the OUT token from the USB host if the FIFO buffer associated with the selected pipe is ready for reception. Otherwise, returns NAK. Returns ACK in response to the PING token from the USB host if the FIFO buffer associated with the selected pipe is ready for reception. Otherwise, returns NAK.
	Interrupt	Receiving direction (DIR = 0)	Receives data and returns ACK response in response to the OUT token from the USB host if the FIFO buffer associated with the selected pipe is ready for reception. Otherwise, returns NAK.
	Bulk or Interrupt	Transmitting direction (DIR = 1)	Transmits data in response to the token from the USB host if the FIFO buffer associated with the selected pipe is ready for transmission. Otherwise, returns NAK.
	Isochronous	Receiving direction (DIR = 0)	Receives data in response to the OUT token from the USB host if the FIFO buffer associated with the selected pipe is ready for reception. Otherwise, discards the data.
		Transmitting direction (DIR = 1)	Transmits data in response to the token from the USB host if the associated FIFO buffer is ready for transmission. Otherwise, transmits a zero-length packet.
10b (STALL) or 11b (STALL)	Bulk or Interrupt	Does not depend on the setting.	Returns STALL in response to the token from the USB host
	Isochronous	Does not depend on the setting.	Returns nothing in response to the token from the USB host

PBUSY flag (Pipe Busy Flag)

The PBUSY flag indicates whether the selected pipe is being used for the current transaction.

The USBHS changes the PBUSY bit from 0 to 1 on start of the USB transaction for the selected pipe, and changes the PBUSY bit from 1 to 0 on completion of one transaction.

Reading the PBUSY bit by software after PID is set to NAK allows you to check whether changing the pipe setting is possible. For details, see section 33.3.7.1, Pipe control register switching procedures.

SQMON flag (Sequence Toggle Bit Monitor Flag)

The SQMON flag indicates the expected value of the sequence toggle bit for the next transaction of the selected pipe.

When the selected pipe is not the isochronous transfer type, the USBHS toggles the SQMON flag on successful completion of the transaction. However, the USBHS does not toggle the SQMON flag when a DATA-PID mismatch occurs during transfer in the receiving direction.

SQSET bit (Sequence Toggle Bit Set)

Setting the SQSET bit to 1 through the software causes the USBHS to set DATA1 as the expected value of the sequence toggle bit for the next transaction on the selected pipe.

SQCLR bit (Sequence Toggle Bit Clear)

Setting the SQCLR bit to 1 through the software causes the USBHS to clear the expected value of the sequence toggle bit for the next transaction on the selected pipe to DATA0.

Table 33.11 USBHS在设备控制器模式下基于PIPEnCTR.PID[1:0]设置的操作

PID[1:0] value	传输类型（TYPE[1:0]值）	传输方向（DIR值）	USBHS operation
00b (NAK)	批量或中断	不依赖于设置	返回NAK以响应来自USB主机的令牌
	Isochronous	接收方向(DIR=0)	响应来自USB主机的令牌，不返回任何内容
		发射方向(DIR=1)	传输一个长度为零的数据包以响应来自USB主机的令牌
01b (BUF)	Bulk	接收方向(DIR=0)	如果与所选管道关联的FIFO缓冲区已准备好接收，则接收数据并返回ACK或NYET以响应来自USB主机的OUT令牌。否则，返回NAK。如果与所选管道关联的FIFO缓冲区已准备好接收，则返回ACK以响应来自USB主机的PING令牌。否则，返回NAK。
	Interrupt	接收方向(DIR=0)	如果与所选管道关联的FIFO缓冲区已准备好接收，则接收数据并返回ACK响应以响应来自USB主机的OUT令牌。否则，返回NAK。
	批量或中断	发射方向(DIR=1)	如果与所选管道关联的FIFO缓冲区已准备好传输，则传输数据以响应来自USB主机的令牌。否则，返回NAK。
	Isochronous	接收方向(DIR=0)	如果与所选管道关联的FIFO缓冲区已准备好接收，则接收数据以响应来自USB主机的OUT令牌。否则，丢弃数据。
		发射方向(DIR=1)	如果关联的FIFO缓冲区已准备好传输，则传输数据以响应来自USB主机的令牌。否则，发送零长度数据包。
10b (STALL) or 11b (STALL)	批量或中断	不依赖于设置。	返回STALL以响应来自USB主机的令牌
	Isochronous	不依赖于设置。	响应来自USB主机的令牌，不返回任何内容

PBUSY标志（管道忙标志）

PBUSY标志指示所选管道是否正在用于当前事务。

USBHS在所选管道的USB事务开始时将PBUSY位从0更改为1，并更改PBUSY位在一个事务完成时从1变为0。

在PID设置为NAK后，通过软件读取PBUSY位可以检查是否可以更改管道设置。详见33.3.7.1管道控制寄存器切换流程。

SQMON标志（序列切换位监视器标志）

SQMON标志指示所选管道的下一个事务的序列切换位的预期值。

当所选管道不是同步传输类型时，USBHS在事务成功完成时切换SQMON标志。但是，当在接收方向的传输过程中发生DATA-PID不匹配时，USBHS不会触发SQMON标志。

SQSET位（序列切换位设置）

通过软件将SQSET位设置为1会导致USBHS将DATA1设置为所选管道上下一个事务的序列切换位的预期值。

SQCLR位（序列切换位清除）

通过软件将SQCLR位设置为1会导致USBHS将所选管道上下一个事务的序列切换位的预期值清除为DATA0。

In host controller mode, when this bit is set to 1 for a bulk OUT transfer pipe, the USBHS starts the next transfer for the selected pipe from a PING token.

ACLRM bit (Auto Buffer Clear Mode)

The ACLRM bit enables or disables auto buffer clear mode for the selected pipe. To completely clear the data in the FIFO buffer allocated to the selected pipe, write 1 and then 0 to the ACLRM bit continuously.

Table 33.12 shows the data cleared by writing 1 and 0 continuously to the ACLRM bit and the cases in which this processing is required.

Table 33.12 Data cleared by the USBHS when ACLRM = 1

Number	Data cleared by setting the ACLRM bit	Situations requiring data clear
1	All data in the FIFO buffer allocated to the selected pipe (two FIFO buffers in double buffer mode)	When clearing all data in the FIFO buffer allocated to the selected pipe
2	Interval count value when the selected pipe is the isochronous transfer type	When resetting the interval count value

ATREPM bit (Auto Response Mode)

The ATREPM bit enables or disables auto response mode for the selected pipe.

This bit can be set to 1 in device controller mode when the selected pipe is the bulk transfer type. When the bit is set to 1, the USBHS responds to the token from the USB host as follows:

- When the selected pipe is set for bulk IN transfers (PIPECFG.TYPE[1:0] = 01b and PIPECFG.DIR = 1):
  a. When the ATREPM bit = 1 and PID = BUF, the USBHS transmits a zero-length packet in response to the IN token.
  b. The USBHS updates (allows toggling of) the sequence toggle bit (DATA-PID) each time the USBHS receives ACK from the USB host. In a single transaction, the IN token is received, a zero-length packet is transmitted, and then ACK is received. The USBHS does not generate the BRDY or BEMP interrupt.
- When the selected pipe is set for bulk OUT transfers (PIPECFG.TYPE[1:0] = 01b and PIPECFG.DIR = 0):

  When the ATREPM bit = 1 and PID = BUF, the USBHS returns NAK in response to the OUT token or PING token and generates an NRDY interrupt.

For USB communication in auto response mode, set the ATREPM bit to 1 while the FIFO buffer is empty. Do not write to the FIFO buffer during USB communication in auto response mode. When the selected pipe uses isochronous transfer, always set this bit to 0.

In host controller mode, always set the ATREPM bit to 0.

CSSTS flag (CSSTS Status Flag)

In host controller mode, the CSSTS flag indicates the complete-split status of a split transaction. It is valid for pipes that are not the isochronous transfer type.

The USBHS sets the CSSTS flag to 1 at the beginning of the complete-split transaction, and sets the CSSTS flag to 0 on detecting completion of the complete-split transaction. If a detach event is detected during the transaction, the CSSTS flag might stay set to 1. In this case, clear the CSSTS flag by setting the CSCLR bit to 1.

Values read from the CSSTS flag in device controller mode are invalid.

CSCLR bit (CSPLIT Status Clear)

In host controller mode, if the software sets the CSCLR bit to 1, the USBHS clears the CSSTS flag to 0. In split transactions, set the CSCLR bit to 1 by software to force the next transfer to restart from start-split. Because the USBHS automatically clears the CSSTS flag to 0 at the end of a successful complete-split transaction in a normal split transaction, clearing the flag through software is not required. Only clear the CSSTS flag using the CSCLR bit when the DVSTCTR0.UACT bit is set to 0 or when no transfer was made after a detach detect. If the CSCLR bit is set to 1 while the CSSTS flag is 0, the CSSTS flag remains 0.

In device controller mode, always write 0 to the CSCLR bit.

在主机控制器模式下，当该位为批量OUT传输管道设置为1时，USBHS从PING令牌开始选定管道的下一次传输。

ACLRM位（自动缓冲区清除模式）

ACLRM位启用或禁用所选管道的自动缓冲区清除模式。彻底清除数据库中的数据FIFO缓冲区分配给所选管道，向ACLRM位连续写入1和0。

表33.12显示了通过向ACLRM位连续写入1和0来清除的数据以及需要进行此处理的情况。

Table 33.12 当ACLRM=1时USBHS清除的数据

Number	通过设置ACLRM位清除数据	需要数据清楚的情况
1	FIFO缓冲区中的所有数据分配给所选管道（双缓冲区模式下的两个FIFO缓冲区）	清除分配给所选管道的FIFO缓冲区中的所有数据时
2	选择管道为等时传输类型时的间隔计数值	重置间隔计数值时

ATREPM位（自动响应模式）

ATREPM位启用或禁用所选管道的自动响应模式。

当所选管道为批量传输类型时，该位可以在设备控制器模式下设置为1。当该位设置为1时，USBHS响应来自USB主机的令牌，如下所示：

- 当所选管道设置为批量IN传输时（PIPECFG.TYPE[1:0]=01b和PIPECFG.DIR=1）：

  一个。当ATREPM位=1且PID=BUF时，USBHS发送一个长度为零的数据包以响应IN令牌。

  湾。每次USBHS从USB主机接收到ACK时，USBHS都会更新（允许切换）序列切换位(DATA-PID)。在单个事务中，收到IN令牌，发送零长度数据包，然后收到ACK。USBHS不会产生BRDY或BEMP中断。

- 当所选管道设置为批量OUT传输时（PIPECFG.TYPE[1:0]=01b和PIPECFG.DIR=0）：

当ATREPM位=1且PID=BUF时，USBHS返回NAK以响应OUT令牌或PING令牌并产生NRDY中断。对于自动响应模式下的USB通信，当FIFO缓冲区为空时，将ATREPM位设置为1。在自动响应模式下的USB通信期间不要写入FIFO缓冲区。当所选管道使用同步传输时，始终将此位设置为0。

在主机控制器模式下，始终将ATREPM位设置为0。

CSSTS标志（CSSTS状态标志）

在主机控制器模式下，CSSTS标志指示拆分事务的完全拆分状态。它对非同步传输类型的管道有效。

USBHS在完成拆分事务开始时将CSSTS标志设置为1，并在检测到完成拆分事务完成时将CSSTS标志设置为0。如果在事务期间检测到分离事件，CSSTS标志可能保持设置为1。在这种情况下，通过将CSCLR位设置为1来清除CSSTS标志。

在设备控制器模式下从CSSTS标志读取的值无效。

CSCLR位（CSPLIT状态清除）

在主机控制器模式下，如果软件将CSCLR位设置为1，则USBHS将CSSTS标志清除为0。在拆分事务中，通过软件将CSCLR位设置为1，以强制下一次传输从start-split重新开始。由于USBHS在正常拆分事务中成功完成拆分事务结束时会自动将CSSTS标志清零，因此不需要通过软件清除该标志。仅当DVSTCTR0.UACT位设置为0或在分离检测后未进行传输时，才使用CSCLR位清除CSSTS标志。如果CSCLR位在CSSTS标志为0时设置为1，则CSSTS标志保持为0。

在设备控制器模式下，始终将0写入CSCLR位。

INBUFM flag (Transmit Buffer Monitor Flag)

The INBUMFM flag indicates the FIFO buffer status for the selected pipe in the transmitting direction.

When the selected pipe is set in the transmitting direction (PIPECFG.DIR = 1), the USBHS sets this bit to 1 when the CPU or DMA/DTC completes writing data to at least one FIFO buffer plane.

The USBHS sets this bit to 0 when the USBHS completes transmission of data from the FIFO buffer plane to which all the data is written. In double buffer mode (PIPECFG.DBLB = 1), the USBHS sets the INBUFM flag to 0 when the USBHS completes transmission of data from the two FIFO buffer planes before the CPU or DMA/DTC completes writing data to one FIFO buffer plane.

The INBUFM flag indicates the same value as the BSTS flag when the selected pipe is in the receiving direction (PIPECFG.DIR = 0).

BSTS flag (Buffer Status Flag)

The BSTS flag indicates the FIFO buffer status for the selected pipe. The meaning of the BSTS flag depends on the PIPECFG.DIR, PIPECFG.BFRE, and DnFIFOSEL.DCLRM settings, as shown in Table 33.13.

Table 33.13 BSTS flag operation

DIR value	BFRE value	DCLRM value	Meaning of BSTS flag
0	0	0	Sets to 1 when receive data can be read from the FIFO buffer, and clears to 0 on completion of data read
		1	Setting prohibited
	1	0	Sets to 1 when receive data can be read from the FIFO buffer, and clears to 0 when the software sets the BCLR bit in the port control register to 1 after the data read is complete
		1	Sets to 1 when receive data can be read from the FIFO buffer, and clears to 0 on completion of data read
1	0	0	Sets to 1 when transmit data can be written to the FIFO buffer, and clears to 0 on completion of data write
		1	Setting prohibited
	1	0	Setting prohibited
		1	Setting prohibited

33.2.39 Pipe n Transaction Counter Enable Register (PIPEnTRE) (n = 1 to 5)

Address(es): USBHS.PIPE1TRE 4006 0090h, USBHS.PIPE2TRE 4006 0094h, USBHS.PIPE3TRE 4006 0098h, USBHS.PIPE4TRE 4006 009Ch, USBHS.PIPE5TRE 4006 00A0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	TRENB	TRCLR	—	—	—	—	—	—	—	—
Value after reset:	x	x	x	x	x	x	0	0	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b7 to b0	—	Reserved	The read value is undefined. The write value should be 0.	R/W
b8	TRCLR	Transaction Counter Clear	0: Invalid (writing 0 has no effect) 1: Clear current counter value.	R/W
b9	TRENB	Transaction Counter Enable	0: Disable transaction counter 1: Enable transaction counter.	R/W
b15 to b10	—	Reserved	The read value is undefined. The write value should be 0.	R/W

Note: Only change the PIPEnTRE settings while the PIPEnCTR.CSSTS flag is 0 and the PIPEnCTR.PID[1:0] bits are 00b (NAK response). Only change the PIPEnCTR.PID[1:0] bits of the selected pipe from 01b (BUF response) to 00b (NAK response)

INBUFM标志（发送缓冲区监控标志）

INBUMFM标志指示发送方向上所选管道的FIFO缓冲区状态。

当所选管道设置为发送方向（PIPECFG.DIR=1）时，USBHS将此位设置为1，此时CPU或DMADTC完成将数据写入至少一个FIFO缓冲平面。

当USBHS完成从写入所有数据的FIFO缓冲区平面的数据传输时，USBHS将该位设置为0。在双缓冲模式(PIPECFG.DBLB=1)中，当USBHS在CPU或DMADTC完成将数据写入一个FIFO缓冲平面之前完成从两个FIFO缓冲平面的数据传输时，USBHS将INBUFM标志设置为0。

当所选管道处于接收方向时（PIPECFG.DIR=0），INBUFM标志表示与BSTS标志相同的值。

BSTS标志（缓冲区状态标志）

BSTS标志指示所选管道的FIFO缓冲区状态。BSTS标志的含义取决于PIPECFG.DIR、PIPECFG.BFRE和DnFIFOSEL.DCLRM设置，如表33.13所示。

Table 33.13 BSTS标志操作

方向值	BFRE value	DCLRM value	BSTS标志的含义
0	0	0	当接收数据可以从FIFO缓冲区读取时设置为1，并在数据读取完成时清除为0
		1	禁止设定
	1	0	接收数据可以从FIFO缓冲区读取时设置为1，当数据读取完成后软件将端口控制寄存器中的BCLR位设置为1时清除为0
		1	当接收数据可以从FIFO缓冲区读取时设置为1，并在数据读取完成时清除为0
1	0	0	当发送数据可以写入FIFO缓冲区时设置为1，并在数据写入完成时清除为0
		1	禁止设定
	1	0	禁止设定
		1	禁止设定

33.2.39 管道n事务计数器启用寄存器(PIPEnTRE)(n=1到5)

Address(es): USBHS.PIPE1TRE 4006 0090h, USBHS.PIPE2TRE 4006 0094h, USBHS.PIPE3TRE 4006 0098h, USBHS.PIPE4TRE 4006 009Ch, USBHS.PIPE5TRE 4006 00A0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	TRENB	TRCLR	—	—	—	—	—	—	—	—
重置后的值：	x	x	x	x	x	x	0	0	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b7 to b0	—	Reserved	读取值未定义。写入值应为0。	R/W
b8	TRCLR	交易计数器清除	0：无效（写0无效）1：清除当前计数器值。	R/W
b9	TRENB	事务计数器启用	0：禁用事务计数器1：启用事务计数器。	R/W
b15 to b10	—	Reserved	读取值未定义。写入值应为0。	R/W

Note: 仅在PIPEnCTR.CSSTS标志为0且PIPEnCTR.PID[1:0]位为00b（NAK响应）时更改PIPEnTRE设置。仅将所选管道的PIPEnCTR.PID[1:0]位从01b（BUF响应）更改为00b（NAK响应）

after confirming that the value of the PIPEnCTR.PBUSY and PIPEnCTR.CSSTS flags is 0. However, software processing to check the PIPEnCTR.PBUSY flag is not required if the USBHS has changed the PID[1:0] bits to 00b (NAK response).

TRCLR bit (Transaction Counter Clear)

When the TRCLR bit sets to 1, the USBHS clears the count value of the transaction counter associated with the selected pipe and then clears the TRCLR bit to 0.

TRENB bit (Transaction Counter Enable)

The TRENB bit enables or disables the transaction counter.

For receiving pipes, setting the TRENB bit to 1 after setting the total number of the packets to be received in the PIPEnTRN.TRNCNT[15:0] bits through the software allows the USBHS to control hardware on having received the number of packets equal to the TRNCNT[15:0] setting as follows:

- When the PIPECFG.SHTNAK bit is 1, the USBHS changes the PID bits to NAK for the associated pipe on having received the number of packets equal to the TRNCNT[15:0] setting
- When the PIPECFG.BFRE bit is 1, the USBHS asserts the BRDY interrupt on having received the number of packets equal to the TRNCNT[15:0] setting and then reading the last received data.

For transmitting pipes, set the TRENB bit to 0.

When the transaction counter is not used, set this bit to 0. When the transaction counter is used, set the TRNCNT[15:0] bits before setting this bit to 1. Set this bit to 1 before receiving the first packet to be counted by the transaction counter.

33.2.40 Pipe n Transaction Counter Register (PIPEnTRN) (n = 1 to 5)

Address(es): USBHS.PIPE1TRN 4006 0092h, USBHS.PIPE2TRN 4006 0096h, USBHS.PIPE3TRN 4006 009Ah, USBHS.PIPE4TRN 4006 009Eh, USBHS.PIPE5TRN 4006 00A2h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TRNCNT[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b15 to b0	TRNCNT[15:0]	Transaction Counter*1	• When written to: Specifies the total packets (number of transactions) to be received by pipe n. • When read from: When PIPEnTRE.TRENB is 0, indicates the specified number of transactions. When PIPEnTRE.TRENB is 1, indicates the current transaction count.	R/W

Note 1. Only set the TRNCNT[15:0] bits while PID is NAK and PIPEnTRE.TRENB is 0. Before setting these bits, check that the PIPEnCTR.CSSTS and PIPEnCTR.PBUSY flags are 0, and then change the PIPEnCTR.PID[1:0] bits from 01b (BUF) to 00b (NAK). If the PIPEnCTR.PID[1:0] bits are changed to 00b (NAK) by the USBHS, checking the PBUSY flag through the software is not necessary.

The PIPEnTRN registers retain their settings during a USB bus reset.

TRNCNT[15:0] bits (Transaction Counter)

The USBHS increments the value of the TRNCNT[15:0] bits by one when all of the following conditions are satisfied on receiving the packet:

- The PIPEnTRE.TRENB bit is 1
- (TRNCNT[15:0] set value ≠ current counter value + 1) on receiving the packet
- The payload of the received packet agrees with the PIPEMAXP.MXPS[8:0] setting.

The USBHS clears the value of the TRNCNT[15:0] bits to 0 when any of the following conditions is satisfied.

在确认PIPEnCTR.PBUSY和PIPEnCTR.CSSTS标志的值为0之后。但是，如果USBHS已将PID[1:0]位更改为00b（NAK响应），则不需要检查PIPEnCTR.PBUSY标志的软件处理）。

TRCLR位（事务计数器清零）

当TRCLR位设置为1时，USBHS清除与所选管道关联的事务计数器的计数值，然后将TRCLR位清除为0。

TRENB位（事务计数器使能）

TRENB位启用或禁用事务计数器。

对于接收管道，在设置接收管道的总包数后，将TRENB位设置为1
PIPEnTRN.TRNCNT[15:0]位通过软件允许USBHS在接收到等于TRNCNT[15:0]设置的数据包数量时控制硬件，如下所示：

- 当PIPECFG.SHTNAK位为1时，USBHS在接收到等于TRNCNT[15:0]设置的数据包数量时将关联管道的PID位更改为NAK
- 当PIPECFG.BFRE位为1时，USBHS在接收到等于TRNCNT[15:0]设置的数据包数量时断言BRDY中断，然后读取最后接收到的数据。

对于传输管道，将TRENB位设置为0。

当不使用事务计数器时，将该位设置为0。当使用事务计数器时，将该位设置为1之前设置TRNCNT[15:0]位。在接收第一个要计数的数据包之前将该位设置为1由交易柜台。

33.2.40 管道n事务计数器寄存器(PIPEnTRN)(n=1到5)

Address(es): USBHS.PIPE1TRN 4006 0092h, USBHS.PIPE2TRN 4006 0096h, USBHS.PIPE3TRN 4006 009Ah, USBHS.PIPE4TRN 4006 009Eh, USBHS.PIPE5TRN 4006 00A2h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TRNCNT[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称		Description	R/W
b15 to b0	TRNCNT[15:0]	交易柜台	*1	当写给： 指定管道n接收的总数据包（事务数）。 从以下位置读取时： 当PIPEnTRE.TRENB为0时，表示指定的事务数。当PIPEnTRE.TRENB为1时，表示当前事务计数。	R/W

Note 1. 仅在PID为NAK且PIPEnTRE.TRENB为0时设置TRNCNT[15:0]位。在设置这些位之前，请检查PIPEnCTR.CSSTS和PIPEnCTR.PBUSY标志为0，然后将PIPEnCTR.PID[1:0]位从01b(BUF)更改为00b(NAK)。如果PIPEnCTR.PID[1:0]位被USBHS更改为00b(NAK)，则无需通过软件检查PBUSY标志。

PIPEnTRN寄存器在USB总线复位期间保留其设置。

TRNCNT[15:0]位（事务计数器）

当接收到数据包时满足以下所有条件时，USBHS将TRNCNT[15:0]位的值加一：

- PIPEnTRE.TRENB位为1
- (TRNCNT[15:0]设定值≠当前计数器值+1)收到数据包
- 接收到的数据包的有效负载与PIPEMAXP.MXPS[8:0]设置一致。

当满足以下任一条件时，USBHS将TRNCNT[15:0]位的值清零。

All of the following conditions are satisfied:

- The PIPEnTRE.TRENB bit = 1
- (TRNCNT[15:0] set value = current counter value + 1) on receiving the packet
- The payload of the received packet agrees with the PIPEMAXP.MXPS[8:0] setting.

Both the following conditions are satisfied:

- The PIPEnTRE.TRENB bit = 1
- The USBHS received a short packet.

Both the following conditions are satisfied:

- The PIPEnTRE.TRENB bit = 1
- The PIPEnTRE.TRCLR bit was set to 1 by software.

For transmitting pipes, set the TRNCNT[15:0] bits to 0. When the transaction counter is not used, set the TRNCNT[15:0] bits to 0.

Setting the number of transactions to be transferred to the TRNCNT[15:0] bits is enabled only when the PIPEnTRE.TRENB bit is 0. To set the number of transactions to be transferred, set the TRCLR bit to 1 to clear the current counter value before setting the PIPEnTRE.TRENB bit to 1.

33.2.41 Device Address m Configuration Register (DEVADDm) (m = 0 to A)

Address(es): USBHS.DEVADD0 4006 00D0h, USBHS.DEVADD1 4006 00D2h, USBHS.DEVADD2 4006 00D4h, USBHS.DEVADD3 4006 00D6h, USBHS.DEVADD4 4006 00D8h, USBHS.DEVADD5 4006 00DAh, USBHS.DEVADD6 4006 00DCh, USBHS.DEVADD7 4006 00DEh, USBHS.DEVADD8 4006 00E0h, USBHS.DEVADD9 4006 00E2h, USBHS.DEVADDA 4006 00E4h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	UPPHUB[3:0]			HUBPORT[2:0]			USBSPD[1:0]			—	—	—	—	—	—
Value after reset:	x	0	0	0	0	0	0	0	0	0	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b5 to b0	—	Reserved	The read value is undefined. The write value should be 0.	R/W
b7, b6	USBSPD[1:0]	Transfer Speed of Communication Target Device	b7 b6 0 0: Do not use DEVADDm 0 1: Low speed 1 0: Full speed 1 1: High speed.	R/W
b10 to b8	HUBPORT[2:0]	Communication Target Connecting Hub Port	b10 b8 0 0 0: Connect directly to the USBHS port 001 to 111: Port number of the hub.	R/W
b14 to b11	UPPHUB[3:0]	Communication Target Connecting Hub Register	b14 b11 0 0 0 0: Connect directly to the USBHS port 0001 to 1010: USB address of the hub 1011 to 1111: Reserved.	R/W
b15	—	Reserved	The read value is undefined. The write value should be 0.	R/W

The DEVADDm register specifies the transfer speed of the peripheral device that is the communication target for pipes 0 to 9.

In host controller mode, set all DEVADDm bits before starting communication to any pipes. Only change the bits in DEVADDm when no valid pipes are using the bit settings. A valid pipe is defined as one that satisfies both of the following conditions:

- DEVADDm is selected in the DEVSEL[3:0] bits
- The PID[1:0] bits are set to BUF for the selected pipe, or the selected pipe is the DCP with the DCPCTR.SUREQ bit set to 1.

满足以下所有条件：

- PIPEnTRE.TRENB位=1
- (TRNCNT[15:0]设置值=当前计数器值+1)接收数据包时
- 接收到的数据包的有效负载与PIPEMAXP.MXPS[8:0]设置一致。

满足以下两个条件：

- PIPEnTRE.TRENB位=1
- USBHS收到一个短数据包。

满足以下两个条件：

- PIPEnTRE.TRENB位=1
- PIPEnTRE.TRCLR位由软件设置为1。

对于传输管道，将TRNCNT[15:0]位设置为0。当不使用事务计数器时，将TRNCNT[15:0]位设置为0。

设置要传输到TRNCNT[15:0]位的事务数仅在PIPEnTRE.TRENB位为0。要设置要传输的事务数，请将TRCLR位设置为1以清除当前计数器值，然后再将PIPEnTRE.TRENB位设置为1。

33.2.41 器件地址m配置寄存器(DEVADDm)(m=0toA)

Address(es): USBHS.DEVADD0 4006 00D0h, USBHS.DEVADD1 4006 00D2h, USBHS.DEVADD2 4006 00D4h, USBHS.DEVADD3 4006 00D6h, USBHS.DEVADD4 4006 00D8h, USBHS.DEVADD5 4006 00DAh, USBHS.DEVADD6 4006 00DCh, USBHS.DEVADD7 4006 00DEh, USBHS.DEVADD8 4006 00E0h, USBHS.DEVADD9 4006 00E2h, USBHS.DEVADDA 4006 00E4h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	UPPHUB[3:0]			HUBPORT[2:0]			USBSPD[1:0]			—	—	—	—	—	—
重置后的值：	x	0	0	0	0	0	0	0	0	0	x	x	x	x	x	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b5 to b0	—	Reserved	读取值未定义。写入值应为0。	R/W
b7, b6	USBSPD[1:0]	传输速度 通信目标设备	b7 b6 0 0：不使用DEVADDm 0 1：低速 1 0：全速 1 1：高速。	R/W
b10 to b8	HUBPORT[2:0]	沟通对象 连接集线器端口	b10 b8 00：直接连接到USBHS端口001至111：集线器的端口号。	R/W
b14 to b11	UPPHUB[3:0]	沟通对象 连接集线器寄存器	b14 b11 00：直接连接USBHS端口0001至1010：集线器的USB地址1011至1111：保留。	R/W
b15	—	Reserved	读取值未定义。写入值应为0。	R/W

DEVADDm寄存器指定作为管道0到9的通信目标的外围设备的传输速度。

在主机控制器模式下，在开始与任何管道通信之前设置所有DEVADDm位。仅更改中的位DEVADDm当没有有效管道使用位设置时。有效管道被定义为同时满足以下两个条件的管道：

- DEVADDm在DEVSEL[3:0]位中选择
- 所选管道的PID[1:0]位设置为BUF，或者所选管道是DCPCTR.SUREQ位设置为1的DCP。

In device controller mode, set all bits in this register to 0.

USBSPD[1:0] bits (Transfer Speed of Communication Target Device)

The USBSPD[1:0] bits specify the USB transfer speed of the target peripheral device. In host controller mode, the USBHS generates packets based on the USBSPD[1:0] setting. In device controller mode, set these bits to 00b.

HUBPORT[2:0] bits (Communication Target Connecting Hub Port)

In host controller mode, the USBHS generates packets based on the HUBPORT[2:0] setting when performing a split transaction.

UPPHUB[3:0] bits (Communication Target Connecting Hub Register)

In host controller mode, the USBHS generates packets based on the UPPHUB[3:0] setting when performing a split transaction.

33.2.42 Low Power Control Register (LPCTRL)

Address(es): USBHS.LPCTRL 4006 0100h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	HWUPM	—	—	—	—	—	—	—
Value after reset:	x	x	x	x	x	x	x	0	0	x	x	x	x	x	x	0

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b6 to b0	—	Reserved	The read value is undefined. The write value should be 0.	R/W
b7	HWUPM	Resume Return Mode Setting	0: Hardware does not recover while CPU clock inactive 1: Hardware recovers while CPU clock inactive.	R/W
b8	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b15 to b9	—	Reserved	The read value is undefined. The write value should be 0.	R/W

HWUPM bit (Resume Return Mode Setting)

The HWUPM bit specifies whether to enable hardware processing for return from low power mode even while the CPU clock is inactive.

In device controller mode, processing for return from low power mode on detecting Resume is enabled even while the CPU clock is inactive.

This bit specifies whether to detect Resume while the CPU clock is inactive. The PL1CTRL1.L1EXTMD bit controls whether to make a hardware return. To make a hardware return from the LPM L1 low power state while the CPU clock is inactive, set this bit and the PL1CTRL1.L1EXTMD bit to 1.

33.2.43 Low Power Status Register (LPSTS)

Address(es): USBHS.LPSTS 4006 0102h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	SUSPENDM	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	x	0	x	0	x	x	x	0	x	x	x	x	0	x	0	0

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b1, b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

在设备控制器模式下，将此寄存器中的所有位设置为0。

USBSPD[1:0]位（通信目标设备的传输速度）

USBSPD[1:0]位指定目标外围设备的USB传输速度。在主机控制器模式下，
USBHS根据USBSPD[1:0]设置生成数据包。在设备控制器模式下，将这些位设置为00b。

HUBPORT[2:0]位（通信目标连接集线器端口）

在主机控制器模式下，USBHS在执行拆分事务时根据HUBPORT[2:0]设置生成数据包。

UPPHUB[3:0]位（通信目标连接集线器寄存器）

在主机控制器模式下，USBHS在执行拆分事务时根据UPPHUB[3:0]设置生成数据包。

33.2.42 低功耗控制寄存器(LPCTRL)

Address(es): USBHS.LPCTRL 4006 0100h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	HWUPM	—	—	—	—	—	—	—
重置后的值：	x	x	x	x	x	x	x	0	0	x	x	x	x	x	x	0

x: Undefined

Bit	Symbol	位名称	Description	R/W
b6 to b0	—	Reserved	读取值未定义。写入值应为0。	R/W
b7	HWUPM	恢复返回模式设置	0：CPU时钟不活动时硬件不恢复1：CPU时钟不活动时硬件恢复。	R/W
b8	—	Reserved	该位读取为0。写入值应为0。	R/W
b15 to b9	—	Reserved	读取值未定义。写入值应为0。	R/W

HWUPM位（恢复返回模式设置）

HWUPM位指定是否启用硬件处理以从低功耗模式返回，即使在CPU时钟不活动时也是如此。

在设备控制器模式下，即使在
CPU时钟处于非活动状态。

该位指定是否在CPU时钟不活动时检测Resume。PL1CTRL1.L1EXTMD位控制是否进行硬件返回。要在CPU时钟不活动时使硬件从LPML1低功耗状态返回，设置该位和PL1CTRL1.L1EXTMD位为1。

33.2.43 低功耗状态寄存器(LPSTS)

Address(es): USBHS.LPSTS 4006 0102h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	SUSPENDM	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	x	0	x	0	x	x	x	0	x	x	x	x	0	x	0	0

x: Undefined

Bit	Symbol	位名称	Description	R/W
b1, b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Bit	Symbol	Bit name	Description	R/W
b2	—	Reserved	The read value is undefined. The write value should be 0.	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b7 to b4	—	Reserved	The read value is undefined. The write value should be 0.	R/W
b8	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b11 to b9	—	Reserved	The read value is undefined. The write value should be 0.	R/W
b12	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b13	—	Reserved	The read value is undefined. The write value should be 0.	R/W
b14	SUSPENDM	UTMI SuspendM Control	0: UTMI suspension mode 1: UTMI normal mode.	R/W
b15	—	Reserved	The read value is undefined. The write value should be 0.	R/W

SUSPENDM bit (UTMI SuspendM Control)

The SUSPENDM bit controls the SuspendM signal to be sent to the PHY designed under the UTMI specification. The initial value is 0 with the UTMI is in suspension mode.

Set this bit to 1 to supply the PHY clock to operate the USB2.0 host or device controller.

In compliance with the UTMI specification, clock output is normally controlled by the SuspendM signal. When the SUSPENDM bit is 0, the clock to LINK is stopped. Because the PHY in this MCU follows the UTMI specification, setting the SUSPENDM bit to 1 is required to supply the PHY clock. For the clock settings, see section 33.3.3, Supplying the Clock.

When the SUSPENDM bit is 0, the USBHS cannot be written to but can be read from. The registers listed in Table 33.14 are writable even when the SUSPENDM bit is 0.

Table 33.14 Registers that can be written to by software when SUSPENDM = 0

Address	Register or bit name
4006 0000h	SYSCFG register
4006 0002h	BUSWAIT register
4006 0032h	INTENB1.PDDETINTE bit
4006 0100h	LPCTRL register
4006 0102h	LPSTS register
4006 0140h	BCCTRL register

The value written to the SYSCFG register while the PHY clock is inactive is updated only after the PHY clock begins oscillating. The PHY clock oscillates in the following cases described in this section.

When SUSPENDM bit is set to 1, the PLLSTA.PLLLOCK flag is set to 1 after the predetermined time has passed. The USB-PHY internal PLL is stopped when the SUSPENDM bit is set to 0.

For details on CL-only mode, see section 33.2.17, PHY Setting Register (PHYSET).

If the PL1CTRL1.L1EXTMD bit is 0, setting or clearing of this bit is controlled by software. If the PL1CTRL1.L1EXTMD bit is 1, transitions to the L1 or L2 state of this bit are controlled by software and recovery from the L1 or L2 state is controlled by hardware.

Bit	Symbol	位名称	Description	R/W
b2	—	Reserved	读取值未定义。写入值应为0。	R/W
b3	—	Reserved	该位读取为0。写入值应为0。	R/W
b7 to b4	—	Reserved	读取值未定义。写入值应为0。	R/W
b8	—	Reserved	该位读取为0。写入值应为0。	R/W
b11 to b9	—	Reserved	读取值未定义。写入值应为0。	R/W
b12	—	Reserved	该位读取为0。写入值应为0。	R/W
b13	—	Reserved	读取值未定义。写入值应为0。	R/W
b14	SUSPENDM	UTMI SuspendM Control	0：UTMI暂停模式1：UTMI正常模式。	R/W
b15	—	Reserved	读取值未定义。写入值应为0。	R/W

SUSPENDM位（UTMISuspendM控制）

SUSPENDM位控制要发送到根据UTMI规范设计的PHY的SuspendM信号。初始值为0，UTMI处于暂停模式。

将此位设置为1以提供PHY时钟以操作USB2.0主机或设备控制器。

根据UTMI规范，时钟输出通常由SuspendM信号控制。当SUSPENDM位为0时，LINK的时钟停止。由于该MCU中的PHY遵循UTMI规范，因此需要将SUSPENDM位设置为1以提供PHY时钟。有关时钟设置，请参阅第33.3.3节，提供时钟。

当SUSPENDM位为0时，USBHS不能被写入但可以被读取。即使SUSPENDM位为0，表33.14中列出的寄存器也是可写的。

Table 33.14 SUSPENDM=0时软件可写入的寄存器

Address	寄存器或位名称
4006 0000h	SYSCFG register
4006 0002h	BUSWAIT register
4006 0032h	INTENB1.PDDETINTE bit
4006 0100h	LPCTRL register
4006 0102h	LPSTS register
4006 0140h	BCCTRL register

PHY时钟不活动时写入SYSCFG寄存器的值仅在PHY时钟开始振荡后更新。PHY时钟在本节所述的以下情况下振荡。

当SUSPENDM位设置为1时，PLLSTA.PLLLOCK标志在经过预定时间后设置为1。这
当SUSPENDM位设置为0时，USB-PHY内部PLL停止。

有关CL-only模式的详细信息，请参见第33.2.17节，PHY设置寄存器(PHYSET)。

如果PL1CTRL1.L1EXTMD位为0，则该位的设置或清除由软件控制。如果
PL1CTRL1.L1EXTMD位为1，转换到该位的L1或L2状态由软件控制，从L1或L2状态恢复由硬件控制。

33.2.44 Battery Charging Control Register (BCCTRL)

Address(es): USBHS.BCCTRL 4006 0140h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	PDDETSTS	CHGDETSTS	—	—	DCPMODE	VDMSRCE	IDPSINKE	VDPSRCE	IDMSINKE	IDPSRCE
Value after reset:	x	x	x	x	x	x	0	0	x	x	0	0	0	0	0	0

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b0	IDPSRCE	IDPSRC Control*2	0: Disable IDP_SRC circuit 1: Enable IDP_SRC circuit.	R/W
b1	IDMSINKE	IDMSINK Control*2	0: Disable IDM_SINK circuit 1: Enable IDM_SINK circuit.	R/W
b2	VDPSRCE	VDPSRC Control*2	0: Disable VDP_SRC circuit 1: Enable VDP_SRC circuit.	R/W
b3	IDPSINKE	IDPSINK Control*2	0: Disable IDP_SINK circuit 1: Enable IDP_SINK circuit.	R/W
b4	VDMSRCE	VDMSRC Control*2	0: Disable VDM_SRC circuit 1: Enable VDM_SRC circuit.	R/W
b5	DCPMODE	DCP Mode Control	0: Disable RDCP_DAT resistor 1: Enable RDCP_DAT resistor.	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	CHGDETSTS	CHGDET Status Flag	0: The CHGDET pin is at low level. 1: The CHGDET pin is at high level.	R
b9	PDDETSTS	PDDET Status Flag	0: The PDDET pin is at low level. 1: The PDDET pin is at high level.	R
b15 to b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. All bits in the BCCTRL register can be changed while the UTMI clock is inactive.
Note 2. In device controller mode, set the IDPSRCE, IDMSINKE, VDPSRCE, IDPSINKE, and VDMSRCE bits to 1 after setting the SYSCFG.DRPD bit to 0.

IDPSRCE bit (IDPSRC Control)

In device controller mode, set the IDPSRCE bit to 1 to perform data contact detection.

The Battery Charging Standard provides two ways to handle data contact detection, one through the software and one using hardware to contact the data line. The IDPSRE bit uses the hardware method.

When the IDPSRE bit is set to 1, the USBHS enables the IDP_SRC circuit and, at the same time, controls D- pull-down. (D- pull-down is controlled with the VUH_DMPULLDOWN signal.)

IDMSINKE bit (IDMSINK Control)

In device controller mode, set the IDMSINKE bit to 1 to perform primary detection.

VDPSRCE bit (VDPSRC Control)

In device controller mode, set the VDPSRCE bit to 1 to perform primary detection.

IDPSINKE bit (IDPSINK Control)

In device controller mode, set the IDPSINKE bit to 1 to perform secondary detection. In host controller mode, set this bit to 1 to enable the portable device detection circuit.

VDMSRCE bit (VDMSRC Control)

In device controller mode, set the VDMSRCE bit to 1 to perform secondary detection. Setting this bit to 1 enables the DCP detection circuit. In host controller mode, set this bit to 1 when a portable device is detected. Setting this bit to 1

33.2.44 电池充电控制寄存器(BCCTRL)

Address(es): USBHS.BCCTRL 4006 0140h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	PDDETSTS	CHGDETSTS	—	—	DCPMODE	VDMSRCE	IDPSINKE	VDPSRCE	IDMSINKE	IDPSRCE
重置后的值：	x	x	x	x	x	x	0	0	x	x	0	0	0	0	0	0

x: Undefined

Bit	Symbol	位名称	Description	R/W
b0	IDPSRCE	IDPSRC Control*2	0：禁用IDP_SRC电路1：启用IDP_SRC电路。	R/W
b1	IDMSINKE	IDMSINK Control*2	0：禁用IDM_SINK电路1：启用IDM_SINK电路。	R/W
b2	VDPSRCE	VDPSRC Control*2	0：禁用VDP_SRC电路1：启用VDP_SRC电路。	R/W
b3	IDPSINKE	IDPSINK Control*2	0：禁用IDP_SINK电路1：启用IDP_SINK电路。	R/W
b4	VDMSRCE	VDMSRC Control*2	0：禁用VDM_SRC电路1：启用VDM_SRC电路。	R/W
b5	DCPMODE	DCP模式控制	0：禁用RDCP_DAT电阻1：启用RDCP_DAT电阻。	R/W
b7, b6	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b8	CHGDETSTS	CHGDET状态标志	0：CHGDET引脚为低电平。1：CHGDET引脚为高电平。	R
b9	PDDETSTS	PDDET状态标志	0：PDDET引脚为低电平。1：PDDET引脚为高电平。	R
b15 to b10	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 当UTMI时钟无效时，可以更改BCCTRL寄存器中的所有位。
Note 2. 在设备控制器模式下，将IDPSRCE、IDMSINKE、VDPSRCE、IDPSINKE和VDMSRCE位设置为1，然后将SYSCFG.DRPD位为0。

IDPSRCE位（IDPSRC控制）

在设备控制器模式下，将IDPSRCE位设置为1以执行数据接触检测。

电池充电标准提供了两种处理数据接触检测的方法，一种是通过软件，另一种是通过硬件接触数据线。IDPSRE位使用硬件方法。

当IDPSRE位设置为1时，USBHS使能IDP_SRC电路，同时控制Dpull-down。（Dpull-down由VUH_DMPULLDOWN信号控制。）

IDMSINKE位（IDMSINK控制）

在设备控制器模式下，将IDMSINKE位设置为1以执行主要检测。

VDPSRCE位（VDPSRC控制）

在设备控制器模式下，将VDPSRCE位设置为1以执行主检测。

IDPSINKE位（IDPSINK控制）

在设备控制器模式下，将IDPSINKE位设置为1以执行辅助检测。在主机控制器模式下，将此位设置为1以启用便携式设备检测电路。

VDMSRCE位（VDMSRC控制）

在设备控制器模式下，将VDMSRCE位设置为1以执行辅助检测。将此位设置为1启用DCP检测电路。在主机控制器模式下，当检测到便携式设备时，将该位设置为1。将此位设置为1

allows the device that is performing primary detection to determine the charger detection method.

DCPMODE bit (DCP Mode Control)

Set the DCPMODE bit to 1 to operate as a dedicated charging port (DCP). Setting this bit to 1 disables USB communication.

CHGDETSTS flag (CHGDET Status Flag)

The CHGDETSTS flag indicates the charger port detection state.

PDDETSTS flag (PDDET Status Flag)

The PDDETSTS flag indicates the following states based on the controller mode:

- In host controller mode: PD detection state
- In device controller mode: DCP detection state.

33.2.45 Function L1 Control Register 1 (PL1CTRL1)

Address(es): USBHS.PL1CTRL1 4006 0144h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	L1EXTMD	—	—	HIRDTHR[3:0]				DVSQ[3:0]				L1NEGOMD	L1RESPMD[1:0]		L1RESPEN
Value after reset:	x	0	x	x	0	0	0	0	0	0	0	0	0	0	0	0

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b0	L1RESPEN	L1 Response Enable	0: Do not support LPM 1: Support LPM.	R/W
b2, b1	L1RESPMD[1:0]	L1 Response Mode	b2 b1 0 0: NYET response 0 1: ACK response 1 0: STALL response 1 1: Response based on L1NEGOMD setting.	R/W
b3	L1NEGOMD	L1 Response Negotiation Control	0: Return ACK when received HIRD is larger than HIRDTHR[3:0]. Otherwise (including when HIRD = HIRDTHR[3:0]), return NYET. 1: Return ACK when received HIRD is smaller than HIRDTHR[3:0]. Otherwise (including when HIRD = HIRDTHR[3:0]), return NYET. This bit is only valid when the L1RESPMD[1:0] value is 11b.	R/W
b7 to b4	DVSQ[3:0]	DVSQ Extension Flag	b7 b4 0 0 0 0: Powered state 0 0 0 1: Default state 0 0 1 0: Address state 0 0 1 1: Configured state 0 1 x x: Suspend state 1 0 x x: L1 state.	R
b11 to b8	HIRDTHR[3:0]	L1 Response Negotiation Threshold Value	HIRD threshold value used when the L1RESPMD[1:0] bits are 11b. The format is the same as the HIRD field in HL1CTRL.	R/W
b13, b12	—	Reserved	The read value is undefined. The write value should be 0.	R/W
b14	L1EXTMD	PHY Control Mode at L1 Return	0: Do not set LPSTS.SUSPENDM bit through hardware when Host K is received 1: Set LPSTS.SUSPENDM bit through hardware when Host K is received.	R/W
b15	—	Reserved	The read value is undefined. The write value should be 0.	R/W

L1RESPEN bit (L1 Response Enable)

If the USBHS receives an LPM token while the L1RESPEN bit is 0, it returns no response. If the USBHS receives an

允许执行主要检测的设备确定充电器检测方法。

DCPMODE位（DCP模式控制）

将DCPMODE位设置为1可用作专用充电端口(DCP)。将此位设置为1将禁用USB通信。

CHGDETSTS标志（CHGDET状态标志）

CHGDETSTS标志指示充电器端口检测状态。

PDDETSTS标志（PDDET状态标志）

PDDETSTS标志根据控制器模式指示以下状态：

- 主控制器模式下：PD检测状态
- 在设备控制器模式下：DCP检测状态。

33.2.45 功能L1控制寄存器1(PL1CTRL1)

Address(es): USBHS.PL1CTRL1 4006 0144h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	L1EXTMD	—	—	HIRDTHR[3:0]				DVSQ[3:0]				L1NEGOMD	L1RESPMD[1:0]		L1RESPEN
重置后的值：	x	0	x	x	0	0	0	0	0	0	0	0	0	0	0	0

x: Undefined

Bit	Symbol	位名称	Description	R/W
b0	L1RESPEN	L1响应启用	0：不支持LPM1：支持LPM。	R/W
b2, b1	L1RESPMD[1:0]	L1响应模式	b2 b1 0 0：纽约时报回应 0 1：ACK响应 1 0：停止响应 1 1：基于L1NEGOMD设置的响应。	R/W
b3	L1NEGOMD	L1响应协商 Control	0：接收到的HIRD大于时返回ACK HIRDTHR[3:0]。否则（包括当HIRD= HIRDTHR[3:0]），返回NYET。1：当接收到的HIRD小于HIRDTHR[3:0]时返回ACK。否则（包括当HIRD= HIRDTHR[3:0]），返回NYET。 该位仅在L1RESPMD[1:0]值为11b时有效。	R/W
b7 to b4	DVSQ[3:0]	DVSQ扩展标志	b7b40000：上电状态00 01：默认状态0010：地址状态0011：配置状态0 1xx：挂起状态10xx：L1状态。	R
b11 to b8	HIRDTHR[3:0]	L1响应协商 阈值	L1RESPMD[1:0]位为11b时使用的HIRD阈值。格式与HL1CTRL中的HIRD字段相同。	R/W
b13, b12	—	Reserved	读取值未定义。写入值应为0。	R/W
b14	L1EXTMD	L1的PHY控制模式 Return	0：接收到HostK时不通过硬件设置LPSTS.SUSPENDM位1：接收到HostK时通过硬件设置LPSTS.SUSPENDM位。	R/W
b15	—	Reserved	读取值未定义。写入值应为0。	R/W

L1RESPEN位（L1响应使能）

如果USBHS在L1RESPEN位为0时接收到LPM令牌，则它不返回任何响应。如果USBHS收到一个

LPM token while this bit is 1, it returns a response based on the L1RESPMD[1:0] setting.

L1RESPMD[1:0] bits (L1 Response Mode)

When the L1RESPEN bit is set to 1, the USBHS returns a response to the LPM token based on the setting in the L1RESPMD[1:0] bits.

L1NEGOMD bit (L1 Response Negotiation Control)

The L1NEGOMD bit specifies the negotiation function for the HIRD value.

HIRDTHR[3:0] bits (L1 Response Negotiation Threshold Value)

The HIRDTHR[3:0] bits specify the HIRD threshold value used for L1NEGOMD. The format of the set value is the same as the HIRD field in HL1CTRL.

L1EXTMD bit (PHY Control Mode at L1 Return)

The L1EXTMD bit specifies the LPSTS.SUSPENDM bit control method when a host K signal is received in the L1 state while the LPSTS.SUSPENDM bit is 0 and the PHY is inactive.

Similar to the Suspend constraints, because the minimum host K period is 50 µs, the PHY might not recover within the host K period specified for software settings on return. The initial value is within software control, so set this bit to 1 during the initialization process when the L1 state is supported.

The LPSTS.SUSPENDM bit is controlled by software on transition to the L1 state regardless of the setting in this bit. It is not cleared by hardware.

When this bit is set to 1, the LPSTS.SUSPENDM bit is also set to 1 on return from L2.

33.2.46 Function L1 Control Register 2 (PL1CTRL2)

Address(es): USBHS.PL1CTRL2 4006 0146h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	RWEMON	HIRDMON[3:0]				—	—	—	—	—	—	—	—
Value after reset:	x	x	x	0	0	0	0	0	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b7 to b0	—	Reserved	The read value is undefined. The write value should be 0.	R/W
b11 to b8	HIRDMON[3:0]	HIRD Value Monitor	When set, indicates that the HIRD field value reflects the last-received LPM token.	R
b12	RWEMON	RWE Value Monitor	When set, indicates that the RWE bit value reflects the last-received LPM token.	R
b15 to b13	—	Reserved	The read value is undefined. The write value should be 0.	R/W

HIRDMON[3:0] bits (HIRD Value Monitor)

Access the HIRDMON[3:0] bits when monitoring the HIRD field value of the received LPM token. The bits reflect the HIRD field value of the last received LPM token.

RWEMON bit (RWE Value Monitor)

Access the RWEMON bit when monitoring the RWE field value of the received LPM token. The bits reflect the RWE field value of the last received LPM token.

当该位为1时，LPM令牌会根据L1RESPMD[1:0]设置返回响应。

L1RESPMD[1:0]位（L1响应模式）

当L1RESPEN位设置为1时，USBHS根据
L1RESPMD[1:0] bits.

L1NEGOMD位（L1响应协商控制）

L1NEGOMD位指定HIRD值的协商功能。

HIRDTHR[3:0]位（L1响应协商阈值）

HIRDTHR[3:0]位指定用于L1NEGOMD的HIRD阈值。设置值的格式与HL1CTRL中的HIRD字段相同。

L1EXTMD位（L1返回时的PHY控制模式）

L1EXTMD位指定LPSTS.SUSPENDM位在L1状态下接收到主机K信号而LPSTS.SUSPENDM位为0且PHY处于非活动状态时的LPSTS.SUSPENDM位控制方法。

与挂起约束类似，由于最小主机K周期为50μs，因此PHY可能无法在返回时为软件设置指定的主机K周期内恢复。初始值在软件控制范围内，因此在支持L1状态的初始化过程中将此位设置为1。

LPSTS.SUSPENDM位在转换到L1状态时由软件控制，无论该位的设置如何。它不会被硬件清除。

当该位设置为1时，LPSTS.SUSPENDM位在从L2返回时也设置为1。

33.2.46 功能L1控制寄存器2(PL1CTRL2)

Address(es): USBHS.PL1CTRL2 4006 0146h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	RWEMON	HIRDMON[3:0]				—	—	—	—	—	—	—	—
重置后的值：	x	x	x	0	0	0	0	0	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b7 to b0	—	Reserved	读取值未定义。写入值应为0。	R/W
b11 to b8	HIRDMON[3:0]	HIRD价值监控器	设置时，指示HIRD字段值反映最后收到的LPM令牌。	R
b12	RWEMON	RWE价值监控器	设置时，指示RWE位值反映最后收到的LPM令牌。	R
b15 to b13	—	Reserved	读取值未定义。写入值应为0。	R/W

HIRDMON[3:0]位（HIRD值监视器）

在监控接收到的LPM令牌的HIRD字段值时访问HIRDMON[3:0]位。这些位反映了
最后收到的LPM令牌的HIRD字段值。

RWEMON位（RWE值监视器）

在监控接收到的LPM令牌的RWE字段值时访问RWEMON位。这些位反映了最后收到的LPM令牌的RWE字段值
。

33.2.47 Host L1 Control Register 1 (HL1CTRL1)

Address(es): USBHS.HL1CTRL1 4006 0148h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	L1STATUS[1:0]		L1REQ
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	0	0	0

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b0	L1REQ	L1 Transition Request	Set this bit to 1 when requesting a transition to the L1 state. This bit is cleared to 0 by the hardware when the LPM transaction is complete.	R/W
b2, b1	L1STATUS[1:0]	L1 Request Completion Status	Indicates the result of the LPM transaction made by the L1REQ bit: b2 b1 0 0: ACK received 0 1: NYET received 1 0: STALL received 1 1: Transaction error.	R
b15 to b3	—	Reserved	The read value is undefined. The write value should be 0.	R/W

L1REQ bit (L1 Transition Request)

Set the L1REQ bit to 1 to transition to the L1 state. When the USBHS detects that this bit is 1, it starts the LPM transaction. The USBHS clears this bit to 0 through hardware on completion of the transaction.

L1STATUS[1:0] bits (L1 Request Completion Status)

The L1STATUS[1:0] bits indicate the result of the LPM transaction initiated by the L1REQ bit.

33.2.48 Host L1 Control Register 2 (HL1CTRL2)

Address(es): USBHS.HL1CTRL2 4006 014Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BESL	—	—	L1RWE	HIRD[3:0]				—	—	—	—	L1ADDR[3:0]			
Value after reset:	0	x	x	0	0	0	0	0	x	x	x	x	0	0	0	0

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b3 to b0	L1ADDR[3:0]	LPM Token DeviceAddress	Specify the value to be set in the ADDR field of the LPM token	R/W
b7 to b4	—	Reserved	The read value is undefined. The write value should be 0.	R/W
b11 to b8	HIRD[3:0]	LPM Token HIRD	Specify the value to be set in the HIRD field of the LPM token	R/W
b12	L1RWE	LPM Token L1 RemoteWake Enable	Specify the value to be set in the RWE field of the LPM token	R/W
b14, b13	—	Reserved	The read value is undefined. The write value should be 0.	R/W
b15	BESL	BESL & Alternate HIRD	Selects the K-State drive period on L1 Resume	R/W

L1ADDR[3:0] bits (LPM Token DeviceAddress)

The L1ADDR[3:0] bits specify the value to be set in the ADDR field of the LPM token that the USBHS transmits when the HL1CTRL1.L1REQ bit is set to 1.

33.2.47 主机L1控制寄存器1(HL1CTRL1)

Address(es): USBHS.HL1CTRL1 4006 0148h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	L1STATUS[1:0]		L1REQ
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	0	0	0

x: Undefined

Bit	Symbol	位名称	Description	R/W
b0	L1REQ	L1转换请求	当请求转换到L1状态时，将此位设置为1。当LPM事务完成时，该位由硬件清零。	R/W
b2, b1	L1STATUS[1:0]	L1请求完成状态	指示L1REQ位进行的LPM事务的结果：b2b1 0 0：收到ACK 0 1：收到NYET 1 0：收到STALL 1 1：交易错误。	R
b15 to b3	—	Reserved	读取值未定义。写入值应为0。	R/W

L1REQ位（L1转换请求）

将L1REQ位设置为1以转换到L1状态。当USBHS检测到该位为1时，它启动LPM事务。USBHS在事务完成时通过硬件将该位清零。

L1STATUS[1:0]位（L1请求完成状态）

L1STATUS[1:0]位指示L1REQ位启动的LPM事务的结果。

33.2.48 主机L1控制寄存器2(HL1CTRL2)

Address(es): USBHS.HL1CTRL2 4006 014Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BESL	—	—	L1RWE	HIRD[3:0]				—	—	—	—	L1ADDR[3:0]			
重置后的值：	0	x	x	0	0	0	0	0	x	x	x	x	0	0	0	0

x: Undefined

Bit	Symbol	位名称	Description	R/W
b3 to b0	L1ADDR[3:0]	LPM Token DeviceAddress	指定要在LPM令牌的ADDR字段中设置的值	R/W
b7 to b4	—	Reserved	读取值未定义。写入值应为0。	R/W
b11 to b8	HIRD[3:0]	LPM Token HIRD	指定要在LPM令牌的HIRD字段中设置的值	R/W
b12	L1RWE	LPM Token L1 RemoteWake Enable	指定要在LPM令牌的RWE字段中设置的值	R/W
b14, b13	—	Reserved	读取值未定义。写入值应为0。	R/W
b15	BESL	BESL & Alternate HIRD	在L1Resume上选择K-State驱动周期	R/W

L1ADDR[3:0]位（LPM令牌设备地址）

L1ADDR[3:0]位指定在HL1CTRL1.L1REQ位设置为1时USBHS发送的LPM令牌的ADDR字段中设置的值。

HIRD[3:0] bits (LPM Token HIRD)

The HIRD[3:0] bits specify the value to be set in the HIRD field of the LPM token that the USBHS transmits when the HL1CTRL1.L1REQ bit is set to 1. Table 33.15 shows the relationship between the HIRD settings and the HIRD field values.

Table 33.15 Relationship between the HIRD bit settings and the HIRD field values

HIRD[3:0] setting	When BESL = 0	When BESL = 1
0000b	50 µs (setting prohibited)	75 µs
0001b	125 µs	100 µs
0010b	200 µs	150 µs
0011b	275 µs	250 µs
0100b	350 µs	350 µs
0101b	425 µs	450 µs
0110b	500 µs	950 µs
0111b	575 µs	1950 µs
1000b	650 µs	2950 µs
1001b	725 µs	3950 µs
1010b	800 µs	4950 µs
1011b	875 µs	5950 µs
1100b	950 µs	6950 µs
1101b	1025 µs (setting prohibited)	7950 µs
1110b	1100 µs (setting prohibited)	8950 µs
1111b	1175 µs (setting prohibited)	9950 µs

Note: The set value of the HIRD bit is used for the host K drive period on host resume and for the host K period on remote wakeup.

L1RWE bit (LPM Token L1 RemoteWake Enable)

The L1RWE bit specifies the value to be set in the RWE field of the LPM token that the USBHS transmits when the HL1CTRL1.L1REQ bit is set to 1.

The USBHS does not control detection of the remote wakeup signal in the L1 state with this bit. The remote wakeup signal is controlled by the DVSTCTR0.RWUPE bit, as with Suspend.

BESL bit (BESL & Alternate HIRD)

The BESL bit selects the K-state drive period on L1 Resume. For details, see the description of the HIRD bits.

HIRD[3:0]位（LPM令牌HIRD）

HIRD[3:0]位指定要在USBHS发送的LPM令牌的HIRD字段中设置的值。
HL1CTRL1.L1REQ位设置为1。表33.15显示了HIRD设置和HIRD字段值之间的关系。

Table 33.15 HIRD位设置和HIRD字段值之间的关系

HIRD[3:0] setting	When BESL = 0	When BESL = 1
0000b	50 µs (setting prohibited)	75 µs
0001b	125 µs	100 µs
0010b	200 µs	150 µs
0011b	275 µs	250 µs
0100b	350 µs	350 µs
0101b	425 µs	450 µs
0110b	500 µs	950 µs
0111b	575 µs	1950 µs
1000b	650 µs	2950 µs
1001b	725 µs	3950 µs
1010b	800 µs	4950 µs
1011b	875 µs	5950 µs
1100b	950 µs	6950 µs
1101b	1025 µs (setting prohibited)	7950 µs
1110b	1100 µs (setting prohibited)	8950 µs
1111b	1175 µs (setting prohibited)	9950 µs

Note: HIRD位的设置值用于主机恢复时的主机K驱动周期和远程唤醒时的主机K周期。

L1RWE位（LPM令牌L1远程唤醒启用）

L1RWE位指定在USBHS发送的LPM令牌的RWE字段中设置的值。
HL1CTRL1.L1REQ位设置为1。

USBHS不通过该位控制L1状态下远程唤醒信号的检测。远程唤醒信号由DVSTCTR0.RWUPE位控制，与挂起一样。

BESL位（BESL和备用HIRD）

BESL位选择L1Resume上的K状态驱动周期。有关详细信息，请参见HIRD位的说明。

33.2.49 Deep Software Standby USB Transceiver Control/Pin Monitor Register (DPUSR0R)

Address(es): USBHS.DPUSR0R 4006 0160h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	DVBSTSHM	—	DOVCBHM	DOVCAHM	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	x	0	x	x	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b19 to b0	—	Reserved	These bits are read as 0	R
b20	DOVCAHM	OVRCURA Input Flag	Indicates OVRCURA input signal on the USBHS side	R
b21	DOVCBHM	OVRCURB Input Flag	Indicates OVRCURB input signal on the USBHS side	R
b22	—	Reserved	This bit is read as 0	R
b23	DVBSTSHM	VBUS Input Flag	Indicates VBUS input signal on the USBHS side	R
b31 to b24	—	Reserved	These bits are read as 0	R

33.2.50 Deep Software Standby USB Suspend/Resume Interrupt Register (DPUSR1R)

Address(es): USBHS.DPUSR1R 4006 0164h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	DVBSTSH	—	DOVCBH	DOVCAH	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	DVBSTSHE	—	DOVCBHE	DOVCAHE	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	DOVCAHE	OVRCURA Interrupt Enable Clear	0: Disable recovery from Deep Software Standby mode 1: Enable recovery from Deep Software Standby mode.	R/W
b5	DOVCBHE	OVRCURB Interrupt Enable Clear	0: Disable recovery from Deep Software Standby mode 1: Enable recovery from Deep Software Standby mode.	R/W
b6	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b7	DVBSTSHE	VBUS Interrupt Enable/Clear	0: Disable recovery from Deep Software Standby mode 1: Enable recovery from Deep Software Standby mode.	R/W
b19 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b20	DOVCAH	OVRCURA Interrupt Source Return Status Flag	0: System has not recovered from Deep Software Standby mode 1: System recovered from Deep Software Standby mode.	R
b21	DOVCBH	OVRCURB Interrupt Source Return Status Flag	0: System has not recovered from Deep Software Standby mode 1: System recovered from Deep Software Standby mode.	R

33.2.49 深度软件待机USB收发器控制引脚监控寄存器(DPUSR0R)

Address(es): USBHS.DPUSR0R 4006 0160h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	DVBSTSHM	—	DOVCBHM	DOVCAHM	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	x	0	x	x	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

x: Undefined

Bit	Symbol	位名称	Description	R/W
b19 to b0	—	Reserved	这些位被读为0	R
b20	DOVCAHM	OVRCURA输入标志	指示USBHS侧的OVRCURA输入信号	R
b21	DOVCBHM	OVRCURB输入标志	指示USBHS侧的OVRCURB输入信号	R
b22	—	Reserved	该位读为0	R
b23	DVBSTSHM	VBUS输入标志	指示USBHS侧的VBUS输入信号	R
b31 to b24	—	Reserved	这些位被读为0	R

33.2.50 深度软件待机USB挂起恢复中断寄存器(DPUSR1R)

Address(es): USBHS.DPUSR1R 4006 0164h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	DVBSTSH	—	DOVCBH	DOVCAH	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	DVBSTSHE	—	DOVCBHE	DOVCAHE	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b3 to b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b4	DOVCAHE	OVRCURA中断使能 Clear	0：禁用从深度软件待机模式恢复1：启用从深度软件待机模式恢复。	R/W
b5	DOVCBHE	OVRCURB中断使能 Clear	0：禁用从深度软件待机模式恢复1：启用从深度软件待机模式恢复。	R/W
b6	—	Reserved	该位读取为0。写入值应为0。	R/W
b7	DVBSTSHE	VBUS Interrupt Enable/Clear	0：禁用从深度软件待机模式恢复1：启用从深度软件待机模式恢复。	R/W
b19 to b8	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b20	DOVCAH	OVRCURA中断源返回状态标志	0：系统尚未从深度软件待机模式恢复1：系统从深度软件待机模式恢复。	R
b21	DOVCBH	OVRCURB中断源返回状态标志	0：系统尚未从深度软件待机模式恢复1：系统从深度软件待机模式恢复。	R

Bit	Symbol	Bit name	Description	R/W
b22	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b23	DVBSTSH	VBUS Interrupt Source Return Status Flag	0: System has not recovered from Deep Software Standby mode 1: System recovered from Deep Software Standby mode.	R
b31 to b24	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

33.2.51 Deep Software Standby USB Suspend/Resume Interrupt Register (DPUSR2R)

Address(es): USBHS.DPUSR2R 4006 0168h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	DMINTE	DPINTE	—	—	DMVAL	DPVAL	—	—	DMINT	DPINT
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	DPINT	Indication of Return from DP Interrupt Source	0: System has not recovered from Deep Software Standby mode 1: System recovered from Deep Software Standby mode.	R
b1	DMINT	Indication of Return from DM Interrupt Source	0: System has not recovered from Deep Software Standby mode 1: System recovered from Deep Software Standby mode.	R
b3, b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	DPVAL	DP Input	Indicates DP input signal on the USBHS side	R
b5	DMVAL	DM Input	Indicates DM input signal on the USBHS side	R
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	DPINTE	DP Interrupt Enable Clear	0: Disable recovery from Deep Software Standby mode 1: Enable recovery from Deep Software Standby mode.	R/W
b9	DMINTE	DM Interrupt Enable Clear	0: Disable recovery from Deep Software Standby mode 1: Enable recovery from Deep Software Standby mode.	R/W
b15 to b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

33.2.52 Deep Software Standby USB Suspend/Resume Command Register (DPUSRCR)

Address(es): USBHS.DPUSRCR 4006 016Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FIXPHYPD	FIXPHY
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	FIXPHY	USB Transceiver Control Fix	0: Normal mode 1: Invoke/recover from Deep Software Standby mode.	R/W
b1	FIXPHYPD	USB Transceiver Control Fix for PLL	0: Normal mode 1: Invoke/recover from Deep Software Standby mode.	R/W
b15 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Bit	Symbol	位名称	Description	R/W
b22	—	Reserved	该位读取为0。写入值应为0。	R/W
b23	DVBSTSH	VBUS中断源返回状态标志	0：系统尚未从深度软件待机模式恢复1：系统从深度软件待机模式恢复。	R
b31 to b24	—	Reserved	这些位被读取为0。写入值应为0。	R/W

33.2.51 深度软件待机USB挂起恢复中断寄存器(DPUSR2R)

Address(es): USBHS.DPUSR2R 4006 0168h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	DMINTE	DPINTE	—	—	DMVAL	DPVAL	—	—	DMINT	DPINT
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	DPINT	从DP返回的指示中断源	0：系统尚未从深度软件待机模式恢复1：系统从深度软件待机模式恢复。	R
b1	DMINT	从DM返回的指示中断源	0：系统尚未从深度软件待机模式恢复1：系统从深度软件待机模式恢复。	R
b3, b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b4	DPVAL	DP Input	指示USBHS侧的DP输入信号	R
b5	DMVAL	DM Input	指示USBHS侧的DM输入信号	R
b7, b6	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b8	DPINTE	DP中断使能清除	0：禁用从深度软件待机模式恢复1：启用从深度软件待机模式恢复。	R/W
b9	DMINTE	DM中断使能清除	0：禁用从深度软件待机模式恢复1：启用从深度软件待机模式恢复。	R/W
b15 to b10	—	Reserved	这些位被读取为0。写入值应为0。	R/W

33.2.52 深度软件待机USB挂起恢复命令寄存器(DPUSRCR)

Address(es): USBHS.DPUSRCR 4006 016Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FIXPHYPD	FIXPHY
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	FIXPHY	USB收发器控制修复	0：正常模式1：调用从深度软件待机模式恢复。	R/W
b1	FIXPHYPD	USB收发器控制修复PLL	0：正常模式1：调用从深度软件待机模式恢复。	R/W
b15 to b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W

33.3 Operation

33.3.1 System Control

This section describes register settings required for initializing the USBHS and controlling power consumption.

33.3.1.1 Setting data to the USBHS registers

Setting the SYSCFG.USBE bit to 1 after starting the PHY clock supply enables and starts USBHS operation. For information on how to supply the PHY clock, see section 33.3.3, Supplying the Clock.

33.3.1.2 Selecting the controller function

The USBHS can operate as a host or device controller.

Use the SYSCFG.DCFM bit to select one of these USBHS functions. The DCFM bit must be changed in the initial settings immediately after a reset or in the D+ pull-up-disabled state (SYSCFG.DPRPU bit = 0) and D+ and D- pull-down-disabled state (SYSCFG.DRPD bit = 0).

33.3.2 Controlling the USB data bus using resistors

The USBHS provides pull-up and pull-down resistors for the D+ and D- lines. Pull these lines up or down by setting the SYSCFG.DPRPU and DRPD bits.

In device controller mode, confirm that connection to the USB host is made, and then set the SYSCFG.DPRPU bit to 1 and pull up the D+ line (in full-speed communication).

When the SYSCFG.DPRPU bit is set to 0 during communication with a PC, the USBHS disables the pull-up resistor for the USB data line, thereby notifying the USB host of disconnection.

In host controller mode, set the SYSCFG.DRPD bit to 1 to pull down the D+ and D- lines.

Table 33.16 shows the settings for controlling the resistors for the USB data bus. Control the USB data bus appropriately for your system using the DRPD and DPRPU bit settings.

Table 33.16 Control settings for the USB data bus resistors (excluding OTG operation)

SYSCFG register settings		USB data bus control		
DRPD bit	**DPRPU bit**	**D-Line**	**D+Line**	**Function**
0	0	Open	Open	When resistors not used
0	1	Open	Pull-Up	When operating as a device controller at full-speed
1	0	Pull-Down	Pull-Down	When operating as a host controller
1	1	—	—	Setting prohibited except during OTG operation

33.3.3 Supplying the Clock

Table 33.17 shows the two input clocks required for the USBHS.

Table 33.17 Input clocks

Input clock name	Description
PCLKA	Peripheral module clock A input. There is no constraint on the frequency of the PCLKA input.
PHY clock	PHY clock generated from external input or internal supply • External input: The clock is generated by the USB-PHY internal PLL based on a 12-MHz, 20-MHz, or 24-MHz clock supplied to the EXTAL pin from outside the MCU. For the external clock specifications, especially the jitter characteristics, strictly follow the specifications of ±50 ppm. • Internal supply: The clock is generated by supplying 48 MHz and 60 MHz to the USB-PHY module and selecting CL-only mode (PHYSET.HSEB). High-speed operation is not supported with this mode.

33.3 Operation

33.3.1 系统控制

本节介绍初始化USBHS和控制功耗所需的寄存器设置。

33.3.1.1 将数据设置到USBHS寄存器

启动PHY时钟电源后将SYSCFG.USBE位设置为1使能并启动USBHS操作。有关如何提供PHY时钟的信息，请参阅第33.3.3节，提供时钟。

33.3.1.2 选择控制器功能

USBHS可以作为主机或设备控制器运行。

使用SYSCFG.DCFM位选择这些USBHS功能之一。DCFM位必须在复位后立即更改为初始设置或在D+上拉禁用状态（SYSCFG.DPRPU位=0）和D+和Dpulldown禁用状态（SYSCFG.DRPD位=0）。

33.3.2 使用电阻控制USB数据总线

USBHS为D+和Dlines提供上拉和下拉电阻。通过设置SYSCFG.DPRPU和DRPD位。

在设备控制器模式下，确认与USB主机的连接已建立，然后将SYSCFG.DPRPU位设置为1并拉高D+线（全速通信）。

当SYSCFG.DPRPU位在与PC通信期间设置为0时，USBHS禁用USB数据线的上拉电阻，从而通知USB主机断开连接。

在主机控制器模式下，将SYSCFG.DRPD位设置为1以拉低D+和Dlines。

表33.16显示了用于控制USB数据总线电阻器的设置。使用DRPD和DPRPU位设置为您的系统适当控制USB数据总线。

Table 33.16 USB数据总线电阻的控制设置（不包括OTG操作）

SYSCFG寄存器设置		USB数据总线控制		
DRPD bit	**DPRPU bit**	**D-Line**	**D+Line**	**Function**
0	0	Open	Open	不使用电阻时
0	1	Open	Pull-Up	作为设备控制器全速运行时
1	0	Pull-Down	Pull-Down	作为主机控制器运行时
1	1	—	—	除OTG操作期间禁止设置

33.3.3 提供时钟

表33.17显示了USBHS所需的两个输入时钟。

Table 33.17 输入时钟

输入时钟名称	Description
PCLKA	外设模块时钟A输入。 PCLKA输入的频率没有限制。
PHY clock	从外部输入或内部电源生成的PHY时钟外部输入： 时钟由USB-PHY内部PLL基于从MCU外部提供给EXTAL引脚的12-MHz、20-MHz或24-MHz时钟生成。对于外部时钟规范，尤其是抖动特性，严格遵循±50ppm的规范。 内部供应： 通过向USB-PHY模块提供48MHz和60MHz并选择仅CL模式(PHYSET.HSEB)。此模式不支持高速操作。

Figure 33.2 illustrates the PHY clock settings.

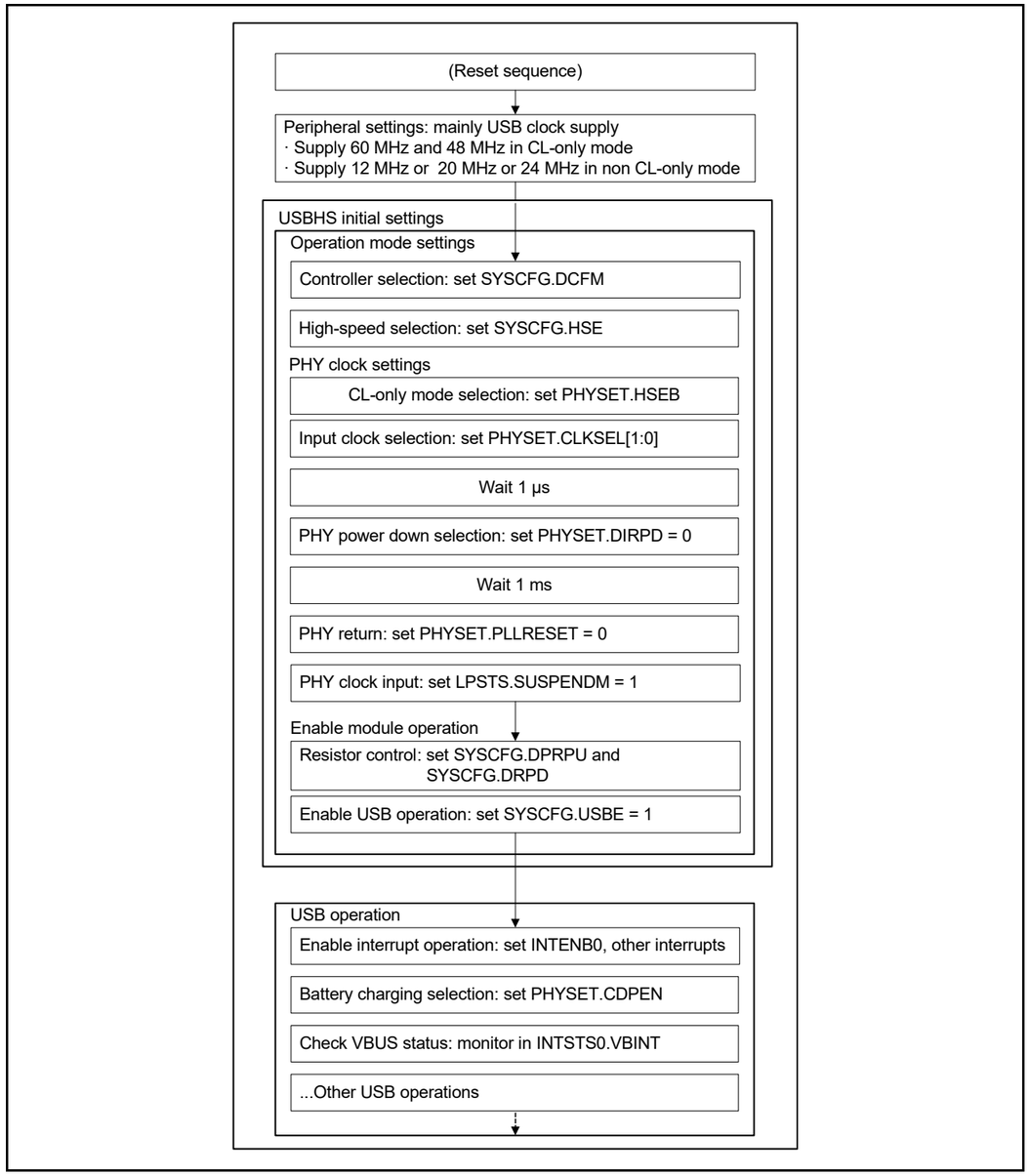


Figure 33.2 PHY clock settings

33.3.4 Constraints on Stopping the Clock

PCLKA and PHY clock can be stopped during disconnection or suspension. However, to stop any of these clocks while the USB is suspended in device controller mode, the stopped clock must be resupplied using the resume interrupt. The PHY clock must be resupplied within 5.5 ms after the resume interrupt is generated.

图33.2说明了PHY时钟设置。

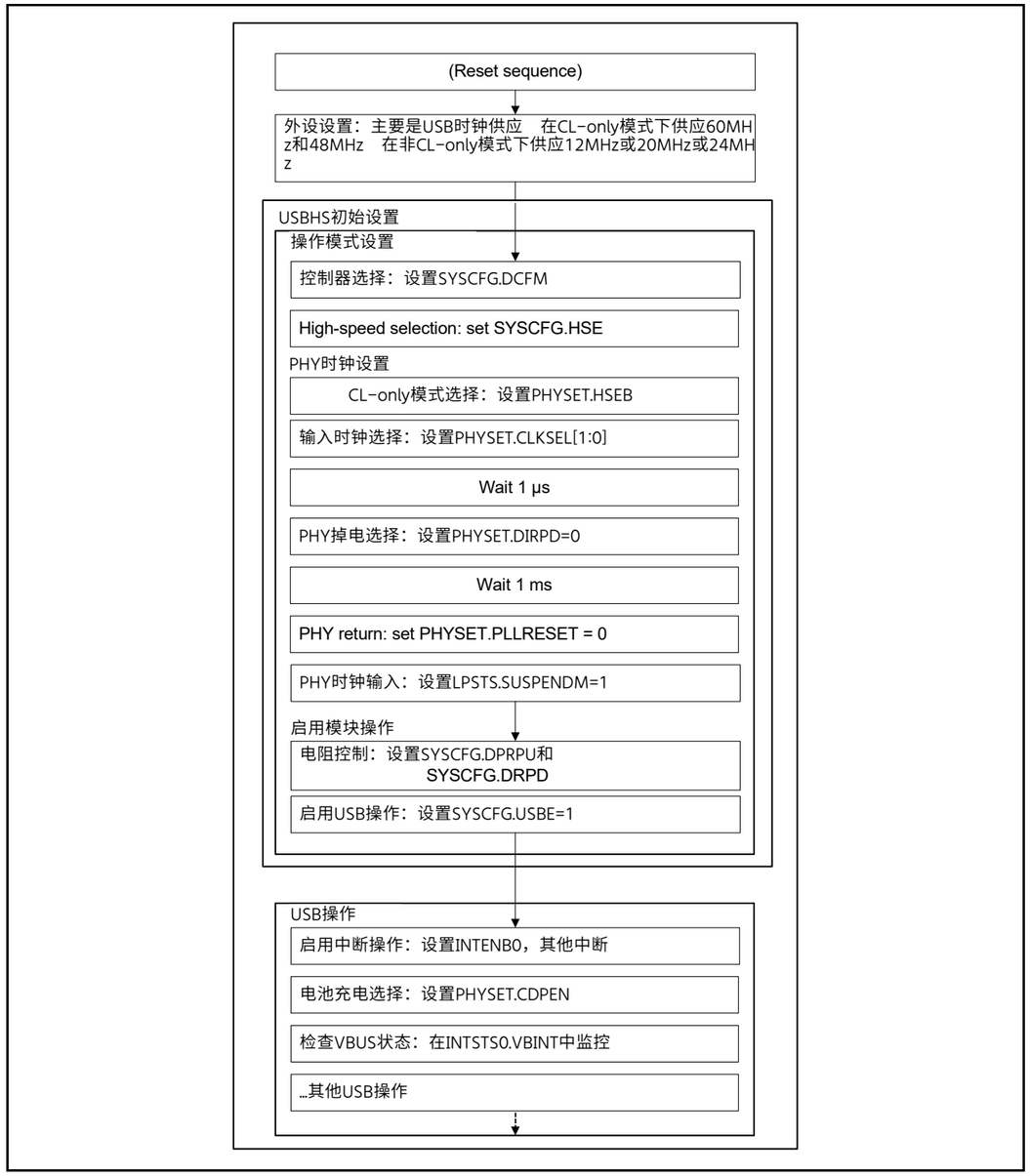


Figure 33.2 PHY时钟设置

33.3.4 停止时钟的限制

PCLKA和PHY时钟可以在断开或挂起期间停止。但是，要在USB在设备控制器模式下暂停时停止任何这些时钟，必须使用恢复中断重新提供停止的时钟。PHY时钟必须在产生恢复中断后的5.5ms内重新提供。

33.3.5 Interrupts

Table 33.18 lists the interrupt sources in the USBHS. When an interrupt generation condition is satisfied and the interrupt output is enabled using the associated interrupt enable register, the USBHS issues a USBHS interrupt request to the Interrupt Controller Unit (ICU) and a USBHS interrupt is generated.

Table 33.18 Interrupt sources (1 of 2)

Flag to be set to 1	Interrupt name	Interrupt source	Applicable controller function	Status flag
VBINT	VBUS interrupt	• A change in the state of the USB_VBUS input pin is detected (low to high or high to low)	Host or function*1	INTSTS0.VBSTS
RESM	Resume interrupt	• A change in the state of the USB bus is detected in the Suspend state (J-state to K-state or J-state to SE0)	Function	—
SOFR	Frame number update interrupt	In host controller mode: • An SOF packet with a different frame number is transmitted In device controller mode: • When SOFRM is 0: An SOF packet with a different frame number is received • When SOFRM is 1: Failed to receive an SOF packet with the µ frame number 0 because the packet is corrupted.	Host or function	—
DVST	Device state transition interrupt	• A device state transition is detected because of one of the following: - USB bus reset is detected - Suspend state is detected - SET_ADDRESS request is received - SET_CONFIGURATION request is received.	Function	PL1CTRL.DVSQ[3:0]
CTRT	Control transfer stage transition interrupt	• A control transfer stage transition is detected because of one of the following: - Setup stage completed - Control write transfer status stage transition occurred - Control read transfer status stage transition occurred - Control transfer completed - Control transfer sequence error occurred	Function	INTSTS0.CTSQ[2:0]
BEMP	Buffer empty interrupt	• The buffer is empty after all FIFO buffer data is transmitted • A packet larger than the maximum packet size is received	Host or function	BEMPSTS.PIPEBEMP
NRDY	Buffer not ready interrupt	In host controller mode: • A STALL response is received from the peripheral device in response to the issued token • The response from the peripheral device in response to the issued token is not received successfully (no response three times consecutively or packet reception error three times consecutively) • An overrun or underrun error occurred during isochronous transfer In device controller mode: • NAK is returned for an IN or OUT token while the PID[1:0] bits were set to 01b (BUF) • A CRC error or bit stuffing error occurred during data reception in isochronous transfer • An interval error occurred during data reception in isochronous transfer	Host or function	NRDYSTS.PIPENRDY
BRDY	Buffer ready interrupt	• The buffer is ready (read or write state)	Host or function	BRDYSTS.PIPEBRDY

33.3.5 Interrupts

表33.18列出了USBHS中的中断源。当满足中断产生条件并使用相关的中断使能寄存器使能中断输出时，USBHS向中断控制器单元(ICU)发出USBHS中断请求，并产生USBHS中断。

Table 33.18 中断源(1of2)

标志设置为1	中断名称	中断源	适用控制器功能	状态标志
VBINT	VBUS interrupt	检测到USB_VBUS输入引脚的状态变化（从低到高或从高到低）	主机或功能*1	INTSTS0.VBSTS
RESM	恢复中断	在Suspend状态下检测到USB总线状态的变化（J-state到K-state或J-state到SE0）	Function	—
SOFR	帧号更新中断	在主机控制器模式下： 发送具有不同帧号的SOF数据包在设备控制器模式下： 当SOFRM为0时：接收到具有不同帧号的SOF数据包 当SOFRM为1时：未能接收到具有不同帧号的SOF数据包µ帧编号为0，因为数据包已损坏。	主机或功能	—
DVST	设备状态转换中断	由于以下原因之一检测到设备状态转换：检测到USB总线复位检测到挂起状态收到SET_ADDRESS请求收到SET_CONFIGURATION请求。	Function	PL1CTRL.DVSQ[3:0]
CTRT	控制转移阶段转换中断	由于以下原因之一检测到控制传输阶段转换：设置阶段完成发生控制写入传输状态阶段转换发生控制读取传输状态阶段转换控制传输完成发生控制传输序列错误	Function	INTSTS0.CTSQ[2:0]
BEMP	缓冲区空中断	发送完所有FIFO缓冲区数据后，缓冲区为空 接收大于最大数据包大小的数据包	主机或功能	BEMPSTS.PIPEBEMP
NRDY	缓冲区未就绪中断	在主机控制器模式下： 从外围设备接收到一个STALL响应以响应发出的令牌 从外围设备响应于发出的令牌的响应未成功接收（连续3次无响应或3次数据包接收错误 同步传输期间发生溢出或欠载错误在设备控制器模式下： 当PID[1:0]位设置为01b(BUF)时，为IN或OUT令牌返回NAK CRC错误或位填充同步传输中的数据接收期间发生错误 同步传输中的数据接收期间发生间隔错误	主机或功能	NRDYSTS.PIPENRDY
BRDY	缓冲区就绪中断	缓冲区准备就绪（读或写状态）	主机或功能	BRDYSTS.PIPEBRDY

Table 33.18 Interrupt sources (2 of 2)

Flag to be set to 1	Interrupt name	Interrupt source	Applicable controller function	Status flag
OVRCR	Overcurrent input change interrupt	• USBHS_OVRCR0A pin or USBHS_OVRCR0B pin state change is detected (low to high or high to low)	Host or function	SYSSTS0.OVCMON[1:0]
BCHG	Bus change interrupt	• USB bus state change is detected	Host	—
DTCH	Device disconnect detection interrupt	• Peripheral device disconnect is detected	Host	—
ATTCH	Device connect detection interrupt	• J-state or K-state is detected on the USB bus for 2.5 µs continuously This interrupt can be used to check whether peripheral devices are connected.	Host	—
EOFERR	EOF error detection interrupt	• An EOF error is detected for a peripheral device	Host	—
SACK	Setup normal interrupt	• A setup transaction normal response (ACK) is received	Host	—
SIGN	Setup error interrupt	• A setup transaction error (no response or ACK packet corruption) is detected three consecutive times	Host	—
PDDETINT	PDDETSTS change detect interrupt	• PDDET pin change is detected	Host or function	BCCTRL.PDDETSTS
LPMEND	LPM transaction end interrupt	• LPM transaction is complete	Host	PL1CTRL.DVSQ[3:0]
L1RSMEND	L1 resume end interrupt	• Resume (from L1 state) processing is complete	Host	PL1CTRL.DVSQ[3:0]

Note 1. Although this interrupt can be generated in host controller mode, it is not usually used in this mode.

33.3.5.1 Selecting the USBHS interrupt detection method

Table 33.19 shows operations for an USBHS interrupt output from the USBHS. In case two or more interrupt sources are generated, the USBHS interrupt output method can be set in the SOFCFG.INTL bit. Set the USBHS interrupt output operation based on your system.

Table 33.19 USBHS interrupt operation

USBHS interrupt output (INTL setting)	When one interrupt source is generated	When two or more interrupt sources are generated
Edge detection (SOFCFG.INTL bit = 0)	Low level output until the source is cleared	When one source is cleared, the USBHS interrupt is negated for 32 clocks at 48 MHz (high pulse output)
Level detection (SOFCFG.INTL bit = 1)	Low level output until the source is cleared	Low level output until all sources are cleared

Table 33.18 中断源（2个中的2个）

标志设置为1	中断名称	中断源	适用控制器功能	状态标志
OVRCR	过流输入变化中断	检测到USBHS_OVRCR0A引脚或USBHS_OVRCR0B引脚状态变化（低到高或高到低）	主机或功能	SYSSTS0.OVCMON[1:0]
BCHG	总线变化中断	检测到USB总线状态变化	Host	—
DTCH	设备断开检测中断	检测到外围设备断开连接	Host	—
ATTCH	设备连接检测中断	在USB总线上连续检测到J-state或K-state2.5µs此中断可用于检查外围设备是否已连接。	Host	—
EOFERR	EOF错误检测中断	检测到外围设备的EOF错误	Host	—
SACK	设置正常中断	收到设置事务正常响应(ACK)	Host	—
SIGN	设置错误中断	连续3次检测到设置事务错误（无响应或ACK数据包损坏）	Host	—
PDDETINT	PDDETSTS变化检测中断	检测到PDDET引脚变化	主机或功能	BCCTRL.PDDETSTS
LPMEND	LPM事务结束中断	LPM交易完成	Host	PL1CTRL.DVSQ[3:0]
L1RSMEND	L1恢复结束中断	恢复（从L1状态）处理完成	Host	PL1CTRL.DVSQ[3:0]

Note 1. 虽然在主机控制器模式下可以产生此中断，但通常不会在此模式下使用。

33.3.5.1 选择USBHS中断检测方法

表33.19显示了来自USBHS的USBHS中断输出的操作。如果产生两个或更多中断源，USBHS中断输出方法可以在SOFCFG.INTL位中设置。根据您的系统设置USBHS中断输出操作。

Table 33.19 USBHS中断操作

USBHS中断输出（INTL设置）	产生一个中断源时	当产生两个或更多中断源时
边沿检测（SOFCFG.INTL位=0）	低电平输出，直到源清除	当一个源被清除时，USBHS中断在48MHz的32个时钟内被否定（高脉冲输出）
电平检测（SOFCFG.INTL位=1）	低电平输出，直到源清除	低电平输出，直到所有源被清除

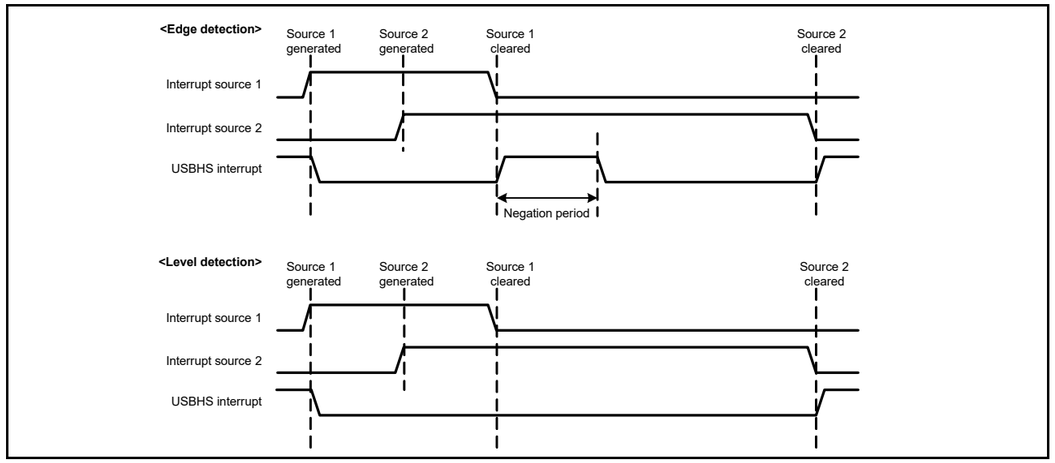


Figure 33.3 USBHS interrupt operation

Figure 33.4 shows an interrupt association chart of the USBHS.

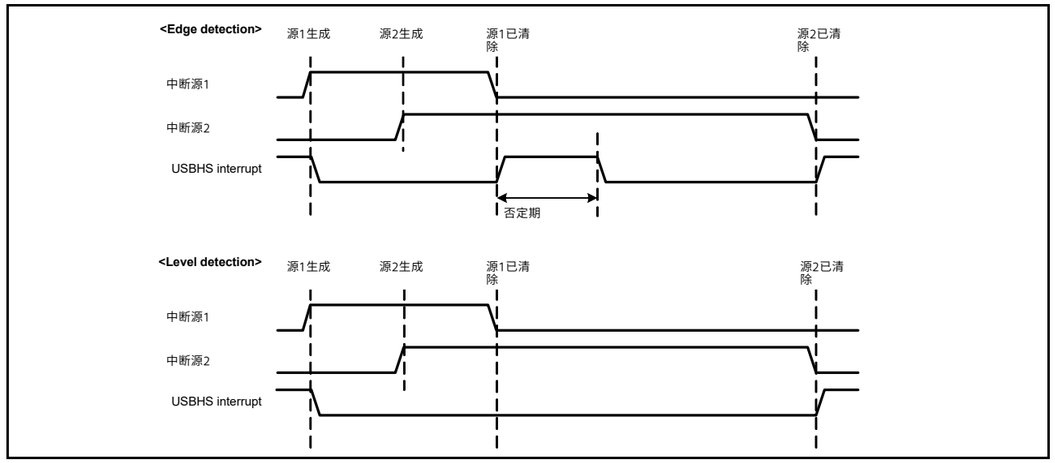


Figure 33.3 USBHS中断操作

图33.4显示了USBHS的中断关联图。

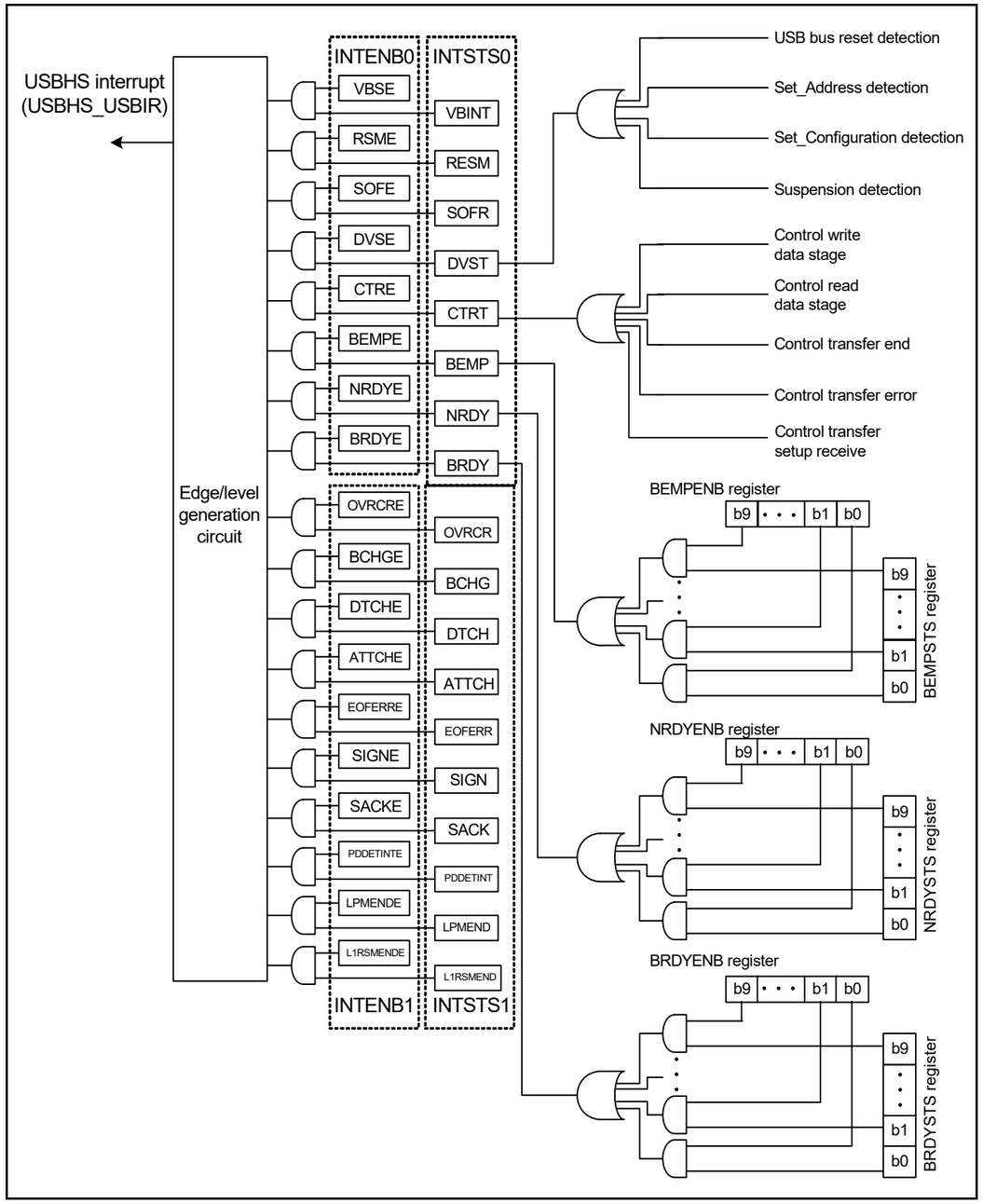


Figure 33.4 USBHS interrupt-related circuits

Table 33.20 shows the interrupts generated by the USBHS.

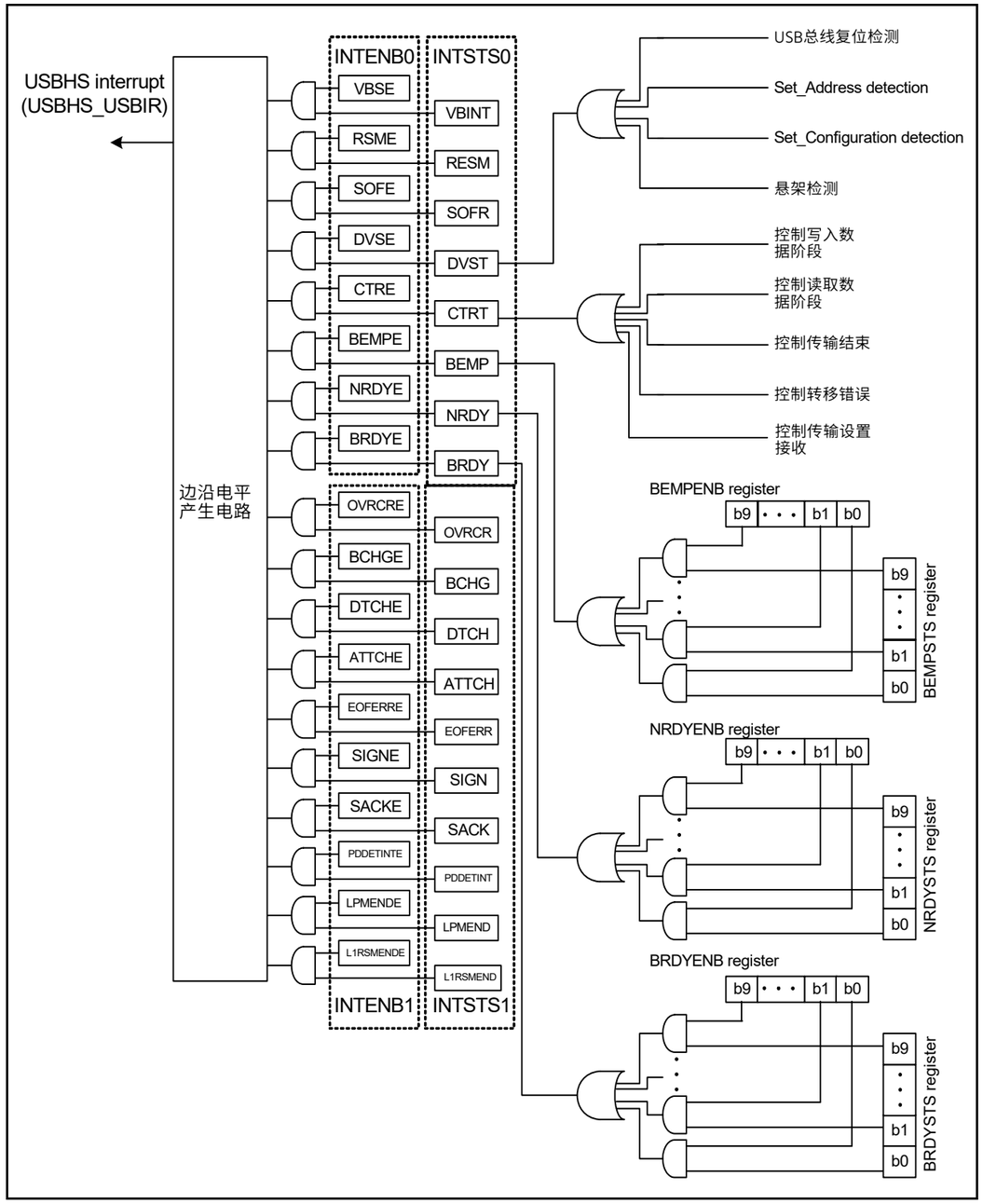


Figure 33.4 USBHS interrupt-related circuits

表33.20显示了USBHS产生的中断。

Table 33.20 USBHS interrupts

Interrupt name	Interrupt status flag	DTC activation	DMAC activation
USBHS_D0FIFO	DMA transfer request 0	Possible	Possible
USBHS_D1FIFO	DMA transfer request 1	Possible	Possible
USBHS_USBIR	VBUS interrupt, resume interrupt, frame number update interrupt, device state transition interrupt, control transfer stage transition interrupt, buffer empty interrupt, buffer not ready interrupt, buffer ready interrupt, overcurrent interrupt, bus change interrupt, device disconnect detection interrupt, device connect detection interrupt, EOF error detection interrupt, normal setup operation interrupt, setup error interrupt, PDDETSTS change detection interrupt, LPM transaction end interrupt, and L1 resume end interrupt	Not possible	Not possible

33.3.6 Interrupt Descriptions

33.3.6.1 BRDY interrupt

The BRDY interrupt is generated in both host and device controller modes. This section describes the conditions in which the USBHS sets the associated bit in BRDYSTS to 1. Under these conditions, the USBHS generates a BRDY interrupt if the software sets the bit in BRDYENB associated with the given pipe to 1 and INTENB0.BRDYE bit to 1.

The conditions for generating and clearing the BRDY interrupt depend on the SOFCFG.BRDYM and PIPECFG.BFRE settings for each pipe as follows:

(1) When SOFCFG.BRDYM = 0 and PIPECFG.BFRE = 0

With these settings, the BRDY interrupt indicates that the FIFO port is accessible.

On any of the following conditions, the USBHS generates an internal BRDY interrupt request trigger and sets the BRDYSTS.PIPEBRDY flag associated with the pipe to 1.

(a) For transmitting pipes

- When the DIR bit is changed from 0 to 1 by software
- When writing by the CPU to the FIFO buffer is disabled for a pipe (when the BSTS flag is read as 0) and the USBHS has completed packet transmission. In continuous transfer, a BRDY interrupt is generated on completion of the transmission of data from one FIFO buffer.
- When one FIFO buffer is empty on completion of writing data to the other FIFO buffer in double buffer mode
- No request trigger is generated until completion of writing data to the currently-written FIFO buffer even if transmission to the other FIFO buffer is complete
- When the hardware flushes the buffer of the pipe for isochronous transfers
- When 1 is written to the PIPEnCTR.ACLRM bit, which causes the FIFO buffer to transition from the write-disabled to write-enabled state.

No request trigger is generated for the DCP, that is, during data transmission for control transfers.

(b) For receiving pipes

- When packet reception is successfully complete, enabling the FIFO buffer to be read while read-access from the CPU to the FIFO buffer for the given pipe is disabled (when the BSTS flag is read as 0). No request trigger is generated for transactions in which DATA-PID mismatch has occurred. In continuous transmission or reception mode, the request trigger is not generated when the data is of the specified maximum packet size and the buffer has available space. When a short packet is received, the request trigger is generated even if the FIFO buffer has available space. When the transaction counter is used, the request trigger is generated on receiving the specified number of packets. In this case, the request trigger is generated even if the FIFO buffer has available space.
- When one FIFO buffer is read-enabled on completion of reading data from the other FIFO buffer in double buffer mode. No request trigger is generated until completion of reading data from the currently-read FIFO buffer, even if reception by the other FIFO buffer is complete.

Table 33.20 USBHS interrupts

中断名称	中断状态标志	DTC activation	DMAC activation
USBHS_D0FIFO	DMA传输请求0	Possible	Possible
USBHS_D1FIFO	DMA传输请求1	Possible	Possible
USBHS_USBIR	VBUS中断、恢复中断、帧号更新中断、设备状态转换中断、控制传输阶段转换中断、缓冲区空中断、缓冲区未就绪中断、缓冲区就绪中断、过流中断、总线改变中断、设备断开检测中断、设备连接检测中断、EOF错误检测中断、正常设置操作中断、设置错误中断、PDDETSTS更改检测中断、LPM事务结束中断和L1恢复结束中断	不可能	不可能

33.3.6 中断说明

33.3.6.1 BRDY interrupt

在主机和设备控制器模式下都会产生BRDY中断。本节介绍USBHS将BRDYSTS中的相关位设置为1的条件。在这些条件下，如果软件将与给定管道相关的BRDYENB中的位设置为1，并且将INTENB0.BRDYE位设置为1，USBHS将生成BRDY中断.

产生和清除BRDY中断的条件取决于每个管道的SOFCFG.BRDYM和PIPECFG.BFRE设置，如下所示：

(1) 当SOFCFG.BRDYM=0且PIPECFG.BFRE=0时

通过这些设置，BRDY中断指示FIFO端口可访问。

在以下任何一种情况下，USBHS产生一个内部BRDY中断请求触发并设置与管道关联的BRDYSTS.PIPEBRDY标志为1。

(a) 用于传输管道

- 当DIR位由软件从0变为1时
- 当CPU对FIFO缓冲区的写入被禁用时（当BSTS标志被读取为0时）并且USBHS已完成数据包传输。在连续传输中，一个FIFO缓冲区的数据传输完成时会产生一个BRDY中断。
- 双缓冲模式下，当一个FIFO缓冲区在完成向另一个FIFO缓冲区写入数据时为空时
- 直到完成向当前写入的FIFO缓冲区写入数据之前，不会生成请求触发，即使传输到另一个FIFO缓冲区已完成
- 当硬件刷新管道缓冲区以进行同步传输时
- 当1写入PIPEnCTR.ACLRM位时，这会导致FIFO缓冲区从写禁止状态转换为写使能状态。

没有为DCP生成请求触发，即在控制传输的数据传输期间。

(b) 用于接收管道

- 当数据包接收成功完成时，允许读取FIFO缓冲区，同时禁用从CPU对给定管道的FIFO缓冲区的读取访问（当BSTS标志被读取为0时）。对于发生DATA-PID不匹配的事务，不会生成请求触发器。在连续发送或接收模式下，当数据达到指定的最大数据包大小且缓冲区有可用空间时，不会生成请求触发。当接收到一个短数据包时，即使FIFO缓冲区有可用空间，也会生成请求触发。当使用事务计数器时，在接收到指定数量的数据包时生成请求触发器。在这种情况下，即使FIFO缓冲区有可用空间，也会生成请求触发。
- 当一个FIFO缓冲区在双缓冲区模式下完成从另一个FIFO缓冲区读取数据后启用读取。在从当前读取的FIFO缓冲区读取数据完成之前，不会生成请求触发，即使其他FIFO缓冲区的接收已完成。

In device controller mode, the BRDY interrupt is not generated in the status stage of control transfers. The PIPEBRDY interrupt status of the selected pipe can be set to 0 by writing 0 to the associated PIPEBRDY flag through the software. In this case, 1s must be written to the associated bits for the other pipes. Clear the BRDY status before accessing the FIFO buffer.

(2) When SOFCFG.BRDYM = 0 and PIPECFG.BFRE = 1

With these settings, the USBHS generates a BRDY interrupt on completion of reading all data for a single transfer using the receiving pipe, and sets the bit in BRDYSTS associated with the pipe to 1.

On any of the following conditions, the USBHS determines that the last data for a single transfer was received:

- When a short packet including a zero-length packet is received
- When the PIPEnTRN register is used and the number of packets specified in the PIPEnTRN.TRNCNT[15:0] bits are completely received.

When the data is completely read after any of these conditions is satisfied, the USBHS determines that all data for a single transfer is completely read.

When a zero-length packet is received while the FIFO buffer is empty, the USBHS determines that all data for a single transfer is completely read when the FRDY flag in the FIFO port control register is 1 and the DTLN[11:0] flags are 0. In this case, to start the next transfer, write 1 to the BCLR bit in the associated port control register through software. With these settings, the USBHS does not detect a BRDY interrupt for the transmitting pipe.

The PIPEBRDY interrupt status of a pipe can be set to 0 by writing 0 to the associated BRDYSTS.PIPEBRDY flag through the software. In this case, 1s must be written to the PIPEBRDY bits for the other pipes.

In this mode, do not change the PIPECFG.BFRE bit setting until all data for a single transfer is processed. When it is necessary to change the PIPECFG.BFRE bit before completion of processing, all FIFO buffers for the pipe must be cleared using the PIPEnCTR.ACLRM bit.

(3) When SOFCFG.BRDYM = 1 and PIPECFG.BFRE = 0

With these settings, the BRDYSTS.PIPEBRDY flag values are linked to the BSTS flag setting for each pipe. In other words, the BRDY interrupt status bits are set to 1 or 0 by the USBHS depending on the FIFO buffer status.

(a) For transmitting pipes

The BRDY interrupt status bits are set to 1 when the FIFO port is ready for write access, and are set to 0 when it is not ready. The BRDY interrupt is not generated for the DCP in the transmitting direction even when it is ready for write access.

(b) For receiving pipes

The BRDY interrupt status bits are set to 1 when the FIFO buffer is ready for read access, and are set to 0 when all data is read (not ready for read access).

When a zero-length packet is received while the FIFO buffer is empty, the associated bit is set to 1 and the BRDY interrupt is continuously generated until the software writes 1 to BCLR. With this setting, the PIPEBRDY flag cannot be set to 0 by software.

When the SOFCFG.BRDYM bit is set to 1, set the PIPECFG.BFRE bit for all pipes to 0, and the SOFCFG.INTL bit to 1 for level detection.

Figure 33.5 shows the timing of BRDY interrupt generation.

在设备控制器模式下，在控制传输的状态阶段不会产生BRDY中断。通过软件将0写入相关的PIPEBRDY标志，可以将所选管道的PIPEBRDY中断状态设置为0。在这种情况下，必须将1写入其他管道的相关位。在访问FIFO缓冲区之前清除BRDY状态。

(2) 当SOFCFG.BRDYM=0且PIPECFG.BFRE=1时

使用这些设置，USBHS在完成使用接收管道读取一次传输的所有数据时生成BRDY中断，并将BRDYSTS中与管道相关的位设置为1。

在以下任何一种情况下，USBHS都会确定接收到单次传输的最后一个数据：

- 当接收到包含零长度数据包的短数据包时
- 当使用PIPEnTRN寄存器并且完全接收到PIPEnTRN.TRNCNT[15:0]位中指定的数据包数量时。

当满足这些条件中的任何一个后数据被完全读取时，USBHS确定单次传输的所有数据都被完全读取。

当FIFO缓冲区为空时接收到零长度数据包时，当FIFO端口控制寄存器中的FRDY标志为1且DTLN[11:0]标志为0.在这种情况下，要开始下一次传输，通过软件向相关端口控制寄存器中的BCLR位写入1。使用这些设置，USBHS不会检测到传输管道的BRDY中断。

通过软件将0写入相关的BRDYSTS.PIPEBRDY标志可以将管道的PIPEBRDY中断状态设置为0。在这种情况下，必须将1写入其他管道的PIPEBRDY位。

在此模式下，在处理完单次传输的所有数据之前，不要更改PIPECFG.BFRE位设置。当需要在处理完成之前更改PIPECFG.BFRE位时，必须使用PIPEnCTR.ACLRM位清除管道的所有FIFO缓冲区。

(3) 当SOFCFG.BRDYM=1且PIPECFG.BFRE=0时

通过这些设置，BRDYSTS.PIPEBRDY标志值链接到每个管道的BSTS标志设置。换言之，BRDY中断状态位由USBHS设置为1或0，具体取决于FIFO缓冲区状态。

(a) 用于传输管道

当FIFO端口准备好进行写访问时，BRDY中断状态位设置为1，当它未准备好时设置为0。发送方向上的DCP不会产生BRDY中断，即使它已准备好进行写访问。

(b) 用于接收管道

当FIFO缓冲区准备好进行读取访问时，BRDY中断状态位设置为1，当读取所有数据（未准备好进行读取访问）时设置为0。

当FIFO缓冲区为空时接收到零长度数据包时，相关位设置为1，并且持续产生BRDY中断，直到软件将1写入BCLR。使用此设置，PIPEBRDY标志不能由软件设置为0。

当SOFCFG.BRDYM位设置为1时，将所有管道的PIPECFG.BFRE位设置为0，并将SOFCFG.INTL位设置为1以进行电平检测。

图33.5显示了BRDY中断产生的时序。

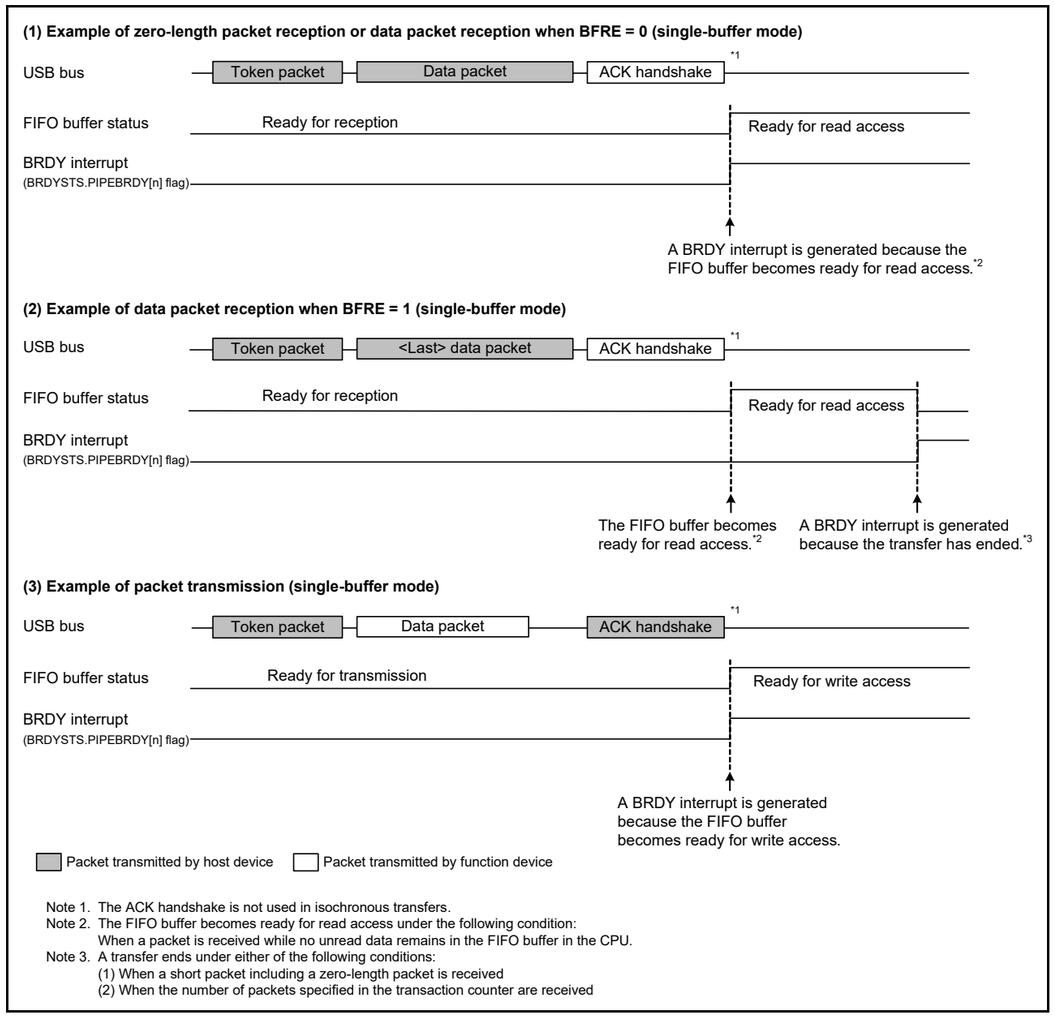


Figure 33.5 Timing of BRDY interrupt generation

The condition for clearing the INTSTS0.BRDY flag depends on the SOFCFG.BRDYM bit setting value, as shown in Table 33.21.

Table 33.21 Conditions for clearing the BRDY flag

BRDYM bit	Condition for clearing BRDY flag
0	The USBHS clears the BRDY flag to 0 when all bits in BRDYSTS are set to 0 by software
1	The USBHS clears the BRDY flag to 0 when the BSTS flags for all pipes have cleared to 0

33.3.6.2 NRDY interrupt

On generating an internal NRDY interrupt request for the pipe whose PID[1:0] bits are set to 01b (BUF response) by software, the USBHS sets the associated NRDYSTS.PIPENRDY flag to 1. If the associated bit in NRDYENB is set to 1 by software, the USBHS sets the INTSTS0.NRDY flag to 1 and generates a USBHS interrupt.

This section describes the conditions in which the USBHS generates the internal NRDY interrupt request for a given

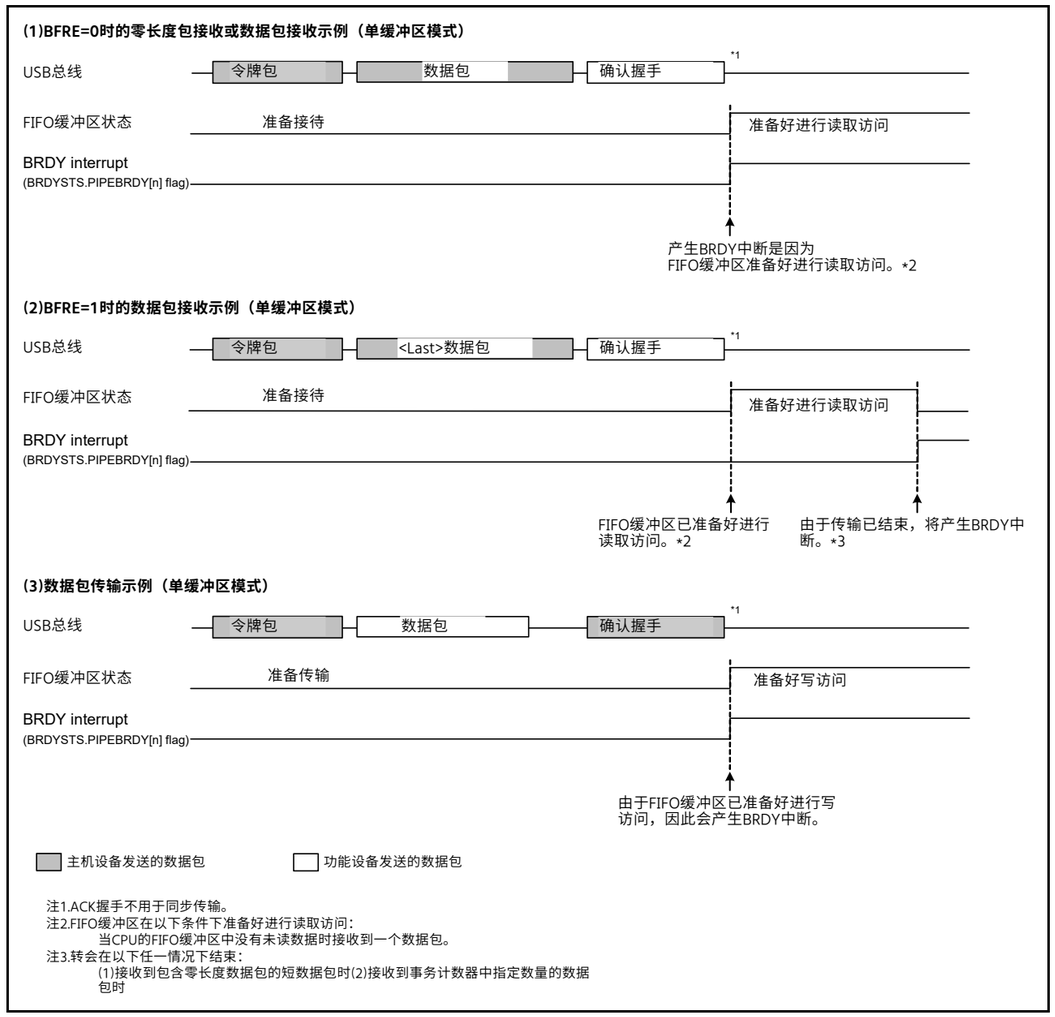


Figure 33.5 BRDY中断产生的时序

清除INTSTS0.BRDY标志的条件取决于SOFCFG.BRDYM位设置值，如图 Table 33.21.

Table 33.21 清除BRDY标志的条件

BRDYM bit	清除BRDY标志的条件
0	当软件将BRDYSTS中的所有位设置为0时，USBHS将BRDY标志清零
1	当所有管道的BSTS标志清除为0时，USBHS将BRDY标志清除为0

33.3.6.2 NRDY interrupt

在为PID[1:0]位被软件设置为01b（BUF响应）的管道生成内部NRDY中断请求时，USBHS将相关的NRDYSTS.PIPENRDY标志设置为1。如果NRDYENB中的相关位设置为通过软件置1，USBHS将INTSTS0.NRDY标志设置为1并产生USBHS中断。

本节描述了USBHS为给定的内部NRDY中断请求产生的条件。

pipe.

The internal NRDY interrupt request is not generated during setup transaction execution in host controller mode. During setup transactions in host controller mode, the SACK or SIGN interrupt is detected.

The internal NRDY interrupt request is not generated during status stage execution of the control transfer in device controller mode.

(1) In host controller mode when no split transactions occur in the connection

(a) For transmitting pipes

On any of the following conditions, the USBHS detects an NRDY interrupt:

- For isochronous transfer pipes, when the time to issue an OUT token comes while there is no data to be transmitted in the FIFO buffer. In this case, the USBHS transmits a zero-length packet following the OUT token and sets the associated NRDYSTS.PIPENRDY flag and the FRMNUM.OVRN flag to 1.
- During communications other than setup transactions on pipes not used for isochronous transfers, when any combination of the following two conditions occurs three consecutive times:
  - No response is returned from the peripheral device (when timeout is detected before detection of the handshake packet from the peripheral device
  - An error is detected in the packet from the peripheral device. In this case, the USBHS sets the associated PIPENRDY flag to 1 and changes the PID[1:0] setting for the associated pipe to 00b (NAK response)
- During communications other than setup transactions, when the STALL handshake is received from the peripheral device (includes STALL for both OUT and PING). In this case, the USBHS sets the associated PIPENRDY flag to 1 and changes the PID[1:0] setting for the associated pipe to 11b (STALL response).

(b) For receiving pipes

- For isochronous transfer pipes, when the time to issue an IN token comes but there is no space available in the FIFO buffer. In this case, the USBHS discards the received data for the IN token and sets the associated PIPENRDY flag and the OVRN flag to 1. When a packet error is detected in the received data for the IN token, the USBHS also sets the FRMNUM.CRCE flag to 1.
- For non-isochronous transfer pipes, when any combination of the following two cases occur three consecutive times:
  - No response is returned from the peripheral device for the IN token issued by the USBHS (when timeout is detected before detection of the DATA packet from the peripheral device)
  - An error is detected in the packet from the peripheral device. In this case, the USBHS sets the associated PIPENRDY flag to 1 and changes the associated PID[1:0] setting for the pipe to 00b (NAK response).
- For isochronous transfer pipes, when no response is returned from the peripheral device for the IN token (when timeout is detected before detection of the DATA packet from the peripheral device) or an error is detected in the packet from the peripheral device. In this case, the USBHS sets the associated NRDYSTS.PIPENRDY flag for each pipe to 1. The PID[1:0] setting for the pipe is not changed.
- For isochronous transfer pipes, when a CRC error or a bit stuffing error is detected in the received data packet. In this case, the USBHS sets the associated NRDYSTS.PIPENRDY flag for each pipe and the CRCE flag to 1.
- When the STALL handshake is received. In this case, the USBHS sets the associated NRDYSTS.PIPENRDY flag for each pipe to 1 and changes the PID[1:0] setting for the associated pipe to STALL.

(2) In host controller mode when split transactions occur in the connection

(a) For transmitting pipes

On any of the following conditions, the USBHS detects an NRDY interrupt:

- For isochronous transfer pipes, when the time to issue an OUT token comes while there is no data to be transmitted in the FIFO buffer. In this case, the USBHS sets the associated RDYSTS.PIPENRDY flag for the given pipes to 1 on issuing a start-split transaction and sets the FRMNUM.OVRN flag to 1. The USBHS also transmits a zero-length

pipe.

内部NRDY中断请求在主控制器模式下的设置事务执行期间不会产生。在主机控制器模式下的设置事务期间，检测到SACK或SIGN中断。

在设备控制器模式下控制传输的状态阶段执行期间，不会产生内部NRDY中断请求。

(1) 在主机控制器模式下，连接中没有发生拆分事务

(a) 用于传输管道

在以下任何一种情况下，USBHS都会检测到NRDY中断：

- 对于同步传输管道，当发出OUT令牌的时间到来时，FIFO缓冲区中没有要传输的数据。在这种情况下，USBHS在OUT令牌之后发送一个长度为零的数据包，并将相关的NRDYSTS.PIPENRDY标志和FRMNUM.OVRN标志设置为1。
- 在不用于同步传输的管道上的设置事务以外的通信期间，当以下两种情况的任意组合连续发生3次时：
  - 外围设备没有返回响应（当在检测到来自外围设备的握手包之前检测到超时时
  - 在来自外围设备的数据包中检测到错误。在这种情况下，USBHS设置相关的PIPENRDY标志为1并将关联管道的PID[1:0]设置更改为00b（NAK响应）
- 在设置事务以外的通信期间，当从外围设备接收到STALL握手时（包括OUT和PING的STALL）。在这种情况下，USBHS将关联的PIPENRDY标志设置为1，并将关联管道的PID[1:0]设置更改为11b（STALL响应）。

(b) 用于接收管道

- 对于同步传输管道，当发出IN令牌的时间到来但FIFO缓冲区中没有可用空间时。在这种情况下，USBHS丢弃IN令牌的接收数据并将相关的PIPENRDY标志和OVRN标志设置为1。当在IN令牌的接收数据中检测到数据包错误时，USBHS也会设置FRMNUM.CRCE标志为1。
- 对于非等时传输管道，当下列两种情况的任意组合连续出现3次时：
  - USBHS发出的IN令牌没有从外围设备返回响应（当在检测到来自外围设备的DATA数据包之前检测到超时时）
  - 在来自外围设备的数据包中检测到错误。在这种情况下，USBHS设置相关的PIPENRDY标志为1并将管道的相关PID[1:0]设置更改为00b（NAK响应）。
- 对于同步传输管道，当外围设备没有返回对IN令牌的响应时（在检测到来自外围设备的DATA数据包之前检测到超时）或在来自外围设备的数据包中检测到错误。在这种情况下，USBHS将每个管道的相关NRDYSTS.PIPENRDY标志设置为1。管道的PID[1:0]设置不会更改。
- 对于同步传输管道，当在接收到的数据包中检测到CRC错误或位填充错误时。在这种情况下，USBHS为每个管道设置相关的NRDYSTS.PIPENRDY标志，并将CRCE标志设置为1。
- 当收到STALL握手时。在这种情况下，USBHS将每个管道的相关NRDYSTS.PIPENRDY标志设置为1，并将相关管道的PID[1:0]设置更改为STALL。

(2) 在连接中发生拆分事务时处于主机控制器模式

(a) 用于传输管道

在以下任何一种情况下，USBHS都会检测到NRDY中断：

- 对于同步传输管道，当发出OUT令牌的时间到来时，FIFO缓冲区中没有要传输的数据。在这种情况下，USBHS将给定管道的相关RDYSTS.PIPENRDY标志设置为1，然后将FRMNUM.OVRN标志设置为1。USBHS还传输零长度

packet following the OUT token.

- For non-isochronous transfer pipes, when any combination of the following two cases occurs three consecutive times:
  - No response is returned from the hub for start-split and complete-split transactions (when timeout is detected before detection of the handshake packet from the hub)
  - An error is detected in the packet from the hub. In this case, the USBHS sets the associated NRDYSTS.PIPENRDY flag for the pipe to 1 and changes the associated PID[1:0] setting for the pipe to 00b (NAK response).When an NRDY interrupt is detected on complete-split issuance, the USBHS clears the CSSTS flag to 0.
- When a STALL handshake is received for the complete-split transaction. In this case, the USBHS sets the associated NRDYSTS.PIPENRDY flag for the pipe to 1, changes the associated PID[1:0] setting for the pipe to 11b (STALL response), and clears the CSSTS flag to 0. An interrupt is not detected during setup transaction.

(b) For receiving pipes

- For isochronous transfer pipes, when the time to issue an IN token comes but there is no space available in the FIFO buffer. In this case, the USBHS sets the associated NRDYSTS.PIPENRDY flag for the given pipe and the FRMNUM.OVRN flag to 1 on start-split issuance. The USBHS discards the received data for the IN token.
- During bulk-pipe transfers or transfers other than setup transactions with the DCP, when any combination of the following two cases occurs three consecutive times:
  - No response is returned from the hub for the IN token the USBHS issued on issuance of the start-split or complete-split transactions (when timeout is detected before detection of the data packet from the hub)
  - An error is detected in the packet from the hub. In this case, the USBHS sets the associated NRDYSTS.PIPENRDY flag for the pipe to 1 and changes the associated PID[1:0] setting for the pipe to 00b (NAK response). When this condition occurs during complete-split, the USBHS clears the CSSTS flag to 0.
- During a complete-split transaction for isochronous transfer or interrupt transfer pipes, when any combination of the following two cases occurs three consecutive times:
  - No response is returned from the hub for the IN token issued by the USBHS (when a timeout is detected before detection of the DATA packet from the hub)
  - An error is detected in the packet from the hub. On generating this condition for an interrupt transfer pipe, the USBHS sets the associated NRDYSTS.PIPENRDY flag to 1, changes the associated PID[1:0] setting for the pipe to 00b (NAK response), and clears the CSSTS flag to 0. On generating this condition for the pipe for isochronous transfers, the USBHS sets the associated NRDYSTS.PIPENRDY flag for the pipe to 1, CRCE flag to 1, and clears the CSSTS bit to 0. It does not change the PID[1:0] setting.
- During a complete-split transaction, when the STALL handshake is received for a non-isochronous transfer pipe. In this case, the USBHS sets the associated NRDYSTS.PIPENRDY flag for the pipe to 1, changes the associated PID[1:0] setting for the pipe to 11b (STALL response), and clears the CSSTS flag to 0.
- During a complete-split transaction, when the NYET handshake is received for an isochronous transfer or interrupt transfer pipe for the microframe number = 4. In this case, the USBHS sets the associated NRDYSTS.PIPENRDY flag for each pipe to 1 and the CRCE flag to 1, and clears the CSSTS flag to 0. It does not change the PID[1:0] setting.

(3) In device controller mode

(a) For transmitting pipes

- When an IN token is received while there is no data to be transmitted in the FIFO buffer. In this case, the USBHS generates an NRDY interrupt request on reception of the IN token and sets the NRDYSTS.PIPENRDY flag to 1. For an isochronous transfer pipe in which an interrupt is generated, the USBHS transmits a zero-length packet and sets the FRMNUM.OVRN flag to 1.

(b) For receiving pipes

- When an OUT token is received but there is no space available in the FIFO buffer. For an isochronous transfer pipe

OUT令牌之后的数据包。

- 对于非等时传输管道，当下列两种情况的任意组合连续出现3次时：
  - 集线器没有响应开始拆分和完成拆分事务（在检测到来自集线器的握手数据包之前检测到超时）
  - 在来自集线器的数据包中检测到错误。在这种情况下，USBHS设置相关的管道的NRDYSTS.PIPENRDY标志为1，并将管道的相关PID[1:0]设置更改为00b（NAK响应）。当在发出完全拆分时检测到NRDY中断时，USBHS将CSSTS标志清除为0.
- 当收到完整拆分事务的STALL握手时。在这种情况下，USBHS将管道的相关NRDYSTS.PIPENRDY标志设置为1，将管道的相关PID[1:0]设置更改为11b（STALL响应），并将CSSTS标志清除为0。中断是在设置事务期间未检测到。

(b) 用于接收管道

- 对于同步传输管道，当发出IN令牌的时间到来但FIFO缓冲区中没有可用空间时。在这种情况下，USBHS将给定管道的相关NRDYSTS.PIPENRDY标志和FRMNUM.OVRN标志设置为1在开始拆分发布时。USBHS丢弃接收到的IN令牌数据。
- 在与DCP进行批量管道传输或设置交易以外的传输期间，当以下两种情况的任意组合连续发生3次时：
  - 没有从集线器返回对USBHS在发布开始拆分或完成拆分事务时发出的IN令牌的响应（当在检测到来自集线器的数据包之前检测到超时时）
  - 在来自集线器的数据包中检测到错误。在这种情况下，USBHS设置相关的管道的NRDYSTS.PIPENRDY标志为1，并将管道的相关PID[1:0]设置更改为00b（NAK响应）。如果在完全拆分期间发生这种情况，USBHS会将CSSTS标志清除为0。
- 在同步传输或中断传输管道的完全拆分事务期间，当以下两种情况的任意组合连续发生3次时：
  - 对于USBHS发出的IN令牌，集线器没有返回响应（在检测到来自集线器的DATA数据包之前检测到超时）
  - 在来自集线器的数据包中检测到错误。在为中断传输管道生成此条件时，USBHS将相关的NRDYSTS.PIPENRDY标志设置为1，将管道的相关PID[1:0]设置更改为00b（NAK响应），并将CSSTS标志清除为0。在为同步传输的管道生成此条件时，USBHS将管道的相关NRDYSTS.PIPENRDY标志设置为1，CRCE标志设置为1，并将CSSTS位清除为0。它不会更改PID[1:0]环境。
- 在完全拆分事务期间，当接收到非同步传输管道的STALL握手时。在这种情况下，USBHS将管道的相关NRDYSTS.PIPENRDY标志设置为1，将管道的相关PID[1:0]设置更改为11b（STALL响应），并将CSSTS标志清除为0。
- 在完全拆分事务期间，当微帧编号=4的同步传输或中断传输管道接收到NYET握手时。在这种情况下，USBHS将每个管道的相关NRDYSTS.PIPENRDY标志设置为1，并将CRCE标志设置为为1，并将CSSTS标志清除为0。它不会更改PID[1:0]设置。

(3) 在设备控制器模式下

(a) 用于传输管道

- 当FIFO缓冲区中没有要传输的数据时接收到IN令牌。在这种情况下，USBHS在接收到IN令牌时产生一个NRDY中断请求，并将NRDYSTS.PIPENRDY标志设置为1。对于产生中断的同步传输管道，USBHS发送一个长度为零的数据包并将FRMNUM.OVRN标志为1。

(b) 用于接收管道

- 当接收到OUT令牌但FIFO缓冲区中没有可用空间时。对于同步传输管

in which an interrupt is generated, the USBHS generates an NRDY interrupt request on reception of the OUT token and sets the NRDYSTS.PIPENRDY flag to 1 and the FRMNUM.OVRN flag to 1. For a non-isochronous transfer pipe in which an interrupt is generated, the USBHS generates an NRDY interrupt request when an NAK handshake is transferred after the data following the OUT token is received, and sets the NRDYSTS.PIPENRDY flag to 1. The NRDY interrupt request is not generated during retransmission because of a DATA-PID mismatch. In addition, the NRDY interrupt request is not generated if an error occurs in the DATA packet.

- On receiving a PING token when there is no space available in the FIFO buffer. The USBHS generates an NRDY interrupt request on reception of the PING token, setting the NRDYSTS.PIPENRDY flag to 1.
- For isochronous transfer pipes, when a token is not received successfully within an interval frame. In this case, the USBHS generates an NRDY interrupt request when the SOF is received, and sets the NRDYSTS.PIPENRDY flag to 1.

Figure 33.6 shows the timing of NRDY interrupt generation in device controller mode.

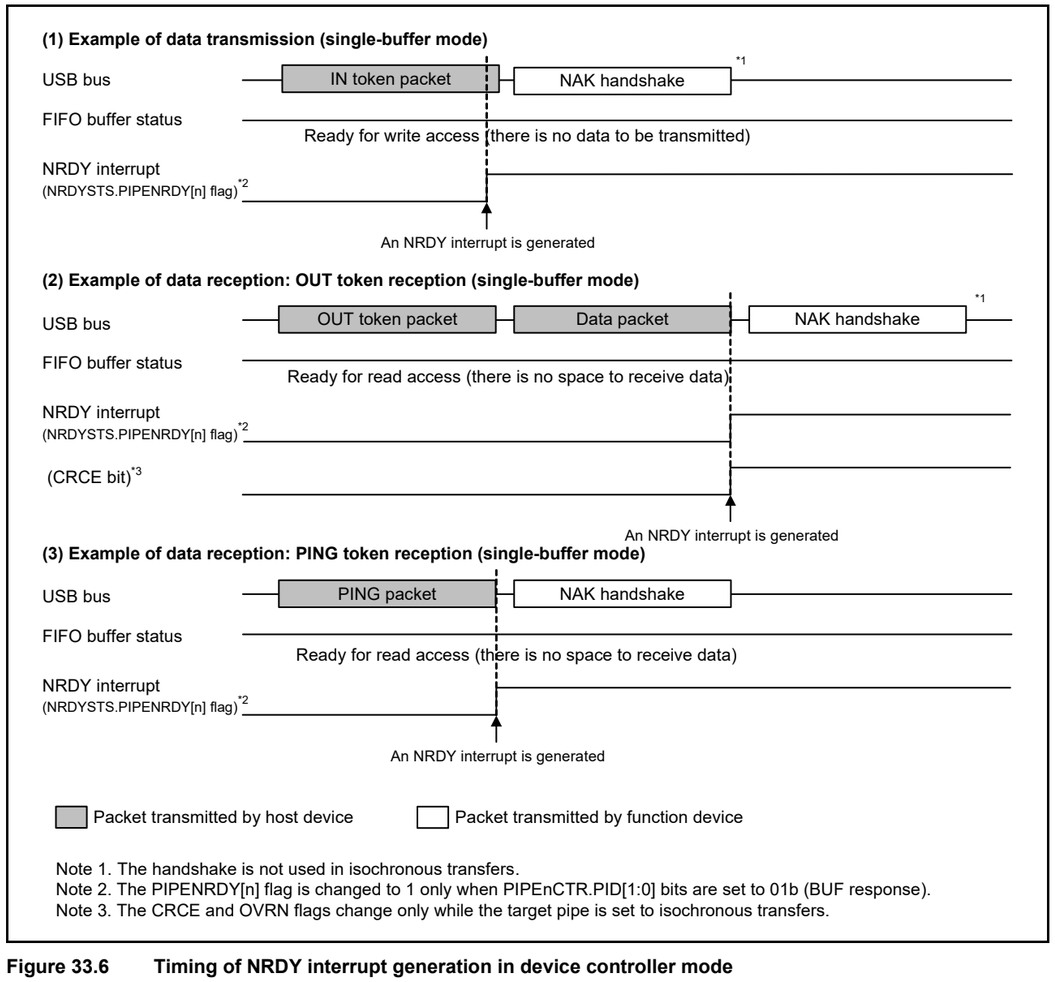


Figure 33.6 Timing of NRDY interrupt generation in device controller mode

33.3.6.3 BEMP interrupt

On detecting a BEMP interrupt for the pipe whose PID[1:0] bits in the pipe control register are set to 01b (BUF response) by software, the USBHS sets the associated BEMPSTS.PIPEBEMP flag to 1. If the associated BEMPENB bit is set to 1 by software, the USBHS sets the INTSTS0.BEMP flag to 1 and generates a USB interrupt. This section describes the

在产生中断时，USBHS在接收到OUT令牌时产生一个NRDY中断请求，并将NRDYSTS.PIPENRDY标志设置为1，将FRMNUM.OVRN标志设置为1。USBHS在接收到OUT令牌之后的数据后，在传输NAK握手时产生NRDY中断请求，并将NRDYSTS.PIPENRDY标志设置为1。由于DATA-PID，在重传期间不会产生NRDY中断请求不匹配。除此之外

如果DATA包中发生错误，则不会产生NRDY中断请求。

- 在FIFO缓冲区中没有可用空间时接收PING令牌。USBHS在接收到PING令牌时生成一个NRDY中断请求，将NRDYSTS.PIPENRDY标志设置为1。
- 对于同步传输管道，当在间隔帧内未成功接收到令牌时。在这种情况下，USBHS在接收到SOF时产生一个NRDY中断请求，并将NRDYSTS.PIPENRDY标志设置为1。

图33.6显示了设备控制器模式下NRDY中断产生的时序。

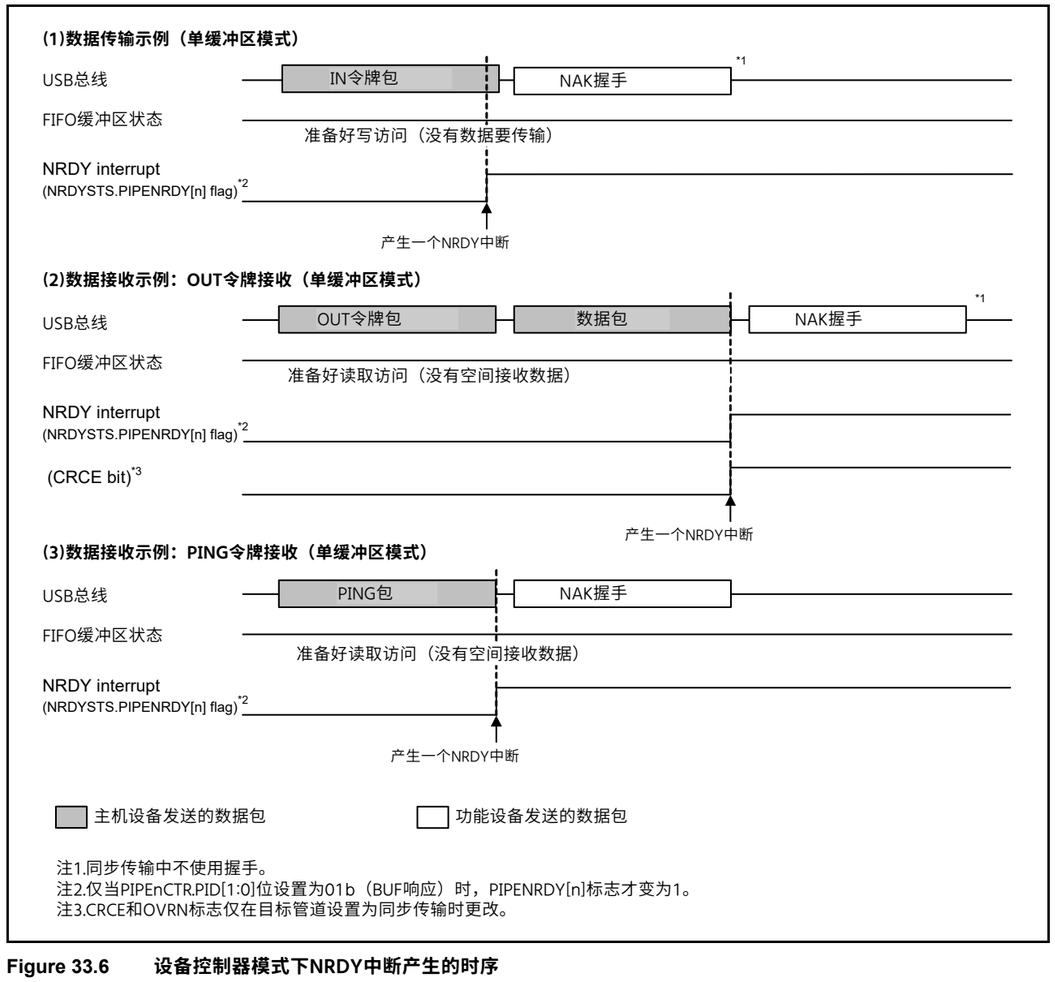


Figure 33.6 设备控制器模式下NRDY中断产生的时序

33.3.6.3 BEMP interrupt

在检测到管道控制寄存器中的PID[1:0]位被软件设置为01b（BUF响应）的管道的BEMP中断时，USBHS将相关的BEMPSTS.PIPEBEMP标志设置为1。如果相关的BEMPENB位是由软件设置为1，USBHS将INTSTS0.BEMP标志设置为1并产生USB中断。本节介绍

conditions in which the USBHS generates an internal BEMP interrupt request.

(1) For transmitting pipes

When the FIFO buffer of the associated pipe is empty on completion of transmission, including zero-length packet transmission, and in single buffer mode, an internal BEMP interrupt request is generated simultaneously with the BRDY interrupt for a non-DCP pipe. The internal BEMP interrupt request is not generated in any of the following conditions:

- When the CPU or DMA/DTC has already started writing data to the FIFO buffer of the CPU on completion of transmitting data from one FIFO buffer in double buffer mode
- When the buffer is cleared (emptied) by setting 1 to the PIPEnCTR.ACLRM or the BCLR bit in the port control register
- When an IN transfer (zero-length packet transmission) is performed during the control transfer status stage in device controller mode.

(2) For receiving pipes

When a successfully-received data packet size exceeds the specified maximum packet size. In this case, the USBHS generates a BEMP interrupt request, sets the associated BEMPSTS.PIPEBEMP flag to 1, discards the received data, and changes the associated PID[1:0] setting for the pipe to STALL (11b). The USBHS returns no response in host controller mode, and returns STALL response in device controller mode.

The internal BEMP interrupt request is not generated in any of the following conditions:

- When a CRC error or a bit stuffing error is detected in the received data
- When a setup transaction is being performed:
  - Writing 0 to the BEMPSTS.PIPEBEMP flag clears the status
  - Writing 1 to the BEMPSTS.PIPEBEMP flag has no effect.

Figure 33.7 shows the timing of BEMP interrupt generation in device controller mode.

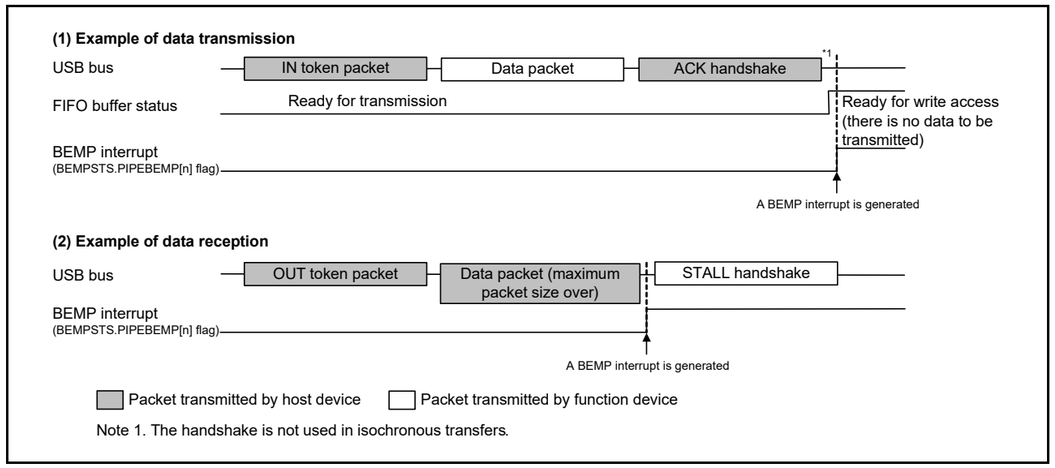


Figure 33.7 Timing of BEMP interrupt generation in device controller mode

33.3.6.4 Device state transition interrupt (device controller mode)

Figure 33.8 shows a diagram of the USBHS device state transitions. The USBHS controls device states and generates device state transition interrupts. However, recovery from the Suspend state (resume signal detection) is detected by means of the resume interrupt. Device state transition interrupts can be enabled or disabled independently in INTENB0. Devices whose states have changed can be checked in the PL1CTRL.DVSQ[3:0] flags.

When a transition is made to the default state, a device state transition interrupt is generated after a USB bus reset is

USBHS产生内部BEMP中断请求的条件。

(1) 用于传输管道

当相关管道的FIFO缓冲区在传输完成时为空时，包括零长度数据包传输，并且在单缓冲区模式下，内部BEMP中断请求与非DCP管道的BRDY中断同时生成。在以下任何一种情况下都不会产生内部BEMP中断请求：

- 当CPU或DMADTC在双缓冲模式下从一个FIFO缓冲区完成数据传输后已经开始向CPU的FIFO缓冲区写入数据时
- 当通过将PIPEnCTR.ACLRM或端口控制寄存器中的BCLR位设置为1来清除（清空）缓冲区时
- 在设备控制器模式下的控制传输状态阶段执行IN传输（零长度数据包传输）时。

(2) 用于接收管道

当成功接收的数据包大小超过指定的最大包大小时。在这种情况下，USBHS生成一个BEMP中断请求，将相关的BEMPSTS.PIPEBEMP标志设置为1，丢弃接收到的数据，并将管道的相关PID[1:0]设置更改为STALL(11b)。USBHS在主机控制器模式下不返回响应，在设备控制器模式下返回STALL响应。

在以下任何一种情况下都不会产生内部BEMP中断请求：

- 在接收到的数据中检测到CRC错误或位填充错误时
- 执行设置事务时：
  - 将0写入BEMPSTS.PIPEBEMP标志会清除状态
  - 向BEMPSTS.PIPEBEMP标志写入1无效。

图33.7显示了设备控制器模式下BEMP中断产生的时序。

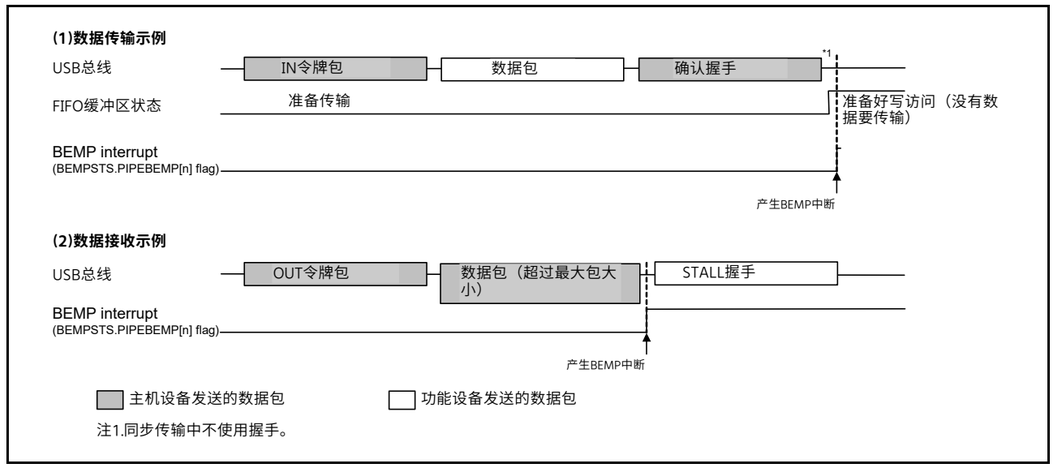


Figure 33.7 设备控制器模式下BEMP中断产生的时序

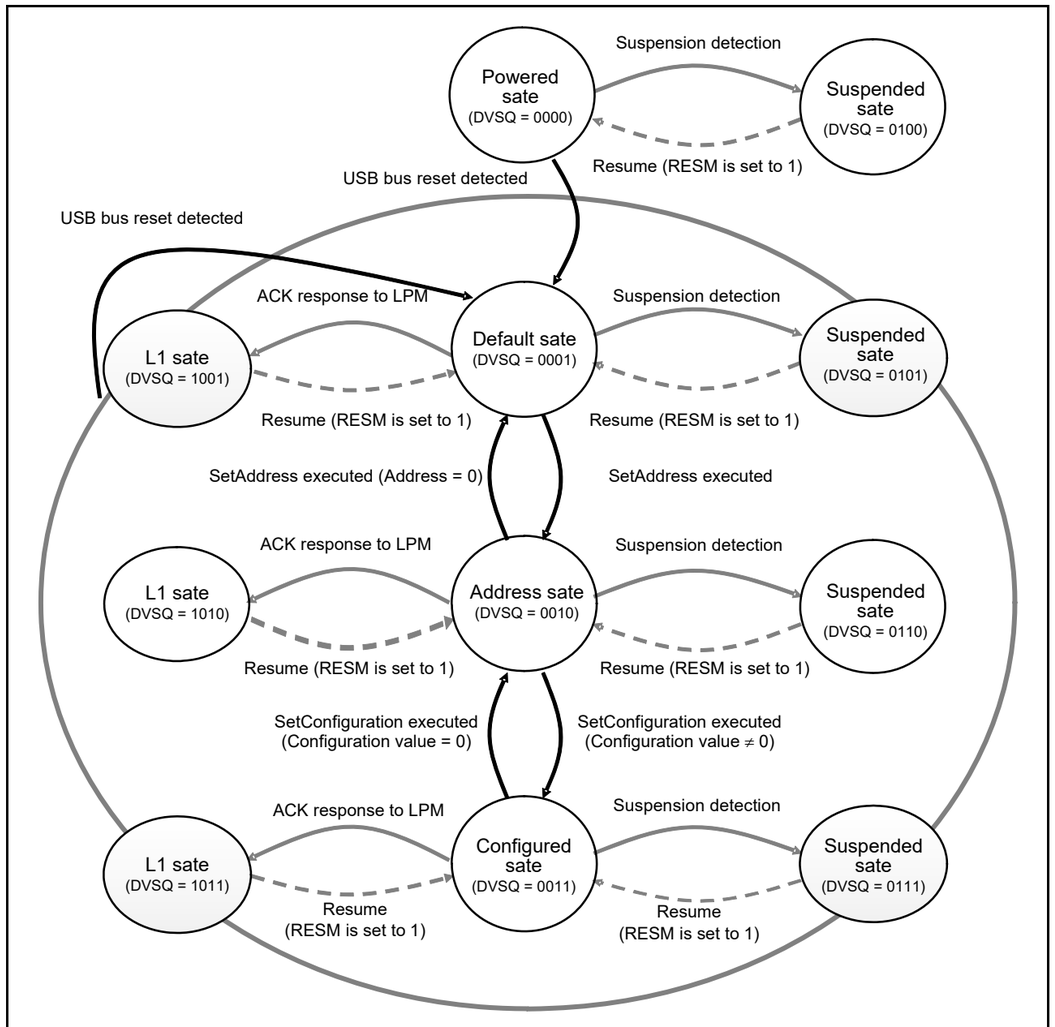
33.3.6.4 设备状态转换中断（设备控制器模式）

图33.8显示了USBHS设备状态转换的示意图。USBHS控制设备状态并产生设备状态转换中断。但是，从挂起状态的恢复（恢复信号检测）是通过恢复中断来检测的。可以在INTENB0中独立启用或禁用设备状态转换中断。可以在PL1CTRL.DVSQ[3:0]标志中检查状态已更改的设备。

当转换到默认状态时，会在USB总线复位后产生设备状态转换中断

detected.

The USBHS controls device states, and device state transition interrupts can be generated, only in device controller mode.



Note: For a transition, indicated by a solid line, the DVST bit is set to 1. For a resume, indicated by a dashed line, the RESM bit is set to 1.

Figure 33.8 Device state transitions

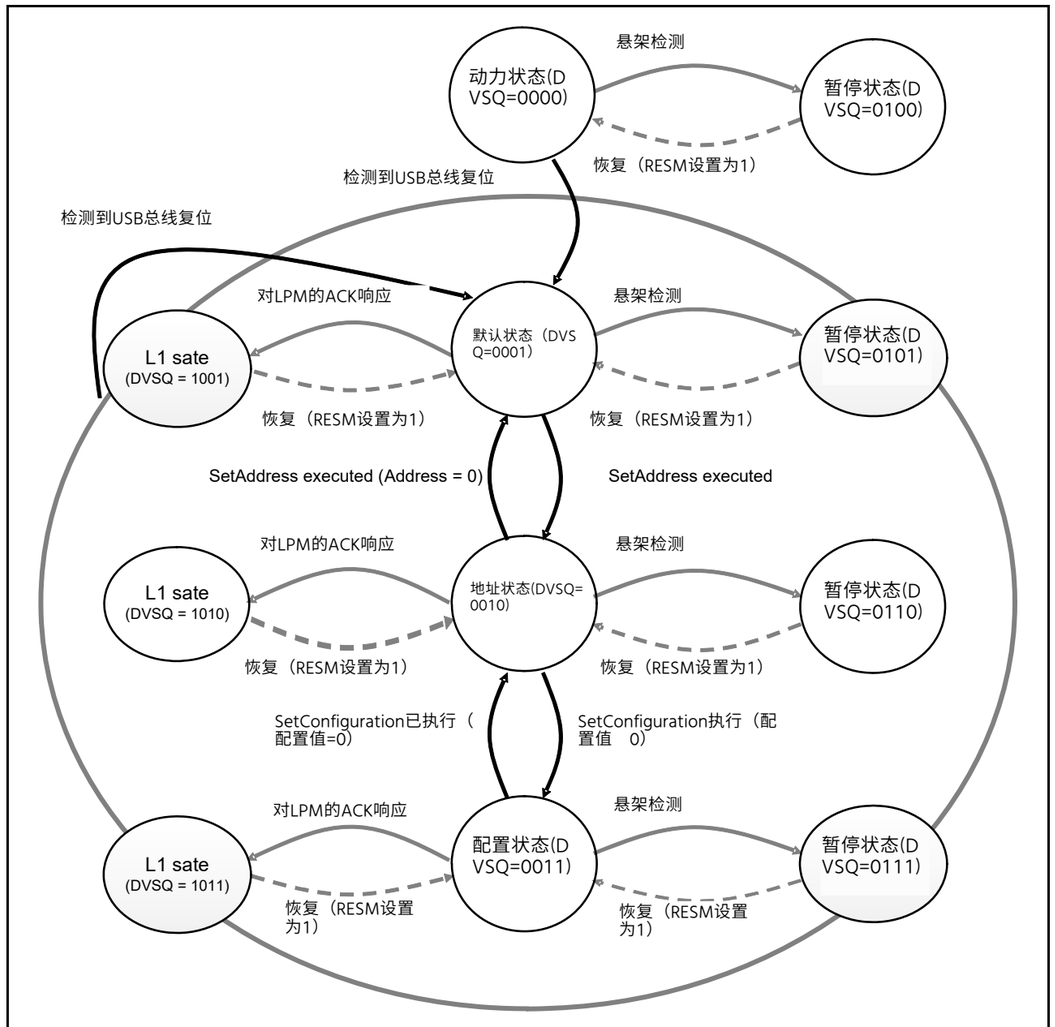
33.3.6.5 Control transfer stage transition interrupt (device controller mode)

Figure 33.9 shows a diagram of the control transfer stage transitions of the USBHS. The USBHS controls the control transfer sequence and generates control transfer stage transition interrupts. Control transfer stage transition interrupts can be enabled or disabled independently in INTENB0. Transfer stages that have transitioned can be checked in the INTSTS0.CTSQ[2:0] bits.

Control transfer stage transition interrupts are generated only in device controller mode. This section describes control transfer sequence errors. When an error occurs, the DCPCTR.PID[1:0] bits are set to 1xb (STALL response).

detected.

USBHS控制设备状态，并且只能在设备控制器模式下产生设备状态转换中断。



Note: 对于由实线指示的转换，DVST位设置为1。对于由虚线指示的恢复，RESM位设置为1。

Figure 33.8 设备状态转换

33.3.6.5 控制转移阶段转换中断（设备控制器模式）

图33.9显示了USBHS的控制传输阶段转换图。USBHS控制控制传输序列并产生控制传输阶段转换中断。控制转移阶段转换中断可以在INTENB0中独立启用或禁用。可以在INTSTS0.CTSQ[2:0]位中检查已转换的传输阶段。

控制转移阶段转换中断仅在设备控制器模式下产生。本节描述控制传输序列错误。发生错误时，DCPCTR.PID[1:0]位设置为1xb（STALL响应）。

(1) Control read transfer errors

- An OUT token or PING token is received but no data is transferred in response to the IN token at the data stage
- An IN token is received at the status stage
- A data packet with DATAPID = DATA0 is received at the status stage.

(2) Control write transfer errors

- An IN token is received but no ACK returned in response to the OUT token in the data stage
- A data packet with DATAPID = DATA0 is received as the first data packet at the data stage
- An OUT token or PING token is received in the status stage.

(3) Control write no data transfer errors

- An OUT token or PING token is received at the status stage.

At the control write transfer data stage, if the receive data length exceeds the wLength value of the USB request, it is not recognized as a control transfer sequence error. At the control read transfer status stage, packets other than zero-length packets are received by an ACK response and the transfer ends normally.

When a CTRT interrupt occurs in response to a sequence error (INTSTS0.CTRT flag = 1), the CTSQ[2:0] = 110b value is saved until CTRT flag clears to 0, clearing the interrupt status. While CTSQ[2:0] bits = 110b is being saved, no CTRT interrupt for ending the setup stage is generated, even if a new USB request is received. The USBHS saves the setup stage completion status, and it generates a CTRT interrupt after the interrupt status is cleared by software.

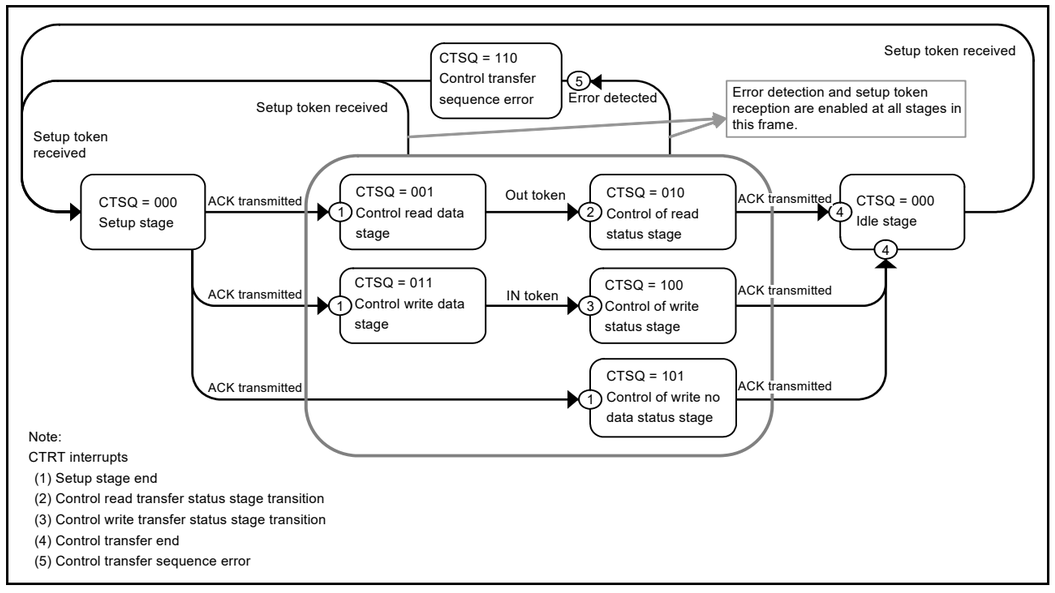


Figure 33.9 Control transfer stage transitions

33.3.6.6 Frame update interrupt

In host controller mode, an interrupt is generated when the frame number is updated.

In device controller mode, an SOFR interrupt is generated when the frame number is updated. The USBHS updates the frame number and generates an SOFR interrupt if it detects a new SOF packet during full-speed operation.

33.3.6.7 VBUS interrupt

When the USBHS_VBUS pin level changes, a VBUS interrupt is generated. The level of the USBHS_VBUS pin can be

(1) 控制读取传输错误

- 接收到OUT令牌或PING令牌，但在数据阶段没有响应IN令牌传输数据
- 在状态阶段收到一个IN令牌
- 在状态阶段接收到一个DATAPID=DATA0的数据包。

(2) 控制写入传输错误

- 接收到IN令牌，但在数据阶段没有响应OUT令牌返回ACK
- DATAPID=DATA0的数据包作为数据阶段的第一个数据包被接收
- 在状态阶段收到一个OUT令牌或PING令牌。

(3) 控制写入无数据传输错误

- 在状态阶段收到OUT令牌或PING令牌。

在控制写入传输数据阶段，如果接收数据长度超过USB请求的wLength值，则不被识别为控制传输序列错误。在控制读取传输状态阶段，除了零长度数据包之外的数据包被一个ACK响应接收并且传输正常结束。

当CTRT中断响应序列错误（INTSTS0.CTRT标志=1）时，CTSQ[2:0]=110b值被保存，直到CTRT标志清除为0，清除中断状态。在保存CTSQ[2:0]位=110b时，不会产生用于结束设置阶段的CTRT中断，即使收到新的USB请求也是如此。USBHS保存建立阶段完成状态，软件清除中断状态后产生CTRT中断。

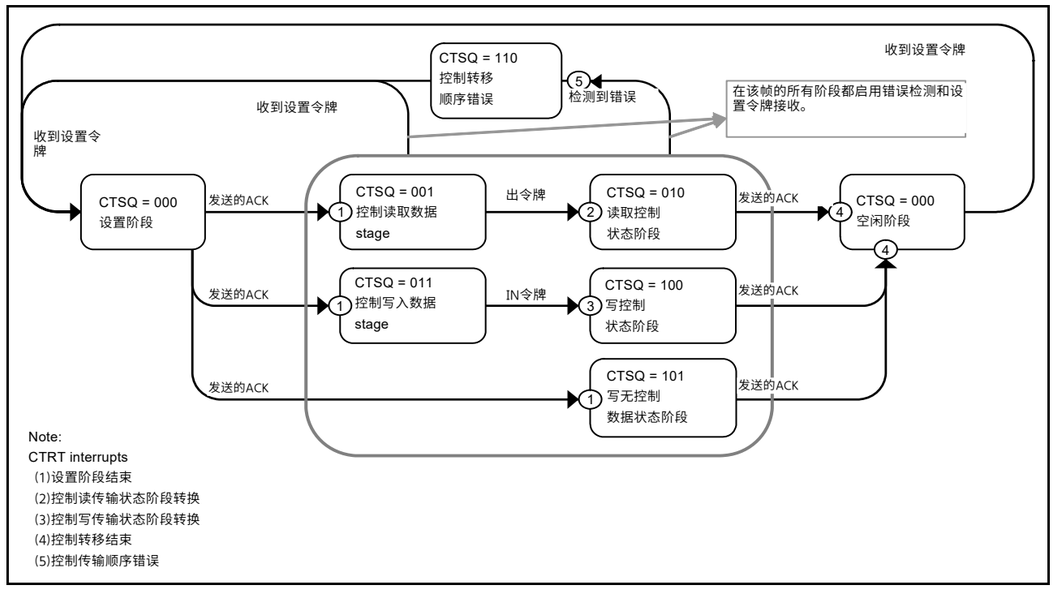


Figure 33.9 控制转移阶段转换

33.3.6.6 帧更新中断

在主机控制器模式下，更新帧号时会产生中断。

在设备控制器模式下，更新帧号时会产生SOFR中断。如果在全速运行期间检测到新的SOF数据包，USBHS会更新帧号并生成SOFR中断。

33.3.6.7 VBUS interrupt

当USBHS_VBUS引脚电平改变时，会产生VBUS中断。USBHS_VBUS引脚的电平可以是

checked in the INTSTS0.VBSTS flag. Whether the host controller is connected or disconnected can be confirmed using the VBUS interrupt. If the system is activated with the host controller connected, the first VBUS interrupt is not generated, because there is no change in the USBHS_VBUS pin level.

33.3.6.8 Resume interrupt

In device controller mode, a resume interrupt is generated when the device is in the Suspend state and the USB bus state has changed (from J-state to K-state, or from J-state to SE0). Recovery from the Suspend state is detected by means of the resume interrupt.

In host controller mode, no resume interrupt is generated. Use the BCHG interrupt to detect a change in the USB bus state.

33.3.6.9 OVRCR interrupt

An OVRCR interrupt is generated when the USBHS_OVRCURA or USBHS_OVRCURB pin level has changed. The levels of the USBHS_OVRCURA and USBHS_OVRCURB pins can be checked in the SYSSTS0.OVCMON[1:0] flags. The external power supply IC can check whether overcurrent is detected using the OVRCR interrupt.

For OTG connections, the OVRCR interrupt allows you to check whether a change is detected in the VBUS comparator.

33.3.6.10 BCHG interrupt

A BCHG interrupt is generated when the USB bus state has changed. The BCHG interrupt can be used to detect whether a peripheral device is connected. It can also be used to detect a remote wakeup in host controller mode. The BCHG interrupt is generated in both host and device controller modes.

33.3.6.11 DTCH interrupt

A DTCH interrupt occurs when a USB bus disconnect is detected in host controller mode. The USBHS detects bus disconnects in compliance with the USB 2.0 specification.

On interrupt detection, all pipes in which communications are being carried out for the relevant port must be terminated by software. The pipes enter the wait state for a bus connection to the port, waiting for an ATTCH interrupt to occur. Regardless of the value set in the associated interrupt enable bit, the USBHS hardware:

- Sets the DVSTCTR0.UACT bit for the port in which the DTCH interrupt is detected to 0
- Puts the port in which the DTCH interrupt occurred into the idle state.

33.3.6.12 SACK interrupt

A SACK interrupt is generated when an ACK response for the transmitted setup packet is received from the peripheral device in host controller mode. The SACK interrupt can be used to confirm that the setup transaction is successfully complete.

33.3.6.13 SIGN interrupt

A SIGN interrupt is generated when an ACK response for the transmitted setup packet is not correctly received from the peripheral device three consecutive times in host controller mode. The SIGN interrupt can be used to detect no ACK response transmitted from the peripheral device or corruption of an ACK packet.

33.3.6.14 ATTCH interrupt

An ATTCH interrupt is generated when J-state or K-state of the full-speed signal level is detected on the USB port for 2.5 µs in host controller mode. To be more specific, an ATTCH interrupt is detected in any of the following conditions:

- When K-state, SE0, or SE1 changes to J-state, and J-state continues 2.5 µs
- When J-state, SE0, or SE1 changes to K-state, and K-state continues 2.5 µs.

33.3.6.15 EOFERR interrupt

An EOFERR interrupt occurs when the USBHS detects that communication is not complete at the EOF2 timing defined in the USB 2.0 specification.

检查INTSTS0.VBSTS标志。主控制器是连接还是断开可以使用VBUS中断来确认。如果系统在连接主机控制器的情况下激活，则不会产生第一个VBUS中断，因为USBHS_VBUS引脚电平没有变化。

33.3.6.8 恢复中断

在设备控制器模式下，当设备处于Suspend状态并且USB总线状态发生变化（从J-state到K-state，或从J-state到SE0）时，会产生一个恢复中断。通过恢复中断检测从挂起状态的恢复。

在主机控制器模式下，不会产生恢复中断。使用BCHG中断来检测USB总线状态的变化。

33.3.6.9 OVRCR interrupt

当USBHS_OVRCURA或USBHS_OVRCURB引脚电平发生变化时，会产生OVRCR中断。USBHS_OVRCURA和USBHS_OVRCURB引脚的电平可以在SYSSTS0.OVCMON[1:0]标志中检查。外部电源IC可以使用OVRCR中断检查是否检测到过电流。

对于OTG连接，OVRCR中断允许您检查是否在VBUS比较器中检测到变化。

33.3.6.10 BCHG interrupt

当USB总线状态改变时会产生BCHG中断。BCHG中断可用于检测是否连接了外围设备。它还可用于检测主机控制器模式下的远程唤醒。BCHG中断在主机和设备控制器模式下产生。

33.3.6.11 DTCH interrupt

当在主机控制器模式下检测到USB总线断开连接时，会发生DTCH中断。USBHS检测符合USB2.0规范的总线断开连接。

在检测到中断时，为相关端口执行通信的所有管道必须由软件终止。管道进入等待状态，等待总线连接到端口，等待ATTCH中断发生。无论相关中断使能位中设置的值如何，USBHS硬件：

- 将检测到DTCH中断的端口的DVSTCTR0.UACT位设置为0
- 将发生DTCH中断的端口置于空闲状态。

33.3.6.12 SACK中断

当在主机控制器模式下从外围设备接收到对发送的设置数据包的ACK响应时，将产生SACK中断。SACK中断可用于确认设置事务成功完成。

33.3.6.13 标志中断

在主机控制器模式下，如果连续三次未从外围设备正确接收到已发送的设置数据包的ACK响应，则会产生SIGN中断。SIGN中断可用于检测没有从外围设备发送的ACK响应或ACK数据包的损坏。

33.3.6.14 ATTCH interrupt

在主机控制器模式下，当在USB端口上检测到全速信号电平的J状态或K状态持续2.5µs时，将产生ATTCH中断。更具体地说，在以下任何一种情况下都会检测到ATTCH中断：

- 当K-state、SE0或SE1变为J-state时，J-state持续2.5μs
- 当J-state、SE0或SE1变为K-state时，K-state持续2.5μs。

33.3.6.15 EOFERR interrupt

当USBHS检测到在USB2.0规范中定义的EOF2时序未完成通信时，将发生EOFERR中断。

On interrupt detection, all pipes in which communications are being carried out for the relevant port must be terminated by software, and the port must be re-enumerated. Regardless of the value set in the associated interrupt enable bit, the USBHS hardware:

- Sets the DVSTCTR0.UACT bit for the port in which the EOFERR interrupt is detected to 0
- Puts the port in which the EOFERR interrupt is generated into the idle state.

33.3.6.16 PDDETINT interrupt

The USBHS sets the INTSTS1.PDDETINT flag to 1 on detecting a level change (high to low or low to high) in the PDDET pin input value and generates the PDDETINT interrupt. When the PDDETINT interrupt is generated, use software to repeatedly read the BCCTRL.PDDETSTS flag until the same value is read three or more times, and perform debounce processing.

33.3.6.17 LPMEND interrupt

When the LPM transaction ends because a response from the peripheral device or a timeout is detected, the INTSTS1.LPMEND flag sets to 1 and the LPMEND interrupt is generated.

33.3.6.18 L1RSMEND interrupt

When performing resume processing when the USBHS has transitioned to the L1 state because an ACK is received in response to an LPM token, the USBHS sets the INTSTS1.L1RSMEND flag to 1 on completion of the resume processing.

33.3.7 Pipe Control

Table 33.22 lists the pipe settings for the USBHS. USB data transfer is performed through logical pipes that the software associates with endpoints. The USBHS provides 10 pipes for data transfer. Set up the pipes based on your system specifications.

Table 33.22 Pipe settings (1 of 2)

Register name	Bit name	Setting	Notes
DCPCFG PIPECFG	TYPE[1:0]	Transfer type	Pipes 1 to 9: Settable
	BFRE	BRDY interrupt mode	Pipes 1 to 5: Settable
	DBLB	Double buffer select	Pipes 1 to 5: Settable
	CNTMD	Selection of continuous transfer or discontinuous transfer	Pipes 1, 2: Settable only for bulk transfers Pipes 3 to 5: Settable
	DIR	Transfer direction select	IN or OUT settable
	EPNUM[3:0]	Endpoint number	Pipes 1 to 9: Settable Set this number to a value other than 0000 when one or more pipes are used.
	SHTNAK	Selects disabled state for pipe when transfer ends	Pipes 1, 2: Settable only for bulk transfers Pipes 3 to 5: Settable
PIPEBUF	BUFSIZE	FIFO buffer size	DCP: Setting disabled (fixed to 256 bytes) Pipes 1 to 5: Settable up to 2 KB Pipes 6 to 9: Setting disabled (fixed to 64 bytes)
	BUFNMB	FIFO buffer number	DCP: Setting disabled (fixed to 0h-3h area) Pipes 1 to 5: Setting disabled (8h-87h area specifiable) Pipes 6 to 9: Setting disabled (fixed to 4h-7h area)
DCPMAXP PIPEMAXP	DEVSEL[3:0]	Device select	Viewable only in host controller mode
	MXPS	Maximum packet size	Setting compliant with USB specification
PIPEPERI	IFIS	Buffer flush	Pipes 1, 2: Settable only for isochronous transfers Pipes 3 to 5: Setting disabled Pipes 6 to 9: Setting disabled
	IITV[2:0]	Interval counter	Pipes 1, 2: Settable only for isochronous transfers Pipes 3 to 5: Setting disabled Pipes 6 to 9: Settable only in host controller mode

在检测到中断时，所有为相关端口执行通信的管道必须由软件终止，并且必须重新枚举该端口。无论相关中断使能位中设置的值如何，USBHS硬件：

- 将检测到EOFERR中断的端口的DVSTCTR0.UACT位设置为0
- 将产生EOFERR中断的端口置于空闲状态。

33.3.6.16 PDDETINT interrupt

USBHS将INTSTS1.PDDETINT标志设置为1在检测到电平变化（高到低或低到高）在PDDET引脚输入值并产生PDDETINT中断。当PDDETINT中断产生时，用软件反复读取BCCTRL.PDDETSTS标志，直到读取3次以上相同的值，并进行去抖动处理。

33.3.6.17 LPMEND interrupt

当LPM事务由于检测到来自外围设备的响应或超时而结束时，INTSTS1.LPMEND标志设置为1并产生LPMEND中断。

33.3.6.18 L1RSMEND interrupt

当USBHS由于接收到响应LPM令牌的ACK而转换到L1状态时执行恢复处理时，USBHS在恢复处理完成时将INTSTS1.L1RSMEND标志设置为1。

33.3.7 管道控制

表33.22列出了USBHS的管道设置。USB数据传输是通过软件与端点关联的逻辑管道执行的。USBHS提供了10个用于数据传输的管道。根据您的系统规格设置管道。

Table 33.22 管道设置(1of2)

注册名称	位名称	Setting	Notes
DCPCFG PIPECFG	TYPE[1:0]	传输类型	管道1至9：可设置
	BFRE	BRDY中断模式	管道1至5：可设置
	DBLB	双缓冲选择	管道1至5：可设置
	CNTMD	选择连续转移或不连续转移	管道1、2：仅可设置批量传输 管道3至5：可设置
	DIR	传输方向选择	输入或输出可设置
	EPNUM[3:0]	端点编号	管道1至9：可设置 当使用一个或多个管道时，将此数字设置为0000以外的值。
	SHTNAK	传输结束时为管道选择禁用状态	管道1、2：仅可设置批量传输 管道3至5：可设置
PIPEBUF	BUFSIZE	FIFO缓冲区大小	DCP：设置禁用（固定为256字节） 管道1到5：最大可设置2KB 管道6到9：设置禁用（固定为64字节）
	BUFNMB	先进先出缓冲器编号	DCP：设置禁用（固定为0h-3h区域） 管道1至5：禁用设置（可指定8h-87h区域） 管道6至9：禁用设置（固定为4h-7h区域）
DCPMAXP PIPEMAXP	DEVSEL[3:0]	设备选择	仅在主机控制器模式下可见
	MXPS	最大数据包大小	符合USB规格的设置
PIPEPERI	IFIS	缓冲区刷新	管道1、2：仅可设置用于同步传输 管道3至5：设置禁用管道6至9：设置禁用
	IITV[2:0]	间隔计数器	管道1、2：仅可设置用于同步传输管道3至5：设置禁用 管道6到9：仅在主机控制器模式下可设置

Table 33.22 Pipe settings (2 of 2)

Register name	Bit name	Setting	Notes
DCPCTR PIPEnCTR	BSTS	Buffer status	For the DCP, receive buffer status and transmit buffer status are switched with the ISEL bit
	INBUFM	IN buffer monitor	Available only for pipes 1 to 5
	SUREQ	Setup request	Settable only for the DCP and controlled in host controller mode
	SUREQCLR	SUREQ clear	Settable only for the DCP and controlled in host controller mode
	CSCLR	CSSTS clear	Controllable only in host controller mode
	CSSTS	Split status check	Viewable only in host controller mode
	ATREPM	Auto response mode	Pipes 1 to 5: Settable only in device controller mode
	ACLRM	Auto buffer clear	Pipes 1 to 9: Settable
	SQCLR	Sequence clear	Clears the data toggle bit
	SQSET	Sequence set	Sets the data toggle bit
	SQMON	Sequence check	Monitors the data toggle bit
	PBUSY	PIPE busy check	-
	PID[1:0]	Response PID	-
PIPEnTRE	TRENB	Transaction count enable	Pipes 1 to 5: Settable
	TRCLR	Current transaction counter clear	Pipes 1 to 5: Settable
PIPEnTRN	TRNCNT	Transaction counter	Pipes 1 to 5: Settable

33.3.7.1 Pipe control register switching procedures

The following bits in the pipe control registers can be changed only when USB communication is prohibited (PID[1:0] bits are 00b (NAK response)). Figure 33.10 shows pipe control register switching procedures when USB communication is enabled (PID[1:0] bits are 00b (BUF response)).

Do not change the following registers and bits when USB communication is enabled (PID[1:0] bits are 01b (BUF response)):

- Bits in DCPCFG and DCPMAXP
- SQCLR and SQSET bits in DCPCTR
- Bits in PIPECFG, PIPEBUF, PIPEMAXP, and PIPEPERI
- ATREPM, ACLRM, SQCLR, and SQSET bits in PIPEnCTR
- Bits in PIPEnTRE and PIPEnTRN
- Bits in DEVADDm (m = 0 to A).

To set the CSCLR bits and bits in DEVADDm (m = 0 to A), follow the procedures described in section 33.2, Register Descriptions.

Table 33.22 管道设置(2of2)

注册名称	位名称	Setting	Notes
DCPCTR PIPEnCTR	BSTS	缓冲状态	对于DCP，接收缓冲区状态和发送缓冲区状态通过ISEL位切换
	INBUFM	IN缓冲监视器	仅适用于管道1至5
	SUREQ	设置请求	只能为DCP设置并在主机控制器模式下控制
	SUREQCLR	SUREQ clear	只能为DCP设置并在主机控制器模式下控制
	CSCLR	CSSTS clear	仅在主机控制器模式下可控
	CSSTS	拆分状态检查	仅在主机控制器模式下可见
	ATREPM	自动响应模式	管道1到5：仅在设备控制器模式下可设置
	ACLRM	自动缓冲区清除	管道1至9：可设置
	SQCLR	序列清晰	清除数据切换位
	SQSET	序列集	设置数据切换位
	SQMON	序列检查	监控数据切换位
	PBUSY	管道忙检查	-
	PID[1:0]	响应PID	-
PIPEnTRE	TRENB	事务计数启用	管道1至5：可设置
	TRCLR	当前交易柜台清零	管道1至5：可设置
PIPEnTRN	TRNCNT	交易柜台	管道1至5：可设置

33.3.7.1 管道控制寄存器切换程序

只有当USB通信被禁止时（PID[1:0]位为00b（NAK响应））才能更改管道控制寄存器中的以下位。图33.10显示了启用USB通信时的管道控制寄存器切换过程（PID[1:0]位为00b（BUF响应））。

启用USB通信时，请勿更改以下寄存器和位（PID[1:0]位为01b（BUF响应））：

- DCPCFG和DCPMAXP中的位
- DCPCTR中的SQCLR和SQSET位
- PIPECFG、PIPEBUF、PIPEMAXP和PIPEPERI中的位
- PIPEnCTR中的ATREPM、ACLRM、SQCLR和SQSET位
- PIPEnTRE和PIPEnTRN中的位
- DEVADDm中的位（m=0到A）。

要设置DEVADDm中的CSCLR位和位（m=0到A），请按照第33.2节“寄存器”中描述的程序进行操作Descriptions.

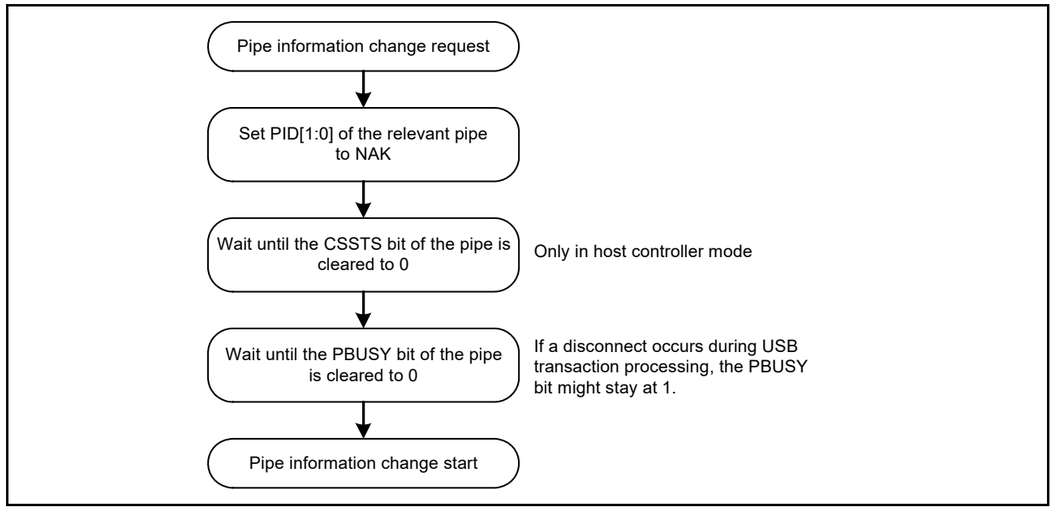


Figure 33.10 Procedure for changing pipe information when USB communication is enabled and PID[1:0] bits are 01b (BUF response)

The following bits in the pipe control registers can be changed only when the selected pipe information is not set in the CURPIPE[3:0] bits in CFIFOSEL, D0FIFOSEL, and D1FIFOSEL.

Do not set the following registers while the CURPIPE[3:0] bits are set:

- Bits in DCPCFG and DCPMAXP
- Bits in PIPECFG, PIPEBUF, PIPEMAXP, and PIPEPERI
- PIPEnCTR and ACLRM bits.

To change pipe information, you must set the CURPIPE[3:0] bits to a pipe other than the one to be changed. For the DCP, the buffer must be cleared using the BCLR bit after the pipe information is changed.

33.3.7.2 Transfer types

The PIPECFG.TYPE[1:0] bits specify the following transfer types for each pipe:

- DCP: No setting necessary (fixed at control transfer)
- Pipes 1 and 2: Set to bulk transfer or isochronous transfer
- Pipes 3 to 5: Set to bulk transfer
- Pipes 6 to 9: Set to interrupt transfer.

33.3.7.3 Endpoint number

The PIPECFG.EPNUM[3:0] bits are used to set the endpoint number for each pipe. The DCP is fixed at endpoint 0. The other pipes can be set from endpoint 1 to 15.

- DCP: No setting is necessary (fixed at endpoint 0)
- Pipes 1 to 9: Select and set the endpoint numbers from 1 to 15 so that the combination of the PIPECFG.DIR and EPNUM[3:0] bits is unique.

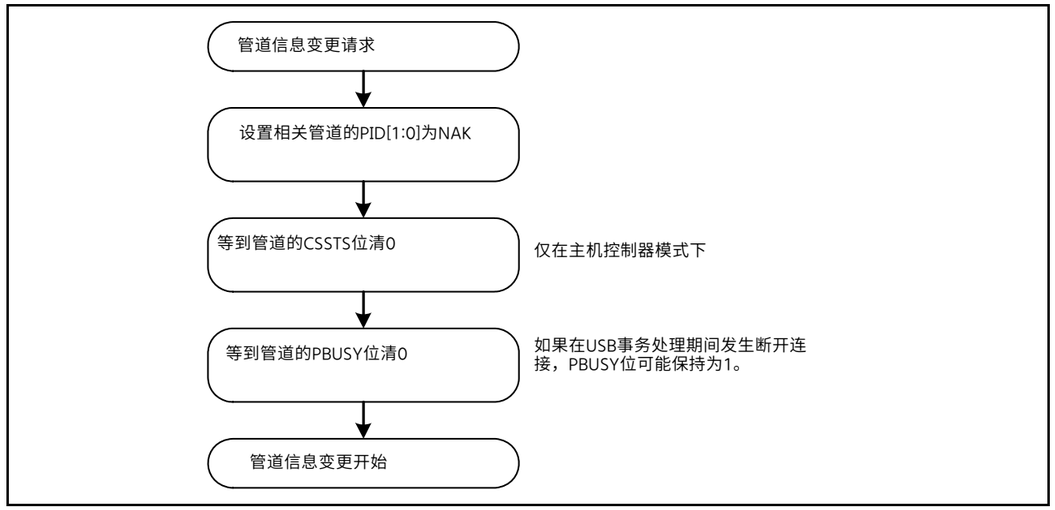


Figure 33.10 USB通信启用且PID[1:0]位为01b（BUF响应）时更改管道信息的过程

管道控制寄存器中的以下位只有在所选管道信息未设置时才能更改CFIFOSEL、D0FIFOSEL和D1FIFOSEL中的CURPIPE[3:0]位。

设置CURPIPE[3:0]位时不要设置以下寄存器：

- DCPCFG和DCPMAXP中的位
- PIPECFG、PIPEBUF、PIPEMAXP和PIPEPERI中的位
- PIPEnCTR和ACLRM位。

要更改管道信息，您必须将CURPIPE[3:0]位设置为要更改的管道以外的管道。对于DCP，必须在管道信息更改后使用BCLR位清除缓冲区。

33.3.7.2 传输类型

PIPECFG.TYPE[1:0]位为每个管道指定以下传输类型：

- DCP：无需设置（控制转移时固定）
- 管道1和2：设置为批量传输或同步传输
- 管道3到5：设置为批量传输
- 管道6到9：设置为中断传输。

33.3.7.3 端点编号

PIPECFG.EPNUM[3:0]位用于设置每个管道的端点编号。DCP固定在端点0。其他管道可以设置从端点1到15。

- DCP：无需设置（固定在端点0）
- 管道1到9：选择并设置从1到15的端点编号，以便PIPECFG.DIR和EPNUM[3:0]位是唯一的。

33.3.7.4 Maximum packet size setting

Specify the maximum packet size for each pipe in the MXPS bits in DCPMAXP and PIPEMAXP. The DCP and pipes 1 to 5 can be set to any of the maximum pipe sizes defined in the USB 2.0 specification. For pipes 6 to 9, the maximum packet size is 64 bytes. Set the maximum packet size as follows before starting a transfer (PID[1:0] bits are set to 01b (BUF response)):

- DCP: Set to 64 for high-speed operation
- DCP: Set to 8, 16, 32, or 64 for full-speed operation
- Pipes 1 to 5: Set to 512 for high-speed bulk transfers
- Pipes 1 to 5: Set to 8, 16, 32, or 64 for full-speed bulk transfers
- Pipes 1, 2: Set between 1 and 1024 for high-speed isochronous transfers
- Pipes 1, 2: Set between 1 and 1023 for full-speed isochronous transfers
- Pipes 6 to 9: Set between 1 and 64.

High-bandwidth interrupt transfers and isochronous transfers are not supported.

33.3.7.5 Transaction counter for pipes 1 to 5 in the receiving direction

When the specified number of transactions is complete in the data packet receiving direction, the USBHS recognizes that the transfer has ended. Two transaction counters are provided. One is the PIPEnTRN register, which specifies the number of transactions to be executed, and the other is the current counter, which internally counts the number of executed transactions. If the PIPECFG.SHTNAK bit is set to 1, when the current counter value matches the specified number of transactions, the associated PIPEnCTR.PID[1:0] bits are set to 00b (NAK response) and the subsequent transfer is disabled. The transactions can be counted again from the beginning by initializing the current counter of the transaction counter function through the PIPEnTRE.TRCLR bit. The data read from PIPEnTRN differs depending on the PIPEnTRE.TRENB setting as follows:

- The TRENB bit = 0: Specified transaction counter value can be read
- The TRENB bit = 1: Current counter value indicating the internally counted number of executed transactions can be read.

The following constraints apply when working with the TRCLR bit:

- If the transactions are being counted and the PIPEnCTR.PID[1:0] bits are set to 01b (BUF response), the current counter cannot be cleared
- If there is any data left in the buffer, the current counter cannot be cleared.

33.3.7.6 Response PID

Specify the response PID for each pipe in the PID[1:0] bits in DCPCTR and PIPEnCTR. This section describes the USBHS operation with different response PID settings.

(1) Software response PID settings in host controller mode

Select the response PID to specify the execution of transactions as follows:

- NAK setting: Using pipes is disabled and no transactions are executed
- BUF setting: Transactions are executed based on the FIFO buffer state:
  OUT direction: An OUT token is issued if the FIFO buffer contains transmit data.
  IN direction: An IN token is issued if the FIFO buffer is not full and can receive data.
- STALL setting: Using pipes is disabled and no transactions are executed.

Note: Use the SUREQ bit to execute setup transactions for the DCP.

33.3.7.4 最大数据包大小设置

在DCPMAXP和PIPEMAXP的MXPS位中指定每个管道的最大数据包大小。DCP和管道1到5可以设置为USB2.0规范中定义的任何最大管道尺寸。对于管道6到9，最大数据包大小为64字节。在开始传输之前设置最大数据包大小如下（PID[1:0]位设置为01b（BUF响应））：

- DCP：设置为64用于高速运行
- DCP：设置为8、16、32或64以实现全速运行
- 管道1到5：设置为512用于高速批量传输
- 管道1到5：设置为8、16、32或64以实现全速批量传输
- 管道1、2：设置在1到1024之间，用于高速同步传输
- 管道1、2：设置在1和1023之间，用于全速同步传输
- 管道6到9：设置在1到64之间。

不支持高带宽中断传输和同步传输。

33.3.7.5 接收方向上管道1到5的事务计数器

当在数据包接收方向完成指定数量的事务时，USBHS识别传输已结束。提供了两个交易柜台。一个是PIPEnTRN寄存器，它指定要执行的事务数，另一个是当前计数器，它在内部对执行的事务数进行计数。如果PIPECFG.SHTNAK位设置为1，则当当前计数器值与指定的事务数匹配时，相关的PIPEnCTR.PID[1:0]位设置为00b（NAK响应）并禁用后续传输。通过PIPEnTRE.TRCLR位初始化事务计数器功能的当前计数器，事务可以从头开始重新计数。从PIPEnTRN读取的数据因PIPEnTRE.TRENB设置而异，如下所示：

- TRENB位=0：可以读取指定的事务计数器值
- TRENB位=1：可以读取表示内部计数的已执行事务数的当前计数器值。

使用TRCLR位时适用以下约束：

- 如果正在对事务进行计数并且PIPEnCTR.PID[1:0]位设置为01b（BUF响应），则无法清除当前计数器
- 如果缓冲区中还有任何数据，则无法清除当前计数器。

33.3.7.6 响应PID

在DCPCTR和PIPEnCTR的PID[1:0]位中指定每个管道的响应PID。本节介绍具有不同响应PID设置的USBHS操作。

(1) 主机控制器模式下的软件响应PID设置

选择响应PID来指定事务的执行，如下所示：

- NAK设置：禁用使用管道并且不执行任何事务
- BUF设置：根据FIFO缓冲区状态执行事务：
  OUT方向：如果FIFO缓冲区包含发送数据，则发出OUT令牌。
  IN方向：如果FIFO缓冲区未满并且可以接收数据，则发出IN令牌。
- STALL设置：禁用使用管道并且不执行任何事务。

Note: 使用SUREQ位执行DCP的设置事务。

(2) Software response PID settings in device controller mode

Select the response PID to respond as follows to transactions from the host:

- NAK setting: A NAK response is returned to all generated transactions
- BUF setting: A response is returned to transactions based on the FIFO buffer
- STALL setting: A STALL response is returned to all generated transactions.

Note: For setup transactions, an ACK response is always returned, regardless of the PID[1:0] bits setting, and the USB request is stored in the register.

(3) and (4) describe situations in which the USBHS writes to the PID[1:0] bits because of specific transaction results.

(3) Hardware response PID settings in host controller mode

- NAK setting: The PID[1:0] bits are set to 00b (NAK response) in the following cases, and issuing of tokens is automatically stopped:
  - When a non-isochronous transfer is performed and an NRDY interrupt is generated. For details, see section 33.3.6.2, NRDY interrupt.
  - If a short packet is received when the PIPECFG.SHTNAK bit is set to 1 for bulk transfers
  - If transaction counting ends when the SHTNAK bit is set to 1 for bulk transfers.
- BUF setting: The USBHS does not write this setting
- STALL setting: The PID[1:0] bits are set to STALL in the following cases, and issuing of tokens is automatically stopped:
  - When STALL is received in response to a transmitted token
  - When a received data packet exceeds the maximum packet size.

(4) Hardware response PID settings in device controller mode

- NAK setting: The PID[1:0] bits are set to 00b (NAK response) in the following cases, and a NAK response is returned to transactions:
  - When the setup token is received normally (DCP only)
  - If transaction counting ends or a short packet is received when the PIPECFG.SHTNAK bit is set to 1 for bulk transfers.
- BUF setting: The USBHS does not write this setting
- STALL setting: The PID[1:0] bits are set to STALL in the following cases, and a STALL response is returned to transactions:
  - When a received data packet exceeds the maximum packet size
  - When a control transfer sequence error is detected.

33.3.7.7 Data PID sequence bit

The USBHS automatically toggles the sequence bit in the data PID when data is transferred successfully in the control transfer data stage, bulk transfer, and interrupt transfer. The sequence bit of the next data PID to be transmitted can be confirmed with the SQMON bit in DCPCTR and PIPEnCTR. When data is transmitted, the sequence bit toggles on ACK handshake reception. When data is received, the sequence bit toggles on ACK handshake transmission. The SQCLR bit in DCPCTR and the SQSET bit in PIPEnCTR can be used to change the data PID sequence bit.

In device controller mode when control transfers are used, the USBHS automatically sets the sequence bit for stage transitions. DATA1 is returned when the setup stage ends. The sequence bit is not referenced and PID = DATA1 is returned in the status stage. Therefore, no software settings are required. However, in host controller mode when control transfers are used, the sequence bit must be set by software for the stage transitions.

For ClearFeature requests for transmission or reception, the data PID sequence bit must be set by software in both host

(2) 设备控制器模式下的软件响应PID设置

选择响应PID以对来自主机的事务进行如下响应：

- NAK设置：向所有生成的事务返回NAK响应
- BUF设置：根据FIFO缓冲区向事务返回响应
- STALL设置：向所有生成的事务返回一个STALL响应。

Note: 对于设置事务，无论PID[1:0]位设置如何，始终返回ACK响应，并且USB请求存储在寄存器中。

(3)和(4)描述了USBHS由于特定事务结果而写入PID[1:0]位的情况。

(3) 主机控制器模式下的硬件响应PID设置

- NAK设置：在以下情况下，PID[1:0]位设置为00b（NAK响应），并自动停止发出令牌：
  - 当执行非同步传输并产生NRDY中断时。有关详细信息，请参阅第33.3.6.2节，NRDY中断。
  - 如果在PIPECFG.SHTNAK位设置为1以进行批量传输时接收到短数据包
  - 如果在SHTNAK位设置为1以进行批量传输时事务计数结束。
- BUF设置：USBHS不写入此设置
- STALL设置：PID[1:0]位在以下情况下设置为STALL，并且令牌的发行自动停止：
  - 当接收到STALL以响应传输的令牌时
  - 当接收到的数据包超过最大包大小时。

(4) 设备控制器模式下的硬件响应PID设置

- NAK设置：在以下情况下，PID[1:0]位设置为00b（NAK响应），并向事务返回NAK响应：
  - 正常接收设置令牌时（仅DCP）
  - 如果在PIPECFG.SHTNAK位设置为1以进行批量传输时，事务计数结束或收到短数据包。
- BUF设置：USBHS不写入此设置
- STALL设置：PID[1:0]位在以下情况下设置为STALL，并向事务返回STALL响应：
  - 当接收到的数据包超过最大包大小时
  - 当检测到控制传输序列错误时。

33.3.7.7 数据PID序列位

当数据在控制传输数据阶段、批量传输和中断传输中成功传输时，USBHS会自动切换数据PID中的序列位。下一个要发送的数据PID的序列位可以通过DCPCTR和PIPEnCTR中的SQMON位来确认。发送数据时，序列位在ACK握手接收时切换。当接收到数据时，序列位在ACK握手传输上切换。DCPCTR中的SQCLR位和PIPEnCTR中的SQSET位可用于更改数据PID序列位。

在使用控制传输的设备控制器模式下，USBHS自动设置阶段转换的序列位。DATA1在设置阶段结束时返回。不引用序列位，在状态阶段返回PID=DATA1。因此，不需要任何软件设置。但是，在使用控制传输的主机控制器模式下，必须由软件设置序列位以进行阶段转换。

对于发送或接收的ClearFeature请求，数据PID序列位必须由两个主机中的软件设置

and device controller modes.

33.3.7.8 Response PID = NAK function

The USBHS provides a function for disabling pipe operation (PID[1:0] bits are set to 00b (NAK response)) when the final data packet of a transaction is received. The USBHS automatically distinguishes this based on reception of a short packet or the transaction counter. Enable this function by setting the PIPECFG.SHTNAK bit to 1.

When the double buffer mode is being used for the FIFO buffer, using this function enables reception of data packets in transfer units. If pipe operation is disabled, software must enable the pipe again (PID[1:0] bits are set to 01b (BUF response)).

The response PID = NAK function can be used only for bulk transfers.

33.3.7.9 Auto response mode

For bulk transfer pipes (1 to 5), when the PIPEnCTR.ATREPM bit is set to 1, a transition is made to auto response mode. During an OUT transfer (PIPECFG.DIR = 0), OUT-NAK mode is invoked, and during an IN transfer (DIR = 1), null auto response mode is invoked.

33.3.7.10 OUT-NAK mode

For bulk OUT transfer pipes, NAK is returned in response to an OUT token, and an NRDY interrupt is output when the PIPEnCTR.ATREPM bit is set to 1. To transition from normal mode to OUT-NAK mode, specify OUT-NAK mode while pipe operation is disabled (PID[1:0] = 00b for NAK response). Next, enable pipe operation (PID[1:0] = 01b for BUF response), on which OUT-NAK mode becomes valid. If an OUT token is received immediately before pipe operation is disabled, the token data is normally received, and an ACK is returned to the host.

To transition from OUT-NAK mode to normal mode, cancel OUT-NAK mode while pipe operation is disabled (NAK). Next enable pipe operation (BUF). In normal mode, reception of OUT data is enabled.

33.3.7.11 Null auto response mode

For bulk IN transfer pipes, zero-length packets are continuously transmitted when the PIPEnCTR.ATREPM bit is set to 1.

To transition from normal mode to null auto response mode, specify null auto response mode while pipe operation is disabled (PID[1:0] bits are set to 00b (NAK response)). Next, enable pipe operation (PID[1:0] bits are set to 01b (BUF response)), on which null auto response mode becomes valid. Before setting null auto response mode, check that PIPEnCTR.INBUFM = 0, because the mode can be set only when the buffer is empty. If the INBUFM bit is 1, empty the buffer using the PIPEnCTR.ACLRM bit. Do not write data from the FIFO port while a transition to null auto response mode is being made.

To transition from null auto response mode to normal mode, keep pipe operation disabled (PID[1:0] bits are set to 00b (NAK response)) for the period of the zero-length packet transmission (about 10 µs) before canceling the null auto response mode. In normal mode, data can be written from the FIFO port, so packet transmission to the host is enabled by enabling pipe operation (PID[1:0] bits are set to 01b (BUF response)).

33.3.8 FIFO Buffer

The USBHS provides a FIFO buffer for data transfers, and it manages the memory area used for each pipe. The FIFO buffer has two states depending on whether the access right is assigned to the system (CPU side) or the USBHS (SIE side).

33.3.8.1 Buffer status

Table 33.23 and Table 33.24 show the buffer status in the USBHS. The FIFO buffer status can be confirmed using the DCPCTR.BSTS and PIPEnCTR.INBUFM bits. The transfer direction for the FIFO buffer can be specified in the PIPECFG.DIR or CFIFOSEL.ISEL bit (when DCP is selected).

The INBUFM bit is valid for pipes 1 to 5 in the transmitting direction.

When a transmitting pipe uses double buffering, the software can read the BSTS bit to monitor the FIFO buffer status on the CPU side and the INBUFM bit to monitor the FIFO buffer status on the SIE side. When write access to the FIFO port

和设备控制器模式。

33.3.7.8 响应PID=NAK功能

USBHS提供了在接收到事务的最终数据包时禁用管道操作（PID[1:0]位设置为00b（NAK响应））的功能。USBHS根据收到的短数据包或事务计数器自动区分这一点。通过将PIPECFG.SHTNAK位设置为1来启用此功能。

当FIFO缓冲区使用双缓冲区模式时，使用此功能可以接收以传输为单位的数据包。如果禁用管道操作，软件必须再次启用管道（PID[1:0]位设置为01b（BUF响应））。

响应PID=NAK函数只能用于批量传输。

33.3.7.9 自动响应模式

对于批量传输管道（1到5），当PIPEnCTR.ATREPM位设置为1时，将转换到自动响应模式。在OUT传输期间(PIPECFG.DIR=0)，将调用OUT-NAK模式，在IN传输期间(DIR=1)，将调用空自动响应模式。

33.3.7.10 OUT-NAK mode

对于批量OUT传输管道，NAK响应OUT令牌返回，并且当PIPEnCTR.ATREPM位设置为1时输出NRDY中断。要从正常模式转换到OUT-NAK模式，请指定OUT-NAK模式，同时管道操作被禁用（PID[1:0]=00b用于NAK响应）。接下来，启用管道操作（PID[1:0]=01b用于BUF响应），此时OUT-NAK模式变为有效。如果在禁用管道操作之前立即收到OUT令牌，则正常接收令牌数据，并向主机返回ACK。

要从OUT-NAK模式转换到正常模式，请在禁用管道操作(NAK)时取消OUT-NAK模式。
接下来启用管道操作(BUF)。在正常模式下，可以接收OUT数据。

33.3.7.11 空自动响应模式

对于批量IN传输管道，当PIPEnCTR.ATREPM位设置为1时，将连续传输零长度数据包。

要从正常模式转换为空自动响应模式，请在禁用管道操作时指定空自动响应模式（PID[1:0]位设置为00b（NAK响应））。接下来，启用管道操作（PID[1:0]位设置为01b（BUF响应）），此时空自动响应模式变为有效。在设置空自动响应模式之前，请检查PIPEnCTR.INBUFM=0，因为只有在缓冲区为空时才能设置模式。如果INBUFM位为1，则使用PIPEnCTR.ACLRM位清空缓冲区。在转换到空自动响应模式时，不要从FIFO端口写入数据。

要从空自动响应模式转换到正常模式，请在零长度数据包传输期间（约10μs）保持管道操作禁用（PID[1:0]位设置为00b（NAK响应）），然后再取消空自动响应模式。在正常模式下，数据可以从FIFO端口写入，因此通过启用管道操作（PID[1:0]位设置为01b（BUF响应））来启用到主机的数据包传输。

33.3.8 FIFO Buffer

USBHS为数据传输提供FIFO缓冲区，并管理用于每个管道的内存区域。FIFO缓冲区有两种状态，具体取决于访问权限是分配给系统（CPU端）还是USBHS（SIE端）。

33.3.8.1 缓冲状态

表33.23和表33.24显示了USBHS中的缓冲区状态。FIFO缓冲区状态可以使用确认DCPCTR.BSTS和PIPEnCTR.INBUFM位。FIFO缓冲区的传输方向可以在pipecfg.dir或cfifosel.isel位（选择DCP时）。

INBUFM位对传输方向的管道1到5有效。

当传输管道使用双缓冲时，软件可以读取BSTS位来监控CPU侧的FIFO缓冲区状态，以及读取INBUFM位来监控SIE侧的FIFO缓冲区状态。当对FIFO端口进行写访问时

by the CPU or DMA/DTC is slow and the buffer empty status cannot be determined using the BEMP interrupt, the software can use the INBUFM bit to confirm the end of transmission.

Table 33.23 Buffer status indicated in the BSTS flag

ISEL or DIR	BSTS	FIFO buffer status
0 (receiving direction)	0	There is no received data, or data is being received. Reading from the FIFO port is disabled.
0 (receiving direction)	1	There is received data, or a zero-length packet is received. Reading from the FIFO port is allowed. When a zero-length packet is received, reading is not possible and the buffer must be cleared.
1 (transmitting direction)	0	Transmission is not complete. Writing to the FIFO port is disabled.
1 (transmitting direction)	1	Transmission is complete. CPU write is allowed.

Table 33.24 Buffer status indicated in the INBUFM bit

DIR	INBUFM	FIFO buffer status
0 (receiving direction)	Invalid	Invalid
1 (transmitting direction)	0	Transmission is complete. There is no data waiting to be transmitted.
1 (transmitting direction)	1	The FIFO port has written data to the buffer. There is data to be transmitted.

33.3.8.2 FIFO buffer clearing

Table 33.25 shows the methods for clearing the FIFO buffer. The FIFO buffer can be cleared using the BCLR bit in the port control register, DnFIFOSEL.DCLRM, or the PIPEnCTR.ACLRM bit.

Single or double buffering can be selected for pipes 1 to 5 in the PIPECFG.DBLB bit.

Table 33.25 Buffer clearing methods

FIFO buffer clearing mode	Clearing the FIFO buffer on the CPU side	Mode for automatically clearing the FIFO buffer after reading the specified pipe data	Auto buffer clear mode for discarding all received packets
Register used	• CFIFOCTR • DnFIFOCTR	DnFIFOSEL	PIPEnCTR
Bit used	BCLR	DCLRM	ACLRM
Clearing condition	Cleared by writing 1	1: Mode valid 0: Mode invalid.	1: Mode valid 0: Mode invalid.

(1) Auto buffer clear mode function

The USBHS discards all received data packets if the PIPEnCTR.ACLRM bit is set to 1. If a correct data packet is received, the ACK response is returned to the host controller. The auto buffer clear mode function can only be set in the FIFO buffer reading direction.

Setting the ACLRM bit to 1 and then to 0 clears the FIFO buffer of the selected pipe regardless of the access direction. An access cycle of at least 100 ns is required for the internal hardware sequence processing between ACLRM = 1 and ACLRM = 0.

33.3.8.3 FIFO port functions

Table 33.26 shows the settings for the FIFO port functions. In write access, writing data until the maximum packet size is reached automatically enables transmission of the data. To enable transmission before the maximum packet size is reached, set the BVAL flag in the port control register to end writing. To send a zero-length packet, use the BCLR bit to clear the buffer, and then set the BVAL flag to end writing.

由于CPU或DMADTC速度慢且无法使用BEMP中断确定缓冲区空状态，软件可以使用INBUFM位来确认传输结束。

Table 33.23 BSTS标志中指示的缓冲区状态

ISEL或DIR	BSTS	FIFO缓冲区状态
0 (receiving direction)	0	没有接收到数据，或正在接收数据。 禁止从FIFO端口读取。
0 (receiving direction)	1	有接收数据，或接收到零长度数据包。 允许从FIFO端口读取。 当接收到零长度数据包时，无法读取，必须清除缓冲区。
1 (transmitting direction)	0	传输未完成。 禁止写入FIFO端口。
1 (transmitting direction)	1	传输完成。 允许CPU写入。

Table 33.24 INBUFM位中指示的缓冲区状态

DIR	INBUFM	FIFO缓冲区状态
0 (receiving direction)	Invalid	Invalid
1 (transmitting direction)	0	传输完成。 没有等待传输的数据。
1 (transmitting direction)	1	FIFO端口已将数据写入缓冲区。 有数据要传输。

33.3.8.2 FIFO缓冲区清除

表33.25显示了清除FIFO缓冲区的方法。可以使用端口控制寄存器中的BCLR位、DnFIFOSEL.DCLRM或PIPEnCTR.ACLRM位清除FIFO缓冲区。

可以在PIPECFG.DBLB位中为管道1到5选择单缓冲或双缓冲。

Table 33.25 缓冲区清除方法

FIFO缓冲区清除模式	清除CPU端的FIFO缓冲区	读取指定管道数据后自动清除FIFO缓冲区的模式	自动缓冲区清除模式，用于丢弃所有接收到的数据包
注册使用	• CFIFOCTR • DnFIFOCTR	DnFIFOSEL	PIPEnCTR
使用的位	BCLR	DCLRM	ACLRM
清算条件	通过写1清除	1：模式有效0 ：模式无效。	1：模式有效0 ：模式无效。

(1) 自动缓冲清除模式功能

如果PIPEnCTR.ACLRM位设置为1，USBHS将丢弃所有接收到的数据包。如果接收到正确的数据包，则向主机控制器返回ACK响应。自动缓冲区清除模式功能只能在FIFO缓冲区读取方向设置。

无论访问方向如何，将ACLRM位设置为1，然后设置为0都会清除所选管道的FIFO缓冲区。ACLRM=1和之间的内部硬件序列处理需要至少100ns的访问周期
ACLRM = 0.

33.3.8.3 先进先出端口功能

表33.26显示了FIFO端口功能的设置。在写访问中，在达到最大数据包大小之前写入数据会自动启用数据传输。要在达到最大数据包大小之前启用传输，请设置端口控制寄存器中的BVAL标志以结束写入。要发送零长度数据包，请使用BCLR位清除缓冲区，然后设置BVAL标志以结束写入。

In reading, reception of new packets is automatically enabled when all data is read. Data cannot be read when a zero-length packet is received (DTLN[11:0] = 0), so the buffer must be cleared with the BCLR bit. The length of the receive data can be confirmed in the DTLN[11:0] flags in the port control register.

Table 33.26 FIFO port function settings

Register name	Bit name	Description
CFIFOSEL, DnFIFOSEL (n = 0, 1)	RCNT	Selects DTLN[11:0] read mode
	REW	FIFO buffer rewind (re-read, rewrite)
	DCLRM	Automatically clears receive data for a specified pipe after the data is read (only for DnFIFO)
	DREQE	Enables DMA/DTC transfers (only for DnFIFO)
	MBW[1:0]	FIFO port access bit width
	BIGEND	Selects FIFO port endian
	ISEL	FIFO port access direction (only for DCP)
	CURPIPE[3:0]	Selects the current pipe
CFIFOCTR, DnFIFOCTR (n = 0, 1)	BVAL	Ends writing to the FIFO buffer
	BCLR	Clears the FIFO buffer on the CPU side
	DTLN[11:0]	Checks the length of receive data

33.3.8.4 FIFO port selection

Table 33.27 shows the pipes that can be selected with the different FIFO ports. The pipe to be accessed must be selected in the CURPIPE[3:0] bits in the port selection register. After a pipe is selected, the software must check whether the written value can be correctly read from the CURPIPE[3:0] bits. (If the previous pipe number is read, it indicates that the USBHS is modifying the pipe.) Next, the software checks that the FRDY flag in the port control register is 1.

In addition, the software must specify the bus width to be accessed in the MBW[1:0] bits in the port selection register. The FIFO buffer access direction conforms to the PIPECFG.DIR setting. For the DCP only, the ISEL bit in the port selection register determines the direction.

Table 33.27 FIFO port access by pipe

Pipe	Access Method	Port that can be used
DCP	CPU access	CFIFO port register
Pipes 1 to 9	CPU access	CFIFO port register D0FIFO/D1FIFO port register
	DMA/DTC access	D0FIFO/D1FIFO port register

(1) REW bit

It is possible to temporarily stop access to a pipe being accessed, access a different pipe, and then continue processing for the first pipe again. The REW bit in the port selection register is used for this processing.

If a pipe is selected in the CURPIPE[3:0] bits in the port selection register with the REW bit set to 1, the pointer used for reading from and writing to the FIFO buffer is reset, and reading or writing can be carried out from the first byte. If a pipe is selected with the REW bit set to 0, data can be read and written in continuation from the previous selection, without the pointer being reset.

To access the FIFO port, the software must check that the FRDY bit in the port control register is 1 after selecting a pipe.

33.3.8.5 DMA/DTC transfers (D0FIFO and D1FIFO ports)

For pipes 1 to 9, the FIFO port can be accessed using the DMAC/DTC. When buffer access for the pipe targeted for DMA/DTC transfer is enabled, a DMA/DTC transfer request is issued.

Select the unit of transfer to the FIFO port in the DnFIFOSEL.MBW[1:0] bits, and select the pipe targeted for the DMA/DTC transfer in the DnFIFOSEL.CURPIPE[3:0] bits. Do not change the selected pipe during the DMA transfer.

在读取中，当所有数据被读取时，自动启用新数据包的接收。接收到零长度数据包时（DTLN[11:0]=0）无法读取数据，因此必须使用BCLR位清除缓冲区。接收数据的长度可以在端口控制寄存器中的DTLN[11:0]标志中确认。

Table 33.26 FIFO端口功能设置

注册名称	位名称	Description
CFIFOSEL, DnFIFOSEL (n = 0, 1)	RCNT	选择DTLN[11:0]读取模式
	REW	FIFO缓冲区倒带（重新读取、重写）
	DCLRM	读取数据后自动清除指定管道的接收数据（仅适用于DnFIFO）
	DREQE	启用DMADTC传输（仅适用于DnFIFO）
	MBW[1:0]	FIFO端口访问位宽
	BIGEND	选择FIFO端口字节序
	ISEL	FIFO端口访问方向（仅适用于DCP）
	CURPIPE[3:0]	选择当前管道
CFIFOCTR, DnFIFOCTR (n = 0, 1)	BVAL	结束写入FIFO缓冲区
	BCLR	清除CPU端的FIFO缓冲区
	DTLN[11:0]	检查接收数据的长度

33.3.8.4 先进先出端口选择

表33.27显示了可以使用不同FIFO端口选择的管道。必须在端口选择寄存器的CURPIPE[3:0]位中选择要访问的管道。选择管道后，软件必须检查是否可以从CURPIPE[3:0]位正确读取写入的值。（如果读取到之前的管道号，则表明USBHS正在修改管道。）接下来，软件检查端口控制寄存器中的FRDY标志为1。

此外，软件必须在端口选择寄存器的MBW[1:0]位中指定要访问的总线宽度。
FIFO缓冲区访问方向符合PIPECFG.DIR设置。仅对于DCP，端口选择寄存器中的ISEL位决定方向。

Table 33.27 通过管道访问FIFO端口

Pipe	访问方法	可以使用的端口
DCP	CPU访问	CFIFO端口寄存器
管道1至9	CPU访问	CFIFO端口寄存器 D0FIFOD1FIFO端口寄存器
	DMA/DTC access	D0FIFOD1FIFO端口寄存器

(1) REW位

可以暂时停止对正在访问的管道的访问，访问不同的管道，然后再次继续处理第一个管道。端口选择寄存器中的REW位用于此处理。

如果在端口选择寄存器的CURPIPE[3:0]位中选择了一个管道，并且REW位设置为1，则用于读取和写入FIFO缓冲区的指针复位，可以进行读取或写入从第一个字节开始。如果在REW位设置为0的情况下选择了管道，则可以从先前的选择继续读取和写入数据，而无需重置指针。

要访问FIFO端口，软件必须在选择管道后检查端口控制寄存器中的FRDY位是否为1。

33.3.8.5 DMADTC传输（D0FIFO和D1FIFO端口）

对于管道1到9，可以使用DMACDTC访问FIFO端口。当对目标管道进行缓冲区访问时启用DMADTC传输，发出DMADTC传输请求。

在DnFIFOSEL.MBW[1:0]位中选择传输到FIFO端口的单位，并选择目标管道DnFIFOSEL.CURPIPE[3:0]位中的DMADTC传输。在DMA传输期间不要更改选定的管道。

(1) DnFIFO auto clear mode (D0FIFO and D1FIFO port reading direction)

If 1 is set in the DnFIFOSEL.DCLRM bit, the USBHS automatically clears the FIFO buffer of the selected pipe when reading of data from the FIFO buffer is complete.

Table 33.28 shows the packet reception and FIFO buffer clearing processing by software for each of the different settings. As shown in the table, the buffer clearing conditions depend on the value set in the PIPECFG.BFRE bit. Using the DnFIFOSEL.DCLRM bit eliminates the need for the buffer to be cleared by software in any situation that requires buffer clearing. This enables DMA/DTC transfers without involving software.

The DnFIFO auto clear mode can only be set in the FIFO buffer reading direction.

Table 33.28 Packet reception and FIFO buffer clearing processing by software

Buffer status when packet is received	Register setting			
	DCLRM = 0		DCLRM = 1	
	BFRE = 0	BFRE = 1	BFRE = 0	BFRE = 1
Buffer full	No clearing required	No clearing required	No clearing required	No clearing required
Zero-length packet reception	Clearing required	Clearing required	No clearing required	No clearing required
Normal short packet reception	No clearing required	Clearing required	No clearing required	No clearing required
Transaction count end	No clearing required	Clearing required	No clearing required	No clearing required

33.3.8.6 Allocating the FIFO buffer

Figure 33.11 shows an example of a memory map of the FIFO buffer. The FIFO buffer is an area shared by the USBHS and the control CPU of the application. There are two situations for the FIFO buffer: (1) access rights are given to the application (CPU side), and (2) access rights are given to the USBHS (SIE side).

An independent area is set for the FIFO buffer for each pipe. A memory area is determined by the first block number and the number of blocks (specified in the BUFNMB[7:0] and BUFSIZE[4:0] bits in PIPEBUF), where 64 bytes is regarded as one block. When the continuous transfer mode is selected in the CNTMD bit in PIPECFG, set the BUFSIZE[4:0] bits to an integral multiple of the maximum packet size. When double buffering is selected in the DBLB bit in PIPECFG, twice the memory area specified in the BUFSIZE[4:0] bits in PIPEBUF is allocated to the same pipe.

Three FIFO ports are used to access (read data from and write data to) the FIFO buffer. Specify the number of the pipe to be allocated to the FIFO port in the CURPIPE[3:0] bits in C/DnFIFOSEL.

The FIFO buffer status of each pipe can be checked in the DCPCTR.BSTS, PIPEnCTR, and INBUFM bits. The FIFO port access rights can be checked in the FRDY flag in C/DnFIFOCTR.

(1) DnFIFO自动清除模式（D0FIFO和D1FIFO端口读取方向）

如果DnFIFOSEL.DCLRM位设置为1，USBHS会在从FIFO缓冲区读取数据完成时自动清除所选管道的FIFO缓冲区。

表33.28显示了软件对每个不同设置的数据包接收和FIFO缓冲区清除处理。如表所示，缓冲区清除条件取决于PIPECFG.BFRE位中设置的值。使用DnFIFOSEL.DCLRM位无需在任何需要清除缓冲区的情况下通过软件清除缓冲区。这可以在不涉及软件的情况下实现DMADTC传输。

DnFIFO自动清除模式只能设置在FIFO缓冲区读取方向。

Table 33.28 通过软件进行数据包接收和FIFO缓冲区清除处理

收到数据包时的缓冲区状态	注册设置			
	DCLRM = 0		DCLRM = 1	
	BFRE = 0	BFRE = 1	BFRE = 0	BFRE = 1
缓冲区已满	无需清算	无需清算	无需清算	无需清算
零长度数据包接收	需要清算	需要清算	无需清算	无需清算
正常短包接收	无需清算	需要清算	无需清算	无需清算
交易计数结束	无需清算	需要清算	无需清算	无需清算

33.3.8.6 分配FIFO缓冲区

图33.11显示了FIFO缓冲区的内存映射示例。FIFO缓冲区是由USBHS和应用程序的控制CPU共享的区域。FIFO缓冲区有两种情况：（1）访问权限给应用程序（CPU端），（2）访问权限给USBHS（SIE端）。

为每个管道的FIFO缓冲区设置一个独立的区域。内存区域由第一个块号和块数（在PIPEBUF中的BUFNMB[7:0]和BUFSIZE[4:0]位指定）确定，其中64个字节被视为一个块。在PIPECFG的CNTMD位中选择连续传输模式时，将BUFSIZE[4:0]位设置为最大数据包大小的整数倍。当在PIPECFG的DBLB位中选择双缓冲时，PIPEBUF中的BUFSIZE[4:0]位指定的内存区域的两倍将分配给同一管道。

三个FIFO端口用于访问（读取数据和写入数据）FIFO缓冲区。在CDnFIFOSEL的CURPIPE[3:0]位中指定要分配给FIFO端口的管道编号。

可以在DCPCTR.BSTS、PIPEnCTR和INBUFM位中检查每个管道的FIFO缓冲区状态。可以在CDnFIFOCTR中的FRDY标志中检查FIFO端口访问权限。

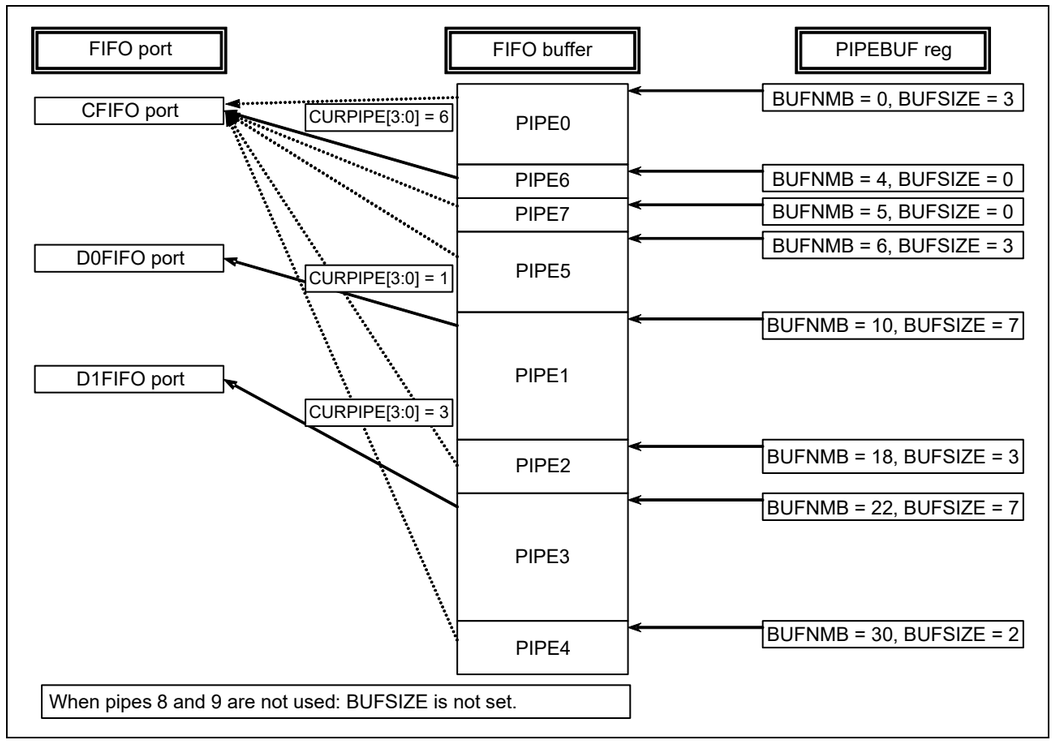


Figure 33.11 Example memory map of the FIFO buffer

33.3.9 Control Transfers Using the DCP

The Default Control Pipe (DCP) is used for data transfers in the control transfer data stage. The FIFO buffer of the DCP is a 64-byte single buffer with a fixed area for both control reads and control writes. The FIFO buffer can be accessed only through the CFIFO port.

33.3.9.1 Control transfers in host controller mode

(1) Setup stage

The USBREQ, USBVAL, USBINDX, and USBLENG registers are used to transmit USB requests for setup transactions. Writing the setup packet data to the register and then writing 1 to the DCPCTR.SUREQ bit transmits the specified data for the setup transaction. On completion of the transaction, the SUREQ bit clears to 0. Do not change these USB request registers while SUREQ = 1.

When an attached function device is detected, the software must issue the first setup transaction for the device using this sequence with the DCPMAXP.DEVSEL[3:0] bits cleared to 0 and the DEVADD0.USBSPD[1:0] bits set appropriately.

When an attached function device is shifted to the Address state, the software must issue setup transactions using this sequence with the assigned USBAddress set in the DEVSEL[3:0] bits and the bits in DEVADDm (m = 0 to A) corresponding to the specified USBAddress set appropriately. For example, when PIPEMAXP.DEVSEL[3:0] = 0010b, make appropriate settings in DEVADD2. When PIPEMAXP.DEVSEL[3:0] = 0101b, make appropriate settings in DEVADD5.

When the setup transaction data is sent, an interrupt request is generated based on the response from the peripheral device (SIGN or SACK bit in INTSTS1). This interrupt request allows the software to check the setup transaction result.

The DATA0 data packet (USB request) for the setup transaction is always transmitted regardless of the status of the DCPCTR.SQMON flag.

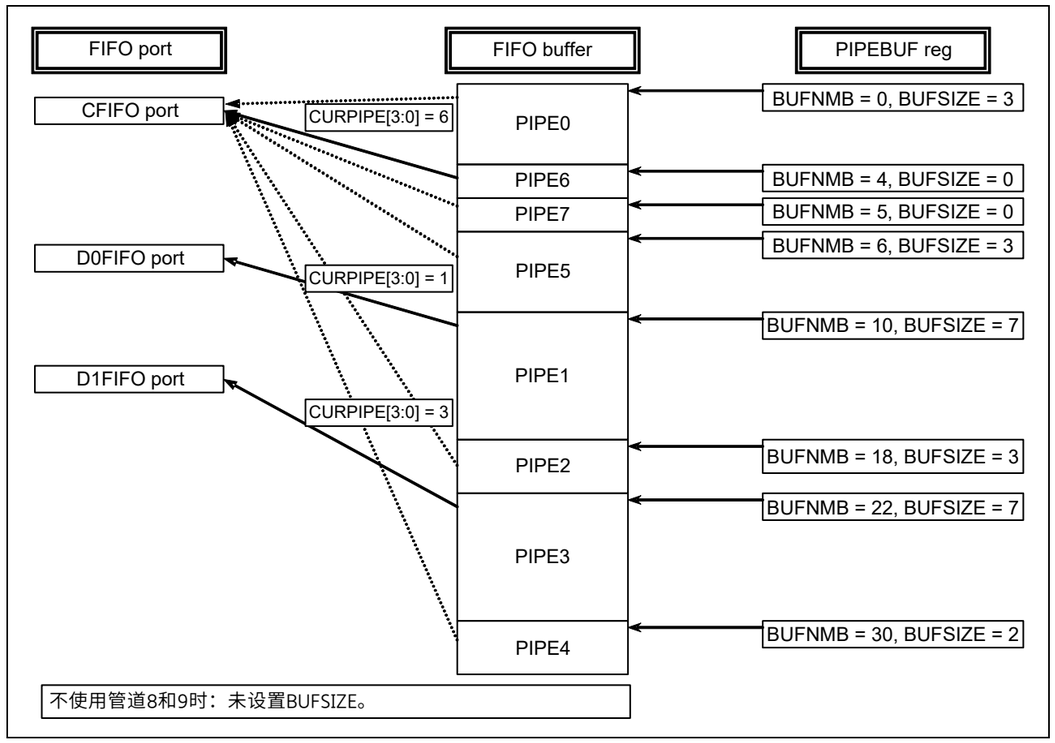


Figure 33.11 FIFO缓冲区的示例内存映射

33.3.9 使用DCP进行控制传输

默认控制管道(DCP)用于控制传输数据阶段的数据传输。DCP的FIFO缓冲区是一个64字节的单缓冲区，具有用于控制读取和控制写入的固定区域。FIFO缓冲区只能通过CFIFO端口访问。

33.3.9.1 主机控制器模式下的控制传输

(1) 设置阶段

USBREQ、USBVAL、USBINDX和USBLENG寄存器用于传输设置事务的USB请求。将设置数据包数据写入寄存器，然后向DCPCTR.SUREQ位写入1，以传输设置事务的指定数据。事务完成后，SUREQ位清除为0。在SUREQ=1时不要更改这些USB请求寄存器。

当检测到连接的功能器件时，软件必须使用此序列为器件发出第一个设置事务，其中DCPMAXP.DEVSEL[3:0]位清零，DEVADD0.USBSPD[1:0]位适当设置。

当连接的功能器件转移到地址状态时，软件必须使用此序列发出设置事务，其中指定的USBAddress设置在DEVSEL[3:0]位和DEVADDm中的位（m=0到A）对应于指定的USBAddress设置得当。例如，当PIPEMAXP.DEVSEL[3:0]=0010b时，在DEVADD2中进行适当的设置。当PIPEMAXP.DEVSEL[3:0]=0101b时，在DEVADD5中进行适当的设置。

发送设置事务数据时，根据外围设备的响应（INTSTS1中的SIGN或SACK位）生成中断请求。该中断请求允许软件检查设置事务结果。

用于设置事务的DATA0数据包（USB请求）始终被传输，无论
DCPCTR.SQMON flag.

(2) Data stage

The data stage is used to transfer data using the DCP FIFO buffer.

Before accessing the DCP FIFO buffer, specify the access direction in the CFIFOSEL.ISEL bit. Specify the transfer direction in the DCPCFG.DIR bit.

For the first data packet of the data stage, the data PID must be transferred as DATA1. Set data PID to DATA1 in the DCPCTR.SQSET bit and set the PID[1:0] bits to 01b (BUF response). Completion of data transfer is detected using the BRDY or BEMP interrupt.

Data transfer of multiple packets is enabled in continuous transfer mode. However, when continuous transfer is specified in the receiving direction, the BRDY interrupt is not generated unless the buffer becomes full or a short packet is received (for 256 bytes or less, which is an integral multiple of the maximum packet size). If the transmit data size is an integral multiple of the maximum packet size, control the control write transfer through the software to transmit a zero-length packet last.

(3) Status stage

The status stage is used for zero-length packet data transfers in the reverse direction of the data stage. As in the data stage, data is transfered using the DCP FIFO buffer. Transactions are executed using the same procedure as the data stage.

Data packets in the status stage must be transmitted and received with the data PID set to DATA1 using the DCPCTR.SQSET bit.

When a zero-length packet is received, check the receive-data length in the CFIFOCTR.DTLN[11:0] flags after a BRDY interrupt is generated, and then clear the FIFO buffer using the BCLR bit.

33.3.9.2 Control transfers in device controller mode

(1) Setup stage

The USBHS returns an ACK response to a normal setup packet for the USBHS. The USBHS operates in the setup stage as follows:

On receiving a new setup packet, the USBHS sets the following bits:

- Sets the INTSTS0.VALID flag to 1
- Sets the DCPCTR.PID[1:0] bits to 00b (NAK response)
- Sets the DCPCTR.CCPL bit to 0.

When the USBHS receives a data packet following a setup packet, it stores the USB request parameters in USBREQ, USBVAL, USBINDX, and USBLENG.

Before performing the response processing for a control transfer, set the VALID flag to 0. When the VALID flag = 1, the PID[1:0] bits cannot be set to 01b (BUF response), and the data stage cannot be terminated.

Using the VALID flag function, the USBHS can suspend a request being processed when it receives a new USB request during a control transfer and return a response to the latest request.

In addition, the USBHS automatically detects the direction bit (bmRequestType bit 8) and the request data length (wLength) in the received USB request. It distinguishes between control read transfers, control write transfers, and no-data control transfers, and it controls stage transitions. For an incorrect sequence, a sequence error occurs in the control transfer stage transition interrupt, and the interrupt is reported to the software. For a diagram of the stage control by the USBHS, see Figure 33.9.

(2) Data stage

The DCP must be used to execute data transfers for received USB requests. Before accessing the DCP FIFO buffer, specify the access direction in the CFIFOSEL.ISEL bit.

If the transfer data is larger than the size of the DCP FIFO buffer, execute the data transfer using the BRDY interrupt for control write transfers and the BEMP interrupt for control read transfers.

In high-speed control write transfers, a NYET handshake response is returned based on the FIFO buffer status.

(2) 数据阶段

数据级用于使用DCPFIFO缓冲区传输数据。

在访问DCPFIFO缓冲区之前，请在CFIFOSEL.ISEL位中指定访问方向。在DCPCFG.DIR位中指定传输方向。

对于数据阶段的第一个数据包，数据PID必须作为DATA1传输。将数据PID设置为DATA1 DCPCTR.SQSET位并将PID[1:0]位设置为01b（BUF响应）。使用检测到数据传输的完成 BRDY或BEMP中断。

在连续传输模式下启用多个数据包的数据传输。但是，当在接收方向指定连续传输时，除非缓冲区变满或接收到短数据包（256字节或更少，这是最大数据包大小的整数倍），否则不会产生BRDY中断。如果传输数据大小是最大数据包大小的整数倍，则通过软件控制控制写入传输，最后传输一个零长度数据包。

(3) 状态阶段

状态阶段用于在数据阶段的相反方向上进行零长度分组数据传输。与数据阶段一样，使用DCPFIFO缓冲区传输数据。事务使用与数据阶段相同的过程执行。

状态阶段的数据包必须在数据PID设置为DATA1的情况下使用 DCPCTR.SQSET bit.

当接收到零长度数据包时，在产生BRDY中断后检查CFIFOCTR.DTLN[11:0]标志中的接收数据长度，然后使用BCLR位清除FIFO缓冲区。

33.3.9.2 设备控制器模式下的控制传输

(1) 设置阶段

USBHS向USBHS的正常设置数据包返回ACK响应。USBHS在设置阶段运行如下：

在接收到新的设置数据包时，USBHS设置以下位：

- 将INTSTS0.VALID标志设置为1
- 将DCPCTR.PID[1:0]位设置为00b（NAK响应）
- 将DCPCTR.CCPL位设置为0。

当USBHS在设置包之后接收到数据包时，它会将USB请求参数存储在USBREQ中， USBVAL, USBINDX, and USBLENG.

在执行控制传输的响应处理之前，将VALID标志设置为0。当VALID标志=1时， PID[1:0]位不能设置为01b（BUF响应），并且不能终止数据阶段。

使用VALID标志功能，USBHS可以在控制传输期间接收到新的USB请求时暂停正在处理的请求，并返回对最新请求的响应。

此外，USBHS会自动检测接收到的USB请求中的方向位（bmRequestTypebit8）和请求数据长度（wLength）。它区分控制读取传输、控制写入传输和无数据控制传输，并控制阶段转换。对于不正确的序列，在控制转移阶段转换中断中发生序列错误，并将中断报告给软件。有关USBHS的舞台控制图，请参见图33.9。

(2) 数据阶段

DCP必须用于执行接收到的USB请求的数据传输。在访问DCPFIFO缓冲区之前，请在CFIFOSEL.ISEL位中指定访问方向。

如果传输数据大于DCPFIFO缓冲区的大小，则使用控制写传输的BRDY中断和控制读传输的BEMP中断执行数据传输。

在高速控制写入传输中，根据FIFO缓冲区状态返回NYET握手响应。

(3) Status stage

Control transfers are terminated by setting the DCPCTR.CCPL bit to 1 while the DCPCTR.PID[1:0] bits are set to 01b (BUF response).

After this setting is made, the USBHS automatically executes the status stage based on the data transfer direction determined at the setup stage. The status stage is executed as follows:

- For control read transfers:
  The USBHS receives a zero-length packet from the USB host and transmits an ACK response
- For control write transfer and no data control transfer:
  The USBHS transmits a zero-length packet and receives an ACK response from the USB host.

(4) Control transfer auto response function

The USBHS automatically responds to a normal SET_ADDRESS request. If the SET_ADDRESS request contains any of the following errors, a response must be returned by software.

- When bmRequestType is not 00h: except control write transfer
- When wIndex is not 00h: request error
- When wLength is not 00h: except no data control transfer
- When wValue is larger than 7Fh: request error
- When PL1CTRL.DVSQ[3:0] flags are 0011b (Configured): control transfer of device state error

A response by the corresponding software is required to all requests other than SET_ADDRESS.

33.3.10 Bulk Transfers (Pipes 1 to 5)

The FIFO buffer usage (setting of single buffer/double buffer or continuous/discontinuous transfer mode) is configurable for bulk transfers. The FIFO buffer size can be set up to 2 KB. The USBHS manages the FIFO buffer state and automatically responds to the PING packet and the NYET handshake.

33.3.10.1 PING packet control in host controller mode

In the OUT direction, a PING packet is automatically transmitted by the USBHS. The USBHS starts communication in the transmitting direction beginning with the PING packet. When it receives an ACK handshake in response to the PING packet, the USBHS transmits an OUT packet. The USBHS returns to the PING transmission state on receiving a NAK or NYET response during an OUT transaction. The procedure is as follows:

Starting OUT data transmission
(1) Transmit PING packet
(2) Receive NAK handshake
(3) Transmit PING packet
(4) Receive ACK handshake
(5) Transmit OUT data packet
(6) Receive ACK handshake
(7) Transmit OUT data packet
:
(8) Receive NAK/NYET handshake

The USBHS returns to the PING packet transmission state when a hardware reset is issued, the NYET or NAK handshake is received, the sequence toggle bit is cleared (SQCLR), or the buffer clear bit (ACLRM) is set.

33.3.10.2 NYET handshake control in device controller mode

Table 33.29 lists responses to received tokens during bulk and control transfers. The USBHS returns a NYET response

(3) 状态阶段

通过将DCPCTR.CCPL位设置为1而将DCPCTR.PID[1:0]位设置为01b（BUF响应）来终止控制传输。

完成此设置后，USBHS根据设置阶段确定的数据传输方向自动执行状态阶段。状态阶段执行如下：

- 对于控制读取传输：
  USBHS接收来自USB主机的零长度数据包并发送ACK响应
- 对于控制写传输和无数据控制传输：
  USBHS发送一个长度为零的数据包并接收来自USB主机的ACK响应。

(4) 控制转移自动响应功能

USBHS自动响应正常的SET_ADDRESS请求。如果SET_ADDRESS请求包含以下任何错误，则必须由软件返回响应。

- bmRequestType不为00h时：控制写入传输除外
- wIndex不为00h时：请求错误
- wLength不为00h时：除非没有数据控制传输
- wValue大于7Fh时：请求错误
- 当PL1CTRL.DVSQ[3:0]标志为0011b（已配置）时：设备状态错误的控制传输

除SET_ADDRESS之外的所有请求都需要相应软件的响应。

33.3.10 批量传输（管道1到5）

FIFO缓冲区使用（设置单缓冲区双缓冲区或连续不连续传输模式）可配置为批量传输。FIFO缓冲区大小可设置为2KB。USBHS管理FIFO缓冲区状态并自动响应PING数据包和NYET握手。

33.3.10.1 主机控制器模式下的PING包控制

在OUT方向，USBHS自动发送一个PING数据包。USBHS从PING数据包开始在传输方向上开始通信。当它接收到响应PING数据包的ACK握手时，USBHS发送一个OUT数据包。USBHS在OUT事务期间收到NAK或NYET响应后返回PING传输状态。程序如下：

开始OUT数据传输
(1)发送PING包
(2)接收NAK握手
(3)发送PING包
(4)接收ACK握手
(5)发送OUT数据包
(6)接收ACK握手
(7)发送OUT数据包
:
(8)接收NAKNYET握手

当发出硬件复位、接收到NYET或NAK握手、清除序列切换位(SQCLR)或设置缓冲区清除位(ACLRM)时，USBHS将返回PING数据包传输状态。

33.3.10.2 设备控制器模式下的NYET握手控制

表33.29列出了在批量和控制传输期间对接收到的令牌的响应。USBHS返回NYET响应

when an available area for only one packet is left in the FIFO buffer when the USBHS has received an OUT token during a bulk or control transfer. When the USBHS receives a short packet, however, it returns an ACK response instead of NYET even when this condition occurs.

Table 33.29 Responses to received tokens

PID[1:0] bit setting	FIFO buffer state	Received token	Response	Note
NAK/STALL	—	SETUP	ACK	—
	—	IN/OUT/PING	NAK/STALL	—
BUF	—	SETUP	ACK	—
	RCV-BRDY	OUT/PING	ACK	When OUT token is received, data packet is received.*1
	RCV-BRDY	OUT	NYET	Data packet is received*2
	RCV-BRDY	OUT (Short)	ACK	Data packet is received*2
	RCV-BRDY	PING	ACK	*2
	RCV-NRDY	OUT/PING	NAK	—
	TRN-BRDY	IN	DATA0/1	Data packet is transmitted
	TRN-NRDY	IN	NAK	—

Note 1. RCV-BRDY: An available area for two packets is left in the FIFO buffer when an OUT token or a PING token is received.
Note 2. RCV-BRDY: An available area for only one packet is left in the FIFO buffer when an OUT token is received.
RCV-NRDY: No available area is left in the FIFO buffer when a PING token is received.
TRN-BRDY: The FIFO buffer contains transmit data when an IN token is received.
TRN-NRDY: The FIFO buffer contains no transmit data when an IN token is received.

33.3.11 Interrupt Transfers (Pipes 6 to 9)

In device controller mode, the USBHS performs interrupt transfers based on the timing dictated by the host controller. In the interrupt transfer, the USBHS ignores PING packets (no response) and does not transmit the NYET handshake, but returns an ACK, NAK, or STALL response.

In host controller mode, the software can set the timing for issuing tokens using the interval counter. The USBHS does not issue a PING token but issues an OUT token, including for transfers in the OUT direction.

The USBHS does not support high-bandwidth interrupt transfers.

33.3.11.1 Interval counter for interrupt transfers in host controller mode

Specify the transaction interval for interrupt transfers in the PIPEPERI.IITV[2:0] bits. The USBHS issues interrupt transfer tokens based on this interval.

(1) Initializing the counter

The USBHS initializes the interval counter under the following conditions:

- Power-on reset:
  This initializes the IITV[2:0] bits
- FIFO buffer initialization using the PIPEnCTR.ACLRM bit:
  This does not initialize the IITV[2:0] bits, but does initialize the count value. Setting the PIPEnCTR.ACLRM bit to 0 starts counting from the value set in IITV[2:0].

(2) Operation when tokens cannot be transmitted or received even on token generation

No token is generated in the following cases even at token generation time. In these cases, the USBHS tries to execute the transaction in the next interval.

- When the PID[1:0] bits are set to NAK or STALL
- When the FIFO buffer is full at token transmit time in the receiving (IN) direction
- When there is no data to be transmitted in the FIFO buffer at token transmit time in the transmitting (OUT)

当USBHS在批量传输或控制传输期间接收到OUT令牌时，FIFO缓冲区中只剩下一个数据包的可用区域。但是，当USBHS接收到一个短数据包时，即使发生这种情况，它也会返回ACK响应而不是NYET。

Table 33.29 对收到的令牌的响应

PID[1:0]位设置	先进先出缓冲器状态	收到令牌	Response	Note
NAK/STALL	—	SETUP	ACK	—
	—	IN/OUT/PING	NAK/STALL	—
BUF	—	SETUP	ACK	—
	RCV-BRDY	OUT/PING	ACK	接收到OUT令牌时，接收数据包。*1
	RCV-BRDY	OUT	NYET	收到数据包*2
	RCV-BRDY	OUT (Short)	ACK	收到数据包*2
	RCV-BRDY	PING	ACK	*2
	RCV-NRDY	OUT/PING	NAK	—
	TRN-BRDY	IN	DATA0/1	传输数据包
	TRN-NRDY	IN	NAK	—

Note 1. RCV-BRDY：当接收到OUT令牌或PING令牌时，FIFO缓冲区中留有两个数据包的可用区域。
Note 2. RCV-BRDY：当接收到OUT令牌时，FIFO缓冲区中只剩下一个数据包的可用区域。
RCV-NRDY：接收到PING令牌时，FIFO缓冲区中没有可用区域。
TRN-BRDY：接收到IN令牌时，FIFO缓冲区包含发送数据。
TRN-NRDY：接收到IN令牌时，FIFO缓冲区不包含发送数据。

33.3.11 中断传输（管道6到9）

在设备控制器模式下，USBHS根据主机控制器规定的时序执行中断传输。在中断传输中，USBHS忽略PING数据包（无响应）并且不发送NYET握手，而是返回ACK、NAK或STALL响应。

在主机控制器模式下，软件可以使用间隔计数器设置发布令牌的时间。USBHS不会发出PING令牌，但会发出OUT令牌，包括用于OUT方向的传输。

USBHS不支持高带宽中断传输。

33.3.11.1 主机控制器模式下中断传输的间隔计数器

在PIPEPERI.IITV[2:0]位中指定中断传输的事务间隔。USBHS基于此间隔发出中断传输令牌。

(1) 初始化计数器

USBHS在以下条件下初始化间隔计数器：

- Power-on reset:
  这将初始化IITV[2:0]位
- 使用PIPEnCTR.ACLRM位初始化FIFO缓冲区：
  这不会初始化IITV[2:0]位，但会初始化计数值。将PIPEnCTR.ACLRM位设置为0从IITV[2:0]中设置的值开始计数。

(2) 即使在生成令牌时也无法发送或接收令牌时的操作

在以下情况下，即使在生成令牌时也不会生成令牌。在这些情况下，USBHS尝试在下一个时间间隔执行事务。

- 当PID[1:0]位设置为NAK或STALL
- 当FIFO缓冲区在接收(IN)方向的令牌传输时间已满时
- 当在发送(OUT)中的令牌发送时间FIFO缓冲区中没有要发送的数据时

direction.

33.3.12 Isochronous Transfers (Pipes 1 and 2)

The USBHS does not support high-bandwidth isochronous transfers but provides the following functions for isochronous transfers:

- Notification of isochronous transfer error
- Interval counter (specified in the PIPEPERI.IITV[2:0] bits)
- Isochronous IN transfer data setup control (IDLY function)
- Isochronous IN transfer buffer flush function (specified in the PIPEPERI.IFIS bit)
- SOF pulse output function.

33.3.12.1 Error detection in isochronous transfers

The USBHS provides a function for detecting the errors described in this section, so that when errors occur in isochronous transfers, they can be controlled by software. Table 33.30 and Table 33.31 show the priority order for errors detected by the USBHS and the associated interrupts.

(1) PID errors

- The PID value of the received packet is invalid.

(2) CRC errors and bit stuffing errors

- A CRC error is found in a received packet or the bit stuffing is illegal.

(3) Maximum packet size exceeded

- The data size of the received packet exceeds the specified maximum packet size.

(4) Overrun and underrun errors

In host controller mode:

- The FIFO buffer is full at token transmit time in the IN (receiving) direction
- There is no data to be sent in the FIFO buffer at token transmit time in the OUT (transmitting) direction.

In device controller mode:

- There is no data to be sent in the FIFO buffer at token receive time in the IN (transmitting) direction
- The FIFO buffer is full at token receive time in the OUT (receiving) direction.

(5) Interval error

In device controller mode, the following cases are treated as an interval error:

- Failure to receive an IN token in the interval frame during an isochronous IN transfer
- Failure to receive an OUT token in the interval frame during an isochronous OUT transfer.

Table 33.30 Error detection for token transmission and reception (1 of 2)

Detection priority	Error type	Interrupt generated at error detection and status
1	PID error	No interrupts are generated in either host or device controller mode. (Ignored as a corrupted packet.)
2	CRC or bit stuffing error	No interrupts are generated in either host or device controller mode. (Ignored as a corrupted packet.)
3	Overrun or underrun error	An NRDY interrupt is generated to set the OVRN flag to 1 in both host and device controller modes. In device controller mode, a zero-length packet is transmitted in response to an IN token. No data packets are received in response to the OUT token.

direction.

33.3.12 同步传输（管道1和2）

USBHS不支持高带宽同步传输，但为同步传输提供以下功能：

- 同步传输错误通知
- 间隔计数器（在PIPEPERI.IITV[2:0]位中指定）
- 同步IN传输数据设置控制（IDLY功能）
- 同步IN传输缓冲区刷新功能（在PIPEPERI.IFIS位中指定）
- SOF脉冲输出功能。

33.3.12.1 同步传输中的错误检测

USBHS提供了检测本节描述的错误的功能，因此当同步传输中出现错误时，可以通过软件进行控制。表33.30和表33.31显示了USBHS检测到的错误和相关中断的优先级顺序。

(1) PID错误

- 接收到的数据包的PID值无效。

(2) CRC错误和位填充错误

- 在收到的数据包中发现CRC错误或比特填充是非法的。

(3) 超出最大数据包大小

- 接收到的数据包的数据大小超过了指定的最大数据包大小。

(4) 溢出和欠载错误

在主机控制器模式下：

- FIFO缓冲区在IN（接收）方向的令牌发送时间已满
- 在OUT（发送）方向的令牌发送时，FIFO缓冲区中没有要发送的数据。

在设备控制器模式下：

- 在IN（发送）方向的令牌接收时间，FIFO缓冲区中没有要发送的数据
- FIFO缓冲区在OUT（接收）方向上的令牌接收时间已满。

(5) 间隔误差

在设备控制器模式下，以下情况被视为间隔错误：

- 在同步IN传输期间未能在间隔帧中接收IN令牌
- 在同步OUT传输期间未能在间隔帧中接收OUT令牌。

Table 33.30 令牌发送和接收的错误检测（1of2）

检测优先级	错误类型	错误检测和状态产生的中断
1	PID错误	在主机或设备控制器模式下都不会产生中断。（作为损坏的数据包被忽略。）
2	CRC或位填充错误	在主机或设备控制器模式下都不会产生中断。（作为损坏的数据包被忽略。）
3	溢出或欠载错误	在主机和设备控制器模式下，都会产生一个NRDY中断来将OVRN标志设置为1。在设备控制器模式下，发送一个零长度数据包以响应IN令牌。 没有接收到响应OUT令牌的数据包。

Table 33.30 Error detection for token transmission and reception (2 of 2)

4	Interval error	An NRDY interrupt is generated in device controller mode. No interrupt is generated in host controller mode.

Table 33.31 Error detection for data packet reception

Detection priority	Error type	Interrupt generated at error detection and status
1	PID error	No interrupt is generated. (Ignored as a corrupted packet.)
2	CRC or bit stuffing error	An NRDY interrupt is generated and the FRMNUM.CRCE bit sets to 1 in both host and device controller modes.
3	Maximum packet size exceeded error	A BEMP interrupt is generated and the PID[1:0] bits set to STALL in both host and device controller modes.

33.3.12.2 DATA PID

The USBHS does not support high-bandwidth transfers. In device controller mode, the USBHS responds as follows to a received PID:

(1) IN direction

- DATA0: Transmitted as data packet PID
- DATA1: Not transmitted
- DATA2: Not transmitted
- mDATA: Not transmitted.

(2) OUT direction (full-speed operation)

- DATA0: Received normally as data packet PID
- DATA1: Received normally as data packet PID
- DATA2: Packets ignored
- mDATA: Packets ignored.

(3) OUT direction (high-speed operation)

- DATA0: Received normally as data packet PID
- DATA1: Received normally as data packet PID
- DATA2: Received normally as data packet PID
- mDATA: Received normally as data packet PID.

33.3.12.3 Interval counter

The isochronous transfer interval can be set in the PIPEPERI.IITV[2:0] bits. In device controller mode, the interval counter enables functions as shown in Table 33.32. In host controller mode, the USBHS generates the token issuance timing, and the interval counter operation is the same as that for interrupt transfers.

Table 33.32 Interval counter functions in device controller mode

Transfer direction	Function	Conditions for detection
IN	Transmit buffer flush	Failure to receive an IN token successfully in the interval frame during an isochronous IN transfer
OUT	Notification of no reception of token	Failure to receive an OUT token successfully in the interval frame during an isochronous OUT transfer

The interval count is performed when an SOF is received or for complemented SOFs, so the isochronism can be maintained even if an SOF is corrupt. The frame interval can be set to 2IITV (μ) frames.

Table 33.30 令牌发送和接收的错误检测(2of2)

4	间隔误差	在设备控制器模式下会产生一个NRDY中断。在主机控制器模式下不产生中断。

Table 33.31 数据包接收错误检测

检测优先级	错误类型	错误检测和状态产生的中断
1	PID错误	不产生中断。（作为损坏的数据包被忽略。）
2	CRC或位填充错误	在主机和设备控制器模式下，都会产生一个NRDY中断并且FRMNUM.CRCE位设置为1。
3	超出最大数据包大小错误	在主机和设备控制器模式下，都会产生BEMP中断并且PID[1:0]位设置为STALL。

33.3.12.2 数据PID

USBHS不支持高带宽传输。在设备控制器模式下，USBHS对接收到的PID做出如下响应：

(1) 在方向

- DATA0：作为数据包PID发送
- DATA1：未发送
- DATA2：未传输
- mDATA：未传输。

(2) OUT方向（全速运行）

- DATA0：作为数据包PID正常接收
- DATA1：作为数据包PID正常接收
- DATA2：数据包被忽略
- mDATA：数据包被忽略。

(3) OUT方向（高速运转）

- DATA0：作为数据包PID正常接收
- DATA1：作为数据包PID正常接收
- DATA2：作为数据包PID正常接收
- mDATA：作为数据包PID正常接收。

33.3.12.3 间隔计数器

同步传输间隔可以在PIPEPERI.IITV[2:0]位中设置。在设备控制器模式下，间隔计数器启用表33.32中所示的功能。在主机控制器模式下，USBHS产生令牌发布时序，间隔计数器操作与中断传输相同。

Table 33.32 设备控制器模式下的间隔计数器功能

转移方向	Function	检测条件
IN	发送缓冲区刷新	在等时期间未能在间隔帧中成功接收IN令牌转入
OUT	未收到令牌的通知	在等时期间未能在间隔帧中成功接收OUT令牌转出

间隔计数是在接收到SOF时执行的，或者是针对补充的SOF执行的，因此即使SOF损坏也可以保持等时性。帧间隔可以设置为2IITV(μ)帧。

(1) Counter initialization in device controller mode

The USBHS initializes the interval counter under the following conditions:

- Power-on reset:
  This initializes the PIPEPERI.IITV[2:0] bits
- FIFO buffer initialization using the ACLRM bit:
  This does not initialize the IITV[2:0] bits, but does initialize the count value.

After the interval counter is initialized, the interval count starts under either of the following conditions when a packet is transferred successfully:

- An SOF is received after data is transmitted in response to an IN token, with the PID[1:0] bits set to 01b (BUF response)
- An SOF is received after data is received in response to an OUT token, with PID[1:0] bits set to 01b (BUF response).

The interval counter is not initialized under the following conditions:

- When the PID[1:0] bits are set to NAK or STALL
  This does not stop the interval timer. The USBHS attempts the transaction in the next interval.
- USB bus reset and USB suspension
  This does not initialize the IITV[2:0] bits. When an SOF is received, the interval counter starts counting from the value set before SOF was received.

(2) Interval counting and transfer control in host controller mode

The USBHS controls the interval between token issuance operations based on the PIPEPERI.IITV[2:0] bit settings. Specifically, the USBHS issues a token for a selected pipe once every 2^{IITV} frames.

The USBHS starts counting the token issuance interval at the frame following the frame in which the PID[1:0] bits are set to 01b (BUF response) by software.

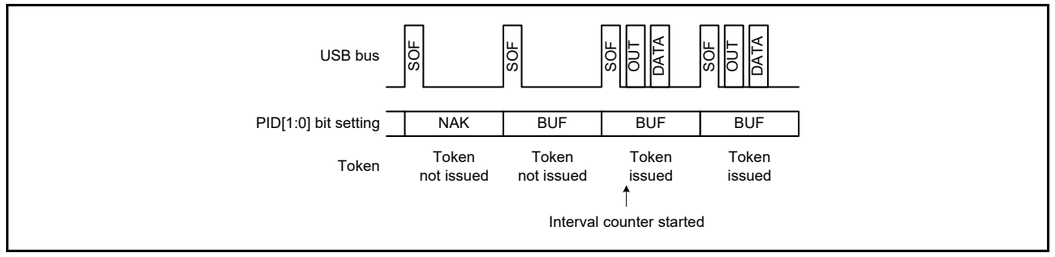


Figure 33.12 Token issuance when IITV[2:0] = 0

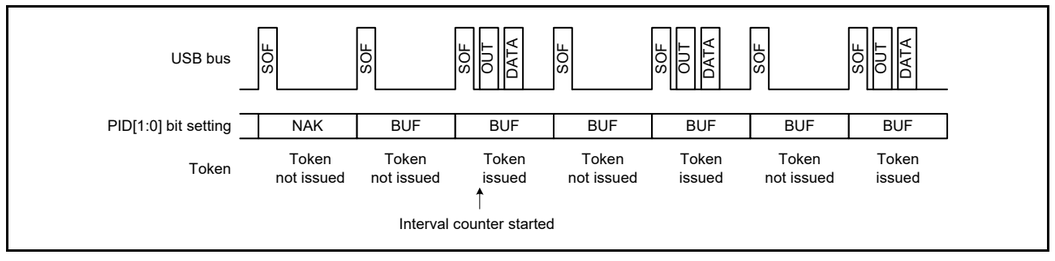


Figure 33.13 Token issuance when IITV[2:0] = 1

When the selected pipe is set for isochronous transfers, the USBHS carries out the following operation in addition to controlling the token issuance interval. The USBHS issues a token even when the NRDY interrupt generation condition is satisfied.

(1) 设备控制器模式下的计数器初始化

USBHS在以下条件下初始化间隔计数器：

- Power-on reset:
  这将初始化PIPEPERI.IITV[2:0]位
- 使用ACLRM位初始化FIFO缓冲区：
  这不会初始化IITV[2:0]位，但会初始化计数值。

间隔计数器初始化后，当数据包传输成功时，间隔计数在以下任一条件下开始：

- 在响应IN令牌传输数据后接收SOF，PID[1:0]位设置为01b（BUF响应）
- 在接收到响应OUT令牌的数据后接收SOF，PID[1:0]位设置为01b（BUF响应）。

间隔计数器在以下情况下不会初始化：

- 当PID[1:0]位设置为NAK或STALL
  这不会停止间隔计时器。USBHS在下一个时间间隔尝试事务。
- USB总线复位和USB暂停这不会初始化IITV[2:0]位。当接收到SOF时，间隔计数器从接收到SOF之前设置的值开始计数。

(2) 主机控制器模式下的间隔计数和传输控制

USBHS根据PIPEPERI.IITV[2:0]位设置控制令牌发布操作之间的间隔。
具体来说，USBHS每2个IITV帧为选定管道发布一次令牌。

USBHS在软件将PID[1:0]位设置为01b（BUF响应）的帧之后的帧开始计算令牌发布间隔。

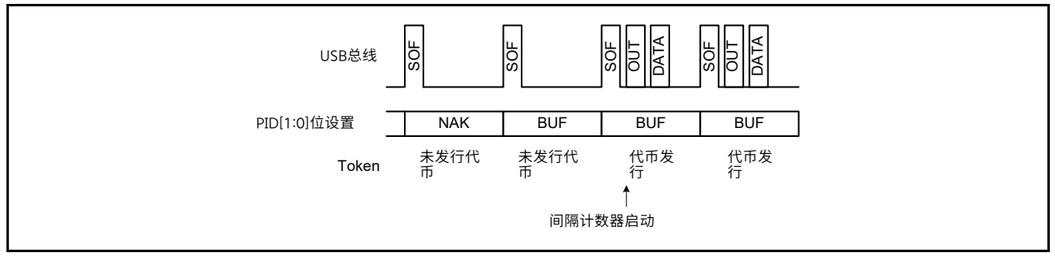


Figure 33.12 IITV[2:0]=0时的代币发行

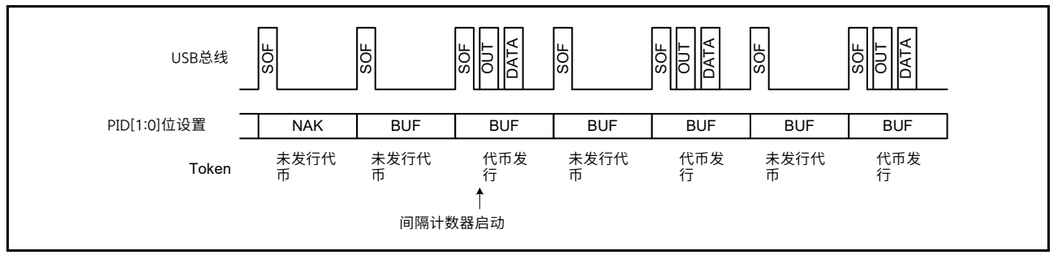


Figure 33.13 IITV[2:0]=1时的代币发行

当所选管道设置为同步传输时，USBHS除了控制令牌发布间隔外，还会执行以下操作。即使满足NRDY中断产生条件，USBHS也会发出一个令牌。

(a) When the selected pipe is for isochronous IN transfers

The USBHS generates an NRDY interrupt when the USBHS issues an IN token but does not receive a packet successfully from a peripheral device (no response or packet error).

(b) When the selected pipe is for isochronous OUT transfers

The USBHS sets the OVRN flag to 1, generating an NRDY interrupt and transmitting a zero-length packet, when the time to issue an OUT token comes while there is no data to be transmitted in the FIFO buffer, because the CPU or DMA/DTC is too slow in writing data to the FIFO buffer.

The token issuance interval is reset on any of the following conditions:

- When the MCU is reset
  This initializes the IITV[2:0] bits
- When the PIPEnCTR.ACLRM bit is set to 1 by software.

(3) Interval counting and transfer control in device controller mode

(a) When the selected pipe is for isochronous OUT transfers

The USBHS generates an NRDY interrupt when it fails to receive a data packet within the interval set in the PIPEPERI.IITV[2:0] bits.

The USBHS also generates an NRDY interrupt when it fails to receive data because of a CRC error or other errors contained in the data packet or because of the FIFO buffer is full.

The NRDY interrupt is generated on SOF packet reception. Even if the SOF packet is corrupted, internal complementation allows the interrupt to be generated when the SOF packet is received. However, when the IITV[2:0] bits are set to a value other than 0, the USBHS generates an NRDY interrupt on receiving an SOF packet for every interval after interval counting starts.

When the PID[1:0] bits are set to 00b (NAK response) by software after starting the interval timer, the USBHS does not generate an NRDY interrupt on receiving an SOF packet.

The timing for starting interval counting depend on the IITV[2:0] setting as follows:

- When the IITV[2:0] bits = 0:
  The interval counting starts when the PID[1:0] bits of the selected pipe are changed to BUF
- When the IITV[2:0] bits ≠ 0:
  The interval counting starts on completion of successful reception of the first data packet after the PID[1:0] bits for the selected pipe are changed to 01b (BUF response).

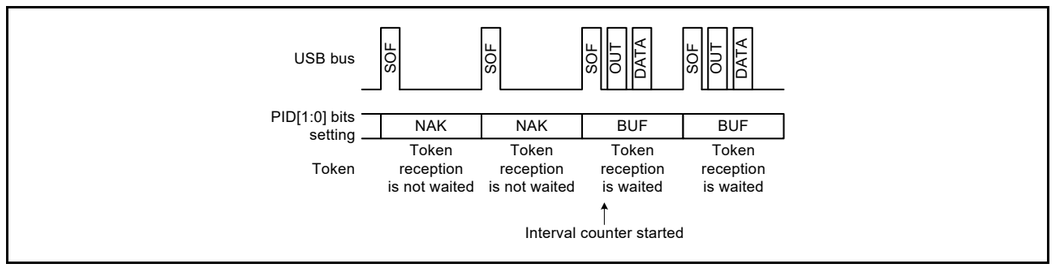


Figure 33.14 Relationship between frames and expected token reception when IITV[2:0] = 0

(a) 当所选管道用于同步IN传输时

当USBHS发出IN令牌但未成功接收到来自外围设备的数据包（无响应或数据包错误）时，USBHS生成NRDY中断。

(b) 当所选管道用于同步OUT传输时

USBHS将OVRN标志设置为1，产生一个NRDY中断并发送一个长度为零的数据包，当发出OUT令牌的时间到来而FIFO缓冲区中没有要发送的数据时，因为CPU或DMADTC是将数据写入FIFO缓冲区太慢。

令牌发行间隔在以下任何条件下重置：

- MCU复位时
  这将初始化IITV[2:0]位
- 当PIPEnCTR.ACLRM位由软件设置为1时。

(3) 设备控制器模式下的间隔计数和传输控制

(a) 当所选管道用于同步OUT传输时

当USBHS在设置的时间间隔内未能接收到数据包时，会产生一个NRDY中断。
PIPEPERI.IITV[2:0] bits.

当由于数据包中包含的CRC错误或其他错误或由于FIFO缓冲区已满而无法接收数据时，USBHS也会产生NRDY中断。

NRDY中断在SOF数据包接收时产生。即使SOF数据包损坏，内部补码也允许在接收到SOF数据包时产生中断。但是，当IITV[2:0]位设置为0以外的值时，USBHS会在间隔计数开始后的每个间隔接收到SOF数据包时产生NRDY中断。

当PID[1:0]位在启动间隔定时器后由软件设置为00b（NAK响应）时，USBHS在接收到SOF数据包时不会产生NRDY中断。

开始间隔计数的时间取决于IITV[2:0]设置，如下所示：

- 当IITV[2:0]位=0时：
  当所选管道的PID[1:0]位更改为BUF时，间隔计数开始
- 当IITV[2:0]位≠0时：
  在所选管道的PID[1:0]位更改为01b（BUF响应）后，第一个数据包的成功接收完成后，间隔计数开始。

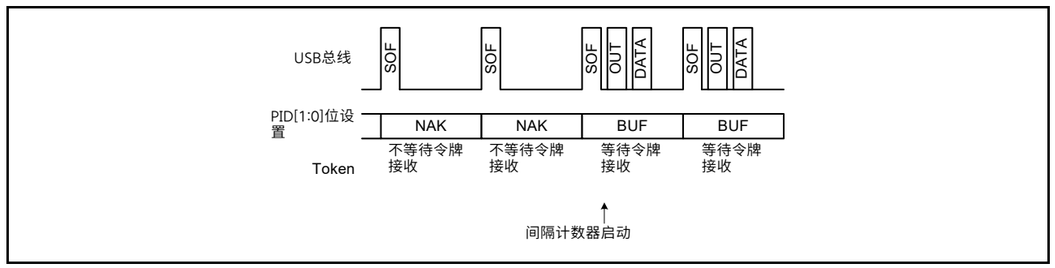


Figure 33.14 IITV[2:0]=0时帧与预期令牌接收之间的关系

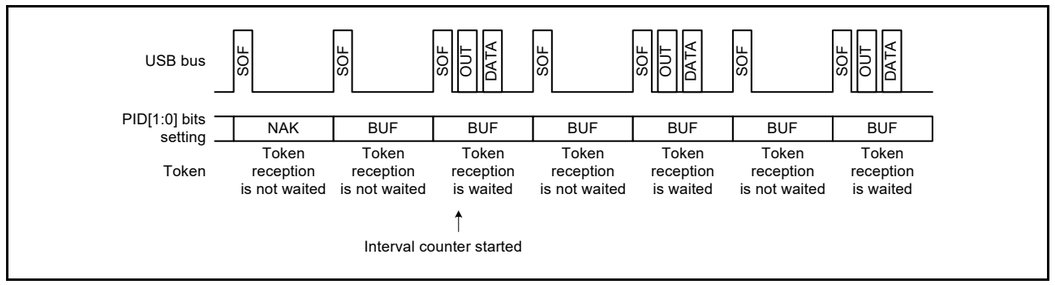


Figure 33.15 Relationship between frames and expected token reception when IITV[2:0] ≠ 0

(b) When the selected pipe is for isochronous IN transfers

The PIPEPERI.IFIS bit must be 1 for this use case. When the IFIS bit is cleared to 0, the USBHS transmits a data packet in response to a received IN token, regardless of the PIPEPERI.IITV[2:0] setting.

When IFIS is 1 and there is data to be transmitted in the FIFO buffer, the USBHS clears the FIFO buffer when it fails to receive an IN token in the frame at the interval set in the IITV[2:0] bits.

The USBHS also clears the FIFO buffer when it fails to receive an IN token successfully because of a bus error, such as a CRC error, contained in the IN token.

The FIFO buffer is cleared on SOF packet reception. Even if the SOF packet is corrupted, the internal complementation allows the FIFO buffer to be cleared when the SOF packet is received.

The timing to start interval counting depends on the IITV[2:0] setting, as with OUT transfers.

The interval is counted on any of the following conditions in device controller mode:

- When a hardware reset is applied to the USBHS (which also sets the IITV[2:0] bits to 000b)
- When the PIPEnCTR.ACLRM bit is set to 1 by software
- When the USBHS detects a USB bus reset.

(4) Transmit data setup for isochronous transfers in device controller mode

With isochronous data transmission using the USBHS in device controller mode, after data is written to the FIFO buffer, a data packet can be transmitted in the first frame after the SOF packet is detected. This isochronous transfer transmit data setup function can identify the frame that started transmission.

When the double buffering is used, transmission is only enabled for the buffer in which data writing was completed first, even after the data write to both buffers is complete. Accordingly, even if multiple IN tokens are received, only the one packet of FIFO buffer data is transmitted.

When the FIFO buffer is ready to transmit data when an IN token is received, the data is transferred and a normal response is returned. However, if the FIFO buffer cannot transmit data, a zero-length packet is transmitted and an underrun error occurs.

Figure 33.16 shows an example of transmission using the isochronous transfer transmit data setup function when the IITV[2:0] bits are set to 0 (every frame).

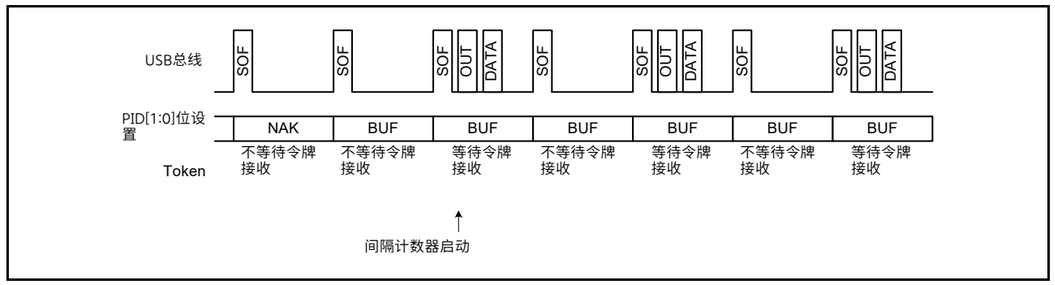


Figure 33.15 IITV[2:0]≠0时帧与预期令牌接收的关系

(b) 当所选管道用于同步IN传输时

对于此用例，PIPEPERI.IFIS位必须为1。当IFIS位清0时，USBHS发送数据包以响应接收到的IN令牌，无论PIPEPERI.IITV[2:0]设置如何。

当IFIS为1且FIFO缓冲区中有数据要发送时，USBHS会在其未能按照IITV[2:0]位设置的时间间隔接收帧中的IN令牌时清除FIFO缓冲区。

当由于IN令牌中包含的总线错误（例如CRC错误）而未能成功接收IN令牌时，USBHS也会清除FIFO缓冲区。

FIFO缓冲区在SOF数据包接收时被清除。即使SOF数据包损坏，内部补码也允许在接收到SOF数据包时清除FIFO缓冲区。

开始间隔计数的时间取决于IITV[2:0]设置，与OUT传输一样。

在设备控制器模式下，根据以下任何条件计算间隔：

- 当对USBHS应用硬件复位时（也将IITV[2:0]位设置为000b）
- 当PIPEnCTR.ACLRM位由软件设置为1时
- 当USBHS检测到USB总线复位时。

(4) 设备控制器模式下同步传输的传输数据设置

在设备控制器模式下使用USBHS进行等时数据传输，数据写入FIFO缓冲区后，可在检测到SOF包后的第一帧发送数据包。此同步传输传输数据设置功能可以识别开始传输的帧。

当使用双缓冲时，即使在两个缓冲区的数据写入都完成之后，也只对首先完成数据写入的缓冲区启用传输。因此，即使接收到多个IN令牌，也仅发送一包FIFO缓冲器数据。

当接收到IN令牌时，当FIFO缓冲区准备好传输数据时，将传输数据并返回正常响应。但是，如果FIFO缓冲区无法传输数据，则会传输零长度数据包并发生欠载错误。

图33.16显示了使用同步传输传输数据设置功能的传输示例，当IITV[2:0]位设置为0（每帧）。

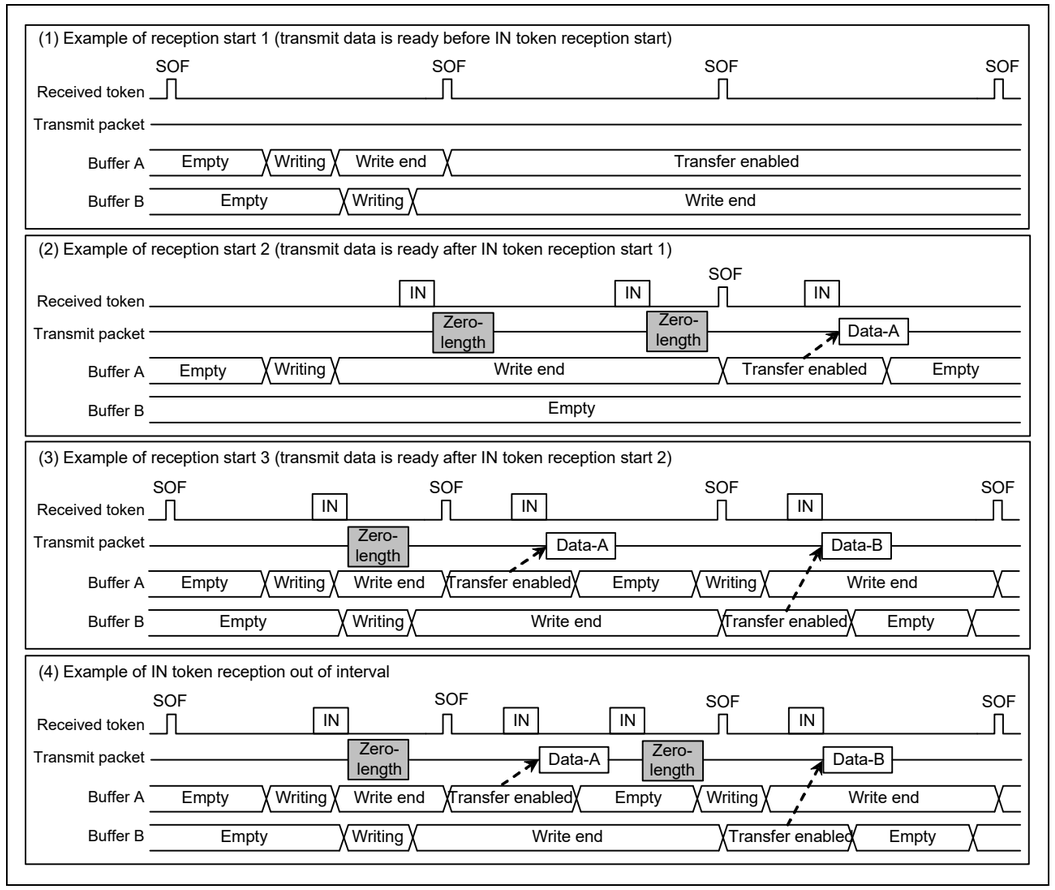


Figure 33.16 Example data setup operation

(5) Isochronous transfer transmit buffer flush in device controller mode

In device controller mode during isochronous data transmission, if the USBHS receives an SOF packet for the next frame without receiving an IN token in the interval frame, it operates as if the IN token is corrupt and clears the buffer that is enabled for transmission, putting that buffer in the writing enabled state.

When double buffering is used and writing to both buffers is complete, the cleared FIFO buffer is assumed to be the one where the data was transmitted in the interval frame, and transmission is enabled for the FIFO buffer that was not cleared on SOF packet reception.

The timing of the buffer flush function depends on the PIPEPERI.IITV[2:0] setting as follows:

- When IITV[2:0] = 0:
  The buffer flush operation starts from the first frame after the pipe is enabled
- When IITV[2:0] ≠ 0:
  The buffer flush operation starts after the first normal transaction.

Figure 33.17 shows an example buffer flush. When an unanticipated token is received before the interval frame, the USBHS sends the write data or a zero-length packet as an underrun error, depending on the data setup status.

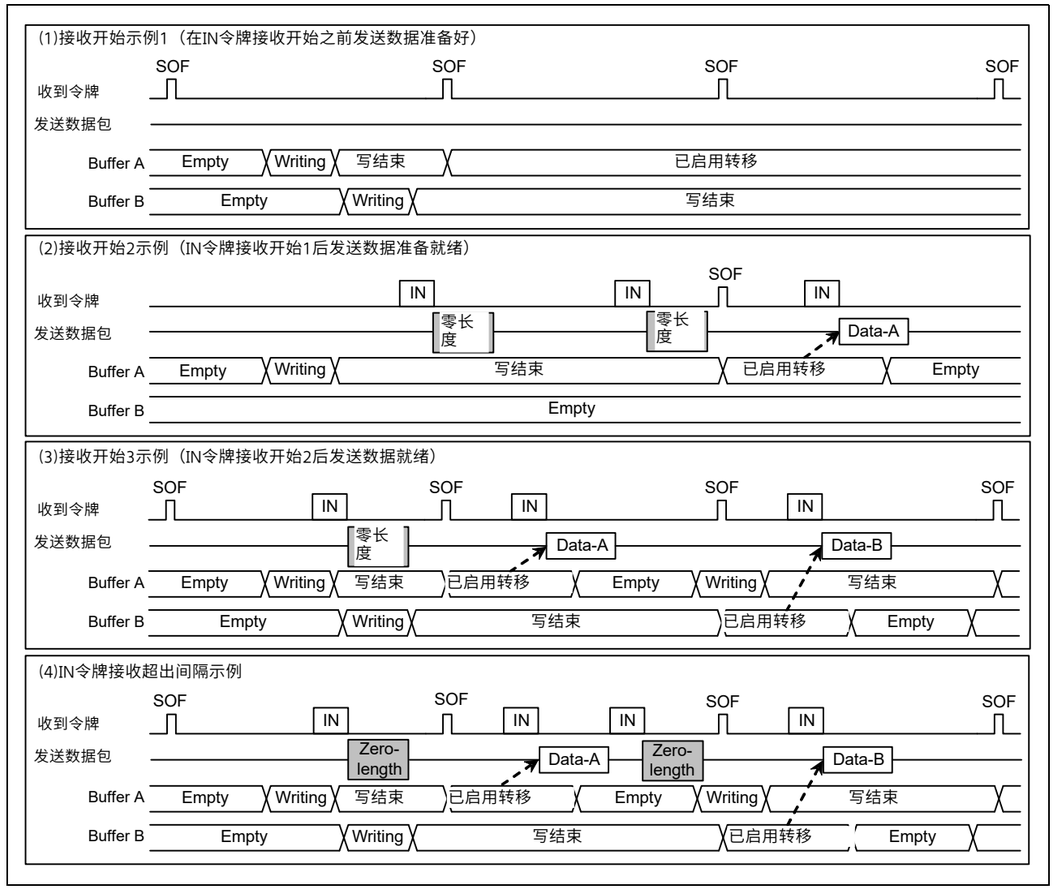


Figure 33.16 示例数据设置操作

(5) 设备控制器模式下的同步传输发送缓冲区刷新

在同步数据传输期间的设备控制器模式下，如果USBHS接收到下一帧的SOF数据包而没有在间隔帧中接收到IN令牌，则它会像IN令牌损坏一样操作并清除启用传输的缓冲区，将该缓冲区处于写入启用状态。

当使用双缓冲并完成对两个缓冲区的写入时，已清除的FIFO缓冲区被假定为在间隔帧中传输数据的缓冲区，并为接收SOF数据包时未清除的FIFO缓冲区启用传输。

缓冲区刷新功能的时间取决于PIPEPERI.IITV[2:0]设置，如下所示：

- When IITV[2:0] = 0:
  缓冲区刷新操作从启用管道后的第一帧开始
- When IITV[2:0] ≠ 0:
  缓冲区刷新操作在第一个正常事务之后开始。

图33.17显示了一个示例缓冲区刷新。当在间隔帧之前收到未预料到的令牌时，USBHS根据数据设置状态将写入数据或零长度数据包作为欠载错误发送。

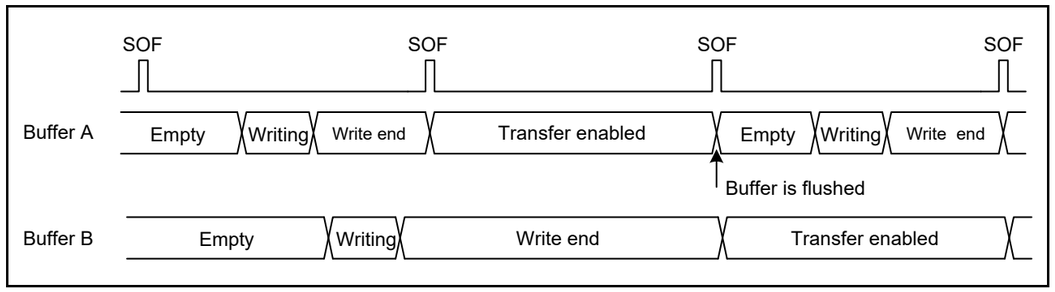


Figure 33.17 Example buffer flush operation

Figure 33.18 shows an example interval error occurrence. There are five types of interval errors, as shown in the figure. An interval error occurs at timing ①, and the buffer flush function is activated.

If an interval error occurs during an IN transfer, the buffer flush function is activated. If it occurs during an OUT transfer, an NRDY interrupt is generated. Use the FRMNUM.OVRN bit to distinguish between this and NRDY interrupts triggered by received packet errors and overrun errors.

For tokens that are shaded in the figure, responses are returned based on the FIFO buffer status.

- IN direction:
  - If the buffer is ready to transfer data, the data is transferred and a normal response is returned
  - If the buffer is not ready to transfer data, a zero-length packet is transmitted and an underrun error occurs.
- OUT direction:
  - If the buffer is ready to receive data, the data is received and a normal response is returned
  - If the buffer is not ready to receive data, the received data is discarded and an overrun error occurs.

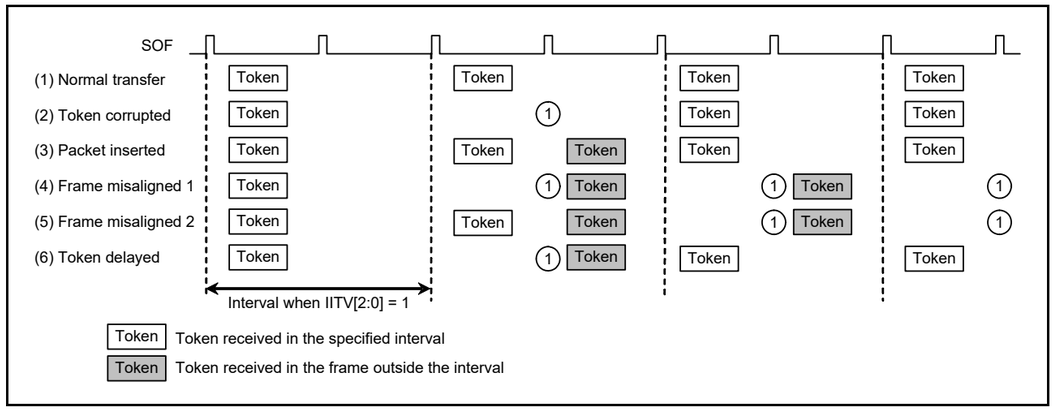


Figure 33.18 Example interval error occurrence when PIPEPERI.IITV[2:0] = 1

33.3.13 SOF Complementation Function

In device controller mode, if packet reception is disabled at intervals of 1 ms in full-speed mode or 125 µs in high-speed mode because the SOF packet is missing or corrupted, the USBHS complements the SOF. SOF complementation begins when the SYSCFG.USBE and LPSTS.SUSPENDM bits are set to 1 and an SOF packet is received. The complementation function is initialized under the following conditions:

- Power-on reset
- USB bus reset

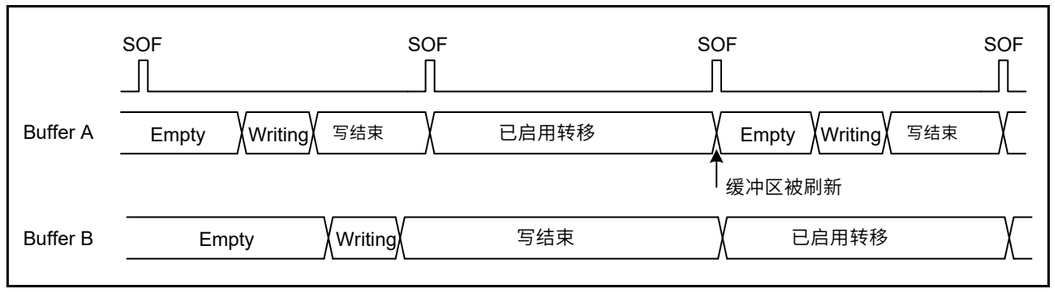


Figure 33.17 缓冲区刷新操作示例

图33.18显示了一个发生间隔错误的示例。如图所示，有五种区间误差。
定时出现间隔错误 ① 并且缓冲区刷新功能被激活。

如果在IN传输期间发生间隔错误，则会激活缓冲区刷新功能。如果它发生在OUT传输期间，则会产生NRDY中断。使用FRMNUM.OVRN位来区分此中断和由接收数据包错误和溢出错误触发的NRDY中断。

对于图中带阴影的令牌，根据FIFO缓冲区状态返回响应。

- IN direction:
  - 如果缓冲区准备好传输数据，则传输数据并返回正常响应
  - 如果缓冲区尚未准备好传输数据，则会传输零长度数据包并发生欠载错误。
- OUT direction:
  - 如果缓冲区准备好接收数据，则接收数据并返回正常响应
  - 如果缓冲区没有准备好接收数据，则丢弃接收到的数据并发生溢出错误。

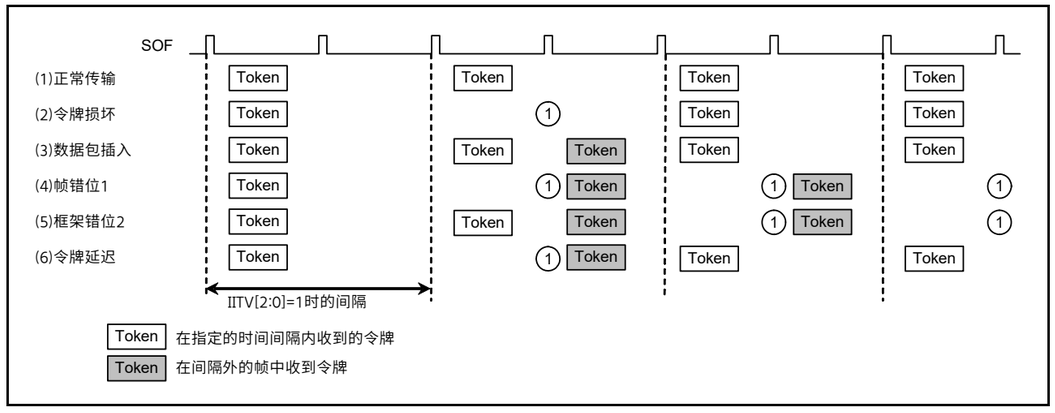


Figure 33.18 PIPEPERI.IITV[2:0]=1时发生的示例间隔错误

33.3.13 SOF互补函数

在设备控制器模式下，如果在全速模式下每隔1ms或在高速模式下每隔125µs禁用数据包接收，因为SOF数据包丢失或损坏，USBHS会补充SOF。当SYSCFG.USBE和LPSTS.SUSPENDM位设置为1并且接收到SOF数据包时，SOF补码开始。补码函数在以下条件下初始化：

- Power-on reset
- USB总线复位

- Suspend state detection.

The SOF complementation function operates as follows:

- The frame interval (125 µs or 1 ms) is determined by the reset handshake protocol result
- The complementation function is not activated until an SOF packet is received
- When the first SOF packet is received, complementation is performed by counting 125 µs or 1 ms on the 48-MHz internal clock
- When the second or subsequent SOF packets are received, complementation is performed at the previous reception interval
- Complementation is not performed in the Suspend state or on reception of a USB bus reset. During high-speed operation, complementation continues for 3 ms from the last packet on transition to the Suspend state.

The USBHS supports the following functions controlled by SOF packet reception. These functions operate normally with SOF complementation if the SOF packet is missing:

- Updating of the frame number and micro frame number
- SOFR interrupt and micro-SOF lock
- SOF pulse output
- Isochronous transfer interval count.

If an SOF packet is missing during full-speed operation, the FFRMNUM.FRNM[10:0] flags are not updated. If a micro-SOF packet is missing during high-speed operation, the URMNUM.UFRNM[2:0] bits are updated.

However, if a micro-SOF packet is missing while the UFRNM[2:0] bits are set to 000b, the FRNM bits are not updated. In this case, even if a subsequent micro-SOF packet with a value other than UFRNM[2:0] bits = 000b is received successfully while UFRNM[2:0] bits are set to the value other than 000b, the FRNM bits are not updated.

33.3.14 Pipe Schedule

33.3.14.1 Conditions for generating transactions

In host controller mode and when the DVSTCTR0.UACT bit is set to 1, the USBHS generates transactions under the conditions as shown in Table 33.33.

Table 33.33 Conditions for generating transactions

	Conditions for generation				
Transaction	**DIR**	**PID[1:0]**	**IITV0**	**Buffer state**	**SUREQ**
Setup	—*1	—*1	—*1	—*1	1 setting
Control transfer data stage, status stage, bulk transfer	IN	BUF	—*1	Receive area exists	—*1
	OUT	BUF	—*1	Transmit data exists	—*1
Interrupt transfer	IN	BUF	Valid	Receive area exists	—*1
	OUT	BUF	Valid	Transmit data exists	—*1
Isochronous transfer	IN	BUF	Valid	*2	—*1
	OUT	BUF	Valid	*3	—*1

Note 1. An em dash (—) in the table indicates that the condition is unrelated to the generating of tokens. “Valid” indicates that, for interrupt transfers and isochronous transfers, a transaction is generated only in transfer frames that are based on the interval counter. “Invalid” indicates that a transaction is generated regardless of the interval counter.
Note 2. This indicates that a transaction is generated regardless of whether there is a receive area. If there is no receive area, however, the received data is discarded.
Note 3. This indicates that a transaction is generated regardless of whether there is any data to be transmitted. If there is no data to be transmitted, however, a zero-length packet is transmitted.

- 暂停状态检测。

SOF互补函数的操作如下：

- 帧间隔（125µs或1ms）由复位握手协议结果决定
- 直到收到SOF数据包才激活补充功能
- 当接收到第一个SOF数据包时，通过在48-MHz内部时钟上计数125µs或1ms来执行补码
- 当接收到第二个或随后的SOF数据包时，在前一个接收间隔执行补充
- 在挂起状态或接收到USB总线复位时不执行补码。在高速操作期间，从最后一个数据包转换到暂停状态的时间为3ms。

USBHS支持以下由SOF数据包接收控制的功能。如果SOF数据包丢失，这些功能在SOF补充的情况下正常运行：

- 更新帧号和微帧号
- SOFR中断和micro-SOF锁定
- SOF脉冲输出
- 同步传输间隔计数。

如果在全速操作期间丢失SOF数据包，则FFRMNUM.FRNM[10:0]标志不会更新。如果一个微SOF数据包在高速运行期间丢失，URMNUM.UFRNM[2:0]位被更新。

但是，如果在UFRNM[2:0]位设置为000b时缺少micro-SOF数据包，则不会更新FRNM位。
在这种情况下，即使在将UFRNM[2:0]位设置为000b以外的值时成功接收到具有非UFRNM[2:0]位=000b的值的后续micro-SOF数据包，FRNM位仍为未更新。

33.3.14 管道计划

33.3.14.1 产生交易的条件

在主机控制器模式下，当DVSTCTR0.UACT位设置为1时，USBHS在表33.33所示的条件下生成事务。

Table 33.33 产生交易的条件

	生成条件				
Transaction	**DIR**	**PID[1:0]**	**IITV0**	**缓冲状态**	**SUREQ**
Setup	—*1	—*1	—*1	—*1	1 setting
控制传输数据阶段、状态阶段、批量传输	IN	BUF	—*1	接收区存在	—*1
	OUT	BUF	—*1	传输数据存在	—*1
中断传输	IN	BUF	Valid	接收区存在	—*1
	OUT	BUF	Valid	传输数据存在	—*1
Isochronous transfer	IN	BUF	Valid	*2	—*1
	OUT	BUF	Valid	*3	—*1

Note 1. 表中的破折号(—)表示该条件与令牌的生成无关。“有效”表示，对于中断传输和同步传输，事务仅在基于间隔计数器的传输帧中生成。“无效”表示无论间隔计数器如何都生成事务。

Note 2. 这表示不管是否有接收区域，都会产生一个事务。但是，如果没有接收区域，则丢弃接收到的数据。

Note 3. 这表明无论是否有任何数据要传输，都会生成一个事务。然而，如果没有要传输的数据，则传输零长度数据包。

33.3.14.2 Transfer schedule

This section describes the transfer scheduling within a frame of the USBHS. After the USBHS sends an SOF, the transfer is carried out in the following sequence:

1. Execution of periodic transfers:
   A pipe is searched for in the order of pipe 1 → pipe 2 → pipe 6 → pipe 7 → pipe 8 → pipe 9, and then if there is a pipe for which an isochronous or interrupt transfer transaction can be generated, the transaction is generated.
2. Setup transactions for control transfers:
   The DCP is checked, and if a setup transaction is possible, it is sent.
3. Execution of bulk transfers, control transfer data stages, and control transfer status stages:
   A pipe is searched for in the order of DCP → pipe 1 → pipe 2 → pipe 3 → pipe 4 → pipe 5, and then if there is a pipe for which a transaction for a bulk transfer, a control transfer data stage, or a control transfer status stage can be generated, the transaction is generated.
   When a transaction is generated, processing moves to the next pipe transaction regardless of whether the response from the peripheral device is ACK or NAK. If there is time for transfer within the frame, step 3 is repeated.

33.3.14.3 Enabling USB communication

Setting the DVSTCTR0.UACT bit to 1 initiates an SOF transmission, and transaction generation is enabled. Setting the UACT bit to 0 stops SOF transmission, and the Suspend state is invoked. If the UACT setting is changed from 1 to 0, processing stops after the next SOF is sent.

33.3.15 Battery charging detection processing

The USBHS provides control over the data contact detection processing (D+ line contact checking), primary detection processing (charger detection processing), and secondary detection processing (charger determination processing) as defined in the Battery Charging Specification.

This section describes operations required in device and host controller modes.

33.3.15.1 Processing in device controller mode

To operate a function device as a battery charging portable device:

1. Start primary detection processing after detecting contact with the D+ and D- lines. The Battery Charging Specification describes two processing methods for Data Contact Detection. The USBHS supports both methods as follows:
   - Software processing
     After a VBINT interrupt or polling of the VBSTS flag indicates a change in the state of the USBHS_VBUS input pin, software controls a wait from 300 to 900 ms. The BCCTRL.VDPSRCE and IDMSINKE bits are then both set to 1, enabling the VDP_SRC and IMP_SINK circuits, respectively, to start primary detection processing.
   - Hardware processing
     Apply 7 to 13 µA of current to the D+ line to hold the D+ line at the logical high level. This is done to detect the D+ and D- lines going to the logical low level because of pull-down resistors on the host device side when the D+ and D- lines come in contact with those of the host. Monitor the SYSSTS0.LNST[1:0] flags while the BCCTRL.IDPSRCE bit is set to 1, enabling the IDP_SRC circuit, to see when the level on the D+ line changes from high to low. After detecting a low level on the D+ line, clear the BCCTRL.IDPSRCE bit to 0, disabling the IDP_SRC circuit, and set both the BCCTRL.VDPSRCE and IDMSINKE bits to 1, enabling the VDP_SRC and IDM_SINK circuits, respectively, to start primary detection processing. The VDPSRCE and IDMSINKE bits must be set to 1 simultaneously.
2. After the start of primary detection processing followed by a software-controlled wait of 40 ms, check the BCCTRL.CHGDETSTS flag. A value of 1 indicates detection of a charger, and secondary detection processing starts.*1
3. To start secondary detection processing, clear both the BCCTRL.VDPSRCE and IDMSINKE bits to 0, disabling the VDP_SRC and IDM_SINK circuits, respectively. Next, set both the BCCTRL.VDMSRCE and IDPSINKE bits to 1, enabling the VDM_SRC and IDP_SINK circuits, respectively.

33.3.14.2 转移时间表

本节介绍USBHS帧内的传输调度。USBHS发送SOF后，按以下顺序进行传输：

1. 执行定期转账：
   按照管道1 管道2 管道6 管道7 管道8 管道9的顺序搜索管道，然后如果存在可以生成等时或中断传输事务的管道，则生成事务.
2. 为控制转移设置交易：
   DCP被检查，如果设置事务是可能的，它被发送。
3. 批量传输、控制传输数据阶段和控制传输状态阶段的执行：
   管道按DCP 管道1 管道2 管道3 管道4 管道5的顺序搜索，然后如果存在要进行批量传输的事务、控制传输数据阶段或可以生成控制转移状态阶段，生成事务。生成事务时，无论来自外围设备的响应是ACK还是NAK
   ，处理都会转移到下一个管道事务。如果帧内有时间进行传输，则重复步骤3。

33.3.14.3 启用USB通信

将DVSTCR0.UACT位设置为1启动SOF传输，并启用事务生成。设置
UACT位为0停止SOF传输，并调用暂停状态。如果UACT设置从1更改为0，则在发送下一个SOF后处理停止。

33.3.15 电池充电检测处理

USBHS提供对电池充电规范中定义的数据接触检测处理（D+线路接触检查）、一次检测处理（充电器检测处理）和二次检测处理（充电器确定处理）的控制。

本节介绍设备和主机控制器模式所需的操作。

33.3.15.1 设备控制器模式下的处理

将功能设备作为电池充电便携式设备操作：

1. 在检测到与D+和Dlines的接触后开始初级检测处理。电池充电
   规范描述了数据接触检测的两种处理方法。USBHS支持以下两种方法：
   - 软件处理
     在VBINT中断或轮询VBSTS标志指示USBHS_VBUS输入引脚的状态发生变化后，软件控制从300到900ms的等待。然后BCCTRL.VDPSRCE和IDMSINKE位都设置为1，分别使VDP_SRC和IMP_SINK电路开始主要检测处理。
   - 硬件加工
     向D+线施加7到13µA的电流，以将D+线保持在逻辑高电平。这样做是为了检测
     当D+和Dlines与主机的电阻接触时，由于主机设备侧的下拉电阻，D+和Dlines变为逻辑低电平。监控SYSSTS0.LNST[1:0]标志，而
     BCCTRL.IDPSRCE位设置为1，启用IDP_SRC电路，以查看D+线上的电平何时从高变为低。检测到D+线上的低电平后，将BCCTRL.IDPSRCE位清除为0，禁用IDP_SRC电路，并将BCCTRL.VDPSRCE和IDMSINKE位都设置为1，启用VDP_SRC和
     IDM_SINK电路分别启动初级检测处理。VDPSRCE和IDMSINKE位必须同时设置为1。
2. 在主要检测处理开始后，软件控制等待40毫秒后，检查
   BCCTRL.CHGDETSTS标志。值为1表示检测到充电器，并开始二次检测处理。*1
3. 要启动二次检测处理，请将BCCTRL.VDPSRCE和IDMSINKE位都清除为0，分别禁用VDP_SRC和IDM_SINK电路。接下来，将BCCTRL.VDMSRCE和IDPSINKE位都设置为1，分别启用VDM_SRC和IDP_SINK电路。

4. After the start of secondary detection processing followed by a software-controlled wait of 40 ms, check the BCCTRL.PDDETSTS flag. A value of 1 indicates that secondary detection processing is complete.

Note 1. In primary detection processing, detection of a voltage above the range from 0.25 to 0.4 V and below the range from 0.8 to 2.0 V on the D-Line indicates that the other device is a host device that supports battery charging (charging downstream port). The BCCTRL.CHGDETSTS flag in the PHY block only indicates whether the voltage on the D- line is higher than the range from 0.25 to 0.4 V, so add processing as required to read the SYSSTS0.LNST[1:0] flags and confirm that the voltage on the D- line is also below the range from 0.8 to 2.0 V.

Figure 33.19 illustrates this processing flow.

4. 在二次检测处理开始后，软件控制等待40毫秒，检查BCCTRL.PDDETSTS标志。值为1表示二次检测处理完成。

注1.在初级检测处理中，在D-Line上检测到高于0.25至0.4V范围且低于0.8至2.0V范围的电压表示其他设备是支持电池充电的主机设备（充电下游港口）。PHY块中的BCCTRL.CHGDETSTS标志位仅指示Dline上的电压是否高于0.25至0.4V的范围，因此根据需要添加处理以读取SYSSTS0.LNST[1:0]标志并确认电压Dline上的电压也低于0.8至2.0V的范围。

图33.19说明了这个处理流程。

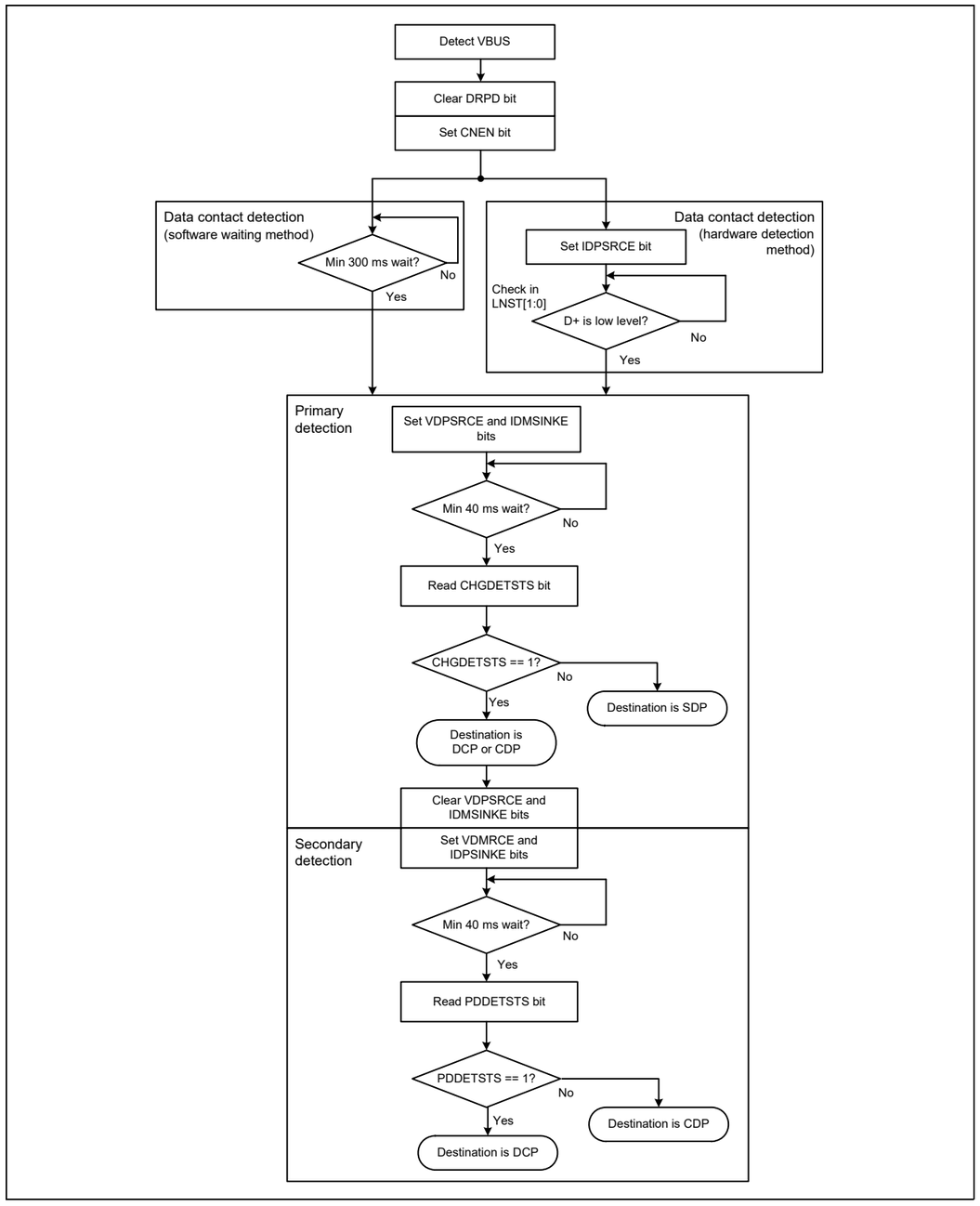


Figure 33.19 Processing flow as portable device

33.3.15.2 Processing in host controller mode

In host controller mode, driving the D- line is required for a portable device to perform primary detection. The USBHS supports the following two primary detection methods:

- When the hardware has a portable device detection function

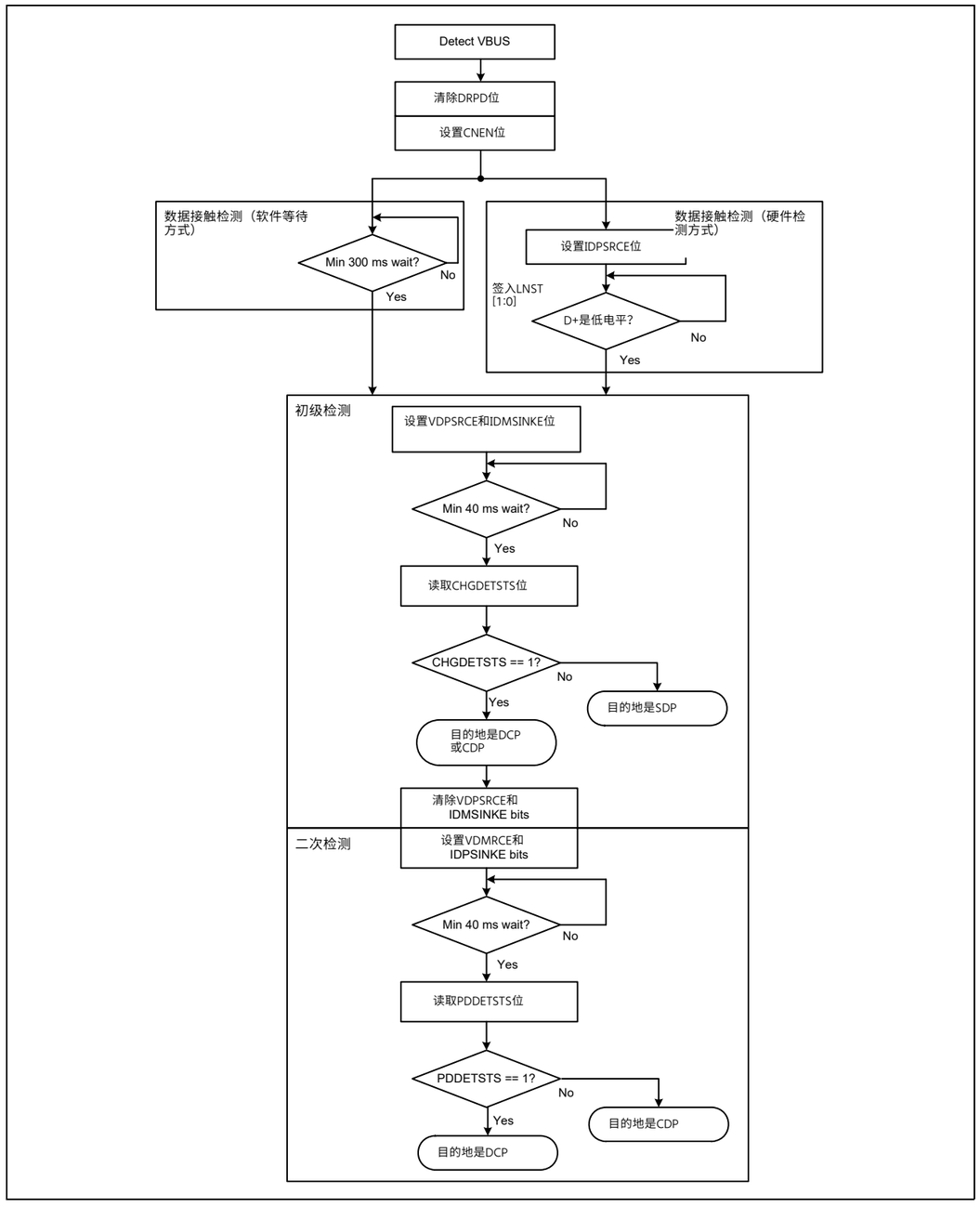


Figure 33.19 作为便携式设备的处理流程

33.3.15.2 主机控制器模式下的处理

在主机控制器模式下，便携式设备需要驱动Dline才能执行初级检测。USBHS支持以下两种主要检测方法：

- 当硬件具有便携设备检测功能时

- When the hardware does not have the function or the function is present but not used.

Figure 33.20 and Figure 33.21 show the processing flows for these methods.

(1) When the hardware has a portable device detection function

a. Start driving the USBHS_VBUS input pin.

b. Set the BCCTRL.IDMSINKE bit to 1 to enable the portable device detection circuit.

c. Monitor the portable device detection signal and start driving the D-line when the level of the portable device detection signal is high*1.

d. Stop driving the D-line when the portable device detection signal is at the low level*1.

Note 1. The PDDETINT interrupt indicates a change in the level of the portable device detection signal (EUH_CPDDET), and the current level can be obtained by reading the PDDETSTS flag.

(2) When the hardware does not have a portable device detection function or the function is not used

Software handles the timing of steps a. and b.

a. After a disconnect is detected, start driving the D-line within 200 ms.

b. After a connect is detected, stop driving the D-line within 10 ms.

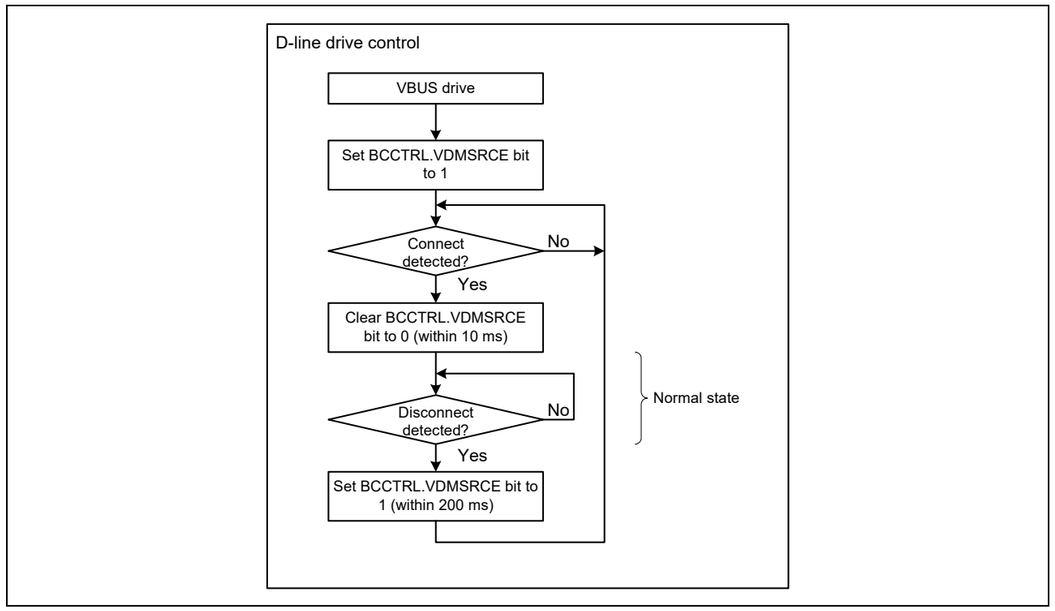


Figure 33.20 Processing flow as charging downstream port without hardware portable device detection function or when function is not used

- 当硬件不具备该功能或该功能存在但未使用时。

图33.20和图33.21显示了这些方法的处理流程。

(1) 当硬件具有便携设备检测功能时

一个。开始驱动USBHS_VBUS输入引脚。

湾。将BCCTRL.IDMSINKE位设置为1以启用便携式设备检测电路。

C。监控便携设备检测信号，当便携设备检测信号的电平为高*1时开始驱动D线。

d。当便携设备检测信号为低电平*1时停止驱动D线。

注1.PDDETINT中断表示便携式设备检测信号（EUH_CPDDET）的电平发生变化，通过读取PDDETSTS标志可以获得当前电平。

(2) 硬件不具备便携设备检测功能或未使用该功能时

软件处理步骤a的时间安排。和b。

一个。检测到断开后，在200毫秒内开始驱动D线。

湾。检测到连接后，在10ms内停止驱动D线。

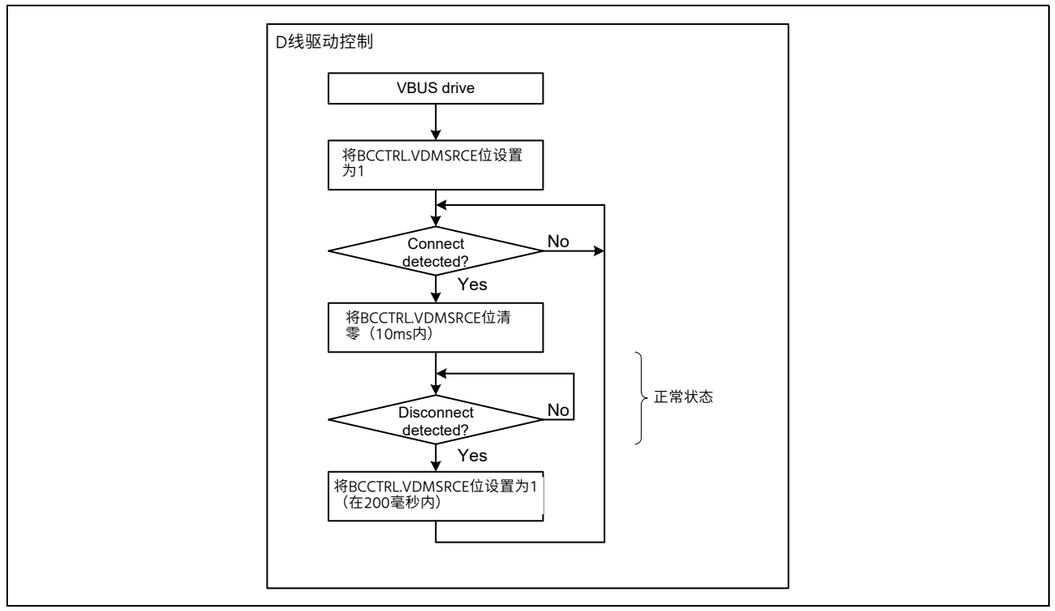


Figure 33.20 不带硬件便携设备检测功能或不使用功能时作为充电下行端口的处理流程

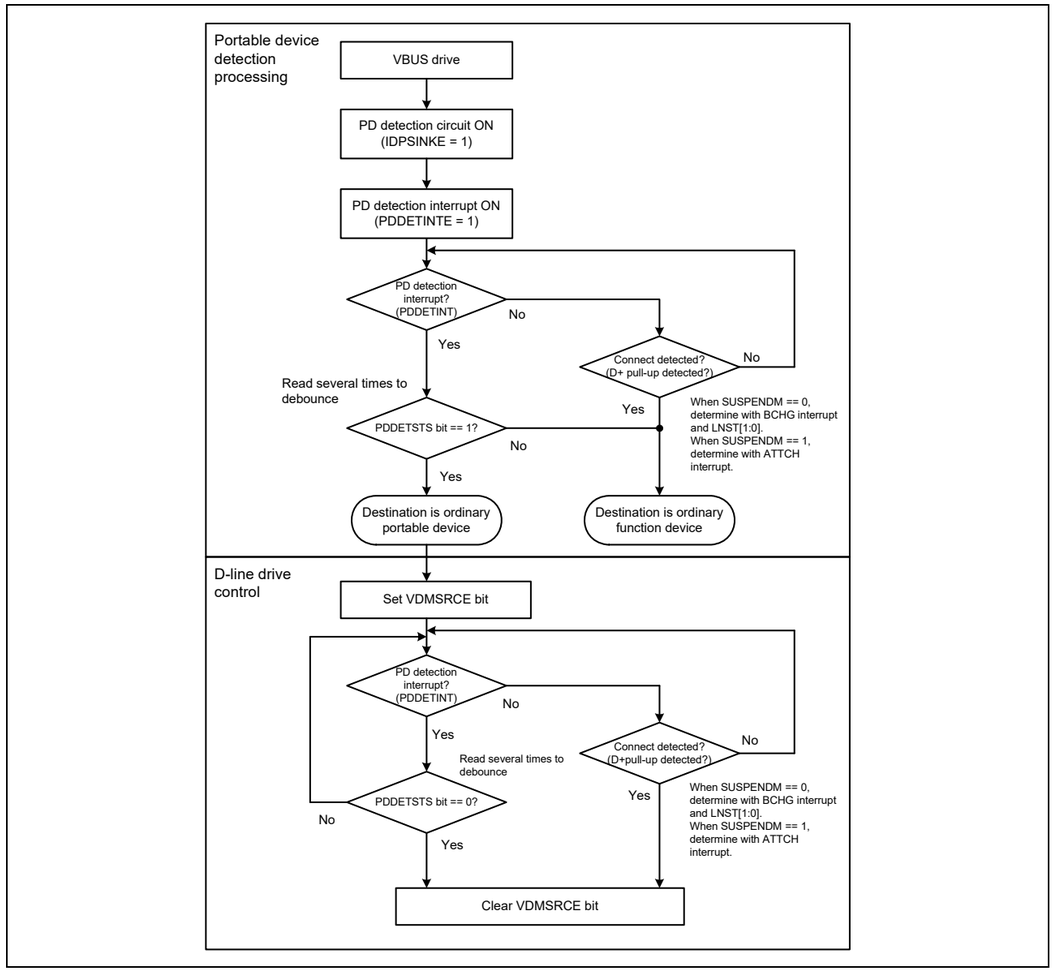


Figure 33.21 Processing flow as charging downstream port with hardware portable device detection function

33.3.16 Link Power Management Processing

The Link Power Management standard defines the existing Suspend state as the L2 state and also defines the L1 state as a state that allows transition and return with lower latency than the L2 state (Suspend). Table 33.34 provides a comparison between the L2 (Suspend) and L1 states.

Table 33.34 Comparison between L2 (Suspend) state and L1 state (1 of 2)

Parameter	L1 state	L2 (Suspend) state
Transition	LPM transaction	Idle for 3 ms
Return caused by host	Host: Minimum drive period (75 µs to 1.175 ms) can be specified by the host. Function: 10-µs K drive	Host: Minimum 20-ms K drive Function: 10-ms K drive

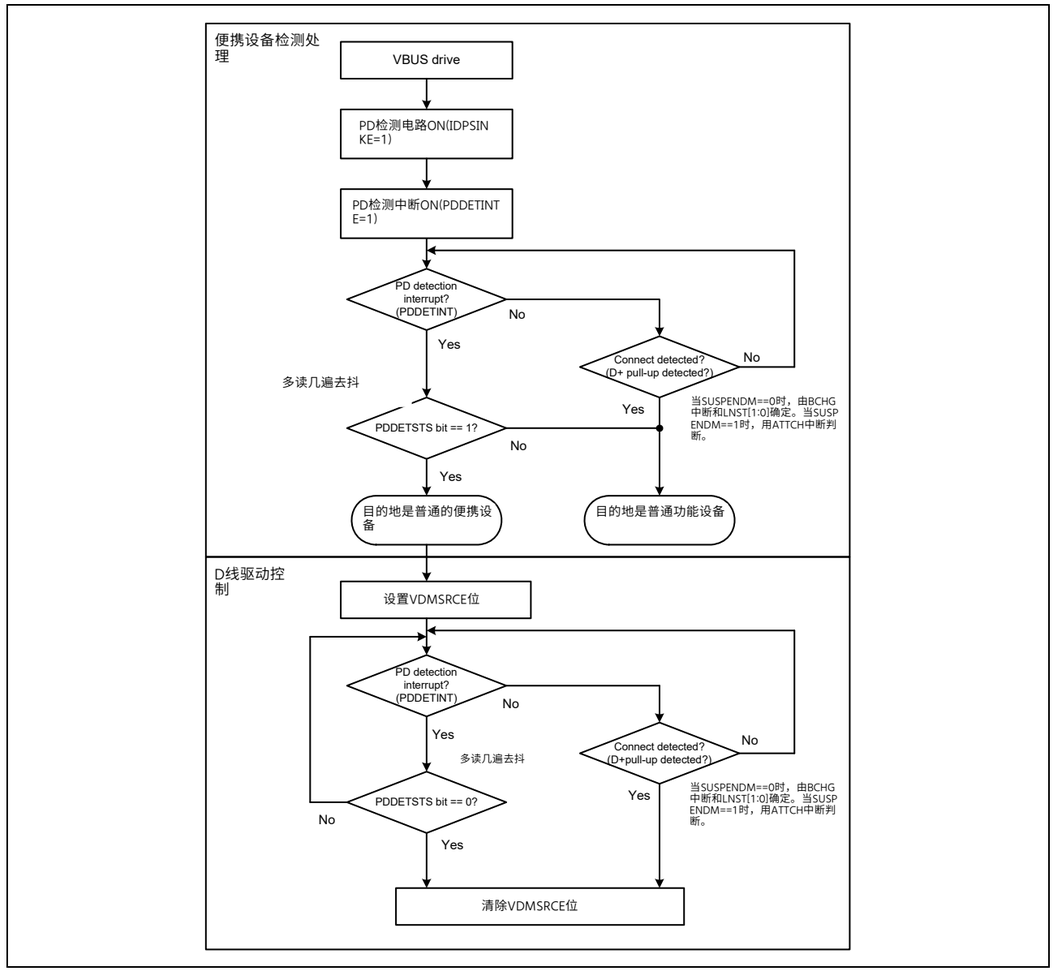


Figure 33.21 具有硬件便携设备检测功能的充电下行端口的处理流程

33.3.16 链路电源管理处理

LinkPowerManagement标准将现有的Suspend状态定义为L2状态，并将L1状态定义为允许转换和返回时延迟低于L2状态(Suspend)的状态。表33.34提供了L2（挂起）和L1状态之间的比较。

Table 33.34 L2（挂起）状态和L1状态之间的比较（1of2）

Parameter	L1 state	L2 (Suspend) state
Transition	LPM transaction	空闲3毫秒
主机造成的退货	Host: 主机可以指定最小驱动周期（75µs至1.175ms）。 功能：10-µsK驱动	Host: 最小20毫秒K驱动器 Function: 10-ms K drive

Table 33.34 Comparison between L2 (Suspend) state and L1 state (2 of 2)

Parameter	L1 state	L2 (Suspend) state
Return caused by function	Device: 50-µs K drive Function: 60- to 990-µs K drive Device: 10-µs K drive	Function: 1- to 15-ms K drive Host: Minimum 20-ms K drive Function: 10-ms K drive
Signaling	Low- and full-speed idle	Low- and full-speed idle

33.3.16.1 Processing in device controller mode

(1) Descriptor contents

In device controller mode, the USBHS must return its descriptor on receiving the GetDescriptor command.

Change the content of the descriptor to be returned depending on whether the transition to and return from the L1 state corresponds to the processing for the LPM transaction. The following table shows the relationship between LPM correspondence and the descriptor.

Table 33.35 Relationship between LPM correspondence and descriptor

Correspondence with LPM	bcdUSB field	USB2.0 extension descriptor		Response to received LPM request	Notes
		Provided/ not provided	Value of LPM bit		
Does not correspond	0200h	Not provided	—	No response	Normal operation when the LPM is not supported
	0201h	Provided	0	STALL	Setting for clear non-correspondence to LPM. In this case, a STALL response must be returned.
Corresponds	0201h	Provided	1	ACK or NYET	Normal operation when the LPM is supported

Declare whether to correspond to the transition to and return from L1 in the LPM bit in the USB 2.0 extension descriptor. To provide the USB2.0 extension descriptor, the bcdUSB field of the device descriptor must be set to a value of 0201h or larger.

When the LPM is not supported, the USB2.0 extension descriptor is not provided and the bcdUSB field value must be 0200h. If an LPM token is received in this case, it must be ignored. It is also possible to set the bcdUSB field value to 0201h and the LPM bit in the USB2.0 extension descriptor to 0 (LPM tokens not supported). In this case, the LPM token cannot be ignored and a STALL response must be returned.

When the LPM token is supported, set the bcdUSB field value to 0201h and set the LPM bit in the USB 2.0 extension descriptor to 1 (LPM tokens supported). This allows acknowledgment when returning a NYET or ACK response to the LPM token.

(2) Processing during LPM token reception

Transition to and return from the L1 state in device controller mode is as follows:

a. When the USBHS receives an LPM token from the host, the L1RESPEN, L1RESPMD[1:0], and L1NEGOMD settings in PL1CTRL1 determine whether a response packet is sent or the token is ignored and, if a response is to be sent, whether it is an ACK, NYET, or STALL packet.

b. If an ACK response to the LPM token is sent and the host does not transmit another LPM token in 8 µs, the USBHS enters the L1 state. The USBHS handles detection of the newly transmitted packet and the transition to the L1 state. The DVST interrupt can be used to detect the transition.

c. Two types of processing can return the USBHS from the L1 state:

- When the host drives the D-line in the K-state:
  The function device detects the K-state and starts processing the return from the L1 state in response to an

Table 33.34 L2（挂起）状态和L1状态之间的比较（2个中的2个）

Parameter	L1 state	L2 (Suspend) state
函数导致的返回	Device: 50-µs K drive Function: 60- to 990-µs K drive Device: 10-µs K drive	Function: 1- to 15-ms K drive Host: 最小20毫秒K驱动器 Function: 10-ms K drive
Signaling	Low- and full-speed idle	Low- and full-speed idle

33.3.16.1 设备控制器模式下的处理

(1) 描述符内容

在设备控制器模式下，USBHS必须在接收到GetDescriptor命令时返回其描述符。

根据L1状态的转换和返回是否对应于LPM事务的处理，更改要返回的描述符的内容。下表显示了LPM对应关系和描述符之间的关系。

Table 33.35 LPM对应与描述符的关系

与LPM的通信	bcdUSB field	USB2.0扩展描述符		收到的回复 LPM request	Notes
		提供未提供	LPM位的值		
不对应	0200h	不提供	—	没有反应	不支持LPM时的正常操作
	0201h	Provided	0	STALL	设置明确不对应 LPM。在这种情况下，必须返回一个STALL响应。
Corresponds	0201h	Provided	1	ACK或NYET	支持LPM时的正常操作

在USB2.0扩展描述符中的LPM位中声明是否对应于L1的转换和返回。要提供USB2.0扩展描述符，设备描述符的bcdUSB字段必须设置为0201h或更大的值。

不支持LPM时，不提供USB2.0扩展描述符，bcdUSB字段值必须为0200h。如果在这种情况下接收到LPM令牌，则必须将其忽略。也可以将bcdUSB字段值设置为0201h，并将USB2.0扩展描述符中的LPM位设置为0（不支持LPM令牌）。在这种情况下，不能忽略LPM令牌并且必须返回STALL响应。

当支持LPM令牌时，将bcdUSB字段值设置为0201h，并将USB2.0扩展描述符中的LPM位设置为1（支持LPM令牌）。这允许在向LPM令牌返回NYET或ACK响应时进行确认。

(2) LPM令牌接收期间的处理

设备控制器模式下L1状态的转换和返回如下：

一个。当USBHS接收到来自主机的LPM令牌时，PL1CTRL1中的L1RESPEN、L1RESPMD[1:0]和L1NEGOMD设置确定是发送响应包还是忽略令牌，如果要发送响应，是否是ACK、NYET或STALL数据包。

湾。如果发送了对LPM令牌的ACK响应并且主机在8µs内没有发送另一个LPM令牌，则
USBHS进入L1状态。USBHS处理新传输数据包的检测和向L1状态的转换。DVST中断可用于检测转换。

C。两种类型的处理可以使USBHS从L1状态返回：

- 当主机在K态驱动D线时：
  功能设备检测到K状态并开始处理从L1状态返回以响应

RESM interrupt request

- When the function device outputs a remote wakeup signal:
  If the software on the function device sets the DVSTCTR0.WKUP bit to 1, it sends a remote wakeup signal to the host.

The software clears the DVSTCTR0.WKUP bit to 0 on returning from the L2 (Suspend) state, and the USBHS clears the DVSTCTR0.WKUP bit to 0 for return from the L1 state.

(3) HIRD field value negotiation function

The HIRD field value included in the LPM token indicates the host K-drive period on return from the L1 state. The HIRD field value can be adjusted according to the requirements of the target system. For example, a small HIRD field value is better for systems focusing on higher transfer efficiency, while a large HIRD field value is better for systems focusing on low power consumption.

Based on the L1NEGOMD and HIRDTHR[3:0] settings in PL1CTRL1, an ACK response is returned when the received HIRD field value is in the expected range, and otherwise a NYET response is returned, requesting the host to change the HIRD field value.

Note: This HIRD field value negotiation function at the host must also support negotiation processing.

33.3.16.2 Processing in host controller mode

(1) Processing during LPM token transmission

Transition to and return from the L1 state in host controller mode is as follows:

a. When the HL1CTRL.L1REQ bit is set to 1, an LPM token is sent to the function device from the host device.

b. If an ACK response is received from the function device, a transition to the L1 state starts within 10 µs and is complete within 50 µs. If a transaction error is detected, another LPM token is transmitted within 8 µs. Retransmission can proceed up to two times. The USBHS handles all of this processing.

c. Two types of processing can return the USBHS from the L1 state:

- When the host drives the D-line for the K state:
  When the DVSTCTR0.RESUME bit is set to 1, the host device starts driving the D-line for the K-state and starts processing the return
- When the function device generates a remote wakeup signal:
  When the host device detects a remote wakeup signal from the function device, it sets the DVSTCTR0.RESUME bit to 1 and starts driving the D-line for the K-state.

Unlike when returning from the Suspend (L2) state, the USBHS clears the DVSTCTR0.RESUME bit to 0. After clearing the RESUME bit, it sets the DVSTCTR0.UACT bit to 1 and issues an L1RSMEND interrupt request.

33.3.17 Release from Deep Software Standby Mode Because of USB Suspend/Resume Interrupts

Deep Software Standby mode can be canceled by a USB suspend/resume interrupt. USB suspend/resume interrupts are detected by the USB resume detecting unit, which controls and monitors the USB I/O pins to detect the interrupts.

Figure 33.22 shows the flow for setting the USBHS when entering Deep Software Standby mode from either host or device controller mode. Figure 33.23 and Figure 33.24 show the flows for setting the USBHS when canceling Deep Software Standby mode from host controller mode. Figure 33.25 shows the flow for setting the USBHS when canceling Deep Software Standby mode from device controller mode.

RESM中断请求

- 当功能设备输出远程唤醒信号时：
  如果功能器件上的软件将DVSTCTR0.WKUP位设置为1，它会向主机发送远程唤醒信号。

软件在从L2（挂起）状态返回时将DVSTCTR0.WKUP位清除为0，并且USBHS清除
DVSTCTR0.WKUP位为0表示从L1状态返回。

(3) HIRD字段值协商功能

LPM令牌中包含的HIRD字段值指示从L1状态返回的主机K-drive周期。这
HIRD字段值可以根据目标系统的要求进行调整。例如，较小的HIRD字段值更适合专注于更高传输效率的系统，而较大的HIRD字段值更适合专注于低功耗的系统。

根据PL1CTRL1中的L1NEGOMD和HIRDTHR[3:0]设置，当接收到的HIRD字段值在预期范围内时返回ACK响应，否则返回NYET响应，请求主机更改
HIRD字段值。

Note: 主机上的这个HIRD字段值协商功能也必须支持协商处理。

33.3.16.2 主机控制器模式下的处理

(1) LPM令牌传输期间的处理

主机控制器模式下L1状态的转换和返回如下：

一个。当HL1CTRL.L1REQ位设置为1时，LPM令牌从主机设备发送到功能设备。

湾。如果从功能设备接收到ACK响应，则在10µs内开始转换到L1状态，并在50µs内完成。如果检测到事务错误，则会在8µs内发送另一个LPM令牌。重传最多可以进行两次。USBHS处理所有这些处理。

C。两种类型的处理可以使USBHS从L1状态返回：

- 当主机驱动D线为K状态时：
  当DVSTCTR0.RESUME位设置为1时，主机设备开始驱动D线为K状态并开始处理返回
- 当功能设备产生远程唤醒信号时：
  当主机设备检测到来自功能设备的远程唤醒信号时，它设置
  DVSTCTR0.RESUME位为1并开始驱动D线为K状态。

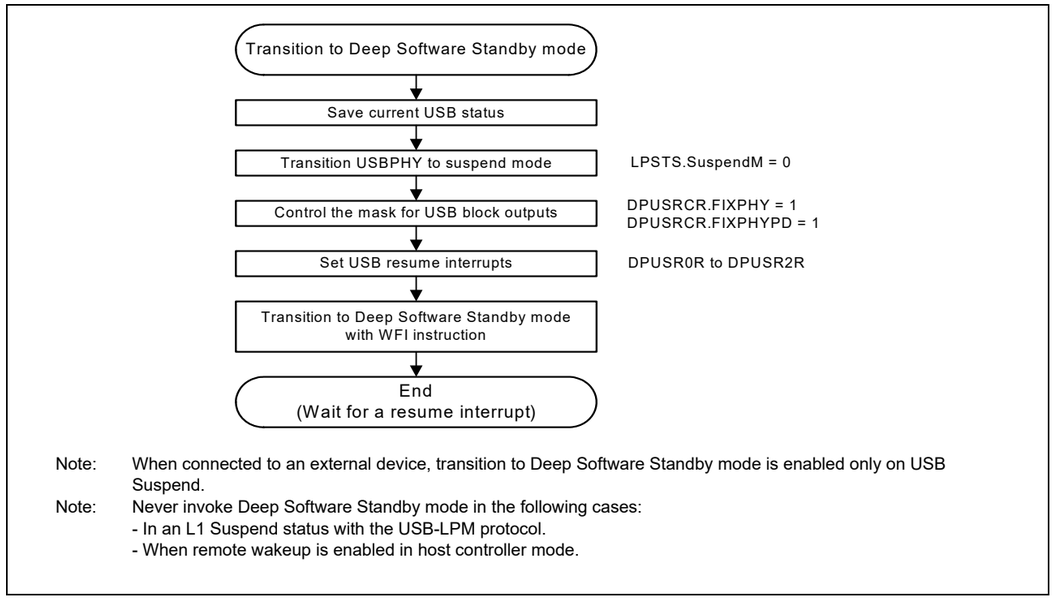
与从挂起(L2)状态返回时不同，USBHS将DVSTCTR0.RESUME位清除为0。清除RESUME位后，将DVSTCTR0.UACT位设置为1并发出L1RSMEND中断请求。

33.3.17 由于USB挂起恢复而从深度软件待机模式中释放 Interrupts

深度软件待机模式可以通过USB挂起恢复中断来取消。USB暂停恢复中断由USB恢复检测单元检测，该单元控制和监视USBIO引脚以检测中断。

图33.22显示了从主机或设备控制器模式进入深度软件待机模式时设置USBHS的流程。图33.23和图33.24显示了从主机控制器模式取消深度软件待机模式时设置USBHS的流程。图33.25显示取消时设置USBHS的流程

设备控制器模式下的深度软件待机模式。



Note: When connected to an external device, transition to Deep Software Standby mode is enabled only on USB Suspend.
Note: Never invoke Deep Software Standby mode in the following cases:
- In an L1 Suspend status with the USB-LPM protocol.
- When remote wakeup is enabled in host controller mode.

Figure 33.22 USBHS setup flow for transition to Deep Software Standby mode as a host or device controller

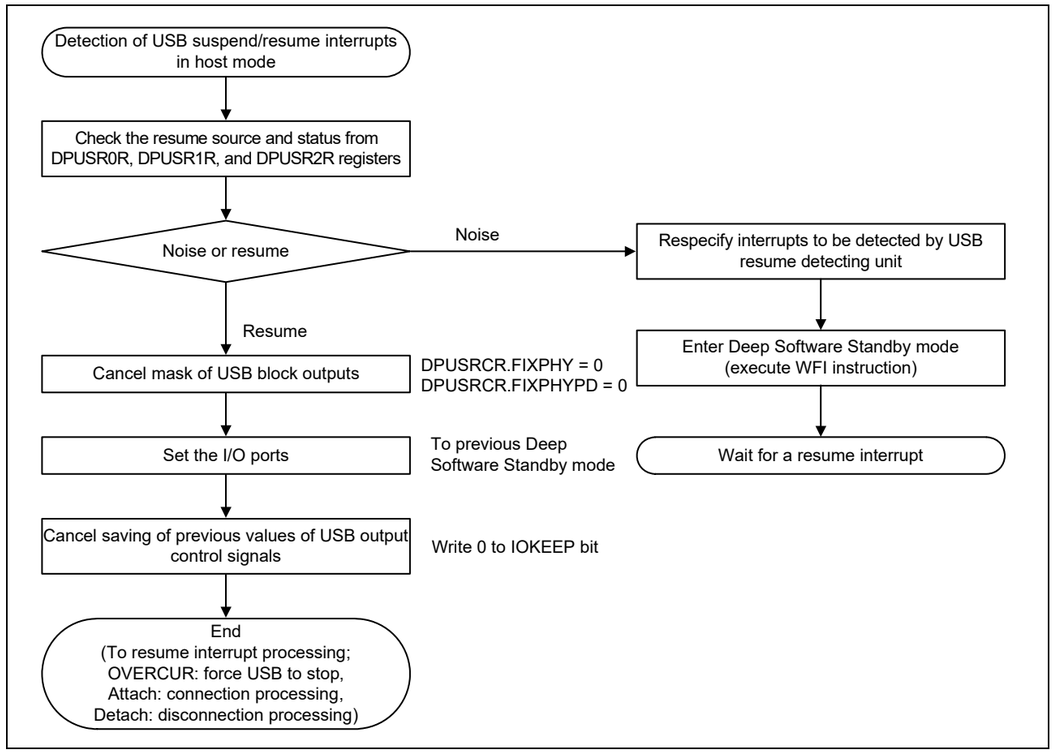
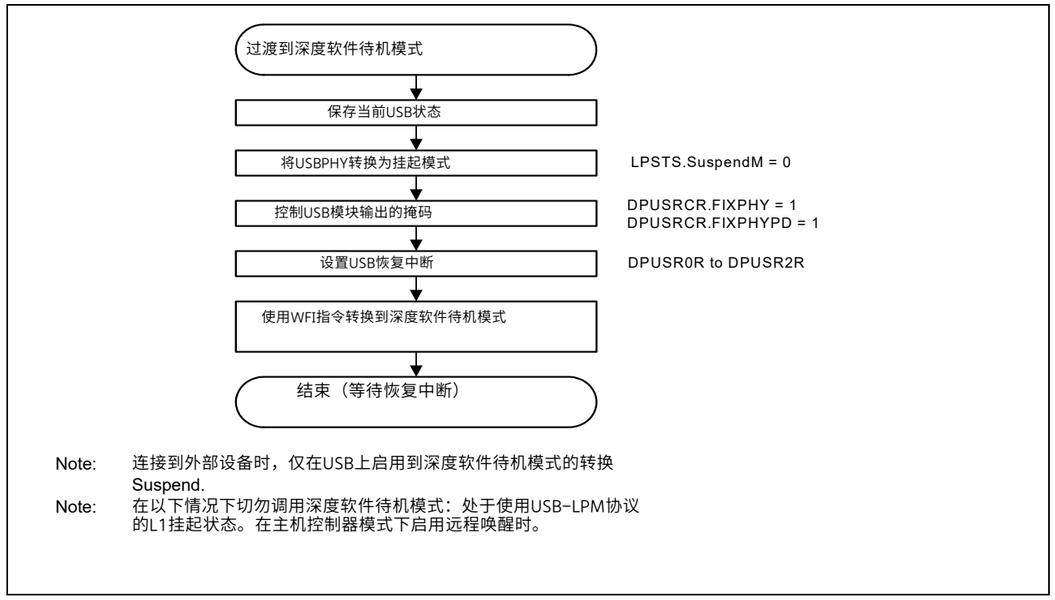


Figure 33.23 USBHS setup flow for canceling Deep Software Standby mode as a host controller (1)



Note: 连接到外部设备时，仅在USB上启用到深度软件待机模式的转换Suspend.
Note: 在以下情况下切勿调用深度软件待机模式：处于使用USB-LPM协议的L1挂起状态。在主机控制器模式下启用远程唤醒时。

Figure 33.22 作为主机或设备控制器转换到深度软件待机模式的USBHS设置流程

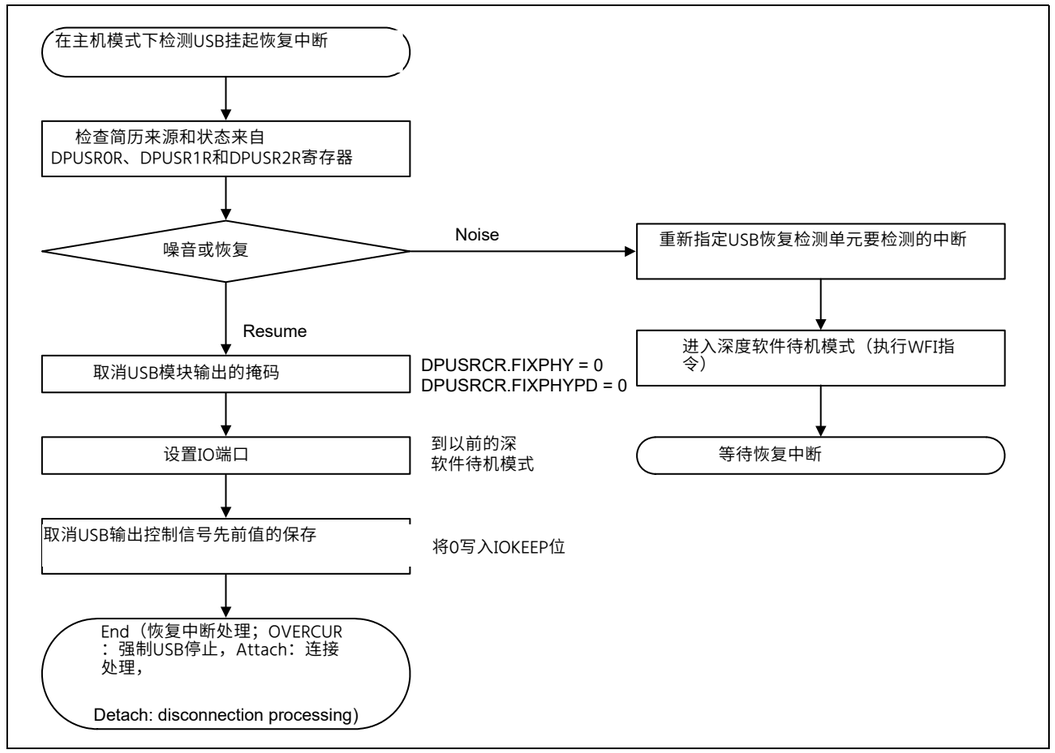


Figure 33.23 用于取消作为主机控制器的深度软件待机模式的USBHS设置流程(1)

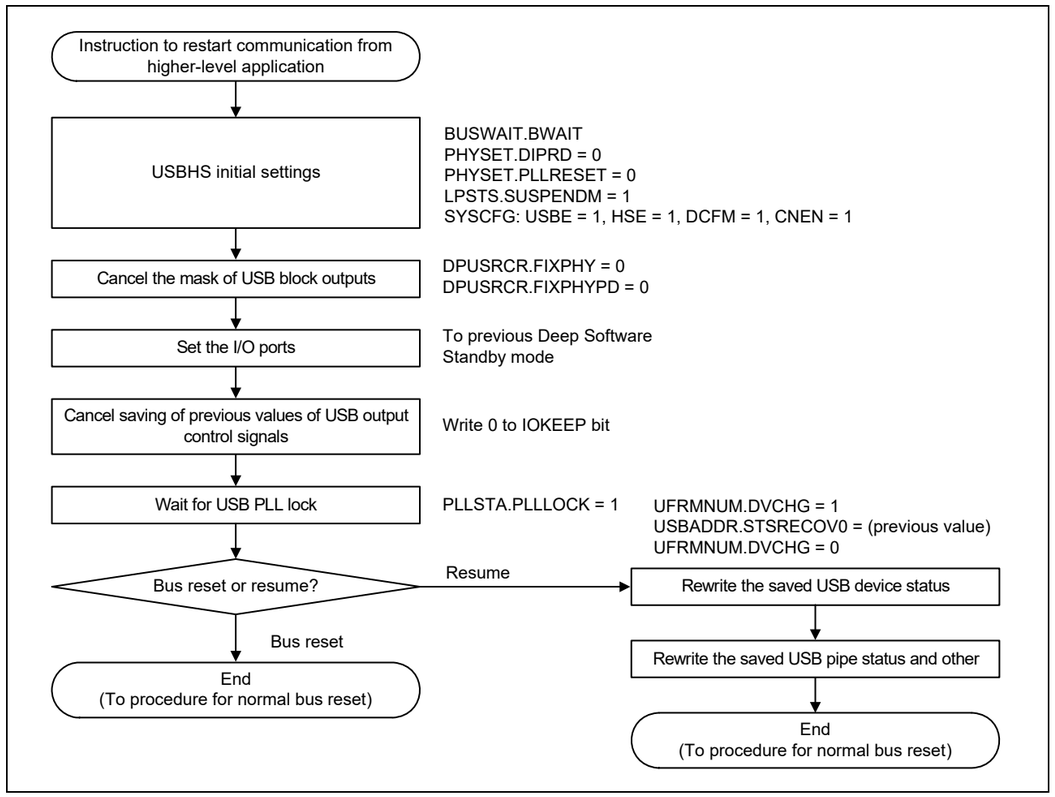


Figure 33.24 USBHS setup flow for canceling Deep Software Standby mode as a host controller (2)

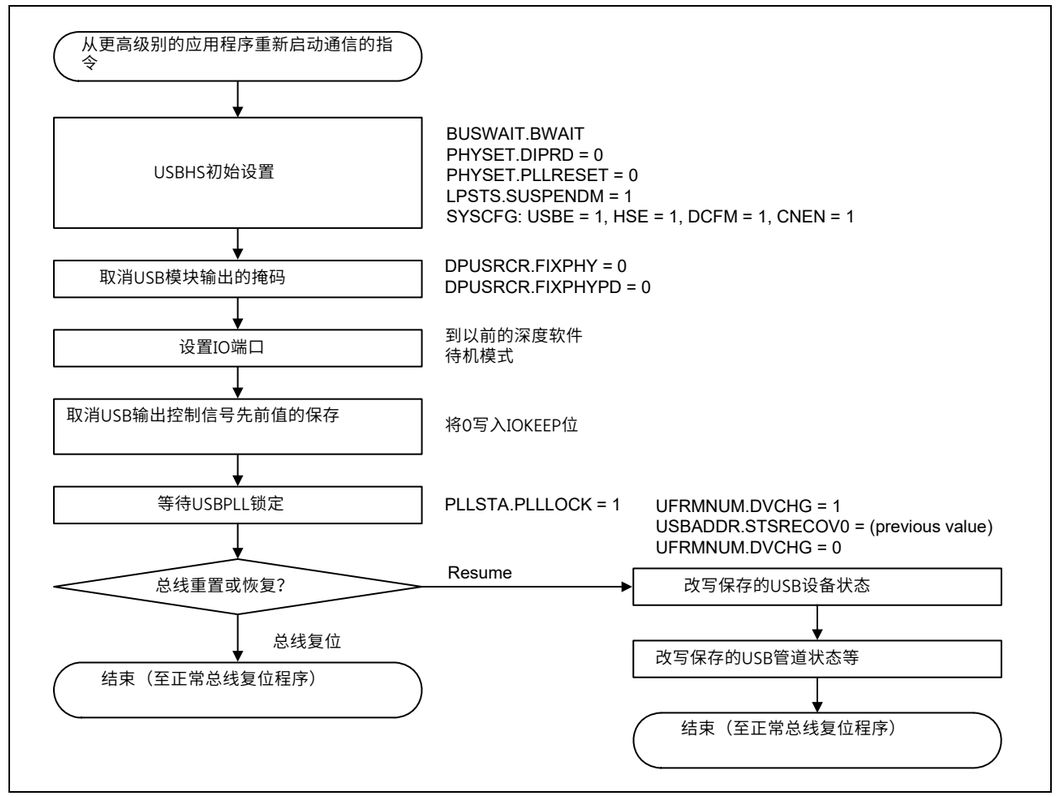
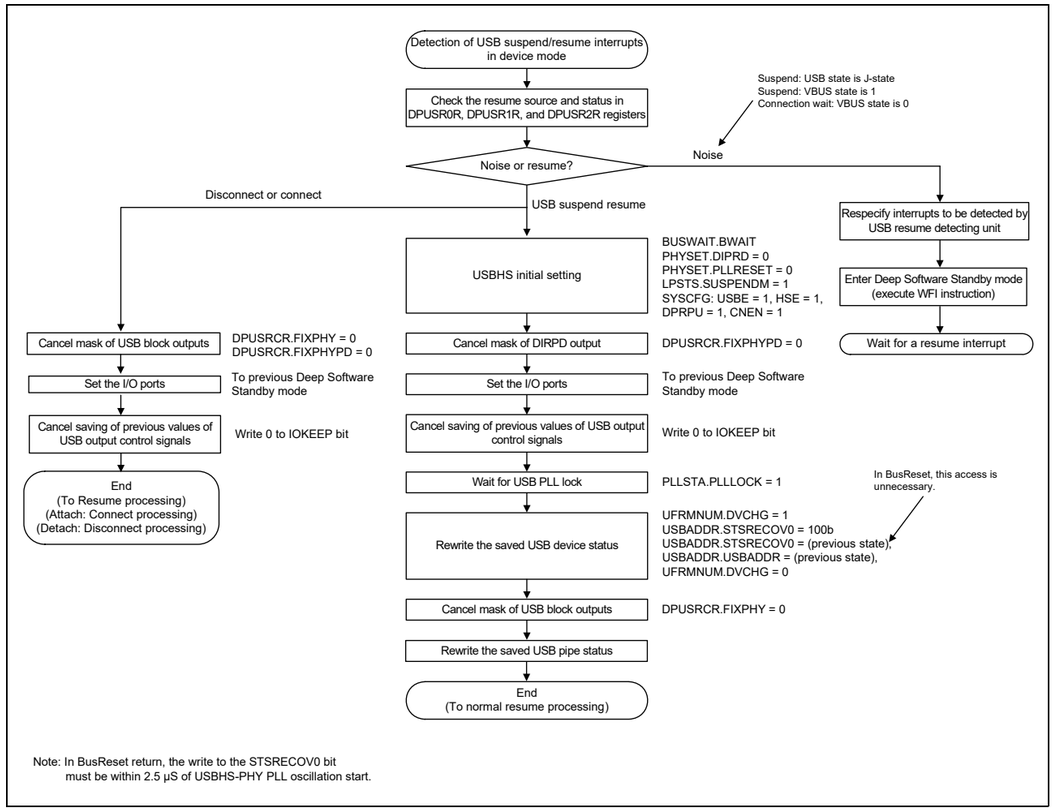
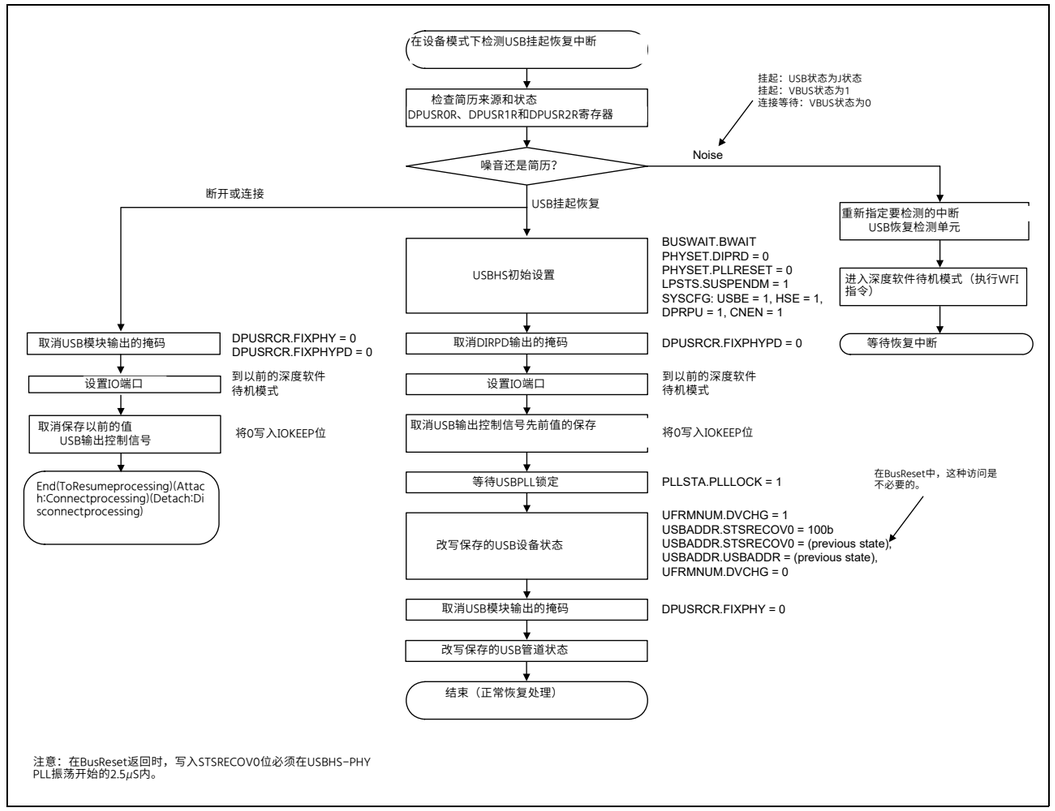


Figure 33.24 用于取消作为主机控制器的深度软件待机模式的USBHS设置流程(2)



Note: In BusReset return, the write to the STSRECOV0 bit must be within 2.5 µS of USBHS-PHY PLL oscillation start.

Figure 33.25 USBHS setup flow for canceling Deep Software Standby mode as a device controller (1)



注意：在BusReset返回时，写入STSRECOV0位必须在USBHS-PHY PLL振荡开始的2.5µS内。

Figure 33.25 用于取消作为设备控制器的深度软件待机模式的USBHS设置流程(1)

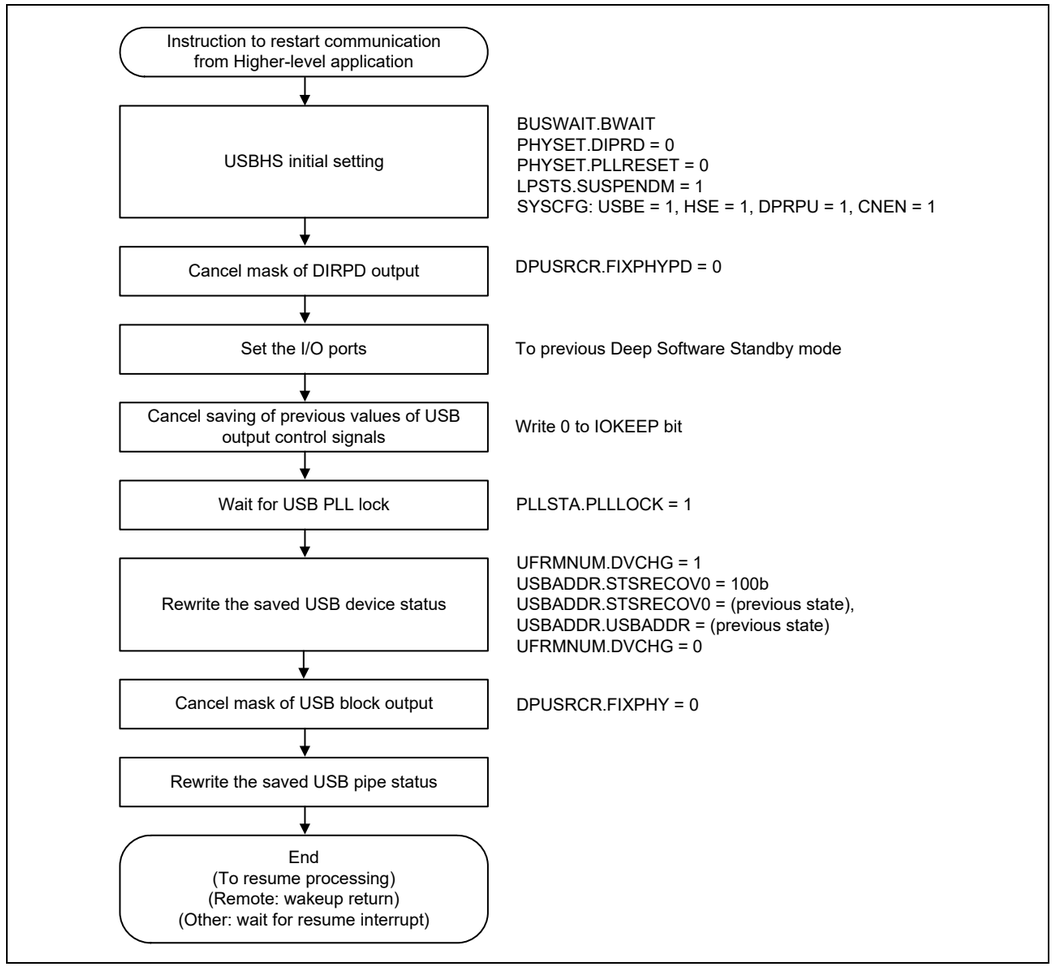


Figure 33.26 USBHS setup flow for canceling Deep Software Standby mode as a device controller (2)

33.3.18 Example External Connection Circuits

Figure 33.27 shows an example OTG connection in a self-powered system. The USBHS controls the pull-up resistor of the D+ line and the pull-down resistor of D+ and D- lines. Select pull-up and pull-down for the lines in the SYSCFG.DPRPU and SYSCFG.DRPD bits. In device controller mode, the pull-up resistor of USB data line is disabled if SYSCFG.DPRPU bit is set to 0 while communicating with the USB host. The USBHS can use this to notify the USB host of a device disconnect.

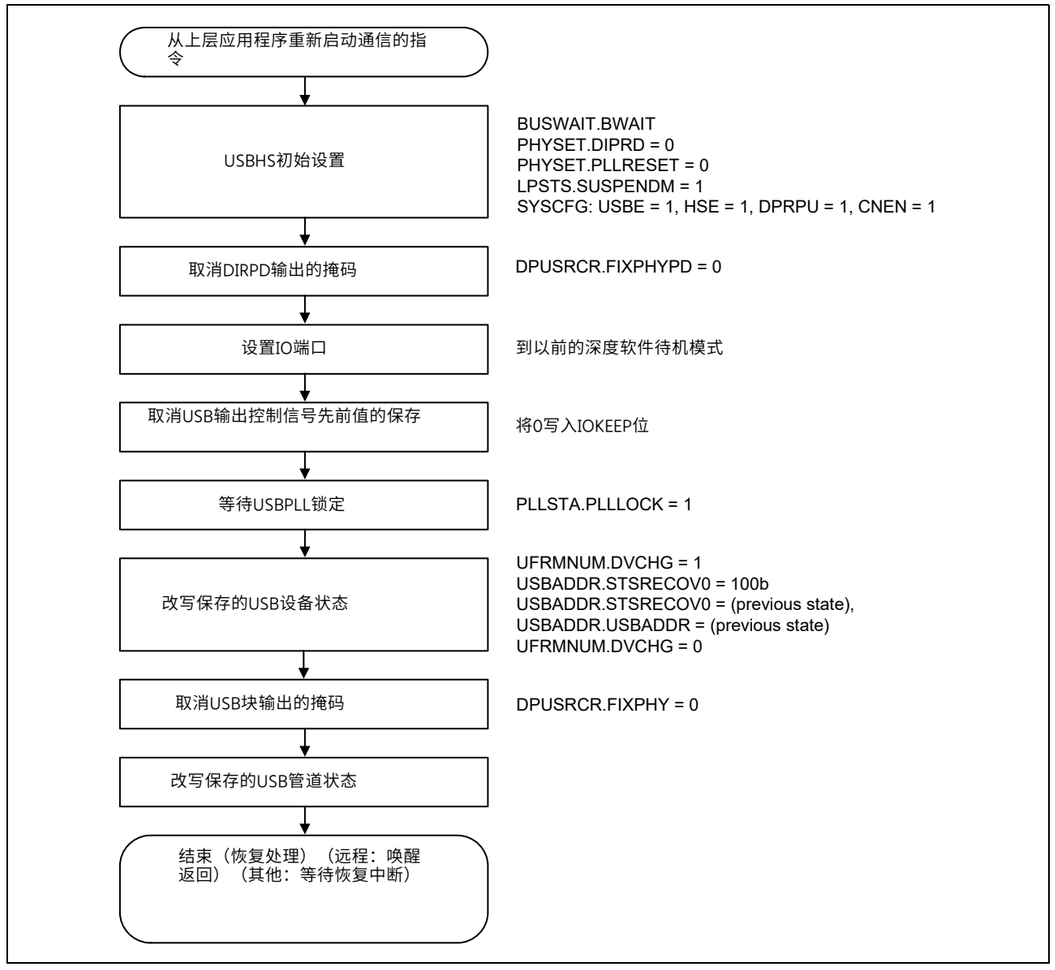


Figure 33.26 用于取消作为设备控制器的深度软件待机模式的USBHS设置流程(2)

33.3.18 外部连接电路示例

图33.27显示了自供电系统中的示例OTG连接。USBHS控制D+线的上拉电阻和D+、D线的下拉电阻。为SYSCFG.DPRPU和SYSCFG.DRPD位中的线路选择上拉和下拉。在设备控制器模式下，USB数据线的上拉电阻被禁用，如果

与USB主机通信时，SYSCFG.DPRPU位设置为0。USBHS可以使用它来通知USB主机设备断开连接。

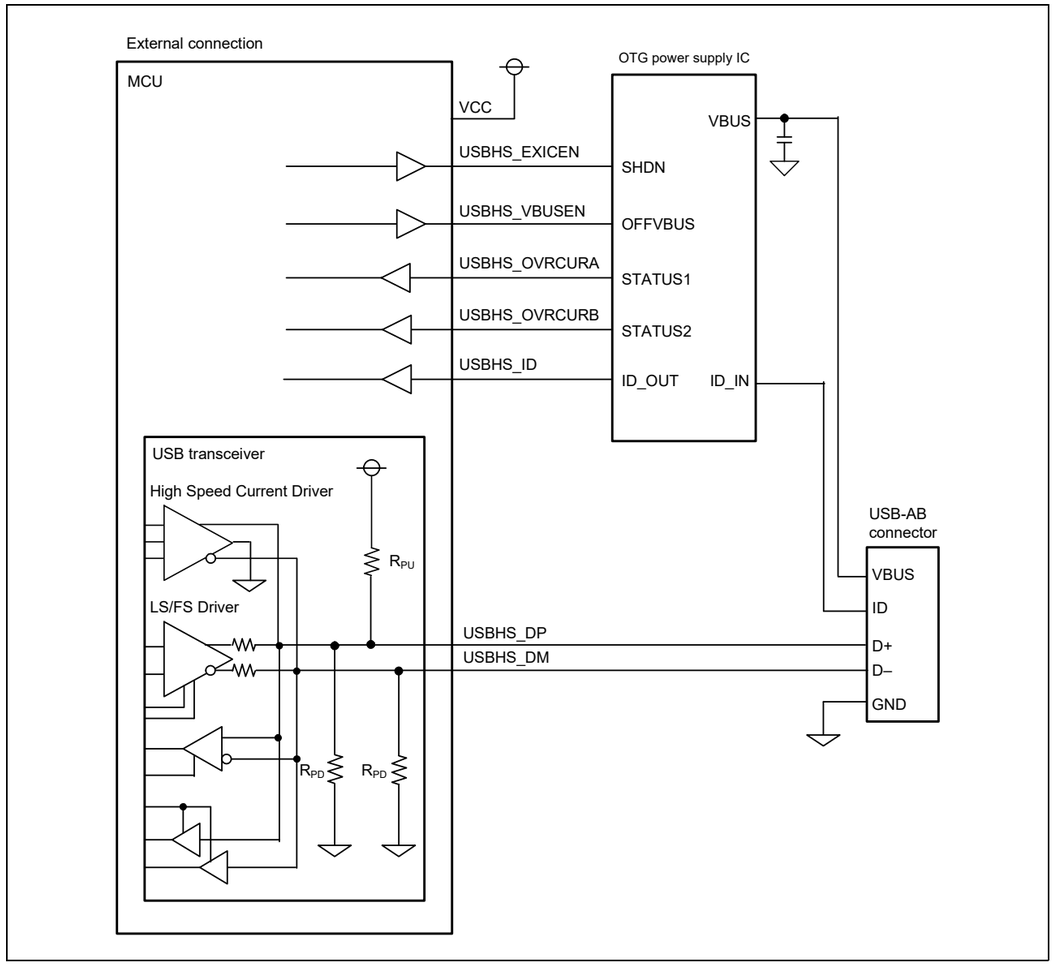


Figure 33.27 Example OTG connection in a self-powered system

Figure 33.28 shows an example USB device connection in a self-powered system.

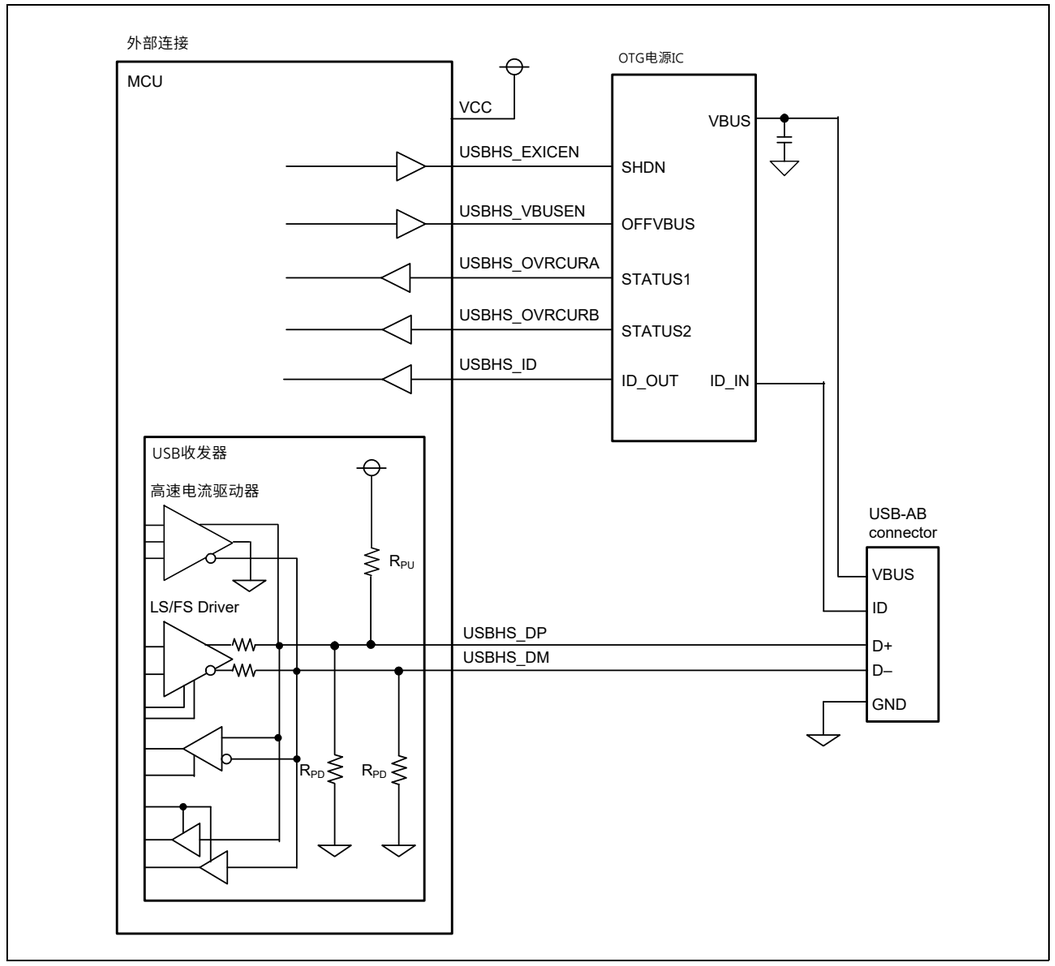


Figure 33.27 自供电系统中的示例OTG连接

图33.28显示了自供电系统中的USB设备连接示例。

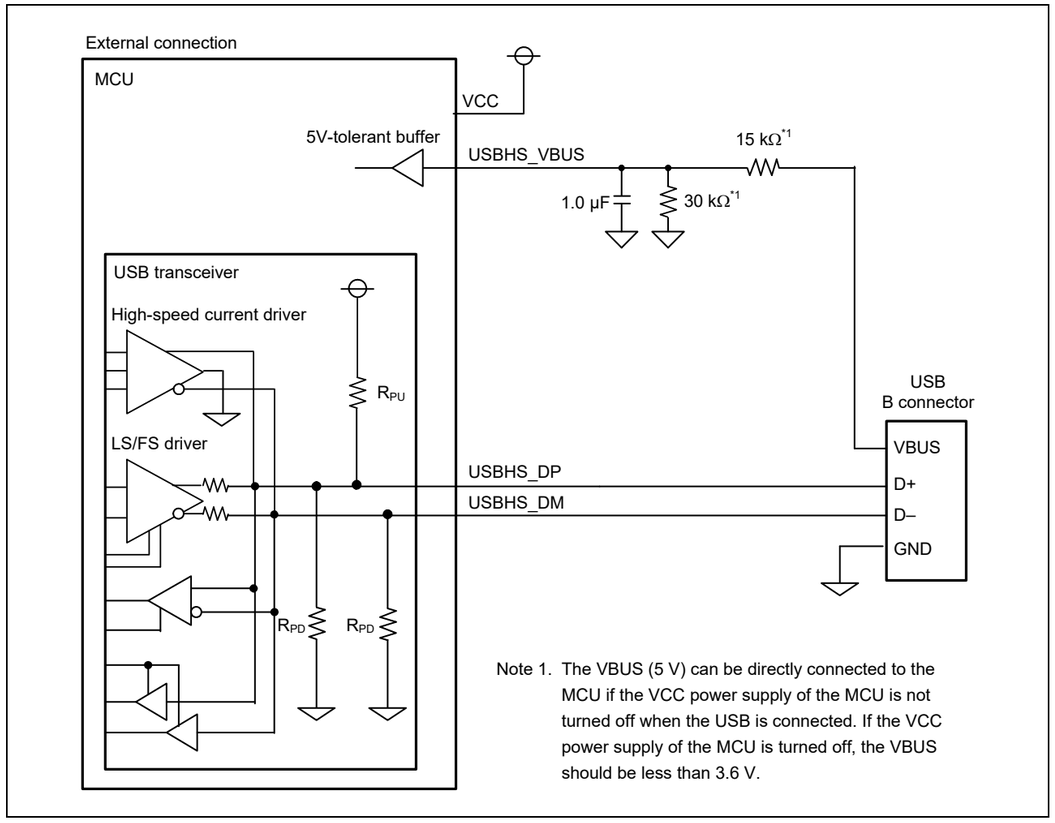


Figure 33.28 Example device connection in self-powered system

Figure 33.29 shows an example USB device connection in a bus-powered system.

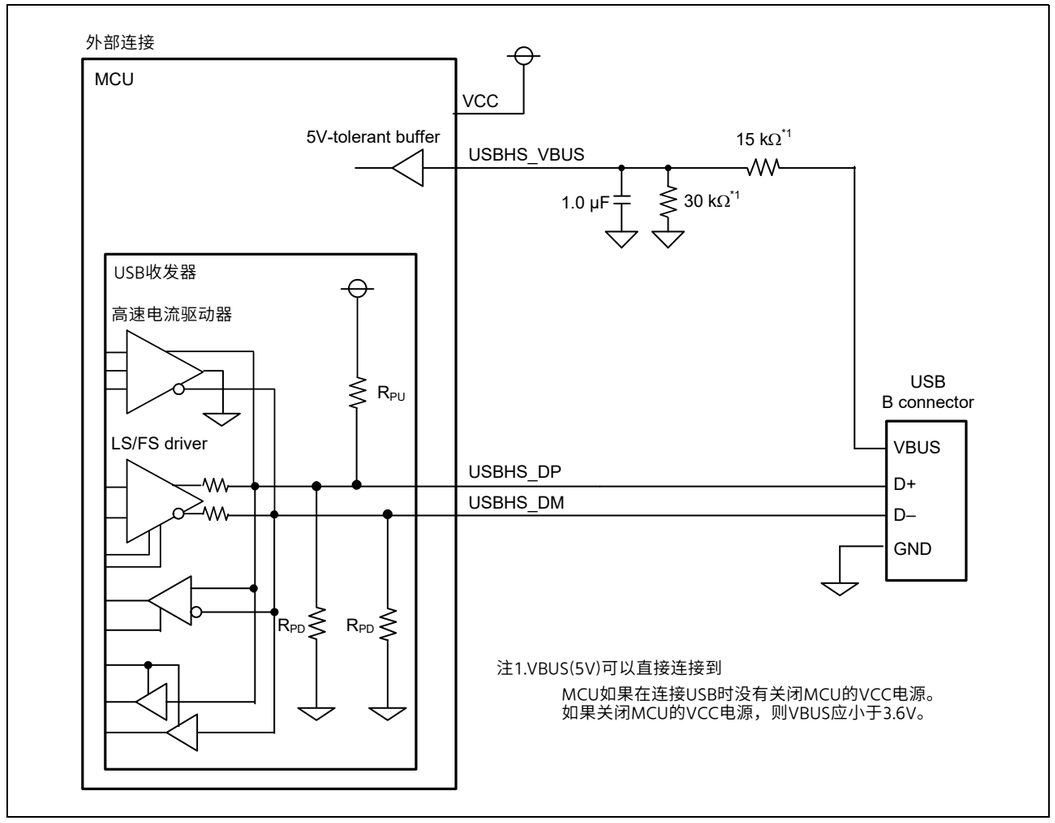


Figure 33.28 自供电系统中的示例设备连接

图33.29显示了总线供电系统中的USB设备连接示例。

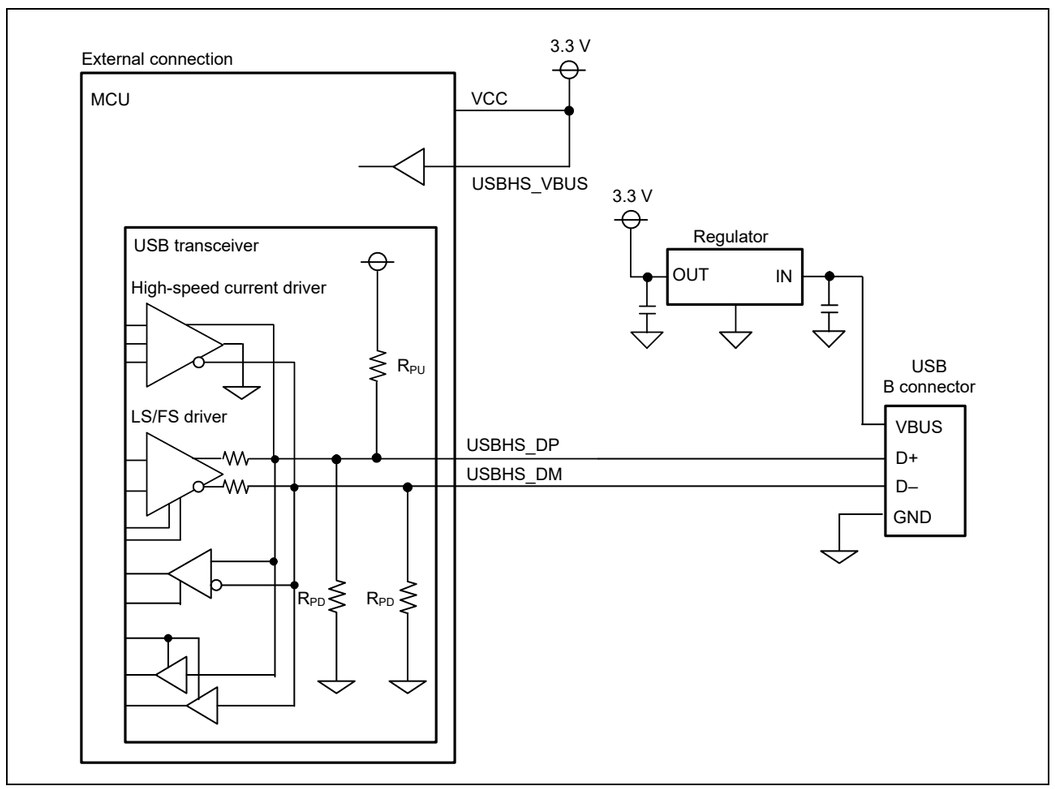


Figure 33.29 Example device connection in a bus-powered system

Figure 33.30 shows an example USB host connection.

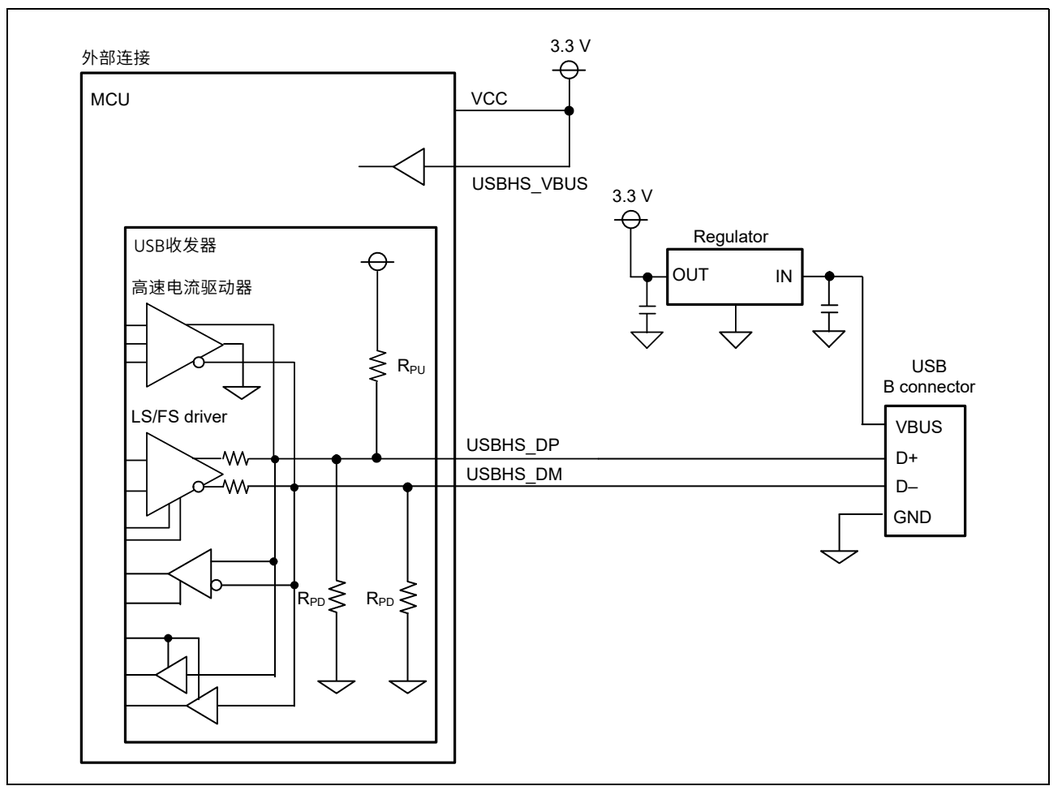


Figure 33.29 总线供电系统中的示例设备连接

图33.30显示了一个示例USB主机连接。

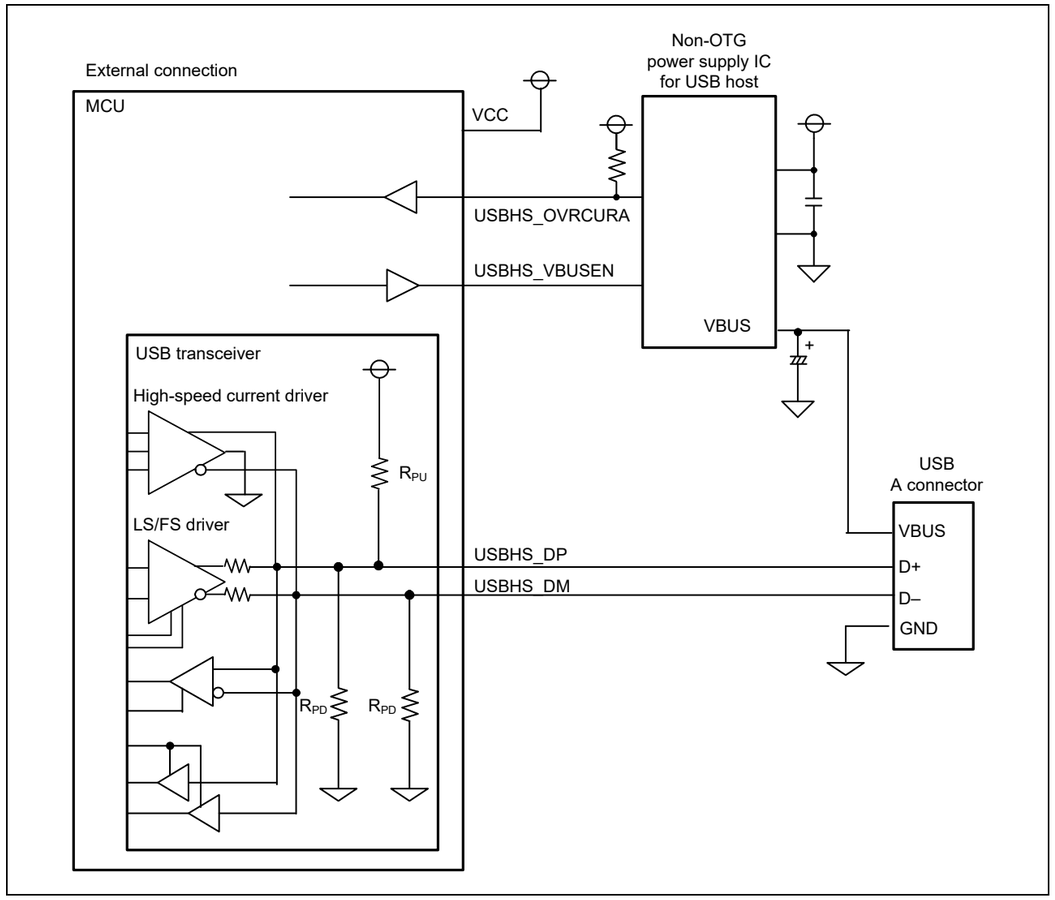


Figure 33.30 Example USB host connection

33.4 Usage Notes

33.4.1 Settings for the Module-Stop Function

USBHS operation can be disabled or enabled using Module Stop Control Register B (MSTPCRB). The USBHS is initially stopped after reset. Releasing the module-stop state enables access to the registers. After releasing module stop, make settings required to activate the PHY circuit, including the input system clock frequency setting, and then clear the PHYSET.DIRPD bit to 0. For details, see section 11, Low Power Modes.

33.4.2 Setup for Transitioning to Deep Software Standby Mode

Before transitioning to Deep Software Standby mode, clear the DVSTCTR0.VBUSEN bit to 0.

33.4.3 Clearing the Interrupt Status Register on Exiting Software Standby Mode

Because the input buffer is always enabled in Software Standby mode, an unexpected interrupt might occur under the following conditions:

- When the interrupt is enabled in Normal mode
- When the interrupt is disabled in Software Standby mode
- When the input level of the pin that cancels Software Standby is changed in Software Standby mode.

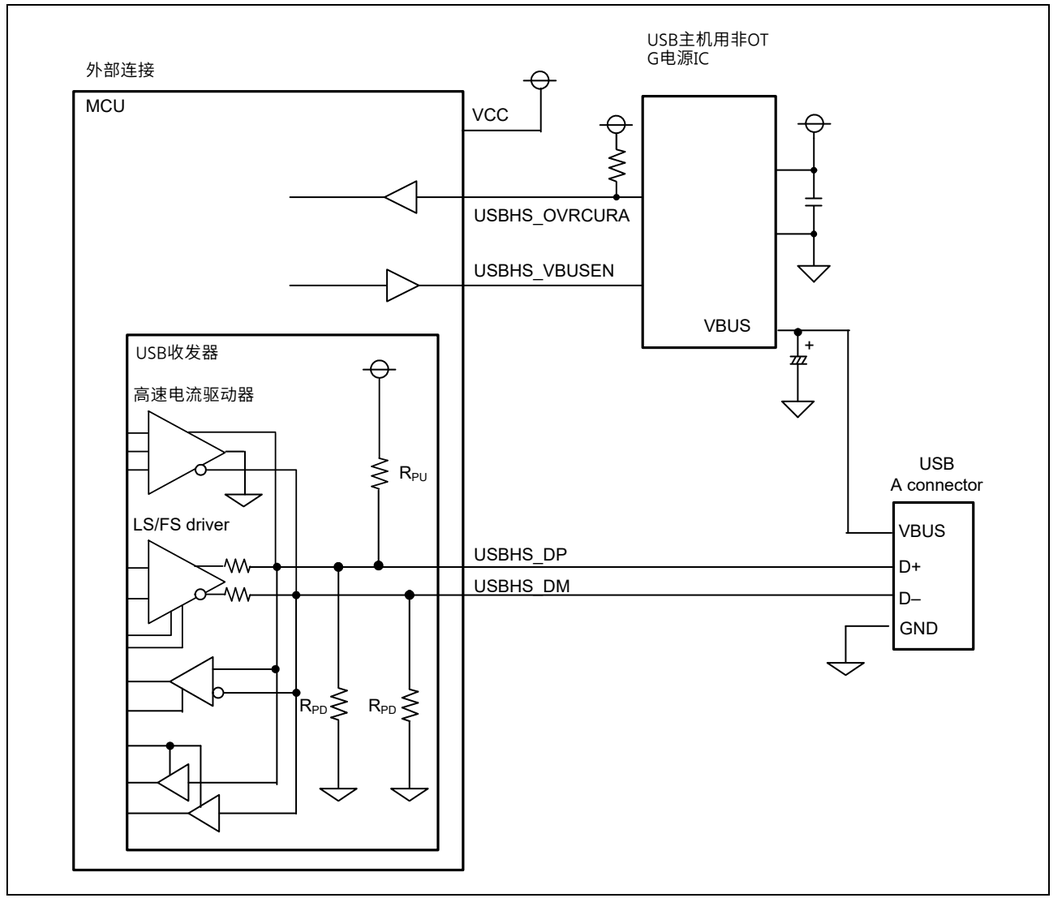


Figure 33.30 示例USB主机连接

33.4 使用说明

33.4.1 模块停止功能的设置

可以使用模块停止控制寄存器B(MSTPCRB)禁用或启用USBHS操作。USBHS在复位后最初停止。释放模块停止状态可以访问寄存器。释放模块停止后，进行激活PHY电路所需的设置，包括输入系统时钟频率设置，然后将PHYSET.DIRPD位清为0。详细信息请参见第11节，低功耗模式。

33.4.2 转换到深度软件待机模式的设置

在转换到深度软件待机模式之前，将DVSTCTR0.VBUSEN位清零。

33.4.3 退出软件待机模式时清除中断状态寄存器

由于在软件待机模式下始终启用输入缓冲区，因此在以下情况下可能会发生意外中断：

- 在正常模式下启用中断时
- 在软件待机模式下禁用中断时
- 在软件待机模式下，当取消软件待机的引脚的输入电平发生变化时。

These conditions might cause the associated interrupt flag in the Interrupt Status Register to set unexpectedly. After the MCU exits the Software Standby mode, the unexpected interrupt might be sent to the interrupt controller. To avoid this, always clear the INTSTS0 and INTSTS1 registers in the canceling sequence.

33.4.4 Clearing the Interrupt Status Register after Setting Up the Port Function

The input buffer is disabled before the PmnPFS.PSEL and PmnPFS.PMR ports are set up, so the internal signal is fixed high or low. The input buffer is enabled after the port is set so that the external pin state is propagated to the MCU. An unexpected interrupt might occur at this time, causing the VBINT and OVRCR bits in INTSTS0 and INTSTS1, or other interrupt status flags to set to 1. To avoid a malfunction, always clear the INTSTS0 and INTSTS1 registers after setting up the port.

这些情况可能会导致中断状态寄存器中的相关中断标志意外设置。MCU退出软件待机模式后，可能会向中断控制器发送意外中断。为避免这种情况，请始终在取消序列中清除INTSTS0和INTSTS1寄存器。

33.4.4 设置端口功能后清除中断状态寄存器

在设置PmnPFS.PSEL和PmnPFS.PMR端口之前，输入缓冲器被禁用，因此内部信号固定为高或低。设置端口后启用输入缓冲器，以便将外部引脚状态传播到MCU。此时可能会发生意外中断，导致INTSTS0和INTSTS1中的VBINT和OVRCR位或其他中断状态标志设置为1。为避免故障，请在设置端口后始终清除INTSTS0和INTSTS1寄存器。

34. Serial Communications Interface (SCI)

34.1 Overview

The Serial Communications Interface (SCI) is configurable to five asynchronous and synchronous serial interfaces:

- Asynchronous interfaces (UART and Asynchronous Communications Interface Adapter (ACIA))
- 8-bit clock synchronous interface
- Simple IIC (master-only)
- Simple SPI
- Smart card interface.

The smart card interface complies with the ISO/IEC 7816-3 standard for electronic signals and transmission protocol. Each SCI has FIFO buffers to enable continuous and full-duplex communication, and the data transfer speed can be configured independently using an on-chip baud rate generator.

Table 34.1 lists the SCI specifications, Figure 34.1 shows a block diagram of SCI channel n, and Table 34.2 lists the I/O pins by mode.

Table 34.1 SCI specifications (1 of 2)

Parameter	Specifications
Serial communication modes	• Asynchronous • Clock synchronous • Smart card interface • Simple IIC • Simple SPI.
Transfer speed	Bit rate specifiable with the on-chip baud rate generator
Full-duplex communications	• Transmitter: Continuous transmission possible using double-buffering • Receiver: Continuous reception possible using double-buffering
I/O pins	See Table 34.2
Data transfer	Selectable as LSB-first or MSB-first transfer
Interrupt sources	Transmit end, transmit data empty, receive data full, receive error, receive data ready, and address match Completion of generation of a start condition, restart condition, or stop condition (for simple IIC mode)
Module-stop function	Module-stop state can be set for each channel
Snooze end request	SCI0 address mismatch (SCI0_DCUF)

34. 串行通信接口(SCI)

34.1 Overview

串行通信接口(SCI)可配置为五个异步和同步串行接口：

- 异步接口（UART和异步通信接口适配器(ACIA)）
- 8位时钟同步接口
- Simple IIC (master-only)
- 简单的SPI
- 智能卡接口。

智能卡接口符合ISOIEC7816-3电子信号和传输协议标准。
每个SCI都有FIFO缓冲区以实现连续和全双工通信，并且可以使用片上波特率发生器独立配置数据传输速度。

表34.1列出了SCI规格，图34.1显示了SCI通道n的框图，表34.2列出了按模式划分的IO引脚。

Table 34.1 SCI规范(1of2)

Parameter	Specifications
串行通信模式	异步 时钟同步 智能卡接口 简单IIC 简单SPI。
传输速度	可通过片上波特率发生器指定比特率
Full-duplex communications	发送器：可以使用双缓冲进行连续传输 接收器：可以使用双缓冲进行连续接收
I/O pins	见表34.2
数据传输	可选择LSB优先或MSB优先传输
中断源	发送结束、发送数据空、接收数据满、接收错误、接收数据就绪、地址匹配开始条件、重启条件或停止条件的生成完成（对于简单IIC模式）
Module-stop function	每个通道可设置模块停止状态
暂停结束请求	SCI0地址不匹配(SCI0_DCUF)

Table 34.1 SCI specifications (2 of 2)

Parameter		Specifications
Asynchronous mode	Data length	7, 8, or 9 bits
	Transmission stop bit	1 or 2 bits
	Parity	Even parity, odd parity, or no parity
	Receive error detection	Parity, overrun, and framing errors
	Hardware flow control	Transmission and reception controllable with CTSn_RTSn pins
	Transmission and reception	Selectable to 1-stage register or 16-stage FIFO
	Address match	Interrupt request/event output can be issued upon detecting a match between received data and the value in the compare match register
	Address non-match (SCI0 only) receive data	Snooze end request can be issued upon detecting a non-match between the received data and the value in the compare match register
	Start-bit detection	Selectable to low level or falling edge detection
	Break detection	Breaks from framing errors detectable by reading from SPTR register
	Clock source	Selectable to internal or external clock
	Double-speed mode	Baud rate generator double-speed mode is selectable
	Multi-processor communications function	Serial communication enabled among multiple processors
	Noise cancellation	Digital noise filters included on signal paths from the RXDn pin inputs
Clock synchronous mode	Data length	8 bits
	Receive error detection	Overrun error
	Clock source	Selectable to internal clock (master mode) or external clock (slave mode)
	Hardware flow control	Transmission and reception controllable with CTSn_RTSn pins
	Transmission and reception	Selectable to 1-stage register or 16-stage FIFO
Smart card interface mode	Error processing	Error signal can be automatically transmitted upon detecting a parity error during reception
		Data can be automatically retransmitted upon receiving an error signal during transmission
	Data type	Both direct and inverse convention supported
Simple IIC mode	Transfer format	I^2C bus format (MSB-first only)
	Operating mode	Master (single-master operation only)
	Transfer rate	Up to 400 kbps
	Noise cancellation	The signal paths from input on the SCLn and SDAn pins incorporate digital noise filters, and provide an adjustable interval for noise cancellation
Simple SPI mode	Data length	8 bits
	Error detection	Overrun error
	Clock source	Selectable to internal clock (master mode) or external clock (slave mode)
	SS input pin function	High impedance state can be invoked on the output pins by driving the SSn pin high
	Clock settings	Configurable among four clock phase and clock polarity settings
Bit rate modulation function		Error reduction through correction of outputs from the on-chip baud rate generator
Event link function		Error event output for receive error or error signal detection (SCIn_ERI, n = 0 to 9)
		Receive data full event output (SCIn_RXI, n = 0 to 9)*1
		Transmit data empty event output (SCIn_TXI, n = 0 to 9)*1
		Transmit end event output (SCIn_TEI, n = 0 to 9)*1
		Address match event output (SCIn_AM, n = 0 to 9)

Table 34.1 SCI规范（2个中的2个）

Parameter		Specifications
异步模式	数据长度	7、8或9位
	传输停止位	1或2位
	Parity	偶校验、奇校验或无校验
	接收错误检测	奇偶校验、溢出和成帧错误
	硬件流控制	可通过CTSn_RTSn引脚控制发送和接收
	传输和接收	可选择1级寄存器或16级FIFO
	地址匹配	检测到接收数据与比较匹配寄存器中的值匹配时，可以发出中断请求事件输出
	地址不匹配（仅SCI0）接收数据	检测到接收到的数据与比较匹配寄存器中的值不匹配时，可以发出贪睡结束请求
	Start-bit detection	可选择低电平或下降沿检测
	断线检测	通过从SPTR寄存器读取可检测到的帧错误中断
	时钟源	可选择内部或外部时钟
	Double-speed mode	波特率发生器双速模式可选
	多处理器通讯功能	在多个处理器之间启用串行通信
	噪音消除	来自RXDn引脚输入的信号路径上包含数字噪声滤波器
时钟同步模式	数据长度	8 bits
	接收错误检测	溢出错误
	时钟源	可选择内部时钟（主模式）或外部时钟（从模式）
	硬件流控制	可通过CTSn_RTSn引脚控制发送和接收
	传输和接收	可选择1级寄存器或16级FIFO
智能卡接口方式	错误处理	在接收过程中检测到奇偶校验错误时可以自动发送错误信号
		传输过程中接收到错误信号可自动重传数据
	数据类型	支持直接和反向约定
简单IIC模式	传输格式	I2C总线格式（仅MSB优先）
	操作模式	主机（仅限单主机操作）
	传输率	高达400kbps
	噪音消除	来自SCLn和SDAn引脚输入的信号路径包含数字噪声滤波器，并提供可调节的噪声消除间隔
简单SPI模式	数据长度	8 bits
	错误检测	溢出错误
	时钟源	可选择内部时钟（主模式）或外部时钟（从模式）
	SS输入引脚功能	通过将SSn引脚驱动为高电平，可以在输出引脚上调用高阻抗状态
	时钟设置	可在四个时钟相位和时钟极性设置之间进行配置
比特率调制功能		通过校正片上波特率发生器的输出来减少错误
事件链接功能		用于接收错误或错误信号检测的错误事件输出（SCIn_ERI，n=0到9）
		接收数据满事件输出(SCIn_RXI n=0to9)*1
		发送数据空事件输出(SCIn_TXI n=0to9)*1
		发送结束事件输出(SCIn_TEI n=0to9)*1
		地址匹配事件输出（SCIn_AM，n=0到9）

Note 1. Using this event link function is prohibited when FIFO operation is selected in asynchronous mode.

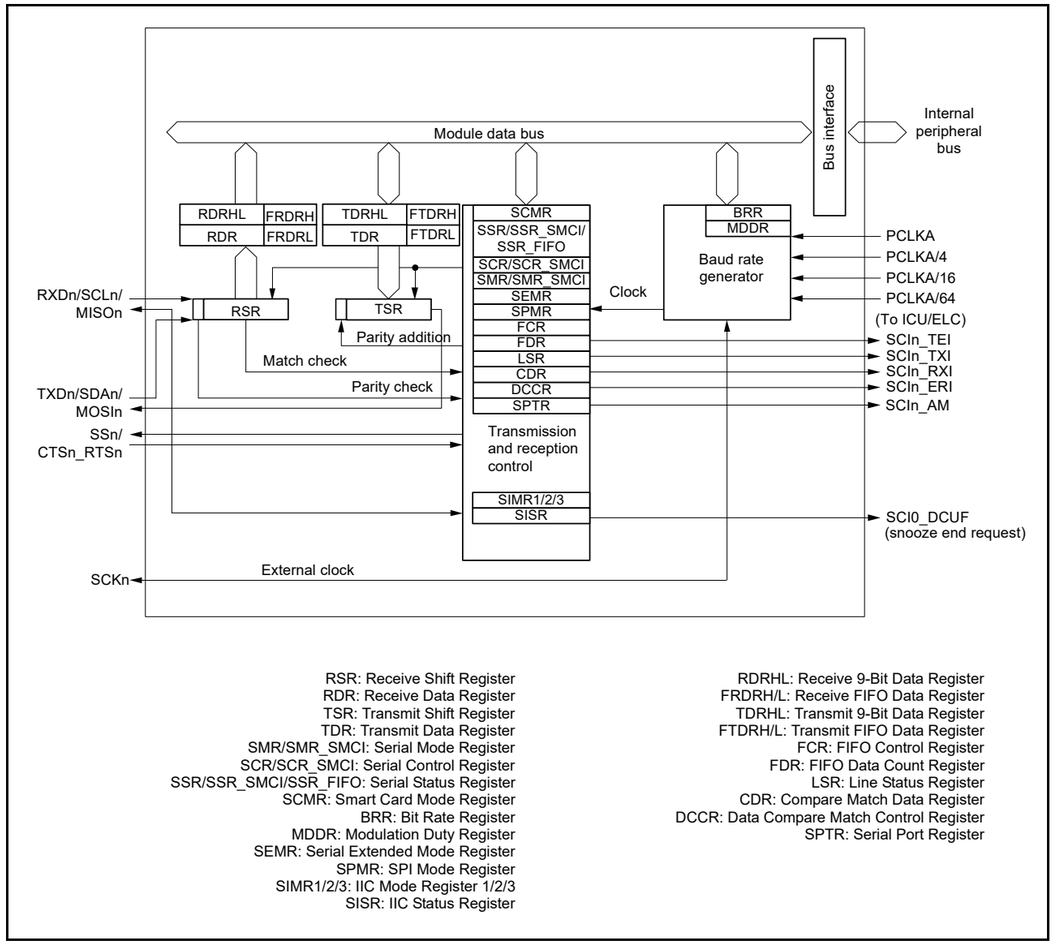


Figure 34.1 SCI channel n block diagram

Table 34.2 SCI I/O pins (1 of 3)

Channel	Pin name	I/O	Function
SCI0	SCK0	I/O	SCI0 clock input/output
	RXD0/SCL0/MISO0	I/O	SCI0 receive data input SCI0 IIC clock input/output SCI0 slave transmit data input/output
	TXD0/SDA0/MOSI0	I/O	SCI0 transmit data output SCI0 IIC data input/output SCI0 master transmit data input/output
	SS0/CTS0_RTS0	I/O	SCI0 chip select input, active low SCI0 transfer start control input/output, active low

注1.在异步模式下选择FIFO操作时，禁止使用此事件链接功能。

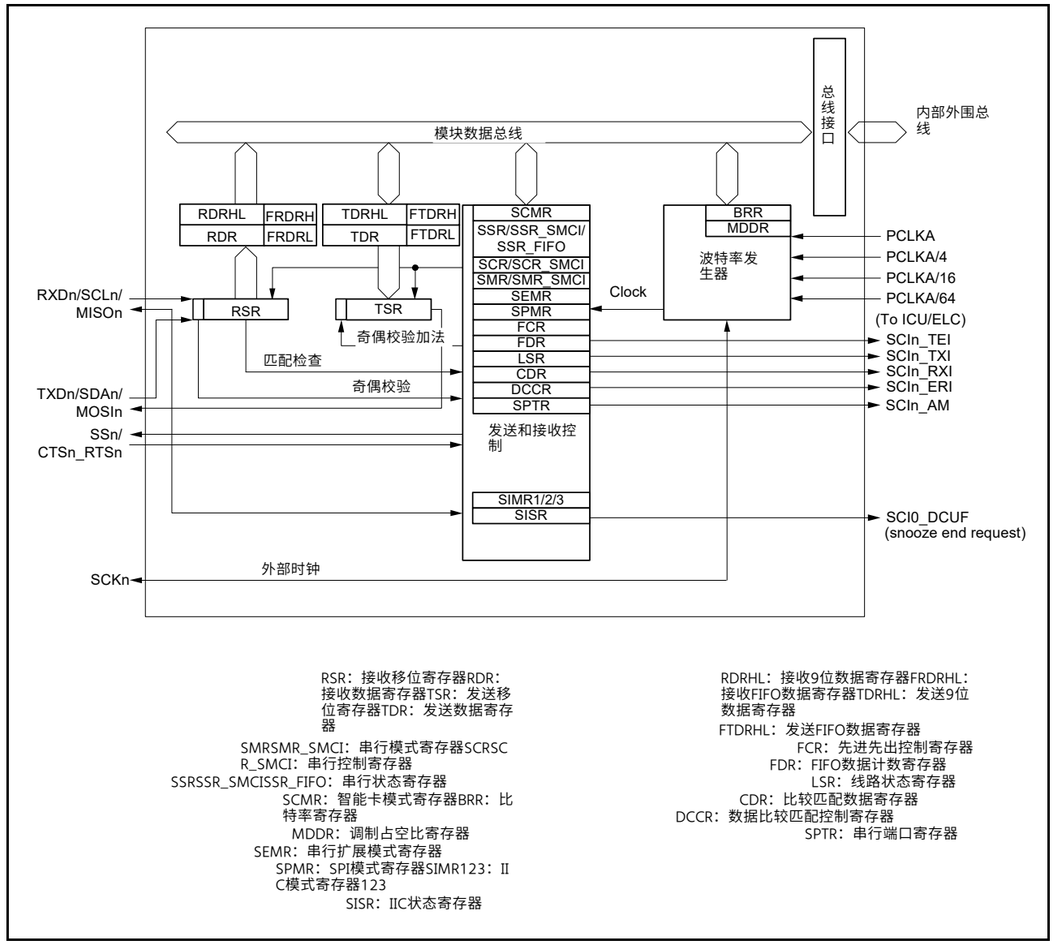


Figure 34.1 SCI通道n框图

Table 34.2 SCIIO引脚（3个中的1个）

Channel	引脚名称	I/O	Function
SCI0	SCK0	I/O	SCI0 clock input/output
	RXD0/SCL0/MISO0	I/O	SCI0接收数据输入 SCI0 IIC clock input/output SCI0从机发送数据输入输出
	TXD0/SDA0/MOSI0	I/O	SCI0发送数据输出SCI0IIC数据输入输出 SCI0主机发送数据输入输出
	SS0/CTS0_RTS0	I/O	SCI0片选输入，低电平有效 SCI0传输启动控制输入输出，低电平有效

Table 34.2 SCI I/O pins (2 of 3)

Channel	Pin name	I/O	Function
SCI1	SCK1	I/O	SCI1 clock input/output
	RXD1/SCL1/MISO1	I/O	SCI1 receive data input SCI1 IIC clock input/output SCI1 slave transmit data input/output
	TXD1/SDA1/MOSI1	I/O	SCI1 transmit data output SCI1 IIC data input/output SCI1 master transmit data input/output
	SS1/CTS1_RTS1	I/O	SCI1 chip select input, active low SCI1 transfer start control input/output, active low
SCI2	SCK2	I/O	SCI2 clock input/output
	RXD2/SCL2/MISO2	I/O	SCI2 receive data input SCI2 IIC clock input/output SCI2 slave transmit data input/output
	TXD2/SDA2/MOSI2	I/O	SCI2 transmit data output SCI2 IIC data input/output SCI2 master transmit data input/output
	SS2/CTS2_RTS2	I/O	SCI2 chip select input, active low SCI2 transfer start control input/output, active low
SCI3	SCK3	I/O	SCI3 clock input/output
	RXD3/SCL3/MISO3	I/O	SCI3 receive data input SCI3 IIC clock input/output SCI3 slave transmit data input/output
	TXD3/SDA3/MOSI3	I/O	SCI3 transmit data output SCI3 IIC data input/output SCI3 master transmit data input/output
	SS3/CTS3_RTS3	I/O	SCI3 chip select input, active low SCI3 transfer start control input/output, active low
SCI4	SCK4	I/O	SCI4 clock input/output
	RXD4/SCL4/MISO4	I/O	SCI4 receive data input SCI4 IIC clock input/output SCI4 slave transmit data input/output
	TXD4/SDA4/MOSI4	I/O	SCI4 transmit data output SCI4 IIC data input/output SCI4 master transmit data input/output
	SS4/CTS4_RTS4	I/O	SCI4 chip select input, active low SCI4 transfer start control input/output, active low
SCI5	SCK5	I/O	SCI5 clock input/output
	RXD5/SCL5/MISO5	I/O	SCI5 receive data input SCI5 IIC clock input/output SCI5 slave transmit data input/output
	TXD5/SDA5/MOSI5	I/O	SCI5 transmit data output SCI5 IIC data input/output SCI5 master transmit data input/output
	SS5/CTS5_RTS5	I/O	SCI5 chip select input, active low SCI5 transfer start control input/output, active low
SCI6	SCK6	I/O	SCI6 clock input/output
	RXD6/SCL6/MISO6	I/O	SCI6 receive data input SCI6 IIC clock input/output SCI6 slave transmit data input/output
	TXD6/SDA6/MOSI6	I/O	SCI6 transmit data output SCI6 IIC data input/output SCI6 master transmit data input/output
	SS6/CTS6_RTS6	I/O	SCI6 chip select input, active low SCI6 transfer start control input/output, active low

Table 34.2 SCIIO引脚（2个，共3个）

Channel	引脚名称	I/O	Function
SCI1	SCK1	I/O	SCI1 clock input/output
	RXD1/SCL1/MISO1	I/O	SCI1接收数据输入 SCI1 IIC clock input/output SCI1从机发送数据输入输出
	TXD1/SDA1/MOSI1	I/O	SCI1发送数据输出SCI1IIC 数据输入输出 SCI1主机发送数据输入输出
	SS1/CTS1_RTS1	I/O	SCI1片选输入，低电平有效 SCI1传输启动控制输入输出，低电平有效
SCI2	SCK2	I/O	SCI2 clock input/output
	RXD2/SCL2/MISO2	I/O	SCI2接收数据输入 SCI2 IIC clock input/output SCI2从机发送数据输入输出
	TXD2/SDA2/MOSI2	I/O	SCI2发送数据输出SCI2IIC 数据输入输出 SCI2主机发送数据输入输出
	SS2/CTS2_RTS2	I/O	SCI2片选输入，低电平有效 SCI2传输启动控制输入输出，低电平有效
SCI3	SCK3	I/O	SCI3 clock input/output
	RXD3/SCL3/MISO3	I/O	SCI3接收数据输入 SCI3 IIC clock input/output SCI3从机发送数据输入输出
	TXD3/SDA3/MOSI3	I/O	SCI3发送数据输出SCI3IIC 数据输入输出 SCI3主机发送数据输入输出
	SS3/CTS3_RTS3	I/O	SCI3片选输入，低电平有效 SCI3传输启动控制输入输出，低电平有效
SCI4	SCK4	I/O	SCI4 clock input/output
	RXD4/SCL4/MISO4	I/O	SCI4接收数据输入 SCI4 IIC clock input/output SCI4从机发送数据输入输出
	TXD4/SDA4/MOSI4	I/O	SCI4发送数据输出SCI4IIC 数据输入输出 SCI4主机发送数据输入输出
	SS4/CTS4_RTS4	I/O	SCI4片选输入，低电平有效 SCI4传输启动控制输入输出，低电平有效
SCI5	SCK5	I/O	SCI5 clock input/output
	RXD5/SCL5/MISO5	I/O	SCI5接收数据输入 SCI5 IIC clock input/output SCI5从机发送数据输入输出
	TXD5/SDA5/MOSI5	I/O	SCI5发送数据输出SCI5IIC 数据输入输出 SCI5主机发送数据输入输出
	SS5/CTS5_RTS5	I/O	SCI5片选输入，低电平有效 SCI5传输启动控制输入输出，低电平有效
SCI6	SCK6	I/O	SCI6 clock input/output
	RXD6/SCL6/MISO6	I/O	SCI6接收数据输入 SCI6 IIC clock input/output SCI6从机发送数据输入输出
	TXD6/SDA6/MOSI6	I/O	SCI6发送数据输出SCI6IIC 数据输入输出 SCI6主机发送数据输入输出
	SS6/CTS6_RTS6	I/O	SCI6片选输入，低电平有效 SCI6传输启动控制输入输出，低电平有效

Table 34.2 SCI I/O pins (3 of 3)

Channel	Pin name	I/O	Function
SCI7	SCK7	I/O	SCI7 clock input/output
	RXD7/SCL7/MISO7	I/O	SCI7 receive data input SCI7 IIC clock input/output SCI7 slave transmit data input/output
	TXD7/SDA7/MOSI7	I/O	SCI7 transmit data output SCI7 IIC data input/output SCI7 master transmit data input/output
	SS7/CTS7_RTS7	I/O	SCI7 chip select input, active low SCI7 transfer start control input/output, active low
SCI8	SCK8	I/O	SCI8 clock input/output
	RXD8/SCL8/MISO8	I/O	SCI8 receive data input SCI8 IIC clock input/output SCI8 slave transmit data input/output
	TXD8/SDA8/MOSI8	I/O	SCI8 transmit data output SCI8 IIC data input/output SCI8 master transmit data input/output
	SS8/CTS8_RTS8	I/O	SCI8 chip select input, active low SCI8 transfer start control input/output, active low
SCI9	SCK9	I/O	SCI9 clock input/output
	RXD9/SCL9/MISO9	I/O	SCI9 receive data input SCI9 IIC clock input/output SCI9 slave transmit data input/output
	TXD9/SDA9/MOSI9	I/O	SCI9 transmit data output SCI9 IIC data input/output SCI9 master transmit data input/output
	SS9/CTS9_RTS9	I/O	SCI9 chip select input, active low SCI9 transfer start control input/output, active low

34.2 Register Descriptions

34.2.1 Receive Shift Register (RSR)

RSR is a shift register that receives serial data input from the RXDn pin and converts it into parallel data. When one frame of data is received, it is automatically transferred to the RDR register, RDRHL register, or receive FIFO. The RSR register cannot be directly accessed by the CPU.

34.2.2 Receive Data Register (RDR)

Address(es): SCI0.RDR 4007 0005h, SCI1.RDR 4007 0025h, SCI2.RDR 4007 0045h, SCI3.RDR 4007 0065h, SCI4.RDR 4007 0085h, SCI5.RDR 4007 00A5h, SCI6.RDR 4007 00C5h, SCI7.RDR 4007 00E5h, SCI8.RDR 4007 0105h, SCI9.RDR 4007 0125h

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0

RDR is an 8-bit register that stores receive data. When one frame of serial data is received, it is transferred from the RSR register to the RDR register, and the RSR register can receive more data. Because RSR and RDR function as a double buffer in this way, continuous receive operations can be performed.

Read the RDR register only once after a receive data full interrupt (SCIn_RXI) occurs.

Note: If the next frame of data is received before the receive data is read from the RDR register, an overrun error occurs. The RDR register cannot be written to by the CPU.

Table 34.2 SCIIO引脚（3个中的3个）

Channel	引脚名称	I/O	Function
SCI7	SCK7	I/O	SCI7 clock input/output
	RXD7/SCL7/MISO7	I/O	SCI7接收数据输入 SCI7 IIC clock input/output SCI7从机发送数据输入输出
	TXD7/SDA7/MOSI7	I/O	SCI7发送数据输出SCI7IIC 数据输入输出 SCI7主机发送数据输入输出
	SS7/CTS7_RTS7	I/O	SCI7片选输入，低电平有效 SCI7传输启动控制输入输出，低电平有效
SCI8	SCK8	I/O	SCI8 clock input/output
	RXD8/SCL8/MISO8	I/O	SCI8接收数据输入 SCI8 IIC clock input/output SCI8从机发送数据输入输出
	TXD8/SDA8/MOSI8	I/O	SCI8发送数据输出SCI8IIC 数据输入输出 SCI8主机发送数据输入输出
	SS8/CTS8_RTS8	I/O	SCI8片选输入，低电平有效 SCI8传输启动控制输入输出，低电平有效
SCI9	SCK9	I/O	SCI9 clock input/output
	RXD9/SCL9/MISO9	I/O	SCI9接收数据输入 SCI9 IIC clock input/output SCI9从机发送数据输入输出
	TXD9/SDA9/MOSI9	I/O	SCI9发送数据输出SCI9IIC 数据输入输出 SCI9主机发送数据输入输出
	SS9/CTS9_RTS9	I/O	SCI9片选输入，低电平有效 SCI9传输启动控制输入输出，低电平有效

34.2 注册说明

34.2.1 接收移位寄存器(RSR)

RSR是一个移位寄存器，它接收从RXDn引脚输入的串行数据并将其转换为并行数据。当接收到一帧数据时，它会自动传输到RDR寄存器、RDRHL寄存器或接收FIFO。CPU不能直接访问RSR寄存器。

34.2.2 接收数据寄存器(RDR)

Address(es): SCI0.RDR 4007 0005h, SCI1.RDR 4007 0025h, SCI2.RDR 4007 0045h, SCI3.RDR 4007 0065h, SCI4.RDR 4007 0085h, SCI5.RDR 4007 00A5h, SCI6.RDR 4007 00C5h, SCI7.RDR 4007 00E5h, SCI8.RDR 4007 0105h, SCI9.RDR 4007 0125h

	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值:	0	0	0	0	0	0	0	0

RDR是一个8位寄存器，用于存储接收数据。当接收到一帧串行数据时，从RSR寄存器传送到RDR寄存器，RSR寄存器可以接收更多的数据。由于RSR和RDR以这种方式充当双缓冲器，因此可以执行连续接收操作。

在接收数据完全中断(SCIn_RXI)发生后，仅读取一次RDR寄存器。

Note: 如果在从RDR寄存器读取接收数据之前接收到下一帧数据，则会发生溢出错误。RDR寄存器不能被CPU写入。

34.2.3 Receive 9-Bit Data Register (RDRHL)

Address(es): SCI0.RDRHL 4007 0010h, SCI1.RDRHL 4007 0030h, SCI2.RDRHL 4007 0050h, SCI3.RDRHL 4007 0070h, SCI4.RDRHL 4007 0090h, SCI5.RDRHL 4007 00B0h, SCI6.RDRHL 4007 00D0h, SCI7.RDRHL 4007 00F0h, SCI8.RDRHL 4007 0110h, SCI9.RDRHL 4007 0130h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RDRHL is a 16-bit register that stores receive data. Use the RDRHL register when asynchronous mode and 9-bit data length are selected.

The lower 8 bits of RDRHL are a shadow register of RDR, so access to the RDRHL register affects the RDR register. Access to the RDRHL register is prohibited if 7-bit or 8-bit data length is selected.

After one frame of data is received, the received data is transferred from the RSR register to the RDRHL register, allowing the RSR register to receive more data.

The RSR and RDRHL registers have a double-buffered construction to enable continuous reception. The RDRHL register must be read only when a receive data full interrupt (SCIn_RXI) request is issued. An overrun error occurs when the next frame of data is received before the received data is read from the RDRHL register.

The CPU cannot write to the RDRHL register. Bits [15:9] are fixed to 0. These bits are read as 0. The write value should be 0.

34.2.4 Receive FIFO Data Register H, L, HL (FRDRH, FRDRL, FRDRHL)

Receive FIFO Data Register H (FRDRH)

Address(es): SCI0.FRDRH 4007 0010h, SCI1.FRDRH 4007 0030h, SCI2.FRDRH 4007 0050h, SCI3.FRDRH 4007 0070h, SCI4.FRDRH 4007 0090h, SCI5.FRDRH 4007 00B0h, SCI6.FRDRH 4007 00D0h, SCI7.FRDRH 4007 00F0h, SCI8.FRDRH 4007 0110h, SCI9.FRDRH 4007 0130h

Receive FIFO Data Register L (FRDRL)

Address(es): SCI0.FRDRL 4007 0011h, SCI1.FRDRL 4007 0031h, SCI2.FRDRL 4007 0051h, SCI3.FRDRL 4007 0071h, SCI4.FRDRL 4007 0091h, SCI5.FRDRL 4007 00B1h, SCI6.FRDRL 4007 00D1h, SCI7.FRDRL 4007 00F1h, SCI8.FRDRL 4007 0111h, SCI9.FRDRL 4007 0131h

Receive FIFO Data Register HL (FRDRHL)

Address(es): SCI0.FRDRHL 4007 0010h, SCI1.FRDRHL 4007 0030h, SCI2.FRDRHL 4007 0050h, SCI3.FRDRHL 4007 0070h, SCI4.FRDRHL 4007 0090h, SCI5.FRDRHL 4007 00B0h, SCI6.FRDRHL 4007 00D0h, SCI7.FRDRHL 4007 00F0h, SCI8.FRDRHL 4007 0110h, SCI9.FRDRHL 4007 0130h

	SCIn.FRDRHL															
	SCIn.FRDRH								SCIn.FRDRL							
	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	RDF	ORER	FER	PER	DR	MPB	RDAT[8:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b8 to b0	RDAT[8:0]	Serial Receive Data	Valid only in asynchronous mode, including multi-processor mode, and clock synchronous mode, and with FIFO selected. Stores the serial receive data.	R
b9	MPB	Multi-Processor Bit Flag	Stores the value of the multi-processor bit in the serial receive data (RDAT[8:0]): 0: Data transmission cycle 1: ID transmission cycle. Valid only in asynchronous mode with SMR.MP = 1, and with FIFO selected.	R

34.2.3 接收9位数据寄存器(RDRHL)

Address(es): SCI0.RDRHL 4007 0010h, SCI1.RDRHL 4007 0030h, SCI2.RDRHL 4007 0050h, SCI3.RDRHL 4007 0070h, SCI4.RDRHL 4007 0090h, SCI5.RDRHL 4007 00B0h, SCI6.RDRHL 4007 00D0h, SCI7.RDRHL 4007 00F0h, SCI8.RDRHL 4007 0110h, SCI9.RDRHL 4007 0130h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

RDRHL是一个16位寄存器，用于存储接收数据。选择异步模式和9位数据长度时，请使用RDRHL寄存器。

RDRHL的低8位是RDR的影子寄存器，因此对RDRHL寄存器的访问会影响RDR寄存器。
如果选择7位或8位数据长度，则禁止访问RDRHL寄存器。

接收到一帧数据后，将接收到的数据从RSR寄存器传送到RDRHL寄存器，让RSR寄存器接收更多数据。

RSR和RDRHL寄存器具有双缓冲结构以实现连续接收。仅当发出接收数据完整中断(SCIn_RXI)请求时，必须读取RDRHL寄存器。在从RDRHL寄存器读取接收到的数据之前接收到下一帧数据时，会发生溢出错误。

CPU无法写入RDRHL寄存器。位[15:9]固定为0。这些位被读取为0。写入值应为0。

34.2.4 接收FIFO数据寄存器H L HL(FRDRH FRDRL FRDRHL)

接收FIFO数据寄存器H(FRDRH)

Address(es): SCI0.FRDRH 4007 0010h, SCI1.FRDRH 4007 0030h, SCI2.FRDRH 4007 0050h, SCI3.FRDRH 4007 0070h, SCI4.FRDRH 4007 0090h, SCI5.FRDRH 4007 00B0h, SCI6.FRDRH 4007 00D0h, SCI7.FRDRH 4007 00F0h, SCI8.FRDRH 4007 0110h, SCI9.FRDRH 4007 0130h

接收FIFO数据寄存器L(FRRDL)

Address(es): SCI0.FRDRL 4007 0011h, SCI1.FRDRL 4007 0031h, SCI2.FRDRL 4007 0051h, SCI3.FRDRL 4007 0071h, SCI4.FRDRL 4007 0091h, SCI5.FRDRL 4007 00B1h, SCI6.FRDRL 4007 00D1h, SCI7.FRDRL 4007 00F1h, SCI8.FRDRL 4007 0111h, SCI9.FRDRL 4007 0131h

接收FIFO数据寄存器HL(FRDRHL)

Address(es): SCI0.FRDRHL 4007 0010h, SCI1.FRDRHL 4007 0030h, SCI2.FRDRHL 4007 0050h, SCI3.FRDRHL 4007 0070h, SCI4.FRDRHL 4007 0090h, SCI5.FRDRHL 4007 00B0h, SCI6.FRDRHL 4007 00D0h, SCI7.FRDRHL 4007 00F0h, SCI8.FRDRHL 4007 0110h, SCI9.FRDRHL 4007 0130h

	SCIn.FRDRHL															
	SCIn.FRDRH								SCIn.FRDRL							
	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	RDF	ORER	FER	PER	DR	MPB	RDAT[8:0]								
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b8 to b0	RDAT[8:0]	串行接收数据	仅在异步模式下有效，包括多处理器模式和时钟同步模式，并且选择了FIFO。存储串行接收数据。	R
b9	MPB	多处理器位标志	将多处理器位的值存储在串行接收数据（RDAT[8:0]）中：0：数据传输周期1：ID传输周期。仅在SMR.MP=1的异步模式下有效，并且 FIFO selected.	R

Bit	Symbol	Bit name	Description	R/W
b10	DR	Receive Data Ready Flag	This flag is the same as SSR_FIFO.DR: 0: Receiving is in progress, or no received data remains in the FRDRH and FRDRL registers after successfully completed reception 1: Next receive data is not received for a period after successfully completed reception.	R*1
b11	PER	Parity Error Flag	0: No parity error occurred in the first data of FRDRH and FRDRL 1: Parity error occurred in the first data of FRDRH and FRDRL.	R
b12	FER	Framing Error Flag	0: No framing error occurred in the first data of FRDRH and FRDRL 1: Framing error occurred in the first data of FRDRH and FRDRL.	R
b13	ORER	Overrun Error Flag	This flag is the same as SSR_FIFO.ORER: 0: No overrun error occurred 1: Overrun error occurred.	R*1
b14	RDF	Receive FIFO Data Full Flag	This flag is the same as SSR_FIFO.RDF: 0: The amount of receive data written in FRDRH and FRDRL is less than the specified receive triggering number 1: The amount of receive data written in FRDRH and FRDRL is equal to or greater than the specified receive triggering number.	R*1
b15	—	Reserved	This bit is read as 0.	R

Note 1. If this flag is read, it indicates the same value as that read from the SSR_FIFO register. Write 0 to the SSR_FIFO register to clear the flag.

FRDRHL is a 16-bit register that consists of the 8-bit FRDRH and FRDRL registers.

FRDRH and FRDRL constitute a 16-stage FIFO register that stores serial receive data and related status information readable by software. This register is only valid in asynchronous mode, including multi-processor mode, or clock synchronous mode.

The SCI completes reception of one frame of serial data by transferring the received data from the Receive Shift Register (RSR) into FRDRH and FRDRL for storage. Continuous reception is executed until 16 stages are stored. If data is read when there is no received data in FRDRH and FRDRL, the value is undefined. When FRDRH and FRDRL are full, subsequent serial receive data is lost. The CPU can read from the FRDRH and FRDRL registers but cannot write to them.

Reading 1 from the RDF, ORER, or DR flags of the FRDRH register is the same as reading from those bits in the SSR_FIFO register. When writing 0 to clear a flag in the SSR_FIFO register after reading the FRDRH register, write 0 only to the flag that is to be cleared and write 1 to the other flags.

When reading both the FRDRH and FRDRL registers, read in order from FRDRH to FRDRL. The FRDRHL register can be accessed in 16-bit units.

34.2.5 Transmit Data Register (TDR)

Address(es): SCI0.TDR 4007 0003h, SCI1.TDR 4007 0023h, SCI2.TDR 4007 0043h, SCI3.TDR 4007 0063h, SCI4.TDR 4007 0083h, SCI5.TDR 4007 00A3h, SCI6.TDR 4007 00C3h, SCI7.TDR 4007 00E3h, SCI8.TDR 4007 0103h, SCI9.TDR 4007 0123h

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1

TDR is an 8-bit register that stores transmit data.

When the SCI detects that the TSR register is empty, it transfers the transmit data written in the TDR register to the TSR register and starts transmission.

The double-buffered structure of the TDR and TSR registers enables continuous serial transmission. If the next transmit data is already written to TDR when one frame of data is transmitted, the SCI transfers the written data to the TSR

Bit	Symbol	位名称	Description	R/W
b10	DR	接收数据就绪标志	该标志与SSR_FIFO.DR相同：0：接收中，或接收成功后FRDRH和FRDRL寄存器中没有接收到的数据1：接收成功后一段时间内没有接收到下一个接收数据。	R*1
b11	PER	奇偶校验错误标志	0：FRRDH和FRDRL的第一个数据没有发生奇偶校验错误1：FRRDH和FRDRL的第一个数据发生奇偶校验错误。	R
b12	FER	成帧错误标志	0：FRRDH和FRDRL的第一个数据没有发生帧错误1：FRRDH和FRDRL的第一个数据发生了帧错误。	R
b13	ORER	溢出错误标志	该标志与SSR_FIFO.ORER相同：0：未发生溢出错误1：发生溢出错误。	R*1
b14	RDF	接收FIFO数据满标志	该标志与SSR_FIFO.RDF相同：0：写入FRDRH和FRDRL的接收数据量小于指定的接收触发数1：写入FRDRH和FRDRL的接收数据量等于或大于指定的接收数据量接收触发号码。	R*1
b15	—	Reserved	该位读为0。	R

Note 1. 如果读取该标志，则表示与从SSR_FIFO寄存器读取的值相同。将0写入SSR_FIFO寄存器以清除标志。

FRDRHL是一个16位寄存器，由8位FRDRH和FRDRL寄存器组成。

FRDRH和FRDRL构成一个16级FIFO寄存器，用于存储串行接收数据和软件可读的相关状态信息。该寄存器仅在异步模式下有效，包括多处理器模式或时钟同步模式。

SCI通过将接收到的数据从接收移位寄存器（RSR）传送到FRDRH和FRDRL中进行存储，从而完成一帧串行数据的接收。执行连续接收，直到存储16个阶段。如果在FRDRH和FRDRL中没有接收到数据时读取数据，则该值未定义。当FRDRH和FRDRL已满时，后续的串行接收数据会丢失。CPU可以读取FRDRH和FRDRL寄存器，但不能写入它们。

从FRDRH寄存器的RDF、ORER或DR标志读取1与从SSR_FIFO寄存器。在读取FRDRH寄存器后写入0以清除SSR_FIFO寄存器中的标志时，仅将0写入要清除的标志，将1写入其他标志。

读取FRDRH和FRDRL寄存器时，按从FRDRH到FRDRL的顺序读取。FRDRHL寄存器可以以16位为单位进行访问。

34.2.5 发送数据寄存器(TDR)

Address(es): SCI0.TDR 4007 0003h, SCI1.TDR 4007 0023h, SCI2.TDR 4007 0043h, SCI3.TDR 4007 0063h, SCI4.TDR 4007 0083h, SCI5.TDR 4007 00A3h, SCI6.TDR 4007 00C3h, SCI7.TDR 4007 00E3h, SCI8.TDR 4007 0103h, SCI9.TDR 4007 0123h

	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	1	1	1	1	1	1	1	1

TDR是一个8位寄存器，用于存储发送数据。

当SCI检测到TSR寄存器为空时，将写入TDR寄存器的发送数据传送到TSR寄存器并开始发送。

TDR和TSR寄存器的双缓冲结构可实现连续串行传输。如果在发送一帧数据时，下一个发送数据已经写入TDR，则SCI将写入的数据传输到TSR

register to continue transmission.

The CPU can read from or write to TDR at any time. Only write transmit data to TDR once after each instance of the transmit data empty interrupt (SCIn_TXI).

34.2.6 Transmit 9-Bit Data Register (TDRHL)

Address(es): SCI0.TDRHL 4007 000Eh, SCI1.TDRHL 4007 002Eh, SCI2.TDRHL 4007 004Eh, SCI3.TDRHL 4007 006Eh, SCI4.TDRHL 4007 008Eh, SCI5.TDRHL 4007 00AEh, SCI6.TDRHL 4007 00CEh, SCI7.TDRHL 4007 00EEh, SCI8.TDRHL 4007 010Eh, SCI9.TDRHL 4007 012Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

TDRHL is a 16-bit register that stores transmit data. Use the TDRHL register when asynchronous mode and 9-bit data length are selected.

The lower 8 bits of TDRHL are a shadow register of TDR, so access to TDRHL affects the TDR register. Access to the TDRHL register is prohibited if 7-bit or 8-bit data length is selected.

When empty space is detected in the TSR register, the transmit data stored in the TDRHL register is transferred to the TSR register and transmission is started.

The TSR and TDRHL registers have a double-buffered structure to support continuous transmission. When the next data to be transmitted is stored in TDRHL after one frame of data is transmitted, the transmitting operation is continued by transferring the data from the TDRHL register to the TSR register.

The CPU can read from and write to the TDRHL register. Bits [15:9] in the TDRHL register are fixed to 1. These bits are read as 1. The write value should be 1.

Write transmit data to the TDRHL register only once when a transmit data empty interrupt (SCIn_TXI) request is issued.

注册以继续传输。

CPU可以随时读取或写入TDR。每次发送数据空中断(SCIn_TXI)后，仅将发送数据写入TDR一次。

34.2.6 发送9位数据寄存器(TDRHL)

Address(es): SCI0.TDRHL 4007 000Eh, SCI1.TDRHL 4007 002Eh, SCI2.TDRHL 4007 004Eh, SCI3.TDRHL 4007 006Eh, SCI4.TDRHL 4007 008Eh, SCI5.TDRHL 4007 00AEh, SCI6.TDRHL 4007 00CEh, SCI7.TDRHL 4007 00EEh, SCI8.TDRHL 4007 010Eh, SCI9.TDRHL 4007 012Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

TDRHL是一个16位寄存器，用于存储发送数据。选择异步模式和9位数据长度时，请使用TDRHL寄存器。

TDRHL的低8位是TDR的影子寄存器，因此访问TDRHL会影响TDR寄存器。访问
如果选择7位或8位数据长度，则禁止TDRHL寄存器。

当在TSR寄存器中检测到空空间时，存储在TDRHL寄存器中的发送数据被传送到
TSR寄存器和传输开始。

TSR和TDRHL寄存器具有双缓冲结构以支持连续传输。当下一个要发送的数据在发送一帧数据后存储在TDRHL中时，通过将数据从TDRHL寄存器传送到TSR寄存器来继续发送操作。

CPU可以读取和写入TDRHL寄存器。TDRHL寄存器中的位[15:9]固定为1。这些位被读取为1。写入值应为1。

当发出发送数据空中断(SCIn_TXI)请求时，仅将发送数据写入TDRHL寄存器一次。

34.2.7 Transmit FIFO Data Register H, L, HL (FTDRH, FTDRL, FTDRHL)

Transmit FIFO Data Register H (FTDRH)

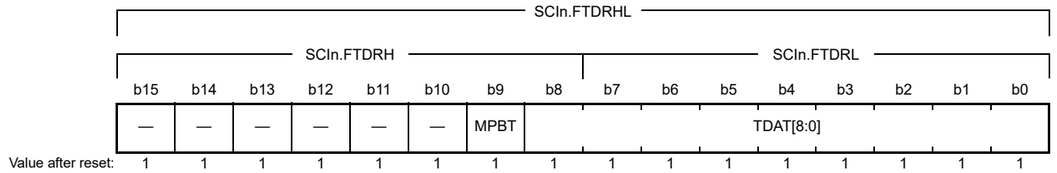
Address(es): SCI0.FTDRH 4007 000Eh, SCI1.FTDRH 4007 002Eh, SCI2.FTDRH 4007 004Eh, SCI3.FTDRH 4007 006Eh, SCI4.FTDRH 4007 008Eh, SCI5.FTDRH 4007 00AEh, SCI6.FTDRH 4007 00CEh, SCI7.FTDRH 4007 00EEh, SCI8.FTDRH 4007 010Eh, SCI9.FTDRH 4007 012Eh

Transmit FIFO Data Register L (FTDRL)

Address(es): SCI0.FTDRL 4007 000Fh, SCI1.FTDRL 4007 002Fh, SCI2.FTDRL 4007 004Fh, SCI3.FTDRL 4007 006Fh, SCI4.FTDRL 4007 008Fh, SCI5.FTDRL 4007 00AFh, SCI6.FTDRL 4007 00CFh, SCI7.FTDRL 4007 00EFh, SCI8.FTDRL 4007 010Fh, SCI9.FTDRL 4007 012Fh

Transmit FIFO Data Register HL (FTDRHL)

Address(es): SCI0.FTDRHL 4007 000Eh, SCI1.FTDRHL 4007 002Eh, SCI2.FTDRHL 4007 004Eh, SCI3.FTDRHL 4007 006Eh, SCI4.FTDRHL 4007 008Eh, SCI5.FTDRHL 4007 00AEh, SCI6.FTDRHL 4007 00CEh, SCI7.FTDRHL 4007 00EEh, SCI8.FTDRHL 4007 010Eh, SCI9.FTDRHL 4007 012Eh



Bit	Symbol	Bit name	Description	R/W
b8 to b0	TDAT[8:0]	Serial Transmit Data	Valid only in asynchronous mode, including multi-processor mode, and clock synchronous mode, and with FIFO selected. Specifies the serial transmit data.	W
b9	MPBT	Multi-Processor Transfer Bit Flag	Specifies the multi-processor bit in the transmission frame: 0: Data transmission cycle 1: ID transmission cycle. Valid only in asynchronous mode and SMR.MP = 1, and with FIFO selected.	W
b15 to b10	—	Reserved	The write value should be 1.	W

FTDRHL is a 16-bit register that consists of the 8-bit FTDRH and FTDRL registers.

FTDRH and FTDRL constitute a 16-stage FIFO register that stores data for serial transmission and a multi-processor transfer bit. This register is only valid in asynchronous mode, including multi-processor mode, or clock synchronous mode.

When the SCI detects that the Transmit Shift Register (TSR) is empty, it transfers data written in the FTDRH and FTDRL registers to the TSR register and starts serial transmission. Continuous serial transmission is executed until no transmit data is left in FTDRH and FTDRL. When FTDRHL is full of transmit data, no more data can be written. If writing new data is attempted, the data is ignored. The CPU can write to the FTDRH and FTDRL registers but cannot read them.

When writing to both the FTDRH and FTDRL registers, write in order from FTDRH to FTDRL.

MPBT flag (Multi-Processor Transfer Bit Flag)

The MPBT flag specifies the value of the multi-processor bit of the transmit frame. When FCR.FM = 1, SSR.MPBT is invalid.

34.2.8 Transmit Shift Register (TSR)

TSR is a shift register that transmits serial data. To perform serial data transmission, the SCI first automatically transfers transmit data from TDR, TDRHL, or transmit FIFO to the TSR register, and then sends the data to the TXDn pin. The CPU cannot directly access the TSR register.

34.2.7 发送FIFO数据寄存器H L HL(FTDRH FTDRL FTDRHL)

发送FIFO数据寄存器H(FTDRH)

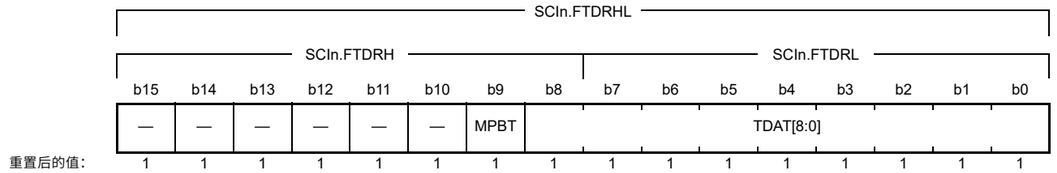
Address(es): SCI0.FTDRH 4007 000Eh, SCI1.FTDRH 4007 002Eh, SCI2.FTDRH 4007 004Eh, SCI3.FTDRH 4007 006Eh, SCI4.FTDRH 4007 008Eh, SCI5.FTDRH 4007 00AEh, SCI6.FTDRH 4007 00CEh, SCI7.FTDRH 4007 00EEh, SCI8.FTDRH 4007 010Eh, SCI9.FTDRH 4007 012Eh

发送FIFO数据寄存器L(FTDRL)

Address(es): SCI0.FTDRL 4007 000Fh, SCI1.FTDRL 4007 002Fh, SCI2.FTDRL 4007 004Fh, SCI3.FTDRL 4007 006Fh, SCI4.FTDRL 4007 008Fh, SCI5.FTDRL 4007 00AFh, SCI6.FTDRL 4007 00CFh, SCI7.FTDRL 4007 00EFh, SCI8.FTDRL 4007 010Fh, SCI9.FTDRL 4007 012Fh

发送FIFO数据寄存器HL(FTDRHL)

Address(es): SCI0.FTDRHL 4007 000Eh, SCI1.FTDRHL 4007 002Eh, SCI2.FTDRHL 4007 004Eh, SCI3.FTDRHL 4007 006Eh, SCI4.FTDRHL 4007 008Eh, SCI5.FTDRHL 4007 00AEh, SCI6.FTDRHL 4007 00CEh, SCI7.FTDRHL 4007 00EEh, SCI8.FTDRHL 4007 010Eh, SCI9.FTDRHL 4007 012Eh



Bit	Symbol	位名称	Description	R/W
b8 to b0	TDAT[8:0]	串行传输数据	仅在异步模式下有效，包括多处理器模式和时钟同步模式，并且选择了FIFO。指定串行传输数据。	W
b9	MPBT	多处理器传输位标志	指定传输帧中的多处理器位：0：数据传输周期1：ID传输周期。仅在异步模式和SMR.MP=1下有效，并且与 FIFO selected.	W
b15 to b10	—	Reserved	写入值应为1。	W

FTDRHL是一个16位寄存器，由8位FTDRH和FTDRL寄存器组成。

FTDRH和FTDRL构成一个16级FIFO寄存器，用于存储串行传输的数据和一个多处理器传输位。该寄存器仅在异步模式下有效，包括多处理器模式或时钟同步模式。

当SCI检测到发送移位寄存器(TSR)为空时，它会传输写入FTDRH中的数据并FTDRL注册到TSR寄存器并开始串行传输。执行连续串行传输，直到在FTDRH和FTDRL中没有剩余传输数据。当FTDRHL充满传输数据时，不能再写入数据。如果尝试写入新数据，则忽略该数据。CPU可以写入FTDRH和FTDRL寄存器，但不能读取它们。

当同时写入FTDRH和FTDRL寄存器时，按照从FTDRH到FTDRL的顺序写入。

MPBT标志（多处理器传输位标志）

MPBT标志指定发送帧的多处理器位的值。FCR.FM=1时，SSR.MPBT无效。

34.2.8 发送移位寄存器(TSR)

TSR是传送串行数据的移位寄存器。进行串行数据传输时，SCI首先自动将发送数据从TDR、TDRHL或发送FIFO传输到TSR寄存器，然后将数据发送到TXDn引脚。CPU不能直接访问TSR寄存器。

34.2.9 Serial Mode Register (SMR) for Non-Smart Card Interface Mode (SCMR.SMIF = 0)

Address(es): SCI0.SMR 4007 0000h, SCI1.SMR 4007 0020h, SCI2.SMR 4007 0040h, SCI3.SMR 4007 0060h, SCI4.SMR 4007 0080h, SCI5.SMR 4007 00A0h, SCI6.SMR 4007 00C0h, SCI7.SMR 4007 00E0h, SCI8.SMR 4007 0100h, SCI9.SMR 4007 0120h

	b7	b6	b5	b4	b3	b2	b1	b0
	CM	CHR	PE	PM	STOP	MP	CKS[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	CKS[1:0]	Clock Select	b1 b0 0 0: PCLKA clock (n = 0)*1 0 1: PCLKA/4 clock (n = 1)*1 1 0: PCLKA/16 clock (n = 2)*1 1 1: PCLKA/64 clock (n = 3).*1	R/W*4
b2	MP	Multi-Processor Mode	Valid only in asynchronous mode: 0: Disable multi-processor communications function 1: Enable multi-processor communications function.	R/W*4
b3	STOP	Stop Bit Length	Valid only in asynchronous mode: 0: 1 stop bit 1: 2 stop bits.	R/W*4
b4	PM	Parity Mode	Valid only when the PE bit is 1: 0: Even parity 1: Odd parity.	R/W*4
b5	PE	Parity Enable	Valid only in asynchronous mode: • When transmitting: 0: Do not add parity bit 1: Add parity bit. • When receiving: 0: Do not check parity bit 1: Check parity bit.	R/W*4
b6	CHR	Character Length	Selects the transmit/receive character length in combination with the SCMR.CHR1 bit: CHR1 CHR 0 0: Transmit/receive in 9-bit data length 0 1: Transmit/receive in 9-bit data length 1 0: Transmit/receive in 8-bit data length (initial value) 1 1: Transmit/receive in 7-bit data length.*3 Valid only in asynchronous mode.*2	R/W*4
b7	CM	Communication Mode	0: Asynchronous mode or simple IIC mode 1: Clock synchronous mode or simple SPI mode.	R/W*4

Note 1. n is the decimal notation of the value of n in the BRR register. See section 34.2.17, Bit Rate Register (BRR).
Note 2. In any mode other than asynchronous mode, this bit setting is invalid and a fixed data length of 8 bits is used.
Note 3. LSB-first is fixed and the MSB (bit [7]) in the TDR register is not transmitted in transmit mode.
Note 4. Writable only when SCR.TE = 0 and SCR.RE = 0 (both serial transmission and reception are disabled).

The SMR register sets the communication format and clock source for the on-chip baud rate generator.

CKS[1:0] bits (Clock Select)

The CKS[1:0] bits select the clock source for the on-chip baud rate generator. For the relationship between the settings of these bits and the baud rate, see section 34.2.17, Bit Rate Register (BRR).

MP bit (Multi-Processor Mode)

The MP bit disables or enables the multi-processor communications function. The PE and PM bit settings are invalid in multi-processor mode.

34.2.9 非智能卡接口模式的串行模式寄存器(SMR)(SCMR.SMIF=0)

Address(es): SCI0.SMR 4007 0000h, SCI1.SMR 4007 0020h, SCI2.SMR 4007 0040h, SCI3.SMR 4007 0060h, SCI4.SMR 4007 0080h, SCI5.SMR 4007 00A0h, SCI6.SMR 4007 00C0h, SCI7.SMR 4007 00E0h, SCI8.SMR 4007 0100h, SCI9.SMR 4007 0120h

	b7	b6	b5	b4	b3	b2	b1	b0
	CM	CHR	PE	PM	STOP	MP	CKS[1:0]	
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b1, b0	CKS[1:0]	时钟选择	b1 b0 0 0: PCLKA clock (n = 0)*1 0 1: PCLKA/4 clock (n = 1)*1 1 0: PCLKA/16 clock (n = 2)*1 1 1: PCLKA/64 clock (n = 3).*1	R/W*4
b2	MP	Multi-Processor Mode	仅在异步模式下有效：0：禁用多处理器通讯功能1：启用多处理器通讯功能。	R/W*4
b3	STOP	停止位长度	仅在异步模式下有效：0：1个停止位1：2个停止位。	R/W*4
b4	PM	奇偶校验模式	仅在PE位为1时有效：0：偶校验1：奇校验。	R/W*4
b5	PE	奇偶校验使能	仅在异步模式下有效：　发送时：0：不添加奇偶校验位1：添加奇偶校验位。　接收时：0：不校验校验位1：校验校验位。	R/W*4
b6	CHR	字符长度	结合SCMR.CHR1位选择发送接收字符长度：CHR1CHR00：发送接收9位数据长度01：发送接收9位数据长度10：发送接收8位数据长度（初始值）11：发送接收7位数据长度。*3仅在异步模式下有效。*2	R/W*4
b7	CM	通讯方式	0：异步模式或简单IIC模式1：时钟同步模式或简单SPI模式。	R/W*4

Note 1. n是BRR寄存器中n值的十进制表示法。请参阅第34.2.17节，比特率寄存器(BRR)。
Note 2. 在异步模式以外的任何模式下，该位设置无效，使用固定的8位数据长度。
Note 3. LSB-first是固定的，并且TDR寄存器中的MSB（位[7]）在发送模式下不发送。
Note 4. 仅当SCR.TE=0和SCR.RE=0时可写（串行发送和接收均禁用）。

SMR寄存器设置片内波特率发生器的通信格式和时钟源。

CKS[1:0]位（时钟选择）

CKS[1:0]位选择片内波特率发生器的时钟源。有关这些位的设置与波特率之间的关系，请参见第34.2.17节，比特率寄存器(BRR)。

MP位（多处理器模式）

MP位禁用或启用多处理器通信功能。PE和PM位设置在多处理器模式下无效。

STOP bit (Stop Bit Length)

The STOP bit selects the stop bit length in transmission.

In reception, only the first stop bit is checked regardless of this bit setting. If the second stop bit is 0, it is treated as the start bit of the next transmit frame.

PM bit (Parity Mode)

The PM bit selects the parity mode (even or odd) for transmission and reception. The PM bit setting is invalid in multi-processor mode.

PE bit (Parity Enable)

When the PE bit is set to 1, the parity bit is added to transmit data, and the parity bit is checked in reception. Regardless of the PE bit setting, the parity bit is not added or checked in multi-processor format.

CHR bit (Character Length)

The CHR bit selects the data length for transmission and reception in combination with the SCMR.CHR1 bit. In modes other than asynchronous, a fixed data length of 8 bits is used.

CM bit (Communication Mode)

The CM bit selects the communication mode:

- Asynchronous mode or simple IIC mode
- Clock synchronous mode or simple SPI mode.

34.2.10 Serial Mode Register for Smart Card Interface Mode (SMR_SMCI) (SCMR.SMIF = 1)

Address(es): SCI0.SMR_SMCI 4007 0000h, SCI1.SMR_SMCI 4007 0020h, SCI2.SMR_SMCI 4007 0040h, SCI3.SMR_SMCI 4007 0060h, SCI4.SMR_SMCI 4007 0080h, SCI5.SMR_SMCI 4007 00A0h, SCI6.SMR_SMCI 4007 00C0h, SCI7.SMR_SMCI 4007 00E0h, SCI8.SMR_SMCI 4007 0100h, SCI9.SMR_SMCI 4007 0120h

	b7	b6	b5	b4	b3	b2	b1	b0
	GM	BLK	PE	PM	BCP[1:0]		CKS[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	CKS[1:0]	Clock Select	b1 b0 0 0: PCLKA clock (n = 0)*1 0 1: PCLKA/4 clock (n = 1)*1 1 0: PCLKA/16 clock (n = 2)*1 1 1: PCLKA/64 clock (n = 3).*1	R/W*2
b3, b2	BCP[1:0]	Base Clock Pulse	Selects the number of base clock cycles in combination with the SCMR.BCP2 bit. Table 34.3 lists the combinations of the SCMR.BCP2 and SMR.BCP[1:0] bits.	R/W*2
b4	PM	Parity Mode	Valid only when the PE bit is 1: 0: Even parity 1: Odd parity.	R/W*2
b5	PE	Parity Enable	When this bit is set to 1, a parity bit is added to transmit data, and the parity of received data is checked. Set this bit to 1 in smart card interface mode.	R/W*2
b6	BLK	Block Transfer Mode	0: Non-block transfer mode operation 1: Block transfer mode operation.	R/W*2
b7	GM	GSM Mode	0: Non-GSM mode operation 1: GSM mode operation.	R/W*2

Note 1. n is the decimal notation of the value of n in the BRR register. See section 34.2.17, Bit Rate Register (BRR).
Note 2. Writable only when SCR_SMCI.TE = 0 and SCR_SMCI.RE = 0 (both serial transmission and reception are disabled).

停止位（停止位长度）

STOP位选择传输中的停止位长度。

在接收中，无论该位设置如何，都只检查第一个停止位。如果第二个停止位为0，则将其视为下一个发送帧的起始位。

PM位（奇偶校验模式）

PM位选择发送和接收的奇偶校验模式（偶数或奇数）。PM位设置在多处理器模式下无效。

PE位（奇偶校验使能）

当PE位设置为1时，发送数据时添加奇偶校验位，接收时检查奇偶校验位。无论PE位设置如何，在多处理器格式中都不会添加或检查奇偶校验位。

CHR位（字符长度）

CHR位与SCMR.CHR1位一起选择发送和接收的数据长度。在非异步模式下，使用8位的固定数据长度。

CM位（通信模式）

CM位选择通信模式：

- 异步模式或简单IIC模式
- 时钟同步模式或简单的SPI模式。

34.2.10 智能卡接口模式的串行模式寄存器(SMR_SMCI)(SCMR.SMIF=1)

Address(es): SCI0.SMR_SMCI 4007 0000h, SCI1.SMR_SMCI 4007 0020h, SCI2.SMR_SMCI 4007 0040h, SCI3.SMR_SMCI 4007 0060h, SCI4.SMR_SMCI 4007 0080h, SCI5.SMR_SMCI 4007 00A0h, SCI6.SMR_SMCI 4007 00C0h, SCI7.SMR_SMCI 4007 00E0h, SCI8.SMR_SMCI 4007 0100h, SCI9.SMR_SMCI 4007 0120h

	b7	b6	b5	b4	b3	b2	b1	b0
	GM	BLK	PE	PM	BCP[1:0]		CKS[1:0]	
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b1, b0	CKS[1:0]	时钟选择	b1 b0 0 0: PCLKA clock (n = 0)*1 0 1: PCLKA/4 clock (n = 1)*1 1 0: PCLKA/16 clock (n = 2)*1 1 1: PCLKA/64 clock (n = 3).*1	R/W*2
b3, b2	BCP[1:0]	基本时钟脉冲	结合SCMR.BCP2位选择基本时钟周期数。表34.3列出了SCMR.BCP2和SMR.BCP[1:0]位的组合。	R/W*2
b4	PM	奇偶校验模式	仅在PE位为1时有效：0：偶校验1：奇校验。	R/W*2
b5	PE	奇偶校验使能	当该位设置为1时，发送数据时添加一个奇偶校验位，并检查接收数据的奇偶校验。在智能卡接口模式下将此位设置为1。	R/W*2
b6	BLK	块传输模式	0：非块传输模式操作1：块传输模式操作。	R/W*2
b7	GM	GSM Mode	0：非GSM模式操作1：GSM模式操作。	R/W*2

Note 1. n是BRR寄存器中n值的十进制表示法。请参阅第34.2.17节，比特率寄存器(BRR)。
Note 2. 仅当SCR_SMCI.TE=0且SCR_SMCI.RE=0时可写（串行传输和接收均禁用）。

The SMR_SMCI register sets the communication format and clock source for the on-chip baud rate generator.

CKS[1:0] bit (Clock Select)

The CKS[1:0] bits select the clock source for the on-chip baud rate generator. For the relationship between the settings of these bits and the baud rate, see section 34.2.17, Bit Rate Register (BRR).

BCP[1:0] bits (Base Clock Pulse)

The BCP[1:0] bits select the number of base clock cycles in a 1-bit data transfer time in smart card interface mode. Set these bits in combination with the SCMR.BCP2 bit.

For details, see section 34.6.4, Receive Data Sampling Timing and Reception Margin.

Table 34.3 Combinations of SCMR.BCP2 and SMR_SMCI.BCP[1:0] bits

SCMR.BCP2 bit	SMR_SMCI.BCP[1:0] bits	Number of base clock cycles for 1-bit transfer period
0	00	93 clock cycles (S = 93)*1
0	01	128 clock cycles (S = 128)*1
0	10	186 clock cycles (S = 186)*1
0	11	512 clock cycles (S = 512)*1
1	00	32 clock cycles (S = 32)*1 (initial value)
1	01	64 clock cycles (S = 64)*1
1	10	372 clock cycles (S = 372)*1
1	11	256 clock cycles (S = 256)*1

Note 1. See section 34.2.17, Bit Rate Register (BRR).

PM bit (Parity Mode)

The PM bit selects the parity mode for transmission and reception (even or odd). For details on the usage of this bit in smart card interface mode, see section 34.6.2, Data Format (Except in Block Transfer Mode).

PE bit (Parity Enable)

Set the PE bit to 1. The parity bit is added to transmit data before transmission, and the parity bit is checked in reception.

BLK bit (Block Transfer Mode)

Setting the BLK bit to 1 enables block transfer mode operation. For details, see section 34.6.3, Block Transfer Mode.

GM bit (GSM Mode)

Setting the GM bit to 1 enables GSM mode operation. In GSM mode, the SSR_SMCI.TEND flag set timing is moved forward to 11.0 ETUs (elementary time unit = 1-bit transfer time) from the start bit, and clock output control is added. For details, see section 34.6.6, Serial Data Transmission (Except in Block Transfer Mode) and section 34.6.8, Clock Output Control.

SMR_SMCI寄存器设置片内波特率发生器的通信格式和时钟源。

CKS[1:0]位（时钟选择）

CKS[1:0]位选择片内波特率发生器的时钟源。有关这些位的设置与波特率之间的关系，请参见第34.2.17节，比特率寄存器(BRR)。

BCP[1:0]位（基本时钟脉冲）

BCP[1:0]位选择智能卡接口模式下1位数据传输时间内的基本时钟周期数。将这些位与SCMR.BCP2位一起设置。

有关详细信息，请参阅第34.6.4节，接收数据采样时序和接收余量。

Table 34.3 SCMR.BCP2和SMR_SMCI.BCP[1:0]位的组合

SCMR.BCP2 bit	SMR_SMCI.BCP[1:0] bits	1位传输周期的基本时钟周期数
0	00	93个时钟周期(S=93)*1
0	01	128个时钟周期(S=128)*1
0	10	186个时钟周期(S=186)*1
0	11	512个时钟周期(S=512)*1
1	00	32个时钟周期(S=32)*1（初始值）
1	01	64个时钟周期(S=64)*1
1	10	372个时钟周期(S=372)*1
1	11	256个时钟周期(S=256)*1

Note 1. 请参阅第34.2.17节，比特率寄存器(BRR)。

PM位（奇偶校验模式）

PM位选择发送和接收的奇偶校验模式（偶数或奇数）。有关该位在智能卡接口模式下的使用详情，请参见第34.6.2节，数据格式（块传输模式除外）。

PE位（奇偶校验使能）

将PE位设置为1。发送数据前添加奇偶校验位，接收时校验奇偶校验位。

BLK位（块传输模式）

将BLK位设置为1可启用块传输模式操作。有关详细信息，请参阅第34.6.3节，块传输模式。

GM位（GSM模式）

将GM位设置为1启用GSM模式操作。在GSM模式下，SSR_SMCI.TEND标志设置时序从起始位前移到11.0ETU（基本时间单位=1位传输时间），并添加了时钟输出控制。有关详细信息，请参见第34.6.6节，串行数据传输（块传输模式除外）和第34.6.8节，时钟
输出控制。

34.2.11 Serial Control Register (SCR) for Non-Smart Card Interface Mode (SCMR.SMIF = 0)

Address(es): SCI0.SCR 4007 0002h, SCI1.SCR 4007 0022h, SCI2.SCR 4007 0042h, SCI3.SCR 4007 0062h, SCI4.SCR 4007 0082h, SCI5.SCR 4007 00A2h, SCI6.SCR 4007 00C2h, SCI7.SCR 4007 00E2h, SCI8.SCR 4007 0102h, SCI9.SCR 4007 0122h

	b7	b6	b5	b4	b3	b2	b1	b0
	TIE	RIE	TE	RE	MPIE	TEIE	CKE[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	CKE[1:0]	Clock Enable	• Asynchronous mode: b1 b0 0 0: On-chip baud rate generator The SCKn pin is available for use as an I/O port based on the I/O port settings 0 1: On-chip baud rate generator A clock with the same frequency as the bit rate is output from the SCKn pin 1 x: External clock Input a clock with a frequency 16 times the bit rate from the SCKn pin when the SEMR.ABCS bit is 0. Input a clock signal with a frequency eight times the bit rate when the SEMR.ABCS bit is 1. • Clock synchronous mode: b1 b0 0 x: Internal clock The SCKn pin functions as the clock output pin 1 x: External clock. The SCKn pin functions as the clock input pin.	R/W*1
b2	TEIE	Transmit End Interrupt Enable	0: Disable SCIn_TEI interrupt requests 1: Enable SCIn_TEI interrupt requests.	R/W
b3	MPIE	Multi-Processor Interrupt Enable	Valid in asynchronous mode when SMR.MP = 1: 0: Non-multi processor reception 1: When data with the multi-processor bit set to 0 is received, the data is not read, and setting the status flags RDRF, ORER, and FER in SSR to 1 is disabled. When data with the multi-processor bit set to 1 is received, the MPIE bit is automatically cleared to 0, and non-multi processor reception is resumed.	R/W*3
b4	RE	Receive Enable	0: Disable serial reception 1: Enable serial reception.	R/W*2
b5	TE	Transmit Enable	0: Disable serial transmission 1: Enable serial transmission.	R/W*2
b6	RIE	Receive Interrupt Enable	0: Disable SCIn_RXI and SCIn_ERI interrupt requests 1: Enable SCIn_RXI and SCIn_ERI interrupt requests.	R/W
b7	TIE	Transmit Interrupt Enable	0: Disable SCIn_TXI interrupt requests 1: Enable SCIn_TXI interrupt requests.	R/W

x: Don’t care

Note 1. Writable only when TE = 0 and RE = 0.
Note 2. 1 can be written only when TE = 0 and RE = 0, when the SMR.CM bit is 1. After setting TE or RE to 1, only 0 can be written to TE and RE. When the SMR.CM bit is 0 and the SIMR1.IICM bit is 0, writing is enabled under any condition.
Note 3. When writing a new value to a bit other than the MPIE bit of this register in multi-processor mode (SMR.MP bit = 1), write 0 to the MPIE bit using the store instruction to avoid accidentally setting the MPIE bit to 1 by a read-modify-write operation when using a bit manipulation instruction.

The SCR register controls operation and clock source selection for transmission and reception.

34.2.11 非智能卡接口模式的串行控制寄存器(SCR)(SCMR.SMIF=0)

Address(es): SCI0.SCR 4007 0002h, SCI1.SCR 4007 0022h, SCI2.SCR 4007 0042h, SCI3.SCR 4007 0062h, SCI4.SCR 4007 0082h, SCI5.SCR 4007 00A2h, SCI6.SCR 4007 00C2h, SCI7.SCR 4007 00E2h, SCI8.SCR 4007 0102h, SCI9.SCR 4007 0122h

	b7	b6	b5	b4	b3	b2	b1	b0
	TIE	RIE	TE	RE	MPIE	TEIE	CKE[1:0]	
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b1, b0	CKE[1:0]	时钟使能	异步模式：b1b000：片上波特率发生器 SCKn引脚可根据IO端口设置用作IO端口01：片上波特率发生器 从SCKn引脚输出与比特率相同频率的时钟1x：外部时钟 当SEMR.ABCS位为0时，从SCKn引脚输入频率为16倍比特率的时钟。当SEMR.ABCS位为1时，输入频率为8倍比特率的时钟信号。 时钟同步模式：b1b00x：内部时钟 SCKn引脚用作时钟输出引脚1x：外部时钟。 SCKn引脚用作时钟输入引脚。	R/W*1
b2	TEIE	发送结束中断使能	0：禁用SCIn_TEI中断请求1：启用SCIn_TEI中断请求。	R/W
b3	MPIE	多处理器中断使能	SMR.MP=1时在异步模式下有效：0：非多处理器接收1：当多处理器位设置为0的数据是 接收时，不读取数据，并且将SSR中的状态标志RDRF、ORER和FER设置为1被禁用。当接收到多处理器位设置为1的数据时，MPIE位自动清零，恢复非多处理器接收。	R/W*3
b4	RE	接收启用	0：禁用串行接收1：启用串行接收。	R/W*2
b5	TE	发送启用	0：禁用串行传输1：启用串行传输。	R/W*2
b6	RIE	接收中断使能	0：禁用SCIn_RXI和SCIn_ERI中断请求1：启用SCIn_RXI和SCIn_ERI中断请求。	R/W
b7	TIE	发送中断使能	0：禁用SCIn_TXI中断请求1：启用SCIn_TXI中断请求。	R/W

x: Don’t care

Note 1. 仅当TE=0且RE=0时可写。
Note 2. 只有当TE=0且RE=0时，SMR.CM位为1时才能写入1。将TE或RE设置为1后，TE和RE只能写入0。当SMR.CM位为0且SIMR1.IICM位为0时，在任何情况下都可以写入。
Note 3. 在多处理器模式下（SMR.MP位=1）向该寄存器的MPIE位以外的位写入新值时，使用存储指令将0写入MPIE位，以避免意外将MPIE位设置为1使用位操作指令时的读-修改-写操作。

SCR寄存器控制发送和接收的操作和时钟源选择。

CKE[1:0] bits (Clock Enable)

The CKE[1:0] bits select the clock source and the SCKn pin function.

TEIE bit (Transmit End Interrupt Enable)

The TEIE bit enables or disables SCIn_TEI interrupt requests. Set TEIE to 0 to disable an SCIn_TEI interrupt request.

In simple IIC mode, SCIn_TEI is allocated to the interrupt on completion of issuing a start, restart, or stop condition (STIn). In this case, the TEIE bit can be used to enable or disable the STI.

MPIE bit (Multi-Processor Interrupt Enable)

When the MPIE bit is set to 1 and data with the multi-processor bit set to 0 is received, the data is not read and setting the status flags RDRF, ORER, and FER in SSR/SSR_FIFO to 1 is disabled. When data with the multi-processor bit set to 1 is received, the MPIE bit is automatically cleared to 0, and non-multi processor reception resumes. For details, see section 34.4, Multi-Processor Communication Function.

When the MPB bit in the SSR register is 0, the receive data is not transferred from the RSR register to the RDR register, a receive error is not detected, and setting the flags ORER and FER to 1 is disabled.

When the MPB bit is set to 1, the MPIE bit is automatically cleared to 0, SCIn_RXI and SCIn_ERI interrupt requests are enabled (if the RIE bit in SCR is set to 1), and setting of the ORER and FER flags to 1 is enabled.

Set MPIE to 0 if the multi-processor communications function is not used.

RE bit (Receive Enable)

The RE bit enables or disables serial reception. When the RE bit is set to 1, serial reception starts by detecting the start bit in asynchronous mode or the synchronous clock input in clock synchronous mode. Set the reception format in the SMR register before setting the RE bit to 1.

In non-FIFO operation, when reception is halted by setting the RE bit to 0, the RDRF, ORER, FER, and PER flags in the SSR register are not affected, and the previous values are retained.

When FIFO operation is selected and reception is halted by setting the RE bit to 0, the RDF, ORER, FER, PER, and DR flags in SSR_FIFO are not affected and the previous values are retained.

TE bit (Transmit Enable)

The TE bit enables or disables serial transmission.

When the TE bit is set to 1, serial transmission is started by writing transmit data to the TDR register. Set the transmission format in the SMR register before setting the TE bit to 1.

RIE bit (Receive Interrupt Enable)

The RIE bit enables or disables SCIn_RXI and SCIn_ERI interrupt requests.

SCIn_RXI and SCIn_ERI interrupt requests are disabled by setting the RIE bit to 0.

An SCIn_ERI interrupt request can be canceled by reading 1 from the ORER, FER, or PER flag in SSR/SSR_FIFO then setting the flag to 0, or by setting the RIE bit to 0.

TIE bit (Transmit Interrupt Enable)

The TIE bit enables or disables SCIn_TXI interrupt requests. SCIn_TXI interrupt requests are disabled by setting the TIE bit to 0. Set the TIE bit to 1 while the TE bit is 1. The SCIn_TXI interrupt occurs after TE and TIE bits are set to 1 simultaneously, before transfer starts.

CKE[1:0]位（时钟使能）

CKE[1:0]位选择时钟源和SCKn引脚功能。

TEIE位（发送结束中断使能）

TEIE位启用或禁用SCIn_TEI中断请求。将TEIE设置为0以禁用SCIn_TEI中断请求。

在简单IIC模式下，SCIn_TEI在完成发出启动、重新启动或停止条件(STIn)时分配给中断。在这种情况下，TEIE位可用于启用或禁用STI。

MPIE位（多处理器中断使能）

当MPIE位设置为1并且接收到多处理器位设置为0的数据时，不读取数据并且将SSRSSR_FIFO中的状态标志RDRF、ORER和FER设置为1被禁用。当接收到多处理器位设置为1的数据时，MPIE位自动清除为0，并恢复非多处理器接收。有关详细信息，请参阅第34.4节，多处理器通信功能。

当SSR寄存器的MPB位为0时，接收数据不会从RSR寄存器传送到RDR寄存器，不会检测到接收错误，并且将标志ORER和FER设置为1被禁止。

当MPB位设置为1时，MPIE位自动清零，启用SCIn_RXI和SCIn_ERI中断请求（如果SCR中的RIE位设置为1），并且启用ORER和FER标志设置为1.

如果不使用多处理器通信功能，则将MPIE设置为0。

RE位（接收使能）

RE位启用或禁用串行接收。当RE位设置为1时，串行接收通过检测异步模式下的起始位或时钟同步模式下的同步时钟输入来启动。在将RE位设置为1之前，在SMR寄存器中设置接收格式。

在非FIFO操作中，当通过将RE位设置为0来停止接收时，RDRF、ORER、FER和PER标志SSR寄存器不受影响，保留之前的值。

WhenFIFOoperationisselectedandreceptionishaltedbysettingtheREbitto0 theRDF ORER FER PER andDRflagsinSSR_FIFOarenotaffectedandthepreviousvaluesareretained.

TE位（发送使能）

TE位启用或禁用串行传输。

当TE位设置为1时，通过将发送数据写入TDR寄存器开始串行发送。在将TE位设置为1之前，在SMR寄存器中设置传输格式。

RIE位（接收中断使能）

RIE位启用或禁用SCIn_RXI和SCIn_ERI中断请求。

通过将RIE位设置为0来禁用SCIn_RXI和SCIn_ERI中断请求。

SCIn_ERI中断请求可以通过从SSRSSR_FIFO中的ORER、FER或PER标志读取1然后将该标志设置为0或通过将RIE位设置为0来取消。

TIE位（发送中断使能）

TIE位启用或禁用SCIn_TXI中断请求。通过将TIE位设置为0来禁用SCIn_TXI中断请求。在TE位为1时将TIE位设置为1。在TE和TIE位同时设置为1之后，在传输开始之前发生SCIn_TXI中断。

34.2.12 Serial Control Register for Smart Card Interface Mode (SCR_SMCI) (SCMR.SMIF = 1)

Address(es): SCI0.SCR_SMCI 4007 0002h, SCI1.SCR_SMCI 4007 0022h, SCI2.SCR_SMCI 4007 0042h, SCI3.SCR_SMCI 4007 0062h, SCI4.SCR_SMCI 4007 0082h, SCI5.SCR_SMCI 4007 00A2h, SCI6.SCR_SMCI 4007 00C2h, SCI7.SCR_SMCI 4007 00E2h, SCI8.SCR_SMCI 4007 0102h, SCI9.SCR_SMCI 4007 0122h

	b7	b6	b5	b4	b3	b2	b1	b0
	TIE	RIE	TE	RE	MPIE	TEIE	CKE[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	CKE[1:0]	Clock Enable	• When SMR_SMCI.GM = 0: b1 b0 0 0: Disable output The SCKn pin is available for use as an I/O port if set up in the I/O port settings 0 1: Output clock 1 x: Setting prohibited. • When SMR_SMCI.GM = 1: b1 b0 0 0: Fix output low x 1: Output clock 1 0: Fix output high.	R/W*1
b2	TEIE	Transmit End Interrupt Enable	Set this bit to 0 in smart card interface mode	R/W
b3	MPIE	Multi-Processor Interrupt Enable	Set this bit to 0 in smart card interface mode	R/W
b4	RE	Receive Enable	0: Disable serial reception 1: Enable serial reception.	R/W*2
b5	TE	Transmit Enable	0: Disable serial transmission 1: Enable serial transmission.	R/W*2
b6	RIE	Receive Interrupt Enable	0: Disable SCIn_RXI and SCIn_ERI interrupt requests 1: Enable SCIn_RXI and SCIn_ERI interrupt requests.	R/W
b7	TIE	Transmit Interrupt Enable	0: Disable SCIn_TXI interrupt requests 1: Enable SCIn_TXI interrupt requests.	R/W

x: Don't care
Note 1. Writable only when TE = 0 and RE = 0.
Note 2. 1 can be written only when TE = 0 and RE = 0. After setting TE or RE to 1, only 0 can be written to TE and RE.

The SCR_SMCI register sets transmission and reception control, interrupt control, and clock source selection for transmission and reception.

For details on interrupt requests, see section 34.10, Interrupt Sources.

CKE[1:0] bits (Clock Enable)

The CKE[1:0] bits control the clock output from the SCKn pin. In GSM mode, clock output can be dynamically switched. For details, see section 34.6.8, Clock Output Control.

TEIE bit (Transmit End Interrupt Enable)

Set the TEIE bit to 0 in smart card interface mode.

MPIE bit (Multi-Processor Interrupt Enable)

Set the MPIE bit to 0 in smart card interface mode.

RE bit (Receive Enable)

The RE bit enables or disables serial reception. When the RE bit is set to 1, serial reception starts by detecting the start bit. Set the reception format in the SMR_SMCI register before setting the RE bit to 1.

34.2.12 智能卡接口模式的串行控制寄存器(SCR_SMCI)(SCMR.SMIF=1)

Address(es): SCI0.SCR_SMCI 4007 0002h, SCI1.SCR_SMCI 4007 0022h, SCI2.SCR_SMCI 4007 0042h, SCI3.SCR_SMCI 4007 0062h, SCI4.SCR_SMCI 4007 0082h, SCI5.SCR_SMCI 4007 00A2h, SCI6.SCR_SMCI 4007 00C2h, SCI7.SCR_SMCI 4007 00E2h, SCI8.SCR_SMCI 4007 0102h, SCI9.SCR_SMCI 4007 0122h

	b7	b6	b5	b4	b3	b2	b1	b0
	TIE	RIE	TE	RE	MPIE	TEIE	CKE[1:0]	
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b1, b0	CKE[1:0]	时钟使能	当SMR_SMCI.GM=0时：b1b 000：禁用输出 如果在IO端口设置中设置SCKn引脚可用作IO端口01：输出时钟1x：禁止设置。 当SMR_SMCI.GM=1时：b1b 000：固定输出低x1：输出时钟10：固定输出高。	R/W*1
b2	TEIE	发送结束中断使能	在智能卡接口模式下将此位设置为0	R/W
b3	MPIE	多处理器中断使能	在智能卡接口模式下将此位设置为0	R/W
b4	RE	接收启用	0：禁用串行接收1：启用串行接收。	R/W*2
b5	TE	发送启用	0：禁用串行传输1：启用串行传输。	R/W*2
b6	RIE	接收中断使能	0：禁用SCIn_RXI和SCIn_ERI中断请求1：启用SCIn_RXI和SCIn_ERI中断请求。	R/W
b7	TIE	发送中断使能	0：禁用SCIn_TXI中断请求1：启用SCIn_TXI中断请求。	R/W

x：不关心注
1。 仅当TE=0且RE=0时可写。
Note 2. 只有在TE=0和RE=0时才能写入1。将TE或RE设置为1后，TE和RE只能写入0。

SCR_SMCI寄存器设置发送和接收的发送和接收控制、中断控制以及发送和接收的时钟源选择。

有关中断请求的详细信息，请参见第34.10节，中断源。

CKE[1:0]位（时钟使能）

CKE[1:0]位控制SCKn引脚的时钟输出。在GSM模式下，时钟输出可以动态切换。有关详细信息，请参见第34.6.8节，时钟输出控制。

TEIE位（发送结束中断使能）

在智能卡接口模式下将TEIE位设置为0。

MPIE位（多处理器中断使能）

在智能卡接口模式下将MPIE位设置为0。

RE位（接收使能）

RE位启用或禁用串行接收。当RE位设置为1时，串行接收通过检测起始位开始。在将RE位设置为1之前，在SMR_SMCI寄存器中设置接收格式。

If reception is halted by setting the RE bit to 0, the ORER, FER, and PER flags in SSR_SMCI are not affected and the previous values are retained.

TE bit (Transmit Enable)

The TE bit enables or disables serial transmission. When the TE bit is set to 1, serial transmission is started by writing transmit data to TDR. Set the transmission format in the SMR_SMCI register before setting the TE bit to 1.

RIE bit (Receive Interrupt Enable)

The RIE bit enables or disables SCIn_RXI and SCIn_ERI interrupt requests.

SCIn_RXI and SCIn_ERI interrupt requests are disabled by setting the RIE bit to 0.

An SCIn_ERI interrupt request can be canceled by reading 1 from the ORER, FER, or PER flag in the SSR_SMCI register, and then setting the flag to 0, or by setting the RIE bit to 0.

TIE bit (Transmit Interrupt Enable)

The TIE bit enables or disables SCIn_TXI interrupt requests. SCIn_TXI interrupt requests are disabled by setting the TIE bit to 0. Set the TIE bit to 1 while the TE bit is 1. The SCIn_TXI interrupt occurs after TE and TIE bits are set to 1 simultaneously, before transfer starts.

34.2.13 Serial Status Register (SSR) for Non-Smart Card Interface and Non-FIFO Mode (SCMR.SMIF = 0 and FCR.FM = 0)

Address(es): SCI0.SSR 4007 0004h, SCI1.SSR 4007 0024h, SCI2.SSR 4007 0044h, SCI3.SSR 4007 0064h, SCI4.SSR 4007 0084h, SCI5.SSR 4007 00A4h, SCI6.SSR 4007 00C4h, SCI7.SSR 4007 00E4h, SCI8.SSR 4007 0104h, SCI9.SSR 4007 0124h

	b7	b6	b5	b4	b3	b2	b1	b0
	TDRE	RDRF	ORER	FER	PER	TEND	MPB	MPBT
Value after reset:	1	0	0	0	0	1	0	0

Bit	Symbol	Bit name	Description	R/W
b0	MPBT	Multi-Processor Bit Transfer	Sets the value of the multi-processor bit in the transmission frame: 0: Data transmission cycle 1: ID transmission cycle.	R/W
b1	MPB	Multi-Processor	Value of the multi-processor bit in the reception frame: 0: Data transmission cycle 1: ID transmission cycle.	R
b2	TEND	Transmit End Flag	0: A character is being transmitted 1: Character transfer is complete.	R
b3	PER	Parity Error Flag	0: No parity error occurred 1: Parity error occurred.	R/(W)*1
b4	FER	Framing Error Flag	0: No framing error occurred 1: Framing error occurred.	R/(W)*1
b5	ORER	Overrun Error Flag	0: No overrun error occurred 1: Overrun error occurred.	R/(W)*1
b6	RDRF	Receive Data Full Flag	0: No received data in RDR register 1: Received data in RDR register.	R/(W)*1
b7	TDRE	Transmit Data Empty Flag	0: Transmit data in TDR register 1: No transmit data in TDR register.	R/(W)*1

Note 1. Only 0 can be written to clear the flag after reading 1.

The SSR register provides SCI status flags and transmission and reception multi-processor bits.

如果通过将RE位设置为0来停止接收，则SSR_SMCI中的ORER、FER和PER标志不受影响，并且保留以前的值。

TE位（发送使能）

TE位启用或禁用串行传输。当TE位设置为1时，通过将发送数据写入TDR开始串行发送。在将TE位设置为1之前，在SMR_SMCI寄存器中设置传输格式。

RIE位（接收中断使能）

RIE位启用或禁用SCIn_RXI和SCIn_ERI中断请求。

通过将RIE位设置为0来禁用SCIn_RXI和SCIn_ERI中断请求。

通过从SSR_SMCI寄存器中的ORER、FER或PER标志读取1，然后将该标志设置为0，或将RIE位设置为0，可以取消SCIn_ERI中断请求。

TIE位（发送中断使能）

TIE位启用或禁用SCIn_TXI中断请求。通过将TIE位设置为0来禁用SCIn_TXI中断请求。在TE位为1时将TIE位设置为1。在TE和TIE位同时设置为1之后，在传输开始之前发生SCIn_TXI中断。

34.2.13 用于非智能卡接口和非FIFO模式的串行状态寄存器(SSR)（SCMR.SMIF=0和FCR.FM=0）

Address(es): SCI0.SSR 4007 0004h, SCI1.SSR 4007 0024h, SCI2.SSR 4007 0044h, SCI3.SSR 4007 0064h, SCI4.SSR 4007 0084h, SCI5.SSR 4007 00A4h, SCI6.SSR 4007 00C4h, SCI7.SSR 4007 00E4h, SCI8.SSR 4007 0104h, SCI9.SSR 4007 0124h

	b7	b6	b5	b4	b3	b2	b1	b0
	TDRE	RDRF	ORER	FER	PER	TEND	MPB	MPBT
重置后的值：	1	0	0	0	0	1	0	0

Bit	Symbol	位名称	Description	R/W
b0	MPBT	多处理器位传输	设置传输帧中多处理器位的值：0：数据传输周期1：ID传输周期。	R/W
b1	MPB	Multi-Processor	接收帧中多处理器位的值：0：数据发送周期1：ID发送周期。	R
b2	TEND	发送结束标志	0：正在传输字符1：字符传输完成。	R
b3	PER	奇偶校验错误标志	0：未发生奇偶校验错误1：发生奇偶校验错误。	R/(W)*1
b4	FER	成帧错误标志	0：未发生帧错误1：发生帧错误。	R/(W)*1
b5	ORER	溢出错误标志	0：未发生溢出错误1：发生溢出错误。	R/(W)*1
b6	RDRF	接收数据满标志	0：RDR寄存器中没有接收到数据1：RDR寄存器中接收到数据。	R/(W)*1
b7	TDRE	传输数据空标志	0：在TDR寄存器中发送数据1：在TDR寄存器中不发送数据。	R/(W)*1

Note 1. 读1后只能写0清除标志。

SSR寄存器提供SCI状态标志和发送和接收多处理器位。

MPBT bit (Multi-Processor Bit Transfer)

The MPBT bit sets the value of the multi-processor bit in the transmit frame.

MPB bit (Multi-Processor)

The MPB bit holds the value of the multi-processor bit in the reception frame. This bit does not change when the SCR.RE bit is 0.

TEND flag (Transmit End Flag)

The TEND flag indicates completion of transmission.

[Setting conditions]

- When the SCR.TE bit is set to 0 (serial transmission is disabled) and the FCR.FM bit is set to 0 (non-FIFO selected). When the SCR.TE bit is set to 1, the TEND flag is not affected and retains the value 1.
- When the TDR register is not updated on transmission of the tail-end bit of a character being transmitted.

[Clearing conditions]

- When transmit data is written to the TDR register while the SCR.TE bit is 1
- When 0 is written to TDRE after 1 is read while the SCR.TE bit is 1.

PER flag (Parity Error Flag)

The PER flag indicates that a parity error occurred during reception in asynchronous mode and the reception ended abnormally.

[Setting condition]

- When a parity error is detected during reception in asynchronous mode when the address match function is disabled (DCCR.DCME = 0).

  Although receive data is transferred to the RDR register when the parity error occurs, no SCIn_RXI interrupt request occurs. When the PER flag is set to 1, the subsequent receive data is not transferred to the RDR register.

[Clearing condition]

- When 0 is written to the PER flag after 1 is read. After writing 0 to this flag, read it to verify that its value is 0.

When the SCR.RE bit is set to 0 (serial reception is disabled), the PER flag is not affected and retains its previous value.

FER flag (Framing Error Flag)

The FER flag indicates that a framing error occurred during reception in asynchronous mode and the reception ended abnormally.

[Setting condition]

- When 0 is sampled as the stop bit during reception in asynchronous mode when the address match function is disabled (DCCR.DCME = 0).

  In 2-stop-bit mode, only the first stop bit is checked. The second stop bit is not checked. Although receive data is transferred to the RDR register when the framing error occurs, no SCIn_RXI interrupt request occurs. When the FER flag is to 1, the subsequent receive data is not transferred to the RDR register.

[Clearing condition]

- When 0 is written to FER after 1 is read. After writing 0 to this flag, read it to verify that its value is 0.

When the SCR.RE bit is set to 0 (serial reception is disabled), the FER flag is not affected and retains its previous value.

ORER flag (Overrun Error Flag)

The ORER flag indicates that an overrun error occurred during reception and the reception ended abnormally.

[Setting condition]

- When the next data is received before receive data that does not have a parity error and a framing error is read from the RDR register.

MPBT位（多处理器位传输）

MPBT位设置发送帧中多处理器位的值。

MPB bit (Multi-Processor)

MPB位保存接收帧中多处理器位的值。该位不改变时
SCR.RE位为0。

TEND标志（发送结束标志）

TEND标志表示传输完成。

[Setting conditions]

- 当SCR.TE位设置为0（禁用串行传输）且FCR.FM位设置为0（选择非FIFO）时。
  当SCR.TE位设置为1时，TEND标志不受影响并保持值1。
- 当TDR寄存器未在传输字符的尾端位时更新时。

[Clearing conditions]

- 当SCR.TE位为1时将发送数据写入TDR寄存器
- 当SCR.TE位为1时读取1后将0写入TDRE。

PER标志（奇偶校验错误标志）

PER标志表示在异步模式接收过程中发生奇偶校验错误，接收异常结束。

[Setting condition]

- 当地址匹配功能被禁用(DCCR.DCME=0)时，在异步模式接收期间检测到奇偶校验错误。

尽管发生奇偶校验错误时接收数据被传送到RDR寄存器，但不会发生SCIn_RXI中断请求。当PER标志设置为1时，后续接收数据不会传送到RDR寄存器。【结算条件】

- 读取1后将0写入PER标志时。将0写入此标志后，读取它以验证其值为0。

当SCR.RE位设置为0（禁用串行接收）时，PER标志不受影响并保留其先前的值。

FER标志（帧错误标志）

FER标志表示在异步模式下接收过程中发生了帧错误，并且接收异常结束。

[Setting condition]

- 当地址匹配功能被禁用(DCCR.DCME=0)时，在异步模式接收期间采样0作为停止位。

在2停止位模式下，仅检查第一个停止位。不检查第二个停止位。虽然发生帧错误时接收数据被传输到RDR寄存器，但不会发生SCIn_RXI中断请求。当FER标志为1时，后续接收数据不传送到RDR寄存器。【结算条件】

- 在读取1后将0写入FER时。将0写入此标志后，读取它以验证其值为0。

当SCR.RE位设置为0（禁用串行接收）时，FER标志不受影响并保留其先前的值。

ORER标志（溢出错误标志）

ORER标志表示接收期间发生溢出错误，接收异常结束。

[Setting condition]

- 在接收没有奇偶校验错误和帧错误的数据之前接收下一个数据时，从RDR寄存器中读取。

The data received before an overrun error occurred is saved in the RDR register, but data received after the error is lost. When the ORER flag is set to 1, receive data is not forwarded to the RDR register. In clock synchronous mode, serial transmission and reception are stopped.

[Clearing condition]

- When 0 is written to the ORER flag after 1 is read. After writing 0 to this flag, read it to verify that its value is 0.

When the SCR.RE bit is set to 0 (serial reception is disabled), the ORER flag is not affected and retains its previous value.

RDRF flag (Receive Data Full Flag)

The RDRF flag indicates the presence of receive data in the RDR register.

[Setting condition]

- When the reception ends normally, and receive data is forwarded from the RSR register to the RDR register.

[Clearing conditions]

- When 0 is written to the RDRF flag after 1 is read
- When data is read from the RDR register.

Note: Do not clear RDRF flag by accessing RDRF bit in the SSR register unless communication is aborted.

TDRE flag (Transmit Data Empty Flag)

The TDRE flag indicates the presence of transmit data in the TDR register.

[Setting conditions]

- When the SCR.TE bit is 0
- When data is transmitted from the TDR register to the TSR register.

[Clearing conditions]

- When 0 is written to the TDRE flag after 1 is read
- When the SCR.TE bit is 1 and data is written to the TDR register.

Note: Do not clear TDRE flag by accessing TDRE bit in the SSR register unless communication is aborted.

34.2.14 Serial Status Register for Non-Smart Card Interface and FIFO Mode (SSR_FIFO) (SCMR.SMIF = 0 and FCR.FM = 1)

Address(es): SCI0.SSR_FIFO 4007 0004h, SCI1.SSR_FIFO 4007 0024h, SCI2.SSR_FIFO 4007 0044h, SCI3.SSR_FIFO 4007 0064h, SCI4.SSR_FIFO 4007 0084h, SCI5.SSR_FIFO 4007 00A4h, SCI6.SSR_FIFO 4007 00C4h, SCI7.SSR_FIFO 4007 00E4h, SCI8.SSR_FIFO 4007 0104h, SCI9.SSR_FIFO 4007 0124h

	b7	b6	b5	b4	b3	b2	b1	b0
	TDFE	RDF	ORER	FER	PER	TEND	—	DR
Value after reset:	1	0	0	0	0	0	x	0

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b0	DR	Receive Data Ready Flag	0: Receiving is in progress, or no received data remains in FRDRHL after successfully completed reception (receive FIFO empty) 1: Next receive data is not received for a period after normal receiving is complete, when the amount of data stored in the FIFO is equal to or less than the receive triggering number.	R/(W)*1
b1	—	Reserved	The read value is undefined. The write value should be 1.	R/W

溢出错误发生前接收到的数据保存在RDR寄存器中，但错误发生后接收到的数据丢失。当ORER标志设置为1时，接收数据不转发到RDR寄存器。在时钟同步模式下，串行发送和接收停止。【结算条件】

- 在读取1后将0写入ORER标志时。将0写入此标志后，读取它以验证其值为0。

当SCR.RE位设置为0（禁用串行接收）时，ORER标志不受影响并保留其先前的值。

RDRF标志（接收数据满标志）

RDRF标志指示RDR寄存器中存在接收数据。

[Setting condition]

- 当接收正常结束时，接收数据从RSR寄存器转发到RDR寄存器。

[Clearing conditions]

- 读取1后向RDRF标志写入0时
- 从RDR寄存器读取数据时。

Note: 除非通信中止，否则不要通过访问SSR寄存器中的RDRF位来清除RDRF标志。

TDRE标志（传输数据空标志）

TDRE标志表示TDR寄存器中存在发送数据。

[Setting conditions]

- 当SCR.TE位为0时
- 当数据从TDR寄存器传输到TSR寄存器时。

[Clearing conditions]

- 读取1后向TDRE标志写入0时
- 当SCR.TE位为1且数据写入TDR寄存器时。

Note: 除非通信被中止，否则不要通过访问SSR寄存器中的TDRE位来清除TDRE标志。

34.2.14 非智能卡接口和FIFO模式的串行状态寄存器(SSR_FIFO)（SCMR.SMIF=0和FCR.FM=1）

Address(es): SCI0.SSR_FIFO 4007 0004h, SCI1.SSR_FIFO 4007 0024h, SCI2.SSR_FIFO 4007 0044h, SCI3.SSR_FIFO 4007 0064h, SCI4.SSR_FIFO 4007 0084h, SCI5.SSR_FIFO 4007 00A4h, SCI6.SSR_FIFO 4007 00C4h, SCI7.SSR_FIFO 4007 00E4h, SCI8.SSR_FIFO 4007 0104h, SCI9.SSR_FIFO 4007 0124h

	b7	b6	b5	b4	b3	b2	b1	b0
	TDFE	RDF	ORER	FER	PER	TEND	—	DR
重置后的值：	1	0	0	0	0	0	x	0

x: Undefined

Bit	Symbol	位名称	Description	R/W
b0	DR	接收数据就绪标志	0：接收中，或者接收成功后FRDRHL中没有接收到的数据（接收FIFO为空）1：在一段时间内没有接收到下一个接收数据 当FIFO中存储的数据量等于或小于接收触发数时，正常接收完成。	R/(W)*1
b1	—	Reserved	读取值未定义。写入值应为1。	R/W

Bit	Symbol	Bit name	Description	R/W
b2	TEND	Transmit End Flag	0: A character is being transmitted 1: Character transfer is complete.	R/(W)*1
b3	PER	Parity Error Flag	0: No parity error occurred 1: Parity error occurred.	R/(W)*1
b4	FER	Framing Error Flag	0: No framing error occurred 1: Framing error occurred.	R/(W)*1
b5	ORER	Overrun Error Flag	0: No overrun error occurred 1: Overrun error occurred.	R/(W)*1
b6	RDF	Receive FIFO Data Full Flag	0: The amount of receive data written in FRDRHL is less than the specified receive triggering number 1: The amount of receive data written in FRDRHL is equal to or greater than the specified receive triggering number.	R/(W)*1
b7	TDFE	Transmit FIFO Data Empty Flag	0: The amount of transmit data written in FTDRHL exceeds the specified transmit triggering number 1: The amount of transmit data written in FTDRHL is equal to or less than the specified transmit triggering number.	R/(W)*1

Note 1. Only 0 can be written, to clear the flag after reading 1.

The SSR_FIFO register provides the SCI with FIFO mode status flags.

DR flag (Receive Data Ready Flag)

The DR flag indicates that the amount of data stored in the Receive FIFO Data Register (FRDRHL) falls below the specified receive triggering number, and that no next data is received after 15 ETUs (elementary time units) from the last stop bit in asynchronous mode. This flag is valid only in asynchronous mode, including multi-processor mode, when FIFO operation is selected.

In clock synchronous mode, the DR flag is not set to 1.

[Setting condition]

- When FRDRHL contains less data than the specified receive triggering number, and no next data is received after 15 ETUs*1 from the last stop bit, and the SSR_FIFO.FER and SSR_FIFO.PER flags are 0.

[Clearing conditions]

- When 1 is read from DR, after all received data is read
- When the FCR.FM bit is changed from 0 to 1.

Note 1. This is equivalent to 1.5 frames in the 8-bit format with one stop bit.
The DR flag is only set to 1 when FIFO is selected in asynchronous mode, including multi-processor mode. It is not set to 1 in other operation modes.

TEND flag (Transmit End Flag)

The TEND flag indicates that FTDRHL does not contain valid data when transmitting the last bit of a serial character, so the transmission is halted.

[Setting condition]

- When FTDRHL does not contain transmit data when the last bit of a 1-byte serial character is transmitted.

[Clearing conditions]

- When transmit data is written to FTDRHL while the SCR.TE bit is 1
- When 0 is written to the TEND flag after 1 is read while the SCR.TE bit is 1
- When the FCR.FM bit is changed from 0 to 1.

Bit	Symbol	位名称	Description	R/W
b2	TEND	发送结束标志	0：正在传输字符1：字符传输完成。	R/(W)*1
b3	PER	奇偶校验错误标志	0：未发生奇偶校验错误1：发生奇偶校验错误。	R/(W)*1
b4	FER	成帧错误标志	0：未发生帧错误1：发生帧错误。	R/(W)*1
b5	ORER	溢出错误标志	0：未发生溢出错误1：发生溢出错误。	R/(W)*1
b6	RDF	接收FIFO数据满标志	0：写入FRDRHL的接收数据量小于指定的接收触发数1：写入FRDRHL的接收数据量为 等于或大于指定的接收触发数。	R/(W)*1
b7	TDFE	发送FIFO数据空标志	0：写入FTDRHL的发送数据量超过指定的发送触发数1：写入FTDRHL的发送数据量等于或小于指定的发送触发数。	R/(W)*1

Note 1. 只能写入0，读取1后清除标志。

SSR_FIFO寄存器为SCI提供FIFO模式状态标志。

DR标志（接收数据就绪标志）

DR标志表示存储在接收FIFO数据寄存器(FRDRHL)中的数据量低于指定的接收触发数，并且在异步模式下从最后一个停止位开始15个ETU（基本时间单位）后没有接收到下一个数据.此标志仅在选择FIFO操作时在异步模式下有效，包括多处理器模式。

在时钟同步模式下，DR标志不设置为1。

[Setting condition]

- 当FRDRHL包含的数据少于指定的接收触发数，并且从最后一个停止位开始15个ETU*1后没有接收到下一个数据，并且SSR_FIFO.FER和SSR_FIFO.PER标志为0。

[Clearing conditions]

- 从DR读取1时，在读取所有接收到的数据之后
- 当FCR.FM位从0变为1时。

注1.这相当于8位格式的1.5帧，带有一位停止位。
只有在异步模式（包括多处理器模式）下选择FIFO时，DR标志才设置为1。在其他操作模式下不设置为1。

TEND标志（发送结束标志）

TEND标志表明FTDRHL在发送串行字符的最后一位时不包含有效数据，因此暂停发送。

[Setting condition]

- 当传输1字节串行字符的最后一位时FTDRHL不包含传输数据。

[Clearing conditions]

- 当SCR.TE位为1时将发送数据写入FTDRHL
- 当SCR.TE位为1时读取1后将0写入TEND标志
- 当FCR.FM位从0变为1时。

PER flag (Parity Error Flag)

The PER flag indicates whether there is a parity error in the data read from the FRDRHL register in asynchronous mode when the address match function is disabled (DCCR.DCME = 0).

[Setting condition]

- When data is received and a parity error is detected, when the address match function is disabled (DCCR.DCME = 0).

[Clearing condition]

- When 0 is written to the PER flag after 1 is read.

The reception operation is continuous, and the receive data is stored in the FRDRHL register, even when a parity error occurs during reception.

When the SCR.RE bit is set to 0 (serial reception is disabled), the PER flag is not affected and retains its previous value.

FER flag (Framing Error Flag)

The FER flag indicates whether there is a framing error in the data read from the FRDRHL register in asynchronous mode when the address match function is disabled (DCCR.DCME = 0).

[Setting condition]

- When 0 is sampled as the stop bit during reception when the address match function is disabled (DCCR.DCME = 0).

[Clearing condition]

- When 0 is written to the FER flag after 1 is read.

The reception operation is continuous, and the receive data is stored in the FRDRHL register, even when a framing error occurs during reception.

When the SCR.RE bit is set to 0 (serial reception is disabled), the FER flag is not affected and retains its previous value.

ORER flag (Overrun Error Flag)

The ORER flag indicates that the receive operation stopped abnormally because an overrun error occurred.

[Setting condition]

- When the next serial reception completes while the receive FIFO is full with 16-byte receive data.

[Clearing condition]

- When 0 is written to the ORER flag after 1 is read.

When the SCR.RE bit is set to 0 (serial reception is disabled), the ORER flag is not affected and retains its previous value.

RDF flag (Receive FIFO Data Full Flag)

The RDF flag indicates that receive data was transferred to the FRDRHL register, and the amount of data in FRDRHL is equal to or exceeds the specified receive triggering number. When RTRG is set to 0, the RDF flag is not set even when the amount of data in the receive FIFO is equal to 0.

[Setting condition]

- When the amount of receive data equal to or greater than the specified receive triggering number is stored in FRDRHL,*1 and the FIFO is not empty.

[Clearing conditions]

- When 0 is written to the RDF flag after 1 is read
- When FRDRHL is read by the DMAC or DTC, but only when the block transfer is the last transmission
- When the setting and clearing conditions occur at the same time, the RDF flag is set to 0. After that, when the amount of data stored in the FRDRHL register is equal to or greater than the RTRG value, RDF is set to 1 after 1

PER标志（奇偶校验错误标志）

PER标志指示在禁用地址匹配功能（DCCR.DCME=0）时，异步模式下从FRDRHL寄存器读取的数据是否存在奇偶校验错误。

[Setting condition]

- 当接收到数据并检测到奇偶校验错误时，当地址匹配功能被禁用时(DCCR.DCME=0)。

[Clearing condition]

- 读取1后将0写入PER标志时。

接收操作是连续的，接收数据存储在FRDRHL寄存器中，即使在接收过程中发生奇偶校验错误。

当SCR.RE位设置为0（禁用串行接收）时，PER标志不受影响并保留其先前的值。

FER标志（帧错误标志）

FER标志指示在禁用地址匹配功能（DCCR.DCME=0）时，异步模式下从FRDRHL寄存器读取的数据是否存在帧错误。

[Setting condition]

- 当地址匹配功能被禁用(DCCR.DCME=0)时，在接收期间采样0作为停止位。

[Clearing condition]

- 读取1后将0写入FER标志时。

接收操作是连续的，接收数据存储在FRDRHL寄存器中，即使在接收过程中发生帧错误。

当SCR.RE位设置为0（禁用串行接收）时，FER标志不受影响并保留其先前的值。

ORER标志（溢出错误标志）

ORER标志指示接收操作由于发生溢出错误而异常停止。

[Setting condition]

- 当接收FIFO充满16字节接收数据时，下一次串行接收完成。

[Clearing condition]

- 在读取1后将0写入ORER标志时。

当SCR.RE位设置为0（禁用串行接收）时，ORER标志不受影响并保留其先前的值。

RDF标志（接收FIFO数据满标志）

RDF标志表示接收数据已传送到FRDRHL寄存器，并且FRDRHL中的数据量等于或超过指定的接收触发数。当RTRG设置为0时，即使接收FIFO中的数据量等于0，RDF标志也不会设置。

[Setting condition]

- 当接收数据量等于或大于指定的接收触发数时存储在FRDRHL *1且FIFO不为空。

[Clearing conditions]

- 读取1后向RDF标志写入0时
- 当DMAC或DTC读取FRDRHL时，但仅当块传输是最后一次传输时
- 当置位和清零条件同时发生时，RDF标志置0。之后，当FRDRHL寄存器中存储的数据量等于或大于RTRG值时，RDF在1后置1

PCLKA.

Note: Do not clear RDF flags by accessing RDF bit in the SSR register before reading receive data unless communication is aborted.

Note 1. Because FRDRHL is a 16-stage FIFO register, the maximum amount of data that can be read when RDF is 1 is equivalent to the specified receive triggering number. If an attempt is made to read after all the data in FRDRHL is read, the data is undefined.

TDFE flag (Transmit FIFO Data Empty Flag)

The TDFE flag indicates that data is transferred from the FTDRHL register into the TSR register, the amount of data in FTDRHL is below the specified transmit triggering number, and writing of transmit data to FTDRHL is enabled.

[Setting conditions]

- When the TE bit in SCR is 0
- When the amount of transmit data written in FTDRHL is equal to or less than the specified transmit triggering number.*1

[Clearing conditions]

- When writing to FTDRHL is executed on the last transmission while the DTC or DMAC is activated
- When 0 is written to the TDFE flag after reading 1 is read.
  The setting conditions are given priority when TE = 0. When the setting condition and clearing condition occur at the same time, the TDFE flag is set to 0. After that, when the amount of data stored in the FTDRHL register is equal to or less than the TTRG value, TDFE is set to 1 after 1 PCLKA.

Note: Do not clear TDFE flags by accessing TDFE bit in the SSR register before writing transmit data unless communication is aborted.

Note 1. Because the FTDRHL register is a 16-stage FIFO register, when the TDFE flag is 1, the maximum amount of data that can be written to the FTDRHL register is 16 minus FDR.T[4:0] bytes. If more data is written, data is discarded.

34.2.15 Serial Status Register for Smart Card Interface Mode (SSR_SMCI) (SCMR.SMIF = 1)

Address(es): SCI0.SSR_SMCI 4007 0004h, SCI1.SSR_SMCI 4007 0024h, SCI2.SSR_SMCI 4007 0044h, SCI3.SSR_SMCI 4007 0064h, SCI4.SSR_SMCI 4007 0084h, SCI5.SSR_SMCI 4007 00A4h, SCI6.SSR_SMCI 4007 00C4h, SCI7.SSR_SMCI 4007 00E4h, SCI8.SSR_SMCI 4007 0104h, SCI9.SSR_SMCI 4007 0124h

	b7	b6	b5	b4	b3	b2	b1	b0
	TDRE	RDRF	ORER	ERS	PER	TEND	MPB	MPBT
Value after reset:	1	0	0	0	0	1	0	0

Bit	Symbol	Bit name	Description	R/W
b0	MPBT	Multi-Processor Bit Transfer	Set this bit to 0 in smart card interface mode	R/W
b1	MPB	Multi-Processor	Set this bit to 0 in smart card interface mode	R
b2	TEND	Transmit End Flag	0: A character is being transmitted 1: Character transfer is complete.	R
b3	PER	Parity Error Flag	0: No parity error occurred 1: Parity error occurred.	R/(W)*
b4	ERS	Error Signal Status Flag	0: No low error signal response 1: Low error signal response occurred.	R/(W)*1
b5	ORER	Overrun Error Flag	0: No overrun error occurred 1: Overrun error occurred.	R/(W)*1
b6	RDRF	Receive Data Full Flag	0: No received data in RDR register 1: Received data in RDR register.	R/(W)*1

PCLKA.

注意：除非通信中止，否则在读取接收数据之前不要通过访问SSR寄存器中的RDF位来清除RDF标志。注1.因为FRDRHL是16级FIFO寄存器，所以当RDF为1时可以读取的最大数据量等于指定的接收触发数。如果在读取FRDRHL中的所有数据后尝试读取，则数据未定义。

TDFE标志（发送FIFO数据空标志）

TDFE标志表示数据从FTDRHL寄存器传送到TSR寄存器，在
FTDRHL低于指定的发送触发数，并且允许将发送数据写入FTDRHL。

[Setting conditions]

- 当SCR的TE位为0时
- 当写入FTDRHL的传输数据量等于或小于指定的传输触发数时。*1

[Clearing conditions]

- 当DTC或DMAC被激活时，在最后一次传输上执行写入FTDRHL
- 当读取1后将0写入TDFE标志。
  当TE=0时，设置条件优先。当设置条件和清除条件同时发生时，TDFE标志设置为0。之后，当FTDRHL寄存器中存储的数据量等于或小于比TTRG值，TDFE在1个PCLKA之后设置为1。

注意：除非通信被中止，否则在写入发送数据之前不要通过访问SSR寄存器中的TDFE位来清除TDFE标志。注1.由于FTDRHL寄存器为16级FIFO寄存器，因此当TDFE标志为1时，可写入FTDRHL寄存器的最大数据量为16减去FDR.T[4:0]字节。如果写入更多数据，则丢弃数据。

34.2.15 智能卡接口模式的串行状态寄存器(SSR_SMCI)(SCMR.SMIF=1)

Address(es): SCI0.SSR_SMCI 4007 0004h, SCI1.SSR_SMCI 4007 0024h, SCI2.SSR_SMCI 4007 0044h, SCI3.SSR_SMCI 4007 0064h, SCI4.SSR_SMCI 4007 0084h, SCI5.SSR_SMCI 4007 00A4h, SCI6.SSR_SMCI 4007 00C4h, SCI7.SSR_SMCI 4007 00E4h, SCI8.SSR_SMCI 4007 0104h, SCI9.SSR_SMCI 4007 0124h

	b7	b6	b5	b4	b3	b2	b1	b0
	TDRE	RDRF	ORER	ERS	PER	TEND	MPB	MPBT
重置后的值：	1	0	0	0	0	1	0	0

Bit	Symbol	位名称	Description	R/W
b0	MPBT	多处理器位传输	在智能卡接口模式下将此位设置为0	R/W
b1	MPB	Multi-Processor	在智能卡接口模式下将此位设置为0	R
b2	TEND	发送结束标志	0：正在传输字符1：字符传输完成。	R
b3	PER	奇偶校验错误标志	0：未发生奇偶校验错误1：发生奇偶校验错误。	R/(W)*
b4	ERS	错误信号状态标志	0：无低位错误信号响应1：发生低位错误信号响应。	R/(W)*1
b5	ORER	溢出错误标志	0：未发生溢出错误1：发生溢出错误。	R/(W)*1
b6	RDRF	接收数据满标志	0：RDR寄存器中没有接收到数据1：RDR寄存器中接收到数据。	R/(W)*1

Bit	Symbol	Bit name	Description	R/W
b7	TDRE	Transmit Data Empty Flag	0: Transmit data in TDR register 1: No transmit data in TDR register.	R/(W)*1

Note 1. Only 0 can be written, to clear the flag after 1 is read.

The SSR_SMCI register provides the SCI with smart card interface mode status flags.

TEND flag (Transmit End Flag)

When there is no error signal from the receiving side, the TEND flag is set to 1 when more data for transfer is ready to be transferred to the TDR register.

[Setting conditions]

- When the SCR_SMCI.TE bit = 0 (serial transmission is disabled).
  When the SCR_SMCI.TE bit is changed from 0 to 1, the TEND flag is not affected and retains the value 1.
- When a specified period elapses after the latest transmission of 1 byte, the ERS flag is 0, and the TDR register is not updated.

  The set timing is determined by the following register settings:
  - When SMR_SMCI.GM = 0 and SMR_SMCI.BLK = 0, 12.5 ETUs after the start of transmission
  - When SMR_SMCI.GM = 0 and SMR_SMCI.BLK = 1, 11.5 ETUs after the start of transmission
  - When SMR_SMCI.GM = 1 and SMR_SMCI.BLK = 0, 11.0 ETUs after the start of transmission
  - When SMR_SMCI.GM = 1 and SMR_SMCI.BLK = 1, 11.0 ETUs after the start of transmission.

[Clearing conditions]

- When transmit data is written to the TDR register while the SCR_SMCI.TE bit is 1
- When 0 is written to the TDRE flag after 1 is read while the SCR_SMCI.TE bit is 1.

PER flag (Parity Error Flag)

The PER flag indicates that a parity error occurred during reception in asynchronous mode and the reception ended abnormally.

[Setting condition]

- When a parity error is detected during reception. Although receive data is transferred to RDR when a parity error occurs, no SCIn_RXI interrupt request occurs. After the PER flag is set to 1, the subsequent receive data is not transferred to RDR.

[Clearing condition]

- When 0 is written to the PER flag after 1 is read. After writing 0 to this flag, read it to verify that its value is 0.

When the RE bit in SCR_SMCI is set to 0 (serial reception is disabled), the PER flag is not affected and retains its previous value.

ERS flag (Error Signal Status Flag)

[Setting condition]

- When a low error signal is sampled.

[Clearing condition]

- When 0 is written to the ERS flag after 1 is read.

ORER flag (Overrun Error Flag)

The ORER flag indicates that an overrun error occurred during reception and the reception ended abnormally.

[Setting condition]

- When the next data is received before receive data that does not have a parity error is read from the RDR register.

Bit	Symbol	位名称	Description	R/W
b7	TDRE	传输数据空标志	0：在TDR寄存器中发送数据1：在TDR寄存器中不发送数据。	R/(W)*1

Note 1. 只能写入0，读取1后清除标志。

SSR_SMCI寄存器为SCI提供智能卡接口模式状态标志。

TEND标志（发送结束标志）

当接收端没有错误信号时，当更多数据准备好传输到TDR寄存器时，TEND标志设置为1。

[Setting conditions]

- 当SCR_SMCI.TE位=0时（禁用串行传输）。
  当SCR_SMCI.TE位从0变为1时，TEND标志不受影响并保持值1。
- 在最后一次发送1个字节后经过指定时间后，ERS标志为0，并且不更新TDR寄存器。

  设置时序由以下寄存器设置确定：
  - 当SMR_SMCI.GM=0且SMR_SMCI.BLK=0时，传输开始后12.5ETU
  - 当SMR_SMCI.GM=0且SMR_SMCI.BLK=1时，传输开始后11.5ETU
  - 当SMR_SMCI.GM=1且SMR_SMCI.BLK=0时，传输开始后11.0ETU
  - 当SMR_SMCI.GM=1和SMR_SMCI.BLK=1时，传输开始后11.0ETU。

[Clearing conditions]

- 当SCR_SMCI.TE位为1时将发送数据写入TDR寄存器
- 当SCR_SMCI.TE位为1时读取1后将0写入TDRE标志。

PER标志（奇偶校验错误标志）

PER标志表示在异步模式接收过程中发生奇偶校验错误，接收异常结束。

[Setting condition]

- 在接收过程中检测到奇偶校验错误时。尽管发生奇偶校验错误时将接收数据传输到RDR，但不会发生SCIn_RXI中断请求。PER标志设置为1后，后续接收数据不会传输到RDR。

[Clearing condition]

- 读取1后将0写入PER标志时。将0写入此标志后，读取它以验证其值为0。

当SCR_SMCI中的RE位设置为0（禁用串行接收）时，PER标志不受影响并保留其先前的值。

ERS标志（错误信号状态标志）

[Setting condition]

- 当对低误差信号进行采样时。

[Clearing condition]

- 读取1后将0写入ERS 标志时。

ORER标志（溢出错误标志）

ORER标志表示接收期间发生溢出错误，接收异常结束。

[Setting condition]

- 在从RDR寄存器读取没有奇偶校验错误的接收数据之前接收到下一个数据时。

The data received before an overrun error occurred is saved in the RDR, but data received after the error is lost. When the ORER flag is set to 1, receive data is not forwarded to the RDR register.

[Clearing condition]

- When 0 is written to the ORER flag after 1 is read. After writing 0 to this flag, read it to verify that its value is 0.

When the RE bit in SCR_SMCI is set to 0, the ORER flag is not affected and retains its previous value.

RDRF flag (Receive Data Full Flag)

The RDRF flag indicates the presence of receive data in the RDR register.

[Setting condition]

- When the reception ends normally, and receive data is forwarded from the RSR register to the RDR register.

[Clearing conditions]

- When 0 is written to the RDRF flag after 1 is read
- When data is read from the RDR register.

TDRE flag (Transmit Data Empty Flag)

The TDRE flag indicates the presence of transmit data in the TDR register.

[Setting conditions]

- When the SCR_SMCI.TE bit is 0
- When data is transmitted from the TDR register to the TSR register.

[Clearing conditions]

- When 0 is written to the TDRE flag after 1 is read
- When the SCR_SMCI.TE bit is 1 and data is written to the TDR register.

Note: Do not clear TDRE flags by accessing TDRE bit in the SSR register unless communication is aborted.

34.2.16 Smart Card Mode Register (SCMR)

Address(es): SCI0.SCMR 4007 0006h, SCI1.SCMR 4007 0026h, SCI2.SCMR 4007 0046h, SCI3.SCMR 4007 0066h, SCI4.SCMR 4007 0086h, SCI5.SCMR 4007 00A6h, SCI6.SCMR 4007 00C6h, SCI7.SCMR 4007 00E6h, SCI8.SCMR 4007 0106h, SCI9.SCMR 4007 0126h

	b7	b6	b5	b4	b3	b2	b1	b0
	BCP2	—	—	CHR1	SDIR	SINV	—	SMIF
Value after reset:	1	1	1	1	0	0	1	0

Bit	Symbol	Bit name	Description	R/W
b0	SMIF	Smart Card Interface Mode Select	0: Non-smart card interface mode (asynchronous mode, clock synchronous mode, simple SPI mode, or simple IIC mode) 1: Smart card interface mode.	R/W*1
b1	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b2	SINV	Transmitted/Received Data Invert	0: TDR register contents are transmitted as they are. Receive data is stored as received in the RDR register. 1: TDR register contents are inverted before transmission. Receive data is stored in inverted form in the RDR register. The SINV bit can be used in the following modes: • Smart card interface mode • Asynchronous mode (including multi-processor mode) • Clock synchronous mode • Simple SPI mode. Set the SINV bit to 0 for operation in simple IIC mode.	R/W*1

发生溢出错误前接收的数据保存在RDR中，但错误发生后接收的数据会丢失。
当ORER标志设置为1时，接收数据不转发到RDR寄存器。

[Clearing condition]

- 在读取1后将0写入ORER标志时。将0写入此标志后，读取它以验证其值为0。

当SCR_SMCI中的RE位设置为0时，ORER标志不受影响并保留其先前的值。

RDRF标志（接收数据满标志）

RDRF标志指示RDR寄存器中存在接收数据。

[Setting condition]

- 当接收正常结束时，接收数据从RSR寄存器转发到RDR寄存器。

[Clearing conditions]

- 读取1后向RDRF标志写入0时
- 从RDR寄存器读取数据时。

TDRE标志（传输数据空标志）

TDRE标志表示TDR寄存器中存在发送数据。

[Setting conditions]

- 当SCR_SMCI.TE位为0时
- 当数据从TDR寄存器传输到TSR寄存器时。

[Clearing conditions]

- 读取1后向TDRE标志写入0时
- 当SCR_SMCI.TE位为1且数据写入TDR寄存器时。

Note: 除非通信被中止，否则不要通过访问SSR寄存器中的TDRE位来清除TDRE标志。

34.2.16 智能卡模式寄存器(SCMR)

Address(es): SCI0.SCMR 4007 0006h, SCI1.SCMR 4007 0026h, SCI2.SCMR 4007 0046h, SCI3.SCMR 4007 0066h, SCI4.SCMR 4007 0086h, SCI5.SCMR 4007 00A6h, SCI6.SCMR 4007 00C6h, SCI7.SCMR 4007 00E6h, SCI8.SCMR 4007 0106h, SCI9.SCMR 4007 0126h

	b7	b6	b5	b4	b3	b2	b1	b0
	BCP2	—	—	CHR1	SDIR	SINV	—	SMIF
重置后的值:	1	1	1	1	0	0	1	0

Bit	Symbol	位名称	Description	R/W
b0	SMIF	智能卡接口模式选择	0：非智能卡接口模式 （异步模式、时钟同步模式、简单SPI模式或简单IIC模式） 1：智能卡接口模式。	R/W*1
b1	—	Reserved	该位读取为1。写入值应为1。	R/W
b2	SINV	发送接收数据反转	0：TDR寄存器内容按原样发送。接收数据存储在RDR寄存器中。1：TDR寄存器内容在发送前反转。接收数据以反转形式存储在RDR寄存器中。 SINV位可用于以下模式： 智能卡接口模式 异步模式（包括多处理器模式） 时钟同步模式 简单SPI模式。将SINV位设置为0，以便在简单IIC模式下运行。	R/W*1

Bit	Symbol	Bit name	Description	R/W
b3	SDIR	Transmitted/Received Data Transfer Direction	0: Transfer LSB-first 1: Transfer MSB-first. The SDIR bit can be used in the following modes: • Smart card interface mode • Asynchronous mode (including multi-processor mode) • Clock synchronous mode • Simple SPI mode. Set the SDIR bit to 1 for operation in simple IIC mode.	R/W*1
b4	CHR1	Character Length 1	Valid only in asynchronous mode.*2 Selects the transmit/receive character length in combination with the SMR.CHR bit: CHR1 CHR 0 0: Transmit/receive in 9-bit data length 0 1: Transmit/receive in 9-bit data length 1 0: Transmit/receive in 8-bit data length (initial value) 1 1: Transmit/receive in 7-bit data length.*3	R/W*1
b6, b5	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b7	BCP2	Base Clock Pulse 2	Selects the number of base clock cycles in combination with the SMR_SMCI.BCP[1:0] bits. Table 34.4 lists the combinations of the SCMR.BCP2 and SMR_SMCI.BCP[1:0] bits.	R/W*1

Note 1. Writable only when the TE and RE bits in SCR/SCR_SMCI are 0 (both serial transmission and reception are disabled).
Note 2. The setting is invalid and a fixed data length of 8 bits is used in modes other than asynchronous mode.
Note 3. LSB-first must be selected and the value of the MSB (bit [7]) in TDR cannot be transmitted.

The SCMR register selects the smart card interface and communication format.

SMIF bit (Smart Card Interface Mode Select)

Setting the SMIF bit to 1 selects smart card interface mode. Setting it to 0 selects all other modes:

- Asynchronous mode, including multi-processor mode
- Clock synchronous mode
- Simple SPI mode
- Simple IIC mode.

SINV bit (Transmitted/Received Data Invert)

The SINV bit inverts the transmit and receive data logic level. It does not affect the logic level of the parity bit. To invert the parity bit, invert the PM bit in SMR or SMR_SMCI.

CHR1 bit (Character Length 1)

The CHR1 bit selects the data length of transmit and receive data in combination with the CHR bit in the SMR register. A fixed data length of 8 bits is used in modes other than asynchronous mode.

BCP2 bit (Base Clock Pulse 2)

The BCP2 bit selects the number of base clock cycles in a 1-bit data transfer time in smart card interface mode. Set this bit in combination with the SMR_SMCI.BCP[1:0] bits.

Table 34.4 Combinations of the SCMR.BCP2 and SMR_SMCI.BCP[1:0] bits (1 of 2)

SCMR.BCP2 bit	SMR_SMCI.BCP[1:0] bits	Number of base clock cycles for 1-bit transfer period
0	00	93 clock cycles (S = 93)*1
0	01	128 clock cycles (S = 128)*1
0	10	186 clock cycles (S = 186)*1
0	11	512 clock cycles (S = 512)*1
1	00	32 clock cycles (S = 32)*1 (Initial Value)

Bit	Symbol	位名称	Description	R/W
b3	SDIR	Transmitted/Received Data 转移方向	0：传输LSB-first1：传输MSB-first。SDIR位可用于以下模式： 智能卡接口模式 异步模式（包括多处理器模式）时钟同步模式 简单SPI模式。将SDIR位设置为1以在简单IIC模式下运行。	R/W*1
b4	CHR1	字符长度1	仅在异步模式下有效。*2 结合SMR.CHR位选择发送接收字符长度：CHR1CHR00：以9位数据长度发送接收01：以9位数据长度发送接收10：以8位数据长度发送接收（初始值）11：以7位数据长度发送接收。*3	R/W*1
b6, b5	—	Reserved	这些位被读取为1。写入值应为1。	R/W
b7	BCP2	基本时钟脉冲2	结合SMR_SMCI.BCP[1:0]位选择基本时钟周期数。表34.4列出了SCMR.BCP2和 SMR_SMCI.BCP[1:0] bits.	R/W*1

Note 1. 仅当SCRSCR_SMCI中的TE和RE位为0时可写（串行发送和接收都被禁用）。
Note 2. 该设置无效，并且在非异步模式下使用了固定的8位数据长度。
Note 3. 必须选择LSB优先，并且不能传输TDR中的MSB（位[7]）的值。

SCMR寄存器选择智能卡接口和通信格式。

SMIF位（智能卡接口模式选择）

将SMIF位设置为1选择智能卡接口模式。将其设置为0会选择所有其他模式：

- 异步模式，包括多处理器模式
- 时钟同步模式
- 简单SPI模式
- 简单的IIC模式。

SINV位（发送接收数据反转）

SINV位反转发送和接收数据逻辑电平。它不影响奇偶校验位的逻辑电平。要反转奇偶校验位，请反转SMR或SMR_SMCI中的PM位。

CHR1位（字符长度1）

CHR1位结合SMR寄存器中的CHR位选择发送和接收数据的数据长度。
在异步模式以外的模式中使用8位的固定数据长度。

BCP2位（基本时钟脉冲2）

BCP2位选择智能卡接口模式下1位数据传输时间内的基本时钟周期数。将该位与SMR_SMCI.BCP[1:0]位一起设置。

Table 34.4 SCMR.BCP2和SMR_SMCI.BCP[1:0]位的组合（1of2）

SCMR.BCP2 bit	SMR_SMCI.BCP[1:0] bits	1位传输周期的基本时钟周期数
0	00	93个时钟周期(S=93)*1
0	01	128个时钟周期(S=128)*1
0	10	186个时钟周期(S=186)*1
0	11	512个时钟周期(S=512)*1
1	00	32个时钟周期(S=32)*1（初始值）

Table 34.4 Combinations of the SCMR.BCP2 and SMR_SMCI.BCP[1:0] bits (2 of 2)

SCMR.BCP2 bit	SMR_SMCI.BCP[1:0] bits	Number of base clock cycles for 1-bit transfer period
1	01	64 clock cycles (S = 64)*1
1	10	372 clock cycles (S = 372)*1
1	11	256 clock cycles (S = 256)*1

Note 1. See section 34.2.17, Bit Rate Register (BRR).

34.2.17 Bit Rate Register (BRR)

Address(es): SCI0.BRR 4007 0001h, SCI1.BRR 4007 0021h, SCI2.BRR 4007 0041h, SCI3.BRR 4007 0061h, SCI4.BRR 4007 0081h, SCI5.BRR 4007 00A1h, SCI6.BRR 4007 00C1h, SCI7.BRR 4007 00E1h, SCI8.BRR 4007 0101h, SCI9.BRR 4007 0121h

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1

BRR is an 8-bit register that adjusts the bit rate.

As each SCI channel has independent baud rate generator control, different bit rates can be set for each channel. Table 34.5 shows the relationship between the setting (N) in the BRR and the bit rate (B) for asynchronous mode, multi-processor transfer, clock synchronous mode, smart card interface mode, simple SPI mode, and simple IIC mode.

The initial value of the BRR register is FFh. The BRR register can be read by the CPU, but it can be written to only when the TE and RE bits in SCR/SCR_SMCI are 0.

Table 34.5 Relationship between N setting in BRR and bit rate B

Mode	SEMR settings BGDM bit	SEMR settings ABCS bit	SEMR settings ABCSE bit	BRR setting	Error
Asynchro-nous, multi-processor transfer	0	0	0	$N = \frac{PCLKA \times 10^6}{64 \times 2^{2n-1} \times B} - 1$	$Error\ (\%) = \{\frac{PCLKA \times 10^6}{B \times 64 \times 2^{2n-1} \times (N+1)} - 1\} \times 100$
	1	0	0	$N = \frac{PCLKA \times 10^6}{32 \times 2^{2n-1} \times B} - 1$	$Error\ (\%) = \{\frac{PCLKA \times 10^6}{B \times 32 \times 2^{2n-1} \times (N+1)} - 1\} \times 100$
	0	1	0		
	1	1	0	$N = \frac{PCLKA \times 10^6}{16 \times 2^{2n-1} \times B} - 1$	$Error\ (\%) = \{\frac{PCLKA \times 10^6}{B \times 16 \times 2^{2n-1} \times (N+1)} - 1\} \times 100$
	Don't care	Don't care	1	$N = \frac{PCLKA \times 10^6}{12 \times 2^{2n-1} \times B} - 1$	$Error\ (\%) = \{\frac{PCLKA \times 10^6}{B \times 12 \times 2^{2n-1} \times (N+1)} - 1\} \times 100$
Clock synchronous, simple SPI				$N = \frac{PCLKA \times 10^6}{8 \times 2^{2n-1} \times B} - 1$	-
Smart card interface				$N = \frac{PCLKA \times 10^6}{S \times 2^{2n+1} \times B} - 1$	$Error\ (\%) = \{\frac{PCLKA \times 10^6}{B \times S \times 2^{2n+1} \times (N+1)} - 1\} \times 100$
Simple IIC*1				$N = \frac{PCLKA \times 10^6}{64 \times 2^{2n-1} \times B} - 1$	-

B: Bit rate (bps)
N: BRR setting for on-chip baud rate generator ($0 \le N \le 255$)
PCLKA: Operating frequency (MHz)

Table 34.4 SCMR.BCP2和SMR_SMCI.BCP[1:0]位的组合(2of2)

SCMR.BCP2 bit	SMR_SMCI.BCP[1:0] bits	1位传输周期的基本时钟周期数
1	01	64个时钟周期(S=64)*1
1	10	372个时钟周期(S=372)*1
1	11	256个时钟周期(S=256)*1

Note 1. 请参阅第34.2.17节，比特率寄存器(BRR)。

34.2.17 比特率寄存器(BRR)

Address(es): SCI0.BRR 4007 0001h, SCI1.BRR 4007 0021h, SCI2.BRR 4007 0041h, SCI3.BRR 4007 0061h, SCI4.BRR 4007 0081h, SCI5.BRR 4007 00A1h, SCI6.BRR 4007 00C1h, SCI7.BRR 4007 00E1h, SCI8.BRR 4007 0101h, SCI9.BRR 4007 0121h

	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	1	1	1	1	1	1	1	1

BRR是一个8位寄存器，用于调整比特率。

由于每个SCI通道都有独立的波特率发生器控制，因此可以为每个通道设置不同的比特率。表34.5显示了BRR中的设置(N)与异步模式、多处理器传输、时钟同步模式、智能卡接口模式、简单SPI模式和简单IIC模式的比特率(B)之间的关系。

BRR寄存器的初始值为FFh。BRR寄存器可以被CPU读取，但只有当SCRSCR_SMCI中的TE和RE位为0时才能写入。

Table 34.5 BRR中的N设置与比特率B的关系

Mode	SEMR settings BGDM bit	SEMR settings ABCS 位	SEMR settings ABCSE bit	BRR setting	Error
异步、多处理器传输	0	0	0	$N = \frac{PCLKA \times 10^6}{64 \times 2^{2n-1} \times B} - 1$	$Error\ (\%) = \{\frac{PCLKA \times 10^6}{B \times 64 \times 2^{2n-1} \times (N+1)} - 1\} \times 100$
	1	0	0	$N = \frac{PCLKA \times 10^6}{32 \times 2^{2n-1} \times B} - 1$	$Error\ (\%) = \{\frac{PCLKA \times 10^6}{B \times 32 \times 2^{2n-1} \times (N+1)} - 1\} \times 100$
	0	1	0		
	1	1	0	$N = \frac{PCLKA \times 10^6}{16 \times 2^{2n-1} \times B} - 1$	$Error\ (\%) = \{\frac{PCLKA \times 10^6}{B \times 16 \times 2^{2n-1} \times (N+1)} - 1\} \times 100$
	Don't care	Don't care	1	$N = \frac{PCLKA \times 10^6}{12 \times 2^{2n-1} \times B} - 1$	$Error\ (\%) = \{\frac{PCLKA \times 10^6}{B \times 12 \times 2^{2n-1} \times (N+1)} - 1\} \times 100$
时钟同步，简单的SPI				$N = \frac{PCLKA \times 10^6}{8 \times 2^{2n-1} \times B} - 1$	-
智能卡接口				$N = \frac{PCLKA \times 10^6}{S \times 2^{2n+1} \times B} - 1$	$Error\ (\%) = \{\frac{PCLKA \times 10^6}{B \times S \times 2^{2n+1} \times (N+1)} - 1\} \times 100$
Simple IIC*1				$N = \frac{PCLKA \times 10^6}{64 \times 2^{2n-1} \times B} - 1$	-

B：比特率（bps）
N：片内波特率发生器的BRR设置(0 N 255)
PCLKA：工作频率（MHz）

n and S: Determined by the SMR/SMR_SMCI and SCMR register settings as listed in Table 34.7 and Table 34.8.

Note 1. Adjust the bit rate so that the widths of high and low level of the SCL output in simple IIC mode satisfy the I^2C bus standard.

Table 34.6 Calculating widths of SCL high and low levels

Mode	SCL	Formula (result in seconds)
IIC	Width at high level (minimum value)	$(N+1) \times 4 \times 2^{2n-1} \times 7 \times \frac{1}{PCLKA \times 10^6}$
	Width at low level (minimum value)	$(N+1) \times 4 \times 2^{2n-1} \times 8 \times \frac{1}{PCLKA \times 10^6}$

Table 34.7 Clock source settings

SMR or SMR_SMCI.CKS[1:0] bit setting		
CKS[1:0] bits	Clock source	n
0 0	PCLKA clock	0
0 1	PCLKA/4 clock	1
1 0	PCLKA/16 clock	2
1 1	PCLKA/64 clock	3

Table 34.8 Base clock settings in smart card interface mode

SCMR.BCP2 bit setting	SMR_SMCI.BCP[1:0] bit setting		
BCP2 bit	BCP[1:0] bits	Base clock cycles for 1-bit period	S
0	0 0	93 clock cycles	93
0	0 1	128 clock cycles	128
0	1 0	186 clock cycles	186
0	1 1	512 clock cycles	512
1	0 0	32 clock cycles	32
1	0 1	64 clock cycles	64
1	1 0	372 clock cycles	372
1	1 1	256 clock cycles	256

Table 34.9 and Table 34.10 list examples of BRR (N) settings in asynchronous mode. Table 34.11 lists the maximum bit rate settable for each operating frequency. Table 34.15 lists examples of BRR (N) settings in smart card interface mode.

In smart card interface mode, the number of base clock cycles S in a 1-bit data transfer time can be selected. For details, see section 34.6.4, Receive Data Sampling Timing and Reception Margin. Table 34.12 and Table 34.14 list the maximum bit rates with external clock input.

When either the Asynchronous Mode Base Clock Select bit (ABCS) or the Baud Rate Generator Double-speed Mode Select bit (BGDM) in the Serial Extended Mode Register (SEMR) is set to 1 in asynchronous mode, the bit rate becomes twice the value listed in Table 34.16. When both of those registers are set to 1, the bit rate becomes four times the listed value.

Table 34.9 Examples of BRR settings for different bit rates in asynchronous mode (1) (1 of 2)

Bit rate (bps)	Operating frequency PCLKA (MHz)														
	8			9.8304			10			12			12.288		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	2	141	0.03	2	174	-0.26	2	177	-0.25	2	212	0.03	2	217	0.08

n和S：由表34.7和表34.8中列出的SMRSMR_SMCI和SCMR寄存器设置决定。

注1.调整比特率，使简单IIC模式下SCL输出的高低电平宽度满足I2C总线标准。

Table 34.6 计算SCL高低电平的宽度

Mode	SCL	公式（以秒为单位的结果）
IIC	高电平宽度（最小值）	$(N+1) \times 4 \times 2^{2n-1} \times 7 \times \frac{1}{PCLKA \times 10^6}$
	低电平宽度（最小值）	$(N+1) \times 4 \times 2^{2n-1} \times 8 \times \frac{1}{PCLKA \times 10^6}$

Table 34.7 时钟源设置

SMR或SMR_SMCI.CKS[1:0]位设置		
CKS[1:0] bits	时钟源	n
0 0	PCLKA clock	0
0 1	PCLKA/4 clock	1
1 0	PCLKA/16 clock	2
1 1	PCLKA/64 clock	3

Table 34.8 智能卡接口模式下的基本时钟设置

SCMR.BCP2位设置	SMR_SMCI.BCP[1:0]位设置		
BCP2 bit	BCP[1:0] bits	1位周期的基本时钟周期	S
0	0 0	93个时钟周期	93
0	0 1	128个时钟周期	128
0	1 0	186个时钟周期	186
0	1 1	512个时钟周期	512
1	0 0	32个时钟周期	32
1	0 1	64个时钟周期	64
1	1 0	372个时钟周期	372
1	1 1	256个时钟周期	256

表34.9和表34.10列出了异步模式下的BRR(N)设置示例。表34.11列出了每个工作频率可设置的最大比特率。表34.15列出了智能卡接口模式下的BRR(N)设置示例。

在智能卡接口模式下，可以选择1位数据传输时间内的基本时钟周期数S。有关详细信息，请参阅第34.6.4节，接收数据采样时序和接收余量。表34.12和表34.14列出了外部时钟输入的最大比特率。

当异步模式基本时钟选择位(ABCS)或波特率发生器双速模式
串行扩展模式寄存器(SEMR)中的选择位(BGDM)在异步模式下设置为1，比特率变为表34.16中列出的值的两倍。当这两个寄存器都设置为1时，比特率变为所列值的四倍。

Table 34.9 异步模式下不同比特率的BRR设置示例(1)(1of2)

比特率(bps)	工作频率PCLKA(MHz)														
	8			9.8304			10			12			12.288		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	2	141	0.03	2	174	-0.26	2	177	-0.25	2	212	0.03	2	217	0.08

Table 34.9 Examples of BRR settings for different bit rates in asynchronous mode (1) (2 of 2)

Bit rate (bps)	Operating frequency PCLKA (MHz)														
	8			9.8304			10			12			12.288		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
150	2	103	0.16	2	127	0.00	2	129	0.16	2	155	0.16	2	159	0.00
300	1	207	0.16	1	255	0.00	2	64	0.16	2	77	0.16	2	79	0.00
600	1	103	0.16	1	127	0.00	1	129	0.16	1	155	0.16	1	159	0.00
1200	0	207	0.16	0	255	0.00	1	64	0.16	1	77	0.16	1	79	0.00
2400	0	103	0.16	0	127	0.00	0	129	0.16	0	155	0.16	0	159	0.00
4800	0	51	0.16	0	63	0.00	0	64	0.16	0	77	0.16	0	79	0.00
9600	0	25	0.16	0	31	0.00	0	32	-1.36	0	38	0.16	0	39	0.00
19200	0	12	0.16	0	15	0.00	0	15	1.73	0	19	-2.34	0	19	0.00
31250	0	7	0.00	0	9	-1.70	0	9	0.00	0	11	0.00	0	11	2.40
38400	—	—	—	0	7	0.00	0	7	1.73	0	9	-2.34	0	9	0.00

Bit rate (bps)	Operating frequency PCLKA (MHz)														
	14			16			17.2032			18			19.6608		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	2	248	-0.17	3	70	0.03	3	75	0.48	3	79	-0.12	3	86	0.31
150	2	181	0.16	2	207	0.16	2	223	0.00	2	233	0.16	2	255	0.00
300	2	90	0.16	2	103	0.16	2	111	0.00	2	116	0.16	2	127	0.00
600	1	181	0.16	1	207	0.16	1	223	0.00	1	233	0.16	1	255	0.00
1200	1	90	0.16	1	103	0.16	1	111	0.00	1	116	0.16	1	127	0.00
2400	0	181	0.16	0	207	0.16	0	223	0.00	0	233	0.16	0	255	0.00
4800	0	90	0.16	0	103	0.16	0	111	0.00	0	116	0.16	0	127	0.00
9600	0	45	-0.93	0	51	0.16	0	55	0.00	0	58	-0.69	0	63	0.00
19200	0	22	-0.93	0	25	0.16	0	27	0.00	0	28	1.02	0	31	0.00
31250	0	13	0.00	0	15	0.00	0	16	1.20	0	17	0.00	0	19	-1.70
38400	—	—	—	0	12	0.16	0	13	0.00	0	14	-2.34	0	15	0.00

Note: In this example, SEMR.ABCS = 0, SEMR.ABCSE = 0, and SEMR.BGDM = 0.
When either the ABCS or BGDM bit is set to 1, the bit rate doubles.
When both ABCS and BGDM are set to 1, the bit rate increases four times.

Table 34.10 Examples of BRR settings for different bit rates in asynchronous mode (2)

Bit rate (bps)	Operating frequency PCLKA (MHz)														
	20			25			30			33			40		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	3	88	-0.25	3	110	-0.02	3	132	0.13	3	145	0.33	3	177	-0.25
150	3	64	0.16	3	80	0.47	3	97	-0.35	3	106	0.39	3	129	0.16
300	2	129	0.16	2	162	-0.15	2	194	0.16	2	214	-0.07	3	64	0.16
600	2	64	0.16	2	80	0.47	2	97	-0.35	2	106	0.39	2	129	0.16
1200	1	129	0.16	1	162	-0.15	1	194	0.16	1	214	-0.07	2	64	0.16
2400	1	64	0.16	1	80	0.47	1	97	-0.35	1	106	0.39	1	129	0.16
4800	0	129	0.16	0	162	-0.15	0	194	0.16	0	214	-0.07	1	64	0.16
9600	0	64	0.16	0	80	0.47	0	97	-0.35	0	106	0.39	0	129	0.16
19200	0	32	-1.36	0	40	-0.76	0	48	-0.35	0	53	-0.54	0	64	0.16
31250	0	19	0.00	0	24	0.00	0	29	0.00	0	32	0.00	0	39	0.00
38400	0	15	1.73	0	19	1.73	0	23	1.73	0	26	-0.54	0	32	-1.36

Table 34.9 异步模式下不同比特率的BRR设置示例(1)(2of2)

比特率(bps)	工作频率PCLKA(MHz)														
	8			9.8304			10			12			12.288		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
150	2	103	0.16	2	127	0.00	2	129	0.16	2	155	0.16	2	159	0.00
300	1	207	0.16	1	255	0.00	2	64	0.16	2	77	0.16	2	79	0.00
600	1	103	0.16	1	127	0.00	1	129	0.16	1	155	0.16	1	159	0.00
1200	0	207	0.16	0	255	0.00	1	64	0.16	1	77	0.16	1	79	0.00
2400	0	103	0.16	0	127	0.00	0	129	0.16	0	155	0.16	0	159	0.00
4800	0	51	0.16	0	63	0.00	0	64	0.16	0	77	0.16	0	79	0.00
9600	0	25	0.16	0	31	0.00	0	32	-1.36	0	38	0.16	0	39	0.00
19200	0	12	0.16	0	15	0.00	0	15	1.73	0	19	-2.34	0	19	0.00
31250	0	7	0.00	0	9	-1.70	0	9	0.00	0	11	0.00	0	11	2.40
38400	—	—	—	0	7	0.00	0	7	1.73	0	9	-2.34	0	9	0.00

比特率(bps)	工作频率PCLKA(MHz)														
	14			16			17.2032			18			19.6608		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	2	248	-0.17	3	70	0.03	3	75	0.48	3	79	-0.12	3	86	0.31
150	2	181	0.16	2	207	0.16	2	223	0.00	2	233	0.16	2	255	0.00
300	2	90	0.16	2	103	0.16	2	111	0.00	2	116	0.16	2	127	0.00
600	1	181	0.16	1	207	0.16	1	223	0.00	1	233	0.16	1	255	0.00
1200	1	90	0.16	1	103	0.16	1	111	0.00	1	116	0.16	1	127	0.00
2400	0	181	0.16	0	207	0.16	0	223	0.00	0	233	0.16	0	255	0.00
4800	0	90	0.16	0	103	0.16	0	111	0.00	0	116	0.16	0	127	0.00
9600	0	45	-0.93	0	51	0.16	0	55	0.00	0	58	-0.69	0	63	0.00
19200	0	22	-0.93	0	25	0.16	0	27	0.00	0	28	1.02	0	31	0.00
31250	0	13	0.00	0	15	0.00	0	16	1.20	0	17	0.00	0	19	-1.70
38400	—	—	—	0	12	0.16	0	13	0.00	0	14	-2.34	0	15	0.00

Note: 在此示例中，SEMR.ABCS=0、SEMR.ABCSE=0和SEMR.BGDM=0。
当ABCS或BGDM位设置为1时，比特率加倍。
当ABCS和BGDM都设置为1时，比特率增加四倍。

Table 34.10 异步模式下不同比特率的BRR设置示例（二）

比特率(bps)	工作频率PCLKA(MHz)														
	20			25			30			33			40		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	3	88	-0.25	3	110	-0.02	3	132	0.13	3	145	0.33	3	177	-0.25
150	3	64	0.16	3	80	0.47	3	97	-0.35	3	106	0.39	3	129	0.16
300	2	129	0.16	2	162	-0.15	2	194	0.16	2	214	-0.07	3	64	0.16
600	2	64	0.16	2	80	0.47	2	97	-0.35	2	106	0.39	2	129	0.16
1200	1	129	0.16	1	162	-0.15	1	194	0.16	1	214	-0.07	2	64	0.16
2400	1	64	0.16	1	80	0.47	1	97	-0.35	1	106	0.39	1	129	0.16
4800	0	129	0.16	0	162	-0.15	0	194	0.16	0	214	-0.07	1	64	0.16
9600	0	64	0.16	0	80	0.47	0	97	-0.35	0	106	0.39	0	129	0.16
19200	0	32	-1.36	0	40	-0.76	0	48	-0.35	0	53	-0.54	0	64	0.16
31250	0	19	0.00	0	24	0.00	0	29	0.00	0	32	0.00	0	39	0.00
38400	0	15	1.73	0	19	1.73	0	23	1.73	0	26	-0.54	0	32	-1.36

Bit rate (bps)	Operating frequency PCLKA (MHz)								
	50			60			120		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	3	221	-0.02	—	—	—	—	—	—
150	3	162	-0.15	3	194	0.16	—	—	—
300	3	80	0.47	3	97	-0.35	3	194	0.16
600	2	162	-0.15	3	48	-0.35	3	97	-0.35
1200	2	80	0.47	2	97	-0.35	3	48	-0.35
2400	1	162	-0.15	2	48	-0.35	2	97	-0.35
4800	1	80	0.47	1	97	-0.35	2	48	-0.35
9600	0	162	-0.15	1	48	-0.35	1	97	-0.35
19200	0	80	0.47	0	97	-0.35	1	48	-0.35
31250	0	49	0.00	0	59	0.00	0	119	0
38400	0	40	-0.76	0	48	-0.35	0	97	-0.35

Note: In this example, SEMR.ABCS = 0, SEMR.ABCSE = 0, and SEMR.BGDM = 0.
When either the ABCS or BGDM bit is set to 1, the bit rate doubles.
When both ABCS = 1 and BGDM = 1, the bit rate increases four times.

Table 34.11 Maximum bit rate for each operating frequency in asynchronous mode (1 of 2)

PCLKA (MHz)	SEMR settings					Maximum bit rate (bps)	PCLKA (MHz)	SEMR settings					Maximum bit rate (bps)
	BGDM bit	ABCS bit	ABCSE bit	n	N			BGDM bit	ABCS bit	ABCSE bit	n	N	
8	0	0	0	0	0	250000	16	0	0	0	0	0	500000
		1	0	0	0	500000			1	0	0	0	1000000
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1000000			1	0	0	0	2000000
	Don't care	Don't care	1	0	0	1333333		Don't care	Don't care	1	0	0	2666666
9.8304	0	0	0	0	0	307200	17.2032	0	0	0	0	0	537600
		1	0	0	0	614400			1	0	0	0	1075200
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1228800			1	0	0	0	2150400
	Don't care	Don't care	1	0	0	1638400		Don't care	Don't care	1	0	0	2867200
10	0	0	0	0	0	312500	18	0	0	0	0	0	562500
		1	0	0	0	625000			1	0	0	0	1125000
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1250000			1	0	0	0	2250000
	Don't care	Don't care	1	0	0	1666666		Don't care	Don't care	1	0	0	3000000
12	0	0	0	0	0	375000	19.6608	0	0	0	0	0	614400
		1	0	0	0	750000			1	0	0	0	1228800
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1500000			1	0	0	0	2457600
	Don't care	Don't care	1	0	0	2000000		Don't care	Don't care	1	0	0	3276800

比特率(bps)	工作频率PCLKA(MHz)								
	50			60			120		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
110	3	221	-0.02	—	—	—	—	—	—
150	3	162	-0.15	3	194	0.16	—	—	—
300	3	80	0.47	3	97	-0.35	3	194	0.16
600	2	162	-0.15	3	48	-0.35	3	97	-0.35
1200	2	80	0.47	2	97	-0.35	3	48	-0.35
2400	1	162	-0.15	2	48	-0.35	2	97	-0.35
4800	1	80	0.47	1	97	-0.35	2	48	-0.35
9600	0	162	-0.15	1	48	-0.35	1	97	-0.35
19200	0	80	0.47	0	97	-0.35	1	48	-0.35
31250	0	49	0.00	0	59	0.00	0	119	0
38400	0	40	-0.76	0	48	-0.35	0	97	-0.35

Note: 在此示例中，SEMR.ABCS=0、SEMR.ABCSE=0和SEMR.BGDM=0。
当ABCS或BGDM位设置为1时，比特率加倍。
当ABCS=1和BGDM=1时，比特率增加四倍。

Table 34.11 异步模式下每个工作频率的最大比特率（1of2）

PCLKA (MHz)	SEMR settings					最大比特率(bps)	PCLKA (MHz)	SEMR settings					最大比特率(bps)
	BGDM bit	ABCS 位	ABCSE bit	n	N			BGDM bit	ABCS 位	ABCSE bit	n	N	
8	0	0	0	0	0	250000	16	0	0	0	0	0	500000
		1	0	0	0	500000			1	0	0	0	1000000
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1000000			1	0	0	0	2000000
	Don't care	Don't care	1	0	0	1333333		Don't care	Don't care	1	0	0	2666666
9.8304	0	0	0	0	0	307200	17.2032	0	0	0	0	0	537600
		1	0	0	0	614400			1	0	0	0	1075200
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1228800			1	0	0	0	2150400
	Don't care	Don't care	1	0	0	1638400		Don't care	Don't care	1	0	0	2867200
10	0	0	0	0	0	312500	18	0	0	0	0	0	562500
		1	0	0	0	625000			1	0	0	0	1125000
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1250000			1	0	0	0	2250000
	Don't care	Don't care	1	0	0	1666666		Don't care	Don't care	1	0	0	3000000
12	0	0	0	0	0	375000	19.6608	0	0	0	0	0	614400
		1	0	0	0	750000			1	0	0	0	1228800
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1500000			1	0	0	0	2457600
	Don't care	Don't care	1	0	0	2000000		Don't care	Don't care	1	0	0	3276800

Table 34.11 Maximum bit rate for each operating frequency in asynchronous mode (2 of 2)

PCLKA (MHz)	SEMR settings					Maximum bit rate (bps)	PCLKA (MHz)	SEMR settings					Maximum bit rate (bps)
	BGDM bit	ABCS bit	ABCSE bit	n	N			BGDM bit	ABCS bit	ABCSE bit	n	N	
12.288	0	0	0	0	0	384000	20	0	0	0	0	0	625000
		1	0	0	0	768000			1	0	0	0	1250000
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1536000			1	0	0	0	2500000
	Don't care	Don't care	1	0	0	2048000		Don't care	Don't care	1	0	0	3333333
14	0	0	0	0	0	437500	25	0	0	0	0	0	781250
		1	0	0	0	875000			1	0	0	0	1562500
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1750000			1	0	0	0	3125000
	Don't care	Don't care	1	0	0	2333333		Don't care	Don't care	1	0	0	4166666
30	0	0	0	0	0	937500	50	0	0	0	0	0	1562500
		1	0	0	0	1875000			1	0	0	0	3125000
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	3750000			1	0	0	0	6250000
	Don't care	Don't care	1	0	0	5000000		Don't care	Don't care	1	0	0	8333333
33	0	0	0	0	0	1031250	60	0	0	0	0	0	1875000
		1	0	0	0	2062500			1	0	0	0	3750000
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	4125000			1	0	0	0	7500000
	Don't care	Don't care	1	0	0	5500000		Don't care	Don't care	1	0	0	10000000
40	0	0	0	0	0	1250000	120	0	0	0	0	0	3750000
		1	0	0	0	2500000			1	0	0	0	7500000
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	5000000			1	0	0	0	15000000
	Don't care	Don't care	1	0	0	6666666		Don't care	Don't care	1	0	0	20000000

Table 34.12 Maximum bit rate with external clock input in asynchronous mode (1 of 2)

PCLKA (MHz)	External input clock (MHz)	Maximum bit rate (bps)	
		SEMR.ABCS bit = 0	SEMR.ABCS bit = 1
8	2.0000	125000	250000
9.8304	2.4576	153600	307200
10	2.5000	156250	312500
12	3.0000	187500	375000
12.288	3.0720	192000	384000
14	3.5000	218750	437500
16	4.0000	250000	500000
17.2032	4.3008	268800	537600
18	4.5000	281250	562500
19.6608	4.9152	307200	614400
20	5.0000	312500	625000

Table 34.11 异步模式下每个工作频率的最大比特率（2之2）

PCLKA (MHz)	SEMR settings					最大比特率(bps)	PCLKA (MHz)	SEMR settings					最大比特率(bps)
	BGDM bit	ABCS 位	ABCSE bit	n	N			BGDM bit	ABCS 位	ABCSE bit	n	N	
12.288	0	0	0	0	0	384000	20	0	0	0	0	0	625000
		1	0	0	0	768000			1	0	0	0	1250000
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1536000			1	0	0	0	2500000
	Don't care	Don't care	1	0	0	2048000		Don't care	Don't care	1	0	0	3333333
14	0	0	0	0	0	437500	25	0	0	0	0	0	781250
		1	0	0	0	875000			1	0	0	0	1562500
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	1750000			1	0	0	0	3125000
	Don't care	Don't care	1	0	0	2333333		Don't care	Don't care	1	0	0	4166666
30	0	0	0	0	0	937500	50	0	0	0	0	0	1562500
		1	0	0	0	1875000			1	0	0	0	3125000
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	3750000			1	0	0	0	6250000
	Don't care	Don't care	1	0	0	5000000		Don't care	Don't care	1	0	0	8333333
33	0	0	0	0	0	1031250	60	0	0	0	0	0	1875000
		1	0	0	0	2062500			1	0	0	0	3750000
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	4125000			1	0	0	0	7500000
	Don't care	Don't care	1	0	0	5500000		Don't care	Don't care	1	0	0	10000000
40	0	0	0	0	0	1250000	120	0	0	0	0	0	3750000
		1	0	0	0	2500000			1	0	0	0	7500000
	1	0	0	0	0			1	0	0	0	0	
		1	0	0	0	5000000			1	0	0	0	15000000
	Don't care	Don't care	1	0	0	6666666		Don't care	Don't care	1	0	0	20000000

Table 34.12 异步模式下外部时钟输入的最大比特率（1of2）

PCLKA (MHz)	外部输入时钟(MHz)	最大比特率(bps)	
		SEMR.ABCS bit = 0	SEMR.ABCS bit = 1
8	2.0000	125000	250000
9.8304	2.4576	153600	307200
10	2.5000	156250	312500
12	3.0000	187500	375000
12.288	3.0720	192000	384000
14	3.5000	218750	437500
16	4.0000	250000	500000
17.2032	4.3008	268800	537600
18	4.5000	281250	562500
19.6608	4.9152	307200	614400
20	5.0000	312500	625000

Table 34.12 Maximum bit rate with external clock input in asynchronous mode (2 of 2)

		Maximum bit rate (bps)	
PCLKA (MHz)	External input clock (MHz)	SEMR.ABCS bit = 0	SEMR.ABCS bit = 1
25	6.2500	390625	781250
30	7.5000	468750	937500
33	8.2500	515625	1031250
40	10.0000	625000	1250000
50	12.5000	781250	1562500
60	15.0000	937500	1875000
120	30.0000	1875000	3750000

Table 34.13 BRR settings for different bit rates in clock synchronous and simple SPI modes

Bit rate (bps)	Operating frequency PCLKA (MHz)																					
	8		10		16		20		25		30		33		40		50		60		120	
	n	N	n	N	n	N	n	N	n	N	n	N	n	N	n	N	n	N	n	N	n	N
110																						
250	3	124	—	—	3	249																
500	2	249	—	—	3	124	—	—			3	233										
1 k	2	124	—	—	2	249	—	—	3	97	3	116	3	128	3	155	3	194	3	233		
2.5 k	1	199	1	249	2	99	2	124	2	155	2	187	2	205	2	249	3	77	3	93	3	186
5 k	1	99	1	124	1	199	1	249	2	77	2	93	2	102	2	124	2	155	3	46	3	93
10 k	0	199	0	249	1	99	1	124	1	155	1	187	1	205	1	249	2	77	2	93	3	46
25 k	0	79	0	99	0	159	0	199	0	249	1	74	1	82	1	99	1	124	1	149	2	74
50 k	0	39	0	49	0	79	0	99	0	124	0	149	0	164	1	49	1	61	1	74	1	149
100 k	0	19	0	24	0	39	0	49	0	62	0	74	0	82	0	99	0	124	0	149	1	74
250 k	0	7	0	9	0	15	0	19	0	24	0	29	0	32	0	39	0	49	0	59	1	29
500 k	0	3	0	4	0	7	0	9	—	—	0	14	—	—	0	19	0	24	0	29	1	14
1 M	0	1			0	3	0	4	—	—	—	—	—	—	0	9	—	—	0	14	0	29
2.5 M			0	0*1			0	1	—	—	0	2	—	—	0	3	0	4	0	5	0	11
5 M							0	0*1	—	—	—	—	—	—	0	1	—	—	0	2	0	5
7.5 M											0	0*1							0	1	0	3
10 M															0	0*1					0	2

Space: Setting prohibited.
—: Can be set, but an error occurs.

Note 1. Continuous transmission or reception is not possible. After transmitting or receiving one frame of data, a 1-bit period elapses before starting to transmit or receive the next frame of data. The output of the synchronization clock is stopped for a 1-bit period. Therefore, it takes 9 bits worth of time to transfer one frame (8 bits) of data, and the average transfer rate is 8/9 times the bit rate. When the FIFO is selected, this setting (BRR = 00h and SMR.CKS[1:0] = 00b) is not available.

Table 34.14 Maximum bit rate with external clock input in clock synchronous and simple SPI modes (1 of 2)

PCLKA (MHz)	External input clock (MHz)	Maximum bit rate (Mbps)
8	1.3333	1.3333333
10	1.6667	1.6666667
12	2.0000	2.0000000
14	2.3333	2.3333333
16	2.6667	2.6666667
18	3.0000	3.0000000
20	3.3333	3.3333333

Table 34.12 异步模式下外部时钟输入的最大比特率（2之2）

		最大比特率(bps)	
PCLKA (MHz)	外部输入时钟(MHz)	SEMR.ABCS bit = 0	SEMR.ABCS bit = 1
25	6.2500	390625	781250
30	7.5000	468750	937500
33	8.2500	515625	1031250
40	10.0000	625000	1250000
50	12.5000	781250	1562500
60	15.0000	937500	1875000
120	30.0000	1875000	3750000

Table 34.13 时钟同步和简单SPI模式下不同比特率的BRR设置

比特率(bps)	工作频率PCLKA(MHz)																					
	8		10		16		20		25		30		33		40		50		60		120	
	n	N	n	N	n	N	n	N	n	N	n	N	n	N	n	N	n	N	n	N	n	N
110																						
250	3	124	—	—	3	249																
500	2	249	—	—	3	124	—	—			3	233										
1 k	2	124	—	—	2	249	—	—	3	97	3	116	3	128	3	155	3	194	3	233		
2.5 k	1	199	1	249	2	99	2	124	2	155	2	187	2	205	2	249	3	77	3	93	3	186
5 k	1	99	1	124	1	199	1	249	2	77	2	93	2	102	2	124	2	155	3	46	3	93
10 k	0	199	0	249	1	99	1	124	1	155	1	187	1	205	1	249	2	77	2	93	3	46
25 k	0	79	0	99	0	159	0	199	0	249	1	74	1	82	1	99	1	124	1	149	2	74
50 k	0	39	0	49	0	79	0	99	0	124	0	149	0	164	1	49	1	61	1	74	1	149
100 k	0	19	0	24	0	39	0	49	0	62	0	74	0	82	0	99	0	124	0	149	1	74
250 k	0	7	0	9	0	15	0	19	0	24	0	29	0	32	0	39	0	49	0	59	1	29
500 k	0	3	0	4	0	7	0	9	—	—	0	14	—	—	0	19	0	24	0	29	1	14
1 M	0	1			0	3	0	4	—	—	—	—	—	—	0	9	—	—	0	14	0	29
2.5 M			0	0*1			0	1	—	—	0	2	—	—	0	3	0	4	0	5	0	11
5 M							0	0*1	—	—	—	—	—	—	0	1	—	—	0	2	0	5
7.5 M											0	0*1							0	1	0	3
10 M															0	0*1					0	2

空格：禁止设置。—：可以设置，
但发生错误。

Note 1. 无法连续发送或接收。在发送或接收一帧数据后，在开始发送或接收下一帧数据之前会经过1位周期。同步时钟的输出停止1位周期。因此，传输一帧（8位）数据需要9位的时间，平均传输速率为89倍的位速率。选择FIFO时，此设置（BRR=00h且SMR.CKS[1:0]=00b）不可用。

Table 34.14 时钟同步和简单SPI模式下外部时钟输入的最大比特率（1of2）

PCLKA (MHz)	外部输入时钟(MHz)	最大比特率(Mbps)
8	1.3333	1.3333333
10	1.6667	1.6666667
12	2.0000	2.0000000
14	2.3333	2.3333333
16	2.6667	2.6666667
18	3.0000	3.0000000
20	3.3333	3.3333333

Table 34.14 Maximum bit rate with external clock input in clock synchronous and simple SPI modes (2 of 2)

PCLKA (MHz)	External input clock (MHz)	Maximum bit rate (Mbps)
25	4.1667	4.1666667
30	5.0000	5.0000000
33	5.5000	5.5000000
40	6.6667	6.6666667
50	8.3333	8.3333333
60	10.0000	10.0000000
120	20.0000 (clock synchronous mode)	20.00000000
	10.0000 (simple SPI mode)	10.00000000

Table 34.15 BRR settings for different bit rates in smart card interface mode (n = 0, S = 372)

	Operating frequency PCLKA (MHz)											
	7.1424			10.00			10.7136			13.00		
Bit rate (bps)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
9600	0	0	0.00	0	1	-30	0	1	-25	0	1	-8.99

	Operating frequency PCLKA (MHz)											
	14.2848			16.00			18.00			20.00		
Bit rate (bps)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
9600	0	1	0.00	0	1	12.01	0	2	-15.99	0	2	-6.66

	Operating frequency PCLKA (MHz)											
	25.00			30.00			33.00			40.00		
Bit rate (bps)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
9600	0	3	-12.49	0	3	5.01	0	4	-7.59	0	5	-6.66

	Operating frequency PCLKA (MHz)								
	50.00			60.00			120.00		
Bit rate (bps)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
9600	0	6	0.01	0	7	5.01	0	16	-1.17

Table 34.16 Maximum bit rate for each operating frequency in smart card interface mode (S = 32)

PCLKA (MHz)	Maximum bit rate (bps)	n	N
10.00	156250	0	0
10.7136	167400	0	0
13.00	203125	0	0
16.00	250000	0	0
18.00	281250	0	0
20.00	312500	0	0
25.00	390625	0	0
30.00	468750	0	0
33.00	515625	0	0
40.00	625000	0	0
50.00	781250	0	0
60.00	937500	0	0
120.00	1875000	0	0

Table 34.14 时钟同步和简单SPI模式下外部时钟输入的最大比特率(2of2)

PCLKA (MHz)	外部输入时钟(MHz)	最大比特率(Mbps)
25	4.1667	4.1666667
30	5.0000	5.0000000
33	5.5000	5.5000000
40	6.6667	6.6666667
50	8.3333	8.3333333
60	10.0000	10.0000000
120	20.0000 (clock synchronous mode)	20.00000000
	10.0000 (simple SPI mode)	10.00000000

Table 34.15 智能卡接口模式下不同比特率的BRR设置（n=0，S=372）

	工作频率PCLKA(MHz)											
	7.1424			10.00			10.7136			13.00		
比特率(bps)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
9600	0	0	0.00	0	1	-30	0	1	-25	0	1	-8.99

	工作频率PCLKA(MHz)											
	14.2848			16.00			18.00			20.00		
比特率(bps)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
9600	0	1	0.00	0	1	12.01	0	2	-15.99	0	2	-6.66

	工作频率PCLKA(MHz)											
	25.00			30.00			33.00			40.00		
比特率(bps)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
9600	0	3	-12.49	0	3	5.01	0	4	-7.59	0	5	-6.66

	工作频率PCLKA(MHz)								
	50.00			60.00			120.00		
比特率(bps)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
9600	0	6	0.01	0	7	5.01	0	16	-1.17

Table 34.16 智能卡接口模式下每个工作频率的最大比特率(S=32)

PCLKA (MHz)	最大比特率(bps)	n	N
10.00	156250	0	0
10.7136	167400	0	0
13.00	203125	0	0
16.00	250000	0	0
18.00	281250	0	0
20.00	312500	0	0
25.00	390625	0	0
30.00	468750	0	0
33.00	515625	0	0
40.00	625000	0	0
50.00	781250	0	0
60.00	937500	0	0
120.00	1875000	0	0

Table 34.17 BRR settings for different bit rates in simple IIC mode

Bit rate (bps)	Operating frequency PCLKA (MHz)														
	8			10			16			20			25		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
10 k	0	24	0.0	0	30	0.8	1	12	-3.8	1	15	-2.3	1	19	-2.3
25 k	0	9	0.0	0	12	-3.8	1	4	0.0	1	5	428	1	7	-2.3
50 k	0	4	0.0	0	5	4.2	1	2	-16.7	1	2	4.2	1	3	-2.3
100 k*1	0	2	-16.7	0	3	-21.9	0	4	0.0	0	6	-10.7	1	1	-2.3
250 k	0	0	0.0	0	0	25	0	1	0.0	0	2	-16.7	0	2	4.2
350 k										0	1	-10.7	0	1	11.6*2
400 k*1										0	1	-21.9	0	1	-2.3*2

Bit rate (bps)	Operating frequency PCLKA (MHz)														
	30			33			40			50			60		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
10 k	1	22	1.9	1	25	-0.8	0	124	0.0	2	9	-2.3	1	46	-0.3
25 k	1	8	4.2	1	9	3.1	0	49	0.0	2	3	-2.3	0	74	0.0
50 k	1	4	-6.3	1	4	3.1	0	24	0.0	2	1	-2.3	0	37	-1.3
100 k*1	1	2	-21.9	1	2	-14.1	0	12	-3.9	1	3	-2.3	0	18	-1.3
250 k	0	3	-6.3	0	3	3.1	0	4	0.0	0	5	4.2	0	7	-6.3
350 k	0	2	-10.7	0	2	-1.8	0	3	-10.7	0	4	-10.7	0	4	7.1
400 k*1	0	2	-21.9	0	2	-14.1	0	3	-21.9	0	3	-2.3*2	0	4	-6.3

Bit rate (bps)	Operating frequency PCLKA (MHz)		
	120		
	n	N	Error (%)
10 k	1	93	-0.3
25 k	0	149	0.0
50 k	0	74	0.0
100 k*1	0	37	-1.3
250 k	0	14	0.0
350 k	0	10	-2.6
400 k*1	0	9	-6.3

Note 1. The bit rate of 100 kbps and 400 kbps indicates the set value at which the error is on the minus side.
Note 2. The minimum value of low width is smaller than 1.3 μs which is the standard value of fast mode.

Table 34.18 Minimum widths at SCL high and low levels for different bit rates in simple IIC mode (1 of 2)

Bit rate (bps)	Operating frequency PCLKA (MHz)											
	8			10			16			20		
	n	N	Minimum widths at SCL high/low levels (μs)	n	N	Minimum widths at SCL high/low levels (μs)	n	N	Minimum widths at SCL high/low levels (μs)	n	N	Minimum widths at SCL high/low levels (μs)
10 k	0	24	43.75/50.00	0	30	43.40/49.60	1	12	45.5/52.00	1	15	44.80/51.20
25 k	0	9	17.50/20.00	0	12	18.2/20.80	1	4	17.50/20.00	1	5	16.80/19.20
50 k	0	4	8.75/10.00	0	5	8.40/9.60	1	2	10.50/12.00	1	2	8.40/9.60
100 k	0	2	5.25/6.00	0	3	5.60/6.40	0	4	4.38/5.00	0	6	4.90/5.60

Table 34.17 简单IIC模式下不同比特率的BRR设置

比特率(bps)	工作频率PCLKA(MHz)														
	8			10			16			20			25		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
10 k	0	24	0.0	0	30	0.8	1	12	-3.8	1	15	-2.3	1	19	-2.3
25 k	0	9	0.0	0	12	-3.8	1	4	0.0	1	5	428	1	7	-2.3
50 k	0	4	0.0	0	5	4.2	1	2	-16.7	1	2	4.2	1	3	-2.3
100 k*1	0	2	-16.7	0	3	-21.9	0	4	0.0	0	6	-10.7	1	1	-2.3
250 k	0	0	0.0	0	0	25	0	1	0.0	0	2	-16.7	0	2	4.2
350 k										0	1	-10.7	0	1	11.6*2
400 k*1										0	1	-21.9	0	1	-2.3*2

比特率(bps)	工作频率PCLKA(MHz)														
	30			33			40			50			60		
	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)	n	N	Error (%)
10 k	1	22	1.9	1	25	-0.8	0	124	0.0	2	9	-2.3	1	46	-0.3
25 k	1	8	4.2	1	9	3.1	0	49	0.0	2	3	-2.3	0	74	0.0
50 k	1	4	-6.3	1	4	3.1	0	24	0.0	2	1	-2.3	0	37	-1.3
100 k*1	1	2	-21.9	1	2	-14.1	0	12	-3.9	1	3	-2.3	0	18	-1.3
250 k	0	3	-6.3	0	3	3.1	0	4	0.0	0	5	4.2	0	7	-6.3
350 k	0	2	-10.7	0	2	-1.8	0	3	-10.7	0	4	-10.7	0	4	7.1
400 k*1	0	2	-21.9	0	2	-14.1	0	3	-21.9	0	3	-2.3*2	0	4	-6.3

比特率(bps)	工作频率 PCLKA (MHz)		
	120		
	n	N	Error (%)
10 k	1	93	-0.3
25 k	0	149	0.0
50 k	0	74	0.0
100 k*1	0	37	-1.3
250 k	0	14	0.0
350 k	0	10	-2.6
400 k*1	0	9	-6.3

Note 1. 100kbps和400kbps的比特率表示错误在负侧的设定值。
Note 2. 低宽度的最小值小于1.3微秒，这是快速模式的标准值。

Table 34.18 简单IIC模式下不同比特率的SCL高电平和低电平的最小宽度（1of2）

比特率(bps)	工作频率PCLKA(MHz)											
	8			10			16			20		
	n	N	SCL高低电平的最小宽度(μs)	n	N	SCL高低电平的最小宽度(μs)	n	N	SCL高低电平的最小宽度(μs)	n	N	SCL高低电平的最小宽度(μs)
10 k	0	24	43.75/50.00	0	30	43.40/49.60	1	12	45.5/52.00	1	15	44.80/51.20
25 k	0	9	17.50/20.00	0	12	18.2/20.80	1	4	17.50/20.00	1	5	16.80/19.20
50 k	0	4	8.75/10.00	0	5	8.40/9.60	1	2	10.50/12.00	1	2	8.40/9.60
100 k	0	2	5.25/6.00	0	3	5.60/6.40	0	4	4.38/5.00	0	6	4.90/5.60

Table 34.18 Minimum widths at SCL high and low levels for different bit rates in simple IIC mode (2 of 2)

Bit rate (bps)	Operating frequency PCLKA (MHz)											
	8			10			16			20		
	n	N	Minimum widths at SCL high/low levels (µs)	n	N	Minimum widths at SCL high/low levels (µs)	n	N	Minimum widths at SCL high/low levels (µs)	n	N	Minimum widths at SCL high/low levels (µs)
250 k	0	0	1.75/2.00	0	0	1.40/1.60	0	1	1.75/2.00	0	2	2.10/2.40
350 k										0	1	1.40/1.60
400 k										0	1	1.40/1.60

Bit rate (bps)	Operating frequency PCLKA (MHz)											
	25			30			33			40		
	n	N	Minimum widths at SCL high/low levels (µs)	n	N	Minimum widths at SCL high/low levels (µs)	n	N	Minimum widths at SCL high/low levels (µs)	n	N	Minimum widths at SCL high/low levels (µs)
10 k	1	19	44.80/51.20	1	22	42.93/49.60	1	25	44.12/50.42	0	124	43.75/50.00
25 k	1	7	17.92/20.48	1	8	16.80/19.20	1	9	16.97/19.39	0	49	17.50/20.00
50 k	1	3	8.96/10.24	1	4	9.33/10.66	1	4	8.48/9.70	0	24	8.75/10.00
100 k	1	1	4.48/5.12	1	2	5.60/6.40	1	2	5.09/5.82	0	12	4.55/5.20
250 k	0	2	1.68/1.92	0	3	1.86/2.13	0	3	1.70/1.94	0	4	1.75/2.00
350 k	0	1	1.12/1.28*1	0	2	1.40/1.60	0	2	1.27/1.45	0	3	1.40/1.60
400 k	0	1	1.12/1.28*1	0	2	1.40/1.60	0	2	1.27 /1.45	0	3	1.40/1.60

Bit rate (bps)	Operating frequency PCLKA (MHz)								
	50			60			120		
	n	N	Minimum widths at SCL high/low levels (µs)	n	N	Minimum widths at SCL high/low levels (µs)	n	N	Minimum widths at SCL high/low levels (µs)
10 k	2	9	44.80/51.20	1	46	43.87/50.13	1	93	43.87/50.13
25 k	2	3	17.92/20.48	0	74	17.50/20.00	0	149	17.50/20.00
50 k	2	1	8.96/10.24	0	37	8.87/10.13	0	74	8.75/10.00
100 k	1	3	4.48/5.12	0	18	4.43/5.07	0	37	4.43/5.07
250 k	0	5	1.68/1.92	0	7	1.87/2.13	0	14	1.75/2.00
350 k	0	4	1.40/1.60	0	4	1.17/1.33	0	10	1.28/1.47
400 k	0	3	1.12/1.28*1	0	4	1.17/1.33	0	8	1.05/1.20

Note 1. The minimum value of low width is smaller than 1.3 µs which is the standard value of fast mode. The setting values are the same as in Table 34.17.

34.2.18 Modulation Duty Register (MDDR)

Address(es): SCI0.MDDR 4007 0012h, SCI1.MDDR 4007 0032h, SCI2.MDDR 4007 0052h, SCI3.MDDR 4007 0072h, SCI4.MDDR 4007 0092h, SCI5.MDDR 4007 00B2h, SCI6.MDDR 4007 00D2h, SCI7.MDDR 4007 00F2h, SCI8.MDDR 4007 0112h, SCI9.MDDR 4007 0132h

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1

The MDDR register corrects the bit rate adjusted by the BRR register.

When the SEMR.BRME bit is set to 1, the bit rate generated by the on-chip baud rate generator is evenly corrected using the settings in the MDDR register (M/256). Table 34.19 shows the relationship between the MDDR setting (M) and the

Table 34.18 简单IIC模式下不同比特率的SCL高电平和低电平的最小宽度(2of2)

比特率(bps)	工作频率PCLKA(MHz)											
	8			10			16			20		
	n	N	SCL高低电平的最小宽度(µs)	n	N	SCL高低电平的最小宽度(µs)	n	N	SCL高低电平的最小宽度(µs)	n	N	SCL高低电平的最小宽度(µs)
250 k	0	0	1.75/2.00	0	0	1.40/1.60	0	1	1.75/2.00	0	2	2.10/2.40
350 k										0	1	1.40/1.60
400 k										0	1	1.40/1.60

比特率(bps)	工作频率PCLKA(MHz)											
	25			30			33			40		
	n	N	SCL高低电平的最小宽度(µs)	n	N	SCL高低电平的最小宽度(µs)	n	N	SCL高低电平的最小宽度(µs)	n	N	SCL高低电平的最小宽度(µs)
10 k	1	19	44.80/51.20	1	22	42.93/49.60	1	25	44.12/50.42	0	124	43.75/50.00
25 k	1	7	17.92/20.48	1	8	16.80/19.20	1	9	16.97/19.39	0	49	17.50/20.00
50 k	1	3	8.96/10.24	1	4	9.33/10.66	1	4	8.48/9.70	0	24	8.75/10.00
100 k	1	1	4.48/5.12	1	2	5.60/6.40	1	2	5.09/5.82	0	12	4.55/5.20
250 k	0	2	1.68/1.92	0	3	1.86/2.13	0	3	1.70/1.94	0	4	1.75/2.00
350 k	0	1	1.12/1.28*1	0	2	1.40/1.60	0	2	1.27/1.45	0	3	1.40/1.60
400 k	0	1	1.12/1.28*1	0	2	1.40/1.60	0	2	1.27 /1.45	0	3	1.40/1.60

比特率(bps)	工作频率PCLKA(MHz)								
	50			60			120		
	n	N	SCL高低电平的最小宽度(µs)	n	N	SCL高低电平的最小宽度(µs)	n	N	SCL高低电平的最小宽度(µs)
10 k	2	9	44.80/51.20	1	46	43.87/50.13	1	93	43.87/50.13
25 k	2	3	17.92/20.48	0	74	17.50/20.00	0	149	17.50/20.00
50 k	2	1	8.96/10.24	0	37	8.87/10.13	0	74	8.75/10.00
100 k	1	3	4.48/5.12	0	18	4.43/5.07	0	37	4.43/5.07
250 k	0	5	1.68/1.92	0	7	1.87/2.13	0	14	1.75/2.00
350 k	0	4	1.40/1.60	0	4	1.17/1.33	0	10	1.28/1.47
400 k	0	3	1.12/1.28*1	0	4	1.17/1.33	0	8	1.05/1.20

Note 1. 低宽度的最小值小于1.3微秒，这是快速模式的标准值。设定值与表34.17相同。

34.2.18 调制占空比寄存器(MDDR)

Address(es): SCI0.MDDR 4007 0012h, SCI1.MDDR 4007 0032h, SCI2.MDDR 4007 0052h, SCI3.MDDR 4007 0072h, SCI4.MDDR 4007 0092h, SCI5.MDDR 4007 00B2h, SCI6.MDDR 4007 00D2h, SCI7.MDDR 4007 00F2h, SCI8.MDDR 4007 0112h, SCI9.MDDR 4007 0132h

	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值:	1	1	1	1	1	1	1	1

MDDR寄存器校正由BRR寄存器调整的比特率。

当SEMR.BRME位设置为1时，片上波特率发生器生成的比特率使用MDDR寄存器(M256)中的设置进行均匀校正。表34.19显示了MDDR设置(M)和

bit rate (B).

The initial value of the MDDR register is FFh. Bit [7] in this register is fixed to 1. The CPU can read the MDDR register, but the MDDR register is only writable when the TE and RE bits in SCR/SCR_SMCI are 0.

Table 34.19 Relationship between MDDR setting (M) and bit rate (B) when bit rate modulation function is used

Mode	SEMR settings BGDM bit	SEMR settings ABCS bit	SEMR settings ABCSE bit	BRR setting	Error
Asynchronous, multi-processor transfer	0	0	0	$N = \frac{PCLKA \times 10^6}{64 \times 2^{2n-1} \times (256/M) \times B} - 1$	$Error\ (\%) = \{\frac{PCLKA \times 10^6}{B \times 64 \times 2^{2n-1} \times (256/M) \times (N+1)} - 1\} \times 100$
	1	0	0	$N = \frac{PCLKA \times 10^6}{32 \times 2^{2n-1} \times (256/M) \times B} - 1$	$Error\ (\%) = \{\frac{PCLKA \times 10^6}{B \times 32 \times 2^{2n-1} \times (256/M) \times (N+1)} - 1\} \times 100$
	0	1	0		
	1	1	0	$N = \frac{PCLKA \times 10^6}{16 \times 2^{2n-1} \times (256/M) \times B} - 1$	$Error\ (\%) = \{\frac{PCLKA \times 10^6}{B \times 16 \times 2^{2n-1} \times (256/M) \times (N+1)} - 1\} \times 100$
	Don't care	Don't care	1	$N = \frac{PCLKA \times 10^6}{12 \times 2^{2n-1} \times (256/M) \times B} - 1$	$Error\ (\%) = \{\frac{PCLKA \times 10^6}{B \times 12 \times 2^{2n-1} \times (256/M) \times (N+1)} - 1\} \times 100$
Clock synchronous, simple SPI*1				$N = \frac{PCLKA \times 10^6}{8 \times 2^{2n-1} \times (256/M) \times B} - 1$	—
Smart card interface				$N = \frac{PCLKA \times 10^6}{S \times 2^{2n+1} \times (256/M) \times B} - 1$	$Error\ (\%) = \{\frac{PCLKA \times 10^6}{B \times S \times 2^{2n+1} \times (256/M) \times (N+1)} - 1\} \times 100$
Simple IIC*2				$N = \frac{PCLKA \times 10^6}{64 \times 2^{2n-1} \times (256/M) \times B} - 1$	—

B: Bit rate (bps)
M: MDDR setting (128 ≤ MDDR ≤ 255)
N: BRR setting for baud rate generator (0 ≤ N ≤ 255)
PCLKA: Operating frequency (MHz)
n and S: Determined by the SMR/SMR_SMCI and SCMR register settings as listed in Table 34.7 and Table 34.8 in section 34, Bit Rate Register (BRR).

Note 1. Do not use this function in clock synchronous mode or in the highest speed settings in simple SPI mode (SMR.CKS[1:0] = 00b, SCR.CKE[1] = 0, and BRR = 0).
Note 2. Adjust the bit rate so that the widths of high and low level of the SCL output in simple IIC mode satisfy the I^2C bus standard.

Table 34.20 and Table 34.21 list examples of N settings in BRR and M settings in MDDR in asynchronous mode.

Table 34.20 Examples of BRR and MDDR settings for multiple bit rates in asynchronous mode (1)

Bit rate (bps)	Operating frequency PCLKA (MHz) 8 n	N	M	BGDM bit	Error (%)	9.8304 n	N	M	BGDM bit	Error (%)	16 n	N	M	BGDM bit	Error (%)
38400	0	5	236	0	0.03	0	7	(256)*1	0	0.00	0	10	173	1	-0.01
57600	0	3	236	0	0.03	0	4	240	0	0.00	0	4	236	0	0.03
115200	0	1	236	0	0.03	0	1	192	0	0.00	0	4	236	1	0.03
230400	0	0	236	0	0.03	0	0	192	0	0.00	0	1	189	1	0.14
460800	0	0	236	1	0.03	0	0	192	1	0.00	0	0	189	1	0.14

比特率(B)。

MDDR寄存器的初始值为FFh。该寄存器中的Bit[7]固定为1。CPU可以读取MDDR寄存器，但MDDR寄存器只有在SCRSCR_SMCI中的TE和RE位为0时才可写。

Table 34.19 使用比特率调制功能时MDDR设置(M)和比特率(B)的关系

Mode	SEMR settings BGDM bit	SEMR settings ABCS位	SEMR settings ABCSE bit	BRR setting	Error
异步、多处理器传输	0	0	0	$N = \frac{PCLKA \times 10^6}{64 \times 2^{2n-1} \times (256/M) \times B} - 1$	$Error\ (\%) = \{\frac{PCLKA \times 10^6}{B \times 64 \times 2^{2n-1} \times (256/M) \times (N+1)} - 1\} \times 100$
	1	0	0	$N = \frac{PCLKA \times 10^6}{32 \times 2^{2n-1} \times (256/M) \times B} - 1$	$Error\ (\%) = \{\frac{PCLKA \times 10^6}{B \times 32 \times 2^{2n-1} \times (256/M) \times (N+1)} - 1\} \times 100$
	0	1	0		
	1	1	0	$N = \frac{PCLKA \times 10^6}{16 \times 2^{2n-1} \times (256/M) \times B} - 1$	$Error\ (\%) = \{\frac{PCLKA \times 10^6}{B \times 16 \times 2^{2n-1} \times (256/M) \times (N+1)} - 1\} \times 100$
	Don't care	Don't care	1	$N = \frac{PCLKA \times 10^6}{12 \times 2^{2n-1} \times (256/M) \times B} - 1$	$Error\ (\%) = \{\frac{PCLKA \times 10^6}{B \times 12 \times 2^{2n-1} \times (256/M) \times (N+1)} - 1\} \times 100$
时钟同步，简单SPI*1				$N = \frac{PCLKA \times 10^6}{8 \times 2^{2n-1} \times (256/M) \times B} - 1$	—
智能卡接口				$N = \frac{PCLKA \times 10^6}{S \times 2^{2n+1} \times (256/M) \times B} - 1$	$Error\ (\%) = \{\frac{PCLKA \times 10^6}{B \times S \times 2^{2n+1} \times (256/M) \times (N+1)} - 1\} \times 100$
Simple IIC*2				$N = \frac{PCLKA \times 10^6}{64 \times 2^{2n-1} \times (256/M) \times B} - 1$	—

B：比特率（bps）
M: MDDR setting (128 ≤ MDDR ≤ 255)
N：波特率发生器的BRR设置（0≤N≤255）
PCLKA：工作频率(MHz)n和S：由SMRSMR_SMCI和SCMR寄存器设置决定，如第34节，比特率寄存器(BRR)中的表34.7和表34.8中所列。

Note 1. 请勿在时钟同步模式或简单SPI模式的最高速度设置中使用此功能（SMR.CKS[1:0]=00b，SCR.CKE[1] = 0, and BRR = 0).
Note 2. 调整码率，使简单IIC模式下SCL输出的高低电平宽度满足I2C总线标准。

表34.20和表34.21列出了异步模式下BRR中的N设置和MDDR中的M设置的示例。

Table 34.20 异步模式下多比特率的BRR和MDDR设置示例(1)

比特率(bps)	工作频率PCLKA(MHz) 8 n	N	M	BGDM bit	Error (%)	9.8304 n	N	M	BGDM bit	Error (%)	16 n	N	M	BGDM bit	Error (%)
38400	0	5	236	0	0.03	0	7	(256)*1	0	0.00	0	10	173	1	-0.01
57600	0	3	236	0	0.03	0	4	240	0	0.00	0	4	236	0	0.03
115200	0	1	236	0	0.03	0	1	192	0	0.00	0	4	236	1	0.03
230400	0	0	236	0	0.03	0	0	192	0	0.00	0	1	189	1	0.14
460800	0	0	236	1	0.03	0	0	192	1	0.00	0	0	189	1	0.14

Bit rate (bps)	Operating frequency PCLKA (MHz)														
	12					12.288					14				
	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)
38400	0	8	236	0	0.03	0	9	(256)*1	0	0.00	0	16	191	1	0.00
57600	0	5	236	0	0.03	0	4	192	0	0.00	0	13	236	1	0.03
115200	0	2	236	0	0.03	0	4	192	1	0.00	0	6	236	1	0.03
230400	0	2	236	1	0.03	0	2	230	1	-0.17	0	2	202	1	-0.11
460800	0	0	157	1	-0.18	0	0	154	1	-0.26	0	0	135	1	0.14

Bit rate (bps)	Operating frequency PCLKA (MHz)														
	16					17.2032					18				
	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)
38400	0	11	236	0	0.03	0	13	(256)*1	0	0.00	0	18	166	1	-0.01
57600	0	7	236	0	0.03	0	6	192	0	0.00	0	18	249	1	-0.01
115200	0	3	236	0	0.03	0	6	192	1	0.00	0	8	236	1	0.03
230400	0	1	236	0	0.03	0	3	219	1	-0.20	0	1	210	0	0.14
460800	0	1	236	1	0.03	0	1	219	1	-0.20	0	0	210	0	0.14

Note 1. In this example, the ABCS and ABCSE bits in the SEMR register are 0. SEMR.BRME = 0 (M = 256) disables the bit rate modulation function.

Table 34.21 Examples of BRR and MDDR settings for different bit rates in asynchronous mode (2)

Bit rate (bps)	Operating frequency PCLKA (MHz)														
	19.6608					20					25				
	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)
38400	0	15	(256)*1	0	0.00	0	10	173	0	-0.01	0	11	151	0	0.00
57600	0	9	240	0	0.00	0	9	236	0	0.03	0	7	151	0	0.00
115200	0	4	240	0	0.00	0	4	236	0	0.03	0	3	151	0	0.00
230400	0	1	192	0	0.00	0	4	236	1	0.03	0	1	151	0	0.00
460800	0	0	192	0	0.00	0	0	189	0	0.14	0	0	151	0	0.00

Bit rate (bps)	Operating frequency PCLKA (MHz)														
	30					33					40				
	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)
38400	0	36	194	1	0.01	0	14	143	0	0.01	0	21	173	0	-0.01
57600	0	10	173	0	-0.01	0	9	143	0	0.01	0	38	230	1	-0.01
115200	0	10	173	1	-0.01	0	4	143	0	0.01	0	9	236	0	0.03
230400	0	6	220	1	-0.09	0	4	143	1	0.01	0	4	236	0	0.03
460800	0	3	252	1	0.14	0	1	229	0	0.10	0	4	236	1	0.03

Bit rate (bps)	Operating frequency PCLKA (MHz)														
	50					60					120				
	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)
38400	0	23	151	0	0.00	0	36	194	0	0.01	0	73	194	0	0.01
57600	0	15	151	0	0.00	0	21	173	0	-0.01	0	58	232	0	0.00
115200	0	7	151	0	0.00	0	10	173	0	-0.01	0	21	173	0	-0.01

比特率(bps)	工作频率PCLKA(MHz)														
	12					12.288					14				
	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)
38400	0	8	236	0	0.03	0	9	(256)*1	0	0.00	0	16	191	1	0.00
57600	0	5	236	0	0.03	0	4	192	0	0.00	0	13	236	1	0.03
115200	0	2	236	0	0.03	0	4	192	1	0.00	0	6	236	1	0.03
230400	0	2	236	1	0.03	0	2	230	1	-0.17	0	2	202	1	-0.11
460800	0	0	157	1	-0.18	0	0	154	1	-0.26	0	0	135	1	0.14

比特率(bps)	工作频率PCLKA(MHz)														
	16					17.2032					18				
	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)
38400	0	11	236	0	0.03	0	13	(256)*1	0	0.00	0	18	166	1	-0.01
57600	0	7	236	0	0.03	0	6	192	0	0.00	0	18	249	1	-0.01
115200	0	3	236	0	0.03	0	6	192	1	0.00	0	8	236	1	0.03
230400	0	1	236	0	0.03	0	3	219	1	-0.20	0	1	210	0	0.14
460800	0	1	236	1	0.03	0	1	219	1	-0.20	0	0	210	0	0.14

Note 1. 在本例中，SEMR寄存器中的ABCS和ABCSE位为0。SEMR.BRME=0(M=256)禁用比特率调制功能。

Table 34.21 异步模式下不同比特率的BRR和MDDR设置示例(2)

比特率(bps)	工作频率PCLKA(MHz)														
	19.6608					20					25				
	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)
38400	0	15	(256)*1	0	0.00	0	10	173	0	-0.01	0	11	151	0	0.00
57600	0	9	240	0	0.00	0	9	236	0	0.03	0	7	151	0	0.00
115200	0	4	240	0	0.00	0	4	236	0	0.03	0	3	151	0	0.00
230400	0	1	192	0	0.00	0	4	236	1	0.03	0	1	151	0	0.00
460800	0	0	192	0	0.00	0	0	189	0	0.14	0	0	151	0	0.00

比特率(bps)	工作频率PCLKA(MHz)														
	30					33					40				
	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)
38400	0	36	194	1	0.01	0	14	143	0	0.01	0	21	173	0	-0.01
57600	0	10	173	0	-0.01	0	9	143	0	0.01	0	38	230	1	-0.01
115200	0	10	173	1	-0.01	0	4	143	0	0.01	0	9	236	0	0.03
230400	0	6	220	1	-0.09	0	4	143	1	0.01	0	4	236	0	0.03
460800	0	3	252	1	0.14	0	1	229	0	0.10	0	4	236	1	0.03

比特率(bps)	工作频率PCLKA(MHz)														
	50					60					120				
	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)
38400	0	23	151	0	0.00	0	36	194	0	0.01	0	73	194	0	0.01
57600	0	15	151	0	0.00	0	21	173	0	-0.01	0	58	232	0	0.00
115200	0	7	151	0	0.00	0	10	173	0	-0.01	0	21	173	0	-0.01

Bit rate (bps)	Operating frequency PCLKA (MHz)														
	50					60					120				
	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)
230400	0	3	151	0	0.00	0	10	173	1	-0.01	0	10	173	0	-0.01
460800	0	1	151	0	0.00	0	6	220	1	-0.09	0	10	173	1	-0.09

Note 1. In this example, the ABCS and ABCSE bits in the SEMR register are 0. SEMR.BRME = 0 (M = 256) disables the bit rate modulation function.

34.2.19 Serial Extended Mode Register (SEMR)

Address(es): SCI0.SEMR 4007 0007h, SCI1.SEMR 4007 0027h, SCI2.SEMR 4007 0047h, SCI3.SEMR 4007 0067h, SCI4.SEMR 4007 0087h, SCI5.SEMR 4007 00A7h, SCI6.SEMR 4007 00C7h, SCI7.SEMR 4007 00E7h, SCI8.SEMR 4007 0107h, SCI9.SEMR 4007 0127h

	b7	b6	b5	b4	b3	b2	b1	b0
	RXDESEL	BGDM	NFEN	ABCS	ABCSE	BRME	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0, b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b2	BRME	Bit Rate Modulation Enable	0: Disable bit rate modulation function 1: Enable bit rate modulation function.	R/W*1
b3	ABCSE	Asynchronous Mode Extended Base Clock Select 1	Valid only in asynchronous mode with SCR.CKE[1] = 0: 0: Clock cycles for 1-bit period determined by combination of the BGDM and ABCS bits in the SEMR register 1: Baud rate is 6 base clock cycles for 1-bit period.	R/W*1
b4	ABCS	Asynchronous Mode Base Clock Select	Valid only in asynchronous mode: 0: Select 16 base clock cycles for 1-bit period 1: Select 8 base clock cycles for 1-bit period.	R/W*1
b5	NFEN	Digital Noise Filter Function Enable	• In asynchronous mode: 0: Disable noise cancellation function for RXDn input signal 1: Enable noise cancellation function for RXDn input signal. • In simple IIC mode: 0: Disable noise cancellation function for SCLn and SDAn input signals 1: Enable noise cancellation function for SCLn and SDAn input signals. The NFEN bit must be 0 in all other modes.	R/W*1
b6	BGDM	Baud Rate Generator Double-Speed Mode Select	Valid only in asynchronous mode with SCR.CKE[1] = 0. 0: Output clock from baud rate generator with single frequency 1: Output clock from baud rate generator with double frequency.	R/W*1
b7	RXDESEL	Asynchronous Start Bit Edge Detection Select	Valid only in asynchronous mode: 0: Detect low level on RXDn pin as start bit 1: Detect falling edge of RXDn pin as start bit.	R/W*1

Note 1. Writable only when the TE and RE bits in SCR/SCR_SMCI are 0 (both serial transmission and reception are disabled).

The SEMR register selects the clock source for the 1-bit period in asynchronous mode.

BRME bit (Bit Rate Modulation Enable)

The BRME bit enables or disables the bit rate modulation function. The bit rate generated by the on-chip baud rate generator is evenly corrected when this function is enabled.

ABCSE bit (Asynchronous Mode Extended Base Clock Select 1)

The ABCSE bit sets the pulse number for the base clock in a 1-bit period to 6, and the double-frequency clock is output from the baud rate generator. When the bit rate is set to 6 while dividing the bus clock frequency, use this bit and set SMR.CKS[1:0] = 00b and BRR = 0. Set this bit to 0 except in asynchronous mode.

比特率(bps)	工作频率PCLKA(MHz)														
	50					60					120				
	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)	n	N	M	BGDM bit	Error (%)
230400	0	3	151	0	0.00	0	10	173	1	-0.01	0	10	173	0	-0.01
460800	0	1	151	0	0.00	0	6	220	1	-0.09	0	10	173	1	-0.09

Note 1. 在本例中，SEMR寄存器中的ABCS和ABCSE位为0。SEMR.BRME=0(M=256)禁用比特率调制功能。

34.2.19 串行扩展模式寄存器(SEMR)

Address(es): SCI0.SEMR 4007 0007h, SCI1.SEMR 4007 0027h, SCI2.SEMR 4007 0047h, SCI3.SEMR 4007 0067h, SCI4.SEMR 4007 0087h, SCI5.SEMR 4007 00A7h, SCI6.SEMR 4007 00C7h, SCI7.SEMR 4007 00E7h, SCI8.SEMR 4007 0107h, SCI9.SEMR 4007 0127h

	b7	b6	b5	b4	b3	b2	b1	b0
	RXDESEL	BGDM	NFEN	ABCS	ABCSE	BRME	—	—
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0, b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b2	BRME	比特率调制 Enable	0：禁用码率调制功能1：启用码率调制功能。	R/W*1
b3	ABCSE	异步模式扩展基本时钟 Select 1	仅在SCR.CKE[1]=0的异步模式下有效：0：1位周期的时钟周期由SEMR寄存器中的BGDM和ABCS位的组合确定1：波特率为1位的6个基本时钟周期时期。	R/W*1
b4	ABCS	异步模式 基本时钟选择	仅在异步模式下有效：0：为1位周期选择16个基本时钟周期1：为1位周期选择8个基本时钟周期。	R/W*1
b5	NFEN	数字噪声滤波器 功能启用	在异步模式下：0：禁用RXDn输入信号的噪声消除功能1：启用RXDn输入信号的噪声消除功能。 在简单IIC模式下：0：禁用SCLn和SDAn输入信号的噪声消除功能1：启用SCLn和SDAn输入信号的噪声消除功能。在所有其他模式下，NFEN位必须为0。	R/W*1
b6	BGDM	波特率发生器双速模式 Select	仅在SCR.CKE[1]=0的异步模式下有效。0：单频波特率发生器的输出时钟1：双频波特率发生器的输出时钟。	R/W*1
b7	RXDESEL	异步起始位边沿检测选择	仅在异步模式下有效：0：检测RXDn引脚的低电平作为起始位1：检测RXDn引脚的下降沿作为起始位。	R/W*1

Note 1. 仅当SCRSCR_SMCI中的TE和RE位为0时可写（串行发送和接收都被禁用）。

SEMR寄存器选择异步模式下1位周期的时钟源。

BRME位（比特率调制使能）

BRME位启用或禁用比特率调制功能。该功能使能时，片内波特率发生器产生的比特率得到均匀校正。

ABCSE位（异步模式扩展基本时钟选择1）

ABCSE位将基本时钟在1位周期内的脉冲数设置为6，并从波特率发生器输出双频时钟。当比特率设置为6并同时分频总线时钟频率时，使用该位并设置SMR.CKS[1:0]=00b和BRR=0。除异步模式外，将此位设置为0。

ABCS bit (Asynchronous Mode Base Clock Select)

The ABCS bit selects the number of clock cycles for a 1-bit period. Set this bit to 0 except in asynchronous mode.

NFEN bit (Digital Noise Filter Function Enable)

The NFEN bit enables or disables the digital noise filter function.

When the digital noise filter function is enabled:

- Noise cancellation is applied to the RXDn input signal in asynchronous mode
- Noise cancellation is applied to the SDAn and SCLn input signals in simple IIC mode.

In all other modes, set the NFEN bit to 0 to disable the digital noise filter function. When the function is disabled, input signals are transferred as received.

BGDM bit (Baud Rate Generator Double-Speed Mode Select)

The BGDM bit selects whether or not to double the base clock frequency output from the baud rate generator.

The BGDM bit is valid when the on-chip baud rate generator is selected as the clock source (SCR.CKE[1] = 0) in asynchronous mode (SMR.CM = 0). The base clock is generated by the clock output from the baud rate generator. When the BGDM bit is set to 1, the base clock cycle is halved and the bit rate is doubled.

Set this bit to 0 in modes other than asynchronous mode.

RXDESEL bit (Asynchronous Start Bit Edge Detection Select)

The RXDSEL bit selects the detection method of the start bit for reception in asynchronous mode. When a break occurs, data reception operation depends on the setting of this bit. Set this bit to 1 when reception must be stopped while a break occurs or when reception must be started without keeping the RXDn pin input at the high level for the period of one data frame or longer after completion of the break.

Set this bit to 0 in modes other than asynchronous mode.

34.2.20 Noise Filter Setting Register (SNFR)

Address(es): SCI0.SNFR 4007 0008h, SCI1.SNFR 4007 0028h, SCI2.SNFR 4007 0048h, SCI3.SNFR 4007 0068h, SCI4.SNFR 4007 0088h, SCI5.SNFR 4007 00A8h, SCI6.SNFR 4007 00C8h, SCI7.SNFR 4007 00E8h, SCI8.SNFR 4007 0108h, SCI9.SNFR 4007 0128h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	NFCS[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	NFCS[2:0]	Noise Filter Clock Select	In asynchronous mode, selects the standard setting for the base clock: b2 b0 0 0 0: Use clock signal divided by 1 with noise filter. In simple IIC mode, selects the standard settings for the clock source of the on-chip baud rate generator selected in the SMR.CKS[1:0] bits: b2 b0 0 0 1: Use clock signal divided by 1 with noise filter 0 1 0: Use clock signal divided by 2 with noise filter 0 1 1: Use clock signal divided by 4 with noise filter 1 0 0: Use clock signal divided by 8 with noise filter. Other settings are prohibited.	R/W*1
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Writing to these bits is only possible when the RE and TE bits in SCR/SCR_SMCI are 0 (serial reception and transmission disabled).

ABCS位（异步模式基本时钟选择）

ABCS位选择1位周期的时钟周期数。除异步模式外，将此位设置为0。

NFEN位（数字噪声滤波器功能使能）

NFEN位启用或禁用数字噪声滤波器功能。

启用数字噪声滤波器功能时：

- 噪声消除应用于异步模式下的RXDn输入信号
- 噪声消除应用于简单IIC模式下的SDAn和SCLn输入信号。

在所有其他模式下，将NFEN位设置为0以禁用数字噪声滤波器功能。禁用该功能时，输入信号按接收到的方式传输。

BGDM位（波特率发生器双速模式选择）

BGDM位选择是否将波特率发生器输出的基本时钟频率加倍。

当在异步模式（SMR.CM=0）下选择片内波特率发生器作为时钟源（SCR.CKE[1]=0）时，BGDM位有效。基本时钟由波特率发生器的时钟输出生成。当BGDM位设置为1时，基本时钟周期减半，比特率加倍。

在异步模式以外的模式下将此位设置为0。

RXDESEL位（异步起始位边沿检测选择）

RXDSEL位选择异步模式下接收起始位的检测方法。发生中断时，数据接收操作取决于该位的设置。如果在发生中断时必须停止接收，或者在中断完成后RXDn引脚输入在一个数据帧或更长时间内不保持高电平而必须开始接收时，将该位设置为1。

34.2.20 噪声滤波器设置寄存器(SNFR)

Address(es): SCI0.SNFR 4007 0008h, SCI1.SNFR 4007 0028h, SCI2.SNFR 4007 0048h, SCI3.SNFR 4007 0068h, SCI4.SNFR 4007 0088h, SCI5.SNFR 4007 00A8h, SCI6.SNFR 4007 00C8h, SCI7.SNFR 4007 00E8h, SCI8.SNFR 4007 0108h, SCI9.SNFR 4007 0128h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	NFCS[2:0]		
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b2 to b0	NFCS[2:0]	噪声滤波器时钟选择	在异步模式下，选择基本时钟的标准设置：b2b0000：使用带噪声滤波器的时钟信号除以1。 在简单IIC模式下，为在SMR.CKS[1:0]位中选择的片内波特率发生器的时钟源选择标准设置：b2b0001：使用时钟信号除以1和噪声滤波器010：使用带噪声滤波器的时钟信号除以2011：使用带噪声滤波器的时钟信号除以4100：使用带噪声滤波器的时钟信号除以8。禁止其他设置。	R/W*1
b7 to b3	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 只有当SCRSCR_SMCI中的RE和TE位为0（串行接收和发送禁用）时，才能写入这些位。

The SNFR register sets the digital noise filter clock.

NFCS[2:0] bits (Noise Filter Clock Select)

The NFCS[2:0] bits select the sampling clock for the digital noise filter. To use the noise filter in asynchronous mode, set these bits to 000b. In simple IIC mode, set the bits to a value in the range from 001b to 100b.

34.2.21 IIC Mode Register 1 (SIMR1)

Address(es): SCI0.SIMR1 4007 0009h, SCI1.SIMR1 4007 0029h, SCI2.SIMR1 4007 0049h, SCI3.SIMR1 4007 0069h, SCI4.SIMR1 4007 0089h, SCI5.SIMR1 4007 00A9h, SCI6.SIMR1 4007 00C9h, SCI7.SIMR1 4007 00E9h, SCI8.SIMR1 4007 0109h, SCI9.SIMR1 4007 0129h

	b7	b6	b5	b4	b3	b2	b1	b0
	IICDL[4:0]					—	—	IICM
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	IICM	Simple IIC Mode Select	SMIF IICM 0 0: Asynchronous mode (including multi-processor mode), clock synchronous mode, or simple SPI mode 0 1: Simple IIC mode 1 0: Smart card interface mode 1 1: Setting prohibited.	R/W*1
b2, b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7 to b3	IICDL[4:0]	SDA Delay Output Select	SDA signal output delay in cycles of the clock signal from the on-chip baud rate generator: b7 b3 0 0 0 0 0: No output delay 0 0 0 0 1: 0 to 1 cycle 0 0 0 1 0: 1 to 2 cycles 0 0 0 1 1: 2 to 3 cycles 0 0 1 0 0: 3 to 4 cycles 0 0 1 0 1: 4 to 5 cycles : 1 1 1 1 0: 29 to 30 cycles 1 1 1 1 1: 30 to 31 cycles.	R/W*1

Note 1. Writing to these bits is only possible when the RE and TE bits in the SCR register are 0 (both serial transmission and reception are disabled).

SIMR1 selects simple IIC mode and the number of delay stages for the SDAn output.

IICM bit (Simple IIC Mode Select)

In combination with the SCMR.SMIF bit, the IICM bit selects the operating mode.

IICDL[4:0] bits (SDA Delay Output Select)

The IICDL[4:0] bits specify an output delay on the SDAn pin relative to the falling edge of the output on the SCLn pin.

The available delay settings range from no delay to 31 cycles, with the clock signal from the on-chip baud rate generator as the base. The signal obtained by frequency-dividing PCLKA by the divisor set in SMR.CKS[1:0] is supplied as the clock signal from the on-chip baud rate generator. Set these bits to 00000b unless operation is in simple IIC mode. In simple IIC mode, set the bits to a value in the range from 00001b to 11111b.

SNFR寄存器设置数字噪声滤波器时钟。

NFCS[2:0]位（噪声滤波器时钟选择）

NFCS[2:0]位选择数字噪声滤波器的采样时钟。要在异步模式下使用噪声滤波器，请将这些位设置为000b。在简单IIC模式下，将位设置为001b到100b范围内的值。

34.2.21 IIC模式寄存器1(SIMR1)

Address(es): SCI0.SIMR1 4007 0009h, SCI1.SIMR1 4007 0029h, SCI2.SIMR1 4007 0049h, SCI3.SIMR1 4007 0069h, SCI4.SIMR1 4007 0089h, SCI5.SIMR1 4007 00A9h, SCI6.SIMR1 4007 00C9h, SCI7.SIMR1 4007 00E9h, SCI8.SIMR1 4007 0109h, SCI9.SIMR1 4007 0129h

	b7	b6	b5	b4	b3	b2	b1	b0
	IICDL[4:0]					—	—	IICM
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	IICM	简单IIC模式选择	SMIFIICM00：异步模式（包括多处理器模式）、时钟同步模式或简单SPI模式01：简单IIC模式10：智能卡接口模式11：禁止设置。	R/W*1
b2, b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b7 to b3	IICDL[4:0]	SDA延迟输出选择	SDA信号输出延迟，以片内波特率发生器的时钟信号周期为单位：b7 b300000：无输出延迟00001：0到1个周期00010：1到2个周期00011：2到3个周期00100：3到4个周期00101：4到5个周期 ：11110：29至30个周期 11111：30至31个周期。	R/W*1

Note 1. 只有当SCR寄存器中的RE和TE位为0（串行发送和接收都被禁用）时，才能写入这些位。

SIMR1选择简单IIC模式和SDAn输出的延迟级数。

IICM位（简单IIC模式选择）

IICM位与SCMR.SMIF位一起选择工作模式。

IICDL[4:0]位（SDA延迟输出选择）

IICDL[4:0]位指定SDAn引脚上相对于SCLn引脚输出下降沿的输出延迟。

可用的延迟设置范围从无延迟到31个周期，以来自片上波特率发生器的时钟信号为基准。通过在SMR.CKS[1:0]中设置的除数对PCLKA进行分频获得的信号作为来自片上波特率发生器的时钟信号提供。除非在简单IIC模式下操作，否则将这些位设置为00000b。在简单IIC模式下，将位设置为00001b到11111b范围内的值。

34.2.22 IIC Mode Register 2 (SIMR2)

Address(es): SCI0.SIMR2 4007 000Ah, SCI1.SIMR2 4007 002Ah, SCI2.SIMR2 4007 004Ah, SCI3.SIMR2 4007 006Ah, SCI4.SIMR2 4007 008Ah, SCI5.SIMR2 4007 00AAh, SCI6.SIMR2 4007 00CAh, SCI7.SIMR2 4007 00EAh, SCI8.SIMR2 4007 010Ah, SCI9.SIMR2 4007 012Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	IICACKT	—	—	—	IICCSC	IICINTM
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	IICINTM	IIC Interrupt Mode Select	0: Use ACK/NACK interrupts 1: Use reception and transmission interrupts.	R/W*1
b1	IICCSC	Clock Synchronization	0: Do not synchronize with clock signal 1: Synchronize with clock signal.	R/W*1
b4 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b5	IICACKT	ACK Transmission Data	0: ACK transmission 1: NACK transmission and ACK/NACK reception.	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Writing to these bits is only possible when the RE and TE bits in the SCR register are 0 (serial reception and transmission disabled).

SIMR2 selects how reception and transmission are controlled in simple IIC mode.

IICINTM bit (IIC Interrupt Mode Select)

The IICINTM bit selects the sources of interrupt requests in simple IIC mode.

IICCSC bit (Clock Synchronization)

Set the IICCSC bit to 1 if the internally generated SCL clock signal is to be synchronized when the SCLn pin is driven low because a wait was inserted by another other device.

The SCL clock signal is not synchronized if the IICCSC bit is 0. The SCL clock signal is generated according to the rate selected in the BRR register regardless of the level being input on the SCLn pin.

Set the IICCSC bit to 1 except during debugging.

IICACKT bit (ACK Transmission Data)

Transmitted data contains ACK bits. Set the IICACKT bit to 1 when ACK and NACK bits are received.

34.2.23 IIC Mode Register 3 (SIMR3)

Address(es): SCI0.SIMR3 4007 000Bh, SCI1.SIMR3 4007 002Bh, SCI2.SIMR3 4007 004Bh, SCI3.SIMR3 4007 006Bh, SCI4.SIMR3 4007 008Bh, SCI5.SIMR3 4007 00ABh, SCI6.SIMR3 4007 00CBh, SCI7.SIMR3 4007 00EBh, SCI8.SIMR3 4007 010Bh, SCI9.SIMR3 4007 012Bh

	b7	b6	b5	b4	b3	b2	b1	b0
	IICSCLS[1:0]		IICSDAS[1:0]		IICSTIF	IICSTPREQ	IICRSTAREQ	IICSTAREQ
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	IICSTAREQ	Start Condition Generation	0: Do not generate start condition 1: Generate start condition.*1, *3, *5, *6	R/W
b1	IICRSTAREQ	Restart Condition Generation	0: Do not generate restart condition 1: Generate restart condition.*2, *3, *5, *6	R/W

34.2.22 IIC模式寄存器2(SIMR2)

Address(es): SCI0.SIMR2 4007 000Ah, SCI1.SIMR2 4007 002Ah, SCI2.SIMR2 4007 004Ah, SCI3.SIMR2 4007 006Ah, SCI4.SIMR2 4007 008Ah, SCI5.SIMR2 4007 00AAh, SCI6.SIMR2 4007 00CAh, SCI7.SIMR2 4007 00EAh, SCI8.SIMR2 4007 010Ah, SCI9.SIMR2 4007 012Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	IICACKT	—	—	—	IICCSC	IICINTM
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	IICINTM	IIC中断模式选择	0：使用ACKNACK中断1：使用接收和发送中断。	R/W*1
b1	IICCSC	时钟同步	0：不与时钟信号同步1：与时钟信号同步。	R/W*1
b4 to b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b5	IICACKT	ACK传输数据	0：ACK发送1：NACK发送和ACKNACK接收。	R/W
b7, b6	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 只有当SCR寄存器中的RE和TE位为0（串行接收和发送禁用）时，才能写入这些位。

SIMR2选择在简单IIC模式下如何控制接收和发送。

IICINTM位（IIC中断模式选择）

IICINTM位选择简单IIC模式下的中断请求源。

IICCSC bit (Clock Synchronization)

如果在SCLn引脚被驱动为低电平时要同步内部生成的SCL时钟信号，则将IICCSC位设置为1，因为另一个其他设备插入了等待。

如果IICCSC位为0，则SCL时钟信号不同步。SCL时钟信号根据BRR寄存器中选择的速率生成，与SCLn引脚上输入的电平无关。

除调试期间外，将IICCSC位设置为1。

IICACKT位（ACK传输数据）

传输的数据包含ACK位。当收到ACK和NACK位时，将IICACKT位设置为1。

34.2.23 IIC模式寄存器3(SIMR3)

Address(es): SCI0.SIMR3 4007 000Bh, SCI1.SIMR3 4007 002Bh, SCI2.SIMR3 4007 004Bh, SCI3.SIMR3 4007 006Bh, SCI4.SIMR3 4007 008Bh, SCI5.SIMR3 4007 00ABh, SCI6.SIMR3 4007 00CBh, SCI7.SIMR3 4007 00EBh, SCI8.SIMR3 4007 010Bh, SCI9.SIMR3 4007 012Bh

	b7	b6	b5	b4	b3	b2	b1	b0
	IICSCLS[1:0]		IICSDAS[1:0]		IICSTIF	IICSTPREQ	IICRSTAREQ	IICSTAREQ
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	IICSTAREQ	开始条件生成	0：不产生启动条件1：产生启动条件。 1，*3，*5，*6	R/W
b1	IICRSTAREQ	重启条件Generation	0：不产生重启条件1：产生重启条件。*2，*3，*5，*6	R/W

Bit	Symbol	Bit name	Description	R/W
b2	IICSTPREQ	Stop Condition Generation	0: Do not generate stop condition 1: Generate stop condition.*2, *3, *5, *6	R/W
b3	IICSTIF	Issuing of Start, Restart, or Stop Condition Completed Flag	0: No requests are being made for generating conditions, or a condition is being generated 1: Generation of start, restart, or stop condition is complete. When 0 is written to IICSTIF, it is cleared to 0.*4	R/W*4
b5, b4	IICSDAS[1:0]	SDA Output Select	b5 b4 0 0: Output serial data 0 1: Generate start, restart, or stop condition 1 0: Output low on SDAn pin 1 1: Drive SDAn pin to high-impedance state.	R/W
b7, b6	IICSCLS[1:0]	SCL Output Select	b7 b6 0 0: Output serial clock 0 1: Generate start, restart, or stop condition 1 0: Output low on SCLn pin 1 1: Drive SCLn pin to high-impedance state.	R/W

Note 1. Only generate a start condition after checking the bus state and confirming that the bus is free.
Note 2. Generate a restart or stop condition after checking the bus state and confirming that the bus is busy.
Note 3. Do not set more than one of the IICSTAREQ, IICRSTAREQ, and IICSTPREQ bits to 1 at a given time.
Note 4. Write only 0. When 1 is written, the value is ignored.
Note 5. Execute the generation of a condition after the value of the IICSTIF flag is 0.
Note 6. Do not write 0 to this bit while it is 1. Generation of a condition is suspended by writing 0 to this bit while it is 1.

IICSTAREQ bit (Start Condition Generation)

When a start condition is to be generated, set both IICSDAS[1:0] and IICSCLS[1:0] to 01b in addition to setting the IICSTAREQ bit to 1.

[Setting condition]

- On writing 1 to the bit.

[Clearing condition]

- On completion of start condition generation.

IICRSTAREQ bit (Restart Condition Generation)

When a restart condition is to be generated, set both IICSDAS[1:0] and IICSCLS[1:0] to 01b in addition to setting the IICRSTAREQ bit to 1.

[Setting condition]

- On writing 1 to the bit.

[Clearing condition]

- On completion of restart condition generation.

IICSTPREQ bit (Stop Condition Generation)

When a stop condition is to be generated, set both IICSDAS[1:0] and IICSCLS[1:0] to 01b in addition to setting the IICSTPREQ bit to 1.

[Setting condition]

- On writing 1 to the bit.

[Clearing condition]

- On completion of stop condition generation.

IICSTIF flag (Issuing of Start, Restart, or Stop Condition Completed Flag)

After generating a condition, the IICSTIF flag indicates that the condition generation is complete. When using the IICSTAREQ, IICRSTAREQ, or IICSTPREQ bit to cause generation of a condition, do so after setting the IICSTIF flag to 0.

Bit	Symbol	位名称	Description	R/W
b2	IICSTPREQ	停止条件生成	0：不产生停止条件1：产生停止条件 。*2 *3 *5 *6	R/W
b3	IICSTIF	发出启动、重启或停止条件已完成 Flag	0：没有请求生成条件，或正在生成条件1：开始、重新启动或停止条件的生成已完成。当0写入IICSTIF时，它被清除为0。*4	R/W*4
b5, b4	IICSDAS[1:0]	SDA输出选择	b5b400：输出串行数据01：产生启动、重启或停止条件10：SDAn引脚1输出低电平1：驱动SDAn引脚为高阻态。	R/W
b7, b6	IICSCLS[1:0]	SCL输出选择	b7b600：输出串行时钟01：产生启动、重启或停止条件10：在SCLn引脚上输出低电平11：将SCLn引脚驱动为高阻态。	R/W

Note 1. 只有在检查总线状态并确认总线空闲后才产生启动条件。
Note 2. 在检查总线状态并确认总线繁忙后生成重新启动或停止条件。
Note 3. 在给定时间，不要将IICSTAREQ、IICRSTAREQ和IICSTPREQ位中的一个以上设置为1。
Note 4. 仅写入0。写入1时，忽略该值。
Note 5. 在IICSTIF标志的值为0后执行条件的生成。
Note 6. 请勿在该位为1时向其写入0。当该位为1时，向该位写入0可暂停条件的生成。

IICSTAREQ位（开始条件生成）

当要产生一个开始条件时，除了设置IICSDAS[1:0]和IICSCLS[1:0]为01b IICSTAREQ位为1。

[Setting condition]

- 在向该位写入1时。

[Clearing condition]

- 完成启动条件生成。

IICRSTAREQ位（重启条件生成）

当要产生重启条件时，除了设置IICSDAS[1:0]和IICSCLS[1:0]为01b IICRSTAREQ位为1。

[Setting condition]

- 在向该位写入1时。

[Clearing condition]

- 完成重启条件生成。

IICSTPREQ位（停止条件生成）

当要产生停止条件时，除了设置IICSDAS[1:0]和IICSCLS[1:0]为01b IICSTPREQ位为1。

[Setting condition]

- 在向该位写入1时。

[Clearing condition]

- 停止条件生成完成后。

IICSTIF标志（发出启动、重启或停止条件完成标志）

生成条件后，IICSTIF标志指示条件生成完成。使用时 IICSTAREQ、IICRSTAREQ或IICSTPREQ位会导致条件生成，请在将IICSTIF标志设置为0后执行此操作。

When the IICSTIF flag is 1 while an interrupt request is enabled by setting the SCR.TEIE bit, an STI request is output.

[Setting condition]

- On completion of a start, restart, or stop condition generation.

  If the setting condition conflicts with any of the clearing conditions for the flag, the clearing condition takes precedence.

[Clearing conditions]

- On writing 0 to the bit. After writing 0 to the IICSTIF bit, read the bit to check that it is actually set to 0.
- On writing 0 to the SIMR1.IICM bit when operation is not in simple IIC mode
- On writing 0 to the SCR.TE bit.

IICSDAS[1:0] bits (SDA Output Select)

The IICSDAS[1:0] bits control output from the SDAn pin. Set IICSDAS[1:0] and IICSCLS[1:0] to the same value.

IICSCLS[1:0] bits (SCL Output Select)

The IICSCLS[1:0] bits control output from the SCLn pin. Set IICSCLS[1:0] and IICSDAS[1:0] to the same value.

34.2.24 IIC Status Register (SISR)

Address(es): SCI0.SISR 4007 000Ch, SCI1.SISR 4007 002Ch, SCI2.SISR 4007 004Ch, SCI3.SISR 4007 006Ch, SCI4.SISR 4007 008Ch, SCI5.SISR 4007 00ACh, SCI6.SISR 4007 00CCh, SCI7.SISR 4007 00ECh, SCI8.SISR 4007 010Ch, SCI9.SISR 4007 012Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	IICACKR
Value after reset:	0	0	x	x	0	x	0	0

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b0	IICACKR	ACK Reception Data Flag	0: ACK received 1: NACK received.	R
b1	—	Reserved	This bit is read as 0.	R
b2	—	Reserved	The read value is undefined.	R
b3	—	Reserved	This bit is read as 0.	R
b5, b4	—	Reserved	The read value is undefined.	R
b7, b6	—	Reserved	These bits are read as 0.	R

SISR monitors the state in simple IIC mode.

IICACKR flag (ACK Reception Data Flag)

Received ACK and NACK bits can be read from the IICACKR flag. The IICACKR flag is updated on the rising edge of the SCLn clock for the received ACK/NACK bit.

当IICSTIF标志为1且通过设置SCR.TEIE位使能中断请求时，输出STI请求。

[Setting condition]

- 在完成启动、重新启动或停止条件生成时。

如果设置条件与标志的任何清除条件冲突，则清除条件优先。【清算条件】

- 将0写入该位。将0写入IICSTIF位后，读取该位以检查它是否实际设置为0。
- 在非简单IIC模式下向SIMR1.IICM位写入0
- 向SCR.TE位写入0。

IICSDAS[1:0]位（SDA输出选择）

IICSDAS[1:0]位控制SDAn引脚的输出。将IICSDAS[1:0]和IICSCLS[1:0]设置为相同的值。

IICSCLS[1:0]位（SCL输出选择）

IICSCLS[1:0]位控制SCLn引脚的输出。将IICSCLS[1:0]和IICSDAS[1:0]设置为相同的值。

34.2.24 IIC状态寄存器(SISR)

Address(es): SCI0.SISR 4007 000Ch, SCI1.SISR 4007 002Ch, SCI2.SISR 4007 004Ch, SCI3.SISR 4007 006Ch, SCI4.SISR 4007 008Ch, SCI5.SISR 4007 00ACh, SCI6.SISR 4007 00CCh, SCI7.SISR 4007 00ECh, SCI8.SISR 4007 010Ch, SCI9.SISR 4007 012Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	IICACKR
重置后的值：	0	0	x	x	0	x	0	0

x: Undefined

Bit	Symbol	位名称	Description	R/W
b0	IICACKR	ACK接收数据标志	0：收到ACK1：收到NACK。	R
b1	—	Reserved	该位读为0。	R
b2	—	Reserved	读取值未定义。	R
b3	—	Reserved	该位读为0。	R
b5, b4	—	Reserved	读取值未定义。	R
b7, b6	—	Reserved	这些位读为0。	R

SISR在简单IIC模式下监控状态。

IICACKR标志（ACK接收数据标志）

接收到的ACK和NACK位可以从IICACKR标志中读取。IICACKR标志在接收到的ACKNACK位的SCLn时钟的上升沿更新。

34.2.25 SPI Mode Register (SPMR)

Address(es): SCI0.SPMR 4007 000Dh, SCI1.SPMR 4007 002Dh, SCI2.SPMR 4007 004Dh, SCI3.SCI3 4007 006Dh, SCI4.SPMR 4007 008Dh, SCI5.SPMR 4007 00ADh, SCI6.SPMR 4007 00CDh, SCI7.SCI7 4007 00EDh, SCI8.SPMR 4007 010Dh, SCI9.SPMR 4007 012Dh

	b7	b6	b5	b4	b3	b2	b1	b0
	CKPH	CKPOL	—	MFF	—	MSS	CTSE	SSE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	SSE	SSn Pin Function Enable	0: Disable SSn pin function 1: Enable SSn pin function.	R/W*1
b1	CTSE	CTS Enable	0: Disable CTS function (enable RTS output function) 1: Enable CTS function.	R/W*1
b2	MSS	Master Slave Select	0: Transmit through TXDn pin and receive through RXDn pin (master mode) 1: Receive through TXDn pin and transmit through RXDn pin (slave mode).	R/W*1
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	MFF	Mode Fault Flag	0: No mode fault error 1: Mode fault error.	R/W*2
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6	CKPOL	Clock Polarity Select	0: Do not invert clock polarity 1: Invert clock polarity.	R/W*1
b7	CKPH	Clock Phase Select	0: Do not delay clock 1: Delay clock.	R/W*1

Note 1. Writing to these bits is only possible when the RE and TE bits in the SCR register are 0 (both serial transmission and reception are disabled).
Note 2. Only 0 can be written to this bit, to clear the flag.

The SPMR register selects settings for simple SPI mode.

SSE bit (SSn Pin Function Enable)

Set the SSE bit to 1 to use the SSn pin to control transmission and reception in simple SPI mode. Set this bit to 0 in all other modes. In simple SPI mode, when master mode is selected (SCR.CKE[1:0] = 00b and SPMR.MSS = 0) and there is a single master, the SSn pin on the master side is not required to control reception and transmission. In such a case, set the SSE bit to 0. Do not set both the SSE and CTSE bits to 1. If this setting is made, operation is the same as that when these bits are set to 0.

CTSE bit (CTS Enable)

Set the CTSE bit to 1 if the SSn pin is to be used for inputting the CTS control signal to control transmission and reception. The RTS signal is output when this bit is set to 0. Set this bit to 0 in smart card interface mode, simple SPI mode, and simple IIC mode. Do not set both the CTSE and SSE bits to 1. If this setting is made, operation is the same as that when these bits are set to 0.

MSS bit (Master Slave Select)

The MSS bit selects master or slave operation in simple SPI mode. The functions of the TXDn and RXDn pins are reversed when this bit is set to 1, so that data is received through the TXDn pin and transmitted through the RXDn pin. Set this bit to 0 in modes other than simple SPI mode.

MFF flag (Mode Fault Flag)

The MFF flag indicates mode fault errors. In a multi-master configuration, determine the mode fault error occurrence by reading this flag.

34.2.25 SPI模式寄存器(SPMR)

Address(es): SCI0.SPMR 4007 000Dh, SCI1.SPMR 4007 002Dh, SCI2.SPMR 4007 004Dh, SCI3.SCI3 4007 006Dh, SCI4.SPMR 4007 008Dh, SCI5.SPMR 4007 00ADh, SCI6.SPMR 4007 00CDh, SCI7.SCI7 4007 00EDh, SCI8.SPMR 4007 010Dh, SCI9.SPMR 4007 012Dh

	b7	b6	b5	b4	b3	b2	b1	b0
	CKPH	CKPOL	—	MFF	—	MSS	CTSE	SSE
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	SSE	SSn引脚功能使能	0：禁用SSn引脚功能1：启用SSn引脚功能。	R/W*1
b1	CTSE	CTS Enable	0：关闭CTS功能（开启RTS输出功能）1：开启CTS功能。	R/W*1
b2	MSS	主从选择	0：通过TXDn引脚发送并通过RXDn引脚接收（主模式）1：通过TXDn引脚接收并通过RXDn引脚发送（从模式）。	R/W*1
b3	—	Reserved	该位读取为0。写入值应为0。	R/W
b4	MFF	模式故障标志	0：无模式故障错误1：模式故障错误。	R/W*2
b5	—	Reserved	该位读取为0。写入值应为0。	R/W
b6	CKPOL	时钟极性选择	0：不反转时钟极性1：反转时钟极性。	R/W*1
b7	CKPH	时钟相位选择	0：不延迟时钟1：延迟时钟。	R/W*1

Note 1. 只有当SCR寄存器中的RE和TE位为0（串行发送和接收都被禁用）时，才能写入这些位。

Note 2. 只能向该位写入0，以清除标志。

SPMR寄存器选择简单SPI模式的设置。

SSE位（SSn引脚功能使能）

将SSE位设置为1以使用SSn引脚控制简单SPI模式下的发送和接收。在所有其他模式下将此位设置为0。在简单的SPI模式下，选择主模式（SCR.CKE[1：0]=00B和SPMR.MSS=0），并且有一个主人，主侧不需要SSNPIN来控制接收和传输.在这种情况下，请将SSE位设置为0。不要将SSE和CTSE位都设置为1。如果进行此设置，则操作与将这些位设置为0时的操作相同。

CTSE位（CTS使能）

如果SSn引脚用于输入CTS控制信号以控制发送和接收，请将CTSE位设置为1。当该位设置为0时输出RTS信号。在智能卡接口模式、简单SPI模式和简单IIC模式下将该位设置为0。不要将CTSE和SSE位都设置为1。如果进行此设置，则操作与将这些位设置为0时的操作相同。

MSS位（主从选择）

MSS位选择简单SPI模式下的主机或从机操作。当该位设置为1时，TXDn和RXDn引脚的功能相反，因此数据通过TXDn引脚接收并通过RXDn引脚发送。在简单SPI模式以外的模式下将此位设置为0。

MFF标志（模式故障标志）

MFF标志指示模式故障错误。在多主机配置中，通过读取该标志确定模式故障错误发生。

[Setting condition]

- When input on the SSn pin is low during master operation in simple SPI mode (SSE bit = 1 and MSS bit = 0).

[Clearing condition]

- On writing 0 to the bit after it is read as 1.

CKPOL bit (Clock Polarity Select)

The CKPOL bit selects the polarity of the clock signal output through the SCKn pin. See Figure 34.70 for details. Set the CKPOL bit to 0 in all modes other than simple SPI mode and clock synchronous mode.

CKPH bit (Clock Phase Select)

The CKPH bit selects the phase of the clock signal output through the SCKn pin. See Figure 34.70 for details. Set the CKPH bit to 0 in all modes other than simple SPI mode and clock synchronous mode.

34.2.26 FIFO Control Register (FCR)

Address(es): SCI0.FCR 4007 0014h, SCI1.FCR 4007 0034h, SCI2.FCR 4007 0054h, SCI3.FCR 4007 0074h, SCI4.FCR 4007 0094h, SCI5.FCR 4007 00B4h, SCI6.FCR 4007 00D4h, SCI7.FCR 4007 00F4h, SCI8.FCR 4007 0114h, SCI9.FCR 4007 0134h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RSTRG[3:0]				RTRG[3:0]				TTRG[3:0]				DRES	TFRST	RFRST	FM
Value after reset:	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	FM	FIFO Mode Select	Valid only in asynchronous mode, including multi-processor mode, or clock synchronous mode: 0: Non-FIFO mode. Selects TDR/RDR or TDRHL/RDRHL for communication. 1: FIFO mode. Selects FTDRHL/FRDRHL for communication.	R/W*1
b1	RFRST	Receive FIFO Data Register Reset	Valid only when FCR.FM = 1: 0: Do not reset FRDRHL 1: Reset FRDRHL.	R/W
b2	TFRST	Transmit FIFO Data Register Reset	Valid only when FCR.FM = 1: 0: Do not reset FTDRHL 1: Reset FTDRHL.	R/W
b3	DRES	Receive Data Ready Error Select Bit	Selects the interrupt requested when detecting receive data ready: 0: Receive data full interrupt (SCIn_RXI) 1: Receive error interrupt (SCIn_ERI).	R/W
b7 to b4	TTRG[3:0]	Transmit FIFO Data Trigger Number	Valid only in asynchronous mode, including multi-processor mode, or clock synchronous mode: 0000: Trigger number 0 : 1111: Trigger number 15.	R/W
b11 to b8	RTRG[3:0]	Receive FIFO Data Trigger Number	Valid only in asynchronous mode, including multi-processor mode, or clock synchronous mode: 0000: Trigger number 0 : 1111: Trigger number 15.	R/W
b15 to b12	RSTRG[3:0]	RTS Output Active Trigger Number Select	Valid only in asynchronous mode, including multi-processor mode, or clock synchronous mode, when FCR.FM = 1, SPMR.CTSE = 0, and SPMR.SSE = 0: 0000: Trigger number 0 : 1111: Trigger number 15.	R/W

Note 1. Writable only when TE = 0 and RE = 0.

[Setting condition]

- 在简单SPI模式（SSE位=1和MSS位=0）下主机操作期间SSn引脚上的输入为低电平时。

[Clearing condition]

- 在读取为1后向该位写入0。

CKPOL位（时钟极性选择）

CKPOL位选择通过SCKn引脚输出的时钟信号的极性。有关详细信息，请参见图34.70。设置在除简单SPI模式和时钟同步模式之外的所有模式中，CKPOL位为0。

CKPH位（时钟相位选择）

CKPH位选择通过SCKn引脚输出的时钟信号的相位。有关详细信息，请参见图34.70。设置CKPH位在除简单SPI模式和时钟同步模式之外的所有模式下为0。

34.2.26 先进先出控制寄存器(FCR)

Address(es): SCI0.FCR 4007 0014h, SCI1.FCR 4007 0034h, SCI2.FCR 4007 0054h, SCI3.FCR 4007 0074h, SCI4.FCR 4007 0094h, SCI5.FCR 4007 00B4h, SCI6.FCR 4007 00D4h, SCI7.FCR 4007 00F4h, SCI8.FCR 4007 0114h, SCI9.FCR 4007 0134h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	RSTRG[3:0]				RTRG[3:0]				TTRG[3:0]				DRES	TFRST	RFRST	FM
重置后的值：	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	FM	先进先出模式选择	仅在异步模式下有效，包括多处理器模式，或时钟同步模式：0：非FIFO模式。 选择TDRRDR或TDRHLRDRHL进行通信。1：先进先出模式。 选择FTDRHLFRDRHL进行通信。	R/W*1
b1	RFRST	接收FIFO数据寄存器Reset	仅在FCR.FM=1时有效：0：不复位FRDRHL1：复位FRDRHL。	R/W
b2	TFRST	发送FIFO数据注册重置	仅当FCR.FM=1时有效：0：不复位FTDRHL1：复位FTDRHL。	R/W
b3	DRES	接收数据就绪错误选择位	选择检测接收数据就绪时请求的中断：0：接收数据满中断（SCIn_RXI）1：接收错误中断（SCIn_ERI）。	R/W
b7 to b4	TTRG[3:0]	发送FIFO数据触发Number	仅在异步模式下有效，包括多处理器模式，或时钟同步模式：0000：触发编号0 :1111:触发器编号15。	R/W
b11 to b8	RTRG[3:0]	接收FIFO数据触发Number	仅在异步模式下有效，包括多处理器模式，或时钟同步模式：0000：触发编号0 :1111:触发器编号15。	R/W
b15 to b12	RSTRG[3:0]	RTS输出有源触发号码选择	仅在异步模式下有效，包括多处理器模式，或时钟同步模式，当FCR.FM=1、SPMR.CTSE=0和SPMR.SSE=0时：0000：触发编号0 :1111:触发器编号15。	R/W

Note 1. 仅当TE=0且RE=0时可写。

FCR selects FIFO mode, resets FTDRHL and FRDRHL, selects the FIFO data trigger number for transmission or reception, and selects the RTS output active trigger number.

FM bit (FIFO Mode Select)

When the FM bit is set to 1, FTDRHL and FRDRHL are selected for communication. When the FM bit is set to 0, TDR and RDR, or TDRHL and RDRHL are selected for communication.

RFRST bit (Receive FIFO Data Register Reset)

When the RFRST bit is set to 1, the FRDRHL register is reset and the received data count resets to 0. When 1 is written to the RFRST bit, it clears to 0 after 1 PCLKA.

TFRST bit (Transmit FIFO Data Register Reset)

When the TFRST bit is set to 1, the FTDRHL register is reset and the transmit data count resets to 0. When 1 is written to the TFRST bit, it clears to 0 after 1 PCLKA.

DRES bit (Receive Data Ready Error Select Bit)

When detecting a receive data ready error, the selection can be made from an SCIn_RXI interrupt request or an SCIn_ERI interrupt request. When starting DMAC or DTC and reading from the FRDRH and FRDRL registers, set the DRES bit to 1.

TTRG[3:0] bits (Transmit FIFO Data Trigger Number)

The TDFE flag is set to 1 when the amount of transmit data in FTDRHL is equal to or less than the transmit triggering number specified in the TTRG[3:0] bits, and software can write data to FTDRHL. If SCR.TIE = 1, an SCIn_TXI interrupt request occurs.

RTRG[3:0] bits (Receive FIFO Data Trigger Number)

The RDF flag is set to 1 when the amount of receive data in FRDRHL is equal to or greater than the receive triggering number specified in the RTRG[3:0] bits, and software can read data from FRDRHL. If SCR.RIE = 1, an SCIn_RXI interrupt request occurs.

When RTRG[3:0] is 0, the RDF flag is not set even when the amount of data in the receive FIFO is equal to 0, and an SCIn_RXI interrupt does not occur.

RSTRG[3:0] bits (RTS Output Active Trigger Number Select)

When the amount of receive data stored in FRDRHL is equal to or greater than the receive triggering number specified in the RSTRG[3:0] bits, the RTS signal goes high.

When RSTRG[3:0] is 0, the RTS signal does not go high even when the amount of data in FRDRHL is equal to 0.

34.2.27 FIFO Data Count Register (FDR)

Address(es): SCI0.FDR 4007 0016h, SCI1.FDR 4007 0036h, SCI2.FDR 4007 0056h, SCI3.FDR 4007 0076h, SCI4.FDR 4007 0096h, SCI5.FDR 4007 00B6h, SCI6.FDR 4007 00D6h, SCI7.FDR 4007 00F6h, SCI8.FDR 4007 0116h, SCI9.FDR 4007 0136h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	T[4:0]					—	—	—	R[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b4 to b0	R[4:0]	Receive FIFO Data Count	Valid only in asynchronous mode, including multi-processor mode, or clock synchronous mode, when FCR.FM = 1. Indicates the amount of receive data stored in FRDRHL.	R
b7 to b5	—	Reserved	These bits are read as 0.	R

FCR选择FIFO模式，复位FTDRHL和FRDRHL，选择发送或接收的FIFO数据触发数，选择RTS输出激活触发数。

FM位（FIFO模式选择）

当FM位设置为1时，选择FTDRHL和FRDRHL进行通信。当FM位设置为0时，选择TDR和RDR，或TDRHL和RDRHL进行通信。

RFRST位（接收FIFO数据寄存器复位）

当RFRST位设置为1时，FRDRHL寄存器复位，接收数据计数复位为0。当RFRST位写入1时，在1个PCLKA后清为0。

TFRST位（发送FIFO数据寄存器复位）

当TFRST位设置为1时，FTDRHL寄存器复位，发送数据计数复位为0。当TFRST位写入1时，在1个PCLKA后清为0。

DRES位（接收数据就绪错误选择位）

当检测到接收数据就绪错误时，可以从SCIn_RXI中断请求或SCIn_ERI中断请求。当启动DMAC或DTC并读取FRDRH和FRDRL寄存器时，设置DRES位为1。

TTRG[3:0]位（发送FIFO数据触发数）

当FTDRHL中的发送数据量等于或小于TTRG[3:0]位中指定的发送触发数时，TDFE标志设置为1，并且软件可以将数据写入FTDRHL。如果SCR.TIE=1，则发生SCIn_TXI中断请求。

RTRG[3:0]位（接收FIFO数据触发数）

当FRDRHL中的接收数据量等于或大于RTRG[3:0]位中指定的接收触发数时，RDF标志设置为1，并且软件可以从FRDRHL中读取数据。如果SCR.RIE=1，则发生SCIn_RXI中断请求。

当RTRG[3:0]为0时，即使接收FIFO中的数据量等于0，RDF标志也不置位，并且SCIn_RXI中断不发生。

RSTRG[3:0]位（RTS输出有效触发数选择）

当FRDRHL中存储的接收数据量等于或大于RSTRG[3:0]位中指定的接收触发数时，RTS信号变为高电平。

当RSTRG[3:0]为0时，即使FRDRHL中的数据量等于0，RTS信号也不会变高。

34.2.27 FIFO数据计数寄存器(FDR)

Address(es): SCI0.FDR 4007 0016h, SCI1.FDR 4007 0036h, SCI2.FDR 4007 0056h, SCI3.FDR 4007 0076h, SCI4.FDR 4007 0096h, SCI5.FDR 4007 00B6h, SCI6.FDR 4007 00D6h, SCI7.FDR 4007 00F6h, SCI8.FDR 4007 0116h, SCI9.FDR 4007 0136h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	T[4:0]					—	—	—	R[4:0]				
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b4 to b0	R[4:0]	接收FIFO数据计数	仅在异步模式下有效，包括多处理器模式，或时钟同步模式，当FCR.FM=1时。表示FRDRHL中存储的接收数据量。	R
b7 to b5	—	Reserved	这些位读为0。	R

Bit	Symbol	Bit name	Description	R/W
b12 to b8	T[4:0]	Transmit FIFO Data Count	Valid only in asynchronous mode, including multi-processor mode, or clock synchronous mode, when FCR.FM = 1. Indicates the amount of non-transmitted data stored in FTDRHL.	R
b15 to b13	—	Reserved	These bits are read as 0.	R

The FDR register indicates the amount of data stored in FRDRHL and FTDRHL.

R[4:0] bits (Receive FIFO Data Count)

The R[4:0] bits indicate the amount of receive data stored in FRDRHL. 00h means no receive data, and 10h means that the maximum received data is stored in FRDRHL.

T[4:0] bits (Transmit FIFO Data Count)

The T[4:0] bits indicate the amount of non-transmitted data stored in FTDRHL. 00h means no transmit data, and 10h means that all (maximum amount) of the data to be transmitted is stored in FTDRHL.

34.2.28 Line Status Register (LSR)

Address(es): SCI0.LSR 4007 0018h, SCI1.LSR 4007 0038h, SCI2.LSR 4007 0058h, SCI3.LSR 4007 0078h, SCI4.LSR 4007 0098h, SCI5.LSR 4007 00B8h, SCI6.LSR 4007 00D8h, SCI7.LSR 4007 00F8h, SCI8.LSR 4007 0118h, SCI9.LSR 4007 0138h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	PNUM[4:0]					—	FNUM[4:0]					—	ORER
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	ORER	Overrun Error Flag	Valid only in asynchronous mode, including multi-processor mode, or clock synchronous mode, and when FIFO is selected: 0: No overrun error occurred 1: Overrun error occurred.	R*1
b1	—	Reserved	This bit is read as 0.	R
b6 to b2	FNUM[4:0]	Framing Error Count	Indicates the amount of data with a framing error in the receive data stored in FRDRHL.	R
b7	—	Reserved	This bit is read as 0.	R
b12 to b8	PNUM[4:0]	Parity Error Count	Indicates the amount of data with a parity error in the receive data stored in FRDRHL.	R
b15 to b13	—	Reserved	These bits are read as 0.	R

Note 1. Write 0 to SSR_FIFO.ORER to clear the flag.

The LSR register indicates the receive error status.

ORER bit (Overrun Error Flag)

The ORER bit reflects the value in SSR_FIFO.ORER.

FNUM[4:0] bits (Framing Error Count)

The FNUM[4:0] value indicates the amount of data with a framing error stored in the FRDRHL register.

PNUM[4:0] bits (Parity Error Count)

The PNUM[4:0] value indicates the amount of data with a parity error stored in the FRDRHL register.

Bit	Symbol	位名称	Description	R/W
b12 to b8	T[4:0]	发送FIFO数据计数	仅在异步模式下有效，包括多处理器模式或时钟同步模式，当FCR.FM =1时。表示存储在FTDRHL中的未传输数据量。	R
b15 to b13	—	Reserved	这些位读为0。	R

FDR寄存器指示存储在FRDRHL和FTDRHL中的数据量。

R[4:0]位（接收FIFO数据计数）

R[4:0]位指示存储在FRDRHL中的接收数据量。00h表示没有接收数据，10h表示最大接收数据存储在FRDRHL中。

T[4:0]位（发送FIFO数据计数）

T[4:0]位指示存储在FTDRHL中的未传输数据量。00h表示不发送数据，10h表示所有（最大量）要发送的数据都存储在FTDRHL中。

34.2.28 线路状态寄存器(LSR)

Address(es): SCI0.LSR 4007 0018h, SCI1.LSR 4007 0038h, SCI2.LSR 4007 0058h, SCI3.LSR 4007 0078h, SCI4.LSR 4007 0098h, SCI5.LSR 4007 00B8h, SCI6.LSR 4007 00D8h, SCI7.LSR 4007 00F8h, SCI8.LSR 4007 0118h, SCI9.LSR 4007 0138h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	PNUM[4:0]					—	FNUM[4:0]					—	ORER
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	ORER	溢出错误标志	仅在异步模式下有效，包括多处理器模式或时钟同步模式，并且选择FIFO时：0：没有发生超支错误1：超出误差。	R*1
b1	—	Reserved	该位读为0。	R
b6 to b2	FNUM[4:0]	帧错误计数	表示FRDRHL中存储的接收数据中存在帧错误的数据量。	R
b7	—	Reserved	该位读为0。	R
b12 to b8	PNUM[4:0]	奇偶错误计数	表示FRDRHL中存储的接收数据中有奇偶校验错误的数据量。	R
b15 to b13	—	Reserved	这些位读为0。	R

Note 1. 将0写入SSR_FIFO.ORER以清除标志。

LSR寄存器指示接收错误状态。

ORER位（溢出错误标志）

ORER位反映了SSR_FIFO.ORER中的值。

FNUM[4:0]位（帧错误计数）

FNUM[4:0]值表示存储在FRDRHL寄存器中的具有帧错误的数据量。

PNUM[4:0]位（奇偶错误计数）

PNUM[4:0]值表示存储在FRDRHL寄存器中的具有奇偶校验错误的数据量。

34.2.29 Compare Match Data Register (CDR)

Address(es): SCI0.CDR 4007 001Ah, SCI1.CDR 4007 003Ah, SCI2.CDR 4007 005Ah, SCI3.CDR 4007 007Ah, SCI4.CDR 4007 009Ah, SCI5.CDR 4007 00BAh, SCI6.CDR 4007 00DAh, SCI7.CDR 4007 00FAh, SCI8.CDR 4007 011Ah, SCI9.CDR 4007 013Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	CMPD[8:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b8 to b0	CMPD[8:0]	Compare Match Data	Holds compare data pattern for address match wakeup function.	R/W
b15 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The CDR register sets the compare data for the address match function.

CMPD[8:0] bits (Compare Match Data)

The CMPD[8:0] bits set the data to be compared to receive data for the address match function, when the address match function is enabled (DCCR.DCME = 1).

Three bit lengths are available:

- CMPD[6:0] with 7-bit length
- CMPD[7:0] with 8-bit length
- CMPD[8:0] with 9-bit length.

34.2.30 Data Compare Match Control Register (DCCR)

Address(es): SCI0.DCCR 4007 0013h, SCI1.DCCR 4007 0033h, SCI2.DCCR 4007 0053h, SCI3.DCCR 4007 0073h, SCI4.DCCR 4007 0093h, SCI5.DCCR 4007 00B3h, SCI6.DCCR 4007 00D3h, SCI7.DCCR 4007 00F3h, SCI8.DCCR 4007 0113h, SCI9.DCCR 4007 0133h

	b7	b6	b5	b4	b3	b2	b1	b0
	DCME	IDSEL	—	DFER	DPER	—	—	DCMF
Value after reset:	0	1	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	DCMF	Data Compare Match Flag	0: Not matched 1: Matched.	R/(W)*1
b2, b1	—	Reserved	These bits are read as 0. The write value should be 0.	R
b3	DPER	Data Compare Match Parity Error Flag	0: No parity error occurred 1: Parity error occurred.	R/(W)*1
b4	DFER	Data Compare Match Framing Error Flag	0: No framing error occurred 1: Framing error occurred.	R/(W)*1
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6	IDSEL	ID Frame Select	Valid only in asynchronous mode, including multi-processor mode: 0: Always compare data regardless of the MPB bit value 1: Only compare data when MPB bit = 1 (ID frame).	R/W
b7	DCME	Data Compare Match Enable	Valid only in asynchronous mode, including multi-processor mode: 0: Disable address match function 1: Enable address match function.	R/W

Note 1. Only 0 can be written, to clear the flag after reading 1.

34.2.29 比较匹配数据寄存器(CDR)

Address(es): SCI0.CDR 4007 001Ah, SCI1.CDR 4007 003Ah, SCI2.CDR 4007 005Ah, SCI3.CDR 4007 007Ah, SCI4.CDR 4007 009Ah, SCI5.CDR 4007 00BAh, SCI6.CDR 4007 00DAh, SCI7.CDR 4007 00FAh, SCI8.CDR 4007 011Ah, SCI9.CDR 4007 013Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	CMPD[8:0]								
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b8 to b0	CMPD[8:0]	比较匹配数据	保存地址匹配唤醒功能的比较数据模式。	R/W
b15 to b9	—	Reserved	这些位被读取为0。写入值应为0。	R/W

CDR寄存器设置地址匹配功能的比较数据。

CMPD[8:0]位（比较匹配数据）

当地址匹配功能启用时（DCCR.DCME=1），CMPD[8:0]位设置要比较的数据以接收地址匹配功能的数据。

提供三种位长：

- 7位长度的CMPD[6:0]
- CMPD[7:0]8位长度
- CMPD[8:0]，长度为9位。

34.2.30 数据比较匹配控制寄存器(DCCR)

Address(es): SCI0.DCCR 4007 0013h, SCI1.DCCR 4007 0033h, SCI2.DCCR 4007 0053h, SCI3.DCCR 4007 0073h, SCI4.DCCR 4007 0093h, SCI5.DCCR 4007 00B3h, SCI6.DCCR 4007 00D3h, SCI7.DCCR 4007 00F3h, SCI8.DCCR 4007 0113h, SCI9.DCCR 4007 0133h

	b7	b6	b5	b4	b3	b2	b1	b0
	DCME	IDSEL	—	DFER	DPER	—	—	DCMF
重置后的值:	0	1	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	DCMF	数据比较匹配标志	0：不匹配1： 匹配。	R/(W)*1
b2, b1	—	Reserved	这些位被读取为0。写入值应为0。	R
b3	DPER	数据比较匹配奇偶校验 错误标志	0：未发生奇偶校验错误1 ：发生奇偶校验错误。	R/(W)*1
b4	DFER	数据比较匹配 成帧错误标志	0：未发生帧错误1：发生帧 错误。	R/(W)*1
b5	—	Reserved	该位读取为0。写入值应为0。	R/W
b6	IDSEL	ID帧选择	仅在异步模式下有效，包括多处理器模式：0：无论MPB位值如何 ，始终比较数据1：仅当MPB位=1（ID帧）时比较数据。	R/W
b7	DCME	数据比较匹配 Enable	仅在异步模式下有效，包括多处理器模式：0：禁用地址匹配功能1 ：启用地址匹配功能。	R/W

Note 1. 只能写入0，读取1后清除标志。

The DCCR register controls the address match function.

DCMF flag (Data Compare Match Flag)

The DCMF flag indicates that the SCI detected a receive data match with the comparison data (CDR.CMPD).

[Setting condition]

- On match of the comparison data (CDR.CMPD) with the receive data when DCCR.DCME = 1.

[Clearing condition]

- When 0 is written after 1 is read from DCMF.

Clearing the SCR.RE bit to 0 does not affect the DCMF flag, which retains its previous value.

DPER flag (Data Compare Match Parity Error Flag)

The DPER flag indicates that a parity error occurred on address match detection (receive data match detection).

[Setting condition]

- When a parity error is detected in a frame in which an address match is detected.

[Clearing conditions]

- When 0 is written after 1 is read from DPER.

When the SCR.RE bit is set to 0 (serial reception is disabled), the DPER flag is not affected and retains its previous value.

DFER flag (Data Compare Match Framing Error Flag)

The DFER flag indicates that a framing error occurred on address match detection (receive data match detection).

[Setting conditions]

- When a stop bit of a frame in which an address match is detected is 0.

  When in 2-stop-bit mode, only the first bit of the stop bits is checked for a value of 1 (the second stop bit is not checked).

[Clearing conditions]

- When 0 is written after 1 is read from DFER.

When the SCR.RE bit is set to 0 (serial reception is disabled), the DFER flag is not affected and retains its previous value.

IDSEL bit (ID Frame Select)

The IDSEL bit selects whether to compare data regardless of the MPB bit value or to compare data only when MPB = 1 (ID frame), when the address match function is enabled.

DCME bit (Data Compare Match Enable)

The DCME bit enables or disables the address match function (data compare match function).

If the SCI detects a match to the comparison data (CDR.CMPD) with the receive data, the DCME bit clears automatically, after which SCI operation mode is in receive mode without data compare match function. See section 34.3.6, Address Match (Receive Data Match Detection) Function.

The write value must be 0 for all modes other than asynchronous mode.

DCCR寄存器控制地址匹配功能。

DCMF标志（数据比较匹配标志）

DCMF标志表示SCI检测到接收数据与比较数据(CDR.CMPD)匹配。

[Setting condition]

- 当DCCR.DCME=1时，比较数据(CDR.CMPD)与接收数据匹配。

[Clearing condition]

- 从DCMF读取1后写入0时。

将SCR.RE位清除为0不会影响DCMF标志，它保留其先前的值。

DPER标志（数据比较匹配奇偶校验错误标志）

DPER标志表示在地址匹配检测（接收数据匹配检测）时发生奇偶校验错误。

[Setting condition]

- 在检测到地址匹配的帧中检测到奇偶校验错误时。

[Clearing conditions]

- 当从DPER读取1后写入0。

当SCR.RE位设置为0（禁用串行接收）时，DPER标志不受影响并保留其先前的值。

DFER标志（数据比较匹配成帧错误标志）

DFER标志表示在地址匹配检测（接收数据匹配检测）时发生了帧错误。

[Setting conditions]

- 当检测到地址匹配的帧的停止位为0时。

在2停止位模式下，仅检查停止位的第一位是否为1（不检查第二个停止位）。【清算条件】

- 从DFER读取1后写入0。

当SCR.RE位设置为0（禁用串行接收）时，DFER标志不受影响并保留其先前的值。

IDSEL位（ID帧选择）

IDSEL位选择无论MPB位值如何比较数据，还是仅在MPB=1（ID帧）时比较数据，当地址匹配功能启用时。

DCME位（数据比较匹配使能）

DCME位启用或禁用地址匹配功能（数据比较匹配功能）。

如果SCI检测到比较数据（CDR.CMPD）与接收数据匹配，则DCME位自动清零，此后SCI操作模式为接收模式，没有数据比较匹配功能。请参见第34.3.6节，地址匹配（接收数据匹配检测）功能。

对于异步模式以外的所有模式，写入值必须为0。

34.2.31 Serial Port Register (SPTR)

Address(es): SCI0.SPTR 4007 001Ch, SCI1.SPTR 4007 003Ch, SCI2.SPTR 4007 005Ch, SCI3.SPTR 4007 007Ch, SCI4.SPTR 4007 009Ch, SCI5.SPTR 4007 00BCh, SCI6.SPTR 4007 00DCh, SCI7.SPTR 4007 00FCh, SCI8.SPTR 4007 011Ch, SCI9.SPTR 4007 013Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	SPB2IO	SPB2DT	RXDMON
Value after reset:	0	0	0	0	0	0	1	1

Bit	Symbol	Bit name	Description	R/W
b0	RXDMON	Serial Input Data Monitor	Indicates the state of the RXDn pin: 0: RXDn pin is low 1: RXDn pin is high.	R
b1	SPB2DT	Serial Port Break Data Select	Selects the output level of the TXDn pin when SCR.TE = 0: 0: Output low level on TXDn pin 1: Output high level on TXDn pin.	R/W
b2	SPB2IO	Serial Port Break I/O	Selects whether the value of SPB2DT is output to TXDn pin: 0: Do not output value of SPB2DT bit on TXDn pin 1: Output value of SPB2DT bit on TXDn pin.	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The SPTR register provides confirmation of the serial reception pin (RXDn pin) status and sets the transmission pin (TXDn pin) status.

This register can only be used in asynchronous mode.

The TXDn pin status is determined by the combination of SCR.TE, SPTR.SPB2IO, and SPTR.SPB2DT settings, as shown in Table 34.22.

Table 34.22 TXDn pin status

Value of SCR.TE	Value of SPTR.SPB2IO	Value of SPTR.SPB2DT	TXDn pin status
0	0	x	Hi-Z (initial value)
0	1	0	Low level output
0	1	1	High level output
1	x	x	Serial transmit data is output

x: Don’t care.

Note: Use the SPTR register in asynchronous mode only. Using this register in any other mode is not guaranteed.

34.3 Operation in Asynchronous Mode

Figure 34.2 shows the general format for asynchronous serial communications. One frame consists of a start bit (low level), transmit or receive data, a parity bit, and stop bits (high level). In asynchronous serial communications, the communications line is held in the mark state (high level) when not communicating.

The SCI monitors the communications line. When the SCI detects a low, it regards that as a start bit and starts serial communication.

Inside the SCI, the transmitter and receiver are independent units, enabling full-duplex communications. Both the transmitter and receiver have a double-buffered structure in addition to FIFO mode, so that data can be read or written during transmission or reception, enabling continuous data transmission and reception.

34.2.31 串行端口寄存器(SPTR)

Address(es): SCI0.SPTR 4007 001Ch, SCI1.SPTR 4007 003Ch, SCI2.SPTR 4007 005Ch, SCI3.SPTR 4007 007Ch, SCI4.SPTR 4007 009Ch, SCI5.SPTR 4007 00BCh, SCI6.SPTR 4007 00DCh, SCI7.SPTR 4007 00FCh, SCI8.SPTR 4007 011Ch, SCI9.SPTR 4007 013Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	SPB2IO	SPB2DT	RXDMON
重置后的值：	0	0	0	0	0	0	1	1

Bit	Symbol	位名称	Description	R/W
b0	RXDMON	串行输入数据监视器	指示RXDn引脚的状态：0：RXDn引脚为低电平1：RXDn引脚为高电平。	R
b1	SPB2DT	串口中断数据Select	选择SCR.TE=0时TXDn引脚的输出电平：0：TXDn引脚输出低电平1：TXDn引脚输出高电平。	R/W
b2	SPB2IO	串口中断IO	选择是否将SPB2DT的值输出到TXDn引脚：0：不输出TXDn引脚上的SPB2DT位的值1：输出TXDn引脚上的SPB2DT位的值。	R/W
b7 to b3	—	Reserved	这些位被读取为0。写入值应为0。	R/W

SPTR寄存器提供串行接收引脚（RXDn引脚）状态的确认并设置发送引脚（TXDn引脚）状态。

该寄存器只能在异步模式下使用。

TXDn引脚状态由SCR.TE、SPTR.SPB2IO和SPTR.SPB2DT设置的组合决定，如表34.22所示。

Table 34.22 TXDn引脚状态

SCR.TE的价值	的价值SPTR.SPB2IO	的价值SPTR.SPB2DT	TXDn引脚状态
0	0	x	Hi-Z (initial value)
0	1	0	低电平输出
0	1	1	高电平输出
1	x	x	串行传输数据输出

x: Don’t care.

Note: 仅在异步模式下使用SPTR寄存器。不保证在任何其他模式下使用该寄存器。

34.3 异步模式下的操作

图34.2显示了异步串行通信的一般格式。一帧由起始位（低电平）、发送或接收数据、奇偶校验位和停止位（高电平）组成。在异步串行通信中，通信线在不通信时保持在标记状态（高电平）。

SCI监控通信线路。当SCI检测到低电平时，将其视为起始位并开始串行通信。

在SCI内部，发射器和接收器是独立的单元，可实现全双工通信。发送器和接收器除了FIFO模式外，都具有双缓冲结构，从而可以在发送或接收过程中读取或写入数据，从而实现数据的连续发送和接收。

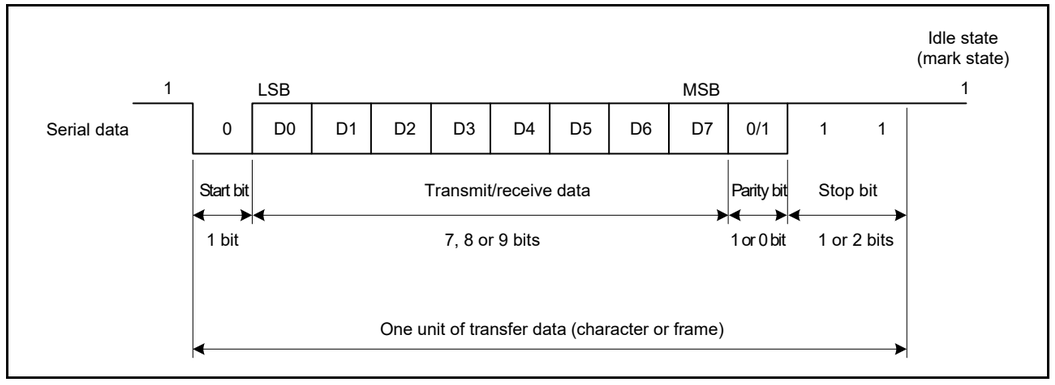


Figure 34.2 Data format in asynchronous serial communications with 8-bit data, parity bit, and 2 stop bits

34.3.1 Serial Data Transfer Format

Table 34.23 lists the serial data transfer formats that can be used in asynchronous mode. Any of 18 transfer formats can be selected with the SMR and SCMR register settings. For details on the multi-processor function, see section 34.4, Multi-Processor Communication Function.

Table 34.23 Serial transfer formats in asynchronous mode (1 of 2)

SCMR setting	SMR setting				Serial transfer format and frame length
CHR1	CHR	PE	MP	STOP	1 2 3 4 5 6 7 8 9 10 11 12 13
0	0	0	0	0	S 9-bit data STOP
0	0	0	0	1	S 9-bit data STOP STOP
0	0	1	0	0	S 9-bit data P STOP
0	0	1	0	1	S 9-bit data P STOP STOP
1	0	0	0	0	S 8-bit data STOP
1	0	0	0	1	S 8-bit data STOP STOP

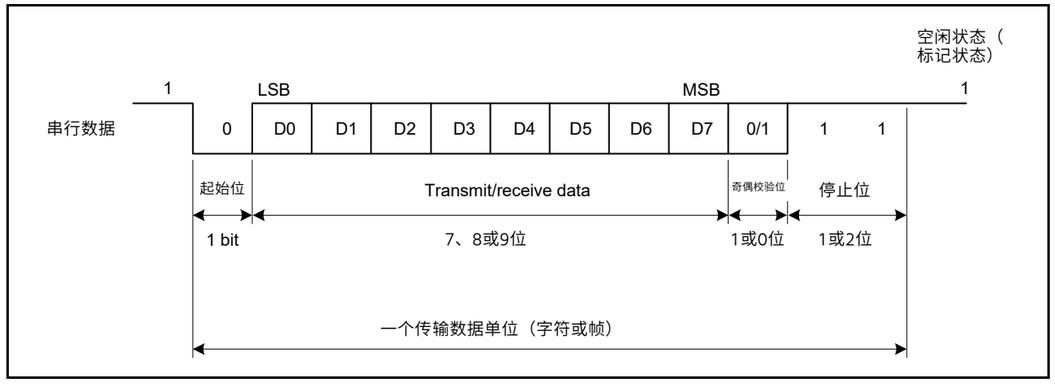


Figure 34.2 异步串行通信中的数据格式，包含8位数据、奇偶校验位和2个停止位

34.3.1 串行数据传输格式

表34.23列出了可以在异步模式下使用的串行数据传输格式。可以通过SMR和SCMR寄存器设置选择18种传输格式中的任何一种。有关多处理器功能的详细信息，请参阅第34.4节，多处理器通信功能。

Table 34.23 异步模式下的串行传输格式（1of2）

SCMR setting	SMR setting				串行传输格式和帧长
CHR1	CHR	PE	MP	STOP	1 2 3 4 5 6 7 8 9 10 11 12 13
0	0	0	0	0	S 9-bit data STOP
0	0	0	0	1	S 9-bit data STOP STOP
0	0	1	0	0	S 9-bit data P STOP
0	0	1	0	1	S 9-bit data P STOP STOP
1	0	0	0	0	S 8-bit data STOP
1	0	0	0	1	S 8-bit data STOP STOP

Table 34.23 Serial transfer formats in asynchronous mode (2 of 2)

SCMR setting	SMR setting				Serial transfer format and frame length
CHR1	CHR	PE	MP	STOP	1 2 3 4 5 6 7 8 9 10 11 12 13
1	0	1	0	0	S | 8-bit data | P | STOP
1	0	1	0	1	S | 8-bit data | P | STOP | STOP
1	1	0	0	0	S | 7-bit data | STOP
1	1	0	0	1	S | 7-bit data | STOP | STOP
1	1	1	0	0	S | 7-bit data | P | STOP
1	1	1	0	1	S | 7-bit data | P | STOP | STOP
0	0	—	1	0	S | 9-bit data | MPB | STOP
0	0	—	1	1	S | 9-bit data | MPB | STOP STOP
1	0	—	1	0	S | 8-bit data | MPB | STOP
1	0	—	1	1	S | 8-bit data | MPB | STOP | STOP
1	1	—	1	0	S | 7-bit data | MPB | STOP
1	1	—	1	1	S | 7-bit data | MPB | STOP | STOP

S: Start bit
STOP: Stop bit
P: Parity bit

Table 34.23 异步模式下的串行传输格式(2of2)

SCMR setting	SMR setting				串行传输格式和帧长
CHR1	CHR	PE	MP	STOP	1 2 3 4 5 6 7 8 9 10 11 12 13
1	0	1	0	0	S | 8-bit data | P | STOP
1	0	1	0	1	S | 8-bit data | P | STOP | STOP
1	1	0	0	0	S | 7-bit data | STOP
1	1	0	0	1	S | 7-bit data | STOP | STOP
1	1	1	0	0	S | 7-bit data | P | STOP
1	1	1	0	1	S | 7-bit data | P | STOP | STOP
0	0	—	1	0	S | 9-bit data | MPB | STOP
0	0	—	1	1	S | 9-bit data | MPB | STOP STOP
1	0	—	1	0	S | 8-bit data | MPB | STOP
1	0	—	1	1	S | 8-bit data | MPB | STOP | STOP
1	1	—	1	0	S | 7-bit data | MPB | STOP
1	1	—	1	1	S | 7-bit data | MPB | STOP | STOP

S: 起始位
STOP: 停止位
P: 奇偶校验位

MPB: Multi-processor bit

34.3.2 Receive Data Sampling Timing and Reception Margin in Asynchronous Mode

In asynchronous mode, the SCI operates on a base clock with a frequency of 16 times*1 the bit rate.

In reception, the SCI samples the falling edge of the start bit using the base clock, and performs synchronization.

Because receive data is sampled on the rising edge of the 8th pulse*1 of the base clock, data is latched at the middle of each bit, as shown in Figure 34.3. The reception margin in asynchronous mode is determined by the following formula (1):

$$M = \left| (0.5 - \frac{1}{2N}) - (L - 0.5)\ F - \frac{\lfloor D - 0.5 \rfloor}{N}\ (1 + F) \right| \times 100\ [\%] \cdots \text{Formula (1)}$$

M: Reception margin
N: Ratio of bit rate to clock
(N = 16 when SEMR.ABCSE = 0 and SEMR.ABCS = 0. N = 8 when SEMR.ABCS = 1. N = 6 when SEMR.ABCSE = 1.)
D: Duty cycle of clock (D = 0.5 to 1.0)
L: Frame length (L = 9 to 13)
F: Absolute value of clock frequency deviation

Assuming values of F = 0 and D = 0.5 in formula (1), the reception margin is determined using the following formula:

$M = \{0.5 - 1/(2 \times 16)\} \times 100\ (\%) = 46.875\%$

This represents the computed value. Renesas recommends a margin of 20% to 30% in system design.

Note 1. In this example, the SEMR.ABCS bit is 0 and the SEMR.ABCSE is 0. When the ABCS bit is 1 and the ABCSE bit is 0, a frequency of 8 times the bit rate is used as a base clock, and receive data is sampled on the rising edge of the 4th pulse of the base clock.
When the ABCSE bit is 1, a sextuple frequency of a bit rate is used as a base clock, and receive data is sampled on the rising edge of the 3rd pulse of the base clock.

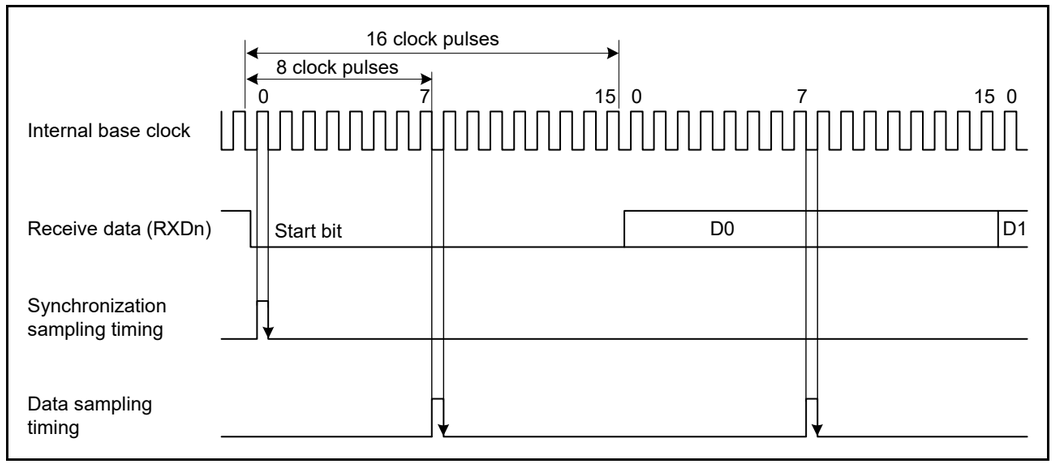


Figure 34.3 Receive data sampling timing in asynchronous mode

34.3.3 Clock

Either an internal clock generated by the on-chip baud rate generator or an external clock input to the SCKn pin can be selected as the transfer clock of the SCI, based on the SMR.CM and SCR.CKE[1:0] settings.

When an external clock is input to the SCKn pin, the clock frequency must be 16 times the bit rate (when SEMR.ABCS = 0) or 8 times the bit rate (when SEMR.ABCS = 1).

MPB: Multi-processor bit

34.3.2 异步模式下接收数据采样时序和接收余量

在异步模式下，SCI在频率为16倍*1比特率的基本时钟上运行。

在接收时，SCI使用基本时钟对起始位的下降沿进行采样，并执行同步。

因为接收数据是在基本时钟的第8个脉冲*1的上升沿采样的，所以数据在每个位的中间锁存，如图34.3所示。异步模式下的接收余量由以下公式（1）确定：

$$M = \left| (0.5 - \frac{1}{2N}) - (L - 0.5)\ F - \frac{\lfloor D - 0.5 \rfloor}{N}\ (1 + F) \right| \times 100\ [\%] \cdots \text{Formula (1)}$$

M：接收余量
N：比特率与时钟的比率（当SEMR.ABCSE=0和SEMR.ABCS=0时，N=16。当SEMR.ABCS=1时，N=8。当SEMR.ABCSE=1时，N=6。）D：占空比时钟（D=0.5到1.0）

L：帧长（L=9到13）
F：时钟频率偏差的绝对值

假设公式（1）中的F=0和D=0.5的值，接收裕量使用以下公式确定：

$M = \{0.5 - 1/(2 \times 16)\} \times 100\ (\%) = 46.875\%$

这表示计算值。瑞萨建议在系统设计中留出20%到30%的余量。

注1.本例中，SEMR.ABCS位为0，SEMR.ABCSE位为0。当ABCS位为1，ABCSE位为0时，使用8倍比特率的频率作为基准时钟，并在基本时钟的第4个脉冲的上升沿对接收数据进行采样。当ABCSE位为1时，以比特率的六倍频为基准时钟，在基准时钟的第3个脉冲的上升沿对接收数据进行采样。

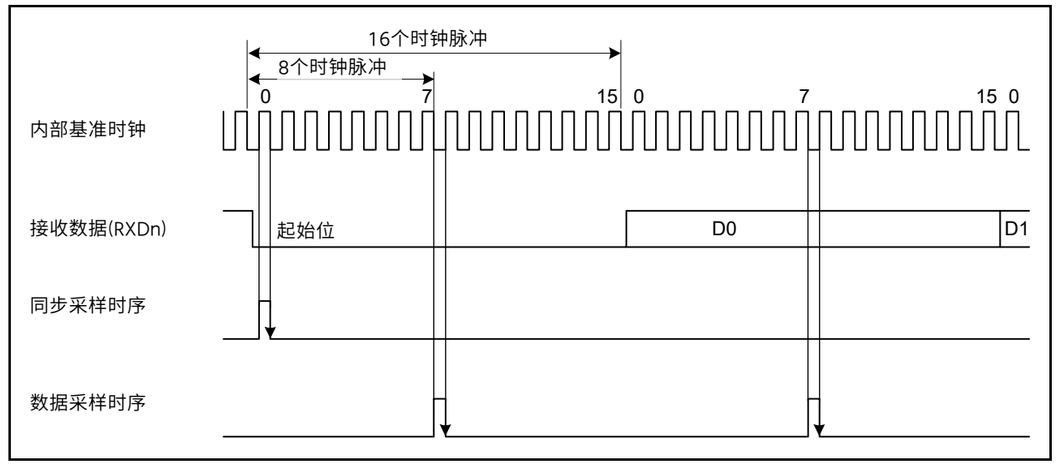


Figure 34.3 异步模式下接收数据采样时序

34.3.3 Clock

根据SMR.CM和SCR.CKE[1:0]设置，可以选择片内波特率发生器产生的内部时钟或输入到SCKn引脚的外部时钟作为SCI的传输时钟。

当外部时钟输入到SCKn引脚时，时钟频率必须为比特率的16倍（SEMR.ABCS=0时）或比特率的8倍（SEMR.ABCS=1时）。

When the SCI uses its internal clock, the clock can be output from the SCKn pin. The frequency of the clock output in this case is equal to the bit rate, and the phase is configured so that the rising edge of the clock is in the middle of the transmit data, as shown in Figure 34.4.

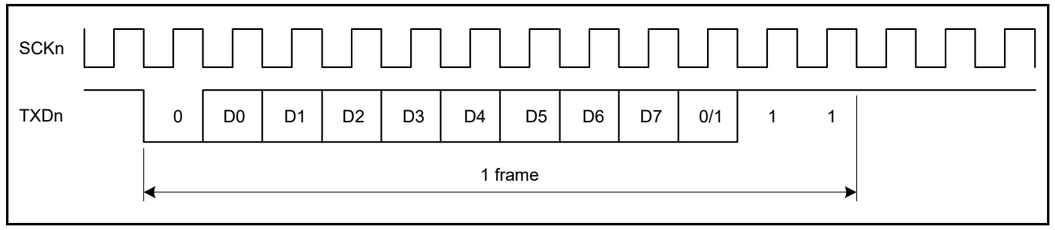


Figure 34.4 Phase relationship between output clock and transmit data in asynchronous mode when SMR.CHR = 0, PE = 1, MP = 0, and STOP = 1

34.3.4 Double-Speed Operation and Frequency of 6 Times the Bit Rate

When the SEMR.ABCS bit is set to 1 and eight pulses of the base clock for a 1-bit period is selected, the SCI operates on the bit rate twice that of when ABCS is set to 0. When the SEMR.BGDM bit is set to 1, the cycle of the base clock is half and the bit rate is double that of when BGDM is set to 0. When the SCR.CKE[1] bit is set to 0 and the on-chip baud rate generator is selected, setting the ABCS and BGDM bits to 1 allows the SCI to operate at a bit rate four times that when the ABCS and BGDM bits are set to 0. When the SEMR.ABCSE bit is set to 1, the number of basic clock pulses is 6 during a period of 1 bit, and the SCI operates at a bit rate 16/3 times that when SEMR.ABCS = 0, SEMR.BGDM = 0, and SMER.ABCSE = 0.

As shown by Formula (1) in section 34.3.2, Receive Data Sampling Timing and Reception Margin in Asynchronous Mode, the reception margin decreases when the SEMR.ABCS or SEMR.ABCSE bit in SEMR is set to 1. Therefore, if the target bit rate can be obtained with ABCS or ABCSE set to 0, it is recommended that you use the SCI with ABCS and ABCSE set to 0.

34.3.5 CTS and RTS Functions

The CTS function uses input on the CTSn_RTSn pin in transmission control. Setting the SPMR.CTSE bit to 1 enables the CTS function. When the CTS function is enabled, placing a low level on the CTSn_RTSn pin causes transmission to start.

Driving the CTSn_RTSn pin high while transmission is in progress does not affect transmission of the current frame.

In the RTS function, which uses output on the CTSn_RTSn pin, a low level is output when reception becomes possible. Conditions for output of the low and high levels are shown in this section.

[Conditions for low-level output]

(a) Non-FIFO selected when all of the following conditions are satisfied

- The value of the SCR.RE bit is 1
- Reception is not in progress
- There is no received data yet to be read
- The ORER, FER, and PER flags in the SSR register are all 0.

(b) FIFO selected when all of the following conditions are satisfied

- The value of the SCR.RE bit is 1
- The amount of receive data written in FRDRHL is equal to or less than the specified receive triggering number
- The ORER bit in the SSR_FIFO register (ORER in FRDRH) is 0.

当SCI使用其内部时钟时，时钟可以从SCKn引脚输出。在这种情况下，时钟输出的频率等于比特率，并配置相位，使时钟的上升沿位于发送数据的中间，如图34.4所示。

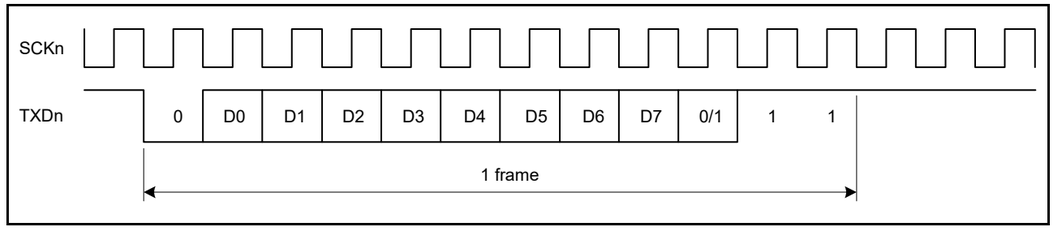


Figure 34.4 异步模式下输出时钟与传输数据的相位关系 SMR.CHR=0，PE=1，MP=0，STOP=1

34.3.4 双倍速操作和6倍比特率的频率

当SEMR.ABCS位设置为1并选择1位周期的8个基本时钟脉冲时，SCI以ABCS设置为0时的两倍比特率运行。当SEMR.BGDM位为设置为1，基本时钟的周期是BGDM设置为0时的一半，比特率是两倍。当SCR.CKE[1]位设置为0并且选择片内波特率发生器时，将ABCS和BGDM位设置为1允许SCI以ABCS和BGDM位设置为0时的四倍的比特率运行。当SEMR.ABCSE位设置为1时，基本时钟脉冲数为6在1位周期内，SCI以16的比特率运行，是SEMR.ABCS=0、SEMR.BGDM=0和SMER.ABCSE=0时的3倍。

如34.3.2节，异步接收数据采样时序和接收裕度中的公式（1）所示模式下，SEMR中的SEMR.ABCS或SEMR.ABCSE位设置为1时，接收余量减小。因此，如果将ABCS或ABCSE设置为0即可获得目标码率，建议您使用SCI与ABCS和ABCSE设置为0。

34.3.5 CTS和RTS函数

CTS功能在传输控制中使用CTSn_RTSn引脚上的输入。将SPMR.CTSE位设置为1可启用CTS功能。当CTS功能使能时，将CTSn_RTSn引脚置于低电平会导致传输开始。

在传输过程中将CTSn_RTSn引脚驱动为高电平不会影响当前帧的传输。

在使用CTSn_RTSn引脚输出的RTS功能中，当可以接收时输出低电平。
本节显示了低电平和高电平的输出条件。

[Conditions for low-level output]

(a) 满足以下所有条件时选择非FIFO

- SCR.RE位的值为1
- 接收未进行
- 没有接收到的数据尚未读取
- SSR寄存器中的ORER、FER和PER标志位均为0。

(b) 满足以下所有条件时选择FIFO

- SCR.RE位的值为1
- FRDRHL中写入的接收数据量等于或小于指定的接收触发数
- SSR_FIFO寄存器中的ORER位（FRRDH中的ORER）为0。

[Condition for high-level output]

(a Non-FIFO selected

- The conditions for low-level output are not satisfied
- When reception is terminated with SCR.RE = 0 without reading the RDR register after reception is complete, RTS remains high. At this time, read the SCR register for dummy values after writing 0 to SCR.RE.

(b) FIFO selected

- The conditions for low-level output are not satisfied.

34.3.6 Address Match (Receive Data Match Detection) Function

The address match function can be used only in asynchronous mode.

If the DCCR.DCME bit is set to 1*4, when one frame of data is received, the SCI compares that received data with the data set in CDR.CMPD. If the SCI detects a match to the comparison data (CDR.CMPD*3) with the received data, the SCI can issue the SCIn_RXI interrupt request.

If the SMR.MP bit is set to 0, comparison occurs only for valid data in receive format. In multi-processor mode (SMR.MP bit = 1), if the DCCR.IDSEL bit is set to 1, receive data where the MPB bit is 1 is subject to comparison for address match and receive data where the MPB bit is 0 is always treated as a mismatch.

If the DCCR.IDSEL bit is set to 0, SCI performs address match detection regardless of the MPB bit value of the received data. Until SCI detects a match between the comparison data (CDR.CMPD*3) and the receive data, the received data is skipped (discarded), and the SCI cannot detect a parity error or framing error.

When SCI detects a match, the DCCR.DCME bit is automatically cleared, and the DCCR.DCMF flag is set to 1. If the DCCR.IDSEL bit is set to 1, the SCR.MPIE bit is automatically cleared. If DCCR.IDSEL is set to 0, the value of the SCR.MPIE bit is retained. If the SCR.RIE bit is set to 1, the SCI issues an SCIn_RXI interrupt request.

If the SCI detects a framing error in the receive data for which a match is detected, the DCCR.DFER bit is set to 1, and if the SCI detects a parity error in that frame, the DCCR.DPER bit is set to 1. The compared receive data is not stored in the RDR register*1, and SSR.RDRF remains 0.*2

After the SCI detects a match, and DCCR.DCME is automatically cleared, the SCI receives the next data continuously based on the current register setting.

When the DCCR.DFER or DCCR.DPER flag is set, the address match is not performed. Before enabling the address match function, set the DCCR.DFER and DCCR.DPER flags to 0.

Examples of the address match function are shown in Figure 34.5 and Figure 34.6.

Note 1. When FCR.FM = 1, this refers to the FRDRHL register.
Note 2. When FCR.FM = 1, this refers to the SSR_FIFO.RDF flag.
Note 3. This comparative target can select one length of 3 types: CMPD[6:0] with 7-bit length, CMPD[7:0] with 8-bit length, and CMPD[8:0] with 9-bit length.
Note 4. Set the DCCR.DCME bit to 1 before receiving the start bit of the received frame that performs address matching.

[Condition for high-level output]

(a Non-FIFO selected

- 不满足低电平输出的条件
- 当接收结束后接收结束且SCR.RE=0且未读取RDR寄存器时，RTS保持高电平。此时，将0写入SCR.RE后，读取SCR寄存器的虚拟值。

(b) FIFO selected

- 不满足低电平输出的条件。

34.3.6 地址匹配（接收数据匹配检测）功能

地址匹配功能只能在异步模式下使用。

如果DCCR.DCME位设置为1*4，当接收到一帧数据时，SCI会将接收到的数据与CDR.CMPD中设置的数据进行比较。如果SCI检测到比较数据(CDR.CMPD*3)与接收到的数据匹配，则SCI可以发出SCIn_RXI中断请求。

如果SMR.MP位设置为0，则仅对接收格式的有效数据进行比较。在多处理器模式下（SMR.MP位=1），如果DCCR.IDSEL位设置为1，则接收MPB位为1的数据进行地址匹配比较，接收MPB位为0的数据总是被视为不匹配。

如果DCCR.IDSEL位设置为0，SCI执行地址匹配检测，而不管接收数据的MPB位值如何。直到SCI检测到比较数据（CDR.CMPD*3）与接收数据匹配，接收数据被跳过（丢弃），SCI无法检测奇偶校验错误或成帧错误。

当SCI检测到匹配时，自动清除DCCR.DCME位，并将DCCR.DCMF标志设置为1。如果DCCR.IDSEL位设置为1，SCR.MPIE位自动清零。如果DCCR.IDSEL设置为0，则SCR.MPIE位被保留。如果SCR.RIE位设置为1，则SCI发出SCIn_RXI中断请求。

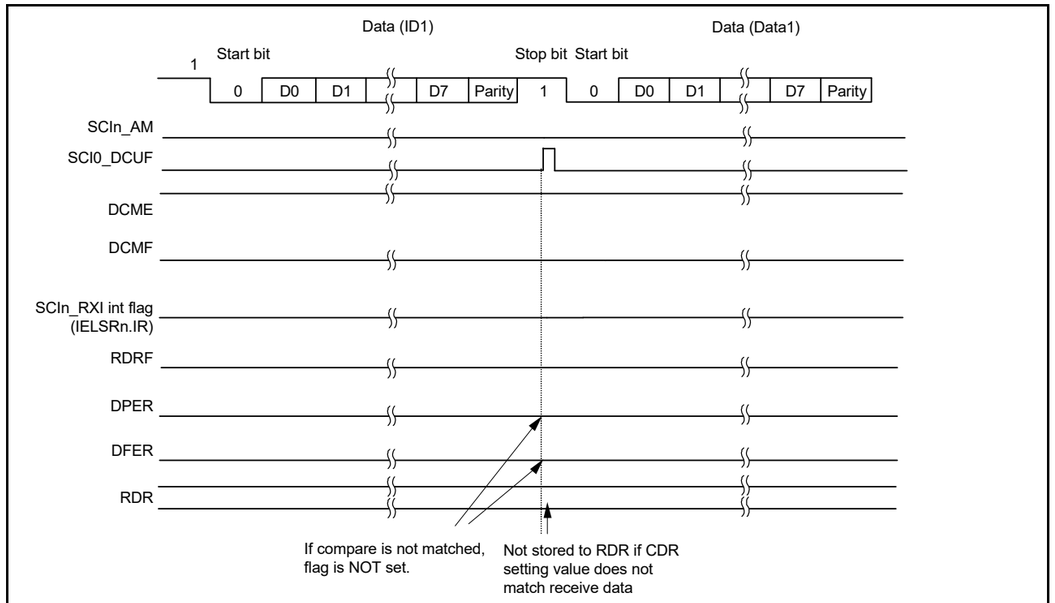
如果SCI在检测到匹配的接收数据中检测到帧错误，则DCCR.DFER位设置为1，如果SCI在该帧中检测到奇偶校验错误，则DCCR.DPER位设置为1。比较后的接收数据不存入RDR寄存器*1，SSR.RDRF保持为0。*2

SCI检测到匹配后，DCCR.DCME自动清零，SCI根据当前寄存器设置连续接收下一个数据。

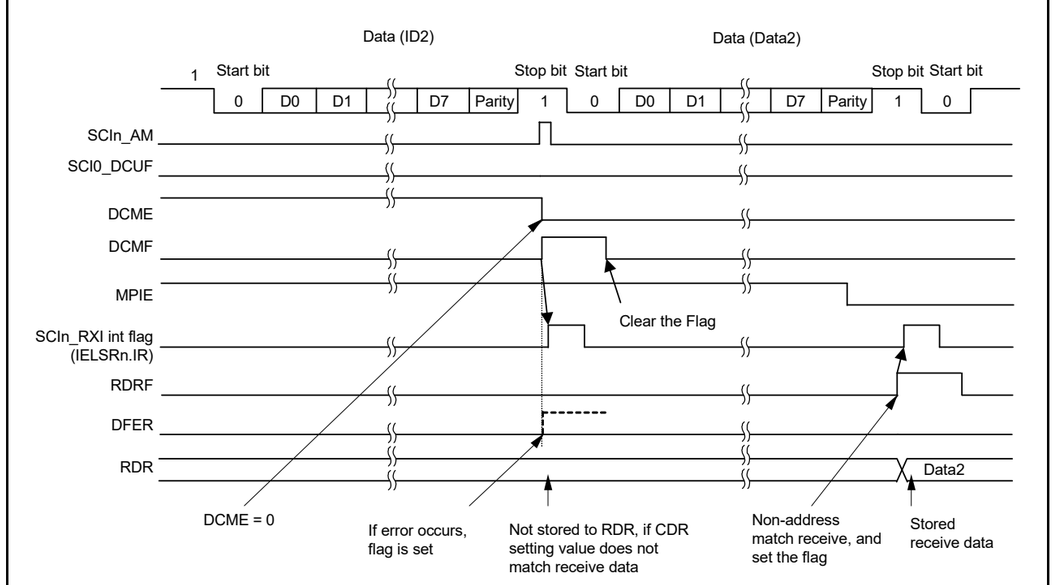
当设置DCCR.DFER或DCCR.DPER标志时，不执行地址匹配。在启用地址匹配功能之前，将DCCR.DFER和DCCR.DPER标志设置为0。

地址匹配函数的例子如图34.5和图34.6所示。

注1.当FCR.FM=1时，指的是FRDRHL寄存器。
注2.当FCR.FM=1时，这指的是SSR_FIFO.RDF标志。
注3.此比较目标可以选择3种长度中的一种：7位长度的CMPD[6:0]、8位长度的CMPD[7:0]和9位长度的CMPD[8:0].注4.在接收到执行地址匹配的接收帧的起始位之前，将DCCR.DCME位设置为1。

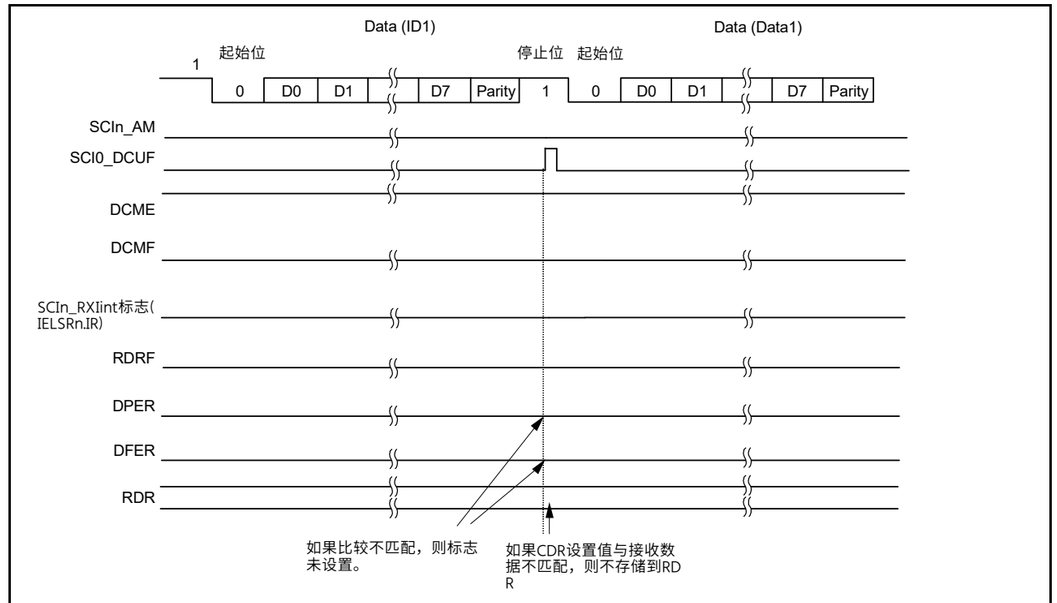


(a) Example of compare non-match between receive data and CDR (8-bit length/parity/non-multi processor mode)

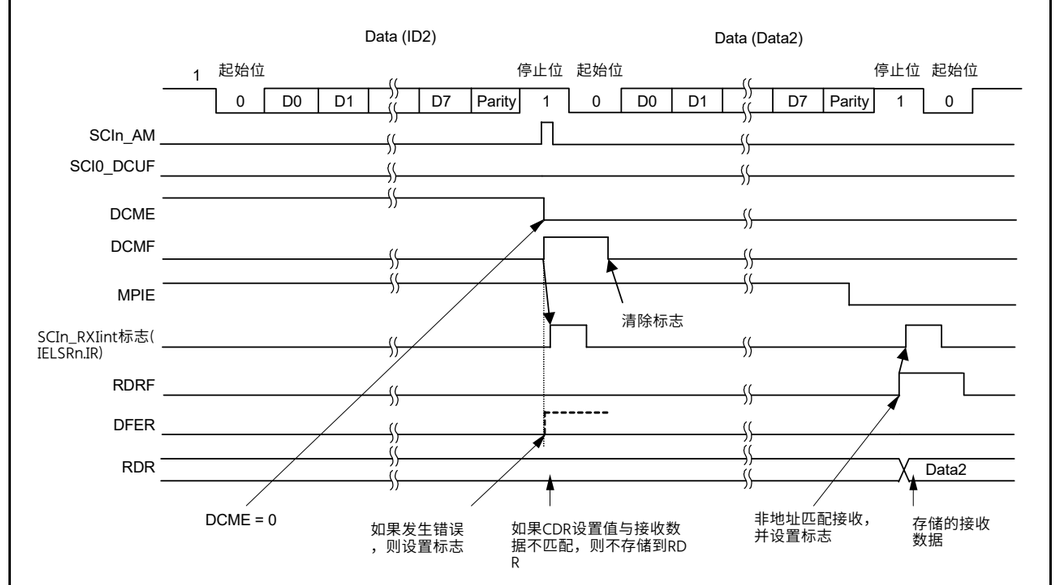


(b) Example of compare match between receive data and CDR (8-bit length/parity/non-multi processor mode)

Figure 34.5 Example of address match (1) non-multi processor mode

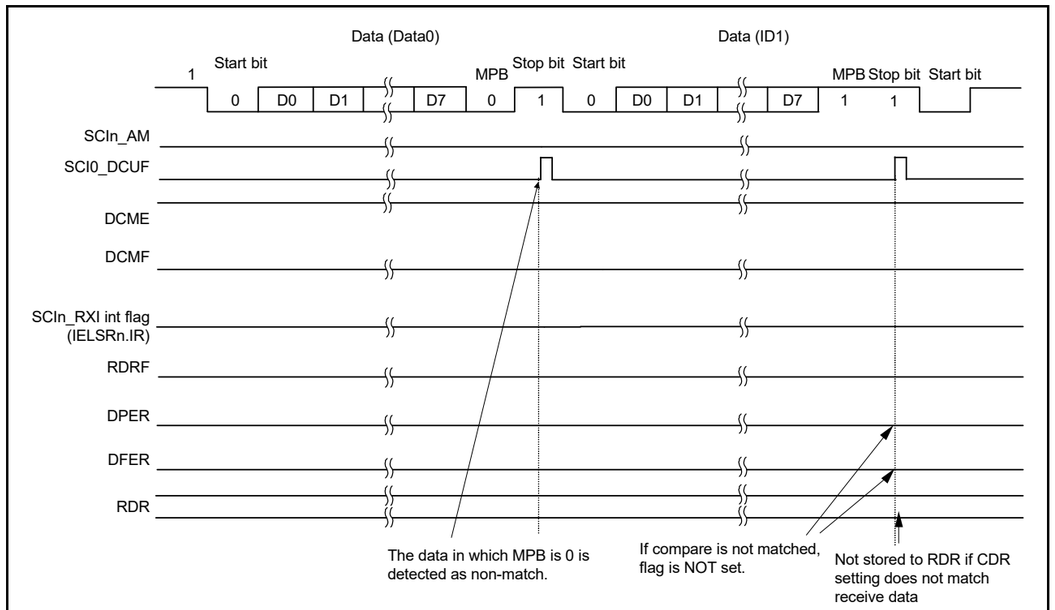


(a)接收数据和CDR比较不匹配的示例（8位长度奇偶校验非多处理器模式）

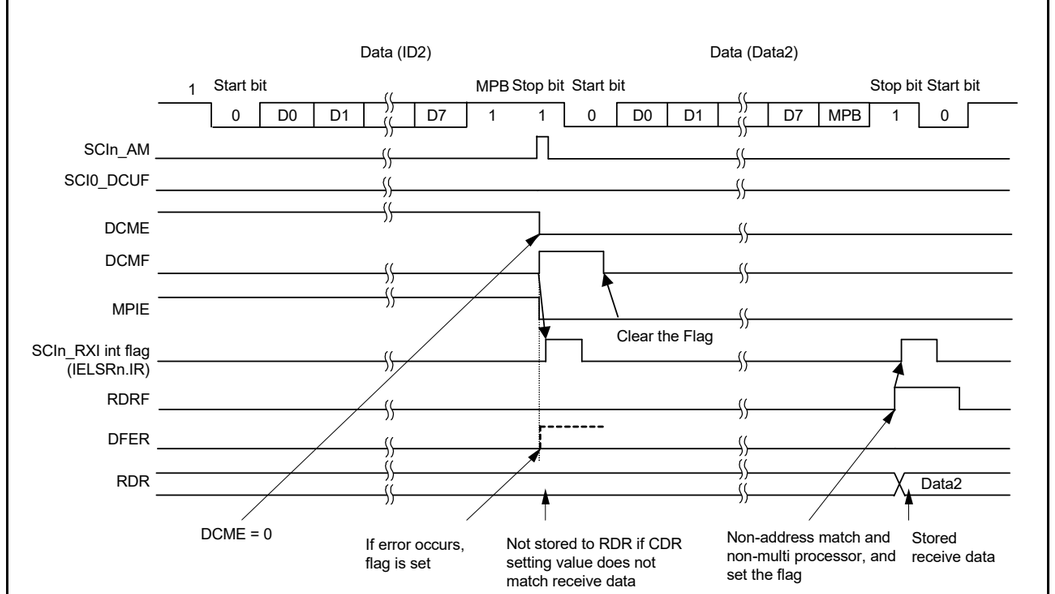


(b)接收数据与CDR比较匹配示例（8位长度奇偶校验非多处理器模式）

Figure 34.5 地址匹配示例（一）非多处理器模式



(a) Example of compare non-match between receive data and CDR (8-bit length/IDSEL = 1/multi-processor mode)

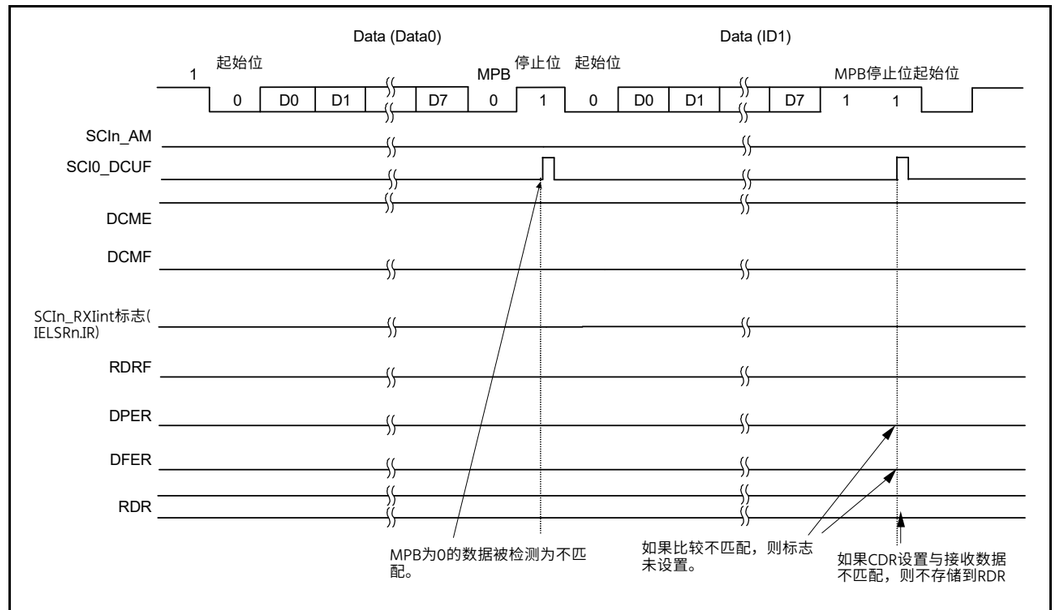


(b) Example of compare match between receive data and CDR (8-bit length/IDSEL = 1/multi-processor mode)

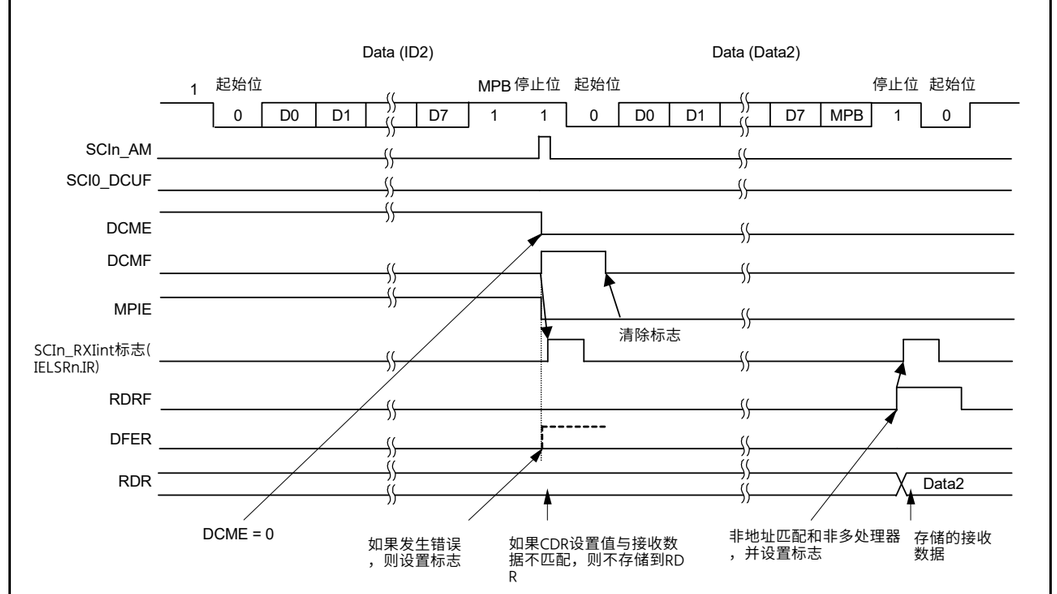
Figure 34.6 Example of address match (2) multi-processor mode

34.3.7 SCI Initialization in Asynchronous Mode

Before transmitting and receiving data, start by writing the initial value 00h to the SCR register, then continue through the SCI initialization procedure (select non-FIFO or FIFO) shown in Figure 34.7 and Figure 34.8. Whenever the



(a)接收数据和CDR比较不匹配的示例（8位长度IDSEL=1多处理器模式）



(b)接收数据与CDR比较匹配示例（8位长度IDSEL=1多处理器模式）

Figure 34.6 地址匹配示例（二）多处理器模式

34.3.7 异步模式下的SCI初始化

在发送和接收数据之前，首先将初始值00h写入SCR寄存器，然后继续执行图34.7和图34.8所示的SCI初始化过程（选择非FIFO或FIFO）。每当

operating mode or transfer format is to be changed, the SCR register must be initialized before the change is made.

When the external clock is used in asynchronous mode, ensure that the clock signal is supplied during initialization.

Note: When the SCR.RE bit is set to 0, the ORER, FER, RDRF, RDF, PER, and DR flags in SSR/SSR_FIFO, and the RDR and RDRHL registers are not initialized. When the TE bit is set to 0, the TEND flag for the selected FIFO buffer is not initialized.

Note: Switching the value of the SCR.TE bit from 1 to 0 or 0 to 1 while the SCR.TIE bit is 1 leads to the generation of an SCIn_TXI interrupt request.

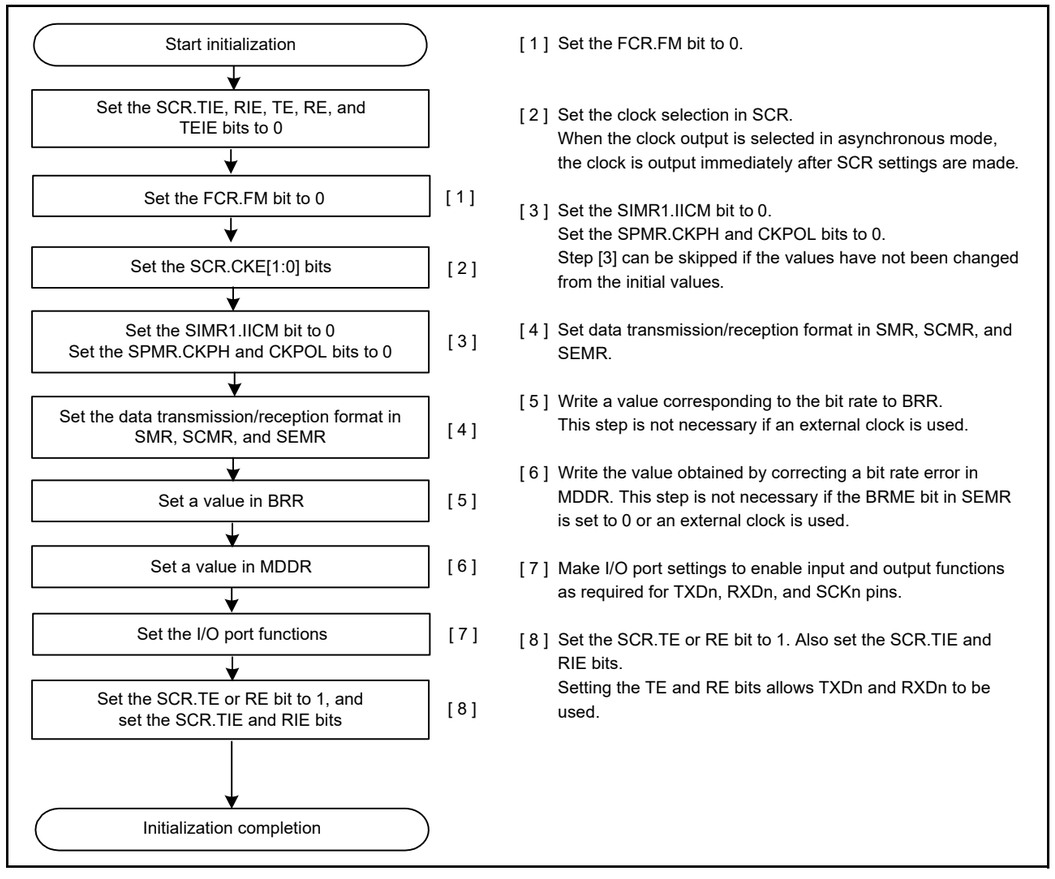


Figure 34.7 Example flow of SCI initialization in asynchronous mode with non-FIFO selected

要更改操作模式或传输格式，必须在更改之前初始化SCR寄存器。

在异步模式下使用外部时钟时，请确保在初始化期间提供时钟信号。

Note: 当SCR.RE位设置为0时，SSRSSR_FIFO中的ORER、FER、RDRF、RDF、PER和DR标志，以及RDR和RDRHL寄存器未初始化。当TE位设置为0时，所选FIFO缓冲区的TEND标志未初始化。

Note: 当SCR.TIE位为1时，将SCR.TE位的值从1切换到0或0到1会导致生成SCIn_TXI中断请求。

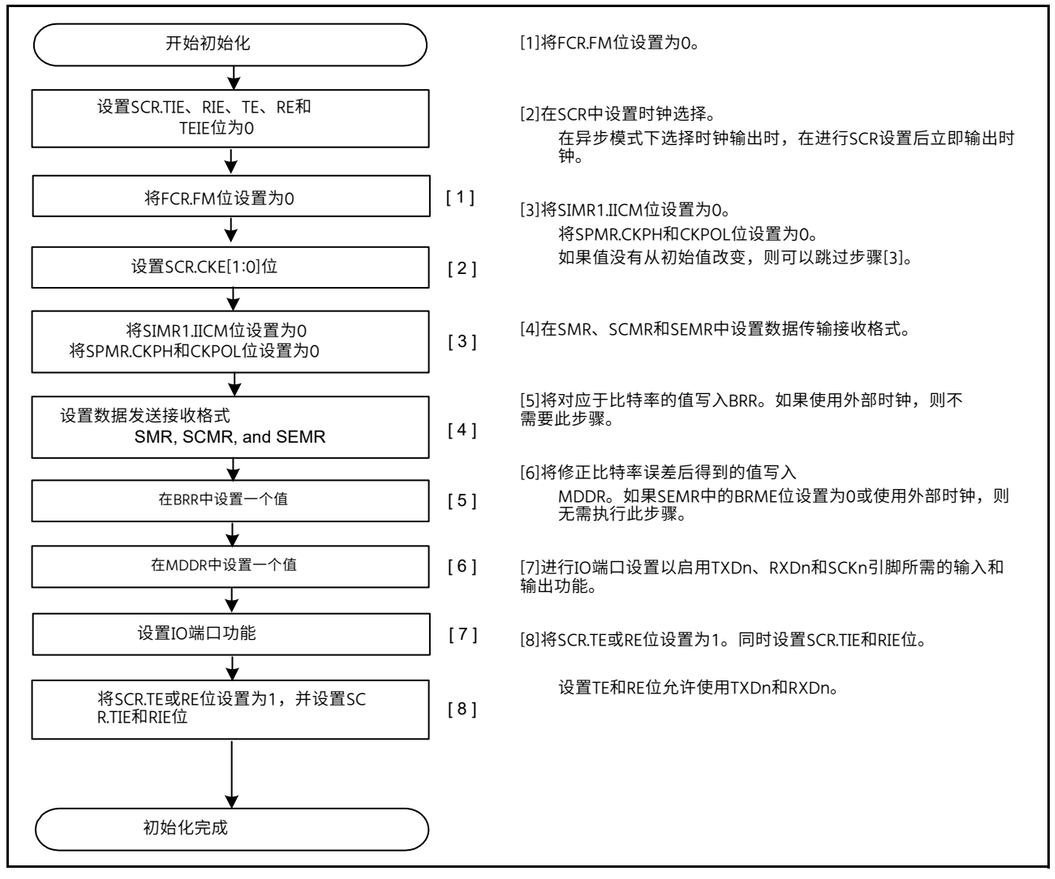


Figure 34.7 选择非FIFO的异步模式下SCI初始化示例流程

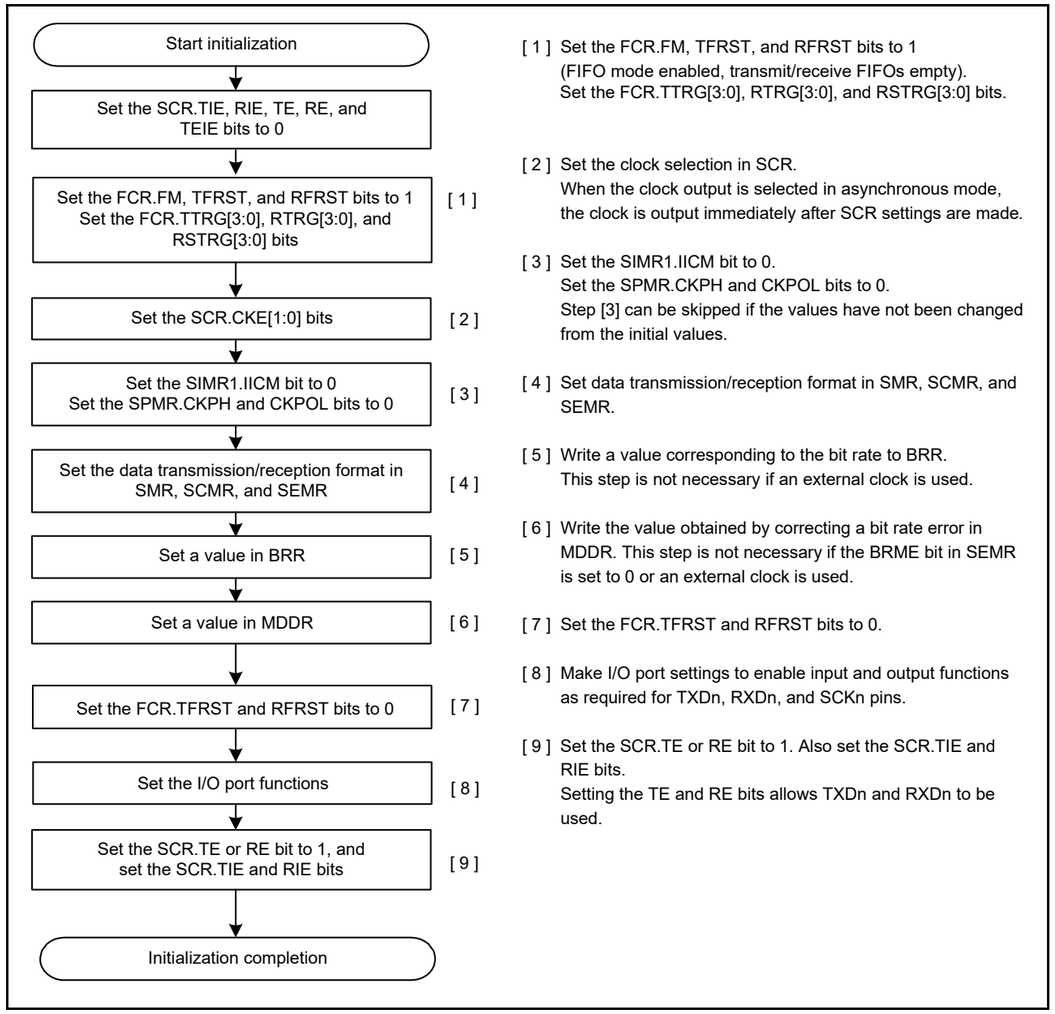


Figure 34.8 Example flow of SCI initialization in asynchronous mode with FIFO selected

34.3.8 Serial Data Transmission in Asynchronous Mode

(1) Non-FIFO selected

Figure 34.9, Figure 34.10, and Figure 34.11 show examples of serial transmission in asynchronous mode.

In serial transmission, the SCI operates as described in this section. When the SCR.TE bit is set to 1, the high level for one frame (preamble) is output to TXD.

1. The SCI transfers data from the TDR*1 register to the TSR register when data is written to TDR*1 in the SCIn_TXI interrupt handling routine.
   The SCIn_TXI interrupt request at the beginning of transmission is generated when the SCR.TE and SCR.TIE bits are set to 1 simultaneously by a single instruction.
2. Transmission starts after the SPMR.CTSE bit is set to 0 (CTS function is disabled) or a low level on the CTSn_RTSn pin causes data transfer from the TDR*1 register to the TSR register. If the SCR.TIE bit is 1, an SCIn_TXI interrupt request is generated. Continuous transmission is possible by writing the next transmit data to the TDR*1 register in the SCIn_TXI interrupt handling routine before transmission of the current transmit data is

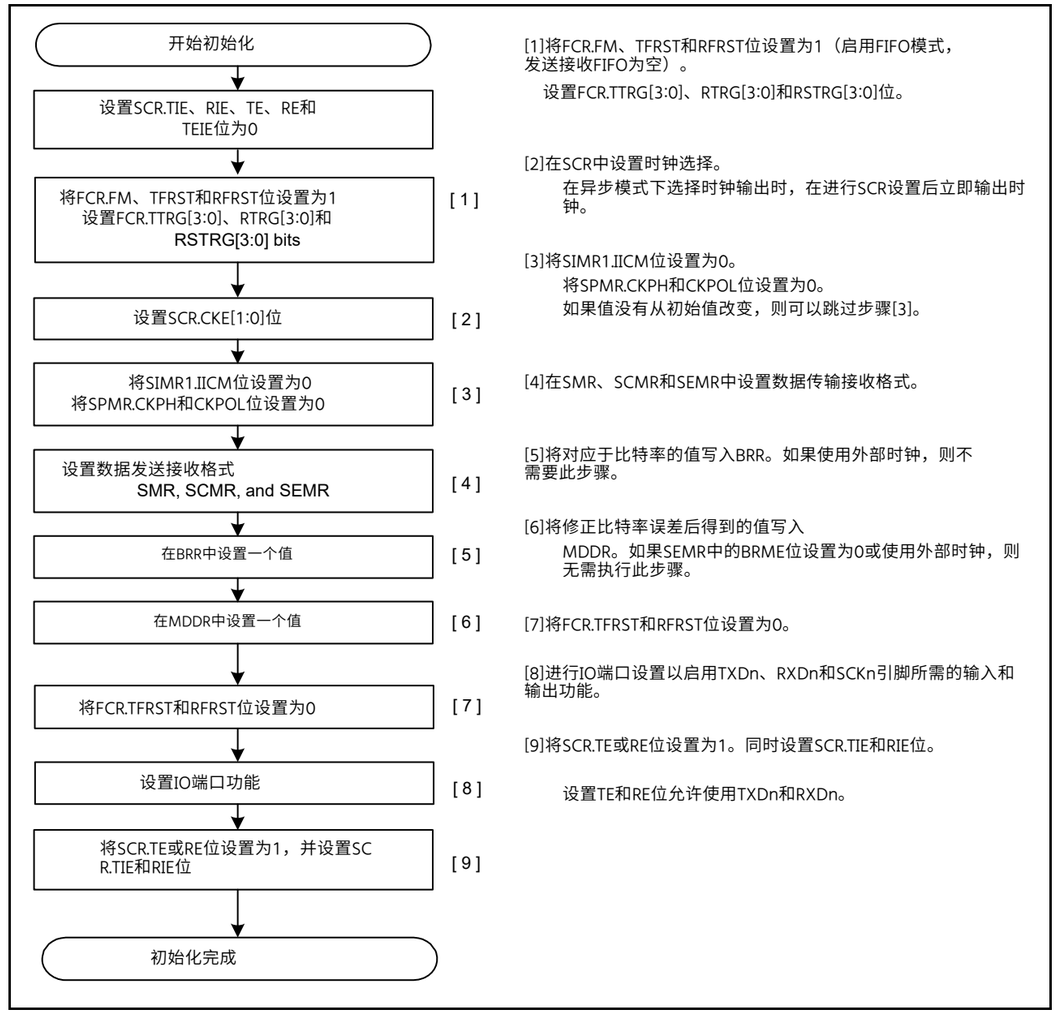


Figure 34.8 选择FIFO的异步模式下SCI初始化示例流程

34.3.8 异步模式下的串行数据传输

(1) Non-FIFO selected

图34.9、图34.10和图34.11显示了异步模式下的串行传输示例。

在串行传输中，SCI的操作如本节所述。当SCR.TE位设置为1时，一帧（前导码）的高电平输出到TXD。

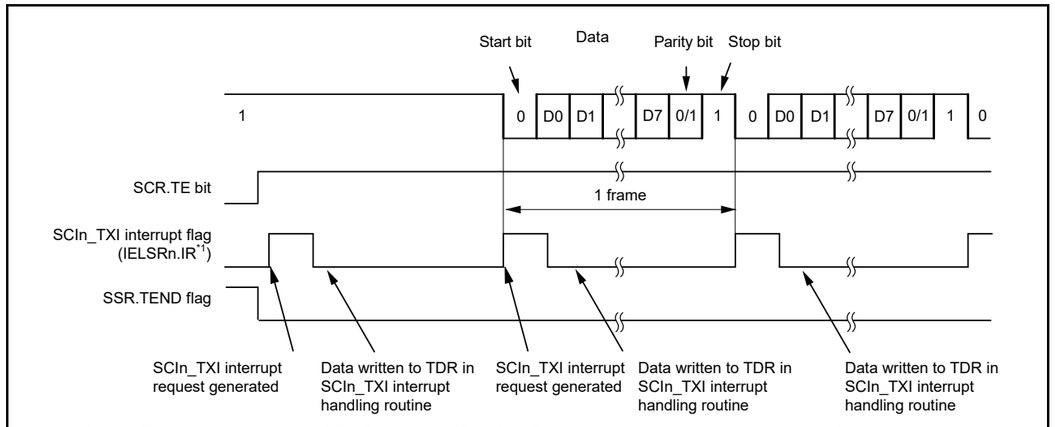
1. 当数据在SCIn_TXI中断处理程序中写入TDR*1时，SCI将数据从TDR*1寄存器传输到TSR寄存器。当一条指令同时将SCR.TE和SCR.TIE位设置为1时，会在传输开始时产生SCIn_TXI中断请求。
2. 在SPMR.CTSE位设置为0（禁用CTS功能）或低电平后开始发送
   CTSn_RTSn引脚导致数据从TDR*1寄存器传输到TSR寄存器。如果SCR.TIE位为1，则
   SCIn_TXI中断请求产生。在发送当前发送数据之前，通过将下一个发送数据写入SCIn_TXI中断处理程序中的TDR*1寄存器，可以实现连续发送

complete. When SCIn_TEI interrupt requests are in use, set the SCR.TIE bit to 0 (SCIn_TXI interrupt requests are disabled) and the SCR.TEIE bit to 1 (an SCIn_TEI interrupt request is enabled) after the last of the data to be transmitted is written to the TDR*1 register from the handling routine for SCIn_TXI requests.

3. Data is sent from the TXDn pin in the following order:
   - Start bit
   - Transmit data
   - Parity bit or multi-processor bit (can be omitted depending on the format)
   - Stop bit.
4. The SCI checks for update of the TDR register on output of the stop bit.
5. When the TDR register is updated, setting the SPMR.CTSE bit to 0 (CTS function is disabled) or a low level input on the CTSn_RTSn pin causes transfer of the next transmit data from the TDR*1 register to the TSR register and transmission of the stop bit, after which serial transmission of the next frame starts.
6. If the TDR register is not updated, the SSR.TEND flag is set to 1, the stop bit is sent, and the mark state is entered, in which 1 is output. If the SCR.TEIE bit is 1, the SSR.TEND flag is set to 1 and an SCIn_TEI interrupt request is generated.

Note 1. Only write data to the TDRHL register when 9-bit data length is selected.

Figure 34.9, Figure 34.10, and Figure 34.11 show examples of serial transmission in asynchronous mode.



Note 1. See section 14, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

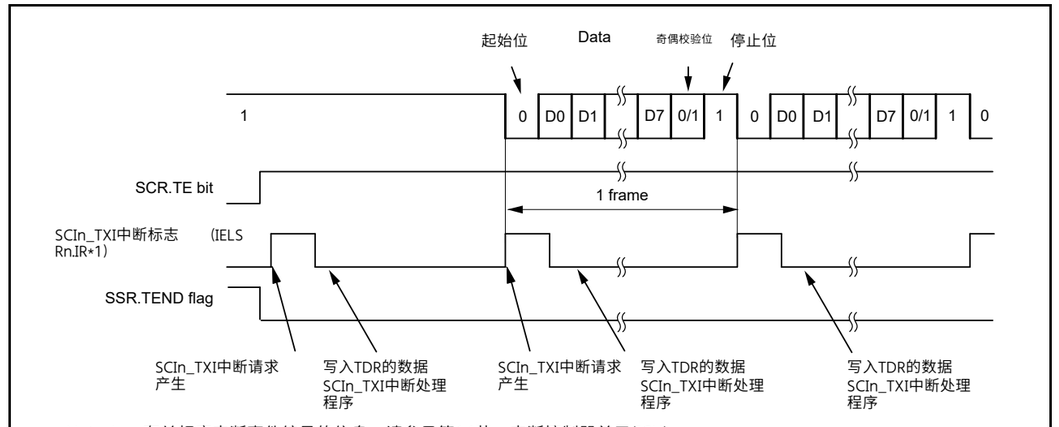
Figure 34.9 Example operation for serial transmission in asynchronous mode (1) with 8-bit data, parity bit, 1 stop bit, CTS function not used, and at the beginning of transmission

完全的。使用SCIn_TEI中断请求时，在写入要发送的最后一个数据后，将SCR.TIE位设置为0（禁止SCIn_TXI中断请求）并将SCR.TEIE位设置为1（启用SCIn_TEI中断请求）从SCIn_TXI请求的处理例程到TDR*1寄存器。

3. 数据按以下顺序从TXDn引脚发送：
   - 起始位
   - 传输数据
   - 奇偶校验位或多处理器位（可根据格式省略）
   - 停止位。
4. SCI在停止位输出时检查TDR寄存器的更新。
5. 更新TDR寄存器时，将SPMR.CTSE位设置为0（禁用CTS功能）或CTSn_RTSn引脚上的低电平输入会导致下一个发送数据从TDR*1寄存器传输到TSR寄存器并发送停止位，之后开始下一帧的串行传输。
6. 如果TDR寄存器没有更新，则SSR.TEND标志置1，发送停止位，进入标记状态，其中输出1。如果SCR.TEIE位为1，则SSR.TEND标志设置为1，并产生SCIn_TEI中断请求。

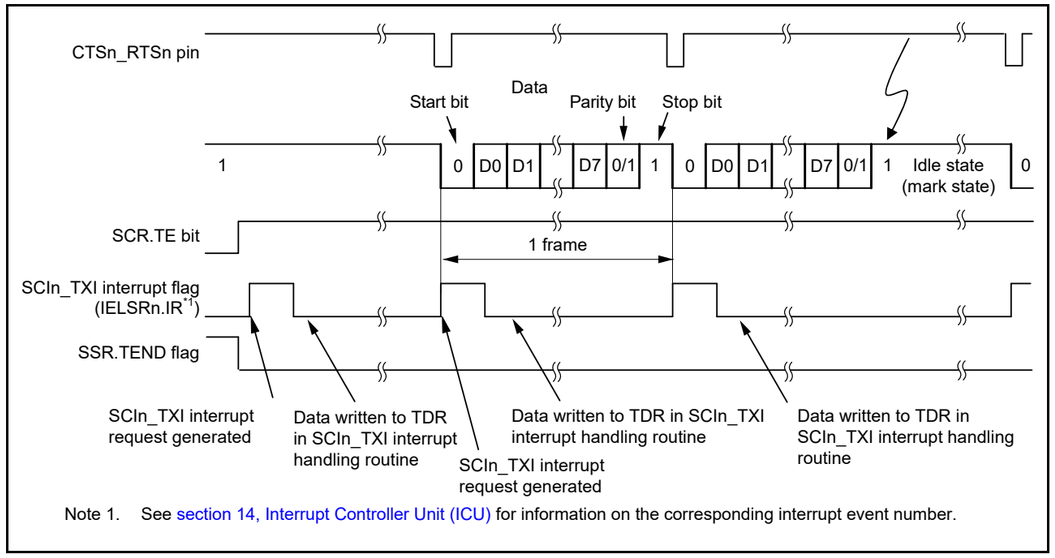
注意1.选择9位数据长度时，仅将数据写入TDRHL寄存器。

图34.9、图34.10和图34.11显示了异步模式下的串行传输示例。



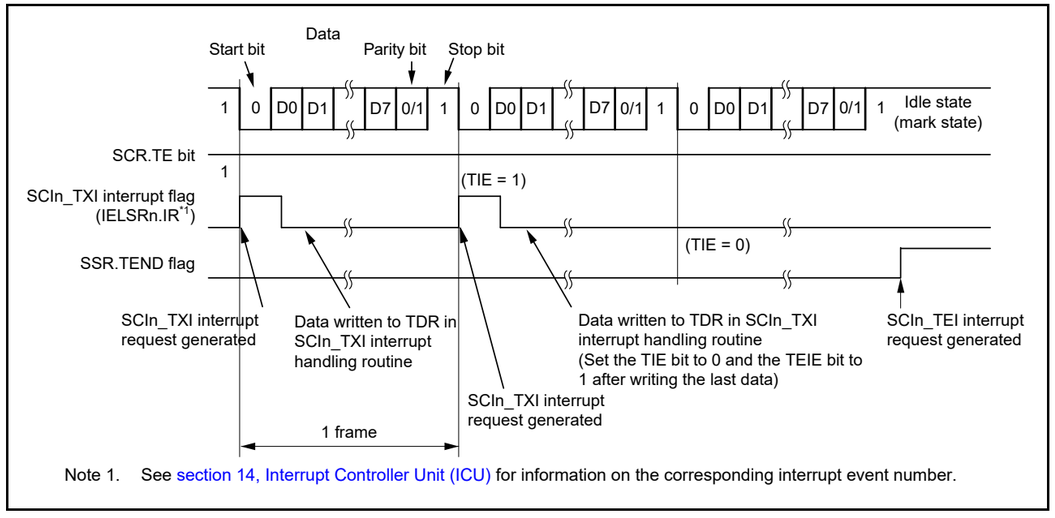
Note 1. 有关相应中断事件编号的信息，请参见第14节，中断控制器单元(ICU)。

Figure 34.9 异步模式下串行传输的示例操作(1)使用8位数据、奇偶校验位、1个停止位、未使用CTS功能以及传输开始时



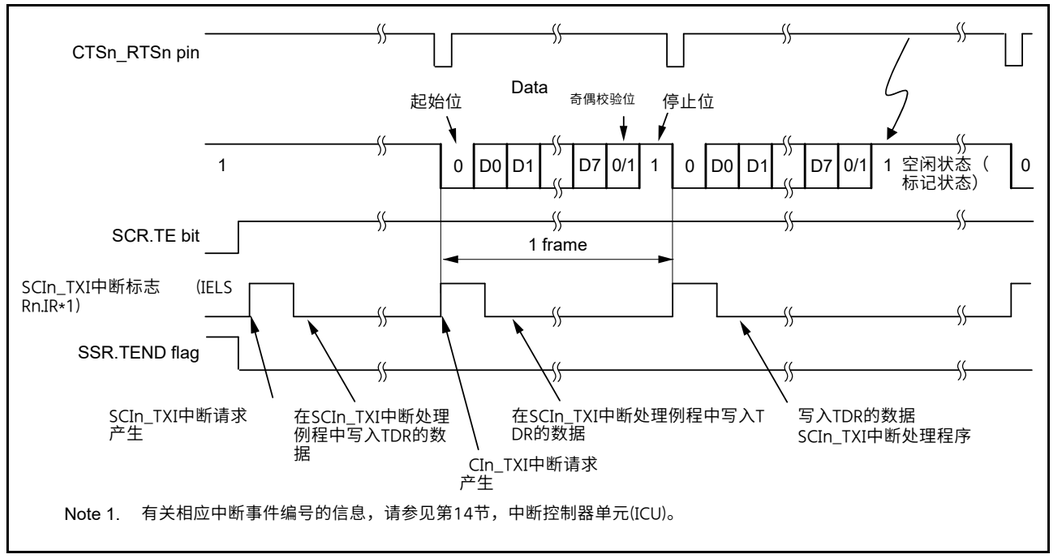
Note 1. See section 14, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 34.10 Example operation for serial transmission in asynchronous mode (2) with 8-bit data, parity bit, one stop bit, CTS function used, and at the beginning of transmission



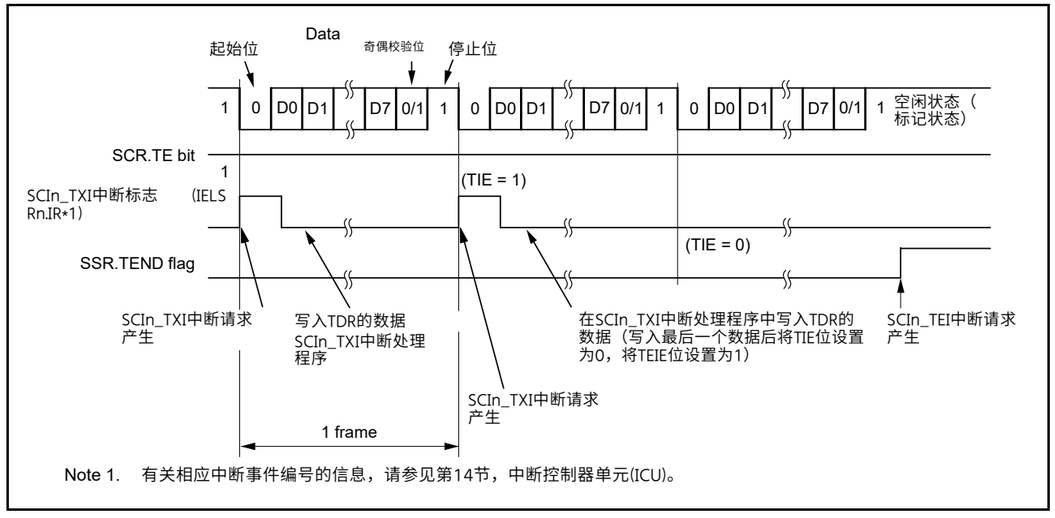
Note 1. See section 14, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 34.11 Example operation for serial transmission in asynchronous mode (3) with 8-bit data, parity bit, one stop bit, CTS function not used, and from the middle of transmission until transmission completion



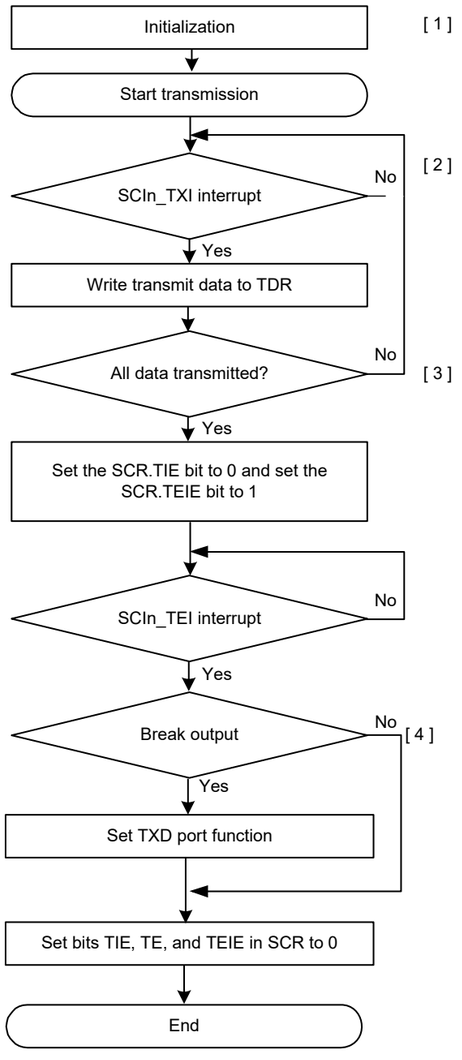
Note 1. 有关相应中断事件编号的信息，请参见第14节，中断控制器单元(ICU)。

Figure 34.10 异步模式下串行传输的示例操作(2)使用8位数据、奇偶校验位、一个停止位、使用CTS功能和传输开始



Note 1. 有关相应中断事件编号的信息，请参见第14节，中断控制器单元(ICU)。

Figure 34.11 异步模式下串行传输的示例操作(3)使用8位数据、奇偶校验位、一个停止位、未使用CTS功能，以及从传输中间到传输完成



[1] SCI Initialization:
Set data transmission.
After the SCR.TE bit is set to 1, 1 is output for a Frame (preamble), and transmission is enabled.

[2] Transmit data write to TDR by an SCIn_TXI interrupt request. When transmit data is transferred from TDR to TSR, a transmit data empty interrupt (SCIn_TXI) request is generated. Write transmit data to TDR once in the SCIn_TXI interrupt processing routine.

[3] Serial transmission continuation procedure:
To continue serial transmission write transmit data to TDR once using an SCIn_TXI interrupt request. Transmit data can also be written to TDR by activating the DMAC or DTC.
When SCIn_TEI interrupt requests are in use, set the SCR.TIE bit to 0 and the SCR.TEIE bit to 1 after the last of the data to be transmitted is written to TDR.

[4] Break output at the end of serial transmission:
To output a break in serial transmission, after setting the output state (LOW level output) of TXDn, pin by SPTR.SPB2IO and SPTR.SPB2DT bits, set the SCR.TE bit to 0.

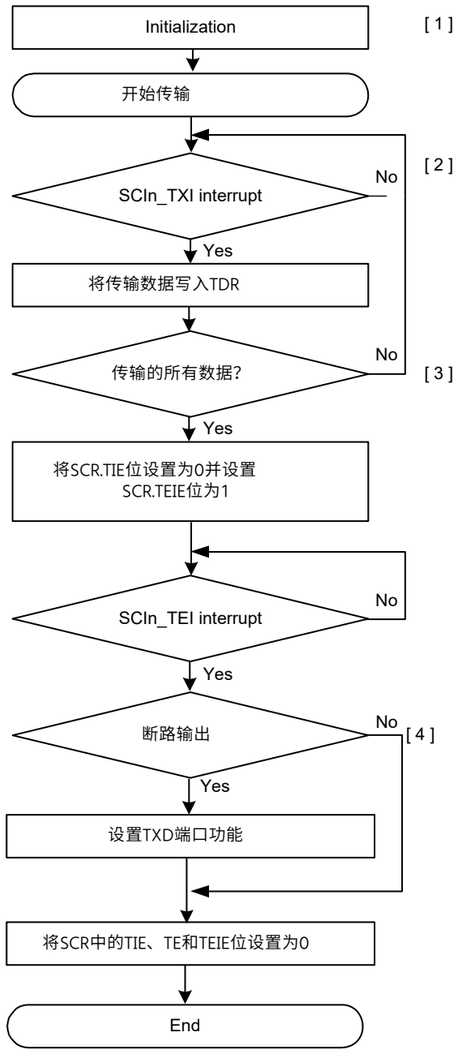
Note: The TDR register becomes the TDRHL register when 9-bit data length is selected.

Figure 34.12 Example flow of serial transmission in asynchronous mode with non-FIFO selected

(2) FIFO selected

Figure 34.13 shows an example of a data format that is written to FTDRH and FTDRL in asynchronous mode.

Data corresponding to the data length is set to FTDRH and FTDRL. Write 0 for unused bits. Write in order from FTDRH to FTDRL.



[1] SCI Initialization:
设置数据传输。
SCR.TE位设置为1后，为帧（前导码）输出1，并启用传输。

[2]通过SCIn_TXI中断请求将数据写入TDR。当发送数据从TDR传输到TSR时，会产生发送数据空中断(SCIn_TXI)请求。在SCIn_TXI中断处理程序中将发送数据写入TDR一次。

[3]串行传输继续程序：
继续串行传输写入传输数据到TDR一次使用SCIn_TXI中断请求。
也可以通过激活DMAC或DTC将传输数据写入TDR。当SCIn_TEI中断请求正在使用时，设置

在将要发送的最后一个数据写入TDR后，SCR.TIE位为0，SCR.TEIE位为1。

[4]串行传输结束时中断输出：
要在串行传输中输出中断，通过SPTR.SPB2IO和SPTR.SPB2DT位设置TXDn的输出状态（低电平输出）后，设置

SCR.TE位为0。

Note: 选择9位数据长度时，TDR寄存器成为TDRHL寄存器。

Figure 34.12 选择非FIFO的异步模式下串行传输示例流程

(2) FIFO selected

图34.13显示了以异步模式写入FTDRH和FTDRL的数据格式示例。

对应于数据长度的数据被设置为FTDRH和FTDRL。为未使用的位写入0。从FTDRH到FTDRL的顺序写。

Data Length	Register Setting		Transmit data in FTDRH, FTDRL															
			FTDRHL															
			FTDRH								FTDRL							
	SCMR.CHR1	SMR.CHR	b7	b6	b5	b4	b3	b2	b1	b0	b7	b6	b5	b4	b3	b2	b1	b0
7 bits	1	0	—	—	—	—	—	—	—	—	—	7-bit transmit data						
8 bits	1	1	—	—	—	—	—	—	—	—	8-bit transmit data							
9 bits	0	Don't care	—	—	—	—	—	—	—	9-bit transmit data								

—: Invalid. The write value should be 0.

Figure 34.13 Data format written to FTDRH and FTDRL with FIFO selected

In serial transmission, the SCI operates as described in this section. When the TE bit is set to 1, the high level is output to TXD for one frame (preamble).

1. The SCI transfers data from the FTDRL*1 register to the TSR register when data is written to FTDRL*1 in the SCIn_TXI interrupt handling routine. The amount of data that can be written to FTDRL is 16 minus FDR.T[4:0] bytes. The SCIn_TXI interrupt request at the beginning of transmission is generated when the SCR.TE and SCR.TIE bits are set to 1 simultaneously by a single instruction.
2. Transmission starts after the SPMR.CTSE bit is set to 0 (CTS function is disabled) or a low level on the CTSn_RTSn pin causes data transfer from the FTDRL*1 register to the TSR register. When the amount of transmit data written in FTDRL is equal to or less than the specified transmit triggering number, SSR_FIFO.TDFE is set to 1. If the SCR.TIE bit is 1, an SCIn_TXI interrupt request is generated. Continuous transmission is possible by writing the next transmit data to FTDRL*1 in the SCIn_TXI interrupt handling routine before transmission of the current transmit data is complete. When SCIn_TEI interrupt requests are in use, set the SCR.TIE bit to 0 (SCIn_TXI interrupt requests are disabled) and the SCR.TEIE bit to 1 (an SCIn_TEI interrupt request is enabled) after the last of the data to be transmitted is written to the FTDRL*1 *2 register from the handling routine for SCIn_TXI requests.
3. Data is sent from the TXDn pin in the following order:
   - Start bit
   - Transmit data
   - Parity bit or multi-processor bit (can be omitted depending on the format)
   - Stop bit.
4. On output of the stop bit, the SCI checks whether non-transmitted data remains in the FTDRL*3 register.
5. When data is set to FTDRL*3, setting the SPMR.CTSE bit to 0 (CTS function is disabled) or a low level input on the CTSn_RTSn pin causes transfer of the next transmit data from FTDRL*1 to TSR and transmission of the stop bit, after which serial transmission of the next frame starts.
6. If data is not set in FTDRL*3, the TEND flag in SSR_FIFO is set to 1, the stop bit is sent, and the mark state is entered in which 1 is output. If the SCR.TEIE bit is 1, the SSR_FIFO.TEND flag is set to 1 and an SCIn_TEI interrupt request is generated.

Note 1. Write data not to FTDRL but to the FTDRH and FTDRL registers.
Note 2. Write data in order from FTDRH to FTDRL when 9-bit data length is selected.
Note 3. The SCI only checks for update to the FTDRL register and not the FTDRH register when 9-bit data length is selected.

Figure 34.14 shows an example flow of serial transmission in asynchronous mode with FIFO selected.

数据长度	寄存器设置		在FTDRH、FTDRL中传输数据															
			FTDRHL															
			FTDRH								FTDRL							
	SCMR.CHR1	SMR.CHR	b7	b6	b5	b4	b3	b2	b1	b0	b7	b6	b5	b4	b3	b2	b1	b0
7 bits	1	0	—	—	—	—	—	—	—	—	—	7位传输数据						
8 bits	1	1	—	—	—	—	—	—	—	—	8位传输数据							
9 bits	0	不在乎	—	—	—	—	—	—	—	9位传输数据								

-：无效的。写入值应为0。

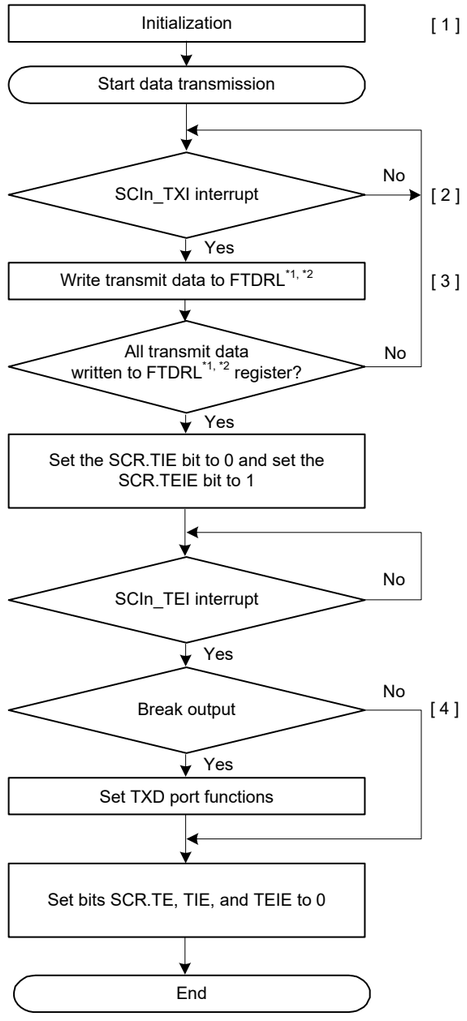
Figure 34.13 选择FIFO写入FTDRH和FTDRL的数据格式

在串行传输中，SCI的操作如本节所述。当TE位设置为1时，高电平输出到一帧的TXD（前导码）。

1. 当数据写入FTDRL*1时，SCI将数据从FTDRL*1寄存器传输到TSR寄存器SCIn_TXI中断处理程序。可写入FTDRL的数据量为16减去FDR.T[4:0]字节。当一条指令同时将SCR.TE和SCR.TIE位设置为1时，会在传输开始时产生SCIn_TXI中断请求。
2. 在SPMR.CTSE位设置为0（禁用CTS功能）或低电平后开始发送CTSn_RTSn引脚导致数据从FTDRL*1寄存器传输到TSR寄存器。当写入FTDRL的发送数据量等于或小于指定的发送触发数时，SSR_FIFO.TDFE设置为1。如果SCR.TIE位为1，则产生SCIn_TXI中断请求。在当前传输数据传输完成之前，通过在SCIn_TXI中断处理例程中将下一个传输数据写入FTDRL*1可以实现连续传输。使用SCIn_TEI中断请求时，在写入最后一个要发送的数据后，将SCR.TIE位设置为0（禁止SCIn_TXI中断请求）并将SCR.TEIE位设置为1（启用SCIn_TEI中断请求）从SCIn_TXI请求的处理例程到FTDRL*1*2寄存器。
3. 数据按以下顺序从TXDn引脚发送：
   - 起始位
   - 传输数据
   - 奇偶校验位或多处理器位（可根据格式省略）
   - 停止位。
4. 在停止位输出时，SCI检查未发送的数据是否保留在FTDRL*3寄存器中。
5. 当数据设置为FTDRL*3时，将SPMR.CTSE位设置为0（禁用CTS功能）或低电平输入CTSn_RTSn管脚使下一个传输数据从FTDRL*1传输到TSR并传输停止位，然后开始下一帧的串行传输。
6. 如果FTDRL*3中未设置数据，则将SSR_FIFO中的TEND标志设置为1，发送停止位，并进入输出1的标记状态。如果SCR.TEIE位为1，则SSR_FIFO.TEND标志设置为1，并产生SCIn_TEI中断请求。

注1.不要将数据写入FTDRL，而是写入FTDRH和FTDRL寄存器。
注2.选择9位数据长度时，按从FTDRH到FTDRL的顺序写入数据。
注意3.SCI仅检查对FTDRL寄存器的更新，而不是选择9位数据长度时的FTDRH寄存器。

图34.14显示了选择FIFO的异步模式下串行传输的示例流程。



[1] SCI initialization:
Set data transmission.
After the SCR.TE bit is set to 1, 1 is output for a frame (preamble), and transmission is enabled.

[2] Transmit data write to FTDRL*1 by an SCIn_TXI interrupt request:
When transmit data is transferred from FTDRL to TSR, when the quantity of transmit data written in FTDRL is equal to or less than the specified transmit triggering number, a transmit data FIFO empty interrupt (SCIn_TXI) request is generated. Write transmit data to FTDRL*1, *2 once in the SCIn_TXI interrupt handling routine.

[3] Serial transmission continuation procedure:
To continue serial transmission, write all transmit data to FTDRL using an SCIn_TXI interrupt request and clear the SSR_FIFO.TDFE flag to 0. The number of transmission data it is possible to write in is 16 - (the number of stored transmit FIFO data).
Transmit data can also be written to FTDRL by activating the DMAC or DTC. When writing the data to FTDRL by DMAC or DTC, the TDFE flag is cleared automatically, so do not write to the TDFE flag.
When SCIn_TEI interrupt requests are in use, set the SCR.TIE bit to 0 and the SCR.TEIE bit to 1 after the last of the data to be transmitted is written to FTDRL.

[4] Break output at the end of serial transmission:
To output a break in serial transmission, after setting the output state (LOW level output) of TXDn pin by SPTR.SPB2IO and SPTR.SPB2DT bits, set the SCR.TE bit to 0.

Note 1. When data length is 9 bits, this refers to FTDRH and FTDRL registers.
Note 2. When data length is 9 bits, write in order from FTDRH to FTDRL.

Figure 34.14 Example flow of serial transmission in asynchronous mode with FIFO selected

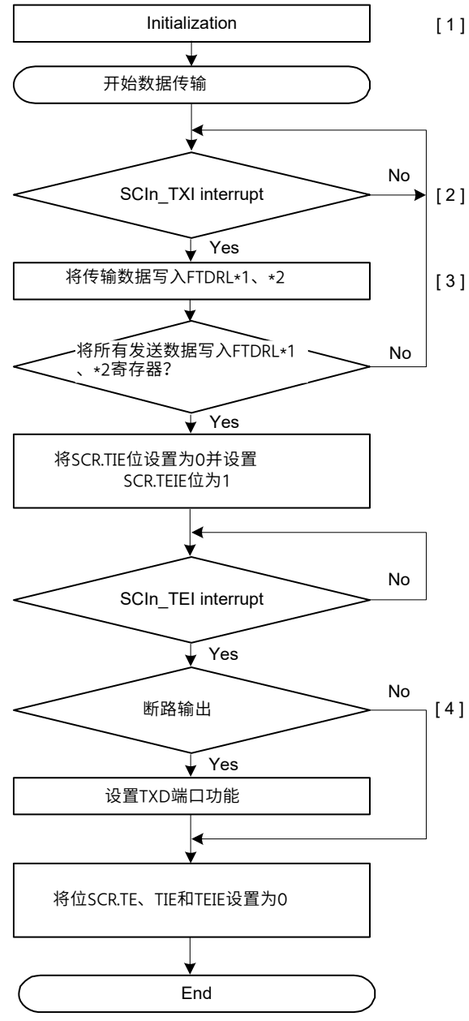
34.3.9 Serial Data Reception in Asynchronous Mode

(1) Non-FIFO selected

Figure 34.15 and Figure 34.16 show an example of the operation for serial data reception in asynchronous mode.

In serial data reception, the SCI operates as follows:

1. When the value of the SCR.RE bit becomes 1, the output signal on the CTSn_RTSn pin goes low.
2. The SCI monitors the communications line and when it detects a start bit, the SCI performs internal synchronization, stores receive data in RSR, and checks the parity bit and stop bit.
3. If an overrun error occurs, the SSR.ORER flag is set to 1. If the SCR.RIE bit is 1, an SCIn_ERI interrupt request is generated. Receive data is not transferred to the RDR*1 register.



[1] SCI initialization:
设置数据传输。
SCR.TE位设置为1后，为一个帧（前导码）输出1，并启用传输。

[2] 通过SCIn_TXI中断请求将发送数据写入FTDRL*1：当发送数据从FTDRL传输到TSR时，当写入FTDRL的发送数据量等于或小于指定的发送触发数时，发送数据FIFO空中断(SCIn_TXI)请求产生。在SCIn_TXI中断处理例程中将发送数据写入FTDRL*1、*2一次。

[3] 串行传输继续程序：
要继续串行传输，请将所有传输数据写入FTDRL使用SCIn_TXI中断请求并将SSR_FIFO.TDFE标志清除为0。可以写入的传输数据数为16（存储的传输FIFO数据数）。也可以通过激活DMAC或DTC将传输数据写入FTDRL。通过DMAC或DTC将数据写入FTDRL时，TDFE标志会自动清除，因此不要写入TDFE标志。当SCIn_TEI中断请求正在使用时，设置

在将要传输的最后一个数据写入FTDRL后，SCR.TIE位为0，SCR.TEIE位为1。

[4] 串行传输结束时中断输出：
要在串行传输中输出中断，在通过SPTR.SPB2IO和SPTR.SPB2DT位设置TXDn引脚的输出状态（低电平输出）后，将SCR.TE位设置为0。

Note 1. 当数据长度为9位时，这是指FTDRH和FTDRL registers.
Note 2. 当数据长度为9位时，按照FTDRH到FTDRL的顺序写入。

Figure 34.14 选择FIFO的异步模式下串行传输示例流程

34.3.9 异步模式下的串行数据接收

(1) Non-FIFO selected

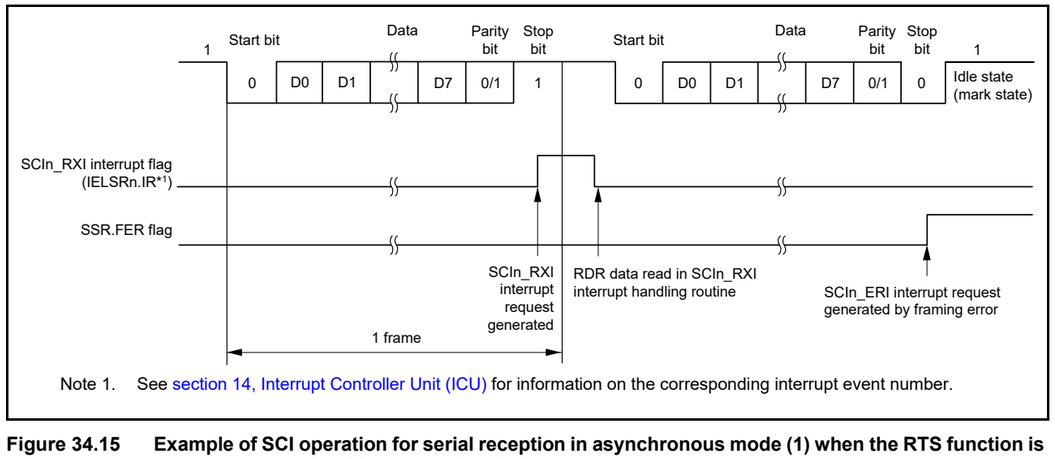
图34.15和图34.16显示了异步模式下串行数据接收操作的示例。

在串行数据接收中，SCI操作如下：

1. 当SCR.RE位的值变为1时，CTSn_RTSn引脚上的输出信号变为低电平。
2. SCI监视通信线路，当它检测到起始位时，SCI执行内部同步，将接收数据存储在RSR中，并检查奇偶校验位和停止位。
3. 如果发生溢出错误，则SSR.ORER标志设置为1。如果SCR.RIE位为1，则产生SCIn_ERI中断请求。接收数据不传送到RDR*1寄存器。

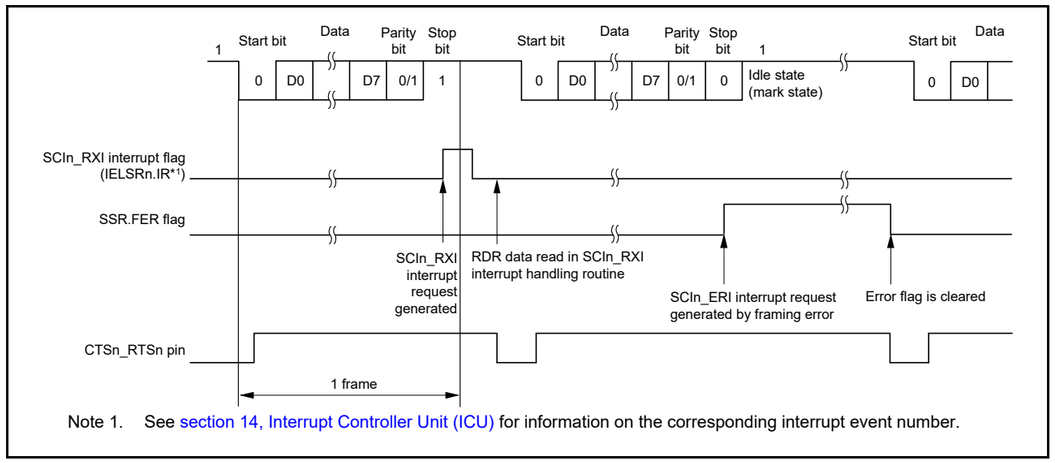
4. If a parity error is detected, the SSR.PER flag is set to 1 and receive data is transferred to the RDR*1 register. If the SCR.RIE bit is 1, an SCIn_ERI interrupt request is generated.
5. If a framing error is detected, the SSR.FER flag is set to 1 and receive data is transferred to the RDR*1 register. If the SCR.RIE bit is 1, an SCIn_ERI interrupt request is generated.
6. When reception finishes successfully, receive data is transferred to the RDR*1 register. If the SCR.RIE bit is 1, an SCIn_RXI interrupt request is generated. Continuous reception is enabled by reading the receive data transferred to the RDR register in the SCIn_RXI interrupt handling routine before reception of the next receive data completes. Reading the received data that was transferred to the RDR register causes the CTSn_RTSn pin to output low.

Note 1. Only read data in the RDRHL register when 9-bit data length is selected.



Note 1. See section 14, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 34.15 Example of SCI operation for serial reception in asynchronous mode (1) when the RTS function is not used, and with 8-bit data, parity bit, and 1 stop bit



Note 1. See section 14, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

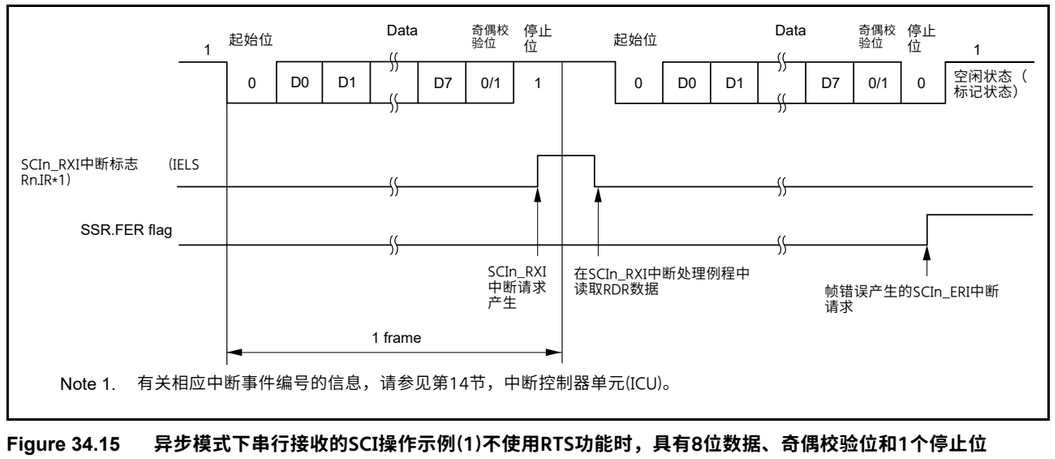
Figure 34.16 Example of SCI operation for serial reception in asynchronous mode (2) when RTS function is used, and with 8-bit data, parity bit, and 1 stop bit

Table 34.24 lists the states of the flags in the SSR register and receive data handling when a receive error is detected.

If a receive error is detected, an SCIn_ERI interrupt request is generated but an SCIn_RXI interrupt request is not generated. Data reception cannot be resumed while the receive error flag is 1. Accordingly, set the ORER, FER, and PER bits to 0 before resuming reception. In addition, be sure to read the RDR or RDRHL register during overrun error

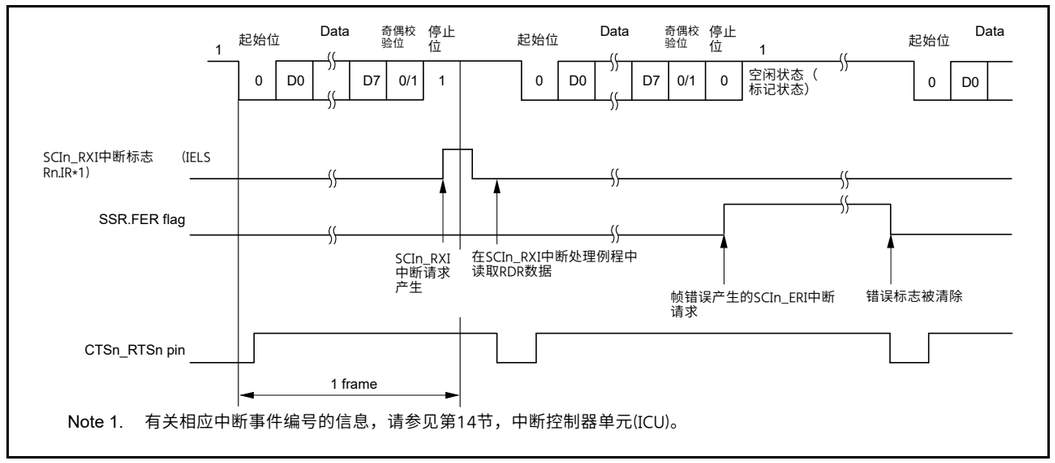
4. 如果检测到奇偶校验错误，则将SSR.PER标志设置为1，并将接收数据传输到RDR*1寄存器。如果SCR.RIE位为1，产生SCIn_ERI中断请求。
5. 如果检测到帧错误，则将SSR.FER标志设置为1，并将接收数据传输到RDR*1寄存器。如果SCR.RIE位为1，则产生SCIn_ERI中断请求。
6. 当接收成功完成时，接收数据被传送到RDR*1寄存器。如果SCR.RIE位为1，则产生SCIn_RXI中断请求。在接收下一个接收数据完成之前，通过在SCIn_RXI中断处理例程中读取传输到RDR寄存器的接收数据来启用连续接收。读取传输到RDR寄存器的接收数据会导致CTSn_RTSn引脚输出低电平。

注1.选择9位数据长度时，仅读取RDRHL寄存器中的数据。



Note 1. 有关相应中断事件编号的信息，请参见第14节，中断控制器单元(ICU)。

Figure 34.15 异步模式下串行接收的SCI操作示例(1)不使用RTS功能时，具有8位数据、奇偶校验位和1个停止位



Note 1. 有关相应中断事件编号的信息，请参见第14节，中断控制器单元(ICU)。

Figure 34.16 使用RTS功能，8位数据、奇偶校验位和1个停止位时，异步模式下串行接收的SCI操作示例(2)

表34.24列出了SSR寄存器中标志的状态以及检测到接收错误时的接收数据处理。

如果检测到接收错误，则会产生SCIn_ERI中断请求，但不会产生SCIn_RXI中断请求。当接收错误标志为1时，无法恢复数据接收。因此，在恢复接收之前，请将ORER、FER和PER位设置为0。另外，请务必在溢出错误期间读取RDR或RDRHL寄存器

processing. When a reception is forced to terminate by setting the SCR.RE bit to 0 during operation, read the RDR or RDRHL register because received data that is not yet read might be left in the RDR or RDRHL.

Figure 34.17 and Figure 34.18 show example flows of serial data reception.

Table 34.24 Flags in SSR Status Register and receive data handling

Flags in the SSR Status Register				
ORER	**FER**	**PER**	**Receive data**	**Receive error type**
1	0	0	Lost	Overrun error
0	1	0	Transferred to RDR	Framing error
0	0	1	Transferred to RDR	Parity error
1	1	0	Lost	Overrun error + framing error
1	0	1	Lost	Overrun error + parity error
0	1	1	Transferred to RDR	Framing error + parity error
1	1	1	Lost	Overrun error + framing error + parity error

Note 1. Only read data in the RDRHL register when 9-bit data length is selected.

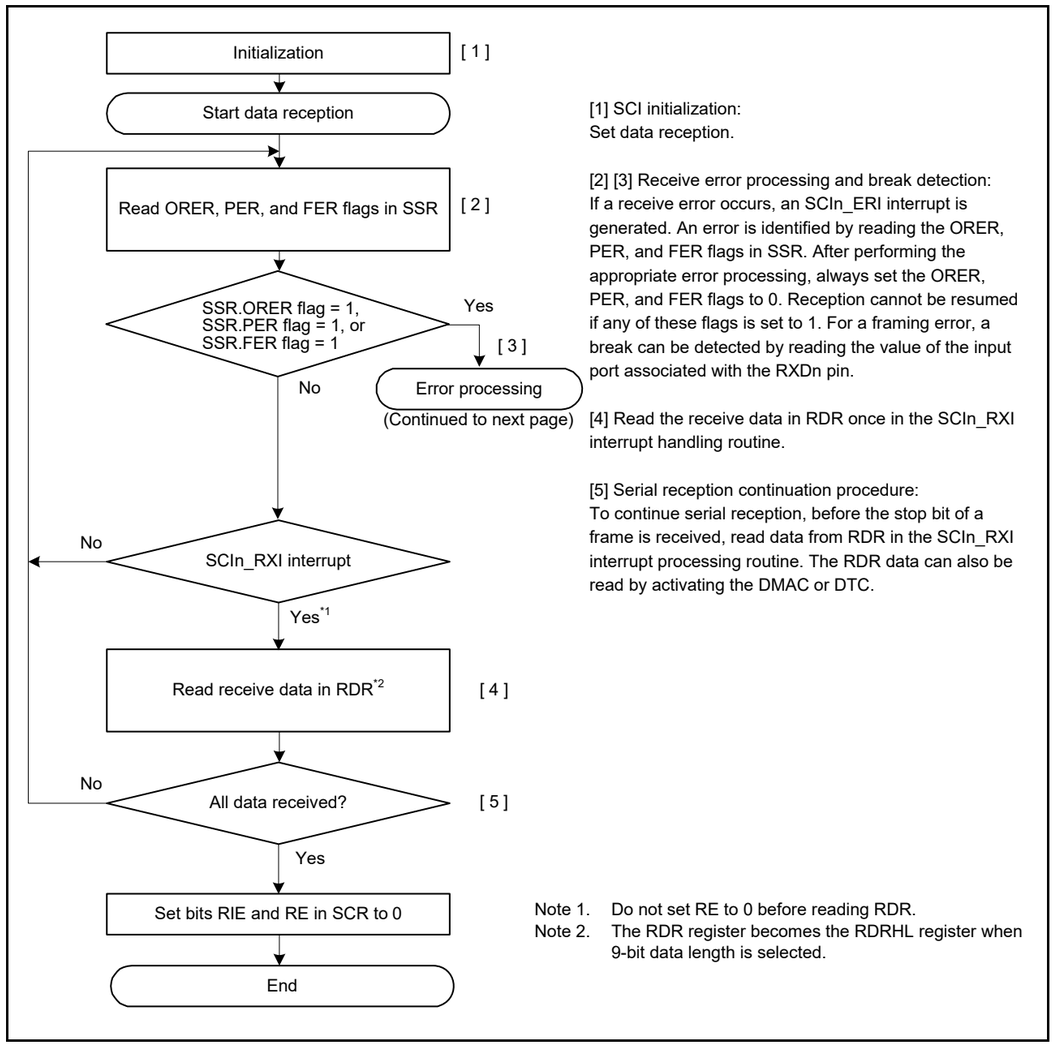
加工。如果在操作期间通过将SCR.RE位设置为0来强制终止接收，请读取RDR或RDRHL寄存器，因为尚未读取的已接收数据可能留在RDR或RDRHL中。

图34.17和图34.18显示了串行数据接收的示例流程。

Table 34.24 SSR状态寄存器中的标志和接收数据处理

SSR状态寄存器中的标志				
ORER	**FER**	**PER**	**接收数据**	**接收错误类型**
1	0	0	Lost	溢出错误
0	1	0	转移到RDR	构图错误
0	0	1	转移到RDR	奇偶校验错误
1	1	0	Lost	溢出错误+成帧错误
1	0	1	Lost	溢出错误+奇偶校验错误
0	1	1	转移到RDR	成帧错误+奇偶校验错误
1	1	1	Lost	溢出错误+帧错误+奇偶校验错误

Note 1. 仅在选择9位数据长度时读取RDRHL寄存器中的数据。



[1] SCI initialization:
Set data reception.

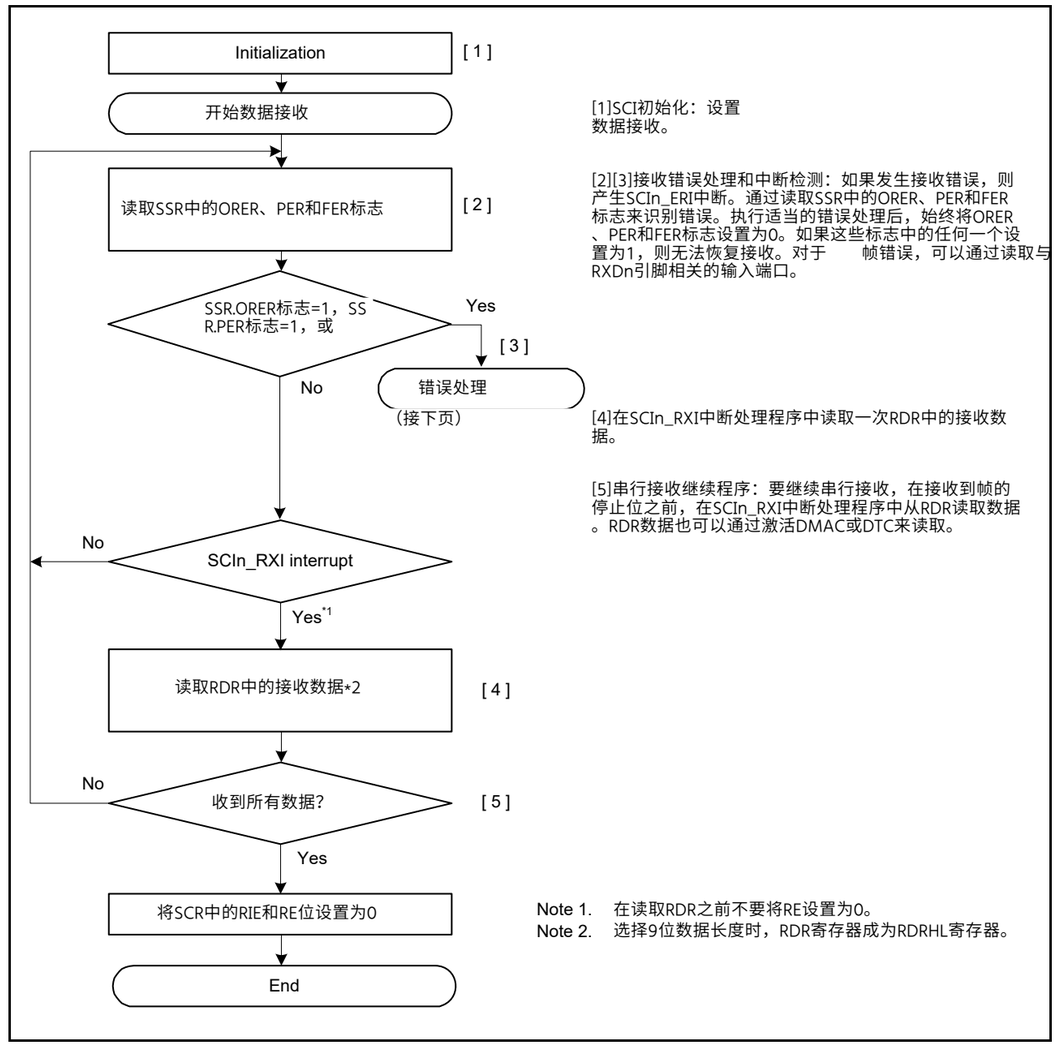
[2] [3] Receive error processing and break detection:
If a receive error occurs, an SCIn_ERI interrupt is generated. An error is identified by reading the ORER, PER, and FER flags in SSR. After performing the appropriate error processing, always set the ORER, PER, and FER flags to 0. Reception cannot be resumed if any of these flags is set to 1. For a framing error, a break can be detected by reading the value of the input port associated with the RXDn pin.

[4] Read the receive data in RDR once in the SCIn_RXI interrupt handling routine.

[5] Serial reception continuation procedure:
To continue serial reception, before the stop bit of a frame is received, read data from RDR in the SCIn_RXI interrupt processing routine. The RDR data can also be read by activating the DMAC or DTC.

Note 1. Do not set RE to 0 before reading RDR.
Note 2. The RDR register becomes the RDRHL register when 9-bit data length is selected.

Figure 34.17 Example flow of serial reception in asynchronous mode with non-FIFO selected (1)



[1]SCI初始化：设置
数据接收。

[2][3]接收错误处理和中断检测：如果发生接收错误，则产生SCIn_ERI中断。通过读取SSR中的ORER、PER和FER标志来识别错误。执行适当的错误处理后，始终将ORER、PER和FER标志设置为0。如果这些标志中的任何一个设置为1，则无法恢复接收。对于 帧错误，可以通过读取与RXDn引脚相关的输入端口。

[4]在SCIn_RXI中断处理程序中读取一次RDR中的接收数据。

[5]串行接收继续程序：要继续串行接收，在接收到帧的停止位之前，在SCIn_RXI中断处理程序中从RDR读取数据。RDR数据也可以通过激活DMAC或DTC来读取。

Note 1. 在读取RDR之前不要将RE设置为0。
Note 2. 选择9位数据长度时，RDR寄存器成为RDRHL寄存器。

Figure 34.17 选择非FIFO的异步模式下串行接收示例流程(1)

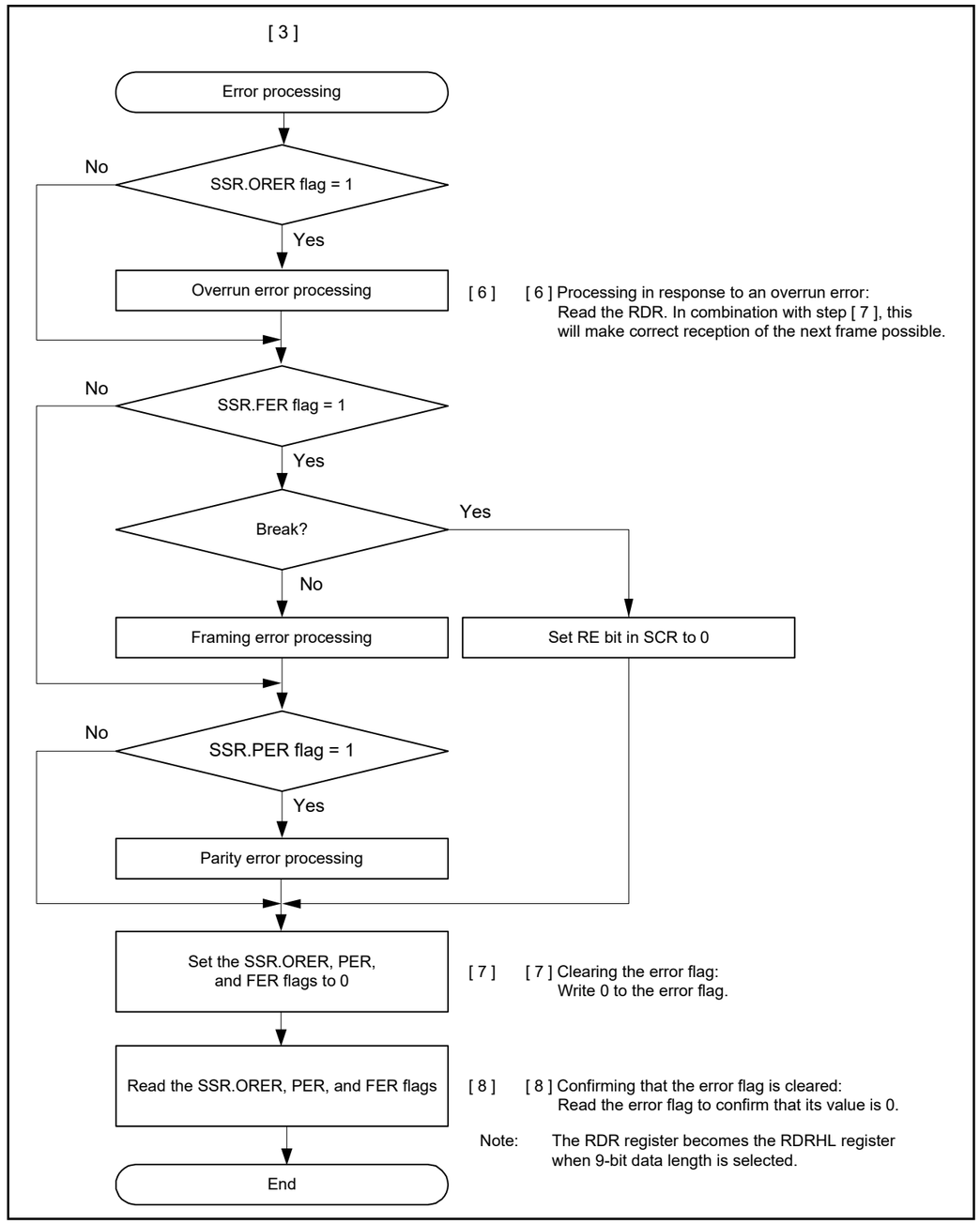


Figure 34.18 Example flow of serial reception in asynchronous mode with non-FIFO selected (2)

(2) FIFO selected

Figure 34.19 shows an example of a data format that is written to FRDRH and FRDRL in asynchronous mode.

In asynchronous mode, 0 is written to the MPB flag in the FRDRH register. Data that corresponds to the data length is written to FRDRH and FRDRL. Unused bits are written as 0. Read in order from FRDRH to FRDRL. If software reads

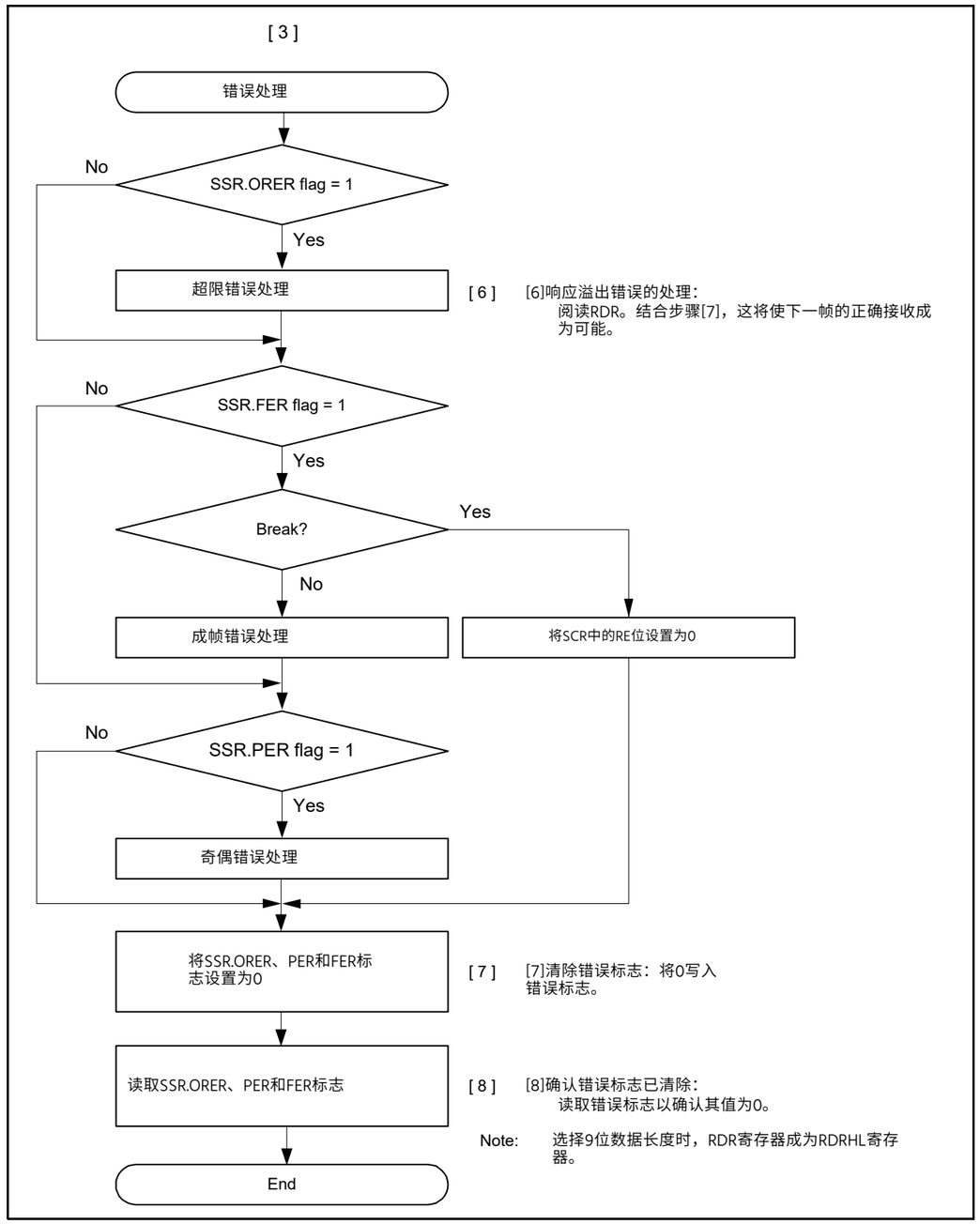


Figure 34.18 选择非FIFO的异步模式下串行接收示例流程(2)

(2) FIFO selected

图34.19显示了以异步模式写入FRDRH和FRDRL的数据格式示例。

在异步模式下，将0写入FRDRH寄存器中的MPB标志。对应于数据长度的数据被写入FRDRH和FRDRL。未使用的位写为0。按从FRDRH到FRDRL的顺序读取。如果软件读取

FRDRL, the SCI updates FER, PER, and receive data (RDAT[8:0]) in the FRDRL register with the next data. The RDF, ORER, and DR flags in the FRDRH register always reflect the associated flags in the SSR_FIFO register.

Data Length	Register Setting		Receive data in FRDRH, FRDRL															
			FRDRHL															
			FRDRH								FRDRL							
	SCMR.CHR1	SMR.CHR	b7	b6	b5	b4	b3	b2	b1	b0	b7	b6	b5	b4	b3	b2	b1	b0
7 bits	1	0	—	RDF	ORER	FER	PER	DR	0	0	0	7-bit receive data						
8 bits	1	1	—	RDF	ORER	FER	PER	DR	0	0	8-bit receive data							
9 bits	0	Don't care	—	RDF	ORER	FER	PER	DR	0	9-bit receive data								

Note: 0 is always read for MPB flag (FRDRH[1]).
When data length is 7 bits, 0 is always read for FRDRH[0] and FRDRL[7].
When data length is 8 bits, 0 is always read for FRDRH[0].
FRDRH[7] bit is read as an indefinite value.

Figure 34.19 Data format stored in FRDRH and FRDRL with FIFO selected

In serial data reception, the SCI operates as follows:

1. When the value of the SCR.RE bit becomes 1, the output signal on the CTSn_RTSn pin goes low.
2. The SCI monitors the communications line and, when it detects a start bit, the SCI performs internal synchronization, stores receive data in the RSR register, and checks the parity bit and stop bit.
3. If an overrun error occurs, the SSR_FIFO.ORER flag is set to 1. If the SCR.RIE bit in SCR is 1, an SCIn_ERI interrupt request is generated. Receive data is not transferred to the FRDRL*1 register.
4. If a parity error is detected, the PER flag and receive data are transferred to the FRDRL*1 register. If the RIE bit is set to 1, an SCIn_ERI interrupt request is generated.
5. If a framing error is detected, the FER flag and receive data are transferred to the FRDRL*1 register. If the RIE bit is set to 1, an SCIn_ERI interrupt request is generated.
6. After a framing error is detected and when SCI detects that the continuous receive data is for one frame, reception stops.
7. When the amount of data stored in the FRDRL register falls below the specified receive triggering number, and the next data is not received after 15 ETUs from the last stop bit in asynchronous mode, the SSR_FIFO.DR bit is set to 1. When the RIE bit is 1 and the FCR.DRES bit is 0, the SCI generates an SCIn_RXI interrupt request. When the FCR.DRES bit is 1, SCI generates an SCIn_ERI interrupt request.
8. When reception finishes successfully, receive data is transferred to the FRDRL*1 register. The RDF bit is set to 1 when the amount of receive data written to FRDRHL is equal to or greater than the specified receive triggering number. If the SCR.RIE bit in SCR is 1, an SCIn_RXI interrupt request is generated. Continuous reception is enabled by reading the receive data transferred to the FRDRL*2 register in the SCIn_RXI interrupt handling routine, before an overrun error occurs. If the received data that is transferred to FRDRL*3 is less than the RTS trigger number, the CTSn_RTSn pin outputs low.

Note 1. Only read data in the FRDRH and FRDRL registers when 9-bit data length is selected.
Note 2. Read data in order from FRDRH to FRDRL when 9-bit data length is selected.
Note 3. The SCI only checks for update to the FRDRL register and not to the FRDRH register when 9-bit data length is selected.

FRDRL，SCI用下一个数据更新FER、PER和FRDRL寄存器中的接收数据（RDAT[8:0]）。RDF，FRDRH寄存器中的ORER和DR标志始终反映SSR_FIFO寄存器中的相关标志。

数据长度	寄存器设置		在FRDRH、FRRDL中接收数据															
			FRDRHL															
			FRDRH								FRDRL							
	SCMR.CHR1	SMR.CHR	b7	b6	b5	b4	b3	b2	b1	b0	b7	b6	b5	b4	b3	b2	b1	b0
7 bits	1	0	—	RDF	ORER	FER	PER	DR	0	0	0	7位接收数据						
8 bits	1	1	—	RDF	ORER	FER	PER	DR	0	0	8位接收数据							
9 bits	0	不在乎	—	RDF	ORER	FER	PER	DR	0	9位接收数据								

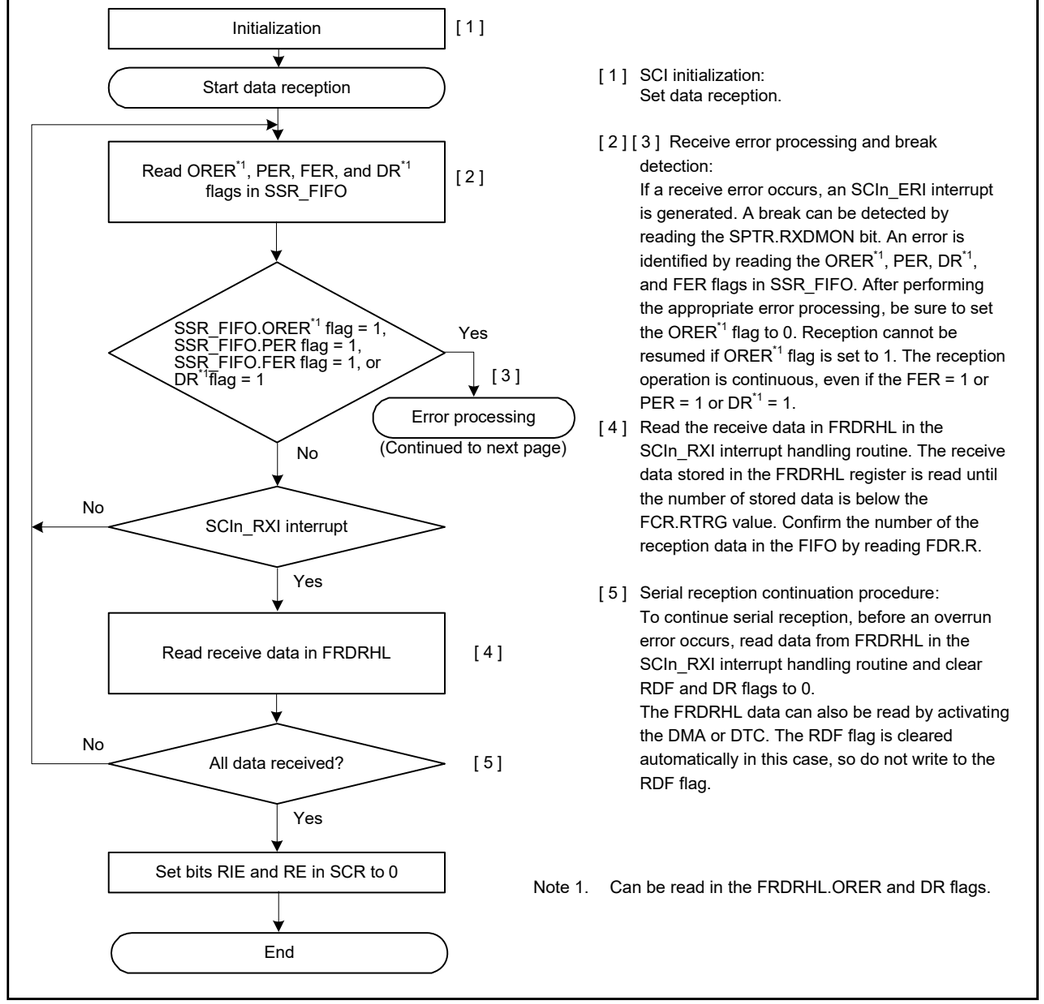
Note: MPB标志(FRDRH[1])总是读取0。当数据长度为7位时，FRRDH[0]和FRDRL[7]总是读取0。
当数据长度为8位时，FRRDH[0]总是读取0。
FRDRH[7]位被读取为不定值。

Figure 34.19 存储在FRDRH和FRDRL中的数据格式，选择了FIFO

在串行数据接收中，SCI操作如下：

1. 当SCR.RE位的值变为1时，CTSn_RTSn引脚上的输出信号变为低电平。
2. SCI监视通信线路，当它检测到起始位时，SCI执行内部同步，将接收数据存储在RSR寄存器中，并检查奇偶校验位和停止位。
3. 如果发生溢出错误，则SSR_FIFO.ORER标志设置为1。如果SCR中的SCR.RIE位为1，则产生SCIn_ERI中断请求。接收数据不传送到FRDRL*1寄存器。
4. 如果检测到奇偶校验错误，则将PER标志和接收数据传送到FRDRL*1寄存器。如果RIE位设置为1，则产生SCIn_ERI中断请求。
5. 如果检测到帧错误，则将FER标志和接收数据传送到FRDRL*1寄存器。如果RIE位设置为1，则产生SCIn_ERI中断请求。
6. 检测到帧错误后，当SCI检测到连续接收数据为一帧时，接收停止。
7. 当存储在FRDRL寄存器中的数据量低于指定的接收触发数，并且在异步模式下从最后一个停止位开始15个ETU后没有接收到下一个数据时，SSR_FIFO.DR位设置为1。当RIE位为1且FCR.DRES位为0，SCI产生一个SCIn_RXI中断请求。当FCR.DRES位为1时，SCI产生一个SCIn_ERI中断请求。
8. 当接收成功完成时，接收数据被传送到FRDRL*1寄存器。当写入FRDRHL的接收数据量等于或大于指定的接收触发数时，RDF位设置为1。如果SCR中的SCR.RIE位为1，则产生SCIn_RXI中断请求。在发生溢出错误之前，通过在SCIn_RXI中断处理例程中读取传输到FRDRL*2寄存器的接收数据来启用连续接收。如果传送到FRDRL*3的接收数据小于RTS触发数，CTSn_RTSn引脚输出低电平。

注1.选择9位数据长度时，仅读取FRDRH和FRDRL寄存器中的数据。
注2.选择9位数据长度时，按从FRDRH到FRDRL的顺序读取数据。
Note3.TheSCIonlychecksforupdatetotheFRDRLregisterandnottotheFRDRHregisterwhen9-bitdatalengthisselected.



[1] SCI initialization:
Set data reception.

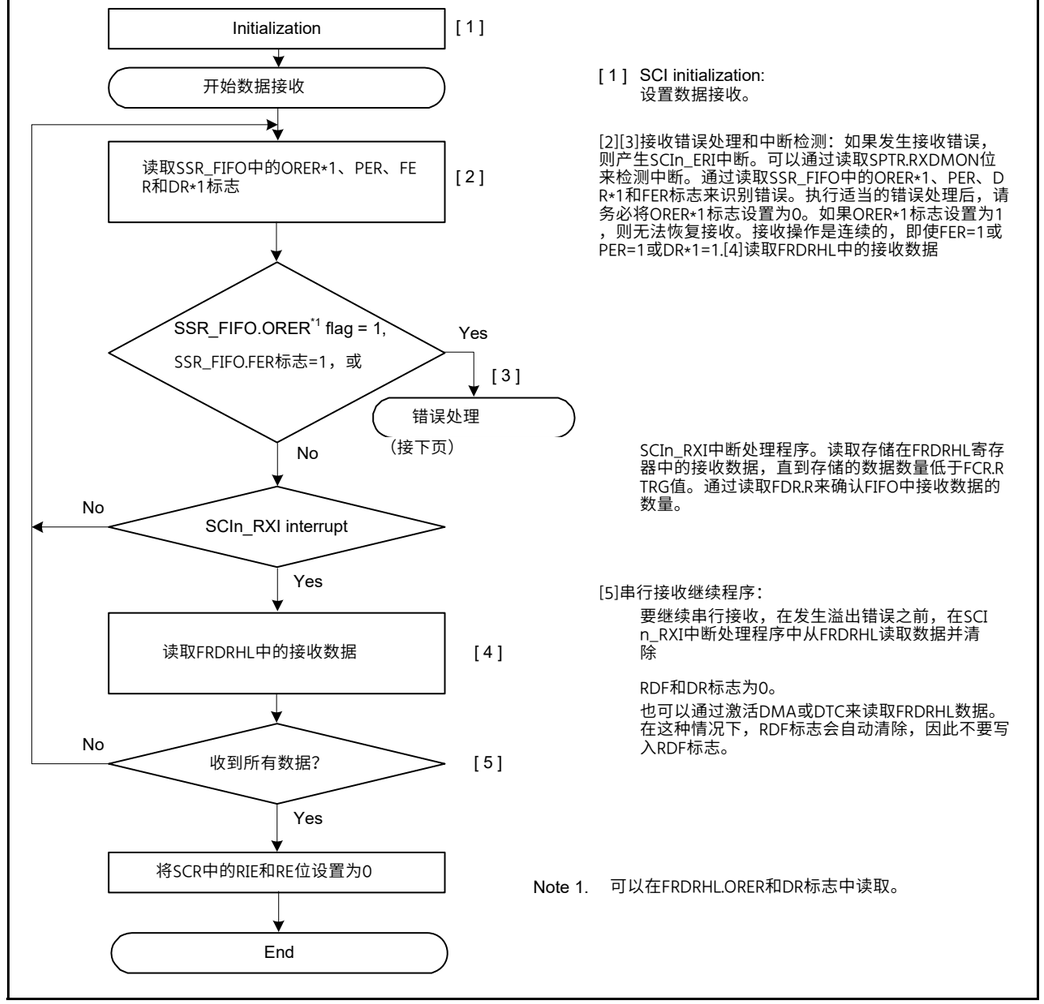
[2] [3] Receive error processing and break detection:
If a receive error occurs, an SCIn_ERI interrupt is generated. A break can be detected by reading the SPTR.RXDMON bit. An error is identified by reading the ORER*1, PER, DR*1, and FER flags in SSR_FIFO. After performing the appropriate error processing, be sure to set the ORER*1 flag to 0. Reception cannot be resumed if ORER*1 flag is set to 1. The reception operation is continuous, even if the FER = 1 or PER = 1 or DR*1 = 1.

[4] Read the receive data in FRDRHL in the SCIn_RXI interrupt handling routine. The receive data stored in the FRDRHL register is read until the number of stored data is below the FCR.RTRG value. Confirm the number of the reception data in the FIFO by reading FDR.R.

[5] Serial reception continuation procedure:
To continue serial reception, before an overrun error occurs, read data from FRDRHL in the SCIn_RXI interrupt handling routine and clear RDF and DR flags to 0.
The FRDRHL data can also be read by activating the DMA or DTC. The RDF flag is cleared automatically in this case, so do not write to the RDF flag.

Note 1. Can be read in the FRDRHL.ORER and DR flags.

Figure 34.20 Example flow of serial reception in asynchronous mode with FIFO selected (1)



[1] SCI initialization:
设置数据接收。

[2][3]接收错误处理和中断检测：如果发生接收错误，则产生SCIn_ERI中断。可以通过读取SPTR.RXDMON位来检测中断。通过读取SSR_FIFO中的ORER*1、PER、DR*1和FER标志来识别错误。执行适当的错误处理后，请务必将ORER*1标志设置为0。如果ORER*1标志设置为1，则无法恢复接收。接收操作是连续的，即使FER=1或PER=1或DR*1=1.[4]读取FRDRHL中的接收数据

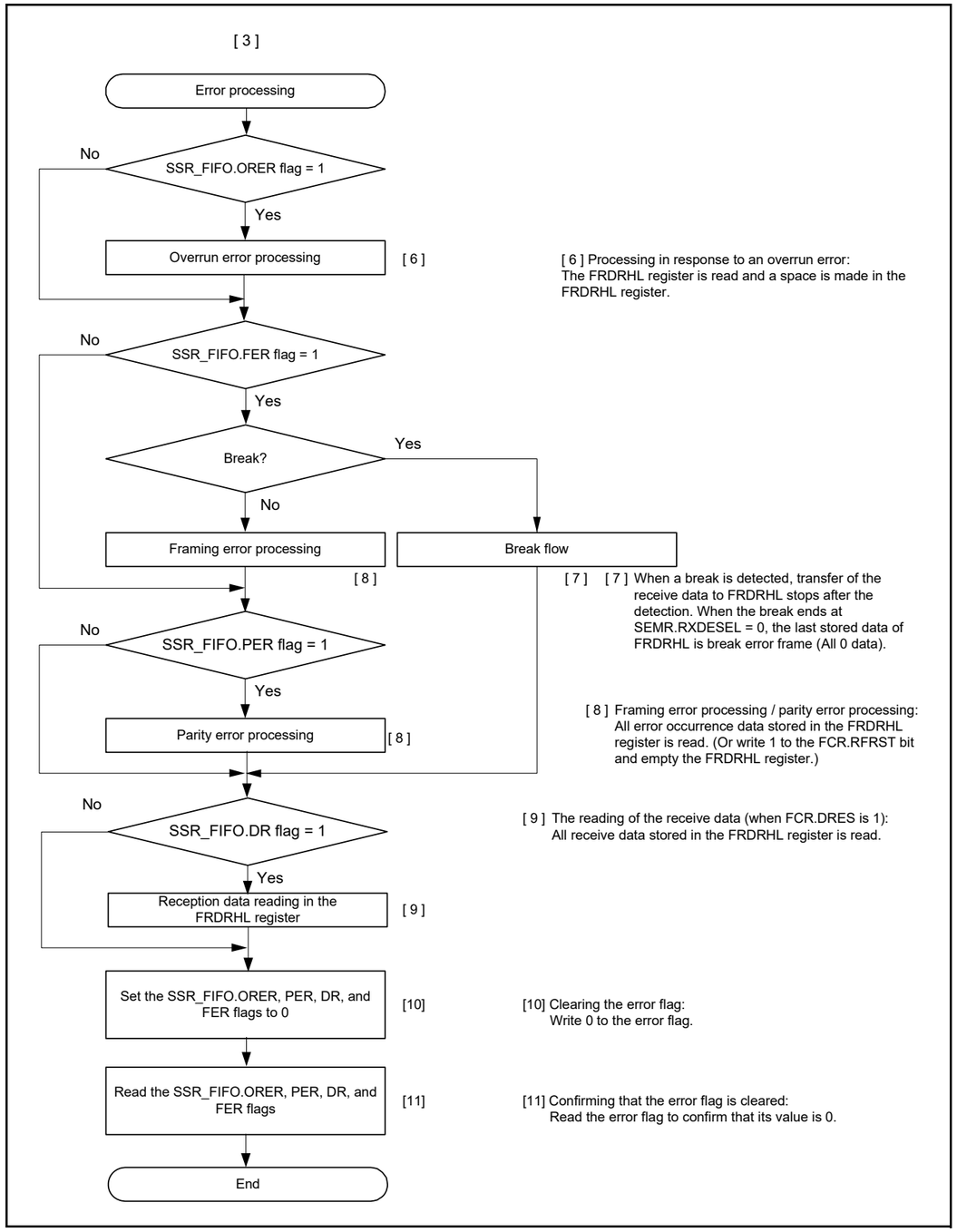
SCIn_RXI中断处理程序。读取存储在FRDRHL寄存器中的接收数据，直到存储的数据数量低于FCR.RTRG值。通过读取FDR.R来确认FIFO中接收数据的数量。

[5]串行接收继续程序：
要继续串行接收，在发生溢出错误之前，在SCIn_RXI中断处理程序中从FRDRHL读取数据并清除

RDF和DR标志为0。
也可以通过激活DMA或DTC来读取FRDRHL数据。在这种情况下，RDF标志会自动清除，因此不要写入RDF标志。

Note 1. 可以在FRDRHL.ORER和DR标志中读取。

Figure 34.20 选择FIFO的异步模式下串行接收示例流程(1)



[6] Processing in response to an overrun error:
The FRDRHL register is read and a space is made in the FRDRHL register.

[7] [7] When a break is detected, transfer of the receive data to FRDRHL stops after the detection. When the break ends at SEMR.RXDESEL = 0, the last stored data of FRDRHL is break error frame (All 0 data).

[8] Framing error processing / parity error processing:
All error occurrence data stored in the FRDRHL register is read. (Or write 1 to the FCR.RFRST bit and empty the FRDRHL register.)

[9] The reading of the receive data (when FCR.DRES is 1):
All receive data stored in the FRDRHL register is read.

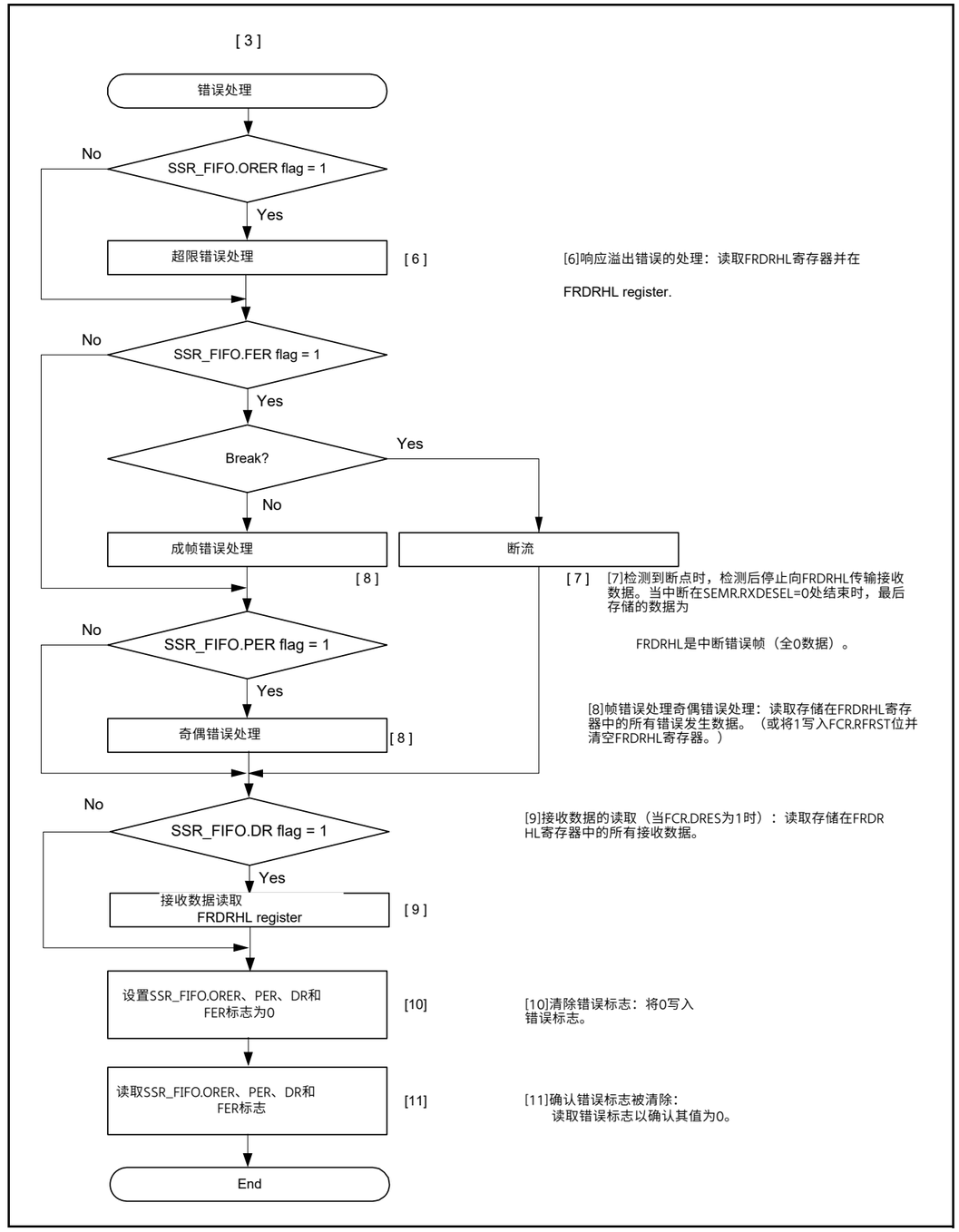
[10] Clearing the error flag:
Write 0 to the error flag.

[11] Confirming that the error flag is cleared:
Read the error flag to confirm that its value is 0.

Figure 34.21 Example flow of serial reception in asynchronous mode with FIFO selected (2)

34.4 Multi-Processor Communication Function

The multi-processor communication function enables the SCI to transmit and receive data between multiple processors



[6]响应溢出错误的处理：读取FRDRHL寄存器并在

FRDRHL register.

[7] [7]检测到断点时，检测后停止向FRDRHL传输接收数据。当中断在SEMR.RXDESEL=0处结束时，最后存储的数据为

FRDRHL是中断错误帧（全0数据）。

[8]帧错误处理奇偶错误处理：读取存储在FRDRHL寄存器中的所有错误发生数据。（或将1写入FCR.RFRST位并清空FRDRHL寄存器。）

[9]接收数据的读取（当FCR.DRES为1时）：读取存储在FRDRHL寄存器中的所有接收数据。

[10]清除错误标志：将0写入
错误标志。

[11]确认错误标志被清除：
读取错误标志以确认其值为0。

Figure 34.21 选择FIFO的异步模式下串行接收示例流程(2)

34.4 多处理器通信功能

多处理器通信功能使SCI能够在多个处理器之间发送和接收数据

by sharing an asynchronous serial communication line that has an added multi-processor bit. In multi-processor communication, a unique ID code is allocated to each receiving station. Serial communication cycles consist of an ID transmission cycle to specify the receiving station and a data transmission cycle to transmit data to the specified receiving station.

The multi-processor bit is used to distinguish between the ID transmission cycle and the data transmission cycle:

- When the multi-processor bit is set to 1, the transmission cycle is the ID transmission cycle
- When the multi-processor bit is set to 0, the transmission cycle is the data transmission cycle.

Figure 34.22 shows an example of communication between processors using a multi-processor format. First, a transmitting station transmits communication data in which the multi-processor bit set to 1 is added to the ID code of the receiving station. Next, the transmitting station transmits communication data in which the multi-processor bit set to 0 is added to the transmit data. After receiving communication data with the multi-processor bit set to 1, the receiving station compares the received ID with the ID of the receiving station itself. If the two match, the receiving station receives communication data that is subsequently transmitted. If the received ID does not match with the ID of the receiving station, the receiving station skips the communication data until it receives data in which the multi-processor bit is set to 1.

(1) Non-FIFO selected

To support this function, the SCI provides the SCR.MPIE bit. When the MPIE bit is set to 1, the following operations are disabled until the reception of data in which the multi-processor bit is set to 1:

- Transfer of receive data from the RSR register to the RDR register (the RDRHL register when 9-bit data length is selected)
- Detection of a receive error
- Setting of the respective RDRF, ORER, and FER status flags in the SSR register.

When the SCI receives a character in which the multi-processor bit is set to 1, the SSR.MPBT bit is set to 1 and the SCR.MPIE bit is automatically cleared, returning the SCI to non-multi processor reception operation. If the SCR.RIE bit is set to 1, an SCIn_RXI interrupt is generated.

When the multi-processor format is specified, the parity bit function is disabled. Apart from this, there is no difference from operation in non-multi processor asynchronous mode. The clock used for the multi-processor communication is the same as the clock used in non-multi processor asynchronous mode.

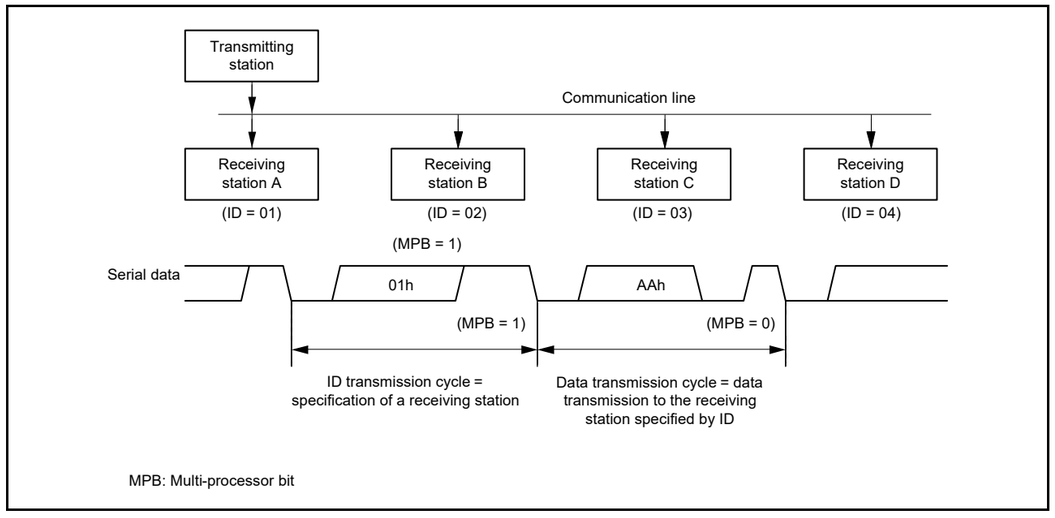


Figure 34.22 Example of communication using multi-processor format with transmission of data AAh to receiving station A

通过共享具有附加多处理器位的异步串行通信线。在多处理器通信中，为每个接收站分配一个唯一的ID代码。串行通信周期由指定接收站的ID传输周期和向指定接收站传输数据的数据传输周期组成。

多处理器位用于区分ID传输周期和数据传输周期：

- 当多处理器位设置为1时，发送周期为ID发送周期
- 当多处理器位设置为0时，传输周期为数据传输周期。

图34.22显示了使用多处理器格式的处理器之间的通信示例。首先，发送站发送将设置为1的多处理器位添加到接收站的ID码的通信数据。接着，发送站发送在发送数据中附加了多处理器比特为0的通信数据。接收站接收到多处理器位设置为1的通信数据后，将接收到的ID与接收站自身的ID进行比较。如果两者匹配，则接收站接收随后发送的通信数据。如果接收到的ID与接收站的ID不匹配，则接收站跳过通信数据，直到接收到多处理器位设置为1的数据。

(1) Non-FIFO selected

为了支持这个功能，SCI提供了SCR.MPIE位。当MPIE位设置为1时，以下操作被禁止，直到接收到多处理器位设置为1的数据：

- 将接收数据从RSR寄存器传送到RDR寄存器（选择9位数据长度时的RDRHL寄存器）
- 检测接收错误
- 在SSR寄存器中设置相应的RDRF、ORER和FER状态标志。

当SCI接收到多处理器位设置为1的字符时，SSR.MPBT位设置为1，并且SCR.MPIE位自动清零，将SCI返回到非多处理器接收操作。如果SCR.RIE位设置为1，则会产生SCIn_RXI中断。

当指定多处理器格式时，奇偶校验位功能被禁用。除此之外，与非多处理器异步模式下的操作没有区别。多处理器通信使用的时钟与非多处理器异步模式使用的时钟相同。

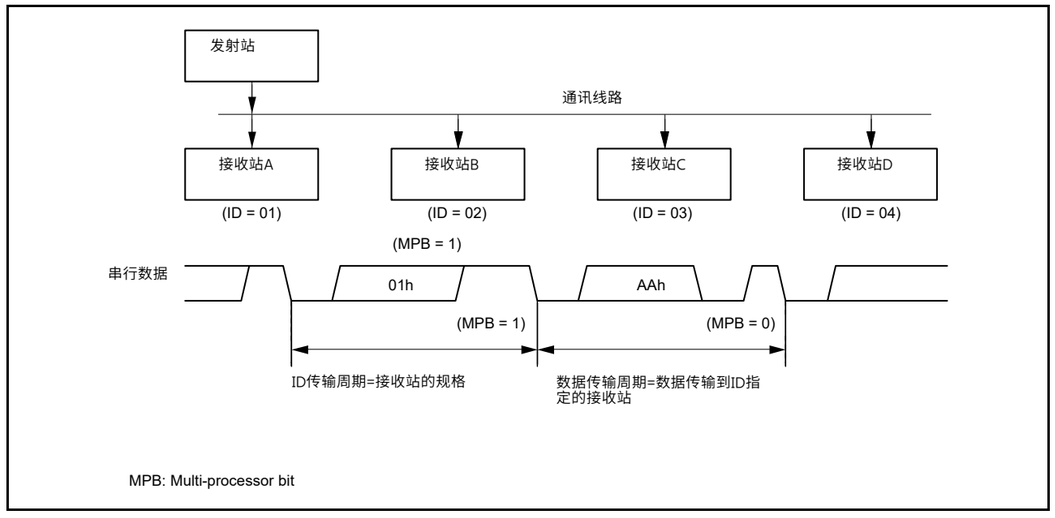


Figure 34.22 使用多处理器格式的通信示例，将数据AAh传输到接收站A

(2) FIFO selected

For data transmission, software must write data to FTDRHL.MPBT that corresponds to transmit data in FTDRHL.TDAT. For data reception, the multi-processor bit that is part of the receive data is written to FRDRHL.MPB and receive data is written to FRDRL.

When the MPIE bit is set to 1, the following operations are disabled until reception of data in which the multi-processor bit is set to 1:

- Transfer of receive data from the RSR register to the FRDRHL register
- Detection of a receive error
- Break
- Setting of the respective RDF, ORER, and FER status flags in the SSR_FIFO register.

When the SCI receives an 8-bit character in which the multi-processor bit is set to 1, the FRDRHL.MPB bit is set to 1 and receive data is written to FRDRHL.RDAT. The SCR.MPIE bit is automatically cleared, returning the SCI to non-multi processor reception operation. If the SCR.RIE bit is set to 1, an SCIn_RXI interrupt is generated.

When the multi-processor format is specified, the parity bit function is disabled. Apart from this, there is no difference from operation in non-multi processor asynchronous mode with non-FIFO selected.

34.4.1 Multi-Processor Serial Data Transmission

(1) Non-FIFO selected

Figure 34.23 shows an example flow of multi-processor data transmission. In the ID transmission cycle, the ID must be transmitted with the SSR.MPBT bit set to 1. In the data transmission cycle, the data must be transmitted with the MPBT bit set to 0. The rest of the operations are the same as operations in asynchronous mode.

(2) FIFO selected

对于数据传输，软件必须将数据写入与FTDRHL.TDAT中的传输数据相对应的FTDRHL.MPBT。对于数据接收，作为接收数据一部分的多处理器位被写入FRDRHL.MPB，接收数据被写入FRDRL。

当MPIE位设置为1时，以下操作被禁止，直到接收到多处理器位设置为1的数据：

- 将接收数据从RSR寄存器传送到FRDRHL寄存器
- 检测接收错误
- Break
- 在SSR_FIFO寄存器中设置相应的RDF、ORER和FER状态标志。

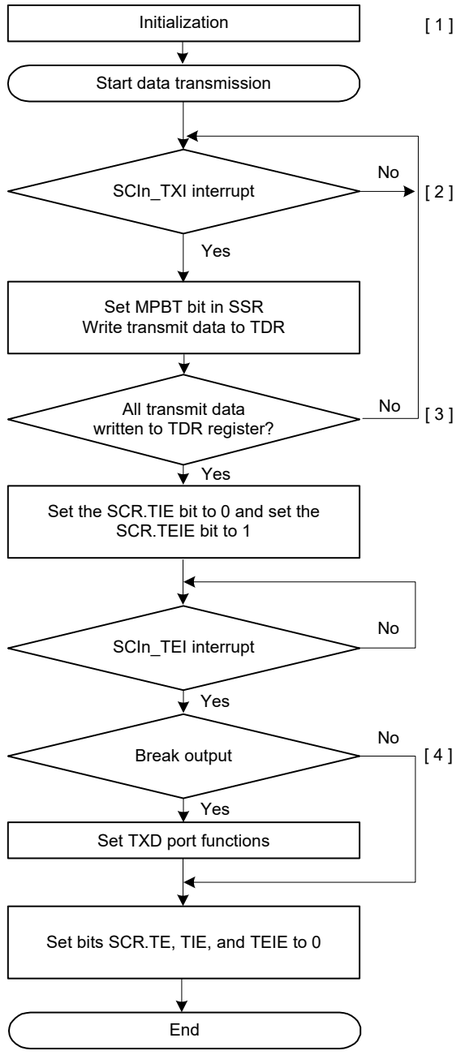
当SCI接收到多处理器位设置为1的8位字符时，FRDRHL.MPB位设置为1，接收数据写入FRDRHL.RDAT。SCR.MPIE位自动清零，将SCI返回到非多处理器接收操作。如果SCR.RIE位设置为1，则会产生SCIn_RXI中断。

当指定多处理器格式时，奇偶校验位功能被禁用。除此之外，与选择非FIFO的非多处理器异步模式下的操作没有区别。

34.4.1 多处理器串行数据传输

(1) Non-FIFO selected

图34.23显示了多处理器数据传输的示例流程。在ID传输周期，ID必须在SSR.MPBT位设置为1的情况下传输。在数据传输周期，数据必须在MPBT位设置为0的情况下传输。其余操作与操作相同在异步模式下。



[1] SCI initialization:
Set data transmission.
After the SCR.TE bit is set to 1, 1 is output for a frame, and transmission is enabled.

[2] SCIn_TXI interrupt request:
When transmit data is transferred from TDR to TSR, a transmit data empty interrupt (SCIn_TXI) request is generated.
Set the MPBT bit in SSR to 0 or 1, and write transmit data to TDR once in the SCIn_TXI interrupt processing routine.

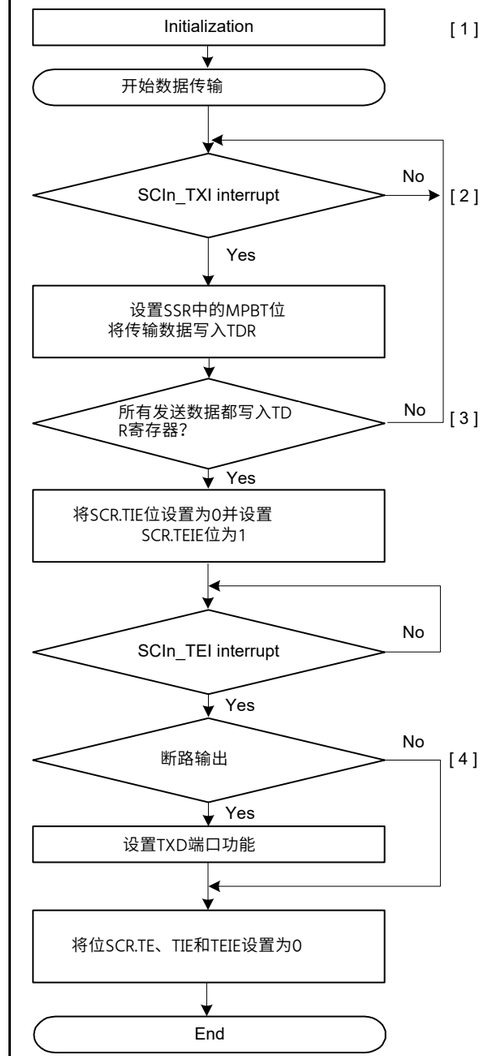
[3] Serial transmission continuation procedure:
To continue serial transmission, write transmit data to TDR once using an SCIn_TXI interrupt request.
Transmit data can also be written to TDR by activating the DMAC or DTC.
When SCIn_TEI interrupt requests are in use, set the SCR.TIE bit to 0 and the SCR.TEIE bit to 1 after the last of the data to be transmitted is written to the TDR.

[4] Break output at the end of serial transmission:
To output a break in serial transmission, after setting the output state (LOW level output) of TXDn pin by SPTR.SPB2IO and SPTR.SPB2DT bits, set the SCR.TE bit to 0.

Figure 34.23 Example flow of multi-processor serial transmission with non-FIFO selected

(2) FIFO selected

Figure 34.24 shows an example of data format that is written to FTDRH and FTDRL in multi-processor mode. The FTDRH.MPBT bit is set to 1. Data is set to FTDRH and FTDRL with the correct data length. Write 0 for unused bits. Write in order from FTDRH to FTDRL.



[1] SCI initialization:
设置数据传输。SCR.TE位设置为1后，每帧输出1，并启用传输。

[2] SCIn_TXI interrupt request:
当发送数据从TDR传输到TSR时，会产生发送数据空中断(SCIn_TXI)请求。将SSR中的MPBT位设置为0或1，并将发送数据写入

TDR在SCIn_TXI中断处理例程中执行一次。

[3] 串行传输继续程序：
要继续串行传输，请使用SCIn_TXI中断请求将传输数据写入TDR一次。发送数据也可以通过激活写入到TDR

DMAC or DTC.
当SCIn_TEI中断请求正在使用时，设置
在要发送的最后一个数据写入TDR后，SCR.TIE位为0，SCR.TEIE位为1。

[4] 串行传输结束时中断输出：
要在串行传输中输出中断，在通过SPTR.SPB2IO和SPTR.SPB2DT位设置TXDn引脚的输出状态（低电平输出）后，将SCR.TE位设置为0。

Figure 34.23 选择非FIFO的多处理器串行传输示例流程

(2) FIFO selected

图34.24显示了在多处理器模式下写入FTDRH和FTDRL的数据格式示例。这
FTDRH.MPBT位设置为1。数据设置为具有正确数据长度的FTDRH和FTDRL。为未使用的位写入0。
从FTDRH到FTDRL的顺序写。

Data Length	Register Setting		Transmit data in FTDRH, FTDRL															
			FTDRHL															
			FTDRH								FTDRL							
	SCMR.CHR1	SMR.CHR	b7	b6	b5	b4	b3	b2	b1	b0	b7	b6	b5	b4	b3	b2	b1	b0
7 bits	1	0	—	—	—	—	—	—	MPBT	—	—	7-bit transmit data						
8 bits	1	1	—	—	—	—	—	—	MPBT	—	8-bit transmit data							
9 bits	0	Don't care	—	—	—	—	—	—	MPBT	9-bit transmit data								

—: Invalid. The write value should be 0.

Figure 34.24 Data format written to FTDRH and FTDRL in multi-processor mode with FIFO selected

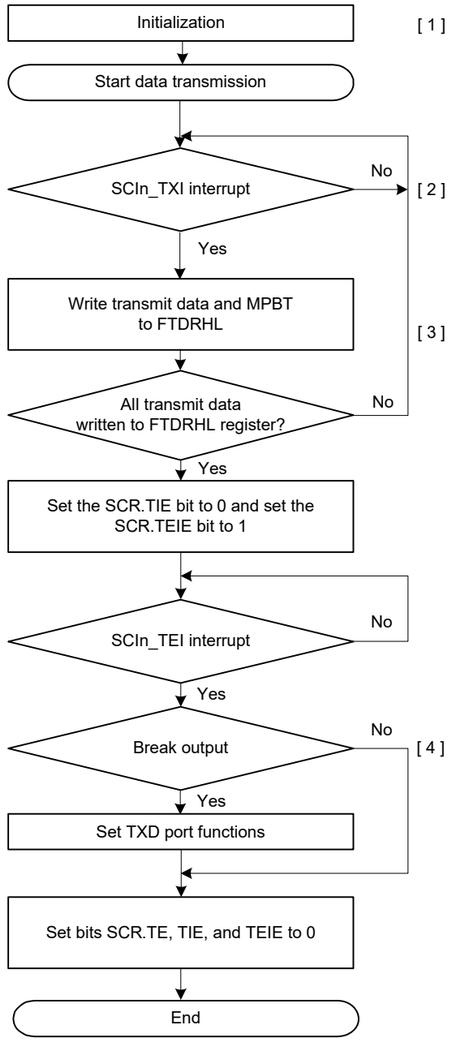
Figure 34.25 shows an example flow of multi-processor data transmission with FIFO selected. In the ID transmission cycle, the ID must be transmitted with the FTDRH.MPBT bit set to 1. In the data transmission cycle, the data must be transmitted with the MPBT bit set to 0. The rest of the operations are the same as operations in asynchronous mode with non-FIFO selected.

数据长度	寄存器设置		在FTDRH、FTDRL中传输数据															
			FTDRHL															
			FTDRH								FTDRL							
	SCMR.CHR1	SMR.CHR	b7	b6	b5	b4	b3	b2	b1	b0	b7	b6	b5	b4	b3	b2	b1	b0
7 bits	1	0	—	—	—	—	—	—	MPBT	—	—	7位传输数据						
8 bits	1	1	—	—	—	—	—	—	MPBT	—	8位传输数据							
9 bits	0	不在乎	—	—	—	—	—	—	MPBT	9位传输数据								

–：无效的。写入值应为0。

Figure 34.24 在选择FIFO的多处理器模式下写入FTDRH和FTDRL的数据格式

图34.25显示了选择FIFO的多处理器数据传输示例流程。在ID传输周期中，必须在FTDRH.MPBT位设置为1的情况下传输ID。在数据传输周期中，必须在MPBT位设置为0的情况下传输数据。其余操作与操作相同在异步模式下选择非FIFO。



[1] SCI initialization:
Set data transmission.
After the SCR.TE bit is set to 1, 1 is output for a frame, and transmission is enabled.

[2] Transmit data write to FTDRHL by an SCIn_TXI interrupt request:
When transmit data is transferred from FTDRHL to TSR, when the quantity of receive data written in FTDRHL is equal to or less than the specified transmit triggering number, a transmit data FIFO empty interrupt (SCIn_TXI) request is generated.

[3] Serial transmission continuation procedure:
To continue serial transmission, write transmit data and MPBT to FTDRHL once using an SCIn_TXI interrupt request. Transmit data can also be written to FTDRHL by activating the DTC.
When SCIn_TEI interrupt requests are in use, set the SCR.TIE bit to 0 and the SCR.TEIE bit to 1 after the last of the data to be transmitted is written to the FTDRHL.

[4] Break output at the end of serial transmission:
To output a break in serial transmission, after setting the output state (LOW level output) of TXDn pin by SPTR.SPB2IO and SPTR.SPB2DT bits, set the SCR.TE bit to 0.

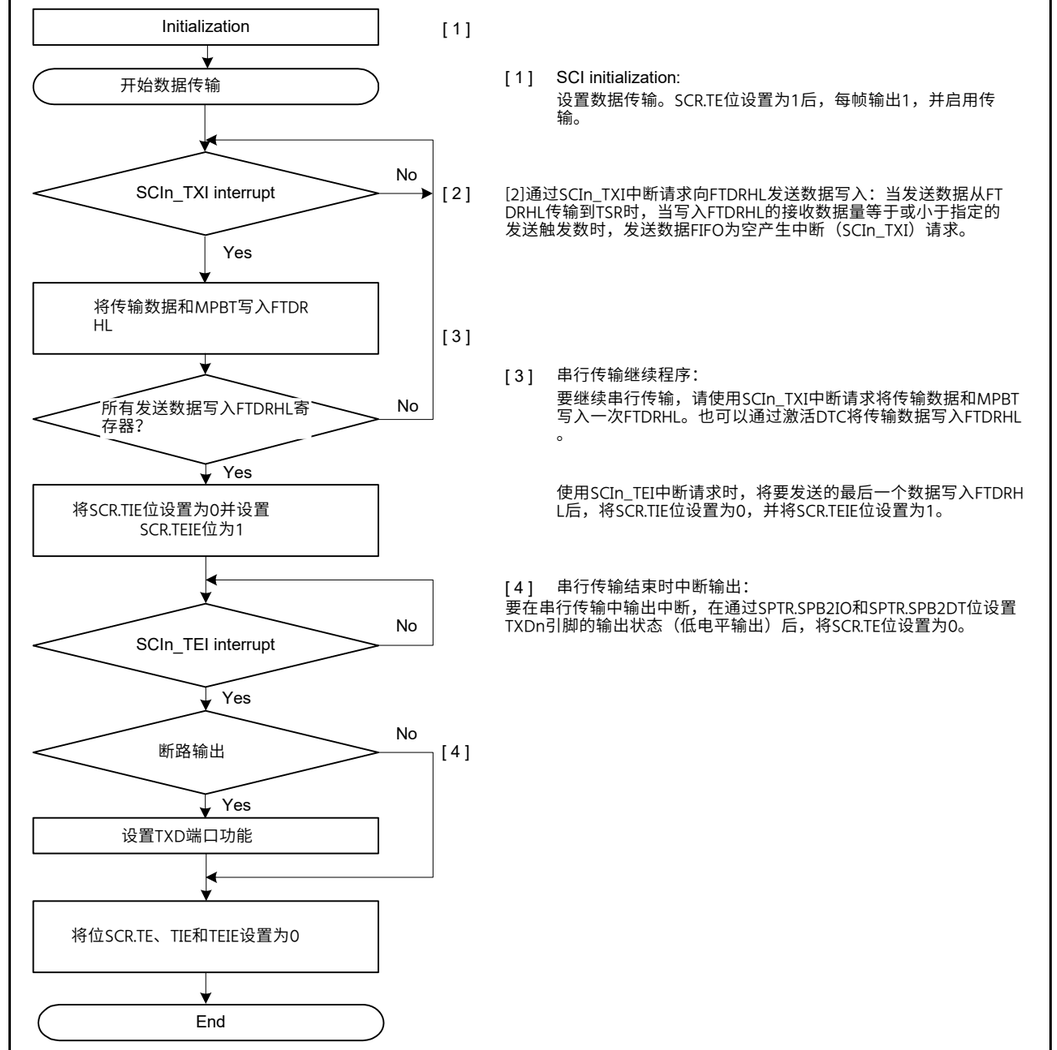
Figure 34.25 Example flow of serial transmission in multi-processor mode with FIFO selected

34.4.2 Multi-Processor Serial Data Reception

(1) Non-FIFO selected

Figure 34.27 and Figure 34.28 are example flows of multi-processor data reception. When the SCR.MPIE bit is set to 1, reading communication data is skipped until reception of communication data in which the multi-processor bit is set to 1. When communication data in which the multi-processor bit is set to 1 is received, the received data is transferred to the RDR register (the RDRHL register when 9-bit data length is selected), and the SCIn_RXI interrupt request is generated. The rest of the operations are the same as operations in asynchronous mode.

Figure 34.26 shows an example operation for data reception.



[1] SCI initialization:
设置数据传输。SCR.TE位设置为1后，每帧输出1，并启用传输。

[2] [2]通过SCIn_TXI中断请求向FTDRHL发送数据写入：当发送数据从FTDRHL传输到TSR时，当写入FTDRHL的接收数据量等于或小于指定的发送触发数时，发送数据FIFO为空产生中断（SCIn_TXI）请求。

[3] 串行传输继续程序：
要继续串行传输，请使用SCIn_TXI中断请求将传输数据和MPBT写入一次FTDRHL。也可以通过激活DTC将传输数据写入FTDRHL。

使用SCIn_TEI中断请求时，将要发送的最后一个数据写入FTDRHL后，将SCR.TIE位设置为0，并将SCR.TEIE位设置为1。

[4] 串行传输结束时中断输出：
要在串行传输中输出中断，在通过SPTR.SPB2IO和SPTR.SPB2DT位设置TXDn引脚的输出状态（低电平输出）后，将SCR.TE位设置为0。

Figure 34.25 选择FIFO的多处理器模式下的串行传输示例流程

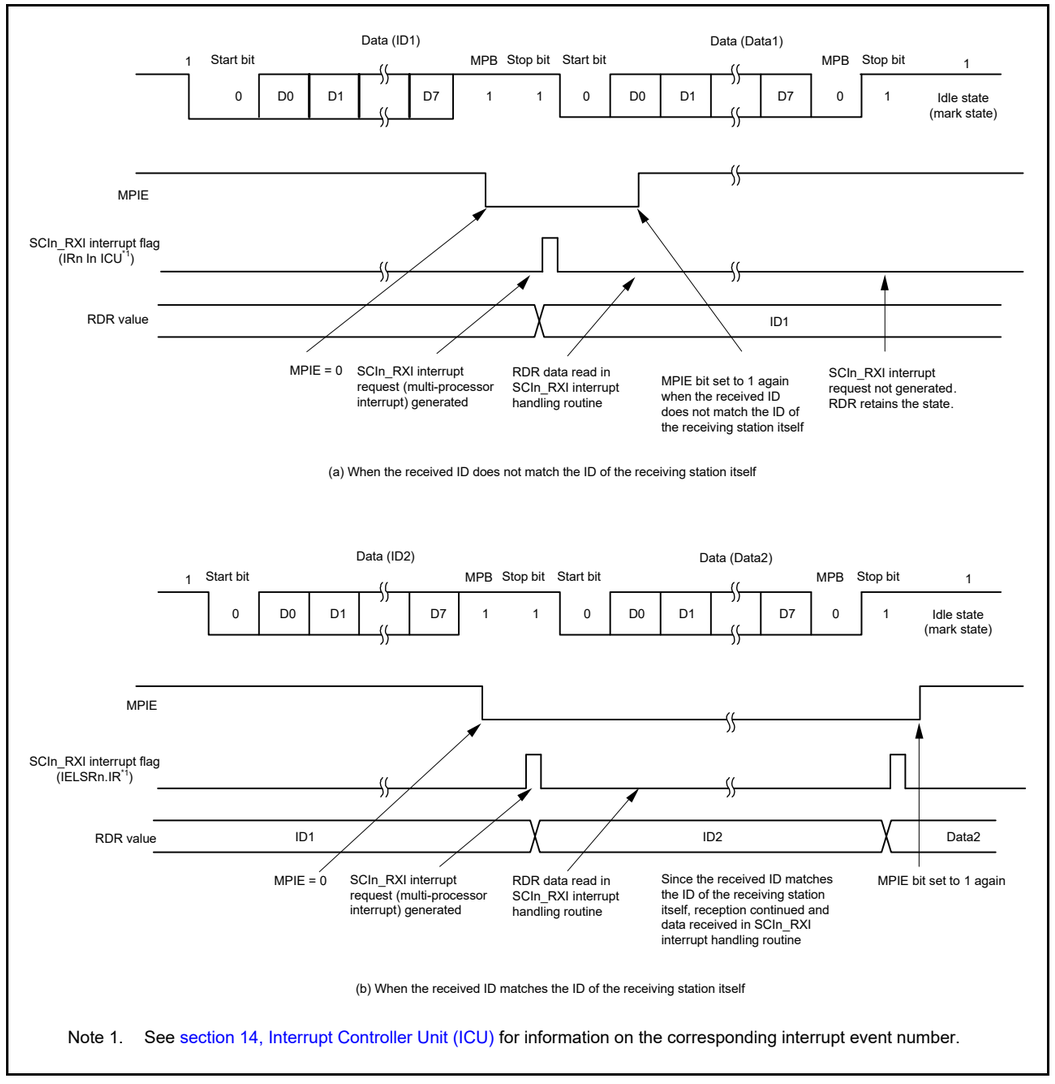
34.4.2 多处理器串行数据接收

(1) Non-FIFO selected

图34.27和图34.28是多处理器数据接收的示例流程。当SCR.MPIE位设置为1时，将跳过读取通信数据，直到接收到多处理器位设置为1的通信数据。当接收到多处理器位设置为1的通信数据时，接收到的数据传送到RDR寄存器（选择9位数据长度时为RDRHL寄存器），并产生SCIn_RXI中断请求。

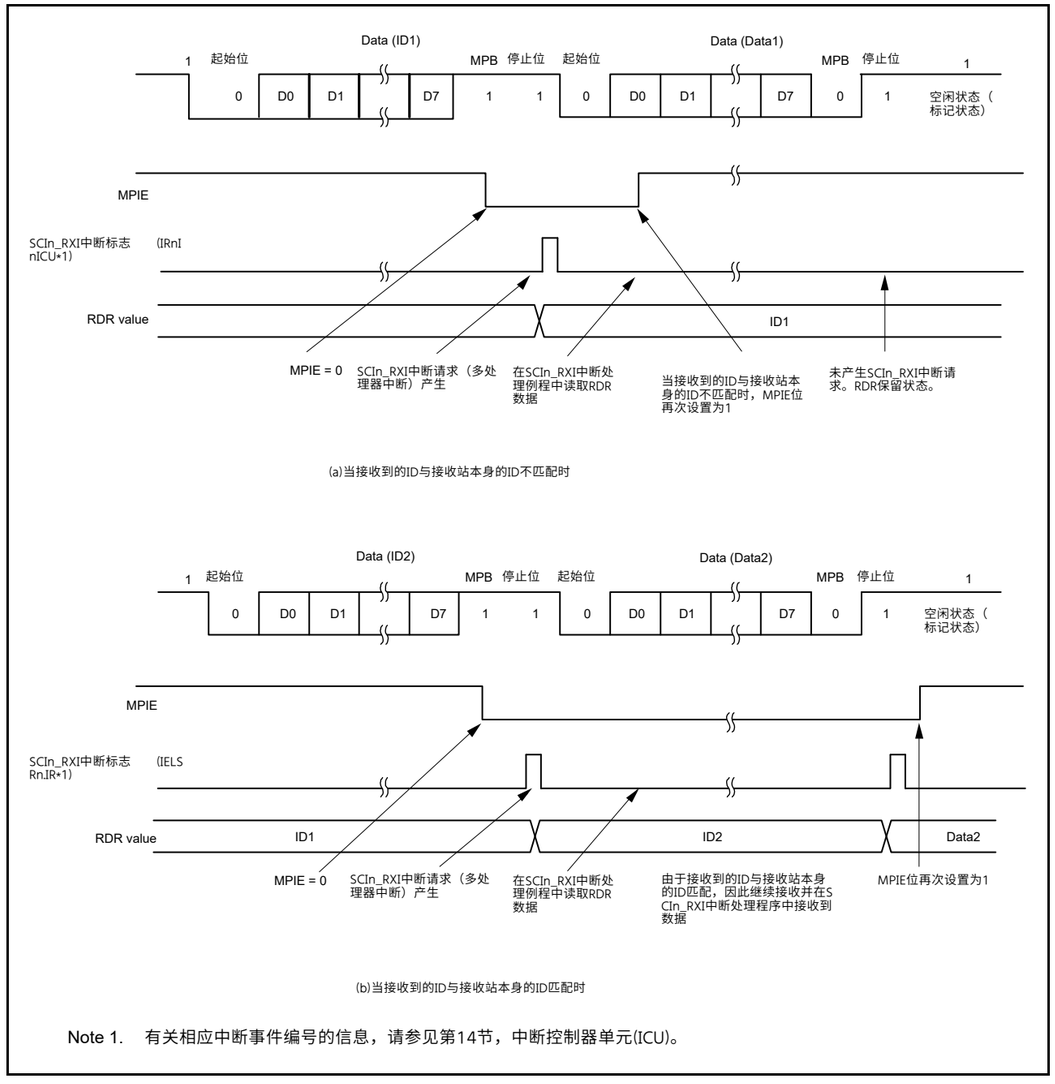
其余操作与异步模式下的操作相同。

图34.26显示了数据接收的示例操作。



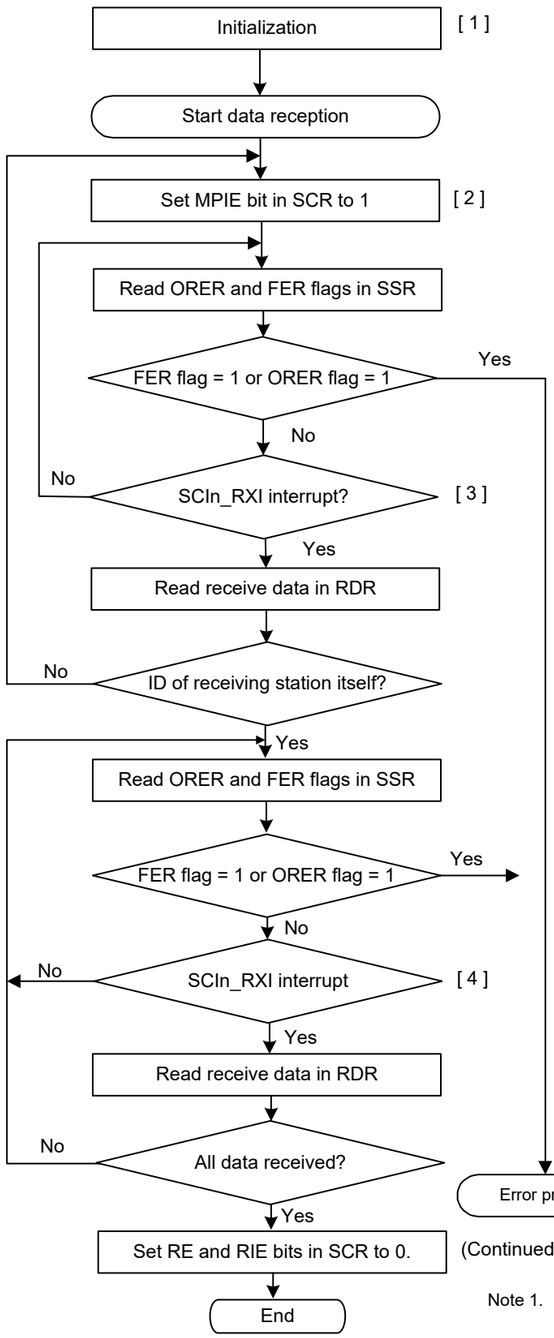
Note 1. See section 14, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 34.26 Example of SCI reception with 8-bit data, multi-processor bit, and 1 stop bit



Note 1. 有关相应中断事件编号的信息，请参见第14节，中断控制器单元(ICU)。

Figure 34.26 使用8位数据、多处理器位和1个停止位的SCI接收示例



[1] SCI initialization:
Set data reception.

[2] ID reception cycle:
Set SCR.MPIE bit to 1 and wait for ID reception.

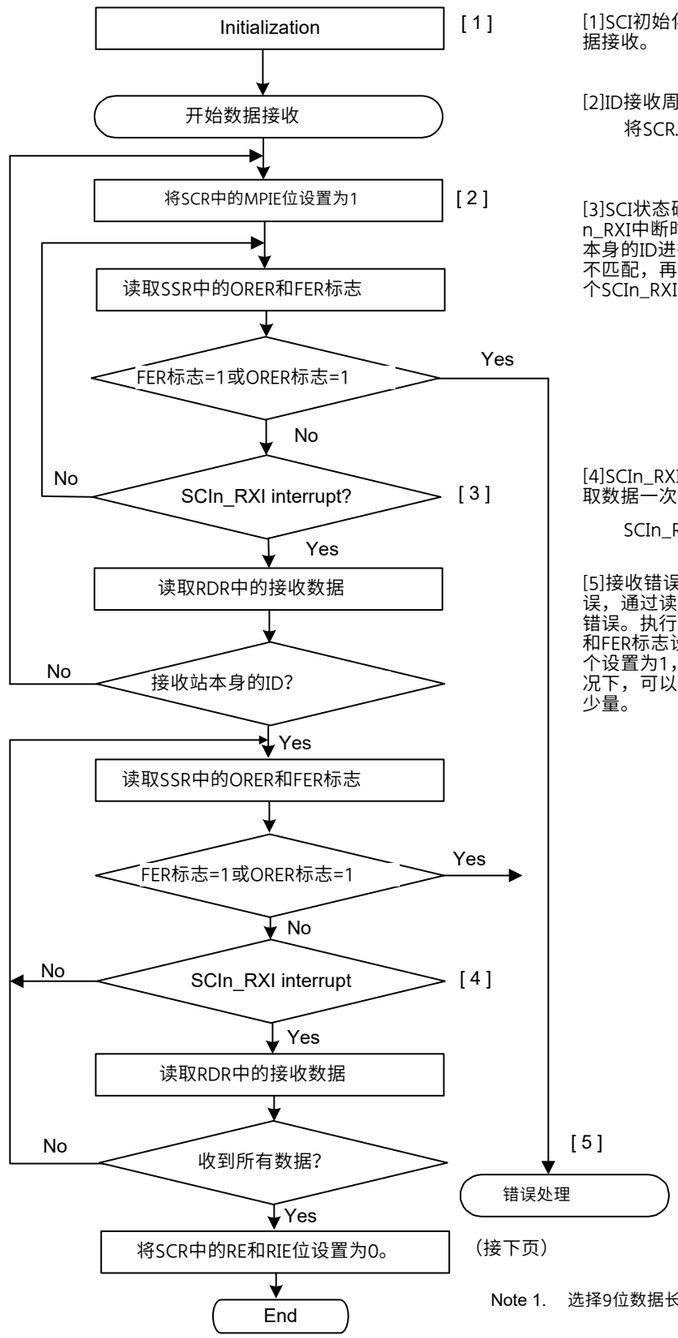
[3] SCI status confirmatIon and reception and comparison of ID:
Read data in RDR*1 at the first SCIn_RXI interrupt and compare it with the ID of the receiving statIon itself. If the ID does not match the ID of the receiving station itself, set the MPIE bit to 1 again, and wait for another SCIn_RXI interrupt request.

[4] Data reception at an SCIn_RXI interrupt:
Read data in RDR*1 once in the SCIn_RXI interrupt routine.

[5] Receive error processing and break detection:
If a receive error occurs, an error is identified by reading ORER and FER flags in SSR. After performing the appropriate error processing, be sure to set ORER and FER flags to 0. Reception cannot be resumed if any of these flags is set to 1. In the case of a framing error, a break can be detected by reading SPTR.RXDMON bit.

Note 1. The RDR register becomes the RDRHL register when 9-bit data length is selected.

Figure 34.27 Example flow of multi-processor serial reception with non-FIFO selected (1)



[1]SCI初始化：设置数据接收。

[2]ID接收周期：
将SCR.MPIE位设置为1并等待ID接收。

[3]SCI状态确认及ID接收与比较：在第一次SCIn_RXI中断时读取RDR*1中的数据，并与接收站本身的ID进行比较。如果ID与接收站本身的ID不匹配，再次将MPIE位设置为1，并等待另一个SCIn_RXI中断请求。

[4]SCIn_RXI中断时的数据接收：在RDR*1中读取数据一次

SCIn_RXI中断程序。

[5]接收错误处理和中断检测：如果发生接收错误，通过读取SSR中的ORER和FER标志来识别错误。执行适当的错误处理后，请务必将ORER和FER标志设置为0。如果这些标志中的任何一个设置为1，则无法恢复接收。在帧错误的情况下，可以通过读取SPTR.RXDMON来检测中断少量。

Note 1. 选择9位数据长度时，RDR寄存器成为RDRHL寄存器。

Figure 34.27 选择非FIFO的多处理器串行接收示例流程(1)

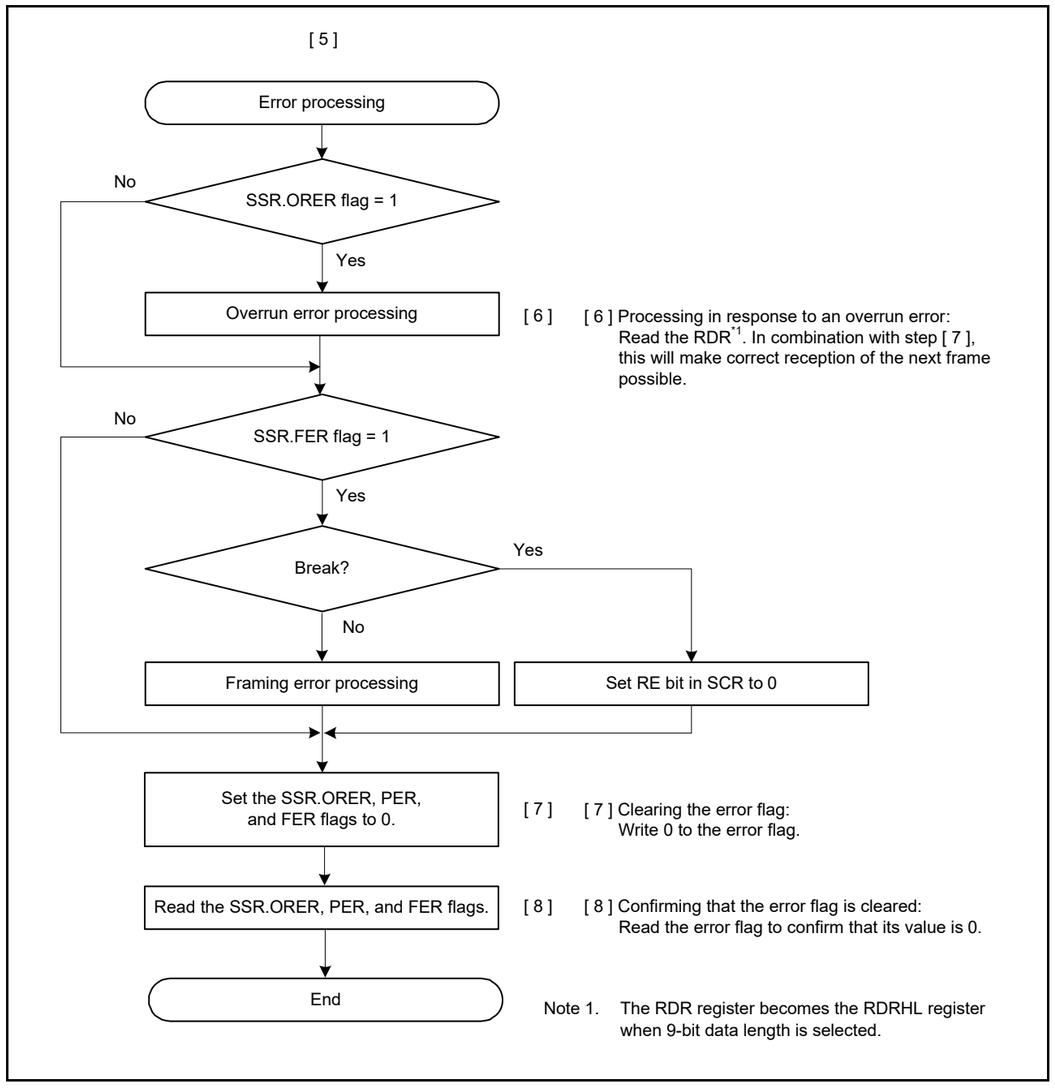


Figure 34.28 Example flow of multi-processor serial reception with non-FIFO selected (2)

(2) FIFO selected

Figure 34.29 shows an example of a data format that is written to FRDRH and FRDRL in multi-processor mode.

In multi-processor mode, the MPB value that is a part of the receive data is written to the FRDRH.MPB flag. A value of 0 is written to the FRDRH.PER flag. Data is written to FRDRH and FRDRL with the correct data length. Unused bits are written with 0. Read in order from FRDRH to FRDRL. When software reads the FRDRL register, the SCI updates FER, MPB, and receive data (RDAT[8:0]) in FRDRL with the next data. The RDF, ORER and DR flags in the FRDRH register always reflect the associated flags in the SSR_FIFO register.

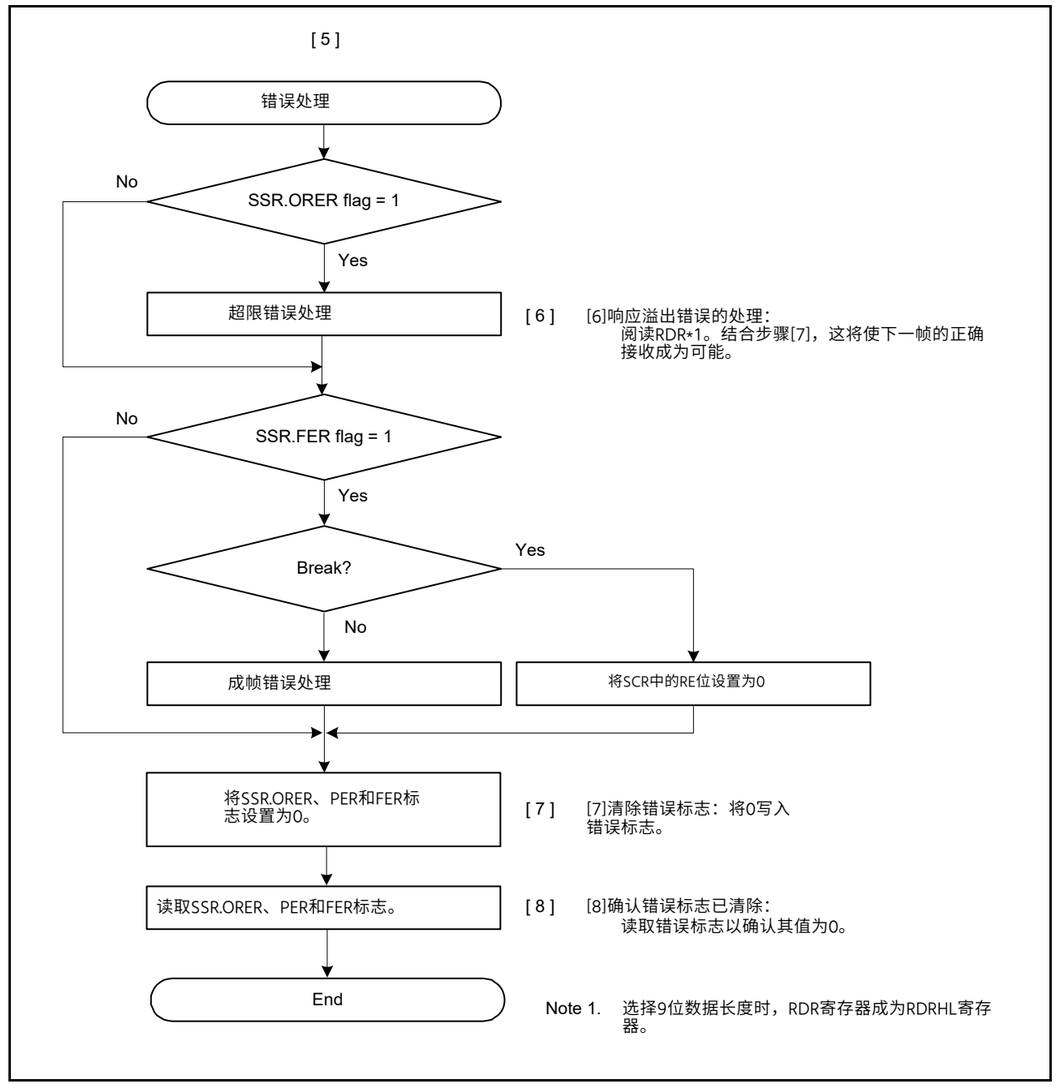


Figure 34.28 选择非FIFO的多处理器串行接收示例流程(2)

(2) FIFO selected

图34.29显示了在多处理器模式下写入FRDRH和FRDRL的数据格式示例。

在多处理器模式下，作为接收数据一部分的MPB值被写入FRDRH.MPB标志。值0写入FRDRH.PER标志。数据以正确的数据长度写入FRDRH和FRDRL。未使用的位写入0。按从FRDRH到FRDRL的顺序读取。当软件读取FRDRL寄存器时，SCI用下一个数据更新FER、MPB和FRDRL中的接收数据（RDAT[8:0]）。FRDRH寄存器中的RDF、OR ER和DR标志始终反映SSR_FIFO寄存器中的相关标志。

Data Length	Register Setting		Receive data in FRDRH, FRDRL															
			FRDRHL															
			FRDRH								FRDRL							
	SCMR.CHR1	SMR.CHR	b7	b6	b5	b4	b3	b2	b1	b0	b7	b6	b5	b4	b3	b2	b1	b0
7 bits	1	0	—	RDF	ORER	FER	0	DR	MPB	0	0	7-bit receive data						
8 bits	1	1	—	RDF	ORER	FER	0	DR	MPB	0	8-bit receive data							
9 bits	0	Don't care	—	RDF	ORER	FER	0	DR	MPB	9-bit receive data								

Note: When data length is 7 bits, 0 is always read for FRDRH[0] and FRDRL[7]
When data length is 8 bits, 0 is always read for FRDRH[0]
FRDRH[7] bit is read as an indefinite value.

Figure 34.29 Data format stored in FRDRH and FRDRL in multi-processor mode with FIFO selected

Figure 34.30 shows an example flow of multi-processor data reception with FIFO selected. When the SCR.MPIE is set to 1, reading communication data is skipped until reception of communication data in which the multi-processor bit is set to 1. When communication data in which the multi-processor bit is set to 1 is received, the received data, MPB and associated errors are transferred to the FRDRHL register. The SCR.MPIE bit is automatically cleared and non-multi processor reception continues.

If a framing error occurs and the SSR_FIFO.FER flag is set to 1, the SCI continues data reception. The rest of the operations are the same as operations in asynchronous mode with non-FIFO selected.

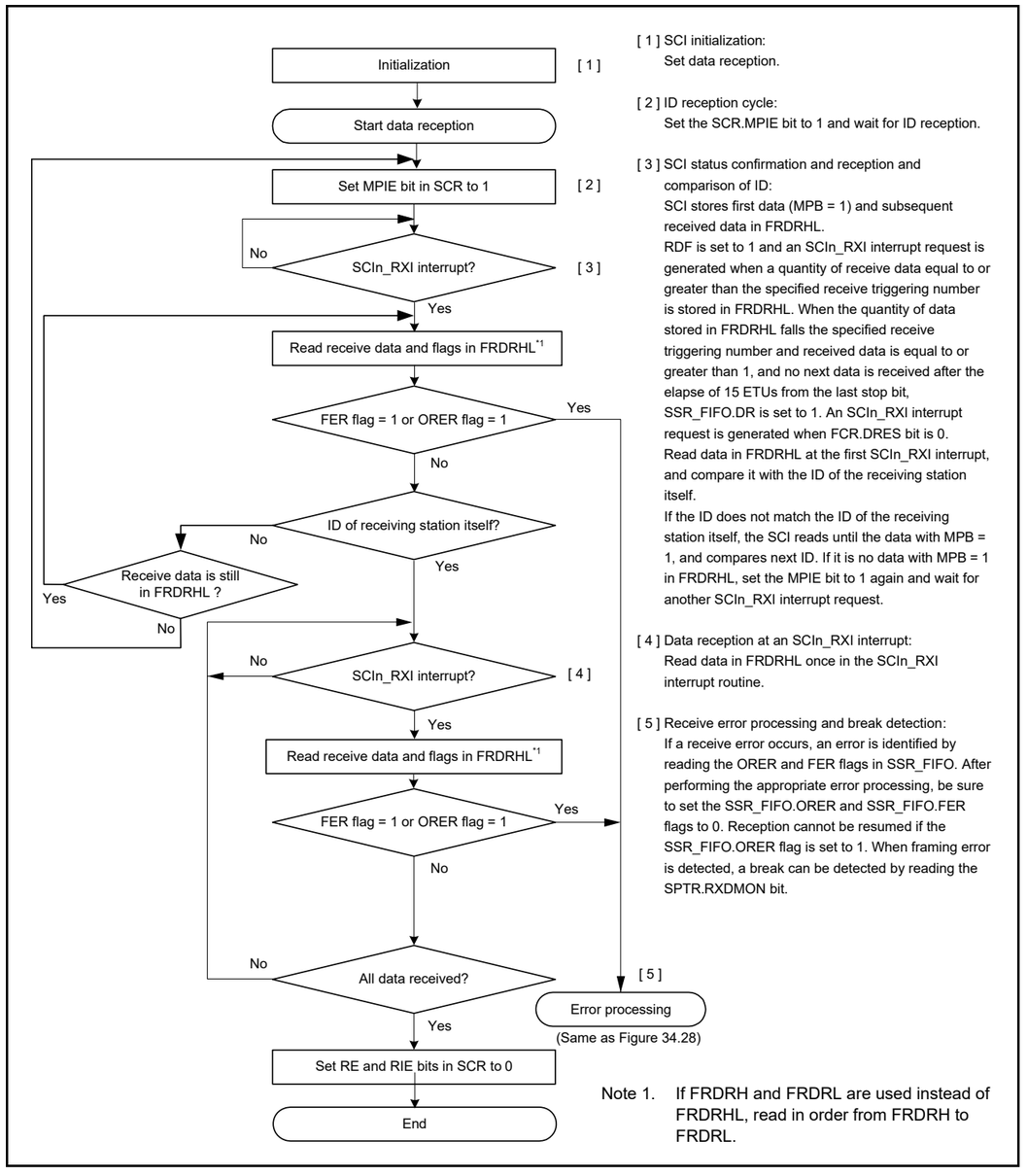
数据长度	寄存器设置		在FRDRH、FRRDL中接收数据															
			FRDRHL															
			FRDRH								FRDRL							
	SCMR.CHR1	SMR.CHR	b7	b6	b5	b4	b3	b2	b1	b0	b7	b6	b5	b4	b3	b2	b1	b0
7 bits	1	0	—	RDF	ORER	FER	0	DR	MPB	0	0	7位接收数据						
8 bits	1	1	—	RDF	ORER	FER	0	DR	MPB	0	8位接收数据							
9 bits	0	不在乎	—	RDF	ORER	FER	0	DR	MPB	9位接收数据								

Note: 当数据长度为7位时，FRRDH[0]和FRDRL[7]总是读取0
当数据长度为8位时，FRRDH[0]总是读取0
FRDRH[7]位被读取为不定值。

Figure 34.29 选择FIFO的多处理器模式下存储在FRDRH和FRDRL中的数据格式

图34.30显示了选择FIFO的多处理器数据接收示例流程。当SCR.MPIE设置为1时，将跳过读取通信数据，直到接收到多处理器位设置为1的通信数据。当接收到多处理器位设置为1的通信数据时，接收到的数据、MPB和相关错误被传送到FRDRHL寄存器。SCR.MPIE位自动清零，非多处理器接收继续。

如果发生帧错误并且SSR_FIFO.FER标志设置为1，则SCI继续数据接收。其余操作与选择非FIFO的异步模式中的操作相同。



[1] SCI initialization:
Set data reception.

[2] ID reception cycle:
Set the SCR.MPIE bit to 1 and wait for ID reception.

[3] SCI status confirmation and reception and comparison of ID:
SCI stores first data (MPB = 1) and subsequent received data in FRDRHL.
RDF is set to 1 and an SCIn_RXI interrupt request is generated when a quantity of receive data equal to or greater than the specified receive triggering number is stored in FRDRHL. When the quantity of data stored in FRDRHL falls the specified receive triggering number and received data is equal to or greater than 1, and no next data is received after the elapse of 15 ETUs from the last stop bit, SSR_FIFO.DR is set to 1. An SCIn_RXI interrupt request is generated when FCR.DRES bit is 0.
Read data in FRDRHL at the first SCIn_RXI interrupt, and compare it with the ID of the receiving station itself.
If the ID does not match the ID of the receiving station itself, the SCI reads until the data with MPB = 1, and compares next ID. If it is no data with MPB = 1 in FRDRHL, set the MPIE bit to 1 again and wait for another SCIn_RXI interrupt request.

[4] Data reception at an SCIn_RXI interrupt:
Read data in FRDRHL once in the SCIn_RXI interrupt routine.

[5] Receive error processing and break detection:
If a receive error occurs, an error is identified by reading the ORER and FER flags in SSR_FIFO. After performing the appropriate error processing, be sure to set the SSR_FIFO.ORER and SSR_FIFO.FER flags to 0. Reception cannot be resumed if the SSR_FIFO.ORER flag is set to 1. When framing error is detected, a break can be detected by reading the SPTR.RXDMON bit.

Note 1. If FRDRH and FRDRL are used instead of FRDRHL, read in order from FRDRH to FRDRL.

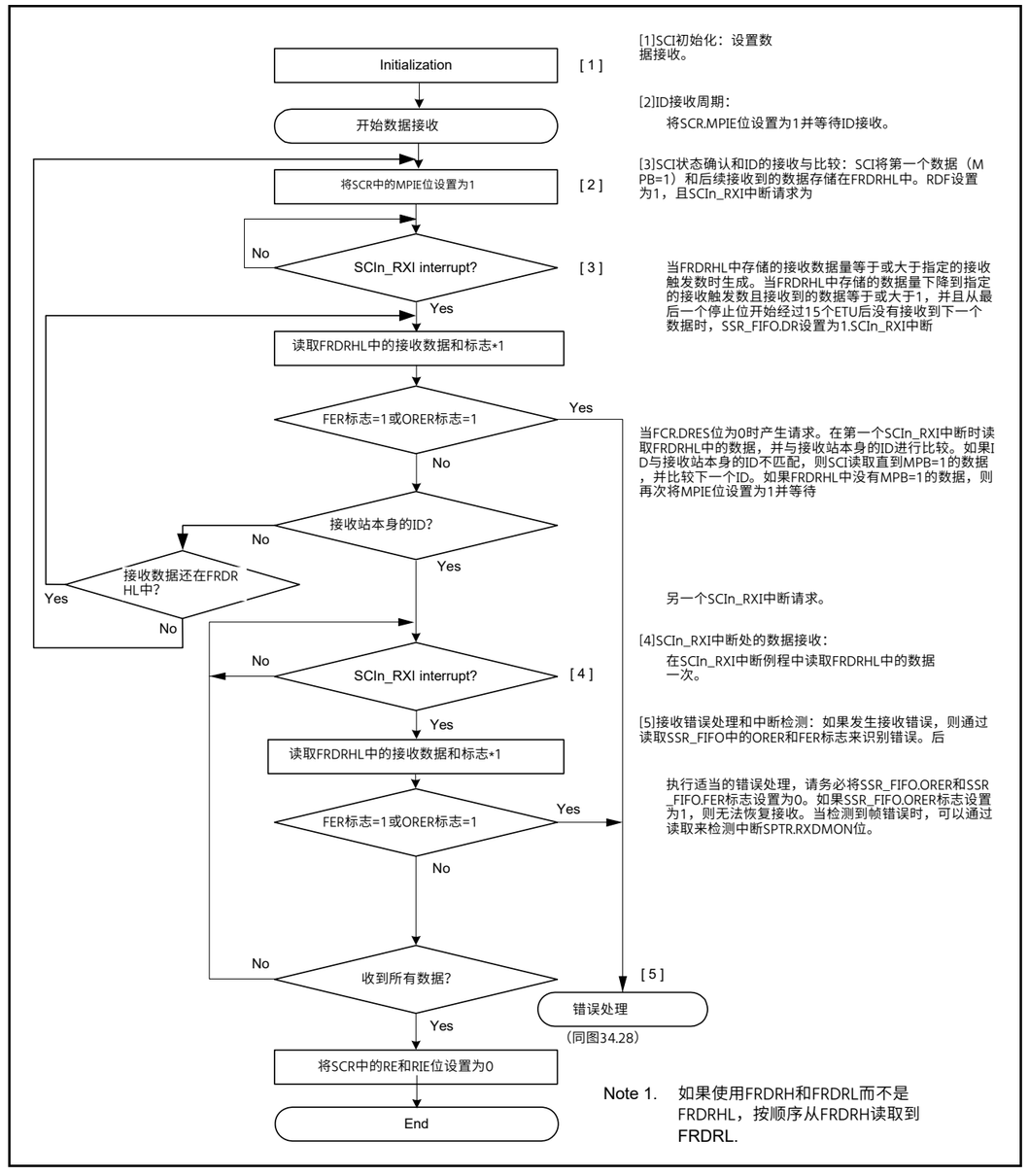
Figure 34.30 Example flow of serial reception in multi-processor mode with FIFO selected

34.5 Operation in Clock Synchronous Mode

Figure 34.31 shows the data format for clock synchronous serial data communications.

In clock synchronous mode, data is transmitted or received in synchronization with clock pulses. One character in transfer data consists of 8-bit data. In clock synchronous mode, no parity bit can be added.

In data transmission, the SCI outputs data from one falling edge of the synchronization clock to the next. In data reception, the SCI receives data in synchronization with the rising edge of the synchronization clock. After 8-bit data is output, the transmission line holds the last bit as output state. When the SPMR.CKPH bit is 1 in slave mode, the



[1]SCI初始化：设置数据接收。

[2]ID接收周期：
将SCR.MPIE位设置为1并等待ID接收。

[3]SCI状态确认和ID的接收与比较：SCI将第一个数据（MPB=1）和后续接收到的数据存储在FRDRHL中。RDF设置为1，且SCIn_RXI中断请求为

当FRDRHL中存储的接收数据量等于或大于指定的接收触发数时生成。当FRDRHL中存储的数据量下降到指定的接收触发数且接收到的数据等于或大于1，并且从最后一个停止位开始经过15个ETU后没有接收到下一个数据时，SSR_FIFO.DR设置为1.SCIn_RXI中断

当FCR.DRES位为0时产生请求。在第一个SCIn_RXI中断时读取FRDRHL中的数据，并与接收站本身的ID进行比较。如果ID与接收站本身的ID不匹配，则SCI读取直到MPB=1的数据，并比较下一个ID。如果FRDRHL中没有MPB=1的数据，则再次将MPIE位设置为1并等待

另一个SCIn_RXI中断请求。

[4]SCIn_RXI中断处的数据接收：
在SCIn_RXI中断例程中读取FRDRHL中的数据一次。

[5]接收错误处理和中断检测：如果发生接收错误，则通过读取SSR_FIFO中的ORER和FER标志来识别错误。后

执行适当的错误处理，请务必将SSR_FIFO.ORER和SSR_FIFO.FER标志设置为0。如果SSR_FIFO.ORER标志设置为1，则无法恢复接收。当检测到帧错误时，可以通过读取来检测中断SPTR.RXDMON位。

Note 1. 如果使用FRDRH和FRDRL而不是FRDRHL，按顺序从FRDRH读取到FRDRL.

Figure 34.30 选择FIFO的多处理器模式下的串行接收示例流程

34.5 时钟同步模式下的操作

图34.31显示了时钟同步串行数据通信的数据格式。

在时钟同步模式下，数据的发送或接收与时钟脉冲同步。传输数据中的一个字符由8位数据组成。在时钟同步模式下，不能添加奇偶校验位。

在数据传输中，SCI从同步时钟的一个下降沿输出数据到下一个下降沿。在数据接收中，SCI与同步时钟的上升沿同步接收数据。8位数据输出后，传输线保持最后一位作为输出状态。当SPMR.CKPH位在从模式下为1时，

transmission line holds the first bit output state.

Within the SCI, the transmitter and receiver are independent units, enabling full-duplex communications by using a shared clock. Both the transmitter and the receiver also have a double-buffered structure, so that the next transmit data can be written during transmission or the previous receive data can be read during reception, enabling continuous data transfer.

However, it is not possible to perform continuous transfer in the fastest bit rate setting (BRR[7:0] = 00h and SMR.CKS[1:0] = 00b). Therefore, when the FIFO is selected, this setting (BRR[7:0] = 00h and SMR.CKS[1:0] = 00b) is not available.

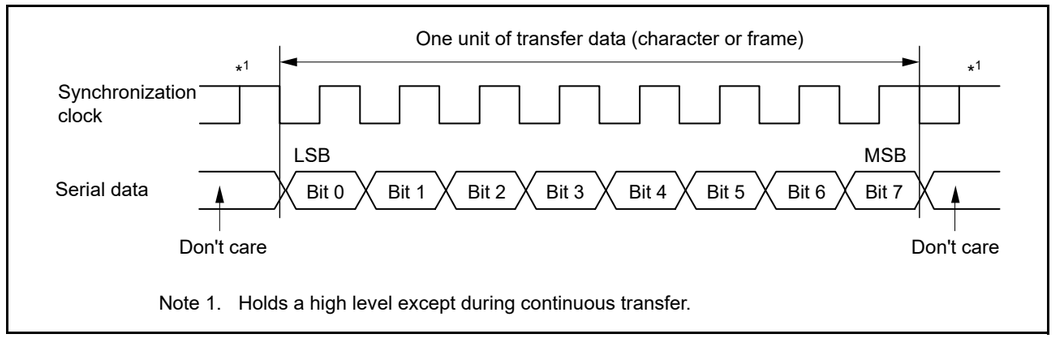


Figure 34.31 Data format in clock synchronous serial communications with LSB-first order

34.5.1 Clock

Either an internal clock generated by the on-chip baud rate generator or an external synchronization clock input at the SCKn pin can be selected based on the SCR.CKE[1:0] setting.

When the SCI operates on an internal clock, the synchronization clock is output from the SCKn pin. Eight synchronization clock pulses are output in the transfer of one character. When no transfer is performed, the clock is held high. However, when only data reception is performed while the CTS function is disabled, the synchronization clock output starts when the SCR.RE bit set to 1. The synchronization clock stops when it goes high*1 and an overrun error occurs or the SCR.RE bit is set to 0.

When only data reception is performed and the CTS function is enabled, the clock output does not start when the SCR.RE bit set to 1 and the CTSn_RTSn pin input is high. The synchronization clock output starts when the SCR.RE bit is set to 1 and the CTSn_RTSn pin input is low. Following that, when the CTSn_RTSn pin input is high on completion of the frame reception, the synchronization clock output stops when it goes high. If the CTSn_RTSn pin input continues to be low, the synchronization clock stops when it goes high*1 and an overrun error occurs or the SCR.RE bit is set to 0.

Note 1. The signal is held high while (SPMR.CKPH = 0 && SPMR.CKPOL = 0) or (SPMR.CKPH = 1 && SPMR.CKPOL = 1). It is held low while (SPMR.CKPH = 0 && SPMR.CKPOL = 1) or (SPMR.CKPH = 1 && SPMR.CKPOL = 0).

34.5.2 CTS and RTS Functions

In the CTS function, the CTSn_RTSn pin input controls the start of data reception or transmission when the clock source is the internal clock. Setting the SPMR.CTSE bit to 1 enables the CTS function. When the CTS function is enabled, setting the CTSn_RTSn pin low causes data reception or transmission to start.

Setting the CTSn_RTSn pin high while the data transmission or reception is in progress does not affect transmission or reception of the current frame.

In the RTS function, the CTSn_RTSn pin output is used to request the start of data reception or transmission when the clock source is an external synchronizing clock. The CTSn_RTSn output goes low when serial communication becomes possible. Conditions for output of the CTSn_RTSn low and high are shown as follows:

传输线保持第一位输出状态。

在SCI中，发送器和接收器是独立的单元，通过使用共享时钟实现全双工通信。发送端和接收端都具有双缓冲结构，可以在发送时写入下一个发送数据，或者在接收时读取前一个接收数据，实现数据的连续传输。

但是，在最快的比特率设置（BRR[7:0]=00h和SMR.CKS[1:0]=00b)。Therefore whentheFIFOisselected thissetting(BRR[7:0]=00handSMR.CKS[1:0]=00b)isnot available.

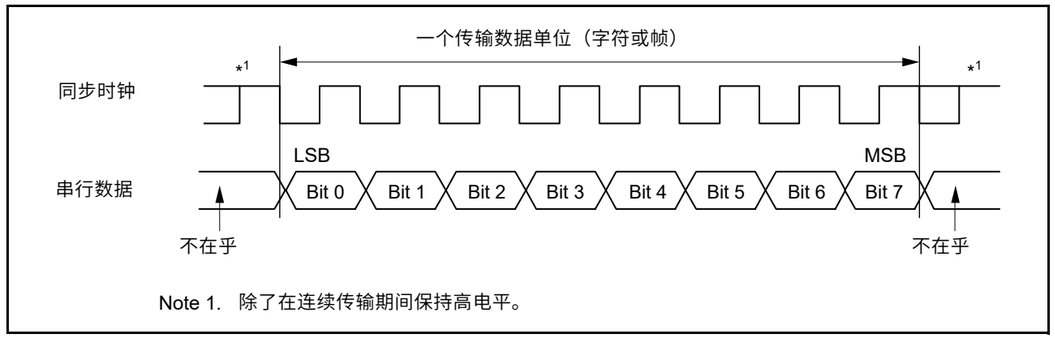


Figure 34.31 具有LSB优先顺序的时钟同步串行通信中的数据格式

34.5.1 Clock

由片内波特率发生器产生的内部时钟或外部同步时钟输入SCKn引脚可根据SCR.CKE[1:0]设置进行选择。

当SCI在内部时钟上运行时，同步时钟从SCKn引脚输出。在一个字符的传输中输出八个同步时钟脉冲。当不执行传输时，时钟保持高电平。但是，当CTS功能禁用时仅执行数据接收时，同步时钟输出在SCR.RE位设置为1时开始。同步时钟在变为高电平时停止*1并且发生溢出错误或SCR.RE位设置为0。

仅进行数据接收且使能CTS功能时，时钟输出不会在SCR.RE位设置为1，CTSn_RTSn引脚输入为高电平。当SCR.RE位设置为1且CTSn_RTSn引脚输入为低电平时，同步时钟输出开始。之后，当CTSn_RTSn引脚输入在帧接收完成时为高电平时，同步时钟输出在其变为高电平时停止。如果CTSn_RTSn引脚输入持续为低电平，则同步时钟在变为高电平时停止*1并发生溢出错误或SCR.RE位设置为0。

注1.当(SPMR.CKPH=0&&SPMR.CKPOL=0)或(SPMR.CKPH=1&&SPMR.CKPOL=1)时，信号保持高电平。它在(SPMR.CKPH=0&&SPMR.CKPOL=1)或(SPMR.CKPH=1&&SPMR.CKPOL=0)时保持低电平。

34.5.2 CTS和RTS函数

在CTS功能中，当时钟源为内部时钟时，CTSn_RTSn引脚输入控制数据接收或发送的开始。将SPMR.CTSE位设置为1可启用CTS功能。当CTS功能使能时，将CTSn_RTSn引脚设置为低电平会导致数据接收或发送开始。

在数据发送或接收过程中将CTSn_RTSn引脚设置为高电平不会影响当前帧的发送或接收。

在RTS功能中，当时钟源为外部同步时钟时，CTSn_RTSn引脚输出用于请求开始数据接收或发送。当串行通信成为可能时，CTSn_RTSn输出变为低电平。CTSn_RTSn低电平和高电平的输出条件如下所示：

[Conditions for low output]

Satisfaction of all the following conditions:

(a) Non-FIFO selected when all of the following conditions are satisfied

- The value of the SCR.RE bit or the SCR.TE bit is 1
- When serial communication is enabled
- There is no received data available to be read when the SCR.RE bit is 1
- Data is available for transmission in the TSR register when SCR.TE bit is 1
- The SSR.ORER flag is 0.

(b) FIFO selected when all of the following conditions are satisfied

- The value of the SCR.RE bit or the SCR.TE bit is 1
- When serial communication is enabled
- The amount of receive data written in FRDRHL is less than the specified CTSn_RTSn output triggering number when SCR.RE = 1
- Data that has not been transmitted is available in FTDRHL when SCR.TE bit is 1 and SCR.CKE[1] bit is 0
- Data is available for transmission in the TSR register when SCR.TE bit is 1 and SCR.CKE[1] bit is 1
- The SSR_FIFO.ORER flag is 0.

[Condition for high output]

(a) Non-FIFO selected

- The conditions for low output are not satisfied
- When reception is terminated with SCR.RE = 0 without reading the RDR register after reception is complete, RTS remains high. At this time, read the SCR register for dummy values after writing 0 to SCR.RE.

(b) FIFO selected

- The conditions for low output are not satisfied.

34.5.3 SCI Initialization in Clock Synchronous Mode

Before transmitting and receiving data, start by writing the initial value 00h to the SCR register, then continue through the SCI initialization procedure given in the sections describing non-FIFO and FIFO selection in 34.5.2 CTS and RTS Functions. Anytime the operating mode or transfer format is to be changed, the SCR register must be initialized before the change can be made.

Note: Setting the SCR.RE bit to 0 initializes neither the ORER, FER, RDRF, RDF, PER, and DR flags in SSR/SSR_FIFO nor the RDR and RDRHL register. When the TE bit is set to 0, the TEND flag for the selected FIFO buffer is not initialized.

Note: Switching the value of the SCR.TE bit from 1 to 0 or 0 to 1 when the SCR.TIE bit is 1 generates an SCIn_TXI interrupt request.

[低输出的条件]

满足以下所有条件：

(a) 满足以下所有条件时选择非FIFO

- SCR.RE位或SCR.TE位的值为1
- 启用串行通信时
- 当SCR.RE位为1时，没有可读取的接收数据
- 当SCR.TE位为1时，TSR寄存器中的数据可用于传输
- SSR.ORER标志为0。

(b) 满足以下所有条件时选择FIFO

- SCR.RE位或SCR.TE位的值为1
- 启用串行通信时
- 当SCR.RE=1时，FRDRHL中写入的接收数据量小于指定的CTSn_RTSn输出触发数
- 当SCR.TE位为1且SCR.CKE[1]位为0时，FTDRHL中的数据可用
- 当SCR.TE位为1且SCR.CKE[1]位为1时，TSR寄存器中的数据可用于传输
- SSR_FIFO.ORER标志为0。

【高输出条件】

(a) Non-FIFO selected

- 不满足低输出条件
- 当接收结束后接收结束且SCR.RE=0且未读取RDR寄存器时，RTS保持高电平。此时，将0写入SCR.RE后，读取SCR寄存器的虚拟值。

(b) FIFO selected

- 不满足低输出的条件。

34.5.3 时钟同步模式下的SCI初始化

在发送和接收数据之前，首先将初始值00h写入SCR寄存器，然后继续执行34.5.2CTS和RTS功能中描述非FIFO和FIFO选择部分中给出的SCI初始化过程。任何时候要更改操作模式或传输格式，必须先初始化SCR寄存器，然后才能进行更改。

Note: 将SCR.RE位设置为0不会初始化ORER、FER、RDRF、RDF、PER和DR标志SSRSSR_FIFO也不是RDR和RDRHL寄存器。当TE位设置为0时，选择的TEND标志FIFO缓冲区未初始化。

Note: 当SCR.TIE位为1时，将SCR.TE位的值从1切换到0或0到1会产生SCIn_TXI中断请求。

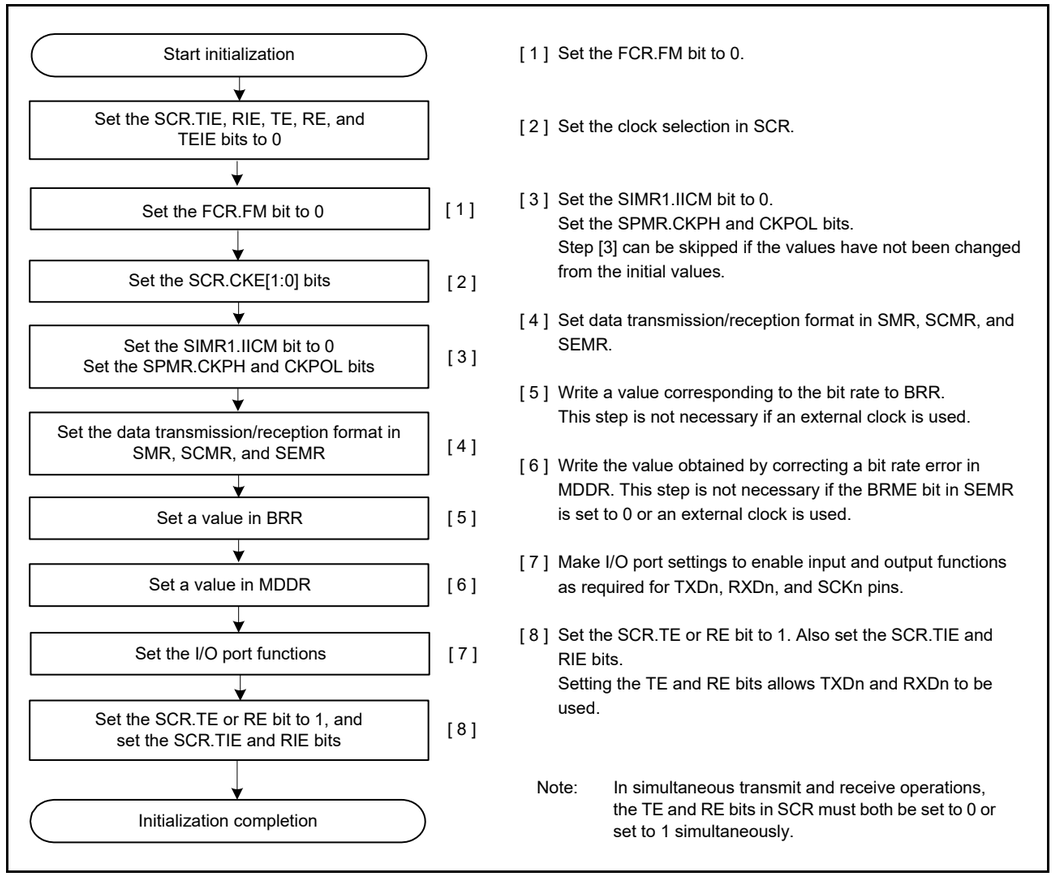


Figure 34.32 Example flow of SCI initialization in clock synchronous mode with non-FIFO selected

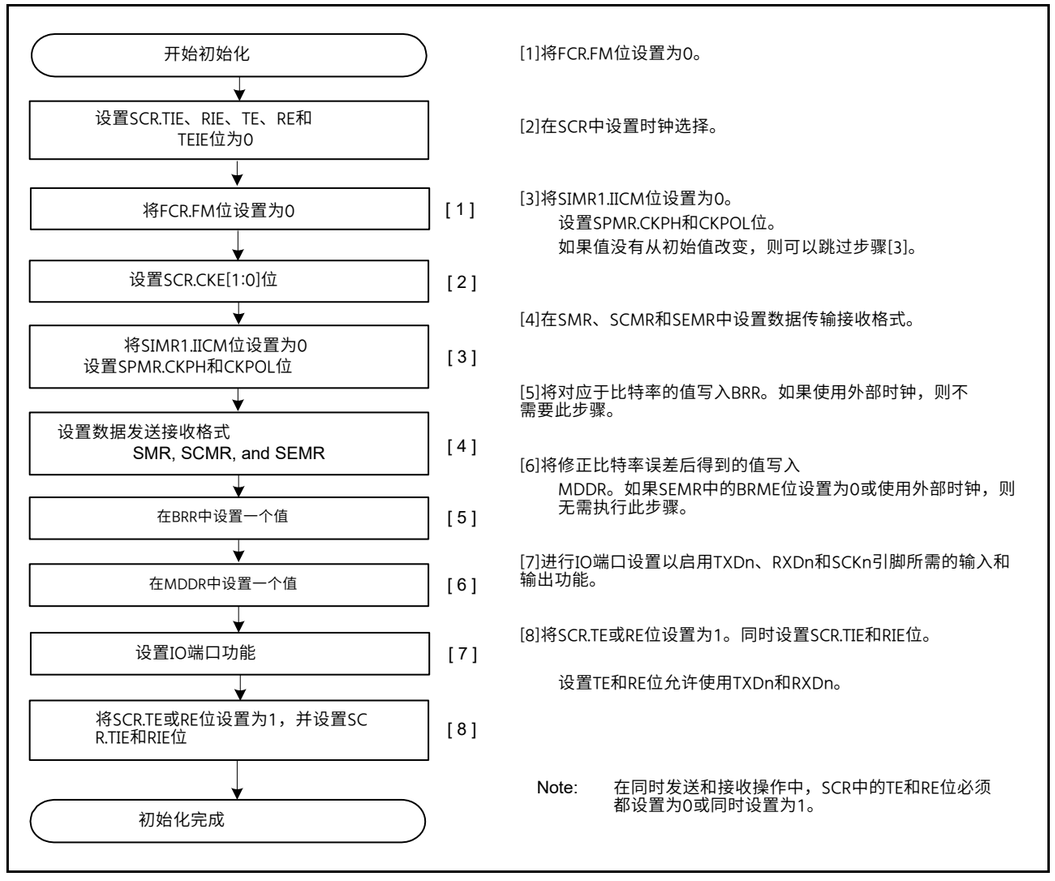


Figure 34.32 在时钟同步模式下选择非FIFO的SCI初始化示例流程

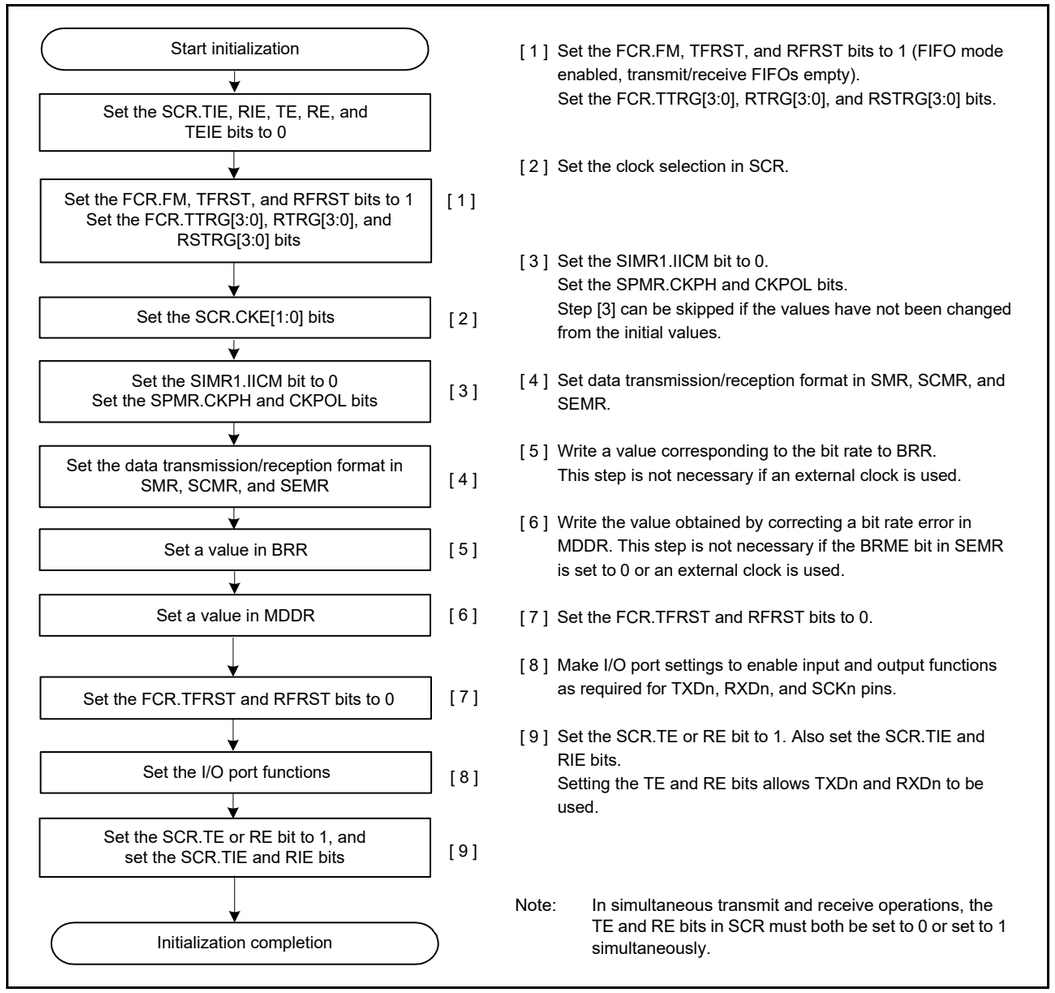


Figure 34.33 Example flow of SCI initialization in clock synchronous mode with FIFO selected

34.5.4 Serial Data Transmission in Clock Synchronous Mode

(1) Non-FIFO selected

Figure 34.34, Figure 34.35, and Figure 34.36 show examples of serial transmission in clock synchronous mode.

In serial data transmission, the SCI operates as follows:

1. The SCI transfers data from the TDR register to the TSR register when data is written to TDR in the SCIn_TXI interrupt handling routine. The SCIn_TXI interrupt request at the beginning of transmission is generated when the TE bit is set to 1 but only after the TIE bit in the SCR is also set to 1 or when these two bits are set to 1 simultaneously by a single instruction.
2. After transferring data from TDR to TSR, the SCI starts transmission. When the SCR.TIE bit is set to 1, an SCIn_TXI interrupt request is generated. Continuous transmission is enabled by writing the next transmit data to TDR in the SCIn_TXI interrupt handling routine before transmission of the current transmit data finishes. When SCIn_TEI interrupt requests are in use, set the SCR.TIE bit to 0 and the SCR.TEIE bit to 1 after the last of the data to be transmitted is written to the TDR register from the handling routine for SCIn_TXI requests.

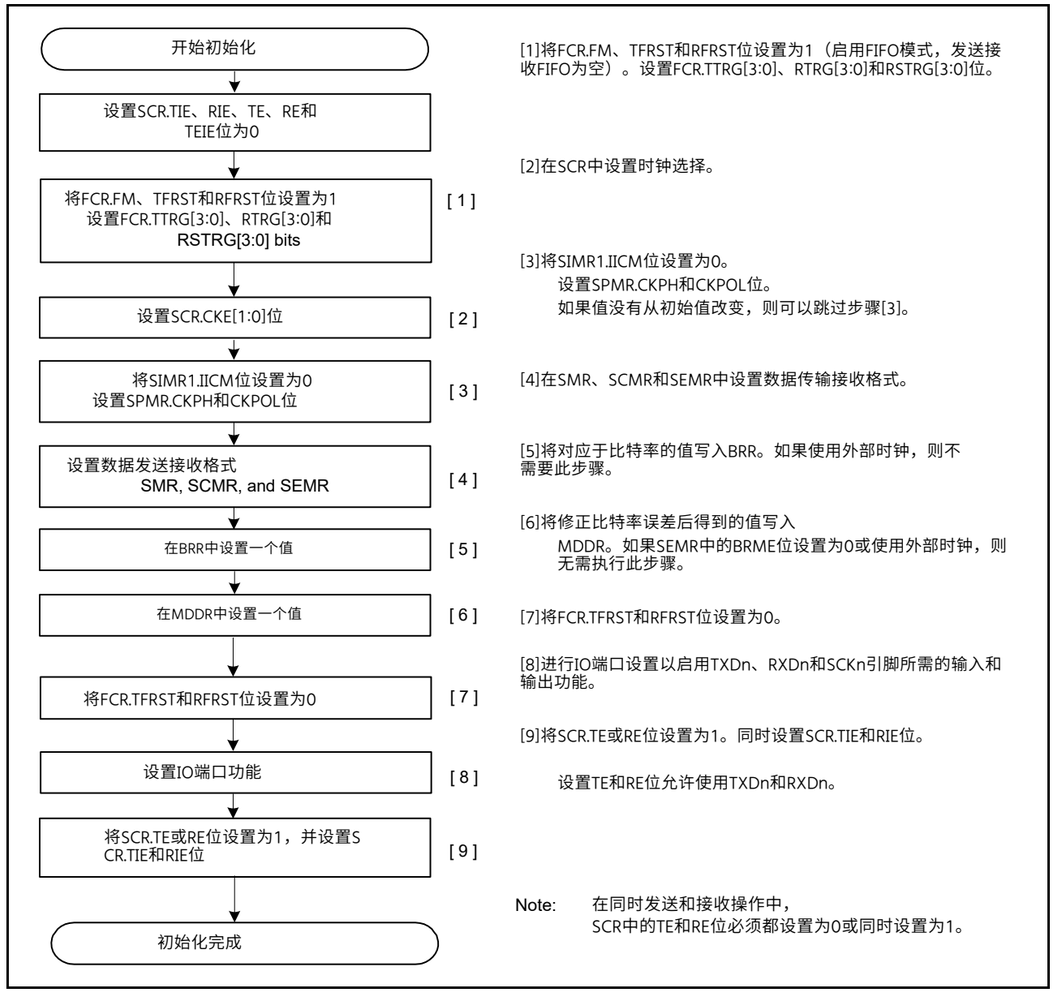


Figure 34.33 选择FIFO的时钟同步模式下的SCI初始化示例流程

34.5.4 时钟同步模式下的串行数据传输

(1) Non-FIFO selected

图34.34、图34.35和图34.36显示了时钟同步模式下的串行传输示例。

在串行数据传输中，SCI操作如下：

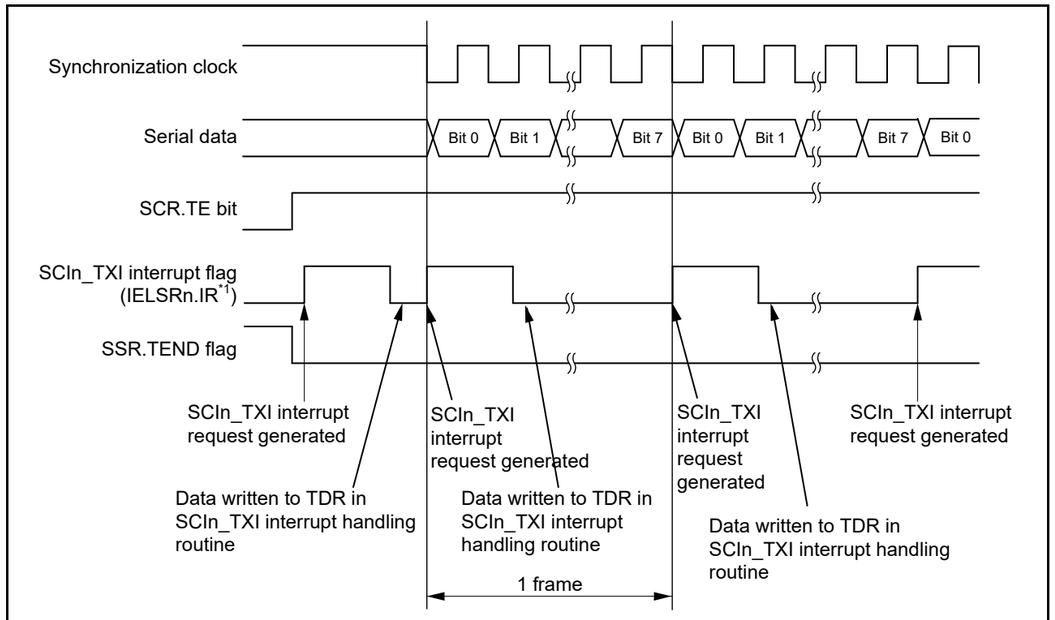
1. 当数据在SCIn_TXI中断处理程序中写入TDR时，SCI将数据从TDR寄存器传输到TSR寄存器。发送开始时的SCIn_TXI中断请求在TE位设置为1时产生，但仅在SCR中的TIE位也设置为1或当这两个位通过一条指令同时设置为1时产生。
2. 将数据从TDR传输到TSR后，SCI开始传输。当SCR.TIE位设置为1时，一个SCIn_TXI中断请求产生。在当前发送数据发送完成之前，通过在SCIn_TXI中断处理例程中将下一个发送数据写入TDR来启用连续发送。什么时候
SCIn_TEI中断请求正在使用中，在SCIn_TXI请求的处理程序将要发送的最后一个数据写入TDR寄存器后，将SCR.TIE位设置为0并将SCR.TEIE位设置为1。

3. 8-bit data is sent from the TXDn pin in synchronization with the output clock when the clock output mode is specified and in synchronization with the input clock when the use of an external clock is specified. Output of the clock signal is suspended until the input CTS signal is low when the SPMR.CTSE bit is 1.
4. The SCI checks for update to the TDR register on output of the last bit.
5. When the TDR register is updated, the next transmit data is transferred from TDR to TSR, and serial transmission of the next frame starts.
6. If TDR is not updated, the SSR.TEND flag is set to 1. The TXDn pin retains the output state of the last bit. If the SCR.TEIE bit is 1, an SCIn_TEI interrupt request is generated and the SCKn pin is held high.

Figure 34.34, Figure 34.35, and Figure 34.36 show examples of serial data transmission.

Transmission does not start while a receive error flag (ORER, FER, or PER in SSR) is set to 1. Always set the receive error flags to 0 before starting transmission.

Note: Setting the SCR.RE bit to 0 does not clear the receive error flags.



Note 1. See section 14, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

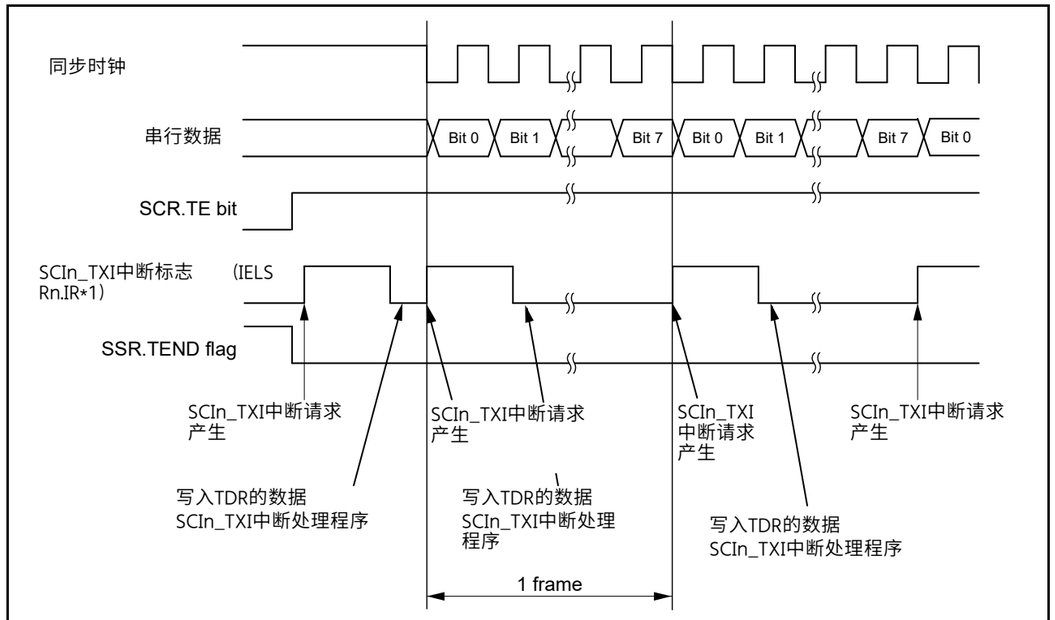
Figure 34.34 Example of serial data transmission in clock synchronous mode when the CTS function is not used at the beginning of transmission

3. 指定时钟输出模式时，与输出时钟同步，指定使用外部时钟时，与输入时钟同步，从TXDn引脚发送8位数据。当SPMR.CTSE位为1时，时钟信号的输出被暂停，直到输入CTS信号为低电平。
4. SCI在最后一位输出时检查对TDR寄存器的更新。
5. 当更新TDR寄存器时，下一个发送数据从TDR传输到TSR，并开始下一帧的串行传输。
6. 如果TDR未更新，则SSR.TEND标志设置为1。TXDn引脚保持最后一位的输出状态。如果SCR.TEIE位为1，产生SCIn_TEI中断请求且SCKn引脚保持高电平。

图34.34、图34.35和图34.36显示了串行数据传输的示例。

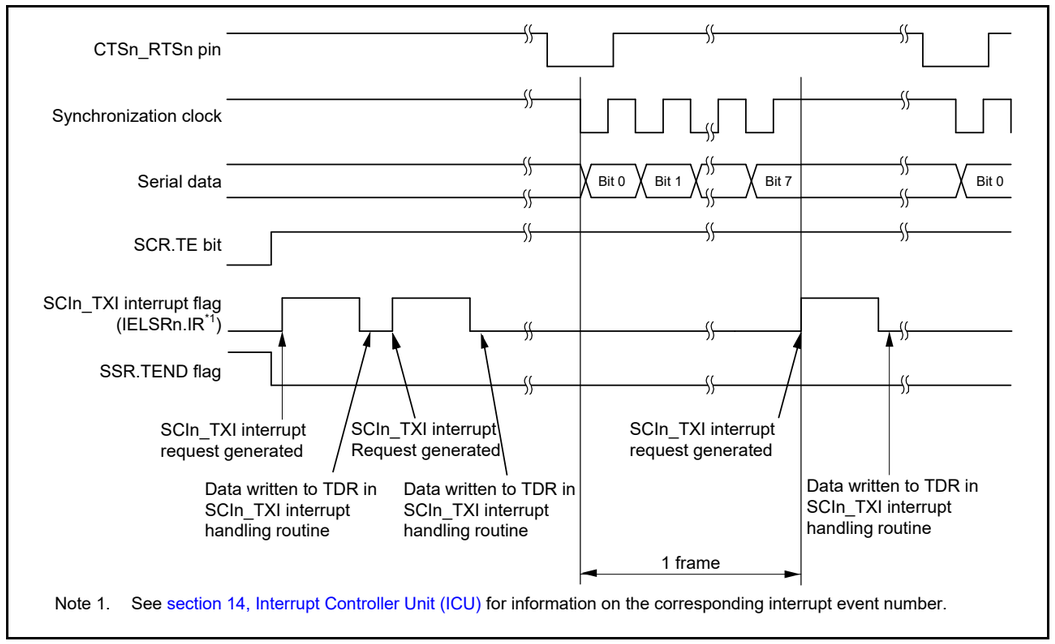
当接收错误标志（SSR中的ORER、FER或PER）设置为1时，发送不会开始。在开始发送之前，请务必将接收错误标志设置为0。

Note: 将SCR.RE位设置为0不会清除接收错误标志。



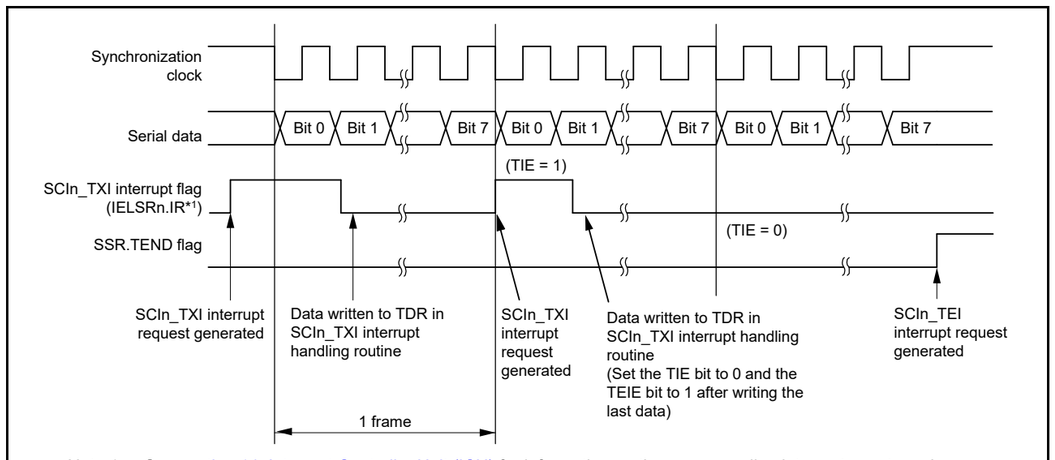
Note 1. 有关相应中断事件编号的信息，请参见第14节，中断控制器单元(ICU)。

Figure 34.34 传输开始时未使用CTS功能时时钟同步模式下的串行数据传输示例



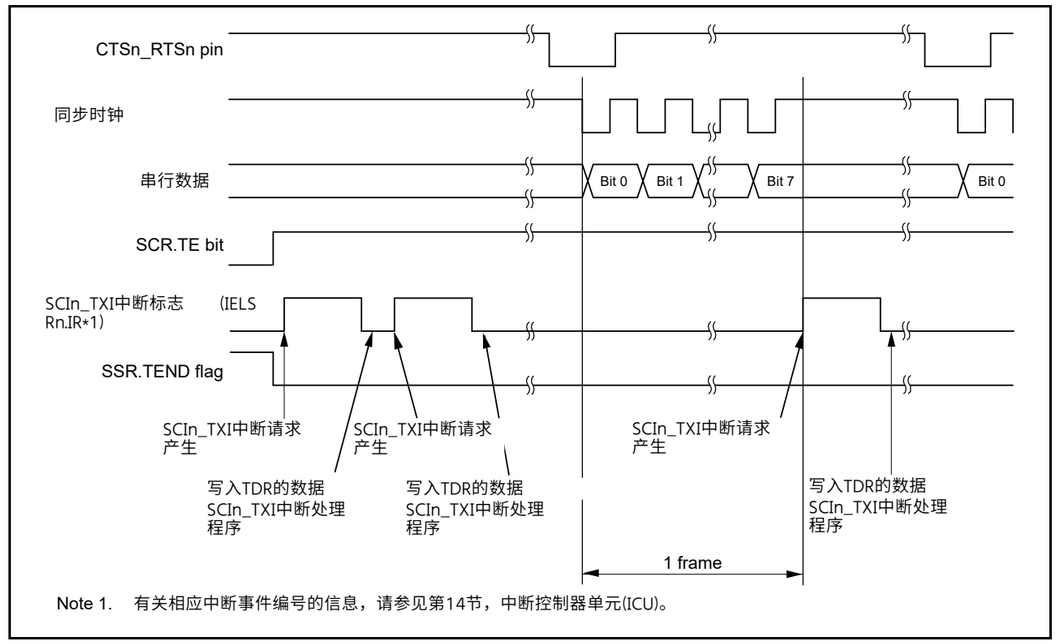
Note 1. See section 14, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 34.35 Example of serial data transmission in clock synchronous mode when the CTS function is used at the beginning of transmission



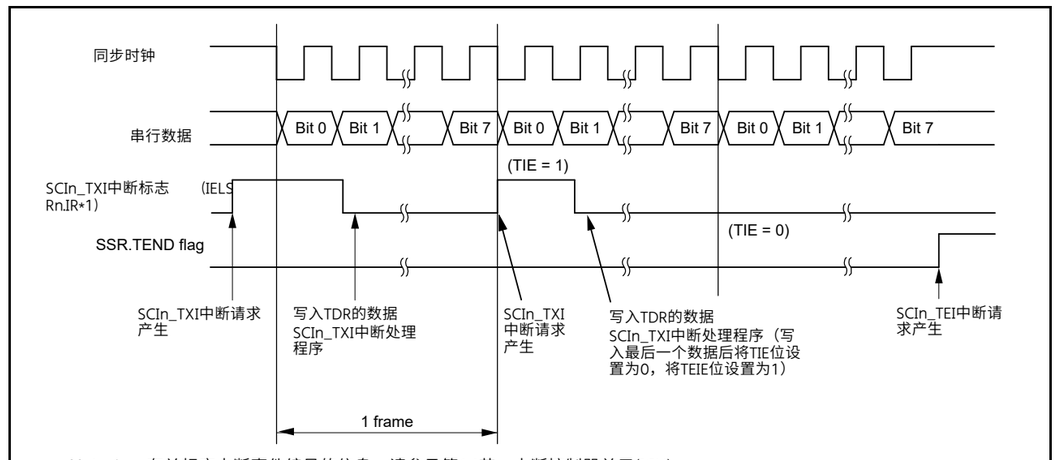
Note 1. See section 14, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 34.36 Example of serial data transmission in clock synchronous mode from the middle of transmission until transmission completion



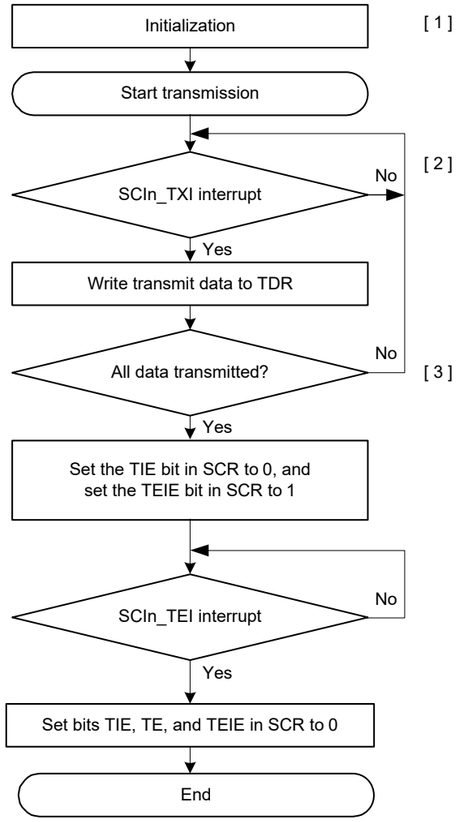
Note 1. 有关相应中断事件编号的信息，请参见第14节，中断控制器单元(ICU)。

Figure 34.35 传输开始时使用CTS功能时时钟同步模式下的串行数据传输示例



Note 1. 有关相应中断事件编号的信息，请参见第14节，中断控制器单元(ICU)。

Figure 34.36 从传输中间到传输完成的时钟同步模式下的串行数据传输示例



[1] SCI initialization:
Set data transmission.

[2] Write transmit data to TDR by an SCIn_TXI interrupt request:
When transmit data is transferred from TDR to TSR, a transmit data empty interrupt (SCIn_TXI) request is generated.
Transmit data is written to TDR once from the handling routine for SCIn_TXI requests.

[3] Serial transmission continuation procedure:
To continue serial transmission, write transmit data to TDR on accepting a transmit data empty interrupt (SCIn_TXI) request.
Transmit data can also be written to TDR by activating the DMAC or DTC by the SCIn_TXI interrupt request.
When SCIn_TEI interrupt requests are in use, set the SCR.TIE bit to 0 and the SCR.TEIE bit to 1 after the last of the data to be transmitted is written to TDR.

Note: When the external clock is in use (the value of the SCR.CKE[1:0] bits is 10b or 11b), the rising edge on the SCK pin for the last bit sets the SSR.TEND flag to 1. Setting the SCR.TE bit to 0 immediately after this might lead to insufficient received-data hold time on the receiver side.

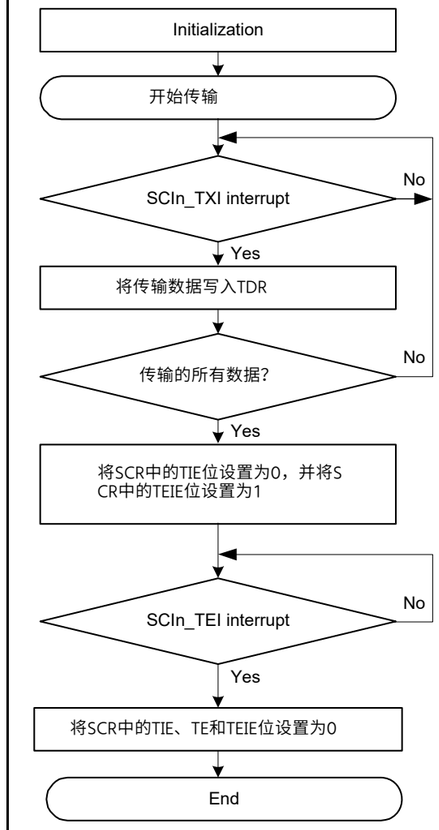
Figure 34.37 Example flow of serial transmission in clock synchronous mode with non-FIFO selected

(2) FIFO selected

Figure 34.38 shows an example of serial transmission in clock synchronous mode with FIFO selected.

In serial data transmission, the SCI operates as follows:

1. The SCI transfers data from the FTDRL*1 register to the TSR register when data is written to FTDRL*1 in the SCIn_TXI interrupt handling routine. The amount of data that can be written to FTDRL is 16 minus FDR.T[4:0] bytes. The SCIn_TXI interrupt request at the beginning of transmission is generated when the SCR.TE bit is set to 1 but only after the SCR.TIE bit is also set to 1 or when these two bits are set to 1 simultaneously by a single instruction.
2. After transferring data from FTDRL to TSR, the SCI starts transmission. When the amount of transmit data written in FTDRL is equal to or less than the specified transmit triggering number, the SSR_FIFO.TDFE is set to 1. When the SCR.TIE bit is set to 1, an SCIn_TXI interrupt request is generated. Continuous transmission is enabled by writing the next transmit data to FTDRL in the SCIn_TXI interrupt handling routine before transmission of the current transmit data has finished. When SCIn_TEI interrupt requests are in use, set the SCR.TIE bit to 0 and the SCR.TEIE bit to 1 after the last of the data to be transmitted is written to the FTDRL from the handling routine for SCIn_TXI requests.



[1]SCI初始化：设置数
据传输。

[2]通过SCIn_TXI中断请求将发送数据写入TDR：当发送数据从TD
R传输到TSR时，会产生发送数据空中断（SCIn_TXI）请求。传输
数据从SCIn_TXI请求的处理例程中写入一次TDR。

[3]串行传输继续程序：要继续串行传输，在接受传输数据空中
断（SCIn_TXI）请求时将传输数据写入TDR。发送数据也可以
通过激活写入到TDR

DMAC或DTC由SCIn_TXI中断请求。
使用SCIn_TEI中断请求时，将要发送的最后一个数据写入TDR后
，将SCR.TIE位设置为0，并将SCR.TEIE位设置为1。

Note: 当使用外部时钟时（SCR.CKE[1:0]位的值为10b或11b），SCK引脚上最后一位的上升沿将SSR.TEND标志设置为1。设置S
CR.TE位在这之后立即变为0可能会导致接收端接收数据保持时间不足。

Figure 34.37 选择非FIFO的时钟同步模式下的串行传输示例流程

(2) FIFO selected

图34.38显示了在时钟同步模式下选择FIFO的串行传输示例。

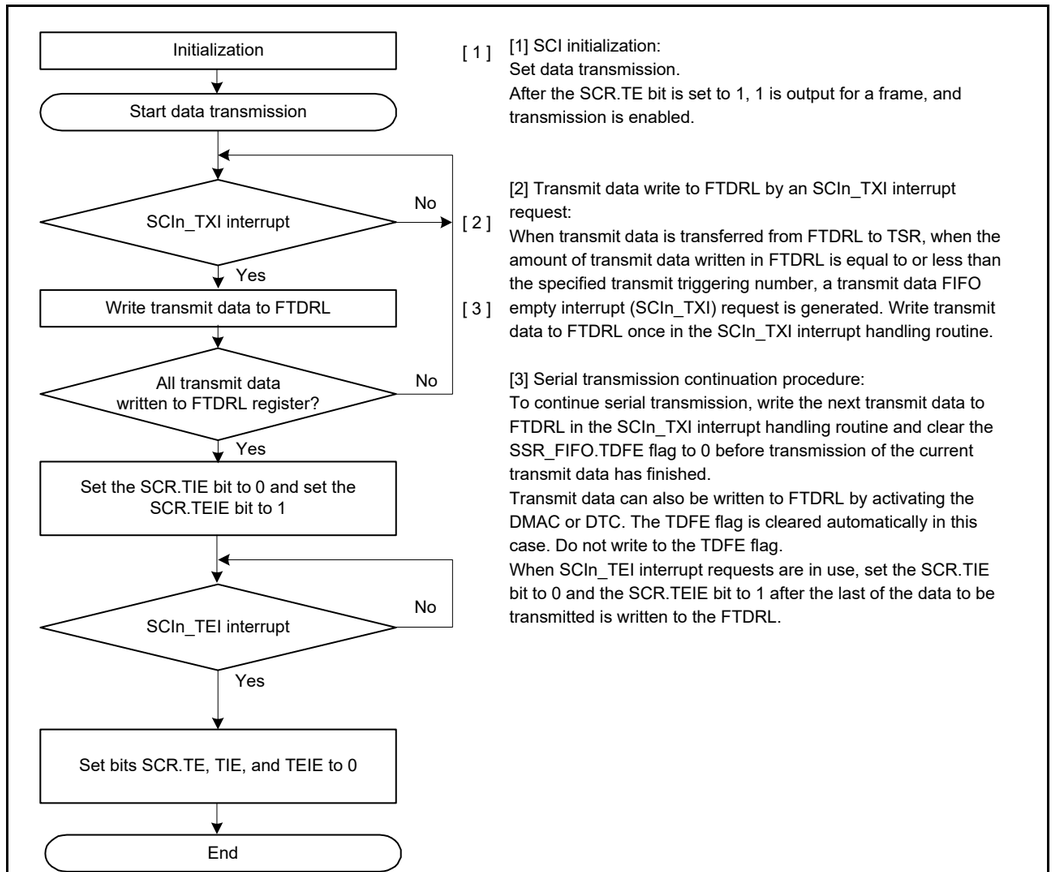
在串行数据传输中，SCI操作如下：

1. 当数据写入FTDRL*1时，SCI将数据从FTDRL*1寄存器传输到TSR寄存器
   SCIn_TXI中断处理程序。可写入FTDRL的数据量为16减去FDR.T[4:0]字节。发送开始时的SCIn_TXI中断请求在SCR.TE位被设置为1时产生，但仅在SCR.TIE位也被设置为1或当这两个位被一条指令同时设置为1时产生。
2. 将数据从FTDRL传输到TSR后，SCI开始传输。当写入FTDRL的发送数据量等于或小于指定的发送触发数时，SSR_FIFO.TDFE设置为1。当SCR.TIE位设置为1时，产生SCIn_TXI中断请求。在当前发送数据的发送完成之前，通过在SCIn_TXI中断处理例程中将下一个发送数据写入FTDRL来启用连续发送。当使用SCIn_TEI中断请求时，在将要传输的最后一个数据从处理例程写入FTDRL后，将SCR.TIE位设置为0，并将SCR.TEIE位设置为1。

SCIn_TXI requests.

3. 8-bit data is sent from the TXDn pin in synchronization with the output clock when the clock output mode is specified and in synchronization with the input clock when the use of an external clock is specified. Output of the clock signal is suspended until the input CTS signal is low when the SPMR.CTSE bit is 1.
4. The SCI checks whether non-transmitted data remains in FTDRL on output of the stop bit.
5. When FTDRL is updated, the next transmit data is transferred from FTDRL to TSR and serial transmission of the next frame starts.
6. If FTDRL is not updated, the SSR_FIFO.TEND flag is set to 1. The TXDn pin retains the output state of the last bit. If the SCR.TEIE bit is 1, an SCIn_TEI interrupt request is generated and the SCKn pin is held high.

Note 1. In clock synchronous mode, FTDRH is not used.



Note: When the external clock is in use (the value of the SCR.CKE[1:0] bits is 10b or 11b), the rising edge on the SCK pin for the last bit sets the SSR_FIFO.TEND flag to 1. Setting the SCR.TE bit to 0 immediately after this might lead to insufficient received-data hold time on the receiver side.

Figure 34.38 Example flow of serial transmission in clock synchronous mode with FIFO selected

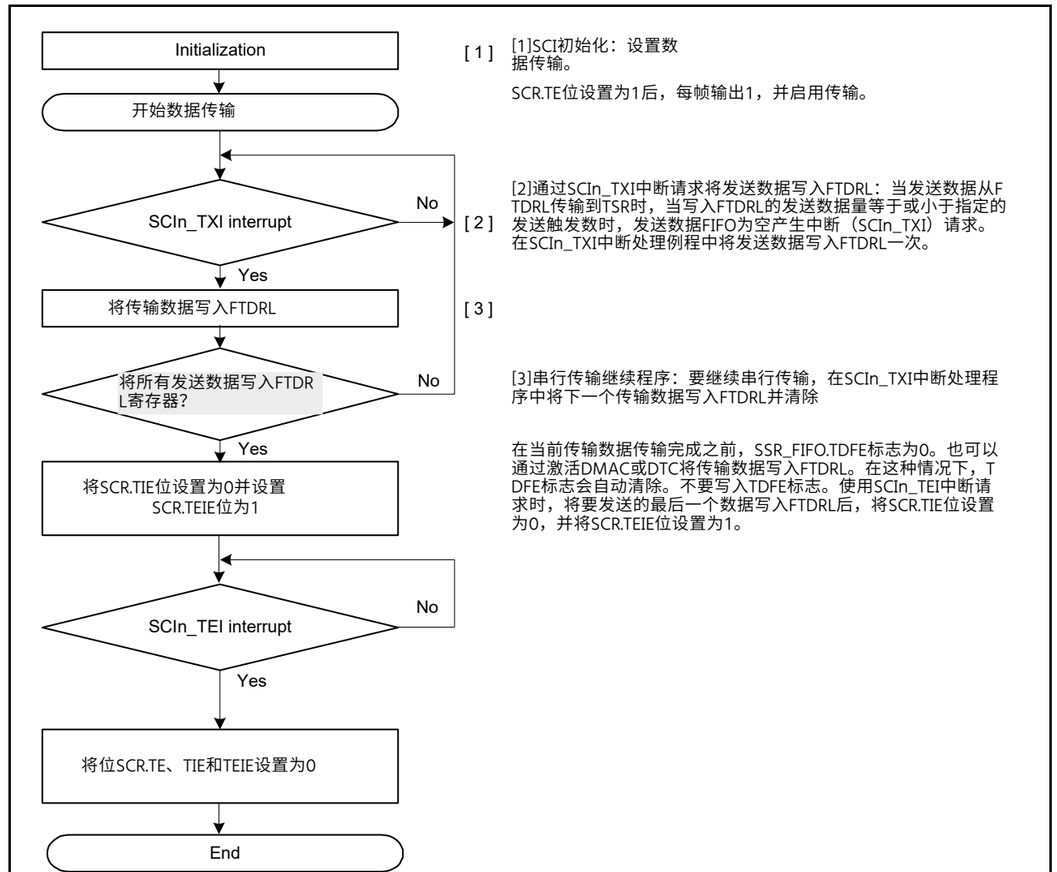
34.5.5 Serial Data Reception in Clock Synchronous Mode

(1) Non-FIFO selected

Figure 34.39 and Figure 34.40 show examples of SCI operation for serial reception in clock synchronous mode.

3. 指定时钟输出模式时，与输出时钟同步，指定使用外部时钟时，与输入时钟同步，从TXDn引脚发送8位数据。当SPMR.CTSE位为1时，时钟信号的输出被暂停，直到输入CTS信号为低电平。
4. SCI在停止位输出时检查未传输的数据是否保留在FTDRL中。
5. 当FTDRL被更新时，下一个传输数据从FTDRL传输到TSR并开始下一帧的串行传输。
6. 如果FTDRL未更新，则SSR_FIFO.TEND标志设置为1。TXDn引脚保持最后一位的输出状态。如果SCR.TEIE位为1，则产生SCIn_TEI中断请求并且SCKn引脚保持高电平。

注1.在时钟同步模式下，不使用FTDRH。



Note: 当使用外部时钟时（SCR.CKE[1:0]位的值为10b或11b），SCK引脚上最后一位的上升沿将SSR_FIFO.TEND标志设置为1。设置SCR.TE位在这之后立即变为0可能会导致接收端接收数据保持时间不足。

Figure 34.38 选择FIFO的时钟同步模式下的串行传输示例流程

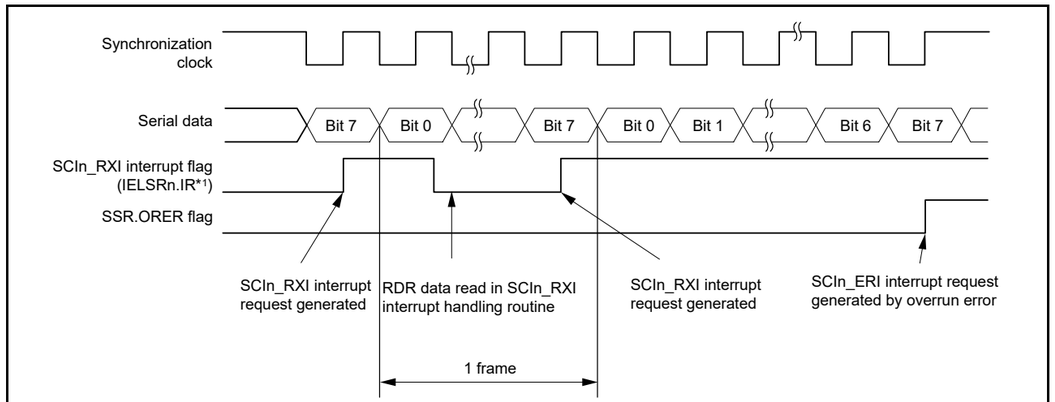
34.5.5 时钟同步模式下的串行数据接收

(1) Non-FIFO selected

图34.39和图34.40显示了时钟同步模式下串行接收的SCI操作示例。

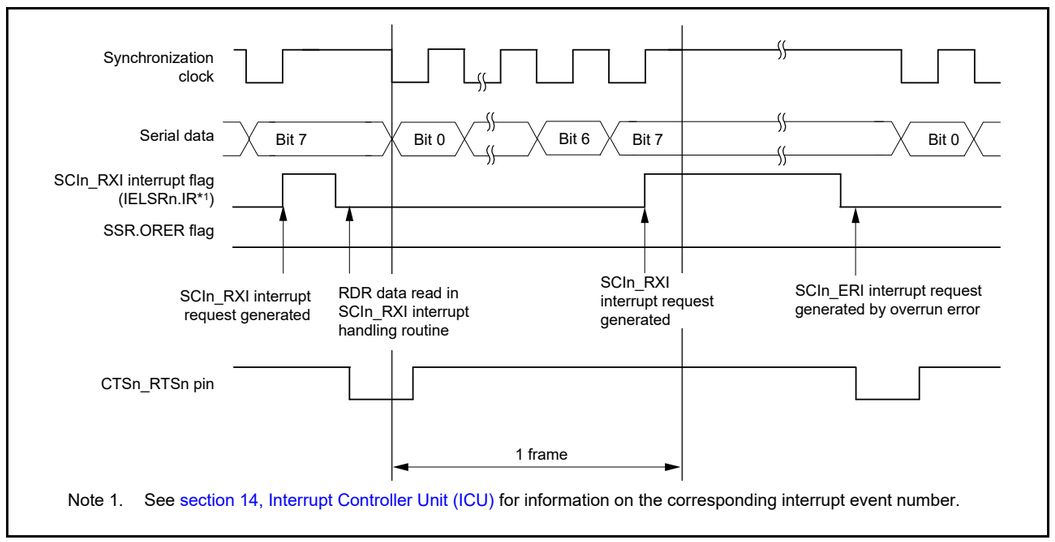
In serial data reception, the SCI operates as follows:

1. When the value of the SCR.RE bit becomes 1, the CTSn_RTSn pin goes low.
2. The SCI performs internal initialization and starts receiving data in synchronization with a synchronization clock input or output, and stores the receive data in the RSR register.
3. If an overrun error occurs, the SSR.ORER bit is set to 1. If the SCR.RIE bit is 1, an SCIn_ERI interrupt request is generated. Receive data is not transferred to the RDR register.
4. When reception completes successfully, receive data is transferred to the RDR register. If the SCR.RIE bit is 1, an SCIn_RXI interrupt request is generated. Continuous reception is enabled by reading the received data transferred to the RDR register in the SCIn_RXI interrupt handling routine before reception of the next receive data completes. Reading the received data that is transferred to RDR causes the CTSn_RTSn pin to output low.



Note 1. See section 14, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 34.39 Example operation for serial reception in clock synchronous mode (1) when the RTS function is not used



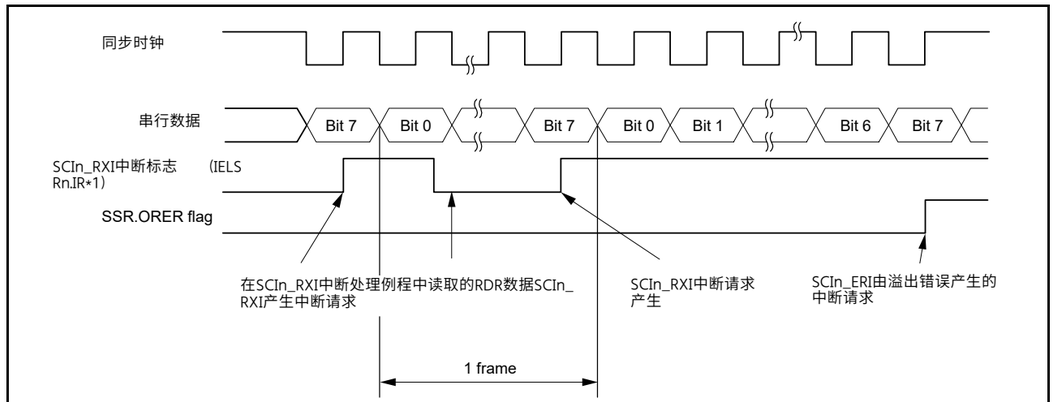
Note 1. See section 14, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 34.40 Example operation for serial reception in clock synchronous mode (2) when RTS function is used

Data transfer cannot resume while the receive error flag is 1. Therefore, clear the ORER, FER, and PER bits in the SSR

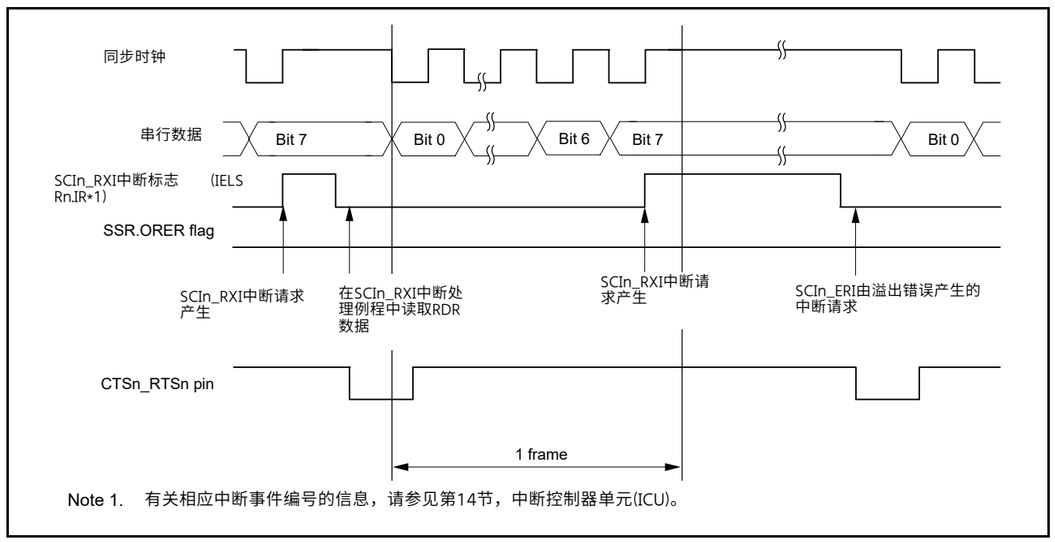
在串行数据接收中，SCI操作如下：

1. 当SCR.RE位的值变为1时，CTSn_RTSn引脚变为低电平。
2. SCI执行内部初始化并与同步时钟输入或输出同步开始接收数据，并将接收数据存储在RSR寄存器中。
3. 如果发生溢出错误，则SSR.ORER位设置为1。如果SCR.RIE位为1，则产生SCIn_ERI中断请求。接收数据不传送到RDR寄存器。
4. 当接收成功完成时，接收数据被传送到RDR寄存器。如果SCR.RIE位为1，则产生SCIn_RXI中断请求。在接收下一个接收数据完成之前，通过在SCIn_RXI中断处理例程中读取传输到RDR寄存器的接收数据来启用连续接收。读取传输到RDR的接收数据会导致CTSn_RTSn引脚输出低电平。



Note 1. 有关相应中断事件编号的信息，请参见第14节，中断控制器单元(ICU)。

Figure 34.39 不使用RTS功能时时钟同步模式下串行接收的示例操作(1)



Note 1. 有关相应中断事件编号的信息，请参见第14节，中断控制器单元(ICU)。

Figure 34.40 使用RTS功能时时钟同步模式下串行接收的示例操作(2)

当接收错误标志为1时，数据传输无法恢复。因此，清除SSR中的ORER、FER和PER位

register to 0 before resuming data reception. Additionally, always read the RDR register during overrun error processing. When a data reception is forced to terminate by a 0 write to the SCR.RE bit during operation, read the RDR register because received data that is not yet read might be left in the RDR register.

Figure 34.41 shows an example flow of serial data reception.

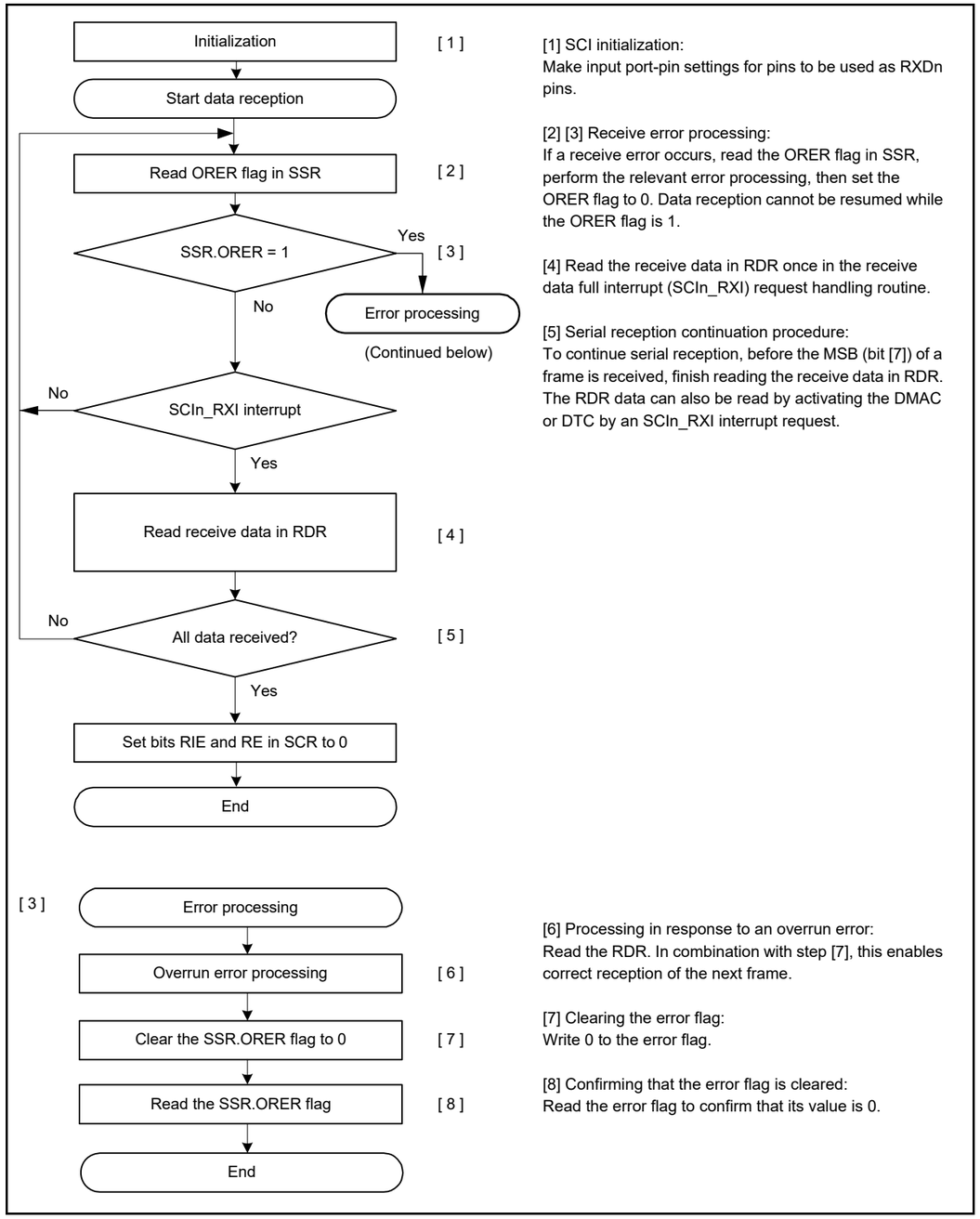


Figure 34.41 Example flow of serial reception in clock synchronous mode with non-FIFO selected

在恢复数据接收之前注册为0。此外，在溢出错误处理期间始终读取RDR寄存器。如果在操作期间通过向SCR.RE位写入0来强制终止数据接收，请读取RDR寄存器，因为尚未读取的已接收数据可能留在RDR寄存器中。

图34.41显示了串行数据接收的示例流程。

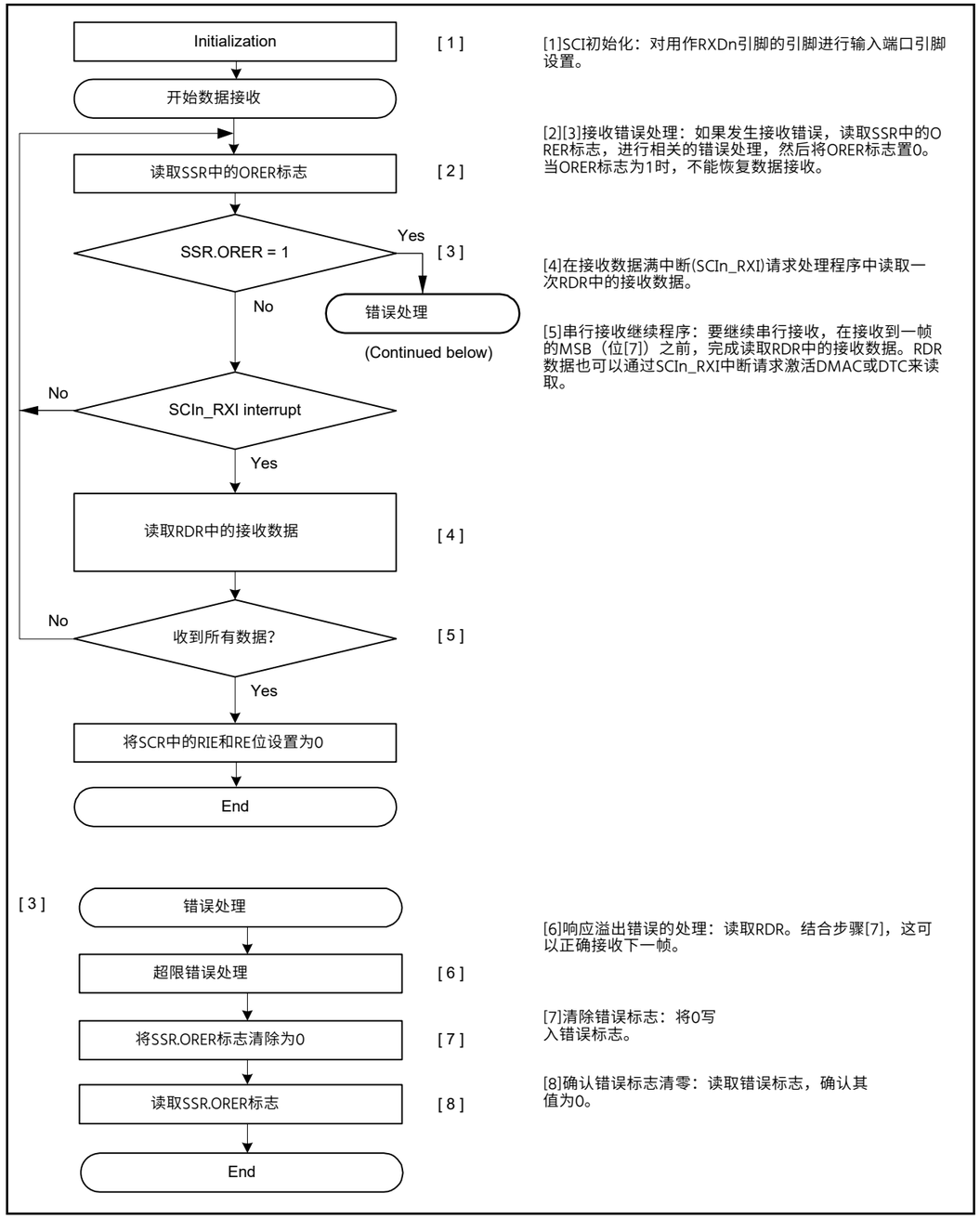


Figure 34.41 选择非FIFO的时钟同步模式下的串行接收示例流程

(2) FIFO selected

Figure 34.42 shows an example of serial reception in clock synchronous mode with FIFO selected.

In serial data reception, the SCI operates as follows:

1. When the value of the SCR.RE bit becomes 1, the CTSn_RTSn pin goes low.
2. The SCI performs internal initialization and starts receiving data in synchronization with a synchronization clock input or output, and stores the receive data in the RSR register.
3. If an overrun error occurs, the SSR_FIFO.ORER bit is set to 1. If the SCR.RIE bit is 1, an SCIn_ERI interrupt request is generated. Received data is not transferred to the FRDRL*1 register.
4. When data reception completes successfully, the receive data is transferred to the FRDRL*1 register. The RDF bit is set to 1 when the amount of the receive data stored in FRDRL is equal to or greater than the specified receive triggering number. If the SCR.RIE bit is 1, an SCIn_RXI interrupt request is generated. Continuous data reception is enabled by reading the receive data transferred to FRDRL*2 in the SCIn_RXI interrupt handling routine before an overrun error occurs. If the amount of received data that is transferred to FRDRL is less than the RTS trigger number, the CTSn_RTSn pin goes low.

Note 1. In clock synchronous mode, FRDRH is not used.
Note 2. Read data in order from FRDRH to FRDRL when RDF and ORER are read with receive data.

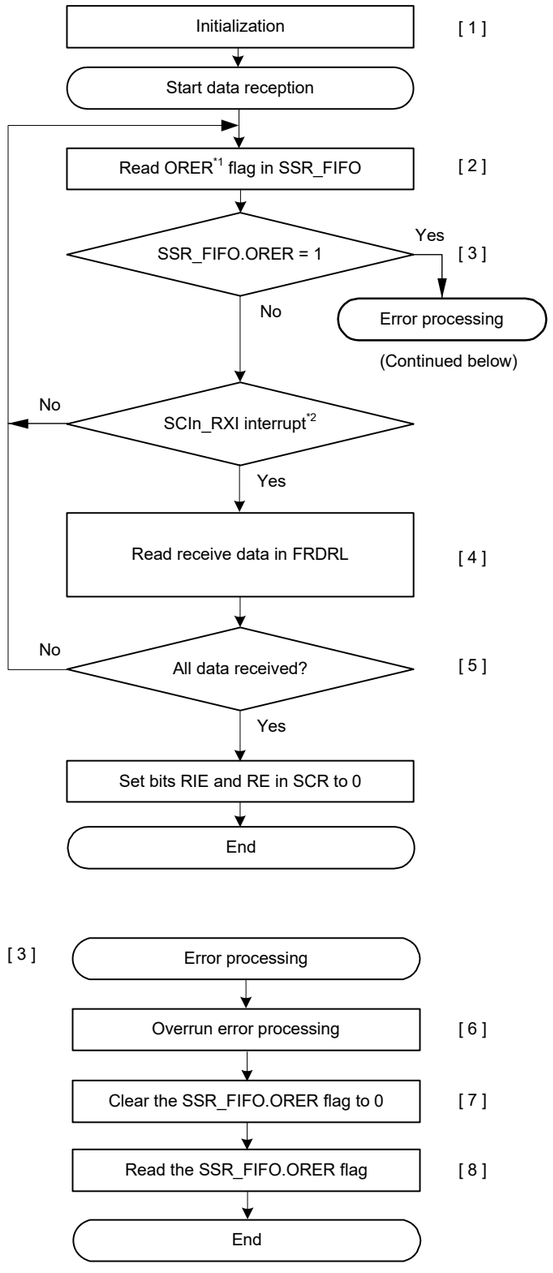
(2) FIFO selected

图34.42显示了选择FIFO的时钟同步模式下的串行接收示例。

在串行数据接收中，SCI操作如下：

1. 当SCR.RE位的值变为1时，CTSn_RTSn引脚变为低电平。
2. SCI执行内部初始化并与同步时钟输入或输出同步开始接收数据，并将接收数据存储在RSR寄存器中。
3. 如果发生溢出错误，则SSR_FIFO.ORER位设置为1。如果SCR.RIE位为1，则产生SCIn_ERI中断请求。接收到的数据不传送到FRDRL*1寄存器。
4. 当数据接收成功完成时，接收数据被传送到FRDRL*1寄存器。当存储在FRDRL中的接收数据量等于或大于指定的接收触发数时，RDF位设置为1。如果SCR.RIE位为1，则产生SCIn_RXI中断请求。在发生溢出错误之前，通过在SCIn_RXI中断处理例程中读取传输到FRDRL*2的接收数据来启用连续数据接收。如果传输到FRDRL的接收数据量小于RTS触发数，则CTSn_RTSn引脚变为低电平。

注1.在时钟同步模式下，不使用FRDRH。
注2.RDF和ORER与接收数据一起读取时，按FRDRH到FRDRL的顺序读取数据。



[1] SCI initialization:
Make input port-pin settings for pins to be used as RXDn pins.

[2] [3] Receive error processing:
If a receive error occurs, read the ORER flag in SSR_FIFO, perform the relevant error processing, then set the SSR_FIFO.ORER flag to 0. Data reception cannot be resumed while the ORER flag is 1.

[4] The receive data stored in FRDRL register is read until the number of stored data is less than the FCR.RTRG value. Software can check readable data in FDR.R[4:0].

[5] Serial reception continuation procedure:
To continue serial reception, before overrun error occurs, finish reading the receive data in FRDRL and clear the SSR_FIFO.RDF flag to 0. The FRDRL data can also be read by activating the DMAC or DTC by an SCIn_RXI interrupt request. The RDF flag is cleared automatically in this case. Do not write to the RDF flag.

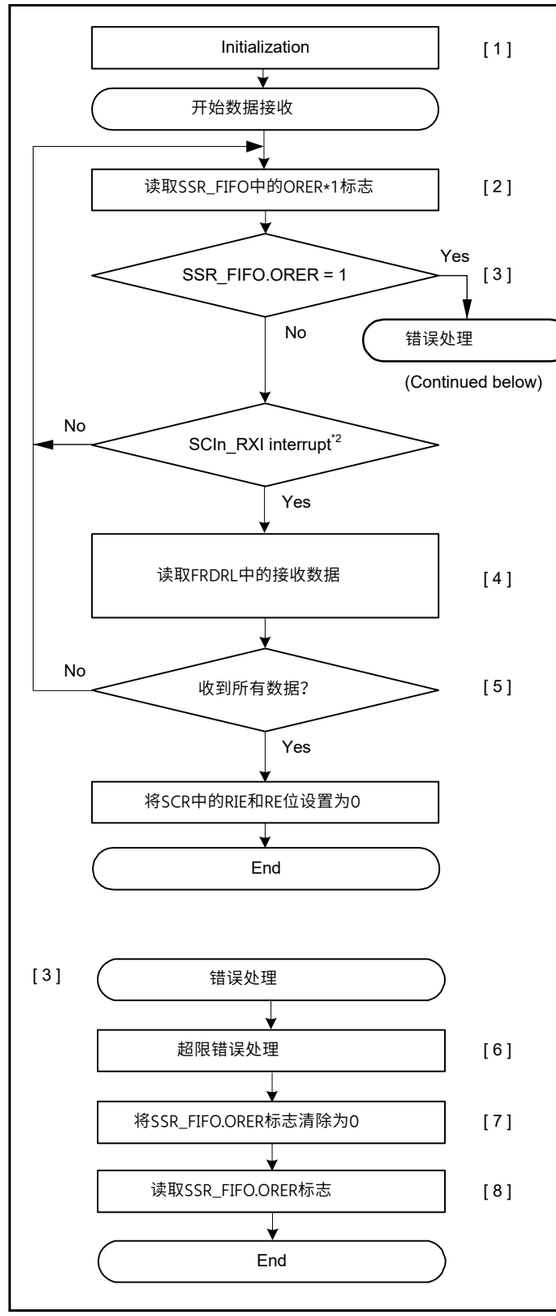
[6] Processing in response to an overrun error:
Read the FRDRL. In combination with step [7], this enables correct reception of the next frame.

[7] Clearing the error flag:
Write 0 to the error flag.

[8] Confirming that the error flag is cleared:
Read the error flag to confirm that its value is 0.

Note 1. It can also be read from FRDRH.ORER. However, to clear the ORER flag, write 0 to the associated bit in the SSR_FIFO register.
Note 2. It should be all receive data and is an integer times the FIFO triggering number.

Figure 34.42 Example flow of serial reception in clock synchronous mode with FIFO selected



[1]SCI初始化：对用作RXDn引脚的引脚进行输入端口引脚设置。

[2][3]接收错误处理：如果发生接收错误，读取ORER标志

SSR_FIFO，进行相关的错误处理，然后将SSR_FIFO.ORER标志置0。当ORER标志为1时，不能恢复数据接收。

[4]读取FRDRL寄存器中存储的接收数据，直到存储的数据数量小于FCR.RTRG值。软件可以检查可读数据

FDR.R[4:0].

[5]串行接收继续程序：要继续串行接收，在发生溢出错误之前，完成读取FRRDL中的接收数据并将SSR_FIFO.RDF标志清0。FRRDL数据也可以通过激活DMAC或DTC来读取。SCIn_RXI中断请求。在这种情况下，RDF标志会自动清除。不要写入RDF标志。

[6]响应溢出错误的处理：读取FRDRL。结合步骤[7]，这可以正确接收下一帧。

[7]清除错误标志：将0写入错误标志。

[8]确认错误标志清零：读取错误标志，确认其值为0。

Note 1. 它也可以从FRDRH.ORER中读取。但是，要清除ORER标志，请将0写入SSR_FIFO寄存器中的相关位。
Note 2. 应该都是接收数据，是FIFO触发数的整数倍。

Figure 34.42 选择FIFO的时钟同步模式下的串行接收示例流程

34.5.6 Simultaneous Serial Data Transmission and Reception in Clock Synchronous Mode

(1) Non-FIFO selected

Figure 34.43 shows an example flow of simultaneous serial transmission and reception operations in clock synchronous mode. After initializing the SCI, use the following procedure for simultaneous serial data transmission and reception operations.

To switch from transmit mode to simultaneous transmit and receive mode:

1. Check that the SCI completes the data transmission by verifying that the SSR.TEND flag is set to 1.
2. Initialize the SCR register, and then set the TIE, RIE, TE, and RE bits in the SCR register to 1 simultaneously by a single instruction.

To switch from receive mode to simultaneous transmit and receive mode:

1. Check that the SCI completes the data reception.
2. Set the RIE and RE bits to 0, and then check that the receive error flag ORER in the SSR register is 0.
3. Set the TIE, RIE, TE, and RE bits in the SCR register to 1 simultaneously by a single instruction.

34.5.6 时钟同步的同时串行数据发送和接收 Mode

(1) Non-FIFO selected

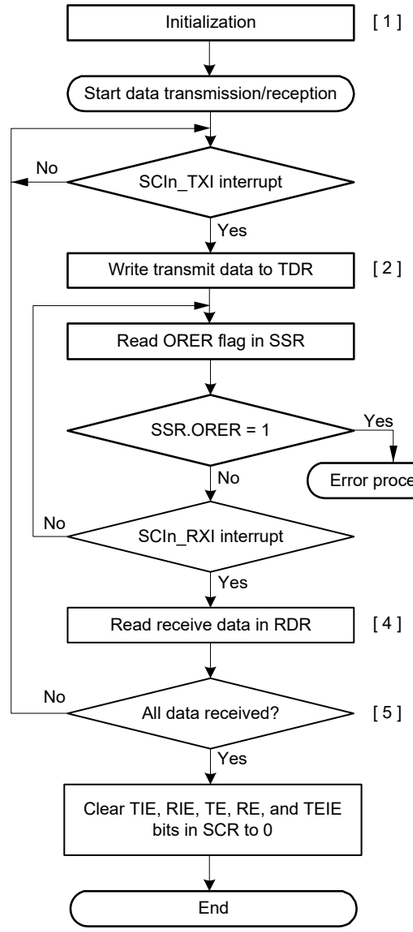
图34.43显示了时钟同步模式下同时串行发送和接收操作的示例流程。初始化SCI后，使用以下程序同时进行串行数据发送和接收操作。

从发送模式切换到同时发送和接收模式：

1. 通过验证SSR.TEND标志是否设置为1来检查SCI是否完成了数据传输。
2. 初始化SCR寄存器，然后通过一条指令同时将SCR寄存器中的TIE、RIE、TE和RE位设置为1。

从接收模式切换到同时发送和接收模式：

1. 检查SCI是否完成数据接收。
2. 将RIE和RE位设置为0，然后检查SSR寄存器中的接收错误标志ORER是否为0。
3. 通过一条指令同时将SCR寄存器中的TIE、RIE、TE和RE位设置为1。



[1] SCI initialization:
The TXDn pin can act as the output pin for transmitted data and the RXDn pin can act as the input pin for received data at the same time.

[2] Transmit data write:
Write transmit data to TDR once in the SCIn_TXI interrupt request handling routine.

[3] Receive error processing:
If a receive error occurs, read the ORER flag in SSR, perform the relevant error processing, then set the ORER flag to 0. Data reception cannot be resumed while the ORER flag is 1.

[4] Reading receive data:
Read the receive data in RDR once in the SCIn_RXI interrupt request handling routine.

[5] Serial transmission or reception continuation procedure:
To continue serial transmission and reception, before the MSB (bit [7]) of the current frame is received, finish reading the receive data in RDR by the SCIn_RXI interrupt. Also, before the MSB (bit [7]) of the current frame is transmitted, write data to TDR by the SCIn_TXI interrupt.
Transmit data can also be written to TDR by activating the DMAC or DTC by a transmit data empty interrupt (SCIn_TXI) request. Similarly, the RDR data can also be read by activating the DMAC or DTC by a receive data full interrupt (SCIn_RXI) request.

Note: When switching from transmit or receive operation to simultaneous transmit and receive operations, first set the TIE, RIE, TE, RE, and TEIE bits in SCR to 0, then set TIE, RIE, TE, and RE bits to 1 simultaneously.

Figure 34.43 Example flow of simultaneous serial transmission and reception in clock synchronous mode with non-FIFO selected

(2) FIFO selected

Figure 34.44 shows an example flow of simultaneous serial transmit and receive operations in clock synchronous mode with FIFO selected.

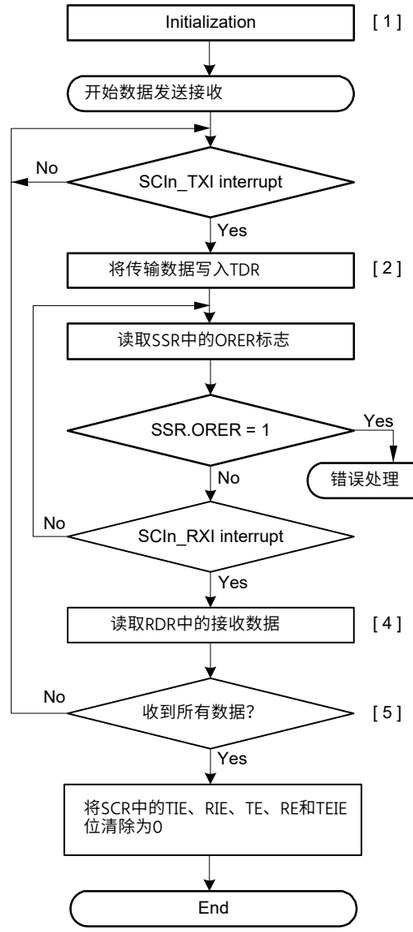
After initializing the SCI, use the following procedure for simultaneous serial data transmit and receive operations.

To switch from transmit mode to simultaneous transmit and receive mode:

1. Check that the SCI completes the transmission by verifying that the SSR_FIFO.TEND flag is set to 1.
2. Initialize the SCR register, then set the TIE, RIE, TE, and RE bits in the SCR register to 1 simultaneously by a single instruction.

To switch from receive mode to simultaneous transmit and receive mode:

1. Check that the SCI completes the reception.



[1]SCI初始化：TXDn管脚可以作为发送数据的输出管脚，RXDn管脚同时可以作为接收数据的输入管脚。

[2]发送数据写入：在SCIn_TXI中断请求处理程序中将发送数据写入TDR一次。

[3]接收错误处理：如果发生接收错误，读取SSR中的ORER标志，进行相关的错误处理，然后将ORER标志设置为0。当ORER标志为1时，不能恢复数据接收。

[4]读取接收数据：在SCIn_RXI中断请求处理程序中读取一次RDR中的接收数据。

[5]串行发送或接收继续程序：要继续串行发送和接收，在

接收到当前帧的MSB（bit[7]），通过SCIn_RXI中断完成读取RDR中的接收数据。此外，在发送当前帧的MSB（位[7]）之前，通过SCIn_TXI中断将数据写入TDR。发送数据也可以通过发送数据空中断(SCIn_TXI)请求激活DMAC或DTC写入TDR。同样，也可以通过接收数据完全中断(SCIn_RXI)请求激活DMAC或DTC来读取RDR数据。

Note: 从发送或接收操作切换到同时发送和接收操作时，首先设置TIE，SCR中的RIE、TE、RE和TEIE位为0，然后将TIE、RIE、TE和RE位同时设置为1。

Figure 34.43 选择非FIFO的时钟同步模式下同时串行发送和接收的示例流程

(2) FIFO selected

图34.44显示了在时钟同步模式下同时串行发送和接收操作的示例流程，并选择了FIFO。

初始化SCI后，使用以下程序同时进行串行数据发送和接收操作。

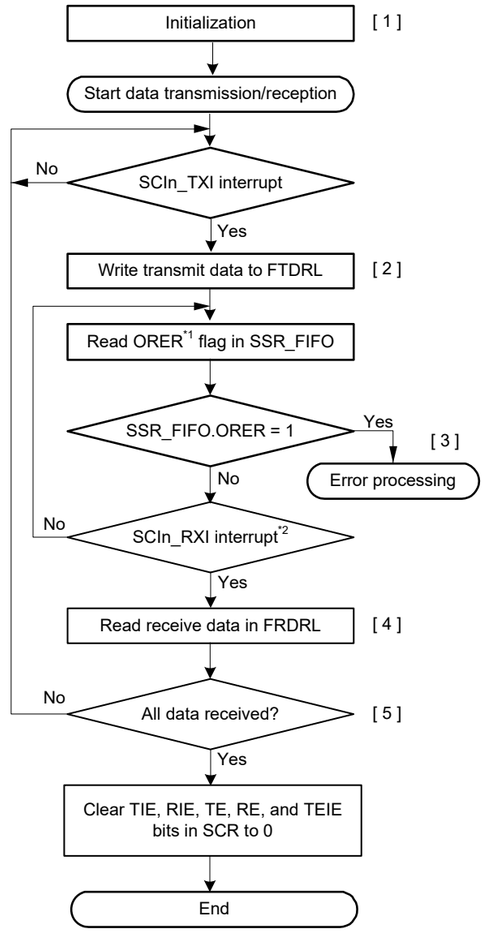
从发送模式切换到同时发送和接收模式：

1. 通过验证SSR_FIFO.TEND标志是否设置为1来检查SCI是否完成了传输。
2. 初始化SCR寄存器，然后通过一条指令同时将SCR寄存器中的TIE、RIE、TE和RE位设置为1。

从接收模式切换到同时发送和接收模式：

1. 检查SCI是否完成接收。

2. Set the RIE and RE bits to 0, then check that the receive error flag ORER in SSR_FIFO is 0.
3. Set the TIE, RIE, TE, and RE bits in SCR to 1 simultaneously by a single instruction.



[1] SCI initialization:
The TXDn pin can act as the output pin for transmitted data and the RXDn pin can act as the input pin for received data at the same time.

[2] Transmit data write:
Write transmit data to FTDRL in the SCIn_TXI Interrupt request handling routine. The amount of transmit data it is possible to write in is 16 minus the amount of stored transmit FIFO data.

[3] Receive error processing:
If a receive error occurs, read the ORER flag in SSR_FIFO, perform the relevant error processing, then set the ORER flag to 0. Data reception cannot be resumed while the ORER flag is 1.

[4] Reading receive data:
The receive data stored in FRDRL register is read until the number of stored data is less than the FCR.RTRG value. Software can check readable data in FDR.R[4:0].

[5] Serial transmission or reception continuation procedure:
To continue serial reception, before overrun error occurs, finish reading the receive data in FRDRL and clear the SSR_FIFO.RDF flag to 0. To continue serial transmission, before transmission of the current transmit data has finished, write the next transmit data to FTDRL in the SCIn_TXI interrupt handling routine and clear the SSR_FIFO.TDFE flag to 0.
Transmit data can also be written to FTDRL by activating the DMAC or DTC by a transmit FIFO data empty interrupt (SCIn_TXI) request. Similarly, the FRDRL data can also be read by activating the DMAC or DTC by a receive FIFO data full interrupt (SCIn_RXI) request. The RDF and TDFE flags are cleared automatically in this case. Do not write to the RDF and TDFE flags.

Note 1. ORER can also read from FRDRH.ORER. To clear the ORER flag, write 0 to SSR_FIFO.ORER.
Note 2. The total receive data amount must be an integral multiple of the FIFO triggering number.

Figure 34.44 Example flow of simultaneous serial transmission and reception in clock synchronous mode with FIFO selected

34.6 Operation in Smart Card Interface Mode

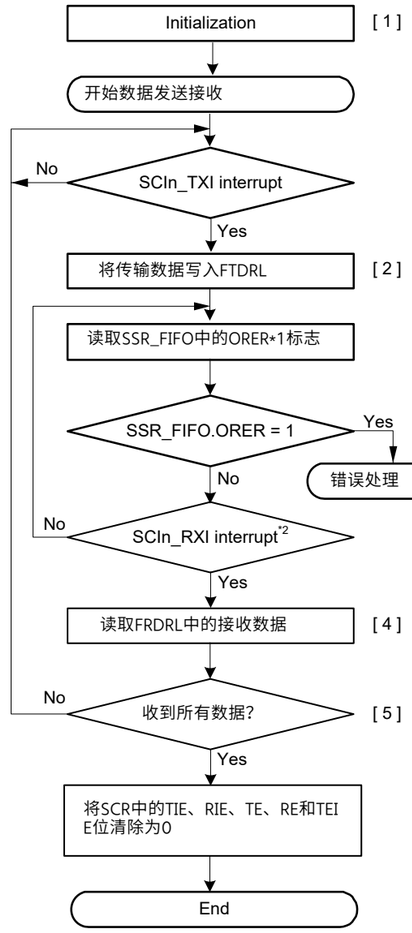
The SCI supports smart card (IC card) interfaces conforming to ISO/IEC 7816-3 (standard for Identification Cards), as an extended function of the SCI.

Smart card interface mode can be selected using the appropriate register.

34.6.1 Example Connection

Figure 34.45 shows an example connection between a smart card (IC card) and the MCU. As shown in Figure 34.45, because the MCU communicates with an IC card using a single transmission line, interconnect the TXDn and RXDn pins and pull up the data transmission line to VCC using a resistor.

2. 将RIE和RE位设置为0，然后检查SSR_FIFO中的接收错误标志ORER是否为0。
3. 通过一条指令同时将SCR中的TIE、RIE、TE和RE位设置为1。



[1]SCI初始化：TXDn管脚可以作为发送数据的输出管脚，RXDn管脚同时可以作为接收数据的输入管脚。

[2]发送数据写入：在SCIn_TXI中断请求处理程序中将发送数据写入FTDRL。可以写入的发送数据量是16减去存储的发送FIFO数据量。

[3]接收错误处理：如果发生接收错误，读取ORER标志

SSR_FIFO，进行相应的错误处理，然后将ORER标志置0。当ORER标志为1时，不能恢复数据接收。

[4]读取接收数据：读取存储在FRRDL寄存器中的接收数据，直到存储的数据个数小于FCR.RTRG值。软件可以检查FDR.R[4:0]中的可读数据。

[5]串行发送或接收继续程序：继续串行接收，在溢出错误发生之前，完成FRRDL中的接收数据读取并将SSR_FIFO.RDF标志清0。继续串行发送，在当前发送数据发送之前完成后，在SCIn_TXI中断处理程序中将下一个发送数据写入FTDRL并清除

SSR_FIFO.TDFE标志为0。
发送数据也可以通过发送FIFO数据空中断(SCIn_TXI)请求激活DMAC或DTC写入FTDRL。同样，也可以通过接收FIFO数据满中断(SCIn_RXI)请求激活DMAC或DTC来读取FRDRL数据。在这种情况下，RDF和TDFE标志会自动清除。不要写入RDF和TDFE标志。

Note 1. ORER也可以从FRDRH.ORER中读取。要清除ORER标志，请将0写入SSR_FIFO.ORER。
Note 2. 总接收数据量必须是FIFO触发数的整数倍。

Figure 34.44 时钟同步模式下同时串行发送和接收的示例流程 FIFO selected

34.6 智能卡接口模式下的操作

SCI支持符合ISOIEC7816-3（识别卡标准）的智能卡（IC卡）接口，作为SCI的扩展功能。

可以使用适当的寄存器选择智能卡接口模式。

34.6.1 示例连接

图34.45显示了智能卡（IC卡）和MCU之间的示例连接。如图34.45所示，由于MCU使用单条传输线与IC卡通信，因此将TXDn和RXDn引脚互连，并使用电阻将数据传输线上拉到VCC。

Setting the SCR_SMCI.TE and SCR_SMCI.RE bits to 1 with an IC card disconnected enables closed-loop transmission or reception, allowing self-diagnosis. To supply an IC card with the clock pulses generated by the SCI, input the SCKn pin output to the CLK pin of an IC card.

An output port of the MCU can be used to output a reset signal.

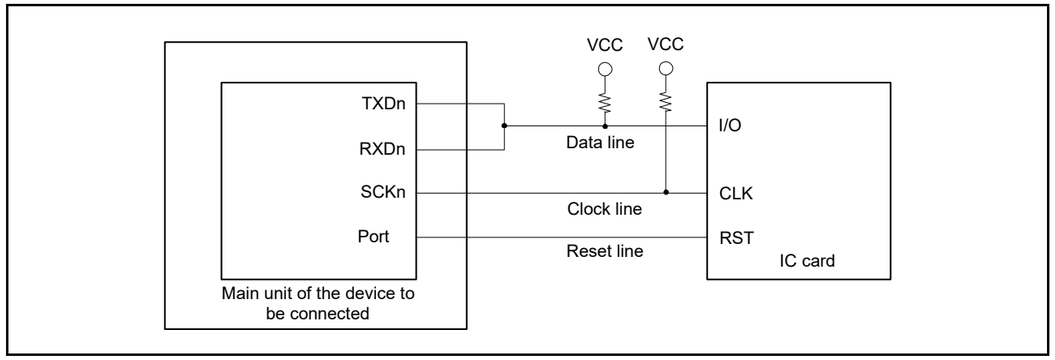


Figure 34.45 Example connection with a smart card (IC card)

34.6.2 Data Format (Except in Block Transfer Mode)

Figure 34.46 shows the data transfer formats in smart card interface mode:

- One frame consists of 8-bit data and a parity bit in asynchronous mode
- During transmission, at least 2 ETUs (elementary time unit — the time required for transferring 1 bit) is set as a guard time from the end of the parity bit until the start of the next frame
- If a parity error is detected during reception, a low error signal is output for 1 ETU after 10.5 ETUs elapse from the start bit
- If an error signal is sampled during transmission, the same data is automatically retransmitted after at least 2 ETUs.

在断开IC卡的情况下将SCR_SMCI.TE和SCR_SMCI.RE位设置为1可启用闭环发送或接收，从而实现自诊断。要将SCI产生的时钟脉冲提供给IC卡，请将SCKn引脚输出输入到IC卡的CLK引脚。

MCU的输出端口可用于输出复位信号。

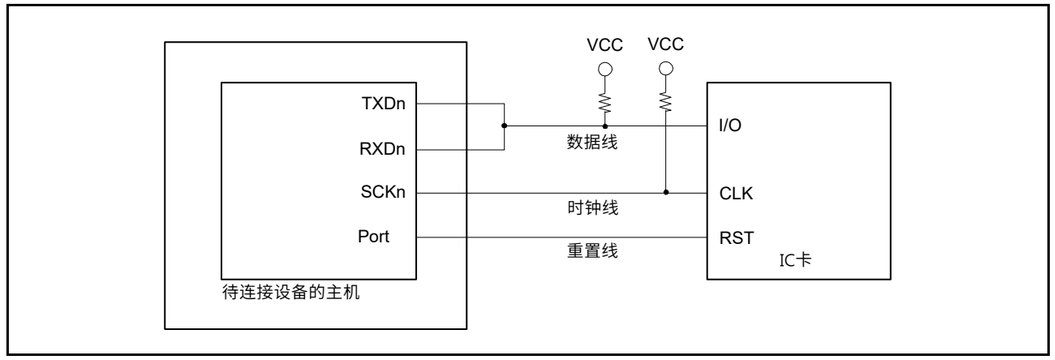


Figure 34.45 与智能卡（IC卡）的连接示例

34.6.2 数据格式（块传输模式除外）

图34.46显示了智能卡接口模式下的数据传输格式：

- 一帧由异步模式下的8位数据和一个奇偶校验位组成
- 在传输过程中，至少有2个ETU（基本时间单位——传输1位所需的时间）设置为从奇偶校验位结束到下一帧开始的保护时间
- 如果在接收期间检测到奇偶校验错误，则在从起始位经过10.5ETU后输出1ETU的低错误信号
- 如果在传输过程中对错误信号进行采样，则在至少2个ETU后会自动重新传输相同的数据。

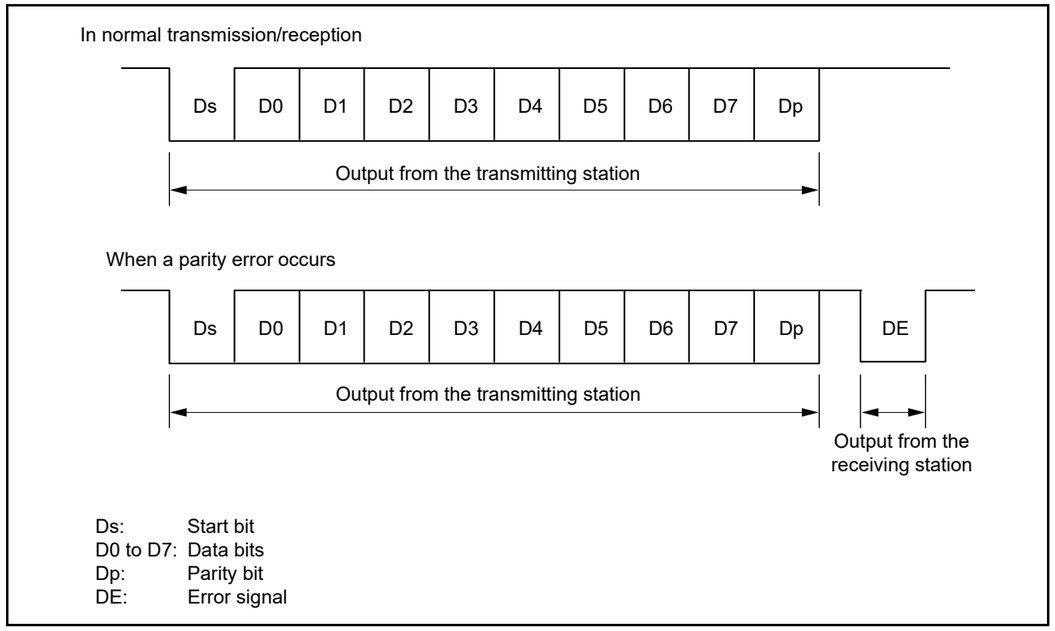


Figure 34.46 Data formats in smart card interface mode

For communications with IC cards of the direct convention type and inverse convention type, follow the procedures in this section.

(1) Direct Convention Type

For the direct convention type, logic levels 1 and 0 indicate the Z and A states, respectively, and data is transferred with LSB-first for the start character, as shown in Figure 34.47. Therefore, data in the start character in the figure is 3Bh.

When using the direct convention type, write 0 to both the SCMR.SDIR and SCMR.SINV bits. Write 0 to the SMR_SMCI.PM bit to use even parity, which is required by the smart card standard.

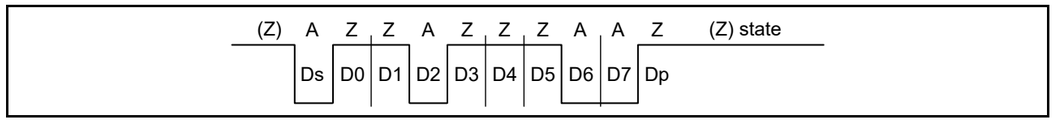


Figure 34.47 Direct convention with SDIR in SCMR = 0, SINV in SCMR = 0, and PM in SMR_SMCI = 0

(2) Inverse Convention Type

For the inverse convention type, logic levels 1 and 0 indicate the A and Z states, respectively, and data is transferred with MSB-first for the start character, as shown in Figure 34.48. Therefore, data in the start character in the figure is 3Fh.

When using the inverse convention type, write 1 to both the SCMR.SDIR and SCMR.SINV bits. The parity bit is logic level 0 to produce even parity, which is prescribed by the smart card standard, and corresponds to the Z state. Because the SINV bit of the MCU only inverts data bits D7 to D0, write 1 to the PM bit in SMR_SMCI to invert the parity bit for both transmission and reception.

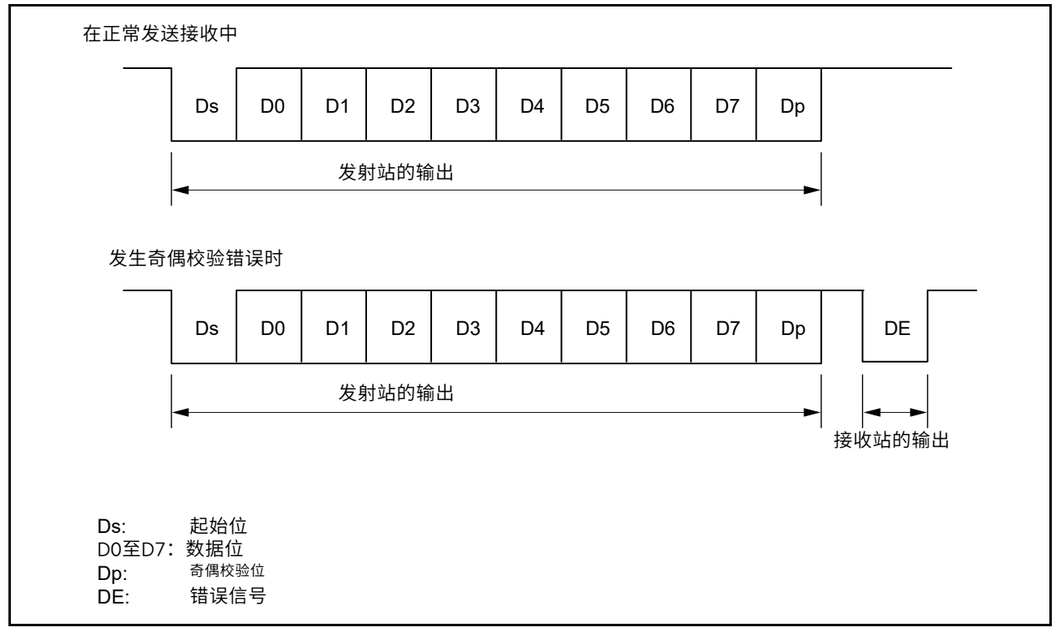


Figure 34.46 智能卡接口模式下的数据格式

与直接约定型和逆约定型IC卡进行通信时，请按照本节的步骤进行。

(1) 直接约定型

对于直接约定类型，逻辑电平1和0分别表示Z和A状态，数据通过LSB-first为起始字符，如图34.47所示。因此，图中起始字符中的数据为3Bh。

使用直接约定类型时，将0写入SCMR.SDIR和SCMR.SINV位。将0写入SMR_SMCI.PM位使用智能卡标准所要求的偶校验。

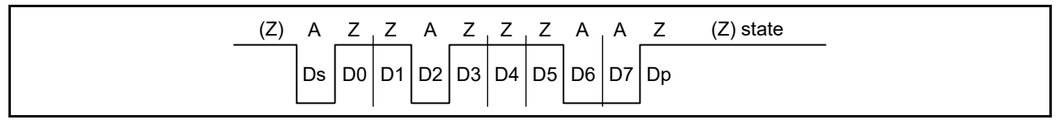


Figure 34.47 与SCMR=0中的SDIR、SCMR=0中的SINV和SMR_SMCI=0中的PM的直接约定

(2) 逆约定型

对于逆约定类型，逻辑电平1和0分别表示A和Z状态，数据通过MSB-first为起始字符，如图34.48所示。因此，图中起始字符中的数据为3Fh。

使用逆约定类型时，将1写入SCMR.SDIR和SCMR.SINV位。奇偶校验位为逻辑电平0，产生偶校验，这是智能卡标准规定的，对应于Z状态。由于MCU的SINV位仅将数据位D7反转为D0，因此向SMR_SMCI中的PM位写入1以反转发送和接收的奇偶校验位。

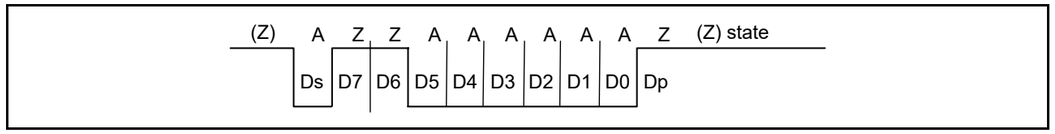


Figure 34.48 Inverse convention with SDIR in SCMR = 1, SINV in SCMR = 1, and PM in SMR_SMCI = 1

34.6.3 Block Transfer Mode

Block transfer mode differs from non-block transfer mode of smart card interface mode as follows:

- Even if a parity error is detected during reception, no error signal is output. Because the PER bit in SSR_SMCI is set by error detection, clear the PER bit before receiving the parity bit of the next frame.
- During transmission, at least 1 ETU is set as a guard time from the end of the parity bit until the start of the next frame
- Because the same data is not retransmitted, the TEND flag in SSR_SMCI is set to 11.5 ETUs after transmission starts
- In block transfer mode, the ERS flag in SSR_SMCI indicates the error signal status as in non-block transfer mode of smart card interface mode, but the flag is read as 0 because no error signal is transferred.

34.6.4 Receive Data Sampling Timing and Reception Margin

Only the clock generated by the on-chip baud rate generator can be used as a transfer clock in smart card interface mode.

In this mode, the SCI can operate on a base clock with a frequency of 32, 64, 372, 256, 93, 128, 186, or 512 times the bit rate set up in the SCMR.BCP2 and the SMR_SMCI.BCP[1:0] bits.

For data reception, the falling edge of the start bit is sampled with the base clock to perform synchronization.

Receive data is sampled on the 16th, 32nd, 186th, 128th, 46th, 64th, 93rd, and 256th rising edges of the base clock so that it can be latched at the middle of each bit as shown in Figure 34.49. The reception margin is determined by the following formula:

$$M = \left| (0.5 - \frac{1}{2N}) - (L - 0.5)\,F - \frac{\left| D - 0.5 \right|}{N}(1 + F) \right| \times 100\ [\%]$$

M: Reception margin (%)

N: Ratio of bit rate to clock (N = 32, 64, 372, 256)

D: Duty cycle of clock (D = 0 to 1.0)

L: Frame length (L = 10)

F: Absolute value of clock frequency deviation

Assuming values of F = 0, D = 0.5, and N = 372 in the specified formula, the reception margin is determined using the following formula:

$M = \{0.5 - 1/(2 \times 372)\} \times 100\ [\%] = 49.866\%$

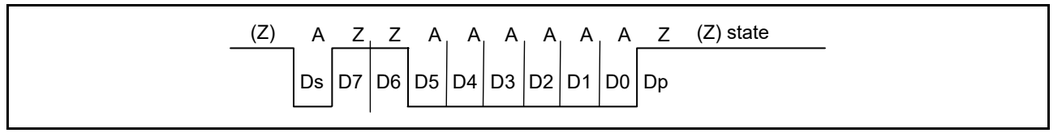


Figure 34.48 SCMR=1中的SDIR、SCMR=1中的SINV和SMR_SMCI=1中的PM的逆约定

34.6.3 块传输模式

块传输模式与智能卡接口模式的非块传输模式的区别如下：

- 即使在接收过程中检测到奇偶校验错误，也不会输出错误信号。因为SSR_SMCI中的PER位是通过错误检测设置的，所以在接收下一帧的奇偶校验位之前清除PER位。
- 在传输过程中，从奇偶校验位结束到下一帧开始至少设置1个ETU作为保护时间
- 因为没有重传相同的数据，所以在传输开始后SSR_SMCI中的TEND标志设置为11.5ETU
- 在块传输模式下，SSR_SMCI中的ERS 标志指示错误信号状态，与智能卡接口模式的非块传输模式一样，但该标志被读取为0，因为没有传输错误信号。

34.6.4 接收数据采样时序和接收裕量

只有片内波特率发生器产生的时钟可以用作智能卡接口模式下的传输时钟。

在这种模式下，SCI可以在频率为SCMR.BCP2和SMR_SMCI.BCP[1:0]位。

对于数据接收，起始位的下降沿与基本时钟一起采样以执行同步。

接收数据在基本时钟的第16、32、186、128、46、64、93和256个上升沿进行采样，以便在每个位的中间锁存，如图34.49所示。接收余量由以下公式确定：

$$M = \left| (0.5 - \frac{1}{2N}) - (L - 0.5)\,F - \frac{\left| D - 0.5 \right|}{N}(1 + F) \right| \times 100\ [\%]$$

M：接收余量（%）

N：比特率与时钟的比率（N=32、64、372、256）

D：时钟的占空比（D=0到1.0）

L：帧长（L=10）

F：时钟频率偏差的绝对值

假设指定公式中的F=0、D=0.5和N=372的值，则使用以下公式确定接收余量：

$M = \{0.5 - 1/(2 \times 372)\} \times 100\ [\%] = 49.866\%$

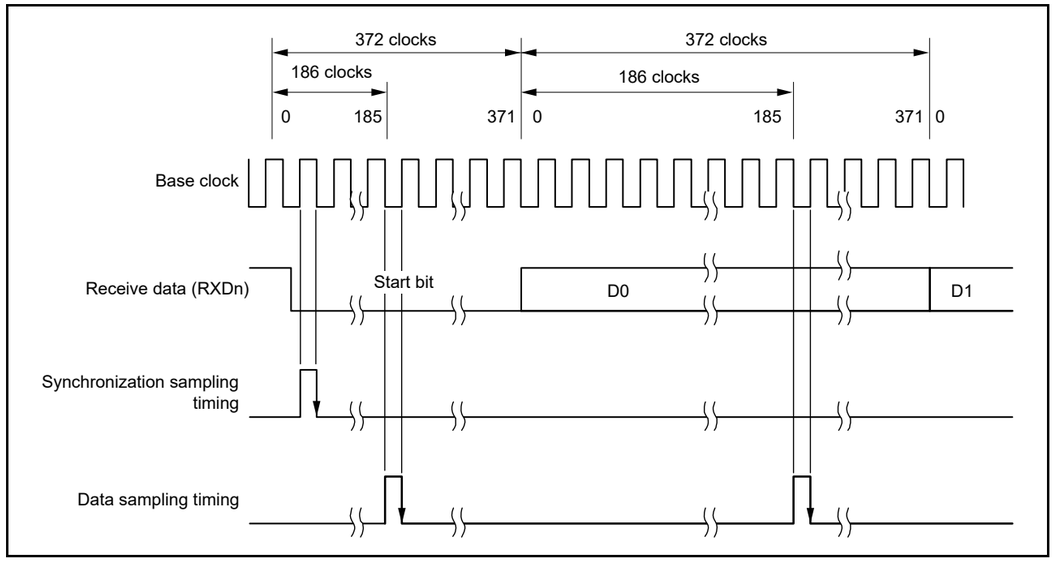


Figure 34.49 Receive data sampling timing in smart card interface mode when clock frequency is 372 times the bit rate

34.6.5 Initialization of the SCI

Before transmitting and receiving data, write the initial value 00h in the SCR_SMCI register and initialize the SCI following the example flow shown in Figure 34.50.

Always set the initial value in the TIE, RIE, TE, RE, TEIE bits in the SCR_SMCI register before switching from transmission to reception mode or from reception to transmission mode. When SCR_SMCI.RE is set to 0, the RDR register is not initialized.

To change from reception mode to transmission mode, first check that reception has completed, then initialize the SCI. At the end of initialization, set SSR_SMCI.TE = 1 and SSR_SMCI.RE = 0. Reception completion can be verified by reading the SCIn_RXI request, ORER, or PER flag in SSR_SMCI.

To change transmission mode to reception mode, first check that transmission has completed, then initialize the SCI. At the end of initialization, set SSR_SMCI.TE = 0 and SSR_SMCI.RE = 1. Transmission completion can be verified by reading the TEND flag in SSR_SMCI.

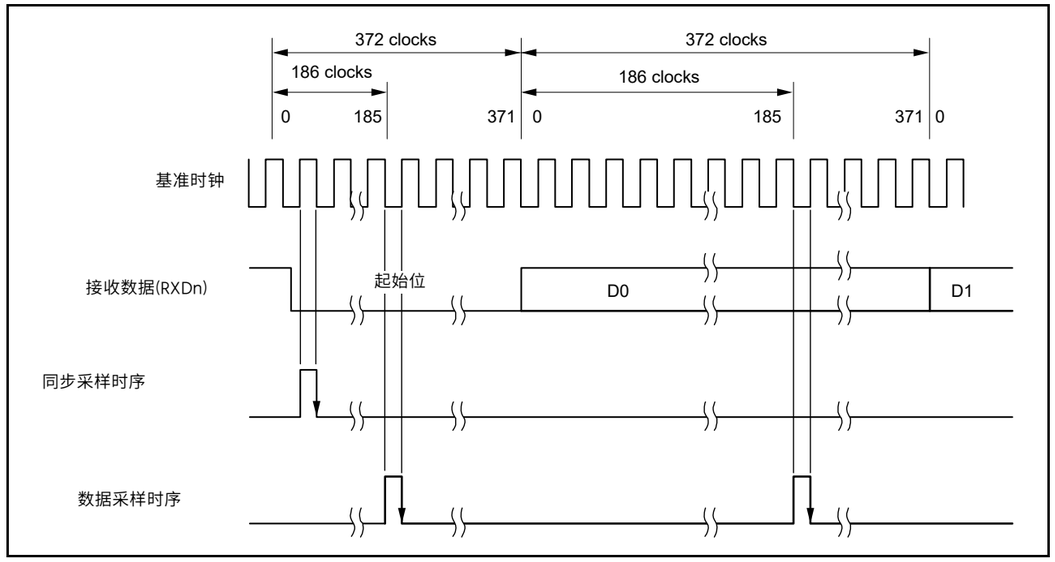


Figure 34.49 时钟频率为372倍比特率时智能卡接口模式下的接收数据采样时序

34.6.5 SCI的初始化

在发送和接收数据之前，将初始值00h写入SCR_SMCI寄存器并按照图34.50所示的示例流程初始化SCI。

在从发送模式切换到接收模式或从接收模式切换到发送模式之前，请务必在SCR_SMCI寄存器中的TIE、RIE、TE、RE、TEIE位中设置初始值。当SCR_SMCI.RE设置为0时，RDR寄存器未初始化。

要从接收模式更改为发送模式，首先检查接收是否完成，然后初始化SCI。
在初始化结束时，设置SSR_SMCI.TE=1和SSR_SMCI.RE=0。可以通过读取SSR_SMCI中的SCIn_RXI请求、ORER或PER标志来验证接收完成。

要将传输模式更改为接收模式，首先检查传输是否完成，然后初始化SCI。在初始化结束时，设置SSR_SMCI.TE=0和SSR_SMCI.RE=1。可以通过读取SSR_SMCI中的TEND标志来验证传输完成。

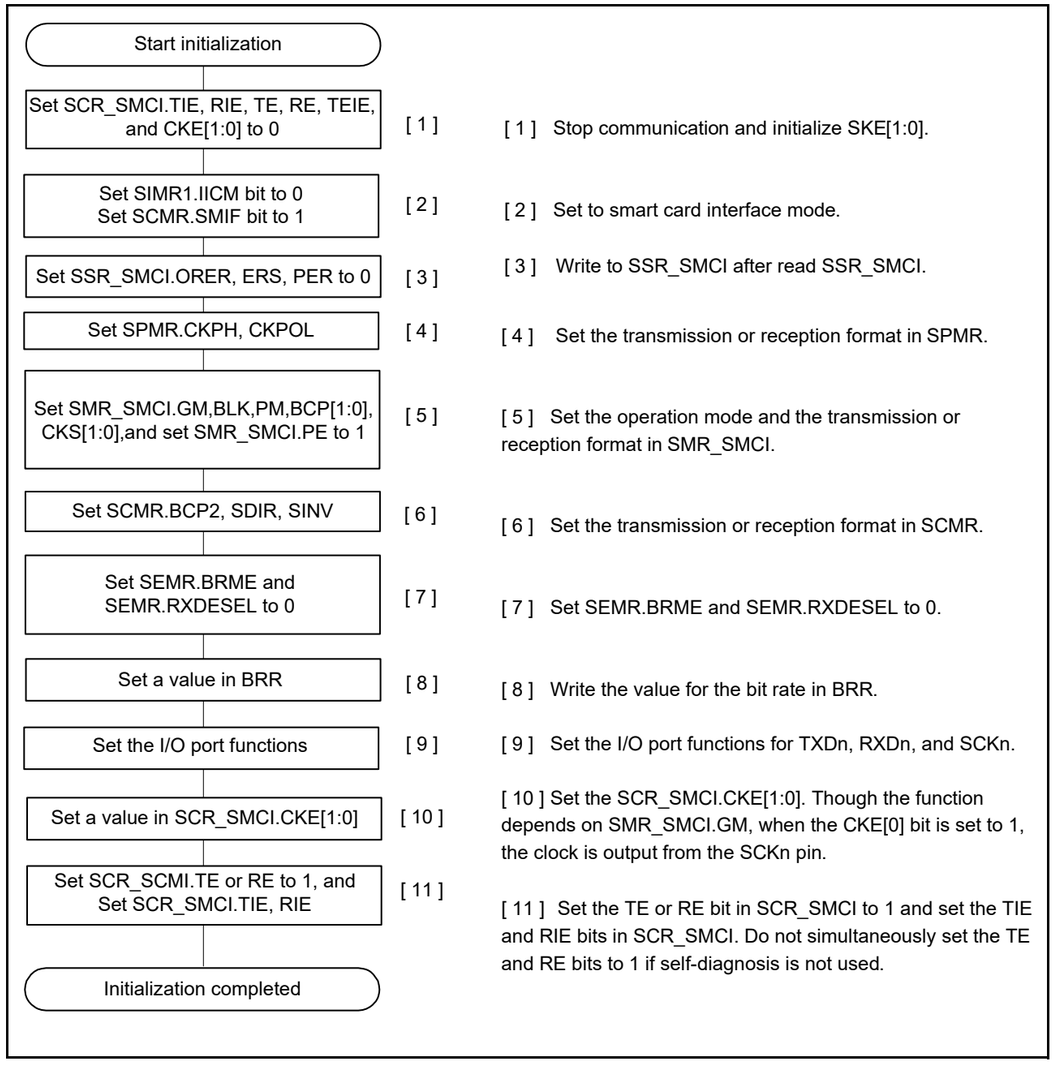


Figure 34.50 Example flow of SCI initialization in smart card interface mode

Figure 34.51 shows a timing diagram when data transmission is performed by transitioning to smart card interface mode according to the flow in Figure 34.50. Figure 34.51 shows when the GM bit in SMR_SMCI is set to 0. The timing in Figure 34.51 shows when the port is connected as SCKn pin and TXDn pin, the pins are Hi-Z because CKE[0] bit in SCR_SMCI is 0.

Start the clock output to the SCK pin by setting CKE[0] bit in SCR_SMCI to 1, then start data transmission by writing transmit data after setting TE bit in SCR_SMCI to 1. When the TE bit in SCR_SMCI changes from 0 to 1, there is a preamble period for one frame before data transmission starts. In smart card interface mode, the TXDn pin is Hi-Z during the preamble period. Pull-up or pull-down for the SCKn and TXDn pins is required outside the MCU.

In the smart card interface mode, even when the TE and RE bits in SCR_SMCI are 0, the clock is continuously output if the clock output setting is used.

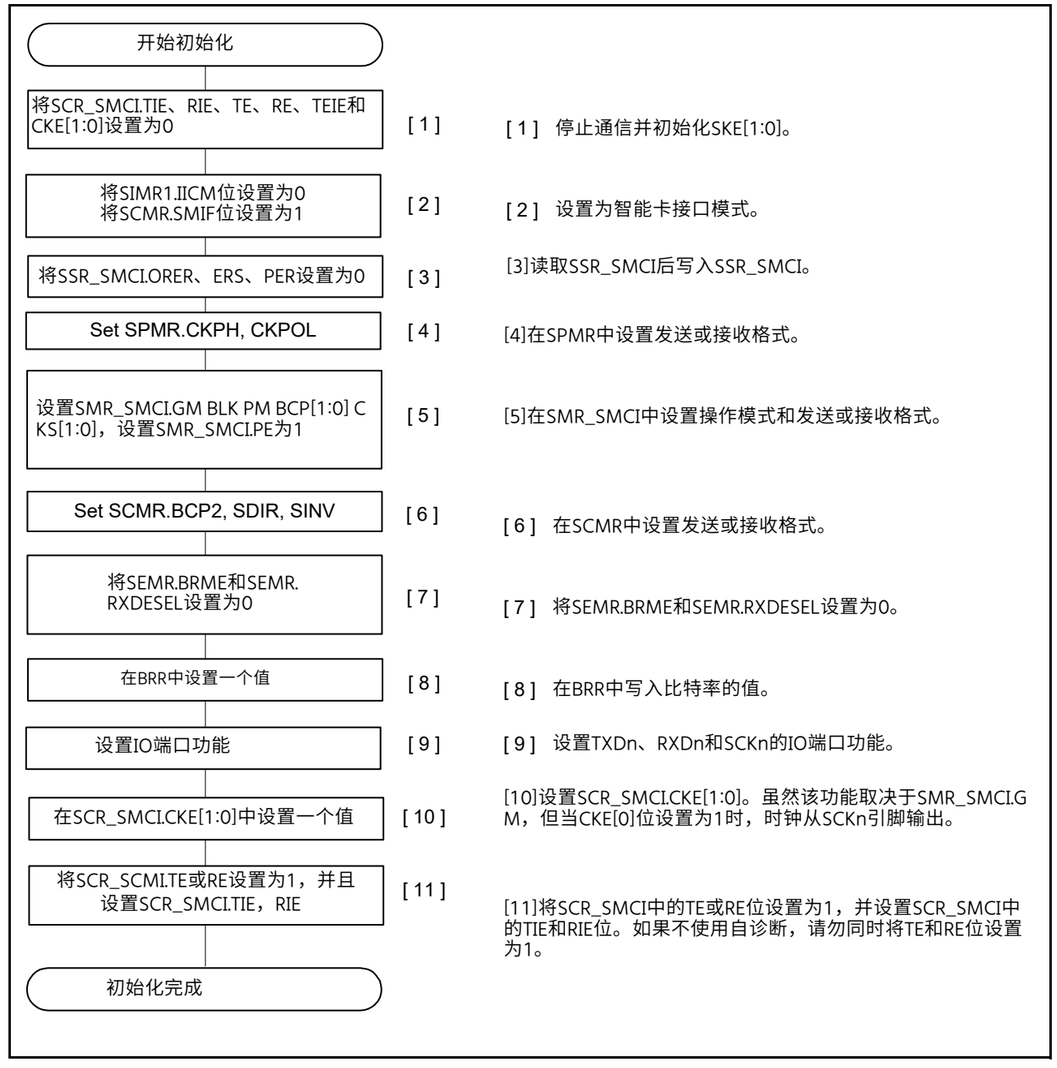


Figure 34.50 智能卡接口模式下SCI初始化流程示例

图34.51显示了根据图34.50中的流程通过转换到智能卡接口模式执行数据传输时的时序图。图34.51显示了SMR_SMCI中的GM位设置为0时。图34.51中的时序显示了当端口连接为SCKn引脚和TXDn引脚时，引脚为Hi-Z，因为CKE[0]位在

SCR_SMCI is 0.

通过将SCR_SMCI中的CKE[0]位设置为1，开始向SCK引脚输出时钟，然后在将SCR_SMCI中的TE位设置为1后，通过写入发送数据开始数据传输。当SCR_SMCI中的TE位从0变为1时，有是数据传输开始前一帧的前导周期。在智能卡接口模式下，TXDn引脚在前导期间为Hi-Z。SCKn和TXDn引脚的上拉或下拉需要在MCU外部进行。

在智能卡接口模式下，即使SCR_SMCI中的TE和RE位为0，如果使用时钟输出设置，时钟也会持续输出。

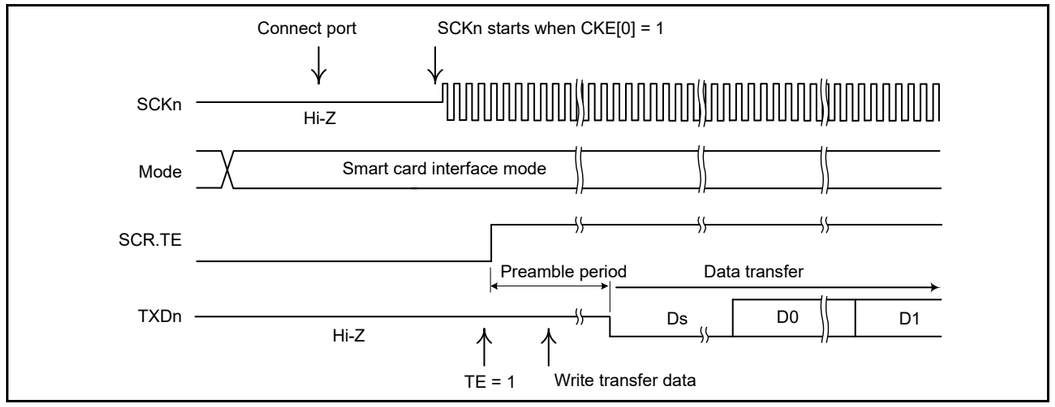


Figure 34.51 Example timing of data transmission in smart card interface mode

34.6.6 Serial Data Transmission (Except in Block Transfer Mode)

Serial data transmission in smart card interface mode (except in block transfer mode) is different from that in non-smart card interface mode, in that an error signal is sampled and data can be re-transmitted in smart card mode. Figure 34.52 shows the data re-transfer operation during transmission.

- [1] indicates when an error signal from the receiver end is sampled after 1-frame data is transmitted, the SSR_SMCI.ERS flag is set to 1. If the SCR_SMCI.RIE bit is 1, an SCIn_ERI interrupt request is generated. Clear the ERS flag to 0 before the next parity bit is sampled.
- [2] indicates for a frame in which an error signal is received, the SSR_SMCI.TEND flag is not set. Data is re-transferred from TDR to TSR, allowing automatic data retransmission.
- [3] indicates if no error signal is returned from the receiver, the ERS flag is not set to 1.
- [4] indicates the SCI determines that transmission of 1-frame data, including the re-transfer, is complete, and the TEND flag is set. If the SCR_SMCI.TIE bit is 1, an SCIn_TXI interrupt request is generated. Write transmit data to the TDR to start transmission of the next data.

Figure 34.54 shows an example flow of serial transmission. All the processing steps are automatically performed using an SCIn_TXI interrupt request to activate the DTC or DMAC.

When the SSR_SMCI.TEND flag is set to 1 in transmission and when the SCR_SMCI.TIE bit is 1, an SCIn_TXI interrupt request is generated.

The DTC or DMAC is activated by an SCIn_TXI interrupt request if the SCIn_TXI interrupt request is previously specified as a source of DTC or DMAC activation, allowing the transfer of transmit data. The TEND flag is automatically set to 0 when the DTC or DMAC transfers the data.

If an error occurs, the SCI automatically retransmits the same data. During this retransmission, the TEND flag is kept at 0 and the DTC or DMAC is not activated. Therefore, the SCI and DTC or DMAC automatically transmit the specified number of bytes, including retransmission when an error occurs. Because the ERS flag is not automatically cleared, set the RIE bit to 1 before enabling an SCIn_ERI interrupt request to be generated if an error occurs, and clear the ERS flag to 0.

When transmitting or receiving data using the DTC or DMAC, always enable the DTC or DMAC before making the SCI settings.

For DTC or DMAC settings, see section 17, DMA Controller (DMAC) and section 18, Data Transfer Controller (DTC).

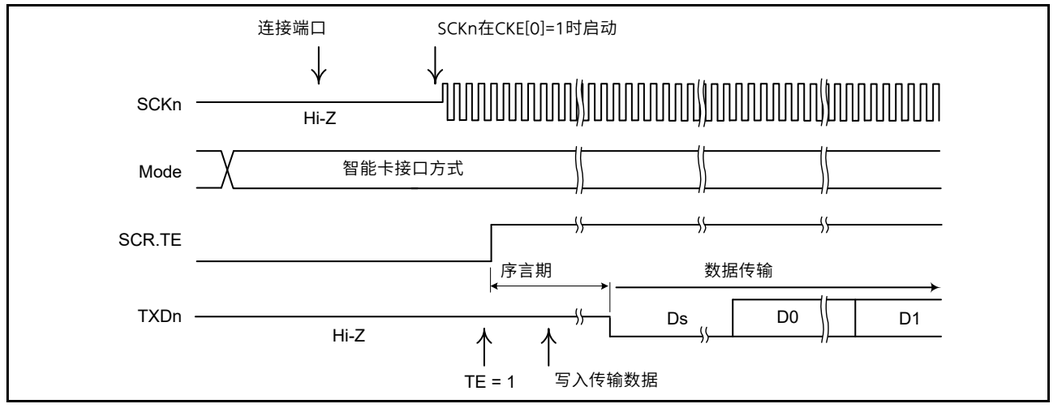


Figure 34.51 智能卡接口模式下数据传输时序示例

34.6.6 串行数据传输（块传输模式除外）

智能卡接口模式下的串行数据传输（块传输模式除外）与非智能卡接口模式下的串行数据传输不同之处在于，在智能卡模式下对错误信号进行采样，数据可以重新传输。图34.52显示了传输过程中的数据重传操作。

- [1]表示在发送1帧数据后采样到来自接收端的错误信号时，SSR_SMCI.ERS标志置1。如果SCR_SMCI.RIE位为1，则产生SCIn_ERI中断请求。在采样下一个奇偶校验位之前将ERS 标志清零。
- [2]表示对于接收到错误信号的帧，未设置SSR_SMCI.TEND标志。数据从TDR重新传输到TSR，允许自动数据重新传输。
- [3]表示如果接收器没有返回错误信号，则ERS 标志不设置为1。
- [4]表示SCI确定1帧数据的传输（包括重新传输）已完成，并且设置了TEND标志。如果SCR_SMCI.TIE位为1，则产生SCIn_TXI中断请求。将传输数据写入TDR以开始传输下一个数据。

图34.54显示了串行传输的示例流程。所有处理步骤都使用SCIn_TXI中断请求自动执行以激活DTC或DMAC。

当发送中SSR_SMCI.TEND标志设置为1且SCR_SMCI.TIE位为1时，将产生SCIn_TXI中断请求。

如果先前将SCIn_TXI中断请求指定为DTC或DMAC激活源，则DTC或DMAC由SCIn_TXI中断请求激活，从而允许传输发送数据。当DTC或DMAC传输数据时，TEND标志自动设置为0。

如果发生错误，SCI会自动重新传输相同的数据。在此重传期间，TEND标志保持为0，并且DTC或DMAC未激活。因此，SCI和DTC或DMAC会自动传输指定的字节数，包括发生错误时的重传。因为ERS 标志不会自动清零，所以如果发生错误，在使能SCIn_ERI中断请求之前将RIE位设置为1，并将ERS 标志清零。

使用DTC或DMAC发送或接收数据时，请务必在进行SCI设置之前启用DTC或DMAC。

有关DTC或DMAC设置，请参阅第17节，DMA控制器(DMAC)和第18节，数据传输控制器(DTC)。

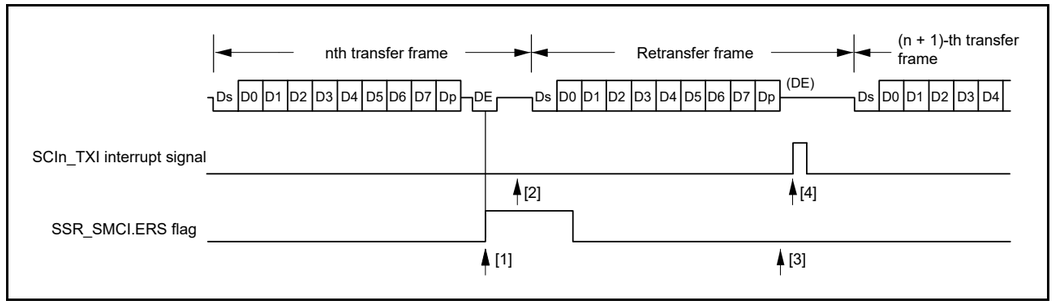


Figure 34.52 Data retransfer operation in SCI transmission mode

The SSR_SMCI.TEND flag is set at different timings depending on the SMR_SMCI.GM bit setting. Figure 34.53 shows the TEND flag generation timing.

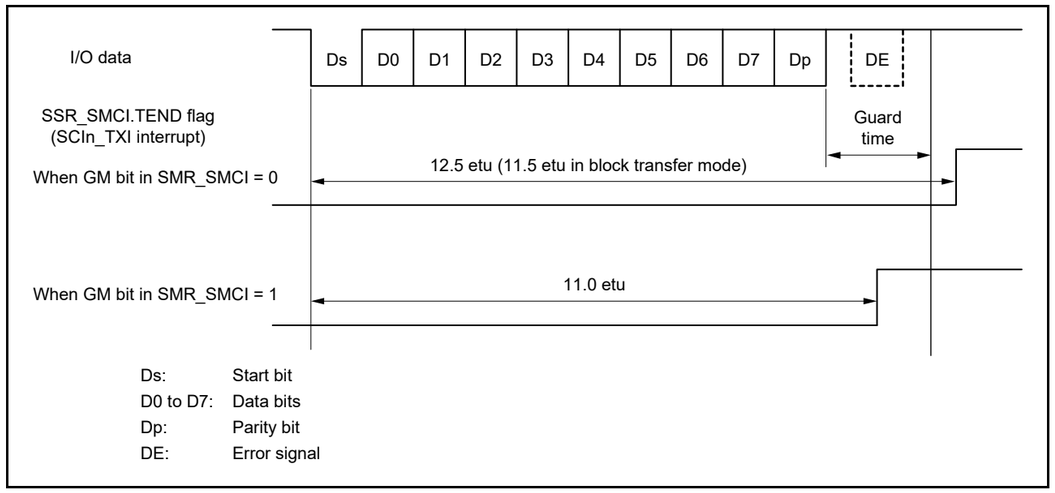


Figure 34.53 SSR.TEND flag generation timing during transmission

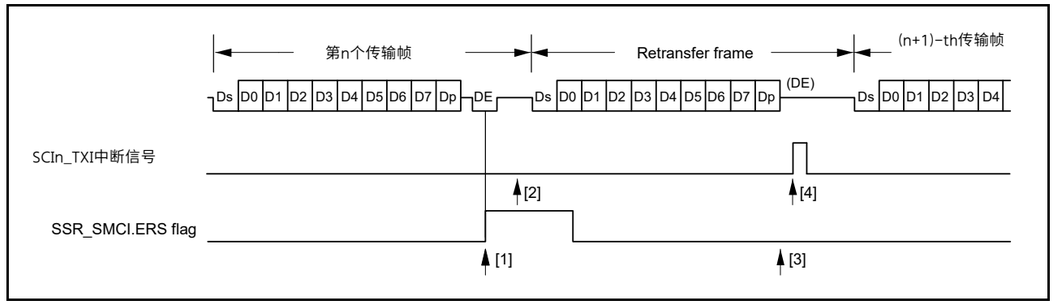


Figure 34.52 SCI传输模式下的数据重传操作

SSR_SMCI.TEND标志根据SMR_SMCI.GM位设置在不同的时间设置。图34.53显示了TEND标志生成时序。

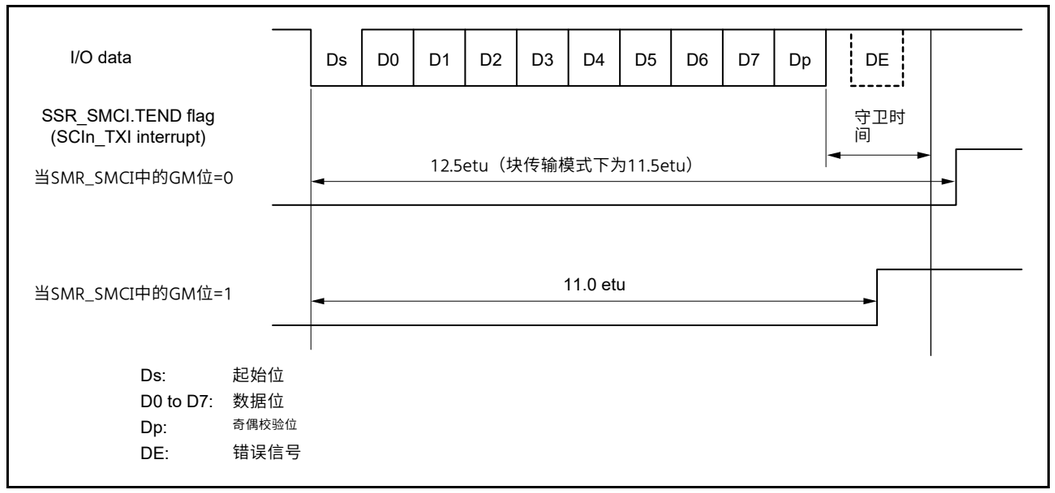


Figure 34.53 发送期间的SSR.TEND标志生成时序

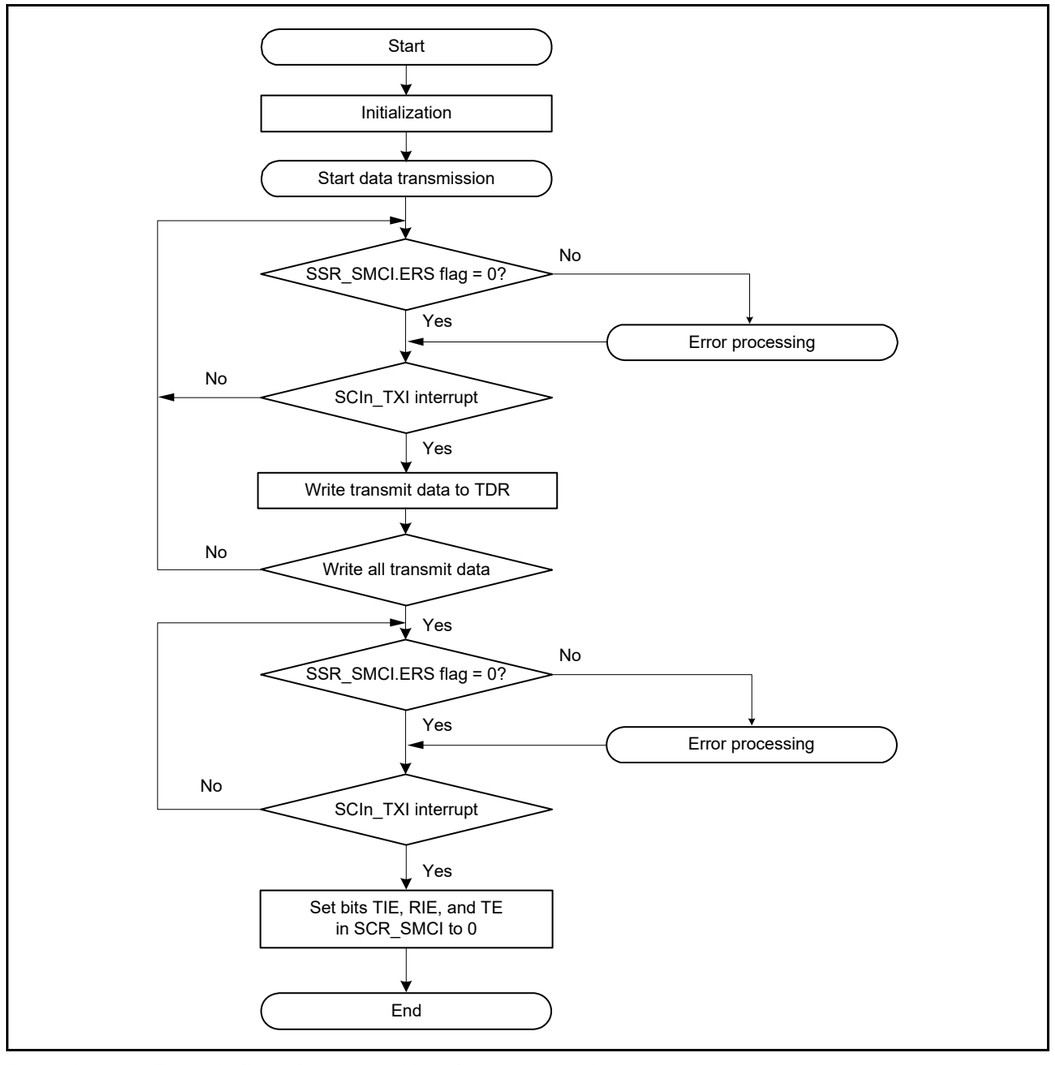


Figure 34.54 Example flow of smart card interface transmission

34.6.7 Serial Data Reception (Except in Block Transfer Mode)

Serial data reception in smart card interface mode is similar to that in non-smart card interface mode. Figure 34.55 shows the data re-transfer operation in reception mode.

- [1] indicates if a parity error is detected in the receive data, the SSR_SMCI.PER flag is set to 1. When the SCR_SMCI.RIE bit is 1, an SCIn_ERI interrupt request is generated. Clear the PER flag to 0 before the next parity bit is sampled.
- [2] indicates for a frame in which a parity error is detected, no SCIn_RXI interrupt is generated.
- [3] indicates when no parity error is detected, the SCR_SMCI.PER flag is not set to 1.
- [4] indicates the data is determined to be received successfully. When the SCR_SMCI.RIE bit is 1, an SCIn_RXI interrupt request is generated.

Figure 34.56 shows an example flow of serial data reception. All the processing steps are automatically performed using

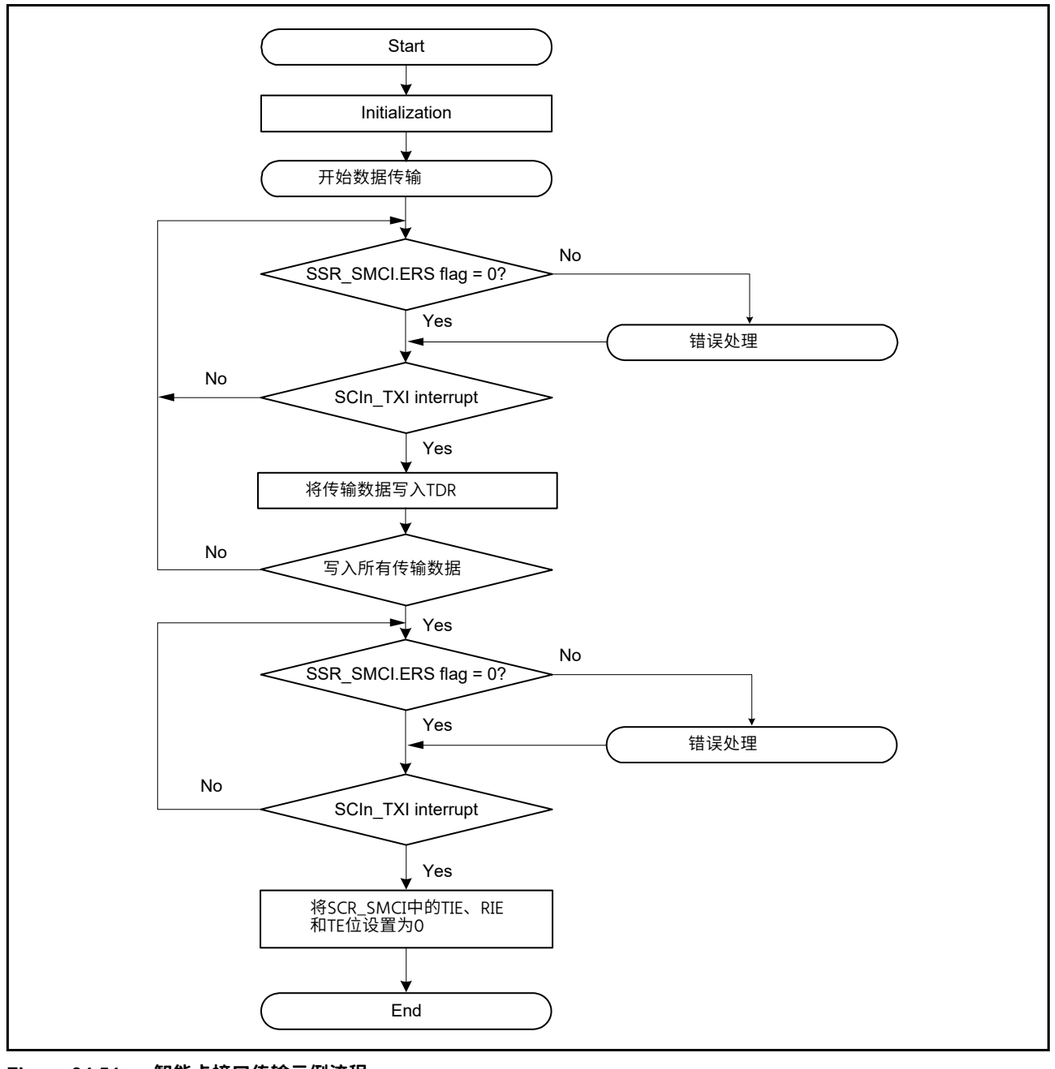


Figure 34.54 智能卡接口传输示例流程

34.6.7 串行数据接收（块传输模式除外）

智能卡接口模式下的串行数据接收与非智能卡接口模式下的串行数据接收类似。图34.55显示了接收模式下的数据重传操作。

- [1]表示如果在接收数据中检测到奇偶校验错误，则SSR_SMCI.PER标志设置为1。当SCR_SMCI.RIE位为1时，产生SCIn_ERI中断请求。在采样下一个奇偶校验位之前将PER标志清零。
- [2]表示对于检测到奇偶校验错误的帧，不产生SCIn_RXI中断。
- [3]表示当没有检测到奇偶校验错误时，SCR_SMCI.PER标志不设置为1。
- [4]表示确定数据接收成功。当SCR_SMCI.RIE位为1时，产生SCIn_RXI中断请求。

图34.56显示了串行数据接收的示例流程。所有处理步骤都使用自动执行

an SCIn_RXI interrupt request to activate the DTC or DMAC.

In reception, setting the RIE bit to 1 allows an SCIn_RXI interrupt request to be generated. The DTC or DMAC is activated by an SCIn_RXI interrupt request if the SCIn_RXI interrupt request is previously specified as a source of DTC or DMAC activation, allowing the transfer of receive data.

If an error occurs during reception and either the ORER or PER flag in SSR_SMCI is set to 1, a receive error interrupt (SCIn_ERI) request is generated. Clear the error flag after the error occurrence. If an error occurs, the DTC or DMAC is not activated and receive data is skipped. Therefore, the number of bytes of receive data specified in the DTC or DMAC is transferred.

If a parity error occurs and the PER flag is set to 1 during reception, the receive data is transferred to RDR, allowing the data to be read.

When a reception is forced to terminate by setting SCR_SMCI.RE to 0 during operation, read the RDR register because the received data that is not yet read might be left in the RDR.

Note: For operations in block transfer mode, see section 34.3.9, Serial Data Reception in Asynchronous Mode.

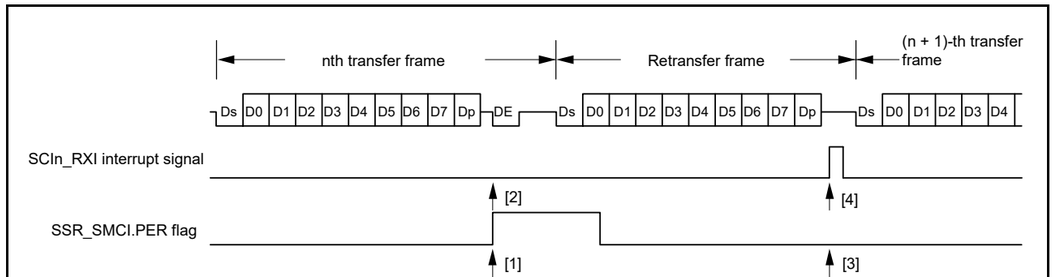


Figure 34.55 Data retransfer operation in SCI reception mode

SCIn_RXI中断请求以激活DTC或DMAC。

在接收时，将RIE位设置为1允许产生SCIn_RXI中断请求。如果先前将SCIn_RXI中断请求指定为DTC或DMAC激活源，则DTC或DMAC由SCIn_RXI中断请求激活，从而允许传输接收数据。

如果接收期间发生错误并且SSR_SMCI中的ORER或PER标志设置为1，则会生成接收错误中断(SCIn_ERI)请求。错误发生后清除错误标志。如果发生错误，则不会激活DTC或DMAC并跳过接收数据。因此，将传输DTC或DMAC中指定的接收数据字节数。

如果在接收过程中发生奇偶校验错误并且PER标志设置为1，则接收数据将传输到RDR，从而可以读取数据。

如果在操作期间通过将SCR_SMCI.RE设置为0来强制终止接收，请读取RDR寄存器，因为尚未读取的已接收数据可能留在RDR中。

Note: 有关块传输模式下的操作，请参见第34.3.9节，异步模式下的串行数据接收。

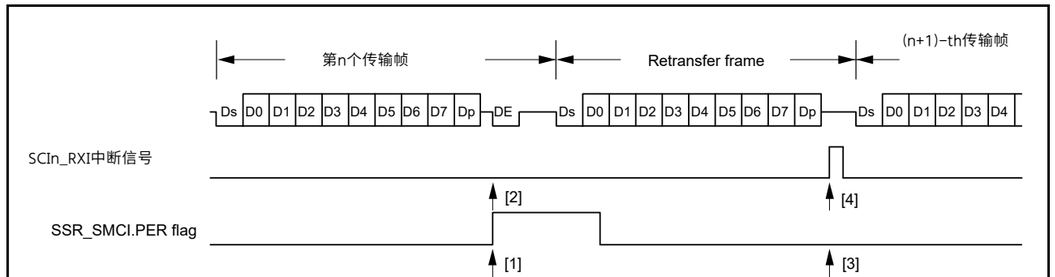


Figure 34.55 SCI接收模式下的数据重传操作

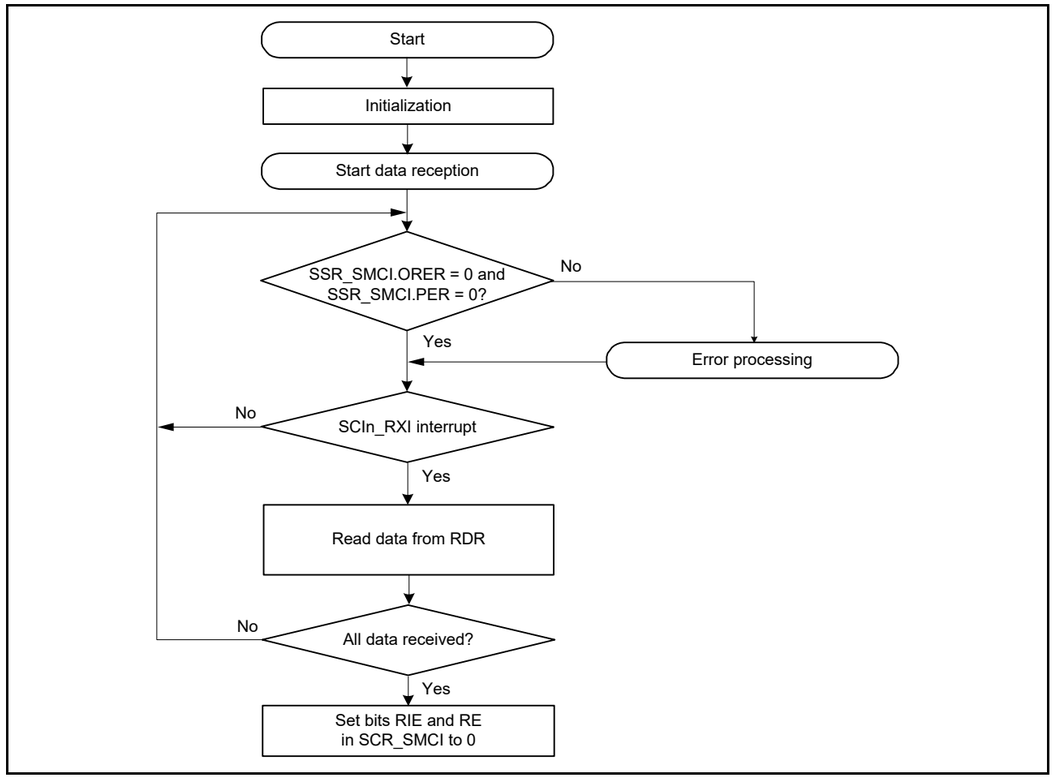


Figure 34.56 Example flow of smart card interface reception

34.6.8 Clock Output Control

When the GM bit in SMR_SMCI is set to 1, the clock output can be controlled by the CKE[1: 0] bits in SCR_SMCI. For details on the CKE[1:0] bits, see section 34.2.12, Serial Control Register for Smart Card Interface Mode (SCR_SMCI) (SCMR.SMIF = 1). When setting the clock output, the base clock described in section 34.6.4, Receive Data Sampling Timing and Reception Margin is output.

Figure 34.57 shows an example timing for the clock output control when the CKE[1] bit in SCR_SMCI is set to 0 and the CKE[0] bit in SCR_SMCI is controlled.

When the GM bit in SMR_SMCI is 0, output control by the CKE[0] bit in SCR_SMCI is immediately reflected on the SCK pin, so there is a possibility that pulses with an unintended width might be output from the SCK pin.

When the GM bit in SMR_SMCI is 1, the clock with the same pulse width as the base clock is output even if the CKE[0] bit in SCR_SMCI is changed.

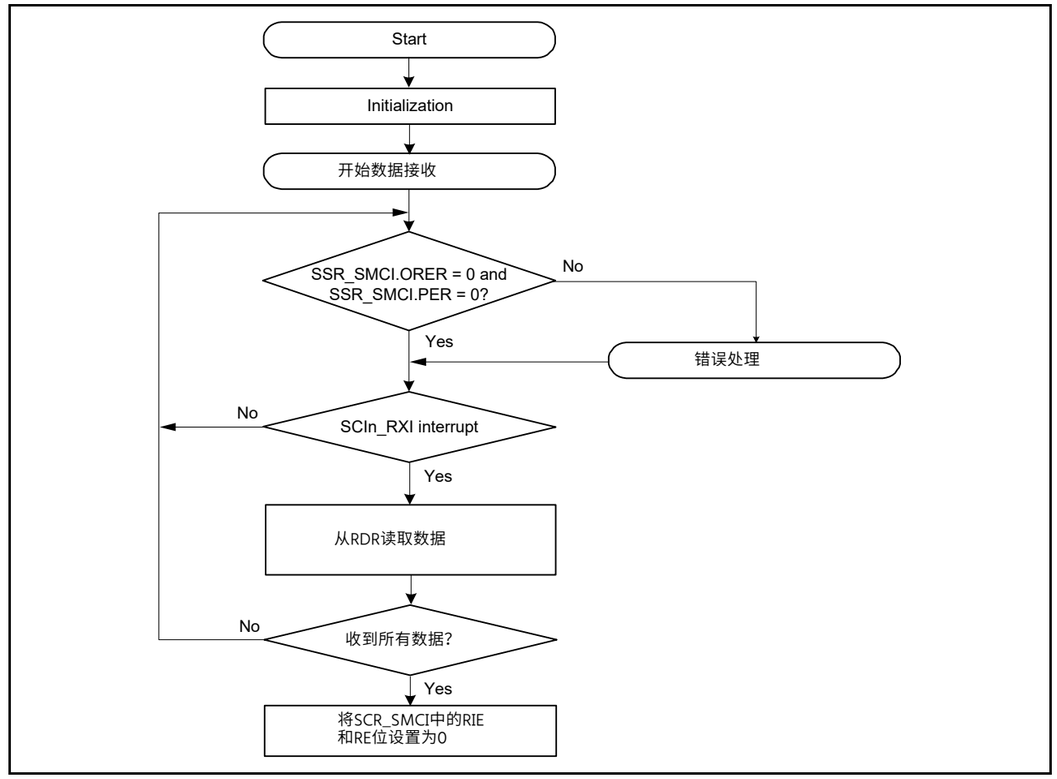


Figure 34.56 智能卡接口接收示例流程

34.6.8 时钟输出控制

当SMR_SMCI中的GM位设置为1时，时钟输出可由SCR_SMCI中的CKE[1:0]位控制。有关CKE[1:0]位的详细信息，请参见第34.2.12节，智能卡接口模式的串行控制寄存器(SCR_SMCI)(SCMR.SMIF=1)。设置时钟输出时，输出第34.6.4节"接收数据采样时序和接收裕度"中描述的基本时钟。

图34.57显示了当SCR_SMCI中的CKE[1]位设置为0且
控制SCR_SMCI中的CKE[0]位。

当SMR_SMCI中的GM位为0时，SCR_SMCI中CKE[0]位的输出控制立即反映在
SCK引脚，因此有可能会从SCK引脚输出具有意外宽度的脉冲。

当SMR_SMCI中的GM位为1时，即使SCR_SMCI中的CKE[0]位发生变化，也会输出与基本时钟脉冲宽度相同的时钟。

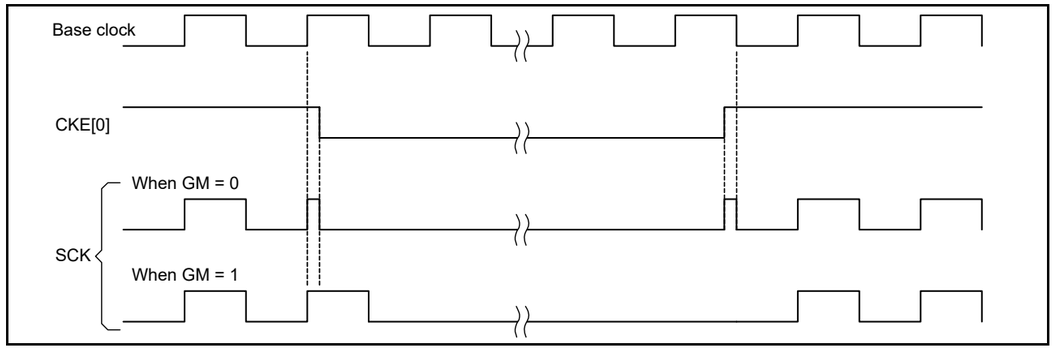


Figure 34.57 Clock output control

34.7 Operation in Simple IIC Mode

Simple IIC mode format is composed of 8 data bits and an acknowledge bit. By continuing into a slave-address frame after a start condition or restart condition, a master device can specify a slave device as the partner for communications. The currently specified slave device remains valid until a new slave device is specified or a stop condition is satisfied. The 8 data bits in all frames are transmitted in order from the MSB.

The I²C bus format and timing of the I²C bus are shown in Figure 34.58 and Figure 34.59.

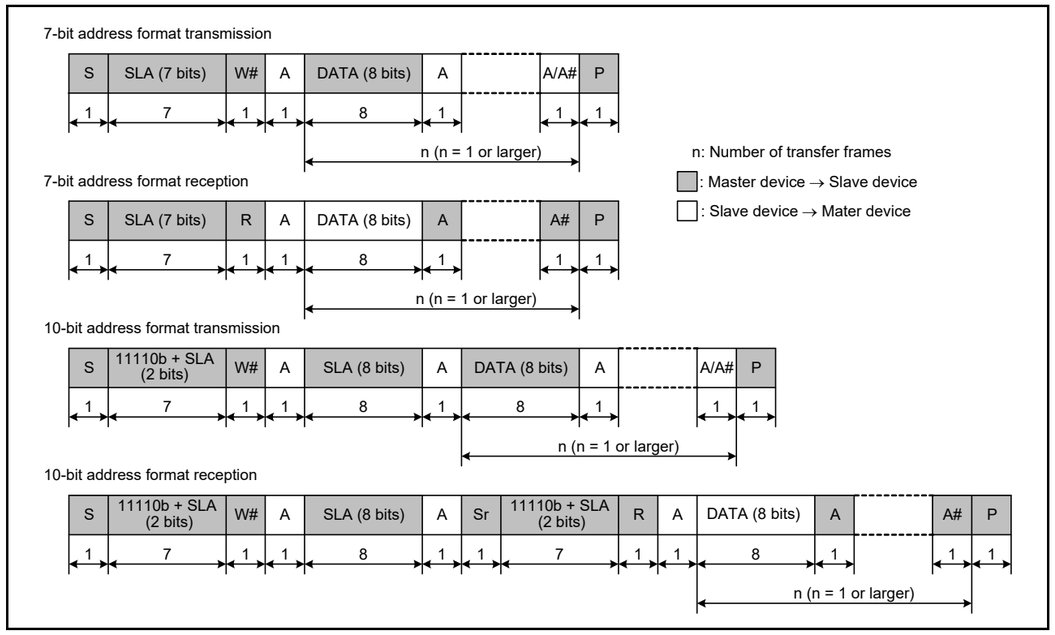


Figure 34.58 I²C bus format

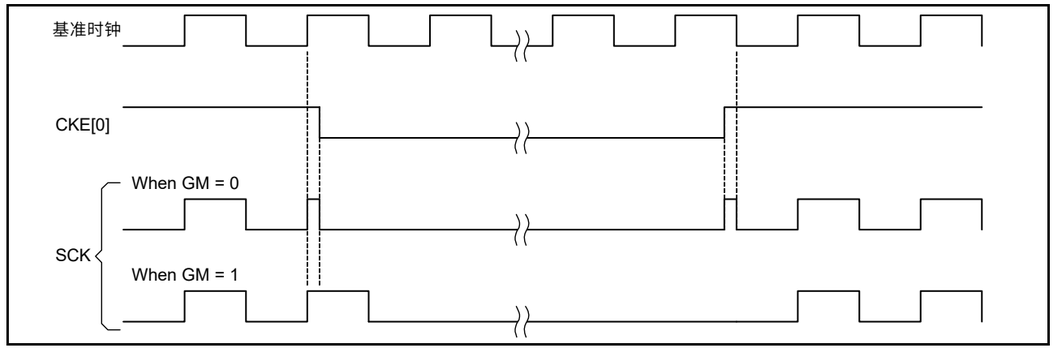


Figure 34.57 时钟输出控制

34.7 简单IIC模式下的操作

简单IIC模式格式由8个数据位和一个确认位组成。通过在启动条件或重新启动条件之后继续进入从地址帧，主设备可以指定从设备作为通信伙伴。当前指定的从设备保持有效，直到指定新的从设备或满足停止条件。

所有帧中的8个数据位从MSB开始按顺序传输。

I2C总线格式和I2C总线时序如图34.58和图34.59所示。

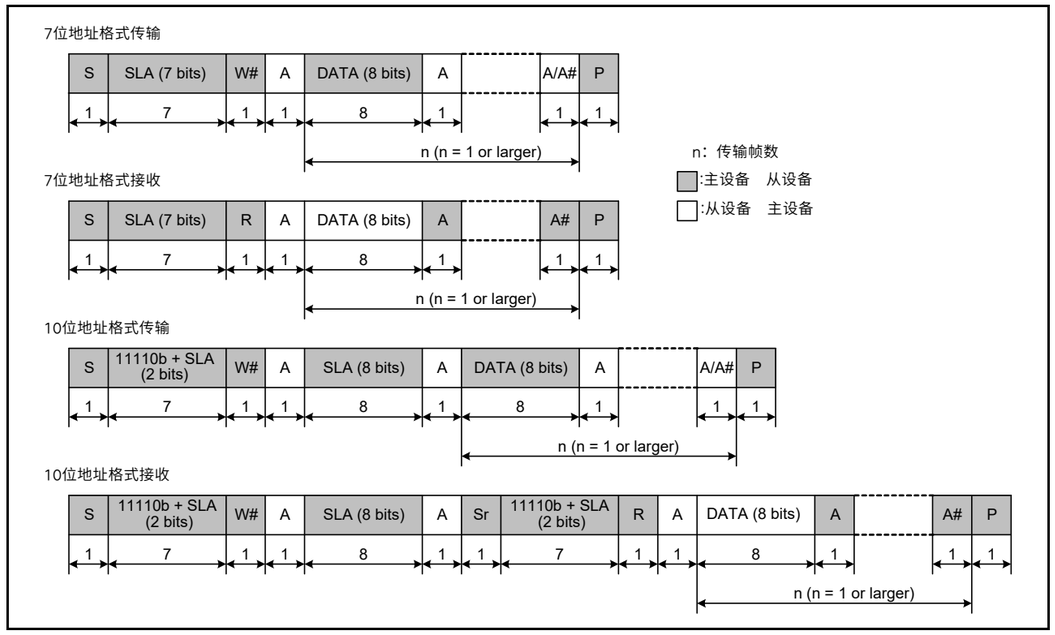


Figure 34.58 I2C总线格式

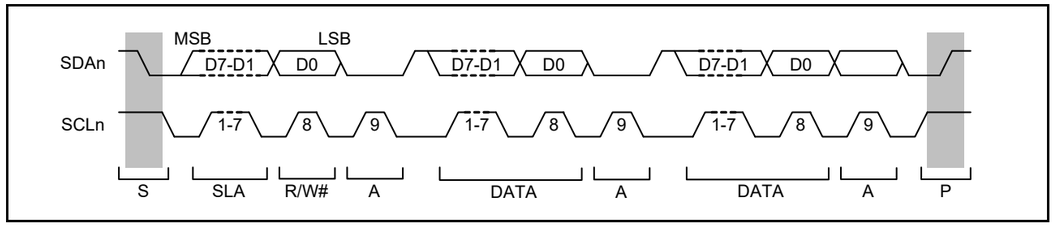


Figure 34.59 I²C bus timing when SLA is 7 bits

- S: Indicates a start condition, when the master device changes the level on the SDAn line from high to low while the SCLn line is high
- SLA: Indicates a slave address, by which the master device selects a slave device
- R/W#: Indicates the direction of transfer (reception or transmission). The value 1 indicates transfer from the slave device to the master device and 0 indicates transfer from the master device to the slave device.
- A/A#: Indicates an acknowledge bit. This is returned by the slave device for master transmission and by the master device for master reception. Return low indicates ACK and return high indicates NACK.
- Sr: Indicates a restart condition, when the master device changes the level on the SDAn line from high to low while the SCLn line is high and after the setup time elapses
- DATA: Indicates the data being received or transmitted
- P: Indicates a stop condition, when the master device changes the level on the SDAn line from low to high while the SCLn line is high.

34.7.1 Generation of Start, Restart, and Stop Conditions

Writing 1 to the SIMR3.IICSTAREQ bit causes the generation of a start condition. The generation of a start condition proceeds through the following operations:

- The level on the SDAn line falls (from the high level to the low level) and the SCLn line is kept in the released state
- The hold time for the start condition is set as half of a bit period at the bit rate determined by the BRR setting
- The level on the SCLn line falls (from the high level to the low level), the IICSTAREQ bit in SIMR3 is set to 0, and a start-condition generated interrupt is output.

Writing 1 to the IICRSTAREQ bit in SIMR3 causes the generation of a restart condition. The generation of a restart condition proceeds through the following operations:

- The SDAn line is released and the SCLn line is kept at the low level
- The period at low level for the SCLn line is set as half of a bit period at the bit rate determined by the BRR setting
- The SCLn line is released (transition from the low to the high level)
- When a high level is detected on the SCLn line, the setup time for the restart condition is set as half of a bit period at the bit rate determined by the BRR setting
- The level on the SDAn line falls (from the high level to the low level)
- The hold time for the restart condition is set as half of a bit period at the bit rate determined by the BRR setting
- The level on the SCLn line falls (from the high level to the low level), the SIMR3.IICRSTAREQ bit is set to 0, and a restart-condition generated interrupt is output.

Writing 1 to the SIMR3.IICSTPREQ bit causes the generation of a stop condition. The generation of a stop condition proceeds through the following operations:

- The level on the SDAn line falls (from the high level to the low level) and the SCLn line is kept at the low level
- The period at low level for the SCLn line is set as half of a bit period at the bit rate determined by the BRR setting

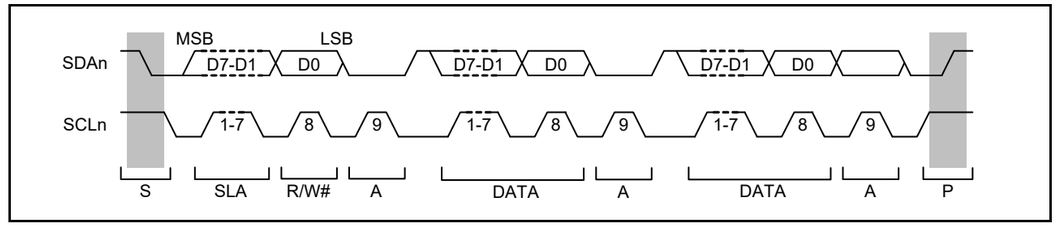


Figure 34.59 SLA为7位时的I2C总线时序

- S：表示启动条件，当主设备将SDAn线上的电平从高电平变为低电平时，SCLn线高
- SLA：表示从地址，主设备通过该地址选择从设备
- RW#：指示传输方向（接收或传输）。值1表示从从设备传输到主设备，0表示从主设备传输到从设备。
- AA#：表示确认位。这由从设备返回用于主传输，并由主设备返回用于主接收。返回低电平表示ACK，返回高电平表示NACK。
- Sr：表示重启条件，当主设备将SDAn线上的电平从高电平变为低电平，而SCLn线为高电平且经过设置时间后
- DATA：表示正在接收或发送的数据
- P：表示停止条件，当主设备将SDAn线上的电平从低变为高，而SCLn线高。

34.7.1 启动、重启和停止条件的生成

将1写入SIMR3.IICSTAREQ位会导致产生启动条件。开始条件的生成通过以下操作进行：

- SDAn线上的电平下降（从高电平到低电平），SCLn线保持在释放状态
- 开始条件的保持时间设置为比特周期的一半，比特率由BRR设置确定
- SCLn线上的电平下降（从高电平变为低电平），SIMR3中的IICSTAREQ位设置为0，并输出一个起始条件产生的中断。

将1写入SIMR3中的IICRSTAREQ位会导致产生重启条件。重新启动条件的生成通过以下操作进行：

- SDAn线被释放，SCLn线保持在低电平
- SCLn线的低电平周期设置为比特周期的一半，比特率由BRR设置确定
- SCLn线被释放（从低电平过渡到高电平）
- 当在SCLn线上检测到高电平时，重新启动条件的建立时间设置为比特周期的一半，比特率由BRR设置确定

- SDAn线上的电平下降（从高电平到低电平）
- 重启条件的保持时间设置为比特周期的一半，比特率由BRR设置确定
- SCLn线上的电平下降（从高电平变为低电平），SIMR3.IICRSTAREQ位设置为0，并输出重启条件产生的中断。

将1写入SIMR3.IICSTPREQ位会导致产生停止条件。停止条件的生成通过以下操作进行：

- SDAn线上的电平下降（从高电平到低电平），SCLn线上保持低电平
- SCLn线的低电平周期设置为比特周期的一半，比特率由BRR设置确定

- The SCLn line is released (transition from the low to the high level)
- When a high level is detected on the SCLn line, the setup time for the stop condition is set as half of a bit period at the bit rate determined by the BRR setting
- The SDAn line is released (transition from the low to the high level), the SIMR3.IICSTPREQ bit is set to 0, and a stop-condition generated interrupt is output.

Figure 34.60 shows the timing of operations in the generation of start, restart, and stop conditions.

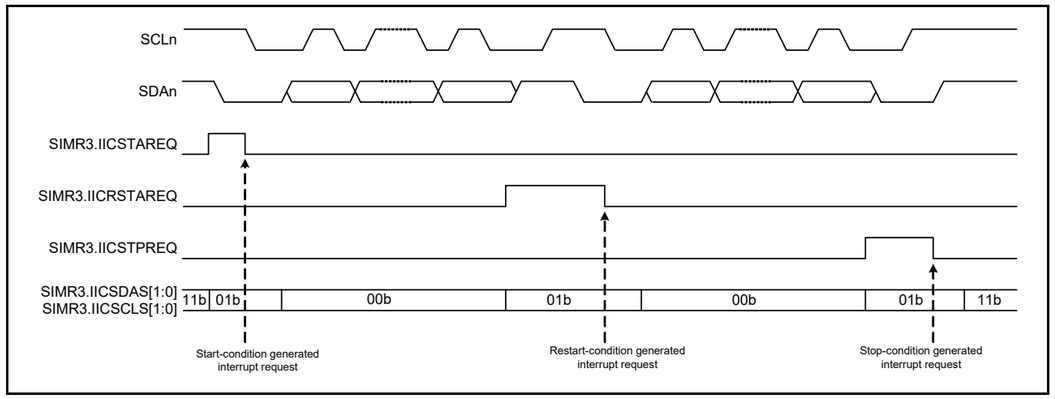


Figure 34.60 Timing of operations in generation of start, restart, and stop conditions

34.7.2 Clock Synchronization

The SCLn line can be driven low if a wait is inserted by a slave device at the other side of the transfer. Setting the SIMR2.IICCSC bit to 1 applies control to obtain synchronization when a difference arises between the levels of the internal SCLn clock signal and the level being input on the SCLn pin.

When the SIMR2.IICCSC bit is set to 1, the level of the internal SCLn clock signal changes from low to high. Counting to determine the period at a high level stops while the low level is being input on the SCLn pin. Counting to determine the period at a high level starts after the transition of the input on the SCLn pin to the high level.

The interval from this time until counting to determine the period at high level starts on the transition of the SCLn pin to the high level, is the total of the delay of SCLn output, delay for noise filtering of the input on the SCLn pin (2 or 3 cycles of sampling clock for the noise filter), and delay for internal processing (1 or 2 cycles of PCLKA). The period at high level of the internal SCLn clock is extended even when other devices do not place the low level on the SCLn line.

If the SIMR2.IICCSC bit is 1, synchronization is obtained for the transmission and reception of data by taking the logical AND of the input on the SCLn pin and the internal SCLn clock. If the SIMR2.IICCSC bit is 0, synchronization with the internal SCLn clock is obtained for the transmission and reception of data.

If a slave device inserts a wait period into the interval until the transition of the internal SCLn clock signal from the low to the high level after a request for the generation of a start, restart, or stop condition is issued, the time until generation is prolonged by that period.

If a slave device inserts a wait period after the transition of the internal SCLn clock signal from the low to the high level, although the generation-completed interrupt is issued without stopping the waiting period, generation of the condition itself is not guaranteed. Figure 34.61 shows an example operation for synchronizing the clocks.

- SCLn线被释放（从低电平过渡到高电平）
- 当在SCLn线上检测到高电平时，停止条件的建立时间设置为由BRR设置确定的比特率的半个比特周期
- SDAn线被释放（从低电平转换为高电平），SIMR3.IICSTPREQ位设置为0，并输出停止条件产生的中断。

图34.60显示了生成启动、重启和停止条件的操作时序。

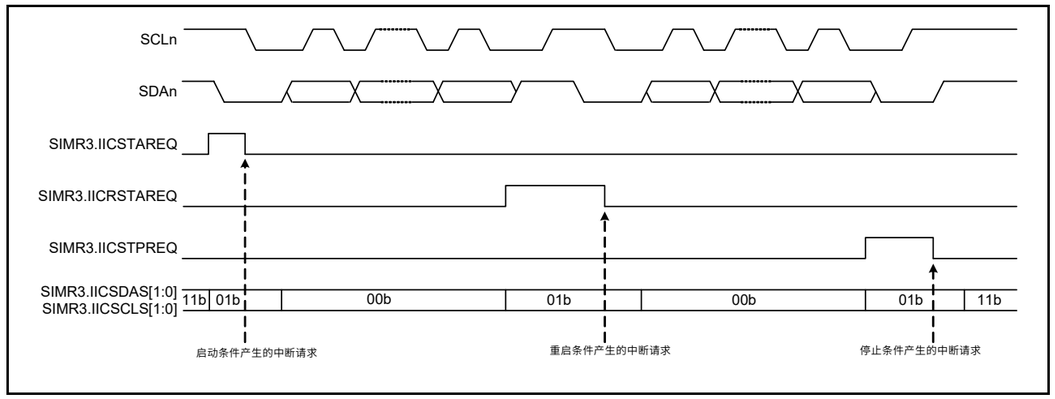


Figure 34.60 生成启动、重启和停止条件时的操作时序

34.7.2 时钟同步

如果从设备在传输的另一侧插入等待，则可以将SCLn线驱动为低电平。设置SIMR2.IICCSC位为1时，当内部SCLn时钟信号的电平与输入到SCLn引脚的电平之间出现差异时，应用控制以获得同步。

当SIMR2.IICCSC位设置为1时，内部SCLn时钟信号的电平由低变为高。当SCLn引脚输入低电平时，停止计数以确定高电平周期。在SCLn引脚上的输入转换为高电平后，开始计数以确定高电平的周期。

从这个时间到从SCLn引脚转换为高电平开始计数确定高电平周期的时间间隔是SCLn输出延迟的总和，SCLn引脚上输入的噪声过滤延迟（2或3个周期的采样时钟用于噪声滤波器），以及延迟用于内部处理（1或2个PCLKA周期）。即使其他设备没有将低电平置于SCLn线上，内部SCLn时钟的高电平周期也会延长。

如果SIMR2.IICCSC位为1，则通过对SCLn引脚上的输入和内部SCLn时钟进行逻辑与来获得数据发送和接收的同步。如果SIMR2.IICCSC位为0，则与内部SCLn时钟同步以进行数据的发送和接收。

如果从设备在发出启动、重新启动或停止条件的生成请求后，在内部SCLn时钟信号从低电平转变为高电平之前的间隔中插入一个等待周期，则直到生成的时间为延长了那个时期。

如果从设备在内部SCLn时钟信号从低电平转变为高电平之后插入等待周期，尽管在不停止等待周期的情况下发出生成完成中断，但不能保证条件本身的生成。图34.61显示了同步时钟的示例操作。

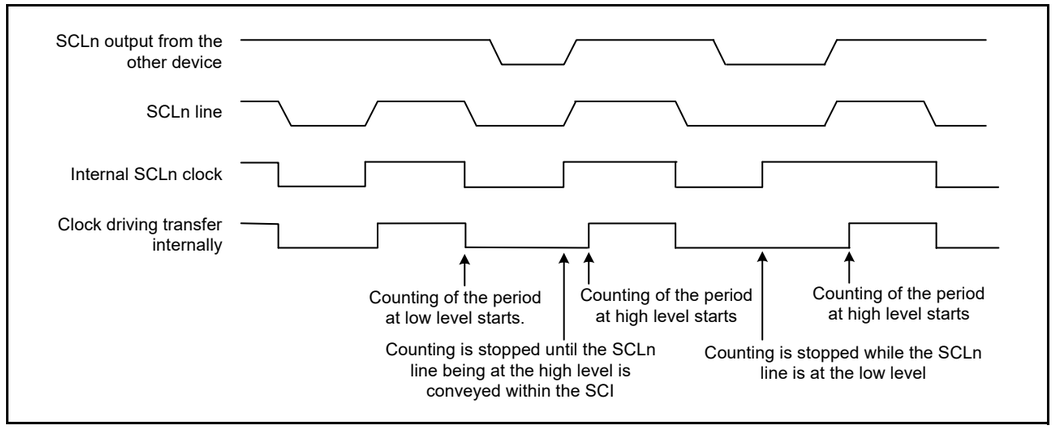


Figure 34.61 Example operations for clock synchronization

34.7.3 SDA Output Delay

The SIMR1.IICDL[4:0] bits can be used to set a delay for output on the SDAn pin relative to falling edges of output on the SCLn pin. Delay settings from 0 to 31 are selectable, representing periods of the corresponding numbers of cycles of the clock signal from the on-chip baud rate generator (derived by frequency-dividing the base clock, PCLKA, by the divisor selected in the SMR.CKS[1:0] bits). A delay for output on the SDAn pin applies to the start condition/restart condition/stop condition signal, 8-bit transmit data, and acknowledge bit.

If the SDA output delay is shorter than the time for the level on the SCLn pin to fall, the change of the output on the SDAn pin starts while the output level on the SCLn pin is falling, creating a possibility of erroneous operation for slave devices. Ensure that settings for the delay of output on the SDAn pin specify times greater than the time output on the SCLn pin takes to fall (300 ns for IIC in standard mode and fast mode).

Figure 34.62 shows the timing of delays in SDA output.

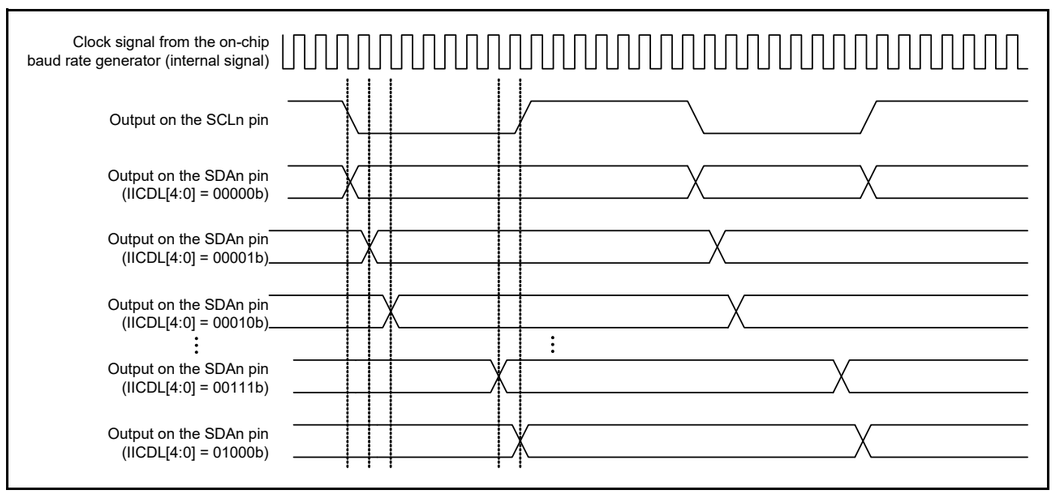


Figure 34.62 Timing of delays in SDA output

34.7.4 SCI Initialization in Simple IIC Mode

Before transferring data, write the initial value 00h to SCR and initialize the interface following the example shown in Figure 34.63.

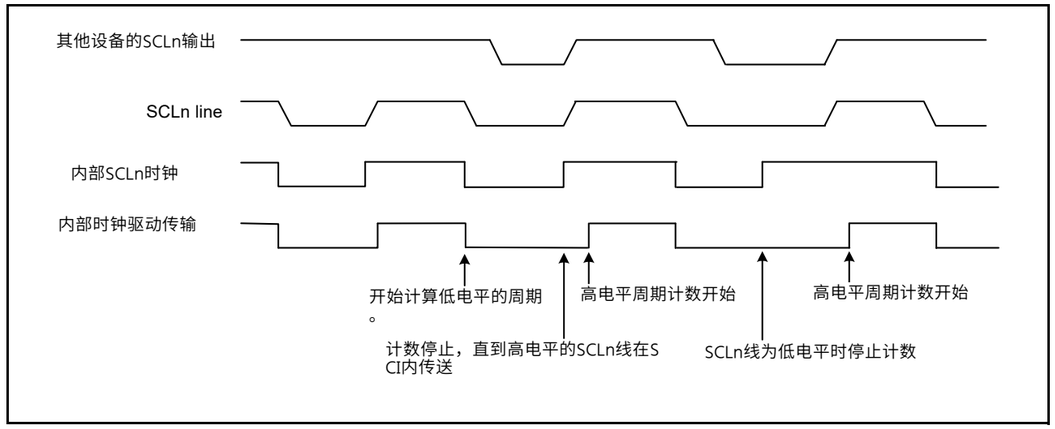


Figure 34.61 时钟同步的示例操作

34.7.3 SDA输出延迟

SIMR1.IICDL[4:0]位可用于设置SDAn引脚输出相对于SCLn引脚输出下降沿的延迟。可选择从0到31的延迟设置，表示来自片上波特率发生器的时钟信号的相应周期数的周期（通过将基本时钟PCLKA分频得到SMR.CKS中选择的除数）[1:0]位）。SDAn引脚上的输出延迟适用于启动条件重启条件停止条件信号、8位发送数据和确认位。

如果SDA输出延迟小于SCLn引脚电平下降的时间，则SDAn引脚在SCLn引脚上的输出电平下降时启动，从而为从设备产生错误操作的可能性。确保SDAn引脚上的输出延迟设置指定的时间大于SCLn引脚上输出的下降时间（标准模式和快速模式下的IIC为300ns）。

图34.62显示了SDA输出的延迟时间。

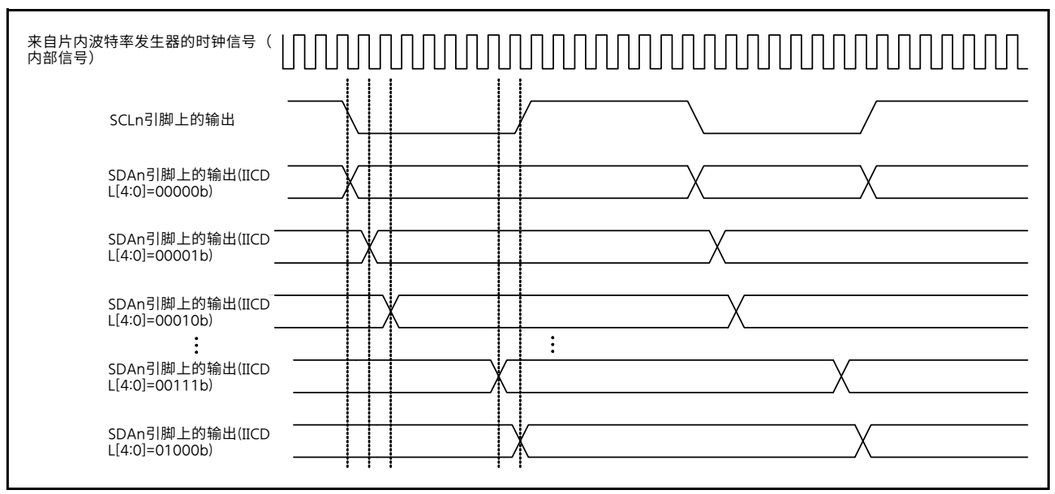


Figure 34.62 SDA输出的延迟时间

34.7.4 简单IIC模式下的SCI初始化

在传输数据之前，将初始值00h写入SCR并按照示例中的示例初始化接口
Figure 34.63.

Always set SCR to its initial value before making any changes to the operating mode or transfer format.

In simple IIC mode, the open-drain setting for the communication ports should be made on the port side.

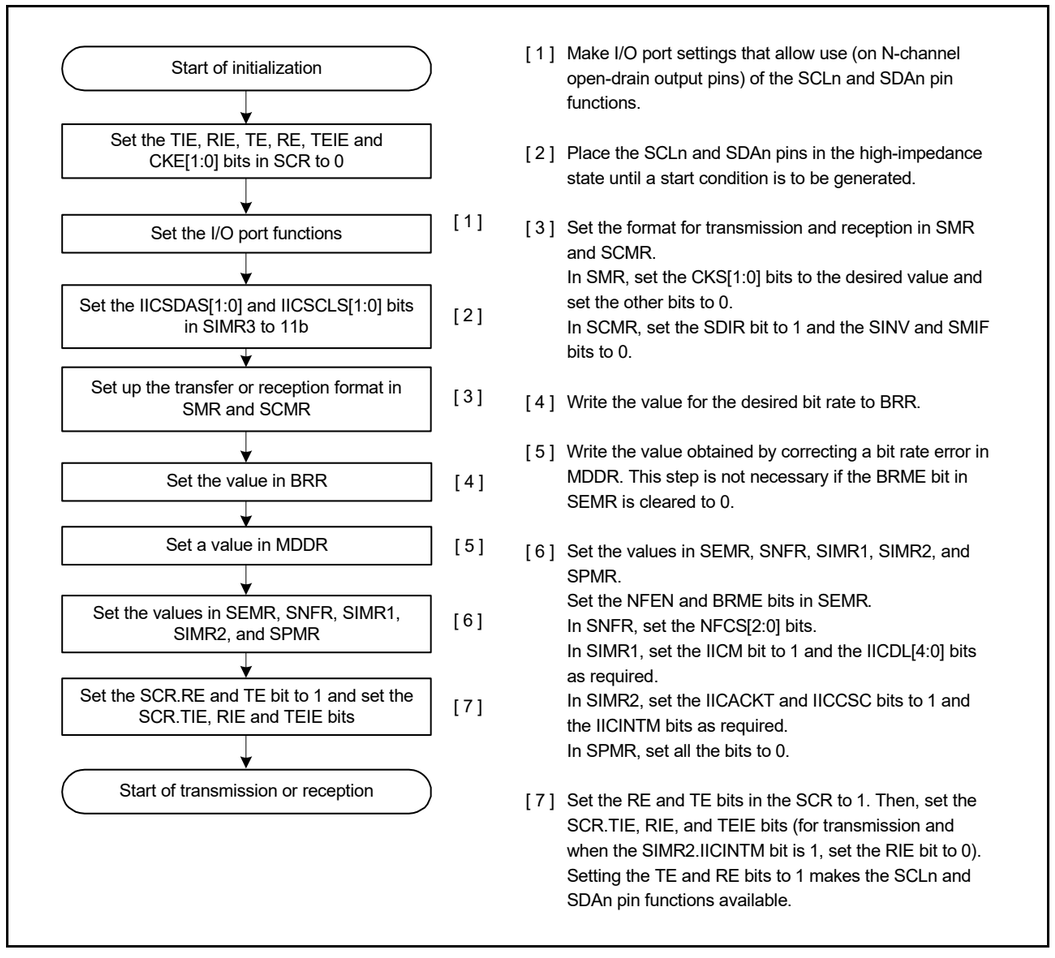


Figure 34.63 Example flow of SCI initialization in simple IIC mode

34.7.5 Operation in Master Transmission in Simple IIC Mode

Figure 34.64 and Figure 34.65 show examples of master transmission and Figure 34.66 shows an example flow of data transmission. The value of the SIMR2.IICINTM bit is assumed to be 1 (use reception and transmission interrupts) and the value of the SCR.RIE bit is assumed to be 0 (SCIn_RXI and SCIn_ERI interrupt requests are disabled). See Table 34.29 for more information on the STI interrupt.

When 10-bit slave addresses are in use, steps [3] and [4] in Figure 34.66 are repeated twice.

In simple IIC mode, the transmit data empty interrupt (SCIn_TXI) is generated when communication of one frame is complete, unlike the SCIn_TXI interrupt request generation timing during clock synchronous transmission.

在对操作模式或传输格式进行任何更改之前，始终将SCR设置为其初始值。

在简单IIC模式下，通信端口的开漏设置应在端口侧进行。

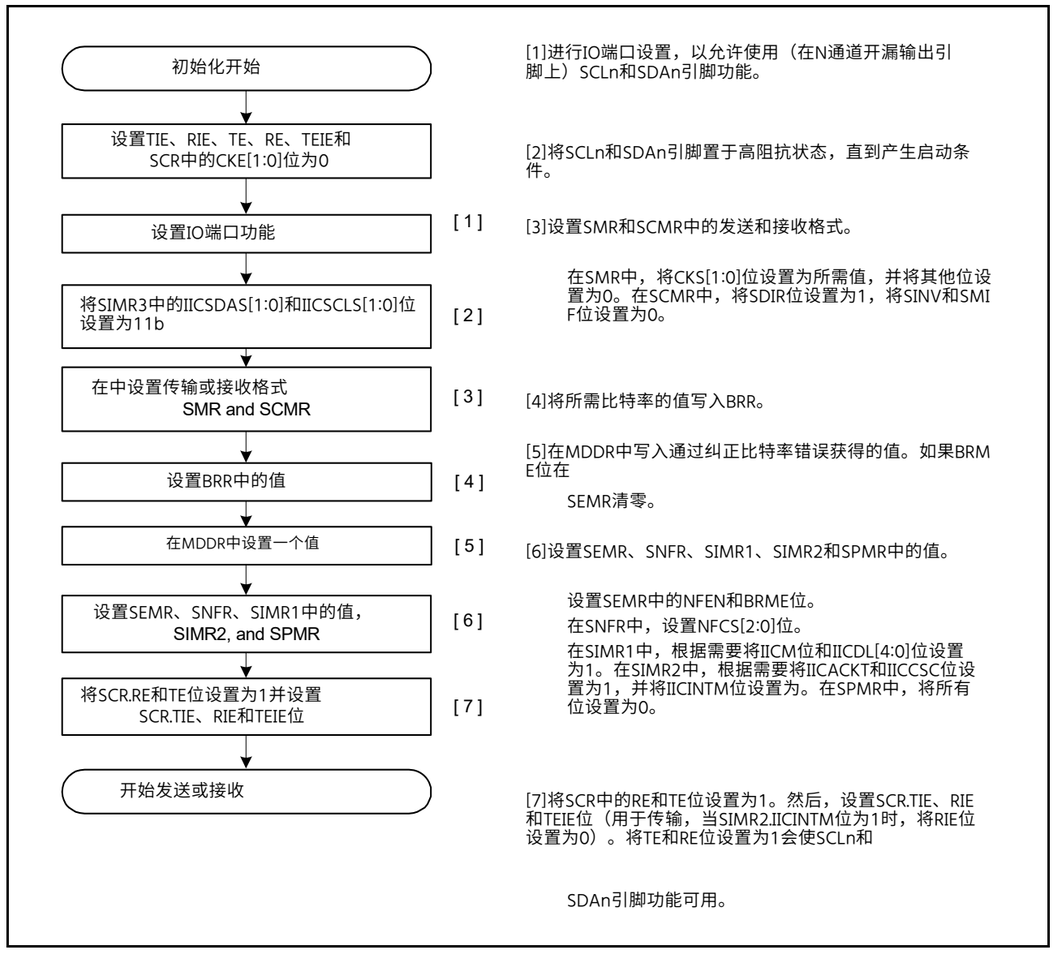


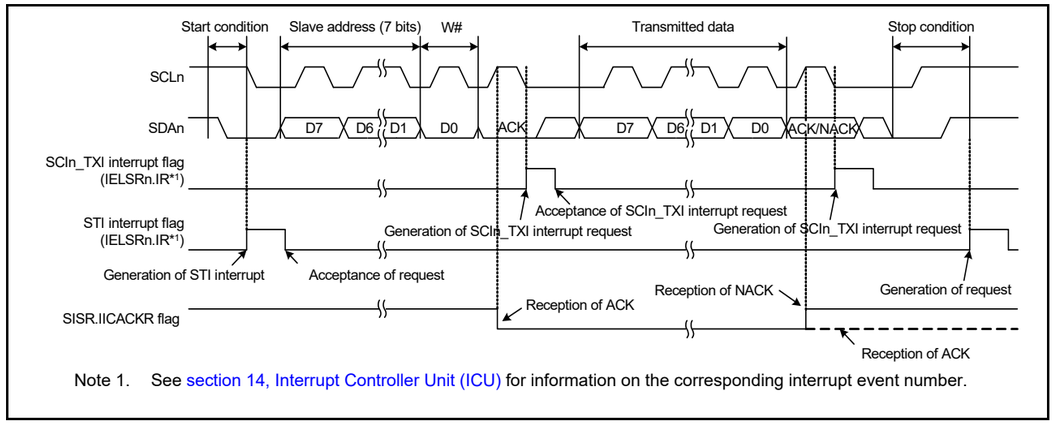
Figure 34.63 简单IIC模式下SCI初始化示例流程

34.7.5 简单IIC模式下的主传输操作

图34.64和图34.65显示了主传输的示例，图34.66显示了数据传输的示例流程。SIMR2.IICINTM位的值假定为1（使用接收和发送中断），SCR.RIE位的值假定为0（SCIn_RXI和SCIn_ERI中断请求被禁用）。有关STI中断的更多信息，请参见表34.29。

当使用10位从地址时，图34.66中的步骤[3]和[4]重复两次。

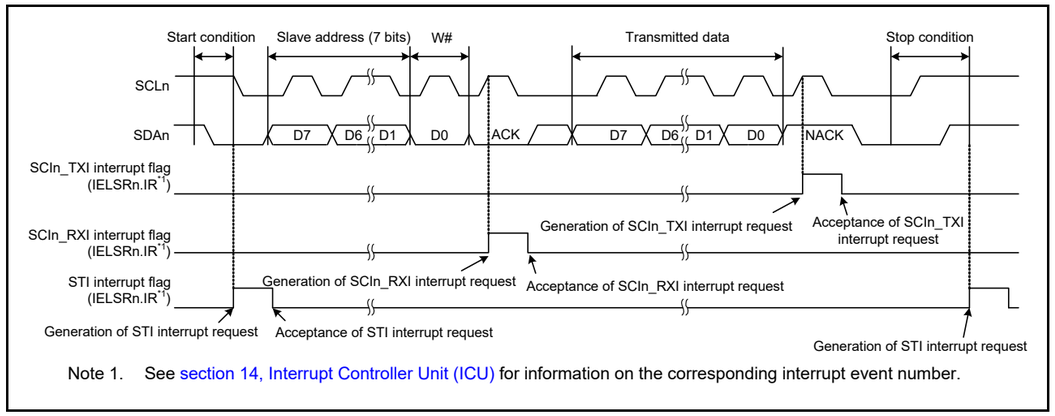
在简单IIC模式下，发送数据空中断(SCIn_TXI)是在一帧通信完成时产生的，与时钟同步传输期间的SCIn_TXI中断请求产生时序不同。



Note 1. See section 14, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

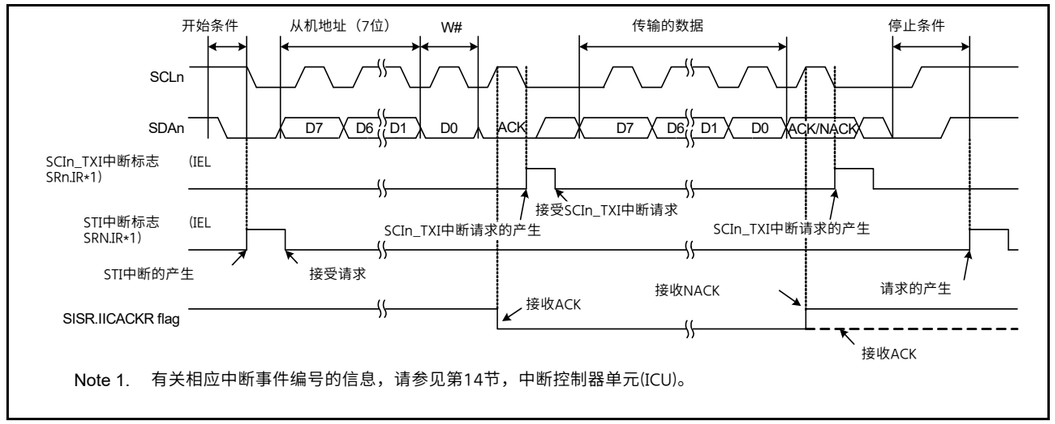
Figure 34.64 Example 1 of operations for master transmission in simple IIC mode with 7-bit slave addresses, transmission interrupts, and reception interrupts

When the SIMR2.IICINTM bit is set to 0 (use ACK/NACK interrupts) during master transmission, the DTC or DMAC is activated by the ACK interrupt as the trigger and required number of data bytes are transmitted. When the NACK is received, error processing such as transmission stop and retransmission is performed using the NACK interrupt as the trigger.



Note 1. See section 14, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

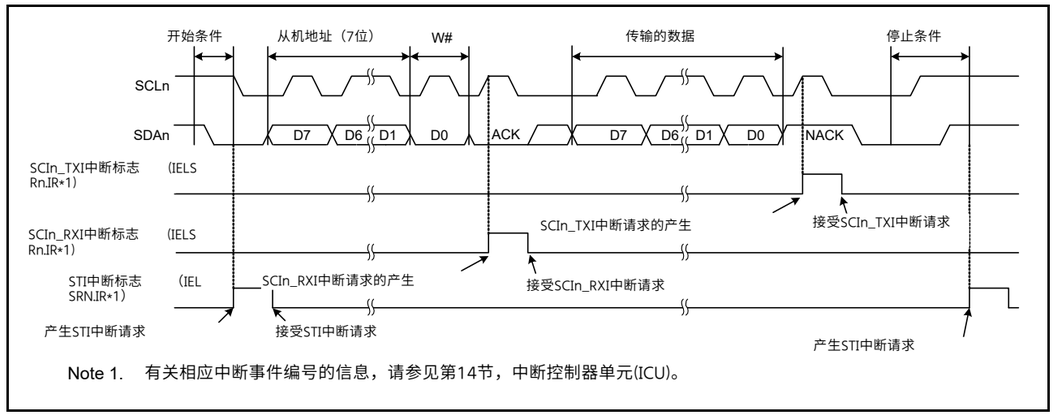
Figure 34.65 Example 2 of operations for master transmission in simple IIC mode with 7-bit slave addresses, ACK interrupts, and NACK interrupts



Note 1. 有关相应中断事件编号的信息，请参见第14节，中断控制器单元(ICU)。

Figure 34.64 简单IIC模式下主机发送操作示例1，具有7位从机地址、发送中断和接收中断

当在主机传输期间SIMR2.IICINTM位设置为0（使用ACKNACK中断）时，DTC或DMAC由ACK中断作为触发器激活并传输所需的数据字节数。接收到NACK时，以NACK中断为触发进行发送停止、重发等错误处理。



Note 1. 有关相应中断事件编号的信息，请参见第14节，中断控制器单元(ICU)。

Figure 34.65 使用7位从机地址的简单IIC模式下主机传输操作示例2，ACK中断和NACK中断

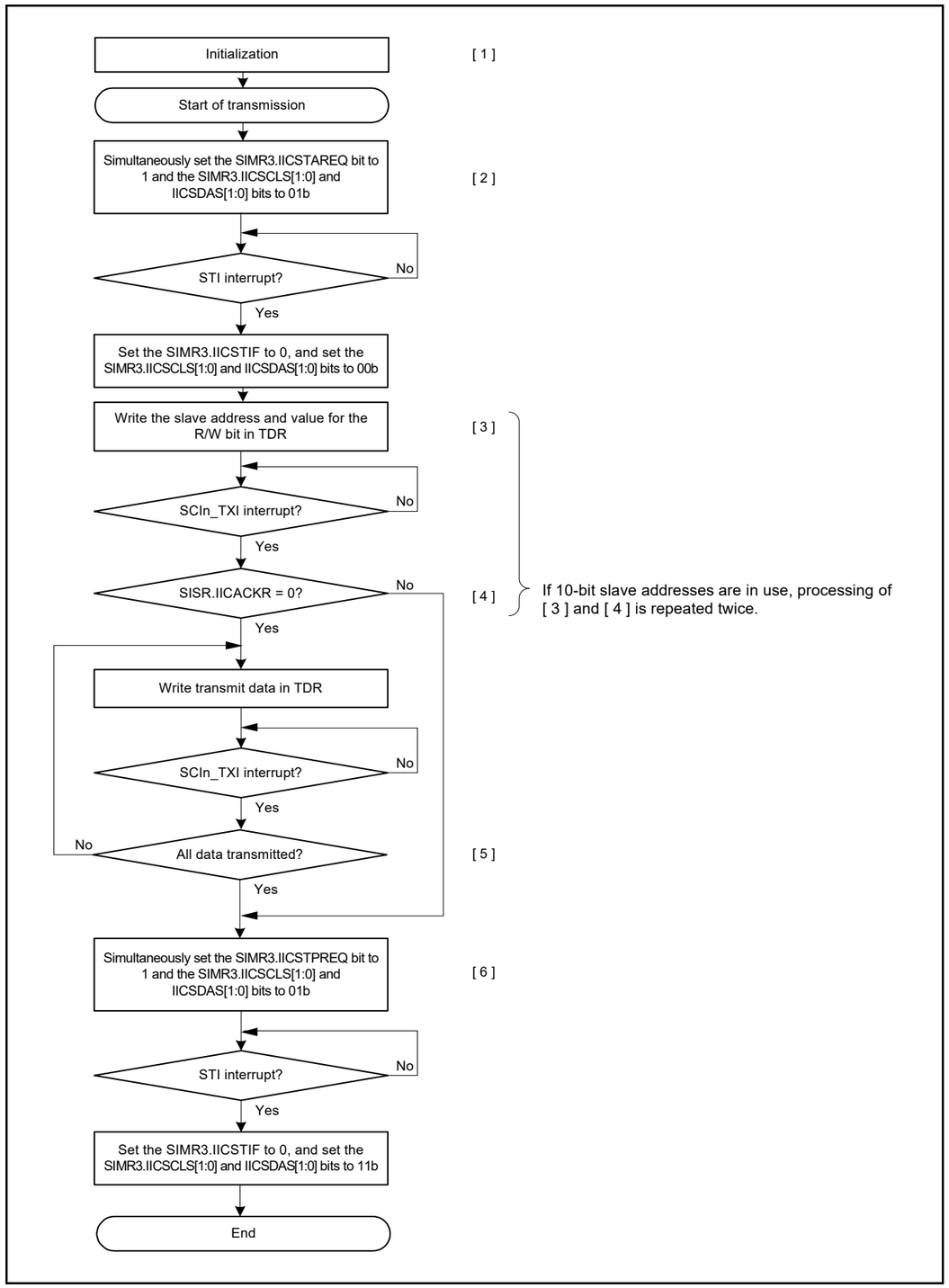


Figure 34.66 Example flow of master transmission in simple IIC mode with transmission interrupts and reception interrupts

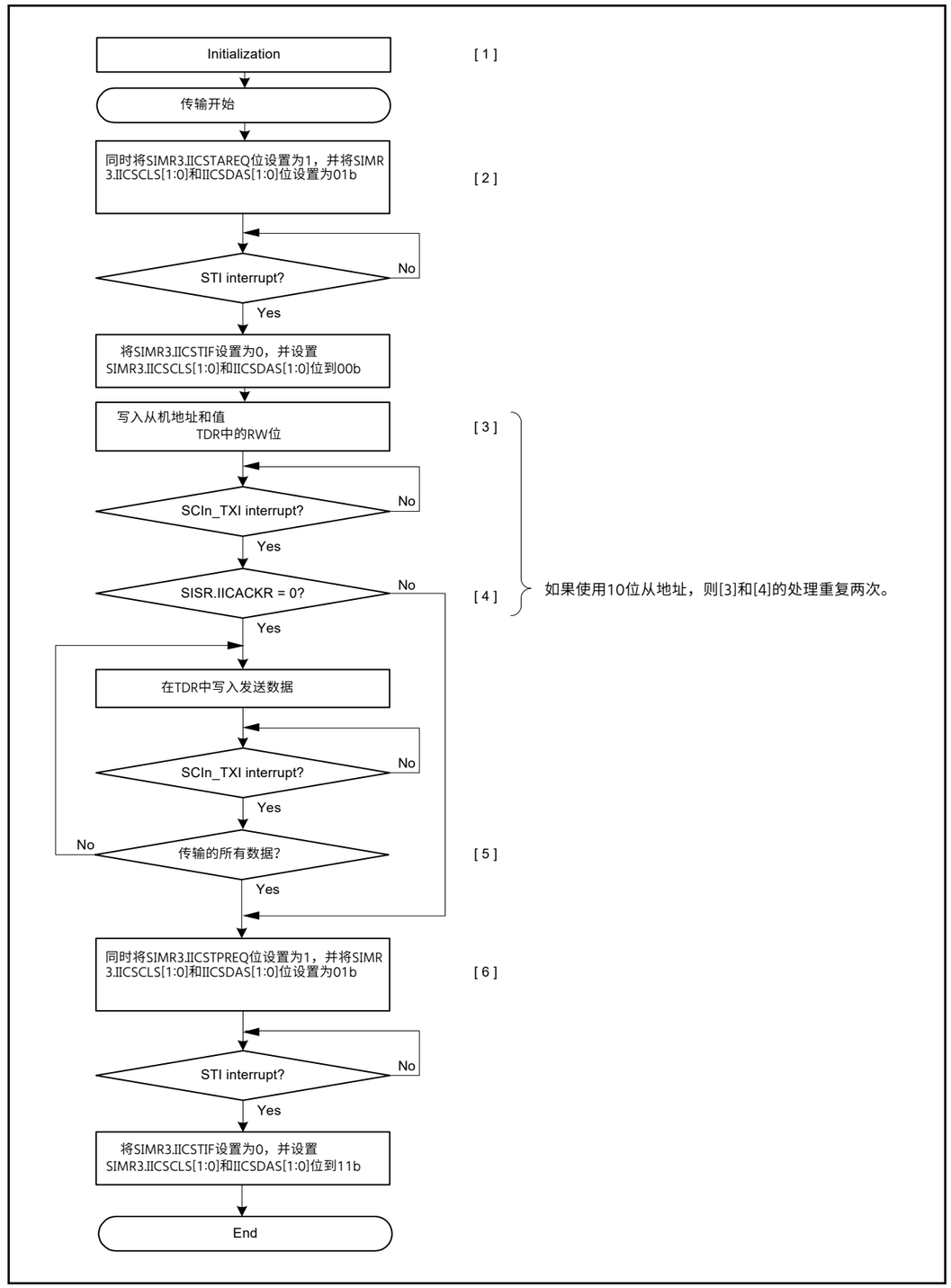


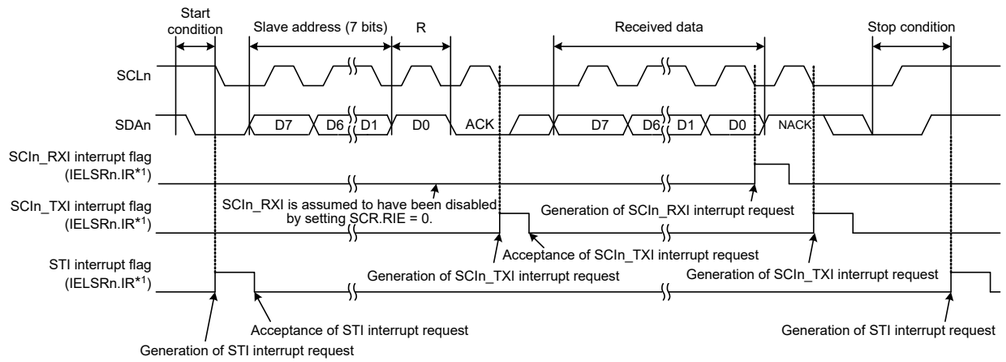
Figure 34.66 带有发送中断和接收中断的简单IIC模式下的主机发送示例流程

34.7.6 Master Reception in Simple IIC Mode

Figure 34.67 shows an example operation in simple IIC mode master reception and Figure 34.68 shows an example flow of master reception.

The value of the SIMR2.IICINTM bit is assumed to be 1 (use reception and transmission interrupts).

In simple IIC mode, the transmit data empty interrupt (SCIn_TXI) is generated when communication of one frame is complete, unlike the SCIn_TXI interrupt request generation timing during clock synchronous transmission.



Note 1. See section 14, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

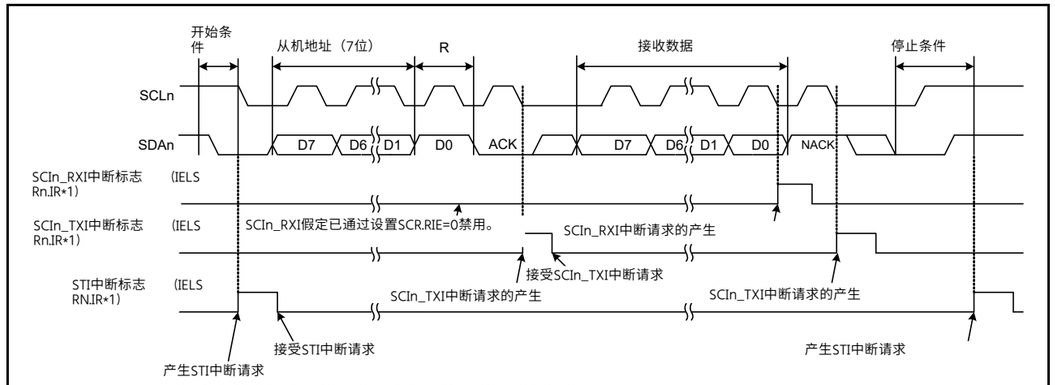
Figure 34.67 Example operations for master reception in simple IIC mode with 7-bit slave addresses, transmission interrupts, and reception interrupts

34.7.6 简单IIC模式下的主接收

图34.67显示了简单IIC模式主机接收的示例操作，图34.68显示了主机接收的示例流程。

SIMR2.IICINTM位的值假定为1（使用接收和发送中断）。

在简单IIC模式下，发送数据空中断(SCIn_TXI)是在一帧通信完成时产生的，与时钟同步传输期间的SCIn_TXI中断请求产生时序不同。



Note 1. 有关相应中断事件编号的信息，请参见第14节，中断控制器单元(ICU)。

Figure 34.67 使用7位从地址、发送中断和接收中断的简单IIC模式下的主机接收示例操作

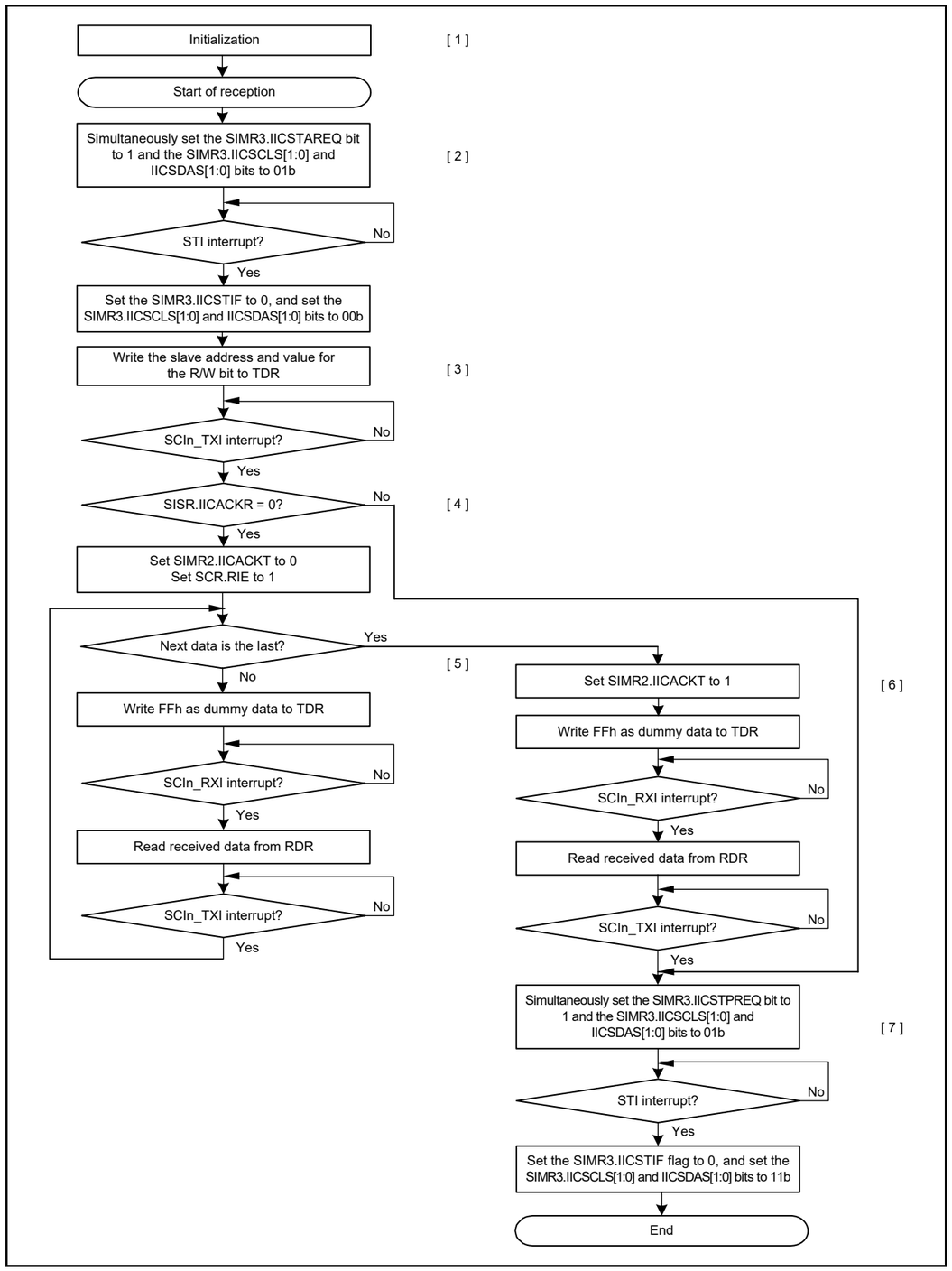


Figure 34.68 Example flow of master reception in simple IIC mode with transmission interrupts and reception interrupts

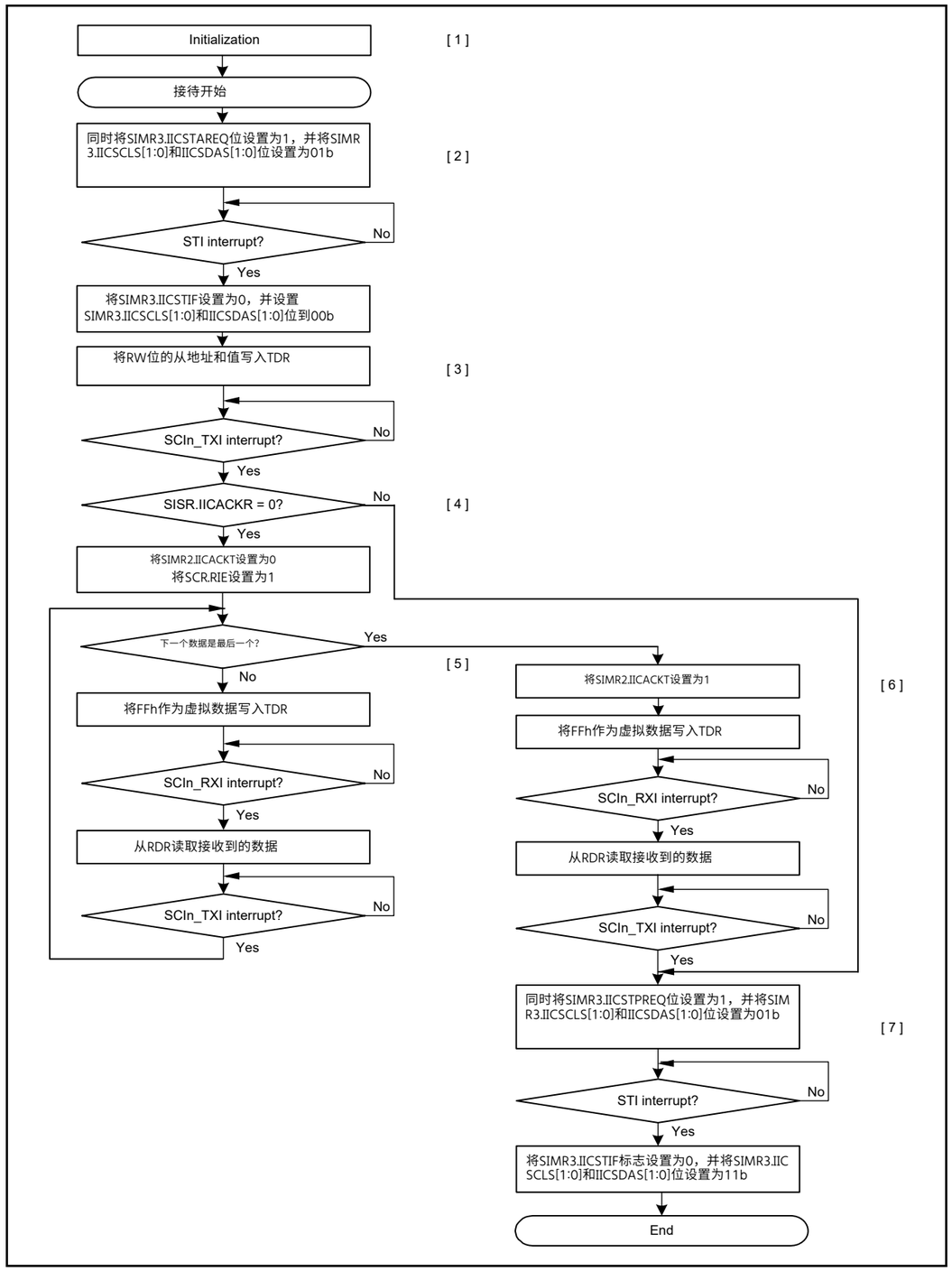


Figure 34.68 带有发送中断和接收中断的简单IIC模式下的主机接收示例流程

34.8 Operation in Simple SPI Mode

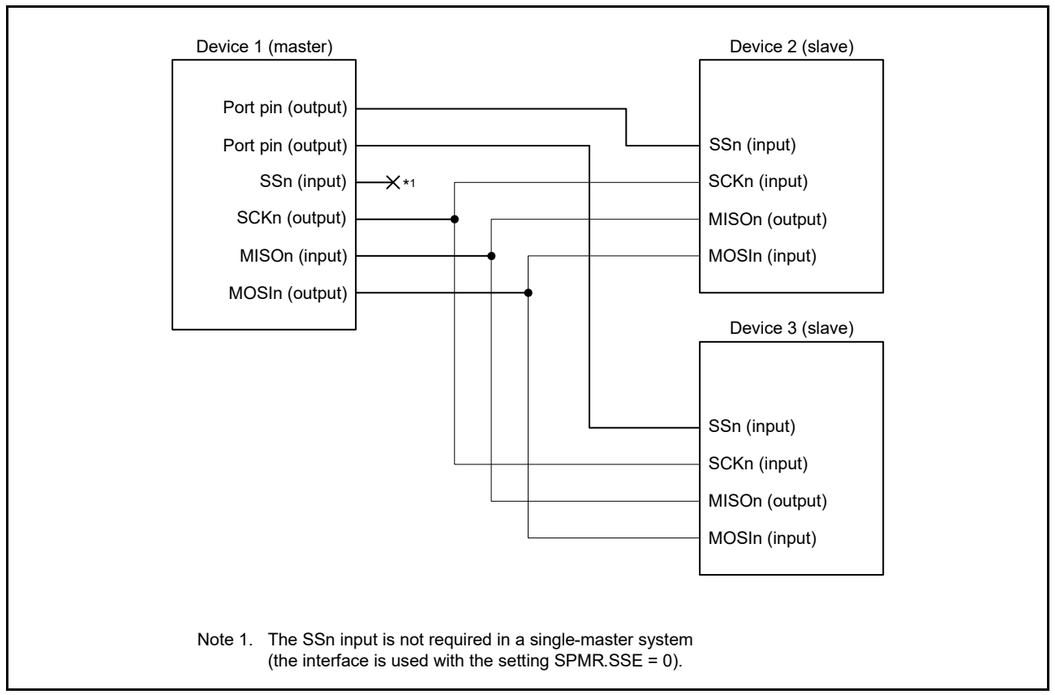
As an extended function, the SCI supports a simple SPI mode that handles transfer among one or multiple master devices and multiple slave devices.

Using the settings for clock synchronous mode (SCMR.SMIF = 0, SIMR1.IICM = 0, SMR.CM = 1) and setting the SPMR.SSE bit to 1 places the SCI in simple SPI mode. However, the SSn pin function on the master side is not required for connection of the device used as the master in simple SPI mode when the configuration only has a single master. Therefore, set the SPMR.SSE bit to 0 in such cases.

Figure 34.69 shows an example of connections for simple SPI mode. Control a general port pin to produce the SSn output signal from the master.

In simple SPI mode, data is transferred in synchronization with clock pulses in the same way as in clock synchronous mode. One character of data for transfer consists of 8 bits of data, and parity bits cannot be appended. The data can be inverted by setting the SCMR.SINV bit to 1.

Because the receiver and transmitter are independent of each other within the SCI module, full-duplex communications are possible, with a shared clock signal. Additionally, because both the transmitter and receiver have a buffered structure, writing the next transmit data while transmission is in progress and reading previously received data while reception is in progress are both possible. This enables continuous transfer.



Note 1. The SSn input is not required in a single-master system (the interface is used with the setting SPMR.SSE = 0).

Figure 34.69 Example connections using simple SPI mode in single master mode with SPMR.SSE bit = 0

34.8.1 States of Pins in Master and Slave Modes

The direction (input or output) of pins for the simple SPI mode interface differs according to whether the device is a master (SCR.CKE[1:0] = 00b or 01b and SPMR.MSS = 0) or slave (SCR.CKE[1:0] = 10b or 11b and SPMR.MSS = 1).

Table 34.25 lists the relationship between the pin states, mode, and level on the SSn pin.

34.8 简单SPI模式下的操作

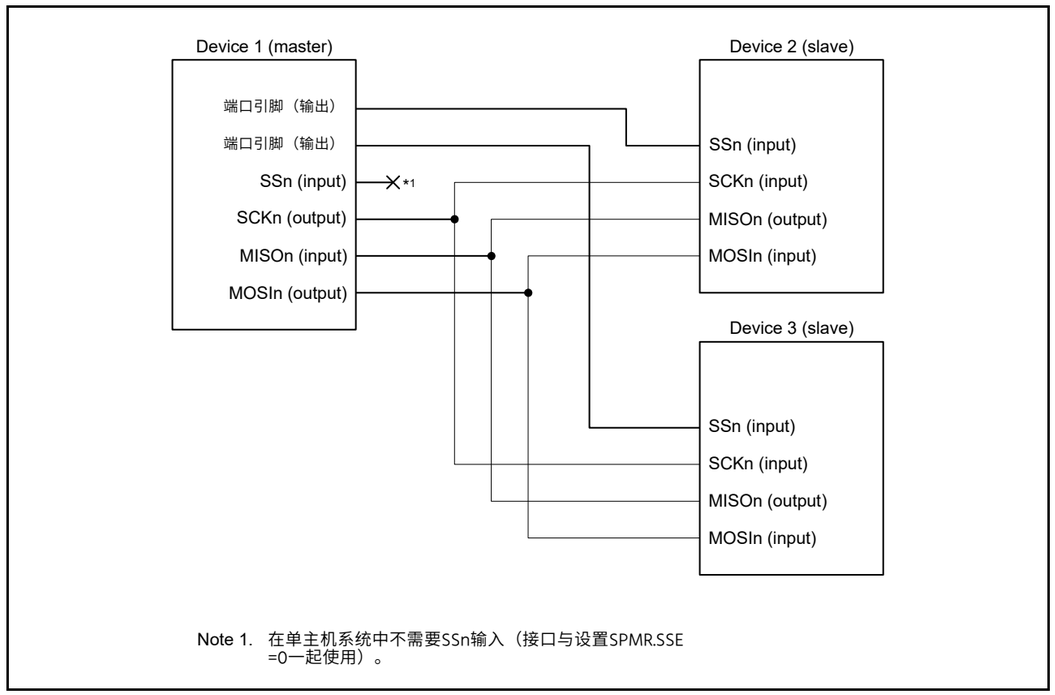
作为一项扩展功能，SCI支持简单的SPI模式，可处理一个或多个主设备与多个从设备之间的传输。

使用时钟同步模式的设置（SCMR.SMIF=0，SIMR1.IICM=0，SMR.CM=1）并将SPMR.SSE位设置为1将SCI置于简单SPI模式。但是，当配置只有一个主控时，在简单SPI模式下连接用作主控的设备不需要主控侧的SSn引脚功能。因此，在这种情况下，将SPMR.SSE位设置为0。

图34.69显示了简单SPI模式的连接示例。控制一个通用端口引脚以产生来自主机的SSn输出信号。

在简单SPI模式下，数据与时钟脉冲同步传输，方式与时钟同步模式相同。1个字符的传输数据由8位数据组成，不能附加奇偶校验位。可以通过将SCMR.SINV位设置为1来反转数据。

由于接收器和发送器在SCI模块中彼此独立，因此可以使用共享时钟信号进行全双工通信。此外，由于发送器和接收器都具有缓冲结构，因此在发送过程中写入下一个发送数据和在接收过程中读取先前接收到的数据都是可能的。这使得连续传输成为可能。



Note 1. 在单主机系统中不需要SSn输入（接口与设置SPMR.SSE=0一起使用）。

Figure 34.69 在SPMR.SSE位=0的单主模式下使用简单SPI模式的示例连接

34.8.1 主从模式下的引脚状态

简单SPI模式接口的引脚方向（输入或输出）根据设备是主设备（SCR.CKE[1:0]=00b或01b且SPMR.MSS=0）还是从设备（SCR.CKE）而不同[1:0]=10b或11b且SPMR.MSS=1)。

表34.25列出了SSn引脚上的引脚状态、模式和电平之间的关系。

Table 34.25 States of pins by mode and input level on SSn pin

Mode	Input on SSn pin	State of TXDn pin	State of RXDn pin	State of SCKn pin
Master mode*1	High level (transfer can proceed)	Output for data transmission*2	Input for received data	Clock output*3
	Low level (transfer cannot proceed)	High-impedance	Input for received data (but disabled)	High-impedance
Slave mode	High level (transfer cannot proceed)	Input for received data (but disabled)	High-impedance	Clock input (but disabled)
	Low level (transfer can proceed)	Input for received data	Output for data transmission	Clock input

Note 1. When there is only a single master (SPMR.SSE = 0), transfer is possible regardless of the input level on the SSn pin. This is equivalent to input of a high level on the SSn pin. Because the SSn pin function is not required, the pin is available for other purposes.
Note 2. The MOSIn pin output is in the high-impedance state when serial transmission is disabled (SCR.TE bit = 0).
Note 3. The SCKn pin output is in the high-impedance state when serial transmission is disabled (SCR.TE and RE bits = 00b) in a multi-master configuration (SPMR.SSE = 1).

34.8.2 SS Function in Master Mode

Setting the SCR.CKE[1:0] bits to 00b and the SPMR.MSS bit to 0 selects master operation.

In single-master configurations (SPMR.SSE = 0), the SSn pin is not used, and so transmission or reception can proceed regardless of the value of the SSn pin.

When the level on the SSn pin is high in a multi-master configuration (SPMR.SSE = 1), a master device outputs clock signals from the SCKn pin before starting transmission or reception to indicate that there are no other masters or another master is performing reception or transmission.

When the level on the SSn pin is low in a multi-master configuration (SPMR.SSE = 1), there are other masters, and this indicates that transmission or reception is in progress. The MOSIn output and SCKn pins are placed in the high-impedance state and starting transmission or reception is not possible. Additionally, the value of the SPMR.MFF bit is 1, indicating a mode fault error. In a multi-master configuration, start error processing by reading SPMR.MFF flag. Even if a mode fault error occurs while transmission or reception is in progress, transmission or reception does not stop, but the MOSIn and SCKn pin outputs are placed in the high-impedance state after completion of the transfer. Use a general port pin to produce the SS output signal from the master.

34.8.3 SS Function in Slave Mode

Setting the SCR.CKE[1:0] bits to 10b and the SPMR.MSS bit to 1 selects slave operation. When the SSn pin is high, the MISOn output pin is in the high-impedance state and clock input through the SCKn pin is ignored. When the SSn pin is low, clock input through the SCKn pin is valid and transmission or reception can proceed.

If the input on the SSn pin changes from low to high during transmission or reception, the MISOn output pin is placed in the high-impedance state. Meanwhile, the internal processing for transmission or reception continues at the rate of the clock input through the SCKn pin until processing for the character being transmitted or received is complete, after which it stops, and the appropriate interrupt (SCIn_TXI, SCIn_RXI, or SCIn_TEI) is generated.

34.8.4 Relationship between Clock and Transmit/Receive Data

The CKPOL and CKPH bits in the SPMR register can be used to set up the clock for use in transmission and reception in four different ways. The relation between the clock signal and the transmission and reception of data is shown in Figure 34.70. The relation is the same for both master and slave operation. This is the same as when the level on the SSn pin is high.

Table 34.25 SSn引脚上的模式和输入电平的引脚状态

Mode	SSn引脚上的输入	TXDn引脚状态	RXDn引脚状态	SCKn引脚状态
Master mode*1	高电平（可以进行转移）	数据传输输出*2	接收数据的输入	Clock output*3
	低电平（传输无法进行）	High-impedance	接收数据的输入（但禁用）	High-impedance
从机模式	高电平（传输无法进行）	接收数据的输入（但禁用）	High-impedance	时钟输入（但禁用）
	低电平（可以继续传输）	接收数据的输入	数据传输输出	时钟输入

注1.当只有一个主机(SPMR.SSE=0)时，无论SSn引脚上的输入电平如何，都可以进行传输。这相当于在SSn引脚上输入高电平。由于不需要SSn引脚功能，因此该引脚可用于其他用途。注2.当串行传输被禁用（SCR.TE位=0）时，MOSIn引脚输出处于高阻抗状态。

注3.在多主机配置(SPMR.SSE=1)中禁用串行传输(SCR.TE和RE位=00b)时，SCKn引脚输出处于高阻抗状态。

34.8.2 主控模式下的SS功能

将SCR.CKE[1:0]位设置为00b并将SPMR.MSS位设置为0选择主机操作。

在单主机配置(SPMR.SSE=0)中，不使用SSn引脚，因此无论SSn引脚的值如何，都可以进行发送或接收。

在多主机配置（SPMR.SSE=1）中，当SSn引脚上的电平为高电平时，主机设备在开始发送或接收之前从SCKn引脚输出时钟信号，以指示没有其他主机或另一个主机在进行接收或发送。

在多主机配置中（SPMR.SSE=1），当SSn引脚上的电平为低电平时，还有其他主机，这表明正在发送或接收。MOSIn输出和SCKn引脚处于高阻抗状态，无法开始发送或接收。此外，SPMR.MFF位的值为1，表示模式故障错误。在多主机配置中，通过读取SPMR.MFF标志开始错误处理。即使在发送或接收过程中发生模式故障错误，发送或接收也不会停止，而是在传输完成后将MOSIn和SCKn引脚输出置于高阻抗状态。使用通用端口引脚从主机产生SS输出信号。

34.8.3 从模式下的SS功能

将SCR.CKE[1:0]位设置为10b并将SPMR.MSS位设置为1选择从机操作。当SSn引脚为高电平时，MIOn输出引脚处于高阻状态，通过SCKn引脚输入的时钟被忽略。当SSn引脚为低电平时，通过SCKn引脚输入的时钟有效，可以进行发送或接收。

如果SSn引脚上的输入在发送或接收期间从低电平变为高电平，则MISOn输出引脚处于高阻抗状态。同时，发送或接收的内部处理以通过SCKn引脚输入的时钟速率继续进行，直到对正在发送或接收的字符的处理完成，之后它停止，并出现适当的中断（SCIn_TXI、SCIn_RXI或SCIn_TEI）生成。

34.8.4 时钟与发送接收数据的关系

SPMR寄存器中的CKPOL和CKPH位可用于以四种不同的方式设置用于发送和接收的时钟。时钟信号与数据收发的关系如图34.70所示。主从操作的关系是相同的。这与SSn引脚上的电平为高电平时相同。

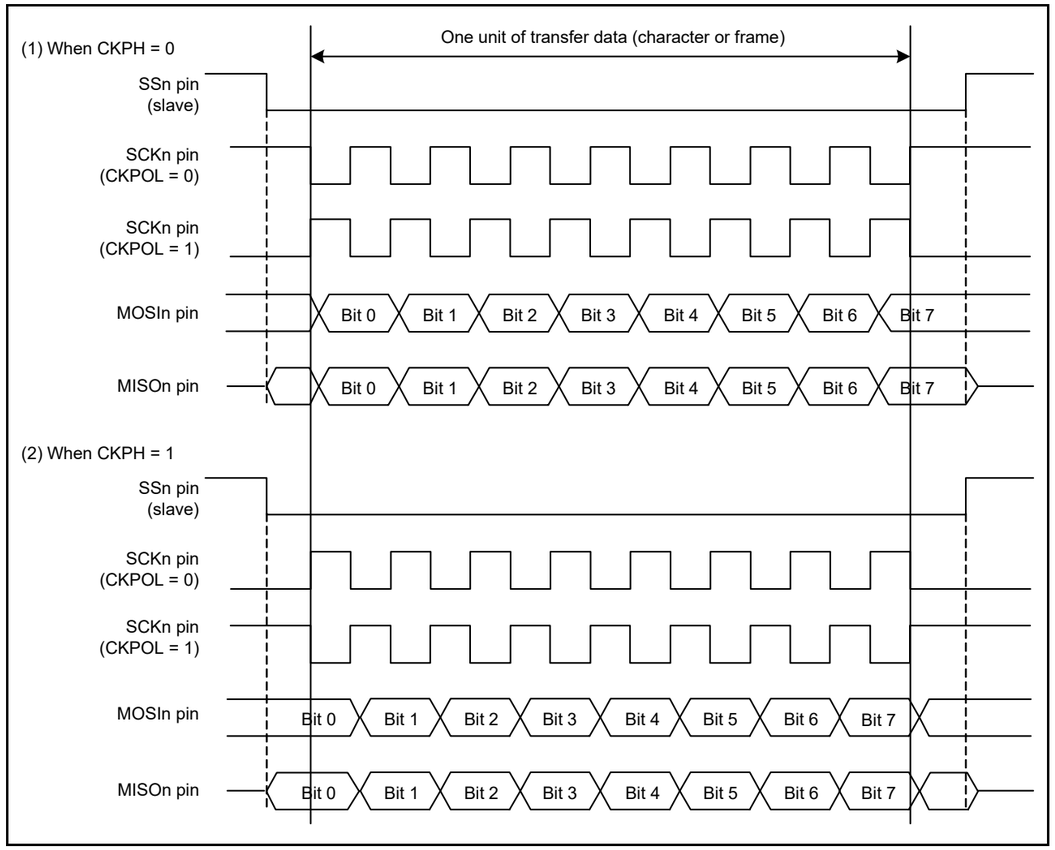


Figure 34.70 Relation between clock signal and transmit or receive data in simple SPI mode

34.8.5 SCI Initialization in Simple SPI Mode

Initialization in simple SPI mode is the same as in clock synchronous mode. See Figure 34.32 for an example initialization flow. The CKPOL and CKPH bits in the SPMR register must be set to ensure that the clock signal is suitable for both master and slave devices.

Always initialize the SCR register before making any changes to the operating mode or transfer format.

Note 1. Only the RE bit is set to 0. The SSR.ORER, FER, PER, and RDR flags are not initialized.
Note 2. Changing the value of the TE bit from 1 to 0 or from 0 to 1 leads to the generation of a transmit data empty interrupt (SCIn_TXI) if the value of the SCR.TIE bit is 1.

34.8.6 Transmission and Reception of Serial Data in Simple SPI Mode

In master operation, ensure that the SSn pin of the slave device on the other side of the transfer is at the low level before starting the transfer and at the high level on completion of the transfer. Otherwise, the procedures are the same as in clock synchronous mode.

34.9 Bit Rate Modulation Function

Using the bit rate modulation function, the bit rate can be evenly corrected using the number specified in the MDDR register when the PCLKA is selected in the CKS[1:0] bits in SMR/SMR_SMCI.

Figure 34.71 shows an example where the PCLKA is selected in the CKS[1:0] bits in SMR/SMR_SMCI, the BRR bit is set to 0, and the MDDR is set to 160 in asynchronous mode. In this example, the cycle of the base clock is evenly

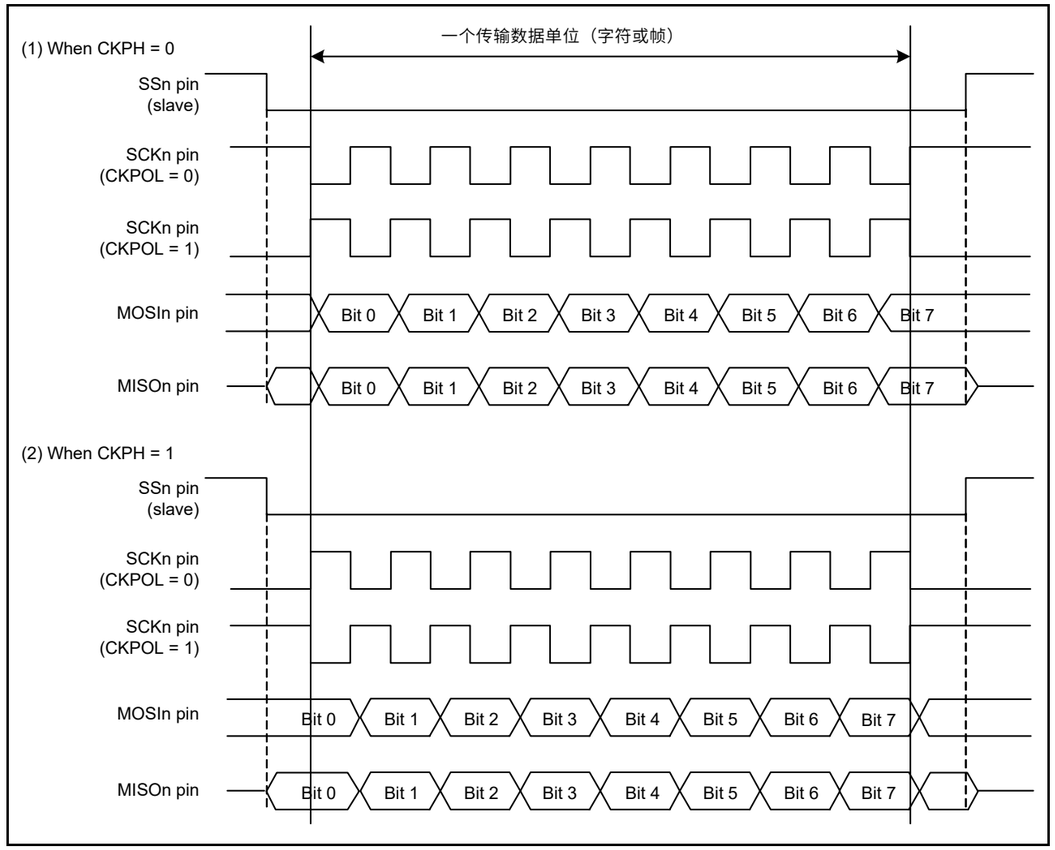


Figure 34.70 简单SPI模式下时钟信号与发送或接收数据的关系

34.8.5 简单SPI模式下的SCI初始化

简单SPI模式的初始化与时钟同步模式相同。有关示例初始化流程，请参见图34.32。必须设置SPMR寄存器中的CKPOL和CKPH位，以确保时钟信号适用于主设备和从设备。

在对操作模式或传输格式进行任何更改之前，始终初始化SCR寄存器。

注1.只有RE位设置为0。SSR.ORER、FER、PER和RDR标志未初始化。
注2.如果SCR.TIE位的值为1，则将TE位的值从1更改为0或从0更改为1会导致产生发送数据空中断(SCIn_TXI)。

34.8.6 简单SPI模式下串行数据的发送和接收

在主机操作中，确保传输另一侧的从设备的SSn管脚在开始传输前为低电平，在传输完成时为高电平。否则，过程与时钟同步模式相同。

34.9 比特率调制功能

使用比特率调制功能，当在SMRSMR_SMCI的CKS[1:0]位中选择PCLKA时，可以使用MDDR寄存器中指定的数字均匀地校正比特率。

图34.71显示了一个示例，其中在SMRSMR_SMCI的CKS[1:0]位中选择PCLKA，BRR位设置为0，异步模式下MDDR设置为160。在这个例子中，基本时钟的周期是均匀的

corrected (256/160) and the bit rate is also corrected (160/256).

Note: Enabling an internal clock causes bias, and expansion and contraction are generated in the pulse width of the internal base clock.

Do not use this function in clock synchronous mode and in the highest speed settings in simple SPI mode (SMR.CKS[1:0] = 00b, SCR.CKE[1] = 0, and BRR = 0).

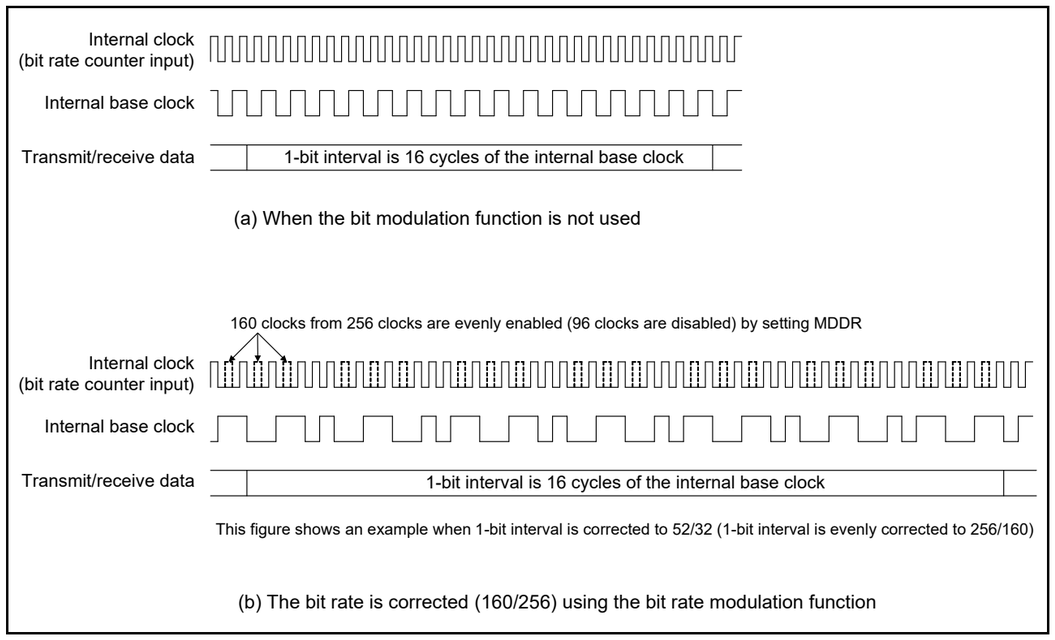


Figure 34.71 Example internal base clock when bit rate modulation function is used

34.10 Interrupt Sources

34.10.1 Buffer Operation for SCIn_TXI and SCIn_RXI Interrupts (non-FIFO selected)

If the conditions for an SCIn_TXI and SCIn_RXI interrupt are satisfied while the interrupt status flag in the Interrupt Controller Unit (ICU) is 1, the ICU does not output the interrupt request but retains it internally (with a capacity for retention of one request per source).

When the interrupt status flag in the ICU is set to 0, the interrupt request retained within the ICU is output. The internally retained interrupt request is automatically discarded when the actual interrupt is output. Clearing of the associated interrupt enable bit (the TIE or RIE bit in the SCR/SCR_SMCI) can also be used to discard an internally retained interrupt request.

34.10.2 Buffer Operation for SCIn_TXI and SCIn_RXI Interrupts (FIFO selected)

Even when an interrupt status flag in the ICU is set to 1, the SCIn_TXI and SCIn_RXI interrupts do not output interrupt requests to the ICU. When an interrupt status flag of the ICU is cleared to 0, and if the conditions for an SCIn_TXI and SCIn_RXI interrupts are satisfied, an interrupt request is generated.

34.10.3 Interrupts in Asynchronous, Clock Synchronous, and Simple SPI Modes

(1) Non-FIFO selected

Table 34.26 lists interrupt sources in asynchronous mode, clock synchronous mode, and simple SPI mode. A different interrupt vector can be assigned to each interrupt source. Individual interrupt sources can be enabled or disabled with the

更正（256160）并且比特率也被更正（160256）。

Note: 启用内部时钟会导致偏差，并且会在内部基本时钟的脉冲宽度中产生扩展和收缩。

不要在时钟同步模式和简单SPI模式的最高速度设置（SMR.CKS[1:0]=00b，SCR.CKE[1]=0和BRR=0）中使用此功能。

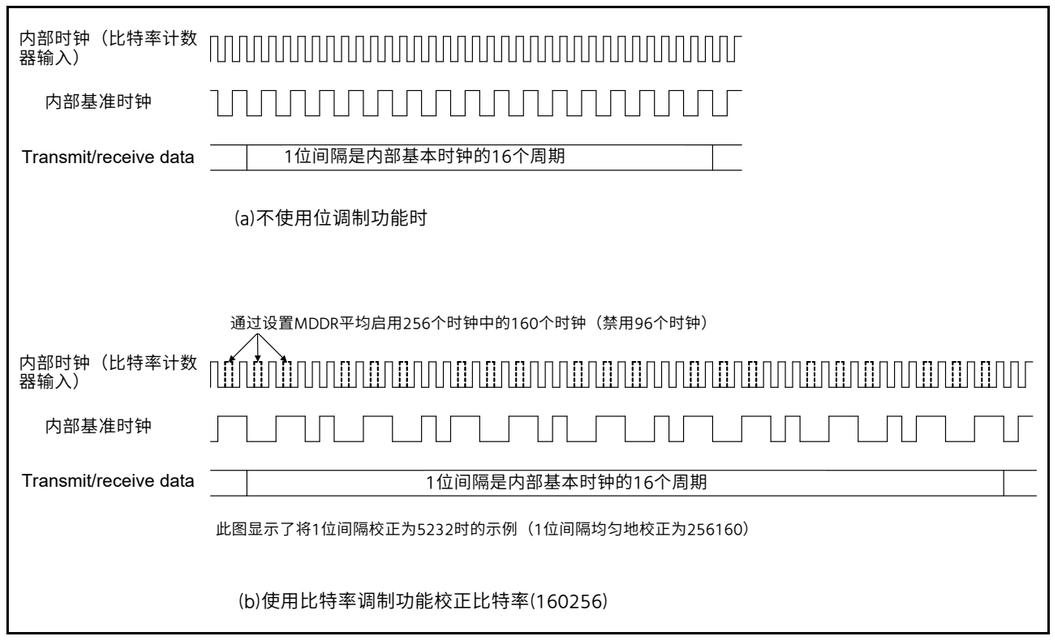


Figure 34.71 使用比特率调制功能时的内部基准时钟示例

34.10 中断源

34.10.1 SCIn_TXI和SCIn_RXI中断的缓冲区操作（选择非FIFO）

如果满足SCIn_TXI和SCIn_RXI中断的条件，同时中断中的中断状态标志控制器单元(ICU)为1，ICU不输出中断请求，而是在内部保留它（每个源可以保留一个请求）。

当ICU中的中断状态标志设置为0时，输出ICU中保留的中断请求。当实际中断输出时，内部保留的中断请求会被自动丢弃。清除相关中断使能位（SCRSCR_SMCI中的TIE或RIE位）也可用于丢弃内部保留的中断请求。

34.10.2 SCIn_TXI和SCIn_RXI中断的缓冲区操作（选择FIFO）

即使ICU中的中断状态标志设置为1，SCIn_TXI和SCIn_RXI中断也不会向ICU输出中断请求。当ICU的中断状态标志清为0时，如果满足SCIn_TXI和SCIn_RXI中断的条件，则产生中断请求。

34.10.3 异步、时钟同步和简单SPI模式下的中断

(1) Non-FIFO selected

表34.26列出了异步模式、时钟同步模式和简单SPI模式下的中断源。可以为每个中断源分配不同的中断向量。个别中断源可以启用或禁用与

enable bits in the SCR register.

If the SCR.TIE bit is 1, an SCIn_TXI interrupt request is generated when transmit data is transferred from the TDR or TDRHL register*1 to the TSR register. An SCIn_TXI interrupt request can also be generated by using a single instruction to set the SCR.TE and SCR.TIE bits to 1 at the same time. An SCIn_TXI interrupt request can activate the DTC or DMAC to handle data transfer.

An SCIn_TXI interrupt request is not generated by setting the SCR.TE bit to 1 when SCR.TIE is 0 or by setting the SCR.TIE bit to 1 when the SCR.TE is 1.*2

When new data is not written by the time of transmission of the last bit of the current transmit data and SCR.TEIE is 1, the SSR.TEND flag is set to 1 and an SCIn_TEI interrupt request is generated. Additionally, when SCR.TE is 1, the SSR.TEND flag retains the value 1 until more transmit data is written to the TDR or TDRHL register*1, and setting SCR.TEIE to 1 leads to the generation of an SCIn_TEI interrupt request.

Writing data to the TDR or TDRHL register*1 leads to clearing of the SSR.TEND flag and, after a certain time, discarding of the SCIn_TEI interrupt request.

If the SCR.RIE bit is 1, an SCIn_RXI interrupt request is generated when received data is stored in the RDR register. An SCIn_RXI interrupt request can activate the DTC or DMAC to handle data transfer.

Setting any of the ORER, FER, and PER flags in the SSR register to 1 while the SCR.RIE bit is 1 leads to the generation of an SCIn_ERI interrupt request. An SCIn_RXI interrupt request is not generated at this time. Clearing all three flags (ORER, FER, and PER) leads to discarding of the SCIn_ERI interrupt request.

(2) FIFO selected

Table 34.27 lists interrupt sources in FIFO selected mode.

If the SCR.TIE bit is 1, an SCIn_TXI interrupt request is generated when the stored amount of data in the FTDRL register becomes the threshold value indicated in FCR.TTRG or below. An SCIn_TXI interrupt request can also be generated by using a single instruction to set the SCR.TE and SCR.TIE bits to 1 at the same time.

An SCIn_TXI interrupt request is not generated by setting SCR.TE to 1 when SCR.TIE is 0 or by setting SCR.TIE to 1 when SCR.TE is 1.

If SCR.TEIE is 1 and if the next data is not written to the FTDRL register by the time the last bit of the transmit data is sent, the SSR_FIFO.TEND flag is set to 1 and the SCIn_TEI interrupt request is generated.

If SCR.RIE is 1, the SCIn_RXI interrupt request is generated when the stored amount of data in the FRDRL register is equal to or greater than the threshold value indicated in FCR.RTRG. When RTRG is 0, an SCIn_RXI interrupt does not occur even when the amount of data in the receive FIFO is equal to 0.

If the SCR.RIE bit is 1, when the SSR_FIFO.ORER flag is set to 1 or data with a framing error or a parity error is stored in the FRDRL register, the SCIn_ERI interrupt request is generated. When the amount of data stored in the FRDRL register is at the threshold value or above, the SCIn_RXI interrupt request is also generated. The SCIn_ERI interrupt request can be canceled, in which case SSR_FIFO.ORER, FER, and PER flags are all cleared.

Note 1. When asynchronous mode and 9-bit data length are selected.
Note 2. To temporarily prohibit SCIn_TXI interrupts on transmission of the last of the data when a new round of transmission is to be started, after handling the transmission-completed interrupt, control activation of the interrupt by using the interrupt request enable bit in the ICU rather than using the SCR.TIE bit. This approach can prevent the suppression of SCIn_TXI interrupt requests in the transfer of new data.

Table 34.26 SCI interrupt sources with non-FIFO selected (1 of 2)

Name	Interrupt source	Interrupt flag	Interrupt enable	DTC activation	DMAC activation
SCIn_ERI	Receive error *1	ORER, FER, PER, DFER, DPER	RIE	Not possible	Not possible
SCIn_RXI	Receive data full	RDRF	RIE	Possible	Possible
	Address match	DCMF	RIE	Possible	Possible
SCIn_AM	Address match	DCMF	—	Possible	Possible

SCR寄存器中的使能位。

如果SCR.TIE位为1，则当发送数据从TDR传输或
TDRHL寄存器*1到TSR寄存器。也可以使用一条指令同时将SCR.TE和SCR.TIE位设置为1，从而产生SCIn_TXI中断请求。SCIn_TXI中断请求可以激活DTC或DMAC来处理数据传输。

当SCR.TIE为0时将SCR.TE位设置为1或通过设置
当SCR.TE为1时，SCR.TIE位为1。*2

当当前发送数据的最后一位发送时没有写入新数据且SCR.TEIE为1，则SSR.TEND标志设置为1，并产生SCIn_TEI中断请求。此外，当SCR.TE为1时，SSR.TEND标志保持值1，直到更多发送数据写入TDR或TDRHL寄存器*1，并设置

SCR.TEIE为1导致产生SCIn_TEI中断请求。

将数据写入TDR或TDRHL寄存器*1会导致SSR.TEND标志清零，并在一定时间后丢弃SCIn_TEI中断请求。

如果SCR.RIE位为1，则当接收到的数据存储在RDR寄存器中时会产生SCIn_RXI中断请求。一个SCIn_RXI中断请求可以激活DTC或DMAC来处理数据传输。

当SCR.RIE位为1时，将SSR寄存器中的任何ORER、FER和PER标志设置为1会导致产生SCIn_ERI中断请求。此时不产生SCIn_RXI中断请求。清除所有三个标志（ORER、FER和PER）会导致丢弃SCIn_ERI中断请求。

(2) FIFO selected

表34.27列出了FIFO选择模式下的中断源。

如果SCR.TIE位为1，当FTDRL寄存器中存储的数据量变为FCR.TTRG中指示的阈值或更低时，将产生SCIn_TXI中断请求。也可以使用一条指令同时将SCR.TE和SCR.TIE位设置为1，从而产生SCIn_TXI中断请求。

当SCR.TIE为0时将SCR.TE设置为1，或者当SCR.TE为1时将SCR.TIE设置为1，不会产生SCIn_TXI中断请求。

如果SCR.TEIE为1，并且在发送数据的最后一位时下一个数据未写入FTDRL寄存器，则SSR_FIFO.TEND标志设置为1，并产生SCIn_TEI中断请求。

如果SCR.RIE为1，则当FRDRL寄存器中存储的数据量等于或大于FCR.RTRG中指示的阈值时，将产生SCIn_RXI中断请求。当RTRG为0时，即使接收FIFO中的数据量等于0，也不会发生SCIn_RXI中断。

如果SCR.RIE位为1，当SSR_FIFO.ORER标志设置为1或帧错误或奇偶校验错误的数据存储在FRDRL寄存器中时，将产生SCIn_ERI中断请求。当FRDRL寄存器中存储的数据量在阈值或以上时，也会产生SCIn_RXI中断请求。SCIn_ERI中断请求可以被取消，在这种情况下SSR_FIFO.ORER、FER和PER标志都被清除。

注意1.选择异步模式和9位数据长度时。
注2.为了在新一轮传输开始时，在传输最后一个数据时暂时禁止SCIn_TXI中断，在处理完传输完成中断后，使用ICU中的中断请求使能位控制中断的激活而不是使用SCR.TIE位。这种方法可以防止在传输新数据时抑制SCIn_TXI中断请求。

Table 34.26 选择了非FIFO的SCI中断源（2个中的1个）

Name	中断源	中断标志	中断使能	DTC activation	DMAC activation
SCIn_ERI	接收错误*1	ORER、FER、PER、DFER、DPER	RIE	不可能	不可能
SCIn_RXI	接收数据已满	RDRF	RIE	Possible	Possible
	地址匹配	DCMF	RIE	Possible	Possible
SCIn_AM	地址匹配	DCMF	—	Possible	Possible

Table 34.26 SCI interrupt sources with non-FIFO selected (2 of 2)

Name	Interrupt source	Interrupt flag	Interrupt enable	DTC activation	DMAC activation
SCIn_TXI	Transmit data empty	TDRE	TIE	Possible	Possible
SCIn_TEI	Transmit end	TEND	TEIE	Not possible	Not possible

Note 1. The interrupt flag is only ORER when in clock synchronous and simple SPI mode.

Table 34.27 SCI interrupt sources with FIFO selected

Name	Interrupt source	Interrupt flag	Interrupt enable	DTC activation	DMAC activation
SCIn_ERI	Receive error*1	ORER, FER, PER, DFER, DPER	RIE	Not possible	Not possible
		DR (when FCR.DRES = 1)	RIE	Not possible	Not possible
SCIn_RXI	Receive data full	RDF	RIE	Possible	Possible
	Receive data ready	DR (when FCR.DRES = 0)	RIE	Possible	Possible
	Address match	DCMF	RIE	Possible	Possible
SCIn_AM	Address match	DCMF	—	Possible	Possible
SCIn_TXI	Transmit data empty	TDFE	TIE	Possible	Possible
SCIn_TEI	Transmit end	TEND	TEIE	Not possible	Not possible

Note 1. The interrupt flag is only ORER when in clock synchronous and simple SPI mode.

34.10.4 Interrupts in Smart Card Interface Mode

Table 34.28 lists interrupt sources in smart card interface mode. A transmit end interrupt (SCIn_TEI) request and an address match (SCIn_AM) request cannot be used in this mode.

Table 34.28 SCI Interrupt sources

Name	Interrupt source	Interrupt flag	Interrupt enable	DTC activation	DMAC activation
SCIn_ERI	Receive error or error signal detection	ORER, FER, ERS	RIE	Not possible	Not possible
SCIn_RXI	Receive data full	RDRF	RIE	Possible	Possible
SCIn_TXI	Transmit end	TEND	TIE	Possible	Possible

Data transmission or reception using the DTC or DMAC is also possible in smart card interface mode. In transmission, when the SSR_SMCI.TEND flag is set to 1, an SCIn_TXI interrupt request is generated. This SCIn_TXI interrupt request activates the DTC or DMAC, allowing transfer of transmit data if the SCIn_TXI request is previously specified as a source of DTC or DMAC activation. The TEND flag is automatically set to 0 when the DTC or DMAC transfers the data.

If an error occurs, the SCI automatically retransmits the same data. During the retransmission, the TEND flag is kept at 0 and the DTC or DMAC is not activated. Therefore, the SCI and DTC or DMAC automatically transmit the specified number of bytes, including retransmission after an error occurrence. However, the SSR_SMCI.ERS flag is not automatically cleared to 0 at error occurrence. Therefore, the ERS flag must be cleared by previously setting the SCR_SMCI.RIE bit to 1 to enable an SCIn_ERI interrupt request to be generated at error occurrence.

When transmitting or receiving data using the DTC or DMAC, always enable the DTC or DMAC before making the SCI settings. For DTC or DMAC settings, see section 17, DMA Controller (DMAC) and section 18, Data Transfer Controller (DTC).

In reception, an SCIn_RXI interrupt request is generated when receive data is set to the RDR register. This SCIn_RXI interrupt request activates the DTC or DMAC, allowing transfer of the receive data if the SCIn_RXI request is previously specified as a source of DTC or DMAC activation. If an error occurs, the error flag is set. Therefore, the DTC or DMAC is not activated and an SCIn_ERI interrupt request is issued to the CPU instead. The error flag must be cleared.

Table 34.26 选择非FIFO的SCI中断源（2个中的2个）

Name	中断源	中断标志	中断使能	DTC activation	DMAC activation
SCIn_TXI	传输数据为空	TDRE	TIE	Possible	Possible
SCIn_TEI	发射端	TEND	TEIE	不可能	不可能

注1.中断标志 仅在时钟同步和简单SPI模式下为ORER。

Table 34.27 选择了FIFO的SCI中断源

Name	中断源	中断标志	中断使能	DTC activation	DMAC activation
SCIn_ERI	Receive error*1	ORER、FER、PER、DFER、DPER	RIE	不可能	不可能
		DR (when FCR.DRES = 1)	RIE	不可能	不可能
SCIn_RXI	接收数据已满	RDF	RIE	Possible	Possible
	接收数据就绪	DR (when FCR.DRES = 0)	RIE	Possible	Possible
	地址匹配	DCMF	RIE	Possible	Possible
SCIn_AM	地址匹配	DCMF	—	Possible	Possible
SCIn_TXI	传输数据为空	TDFE	TIE	Possible	Possible
SCIn_TEI	发射端	TEND	TEIE	不可能	不可能

注1.中断标志 仅在时钟同步和简单SPI模式下为ORER。

34.10.4 智能卡接口模式中的中断

表34.28列出了智能卡接口模式下的中断源。在此模式下不能使用发送结束中断(SCIn_TEI)请求和地址匹配(SCIn_AM)请求。

Table 34.28 SCI中断源

Name	中断源	中断标志	中断使能	DTC activation	DMAC activation
SCIn_ERI	接收错误或错误信号检测	ORER、FER、ERS	RIE	不可能	不可能
SCIn_RXI	接收数据已满	RDRF	RIE	Possible	Possible
SCIn_TXI	发射端	TEND	TIE	Possible	Possible

在智能卡接口模式下也可以使用DTC或DMAC进行数据传输或接收。在发送过程中，当SSR_SMCI.TEND标志设置为1时，会产生一个SCIn_TXI中断请求。该SCIn_TXI中断请求激活DTC或DMAC，如果之前将SCIn_TXI请求指定为DTC或DMAC激活源，则允许传输数据。当DTC或DMAC传输数据时，TEND标志自动设置为0。

如果发生错误，SCI会自动重新传输相同的数据。在重传期间，TEND标志保持为0，并且DTC或DMAC不被激活。因此，SCI和DTC或DMAC会自动传输指定的字节数，包括发生错误后的重传。但是，发生错误时，SSR_SMCI.ERS标志不会自动清除为0。因此，必须通过预先将SCR_SMCI.RIE位设置为1来清除ERS 标志，以在发生错误时启用SCIn_ERI中断请求。

使用DTC或DMAC发送或接收数据时，请务必在进行SCI设置之前启用DTC或DMAC。有关DTC或DMAC设置，请参阅第17节，DMA控制器(DMAC)和第18节，数据传输控制器(DTC)。

在接收中，当接收数据设置到RDR寄存器时，会产生SCIn_RXI中断请求。该SCIn_RXI中断请求激活DTC或DMAC，如果先前将SCIn_RXI请求指定为DTC或DMAC激活源，则允许传输接收数据。如果发生错误，则设置错误标志。因此，不会激活DTC或DMAC，而是向CPU发出SCIn_ERI中断请求。必须清除错误标志。

34.10.5 Interrupts in Simple IIC Mode

Table 34.29 lists the interrupt sources in simple IIC mode. The STI interrupt is allocated to the transmit end interrupt (SCIn_TEI) request. The receive error interrupt (SCIn_ERI) and the address match (SCIn_AM) request cannot be used.

The DTC or DMAC can also be used to handle transfer in simple IIC mode.

When the SIMR2.IICINTM bit is 1:

- An SCIn_RXI request is generated on the falling edge of the SCLn signal for the 8th bit. If SCIn_RXI is previously set up as an activation source for the DTC or DMAC, the SCIn_RXI request activates the DTC or DMAC to handle transfer of the received data.
- An SCIn_TXI request is generated on the falling edge of the SCLn signal for the 9th bit (acknowledge bit). If SCIn_TXI is previously set up as an activation source for the DTC or DMAC, the SCIn_TXI request activates the DTC or DMAC to handle transfer of the transmit data.

When the SIMR2.IICINTM bit is 0:

- An SCIn_RXI request (ACK detection) is generated if the input on the SDAn pin is low on the rising edge of the SCLn signal for the 9th bit (acknowledge bit)
- An SCIn_TXI request (NACK detection) is generated if the input on the SDAn pin is high on the rising edge of the SCLn signal for the 9th bit (acknowledge bit)
- If SCIn_RXI is previously set up as an activation source for the DTC or DMAC, the SCIn_RXI request activates the DTC or DMAC to handle transfer of the received data.

If the DTC or DMAC is used for data transfer in reception or transmission, always set up and enable the DTC or DMAC before setting up the SCI.

When the IICSTAREQ, IICRSTAREQ, and IICSTPREQ bits in SIMR3 are used to generate a start condition, restart condition, or stop condition, the STI request is issued when generation is complete.

Table 34.29 SCI interrupt sources

Name	Interrupt source	Interrupt flag	Interrupt enable	DTC activation	DMAC activation
SCIn_RXI	Reception, ACK detection	—	RIE	Possible	Possible
SCIn_TXI	Transmission, NACK detection	—	TIE	Possible	Possible
STIn	Completion of generation of a start, restart, or stop condition	IICSTIF	TEIE	Not possible	Not possible

Note 1. Activation of the DTC is only possible when the SIMR2.IICINTM bit is 1 (use reception and transmission interrupts).

34.11 Event Linking

By using interrupt request signals as event signals, the SCI can provide linked operation through the ELC for modules selected in advance.

Event signals can be output regardless of the values of the associated interrupt request enable bits.

(1) Error event output (receive error or error signal detected)

- Indicates abnormal termination because of a parity error during reception in asynchronous mode
- Indicates abnormal termination because of a framing error during reception in asynchronous mode
- Indicates abnormal termination because of an overrun error during reception
- Indicates detection of the error signal during transmission in smart card interface mode
- The SSR_FIFO.FER and PER flags are 0, and receive data less than the receive FIFO data trigger number is set in a reception FIFO buffer, and it indicates that 15 ETUs elapse when FIFO is selected and the FCR.DRES bit is 1.

34.10.5 简单IIC模式下的中断

表34.29列出了简单IIC模式下的中断源。STI中断分配给发送结束中断(SCIn_TEI)请求。不能使用接收错误中断(SCIn_ERI)和地址匹配(SCIn_AM)请求。

DTC或DMAC也可用于处理简单IIC模式下的传输。

当SIMR2.IICINTM位为1时：

- SCIn_RXI请求在第8位的SCLn信号的下降沿产生。如果SCIn_RXI先前设置为DTC或DMAC的激活源，则SCIn_RXI请求将激活DTC或DMAC以处理接收数据的传输。
- SCIn_TXI请求在第9位（确认位）的SCLn信号的下降沿生成。如果SCIn_TXI先前设置为DTC或DMAC的激活源，SCIn_TXI请求激活DTC或DMAC来处理传输数据的传输。

当SIMR2.IICINTM位为0时：

- 如果SDAn引脚上的输入在第9位的SCLn信号（确认位）
- 如果SDAn引脚上的输入在第9位的SCLn信号（确认位）
- 如果SCIn_RXI先前设置为DTC或DMAC的激活源，则SCIn_RXI请求会激活DTC或DMAC处理接收数据的传输。

如果DTC或DMAC用于接收或传输中的数据传输，请务必在设置SCI之前设置并启用DTC或DMAC。

当SIMR3中的IICSTAREQ、IICRSTAREQ和IICSTPREQ位用于生成开始条件、重新启动条件或停止条件时，生成完成时会发出STI请求。

Table 34.29 SCI中断源

Name	中断源	中断标志	中断使能	DTC activation	DMAC activation
SCIn_RXI	接收、ACK检测	—	RIE	Possible	Possible
SCIn_TXI	传输、NACK检测	—	TIE	Possible	Possible
STIn	完成启动、重新启动或停止条件的生成	IICSTIF	TEIE	不可能	不可能

注1.只有当SIMR2.IICINTM位为1（使用接收和发送中断）时，才能激活DTC。

34.11 事件链接

通过使用中断请求信号作为事件信号，SCI可以通过ELC为预先选择的模块提供联动操作。

无论相关中断请求使能位的值如何，都可以输出事件信号。

(1) 错误事件输出（接收错误或检测到错误信号）

- 表示在异步模式下接收期间由于奇偶校验错误而异常终止
- 指示在异步模式下接收期间由于帧错误而异常终止
- 表示接收期间由于溢出错误而异常终止
- 指示在智能卡接口模式下传输期间检测到错误信号
- ssr_fifo.fer和每个标志为0，并且接收数据小于接收FIFO数据触发器编号在接收FIFO缓冲区中设置，这表明选择FIFO时15ETUSETALESE，而FCR.DRES位为1。

(2) Receive data full event output

- Indicates that ACK is detected if the SIMR2.IICINTM bit is 0 in simple IIC mode
- Indicates that the 8th-bit SCLn falling edge is detected if the SIMR2.IICINTM bit is 1 in simple IIC mode
- When the SIMR2.IICINTM bit is 1 during master transmission in simple IIC mode, set the ELC so that receive data full events are not used.

(a) Non-FIFO selected

- Indicates that received data is set in the Receive Data Register (RDR or RDRHL).

(b) FIFO selected

- Using this event output is prohibited.

(3) Transmit data empty event output

- Indicates that the SCR/SCR_SMCI.TE bit is changed from 0 to 1
- Indicates that transmission is complete in smart card interface mode
- Indicates that NACK is detected if the SIMR2.IICINTM bit is 0 in simple IIC mode
- Indicates that the 9th-bit SCLn falling edge is detected if the SIMR2.IICINTM bit is 1 in simple IIC mode.

(a) Non-FIFO selected

- Indicates that transmit data is transferred from the Transmit Data Register (TDR or TDRHL) to the Transmit Shift Register (TSR).

(b) FIFO selected

- Using this event output is prohibited.

(4) Transmit end event output

- Indicates the completion of transmission
- Indicates that the starting condition, resumption condition, or termination condition is generated in simple IIC mode
- When FIFO is selected, using this event output is prohibited.

(5) Address match event output

- Indicates a match of the comparison data (CDR.CMPD) with one frame of receive data when DCCR.DCME is set to 1 in asynchronous mode, including multi-processor mode.

34.12 Address Mismatch Event Output (SCI0_DCUF)

SCI0_DCUF indicates the mismatch of comparison data (CDR.CMPD) with one frame of receive data when DCCR.DCME is set to 1 in asynchronous mode, including multi-processor mode. This event can be used for Snooze end request only.

34.13 Noise Cancellation Function

Figure 34.72 shows the configuration of the noise filter used for noise cancellation. The noise filter consists of a 2-stage flip-flop circuit and a match detection circuit. When the input signals of the noise filter and the output signals of the 2-stage flip-flop circuits completely match, the matched level is conveyed as an internal signal. Unless otherwise matched, the previous value is retained. When the same level is retained for 3 cycles or longer on the sampling clock of the noise filter, it is considered as a valid receive signal. A change in pulse for 3 cycles or shorter is considered as noise, not as a receive signal.

When SEMR.ABCS = 0 and SEMR.ABCSE = 0, the cycle is 1/16 the period of 1 transfer bit.

When SEMR.ABCS = 1 and SEMR.ABCSE = 0, the cycle is 1/8 the period of 1 transfer bit.

When SEMR.ABCSE = 1, the cycle is 1/6 the period of 1 transfer bit.

(2) 接收数据满事件输出

- 如果SIMR2.IICINTM位在简单IIC模式下为0，则表示检测到ACK
- 表示如果SIMR2.IICINTM位在简单IIC模式下为1，则检测到第8位SCLn下降沿
- 当SIMR2.IICINTM位在简单IIC模式下主机发送期间为1时，设置ELC以便不使用接收数据满事件。

(a) Non-FIFO selected

- 表示接收数据设置在接收数据寄存器（RDR或RDRHL）中。

(b) FIFO selected

- 禁止使用此事件输出。

(3) 传输数据空事件输出

- 表示SCRSCR_SMCI.TE位由0变为1
- 表示在智能卡接口模式下传输完成
- 如果SIMR2.IICINTM位在简单IIC模式下为0，则表示检测到NACK
- 表示如果SIMR2.IICINTM位在简单IIC模式下为1，则检测到第9位SCLn下降沿。

(a) Non-FIFO selected

- 表示发送数据从发送数据寄存器（TDR或TDRHL）传输到发送移位 Register (TSR).

(b) FIFO selected

- 禁止使用此事件输出。

(4) 发送结束事件输出

- 表示传输完成
- 指示在简单IIC模式下生成启动条件、恢复条件或终止条件
- 选择FIFO时，禁止使用该事件输出。

(5) 地址匹配事件输出

- 当DCCR.DCME在异步模式（包括多处理器模式）下设置为1时，表示比较数据(CDR.CMPD)与一帧接收数据的匹配。

34.12 地址不匹配事件输出(SCI0_DCUF)

SCI0_DCUF表示比较数据（CDR.CMPD）与一帧接收数据不匹配时
DCCR.DCME在异步模式下设置为1，包括多处理器模式。此事件仅可用于贪睡结束请求。

34.13 降噪功能

图34.72显示了用于噪声消除的噪声滤波器的配置。噪声滤波器由一个2级触发器电路和一个匹配检测电路组成。当噪声滤波器的输入信号和2级触发器电路的输出信号完全匹配时，匹配的电平作为内部信号传送。除非另有匹配，否则将保留先前的值。当相同电平在噪声滤波器的采样时钟上保持3个周期或更长时间时，它被认为是有效的接收信号。3个周期或更短的脉冲变化被认为是噪声，而不是接收信号。

当SEMR.ABCS=0且SEMR.ABCSE=0时，周期为1161个传输位的周期。

当SEMR.ABCS=1和SEMR.ABCSE=0时，周期为181个传输位的周期。

当SEMR.ABCSE=1时，周期为161个传输位的周期。

In asynchronous mode, the noise cancellation function can be applied to the receive signal input to the RXDn pin. The receive level of the RXDn is taken in the flip-flop circuit of the noise filter on the base clock of asynchronous mode.

In simple IIC mode, this function can be used for each input on SDAn and SCLn. The sampling clock for the noise cancellation function is selected in the SNFR.NFCS bit by dividing the baud rate generator source clock by 1, 2, 4, or 8.

If the base clock is stopped once with the noise filter enabled and then the base clock input is restarted again, the noise filter operation resumes from the state where the clock was stopped. When SCR.TE and SCR.RE are set to 0 during base clock input, all of the noise filter flip-flop values are initialized to 1. Accordingly, if the input data is 1 when reception operation resumes, the function determines that a level match is detected and the result is conveyed as an internal signal. When the level being input corresponds to 0, the initial output of the noise filter is retained until the level matches in three consecutive sampling cycles.

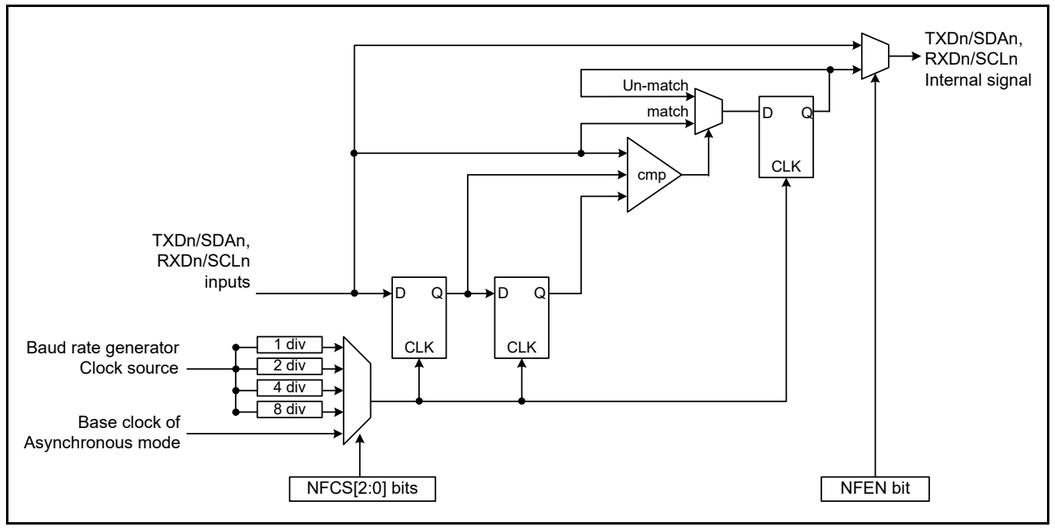


Figure 34.72 Digital noise filter circuit block diagram

34.14 Usage Notes

34.14.1 Settings for the Module-Stop Function

The Module Stop Control Register B (MSTPCRB) can enable or disable SCI operation. The SCI is initially stopped after reset. Releasing the module-stop state enables access to the registers. For details, see section 11, Low Power Modes.

34.14.2 SCI Operation during Low Power State

(1) Transmission

When setting the module to the stopped state or in transitions to Software Standby, stop operations (by setting the TIE, TE, and TEIE bits in the SCR/SCR_SMCI to 0) after switching the TXDn pin to the general I/O port pin function. When setting I/O port as an SCI connection, the SPTR register can control the state of the TXDn pin. Setting the TE bit to 0 initializes the TSR register and the TEND bit in the SSR/SSR_SMCI is initialized to 1 with non-FIFO selected. The value is saved with FIFO selected. Depending on the port settings and SPTR register settings, output pins might output the level before a transition to the low power state is made after release from the module-stop state or Software Standby mode. When transitions to these states are made during transmission, the transmitted data becomes indeterminate.

To transmit data in the same transmission mode after cancellation of the low power state:

1. Set the TE bit to 1.
2. Read SSR/SSR_FIFO/SSR_SMCI.
3. Write data to TDR sequentially to start data transmission.

在异步模式下，可以对输入到RXDn引脚的接收信号应用噪声消除功能。RXDn的接收电平是在异步模式的基本时钟上的噪声滤波器的触发器电路中获取的。

在简单IIC模式下，该功能可用于SDAn和SCLn上的每个输入。通过将波特率发生器源时钟除以1、2、4或8，在SNFR.NFCS位中选择噪声消除功能的采样时钟。

如果在启用噪声滤波器的情况下基准时钟停止一次，然后再次重新启动基准时钟输入，则噪声滤波器操作将从时钟停止的状态恢复。当SCR.TE和SCR.RE在基本时钟输入期间设置为0时，所有噪声滤波器触发器值都被初始化为1。因此，如果在接收操作恢复时输入数据为1，则该函数确定一个电平检测到匹配并将结果作为内部信号传送。当输入的电平对应于0时，保留噪声滤波器的初始输出，直到电平在三个连续的采样周期中匹配。

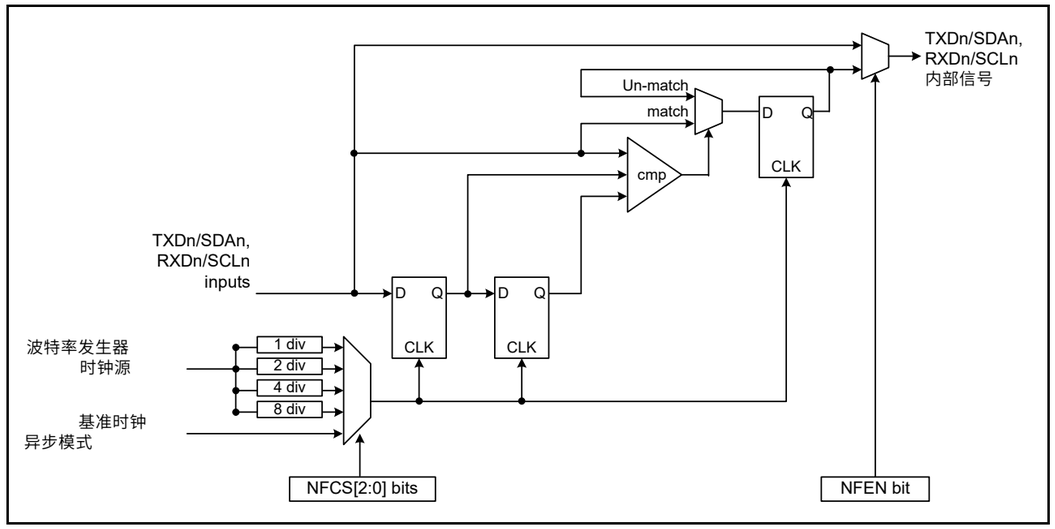


Figure 34.72 数字噪声滤波器电路框图

34.14 使用说明

34.14.1 模块停止功能的设置

模块停止控制寄存器B(MSTPCRB)可以启用或禁用SCI操作。SCI在复位后最初停止。释放模块停止状态可以访问寄存器。有关详细信息，请参阅第11节，低功耗模式。

34.14.2 低功耗状态下的SCI操作

(1) Transmission

将模块设置为停止状态或转换到软件待机时，在将TXDn引脚切换到通用IO端口引脚功能后停止操作（通过将SCRSCR_SMCI中的TIE、TE和TEIE位设置为0）。当设置IO端口为SCI连接时，SPTR寄存器可以控制TXDn引脚的状态。将TE位设置为0会初始化TSR寄存器，并且SSRSSR_SMCI中的TEND位会在选择非FIFO时初始化为1。该值在选择FIFO的情况下保存。根据端口设置和SPTR寄存器设置，输出引脚可能会在从模块停止状态或软件待机模式释放后转换到低功耗状态之前输出电平。在传输过程中转换到这些状态时，传输的数据变得不确定。

在取消低功耗状态后以相同的传输模式传输数据：

1. 将TE位设置为1。
2. Read SSR/SSR_FIFO/SSR_SMCI.
3. 将数据顺序写入TDR以开始数据传输。

To transmit data with a different transmission mode, initialize the SCI first.

Figure 34.73 shows an example flow of transition to Software Standby mode during transmission. Figure 34.74 and Figure 34.75 show the port pin states during transition to Software Standby mode.

Before specifying the module-stop state or making a transition to Software Standby mode from the transmission mode using DTC transfer, stop the transmit operations (TE = 0). To start transmission after cancellation using the DTC, set the TE bit to 1. The SCIn_TXI interrupt flag is set to 1 and transmission starts using the DTC.

(2) Reception

(a) When address match function is not used as wakeup condition

Before specifying the module-stop state or making a transition to Software Standby mode, stop the receive operations (RE = 0 in SCR/SCR_SMCI). If transition is made during data reception, the received data is invalid.

Figure 34.76 shows an example flow of transition to Software Standby mode during reception.

(b) When address match function is used as wakeup condition

Before specifying the module-stop state or making a transition to Software Standby mode:

1. Set the operations after cancellation of the low power state.
2. Set CDR.CMPD and DCCR.DCME to 1.
3. Set the receive operations (RE = 1 in SCR/SCR_SMCI).
4. Set the module-stop state or Software Standby mode.

When SCI transfers to low power mode, if the receive data pin (RXD) is at the low level, set SEMR.RXDESEL = 0. When setting SEMR.RXDESEL = 1, there is a possibility that a start bit (falling edge of RXDn pin) cannot be detected on release of the low power mode.

Figure 34.77 shows an example flow of transition to Software Standby mode during reception with address match.

(c) When using SCI0 in Snooze mode

When using SCI0 in Snooze mode, some restrictions apply, including maximum bit rates. For details, see section 11, Low Power Modes.

要以不同的传输模式传输数据，请先初始化SCI。

图34.73显示了传输期间转换到软件待机模式的示例流程。图34.74和
图34.75显示了转换到软件待机模式期间的端口引脚状态。

在使用DTC传输指定模块停止状态或从传输模式转换到软件待机模式之前，请停止传输操作(TE=0)。要在使用DTC取消后开始发送，请将TE位设置为1。SCIn_TXI中断标志 设置为1并使用DTC开始发送。

(2) Reception

(a) 当地址匹配功能不用作唤醒条件时

在指定模块停止状态或转换到软件待机模式之前，停止接收操作（SCRSCR_SMCI中的RE=0）。如果在数据接收期间进行转换，则接收到的数据无效。

图34.76显示了接收期间转换到软件待机模式的示例流程。

(b) 当地址匹配功能用作唤醒条件时

在指定模块停止状态或转换到软件待机模式之前：

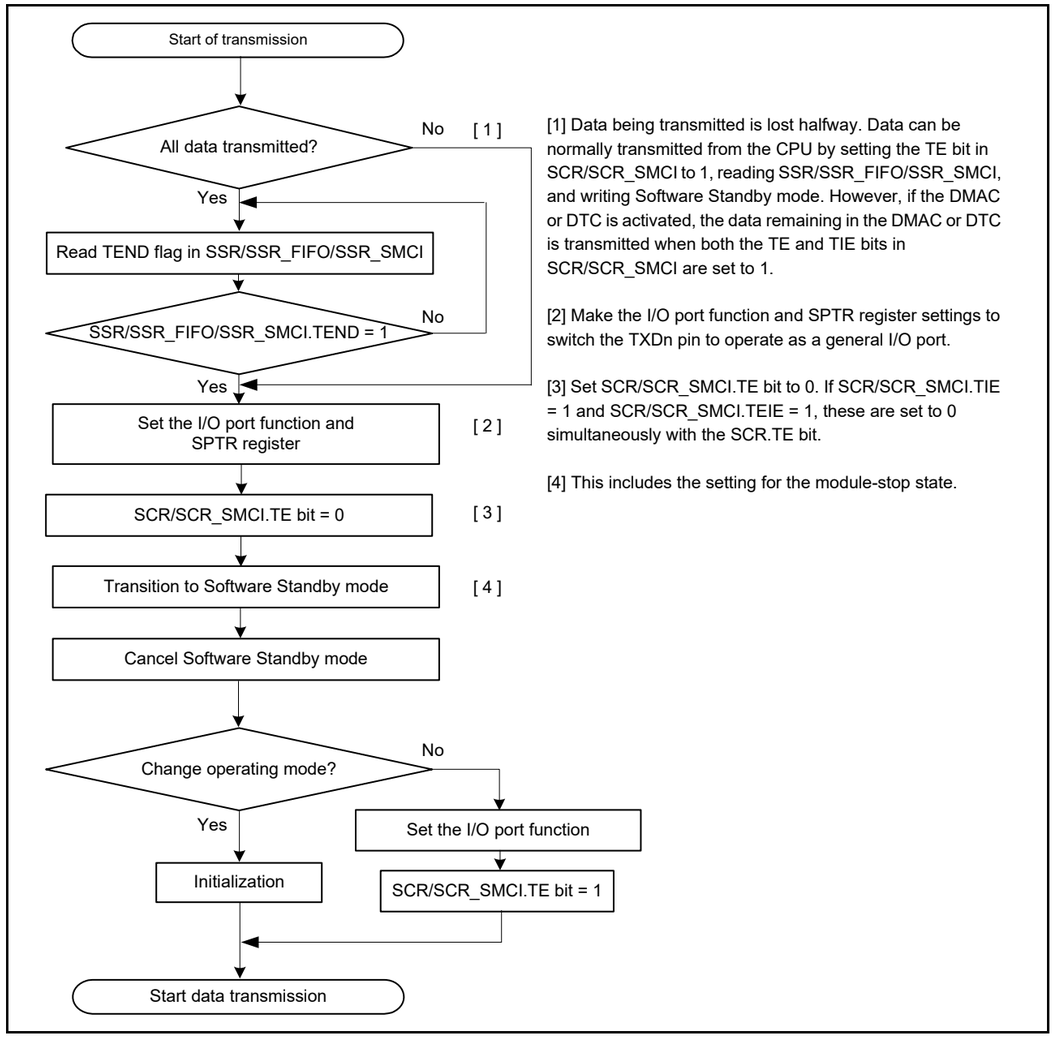
1. 设置取消低功耗状态后的操作。
2. 将CDR.CMPD和DCCR.DCME设置为1。
3. 设置接收操作（在SCRSCR_SMCI中RE=1）。
4. 设置模块停止状态或软件待机模式。

当SCI转移到低功耗模式时，如果接收数据引脚(RXD)为低电平，则设置SEMR.RXDESEL=0。
当设置SEMR.RXDESEL=1时，在解除低功耗模式时可能无法检测到起始位（RXDn引脚的下降沿）。

图34.77显示了在地址匹配的接收期间转换到软件待机模式的示例流程。

(c) 在贪睡模式下使用SCI0时

在贪睡模式下使用SCI0时，有一些限制，包括最大比特率。有关详细信息，请参阅第11节，低功耗模式。



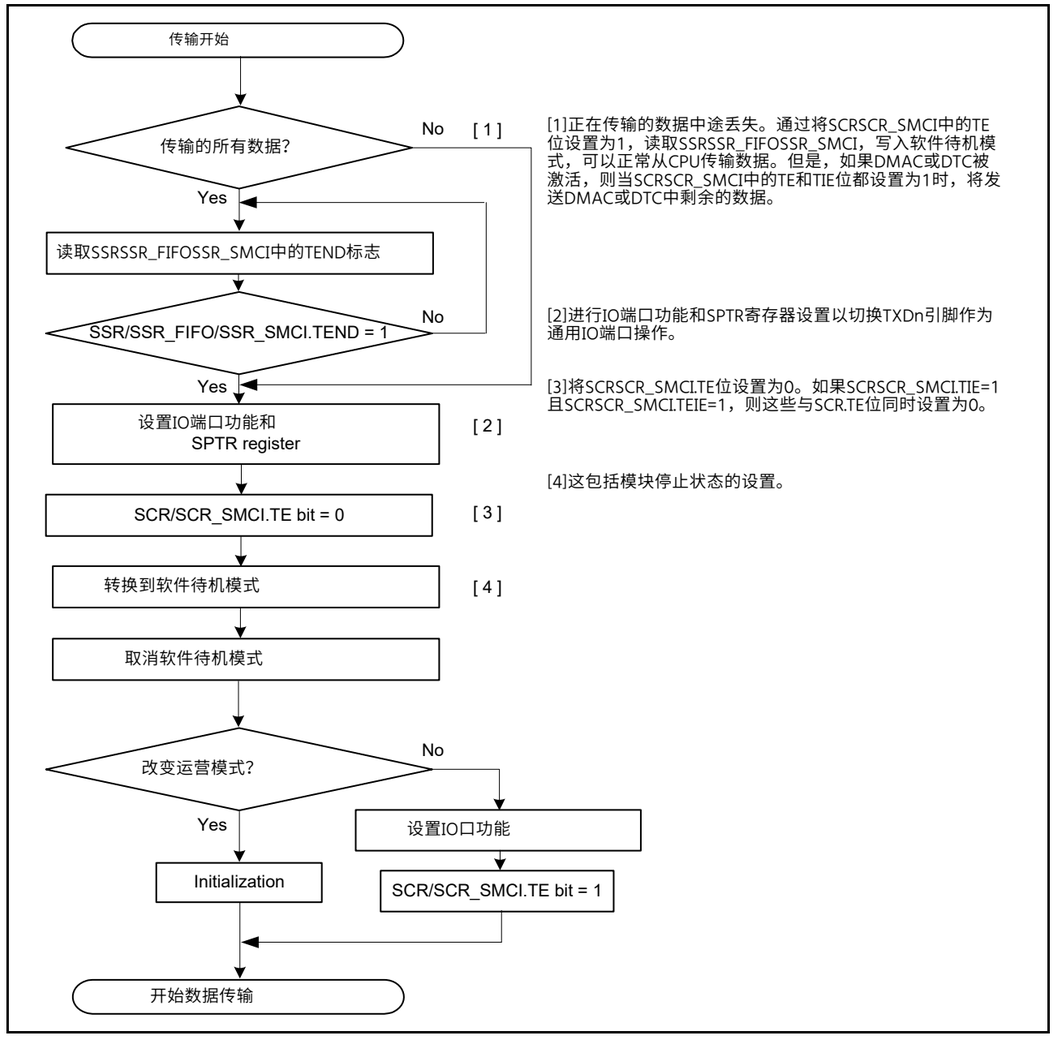
[1] Data being transmitted is lost halfway. Data can be normally transmitted from the CPU by setting the TE bit in SCR/SCR_SMCI to 1, reading SSR/SSR_FIFO/SSR_SMCI, and writing Software Standby mode. However, if the DMAC or DTC is activated, the data remaining in the DMAC or DTC is transmitted when both the TE and TIE bits in SCR/SCR_SMCI are set to 1.

[2] Make the I/O port function and SPTR register settings to switch the TXDn pin to operate as a general I/O port.

[3] Set SCR/SCR_SMCI.TE bit to 0. If SCR/SCR_SMCI.TIE = 1 and SCR/SCR_SMCI.TEIE = 1, these are set to 0 simultaneously with the SCR.TE bit.

[4] This includes the setting for the module-stop state.

Figure 34.73 Example flow of transition to Software Standby mode during transmission



[1]正在传输的数据中途丢失。通过将SCRSCR_SMCI中的TE位设置为1，读取SSRSSR_FIFOSSR_SMCI，写入软件待机模式，可以正常从CPU传输数据。但是，如果DMAC或DTC被激活，则当SCRSCR_SMCI中的TE和TIE位都设置为1时，将发送DMAC或DTC中剩余的数据。

[2]进行IO端口功能和SPTR寄存器设置以切换TXDn引脚作为通用IO端口操作。

[3]将SCRSCR_SMCI.TE位设置为0。如果SCRSCR_SMCI.TIE=1且SCRSCR_SMCI.TEIE=1，则这些与SCR.TE位同时设置为0。

[4]这包括模块停止状态的设置。

Figure 34.73 传输期间转换到软件待机模式的示例流程

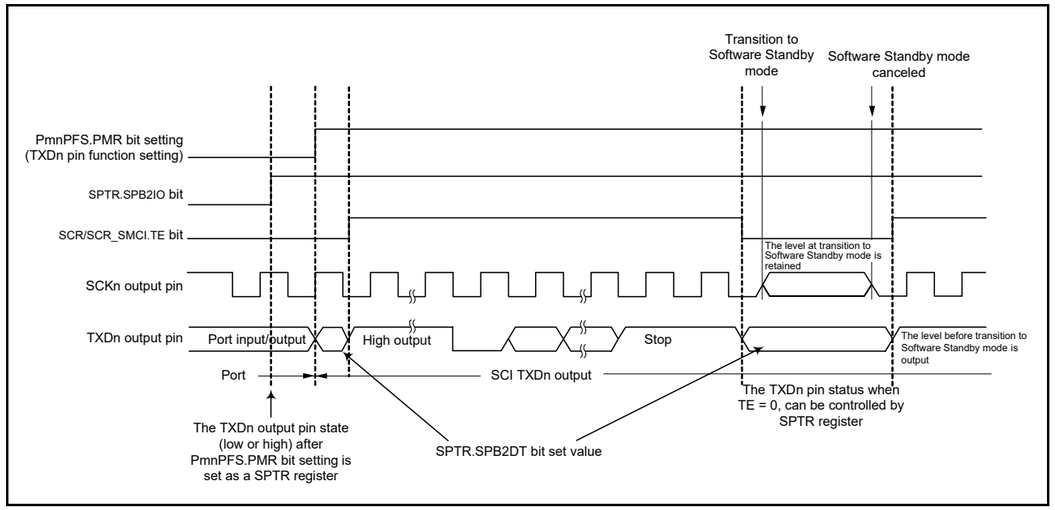


Figure 34.74 Port pin states during transition to Software Standby mode with internal clock and asynchronous transmission

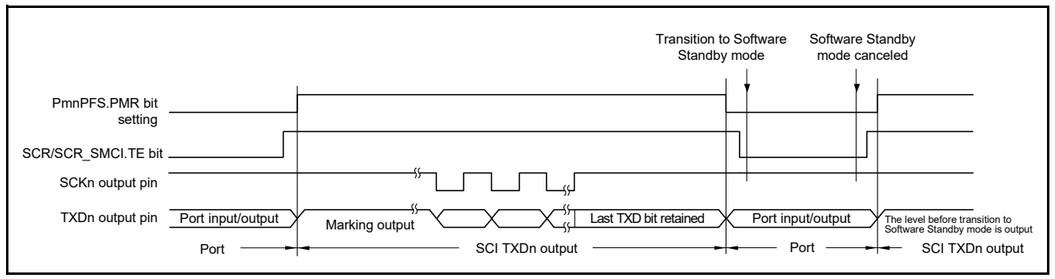


Figure 34.75 Port pin states during transition to Software Standby mode with internal clock and clock synchronous transmission

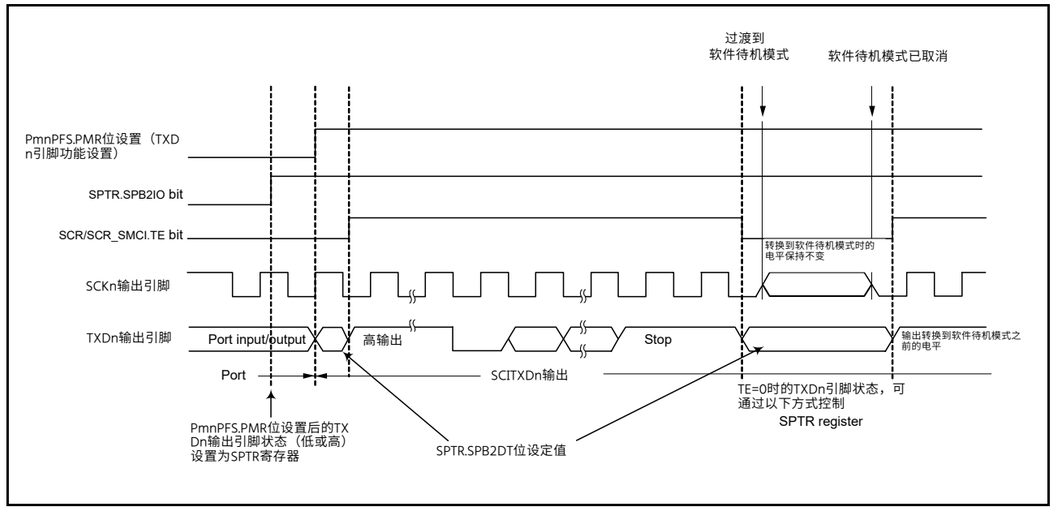


Figure 34.74 转换到内部时钟和异步传输的软件待机模式期间的端口引脚状态

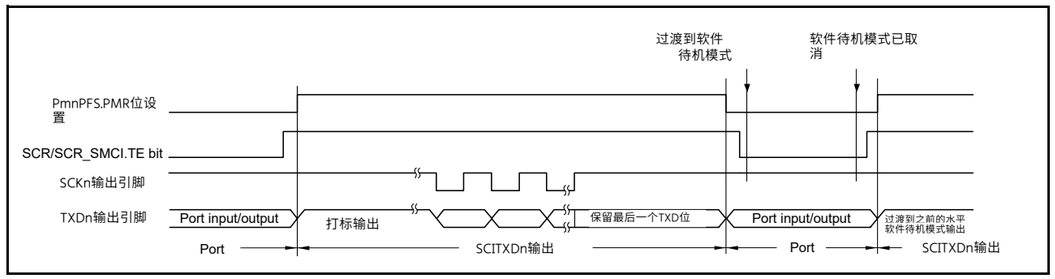
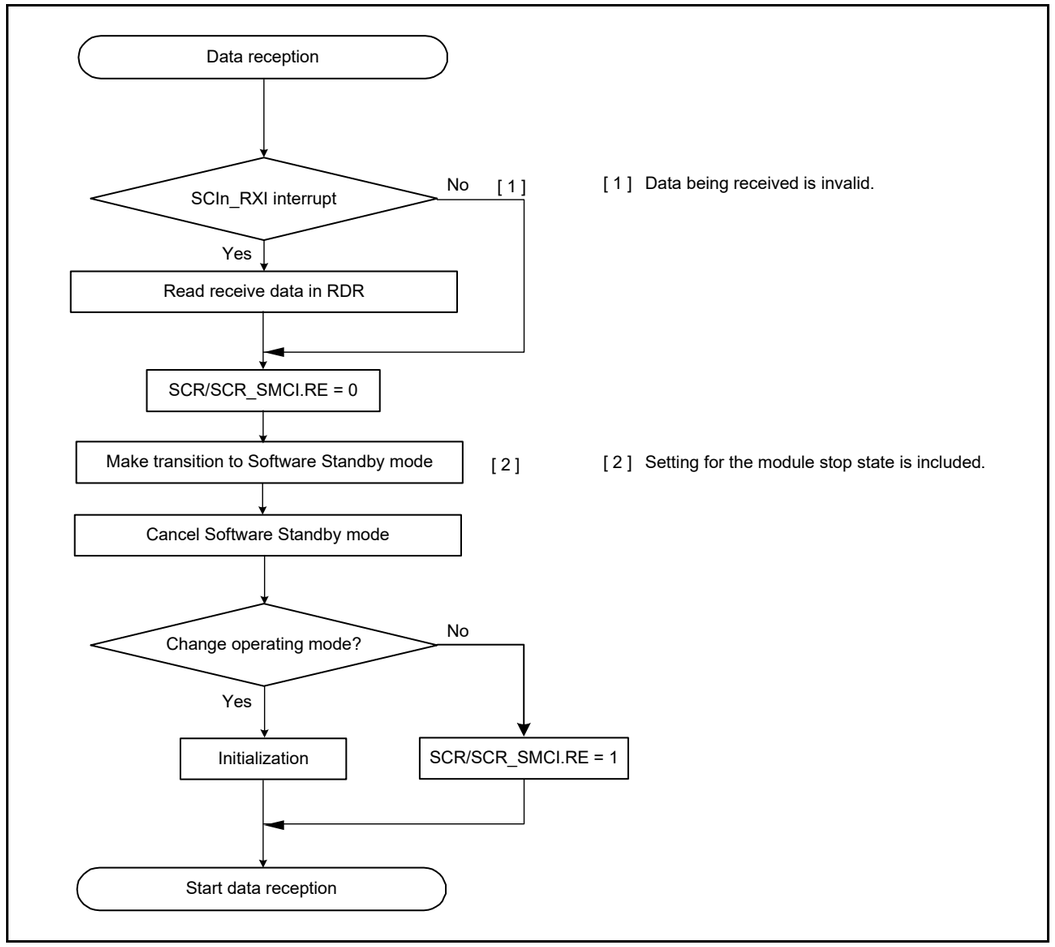


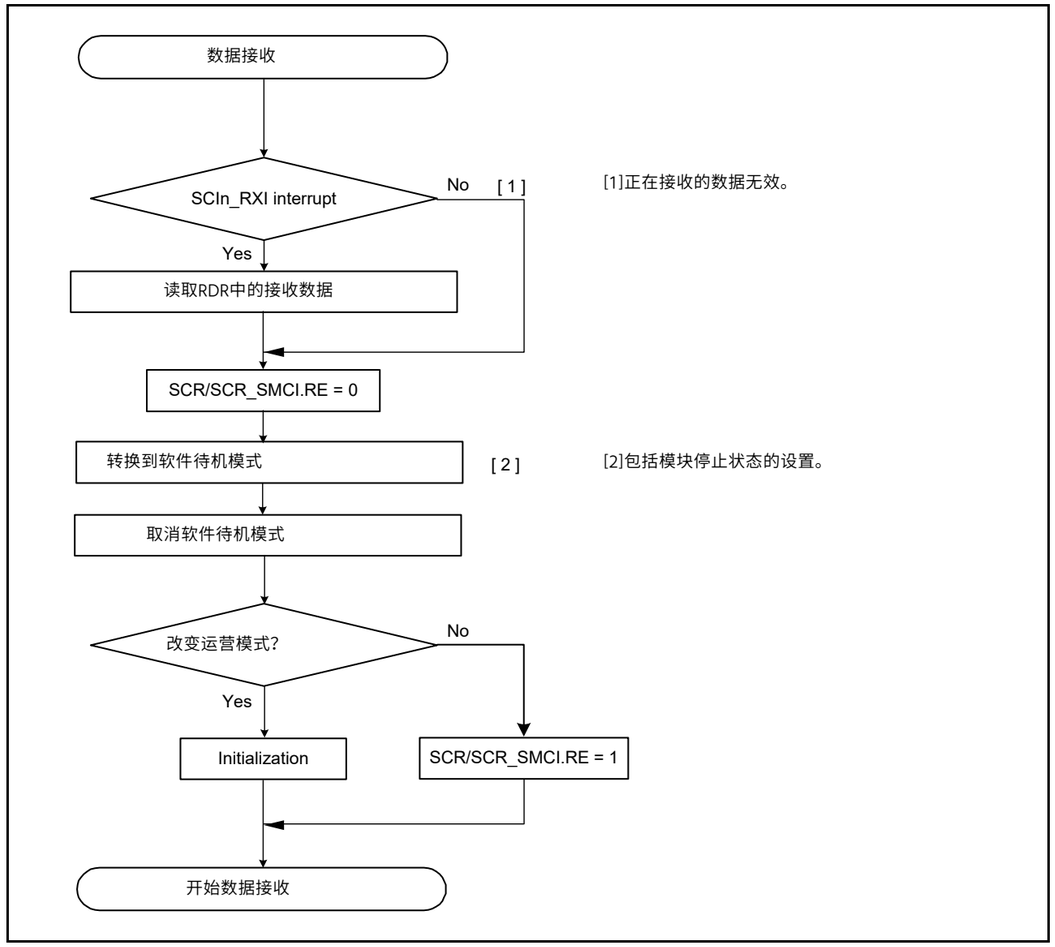
Figure 34.75 通过内部时钟和时钟同步传输转换到软件待机模式期间的端口引脚状态



[1] Data being received is invalid.

[2] Setting for the module stop state is included.

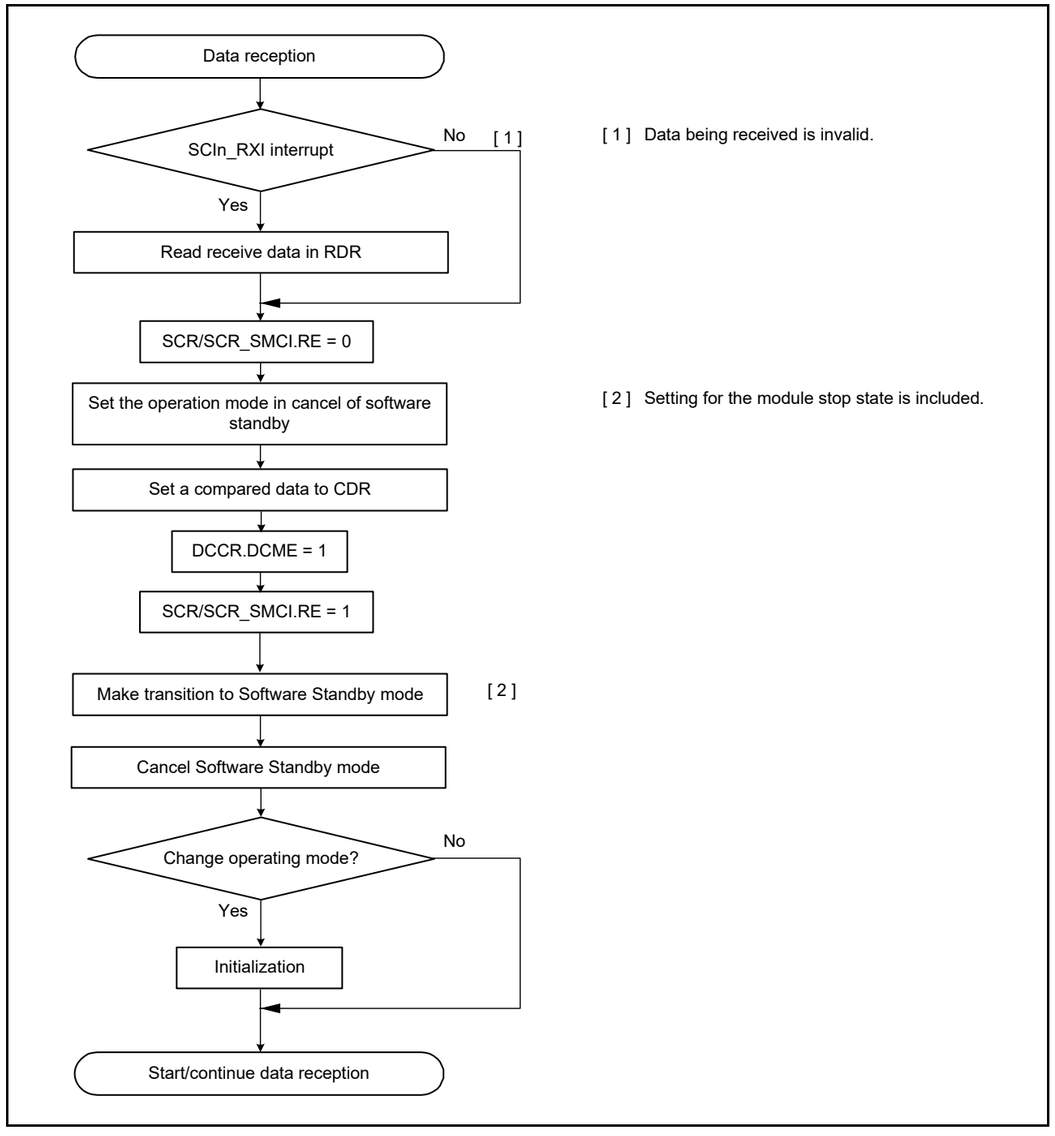
Figure 34.76 Example flow of transition to Software Standby mode during reception



[1]正在接收的数据无效。

[2]包括模块停止状态的设置。

Figure 34.76 接收期间转换到软件待机模式的示例流程



[1] Data being received is invalid.

[2] Setting for the module stop state is included.

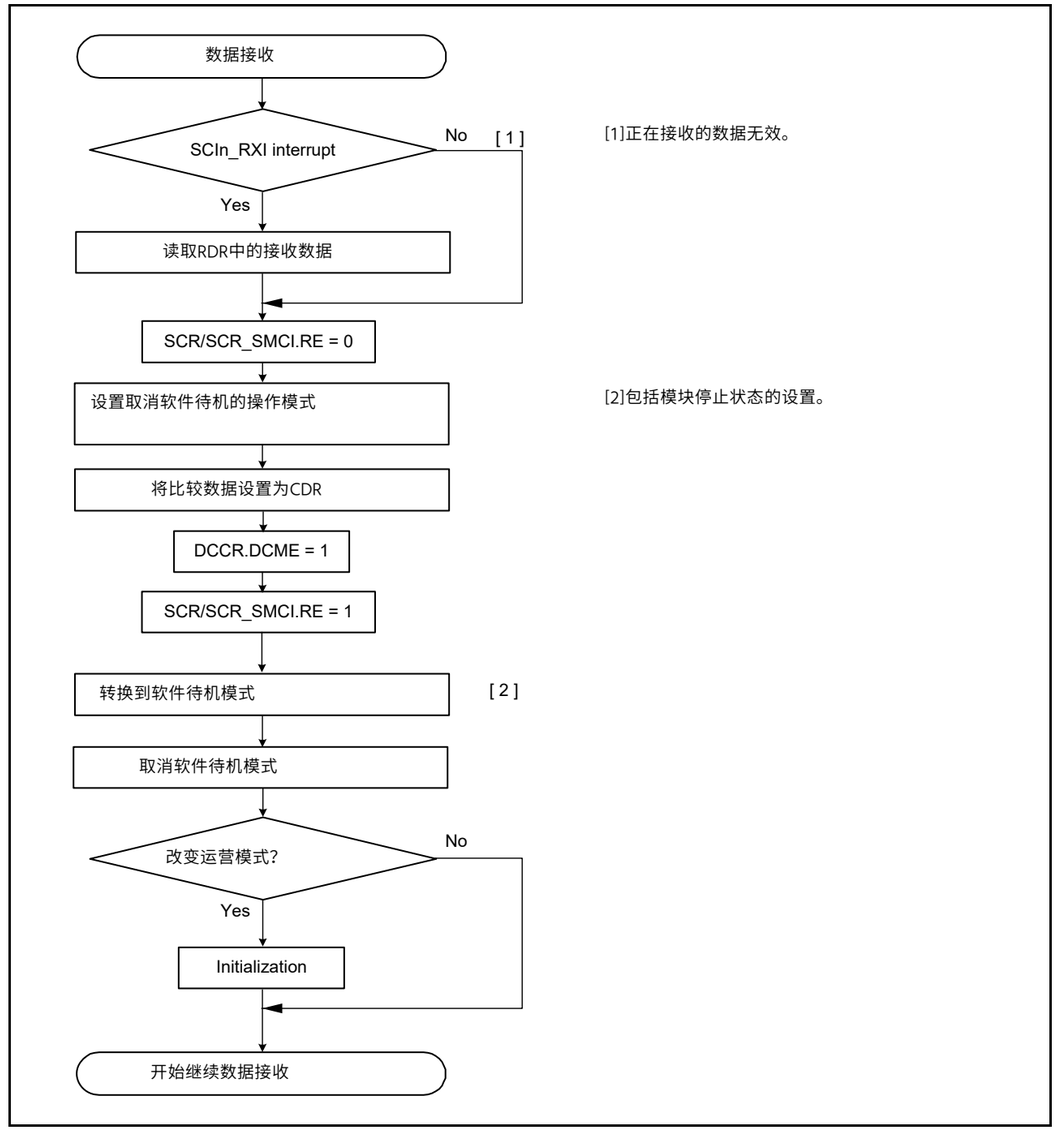
Figure 34.77 Example flow of transition to Software Standby mode during reception with address match

34.14.3 Break Detection and Processing

(1) Non-FIFO selected

When a framing error is detected, a break can be detected by reading the RXDn pin value directly. In a break, the input from the RXDn pin becomes all 0s, and the SSR.FER flag is set to 1 to indicate a framing error, and the SSR.PER flag might also be set to 1 to indicate a parity error. The SCI continues the receive operation even after a break is received. Therefore, even if the FER flag is 0, indicating that no framing error occurred, it is set to 1 again. When the SEMR.RXDESEL bit is 1, the SCI sets the SSR.FER flag to 1 and stops receiving operations until a start bit of the next data frame is detected. If the SSR.FER flag is set to 0, the SSR.FER flag retains 0 during the break.

When the RXDn pin is set to 1 and the break ends, detecting the beginning of the start bit on the first falling edge of the



[1]正在接收的数据无效。

[2]包括模块停止状态的设置。

Figure 34.77 在地址匹配的接收期间转换到软件待机模式的示例流程

34.14.3 断裂检测和处理

(1) Non-FIFO selected

当检测到帧错误时，可以通过直接读取RXDn引脚值来检测中断。在中断时，来自RXDn引脚的输入变为全0，并且SSR.FER标志设置为1表示帧错误，SSR.PER标志也可能设置为1表示奇偶校验错误。即使在收到中断后，SCI仍继续接收操作。因此，即使FER标志为0，表示没有发生帧错误，它也会再次设置为1。当。。。的时候

SEMR.RXDESEL位为1，SCI将SSR.FER标志设置为1，并停止接收操作，直到检测到下一个数据帧的起始位。如果SSR.FER标志设置为0，则SSR.FER标志在中断期间保持0。

当RXDn引脚设置为1且中断结束时，在第一个下降沿检测起始位的开始

RXDn pin allows the SCI to start the receiving operation.

(2) FIFO selected

After a framing error is detected and when the SCI detects that continuous receive data is 0 for 1 frame, reception stops. When a framing error is detected, a break can be detected by reading the SPTR.RXDMON bit value. After the RXD signal is in the mark state and the break is finished, data reception to the FRDRHL register resumes.

34.14.4 Mark State and Production of Breaks

When the SCR/SCR_SMCI.TE bit is 0, disabling serial transmission, the state of the TXDn pin can be set using the SPTR.SPB2IO and SPTR.SPB2DT bits. With this approach, a TXDn pin can be placed in the mark state to transmit a break.

Before setting the SCR/SCR_SMCI.TE bit to 1, enabling serial transmission, set the SPB2IO and SPB2DT bits to put the communication line in the mark state (the state of 1), and change the TxDn pin using I/O port function. To output a break on data transmission, after setting the TXDn pin to output 0 by setting the SPB2IO and SPB2DT bits, change the TXDn pin using the I/O port function and set the SCR/SCR_SMCI.TE bit to 0. When the SCR/SCR_SMCI.TE bit is set to 0, the transmitter is initialized regardless of the current state of transmission.

34.14.5 Receive Error Flags and Transmit Operation in Clock Synchronous and Simple SPI Modes

Transmission cannot start when a receive error flag (ORER) in SSR/SSR_FIFO is set to 1, even when data is written to TDR or FTDRL*2. Always set the receive error flags to 0 before starting transmission.

Note 1. The receive error flags cannot be set to 0 when serial reception is disabled by setting the RE bit in SCR/SCR_SMCI to 0.
Note 2. Do not use the FTDRH register in simple SPI mode.

34.14.6 Restrictions on Clock Synchronous Transmission in Clock Synchronous and Simple SPI Modes

When the external clock source is used as a synchronization clock, the following restrictions apply.

(1) Start of transmission

Wait at least the following time from writing transmit data to TDR to the start of the external clock input:
1 PCLKA cycle + data output delay time for the slave (t_{DO}) + setup time for the master (t_{SU}). See Figure 34.78.

(2) Continuous transmission

Write the next transmit data to TDR or TDRHL before the falling edge of the transmit clock for bit [7] (see Figure 34.78).

When updating TDR after bit [7] has started to transmit, update TDR while the synchronization clock is in the low-level period, and set the high-level width of the transmit clock (bit [7]) to 4 PCLKA cycles or longer (see Figure 34.78).

RXDn引脚允许SCI开始接收操作。

(2) FIFO selected

检测到帧错误后，当SCI检测到1帧连续接收数据为0时，接收停止。
当检测到帧错误时，可以通过读取SPTR.RXDMON位的值来检测中断。在RXD信号处于标记状态且中断完成后，FRDRHL寄存器的数据接收恢复。

34.14.4 标记状态和产生的中断

当SCRSCR_SMCI.TE位为0时，禁用串行传输，TXDn引脚的状态可以使用SPTR.SPB2IO和SPTR.SPB2DT位。使用这种方法，可以将TXDn引脚置于标记状态以发送中断。

在设置SCRSCR_SMCI.TE位为1，使能串行传输之前，设置SPB2IO和SPB2DT位使通信线处于标记状态（状态为1），并使用IO端口功能更改TxDn引脚。要输出数据传输中断，通过设置SPB2IO和SPB2DT位将TXDn引脚设置为输出0后，使用IO端口功能更改TXDn引脚并将SCRSCR_SMCI.TE位设置为0。当SCRSCR_SMCI.TE位设置为0，无论当前的传输状态如何，都初始化发送器。

34.14.5 在时钟同步和简单的接收错误标志和发送操作 SPI模式

当SSRSSR_FIFO中的接收错误标志(ORER)设置为1时，传输无法开始，即使数据已写入TDR或FTDRL*2。在开始传输之前，始终将接收错误标志设置为0。

注1.当通过设置RE位禁用串行接收时，接收错误标志不能设置为0 SCR/SCR_SMCI to 0.
注2.不要在简单SPI模式下使用FTDRH寄存器。

34.14.6 时钟同步和时钟同步传输的限制 简单的SPI模式

当外部时钟源用作同步时钟时，有以下限制。

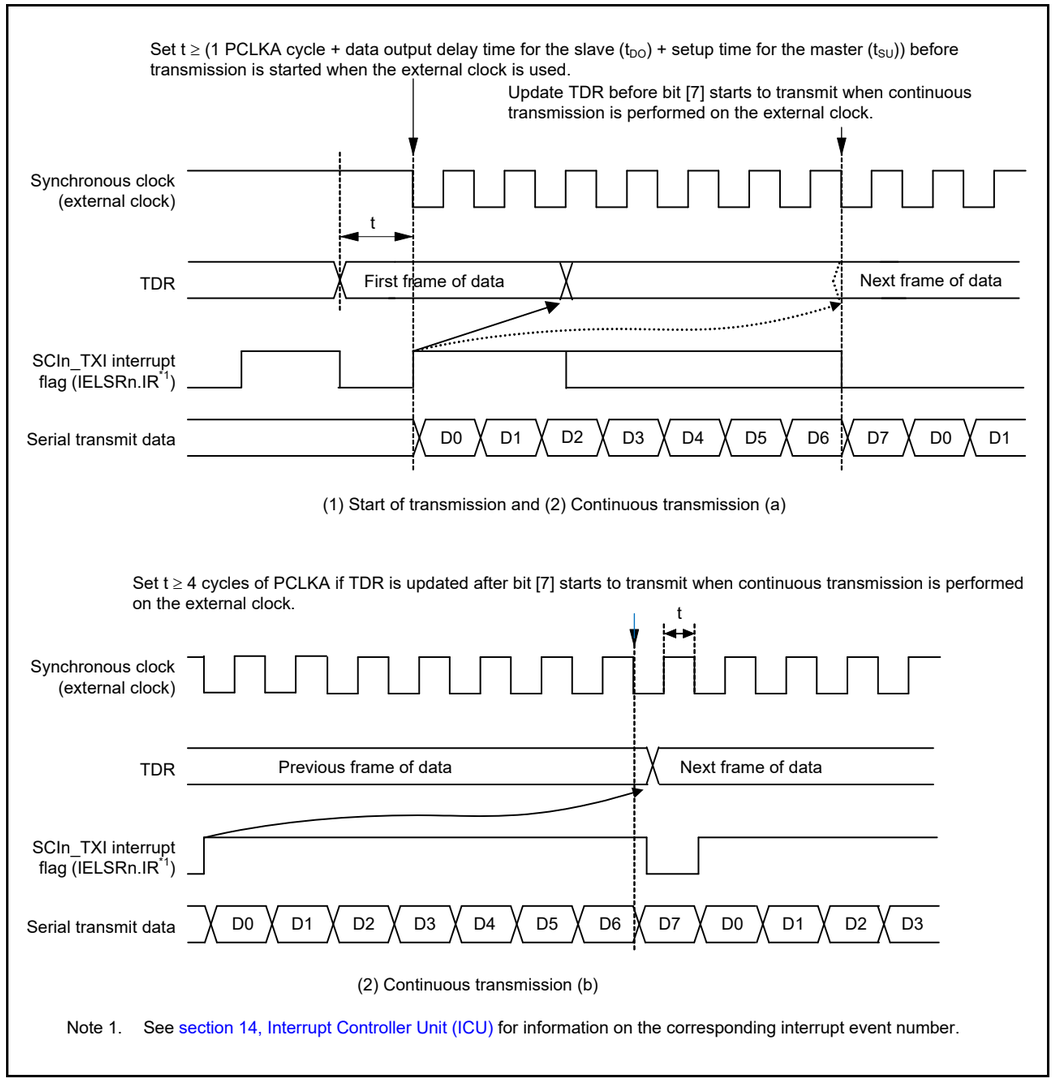
(1) 传输开始

从将发送数据写入TDR到开始外部时钟输入，至少等待以下时间：1个PCLKA周期+从设备的数据输出延迟时间(tDO)+主设备的建立时间(tSU)。请参见图34.78。

(2) 连续传输

在位[7]的发送时钟下降沿之前将下一个发送数据写入TDR或TDRHL（参见图34.78）。

在bit[7]开始发送后更新TDR时，在同步时钟处于低电平期间更新TDR，并将发送时钟（bit[7]）的高电平宽度设置为4个PCLKA周期或更长（见图34.78）。



Note 1. See section 14, Interrupt Controller Unit (ICU) for information on the corresponding interrupt event number.

Figure 34.78 Restrictions on use of external clock in clock synchronous transmission

34.14.7 Restrictions on Using DMAC or DTC

During transmission or reception operations using the DMAC or DTC, do not set transfer data for the DMAC/DTC.

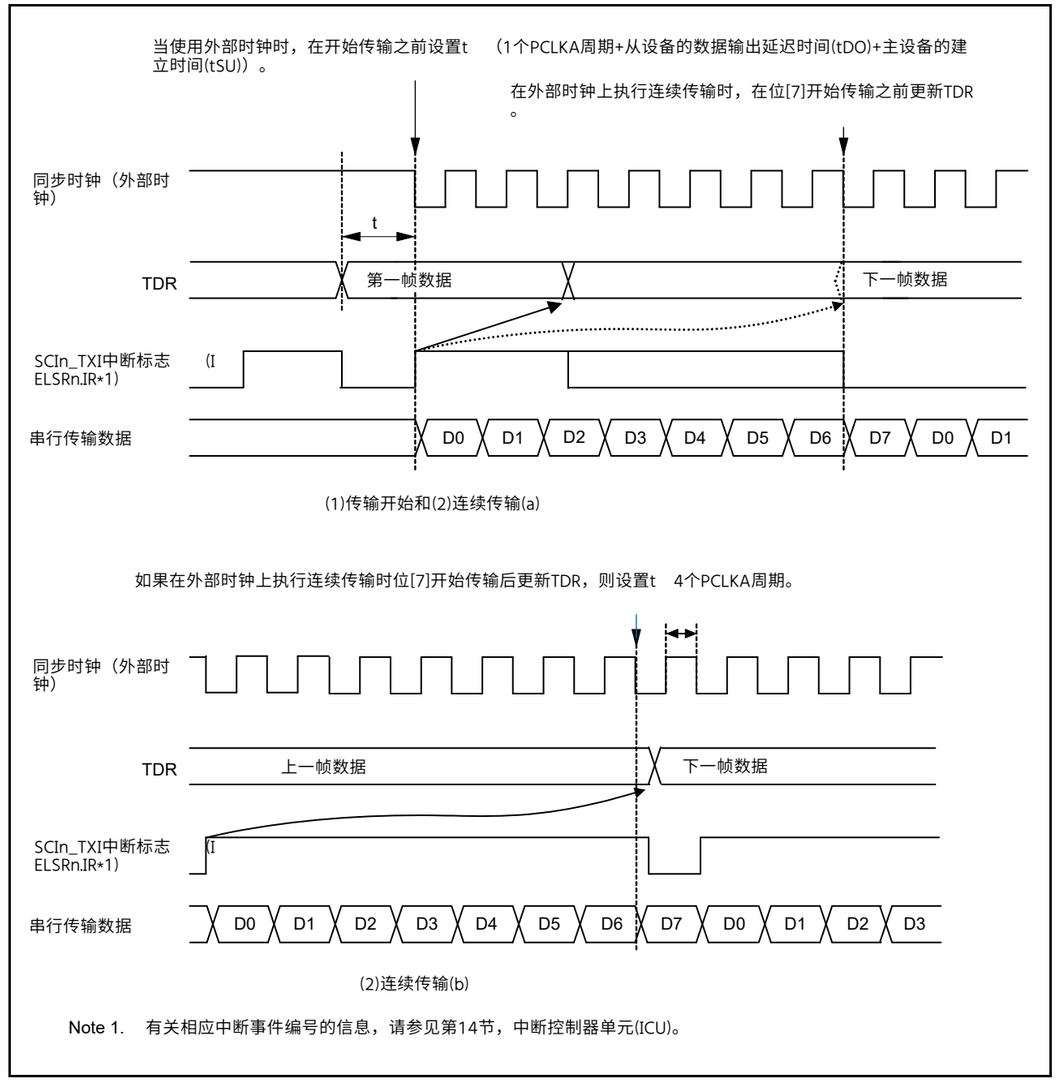
(1) Writing data to TDR (FTDRHL)

(a) Non-FIFO selected

Data can be written to TDR and TDRHL. However, if new data is written to TDR or TDRHL when transmit data remains in TDR or TDRHL, the previous data in TDR and TDRHL is lost because it was not transferred to TSR yet. When using DTC or DMAC, always write transmit data to TDR or TDRHL in the SCIn_TXI interrupt request handling routine.

(b) FIFO selected

It is possible to write data to the FTDRH and FTDRL registers when SCR.TE is 1. Confirm the amount of writable data



Note 1. 有关相应中断事件编号的信息，请参见第14节，中断控制器单元(ICU)。

Figure 34.78 时钟同步传输中使用外部时钟的限制

34.14.7 使用DMAC或DTC的限制

在使用DMAC或DTC进行发送或接收操作期间，请勿为DMACDTC设置传输数据。

(1) 将数据写入TDR(FTDRHL)

(a) Non-FIFO selected

数据可以写入TDR和TDRHL。但是，如果在发送数据保留在TDR或TDRHL中时将新数据写入TDR或TDRHL，则TDR和TDRHL中的先前数据将丢失，因为它尚未传输到TSR。使用DTC或DMAC时，始终在SCIn_TXI中断请求处理程序中将发送数据写入TDR或TDRHL。

(b) FIFO selected

当SCR.TE为1时，可以将数据写入FTDRH和FTDRL寄存器。确认可写入数据量

using the FDR.T[4:0] bits.

(2) Reading data from RDR (FRDRHL)

When using the DMAC or DTC to read RDR and RDRHL, always set the receive data full interrupt (SCIn_RXI) as the activation source of the relevant SCI.

34.14.8 Notes on Starting Transfer

When transfer starts while the Interrupt Status flag (IELSRn.IR) in the ICU is 1, follow the procedure in this section to clear interrupt requests before permitting operations (by setting the SCR/SCR_SMCI.TE or SCR/SCR_SMCI.RE bit to 1). For details on the Interrupt Status flag, see section 14, Interrupt Controller Unit (ICU).

- Confirm that transfer has stopped (the SCR/SCR_SMCI.TE or SCR/SCR_SMCI.RE bit is 0)
- Set the associated interrupt enable bit (SCR/SCR_SMCI.TIE or SCR/SCR_SMCI.RIE) to 0
- Read the associated interrupt enable bit (SCR/SCR_SMCI.TIE or SCR/SCR_SMCI.RIE bit) to check that it actually becomes 0
- Set the Interrupt Status flag, IELSRn.IR, in the ICU to 0.

34.14.9 External Clock Input in Clock Synchronous and Simple SPI Modes

In clock synchronous mode and simple SPI mode, the external clock (SCKn) must be input as follows:

High-pulse period, low-pulse period = 2 PCLKA cycles or more, period = 6 PCLKA cycles or more.

34.14.10 Limitations on Simple SPI Mode

(1) Master mode

- Use a resistor to pull up or pull down the clock line matching the initial settings for the transfer clock set in the SPMR.CKPH and CKPOL bits when the SPMR.SSE bit is 1.

  This prevents the clock line from being placed in the high-impedance state when the SCR.TE bit is set to 0 or unexpected edges from being generated on the clock line when the SCR.TE bit changes from 0 to 1. When the SPMR.SSE bit is 0 in single master mode, pulling up or pulling down the clock line is not required because the clock line is not placed in the high-impedance state even when the SCR.TE bit is set to 0.
- For the clock delay setting (SPMR.CKPH bit is 1), the receive data full interrupt (SCIn_RXI) is generated before the final clock edge on the SCKn pin as indicated in Figure 34.79. If the TE and RE bits in the SCR register become 0 before the final edge of the clock signal on the SCKn pin, the SCKn pin is placed in the high-impedance state, so the width of the last clock pulse of the transfer clock is shortened. Additionally, an SCIn_RXI interrupt might lead to the input signal on the SSn pin of a connected slave going to the high level before the final edge of the clock signal on the SCKn pin, leading to incorrect operation of the slave.
- In a multi-master configuration, the SCKn pin output goes to high-impedance while the input on the SSn pin is at the low level if a mode fault error occurs while a character is being transferred, stopping supply of the clock signal to the connected slave. Reset the connected slave to avoid misaligned bits when transfer is restarted.

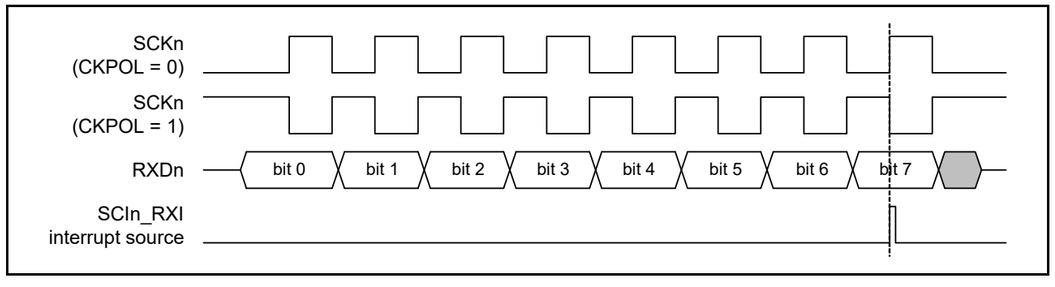


Figure 34.79 Timing of SCIn_RXI interrupt in simple SPI mode with clock delay

使用FDR.T[4:0]位。

(2) 从RDR(FRDRHL)读取数据

使用DMAC或DTC读取RDR和RDRHL时，始终将接收数据满中断（SCIn_RXI）设置为相关SCI的激活源。

34.14.8 开始转移注意事项

当ICU中的中断状态标志(IELSRn.IR)为1时开始传输时，请按照本节中的程序在允许操作之前清除中断请求（通过将SCRSCR_SMCI.TE或SCRSCR_SMCI.RE位设置为1）。有关中断状态标志的详细信息，请参见第14节，中断控制器单元(ICU)。

- 确认传输已停止（SCRSCR_SMCI.TE或SCRSCR_SMCI.RE位为0）
- 将相关的中断使能位（SCRSCR_SMCI.TIE或SCRSCR_SMCI.RIE）设置为0
- 读取相关的中断使能位（SCRSCR_SMCI.TIE或SCRSCR_SMCI.RIE位）以检查它是否实际变为0
- 将ICU中的中断状态标志IELSRn.IR设置为0。

34.14.9 时钟同步和简单SPI模式下的外部时钟输入

在时钟同步模式和简单SPI模式下，外部时钟（SCKn）必须输入如下：

高脉冲周期，低脉冲周期=2个PCLKA周期或更多，周期=6个PCLKA周期或更多。

34.14.10 简单SPI模式的限制

(1) 主模式

- 使用电阻上拉或下拉与传输时钟设置的初始设置相匹配的时钟线SPMR.SSE位为1时的SPMR.CKPH和CKPOL位。

  这可以防止当SCR.TE位设置为0时时钟线处于高阻抗状态，或者当SCR.TE位从0变为1时在时钟线上产生意外边沿。SSE位在单主机模式下为0，不需要上拉或下拉时钟线，因为即使SCR.TE位设置为0，时钟线也不会处于高阻状态。
- 对于时钟延迟设置（SPMR.CKPH位为1），接收数据完全中断（SCIn_RXI）在SCKn引脚上的最终时钟沿之前产生，如图34.79所示。如果SCR寄存器中的TE和RE位在SCKn引脚上的时钟信号的最后一个边沿之前变为0，则SCKn引脚处于高阻状态，因此传输时钟的最后一个时钟脉冲的宽度为缩短。此外，SCIn_RXI中断可能会导致所连接从机的SSn引脚上的输入信号在SCKn引脚上的时钟信号的最后一个边沿之前变为高电平，从而导致从机的错误操作。
- 在多主机配置中，如果在传输字符时发生模式故障错误，则SCKn引脚输出变为高阻态，而SSn引脚上的输入处于低电平，从而停止向连接的时钟信号提供奴隶。重新启动传输时，重置连接的从机以避免未对齐的位。

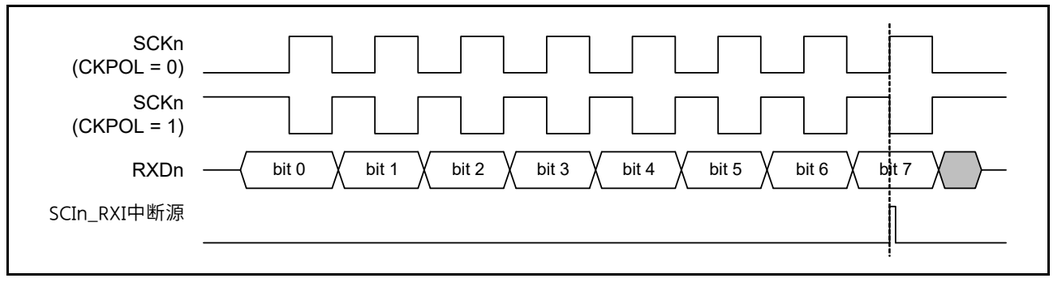


Figure 34.79 带时钟延迟的简单SPI模式下SCIn_RXI中断的时序

(2) Slave mode

- Wait at least the following time from writing transmit data in the TDR register to the start of the external clock input.
  1 PCLKA cycle + data output delay for the slave (tDO) + setup time for the master (tSU)

  Also wait at least 5 PCLKA cycles from the input of the low level on the SSn pin to the start of the external clock input.
- Provide an external clock signal to the master the same as the data length for transfer
- Control the input on the SSn pin before the start and after the end of data transfer
- When the input level on the SSn pin is to be changed from low to high while a character is being transferred, set the TE and RE bits in the SCR register to 0 and, after restoring the settings, restart transfer of the first byte.

(2) 从机模式

- 从将发送数据写入TDR寄存器到开始外部时钟输入，至少等待以下时间。1个PCLKA周期+从机的数据输出延迟(tDO)+主机的建立时间(tSU)

  还要等待至少5个PCLKA周期，从SSn引脚上的低电平输入到外部时钟输入开始。
- 向主机提供与传输数据长度相同的外部时钟信号
- 在数据传输开始之前和结束之后控制SSn引脚上的输入
- 当SSn引脚上的输入电平要在传输字符时从低电平变为高电平时，设置SCR寄存器中的TE和RE位为0，并在恢复设置后重新开始传输第一个字节。

35. IrDA Interface

35.1 Overview

The IrDA interface sends and receives IrDA data communication waveforms in cooperation with the SCI1 based on the IrDA (Infrared Data Association) standard 1.0.

Enabling the IrDA function in the IRE bit in the IRCR register allows encoding and decoding of the TXD1 and RXD1 signals of the SCI1 to the waveforms conforming to the IrDA standard 1.0 (IRTXD1 and IRRXD1 pins). Connecting the waveforms to an infrared transmitter/receiver implements infrared data communication conforming to the IrDA standard 1.0 system.

With the IrDA standard 1.0 system, data transfer can be started at 9,600 bps and the transfer rate can be changed whenever necessary. Because the IrDA interface cannot change the transfer rate automatically, the transfer rate must be changed through the software.

Figure 35.1 shows the cooperation between the IrDA interface and SCI1.

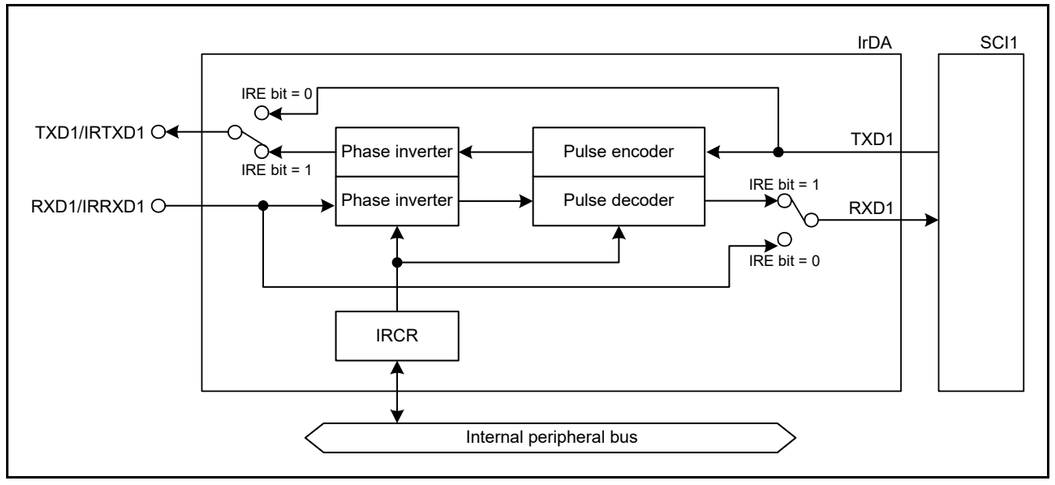


Figure 35.1 Cooperation between the IrDA interface and SCI1

Table 35.1 IrDA interface I/O pins

Pin name	I/O	Function
IRTXD1	Output	Data to be transmitted
IRRXD1	Input	Received data

35. IrDA Interface

35.1 Overview

IrDA接口与SCI1配合发送和接收IrDA数据通信波形，基于
IrDA（红外数据协会）标准1.0。

在IRCR寄存器的IRE位中使能IrDA功能，可以将SCI1的TXD1和RXD1信号编码和解码为符合IrDA标准1.0（IRTXD1和IRRXD1引脚）的波形。将波形连接到红外发射器接收器可实现符合IrDA标准1.0系统的红外数据通信。

使用IrDA标准1.0系统，可以以9 600bps开始数据传输，并且可以随时更改传输速率。因为IrDA接口不能自动改变传输速率，所以必须通过软件来改变传输速率。

图35.1显示了IrDA接口和SCI1之间的配合。

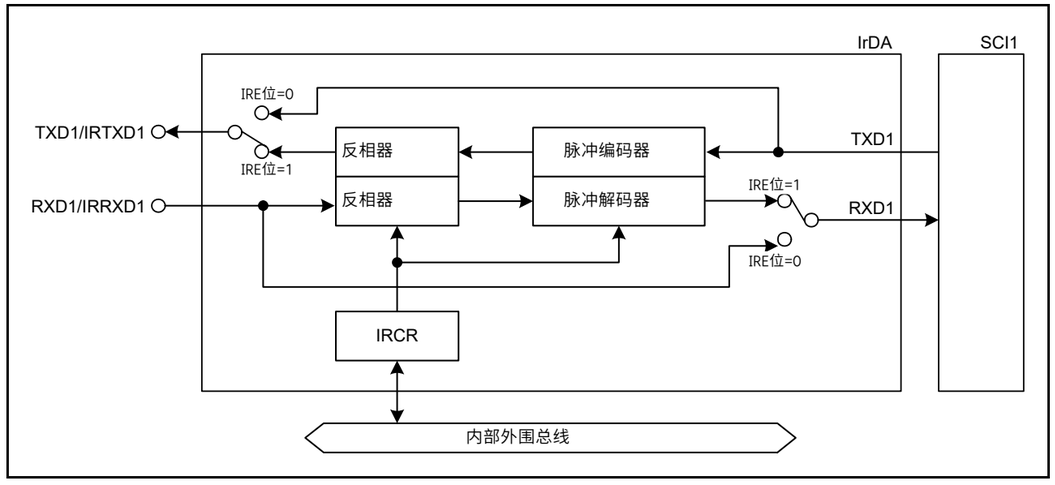


Figure 35.1 IrDA接口与SCI1的合作

Table 35.1 IrDA接口IO引脚

引脚名称	I/O	Function
IRTXD1	Output	要传输的数据
IRRXD1	Input	接收数据

35.2 Register Descriptions

35.2.1 IrDA Control Register (IRCR)

Address(es): IRDA.IRCR 4007 0F00h

	b7	b6	b5	b4	b3	b2	b1	b0
	IRE	—	—	—	IRTXINV	IRRXINV	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b2	IRRXINV	IRRXD Polarity Switching	0: Use IRRXD input as received data as-is 1: Use IRRXD input as received data after the polarity is inverted.	R/W
b3	IRTXINV	IRTXD Polarity Switching	0: Output data to be transmitted to IRTXD as-is 1: Output data to be transmitted IRTXD after the polarity is inverted.	R/W
b6 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	IRE	IrDA Enable	0: Use serial input/output pins for normal serial communication 1: Use serial input/output pins for IrDA data communication.	R/W

Note: The IRCR register values are retained in Sleep, Software Standby, and Deep Software Standby modes.

IRRXINV bit (IRRXD Polarity Switching)

The IRRXINV bit inverts the logic level of the IRRXD input. When inverted, the high-level pulse width is applied to the low-level pulse width.

IRTXINV bit (IRTXD Polarity Switching)

The IRTXINV bit inverts the logic level of the IRTXD output. When inverted, the high-level pulse width is applied to the low-level pulse width.

IRE bit (IrDA Enable)

The IRE bit configures the I/O pins for normal communication mode or IrDA data communication mode.

35.3 Operation

35.3.1 IrDA Interface Setup Procedure

To set up IrDA interface operation:

1. Set the associated pins to IRTXD1 and IRRXD1 in the Pin Function Control Register (PmnPFS.PSEL = 00101b) of the I/O ports function.
2. Specify the peripheral function in the Pin Function Control Register (PmnPFS.PMR = 1) of the I/O ports function.
3. Specify the IrDA function in the IRCR register.
4. Set the SCI1-related registers of the Serial Communications Interface (SCI).

35.3.2 Transmission

During transmission, the signals output from the SCI1 (UART frames) are converted to the IR frame data through the IrDA interface (see Figure 35.2). When the IRCR.IRTXINV bit is 0 and serial data is 0, high-level pulses with 3/16 the width of the bit rate (1-bit width period) are output (initial setting). The standard prescribes that the minimum high-level pulse width must be 1.41 µs and the maximum high-level pulse width must be (3/16 + 2.5%) × bit rate or (3/16 × bit rate) + 1.08 µs. When the serial data is 1, no pulses are output.

35.2 注册说明

35.2.1 IrDA控制寄存器(IRCR)

Address(es): IRDA.IRCR 4007 0F00h

	b7	b6	b5	b4	b3	b2	b1	b0
	IRE	—	—	—	IRTXINV	IRRXINV	—	—
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b1, b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b2	IRRXINV	IRRXD极性切换	0：按原样使用IRRXD输入作为接收数据1：在极性反转后使用IRRXD输入作为接收数据。	R/W
b3	IRTXINV	IRTXD极性切换	0：输出数据按原样发送到IRTXD1：输出数据在极性反转后发送到IRTXD。	R/W
b6 to b4	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b7	IRE	IrDA Enable	0：使用串行输入输出引脚进行正常串行通信1：使用串行输入输出引脚进行IrDA数据通信。	R/W

Note: IRCR寄存器值在休眠、软件待机和深度软件待机模式下保持不变。

IRRXINV位（IRRXD极性切换）

IRRXINV位反转IRRXD输入的逻辑电平。反转时，高电平脉冲宽度应用于低电平脉冲宽度。

IRTXINV位（IRTXD极性切换）

IRTXINV位反转IRTXD输出的逻辑电平。反转时，高电平脉冲宽度应用于低电平脉冲宽度。

IRE位（IrDA使能）

IRE位将IO引脚配置为正常通信模式或IrDA数据通信模式。

35.3 Operation

35.3.1 IrDA接口设置程序

设置IrDA接口操作：

1. 在IO端口功能的引脚功能控制寄存器(PmnPFS.PSEL=00101b)中将相关引脚设置为IRTXD1和IRRXD1。
2. 在IO端口功能的引脚功能控制寄存器(PmnPFS.PMR=1)中指定外设功能。
3. 在IRCR寄存器中指定IrDA功能。
4. 设置串行通信接口(SCI)的SCI1相关寄存器。

35.3.2 Transmission

在传输过程中，从SCI1输出的信号（UART帧）通过IrDA接口（见图35.2）。当IRCR.IRTXINV位为0且串行数据为0时，输出具有316位速率宽度（1位宽度周期）的高电平脉冲（初始设置）。标准规定最小高电平脉冲宽度必须为1.41µs，最大高电平脉冲宽度必须为（316+2.5%）×比特率或（316×比特率）+1.08µs。当串行数据为1时，不输出脉冲。

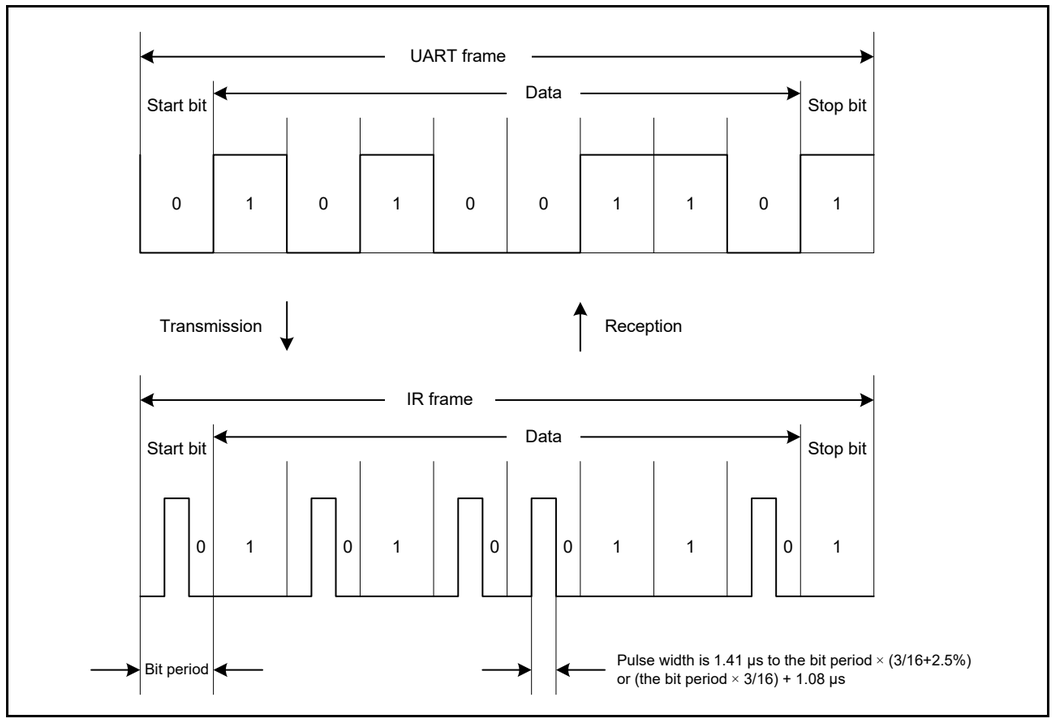


Figure 35.2 IrDA transmission and reception

35.3.3 Reception

During reception, the IR frame data is converted to the UART frame data through the IrDA interface and is input to the SCI1. Low-level data is input to SCI1 when the IRCR.IRRXINV bit is 0 and a high-level pulse is detected. High-level data is input to SCI1 when no pulse is detected for a 1-bit period.

35.4 Usage Notes

35.4.1 Settings for the Module-Stop Function

IrDA operation can be disabled or enabled using the Module Stop Control Register. The IrDA is initially stopped after reset. Releasing the module-stop state enables access to the registers. For details, see section 11, Low Power Modes.

35.4.2 Asynchronous Reference Clock for SCI1

The IrDA receives a clock with a frequency 16 times the bit rate from SCI1 and operates in conjunction with SCI1. When using the IrDA, set the SCI1.SEMR.ABCS bit to 0.

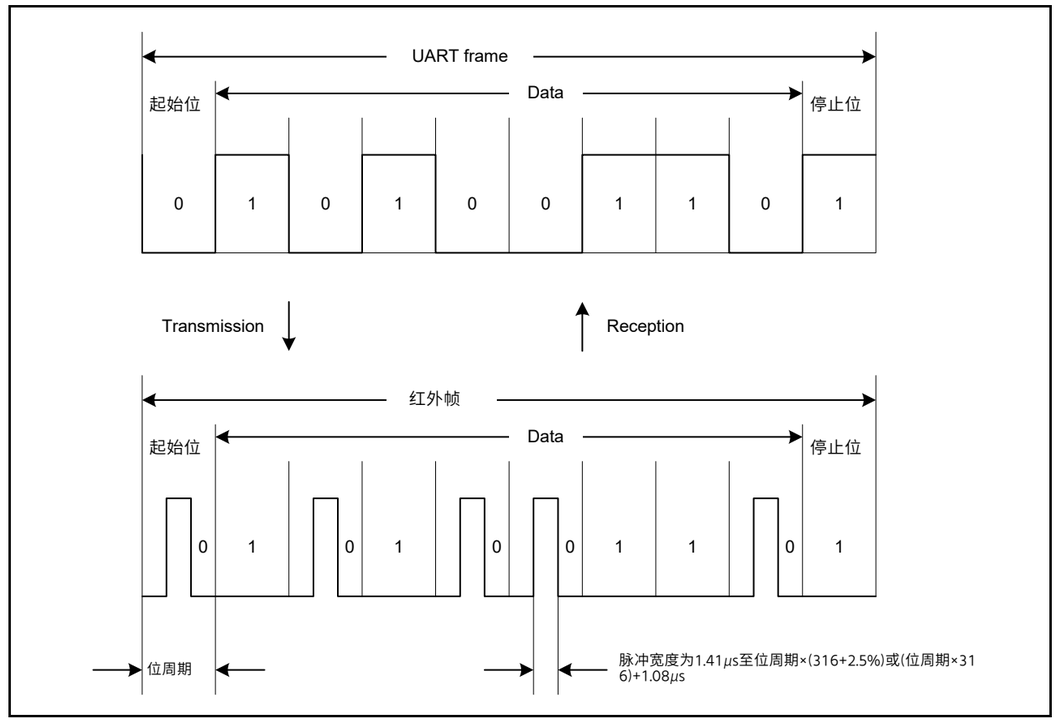


Figure 35.2 IrDA发射和接收

35.3.3 Reception

接收时，IR帧数据通过IrDA接口转换为UART帧数据，输入到SCI1。当IRCR.IRRXINV位为0且检测到高电平脉冲时，低电平数据输入到SCI1。当1位周期内没有检测到脉冲时，高电平数据输入到SCI1。

35.4 使用说明

35.4.1 模块停止功能的设置

可以使用模块停止控制寄存器禁用或启用IrDA操作。IrDA在复位后最初停止。释放模块停止状态可以访问寄存器。有关详细信息，请参阅第11节，低功耗模式。

35.4.2 SCI1的异步参考时钟

IrDA从SCI1接收频率为比特率16倍的时钟，并与SCI1一起工作。使用IrDA时，将SCI1.SEMR.ABCS位设置为0。

36. I2C Bus Interface (IIC)

36.1 Overview

The 3-channel I2C Bus Interface (IIC) module conforms with and provides a subset of the NXP I2C bus (inter-integrated circuit bus) interface functions. Table 36.1 lists the IIC specifications, Figure 36.1 shows a block diagram, and Figure 36.2 shows an example of I/O pin connections to external circuits, with an I2C bus configuration. Table 36.2 lists the I/O pins.

Table 36.1 IIC specifications (1 of 2)

Parameter	Specifications
Communications format	• I2C-bus format or SMBus format • Master or slave mode selectable • Automatic securing of the setup times, hold times, and bus-free times for the transfer rate
Transfer rate	Fast-mode Plus supported, up to 1 Mbps
SCL clock	For master operation, the duty cycle of the SCL clock is selectable in the range from 4% to 96%
Issuing and detecting conditions	• Start, restart, and stop conditions are automatically generated • Start conditions (including restart conditions) and stop conditions are detectable
Slave address	• Configurable for up to three different slave addresses • 7- and 10-bit address formats supported, including simultaneous use • General call addresses, device ID addresses, and SMBus host addresses detectable
Acknowledgment	• For transmission, automatic loading of the acknowledge bit Transfer of the next transmit data can be automatically suspended on detection of a not-acknowledge bit. • For reception, automatical transmission of the acknowledge bit If a wait between the eighth and ninth clock cycles is selected, the software can control the value in the acknowledge field in response to the received value.
Wait function	During reception, the following wait periods are available by holding the SCL clock low: • Waiting between the eighth and ninth clock cycles • Waiting between the ninth clock cycle and the first clock cycle of the next transfer
SDA output delay function	Output timing of transmitted data, including the acknowledge bit, can be delayed
Arbitration	• For multi-master operation: - SCL clock synchronization is possible when conflict occurs with the SCL signal from another master - When issuing the start condition would create conflict on the bus, loss of arbitration is detected by testing for non-matching between the internal signal for the SDA line and the level on the SDA line - In master operation, loss of arbitration is detected by testing for non-matching between the signal on the SDA line and the internal signal for the SDA line • Loss of arbitration because the start condition occurs while the bus is busy is detectable, to prevent the issuing of double start conditions • Loss of arbitration is detectable on transfer of a not-acknowledge bit because the internal signal for the SDA line and the level on the SDA line do not match • Loss of arbitration because non-matching of internal and line levels for data is detectable in slave transmission
Timeout function	Internal detection of long-interval stops of the SCL clock
Noise cancellation	• Digital noise filters for both the SCL and SDA signals • Programmable window for noise cancellation by the filters
Interrupt sources	• Transfer error or event occurrence (arbitration-lost, NACK, timeout, start or restart condition, or stop condition) • Receive data full, including matching with a slave address • Transmit data empty, including matching with a slave address • Transmit end
Module-stop function	Module-stop state can be set to reduce power consumption
IIC operating modes	• Master transmit • Master receive • Slave transmit • Slave receive

36. I2C总线接口(IIC)

36.1 Overview

3通道I2C总线接口(IIC)模块符合并提供NXPI2C总线（集成电路间总线）接口功能的子集。表36.1列出了IIC规范，图36.1显示了框图，图36.2显示了IO引脚连接到外部电路的示例，具有I2C总线配置。表36.2列出了IO引脚。

Table 36.1 IIC规格(1of2)

Parameter	Specifications
通讯格式	I2C总线格式或SMBus格式 可选择主模式或从模式 自动保护传输速率的设置时间、保持时间和无总线时间
传输率	支持快速模式Plus，最高1Mbps
SCL clock	对于主机操作，SCL时钟的占空比可在4%至96%的范围内选择
发布和检测条件	自动生成启动、重启和停止条件 可检测启动条件（包括重启条件）和停止条件
从机地址	最多可配置三个不同的从地址 支持7位和10位地址格式，包括同时使用 可检测到广播呼叫地址、设备ID地址和SMBus主机地址
Acknowledgment	对于传输，自动加载确认位 检测到未确认位时，可以自动暂停下一个发送数据的传输。 对于接收，确认位的自动传输 如果选择在第8个和第9个时钟周期之间等待，则软件可以控制确认字段中的值以响应接收到的值。
等待功能	在接收期间，通过将SCL时钟保持为低电平可获得以下等待周期： 在第8个和第9个时钟周期之间等待 在第9个时钟周期和下一次传输的第一个时钟周期之间等待
SDA输出延迟功能	传输数据的输出时序，包括确认位，可以延迟
Arbitration	• For multi-master operation: 当与来自另一个主机的SCL信号发生冲突时，SCL时钟同步是可能的当发出启动条件会在总线上产生冲突时，通过测试SDA线的内部信号和ON电平之间的不匹配来检测仲裁丢失SDA线在主机操作中，通过测试SDA线上的信号与SDA线的内部信号之间的不匹配来检测仲裁丢失 可检测到由于在总线繁忙时出现启动条件而导致的仲裁丢失，防止发出双启动条件 由于SDA线的内部信号和SDA线上的电平不匹配，在传输未确认位时可检测到仲裁丢失 由于内部不匹配而导致仲裁丢失从传输中可检测到数据的线路电平
超时功能	内部检测SCL时钟的长间隔停止
噪音消除	用于SCL和SDA信号的数字噪声滤波器 用于通过滤波器消除噪声的可编程窗口
中断源	传输错误或事件发生（仲裁丢失、NACK、超时、启动或重启条件或停止条件） 接收数据已满，包括与从地址匹配 传输数据为空，包括与从地址匹配 传输结束
Module-stop function	可设置模块停止状态以降低功耗
IIC操作模式	主机发送 主机接收 从机发送 从机接收

Table 36.1 IIC specifications (2 of 2)

Parameter	Specifications
Event link function (output)	• Transfer error or event occurrence (arbitration-lost, NACK, timeout, start or restart condition, or stop condition) • Receive data full, including matching with a slave address • Transmit data empty, including matching with a slave address • Transmit end
Wakeup function*1	CPU can return from Software Standby mode using a wakeup event

Note 1. Only supported for IIC0. IIC1 and IIC2 are not supported.

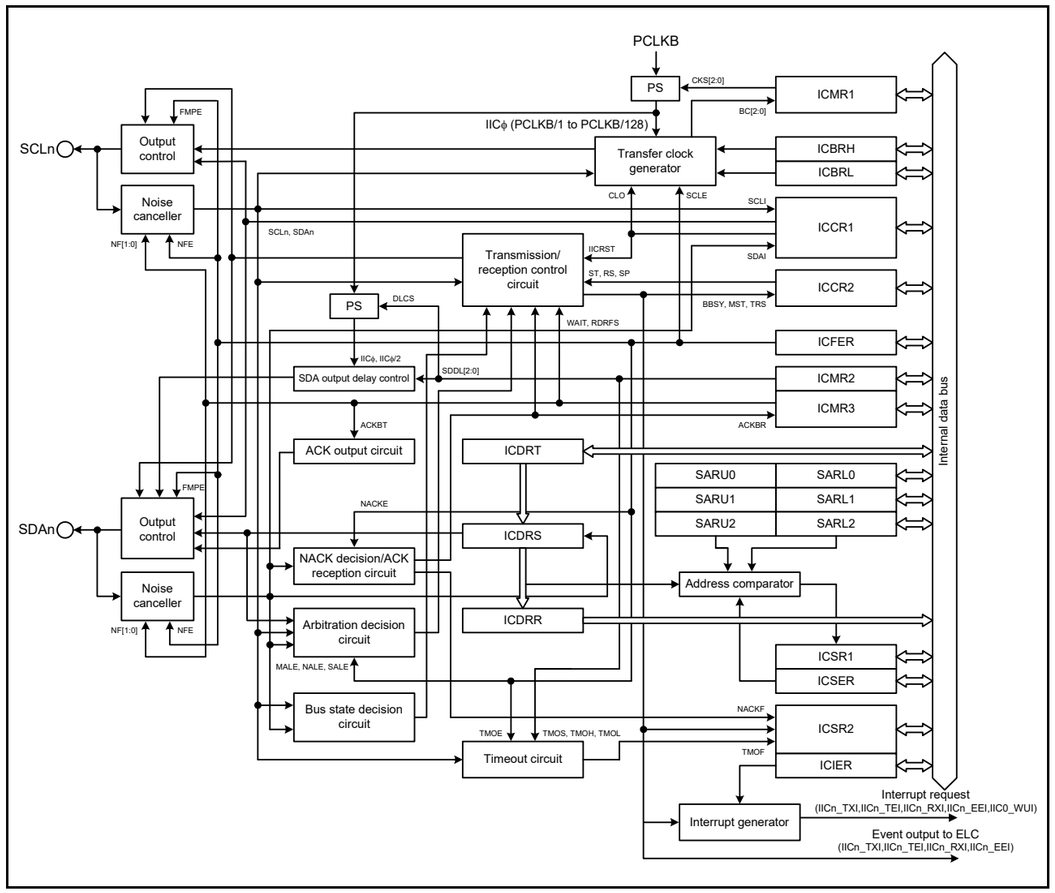


Figure 36.1 IIC block diagram

Table 36.1 IIC规格（2个中的2个）

Parameter	Specifications
事件链接功能（输出）	传输错误或事件发生（仲裁丢失、NACK、超时、启动或重启条件或停止条件） 接收数据已满，包括与从地址匹配 传输数据为空，包括与从地址匹配 传输结束
Wakeup function*1	CPU可以使用唤醒事件从软件待机模式返回

注1.仅支持IIC0。不支持IIC1和IIC2。

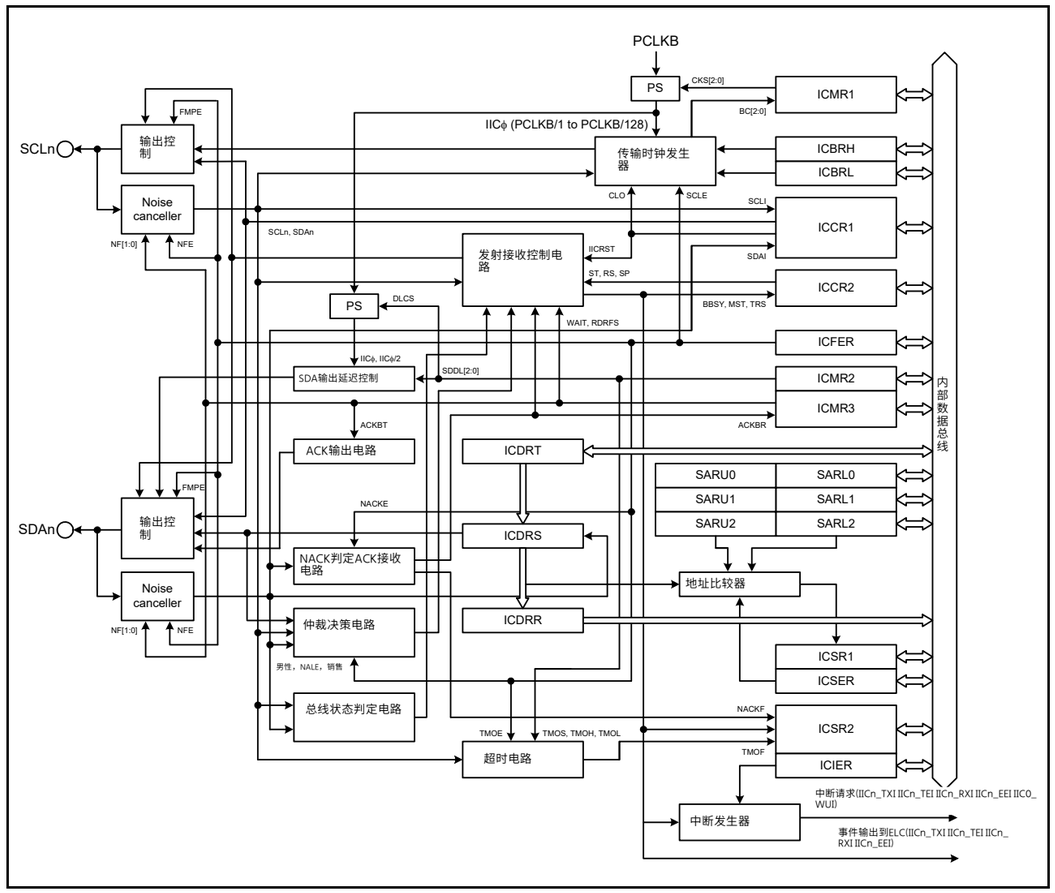


Figure 36.1 IIC框图

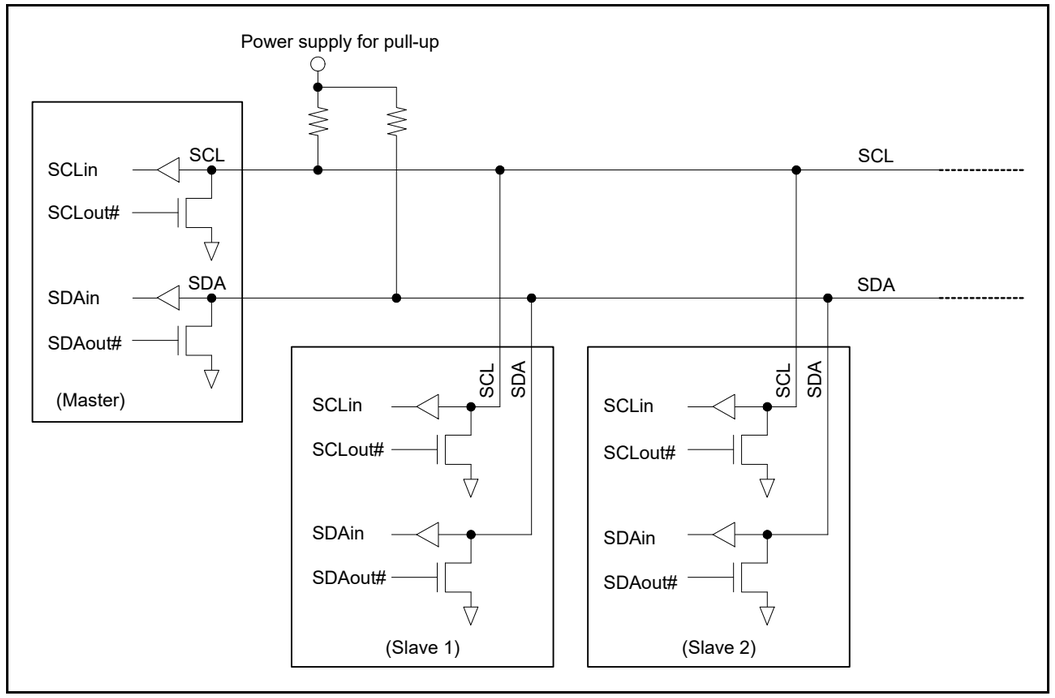


Figure 36.2 I/O pin connection to an external circuit (I2C bus configuration example)

The input level of the signals for IIC is CMOS when I2C bus is selected (ICMR3.SMBS = 0), or TTL when SMBus is selected (ICMR3.SMBS = 1).

Table 36.2 IIC I/O pins

Channel	Pin name	I/O	Function
IIC0	SCL0	I/O	IIC0 serial clock input/output pin
	SDA0	I/O	IIC0 serial data input/output pin
IIC1	SCL1	I/O	IIC1 serial clock input/output pin
	SDA1	I/O	IIC1 serial data input/output pin
IIC2	SCL2	I/O	IIC2 serial clock input/output pin
	SDA2	I/O	IIC2 serial data input/output pin

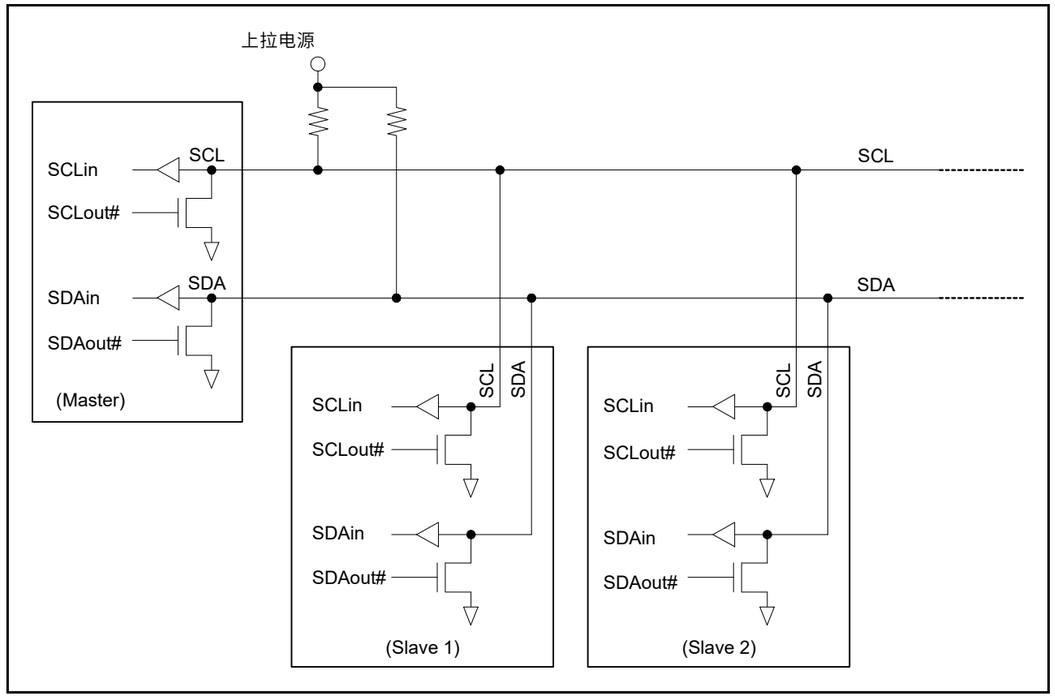


Figure 36.2 IO引脚连接到外部电路（I2C总线配置示例）

TheinputlevelofthesignalsforIICisCMOSwhenI2Cbusisselected(ICMR3.SMBS=0) orTTLwhenSMBusisselected(ICMR3.SMBS=1).

Table 36.2 IIC I/O pins

Channel	引脚名称	I/O	Function
IIC0	SCL0	I/O	IIC0串行时钟输入输出引脚
	SDA0	I/O	IIC0串行数据输入输出引脚
IIC1	SCL1	I/O	IIC1串行时钟输入输出引脚
	SDA1	I/O	IIC1串行数据输入输出引脚
IIC2	SCL2	I/O	IIC2串行时钟输入输出引脚
	SDA2	I/O	IIC2串行数据输入输出引脚

36.2 Register Descriptions

36.2.1 I2C Bus Control Register 1 (ICCR1)

Address(es): IIC0.ICCR1 4005 3000h, IIC1.ICCR1 4005 3100h, IIC2.ICCR1 4005 3200h

	b7	b6	b5	b4	b3	b2	b1	b0
	ICE	IICRST	CLO	SOWP	SCLO	SDAO	SCLI	SDAI
Value after reset:	0	0	0	1	1	1	1	1

Bit	Symbol	Bit name	Description	R/W
b0	SDAI	SDA Line Monitor	0: SDAn line is low 1: SDAn line is high.	R
b1	SCLI	SCL Line Monitor	0: SCLn line is low 1: SCLn line is high.	R
b2	SDAO	SDA Output Control/Monitor	• Read: 0: IIC drove SDAn pin low 1: IIC released SDAn pin. • Write: 0: Drive SDAn pin low through IIC 1: Release SDAn pin through IIC.	R/W
b3	SCLO	SCL Output Control/Monitor	• Read: 0: IIC drove SCLn pin low 1: IIC released SCLn pin. • Write: 0: Drive SCLn pin low through IIC 1: Release SCLn pin through IIC. Use an external pull-up resistor to drive the signal high.	R/W
b4	SOWP	SCLO/SDAO Write Protect	0: Write enable SCLO and SDAO bits 1: Write protect SCLO and SDAO bits. This bit is read as 1.	R/W
b5	CLO	Extra SCL Clock Cycle Output	0: Do not output extra SCL clock cycle (default) 1: Output extra SCL clock cycle. This bit clears automatically after one clock cycle is output.	R/W
b6	IICRST	IIC-Bus Interface Internal Reset	0: Release IIC reset or internal reset 1: Initiate IIC reset or internal reset. This setting clears the bit counter and the SCLn/SDAn output latch.	R/W
b7	ICE	IIC-Bus Interface Enable	0: Disable (SCLn and SDAn pins in inactive state) 1: Enable (SCLn and SDAn pins in active state). Combined with the IICRST bit to select either IIC or internal reset.	R/W

SDAO bit (SDA Output Control/Monitor) and SCLO bit (SCL Output Control/Monitor)

The SDAO bit directly controls the SDAn and SCLn signals output from the IIC. When writing to these bits, also write 0 to the SOWP bit. Setting these bits results in input to the IIC by the input buffer. When slave mode is selected, a start condition might be detected and the bus might be released, depending on the bit settings.

Do not rewrite these bits during a start condition, stop condition, restart condition, transmission, or reception. Operation after rewriting under these conditions is not guaranteed. When reading these bits, the state of signals output from the IIC can be read.

CLO bit (Extra SCL Clock Cycle Output)

The CLO bit allows output of an extra SCL clock cycle for debugging or error processing. Normally, set the bit to 0. Setting the bit to 1 in a normal communication state causes a communication error. For details on this function, see section 36.12.2, Extra SCL Clock Cycle Output Function.

IICRST bit (IIC-Bus Interface Internal Reset)

The IICRST bit initiates an internal state reset of the IIC. Setting this bit to 1 initiates an IIC reset or internal reset.

36.2 注册说明

36.2.1 I2C总线控制寄存器1(ICCR1)

Address(es): IIC0.ICCR1 4005 3000h, IIC1.ICCR1 4005 3100h, IIC2.ICCR1 4005 3200h

	b7	b6	b5	b4	b3	b2	b1	b0
	ICE	IICRST	CLO	SOWP	SCLO	SDAO	SCLI	SDAI
重置后的值：	0	0	0	1	1	1	1	1

Bit	Symbol	位名称	Description	R/W
b0	SDAI	SDA线路监视器	0：SDAn线为低电平1 ：SDAn线为高电平。	R
b1	SCLI	SCL线路监视器	0：SCLn线低1：SC Ln线高。	R
b2	SDAO	SDA Output Control/Monitor	• Read: 0：IIC将SDAn引脚拉低1：I C释放SDAn引脚。 写： 0：通过IIC将SDAn引脚驱动为低 电平1：通过IIC释放SDAn引脚。	R/W
b3	SCLO	SCL Output Control/Monitor	• Read: 0：IIC将SCLn引脚拉低1：I C释放SCLn引脚。 写： 0：通过IIC将SCLn引脚驱动为低电平1：通过IIC释放SC Ln引脚。使用外部上拉电阻将信号驱动为高电平。	R/W
b4	SOWP	SCLOSDAO写保护	0：写使能SCLO和SDAO位1：写保护S CLO和SDAO位。该位读为1。	R/W
b5	CLO	额外的SCL时钟周期输出	0：不输出额外的SCL时钟周期（默认）1：输出额外的SCL 时钟周期。该位在输出一个时钟周期后自动清零。	R/W
b6	IICRST	IIC总线接口内部 Reset	0：释放IIC复位或内部复位1：启动IIC复位或内部复位。该设置清除 位计数器和SCLnSDAn输出锁存器。	R/W
b7	ICE	IIC总线接口使能	0：禁用（SCLn和SDAn引脚处于非活动状态）1：启用（SCLn和S DAn引脚处于活动状态）。结合IICRST位选择IIC或内部复位。	R/W

SDAO位（SDA输出控制监视器）和SCLO位（SCL输出控制监视器）

SDAO位直接控制IIC输出的SDAn和SCLn信号。写入这些位时，还要向SOWP位写入0。设置这些位会导致输入缓冲器向IIC输入。选择从模式时，可能会检测到启动条件并释放总线，具体取决于位设置。

不要在开始条件、停止条件、重启条件、发送或接收期间重写这些位。不保证在这些条件下重写后的操作。读取这些位时，可以读取IIC输出的信号状态。

CLO位（额外SCL时钟周期输出）

CLO位允许输出额外的SCL时钟周期用于调试或错误处理。通常，将该位设置为0。
在正常通信状态下将该位设置为1会导致通信错误。有关此功能的详细信息，请参见第36.12.2节，额外SCL时钟周期输出功能。

IICRST位（IIC总线接口内部复位）

IICRST位启动IIC的内部状态复位。将此位设置为1会启动IIC复位或内部复位。

Whether an IIC reset or internal reset is initiated is determined by the settings of this bit in combination with the ICE bit. Table 36.3 lists the IIC resets.

The IIC reset initializes all registers except ICCR1.ICE and ICCR1.IICRST bits, and internal states of the IIC.

The internal reset initializes the following in addition to the internal states of the IIC:

- Bit counter (ICMR1.BC[2:0] bits)
- I2C Bus Shift Register (ICDRS)
- I2C Bus Status Registers (ICSR1 and ICSR2)
- SDAO and SCLO Output Control/Monitor (ICCR1.SCLO and ICCR1.SDAO bits)
- I2C Bus Control Register 2 (except ICCR2.BBSY bit).

For the reset conditions for each register, see section 36.15, State of Registers when Issuing each Condition.

An internal reset initiated with the IICRST bit set to 1 during operation (with the ICE bit set to 1) resets the internal states of the IIC without initializing the port settings and the control and setting registers of the IIC when the bus or IIC hangs up because of a communication error. If the IIC hangs up in a low level output state, resetting the internal states cancels the low level output state and releases the bus with the SCLn pin and SDAn pin at high impedance.

Note: If an internal reset is initiated using the IICRST bit for a bus hang-up that occurs during communication with the master device in slave mode, the slave and master devices might enter different states, because the bit counter information differs. For this reason, do not initiate an internal reset in slave mode. Initiate recovery processing from the master device. If an internal reset is necessary because the IIC hangs up with the SCLn line in a low level output state in slave mode, initiate an internal reset, and then issue a restart condition from the master device, or issue a stop condition and resume communication from the start condition. If communication is restarted by initiating a reset solely in the slave device without issuing a start or restart condition from the master device, synchronization is lost because the master and slave devices operate asynchronously.

Table 36.3 IIC resets

IICRST	ICE	State	Specifications
1	0	IIC reset	Resets all registers except ICCR1.ICE and ICCR1.IICRST bits, and internal states of the IIC
	1	Internal reset	Resets the ICMR1.BC[2:0] bits, the ICSR1, ICSR2, ICDRS registers, and SDAO and SCLO Output Control/Monitor (ICCR1.SCLO and ICCR1.SDAO bits), I2C Bus Control Register 2 (except ICCR2.BBSY bit) and the internal states of the IIC

ICE bit (IIC-Bus Interface Enable)

The ICE bit selects the active or inactive state of the SCLn and SDAn pins. It can also be combined with the IICRST bit to initiate two types of resets. See Table 36.3 for the reset descriptions.

Set the ICE bit to 1 when using the IIC. The SCLn and SDAn pins are placed in the active state when the ICE bit is set to 1. Set the ICE bit to 0 when the IIC is not used. The SCLn and SDAn pins are placed in the inactive state when the ICE bit is set to 0. Do not assign the SCLn or SDAn pin to the IIC when setting up the pin function control. Slave address comparison is performed if the pins are assigned to the IIC.

是IIC复位还是内部复位由该位的设置和ICE位共同决定。
表36.3列出了IIC复位。

IIC复位初始化除ICCR1.ICE和ICCR1.IICRST位之外的所有寄存器，以及IIC的内部状态。

除了IIC的内部状态之外，内部复位还会初始化以下内容：

- 位计数器（ICMR1.BC[2:0]位）
- I2C总线移位寄存器(ICDRS)
- I2C总线状态寄存器（ICSR1和ICSR2）
- SDAO和SCLO输出控制监视器（ICCR1.SCLO和ICCR1.SDAO位）
- I2C总线控制寄存器2（ICCR2.BBSY位除外）。

有关每个寄存器的复位条件，请参阅第36.15节，发出每个条件时的寄存器状态。

在操作期间将IICRST位设置为1（ICE位设置为1）启动的内部复位会在总线或IIC挂起时复位IIC的内部状态，而无需初始化IIC的端口设置以及控制和设置寄存器因为通讯错误。如果IIC在低电平输出状态下挂起，复位内部状态会取消低电平输出状态并释放总线，同时SCLn引脚和SDAn引脚处于高阻态。

Note: 如果在从模式下与主设备通信期间发生的总线挂断使用IICRST位启动内部复位，则从设备和主设备可能会进入不同的状态，因为位计数器信息不同。因此，不要在从模式下启动内部复位。从主设备启动恢复处理。如果由于IIC在从模式下SCLn线处于低电平输出状态而挂起而需要内部复位，则启动内部复位，然后从主设备发出重新启动条件，或者发出停止条件并从主设备恢复通信开始条件。如果通过仅在从设备中启动复位来重新启动通信，而没有从主设备发出启动或重新启动条件，则由于主设备和从设备异步操作而失去同步。

Table 36.3 IIC resets

IICRST	ICE	State	Specifications
1	0	IIC reset	复位除ICCR1.ICE和ICCR1.IICRST位之外的所有寄存器，以及内部状态 IIC
	1	内部复位	复位ICMR1.BC[2:0]位、ICSR1、ICSR2、ICDRS寄存器以及SDAO和SCLO输出控制监视器（ICCR1.SCLO和ICCR1.SDAO位），I2C总线控制 寄存器2（ICCR2.BBSY位除外）和IIC的内部状态

ICE位（IIC总线接口使能）

ICE位选择SCLn和SDAn引脚的有效或无效状态。它也可以与IICRST位组合来启动两种类型的复位。复位说明见表36.3。

使用IIC时将ICE位设置为1。当ICE位设置为1时，SCLn和SDAn引脚处于活动状态。不使用IIC时，将ICE位设置为0。当ICE位设置为0时，SCLn和SDAn引脚处于无效状态。在设置引脚功能控制时，不要将SCLn或SDAn引脚分配给IIC。如果引脚分配给IIC，则执行从地址比较。

36.2.2 I2C Bus Control Register 2 (ICCR2)

Address(es): IIC0.ICCR2 4005 3001h, IIC1.ICCR2 4005 3101h, IIC2.ICCR2 4005 3201h

	b7	b6	b5	b4	b3	b2	b1	b0
	BBSY	MST	TRS	—	SP	RS	ST	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b1	ST	Start Condition Issuance Request	0: Do not issue a start condition request 1: Issue a start condition request.	R/W
b2	RS	Restart Condition Issuance Request	0: Do not issue a restart condition request 1: Issue a restart condition request.	R/W
b3	SP	Stop Condition Issuance Request	0: Do not issue a stop condition request 1: Issue a stop condition request.	R/W
b4	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b5	TRS	Transmit/Receive Mode	0: Receive mode 1: Transmit mode.	R/W*1
b6	MST	Master/Slave Mode	0: Slave mode 1: Master mode.	R/W*1
b7	BBSY	Bus Busy Detection Flag	0: I2C bus released (bus free state) 1: I2C bus occupied (bus busy state).	R

Note 1. The MST and TRS bits can be written to when the ICMR1.MTWP bit is set to 1.

ST bit (Start Condition Issuance Request)

The ST bit requests transition to master mode and triggers a start condition. When this bit is set to 1, a start condition is issued when the BBSY flag is set to 0 (bus free state). For details on this function, see section 36.11, Start, Restart, and Stop Condition Issuing Function.

[Setting condition]

- When 1 is written to the ST bit.

[Clearing conditions]

- When 0 is written to the ST bit
- When a start condition is issued (a start condition is detected)
- When the AL (arbitration-lost) flag in ICSR2 is set to 1
- When 1 is written to the IICRST bit in ICCR1 to apply an IIC reset or an internal reset.

Note: Only set the ST bit to 1 (start condition issuance request) when the BBSY flag is set to 0 (bus free state). Arbitration might be lost if the ST bit is set to 1 (start condition request) when the BBSY flag is 1 (bus busy state).

RS bit (Restart Condition Issuance Request)

The RS bit requests that a restart condition be issued in master mode. When this bit is set to 1 to request a restart condition, a restart condition is issued when the BBSY flag is set to 1 (bus busy state) and the MST bit is set to 1 (master mode). For details on this function, see section 36.11, Start, Restart, and Stop Condition Issuing Function.

[Setting condition]

- When 1 is written to the RS bit with the BBSY flag in ICCR2 set to 1.

[Clearing conditions]

36.2.2 I2C总线控制寄存器2(ICCR2)

Address(es): IIC0.ICCR2 4005 3001h, IIC1.ICCR2 4005 3101h, IIC2.ICCR2 4005 3201h

	b7	b6	b5	b4	b3	b2	b1	b0
	BBSY	MST	TRS	—	SP	RS	ST	—
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	—	Reserved	该位读取为0。写入值应为0。	R/W
b1	ST	开始条件签发 Request	0：不发出启动条件请求1：发出启动条件请求。	R/W
b2	RS	重启条件发布 Request	0：不发出重启条件请求1：发出重启条件请求。	R/W
b3	SP	停止条件发布 Request	0：不发出停止条件请求1：发出停止条件请求。	R/W
b4	—	Reserved	该位读取为0。写入值应为0。	R/W
b5	TRS	Transmit/Receive Mode	0：接收模式1：发送模式。	R/W*1
b6	MST	Master/Slave Mode	0：从模式1：主模式。	R/W*1
b7	BBSY	总线忙检测标志	0：I2C总线释放（总线空闲状态）1：I2C总线占用（总线忙状态）。	R

Note 1. 当ICMR1.MTWP位设置为1时，可以写入MST和TRS位。

ST位（开始条件发布请求）

ST位请求转换到主模式并触发启动条件。当该位设置为1时，当BBSY标志设置为0（总线空闲状态）时发出启动条件。有关此功能的详细信息，请参阅第36.11节“启动、重启和停止条件发出功能”。

[Setting condition]

- 当1写入ST位时。

[Clearing conditions]

- 当0写入ST位时
- 发出启动条件时（检测到启动条件）
- ICSR2中的AL（仲裁失败）标志设置为1时
- 当向ICCR1中的IICRST位写入1时，应用IIC复位或内部复位。

Note: 仅当BBSY标志设置为0（总线空闲状态）时，才将ST位设置为1（开始条件发出请求）。
如果在BBSY标志为1（总线繁忙状态）时将ST位设置为1（开始条件请求），则仲裁可能会丢失。

RS位（重启条件发布请求）

RS位请求在主机模式下发出重启条件。当该位设置为1以请求重新启动条件时，当BBSY标志设置为1（总线繁忙状态）且MST位设置为1（主模式）时，发出重新启动条件。有关此功能的详细信息，请参阅第36.11节“启动、重启和停止条件发出功能”。

[Setting condition]

- 当ICCR2中的BBSY标志设置为1时，将1写入RS位。

[Clearing conditions]

- When 0 is written to the RS bit
- When a restart condition is issued (a start condition is detected)
- When the AL (arbitration-lost) flag in ICSR2 is set to 1
- When 1 is written to the IICRST bit in ICCR1 to apply an IIC reset or an internal reset.

Note: Do not set the RS bit to 1 while issuing a stop condition.
Note: If 1 (restart condition request) is written to the RS bit in slave mode, the restart condition is not issued, but the RS bit remains set to 1. If the operating mode changes to master mode without the bit being cleared, a restart condition might be issued.

SP bit (Stop Condition Issuance Request)

The SP bit requests that a stop condition be issued in master mode. When this bit is set to 1, a stop condition is issued when the BBSY flag is set to 1 (bus busy state) and the MST bit is set to 1 (master mode). For details on this function, see section 36.11, Start, Restart, and Stop Condition Issuing Function.

[Setting condition]

- When 1 is written to the SP bit with both the BBSY flag and the MST bit in ICCR2 set to 1.

[Clearing conditions]

- When 0 is written to the SP bit
- When a stop condition is issued (a stop condition is detected)
- When the AL (arbitration-lost) flag in ICSR2 is set to 1
- When a start condition and a restart condition are detected
- When 1 is written to the IICRST bit in ICCR1 to apply an IIC reset or an internal reset.

Note: Writing to the SP bit is not possible while the BBSY flag is 0 (bus free state).
Note: Do not set the SP bit to 1 while a restart condition is being issued.

TRS bit (Transmit/Receive Mode)

The TRS bit indicates transmit or receive mode. The IIC is in receive mode when the TRS bit is 0 and in transmit mode when the bit is 1. The combination of this bit and the MST bit indicates the operating mode of the IIC.

The value of the TRS bit automatically changes to 1 for transmit mode or 0 for receive mode when a start condition is issued or detected and the R/W# bit is set. Although writing to the TRS bit is possible when the MTWP bit in ICMR1 is set to 1, writing to this bit is not necessary during normal usage.

[Setting conditions]

- When a start condition is issued normally because of a start condition request (when a start condition is detected with the ST bit set to 1)
- When a restart condition is issued normally because of a restart condition request (when a restart condition is detected with the RS bit set to 1)
- When the R/W# bit appended to the slave address is set to 0 in master mode
- When the address received in slave mode matches the address enabled in ICSER, with the R/W# bit set to 1
- When 1 is written to the TRS bit with the MTWP bit in ICMR1 set to 1.

[Clearing conditions]

- When a stop condition is detected
- When the AL (arbitration-lost) flag in ICSR2 is set to 1
- When the R/W# bit appended to the slave address is set to 1 in master mode
- In slave mode, on a match between the received address and the address enabled in ICSER when the value of the

- 当0写入RS位时
- 发出重新启动条件时（检测到启动条件）
- ICSR2中的AL（仲裁失败）标志设置为1时
- 当向ICCR1中的IICRST位写入1时，应用IIC复位或内部复位。

Note: 发出停止条件时不要将RS位设置为1。
Note: 如果在从模式下将1（重新启动条件请求）写入RS位，则不会发出重新启动条件，但RS位保持设置为1。如果操作模式更改为主模式而未清除该位，则重新启动条件可能会发出。

SP位（停止条件发出请求）

SP位请求在主机模式下发出停止条件。当该位设置为1时，当BBSY标志设置为1（总线繁忙状态）且MST位设置为1（主模式）时，发出停止条件。有关此功能的详细信息，请参阅第36.11节“启动、重启和停止条件发出功能”。

[Setting condition]

- 当1写入SP位时，且ICCR2中的BBSY标志和MST位都设置为1。

[Clearing conditions]

- 当0写入SP位时
- 发出停止条件时（检测到停止条件）
- ICSR2中的AL（仲裁失败）标志设置为1时
- 当检测到启动条件和重新启动条件时
- 当向ICCR1中的IICRST位写入1时，应用IIC复位或内部复位。

Note: 当BBSY标志为0（总线空闲状态）时，不能写入SP位。
Note: 发出重启条件时不要将SP位设置为1。

TRS位（发送接收模式）

TRS位指示发送或接收模式。当TRS位为0时IIC处于接收模式，当该位为1时IIC处于发送模式。该位和MST位的组合指示IIC的工作模式。

当发出或检测到启动条件并且设置RW#位时，TRS位的值自动更改为1（发送模式）或0（接收模式）。虽然当ICMR1的MTWP位设置为1时可以写入TRS位，但在正常使用期间不需要写入该位。

[Setting conditions]

- 由于启动条件请求而正常发出启动条件时（在ST位设置为1的情况下检测到启动条件时）
- 由于重新启动条件请求而正常发出重新启动条件时（在RS位设置为1的情况下检测到重新启动条件时）
- 当附加到从地址的RW#位在主模式下设置为0时
- 当从机模式接收到的地址与ICSER中使能的地址匹配时，RW#位设置为1
- 当将1写入TRS位且ICMR1中的MTWP位设置为1时。

[Clearing conditions]

- 检测到停止条件时
- ICSR2中的AL（仲裁失败）标志设置为1时
- 当附加到从地址的RW#位在主模式下设置为1时
- 在从模式下，当接收到的地址与ICSER中启用的地址匹配时，

received R/W# bit is 0, including when the received address is the general call address

- In slave mode, when a restart condition is detected (a restart condition is detected with ICCR2.BBSY = 1 and ICCR2.MST = 0)
- When 0 is written to the TRS bit with the MTWP bit in ICMR1 set to 1
- When 1 is written to the IICRST bit in ICCR1 to apply an IIC reset or an internal reset.

MST bit (Master/Slave Mode)

The MST bit indicates master or slave mode. The IIC is in slave mode when the MST bit is 0 and is in master mode when the bit is 1. The combination of this bit and the TRS bit indicates the operating mode of the IIC.

The value of the MST bit automatically changes to 1 for master mode or 0 for slave mode when a start condition is issued or a stop condition is issued or detected. Although writing to the MST bit is possible when the MTWP bit in ICMR1 is set to 1, writing to this bit is not necessary during normal usage.

[Setting conditions]

- When a start condition is issued normally because of a start condition request (when a start condition is detected with the ST bit set to 1)
- When 1 is written to the MST bit with the MTWP bit in ICMR1 set to 1.

[Clearing conditions]

- When a stop condition is detected
- When the AL (arbitration-lost) flag in ICSR2 is set to 1
- When 0 is written to the MST bit with the MTWP bit in ICMR1 set to 1
- When 1 is written to the IICRST bit in ICCR1 to apply an IIC reset or an internal reset.

BBSY flag (Bus Busy Detection Flag)

The BBSY flag indicates whether the I2C bus is occupied (bus busy state) or released (bus free state). The flag is set to 1 when the SDAn line changes from high to low when the SCLn line is high, assuming that a start condition was issued. The flag then is set to 0 if a start condition is not detected for the bus free time (ICBRL setting), assuming that a stop condition was issued.

[Setting condition]

- When a start condition is detected.

[Clearing conditions]

- When a start condition is not detected for the bus free time (ICBRL setting) after detecting a stop condition
- When 1 is written to the IICRST bit in ICCR1 with the ICE bit in ICCR1 set to 0 (IIC reset).

接收到的RW#位为0，包括接收到的地址是广播地址时

- 在从模式下，当检测到重启条件时（检测到重启条件时ICCR2.BBSY=1并且ICCR2.MST = 0)
- 当将0写入TRS位且ICMR1中的MTWP位设置为1时
- 当向ICCR1中的IICRST位写入1时，应用IIC复位或内部复位。

MST位（主从模式）

MST位指示主机或从机模式。当MST位为0时IIC处于从机模式，当该位为1时IIC处于主机模式。该位和TRS位的组合表示IIC的工作模式。

当发出启动条件或发出或检测到停止条件时，MST位的值自动变为1（主机模式）或0（从机模式）。虽然当ICMR1的MTWP位设置为1时可以写入MST位，但在正常使用期间不需要写入该位。

[Setting conditions]

- 由于启动条件请求而正常发出启动条件时（在ST位设置为1的情况下检测到启动条件时）
- 当ICMR1中的MTWP位设置为1时，将1写入MST位。

[Clearing conditions]

- 检测到停止条件时
- ICSR2中的AL（仲裁失败）标志设置为1时
- 将0写入MST位且ICMR1中的MTWP位设置为1时
- 当向ICCR1中的IICRST位写入1时，应用IIC复位或内部复位。

BBSY标志（总线忙检测标志）

BBSY标志指示I2C总线是被占用（总线繁忙状态）还是被释放（总线空闲状态）。当SCLn线为高时SDAn线从高变为低时，该标志设置为1，假设发出了启动条件。如果在总线空闲时间（ICBRL设置）没有检测到启动条件，则该标志设置为0，假设发出了停止条件。

[Setting condition]

- 当检测到启动条件时。

[Clearing conditions]

- 检测到停止条件后，在总线空闲时间（ICBRL设置）未检测到启动条件时
- 当ICCR1中的IICRST位写入1且ICCR1中的ICE位设置为0时（IIC复位）。

36.2.3 I2C Bus Mode Register 1 (ICMR1)

Address(es): IIC0.ICMR1 4005 3002h, IIC1.ICMR1 4005 3102h, IIC2.ICMR1 4005 3202h

	b7	b6	b5	b4	b3	b2	b1	b0
	MTWP	CKS[2:0]			BCWP	BC[2:0]		
Value after reset:	0	0	0	0	1	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	BC[2:0]	Bit Counter	b2 b0 0 0 0: 9 bits 0 0 1: 2 bits 0 1 0: 3 bits 0 1 1: 4 bits 1 0 0: 5 bits 1 0 1: 6 bits 1 1 0: 7 bits 1 1 1: 8 bits.	R/W*1
b3	BCWP	BC Write Protect	0: Write enable BC[2:0] bits 1: Write protect BC[2:0] bits. This bit is read as 1.	R/W*1
b6 to b4	CKS[2:0]	Internal Reference Clock Select	Select the internal reference clock source (IICϕ) for the IIC. b6 b4 0 0 0: PCLKB clock 0 0 1: PCLKB/2 clock 0 1 0: PCLKB/4 clock 0 1 1: PCLKB/8 clock 1 0 0: PCLKB/16 clock 1 0 1: PCLKB/32 clock 1 1 0: PCLKB/64 clock 1 1 1: PCLKB/128 clock.	R/W
b7	MTWP	MST/TRS Write Protect	0: Write protect MST and TRS bits in ICCR2 1: Write enable MST and TRS bits in ICCR2.	R/W

Note 1. Rewrite the BC[2:0] bits and set the BCWP bit to 0 at the same time.

BC[2:0] bits (Bit Counter)

The BC[2:0] bits function as a counter indicating the number of bits remaining to be transferred on detection of a rising edge on the SCLn line. Although BC[2:0] are read/write bits, it is not normally necessary to access these bits.

To write to these bits, specify the number of bits to be transferred plus one, for an additional acknowledge bit, between transferred frames when the SCLn line is at a low level. The value in the BC[2:0] bits returns to 000b at the end of a data transfer, including the acknowledge bit, or when a start or restart condition is detected.

36.2.4 I2C Bus Mode Register 2 (ICMR2)

Address(es): IIC0.ICMR2 4005 3003h, IIC1.ICMR2 4005 3103h, IIC2.ICMR2 4005 3203h

	b7	b6	b5	b4	b3	b2	b1	b0
	DLCS	SDDL[2:0]			—	TMOH	TMOL	TMOS
Value after reset:	0	0	0	0	0	1	1	0

Bit	Symbol	Bit name	Description	R/W
b0	TMOS	Timeout Detection Time Select	0: Select long mode 1: Select short mode.	R/W

36.2.3 I2C总线模式寄存器1(ICMR1)

Address(es): IIC0.ICMR1 4005 3002h, IIC1.ICMR1 4005 3102h, IIC2.ICMR1 4005 3202h

	b7	b6	b5	b4	b3	b2	b1	b0
	MTWP	CKS[2:0]			BCWP	BC[2:0]		
重置后的值:	0	0	0	0	1	0	0	0

Bit	Symbol	位名称	Description	R/W
b2 to b0	BC[2:0]	位计数器	b2 b0 0 0 0: 9 bits 0 0 1: 2 bits 0 1 0: 3 bits 0 1 1: 4 bits 1 0 0: 5 bits 1 0 1: 6 bits 1 1 0: 7 bits 1 1 1: 8 bits.	R/W*1
b3	BCWP	BC写保护	0：写使能BC[2:0]位1：写保护BC[2:0]位。该位读为1。	R/W*1
b6 to b4	CKS[2:0]	内部参考时钟选择	选择IIC的内部参考时钟源(IIC)。b6b4000：PCLKB时钟001：PCLKB2时钟010：PCLKB4时钟011：PCLKB8时钟100：PCLKB16时钟101：PCLKB32时钟110：PCLKB64时钟111：PCLKB128时钟。	R/W
b7	MTWP	MSTTRS写保护	0：写保护ICCR2中的MST和TRS位1：写使能ICCR2中的MST和TRS位。	R/W

Note 1. 重写BC[2:0]位，同时将BCWP位设置为0。

BC[2:0]位（位计数器）

BC[2:0]位用作计数器，指示在检测到SCLn线上的上升沿时要传输的剩余位数。虽然BC[2:0]是读写位，但通常不需要访问这些位。

要写入这些位，在SCLn线处于低电平时，指定要传输的位数加1，作为附加确认位，在传输的帧之间。BC[2:0]位中的值在数据传输结束时返回到000b，包括确认位，或者当检测到启动或重启条件时。

36.2.4 I2C总线模式寄存器2(ICMR2)

Address(es): IIC0.ICMR2 4005 3003h, IIC1.ICMR2 4005 3103h, IIC2.ICMR2 4005 3203h

	b7	b6	b5	b4	b3	b2	b1	b0
	DLCS	SDDL[2:0]			—	TMOH	TMOL	TMOS
重置后的值:	0	0	0	0	0	1	1	0

Bit	Symbol	位名称	Description	R/W
b0	TMOS	超时检测时间选择	0：选择长模式1：选择短模式。	R/W

Bit	Symbol	Bit name	Description	R/W
b1	TMOL	Timeout L Count Control	0: Disable count while SCLn line is low 1: Enable count while SCLn line is low.	R/W
b2	TMOH	Timeout H Count Control	0: Disable count while SCLn line is high 1: Enable count while SCLn line is high.	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6 to b4	SDDL[2:0]	SDA Output Delay Counter	• When ICMR2.DLCS = 0 (IICϕ) b6 b4 0 0 0: No output delay 0 0 1: 1 IICϕ cycle 0 1 0: 2 IICϕ cycles 0 1 1: 3 IICϕ cycles 1 0 0: 4 IICϕ cycles 1 0 1: 5 IICϕ cycles 1 1 0: 6 IICϕ cycles 1 1 1: 7 IICϕ cycles. • When ICMR2.DLCS = 1 (IICϕ/2) b6 b4 0 0 0: No output delay 0 0 1: 1 or 2 IICϕ cycles 0 1 0: 3 or 4 IICϕ cycles 0 1 1: 5 or 6 IICϕ cycles 1 0 0: 7 or 8 IICϕ cycles 1 0 1: 9 or 10 IICϕ cycles 1 1 0: 11 or 12 IICϕ cycles 1 1 1: 13 or 14 IICϕ cycles.	R/W
b7	DLCS	SDA Output Delay Clock Source Select	0: Select internal reference clock (IICϕ) as clock source for SDA output delay counter 1: Select internal reference clock divided by 2 (IICϕ/2) as clock source for SDA output delay counter.*1	R/W

Note 1. The setting DLCS = 1 (IICϕ/2) is only valid when SCL is low. When SCL is high, the DLCS = 1 setting becomes invalid and the clock source becomes the internal reference clock (IICϕ).

TMOS bit (Timeout Detection Time Select)

The TMOS bit selects long or short mode for the timeout detection time when the timeout function is enabled (ICFER.TMOE = 1). When this bit is set to 0, long mode is selected. When it is set to 1, short mode is selected. In long mode, the timeout detection internal counter functions as a 16 bit-counter. In short mode, the counter functions as a 14-bit counter. While the SCLn line is in the state that enables this counter as specified in the TMOH and TMOL bits, the counter counts up in synchronization with the internal reference clock (IICϕ) as a count source. For details on this function, see section 36.12.1, Timeout Function.

TMOL bit (Timeout L Count Control)

The TMOL bit enables or disables up-counting on the internal counter of the timeout function while the SCLn line is held low and the timeout function is enabled (ICFER.TMOE = 1).

TMOH bit (Timeout H Count Control)

The TMOH bit enables or disables up-counting on the internal counter of the timeout function while the SCLn line is held high and the timeout function is enabled (ICFER.TMOE = 1).

SDDL[2:0] bits (SDA Output Delay Counter)

The SDDL[2:0] bits can be used to delay the SDA output. This counter works with the clock source selected in the DLCS bit. This setting can be used for all types of SDA output, including transmission of the acknowledge bit.

Set the SDA output delay to meet the I2C bus standard for the data enable time/acknowledge enable time,*1 or the SMBus standard, within [data hold time (300 ns or more + the SCL-clock low-level period) - the data setup time (250 ns)]. If a value outside the standard is set, communication between devices might malfunction or falsely indicate a start or stop condition, depending on the bus state.

For details on this function, see section 36.5, SDA Output Delay Function.

Note 1. Data enable time/acknowledge enable time

Bit	Symbol	位名称	Description	R/W
b1	TMOL	超时L计数控制	0：SCLn线为低电平时禁止计数1：SCLn线为低电平时使能计数。	R/W
b2	TMOH	超时H计数控制	0：SCLn线为高时禁止计数1：SCLn线为高时使能计数。	R/W
b3	—	Reserved	该位读取为0。写入值应为0。	R/W
b6 to b4	SDDL[2:0]	SDA输出延迟计数器	当ICMR2.DLCS=0(IIC)b6b4000：无输出延迟001：1IIC 周期010：2IIC 周期011：3IIC 周期100：4IIC 周期101：5IIC 周期110：6IIC 周期111：7IIC 周期。 当ICMR2.DLCS=1(IIC 2)b6b4000：无输出延迟001：1或2个IIC 周期010：3或4个IIC 周期011：5或6个IIC 周期100：7或8个IIC 周期101：9或10个IIC 周期110：11或12个IIC 周期111：13或14个IIC 周期。	R/W
b7	DLCS	SDA输出延迟时钟源Select	0：选择内部参考时钟（IIC ）作为SDA输出延迟计数器的时钟源 1：选择内部参考时钟除以2（IIC 2）作为SDA输出延迟计数器的时钟源。*1	R/W

Note 1. 设置DLCS=1(IIC 2)仅在SCL为低电平时有效。当SCL为高电平时，DLCS=1设置无效，时钟源变为内部参考时钟(IIC)。

TMOS位（超时检测时间选择）

当使能超时功能（ICFER.TMOE=1）时，TMOS位为超时检测时间选择长模式或短模式。当该位设置为0时，选择长模式。当设置为1时，选择短模式。在长模式下，超时检测内部计数器用作16位计数器。在短模式下，计数器用作14位计数器。当SCLn线处于启用TMOH和TMOL位中指定的计数器的状态时，计数器与作为计数源的内部参考时钟(IIC)同步递增计数。有关此功能的详细信息，请参阅第36.12.1节，超时功能。

TMOL位（超时L计数控制）

TMOL位启用或禁用超时功能内部计数器的递增计数，同时SCLn线保持低电平且启用超时功能(ICFER.TMOE=1)。

TMOH位（超时H计数控制）

TMOH位启用或禁用超时功能内部计数器的递增计数，同时SCLn线保持高电平且启用超时功能(ICFER.TMOE=1)。

SDDL[2:0]位（SDA输出延迟计数器）

SDDL[2:0]位可用于延迟SDA输出。该计数器与在DLCS位中选择的时钟源一起工作。该设置可用于所有类型的SDA输出，包括确认位的传输。

设置SDA输出延迟以满足I2C总线标准的数据启用时间确认启用时间，*1或SMBus标准，在[数据保持时间（300ns或更长+SCL时钟低电平周期）数据建立时间（250ns）内]。如果设置了超出标准的值，则设备之间的通信可能会发生故障或错误地指示开始或停止条件，具体取决于总线状态。

有关此功能的详细信息，请参阅第36.5节，SDA输出延迟功能。

注1.数据使能时间确认使能时间

3,450 ns for up to 100 kbps: Standard-mode (Sm)
900 ns for up to 400 kbps: Fast-mode (Fm)
450 ns for up to 1 Mbps: Fast-mode Plus (Fm+)

36.2.5 I2C Bus Mode Register 3 (ICMR3)

Address(es): IIC0.ICMR3 4005 3004h, IIC1.ICMR3 4005 3104h, IIC2.ICMR3 4005 3204h

	b7	b6	b5	b4	b3	b2	b1	b0
	SMBS	WAIT	RDRFS	ACKWP	ACKBT	ACKBR	NF[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	NF[1:0]	Noise Filter Stage Select	b1 b0 0 0: Filter out noise of up to 1 IICϕ cycle (single-stage filter) 0 1: Filter out noise of up to 2 IICϕ cycles (2-stage filter) 1 0: Filter out noise of up to 3 IICϕ cycles (3-stage filter) 1 1: Filter out noise of up to 4 IICϕ cycles (4-stage filter).	R/W
b2	ACKBR	Receive Acknowledge	0: 0 received as the acknowledge bit (ACK reception) 1: 1 received as the acknowledge bit (NACK reception).	R
b3	ACKBT	Transmit Acknowledge	0: Send 0 as the acknowledge bit (ACK transmission) 1: Send 1 as the acknowledge bit (NACK transmission).	R/W*1
b4	ACKWP	ACKBT Write Protect	0: Write protect ACKBT bit 1: Write enable ACKBT bit.	R/W*1
b5	RDRFS	RDRF Flag Set Timing Select	0: Set the RDRF flag on the rising edge of the ninth SCL clock cycle (no low-hold on the SCLn line on the falling edge of the eighth clock cycle) 1: Set the RDRF flag on the rising edge of the eighth SCL clock cycle (low-hold on the SCLn line low on the falling edge of the eighth clock cycle). Low-hold is released by writing to ACKBT.	R/W*2
b6	WAIT	WAIT	0: No wait (no low-hold between ninth clock cycle and first clock cycle) 1: Wait (low-hold between ninth clock cycle and first clock cycle). Low-hold is released by reading ICDRR.	R/W*2
b7	SMBS	SMBus/IIC-Bus Select	0: Select I2C bus 1: Select SMBus.	R/W

Note 1. Write to the ACKBT bit only while the ACKWP bit is already 1. If the application writes 1 to the ACKWP and ACKBT bits at the same time, the ACKBT bit does not set to 1.
Note 2. The WAIT and RDRFS bits are only valid in receive mode (invalid in transmit mode).

NF[1:0] bits (Noise Filter Stage Select)

The NF[1:0] bits select the number of stages in the digital noise filter. For details on this function, see section 36.6, Digital Noise Filter Circuits.

Note: Set the noise range to be filtered within a range less than the SCLn line high- or low-level period. If the noise range is set to a value of [SCL clock width: high- or low-level period, whichever is shorter] - [1.5 internal reference clock (IICϕ) cycles + analog noise filter: 120 ns (reference values)] or more, the SCL clock is regarded as noise, which might prevent the IIC from operating normally.

ACKBR bit (Receive Acknowledge)

The ACKBR bit stores the acknowledge bit information received from the receive device in transmit mode.

[Setting condition]

- When 1 is received as the acknowledge bit with the TRS bit in ICCR2 set to 1.

[Clearing conditions]

- When 0 is received as the acknowledge bit with the TRS bit in ICCR2 set to 1

3 450ns，最高100kbps：标准模式(Sm)900ns，
最高400kbps：快速模式(Fm)450ns，最高1Mbps
：快速模式Plus(Fm+)

36.2.5 I2C总线模式寄存器3(ICMR3)

Address(es): IIC0.ICMR3 4005 3004h, IIC1.ICMR3 4005 3104h, IIC2.ICMR3 4005 3204h

	b7	b6	b5	b4	b3	b2	b1	b0
	SMBS	WAIT	RDRFS	ACKWP	ACKBT	ACKBR	NF[1:0]	
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b1, b0	NF[1:0]	噪声过滤级选择	b1b000：过滤最多1个IIC 周期的噪声（单级滤波器）01：最多过滤2个IIC 周期的噪声（2级滤波器）10：最多过滤3个噪声IIC 周期（3级滤波器）11：滤除最多4个IIC 周期（4级滤波器）的噪声。	R/W
b2	ACKBR	接收确认	0：0作为确认位接收（ACK接收）1：1作为确认位接收（NACK接收）。	R
b3	ACKBT	发送确认	0：发送0作为确认位（ACK发送）1：发送1作为确认位（NACK发送）。	R/W*1
b4	ACKWP	ACKBT写保护	0：写保护ACKBT位1：写使能ACKBT位。	R/W*1
b5	RDRFS	RDRF标志设置时序Select	0：在第9个SCL时钟周期的上升沿设置RDRF标志（在第8个时钟周期的下降沿SCLn线上无低保持）1：在第8个SCL时钟的上升沿设置RDRF标志周期（在第8个时钟周期的下降沿SCLn线保持低电平）。通过写入ACKBT释放低保持。	R/W*2
b6	WAIT	WAIT	0：无等待（第9个时钟周期和第一个时钟周期之间不保持低电平）1：等待（第9个时钟周期和第一个时钟周期之间保持低电平）。通过读取ICDRR释放低保持。	R/W*2
b7	SMBS	SMBus/IIC-Bus Select	0：选择I2C总线1：选择SMBus。	R/W

Note 1. 仅当ACKWP位已经为1时才写入ACKBT位。如果应用程序同时向ACKWP和ACKBT位写入1，则ACKBT位不会设置为1。

Note 2. WAIT和RDRFS位仅在接收模式下有效（在发送模式下无效）。

NF[1:0]位（噪声滤波器级选择）

NF[1:0]位选择数字噪声滤波器的级数。有关此功能的详细信息，请参阅第36.6节，数字噪声滤波电路。

Note: 将要过滤的噪声范围设置在小于SCLn线高电平或低电平周期的范围内。如果噪声范围设置为[SCL时钟宽度：高电平或低电平周期，以较短者为准][1.5内部参考时钟(IIC)周期+模拟噪声滤波器：120ns（参考值）]或更大的值，SCL时钟被视为噪声，可能会导致IIC无法正常工作。

ACKBR位（接收确认）

ACKBR位存储在发送模式下从接收设备接收到的确认位信息。

[Setting condition]

- 当ICCR2中的TRS位设置为1接收到1作为确认位时。

[Clearing conditions]

- 当ICCR2中的TRS位设置为1接收到0作为确认位时

- When 1 is written to the IICRST bit in ICCR1 while the ICE bit in ICCR1 is 0 (IIC reset).

ACKBT bit (Transmit Acknowledge)

The ACKBT bit sets the acknowledge bit to be sent in receive mode.

[Setting condition]

- When 1 is written to this bit with the ACKWP bit set to 1.

[Clearing conditions]

- When 0 is written to this bit with the ACKWP bit set to 1
- When stop condition issuance is detected (when a stop condition is detected with the SP bit in ICCR2 set to 1)
- When 1 is written to the IICRST bit in ICCR1 while the ICE bit in ICCR1 is 0 (IIC reset).

ACKWP bit (ACKBT Write Protect)

The ACKWP bit controls write enabling of the ACKBT bit.

RDRFS bit (RDRF Flag Set Timing Select)

The RDRFS bit selects the RDRF flag set timing in receive mode and also selects whether to hold the SCLn line low on the falling edge of the eighth SCL clock cycle.

When the RDRFS bit is 0, the SCLn line is not held low on the falling edge of the eighth SCL clock cycle, and the RDRF flag is set to 1 on the rising edge of the ninth SCL clock cycle.

When the RDRFS bit is 1, the RDRF flag is set to 1 on the rising edge of the eighth SCL clock cycle, and the SCLn line is held low on the falling edge of the eighth SCL clock cycle. The low-hold of the SCLn line is released by a write to the ACKBT bit.

After data is received with this setting, the SCLn line is automatically held low before the acknowledge bit is sent. This enables processing to send ACK (ACKBT = 0) or NACK (ACKBT = 1), based on the receive data.

WAIT bit (WAIT)

The WAIT bit controls whether to force a low-hold between the ninth SCL clock cycle and the first SCL clock cycle, until the receive data buffer (ICDRR) is completely read each time single-byte data is received in receive mode.

When the WAIT bit is 0, the receive operation is continued without a low-hold between the ninth and the first SCL clock cycle. When both the RDRFS and WAIT bits are 0, continuous receive operation is enabled with the double buffer.

When the WAIT bit is 1, the SCLn line is held low from the falling edge of the ninth clock cycle until the ICDRR value is read each time single-byte data is received. This enables receive operation in byte units.

Note: When the value of the WAIT bit is to be read, always read ICDRR first.

SMBS bit (SMBus/IIC-Bus Select)

Setting the SMBS bit to 1 selects the SMBus and enables the HOAE bit in ICSER.

- 当ICCR1中的IICRST位写入1而ICCR1中的ICE位为0时（IIC复位）。

ACKBT位（发送确认）

ACKBT位设置要在接收模式下发送的确认位。

[Setting condition]

- 当1写入该位且ACKWP位设置为1时。

[Clearing conditions]

- 当0写入该位且ACKWP位设置为1时
- 当检测到停止条件发出时（当ICCR2的SP位设置为1时检测到停止条件时）
- 当ICCR1中的IICRST位写入1而ICCR1中的ICE位为0时（IIC复位）。

ACKWP位（ACKBT写保护）

ACKWP位控制ACKBT位的写使能。

RDRFS位（RDRF标志设置时序选择）

RDRFS位选择接收模式下的RDRF标志设置时序，还选择是否在第8个SCL时钟周期的下降沿保持SCLn线为低电平。

当RDRFS位为0时，SCLn线在第8个SCL时钟周期的下降沿不保持低电平，在第9个SCL时钟周期的上升沿将RDRF标志设置为1。

当RDRFS位为1时，RDRF标志在第8个SCL时钟周期的上升沿设置为1，并且SCLn线在第8个SCL时钟周期的下降沿保持低电平。SCLn线的低保持通过写ACKBT位来释放。

使用此设置接收数据后，SCLn线在发送确认位之前自动保持低电平。这使处理能够根据接收数据发送ACK(ACKBT=0)或NACK(ACKBT=1)。

等待位（等待）

WAIT位控制是否在第9个SCL时钟周期和第一个SCL时钟周期之间强制保持低电平，直到每次在接收模式下接收到单字节数据时完全读取接收数据缓冲区(ICDRR)。

当WAIT位为0时，接收操作继续，在第9个和第一个SCL时钟周期之间没有低电平保持。当RDRFS和WAIT位都为0时，双缓冲器使能连续接收操作。

当WAIT位为1时，SCLn线从第9个时钟周期的下降沿保持低电平，直到每次接收到单字节数据时读取ICDRR值。这启用了以字节为单位的接收操作。

Note: 当要读取WAIT位的值时，总是先读取ICDRR。

SMBS位（SMBusIIC−Bus选择）

将SMBS位设置为1可选择SMBus并启用ICSER中的HOAE位。

36.2.6 I2C Bus Function Enable Register (ICFER)

Address(es): IIC0.ICFER 4005 3005h, IIC1.ICFER 4005 3105h, IIC2.ICFER 4005 3205h

	b7	b6	b5	b4	b3	b2	b1	b0
	FMPE	SCLE	NFE	NACKE	SALE	NALE	MALE	TMOE
Value after reset:	0	1	1	1	0	0	1	0

Bit	Symbol	Bit name	Description	R/W
b0	TMOE	Timeout Function Enable	0: Disable 1: Enable.	R/W
b1	MALE	Master Arbitration-Lost Detection Enable	0: Disable the arbitration-lost detection function and disable automatic clearing of the MST and TRS bits in ICCR2 when arbitration is lost 1: Enable the arbitration-lost detection function and enable automatic clearing of the MST and TRS bits in ICCR2 when arbitration is lost.	R/W
b2	NALE	NACK Transmission Arbitration-Lost Detection Enable	0: Disable 1: Enable.	R/W
b3	SALE	Slave Arbitration-Lost Detection Enable	0: Disable 1: Enable.	R/W
b4	NACKE	NACK Reception Transfer Suspension Enable	0: Do not suspend transfer operation during NACK reception (disable transfer suspension) 1: Suspend transfer operation during NACK reception (enable transfer suspension).	R/W
b5	NFE	Digital Noise Filter Circuit Enable	0: Do not use the digital noise filter circuit 1: Use the digital noise filter circuit.	R/W
b6	SCLE	SCL Synchronous Circuit Enable	0: Do not use the SCL synchronous circuit 1: Use the SCL synchronous circuit.	R/W
b7	FMPE*1	Fast-Mode Plus Enable	0: Do not use the Fm+ slope control circuit for the SCLn and SDAn pins 1: Use the Fm+ slope control circuit for the SCLn and SDAn pins.	R/W

Note 1. The Fast-mode Plus enable bit (FMPE) is supported only by IIC0 (SCL0-A, SDA0-A). Bit [7] is reserved in IIC1 and IIC2.

TMOE bit (Timeout Function Enable)

The TMOE bit enables or disables the timeout function. For details on this function, see section 36.12.1, Timeout Function.

MALE bit (Master Arbitration-Lost Detection Enable)

The MALE bit specifies whether to use the arbitration-lost detection function in master mode. Normally, set this bit to 1.

NALE bit (NACK Transmission Arbitration-Lost Detection Enable)

The NALE bit specifies whether to cause arbitration to be lost when ACK is detected during transmission of NACK in receive mode, for example when slaves with the same address exist on the bus or when two or more masters select the same slave device simultaneously with a different number of receive bytes.

SALE bit (Slave Arbitration-Lost Detection Enable)

The SALE bit specifies whether to cause arbitration to be lost when a value different from the value being transmitted is detected on the bus in slave transmit mode, for example when slaves with the same address exist on the bus or when a mismatch with the transmit data occurs because of noise.

NACKE bit (NACK Reception Transfer Suspension Enable)

The NACKE bit specifies whether to continue or discontinue the transfer operation when NACK is received in transmit mode. Normally, set this bit to 1.

When NACK is received with the NACKE bit set to 1, the next transfer operation is suspended. When the NACKE bit is

36.2.6 I2C总线功能使能寄存器(ICFER)

Address(es): IIC0.ICFER 4005 3005h, IIC1.ICFER 4005 3105h, IIC2.ICFER 4005 3205h

	b7	b6	b5	b4	b3	b2	b1	b0
	FMPE	SCLE	NFE	NACKE	SALE	NALE	MALE	TMOE
重置后的值:	0	1	1	1	0	0	1	0

Bit	Symbol	位名称	Description	R/W
b0	TMOE	超时功能启用	0：禁用1 ：启用。	R/W
b1	MALE	Master Arbitration-Lost 检测启用	0：禁止仲裁丢失检测功能，禁止仲裁丢失时自动清除ICCR2中的MST和TRS位1：使能仲裁丢失检测功能，并启用仲裁丢失时自动清除ICCR2中的MST和TRS位.	R/W
b2	NALE	NACK传输 Arbitration-Lost Detection Enable	0：禁用1 ：启用。	R/W
b3	SALE	Slave Arbitration-Lost 检测启用	0：禁用1 ：启用。	R/W
b4	NACKE	NACK接收传输 暂停启用	0：在NACK接收期间不暂停传输操作（禁用传输暂停）1：在NACK接收期间暂停传输操作（启用传输暂停）。	R/W
b5	NFE	数字噪声滤波电路 Enable	0：不使用数字噪声滤波电路1：使用数字噪声滤波电路。	R/W
b6	SCLE	SCL同步电路 Enable	0：不使用SCL同步电路1：使用SCL同步电路。	R/W
b7	FMPE*1	快速模式加启用	0：SCLn和SDAn引脚不使用Fm+斜率控制电路1：SCLn和SDAn引脚使用Fm+斜率控制电路。	R/W

Note 1. 只有IIC0（SCL0-A、SDA0-A）支持Fast-modePlus使能位（FMPE）。位[7]在IIC1和IIC2中保留。

TMOE位（超时功能使能）

TMOE位启用或禁用超时功能。有关此功能的详细信息，请参阅第36.12.1节，超时 Function.

MALE位（主仲裁丢失检测使能）

MALE位指定是否在主机模式下使用仲裁丢失检测功能。通常，将此位设置为1。

NALE位（NACK传输仲裁丢失检测使能）

NALE位指定在接收模式下发送NACK期间检测到ACK时是否导致仲裁丢失，例如，当总线上存在具有相同地址的从设备时，或者当两个或多个主设备同时选择相同的从设备时接收字节数。

SALE位（从设备仲裁丢失检测使能）

SALE位指定当在从发送模式下在总线上检测到与正在发送的值不同的值时，是否导致仲裁丢失，例如，当总线上存在具有相同地址的从机或与发送数据不匹配时由于噪音而发生。

NACKE位（NACK接收传输暂停使能）

NACKE位指定在发送模式下接收到NACK时是继续还是停止传输操作。通常，将此位设置为1。

当在NACKE位设置为1的情况下接收到NACK时，暂停下一个传输操作。当NACKE位是

0, the next transfer operation is continued regardless of the received acknowledge content.

For details, see section 36.9.2, NACK Reception Transfer Suspension Function.

SCLE bit (SCL Synchronous Circuit Enable)

The SCLE bit specifies whether to synchronize the SCL clock with the SCL input clock. Normally, set this bit to 1.

When the SCLE bit is set to 0 (no SCL synchronous circuit used), the IIC does not synchronize the SCL clock with the SCL input clock. With this setting, the IIC outputs the SCL clock at the transfer rate set in ICBRH and ICBRL, regardless of the SCLn line state. For this reason, if the bus load of the I2C bus line is much larger than the specification value, or if the SCL clock output overlaps in multiple masters, a short-cycle SCL clock that does not meet the specification might be output. When no SCL synchronous circuit is used, it also affects the issuance of the start, restart, and stop conditions, and the continuous output of extra SCL clock cycles.

Do not set this bit to 0 except when checking the output of the set transfer rate.

FMPE bit (Fast-Mode Plus Enable)

The FMPE bit specifies whether to use a slope control circuit for Fast-mode Plus (Fm+).

When this bit is set to 1, a slope control circuit conforming to the I2C bus Fast-mode Plus (Fm+) standard (tof) is selected. When this bit is set to 0, a slope control circuit conforming to the I2C bus Standard-mode (Sm) and Fast-mode (Fm) standards (tof) is selected.

Set this bit to 1 when using transmission rates up to 1 Mbps (Fast-mode Plus (Fm+) standard). Set it to 0 when using other transmission rates (up to 100 kbps (Sm) or up to 400 kbps (Fm)) or for SMBus (10 to 100 kbps).

36.2.7 I2C Bus Status Enable Register (ICSER)

Address(es): IIC0.ICSER 4005 3006h, IIC1.ICSER 4005 3106h, IIC2.ICSER 4005 3206h

	b7	b6	b5	b4	b3	b2	b1	b0
	HOAE	—	DIDE	—	GCAE	SAR2E	SAR1E	SAR0E
Value after reset:	0	0	0	0	1	0	0	1

Bit	Symbol	Bit name	Description	R/W
b0	SAR0E	Slave Address Register 0 Enable	0: Disable slave address in SARL0 and SARU0 1: Enable slave address in SARL0 and SARU0.	R/W
b1	SAR1E	Slave Address Register 1 Enable	0: Disable slave address in SARL1 and SARU1 1: Enable slave address in SARL1 and SARU1.	R/W
b2	SAR2E	Slave Address Register 2 Enable	0: Disable slave address in SARL2 and SARU2 1: Enable slave address in SARL2 and SARU2.	R/W
b3	GCAE	General Call Address Enable	0: Disable general call address detection 1: Enable general call address detection.	R/W
b4	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b5	DIDE	Device-ID Address Detection Enable	0: Disable device-ID address detection 1: Enable device-ID address detection.	R/W
b6	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b7	HOAE	Host Address Enable	0: Disable host address detection 1: Enable host address detection.	R/W

SARyE bit (Slave Address Register y Enable) (y = 0 to 2)

The SARyE bit enables or disables the received slave address and the slave address set in SARLy and SARUy.

When this bit is set to 1, the slave address set in SARLy and SARUy is enabled and is compared with the received slave address. When this bit is set to 0, the slave address set in SARLy and SARUy is disabled and is ignored even if it matches the received slave address.

0，无论接收到的确认内容如何， 都继续下一个传输操作。

有关详细信息，请参阅第36.9.2节，NACK接收传输暂停功能。

SCLE位（SCL同步电路使能）

SCLE位指定是否将SCL时钟与SCL输入时钟同步。通常，将此位设置为1。

当SCLE位设置为0（不使用SCL同步电路）时，IIC不会将SCL时钟与SCL输入时钟同步。使用此设置，无论SCLn线路状态如何，IIC都以ICBRH和ICBRL中设置的传输速率输出SCL时钟。因此，如果I2C总线的总线负载远大于规格值，或者多个主机的SCL时钟输出重叠，则可能会输出不符合规格的短周期SCL时钟。当不使用SCL同步电路时，也会影响启动、重启和停止条件的发出，以及额外SCL时钟周期的连续输出。

除非检查设置传输速率的输出，否则不要将此位设置为0。

FMPE位（快速模式加启用）

FMPE位指定是否对Fast-modePlus(Fm+)使用斜率控制电路。

当该位设置为1时，选择符合I2C总线快速模式加(Fm+)标准(tof)的斜率控制电路。当该位设置为0时，选择符合I2C总线标准模式(Sm)和快速模式(Fm)标准(tof)的斜率控制电路。

当使用高达1Mbps的传输速率（Fast-modePlus(Fm+)标准）时，将此位设置为1。当使用其他传输速率（最高100kbps(Sm)或最高400kbps(Fm)）或SMBus（10至100kbps）时，将其设置为0。

36.2.7 I2C总线状态使能寄存器(ICSER)

Address(es): IIC0.ICSER 4005 3006h, IIC1.ICSER 4005 3106h, IIC2.ICSER 4005 3206h

	b7	b6	b5	b4	b3	b2	b1	b0
	HOAE	—	DIDE	—	GCAE	SAR2E	SAR1E	SAR0E
重置后的值：	0	0	0	0	1	0	0	1

Bit	Symbol	位名称	Description	R/W
b0	SAR0E	从地址寄存器0使能	0：禁用SARL0和SARU0中的从地址1：启用SARL0和SARU0中的从地址。	R/W
b1	SAR1E	从地址寄存器1使能	0：禁用SARL1和SARU1中的从地址1：启用SARL1和SARU1中的从地址。	R/W
b2	SAR2E	从地址寄存器2使能	0：禁用SARL2和SARU2中的从机地址1：启用SARL2和SARU2中的从机地址。	R/W
b3	GCAE	广播呼叫地址启用	0：禁用广播地址检测1：启用广播地址检测。	R/W
b4	—	Reserved	该位读取为0。写入值应为0。	R/W
b5	DIDE	设备ID地址检测 Enable	0：禁用设备ID地址检测1：启用设备ID地址检测。	R/W
b6	—	Reserved	该位读取为0。写入值应为0。	R/W
b7	HOAE	主机地址启用	0：禁用主机地址检测1：启用主机地址检测。	R/W

SARyE位（从地址寄存器y使能）（y=0到2）

SARyE位启用或禁用接收到的从机地址和设置在SARLy和SARUy中的从机地址。

当该位设置为1时，设置在SARLy和SARUy中的从机地址被启用，并与接收到的从机地址进行比较。当该位设置为0时，设置在SARLy和SARUy中的从机地址被禁用并被忽略，即使它与接收到的从机地址匹配。

GCAE bit (General Call Address Enable)

The GCAE bit specifies whether to ignore the general call address (0000 000b + 0 [W]: All 0) when it is received.

When this bit is set to 1, if the received slave address matches the general call address, the IIC recognizes the received slave address as the general call address independently of the slave addresses set in SARLy and SARUy (y = 0 to 2) and performs the data receive operation. When this bit is set to 0, the received slave address is ignored even if it matches the general call address.

DIDE bit (Device-ID Address Detection Enable)

The DIDE bit specifies whether to recognize and execute the device-ID address when a device ID (1111 100b) is received in the first frame after a start or restart condition is detected.

When this bit is set to 1, if the received first frame matches the device ID, the IIC recognizes that the device-ID address was received. When the next R/W# bit is 0 (W), the IIC recognizes the second and the subsequent frames as slave addresses and continues the receive operation. When this bit is set to 0, the IIC ignores the received first frame even if it matches the device-ID address, and it recognizes the first frame as a normal slave address.

For details on this function, see section 36.7.3, Device-ID Address Detection.

HOAE bit (Host Address Enable)

The HOAE bit specifies whether to ignore the received host address (0001 000b) when the SMBS bit in ICMR3 is 1.

When this bit is set to 1 while the SMBS bit in ICMR3 is 1, if the received slave address matches the host address, the IIC recognizes the received slave address as the host address independently of the slave addresses set in SARLy and SARUy (y = 0 to 2) and performs the receive operation.

When the SMBS bit in ICMR3 or the HOAE bit is set to 0, the received slave address is ignored even if it matches the host address.

36.2.8 I2C Bus Interrupt Enable Register (ICIER)

Address(es): IIC0.ICIER 4005 3007h, IIC1.ICIER 4005 3107h, IIC2.ICIER 4005 3207h

	b7	b6	b5	b4	b3	b2	b1	b0
	TIE	TEIE	RIE	NAKIE	SPIE	STIE	ALIE	TMOIE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	TMOIE	Timeout Interrupt Request Enable	0: Disable timeout interrupt (TMOI) request 1: Enable timeout interrupt (TMOI) request.	R/W
b1	ALIE	Arbitration-Lost Interrupt Request Enable	0: Disable arbitration-lost interrupt (ALI) request 1: Enable arbitration-lost interrupt (ALI) request.	R/W
b2	STIE	Start Condition Detection Interrupt Request Enable	0: Disable start condition detection interrupt (STI) request 1: Enable start condition detection interrupt (STI) request.	R/W
b3	SPIE	Stop Condition Detection Interrupt Request Enable	0: Disable stop condition detection interrupt (SPI) request 1: Enable stop condition detection interrupt (SPI) request.	R/W
b4	NAKIE	NACK Reception Interrupt Request Enable	0: Disable NACK reception interrupt (NAKI) request 1: Enable NACK reception interrupt (NAKI) request.	R/W
b5	RIE	Receive Data Full Interrupt Request Enable	0: Disable receive data full interrupt (IICn_RXI) request 1: Enable receive data full interrupt (IICn_RXI) request.	R/W
b6	TEIE	Transmit End Interrupt Request Enable	0: Disable transmit end interrupt (IICn_TEI) request 1: Enable transmit end interrupt (IICn_TEI) request.	R/W
b7	TIE	Transmit Data Empty Interrupt Request Enable	0: Disable transmit data empty interrupt (IICn_TXI) request 1: Enable transmit data empty interrupt (IICn_TXI) request.	R/W

GCAE位（广播呼叫地址使能）

GCAE位指定接收到的广播调用地址（0000000b+0[W]：全0）是否忽略。

当该位设置为1时，如果接收到的从机地址与广播呼叫地址匹配，则IIC将接收到的从机地址识别为广播呼叫地址，而与在SARLy和SARUy中设置的从机地址（y=0到2）无关，并执行数据接收操作。当该位设置为0时，即使接收到的从机地址与广播呼叫地址匹配，也会忽略它。

DIDE位（设备ID地址检测使能）

DIDE位指定在检测到启动或重新启动条件后的第一帧中接收到设备ID(1111100b)时是否识别和执行设备ID地址。

当该位设置为1时，如果接收到的第一个帧与设备ID匹配，则IIC识别出设备ID地址已被接收。当下一个RW#位为0(W)时，IIC将第二个和后续帧识别为从地址并继续接收操作。当该位设置为0时，IIC忽略接收到的第一帧，即使它与设备ID地址匹配，并将第一帧识别为正常的从地址。

有关此功能的详细信息，请参阅第36.7.3节，设备ID地址检测。

HOAE位（主机地址使能）

HOAE位指定当ICMR3中的SMBS位为1时是否忽略接收到的主机地址（0001000b）。

当该位设置为1且ICMR3中的SMBS位为1时，如果接收到的从机地址与主机地址匹配，则IIC将接收到的从地址识别为主机地址，与SARLy中设置的从地址无关，并且SARUy（y=0到2）并执行接收操作。

当ICMR3中的SMBS位或HOAE位设置为0时，即使接收到的从机地址与主机地址匹配，也会忽略它。

36.2.8 I2C总线中断使能寄存器(ICIER)

Address(es): IIC0.ICIER 4005 3007h, IIC1.ICIER 4005 3107h, IIC2.ICIER 4005 3207h

	b7	b6	b5	b4	b3	b2	b1	b0
	TIE	TEIE	RIE	NAKIE	SPIE	STIE	ALIE	TMOIE
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	TMOIE	超时中断请求使能	0：禁用超时中断（TMOI）请求1：启用超时中断（TMOI）请求。	R/W
b1	ALIE	仲裁失败中断请求Enable	0：禁用仲裁丢失中断(ALI)请求1：启用仲裁丢失中断(ALI)请求。	R/W
b2	STIE	启动条件检测中断请求启用	0：禁止启动条件检测中断（STI）请求1：允许启动条件检测中断（STI）请求。	R/W
b3	SPIE	停止条件检测中断请求启用	0：禁止停止条件检测中断（SPI）请求1：使能停止条件检测中断（SPI）请求。	R/W
b4	NAKIE	NACK接收中断请求Enable	0：禁止NACK接收中断（NAKI）请求1：允许NACK接收中断（NAKI）请求。	R/W
b5	RIE	接收数据完整中断请求Enable	0：禁止接收数据满中断（IICn_RXI）请求1：使能接收数据满中断（IICn_RXI）请求。	R/W
b6	TEIE	发送结束中断请求Enable	0：禁止发送结束中断（IICn_TEI）请求1：允许发送结束中断（IICn_TEI）请求。	R/W
b7	TIE	发送数据空中断请求启用	0：禁止发送数据空中断（IICn_TXI）请求1：使能发送数据空中断（IICn_TXI）请求。	R/W

TMOIE bit (Timeout Interrupt Request Enable)

The TMOIE bit enables or disables timeout interrupt (TMOI) requests when the TMOF flag in ICSR2 is 1. To cancel a TMOI interrupt request, set the TMOF flag or the TMOIE bit to 0.

ALIE bit (Arbitration-Lost Interrupt Request Enable)

The ALIE bit enables or disables arbitration-lost interrupt (ALI) requests when the AL flag in ICSR2 is 1. To cancel an ALI interrupt request, set the AL flag or the ALIE bit to 0.

STIE bit (Start Condition Detection Interrupt Request Enable)

The STIE bit enables or disables start condition detection interrupt (STI) requests when the START flag in ICSR2 is 1. To cancel an STI interrupt request, set the START flag or the STIE bit to 0.

SPIE bit (Stop Condition Detection Interrupt Request Enable)

The SPIE bit enables or disables stop condition detection interrupt (SPI) requests when the STOP flag in ICSR2 is 1. To cancel an SPI interrupt request, set the STOP flag or the SPIE bit to 0.

NAKIE bit (NACK Reception Interrupt Request Enable)

The NAKIE bit enables or disables NACK reception interrupt (NAKI) requests when the NACKF flag in ICSR2 is 1. To cancel an NAKI interrupt request, set the NACKF flag or the NAKIE bit to 0.

RIE bit (Receive Data Full Interrupt Request Enable)

The RIE bit enables or disables receive data full interrupt (IICn_RXI) requests when the RDRF flag in ICSR2 is 1.

TEIE bit (Transmit End Interrupt Request Enable)

The TEIE bit enables or disables transmit end interrupt (IICn_TEI) requests when the TEND flag in ICSR2 is 1. To cancel an IICn_TEI interrupt request, set the TEND flag or the TEIE bit to 0.

TIE bit (Transmit Data Empty Interrupt Request Enable)

The TIE bit enables or disables transmit data empty interrupt (IICn_TXI) requests when the TDRE flag in ICSR2 is 1.

36.2.9 I2C Bus Status Register 1 (ICSR1)

Address(es): IIC0.ICSR1 4005 3008h, IIC1.ICSR1 4005 3108h, IIC2.ICSR1 4005 3208h

	b7	b6	b5	b4	b3	b2	b1	b0
	HOA	—	DID	—	GCA	AAS2	AAS1	AAS0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	AAS0	Slave Address 0 Detection Flag	0: Slave address 0 not detected 1: Slave address 0 detected.	R/(W) *1
b1	AAS1	Slave Address 1 Detection Flag	0: Slave address 1 not detected 1: Slave address 1 detected.	R/(W) *1
b2	AAS2	Slave Address 2 Detection Flag	0: Slave address 2 not detected 1: Slave address 2 detected.	R/(W) *1
b3	GCA	General Call Address Detection Flag	0: General call address not detected 1: General call address detected.	R/(W) *1
b4	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b5	DID	Device-ID Address Detection Flag	0: Device-ID command not detected 1: Device-ID command detected. This bit is set to 1 when the first frame received immediately after a start condition is detected matches a value of (device ID (1111 100b) + 0[W]).	R/(W) *1

TMOIE位（超时中断请求使能）

当ICSR2中的TMOF标志为1时，TMOIE位启用或禁用超时中断(TMOI)请求。取消一个TMOI中断请求，设置TMOF标志或TMOIE位为0。

ALIE位（仲裁丢失中断请求使能）

当ICSR2中的AL标志为1时，ALIE位启用或禁用仲裁丢失中断(ALI)请求。取消ALI中断请求，设置AL标志或ALIE位为0。

STIE位（启动条件检测中断请求使能）

当ICSR2中的START标志为1时，STIE位启用或禁用启动条件检测中断(STI)请求。要取消STI中断请求，请将START标志或STIE位设置为0。

SPIE位（停止条件检测中断请求使能）

当ICSR2中的STOP标志为1时，SPIE位启用或禁用停止条件检测中断(SPI)请求。要取消SPI中断请求，请将STOP标志或SPIE位设置为0。

NAKIE位（NACK接收中断请求使能）

当ICSR2中的NACKF标志为1时，NAKIE位启用或禁用NACK接收中断(NAKI)请求。要取消NAKI中断请求，请将NACKF标志或NAKIE位设置为0。

RIE位（接收数据满中断请求使能）

当ICSR2中的RDRF标志为1时，RIE位启用或禁用接收数据完整中断(IICn_RXI)请求。

TEIE位（发送结束中断请求使能）

当ICSR2中的TEND标志为1时，TEIE位启用或禁用发送结束中断(IICn_TEI)请求。要取消IICn_TEI中断请求，请将TEND标志或TEIE位设置为0。

TIE位（发送数据空中断请求使能）

当ICSR2中的TDRE标志为1时，TIE位启用或禁用发送数据空中断（IICn_TXI）请求。

36.2.9 I2C总线状态寄存器1(ICSR1)

Address(es): IIC0.ICSR1 4005 3008h, IIC1.ICSR1 4005 3108h, IIC2.ICSR1 4005 3208h

	b7	b6	b5	b4	b3	b2	b1	b0
	HOA	—	DID	—	GCA	AAS2	AAS1	AAS0
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	AAS0	从地址0检测标志	0：未检测到从地址01：检测到从地址0。	R/(W) *1
b1	AAS1	从地址1检测标志	0：未检测到从地址11：检测到从地址1。	R/(W) *1
b2	AAS2	从地址2检测标志	0：未检测到从地址21：检测到从地址2。	R/(W) *1
b3	GCA	广播呼叫地址检测Flag	0：未检测到广播呼叫地址1：检测到广播呼叫地址。	R/(W) *1
b4	—	Reserved	该位读取为0。写入值应为0。	R/W
b5	DID	设备ID地址检测标志	0：未检测到设备ID命令1：检测到设备ID命令。当检测到开始条件后立即接收到的第一个帧与(设备ID(1111100b)+0[W])的值匹配时，该位设置为1。	R/(W) *1

Bit	Symbol	Bit name	Description	R/W
b6	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b7	HOA	Host Address Detection Flag	0: Host address not detected 1: Host address detected. This bit is set to 1 when the received slave address matches the host address (0001 000b).	R/(W) *1

Note 1. Only 0 can be written, to clear the flag.

AASy flag (Slave Address y Detection Flag) (y = 0 to 2)

The AASy flag indicates whether slave address y was detected.

[Setting conditions]

For 7-bit address format (SARUy.FS = 0):

- When the received slave address matches the SVA[6:0] value in SARLy, with the SARyE bit in ICSER set to 1 (slave address y detection enabled).
  The AASy flag is set to 1 on the rising edge of the ninth SCL clock cycle in the frame.

For 10-bit address format: (SARUy.FS = 1):

- When the received slave address matches a value of (11110b + SVA[1:0] in SARUy), and the subsequent address matches the SARLy value, with the SARyE bit in ICSER set to 1 (slave address y detection enabled).
  The AASy flag is set to 1 on the rising edge of the ninth SCL clock cycle in the frame.

[Clearing conditions]

- When 0 is written to the AASy flag after reading AASy = 1
- When a stop condition is detected
- When 1 is written to the IICRST bit in ICCR1 to apply an IIC reset or an internal reset.

For 7-bit address format (SARUy.FS = 0):

- When the received slave address does not match the SVA[6:0] value in SARLy, with the SARyE bit in ICSER set to 1 (slave address y detection enabled).
  The AASy flag is set to 0 on the rising edge of the ninth SCL clock cycle in the frame.

For 10-bit address format (SARUy.FS = 1):

- When the received slave address does not match a value of (11110b + SVA[1:0] in SARUy), with the SARyE bit in ICSER set to 1 (slave address y detection enabled)
  The AASy flag is set to 0 on the rising edge of the ninth SCL clock cycle in the frame.
- When the received slave address matches a value of (11110b + SVA[1:0] in SARUy), and the subsequent address does not match the SARLy value, with the SARyE bit in ICSER set to 1 (slave address y detection enabled).
  The AASy flag is set to 0 on the rising edge of the ninth SCL clock cycle in the frame.

GCA flag (General Call Address Detection Flag)

The GCA flag indicates whether the general call address was detected.

[Setting condition]

- When the received slave address matches the general call address (0000 000b + 0 [W]), with the GCAE bit in ICSER set to 1 (general call address detection enabled).
  The GCA flag is set to 1 on the rising edge of the ninth SCL clock cycle in the frame.

[Clearing conditions]

- When 0 is written to the GCA flag after reading GCA = 1
- When a stop condition is detected
- When the received slave address does not match the general call address (0000 000b + 0 [W]), with the GCAE bit in ICSER set to 1 (general call address detection enabled)

Bit	Symbol	位名称	Description	R/W
b6	—	Reserved	该位读取为0。写入值应为0。	R/W
b7	HOA	主机地址检测标志	0：未检测到主机地址1：检测到主机地址。当接收到的从机地址与主机地址(0001000b)匹配时，该位设置为1。	R/(W) *1

Note 1. 只能写入0，以清除标志。

AASy标志（从机地址y检测标志）（y=0到2）

AASy标志指示是否检测到从地址y。

[Setting conditions]

对于7位地址格式(SARUy.FS=0)：

- 当接收到的从机地址与SARLy中的SVA[6:0]值匹配时，ICSER中的SARyE位设置为1（启用从机地址y检测）。AASy标志在帧中第9个SCL时钟周期的上升沿设置为1。

对于10位地址格式：(SARUy.FS=1)：

- 当接收到的从地址与(SARUy中的11110b+SVA[1:0])值匹配，并且后续地址与SARLy值匹配时，ICSER中的SARyE位设置为1（启用从地址y检测）。AASy标志在帧中第9个SCL时钟周期的上升沿设置为1。

[Clearing conditions]

- 读取AASy=1后将0写入AASy标志时
- 检测到停止条件时
- 当向ICCR1中的IICRST位写入1时，应用IIC复位或内部复位。

对于7位地址格式(SARUy.FS=0)：

- 当接收到的从地址与SARLy中的SVA[6:0]值不匹配时，ICSER中的SARyE位设置为1（从地址y检测使能）。AASy标志在帧中第9个SCL时钟周期的上升沿设置为0。

对于10位地址格式(SARUy.FS=1)：

- 当接收到的从机地址与（SARUy中的11110b+SVA[1:0]）的值不匹配时，使用SARyE位
  ICSER设置为1（启用从地址y检测）
  AASy标志在帧中第9个SCL时钟周期的上升沿设置为0。
- 当接收到的从地址与(SARUy中的11110b+SVA[1:0])的值匹配，并且后续地址与SARLy值不匹配时，ICSER中的SARyE位设置为1（启用从地址y检测）。AASy标志在帧中第9个SCL时钟周期的上升沿设置为0。

GCA标志（广播呼叫地址检测标志）

GCA标志指示是否检测到广播呼叫地址。

[Setting condition]

- 当接收到的从机地址与广播地址（0000000b+0[W]）匹配时，GCAE位在
  ICSER设置为1（启用广播呼叫地址检测）。
  GCA标志在帧中第9个SCL时钟周期的上升沿设置为1。

[Clearing conditions]

- 读取GCA=1后将0写入GCA标志时
- 检测到停止条件时
- 当接收到的从机地址与广播地址（0000000b+0[W]）不匹配时，GCAE位在
  ICSER设置为1（启用广播地址检测）

The GCA flag is set to 0 on the rising edge of the ninth SCL clock cycle in the frame.

- When 1 is written to the IICRST bit in ICCR1 to apply an IIC reset or an internal reset.

DID flag (Device-ID Address Detection Flag)

The DID flag indicates whether the device-ID address was detected.

[Setting condition]

- When the first frame received immediately after a start or restart condition is detected matches a value of (device ID (1111 100b) + 0 [W]), with the DIDE bit in ICSER set to 1 (device-ID address detection enabled).
  The DID flag is set to 1 on the rising edge of the ninth SCL clock cycle in the frame.

[Clearing conditions]

- When 0 is written to the DID flag after reading DID = 1
- When a stop condition is detected
- When the first frame received immediately after a start or restart condition is detected does not match a value of (device ID (1111 100b)), with the DIDE bit in ICSER set to 1 (device-ID address detection enabled)
  The DID flag is set to 0 on the rising edge of the ninth SCL clock cycle in the frame.
- When the first frame received immediately after a start or restart condition is detected matches a value of (device ID (1111 100b) + 0 [W]), and the second frame does not match any slave address from 0 to 2, with the DIDE bit in ICSER set to 1 (device-ID address detection enabled)
  The DID flag is set to 0 on the rising edge of the ninth SCL clock cycle in the frame.
- When 1 is written to the IICRST bit in ICCR1 to apply an IIC reset or an internal reset.

HOA flag (Host Address Detection Flag)

The HOA flag indicates whether the host address was detected.

[Setting condition]

- When the received slave address matches the host address (0001 000b), with the HOAE bit in ICSER set to 1 (host address detection enabled).
  The HOA flag is set to 1 on the rising edge of the ninth SCL clock cycle in the frame.

[Clearing conditions]

- When 0 is written to the HOA flag after reading HOA = 1
- When a stop condition is detected
- When the received slave address does not match the host address (0001 000b), with the HOAE bit in ICSER set to 1 (host address detection enabled)
  The HOA flag is set to 0 on the rising edge of the ninth SCL clock cycle in the frame.
- When 1 is written to the IICRST bit in ICCR1 to apply an IIC reset or an internal reset.

36.2.10 I2C Bus Status Register 2 (ICSR2)

Address(es): IIC0.ICSR2 4005 3009h, IIC1.ICSR2 4005 3109h, IIC2.ICSR2 4005 3209h

	b7	b6	b5	b4	b3	b2	b1	b0
	TDRE	TEND	RDRF	NACKF	STOP	START	AL	TMOF
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	TMOF	Timeout Detection Flag	0: Timeout not detected 1: Timeout detected.	R/(W) *1

GCA标志在帧中第9个SCL时钟周期的上升沿设置为0。

- 当向ICCR1中的IICRST位写入1时，应用IIC复位或内部复位。

DID标志（Device-ID地址检测标志）

DID标志指示是否检测到设备ID地址。

[Setting condition]

- 当检测到启动或重新启动条件后立即接收到的第一帧与(设备ID(1111100b)+0[W])的值匹配，且ICSER中的DIDE位设置为1（启用设备ID地址检测）。DID标志在帧中第9个SCL时钟周期的上升沿设置为1。

[Clearing conditions]

- 当读取DID=1后将0写入DID标志
- 检测到停止条件时
- 当检测到启动或重新启动条件后立即接收的第一帧与（设备ID（1111100b））的值不匹配时，ICSER中的DIDE位设置为1（启用设备ID地址检测）DID标志为在帧的第9个SCL时钟周期的上升沿设置为0。
- 当检测到启动或重新启动条件后立即接收到的第一帧与(设备ID(1111100b)+0[W])的值匹配，并且第二帧不匹配从0到2的任何从地址时，使用DIDEICSER中的位设置为1（启用设备ID地址检测）

  DID标志在帧中第9个SCL时钟周期的上升沿设置为0。
- 当向ICCR1中的IICRST位写入1时，应用IIC复位或内部复位。

HOA标志（主机地址检测标志）

HOA标志指示是否检测到主机地址。

[Setting condition]

- 当接收到的从机地址与主机地址（0001000b）匹配时，ICSER中的HOAE位设置为1（主机地址检测使能）。HOA标志在帧中第9个SCL时钟周期的上升沿设置为1。

[Clearing conditions]

- 读取HOA=1后将0写入HOA标志时
- 检测到停止条件时
- 当接收到的从机地址与主机地址（0001000b）不匹配时，ICSER中的HOAE位设置为1（主机地址检测使能）在第9个SCL时钟周期的上升沿将HOA标志设置为0框架。
- 当向ICCR1中的IICRST位写入1时，应用IIC复位或内部复位。

36.2.10 I2C总线状态寄存器2(ICSR2)

Address(es): IIC0.ICSR2 4005 3009h, IIC1.ICSR2 4005 3109h, IIC2.ICSR2 4005 3209h

	b7	b6	b5	b4	b3	b2	b1	b0
	TDRE	TEND	RDRF	NACKF	STOP	START	AL	TMOF
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	TMOF	超时检测标志	0：未检测到超时1：检测到超时。	R/(W) *1

Bit	Symbol	Bit name	Description	R/W
b1	AL	Arbitration-Lost Flag	0: Arbitration not lost 1: Arbitration lost.	R/(W) *1
b2	START	Start Condition Detection Flag	0: Start condition not detected 1: Start condition detected.	R/(W) *1
b3	STOP	Stop Condition Detection Flag	0: Stop condition not detected 1: Stop condition detected.	R/(W) *1
b4	NACKF	NACK Detection Flag	0: NACK not detected 1: NACK detected.	R/(W) *1
b5	RDRF	Receive Data Full Flag	0: ICDRR contains no receive data 1: ICDRR contains receive data.	R/(W) *1
b6	TEND	Transmit End Flag	0: Data being transmitted 1: Data transmit complete.	R/(W) *1
b7	TDRE	Transmit Data Empty Flag	0: ICDRT contains transmit data 1: ICDRT contains no transmit data.	R

Note 1. Only 0 can be written, to clear the flag.

TMOF flag (Timeout Detection Flag)

The TMOF flag is set to 1 when the IIC detects a timeout because the SCLn line state remains unchanged for the set period.

[Setting condition]

- When the SCLn line state remains unchanged for the period specified in the ICMR2.TMOH, TMOL, and TMOS bits while the ICFER.TMOE bit is 1 (timeout function enabled) in master or in slave mode and the received slave address matches.

[Clearing conditions]

- When 0 is written to the TMOF flag after reading TMOF = 1
- When 1 is written to the IICRST bit in ICCR1 to apply an IIC reset or an internal reset.

AL flag (Arbitration-Lost Flag)

The AL flag indicates that bus mastership was lost in arbitration because of a bus conflict or some other reason when a start condition was issued or an address and data was transmitted. The IIC monitors the level on the SDAn line during transmission and, if the level on the line does not match the value of the bit being output, is set the value of the AL flag to 1 to indicate that the bus is occupied by another device.

The IIC can also set the flag to indicate the detection of arbitration loss during NACK transmission or during data transmission.

[Setting conditions]

When master arbitration-lost detection is enabled (ICFER.MALE = 1):

- When the internal SDA output state does not match the SDAn line level on the rising edge of the SCL clock except for the ACK period during data transmission in master transmit mode
- When a start condition is detected while the ST bit in ICCR2 is 1 (start condition requested) or the internal SDA output state does not match the SDAn line level
- When the ST bit in ICCR2 is 1 (start condition requested), with the BBSY flag in ICCR2 set to 1.

When NACK arbitration-lost detection is enabled (ICFER.NALE = 1):

- When the internal SDA output state does not match the SDAn line level on the rising edge of the SCL clock in the ACK period during NACK transmission in receive mode.

When slave arbitration-lost detection is enabled (ICFER.SALE = 1):

- When the internal SDA output state does not match the SDAn line level on the rising edge of the SCL clock, except for the ACK period during data transmission in slave transmit mode.

Bit	Symbol	位名称	Description	R/W
b1	AL	Arbitration-Lost Flag	0：仲裁未失败1： 仲裁失败。	R/(W) *1
b2	START	启动条件检测标志	0：未检测到启动条件1：检测 到启动条件。	R/(W) *1
b3	STOP	停止条件检测标志	0：未检测到停止条件1：检 测到停止条件。	R/(W) *1
b4	NACKF	NACK检测标志	0：未检测到NACK1 ：检测到NACK。	R/(W) *1
b5	RDRF	接收数据满标志	0：ICDRR不包含接收数据1：ICDR R包含接收数据。	R/(W) *1
b6	TEND	发送结束标志	0：数据传输中1：数据传 输完成。	R/(W) *1
b7	TDRE	传输数据空标志	0：ICDRT包含发送数据1：ICDRT不 包含发送数据。	R

Note 1. 只能写入0，以清除标志。

TMOF标志（超时检测标志）

当IIC检测到超时时，TMOF标志设置为1，因为SCLn线路状态在设置的周期内保持不变。

[Setting condition]

- 当SCLn线状态在ICMR2.TMOH、TMOL和TMOS位指定的时间段内保持不变，而ICFER.TMOE位在主机或从机模式下为1（启用超时功能）并且接收到的从机地址匹配。

[Clearing conditions]

- 读取TMOF=1后向TMOF标志写入0时
- 当向ICCR1中的IICRST位写入1时，应用IIC复位或内部复位。

AL标志（仲裁失败标志）

AL标志表明在发出启动条件或传输地址和数据时，由于总线冲突或其他原因，总线控制权在仲裁中丢失。IIC在传输过程中监视SDAn线上的电平，如果线上的电平与正在输出的位的值不匹配，则将AL标志的值设置为1，以指示总线被另一个设备占用.

IIC还可以设置该标志以指示在NACK传输期间或数据传输期间检测到仲裁丢失。

[Setting conditions]

当启用主机仲裁丢失检测时(ICFER.MALE=1)：

- 当内部SDA输出状态与SCL时钟上升沿上的SDAn线电平不匹配时，除了在主传输模式下的数据传输期间的ACK周期
- 当ICCR2中的ST位为1（请求启动条件）或内部SDA输出状态与SDAn线电平不匹配时检测到启动条件
- ICCR2中的ST位为1（请求启动条件）时，ICCR2中的BBSY标志设置为1。

当启用NACK仲裁丢失检测时(ICFER.NALE=1)：

- 当内部SDA输出状态与SCL时钟上升沿上的SDAn线电平不匹配时
接收模式下NACK传输期间的ACK周期。

当启用从设备仲裁丢失检测时(ICFER.SALE=1)：

- 当内部SDA输出状态与SCL时钟上升沿上的SDAn线电平不匹配时，除了从机发送模式下数据传输期间的ACK周期。

[Clearing conditions]

- When 0 is written to the AL flag after reading AL = 1
- When 1 is written to the IICRST bit in ICCR1 to apply an IIC reset or an internal reset.

Table 36.4 Relationship between arbitration-lost generation sources and arbitration-lost enable functions

ICFER			ICSR2		
MALE	NALE	SALE	AL	Error	Arbitration-lost generation source
1	×	×	1	Start condition issuance error	When internal SDA output state does not match SDAn line level when a start condition is detected, while the ST bit in ICCR2 is 1
					When ST in ICCR2 is set to 1 while BBSY in ICCR2 is 1
			1	Transmit data mismatch	When transmit data (including slave address) does not match the bus state in master transmit mode
×	1	×	1	NACK transmission mismatch	When ACK is detected during transmission of NACK in master or slave receive mode
×	×	1	1	Transmit data mismatch	When transmit data does not match the bus state in slave transmit mode

×: Don't care

START flag (Start Condition Detection Flag)

The START flag indicates whether a start condition was detected.

[Setting condition]

- When a start (or restart) condition is detected.

[Clearing conditions]

- When 0 is written to the START flag after reading START = 1
- When a stop condition is detected
- When 1 is written to the IICRST bit in ICCR1 to apply an IIC reset or an internal reset.

STOP flag (Stop Condition Detection Flag)

The STOP flag indicates whether a stop condition was detected.

[Setting condition]

- When a stop condition is detected.

[Clearing conditions]

- When 0 is written to the STOP flag after reading STOP = 1
- When 1 is written to the IICRST bit in ICCR1 to apply an IIC reset or an internal reset.

NACKF flag (NACK Detection Flag)

The NACKF flag indicates whether a NACK was detected.

[Setting condition]

- When acknowledge is not received (NACK received) from the receive device in transmit mode, with the NACKE bit in ICFER set to 1 (transfer suspension enabled).

[Clearing conditions]

- When 0 is written to the NACKF flag after reading NACKF = 1
- When 1 is written to the IICRST bit in ICCR1 to apply an IIC reset or an internal reset.

Note: When the NACKF flag is set to 1, the IIC suspends data transmission and reception. Writing to ICDRT in transmit

[Clearing conditions]

- 读取AL=1后向AL标志写入0时
- 当向ICCR1中的IICRST位写入1时，应用IIC复位或内部复位。

Table 36.4 仲裁丢失生成源和仲裁丢失使能函数之间的关系

ICFER			ICSR2		
MALE	NALE	SALE	AL	Error	仲裁失败的生成源
1	×	×	1	开始条件发布错误	当检测到启动条件时内部SDA输出状态与SDAn线电平不匹配，而ICCR2中的ST位为1
					ICCR2中的ST设置为1而ICCR2中的BBSY为1时
			1	传输数据不匹配	当发送数据（包括从地址）与主发送模式下的总线状态不匹配时
×	1	×	1	NACK传输不匹配	在主机或从机接收模式下发送NACK期间检测到ACK时
×	×	1	1	传输数据不匹配	当发送数据与从发送模式下的总线状态不匹配时

×: Don't care

START标志（开始条件检测标志）

START标志指示是否检测到启动条件。

[Setting condition]

- 当检测到启动（或重新启动）条件时。

[Clearing conditions]

- 读取START=1后将0写入START标志时
- 检测到停止条件时
- 当向ICCR1中的IICRST位写入1时，应用IIC复位或内部复位。

停止标志（停止条件检测标志）

STOP标志指示是否检测到停止条件。

[Setting condition]

- 当检测到停止条件时。

[Clearing conditions]

- 在读取STOP=1后将0写入STOP标志时
- 当向ICCR1中的IICRST位写入1时，应用IIC复位或内部复位。

NACKF标志（NACK检测标志）

NACKF标志指示是否检测到NACK。

[Setting condition]

- 当在发送模式下没有从接收设备接收到确认（NACK接收）时，ICFER中的NACKE位设置为1（使能传输暂停）。

[Clearing conditions]

- 读取NACKF=1后将0写入NACKF标志时
- 当向ICCR1中的IICRST位写入1时，应用IIC复位或内部复位。

Note: 当NACKF标志设置为1时，IIC暂停数据发送和接收。在传输中写入ICDRT

mode or reading from ICDRR in receive mode with the NACKF flag set to 1 does not enable data transmit or receive operation. To restart data transmission or reception, set the NACKF flag to 0.

RDRF flag (Receive Data Full Flag)

The RDRF flag indicates whether the IDCRR contains receive data.

[Setting conditions]

- When receive data is transferred from ICDRS to ICDRR
  The RDRF flag is set to 1 on the rising edge of the eighth or ninth SCL clock cycle (selected in the RDRFS bit in ICMR3).
- When the received slave address matches after a start (or restart) condition is detected with the TRS bit in ICCR2 set to 0.

[Clearing conditions]

- When 0 is written to the RDRF flag after reading RDRF = 1
- When data is read from ICDRR
- When 1 is written to the IICRST bit in ICCR1 to apply an IIC reset or an internal reset.

TEND flag (Transmit End Flag)

The TEND flag indicates whether data transmission is still being transmitted or is complete.

[Setting condition]

- On the rising edge of the ninth SCL clock cycle while the TDRE flag is 1.

[Clearing conditions]

- When 0 is written to the TEND flag after reading TEND = 1
- When data is written to ICDRT
- When a stop condition is detected
- When 1 is written to the IICRST bit in ICCR1 to apply an IIC reset or an internal reset.

TDRE flag (Transmit Data Empty Flag)

The TDRE flag indicates whether the ICDRT contains transmit data.

[Setting conditions]

- When data is transferred from ICDRT to ICDRS and ICDRT becomes empty
- When the TRS bit in ICCR2 is set to 1
- When the received slave address matches while the TRS bit is 1.

[Clearing conditions]

- When data is written to ICDRT
- When the TRS bit in ICCR2 is set to 0
- When 1 is written to the IICRST bit in ICCR1 to apply an IIC reset or an internal reset.

Note: When the NACKF flag is set to 1 while the NACKE bit in ICFER is 1, the IIC suspends data transmission and reception. Here, if the TDRE flag is 0 (next transmit data written), data is transferred to the ICDRS register and the ICDRT register becomes empty on the rising edge of the ninth clock cycle, but the TDRE flag does not set to 1.

模式或在NACKF标志设置为1的接收模式下从ICDRR读取不会启用数据发送或接收操作。要重新开始数据发送或接收，请将NACKF标志设置为0。

RDRF标志（接收数据满标志）

RDRF标志指示IDCRR是否包含接收数据。

[Setting conditions]

- 当接收数据从ICDRS传输到ICDRR
  RDRF标志在第8个或第9个SCL时钟周期的上升沿设置为1（在RDRFS位中选择ICMR3).
- 当ICCR2中的TRS位设置为0检测到启动（或重新启动）条件后接收到的从机地址匹配时。

[Clearing conditions]

- 读取RDRF=1后向RDRF标志写入0时
- 从ICDRR读取数据时
- 当向ICCR1中的IICRST位写入1时，应用IIC复位或内部复位。

TEND标志（发送结束标志）

TEND标志指示数据传输是否仍在传输中或已完成。

[Setting condition]

- 在第9个SCL时钟周期的上升沿，同时TDRE标志为1。

[Clearing conditions]

- 读取TEND=1后将0写入TEND标志时
- 数据写入ICDRT时
- 检测到停止条件时
- 当向ICCR1中的IICRST位写入1时，应用IIC复位或内部复位。

TDRE标志（传输数据空标志）

TDRE标志指示ICDRT是否包含发送数据。

[Setting conditions]

- 当数据从ICDRT传输到ICDRS并且ICDRT变为空时
- ICCR2中的TRS位设置为1时
- 当TRS位为1时接收到的从机地址匹配。

[Clearing conditions]

- 数据写入ICDRT时
- ICCR2中的TRS位设置为0时
- 当向ICCR1中的IICRST位写入1时，应用IIC复位或内部复位。

Note: 当ICFER的NACKE位为1时NACKF标志设置为1，IIC暂停数据发送和接收。此处，如果TDRE标志为0（写入下一个发送数据），则数据被传送到ICDRS寄存器，并且ICDRT寄存器在第9个时钟周期的上升沿变为空，但TDRE标志不设置为1。

36.2.11 I2C Bus Wakeup Unit Register (ICWUR)

Address(es): IIC0.ICWUR 4005 3016h

	b7	b6	b5	b4	b3	b2	b1	b0
	WUE	WUIE	WUF	WUACK	—	—	—	WUAFA
Value after reset:	0	0	0	1	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	WUAFA	Wakeup Analog Filter Additional Selection	0: Do not add the wakeup analog filter 1: Add the wakeup analog filter.	R/W
b3 to b1	—	Reserved	These bit are read as 0. The write value should be 0.	R/W
b4	WUACK	ACK Bit for Wakeup Mode	Choice of four response modes in combination with ICCR1.IICRST and WUACK. See Table 36.5.	R/W
b5	WUF	Wakeup Event Occurrence Flag	0: Slave address not matching during wakeup 1: Slave address matching during wakeup.	R/W
b6	WUIE	Wakeup Interrupt Request Enable	0: Disable wakeup interrupt request (IIC0_WUI) 1: Enable wakeup interrupt request (IIC0_WUI).	R/W
b7	WUE	Wakeup Function Enable	0: Disable wakeup function 1: Enable wakeup function.	R/W

Table 36.5 Wakeup mode

IICRST	WUACK	Operation mode	Description
0	0	Normal wakeup mode 1	ACK response on ninth SCL, and SCL low-hold after ninth SCL.
0	1	Normal wakeup mode 2	No ACK response immediately and SCL low-hold between eight and ninth SCL. SCL low-hold release and ACK response on ninth SCL.
1	0	Command recovery mode	ACK response on ninth SCL and no SCL low-hold.
1	1	EEP response mode	NACK response on ninth SCL and no SCL low-hold.

WUF flag (Wakeup Event Occurrence Flag)

The WUF flag indicates whether the slave address is matching during wakeup.

[Setting condition]

- When PCLKB is supplied after a slave-address match in the first eighth SCL low during wakeup mode.

[Clearing conditions]

- When 0 is written to the WUF flag after reading WUF = 1
- When ICE = 0 and IICRST = 1.

36.2.11 I2C总线唤醒单元寄存器(ICWUR)

Address(es): IIC0.ICWUR 4005 3016h

	b7	b6	b5	b4	b3	b2	b1	b0
	WUE	WUIE	WUF	WUACK	—	—	—	WUAFA
重置后的值:	0	0	0	1	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	WUAFA	唤醒模拟滤波器附加选择	0：不加唤醒模拟滤波器1：加唤醒模拟滤波器。	R/W
b3 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b4	WUACK	唤醒模式的ACK位	四种响应模式的选择结合ICCR1.IICRST和WUACK。见表36.5。	R/W
b5	WUF	唤醒事件发生标志	0：唤醒期间从机地址不匹配1：唤醒期间从机地址匹配。	R/W
b6	WUIE	唤醒中断请求使能	0：禁用唤醒中断请求（IIC0_WUI）1：启用唤醒中断请求（IIC0_WUI）。	R/W
b7	WUE	唤醒功能启用	0：禁用唤醒功能1：启用唤醒功能。	R/W

Table 36.5 唤醒模式

IICRST	WUACK	操作模式	Description
0	0	正常唤醒模式1	第9个SCL的ACK响应，以及第9个SCL之后的SCL低保持。
0	1	正常唤醒模式2	没有ACK立即响应，并且SCL在8到9之间保持低电平SCL。SCL低保持释放和第九个SCL的ACK响应。
1	0	命令恢复模式	第9个SCL的ACK响应且没有SCL低保持。
1	1	EEP响应模式	第九个SCL上的NACK响应且没有SCL低保持。

WUF标志（唤醒事件发生标志）

WUF标志指示在唤醒期间从地址是否匹配。

[Setting condition]

- 当PCLKB在唤醒模式下第一个8个SCL低电平的从地址匹配后提供时。

[Clearing conditions]

- 读取WUF=1后向WUF标志写入0时
- 当ICE=0且IICRST=1时。

36.2.12 I2C Bus Wakeup Unit Register 2 (ICWUR2)

Address(es): IIC0.ICWUR2 4005 3017h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	WUSYF	WUASYF	WUSEN
Value after reset:	1	1	1	1	1	1	0	1

Bit	Symbol	Bit name	Description	R/W
b0	WUSEN	Wakeup Function Synchronous Enable	0: IIC asynchronous circuit enable 1: IIC synchronous circuit enable.	R/W
b1	WUASYF	Wakeup Function Asynchronous Operation Status Flag	0: IIC synchronous circuit enable condition 1: IIC asynchronous circuit enable condition.	R
b2	WUSYF	Wakeup Function Synchronous Operation Status Flag	0: IIC asynchronous circuit enable condition 1: IIC synchronous circuit enable condition.	R
b7 to b3	—	Reserved	These bits are read as1. The write value should be 1.	R/W

WUSEN bit (Wakeup Function Synchronous Enable)

It combines with the WUASYF flag (or WUSYF flag) at wakeup effective function (ICWUR.WUE = 1), and the PCLKB synchronous operation and the PCLKB asynchronous operation are switched.

[When switching from the PCLKB synchronous operation to the PCLKB asynchronous operation]

It changes into the PCLKB asynchronous operation when the ICCR2.BBSY flag is 0 if the WUASYF flag writes 0 in the WUSEN bit in the state of 0. The reception can operate without depending on the state of operation of PCLKB (with PCLKB stopped) after it switches to the PCLKB asynchronous operation (wakeup event detection operation).

[When switching from the PCLKB asynchronous operation to the PCLKB synchronous operation]

It changes into the PCLKB synchronization and the WUASYF flag becomes 0 at once after writing of 1 when the wakeup event is detected if 1 is written in the WUSEN bit when the WUASYF flag is 1. At the same time, WUASYF flag becomes 0. In other case, it changes into the PCLKB synchronous operation when the stop condition is detected at the wakeup event undetected.

WUASYF flag (Wakeup Function Asynchronous Operation Status Flag)

It is shown that IIC is in the PCLKB asynchronous operation at wakeup effective function (ICWUR.WUE = 1).

[Setting condition]

- When the ICCR2.BBSY flag is 0 with the ICWUR.WUE bit set to 1 after writing 0 to the WUSEN bit.

[Clearing conditions]

- When 1 is written to the WUSEN bit after detecting the wakeup event with ICWUR.WUE bit set to 1.
- When a stop condition is detected with WUSEN bit set to 1 before detecting the wakeup event with WUASY flag set to 1 with ICWUR.WUE bit set to 1.
- When you write 1 in the WUSEN bit with the WUASYF flag detected 1 and the wakeup event in the state of ICWUR.WUE = 1.
- ICCR1.ICE = 0 and ICCRST = 1 (ICC reset)
- ICWUR.WUE = 0.

WUSYF flag (Wakeup Function Synchronous Operation Status Flag)

It is shown that IIC is in the PCLKB synchronous operation at wakeup effective function (ICWUR.WUE = 1). This flag is a value in which the WUASYF flag is always reserved.

36.2.12 I2C总线唤醒单元寄存器2(ICWUR2)

Address(es): IIC0.ICWUR2 4005 3017h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	WUSYF	WUASYF	WUSEN
重置后的值：	1	1	1	1	1	1	0	1

Bit	Symbol	位名称	Description	R/W
b0	WUSEN	唤醒功能同步使能	0：IIC异步电路使能1：IIC同步电路使能。	R/W
b1	WUASYF	唤醒功能异步操作状态标志	0：IIC同步电路使能条件1：IIC异步电路使能条件。	R
b2	WUSYF	唤醒功能同步操作状态标志	0：IIC异步电路使能条件1：IIC同步电路使能条件。	R
b7 to b3	—	Reserved	这些位被读取为1。写入值应为1。	R/W

WUSEN位（唤醒功能同步使能）

它在唤醒有效功能（ICWUR.WUE=1）时与WUASYF标志（或WUSYF标志）结合，切换PCLKB同步操作和PCLKB异步操作。

[从PCLKB同步操作切换到PCLKB异步操作时]

如果WUASYF标志在
WUSEN位处于0状态。接收可以在不依赖于PCLKB的操作状态的情况下进行操作（与PCLKB停止）后切换到PCLKB异步操作（唤醒事件检测操作）。

[从PCLKB异步操作切换到PCLKB同步操作时]

当WUASYF标志为1时，如果向WUSEN位写入1，则当WUASYF标志为1时，写入1后，WUASYF标志立即变为0。同时，WUASYF标志变为0。其他情况下，当在未检测到唤醒事件时检测到停止条件时，它变为PCLKB同步操作。

WUASYF标志（唤醒功能异步操作状态标志）

表明IIC在唤醒有效功能(ICWUR.WUE=1)时处于PCLKB异步操作。

[Setting condition]

- 当ICCR2.BBSY标志为0且ICWUR.WUE位在WUSEN位写入0后设置为1时。

[Clearing conditions]

- 当检测到唤醒事件后将1写入WUSEN位，且ICWUR.WUE位设置为1。
- 在检测到WUASY标志设置为1且ICWUR.WUE位设置为1的唤醒事件之前检测到WUSEN位设置为1的停止条件时。
- 当您向WUSEN位写入1时，检测到WUASYF标志为1，并且唤醒事件处于ICWUR.WUE = 1.
- ICCR1.ICE = 0 and ICCRST = 1 (ICC reset)
- ICWUR.WUE = 0.

WUSYF标志（唤醒功能同步操作状态标志）

表明IIC在唤醒有效功能(ICWUR.WUE=1)时处于PCLKB同步操作。此标志是WUASYF标志始终保留的值。

[Setting conditions]

- When 1 is written to the WUSEN bit after detecting the wakeup event with ICWUR.WUE bit set to 1 with WUSYF flag cleared to 0 with ICWUR.WUE bit set to 1.
- When a stop condition is detected with WUSEN bit set to 1 before detecting the wakeup event with WUSYF flag cleared to 0 with ICWUR.WUE bit set to 1.
- ICCR1.ICE = 0 and ICCRST = 1 (ICC reset)
- ICWUR.WUE = 0.

[Clearing condition]

- When the ICCR2.BBSY flag is 0 with the ICWUR.WUE bit set to 1 after writing 0 to the WUSEN bit.

36.2.13 Slave Address Register L y (SARLy) (y = 0 to 2)

Address(es): IIC0.SARL0 4005 300Ah, IIC1.SARL0 4005 310Ah, IIC2.SARL0 4005 320Ah, IIC0.SARL1 4005 300Ch, IIC1.SARL1 4005 310Ch, IIC2.SARL1 4005 320Ch, IIC0.SARL2 4005 300Eh, IIC1.SARL2 4005 310Eh, IIC2.SARL2 4005 320Eh

	b7	b6	b5	b4	b3	b2	b1	b0
	SVA[6:0]							SVA0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	SVA0	10-Bit Address LSB	Slave address setting.	R/W
b7 to b1	SVA[6:0]	7-Bit Address/10-Bit Address Lower Bits	Slave address setting.	R/W

SVA0 bit (10-Bit Address LSB)

When the 10-bit address format is selected (SARUy.FS = 1), the SVA0 bit functions as the LSB of a 10-bit address and is combined with the SVA[6:0] bits to form the lower 8 bits of a 10-bit address.

This bit is valid when the SARyE bit in ICSER is set to 1 (SARLy and SARUy enabled) and the SARUy.FS bit is 1. When the SARUy.FS or SARyE bit is 0, the setting in this bit is ignored.

SVA[6:0] bits (7-Bit Address/10-Bit Address Lower Bits)

When the 7-bit address format is selected (SARUy.FS = 0), the SVA[6:0] bits function as a 7-bit address. When the 10-bit address format is selected (SARUy.FS = 1), these bits combine with the SVA0 bit to form the lower 8 bits of a 10-bit address.

When the SARyE bit in ICSER is 0, the setting in these bits is ignored.

36.2.14 Slave Address Register U y (SARUy) (y = 0 to 2)

Address(es): IIC0.SARU0 4005 300Bh, IIC1.SARU0 4005 310Bh, IIC2.SARU0 4005 320Bh, IIC0.SARU1 4005 300Dh, IIC1.SARU1 4005 310Dh, IIC2.SARU1 4005 320Dh, IIC0.SARU2 4005 300Fh, IIC1.SARU2 4005 310Fh, IIC2.SARU2 4005 320Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	SVA[1:0]		FS
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	FS	7-Bit/10-Bit Address Format Select	0: Select 7-bit address format 1: Select 10-bit address format.	R/W

[Setting conditions]

- 当检测到唤醒事件后将1写入WUSEN位时，ICWUR.WUE位设置为1，WUSYF标志清零，ICWUR.WUE位设置为1。
- 当检测到WUSEN位设置为1的停止条件时，在检测到唤醒事件之前将WUSYF标志清零且ICWUR.WUE位设置为1。
- ICCR1.ICE = 0 and ICCRST = 1 (ICC reset)
- ICWUR.WUE = 0.

[Clearing condition]

- 当ICCR2.BBSY标志为0且ICWUR.WUE位在WUSEN位写入0后设置为1时。

36.2.13 从地址寄存器Ly(SARLy)(y=0to2)

Address(es): IIC0.SARL0 4005 300Ah, IIC1.SARL0 4005 310Ah, IIC2.SARL0 4005 320Ah, IIC0.SARL1 4005 300Ch, IIC1.SARL1 4005 310Ch, IIC2.SARL1 4005 320Ch, IIC0.SARL2 4005 300Eh, IIC1.SARL2 4005 310Eh, IIC2.SARL2 4005 320Eh

	b7	b6	b5	b4	b3	b2	b1	b0
	SVA[6:0]							SVA0
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	SVA0	10-Bit Address LSB	从机地址设置。	R/W
b7 to b1	SVA[6:0]	7位地址10位地址低位	从机地址设置。	R/W

SVA0位（10位地址LSB）

Whenthe10-bitaddressformatisselected(SARUy.FS=1) theSVA0bitfunctionsastheLSBofa10-bitaddressandiscombinedwiththeSVA[6:0]bitstoformthelower8bitsofa10位地址。

当ICSER中的SARyE位设置为1（启用SARLy和SARUy）且SARUy.FS位为1时，该位有效。
当SARUy.FS或SARyE位为0时，忽略该位的设置。

SVA[6:0]位（7位地址10位地址低位）

Whenthe7-bitaddressformatisselected(SARUy.FS=0) theSVA[6:0]bitsfunctionasa7-bitaddress.Whenthe10bitaddressformatisselected(SARUy.FS=1) thesebitscombinewiththeSVA0bittoformthelower8bitsofa10-bitaddress.

当ICSER中的SARyE位为0时，这些位中的设置将被忽略。

36.2.14 从地址寄存器Uy(SARUy)(y=0to2)

Address(es): IIC0.SARU0 4005 300Bh, IIC1.SARU0 4005 310Bh, IIC2.SARU0 4005 320Bh, IIC0.SARU1 4005 300Dh, IIC1.SARU1 4005 310Dh, IIC2.SARU1 4005 320Dh, IIC0.SARU2 4005 300Fh, IIC1.SARU2 4005 310Fh, IIC2.SARU2 4005 320Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	SVA[1:0]		FS
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	FS	7位10位地址格式选择	0：选择7位地址格式1：选择1 0位地址格式。	R/W

Bit	Symbol	Bit name	Description	R/W
b2, b1	SVA[1:0]	10-Bit Address Upper Bits	Slave address setting.	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

FS bit (7-Bit/10-Bit Address Format Select)

The FS bit selects 7- or 10-bit format for slave address y (in SARLy and SARUy).

When the SARyE bit in ICSER is set to 1 (SARLy and SARUy enabled) and the SARUy.FS bit is 0, the 7-bit address format is selected for slave address y, the SVA[6:0] setting in SARLy is valid, and the SVA[1:0] and SVA0 settings in SARLy are ignored.

When the SARyE bit in ICSER is set to 1 (SARLy and SARUy enabled) and the SARUy.FS bit is 1, the 10-bit address format is selected for slave address y and the SVA[1:0] and SARLy settings are valid.

When the SARyE bit in ICSER is 0 (SARLy and SARUy disabled), the SARUy.FS setting is invalid.

SVA[1:0] bits (10-Bit Address Upper Bits)

When the 10-bit address format is selected (FS = 1), the SVA[1:0] bits function as the upper 2 bits of a 10-bit address.

These bits are valid when the SARyE bit in ICSER is set to 1 (SARLy and SARUy enabled) and the SARUy.FS bit is 1. When the SARUy.FS or SARyE bit is 0, the setting in these bits is ignored.

36.2.15 I2C Bus Bit Rate Low-Level Register (ICBRL)

Address(es): IIC0.ICBRL 4005 3010h, IIC1.ICBRL 4005 3110h, IIC2.ICBRL 4005 3210h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	BRL[4:0]				
Value after reset:	1	1	1	1	1	1	1	1

Bit	Symbol	Bit name	Description	R/W
b4 to b0	BRL[4:0]	Bit Rate Low-Level Period	Low-level period of SCL clock.	R/W
b7 to b5	—	Reserved	These bits are read as 1. The write value should be 1.	R/W

ICBRL is a 5-bit register that sets the low-level period of the SCL clock. ICBRL also works to generate the data setup time for the automatic SCL low-hold operation (see section 36.9, Automatic Low-Hold Function for SCL). When the IIC is used only in slave mode, this register must be set to a value longer than the data setup time.*1 ICBRL counts the low-level period with the internal reference clock source (IICϕ) specified in the CKS[2:0] bits in ICMR1. If the digital noise filter is enabled (the NFE bit in ICFER is 1), set the ICBRL register to a value at least one greater than the number of stages in the noise filter. For this number, see the description of the ICMR3.NF[1:0] bits.

Note 1. Data setup time (tSU: DAT)
250 ns for up to 100 kbps: Standard-mode (Sm)
100 ns for up to 400 kbps: Fast-mode (Fm)
50 ns for up to 1 Mbps: Fast-mode plus (Fm+)

Bit	Symbol	位名称	Description	R/W
b2, b1	SVA[1:0]	10位地址高位	从机地址设置。	R/W
b7 to b3	—	Reserved	这些位被读取为0。写入值应为0。	R/W

FS位（7位10位地址格式选择）

FS位为从地址y选择7位或10位格式（在SARLy和SARUy中）。

当ICSER中的SARyE位设置为1（启用SARLy和SARUy）且SARUy.FS位为0时，从机地址y选择7位地址格式，SARLy中的SVA[6:0]设置有效 并且忽略SARLy中的SVA[1:0]和SVA0设置。

当ICSER中的SARyE位设置为1（启用SARLy和SARUy）且SARUy.FS位为1时，从机地址y选择10位地址格式且SVA[1:0]和SARLy设置有效.

当ICSER中的SARyE位为0（SARLy和SARUy禁用）时，SARUy.FS设置无效。

SVA[1:0]位（10位地址高位）

Whenthe10-bitaddressformatisselected(FS=1) theSVA[1:0]bitsfunctionastheupper2bitsofa10-bitaddress.

当ICSER中的SARyE位设置为1（启用SARLy和SARUy）且SARUy.FS位为1时，这些位有效。
当SARUy.FS或SARyE位为0时，这些位中的设置将被忽略。

36.2.15 I2C总线比特率低电平寄存器(ICBRL)

Address(es): IIC0.ICBRL 4005 3010h, IIC1.ICBRL 4005 3110h, IIC2.ICBRL 4005 3210h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	BRL[4:0]				
重置后的值:	1	1	1	1	1	1	1	1

Bit	Symbol	位名称	Description	R/W
b4 to b0	BRL[4:0]	比特率低电平周期	SCL时钟的低电平周期。	R/W
b7 to b5	—	Reserved	这些位被读取为1。写入值应为1。	R/W

ICBRL是一个5位寄存器，用于设置SCL时钟的低电平周期。ICBRL还用于为自动SCL低保持操作生成数据建立时间（参见第36.9节，SCL的自动低保持功能）。当IIC仅用于从机模式时，该寄存器必须设置为比数据建立时间更长的值。*1ICBRL使用ICMR1的CKS[2:0]位中指定的内部参考时钟源(IIC)对低电平周期进行计数。如果启用了数字噪声滤波器（ICFER中的NFE位为1），请将ICBRL寄存器设置为至少比噪声滤波器中的级数大1的值。对于这个数字，请参见ICMR3.NF[1:0]位的描述。

注1.数据建立时间(tSU:DAT)
250ns，最高100kbps：标准模式(Sm)100ns，
最高400kbps：快速模式(Fm)50ns，最高1Mbps
：快速模式加(Fm+)

36.2.16 I2C Bus Bit Rate High-Level Register (ICBRH)

Address(es): IIC0.ICBRH 4005 3011h, IIC1.ICBRH 4005 3111h, IIC2.ICBRH 4005 3211h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	BRH[4:0]				
Value after reset:	1	1	1	1	1	1	1	1

Bit	Symbol	Bit name	Description	R/W
b4 to b0	BRH[4:0]	Bit Rate High-Level Period	High-level period of SCL clock.	R/W
b7 to b5	—	Reserved	These bits are read as 1. The write value should be 1.	R/W

ICBRH is a 5-bit register that sets the high-level period of the SCL clock. ICBRH is valid in master mode. If the IIC is used only in slave mode, no setting is required in this register. ICBRH counts the high-level period with the internal reference clock source (IICϕ) specified in the CKS[2:0] bits in ICMR1. If the digital noise filter is enabled (the NFE bit in ICFER is 1), set the ICBRH register to a value at least one greater than the number of stages in the noise filter. For this number, see the description of the ICMR3.NF[1:0] bits.

The IIC transfer rate and the SCL clock duty are calculated using the following expressions (1) to (5):

1. ICFER.SCLE = 0
   Transfer rate = $1/\{[(BRH + 1) + (BRL + 1)]/IIC\varphi^{*1} + tr^{*2} + tf^{*2}\}$
   Duty cycle = $\{tr + [(BRH + 1)/IIC\varphi]\}/\{tr + tf + [(BRH + 1) + (BRL + 1)]/IIC\varphi\}$
2. ICFER.SCLE = 1 and ICFER.NFE = 0 and CKS[2:0] = 000b (IICφ = PCLKB)
   Transfer rate = $1/\{[(BRH + 3) + (BRL+ 3)]/IIC\varphi + tr + tf\}$
   Duty cycle = $\{tr + [(BRH + 3)/IIC\varphi]\}/\{tr + tf + [(BRH + 3) + (BRL + 3)]/IIC\varphi\}$
3. ICFER.SCLE = 1 and ICFER.NFE = 1 and CKS[2:0] = 000b (IICφ = PCLKB)
   Transfer rate = $1/\{[(BRH + 3 + nf^{*3}) + (BRL + 3 + nf)]/IIC\varphi + tr + tf\}$
   Duty cycle = $\{tr + [(BRH + 3 + nf)/IIC\varphi]\}/\{tr + tf + [(BRH + 3 + nf) + (BRL + 3 + nf)]/IIC\varphi\}$
4. ICFER.SCLE = 1 and ICFER.NFE = 0 and CKS[2:0] ≠ 000b
   Transfer rate = $1/\{[(BRH + 2) + (BRL + 2)]/IIC\varphi + tr + tf\}$
   Duty cycle = $\{tr + [(BRH + 2)/IIC\varphi]\}/\{tr + tf + [(BRH + 2) + (BRL + 2)]/IIC\varphi\}$
5. ICFER.SCLE = 1 and ICFER.NFE = 1 and CKS[2:0] ≠ 000b
   Transfer rate = $1/\{[(BRH + 2 + nf) + (BRL + 2 + nf)]/IIC\varphi + tr + tf\}$
   Duty cycle = $\{tr + [(BRH + 2 + nf)/IIC\varphi]\}/\{tr + tf + [(BRH + 2 + nf) + (BRL + 2 + nf)]/IIC\varphi\}$

Note 1. IICφ = PCLKB × division ratio
Note 2. The SCLn line rise time (tr) and SCLn line fall time (tf) depend on the total bus line capacitance (Cb) and the pull-up resistor (Rp). For details, see the I2C bus standard from NXP Semiconductors.
Note 3. nf = Number of digital noise filters selected in the ICMR3.NF bit.

Table 36.6 Example of ICBRH/ICBRL settings for transfer rate when SCLE = 0

Transfer rate (kbps)	CKS[2:0]	BRH[4:0](ICBRH)	BRL[4:0](ICBRL)	PCLKB (MHz)	NF[1:0]	Computation expression
100	100b	14 (EEh)	17 (F1h)	60	—	(1)
400	010b	8 (E8h)	19 (F3h)	60	—	(1)
1000	000b	15 (EFh)	29 (FDh)	60	—	(1)

36.2.16 I2C总线比特率高级寄存器(ICBRH)

Address(es): IIC0.ICBRH 4005 3011h, IIC1.ICBRH 4005 3111h, IIC2.ICBRH 4005 3211h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	BRH[4:0]				
重置后的值:	1	1	1	1	1	1	1	1

Bit	Symbol	位名称	Description	R/W
b4 to b0	BRH[4:0]	比特率高级期	SCL时钟的高电平周期。	R/W
b7 to b5	—	Reserved	这些位被读取为1。写入值应为1。	R/W

ICBRH是一个5位寄存器，用于设置SCL时钟的高电平周期。ICBRH在主模式下有效。如果IIC仅用于从机模式，则无需对该寄存器进行设置。ICBRH使用ICMR1的CKS[2:0]位中指定的内部参考时钟源(IIC　)计算高电平周期。如果启用了数字噪声滤波器（ICFER中的NFE位为1），请将ICBRH寄存器设置为至少比噪声滤波器中的级数大1的值。对于这个数字，请参见ICMR3.NF[1:0]位的描述。

IIC传输速率和SCL时钟占空比使用以下表达式(1)到(5)计算：

1. ICFER.SCLE = 0
   传输率=$1\{[(BRH+1)+(BRL+1)]IIC\phi*1+tr*2+tf*2$
   占空比=$\{tr+[(BRH+1)IIC\phi]\ \{tr+tf+[(BRH+1)+(BRL+1)]IIC\phi$
2. ICFER.SCLE = 1 and ICFER.NFE = 0 and CKS[2:0] = 000b (IICφ = PCLKB)
   传输率=$1\{[(BRH+3)+(BRL+3)]IIC\phi+tr+tf$
   占空比=$\{tr+[(BRH+3)IIC\phi]\ \{tr+tf+[(BRH+3)+(BRL+3)]IIC\phi$
3. ICFER.SCLE = 1 and ICFER.NFE = 1 and CKS[2:0] = 000b (IICφ = PCLKB)
   传输率=$1\{[(BRH+3+nf*3)+(BRL+3+nf)]IIC\phi+tr+tf$
   占空比=$\{tr+[(BRH+3+nf)IIC\phi]\ \{tr+tf+[(BRH+3+nf)+(BRL+3+nf)]IIC\phi$
4. ICFER.SCLE = 1 and ICFER.NFE = 0 and CKS[2:0] ≠ 000b
   传输率=$1\{[(BRH+2)+(BRL+2)]IIC\phi+tr+tf$
   占空比=$\{tr+[(BRH+2)IIC\phi]\ \{tr+tf+[(BRH+2)+(BRL+2)]IIC\phi$
5. ICFER.SCLE = 1 and ICFER.NFE = 1 and CKS[2:0] ≠ 000b
   传输率=$1\{[(BRH+2+nf)+(BRL+2+nf)]IIC\phi+tr+tf$
   占空比=$\{tr+[(BRH+2+nf)IIC\phi]\ \{tr+tf+[(BRH+2+nf)+(BRL+2+nf)]IIC\phi$

注1.IICφ=PCLKB×分频比
注2.SCLn线路上升时间(tr)和SCLn线路下降时间(tf)取决于总总线电容(Cb)和上拉电阻(Rp)。有关详细信息，请参阅NXPSemiconductors的I2C总线标准。注3.nf=在ICMR3.NF位中选择的数字噪声滤波器的数量。

Table 36.6 SCLE=0时传输速率的ICBRHICBRL设置示例

传输速率(kbps)	CKS[2:0]	BRH[4:0](ICBRH)	BRL[4:0](ICBRL)	PCLKB (MHz)	NF[1:0]	计算表达式
100	100b	14 (EEh)	17 (F1h)	60	—	(1)
400	010b	8 (E8h)	19 (F3h)	60	—	(1)
1000	000b	15 (EFh)	29 (FDh)	60	—	(1)

Table 36.7 Example of ICBRH/ICBRL settings for transfer rate when SCLE = 1 and NFE = 0

Transfer rate (kbps)	CKS[2:0]	BRH[4:0](ICBRH)	BRL[4:0](ICBRL)	PCLKB (MHz)	NF[1:0]	Computation expression
100	100b	13 (EDh)	16 (F0h)	60	—	(4)
400	010b	7 (E7h)	18 (F2h)	60	—	(4)
1000	000b	13 (EDh)	27 (FBh)	60	—	(2)

Table 36.8 Example of ICBRH/ICBRL settings for transfer rate when SCLE = 1 and NFE = 1

Transfer rate (kbps)	CKS[2:0]	BRH[4:0](ICBRH)	BRL[4:0](ICBRL)	PCLKB (MHz)	NF[1:0]	Computation expression
100	100b	11 (EBh)	14 (EEh)	60	01b	(5)
400	010b	5 (E5h)	16 (F0h)	60	01b	(5)
1000	000b	11 (EBh)	25 (F9h)	60	01b	(3)

36.2.17 I2C Bus Transmit Data Register (ICDRT)

Address(es): IIC0.ICDRT 4005 3012h, IIC1.ICDRT 4005 3112h, IIC2.ICDRT 4005 3212h

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1

When ICDRT detects a space in the IIC-Bus Shift Register (ICDRS), it transfers the transmit data that was written to ICDRT to ICDRS and starts transmitting data in transmit mode. The double-buffer structure of ICDRT and ICDRS allows continuous transmit operation if the next transmit data is written to ICDRT while the ICDRS data is being transmitted.

ICDRT can always be read and written to. Write transmit data to ICDRT once when a transmit data empty interrupt (IICn_TXI) request is generated.

36.2.18 I2C Bus Receive Data Register (ICDRR)

Address(es): IIC0.ICDRR 4005 3013h, IIC1.ICDRR 4005 3113h, IIC2.ICDRR 4005 3213h

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0

When 1 byte of data is received, the received data is transferred from the IIC-Bus Shift Register (ICDRS) to ICDRR to enable the next data to be received. The double-buffer structure of ICDRS and ICDRR allows continuous receive operation if the received data is read from ICDRR while ICDRS is receiving data. ICDRR cannot be written to. Read data from ICDRR once when a receive data full interrupt (IICn_RXI) request is generated.

If ICDRR receives the next receive data before the current data is read from ICDRR (while the RDRF flag in ICSR2 is 1), the IIC automatically holds the SCL clock low 1 cycle before the RDRF flag is set to 1 next.

Table 36.7 SCLE=1和NFE=0时传输速率的ICBRHICBRL设置示例

传输速率(kbps)	CKS[2:0]	BRH[4:0](ICBRH)	BRL[4:0](ICBRL)	PCLKB (MHz)	NF[1:0]	计算表达式
100	100b	13 (EDh)	16 (F0h)	60	—	(4)
400	010b	7 (E7h)	18 (F2h)	60	—	(4)
1000	000b	13 (EDh)	27 (FBh)	60	—	(2)

Table 36.8 SCLE=1和NFE=1时传输速率的ICBRHICBRL设置示例

传输速率(kbps)	CKS[2:0]	BRH[4:0](ICBRH)	BRL[4:0](ICBRL)	PCLKB (MHz)	NF[1:0]	计算表达式
100	100b	11 (EBh)	14 (EEh)	60	01b	(5)
400	010b	5 (E5h)	16 (F0h)	60	01b	(5)
1000	000b	11 (EBh)	25 (F9h)	60	01b	(3)

36.2.17 I2C总线发送数据寄存器(ICDRT)

Address(es): IIC0.ICDRT 4005 3012h, IIC1.ICDRT 4005 3112h, IIC2.ICDRT 4005 3212h

	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	1	1	1	1	1	1	1	1

当ICDRT检测到IIC总线移位寄存器(ICDRS)中有空间时，它会将写入的发送数据传输到ICDRT到ICDRS并开始在传输模式下传输数据。ICDRT和ICDRS的双缓冲结构允许在传输ICDRS数据的同时将下一个传输数据写入ICDRT的连续传输操作。

ICDRT始终可以被读取和写入。当产生发送数据空中断（IICn_TXI）请求时，将发送数据写入ICDRT。

36.2.18 I2C总线接收数据寄存器(ICDRR)

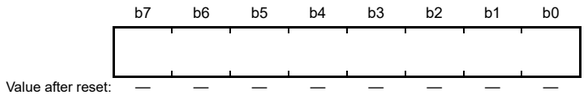
Address(es): IIC0.ICDRR 4005 3013h, IIC1.ICDRR 4005 3113h, IIC2.ICDRR 4005 3213h

	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	0	0	0	0	0	0	0	0

当接收到1个字节的数据时，接收到的数据会从IIC总线移位寄存器(ICDRS)传输到ICDRR，以便接收下一个数据。如果在ICDRS正在接收数据时从ICDRR读取接收到的数据，ICDRS和ICDRR的双缓冲结构允许连续接收操作。无法写入ICDRR。当产生接收数据完全中断(IICn_RXI)请求时，从ICDRR读取数据一次。

如果ICDRR在从ICDRR读取当前数据之前接收到下一个接收数据（此时ICSR2中的RDRF标志为1），则IIC在下一个RDRF标志设置为1之前自动将SCL时钟保持低1个周期。

36.2.19 I2C Bus Shift Register (ICDRS)



ICDRS is an 8-bit shift register for data transmit and receive. During transmission, transmit data is transferred from ICDRT to ICDRS and is transmitted from the SDAn pin. During reception, data is transferred from ICDRS to ICDRR after 1 byte of data is received. ICDRS cannot be accessed directly.

36.3 Operation

36.3.1 Communication Data Format

The I2C bus format consists of 8-bit data and 1-bit acknowledge. The frame following a start or restart condition is an address frame that specifies a slave device with which the master device communicates. The specified slave is valid until a new slave is specified or a stop condition is issued.

Figure 36.3 shows the I2C bus format, and Figure 36.4 shows the I2C bus timing.

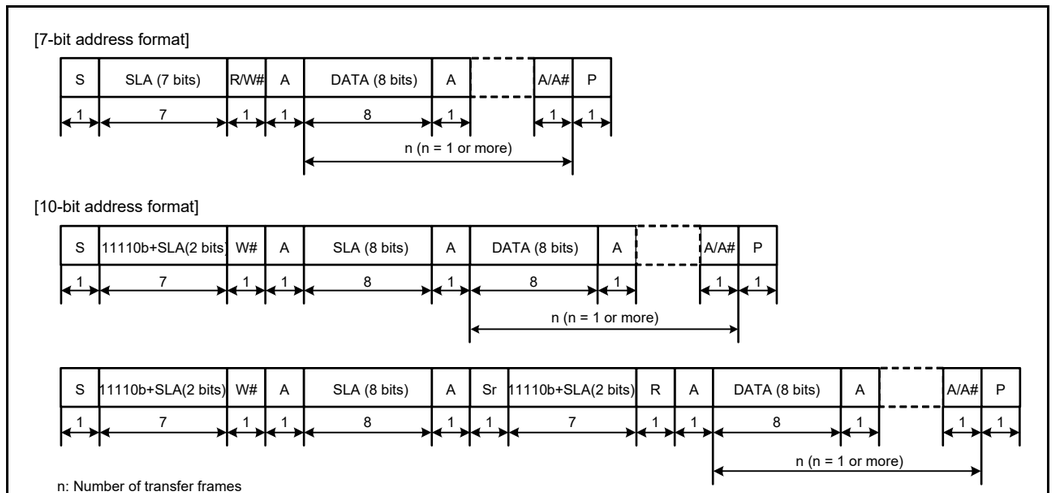


Figure 36.3 I2C bus format

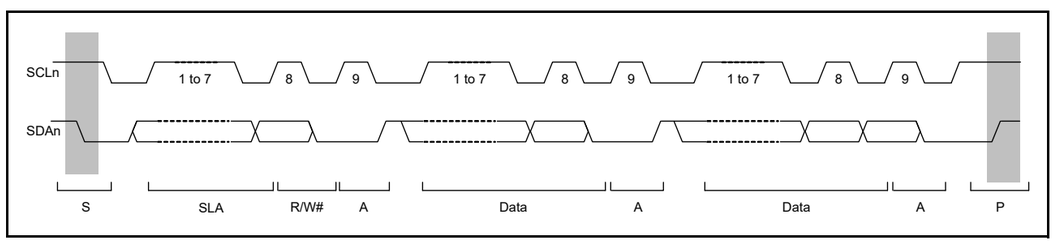
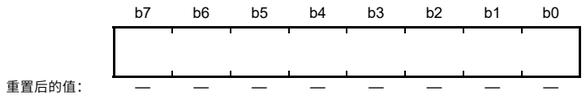


Figure 36.4 I2C bus timing when the SLA setting = 7 bits

S: Start condition. The master device drives the SDAn line low from high while the SCLn line is high.

SLA: Slave address, by which the master device selects a slave device.

36.2.19 I2C总线移位寄存器(ICDRS)



ICDRS是一个用于数据发送和接收的8位移位寄存器。在传输过程中，传输数据从ICDRT到ICDRS并从SDAn引脚传输。在接收过程中，接收到1个字节的数据后，数据从ICDRS传输到ICDRR。ICDRS不能直接访问。

36.3 Operation

36.3.1 通讯数据格式

I2C总线格式由8位数据和1位确认组成。开始或重启条件之后的帧是地址帧，它指定与主设备通信的从设备。指定的从站有效，直到指定新的从站或发出停止条件。

图36.3显示了I2C总线格式，图36.4显示了I2C总线时序。

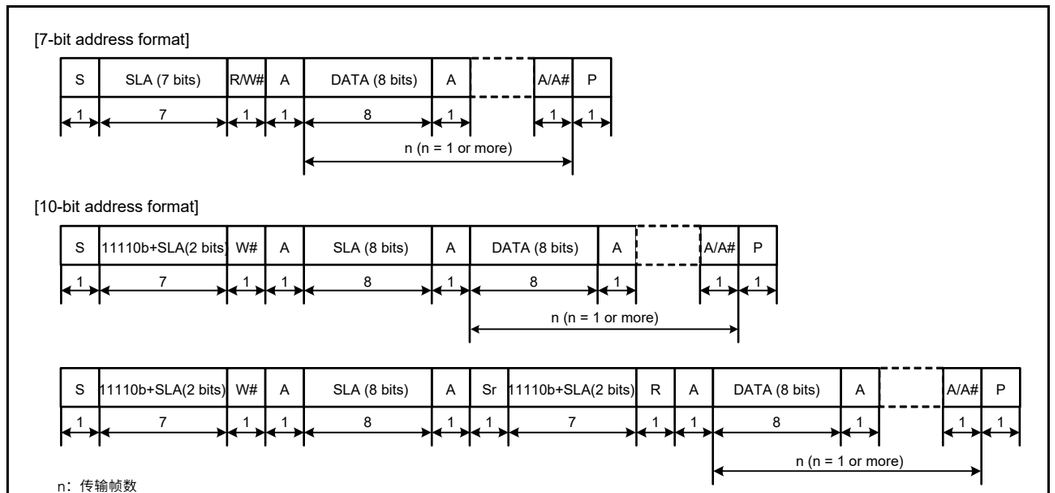


Figure 36.3 I2C总线格式

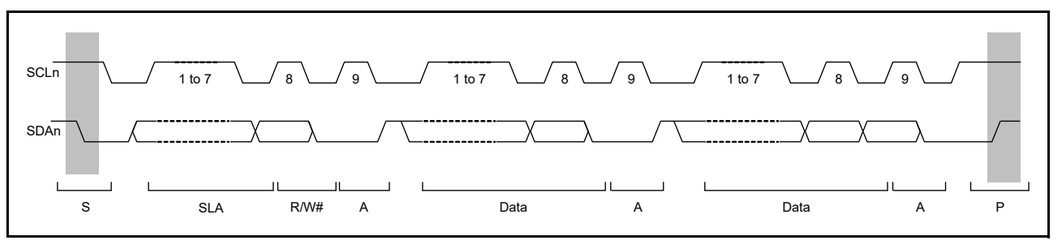


Figure 36.4 SLA设置=7位时的I2C总线时序

S: 启动条件。主设备将SDAn线从高电平驱动为低电平，而SCLn线为高电平。

SLA: 从地址，主设备通过该地址选择从设备。

R/W#: Indicates the direction of data transfer: from the slave device to the master device when R/W# is 1, or from the master device to the slave device when R/W# is 0.

A: Acknowledge. The receive device drives the SDAn line low. In master transmit mode, the slave device returns acknowledge. In master receive mode, the master device returns acknowledge.

A#: Not Acknowledge. The receive device drives the SDAn line high.

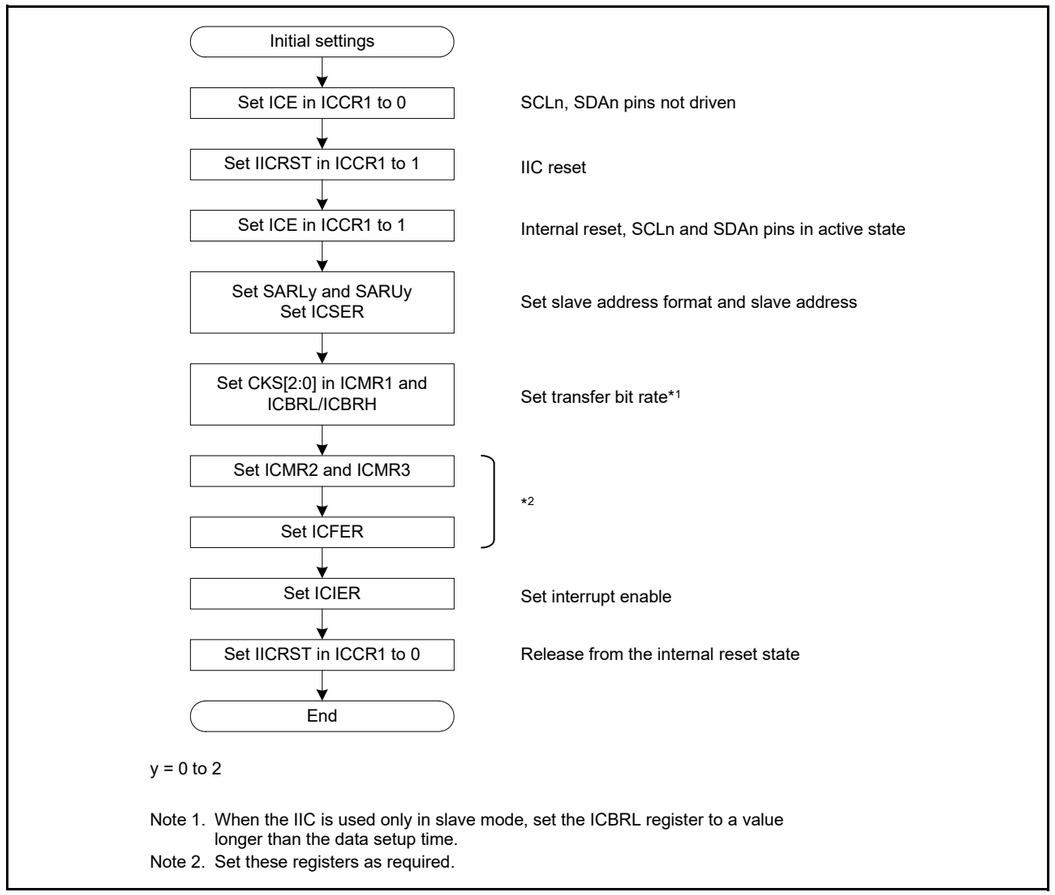
Sr: Restart condition. The master device drives the SDAn line low from the high level after the setup time has elapsed with the SCLn line high.

DATA: Transmitted or received data.

P: Stop condition. The master device drives the SDAn line high from low while the SCLn line is high.

36.3.2 Initial Settings

Before starting data transmission and reception, initialize the IIC using the procedure shown in Figure 36.5. Set the ICCR1.ICE bit to 1 (internal reset) after setting the ICCR1.IICRST bit to 1 (IIC reset) with the ICCR1.ICE bit set to 0 (SCLn and SDAn pins in inactive state). This internal reset procedure initializes the flags and the internal state of the ICSR1 register. Next, set the SARLy, SARUy, ICSER, ICMR1, ICBRH, and ICBRL registers (y = 0 to 2), and set the other registers as required (for the initial IIC settings, see Figure 36.5). When the required register settings are complete, set the ICCR1.IICRST bit to 0, releasing the IIC reset. This step is not necessary if initialization of the IIC is already complete.



Note 1. When the IIC is used only in slave mode, set the ICBRL register to a value longer than the data setup time.
Note 2. Set these registers as required.

Figure 36.5 Example IIC initialization flow

R/W#: 指示数据传输的方向：当RW#为1时从从设备到主设备，或者当RW#为0时从主设备到从设备。

A: 承认。接收设备将SDAn线驱动为低电平。在主发送模式下，从设备返回确认。
在主接收模式下，主设备返回确认。

A#: 不承认。接收设备将SDAn线驱动为高电平。

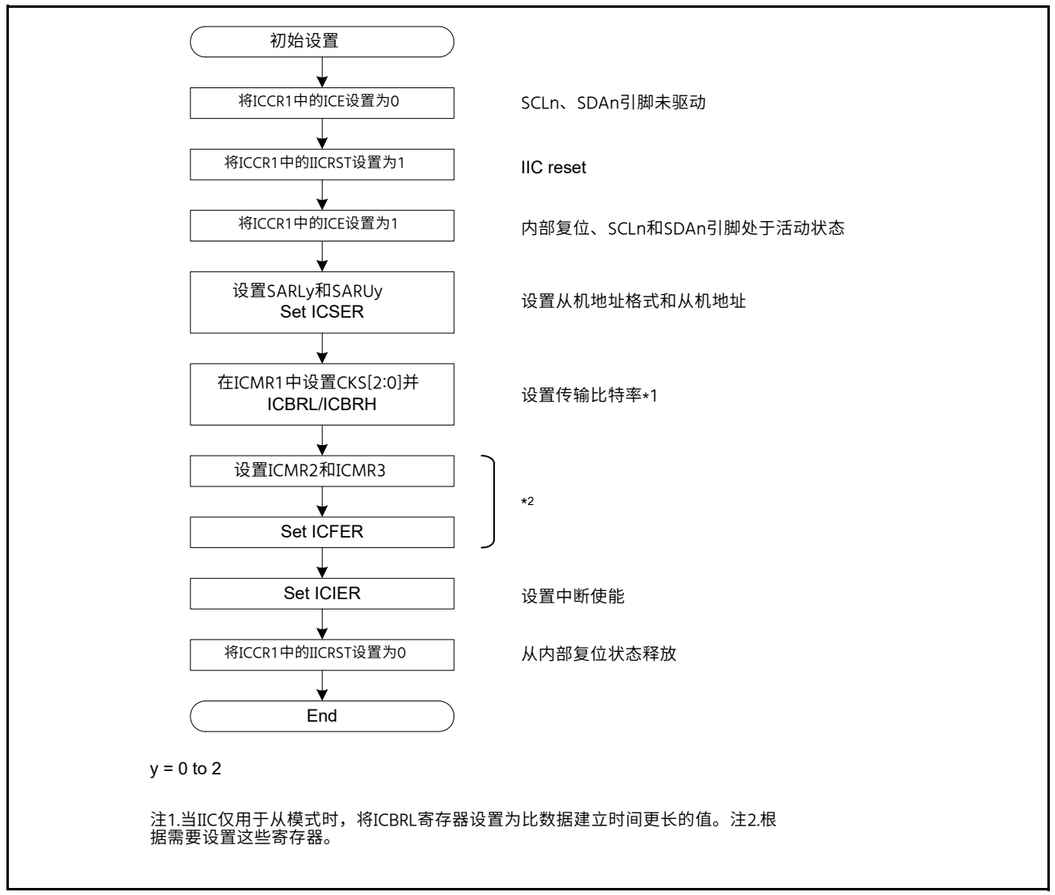
Sr: 重启条件。建立时间过后，主设备将SDAn线从高电平驱动为低电平
SCLn线高。

DATA: 传输或接收的数据。

P: 停止条件。主设备将SDAn线从低电平驱动至高电平，而SCLn线为高电平。

36.3.2 初始设置

在开始数据发送和接收之前，使用图36.5所示的过程初始化IIC。设置
将ICCR1.IICRST位设置为1（IIC复位）且ICCR1.ICE位设置为0（SCLn和SDAn引脚处于非活动状态）后，ICCR1.ICE位为1（内部复位）。此内部复位程序初始化ICSR1寄存器的标志和内部状态。接下来，设置SARLy、SARUy、ICSER、ICMR1、ICBRH和ICBRL寄存器（y=0到2），并根据需要设置其他寄存器（有关初始IIC设置，请参见图36.5）。当所需的寄存器设置完成后，将ICCR1.IICRST位设置为0，释放IIC复位。如果IIC的初始化已经完成，则不需要此步骤。



注1.当IIC仅用于从模式时，将ICBRL寄存器设置为比数据建立时间更长的值。注2.根据需要设置这些寄存器。

Figure 36.5 示例IIC初始化流程

36.3.3 Master Transmit Operation

In master transmit operation, the IIC outputs the SCL clock and transmitted data signals as the master device, and the slave device returns acknowledgments. Figure 36.6 shows an example of master transmission, and Figure 36.7 to Figure 36.9 show the operation timing in master transmission.

To set up and perform master transmission:

1. Process initial settings. For details, see section 36.3.2, Initial Settings.
2. Read the BBSY flag in ICCR2 to check that the bus is free, and then set the ST bit in ICCR2 to 1 (start condition request). On receiving the request, the IIC issues a start condition. At the same time, the BBSY and START flags in ICSR2 automatically set to 1 and the ST bit automatically is set to 0. At this time, if the start condition is detected and the internal levels for the SDA output state and the levels on the SDAn line match while the ST bit is 1, the IIC recognizes that issuance of the start condition as requested by the ST bit is successfully complete, and the MST and TRS bits in ICCR2 automatically set to 1, placing the IIC in master transmit mode. The TDRE flag in ICSR2 also automatically is set to 1 in response to the setting of the TRS bit to 1.
3. Check that the TDRE flag in ICSR2 is 1, and then write the value for transmission (the slave address and the R/W# bit) to ICDRT. When the transmit data is written to ICDRT, the TDRE flag automatically is set to 0, the data is transferred from ICDRT to ICDRS, and the TDRE flag again is set to 1. After the byte containing the slave address and R/W# bit is transmitted, the value of the TRS bit automatically updates to select master transmit or master receive mode based on the value of the transmitted R/W# bit. If the value of the R/W# bit was 0, the IIC continues in master transmit mode.
   Because the ICSR2.NACKF flag being 1 at this time indicates that no slave device recognized the address or there was an error in communications, write 1 to the ICCR2.SP bit to issue a stop condition.
   For data transmission with an address in the 10-bit format, start by writing 1111 0b, the 2 higher-order bits of the slave address, and W to ICDRT as the first address transmission. For the second address transmission, write the 8 lower-order bits of the slave address to ICDRT.
4. Check that the TDRE flag in ICSR2 is 1, and then write the transmit data to the ICDRT register. The IIC automatically holds the SCLn line low until the transmit data is ready or a stop condition is issued.
5. After all bytes of transmit data are written to the ICDRT register, wait until the value in the TEND flag in ICSR2 returns to 1, and then set the SP bit in ICCR2 to 1 (stop condition requested). On receiving a stop condition request, the IIC issues the stop condition. For details on issuing a stop condition, see section 36.11.3, Issuing a Stop Condition.
6. On detecting the stop condition, the IIC automatically sets the MST and TRS bits in ICCR2 to 00b and enters slave receive mode. Additionally, it automatically sets the TDRE and TEND flags to 0, and sets the STOP flag in ICSR2 to 1.
7. Check that the ICSR2.STOP flag is 1, and then set the ICSR2.NACKF and STOP flags to 0 for the next transfer operation.

36.3.3 主发送操作

在主设备发送操作中，IIC作为主设备输出SCL时钟和发送的数据信号，从设备返回确认。图36.6显示了主传输的示例，图36.7至图36.9显示了主传输中的操作时序。

设置和执行主传输：

1. 处理初始设置。有关详细信息，请参阅第36.3.2节，初始设置。
2. 读取ICCR2中的BBSY标志以检查总线是否空闲，然后将ICCR2中的ST位设置为1（启动条件请求）。收到请求后，IIC发出一个开始条件。同时，ICSR2中的BBSY和START标志位自动置1，ST位自动置0。此时，如果检测到启动条件，内部电平为SDA输出状态和当ST位为1时SDAn线匹配，IIC识别出ST位请求的启动条件的发布已成功完成，并且ICCR2中的MST和TRS位自动设置为1，将IIC置于主机发送模式。ICSR2中的TDRE标志也自动设置为1，以响应TRS位设置为1。
3. 检查ICSR2中的TDRE标志是否为1，然后将要发送的值（从机地址和RW#位）写入ICDRT。当发送数据写入ICDRT时，TDRE标志自动设置为0，数据从ICDRT传输到ICDRS，TDRE标志再次设置为1。在发送包含从机地址和RW#位的字节后，TRS位的值会自动更新，以根据发送的RW#位的值选择主机发送或主机接收模式。如果RW#位的值为0，则IIC继续处于主机发送模式。因为此时ICSR2.NACKF标志为1表示没有从设备识别该地址或通信中有错误，所以向ICCR2.SP位写入1以发出停止条件。对于地址为10位格式的数据传输，首先将11110b、从机地址的高2位和W写入ICDRT作为第一个地址传输。对于第二次地址传输，将从地址的低8位写入ICDRT。
4. 检查ICSR2中的TDRE标志是否为1，然后将发送数据写入ICDRT寄存器。IIC自动将SCLn线保持为低电平，直到发送数据准备好或发出停止条件。
5. 将发送数据的所有字节写入ICDRT寄存器后，等待ICSR2中的TEND标志中的值返回1，然后将ICCR2中的SP位设置为1（请求停止条件）。在收到停止条件请求时，IIC发出停止条件。有关发出停止条件的详细信息，请参阅第36.11.3节，发出停止条件。
6. 在检测到停止条件时，IIC自动将ICCR2中的MST和TRS位设置为00b并进入从机接收模式。此外，它自动将TDRE和TEND标志设置为0，并将ICSR2中的STOP标志设置为1。
7. 检查ICSR2.STOP标志是否为1，然后将ICSR2.NACKF和STOP标志设置为0以进行下一次传输操作。

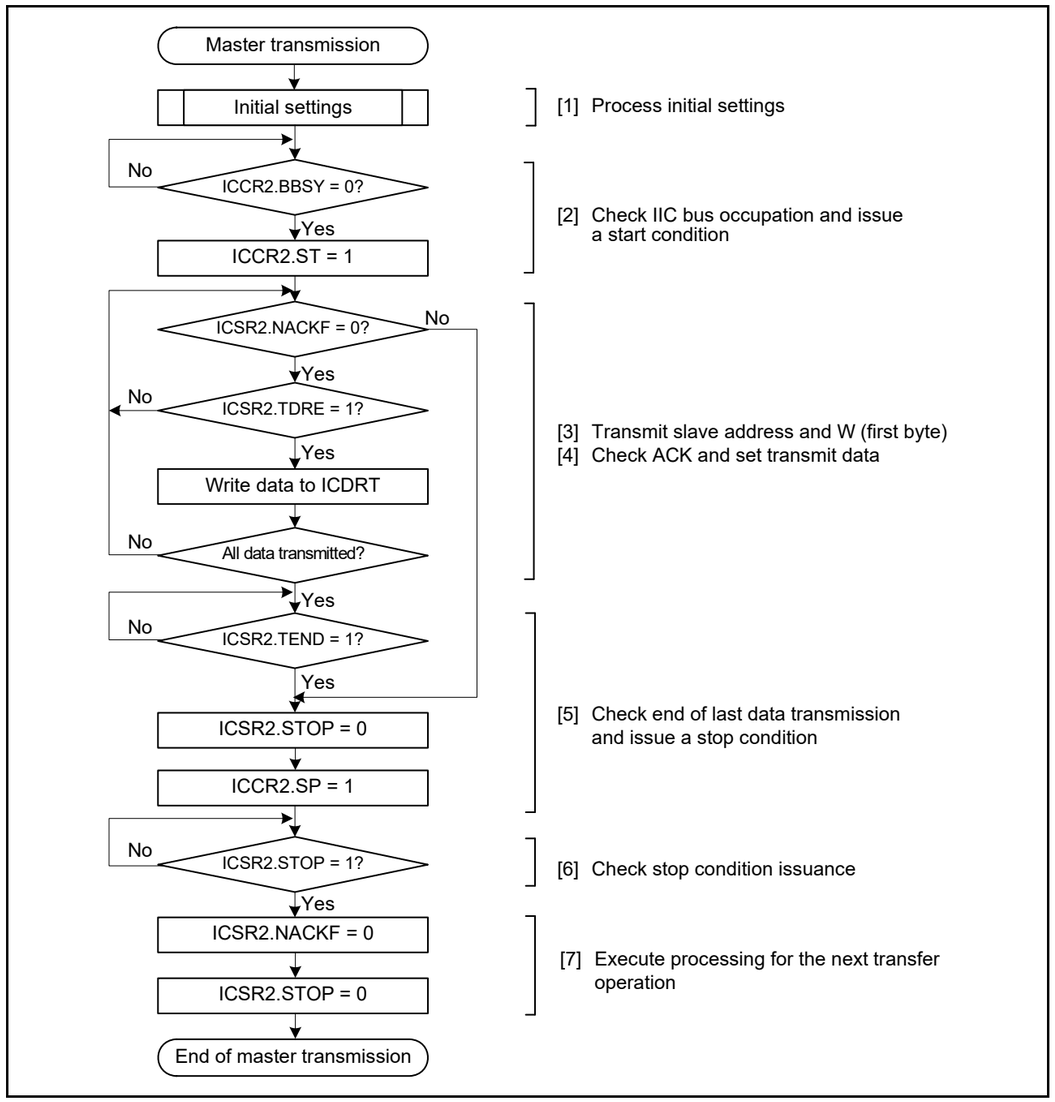


Figure 36.6 Example master transmission flow

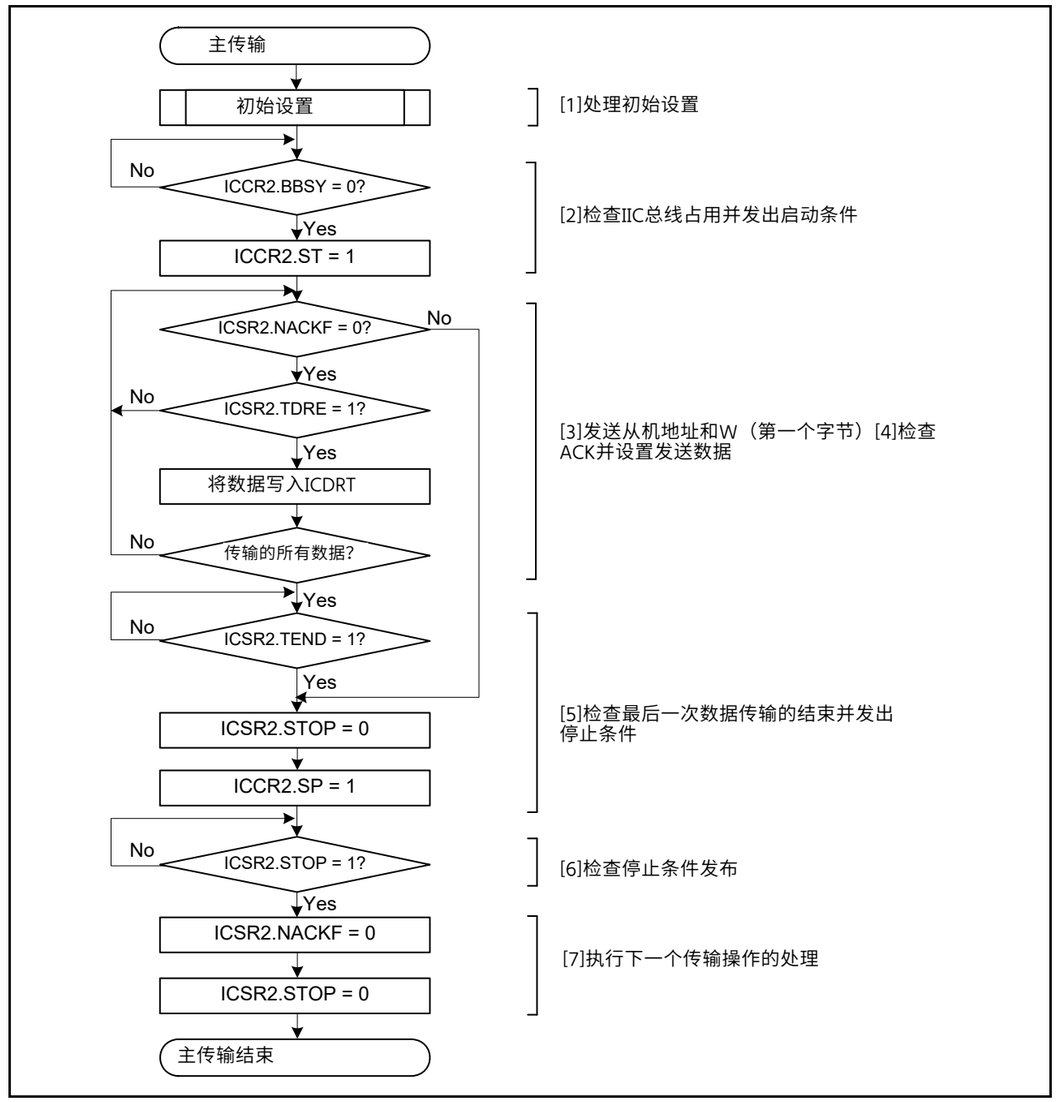


Figure 36.6 示例主传输流程

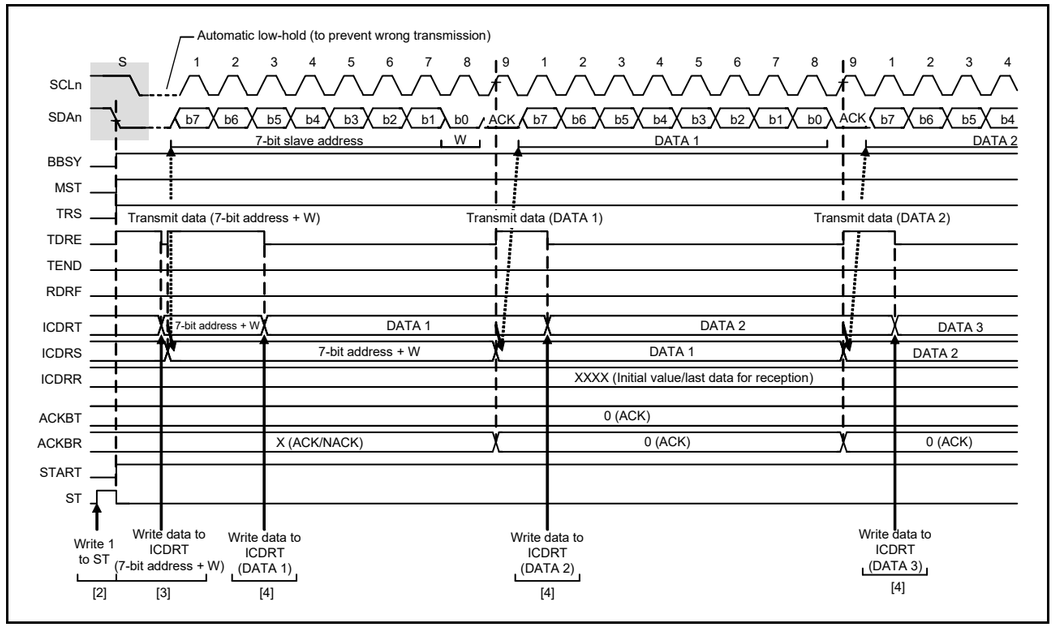


Figure 36.7 Master transmit operation timing (1) with 7-bit address format

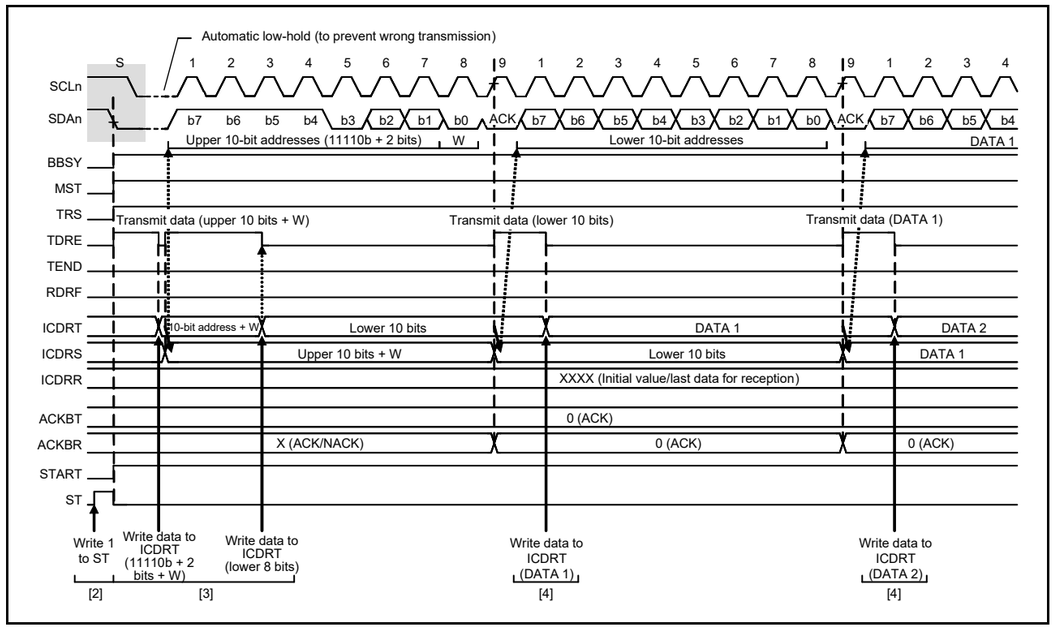


Figure 36.8 Master transmit operation timing (2) with 10-bit address format

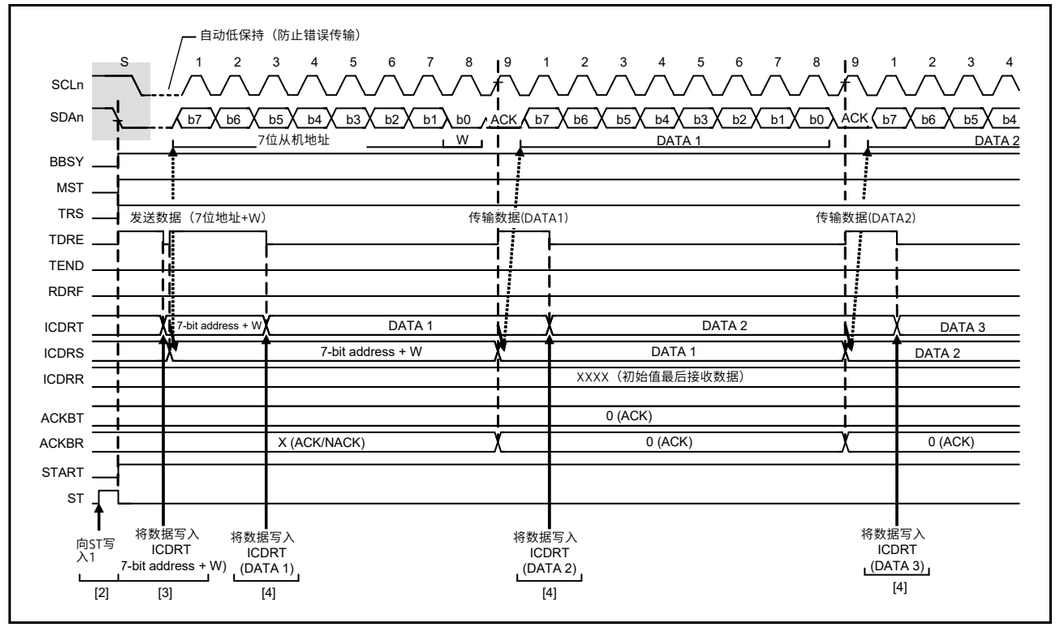


Figure 36.7 7位地址格式的主机发送操作时序(1)

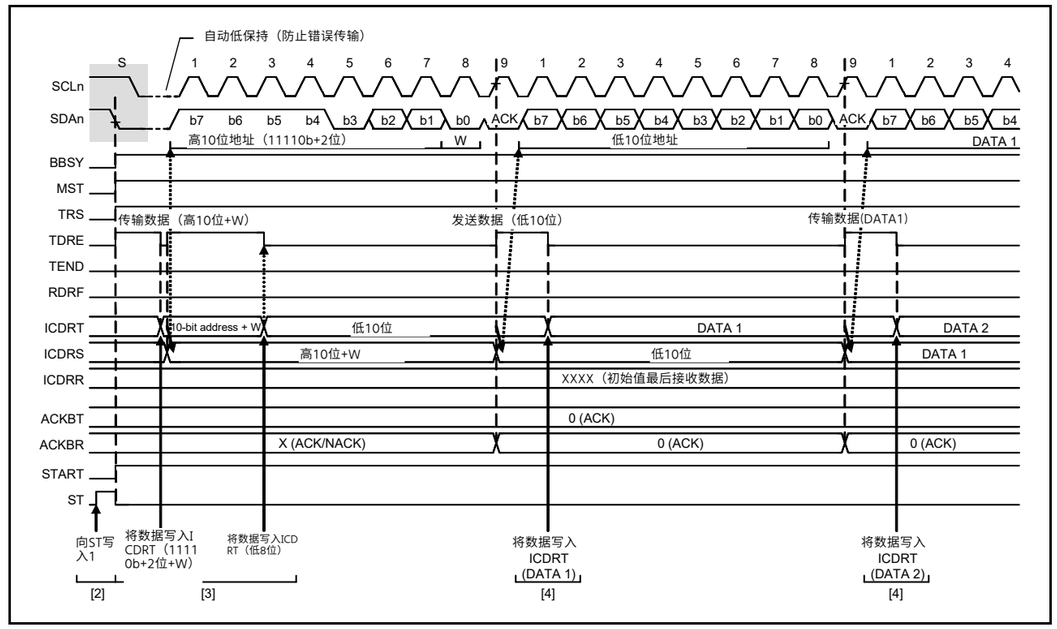


Figure 36.8 10位地址格式的主机发送操作时序(2)

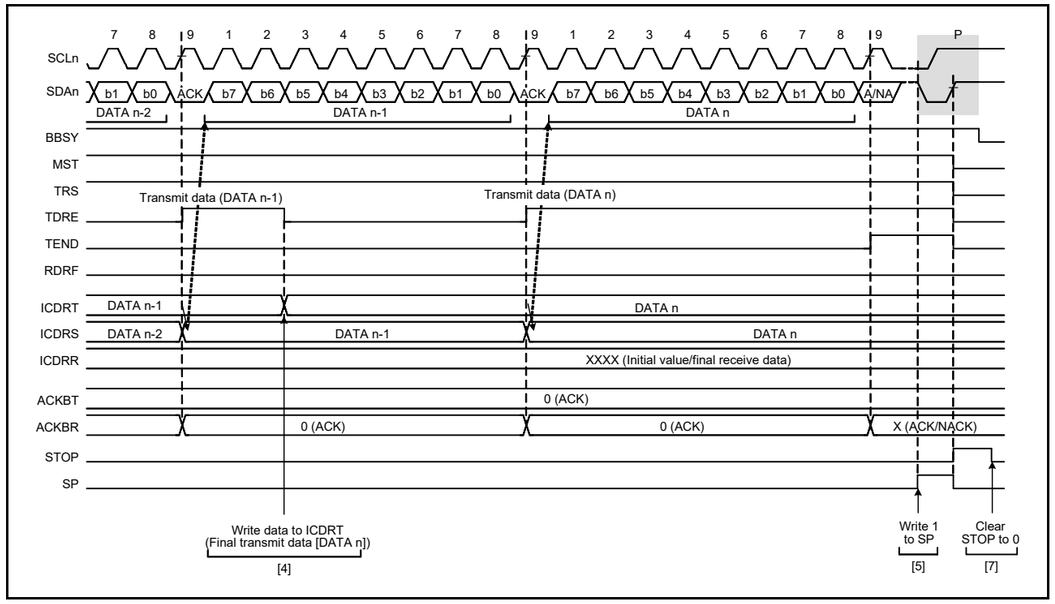


Figure 36.9 Master transmit operation timing (3)

36.3.4 Master Receive Operation

In master receive operation, the IIC as a master device outputs the SCL clock, receives data from the slave device, and returns acknowledgments. Because the IIC must start by sending a slave address to the associated slave device, this part of the procedure is performed in master transmit mode, but the subsequent steps are in master receive mode.

Figure 36.10 and Figure 36.11 show examples of master reception (7-bit address format), and Figure 36.12 to Figure 36.14 show the operation timing in master reception.

To set up and perform master reception:

1. Process initial settings. For details, see section 36.3.2, Initial Settings.
2. Read the BBSY flag in ICCR2 to check that the bus is free, and then set the ST bit in ICCR2 to 1 (start condition request). On receiving the request, the IIC issues a start condition. When the IIC detects the start condition, the BBSY and START flags in ICSR2 automatically set to 1, and the ST bit automatically is set to 0. At this time, if the start condition is detected and the levels for the SDA output and the levels on the SDAn line match while the ST bit is 1, the IIC recognizes that issuance of the start condition as requested by the ST bit is successfully complete, and the MST and TRS bits in ICCR2 automatically set to 1, placing the IIC in master transmit mode. The TDRE flag in ICSR2 also automatically is set to 1 in response to the setting of the TRS bit to 1.
3. Check that the TDRE flag in ICSR2 is 1, and then write the value for transmission (the first byte indicates the slave address and value of the R/W# bit) to ICDRT. When the transmit data is written to ICDRT, the TDRE flag automatically is set to 0, the data is transferred from ICDRT to ICDRS, and the TDRE flag again is set to 1. When the byte containing the slave address and R/W# bit is transmitted, the value of the ICCR2.TRS bit automatically updates to select transmit or receive mode based on the value of the transmitted R/W# bit. If the value of the R/W# bit is 1, the TRS bit is set to 0 on the rising edge of the ninth cycle of the SCL clock, placing the IIC in master receive mode. At this time, the TDRE flag is set to 0 and the ICSR2.RDRF flag automatically is set to 1.
   Because the ICSR2.NACKF flag being 1 at this time indicates that no slave device recognized the address or there was an error in communications, write 1 to the ICCR2.SP bit to issue a stop condition.
   For master reception from a device with a 10-bit address, start by using master transmission to issue the 10-bit address, and then issue a restart condition. After that, transmitting 1111 0b, the two higher-order bits of the slave address, and the R bit places the IIC in master receive mode.
4. Dummy read ICDRR after confirming that the RDRF flag in ICSR2 is 1. This makes the IIC start output of the SCL

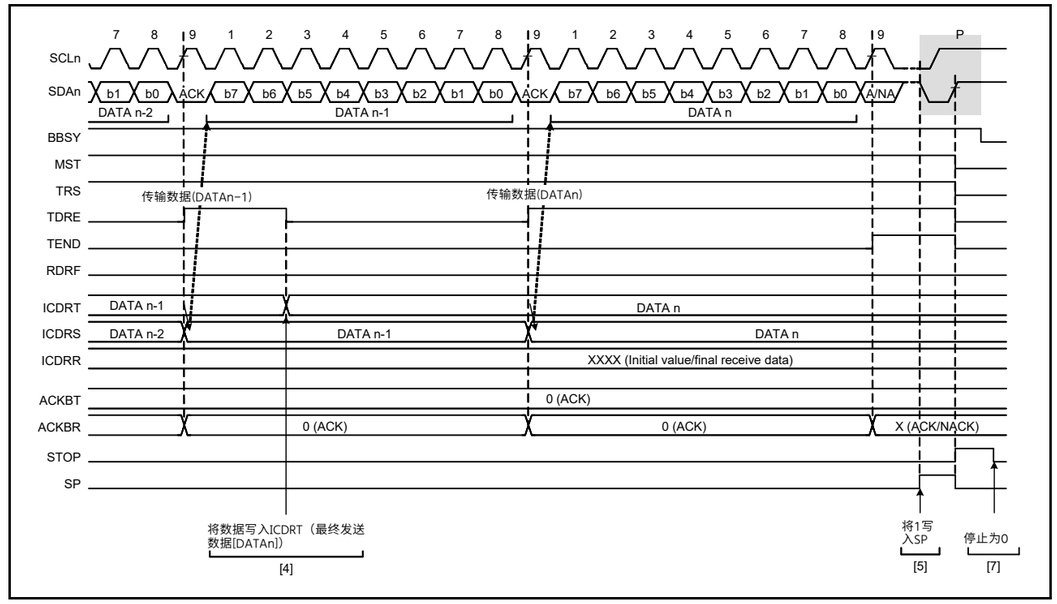


Figure 36.9 主机发送操作时序（3）

36.3.4 主接收操作

在主设备接收操作中，作为主设备的IIC输出SCL时钟，从从设备接收数据，并返回确认。因为IIC必须首先向相关的从设备发送一个从地址，所以这部分程序在主发送模式下执行，但后续步骤在主接收模式下执行。

图36.10和图36.11显示了主机接收示例（7位地址格式），图36.12至图36.14显示了主机接收的操作时序。

设置和执行主接收：

1. 处理初始设置。有关详细信息，请参阅第36.3.2节，初始设置。
2. 读取ICCR2中的BBSY标志以检查总线是否空闲，然后将ICCR2中的ST位设置为1（启动条件请求）。收到请求后，IIC发出一个开始条件。当IIC检测到启动条件时，ICSR2中的BBSY和START标志位自动置1，ST位自动置0。此时，如果检测到启动条件，则SDA输出的电平和电平当ST位为1时SDAn线匹配时，IIC识别出由ST位请求的启动条件的发布已成功完成，并且ICCR2中的MST和TRS位自动设置为1，将IIC置于主机发送模式。ICSR2中的TDRE标志也自动设置为1，以响应TRS位设置为1。
3. 检查ICSR2中的TDRE标志是否为1，然后将要发送的值（第一个字节表示从机地址和RW#位的值）写入ICDRT。当发送数据写入ICDRT时，TDRE标志自动设置为0，数据从ICDRT传输到ICDRS，TDRE标志再次设置为1。当发送包含从机地址和RW#位的字节时，ICCR2.TRS位的值自动更新以根据发送的RW#位的值选择发送或接收模式。如果RW#位的值为1，则在SCL时钟的第9个周期的上升沿将TRS位设置为0，将IIC置于主机接收模式。此时TDRE标志置0，ICSR2.RDRF标志自动置1。因为此时ICSR2.NACKF标志为1表示没有从设备识别该地址或通信出现错误，向ICCR2.SP位写入1以发出停止条件。对于来自具有10位地址的设备的主机接收，首先使用主机发送来发出10位地址，然后发出重启条件。之后，发送11110b、从机地址的两个高位和R位将IIC置于主机接收模式。
4. 确认ICSR2中的RDRF标志为1后虚拟读取ICDRR。这使得SCL的IIC开始输出

clock and start data reception.

5. After 1 byte of data is received, the RDRF flag in ICSR2 is set to 1 on the rising edge of the eighth or ninth cycle of the SCL clock, as selected in the RDRFS bit in ICMR3. Reading ICDRR at this time produces the received data, and the RDRF flag automatically is set to 0 at the same time. Additionally, the value of the acknowledgment field received during the ninth cycle of the SCL clock is returned as the value set in the ICMR3.ACKBT bit. If the next byte to be received is the second-to-last byte, set the ICMR3.WAIT bit to 1, for wait insertion, before reading ICDRR, containing the second-to-last byte. In addition to enabling NACK output, even when interrupts or other operations result in delays in setting the ICMR3.ACKBT bit to 1 (NACK) in step (6), this fixes the SCLn line to the low level on the rising edge of the ninth clock cycle in reception of the last byte, which enables the issuing of a stop condition.
6. When the ICMR3.RDRFS bit is 0, and the slave device must be notified that it is to end transfer for data reception after transfer of the next and final byte, set the ICMR3.ACKBT bit to 1 (NACK).
7. After reading the second-to-last byte from the ICDRR register, if the value of the ICSR2.RDRF flag is 1, write 1 to the SP bit in ICCR2 (stop condition requested), and then read the last byte from ICDRR. When ICDRR is read, the IIC is released from the wait state and issues the stop condition after low-level output in the ninth clock cycle is complete or the SCLn line is released from the low-hold state.
8. On detecting the stop condition, the IIC automatically sets the MST and TRS bits in ICCR2 to 00b and enters slave receive mode. Additionally, detection of the stop condition sets the ICSR2.STOP flag to 1.
9. Check that the ICSR2.STOP flag is 1, and then set the ICSR2.NACKF and STOP flags to 0 for the next transfer operation.

时钟并开始数据接收。

5. 在接收到1个字节的数据后，ICSR2中的RDRF标志在SCL时钟的第8个或第9个周期的上升沿被设置为1，这在ICMR3中的RDRFS位中选择。此时读取ICDRR产生接收数据，同时RDRF标志位自动置0。此外，在SCL时钟的第9个周期内接收到的确认字段的值作为ICMR3.ACKBT位中设置的值返回。如果要接收的下一个字节是倒数第二个字节，则将ICMR3.WAIT位设置为1，等待插入，然后再读取包含倒数第二个字节的ICDRR。除了使能NACK输出外，即使在中断或其他操作导致在步骤(6)中将ICMR3.ACKBT位设置为1(NACK)时出现延迟，这也会在第9次的上升沿将SCLn线固定为低电平接收最后一个字节的时钟周期，它可以发出停止条件。
6. 当ICMR3.RDRFS位为0，并且必须通知从设备在传输下一个和最后一个字节后结束传输以进行数据接收时，将ICMR3.ACKBT位设置为1(NACK)。
7. 从ICDRR寄存器中读取倒数第二个字节后，如果ICSR2.RDRF标志的值为1，则将1写入ICCR2中的SP位（请求停止条件），然后从ICDRR中读取最后一个字节。当读取ICDRR时，IIC从等待状态中释放，并在第9个时钟周期的低电平输出完成或SCLn线从低保持状态释放后发出停止条件。
8. 在检测到停止条件时，IIC自动将ICCR2中的MST和TRS位设置为00b并进入从机接收模式。此外，检测到停止条件会将ICSR2.STOP标志设置为1。
9. 检查ICSR2.STOP标志是否为1，然后将ICSR2.NACKF和STOP标志设置为0以进行下一次传输操作。

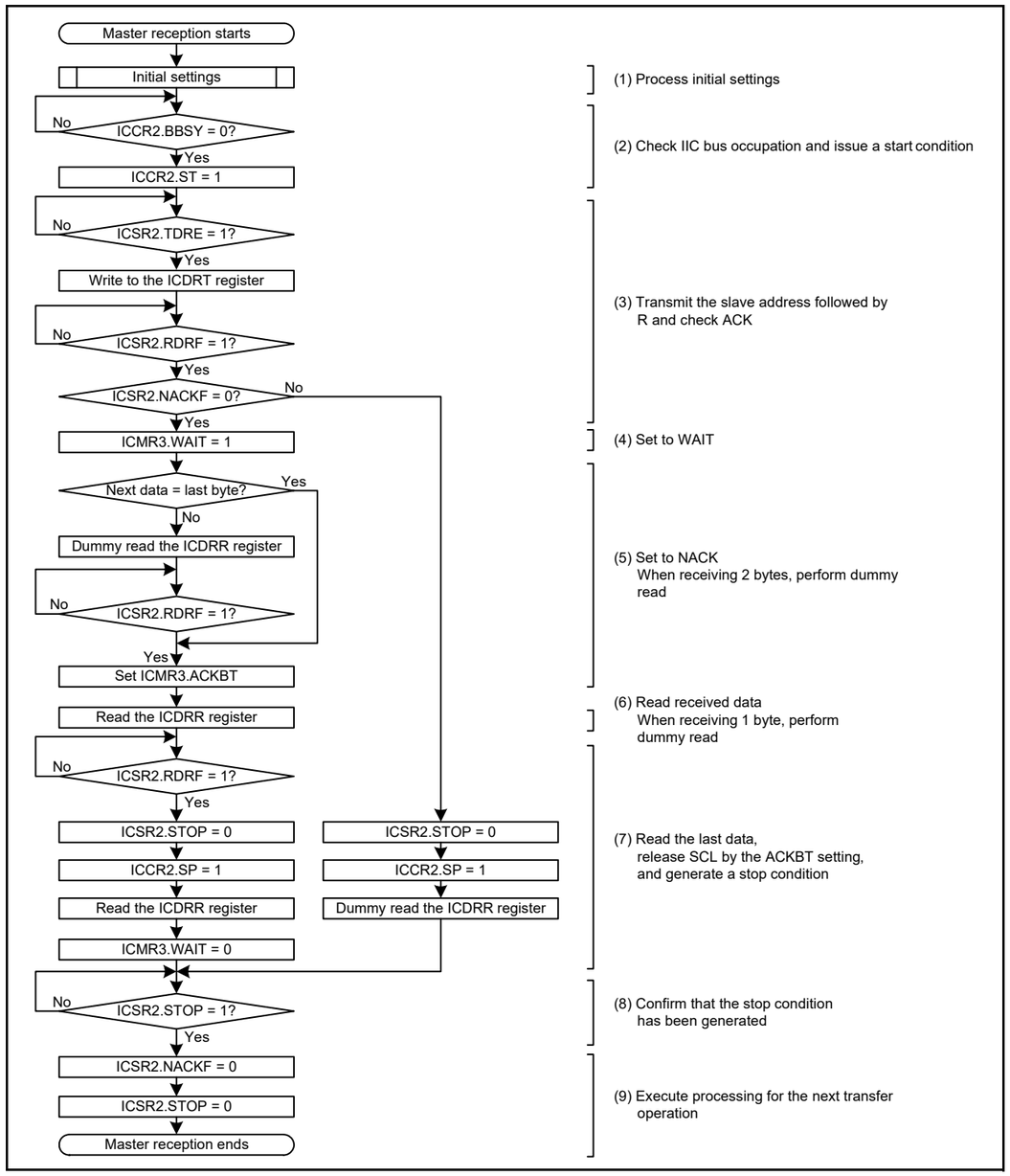


Figure 36.10 Example master reception flow with 7-bit address format and 1 or 2 bytes

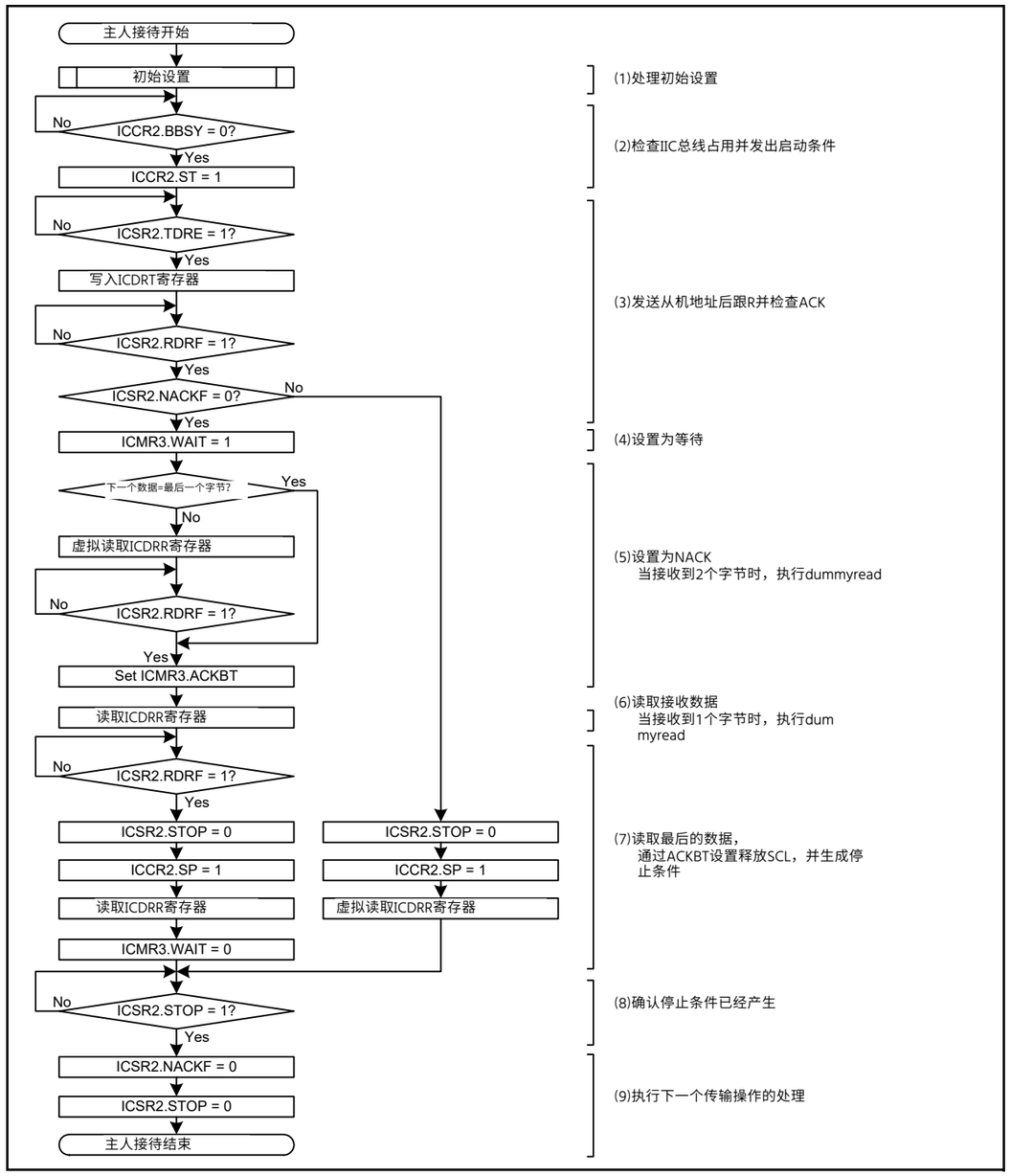


Figure 36.10 具有7位地址格式和1或2个字节的主机接收流程示例

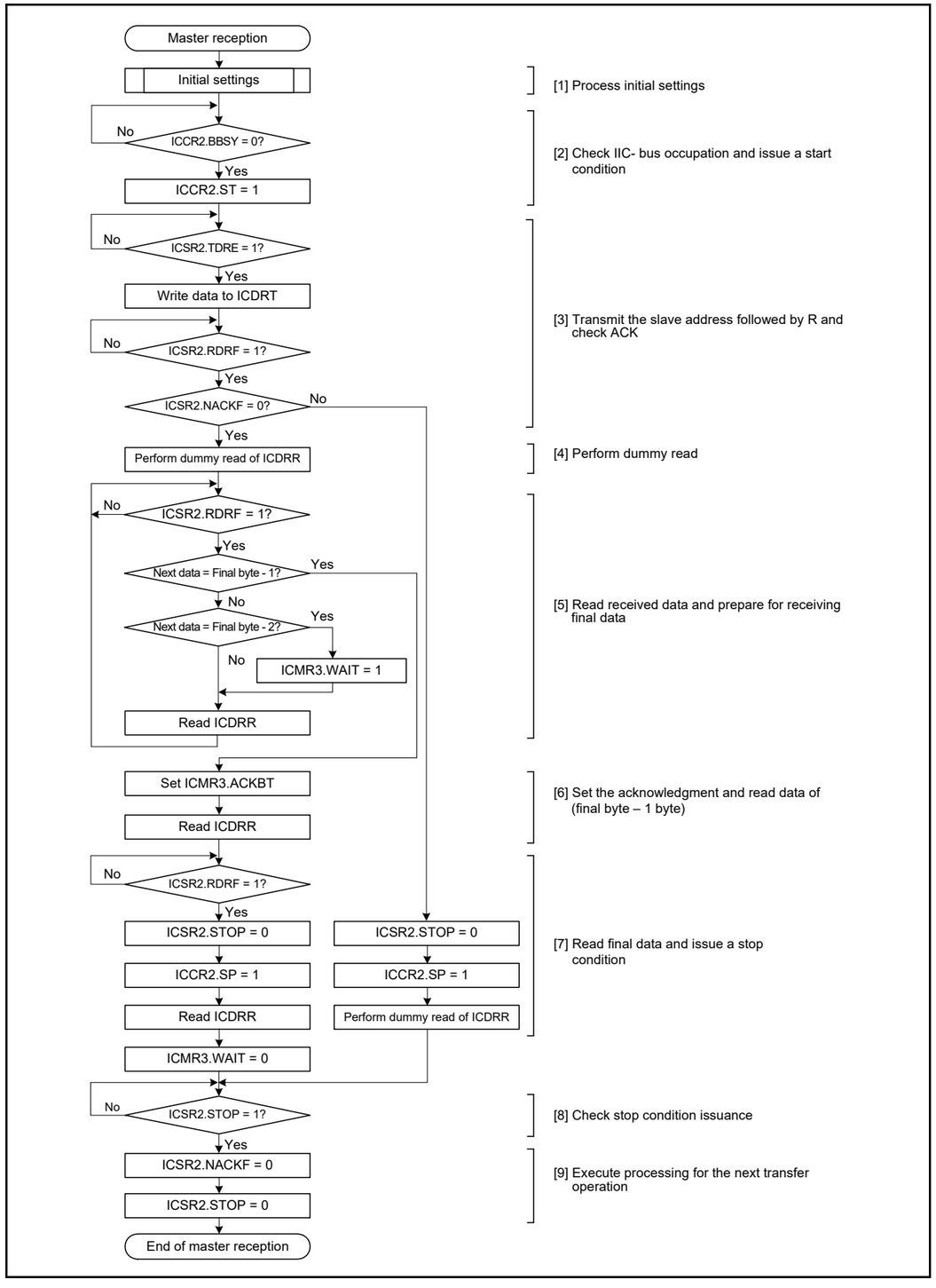


Figure 36.11 Example master reception flow with 7-bit address format and 3 or more bytes

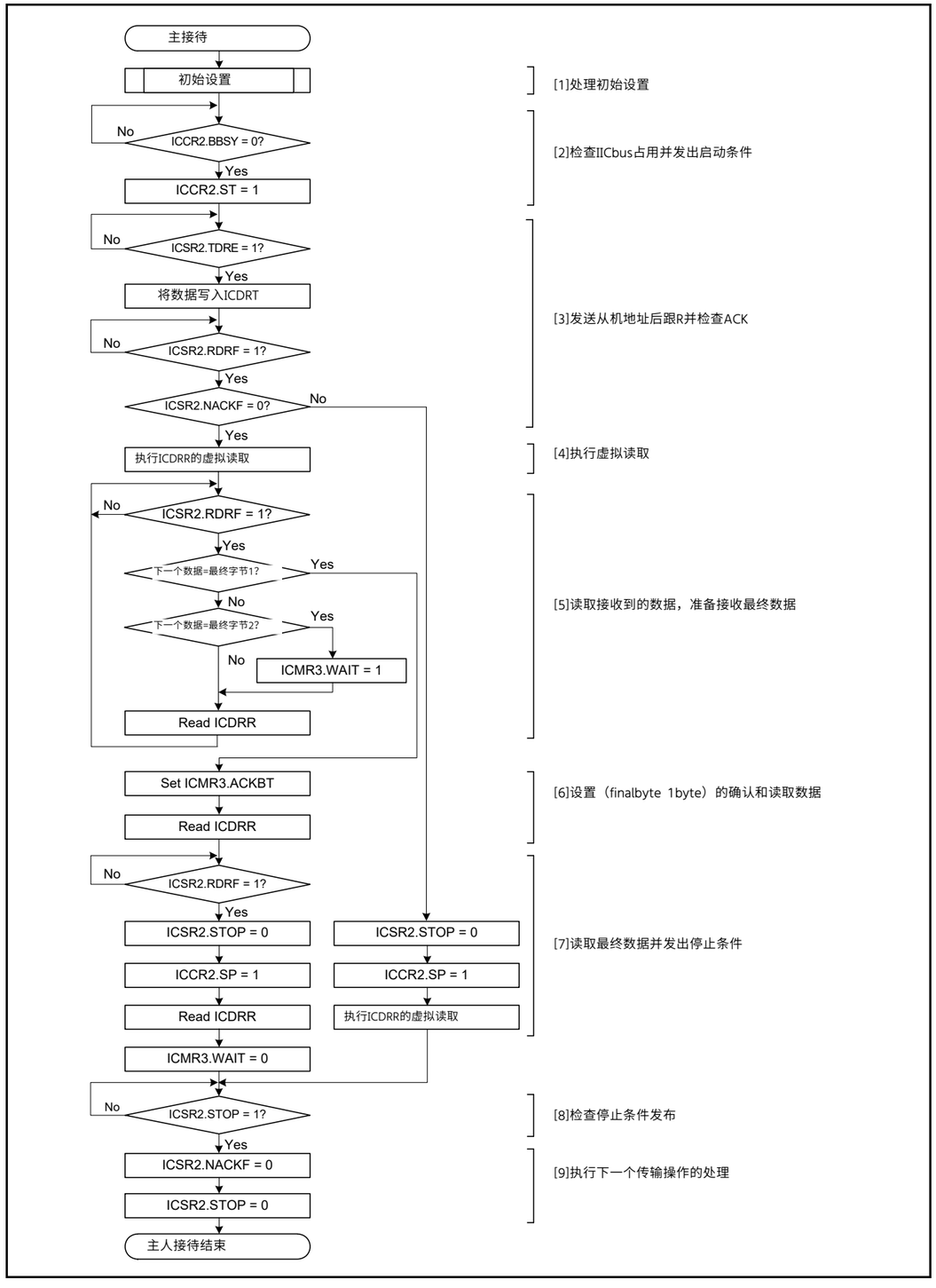


Figure 36.11 具有7位地址格式和3个或更多字节的主接收流示例

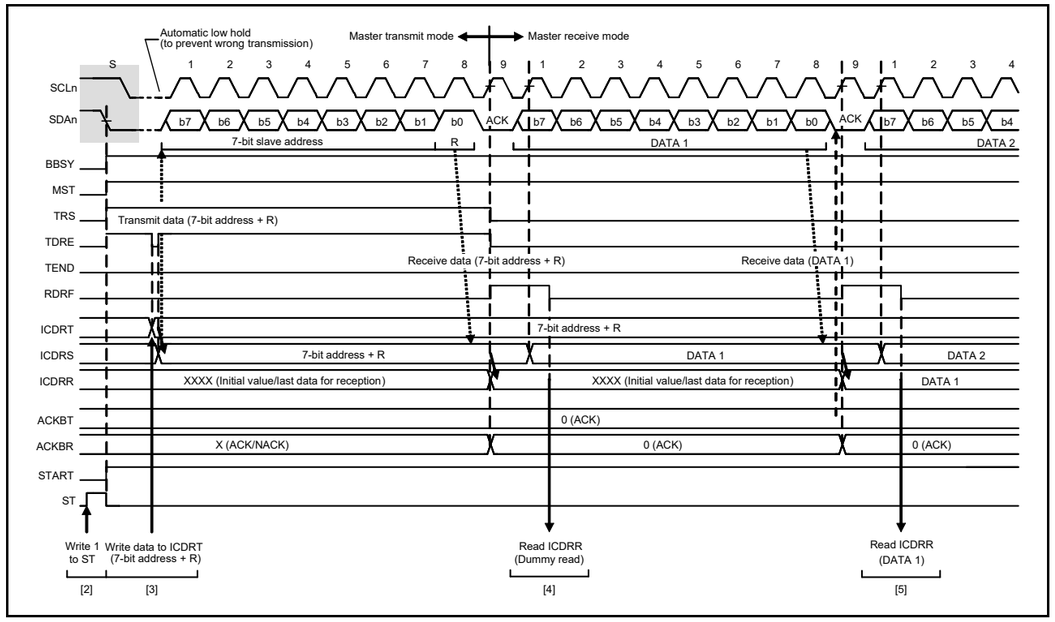


Figure 36.12 Master receive operation timing (1) with 7-bit address format, when RDRFS = 0

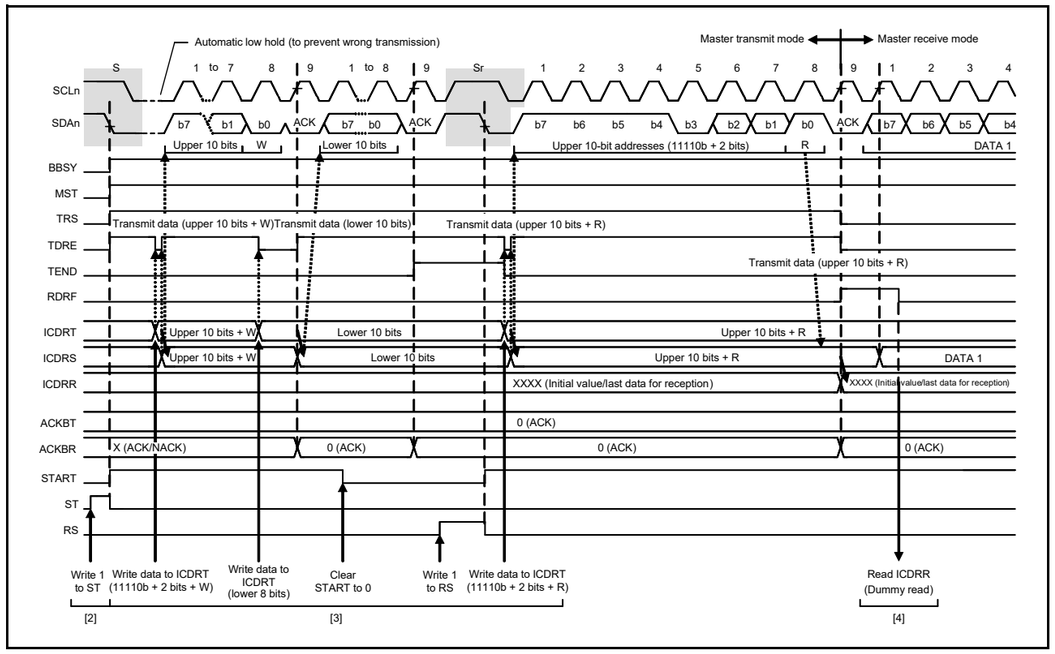


Figure 36.13 Master receive operation timing (2) with 10-bit address format, when RDRFS = 0

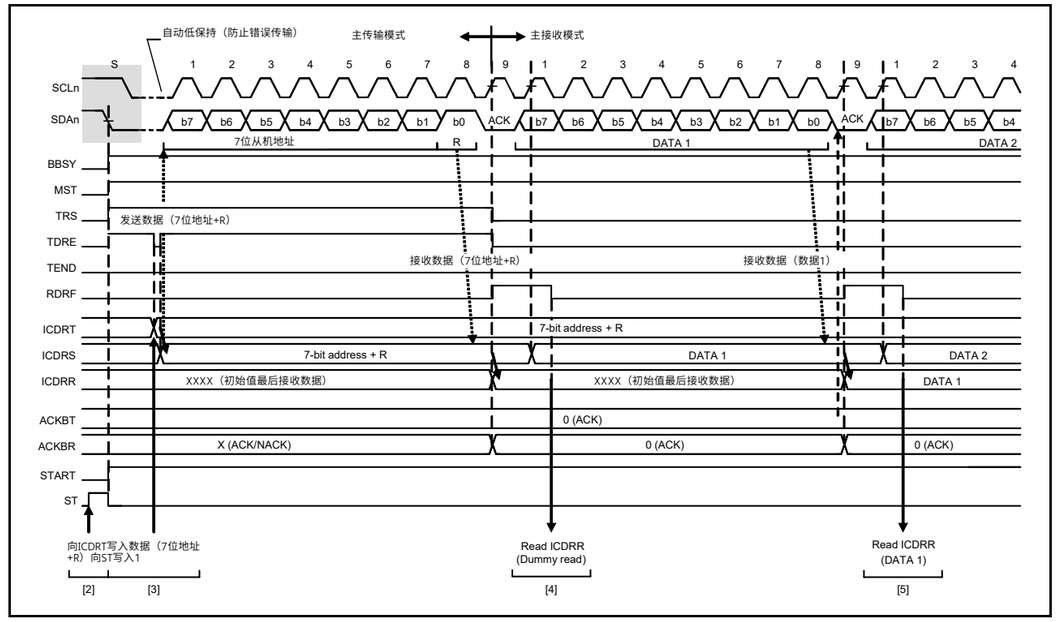


Figure 36.12 当RDRFS=0时，采用7位地址格式的主机接收操作时序(1)

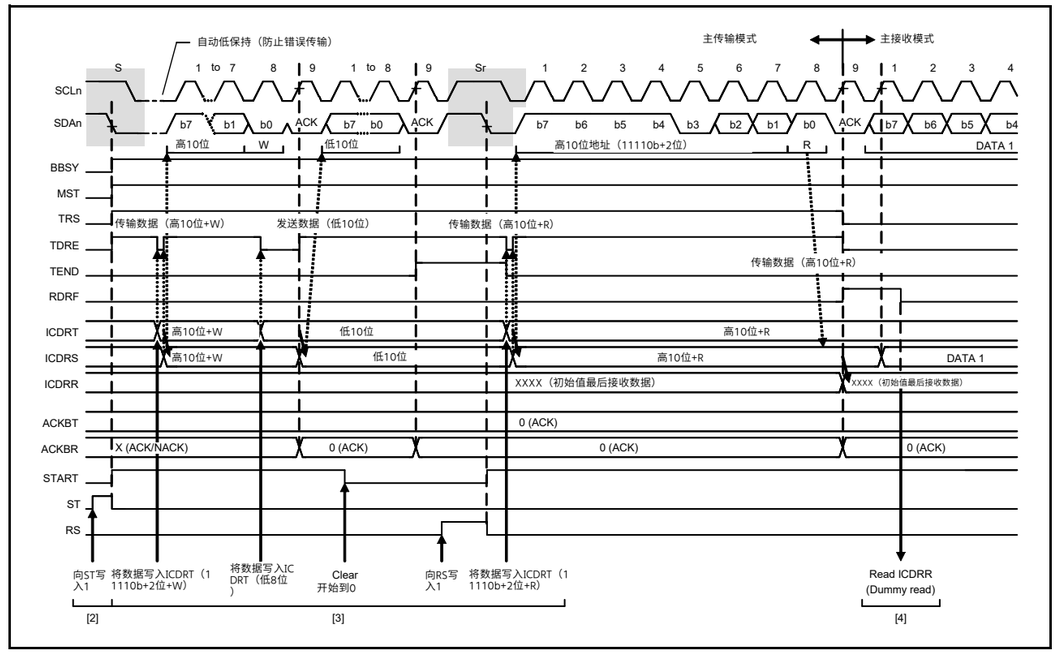


Figure 36.13 10位地址格式的主机接收操作时序（2），当RDRFS=0时

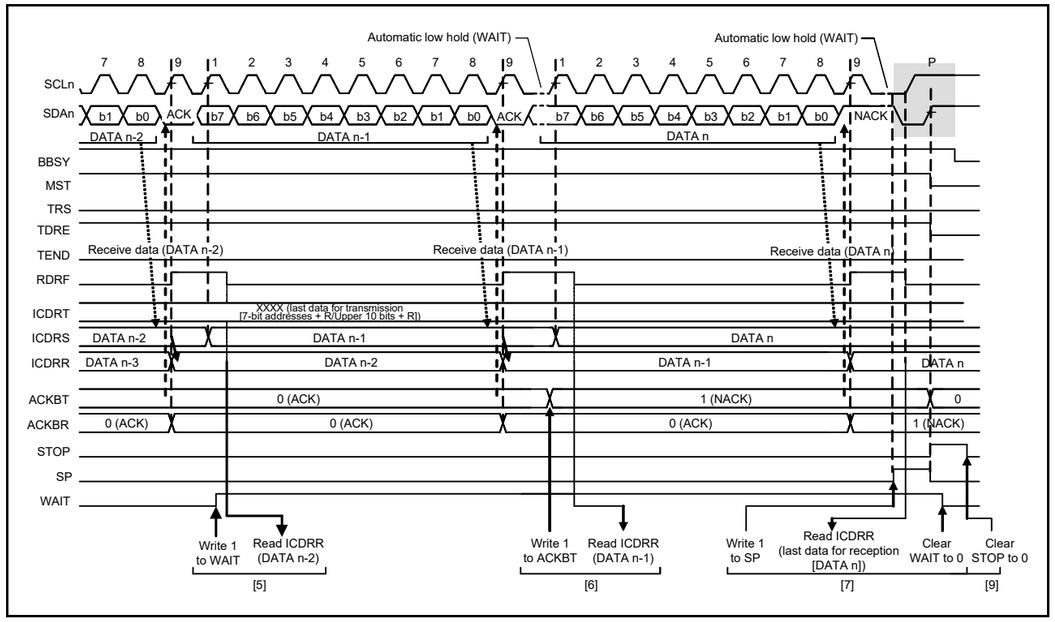


Figure 36.14 Master receive operation timing (3) when RDRFS = 0

36.3.5 Slave Transmit Operation

In slave transmit operation, the master device outputs the SCL clock, the IIC transmits data as a slave device, and the master device returns acknowledgments.

Figure 36.15 shows an example of slave transmission, and Figure 36.16 and Figure 36.17 show the operation timing in slave transmission.

To set up and perform slave transmission:

1. Process initial settings. For details, see section 36.3.2, Initial Settings.
   After the initial settings, the IIC stays in the standby state until it receives a slave address that matches.
2. After receiving a matching slave address, the IIC sets one of the associated ICSR1.HOA, GCA, and AASy flags (y = 0 to 2) to 1 on the rising edge of the ninth cycle of the SCL clock and outputs the value set in the ICMR3.ACKBT bit to the acknowledge bit on the ninth cycle of the SCL clock. If the value of the R/W# bit that was also received at this time is 1, the IIC automatically places itself in slave transmit mode by setting both the ICCR2.TRS bit and the ICSR2.TDRE flag to 1.
3. Check that the ICSR2.TEND flag is 1, and then write the transmit data to the ICDRT register. At this time, if the IIC receives no acknowledge from the master device (receives an NACK signal) while the ICFER.NACKE bit is 1, the IIC suspends transfer of the next data.
4. Wait until the ICSR2.TEND flag is set to 1 while the ICSR2.TDRE flag is 1, after the ICSR2.NACKF flag is set to 1 or the last byte for transmission is written to the ICDRT register. When the ICSR2.NACKF flag or the TEND flag is 1, the IIC drives the SCLn line low on the ninth falling edge of the SCL clock.
5. When the ICSR2.NACKF flag or the ICSR2.TEND flag is 1, dummy read ICDRR to complete the processing. This releases the SCLn line.
6. On detecting the stop condition, the IIC automatically sets the ICSR1.HOA, GCA, and AASy flags (y = 0 to 2), the ICSR2.TDRE and TEND flags, and the ICCR2.TRS bit to 0, and enters slave receive mode.
7. Check that the ICSR2.STOP flag is 1, and then set the ICSR2.NACKF and STOP flags to 0 for the next transfer operation.

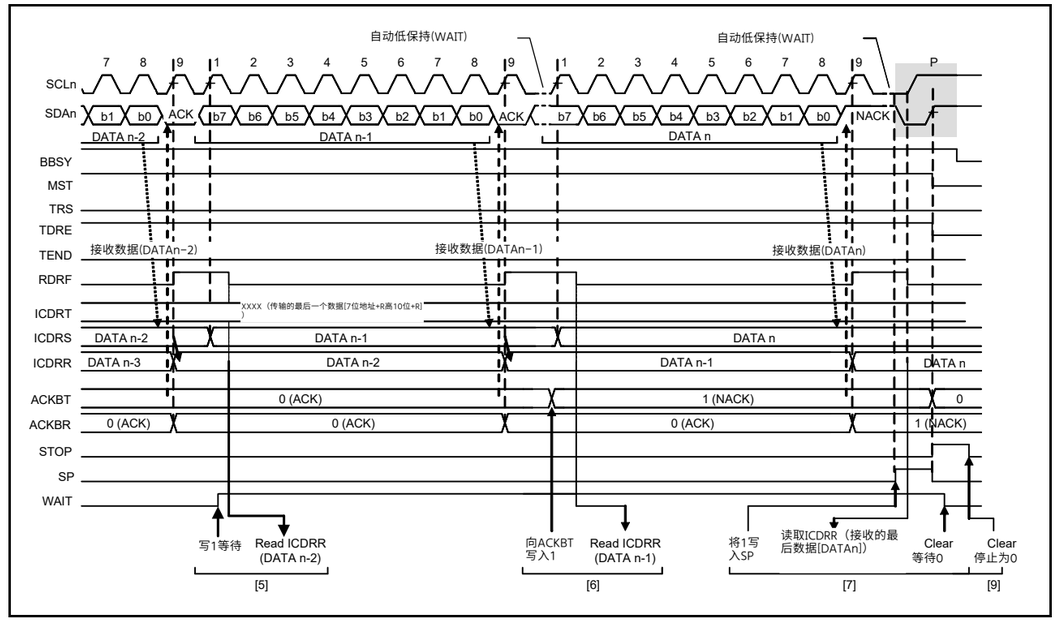


Figure 36.14 RDRFS=0时的主机接收操作时序(3)

36.3.5 从机发送操作

在从发送操作中，主设备输出SCL时钟，IIC作为从设备发送数据，主设备返回确认。

图36.15显示了从机传输的示例，图36.16和图36.17显示了从机传输的操作时序。

设置和执行从属传输：

1. 处理初始设置。有关详细信息，请参阅第36.3.2节，初始设置。
   初始设置后，IIC一直处于待机状态，直到收到匹配的从机地址。
2. 接收到匹配的从地址后，IIC在SCL时钟的第九个周期的上升沿将相关的ICSR1.HOA、GCA和AASy标志之一（y=0到2）设置为1，并输出设置的值在SCL时钟的第9个周期将ICMR3.ACKBT位转换为确认位。如果此时也接收到的RW#位的值为1，则IIC通过将ICCR2.TRS位和ICSR2.TDRE标志都设置为1自动将自身置于从发送模式。
3. 检查ICSR2.TEND标志是否为1，然后将发送数据写入ICDRT寄存器。此时，如果IIC在ICFER.NACKE位为1时没有收到来自主设备的确认（接收到NACK信号），则IIC暂停下一个数据的传输。
4. 等到ICSR2.TEND标志设置为1，而ICSR2.TDRE标志为1，在ICSR2.NACKF标志设置为1或将要发送的最后一个字节写入ICDRT寄存器之后。当ICSR2.NACKF标志或TEND标志为1时，IIC在SCL时钟的第九个下降沿将SCLn线驱动为低电平。
5. 当ICSR2.NACKF标志或ICSR2.TEND标志为1时，假读ICDRR以完成处理。这将释放SCLn线。
6. 在检测到停止条件时，IIC自动设置ICSR1.HOA、GCA和AASy标志（y=0到2），ICSR2.TDRE和TEND标志位，且ICCR2.TRS位为0，进入从机接收模式。
7. 检查ICSR2.STOP标志是否为1，然后将ICSR2.NACKF和STOP标志设置为0以进行下一次传输操作。

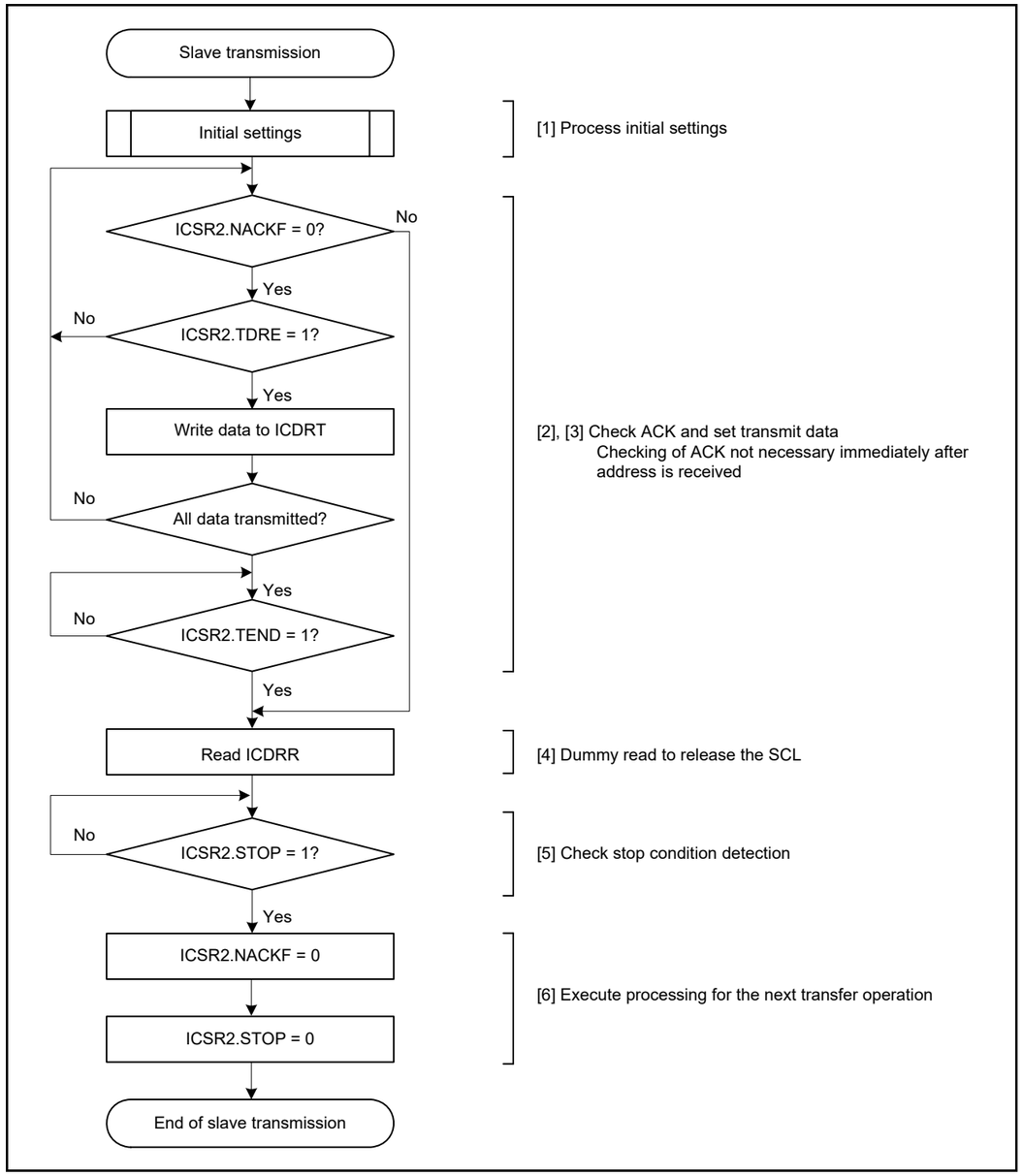


Figure 36.15 Example slave transmission flow

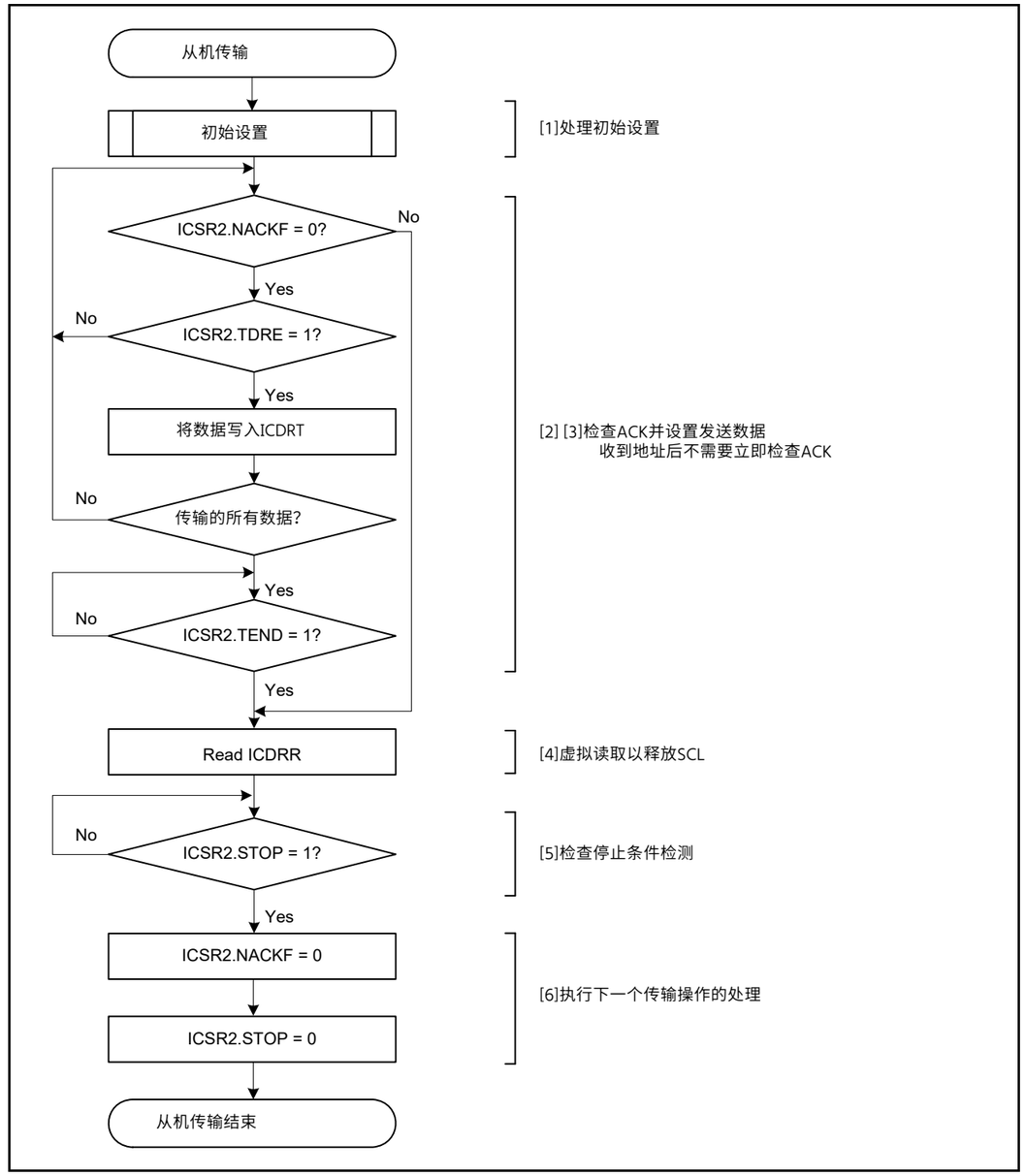


Figure 36.15 从机传输流程示例

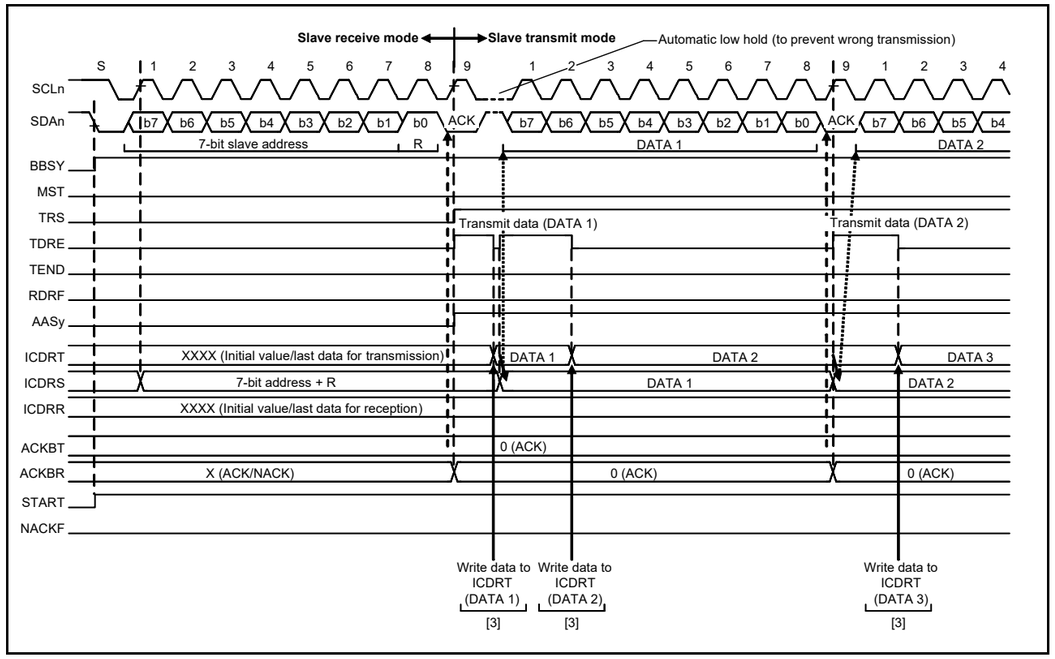


Figure 36.16 Slave transmit operation timing (1) with 7-bit address format

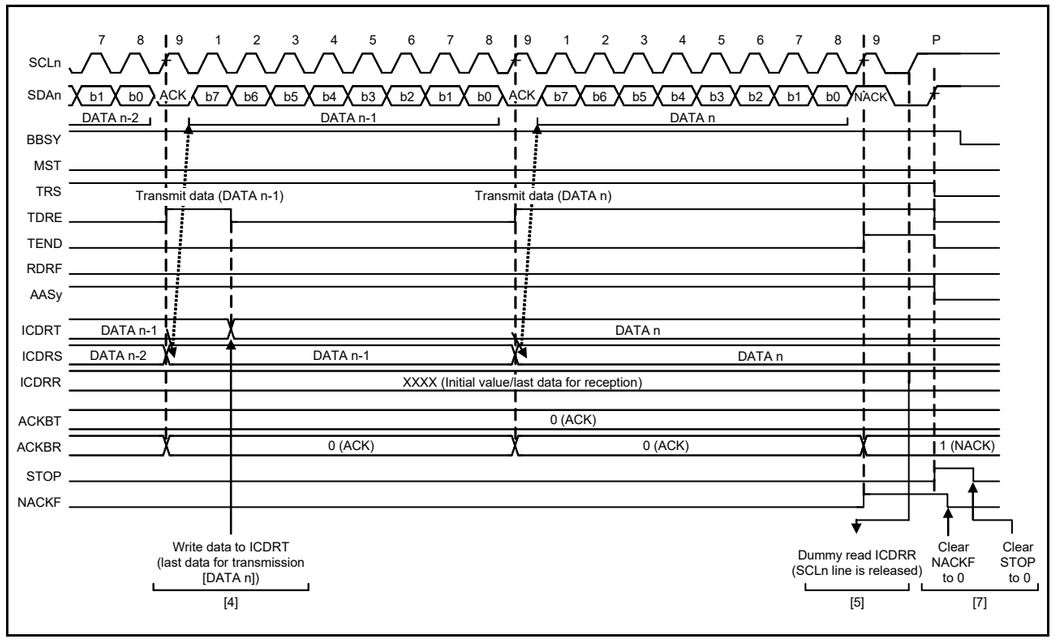


Figure 36.17 Slave transmit operation timing (2)

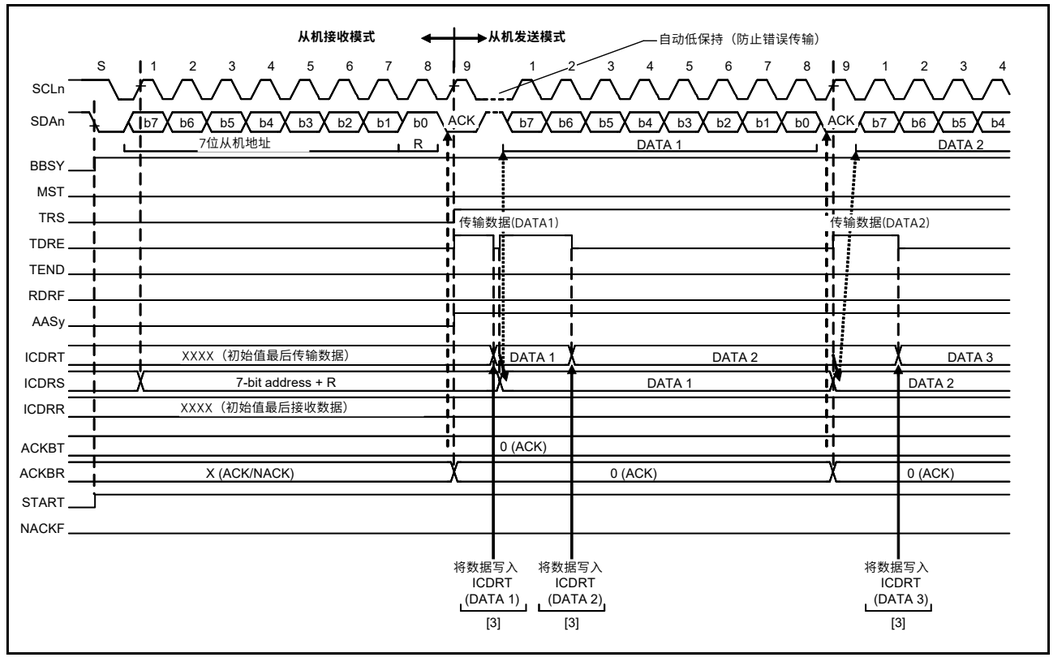


Figure 36.16 7位地址格式的从机发送操作时序(1)

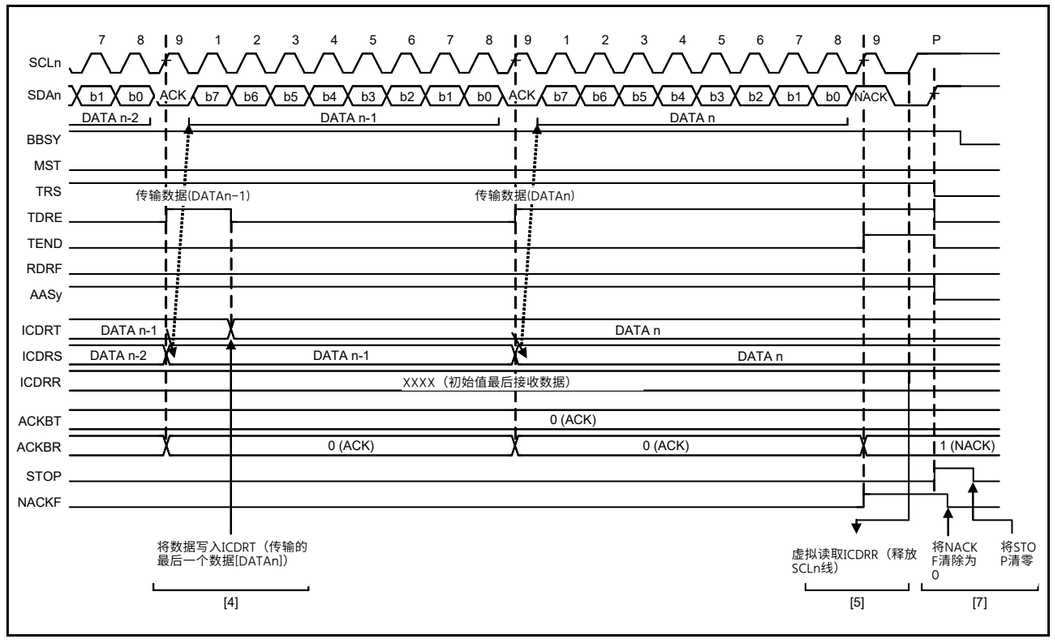


Figure 36.17 从机发送操作时序（2）

36.3.6 Slave Receive Operation

In slave receive operation, the master device outputs the SCL clock and transmit data, and the IIC returns acknowledgments as a slave device.

Figure 36.18 shows an example of slave reception, and Figure 36.19 and Figure 36.20 show the operation timing in slave reception.

To set up and perform slave reception:

1. Process initial settings. For details, see section 36.3.2, Initial Settings.
   After the initial settings, the IIC stays in the standby state until it receives a slave address that matches.
2. After receiving a matching slave address, the IIC sets one of the associated ICSR1.HOA, GCA, and AASy flags (y = 0 to 2) to 1 on the rising edge of the ninth cycle of the SCL clock and outputs the value set in the ICMR3.ACKBT bit to the acknowledge bit on the ninth cycle of the SCL clock. If the value of the R/W# bit that was also received at this time is 0, the IIC continues to place itself in slave receive mode and sets the RDRF flag in ICSR2 to 1.
3. Check that the ICSR2.STOP flag is 0 and the ICSR2.RDRF flag is 1, and then dummy read ICDRR. The dummy value consists of the slave address and R/W# bit when the 7-bit address format is selected, or the lower 8 bits when the 10-bit address format is selected.
4. When ICDRR is read, the IIC automatically sets the ICSR2.RDRF flag to 0. If reading of ICDRR is delayed and a next byte is received while the RDRF flag is still set to 1, the IIC holds the SCLn line low until one SCL cycle before the point where RDRF must be set. In this case, reading ICDRR releases the SCLn line from being held at the low level.
   When the ICSR2.STOP flag is 1 and the ICSR2.RDRF flag is also 1, read ICDRR until all the data is completely received.
5. On detecting the stop condition, the IIC automatically clears the ICSR1.HOA, GCA, and AASy flags (y = 0 to 2) to 0.
6. Check that the ICSR2.STOP flag is 1, and then set the ICSR2.STOP flag to 0 for the next transfer operation.

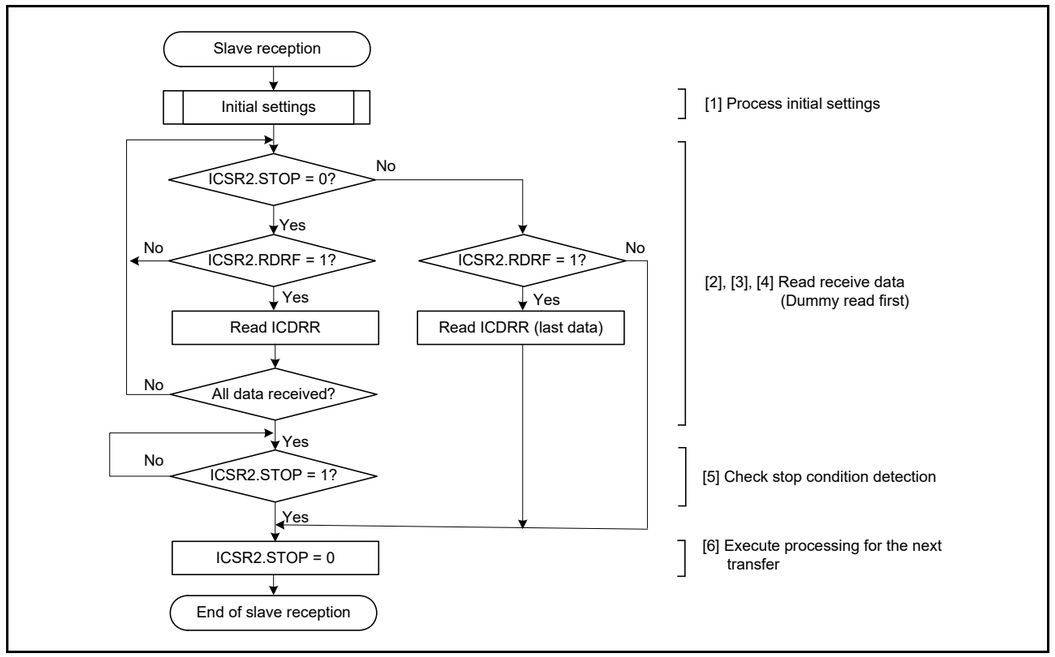


Figure 36.18 Example slave reception flow

36.3.6 从机接收操作

在从机接收操作中，主设备输出SCL时钟并发送数据，IIC作为从设备返回确认。

图36.18显示了从机接收的示例，图36.19和图36.20显示了从机接收的操作时序。

设置和执行从属接收：

1. 处理初始设置。有关详细信息，请参阅第36.3.2节，初始设置。
   初始设置后，IIC一直处于待机状态，直到收到匹配的从机地址。
2. 接收到匹配的从地址后，IIC在SCL时钟的第九个周期的上升沿将相关的ICSR1.HOA、GCA和AASy标志之一（y=0到2）设置为1，并输出设置的值在SCL时钟的第9个周期将ICMR3.ACKBT位转换为确认位。如果此时也接收到的RW#位的值为0，则IIC继续将自身置于从接收模式并将ICSR2中的RDRF标志设置为1。
3. 检查ICSR2.STOP标志是否为0，ICSR2.RDRF标志是否为1，然后虚拟读取ICDRR。Thedummyvalueconsistsoftheslaveaddressand RW#bitwhenthe7-bitaddressformatisselected orthelower8bitswhenthe10-bitaddressformatisselected.
4. 当读取ICDRR时，IIC自动将ICSR2.RDRF标志设置为0。如果ICDRR的读取延迟并且在RDRF标志仍设置为1时接收到下一个字节，则IIC将SCLn线保持为低电平，直到一个SCL周期在必须设置RDRF之前。在这种情况下，读取ICDRR会解除SCLn线保持在低电平的状态。当ICSR2.STOP标志为1且ICSR2.RDRF标志也为1时，读取ICDRR直到完全接收到所有数据。
5. 在检测到停止条件时，IIC自动将ICSR1.HOA、GCA和AASy标志（y=0到2）清除为0。
6. 检查ICSR2.STOP标志是否为1，然后将ICSR2.STOP标志设置为0以进行下一次传输操作。

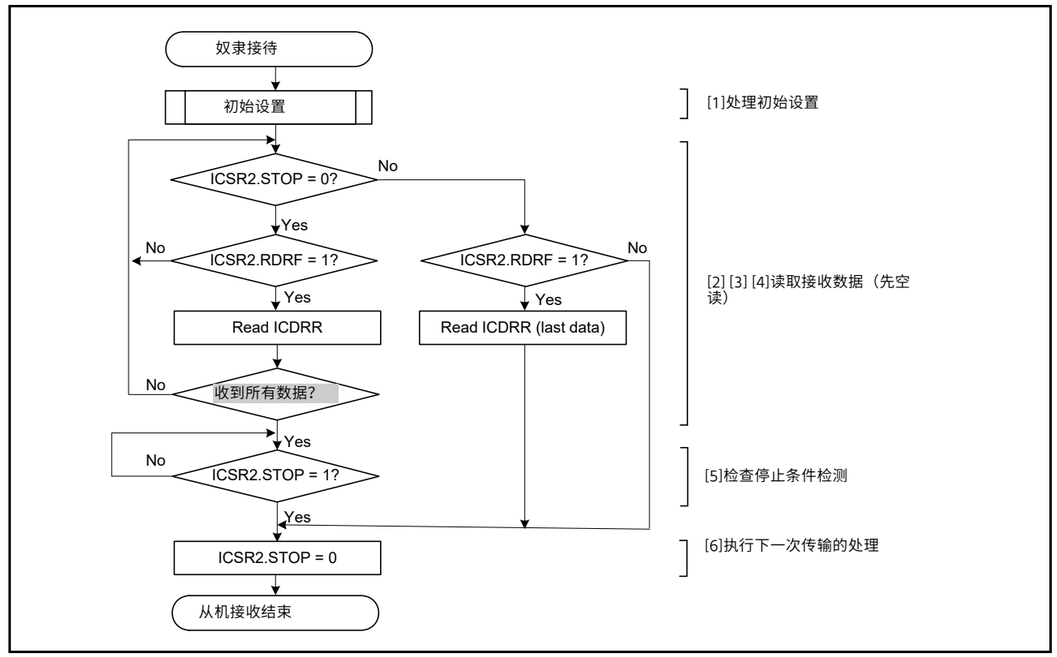


Figure 36.18 从机接收流程示例

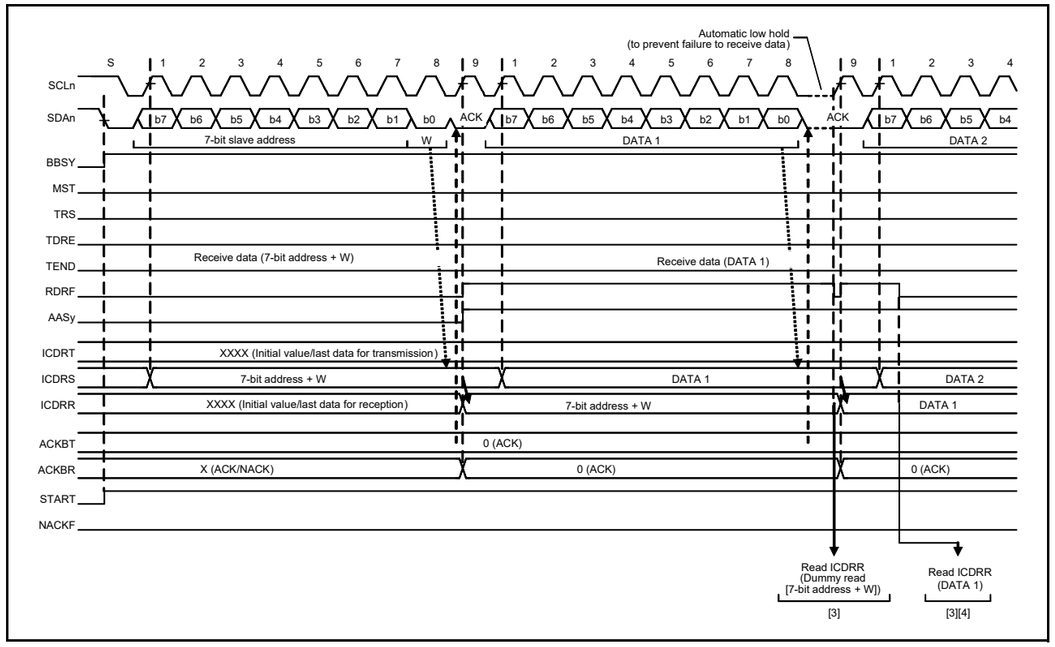


Figure 36.19 Slave receive operation timing (1) with 7-bit address format, when RDRFS = 0

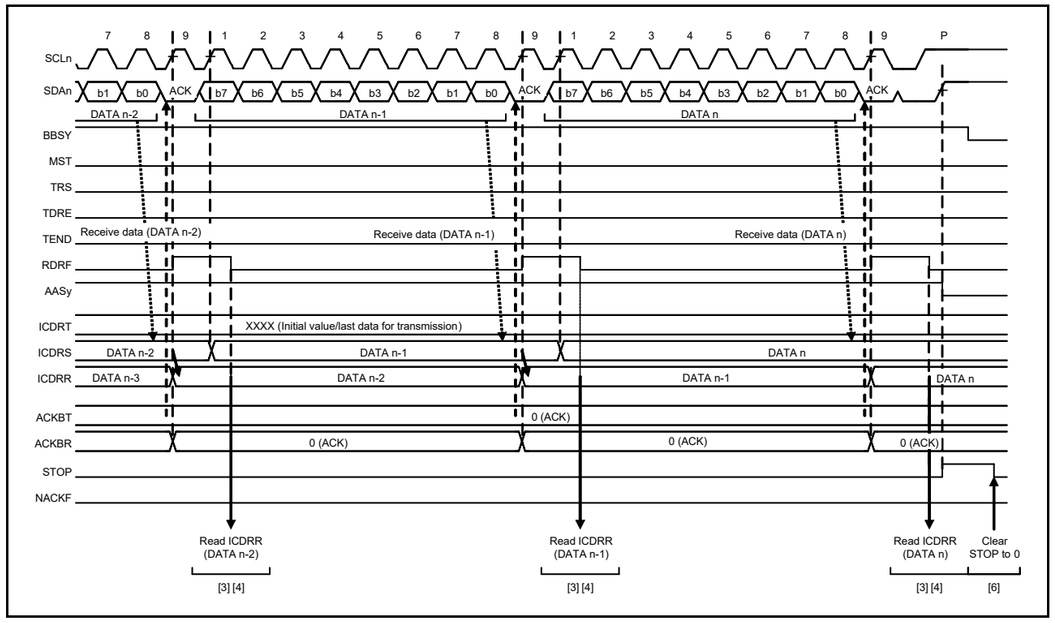


Figure 36.20 Slave receive operation timing (2) when RDRFS = 0

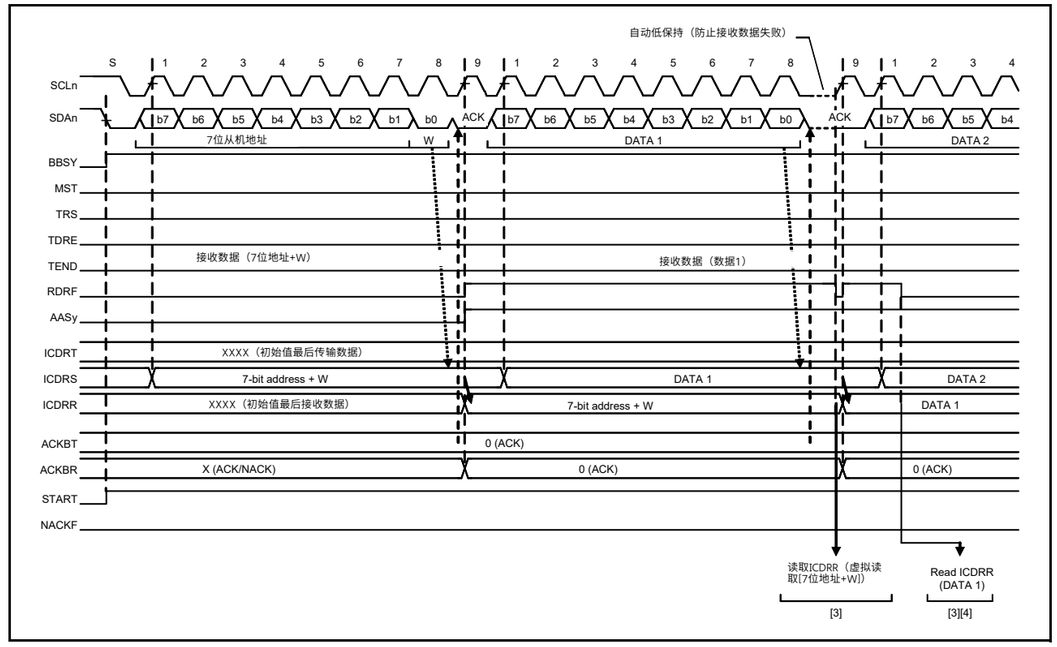


Figure 36.19 当RDRFS=0时，7位地址格式的从机接收操作时序(1)

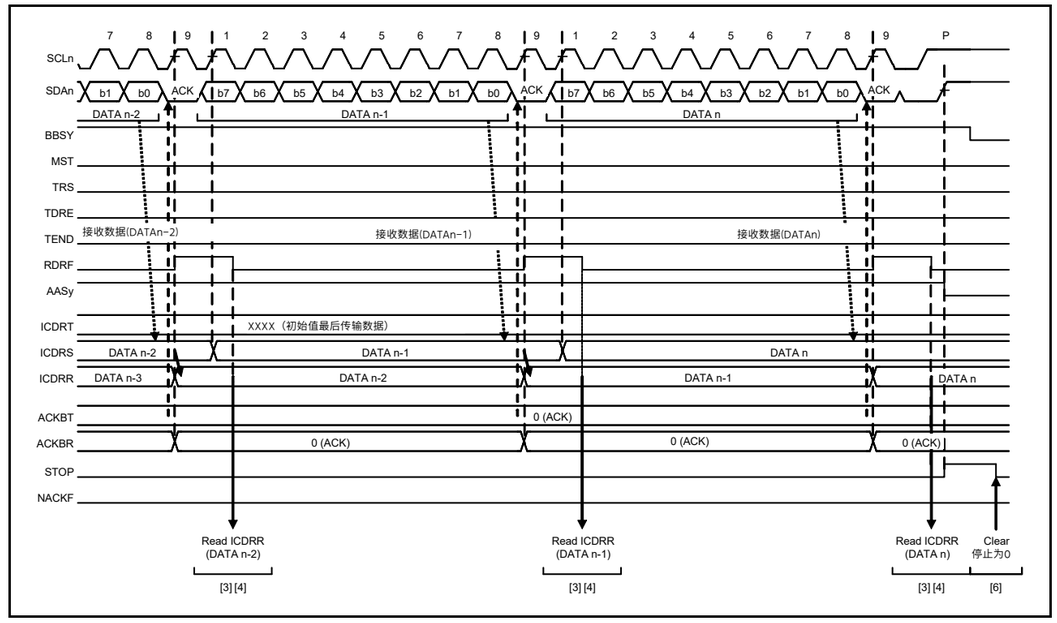


Figure 36.20 RDRFS=0时的从机接收操作时序(2)

36.4 SCL Synchronization Circuit

For generation of the SCL clock, the IIC starts counting the value for the high-level period specified in ICBRH when it detects a rising edge on the SCLn line, and it drives the SCLn line low when it completes counting. When the IIC detects the falling edge of the SCLn line, it starts counting the value for the low-level period specified in ICBRL, and then it stops driving the SCLn line, releasing the line, when it completes counting. The IIC repeats this process to generate the SCL clock.

If multiple master devices are connected to the I2C bus, a collision of SCL signals might arise because of contention with another master device. In such cases, the master devices must synchronize their SCL signals. Because this synchronization of SCL signals must be bit by bit, the IIC is equipped with an SCL synchronization circuit to obtain bit-by-bit synchronization of the SCL clock signals by monitoring the SCLn line while in master mode.

When the IIC detects a rising edge on the SCLn line and so starts counting out the high-level period specified in ICBRH, and the level on the SCLn line falls because an SCL signal is being generated by another master device, the IIC stops counting when it detects the falling edge, drives the level on the SCLn line low, and starts counting the low-level period specified in ICBRL. When the IIC finishes counting the low-level period, it stops driving the SCLn line low to release the line. At this time, if the low-level period of the SCL clock signal from the other master device is longer than the low-level period set in the IIC, the low-level period of the SCL signal is extended. When the low-level period for the other master device has ended, the SCL signal rises because the SCLn line was released. When the IIC finishes outputting the low-level period of the SCL clock, the SCLn line is released and the SCL clock rises. That is, when SCL signals from more than one master are contending, the high-level period of the SCL signal is synchronized with that of the clock with the narrower period, and the low-level period of the SCL signal is synchronized with that of the clock with the broader period. This synchronization of the SCL signal is only enabled when the SCLE bit in ICFER is set to 1.

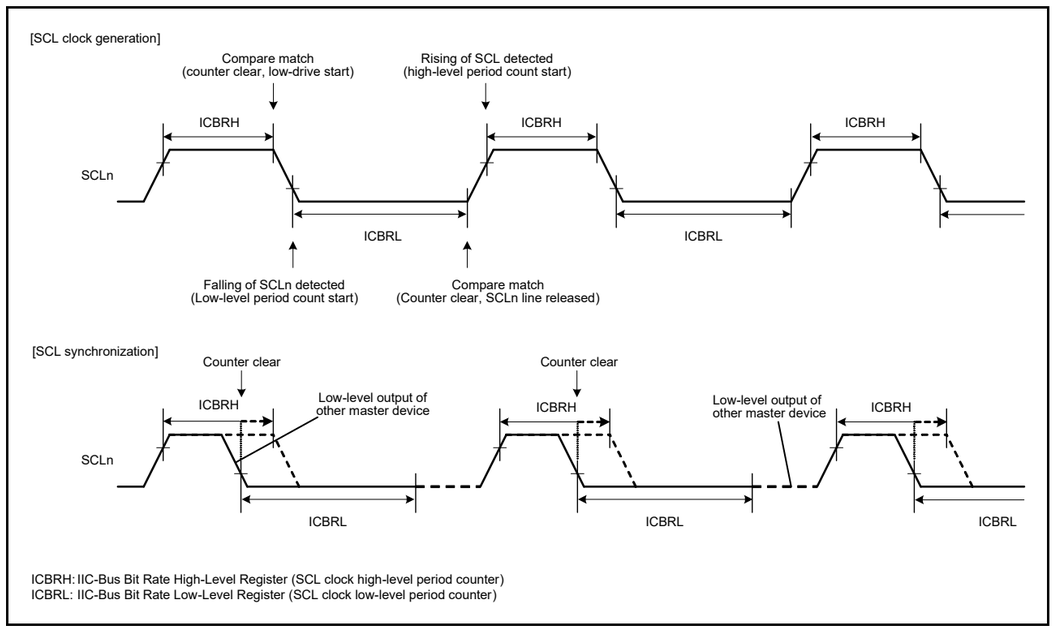


Figure 36.21 Generation and synchronization of SCL signal from IIC

36.4 SCL同步电路

为了生成SCL时钟，IIC在检测到SCLn线上的上升沿时开始对ICBRH中指定的高电平周期的值进行计数，并在完成计数时将SCLn线驱动为低电平。当IIC检测到SCLn线的下降沿时，它开始计数ICBRL中指定的低电平周期的值，然后停止驱动SCLn线，当它完成计数时释放线。IIC重复此过程以生成SCL时钟。

如果多个主设备连接到I2C总线，由于与另一个主设备争用，可能会出现SCL信号冲突。在这种情况下，主设备必须同步它们的SCL信号。由于SCL信号的这种同步必须逐位进行，因此IIC配备了SCL同步电路，通过在主机模式下监视SCLn线来获得SCL时钟信号的逐位同步。

当IIC检测到SCLn线上的上升沿并开始计数ICBRH中指定的高电平周期，并且SCLn线上的电平由于另一个主设备正在生成SCL信号而下降，IIC停止计数它检测下降沿，将SCLn线上的电平驱动为低电平，并开始计算ICBRL中指定的低电平周期。当IIC完成对低电平周期的计数时，它停止将SCLn线驱动为低电平以释放该线。此时，如果来自其他主设备的SCL时钟信号的低电平周期长于IIC中设置的低电平周期，则延长SCL信号的低电平周期。当另一个主设备的低电平周期结束时，SCL信号上升，因为SCLn线被释放。当IIC输出完SCL时钟的低电平周期后，SCLn线被释放，SCL时钟上升。即当来自多个主控的SCL信号竞争时，SCL信号的高电平周期与周期较窄的时钟同步，SCL信号的低电平周期与主控的低电平周期同步。具有更广泛周期的时钟。仅当ICFER中的SCLE位设置为1时，才启用SCL信号的这种同步。

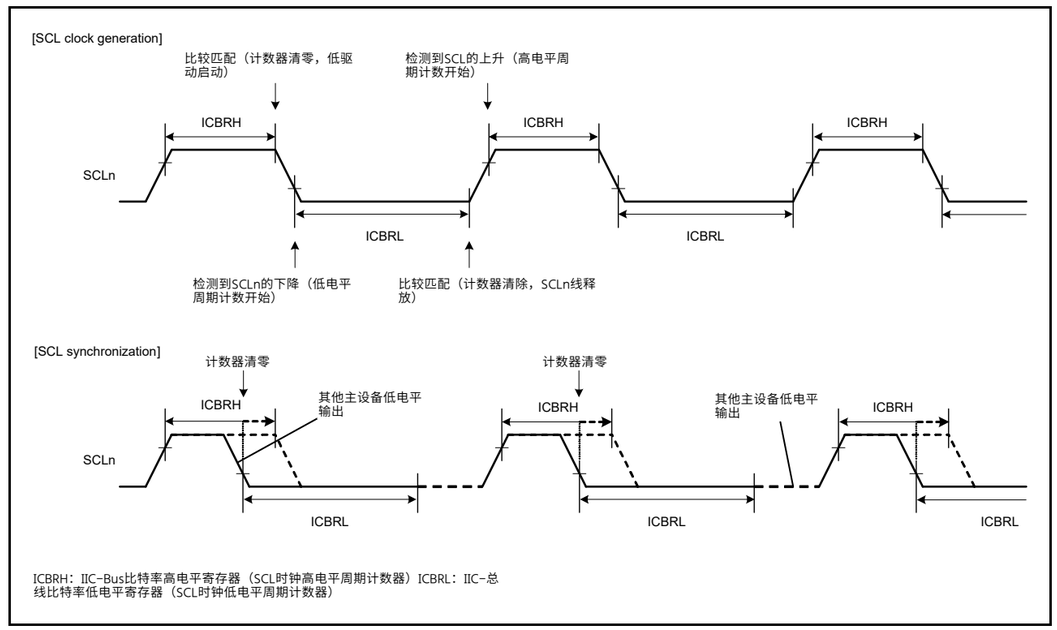


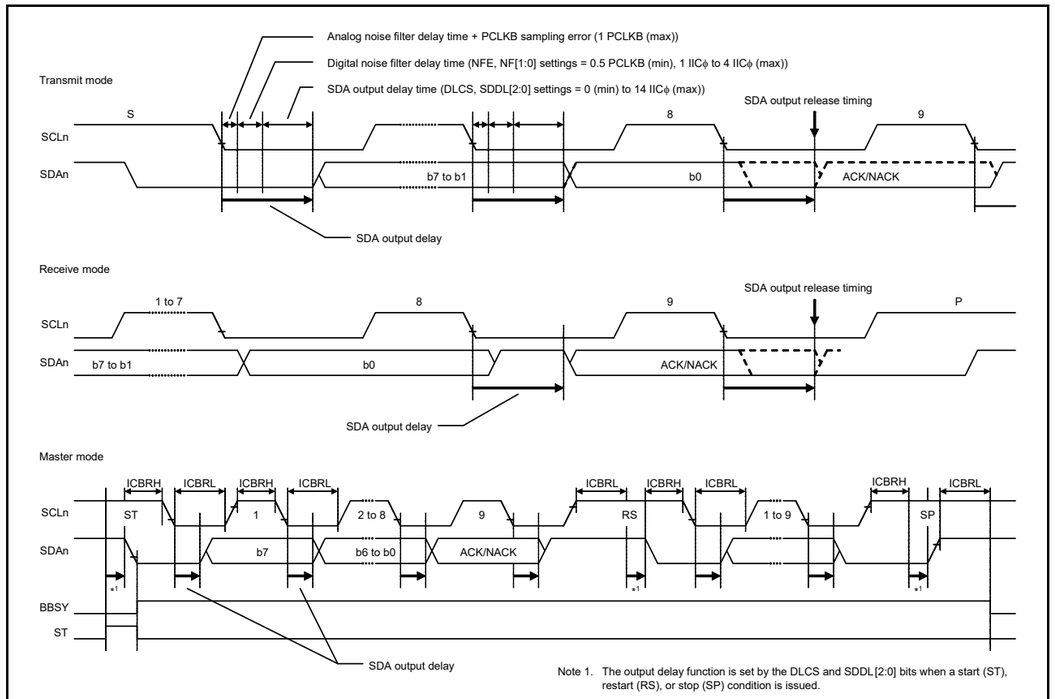
Figure 36.21 从IIC生成和同步SCL信号

36.5 SDA Output Delay Function

The IIC module incorporates a function for delaying output on the SDA line. The delay can be applied to all output on the SDA line, including issuing of the start, restart, and stop conditions, data, and the ACK and NACK signals.

With this function, SDA output is delayed from the detection of a falling edge of the SCL signal to ensure that the SDA signal is output within the interval during which the SCL clock is low. This approach helps prevent erroneous operation of communications devices, with the aim of satisfying the 300-ns minimum data-hold time requirement of the SMBus specification. The output delay function is enabled by setting the SDDL[2:0] bits in ICMR2 to any value other than 000b, and disabled by setting the same bits to 000b.

While the SDA output delay function is enabled, for example, while the SDDL[2:0] bits in ICMR2 are set to any value other than 000b, the DLCS bit in ICMR2 selects the clock source for counting by the SDA output delay counter either as the internal base clock (IICϕ) for the IIC module or as the internal base clock divided by 2 (IICϕ/2). The counter counts the number of cycles set in the SDDL[2:0] bits in ICMR2. After the delay cycles count is complete, the IIC module places the required output (start, restart, or stop condition, data, or an ACK or NACK signal) on the SDA line.



Note 1. The output delay function is set by the DLCS and SDDL[2:0] bits when a start (ST), restart (RS), or stop (SP) condition is issued.

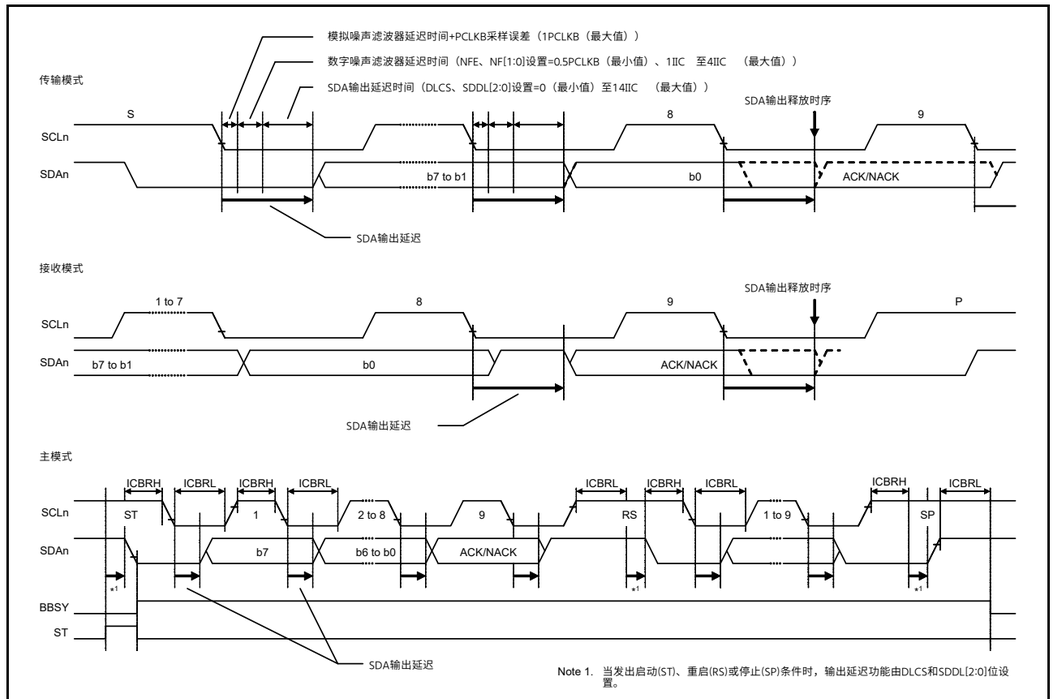
Figure 36.22 SDA output delay function

36.5 SDA输出延迟功能

IIC模块包含延迟SDA线上输出的功能。延迟可应用于SDA线上的所有输出，包括发出启动、重启和停止条件、数据以及ACK和NACK信号。

使用此功能，SDA输出从检测到SCL信号的下降沿开始延迟，以确保在SCL时钟为低电平的时间间隔内输出SDA信号。这种方法有助于防止通信设备的错误操作，旨在满足SMBus规范的300ns最小数据保持时间要求。通过将ICMR2中的SDDL[2:0]位设置为000b以外的任何值来启用输出延迟功能，并通过将相同位设置为000b来禁用输出延迟功能。

当SDA输出延迟功能使能时，例如，当ICMR2中的SDDL[2:0]位设置为000b以外的任何值时，ICMR2中的DLCS位选择时钟源以供SDA输出延迟计数器计数作为IIC模块的内部基本时钟(IIC)或除以2的内部基本时钟(IIC 2)。计数器计算ICMR2中SDDL[2:0]位中设置的周期数。延迟周期计数完成后，IIC模块将所需的输出（启动、重启或停止条件、数据或ACK或NACK信号）放在SDA线上。



Note 1. 当发出启动(ST)、重启(RS)或停止(SP)条件时，输出延迟功能由DLCS和SDDL[2:0]位设置。

Figure 36.22 SDA输出延迟功能

36.6 Digital Noise Filter Circuits

The states of the SCLn and SDAn pins are conveyed to the internal circuitry through analog and digital noise-filter circuits. Figure 36.23 shows a block diagram of the digital noise-filter circuit.

The on-chip digital noise-filter circuit of the IIC consists of four flip-flop circuit stages connected in series and a match-detection circuit. The number of valid stages in the digital noise filter is selected in the NF[1:0] bits in ICMR3. The selected number of valid stages determines the noise-filtering capability as a period from one to four IICϕ cycles.

The input signal to the SCLn pin (or SDAn pin) is sampled on falling edges of the IICϕ signal. When the input signal level matches the output level of the number of valid flip-flop circuit stages as selected in the NF[1:0] bits in ICMR3, the signal level is conveyed to the subsequent stage. If the signal levels do not match, the previous value is saved.

If the ratio between the frequency of the internal operating clock (PCLKB) and the transfer rate is small, for example, if data transfer is 400 kbps with PCLKB = 4 MHz, the characteristics of the digital noise filter might lead to the elimination of required signals as noise. In such cases, it is possible to disable the digital noise-filter circuit, by setting the ICFER.NFE bit to 0, and use only the analog noise filter circuit.

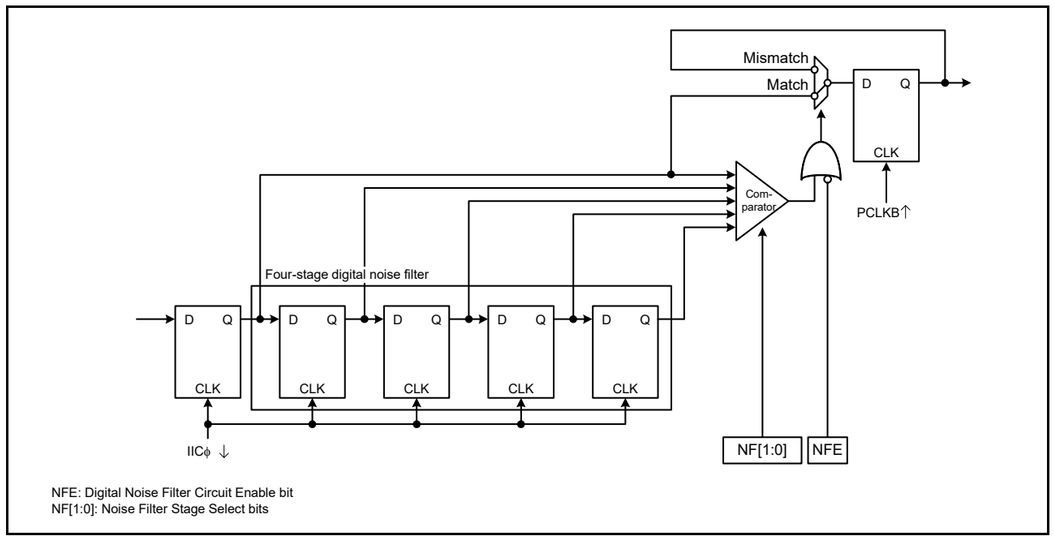


Figure 36.23 Digital noise filter circuit block diagram

36.7 Address Match Detection

The IIC can set three unique slave addresses in addition to the general call address and host address, and also can set 7- or 10-bit slave addresses.

36.7.1 Slave-Address Match Detection

The IIC can set three unique slave addresses and has a slave address detection function for each unique slave address. When the SARyE bit (y = 0 to 2) in ICSER is set to 1, the slave addresses set in SARUy and SARLy (y = 0 to 2) can be detected.

When the IIC detects a match of the set slave address, the associated AASy flag (y = 0 to 2) in ICSR1 is set to 1 on the rising edge of the ninth SCL clock cycle, and the RDRF flag in ICSR2 or the TDRE flag in ICSR2 is set to 1 by the subsequent R/W# bit. This causes a receive data full interrupt (IICn_RXI) or transmit data empty interrupt (IICn_TXI) to be generated. The AASy flag identifies which slave address is specified.

Figure 36.24 to Figure 36.26 show the AASy flag set timing in three cases.

36.6 数字噪声滤波器电路

SCLn和SDAn引脚的状态通过模拟和数字噪声滤波器电路传送到内部电路。图36.23显示了数字噪声滤波器电路的框图。

IIC的片上数字噪声滤波器电路由四个串联的触发器电路级和一个匹配检测电路组成。数字噪声滤波器的有效级数在ICMR3的NF[1:0]位中选择。选定的有效级数决定了噪声过滤能力，周期为1到4个IIC 周期。

SCLn引脚（或SDAn引脚）的输入信号在IIC 信号的下降沿采样。当输入信号电平与在ICMR3的NF[1:0]位中选择的有效触发器电路级数的输出电平匹配时，信号电平被传送到下一级。如果信号电平不匹配，则保存先前的值。

如果内部工作时钟(PCLKB)的频率与传输速率之间的比率很小，例如，如果数据传输为400kbps，PCLKB=4MHz，则数字噪声滤波器的特性可能会导致消除所需的信号作为噪声。在这种情况下，可以通过将ICFER.NFE位设置为0来禁用数字噪声滤波器电路，并仅使用模拟噪声滤波器电路。

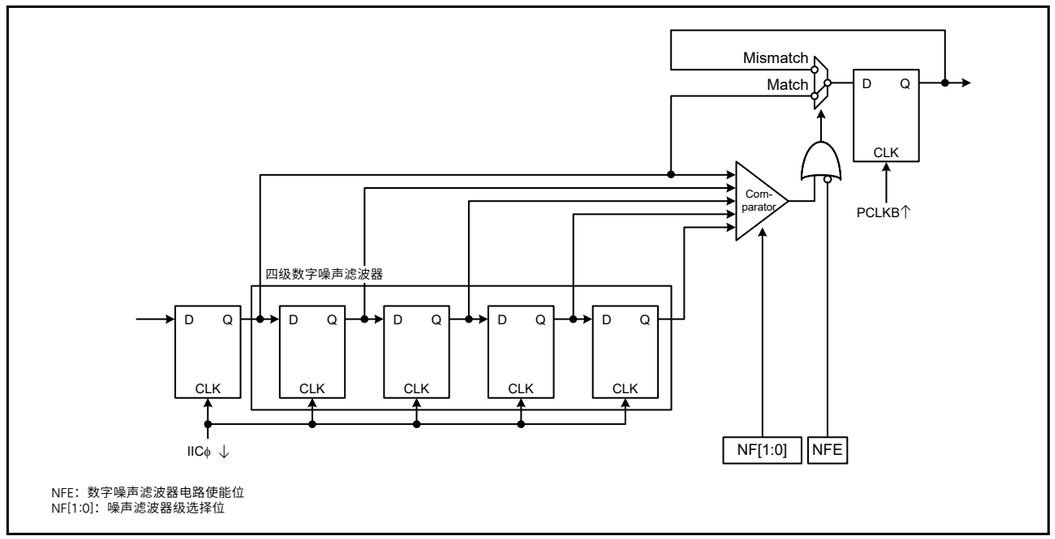


Figure 36.23 数字噪声滤波器电路框图

36.7 地址匹配检测

IIC除了可以设置广播地址和主机地址外，还可以设置三个唯一的从机地址，也可以设置7位或10位的从机地址。

36.7.1 从地址匹配检测

IIC可以设置三个唯一的从机地址，并对每个唯一的从机地址具有从机地址检测功能。
当ICSER中的SARyE位（y=0到2）设置为1时，可以检测到设置在SARUy和SARLy（y=0到2）中的从机地址。

当IIC检测到与设置的从地址匹配时，ICSR1中相关的AASy标志（y=0到2）在第9个SCL时钟周期的上升沿设置为1，并且ICSR2中的RDRF标志或TDRE标志ICSR2中的1由随后的RW#位设置为1。这会导致产生接收数据满中断（IICn_RXI）或发送数据空中断（IICn_TXI）。AASy标志标识指定了哪个从地址。

图36.24至图36.26显示了三种情况下的AASy标志设置时序。

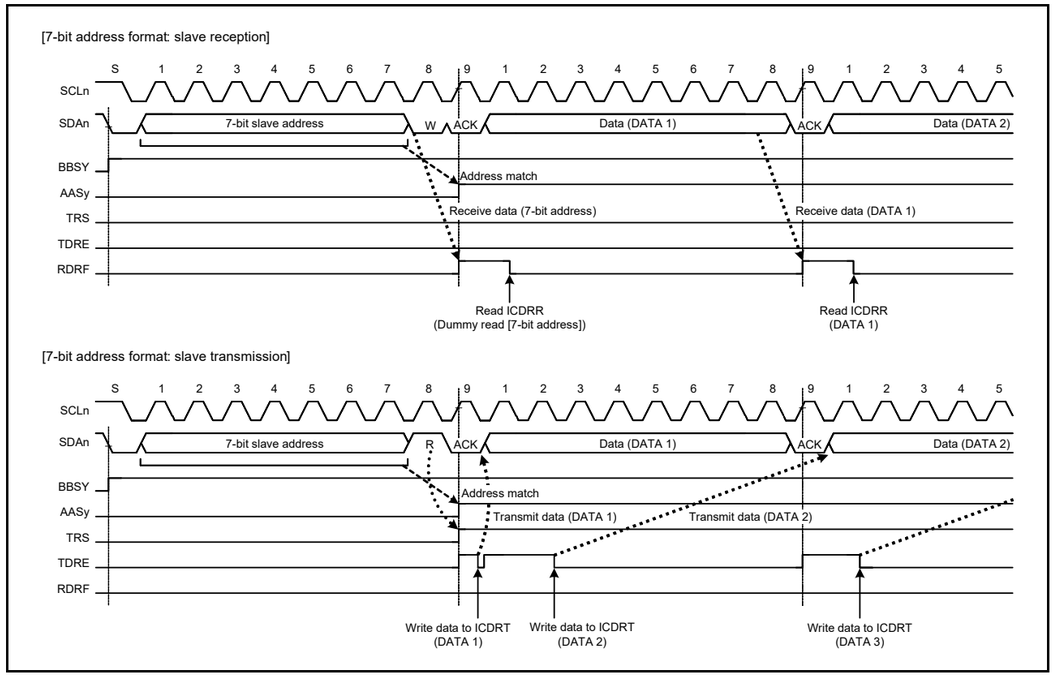


Figure 36.24 AASy flag set timing with 7-bit address format

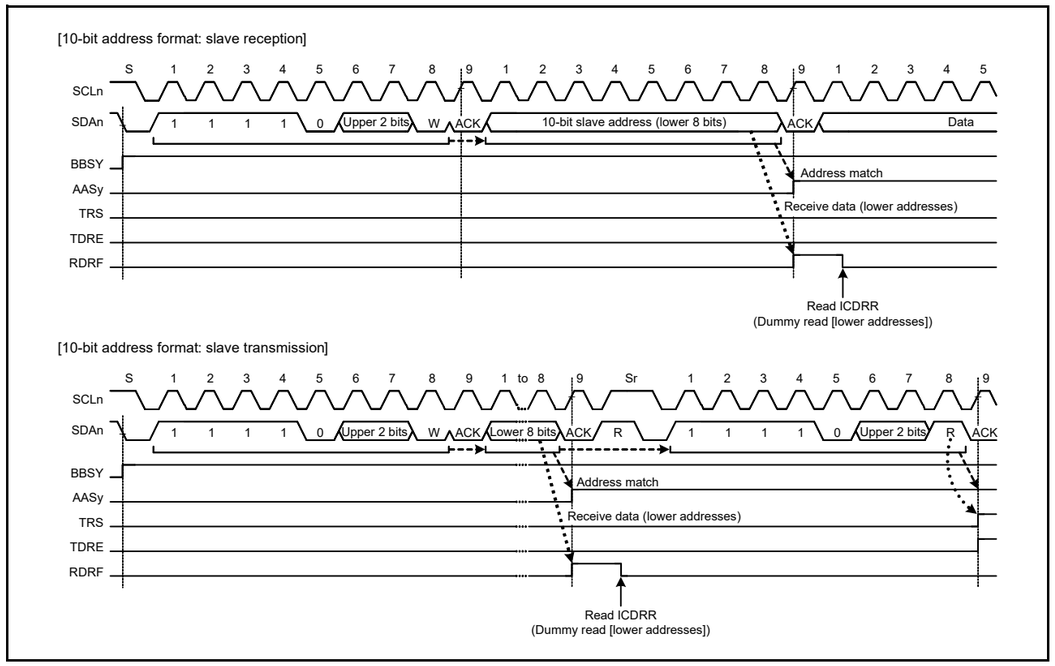


Figure 36.25 AASy flag set timing with 10-bit address format

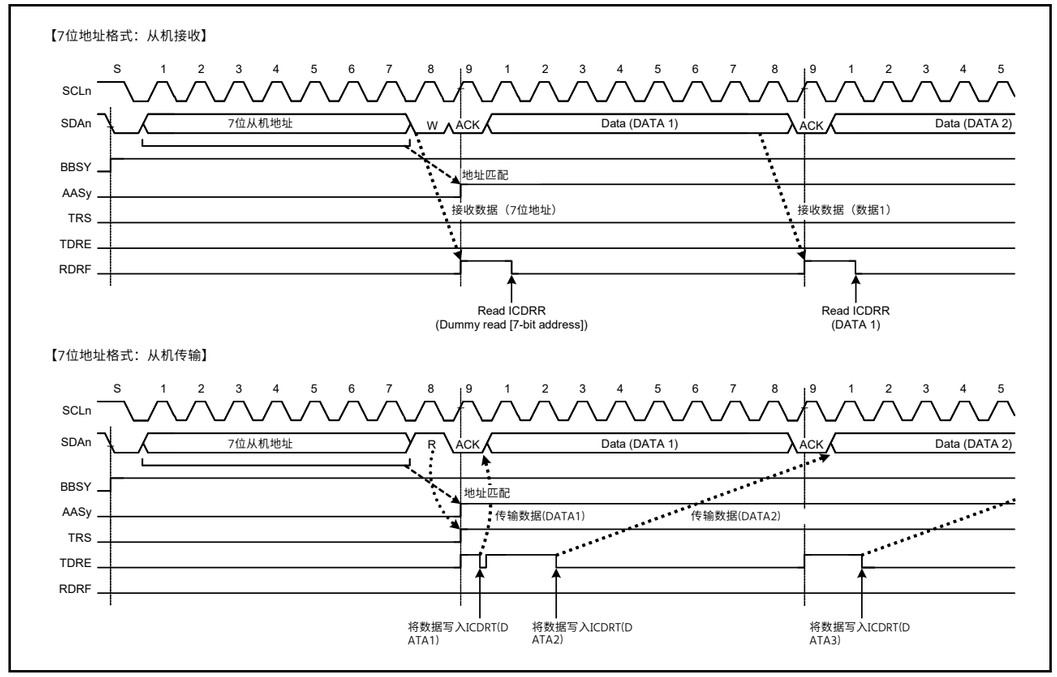


Figure 36.24 7位地址格式的AASy标志设置时序

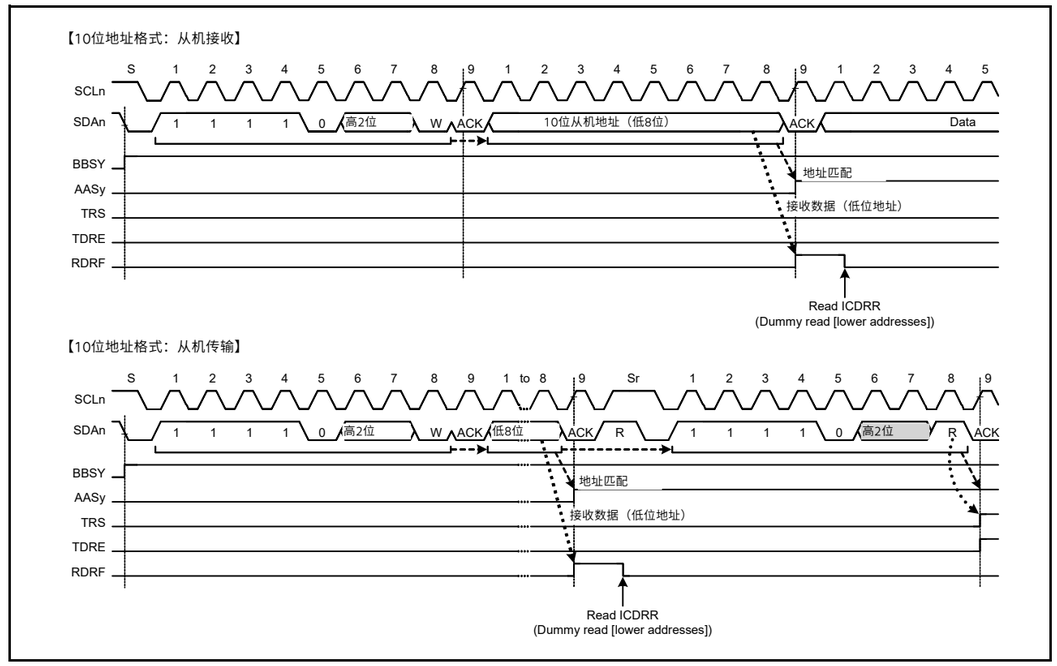


Figure 36.25 10位地址格式的AASy标志设置时序

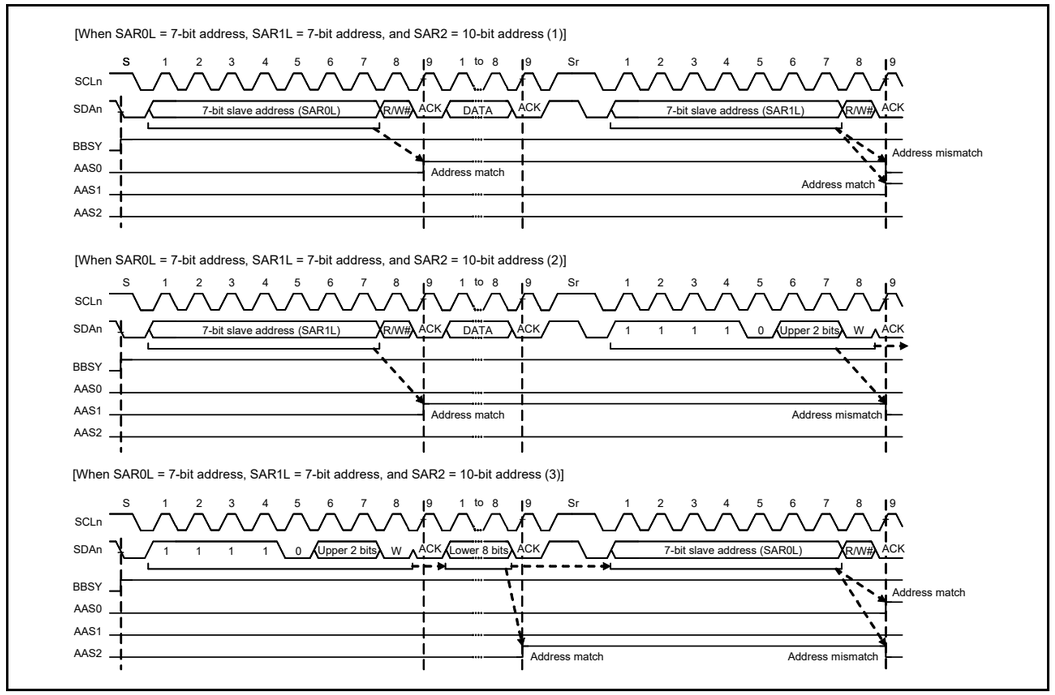


Figure 36.26 AASy flag set and clear timing with 7-bit and 10-bit address formats mixed

36.7.2 Detection of General Call Address

The IIC provides detection of the general call address (0000 000b + 0 [W]). This is enabled by setting the GCAE bit in ICSER to 1.

If the address received after a start or restart condition is issued is 0000 000b + 1[R] (start byte), the IIC recognizes this as the address of a slave device with an all-zero address, but not as the general call address.

When the IIC detects the general call address, both the GCA flag in ICSR1 and the RDRF flag in ICSR2 set to 1 on the rising edge of the ninth cycle of the SCL clock. This leads to the generation of a receive data full interrupt (IICn_RXI). The value of the GCA flag can be checked to confirm that the general call address was transmitted.

Operation after detection of the general call address is the same as normal slave receive operation.

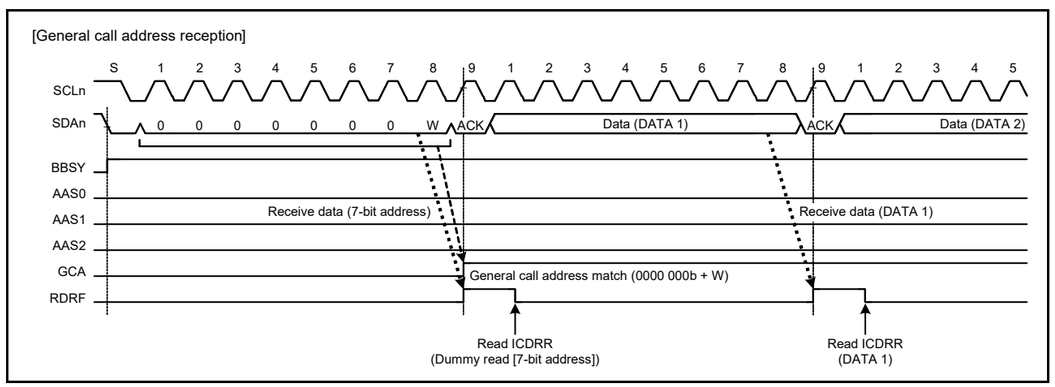


Figure 36.27 Timing of GCA flag setting during reception of general call address

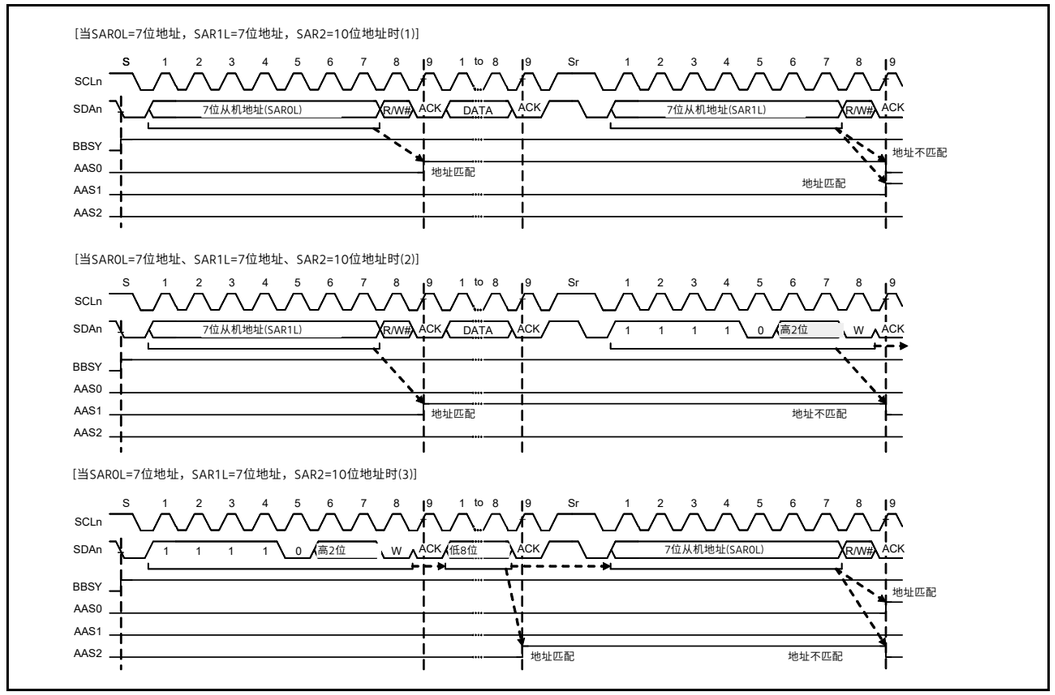


Figure 36.26 混合7位和10位地址格式的AASy标志设置和清除时序

36.7.2 广播呼叫地址检测

IIC提供对广播呼叫地址(0000000b+0[W])的检测。这是通过设置GCAE位启用
ICSER to 1.

如果在发出启动或重新启动条件后接收到的地址是0000000b+1[R]（起始字节），则IIC将其识别为具有全零地址的从设备的地址，但不是广播地址.

当IIC检测到广播呼叫地址时，ICSR1中的GCA标志和ICSR2中的RDRF标志都在SCL时钟的第9个周期的上升沿设置为1。这会导致接收数据完全中断(IICn_RXI)的产生。可以检查GCA标志的值以确认广播呼叫地址已被传输。

检测到广播呼叫地址后的操作与正常的从机接收操作相同。

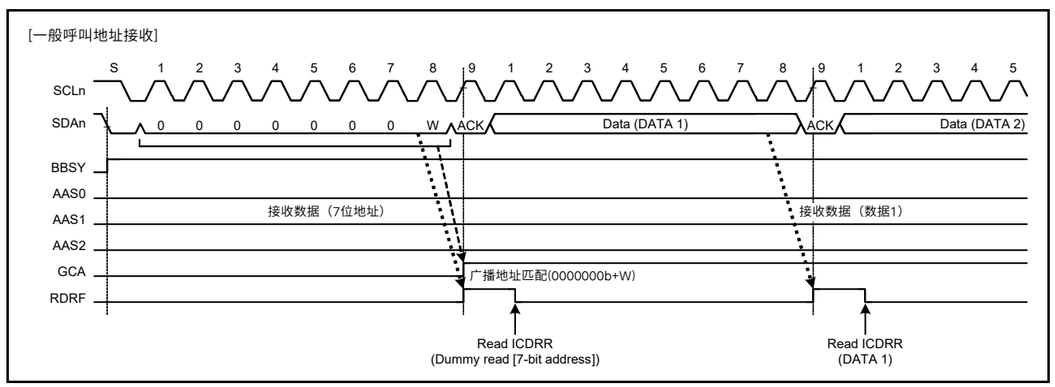


Figure 36.27 在接收广播呼叫地址期间设置GCA标志的时机

36.7.3 Device-ID Address Detection

The IIC module provides detection of device-ID address compliant with the I2C bus specification (revision 03). When the IIC receives 1111 100b as the first byte after a start or restart condition was issued with the DIDE bit in ICSER set to 1, it recognizes the address as a device ID, sets the DID flag in ICSR1 to 1 on the rising edge of the 9th SCL clock cycle when the subsequent R/W# bit is 0, and then compares the second and subsequent bytes with its own slave address. If the address matches the value in the slave address register, the IIC sets the associated AASy flag (y = 0 to 2) in ICSR1 to 1.

After that, when the first byte received after issuance of a start or restart condition matches the device ID address (1111 100b) again and the subsequent R/W# bit is 1, the IIC does not compare the second and subsequent bytes and sets the ICSR2.TDRE flag to 1.

In the device-ID address detection function, the IIC sets the DID flag to 0 if a match with the IIC slave address is not obtained or a match with the device ID address is not obtained after a match with the IIC slave address and the detection of a restart condition. If the first byte after detection of a start or restart condition matches the device-ID address (1111 100b), and the R/W# bit is 0, the IIC sets the DID flag to 1 and compares the second and subsequent bytes with the slave address of the IIC. If the R/W# bit is 1, the DID flag holds the previous value and the IIC does not compare the second and subsequent bytes. In this way, the reception of a device-ID address can be checked by reading the DID flag after confirming that TDRE = 1.

Additionally, prepare the device-ID fields (3 bytes: 12 bits indicating the manufacturer + 9 bits identifying the part + 3 bits indicating the revision) that must be sent to the host after reception of a continuous device-ID field as normal transmit data. For details on the information that must be included in device-ID fields, contact NXP Semiconductors.

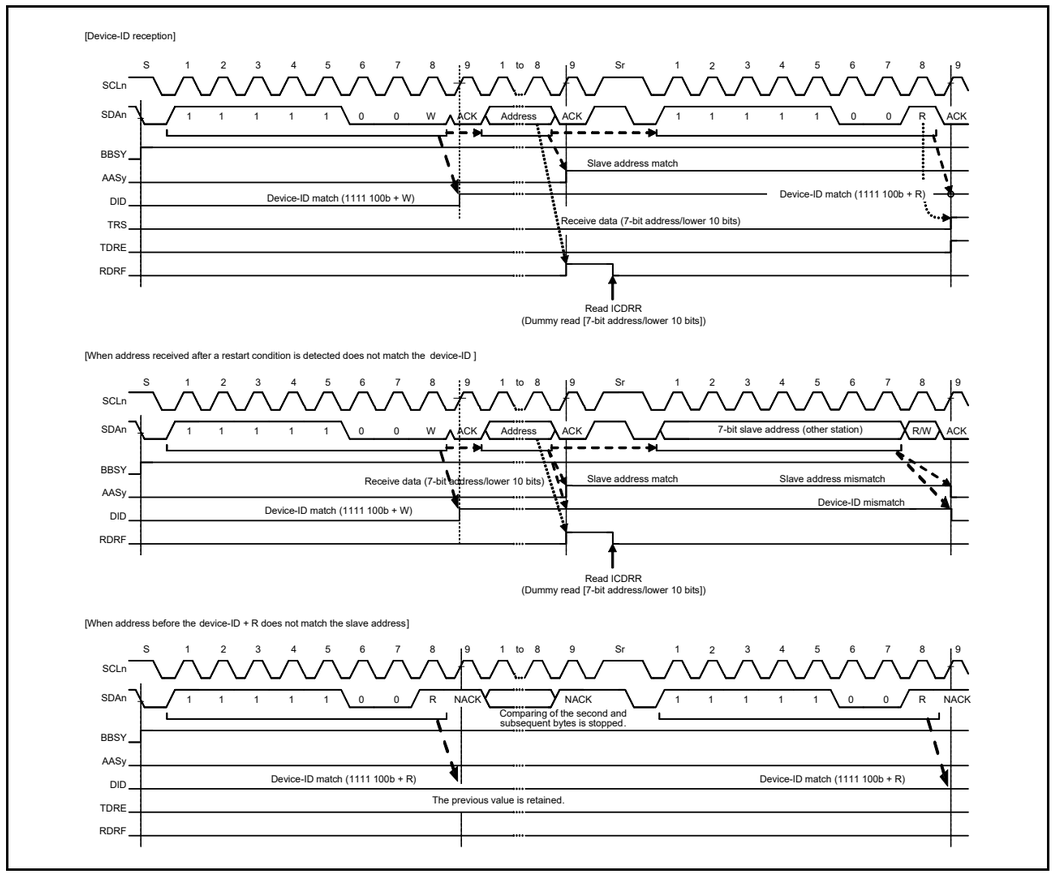


Figure 36.28 AASy and DID flag set and clear timing during reception of device-ID

36.7.3 设备ID地址检测

IIC模块提供符合I2C总线规范（修订版03）的设备ID地址检测。当IIC在ICSER中的DIDE位设置为1的情况下发出启动或重启条件后接收到1111100b作为第一个字节时，它将地址识别为设备ID，在ICSR1的上升沿将DID标志设置为1当后续的RW#位为0时，第9个SCL时钟周期，然后将第二个和后续字节与自己的从地址进行比较。如果地址与从地址寄存器中的值匹配，则IIC将ICSR1中相关的AASy标志（y=0到2）设置为1。

之后，当发出启动或重启条件后接收到的第一个字节再次与设备ID地址(1111100b)匹配且后续RW#位为1时，IIC不比较第二个和后续字节并设置ICSR2。TDRE标志为1。

在device-ID地址检测功能中，如果与IIC从机地址匹配未得到匹配或与IIC从机地址匹配后未得到与设备ID地址匹配，则IIC将DID标志设置为0。的重新启动条件。如果检测到启动或重启条件后的第一个字节与设备ID地址(1111100b)匹配，并且RW#位为0，则IIC将DID标志设置为1，并将第二个和后续字节与从机地址进行比较IIC的。如果RW#位为1，则DID标志保持前一个值，并且IIC不比较第二个和后续字节。这样，在确认TDRE=1后，可以通过读取DID标志来检查设备ID地址的接收。

此外，准备设备ID字段（3个字节：12位表示制造商+9位表示部件+3位表示修订）在接收到连续的设备ID字段作为正常发送数据后必须发送到主机.有关必须包含在设备ID字段中的信息的详细信息，请联系NXPSemiconductors。

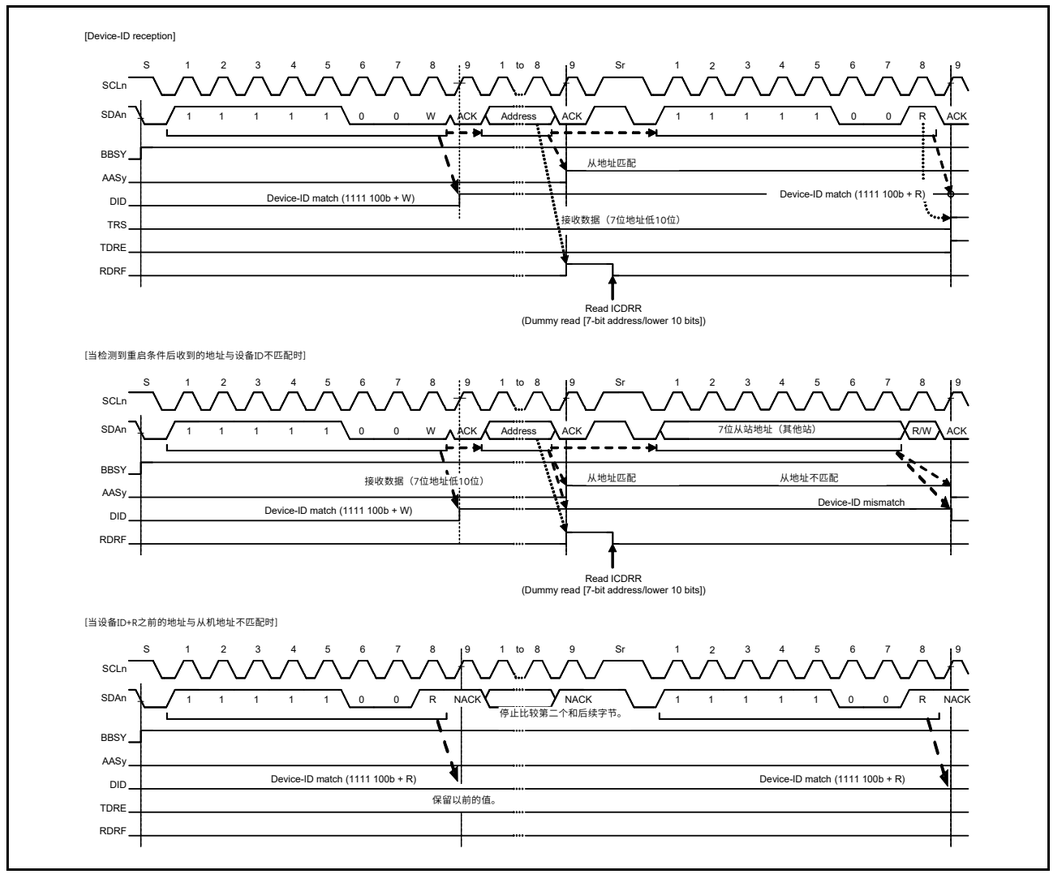


Figure 36.28 在接收设备ID期间设置AASy和DID标志并清除时序

36.7.4 Host Address Detection

The IIC provides host address detection while the SMBus is operating. When the HOAE bit in ICSER is set to 1 while the SMBS bit in ICMR3 is 1, the IIC can detect the host address (0001 000b) in slave receive mode (MST and TRS bits = 00b in ICCR2).

When the IIC detects the host address, the HOA flag in ICSR1 is set to 1 on the rising edge of the ninth SCL clock cycle, and at the same time, the RDRF flag in ICSR2 is set to 1 when the R/W# bit is 0 (Wr bit). This causes a receive data full interrupt (IICn_RXI) to be generated. The HOA flag indicates that the host address was sent from another device.

If the bit following the host address (0001 000b) is an Rd bit (R/W# bit = 1), the IIC can also detect the host address. After the host address is detected, the IIC operates in the same manner as in normal slave operation.

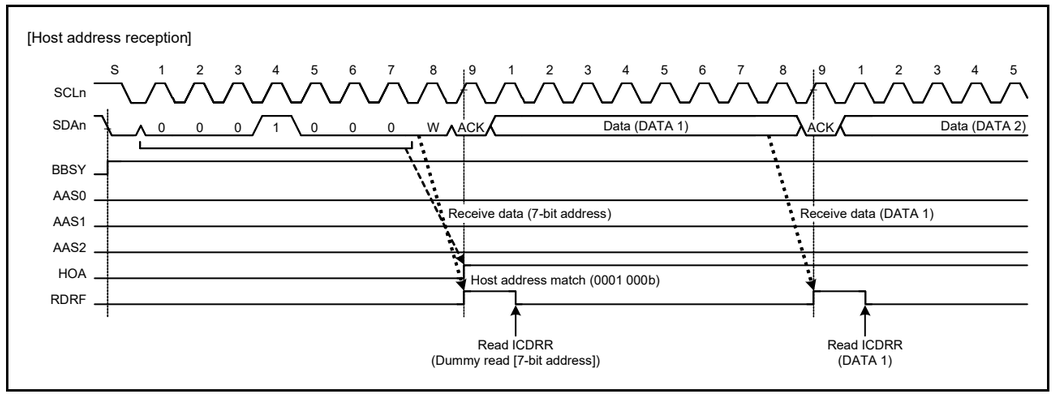


Figure 36.29 HOA flag set timing during reception of host address

36.8 Wakeup Function

The IIC provides a wakeup function that causes the MCU to transition from Software Standby mode to normal operation. The wakeup function enables the reception of data when the system clock is stopped, and it generates a wakeup interrupt signal on the match of the slave address of the received data. This interrupt signal triggers the return to normal operation.

The wakeup function has four operation modes: normal wakeup mode 1, normal wakeup mode 2, command recovery mode, and EEP response mode. Table 36.9 describes the behavior in these modes.

Table 36.9 Wakeup operation modes

Operation mode	ACK response timing	ACK response before wakeup	SCL state during wakeup
Normal wakeup mode 1	Before wakeup	ACK	Fixed low
Normal wakeup mode 2	After wakeup	Before wakeup: no response After wakeup: ACK response	Fixed low
Command recovery mode	Before wakeup	ACK	Open
EEP response mode	Before wakeup	NACK	Open

Precautions on the use of the wakeup function

1. Disable the wakeup function (WUE = 0) after a wakeup interrupt triggers the transition from Software Standby mode to normal operation.
2. Do not change the content of the IIC registers while WUF = 0, even if the wakeup interrupt recovers the system clock. Make register settings after confirming that WUF = 1.
3. Set WUE = WUIE = 1 and MST = TRS = 0 (slave reception mode) before entering Software Standby mode.
4. Do not invoke Software Standby mode while BBSY = 1.
5. The wakeup function supports the 7-bit slave address of slave address register SARL0, the general call address, and

36.7.4 主机地址检测

IIC在SMBus运行时提供主机地址检测。当ICSER中的HOAE位设置为1而ICMR3中的SMBS位为1时，IIC可以在从机接收模式下检测主机地址（0001000b）（ICCR2中的MST和TRS位=00b）。

当IIC检测到主机地址时，ICSR1中的HOA标志在第9个SCL时钟周期的上升沿置1，同时在RW#位为0时ICSR2中的RDRF标志置1（写位）。这会导致产生接收数据完全中断（IICn_RXI）。HOA标志表明主机地址是从另一个设备发送的。

如果主机地址（0001000b）后面的位是Rd位（RW#位=1），则IIC也可以检测主机地址。
检测到主机地址后，IIC以与正常从机操作相同的方式运行。

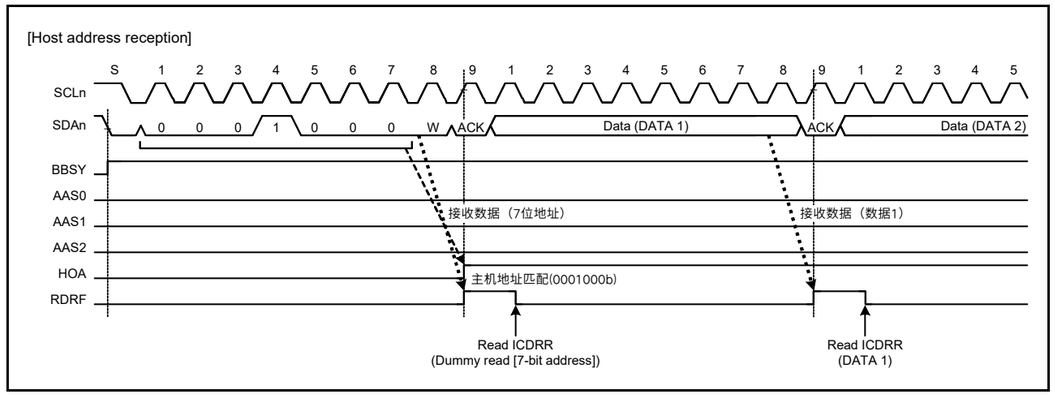


Figure 36.29 接收主机地址期间的HOA标志设置时序

36.8 唤醒功能

IIC提供唤醒功能，使MCU从软件待机模式转换到正常操作。唤醒功能在系统时钟停止时启用数据接收，并在接收到的数据的从地址匹配时产生唤醒中断信号。该中断信号触发返回正常操作。

唤醒功能有四种操作模式：正常唤醒模式1、正常唤醒模式2、命令恢复模式和EEP响应模式。表36.9描述了这些模式下的行为。

Table 36.9 唤醒操作模式

操作模式	ACK响应时间	唤醒前的ACK响应	唤醒期间的SCL状态
正常唤醒模式1	醒来前	ACK	固定低
正常唤醒模式2	醒来后	唤醒前：无响应唤醒后：ACK响应	固定低
命令恢复模式	醒来前	ACK	Open
EEP响应模式	醒来前	NACK	Open

唤醒功能使用注意事项

1. 在唤醒中断触发从软件待机模式到正常操作的转换后，禁用唤醒功能(WUE=0)。
2. 当WUF=0时不要改变IIC寄存器的内容，即使唤醒中断恢复了系统时钟。确认WUF=1后进行寄存器设置。
3. 在进入软件待机模式之前设置WUE=WUIE=1和MST=TRS=0（从接收模式）。
4. 当BBSY=1时不要调用软件待机模式。
5. 唤醒功能支持从地址寄存器SARL0的7位从地址、广播地址和

the host address. 10-bit slave addresses, SARL1 and SARL2, are not supported. Do not use them.

6. When the wakeup function is enabled, disable the interrupt selectable in the ICIER bits (TIE, TEIE, RIE, NAKIE, SPIE, STIE, ALIE, and TMOIE).
7. When the wakeup function is enabled, do not use the timeout function.
8. If the transition from Software Standby mode is triggered by the interrupt (such as IRQn) other than a wakeup interrupt. WUF is not set in this case. Follow the processing shown in Figure 36.31 and Figure 36.36.

36.8.1 Normal Wakeup Mode 1

This section describes the behavior, the timing, and an example operation of normal wakeup mode 1.

1. A wakeup interrupt triggered by a match of the slave address initiates the transition to normal operation as follows. Figure 36.32 provides detailed timing and Figure 36.30 shows an example operation.

   Before wakeup:ACK is sent in response to the data received with the own slave address of the IIC.

   During wakeup:ACK response is made on the ninth clock cycle of SCL, and SCL is held low afterwards.*1

   After wakeup:Normal operation continues.

   If the slave address does not match, the SCL line is not held low after the fall of the ninth clock cycle of SCL, and the slave operation continues.

Note 1. Between the ninth clock cycle and the first clock cycle during wakeup, WAIT = 1 is invalid.

2. If the transition from Software Standby mode is triggered by the interrupt (such as IRQn) other than a wakeup interrupt. WUF is not set in this case. Follow the processing shown in Figure 36.31.

主机地址。不支持10位从机地址SARL1和SARL2。不要使用它们。

6. 启用唤醒功能时，禁用ICIER位（TIE、TEIE、RIE、NAKIE、SPIE, STIE, ALIE, and TMOIE).
7. 启用唤醒功能时，请勿使用超时功能。
8. 如果从软件待机模式的转换是由唤醒中断以外的中断（例如IRQn）触发的。在这种情况下没有设置WUF。按照图36.31和图36.36所示的处理。

36.8.1 正常唤醒模式1

本节介绍正常唤醒模式1的行为、时序和示例操作。

1. 由匹配的从地址触发的唤醒中断启动到正常操作的转换，如下所示。
   图36.32提供了详细的时序，图36.30显示了一个示例操作。

   唤醒前：发送ACK以响应接收到的带有IIC自身从地址的数据。

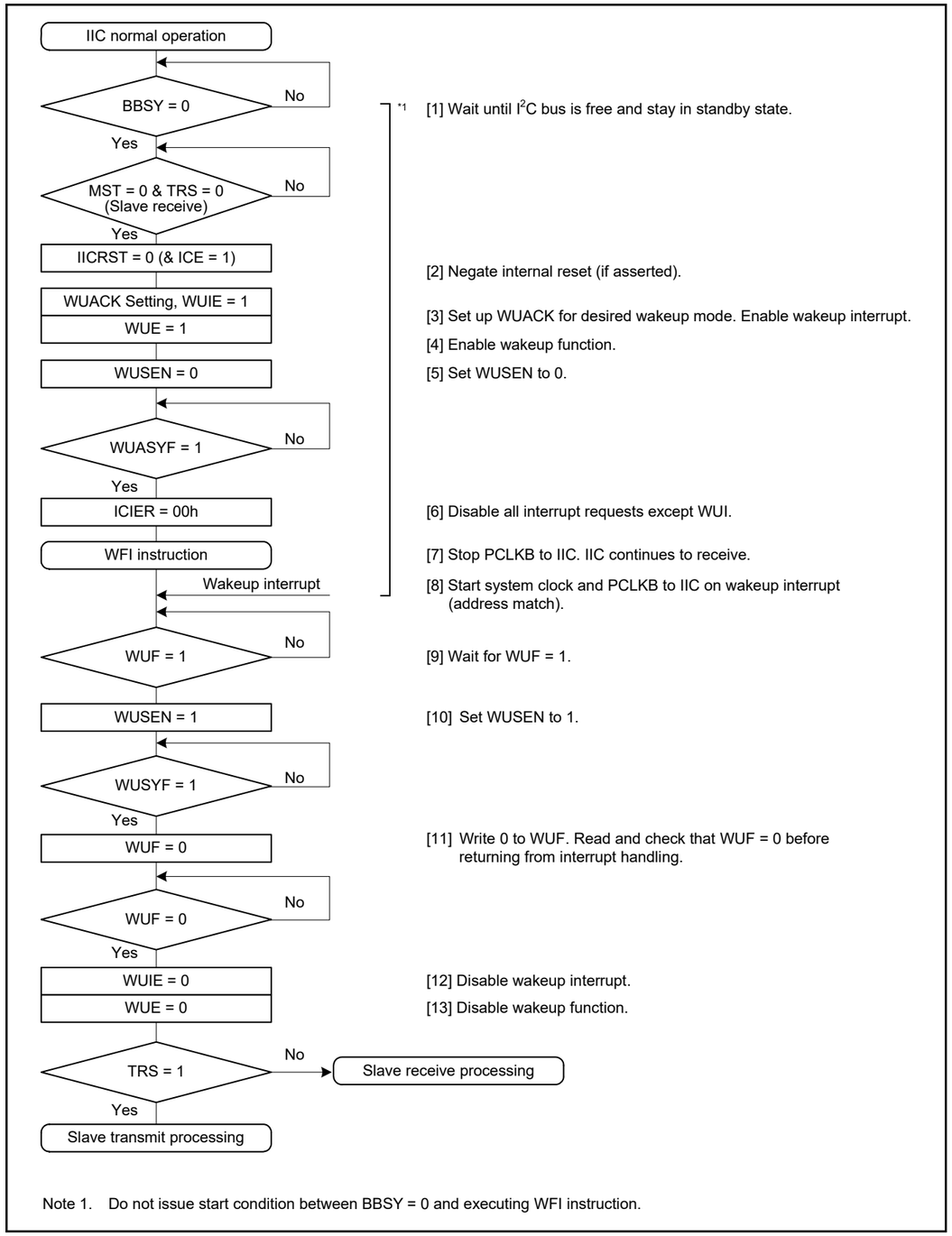
   唤醒期间：在SCL的第9个时钟周期做出ACK响应，之后SCL保持低电平。*1

   唤醒后：继续正常运行。

   如果从机地址不匹配，则在SCL的第9个时钟周期下降后，SCL线不保持低电平，从机操作继续。

注1.在唤醒期间的第9个时钟周期和第一个时钟周期之间，WAIT=1无效。

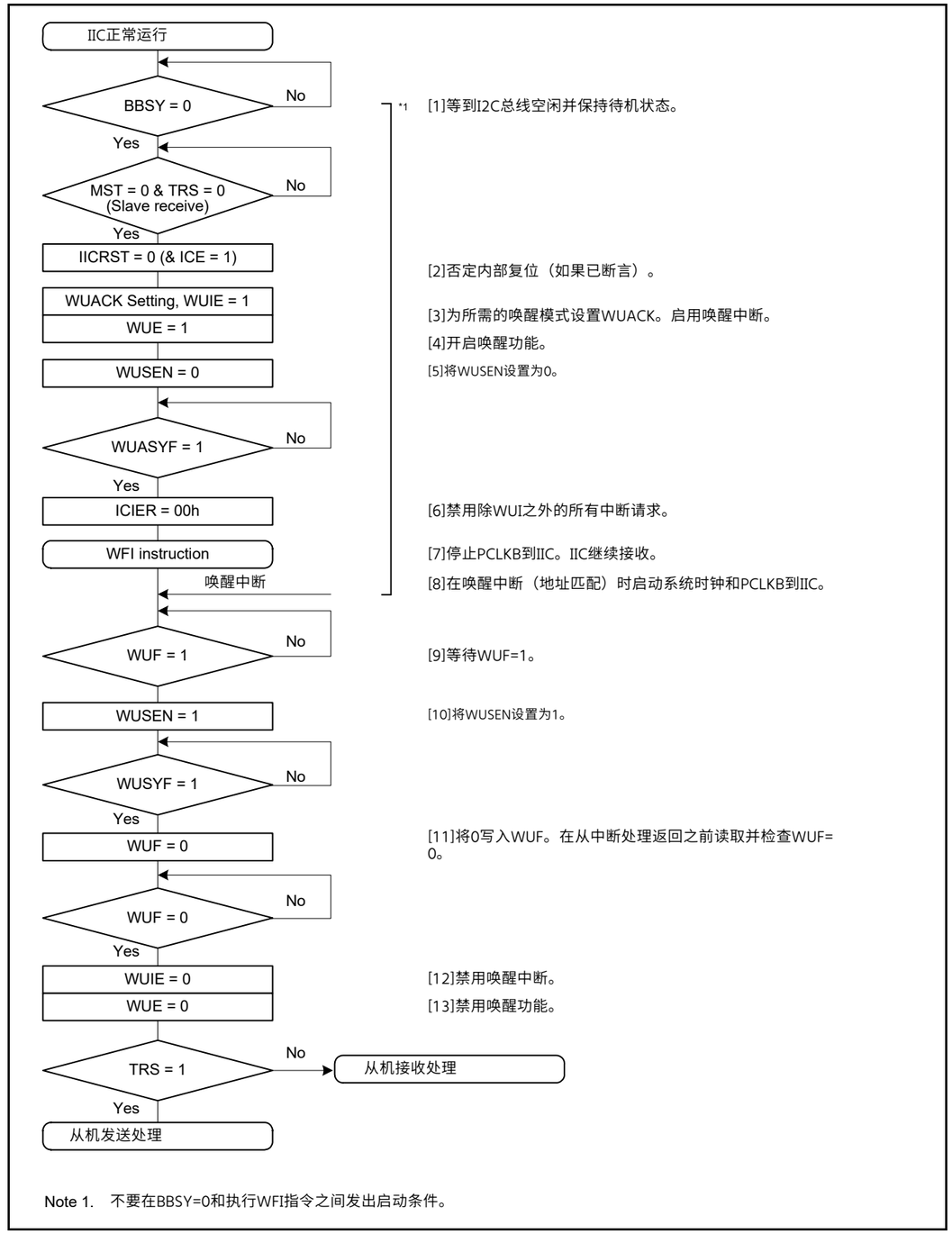
2. 如果从软件待机模式的转换是由唤醒中断以外的中断（例如IRQn）触发的。在这种情况下没有设置WUF。按照图36.31所示的处理。



Note 1. Do not issue start condition between BBSY = 0 and executing WFI instruction.

Figure 36.30 Example operation of normal wakeup mode 1 when wakeup is triggered by a wakeup interrupt on match of the slave address

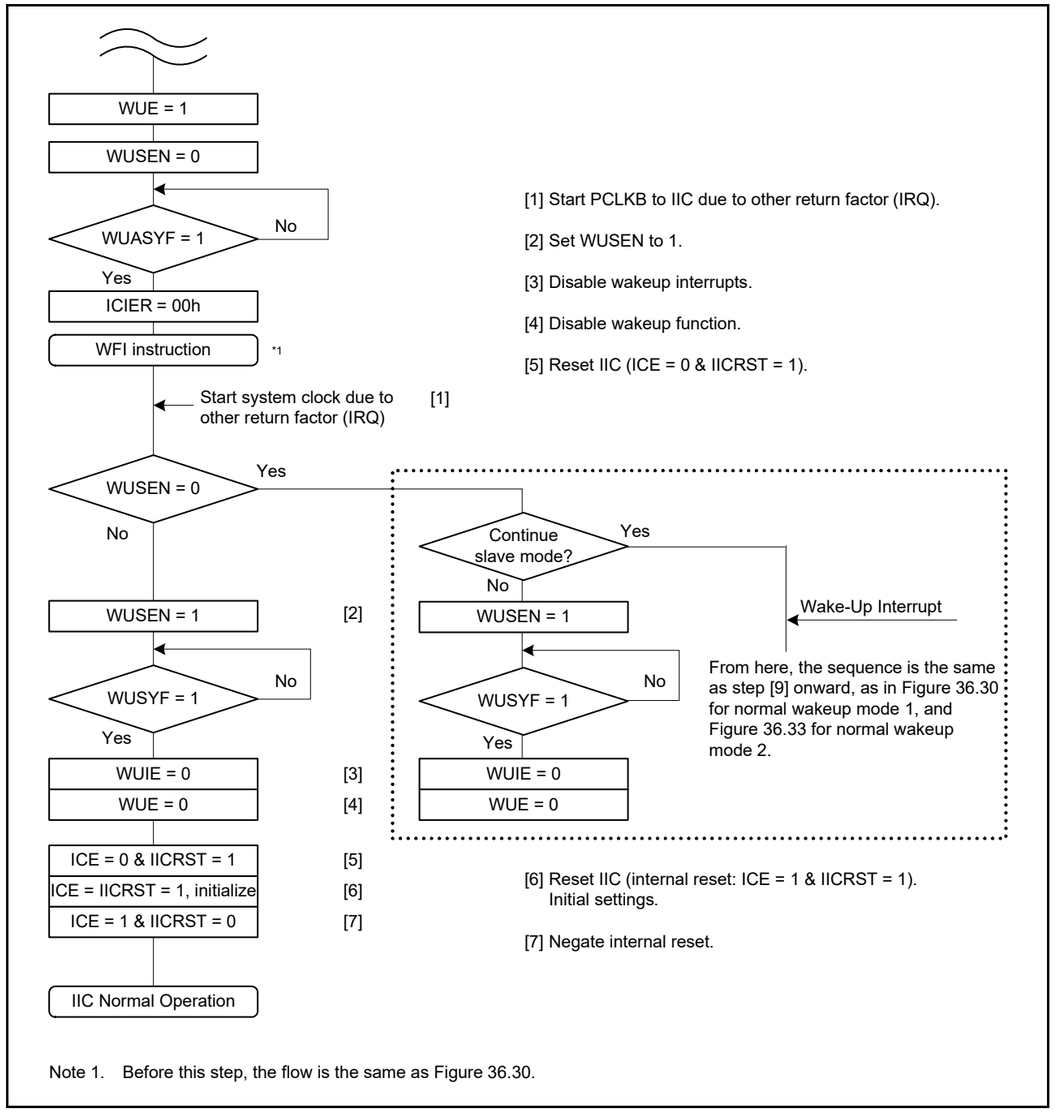
Note: See Precautions on the use of the wakeup function.



Note 1. 不要在BBSY=0和执行WFI指令之间发出启动条件。

Figure 36.30 正常唤醒模式1的示例操作，当唤醒由从地址匹配时的唤醒中断触发时

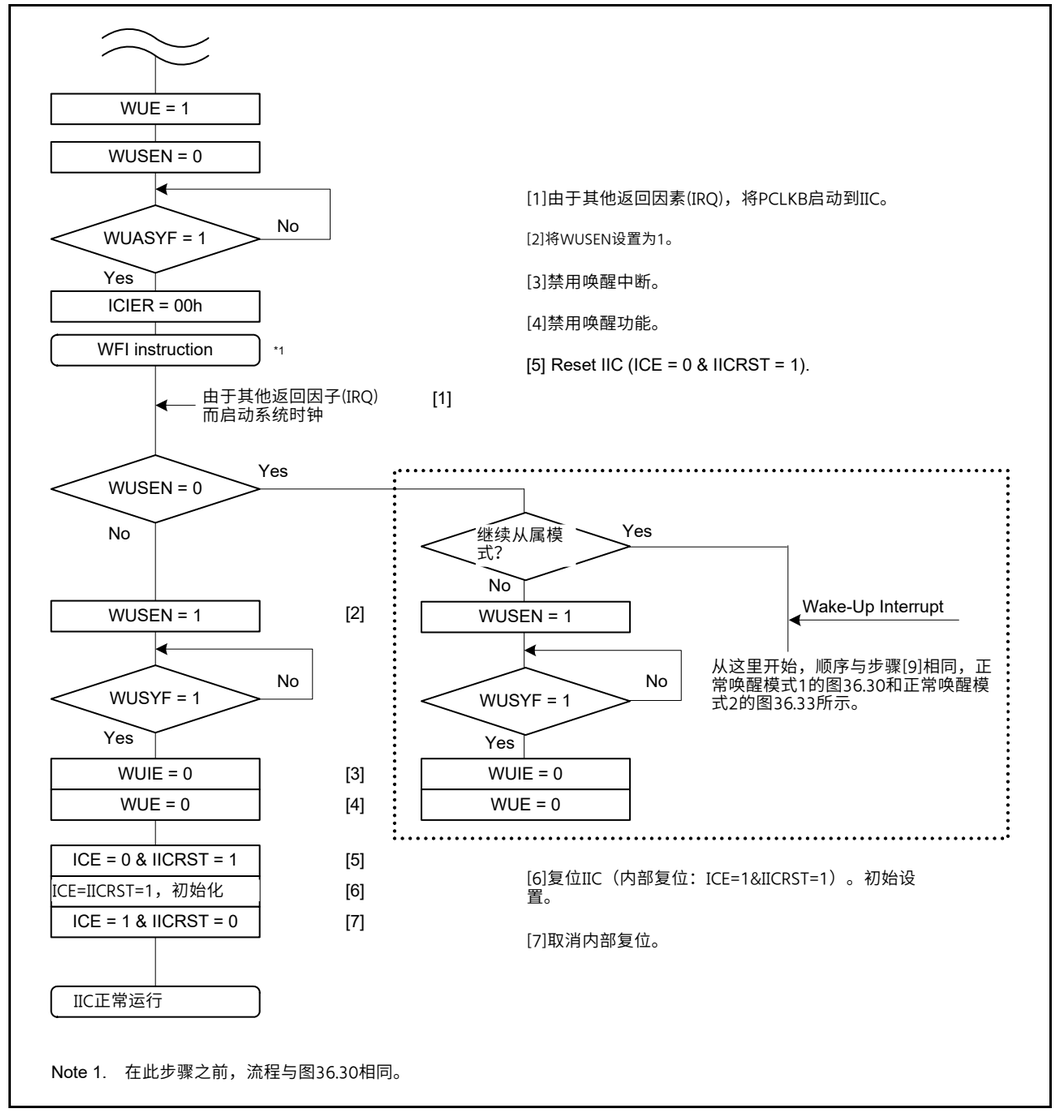
Note: 请参阅唤醒功能使用注意事项。



Note 1. Before this step, the flow is the same as Figure 36.30.

Figure 36.31 Example operation of normal wakeup modes 1 and 2 when wakeup is triggered by an interrupt other than IIC wakeup interrupt, for example IRQn

Note: For details on the IIC initial settings, see section 36.3.2, Initial Settings.



Note 1. 在此步骤之前，流程与图36.30相同。

Figure 36.31 当唤醒由IIC唤醒中断以外的中断（例如IRQn）触发时，正常唤醒模式1和2的示例操作

Note: 有关IIC初始设置的详细信息，请参阅第36.3.2节，初始设置。

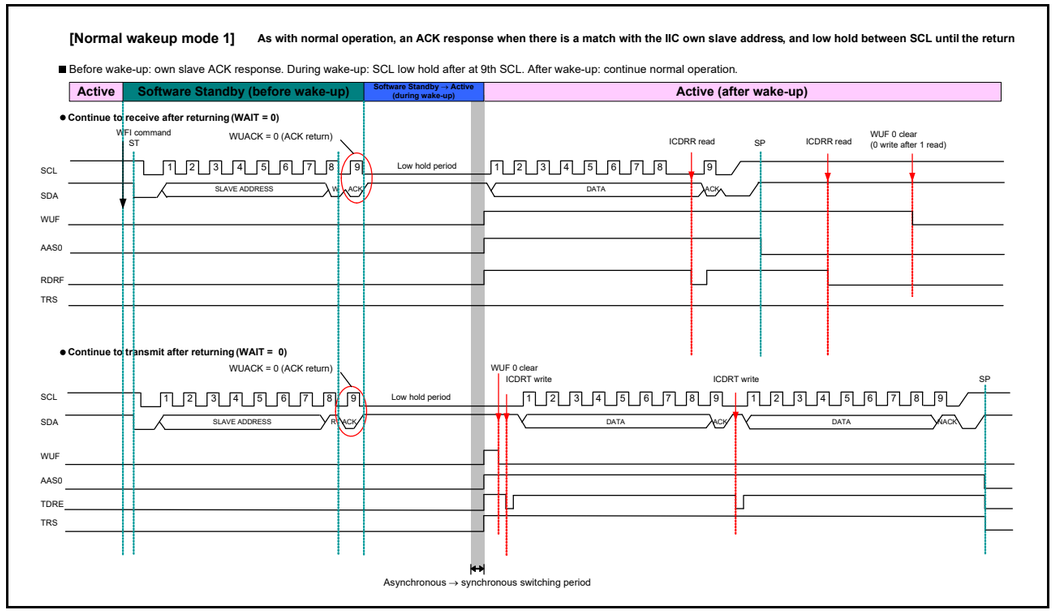


Figure 36.32 Timing of normal wakeup mode 1

36.8.2 Normal Wakeup Mode 2

This section describes the behavior, the timing, and an example operation of normal wakeup mode 2.

1. A wakeup interrupt triggered by a match of the slave address initiates the transition to normal operation as follows. Figure 36.34 provides detailed timing and Figure 36.33 shows an example operation.

   Before wakeup:No response to the data received with the own slave address of the IIC until the end of the eighth SCL cycle.

   During wakeup:SCL line held low during the eighth and ninth clock cycles.

   After wakeup:ACK returns on the ninth clock cycle of SCL, and normal operation continues.

   If the slave address does not match, the SCL line is not held low after the fall of the eighth SCL clock cycle. The slave operation continues.

2. If the transition from Software Standby mode is triggered by the interrupt (such as IRQn) other than a wakeup interrupt. WUF is not set in this case. Follow the processing shown in Figure 36.31.

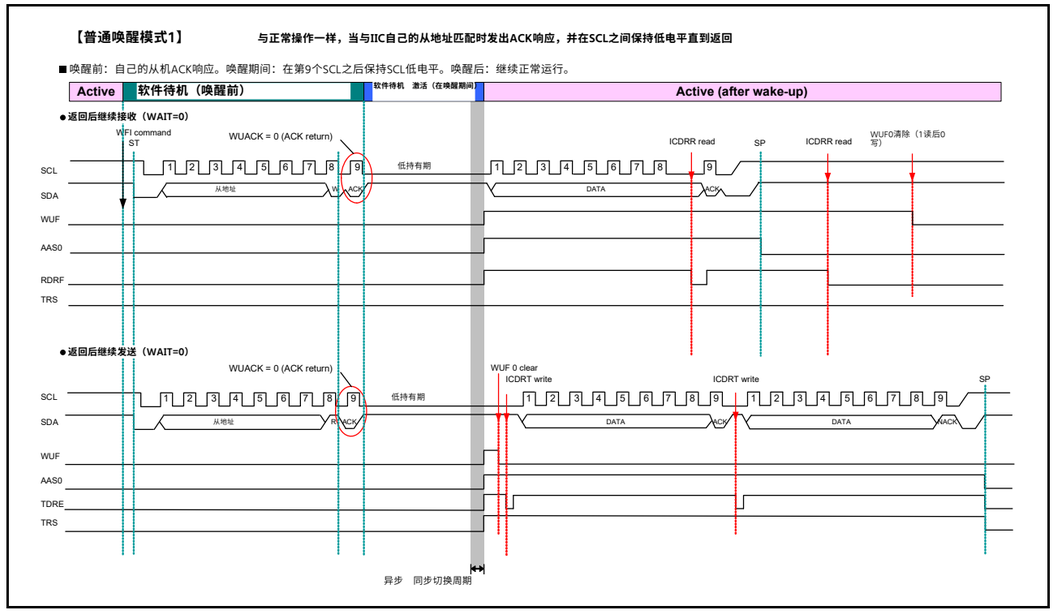


Figure 36.32 正常唤醒模式1的时序

36.8.2 正常唤醒模式2

本节介绍正常唤醒模式2的行为、时序和示例操作。

1. 由匹配的从地址触发的唤醒中断启动到正常操作的转换，如下所示。
   图36.34提供了详细的时序，图36.33显示了一个示例操作。

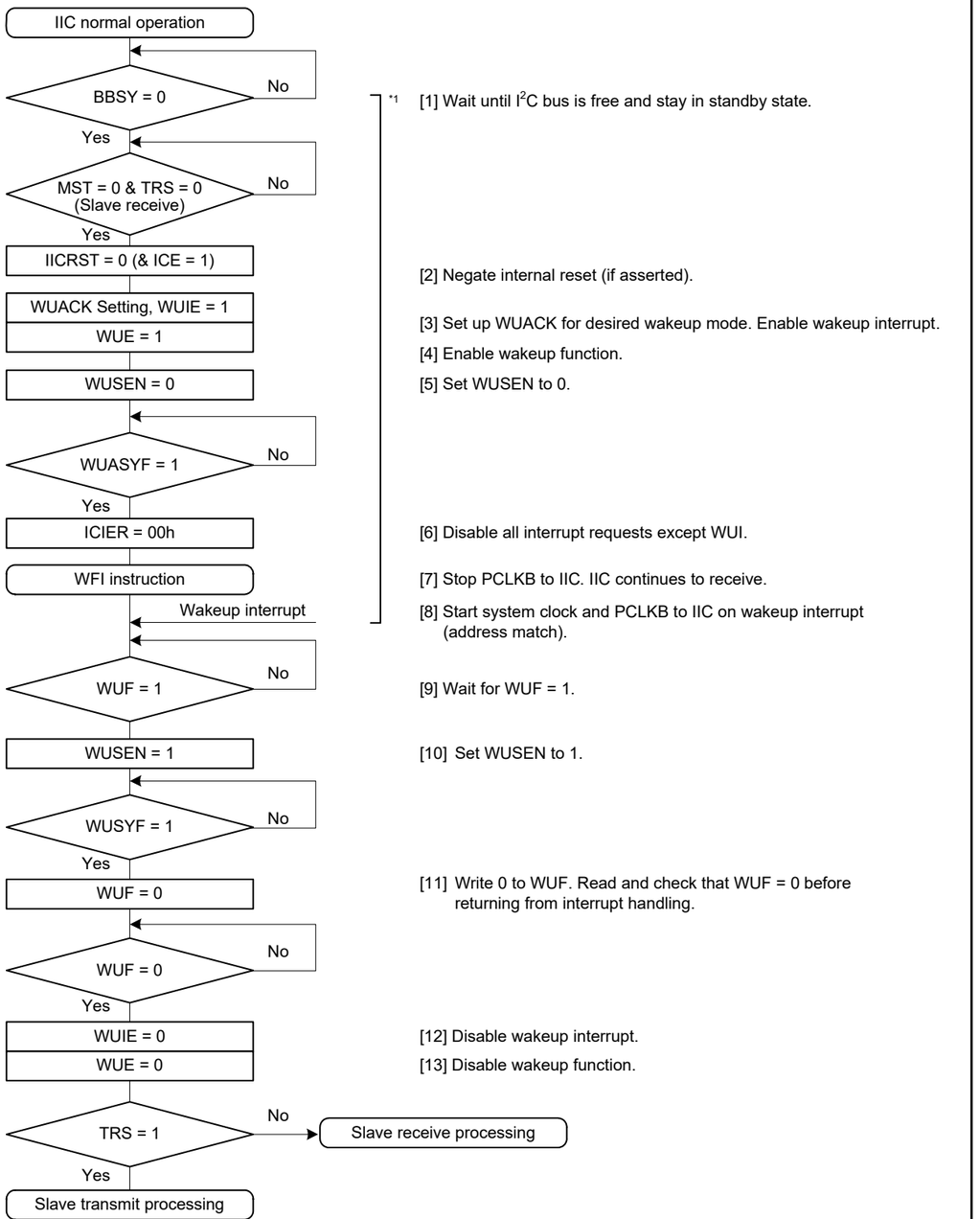
   唤醒前：直到第8个结束，才响应接收到的带有IIC自己从地址的数据SCL cycle.

   在唤醒期间：SCL线在第八和第九个时钟周期保持低电平。

   唤醒后：ACK在SCL的第9个时钟周期返回，继续正常运行。

   如果从机地址不匹配，则在第8个SCL时钟周期下降后，SCL线不会保持低电平。从操作继续。

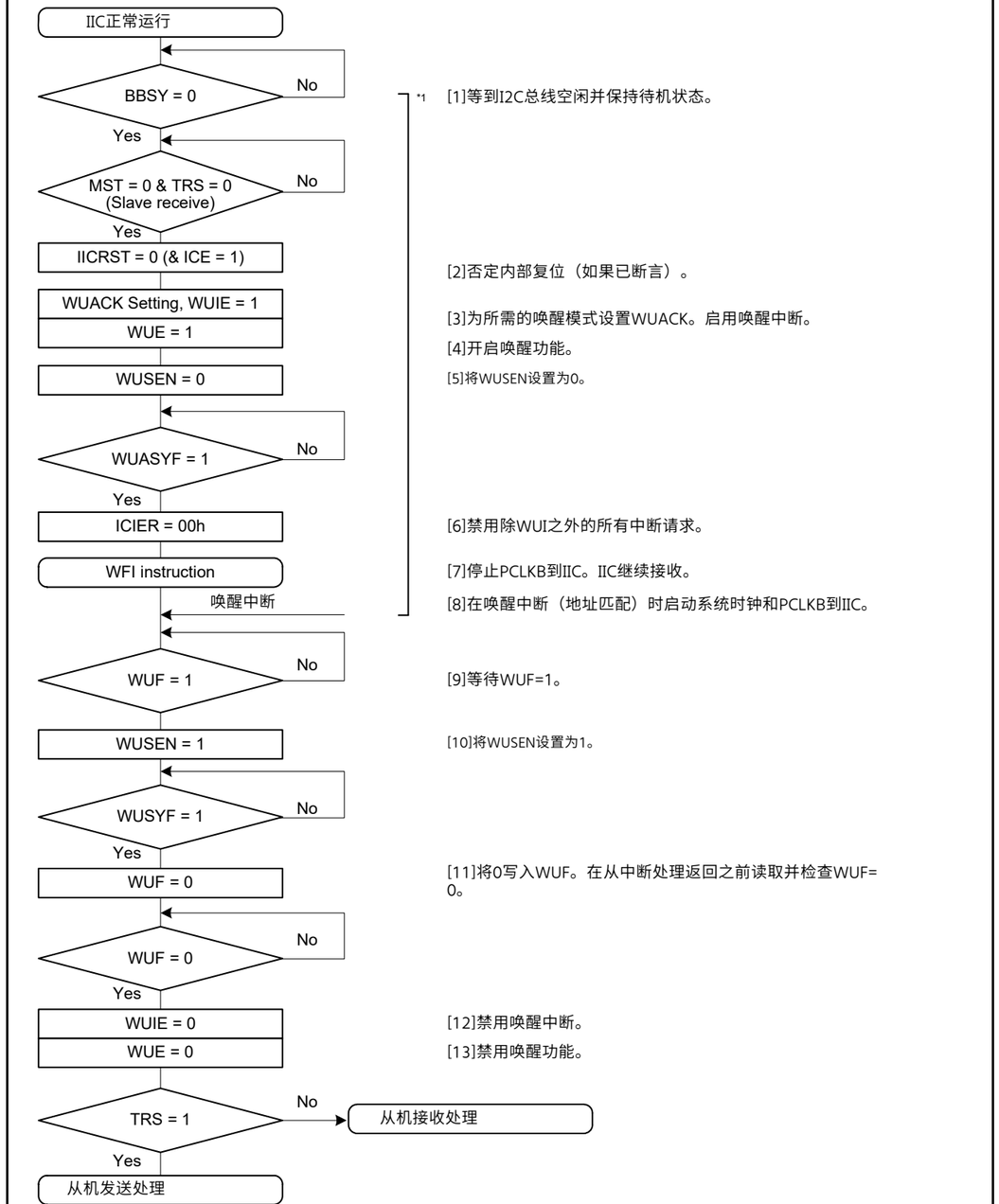
2. 如果从软件待机模式的转换是由唤醒中断以外的中断（例如IRQn）触发的。在这种情况下没有设置WUF。按照图36.31所示的处理。



Note 1. Do not issue start condition between BBSY = 0 and executing WFI instruction.

Figure 36.33 Example operation of normal wakeup mode 2 when wakeup is triggered by a wakeup interrupt on match of the slave address

Note: See Precautions on the use of the wakeup function.



Note 1. 不要在BBSY=0和执行WFI指令之间发出启动条件。

Figure 36.33 正常唤醒模式2的示例操作，当唤醒由从地址匹配时的唤醒中断触发时

Note: 请参阅唤醒功能使用注意事项。

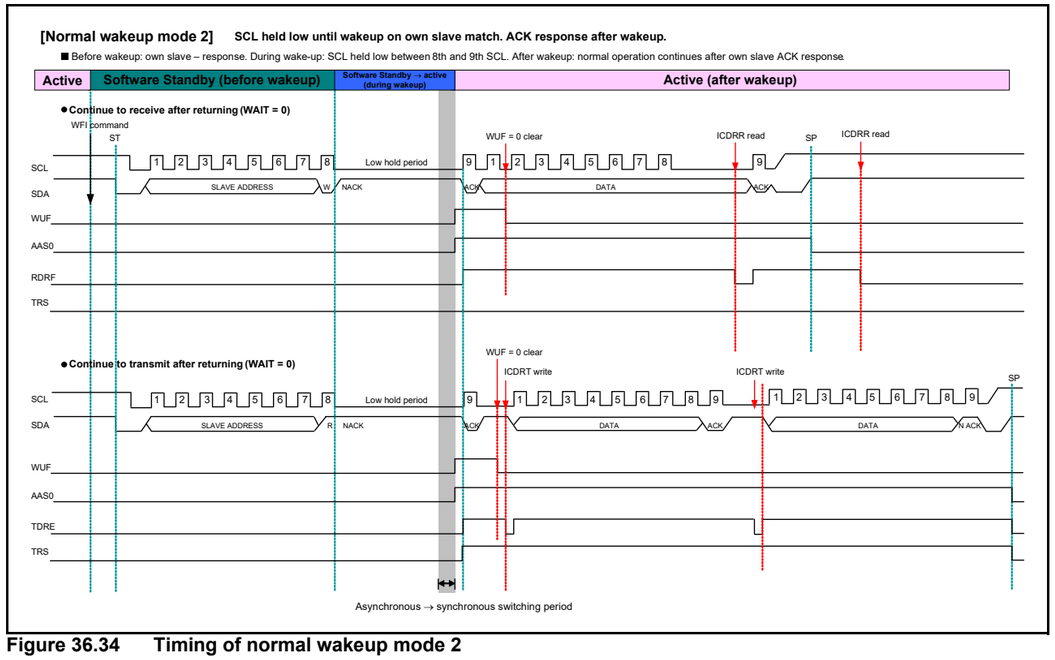


Figure 36.34 Timing of normal wakeup mode 2

36.8.3 Command Recovery Mode and EEP Response Mode (Special Wakeup Modes)

In the command recovery and EEP response modes, the SCL line is not held low during the wakeup period (after the rise of the ninth clock cycle of SCL), so other IIC devices can use the I2C bus during this period.

This section describes the behavior, the timing, and example operations of the command recovery and EEP response modes.

1. A wakeup interrupt triggered by a match of the slave address initiates the transition to normal operation as follows. Figure 36.37 provides detailed timing and Figure 36.35 shows an example operation.

   Before wakeup:In response to the data received with the own slave address of the IIC, ACK (command recovery mode) or NACK (EEP response mode) is returned.

   During wakeup:The SCL line is not held low.

   After wakeup:Normal operation continues after the IIC initial settings.

   If the slave address does not match, the slave operation continues.

Note 1. Because the SCL line is not held low during wakeup, transmission or reception of the data that follows the slave address is not possible.
Note 2. The command recovery and EEP response modes are internal reset states (ICE = IICRST = 1). Therefore, the match of the slave address does not set the ICSR1 flags, HOA, GCA, and ASS0,ASS1,ASS2.

2. If the transition from Software Standby mode is triggered by the interrupt (such as IRQn) other than a wakeup interrupt. WUF is not set in this case. Follow the processing shown in Figure 36.36.

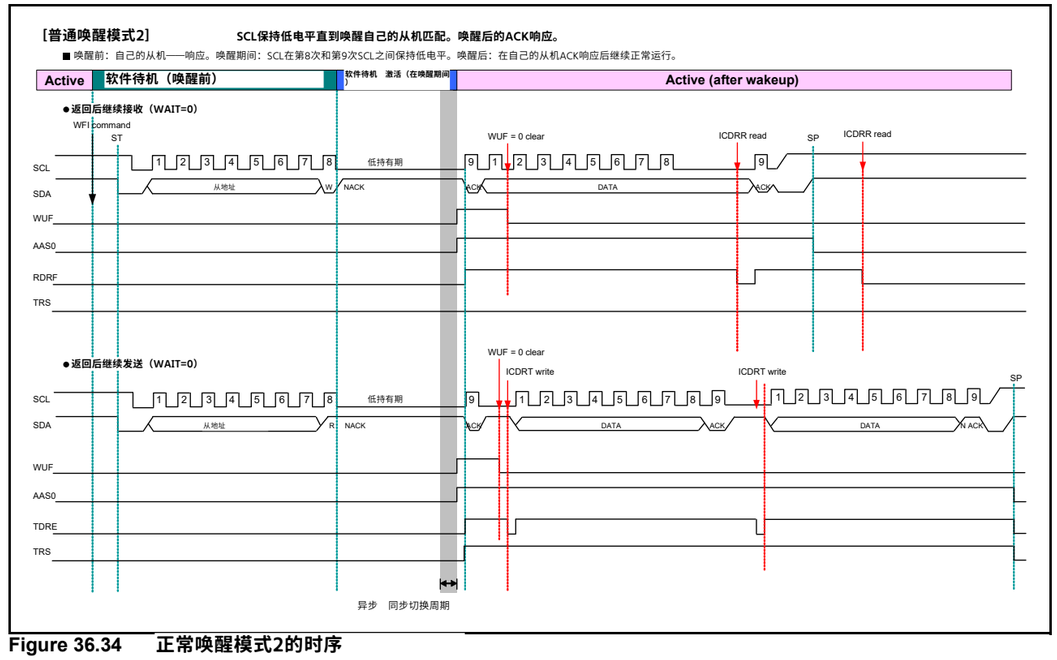


Figure 36.34 正常唤醒模式2的时序

36.8.3 命令恢复模式和EEP响应模式（特殊唤醒模式）

在命令恢复和EEP响应模式下，SCL线在唤醒期间（在SCL的第9个时钟周期上升后）不保持低电平，因此其他IIC设备可以在此期间使用I2C总线。

本节介绍命令恢复和EEP响应模式的行为、时序和示例操作。

1. 由匹配的从地址触发的唤醒中断启动到正常操作的转换，如下所示。
   图36.37提供了详细的时序，图36.35显示了一个示例操作。

   唤醒前：以IIC自己的从机地址接收到的数据，返回ACK（命令恢复模式）或NACK（EEP响应模式）。

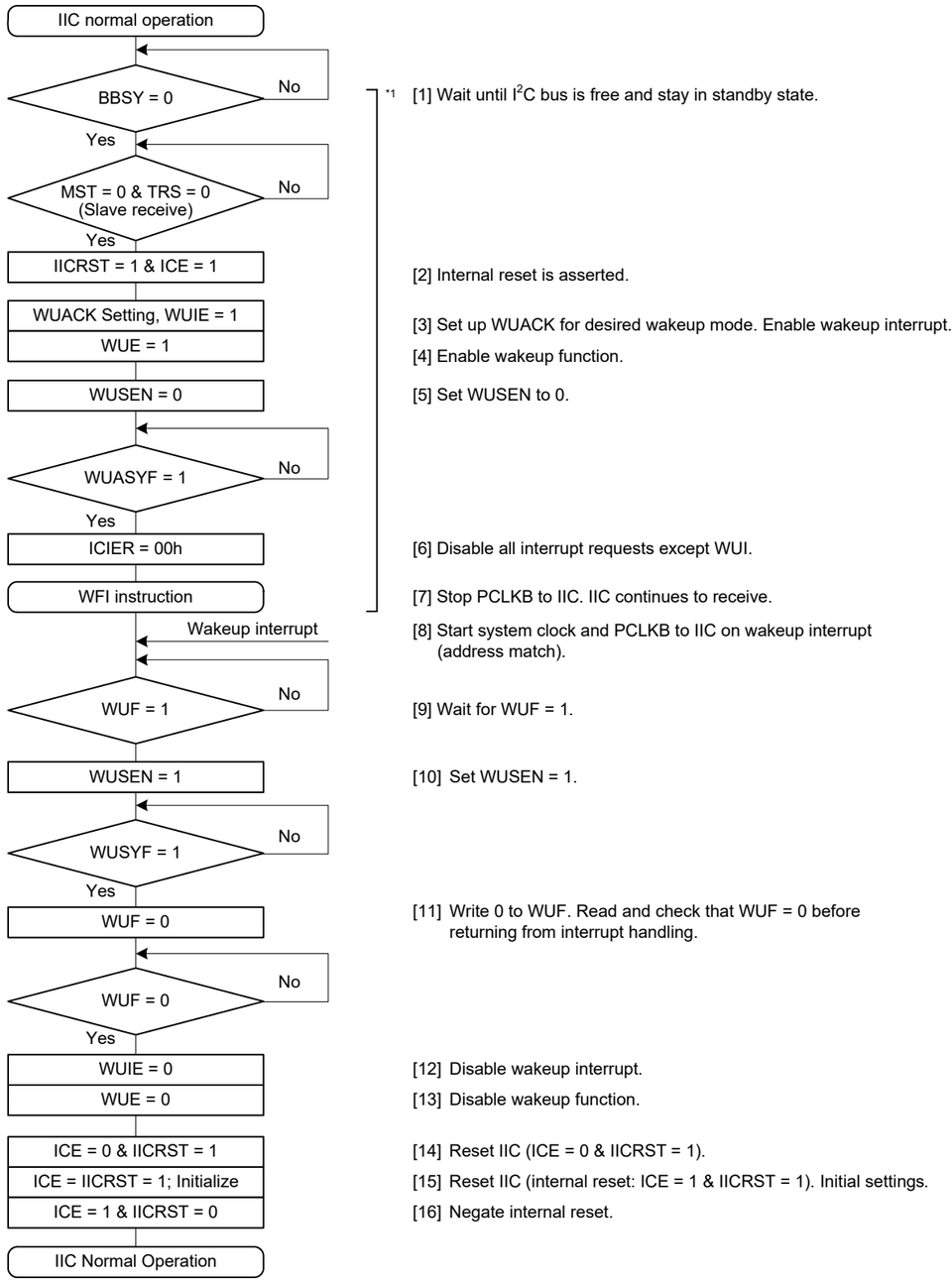
   唤醒期间：SCL线不保持低电平。

   唤醒后：IIC初始设置后继续正常运行。

   如果从机地址不匹配，从机操作继续。

注1.由于SCL线在唤醒期间未保持低电平，因此无法发送或接收跟随从地址的数据。注2.命令恢复和EEP响应模式是内部复位状态(ICE=IICRST=1)。因此，从地址的匹配不会设置ICSR1标志、HOA、GCA和ASS0、ASS1、ASS2。

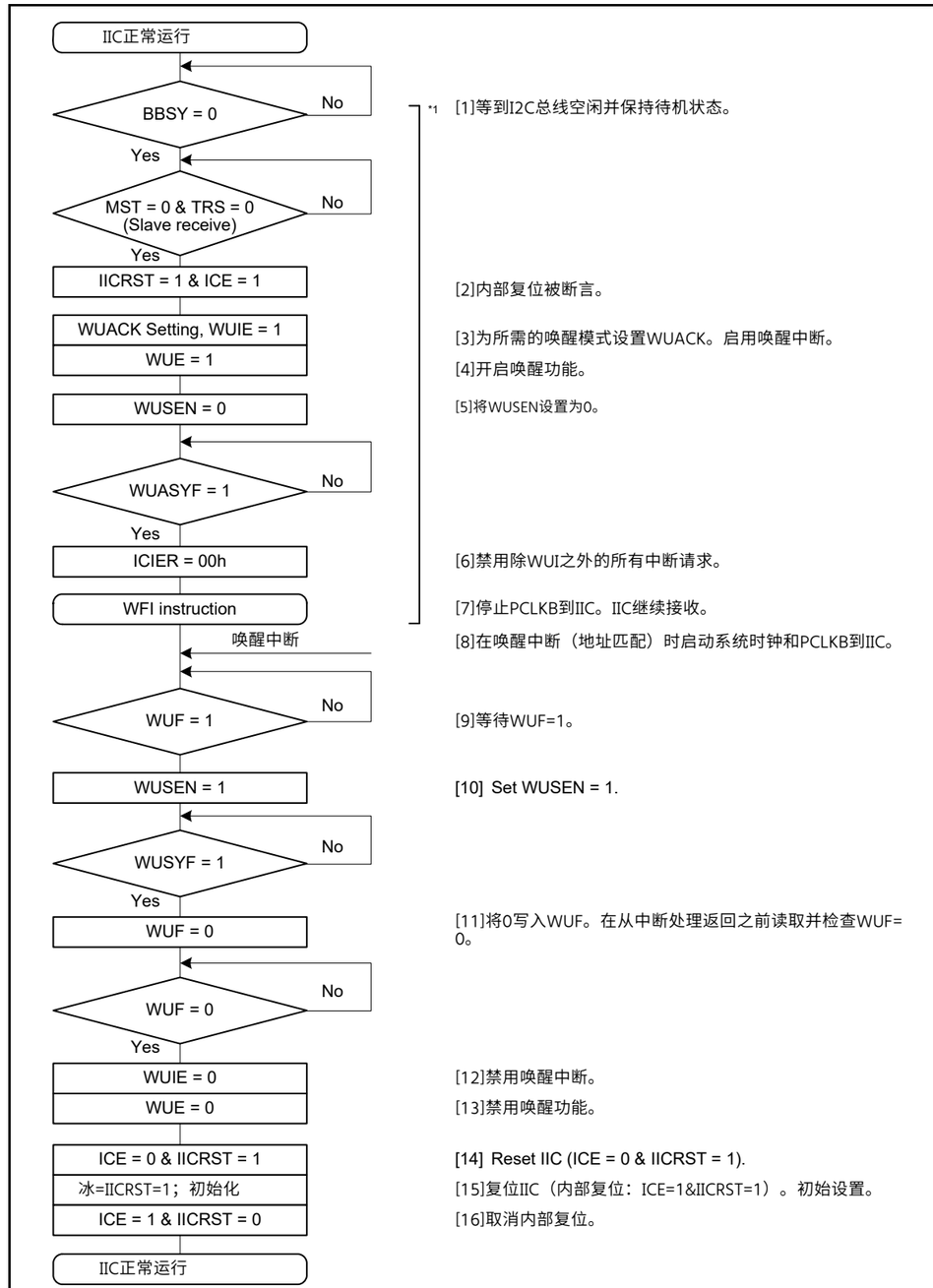
2. 如果从软件待机模式的转换是由唤醒中断以外的中断（例如IRQn）触发的。在这种情况下没有设置WUF。按照图36.36所示的处理。



Note 1. Do not issue start condition between BBSY = 0 and executing WFI instruction.

Figure 36.35 Example operation of command recovery mode and EEP response mode when wakeup is triggered by a wakeup interrupt on match of the slave address

Note: See Precautions on the use of the wakeup function.



Note 1. 不要在BBSY=0和执行WFI指令之间发出启动条件。

Figure 36.35 从地址匹配时唤醒中断触发唤醒时命令恢复模式和EEP响应模式的示例操作

Note: 请参阅唤醒功能使用注意事项。

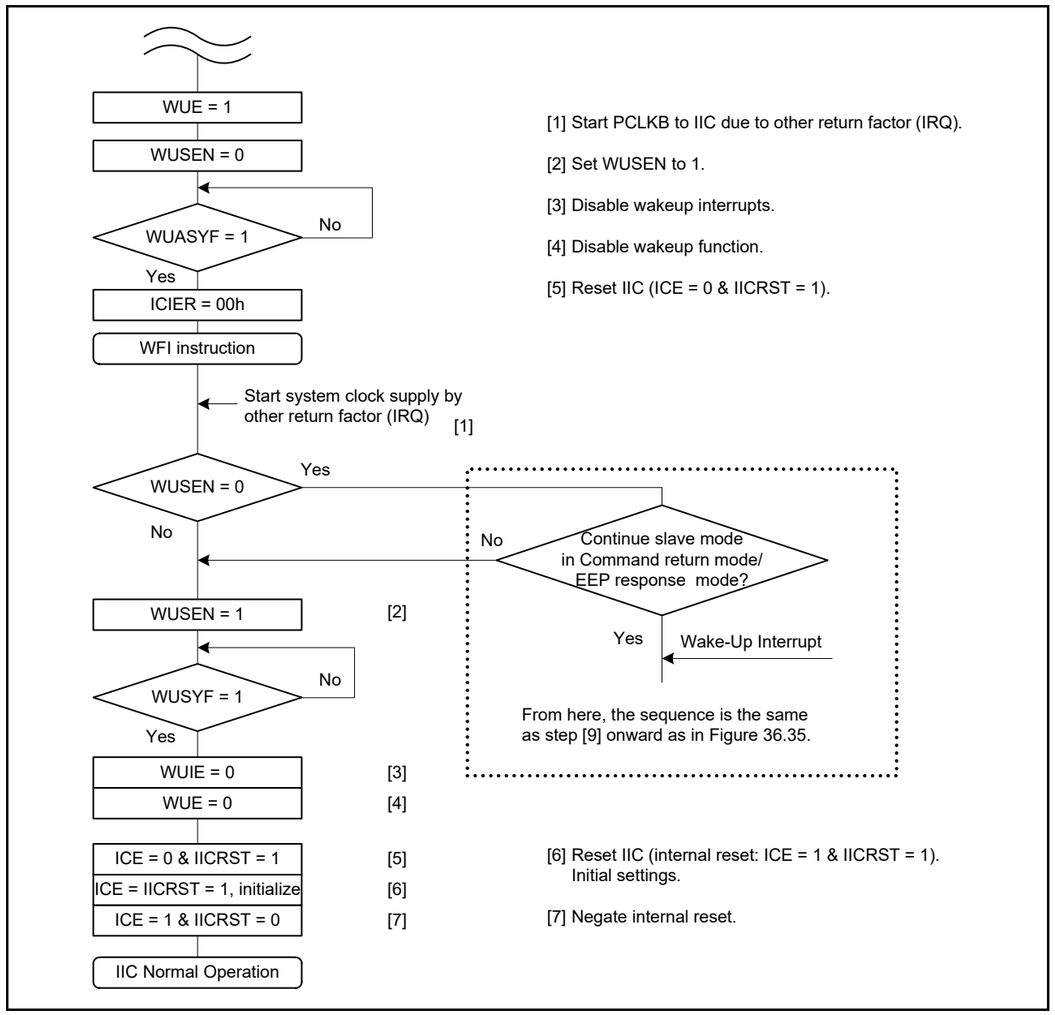


Figure 36.36 Example operation of command recovery mode and EEP response mode when wakeup is triggered by an interrupt other than IIC wakeup interrupt, for example IRQn

Note: For details on the IIC initial settings, see section 36.3.2, Initial Settings.

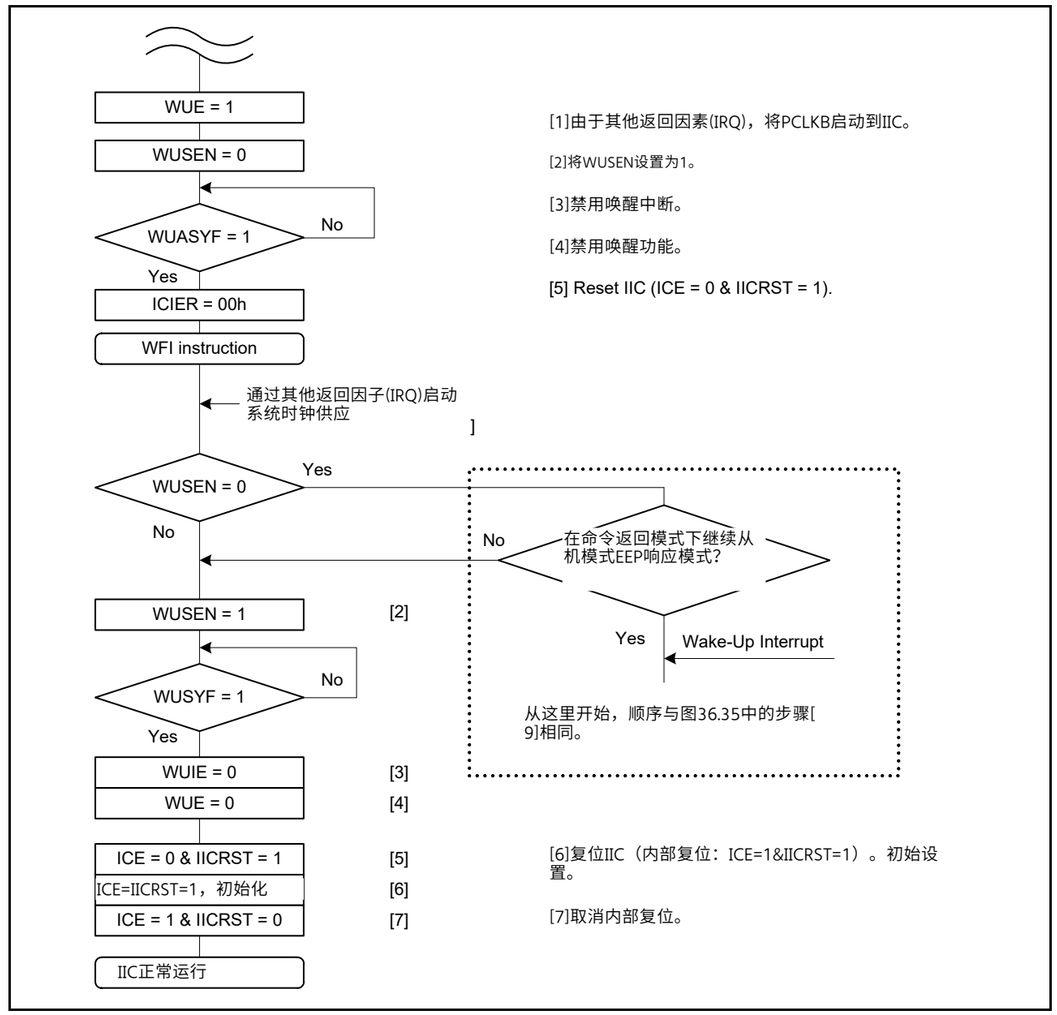


Figure 36.36 由IIC唤醒中断以外的中断（例如IRQn）触发唤醒时的命令恢复模式和EEP响应模式的示例操作

Note: 有关IIC初始设置的详细信息，请参阅第36.3.2节，初始设置。

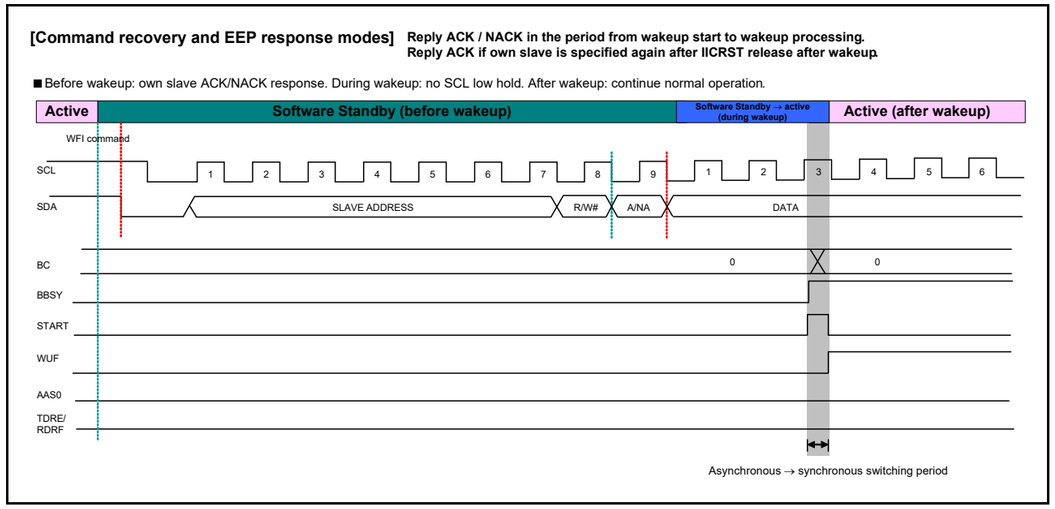


Figure 36.37 Timing of command recovery and EEP response modes

36.8.4 Precautions for WFI instruction Execution

In the example operations for the wakeup mode shown in Figure 36.30, Figure 36.33, and Figure 36.35, make sure that the start condition is not issued during the period from the setting of BBSY = 0 to the execution of the WFI instruction. When a start condition is issued during this period, NACK is returned after the reception of the first byte of the first data block. Then the detection of the start or restart condition enables the wakeup function.

36.9 Automatic Low-Hold Function for SCL

36.9.1 Function to Prevent Wrong Transmission of Transmit Data

If the I2C Bus Shift Register (ICDRS) is empty and data has not been written to the IIC-Bus Transmit Data Register (ICDRT) with the IIC in transmission mode (TRS bit = 1 in ICCR2), the SCLn line is automatically held low over the subsequent intervals. This low-hold period is extended until the transmit data is written, which prevents the unintended transmission of erroneous data.

Master transmit mode

- Low-level interval after a start or restart condition is issued
- Low-level interval between the ninth clock cycle of one transfer and the first clock cycle of the next.

Slave transmit mode

- Low-level interval between the ninth clock cycle of one transfer and the first clock cycle of the next.

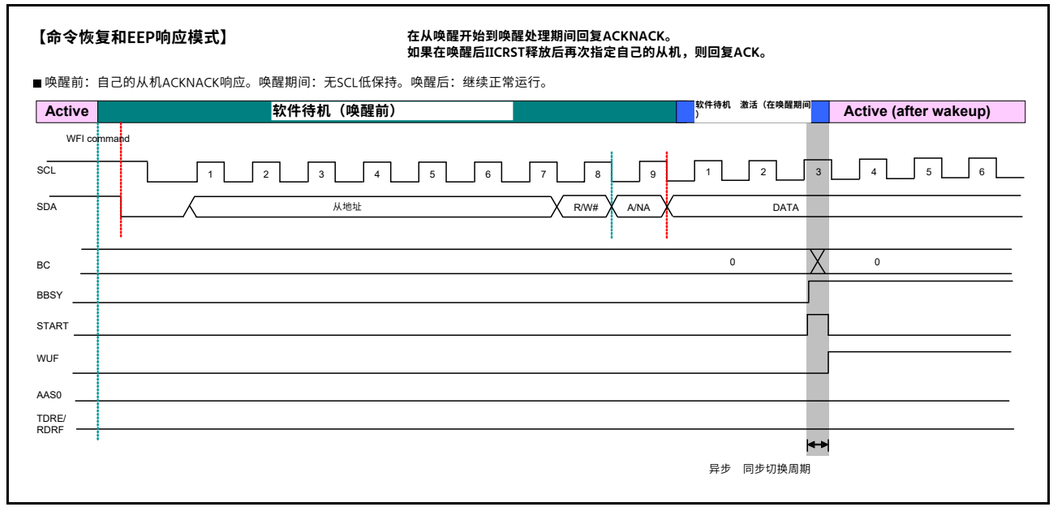


Figure 36.37 命令恢复和EEP响应模式的时序

36.8.4 WFI指令执行注意事项

在图36.30、图36.33和图36.35所示的唤醒模式的示例操作中，请确保从设置BBSY=0到执行WFI指令期间不发出启动条件。如果在此期间发出启动条件，则在接收到第一个数据块的第一个字节后返回NACK。然后检测到启动或重新启动条件启用唤醒功能。

36.9 SCL的自动低保持功能

36.9.1 防止传输数据错误传输的功能

如果I2C总线移位寄存器(ICDRS)为空且数据尚未写入IIC总线发送数据寄存器(ICDRT)且IIC处于传输模式（TRS位=ICCR2中的1），则SCLn线自动在随后的时间间隔内保持低位。这个低保持期一直延长到发送数据被写入，这样可以防止错误数据的意外传输。

主传输模式

- 发出启动或重启条件后的低电平间隔
- 一次传输的第9个时钟周期和下一次传输的第一个时钟周期之间的低电平间隔。

从机发送模式

- 一次传输的第9个时钟周期和下一次传输的第一个时钟周期之间的低电平间隔。

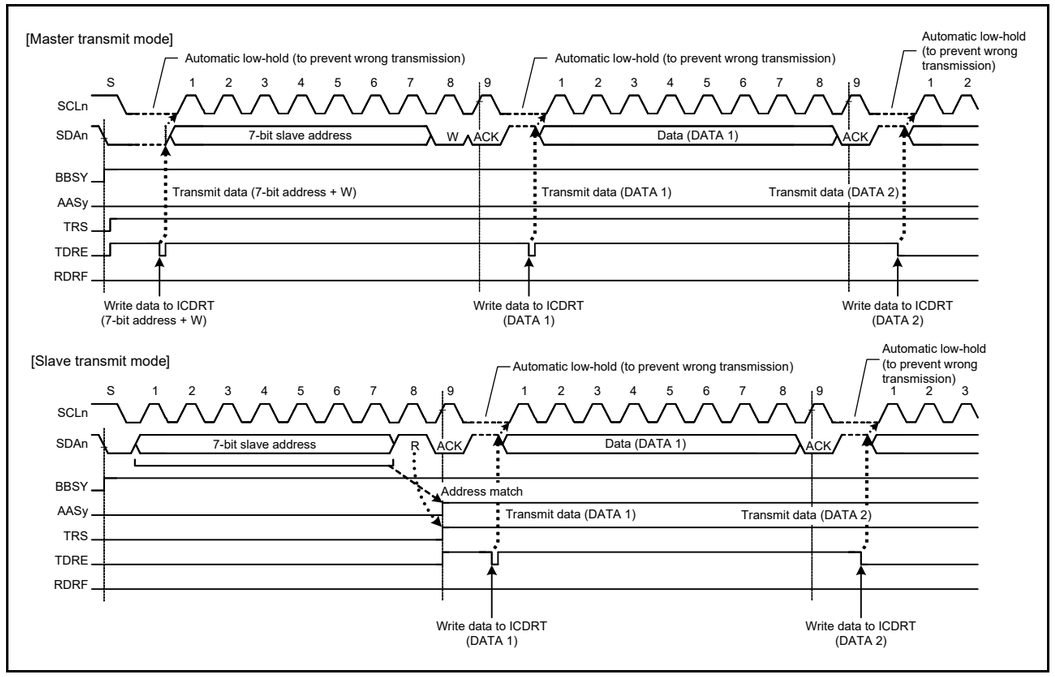


Figure 36.38 Automatic low-hold operation in transmit mode

36.9.2 NACK Reception Transfer Suspension Function

This function suspends transfer operation when NACK is received in transmit mode (TRS bit = 1 in ICCR2). It is enabled when the NACKE bit in ICFER is set to 1. If the next transmit data is already written (TDRE flag = 0 in ICSR2) when NACK is received, the next data transmission on the falling edge of the ninth SCL clock cycle is automatically suspended. This prevents the SDAn line output level from being held low when the MSB of the next transmit data is 0.

If the transfer operation is suspended by this function (NACKF flag = 1 in ICSR2), transmit and receive operations are discontinued. To restore transmit or receive operation, you must set the NACKF flag to 0. In master transmit mode, after issue a restart or stop condition, set the NACKF flag to 0, and then issue a start condition again.

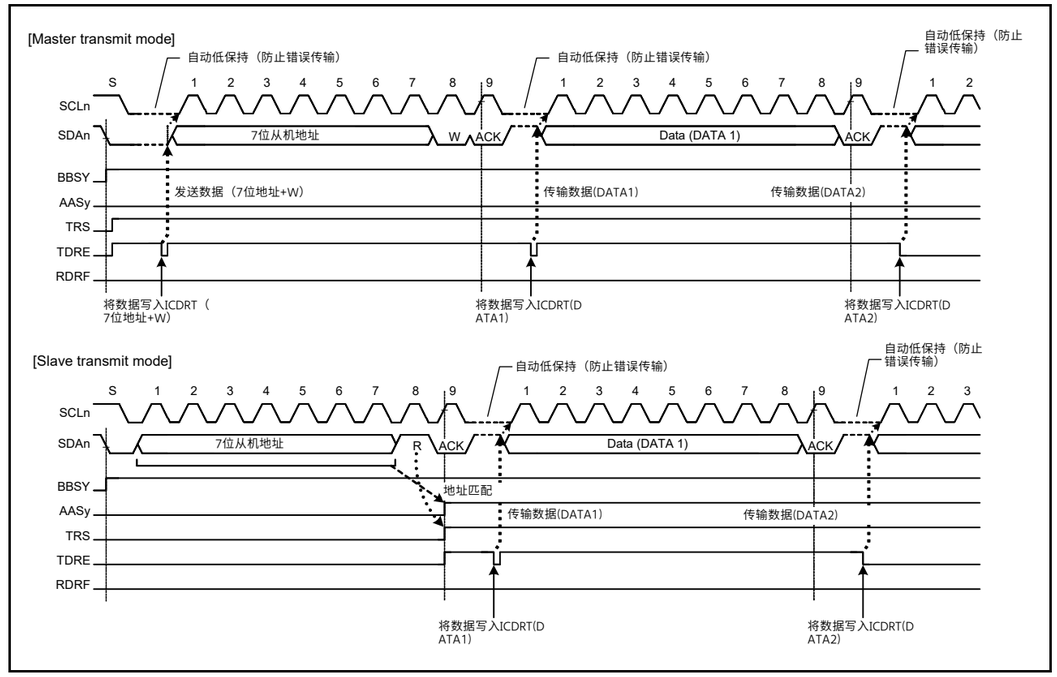


Figure 36.38 发送模式下的自动低保持操作

36.9.2 NACK接收传输暂停功能

当在发送模式下接收到NACK（ICCR2中的TRS位=1）时，该函数暂停传输操作。当ICFER中的NACKE位设置为1时使能。如果在接收到NACK时已经写入下一个发送数据（ICSR2中的TDRE标志=0），则在第9个SCL时钟周期的下降沿进行下一个数据传输自动暂停。这可以防止SDAn线路输出电平在下一个发送数据的MSB为0时保持低电平。

如果传输操作被该函数挂起（ICSR2中的NACKF标志=1），发送和接收操作将中断。要恢复发送或接收操作，必须将NACKF标志设置为0。在主机发送模式下，发出重启或停止条件后，将NACKF标志设置为0，然后再次发出启动条件。

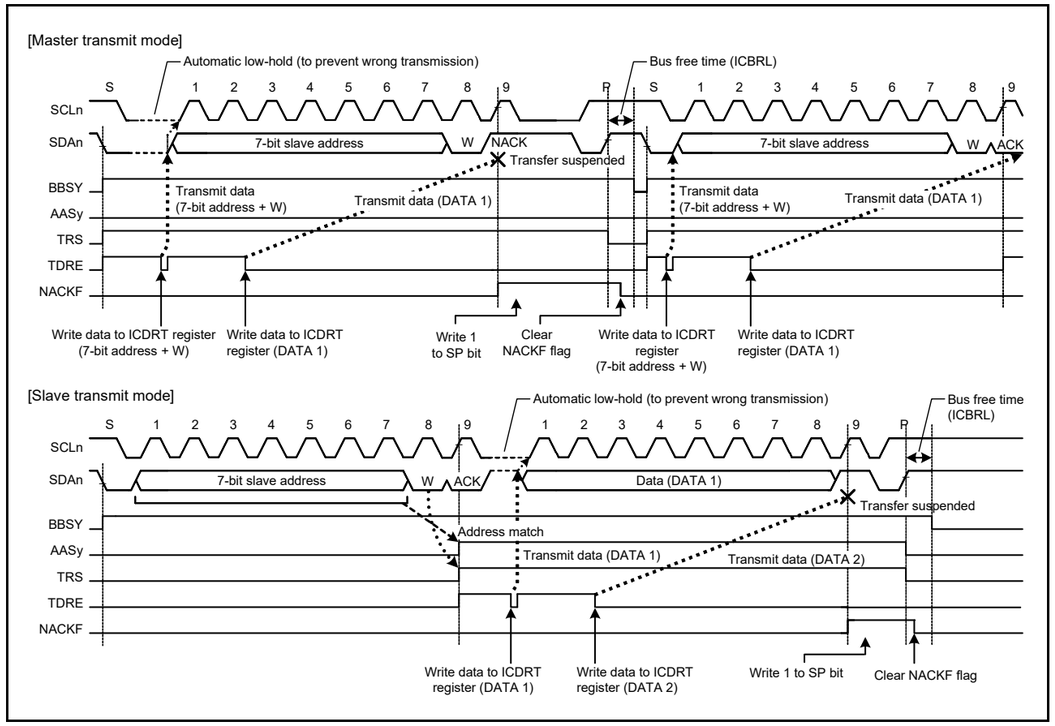


Figure 36.39 Suspension of data transfer when NACK is received, when NACKE = 1

36.9.3 Function to Prevent Failure to Receive Data

If response processing is delayed when receive data (ICDRR) read is delayed for a period of one transfer frame or more with receive data full (RDRF flag = 1 in ICSR2) in receive mode (TRS = 0 in ICCR2), the IIC holds the SCLn line low automatically immediately before the next data is received to prevent a failure to receive data.

This function is enabled even if the read processing of the final receive data is delayed and, in the meantime, the IIC slave address is designated after a stop condition is issued. This function does not interfere with other communication because the IIC does not hold the SCLn line low when a mismatch with its own slave address occurs after a stop condition is issued.

Periods in which the SCLn line is held low can be selected with a combination of the WAIT and RDRFS bits in ICMR3.

(1) 1-byte receive operation and automatic low-hold function using the WAIT bit

When the WAIT bit in ICMR3 is set to 1, the IIC performs a 1-byte receive operation using the WAIT bit function. Additionally, when the ICMR3.RDRFS bit is 0, the IIC automatically sends the ACKBT bit value in ICMR3 for the acknowledge bit in the period from the falling edge of the eighth SCL clock cycle to the falling edge of the ninth SCL clock cycle, and automatically holds the SCLn line low on the falling edge of the ninth SCL clock cycle using the WAIT bit function. This low-hold is released by reading data from ICDRR, which enables byte-wise receive operation.

The WAIT bit function is enabled for receive frames after a match with the IIC slave address, including the general call address and host address, is obtained in master or slave receive mode.

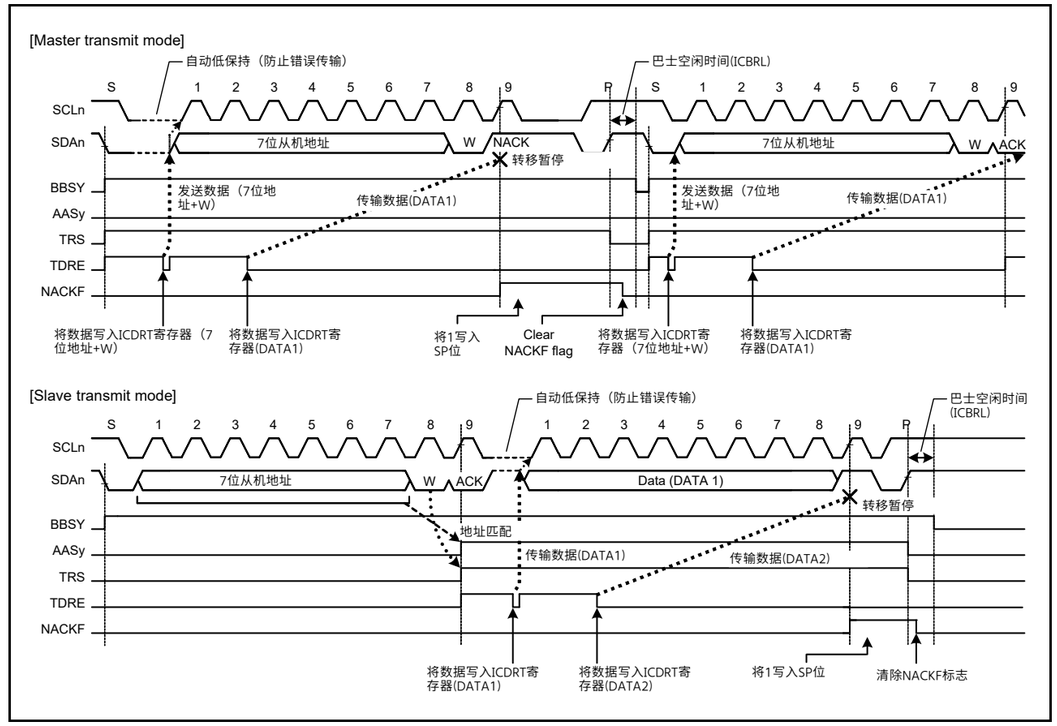


Figure 36.39 接收到NACK时暂停数据传输，当NACKE=1

36.9.3 防止数据接收失败的功能

如果在接收模式（ICCR2中的TRS=0）下接收数据（ICDRR）读取延迟一个传输帧或更长时间且接收数据已满（ICSR2中的RDRF标志=1）时响应处理延迟，则IIC保持在接收到下一个数据之前，SCLn线自动变为低电平，以防止接收数据失败。

即使最终接收数据的读取处理延迟，该功能也有效，同时，在发出停止条件后指定IIC从机地址。此功能不会干扰其他通信，因为在发出停止条件后发生与其自己的从地址不匹配时，IIC不会将SCLn线保持为低电平。

SCLn线保持低电平的周期可以通过ICMR3中的WAIT和RDRFS位的组合来选择。

(1) 使用WAIT位的1字节接收操作和自动低保持功能

当ICMR3中的WAIT位设置为1时，IIC使用WAIT位功能执行1字节接收操作。此外，当ICMR3.RDRFS位为0时，IIC会在第8个SCL时钟周期的下降沿到第9个SCL时钟周期的下降沿期间自动发送ICMR3中的ACKBT位值作为确认位，并且使用WAIT位功能在第9个SCL时钟周期的下降沿自动将SCLn线保持为低电平。该低保持通过从ICDRR读取数据来释放，从而启用逐字节接收操作。

在主机或从机接收模式下获得与IIC从机地址（包括广播地址和主机地址）匹配后的接收帧启用WAIT位功能。

(2) 1-byte receive operation (ACK/NACK transmission control) and automatic low-hold function using the RDRFS bit

When the RDRFS bit in ICMR3 is set to 1, the IIC performs a 1-byte receive operation using the RDRFS bit function. When the RDRFS bit is set to 1, the RDRF flag in ICSR2 is set to 1 (receive data full) on the rising edge of the eighth SCL clock cycle, and the SCLn line is automatically held low on the falling edge of the eighth SCL clock cycle. This low-hold is released by writing a value to the ACKBT bit in ICMR3, but cannot be released by reading data from ICDRR, which enables receive operation through the ACK or NACK transmission control based on the data received in byte units.

The RDRFS bit function is enabled for receive frames after a match with the IIC slave address, including the general call address and host address, is obtained in master or slave receive mode.

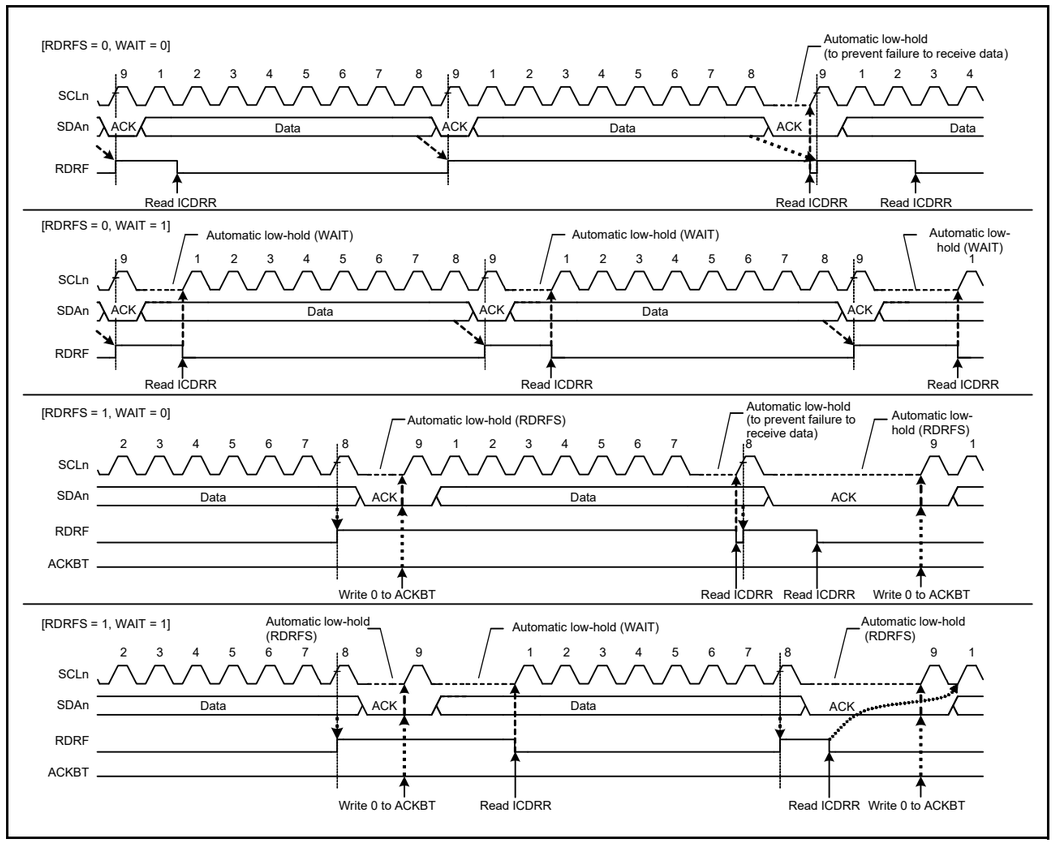


Figure 36.40 Automatic low-hold operation in receive mode using the RDRFS and WAIT bits

(2) 1字节接收操作（ACKNACK传输控制）和使用RDRFS位的自动低保持功能

当ICMR3中的RDRFS位设置为1时，IIC使用RDRFS位功能执行1字节接收操作。当RDRFS位为1时，ICSR2中的RDRF标志位在第8个SCL时钟周期的上升沿置1（接收数据满），并且SCLn线在第8个SCL的下降沿自动保持为低时钟周期。该低保持通过向ICMR3中的ACKBT位写入值来释放，但不能通过从ICDRR读取数据来释放，ICDRR可以根据以字节为单位接收的数据通过ACK或NACK传输控制进行接收操作。

在主机或从机接收模式下获得与IIC从机地址（包括广播地址和主机地址）匹配后的接收帧启用RDRFS位功能。

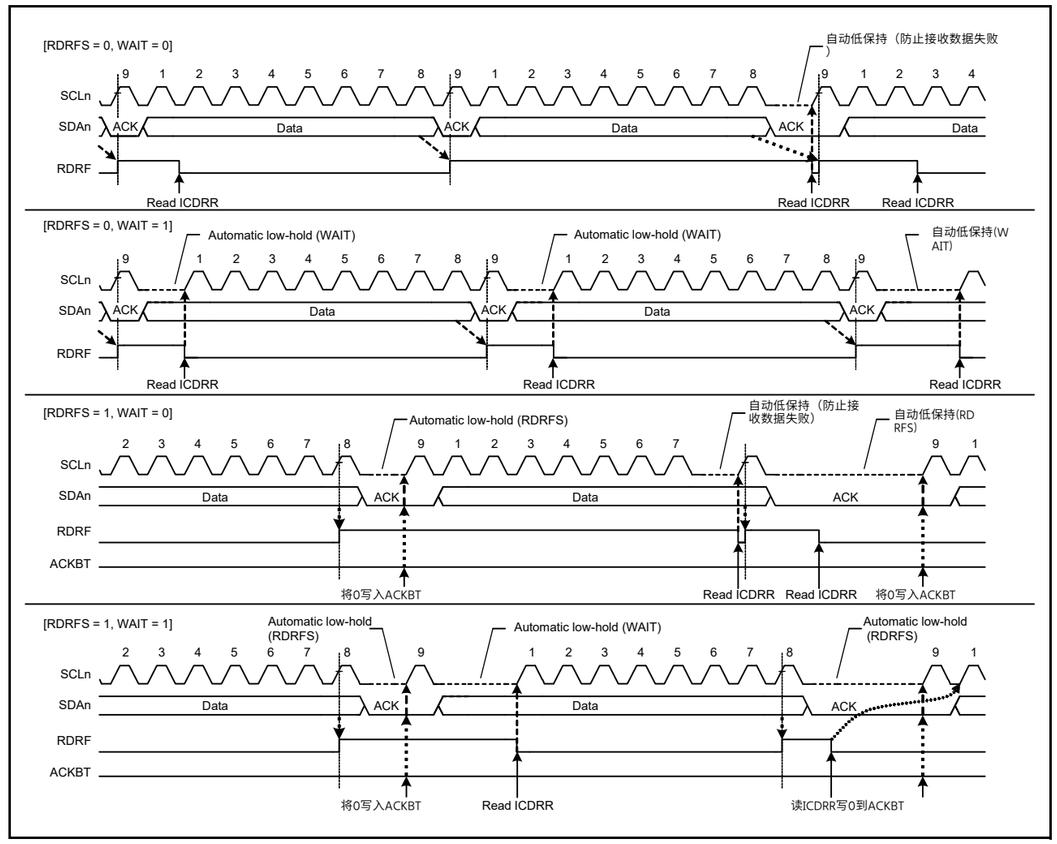


Figure 36.40 使用RDRFS和WAIT位在接收模式下自动保持低电平操作

36.10 Arbitration-Lost Detection Functions

In addition to the normal arbitration-lost detection function defined by the I2C bus standard, the IIC provides functions to prevent double-issue of a start condition, detect arbitration-lost during transmission of NACK, and detect arbitration-lost in slave transmit mode.

36.10.1 Master Arbitration-Lost Detection (MALE Bit)

The IIC drives the SDAn line low to issue a start condition. However, if the SDAn line was already driven low by another master device issuing a start condition, the IIC regards its own start condition as an error and considers this a loss in arbitration. Priority is given to transfer by the other master device. Similarly, if a request to issue a start condition is made by setting the ST bit in ICCR2 to 1 while the bus is busy (BBSY flag = 1 in ICCR2), the IIC regards this as a double-issuing-of-start-condition error and considers itself to have lost in arbitration. This prevents a failure of transfer resulting from a start condition being issued while transfer is in progress.

When a start condition is issued successfully, if the transmit data including the address bits (internal SDA output level) and the level on the SDAn line do not match (high output as the internal SDA output, meaning the SDAn pin is in the high-impedance state) and a low level is detected on the SDAn line, the IIC loses in arbitration.

After a loss in arbitration of mastership, the IIC immediately enters slave receive mode. If a slave address, including the general call address, matches its own address at this time, the IIC continues in slave operation.

A loss in arbitration of mastership is detected when the following conditions are met while the MALE bit in ICFER is 1 (master arbitration-lost detection enabled).

[Master arbitration-lost conditions]

- Non-matching of the internal level for output on SDA and the level on the SDAn line after a start condition was issued by setting the ST bit in ICCR2 to 1 while the BBSY flag in ICCR2 was set to 0 (erroneous issuing of a start condition)
- Setting of the ST bit in ICCR2 to 1 (start condition double-issue error) while the BBSY flag is 1
- When the transmit data excluding acknowledge (internal SDA output level) does not match the level on the SDAn line in master transmit mode (MST and TRS bits = 11b in ICCR2).

36.10 仲裁丢失检测功能

除了I2C总线标准定义的正常仲裁丢失检测功能外，IIC还提供防止重复发出启动条件、在NACK传输期间检测仲裁丢失以及在从机发送中检测仲裁丢失的功能模式。

36.10.1 主仲裁丢失检测（MALE位）

IIC将SDAn线驱动为低电平以发出启动条件。但是，如果SDAn线已经被另一个发出启动条件的主设备驱动为低电平，则IIC将其自己的启动条件视为错误，并认为这是仲裁失败。其他主设备优先传输。类似地，如果在总线繁忙时通过将ICCR2中的ST位设置为1来请求发出启动条件（ICCR2中的BBSY标志=1），则IIC将此视为双重发出启动条件错误并认为自己在仲裁中败诉。这可以防止由于在传输过程中发出启动条件而导致传输失败。

当启动条件成功发出时，如果发送数据包括地址位（内部SDA输出电平）与SDAn线上的电平不匹配（高输出作为内部SDA输出，意味着SDAn引脚处于高电平）阻抗状态）并且在SDAn线上检测到低电平，则IIC在仲裁中失败。

在主控权仲裁失败后，IIC立即进入从机接收模式。如果此时从机地址（包括广播地址）与自己的地址匹配，则IIC继续从机操作。

当ICFER中的MALE位为1（启用主仲裁丢失检测）时满足以下条件时，检测到主控仲裁丢失。

[Master arbitration-lost conditions]

- 通过将ICCR2中的ST位设置为1，同时ICCR2中的BBSY标志设置为0，发出启动条件后，SDA输出的内部电平与SDAn线上的电平不匹配（错误发出启动条件）
- 当BBSY标志为1时，将ICCR2中的ST位设置为1（启动条件双发错误）
- 当发送数据不包括确认（内部SDA输出电平）与主发送模式下SDAn线上的电平不匹配时（ICCR2中的MST和TRS位=11b）。

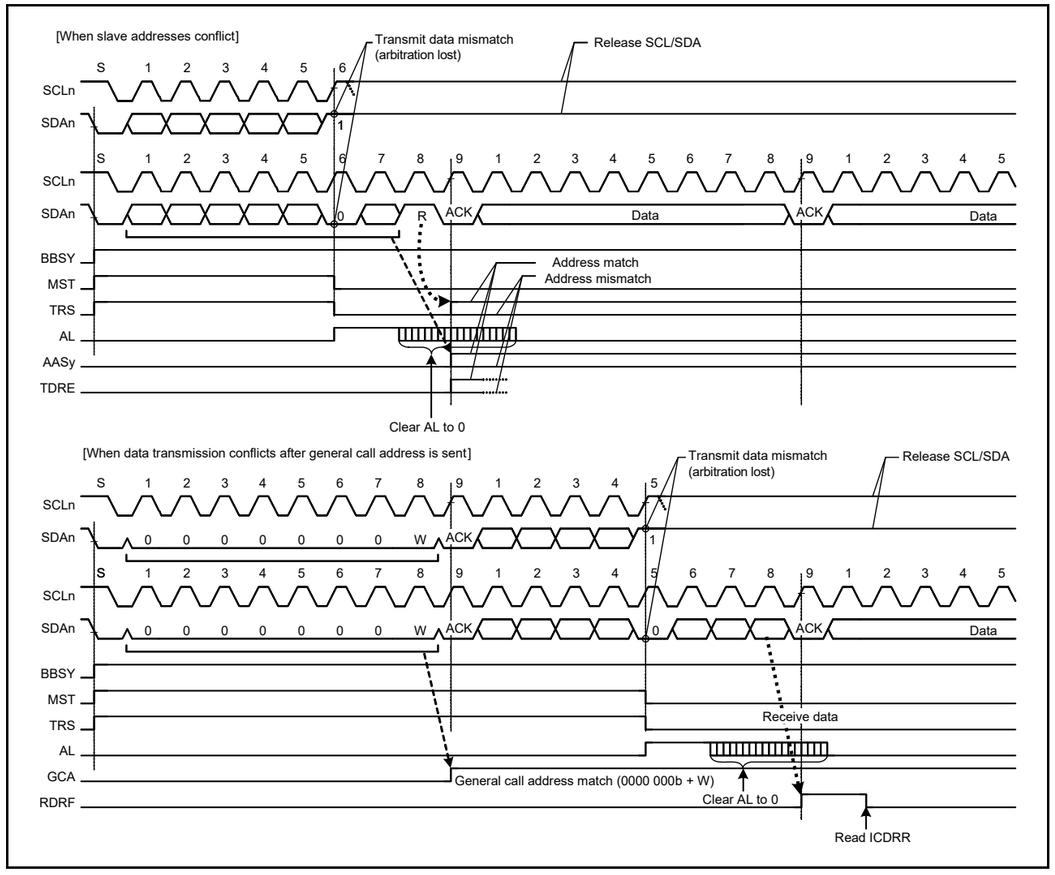


Figure 36.41 Examples of master arbitration-lost detection when MALE = 1

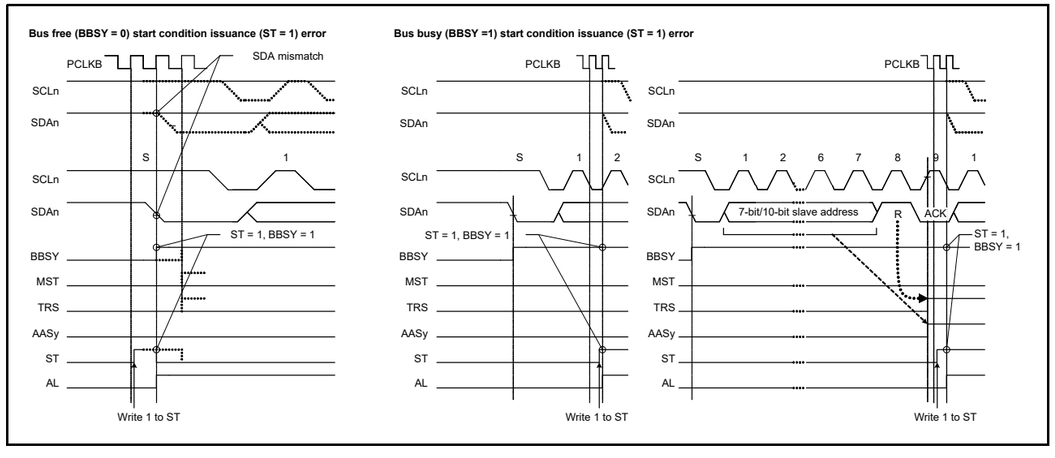


Figure 36.42 Arbitration-lost when start condition is issued when MALE = 1

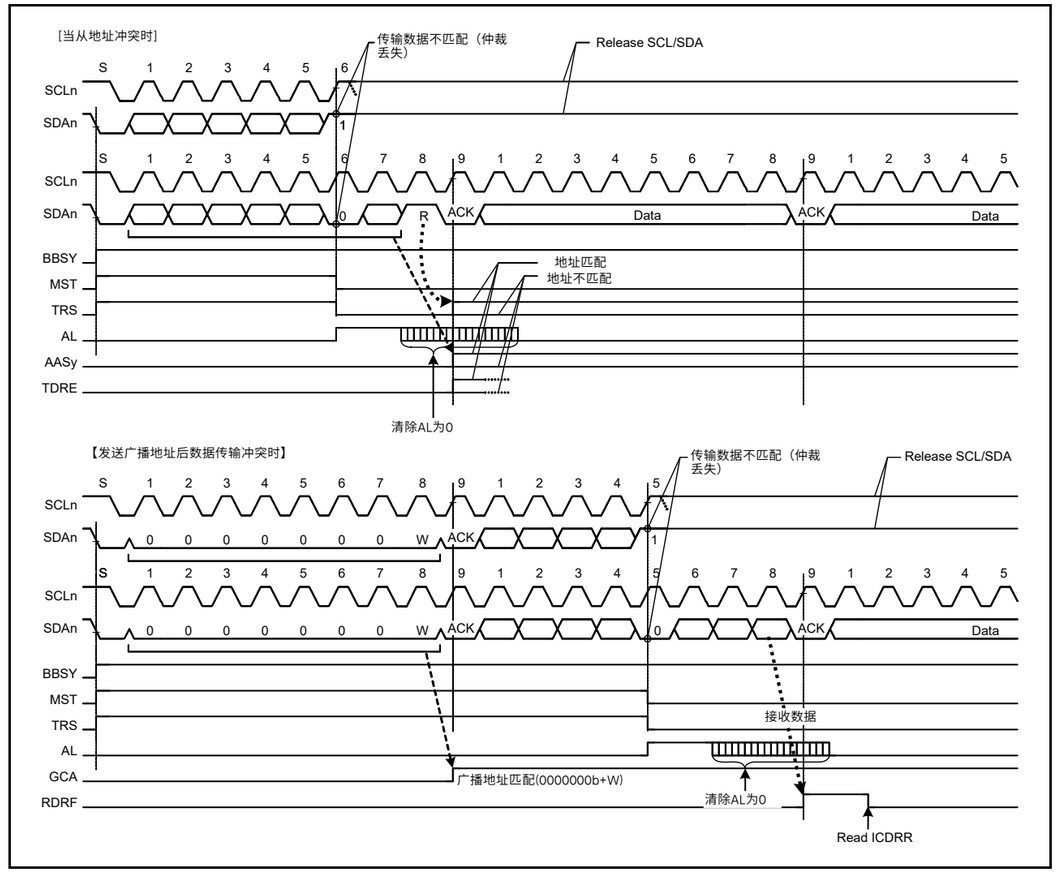


Figure 36.41 MALE=1时的主仲裁丢失检测示例

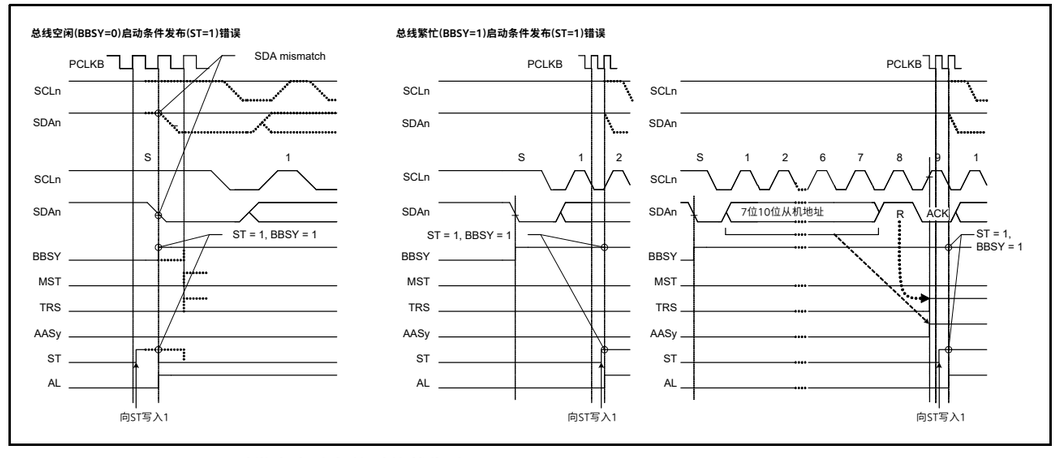


Figure 36.42 MALE=1时发出启动条件时仲裁失败

36.10.2 Function to Detect Loss of Arbitration during NACK Transmission (NALE Bit)

This function causes arbitration to be lost if the internal SDA output level does not match the level on the SDAn line (high output as the internal SDA output, meaning the SDAn pin is in the high-impedance state) and the low level is detected on the SDAn line during transmission of NACK in receive mode. Arbitration is lost because of a conflict of NACK and ACK transmission when two or more master devices receive data from the same slave device simultaneously in a multi-master system. Such conflict occurs when multiple master devices send or receive the same information through a single slave device. Figure 36.43 shows an example of arbitration-lost detection during transmission of NACK.

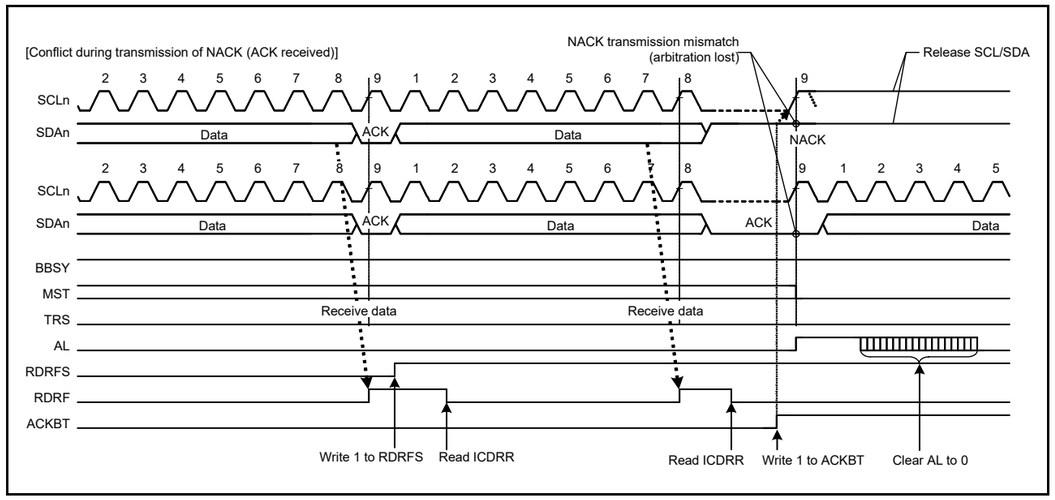


Figure 36.43 Example of arbitration-lost detection during transmission of NACK when NALE = 1

The following explains arbitration-lost detection using an example where two master devices (masters A and B) and a single slave device are connected through the bus. In this example, master A receives 2 bytes of data from the slave device, and master B receives 4 bytes of data from the slave device.

If masters A and B access the slave device simultaneously, because the slave address is identical, arbitration is not lost in either master A or B during access to the slave device. Both masters A and B recognize that they obtained the bus mastership and operate as such. Here, master A sends NACK when it has received 2 final bytes of data from the slave device. Meanwhile, master B sends ACK because it has not received the necessary 4 bytes of data. At this time, the NACK transmission from master A and the ACK transmission from master B conflict. In general, if a conflict like this occurs, master A cannot detect the ACK transmitted by master B and issues a stop condition. The issuance of the stop condition conflicts with the SCL clock output of master B, which disrupts communication.

When the IIC receives ACK during transmission of NACK, it detects a defeat in conflict with other master devices and causes arbitration to be lost. If arbitration is lost during transmission of NACK, the IIC immediately cancels the slave match condition and enters slave receive mode. This prevents a stop condition from being issued, preventing a communication failure on the bus.

Similarly, in the ARP command processing of SMBus, the function to detect loss of arbitration during transmission of NACK is also available for eliminating the extra clock cycle processing, such as FFh transmission processing, necessary if the UDID (Unique Device Identifier) of the assigned address does not match in the Get UDID general processing after the Assign Address command.

The IIC detects arbitration-lost during transmission of NACK when the following condition is met with the NALE bit in ICFER set to 1 (arbitration-lost detection during NACK transmission enabled).

[Condition for arbitration-lost during NACK transmission]

- When the internal SDA output level does not match the SDAn line (ACK is received) during transmission of NACK (ACKBT bit = 1 in ICMR3)

36.10.2 在NACK传输期间检测仲裁丢失的功能（NALE位）

如果内部SDA输出电平与SDAn线上的电平不匹配（高输出作为内部SDA输出，意味着SDAn引脚处于高阻抗状态）并且在上检测到低电平，此功能会导致仲裁丢失在接收模式下发送NACK期间的SDAn线。在多主系统中，当两个或多个主设备同时从同一从设备接收数据时，由于NACK和ACK传输冲突，导致仲裁丢失。当多个主设备通过单个从设备发送或接收相同的信息时，就会发生这种冲突。图36.43显示了在NACK传输期间检测仲裁丢失的示例。

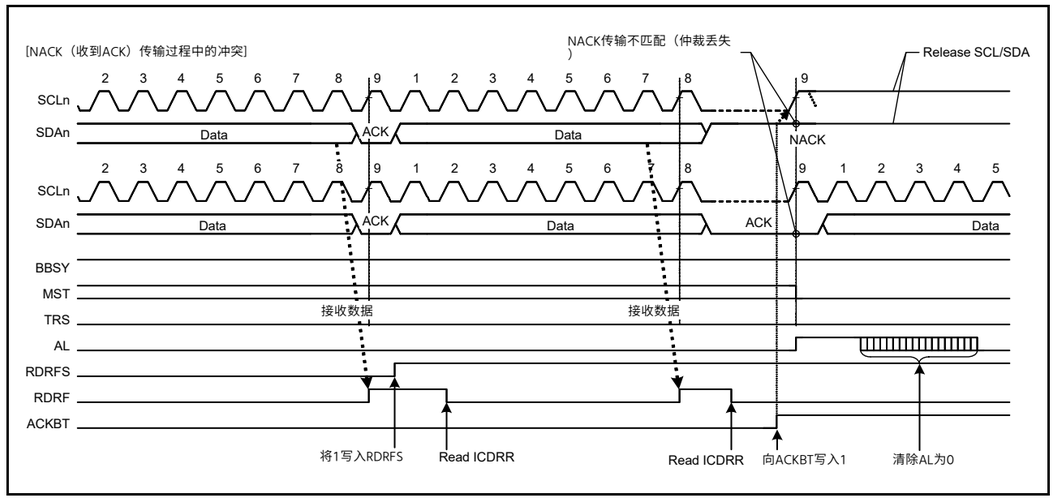


Figure 36.43 NALE=1时NACK传输期间仲裁丢失检测的示例

下面以两个主设备（主设备A和B）和一个从设备通过总线连接的示例来说明仲裁丢失检测。在本例中，主设备A从从设备接收2个字节的数据，主设备B从从设备接收4个字节的数据。

如果主设备A和B同时访问从设备，因为从设备地址相同，所以在访问从设备期间，主设备A或B都不会丢失仲裁。主控A和B都承认他们获得了总线主控权并以此进行操作。此处，主设备A在从从设备接收到最后2个字节的数据时发送NACK。同时，masterB发送ACK，因为它没有收到必要的4字节数据。此时，来自masterA的NACK传输和来自masterB的ACK传输冲突。一般来说，如果发生这样的冲突，masterA无法检测到masterB发送的ACK并发出停止条件。停止条件的发出与主机B的SCL时钟输出冲突，从而中断通信。

当IIC在NACK传输过程中收到ACK时，它会检测到与其他主设备冲突的失败并导致仲裁丢失。如果在NACK传输过程中仲裁丢失，IIC立即取消从机匹配条件并进入从机接收模式。这可以防止发出停止条件，从而防止总线上的通信故障。

同样，在SMBus的ARP命令处理中，检测传输过程中仲裁丢失的功能
NACK也可用于消除额外的时钟周期处理，例如FFh传输处理，如果分配地址的UDID（唯一设备标识符）在分配地址命令之后的获取UDID常规处理中不匹配，则这是必要的。

IIC在NACK传输期间检测到仲裁丢失，当满足以下条件时
ICFER设置为1（启用NACK传输期间的仲裁丢失检测）。

[在NACK传输期间仲裁丢失的条件]

- 在NACK传输期间内部SDA输出电平与SDAn线不匹配（接收到ACK）时（ICMR3中的ACKBT位=1）

36.10.3 Slave Arbitration-Lost Detection (SALE Bit)

This function causes arbitration to be lost if the transmit data (internal SDA output level) and the level on the SDAn line do not match (high output as the internal SDA output, meaning the SDAn pin is in the high-impedance state), and the low level is detected on the SDAn line in slave transmit mode. This arbitration-lost detection function is mainly used when transmitting a UDID (Unique Device Identifier) over an SMBus.

When it loses slave arbitration, the IIC is immediately released from the slave-matched state and enters slave receive mode. This function can detect conflicts of data during transmission of UDIDs over an SMBus and eliminates subsequent redundant processing for the transmission of FFh.

The IIC detects slave arbitration-lost when the following condition is met with the SALE bit in ICFER set to 1 (slave arbitration-lost detection enabled).

[Condition for slave arbitration-lost]

- When transmit data excluding acknowledge (internal SDA output level) does not match the SDAn line in slave transmit mode (MST and TRS bits = 01b in ICCR2).

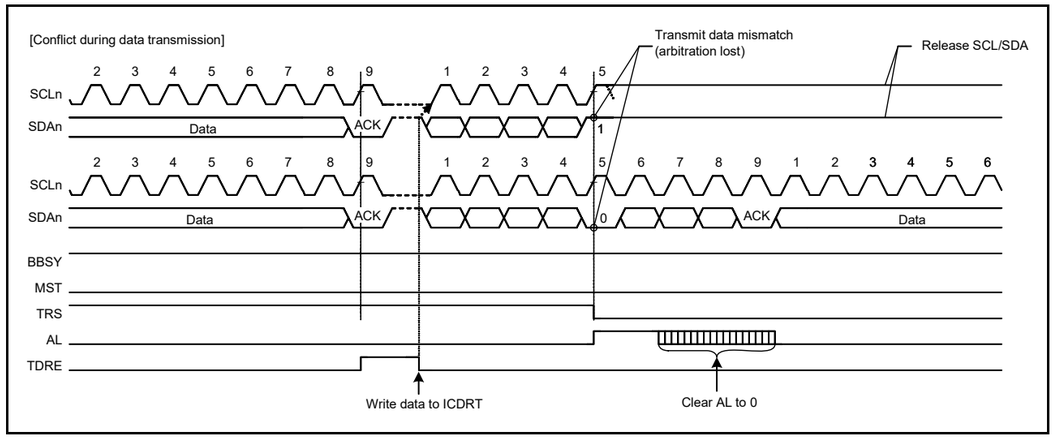


Figure 36.44 Example of slave arbitration-lost detection when SALE = 1

36.11 Start, Restart, and Stop Condition Issuing Function

36.11.1 Issuing a Start Condition

The IIC issues a start condition when the ST bit in ICCR2 is set to 1. When the ST bit is set to 1, a start condition request is made, and the IIC issues a start condition when the BBSY flag in ICCR2 is 0 (bus free state). When a start condition is issued normally, the IIC automatically shifts to the master transmit mode.

To issue a start condition:

1. Drive the SDAn line low (high level to low level).
2. Ensure that the time set in ICBRH and the start condition hold time elapse.
3. Drive the SCLn line low (high level to low level).
4. Detect low level on the SCLn line and ensure the low-level period of the SCLn line set in ICBRL elapses.

36.10.3 从设备仲裁丢失检测（SALE位）

如果发送数据（内部SDA输出电平）和SDAn线上的电平不匹配（高输出作为内部SDA输出，意味着SDAn引脚处于高阻状态），此功能会导致仲裁丢失，并且在从机发送模式下，SDAn线上检测到低电平。这种仲裁丢失检测功能主要用于通过SMBus传输UDID（唯一设备标识符）时。

当它失去从机仲裁时，IIC立即从从机匹配状态释放并进入从机接收模式。此功能可以检测在SMBus上传输UDID期间的数据冲突，并消除后续传输FFh的冗余处理。

当ICFER中的SALE位设置为1（启用从设备仲裁丢失检测）满足以下条件时，IIC检测从设备仲裁丢失。

[从机仲裁失败的条件]

- 当发送数据不包括确认（内部SDA输出电平）与从发送模式下的SDAn线不匹配时（MST和TRS位=ICCR2中的01b）。

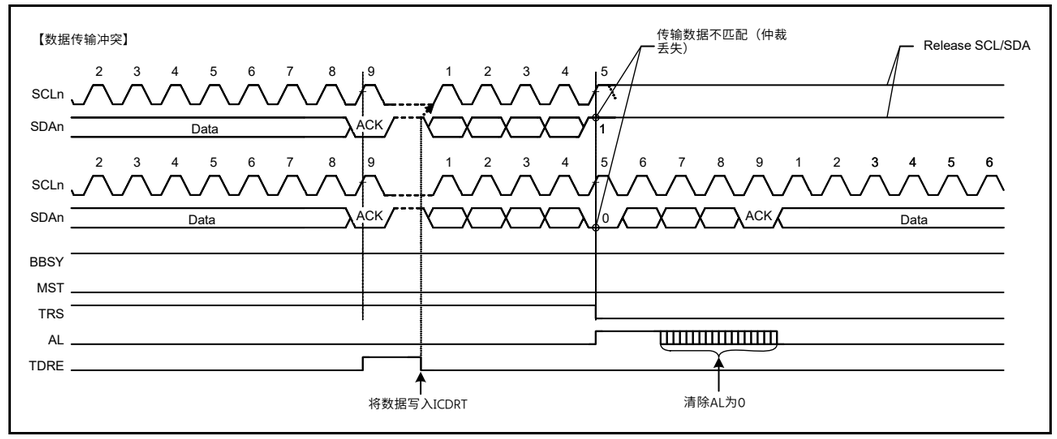


Figure 36.44 SALE=1时从设备仲裁丢失检测示例

36.11 启动、重启和停止条件发布功能

36.11.1 发出开始条件

当ICCR2中的ST位设置为1时，IIC发出启动条件。 当ST位设置为1时，发出启动条件请求，当ICCR2中的BBSY标志为0时，IIC发出启动条件（总线自由状态）。当启动条件正常发出时，IIC自动切换到主机发送模式。

发出开始条件：

1. 将SDAn线驱动为低电平（高电平到低电平）。
2. 确保ICBRH中设置的时间和启动条件保持时间已过。
3. 将SCLn线驱动为低电平（高电平到低电平）。
4. 检测SCLn线上的低电平，确保经过ICBRL中设置的SCLn线的低电平周期。

36.11.2 Issuing a Restart Condition

The IIC issues a restart condition when the RS bit in ICCR2 is set to 1. When the RS bit is set to 1, a restart condition request is made, and the IIC issues a restart condition when the BBSY flag in ICCR2 is 1 (bus busy state) and the MST bit in ICCR2 is 1 (master mode).

To issue a restart condition:

1. Release the SDAn line.
2. Ensure the low-level period of the SCLn line set in ICBRL elapses.
3. Release the SCLn line (low level to high level).
4. Detect a high level on the SCLn line and ensure the time set in ICBRL and the restart condition setup time elapse.
5. Drive the SDAn line low (high level to low level).
6. Ensure the time set in ICBRH and the restart condition hold time elapse.
7. Drive the SCLn line low (high level to low level).
8. Detect a low level on the SCLn line and ensure the low-level period of the SCLn line set in ICBRL elapses.

Note: When issuing restart condition requests, write the slave address to ICDRT after confirming that ICCR2.RS = 0. Data written while ICCR2.RS = 1 is not forwarded because of the retransmission condition before the occurrence.

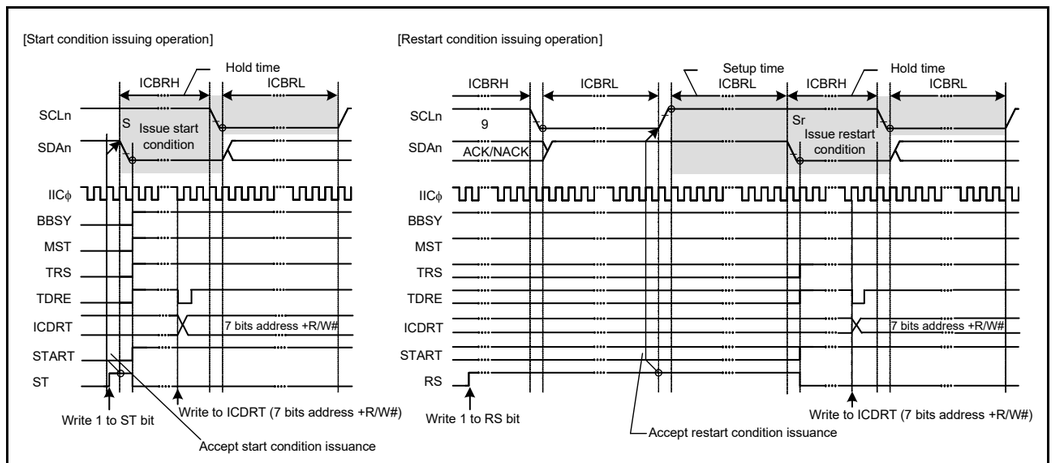


Figure 36.45 Start and restart condition issue timing using the ST and RS bits

Figure 36.46 shows the operation timing when a restart condition is issued after the master transmission.

[Restart condition issuance after the master transmission]

1. Initial setting. For details, refer to section 36.3.2, Initial Settings.
2. Read the BBSY flag in IICR2 to check that the bus is free, and then set the ST bit in ICCR2 to 1 (start condition issuance request). Upon receiving the request, the IIC issues a start condition. At the same time, the BBSY flag and the START flag in ICSR2 are automatically set to 1 and the ST bit is automatically set to 0. At this time, if the start condition is detected and the internal levels for the SDA output state and the levels on the SDAn line have matched while the ST bit is 1, the IIC recognizes that issuing of the start condition as requested by the ST bit has been successfully completed, and MST and TRS bits in ICCR2 are automatically set to 1, placing the IIC in master transmit mode. The TDRE flag in ICSR2 is also automatically set to 1 in response to setting of the TRS bit to 1.
3. Check that the TDRE flag in ICSR2 is 1, and then write the value for transmission (the slave address and the R/W# bit) to ICDRT. Once the data for transmission are written to ICDRT, the TDRE flag is automatically set to 0, the data are transferred from ICDRT to ICDRS, and the TDRE flag is again set to 1. After the byte containing the slave

36.11.2 发出重启条件

当ICCR2中的RS位设置为1时，IIC发出重启条件。当RS位设置为1时，发出重启条件请求，当ICCR2中的BBSY标志为1时，IIC发出重启条件（总线忙状态）并且ICCR2中的MST位为1（主模式）。

发出重启条件：

1. 释放SDAn线。
2. 确保ICBRL中设置的SCLn线的低电平周期已过。
3. 释放SCLn线（低电平到高电平）。
4. 检测SCLn线上的高电平并确保ICBRL中设置的时间和重启条件设置时间已过。
5. 将SDAn线驱动为低电平（高电平到低电平）。
6. 确保ICBRH中设置的时间和重启条件保持时间已过。
7. 将SCLn线驱动为低电平（高电平到低电平）。
8. 检测SCLn线上的低电平，确保经过ICBRL中设置的SCLn线的低电平周期。

Note: 发出重启条件请求时，确认ICCR2.RS=0后，将从机地址写入ICDRT。ICCR2.RS=1时写入的数据由于发生前的重发条件而不会转发。

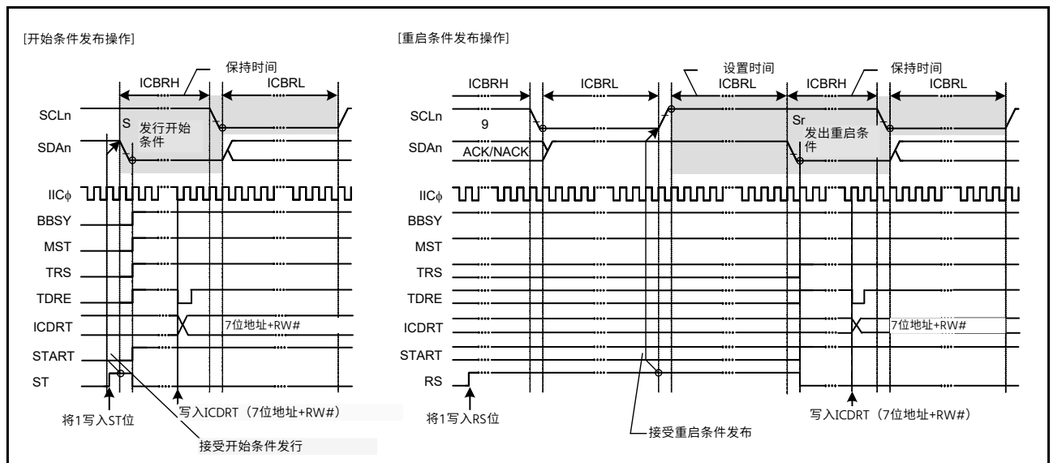


Figure 36.45 使用ST和RS位的启动和重启条件发出时序

图36.46显示了在主机发送后发出重新启动条件时的操作时序。

[主传输后的重启条件发布]

1. 初始设定。有关详细信息，请参阅第36.3.2节，初始设置。
2. 读取IICR2中的BBSY标志以检查总线是否空闲，然后将ICCR2中的ST位设置为1（开始条件发出请求）。收到请求后，IIC发出启动条件。同时，ICSR2中的BBSY标志和START标志自动置1，ST位自动置0。此时，如果检测到启动条件，内部电平为SDA输出状态和当ST位为1时SDAn线上的电平已匹配，IIC识别出ST位请求的启动条件的发布已成功完成，并且ICCR2中的MST和TRS位自动设置为1，将IIC在主发送模式。ICSR2中的TDRE标志也自动设置为1，以响应TRS位设置为1。
3. 检查ICSR2中的TDRE标志是否为1，然后将要发送的值（从机地址和RW#位）写入ICDRT。一旦将要传输的数据写入ICDRT，TDRE标志自动设置为0，数据从ICDRT传输到ICDRS，TDRE标志再次设置为1。在包含从机的字节之后

address and R/W# bit has been transmitted, the value of the TRS bit is automatically updated to select master transmit or master receive mode in accord with the value of the transmitted R/W# bit. If the value of the R/W# bit was 0, the IIC continues in master transmit mode. Since the ICSR2.NACKF flag being 1 at this time indicates that no slave device recognized the address or there was an error in communications, write 1 to ICCR2.SP bit to issue a stop condition. For data transmission with an address in the 10-bit format, start by writing 1111 0b, the 2 higher-order bits of the slave address, and W to ICDRT as the first address transmission. Then, as the second address transmission, write the 8 lower-order bits of the slave address to ICDRT.

4. After confirming that the TDRE flag in ICSR2 is 1, write the data for transmission to the ICDRT register. The IIC automatically holds the SCLn line low until the data for transmission are ready, a restart condition is issued or a stop condition is issued.
5. After all bytes of data for transmission have been written to the ICDRT register, wait until the value of the TEND flag in ICSR2 returns to 1, and then, after check that the START flag in ICSR2 is 1, set the START flag in ICSR2 to 0.
6. Set the RS bit in ICCR2 to 1 (restart condition issuance request). Upon receiving the request, the IIC issues a restart condition.
7. After check that the START flag in ICSR2 is 1, write the value for transmission (the slave address and the R/W# bit) to ICDRT.

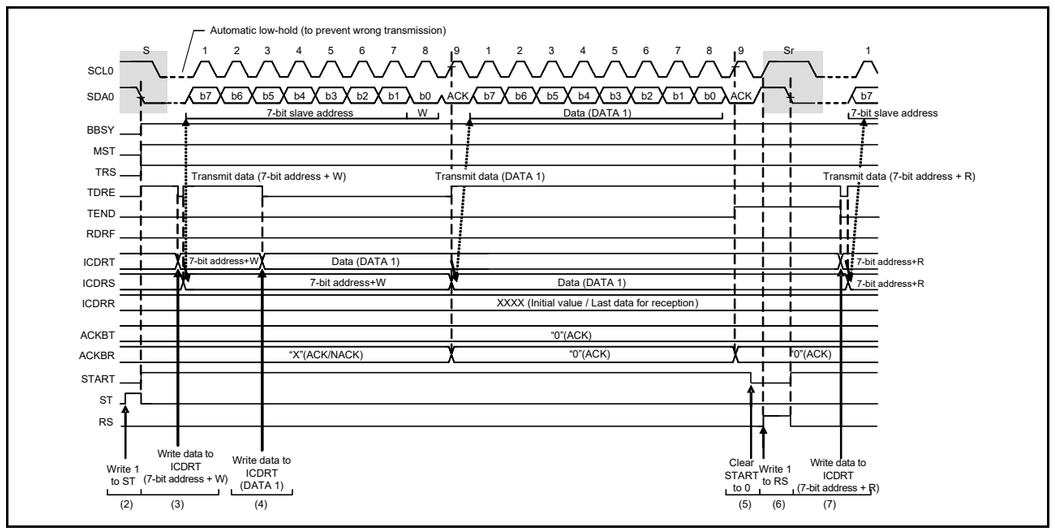


Figure 36.46 Restart condition issue timing after master transmission.

36.11.3 Issuing a Stop Condition

The IIC issues a stop condition when the SP bit in ICCR2 is set to 1. When the SP bit is set to 1, a stop condition request is made, and the IIC issues a stop condition when the BBSY flag in ICCR2 is 1 (bus busy state) and the MST bit in ICCR2 is 1 (master mode).

To issue a stop condition:

1. Drive the SDAn line low (high level to low level).
2. Ensure the low-level period of the SCLn line set in ICBRL elapses.
3. Release the SCLn line (low level to high level).
4. Detect a high level on the SCLn line and ensure the time set in ICBRH and the stop condition setup time elapse.
5. Release the SDAn line (low level to high level).
6. Ensure the time set in ICBRL and the bus free time elapse.

地址和RW#位已发送，TRS位的值会自动更新以根据发送的RW#位的值选择主机发送或主机接收模式。如果RW#位的值为0，则IIC继续处于主机发送模式。由于此时ICSR2.NACKF标志为1表示没有从设备识别该地址或通信出现错误，因此向ICCR2.SP位写入1以发出停止条件。对于地址为10位格式的数据传输，首先将11110b、从机地址的高2位和W写入ICDRT作为第一个地址传输。然后，作为第二次地址传输，将从地址的低8位写入ICDRT。

4. 确认ICSR2中的TDRE标志为1后，将要发送的数据写入ICDRT寄存器。IIC自动将SCLn线保持为低电平，直到传输数据准备好、发出重启条件或发出停止条件。
5. 待发送的所有字节数据写入ICDRT寄存器后，等待ICSR2中的TEND标志的值返回1，然后检查ICSR2中的START标志为1后，将ICSR2中的START标志设置为0。
6. 将ICCR2中的RS位设置为1（重新启动条件发布请求）。收到请求后，IIC发出重启条件。
7. 检查ICSR2中的START标志是否为1后，将要发送的值（从机地址和RW#位）写入ICDRT。

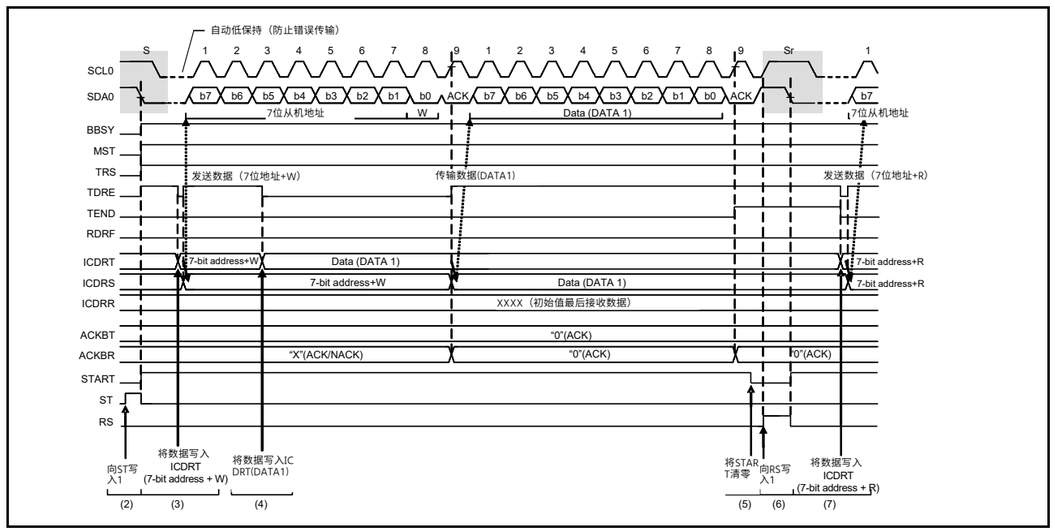


Figure 36.46 主传输后重启条件发出时序。

36.11.3 发出停止条件

当ICCR2中的SP位设置为1时，IIC发出停止条件。当SP位设置为1时，发出停止条件请求，当ICCR2中的BBSY标志为1时，IIC发出停止条件（总线忙状态）并且ICCR2中的MST位为1（主模式）。

发出停止条件：

1. 将SDAn线驱动为低电平（高电平到低电平）。
2. 确保ICBRL中设置的SCLn线的低电平周期已过。
3. 释放SCLn线（低电平到高电平）。
4. 检测SCLn线上的高电平并确保ICBRH中设置的时间和停止条件设置时间已过。
5. 释放SDAn线（低电平到高电平）。
6. 确保ICBRL中设置的时间和巴士空闲时间已过。

7. Clear the BBSY flag to 0 to release the bus mastership.

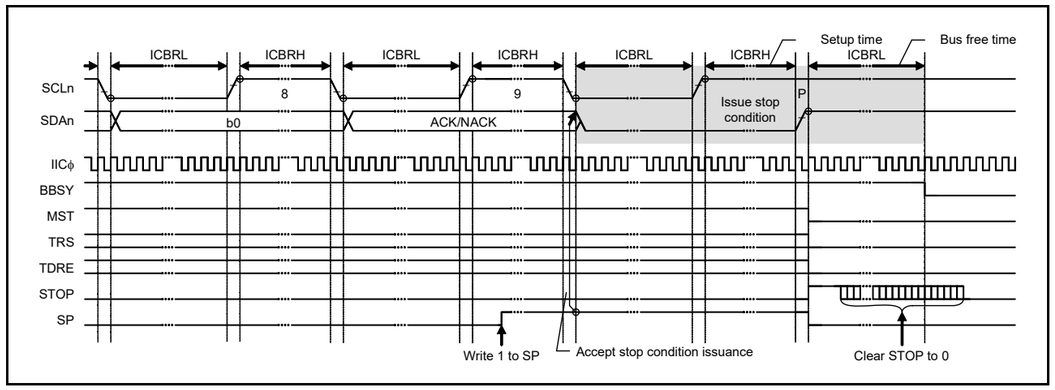


Figure 36.47 Stop condition issue timing using the SP bit

36.12 Bus Hanging

If the clock signals from the master and slave devices go out of synchronization because of noise or other factors, the I2C bus might hang with a fixed level on the SCLn or SDAn line.

To manage bus hanging, the IIC has:

- A timeout function to detect hanging by monitoring the SCLn line
- A function for the output of an extra SCL clock cycle to release the bus from a hung state because of clock signals being out of synchronization
- The IIC reset function
- An internal reset function.

By checking the SCLO, SDAO, SCLI, and SDAI bits in ICCR1, it is possible to see whether the IIC or its communicating partner is placing the low level on the SCLn or SDAn line.

36.12.1 Timeout Function

The timeout function can detect when the SCLn line is stuck longer than the predetermined time. The IIC can detect an abnormal bus state by monitoring that the SCLn line is stuck low or high for a predetermined time.

The timeout function monitors the SCLn line state and counts the low- or high-level period using the internal counter. The timeout function resets the internal counter each time the SCLn line changes (rises or falls), but continues to count unless the SCLn line changes. If the internal counter overflows because no SCLn line changes, the IIC can detect the timeout and report the bus hung state.

This timeout function is enabled when the ICFER.TMOE bit is 1. It detects a hung state when the SCLn line is stuck low or high during the following conditions:

- The bus is busy (ICCR2.BBSY flag is 1) in master mode (ICCR2.MST bit is 1)
- The IIC slave address is detected (ICSR1 register is not 00h) and the bus is busy (ICCR2.BBSY flag is 1) in slave mode (ICCR2.MST bit is 0)
- The bus is free (ICCR2.BBSY flag is 0) while a start condition is requested (ICCR2.ST bit is 1).

The internal counter of the timeout function uses the internal reference clock (IICϕ) set in the CKS[2:0] bits in ICMR1 as a count source. It functions as a 16-bit counter when long mode is selected (TMOS bit = 0 in ICMR2) or a 14-bit counter when short mode is selected (TMOS bit = 1).

The SCLn line level (low, high, or both levels) during which this counter is activated can be selected in the TMOH and TMOL bits in ICMR2. If both TMOL and TMOH bits are set to 0, the internal counter does not work.

7. 将BBSY标志清除为0以释放总线主控权。

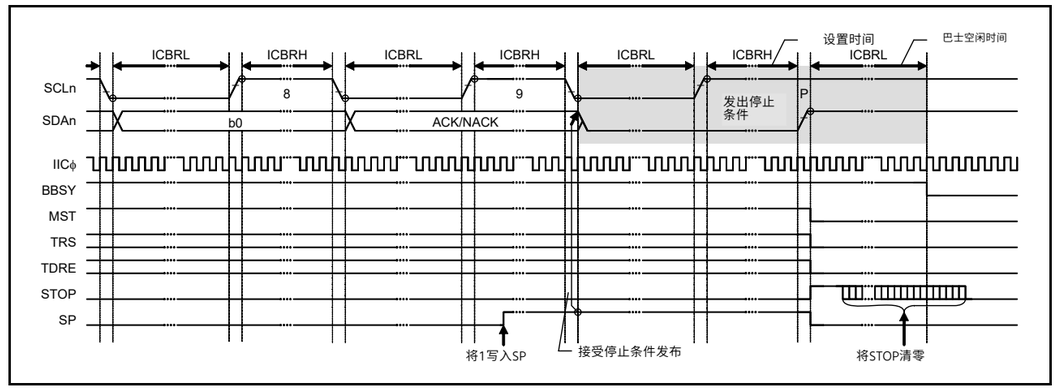


Figure 36.47 使用SP位的停止条件发出时序

36.12 巴士挂

如果来自主设备和从设备的时钟信号由于噪声或其他因素而失去同步，则I2C总线可能会在SCLn或SDAn线上以固定电平挂起。

为了管理总线挂起，IIC具有：

- 通过监控SCLn线路来检测挂起的超时功能
- 由于时钟信号不同步而输出额外SCL时钟周期以将总线从挂起状态中释放的功能
- IIC复位功能
- 内部复位功能。

通过检查ICCR1中的SCLO、SDAO、SCLI和SDAI位，可以查看IIC或其通信伙伴是否将SCLn或SDAn线置于低电平。

36.12.1 超时功能

超时功能可以检测SCLn线路何时卡住超过预定时间。IIC可以通过监视SCLn线在预定时间内保持低电平或高电平来检测异常总线状态。

超时功能监控SCLn线路状态并使用内部计数器计算低电平或高电平周期。每次SCLn线改变（上升或下降）时，超时功能都会复位内部计数器，但除非SCLn线改变，否则会继续计数。如果内部计数器因为SCLn线没有变化而溢出，IIC可以检测到超时并报告总线挂起状态。

此超时功能在ICFER.TMOE位为1时启用。在以下情况下，当SCLn线卡在低电平或高电平时，它会检测到挂起状态：

- 总线繁忙（ICCR2.BBSY标志为1）处于主模式（ICCR2.MST位为1）
- 检测到IIC从机地址（ICSR1寄存器不是00h）并且在从机模式下总线忙（ICCR2.BBSY标志为1）（ICCR2.MST位为0）
- 当请求启动条件时（ICCR2.ST位为1），总线空闲（ICCR2.BBSY标志为0）。

超时功能的内部计数器使用ICMR1的CKS[2:0]位中设置的内部参考时钟(IIC)作为计数源。Itfunctionsasa16-bitcounterwhenlongmodeisselected(TMOSbit=0inICMR2)ora14-bitcounterwhenshortmodeisselected(TMOSbit=1).

可以在TMOH和
ICMR2中的TMOL位。如果TMOL和TMOH位都设置为0，则内部计数器不工作。

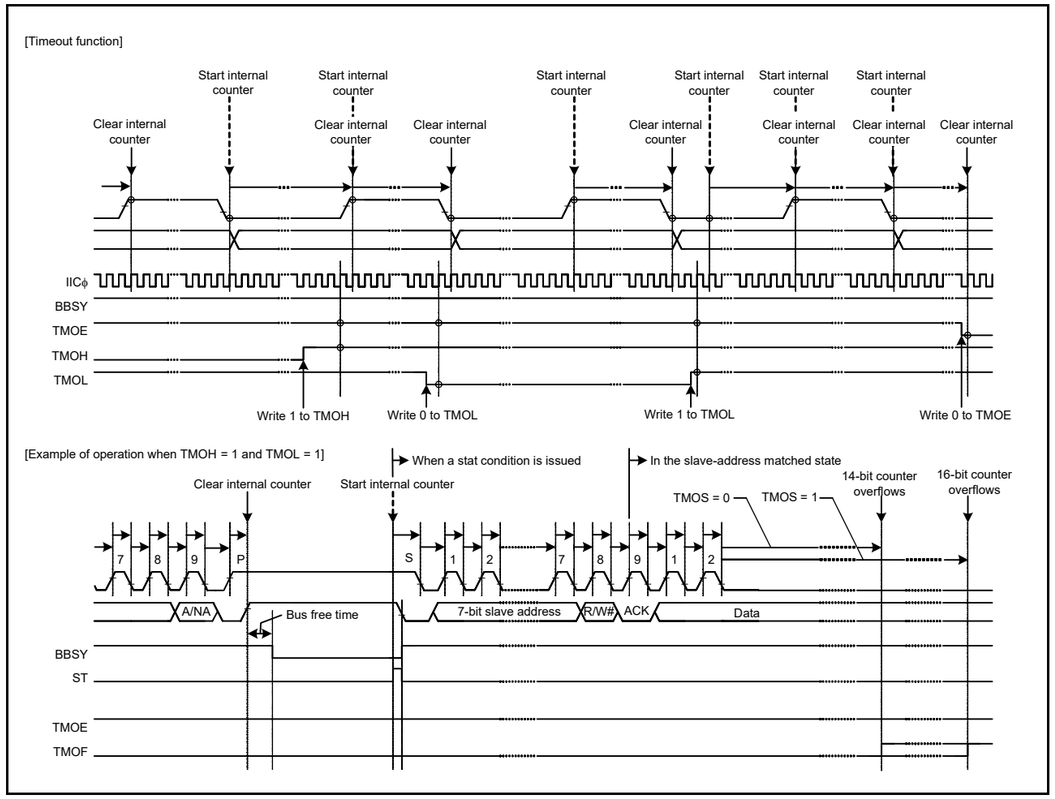


Figure 36.48 Timeout function using the TMOE, TMOS, TMOH, and TMOL bits

36.12.2 Extra SCL Clock Cycle Output Function

In master mode, this function outputs extra SCL clock cycles to release the SDAn line of the slave device from being held at the low level because the master is out of synchronization with the slave device. This function is mainly used in master mode to release the SDAn line of the slave device from being fixed low by including extra cycles of SCL output from the IIC. It uses single cycles of the SCL clock for a bus error where the IIC cannot issue a stop condition because the slave device is holding the SDAn line at the low level. Do not use this function in normal situations. Using it when communications are proceeding correctly leads to malfunctions.

When the CLO bit in ICCR1 is set to 1 in master mode, a single cycle of the SCL clock at the transfer rate specified in the CKS[2:0] bits in ICMR1, and in the ICBRH and ICBRL registers, is output as an extra clock cycle. After output of this single cycle of the SCL clock, the CLO bit automatically is set to 0. If the BBSY flag is 1, SCL terminal keeps low output, if BBSY flag is 0, SCL terminal keeps high output. Additional clock cycles can be output consecutively by writing 1 to the CLO bit with software after reading the bit as 0.

When the IIC module is in master mode and the slave device is holding the SDAn line at the low level because synchronization with the slave device was lost because of noise or other effects, the output of a stop condition is not possible. This function can be used to output extra cycles of SCL one by one to make the slave device release the SDAn line from being held at the low level, and so recovering the bus from an unusable state. Release of the SDAn line by the slave device can be monitored by reading the SDAI bit in ICCR1. After confirming release of the SDAn line by the slave device, complete communications by reissuing the stop condition.

[Output conditions for using the CLO bit in ICCR1]

- When the bus is free (BBSY flag in ICCR2 = 0) or in master mode (MST bit = 1 and BBSY flag = 1 in ICCR2)
- When the communication device does not hold the SCLn line low.

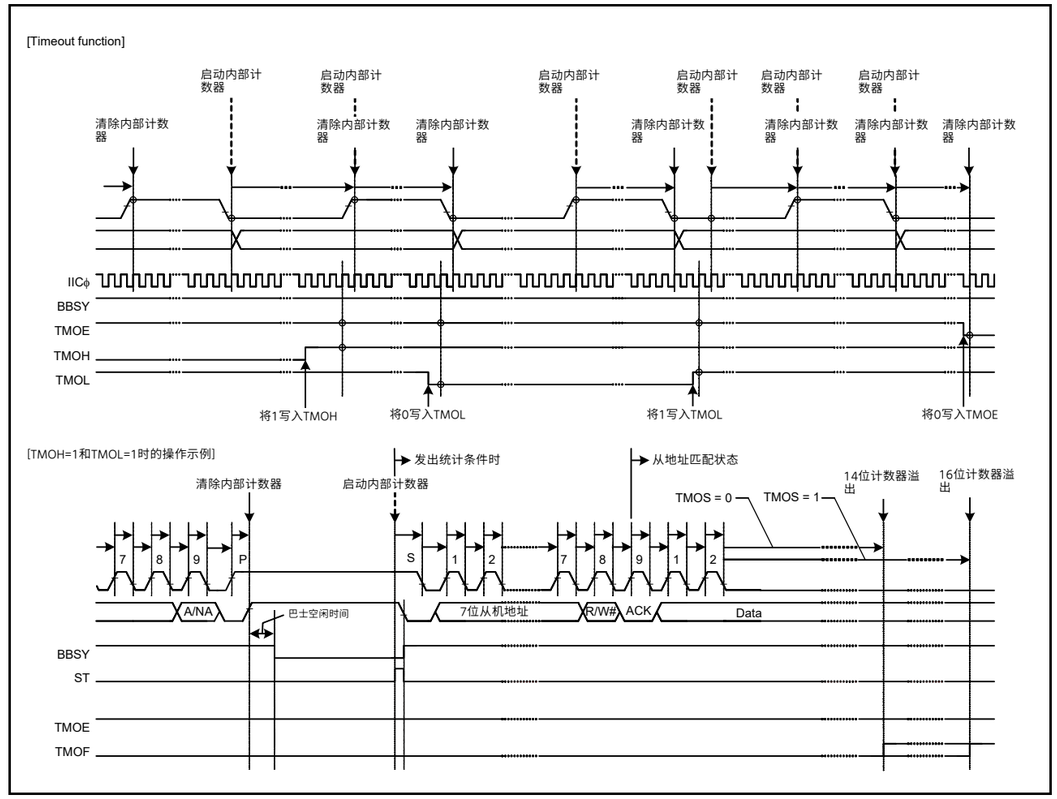


Figure 36.48 使用TMOE、TMOS、TMOH和TMOL位的超时功能

36.12.2 额外的SCL时钟周期输出功能

在主模式下，该函数输出额外的SCL时钟周期，以释放从设备的SDAn线保持在低电平，因为主设备与从设备不同步。该功能主要用于主机模式，通过包含IIC的额外SCL输出周期来释放从机设备的SDAn线固定为低电平。它使用SCL时钟的单个周期来处理IIC无法发出停止条件的总线错误，因为从设备将SDAn线保持在低电平。在正常情况下不要使用此功能。在通信正常进行时使用它会导致故障。

当ICCR1中的CLO位在主机模式下设置为1时，以ICMR1中的CKS[2:0]位以及ICBRH和ICBRL寄存器中指定的传输速率输出一个SCL时钟周期作为额外的时钟周期。在SCL时钟的这个单周期输出后，CLO位自动置0。如果BBSY标志为1，SCL端保持低电平输出，如果BBSY标志为0，SCL端保持高电平输出。将CLO位读为0后，用软件将1写入CLO位，可以连续输出额外的时钟周期。

当IIC模块处于主机模式并且从机由于噪声或其他影响而失去与从机的同步而将SDAn线保持在低电平时，停止条件的输出是不可能的。该功能可用于逐个输出额外的SCL周期，使从设备释放SDAn线保持在低电平，从而使总线从不可用状态恢复。从设备释放SDAn线可以通过读取ICCR1中的SDAI位来监控。确认从设备释放SDAn线后，通过重新发出停止条件完成通信。

[使用ICCR1中CLO位的输出条件]

- 当总线空闲（ICCR2中的BBSY标志=0）或处于主机模式（ICCR2中的MST位=1且BBSY标志=1）时
- 当通信设备不保持SCLn线为低电平时。

Figure 36.49 shows the operation timing of the extra SCL clock cycle output function (CLO bit).

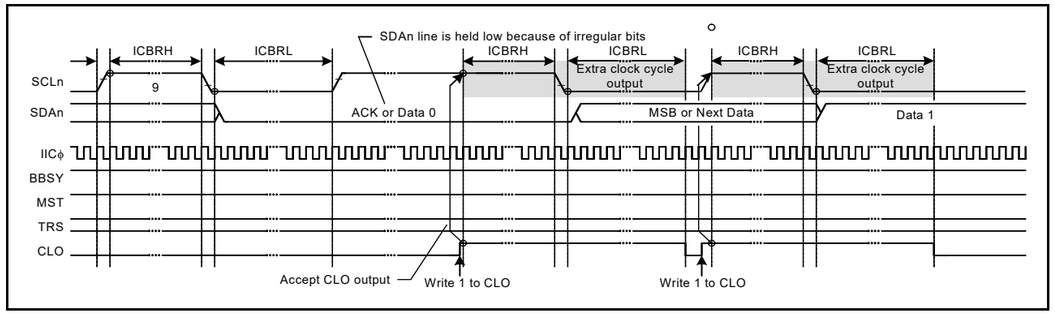


Figure 36.49 Extra SCL clock cycle output function using the CLO bit

36.12.3 IIC Reset and Internal Reset

The IIC module incorporates a function for resetting itself. It uses two types of resets: an IIC reset, which initializes all registers, including the BBSY flag in ICCR2, and an internal reset, which releases the IIC from the slave-address matched state and initializes the internal counter while saving other settings. After issuing a reset, always set the IICRST bit in ICCR1 to 0.

Both types of resets are valid for release from bus-hung states, because both restore the output state of the SCLn and SDAn pins to the high-impedance state.

Issuing a reset during slave operation might lead to a loss of synchronization between the master device clock and the slave device clock, so avoid this when possible. In addition, monitoring of the bus state, such as for the presence of a start condition, is not possible during an IIC reset (ICE and IICRST bits = 01b in ICCR1).

For a detailed description of the IIC and internal resets, see section 36.15, State of Registers when Issuing each Condition.

36.13 SMBus Operation

The IIC is available for data communication conforming to the SMBus Specification (version 2.0). To perform SMBus communication, set the SMBS bit in ICMR3 to 1. To use the transfer rate within a range of 10 to 100 kbps of the SMBus standard, set the CKS[2:0] bits in ICMR1, ICBRH, and ICBRL. In addition, specify the values in the DLCS bit in ICMR2 and the SDDL[2:0] bits in ICMR2 to meet the data hold time specification of 300 ns or more. When the IIC is used only as a slave device, the transfer rate setting is not required, but ICBRL must be set to a value longer than the data setup time (250 ns).

For the SMBus device default address (1100 001b), use one of the slave address registers L0 to L2 (SARL0, SARL1, and SARL2), and set the associated FS bit (7- or 10-bit address format select) in SARUy (y = 0 to 2) to 0 (7-bit address format).

When transmitting the UDID (Unique Device Identifier), set the SALE bit in ICFER to 1 to enable the slave arbitration-lost detection function.

图36.49显示了额外SCL时钟周期输出功能（CLO位）的操作时序。

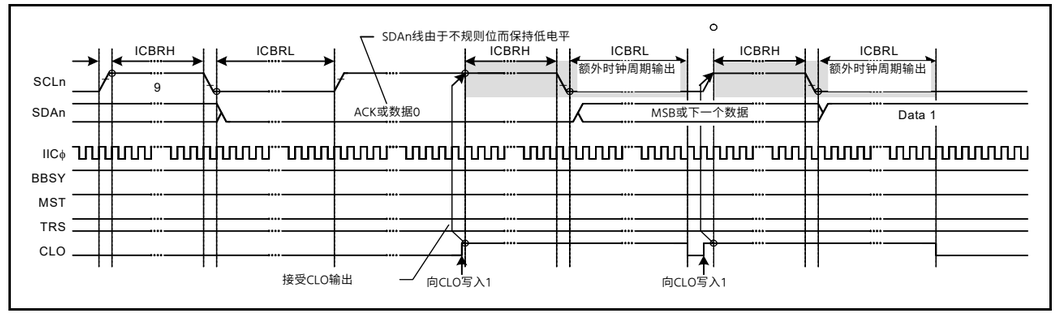


Figure 36.49 使用CLO位的额外SCL时钟周期输出功能

36.12.3 IIC复位和内部复位

IIC模块包含一个自我复位功能。它使用两种类型的复位：IIC复位，初始化所有寄存器，包括ICCR2中的BBSY标志，以及内部复位，将IIC从从地址匹配状态释放并初始化内部计数器，同时保存其他设置。发出复位后，始终将ICCR1中的IICRST位设置为0。

这两种类型的复位对于从总线挂起状态中释放都是有效的，因为两者都恢复了SCLn的输出状态和SDAn引脚处于高阻抗状态。

在从机操作期间发出复位可能会导致主设备时钟和从设备时钟之间失去同步，因此请尽可能避免这种情况。此外，在IIC复位（ICE和IICRST位=ICCR1中的01b）期间无法监控总线状态，例如是否存在启动条件。

有关IIC和内部复位的详细说明，请参阅第36.15节，发出每个寄存器时的状态Condition.

36.13 SMBus Operation

IIC可用于符合SMBus规范（2.0版）的数据通信。要进行SMBus通信，请将ICMR3中的SMBS位设置为1。要使用SMBus标准的10至100kbps范围内的传输速率，请设置ICMR1、ICBRH和ICBRL中的CKS[2:0]位。此外，请指定ICMR2中的DLCS位和ICMR2中的SDDL[2:0]位中的值，以满足300ns或更长的数据保持时间规范。当IIC仅用作从设备时，不需要设置传输速率，但必须将ICBRL设置为比数据建立时间（250ns）更长的值。

对于SMBus器件默认地址(1100001b)，使用从地址寄存器L0到L2之一（SARL0、SARL1和SARL2），并将SARUy(y=0to2)中相关的FS位（7位或10位地址格式选择）设置为0（7位地址格式）。

发送UDID（UniqueDeviceIdentifier）时，将ICFER中的SALE位设置为1，以使能从机仲裁丢失检测功能。

36.13.1 SMBus Timeout Measurement

(1) Measuring slave device timeout

The following period (timeout interval: $T_{LOW: SEXT}$) must be measured for slave devices in SMBus communication:

- From start condition to stop condition.

To measure timeout for slave devices, measure the period from start condition detection to stop condition detection with the GPT using the IIC start condition detection interrupt (STIn) and stop condition detection interrupt (SPIn). The measured timeout period must be within the total clock low-level period [slave device] $T_{LOW: SEXT}$: 25 ms (maximum) of the SMBus standard.

If the time measured with the GPT exceeds the clock low-level detection timeout $T_{TIMEOUT}$: 25 ms (minimum) of the SMBus standard, the slave device must release the bus by writing 1 to the IICRST bit in ICCR1 to issue an internal reset of the IIC. When an internal reset is issued, the IIC stops driving the bus for the SCLn and SDAn pins, making them output high-impedance, which releases the bus.

(2) Measuring master device timeout

The following periods (timeout interval: $T_{LOW: MEXT}$) must be measured for master devices in SMBus communication:

- From start condition to acknowledge bit
- Between acknowledge bits
- From acknowledge bit to stop condition.

To measure timeout for master devices, measure these periods with the GPT using the IIC start condition detection interrupt (STIn), stop condition detection interrupt (SPIn), transmit end interrupt (IICn_TEI), or receive data full interrupt (IICn_RXI). The measured timeout period must be within the total clock low-level extended period (master device) $T_{LOW: MEXT}$: 10 ms (maximum) of the SMBus standard, and the total of all $T_{LOW: MEXT}$ values from start condition to stop condition must be within $T_{LOW: SEXT}$: 25 ms (maximum).

For the ACK receive timing (rising edge of the ninth SCL clock cycle), monitor the TEND flag in ICSR2 in master transmit mode (master transmitter) and the RDRF flag in ICSR2 in master receive mode (master receiver). Perform byte-wise transmit operations in master transmit mode, and hold the RDRFS bit in ICMR3 at 0 until the byte immediately before reception of the final byte in master receive mode. While the RDRFS bit is 0, the RDRF flag is set to 1 on the rising edge of the ninth SCL clock cycle.

If the period measured with the GPT exceeds the total clock low-level extended period (master device) $T_{LOW: MEXT}$: 10 ms (maximum) of the SMBus standard or the total of measured periods exceeds the clock low-level detection timeout $T_{TIMEOUT}$: 25 ms (minimum) of the SMBus standard, the master device must stop the transaction by issuing a stop condition. In master transmit mode, immediately stop the transmit operation (writing data to ICDRT).

36.13.1 SMBus超时测量

(1) 测量从设备超时

对于SMBus通信中的从设备，必须测量以下周期（超时间隔：TLOW:SEXT）：

- 从开始条件到停止条件。

要测量从设备的超时，请使用GPT使用IIC启动条件检测中断(STIn)和停止条件检测中断(SPIn)测量从启动条件检测到停止条件检测的周期。测得的超时周期必须在总时钟低电平周期[从设备]TLOW:SEXT:SMBus标准的25ms（最大值）内。

如果用GPT测量的时间超过时钟低电平检测超时TTIMEOUT:25ms（最小值）
SMBus标准，从设备必须通过向ICCR1中的IICRST位写入1来释放总线，以发出IIC的内部复位。当发出内部复位时，IIC停止驱动SCLn和SDAn引脚的总线，使它们输出高阻抗，从而释放总线。

(2) 测量主设备超时

对于SMBus通信中的主设备，必须测量以下周期（超时间隔：TLOW:MEXT）：

- 从开始条件到确认位
- 确认位之间
- 从确认位到停止条件。

要测量主设备的超时，请使用GPT使用IIC开始条件检测中断(STIn)、停止条件检测中断(SPIn)、发送结束中断(IICn_TEI)或接收数据完整中断(IICn_RXI)来测量这些周期。测量的超时周期必须在总时钟低电平扩展周期（主设备）TLOW：MEXT：SMBus标准的10毫秒（最大值）内，以及所有TLOW：从启动条件到停止条件的MEXT值的总和必须在TLOW内：SEXT：25毫秒（最大值）。

对于ACK接收时序（第9个SCL时钟周期的上升沿），在主机发送模式（主机发送器）监视ICSR2中的TEND标志，在主机接收模式（主机接收器）监视ICSR2中的RDRF标志。在主机发送模式下执行逐字节发送操作，并将ICMR3中的RDRFS位保持为0，直到在主机接收模式下接收到最后一个字节之前的字节。当RDRFS位为0时，RDRF标志在第9个SCL时钟周期的上升沿设置为1。

如果用GPT测量的周期超过总时钟低电平延长周期（主设备）TLOW:MEXT:SMBus标准的10ms（最大值）或总测量周期超过时钟低电平检测超时TTIMEOUT：SMBus标准的25ms（最小值），主设备必须通过发出停止条件来停止事务。在主机发送模式下，立即停止发送操作（将数据写入ICDRT）。

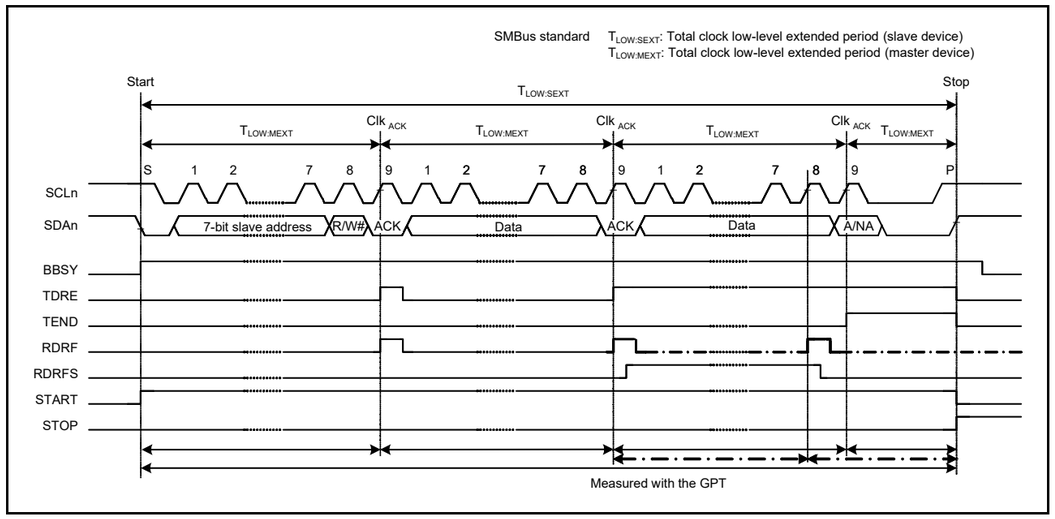


Figure 36.50 SMBus timeout measurement

36.13.2 Packet Error Code (PEC)

The MCU incorporates a CRC calculator, which enables transmission of a packet error code (PEC) or allows checking of the received data in SMBus data communication for the IIC. For the CRC-generating polynomials of the CRC calculator, see section 40, Cyclic Redundancy Check (CRC) Calculator.

In master transmit mode, the PEC data can be invoked by writing all transmit data to the CRC data input register (CRCDIR) in the CRC calculator.

In master receive mode, the PEC data can be checked by writing all receive data to CRCDIR in the CRC calculator and comparing the obtained value in the CRC Data Output Register (CRCDOR) with the received PEC data.

To send ACK or NACK based on the match or mismatch result when the final byte is received as a result of the PEC code check, set the RDRFS bit in ICMR3 to 1 before the rising edge of the eighth SCL clock cycle during reception of the final byte, and hold the SCLn line low on the falling edge of the eighth clock cycle.

36.13.3 SMBus Host Notification Protocol (Notify ARP Master Command)

In communicating on an SMBus, a slave device can temporarily act as a master device to notify the SMBus host or ARP master of, or request the SMBus host for, its own slave address or request its own slave address from the SMBus host.

For a product using the MCU to operate as an SMBus host or ARP master, the host address (0001 000b) sent from the slave device must be detected as a slave address, so the IIC provides a function for detecting the host address. To detect the host address as a slave address, set the SMBS bit in ICMR3 and the HOAE bit in ICSER to 1. Operation after the host address is detected is the same as normal slave operation.

36.14 Interrupt Sources

The IIC issues four types of interrupt requests: transfer error or event occurrence (detection of arbitration-lost, NACK, timeout, start or restart condition, or stop condition), receive data full, transmit data empty, and transmit end. Table 36.10 lists details about the interrupt requests. The receive data full and transmit data empty interrupts are both capable of activating data transfer by the DTC or DMAC.

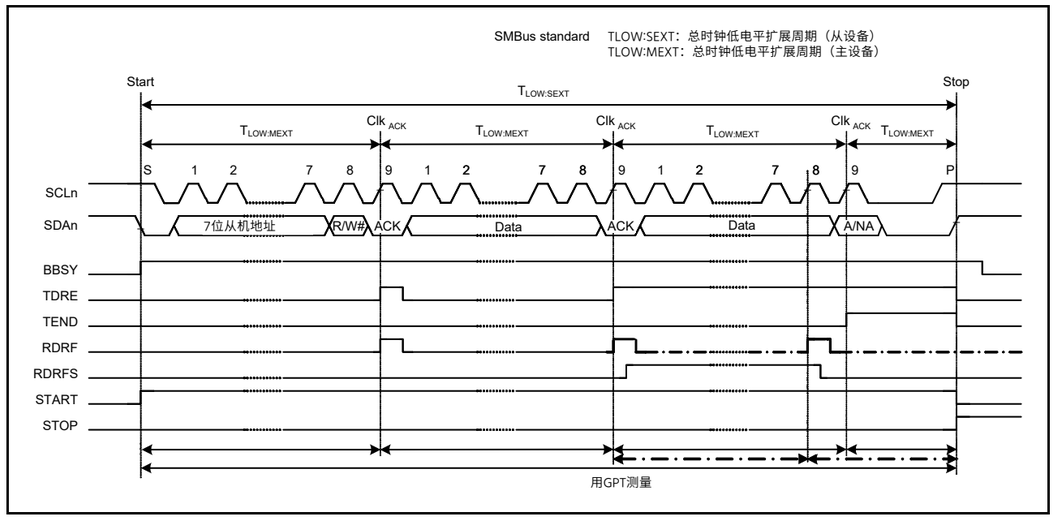


Figure 36.50 SMBus超时测量

36.13.2 数据包错误代码(PEC)

MCU包含一个CRC计算器，它可以传输数据包错误代码(PEC)或允许检查IIC的SMBus数据通信中接收到的数据。有关CRC计算器的CRC生成多项式，请参阅第40节，循环冗余校验(CRC)计算器。

在主机发送模式下，可以通过将所有发送数据写入CRC计算器中的CRC数据输入寄存器(CRCDIR)来调用PEC数据。

在主机接收模式下，可以通过将所有接收数据写入CRC计算器中的CRCDIR并将CRC数据输出寄存器(CRCDOR)中获得的值与接收到的PEC数据进行比较来检查PEC数据。

在接收到作为PEC代码检查的结果的最后一个字节时，要根据匹配或不匹配结果发送ACK或NACK，在接收最后一个字节期间，在第8个SCL时钟周期的上升沿之前将ICMR3中的RDRFS位设置为1字节，并在第八个时钟周期的下降沿保持SCLn线为低电平。

36.13.3 SMBus主机通知协议（通知ARP主机命令）

在SMBus上进行通信时，从设备可以临时充当主设备来通知SMBus主机或ARP主机，或向SMBus主机请求其自己的从地址，或从SMBus主机请求其自己的从地址。

对于使用MCU作为SMBus主机或ARP主机的产品，从机发送的主机地址（0001000b）必须被检测为从机地址，因此IIC提供了主机地址检测功能。要将主机地址检测为从机地址，请将ICMR3中的SMBS位和ICSER中的HOAE位设置为1。检测到主机地址后的操作与正常从机操作相同。

36.14 中断源

IIC发出四种类型的中断请求：传输错误或事件发生（检测仲裁丢失、NACK、超时、开始或重新启动条件或停止条件）、接收数据满、发送数据空和发送结束。表36.10列出了有关中断请求的详细信息。接收数据满和发送数据空中断都能够通过DTC或DMAC激活数据传输。

Table 36.10 Interrupt sources

Symbol	Interrupt source	Interrupt flag	DMAC/DTC activation	Interrupt condition
IICn_EEI*5	Transfer error or event occurrence	AL	Not possible	AL = 1, ALIE = 1
		NACKF		NACKF = 1, NAKIE = 1
		TMOF		TMOF = 1, TMOIE = 1
		START		START = 1, STIE = 1
		STOP		STOP = 1, SPIE = 1
IICn_RXI*2, *5	Receive data full	RDRF	Possible	RDRF = 1, RIE = 1
IICn_TXI*1, *5	Transmit data empty	TDRE	Possible	TDRE = 1, TIE = 1
IICn_TEI*3, *5	Transmit end	TEND	Not possible	TEND = 1, TEIE = 1
IIC0_WUI*4	Slave address match during wakeup function	WUF	Not possible	Slave address match Slave receive complete RWAK operation ASY0 = 1 WUIE = 1

Note: There is a delay between the execution of a write instruction for a peripheral module by the CPU and the actual writing to the module. When an interrupt flag is cleared or masked, read the relevant flag again to check whether clearing or masking is complete, and then return from interrupt handling. Not doing so creates the possibility of repeated processing of the same interrupt.
Note 1. Because IICn_TXI is edge-detected, it does not require clearing. Additionally, the TDRE flag in ICSR2 (condition for IICn_TXI) automatically is set to 0 when transmit data is written to ICDRT or a stop condition is detected (STOP flag = 1 in ICSR2).
Note 2. Because IICn_RXI is edge-detected, it does not require clearing. Additionally, the RDRF flag in ICSR2 (condition for IICn_RXI) automatically is set to 0 when data is read from ICDRR.
Note 3. When using the IICn_TEI interrupt, clear the TEND flag in ICSR2 in the IICn_TEI interrupt handling. The TEND flag in ICSR2 automatically is set to 0 when transmit data is written to ICDRT or a stop condition is detected (STOP flag = 1 in ICSR2).
Note 4. Only channel 0 has a wakeup function, so IIC0_WUI is for channel 0 only.
Note 5. Channel number (n = 0 to 2).

Clear or mask each flag during interrupt handling.

36.14.1 Buffer Operation for IICn_TXI and IICn_RXI Interrupts

If the conditions for generating an IICn_TXI or IICn_RXI interrupt are satisfied while the associated IR flag is 1, the interrupt request is not output for the ICU but saved internally. One request per source can be saved internally.

An interrupt request that was being saved in the ICU is output when the ICU.IELSRn.IR flag is set to 0. Internally saved interrupt requests are automatically cleared under normal conditions. They can also be cleared by writing 0 to the interrupt enable bit within the given peripheral module.

36.15 State of Registers when Issuing each Condition

The IIC has two dedicated resets, IIC reset and internal reset. Table 36.11 shows the register states when issuing each condition.

Table 36.11 Register states when issuing each condition (1 of 2)

Registers		Reset	IIC reset (ICE = 0, IICRST = 1)	Internal reset (ICE = 1, IICRST = 1)	Start or restart condition detection	Stop condition detection
ICCR1	ICE, IICRST	In reset	Saved	Saved	Saved	Saved
	SCLO, SDAO		In reset	In reset		
	Others			Saved		
ICCR2	BBSY	In reset	In reset	Saved	Set	In reset
	ST, RS			In reset	In reset	Saved
	SP					In reset
	TRS				Set or saved	
	MST					

Table 36.10 中断源

Symbol	中断源	中断标志	DMAC/DTC activation	中断条件
IICn_EEI*5	传输错误或事件发生	AL	不可能	AL = 1, ALIE = 1
		NACKF		NACKF = 1, NAKIE = 1
		TMOF		TMOF = 1, TMOIE = 1
		START		START = 1, STIE = 1
		STOP		STOP = 1, SPIE = 1
IICn_RXI*2, *5	接收数据已满	RDRF	Possible	RDRF = 1, RIE = 1
IICn_TXI*1, *5	传输数据为空	TDRE	Possible	TDRE = 1, TIE = 1
IICn_TEI*3, *5	发射端	TEND	不可能	TEND = 1, TEIE = 1
IIC0_WUI*4	唤醒功能期间的从机地址匹配	WUF	不可能	从地址匹配 从机接收完成 RWAK operation ASY0 = 1 WUIE = 1

Note: CPU执行外围模块的写指令与实际写入模块之间存在延迟。当一个中断标志被清除或屏蔽时，再次读取相关标志，检查清除或屏蔽是否完成，然后从中断处理返回。不这样做会产生重复处理同一中断的可能性。

Note 1. 因为IICn_TXI是边沿检测，所以不需要清零。此外，当发送数据写入ICDRT或检测到停止条件（ICSR2中的STOP标志=1）时，ICSR2中的TDRE标志（IICn_TXI的条件）自动设置为0。
Note 2. 因为IICn_RXI是边沿检测，所以不需要清零。此外，从ICDRR读取数据时，ICSR2中的RDRF标志（IICn_RXI的条件）自动设置为0。
Note 3. 使用IICn_TEI中断时，在IICn_TEI中断处理中清除ICSR2中的TEND标志。当发送数据写入ICDRT或检测到停止条件（ICSR2中的STOP标志=1）时，ICSR2中的TEND标志自动设置为0。
Note 4. 只有通道0有唤醒功能，所以IIC0_WUI仅适用于通道0。
Note 5. 通道号（n=0到2）。

在中断处理期间清除或屏蔽每个标志。

36.14.1 IICn_TXI和IICn_RXI中断的缓冲区操作

如果在相关的IR标志为1时满足产生IICn_TXI或IICn_RXI中断的条件，则中断请求不会输出给ICU，而是在内部保存。每个源的一个请求可以在内部保存。

当ICU.IELSRn.IR标志设置为0时，会输出保存在ICU中的中断请求。在正常情况下，内部保存的中断请求会自动清除。也可以通过将0写入给定外设模块中的中断使能位来清除它们。

36.15 发布每个条件时的注册状态

IIC有两个专用复位，IIC复位和内部复位。表36.11显示了发出每个条件时的寄存器状态。

Table 36.11 发出每个条件时注册状态（2个中的1个）

Registers		Reset	IIC reset (ICE = 0, IICRST = 1)	内部复位（ICE=1，IICRST=1）	启动或重启条件检测	停止条件检测
ICCR1	ICE, IICRST	复位中	Saved	Saved	Saved	Saved
	SCLO, SDAO		复位中	复位中		
	Others			Saved		
ICCR2	BBSY	复位中	复位中	Saved	Set	复位中
	ST, RS			复位中	复位中	Saved
	SP					复位中
	TRS				设置或保存	
	MST					

Table 36.11 Register states when issuing each condition (2 of 2)

Registers		Reset	IIC reset (ICE = 0, IICRST = 1)	Internal reset (ICE = 1, IICRST = 1)	Start or restart condition detection	Stop condition detection
ICMR1	BC[2:0]	In reset	In reset	In reset	In reset	Saved
	Others			Saved	Saved	
ICMR2		In reset	In reset	Saved	Saved	Saved
ICMR3	ACKBIT	In reset	In reset	Saved	Saved	In reset
	Others					Saved
ICFER		In reset	In reset	Saved	Saved	Saved
ICSER		In reset	In reset	Saved	Saved	Saved
ICIER		In reset	In reset	Saved	Saved	Saved
ICSR1		In reset	In reset	In reset	Saved	In reset
ICSR2	TEND	In reset	In reset	In reset	Saved	In reset
	TDRE				Set or saved	
	START				Set	
	STOP				Saved	Set
	Others				Saved	Saved
ICWUR		In reset	In reset	Saved	Saved	Saved
SARL0, SARL1, SARL2 SARU0, SARU1, SARU2		In reset	In reset	Saved	Saved	Saved
ICBRH, ICBRL		In reset	In reset	Saved	Saved	Saved
ICDRT		In reset	In reset	Saved	Saved	Saved
ICDRR		In reset	In reset	Saved	Saved	Saved
ICDRS		In reset	In reset	In reset	Saved	Saved
Timeout function		In reset	In reset	In reset	Operating	Operating
Bus free time measurement		In reset	In reset	Operating	Operating	Operating
ICWUR2	WUSEN	In reset	In reset	Saved	Saved	Saved
	Others					Saved or Set or Reset

36.16 Output to the Event Link Controller (ELC)

The IIC0 to IIC2 modules handle event output for the ELC for the following sources:

(1) Transfer error event

When a transfer error event occurs, the associated event signal can be output to another module by the ELC.

(2) Receive data full

When a receive data register becomes full, the associated event signal can be output to another module by the ELC.

(3) Transmit data empty

When a transmit data register becomes empty, the associated event signal can be output to another module by the ELC.

(4) Transmit end

On completion of transfer, the associated event signal can be output to another module by the ELC.

36.16.1 Interrupt Handling and Event Linking

Each of the IIC interrupt types (see Table 36.10) has an enable bit to control enabling and disabling of the associated interrupt signal. An interrupt request signal is output to the CPU when an interrupt source condition is satisfied while the associated enable bit is set.

The associated event link output signals are sent to other modules as event signals by the ELC when the interrupt source

Table 36.11 发布每个条件时注册状态（2个中的2个）

Registers		Reset	IIC reset (ICE = 0, IICRST = 1)	内部复位（ICE=1，IICRST=1）	启动或重启条件检测	停止条件检测
ICMR1	BC[2:0]	复位中	复位中	复位中	复位中	Saved
	Others			Saved	Saved	
ICMR2		复位中	复位中	Saved	Saved	Saved
ICMR3	ACKBIT	复位中	复位中	Saved	Saved	复位中
	Others					Saved
ICFER		复位中	复位中	Saved	Saved	Saved
ICSER		复位中	复位中	Saved	Saved	Saved
ICIER		复位中	复位中	Saved	Saved	Saved
ICSR1		复位中	复位中	复位中	Saved	复位中
ICSR2	TEND	复位中	复位中	复位中	Saved	复位中
	TDRE				设置或保存	
	START				Set	
	STOP				Saved	Set
	Others				Saved	Saved
ICWUR		复位中	复位中	Saved	Saved	Saved
SARL0, SARL1, SARL2 SARU0, SARU1, SARU2		复位中	复位中	Saved	Saved	Saved
ICBRH, ICBRL		复位中	复位中	Saved	Saved	Saved
ICDRT		复位中	复位中	Saved	Saved	Saved
ICDRR		复位中	复位中	Saved	Saved	Saved
ICDRS		复位中	复位中	复位中	Saved	Saved
超时功能		复位中	复位中	复位中	Operating	Operating
公交车空闲时间测量		复位中	复位中	Operating	Operating	Operating
ICWUR2	WUSEN	复位中	复位中	Saved	Saved	Saved
	Others					保存或设置或重置

36.16 输出到事件链接控制器(ELC)

IIC0到IIC2模块为以下源处理ELC的事件输出：

(1) 传输错误事件

当发生传输错误事件时，ELC可以将相关事件信号输出到另一个模块。

(2) 接收数据已满

当接收数据寄存器变满时，ELC可以将相关的事件信号输出到另一个模块。

(3) 传输数据为空

当发送数据寄存器变为空时，ELC可以将相关的事件信号输出到另一个模块。

(4) 发射端

传输完成后，ELC可以将相关的事件信号输出到另一个模块。

36.16.1 中断处理和事件链接

每种IIC中断类型（见表36.10）都有一个启用位来控制相关中断信号的启用和禁用。当相关的使能位设置时，中断源条件成立时，将向CPU输出中断请求信号。

当中断源发生时，关联的事件链接输出信号由ELC作为事件信号发送到其他模块

conditions are satisfied, regardless of the interrupt enable bit settings. For details on interrupt sources, see Table 36.10.

36.17 Usage Notes

36.17.1 Settings for the Module-Stop Function

IIC operation can be disabled or enabled using Module Stop Control Register B (MSTPCRB). The IIC is initially stopped after reset. Releasing the module-stop state enables access to the registers. For details, see section 11, Low Power Modes.

36.17.2 Starting Transfer after an Interrupt Occurrence

If the IR flag associated with the IIC interrupt is 1 when transfer is started (ICCR1.ICE bit = 1), follow the procedure shown here to clear interrupts before enabling operations. Starting transfer with the IR flag set to 1 while the ICCR1.ICE bit is 1 leads to an interrupt request being internally saved after transfer starts, and this can lead to unanticipated behavior of the IR flag.

To clear interrupts before starting transfer:

1. Confirm that the ICCR1.ICE bit is 0.
2. Set the relevant interrupt enable bits, such as ICIER.TIE, in the peripheral function to 0.
3. Read the relevant interrupt enable bits, such as ICIER.TIE, in the peripheral function and confirm that their value is 0.
4. Set the IR flag to 0.

无论中断使能位设置如何，条件都满足。有关中断源的详细信息，请参见表36.10。

36.17 使用说明

36.17.1 模块停止功能的设置

可以使用模块停止控制寄存器B(MSTPCRB)禁用或启用IIC操作。IIC在复位后最初停止。释放模块停止状态可以访问寄存器。有关详细信息，请参阅第11节，低功耗模式。

36.17.2 发生中断后开始传输

如果在传输开始时与IIC中断相关的IR标志为1（ICCR1.ICE位=1），请按照此处所示的步骤在使能操作之前清除中断。在ICCR1.ICE位为1时将IR标志设置为1开始传输会导致在传输开始后内部保存中断请求，这可能导致IR标志的意外行为。

在开始传输之前清除中断：

1.确认ICCR1.ICE位为0。

2.设置外设功能中相关的中断使能位，如ICIER.TIE为0。

3.读取外设功能中相关的中断使能位，如ICIER.TIE，确认其值为0。

4.将IR标志设置为0。

37. Controller Area Network (CAN) Module

37.1 Overview

The Controller Area Network (CAN) module uses a message-based protocol to receive and transmit data between multiple slaves and masters in electromagnetically noisy applications. The module complies with the ISO 11898-1 (CAN 2.0A/CAN 2.0B) standard and supports up to 32 mailboxes, which can be configured for transmission or reception in normal mailbox and FIFO modes. Both standard (11-bit) and extended (29-bit) messaging formats are supported.

Table 37.1 lists the CAN module specifications and Figure 37.1 shows a block diagram. The CAN module requires an additional external CAN transceiver.

Table 37.1 CAN module specifications (1 of 2)

Parameter	Specifications
Data transfer rate	ISO11898-1-compliant for standard and extended frames
Bit rate	Data transfer rate programmable up to 1 Mbps (fCAN ≥ 8 MHz) fCAN: CAN clock source
Message box	32 mailboxes, with two selectable mailbox modes • Normal mode: 32 mailboxes independently configurable for either transmission or reception • FIFO mode: 24 mailboxes independently configurable for either transmission or reception, with remaining mailboxes used for receive and transmit 4-stage FIFOs.
Reception	• Support for data frame and remote frame reception • Reception ID format selectable to only standard ID, only extended ID, or mixed IDs • Programmable one-shot reception function • Selectable between overwrite mode (unread message overwritten) and overrun mode (unread message saved) • Reception complete interrupt independently enabled or disabled for each mailbox.
Acceptance filter	• Eight acceptance masks (one for every four mailboxes) • Masks independently enabled or disabled for each mailbox.
Transmission	• Support for data frame and remote frame transmission • Transmission ID format selectable to only standard ID, only extended ID, or mixed IDs) • Programmable one-shot transmission function • Broadcast messaging function • Priority mode selectable based on message ID or mailbox number • Support for transmission request abort, with abort completion comfirmable in status flag • Transmission complete interrupt independently enabled or disabled for each mailbox.
Mode transition for bus-off recovery	Mode transition for the recovery from the bus-off state selectable to: • ISO11898-1 specification-compliant • Automatic invoking of CAN halt mode on bus-off entry • Automatic invoking of CAN halt mode on bus-off end • Invoking of CAN halt mode through the software • Transition to error-active state through the software.
Error status monitoring	• Monitoring of CAN bus errors, including stuff error, form error, ACK error, 15-bit CRC error, bit error, and ACK delimiter error • Detection of transition to error states, including error-warning, error-passive, bus-off entry, and bus-off recovery • Supports reading of error counters.
Time stamping	• Time stamp function using a 16-bit counter • Reference clock selectable to 1-bit, 2-bit, 4-bit, and 8-bit time periods.
Interrupt function	Supports five interrupt sources: reception complete, transmission complete, receive FIFO, transmit FIFO, and error interrupts
CAN sleep mode	CAN clock stopped to reduce power consumption
Software support unit	Three software support units: • Acceptance filter support • Mailbox search support, including receive mailbox search, transmit mailbox search, and message lost search • Channel search support.
CAN clock source	PCLKB or CANMCLK

37. 控制器局域网(CAN)模块

37.1 Overview

控制器局域网(CAN)模块使用基于消息的协议在电磁噪声应用中的多个从机和主机之间接收和传输数据。该模块符合ISO11898-1(CAN2.0ACAN2.0B)标准，最多支持32个邮箱，可配置为普通邮箱和FIFO模式下的发送或接收。支持标准（11位）和扩展（29位）消息格式。

表37.1列出了CAN模块规格，图37.1显示了框图。CAN模块需要额外的外部CAN收发器。

Table 37.1 CAN模块规格(1of2)

Parameter	Specifications
数据传输率	标准和扩展框架符合ISO11898-1
比特率	数据传输速率可编程高达1Mbps(fCAN 8MHz)fCAN：CAN时钟源
消息框	32个邮箱，有两种可选择的邮箱模式 普通模式：32个邮箱可独立配置为发送或接收 FIFO模式：24个邮箱可独立配置为发送或接收，其余邮箱用于接收和发送4级FIFO。
Reception	支持数据帧和远程帧接收 接收ID格式可选择仅标准ID、仅扩展ID或混合ID 可编程一次性接收功能可选择覆盖模式（未读消息覆盖）和溢出模式（未读消息已保存）） 为每个邮箱独立启用或禁用接收完成中断。
验收过滤器	八个接受掩码（每四个邮箱一个） 为每个邮箱独立启用或禁用掩码。
Transmission	支持数据帧和远程帧传输 传输ID格式可选择仅标准ID、仅扩展ID或混合ID） 可编程一次性传输功能 广播消息功能 可根据消息ID或邮箱号选择优先模式 支持传输请求中止，状态标志中可确认中止完成 为每个邮箱独立启用或禁用传输完成中断。
总线关闭恢复的模式转换	从总线关闭状态恢复的模式转换可选择： 符合ISO11898-1规范 在总线关闭进入时自动调用CAN暂停模式 在总线关闭结束时自动调用CAN暂停模式 调用CAN暂停通过软件模式 通过软件转换到错误激活状态。
错误状态监控	监控CAN总线错误，包括填充错误、格式错误、ACK错误、15位CRC错误、位错误和ACK分隔符错误 检测到错误状态的转换，包括错误警告、错误被动、总线关闭入口和总线关闭恢复 支持读取错误计数器。
时间戳	使用16位计数器的时间戳功能 可选择1位、2位、4位和8位时间周期的参考时钟。
中断功能	支持五种中断源：接收完成、发送完成、接收FIFO、发送FIFO、错误中断
CAN睡眠模式	CAN时钟停止以降低功耗
软件支持单位	三个软件支持单元： 接受过滤器支持 邮箱搜索支持，包括接收邮箱搜索、发送邮箱搜索和邮件丢失搜索渠道搜索支持。
CAN时钟源	PCLKB or CANMCLK

Table 37.1 CAN module specifications (2 of 2)

Parameter	Specifications
Test mode	Three test modes available for evaluation purposes: • Listen-only mode • Self-test mode 0 (external loopback) • Self-test mode 1 (internal loopback).
Module-stop function	Module-stop state can be set to reduce power consumption

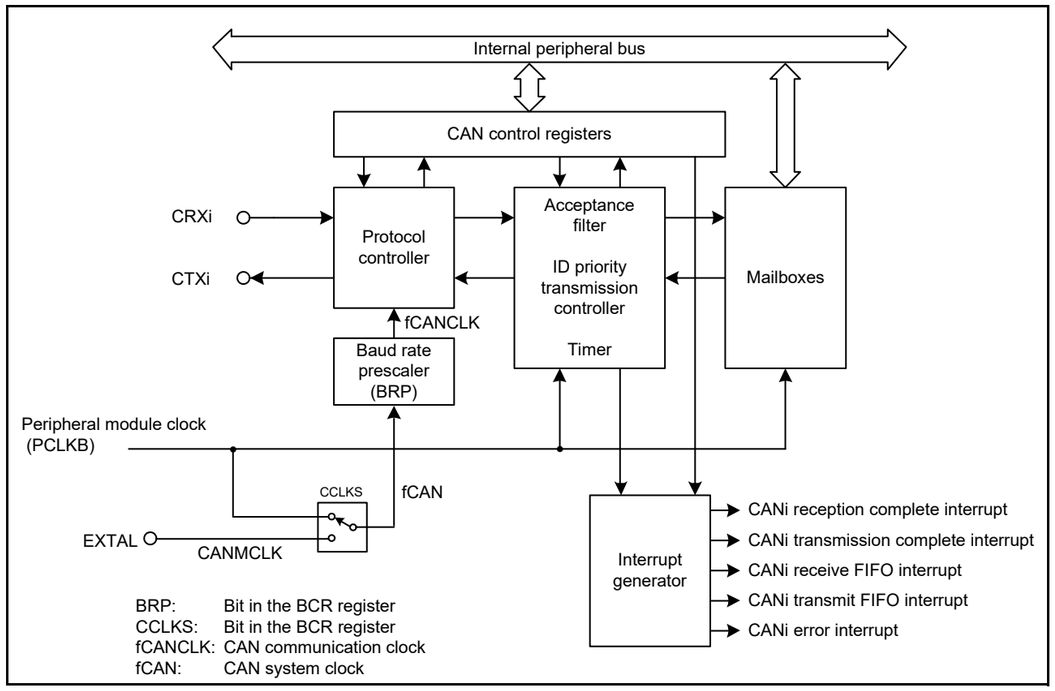


Figure 37.1 CAN module block diagram (i = 0, 1)

The CAN module includes the following blocks:

- CAN input and output pins
  CRXi and CTXi, where i = 0, 1
- Protocol controller
  Handles CAN protocol processing such as bus arbitration, bit timing during transmission and reception, stuffing, and error handling.
- Mailboxes
  Consists of 32 mailboxes, which can be configured as either transmit or receive. Each mailbox has an individual ID, data length code (DLC), data field (8 bytes), and time stamp.
- Acceptance filter
  Performs filtering of received messages. MKR0 to MKR7 are used for the filtering process.
- Timer
  Used for the time stamp function. The timer value when a message is stored in the mailbox is written as the time stamp value.
- Interrupt generator
  Generates five types of interrupts:
  - CANi reception complete interrupt

Table 37.1 CAN模块规格（2个中的2个）

Parameter	Specifications
测试模式	三种测试模式可用于评估目的： 只听模式 自测模式0（外部环回） 自测模式1（内部环回）。
Module-stop function	可设置模块停止状态以降低功耗

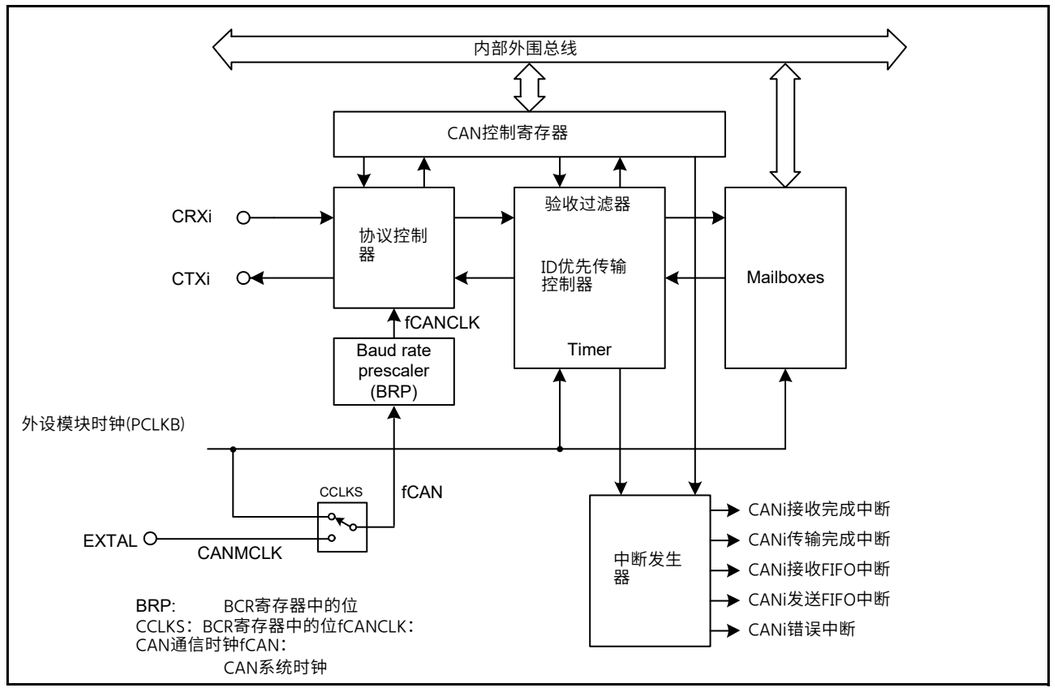


Figure 37.1 CAN模块框图(i=0 1)

CAN模块包括以下模块：

- CAN输入和输出引脚
  CRXi和CTXi，其中i=0 1
- 协议控制器处理CAN协议处理，例如总线仲裁、发送和接收期间的位时序、填充和错误处理。
- Mailboxes
  包含32个邮箱，可配置为发送或接收。每个邮箱都有一个单独的ID、数据长度代码(DLC)、数据字段（8个字节）和时间戳。
- 验收过滤器
  对收到的消息执行过滤。MKR0到MKR7用于过滤过程。
- Timer
  用于时间戳功能。将消息存储在邮箱中时的计时器值作为时间戳值写入。
- 中断发生器
  产生五种类型的中断：
  - CANi接收完成中断

- CANi transmission complete interrupt
- CANi receive FIFO interrupt
- CANi transmit FIFO interrupt
- CANi error interrupt.

The CAN module communicates on the pins listed in Table 37.2. These pins are multiplexed with other signals on the MCU. For details, see section 20, I/O Ports.

Table 37.2 CAN module I/O pins

Pin name	I/O	Function
CRX0	Input	Data receive pin
CTX0	Output	Data transmit pin
CRX1	Input	Data receive pin
CTX1	Output	Data transmit pin

37.2 Register Descriptions

37.2.1 Control Register (CTLR)

Address(es): CAN0.CTLR 4005 0840h, CAN1.CTLR 4005 1840h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	RBOC	BOM[1:0]		SLPM	CANM[1:0]		TSPS[1:0]		TSRC	TPM	MLM	IDFM[1:0]		MBM
Value after reset:	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	MBM	CAN Mailbox Mode Select*1	0: Normal mailbox mode 1: FIFO mailbox mode.	R/W
b2, b1	IDFM[1:0]	ID Format Mode Select *1	b2 b1 0 0: Standard ID mode All mailboxes, including FIFO mailboxes, handle only standard IDs 0 1: Extended ID mode All mailboxes, including FIFO mailboxes, handle only extended IDs 1 0: Mixed ID mode All mailboxes, including FIFO mailboxes, handle both standard and extended IDs. In normal mailbox mode, use the associated IDE bit to differentiate standard and extended IDs. In FIFO mailbox mode, the associated IDE bits are used for mailboxes 0 to 23, the IDE bits in FIDCR0 and FIDCR1 are used for the receive FIFO, and the IDE bit associated with mailbox 24 is used for the transmit FIFO. 1 1: Setting prohibited.	R/W
b3	MLM	Message Lost Mode Select*1	0: Overwrite mode 1: Overrun mode.	R/W
b4	TPM	Transmission Priority Mode Select*1	0: ID priority transmit mode 1: Mailbox number priority transmit mode.	R/W
b5	TSRC	Time Stamp Counter Reset Command*4	0: Nothing occurred 1: Reset.*3	R/W
b7, b6	TSPS[1:0]	Time Stamp Prescaler Select*1	b7 b6 0 0: Every bit time 0 1: Every 2-bit time 1 0: Every 4-bit time 1 1: Every 8-bit time.	R/W

- CANi传输完成中断
- CANi接收FIFO中断
- CANi发送FIFO中断
- CANi错误中断。

CAN模块在表37.2中列出的引脚上进行通信。这些引脚与其他信号复用
单片机。有关详细信息，请参阅第20节，IO端口。

Table 37.2 CAN模块IO引脚

引脚名称	I/O	Function
CRX0	Input	数据接收引脚
CTX0	Output	数据传输引脚
CRX1	Input	数据接收引脚
CTX1	Output	数据传输引脚

37.2 注册说明

37.2.1 控制寄存器(CTLR)

Address(es): CAN0.CTLR 4005 0840h, CAN1.CTLR 4005 1840h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	RBOC	BOM[1:0]		SLPM	CANM[1:0]		TSPS[1:0]		TSRC	TPM	MLM	IDFM[1:0]		MBM
重置后的值：	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	MBM	CAN邮箱模式 Select*1	0：普通邮箱模式1：FIF O邮箱模式。	R/W
b2, b1	IDFM[1:0]	ID格式模式选择*1	b2b100：标准ID模式 所有邮箱，包括FIFO邮箱，只处理标准ID01：扩展ID模式 所有邮箱，包括FIFO邮箱，只处理扩展ID10：混合ID模式 所有邮箱，包括FIFO邮箱，都处理标准ID和扩展ID。在普通邮箱模式下，使用相关的IDE位来区分标准ID和扩展ID。在FIFO邮箱模式下，相关的IDE位用于邮箱0到23，FIDCR0和FIDCR1中的IDE位用于接收FIFO，与邮箱24相关的IDE位用于发送FIFO。11：禁止设置。	R/W
b3	MLM	消息丢失模式 Select*1	0：覆盖模式1： 溢出模式。	R/W
b4	TPM	传输优先级 Mode Select*1	0：ID优先发送模式1：邮箱号码优先发送 模式。	R/W
b5	TSRC	时间戳计数器 Reset Command*4	0：未发生任何事情 1：复位。*3	R/W
b7, b6	TSPS[1:0]	时间戳预分频器 Select*1	b7b600：每比特时间 01：每2比特时间10 ：每4比特时间11：每 8比特时间。	R/W

Bit	Symbol	Bit name	Description	R/W
b9, b8	CANM[1:0]	CAN Operating Mode Select*5	b9 b8 0 0: CAN operation mode 0 1: CAN reset mode 1 0: CAN halt mode 1 1: CAN reset mode (forced transition).	R/W
b10	SLPM	CAN Sleep Mode*5,*6	0: All other modes 1: CAN sleep mode.	R/W
b12, b11	BOM[1:0]	Bus-Off Recovery Mode*1	b12 b11 0 0: Normal mode (ISO11898-1-compliant) 0 1: Enter CAN halt mode automatically on entering bus-off state 1 0: Enter CAN halt mode automatically on end of bus-off state 1 1: Enter CAN halt mode during bus-off recovery period through a software request.	R/W
b13	RBOC	Forcible Return from Bus-Off*2	0: Nothing occurred 1: Forced return from bus-off state.*3	R/W
b15, b14	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Write to the BOM[1:0], TSPS[1:0], TPM, MLM, IDFM[1:0], and MBM bits in CAN reset mode.
Note 2. Set the RBOC bit to 1 in the bus-off state.
Note 3. This bit automatically is set to 0 after being set to 1. It should read as 0.
Note 4. Set the TSRC bit to 1 in CAN operation mode.
Note 5. When the CANM[1:0] and SLPM bits are changed, check STR to ensure that the mode is switched. Do not change the CANM[1:0] bits or SLPM bit until the mode is switched.
Note 6. Write to the SLPM bit in CAN reset mode or CAN halt mode. When changing the SLPM bit, write 0 or 1 to only the SLPM bit.

MBM bit (CAN Mailbox Mode Select)

When the MBM bit is 0 (normal mailbox mode), mailboxes 0 to 31 are configured as transmit or receive mailboxes.
When the MBM bit is 1 (FIFO mailbox mode), mailboxes 0 to 23 are configured as transmit or receive mailboxes. Mailboxes 24 to 27 are configured as a transmit FIFO, and mailboxes 28 to 31 are configured as a receive FIFO. Transmit data is written into mailbox 24, the window mailbox for the transmit FIFO. Receive data is read from mailbox 28, the window mailbox for the receive FIFO.

Table 37.3 lists the mailbox configuration.

IDFM[1:0] bits (ID Format Mode Select)

The IDFM[1:0] bits specify the ID format.

MLM bit (Message Lost Mode Select)

The MLM bit specifies the operation when a new message is captured in the unread mailbox. Overwrite mode or overrun mode can be selected. In both cases, the mode applies to all mailboxes, including the receive FIFO.

When the MLM bit is 0, all mailboxes are set to overwrite mode. Any new message received overwrites the pre-existing message.

When the MLM bit is 1, all mailboxes are set to overrun mode. Any new message received does not overwrite the pre-existing message, and it is discarded.

TPM bit (Transmission Priority Mode Select)

The TPM bit specifies the priority when transmitting messages. ID priority transmit mode or mailbox number transmit mode can be selected. All mailboxes are set for either ID priority transmission or mailbox number priority transmission.

When TPM is 0, ID priority transmit mode is selected and transmission priority is arbitrated as defined in the ISO11898-1 CAN specification. In ID priority transmit mode, mailboxes 0 to 31 (in normal mailbox mode), and mailboxes 0 to 23 (in FIFO mailbox mode), and the transmit FIFO are compared for the IDs of mailboxes configured for transmission. If two or more mailbox IDs are the same, the mailbox with the smaller number has higher priority.

Only the next message to be transmitted from the transmit FIFO is included in the transmission arbitration. If a FIFO message is being transmitted, the next pending message within the transmit FIFO is included in the transmission arbitration.

When TPM is 1, mailbox number transmit mode is selected and the transmit mailbox with the smallest mailbox number

Bit	Symbol	位名称	Description	R/W
b9, b8	CANM[1:0]	CAN操作模式 Select*5	b9b800：CAN操作模式01：CAN复位模式10：CAN暂停模式11：CAN复位模式（强制转换）。	R/W
b10	SLPM	CAN睡眠模式*5 *6	0：所有其他模式1 ：CAN睡眠模式。	R/W
b12, b11	BOM[1:0]	Bus-Off Recovery Mode*1	b12b1100：正常模式（符合ISO11898-1）01：进入总线关闭状态时自动进入CAN停止模式10：在总线关闭状态结束时自动进入CAN停止模式11：进入CAN停止模式在总线关闭恢复期间通过软件请求。	R/W
b13	RBOC	强行返回 Bus-Off*2	0：什么都没有发生1：从总线关闭状态强制返回。*3	R/W
b15, b14	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 在CAN复位模式下写入BOM[1:0]、TSPS[1:0]、TPM、MLM、IDFM[1:0]和MBM位。
Note 2. 在总线关闭状态下将RBOC位设置为1。
Note 3. 该位在设置为1后自动设置为0。它应该读为0。
Note 4. 在CAN操作模式下将TSRC位设置为1。
Note 5. 当CANM[1:0]和SLPM位改变时，检查STR以确保模式切换。不要改变CANM[1:0]位或SLPM位，直到模式切换。
Note 6. 在CAN复位模式或CAN暂停模式下写入SLPM位。更改SLPM位时，仅向SLPM位写入0或1。

MBM位（CAN邮箱模式选择）

当MBM位为0（正常邮箱模式）时，邮箱0到31被配置为发送或接收邮箱。
当MBM位为1（FIFO邮箱模式）时，邮箱0到23被配置为发送或接收邮箱。
邮箱24到27配置为发送FIFO，邮箱28到31配置为接收FIFO。
发送数据写入邮箱24，即发送FIFO的窗口邮箱。接收数据从邮箱28中读取，该邮箱是接收FIFO的窗口邮箱。

表37.3列出了邮箱配置。

IDFM[1:0]位（ID格式模式选择）

IDFM[1:0]位指定ID格式。

MLM位（消息丢失模式选择）

MLM位指定在未读邮箱中捕获新消息时的操作。可以选择覆盖模式或溢出模式。在这两种情况下，该模式都适用于所有邮箱，包括接收FIFO。

当MLM位为0时，所有邮箱都设置为覆盖模式。收到的任何新消息都会覆盖先前存在的消息。

当MLM位为1时，所有邮箱都设置为溢出模式。收到的任何新消息都不会覆盖先前存在的消息，并且会被丢弃。

TPM位（传输优先模式选择）

TPM位指定传输消息时的优先级。可选择ID优先传输模式或邮箱号码传输模式。所有信箱都设置为ID优先传输或信箱号码优先传输。

当TPM为0时，选择ID优先传输模式，传输优先级按照ISO118981CAN规范中的定义进行仲裁。在ID优先传输模式下，邮箱0到31（在普通邮箱模式下）和邮箱0到23（在FIFO邮箱模式下）和传输FIFO会针对配置为传输的邮箱ID进行比较。如果两个或多个邮箱ID相同，则编号较小的邮箱优先级较高。

只有从发送FIFO发送的下一条消息包含在发送仲裁中。如果正在发送FIFO消息，则发送FIFO中的下一个待处理消息将包含在发送仲裁中。

TPM为1时，选择邮箱号发送方式，发送邮箱号最小的邮箱

has the highest priority. In FIFO mailbox mode, the transmit FIFO has lower priority than normal mailboxes (0 to 23).

TSRC bit (Time Stamp Counter Reset Command)

The TSRC bit resets the time stamp counter. When it is set to 1, TSR is set to 0000h. TSRC is set to 0 automatically.

TSPS[1:0] bits (Time Stamp Prescaler Select)

The TSPS[1:0] bits select the prescaler for the time stamp. The reference clock for the time stamp can be selected to 1-bit, 2-bit, 4-bit, or 8-bit time periods.

CANM[1:0] bits (CAN Operating Mode Select)

The CANM[1:0] bits select one of the following modes for the CAN module: CAN operation mode, CAN reset mode, or CAN halt mode. CAN sleep mode is set in the SLPM bit. For details, see section 37.3, Operation Modes.

When the CAN module enters CAN halt mode based on the BOM[1:0] setting, the CANM[1:0] bits are automatically set to 10b.

SLPM bit (CAN Sleep Mode)

When the SLPM bit is set to 1, the CAN module enters CAN sleep mode. When the SLPM bit is set to 0, the CAN module exits CAN sleep mode. For details, see section 37.3, Operation Modes.

BOM[1:0] bits (Bus-Off Recovery Mode)

The BOM[1:0] bits select bus-off recovery mode for the CAN module.

When the BOM[1:0] bits are 00b, the recovery from bus-off is compliant with the ISO11898-1 specification. The CAN module recovers CAN communication (error-active state) after detecting 11 consecutive recessive bits 128 times. A bus-off recovery interrupt request occurs when recovering from bus-off.

When the BOM[1:0] bits are 01b and the CAN module reaches the bus-off state, the CANM[1:0] bits in CTLR set 10b to enter CAN halt mode. No bus-off recovery interrupt request occurs when recovering from bus-off, and TECR and RECR are set to 00h.

When the BOM[1:0] bits are 10b, the CANM[1:0] bits are set to 10b as soon as the CAN module reaches the bus-off state. The CAN module enters CAN halt mode after the recovery from the bus-off state, and after detecting 11 consecutive recessive bits 128 times. A bus-off recovery interrupt request occurs when recovering from bus-off, and TECR and RECR are set to 00h.

When the BOM[1:0] bits are 11b, the CAN module enters CAN halt mode by setting the CANM[1:0] bits to 10b while the CAN module is still in the bus-off state. No bus-off recovery interrupt request occurs when recovering from bus-off, and TECR and RECR are set to 00h. However, the interrupt does occur if the CAN module recovers from bus-off after detecting 11 consecutive recessive bits 128 times before the CANM[1:0] bits are set to 10b.

If the CPU requests an entry to CAN reset mode at the same time as the CAN module attempts to enter CAN halt mode (at bus-off entry when the BOM[1:0] bits are 01b, or at bus-off end when the BOM[1:0] bits are 10b), then the CPU request has higher priority.

RBOC bit (Forcible Return from Bus-Off)

When the RBOC bit is set to 1 in the bus-off state, the CAN module forcibly exits bus-off. It is set to 0 automatically, and the error state changes from bus-off to error-active. When the RBOC bit is set to 1, RECR and TECR clear to 00h and the BOST bit in STR is set to 0, indicating no bus-off state. The other registers remain unchanged when RBOC is set to 1. No bus-off recovery interrupt request occurs. Use the RBOC bit only when the BOM[1:0] bits are 00b (normal mode).

Table 37.3 Mailbox configuration

Mailbox	MBM bit = 0 (normal mailbox mode)	MBM bit = 1 (FIFO mailbox mode)*1 to *5
Mailboxes 0 to 23	Normal mailbox	Normal mailbox
Mailboxes 24 to 27		Transmit FIFO
Mailboxes 28 to 31		Receive FIFO

Note 1. The transmit FIFO is controlled by TFCR. The MCTL_TXj registers associated with mailboxes 24 to 27 are disabled. MCTL_TX24 to MCTL_TX27 cannot be used by the transmit FIFO.

具有最高优先级。在FIFO邮箱模式下，发送FIFO的优先级低于普通邮箱（0到23）。

TSRC位（时间戳计数器复位命令）

TSRC位复位时间戳计数器。当它设置为1时，TSR设置为0000h。TSRC自动设置为0。

TSPS[1:0]位（时间戳预分频器选择）

TSPS[1:0]位选择时间戳的预分频器。时间戳的参考时钟可以选择为1位、2位、4位或8位时间段。

CANM[1:0]位（CAN操作模式选择）

CANM[1:0]位为CAN模块选择以下模式之一：CAN操作模式、CAN复位模式或CAN暂停模式。CAN睡眠模式在SLPM位中设置。有关详细信息，请参阅第37.3节，操作模式。

当CAN模块根据BOM[1:0]设置进入CAN暂停模式时，CANM[1:0]位自动设置为10b。

SLPM位（CAN休眠模式）

当SLPM位设置为1时，CAN模块进入CAN睡眠模式。当SLPM位设置为0时，CAN模块退出CAN睡眠模式。有关详细信息，请参阅第37.3节，操作模式。

BOM[1:0]位（总线关闭恢复模式）

BOM[1:0]位选择CAN模块的总线关闭恢复模式。

当BOM[1:0]位为00b时，从总线关闭中恢复符合ISO11898-1规范。CAN模块在检测到11个连续隐性位128次后恢复CAN通信（错误激活状态）。从总线关闭中恢复时会出现总线关闭恢复中断请求。

当BOM[1:0]位为01b且CAN模块达到总线关闭状态时，CTLR中的CANM[1:0]位设置10b以进入CAN停止模式。总线关闭恢复时不产生总线关闭恢复中断请求，TECR和RECR设置为00h。

当BOM[1:0]位为10b时，CAN模块一到达总线关闭状态，CANM[1:0]位就会设置为10b。CAN模块从总线关闭状态恢复后，并在检测到11个连续的隐性位128次后进入CAN停止模式。总线关闭恢复时产生总线关闭恢复中断请求，TECR和RECR设置为00h。

当BOM[1:0]位为11b时，CAN模块通过将CANM[1:0]位设置为10b进入CAN停止模式，同时CAN模块仍处于总线关闭状态。总线关闭恢复时不产生总线关闭恢复中断请求，TECR和RECR设置为00h。但是，如果CAN模块在CANM[1:0]位设置为10b之前128次检测到11个连续隐性位后从总线关闭中恢复，则确实会发生中断。

如果CPU在CAN模块尝试进入CAN暂停模式的同时请求进入CAN复位模式（当BOM[1:0]位为01b时在总线关闭进入，或者当BOM[1:0]位为10b），则CPU请求具有更高的优先级。

RBOC位（从总线关闭强制返回）

当RBOC位在总线关闭状态下设置为1时，CAN模块强制退出总线关闭。它自动设置为0，错误状态从总线关闭变为错误激活。当RBOC位设置为1时，RECR和TECR清除为00h，并且STR中的BOST位设置为0，表示没有总线关闭状态。当RBOC设置为1时，其他寄存器保持不变。没有总线关闭恢复中断请求发生。仅当BOM[1:0]位为00b（正常模式）时才使用RBOC位。

Table 37.3 邮箱配置

Mailbox	MBM位=0（正常邮箱模式）	MBM位=1（FIFO邮箱模式）*1到*5
邮箱0到23	普通邮箱	普通邮箱
邮箱24至27		Transmit FIFO
邮箱28至31		Receive FIFO

Note 1. 发送FIFO由TFCR控制。与邮箱24到27关联的MCTL_TXj寄存器被禁用。发送FIFO不能使用MCTL_TX24到MCTL_TX27。

Note 2. The receive FIFO is controlled by RFCR. The MCTL_RXj registers associated with mailboxes 28 to 31 are disabled. MCTL_RX28 to MCTL_RX31 cannot be used by the receive FIFO.
Note 3. See the MIER_FIFO description for information on the FIFO interrupts.
Note 4. The bits in MKIVLR associated with mailboxes 24 to 31 are disabled. Set 0 to these bits.
Note 5. The transmit and receive FIFOs can be used for both data frames and remote frames.

37.2.2 Bit Configuration Register (BCR)

Address(es): CAN0.BCR 4005 0844h, CAN1.BCR 4005 1844h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	TSEG1[3:0]				—		BRP[9:0]									
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	SJW[1:0]		—	TSEG2[2:0]			—	—	—	—	—	—	—	CCLKS
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	CCLKS	CAN Clock Source Selection	0: PCLKB (generated by the PLL clock) 1: CANMCLK (generated by the main clock oscillator).	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b10 to b8	TSEG2[2:0]	Time Segment 2 Control	b10 b8 0 0 0: Setting prohibited 0 0 1: 2 Tq 0 1 0: 3 Tq 0 1 1: 4 Tq 1 0 0: 5 Tq 1 0 1: 6 Tq 1 1 0: 7 Tq 1 1 1: 8 Tq.	R/W
b11	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b13, b12	SJW[1:0]	Synchronization Jump Width Control	b13 b12 0 0: 1 Tq 0 1: 2 Tq 1 0: 3 Tq 1 1: 4 Tq.	R/W
b15, b14	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b25 to b16	BRP[9:0]	Baud Rate Prescaler Select *1	These bits set the frequency of the CAN communication clock (fCANCLK).	R/W
b27, b26	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b31 to b28	TSEG1[3:0]	Time Segment 1 Control	b31 b28 0 0 0 0: Setting prohibited 0 0 0 1: Setting prohibited 0 0 1 0: Setting prohibited 0 0 1 1: 4 Tq 0 1 0 0: 5 Tq 0 1 0 1: 6 Tq 0 1 1 0: 7 Tq 0 1 1 1: 8 Tq 1 0 0 0: 9 Tq 1 0 0 1: 10 Tq 1 0 1 0: 11 Tq 1 0 1 1: 12 Tq 1 1 0 0: 13 Tq 1 1 0 1: 14 Tq 1 1 1 0: 15 Tq 1 1 1 1: 16 Tq.	R/W

Tq: Time Quantum

Note 2. 接收FIFO由RFCR控制。与邮箱28到31关联的MCTL_RXj寄存器被禁用。MCTL_RX28到MCTL_RX31不能被接收FIFO使用。
Note 3. 有关FIFO中断的信息，请参见MIER_FIFO描述。
Note 4. MKIVLR中与邮箱24到31关联的位被禁用。将这些位设置为0。
Note 5. 发送和接收FIFO可用于数据帧和远程帧。

37.2.2 位配置寄存器(BCR)

Address(es): CAN0.BCR 4005 0844h, CAN1.BCR 4005 1844h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	TSEG1[3:0]				—		BRP[9:0]									
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	SJW[1:0]		—	TSEG2[2:0]			—	—	—	—	—	—	—	CCLKS
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	CCLKS	CAN时钟源 Selection	0：PCLKB（由PLL时钟产生）1：CANMCLK（由主时钟振荡器产生）。	R/W
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b10 to b8	TSEG2[2:0]	时间段2控制	b10b8000：禁止设置001：2Tq010：3Tq011：4Tq100：5Tq101：6Tq110：7Tq111：8Tq.	R/W
b11	—	Reserved	该位读取为0。写入值应为0。	R/W
b13, b12	SJW[1:0]	同步跳转宽度控制	b13 b12 0 0: 1 Tq 0 1: 2 Tq 1 0: 3 Tq 1 1: 4 Tq.	R/W
b15, b14	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b25 to b16	BRP[9:0]	Baud Rate Prescaler Select *1	这些位设置CAN通信时钟(fCANCLK)的频率。	R/W
b27, b26	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b31 to b28	TSEG1[3:0]	时间段1控制	b31b280000：禁止设置0001：禁止设置0010：禁止设置0011：4Tq0100：5Tq0101：6Tq0110：7Tq0111：8Tq1000：9Tq1001：10Tq1010：11Tq1011：12Tq1100：13Tq1101：14Tq1110：15Tq1111：16Tq。	R/W

Tq：时间量子

Note 1. Do not select a value less than or equal to 1 while the SCKSCR.CKSEL[2:0] bits are 011b (selecting the main clock oscillator).

For setting the bit timing, see section 37.4, Data Transfer Rate Configuration. Set BCR before entering CAN halt or operation mode from reset mode. After the setting is made once, this register can be written to in CAN reset or CAN halt mode. 32-bit read/write accesses must be performed carefully so as not to change bits [7:0].

CCLKS bit (CAN Clock Source Selection)

When the CCLKS bit is 0, the peripheral module clock (PCLKB) produced by the PLL frequency synthesizer is used as the CAN clock source (fCAN). When the CCLKS bit is 1, CANMCLK produced externally by the EXTAL pins is used as the CAN clock source (fCAN).

TSEG2[2:0] bits (Time Segment 2 Control)

The TSEG2[2:0] bits specify the length of phase buffer segment 2 (PHASE_SEG2) with a Tq value. A value from 2 to 8 Tq can be set. Set a value smaller than that of the TSEG1[3:0] bits.

SJW[1:0] bits (Synchronization Jump Width Control)

The SJW[1:0] bits specify the synchronization jump width with a Tq value. A value from 1 to 4 Tq can be set. Set a value smaller than or equal to that of the TSEG2[2:0] bits.

BRP[9:0] bits (Baud Rate Prescaler Select)

The BRP[9:0] bits set the frequency of the CAN communication clock (fCANCLK). The fCANCLK cycle is 1 Tq. If the setting is P (0 to 1023), the baud rate prescaler divides fCAN by P + 1.

TSEG1[3:0] bits (Time Segment 1 Control)

The TSEG1[3:0] bits specify the total length of the propagation time segment (PROP_SEG) and phase buffer segment 1 (PHASE_SEG1) with a time quantum (Tq) value. A value from 4 to 16 Tq can be set.

37.2.3 Mask Register k (MKRk) (k = 0 to 7)

Address(es): CAN0.MKR[0] 4005 0400h to CAN0.MKR[7] 4005 041Ch, CAN1.MKR[0] 4005 1400h to CAN1.MKR[7] 4005 141Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	SID[10:0]											EID[17:0]	
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	EID[17:0]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b17 to b0	EID[17:0]	Extended ID	0: Do not compare associated EID[17:0] bits 1: Compare associated EID[17:0] bits.	R/W
b28 to b18	SID[10:0]	Standard ID	0: Do not compare associated SID[10:0] bits 1: Compare associated SID[10:0] bits.	R/W
b31 to b29	—	Reserved	The read value is undefined. The write value should be 0.	R/W

For the mask function in FIFO mailbox mode, see section 37.6, Acceptance Filtering and Masking Functions.

Write to MKR0 to MKR7 in CAN reset mode or CAN halt mode.

EID[17:0] bits (Extended ID)

The EID[17:0] bits are the filter mask bits associated with the CAN extended ID bits. They are used to receive extended ID messages. When an EID[17:0] bit is set to 0, the received ID is not compared with the associated mailbox ID. When the EID[17:0] bits are set to 1, the received ID is compared with the associated mailbox ID.

Note 1. 当SCKSCR.CKSEL[2:0]位为011b（选择主时钟振荡器）时，请勿选择小于或等于1的值。

有关设置位时序，请参见第37.4节，数据传输速率配置。在从复位模式进入CAN停止或操作模式之前设置BCR。设置一次后，可在CAN复位或CAN停止模式下写入该寄存器。必须小心执行32位读写访问，以免更改位[7:0]。

CCLKS位（CAN时钟源选择）

当CCLKS位为0时，PLL频率合成器产生的外设模块时钟（PCLKB）用作CAN时钟源（fCAN）。当CCLKS位为1时，由EXTAL引脚从外部产生的CANMCLK用作CAN时钟源(fCAN)。

TSEG2[2:0]位（时间段2控制）

TSEG2[2:0]位用Tq值指定相位缓冲段2(PHASE_SEG2)的长度。一个从2到8的值可以设置Tq。设置一个小于TSEG1[3:0]位的值。

SJW[1:0]位（同步跳转宽度控制）

SJW[1:0]位用Tq值指定同步跳转宽度。可以设置1到4Tq的值。设置小于或等于TSEG2[2:0]位的值。

BRP[9:0]位（波特率预分频器选择）

BRP[9:0]位设置CAN通信时钟(fCANCLK)的频率。fCANCLK周期为1Tq。如果设置为P（0到1023），则波特率预分频器将fCAN除以P+1。

TSEG1[3:0]位（时间段1控制）

TSEG1[3:0]位用时间量(Tq)值指定传播时间段(PROP_SEG)和相位缓冲段1(PHASE_SEG1)的总长度。可以设置4到16Tq的值。

37.2.3 屏蔽寄存器k(MKRk)(k=0到7)

Address(es): CAN0.MKR[0] 4005 0400h to CAN0.MKR[7] 4005 041Ch, CAN1.MKR[0] 4005 1400h to CAN1.MKR[7] 4005 141Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	SID[10:0]											EID[17:0]	
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	EID[17:0]															
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b17 to b0	EID[17:0]	扩展ID	0：不比较关联的EID[17:0]位1：比较关联的EID[17:0]位。	R/W
b28 to b18	SID[10:0]	标准标识	0：不比较关联的SID[10:0]位1：比较关联的SID[10:0]位。	R/W
b31 to b29	—	Reserved	读取值未定义。写入值应为0。	R/W

对于FIFO邮箱模式下的屏蔽功能，请参见第37.6节，接受过滤和屏蔽功能。

在CAN复位模式或CAN暂停模式下写入MKR0至MKR7。

EID[17:0]位（扩展ID）

EID[17:0]位是与CAN扩展ID位相关的过滤器掩码位。它们用于接收扩展ID消息。当EID[17:0]位设置为0时，接收到的ID不会与关联的邮箱ID进行比较。当EID[17:0]位设置为1时，接收到的ID将与关联的邮箱ID进行比较。

SID[10:0] bits (Standard ID)

The SID[10:0] bits are the filter mask bits associated with the CAN standard ID bits. They are used to receive both standard ID and extended ID messages. When the SID[10:0] bits are set to 0, the received ID is not compared with the associated mailbox ID. When the SID[10:0] bits are set to 1, the received ID is compared with the associated mailbox ID.

37.2.4 FIFO Received ID Compare Registers 0 and 1 (FIDCR0 and FIDCR1)

Address(es): CAN0.FIDCR0 4005 0420h, CAN0.FIDCR1 4005 0424h, CAN1.FIDCR0 4005 1420h, CAN1.FIDCR1 4005 1424h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	IDE	RTR	—	SID[10:0]											EID[17:0]	
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	EID[17:0]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b17 to b0	EID[17:0]	Extended ID	Extended ID of the data and remote frames	R/W
b28 to b18	SID[10:0]	Standard ID	Standard ID of the data and remote frames	R/W
b29	—	Reserved	The read value is undefined. The write value should be 0.	R/W
b30	RTR	Remote Transmission Request	0: Data frame 1: Remote frame.	R/W
b31	IDE	ID Extension*1	0: Standard ID 1: Extended ID.	R/W

Note 1. The IDE bit is enabled when the CTLR.IDFM[1:0] bits are 10b (mixed ID mode). When the IDFM[1:0] bits are not 10b, only write 0 to IDE. It reads as 0.

FIDCR0 and FIDCR1 are enabled when the MBM bit in CTLR is set to 1 (FIFO mailbox mode). In this mode, the EID[17:0], SID[10:0], RTR, and IDE bits in mailbox 28 to mailbox 31 are disabled. Write to FIDCR0 and FIDCR1 in CAN reset mode or CAN halt mode. For information on using FIDCR0 and FIDCR1, see section 37.6, Acceptance Filtering and Masking Functions.

EID[17:0] bits (Extended ID)

The EID[17:0] bits set the extended ID of data frames and remote frames. They are used to receive extended ID messages.

SID[10:0] bits (Standard ID)

The SID[10:0] bits set the standard ID of data frames and remote frames. They are used to receive both standard ID and extended ID messages.

RTR bit (Remote Transmission Request)

The RTR bit sets the frame format to data frames or remote frames:

- When both RTR bits in FIDCR0 and FIDCR1 are set to 0, only data frames are received
- When both RTR bits in FIDCR0 and FIDCR1 are set to 1, only remote frames are received
- When the RTR bits in FIDCR0 and FIDCR1 are set to different values, both data frames and remote frames are received.

IDE bit (ID Extension)

The IDE bit sets the ID format to standard ID or extended ID. The IDE bit is enabled when the IDFM[1:0] bits in CTLR

SID[10:0]位（标准ID）

SID[10:0]位是与CAN标准ID位相关的过滤器掩码位。它们用于接收标准ID和扩展ID消息。当SID[10:0]位设置为0时，接收到的ID不会与关联的邮箱ID进行比较。当SID[10:0]位设置为1时，接收的ID将与关联的邮箱ID进行比较。

37.2.4 FIFO接收ID比较寄存器0和1（FIDCR0和FIDCR1）

Address(es): CAN0.FIDCR0 4005 0420h, CAN0.FIDCR1 4005 0424h, CAN1.FIDCR0 4005 1420h, CAN1.FIDCR1 4005 1424h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	IDE	RTR	—	SID[10:0]											EID[17:0]	
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	EID[17:0]															
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b17 to b0	EID[17:0]	扩展ID	数据和远程帧的扩展ID	R/W
b28 to b18	SID[10:0]	标准标识	数据和远程帧的标准ID	R/W
b29	—	Reserved	读取值未定义。写入值应为0。	R/W
b30	RTR	远程传输 Request	0：数据帧1：远程帧。	R/W
b31	IDE	身份扩展 *1	0：标准ID1：扩展ID。	R/W

Note 1. 当CTLR.IDFM[1:0]位为10b（混合ID模式）时，IDE位被使能。当IDFM[1:0]位不是10b时，只向IDE写入0。它读作0。

当CTLR中的MBM位设置为1（FIFO邮箱模式）时，FIDCR0和FIDCR1被使能。在此模式下，邮箱28到邮箱31中的EID[17:0]、SID[10:0]、RTR和IDE位被禁用。写入FIDCR0和FIDCR1中CAN复位模式或CAN暂停模式。有关使用FIDCR0和FIDCR1的信息，请参阅第37.6节，验收过滤和屏蔽功能。

EID[17:0]位（扩展ID）

EID[17:0]位设置数据帧和远程帧的扩展ID。它们用于接收扩展ID消息。

SID[10:0]位（标准ID）

SID[10:0]位设置数据帧和远程帧的标准ID。它们用于接收标准ID和扩展ID消息。

RTR位（远程传输请求）

RTR位将帧格式设置为数据帧或远程帧：

- 当FIDCR0和FIDCR1中的RTR位都设置为0时，只接收数据帧
- 当FIDCR0和FIDCR1中的RTR位都设置为1时，只接收远程帧
- 当FIDCR0和FIDCR1中的RTR位设置为不同的值时，数据帧和远程帧都被接收。

IDE位（ID扩展）

IDE位将ID格式设置为标准ID或扩展ID。当CTLR中的IDFM[1:0]位使能IDE位

are 10b (mixed ID mode):

- When both IDE bits in FIDCR0 and FIDCR1 are set to 0, only standard ID frames are received
- When both IDE bits in FIDCR0 and FIDCR1 are set to 1, only extended ID frames are received
- When the IDE bits in FIDCR0 and FIDCR1 are set to different values, both standard ID and extended ID frames are received.

37.2.5 Mask Invalid Register (MKIVLR)

Address(es): CAN0.MKIVLR 4005 0428h, CAN1.MKIVLR 4005 1428h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	MB31	MB30	MB29	MB28	MB27	MB26	MB25	MB24	MB23	MB22	MB21	MB20	MB19	MB18	MB17	MB16
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MB15	MB14	MB13	MB12	MB11	MB10	MB9	MB8	MB7	MB6	MB5	MB4	MB3	MB2	MB1	MB0
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b31 to b0	MB31 to MB0	Mask Invalid	0: Mask valid 1: Mask invalid.	R/W

Each bit in MKIVLR is associated with a mailbox of the same number. Bit [0] in MKIVLR corresponds to mailbox 0 (MB0), and bit [31] corresponds to mailbox 31 (MB31).*1

When a bit is set to 1, the associated acceptance mask register becomes invalid for the associated mailbox. When a mask invalid bit is set to 1, a message is received by the associated mailbox only if the receive message ID matches the mailbox ID exactly.

Write to MKIVLR in CAN reset or halt mode.

Note 1. Set bits [31:24] to 0 in FIFO mailbox mode.

37.2.6 Mailbox Register j (MBj_ID, MBj_DL, MBj_Dm, MBj_TS) (j = 0 to 31; m = 0 to 7)

Table 37.4 lists the CANi mailbox memory mapping, and Table 37.5 lists the CAN data frame configuration.

The value after reset of the CANi mailbox is undefined.

Write to MBj_ID, MBj_DL, MBj_Dm, and MBj_TS only when the related MCTL_TXj or MCTL_RXj register (j = 0 to 31) is 00h and the associated mailbox is not processing an abort request.

See Table 37.4 for detailed register addresses.

Table 37.4 CANi mailbox memory mapping (1 of 2)

Address		Message content
CAN0	CAN1	Memory mapping
4005 0200h + 16 × j + 0	4005 1200h + 16 × j + 0	IDE, RTR, SID10 to SID6
4005 0200h + 16 × j + 1	4005 1200h + 16 × j + 1	SID5 to SID0, EID17, EID16
4005 0200h + 16 × j + 2	4005 1200h + 16 × j + 2	EID15 to EID8
4005 0200h + 16 × j + 3	4005 1200h + 16 × j + 3	EID7 to EID0
4005 0200h + 16 × j + 4	4005 1200h + 16 × j + 4	—

是10b（混合ID模式）：

- 当FIDCR0和FIDCR1中的IDE位都设置为0时，只接收标准ID帧
- 当FIDCR0和FIDCR1中的IDE位都设置为1时，只接收扩展ID帧
- 当FIDCR0和FIDCR1中的IDE位设置为不同的值时，标准ID和扩展ID帧都会被接收。

37.2.5 屏蔽无效寄存器(MKIVLR)

Address(es): CAN0.MKIVLR 4005 0428h, CAN1.MKIVLR 4005 1428h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	MB31	MB30	MB29	MB28	MB27	MB26	MB25	MB24	MB23	MB22	MB21	MB20	MB19	MB18	MB17	MB16
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MB15	MB14	MB13	MB12	MB11	MB10	MB9	MB8	MB7	MB6	MB5	MB4	MB3	MB2	MB1	MB0
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b31 to b0	MB31 to MB0	掩码无效	0：屏蔽有效1 ：屏蔽无效。	R/W

MKIVLR中的每个位都与一个相同号码的邮箱相关联。MKIVLR中的位[0]对应邮箱0(MB0)，位[31]对应邮箱31(MB31)。*1

当某个位设置为1时，相关联的接受屏蔽寄存器对于相关联的邮箱变得无效。当掩码无效位设置为1时，只有当接收消息ID与邮箱ID完全匹配时，相关邮箱才会接收消息。

在CAN复位或暂停模式下写入MKIVLR。

注1.在FIFO邮箱模式下将位[31:24]设置为0。

37.2.6 邮箱寄存器j（MBj_ID、MBj_DL、MBj_Dm、MBj_TS）（j=0到31；m=0到7）

表37.4列出了CANi邮箱内存映射，表37.5列出了CAN数据帧配置。

CANi邮箱复位后的值未定义。

仅当相关的MCTL_TXj或MCTL_RXj寄存器（j=0到31）为00h且相关邮箱未处理中止请求时才写入MBj_ID、MBj_DL、MBj_Dm和MBj_TS。

有关详细的寄存器地址，请参见表37.4。

Table 37.4 CANi邮箱内存映射(1of2)

Address		留言内容
CAN0	CAN1	内存映射
4005 0200h + 16 × j + 0	4005 1200h + 16 × j + 0	IDE、RTR、SID10到SID6
4005 0200h + 16 × j + 1	4005 1200h + 16 × j + 1	SID5 to SID0, EID17, EID16
4005 0200h + 16 × j + 2	4005 1200h + 16 × j + 2	EID15 to EID8
4005 0200h + 16 × j + 3	4005 1200h + 16 × j + 3	EID7 to EID0
4005 0200h + 16 × j + 4	4005 1200h + 16 × j + 4	—

Table 37.4 CANi mailbox memory mapping (2 of 2)

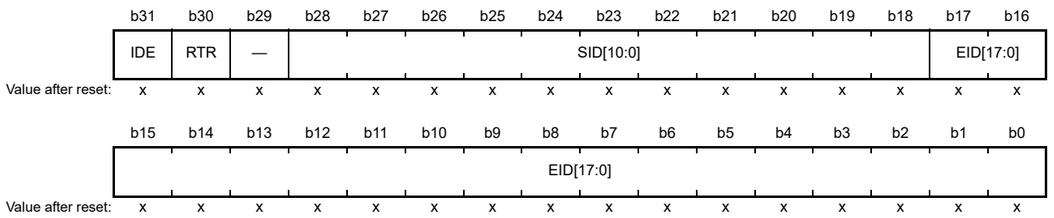
Address		Message content
CAN0	CAN1	Memory mapping
4005 0200h + 16 × j + 5	4005 1200h + 16 × j + 5	Data length code (DLC[3:0])
4005 0200h + 16 × j + 6	4005 1200h + 16 × j + 6	Data byte 0
4005 0200h + 16 × j + 7	4005 1200h + 16 × j + 7	Data byte 1
4005 0200h + 16 × j + 8	4005 1200h + 16 × j + 8	Data byte 2
4005 0200h + 16 × j + 9	4005 1200h + 16 × j + 9	Data byte 3
4005 0200h + 16 × j + 10	4005 1200h + 16 × j + 10	Data byte 4
4005 0200h + 16 × j + 11	4005 1200h + 16 × j + 11	Data byte 5
4005 0200h + 16 × j + 12	4005 1200h + 16 × j + 12	Data byte 6
4005 0200h + 16 × j + 13	4005 1200h + 16 × j + 13	Data byte 7
4005 0200h + 16 × j + 14	4005 1200h + 16 × j + 14	Time stamp upper byte
4005 0200h + 16 × j + 15	4005 1200h + 16 × j + 15	Time stamp lower byte

Table 37.5 CAN data frame configuration

SID10 to SID6	SID5 to SID0	EID17 to EID16	EID15 to EID8	EID7 to EID0	DLC3 to DLC1	DATA0	DATA1	…	DATA7

The previous value of each mailbox is retained unless a new message is received.

Address(es): CAN0.MB0_ID 4005 0200h to CAN0.MB31_ID 4005 03F0h, CAN1.MB0_ID 4005 1200h to CAN1.MB31_ID 4005 13F0h



x: Undefined

Bit	Symbol	Bit name	Description	R/W
b17 to b0	EID[17:0]	Extended ID*1	Extended ID of the data and remote frames	R/W
b28 to b18	SID[10:0]	Standard ID	Standard ID of the data and remote frames	R/W
b29	—	Reserved	The read value is undefined. The write value should be 0.	R/W
b30	RTR	Remote Transmission Request	0: Data frame 1: Remote frame.	R/W
b31	IDE	ID Extension*2	0: Standard ID 1: Extended ID.	R/W

Note 1. If the mailbox receives a standard ID message, the EID bits in the mailbox are undefined.
Note 2. The IDE bit is enabled when the CTLR.IDFM[1:0] bits are 10b (mixed ID mode). When the IDFM[1:0] bits are any value other than 10b, the IDE bit should be written with 0 and read as 0.

Table 37.4 CANi邮箱内存映射(2of2)

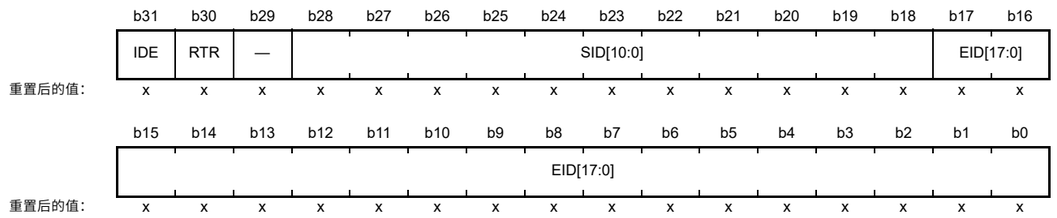
Address		留言内容
CAN0	CAN1	内存映射
4005 0200h + 16 × j + 5	4005 1200h + 16 × j + 5	数据长度码（DLC[3:0]）
4005 0200h + 16 × j + 6	4005 1200h + 16 × j + 6	数据字节0
4005 0200h + 16 × j + 7	4005 1200h + 16 × j + 7	数据字节1
4005 0200h + 16 × j + 8	4005 1200h + 16 × j + 8	数据字节2
4005 0200h + 16 × j + 9	4005 1200h + 16 × j + 9	数据字节3
4005 0200h + 16 × j + 10	4005 1200h + 16 × j + 10	数据字节4
4005 0200h + 16 × j + 11	4005 1200h + 16 × j + 11	数据字节5
4005 0200h + 16 × j + 12	4005 1200h + 16 × j + 12	数据字节6
4005 0200h + 16 × j + 13	4005 1200h + 16 × j + 13	数据字节7
4005 0200h + 16 × j + 14	4005 1200h + 16 × j + 14	时间戳高字节
4005 0200h + 16 × j + 15	4005 1200h + 16 × j + 15	时间戳低字节

Table 37.5 CAN数据帧配置

SID10 to SID6	SID5 to SID0	EID17 to EID16	EID15 to EID8	EID7 to EID0	DLC3 to DLC1	DATA0	DATA1	…	DATA7

除非收到新邮件，否则保留每个邮箱的先前值。

Address(es): CAN0.MB0_ID 4005 0200h to CAN0.MB31_ID 4005 03F0h, CAN1.MB0_ID 4005 1200h to CAN1.MB31_ID 4005 13F0h



x: Undefined

Bit	Symbol	位名称	Description	R/W
b17 to b0	EID[17:0]	扩展ID *1	数据和远程帧的扩展ID	R/W
b28 to b18	SID[10:0]	标准标识	数据和远程帧的标准ID	R/W
b29	—	Reserved	读取值未定义。写入值应为0。	R/W
b30	RTR	远程传输请求	0：数据帧1：远 程帧。	R/W
b31	IDE	身份扩展 *2	0：标准ID1： 扩展ID。	R/W

Note 1. 如果邮箱收到标准ID消息，则邮箱中的EID位未定义。
Note 2. 当CTLR.IDFM[1:0]位为10b（混合ID模式）时，IDE位被使能。当IDFM[1:0]位为10b以外的任何值时，IDE位应写为0，读为0。

Address(es): CAN0.MB0_DL 4005 0204h to CAN0.MB31_DL 4005 03F4h, CAN1.MB0_DL 4005 1204h to CAN1.MB31_DL 4005 13F4h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	DLC[3:0]			
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b3 to b0	DLC[3:0]	Data Length Code*1	b3 b0 0 0 0 0: Data length = 0 byte 0 0 0 1: Data length = 1 byte 0 0 1 0: Data length = 2 bytes 0 0 1 1: Data length = 3 bytes 0 1 0 0: Data length = 4 bytes 0 1 0 1: Data length = 5 bytes 0 1 1 0: Data length = 6 bytes 0 1 1 1: Data length = 7 bytes 1 x x x: Data length = 8 bytes.	R/W
b15 to b4	—	Reserved	The read value is undefined. The write value should be 0.	R/W

x: Don't care

Note 1. If the mailbox receives a message with data length (set in DLC[3:0]) of n bytes, where n is less than 8, the data in the DATAn to DATA7 registers in the mailbox is undefined. DATA0 to DATA7 are data registers for this mailbox. For example, if data length is 6 bytes (DLC[3:0] = 6h), the data in DATA6 and DATA7 registers is undefined.

Address(es): CAN0.MB0_DL 4005 0204h to CAN0.MB31_DL 4005 03F4h, CAN1.MB0_DL 4005 1204h to CAN1.MB31_DL 4005 13F4h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	DLC[3:0]			
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	位名称		Description	R/W
b3 to b0	DLC[3:0]	数据长度代码	*1	b3b00000：数据长度=0字节0001：数据长度=1字节0010：数据长度=2字节0011：数据长度=3字节0100：数据长度=4字节0101：数据长度=5字节0110：数据长度=6字节0111：数据长度=7字节1xxx：数据长度=8字节。	R/W
b15 to b4	—	Reserved		读取值未定义。写入值应为0。	R/W

x: Don't care

Note 1. 如果邮箱接收到数据长度（在DLC[3:0]中设置）为n字节的消息，其中n小于8，则邮箱中DATAn到DATA7寄存器中的数据未定义。DATA0到DATA7是该邮箱的数据寄存器。例如，如果数据长度为6字节（DLC[3:0]=6h），则DATA6和DATA7寄存器中的数据未定义。

Address(es): CAN0.MB0_D0 4005 0206h to CAN0.MB31_D0 4005 03F6h, CAN1.MB0_D0 4005 1206h to CAN1.MB31_D0 4005 13F6h

	b7	b6	b5	b4	b3	b2	b1	b0
	DATA0							
Value after reset:	x	x	x	x	x	x	x	x

Address(es): CAN0.MB0_D1 4005 0207h to CAN0.MB31_D1 4005 03F7h, CAN1.MB0_D1 4005 1207h to CAN1.MB31_D1 4005 13F7h

	b7	b6	b5	b4	b3	b2	b1	b0
	DATA1							
Value after reset:	x	x	x	x	x	x	x	x

Address(es): CAN0.MB0_D2 4005 0208h to CAN0.MB31_D2 4005 03F8h, CAN1.MB0_D2 4005 1208h to CAN1.MB31_D2 4005 13F8h

	b7	b6	b5	b4	b3	b2	b1	b0
	DATA2							
Value after reset:	x	x	x	x	x	x	x	x

Address(es): CAN0.MB0_D3 4005 0209h to CAN0.MB31_D3 4005 03F9h, CAN1.MB0_D3 4005 1209h to CAN1.MB31_D3 4005 13F9h

	b7	b6	b5	b4	b3	b2	b1	b0
	DATA3							
Value after reset:	x	x	x	x	x	x	x	x

Address(es): CAN0.MB0_D4 4005 020Ah to CAN0.MB31_D4 4005 03FAh, CAN1.MB0_D4 4005 120Ah to CAN1.MB31_D4 4005 13FAh

	b7	b6	b5	b4	b3	b2	b1	b0
	DATA4							
Value after reset:	x	x	x	x	x	x	x	x

Address(es): CAN0.MB0_D5 4005 020Bh to CAN0.MB31_D5 4005 03FBh, CAN1.MB0_D5 4005 120Bh to CAN1.MB31_D5 4005 13FBh

	b7	b6	b5	b4	b3	b2	b1	b0
	DATA5							
Value after reset:	x	x	x	x	x	x	x	x

Address(es): CAN0.MB0_D6 4005 020Ch to CAN0.MB31_D6 4005 03FCh, CAN1.MB0_D6 4005 120Ch to CAN1.MB31_D6 4005 13FCh

	b7	b6	b5	b4	b3	b2	b1	b0
	DATA6							
Value after reset:	x	x	x	x	x	x	x	x

Address(es): CAN0.MB0_D7 4005 020Dh to CAN0.MB31_D7 4005 03FDh, CAN1.MB0_D7 4005 120Dh to CAN1.MB31_D7 4005 13FDh

	b7	b6	b5	b4	b3	b2	b1	b0
	DATA7							
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Address(es): CAN0.MB0_D0 4005 0206h to CAN0.MB31_D0 4005 03F6h, CAN1.MB0_D0 4005 1206h to CAN1.MB31_D0 4005 13F6h

	b7	b6	b5	b4	b3	b2	b1	b0
	DATA0							
重置后的值：	x	x	x	x	x	x	x	x

Address(es): CAN0.MB0_D1 4005 0207h to CAN0.MB31_D1 4005 03F7h, CAN1.MB0_D1 4005 1207h to CAN1.MB31_D1 4005 13F7h

	b7	b6	b5	b4	b3	b2	b1	b0
	DATA1							
重置后的值：	x	x	x	x	x	x	x	x

Address(es): CAN0.MB0_D2 4005 0208h to CAN0.MB31_D2 4005 03F8h, CAN1.MB0_D2 4005 1208h to CAN1.MB31_D2 4005 13F8h

	b7	b6	b5	b4	b3	b2	b1	b0
	DATA2							
重置后的值：	x	x	x	x	x	x	x	x

Address(es): CAN0.MB0_D3 4005 0209h to CAN0.MB31_D3 4005 03F9h, CAN1.MB0_D3 4005 1209h to CAN1.MB31_D3 4005 13F9h

	b7	b6	b5	b4	b3	b2	b1	b0
	DATA3							
重置后的值：	x	x	x	x	x	x	x	x

Address(es): CAN0.MB0_D4 4005 020Ah to CAN0.MB31_D4 4005 03FAh, CAN1.MB0_D4 4005 120Ah to CAN1.MB31_D4 4005 13FAh

	b7	b6	b5	b4	b3	b2	b1	b0
	DATA4							
重置后的值：	x	x	x	x	x	x	x	x

Address(es): CAN0.MB0_D5 4005 020Bh to CAN0.MB31_D5 4005 03FBh, CAN1.MB0_D5 4005 120Bh to CAN1.MB31_D5 4005 13FBh

	b7	b6	b5	b4	b3	b2	b1	b0
	DATA5							
重置后的值：	x	x	x	x	x	x	x	x

Address(es): CAN0.MB0_D6 4005 020Ch to CAN0.MB31_D6 4005 03FCh, CAN1.MB0_D6 4005 120Ch to CAN1.MB31_D6 4005 13FCh

	b7	b6	b5	b4	b3	b2	b1	b0
	DATA6							
重置后的值：	x	x	x	x	x	x	x	x

Address(es): CAN0.MB0_D7 4005 020Dh to CAN0.MB31_D7 4005 03FDh, CAN1.MB0_D7 4005 120Dh to CAN1.MB31_D7 4005 13FDh

	b7	b6	b5	b4	b3	b2	b1	b0
	DATA7							
重置后的值：	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b7 to b0	DATA0 to DATA7	Data Bytes 0 to 7*1,*2	DATA0 to DATA7 store the transmitted or received CAN message data. Transmission or reception starts from DATA0. The bit order on the CAN bus is MSB-first, and transmission or reception starts from bit [7].	R/W

Note 1. If the mailbox receives a message with n bytes less than 8 bytes, the values of DATAn to DATA7 in the mailbox are undefined.
Note 2. If the mailbox receives a remote frame, the previous values of DATA0 to DATA7 in the mailbox are saved.

Address(es): CAN0.MB0_TS 4005 020Eh to CAN0.MB31_TS 4005 03FEh, CAN1.MB0_TS 4005 120Eh to CAN1.MB31_TS 4005 13FEh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TSH[7:0]								TSL[7:0]							
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b7 to b0	TSL[7:0]	Time Stamp Lower Byte	The TSH[7:0] and TSL[7:0] bits store the counter value of the time stamp when received messages are stored in the mailbox.	R/W
b15 to b8	TSH[7:0]	Time Stamp Higher Byte		R/W

EID[17:0] bits (Extended ID)

The EID[17:0] bits set the extended ID of data frames and remote frames. They are used to transmit or receive extended ID messages.

SID[10:0] bits (Standard ID)

The SID[10:0] bits set the standard ID of data frames and remote frames. They are used to transmit or receive both standard ID and extended ID messages.

RTR bit (Remote Transmission Request)

The RTR bit sets the frame format to data frames or remote frames.

- The receive mailbox only receives frames with the format specified in the RTR bit
- The transmit mailbox transmits with the frame format specified in the RTR bit
- The receive FIFO mailbox receives the data frame, remote frame, or both frames specified in the RTR bit in FIDCR0 and FIDCR1
- The transmit FIFO mailbox transmits the data frame or remote frame specified in the RTR bit in the transmit message.

IDE bit (ID Extension)

The IDE bit sets the ID format to standard IDs or extended IDs. The IDE bit is enabled when the IDFM[1:0] bits in CTLR are 10b (mixed ID mode).

- The receive mailbox only receives the ID format specified in the IDE bit
- The transmit mailbox transmits with the ID format specified in the IDE bit
- The receive FIFO mailbox receives messages with the standard ID and extended ID settings specified in the IDE bit in FIDCR0 and FIDCR1
- The transmit FIFO mailbox transmits messages with the standard ID or extended ID settings specified in the IDE bit in the transmit message.

Bit	Symbol	位名称	Description	R/W
b7 to b0	DATA0 to DATA7	数据字节0到7*1 *2	DATA0到DATA7存储发送或接收的CAN报文数据。发送或接收从DATA0开始。CAN总线上的位顺序是MSB优先，发送或接收从位[7]开始。	R/W

Note 1. 如果邮箱收到n字节小于8字节的消息，邮箱中DATAn到DATA7的值是未定义的。
Note 2. 如果邮箱接收到远程帧，则邮箱中DATA0到DATA7的先前值被保存。

Address(es): CAN0.MB0_TS 4005 020Eh to CAN0.MB31_TS 4005 03FEh, CAN1.MB0_TS 4005 120Eh to CAN1.MB31_TS 4005 13FEh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TSH[7:0]								TSL[7:0]							
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b7 to b0	TSL[7:0]	时间戳低字节	当收到的消息存储在邮箱中时，TSH[7:0]和TSL[7:0]位存储时间戳的计数器值。	R/W
b15 to b8	TSH[7:0]	时间戳高字节		R/W

EID[17:0]位（扩展ID）

EID[17:0]位设置数据帧和远程帧的扩展ID。它们用于发送或接收扩展身份信息。

SID[10:0]位（标准ID）

SID[10:0]位设置数据帧和远程帧的标准ID。它们用于发送或接收标准ID和扩展ID消息。

RTR位（远程传输请求）

RTR位将帧格式设置为数据帧或远程帧。

- 接收邮箱只接收RTR位指定格式的帧
- 发送邮箱以RTR位中指定的帧格式发送
- 接收FIFO邮箱接收在RTR位中指定的数据帧、远程帧或两个帧 FIDCR0 and FIDCR1
- 发送FIFO邮箱发送发送报文中RTR位指定的数据帧或远程帧。

IDE位（ID扩展）

IDE位将ID格式设置为标准ID或扩展ID。当IDFM[1:0]位在CTLR为10b（混合ID模式）。

- 接收邮箱只接收IDE位指定的ID格式
- 发送邮箱以IDE位中指定的ID格式发送
- 接收FIFO邮箱接收具有FIDCR0和FIDCR1中的IDE位指定的标准ID和扩展ID设置的消息
- 发送FIFO邮箱使用发送消息的IDE位中指定的标准ID或扩展ID设置发送消息。

DLC[3:0] bits (Data Length Code)

The DLC[3:0] bits specify the data length to be transmitted in data frames. When a remote frame is used to request data, this field specifies the requested data length.

When a data frame is received, the received data length is stored in this field. When a remote frame is received, this field stores the requested data length.

37.2.7 Mailbox Interrupt Enable Register (MIER)

Address(es): CAN0.MIER 4005 042Ch, CAN1.MIER 4005 142Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	MB31	MB30	MB29	MB28	MB27	MB26	MB25	MB24	MB23	MB22	MB21	MB20	MB19	MB18	MB17	MB16
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MB15	MB14	MB13	MB12	MB11	MB10	MB9	MB8	MB7	MB6	MB5	MB4	MB3	MB2	MB1	MB0
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b31 to b0	MB31 to MB0	Interrupt Enable	0: Disable interrupt 1: Enable interrupt. Bit [31] is associated with mailbox 31 (MB31), and bit [0] with mailbox 0 (MB0).	R/W

MIER can enable interrupts for each mailbox independently. This register is available in normal mailbox mode. Do not access this register in FIFO mailbox mode.

Each bit is associated with the mailbox having the same number. These bits enable or disable transmission and reception complete interrupts for the associated mailboxes:

- Bit [0] in MIER corresponds to mailbox 0 (MB0)
- Bit [31] in MIER corresponds to mailbox 31 (MB31).

Write to MIER only when the associated MCTL_TXj or MCTL_RXj register (j = 0 to 31) is 00h and the associated mailbox is not processing a transmission or reception abort request.

DLC[3:0]位（数据长度代码）

DLC[3:0]位指定要在数据帧中传输的数据长度。当使用远程帧请求数据时，该字段指定请求的数据长度。

当接收到一个数据帧时，接收到的数据长度存储在该字段中。当接收到远程帧时，该字段存储请求的数据长度。

37.2.7 邮箱中断使能寄存器(MIER)

Address(es): CAN0.MIER 4005 042Ch, CAN1.MIER 4005 142Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	MB31	MB30	MB29	MB28	MB27	MB26	MB25	MB24	MB23	MB22	MB21	MB20	MB19	MB18	MB17	MB16
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MB15	MB14	MB13	MB12	MB11	MB10	MB9	MB8	MB7	MB6	MB5	MB4	MB3	MB2	MB1	MB0
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b31 to b0	MB31 to MB0	中断使能	0：禁用中断1：启用中断。位[31]与邮箱31(MB31)相关联，位[0]与邮箱0(MB0)相关联。	R/W

MIER可以独立为每个邮箱启用中断。该寄存器在正常邮箱模式下可用。不要在FIFO邮箱模式下访问该寄存器。

每个位与具有相同编号的邮箱相关联。这些位启用或禁用相关邮箱的发送和接收完成中断：

- MIER中的位[0]对应邮箱0(MB0)
- MIER中的位[31]对应邮箱31(MB31)。

仅当相关的MCTL_TXj或MCTL_RXj寄存器（j=0到31）为00h且相关邮箱未处理发送或接收中止请求时才写入MIER。

37.2.8 Mailbox Interrupt Enable Register for FIFO Mailbox Mode (MIER_FIFO)

Address(es): CAN0.MIER_FIFO 4005 042Ch, CAN1.MIER_FIFO 4005 142Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	MB29	MB28	—	—	MB25	MB24	MB23	MB22	MB21	MB20	MB19	MB18	MB17	MB16
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MB15	MB14	MB13	MB12	MB11	MB10	MB9	MB8	MB7	MB6	MB5	MB4	MB3	MB2	MB1	MB0
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b23 to b0	MB23 to MB0	Interrupt Enable	0: Disable interrupt 1: Enable interrupt. Bit [23] is associated with mailbox 23 (MB23), and bit [0] with mailbox 0 (MB0).	R/W
b24	MB24	Transmit FIFO Interrupt Enable	0: Disable interrupt 1: Enable interrupt.	R/W
b25	MB25	Transmit FIFO Interrupt Generation Timing Control	0: Generate every time transmission completes 1: Generate when the transmit FIFO empties on transmission completion.	R/W
b27, b26	—	Reserved	The read value is undefined. The write value should be 0.	R/W
b28	MB28	Receive FIFO Interrupt Enable	0: Disable interrupt 1: Enable interrupt.	R/W
b29	MB29	Receive FIFO Interrupt Generation Timing Control*1	0: Generate every time reception completes 1: Generate when the receive FIFO becomes a buffer warning*2 on reception completion.	R/W
b31, b30	—	Reserved	The read value is undefined. The write value should be 0.	R/W

Note 1. No interrupt request occurs when the receive FIFO becomes buffer warning because it is full.
Note 2. “Buffer warning” indicates a state in which the third message is stored in the receive FIFO.

MIER_FIFO can individually enable interrupts for each mailbox and FIFO. This register is available in normal mailbox mode and FIFO mailbox mode. Do not access it in normal mailbox mode.

The MB0 to MB23 bits are associated with the mailbox having the same number. These bits enable or disable transmission and reception complete interrupts for the associated mailboxes:

- Bit [0] in MIER_FIFO is associated with mailbox 0 (MB0)
- Bit [23] in MIER_FIFO is associated with mailbox 23 (MB23).

MB24, MB25, MB28, and MB29 specify whether transmit and receive FIFO interrupts are enabled or disabled, and the timing of interrupt requests.

Write to MIER_FIFO only when the associated MCTL_TXj or MCTL_RXj register (j = 0 to 31) is 00h and the associated mailbox is not processing a transmission or reception abort request. In addition, change the bits in MIER_FIFO for the associated FIFO only when the TFE bit in TFCR is 0 and the TFEST bit is 1, and the RFE bit in RFCR is 0 and the RFEST bit in RFCR is 1.

37.2.8 FIFO邮箱模式的邮箱中断使能寄存器(MIER_FIFO)

Address(es): CAN0.MIER_FIFO 4005 042Ch, CAN1.MIER_FIFO 4005 142Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	MB29	MB28	—	—	MB25	MB24	MB23	MB22	MB21	MB20	MB19	MB18	MB17	MB16
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	MB15	MB14	MB13	MB12	MB11	MB10	MB9	MB8	MB7	MB6	MB5	MB4	MB3	MB2	MB1	MB0
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b23 to b0	MB23 to MB0	中断使能	0：禁用中断1：启用中断。位[23]与邮箱23(MB23)相关联，位[0]与邮箱0(MB0)相关联。	R/W
b24	MB24	发送FIFO中断 Enable	0：禁用中断1：启用中断。	R/W
b25	MB25	发送FIFO中断 发电时序控制	0：每次发送完成时产生1：发送完成时发送FIFO清空时产生。	R/W
b27, b26	—	Reserved	读取值未定义。写入值应为0。	R/W
b28	MB28	接收FIFO中断 Enable	0：禁用中断1：启用中断。	R/W
b29	MB29	接收FIFO中断 发电时序控制*1	0：每次接收完成时生成1：当接收FIFO变为缓冲区警告时生成*2接收完成时生成。	R/W
b31, b30	—	Reserved	读取值未定义。写入值应为0。	R/W

Note 1. 当接收FIFO因已满而变为缓冲区警告时，不会发生中断请求。
Note 2. “缓冲区警告”表示第三个消息存储在接收FIFO中的状态。

MIER_FIFO可以为每个邮箱和FIFO单独启用中断。该寄存器在普通邮箱模式和FIFO邮箱模式下可用。不要在普通邮箱模式下访问它。

MB0到MB23位与具有相同编号的邮箱相关联。这些位启用或禁用相关邮箱的发送和接收完成中断：

- MIER_FIFO中的位[0]与邮箱0(MB0)相关联
- MIER_FIFO中的位[23]与邮箱23(MB23)相关联。

MB24、MB25、MB28和MB29指定是启用还是禁用发送和接收FIFO中断，以及中断请求的时序。

仅当相关的MCTL_TXj或MCTL_RXj寄存器（j=0到31）为00h且相关邮箱未处理发送或接收中止请求时才写入MIER_FIFO。此外，仅当TFCR中的TFE位为0且TFEST位为1且RFE位为

RFCR为0，RFCR中的RFEST位为1。

37.2.9 Message Control Register for Transmit (MCTL_TXj) (j = 0 to 31)

- Transmit mode (when the TRMREQ bit is 1 and the RECREQ bit is 0)

Address(es): CAN0.MCTL_TX[0] 4005 0820h to CAN0.MCTL_TX[31] 4005 083Fh, CAN1.MCTL_TX[0] 4005 1820h to CAN1.MCTL_TX[31] 4005 183Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	TRMREQ	RECREQ	—	ONESHOT	—	TRMABT	TRMACTIVE	SENTDATA
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	SENTDATA	Transmission Complete Flag *1,*2	0: Transmission not complete 1: Transmission complete.	R/W
b1	TRMACTIVE	Transmission-in-Progress Status Flag	0: Transmission pending or not requested 1: Transmission in progress.	R
b2	TRMABT	Transmission Abort Complete Flag*1,*2	0: Transmission started, transmission abort failed because transmission completed, or transmission abort not requested 1: Transmission abort complete.	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	ONESHOT	One-Shot Enable*2,*3	0: Disable one-shot transmission 1: Enable one-shot transmission.	R/W
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6	RECREQ	Receive Mailbox Request *2,*3,*4,*5	0: Do not configure for reception 1: Configure for reception.	R/W
b7	TRMREQ	Transmit Mailbox Request *2,*4	0: Do not configure for transmission 1: Configure for transmission.	R/W

Note 1. Write 0 only. Writing 1 has no effect.
Note 2. When writing to bits of this register, write 1 to SENTDATA and TRMABT if these bits are not the write target.
Note 3. To enter one-shot transmit mode, write 1 to the ONESHOT bit at the same time as setting the TRMREQ bit to 1. To exit one-shot transmit mode, write 0 to the ONESHOT bit after the message is transmitted or aborted.
Note 4. Do not set both the RECREQ and TRMREQ bits to 1.
Note 5. When setting the RECREQ bit to 0, set the SENTDATA, TRMACTIVE, and TRMABT flags to 0 simultaneously.

MCTL_TXj sets mailbox j to transmit mode or receive mode. In transmit mode, MCTL_TXj also controls and indicates the transmission status. Do not access MCTL_TXj if mailbox j is in receive mode. Only write to MCTL_TXj in CAN operation or halt mode. Do not use MCTL_TX24 to MCTL_TX31 in FIFO mailbox mode.

SENTDATA flag (Transmission Complete Flag)

The SENTDATA flag is set to 1 when data transmission from the associated mailbox is complete. The SENTDATA flag is set to 0 through a software write. To set it to 0, first set the TRMREQ bit to 0. The SENTDATA and TRMREQ flags cannot be set to 0 simultaneously. To transmit a new message from the associated mailbox, set the SENTDATA flag to 0.

TRMACTIVE flag (Transmission-in-Progress Status Flag)

The TRMACTIVE flag is set to 1 when the associated mailbox of the CAN module begins transmitting a message. It is set to 0 when the CAN module loses CAN bus arbitration, a CAN bus error occurs, or data transmission completes.

TRMABT flag (Transmission Abort Complete Flag)

The TRMABT flag is set to 1 in the following cases:

- Following a transmission abort request, when the transmission abort is complete before starting transmission
- Following a transmission abort request, when the CAN module detects CAN bus arbitration-lost or a CAN bus error
- In one-shot transmission mode (RECREQ = 0, TRMREQ = 1, and ONESHOT = 1), when the CAN module detects a CAN bus arbitration-lost or a CAN bus error.

37.2.9 用于发送的消息控制寄存器(MCTL_TXj)(j=0到31)

发送模式（当TRMREQ位为1且RECREQ位为0时）

Address(es): CAN0.MCTL_TX[0] 4005 0820h to CAN0.MCTL_TX[31] 4005 083Fh, CAN1.MCTL_TX[0] 4005 1820h to CAN1.MCTL_TX[31] 4005 183Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	TRMREQ	RECREQ	—	ONESHOT	—	TRMABT	TRMACTIVE	SENTDATA
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	SENTDATA	传输完成标志*1 *2	0：传输未完成1：传输完成 。	R/W
b1	TRMACTIVE	Transmission-in-Progress 状态标志	0：传输未决或未请求1：传输中。	R
b2	TRMABT	传输中止完成 Flag*1,*2	0：传输开始，传输中止失败，因为 传输完成，或未请求传输中止1：传输中止完成。	R/W
b3	—	Reserved	该位读取为0。写入值应为0。	R/W
b4	ONESHOT	One-Shot Enable*2,*3	0：禁止一次性发送1：允许一次 性发送。	R/W
b5	—	Reserved	该位读取为0。写入值应为0。	R/W
b6	RECREQ	接收邮箱请求*2 *3 *4 *5	0：不配置接收1：配置接收。	R/W
b7	TRMREQ	发送邮箱请求*2 *4	0：不配置传输1：配置传输。	R/W

Note 1. 只写0。写1无效。
Note 2. 写入该寄存器的位时，如果这些位不是写入目标，则向SENTDATA和TRMABT写入1。
Note 3. 要进入一次性发送模式，请在将TRMREQ位设置为1的同时将1写入ONESHOT位。要退出一次性发送模式，请在发送或中止消息后向ONESHOT位写入0。
Note 4. 不要将RECREQ和TRMREQ位都设置为1。
Note 5. 将RECREQ位设置为0时，同时将SENTDATA、TRMACTIVE和TRMABT标志设置为0。

MCTL_TXj将邮箱j设置为发送模式或接收模式。在传输模式下，MCTL_TXj也控制和指示传输状态。如果邮箱j处于接收模式，则不要访问MCTL_TXj。仅在CAN操作或暂停模式下写入MCTL_TXj。不要在FIFO邮箱模式下使用MCTL_TX24到MCTL_TX31。

SENTDATA标志（传输完成标志）

当来自相关邮箱的数据传输完成时，SENTDATA标志设置为1。SENTDATA标志通过软件写入设置为0。要将其设置为0，首先将TRMREQ位设置为0。SENTDATA和TRMREQ标志不能同时设置为0。要从关联邮箱发送新消息，请将SENTDATA标志设置为0。

TRMACTIVE标志（传输中状态标志）

当CAN模块的相关邮箱开始发送消息时，TRMACTIVE标志设置为1。当CAN模块失去CAN总线仲裁、出现CAN总线错误或数据传输完成时设置为0。

TRMABT标志（传输中止完成标志）

在以下情况下，TRMABT标志设置为1：

- 在传输中止请求之后，当传输中止在开始传输之前完成时
- 在发送中止请求之后，当CAN模块检测到CAN总线仲裁丢失或CAN总线错误时
- 在一次性传输模式下（RECREQ=0、TRMREQ=1和ONESHOT=1），当CAN模块检测到CAN总线仲裁丢失或CAN总线错误时。

The TRMABT flag does not set to 1 when data transmission is complete. The SENTDATA flag is set to 1. The TRMABT flag is set to 0 through a software write.

ONESHOT bit (One-Shot Enable)

When the ONESHOT bit is set to 1 in transmit mode (RECREQ = 0 and TRMREQ = 1), the CAN module transmits a message only one time. The CAN module does not transmit the message again if a CAN bus error or CAN bus arbitration-lost occurs. When transmission is complete, the SENTDATA flag is set to 1. If transmission does not complete because of a CAN bus error or CAN bus arbitration-lost error, the TRMABT flag is set to 1. Set the ONESHOT bit to 0 after the SENTDATA or TRMABT flag is set to 1.

RECREQ bit (Receive Mailbox Request)

The RECREQ bit selects the receive modes listed in Table 37.10.

When the RECREQ bit is set to 1, the associated mailbox is configured for reception of a data or remote frame.

When the RECREQ bit is set to 0, the associated mailbox is not configured for reception of a data or remote frame.

Due to hardware protection, the RECREQ bit cannot be set to 0 through a software write during the following period:

- Hardware protection is started from the acceptance filter processing (the beginning of the CRC field)
- Hardware protection is released:
  - For the mailbox that is specified to receive the incoming message, after the received data is stored in the mailbox or a CAN bus error occurs. This means that the maximum period of hardware protection is from the beginning of CRC field to the end of the 7th bit of EOF.
  - For the other mailboxes, after acceptance filter processing
  - If no mailbox is specified to receive the message, after acceptance filter processing.

When setting the RECREQ bit to 1, do not set the TRMREQ bit to 1. To change the configuration of a mailbox from transmission to reception, first abort the transmission and then set the SENTDATA and TRMABT flags to 0 before changing to reception.

Note: MCTL_TXj.RECREQ is the mirror bit of MCTL_RXj.RECREQ.

TRMREQ bit (Transmit Mailbox Request)

The TRMREQ bit selects the transmit modes listed in Table 37.10.

When the TRMREQ bit is set to 1, the associated mailbox is configured for transmission of a data or remote frame.

When the TRMREQ bit is set to 0, the associated mailbox is not configured for transmission of a data or remote frame.

If the TRMREQ bit is changed from 1 to 0 to cancel the associated transmission request, either the TRMABT or SENTDATA flag is set to 1. When setting the TRMREQ bit to 1, do not set the RECREQ bit to 1. To change the configuration of a mailbox from reception to transmission, first abort the reception, and then set the NEWDATA and MSGLOST bits to 0 before changing to transmission.

Note: MCTL_TXj.TRMREQ is the mirror bit of MCTL_RXj.TRMREQ.

数据传输完成时，TRMABT标志不设置为1。SENTDATA标志设置为1。TRMABT标志通过软件写入设置为0。

ONESHOT位（一次性启用）

在发送模式下（RECREQ=0且TRMREQ=1）将ONESHOT位设置为1时，CAN模块仅发送一次报文。如果发生CAN总线错误或CAN总线仲裁失败，CAN模块不会再次发送消息。当传输完成时，SENTDATA标志设置为1。如果由于CAN总线错误或CAN总线仲裁丢失错误导致传输未完成，则TRMABT标志设置为1。在SENTDATA或TRMABT标志设置为1。

RECREQ位（接收邮箱请求）

RECREQ位选择表37.10中列出的接收模式。

当RECREQ位设置为1时，相关邮箱配置为接收数据或远程帧。

当RECREQ位设置为0时，相关邮箱未配置为接收数据或远程帧。

由于硬件保护，RECREQ位在以下期间不能通过软件写入设置为0：

- 硬件保护从验收过滤器处理开始（CRC字段的开始）
- 硬件保护发布：
  - 对于指定接收传入报文的邮箱，在接收到的数据存入邮箱后或出现CAN总线错误。这意味着硬件保护的最大周期是从CRC字段的开始到EOF的第7位结束。
  - 对于其他邮箱，接受过滤处理后
  - 如果没有指定邮箱接收邮件，则经过接受过滤处理。

将RECREQ位设置为1时，不要将TRMREQ位设置为1。要将邮箱配置从发送更改为接收，首先中止发送，然后在更改为接收之前将SENTDATA和TRMABT标志设置为0。

Note: MCTL_TXj.RECREQ是MCTL_RXj.RECREQ的镜像位。

TRMREQ位（发送邮箱请求）

TRMREQ位选择表37.10中列出的发送模式。

当TRMREQ位设置为1时，相关邮箱配置为传输数据或远程帧。

当TRMREQ位设置为0时，相关邮箱未配置为传输数据或远程帧。

如果TRMREQ位从1更改为0以取消相关的发送请求，则TRMABT或SENTDATA标志设置为1。将TRMREQ位设置为1时，不要将RECREQ位设置为1。要更改一个邮箱从接收到发送，首先中止接收，然后将NEWDATA和MSGLOST位设置为0，然后再更改为发送。

Note: MCTL_TXj.TRMREQ是MCTL_RXj.TRMREQ的镜像位。

37.2.10 Message Control Register for Receive (MCTL_RXj) (j = 0 to 31)

- Receive mode (when the TRMREQ bit is 0 and the RECREQ bit is 1)

Address(es): CAN0.MCTL_RX[0] 4005 0820h to CAN0.MCTL_RX[31] 4005 083Fh, CAN1.MCTL_RX[0] 4005 1820h to CAN1.MCTL_RX[31] 4005 183Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	TRMREQ	RECREQ	—	ONESHOT	—	MSGLOST	INVALDATA	NEWDATA
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	NEWDATA	Reception Complete Flag*1,*2	0: No data received, or 0 was written to the bit 1: New message being stored or was stored in the mailbox.	R/W
b1	INVALDATA	Reception-in-Progress Status Flag	0: Message valid 1: Message being updated.	R
b2	MSGLOST	Message Lost Flag*1,*2	0: Message not overwritten or overrun 1: Message overwritten or overrun.	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	ONESHOT	One-Shot Enable*2,*3	0: Disable one-shot reception 1: Enable one-shot reception.	R/W
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6	RECREQ	Receive Mailbox Request *2,*3,*4,*5	0: Do not configure for reception 1: Configure for reception.	R/W
b7	TRMREQ	Transmit Mailbox Request *2,*4	0: Do not configure for transmission 1: Configure for transmission.	R/W

Note 1. Write 0 only. Writing 1 has no effect.
Note 2. When writing to bits of this register, write 1 to the NEWDATA and MSGLOST bits if they are not the write target.
Note 3. To enter one-shot receive mode, write 1 to the ONESHOT bit at the same time as setting the RECREQ bit to 1. To exit one-shot receive mode, write 0 to the ONESHOT bit after writing 0 to the RECREQ bit and confirming that it is 0.
Note 4. Do not set both the RECREQ and TRMREQ bits to 1.
Note 5. When setting the RECREQ bit to 0, set the MSGLOST, NEWDATA, and RECREQ bits to 0 simultaneously.

MCTL_RXj sets mailbox j to transmit or receive mode. In receive mode, MCTL_RXj also controls and indicates the reception status. Do not access MCTL_RXj if mailbox j is in transmit mode. Only write to the MCTL_RXj in CAN operation or halt mode. Do not use MCTL_RX24 to MCTL_RX31 in FIFO mailbox mode.

NEWDATA flag (Reception Complete Flag)

The NEWDATA flag is set to 1 when a new message is being stored or was stored in the mailbox. Always set this bit to 1 simultaneously with the INVALDATA flag. The NEWDATA flag is cleared to 0 through a software write. The NEWDATA flag cannot be set to 0 through a software write while the associated INVALDATA flag is 1.

INVALDATA flag (Reception-in-Progress Status Flag)

After the completion of a message reception, the INVALDATA flag is set to 1 while the received message is being updated into the associated mailbox. The INVALDATA flag is set to 0 immediately after the message is stored. If the mailbox is read while the INVALDATA flag is 1, the data is undefined.

MSGLOST flag (Message Lost Flag)

The MSGLOST flag is set to 1 when the mailbox is overwritten or overrun by a new received message while the NEWDATA flag is 1. The MSGLOST flag is set to 1 at the end of the 6th bit of EOF. The MSGLOST flag is set to 0 through a software write.

In both overwrite and overrun modes, the MSGLOST flag cannot be set to 0 through a software write during the 5 PCLKB cycles following the 6th bit of EOF.

37.2.10 接收消息控制寄存器(MCTL_RXj)(j=0to31)

接收模式（当TRMREQ位为0且RECREQ位为1时）

Address(es): CAN0.MCTL_RX[0] 4005 0820h to CAN0.MCTL_RX[31] 4005 083Fh, CAN1.MCTL_RX[0] 4005 1820h to CAN1.MCTL_RX[31] 4005 183Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	TRMREQ	RECREQ	—	ONESHOT	—	MSGLOST	INVALDATA	NEWDATA
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	NEWDATA	接收完成标志*1 *2	0：未接收到数据，或向该位写入01：新消息正在存储或已存储在邮箱中。	R/W
b1	INVALDATA	Reception-in-Progress Status Flag	0：消息有效1：消息正在更新。	R
b2	MSGLOST	消息丢失标志*1 *2	0：信息未被覆盖或溢出1：信息被覆盖或溢出。	R/W
b3	—	Reserved	该位读取为0。写入值应为0。	R/W
b4	ONESHOT	One-Shot Enable*2,*3	0：关闭一键接收1：打开一键接收。	R/W
b5	—	Reserved	该位读取为0。写入值应为0。	R/W
b6	RECREQ	接收邮箱请求*2 *3 *4 *5	0：不配置接收1：配置接收。	R/W
b7	TRMREQ	发送邮箱请求*2 *4	0：不配置传输1：配置传输。	R/W

Note 1. 只写0。写1无效。
Note 2. 写入该寄存器的位时，如果NEWDATA和MSGLOST位不是写入目标，则向它们写入1。
Note 3. 要进入一次性接收模式，请在将RECREQ位设置为1的同时向ONESHOT位写入1。要退出一次性接收模式，请在向RECREQ位写入0并确认后向ONESHOT位写入0它是0。
Note 4. 不要将RECREQ和TRMREQ位都设置为1。
Note 5. 将RECREQ位设置为0时，同时将MSGLOST、NEWDATA和RECREQ位设置为0。

MCTL_RXj将邮箱j设置为发送或接收模式。在接收模式下，MCTL_RXj还控制和指示接收状态。如果邮箱j处于传输模式，则不要访问MCTL_RXj。仅在CAN操作或暂停模式下写入MCTL_RXj。不要在FIFO邮箱模式下使用MCTL_RX24到MCTL_RX31。

NEWDATA标志（接收完成标志）

当新消息正在存储或已存储在邮箱中时，NEWDATA标志设置为1。始终将此位与INVALDATA标志同时设置为1。NEWDATA标志通过软件写入清除为0。当相关的INVALDATA标志为1时，不能通过软件写入将NEWDATA标志设置为0。

INVALDATA标志（接收进行中状态标志）

消息接收完成后，INVALDATA标志设置为1，同时接收到的消息正在更新到相关邮箱中。INVALDATA标志在消息存储后立即设置为0。如果在INVALDATA标志为1时读取邮箱，则数据未定义。

MSGLOST标志（消息丢失标志）

当邮箱被新收到的消息覆盖或溢出时，MSGLOST标志设置为1，而NEWDATA标志为1。MSGLOST标志在EOF的第6位末尾设置为1。MSGLOST标志通过软件写入设置为0。

在覆盖和溢出模式下，MSGLOST标志不能在5期间通过软件写入设置为0EOF的第6位之后的PCLKB周期。

ONESHOT bit (One-Shot Enable)

When the ONESHOT bit is set to 1 in receive mode (RECREQ = 1 and TRMREQ = 0), the mailbox receives a message only one time. The mailbox does not behave as a receive mailbox after having received a message one time. The behavior of the NEWDATA and INVALDATA flags is the same as in normal receive mode. In one-shot receive mode, the MSGLOST flag does not set to 1. To set the ONESHOT bit to 0, first write 0 to the RECREQ bit and ensure that it is 0.

RECREQ bit (Receive Mailbox Request)

The RECREQ bit selects receive modes listed in Table 37.10.

When the RECREQ bit is set to 1, the associated mailbox is configured for reception of a data or remote frame.

When the RECREQ bit is set to 0, the associated mailbox is not configured for reception of a data or remote frame.

Due to hardware protection, the RECREQ bit cannot be set to 0 through a software write during the following period:

- Hardware protection is started from the acceptance filter processing (the beginning of the CRC field)
- Hardware protection is released:
  - For the mailbox that is specified to receive the incoming message, after the received data is stored in the mailbox or a CAN bus error occurs. This means that the maximum period of hardware protection is from the beginning of the CRC field to the end of the 7th bit of EOF.
  - For the other mailboxes, after acceptance filter processing
  - If no mailbox is specified to receive the message, after acceptance filter processing.

When setting the RECREQ bit to 1, do not set the TRMREQ bit to 1. To change the configuration of a mailbox from transmission to reception, first abort the transmission and then set the SENTDATA and TRMABT flags to 0 before changing to reception.

Note: MCTL_RXj.RECREQ is the mirror bit of MCTL_TXj.RECREQ.

TRMREQ bit (Transmit Mailbox Request)

The TRMREQ bit selects the transmit modes listed in Table 37.10.

When the TRMREQ bit is set to 1, the associated mailbox is configured for transmission of a data or remote frame.

When the TRMREQ bit is set to 0, the associated mailbox is not configured for transmission of a data or remote frame.

If the TRMREQ bit is changed from 1 to 0 to cancel the associated transmission request, either the TRMABT or SENTDATA flag is set to 1. When setting the TRMREQ bit to 1, do not set the RECREQ bit to 1. To change the configuration of a mailbox from reception to transmission, first abort the reception and then set the NEWDATA and MSGLOST bits to 0 before changing to transmission.

Note: MCTL_RXj.TRMREQ is the mirror bit of MCTL_TXj.TRMREQ.

37.2.11 Receive FIFO Control Register (RFCR)

Address(es): CAN0.RFCR 4005 0848h, CAN1.RFCR 4005 1848h

	b7	b6	b5	b4	b3	b2	b1	b0
	RFEST	RFWST	RFFST	RFMLF	RFUST[2:0]			RFE
Value after reset:	1	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	RFE	Receive FIFO Enable	0: Disable receive FIFO 1: Enable receive FIFO.	R/W

ONESHOT位（一次性启用）

在接收模式下（RECREQ=1和TRMREQ=0）将ONESHOT位设置为1时，邮箱只接收一次消息。邮箱在收到一次消息后不再充当接收邮箱。NEWDATA和INVALDATA标志的行为与正常接收模式相同。在单次接收模式下，MSGLOST标志不设置为1。要将ONESHOT位设置为0，首先将0写入RECREQ位并确保其为0。

RECREQ位（接收邮箱请求）

RECREQ位选择表37.10中列出的接收模式。

当RECREQ位设置为1时，相关邮箱配置为接收数据或远程帧。

当RECREQ位设置为0时，相关邮箱未配置为接收数据或远程帧。

由于硬件保护，RECREQ位在以下期间不能通过软件写入设置为0：

- 硬件保护从验收过滤器处理开始（CRC字段的开始）
- 硬件保护发布：
  - 对于指定接收传入报文的邮箱，在接收到的数据存入邮箱后或出现CAN总线错误。这意味着硬件保护的最大周期是从CRC字段的开始到EOF的第7位结束。
  - 对于其他邮箱，接受过滤处理后
  - 如果没有指定邮箱接收邮件，则经过接受过滤处理。

将RECREQ位设置为1时，不要将TRMREQ位设置为1。要将邮箱配置从发送更改为接收，首先中止发送，然后在更改为接收之前将SENTDATA和TRMABT标志设置为0。

Note: MCTL_RXj.RECREQ是MCTL_TXj.RECREQ的镜像位。

TRMREQ位（发送邮箱请求）

TRMREQ位选择表37.10中列出的发送模式。

当TRMREQ位设置为1时，相关邮箱配置为传输数据或远程帧。

当TRMREQ位设置为0时，相关邮箱未配置为传输数据或远程帧。

如果TRMREQ位从1更改为0以取消相关的发送请求，则TRMABT或SENTDATA标志设置为1。将TRMREQ位设置为1时，不要将RECREQ位设置为1。要更改邮箱从接收到发送，首先中止接收，然后将NEWDATA和MSGLOST位设置为0，然后再更改为发送。

Note: MCTL_RXj.TRMREQ是MCTL_TXj.TRMREQ的镜像位。

37.2.11 接收FIFO控制寄存器(RFCR)

Address(es): CAN0.RFCR 4005 0848h, CAN1.RFCR 4005 1848h

	b7	b6	b5	b4	b3	b2	b1	b0
	RFEST	RFWST	RFFST	RFMLF	RFUST[2:0]			RFE
重置后的值：	1	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	RFE	接收FIFO使能	0：禁用接收FIFO1：启用接收FIFO。	R/W

Bit	Symbol	Bit name	Description	R/W
b3 to b1	RFUST[2:0]	Receive FIFO Unread Message Number Status	b3 b1 0 0 0: No unread message 0 0 1: 1 unread message 0 1 0: 2 unread messages 0 1 1: 3 unread messages 1 0 0: 4 unread messages 1 0 1: Reserved 1 1 0: Reserved 1 1 1: Reserved.	R
b4	RFMLF	Receive FIFO Message Lost Flag	0: Receive FIFO message not lost 1: Receive FIFO message lost.	R/W
b5	RFFST	Receive FIFO Full Status Flag	0: Receive FIFO not full 1: Receive FIFO full (4 unread messages).	R
b6	RFWST	Receive FIFO Buffer Warning Status Flag	0: Receive FIFO is not buffer warning 1: Receive FIFO is buffer warning (3 unread messages).	R
b7	RFEST	Receive FIFO Empty Status Flag	0: Unread message in receive FIFO 1: No unread message in receive FIFO.	R

Write to RFCR in CAN operation or halt mode.

RFE bit (Receive FIFO Enable)

When the RFE bit is set to 1, the receive FIFO is enabled.

When the RFE bit is set to 0, the receive FIFO is disabled for reception and becomes empty (RFEST bit = 1). Write 0 to the RFE bit simultaneously with setting the RFMLF flag.

Do not set this bit to 1 in normal mailbox mode (MBM bit in CTLR = 0). Due to hardware protection, the RFE bit cannot be set to 0 through a software write during the following period:

- Hardware protection is started from acceptance filter processing (the beginning of the CRC field)
- When hardware protection is released:
  - If the receive FIFO is specified to receive the incoming message, after the received data is stored in the receive FIFO or a CAN bus error occurs. This means that the maximum period of hardware protection is from the beginning of the CRC field to the end of the 7th bit of EOF.
  - If the receive FIFO is not specified to receive the message, after acceptance filter processing.

RFUST[2:0] bits (Receive FIFO Unread Message Number Status)

The RFUST[2:0] bits indicate the number of unread messages in the receive FIFO. The value of the RFUST[2:0] bits initializes to 000b when the RFE bit is set to 0.

RFMLF flag (Receive FIFO Message Lost Flag)

The RFMLF flag is set to 1 (receive FIFO message lost) when the receive FIFO receives a new message and is full. It is set to 1 at the end of the 6th bit of EOF.

The RFMLF flag is set to 0 through a software write. Writing 1 has no effect. In both overwrite and overrun modes, if the receive FIFO is full and determined to have received a message, the RFMLF flag cannot be set to 0 (receive FIFO message was not lost) through a software write because of hardware protection during the 5 PCLKB cycles following the 6th bit of EOF.

RFFST flag (Receive FIFO Full Status Flag)

The RFFST flag is set to 1 (receive FIFO is full) when the number of unread messages in the receive FIFO is 4. It is 0 (receive FIFO is not full) when the number of unread messages in the receive FIFO is less than 4. The flag is set to 0 when the RFE bit is 0.

RFWST flag (Receive FIFO Buffer Warning Status Flag)

The RFWST flag is set to 1 (receive FIFO is a buffer warning) when the number of unread messages in the receive FIFO is 3. It is 0 (receive FIFO is not a buffer warning) when the number of unread messages in the receive FIFO is less than 3

Bit	Symbol	位名称	Description	R/W
b3 to b1	RFUST[2:0]	接收FIFO未读消息号码状态	b3b1000：没有未读消息00 1：1条未读消息010：2条未读消息011：3条未读消息10 0：4条未读消息101：保留1 10：保留111：预订的。	R
b4	RFMLF	接收FIFO消息丢失标志	0：接收FIFO报文不丢失1：接收FIFO报文丢失。	R/W
b5	RFFST	接收FIFO满状态标志	0：接收FIFO未满1：接收FIFO已满（4个未读消息）。	R
b6	RFWST	接收FIFO缓冲区警告状态标志	0：接收FIFO不是缓冲区警告1：接收FIFO是缓冲区警告（3个未读消息）。	R
b7	RFEST	接收FIFO空状态标志	0：接收FIFO中未读消息1：接收FIFO中没有未读消息。	R

在CAN操作或暂停模式下写入RFCR。

RFE位（接收FIFO使能）

当RFE位设置为1时，启用接收FIFO。

当RFE位设置为0时，接收FIFO禁止接收并变为空（RFEST位=1）。在设置RFMLF标志的同时将0写入RFE位。

在正常邮箱模式下不要将此位设置为1（CTLR中的MBM位=0）。由于硬件保护，RFE位在以下期间不能通过软件写入设置为0：

- 硬件保护从验收过滤器处理开始（CRC字段的开始）
- 硬件保护解除时：
  - 如果指定接收FIFO接收进来的报文，接收到的数据存入receive出现FIFO或CAN总线错误。这意味着硬件保护的最大周期是从CRC字段的开始到EOF的第7位结束。
  - 如果接收FIFO没有指定接收报文，接受过滤后处理。

RFUST[2:0]位（接收FIFO未读消息编号状态）

RFUST[2:0]位指示接收FIFO中未读消息的数量。当RFE位设置为0时，RFUST[2:0]位的值初始化为000b。

RFMLF标志（接收FIFO消息丢失标志）

当接收FIFO接收到新消息并已满时，RFMLF标志设置为1（接收FIFO消息丢失）。它在EOF的第6位末尾设置为1。

RFMLF标志通过软件写入设置为0。写1无效。在覆盖和溢出模式下，如果接收FIFO已满并确定已接收到消息，则RFMLF标志不能通过软件写入设置为0（接收FIFO消息未丢失），因为在5个PCLKB周期内有硬件保护在EOF的第6位之后。

RFFST标志（接收FIFO满状态标志）

当接收FIFO中未读报文数为4时，RFFST标志设置为1（接收FIFO已满）。当接收FIFO中未读报文数小于4时，该标志为0（接收FIFO未满）.当RFE位为0时，该标志设置为0。

RFWST标志（接收FIFO缓冲区警告状态标志）

当接收FIFO中的未读消息数为3时，RFWST标志设置为1（接收FIFO为缓冲区警告）。当接收FIFO中的未读消息数为0（接收FIFO不是缓冲区警告）时小于3

or equal to 4. The RFWST flag is set to 0 when the RFE bit is 0.

RFEST flag (Receive FIFO Empty Status Flag)

The RFEST flag is set to 1 (no unread message in receive FIFO) when the number of unread messages in the receive FIFO is 0. It is set to 1 when the RFE bit is set to 0. The flag is set to 0 (unread message in receive FIFO) when the number of unread messages in the receive FIFO is one or more. Figure 37.2 shows the receive FIFO mailbox operation.

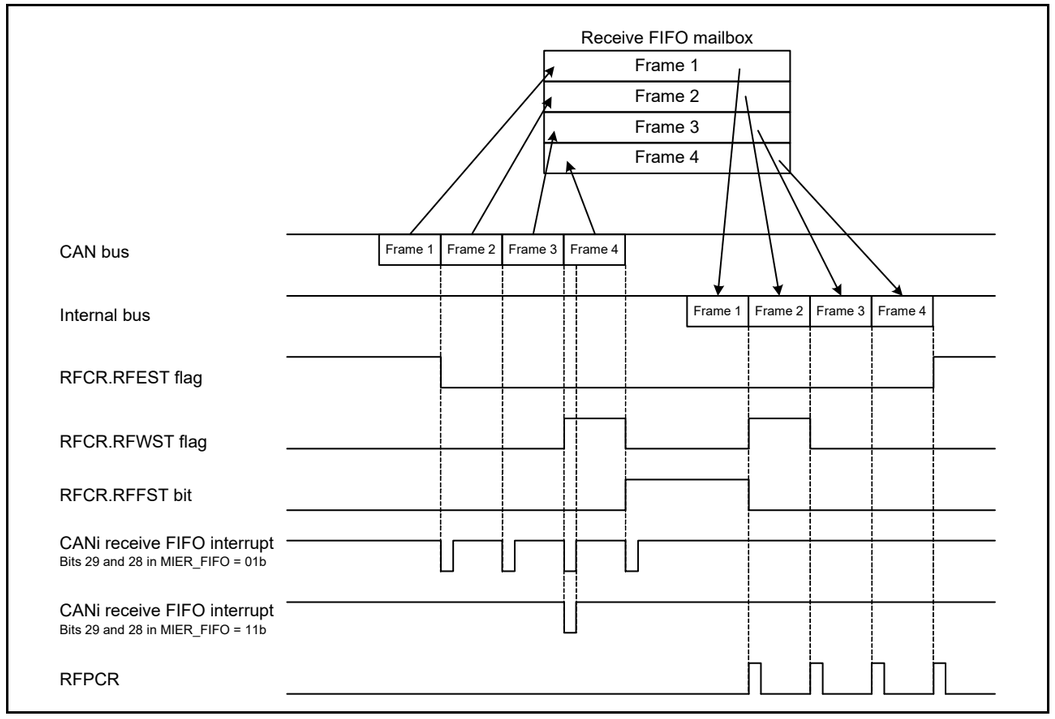


Figure 37.2 Receive FIFO mailbox operation when bits [29] and [28] in MIER_FIFO = 01b or 11b

37.2.12 Receive FIFO Pointer Control Register (RFPCR)

Address(es): CAN0.RFPCR 4005 0849h, CAN1.RFPCR 4005 1849h

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Description	R/W
b7 to b0	The CPU-side pointer for the receive FIFO is incremented by writing FFh to RFPCR.	W

When the receive FIFO is not empty, write FFh to RFPCR through the software to increment the CPU pointer to the next mailbox location. Do not write to RFPCR when the RFE bit in RFCR is 0 (receive FIFO disabled).

Both the CAN and CPU pointers increment when a new message is received and the RFFST flag is 1 (receive FIFO is full) in overwrite mode. When the RFMLF flag is 1 in this state, the CPU pointer does not increment on a software write to RFPCR.

或等于4。当RFE位为0时，RFWST标志设置为0。

RFEST标志（接收FIFO空状态标志）

RFEST标志设置为1（接收FIFO中没有未读消息），当接收中的未读消息数FIFO为0。当RFE位设置为0时设置为1。当接收FIFO中的未读报文数为1或更多时，该标志设置为0（接收FIFO中的未读报文）。图37.2显示了接收FIFO邮箱操作。

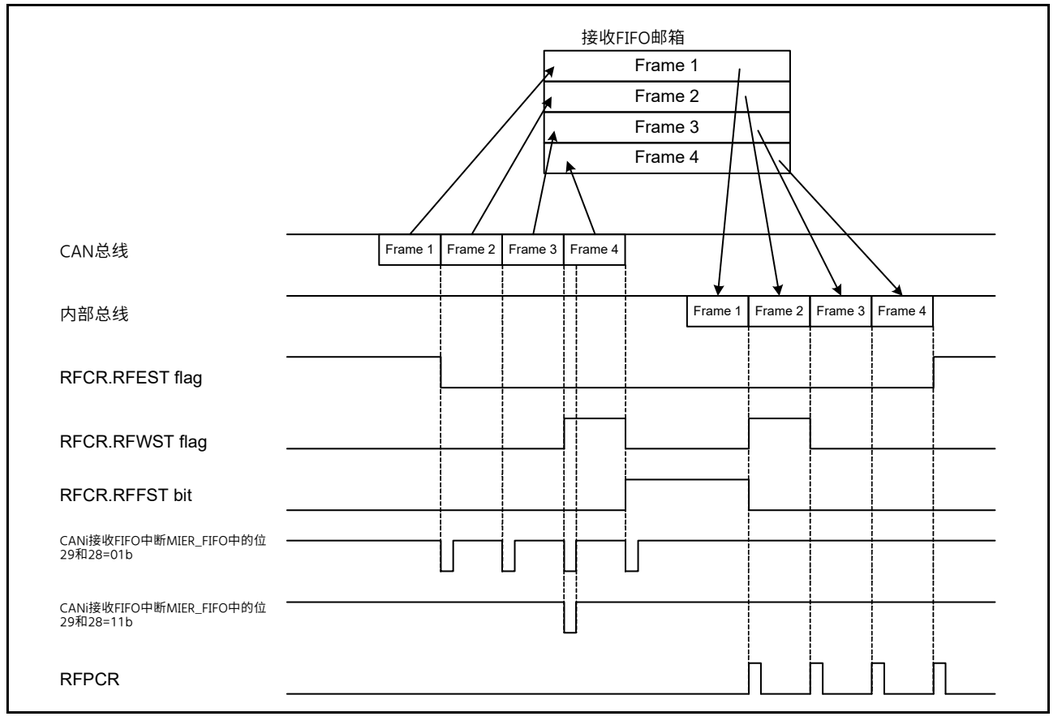


Figure 37.2 当MIER_FIFO中的位[29]和[28]=01b或11b时接收FIFO邮箱操作

37.2.12 接收FIFO指针控制寄存器(RFPCR)

Address(es): CAN0.RFPCR 4005 0849h, CAN1.RFPCR 4005 1849h

	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	x	x	x	x	x	x	x	x

x: Undefined

Bit	Description	R/W
b7 to b0	通过将FFh写入RFPCR，接收FIFO的CPU端指针递增。	W

当接收FIFO不为空时，通过软件将FFh写入RFPCR，使CPU指针递增到下一个邮箱位置。当RFCR中的RFE位为0（禁用接收FIFO）时，不要写入RFPCR。

当接收到新消息并且在覆盖模式下RFFST标志为1（接收FIFO已满）时，CAN和CPU指针都会递增。在此状态下，当RFMLF标志为1时，CPU指针不会在软件写入RFPCR时递增。

37.2.13 Transmit FIFO Control Register (TFCR)

Address(es): CAN0.TFCR 4005 084Ah, CAN1.TFCR 4005 184Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	TFEST	TFFST	—	—	TFUST[2:0]			TFE
Value after reset:	1	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	TFE	Transmit FIFO Enable	0: Disable transmit FIFO 1: Enable transmit FIFO.	R/W
b3 to b1	TFUST[2:0]	Transmit FIFO Unsent Message Number Status	b3 b1 0 0 0: 0 unsent messages 0 0 1: 1 unsent message 0 1 0: 2 unsent messages 0 1 1: 3 unsent messages 1 0 0: 4 unsent messages 1 0 1: Reserved 1 1 0: Reserved 1 1 1: Reserved.	R
b5, b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6	TFFST	Transmit FIFO Full Status	0: Transmit FIFO not full 1: Transmit FIFO full (4 unsent messages).	R
b7	TFEST	Transmit FIFO Empty Status	0: Unsent message in transmit FIFO 1: No unsent message in transmit FIFO.	R

Write to TFCR in CAN operation or halt mode.

TFE bit (Transmit FIFO Enable)

Setting the TFE bit set to 1 enables the transmit FIFO. Setting the TFE bit to 0 empties the transmit FIFO (TFEST bit = 1), and unsent messages in the transmit FIFO are lost in the following ways:

- Immediately if a message from the transmit FIFO is not scheduled for the next transmission or is already in transmission
- On completion of transmission, on a CAN bus error, CAN bus arbitration-lost, or entry to CAN halt mode, if a message from the transmit FIFO is scheduled for the next transmission or is already in transmission.

Before setting the TFE bit to 1 again, ensure that the TFEST bit is set to 1. After setting the TFE bit to 1, write transmit data to mailbox 24.

Do not set the TFE bit to 1 in normal mailbox mode (MBM bit in CTLR = 0).

TFUST[2:0] bits (Transmit FIFO Unsent Message Number Status)

The TFUST[2:0] bits indicate the number of unsent messages in the transmit FIFO. They are set to 000b after TFE bit is set to 0 and transmission aborts or completes.

TFFST bit (Transmit FIFO Full Status)

The TFFST bit is set to 1 (transmit FIFO is full) when the number of unsent messages in the transmit FIFO is 4. The TFFST bit is set to 0 (transmit FIFO is not full) when the number of unsent messages in the transmit FIFO is less than 4. The TFFST bit is set to 0 when transmission from the transmit FIFO is aborted.

TFEST bit (Transmit FIFO Empty Status)

The TFEST bit is set to 1 (no message in transmit FIFO) when the number of unsent messages in the transmit FIFO is 0. The TFEST bit is set to 1 when transmission from the transmit FIFO is aborted. The TFEST bit is set to 0 (message in transmit FIFO) when the number of unsent messages in the transmit FIFO is not 0.

Figure 37.3 shows the transmit FIFO mailbox operation.

37.2.13 发送FIFO控制寄存器(TFCR)

Address(es): CAN0.TFCR 4005 084Ah, CAN1.TFCR 4005 184Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	TFEST	TFFST	—	—	TFUST[2:0]			TFE
重置后的值：	1	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	TFE	发送FIFO使能	0：禁用发送FIFO1：启用发送FIFO。	R/W
b3 to b1	TFUST[2:0]	发送FIFO未发送消息号码状态	b3b1000：0条未发送消息001：1条未发送消息010：2条未发送消息011：3条未发送消息100：4条未发送消息101：保留110：保留111：预订的。	R
b5, b4	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b6	TFFST	发送FIFO满状态	0：发送FIFO未满1：发送FIFO已满（4个未发送消息）。	R
b7	TFEST	发送FIFO空状态	0：发送FIFO中未发送消息1：发送FIFO中没有未发送消息。	R

在CAN操作或暂停模式下写入TFCR。

TFE位（发送FIFO使能）

将TFE位设置为1会启用发送FIFO。将TFE位设置为0会清空发送FIFO（TFEST位=1），发送FIFO中未发送的消息会通过以下方式丢失：

- 如果来自发送FIFO的消息未安排下一次发送或已在发送中，则立即
- 在传输完成、CAN总线错误、CAN总线仲裁丢失或进入CAN暂停模式时，如果来自传输FIFO的消息被安排用于下一次传输或已经在传输中。

再次将TFE位设置为1之前，请确保TFEST位设置为1。将TFE位设置为1后，将发送数据写入邮箱24。

不要在正常邮箱模式下将TFE位设置为1（CTLR中的MBM位=0）。

TFUST[2:0]位（发送FIFO未发送消息编号状态）

TFUST[2:0]位指示发送FIFO中未发送消息的数量。在TFE位设置为0并且传输中止或完成后，它们设置为000b。

TFFST位（发送FIFO满状态）

当发送FIFO中未发送的消息数为4时，TFFST位设置为1（发送FIFO已满）。
当发送FIFO中未发送消息的数量小于4时，TFFST位设置为0（发送FIFO未满）。
当来自发送FIFO的发送被中止时，TFFST位设置为0。

TFEST位（发送FIFO空状态）

当发送FIFO中未发送消息的数量为0时，TFEST位设置为1（发送FIFO中没有消息）。
当来自发送FIFO的发送被中止时，TFEST位设置为1。当发送FIFO中未发送消息的数量不为0时，TFEST位设置为0（发送FIFO中的消息）。

图37.3显示了发送FIFO邮箱操作。

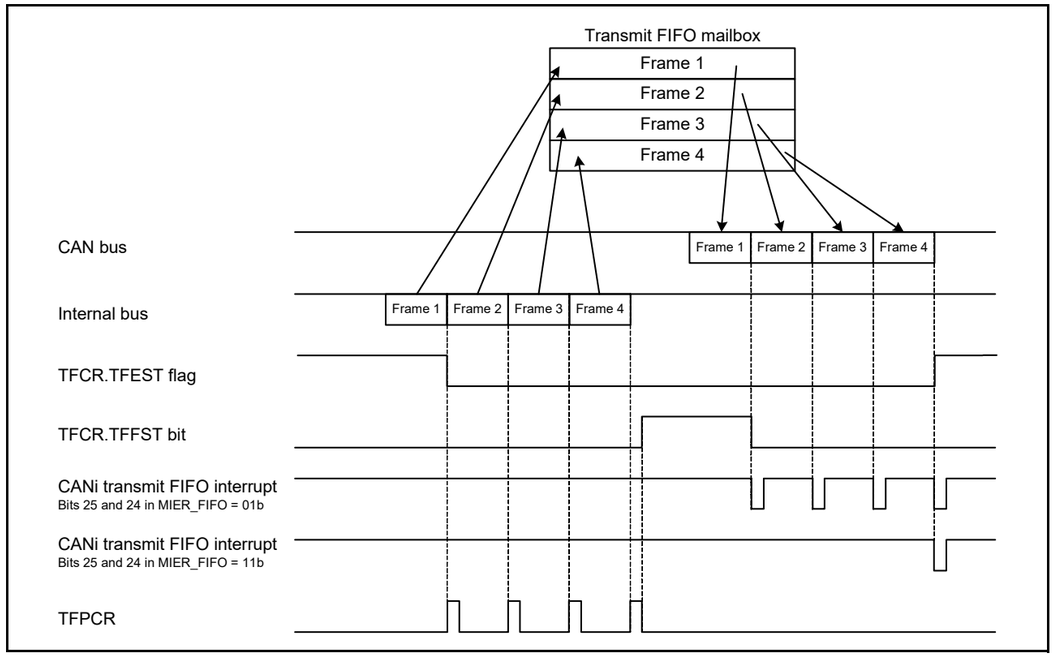


Figure 37.3 Transmit FIFO mailbox operation when bits [25] and [24] in MIER_FIFO = 01b or 11b

37.2.14 Transmit FIFO Pointer Control Register (TFPCR)

Address(es): CAN0.TFPCR 4005 084Bh, CAN1.TFPCR 4005 184Bh

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Description	R/W
b7 to b0	The CPU pointer for the transmit FIFO is incremented by writing FFh to TFPCR.	W

When the transmit FIFO is not full, write FFh to TFPCR through the software to increment the CPU pointer for the transmit FIFO to the next mailbox location.

Do not write to TFPCR when the TFE bit in TFCR is 0 (transmit FIFO disabled).

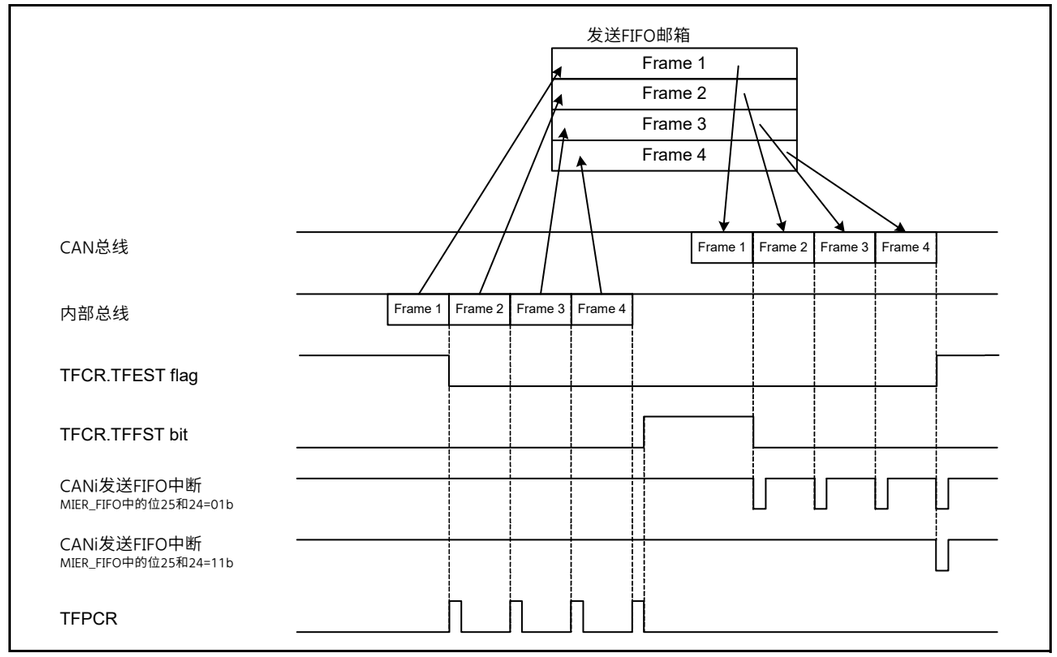


Figure 37.3 当MIER_FIFO中的位[25]和[24]=01b或11b时发送FIFO邮箱操作

37.2.14 发送FIFO指针控制寄存器(TFPCR)

Address(es): CAN0.TFPCR 4005 084Bh, CAN1.TFPCR 4005 184Bh

	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	x	x	x	x	x	x	x	x

x: Undefined

Bit	Description	R/W
b7 to b0	通过将FFh写入TFPCR，发送FIFO的CPU指针递增。	W

当发送FIFO未满时，通过软件将FFh写入TFPCR，以将发送FIFO的CPU指针递增到下一个邮箱位置。

当TFCR中的TFE位为0（禁用发送FIFO）时，不要写入TFPCR。

37.2.15 Status Register (STR)

Address(es): CAN0.STR 4005 0842h, CAN1.STR 4005 1842h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	RECST	TRMST	BOST	EPST	SLPST	HLTST	RSTST	EST	TABST	FMLST	NMLST	TFST	RFST	SDST	NDST
Value after reset:	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	NDST	NEWDATA Status Flag	0: No mailbox with NEWDATA = 1 1: 1 or more mailboxes with NEWDATA = 1.	R
b1	SDST	SENTDATA Status Flag	0: No mailbox with SENTDATA = 1 1: 1 or more mailboxes with SENTDATA = 1.	R
b2	RFST	Receive FIFO Status Flag	0: Empty receive FIFO 1: Message in receive FIFO.	R
b3	TFST	Transmit FIFO Status Flag	0: Transmit FIFO is full 1: Transmit FIFO is not full.	R
b4	NMLST	Normal Mailbox Message Lost Status Flag	0: No mailbox with MSGLOST = 1 1: 1 or more mailboxes with MSGLOST = 1.	R
b5	FMLST	FIFO Mailbox Message Lost Status Flag	0: RFMLF = 0 1: RFMLF = 1.	R
b6	TABST	Transmission Abort Status Flag	0: No mailbox with TRMABT = 1 1: 1 or more mailboxes with TRMABT = 1.	R
b7	EST	Error Status Flag	0: No error occurred 1: Error occurred.	R
b8	RSTST	CAN Reset Status Flag	0: Not in CAN reset mode 1: In CAN reset mode.	R
b9	HLTST	CAN Halt Status Flag	0: Not in CAN halt mode 1: In CAN halt mode.	R
b10	SLPST	CAN Sleep Status Flag	0: Not in CAN sleep mode 1: In CAN sleep mode.	R
b11	EPST	Error-Passive Status Flag	0: Not in error-passive state 1: In error-passive state.	R
b12	BOST	Bus-Off Status Flag	0: Not in bus-off state 1: In bus-off state.	R
b13	TRMST	Transmit Status Flag	0: Bus idle or reception in progress 1: Transmission in progress or module in bus-off state.	R
b14	RECST	Receive Status Flag	0: Bus idle or transmission in progress 1: Reception in progress.	R
b15	—	Reserved	This bit is read as 0.	R

NDST flag (NEWDATA Status Flag)

The NDST flag is set to 1 when at least one NEWDATA flag in MCTL_RXj (j = 0 to 31) is 1, regardless of the value of MIER or MIER_FIFO. It is set to 0 when all NEWDATA flags are 0.

SDST flag (SENTDATA Status Flag)

The SDST flag is set to 1 when at least one SENTDATA flag in MCTL_TXj (j = 0 to 31) is 1, regardless of the value of MIER or MIER_FIFO. It is set to 0 when all SENTDATA flags are 0.

RFST flag (Receive FIFO Status Flag)

The RFST flag is set to 1 when the receive FIFO is not empty. It is set to 0 when the receive FIFO is empty or normal mailbox mode is selected.

37.2.15 状态寄存器(STR)

Address(es): CAN0.STR 4005 0842h, CAN1.STR 4005 1842h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	RECST	TRMST	BOST	EPST	SLPST	HLTST	RSTST	EST	TABST	FMLST	NMLST	TFST	RFST	SDST	NDST
重置后的值：	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	NDST	NEWDATA状态标志	0：没有NEWDATA=1的邮箱1：有1个或多个NEWDATA=1的邮箱。	R
b1	SDST	SENTDATA状态标志	0：没有SENTDATA=1的邮箱1：1个或多个SENTDATA=1的邮箱。	R
b2	RFST	接收FIFO状态标志	0：空接收FIFO1：接收FIFO中的报文。	R
b3	TFST	发送FIFO状态标志	0：发送FIFO已满1：发送FIFO未满。	R
b4	NMLST	普通邮箱消息丢失状态标志	0：没有MSGLOST=1的邮箱1：1个或多个MSGLOST=1的邮箱。	R
b5	FMLST	FIFO邮箱消息丢失状态Flag	0: RFMLF = 0 1: RFMLF = 1.	R
b6	TABST	传输中止状态标志	0：没有TRMABT=1的邮箱1：1个或多个TRMABT=1的邮箱。	R
b7	EST	错误状态标志	0：未发生错误1：发生错误。	R
b8	RSTST	CAN复位状态标志	0：不处于CAN复位模式1：处于CAN复位模式。	R
b9	HLTST	CAN停止状态标志	0：不处于CAN停止模式1：处于CAN停止模式。	R
b10	SLPST	CAN睡眠状态标志	0：不处于CAN睡眠模式1：处于CAN睡眠模式。	R
b11	EPST	错误被动状态标志	0：不处于被动错误状态1：处于被动错误状态。	R
b12	BOST	总线关闭状态标志	0：不处于总线关闭状态 1：处于总线关闭状态。	R
b13	TRMST	发送状态标志	0：总线空闲或接收中1：传输中或模块处于总线关闭状态。	R
b14	RECST	接收状态标志	0：总线空闲或传输中1：接收中。	R
b15	—	Reserved	该位读为0。	R

NDST标志（NEWDATA状态标志）

当MCTL_RXj(j=0to31)中的至少一个NEWDATA标志为1时，NDST标志设置为1，无论MIER或MIER_FIFO。当所有NEWDATA标志为0时，它设置为0。

SDST标志（SENTDATA状态标志）

当MCTL_TXj(j=0to31)中的至少一个SENTDATA标志为1时，SDST标志设置为1，无论MIER或MIER_FIFO。当所有SENTDATA标志为0时，它设置为0。

RFST标志（接收FIFO状态标志）

当接收FIFO不为空时，RFST标志设置为1。当接收FIFO为空或选择正常邮箱模式时，它设置为0。

TFST flag (Transmit FIFO Status Flag)

The TFST flag is set to 1 when the transmit FIFO is not full. It is set to 0 when the transmit FIFO is full or normal mailbox mode is selected.

NMLST flag (Normal Mailbox Message Lost Status Flag)

The NMLST flag is set to 1 when at least one MSGLOST flag in MCTL_RXj (j = 0 to 31) is 1, regardless of the value of MIER or MIER_FIFO. It is set to 0 when all MSGLOST flags are 0.

FMLST flag (FIFO Mailbox Message Lost Status Flag)

The FMLST flag is set to 1 when the RFMLF flag in RFCR is 1, regardless of the value of MIER_FIFO. It is set to 0 when the RFMLF flag is 0.

TABST flag (Transmission Abort Status Flag)

The TABST flag is set to 1 when at least one TRMABT flag in MCTL_TXj (j = 0 to 31) is 1, regardless of the value of MIER or MIER_FIFO. It is set to 0 when all TRMABT flags are 0.

EST flag (Error Status Flag)

The EST flag is set to 1 when at least one error is detected by EIFR, regardless of the value of EIER. It is set to 0 when no error is detected by EIFR.

RSTST flag (CAN Reset Status Flag)

The RSTST flag is set to 1 when the CAN module is in CAN reset mode. It is 0 when the CAN module is not in CAN reset mode. It remains 1, even when the state changes from CAN reset to sleep mode.

HLTST flag (CAN Halt Status Flag)

The HLTST flag is set to 1 when the CAN module is in CAN halt mode. It is set to 0 when the CAN module is not in CAN halt mode. It remains 1, even when the state changes from CAN halt to sleep mode.

SLPST flag (CAN Sleep Status Flag)

The SLPST flag is set to 1 when the CAN module is in CAN sleep mode. It is set to 0 when the CAN module is not in CAN sleep mode.

EPST flag (Error-Passive Status Flag)

The EPST flag is set to 1 when the value of TECR or RECR exceeds 127 and the CAN module is in an error-passive state ($128 \leq TEC < 256$ or $128 \leq REC < 256$). It is set to 0 when the CAN module is not in the error-passive state.

BOST flag (Bus-Off Status Flag)

The BOST flag is set to 1 when the value of TECR exceeds 255 and the CAN module is in the bus-off state ($TEC \geq 256$). It is set to 0 when the CAN module is not in the bus-off state.

TRMST flag (Transmit Status Flag)

The TRMST flag is set to 1 when the CAN module performs as a transmitter node or is in the bus-off state. It is set to 0 when the CAN module performs as a receiver node or is in the bus-idle state.

RECST flag (Receive Status Flag)

The RECST flag is set to 1 when the CAN module performs as a receiver node. It is set to 0 when the CAN module performs as a transmitter node or is in the bus-idle state.

TFST标志（发送FIFO状态标志）

当发送FIFO未满时，TFST标志设置为1。当发送FIFO已满或选择正常邮箱模式时，它设置为0。

NMLST标志（正常邮箱消息丢失状态标志）

当MCTL_RXj(j=0to31)中的至少一个MSGLOST标志为1时，NMLST标志设置为1，无论MIER或MIER_FIFO。当所有MSGLOST标志为0时，它设置为0。

FMLST标志（FIFO邮箱消息丢失状态标志）

当RFCR中的RFMLF标志为1时，无论MIER_FIFO的值如何，FMLST标志都设置为1。当RFMLF标志为0时，它设置为0。

TABST标志（传输中止状态标志）

当MCTL_TXj(j=0到31)中的至少一个TRMABT标志为1时，TABST标志设置为1，无论MIER或MIER_FIFO。当所有TRMABT标志为0时，它设置为0。

EST标志（错误状态标志）

当EIFR检测到至少一个错误时，无论EIER的值如何，EST标志设置为1。当EIFR未检测到错误时，它设置为0。

RSTST标志（CAN复位状态标志）

当CAN模块处于CAN复位模式时，RSTST标志设置为1。CAN模块不处于CAN复位模式时为0。即使状态从CAN复位变为睡眠模式，它仍保持为1。

HLTST标志（CAN停止状态标志）

当CAN模块处于CAN暂停模式时，HLTST标志设置为1。CAN模块不在时设置为0
CAN暂停模式。即使状态从CAN停止变为睡眠模式，它仍保持为1。

SLPST标志（CAN睡眠状态标志）

当CAN模块处于CAN睡眠模式时，SLPST标志设置为1。CAN模块不在时设置为0
CAN睡眠模式。

EPST标志（错误被动状态标志）

当TECR或RECR的值超过127并且CAN模块处于错误被动状态（128≤TEC<256或128≤REC<256）时，EPST标志设置为1。当CAN模块不处于被动错误状态时，它设置为0。

BOST标志（总线关闭状态标志）

当TECR的值超过255并且CAN模块处于总线关闭状态（TEC≥256）时，BOST标志设置为1。
CAN模块不处于总线关闭状态时设置为0。

TRMST标志（发送状态标志）

当CAN模块作为发送器节点运行或处于总线关闭状态时，TRMST标志设置为1。当CAN模块作为接收器节点或处于总线空闲状态时，它设置为0。

RECST标志（接收状态标志）

当CAN模块作为接收器节点运行时，RECST标志设置为1。当CAN模块作为发送器节点或处于总线空闲状态时，它设置为0。

37.2.16 Mailbox Search Mode Register (MSMR)

Address(es): CAN0.MSMR 4005 0853h, CAN1.MSMR 4005 1853h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	MBSM[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	MBSM[1:0]	Mailbox Search Mode Select	b1 b0 0 0: Receive mailbox search mode 0 1: Transmit mailbox search mode 1 0: Message lost search mode 1 1: Channel search mode.	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Write to MSMR in CAN operation or halt mode.

MBSM[1:0] bits (Mailbox Search Mode Select)

The MBSM[1:0] bits select the search mode for the mailbox search function.

When the MBSM[1:0] bits are 00b, receive mailbox search mode is selected. In this mode, the search targets are the NEWDATA flag in MCTL_RXj (j = 0 to 31) for the normal mailbox and the RFEST bit in RFCR.

When the MBSM[1:0] bits are 01b, transmit mailbox search mode is selected. In this mode, the search target is the SENTDATA flag in MCTL_TXj.

When the MBSM[1:0] bits are 10b, message lost search mode is selected. In this mode, the search targets are the MSGLOST flag in MCTL_RXj for the normal mailbox and the RFMLF flag in RFCR.

When the MBSM[1:0] bits are 11b, channel search mode is selected. In this mode, the search target is CSSR. See section 37.2.18, Channel Search Support Register (CSSR).

37.2.17 Mailbox Search Status Register (MSSR)

Address(es): CAN0.MSSR 4005 0852h, CAN1.MSSR 4005 1852h

	b7	b6	b5	b4	b3	b2	b1	b0
	SEST	—	—	MBNST[4:0]				
Value after reset:	1	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b4 to b0	MBNST[4:0]	Search Result Mailbox Number Status	These bits output the smallest mailbox number that is found in each mode of MSMR.	R
b6, b5	—	Reserved	These bits are read as 0.	R
b7	SEST	Search Result Status	0: Search result found 1: No search result.	R

MBNST[4:0] bits (Search Result Mailbox Number Status)

In all MSMR modes, the MBNST[4:0] bits output the smallest found mailbox number. In receive mailbox search mode, transmit mailbox search mode, and message lost search mode, the value of the mailbox (the search result to be output) is updated under the following conditions:

- When the NEWDATA, SENTDATA, or MSGLOST flag for a mailbox output by MBNST is set to 0
- When the NEWDATA, SENTDATA, or MSGLOST flag for a mailbox with a smaller number than of MBNST is

37.2.16 邮箱搜索模式寄存器(MSMR)

Address(es): CAN0.MSMR 4005 0853h, CAN1.MSMR 4005 1853h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	MBSM[1:0]	
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b1, b0	MBSM[1:0]	邮箱搜索模式选择	b1b000：接收邮箱搜索模式01：发送邮箱搜索模式10：消息丢失搜索模式11：频道搜索模式。	R/W
b7 to b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W

在CAN操作或暂停模式下写入MSMR。

MBSM[1:0]位（邮箱搜索模式选择）

MBSM[1:0]位选择邮箱搜索功能的搜索模式。

当MBSM[1:0]位为00b时，选择接收邮箱搜索模式。在这种模式下，搜索目标是MCTL_RXj中的NEWDATA标志（j=0到31）用于普通邮箱和RFCR中的RFEST位。

当MBSM[1:0]位为01b时，选择发送邮箱搜索模式。在这种模式下，搜索目标是MCTL_TXj中的SENTDATA标志。

当MBSM[1:0]位为10b时，选择消息丢失搜索模式。在这种模式下，搜索目标是正常邮箱的MCTL_RXj中的MSGLOST标志和RFCR中的RFMLF标志。

当MBSM[1:0]位为11b时，选择频道搜索模式。在这种模式下，搜索目标是CSSR。请参阅第37.2.18节，频道搜索支持寄存器(CSSR)。

37.2.17 邮箱搜索状态寄存器(MSSR)

Address(es): CAN0.MSSR 4005 0852h, CAN1.MSSR 4005 1852h

	b7	b6	b5	b4	b3	b2	b1	b0
	SEST	—	—	MBNST[4:0]				
重置后的值：	1	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b4 to b0	MBNST[4:0]	搜索结果邮箱号码状态	这些位输出在MSMR的每个模式中找到的最小邮箱号。	R
b6, b5	—	Reserved	这些位读为0。	R
b7	SEST	搜索结果状态	0：找到搜索结果1：没有搜索结果。	R

MBNST[4:0]位（搜索结果邮箱号码状态）

在所有MSMR模式下，MBNST[4:0]位输出找到的最小邮箱号。在接收邮箱搜索模式、发送邮箱搜索模式和消息丢失搜索模式下，邮箱的值（要输出的搜索结果）在以下条件下更新：

- 当MBNST输出的邮箱的NEWDATA、SENTDATA或MSGLOST标志设置为0时
- 当邮箱的NEWDATA、SENTDATA或MSGLOST标志为小于MBNST的邮箱时

set to 1.

If the MBSM[1:0] bits are set to 00b (receive mailbox search mode) or 10b (message lost search mode), the receive FIFO (mailbox 28) is output when it is not empty and there are no unread received messages and no lost messages in any of the normal mailboxes (0 to 23). If the MBSM[1:0] bits are set to 01b (transmit mailbox search mode), the transmit FIFO (mailbox 24) is not output. Table 37.6 lists the behavior of the MBNST[4:0] bits in FIFO mailbox mode.

In channel search mode, the MBNST[4:0] bits output the associated channel number. After MSSR is read by software, the next target channel number is output.

SEST bit (Search Result Status)

The SEST bit is set to 1 (no search result) when no associated mailbox is found after searching all mailboxes. For example, in transmit mailbox search mode, the SEST bit is set to 1 when no SENTDATA flag for the mailboxes is 1. The SEST bit is set to 0 when at least one SENTDATA flag is 1. When the SEST bit is 1, the value of the MBNST[4:0] bits is undefined.

Table 37.6 Behavior of MBNST[4:0] bits in FIFO mailbox mode

MBSM[1:0] bits	Mailbox 24 (transmit FIFO)	Mailbox 28 (receive FIFO)
00b	Mailbox 24 is not output.	Mailbox 28 is output when no MCTL_RXj.NEWDATA flag for the normal mailboxes is set to 1 (new message is being stored or was stored in the mailbox) and the receive FIFO is not empty.
01b		Mailbox 28 is not output.
10b		Mailbox 28 is output when no MCTL_RXj.MSGLOST flag for the normal mailboxes is set to 1 (message is overwritten or overrun) and the RFCR.RFMLF flag is set to 1 (receive FIFO message lost) in the receive FIFO.
11b		Mailbox 28 is not output.

37.2.18 Channel Search Support Register (CSSR)

Address(es): CAN0.CSSR 4005 0851h, CAN1.CSSR 4005 1851h

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Description	R/W
b7 to b0	When the value for the channel search is input, the channel number is output to MSSR.	R/W

The bits in CSSR, which are set to 1, are encoded by an 8/3 encoder (the LSB position has the higher priority) and output to the MBNST[4:0] bits in MSSR. MSSR outputs the updated value whenever MSSR is read by software.

Write to CSSR only when the MSMR.MBSM[1:0] bits are 11b (channel search mode). Write to CSSR in CAN operation mode or CAN halt mode.

Figure 37.4 shows writes to and reads from CSSR and MSSR.

设置为1。

如果MBSM[1:0]位设置为00b（接收邮箱搜索模式）或10b（邮件丢失搜索模式），则在接收FIFO（邮箱28）不为空且没有未读接收到的消息时输出在任何普通邮箱（0到23）中都没有丢失消息。如果MBSM[1:0]位设置为01b（发送邮箱搜索模式），则不输出发送FIFO（邮箱24）。表37.6列出了MBNST[4:0]位在FIFO邮箱模式下的行为。

在频道搜索模式下，MBNST[4:0]位输出相关的频道号。软件读取MSSR后，输出下一个目标通道号。

SEST位（搜索结果状态）

当搜索所有邮箱后未找到相关邮箱时，SEST位设置为1（无搜索结果）。例如，在发送邮箱搜索模式中，当邮箱没有SENTDATA标志为1时，SEST位设置为1。当至少一个SENTDATA标志为1时，SEST位设置为0。当SEST位为1时，MBNST[4:0]位的值未定义。

Table 37.6 FIFO邮箱模式下MBNST[4:0]位的行为

MBSM[1:0] bits	Mailbox 24 (transmit FIFO)	Mailbox 28 (receive FIFO)
00b	邮箱24不输出。	当正常邮箱的MCTL_RXj.NEWDATA标志未设置为1（新消息正在存储或已存储在邮箱中）且接收FIFO不为空时，输出邮箱28。
01b		邮箱28不输出。
10b		当正常邮箱的MCTL_RXj.MSGLOST标志未设置为1（消息被覆盖或溢出）且接收FIFO中的RFCR.RFMLF标志设置为1（接收FIFO消息丢失）时，输出邮箱28。
11b		邮箱28不输出。

37.2.18 频道搜索支持寄存器(CSSR)

Address(es): CAN0.CSSR 4005 0851h, CAN1.CSSR 4005 1851h

	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	x	x	x	x	x	x	x	x

x: Undefined

Bit	Description	R/W
b7 to b0	输入频道搜索的值时，频道号将输出到MSSR。	R/W

CSSR中设置为1的位由83编码器（LSB位置具有较高优先级）编码并输出到MSSR中的MBNST[4:0]位。每当MSSR被软件读取时，MSSR就会输出更新的值。

仅当MSMR.MBSM[1:0]位为11b（通道搜索模式）时才写入CSSR。在CAN操作模式或CAN暂停模式下写入CSSR。

图37.4显示了对CSSR和MSSR的写入和读取。

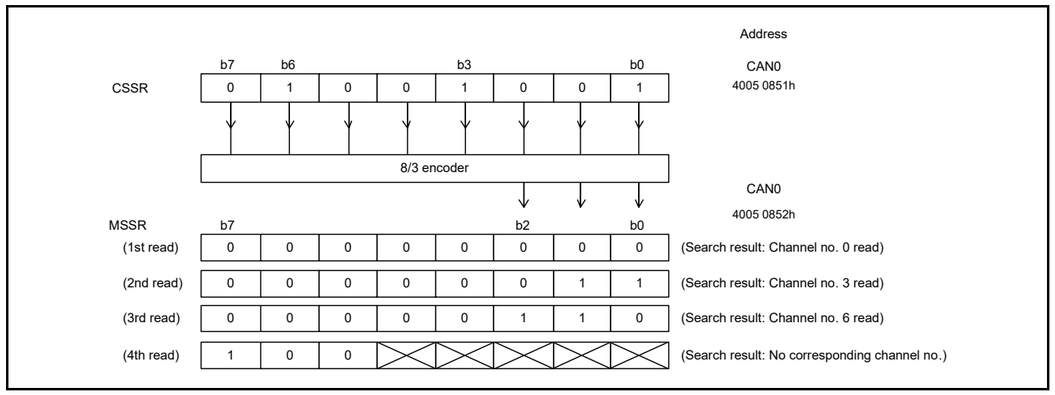


Figure 37.4 Writes to and reads from CSSR and MSSR

The value of CSSR is also updated whenever MSSR is read. On this read, the value prior to conversion by the 8/3 encoder can be read.

37.2.19 Acceptance Filter Support Register (AFSR)

Address(es): CAN0.AFSR 4005 0856h, CAN1.AFSR 4005 1856h

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Description	R/W
b15 to b0	After the standard ID of a received message is written, the value converted for data table search can be read.	R/W

Note: Write to AFSR in CAN operation mode or CAN halt mode.

The acceptance filter support unit (ASU) can be used for data table (8 bits × 256) searches. In the data table, all standard IDs that you create are set as valid or invalid in bit units. When AFSR is written with data in 16-bit units including the SID[10:0] bits in MBj_ID (j = 0 to 31), in which a received standard ID is stored, a decoded row (byte offset) position and column (bit) position for data table search can be read. The ASU can be used for standard (11-bit) IDs only.

The ASU is enabled in the following cases:

- When the ID to be received cannot be masked by the acceptance filter. For example, if IDs to be received are 078h, 087h, and 111h
- When there are too many IDs to receive, and the software filtering time is expected to be shortened.

Note: AFSR cannot be set in CAN reset mode.

Figure 37.5 shows the writes to and reads from AFSR.

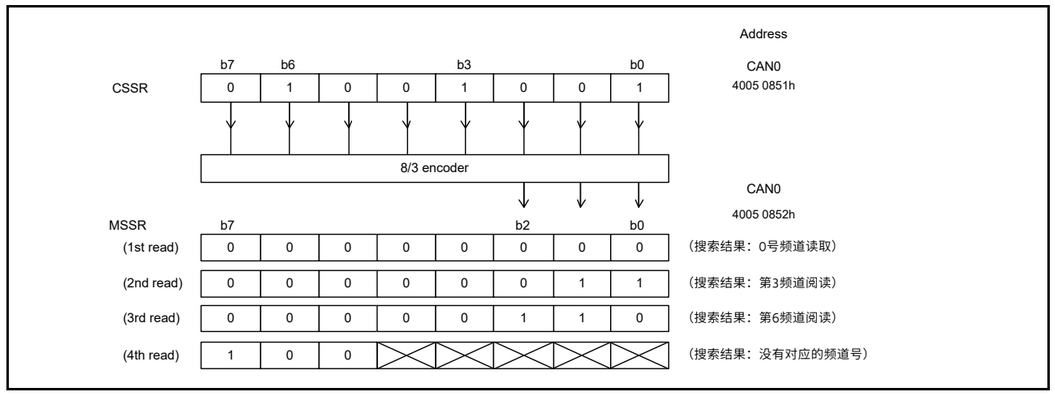


Figure 37.4 读写CSSR和MSSR

每当读取MSSR时，CSSR的值也会更新。在此读取中，可以读取83编码器转换之前的值。

37.2.19 接受过滤器支持寄存器(AFSR)

Address(es): CAN0.AFSR 4005 0856h, CAN1.AFSR 4005 1856h

b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Description	R/W
b15 to b0	将接收到的消息的标准ID写入后，就可以读取为数据查表转换的值了。	R/W

Note: 在CAN操作模式或CAN暂停模式下写入AFSR。

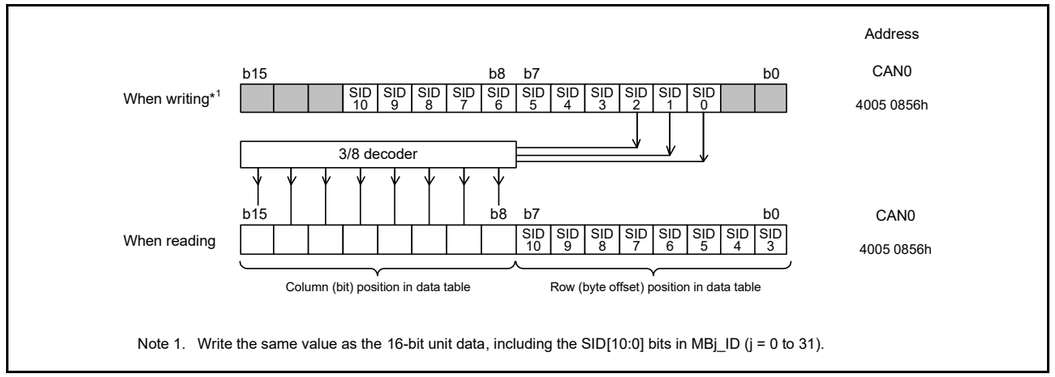
验收滤波器支持单元(ASU)可用于数据表（8位×256）搜索。在数据表中，所有标准
您创建的ID以位为单位设置为有效或无效。当AFSR以16位单元写入数据时，包括MBj_ID(j=0到31)中的SID[10:0]位，其中存储了接收到的标准ID，解码的行（字节偏移）位置和列（位）数据表搜索的位置可以被读取。ASU只能用于标准（11位）ID。

ASU在以下情况下启用：

- 当接受过滤器不能屏蔽要接收的ID时。例如，如果要接收的ID是078h、087h和111h
- 当接收的ID太多时，预计软件过滤时间会缩短。

Note: CAN复位模式下不能设置AFSR。

图37.5显示了对AFSR的写入和读取。



Note 1. Write the same value as the 16-bit unit data, including the SID[10:0] bits in MBj_ID (j = 0 to 31).

Figure 37.5 Writes to and reads from AFSR

37.2.20 Error Interrupt Enable Register (EIER)

Address(es): CAN0.EIER 4005 084Ch, CAN1.EIER 4005 184Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	BLIE	OLIE	ORIE	BORIE	BOEIE	EPIE	EWIE	BEIE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	BEIE	Bus Error Interrupt Enable	0: Disable interrupt 1: Enable interrupt.	R/W
b1	EWIE	Error-Warning Interrupt Enable	0: Disable interrupt 1: Enable interrupt.	R/W
b2	EPIE	Error-Passive Interrupt Enable	0: Disable interrupt 1: Enable interrupt.	R/W
b3	BOEIE	Bus-Off Entry Interrupt Enable	0: Disable interrupt 1: Enable interrupt.	R/W
b4	BORIE	Bus-Off Recovery Interrupt Enable	0: Disable interrupt 1: Enable interrupt.	R/W
b5	ORIE	Overrun Interrupt Enable	0: Disable interrupt 1: Enable interrupt.	R/W
b6	OLIE	Overload Frame Transmit Interrupt Enable	0: Disable interrupt 1: Enable interrupt.	R/W
b7	BLIE	Bus Lock Interrupt Enable	0: Disable interrupt 1: Enable interrupt.	R/W

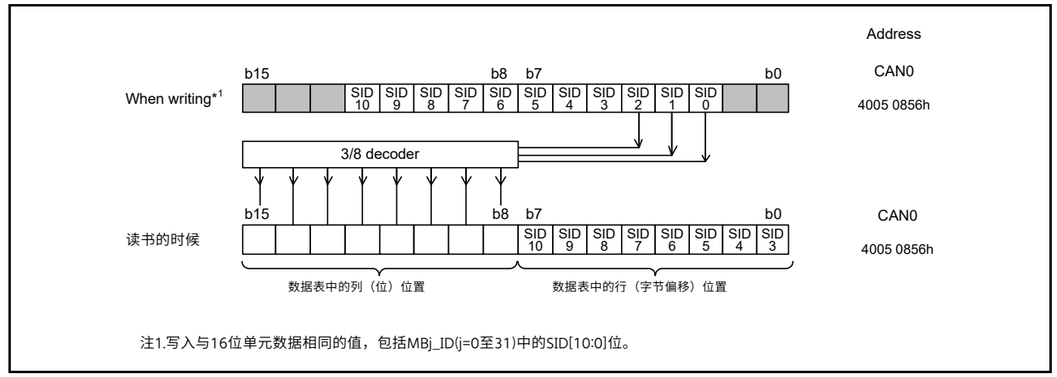
EIER enables or disables each error interrupt source independently in EIFR. Write to EIER in CAN reset mode.

BEIE bit (Bus Error Interrupt Enable)

When the BEIE bit is 0, no error interrupt request occurs even if the BEIF bit in EIFR is 1. When the BEIE bit is 1, an error interrupt request occurs if the BEIF bit is set to 1.

EWIE bit (Error-Warning Interrupt Enable)

When the EWIE bit is 0, no error interrupt request occurs even if the EWIF bit in EIFR is 1. When the EWIE bit is 1, an error interrupt request is generated if the EWIF bit is set to 1.



注1.写入与16位单元数据相同的值，包括MBj_ID(j=0至31)中的SID[10:0]位。

Figure 37.5 写入和读取AFSR

37.2.20 错误中断使能寄存器(EIER)

Address(es): CAN0.EIER 4005 084Ch, CAN1.EIER 4005 184Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	BLIE	OLIE	ORIE	BORIE	BOEIE	EPIE	EWIE	BEIE
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	BEIE	总线错误中断使能	0：禁用中断1：启用中断。	R/W
b1	EWIE	错误警告中断使能	0：禁用中断1：启用中断。	R/W
b2	EPIE	错误被动中断使能	0：禁用中断1：启用中断。	R/W
b3	BOEIE	总线关闭进入中断使能	0：禁用中断1：启用中断。	R/W
b4	BORIE	总线关闭恢复中断使能	0：禁用中断1：启用中断。	R/W
b5	ORIE	溢出中断使能	0：禁用中断1：启用中断。	R/W
b6	OLIE	过载帧发送中断 Enable	0：禁用中断1：启用中断。	R/W
b7	BLIE	总线锁定中断使能	0：禁用中断1：启用中断。	R/W

EIER在EIFR中独立启用或禁用每个错误中断源。在CAN复位模式下写入EIER。

BEIE位（总线错误中断使能）

当BEIE位为0时，即使EIFR中的BEIF位为1，也不会发生错误中断请求。当BEIE位为1时，如果BEIF位设置为1，则会发生错误中断请求。

EWIE位（错误警告中断使能）

当EWIE位为0时，即使EIFR中的EWIF位为1，也不会产生错误中断请求。当EWIE位为1时，如果EWIF位被设置为1，则产生错误中断请求。

EPIE bit (Error-Passive Interrupt Enable)

When the EPIE bit is 0, no error interrupt request occurs even if the EPIF bit in EIFR is 1. When the EPIE bit is 1, an error interrupt request occurs if the EPIF bit is set to 1.

BOEIE bit (Bus-Off Entry Interrupt Enable)

When the BOEIE bit is 0, no error interrupt request occurs even if the BOEIF bit in EIFR is 1. When the BOEIE bit is 1, an error interrupt request occurs if the BOEIF bit is set to 1.

BORIE bit (Bus-Off Recovery Interrupt Enable)

When the BORIE bit is 0, no error interrupt request occurs even if the BORIF bit in EIFR is 1. When the BORIE bit is 1, an error interrupt request occurs if the BORIF bit is set to 1.

ORIE bit (Overrun Interrupt Enable)

When the ORIE bit is 0, no error interrupt request occurs even if the ORIF bit in EIFR is 1. When the ORIE bit is 1, an error interrupt request occurs if the ORIF bit is set to 1.

OLIE bit (Overload Frame Transmit Interrupt Enable)

When the OLIE bit is 0, no error interrupt request occurs even if the OLIF bit in EIFR is 1. When the OLIE bit is 1, an error interrupt request occurs if the OLIF bit is set to 1.

BLIE bit (Bus Lock Interrupt Enable)

When the BLIE bit is 0, no error interrupt request occurs even if the BLIF bit in EIFR is 1. When the BLIE bit is 1, an error interrupt request occurs if the BLIF bit is set to 1.

37.2.21 Error Interrupt Factor Judge Register (EIFR)

Address(es): CAN0.EIFR 4005 084Dh, CAN1.EIFR 4005 184Dh

	b7	b6	b5	b4	b3	b2	b1	b0
	BLIF	OLIF	ORIF	BORIF	BOEIF	EPIF	EWIF	BEIF
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	BEIF	Bus Error Detect Flag	0: No bus error detected 1: Bus error detected.	R/W
b1	EWIF	Error-Warning Detect Flag	0: No error-warning detected 1: Error-warning detected.	R/W
b2	EPIF	Error-Passive Detect Flag	0: No error-passive detected 1: Error-passive detected.	R/W
b3	BOEIF	Bus-Off Entry Detect Flag	0: No bus-off entry detected 1: Bus-off entry detected.	R/W
b4	BORIF	Bus-Off Recovery Detect Flag	0: No bus-off recovery detected 1: Bus-off recovery detected.	R/W
b5	ORIF	Receive Overrun Detect Flag	0: No receive overrun detected 1: Receive overrun detected.	R/W
b6	OLIF	Overload Frame Transmission Detect Flag	0: No overload frame transmission detected 1: Overload frame transmission detected.	R/W
b7	BLIF	Bus Lock Detect Flag	0: No bus lock detected 1: Bus lock detected.	R/W

If an event associated with one of these bits occurs, the associated bit in EIFR is set to 1, regardless of the setting of EIER.

Clear the bits to 0 through a software write. If a bit is set to 1 at the same time that the software clears it, it becomes 1. When setting a single bit to 0 in the software, use the transfer instruction (MOV) to ensure that only the specified bit is

EPIE位（错误被动中断使能）

当EPIE位为0时，即使EIFR中的EPIF位为1，也不会产生错误中断请求。当EPIE位为1时，如果EPIF位被设置为1，则会产生错误中断请求。

BOEIE位（总线关闭进入中断使能）

当BOEIE位为0时，即使EIFR中的BOEIF位为1，也不会产生错误中断请求。当BOEIE位为1时，如果将BOEIF位设置为1，则会产生错误中断请求。

BORIE位（总线关闭恢复中断使能）

当BORIE位为0时，即使EIFR中的BORIF位为1，也不会发生错误中断请求。当BORIE位为1时，如果BORIF位设置为1，则会发生错误中断请求。

ORIE位（溢出中断使能）

当ORIE位为0时，即使EIFR中的ORIF位为1，也不会发生错误中断请求。当ORIE位为1时，如果ORIF位设置为1，则会发生错误中断请求。

OLIE位（过载帧发送中断使能）

当OLIE位为0时，即使EIFR中的OLIF位为1，也不会发生错误中断请求。当OLIE位为1时，如果OLIF位设置为1，则会发生错误中断请求。

BLIE位（总线锁定中断使能）

当BLIE位为0时，即使EIFR中的BLIF位为1，也不会产生错误中断请求。当BLIE位为1时，如果BLIF位被设置为1，则会产生错误中断请求。

37.2.21 错误中断因素判断寄存器（EIFR）

Address(es): CAN0.EIFR 4005 084Dh, CAN1.EIFR 4005 184Dh

	b7	b6	b5	b4	b3	b2	b1	b0
	BLIF	OLIF	ORIF	BORIF	BOEIF	EPIF	EWIF	BEIF
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	BEIF	总线错误检测标志	0：未检测到总线错误1 ：检测到总线错误。	R/W
b1	EWIF	错误警告检测标志	0：未检测到错误警告1：检 测到错误警告。	R/W
b2	EPIF	错误被动检测标志	0：未检测到被动错误1：检 测到被动错误。	R/W
b3	BOEIF	总线关闭进入检测标志	0：未检测到总线关闭条目1 ：检测到总线关闭条目。	R/W
b4	BORIF	总线关闭恢复检测标志	0：未检测到总线关闭恢复1： 检测到总线关闭恢复。	R/W
b5	ORIF	接收溢出检测标志	0：未检测到接收溢出1：检测 到接收溢出。	R/W
b6	OLIF	过载帧传输 检测标志	0：未检测到过载帧传输1：检测到过载帧传 输。	R/W
b7	BLIF	总线锁定检测标志	0：未检测到总线锁定1 ：检测到总线锁定。	R/W

如果发生与这些位之一相关的事件，则EIFR中的相关位设置为1，而不管EIER.

通过软件写入将这些位清除为0。如果某位在软件清零的同时置1，则变为1。在软件中设置单个位为0时，使用传输指令（MOV）确保只有指定位为

set to 0 and the other bits are set to 1. Writing 1 has no effect to these bit values.

BEIF flag (Bus Error Detect Flag)

The BEIF flag is set to 1 when a bus error is detected.

EWIF flag (Error-Warning Detect Flag)

The EWIF flag is set to 1 when the value of the receive error counter (REC) or transmit error counter (TEC) exceeds 95. It is set to 1 only when REC or TEC initially exceeds 95. If 0 is written to the EWIF flag by software while REC or TEC remains greater than 95, the EWIF flag does not set to 1 until REC or TEC goes below 95 and then exceeds 95 again.

EPIF flag (Error-Passive Detect Flag)

The EPIF flag is set to 1 when the CAN error state becomes error-passive, when the receive error counter (REC) or transmit error counter (TEC) value exceeds 127. It is set to 1 only when REC or TEC initially exceeds 127. If 0 is written to the EPIF flag by software while REC or TEC remains greater than 127, the flag does not set to 1 until REC or TEC goes below 127 and then exceeds 127 again.

BOEIF flag (Bus-Off Entry Detect Flag)

The BOEIF flag is set to 1 when the CAN error state becomes bus-off, when the transmit error counter (TEC) value exceeds 255. It also is set to 1 when the BOM[1:0] bits in CTLR are 01b (automatic entry to CAN halt mode on bus-off entry) and the CAN module becomes the bus-off state.

BORIF flag (Bus-Off Recovery Detect Flag)

The BORIF flag is set to 1 when the CAN module recovers from the bus-off state normally by detecting 11 consecutive recessive bits 128 times in the following conditions:

- When the BOM[1:0] bits in CTLR are 00b
- When the BOM[1:0] bits in CTLR are 10b
- When the BOM[1:0] bits in CTLR are 11b.

However, the BORIF flag does not set to 1 if the CAN module recovers from the bus-off state in the following conditions:

- When the CANM[1:0] bits in CTLR are set to 01b or 11b (CAN reset mode)
- When the RBOC bit in CTLR is set to 1 (forced return from bus-off)
- When the BOM[1:0] bits in CTLR are set to 01b
- When the BOM[1:0] bits in CTLR are set to 11b and the CANM[1:0] bits in CTLR are set to 10b (CAN halt mode) before normal recovery occurs.

Table 37.7 lists the behavior of the BOEIF and BORIF bits for each CTLR.BOM[1:0] bit setting.

Table 37.7 Behavior of BOEIF and BORIF flags for each CTLR.BOM[1:0] setting

BOM[1:0] bits	BOEIF bit	BORIF bit
00b	Set to 1 on entry to the bus-off state	Sets to 1 on exit from the bus-off state
01b		Does not set to 1
10b		Sets to 1 on exit from the bus-off state
11b		Sets to 1 if normal bus-off recovery occurs before the CANM[1:0] bits are set to 10b (CAN halt mode)

ORIF flag (Receive Overrun Detect Flag)

The ORIF flag is set to 1 when a receive overrun occurs. It does not set to 1 in overwrite mode.

In overwrite mode, a reception complete interrupt request occurs if an overwrite condition occurs and the ORIF bit is not set to 1.

设置为0，其他位设置为1。写入1对这些位值没有影响。

BEIF标志（总线错误检测标志）

当检测到总线错误时，BEIF标志设置为1。

EWIF标志（错误警告检测标志）

当接收错误计数器(REC)或发送错误计数器(TEC)的值超过95时，EWIF标志设置为1。仅当REC或TEC最初超过95时设置为1。如果将0写入EWIF标志通过软件，当REC或TEC保持大于95时，EWIF标志不会设置为1，直到REC或TEC低于95，然后再次超过95。

EPIF标志（错误被动检测标志）

当CAN错误状态变为被动错误，当接收错误计数器(REC)或发送错误计数器(TEC)值超过127时，EPIF标志设置为1。仅当REC或TEC最初超过127时，它才设置为1。如果0被软件写入EPIF标志，而REC或TEC保持大于127，则标志不会设置为1，直到REC或TEC低于127，然后再次超过127。

BOEIF标志（总线关闭进入检测标志）

当CAN错误状态变为总线关闭时，当发送错误计数器(TEC)值超过255时，BOEIF标志设置为1。当CTLR中的BOM[1:0]位为01b（自动进入总线关闭时进入CAN暂停模式）并且CAN模块变为总线关闭状态。

BORIF标志（总线关闭恢复检测标志）

当CAN模块在以下情况下通过检测11个连续的隐性位128次从总线关闭状态正常恢复时，BORIF标志设置为1：

- CTLR的BOM[1:0]位为00b时
- CTLR中BOM[1:0]位为10b时
- 当CTLR的BOM[1:0]位为11b时。

但是，如果CAN模块在以下情况下从总线关闭状态恢复，则BORIF标志不会设置为1：

- 当CTLR中的CANM[1:0]位设置为01b或11b时（CAN复位模式）
- 当CTLR的RBOC位设置为1时（从总线关闭强制返回）
- 当CTLR中的BOM[1:0]位设置为01b
- 当CTLR中的BOM[1:0]位设置为11b且CTLR中的CANM[1:0]位设置为10b（CAN停止模式）时，才会发生正常恢复。

表37.7列出了每个CTLR.BOM[1:0]位设置的BOEIF和BORIF位的行为。

Table 37.7 每个CTLR.BOM[1:0]设置的BOEIF和BORIF标志的行为

BOM[1:0] bits	BOEIF bit	BORIF bit
00b	进入总线关闭状态时设置为1	退出总线关闭状态时设置为1
01b		不设置为1
10b		退出总线关闭状态时设置为1
11b		如果在CANM[1:0]位设置为10b（CAN停止模式）之前发生正常的总线关闭恢复，则设置为1

ORIF标志（接收溢出检测标志）

当发生接收溢出时，ORIF标志设置为1。在覆盖模式下它不会设置为1。

在覆盖模式下，如果出现覆盖条件且ORIF位未设置为1，则会产生接收完成中断请求。

In overrun mode with normal mailbox mode, if an overrun occurs in any of mailboxes 0 to 31, this flag is set to 1. In overrun mode with FIFO mailbox mode, if an overrun occurs in any of mailboxes 0 to 23 or the receive FIFO, this bit is set to 1.

OLIF flag (Overload Frame Transmission Detect Flag)

The OLIF flag is set to 1 if the transmitting condition of an overload frame is detected when the CAN module is transmitting or receiving.

BLIF flag (Bus Lock Detect Flag)

The BLIF flag is set to 1 if 32 consecutive dominant bits are detected on the CAN bus while the CAN module is in CAN operation mode. After the BLIF flag is set to 1, 32 consecutive dominant bits are detected again under either of the following conditions:

- Recessive bits are detected after this flag changes to 0 from 1
- The CAN module enters CAN reset or halt mode and then enters CAN operation mode again after this flag changes to 0 from 1.

37.2.22 Receive Error Count Register (RECR)

Address(es): CAN0.RECR 4005 084Eh, CAN1.RECR 4005 184Eh

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Description	R/W
b7 to b0	Receive error count function RECR increments or decrements the counter value based on the error status of the CAN module during reception.	R

RECR indicates the value of the receive error counter. See the CAN specification (ISO11898-1) for the increment and decrement conditions of the receive error counter. The value of RECR in the bus-off state is undefined.

37.2.23 Transmit Error Count Register (TECR)

Address(es): CAN0.TECR 4005 084Fh, CAN1.TECR 4005 184Fh

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0

Bit	Description	R/W
b7 to b0	Transmit error count function TECR increments or decrements the counter value based on the error status of the CAN module during transmission.	R

TECR indicates the value of the transmit error counter. See the CAN specification (ISO11898-1) for the increment and decrement conditions of the transmit error counter. The value of TECR in the bus-off state is undefined.

在具有正常邮箱模式的溢出模式中，如果在任何邮箱0到31中发生溢出，则该标志设置为1。在具有FIFO邮箱模式的溢出模式中，如果在任何邮箱0到23或接收FIFO中发生溢出，该位设置为1。

OLIF标志（过载帧传输检测标志）

如果在CAN模块发送或接收时检测到过载帧的发送条件，则OLIF标志设置为1。

BLIF标志（总线锁定检测标志）

如果在CAN模块处于CAN操作模式时在CAN总线上检测到32个连续显性位，则BLIF标志设置为1。将BLIF标志设置为1后，在以下任一条件下再次检测到32个连续显性位：

- 此标志从1变为0后检测到隐性位
- CAN模块进入CAN复位或停止模式，然后在该标志由1变为0后再次进入CAN操作模式。

37.2.22 接收错误计数寄存器(RECR)

Address(es): CAN0.RECR 4005 084Eh, CAN1.RECR 4005 184Eh

	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	0	0	0	0	0	0	0	0

Bit	Description	R/W
b7 to b0	接收错误计数功能 RECR根据接收期间CAN模块的错误状态递增或递减计数器值。	R

RECR指示接收错误计数器的值。有关接收错误计数器的递增和递减条件，请参见CAN规范(ISO11898-1)。总线关闭状态下RECR的值未定义。

37.2.23 发送错误计数寄存器(TECR)

Address(es): CAN0.TECR 4005 084Fh, CAN1.TECR 4005 184Fh

	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	0	0	0	0	0	0	0	0

Bit	Description	R/W
b7 to b0	发送错误计数功能 TECR根据CAN模块在传输过程中的错误状态递增或递减计数器值。	R

TECR指示发送错误计数器的值。有关发送错误计数器的递增和递减条件，请参见CAN规范(ISO11898-1)。总线关闭状态下的TECR值未定义。

37.2.24 Error Code Store Register (ECSR)

Address(es): CAN0.ECSR 4005 0850h, CAN1.ECSR 4005 1850h

	b7	b6	b5	b4	b3	b2	b1	b0
	EDPM	ADEF	BE0F	BE1F	CEF	AEF	FEF	SEF
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	SEF	Stuff Error Flag*1,*2	0: No stuff error detected 1: Stuff error detected.	R/W
b1	FEF	Form Error Flag*1,*2	0: No form error detected 1: Form error detected.	R/W
b2	AEF	ACK Error Flag*1,*2	0: No ACK error detected 1: ACK error detected.	R/W
b3	CEF	CRC Error Flag*1,*2	0: No CRC error detected 1: CRC error detected.	R/W
b4	BE1F	Bit Error (recessive) Flag*1,*2	0: No bit error (recessive) detected 1: Bit error (recessive) detected.	R/W
b5	BE0F	Bit Error (dominant) Flag*1,*2	0: No bit error (dominant) detected 1: Bit error (dominant) detected.	R/W
b6	ADEF	ACK Delimiter Error Flag*1,*2	0: No ACK delimiter error detected 1: ACK delimiter error detected.	R/W
b7	EDPM	Error Display Mode Select*3,*4	0: Output first detected error code 1: Output accumulated error code.	R/W

Note 1. Writing 1 has no effect on these bit values.
Note 2. To write 0 to the SEF, FEF, AEF, CEF, BE1F, BE0F, and ADEF bits, use the transfer (MOV) instruction to ensure that only the specified bit is set to 0 and the other bits are set to 1.
Note 3. Write to the EDPM bit in CAN reset or halt mode.
Note 4. If more than one error condition is detected simultaneously, all related bits are set to 1.

ECSR indicates whether an error occurs on the CAN bus. See the CAN specification (ISO11898-1) for the conditions when each error occurs.

Clear all of the bits except for the EDPM bit to 0 through a software write. If a bit is set to 1 at the same time that the software clears it, it becomes 1.

SEF flag (Stuff Error Flag)

The SEF flag is set to 1 when a stuff error is detected.

FEF flag (Form Error Flag)

The FEF flag is set to 1 when a form error is detected.

AEF flag (ACK Error Flag)

The AEF flag is set to 1 when an ACK error is detected.

CEF flag (CRC Error Flag)

The CEF flag is set to 1 when a CRC error is detected.

BE1F flag (Bit Error (recessive) Flag)

The BE1F flag is set to 1 when a recessive bit error is detected.

BE0F flag (Bit Error (dominant) Flag)

The BE0F flag is set to 1 when a dominant bit error is detected.

37.2.24 错误代码存储寄存器(ECSR)

Address(es): CAN0.ECSR 4005 0850h, CAN1.ECSR 4005 1850h

	b7	b6	b5	b4	b3	b2	b1	b0
	EDPM	ADEF	BE0F	BE1F	CEF	AEF	FEF	SEF
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	SEF	填充错误标志 *1,*2	0：未检测到填充错误1 ：检测到填充错误。	R/W
b1	FEF	表单错误标志 *1,*2	0：未检测到表单错误1 ：检测到表单错误。	R/W
b2	AEF	ACK错误标志 *1,*2	0：未检测到ACK错误1： 检测到ACK错误。	R/W
b3	CEF	CRC错误标志 *1,*2	0：未检测到CRC错误1： 检测到CRC错误。	R/W
b4	BE1F	位错误（隐性）标志 *1,*2	0：未检测到位错误（隐性）1：检 测到位错误（隐性）。	R/W
b5	BE0F	位错误（显性）标志 *1,*2	0：未检测到位错误（显性）1：检 测到位错误（显性）。	R/W
b6	ADEF	ACK定界符错误标志 *1,*2	0：未检测到ACK分隔符错误1：检 测到ACK分隔符错误。	R/W
b7	EDPM	错误显示模式选择 *3,*4	0：输出第一个检测到的错误代码 1：输出累积错误代码。	R/W

Note 1. 写1对这些位值没有影响。
Note 2. 要将0写入SEF、FEF、AEF、CEF、BE1F、BE0F和ADEF位，请使用传输(MOV)指令确保仅将指定位设置为0，而将其他位设置为1。
Note 3. 在CAN复位或暂停模式下写入EDPM位。
Note 4. 如果同时检测到多个错误条件，则所有相关位都设置为1。

ECSR指示CAN总线上是否发生错误。有关每个错误发生的条件，请参见CAN规范(ISO11898-1)。

通过软件写入将除EDPM位之外的所有位清零。如果在软件清零的同时将某个位设置为1，则该位变为1。

SEF标志（东西错误标志）

当检测到填充错误时，SEF标志设置为1。

FEF标志（表单错误标志）

当检测到表单错误时，FEF标志设置为1。

AEF标志（ACK错误标志）

当检测到ACK错误时，AEF标志设置为1。

CEF标志（CRC错误标志）

当检测到CRC错误时，CEF标志设置为1。

BE1F标志（位错误（隐性）标志）

当检测到隐性位错误时，BE1F标志设置为1。

BE0F标志（位错误（显性）标志）

当检测到显性位错误时，BE0F标志设置为1。

ADEF flag (ACK Delimiter Error Flag)

The ADEF flag is set to 1 when a form error is detected with the ACK delimiter during transmission.

EDPM bit (Error Display Mode Select)

The EDPM bit selects the output mode of ECSR. When the EDPM bit is set to 0, ECSR outputs the first error code. When the EDPM bit is set to 1, ECSR outputs the accumulated error code.

37.2.25 Time Stamp Register (TSR)

Address(es): CAN0.TSR 4005 0854h, CAN1.TSR 4005 1854h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Description	R/W
b15 to b0	Free-running counter value for the time stamp function	R

Note: Read TSR in 16-bit units.

When TSR is read, the value of the time stamp counter (16-bit free-running counter) at that moment is read. The time stamp counter reference clock is configured in the TSPS[1:0] bits in CTLR. The counter stops in CAN sleep and halt modes, and is initialized in CAN reset mode. Its value is stored in the TSL[7:0] and TSH[7:0] bits in MBj_TS when a received message is stored in a receive mailbox.

37.2.26 Test Control Register (TCR)

Address(es): CAN0.TCR 4005 0858h, CAN1.TCR 4005 1858h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	TSTM[1:0]		TSTE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	TSTE	CAN Test Mode Enable	0: Disable CAN test mode 1: Enable CAN test mode.	R/W
b2, b1	TSTM[1:0]	CAN Test Mode Select	b2 b1 0 0: Not CAN test mode 0 1: Listen-only mode 1 0: Self-test mode 0 (external loopback) 1 1: Self-test mode 1 (internal loopback).	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

TCR controls the CAN test mode. Write to TCR in CAN halt mode only.

(1) Listen-only mode

The CAN specification (ISO11898-1) recommends an optional bus monitoring mode. In listen-only mode, valid data frames and valid remote frames can be received. However, only recessive bits can be sent on the CAN bus. The ACK bit, overload flag, and active error flag cannot be sent.

Listen-only mode can be used for baud rate detection.

Do not request transmission from any mailboxes in listen-only mode.

Figure 37.6 shows the connection when listen-only mode is selected.

ADEF标志（ACK分隔符错误标志）

当在传输过程中使用ACK定界符检测到格式错误时，ADEF标志设置为1。

EDP M位（错误显示模式选择）

EDP M位选择ECSR的输出模式。当EDPM位设置为0时，ECSR输出第一个错误代码。
当EDPM位设置为1时，ECSR输出累积的错误代码。

37.2.25 时间戳寄存器(TSR)

Address(es): CAN0.TSR 4005 0854h, CAN1.TSR 4005 1854h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Description	R/W
b15 to b0	时间戳功能的自由运行计数器值	R

Note: 以16位为单位读取TSR。

读取TSR时，读取当时的时间戳计数器（16位自由运行计数器）的值。时间戳计数器参考时钟在CTLR的TSPS[1:0]位中配置。计数器在CAN睡眠和暂停模式下停止，并在CAN复位模式下初始化。当接收到的消息存储在接收邮箱中时，其值存储在MBj_TS中的TSL[7:0]和TSH[7:0]位中。

37.2.26 测试控制寄存器(TCR)

Address(es): CAN0.TCR 4005 0858h, CAN1.TCR 4005 1858h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	TSTM[1:0]		TSTE
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	TSTE	CAN测试模式启用	0：禁用CAN测试模式1： 启用CAN测试模式。	R/W
b2, b1	TSTM[1:0]	CAN测试模式选择	b2b100：非CAN测试模式01：只听模式1 0：自测模式0（外部环回）11：自测模式 1（内部环回）。	R/W
b7 to b3	—	Reserved	这些位被读取为0。写入值应为0。	R/W

TCR控制CAN测试模式。仅在CAN停止模式下写入TCR。

(1) Listen-only mode

CAN规范(ISO11898-1)推荐一种可选的总线监控模式。在只听模式下，可以接收到有效的数据帧和有效的远程帧。但是，只能在CAN总线上发送隐性位。不能发送ACK位、过载标志和活动错误标志。

只听模式可用于波特率检测。

不要在只听模式下从任何邮箱请求传输。

图37.6显示了选择只听模式时的连接。

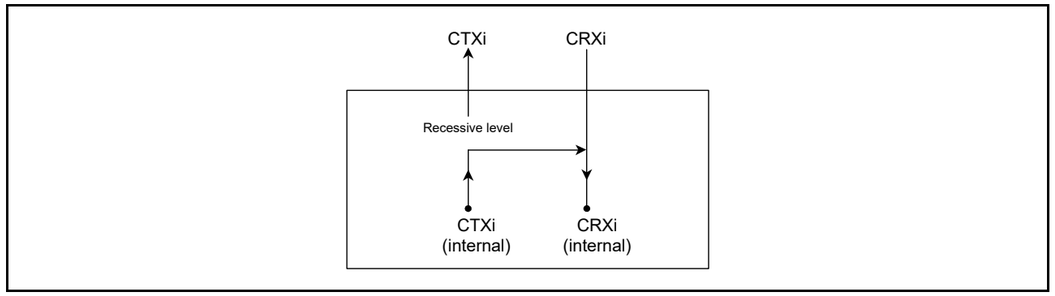


Figure 37.6 Connection when listen-only mode is selected (i = 0, 1)

(2) Self-test mode 0 (external loopback)

Self-test mode 0 is provided for CAN transceiver tests. In this mode, the protocol module treats its own transmitted messages as those received by the CAN transceiver and stores them into the receive mailbox. To be independent from external stimulation, the protocol module generates the ACK bit.

Connect the CTXi and CRXi pins to the transceiver.

Figure 37.7 shows the connection when self-test mode 0 is selected.

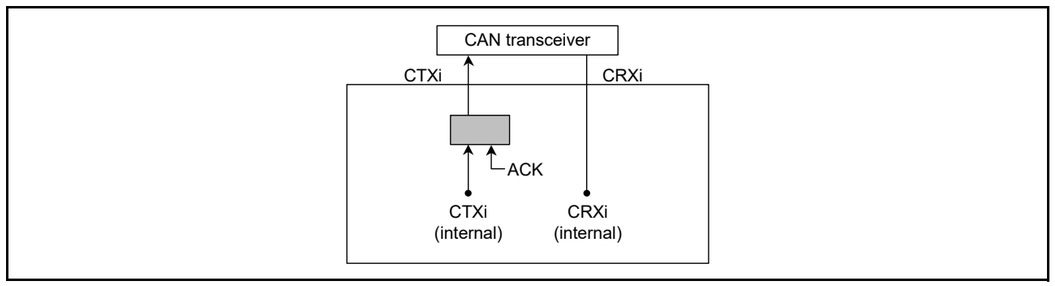


Figure 37.7 Connection when self-test mode 0 is selected (i = 0, 1)

(3) Self-test mode 1 (internal loopback)

Self-test mode 1 is provided for self-test functions.

In self-test mode 1, the protocol controller treats its transmitted messages as received messages and stores them into the receive mailbox. To be independent from external stimulation, the protocol controller generates the ACK bit.

In self-test mode 1, the protocol controller performs an internal feedback from the internal CTXi pin to the internal CRXi pin. The input value of the external CRXi pin is ignored. The external CTXi pin outputs only recessive bits. The CTXi and CRXi pins are not required to be connected to the CAN bus or any external device.

Figure 37.8 shows the connection when self-test mode 1 is selected.

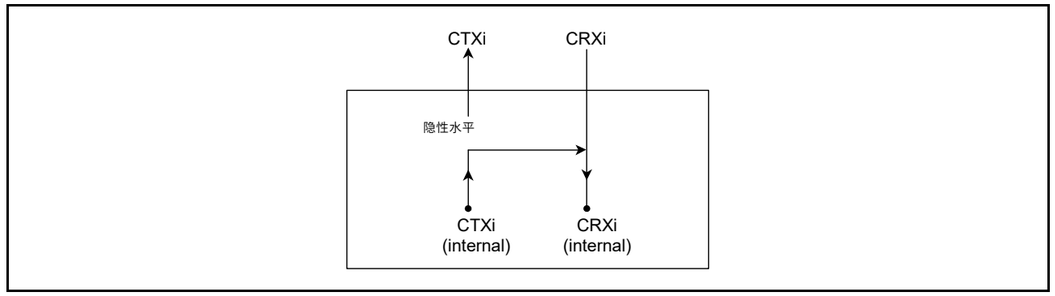


Figure 37.6 选择只听模式时的连接(i=0 1）

(2) Self-test mode 0 (external loopback)

自测模式0用于CAN收发器测试。在该模式下，协议模块将自己发送的报文视为CAN收发器接收到的报文，并将其存储到接收邮箱中。为独立于外部刺激，协议模块生成ACK位。

将CTXi和CRXi引脚连接到收发器。

图37.7显示了选择自检模式0时的连接。

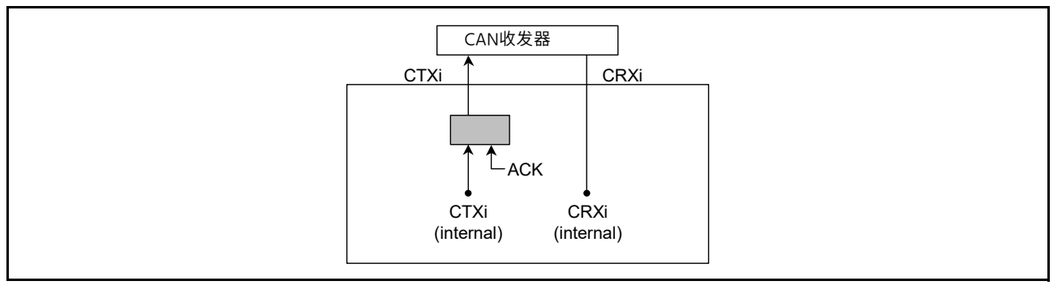


Figure 37.7 选择自检模式0时的连接(i=0 1）

(3) Self-test mode 1 (internal loopback)

自检模式1用于自检功能。

在自检模式1中，协议控制器将其发送的消息视为收到的消息，并将它们存储到接收邮箱中。为了独立于外部刺激，协议控制器生成ACK位。

在自检模式1中，协议控制器执行从内部CTXi引脚到内部CRXi引脚的内部反馈。外部CRXi引脚的输入值被忽略。外部CTXI引脚仅输出隐性位。CTXi和CRXi引脚不需要连接到CAN总线或任何外部设备。

图37.8显示了选择自检模式1时的连接。

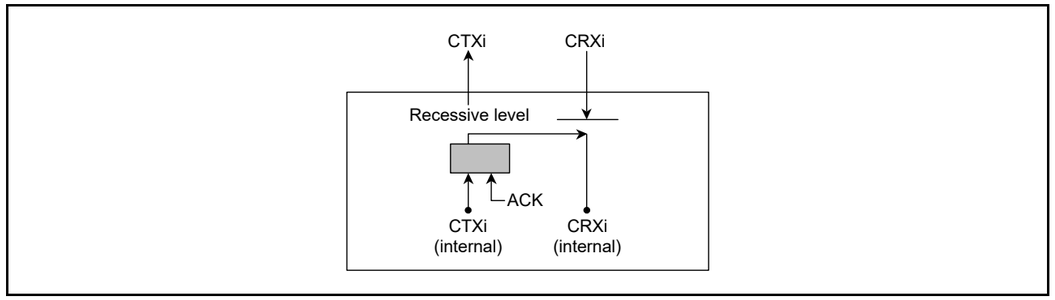


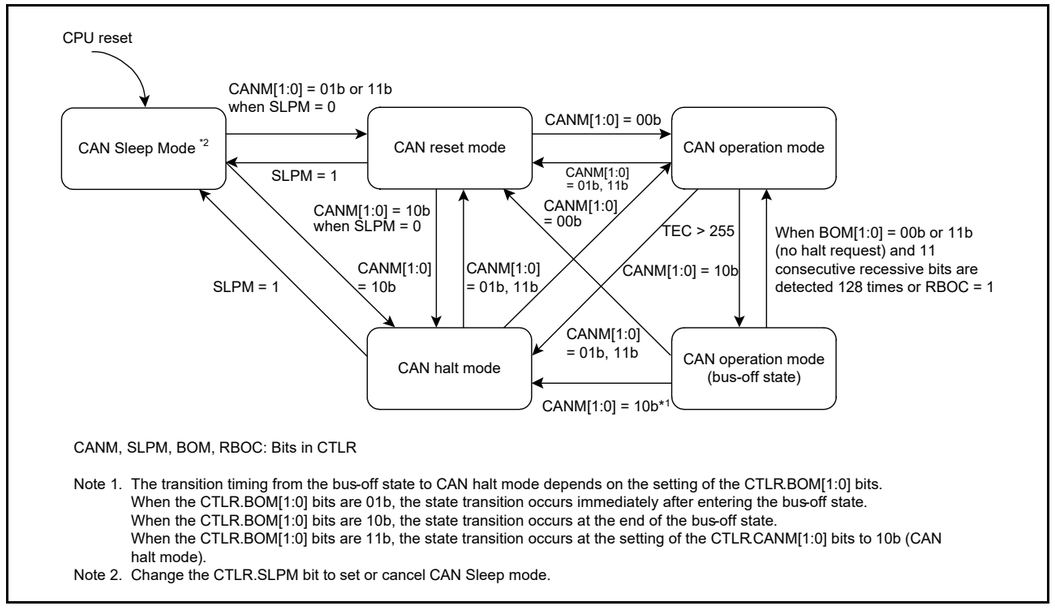
Figure 37.8 Connection when self-test mode 1 is selected (i = 0, 1)

37.3 Operation Modes

The CAN module operation modes include:

- CAN reset mode
- CAN halt mode
- CAN operation mode
- CAN sleep mode.

Figure 37.9 shows the transitions between the operation modes.



Note 1. The transition timing from the bus-off state to CAN halt mode depends on the setting of the CTLR.BOM[1:0] bits.
When the CTLR.BOM[1:0] bits are 01b, the state transition occurs immediately after entering the bus-off state.
When the CTLR.BOM[1:0] bits are 10b, the state transition occurs at the end of the bus-off state.
When the CTLR.BOM[1:0] bits are 11b, the state transition occurs at the setting of the CTLR.CANM[1:0] bits to 10b (CAN halt mode).
Note 2. Change the CTLR.SLPM bit to set or cancel CAN Sleep mode.

Figure 37.9 Transition between different operation modes

37.3.1 CAN Reset Mode

CAN reset mode is provided for CAN communication configuration. When the CTLR.CANM[1:0] bits are set to 01b or 11b, the CAN module enters CAN reset mode. The STR.RSTST bit then is set to 1. Do not change the CTLR.CANM[1:0] bits until the RSTST bit is 1. Set BCR before exiting CAN reset mode to any other modes.

The following registers are initialized to their reset values after entering CAN reset mode, and their initial values are

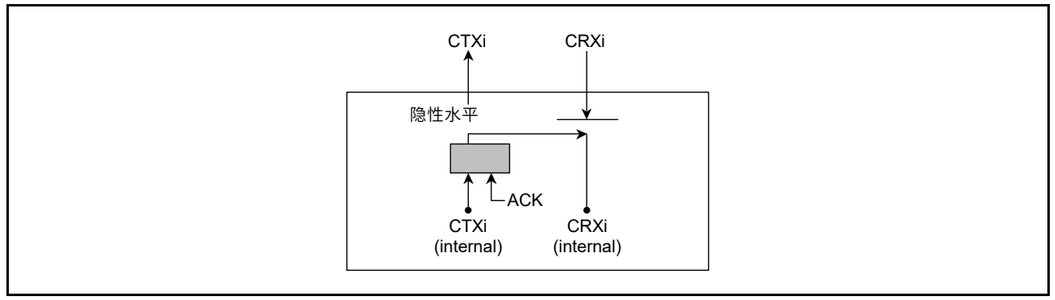


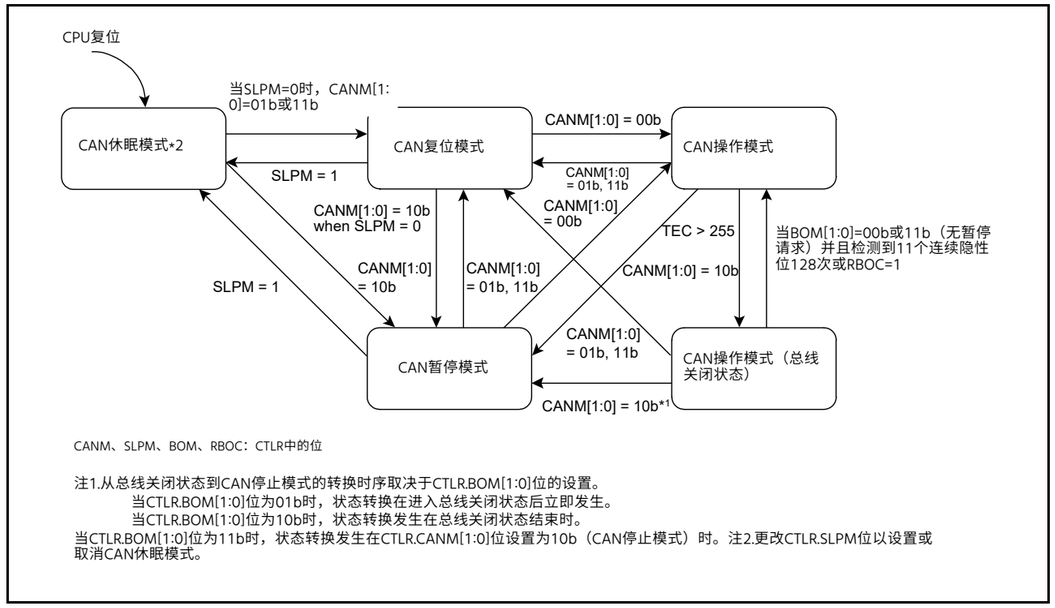
Figure 37.8 选择自检模式1时的连接(i=0 1）

37.3 操作模式

CAN模块操作模式包括：

- CAN复位模式
- CAN暂停模式
- CAN操作模式
- CAN睡眠模式。

图37.9显示了操作模式之间的转换。



注1.从总线关闭状态到CAN停止模式的转换时序取决于CTLR.BOM[1:0]位的设置。
当CTLR.BOM[1:0]位为01b时，状态转换在进入总线关闭状态后立即发生。
当CTLR.BOM[1:0]位为10b时，状态转换发生在总线关闭状态结束时。
当CTLR.BOM[1:0]位为11b时，状态转换发生在CTLR.CANM[1:0]位设置为10b（CAN停止模式）时。注2.更改CTLR.SLPM位以设置或取消CAN休眠模式。

Figure 37.9 不同操作模式之间的转换

37.3.1 CAN复位模式

CAN复位模式用于CAN通信配置。当CTLR.CANM[1:0]位设置为01b或11b时，CAN模块进入CAN复位模式。然后将STR.RSTST位设置为1。在RSTST位为1之前不要更改CTLR.CANM[1:0]位。在退出CAN复位模式到任何其他模式之前设置BCR。

以下寄存器在进入CAN复位模式后初始化为其复位值，其初始值为

saved during CAN reset mode:

- MCTL_TXj and MCTL_RXj
- STR (except for the SLPST and TFST bits)
- EIFR
- RECR
- TECR
- TSR
- MSSR
- MSMR
- RFCR
- TFCR
- TCR
- ECSR (except for the EDPM bit).

The following registers retain their previous values even after entering CAN reset mode:

- CTLR
- STR (only the SLPST and TFST bits)
- MIER and MIER_FIFO
- EIER
- BCR
- CSSR
- ECSR (only the EDPM bit)
- MBj_ID, MBj_DL, MBj_Dm and MBj_TS
- MKRk
- FIDCR0 and FIDCR1
- MKIVLR
- AFSR
- RFPCR
- TFPCR.

37.3.2 CAN Halt Mode

CAN halt mode is used for mailbox configuration and test mode setting.

When the CTLR.CANM[1:0] bits are set to 10b, CAN halt mode is selected. Then the STR.HLTST bit is set to 1. Do not change the CTLR.CANM[1:0] bits until the HLTST bit is 1.

See Table 37.8 for the state transition conditions when transmitting or receiving.

All registers except for the RSTST, HLTST, and SLPST bits in STR remain unchanged when the CAN enters CAN halt mode.

Do not change CTLR (except for the CANM[1:0] and SLPM bits) and EIER in CAN halt mode. BCR can be changed in CAN halt mode only when listen-only mode is selected for automatic baud rate detection.

在CAN复位模式下保存：

- MCTL_TXj and MCTL_RXj
- STR（SLPST和TFST位除外）
- EIFR
- RECR
- TECR
- TSR
- MSSR
- MSMR
- RFCR
- TFCR
- TCR
- ECSR（EDPM位除外）。

即使在进入CAN复位模式后，以下寄存器仍保留其先前的值：

- CTLR
- STR（仅SLPST和TFST位）
- MIER and MIER_FIFO
- EIER
- BCR
- CSSR
- ECSR (only the EDPM bit)
- MBj_ID, MBj_DL, MBj_Dm and MBj_TS
- MKRk
- FIDCR0 and FIDCR1
- MKIVLR
- AFSR
- RFPCR
- TFPCR.

37.3.2 CAN暂停模式

CAN暂停模式用于邮箱配置和测试模式设置。

当CTLR.CANM[1:0]位设置为10b时，选择CAN暂停模式。然后将STR.HLTST位设置为1。在HLTST位为1之前不要更改CTLR.CANM[1:0]位。

发送或接收时的状态转换条件见表37.8。

当CAN进入CAN暂停模式时，除STR中的RSTST、HLTST和SLPST位之外的所有寄存器都保持不变。

不要在CAN暂停模式下更改CTLR（CANM[1:0]和SLPM位除外）和EIER。BCR可以在仅当为自动波特率检测选择只听模式时，才可以暂停模式。

Table 37.8 Operation in CAN reset and halt modes

Operation mode	Receiver	Transmitter	Bus-off
CAN reset mode (forced transition) CANM[1:0] = 11b	CAN module enters CAN reset mode without waiting for the end of message reception.	CAN module enters CAN reset mode without waiting for the end of message transmission.	CAN module enters CAN reset mode without waiting for the end of bus-off recovery.
CAN reset mode CANM[1:0] = 01b	CAN module enters CAN reset mode without waiting for the end of message reception.	CAN module enters CAN reset mode after waiting for the end of message transmission.*1,*4	CAN module enters CAN reset mode without waiting for the end of bus-off recovery.
CAN halt mode	CAN module enters CAN halt mode after waiting for the end of message reception.*2,*3	CAN module enters CAN halt mode after waiting for the end of message transmission.*1,*4	When the BOM[1:0] bits are 00b: A halt request from software is accepted only after bus-off recovery. When the BOM[1:0] bits are 01b: CAN module automatically enters CAN halt mode without waiting for the end of bus-off recovery, regardless of a halt request from the software. When the BOM[1:0] bits are 10b: CAN module automatically enters CAN halt mode after waiting for the end of bus-off recovery, regardless of a halt request from software. When the BOM[1:0] bits are 11b: CAN module enters CAN halt mode without waiting for the end of bus-off recovery, if a halt is requested by software during bus-off.

BOM[1:0] bits: Bits in CTLR

Note 1. If transmission of multiple messages is requested, a mode transition occurs on completion of the first transmission. If the CAN reset mode is being requested during suspend transmission, mode transition occurs when the bus is idle, the next transmission ends, or the CAN module becomes a receiver.
Note 2. If the CAN bus is locked at the dominant level, the program can detect this state by monitoring the BLIF bit in EIFR.
Note 3. If a CAN bus error occurs during reception after CAN halt mode is requested, the CAN module transitions to CAN halt mode.
Note 4. If a CAN bus error or arbitration-lost occurs during transmission after CAN reset mode or CAN halt mode is requested, the CAN module transits to the requested CAN mode.

37.3.3 CAN Sleep Mode

CAN sleep mode reduces power consumption by stopping the clock supply to the CAN module. After a reset from an MCU pin or a software reset, the CAN module starts from CAN sleep mode.

When the SLPM bit in CTLR is set to 1, the CAN module enters CAN sleep mode. Then the SLPST bit in STR is set to 1. Do not change the value of the SLPM bit until the SLPST bit is 1. The other registers remain unchanged when the CAN module enters CAN sleep mode.

Write to the SLPM bit in CAN reset mode and CAN halt mode. Do not change any registers (except for the SLPM bit) during CAN sleep mode. Read operation is still allowed.

When the SLPM bit is set to 0, the CAN module is released from CAN sleep mode. When the CAN module exits CAN sleep mode, the other registers remain unchanged.

37.3.4 CAN Operation Mode (Excluding Bus-Off State)

CAN operation mode is used for CAN communication.

When the CANM[1:0] bits in CTLR are set to 00b, the CAN module enters CAN operation mode. Then the RSTST and HLTST bits in STR set to 0. Do not change the value of the CANM[1:0] bits until the RSTST and HLTST bits are 0.

If 11 consecutive recessive bits are detected after entering CAN operation mode, the following occurs:

- The CAN module becomes an active node on the network, which enables transmission and reception of CAN

Table 37.8 CAN复位和暂停模式下的操作

操作模式	Receiver	Transmitter	Bus-off
CAN复位模式（强制转换）CANM[1:0]=11b	CAN模块无需等待报文接收结束即可进入CAN复位模式。	CAN模块无需等待报文传输结束就进入CAN复位模式。	CAN模块无需等待总线关闭恢复结束即可进入CAN复位模式。
CAN复位模式CANM[1:0]=01b	CAN模块无需等待报文接收结束即可进入CAN复位模式。	CAN模块等待报文传输结束后进入CAN复位模式。*1 *4	CAN模块无需等待总线关闭恢复结束即可进入CAN复位模式。
CAN暂停模式	CAN模块等待报文接收结束后进入CAN暂停模式。*2 *3	CAN模块等待报文传输结束后进入CAN停止模式。*1 *4	当BOM[1:0]位为00b时： 仅在总线关闭恢复后才接受来自软件的暂停请求。 当BOM[1:0]位为01b时： CAN模块自动进入CAN停止模式，无需等待总线关闭恢复结束，无论来自软件的停止请求如何。 当BOM[1:0]位为10b时： CAN模块在等待总线关闭恢复结束后自动进入CAN停止模式，无论软件是否有停止请求。 当BOM[1:0]位为11b时： 如果在总线关闭期间软件请求停止，CAN模块无需等待总线关闭恢复结束即可进入CAN停止模式。

BOM[1:0] bits: CTLR中的位

Note 1. 如果请求传输多个消息，则在第一次传输完成时发生模式转换。如果在暂停传输期间请求CAN复位模式，则在总线空闲、下一次传输结束或CAN模块成为接收器时发生模式转换。
Note 2. 如果CAN总线被锁定在显性电平，程序可以通过监控EIFR中的BLIF位来检测该状态。
Note 3. 如果在请求CAN暂停模式后接收期间发生CAN总线错误，则CAN模块将转换到CAN暂停模式。
Note 4. 如果在请求CAN复位模式或CAN暂停模式后的传输过程中发生CAN总线错误或仲裁丢失，则CAN模块将转换到请求的CAN模式。

37.3.3 CAN睡眠模式

CAN睡眠模式通过停止向CAN模块提供时钟来降低功耗。从一个复位后MCU引脚或软件复位，CAN模块从CAN睡眠模式启动。

当CTLR中的SLPM位设置为1时，CAN模块进入CAN休眠模式。然后将STR中的SLPST位设置为1。在SLPST位为1之前不要更改SLPM位的值。当CAN模块进入CAN休眠模式时，其他寄存器保持不变。

在CAN复位模式和CAN暂停模式下写入SLPM位。在CAN睡眠模式期间不要更改任何寄存器（SLPM位除外）。仍然允许读取操作。

当SLPM位设置为0时，CAN模块从CAN睡眠模式中释放。当CAN模块退出CAN休眠模式时，其他寄存器保持不变。

37.3.4 CAN操作模式（不包括总线关闭状态）

CAN操作模式用于CAN通信。

当CTLR中的CANM[1:0]位设置为00b时，CAN模块进入CAN操作模式。然后RSTST和STR中的HLTST位设置为0。在RSTST和HLTST位为0之前，不要更改CANM[1:0]位的值。

如果在进入CAN操作模式后检测到11个连续的隐性位，则会发生以下情况：

- CAN模块成为网络上的一个有源节点，使CAN的传输和接收成为可能

messages

- Error monitoring of the CAN bus, such as receive and transmit error counters, is performed.

During CAN operation mode, the CAN module might be in one of the following three sub-modes, depending on the status of the CAN bus.

- Idle mode: No transmission or reception occurs
- Receive mode: A CAN message sent by another node is being received
- Transmit mode: A CAN message is being transmitted. The CAN module receives a message transmitted by the local node simultaneously when self-test mode 0 (TSTM[1:0] bits in TCR = 10b) or self-test mode 1 (TSTM[1:0] bits = 11b) is selected.

Figure 37.10 demonstrates the sub-modes in CAN operation mode.

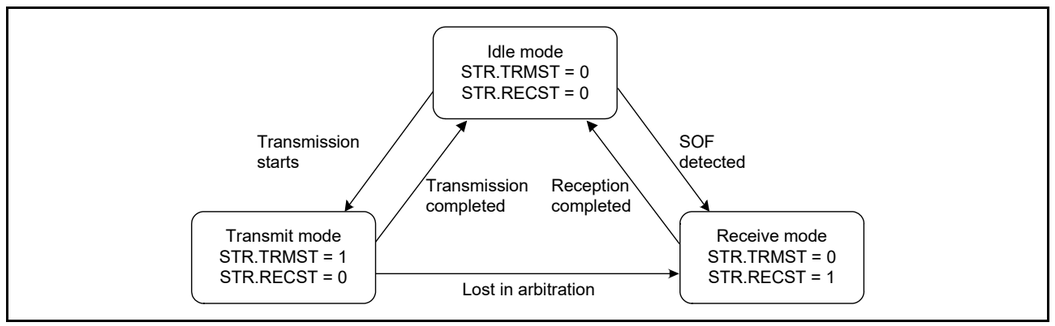


Figure 37.10 Sub-modes of CAN operation mode

37.3.5 CAN Operation Mode (Bus-Off State)

The CAN module enters the bus-off state based on the incrementing decrementing rules for the transmit and error counters defined in the CAN Specifications. The following cases apply when the CAN module is recovering from the bus-off state. When the CAN module is in the bus-off state, the values of the CAN-related registers remain unchanged, except for those in STR, EIFR, RECR, TECR, and TSR.

(1) When CTLR.BOM[1:0] = 00b (normal mode)

The CAN module enters the error-active state after it completes recovery from the bus-off state and CAN communication is enabled. The BORIF flag in EIFR is set to 1 (bus-off recovery detected) at this time.

(2) When CTLR.RBOC = 1 (forced return from bus-off)

The CAN module enters the error-active state when it is in the bus-off state and the RBOC bit is 1. CAN communication is enabled again after 11b consecutive recessive bits are detected. The BORIF bit does not set to 1 at this time.

(3) When CTLR.BOM[1:0] = 01b (automatic transition to CAN halt mode on bus-off)

The CAN module enters CAN halt mode when it reaches the bus-off state. The BORIF flag does not set to 1 at this time.

(4) When CTLR.BOM[1:0] = 10b (automatic transition to CAN halt mode on bus-off end)

The CAN module enters CAN halt mode when it completes recovery from bus-off. The BORIF flag is set to 1 at this time.

(5) When CTLR.BOM[1:0] = 11b (automatic transition to CAN halt mode through software) and CTLR.CANM[1:0] = 10b (CAN halt mode) during bus-off state

The CAN module enters CAN halt mode when it is in the bus-off state and the CANM[1:0] bits are set to 10b (CAN halt mode). The BORIF flag does not set to 1 at this time.

If the CANM[1:0] bits are not set to 10b during bus-off, the same behavior as (1) applies.

messages

- 执行CAN总线的错误监控，例如接收和发送错误计数器。

在CAN操作模式下，CAN模块可能处于以下三种子模式之一，具体取决于CAN总线的状态。

- 空闲模式：没有发送或接收发生
- 接收模式：正在接收另一个节点发送的CAN报文
- 传输模式：正在传输CAN消息。选择自测模式0（TCR中的TSTM[1:0]位=10b）或自测模式1（TSTM[1:0]位=11b）时，CAN模块同时接收本地节点发送的消息.

图37.10展示了CAN操作模式下的子模式。

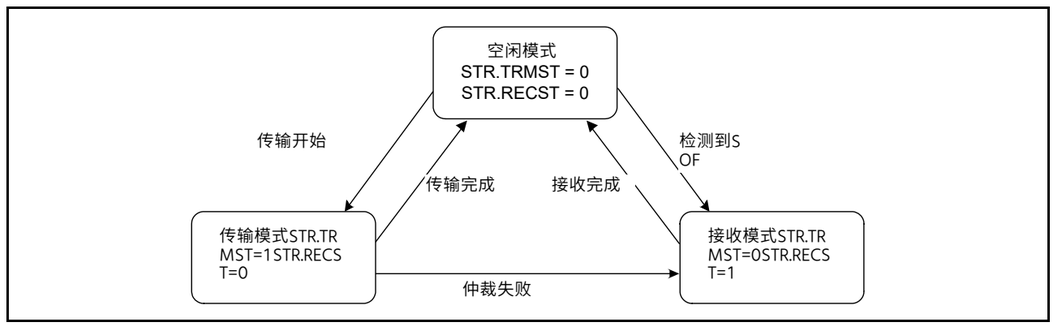


Figure 37.10 CAN操作模式的子模式

37.3.5 CAN操作模式（总线关闭状态）

CAN模块根据CAN规范中定义的发送和错误计数器的递增递减规则进入总线关闭状态。以下情况适用于CAN模块从总线关闭状态恢复时。当CAN模块处于总线关闭状态时，CAN相关寄存器的值保持不变，除了STR、EIFR、RECR、TECR和TSR中的值。

(1) When CTLR.BOM[1:0] = 00b (normal mode)

CAN模块在完成从总线关闭状态恢复并启用CAN通信后进入错误激活状态。此时EIFR中的BORIF标志设置为1（检测到总线关闭恢复）。

(2) 当CTLR.RBOC=1时（从总线关闭强制返回）

当CAN模块处于总线关闭状态且RBOC位为1时，进入错误激活状态。在检测到11b个连续的隐性位后再次启用CAN通信。此时BORIF位不设置为1。

(3) 当CTLR.BOM[1:0]=01b时（总线关闭时自动转换到CAN暂停模式）

CAN模块在达到总线关闭状态时进入CAN停止模式。BORIF标志此时不设置为1。

(4) 当CTLR.BOM[1:0]=10b时（在总线关闭结束时自动转换到CAN暂停模式）

CAN模块在完成总线关闭恢复后进入CAN暂停模式。此时BORIF标志设置为1。

(5) 当CTLR.BOM[1:0]=11b（通过软件自动转换到CAN暂停模式）并且总线关闭状态期间CTLR.CANM[1:0]=10b（CAN停止模式）

CAN模块在总线关闭状态且CANM[1:0]位设置为10b（CAN停止模式）时进入CAN停止模式。BORIF标志此时不设置为1。

如果在总线关闭期间CANM[1:0]位未设置为10b，则适用与(1)相同的行为。

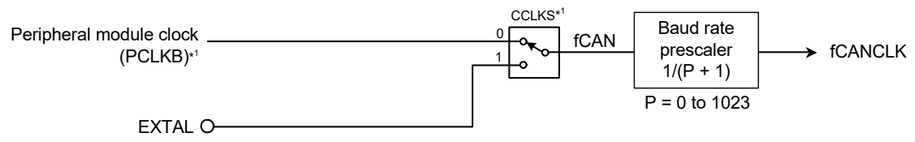
37.4 Data Transfer Rate Configuration

This section describes how to configure the data transfer rate.

37.4.1 Clock Setting

The CAN module has a CAN clock generator that can be set by the CCLKS and the BRP[9:0] bits in the BCR register.

Figure 37.11 shows a block diagram of the CAN clock generator.



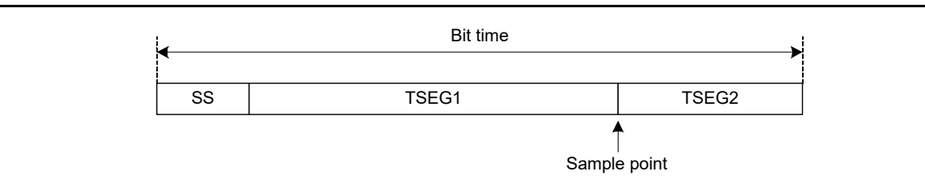
CCLKS: Bit in the BCR register
fCAN: CAN system clock
P: Value selected in BRP[9:0] bits in BCR (P = 0 to 1023)
fCANCLK: CAN communication clock (fCANCLK = fCAN/(P + 1))

Note 1. See section 9, Clock Generation Circuit. When using the CAN module while the CCLKS bit is cleared to 0, PLL must be selected as the source of the peripheral module clock.

Figure 37.11 Block diagram of CAN clock generator

37.4.2 Bit Timing Setting

The bit time consists of the following three segments shown in Figure 37.12.



The range of each segment: Bit time = 8 Tq to 25 Tq
SS = 1 Tq
TSEG1 = 4 Tq to 16 Tq
TSEG2 = 2 Tq to 8 Tq
SJW = 1 Tq to 4 Tq
Setting of TSEG1 and TSEG2: TSEG1 > TSEG2 ≥ SJW

Figure 37.12 Bit timing

37.4.3 Data Transfer Rate

The data transfer rate depends on the division value of fCAN (CAN system clock), the division value of the baud rate prescaler, and the Tq count for 1 bit time.

$$\text{Data transfer rate (bps)} = \frac{\text{fCAN}}{\text{Baud rate prescaler division value*1 x number of Tq of 1 bit time}} = \frac{\text{fCANCLK}}{\text{Tq count for 1 bit time}}$$

Note 1. Division value of baud rate prescaler = P + 1 (P: 0 to 1023), where P is the BRP[9:0] setting in BCR.

Table 37.9 lists data transfer rate examples.

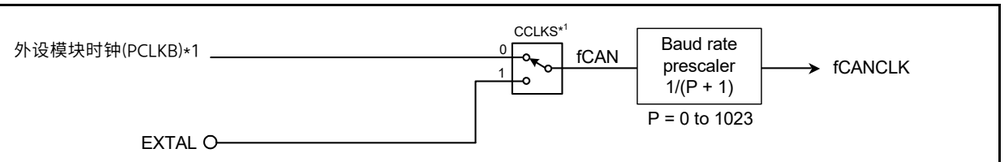
37.4 数据传输率配置

本节介绍如何配置数据传输速率。

37.4.1 时钟设置

CAN模块有一个CAN时钟发生器，可以通过BCR寄存器中的CCLKS和BRP[9:0]位进行设置。

图37.11显示了CAN时钟发生器的框图。



CCLKS: BCR寄存器中的位
fCAN: CAN系统时钟
P：在BCR中的BRP[9:0]位中选择的值（P=0到1023）fCANCLK：
CAN通信时钟（fCANCLK=fCAN(P+1)）

注1.见第9节，时钟生成电路。在CCLKS位清0时使用CAN模块时，必须选择PLL作为外设模块时钟源。

Figure 37.11 CAN时钟发生器框图

37.4.2 位时序设置

位时间由图37.12所示的以下三个部分组成。

每个段的范围： 位时间=8Tq到25TqSS=
1Tq
TSEG1 = 4 Tq to 16 Tq
TSEG2 = 2 Tq to 8 Tq
SJW = 1 Tq to 4 Tq
TSEG1和TSEG2的设置：TSEG1>TSEG2 SJW

Figure 37.12 位时序

37.4.3 数据传输率

数据传输速率取决于fCAN（CAN系统时钟）的分频值、波特率预分频器的分频值和1位时间的Tq计数。

$$\text{数据传输率(bps)} = \frac{\text{fCAN}}{\text{波特率预分频器分频值*1x1位时间的Tq数}} = \frac{\text{fCANCLK}}{\text{1位时间的Tq计数}}$$

注1.波特率预分频器的分频值=P+1(P:0to1023)，其中P是BCR中的BRP[9:0]设置。

表37.9列出了数据传输率示例。

Table 37.9 Data transfer rate examples

fCAN	50 MHz		48 MHz		40 MHz		32 MHz	
Data transfer rate	Tq count	P + 1	Tq count	P + 1	Tq count	P + 1	Tq count	P + 1
1 Mbps	10 Tq 25 Tq	5 2	8 Tq 12 Tq 16 Tq	6 4 3	10 Tq 20 Tq	4 2	8 Tq 16 Tq	4 2
500 kbps	10 Tq 25 Tq	10 4	8 Tq 12 Tq 16 Tq	12 8 6	10 Tq 20 Tq	8 4	8 Tq 16 Tq	8 4
250 kbps	10 Tq 25 Tq	20 8	8 Tq 12 Tq 16 Tq	24 16 12	10 Tq 20 Tq	16 8	8 Tq 16 Tq	16 8
125 kbps	10 Tq 25 Tq	40 16	8 Tq 12 Tq 16 Tq	48 32 24	10 Tq 20 Tq	32 16	8 Tq 16 Tq	32 16
83.3 kbps	10 Tq 25 Tq	60 24	8 Tq 12 Tq 16 Tq	72 48 36	8 Tq 10 Tq 16 Tq 20 Tq	60 48 30 24	8 Tq 16 Tq	48 24
33.3 kbps	10 Tq 25 Tq	150 60	8 Tq 12 Tq 16 Tq	180 120 90	8 Tq 10 Tq 20 Tq	150 120 60	8 Tq 10 Tq 16 Tq 20 Tq	120 96 60 48

37.5 Mailbox and Mask Register Structure

Figure 37.13 shows the structure of the 32 mailbox registers: MBj_ID, MBj_DL, MBj_Dm, and MBj_TS.

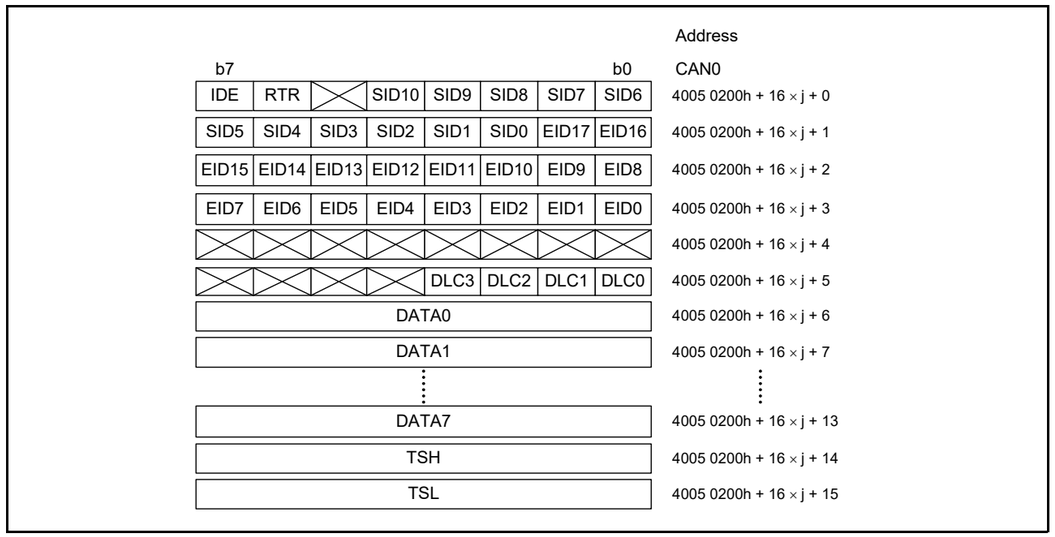


Figure 37.13 Structure of the mailbox registers (j = 0 to 31)

Figure 37.14 shows the structure of the eight mask registers: MKRk.

Table 37.9 数据传输率示例

fCAN	50 MHz		48 MHz		40 MHz		32 MHz	
数据传输率	Tq count	P + 1	Tq count	P + 1	Tq count	P + 1	Tq count	P + 1
1 Mbps	10 Tq 25 Tq	5 2	8 Tq 12 Tq 16 Tq	6 4 3	10 Tq 20 Tq	4 2	8 Tq 16 Tq	4 2
500 kbps	10 Tq 25 Tq	10 4	8 Tq 12 Tq 16 Tq	12 8 6	10 Tq 20 Tq	8 4	8 Tq 16 Tq	8 4
250 kbps	10 Tq 25 Tq	20 8	8 Tq 12 Tq 16 Tq	24 16 12	10 Tq 20 Tq	16 8	8 Tq 16 Tq	16 8
125 kbps	10 Tq 25 Tq	40 16	8 Tq 12 Tq 16 Tq	48 32 24	10 Tq 20 Tq	32 16	8 Tq 16 Tq	32 16
83.3 kbps	10 Tq 25 Tq	60 24	8 Tq 12 Tq 16 Tq	72 48 36	8 Tq 10 Tq 16 Tq 20 Tq	60 48 30 24	8 Tq 16 Tq	48 24
33.3 kbps	10 Tq 25 Tq	150 60	8 Tq 12 Tq 16 Tq	180 120 90	8 Tq 10 Tq 20 Tq	150 120 60	8 Tq 10 Tq 16 Tq 20 Tq	120 96 60 48

37.5 邮箱和掩码寄存器结构

图37.13显示了32个邮箱寄存器的结构：MBj_ID、MBj_DL、MBj_Dm和MBj_TS。

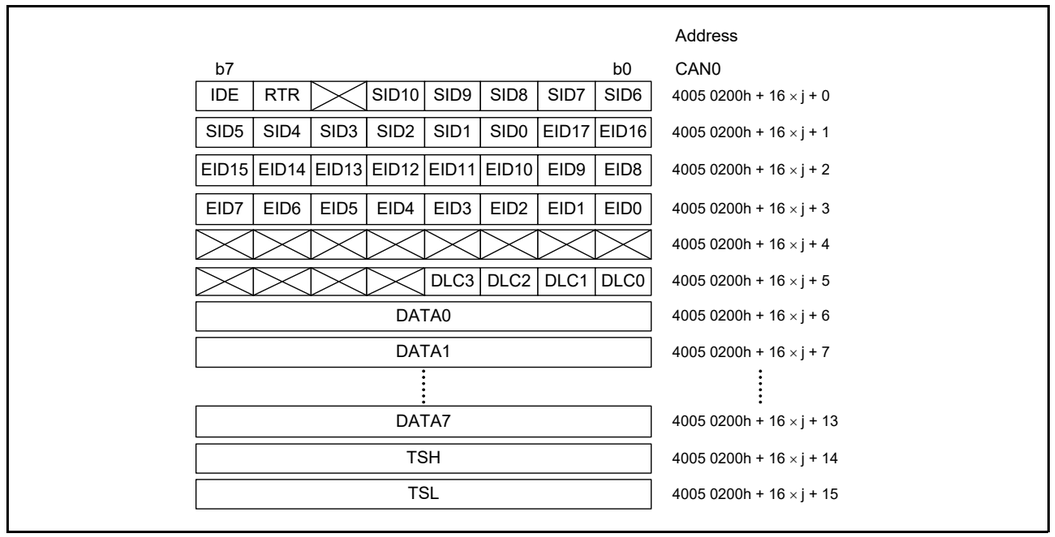


Figure 37.13 邮箱寄存器的结构（j=0到31）

图37.14显示了八个屏蔽寄存器的结构：MKRk。

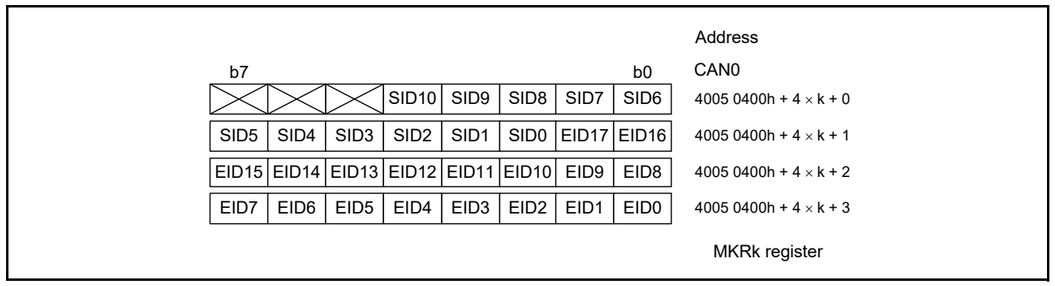


Figure 37.14 Structure of the MKRk registers (k = 0 to 7)

Figure 37.15 shows the structure of the two FIFO receive ID compare registers: FIDCR0 and FIDCR1.

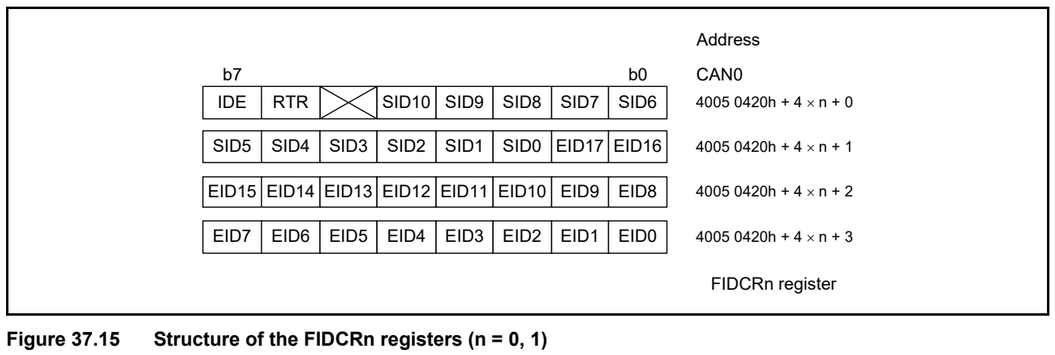


Figure 37.15 Structure of the FIDCRn registers (n = 0, 1)

37.6 Acceptance Filtering and Masking Functions

The acceptance filtering and masking functions allow you to select and receive messages with multiple IDs for mailboxes within a specified range.

The MKRk registers can mask the standard ID and the extended ID for 29 bits.

- MKR0 controls mailboxes 0 to 3
- MKR1 controls mailboxes 4 to 7
- MKR2 controls mailboxes 8 to 11
- MKR3 controls mailboxes 12 to 15
- MKR4 controls mailboxes 16 to 19
- MKR5 controls mailboxes 20 to 23
- MKR6 controls mailboxes 24 to 27 in normal mailbox mode and the receive FIFO mailboxes 28 to 31 in FIFO mailbox mode
- MKR7 controls mailboxes 28 to 31 in normal mailbox mode and the receive FIFO mailboxes 28 to 31 in FIFO mailbox mode.

MKIVLR disables acceptance filtering independently for each mailbox.

The IDE bit in MBj_ID is valid when the IDFM[1:0] bits in CTLR are 10b (mixed ID mode).

The RTR bit in MBj_ID selects a data or remote frame.

In FIFO mailbox mode, the normal mailboxes (0 to 23) use one associated register from MKR0 to MKR5 for acceptance filtering. The receive FIFO mailboxes (28 to 31) use two registers, MKR6 and MKR7, for acceptance filtering.

The receive FIFO also uses two registers, FIDCR0 and FIDCR1, for ID comparison. The EID[17:0], SID[10:0], RTR,

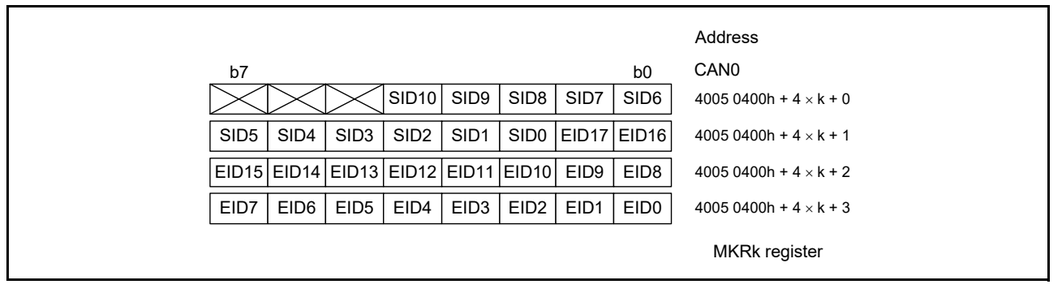


Figure 37.14 MKRk寄存器的结构（k=0到7）

图37.15显示了两个FIFO接收ID比较寄存器的结构：FIDCR0和FIDCR1。

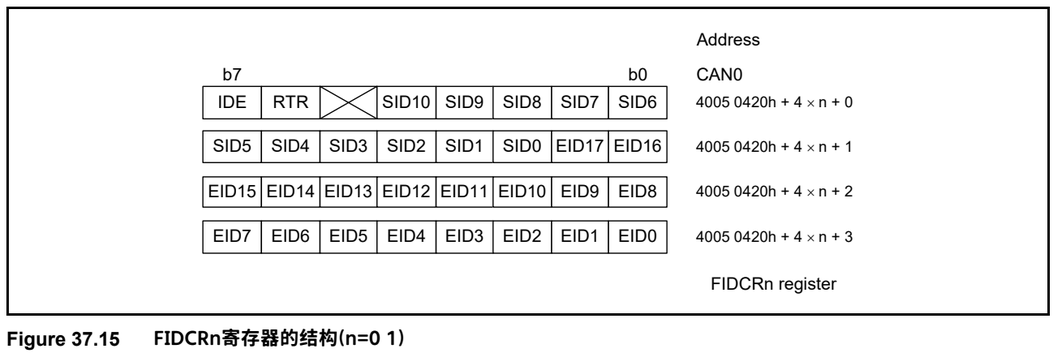


Figure 37.15 FIDCRn寄存器的结构(n=0 1)

37.6 接受过滤和屏蔽功能

接受过滤和屏蔽功能允许您为指定范围内的邮箱选择和接收具有多个ID的消息。

MKRk寄存器可以屏蔽29位的标准ID和扩展ID。

- MKR0控制邮箱0到3
- MKR1控制邮箱4到7
- MKR2控制邮箱8到11
- MKR3控制邮箱12到15
- MKR4控制邮箱16到19
- MKR5控制邮箱20到23
- MKR6在正常邮箱模式下控制邮箱24到27，在FIFO邮箱模式下控制接收FIFO邮箱28到31
- MKR7在正常邮箱模式下控制邮箱28到31，在FIFO邮箱模式下控制接收FIFO邮箱28到31。

MKIVLR为每个邮箱单独禁用接受过滤。

当CTLR中的IDFM[1:0]位为10b（混合ID模式）时，MBj_ID中的IDE位有效。

MBj_ID中的RTR位选择数据或远程帧。

在FIFO邮箱模式下，普通邮箱（0到23）使用一个从MKR0到MKR5的关联寄存器进行接受过滤。接收FIFO邮箱（28到31）使用两个寄存器MKR6和MKR7，用于接受过滤。

接收FIFO还使用两个寄存器FIDCR0和FIDCR1进行ID比较。EID[17:0]、SID[10:0]、RTR、

and IDE bits in mailbox28 to mailbox31 for the receive FIFO are disabled. As acceptance filtering depends on the result of two logic OR operations, two ranges of IDs can be received into the receive FIFO.

MKIVLR is disabled for the receive FIFO.

If different standard ID and extended ID values are set in the IDE bits in FIDCR0 and FIDCR1, both ID formats are received.

If different data frame and remote frame values are set in the RTR bits in FIDCR0 and FIDCR1, both data and remote frames are received.

When a combination of two ranges of IDs is not necessary, set the same mask value and the same ID into both the FIFO ID and mask registers.

Figure 37.16 shows the associations between the mask registers and mailboxes. Figure 37.17 shows the acceptance filtering.

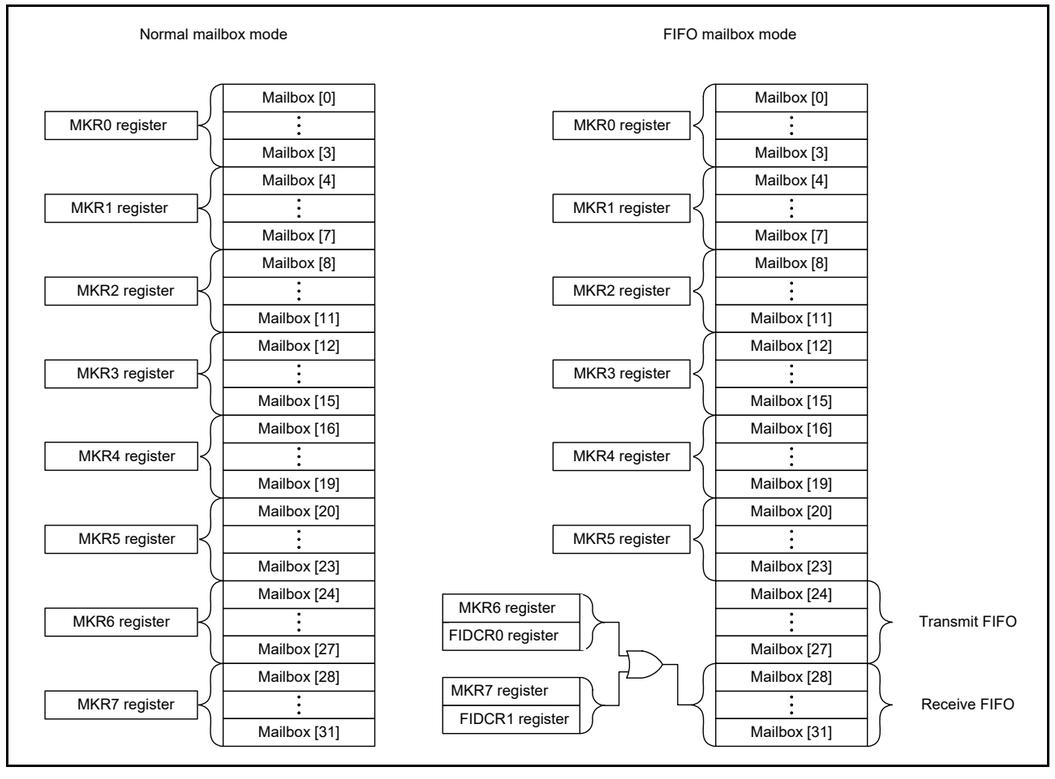


Figure 37.16 Associations between mask registers and mailboxes

接收FIFO的邮箱28到邮箱31中的IDE位被禁用。由于接受过滤取决于两个逻辑或运算的结果，因此可以将两个范围的ID接收到接收FIFO中。

MKIVLR对接收FIFO禁用。

如果在FIDCR0和FIDCR1的IDE位中设置了不同的标准ID和扩展ID值，则会接收两种ID格式。

如果在FIDCR0和FIDCR1的RTR位中设置了不同的数据帧和远程帧值，则数据帧和远程帧都被接收。

当不需要组合两个范围的ID时，将相同的掩码值和相同的ID设置到两个FIFO中
ID和掩码寄存器。

图37.16显示了掩码寄存器和邮箱之间的关联。图37.17显示了接受过滤。

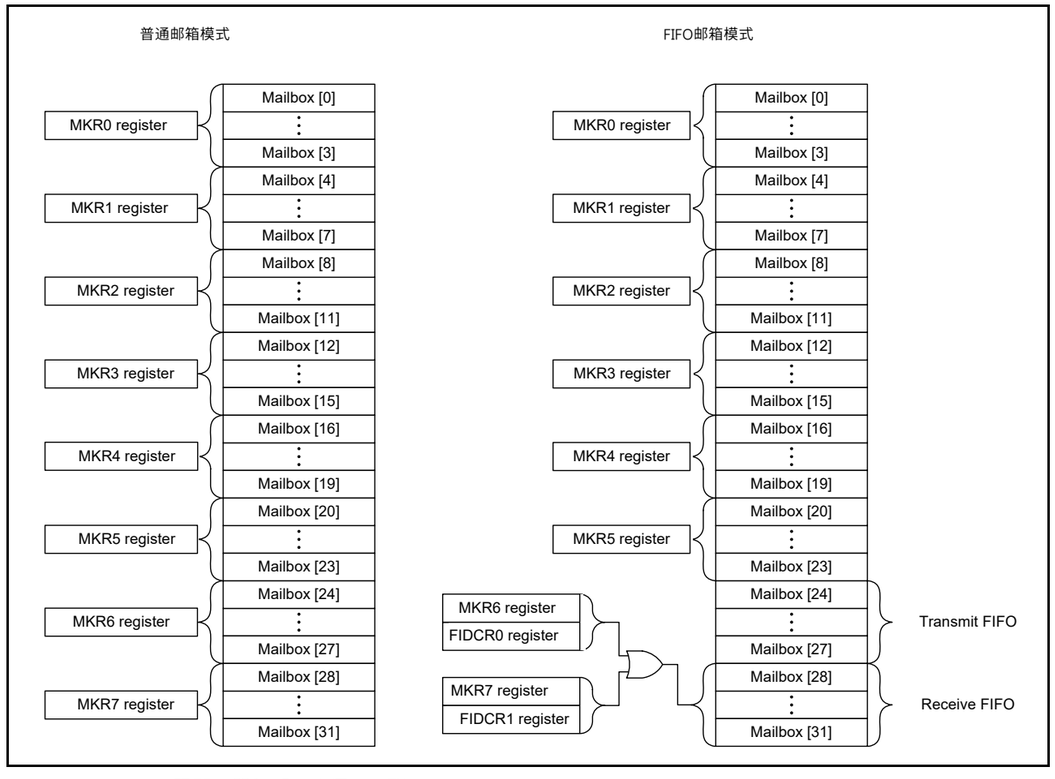


Figure 37.16 掩码寄存器和邮箱之间的关联

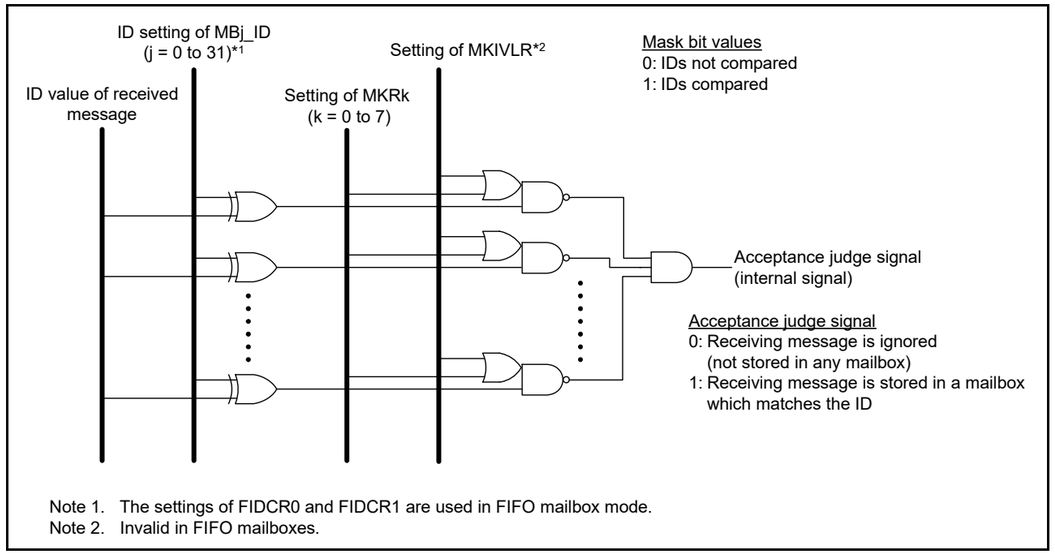


Figure 37.17 Acceptance filtering

37.7 Reception and Transmission

Table 37.10 lists the CAN communication mode settings.

Table 37.10 Settings for CAN receive and transmit modes

MCTL_TXj.TRMREQ and MCTL_RXj.TRMREQ	MCTL_TXj.RECREQ and MCTL_RXj.RECREQ	MCTL_TXj.ONESHOT and MCTL_RXj.ONESHOT	Mailbox communication mode
0	0	0	Mailbox disabled or transmission being aborted
0	0	1	Can be configured only when transmission or reception from a mailbox programmed in one-shot mode is aborted
0	1	0	Configured as a receive mailbox for a data or remote frame
0	1	1	Configured as a one-shot receive mailbox for a data or remote frame.
1	0	0	Configured as a transmit mailbox for a data or remote frame.
1	0	1	Configured as a one-shot transmit mailbox for a data or remote frame.
1	1	0	Do not set.
1	1	1	Do not set.

j = 0 to 31

When a mailbox is configured as a receive mailbox or a one-shot receive mailbox, the following restrictions apply:

- Before configuring the mailbox, set MCTL_RXj to 00h.
- A received message is stored in the first mailbox that matches the condition resulting from the receive mode settings and acceptance filtering. The matching mailbox with the smallest number takes priority for storing the received message.
- In CAN operation mode, the CAN module does not receive its own transmitted data even if the ID is a match. In self-test mode, however, the CAN module receives its own transmitted data and returns ACK.

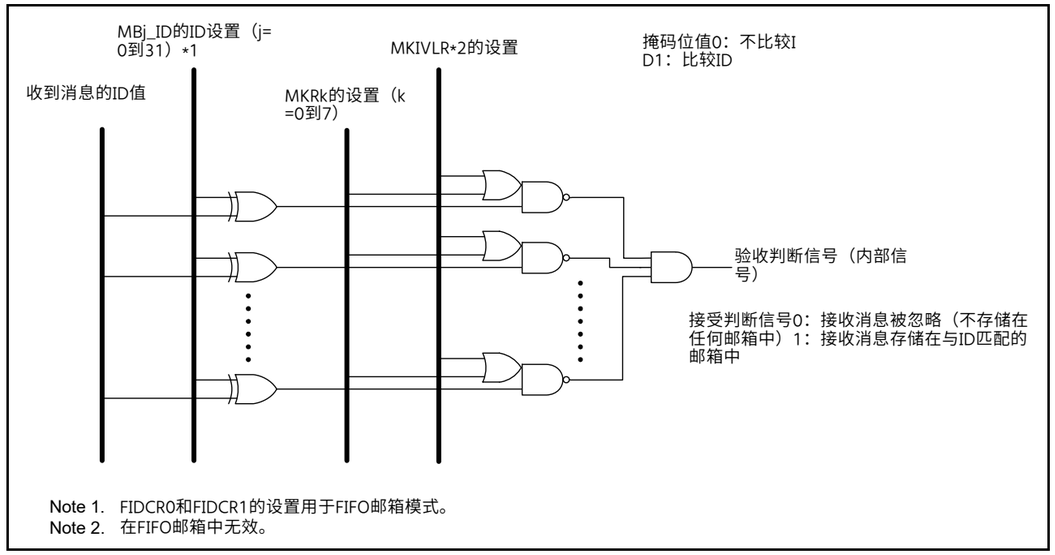


Figure 37.17 验收过滤

37.7 接收和传输

表37.10列出了CAN通信模式设置。

Table 37.10 CAN接收和发送模式的设置

MCTL_TXj.TRMREQ and MCTL_RXj.TRMREQ	MCTL_TXj.RECREQ and MCTL_RXj.RECREQ	MCTL_TXj.ONESHOT and MCTL_RXj.ONESHOT	邮箱通讯方式
0	0	0	邮箱禁用或传输被中止
0	0	1	只有在一次性模式中编程的邮箱的发送或接收被中止时才可以配置
0	1	0	配置为数据或远程帧的接收邮箱
0	1	1	配置为数据或远程帧的一次性接收邮箱。
1	0	0	配置为数据或远程帧的传输邮箱。
1	0	1	配置为数据或远程帧的一次性发送邮箱。
1	1	0	不要设置。
1	1	1	不要设置。

j = 0 to 31

当邮箱配置为接收邮箱或一次性接收邮箱时，以下限制适用：

- 在配置邮箱之前，将MCTL_RXj设置为00h。
- 收到的消息存储在与接收模式设置和接受过滤产生的条件匹配的第一个邮箱中。编号最小的匹配邮箱优先存储收到的消息。
- 在CAN操作模式下，即使ID匹配，CAN模块也不会接收到自己发送的数据。然而，在自检模式下，CAN模块接收自己发送的数据并返回ACK。

When configuring a mailbox as a transmit mailbox or a one-shot transmit mailbox, the following constraint applies:

- Before configuring a mailbox, ensure that MCTL_TXj is 00h and that there is no pending abort process.

37.7.1 Reception

Figure 37.18 shows an operation example of data frame reception in overwrite mode. The example shows the overwriting of the first message when the CAN module receives two consecutive CAN messages that match the receiving conditions in MCTL_RXj (j = 0 to 31).

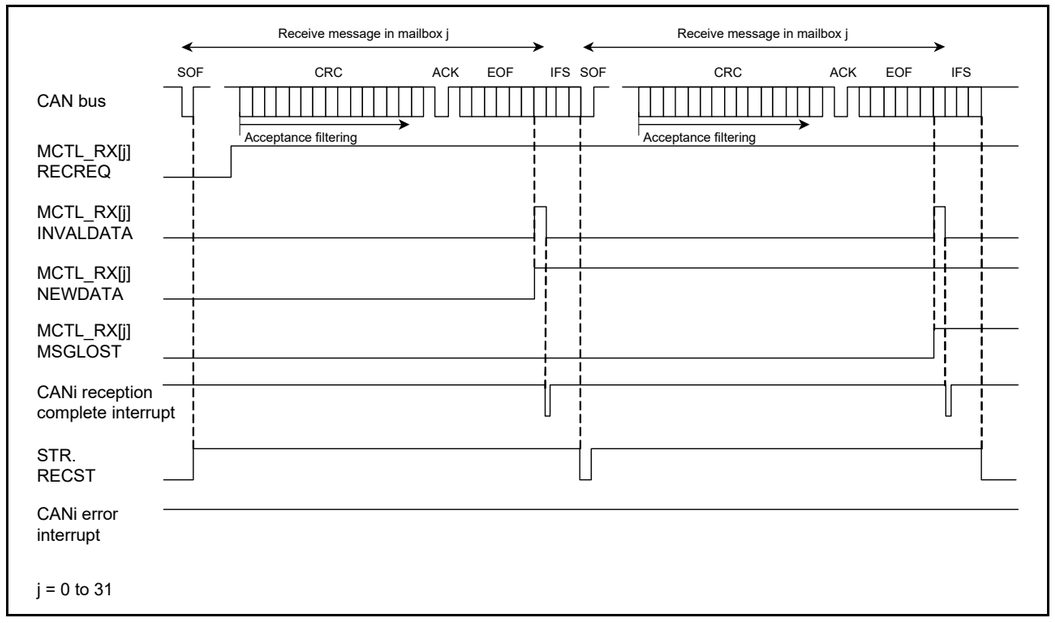


Figure 37.18 Operation example of data frame reception in overwrite mode

1. When an SOF is detected on the CAN bus, the RECST bit in STR is set to 1 (reception in progress) if the CAN module has no message ready to start transmission.
2. Acceptance filtering starts at the beginning of the CRC field to select the receive mailbox.
3. After a message is received, the NEWDATA flag in MCTL_RXj for the receive mailbox is set to 1 (new message is being stored or was stored in the mailbox). The INVALDATA flag in MCTL_RXj is set to 1 (message is being updated) at the same time, and then the INVALDATA flag is set to 0 (message valid) again after the complete message is transferred to the mailbox.
4. When the interrupt enable bit in MIER for the receive mailbox is 1 (interrupt enabled), the INVALDATA flag is set to 0, which triggers a CAN0 reception complete interrupt request.
5. After reading the message from the mailbox, the NEWDATA flag must be set to 0 by software.
6. In overwrite mode, if the next CAN message is received while the NEWDATA flag in MCTL_RXj is set to 1, the MSGLOST flag in MCTL_RXj is set to 1 (message was overwritten). The new received message is transferred to the mailbox. The CAN0 reception complete interrupt request occurs the same as in step 4.

Figure 37.19 shows an operation example of data frame reception in overrun mode. The example shows the overrunning of the second message when the CAN module receives two consecutive CAN messages that match the receiving conditions in MCTL_RXj (j = 0 to 31).

将邮箱配置为传输邮箱或一次性传输邮箱时，适用以下约束：

- 在配置邮箱之前，请确保MCTL_TXj为00h并且没有挂起的中止进程。

37.7.1 Reception

图37.18显示了覆盖模式下数据帧接收的操作示例。该示例显示当CAN模块接收到与MCTL_RXj（j=0到31）中的接收条件匹配的两个连续CAN报文时，第一条报文的覆盖。

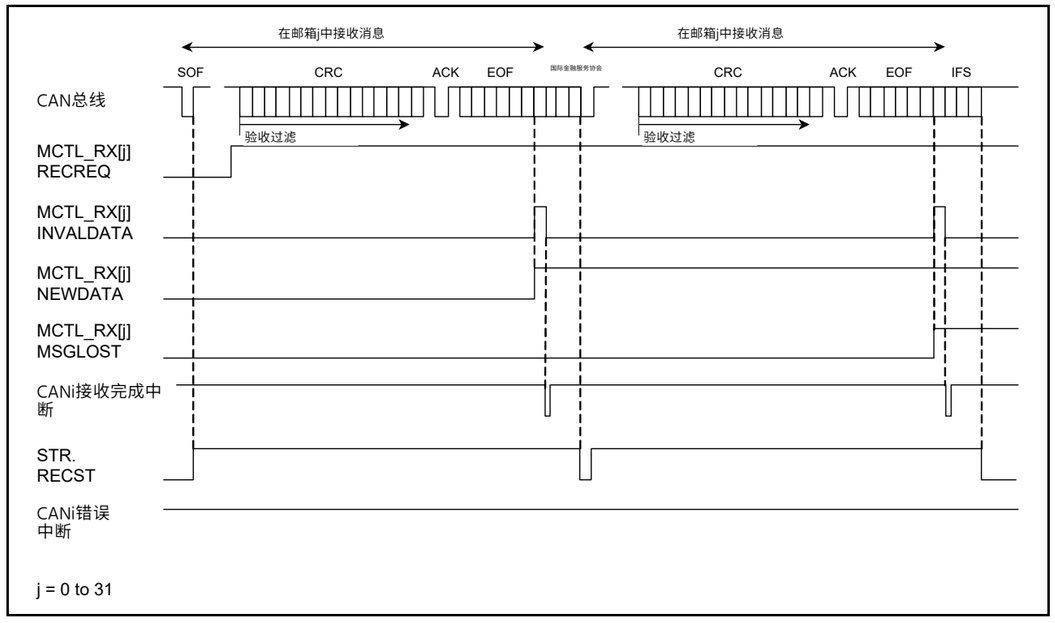


Figure 37.18 覆盖模式下数据帧接收的操作示例

1. 当在CAN总线上检测到SOF时，如果CAN模块没有准备好开始发送的消息，则STR中的RECST位设置为1（正在接收）。
2. 接受过滤从CRC字段的开头开始，以选择接收邮箱。
3. 收到消息后，接收邮箱的MCTL_RXj中的NEWDATA标志设置为1（新消息正在存储或已存储在邮箱中）。MCTL_RXj中的INVALDATA标志同时设置为1（消息正在更新），然后在完整的消息传送到邮箱后再次将INVALDATA标志设置为0（消息有效）。
4. 当接收邮箱的MIER中的中断使能位为1（使能中断）时，INVALDATA标志设置为0，从而触发CAN0接收完成中断请求。
5. 从邮箱读取消息后，NEWDATA标志必须由软件设置为0。
6. 在覆盖模式下，如果在MCTL_RXj中的NEWDATA标志设置为1时接收到下一条CAN消息，则MCTL_RXj中的MSGLOST标志设置为1（消息被覆盖）。新收到的消息被传送到邮箱。CAN0接收完成中断请求的发生与步骤4相同。

图37.19显示了溢出模式下数据帧接收的操作示例。该示例显示当CAN模块接收到与MCTL_RXj（j=0到31）中的接收条件匹配的两个连续CAN报文时，第二条报文的溢出。

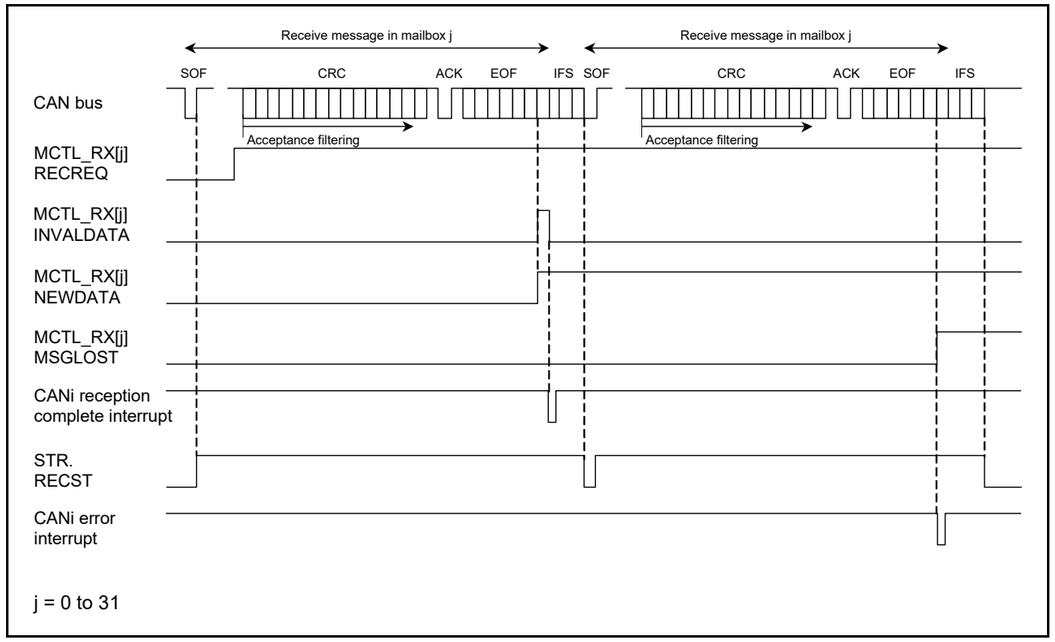


Figure 37.19 Operation example of data frame reception in overrun mode

Steps 1 to 5 are the same as in overwrite mode.

6. In overrun mode, if the next CAN message is received before the NEWDATA flag in MCTL_RXj is set to 0, the MSGLOST flag in MCTL_RXj is set to 1 (message overrun). The new received message is discarded and a CANi error interrupt request occurs if the associated interrupt enable bit in EIER is set to 1 (interrupt enabled).

37.7.2 Transmission

Figure 37.20 shows an operation example of data frame transmission.

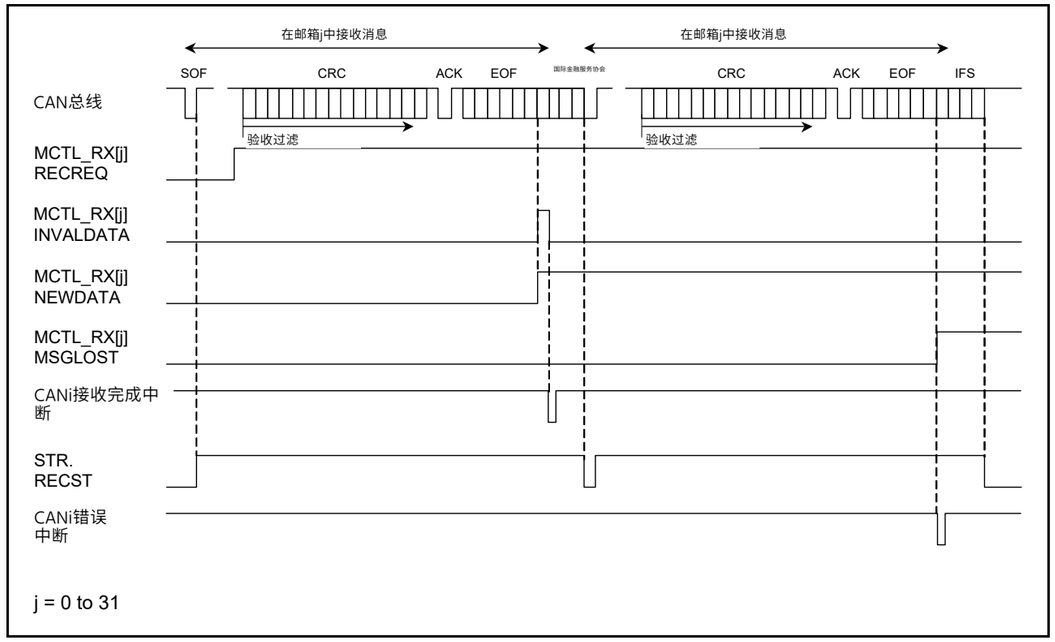


Figure 37.19 溢出模式下数据帧接收的操作示例

步骤1至5与覆盖模式相同。

6. 在溢出模式下，如果在MCTL_RXj中的NEWDATA标志设置为0之前接收到下一个CAN报文，则MCTL_RXj中的MSGLOST标志设置为1（消息溢出）。如果EIER中的相关中断使能位设置为1（中断使能），则丢弃新接收到的消息并产生CANi错误中断请求。

37.7.2 Transmission

图37.20显示了数据帧传输的操作示例。

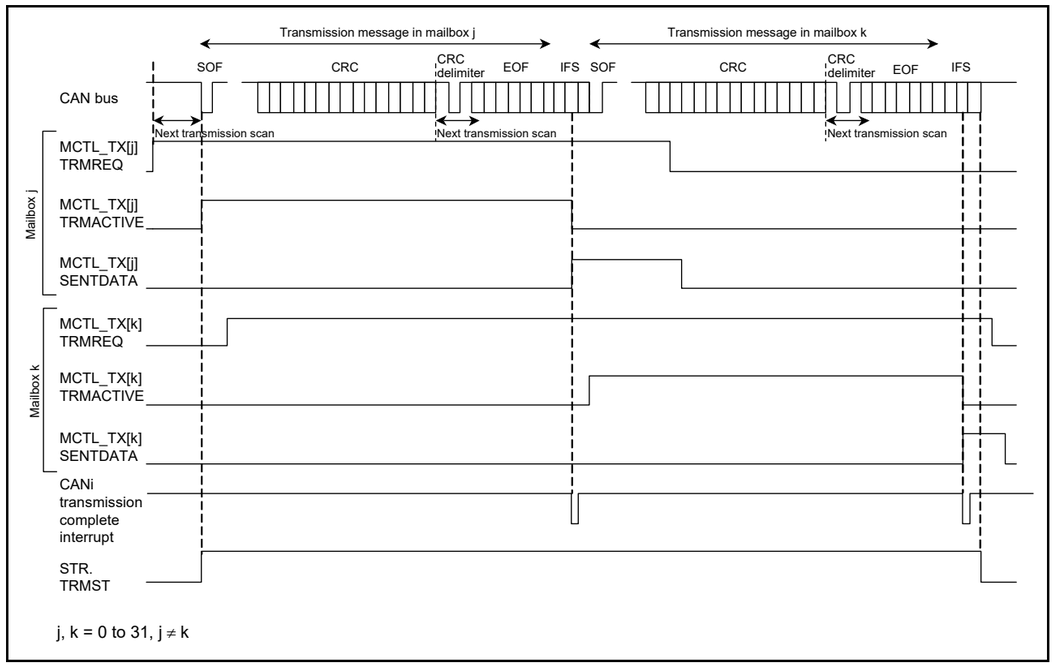


Figure 37.20 Operation example of data frame transmission

1. When a TRMREQ bit in MCTL_TXj (j = 0 to 31) is set to 1 (transmit mailbox) in the bus-idle state, mailbox scanning starts to decide the highest-priority mailbox for transmission. When the transmit mailbox is decided, the TRMACTIVE flag in MCTL_TXj is set to 1 (from acceptance of transmission request to completion of transmission, or error or arbitration-lost), the TRMST bit in STR is set to 1 (transmission in progress), and the CAN module starts transmission.*1
2. If other TRMREQ bits are set, the transmission scanning starts with the CRC delimiter for the next transmission.
3. If transmission is completed without losing arbitration, the SENTDATA flag in MCTL_TXj is set to 1 (transmission complete) and the TRMACTIVE flag is set to 0 (transmission is pending or transmission is not requested). If the interrupt enable bit in MIER is 1 (interrupt enabled), the CANi transmission complete interrupt request is generated.
4. When requesting the next transmission from the same mailbox, set the SENTDATA flag and TRMREQ bit to 0, and then set the TRMREQ bit to 1 after checking that the SENTDATA flag and TRMREQ bit are set to 0.

Note 1. If arbitration is lost after the CAN module starts transmission, the TRMACTIVE flag is set to 0. Transmission scanning is performed again to search for the highest-priority transmit mailbox from the beginning of the CRC delimiter. If an error occurs either during transmission or following arbitration-lost, transmission scanning is performed again to search for the highest-priority transmit mailbox from the start of the error delimiter.

37.8 Interrupts

The CAN module provides the following interrupts for each channel. Table 37.11 lists the CAN interrupts.

- CANi reception complete interrupt for mailboxes 0 to 31 (CANi_RXM)
- CANi transmission complete interrupt for mailboxes 0 to 31 (CANi_TXM)
- CANi receive FIFO interrupt (CANi_RXF)
- CANi transmit FIFO interrupt (CANi_TXF)
- CANi error interrupt (CANi_ERS).

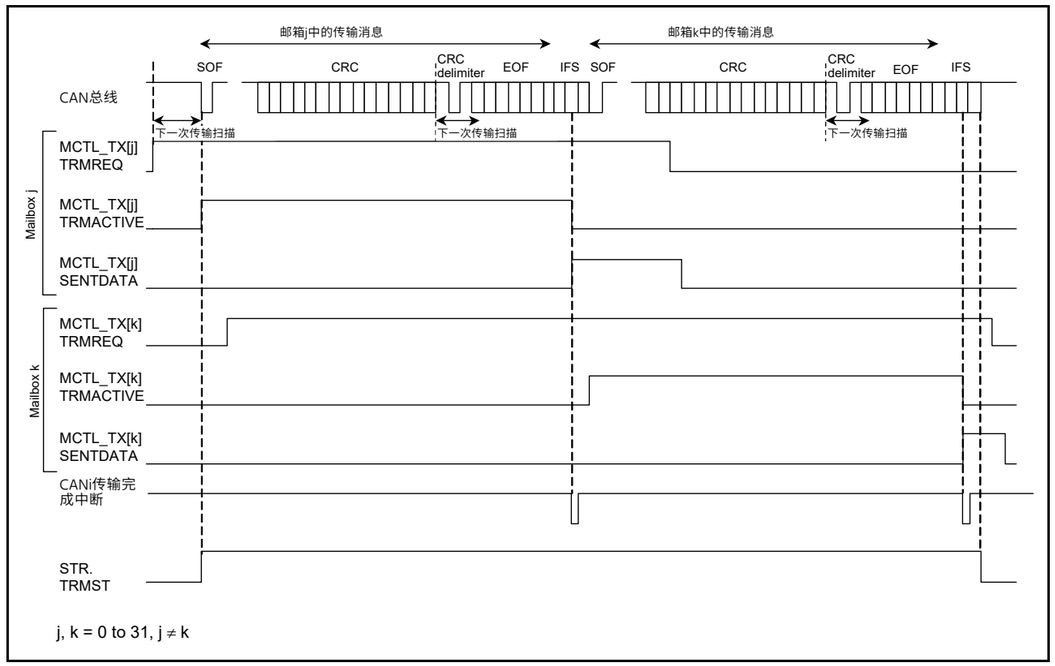


Figure 37.20 数据帧传输的操作示例

1. 当MCTL_TXj（j=0到31）中的TRMREQ位在总线空闲状态下设置为1（发送邮箱）时，邮箱扫描开始决定发送的最高优先级邮箱。当确定发送邮箱时，MCTL_TXj中的TRMACTIVE标志设置为1（从接受发送请求到发送完成，或错误或仲裁丢失），STR中的TRMST位设置为1（正在发送），CAN模块开始传输。*1
2. 如果设置了其他TRMREQ位，则传输扫描以CRC定界符开始，以进行下一次传输。
3. 如果传输完成且没有丢失仲裁，则MCTL_TXj中的SENTDATA标志设置为1（传输完成），TRMACTIVE标志设置为0（传输未决或未请求传输）。如果MIER中的中断使能位为1（中断使能），则产生CANi传输完成中断请求。
4. 从同一邮箱请求下一次发送时，将SENTDATA标志和TRMREQ位设置为0，然后在检查SENTDATA标志和TRMREQ位设置为0后将TRMREQ位设置为1。

注1.如果CAN模块开始发送后仲裁丢失，则TRMACTIVE标志设置为0。再次执行发送扫描以从CRC分隔符的开头搜索优先级最高的发送邮箱。如果在传输过程中或仲裁丢失后发生错误，则再次执行传输扫描以从错误分隔符的开头搜索最高优先级的传输邮箱。

37.8 Interrupts

CAN模块为每个通道提供以下中断。表37.11列出了CAN中断。

- 邮箱0到31(CANi_RXM)的CANi接收完成中断
- 邮箱0到31(CANi_TXM)的CANi传输完成中断
- CANi接收FIFO中断(CANi_RXF)
- CANi发送FIFO中断(CANi_TXF)
- CANi错误中断(CANi_ERS)。

Eight interrupt sources are available for CANi error interrupts. Check EIFR to determine whether these sources were triggered:

- Bus error
- Error-warning
- Error-passive
- Bus-off entry
- Bus-off recovery
- Receive overrun
- Overload frame transmission
- Bus lock.

Table 37.11 CAN interrupts

Module	Interrupt name	Interrupt source	Source flag
CANi i = 0, 1	CANi_ERS	Bus lock detected	EIFR.BLIF
		Overload frame transmission detected	EIFR.OLIF
		Overrun detected	EIFR.ORIF
		Bus-off recovery detected	EIFR.BORIF
		Bus-off entry detected	EIFR.BOEIF
		Error-passive detected	EIFR.EPIF
		Error-warning detected	EIFR.EWIF
		Bus error detected	EIFR.BEIF
	CANi_RXF	Receive FIFO message received (MIER_FIFO.MB29 = 0)	RFCR.RFUST[2:0]
		Receive FIFO warning (MIER_FIFO.MB29 = 1)	
	CANi_TXF	Transmit FIFO message transmission completed (MIER_FIFO.MB25 = 0)	TFCR.TFUST[2:0]
		FIFO last message transmission completed (MIER_FIFO.MB25 = 1)	
	CANi_RXM	Mailbox 0 to 31 message received	MCTL_RX0.NEWDATA to MCTL_RX31.NEWDATA
	CANi_TXM	Mailbox 0 to 31 message transmission completed	MCTL_TX0.SENTDATA to MCTL_TX31.SENTDATA

37.9 Usage Notes

37.9.1 Settings for the Module-Stop Function

CAN operation can be disabled or enabled using Module Stop Control Register B (MSTPCRB). The CAN module is initially stopped after reset. Releasing the module-stop state enables access to the registers. For details, see section 11, Low Power Modes.

37.9.2 Settings for the Operating Clock

The settings for the operating clock can be made as follows:

- The following clock constraint must be satisfied for the CAN module when the CCLKS bit is 1:

  fPCLKB ≥ fCANMCLK

- The source of the peripheral module clock must be PLL for the CAN module when the CCLKS bit is 0.

八个中断源可用于CANi错误中断。检查EIFR以确定是否触发了这些源：

- 总线错误
- Error-warning
- Error-passive
- Bus-off entry
- Bus-off recovery
- 接收溢出
- 过载帧传输
- 巴士锁。

Table 37.11 CAN中断

Module	中断名称	中断源	源标志
CANi i = 0, 1	CANi_ERS	检测到总线锁	EIFR.BLIF
		检测到过载帧传输	EIFR.OLIF
		检测到溢出	EIFR.ORIF
		检测到总线关闭恢复	EIFR.BORIF
		检测到总线关闭条目	EIFR.BOEIF
		Error-passive detected	EIFR.EPIF
		Error-warning detected	EIFR.EWIF
		检测到总线错误	EIFR.BEIF
	CANi_RXF	接收接收到的FIFO消息(MIER_FIFO.MB29=0)	RFCR.RFUST[2:0]
		接收FIFO警告(MIER_FIFO.MB29=1)	
	CANi_TXF	传输FIFO消息传输完成(MIER_FIFO.MB25=0)	TFCR.TFUST[2:0]
		FIFO最后一条消息传输完成(MIER_FIFO.MB25=1)	
	CANi_RXM	邮箱0到31收到消息	MCTL_RX0.NEWDATA to MCTL_RX31.NEWDATA
	CANi_TXM	邮箱0到31消息传输完成	MCTL_TX0.SENTDATA to MCTL_TX31.SENTDATA

37.9 使用说明

37.9.1 模块停止功能的设置

可以使用模块停止控制寄存器B(MSTPCRB)禁用或启用CAN操作。CAN模块在复位后最初停止。释放模块停止状态可以访问寄存器。有关详细信息，请参阅第11节，低功耗模式。

37.9.2 工作时钟设置

工作时钟的设置可按如下方式进行：

- 当CCLKS位为1时，CAN模块必须满足以下时钟约束：

  fPCLKB ≥ fCANMCLK

- 当CCLKS位为0时，外设模块时钟源必须是CAN模块的PLL。

38. Serial Peripheral Interface (SPI)

38.1 Overview

The MCU provides two independent channels for the Serial Peripheral Interface (SPI). The SPI channels are capable of high-speed, full-duplex, synchronous serial communications with multiple processors and peripheral devices. Table 38.1 lists the SPI specifications, Figure 38.1 shows a block diagram, and Table 38.2 lists the I/O pins.

In this section, *n* indicates A or B, and *i* indicates 0 or 1. A lower-case letter *i* in pin and signal names indicates a value from 0 to 3, and a lower-case letter *m* in SPI Command Register m (SPCMDm) indicates a value from 0 to 7.

Table 38.1 SPI specifications (1 of 2)

Parameter	Specifications
Number of channels	Two channels
SPI transfer functions	• Use of MOSI (master out/slave in), MISO (master in/slave out), SSL (slave select), and RSPCK (SPI clock) signals allows serial communications through SPI operation (4-wire method) or clock synchronous operation (3-wire method) • Transmit-only operation available • Communication mode selectable to full-duplex or transmit-only • RSPCK polarity switching • RSPCK phase switching
Data format	• MSB-first or LSB-first selectable • Transfer bit length selectable to 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits • 128-bit transmit and receive buffers • Up to four frames transferrable in one round of transmission or reception (each frame consisting of up to 32 bits) • Byte swap operating function
Bit rate	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLKA (the division ratio ranges from divided by 2 to divided by 4096) • In slave mode, the minimum PCLKA clock divided by 4 can be input as RSPCK (PCLKA divided by 4 is the maximum RSPCK frequency) Width at high level: 2 PCLKA cycles; width at low level: 2 PCLKA cycles
Buffer configuration	• Double buffer configuration for the transmit and receive buffers • 128 bits for the transmit and receive buffers
Error detection	• Mode fault error detection • Underrun error detection • Overrun error detection*1 • Parity error detection
SSL control function	• Four SSL pins (SSLn0 to SSLn3) for each channel • In single master mode, SSLn0 to SSLn3 pins are output. • In multi-master mode, SSLn0 pin for input, and SSLn1 to SSLn3 pins either for output or unused • In slave mode, SSLn0 pin for input, and SSLn1 to SSLn3 pins unused • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Controllable wait for next-access SSL output assertion (next-access delay) Range: 1 to 8 RSPCK cycles (set in RSPCK-cycle units) • Function for changing SSL polarity
Control in master transfer	• Transfers of up to eight commands each can be executed sequentially in looped execution • For each command, the following can be set: SSL signal value, bit rate, RSPCK polarity and phase, transfer data length, MSB- or LSB-first, burst, RSPCK delay, SSL negation delay, and next-access delay • Transfers can be initiated by writing to the transmit buffer • MOSI signal value specifiable in SSL negation • RSPCK auto-stop function
Interrupt sources	Interrupt sources: • Receive buffer full interrupt • Transmit buffer empty interrupt • SPI error interrupt (mode fault, overrun, parity error) • SPI idle interrupt (SPI idle) • Transmission-complete interrupt

38. 串行外设接口(SPI)

38.1 Overview

MCU为串行外设接口(SPI)提供两个独立通道。SPI通道能够与多个处理器和外围设备进行高速、全双工、同步串行通信。表38.1列出了SPI规格，图38.1显示了框图，表38.2列出了IO引脚。

在本节中，n表示A或B，i表示0或1。引脚和信号名称中的小写字母i表示从0到3的值，SPI命令寄存器m(SPCMDm)中的小写字母m)表示从0到7的值。

Table 38.1 SPI规格（2个中的1个）

Parameter	Specifications
通道数	两个通道
SPI传输函数	使用MOSI（主输出从输入）、MISO（主输入从输出）、SSL（从选择）和RSPCK（SPI时钟）信号允许通过SPI操作（4线方法）或时钟同步操作（3线法） 仅传输操作可用 通信模式可选择为全双工或仅传输 RSPCK极性切换 RSPCK相位切换
数据格式	可选择MSB优先或LSB优先 传输位长度可选择为8、9、10、11、12、13、14、15、16、20、24或32位 128位发送和接收缓冲区 向上在一轮发送或接收中可传输到四帧（每帧最多由32位组成） 字节交换操作功能
比特率	在主机模式下，片内波特率发生器通过对PCLKA分频产生RSPCK（分频比范围从2分频到4096分频） 在从机模式下，可以输入最小PCLKA时钟4分频作为RSPCK（PCLKA除以4为最大RSPCK频率）高电平宽度：2个PCLKA周期；低电平宽度：2个PCLKA周期
缓冲区配置	发送和接收缓冲区的双缓冲区配置 发送和接收缓冲区为128位
错误检测	模式故障错误检测 欠载错误检测 溢出错误检测*1 奇偶校验错误检测
SSL控制功能	每个通道有四个SSL引脚（SSLn0到SSLn3） 在单主模式下，输出SSLn0到SSLn3引脚。 在多主模式下，SSLn0引脚用于输入，SSLn1至SSLn3引脚用于输出或未使用 从模式下，SSLn0引脚用于输入，SSLn1至SSLn3引脚未使用 从SSL输出断言到RSPCK操作的可控延迟（RSPCK延迟）范围：1到8个RSPCK周期（以RSPCK周期为单位设置） 从RSPCK停止到SSL输出否定的可控延迟（SSL否定延迟）范围：1到8个RSPCK周期（以RSPCK周期为单位设置） 可控等待用于下一次访问SSL输出断言（下一次访问延迟）范围：1到8个RSPCK周期（以RSPCK周期为单位设置） 更改SSL极性的功能
主传输中的控制	最多可以在循环执行中顺序执行8个命令的传输 对于每个命令，可以设置以下内容： SSL信号值、比特率、RSPCK极性和相位、传输数据长度、MSB或LSB优先、突发、RSPCK延迟、SSL否定延迟和下一次访问延迟 可以通过写入传输缓冲区来启动传输 在SSL否定中指定MOSI信号值 RSPCK自动停止功能
中断源	中断源： 接收缓冲区满中断 发送缓冲区空中断 SPI错误中断（模式错误、溢出、奇偶校验错误） SPI空闲中断（SPI空闲） 传输完成中断

Table 38.1 SPI specifications (2 of 2)

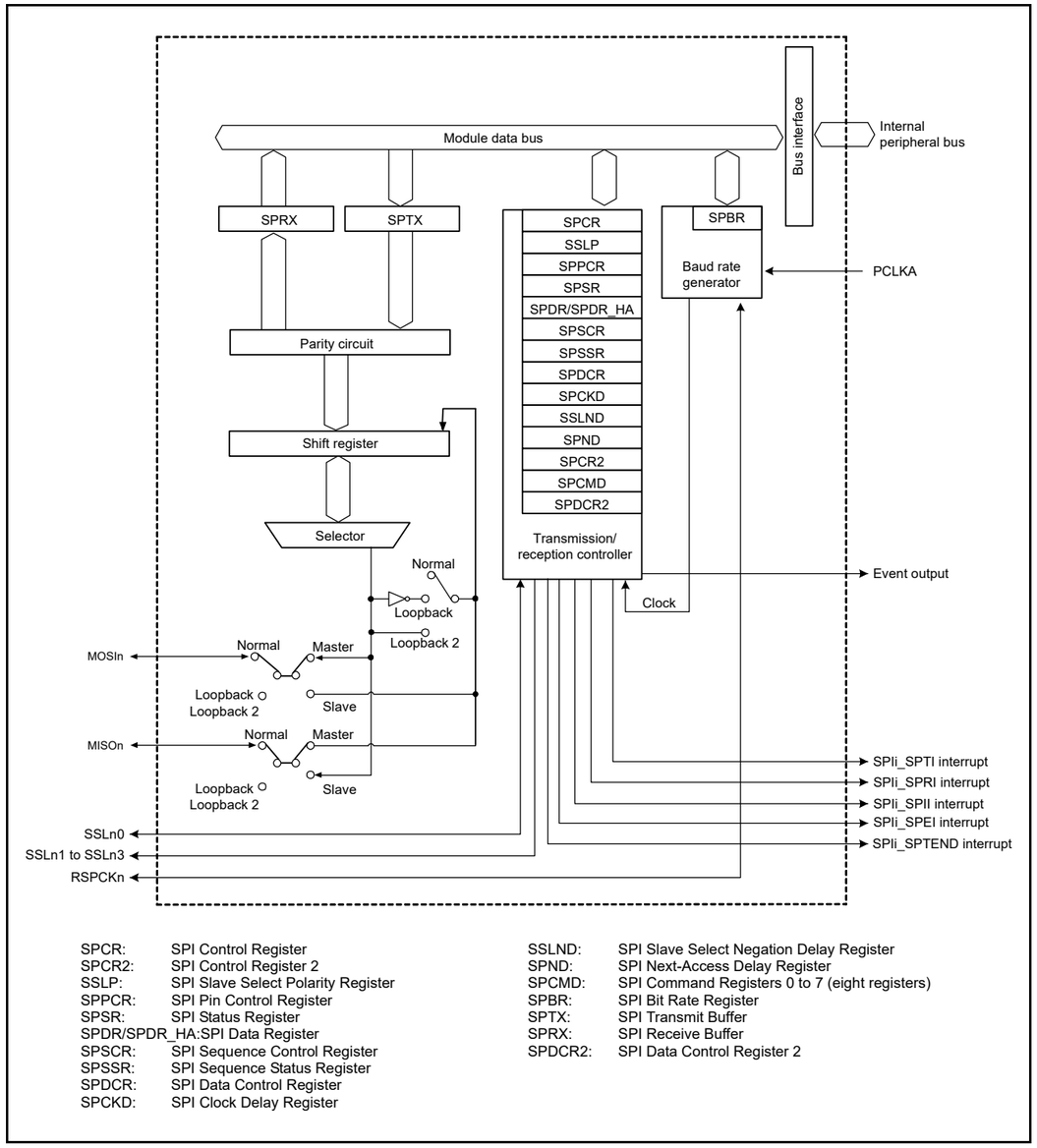
Parameter	Specifications
Event link function (output)	The following events can be output to the Event Link Controller (ELC): • Receive buffer full signal • Transmit buffer empty signal • Mode fault, underrun, overrun, or parity error signal • SPI idle signal • Transmission-complete signal
Other functions	• Switching between CMOS output and open-drain output • SPI initialization function • Loopback mode
Module-stop function	Module-stop state can be set to reduce power consumption

Note 1. In master reception and when the RSPCK auto-stop function is enabled, an overrun error does not occur because the transfer clock is stopped on overrun error detection.

Table 38.1 SPI规范（2个中的2个）

Parameter	Specifications
事件链接功能（输出）	以下事件可以输出到事件链接控制器(ELC)： 接收缓冲区满信号 发送缓冲区空信号 模式错误、欠载、溢出或奇偶校验错误信号 SPI空闲信号 传输完成信号
其他功能	在CMOS输出和开漏输出之间切换 SPI初始化功能 Loopback模式
Module-stop function	可设置模块停止状态以降低功耗

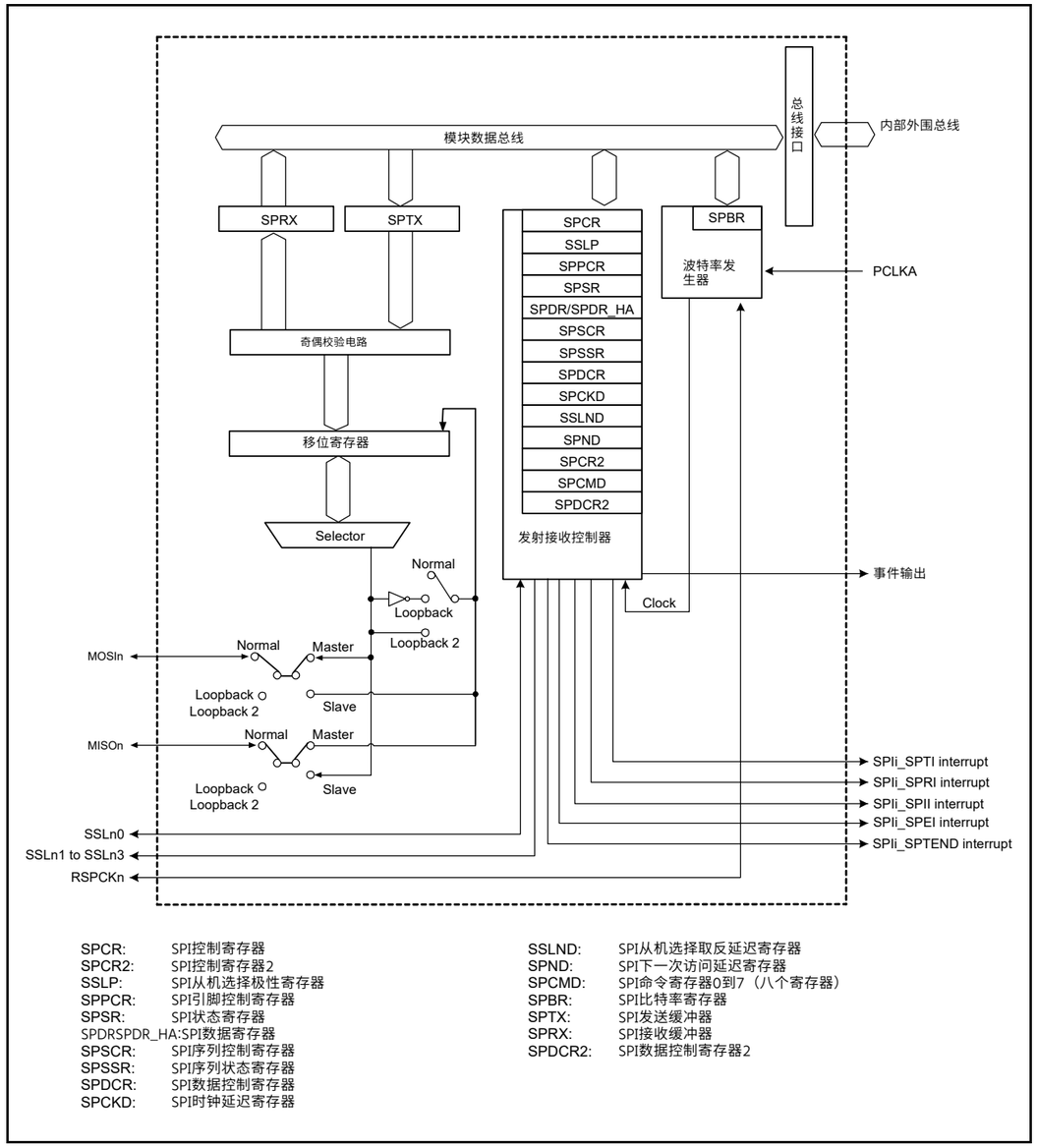
Note 1. 在主机接收和启用RSPCK自动停止功能时，不会发生溢出错误，因为传输时钟在检测到溢出错误时停止。



SPCR: SPI Control Register
SPCR2: SPI Control Register 2
SSLP: SPI Slave Select Polarity Register
SPPCR: SPI Pin Control Register
SPSR: SPI Status Register
SPDR/SPDR_HA:SPI Data Register
SPSCR: SPI Sequence Control Register
SPSSR: SPI Sequence Status Register
SPDCR: SPI Data Control Register
SPCKD: SPI Clock Delay Register
SSLND: SPI Slave Select Negation Delay Register
SPND: SPI Next-Access Delay Register
SPCMD: SPI Command Registers 0 to 7 (eight registers)
SPBR: SPI Bit Rate Register
SPTX: SPI Transmit Buffer
SPRX: SPI Receive Buffer
SPDCR2: SPI Data Control Register 2

Figure 38.1 SPI block diagram

Table 38.2 lists the I/O pins used in the SPI. The SPI automatically switches the I/O direction of the SSLn0 pin. SSLn0 is set as an output when the SPI is a single master and as an input when the SPI is a multi-master or a slave. The RSPCKn, MOSIn, and MISOn pins are automatically set as inputs or outputs based on the master or slave setting and the level input on the SSLn0 pin. For details, see section 38.3.2, Controlling the SPI Pins.



SPCR: SPI控制寄存器
SPCR2: SPI控制寄存器2
SSLP: SPI从机选择极性寄存器
SPPCR: SPI引脚控制寄存器
SPSR: SPI状态寄存器
SPDRSPDR_HA:SPI数据寄存器
SPSCR: SPI序列控制寄存器
SPSSR: SPI序列状态寄存器
SPDCR: SPI数据控制寄存器
SPCKD: SPI时钟延迟寄存器
SSLND: SPI从机选择取反延迟寄存器
SPND: SPI下一次访问延迟寄存器
SPCMD: SPI命令寄存器0到7（八个寄存器）
SPBR: SPI比特率寄存器
SPTX: SPI发送缓冲器
SPRX: SPI接收缓冲器
SPDCR2: SPI数据控制寄存器2

Figure 38.1 SPI框图

表38.2列出了SPI中使用的IO引脚。SPI自动切换SSLn0引脚的IO方向。当SPI为单主机时SSLn0设置为输出，当SPI为多主机或从机时设置为输入。RSPCKn、MOSIn和MISOn引脚会根据主机或从机设置以及SSLn0引脚上的电平输入自动设置为输入或输出。有关详细信息，请参见第38.3.2节，控制SPI引脚。

Table 38.2 SPI I/O pins

Channel	Pin name	I/O	Function
SPI0	RSPCKA	I/O	Clock input/output
	MOSIA	I/O	Master transmit data input/output
	MISOA	I/O	Slave transmit data input/output
	SSLA0	I/O	Slave selection input/output
	SSLA1	Output	Slave selection output
	SSLA2	Output	Slave selection output
	SSLA3	Output	Slave selection output
SPI1	RSPCKB	I/O	Clock input/output
	MOSIB	I/O	Master transmit data input/output
	MISOB	I/O	Slave transmit data input/output
	SSLB0	I/O	Slave selection input/output
	SSLB1	Output	Slave selection output
	SSLB2	Output	Slave selection output
	SSLB3	Output	Slave selection output

38.2 Register Descriptions

38.2.1 SPI Control Register (SPCR)

Address(es): SPI0.SPCR 4007 2000h, SPI1.SPCR 4007 2100h

	b7	b6	b5	b4	b3	b2	b1	b0
	SPRIE	SPE	SPTIE	SPEIE	MSTR	MODF EN	TXMD	SPMS
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	SPMS	SPI Mode Select	0: Select SPI operation (4-wire method) 1: Select clock synchronous operation (3-wire method).	R/W
b1	TXMD	Communications Operating Mode Select	0: Select full-duplex synchronous serial communications 1: Select serial communications with transmit-only.	R/W
b2	MODFEN	Mode Fault Error Detection Enable	0: Disable detection of mode fault errors 1: Enable detection of mode fault errors.	R/W
b3	MSTR	SPI Master/Slave Mode Select	0: Select slave mode 1: Select master mode.	R/W
b4	SPEIE	SPI Error Interrupt Enable	0: Disable SPI error interrupt requests 1: Enable SPI error interrupt requests.	R/W
b5	SPTIE	Transmit Buffer Empty Interrupt Enable	0: Disable transmit buffer empty interrupt requests 1: Enable transmit buffer empty interrupt requests.	R/W
b6	SPE	SPI Function Enable	0: Disable SPI function 1: Enable SPI function.	R/W
b7	SPRIE	SPI Receive Buffer Full Interrupt Enable	0: Disable SPI receive buffer full interrupt requests 1: Enable SPI receive buffer full interrupt requests.	R/W

If the SPCR.MSTR, SPCR.MODFEN, or SPCR.TXMD bit is changed while the SPCR.SPE bit is 1, do not perform subsequent operations.

SPMS bit (SPI Mode Select)

The SPMS bit selects SPI operation (4-wire method) or clock synchronous operation (3-wire method).

Table 38.2 SPIIO引脚

Channel	引脚名称	I/O	Function
SPI0	RSPCKA	I/O	Clock input/output
	MOSIA	I/O	主机发送数据输入输出
	MISOA	I/O	从机发送数据输入输出
	SSLA0	I/O	从机选择输入输出
	SSLA1	Output	从机选择输出
	SSLA2	Output	从机选择输出
	SSLA3	Output	从机选择输出
SPI1	RSPCKB	I/O	Clock input/output
	MOSIB	I/O	主机发送数据输入输出
	MISOB	I/O	从机发送数据输入输出
	SSLB0	I/O	从机选择输入输出
	SSLB1	Output	从机选择输出
	SSLB2	Output	从机选择输出
	SSLB3	Output	从机选择输出

38.2 注册说明

38.2.1 SPI控制寄存器(SPCR)

Address(es): SPI0.SPCR 4007 2000h, SPI1.SPCR 4007 2100h

	b7	b6	b5	b4	b3	b2	b1	b0
	SPRIE	SPE	SPTIE	SPEIE	MSTR	MODF EN	TXMD	SPMS
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	SPMS	SPI模式选择	0：选择SPI操作（4线方式）1：选择时钟同步操作（3线方式）。	R/W
b1	TXMD	通讯操作模式 Select	0：选择全双工同步串行通信1：选择仅发送的串行通信。	R/W
b2	MODFEN	模式故障错误检测启用	0：禁用模式故障错误检测1：启用模式故障错误检测。	R/W
b3	MSTR	SPI主从模式选择	0：选择从模式1：选择主模式。	R/W
b4	SPEIE	SPI错误中断使能	0：禁用SPI错误中断请求1：启用SPI错误中断请求。	R/W
b5	SPTIE	发送缓冲区空中断 Enable	0：禁止发送缓冲区空中断请求1：使能发送缓冲区空中断请求。	R/W
b6	SPE	SPI功能使能	0：禁用SPI功能1：启用SPI功能。	R/W
b7	SPRIE	SPI接收缓冲器满中断 Enable	0：禁止SPI接收缓冲区满中断请求1：使能SPI接收缓冲区满中断请求。	R/W

如果在SPCR.SPE位为1时更改了SPCR.MSTR、SPCR.MODFEN或SPCR.TXMD位，则不要执行后续操作。

SPMS位（SPI模式选择）

SPMS位选择SPI操作（4线方法）或时钟同步操作（3线方法）。

The SSLn0 to SSLn3 pins are not used in clock synchronous operation. The RSPCKn, MOSIn, and MISOn pins handle communications. For clock synchronous operation in master mode (SPCR.MSTR = 1), the SPCMDm.CPHA bit can be set to either 0 or 1. For clock synchronous operation in slave mode (SPCR.MSTR = 0), always set the CPHA bit to 1. Do not perform operations if the CPHA bit is set to 0 for clock synchronous operation in slave mode (SPCR.MSTR = 0).

TXMD bit (Communications Operating Mode Select)

The TXMD bit selects full-duplex synchronous serial communications or transmit-only operations. When this bit is set to 1, the SPI only performs transmit operations and not receive operations (see section 38.3.6, Data Transfer Modes), and receive buffer full interrupt requests cannot be used.

MODFEN bit (Mode Fault Error Detection Enable)

The MODFEN bit enables or disables the detection of mode fault errors (see section 38.3.8, Error Detection). In addition, the SPI determines the I/O direction of the SSLn0 to SSLn3 pins based on combination of the MODFEN and MSTR bits (see section 38.3.2, Controlling the SPI Pins).

MSTR bit (SPI Master/Slave Mode Select)

The MSTR bit selects master or slave mode for the SPI. Based on the MSTR bit settings, the SPI determines the direction of the RSPCKn, MOSIn, MISOn, and SSLn0 to SSLn3 pins.

SPEIE bit (SPI Error Interrupt Enable)

The SPEIE bit enables or disables the generation of SPI error interrupt requests when one of the following occurs:

- The SPI detects a mode fault error or underrun error and sets the SPSR.MODF flag to 1
- The SPI detects an overrun error and sets the SPSR.OVRF flag to 1
- The SPI detects a parity error and sets the SPSR.PERF flag to 1.

For details, see section 38.3.8, Error Detection.

SPTIE bit (Transmit Buffer Empty Interrupt Enable)

The SPTIE bit enables or disables the generation of transmit buffer empty interrupt requests when the SPI detects that the transmit buffer is empty. To generate a transmit buffer empty interrupt request when transmission starts, set the SPE and SPTIE bits to 1 at the same time or set the SPE bit to 1 after setting the SPTIE bit to 1.

When the SPTIE bit is 1, transmit buffer interrupts are generated even when the SPI function is disabled (when the SPE bit is changed to 0).

SPE bit (SPI Function Enable)

The SPE bit enables or disables the SPI function. The SPE bit cannot be set to 1 when the SPSR.MODF flag is 1. For details, see section 38.3.8, Error Detection.

Setting the SPE bit to 0 disables the SPI function and initializes a part of the module function. For details, see section 38.3.9, Initializing the SPI. In addition, a transmit buffer empty interrupt request is generated when the SPE bit is changed from 0 to 1 or from 1 to 0.

SPRIE bit (SPI Receive Buffer Full Interrupt Enable)

The SPRIE bit enables or disables the generation of an SPI receive buffer full interrupt request when the SPI detects a receive buffer full write after completion of a serial transfer.

SSLn0到SSLn3引脚不用于时钟同步操作。RSPCKn、MOSIn和MIOn引脚处理通信。对于主机模式下的时钟同步操作(SPCR.MSTR=1)，SPCMDm.CPHA位可以设置为0或1。对于从机模式下的时钟同步操作(SPCR.MSTR=0)，始终将CPHA位设置为1.如果CPHA位设置为0以在从机模式下进行时钟同步操作（SPCR.MSTR=0），则不要执行操作。

TXMD位（通信操作模式选择）

TXMD位选择全双工同步串行通信或仅发送操作。当该位设置为1时，SPI只执行发送操作而不执行接收操作（参见第38.3.6节，数据传输模式），并且无法使用接收缓冲区满中断请求。

MODFEN位（模式故障错误检测使能）

MODFEN位启用或禁用模式故障错误检测（参见第38.3.8节，错误检测）。此外，SPI根据MODFEN和MSTR位的组合确定SSLn0到SSLn3引脚的IO方向（请参见第38.3.2节，控制SPI引脚）。

MSTR位（SPI主从模式选择）

MSTR位选择SPI的主模式或从模式。根据MSTR位设置，SPI确定RSPCKn、MOSIn、MISOn和SSLn0到SSLn3引脚的方向。

SPEIE位（SPI错误中断使能）

当发生以下情况之一时，SPEIE位启用或禁用SPI错误中断请求的生成：

- SPI检测到模式故障错误或欠载错误并将SPSR.MODF标志设置为1
- SPI检测到溢出错误并将SPSR.OVRF标志设置为1
- SPI检测到奇偶校验错误并将SPSR.PERF标志设置为1。

有关详细信息，请参阅第38.3.8节，错误检测。

SPTIE位（发送缓冲区空中断使能）

当SPI检测到发送缓冲区为空时，SPTIE位使能或禁止生成发送缓冲区空中断请求。要在发送开始时产生发送缓冲区空中断请求，请将SPE和SPTIE位同时设置为1，或在将SPTIE位设置为1后将SPE位设置为1。

当SPTIE位为1时，即使禁用SPI功能（当SPE位变为0时）也会产生发送缓冲区中断。

SPE位（SPI功能使能）

SPE位启用或禁用SPI功能。当SPSR.MODF标志为1时，SPE位不能设置为1。有关详细信息，请参阅第38.3.8节，错误检测。

将SPE位设置为0将禁用SPI功能并初始化部分模块功能。有关详细信息，请参阅第38.3.9节，初始化SPI。此外，当SPE位从0变为1或从1变为0时，会产生发送缓冲区空中断请求。

SPRIE位（SPI接收缓冲区满中断使能）

当SPI在串行传输完成后检测到接收缓冲区已满写入时，SPRIE位启用或禁用SPI接收缓冲区已满中断请求的生成。

38.2.2 SPI Slave Select Polarity Register (SSLP)

Address(es): SPI0.SSLP 4007 2001h, SPI1.SSLP 4007 2101h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	SSL3P	SSL2P	SSL1P	SSL0P
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	SSL0P	SSL0 Signal Polarity Setting	0: Set SSL0 signal to active low 1: Set SSL0 signal to active high.	R/W
b1	SSL1P	SSL1 Signal Polarity Setting	0: Set SSL1 signal to active low 1: Set SSL1 signal to active high.	R/W
b2	SSL2P	SSL2 Signal Polarity Setting	0: Set SSL2 signal to active low 1: Set SSL2 signal to active high.	R/W
b3	SSL3P	SSL3 Signal Polarity Setting	0: Set SSL3 signal to active low 1: Set SSL3 signal to active high.	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

If the contents of SSLP are changed while the SPCR.SPE bit is 1, do not perform subsequent operations.

38.2.3 SPI Pin Control Register (SPPCR)

Address(es): SPI0.SPPCR 4007 2002h, SPI1.SPPCR 4007 2102h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	MOIFE	MOIFV	—	—	SPLP2	SPLP
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	SPLP	SPI Loopback	0: Normal mode 1: Loopback mode (data is inverted for transmission).	R/W
b1	SPLP2	SPI Loopback 2	0: Normal mode 1: Loopback mode (data is not inverted for transmission).	R/W
b3, b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	MOIFV	MOSI Idle Fixed Value	0: Set level output on MOSIn pin during MOSI idling to correspond to low 1: Set level output on MOSIn pin during MOSI idling to correspond to high.	R/W
b5	MOIFE	MOSI Idle Value Fixing Enable	0: Set MOSI output value to equal final data from previous transfer 1: Set MOSI output value to equal value set in the MOIFV bit.	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

If the contents of SPPCR are changed while the SPCR.SPE bit is 1, do not perform subsequent operations.

SPLP bit (SPI Loopback)

The SPLP bit selects the mode of the SPI pins. When this bit is set to 1, the SPI shuts off the path between the MISOn pin and the shift register if the SPCR.MSTR bit is 1, and between the MOSIn pin and the shift register if the SPCR.MSTR bit is 0. The SPI then connects the input path and output path for the shift register (loopback mode).

SPLP2 bit (SPI Loopback 2)

The SPLP2 bit selects the mode of the SPI pins. When this bit is set to 1, the SPI shuts off the path between the MISOn pin and the shift register if the SPCR.MSTR bit is 1, and between the MOSIn pin and the shift register if the

38.2.2 SPI从机选择极性寄存器(SSLP)

Address(es): SPI0.SSLP 4007 2001h, SPI1.SSLP 4007 2101h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	SSL3P	SSL2P	SSL1P	SSL0P
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	SSL0P	SSL0信号极性设置	0：将SSL0信号设置为低电平有效1： 将SSL0信号设置为高电平有效。	R/W
b1	SSL1P	SSL1信号极性设置	0：将SSL1信号设置为低电平有效1： 将SSL1信号设置为高电平有效。	R/W
b2	SSL2P	SSL2信号极性设置	0：将SSL2信号设置为低电平有效1： 将SSL2信号设置为高电平有效。	R/W
b3	SSL3P	SSL3信号极性设置	0：将SSL3信号设置为低电平有效1： 将SSL3信号设置为高电平有效。	R/W
b7 to b4	—	Reserved	这些位被读取为0。写入值应为0。	R/W

如果SPCR.SPE位为1时SSLP的内容发生了变化，请不要进行后续操作。

38.2.3 SPI引脚控制寄存器(SPPCR)

Address(es): SPI0.SPPCR 4007 2002h, SPI1.SPPCR 4007 2102h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	MOIFE	MOIFV	—	—	SPLP2	SPLP
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	SPLP	SPI Loopback	0：正常模式1：环回模式（数据反转传输）。	R/W
b1	SPLP2	SPI Loopback 2	0：正常模式1：环回模式（数据不反转传输）。	R/W
b3, b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b4	MOIFV	MOSI空闲固定值	0：在MOSI空闲期间将MOSIn引脚上的电平输出设置为对应于低电平1：在MOSI空闲期间将MOSIn引脚上的电平输出设置为对应于高电平。	R/W
b5	MOIFE	MOSI空闲值修复Enable	0：设置MOSI输出值等于上次传输的最终数据1：设置MOSI输出值等于MOIFV位中设置的值。	R/W
b7, b6	—	Reserved	这些位被读取为0。写入值应为0。	R/W

如果在SPCR.SPE位为1时改变了SPPCR的内容，则不要执行后续操作。

SPLP位（SPI环回）

SPLP位选择SPI引脚的模式。当该位设置为1时，如果SPCR.MSTR位为1，则SPI关闭MIOn引脚和移位寄存器之间的路径，如果SPCR.MSTR位为0，则关闭MOSIn引脚和移位寄存器之间的路径。然后SPI连接移位寄存器的输入路径和输出路径（环回模式）。

SPLP2位（SPI环回2）

SPLP2位选择SPI引脚的模式。当该位设置为1时，如果SPCR.MSTR位为1，则SPI关闭MISOn引脚和移位寄存器之间的路径，如果该位为1，则SPI关闭MOSIn引脚和移位寄存器之间的路径。

SPCR.MSTR bit is 0. The SPI then connects the input path and output path for the shift register (loopback mode).

MOIFV bit (MOSI Idle Fixed Value)

If the MOIFE bit is 1 in master mode, the MOIFV bit determines the MOSIn pin output value during the SSL negation period, including the SSL retention period during a burst transfer.

MOIFE bit (MOSI Idle Value Fixing Enable)

The MOIFE bit fixes the MOSIn output value when the SPI is in master mode and in an SSL negation period, including the SSL retention period during a burst transfer. When the MOIFE bit is 0, the SPI outputs the last data from the previous serial transfer during the SSL negation period to the MOSIn pin. When the MOIFE bit is 1, the SPI outputs the fixed value set in the MOIFV bit to the MOSIn pin.

38.2.4 SPI Status Register (SPSR)

Address(es): SPI0.SPSR 4007 2003h, SPI1.SPSR 4007 2103h

	b7	b6	b5	b4	b3	b2	b1	b0
	SPRF	—	SPTEF	UDRF	PERF	MODF	IDLNF	OVRF
Value after reset:	0	0	1	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	OVRF	Overrun Error Flag	0: No overrun error occurred 1: Overrun error occurred.	R/(W)*1
b1	IDLNF	SPI Idle Flag	0: SPI is in the idle state 1: SPI is in the transfer state.	R
b2	MODF	Mode Fault Error Flag	0: No mode fault or underrun error occurred 1: Mode fault error or underrun error occurred.	R/(W)*1
b3	PERF	Parity Error Flag	0: No parity error occurred 1: Parity error occurred.	R/(W)*1
b4	UDRF	Underrun Error Flag	0: Mode fault error occurred (MODF = 1) 1: Underrun error occurred (MODF = 1). This bit is invalid when MODF flag is 0.	R/W*1,*2
b5	SPTEF	SPI Transmit Buffer Empty Flag	0: Data is in the transmit buffer 1: No data is in the transmit buffer.	R/(W)*3
b6	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b7	SPRF	SPI Receive Buffer Full Flag	0: No valid data is in SPDR/SPDR_HA 1: Valid data is in SPDR/SPDR_HA.	R/(W)*3

Note 1. Only 0 can be written to clear the flag after reading 1.
Note 2. The UDRF flag clears at the same time that the software clears the MODF flag.
Note 3. The write value should be 1.

OVRF flag (Overrun Error Flag)

The OVRF flag indicates the occurrence of an overrun error. In master mode (SPCR.MSTR bit = 1) and when the RSPCK clock auto-stop function is enabled (SPCR2.SCKASE bit = 1), overrun errors do not occur. This flag does not set to 1. For details, see section 38.3.8.1, Overrun errors.

[Setting condition]

- When the next serial transfer ends while the SPCR.TXMD bit is 0 and the receive buffer is full.

[Clearing condition]

- When 0 is written to the OVRF flag after the OVRF flag is confirmed to be 1 by a read of SPSR.

IDLNF flag (SPI Idle Flag)

The IDLNF flag indicates the transfer status of the SPI.

SPCR.MSTR位为0。然后SPI连接移位寄存器的输入路径和输出路径（环回模式）。

MOIFV位（MOSI空闲固定值）

如果MOIFE位在主模式下为1，则MOIFV位确定SSL否定期间的MOSIn引脚输出值，包括突发传输期间的SSL保持期间。

MOIFE位（MOSI空闲值固定使能）

MOIFE位在SPI处于主模式和SSL否定周期（包括突发传输期间的SSL保留周期）时固定MOSIn输出值。当MOIFE位为0时，SPI将SSL否定期间上次串行传输的最后一个数据输出到MOSIn引脚。当MOIFE位为1时，SPI将MOIFV位中设置的固定值输出到MOSIn引脚。

38.2.4 SPI状态寄存器(SPSR)

Address(es): SPI0.SPSR 4007 2003h, SPI1.SPSR 4007 2103h

	b7	b6	b5	b4	b3	b2	b1	b0
	SPRF	—	SPTEF	UDRF	PERF	MODF	IDLNF	OVRF
重置后的值：	0	0	1	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	OVRF	溢出错误标志	0：未发生溢出错误1：发生溢出错误。	R/(W)*1
b1	IDLNF	SPI空闲标志	0：SPI处于空闲状态1：SPI处于传输状态。	R
b2	MODF	模式故障错误标志	0：未发生模式故障或欠载错误1：发生模式故障错误或欠载错误。	R/(W)*1
b3	PERF	奇偶校验错误标志	0：未发生奇偶校验错误1：发生奇偶校验错误。	R/(W)*1
b4	UDRF	欠载错误标志	0：发生模式故障错误（MODF=1）1：发生欠载错误（MODF=1）。当MODF标志为0时，该位无效。	R/W*1,*2
b5	SPTEF	SPI发送缓冲区空标志	0：发送缓冲区中有数据1：发送缓冲区中没有数据。	R/(W)*3
b6	—	Reserved	该位读取为0。写入值应为0。	R/W
b7	SPRF	SPI接收缓冲区满标志	0：SPDRSPDR_HA中没有有效数据1：SPDRSPDR_HA中有有效数据。	R/(W)*3

Note 1. 读1后只能写0清除标志。
Note 2. UDRF标志在软件清除MODF标志的同时清除。
Note 3. 写入值应为1。

OVRF标志（溢出错误标志）

OVRF标志指示发生溢出错误。在主机模式（SPCR.MSTR位=1）和当RSPCK时钟自动停止功能使能（SPCR2.SCKASE位=1），不会发生溢出错误。此标志不设置为1。有关详细信息，请参阅第38.3.8.1节，溢出错误。

[Setting condition]

- 当SPCR.TXMD位为0且接收缓冲区已满时，下一次串行传输结束。

[Clearing condition]

- 在通过读取SPSR确认OVRF标志为1后将0写入OVRF标志时。

IDLNF标志（SPI空闲标志）

IDLNF标志指示SPI的传输状态。

[Setting conditions]

Master mode

- When conditions 1. and 2. in the master mode [Clearing conditions] are not satisfied.

Slave mode

- When the SPCR.SPE bit is 1, enabling the SPI function.

[Clearing conditions]

Master mode

- When condition 1. OR conditions 2., 3., and 4. are satisfied.

1. The SPCR.SPE bit is 0, indicating the SPI is initialized.
2. The transmit buffer (SPTX) is empty, indicating that data for the next transfer is not set.
3. The SPSSR.SPCP[2:0] bits are 000b, indicating the beginning of sequence control.
4. The SPI internal sequencer enters the idle state, indicating that operations up to the next-access delay are complete.

Slave mode

- When condition 1. is satisfied.

MODF flag (Mode Fault Error Flag)

The MODF flag indicates the occurrence of a mode fault error or an underrun error. Use the UDRF flag to identify which error occurred.

[Setting conditions]

Multi-master mode

- When the input level of the SSLni pin changes to the active level while the SPCR.MSTR bit is 1 (master mode) and the SPCR.MODFEN bit is 1 (mode fault error detection is enabled). The SPI detects a mode fault error.

Slave mode

- When condition 1. OR 2. is satisfied.

1. The SSLni pin is negated before the RSPCK cycle necessary for data transfer ends while the SPCR.MSTR bit is 0 (slave mode) and the SPCR.MODFEN bit is 1 (mode fault error detection is enabled). The SPI detects a mode fault error.
2. The serial transfer begins while the SPCR.MSTR bit is 0 (slave mode), the SPCR.SPE bit is 1, and the transmission data is not prepared. The SPI detects an underrun error.

The active level of the SSLni signal is determined by the SSLP.SSLiP bit (SSLi signal polarity setting bit).

[Clearing condition]

- When 0 is written to the MODF flag after the MODF flag is confirmed to be 1 by a read of SPSR.

PERF flag (Parity Error Flag)

The PERF flag indicates the occurrence of a parity error.

[Setting condition]

- When a serial transfer ends while the SPCR.TXMD bit is 0 and the SPCR2.SPPE bit is 1. The SPI detects a parity error.

[Clearing condition]

- When 0 is written to the PERF flag after the PERF flag is confirmed to be 1 by a read of SPSR.

UDRF flag (Underrun Error Flag)

The UDRF flag indicates the occurrence of an underrun error.

[Setting conditions]

主模式

- 不满足主模式[清除条件]中的条件1.和2.时。

从机模式

- 当SPCR.SPE位为1时，使能SPI功能。

[Clearing conditions]

主模式

- 当条件1.OR条件2. 3. 和4.满足时。

1. SPCR.SPE位为0，表示SPI已初始化。
2. 发送缓冲区(SPTX)为空，表示未设置下一次传输的数据。
3. SPSSR.SPCP[2:0]位为000b，表示序列控制的开始。
4. SPI内部定序器进入空闲状态，表示直到下一次访问延迟的操作已完成。

从机模式

- 当条件1.满足时。

MODF标志（模式故障错误标志）

MODF标志指示发生模式故障错误或欠载错误。使用UDRF标志来识别发生了哪个错误。

[Setting conditions]

Multi-master mode

- 当SPCR.MSTR位为1（主模式）且SPCR.MODFEN位为1（启用模式故障错误检测）时SSLni引脚的输入电平变为有效电平。SPI检测到模式故障错误。

从机模式

- 当条件1.OR2.满足时。

1. 在SPCR.MSTR位为0（从模式）和SPCR.MODFEN位为1（启用模式故障错误检测）时，SSLni引脚在数据传输所需的RSPCK周期结束之前被取消。SPI检测到模式故障错误。
2. 当SPCR.MSTR位为0（从模式）、SPCR.SPE位为1且未准备传输数据时，串行传输开始。SPI检测到欠载错误。

SSLni信号的有效电平由SSLP.SSLiP位（SSLi信号极性设置位）决定。

[Clearing condition]

- 在通过读取SPSR确认MODF标志为1后，向MODF标志写入0时。

PERF标志（奇偶校验错误标志）

PERF标志指示奇偶校验错误的发生。

[Setting condition]

- 当SPCR.TXMD位为0且SPCR2.SPPE位为1时串行传输结束。SPI检测到奇偶校验错误。

[Clearing condition]

- 在通过读取SPSR确认PERF标志为1后，将0写入PERF标志时。

UDRF标志（欠载错误标志）

UDRF标志指示发生了欠载错误。

[Setting condition]

- When the serial transfer begins while the SPCR.MSTR bit is 0 (slave mode), the SPCR.SPE bit is 1, and the transmission data is not prepared. The SPI detects an underrun error.

[Clearing condition]

- When 0 is written to the UDRF flag after the UDRF flag is confirmed to be 1 by a read of SPSR.

SPTEF flag (SPI Transmit Buffer Empty Flag)

The SPTEF flag indicates the status of the transmit buffer for the SPI Data Register (SPDR/SPDR_HA).

[Setting conditions]

- When condition 1. OR 2. is satisfied.

1. The SPCR.SPE bit is 0 (the SPI is initialized).
2. Transmit data was transferred from the transmit buffer to the shift register.

[Clearing condition]

- When data written to SPDR/SPDR_HA equals the number of frames set in the SPFC[1:0] bits in the SPI Data Control Register (SPDCR).

Data can only be written to SPDR/SPDR_HA when the SPTEF flag is 1. If data is written to the transmit buffer of SPDR/SPDR_HA when the SPTEF flag is 0, the data in the transmit buffer is not updated.

SPRF flag (SPI Receive Buffer Full Flag)

The SPRF flag indicates the status of the receive buffer for the SPI Data Register (SPDR/SPDR_HA).

[Setting condition]

- When a serial transfer ends while the communication operating mode select bit (TXMD) in the SPI Control Register (SPCR) is 0, the SPRF flag is 0, and the SPI transfers the receive data from the shift register to SPDR/SPDR_HA. However, when the OVRF flag is 1, the SPRF flag does not change from 0 into 1.

[Clearing condition]

- When received data is read from the SPDR/SPDR_HA.

38.2.5 SPI Data Register (SPDR/SPDR_HA)

Address(es): SPI0.SPDR 4007 2004h, SPI1.SPDR 4007 2104h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Address(es): SPI0.SPDR_HA 4007 2004h, SPI1.SPDR_HA 4007 2104h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SPDR/SPDR_HA is the interface with the buffers that hold data for transmission and reception by the SPI. When accessing this register in words (the SPLW bit is 1), access SPDR. When accessing it in halfwords (the SPLW bit is 0), access SPDR_HA.

[Setting condition]

- 当SPCR.MSTR位为0（从模式）时串行传输开始时，SPCR.SPE位为1，不准备传输数据。SPI检测到欠载错误。

[Clearing condition]

- 在通过读取SPSR确认UDRF标志为1后，将0写入UDRF标志时。

SPTEF标志（SPI发送缓冲区空标志）

SPTEF标志指示SPI数据寄存器(SPDRSPDR_HA)的发送缓冲区的状态。

[Setting conditions]

- 当条件1.OR2.满足时。

1. SPCR.SPE位为0（SPI已初始化）。
2. 发送数据从发送缓冲器传送到移位寄存器。

[Clearing condition]

- 当写入SPDR的数据SPDR_HA等于SPI数据中SPFC[1:0]位中设置的帧数时控制寄存器(SPDCR)。

只有当SPTEF标志为1时，才能将数据写入SPDRSPDR_HA。如果将数据写入SPDRSPDR_HA当SPTEF标志为0时，发送缓冲区中的数据不更新。

SPRF标志（SPI接收缓冲区满标志）

SPRF标志指示SPI数据寄存器(SPDRSPDR_HA)的接收缓冲区的状态。

[Setting condition]

- 当串行传输结束且SPI控制寄存器(SPCR)中的通信操作模式选择位(TXMD)为0时，SPRF标志为0，SPI将接收数据从移位寄存器传输到SPDRSPDR_HA。但是，当OVRF标志为1时，SPRF标志不会从0变为1。

[Clearing condition]

- 从SPDRSPDR_HA读取接收到的数据时。

38.2.5 SPI数据寄存器(SPDRSPDR_HA)

Address(es): SPI0.SPDR 4007 2004h, SPI1.SPDR 4007 2104h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Address(es): SPI0.SPDR_HA 4007 2004h, SPI1.SPDR_HA 4007 2104h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SPDRSPDR_HA是与保存数据以供SPI发送和接收的缓冲区的接口。以字访问该寄存器时（SPLW位为1），访问SPDR。当以半字访问时（SPLW位为0），访问SPDR_HA。

The transmit buffer (SPTX) and receive buffer (SPRX) are independent but are both mapped to SPDR/SPDR_HA. Figure 38.2 shows the configuration.

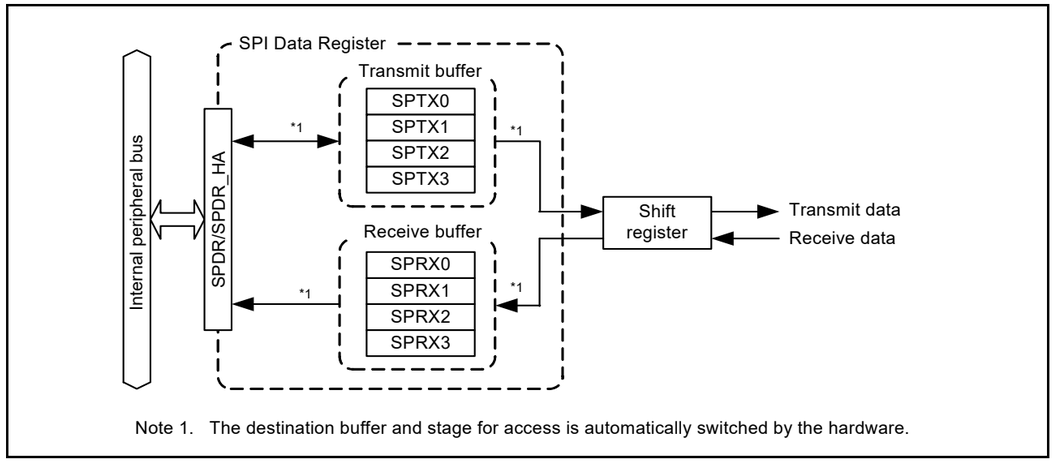


Figure 38.2 Configuration of SPDR/SPDR_HA

The transmit and receive buffers each have four stages. The number of stages to be used is selectable in the number of frames specification bits in the SPI Data Control Register (SPDCR.SPFC[1:0]). The eight stages of the buffer are all mapped to the single address of SPDR/SPDR_HA.

Data written to SPDR/SPDR_HA is written to a transmit-buffer stage (SPTXn) (n = 0 to 3) and then transmitted from the buffer. The receive buffer holds received data on completion of reception. The receive buffer is not updated if an overrun is generated.

Additionally, if the data length is other than 32 bits, bits not referred to in SPTXn (n = 0 to 3) are stored in the associated bits in SPRXn (n = 0 to 3). For example, if the data length is 9 bits, the received data is stored in the SPRXn[8:0] bits, and the SPTXn[31:9] bits are stored in the SPRXn[31:9] bits.

(1) Bus interface

SPDR/SPDR_HA is an interface with 32-bit wide transmit and receive buffers, each of which has four stages, for a total of 32 bytes. In other words, the 32 bytes are mapped to the 4-byte address space for SPDR/SPDR_HA. Additionally, the unit of access for SPDR/SPDR_HA is selected by the SPI word access/halfword access specification bit in the SPI Data Control Register (SPDCR.SPLW). Other case, make an access to SPDR with the access size specified by the SPI byte access bit in the SPI Data Control Register (SPDCR.SPBYT).

Flush transmission data at the LSB end of the register, and store received data at the LSB end.

This section describes the operations involved in writing to and reading from SPDR/SPDR_HA.

(a) Writing

Data written to SPDR/SPDR_HA is written to a transmit buffer (SPTXn). This is not affected by the value of the SPDCR.SPRDTD bit, unlike when reading from SPDR/SPDR_HA. The transmit buffer includes a transmit buffer write pointer that is automatically updated to reference the next stage each time data is written to SPDR/SPDR_HA.

Figure 38.3 shows the configuration of the bus interface with the transmit buffer when writing to SPDR.

发送缓冲区(SPTX)和接收缓冲区(SPRX)是独立的，但都映射到SPDRSPDR_HA。
图38.2显示了配置。

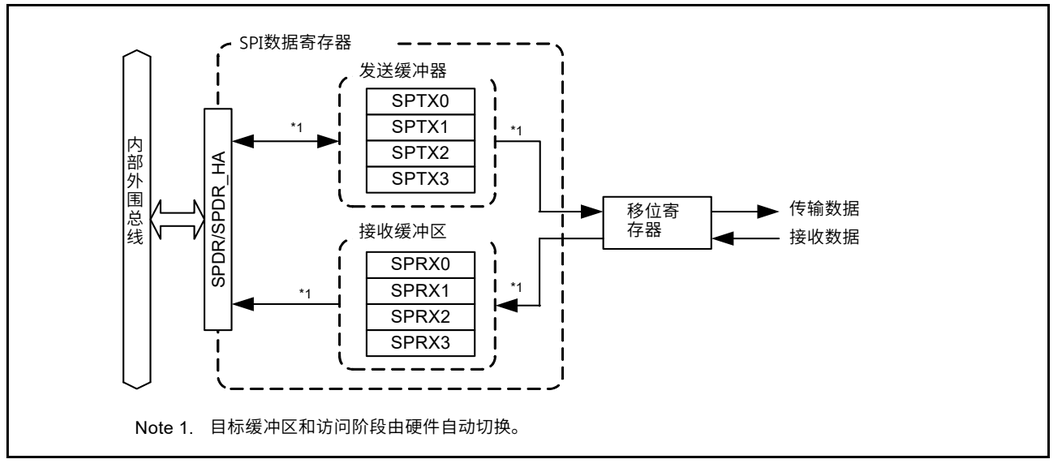


Figure 38.2 SPDRSPDR_HA的配置

发送和接收缓冲器各有四个阶段。要使用的级数可在SPI数据控制寄存器(SPDCR.SPFC[1:0])中的帧数规范位中选择。缓冲区的八个阶段都映射到SPDRSPDR_HA的单个地址。

写入SPDRSPDR_HA的数据被写入发送缓冲器级(SPTXn)（n=0到3），然后从缓冲器发送。接收缓冲器在接收完成时保存接收到的数据。如果产生溢出，接收缓冲区不会更新。

此外，如果数据长度不是32位，SPTXn(n=0到3)中未引用的位将存储在SPRXn(n=0到3)的相关位中。例如，如果数据长度为9位，则接收到的数据存储在SPRXn[8:0]位中，SPTXn[31:9]位存储在SPRXn[31:9]位中。

(1) 总线接口

SPDRSPDR_HA是一个具有32位宽的发送和接收缓冲区的接口，每个缓冲区有四个阶段，总共32个字节。换句话说，这32个字节映射到SPDRSPDR_HA的4字节地址空间。此外，SPDRSPDR_HA的访问单元由SPI数据控制寄存器(SPDCR.SPLW)中的SPI字访问半字访问规范位选择。其他情况下，使用SPI数据控制寄存器(SPDCR.SPBYT)中的SPI字节访问位指定的访问大小访问SPDR。

在寄存器的LSB端刷新发送数据，在LSB端存储接收到的数据。

本节介绍写入和读取SPDRSPDR_HA所涉及的操作。

(a) Writing

写入SPDRSPDR_HA的数据被写入发送缓冲器(SPTXn)。这不受价值的影响
SPDCR.SPRDTD位，与从SPDRSPDR_HA读取时不同。发送缓冲区包括一个发送缓冲区写指针，每次将数据写入SPDRSPDR_HA时，该写指针会自动更新以引用下一阶段。

图38.3显示了写入SPDR时带有发送缓冲器的总线接口的配置。

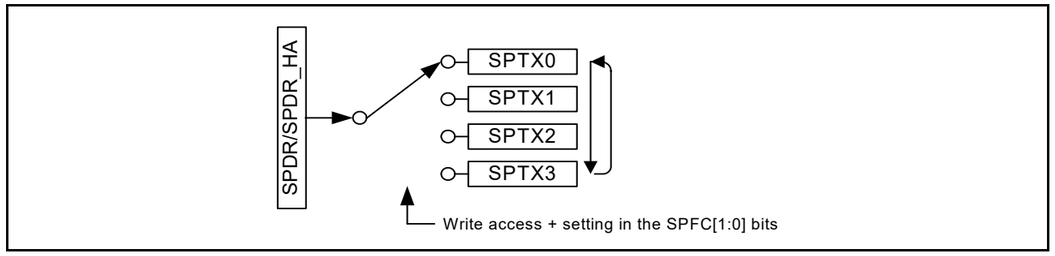


Figure 38.3 Configuration of SPDR/SPDR_HA for write access

The sequence for switching the transmit buffer write pointer differs with the setting of the number of frames specification bits in the SPI Data Control Register (SPDCR.SPFC[1:0]). The relationship of the SPFC[1:0] setting and the sequence of pointer switching among SPTX0 to SPTX3 is as follows:

- When SPFC[1:0] = 00b: SPTX0 → SPTX0 → SPTX0 → …
- When SPFC[1:0] = 01b: SPTX0 → SPTX1 → SPTX0 → SPTX1 → …
- When SPFC[1:0] = 10b: SPTX0 → SPTX1 → SPTX2 → SPTX0 → SPTX1 → …
- When SPFC[1:0] = 11b: SPTX0 → SPTX1 → SPTX2 → SPTX3 → SPTX0 → SPTX1 → …

When 1 is written to the SPI function enable bit in the SPI Control Register (SPCR.SPE) while the value of the bit is 0, SPTX0 is the destination the next time writing proceeds.

When writing to the transmit buffer (SPTXn) after generating the transmit buffer empty interrupt (when SPSR.SPTEF is 1), write the number of frames set in SPFC[1:0] in the SPI Data Control Register (SPDCR). Even when the specified number of frames is written to the transmit buffer (SPTXn), the value of the buffer is not updated after completion of the writing and before the next transmit buffer empty interrupt is generated (when SPTEF is 0).

(b) Reading

SPDR/SPDR_HA can be accessed to read the value of a receive buffer (SPRXn) or a transmit buffer (SPTXn). The setting in the SPI receive/transmit data select bit in the SPI Data Control Register (SPDCR.SPRDTD) selects whether reading is of the receive or transmit buffer. The sequence of reading the SPDR/SPDR_HA register is controlled by the independent receive buffer and transmit buffer read pointers.

Figure 38.4 shows the configuration of the bus interface with the receive and transmit buffers for a read from SPDR/SPDR_HA.

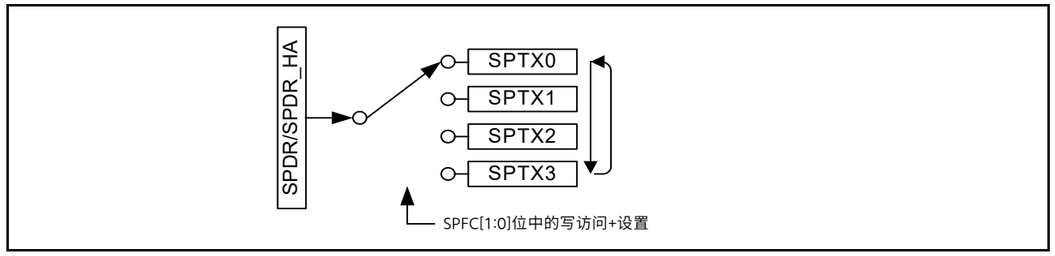


Figure 38.3 为写访问配置SPDRSPDR_HA

发送缓冲区写指针的切换顺序因SPI数据控制寄存器(SPDCR.SPFC[1:0])中帧数规范位的设置而异。SPFC[1:0]设置与SPTX0到SPTX3指针切换顺序的关系如下：

- When SPFC[1:0] = 00b: SPTX0 → SPTX0 → SPTX0 → …
- When SPFC[1:0] = 01b: SPTX0 → SPTX1 → SPTX0 → SPTX1 → …
- When SPFC[1:0] = 10b: SPTX0 → SPTX1 → SPTX2 → SPTX0 → SPTX1 → …
- When SPFC[1:0] = 11b: SPTX0 → SPTX1 → SPTX2 → SPTX3 → SPTX0 → SPTX1 → …

当SPI控制寄存器(SPCR.SPE)中的SPI功能使能位写入1而该位的值为0时，
SPTX0是下一次写入的目的地。

在产生发送缓冲区空中断后写入发送缓冲区(SPTXn)时（当SPSR.SPTEF为1时），将SPFC[1:0]中设置的帧数写入SPI数据控制寄存器(SPDCR)。即使将指定数量的帧写入发送缓冲区(SPTXn)，缓冲区的值在写入完成后和下一个发送缓冲区空中断产生之前（SPTEF为0时）也不会更新。

(b) Reading

SPDR可以访问SPDR_HA以读取接收缓冲区(SPRXn)或发送缓冲区(SPTXn)的值。SPI数据控制寄存器(SPDCR.SPRDTD)中SPI接收发送数据选择位的设置选择读取接收缓冲区还是发送缓冲区。读取SPDRSPDR_HA寄存器的顺序由独立的接收缓冲区和发送缓冲区读取指针控制。

图38.4显示了带有用于读取的接收和发送缓冲区的总线接口的配置
SPDR/SPDR_HA.

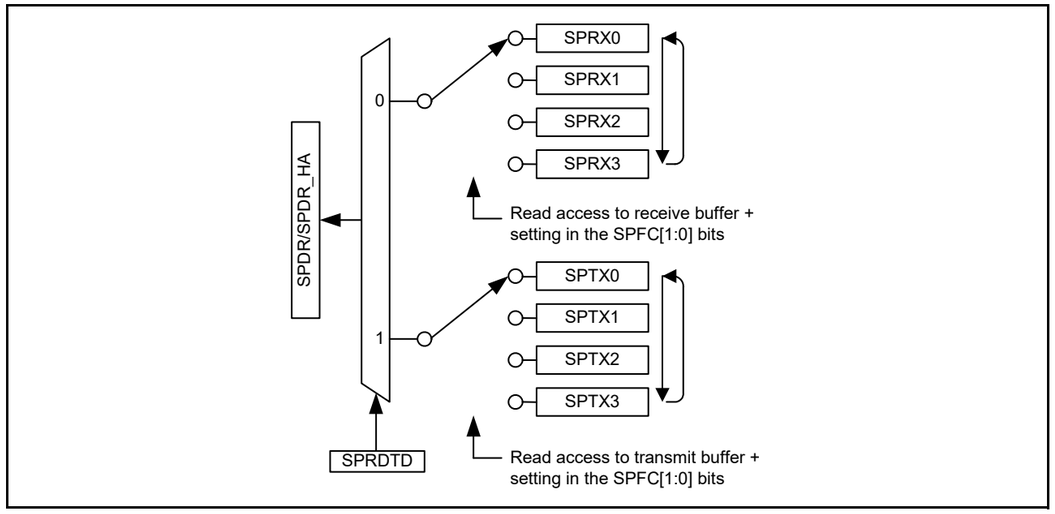


Figure 38.4 Configuration of SPDR/SPDR_HA for read access

Reading the receive buffer switches the receive buffer read pointer to the next buffer automatically. The switching sequence for the receive buffer read pointer is the same as that for the transmit buffer write pointer. However, when 1 is written to the SPI function enable bit in the SPI Control Register (SPCR.SPE) while the value of the bit is 1, SPRX0 is referenced by the buffer read pointer the next time reading proceeds.

The transmit buffer read pointer is updated when writing to SPDR/SPDR_HA, and not updated when reading from the transmit buffer. When reading from the transmit buffer, the value most recently written to SPDR/SPDR_HA is read. However, after generation of the transmit buffer empty interrupt, the values read from the transmit buffer are all 0s in the interval after completion of writing the number of frames of data specified in the SPDCR.SPFC[1:0] bits and before generation of the next buffer empty interrupt (when SPTEF is 0).

38.2.6 SPI Sequence Control Register (SPSCR)

Address(es): SPI0.SPSCR 4007 2008h, SPI1.SPSCR 4007 2108h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	SPSLN[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	SPSLN[2:0]	SPI Sequence Length Specification	b2 b0: Sequence Length — Referenced SPCMD0 to SPCMD7 (No.) 0 0 0: 1 — 0→0→… 0 0 1: 2 — 0→1→0→… 0 1 0: 3 — 0→1→2→0→… 0 1 1: 4 — 0→1→2→3→0→… 1 0 0: 5 — 0→1→2→3→4→0→… 1 0 1: 6 — 0→1→2→3→4→5→0→… 1 1 0: 7 — 0→1→2→3→4→5→6→0→… 1 1 1: 8 — 0→1→2→3→4→5→6→7→0→… The sequence length that is set in these bits determines the order in which the SPCMD0 to SPCMD07 registers are referenced. The setting defines the relationship between the sequence length and the SPCMD0 to SPCMD7 registers referenced by the SPI. In slave mode, the SPI references SPCMD0.	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

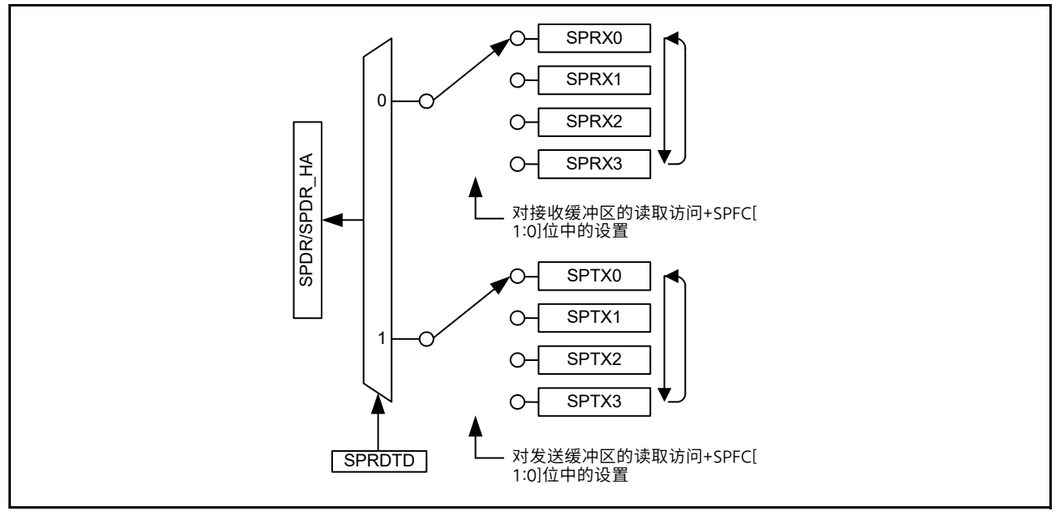


Figure 38.4 为读取访问配置SPDRSPDR_HA

读取接收缓冲区会自动将接收缓冲区读取指针切换到下一个缓冲区。接收缓冲区读指针的切换顺序与发送缓冲区写指针的切换顺序相同。但是，当1写入SPI控制寄存器(SPCR.SPE)中的SPI功能使能位且该位的值为1时，下次读取继续时，缓冲区读取指针将引用SPRX0。

发送缓冲区读指针在写入SPDRSPDR_HA时更新，而在从发送缓冲区读取时不更新。从发送缓冲区读取时，会读取最近写入SPDRSPDR_HA的值。但是，在产生发送缓冲区空中断后，从发送缓冲区读取的值在完成写入SPDCR.SPFC[1:0]位中指定的数据帧数之后和产生之前的间隔内全为0。下一个缓冲区空中断（当SPTEF为0时）。

38.2.6 SPI序列控制寄存器(SPSCR)

Address(es): SPI0.SPSCR 4007 2008h, SPI1.SPSCR 4007 2108h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	SPSLN[2:0]		
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b2 to b0	SPSLN[2:0]	SPI序列长度 Specification	b2b0参考SPCMD0到SPCMD7的序列长度（编号）000：10→0→…001：20→1→0→…010：30→1→2→0→…011：40→1→2→3→0→…100：50→1→2→3→4→0→…101：60→1→2→3→4→5→0→…110:70→1→2→3→4→5→6→0→…111:80→1→2→3→4→5→6→7→0→…顺序在这些位中设置的长度决定了引用SPCMD0到SPCMD07寄存器的顺序。该设置定义了序列长度与SPI引用的SPCMD0到SPCMD7寄存器之间的关系。在从机模式下，SPI参考SPCMD0。	R/W
b7 to b3	—	Reserved	这些位被读取为0。写入值应为0。	R/W

SPSCR specifies the sequence length when the SPI operates in master mode. Before changing the SPSCR.SPSLN[2:0] bits while both the SPCR.MSTR and SPCR.SPE bits are 1, always check that the SPSR.IDLNF flag is 0.

SPSLN[2:0] bits (SPI Sequence Length Specification)

The SPSLN[2:0] bits specify the sequence length when the SPI in master mode performs sequential operations. The SPI in master mode changes the SPCMD0 to SPCMD7 registers to be referenced, and the order in which they are referenced is based on this sequence length setting. In slave mode, SPCMD0 is referenced.

38.2.7 SPI Sequence Status Register (SPSSR)

Address(es): SPI0.SPSSR 4007 2009h, SPI1.SPSSR 4007 2109h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	SPECM[2:0]			—	SPCP[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	SPCP[2:0]	SPI Command Pointer	b2 b0 0 0 0: SPCMD0 0 0 1: SPCMD1 0 1 0: SPCMD2 0 1 1: SPCMD3 1 0 0: SPCMD4 1 0 1: SPCMD5 1 1 0: SPCMD6 1 1 1: SPCMD7.	R
b3	—	Reserved	This bit is read as 0.	R
b6 to b4	SPECM[2:0]	SPI Error Command	b6 b4 0 0 0: SPCMD0 0 0 1: SPCMD1 0 1 0: SPCMD2 0 1 1: SPCMD3 1 0 0: SPCMD4 1 0 1: SPCMD5 1 1 0: SPCMD6 1 1 1: SPCMD7.	R
b7	—	Reserved	This bit is read as 0.	R

SPSSR indicates the sequence control status when the SPI operates in master mode. Any writes to SPSSR are ignored.

SPCP[2:0] bits (SPI Command Pointer)

The SPCP[2:0] bits indicate the SPCMDm register that is referenced to by the pointer during sequence control by the SPI. For the SPI sequence control, see section 38.3.10.1, Master mode operation.

SPECM[2:0] bits (SPI Error Command)

The SPECM[2:0] bits indicate the SPCMDm register that is specified in the SPCP[2:0] bits when an error is detected during sequence control by the SPI. The SPI updates the SPECM[2:0] bits only when an error is detected. If both the SPSR.OVRF and SPSR.MODF flags are 0 and there is no error, the values of the SPECM[2:0] bits have no meaning.

For the SPI error detection function, see section 38.3.8, Error Detection. For the SPI sequence control, see section 38.3.10.1, Master mode operation.

SPSCR指定SPI在主模式下工作时的序列长度。在SPCR.MSTR和SPCR.SPE位均为1时更改SPSCR.SPSLN[2:0]位之前，请始终检查SPSR.IDLNF标志是否为0。

SPSLN[2:0]位（SPI序列长度规范）

SPSLN[2:0]位指定SPI在主模式下执行顺序操作时的序列长度。主机模式下的SPI将SPCMD0到SPCMD7寄存器更改为被引用，它们被引用的顺序基于此序列长度设置。在从模式下，以SPMD0为参考。

38.2.7 SPI序列状态寄存器(SPSSR)

Address(es): SPI0.SPSSR 4007 2009h, SPI1.SPSSR 4007 2109h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	SPECM[2:0]			—	SPCP[2:0]		
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b2 to b0	SPCP[2:0]	SPI命令指针	b2 b0 0 0 0: SPCMD0 0 0 1: SPCMD1 0 1 0: SPCMD2 0 1 1: SPCMD3 1 0 0: SPCMD4 1 0 1: SPCMD5 1 1 0: SPCMD6 1 1 1: SPCMD7.	R
b3	—	Reserved	该位读为0。	R
b6 to b4	SPECM[2:0]	SPI错误命令	b6 b4 0 0 0: SPCMD0 0 0 1: SPCMD1 0 1 0: SPCMD2 0 1 1: SPCMD3 1 0 0: SPCMD4 1 0 1: SPCMD5 1 1 0: SPCMD6 1 1 1: SPCMD7.	R
b7	—	Reserved	该位读为0。	R

SPSSR指示SPI在主模式下工作时的序列控制状态。对SPSSR的任何写入都将被忽略。

SPCP[2:0]位（SPI命令指针）

SPCP[2:0]位指示在序列控制期间由指针引用的SPCMDm寄存器
SPI。对于SPI序列控制，请参见第38.3.10.1节，主模式操作。

SPECM[2:0]位（SPI错误命令）

SPECM[2:0]位指示在SPI序列控制期间检测到错误时在SPCP[2:0]位中指定的SPCMDm寄存器。SPI仅在检测到错误时更新SPECM[2:0]位。如果SPSR.OVRF和SPSR.MODF标志均为0且没有错误，则SPECM[2:0]位的值没有意义。

关于SPI错误检测功能，请参见第38.3.8节，错误检测。对于SPI序列控制，请参见第38.3.10.1节，主模式操作。

38.2.8 SPI Bit Rate Register (SPBR)

Address(es): SPI0.SPBR 4007 200Ah, SPI1.SPBR 4007 210Ah

	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	1	1	1	1	1	1	1	1

SPBR sets the bit rate in master mode. If the contents of SPBR are changed while both the SPCR.MSTR and SPCR.SPE bits are 1, do not perform subsequent operations.

When the SPI is used in slave mode, the bit rate depends on the bit rate of the input clock regardless of the settings in SPBR and the SPCMDm.BRDV[1:0] bits (bit rate division setting). Use bit rates that satisfy the electrical characteristics.

The bit rate is determined by combinations of the SPBR and SPCMDm.BRDV[1:0] settings. The equation for calculating the bit rate is as follows:

$$\text{Bit rate} = \frac{f(\text{PCLKA})}{2 \times (n + 1) \times 2^N}$$

In the equation, n denotes an SPBR setting (0, 1, 2, …, 255), and N denotes a BRDV[1:0] setting (0, 1, 2, 3).

Table 38.3 lists examples of the relationship among the SPBR settings, the BRDV[1:0] settings, and bit rates.

Table 38.3 Relationship among SPBR settings, BRDV[1:0] settings, and bit rates

SPBR (n)	BRDV[1:0] bits (N)	Division ratio	Bit rate							
			PCLKA = 32 MHz	PCLKA = 36 MHz	PCLKA = 40 MHz	PCLKA = 50 MHz	PCLKA = 60 MHz	PCLKA = 80 MHz	PCLKA = 100 MHz	PCLKA = 120 MHz
0	0	2	16.0 Mbps	18.0 Mbps	20.0 Mbps	25.0 Mbps	30.0 Mbps	Not supported		
1	0	4	8.00 Mbps	9.00 Mbps	10.0 Mbps	12.5 Mbps	15.0 Mbps	20.0 Mbps	25.0 Mbps	30.0 Mbps
2	0	6	5.33 Mbps	6.00 Mbps	6.67 Mbps	8.33 Mbps	10.0 Mbps	13.3 Mbps	16.7 Mbps	20.0 Mbps
3	0	8	4.00 Mbps	4.50 Mbps	5.00 Mbps	6.25 Mbps	7.50Mbps	10.0 Mbps	12.5 Mbps	15.0 Mbps
4	0	10	3.20 Mbps	3.60 Mbps	4.00 Mbps	5.00 Mbps	6.00 Mbps	8.00 Mbps	10.0 Mbps	12.0 Mbps
5	0	12	2.67 Mbps	3.00 Mbps	3.33 Mbps	4.16 Mbps	5.00 Mbps	6.67 Mbps	8.33 Mbps	10.0 Mbps
5	1	24	1.33 Mbps	1.50 Mbps	1.67 Mbps	2.08 Mbps	2.50 Mbps	3.33 Mbps	4.17 Mbps	5.00 Mbps
5	2	48	667 kbps	750 kbps	833 kbps	1.04 Mbps	1.25 Mbps	1.67 Mbps	2.08 Mbps	2.50 Mbps
5	3	96	333 kbps	375 kbps	417 kbps	521 kbps	625 kbps	833 kbps	1.04 Mbps	1.25 Mbps
255	3	4096	7.81 kbps	8.80 kbps	9.78 kbps	12.2 kbps	14.6 kbps	19.5 kbps	24.4 kbps	29.3 kbps

38.2.8 SPI比特率寄存器（SPBR）

Address(es): SPI0.SPBR 4007 200Ah, SPI1.SPBR 4007 210Ah

	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	1	1	1	1	1	1	1	1

SPBR在主模式下设置比特率。如果在SPCR.MSTR和SPCR.SPE位都为1时SPBR的内容发生了变化，则不要执行后续操作。

当SPI在从机模式下使用时，比特率取决于输入时钟的比特率，与SPBR和SPCMDm.BRDV[1:0]位（比特率划分设置）。使用满足电气特性的比特率。

比特率由SPBR和SPMDm.BRDV[1:0]设置的组合决定。比特率的计算公式如下：

$$\text{比特率} = \frac{f(\text{PCLKA})}{2 \times (n + 1) \times 2^N}$$

在等式中，n表示SPBR设置(0 1 2 … 255)，N表示BRDV[1:0]设置(0 1 2 3)。

表38.3列出了SPBR设置、BRDV[1:0]设置和比特率之间的关系示例。

Table 38.3 SPBR设置、BRDV[1:0]设置和比特率之间的关系

SPBR (n)	BRDV[1:0] bits (N)	分工比	比特率							
			PCLKA = 32 MHz	PCLKA = 36 MHz	PCLKA = 40 MHz	PCLKA = 50 MHz	PCLKA = 60 MHz	PCLKA = 80 MHz	PCLKA = 100 MHz	PCLKA = 120 MHz
0	0	2	16.0 Mbps	18.0 Mbps	20.0 Mbps	25.0 Mbps	30.0 Mbps	不支持		
1	0	4	8.00 Mbps	9.00 Mbps	10.0 Mbps	12.5 Mbps	15.0 Mbps	20.0 Mbps	25.0 Mbps	30.0 Mbps
2	0	6	5.33 Mbps	6.00 Mbps	6.67 Mbps	8.33 Mbps	10.0 Mbps	13.3 Mbps	16.7 Mbps	20.0 Mbps
3	0	8	4.00 Mbps	4.50 Mbps	5.00 Mbps	6.25 Mbps	7.50Mbps	10.0 Mbps	12.5 Mbps	15.0 Mbps
4	0	10	3.20 Mbps	3.60 Mbps	4.00 Mbps	5.00 Mbps	6.00 Mbps	8.00 Mbps	10.0 Mbps	12.0 Mbps
5	0	12	2.67 Mbps	3.00 Mbps	3.33 Mbps	4.16 Mbps	5.00 Mbps	6.67 Mbps	8.33 Mbps	10.0 Mbps
5	1	24	1.33 Mbps	1.50 Mbps	1.67 Mbps	2.08 Mbps	2.50 Mbps	3.33 Mbps	4.17 Mbps	5.00 Mbps
5	2	48	667 kbps	750 kbps	833 kbps	1.04 Mbps	1.25 Mbps	1.67 Mbps	2.08 Mbps	2.50 Mbps
5	3	96	333 kbps	375 kbps	417 kbps	521 kbps	625 kbps	833 kbps	1.04 Mbps	1.25 Mbps
255	3	4096	7.81 kbps	8.80 kbps	9.78 kbps	12.2 kbps	14.6 kbps	19.5 kbps	24.4 kbps	29.3 kbps

38.2.9 SPI Data Control Register (SPDCR)

Address(es): SPI0.SPDCR 4007 200Bh, SPI1.SPDCR 4007 210Bh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	SPBYT	SPLW	SPRDTD	—	—	SPFC[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	SPFC[1:0]	Number of Frames Specification	b1 b0 0 0: 1 frame 0 1: 2 frames 1 0: 3 frames 1 1: 4 frames.	R/W
b3, b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	SPRDTD	SPI Receive/Transmit Data Select	0: Read SPDR/SPDR_HA values from receive buffer 1: Read SPDR/SPDR_HA values from transmit buffer, but only if the transmit buffer is empty.	R/W
b5	SPLW	SPI Word Access/Halfword Access Specification	0: Set SPDR_HA to valid for halfword access 1: Set SPDR to valid for word access.	R/W
b6	SPBYT	SPI Byte Access Specification	0: SPDR is accessed in halfword or word (SPLW is valid) 1: SPDR is accessed in byte (SPLW is invalid).	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Up to four frames can be transmitted or received in one round of transmission or reception. The amount of data in each transfer is controlled by the combination of the SPCMDm.SPB[3:0] bits, the SPSCR.SPSLN[2:0] bits, and the SPDCR.SPFC[1:0] bits.

When changing the SPDCR.SPFC[1:0] bits while the SPCR.SPE bit is 1, always check that the SPSR.IDLNF flag is 0.

SPFC[1:0] bits (Number of Frames Specification)

The SPFC[1:0] bits specify the number of frames that can be stored in SPDR/SPDR_HA per transfer activation. Up to four frames can be transmitted or received in one round of transmission or reception.

When the number of transmission data frames specified in the SPFC[1:0] bits is written to the SPDR/SPDR_HA register, SPI clears the SPSR.SPTEF flag to 0 and begins transmitting. After that, when the number of transmission data frames specified in the SPFC[1:0] bits is transmitted to the shift register, the SPI generates the transmit buffer empty interrupt (SPSR.SPTEF sets to 1).

When the number of data frames specified in the SPFC[1:0] bits is received, the SPI generates the receive buffer full interrupt (SPSR.SPRF sets to 1).

Table 38.4 Settable combinations of the SPSLN[2:0] and SPFC[1:0] bits (1 of 2)

Setting	SPSLN[2:0]	SPFC[1:0]	Number of frames in a single sequence	Number of frames at which transmission or receive buffer is filled
1-1	000b	00b	1	1
1-2	000b	01b	2	2
1-3	000b	10b	3	3
1-4	000b	11b	4	4
2-1	001b	01b	2	2
2-2	001b	11b	4	4
3	010b	10b	3	3
4	011b	11b	4	4
5	100b	00b	5	1

38.2.9 SPI数据控制寄存器(SPDCR)

Address(es): SPI0.SPDCR 4007 200Bh, SPI1.SPDCR 4007 210Bh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	SPBYT	SPLW	SPRDTD	—	—	SPFC[1:0]	
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b1, b0	SPFC[1:0]	帧数 Specification	b1b000：1帧0 1：2帧10：3 帧11：4帧。	R/W
b3, b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b4	SPRDTD	SPI接收发送数据 Select	0：从接收缓冲区读取SPDRSPDR_HA值1：从发送缓冲区读取SPDRSPDR_HA值，但前提是发送缓冲区为空。	R/W
b5	SPLW	SPI字访问半字 访问规范	0：将SPDR_HA设置为对半字访问有效1：将SPDR设置为对字访问有效。	R/W
b6	SPBYT	SPI字节访问规范	0：SPDR按半字或字访问（SPLW有效）1：SPDR按字节访问（SPLW无效）。	R/W
b7	—	Reserved	该位读取为0。写入值应为0。	R/W

在一轮发送或接收中最多可以发送或接收四帧。每次传输中的数据量由SPCMDm.SPB[3:0]位、SPSCR.SPSLN[2:0]位和SPDCR.SPFC[1:0]位的组合控制。

在SPCR.SPE位为1时更改SPDCR.SPFC[1:0]位时，请始终检查SPSR.IDLNF标志是否为0。

SPFC[1:0]位（帧数规范）

SPFC[1:0]位指定每次传输激活时可以存储在SPDRSPDR_HA中的帧数。在一轮发送或接收中最多可以发送或接收四帧。

当SPFC[1:0]位中指定的发送数据帧数写入SPDRSPDR_HA寄存器时，SPI将SPSR.SPTEF标志清零并开始发送。之后，当SPFC[1:0]位中指定的发送数据帧数被发送到移位寄存器时，SPI产生发送缓冲区空中断（SPSR.SPTEF设置为1）。

当接收到SPFC[1:0]位中指定的数据帧数时，SPI产生接收缓冲区满中断（SPSR.SPRF设置为1）。

Table 38.4 SPSLN[2:0]和SPFC[1:0]位的可设置组合（2个中的1个）

Setting	SPSLN[2:0]	SPFC[1:0]	单个序列中的帧数	填充传输或接收缓冲区的帧数
1-1	000b	00b	1	1
1-2	000b	01b	2	2
1-3	000b	10b	3	3
1-4	000b	11b	4	4
2-1	001b	01b	2	2
2-2	001b	11b	4	4
3	010b	10b	3	3
4	011b	11b	4	4
5	100b	00b	5	1

Table 38.4 Settable combinations of the SPSLN[2:0] and SPFC[1:0] bits (2 of 2)

Setting	SPSLN[2:0]	SPFC[1:0]	Number of frames in a single sequence	Number of frames at which transmission or receive buffer is filled
6	101b	00b	6	1
7	110b	00b	7	1
8	111b	00b	8	1

SPRDTD bit (SPI Receive/Transmit Data Select)

The SPRDTD bit selects whether the SPDR/SPDR_HA reads values from the receive buffer or from the transmit buffer. If reading is from the transmit buffer, the value written to SPDR/SPDR_HA register immediately beforehand is read. When reading the transmit buffer, do so before writing of the number of frames set in the SPFC[1:0] bits is finished and after generation of the transmit buffer empty interrupt (when SPSR.SPTEF is 1).

For details, see section 38.2.5, SPI Data Register (SPDR/SPDR_HA).

SPLW bit (SPI Word Access/Halfword Access Specification)

The SPLW bit specifies the access width for SPDR. Access to SPDR_HA in halfwords is valid when the SPLW bit is 0 and access to SPDR in words is valid when the SPLW bit is 1. Also, when this bit is 0, set the SPCMDm.SPB[3:0] bits (SPI data length setting) from 8 to 16 bits. Do not perform any operations when 20, 24, or 32 bits is specified.

SPBYT bit (SPI Byte Access Specification)

This bit is used to set the data width of access to the SPI Data Register (SPDR). When SPBYT = 0, use word or half word access to SPDR. When SPBYT = 1 (in that case, SPLW is invalid), use byte access to SPDR.

When SPBYT = 1, set the SPI data length bits (SPB[3:0]) in the SPI Command Register n (SPCMDn) to 0 bits. If SPB[3:0] are set to 9 to 16, 20, 24, or 32 bit, subsequent operation is not guaranteed.

38.2.10 SPI Clock Delay Register (SPCKD)

Address(es): SPI0.SPCKD 4007 200Ch, SPI1.SPCKD 4007 210Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	SCKDL[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	SCKDL[2:0]	RSPCK Delay Setting	b2 b0 0 0 0: 1 RSPCK 0 0 1: 2 RSPCK 0 1 0: 3 RSPCK 0 1 1: 4 RSPCK 1 0 0: 5 RSPCK 1 0 1: 6 RSPCK 1 1 0: 7 RSPCK 1 1 1: 8 RSPCK.	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

SPCKD specifies the RSPCK delay, the period from the beginning of SSLni signal assertion to RSPCK oscillation, when the SPCMDm.SCKDEN bit is 1. If the contents of SPCKD are changed while both the SPCR.MSTR and SPCR.SPE bits are 1, do not perform subsequent operations.

SCKDL[2:0] bits (RSPCK Delay Setting)

The SCKDL[2:0] bits specify an RSPCK delay value when the SPCMDm.SCKDEN bit is 1. When using the SPI in slave mode, set the SCKDL[2:0] bits to 000b.

Table 38.4 SPSLN[2:0]和SPFC[1:0]位的可设置组合（2个中的2个）

Setting	SPSLN[2:0]	SPFC[1:0]	单个序列中的帧数	填充传输或接收缓冲区的帧数
6	101b	00b	6	1
7	110b	00b	7	1
8	111b	00b	8	1

SPRDTD位（SPI接收发送数据选择）

SPRDTD位选择SPDRSPDR_HA是从接收缓冲区还是从发送缓冲区读取值。如果从发送缓冲区读取，则读取之前立即写入SPDRSPDR_HA寄存器的值。

读取发送缓冲区时，在SPFC[1:0]位中设置的帧数写入完成之前和发送缓冲区空中断产生之后（当SPSR.SPTEF为1时）执行此操作。

有关详细信息，请参阅第38.2.5节，SPI数据寄存器(SPDRSPDR_HA)。

SPLW位（SPI字访问半字访问规范）

SPLW位指定SPDR的访问宽度。当SPLW位为0时，以半字访问SPDR_HA有效，当SPLW位为1时，以字访问SPDR有效。此外，当该位为0时，设置SPCMDm.SPB[3:0]位（SPI数据长度设置）从8到16位。指定20、24或32位时不要执行任何操作。

SPBYT位（SPI字节访问规范）

该位用于设置访问SPI数据寄存器(SPDR)的数据宽度。当SPBYT=0时，使用字或半字访问SPDR。当SPBYT=1时（在这种情况下，SPLW无效），使用字节访问SPDR。

当SPBYT=1时，将SPI命令寄存器n(SPCMDn)中的SPI数据长度位(SPB[3:0])设置为0位。如果SPB[3:0]设置为9至16、20、24或32位，不保证后续操作。

38.2.10 SPI时钟延迟寄存器(SPCKD)

Address(es): SPI0.SPCKD 4007 200Ch, SPI1.SPCKD 4007 210Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	SCKDL[2:0]		
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b2 to b0	SCKDL[2:0]	RSPCK延迟设置	b2 b0 0 0 0: 1 RSPCK 0 0 1: 2 RSPCK 0 1 0: 3 RSPCK 0 1 1: 4 RSPCK 1 0 0: 5 RSPCK 1 0 1: 6 RSPCK 1 1 0: 7 RSPCK 1 1 1: 8 RSPCK.	R/W
b7 to b3	—	Reserved	这些位被读取为0。写入值应为0。	R/W

SPCKD指定RSPCK延迟，即从SSLni信号断言开始到RSPCK振荡的周期，当SPCMDm.SCKDEN位为1时。如果SPCKD的内容在SPCR.MSTR和SPCR.SPE位都为1时改变，请不进行后续操作。

SCKDL[2:0]位（RSPCK延迟设置）

当SPCMDm.SCKDEN位为1时，SCKDL[2:0]位指定RSPCK延迟值。在从机模式下使用SPI时，将SCKDL[2:0]位设置为000b。

38.2.11 SPI Slave Select Negation Delay Register (SSLND)

Address(es): SPI0.SSLND 4007 200Dh, SPI1.SSLND 4007 210Dh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	SLNDL[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	SLNDL[2:0]	SSL Negation Delay Setting	b2 b0 0 0 0: 1 RSPCK 0 0 1: 2 RSPCK 0 1 0: 3 RSPCK 0 1 1: 4 RSPCK 1 0 0: 5 RSPCK 1 0 1: 6 RSPCK 1 1 0: 7 RSPCK 1 1 1: 8 RSPCK.	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

SSLND specifies the SSL negation delay, the period from the transmission of a final RSPCK edge to the negation of the SSLni signal during a serial transfer by the SPI in master mode. If the contents of SSLND are changed while both the SPCR.MSTR and SPCR.SPE bits are 1, do not perform subsequent operations.

SLNDL[2:0] bits (SSL Negation Delay Setting)

The SLNDL[2:0] bits specify an SSL negation delay value when the SPI is in master mode. When using the SPI in slave mode, set the SLNDL[2:0] bits to 000b.

38.2.12 SPI Next-Access Delay Register (SPND)

Address(es): SPI0.SPND 4007 200Eh, SPI1.SPND 4007 210Eh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	SPNDL[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	SPNDL[2:0]	SPI Next-Access Delay Setting	b2 b0 0 0 0: 1 RSPCK + 2 PCLKA 0 0 1: 2 RSPCK + 2 PCLKA 0 1 0: 3 RSPCK + 2 PCLKA 0 1 1: 4 RSPCK + 2 PCLKA 1 0 0: 5 RSPCK + 2 PCLKA 1 0 1: 6 RSPCK + 2 PCLKA 1 1 0: 7 RSPCK + 2 PCLKA 1 1 1: 8 RSPCK + 2 PCLKA.	R/W
b7 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

SPND specifies the next-access delay, the non-active period of the SSLni signal after termination of a serial transfer, when the SPCMDm.SPNDEN bit is 1. If the contents of SPND are changed while both the SPCR.MSTR and SPCR.SPE bits are 1, do not perform subsequent operations.

SPNDL[2:0] bits (SPI Next-Access Delay Setting)

The SPNDL[2:0] bits specify a next-access delay when the SPCMDm.SPNDEN bit is 1. When using the SPI in slave mode, set the SPNDL[2:0] bits to 000b.

38.2.11 SPI从机选择否定延迟寄存器(SSLND)

Address(es): SPI0.SSLND 4007 200Dh, SPI1.SSLND 4007 210Dh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	SLNDL[2:0]		
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b2 to b0	SLNDL[2:0]	SSL否定延迟设置	b2 b0 0 0 0: 1 RSPCK 0 0 1: 2 RSPCK 0 1 0: 3 RSPCK 0 1 1: 4 RSPCK 1 0 0: 5 RSPCK 1 0 1: 6 RSPCK 1 1 0: 7 RSPCK 1 1 1: 8 RSPCK.	R/W
b7 to b3	—	Reserved	这些位被读取为0。写入值应为0。	R/W

SSLND指定SSL否定延迟，从传输最终RSPCK边缘到否定
SPI在主模式下进行串行传输期间的SSLni信号。如果SSLND的内容发生更改，而
SPCR.MSTR和SPCR.SPE位为1，不执行后续操作。

SLNDL[2:0]位（SSL否定延迟设置）

当SPI处于主模式时，SLNDL[2:0]位指定SSL否定延迟值。在从机模式下使用SPI时，将SLNDL[2:0]位设置为000b。

38.2.12 SPI下一次访问延迟寄存器(SPND)

Address(es): SPI0.SPND 4007 200Eh, SPI1.SPND 4007 210Eh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	SPNDL[2:0]		
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b2 to b0	SPNDL[2:0]	SPI下一次访问延迟设置	b2 b0 0 0 0: 1 RSPCK + 2 PCLKA 0 0 1: 2 RSPCK + 2 PCLKA 0 1 0: 3 RSPCK + 2 PCLKA 0 1 1: 4 RSPCK + 2 PCLKA 1 0 0: 5 RSPCK + 2 PCLKA 1 0 1: 6 RSPCK + 2 PCLKA 1 1 0: 7 RSPCK + 2 PCLKA 1 1 1: 8 RSPCK + 2 PCLKA.	R/W
b7 to b3	—	Reserved	这些位被读取为0。写入值应为0。	R/W

当SPCMDm.SPNDEN位为1时，SPND指定下一次访问延迟，即串行传输终止后SSLni信号的非活动周期。如果在SPCR.MSTR和SPCR.SPE都更改了SPND的内容时位为1，不执行后续操作。

SPNDL[2:0]位（SPI下一次访问延迟设置）

当SPMDm.SPNDEN位为1时，SPNDL[2:0]位指定下一次访问延迟。在从机模式下使用SPI时，将SPNDL[2:0]位设置为000b。

38.2.13 SPI Control Register 2 (SPCR2)

Address(es): SPI0.SPCR2 4007 200Fh, SPI1.SPCR2 4007 210Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	SCKASE	PTE	SPIIE	SPOE	SPPE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	SPPE	Parity Enable	0: Do not add parity bit to transmit data and do not check parity bit of receive data 1: When SPCR.TXMD = 0: Add parity bit to transmit data and check parity bit of receive data When SPCR.TXMD = 1: Add parity bit to transmit data but do not check parity bit of receive data.	R/W
b1	SPOE	Parity Mode	0: Select even parity for transmission and reception 1: Select odd parity for transmission and reception.	R/W
b2	SPIIE	SPI Idle Interrupt Enable	0: Disable idle interrupt requests 1: Enable idle interrupt requests.	R/W
b3	PTE	Parity Self-Testing	0: Disable self-diagnosis function of the parity circuit 1: Enable self-diagnosis function of the parity circuit.	R/W
b4	SCKASE	RSPCK Auto-Stop Function Enable	0: Disable RSPCK auto-stop function 1: Enable RSPCK auto-stop function.	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

If the SPPE, SPOE, or SCKASE bit in SPCR2 is changed while the SPCR.SPE bit is 1, do not perform subsequent operations.

SPPE bit (Parity Enable)

The SPPE bit enables or disables the parity function.

When the SPCR.TXMD bit is 0 and this bit is 1, the parity bit is added to transmit data and parity checking is performed for receive data.

When the SPCR.TXMD bit is 1 and this bit is 1, the parity bit is added to transmit data but parity checking is not performed for receive data.

SPOE bit (Parity Mode)

The SPOE bit specifies odd or even parity.

When even parity is set, parity bit addition is performed so that the total number of 1-bits in the transmit or receive character plus the parity bit is even. Similarly, when odd parity is set, parity bit addition is performed so that the total number of 1-bits in the transmit or receive character plus the parity bit is odd.

The SPOE bit is only valid when the SPPE bit is 1.

SPIIE bit (SPI Idle Interrupt Enable)

The SPIIE bit enables or disables the generation of SPI idle interrupt requests when an idle state is detected in the SPI and the SPSR.IDLNF flag clears to 0.

PTE bit (Parity Self-Testing)

The PTE bit enables self-diagnosis of the parity circuit to check whether the parity function is operating correctly.

SCKASE bit (RSPCK Auto-Stop Function Enable)

The SCKASE bit enables or disables the RSPCK auto-stop function. When this function is enabled, the RSPCK clock is stopped before an overrun error occurs when data is received in master mode. For details, see section 38.3.8.1, Overrun errors.

38.2.13 SPI控制寄存器2(SPCR2)

Address(es): SPI0.SPCR2 4007 200Fh, SPI1.SPCR2 4007 210Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	SCKASE	PTE	SPIIE	SPOE	SPPE
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	SPPE	奇偶校验使能	0：发送数据不添加奇偶校验位，接收数据不校验校验位1：当SPCR.TXMD=0：发送数据添加校验位，接收数据校验校验位当SPCR.TXMD=1：添加校验位位发送数据，但不检查接收数据的奇偶校验位。	R/W
b1	SPOE	奇偶校验模式	0：发送和接收选择偶校验1：发送和接收选择奇校验。	R/W
b2	SPIIE	SPI空闲中断使能	0：禁用空闲中断请求1：启用空闲中断请求。	R/W
b3	PTE	Parity Self-Testing	0：禁用奇偶电路自诊断功能1：启用奇偶电路自诊断功能。	R/W
b4	SCKASE	RSPCK Auto-Stop Function Enable	0：禁用RSPCK自动停机功能1：启用RSPCK自动停机功能。	R/W
b7 to b5	—	Reserved	这些位被读取为0。写入值应为0。	R/W

如果SPCR.SPE位为1时SPCR2中的SPPE、SPOE或SCKASE位发生变化，则不要执行后续操作。

SPPE位（奇偶校验使能）

SPPE位启用或禁用奇偶校验功能。

当SPCR.TXMD位为0且该位为1时，发送数据添加奇偶校验位，接收数据执行奇偶校验。

当SPCR.TXMD位为1且该位为1时，发送数据添加奇偶校验位，但接收数据不执行奇偶校验。

SPOE位（奇偶校验模式）

SPOE位指定奇校验或偶校验。

设置偶校验时，执行奇偶校验位相加，使发送或接收字符中的1位总数加上奇偶校验位为偶数。类似地，当设置奇校验时，执行奇偶校验位相加，以使发送或接收字符中的1位加上奇偶校验位的总数为奇数。

SPOE位仅在SPPE位为1时有效。

SPIIE位（SPI空闲中断使能）

当在SPI中检测到空闲状态并且SPSR.IDLNF标志清零时，SPIIE位启用或禁用SPI空闲中断请求的生成。

PTE位（奇偶自检）

PTE位启用奇偶校验电路的自诊断，以检查奇偶校验功能是否正常运行。

SCKASE位（RSPCK自动停止功能使能）

SCKASE位启用或禁用RSPCK自动停止功能。当此功能使能时，在主机模式下接收数据时，在发生溢出错误之前停止RSPCK时钟。有关详细信息，请参阅第38.3.8.1节，溢出错误。

38.2.14 SPI Command Registers 0 to 7 (SPCMD0 to SPCMD7)

Address(es): SPI0.SPCMD0 4007 2010h, SPI0.SPCMD1 4007 2012h, SPI0.SPCMD2 4007 2014h, SPI0.SPCMD3 4007 2016h, SPI0.SPCMD4 4007 2018h, SPI0.SPCMD5 4007 201Ah, SPI0.SPCMD6 4007 201Ch, SPI0.SPCMD7 4007 201Eh, SPI1.SPCMD0 4007 2110h, SPI1.SPCMD1 4007 2112h, SPI1.SPCMD2 4007 2114h, SPI1.SPCMD3 4007 2116h, SPI1.SPCMD4 4007 2118h, SPI1.SPCMD5 4007 211Ah, SPI1.SPCMD6 4007 211Ch, SPI1.SPCMD7 4007 211Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SCKDEN	SLNDEN	SPNDEN	LSBF	SPB[3:0]				SSLKP	SSLA[2:0]			BRDV[1:0]		CPOL	CPHA
Value after reset:	0	0	0	0	0	1	1	1	0	0	0	0	1	1	0	1

Bit	Symbol	Bit name	Description	R/W
b0	CPHA	RSPCK Phase Setting	0: Select data sampling on leading edge, data change on trailing edge 1: Select data change on leading edge, data sampling on trailing edge.	R/W
b1	CPOL	RSPCK Polarity Setting	0: Set RSPCK low during idle 1: Set RSPCK high during idle.	R/W
b3, b2	BRDV[1:0]	Bit Rate Division Setting	b3 b2 0 0: Base bit rate 0 1: Base bit rate divided by 2 1 0: Base bit rate divided by 4 1 1: Base bit rate divided by 8.	R/W
b6 to b4	SSLA[2:0]	SSL Signal Assertion Setting	b6 b4 0 0 0: SSL0 0 0 1: SSL1 0 1 0: SSL2 0 1 1: SSL3 1 x x: Setting prohibited. x: Don't care.	R/W
b7	SSLKP	SSL Signal Level Keeping	0: Negate all SSL signals on completion of transfer 1: Keep SSL signal level from the end of transfer until the beginning of the next access.	R/W
b11 to b8	SPB[3:0]	SPI Data Length Setting	b11 b8 0100 to 0111: 8 bits 1 0 0 0: 9 bits 1 0 0 1: 10 bits 1 0 1 0: 11 bits 1 0 1 1: 12 bits 1 1 0 0: 13 bits 1 1 0 1: 14 bits 1 1 1 0: 15 bits 1 1 1 1: 16 bits 0 0 0 0: 20 bits 0 0 0 1: 24 bits 0010, 0011: 32 bits.	R/W
b12	LSBF	SPI LSB First	0: MSB first 1: LSB first.	R/W
b13	SPNDEN	SPI Next-Access Delay Enable	0: Select next-access delay of 1 RSPCK + 2 PCLKA 1: Select next-access delay equal to the setting in the SPI Next-Access Delay Register (SPND).	R/W
b14	SLNDEN	SSL Negation Delay Setting Enable	0: Select SSL negation delay of 1 RSPCK 1: Select SSL negation delay equal to the setting in the SPI Slave Select Negation Delay Register (SSLND).	R/W
b15	SCKDEN	RSPCK Delay Setting Enable	0: Select RSPCK delay of 1 RSPCK 1: Select RSPCK delay equal to the setting in the SPI Clock Delay Register (SPCKD).	R/W

The SPCMDm registers specify the transfer format for the SPI in master mode. Each channel has eight SPI Command Registers (SPCMD0 to SPCMD7). Some of the bits in the SPCMD0 register are used to set the transfer mode for the SPI in slave mode. The SPI in master mode sequentially references the SPCMDm registers based on the settings in the

38.2.14 SPI命令寄存器0到7(SPCMD0到SPCMD7)

Address(es): SPI0.SPCMD0 4007 2010h, SPI0.SPCMD1 4007 2012h, SPI0.SPCMD2 4007 2014h, SPI0.SPCMD3 4007 2016h, SPI0.SPCMD4 4007 2018h, SPI0.SPCMD5 4007 201Ah, SPI0.SPCMD6 4007 201Ch, SPI0.SPCMD7 4007 201Eh, SPI1.SPCMD0 4007 2110h, SPI1.SPCMD1 4007 2112h, SPI1.SPCMD2 4007 2114h, SPI1.SPCMD3 4007 2116h, SPI1.SPCMD4 4007 2118h, SPI1.SPCMD5 4007 211Ah, SPI1.SPCMD6 4007 211Ch, SPI1.SPCMD7 4007 211Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SCKDEN	SLNDEN	SPNDEN	LSBF	SPB[3:0]				SSLKP	SSLA[2:0]			BRDV[1:0]		CPOL	CPHA
重置后的值：	0	0	0	0	0	1	1	1	0	0	0	0	1	1	0	1

Bit	Symbol	位名称	Description	R/W
b0	CPHA	RSPCK相位设置	0：选择前沿数据采样，后沿数据变化1：选择前沿数据变化，后沿数据采样。	R/W
b1	CPOL	RSPCK极性设置	0：空闲时将RSPCK设置为低电平1：空闲时将RSPCK设置为高电平。	R/W
b3, b2	BRDV[1:0]	比特率划分设置	b3b200：基本比特率01：基本比特率除以210：基本比特率除以411：基本比特率除以8。	R/W
b6 to b4	SSLA[2:0]	SSL信号断言设置	b6b4000：SSL0001：SSL1010：SSL2011：SSL31xx：禁止设置。x：不在乎。	R/W
b7	SSLKP	SSL信号电平保持	0：在传输完成时否定所有SSL信号1：从传输结束到下一次访问开始时保持SSL信号电平。	R/W
b11 to b8	SPB[3:0]	SPI数据长度设置	b11b80100到0111：8位1000：9位1001：10位1010：11位1011：12位1100：13位1101：14位1110：15位1111：16位0000：20位0001：24位0010、0011：32位。	R/W
b12	LSBF	SPILSB优先	0: MSB first 1: LSB first.	R/W
b13	SPNDEN	SPI下一次访问延迟Enable	0：选择下一次访问延迟1RSPCK+2PCLKA1：选择下一次访问延迟等于SPI下一次访问延迟寄存器(SPND)中的设置。	R/W
b14	SLNDEN	SSL否定延迟设置Enable	0：选择SSL否定延迟为1RSPCK1：选择SSL否定延迟等于SPI从器件选择否定延迟寄存器(SSLND)中的设置。	R/W
b15	SCKDEN	RSPCK延迟设置启用	0：选择RSPCK延迟为1RSPCK1：选择RSPCK延迟等于SPI时钟延迟寄存器(SPCKD)中的设置。	R/W

SPCMDm寄存器指定主模式下SPI的传输格式。每个通道有8个SPI命令寄存器（SPCMD0到SPCMD7）。SPCMD0寄存器中的一些位用于设置SPI在从机模式下的传输模式。主模式下的SPI根据

SPSCR.SPSLN[2:0] bits and executes the serial transfer that is set in the referenced SPCMDm register.

Set the SPCMDm registers while the transmit buffer is empty (SPSR.SPTEF is 1 and data for the next transfer is not set) and before the setting of the data to be transmitted when that SPCMDm register is referenced.

The SPCMDm register referenced by the SPI in master mode can be checked by means of the SPSSR.SPCP[2:0] bits. If the contents of SPCMDm are changed while the SPCR.MSTR bit is 0 and the SPCR.SPE bit is 1, do not perform subsequent operations.

CPHA bit (RSPCK Phase Setting)

The CPHA bit selects the RSPCK phase of the SPI in master or slave mode. Data communications between SPI modules require the same RSPCK phase setting between the modules.

CPOL bit (RSPCK Polarity Setting)

The CPOL bit selects the RSPCK polarity of the SPI in master or slave mode. Data communications between SPI modules require the same RSPCK polarity setting between the modules.

BRDV[1:0] bits (Bit Rate Division Setting)

The BRDV[1:0] bits determine the bit rate. The bit rate is determined by the combination of the settings in the BRDV[1:0] bits and SPBR (see section 38.2.8, SPI Bit Rate Register (SPBR)). The SPBR settings determine the base bit rate. The BRDV[1:0] setting selects the bit rate obtained by dividing the base bit rate by 1, 2, 4, or 8. Different BRDV[1:0] bit settings can be specified in the SPCMDm registers. This enables execution of serial transfers at different bit rates for each command.

SSLA[2:0] bits (SSL Signal Assertion Setting)

The SSLA[2:0] bits control the SSLni signal assertion when the SPI performs serial transfers in master mode. When an SSLni signal is asserted, its polarity is determined by the value set in the associated SSLP. When the SSLA[2:0] bits are set to 000b in multi-master mode, serial transfers are performed with all the SSL signals in the negated state (as the SSLn0 pin acts as input).

When using the SPI in slave mode, set the SSLA[2:0] bits to 000b.

SSLKP bit (SSL Signal Level Keeping)

When the SPI in master mode performs a serial transfer, the SSLKP bit specifies whether the SSLni signal level for the current command is to be kept or negated between the SSL negation associated with the current command and the SSL assertion associated with the next command. Setting the SSLKP bit to 1 enables a burst transfer. For details, see section 38.3.10.1, Master mode operation. When using the SPI in slave mode, set the SSLKP bit to 0.

SPB[3:0] bits (SPI Data Length Setting)

The SPB[3:0] bits specify the transfer data length for the SPI in master or slave mode. When the SPLW bit is 0, set these bits from 8 to 16 bits.

LSBF bit (SPI LSB First)

The LSBF bit specifies the data format of the SPI in master or slave mode to MSB-first or LSB-first.

SPNDEN bit (SPI Next-Access Delay Enable)

The SPNDEN bit specifies the next-access delay, the period from the time the SPI in master mode terminates a serial transfer and sets the SSLni signal inactive until the SPI enables the SSLni signal assertion for the next access. If the SPNDEN bit is 0, the SPI sets the next-access delay to 1 RSPCK + 2 PCLKA. If the SPNDEN bit is 1, the SPI inserts a next-access delay in accordance with the SPND setting.

When using the SPI in slave mode, set the SPNDEN bit to 0.

SLNDEN bit (SSL Negation Delay Setting Enable)

The SLNDEN bit specifies the SSL negation delay, the period from the time the SPI in master mode stops RSPCK oscillation until the SPI sets the SSLni signal to inactive. If the SLNDEN bit is 0, the SPI sets the SSL negation delay to 1 RSPCK. If the SLNDEN bit is 1, the SPI negates the SSL signal at the SSL negation delay determined by the SSLND setting.

SPSCR.SPSLN[2:0]位并执行在引用的SPMDm寄存器中设置的串行传输。

在发送缓冲区为空时（SPSR.SPTEF为1且未设置下一次传输的数据）以及在引用该SPCMDm寄存器时设置要发送的数据之前设置SPCMDm寄存器。

SPI在主机模式下引用的SPCMDm寄存器可以通过SPSSR.SPCP[2:0]位进行检查。如果在SPCR.MSTR位为0且SPCR.SPE位为1时改变了SPCMDm的内容，则不要执行后续操作。

CPHA位（RSPCK相位设置）

CPHA位在主模式或从模式下选择SPI的RSPCK相位。SPI模块之间的数据通信需要模块之间相同的RSPCK相位设置。

CPOL位（RSPCK极性设置）

CPOL位在主模式或从模式下选择SPI的RSPCK极性。SPI模块之间的数据通信要求模块之间的RSPCK极性设置相同。

BRDV[1:0]位（比特率划分设置）

BRDV[1:0]位决定比特率。比特率由BRDV[1:0]位和SPBR中的设置组合确定（参见第38.2.8节，SPI比特率寄存器(SPBR)）。SPBR设置决定了基本比特率。BRDV[1:0]设置选择通过将基本比特率除以1、2、4或8获得的比特率。可以在SPCMDm寄存器中指定不同的BRDV[1:0]位设置。这使得每个命令能够以不同的比特率执行串行传输。

SSLA[2:0]位（SSL信号断言设置）

当SPI在主模式下执行串行传输时，SSLA[2:0]位控制SSLni信号断言。当SSLni信号被置位时，其极性由相关SSLP中设置的值确定。当SSLA[2:0]位在多主模式下设置为000b时，串行传输将在所有SSL信号处于否定状态时执行（因为SSLn0引脚用作输入）。

在从机模式下使用SPI时，将SSLA[2:0]位设置为000b。

SSLKP位（SSL信号电平保持）

当主模式的SPI执行串行传输时，SSLKP位指定当前命令的SSLni信号电平是在与当前命令关联的SSL否定和与下一个命令关联的SSL断言之间保持还是否定。将SSLKP位设置为1可启用突发传输。有关详细信息，请参阅第38.3.10.1节，主模式操作。在从机模式下使用SPI时，将SSLKP位设置为0。

SPB[3:0]位（SPI数据长度设置）

SPB[3:0]位指定SPI在主模式或从模式下的传输数据长度。当SPLW位为0时，将这些位设置为8至16位。

LSBF位（SPILSB优先）

LSBF位指定SPI在主模式或从模式下的数据格式为MSB优先或LSB优先。

SPNDEN位（SPI下一次访问延迟使能）

SPNDEN位指定下一次访问延迟，即从主模式下的SPI终止串行传输并将SSLni信号设置为无效到SPI为下一次访问启用SSLni信号断言的时间段。如果SPNDEN位为0，则SPI将下一次访问延迟设置为1RSPCK+2PCLKA。如果SPNDEN位为1，则SPI根据SPND设置插入下一次访问延迟。

在从机模式下使用SPI时，将SPNDEN位设置为0。

SLNDEN位（SSL否定延迟设置启用）

SLNDEN位指定SSL否定延迟，即从主模式下的SPI停止RSPCK振荡到SPI将SSLni信号设置为无效的时间段。如果SLNDEN位为0，则SPI将SSL否定延迟设置为1RSPCK。如果SLNDEN位为1，则SPI在SSL否定延迟由SSLND设置确定时否定SSL信号。

When using the SPI in slave mode, set the SLNDEN bit to 0.

SCKDEN bit (RSPCK Delay Setting Enable)

The SCKDEN bit specifies the SPI clock delay, the period from the point when the SPI in master mode asserts the SSLni signal until the RSPCK starts oscillation. If the SCKDEN bit is 0, the SPI sets the RSPCK delay to 1 RSPCK. If the SCKDEN bit is 1, the SPI starts the oscillation of RSPCK at the RSPCK delay determined by the SPCKD setting.

When using the SPI in slave mode, set the SCKDEN bit to 0.

38.2.15 SPI Data Control Register 2 (SPDCR2)

Address(es): SPI0.SPDCR2 4007 2020h, SPI1.SPDCR2 4007 2120h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	BYSW
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	BYSW	Byte Swap Operating Mode Select	0: Byte Swap OFF 1: Byte Swap ON	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

SPI Data Control Register2 (SPDCR2) is the setting register, that is to swap a transmit/receive data in byte units. When a data of transmit buffers copies to a shift register, it is to swap in byte units. When a data of shift register copies to a receive buffers, it is to swap in byte units.

BYSW bit (Byte Swap Operating Mode Select)

It is a setting bit, that is to swap a transmit/receive data in byte units. When byte access is valid (SPDCR.SPBYT = 1), byte swap is invalid. When byte swap is valid, parity function must be invalid (SPCR2.SPPE bit = 0). Setting change of BYSW bit must be SPCR.SPE bit = 0.

A data after byte swap is different by a data length (setting of SPCMD.SPB[3:0]).

When byte swap, A data length (setting of SPB[3:0]) must be set to 32 bit or 16bit. Other case of data length (that is 8 to 15, 20, 24 bit length), byte swap is not guaranteed. Before swap and after swap are shown below (length data (32 bit/16 bit)).

- Length data 32bit (SPB[3:0] = 0010 or 0011)

  Before swap: [31:24] [23:16] [15:8] [7:0]

  After swap: [7:0] [15:8] [23:16] [31:24]

- Length data 16bit (SPB[3:0] = 1111)

  Before swap: [31:24] [23:16]

  After swap: [23:16] [31:24].

When byte access mode (SPDCR.SPBT = 1), byte swap setting is invalid.

When byte swap is valid, set parity function to invalid (SPCR2.SPPE = 0). When the parity function set to valid, the behavior is not guaranteed.

38.3 Operation

In this section, the serial transfer period refers to the period from the beginning of driving valid data to the fetching of the final valid data.

38.3.1 Overview of SPI Operation

The SPI is capable of synchronous serial transfers in the following modes:

在从机模式下使用SPI时，将SLNDEN位设置为0。

SCKDEN位（RSPCK延迟设置使能）

SCKDEN位指定SPI时钟延迟，即从主模式下的SPI断言SSLni信号到RSPCK开始振荡的周期。如果SCKDEN位为0，则SPI将RSPCK延迟设置为1RSPCK。如果SCKDEN位为1，则SPI以由SPCKD设置确定的RSPCK延迟启动RSPCK的振荡。

在从机模式下使用SPI时，将SCKDEN位设置为0。

38.2.15 SPI数据控制寄存器2(SPDCR2)

Address(es): SPI0.SPDCR2 4007 2020h, SPI1.SPDCR2 4007 2120h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	BYSW
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	BYSW	字节交换操作模式选择	0：字节交换关闭 1：字节交换开启	R/W
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

SPI数据控制寄存器2(SPDCR2)是设置寄存器，即以字节为单位交换一个发送接收数据。当发送缓冲区的数据复制到移位寄存器时，是以字节为单位进行交换。当移位寄存器的数据复制到接收缓冲区时，是以字节为单位进行交换。

BYSW位（字节交换操作模式选择）

它是一个设置位，即以字节为单位交换一个发送接收数据。当字节访问有效时（SPDCR.SPBYT=1），字节交换无效。当字节交换有效时，奇偶校验功能必须无效（SPCR2.SPPE位=0）。BYSW位的设置更改必须是SPCR.SPE位=0。

字节交换后的数据因数据长度不同（SPCMD.SPB[3:0]的设置）。

字节交换时，A数据长度（SPB[3:0]的设置）必须设置为32位或16位。其他数据长度情况（即8到15、20、24位长度），不保证字节交换。交换前和交换后如下所示（长度数据（32位16位））。

- 长度数据32bit(SPB[3:0]=0010or0011)

  Before swap: [31:24] [23:16] [15:8] [7:0]

  After swap: [7:0] [15:8] [23:16] [31:24]

- 长度数据16bit(SPB[3:0]=1111)

  Before swap: [31:24] [23:16]

  After swap: [23:16] [31:24].

当字节访问模式（SPDCR.SPBT=1）时，字节交换设置无效。

当字节交换有效时，将奇偶校验功能设置为无效（SPCR2.SPPE=0）。当奇偶校验函数设置为有效时，行为不被保证。

38.3 Operation

在本节中，串行传输周期是指从开始驱动有效数据到获取最终有效数据的周期。

38.3.1 SPI操作概述

SPI能够在以下模式下进行同步串行传输：

- Slave mode (SPI operation)
- Single master mode (SPI operation)
- Multi-master mode (SPI operation)
- Slave mode (clock synchronous operation)
- Master mode (clock synchronous operation).

The SPI mode can be selected by using the MSTR, MODFEN, and SPMS bits in SPCR. Table 38.5 lists the relationship between SPI modes and SPCR settings, and a description of each mode.

Table 38.5 Relationship between SPCR settings and SPI modes (1 of 2)

Mode	Slave (SPI operation)	Single master (SPI operation)	Multi-master (SPI operation)	Slave (clock synchronous operation)	Master (clock synchronous operation)
MSTR bit setting	0	1	1	0	1
MODFEN bit setting	0 or 1	0	1	0	0
SPMS bit setting	0	0	0	1	1
RSPCKn signal	Input	Output	Output/Hi-Z	Input	Output
MOSIn signal	Input	Output	Output/Hi-Z	Input	Output
MISOn signal	Output/Hi-Z	Input	Input	Output	Input
SSLn0 signal	Input	Output	Input	Hi-Z*1	Hi-Z*1
SSLn1 to SSLn3 signals	Hi-Z*1	Output	Output/Hi-Z	Hi-Z*1	Hi-Z*1
SSL polarity change function	Supported	Supported	Supported	-	-
Max transfer rate	PCLKA/4	PCLKA/2	PCLKA/2	PCLKA/4	PCLKA/2
Clock source	RSPCKn input	On-chip baud rate generator	On-chip baud rate generator	RSPCKn input	On-chip baud rate generator
Clock polarity	Two				
Clock phase	Two	Two	Two	One (CPHA = 1)	Two
First transfer bit	MSB/LSB				
Transfer data length	8 to 16, 20, 24, 32 bits				
Burst transfer	Possible (CPHA = 1)	Possible (CPHA = 0,1)	Possible (CPHA = 0,1)	-	-
RSPCK delay control	Not supported	Supported	Supported	Not supported	Supported
SSL negation delay control	Not supported	Supported	Supported	Not supported	Supported
Next-access delay control	Not supported	Supported	Supported	Not supported	Supported
Transfer trigger	SSL input active or RSPCK oscillation	Write to transmit buffer on generation of transmit buffer empty interrupt request (SPTEF = 1)	Write to transmit buffer on generation of transmit buffer empty interrupt request (SPTEF = 1)	RSPCK oscillation	Write to transmit buffer on generation of transmit buffer empty interrupt request (SPTEF = 1)
Sequence control	Not supported	Supported	Supported	Not supported	Supported
Transmit buffer empty detection	Supported				
Receive buffer full detection	Supported*2				
Overrun error detection	Supported*2	Supported*2, *4	Supported*2, *4	Supported*2	Supported*2
Parity error detection	Supported*2,*3				
Mode fault error detection	Supported (MODFEN = 1)	Not supported	Supported	Not supported	Not supported

- 从机模式（SPI操作）
- 单主模式（SPI操作）
- Multi-master mode (SPI operation)
- 从机模式（时钟同步操作）
- 主模式（时钟同步操作）。

可以使用SPCR中的MSTR、MODFEN和SPMS位选择SPI模式。表38.5列出了SPI模式和SPCR设置之间的关系，以及每种模式的说明。

Table 38.5 SPCR设置和SPI模式之间的关系(1of2)

Mode	Slave (SPI operation)	单主机（SPI操作）	Multi-master (SPI operation)	从机（时钟同步操作）	主控（时钟同步操作）
MSTR位设置	0	1	1	0	1
MODFEN位设置	0 or 1	0	1	0	0
SPMS位设置	0	0	0	1	1
RSPCKn signal	Input	Output	Output/Hi-Z	Input	Output
MOSIn signal	Input	Output	Output/Hi-Z	Input	Output
MISOn signal	Output/Hi-Z	Input	Input	Output	Input
SSLn0 signal	Input	Output	Input	Hi-Z*1	Hi-Z*1
SSLn1到SSLn3信号	Hi-Z*1	Output	Output/Hi-Z	Hi-Z*1	Hi-Z*1
SSL极性改变功能	Supported	Supported	Supported	-	-
最大传输率	PCLKA/4	PCLKA/2	PCLKA/2	PCLKA/4	PCLKA/2
时钟源	RSPCKn input	片上波特率发生器	片上波特率发生器	RSPCKn input	片上波特率发生器
时钟极性	Two				
时钟相位	Two	Two	Two	One (CPHA = 1)	Two
第一个传输位	MSB/LSB				
传输数据长度	8至16、20、24、32位				
突发传输	Possible (CPHA = 1)	Possible (CPHA = 0,1)	Possible (CPHA = 0,1)	-	-
RSPCK延迟控制	不支持	Supported	Supported	不支持	Supported
SSL否定延迟控制	不支持	Supported	Supported	不支持	Supported
下一次访问延迟控制	不支持	Supported	Supported	不支持	Supported
转移触发	SSL输入有效或RSPCK振荡	在产生发送缓冲区空中断请求时写入发送缓冲区(SPTEF=1)	在产生发送缓冲区空中断请求时写入发送缓冲区(SPTEF=1)	RSPCK oscillation	在产生发送缓冲区空中断请求时写入发送缓冲区(SPTEF=1)
顺序控制	不支持	Supported	Supported	不支持	Supported
发送缓冲区空检测	Supported				
接收缓冲区满检测	Supported*2				
溢出错误检测	Supported*2	Supported*2, *4	Supported*2, *4	Supported*2	Supported*2
奇偶校验错误检测	Supported*2,*3				
模式故障错误检测	Supported (MODFEN = 1)	不支持	Supported	不支持	不支持

Table 38.5 Relationship between SPCR settings and SPI modes (2 of 2)

Mode	Slave (SPI operation)	Single master (SPI operation)	Multi-master (SPI operation)	Slave (clock synchronous operation)	Master (clock synchronous operation)
Underrun error detection	Supported	Not supported	Not supported	Supported	Not supported

Note 1. This function is not supported in this mode.
Note 2. When the SPCR.TXMD bit is 1, receiver buffer full detection, overrun error detection, and parity error detection are not performed.
Note 3. When the SPCR2.SPPE bit is 0, parity error detection is not performed.
Note 4. When the SPCR2.SCKASE bit is 1, overrun error detection is not performed.

38.3.2 Controlling the SPI Pins

The SPI can switch pin states based on the settings in the MSTR, MODFEN, and SPMS bits in SPCR and the PmnPFS.NCODR bit for the I/O ports. Table 38.6 lists the relationship between the pin states and bit settings. Setting the PmnPFS.NCODR bit for an I/O port to 0 selects CMOS output. Setting it to 1 selects open-drain output. The I/O port settings must follow this relationship.

Table 38.6 Relationship between pin states and bit settings

Mode	Pin	Pin state*2	
		PmnPFS.NCODR bit for I/O ports = 0	PmnPFS.NCODR bit for I/O ports = 1
Single master mode (SPI operation) (MSTR = 1, MODFEN = 0, SPMS = 0)	RSPCKn	CMOS output	Open-drain output
	SSLn0 to SSLn3	CMOS output	Open-drain output
	MOSIn	CMOS output	Open-drain output
	MISOn	Input	Input
Multi-master mode (SPI operation) (MSTR = 1, MODFEN = 1, SPMS = 0)	RSPCKn*3	CMOS output/Hi-Z	Open-drain output/Hi-Z
	SSLn0	Input	Input
	SSLn1 to SSLn3*3	CMOS output/Hi-Z	Open-drain output/Hi-Z
	MOSIn*3	CMOS output/Hi-Z	Open-drain output/Hi-Z
	MISOn	Input	Input
Slave mode (SPI operation) (MSTR = 0, SPMS = 0)	RSPCKn	Input	Input
	SSLn0	Input	Input
	SSLn1 to SSLn3*5	Hi-Z*1	Hi-Z*1
	MOSIn	Input	Input
	MISOn*4	CMOS output/Hi-Z	Open-drain output/Hi-Z
Master mode (clock synchronous operation) (MSTR = 1, MODFEN = 0, SPMS = 1)	RSPCKn	CMOS output	Open-drain output
	SSLn0 to SSLn3*5	Hi-Z*1	Hi-Z*1
	MOSIn	CMOS output	Open-drain output
	MISOn	Input	Input
Slave mode (clock synchronous operation) (MSTR = 0, SPMS = 1)	RSPCKn	Input	Input
	SSLn0 to SSLn3*5	Hi-Z*1	Hi-Z*1
	MOSIn	Input	Input
	MISOn	CMOS output	Open-drain output

Note 1. This function is not supported in this mode.
Note 2. SPI settings are not reflected in multiplexed pins for which the SPI function is not selected.
Note 3. When SSLn0 is at the active level, the pin state is Hi-Z.
Note 4. When SSLn0 is at the non-active level or the SPCR.SPE bit is 0, the pin state is Hi-Z.
Note 5. These pins are available for use as I/O port pins.

The SPI in single master mode (SPI operation) or multi-master mode (SPI operation) determines the MOSI signal values during the SSL negation period (including the SSL retention period during a burst transfer) based on the MOIFE and

Table 38.5 SPCR设置和SPI模式之间的关系(2of2)

Mode	Slave (SPI operation)	单主机（SPI操作）	Multi-master (SPI operation)	从机（时钟同步操作）	主控（时钟同步操作）
欠载错误检测	Supported	不支持	不支持	Supported	不支持

Note 1. 此模式不支持此功能。
Note 2. 当SPCR.TXMD位为1时，不执行接收缓冲区满检测、溢出错误检测和奇偶校验错误检测。

Note 3. 当SPCR2.SPPE位为0时，不执行奇偶校验错误检测。
Note 4. 当SPCR2.SCKASE位为1时，不执行溢出错误检测。

38.3.2 控制SPI引脚

SPI可以根据SPCR中的MSTR、MODFEN和SPMS位的设置来切换引脚状态，以及IO端口的PmnPFS.NCODR位。表38.6列出了引脚状态和位设置之间的关系。设置IO端口的PmnPFS.NCODR位为0选择CMOS输出。将其设置为1选择开漏输出。IO端口设置必须遵循这种关系。

Table 38.6 引脚状态和位设置之间的关系

Mode	Pin	Pin state*2	
		IO端口的PmnPFS.NCODR位=0	IO端口的PmnPFS.NCODR位=1
单主模式（SPI操作）（MSTR=1，MODFEN=0，SPMS=0）	RSPCKn	CMOS output	Open-drain output
	SSLn0 to SSLn3	CMOS output	Open-drain output
	MOSIn	CMOS output	Open-drain output
	MISOn	Input	Input
Multi-master mode (SPI operation) (MSTR = 1, MODFEN = 1, SPMS = 0)	RSPCKn*3	CMOS output/Hi-Z	Open-drain output/Hi-Z
	SSLn0	Input	Input
	SSLn1 to SSLn3*3	CMOS output/Hi-Z	Open-drain output/Hi-Z
	MOSIn*3	CMOS output/Hi-Z	Open-drain output/Hi-Z
	MISOn	Input	Input
从机模式（SPI操作）（MSTR=0，SPMS=0）	RSPCKn	Input	Input
	SSLn0	Input	Input
	SSLn1 to SSLn3*5	Hi-Z*1	Hi-Z*1
	MOSIn	Input	Input
	MISOn*4	CMOS output/Hi-Z	Open-drain output/Hi-Z
主模式（时钟同步操作）（MSTR=1，MODFEN=0，SPMS=1）	RSPCKn	CMOS output	Open-drain output
	SSLn0 to SSLn3*5	Hi-Z*1	Hi-Z*1
	MOSIn	CMOS output	Open-drain output
	MISOn	Input	Input
从机模式（时钟同步操作）（MSTR=0，SPMS=1）	RSPCKn	Input	Input
	SSLn0 to SSLn3*5	Hi-Z*1	Hi-Z*1
	MOSIn	Input	Input
	MISOn	CMOS output	Open-drain output

Note 1. 此模式不支持此功能。
Note 2. SPI设置不会反映在未选择SPI功能的复用引脚中。
Note 3. 当SSLn0处于有效电平时，引脚状态为Hi-Z。
Note 4. 当SSLn0处于非活动电平或SPCR.SPE位为0时，引脚状态为Hi-Z。
Note 5. 这些引脚可用作IO端口引脚。

单主机模式（SPI操作）或多主机模式（SPI操作）的SPI根据MOIFE和

MOIFV bit settings in SPPCR, as listed in Table 38.7.

Table 38.7 MOSI signal value determination during SSL negation

MOIFE bit	MOIFV bit	MOSIn signal value during SSL negation
0	0, 1	Final data from previous transfer
1	0	Low
1	1	High

38.3.3 SPI System Configuration Examples

38.3.3.1 Single master and single slave with the MCU as a master

Figure 38.5 shows a single-master and single-slave SPI system configuration example where the MCU is a master. In the single-master/single-slave configuration, the SSLn0 to SSLn3 outputs of the MCU (master) are not used. The SSL input of the SPI slave is fixed to the low level, and the SPI slave is maintained in the selected state.*1

The MCU (master) drives the RSPCKn and MOSIn signals. The SPI slave drives the MISO signal.

Note 1. In the transfer format configured when the SPCMDm.CPHA bit is 0, the SSL signal cannot be fixed to the active level for some slave devices. In situations where the SSL signal cannot be fixed, the SSLni output of the MCU must be connected to the SSL input of the slave device.

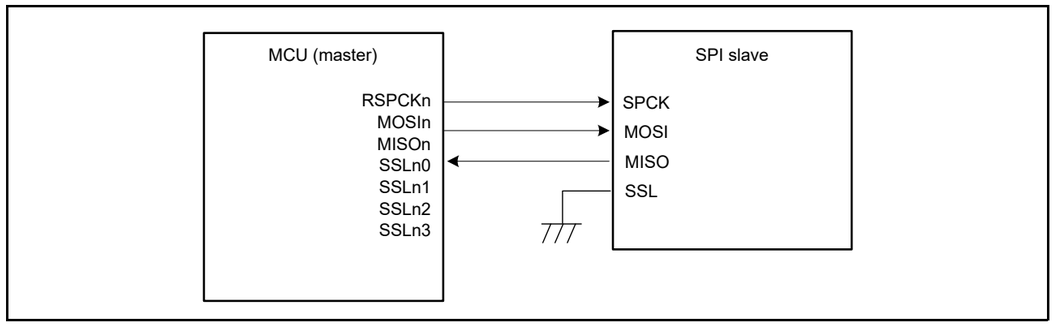


Figure 38.5 Single-master/single-slave configuration example with the MCU as a master

38.3.3.2 Single master and single slave with the MCU as a slave

Figure 38.6 shows a single-master/single-slave SPI system configuration example where the MCU is a slave. When the MCU is a slave, the SSLn0 pin is used as SSL input. The SPI master drives the RSPCK and MOSI signals. The MCU (slave) drives the MISOn signal.*1

In the single-slave configuration when the SPCMDm.CPHA bit is set to 1, the SSLn0 input of the MCU (slave) is fixed to the low level and the MCU (slave) stays selected. This enables serial transfer execution (Figure 38.7).

Note 1. When SSLn0 is at the non-active level, the pin state is Hi-Z.

SPPCR中的MOIFV位设置，如表38.7中所列。

Table 38.7 SSL否定期间的MOSI信号值确定

MOIFE bit	MOIFV bit	SSL否定期间的MOSIn信号值
0	0, 1	上次传输的最终数据
1	0	Low
1	1	High

38.3.3 SPI系统配置示例

38.3.3.1 单主单从，单片机为主

图38.5显示了单主单从SPI系统配置示例，其中MCU为主。在单主单从配置中，不使用MCU（主）的SSLn0到SSLn3输出。SPI从机的SSL输入固定为低电平，SPI从机保持在选中状态。*1

MCU（主控）驱动RSPCKn和MOSIn信号。SPI从机驱动MISO信号。

注1.在SPCMDm.CPHA位为0时配置的传输格式中，对于某些从设备，SSL信号不能固定为有效电平。在SSL信号无法固定的情况下，MCU的SSLni输出必须连接到从设备的SSL输入。

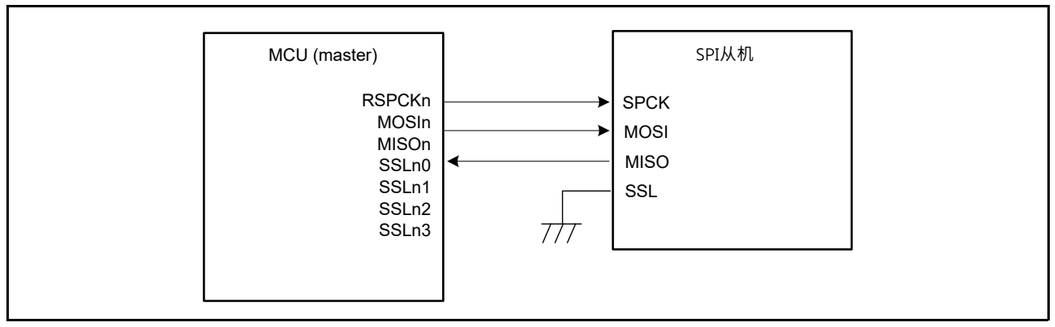


Figure 38.5 MCU为主的单主单从配置示例

38.3.3.2 单主单从单片机作为从机

图38.6显示了单主单从SPI系统配置示例，其中MCU为从设备。当。。。的时候
MCU为从机，SSLn0引脚用作SSL输入。SPI主机驱动RSPCK和MOSI信号。MCU（从机）驱动MIOn信号。*1

在单从配置中，当SPCMDm.CPHA位设置为1时，MCU（从）的SSLn0输入固定为低电平，MCU（从）保持选择状态。这将启用串行传输执行（图38.7）。

注1.当SSLn0处于非活动电平时，引脚状态为Hi-Z。

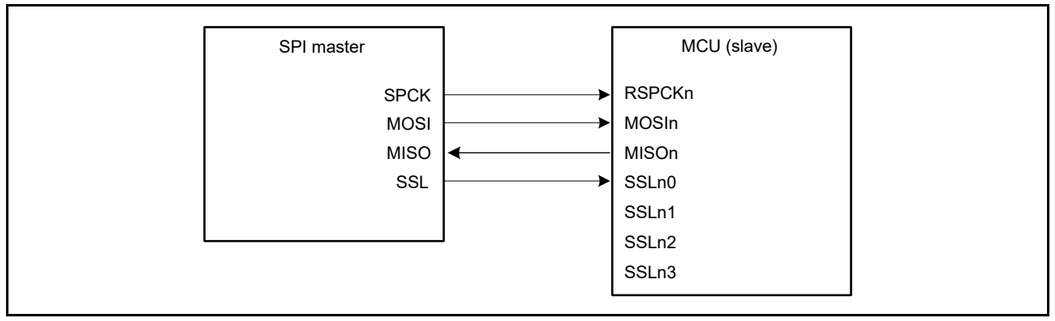


Figure 38.6 Single-master/single-slave configuration example with the MCU as a slave and CPHA = 0

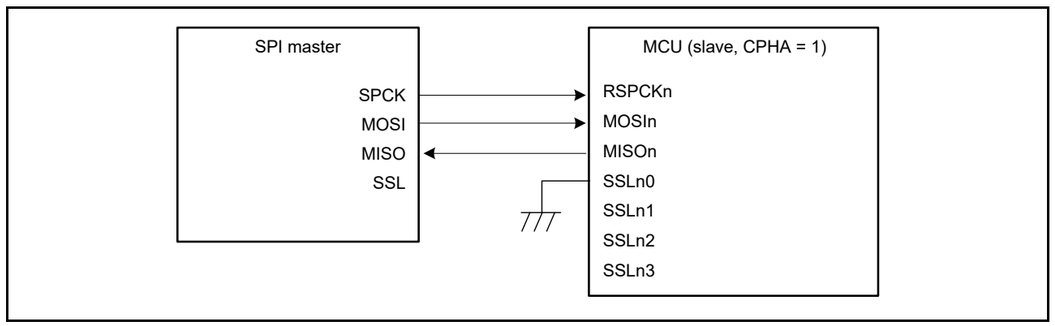


Figure 38.7 Single-master/single-slave configuration example with the MCU as a slave and CPHA = 1

38.3.3.3 Single master and multi slave with the MCU as a master

Figure 38.8 shows a single-master/multi-slave SPI system configuration example where the MCU is a master. In this example, the SPI system includes the MCU (master) and four slaves (SPI slave 0 to SPI slave 3).

The RSPCKn and MOSIn outputs of the MCU (master) are connected to the RSPCK and MOSI inputs of SPI slaves 0 to 3. The MISO outputs of SPI slaves 0 to 3 are all connected to the MISOn input of the MCU (master). The SSLn0 to SSLn3 outputs of the MCU (master) are connected to the SSL inputs of SPI slaves 0 to 3, respectively.

The MCU (master) drives the RSPCKn, MOSIn, and SSLn0 to SSLn3 signals. Of the SPI slaves 0 to 3, the slave that receives low-level input into the SSL input drives the MISO signal.

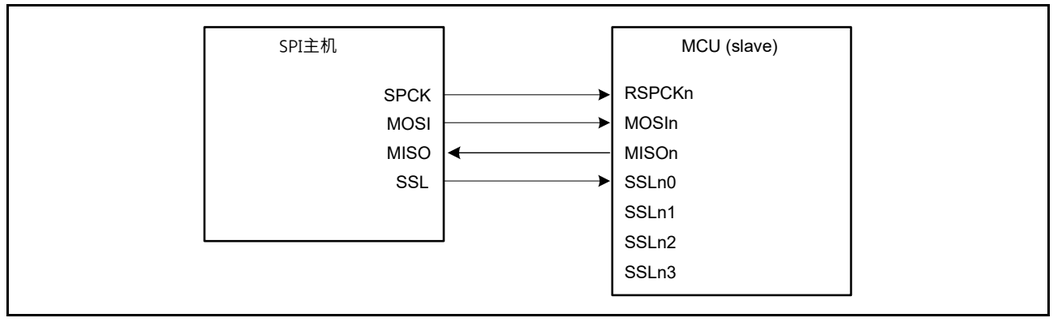


Figure 38.6 单主单从配置示例，单片机作为从机，CPHA=0

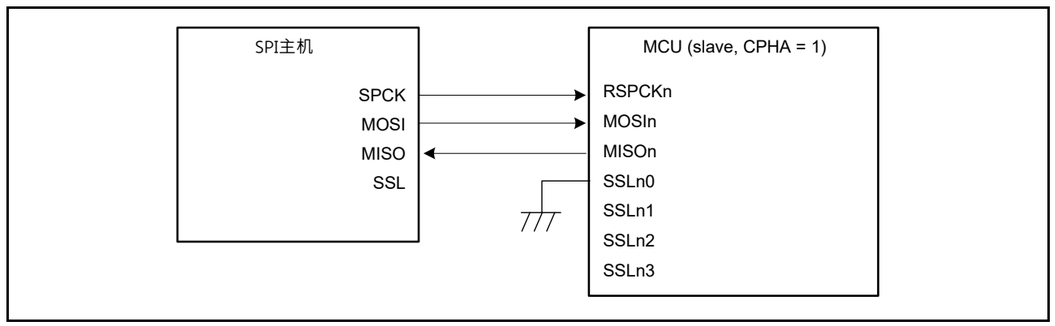


Figure 38.7 MCU作为从机且CPHA=1的单主单从配置示例

38.3.3.3 单主多从，单片机为主

图38.8显示了单主多从SPI系统配置示例，其中MCU为主。在本例中，SPI系统包括MCU（主机）和四个从机（SPI从机0到SPI从机3）。

MCU（主机）的RSPCKn和MOSIn输出连接到SPI从机0到3的RSPCK和MOSI输入。SPI从机0到3的MISO输出都连接到MCU（主机）的MISOn输入。MCU（主机）的SSLn0到SSLn3输出分别连接到SPI从机0到3的SSL输入。

MCU（主控）驱动RSPCKn、MOSIn和SSLn0到SSLn3信号。在SPI从机0到3中，接收到SSL输入的低电平输入的从机驱动MISO信号。

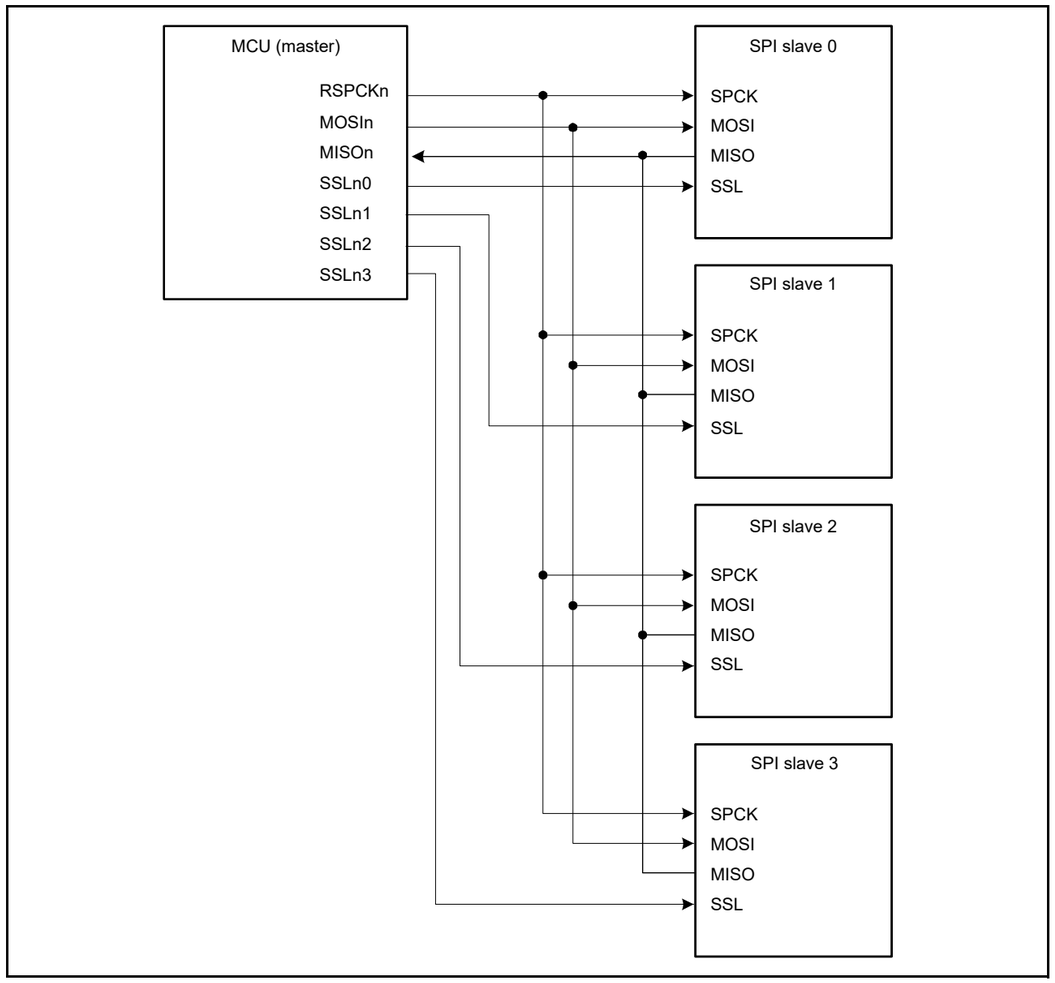


Figure 38.8 Single master/multi-slave configuration example with the MCU as a master

38.3.3.4 Single master and multi slave with the MCU as a slave

Figure 38.9 shows a single-master and multi-slave SPI system configuration example where the MCU is a slave. In this example, the SPI system includes an SPI master and two MCUs (slaves X and Y).

The SPCK and MOSI outputs of the SPI master are connected to the RSPCKn and MOSIn inputs of the MCUs (slaves X and Y). The MISOn outputs of the MCUs (slaves X and Y) are all connected to the MISO input of the SPI master. The SSLX and SSLY outputs of the SPI master are connected to the SSLn0 inputs of the MCUs (slaves X and Y, respectively).

The SPI master drives the SPCK, MOSI, SSLX, and SSLY signals. Of the MCUs (slaves X and Y), the slave that receives low-level input into the SSLn0 input drives the MISOn signal.

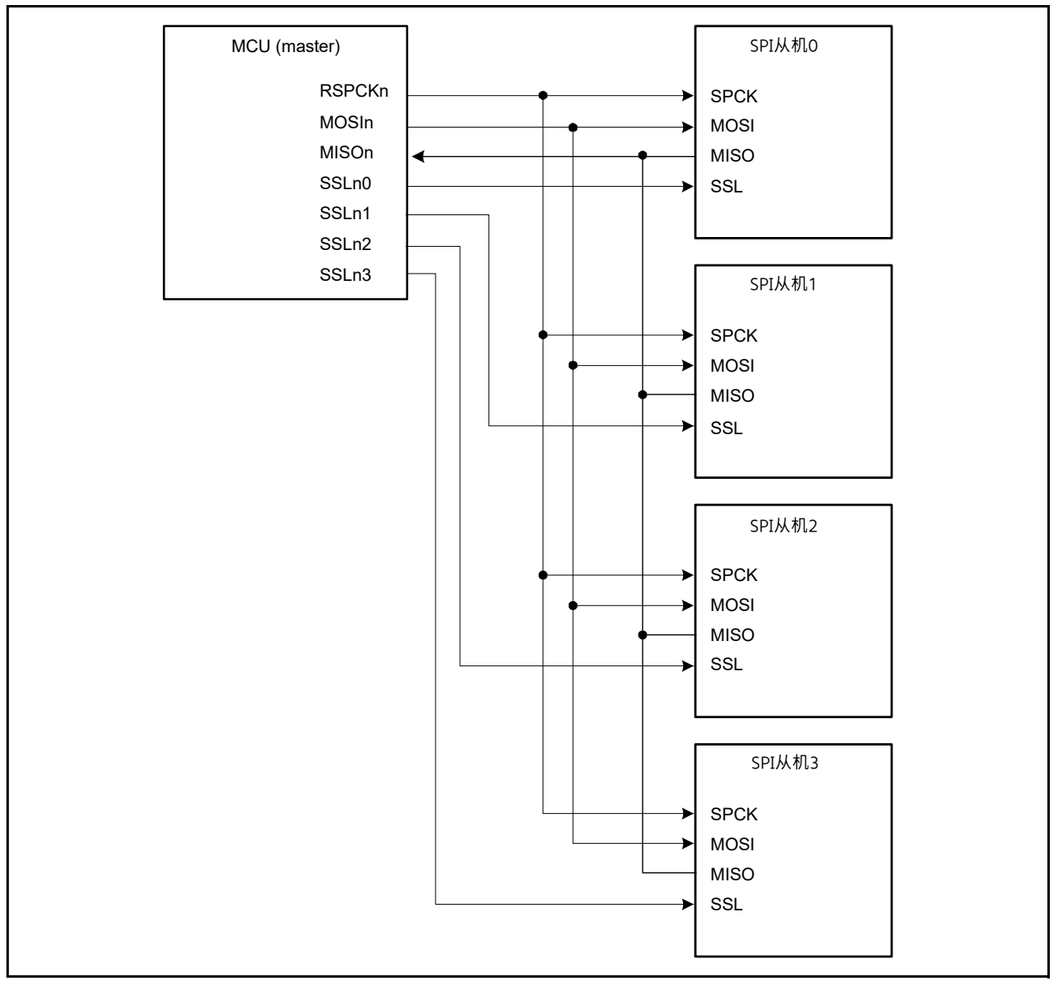


Figure 38.8 MCU为主的单主多从配置示例

38.3.3.4 单主多从，单片机作为从机

图38.9显示了单主多从SPI系统配置示例，其中MCU是从设备。在本例中，SPI系统包括一个SPI主控和两个MCU（从属X和Y）。

SPI主机的SPCK和MOSI输出连接到MCU（从机X和Y）的RSPCKn和MOSIn输入。MCU（从机X和Y）的MISOn输出都连接到SPI主机的MISO输入。SPI主机的SSLX和SSLY输出连接到MCU的SSLn0输入（分别为从机X和Y）。

SPI主机驱动SPCK、MOSI、SSLX和SSLY信号。在MCU（从机X和Y）中，接收到SSLn0输入的低电平输入的从机驱动MISOn信号。

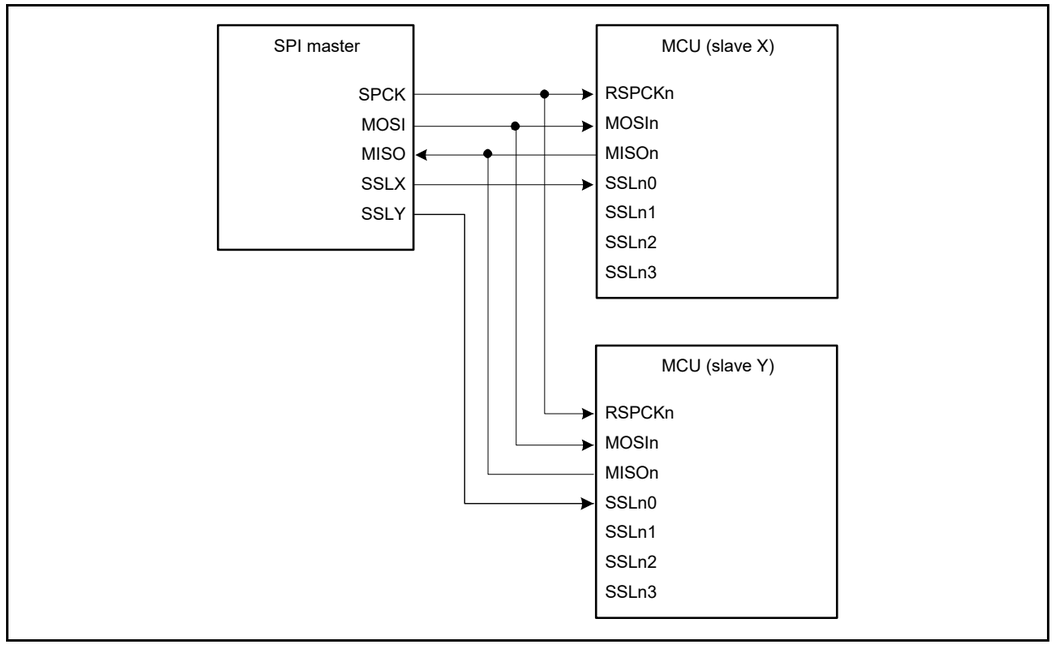


Figure 38.9 Single-master/multi-slave configuration example with the MCU as a slave

38.3.3.5 Multi master and multi slave with the MCU as a master

Figure 38.10 shows a multi-master/multi-slave SPI system configuration example where the MCU is a master. In this example, the SPI system includes two MCUs (masters X and Y) and two SPI slaves (SPI slaves 1 and 2).

The RSPCKn and MOSIn outputs of the MCUs (masters X and Y) are connected to the RSPCK and MOSI inputs of SPI slaves 1 and 2. The MISO outputs of SPI slaves 1 and 2 are connected to the MISOn inputs of the MCUs (masters X and Y). Any generic port Y output from the MCU (master X) is connected to the SSLn0 input of the MCU (master Y). Any generic port X output of the MCU (master Y) is connected to the SSLn0 input of the MCU (master X). The SSLn1 and SSLn2 outputs of the MCUs (masters X and Y) are connected to the SSL inputs of the SPI slaves 1 and 2. In this configuration example, because the system can be comprised solely of SSLn0 input, and SSLn1 and SSLn2 outputs for slave connections, the SSLn3 output of the MCU is not required.

The MCU drives the RSPCKn, MOSIn, SSLn1, and SSLn2 signals when the SSLn0 input level is high. When the SSLn0 input level is low, the MCU detects a mode fault error, sets RSPCKn, MOSIn, SSLn1, and SSLn2 to Hi-Z, and releases the SPI bus directly to the other master. Of the SPI slaves 1 and 2, the slave that receives low-level input into the SSL input drives the MISO signal.

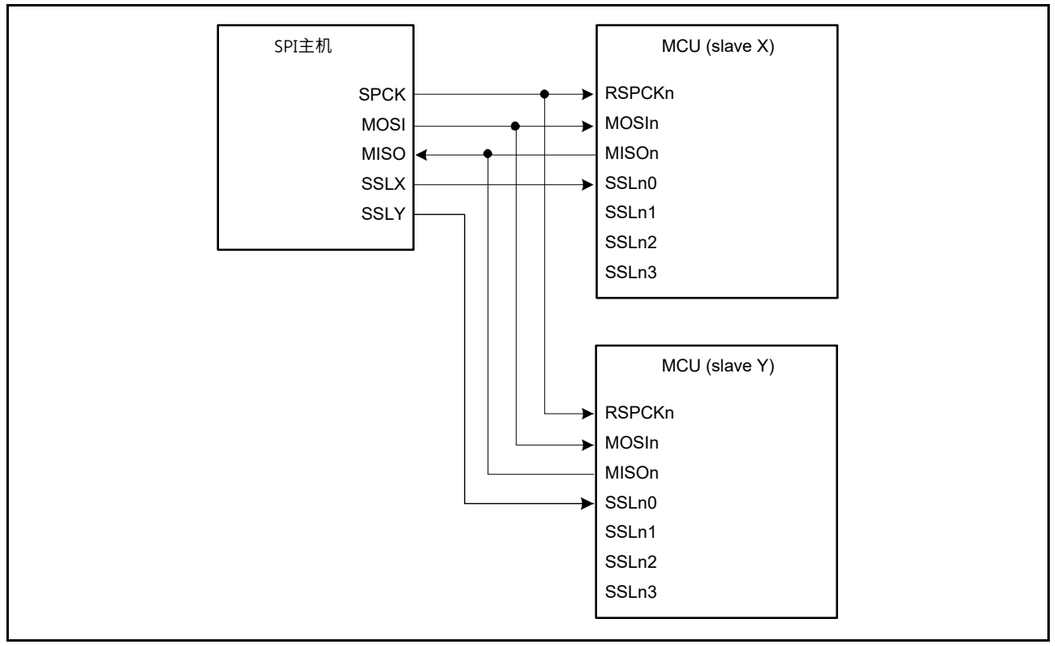


Figure 38.9 MCU作为从机的单主多从配置示例

38.3.3.5 以单片机为主的多主多从

图38.10显示了一个多主多从SPI系统配置示例，其中MCU为主。在此示例中，SPI系统包括两个MCU（主X和Y）和两个SPI从机（SPI从机1和2）。

MCU（主机X和Y）的RSPCKn和MOSIn输出连接到SPI从机1和2的RSPCK和MOSI输入。SPI从机1和2的MISO输出连接到MCU（主机X）的MISOn输入和Y)。来自MCU（主X）的任何通用端口Y输出都连接到MCU（主Y）的SSLn0输入。MCU（主设备Y）的任何通用端口X输出都连接到MCU（主设备X）的SSLn0输入。MCU（主机X和Y）的SSLn1和SSLn2输出连接到SPI从机1和2的SSL输入。在此配置示例中，因为系统可以仅由SSLn0输入和SSLn1和SSLn2输出组成从连接，不需要MCU的SSLn3输出。

当SSLn0输入电平为高电平时，MCU驱动RSPCKn、MOSIn、SSLn1和SSLn2信号。当SSLn0输入电平为低时，MCU检测到模式故障错误，将RSPCKn、MOSIn、SSLn1和SSLn2设置为Hi-Z，并将SPI总线直接释放到另一个主控。在SPI从机1和2中，接收到SSL输入的低电平输入的从机驱动MISO信号。

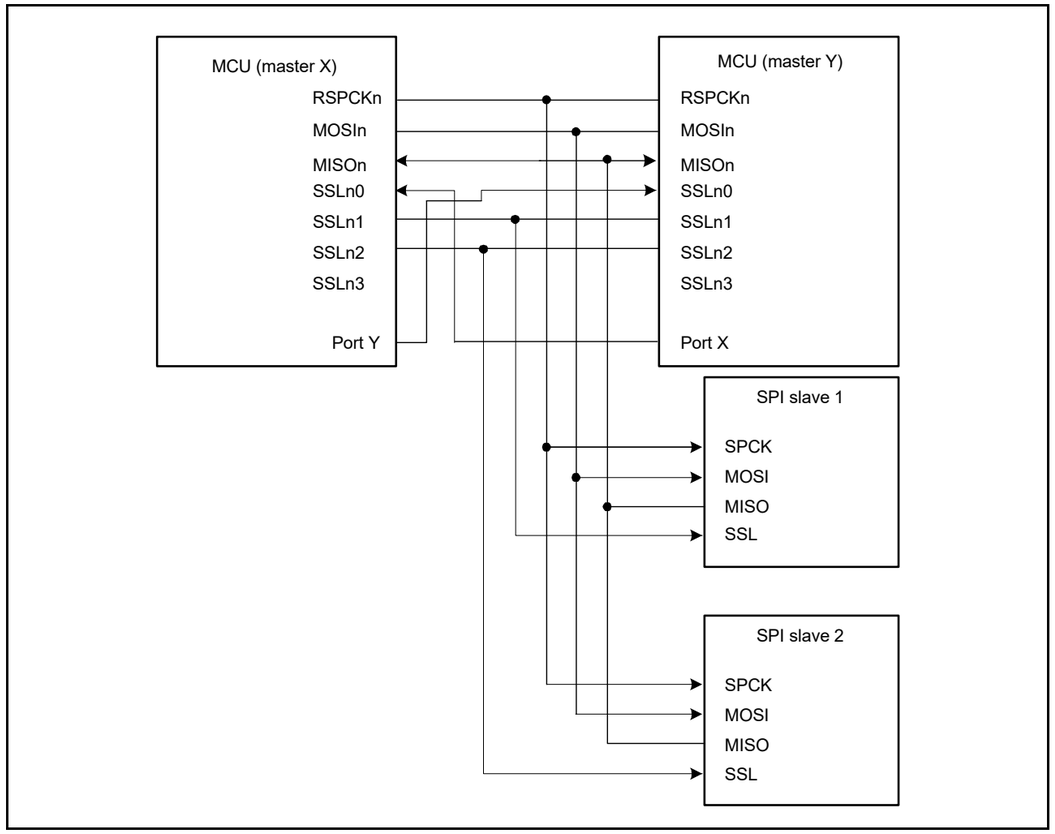


Figure 38.10 Multi-master/multi-slave configuration example with the MCU as a master

38.3.3.6 Master and slave in clock synchronous mode with the MCU as a master

Figure 38.11 shows master and slave in clock synchronous mode where the MCU is a master. In this configuration, SSLn0 to SSLn3 of the MCU (master) are not used.

The MCU (master) drives the RSPCKn and MOSIn signals. The SPI slave drives the MISO signal.

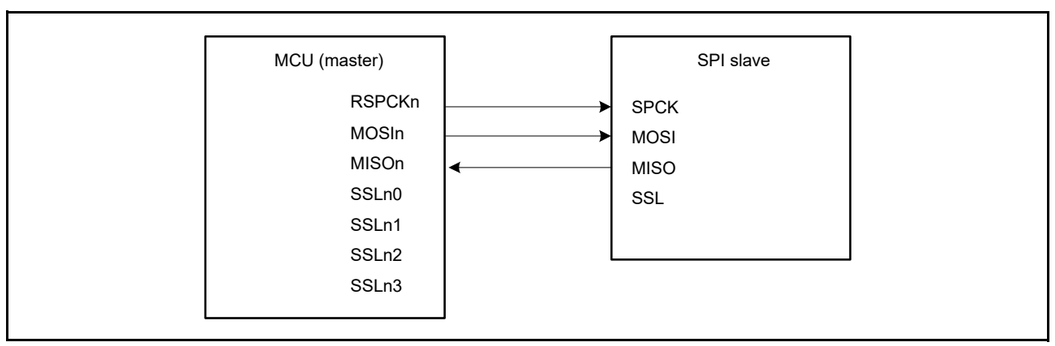


Figure 38.11 Configuration example of master/slave in clock synchronous mode with the MCU as a master

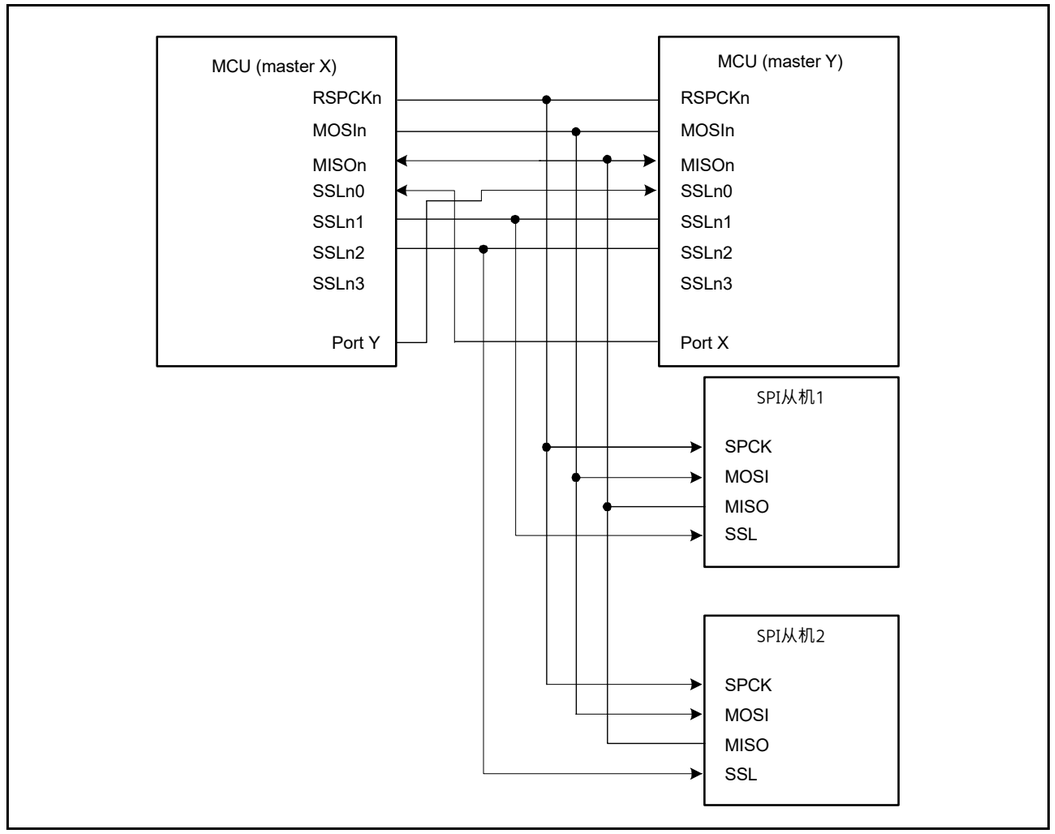


Figure 38.10 MCU为主的多主多从配置示例

38.3.3.6 主从时钟同步模式，单片机作为主控

图38.11显示了时钟同步模式下的主机和从机，其中MCU是主机。在这种配置中，不使用MCU（主）的SSLn0到SSLn3。

MCU（主控）驱动RSPCKn和MOSIn信号。SPI从机驱动MISO信号。

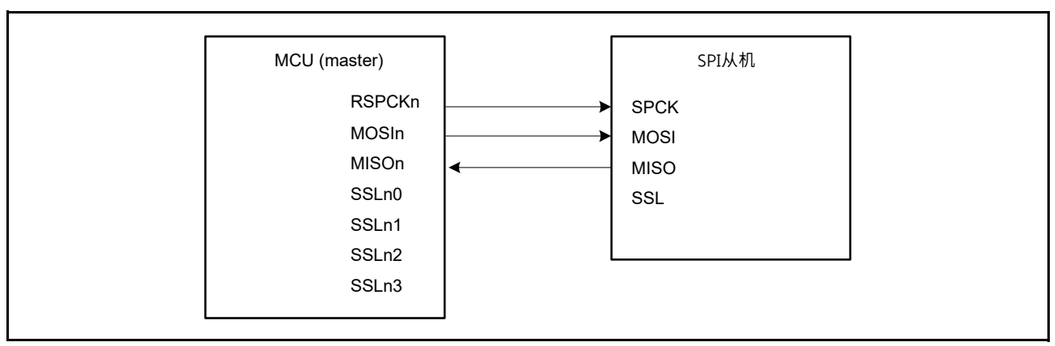


Figure 38.11 MCU作为主控时钟同步模式主从配置示例

38.3.3.7 Master and slave in clock synchronous mode with the MCU as a slave

Figure 38.12 shows a master and slave in clock synchronous mode configuration where the MCU is a slave. When the MCU operates as a slave in clock synchronous mode, the MCU (slave) drives the MISOn signal and the SPI master drives the SPCK and MOSI signals. In addition, SSLn0 to SSLn3 of the MCU (slave) are not used.

The MCU (slave) can only execute serial transfers in the single slave configuration when the SPCMDm.CPHA bit is set to 1.

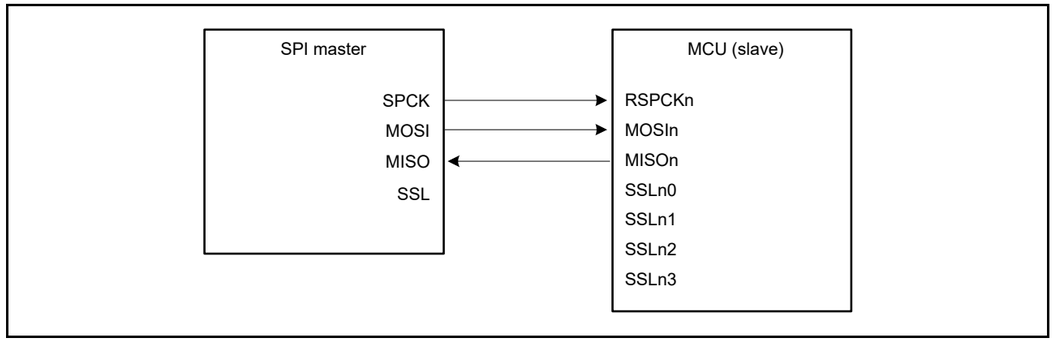


Figure 38.12 Configuration example of master and slave in clock synchronous mode with the MCU as a slave and CPHA = 1

38.3.4 Data Formats

The data format of the SPI depends on the settings in SPI Command Register m (SPCMDm) (m = 0 to 7) and the parity enable bit in SPI Control Register 2 (SPCR2.SPPE). Regardless of whether the MSB or LSB is first, the SPI treats the range from the LSB bit in the SPI Data Register (SPDR/SPDR_HA) to the bit corresponding to the selected data length, as transfer data.

This section shows the format of one frame of data before or after transfer.

(a) Data format with parity disabled

When parity is disabled, transmission or reception of data proceeds with the length in bits selected in the SPI data length setting in SPI Command Register m (SPCMDm.SPB[3:0]).

(b) Data format with parity enabled

When parity is enabled, transmission or reception of data proceeds with the length in bits selected in the SPI data length setting in SPI Command Register m (SPCMDm.SPB[3:0]). In this case, however, the last bit is a parity bit.

38.3.3.7 主从时钟同步模式，单片机作为从机

图38.12显示了时钟同步模式配置中的主机和从机，其中MCU是从机。当。。。的时候
MCU在时钟同步模式下作为从机运行，MCU（从机）驱动MISON信号，SPI主机驱动SPCK和MOSI信号。此外，不使用MCU（从机）的SSLn0到SSLn3。

当SPMDm.CPHA位设置为1时，MCU（从机）只能在单从机配置中执行串行传输。

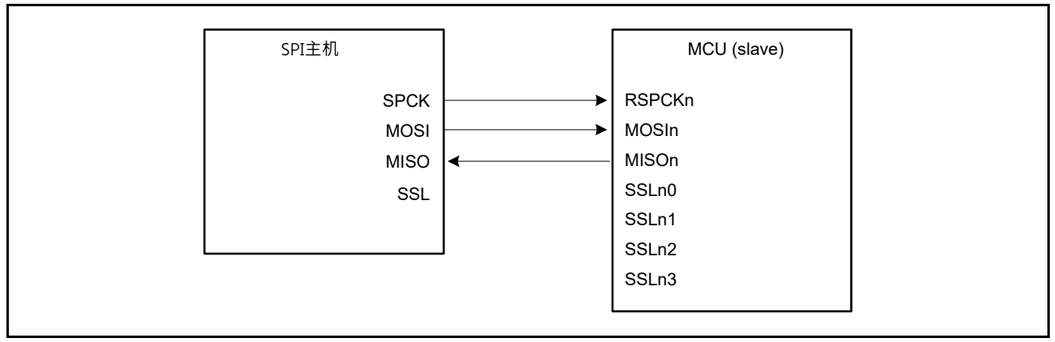


Figure 38.12 单片机作为从机，CPHA=1，时钟同步模式的主从配置示例

38.3.4 数据格式

SPI的数据格式取决于SPI命令寄存器m(SPCMDm)(m=0to7)中的设置和SPI控制寄存器2(SPCR2.SPPE)中的奇偶校验使能位。无论是MSB还是LSB在前，SPI都将SPI数据寄存器(SPDRSPDR_HA)中的LSB位到所选数据长度对应的位的范围视为传输数据。

本节显示传输前后一帧数据的格式。

(a) 禁用奇偶校验的数据格式

当奇偶校验被禁用时，数据的发送或接收将按照在SPI命令寄存器m(SPCMDm.SPB[3:0])的SPI数据长度设置中选择的位长度进行。

(b) 启用奇偶校验的数据格式

当奇偶校验使能时，数据的发送或接收按照在SPI命令寄存器m(SPCMDm.SPB[3:0])的SPI数据长度设置中选择的位长度进行。然而，在这种情况下，最后一位是奇偶校验位。

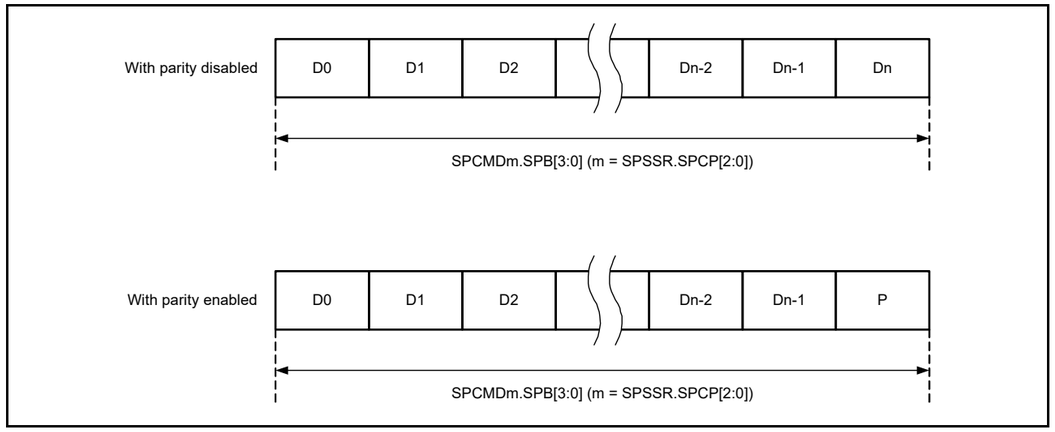


Figure 38.13 Data format with parity disabled and enabled

38.3.4.1 Operation when parity is disabled (SPCR2.SPPE = 0)

When parity is disabled, data for transmission is copied to the shift register with no pre-processing. This section describes the connection between the SPI Data Register (SPDR/SPDR_HA) and the shift register in terms of the combination of MSB- or LSB-first order and data length.

(1) MSB-first transfer with 32-bit data

Figure 38.14 shows the transfer operations of the SPI Data Register (SPDR) and the shift register with parity disabled, an SPI data length of 32 bits, and MSB-first selected.

In transmission, bits T31 to T00 from the current stage of the transmit buffer are copied to the shift register. Data for transmission is shifted out from the shift register from T31 to T30, and continuing to T00, in that order.

In reception, received data is shifted in bit-by-bit through bit [0] of the shift register. When the R31 to R00 bits are collected after input of the required number of RSPCK cycles, the value in the shift register is copied to the receive buffer.

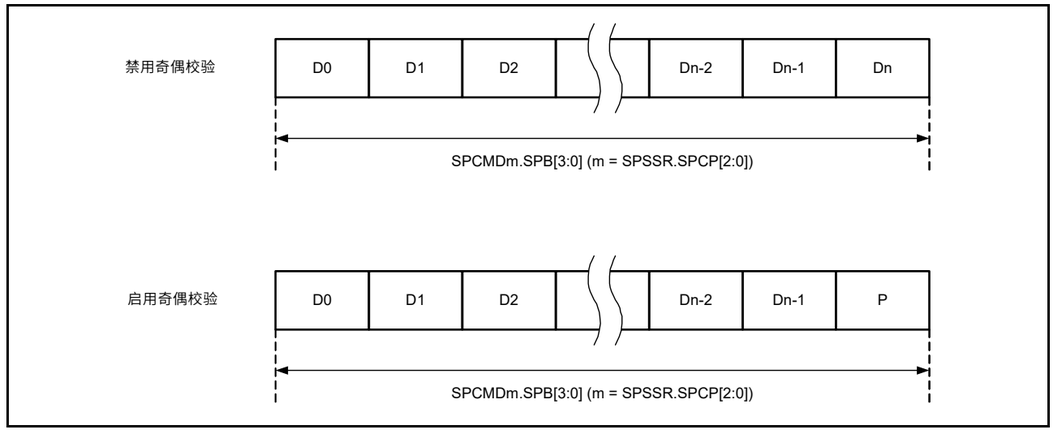


Figure 38.13 禁用和启用奇偶校验的数据格式

38.3.4.1 禁用奇偶校验时的操作(SPCR2.SPPE=0)

当奇偶校验被禁用时，用于传输的数据被复制到移位寄存器而不进行预处理。本节从MSB或LSB-firstorder和数据长度的组合来描述SPI数据寄存器(SPDRSPDR_HA)和移位寄存器之间的连接。

(1) 32位数据的MSB优先传输

图38.14显示了SPI数据寄存器(SPDR)和禁用奇偶校验的移位寄存器的传输操作，SPI数据长度为32位，且MSB优先选择。

在发送过程中，发送缓冲器当前级的T31到T00位被复制到移位寄存器。用于发送的数据从移位寄存器中移出，从T31移出到T30，并按此顺序继续移到T00。

在接收时，接收到的数据通过移位寄存器的位[0]逐位移位。在输入所需的RSPCK周期数后收集R31至R00位时，将移位寄存器中的值复制到接收缓冲区。

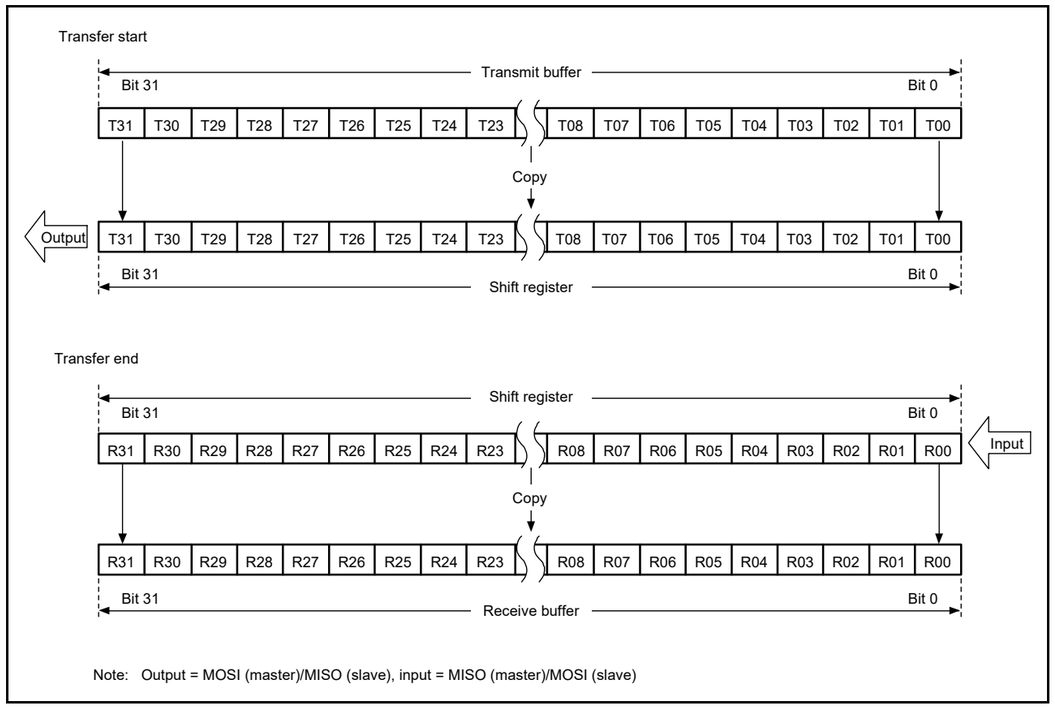


Figure 38.14 MSB-first transfer with 32-bit data and parity disabled

(2) MSB-first transfer with 24-bit data

Figure 38.15 shows the transfer operations of the SPI Data Register (SPDR) and the shift register with parity disabled, an SPI data length of 24 bits, and MSB-first selected.

In transmission, the lower 24 bits (T23 to T00) from the current stage of the transmit buffer are copied to the shift register. Data for transmission is shifted out from the shift register from T23 to T22, and continuing to T00, in that order.

In reception, received data is shifted in bit-by-bit through bit [0] of the shift register. When the R23 to R00 bits are collected after input of the required number of RSPCK cycles, the value in the shift register is copied to the receive buffer. The upper 8 bits of the transmit buffer are stored in the upper 8 bits of the receive buffer. Writing 0 to bits T31 to T24 at the time of transmission leads to 0 being inserted in the upper 8 bits of the receive buffer.

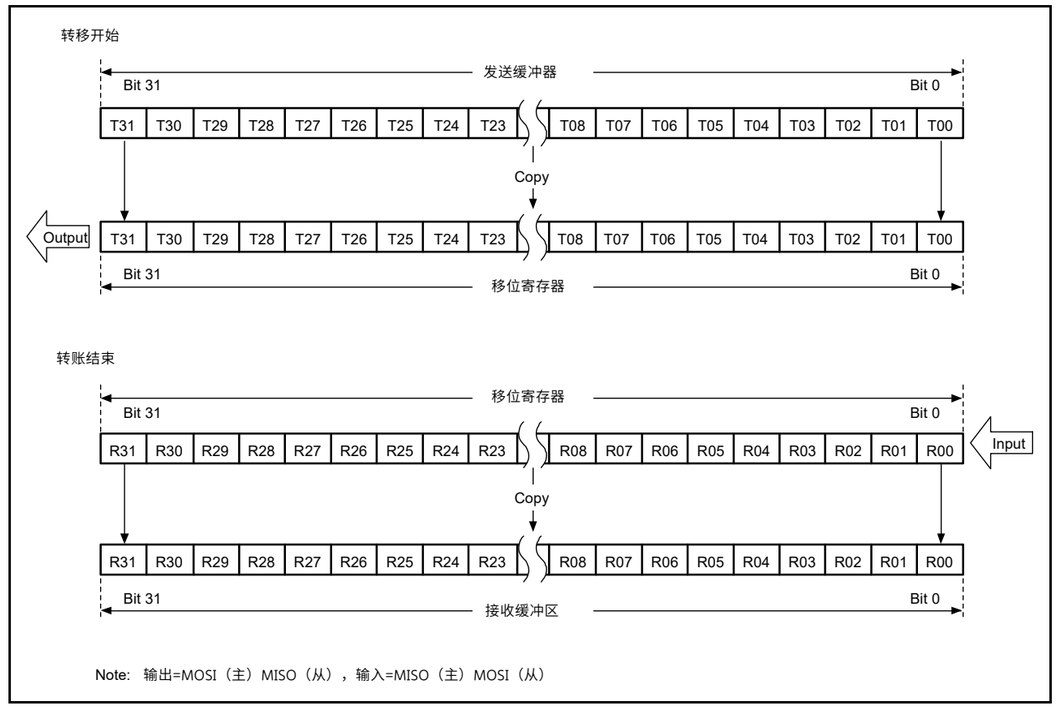


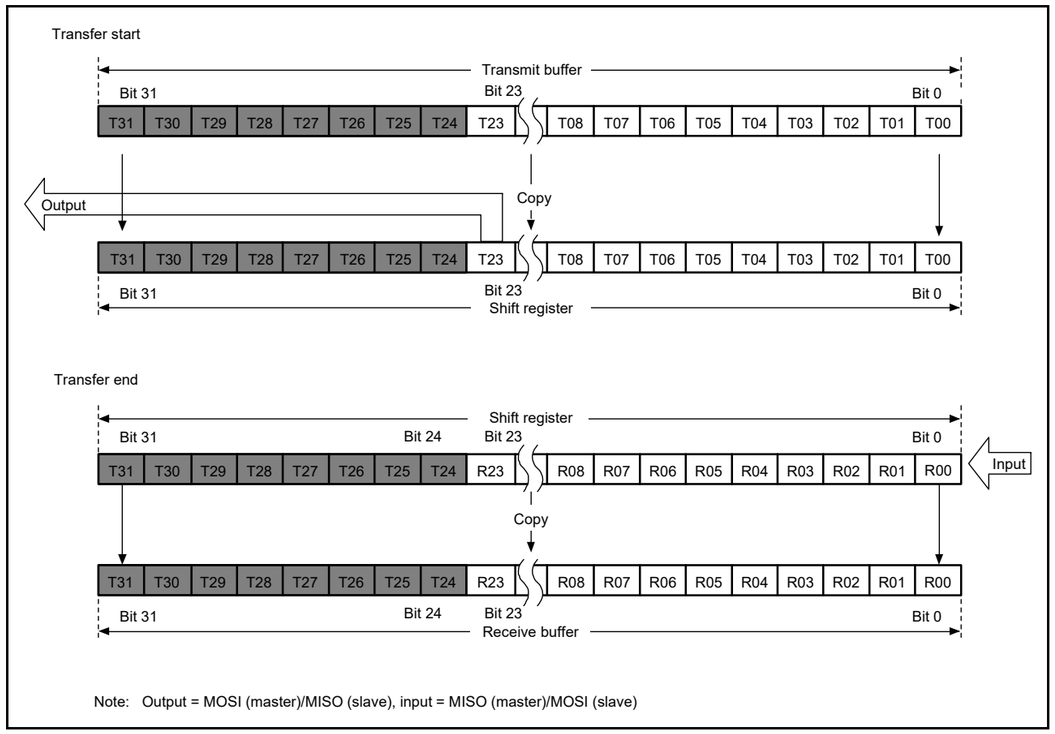
Figure 38.14 禁用32位数据和奇偶校验的MSB优先传输

(2) 24位数据的MSB优先传输

图38.15显示了SPI数据寄存器(SPDR)和禁用奇偶校验的移位寄存器的传输操作，
SPI数据长度为24位，且MSB优先选择。

在发送过程中，来自发送缓冲器当前阶段的低24位（T23到T00）被复制到移位寄存器。用于发送的数据从移位寄存器中从T23移出到T22，并按此顺序继续移到T00。

在接收时，接收到的数据通过移位寄存器的位[0]逐位移位。在输入所需数量的RSPCK周期后，当R23到R00位被收集时，移位寄存器中的值被复制到接收缓冲区。发送缓冲区的高8位存储在接收缓冲区的高8位中。在发送时将0写入位T31至T24会导致将0插入接收缓冲区的高8位。



Note: Output = MOSI (master)/MISO (slave), input = MISO (master)/MOSI (slave)

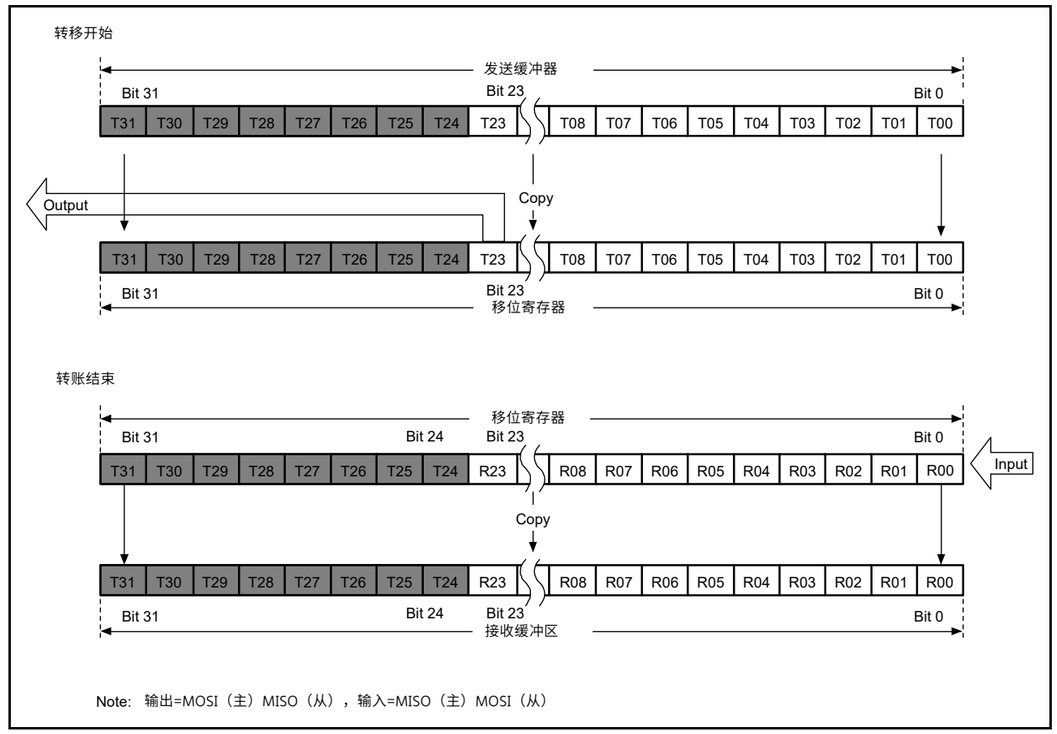
Figure 38.15 MSB-first transfer with 24-bit data and parity disabled

(3) LSB-first transfer with 32-bit data

Figure 38.16 shows the transfer operations of the SPI Data Register (SPDR) and the shift register with parity disabled, an SPI data length of 32 bits, and LSB-first selected.

In transmission, bits T31 to T00 from the current stage of the transmit buffer are reordered bit-by-bit to obtain the order T00 to T31 for copying to the shift register. Data for transmission is shifted out from the shift register from T00 to T01, and continuing to T31, in that order.

In reception, received data is shifted in bit-by-bit through bit [0] of the shift register. When the R00 to R31 bits are collected after input of the required number of RSPCK cycles, the value in the shift register is copied to the receive buffer.



Note: 输出=MOSI（主）MISO（从），输入=MISO（主）MOSI（从）

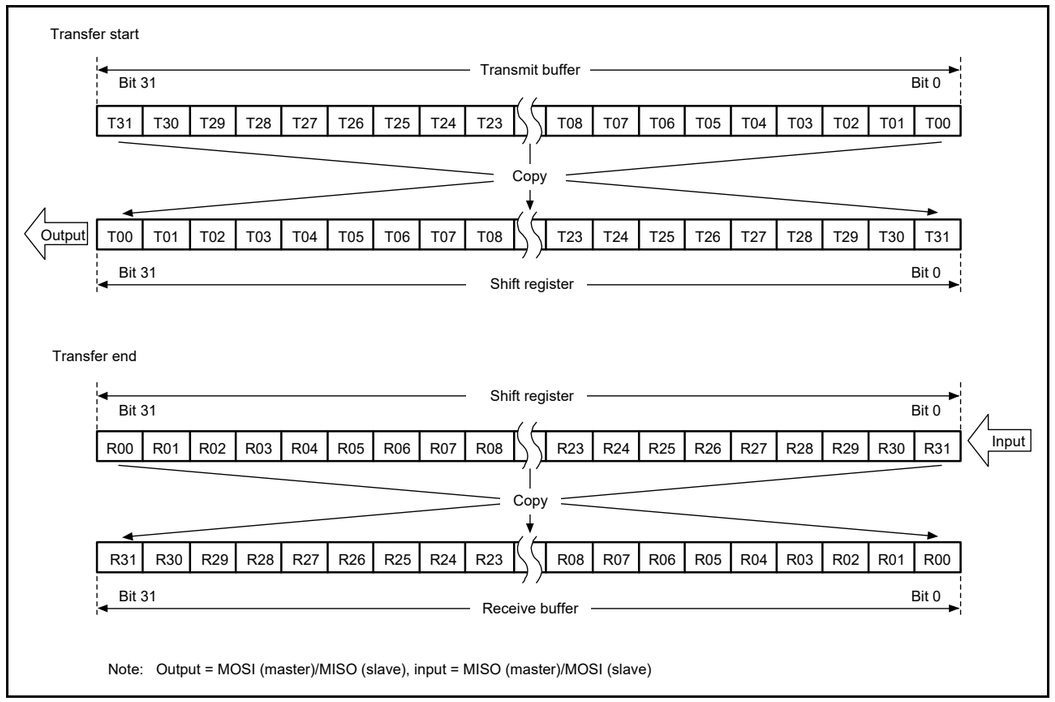
Figure 38.15 禁用24位数据和奇偶校验的MSB优先传输

(3) 32位数据的LSB优先传输

图38.16显示了SPI数据寄存器(SPDR)和禁用奇偶校验的移位寄存器的传输操作，
SPI数据长度为32位，并选择LSB-first。

在传输过程中，传输缓冲器当前级的位T31到T00被逐位重新排序，以获得用于复制到移位寄存器的顺序T00到T31。用于发送的数据从移位寄存器中从T00移出到T01，并按此顺序继续到T31。

在接收时，接收到的数据通过移位寄存器的位[0]逐位移位。在输入所需数量的RSPCK周期后收集R00至R31位时，将移位寄存器中的值复制到接收缓冲区。



Note: Output = MOSI (master)/MISO (slave), input = MISO (master)/MOSI (slave)

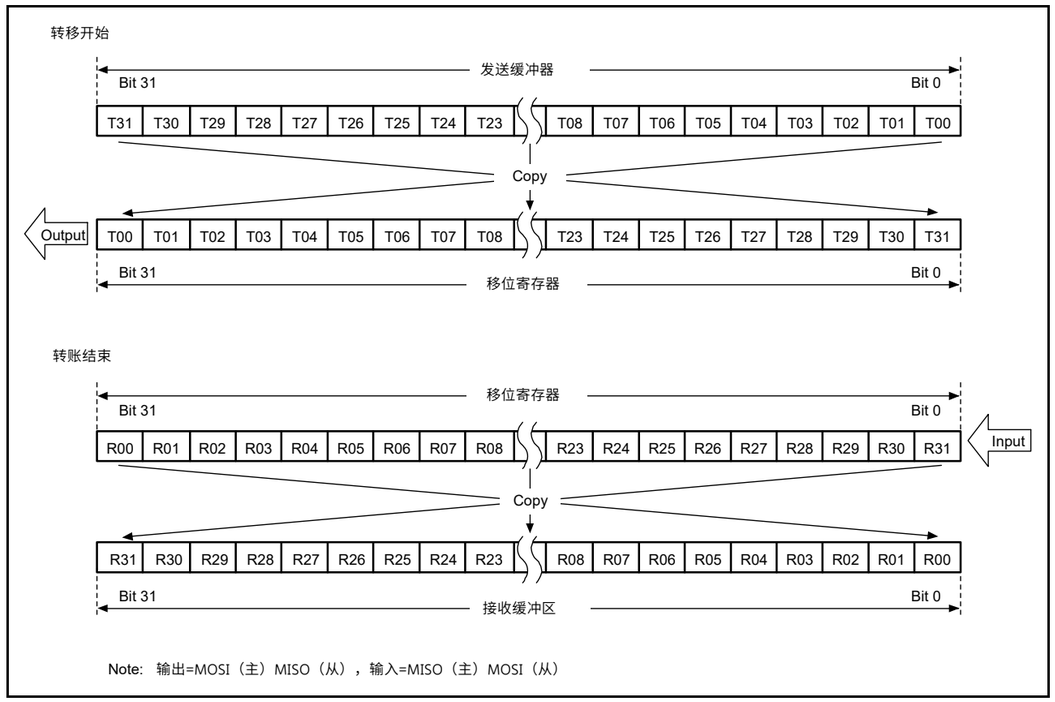
Figure 38.16 LSB-first transfer with 32-bit data and parity disabled

(4) LSB-first transfer with 24-bit data

Figure 38.17 shows the transfer operations of the SPI Data Register (SPDR) and the shift register with parity disabled, an SPI data length of 24 bits, and LSB-first selected.

In transmission, the lower 24 bits (T23 to T00) from the current stage of the transmit buffer are reordered bit-by-bit to obtain the order T00 to T23 for copying to the shift register. Data for transmission is shifted out from the shift register from T00 to T01, and continuing to T23, in that order.

In reception, received data is shifted in bit-by-bit through bit [8] of the shift register. When the R00 to R23 bits are collected after input of the required number of RSPCK cycles, the value in the shift register is copied to the receive buffer. The upper 8 bits of the transmit buffer are stored in the upper 8 bits of the receive buffer. Writing 0 to bits T31 to T24 at the time of transmission leads to 0 being inserted in the upper 8 bits of the receive buffer.



Note: 输出=MOSI（主）MISO（从），输入=MISO（主）MOSI（从）

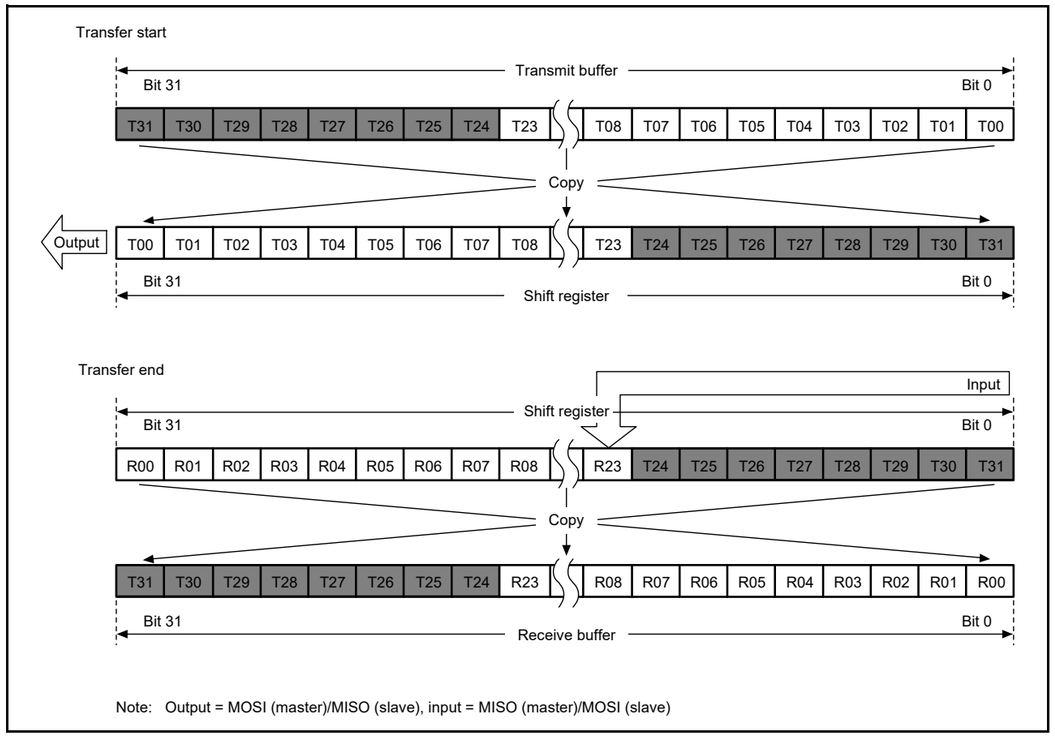
Figure 38.16 LSB优先传输，32位数据和奇偶校验禁用

(4) 24位数据的LSB优先传输

图38.17显示了SPI数据寄存器(SPDR)和禁用奇偶校验的移位寄存器的传输操作，
SPI数据长度为24位，并选择LSB优先。

发送时，将发送缓冲器当前级的低24位（T23到T00）逐位重新排序，得到T00到T23的顺序，用于复制到移位寄存器。用于发送的数据从移位寄存器移出，从T00移出到T01，并按此顺序继续移到T23。

在接收中，接收到的数据通过移位寄存器的位[8]逐位移位。在输入所需的RSPCK周期数后收集R00至R23位时，将移位寄存器中的值复制到接收缓冲区。发送缓冲区的高8位存储在接收缓冲区的高8位中。在发送时将0写入位T31至T24会导致将0插入接收缓冲区的高8位。



Note: Output = MOSI (master)/MISO (slave), input = MISO (master)/MOSI (slave)

Figure 38.17 LSB-first transfer with 24-bit data and parity disabled

38.3.4.2 Operation when parity is enabled (SPCR2.SPPE = 1)

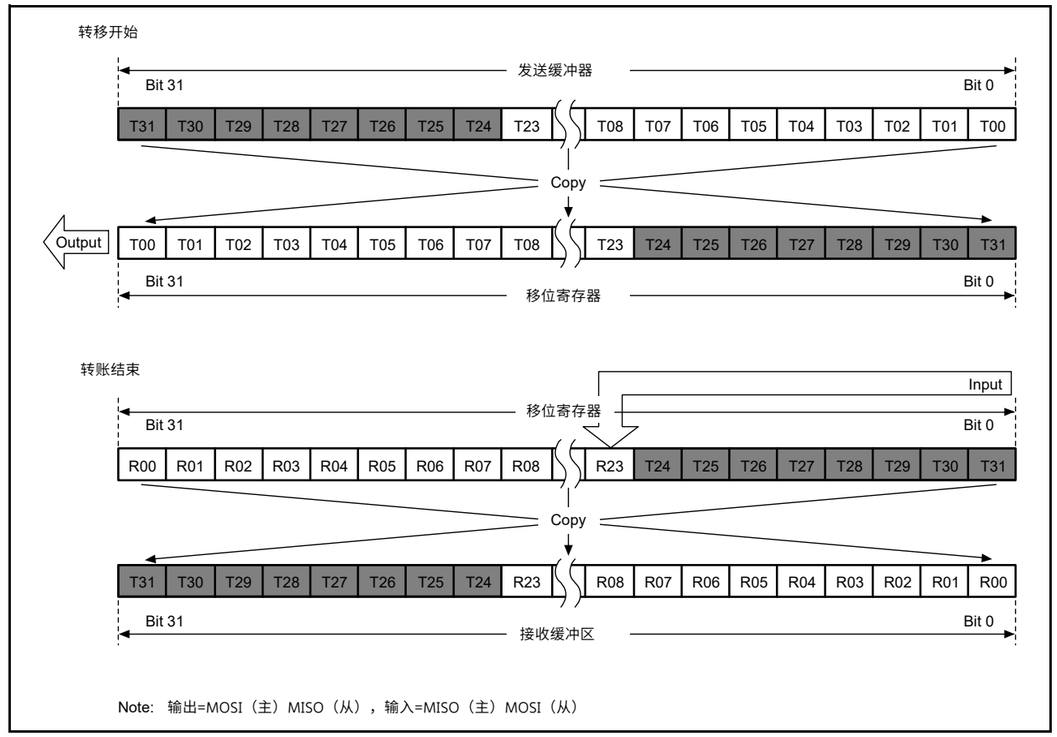
When parity is enabled, the lowest-order bit of the data for transmission becomes a parity bit. Hardware calculates the value of the parity bit.

(1) MSB-first transfer with 32-bit data

Figure 38.18 shows the transfer operations of the SPI Data Register (SPDR) and the shift register with parity enabled, an SPI data length of 32 bits, and MSB-first selected.

In transmission, the value of the parity bit (P) is calculated from bits T31 to T01. This replaces the final bit, T00, and the whole is copied to the shift register. Data is transmitted in the order T31, T30, …, T01, and P.

In reception, received data is shifted in bit-by-bit through bit [0] of the shift register. When the R31 to P bits are collected after input of the required number of RSPCK cycles, the value in the shift register is copied to the receive buffer. On copying of data to the shift register, data from R31 to P is checked for parity.



Note: 输出=MOSI（主）MISO（从），输入=MISO（主）MOSI（从）

Figure 38.17 LSB优先传输，24位数据和奇偶校验禁用

38.3.4.2 启用奇偶校验时的操作(SPCR2.SPPE=1)

启用奇偶校验时，传输数据的最低位变为奇偶校验位。硬件计算奇偶校验位的值。

(1) 32位数据的MSB优先传输

图38.18显示了SPI数据寄存器(SPDR)和启用奇偶校验的移位寄存器的传输操作，
SPI数据长度为32位，且MSB优先选择。

在传输中，奇偶校验位(P)的值是从位T31到T01计算的。这将替换最后一位T00，并将整体复制到移位寄存器中。数据按T31、T30、……、T01和P的顺序传输。

在接收时，接收到的数据通过移位寄存器的位[0]逐位移位。在输入所需数量的RSPCK周期后收集R31至P位时，将移位寄存器中的值复制到接收缓冲区。在将数据复制到移位寄存器时，检查从R31到P的数据的奇偶性。

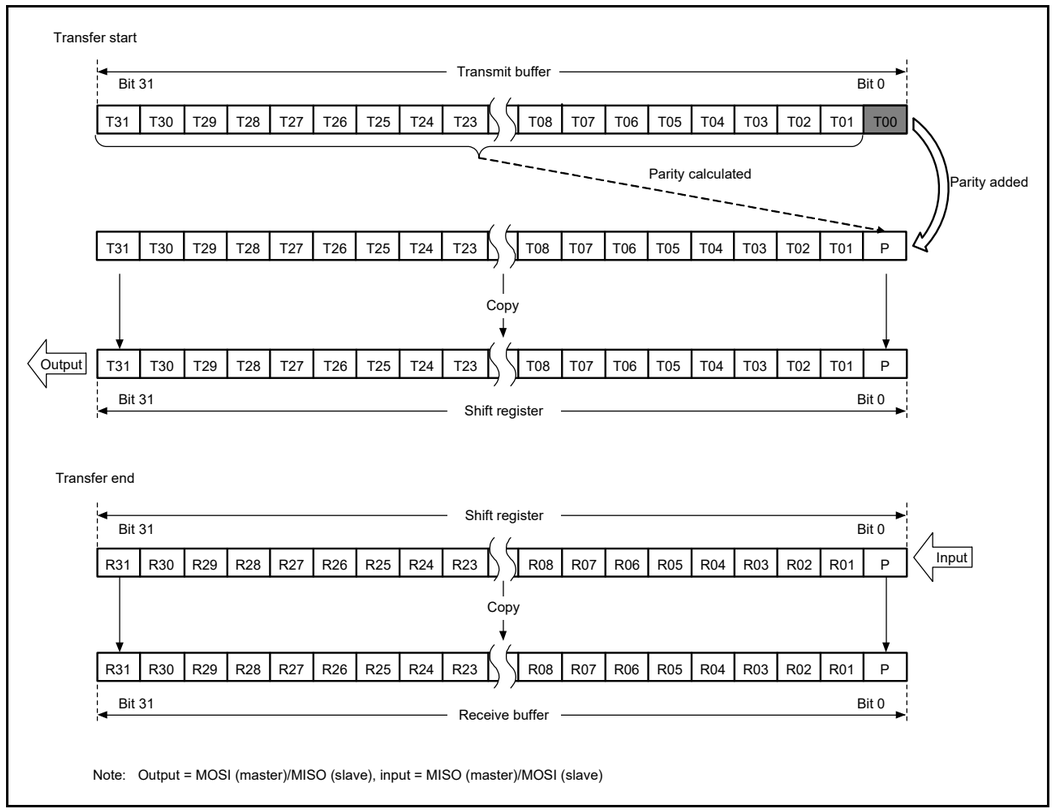


Figure 38.18 MSB-first transfer with 32-bit data and parity enabled

(2) MSB-first transfer with 24-bit data

Figure 38.19 shows the transfer operations of the SPI Data Register (SPDR) and the shift register with parity enabled, an SPI data length of 24 bits and MSB-first selected.

In transmission, the value of the parity bit (P) is calculated from bits T23 to T01. This replaces the final bit, T00, and the whole is copied to the shift register. Data is transmitted in the order T23, T22, …, T01, and P.

In reception, received data is shifted in bit-by-bit through bit [0] of the shift register. When the R23 to P bits are collected after input of the required number of RSPCK cycles, the value in the shift register is copied to the receive buffer. On copying of data to the shift register, data from R23 to P is checked for parity. The upper 8 bits of the transmit buffer are stored in the upper 8 bits of the receive buffer. Writing 0 to bits T31 to T24 at the time of transmission leads to 0 being inserted in the upper 8 bits of the receive buffer.

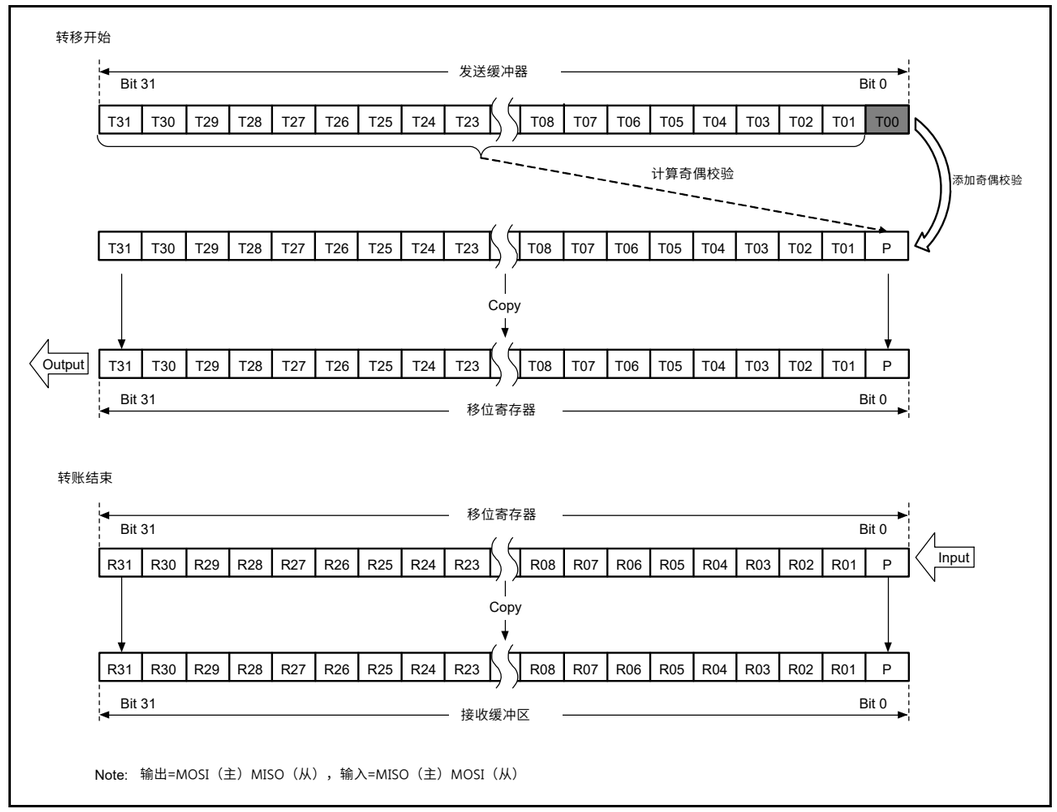


Figure 38.18 启用32位数据和奇偶校验的MSB优先传输

(2) 24位数据的MSB优先传输

图38.19显示了SPI数据寄存器(SPDR)和启用奇偶校验的移位寄存器的传输操作，
SPI数据长度为24位，选择MSB优先。

在传输中，奇偶校验位(P)的值是从位T23到T01计算的。这将替换最后一位T00，并将整体复制到移位寄存器中。数据按T23、T22、……、T01和P的顺序传输。

在接收时，接收到的数据通过移位寄存器的位[0]逐位移位。在输入所需数量的RSPCK周期后收集R23至P位时，将移位寄存器中的值复制到接收缓冲区。在将数据复制到移位寄存器时，会检查从R23到P的数据是否有奇偶性。发送缓冲区的高8位存储在接收缓冲区的高8位中。在发送时将0写入位T31至T24会导致将0插入接收缓冲区的高8位。

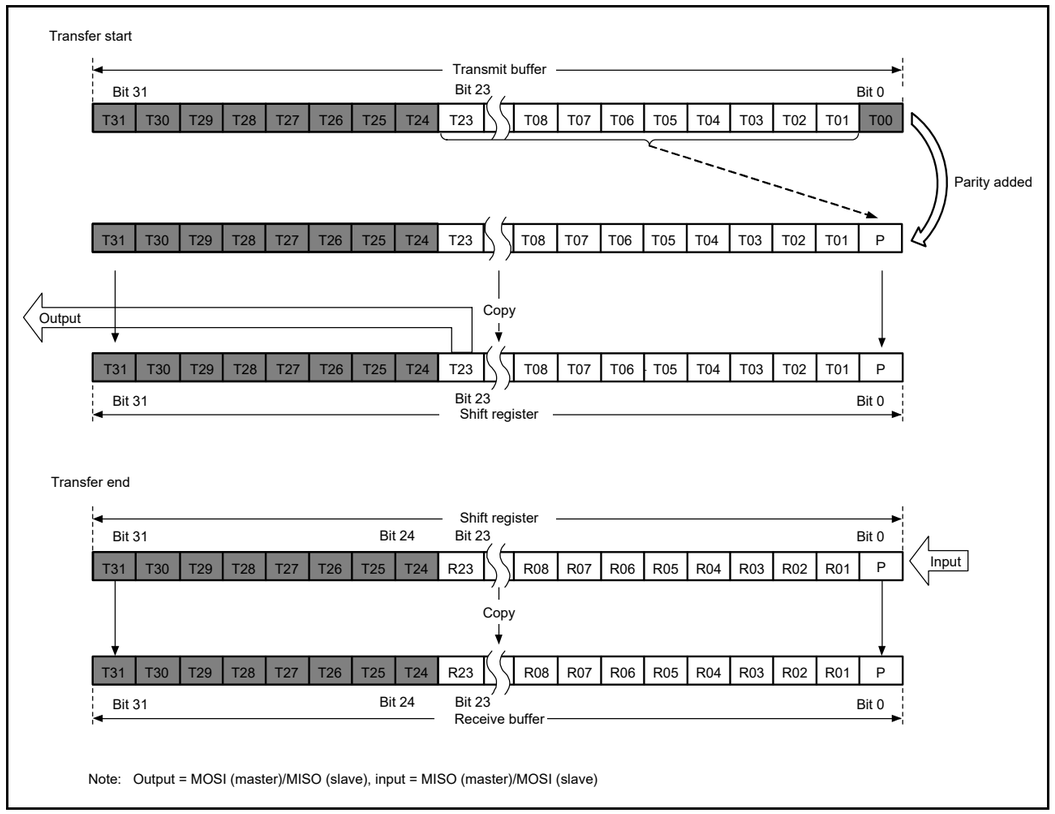


Figure 38.19 MSB-first transfer with 24-bit data and parity enabled

(3) LSB-first transfer with 32-bit data

Figure 38.20 shows the transfer operations of the SPI Data Register (SPDR) and the shift register with parity enabled, an SPI data length of 32 bits, and LSB-first selected.

In transmission, the value of the parity bit (P) is calculated from bits T30 to T00. This replaces the final bit, T31, and the whole is copied to the shift register. Data is transmitted in the order T00, T01, …, T30, and P.

In reception, received data is shifted in bit-by-bit through bit [0] of the shift register. When the R00 to P bits are collected after input of the required number of RSPCK cycles, the value in the shift register is copied to the receive buffer. On copying of data to the shift register, data from R00 to P is checked for parity.

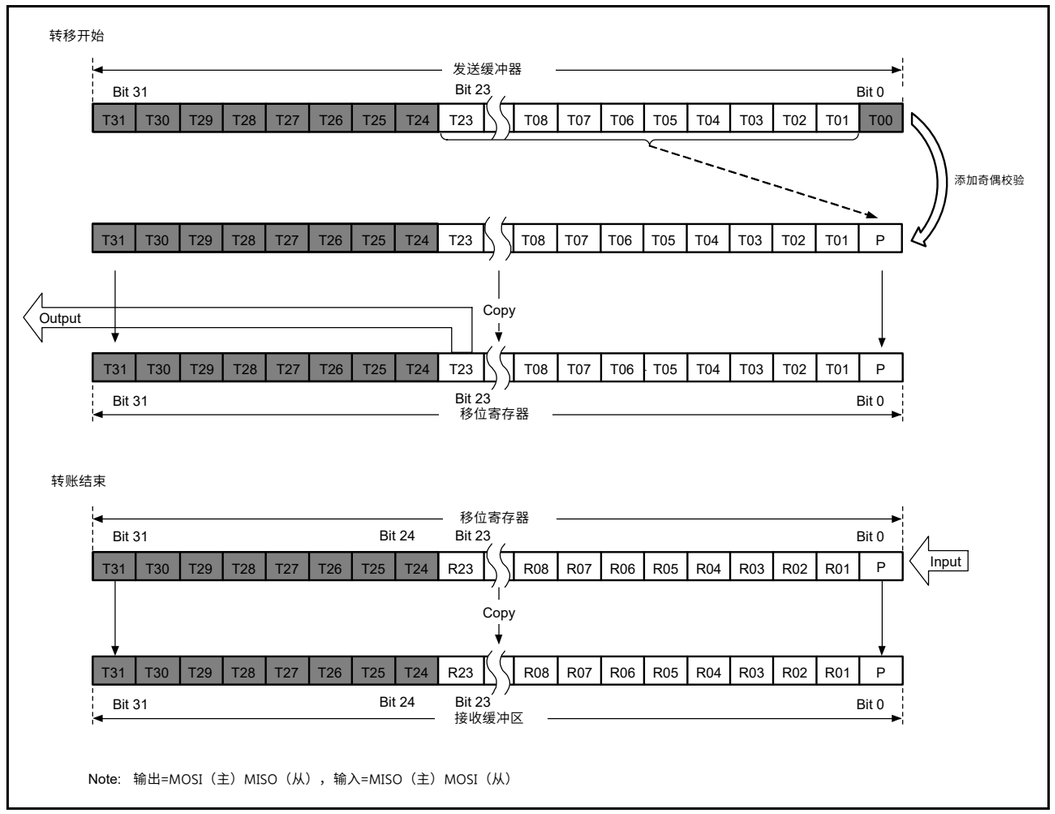


Figure 38.19 启用24位数据和奇偶校验的MSB优先传输

(3) 32位数据的LSB优先传输

图38.20显示了SPI数据寄存器(SPDR)和启用奇偶校验的移位寄存器的传输操作，
SPI数据长度为32位，并选择LSB-first。

在传输中，奇偶校验位(P)的值是从位T30到T00计算的。这将替换最后一位T31，并将整体复制到移位寄存器。
数据按T00、T01、……、T30和P的顺序传输。

在接收时，接收到的数据通过移位寄存器的位[0]逐位移位。在输入所需数量的RSPCK周期后收集R00至P位时，
将移位寄存器中的值复制到接收缓冲区。在将数据复制到移位寄存器时，检查从R00到P的数据的奇偶性。

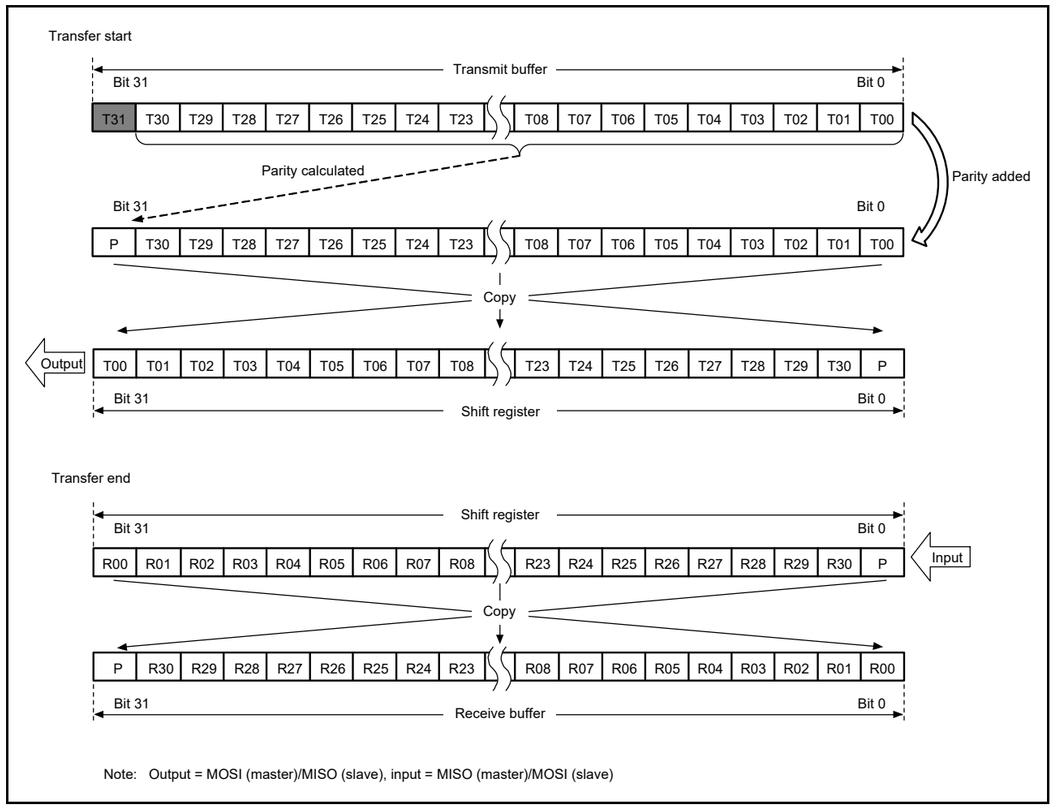


Figure 38.20 LSB-first transfer with 32-bit data and parity enabled

(4) LSB-first transfer with 24-bit data

Figure 38.21 shows the transfer operations of the SPI Data Register (SPDR) and the shift register with parity enabled, an SPI data length of 24 bits, and LSB-first selected.

In transmission, the value of the parity bit (P) is calculated from bits T22 to T00. This replaces the final bit, T23, and the whole is copied to the shift register. Data is transmitted in the order T00, T01, …, T22, and P.

In reception, received data is shifted in bit-by-bit through bit [8] of the shift register. When the R00 to P bits are collected after input of the required number of RSPCK cycles, the value in the shift register is copied to the receive buffer. On copying of data to the shift register, data from R00 to P is checked for parity. The upper 8 bits of the transmit buffer are stored in the upper 8 bits of the receive buffer. Writing 0 to bits T31 to T24 at the time of transmission leads to 0 being inserted in the upper 8 bits of the receive buffer.

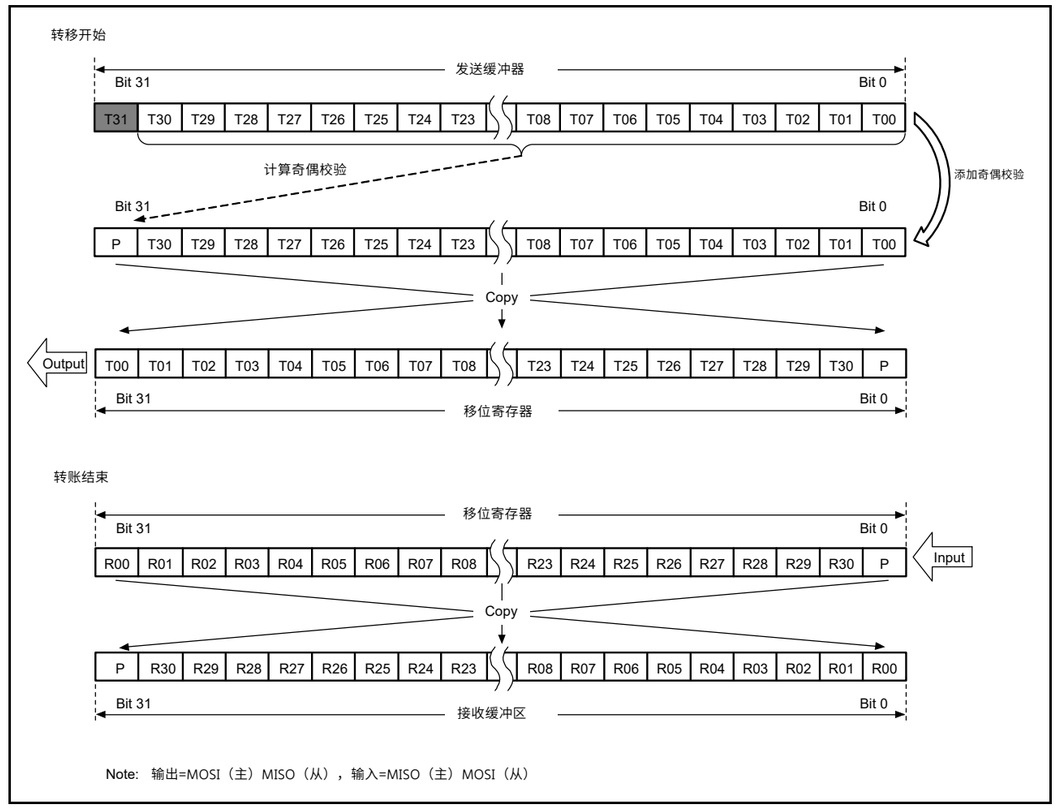


Figure 38.20 启用32位数据和奇偶校验的LSB优先传输

(4) 24位数据的LSB优先传输

图38.21显示了SPI数据寄存器(SPDR)和启用奇偶校验的移位寄存器的传输操作，SPI数据长度为24位，并选择LSB优先。

在传输中，奇偶校验位(P)的值是从位T22到T00计算的。这将替换最后一位T23，并将整体复制到移位寄存器中。数据按T00、T01、……、T22和P的顺序传输。

在接收中，接收到的数据通过移位寄存器的位[8]逐位移位。在输入所需数量的RSPCK周期后收集R00至P位时，将移位寄存器中的值复制到接收缓冲区。在将数据复制到移位寄存器时，检查从R00到P的数据的奇偶性。发送缓冲区的高8位存储在接收缓冲区的高8位中。在发送时将0写入位T31至T24会导致将0插入接收缓冲区的高8位。

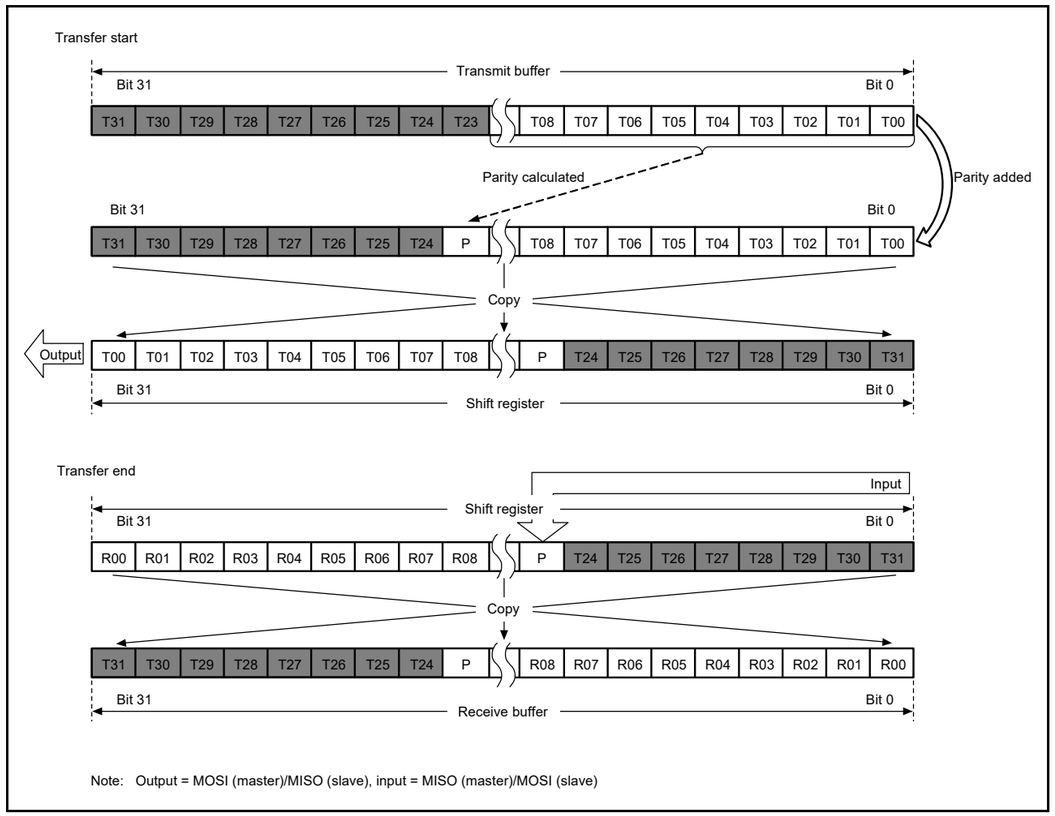


Figure 38.21 LSB-first transfer with 24-bit data and parity enabled

38.3.5 Transfer Formats

38.3.5.1 Transfer format when CPHA = 0

Figure 38.22 shows an example transfer format for the serial transfer of 8-bit data when the SPCMDm.CPHA bit is 0. Do not perform clock synchronous operation (SPCR.SPMS = 1) when the SPI operates in slave mode (SPCR.MSTR = 0) and the CPHA bit is 0. In the figure, RSPCKn (CPOL = 0) indicates the RSPCKn signal waveform when the SPCMDm.CPOL bit is 0, and RSPCKn (CPOL = 1) indicates the RSPCKn signal waveform when the CPOL bit is 1. The sampling timing represents the timing at which the SPI fetches serial transfer data into the shift register. The I/O directions of the signals depend on the SPI settings. For details, see section 38.3.2, Controlling the SPI Pins.

When the SPCMDm.CPHA bit is 0, the driving of valid data to the MOSIn and MISOn signals commences on an SSLni signal assertion. The first RSPCKn signal change that occurs after the SSLni signal assertion becomes the first transfer data fetch. After this, data is sampled every 1 RSPCK cycle. The change timing for MOSIn and MISOn signals is 1/2 RSPCK cycles after the transfer data fetch timing. The CPOL bit setting does not affect the RSPCK signal operation timing as it only affects the signal polarity.

t1 denotes the period from an SSLni signal assertion to RSPCKn oscillation (RSPCK delay). t2 denotes the period from the termination of RSPCKn oscillation to an SSLni signal negation (SSL negation delay). t3 denotes the period in which SSLni signal assertion is suppressed for the next transfer after the end of serial transfer (next-access delay). t1, t2, and t3 are controlled by a master device running on the SPI system. For a description of t1, t2, and t3 when the SPI is in master mode, see section 38.3.10.1, Master mode operation.

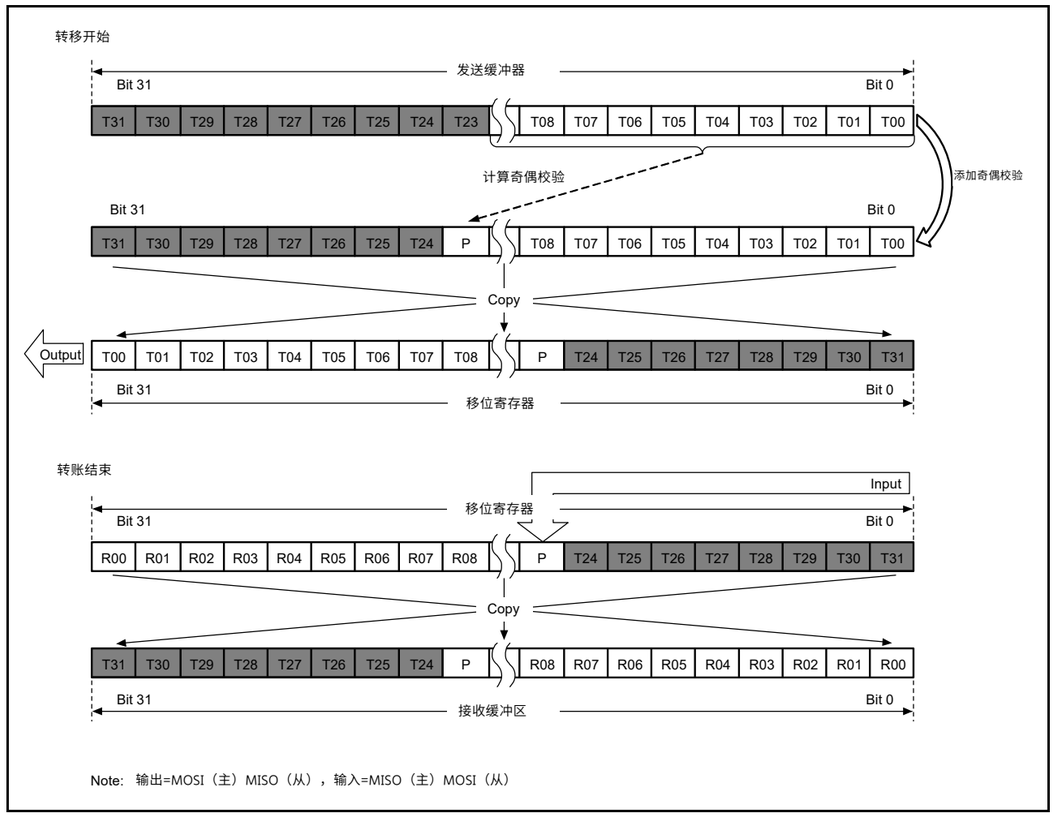


Figure 38.21 启用24位数据和奇偶校验的LSB优先传输

38.3.5 传输格式

38.3.5.1 CPHA=0时的传输格式

图38.22显示了当SPCMDm.CPHA位为0时串行传输8位数据的示例传输格式。当SPI在从机模式下运行时（SPCR.MSTR=0），CPHA位为0。图中，RSPCKn(CPOL=0)表示SPCMDm.CPOL位为0时的RSPCKn信号波形，RSPCKn(CPOL=1)表示CPOL位为0时的RSPCKn信号波形1.采样时序表示SPI将串行传输数据取入移位寄存器的时序。信号的IO方向取决于SPI设置。有关详细信息，请参见第38.3.2节，控制SPI引脚。

当SPCMDm.CPHA位为0时，有效数据驱动到MOSIn和MISOn信号在SSLni信号断言时开始。在SSLni信号断言之后发生的第一个RSPCKn信号变化成为第一次传输数据获取。此后，每1个RSPCK周期对数据进行采样。MOSIn和MISOn信号的变化时序是传输数据获取时序之后的12RSPCK周期。CPOL位设置不影响RSPCK信号操作时序，因为它只影响信号极性。

t1表示从SSLni信号断言到RSPCKn振荡（RSPCK延迟）的周期。t2表示从RSPCKn振荡终止到SSLni信号否定（SSL否定延迟）的周期。t3表示在串行传输结束后（下一次访问延迟）为下一次传输抑制SSLni信号断言的时间段。t1、t2和t3由在SPI系统上运行的主设备控制。有关SPI处于主机模式时的t1、t2和t3的说明，请参阅第38.3.10.1节，主机模式操作。

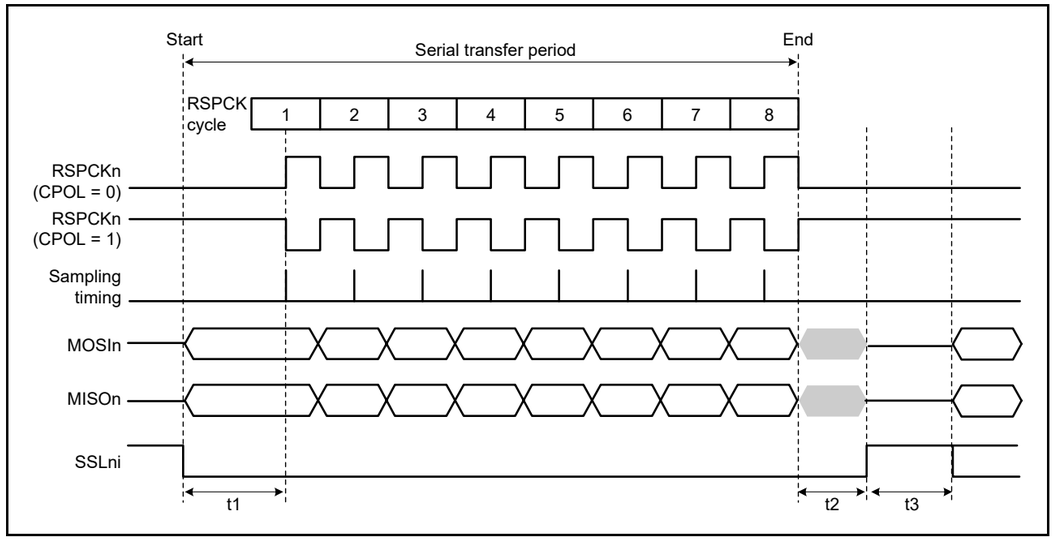


Figure 38.22 SPI transfer format when CPHA = 0

38.3.5.2 When CPHA = 1

Figure 38.23 shows an example transfer format for the serial transfer of 8-bit data when the SPCMDm.CPHA bit is 1. However, when the SPCR.SPMS bit is 1, the SSLni signals are not used, and only the three signals RSPCKn, MOSIn, and MISOn handle communications. In Figure 38.23, RSPCK (CPOL = 0) indicates the RSPCKn signal waveform when the SPCMDm.CPOL bit is 0; RSPCK (CPOL = 1) indicates the RSPCKn signal waveform when the CPOL bit is 1. The sampling timing represents the timing at which the SPI fetches serial transfer data into the shift register. The I/O directions of the signals depend on the SPI mode (master or slave). For details, see section 38.3.2, Controlling the SPI Pins.

When the SPCMDm.CPHA bit is 1, the driving of invalid data to the MISOn signal commences on an SSLni signal assertion. The output of valid data to the MOSIn and MISOn signals commences at the first RSPCKn signal change that occurs after the SSLni signal assertion. After this, data is updated every 1 RSPCK cycle. The transfer data fetch timing is 1/2 RSPCK cycles after the data update timing. The SPCMDm.CPOL bit setting does not affect the RSPCKn signal operation timing; it only affects the signal polarity.

t1, t2, and t3 are the same as those when CPHA = 0. For a description of t1, t2, and t3 when the SPI of the MCU is in master mode, see section 38.3.10.1, Master mode operation.

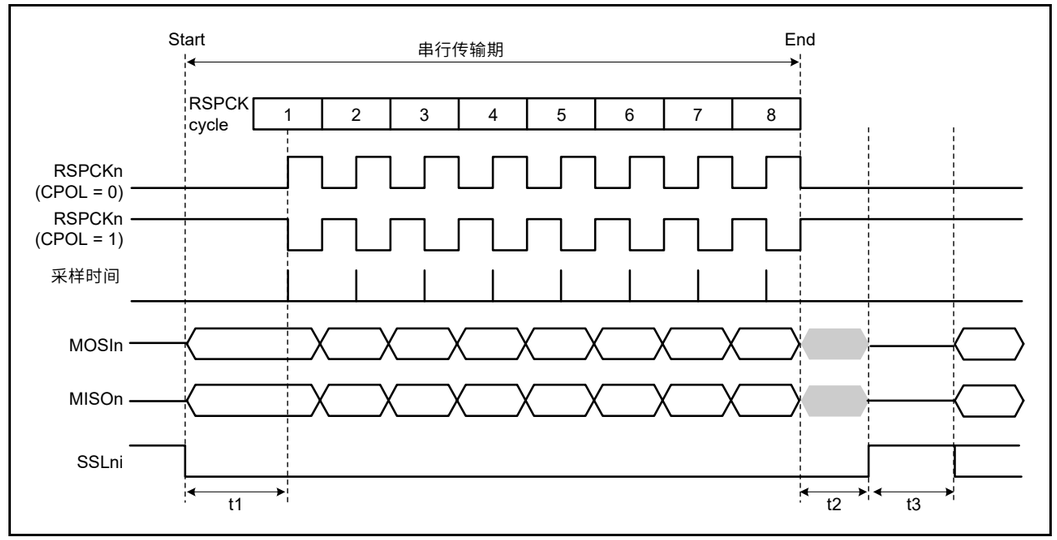


Figure 38.22 CPHA=0时的SPI传输格式

38.3.5.2 When CPHA = 1

图38.23显示了SPCMDm.CPHA位为1时串行传输8位数据的示例传输格式。然而，当SPCR.SPMS位为1时，不使用SSLni信号，仅使用三个信号RSPCKn，MOSIn和MISon处理通信。图38.23中，RSPCK(CPOL=0)表示SPCMDm.CPOL位为0时的RSPCKn信号波形；RSPCK(CPOL=1)表示CPOL位为1时的RSPCKn信号波形。采样时序表示SPI将串行传输数据取入移位寄存器的时序。信号的IO方向取决于SPI模式（主机或从机）。有关详细信息，请参见第38.3.2节，控制SPI引脚。

当SPCMDm.CPHA位为1时，在SSLni信号断言时开始将无效数据驱动到MIOn信号。在SSLni信号断言之后发生的第一个RSPCKn信号变化时，开始向MOSIn和MISOn信号输出有效数据。此后，每1个RSPCK周期更新一次数据。传输数据获取时序是数据更新时序之后的12个RSPCK周期。SPCMDm.CPOL位设置不影响RSPCKn信号操作时序；它只影响信号极性。

t1、t2、t3与CPHA=0时相同。关于MCU的SPI处于主机模式时的t1、t2和t3说明，请参见第38.3.10.1节，主机模式操作。

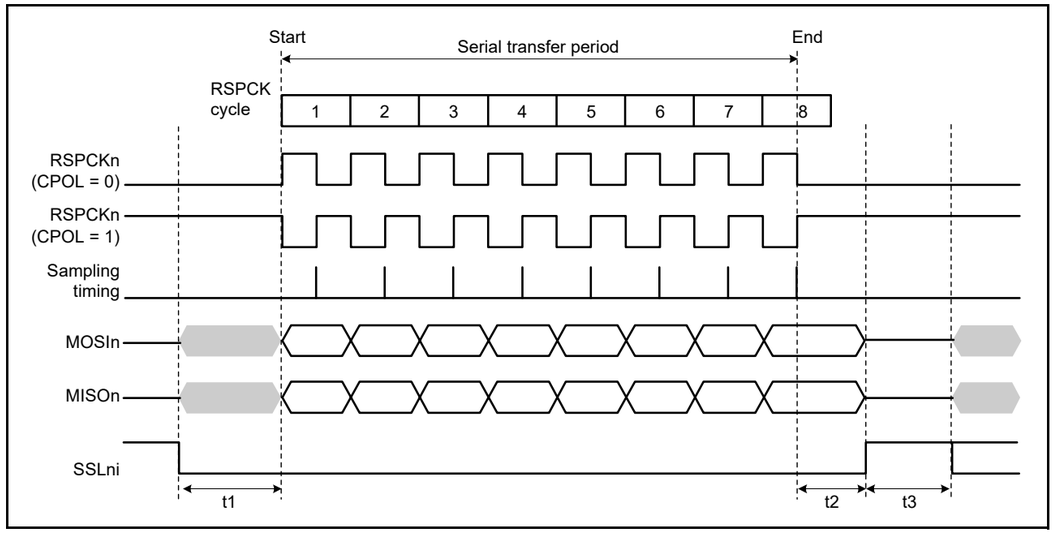


Figure 38.23 SPI transfer format when CPHA = 1

38.3.6 Data Transfer Modes

Full-duplex synchronous serial communications or transmit operations can only be selected in the communications operating mode select bit (SPCR.TXMD). The SPDR/SPDR_HA access shown in Figure 38.24 and Figure 38.25 indicate the condition of access to the register, where W denotes a write cycle.

38.3.6.1 Full-duplex synchronous serial communications (SPCR.TXMD = 0)

Figure 38.24 shows an example of operation where the communications operating mode select bit (SPCR.TXMD) is set to 0. In this example, the SPI performs an 8-bit serial transfer when SPDCR.SPFC[1:0] bits are 00b, the SPCMDm.CPHA bit is 1, and the SPCMDm.CPOL bit is 0. The numbers given for RSPCKn in the waveform represent the number of RSPCK cycles, indicating the number of transferred bits.

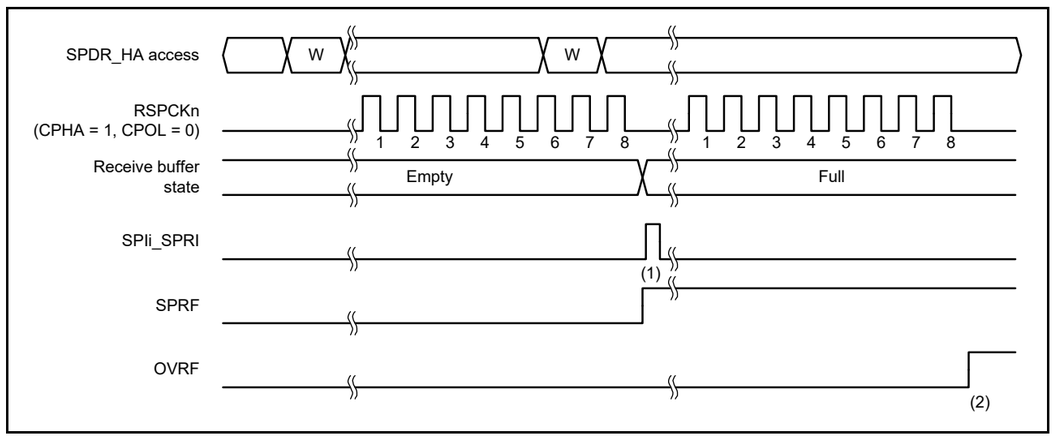


Figure 38.24 Operation example when SPCR.TXMD = 0

The operation of the flags at times (1) and (2) in the figure is as follows:

1. When a serial transfer ends with the receive buffer of SPDR_HA empty, the SPI generates a receive buffer full interrupt request (SPIi_SPRI) (the SPI sets the SPSR.SPRF flag to 1) and copies the received data in the shift

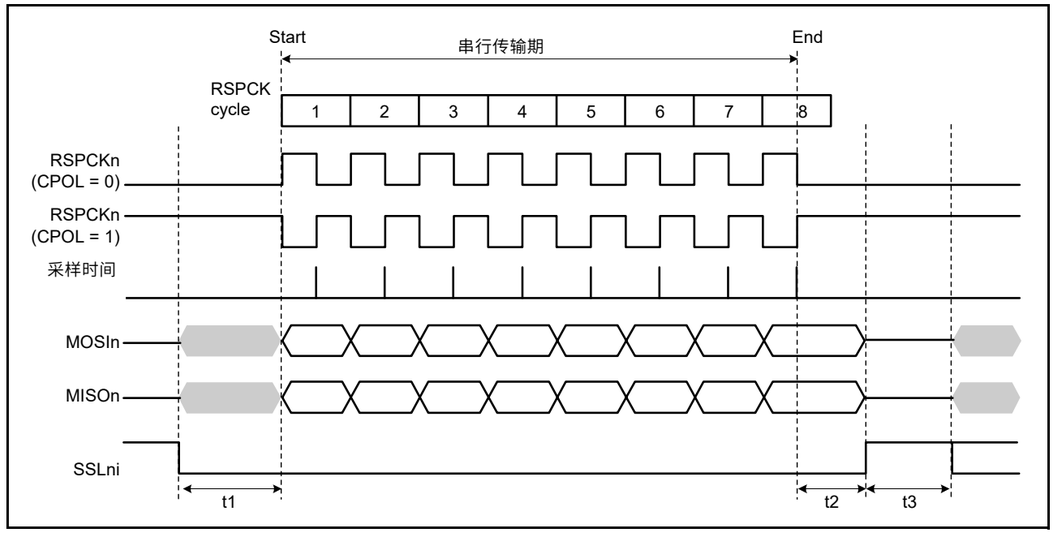


Figure 38.23 CPHA=1时的SPI传输格式

38.3.6 数据传输模式

全双工同步串行通信或发送操作只能在通信操作模式选择位(SPCR.TXMD)中选择。图38.24和图38.25所示的SPDRSPDR_HA访问表示访问寄存器的条件，其中W表示写周期。

38.3.6.1 全双工同步串行通信(SPCR.TXMD=0)

图38.24显示了通信操作模式选择位(SPCR.TXMD)设置为0的操作示例。在此示例中，当SPDCR.SPFC[1:0]位为00b时，SPI执行8位串行传输，SPCMDm.CPHA位为1，SPCMDm.CPOL位为0。波形中为RSPCKn给出的数字表示RSPCK周期数，表示传输的位数。

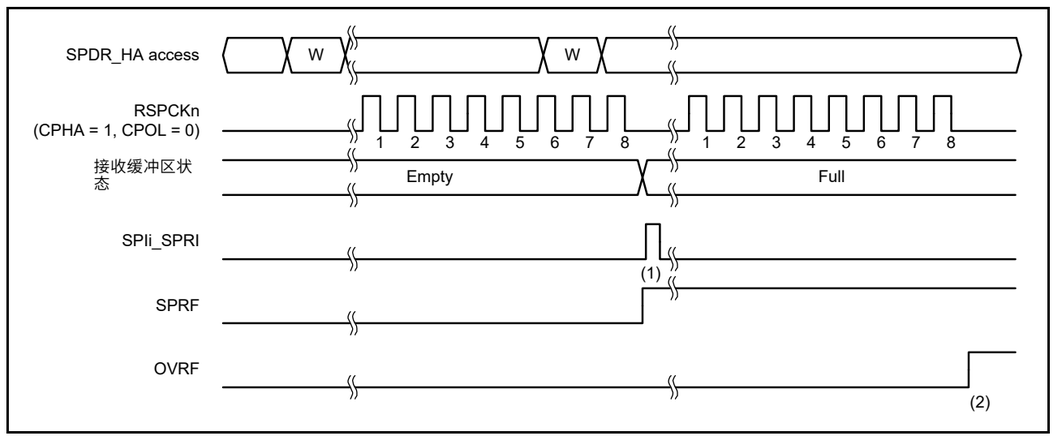


Figure 38.24 SPCR.TXMD=0时的操作示例

图中（1）和（2）时刻flags的操作如下：

1. 当串行传输结束且SPDR_HA的接收缓冲区为空时，SPI产生接收缓冲区满中断请求（SPIi_SPRI）（SPI将SPSR.SPRF标志设置为1）并将接收到的数据复制到移位中

register to the receive buffer.

2. When a serial transfer ends with the receive buffer of SPDR_HA holding data that was received in the previous serial transfer, the SPI sets the SPSR.OVRF flag to 1 and discards the received data in the shift register.

38.3.6.2 Transmit operations only (SPCR.TXMD = 1)

Figure 38.25 shows an example of operation where the communications operating mode select bit (SPCR.TXMD) is set to 1. In this example, the SPI performs an 8-bit serial transfer when SPDCR.SPFC[1:0] bits are 00b, the SPCMDm.CPHA bit is 1, and the SPCMDm.CPOL bit is 0. The numbers given for RSPCKn in the waveform represent the number of RSPCK cycles, indicating the number of transferred bits.

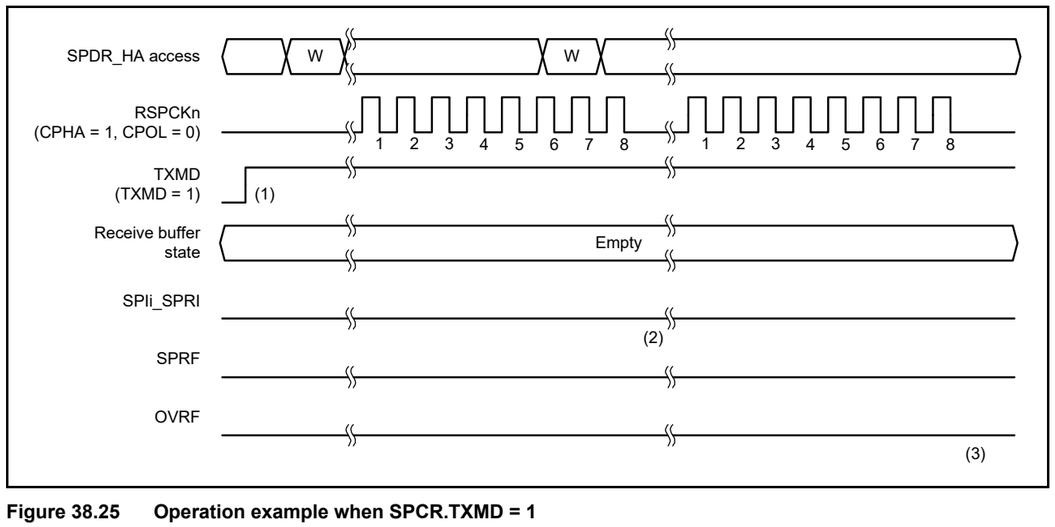


Figure 38.25 Operation example when SPCR.TXMD = 1

The operation of the flags at times (1) to (3) in the figure is as follows:

1. Make sure there is no data left in the receive buffer (the SPSR.SPRF flag is 0) and the SPSR.OVRF flag is 0 before entering transmit-only mode (SPCR.TXMD = 1).
2. When a serial transfer ends with the receive buffer of SPDR_HA empty, if the transmit-only mode is selected (SPCR.TXMD = 1), the SPSR.SPRF flag retains the value of 0, and the SPI does not copy the data in the shift register to the receive buffer.
3. Because the receive buffer of SPDR_HA does not hold data that was received in the previous serial transfer, even when a serial transfer ends, the SPSR.OVRF flag retains the value of 0, and the data in the shift register is not copied to the receive buffer.

In transmit-only mode (SPCR.TXMD = 1), the SPI transmits data but does not receive data. Therefore, the SPSR.SPRF and SPSR.OVRF flags remain 0 at times (1) to (3).

38.3.7 Transmit Buffer Empty and Receive Buffer Full Interrupts

Figure 38.26 and Figure 38.27 show examples of operation of the transmit buffer empty interrupt (SPIi_SPTI) and the receive buffer full interrupt (SPIi_SPRI). The SPDR_HA register accesses shown in these figures indicate the condition of access to the register, where W denotes a write cycle and R a read cycle. In the example in Figure 38.26, the SPI performs an 8-bit serial transfer when SPCR.TXMD bit is 0, the SPDCR.SPFC[1:0] bits are 00b, the SPCMDm.CPHA bit is 0, and the SPCMDm.CPOL bit is 0. In the example in Figure 38.27, the SPI performs an 8-bit serial transfer when SPCR.TXMD bit is 0, the SPDCR.SPFC[1:0] bits are 00b, the SPCMDm.CPHA bit is 1, and the SPCMDm.CPOL bit is 0. The numbers given for RSPCKn in the waveform represent the number of RSPCK cycles, indicating the number of transferred bits.

注册到接收缓冲区。

2. 当串行传输结束时，SPDR_HA的接收缓冲区保存了前一次串行传输中接收到的数据，SPI将SPSR.OVRF标志设置为1，并丢弃移位寄存器中接收到的数据。

38.3.6.2 仅发送操作(SPCR.TXMD=1)

图38.25显示了通信操作模式选择位(SPCR.TXMD)设置为1的操作示例。在此示例中，当SPDCR.SPFC[1:0]位为00b时，SPI执行8位串行传输，SPCMDm.CPHA位为1，SPCMDm.CPOL位为0。波形中为RSPCKn给出的数字表示RSPCK周期数，表示传输的位数。

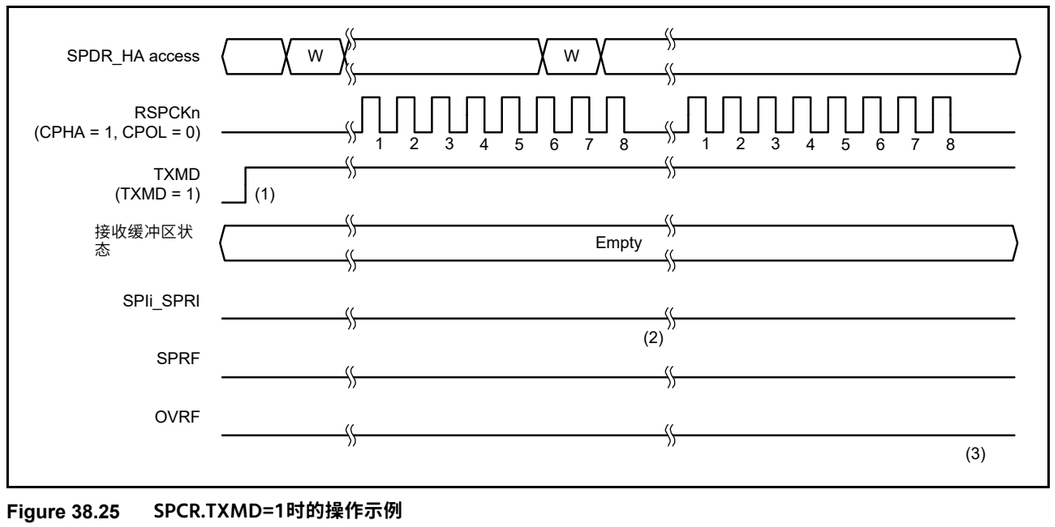


Figure 38.25 SPCR.TXMD=1时的操作示例

图中（1）到（3）时刻flags的操作如下：

1. 在进入仅发送模式（SPCR.TXMD=1）之前，确保接收缓冲区中没有数据（SPSR.SPRF标志为0）且SPSR.OVRF标志为0。
2. 当串行传输结束且SPDR_HA的接收缓冲区为空时，如果选择了仅发送模式（SPCR.TXMD=1），则SPSR.SPRF标志保持值为0，SPI不会复制移位寄存器到接收缓冲器。
3. 因为SPDR_HA的接收缓冲区不保存之前串行传输中接收到的数据，所以即使串行传输结束，SPSR.OVRF标志保持值0，移位寄存器中的数据不会复制到接收缓冲。

在仅发送模式（SPCR.TXMD=1）下，SPI发送数据但不接收数据。因此，SPSR.SPRF和SPSR.OVRF标志在时间(1)到(3)处保持为0。

38.3.7 发送缓冲区空和接收缓冲区满中断

图38.26和图38.27显示了发送缓冲区空中断(SPIi_SPTI)和接收缓冲区满中断(SPIi_SPRI)的操作示例。这些图中显示的SPDR_HA寄存器访问表示对寄存器的访问条件，其中W表示写周期，R表示读周期。在图38.26的示例中，当SPCR.TXMD位为0、SPDCR.SPFC[1:0]位为00b、SPCMDm.CPHA位为0、SPCMDm.CPOL时SPI执行8位串行传输bit为0。在图38.27的示例中，当SPCR.TXMD位为0、SPDCR.SPFC[1:0]位为00b、SPCMDm.CPHA位为1时，SPI执行8位串行传输，并且SPCMDm.CPOL位为0。波形中为RSPCKn给出的数字表示RSPCK周期数，表示传输的位数。

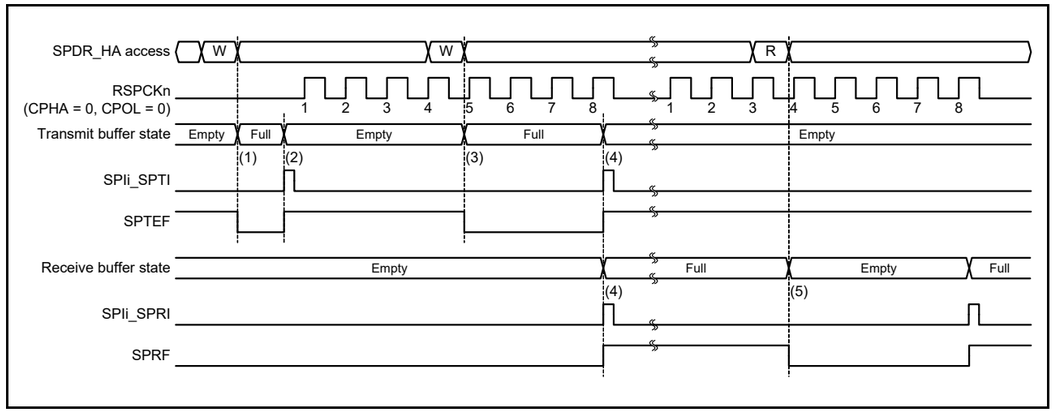


Figure 38.26 Operation example of the SPIi_SPTI and SPIi_SPRI interrupts when CPHA = 0 and CPOL = 0

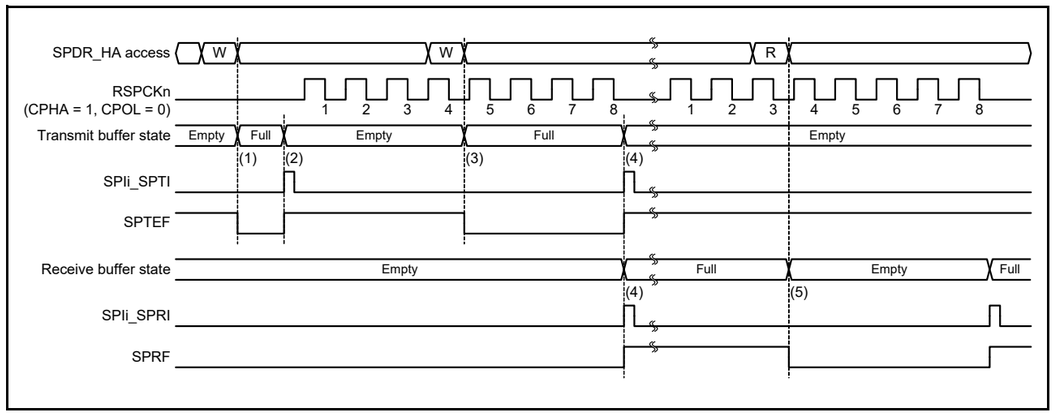


Figure 38.27 Operation example of the SPIi_SPTI and SPIi_SPRI interrupts when CPHA = 1 and CPOL = 0

The operation of the SPI at times (1) to (5) in the figure is as follows:

1. When transmit data is written to SPDR_HA and when the transmit buffer of SPDR_HA is empty (data for the next transfer is not set), the SPI writes data to the transmit buffer and clears the SPSR.SPTEF flag to 0.
2. If the shift register is empty, the SPI copies the data in the transmit buffer to the shift register, generates a transmit buffer empty interrupt request (SPIi_SPTI), and sets the SPSR.SPTEF flag to 1. How a serial transfer is started depends on the mode of the SPI. For details, see section 38.3.10, SPI Operation, and section 38.3.11, Clock Synchronous Operation.
3. When transmit data is written to SPDR_HA either by the transmit buffer empty interrupt routine, or by the processing of the transmit buffer empty state using the SPTEF flag, the SPI writes data to the transmit buffer and clears the SPTEF flag to 0. Because the data being transferred serially is stored in the shift register, the SPI does not copy the data in the transmit buffer to the shift register.
4. When the serial transfer ends and the receive buffer of SPDR_HA is empty, the SPI copies the receive data in the shift register to the receive buffer, generates a receive buffer full interrupt request (SPIi_SPRI), and sets the SPRF flag to 1. Because the shift register becomes empty on completion of the serial transfer, when the transmit buffer is full before the serial transfer ended, the SPI sets the SPTEF flag to 1 and copies data in the transmit buffer to the shift register. Even when received data is not copied from the shift register to the receive buffer in an overrun error status, on completion of the serial transfer, the SPI determines that the shift register is empty, so data transfer from the transmit buffer to the shift register is enabled.

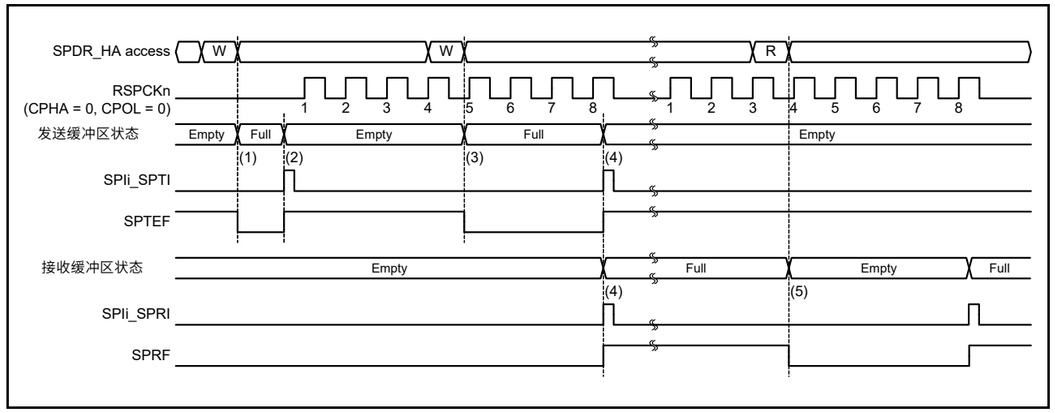


Figure 38.26 CPHA=0和CPOL=0时SPIi_SPTI和SPIi_SPRI中断的操作示例

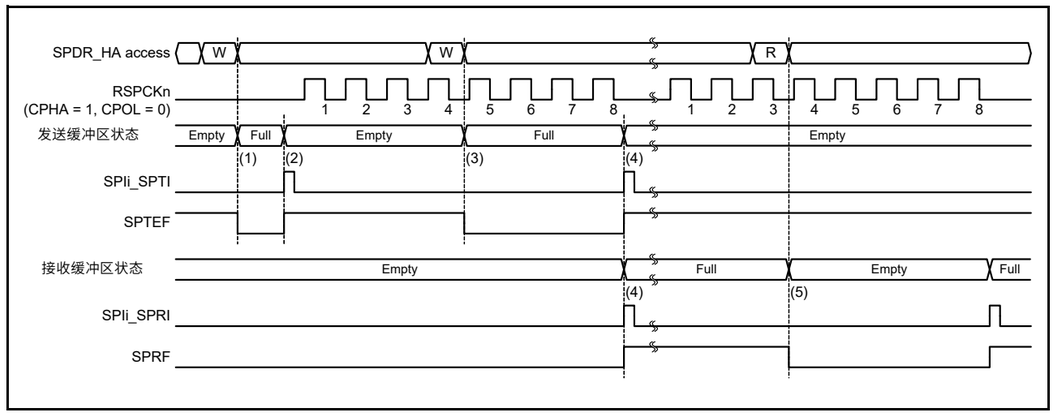


Figure 38.27 CPHA=1和CPOL=0时SPIi_SPTI和SPIi_SPRI中断的操作示例

图中（1）到（5）时刻SPI的操作如下：

1. 当发送数据写入SPDR_HA且SPDR_HA的发送缓冲区为空（未设置下一次传输的数据）时，SPI将数据写入发送缓冲区并将SPSR.SPTEF标志清除为0。
2. 如果移位寄存器为空，则SPI将发送缓冲区中的数据复制到移位寄存器，产生发送缓冲区空中断请求（SPIi_SPTI），并将SPSR.SPTEF标志设置为1。如何启动串行传输取决于SPI的模式。有关详细信息，请参见第38.3.10节，SPI操作和第38.3.11节，时钟同步操作。
3. 当发送数据被发送缓冲区空中断程序或使用SPTEF标志处理发送缓冲区空状态写入SPDR_HA时，SPI将数据写入发送缓冲区并将SPTEF标志清除为0。因为数据串行传输的数据存储在移位寄存器中，SPI不会将发送缓冲区中的数据复制到移位寄存器中。
4. 当串行传输结束且SPDR_HA的接收缓冲区为空时，SPI将移位寄存器中的接收数据复制到接收缓冲区，产生接收缓冲区满中断请求（SPIi_SPRI），并将SPRF标志设置为1。串行传输完成后移位寄存器变为空，当串行传输结束前发送缓冲区已满时，SPI将SPTEF标志设置为1，并将发送缓冲区中的数据复制到移位寄存器。即使在溢出错误状态下没有将接收到的数据从移位寄存器复制到接收缓冲区，在串行传输完成时，SPI会确定移位寄存器为空，因此从发送缓冲区到移位寄存器的数据传输是启用。

5. When SPDR_HA is read either by the receive buffer full interrupt routine or processing of the receive buffer full state using the SPRF flag, the receive data can be read.

If SPDR_HA is written to when the transmit buffer holds data that is not yet transmitted (the SPTEF flag is 0), the SPI does not update data in the transmit buffer. When writing to SPDR_HA, always use either a transmit buffer empty interrupt request or processing of the transmit buffer empty interrupt using the SPTEF flag. To use a transmit buffer empty interrupt, set the SPTIE bit in SPCR to 1. If the SPI function is disabled (the SPCR.SPE bit is 0), set the SPTIE bit to 0.

When serial transfer ends and the receive buffer is full (the SPRF flag is 1), the SPI does not copy data from the shift register to the receive buffer, and it detects an overrun error (see section 38.3.8, Error Detection). To prevent a receive data overrun error, read the received data using a receive buffer full interrupt request before the next serial transfer ends. To use an SPI receive buffer full interrupt, set the SPCR.SPRIE bit to 1.

Transmission and reception interrupts or the associated IELSRn.IR flags (where n is the interrupt vector number) in the ICU can be used to confirm the states of the transmit and receive buffers.

Similarly, the SPTEF and SPRF flags can be used to confirm the states of the transmit and receive buffers. See section 14, Interrupt Controller Unit (ICU) for the interrupt vector numbers.

38.3.8 Error Detection

In normal SPI serial transfers, data written to the transmit buffer of SPDR/SPDR_HA is transmitted, and received data can be read from the receive buffer of SPDR/SPDR_HA. In some cases non-normal transfers can be executed when SPDR/SPDR_HA is accessed, depending on the status of the transmit or receive buffer or the status of the SPI at the beginning or end of serial transfer.

If a non-normal transfer operation occurs, the SPI detects the event as an underrun error, overrun error, parity error, or mode fault error. Table 38.8 lists the relationship between non-normal transfer operations and the SPI error detection function.

Table 38.8 Relationship between non-normal transfer operations and SPI error detection

Operation	Occurrence condition	SPI operation	Error detection
1	SPDR/SPDR_HA is written when the transmit buffer is full.	• Keeps the contents of the transmit buffer • Missing write data.	None
2	SPDR/SPDR_HA is read when the receive buffer is empty.	Outputs the contents of the receive buffer and previously received data.	None
3	Serial transfer is started in slave mode when the SPI is not able to transmit data.	• Suspends serial transfer • Missing transmit and receive data • Stops driving of the MISOA output signal • Disables the SPI function.	Underrun error
4	Serial transfer terminates when the receive buffer is full.	• Keeps the contents of the receive buffer • Missing receive data.	Overrun error
5	An incorrect parity bit is received when performing full-duplex synchronous serial communications with the parity function enabled.	Asserts the parity error flag.	Parity error
6	The SSLn0 input signal is asserted when the serial transfer is idle in multi-master mode.	• Stops driving of the RSPCKn, MOSIn, SSLn1 to SSLn3 output signals • Disables the SPI function.	Mode fault error
7	The SSLn0 input signal is asserted during serial transfer in multi-master mode.	• Suspends serial transfer • Missing transmit and receive data • Stops driving of the RSPCKn, MOSIn, SSLn1 to SSLn3 output signals • Disables the SPI function.	Mode fault error
8	The SSLn0 input signal is negated during serial transfer in slave mode.	• Suspends serial transfer • Missing transmit and receive data • Stops driving of the MISOn output signal • Disables the SPI function.	Mode fault error

In operation 1 described in Table 38.8, the SPI does not detect an error. To prevent data omission during the writing to SPDR/SPDR_HA, write operations to SPDR/SPDR_HA must be executed using a transmit buffer empty interrupt

5. 当接收缓冲区满中断例程或使用SPRF标志处理接收缓冲区满状态读取SPDR_HA时，可以读取接收数据。

如果在发送缓冲区保存尚未发送的数据时写入SPDR_HA（SPTEF标志为0），则SPI不会更新发送缓冲区中的数据。写入SPDR_HA时，始终使用发送缓冲区空中断请求或使用SPTEF标志处理发送缓冲区空中断。要使用发送缓冲区空中断，请将SPCR中的SPTIE位设置为1。如果禁用SPI功能（SPCR.SPE位为0），请将SPTIE位设置为0。

当串行传输结束且接收缓冲区已满（SPRF标志为1）时，SPI不会将数据从移位寄存器复制到接收缓冲区，它会检测到溢出错误（参见第38.3.8节，错误检测）。为防止接收数据溢出错误，请在下一次串行传输结束前使用接收缓冲区满中断请求读取接收数据。要使用SPI接收缓冲区满中断，请将SPCR.SPRIE位设置为1。

发送和接收中断或相关的IELSRn.IR标志（其中n是中断向量号）在
ICU可用于确认发送和接收缓冲区的状态。

类似地，SPTEF和SPRF标志可用于确认发送和接收缓冲区的状态。有关中断向量编号，请参见第14节，中断控制器单元(ICU)。

38.3.8 错误检测

在正常的SPI串行传输中，写入到SPDRSPDR_HA的发送缓冲区的数据被发送，接收到的数据可以从SPDRSPDR_HA的接收缓冲区中读取。在某些情况下，访问SPDRSPDR_HA时可能会执行非正常传输，具体取决于发送或接收缓冲区的状态或串行传输开始或结束时SPI的状态。

如果发生非正常传输操作，SPI会将事件检测为欠载错误、溢出错误、奇偶校验错误或模式故障错误。表38.8列出了非正常传输操作和SPI错误检测功能之间的关系。

Table 38.8 非正常传输操作与SPI错误检测的关系

Operation	发生条件	SPI操作	错误检测
1	SPDRSPDR_HA在发送缓冲区已满时写入。	保留发送缓冲区的内容 缺少写入数据。	None
2	SPDRSPDR_HA在接收缓冲区为空时读取。	输出接收缓冲区的内容和先前接收的数据。	None
3	当SPI无法传输数据时，串行传输在从模式下启动。	暂停串行传输 缺少发送和接收数据 停止驱动MISOA输出信号 禁用SPI功能。	Underrun error
4	当接收缓冲区已满时，串行传输终止。	保留接收缓冲区的内容 缺少接收数据。	溢出错误
5	在启用奇偶校验功能的情况下执行全双工同步串行通信时收到错误的奇偶校验位。	断言奇偶校验错误标志。	奇偶校验错误
6	当串行传输在多主模式下空闲时，SSLn0输入信号被置位。	停止驱动RSPCKn、MOSIn、SSLn1到SSLn3输出信号 禁用SPI功能。	模式故障错误
7	SSLn0输入信号在多主机模式下的串行传输期间被置位。	暂停串行传输 缺少发送和接收数据 停止驱动RSPCKn、MOSIn、SSLn1到SSLn3输出信号 禁用SPI功能。	模式故障错误
8	SSLn0输入信号在从模式下的串行传输期间被否定。	暂停串行传输 缺少发送和接收数据 停止驱动MIOn输出信号 禁用SPI功能。	模式故障错误

在表38.8中描述的操作1中，SPI未检测到错误。为了防止写入过程中的数据遗漏SPDRSPDR_HA，对SPDRSPDR_HA的写操作必须使用发送缓冲区空中断执行

request (when the SPSR.SPTEF flag is 1).

Similarly, the SPI does not detect an error in operation 2. To prevent extraneous data from being read, SPDR/SPDR_HA read operations must be executed with an SPI receive buffer full interrupt request (when the SPSR.SPRF flag is 1).

For the other errors in the figure, see the following sections:

- Underrun error (operation 3): section 38.3.8.4, Underrun errors
- Overrun error (operation 4): section 38.3.8.1, Overrun errors
- Parity error (operation 5): section 38.3.8.2, Parity errors
- Mode fault error (operations 6 to 8): section 38.3.8.3, Mode fault errors.

For the transmit and receive interrupts, see section 38.3.7, Transmit Buffer Empty and Receive Buffer Full Interrupts.

38.3.8.1 Overrun errors

If a serial transfer ends when the receive buffer of SPDR/SPDR_HA is full, the SPI detects an overrun error and sets the SPSR.OVRF flag to 1. When the OVRF flag is 1, the SPI does not copy data from the shift register to the receive buffer, so the data prior to the error occurrence is retained in the receive buffer. To set the OVRF flag to 0, write 0 to the OVRF flag after the CPU reads SPSR with the OVRF flag set to 1.

Figure 38.28 shows an example of operation of the OVRF and SPRF flags. The SPSR and SPDR_HA accesses shown in the figure indicate the condition of access to the register, where W denotes a write cycle and R a read cycle. In this example, the SPI performs an 8-bit serial transfer when SPCMDm.CPHA bit is 1 and the SPCMDm.CPOL bit is 0. The numbers given for RSPCKn in the waveform represent the number of RSPCK cycles, indicating the number of transferred bits.

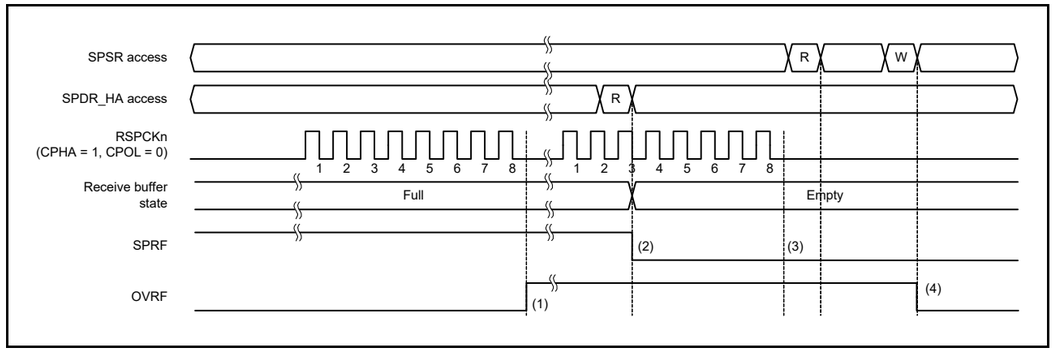


Figure 38.28 Operation example of the OVRF and SPRF flags

The operation of the flags at times (1) to (4) in the figure is as follows:

1. If a serial transfer terminates with the SPRF flag set to 1 (receive buffer full), the SPI detects an overrun error, and sets the OVRF flag to 1. The SPI does not copy the data in the shift register to the receive buffer. Even when the SPPE bit is 1, parity errors are not detected. In master mode, the SPI copies the value of the SPCMDm pointer to the SPSSR.SPECM[2:0] bits.
2. When SPDR_HA is read, the SPI outputs the data in the receive buffer. The SPRF flag is then set to 0. The receive buffer becoming empty does not set the OVRF flag to 0.
3. If the serial transfer ends with the OVRF flag set to 1 (overrun error occurred), the SPI does not copy data in the shift register to the receive buffer (the SPRF flag does not set to 1). A receive buffer full interrupt is not generated. Even when the SPPE bit is 1, parity errors are not detected. In master mode, the SPI does not update the SPSSR.SPECM[2:0] bits. In an overrun error state when the SPI does not copy the received data from the shift register to the receive buffer, on termination of the serial transfer, the SPI determines that the shift register is empty. This enables data transfer from the transmit buffer to the shift register.
4. If 0 is written to the OVRF flag after SPSR is read when the OVRF flag is 1, the OVRF flag clears to 0.

请求（当SPSR.SPTEF标志为1时）。

同样，SPI不会检测到操作2中的错误。为防止读取无关数据，必须使用SPI接收缓冲区满中断请求（当SPSR.SPRF标志为1时）执行SPDRSPDR_HA读取操作。

对于图中的其他错误，请参见以下部分：

- 欠载错误（操作3）：第38.3.8.4节，欠载错误
- 溢出错误（操作4）：第38.3.8.1节，溢出错误
- 奇偶校验错误（操作5）：第38.3.8.2节，奇偶校验错误
- 模式故障错误（操作6到8）：第38.3.8.3节，模式故障错误。

对于发送和接收中断，请参见第38.3.7节，发送缓冲区空和接收缓冲区满中断。

38.3.8.1 溢出错误

如果串行传输在SPDRSPDR_HA的接收缓冲区已满时结束，则SPI检测到溢出错误并将SPSR.OVRF标志设置为1。当OVRF标志为1时，SPI不会将数据从移位寄存器复制到接收缓冲区，因此错误发生之前的数据保留在接收缓冲区中。要将OVRF标志设置为0，请在CPU读取OVRF标志设置为1的SPSR后将0写入OVRF标志。

图38.28显示了OVRF和SPRF标志的操作示例。图中所示的SPSR和SPDR_HA访问表示访问寄存器的条件，其中W表示写周期，R表示读周期。在本例中，当SPCMDm.CPHA位为1且SPCMDm.CPOL位为0时，SPI执行8位串行传输。波形中为RSPCKn给出的数字表示RSPCK周期数，表示传输的位数.

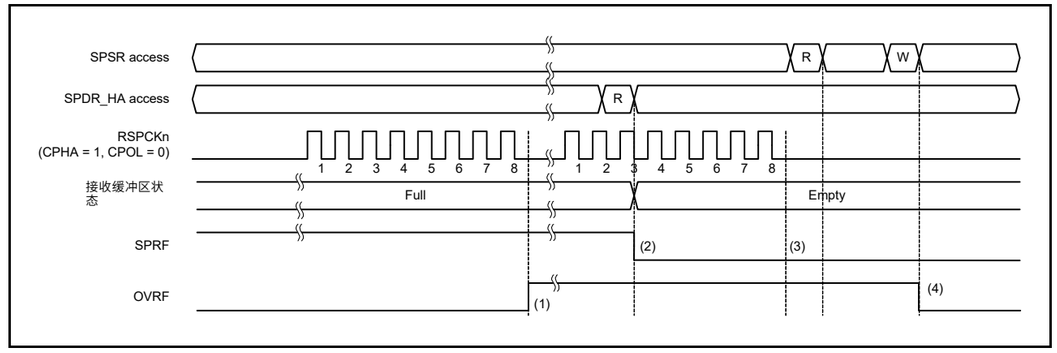


Figure 38.28 OVRF和SPRF标志的操作示例

图中（1）到（4）时刻flags的操作如下：

1. 如果串行传输终止且SPRF标志设置为1（接收缓冲区已满），则SPI检测到溢出错误，并将OVRF标志设置为1。SPI不会将移位寄存器中的数据复制到接收缓冲区。即使SPPE位为1，也不会检测到奇偶校验错误。在主机模式下，SPI将SPMDm指针的值复制到

   SPSSR.SPECM[2:0] bits.
2. 当读取SPDR_HA时，SPI输出接收缓冲区中的数据。然后SPRF标志设置为0。接收缓冲区变空不会将OVRF标志设置为0。
3. 如果串行传输结束时OVRF标志设置为1（发生溢出错误），则SPI不会将移位寄存器中的数据复制到接收缓冲区（SPRF标志不设置为1）。不产生接收缓冲区满中断。即使SPPE位为1，也不会检测到奇偶校验错误。在主模式下，SPI不更新

   SPSSR.SPECM[2:0]位。在SPI未将接收到的数据从移位寄存器复制到接收缓冲区的溢出错误状态下，在串行传输终止时，SPI确定移位寄存器为空。这使数据能够从发送缓冲器传输到移位寄存器。
4. 如果在OVRF标志为1时读取SPSR后将0写入OVRF标志，则OVRF标志清除为0。

The occurrence of an overrun can be checked either by reading SPSR or by using an SPI error interrupt and reading SPSR. When executing a serial transfer, you must ensure that overrun errors are detected early, for example by reading SPSR immediately after SPDR_HA is read. In master mode, the value of the SPCMDm pointer at the error occurrence can be checked by reading the SPSSR.SPECM[2:0] bits.

If an overrun error occurs and the OVRF flag sets to 1, normal reception operations cannot be performed until the OVRF flag is cleared to 0.

When the RSPCK auto-stop function is enabled in master mode, an overrun error does not occur. Figure 38.29 and Figure 38.30 show the clock stop waveform when a serial transfer continues while the receive buffer is full in master mode.

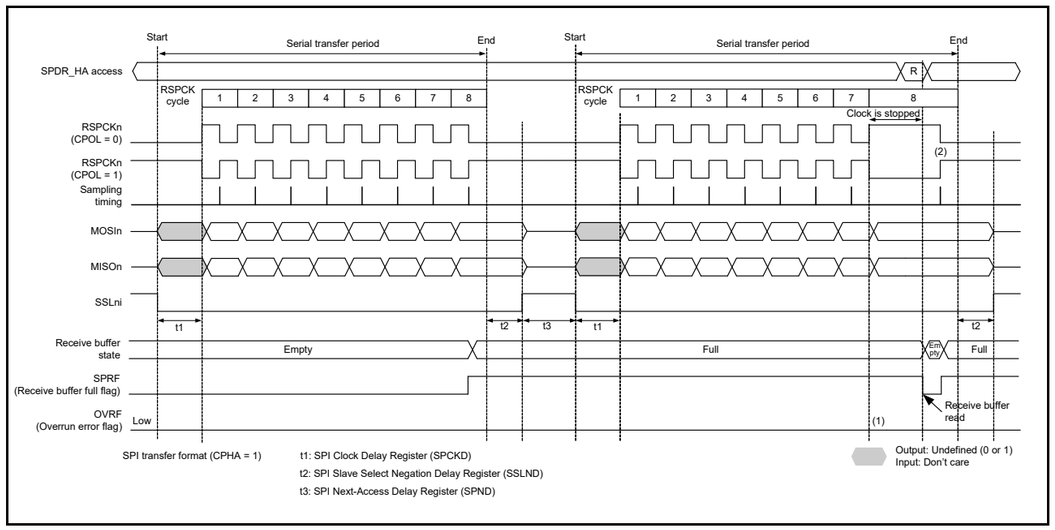


Figure 38.29 Clock stop waveform when serial transfer continues while receive buffer is full in master mode (CPHA = 1)

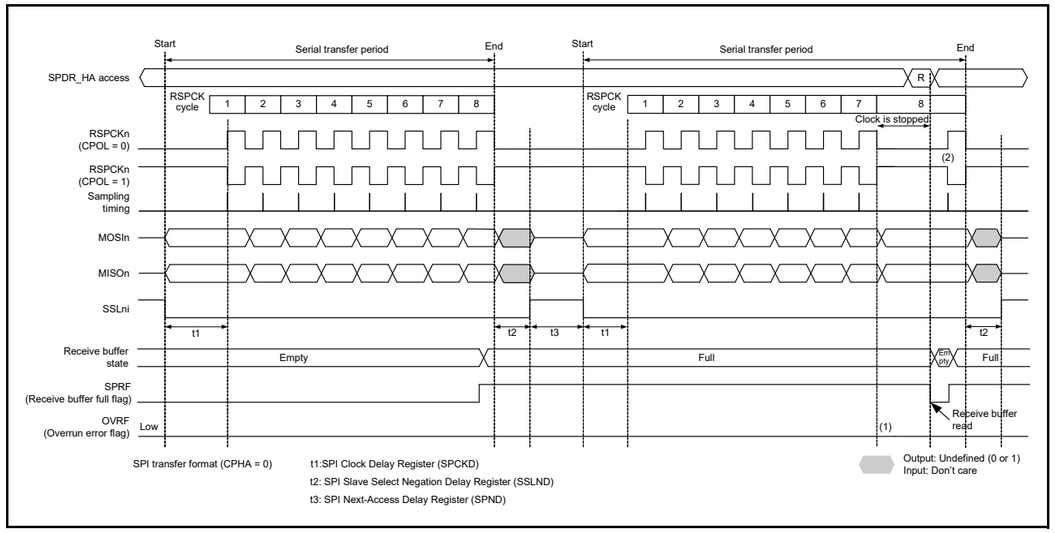


Figure 38.30 Clock stop waveform when serial transfer continues while receive buffer is full in master mode (CPHA = 0)

溢出的发生可以通过读取SPSR或使用SPI错误中断和读取来检查SPSR。执行串行传输时，必须确保及早检测到溢出错误，例如在读取SPDR_HA后立即读取SPSR。在主模式下，可以通过读取SPSSR.SPECM[2:0]位来检查发生错误时的SPCMDm指针的值。

如果发生溢出错误并且OVRF标志设置为1，则在OVRF标志被清除为0之前无法执行正常接收操作。

在主机模式下启用RSPCK自动停止功能时，不会发生溢出错误。图38.29和图38.30显示了在主机模式下接收缓冲器满时串行传输继续时的时钟停止波形。

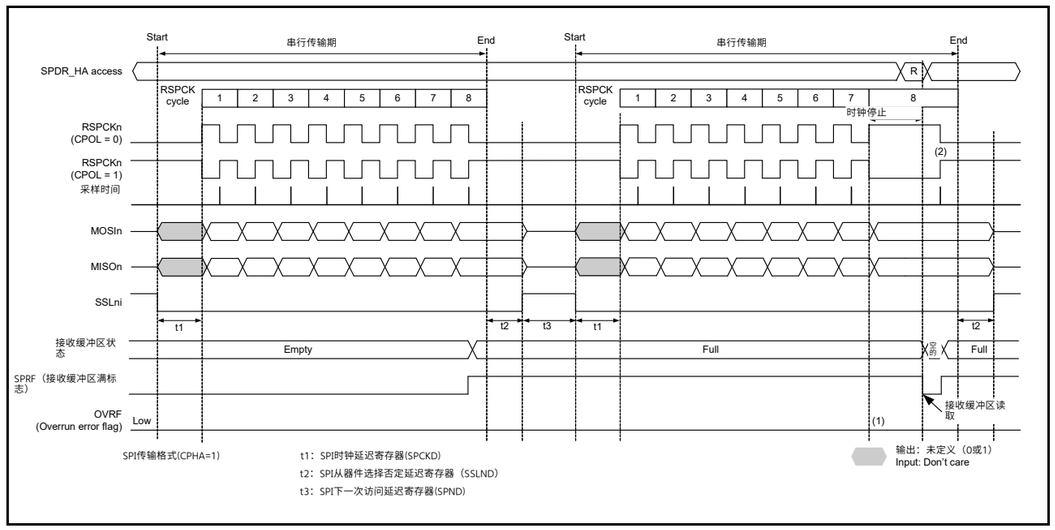


Figure 38.29 主机模式下接收缓冲器满时串行传输继续时的时钟停止波形(CPHA=1)

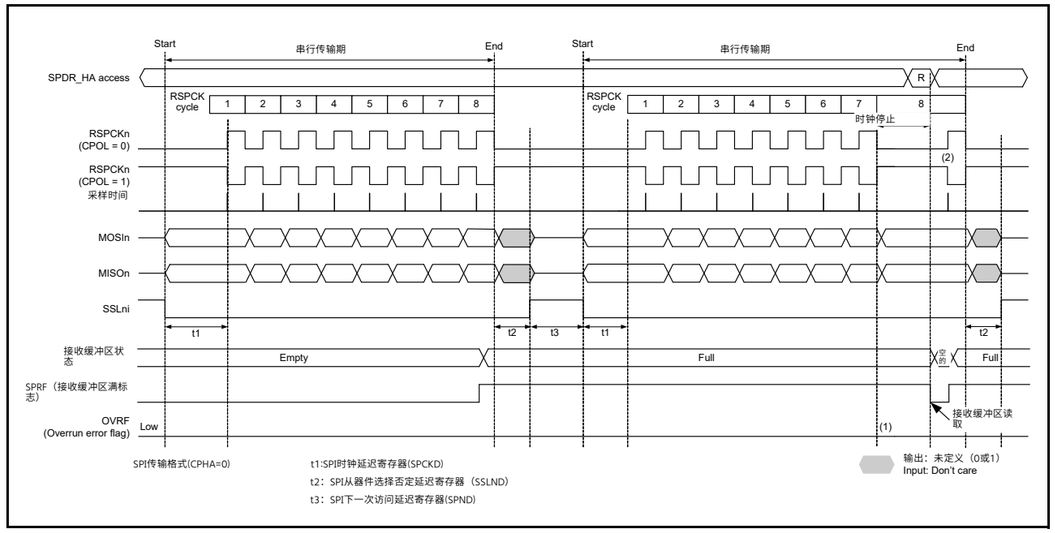


Figure 38.30 主机模式下接收缓冲器满时串行传输继续时的时钟停止波形(CPHA=0)

The operation of the flags at times (1) and (2) in the figure is as follows:

1. When the receive buffer is full, an overrun error does not occur because the RSPCK clock is stopped.
2. If SPDR_HA is read while the clock is stopped, data in the receive buffer can be read. The RSPCK clock restarts after reading the receive buffer (after the SPSR.SPRF flag clears to 0).

38.3.8.2 Parity errors

When full-duplex synchronous serial communication is performed with the SPCR.TXMD bit set to 0 and the SPCR2.SPPE bit set to 1, the SPI checks for parity errors when serial transfer ends. On detecting a parity error in the received data, the SPI sets the SPSR.PERF flag to 1. Because the SPI does not copy data in the shift register to the receive buffer when the SPSR.OVRF flag sets to 1, parity error detection is not performed for the received data. To set the PERF flag to 0, write 0 to the PERF flag after the SPSR register is read with the PERF flag set to 1.

Figure 38.31 shows an example of operation of the OVRF and PERF flags. The SPSR access shown in Figure 38.31 indicates the condition of access to the register, where W denotes a write cycle and R a read cycle. In this example, full-duplex synchronous serial communication is performed while the SPCR.TXMD bit is 0 and the SPCR2.SPPE bit is 1. The SPI performs an 8-bit serial transfer when SPCMDm.CPHA bit is 1 and the SPCMDm.CPOL bit is 0. The numbers given for RSPCKn in the waveform represent the number of RSPCK cycles, meaning the number of transferred bits.

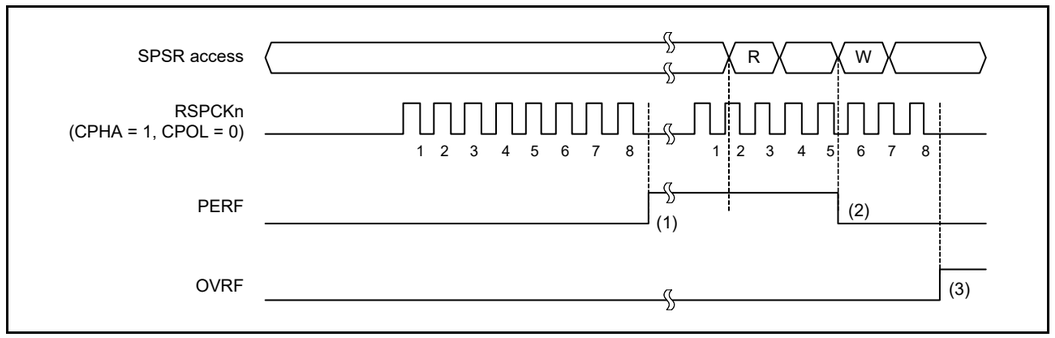


Figure 38.31 Operation example of the PERF flag

The operation of the flags at times (1) to (3) in the figure is as follows:

1. If a serial transfer terminates with the SPI not detecting an overrun error, the SPI copies the data in the shift register to the receive buffer. The SPI checks the received data at this timing and sets the PERF flag to 1 if a parity error is detected. In master mode, the SPI copies the value of the SPCMDm pointer to the SPSSR.SPECM[2:0] bits.
2. If 0 is written to the PERF flag after the SPSR register is read when the PERF flag is 1, the PERF flag clears to 0.
3. When the SPI detects an overrun error and serial transfer is terminated, the data in the shift register is not copied to the receive buffer. The SPI does not perform parity error detection at this time.

Parity errors can be checked for by either reading the SPSR register or using an SPI error interrupt and reading the SPSR register. When executing a serial transfer, such checks are required to ensure early detection of parity errors. When the SPI is used in master mode, the pointer value to the SPCMDm register at the occurrence of the error can be checked by reading the SPSSR.SPECM[2:0] bits.

38.3.8.3 Mode fault errors

The SPI operates in multi-master mode when the SPCR.MSTR bit is 1, the SPCR.SPMS bit is 0, and the SPCR.MODFEN bit is 1. If the active level is input for the SSLn0 input signal of the SPI in multi-master mode, the SPI detects a mode fault error regardless of the status of the serial transfer, and sets the SPSR.MODF flag to 1. On detecting the mode fault error, the SPI copies the value of the SPCMDm pointer to the SPSSR.SPECM[2:0] bits. The active level of the SSLn0 signal is determined by the SSLP.SSL0P bit.

When the MSTR bit is 0, the SPI operates in slave mode. The SPI detects a mode fault error if the MODFEN bit of the SPI in slave mode is 1, and the SPMS bit is 0, and if the SSLn0 input signal is negated during the serial transfer period (from the time the driving of valid data is started to the time the final valid data is fetched).

图中（1）和（2）时刻flags的操作如下：

1. 当接收缓冲器已满时，不会发生溢出错误，因为RSPCK时钟已停止。
2. 如果在时钟停止时读取SPDR_HA，则可以读取接收缓冲区中的数据。RSPCK时钟在读取接收缓冲区后重新启动（在SPSR.SPRF标志清除为0后）。

38.3.8.2 奇偶校验错误

当SPCR.TXMD位设置为0且
SPCR2.SPPE位设置为1，SPI在串行传输结束时检查奇偶校验错误。在接收到的数据中检测到奇偶校验错误时，SPI将SPSR.PERF标志设置为1。因为当SPSR.OVRF标志设置为1时，SPI不会将移位寄存器中的数据复制到接收缓冲区，所以奇偶校验错误检测是不为接收到的数据执行。要将PERF标志设置为0，请在读取SPSR寄存器并将PERF标志设置为1后将0写入PERF标志。

图38.31显示了OVRF和PERF标志的操作示例。图38.31所示的SPSR访问表示访问寄存器的条件，其中W表示写周期，R表示读周期。在本例中，当SPCR.TXMD位为0且SPCR2.SPPE位为1时执行全双工同步串行通信。当SPCMDm.CPHA位为1且SPCMDm.CPOL位为1时，SPI执行8位串行传输0.波形中为RSPCKn给出的数字表示RSPCK周期数，即传输的位数。

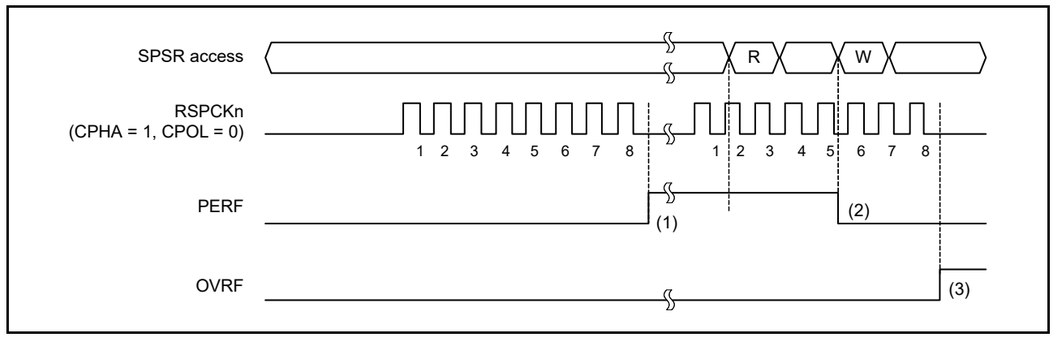


Figure 38.31 PERF标志的操作示例

图中（1）到（3）时刻flags的操作如下：

1. 如果串行传输因SPI未检测到溢出错误而终止，则SPI将移位寄存器中的数据复制到接收缓冲区。SPI在此时检查接收到的数据，如果检测到奇偶校验错误，则将PERF标志设置为1。在主模式下，SPI将SPCMDm指针的值复制到SPSSR.SPECM[2:0]位。
2. 如果在PERF标志为1时读取SPSR寄存器后将0写入PERF标志，则PERF标志清除为0。
3. 当SPI检测到溢出错误并终止串行传输时，移位寄存器中的数据不会复制到接收缓冲区。此时SPI不执行奇偶校验错误检测。

可以通过读取SPSR寄存器或使用SPI错误中断并读取SPSR寄存器来检查奇偶校验错误。在执行串行传输时，需要进行此类检查以确保及早发现奇偶校验错误。当SPI用于主机模式时，可以通过读取SPSSR.SPECM[2:0]位来检查发生错误时指向SPCMDm寄存器的指针值。

38.3.8.3 模式故障错误

当SPCR.MSTR位为1、SPCR.SPMS位为0且
SPCR.MODFEN位为1。如果在多主机模式下为SPI的SSLn0输入信号输入有效电平，则无论串行传输的状态如何，SPI都会检测到模式故障错误，并设置SPSR.MODF标志为1.在检测到模式故障错误时，SPI将SPCMDm指针的值复制到SPSSR.SPECM[2:0]位。SSLn0信号的有效电平由SSLP.SSL0P位决定。

当MSTR位为0时，SPI工作在从机模式。如果从机模式下SPI的MODFEN位为1，SPMS位为0，并且在串行传输期间（从驱动有效数据开始开始到获取最终有效数据的时间）。

On detecting a mode fault error, the SPI stops the driving of output signals and clears the SPCR.SPE bit to 0 (see section 38.3.9, Initializing the SPI). For multi-master configuration, detection of a mode fault error is used to stop the driving of output signals and the SPI function, which allows the master to be released.

The occurrence of a mode fault error can be checked either by reading SPSR or by using an SPI error interrupt and reading SPSR. SPSR polling is required for detecting mode fault errors if the SPI error interrupt is not used. When using the SPI in master mode, the value of the SPCMDm pointer at the error occurrence can be checked by reading the SPSSR.SPECM[2:0] bits.

When the MODF flag is 1, writing 1 to the SPE bit is ignored by the SPI. To enable the SPI function after the detection of a mode fault error, the MODF flag must be set to 0.

38.3.8.4 Underrun errors

When the serial transfer begins while the SPCR.MSTR bit is 0 (slave mode), SPCR.SPE bit is 1 and the transmission data not prepared, the SPI detects an underrun error. Then, SPI sets the SPSR.MODF and SPSR.UDRF flags to 1.

On detecting an underrun error, the SPI stops the driving of output signals and clears the SPCR.SPE bit to 0 (see section 38.3.9, Initializing the SPI).

The occurrence of an underrun error can be checked either by reading SPSR or by using an SPI error interrupt and reading SPSR. SPSR polling is required for detecting underrun errors if the SPI error interrupt is not used.

When the MODF flag is 1, writing 1 to the SPE bit is ignored by the SPI. To enable the SPI function after the detection of an underrun error, the MODF flag must be cleared to 0.

38.3.9 Initializing the SPI

If 0 is written to the SPCR.SPE bit or the SPI sets the SPE bit to 0 because of the detection of a mode fault error or an underrun error, the SPI disables the SPI function and initializes some of the module functions. When a system reset is generated, the SPI initializes all of the module functions. This section describes initialization by clearing of the SPCR.SPE bit and by a system reset.

38.3.9.1 Initialization by clearing of the SPE bit

When the SPCR.SPE bit is set to 0, the SPI performs the following initialization:

- Suspends any serial transfer that is being executed
- Stops the driving of output signals (Hi-Z) in slave mode
- Initializes the internal state of the SPI
- Initializes the transmit buffer of the SPI (the SPSR.SPTEF flag sets to 1).

Initialization by clearing of the SPE bit does not initialize the control bits of the SPI. For this reason, the SPI can be started in the same transfer mode in use prior to initialization when the SPE bit is set to 1 again.

The SPSR.SPRF, SPSR.OVRF, SPSR.MODF, SPSR.PERF, and SPSR.UDRF flags are not initialized, and the value of the SPI Sequence Status Register (SPSSR) is not initialized. Therefore, even after the SPI is initialized, data from the receive buffer can be read to check the status of error occurrence during an SPI transfer.

The transmit buffer is initialized to an empty state (the SPSR.SPTEF flag sets to 1). Therefore, if the SPCR.SPTIE bit is set to 1 after SPI initialization, a transmit buffer empty interrupt is generated. To disable any transmit buffer empty interrupts when the SPI is initialized, write 0 to the SPTIE bit at the same time as writing 0 to the SPE bit.

38.3.9.2 System reset

An initialization by a system reset completely initializes the SPI by initializing all SPI control bits, status bits, and data registers, in addition to meeting the requirements described in section 38.3.9.1, Initialization by clearing of the SPE bit.

38.3.10 SPI Operation

38.3.10.1 Master mode operation

The only difference between single- and multi-master mode operation lies in mode fault error detection (see section

在检测到模式故障错误时，SPI会停止驱动输出信号并将SPCR.SPE位清除为0（请参阅第38.3.9节，初始化SPI）。对于多主机配置，检测到模式故障错误用于停止驱动输出信号和SPI功能，从而释放主机。

可以通过读取SPSR或使用SPI错误中断并读取SPSR来检查模式故障错误的发生。如果不使用SPI错误中断，则需要SPSR轮询来检测模式错误。在主模式下使用SPI时，可以通过读取SPSSR.SPECM[2:0]位来检查发生错误时SPCMDm指针的值。

当MODF标志为1时，向SPE位写入1会被SPI忽略。要在检测到模式故障错误后启用SPI功能，MODF标志必须设置为0。

38.3.8.4 Underrun errors

当SPCR.MSTR位为0（从模式）、SPCR.SPE位为1且未准备好传输数据时串行传输开始时，SPI检测到欠载错误。然后，SPI将SPSR.MODF和SPSR.UDRF标志设置为1。

检测到欠载错误时，SPI停止驱动输出信号并将SPCR.SPE位清零（请参见第38.3.9节，初始化SPI）。

可以通过读取SPSR或使用SPI错误中断并读取SPSR来检查欠载错误的发生。如果不使用SPI错误中断，则需要SPSR轮询来检测欠载错误。

当MODF标志为1时，向SPE位写入1会被SPI忽略。要在检测到欠载错误后启用SPI功能，必须将MODF标志清零。

38.3.9 初始化SPI

如果向SPCR.SPE位写入0或SPI由于检测到模式故障错误或欠载错误而将SPE位设置为0，则SPI将禁用SPI功能并初始化一些模块功能。当产生系统复位时，SPI初始化所有模块功能。本节介绍通过清除SPCR.SPE位和系统复位进行的初始化。

38.3.9.1 通过清除SPE位进行初始化

当SPCR.SPE位设置为0时，SPI执行以下初始化：

- 暂停任何正在执行的串行传输
- 在从模式下停止驱动输出信号(Hi-Z)
- 初始化SPI的内部状态
- 初始化SPI的发送缓冲区（SPSR.SPTEF标志设置为1）。

通过清除SPE位进行的初始化不会初始化SPI的控制位。因此，当SPE位再次设置为1时，SPI可以在初始化之前以相同的传输模式启动。

SPSR.SPRF、SPSR.OVRF、SPSR.MODF、SPSR.PERF和SPSR.UDRF标志未初始化，SPI序列状态寄存器(SPSSR)的值未初始化。因此，即使在SPI初始化之后，也可以从接收缓冲区读取数据，以检查SPI传输期间发生错误的状态。

发送缓冲区初始化为空状态（SPSR.SPTEF标志设置为1）。因此，如果SPCR.SPTIE位在SPI初始化后设置为1，则会产生发送缓冲区空中断。要在SPI初始化时禁用任何发送缓冲区空中断，请在向SPE位写入0的同时向SPTIE位写入0。

38.3.9.2 系统重置

除了满足第38.3.9.1节，通过清除SPE位进行的初始化中描述的要求之外，系统复位的初始化还通过初始化所有SPI控制位、状态位和数据寄存器来完全初始化SPI。

38.3.10 SPI操作

38.3.10.1 主模式操作

单主机模式和多主机模式操作之间的唯一区别在于模式故障错误检测（参见章节

38.3.8, Error Detection). The SPI does not detect mode fault errors in single master mode and does in multi-master mode. This section explains operations that are the same for single- and multi-master modes.

(1) Starting a serial transfer

The SPI updates the data in the transmit buffer (SPTX) when data is written to the SPI Data Register (SPDR/SPDR_HA) and the SPI transmit buffer is empty (data for the next transfer is not set and the SPSR.SPTEF flag is 1). When the shift register is empty after the number of frames set in the SPDCR.SPFC[1:0] bits are written to the SPDR/SPDR_HA, the SPI copies data from the transmit buffer to the shift register and starts serial transfer. On copying transmit data to the shift register, the SPI changes the status of the shift register to full. On termination of the serial transfer, it changes the status of the shift register to empty. The status of the shift register cannot be referenced.

The polarity of the SSLni output pins depends on the SSLP register settings. For details on the SPI transfer format, see section 38.3.5, Transfer Formats.

(2) Terminating a serial transfer

Regardless of the SPCMDm.CPHA bit setting, the SPI terminates the serial transfer after transmitting an RSPCKn edge corresponding to the final sampling timing. If free space is available in the receive buffer (SPRX) (the SPSR.SPRF flag is 0), on termination of the serial transfer, the SPI copies data from the shift register to the receive buffer of the SPDR/SPDR_HA register.

The final sampling timing varies depending on the bit length of transfer data. In master mode, the SPI data length depends on the SPCMDm.SPB[3:0] bit setting. The polarity of the SSLni output pin depends on the SSLP register settings. For details on the SPI transfer format, see section 38.3.5, Transfer Formats.

(3) Sequence control

The transfer format used in master mode is determined by the SPSCR, SPCMDm, SPBR, SPCKD, SSLND, and SPND registers.

The SPSCR register determines the sequence configuration for serial transfers that are executed by the SPI in master mode. The following Parameters are set in the SPCMDm register:

- SSLni pin output signal value
- MSB- or LSB-first
- Data length
- Some of the bit rate settings
- RSPCK polarity and phase
- Whether SPCKD is to be referenced
- Whether SSLND is to be referenced
- Whether SPND is to be referenced.

SPBR holds some of the bit rate settings, including SPCKD (SPI clock delay), SSLND (SSL negation delay), and SPND (next-access delay).

Based on the sequence length assigned in SPSCR, the SPI makes up a sequence comprised of a part or all of the SPCMDm register. The SPI contains a pointer to the SPCMDm register that makes up the sequence. The value of this pointer can be checked by reading the SPSSR.SPCP[2:0] bits. When the SPCR.SPE bit is set to 1 and the SPI function is enabled, the SPI loads the pointer to the commands in SPCMD0, and incorporates the SPCMD0 settings into the transfer format at the beginning of serial transfer. The SPI increments the pointer each time the next-access delay period for a data transfer ends. On completion of the serial transfer that corresponds to the final command in the sequence, the SPI sets the pointer to SPCMD0, and in this way the sequence is executed repeatedly.

38.3.8，错误检测）。SPI在单主模式下不检测模式故障错误，而在多主模式下检测。本节说明单主机模式和多主机模式的相同操作。

(1) 开始串行传输

当数据写入SPI数据寄存器(SPDRSPDR_HA)且SPI发送缓冲区为空（未设置下一次传输的数据且SPSR.SPTEF标志为1）时，SPI更新发送缓冲区(SPTX)中的数据.当SPDCR.SPFC[1:0]位中设置的帧数写入SPDRSPDR_HA后移位寄存器为空时，SPI将数据从发送缓冲区复制到移位寄存器并开始串行传输。在将发送数据复制到移位寄存器时，SPI将移位寄存器的状态更改为已满。在串行传输终止时，它将移位寄存器的状态更改为空。无法引用移位寄存器的状态。

SSLni输出引脚的极性取决于SSLP寄存器设置。有关SPI传输格式的详细信息，请参阅第38.3.5节，传输格式。

(2) 终止串行传输

无论SPMDm.CPHA位设置如何，SPI在发送对应于最终采样时序的RSPCKn边沿后终止串行传输。如果接收缓冲区(SPRX)中有可用空间（SPSR.SPRF标志为0），则在串行传输终止时，SPI将数据从移位寄存器复制到SPDRSPDR_HA寄存器的接收缓冲区。

最终的采样时序根据传输数据的位长而变化。在主机模式下，SPI数据长度取决于SPMDm.SPB[3:0]位设置。SSLni输出引脚的极性取决于SSLP寄存器设置。有关SPI传输格式的详细信息，请参阅第38.3.5节，传输格式。

(3) 顺序控制

主机模式中使用的传输格式由SPSCR、SPCMDm、SPBR、SPCKD、SSLND和SPND寄存器确定。

SPSCR寄存器确定由SPI在主模式下执行的串行传输的序列配置。在SPMDm寄存器中设置以下参数：

- SSLni管脚输出信号值
- MSB- or LSB-first
- 数据长度
- 一些比特率设置
- RSPCK极性和相位
- 是否要引用SPCKD
- 是否要引用SSLND
- 是否要引用SPND。

SPBR保存一些比特率设置，包括SPCKD（SPI时钟延迟）、SSLND（SSL否定延迟）和SPND（下一次访问延迟）。

基于在SPSCR中分配的序列长度，SPI组成一个序列，由部分或全部SPMDm寄存器。SPI包含一个指向构成序列的SPCMDm寄存器的指针。该指针的值可以通过读取SPSSR.SPCP[2:0]位来检查。当SPCR.SPE位设置为1且SPI功能使能时，SPI加载指向SPCMD0中命令的指针，并在串行传输开始时将SPCMD0设置合并到传输格式中。每次数据传输的下一个访问延迟周期结束时，SPI都会递增指针。在完成对应于序列中最后一个命令的串行传输后，SPI将指针设置为SPCMD0，并以此方式重复执行序列。

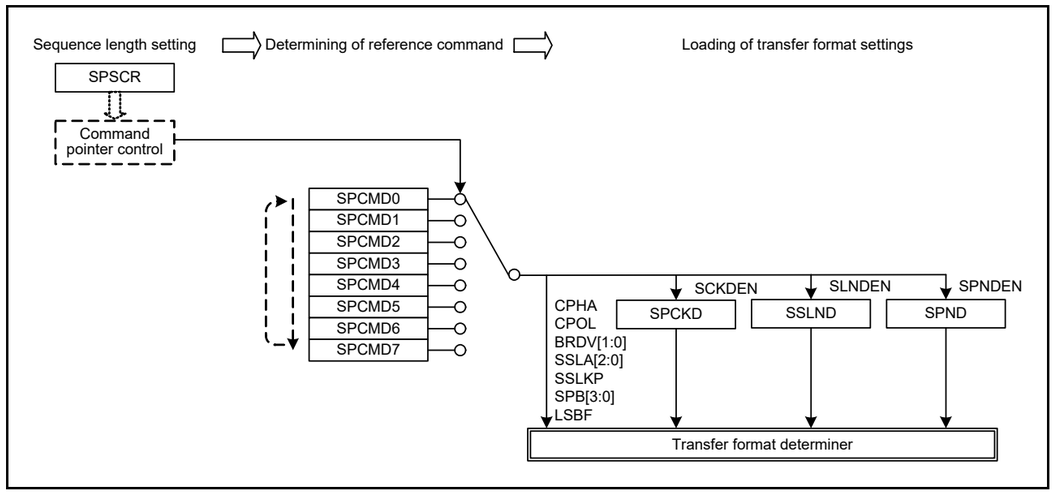


Figure 38.32 Procedure for determining the form of a serial transfer in master mode

In this section, a frame is the combination of the data in SPDR/SPDR_HA and the settings in SPCMDm.

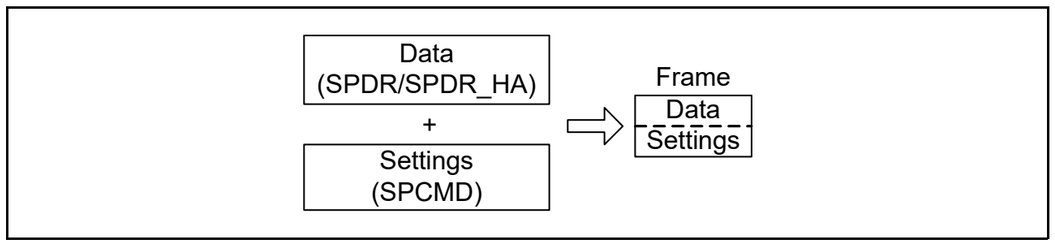


Figure 38.33 Conceptual diagram of frames

Figure 38.34 shows the correspondence between the commands and the transmit and receive buffers in the sequence of operations specified by the settings in Table 38.4.

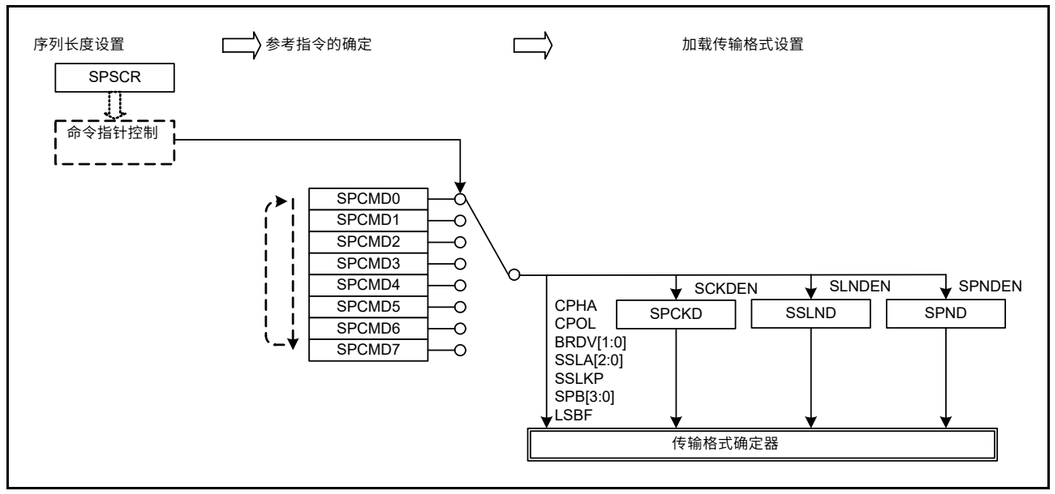


Figure 38.32 确定主模式下串行传输形式的过程

在本节中，帧是SPDRSPDR_HA中的数据和SPMDm中的设置的组合。

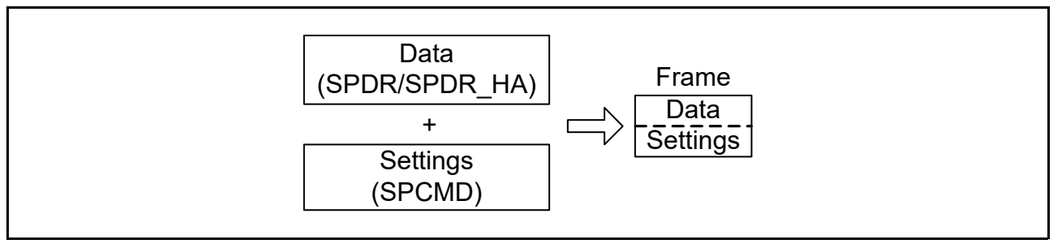


Figure 38.33 框架的概念图

图38.34显示了在表38.4中的设置指定的操作序列中命令与发送和接收缓冲区之间的对应关系。

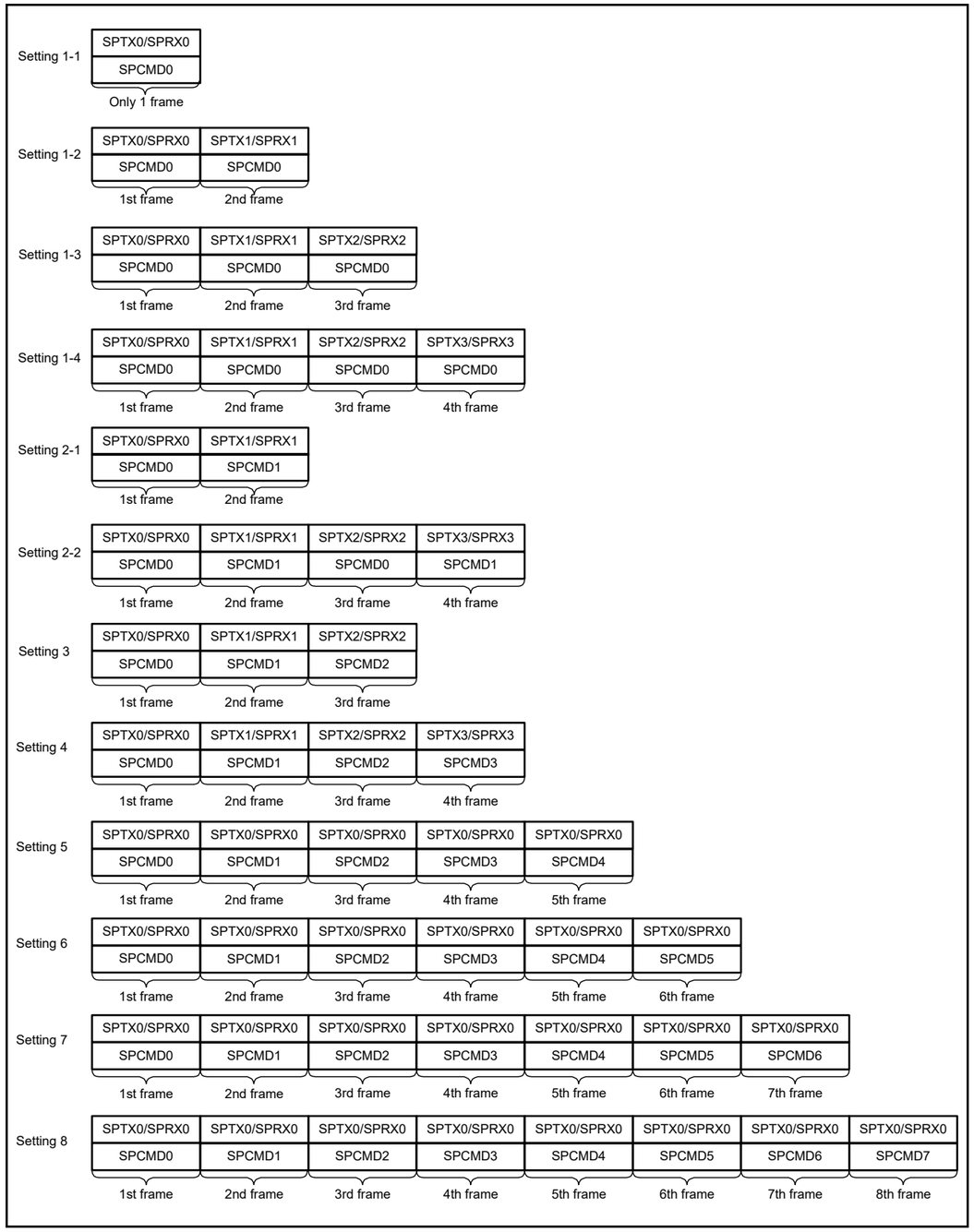


Figure 38.34 Correspondence between SPI Command Register and transmit and receive buffers in sequence operations

(4) Burst transfers

If the SPCMDm.SSLKP bit that the SPI references during the current serial transfer is 1, the SPI maintains the SSLni

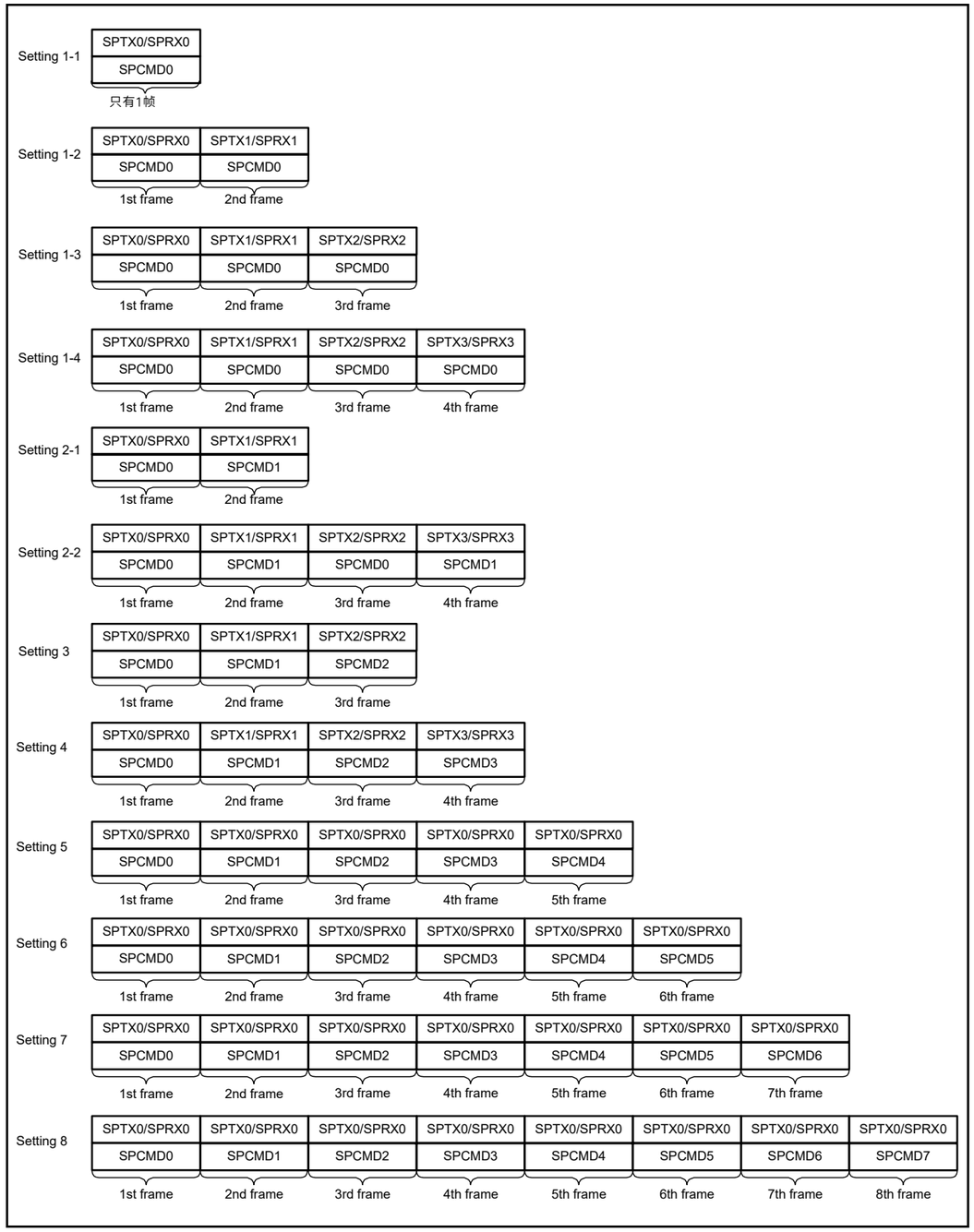


Figure 38.34 顺序操作中SPI命令寄存器与发送接收缓冲区的对应关系

(4) 突发传输

如果SPI在当前串行传输期间引用的SPCMDm.SSLKP位为1，则SPI维护SSLni

signal level during the serial transfer until the beginning of the SSLni signal assertion for the next serial transfer. If the SSLni signal level for the next serial transfer is the same as the SSLni signal level for the current serial transfer, the SPI can execute continuous serial transfers while keeping the SSLni signal assertion status (burst transfer).

Figure 38.35 shows an example of an SSLni signal operation for a burst transfer that is implemented using the SPCMD0 and SPCMD1 register settings. This section describes SPI operations (1) to (7) shown in Figure 38.35.

Note: The polarity of the SSLni output signal depends on the SSLP register settings.

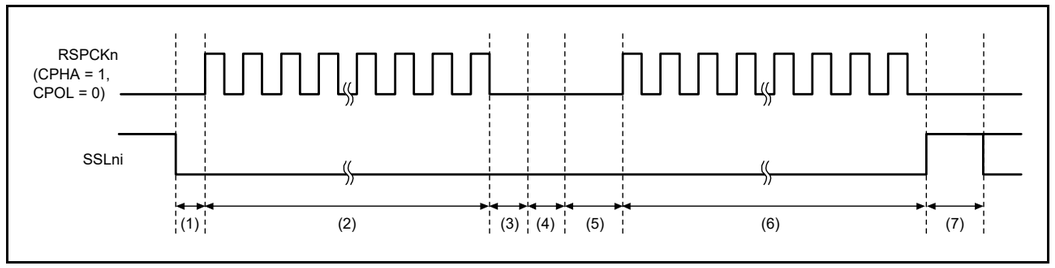


Figure 38.35 Example of burst transfer operation using the SSLKP bit

The SPI operation at times (1) to (7) in the figure is as follows:

1. Based on the SPCMD0 settings, the SPI asserts the SSLni signal and inserts RSPCK delays.
2. The SPI executes serial transfers in accordance with the SPCMD0 settings.
3. The SPI inserts an SSL negation delay.
4. Because the SPCMD0.SSLKP bit is 1, the SPI keeps the SSLni signal value specified in SPCMD0. This period is sustained at a minimum for a period equal to the next-access delay in SPCMD0. If the shift register is empty after the passage of the minimum period, this period is sustained until the transmit data is stored in the shift register for the next transfer.
5. Based on the SPCMD1 settings, the SPI asserts the SSLni signal and inserts RSPCK delays.
6. The SPI executes serial transfers in accordance with the SPCMD1 settings.
7. Because the SPCMD1.SSLKP bit is 0, the SPI negates the SSLni signal. In addition, a next-access delay is inserted in accordance with SPCMD1.

If the SSLni signal output settings in the SPCMDm register where 1 is assigned to the SSLKP bit are different from the SSLni signal output settings in the SPCMDm register to be used in the next transfer, the SPI switches the SSLni signal status to SSLni signal assertion as shown in (5) in Figure 38.35. This corresponds to the command for the next transfer.

Note: If such an SSLni signal switching occurs, the slaves that drive the MISOn signal compete, and collision of signal levels might occur.

The SPI in master mode references the SSLni signal operation within the module when the SSLKP bit is not used. When the SPCMDm.CPHA bit is 0, the SPI can accurately start serial transfers by using the SSLni signal assertion for the next transfer that is detected internally.

(5) RSPCK delay (t1)

The RSPCK delay value of the SPI in master mode depends on the SPCMDm.SCKDEN bit setting and the SPCKD register setting. The SPI determines the SPCMDm register to be referenced during a serial transfer by pointer control, and determines the RSPCK delay value by using the SPCMDm.SCKDEN bit and SPCKD, as listed in Table 38.9. For a definition of the RSPCK delay, see section 38.3.5, Transfer Formats.

Table 38.9 Relationship among the SCKDEN bit, SPCKD register, and RSPCK delay (1 of 2)

SPCMDm.SCKDEN bit	SPCKD.SCKDL[2:0] bits	RSPCK delay
0	000b to 111b	1 RSPCK

串行传输期间的信号电平，直到下一次串行传输的SSLni信号断言开始。如果下一次串行传输的SSLni信号电平与当前串行传输的SSLni信号电平相同，则SPI可以在保持SSLni信号断言状态（突发传输）的同时执行连续串行传输。

图38.35显示了使用SPCMD0和SPCMD1寄存器设置实现的突发传输的SSLni信号操作示例。本节介绍图38.35所示的SPI操作(1)至(7)。

Note: SSLni输出信号的极性取决于SSLP寄存器设置。

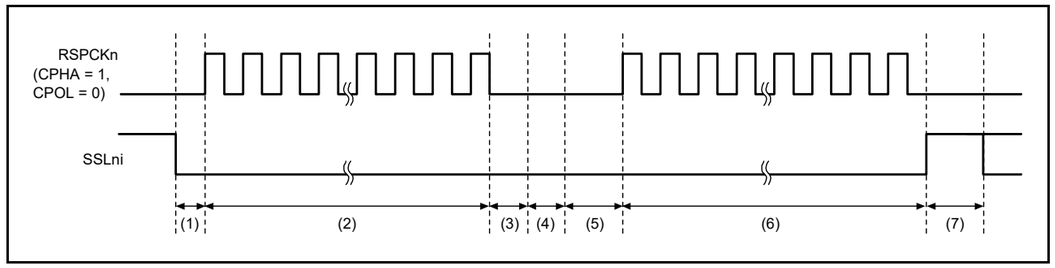


Figure 38.35 使用SSLKP位的突发传输操作示例

图中（1）到（7）时刻的SPI操作如下：

1. 基于SPCMD0设置，SPI断言SSLni信号并插入RSPCK延迟。
2. SPI根据SPMD0设置执行串行传输。
3. SPI插入SSL否定延迟。
4. 由于SPCMD0.SSLKP位为1，SPI保持SPCMD0中指定的SSLni信号值。该周期至少持续一段时间，等于SPMD0中的下一次访问延迟。如果在经过最小周期后移位寄存器为空，则该周期一直持续到发送数据存储在移位寄存器中以供下一次传输。
5. 基于SPCMD1设置，SPI断言SSLni信号并插入RSPCK延迟。
6. SPI根据SPMD1设置执行串行传输。
7. 因为SPCMD1.SSLKP位为0，SPI否定SSLni信号。此外，根据SPMD1插入下一个访问延迟。

如果SPCMDm寄存器中SSLKP位为1的SSLni信号输出设置与下次传输使用的SPCMDm寄存器中的SSLni信号输出设置不同，则SPI将SSLni信号状态切换为SSLni信号断言，如下所示如图38.35(5)所示。这对应于下一次传输的命令。

Note: 如果发生这种SSLni信号切换，驱动MISon信号的从机竞争，可能会发生信号电平冲突。

当不使用SSLKP位时，主模式下的SPI参考模块内的SSLni信号操作。当SPCMDm.CPHA位为0时，SPI可以通过使用SSLni信号断言来准确启动串行传输，以进行内部检测到的下一次传输。

(5) RSPCK delay (t1)

主机模式下SPI的RSPCK延迟值取决于SPMDm.SCKDEN位设置和SPCKD寄存器设置。SPI通过指针控制确定串行传输期间要引用的SPCMDm寄存器，并通过使用SPCMDm.SCKDEN位和SPCKD确定RSPCK延迟值，如表38.9中所列。有关RSPCK延迟的定义，请参阅第38.3.5节，传输格式。

Table 38.9 SCKDEN位、SPCKD寄存器和RSPCK延迟之间的关系（1of2）

SPCMDm.SCKDEN bit	SPCKD.SCKDL[2:0] bits	RSPCK delay
0	000b to 111b	1 RSPCK

Table 38.9 Relationship among the SCKDEN bit, SPCKD register, and RSPCK delay (2 of 2)

SPCMDm.SCKDEN bit	SPCKD.SCKDL[2:0] bits	RSPCK delay
1	000b	1 RSPCK
	001b	2 RSPCK
	010b	3 RSPCK
	011b	4 RSPCK
	100b	5 RSPCK
	101b	6 RSPCK
	110b	7 RSPCK
	111b	8 RSPCK

(6) SSL negation delay (t2)

The SSL negation delay value of the SPI in master mode depends on the SPCMDm.SLNDEN bit setting and the SSLND register setting. The SPI determines the SPCMDm register to be referenced by pointer control during a serial transfer, and determines the SSL negation delay by using the SPCMDm.SLNDEN bit and SSLND, as listed in Table 38.10. For a definition of the SSL negation delay, see section 38.3.5, Transfer Formats.

Table 38.10 Relationship among the SLNDEN bit, SSLND, and SSL negation delay

SPCMDm.SLNDEN bit	SSLND.SLNDL[2:0] bits	SSL negation delay
0	000b to 111b	1 RSPCK
1	000b	1 RSPCK
	001b	2 RSPCK
	010b	3 RSPCK
	011b	4 RSPCK
	100b	5 RSPCK
	101b	6 RSPCK
	110b	7 RSPCK
	111b	8 RSPCK

(7) Next-access delay (t3)

The next-access delay value of the SPI in master mode depends on the SPCMDm.SPNDEN bit setting and the SPND register setting. The SPI determines the SPCMDm register to be referenced during serial transfer by pointer control, and determines the next-access delay during serial transfer by using the SPCMDm.SPNDEN bit and SPND, as listed in Table 38.11. For a definition of the next-access delay, see section 38.3.5, Transfer Formats.

Table 38.11 Relationship among the SPNDEN bit, SPND, and next-access delay

SPCMDm.SPNDEN bit	SPND.SPNDL[2:0] bits	Next-access delay
0	000b to 111b	1 RSPCK + 2 PCLKA
1	000b	1 RSPCK + 2 PCLKA
	001b	2 RSPCK + 2 PCLKA
	010b	3 RSPCK + 2 PCLKA
	011b	4 RSPCK + 2 PCLKA
	100b	5 RSPCK + 2 PCLKA
	101b	6 RSPCK + 2 PCLKA
	110b	7 RSPCK + 2 PCLKA
	111b	8 RSPCK + 2 PCLKA

(8) Initialization flow

Figure 38.36 shows an example of initialization flow for SPI operation when the SPI is used in master mode. For a

Table 38.9 SCKDEN位、SPCKD寄存器和RSPCK延迟之间的关系(2of2)

SPCMDm.SCKDEN bit	SPCKD.SCKDL[2:0] bits	RSPCK delay
1	000b	1 RSPCK
	001b	2 RSPCK
	010b	3 RSPCK
	011b	4 RSPCK
	100b	5 RSPCK
	101b	6 RSPCK
	110b	7 RSPCK
	111b	8 RSPCK

(6) SSL否定延迟(t2)

主模式下SPI的SSL否定延迟值取决于SPMDm.SLNDEN位设置和SSLND寄存器设置。SPI确定串行传输期间指针控制要引用的SPCMDm寄存器，并通过使用SPCMDm.SLNDEN位和SSLND确定SSL否定延迟，如表38.10中所列。有关SSL否定延迟的定义，请参阅第38.3.5节，传输格式。

Table 38.10 SLNDEN位、SSLND和SSL否定延迟之间的关系

SPCMDm.SLNDEN bit	SSLND.SLNDL[2:0] bits	SSL否定延迟
0	000b to 111b	1 RSPCK
1	000b	1 RSPCK
	001b	2 RSPCK
	010b	3 RSPCK
	011b	4 RSPCK
	100b	5 RSPCK
	101b	6 RSPCK
	110b	7 RSPCK
	111b	8 RSPCK

(7) Next-access delay (t3)

主机模式下SPI的下一次访问延迟值取决于SPMDm.SPNDEN位设置和SPND寄存器设置。SPI通过指针控制确定串行传输过程中要引用的SPCMDm寄存器，并通过使用SPCMDm.SPNDEN位和SPND确定串行传输过程中的下一次访问延迟，如表38.11所示。有关下一次访问延迟的定义，请参阅第38.3.5节，传输格式。

Table 38.11 SPNDEN位、SPND和下一次访问延迟之间的关系

SPCMDm.SPNDEN bit	SPND.SPNDL[2:0] bits	Next-access delay
0	000b to 111b	1 RSPCK + 2 PCLKA
1	000b	1 RSPCK + 2 PCLKA
	001b	2 RSPCK + 2 PCLKA
	010b	3 RSPCK + 2 PCLKA
	011b	4 RSPCK + 2 PCLKA
	100b	5 RSPCK + 2 PCLKA
	101b	6 RSPCK + 2 PCLKA
	110b	7 RSPCK + 2 PCLKA
	111b	8 RSPCK + 2 PCLKA

(8) 初始化流程

图38.36显示了当SPI用于主机模式时SPI操作的初始化流程示例。为一个

description of how to set up the Interrupt Controller Unit (ICU), DMAC, and I/O ports, see the descriptions given in the individual blocks.

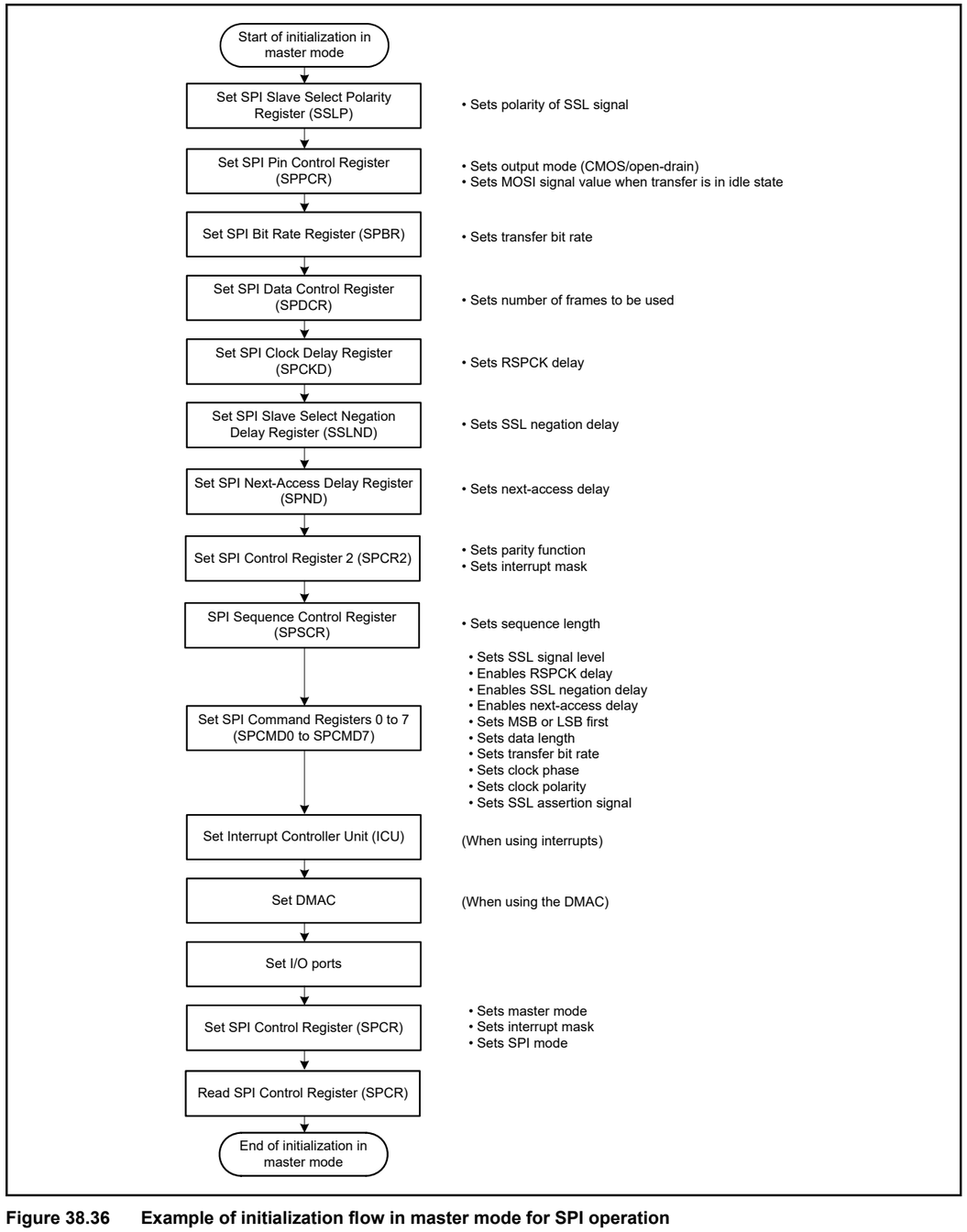


Figure 38.36 Example of initialization flow in master mode for SPI operation

(9) Software processing flow

Figure 38.37 to Figure 38.39 show examples of the software processing flow.

有关如何设置中断控制器单元(ICU)、DMAC和IO端口的说明，请参见各个块中给出的说明。

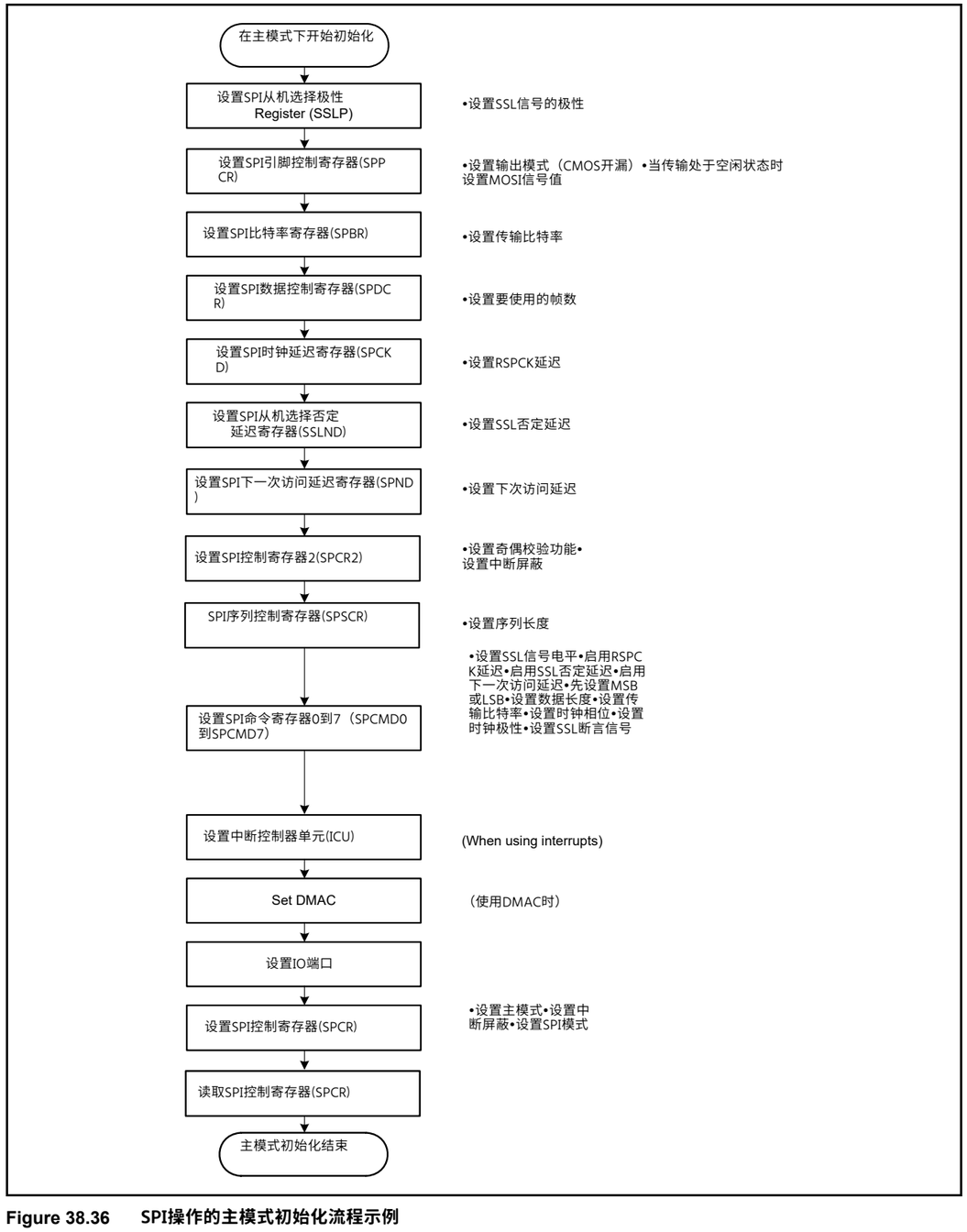


Figure 38.36 SPI操作的主模式初始化流程示例

(9) 软件处理流程

图38.37至图38.39显示了软件处理流程的示例。

(a) Transmit processing flow

When transmitting data and when the SPIi_SPII interrupt is enabled, the CPU is notified of the completion of data transmission after the last writing of data for transmission.

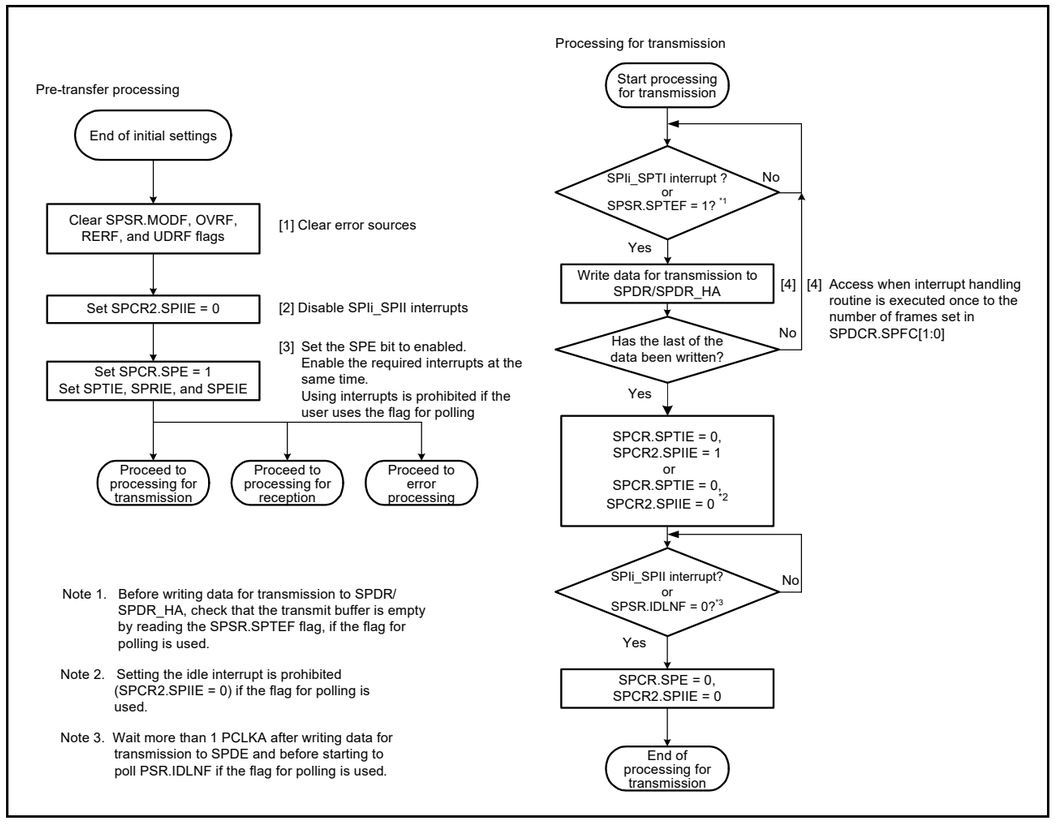


Figure 38.37 Transmission flow in master mode transmission

(b) Receive processing flow

The SPI does not handle receive-only operation, so processing for transmission is required.

(a) 传输处理流程

发送数据时和SPIi_SPII中断使能时，在最后一次写入发送数据后通知CPU数据发送完成。

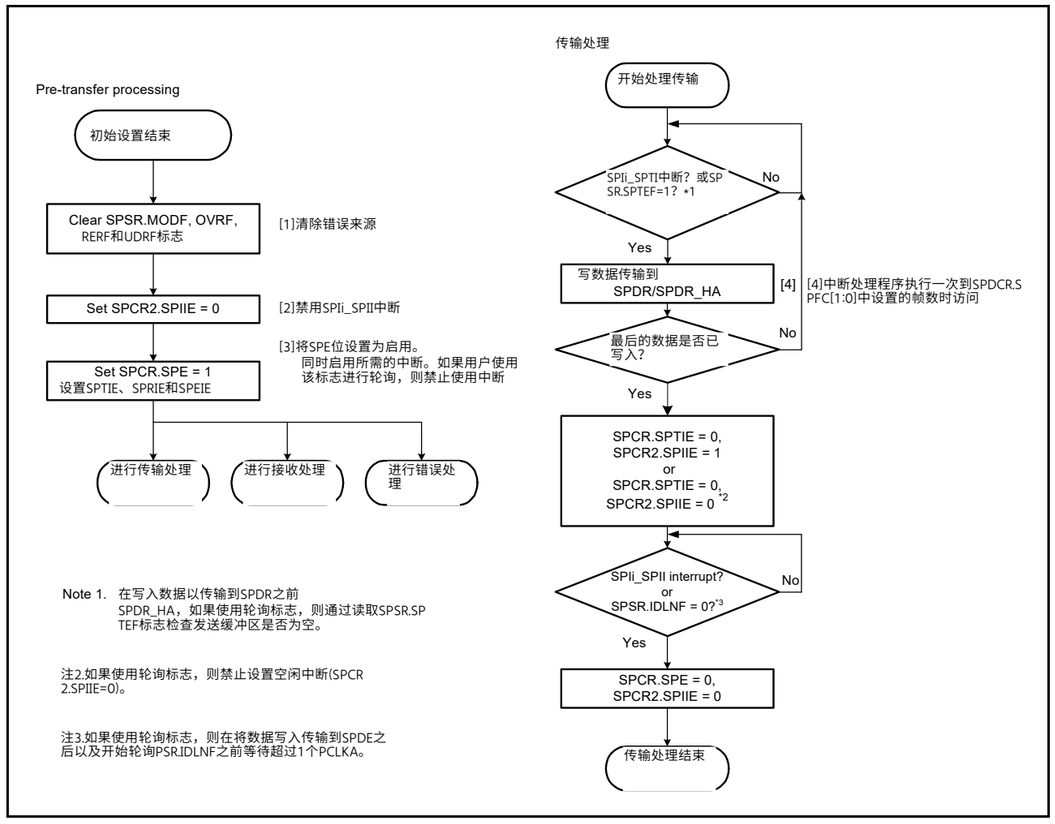


Figure 38.37 主模式传输中的传输流程

(b) 接收处理流程

SPI不处理只接收操作，因此需要处理传输。

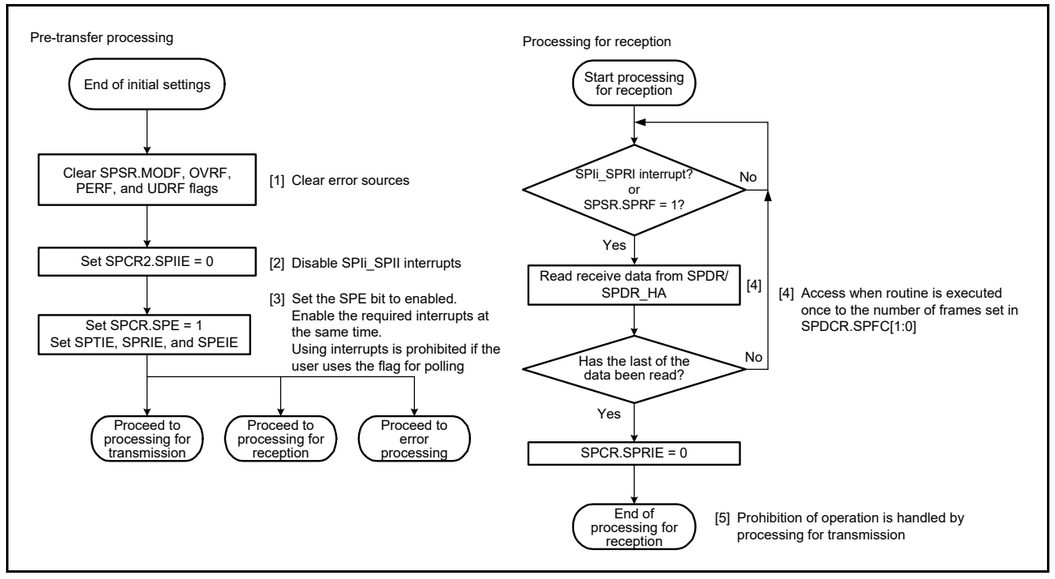


Figure 38.38 Reception flow in master mode

(c) Error processing flow

The SPI detects mode fault errors, underrun errors, overrun errors, and parity errors. When a mode fault error is generated, the SPCR.SPE bit is automatically cleared, stopping operations for transmission and reception. For errors from other sources, the SPCR.SPE bit is not cleared and operations for transmission and reception continue. Therefore, Renesas recommends clearing the SPCR.SPE bit to stop operations for errors other than mode fault errors. Not doing so leads to updating of the SPSSR.SPECM[2:0] bits.

When an error is detected by using an interrupt, clear the ICU.IELSRn.IR flag in the error processing routine. If this is not done, the ICU.IELSRn.IR flag might continue to indicate the SPIi_SPTI or SPIi_SPRI interrupt request. If the SPIi_SPRI interrupt request is indicated, read the receive buffer and initialize the sequencer in the SPI.

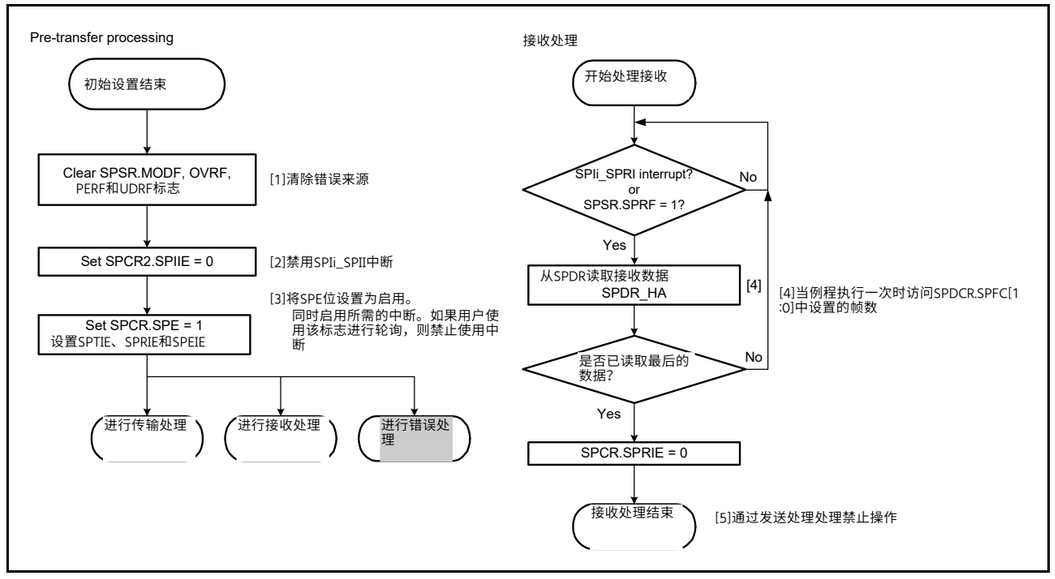


Figure 38.38 主模式下的接收流程

(c) 错误处理流程

SPI检测模式故障错误、欠载错误、溢出错误和奇偶校验错误。当产生模式故障错误时，SPCR.SPE位自动清零，停止发送和接收操作。对于其他来源的错误，SPCR.SPE位不会被清除，发送和接收操作会继续。因此，瑞萨建议清除SPCR.SPE位以停止除模式故障错误以外的错误操作。不这样做会导致更新SPSSR.SPECM[2:0]位。

当使用中断检测到错误时，清除错误处理例程中的ICU.IELSRn.IR标志。如果不这样做，ICU.IELSRn.IR标志可能会继续指示SPIi_SPTI或SPIi_SPRI中断请求。如果指示了SPIi_SPRI中断请求，则读取接收缓冲区并初始化SPI中的定序器。

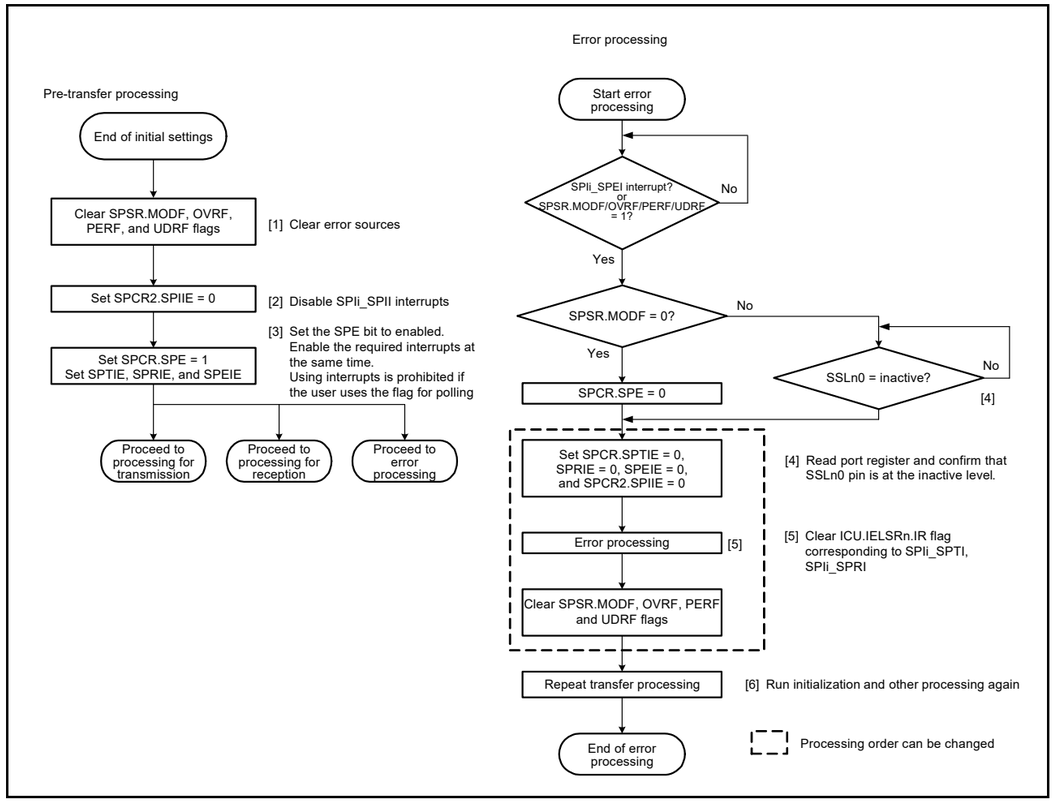


Figure 38.39 Error processing flow for master mode

38.3.10.2 Slave mode operation

(1) Starting a serial transfer

When the SPCMD0.CPHA bit is 0, if the SPI detects an SSLn0 input signal assertion, it must drive valid data to the MISOn output signal. For this reason, when the CPHA bit is 0, the assertion of the SSLn0 input signal triggers the start of a serial transfer.

When the CPHA bit is 1, if the SPI detects the first RSPCKn edge in an SSLn0 signal asserted condition, it must drive valid data to the MISOn output signal. For this reason, when the CPHA bit is 1, the first RSPCKn edge in an SSLn0 signal asserted condition triggers the start of a serial transfer.

Regardless of the CPHA bit setting, the SPI drives the MISOn output signal on SSLn0 signal assertion. The data that is output by the SPI is either valid or invalid, depending on the CPHA bit setting.

For details on the SPI transfer format, see section 38.3.5, Transfer Formats. The polarity of the SSLn0 input signal depends on the SSLP.SSL0P setting.

(2) Terminating a serial transfer

Regardless of the SPCMD0.CPHA bit setting, the SPI terminates the serial transfer after detecting an RSPCKn edge corresponding to the final sampling timing. When free space is available in the receive buffer (the SPSR.SPRF flag is 0), on termination of serial transfer, the SPI copies received data from the shift register to the receive buffer of the SPDR/SPDR_HA register. On termination of a serial transfer, the SPI changes the status of the shift register to empty, regardless of the receive buffer state. A mode fault error occurs if the SPI detects an SSLn0 input signal negation from the beginning of serial transfer to the end of serial transfer (see section 38.3.8, Error Detection).

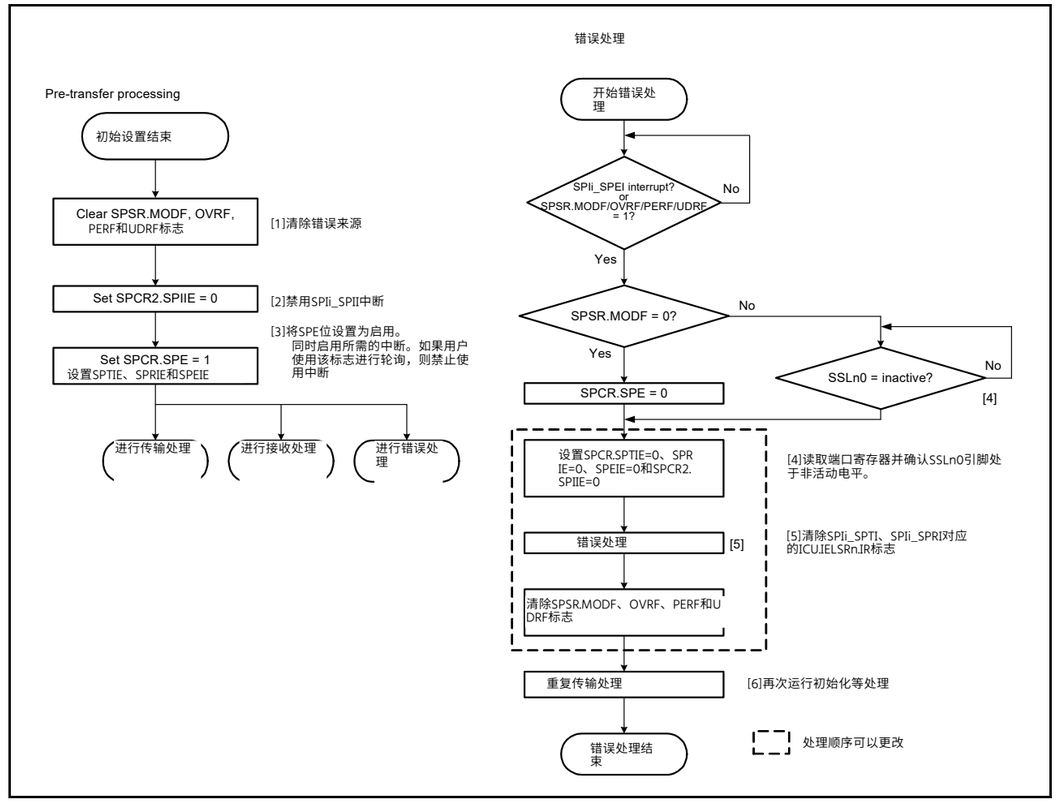


Figure 38.39 主模式的错误处理流程

38.3.10.2 从模式操作

(1) 开始串行传输

当SPCMD0.CPHA位为0时，如果SPI检测到SSLn0输入信号断言，它必须将有效数据驱动到MISon输出信号。因此，当CPHA位为0时，SSLn0输入信号的断言触发串行传输的开始。

当CPHA位为1时，如果SPI在SSLn0信号置位条件下检测到第一个RSPCKn边沿，它必须将有效数据驱动到MISOn输出信号。因此，当CPHA位为1时，SSLn0信号断言条件中的第一个RSPCKn边沿触发串行传输的开始。

无论CPHA位设置如何，SPI都会在SSLn0信号置位时驱动MIOn输出信号。SPI输出的数据是有效还是无效，取决于CPHA位设置。

有关SPI传输格式的详细信息，请参阅第38.3.5节，传输格式。SSLn0输入信号的极性取决于SSLP.SSL0P设置。

(2) 终止串行传输

无论SPCMD0.CPHA位设置如何，SPI在检测到对应于最终采样时序的RSPCKn边沿后终止串行传输。当接收缓冲区中有可用空间（SPSR.SPRF标志为0）时，串行传输终止时，SPI将接收到的数据从移位寄存器复制到SPDR/SPDR_HA寄存器的接收缓冲区。在串行传输终止时，SPI将移位寄存器的状态更改为空，而与接收缓冲区状态无关。如果SPI从串行传输开始到串行传输结束检测到SSLn0输入信号取反，则会发生模式故障错误（请参阅第38.3.8节，错误检测）。

The final sampling timing changes depending on the bit length of transfer data. In slave mode, the SPI data length is determined by the SPCMD0.SPB[3:0] bit setting. The polarity of the SSLn0 input signal is determined by the SSLP.SSL0P bit setting. For details on the SPI transfer format, see section 38.3.5, Transfer Formats.

(3) Notes on single slave operations

If the SPCMD0.CPHA bit is 0, the SPI starts serial transfers when it detects the assertion edge for an SSLn0 input signal. In the type of configuration shown in Figure 38.7, for example, if the SPI is used in single slave mode, the SSLn0 signal is fixed at the active state. Therefore, when the CPHA bit is set to 0, the SPI cannot correctly start a serial transfer. To correctly execute transmit and receive operations by the SPI in slave mode when the SSLn0 input signal is fixed at the active state, the CPHA bit must be set to 1. Do not fix the SSLn0 input signal if there is a requirement for setting the CPHA bit to 0.

(4) Burst transfer

If the SPCMD0.CPHA bit is 1, continuous serial transfer (burst transfer) can be executed while retaining the assertion state for the SSLn0 input signal. When the CPHA bit is 1, the serial transfer period is the period from the first RSPCKn edge to the sampling timing for the reception of the final bit in an SSLn0 signal active state. Even when the SSLn0 input signal remains at the active level, the SPI can accommodate burst transfers, because it can detect the start of an access.

When the CPHA bit is 0, the second and subsequent serial transfers during burst transfer cannot be executed correctly.

(5) Initialization flow

Figure 38.40 shows an example of initialization flow for SPI operation when the SPI is used in slave mode. For a description of how to set up the ICU, DMAC, and I/O ports, see the descriptions given in the individual blocks.

最终的采样时序根据传输数据的位长而变化。在从机模式下，SPI数据长度由SPCMD0.SPB[3:0]位设置决定。SSLn0输入信号的极性由SSLP.SSL0P位设置决定。有关SPI传输格式的详细信息，请参阅第38.3.5节，传输格式。

(3) 单从操作注意事项

如果SPCMD0.CPHA位为0，则SPI在检测到SSLn0输入信号的断言边沿时开始串行传输。例如，在图38.7所示的配置类型中，如果SPI用于单从模式，则SSLn0信号固定在活动状态。因此，当CPHA位设置为0时，SPI无法正确启动串行传输。当SSLn0输入信号固定为激活状态时，为了在从机模式下正确执行SPI的发送和接收操作，CPHA位必须设置为1。如果需要设置CPHA，请不要固定SSLn0输入信号位为0。

(4) 突发传输

如果SPCMD0.CPHA位为1，则可以执行连续串行传输（突发传输），同时保持SSLn0输入信号的断言状态。当CPHA位为1时，串行传输周期是从第一个RSPCKn边沿到SSLn0信号有效状态下接收最后一个位的采样时序的周期。即使SSLn0输入信号保持在有效电平，SPI也可以适应突发传输，因为它可以检测访问的开始。

当CPHA位为0时，突发传输期间的第二次和后续串行传输无法正确执行。

(5) 初始化流程

图38.40显示了当SPI用于从机模式时SPI操作的初始化流程示例。有关如何设置ICU、DMAC和IO端口的说明，请参见各个块中给出的说明。

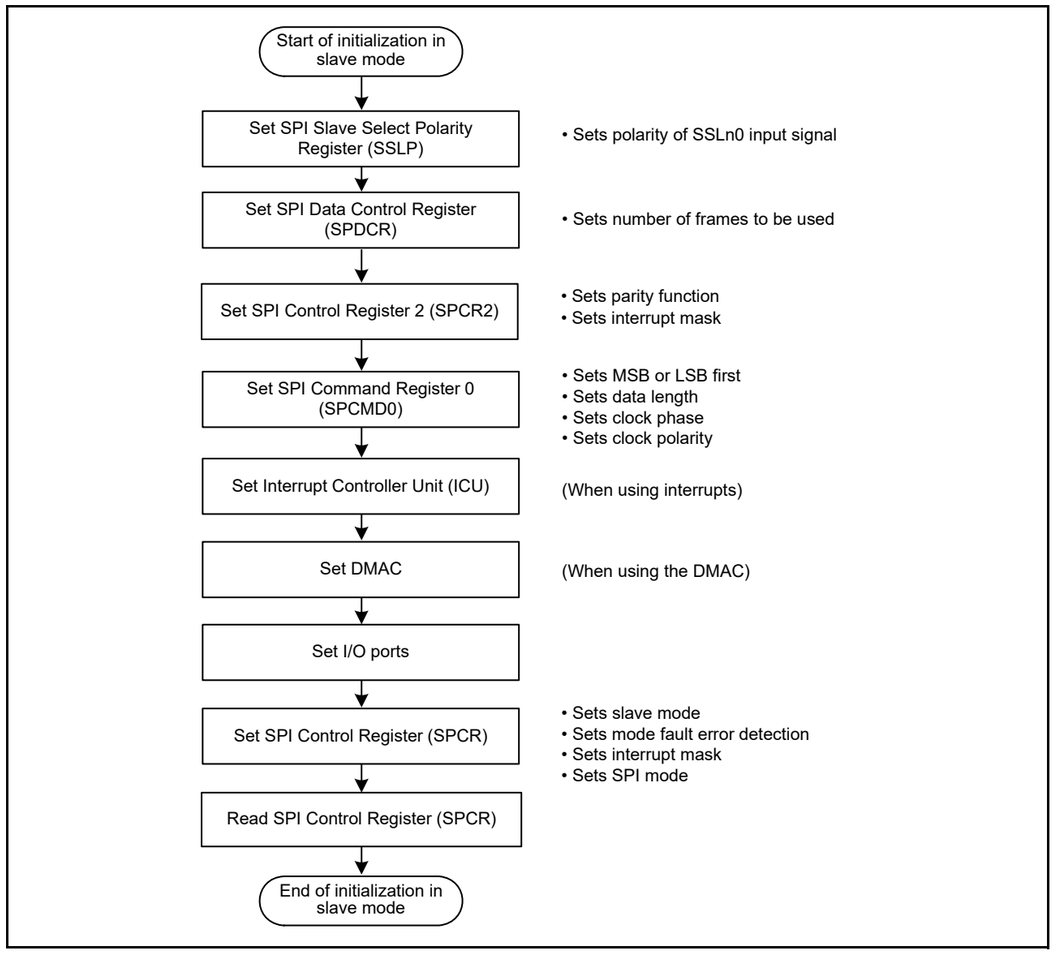


Figure 38.40 Example initialization flow in slave mode for SPI operation

(6) Software processing flow

Figure 38.41 to Figure 38.43 show examples of the flow of software processing.

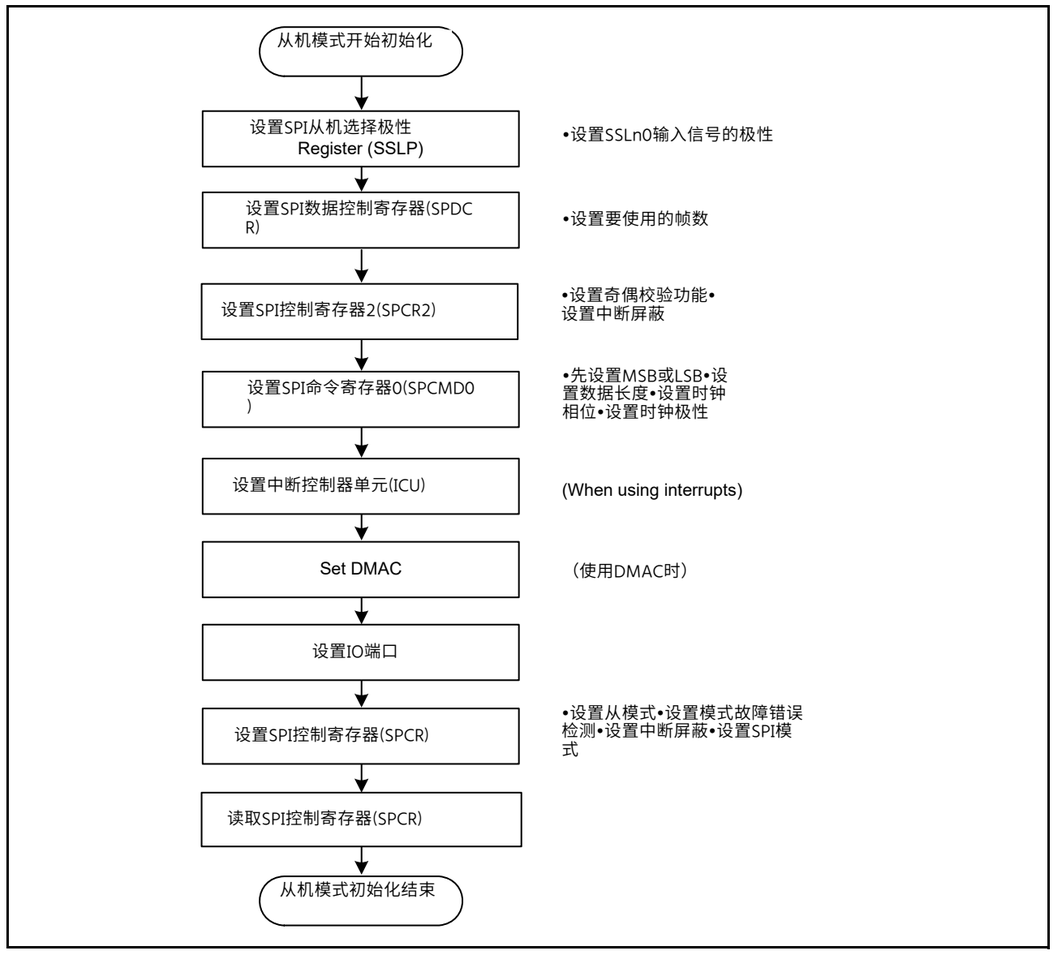
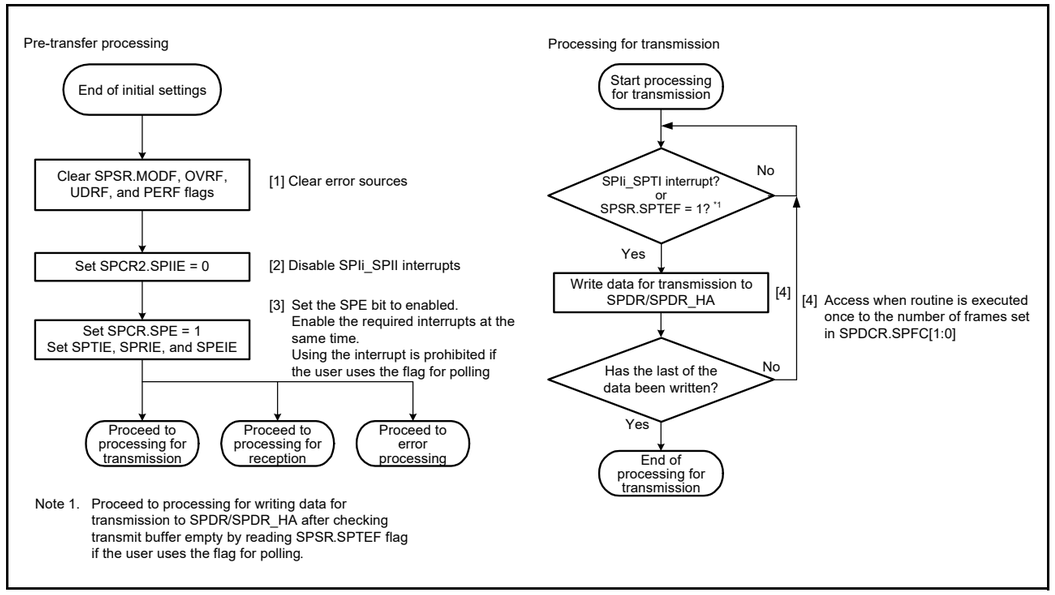


Figure 38.40 SPI操作的从模式初始化流程示例

(6) 软件处理流程

图38.41至图38.43显示了软件处理流程的示例。

(a) Transmit processing flow



Note 1. Proceed to processing for writing data for transmission to SPDR/SPDR_HA after checking transmit buffer empty by reading SPSR.SPTEF flag if the user uses the flag for polling.

Figure 38.41 Transmission flow in slave mode

(b) Receive processing flow

The SPI does not handle receive-only operation, so processing for transmission is required.

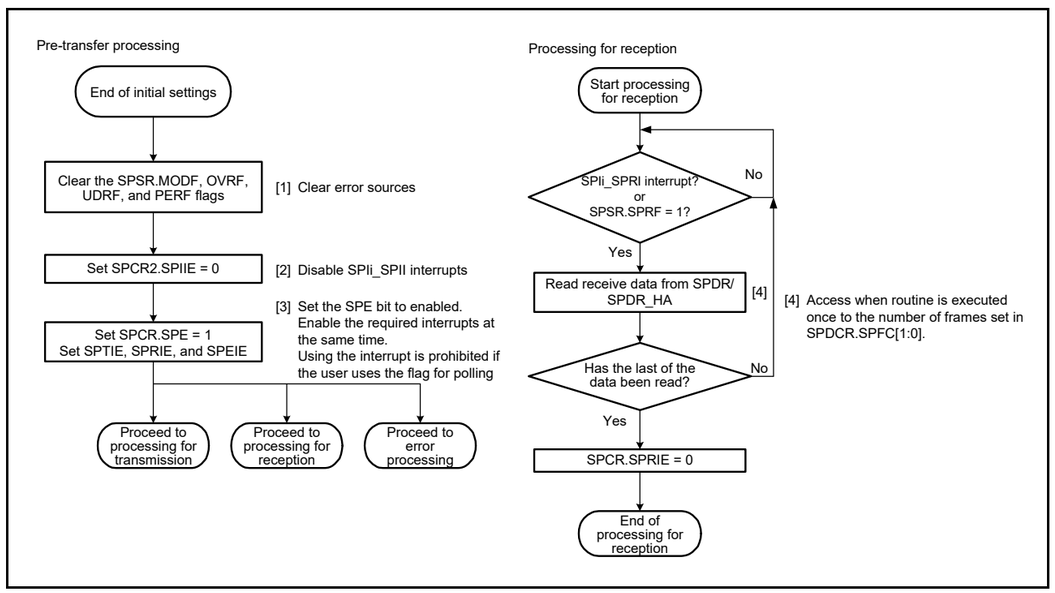
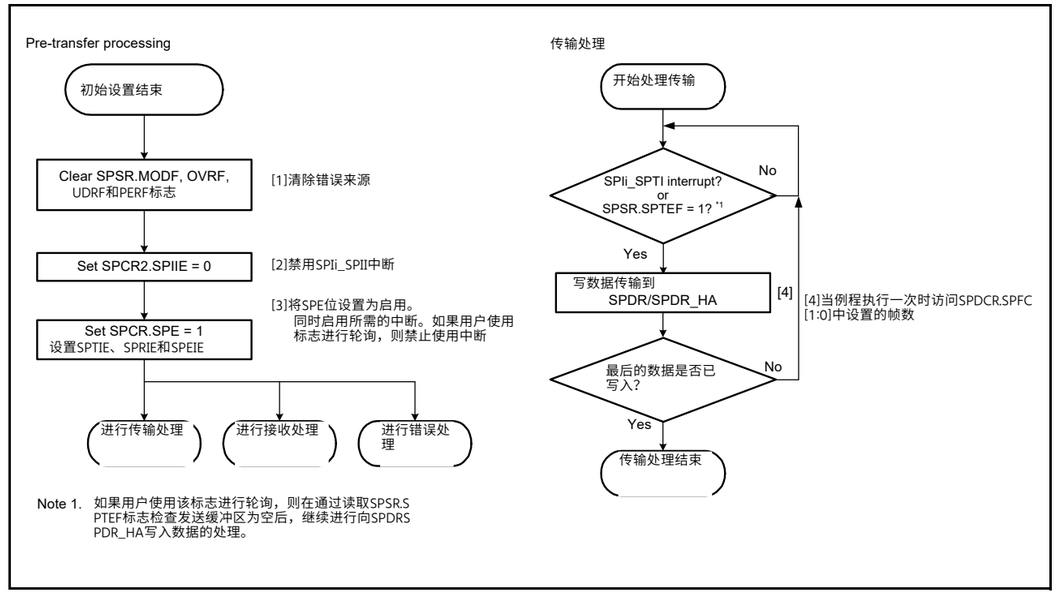


Figure 38.42 Reception flow in slave mode

(a) 传输处理流程



Note 1. 如果用户使用该标志进行轮询，则在通过读取SPSR.SPTEF标志检查发送缓冲区为空后，继续进行向SPDRSPDR_HA写入数据的处理。

Figure 38.41 从模式下的传输流

(b) 接收处理流程

SPI不处理只接收操作，因此需要处理传输。

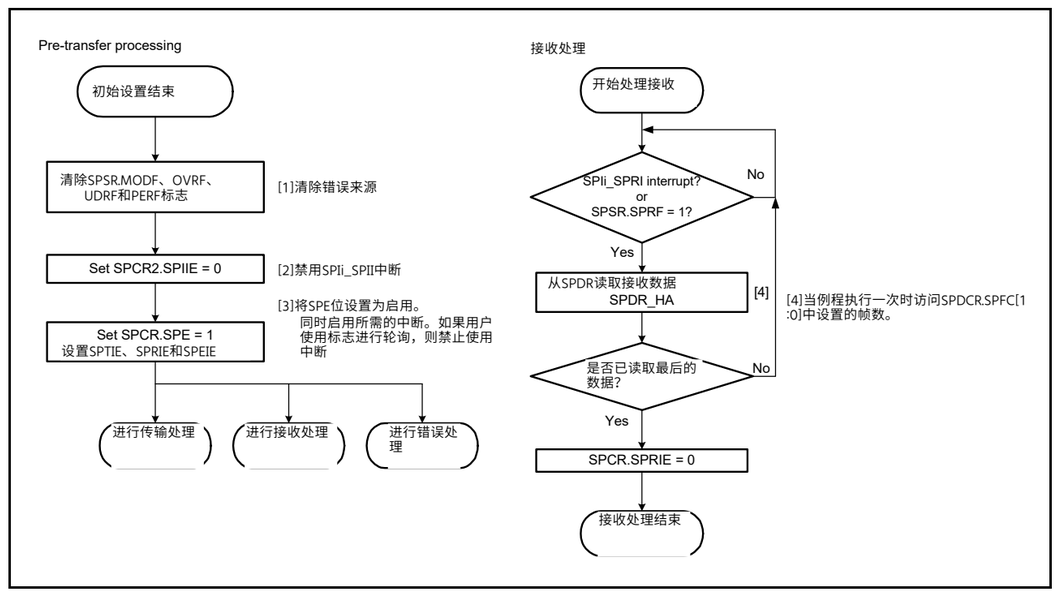


Figure 38.42 从机模式下的接收流程

(c) Error processing flow

In slave operation, even when a mode fault error is generated, the SPSR.MODF flag can be cleared regardless of the state of the SSLn0 pin.

When an error is detected by using an interrupt, clear the ICU.IELSRn.IR flag in the error processing routine. If this is not done, the ICU.IELSRn.IR flag might continue to indicate the SPIi_SPTI or SPIi_SPRI interrupt request. If the SPIi_SPRI interrupt request is indicated, read the receive buffer and initialize the sequencer in the SPI.

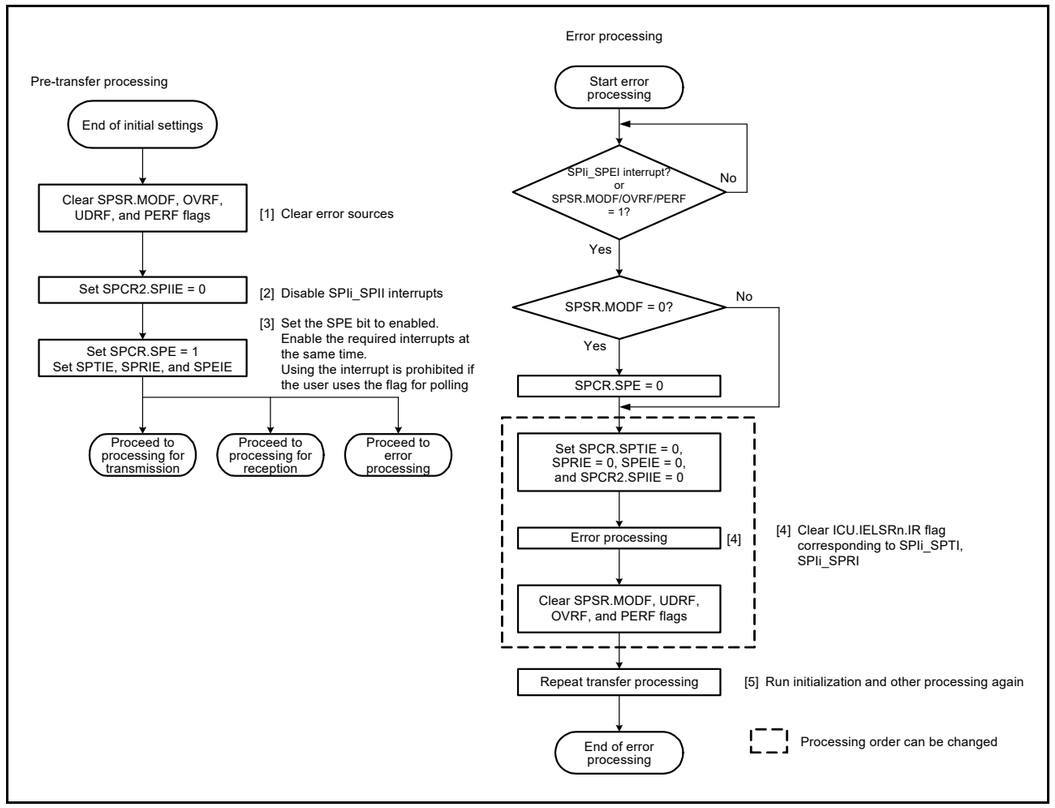


Figure 38.43 Error processing flow for slave mode

38.3.11 Clock Synchronous Operation

Setting the SPCR.SPMS bit to 1 selects clock synchronous operation of the SPI. In clock synchronous operation, the SSLni pin is not used, and the RSPCKn, MOSIn, and MISOn pins handle communications. All SSLni pins are available as I/O port pins.

Although clock synchronous operation does not require the use of the SSLni pin, operation of the module is the same as in SPI operation. In both master and slave operations, communications can be performed with the same flow as in SPI operation. However, mode fault errors are not detected, because the SSLni pin is not used.

Additionally, do not perform operation if clock synchronous operation enabled when the SPCMDm.CPHA bit is set to 0 in slave mode (SPCR.MSTR = 0).

(c) 错误处理流程

在从机操作中，即使产生模式故障错误，SPSR.MODF标志也可以被清除，而与SSLn0引脚的状态无关。

当使用中断检测到错误时，清除错误处理例程中的ICU.IELSRn.IR标志。如果不这样做，ICU.IELSRn.IR标志可能会继续指示SPIi_SPTI或SPIi_SPRI中断请求。如果指示了SPIi_SPRI中断请求，则读取接收缓冲区并初始化SPI中的定序器。

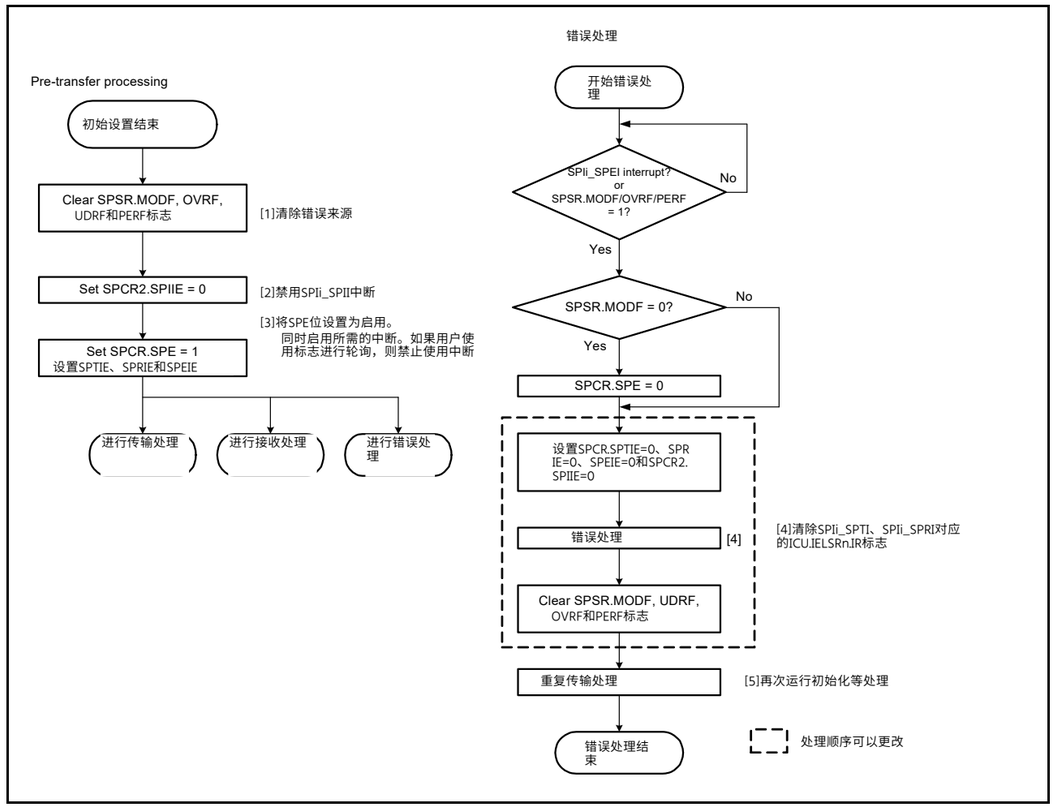


Figure 38.43 从机模式的错误处理流程

38.3.11 时钟同步操作

将SPCR.SPMS位设置为1可选择SPI的时钟同步操作。在时钟同步操作中，不使用SSLni引脚，而RSPCKn、MOSIn和MISOn引脚处理通信。所有SSLni引脚都可用作IO端口引脚。

虽然时钟同步操作不需要使用SSLni引脚，但模块的操作与SPI操作相同。在主机和从机操作中，可以使用与SPI操作相同的流程执行通信。但是，未检测到模式故障错误，因为未使用SSLni引脚。

此外，如果在从模式(SPCR.MSTR=0)下SPCMDm.CPHA位设置为0时时钟同步操作使能，则不要执行操作。

38.3.11.1 Master mode operation

(1) Starting serial transfer

The SPI updates the data in the transmit buffer (SPTX) of SPDR/SPDR_HA when data is written to the SPDR/SPDR_HA register and the transmit buffer is empty (data for the next transfer is not set and the SPSR.SPTEF flag is 1). When the shift register is empty after the number of frames set in the SPDCR.SPFC[1:0] bits are written to the SPDR/SPDR_HA, the SPI copies data from the transmit buffer to the shift register and starts serial transmission. On copying transmit data to the shift register, the SPI changes the status of the shift register to full, and on termination of serial transfer, it changes the status of the shift register to empty. The status of the shift register cannot be referenced.

Transfer in clock synchronous operation is conducted without the SSLn0 output signal. For details on the SPI transfer format, see section 38.3.5, Transfer Formats.

(2) Terminating serial transfer

The SPI terminates the serial transfer after transmitting an RSPCKn edge corresponding to the sampling timing. If free space is available in the receive buffer (the SPSR.SPRF flag is 0), on termination of serial transfer, the SPI copies data from the shift register to the receive buffer of the SPI Data Register (SPDR/SPDR_HA).

The final sampling timing varies depending on the bit length of transfer data. In master mode, the SPI data length depends on the SPCMDm.SPB[3:0] bit setting. Transfer in clock synchronous operation is conducted without the SSLn0 output signal. For details on the SPI transfer format, see section 38.3.5, Transfer Formats.

(3) Sequence control

The transfer format used in master mode is determined by the SPSCR, SPCMDm, SPBR, SPCKD, SSLND, and SPND registers. Although the SSLni signals are not output in clock synchronous operation, these settings are valid.

The SPSCR register determines the sequence configuration for serial transfers that are executed by the SPI in master mode. The following parameters are specified in the SPCMDm register:

- SSLni output signal value
- MSB or LSB first
- Data length
- Some of the bit rate settings
- RSPCKn polarity and phase
- Whether SPCKD is to be referenced
- Whether SSLND is to be referenced
- Whether SPND is to be referenced.

SPBR holds some of the bit rate settings such as SPCKD, an SPI clock delay value, SSLND, an SSL negation delay, and SPND, a next-access delay value.

Based on the sequence length that is assigned to SPSCR, the SPI makes up a sequence comprised of a part or all of SPCMDm register. The SPI contains a pointer to the SPCMDm register that makes up the sequence. The value of this pointer can be checked by reading the SPSSR.SPCP[2:0] bits. When the SPCR.SPE bit is set to 1 and the SPI function is enabled, the SPI loads the pointer to the commands in SPCMD0 register, and incorporates the SPCMD0 register setting into the transfer format at the beginning of serial transfer. The SPI increments the pointer each time the next-access delay period for a data transfer ends. On completion of the serial transfer that corresponds to the final command comprising the sequence, the SPI sets the pointer to the SPCMD0 register, and in this manner the sequence is executed repeatedly.

38.3.11.1 主模式操作

(1) 开始串行传输

SPI更新SPDRSPDR_HA的发送缓冲区(SPTX)中的数据
SPDRSPDR_HA寄存器且发送缓冲区为空（未设置下一次传输的数据且SPSR.SPTEF标志为1）。当SPDCR.SPFC[1:0]位中设置的帧数写入SPDRSPDR_HA后移位寄存器为空时，SPI将数据从发送缓冲区复制到移位寄存器并开始串行传输。将发送数据复制到移位寄存器时，SPI将移位寄存器的状态更改为满，而在串行传输终止时，它将移位寄存器的状态更改为空。无法引用移位寄存器的状态。

在没有SSLn0输出信号的情况下进行时钟同步操作的传输。有关SPI传输格式的详细信息，请参阅第38.3.5节，传输格式。

(2) 终止串行传输

SPI在发送对应于采样时序的RSPCKn边沿后终止串行传输。如果接收缓冲区中有可用空间（SPSR.SPRF标志为0），则在串行传输终止时，SPI将数据从移位寄存器复制到SPI数据寄存器(SPDRSPDR_HA)的接收缓冲区。

最终的采样时序根据传输数据的位长而变化。在主机模式下，SPI数据长度取决于SPMDm.SPB[3:0]位设置。在没有SSLn0输出信号的情况下进行时钟同步操作的传输。有关SPI传输格式的详细信息，请参阅第38.3.5节，传输格式。

(3) 顺序控制

主机模式中使用的传输格式由SPSCR、SPCMDm、SPBR、SPCKD、SSLND和SPND寄存器确定。虽然在时钟同步操作中不输出SSLni信号，但这些设置是有效的。

SPSCR寄存器确定由SPI在主模式下执行的串行传输的序列配置。SPCMDm寄存器中指定了以下参数：

- SSLni输出信号值
- MSB或LSB在前
- 数据长度
- 一些比特率设置
- RSPCKn极性和相位
- 是否要引用SPCKD
- 是否要引用SSLND
- 是否要引用SPND。

SPBR保存一些比特率设置，例如SPCKD、SPI时钟延迟值、SSLND、SSL否定延迟和
SPND，下一次访问延迟值。

根据分配给SPSCR的序列长度，SPI组成一个序列，该序列由部分或全部
SPMDm寄存器。SPI包含一个指向构成序列的SPCMDm寄存器的指针。该指针的值可以通过读取SPSSR.SPCP[2:0]位来检查。当SPCR.SPE位设置为1且SPI功能使能时，SPI将指针加载到SPCMD0寄存器中的命令，并在串行传输开始时将SPCMD0寄存器设置合并到传输格式中。每次数据传输的下一个访问延迟周期结束时，SPI都会递增指针。在完成对应于包含序列的最终命令的串行传输后，SPI将指针设置为SPMD0寄存器，并以这种方式重复执行序列。

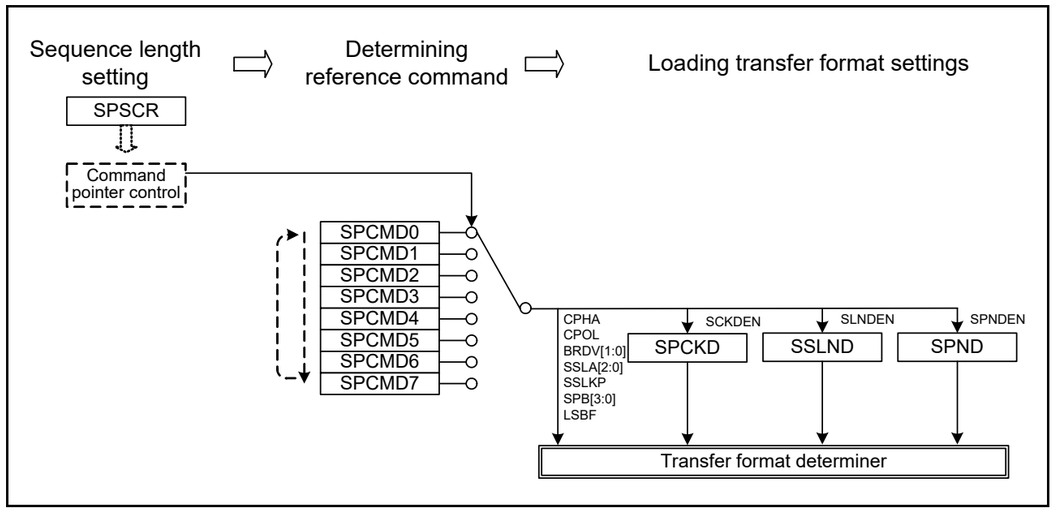


Figure 38.44 Procedure for determining the form of serial transmission in master mode

In this section, a frame is the combination of the data (SPDR/SPDR_HA) and the settings (SPCMDm).

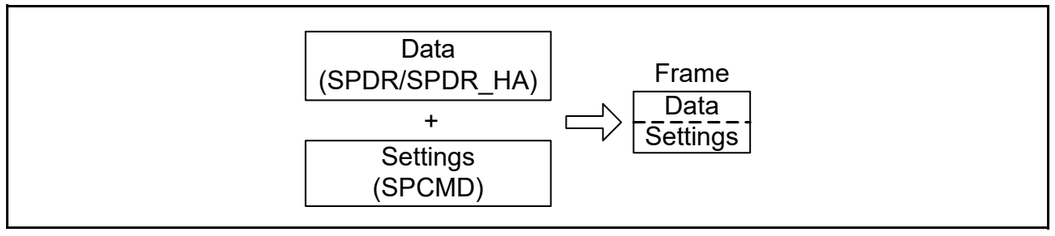


Figure 38.45 Conceptual diagram of frames

Figure 38.46 shows the relationship between the command and the transmit and receive buffers in the sequence of operations specified by the settings in Table 38.4.

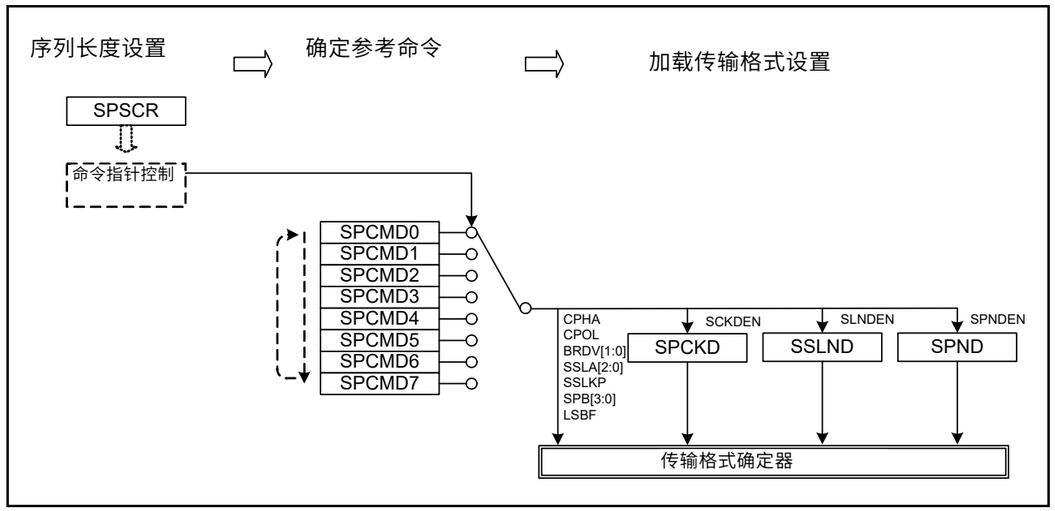


Figure 38.44 确定主机模式下串行传输形式的程序

在本节中，帧是数据(SPDRSPDR_HA)和设置(SPCMDm)的组合。

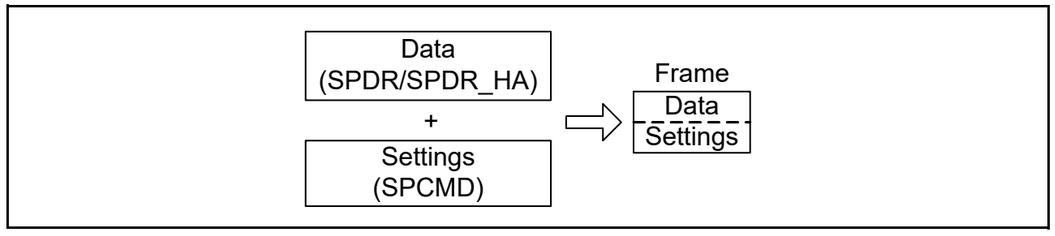


Figure 38.45 框架的概念图

图38.46显示了在表38.4中的设置指定的操作序列中命令与发送和接收缓冲区之间的关系。

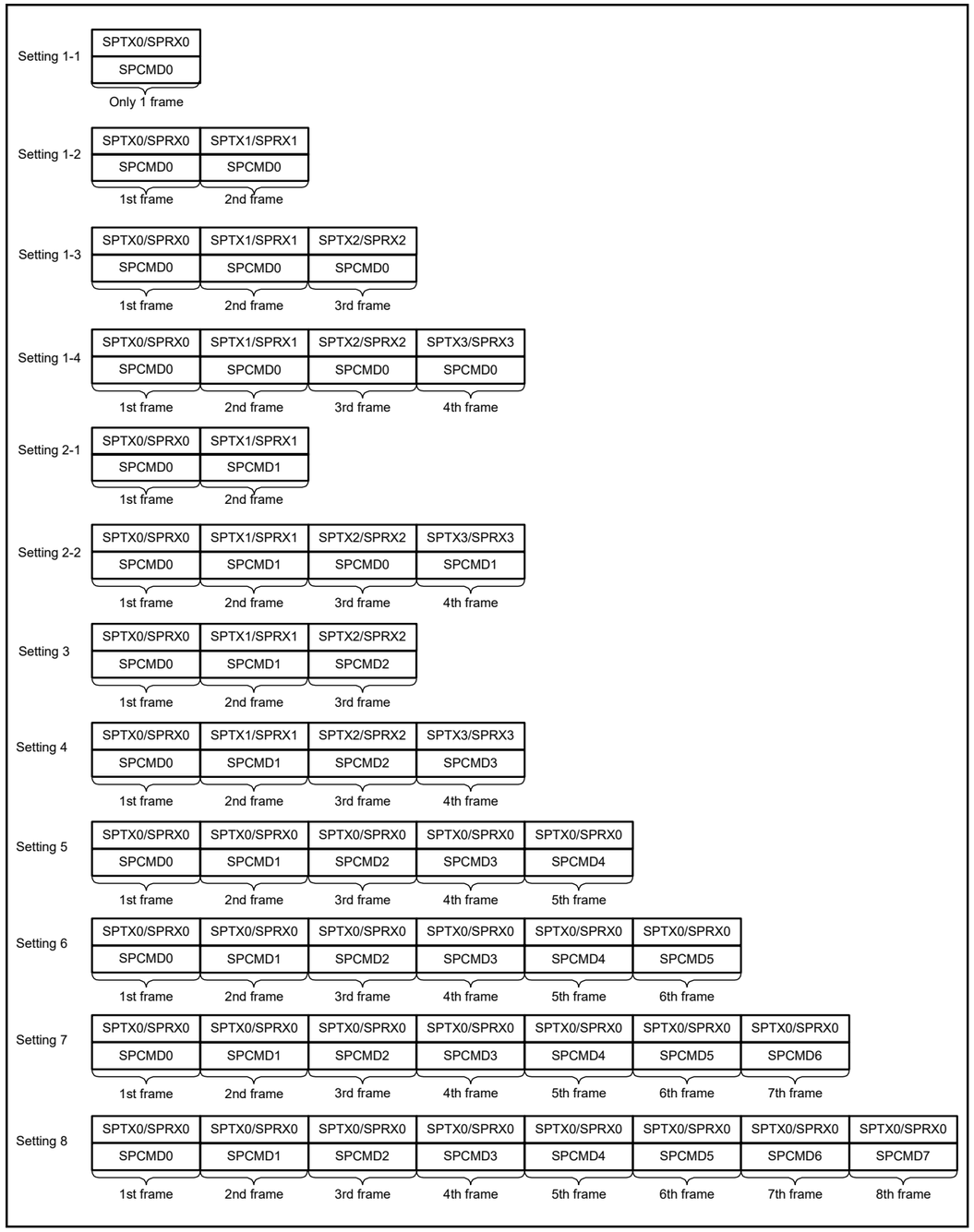


Figure 38.46 Correspondence between SPI Command Register and transmit and receive buffers in sequence operations

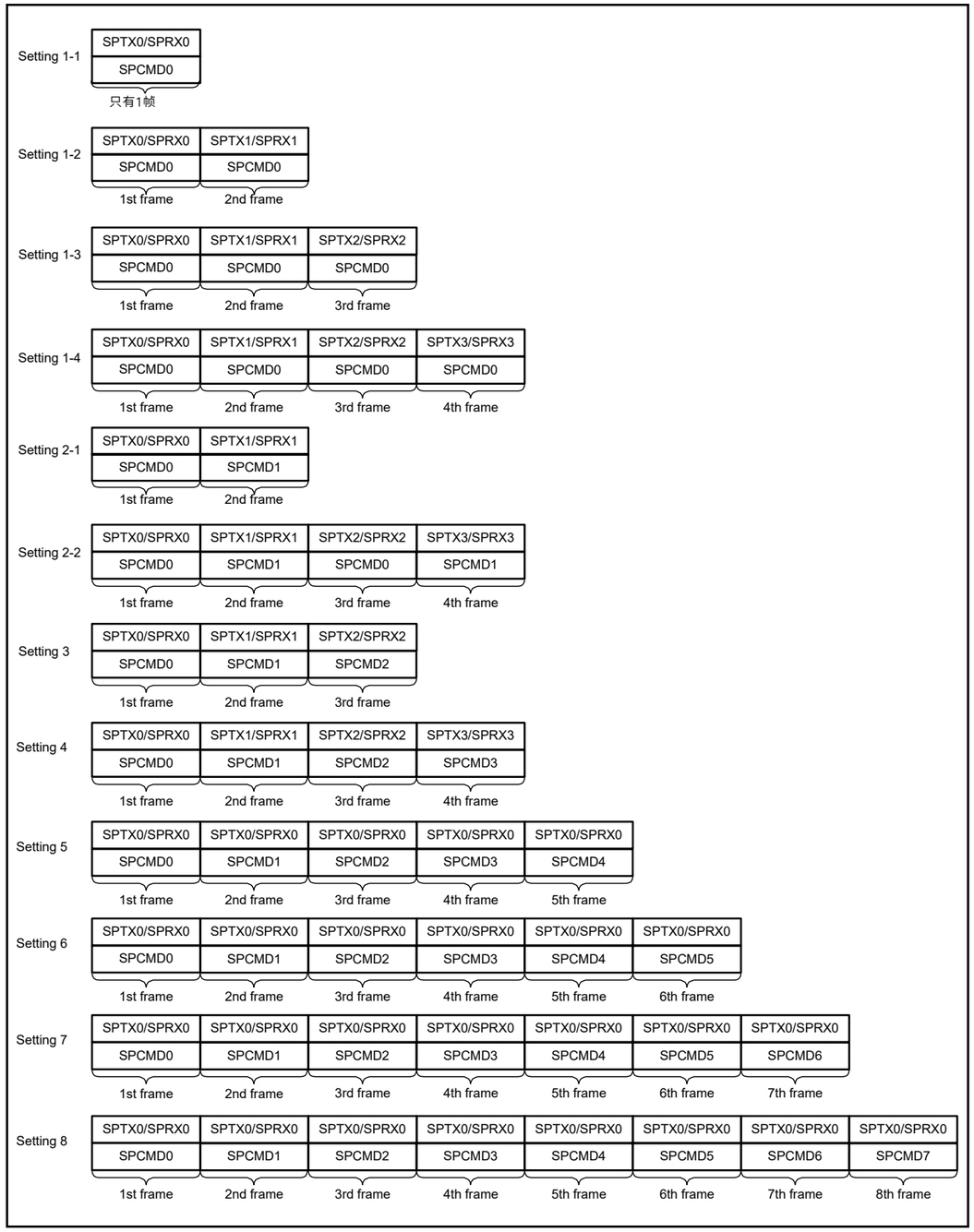


Figure 38.46 顺序操作中SPI命令寄存器与发送接收缓冲区的对应关系

(4) Initialization flow

Figure 38.47 shows an example of initialization flow for clock synchronous operation when the SPI is used in master mode. For a description of how to set up the ICU, DMAC, and I/O ports, see the descriptions given in the individual blocks.

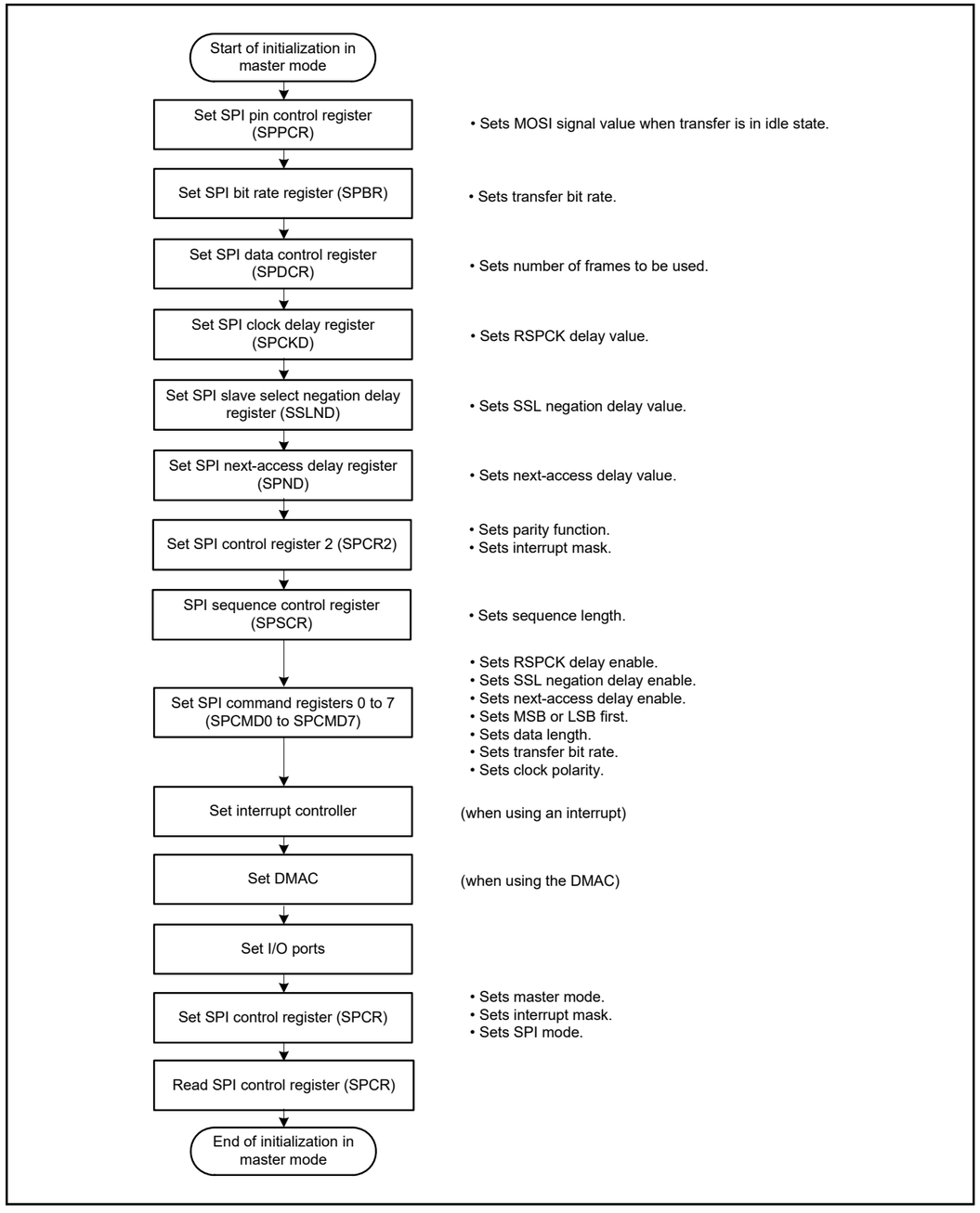


Figure 38.47 Example of initialization flow in master mode for clock synchronous operation

(4) 初始化流程

图38.47显示了在主模式下使用SPI时时钟同步操作的初始化流程示例。有关如何设置ICU、DMAC和IO端口的说明，请参见各个块中给出的说明。

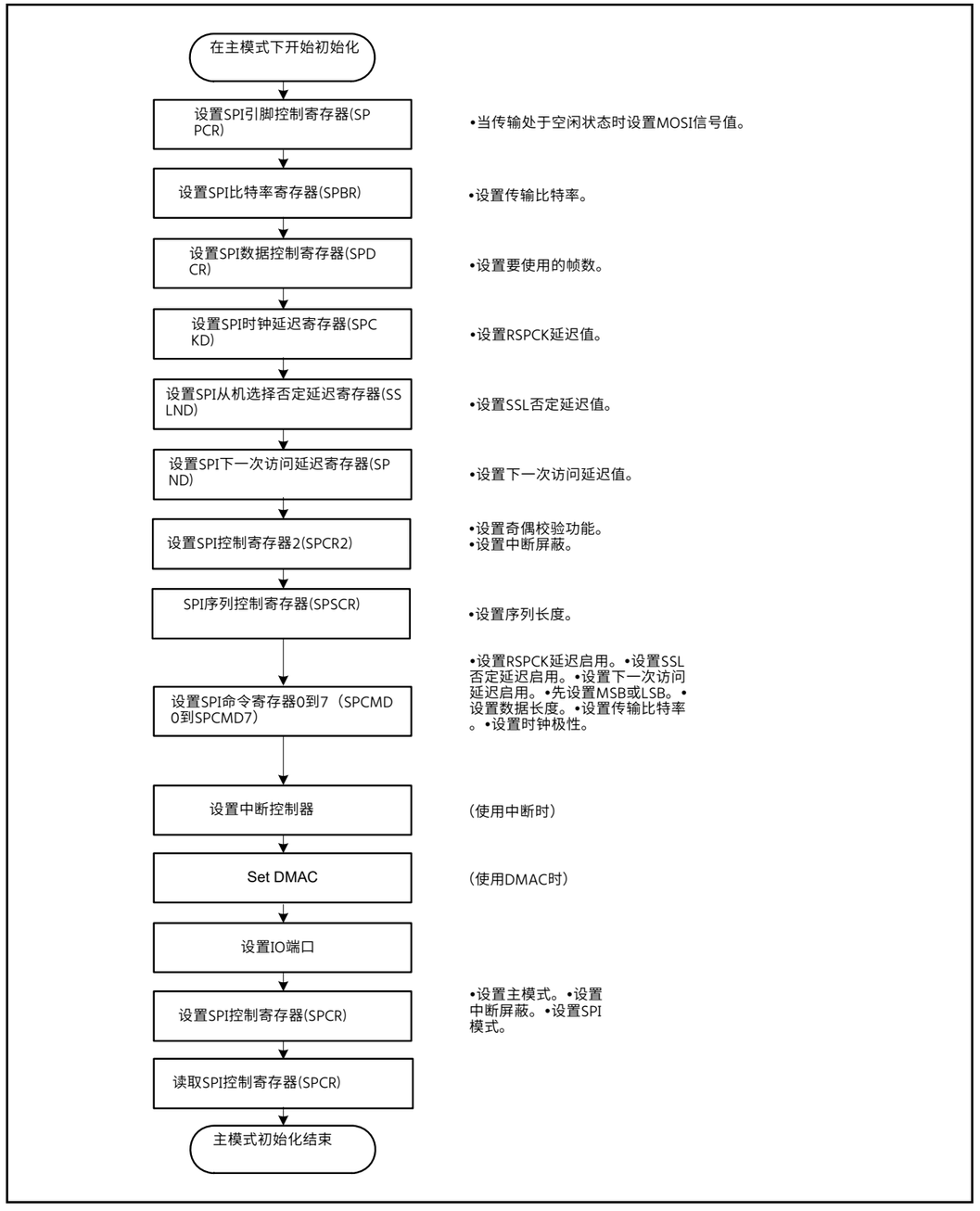


Figure 38.47 时钟同步操作的主模式初始化流程示例

(5) Software processing flow

Software processing during clock synchronous master operation is the same as that for SPI master operation. For details, see section 38.3.10.1, (9) Software processing flow. Mode fault errors do not occur in clock synchronous operation.

38.3.11.2 Slave mode operation

(1) Starting serial transfer

When the SPCR.SPMS bit is 1, the first RSPCKn edge triggers the start of a serial transfer in the SPI, and the SPI drives the MISOn output signal. The SSLn0 input signal is not used in clock synchronous operation. For details on the SPI transfer format, see section 38.3.5, Transfer Formats.

(2) Terminating serial transfer

The SPI terminates the serial transfer after detecting an RSPCKn edge corresponding to the final sampling timing. When free space is available in the receive buffer (the SPSR.SPRF flag is 0), on termination of serial transfer the SPI copies received data from the shift register to the receive buffer of the SPDR/SPDR_HA register. On termination of a serial transfer the SPI changes the status of the shift register to empty regardless of the receive buffer.

The final sampling timing changes depending on the bit length of transfer data. In slave mode, the SPI data length depends on the SPCMD0.SPB[3:0] bit setting. For details on the SPI transfer format, see section 38.3.5, Transfer Formats.

(3) Initialization flow

Figure 38.48 shows an example of initialization flow for clock synchronous operation when the SPI is used in slave mode. For a description of how to set up the ICU, DMAC, and I/O ports, see the descriptions given in the individual blocks.

(5) 软件处理流程

时钟同步主机操作期间的软件处理与SPI主机操作相同。详见38.3.10.1节，（9）软件处理流程。时钟同步操作中不会发生模式故障错误。

38.3.11.2 从模式操作

(1) 开始串行传输

当SPCR.SPMS位为1时，第一个RSPCKn边沿触发SPI中串行传输的开始，SPI驱动MISOn输出信号。SSLn0输入信号不用于时钟同步操作。有关SPI传输格式的详细信息，请参阅第38.3.5节，传输格式。

(2) 终止串行传输

SPI在检测到对应于最终采样时序的RSPCKn边沿后终止串行传输。当接收缓冲区中有可用空间时（SPSR.SPRF标志为0），在串行传输终止时，SPI将接收到的数据从移位寄存器复制到SPDRSPDR_HA寄存器的接收缓冲区。在串行传输终止时，SPI将移位寄存器的状态更改为空，而与接收缓冲区无关。

最终的采样时序根据传输数据的位长而变化。在从机模式下，SPI数据长度取决于SPCMD0.SPB[3:0]位设置。有关SPI传输格式的详细信息，请参阅第38.3.5节，传输格式。

(3) 初始化流程

图38.48显示了在从模式下使用SPI时时钟同步操作的初始化流程示例。有关如何设置ICU、DMAC和IO端口的说明，请参见各个块中给出的说明。

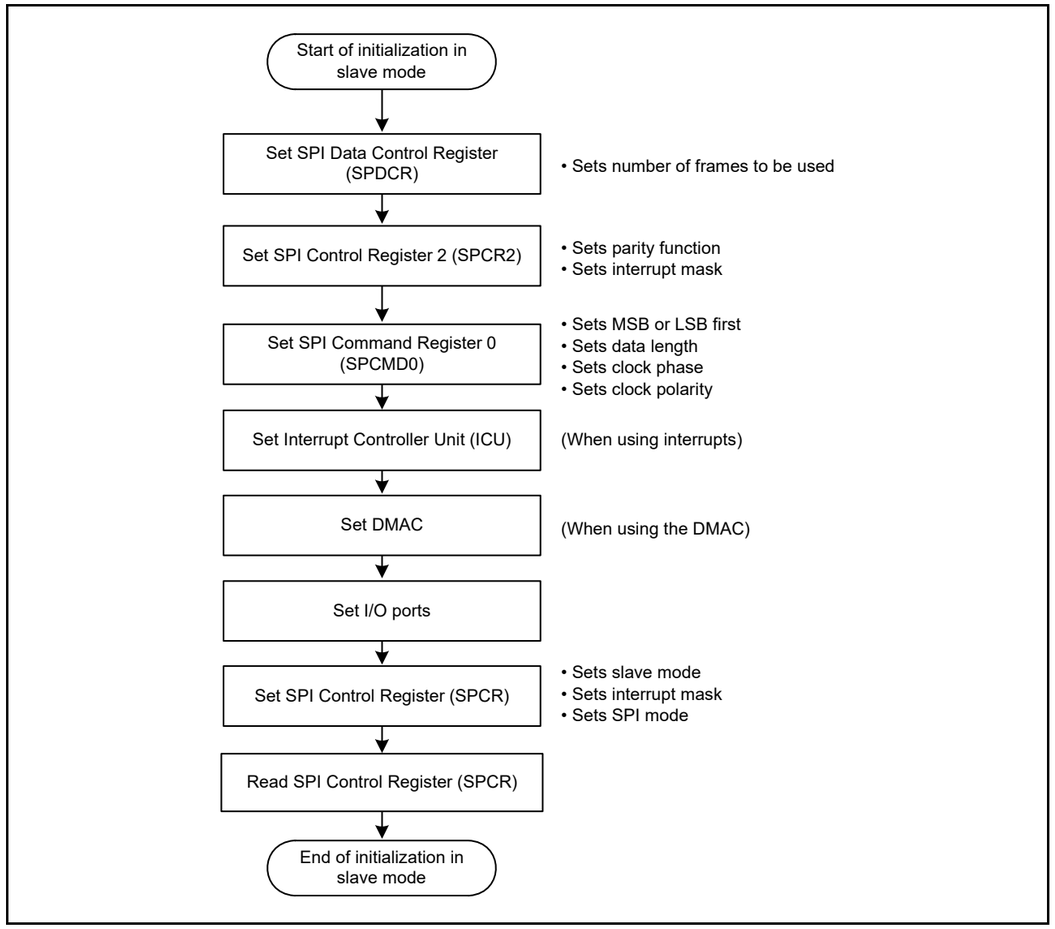


Figure 38.48 Example of initialization flow in slave mode for clock synchronous operation

(4) Software processing flow

Software processing during clock synchronous slave operation is the same as that for SPI slave operation. For details, see section 38.3.10.2, (6) Software processing flow. Mode fault errors do not occur in clock synchronous mode.

38.3.12 Loopback Mode

When 1 is written to the SPPCR.SPLP2 bit or SPPCR.SPLP bit, the SPI shuts off the path between the MISOn pin and the shift register if the SPCR.MSTR bit is 1, or between the MOSIn pin and the shift register if the SPCR.MSTR bit is 0, and connects the input and output paths of the shift register. The SPI does not shut off the path between the MOSIn pin and the shift register if the SPCR.MSTR bit is 1, or between the MISOn pin and the shift register if the SPCR.MSTR bit is 0. This is called loopback mode. When a serial transfer is executed in loopback mode, the transmit data for the SPI or the reversed transmit data becomes the received data for the SPI.

Table 38.12 lists the relationship between the SPLP2 and SPLP bits and the received data. Figure 38.49 shows the configuration of the shift register I/O paths when the SPI in master mode is set to loopback mode (SPPCR.SPLP2 = 1, SPPCR.SPLP = 0 or 1).

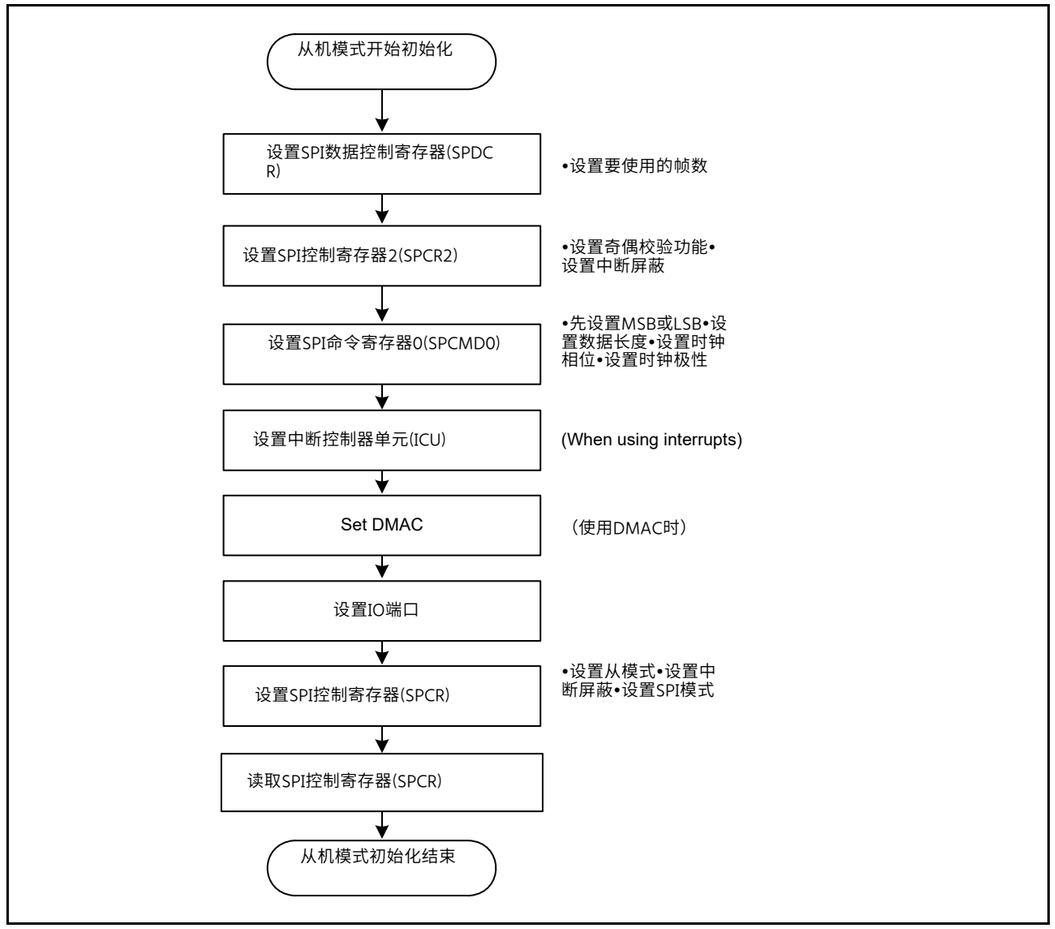


Figure 38.48 时钟同步操作的从模式初始化流程示例

(4) 软件处理流程

时钟同步从机操作期间的软件处理与SPI从机操作相同。详见38.3.10.2节，（6）软件处理流程。时钟同步模式下不会发生模式故障错误。

38.3.12 Loopback Mode

当向SPPCR.SPLP2位或SPPCR.SPLP位写入1时，如果SPCR.MSTR位为1，则SPI关闭MISOn引脚和移位寄存器之间的路径，或者如果SPCR.MSTR位为0，连接移位寄存器的输入和输出路径。如果SPCR.MSTR位为1，SPI不关闭MOSIn引脚和移位寄存器之间的路径，如果SPCR.MSTR位为0，则SPI不关闭MISOn引脚和移位寄存器之间的路径。这称为环回模式。当在环回模式下执行串行传输时，SPI的发送数据或反向发送数据将成为SPI的接收数据。

表38.12列出了SPLP2和SPLP位与接收数据之间的关系。图38.49显示了当主模式下的SPI设置为环回模式（SPPCR.SPLP2=1，SPPCR.SPLP=0或1）时移位寄存器IO路径的配置。

Table 38.12 SPLP2 and SPLP bit settings and received data

SPPCR.SPLP2 bit	SPPCR.SPLP bit	Received data
0	0	Input data from the MOSIn pin or MISOn pin
0	1	Inverted transmit data
1	0	Transmit data
1	1	Transmit data

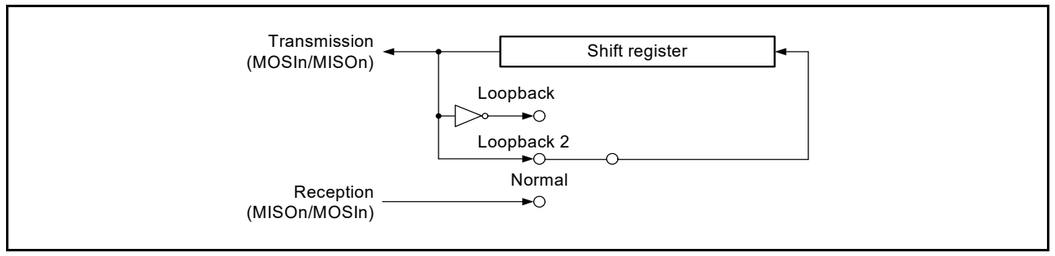


Figure 38.49 Configuration of Shift register I/O paths in loopback mode for master mode

38.3.13 Self-Diagnosis of Parity Bit Function

The parity circuit consists of a parity bit adding unit used for transmit data and an error detecting unit used for received data. To detect defects in the parity bit adding unit and error detecting unit of the parity circuit, self-diagnosis is executed for the parity circuit following the flow shown in Figure 38.50.

Table 38.12 SPLP2和SPLP位设置和接收数据

SPPCR.SPLP2 bit	SPPCR.SPLP bit	接收数据
0	0	从MOSIn引脚或MIOn引脚输入数据
0	1	反相传输数据
1	0	传输数据
1	1	传输数据

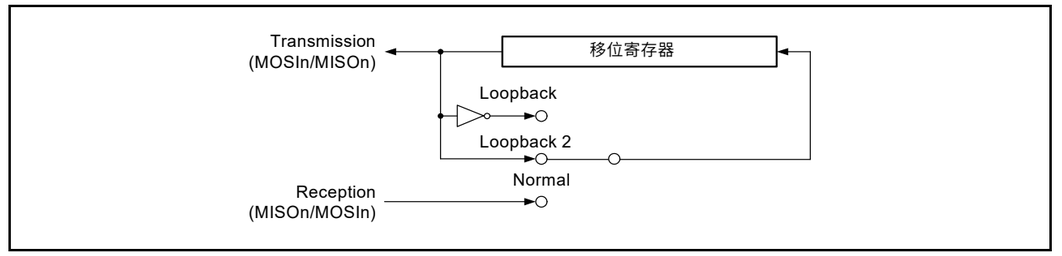


Figure 38.49 在主模式的环回模式下配置移位寄存器IO路径

38.3.13 奇偶校验位功能自诊断

奇偶校验电路由用于发送数据的奇偶校验位添加单元和用于接收数据的错误检测单元组成。为了检测奇偶校验电路的奇偶校验位添加单元和错误检测单元的缺陷，按照图38.50所示的流程对奇偶校验电路执行自诊断。

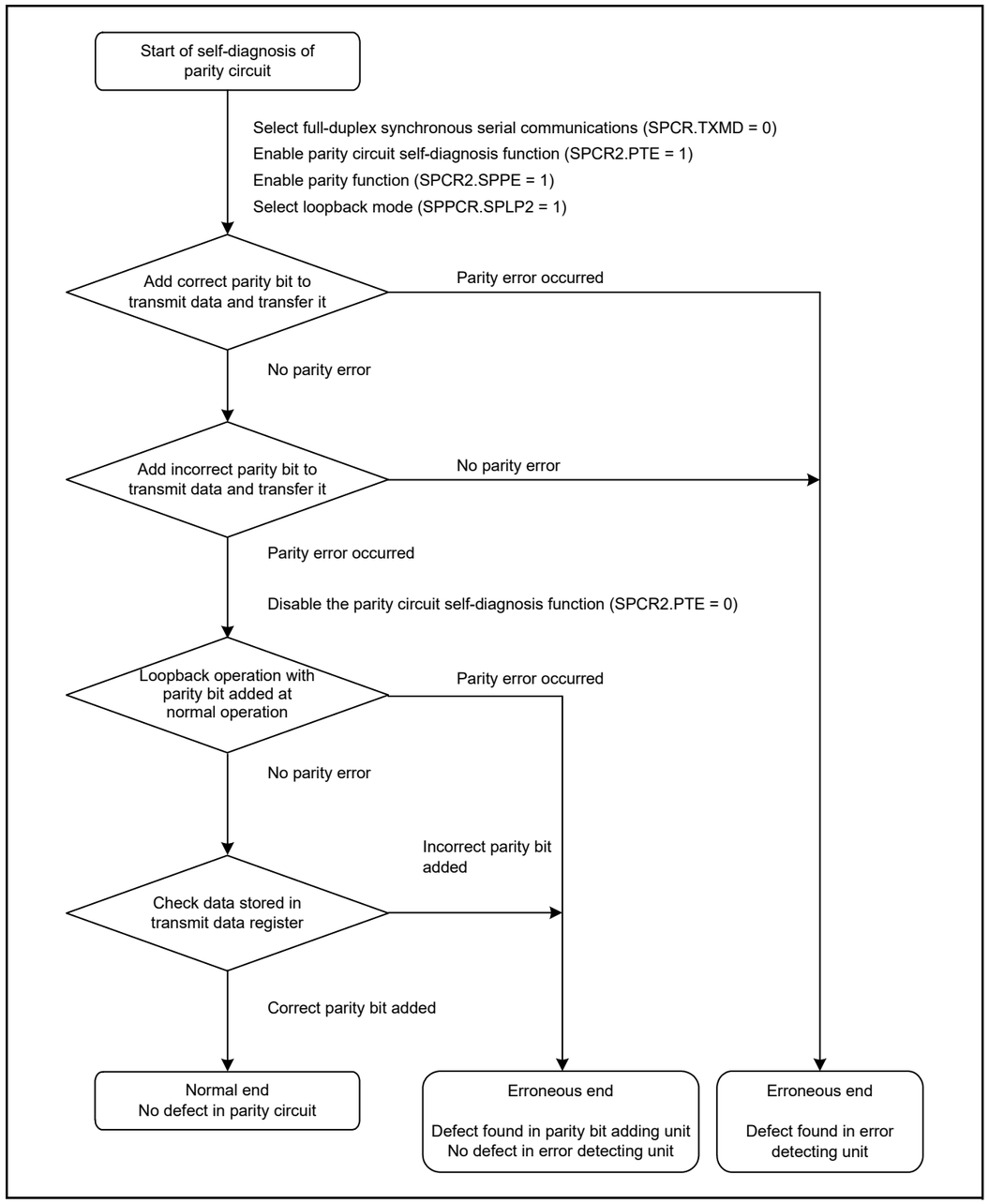


Figure 38.50 Self-diagnosis flow for parity circuit

38.3.14 Interrupt Sources

The SPI interrupt sources include:

- Receive buffer full
- Transmit buffer empty

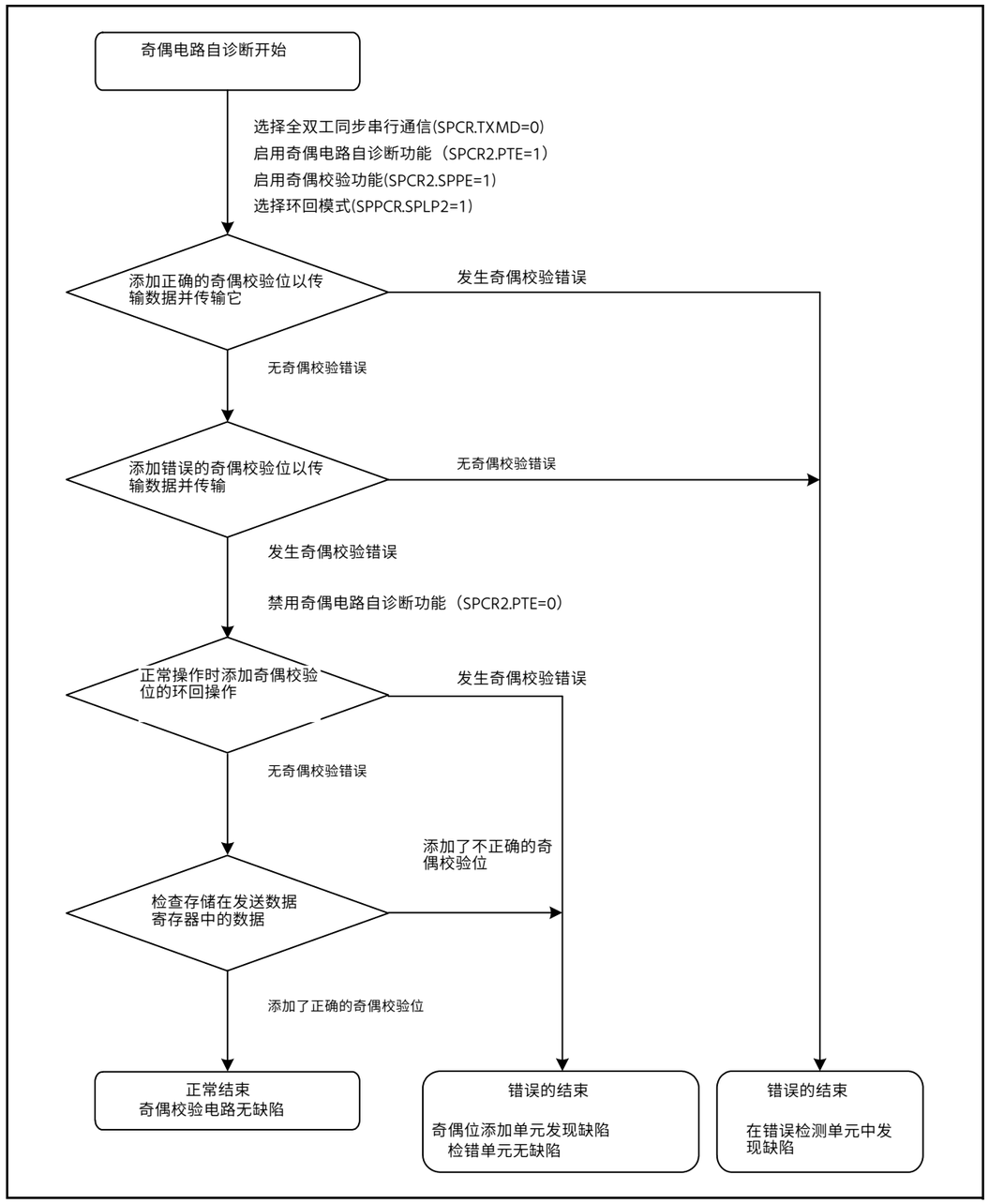


Figure 38.50 奇偶校验电路的自诊断流程

38.3.14 中断源

SPI中断源包括：

- 接收缓冲区已满
- 发送缓冲区为空

- SPI error (mode fault, underrun, overrun, or parity error)
- SPI idle
- Transmission-complete

The DTC or DMAC can be activated by the receive buffer full or transmit buffer empty interrupt to perform data transfer.

Because the vector address for the SPIi_SPEI (SPI error interrupt) is allocated to interrupt requests on mode fault, underrun, overrun, and parity errors, the actual interrupt source must be determined from the flags. Interrupt sources for the SPI are listed in Table 38.13. An interrupt is generated on satisfaction of one of the interrupt conditions in Table 38.13. Clear the receive buffer full and transmit buffer empty sources through a data transfer.

When using the DTC or DMAC to perform data transmission and reception, the DTC or DMAC must be set up first to a transfer-enabled status before making the SPI settings. For information on setting up the DTC or DMAC, see section 17, DMA Controller (DMAC), or section 18, Data Transfer Controller (DTC).

If the conditions for generating a transmit buffer empty or receive buffer full interrupt occur while the ICU.IELSRn.IR flag is 1, the interrupt is not output as a request for the ICU but is retained internally (the capacity for retention is one request per source). A retained interrupt request is output when the ICU.IELSRn.IR flag clears to 0. A retained interrupt request is automatically discarded when it is output as an actual interrupt request. The interrupt enable bit (the SPCR.SPTIE or SPCR.SPRIE bit) for an internally retained interrupt request can also be cleared to 0.

Table 38.13 SPI interrupt sources

Interrupt source	Symbol	Interrupt condition	DMAC or DTC activation
Receive buffer full	SPIi_SPRI	Receive buffer becomes full (SPSR.SPRF flag is 1) while the SPCR.SPRIE bit is 1	Possible
Transmit buffer empty	SPIi_SPTI	Transmit buffer becomes empty (SPSR.SPTEF flag is 1) while the SPCR.SPTIE bit is 1	Possible
SPI error (mode fault, underrun, overrun, or parity error)	SPIi_SPEI	SPSR.MODF, OVRF, PERF, or UDRF flag sets to 1 while the SPCR.SPEIE bit is 1	Impossible
SPI idle	SPIi_SPII	SPSR.IDLNF flag clears to 0 while the SPCR2.SPIIE bit is 1	Impossible
Transmission-complete	SPIi_SPTEND	• Master mode: Interrupt is generated when the IDLNF flag (SPI idle flag) changes from 1 to 0 • Slave mode: interrupt occurs on conditions shown in Table 38.15	Impossible

38.4 Output to the Event Link Controller (ELC)

The ELC can produce the following event output signals:

- Receive buffer full event output
- Transmit buffer empty event output
- Mode-fault, underrun, overrun, or parity error event output
- SPI idle event output
- Transmission-completed event output.

The event link output signal is output regardless of the interrupt enable bit setting.

38.4.1 Receive Buffer Full Event Output

This event signal is output when received data is transferred from the shift register to the SPDR/SPDR_HA on completion of serial transfer.

38.4.2 Transmit Buffer Empty Event Output

This event signal is output when data for transmission is transferred from the transmit buffer to the shift register and when the value of the SPE bit changes from 0 to 1.

- SPI错误（模式故障、欠载、溢出或奇偶校验错误）
- SPI空闲
- Transmission-complete

DTC或DMAC可以由接收缓冲区满或发送缓冲区空中断激活以执行数据传输。

因为SPIi_SPEI（SPI错误中断）的向量地址分配给模式错误、欠载、溢出和奇偶校验错误的中断请求，所以必须根据标志确定实际中断源。SPI的中断源在表38.13中列出。满足表38.13中的中断条件之一时会产生中断。通过数据传输清除接收缓冲区满和发送缓冲区空源。

使用DTC或DMAC进行数据传输和接收时，必须先将DTC或DMAC设置为传输使能状态，然后再进行SPI设置。有关设置DTC或DMAC的信息，请参阅第17节，DMA控制器(DMAC)或第18节，数据传输控制器(DTC)。

如果在ICU.IELSRn.IR标志为1时发生发送缓冲区空或接收缓冲区满中断的条件，则该中断不会作为对ICU的请求输出，而是在内部保留（保留容量为每个请求一个请求）资源）。当ICU.IELSRn.IR标志清除为0时，输出保留中断请求。当作为实际中断请求输出时，自动丢弃保留中断请求。内部保留中断请求的中断使能位（SPCR.SPTIE或SPCR.SPRIE位）也可以清零。

Table 38.13 SPI中断源

中断源	Symbol	中断条件	DMAC或DTC激活
接收缓冲区已满	SPIi_SPRI	当SPCR.SPRIE位为1时，接收缓冲区变满（SPSR.SPRF标志为1）	Possible
发送缓冲区为空	SPIi_SPTI	当SPCR.SPTIE位为1时，发送缓冲区变为空（SPSR.SPTEF标志为1）	Possible
SPI错误（模式故障、欠载、溢出或奇偶校验错误）	SPIi_SPEI	SPSR.MODF、OVRF、PERF或UDRF标志设置为1，而SPCR.SPEIE位为1	Impossible
SPI空闲	SPIi_SPII	SPSR.IDLNF标志在SPCR2.SPIIE位为1时清除为0	Impossible
Transmission-complete	SPIi_SPTEND	主模式：当IDLNF标志（SPI空闲标志）从1变为0时产生中断 从模式：在所示条件下发生中断 Table 38.15	Impossible

38.4 输出到事件链接控制器(ELC)

ELC可以产生以下事件输出信号：

- 接收缓冲区满事件输出
- 发送缓冲区空事件输出
- 模式故障、欠载、溢出或奇偶校验错误事件输出
- SPI空闲事件输出
- 传输完成事件输出。

无论中断允许位设置如何，都会输出事件链接输出信号。

38.4.1 接收缓冲区满事件输出

串行传输完成后，当接收到的数据从移位寄存器传输到SPDRSPDR_HA时，输出此事件信号。

38.4.2 发送缓冲区空事件输出

当要发送的数据从发送缓冲器传送到移位寄存器时，以及SPE位的值从0变为1时，输出该事件信号。

38.4.3 Mode-Fault, Underrun, Overrun, or Parity Error Event Output

This event signal is output when mode fault, underrun, overrun, or parity error is detected. See section 38.5.4, Constraints on Mode-Fault, Underrun, Overrun, or Parity Error Event Output if using this event signal.

(1) Mode-fault

Table 38.14 lists the conditions for occurrence of a mode-fault event.

Table 38.14 Conditions for mode fault occurrence

SPI mode	SPCR.MODFEN bit	SSLn0 pin	Remarks
SPI operation (SPMS = 0) Slave (SPCR.MSTR bit = 0)	1	Not active	Event is output only when the pin is deactivated during transmission

(2) Underrun

This event signal is output in response to an underrun when a serial transfer starts while the transmission data is not ready, and the value of the SPCR.MSTR bit is 0 and the SPCR.SPE bit is 1. Under these conditions, the MODF and UDRF flags set to 1.

(3) Overrun

This event signal is output in response to an overrun when a serial transfer completes while the receive buffer contains unread data and the value of the SPCR.TXMD bit is 0. Under these conditions, the OVRF flag sets to 1.

(4) Parity error

This event signal is output in response to a parity error detected on completion of a serial transfer while the value of the TXMD bit in SPCR is 0 and the value of the SPPE bit in SPCR2 is 1.

38.4.4 SPI Idle Event Output

(1) In master mode

In master mode, an event is output when the condition for setting the IDLNF flag (SPI idle flag) to 0 is satisfied.

(2) In slave mode

In slave mode, an event is output when the SPCR.SPE bit is set to 0 (SPI is initialized).

38.4.5 Transmission-Completed Event Output

During both SPI operation and clock synchronous operation in master mode, an event is output when the IDLNF flag (SPI idle flag) changes from 1 to 0. Table 38.15 lists the conditions for occurrence of a transmission-completed event.

Table 38.15 Conditions for generation of transmission-complete event in slave mode

SPI mode	Transmit buffer state	Shift register state	Other
SPI operation (SPMS = 0)	Empty	Empty	Negation of SSLn0 input
Clock synchronous operation (SPMS = 1)	Empty	Empty	Edge detection of the last RSPCKn

Whether the operation is in master mode or slave mode, an event is not output if 0 is written to the SPCR.SPE bit in transmission or the SPCR.SPE bit is cleared by the mode-fault error or the underrun error.

38.5 Usage Notes

38.5.1 Settings for the Module-Stop Function

The Module Stop Control Register B (MSTPCRB) can enable or disable SPI operation. The SPI is initially stopped after reset. Releasing the module-stop state enables access to the registers. For details, see section 11, Low Power Modes.

38.4.3 模式故障、欠载、溢出或奇偶校验错误事件输出

当检测到模式故障、欠载、溢出或奇偶校验错误时，输出该事件信号。见第38.5.4节，如果使用此事件信号，则对模式故障、欠载、溢出或奇偶校验错误事件输出的约束。

(1) Mode-fault

表38.14列出了模式故障事件发生的条件。

Table 38.14 模式故障发生的条件

SPI模式	SPCR.MODFEN bit	SSLn0 pin	Remarks
SPI操作(SPMS=0) 从机（SPCR.MSTR位=0）	1	不活跃	仅当在传输过程中禁用该引脚时才输出事件

(2) Underrun

当串行传输开始而传输数据未准备好，并且SPCR.MSTR位的值为0和SPCR.SPE位为1时，输出该事件信号以响应欠载。在这些条件下，MODF和UDRF标志设置为1。

(3) Overrun

当串行传输完成而接收缓冲区包含未读数据且SPCR.TXMD位的值为0时，输出此事件信号以响应溢出。在这些情况下，OVRF标志设置为1。

(4) 奇偶校验错误

该事件信号是响应在串行传输完成时检测到的奇偶校验错误而输出的，而SPCR中的TXMD位为0，SPCR2中的SPPE位的值为1。

38.4.4 SPI空闲事件输出

(1) 在主模式

在主机模式下，当将IDLNF标志（SPI空闲标志）设置为0的条件成立时输出事件。

(2) 在从模式

在从机模式下，当SPCR.SPE位设置为0（SPI初始化）时，会输出一个事件。

38.4.5 传输完成事件输出

在主机模式下的SPI操作和时钟同步操作期间，当IDLNF标志（SPI空闲标志）从1变为0时输出事件。表38.15列出了发生传输完成事件的条件。

Table 38.15 从机模式下产生传输完成事件的条件

SPI模式	发送缓冲区状态	移位寄存器状态	Other
SPI操作(SPMS=0)	Empty	Empty	SSLn0输入的否定
时钟同步操作(SPMS=1)	Empty	Empty	最后一个RSPCKn的边缘检测

无论操作是主模式还是从模式，如果在传输过程中向SPCR.SPE位写入0或SPCR.SPE位因模式故障错误或欠载错误而清零，则不输出事件。

38.5 使用说明

38.5.1 模块停止功能的设置

模块停止控制寄存器B(MSTPCRB)可以启用或禁用SPI操作。SPI在复位后最初停止。释放模块停止状态可以访问寄存器。有关详细信息，请参阅第11节，低功耗模式。

38.5.2 Constraint on Low Power Functions

When using the module-stop function and entering a low power mode other than Sleep, set the SPCR.SPE bit to 0 before completing communication.

38.5.3 Constraints on Starting Transfer

If the ICU.IELSRn.IR flag is 1 when transfer starts, the interrupt request is internally saved, which can lead to unanticipated behavior of the ICU.IELSRn.IR flag.

To prevent this, use the following procedure to clear interrupt requests before enabling operations (by setting the SPCR.SPE bit to 1):

1. Confirm that transfer stopped (the SPCR.SPE bit is 0).
2. Set the associated interrupt enable bit (SPCR.SPTIE or SPCR.SPRIE) to 0.
3. Read the associated interrupt enable bit (SPCR.SPTIE or SPCR.SPRIE) and confirm that its value is 0.
4. Set the ICU.IELSRn.IR flag to 0.

38.5.4 Constraints on Mode-Fault, Underrun, Overrun, or Parity Error Event Output

Using the mode-fault, underrun, overrun or parity error event is prohibited if the SPI is in multi-master mode (when the SPCR.SPMS bit is 0, the SPCR.MSTR bit is 1, and the SPCR.MODFEN bit is 1).

38.5.5 Constraints on the SPRF and SPTEF Flags

If the polling flags, SPRF and SPTEF, are used, interrupt usage is prohibited, and you must set the SPCR.SPRIE and SPCR.SPTIE bits to 0. Either the interrupts or the flags can be used, but not both.

38.5.2 对低功耗函数的约束

当使用模块停止功能并进入除睡眠以外的低功耗模式时，在完成通信之前将SPCR.SPE位设置为0。

38.5.3 开始传输的限制

如果ICU.IELSRn.IR标志在传输开始时为1，则内部保存中断请求，这可能导致ICU.IELSRn.IR标志的意外行为。

为防止这种情况发生，请使用以下过程在启用操作之前清除中断请求（通过设置SPCR.SPE位为1）：

1. 确认传输停止（SPCR.SPE位为0）。
2. 将相关的中断使能位（SPCR.SPTIE或SPCR.SPRIE）设置为0。
3. 读取相关的中断使能位（SPCR.SPTIE或SPCR.SPRIE）并确认其值为0。
4. 将ICU.IELSRn.IR标志设置为0。

38.5.4 模式故障、欠载、溢出或奇偶校验错误事件输出的约束

如果SPI处于多主模式（当SPCR.SPMS位为0，SPCR.MSTR位为1，SPCR.MODFEN位为1）。

38.5.5 SPRF和SPTEF标志的约束

如果使用轮询标志SPRF和SPTEF，则禁止使用中断，您必须设置SPCR.SPRIE和SPCR.SPTIE位为0。可以使用中断或标志，但不能同时使用。

39. Quad Serial Peripheral Interface (QSPI)

39.1 Overview

The Quad Serial Peripheral Interface (QSPI) module is a memory controller for connecting serial ROM that has an SPI-compatible interface. This includes nonvolatile memory, such as a serial flash memory, serial EEPROM, or serial FeRAM. Table 39.1 lists the QSPI specifications, Figure 39.1 shows a block diagram, and Table 39.2 lists the I/O pins.

Table 39.1 QSPI specifications

Parameter	Specifications
Number of channels	1 channel
SPI	• Support for Extended SPI, Dual SPI, and Quad SPI protocols • Configurable to SPI mode 0 and SPI mode 3 • Address width selectable to 8, 16, 24, or 32 bits.
Timing adjustment function	Configurable to support a wide range of serial flash
Flash read function	• Support for Read, Fast Read, Fast Read Dual Output, Fast Read Dual I/O, Fast Read Quad Output, and Fast Read Quad I/O instructions • Substitutable instruction code • Adjustable number of dummy cycles • Prefetch function • Polling processing • SPI bus cycle extension function.
Direct communication function	Flexible support for a wide variety of serial flash instructions and functions through software control, including erase, write, ID read, and power-down control
Interrupt source	Error interrupts
Module-stop function	Module-stop state can be set to reduce power consumption

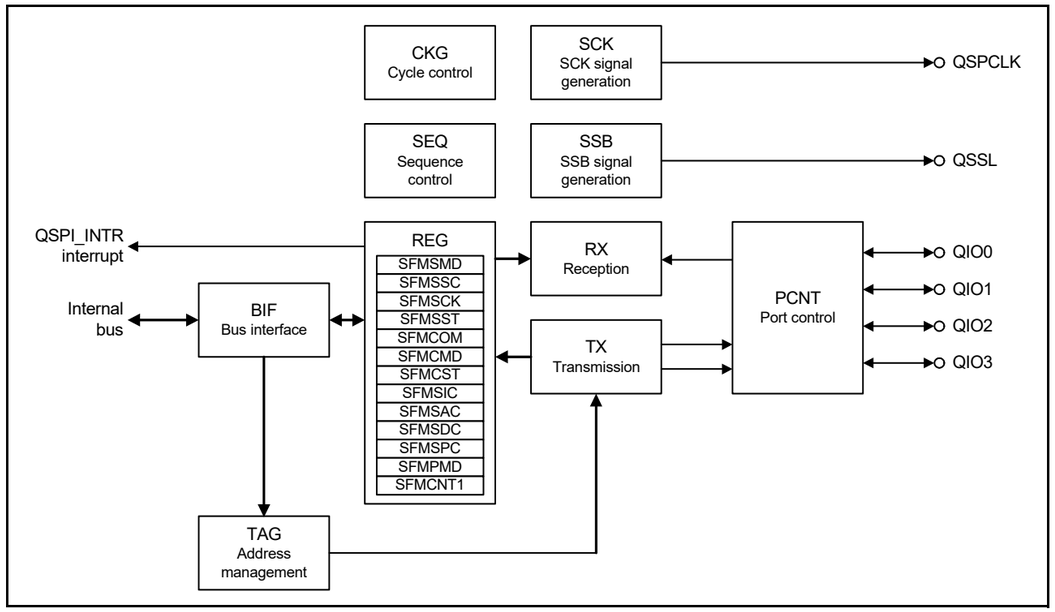


Figure 39.1 QSPI block diagram

39. 四路串行外设接口(QSPI)

39.1 Overview

QuadSerialPeripheralInterface(QSPI)模块是一种存储器控制器，用于连接具有SPI兼容接口的串行ROM。这包括非易失性存储器，例如串行闪存、串行EEPROM或串行FeRAM。表39.1列出了QSPI规范，图39.1显示了框图，表39.2列出了IO引脚。

Table 39.1 QSPI specifications

Parameter	Specifications
通道数	1 channel
SPI	支持扩展SPI、双SPI和QuadSPI协议 可配置为SPI模式0和SPI模式3 地址宽度可选择为8、16、24或32位。
定时调整功能	可配置以支持各种串行闪存
闪存读取功能	支持读取、快速读取、快速读取双输出、快速读取双IO、快速读取四输出和快速读取四IO指令可替换指令代码 可调整的虚拟周期数 预取功能 轮询处理 SPI总线周期扩展功能。
直接通讯功能	通过软件控制灵活支持各种串行闪存指令和功能，包括擦除、写入、ID读取和断电控制
中断源	错误中断
Module-stop function	可设置模块停止状态以降低功耗

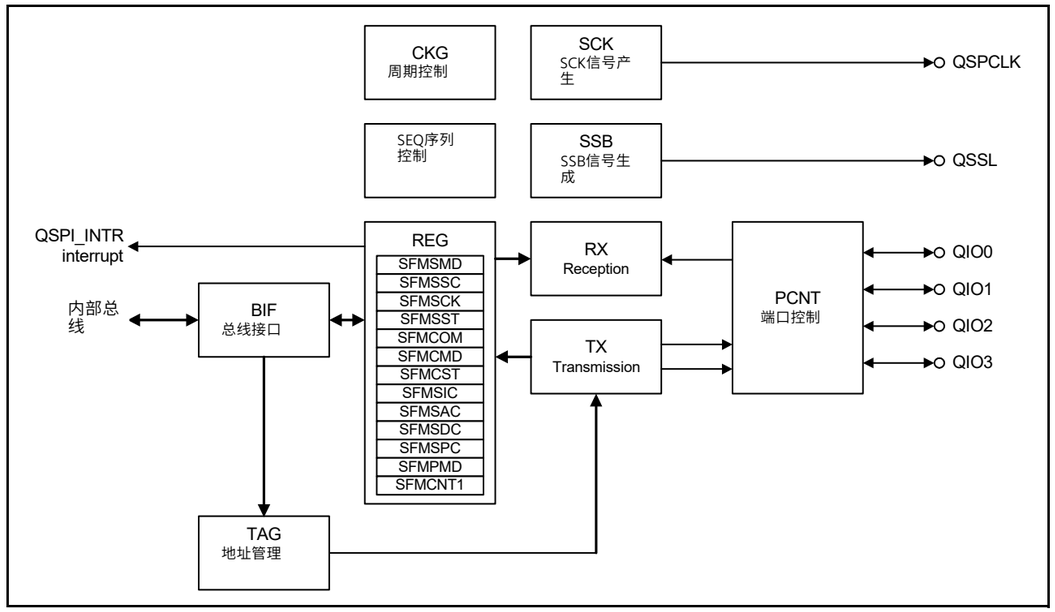


Figure 39.1 QSPI框图

Table 39.2 QSPI I/O pins

Pin name	I/O	Function
QSPCLK	Output	QSPI clock output pin
QSSL	Output	QSPI slave select pin
QIO0	I/O	Data 0 input/output
QIO1	I/O	Data 1 input/output
QIO2	I/O	Data 2 input/output
QIO3	I/O	Data 3 input/output

39.2 Register Descriptions

39.2.1 Transfer Mode Control Register (SFMSMD)

Address(es): QSPI.SFMSMD 6400 0000h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SFMCCE	—	—	—	SFMOSW	SFMOHW	SFMOEX	SFMMD3	SFMPAE	SFMPFE	SFMSE[1:0]		—	SFMRM[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Symbol	Bit name	Description	R/W
b2 to b0	SFMRM[2:0]	Serial interface read mode select	b2 b0 0 0 0: Standard Read 0 0 1: Fast Read 0 1 0: Fast Read Dual Output 0 1 1: Fast Read Dual I/O 1 0 0: Fast Read Quad Output 1 0 1: Fast Read Quad I/O 1 1 0: Setting prohibited (unpredictable operation can result) 1 1 1: Setting prohibited (unpredictable operation can result).	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b5, b4	SFMSE[1:0]	QSSL extension function select after SPI bus access	b5 b4 0 0: Do not extend QSSL 0 1: Extend QSSL by 33 QSPCLK 1 0: Extend QSSL by 129 QSPCLK 1 1: Extend QSSL infinitely.	R/W
b6	SFMPFE	Prefetch function select	0: Disable function 1: Enable function.	R/W
b7	SFMPAE	Function select for stopping prefetch at locations other than on byte boundaries	0: Disable function 1: Enable function.	R/W
b8	SFMMD3	SPI mode select	0: SPI mode 0 1: SPI mode 3.	R/W
b9	SFMOEX	Extension select for the I/O buffer output enable signal for the serial interface	0: Do not extend 1: Extend by 1 QSPCLK.	R/W

Table 39.2 QSPI I/O pins

引脚名称	I/O	Function
QSPCLK	Output	QSPI时钟输出引脚
QSSL	Output	QSPI从机选择引脚
QIO0	I/O	Data 0 input/output
QIO1	I/O	Data 1 input/output
QIO2	I/O	Data 2 input/output
QIO3	I/O	Data 3 input/output

39.2 注册说明

39.2.1 传输模式控制寄存器(SFMSMD)

Address(es): QSPI.SFMSMD 6400 0000h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SFMCCE	—	—	—	SFMOSW	SFMOHW	SFMOEX	SFMMD3	SFMPAE	SFMPFE	SFMSE[1:0]		—	SFMRM[2:0]		
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Symbol	位名称	Description	R/W
b2 to b0	SFMRM[2:0]	串行接口读取模式选择	b2b0000：标准读取001：快速读取010：快速读取双路输出011：快速读取双路IO100：快速读取四路输出101：快速读取四路IO110：设置禁止（可能导致不可预知的操作）111：设置禁止（可能导致不可预知的操作）。	R/W
b3	—	Reserved	该位读取为0。写入值应为0。	R/W
b5, b4	SFMSE[1:0]	SPI总线访问后QSSL扩展功能选择	b5b400：不扩展QSSL01：将QSSL扩展33QSPCLK10：将QSSL扩展129QSPCLK11：无限扩展QSSL。	R/W
b6	SFMPFE	预取功能选择	0：禁用功能1：启用功能。	R/W
b7	SFMPAE	用于在字节边界以外的位置停止预取的函数选择	0：禁用功能1：启用功能。	R/W
b8	SFMMD3	SPI模式选择	0：SPI模式01：SPI模式3。	R/W
b9	SFMOEX	串行接口的IO缓冲器输出使能信号的扩展选择	0：不扩展1：扩展1个QSPCLK。	R/W

Bits	Symbol	Bit name	Description	R/W
b10	SFMOHW	Hold time adjustment for serial transmission	0: Do not extend high-level width of QSPCLK during transmission 1: Extend high-level width of QSPCLK by 1 PCLKA during transmission.	R/W
b11	SFMOSW	Setup time adjustment for serial transmission	0: Do not extend low-level width of QSPCLK during transmission 1: Extend low-level width of QSPCLK by 1 PCLKA during transmission.	R/W
b14 to b12	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15	SFMCCE	Read instruction code select	0: Set default instruction code for each instruction 1: Write instruction code in the SFMSIC register.	R/W
b31 to b16	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

39.2.2 Chip Selection Control Register (SFMSSC)

Address(es): QSPI.SFMSSC 6400 0004h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	SFMSLD	SFMSHD	SFMSW			
Value after reset:	0	0	0	0	0	0	0	0	0	0	1	1	0	1	1	1

Bits	Symbol	Bit name	Description	R/W
b3 to b0	SFMSW	Minimum high-level width select for QSSL signal	b3 b0 0 0 0 0: 1 QSPCLK 0 0 0 1: 2 QSPCLK 0 0 1 0: 3 QSPCLK 0 0 1 1: 4 QSPCLK 0 1 0 0: 5 QSPCLK 0 1 0 1: 6 QSPCLK 0 1 1 0: 7 QSPCLK 0 1 1 1: 8 QSPCLK 1 0 0 0: 9 QSPCLK 1 0 0 1: 10 QSPCLK 1 0 1 0: 11 QSPCLK 1 0 1 1: 12 QSPCLK 1 1 0 0: 13 QSPCLK 1 1 0 1: 14 QSPCLK 1 1 1 0: 15 QSPCLK 1 1 1 1: 16 QSPCLK.	R/W
b4	SFMSHD	QSSL signal release timing select	0: Release QSSL 0.5 QSPCLK cycles after the last rising edge of QSPCLK 1: Release QSSL 1.5 QSPCLK cycles after the last rising edge of QSPCLK.	R/W
b5	SFMSLD	QSSL signal output timing select	0: Output QSSL 0.5 QSPCLK cycles before the first rising edge of QSPCLK 1: Output QSSL 1.5 QSPCLK cycles before the first rising edge of QSPCLK.	R/W
b31 to b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Bits	Symbol	位名称	Description	R/W
b10	SFMOHW	串行传输的保持时间调整	0：在传输过程中不扩展QSPCLK的高电平宽度1：在传输过程中将QSPCLK的高电平宽度扩展1PCLKA。	R/W
b11	SFMOSW	串行传输的建立时间调整	0：在传输过程中不扩展QSPCLK的低电平宽度1：在传输过程中将QSPCLK的低电平宽度扩展1PCLKA。	R/W
b14 to b12	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b15	SFMCCE	读取指令代码选择	0：为每条指令设置默认指令代码1：将指令代码写入SFMSIC寄存器。	R/W
b31 to b16	—	Reserved	这些位被读取为0。写入值应为0。	R/W

39.2.2 片选控制寄存器(SFMSSC)

Address(es): QSPI.SFMSSC 6400 0004h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	SFMSLD	SFMSHD	SFMSW			
重置后的值：	0	0	0	0	0	0	0	0	0	0	1	1	0	1	1	1

Bits	Symbol	位名称	Description	R/W
b3 to b0	SFMSW	QSSL信号的最小高电平宽度选择	b3 b0 0 0 0 0: 1 QSPCLK 0 0 0 1: 2 QSPCLK 0 0 1 0: 3 QSPCLK 0 0 1 1: 4 QSPCLK 0 1 0 0: 5 QSPCLK 0 1 0 1: 6 QSPCLK 0 1 1 0: 7 QSPCLK 0 1 1 1: 8 QSPCLK 1 0 0 0: 9 QSPCLK 1 0 0 1: 10 QSPCLK 1 0 1 0: 11 QSPCLK 1 0 1 1: 12 QSPCLK 1 1 0 0: 13 QSPCLK 1 1 0 1: 14 QSPCLK 1 1 1 0: 15 QSPCLK 1 1 1 1: 16 QSPCLK.	R/W
b4	SFMSHD	QSSL信号释放时序选择	0：在QSPCLK的最后一个上升沿之后释放QSSL0.5个QSPCLK周期1：在QSPCLK的最后一个上升沿之后释放QSSL1.5个QSPCLK周期。	R/W
b5	SFMSLD	QSSL信号输出时序选择	0：在QSPCLK的第一个上升沿之前输出QSSL0.5个QSPCLK周期1：在QSPCLK的第一个上升沿之前输出QSSL1.5个QSPCLK周期。	R/W
b31 to b6	—	Reserved	这些位被读取为0。写入值应为0。	R/W

39.2.3 Clock Control Register (SFMSKC)

Address(es): QSPI.SFMSKC 6400 0008h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	SFMDTY	SFMDV				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Bits	Symbol	Bit name	Description	R/W
b4 to b0	SFMDV	Serial interface reference cycle select. (Pay attention to irregularities.)	b4 b3 b2 b1 b0 0 0 0 0 0: 2 PCLKA 0 0 0 0 1: 3 PCLKA (multiplied by an odd number)*1 0 0 0 1 0: 4 PCLKA 0 0 0 1 1: 5 PCLKA (multiplied by an odd number)*1 0 0 1 0 0: 6 PCLKA 0 0 1 0 1: 7 PCLKA (multiplied by an odd number)*1 0 0 1 1 0: 8 PCLKA 0 0 1 1 1: 9 PCLKA (multiplied by an odd number)*1 0 1 0 0 0: 10 PCLKA 0 1 0 0 1: 11 PCLKA (multiplied by an odd number)*1 0 1 0 1 0: 12 PCLKA 0 1 0 1 1: 13 PCLKA (multiplied by an odd number)*1 0 1 1 0 0: 14 PCLKA 0 1 1 0 1: 15 PCLKA (multiplied by an odd number)*1 0 1 1 1 0: 16 PCLKA 0 1 1 1 1: 17 PCLKA (multiplied by an odd number)*1 1 0 0 0 0: 18 PCLKA 1 0 0 0 1: 20 PCLKA 1 0 0 1 0: 22 PCLKA 1 0 0 1 1: 24 PCLKA 1 0 1 0 0: 26 PCLKA 1 0 1 0 1: 28 PCLKA 1 0 1 1 0: 30 PCLKA 1 0 1 1 1: 32 PCLKA 1 1 0 0 0: 34 PCLKA 1 1 0 0 1: 36 PCLKA 1 1 0 1 0: 38 PCLKA 1 1 0 1 1: 40 PCLKA 1 1 1 0 0: 42 PCLKA 1 1 1 0 1: 44 PCLKA 1 1 1 1 0: 46 PCLKA 1 1 1 1 1: 48 PCLKA.	R/W
b5	SFMDTY	Duty ratio correction function select for the QSPCLK signal	0: Make no correction 1: Delay the rising of the QSPCLK signal by 0.5 PCLKA cycles. (Valid when PCLKA is multiplied by an odd number.)	R/W
b31 to b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. When PCLKA multiplied by an odd number is selected, the high-level width of the QSPCLK signal is longer than the low-level width by 1 PCLKA before duty ratio correction.

39.2.3 时钟控制寄存器(SFMSKC)

Address(es): QSPI.SFMSKC 6400 0008h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	SFMDTY	SFMDV				
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0

Bits	Symbol	位名称	Description	R/W
b4 to b0	SFMDV	串行接口参考周期选择。（注意违规行为。）	b4b000000：2PCLKA00001：3PCLKA（乘以奇数）*100010：4PCLKA00011：5PCLKA（乘以奇数）*100100：6PCLKA00101：7PCLKA（乘以奇数）*100110：8PCLKA00111：9PCLKA（乘以奇数）*101000：10PCLKA01001：11PCLKA（乘以奇数）*101010：12PCLKA01011：13PCLKA（乘以奇数）*101100：14PCLKA01101：15PCLKA（乘以奇数）*101110：16PCLKA01111：17PCLKA（乘以奇数）*110000：18PCLKA10001：20PCLKA10010：22PCLKA10011：24PCLKA10100：26PCLKA10101：28PCLKA10110：30PCLKA10111：32PCLKA11000：34PCLKA11001：36PCLKA11010：38PCLKA11011：40PCLKA11100：42PCLKA11101：44PCLKA11110：46个PCLKA11111：48个PCLKA。	R/W
b5	SFMDTY	QSPCLK信号的占空比校正功能选择	0：不进行修正1：将QSPCLK信号的上升沿延迟0.5个PCLKA周期。（当PCLKA乘以奇数时有效。）	R/W
b31 to b6	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. WhenPCLKAmultipliedbyanoddnumberisselected thehigh-levelwidthoftheQSPCLKsignalislongerthanthelow-levelwidthby1PCLKAbeforedutyratiocorrection.

39.2.4 Status Register (SFMSST)

Address(es): QSPI.SFMSST 6400 000Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	PFOFF	PFFUL	—	PFCNT				
Value after reset:	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bits	Symbol	Bit name	Description	R/W
b4 to b0	PFCNT	Number of bytes of prefetched data	b4 b0 0 0 0 0 0: 0 bytes 0 0 0 0 1: 1 byte 0 0 0 1 0: 2 bytes 0 0 0 1 1: 3 bytes 0 0 1 0 0: 4 bytes 0 0 1 0 1: 5 bytes 0 0 1 1 0: 6 bytes 0 0 1 1 1: 7 bytes 0 1 0 0 0: 8 bytes 0 1 0 0 1: 9 bytes 0 1 0 1 0: 10 bytes 0 1 0 1 1: 11 bytes 0 1 1 0 0: 12 bytes 0 1 1 0 1: 13 bytes 0 1 1 1 0: 14 bytes 0 1 1 1 1: 15 bytes 1 0 0 0 0: 16 bytes 1 0 0 0 1: 17 bytes 1 0 0 1 0: 18 bytes. Other settings are reserved.	R
b5	—	Reserved	This bit is read as 0.	R
b6	PFFUL	Prefetch buffer state	0: Prefetch buffer has free space 1: Prefetch buffer is full.	R
b7	PFOFF	Prefetch function operating state	0: Prefetch function operating 1: Prefetch function not enabled or not operating.	R
b31 to b8	—	Reserved	These bits are read as 0.	R

39.2.4 状态寄存器(SFMSST)

Address(es): QSPI.SFMSST 6400 000Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	PFOFF	PFFUL	—	PFCNT				
重置后的值:	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0

Bits	Symbol	位名称	Description	R/W
b4 to b0	PFCNT	预取数据的字节数	b4b000000：0字节00001：1字节00010：2字节00011：3字节00100：4字节00101：5字节00110：6字节00111：7字节01000：8字节01001：9字节01010：10字节01011：11字节01100：12字节01101：13字节01110：14字节01111：15字节10000：16字节10001：17字节10010：18字节。保留其他设置。	R
b5	—	Reserved	该位读为0。	R
b6	PFFUL	预取缓冲区状态	0：预取缓冲区有空闲空间1：预取缓冲区已满。	R
b7	PFOFF	预取功能运行状态	0：预取功能运行1：预取功能未使能或未运行。	R
b31 to b8	—	Reserved	这些位读为0。	R

39.2.5 Communication Port Register (SFMCOM)

Address(es): QSPI.SFMCOM 6400 0010h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	SFMD							
Value after reset:	0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x

x: Undefined

Bits	Symbol	Bit name	Description	R/W
b7 to b0	SFMD	Port select for direct communication with the SPI bus	Input to and output from this port is converted to an SPI bus cycle. This port is only accessible in direct communication mode, when DCOM = 1. Access to this port is ignored in the ROM access mode.	R/W
b 31 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

39.2.6 Communication Mode Control Register (SFMCMD)

Address(es): QSPI.SFMCMD 6400 0014h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DCOM
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Symbol	Bit name	Description	R/W
b0	DCOM	Mode select for communication with the SPI bus	0: ROM access mode 1: Direct communication mode.	R/W
b 31 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

39.2.5 通讯端口寄存器(SFMCOM)

Address(es): QSPI.SFMCOM 6400 0010h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	SFMD							
重置后的值：	0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x

x: Undefined

Bits	Symbol	位名称	Description	R/W
b7 to b0	SFMD	用于与SPI总线直接通信的端口选择	该端口的输入和输出转换为SPI总线周期。此端口仅在直接通信模式下可访问，当DCOM=1时。在ROM访问模式下忽略对该端口的访问。	R/W
b 31 to b8	—	Reserved	这些位被读取为0。写入值应为0。	R/W

39.2.6 通信模式控制寄存器(SFMCMD)

Address(es): QSPI.SFMCMD 6400 0014h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DCOM
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Symbol	位名称	Description	R/W
b0	DCOM	与SPI总线通信的模式选择	0：ROM访问方式1：直接通信方式。	R/W
b 31 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

39.2.7 Communication Status Register (SFMCST)

Address(es): QSPI.SFMCST 6400 0018h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	EROMR	—	—	—	—	—	—	COMBSY
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Symbol	Bit name	Description	R/W
b0	COMBSY	SPI bus cycle completion state in direct communication	0: No serial transfer being processed 1: Serial transfer being processed.	R
b6 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	EROMR	ROM access detection status in direct communication mode	0: ROM access not detected 1: ROM access detected.	R/(W)*1
b31 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Only 0 can be written to this bit.

39.2.8 Instruction Code Register (SFMSIC)

Address(es): QSPI.SFMSIC 6400 0020h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	SFMCIC							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Symbol	Bit name	Description	R/W
b7 to b0	SFMCIC	Serial flash instruction code to substitute		R/W
b31 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

39.2.7 通信状态寄存器(SFMCST)

Address(es): QSPI.SFMCST 6400 0018h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	EROMR	—	—	—	—	—	—	COMBSY
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Symbol	位名称	Description	R/W
b0	COMBSY	直接通信中的SPI总线周期完成状态	0：未处理串行传输1：正在处理串行传输。	R
b6 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b7	EROMR	直接通信模式下的ROM访问检测状态	0：未检测到ROM访问1：检测到ROM访问。	R/(W)*1
b31 to b8	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 该位只能写入0。

39.2.8 指令码寄存器(SFMSIC)

Address(es): QSPI.SFMSIC 6400 0020h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	SFMCIC							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Symbol	位名称	Description	R/W
b7 to b0	SFMCIC	替代的串行闪存指令代码		R/W
b31 to b8	—	Reserved	这些位被读取为0。写入值应为0。	R/W

39.2.9 Address Mode Control Register (SFMSAC)

Address(es): QSPI.SFMSAC 6400 0024h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	SFM4BC	—	—	SFMAS	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Symbol	Bit name	Description	R/W
b1, b0	SFMAS	Number of address bytes select for the serial interface	b1 b0 0 0: 1 byte 0 1: 2 bytes 1 0: 3 bytes 1 1: 4 bytes.	R/W
b3, b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	SFM4BC	Default instruction code select, when the serial interface address width is 4 bytes	0: Do not use 4-byte address read instruction code 1: Use 4-byte address read instruction code.	R/W
b31 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

39.2.9 地址模式控制寄存器(SFMSAC)

Address(es): QSPI.SFMSAC 6400 0024h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	SFM4BC	—	—	SFMAS	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits	Symbol	位名称	Description	R/W
b1, b0	SFMAS	为串行接口选择的地址字节数	b1b000：1个字节01：2个字节10：3个字节11：4个字节。	R/W
b3, b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b4	SFM4BC	默认指令码选择，当串口地址宽度为4字节时	0：不使用4字节地址读取指令码1：使用4字节地址读取指令码。	R/W
b31 to b5	—	Reserved	这些位被读取为0。写入值应为0。	R/W

39.2.10 Dummy Cycle Control Register (SFMSDC)

Address(es): QSPI.SFMSDC 6400 0028h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SFMXD								SFMXEN	SFMXST	—	—	SFMDN[3:0]			
Value after reset:	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Bits	Symbol	Bit name	Description	R/W
b3 to b0	SFMDN[3:0]	Number of dummy cycles select for Fast Read instructions	b3 b0 0 0 0 0: Default dummy cycles for each instruction: - Fast Read Quad I/O: 6 QSPCLK - Fast Read Quad Output: 8 QSPCLK - Fast Read Dual I/O: 4 QSPCLK - Fast Read Dual Output: 8 QSPCLK - Fast Read: 8 QSPCLK. 0 0 0 1: 3 QSPCLK*1 0 0 1 0: 4 QSPCLK 0 0 1 1: 5 QSPCLK 0 1 0 0: 6 QSPCLK 0 1 0 1: 7 QSPCLK 0 1 1 0: 8 QSPCLK 0 1 1 1: 9 QSPCLK 1 0 0 0: 10 QSPCLK 1 0 0 1: 11 QSPCLK 1 0 1 0: 12 QSPCLK 1 0 1 1: 13 QSPCLK 1 1 0 0: 14 QSPCLK 1 1 0 1: 15 QSPCLK 1 1 1 0: 16 QSPCLK 1 1 1 1: 17 QSPCLK.	R/W
b5, b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6	SFMXST	XIP mode status	0: Normal (non-XIP) mode 1: XIP mode.	R
b7	SFMXEN	XIP mode permission in the QSPI	0: Prohibit XIP mode 1: Permit XIP mode.	R/W
b15 to b8	SFMXD	Mode data for serial flash. (Controls XIP mode.)		R/W
b31 to b16	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. To avoid a conflict with the input/output switch of the serial flash pin connected to QIO0 pin, select more than 4 QSPCLK dummy cycles when the output enable signal is extended by setting the SFMOEX bit in the SFMSMD register to 1.

39.2.10 虚拟周期控制寄存器(SFMSDC)

Address(es): QSPI.SFMSDC 6400 0028h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SFMXD								SFMXEN	SFMXST	—	—	SFMDN[3:0]			
重置后的值:	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0

Bits	Symbol	位名称	Description	R/W
b3 to b0	SFMDN[3:0]	为快速读取指令选择的虚拟周期数	b3b00000：每条指令的默认虚拟周期：快速读取四IO：6QSPCLK快速读取四输出：8QSPCLK快速读取双IO：4QSPCLK快速读取双输出：8QSPCLK快速读取：8QSPCLK。0001:3QSPCLK*10010:4QSPCLK0011:5QSPCLK0100:6QSPCLK0101:7QSPCLK0110:8QSPCLK0111:9QSPCLK1000：10QSPCLK1001：11QSPCLK1010：12QSPCLK1011：13QSPCLK1100：14QSPCLK1101：15QSPCLK1110：16QSPCLK1111：17QSPCLK。	R/W
b5, b4	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b6	SFMXST	XIP模式状态	0：正常（非XIP）模式1：XIP模式。	R
b7	SFMXEN	XIP模式权限在QSPI	0：禁止XIP模式1：允许XIP模式。	R/W
b15 to b8	SFMXD	串行闪存的模式数据。（控制XIP模式。）		R/W
b31 to b16	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 为避免与连接到QIO0引脚的串行闪存引脚的输入输出开关冲突，通过将SFMSMD寄存器中的SFMOEX位设置为1，在输出使能信号扩展时选择4个以上的QSPCLK空周期。

39.2.11 SPI Protocol Control Register (SFMSPC)

Address(es): QSPI.SFMSPC 6400 0030h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	SFMSDE	—	—	SFMSPI	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Symbol	Bit name	Description	R/W
b1, b0	SFMSPI	SPI protocol select	b1 b0 0 0: Extended SPI protocol 0 1: Dual SPI protocol 1 0: Quad SPI protocol 1 1: Setting prohibited.	R/W
b3, b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	SFMSDE	Minimum time select for input/output switch, when Dual SPI or Quad SPI protocol is selected and in standard read mode	0: Do not allocate minimum switch time 1: Allocate minimum switch time equivalent to 1 QSPCLK.	R/W
b31 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

39.2.12 Port Control Register (SFMPMD)

Address(es): QSPI.SFMPMD 6400 0034h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	SFMWPL	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Symbol	Bit name	Description	R/W
b1, b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b2	SFMWPL	WP pin level specification	0: Low level 1: High level.	R/W
b31 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

39.2.11 SPI协议控制寄存器(SFMSPC)

Address(es): QSPI.SFMSPC 6400 0030h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	SFMSDE	—	—	SFMSPI	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bits	Symbol	位名称	Description	R/W
b1, b0	SFMSPI	SPI协议选择	b1b000：扩展SPI协议01： 双SPI协议10：四SPI协议11 ：禁止设置。	R/W
b3, b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b4	SFMSDE	选择输入输出开关的最小时间 选择双SPI或QUADSPI协议并在 标准读取模式下选择	0：不分配最小切换时间1：分配等于1个QSPCLK的最小切 换时间。	R/W
b31 to b5	—	Reserved	这些位被读取为0。写入值应为0。	R/W

39.2.12 端口控制寄存器(SFMPMD)

Address(es): QSPI.SFMPMD 6400 0034h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	SFMWPL	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Symbol	位名称	Description	R/W
b1, b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b2	SFMWPL	WP引脚电平规范	0：低电平1 ：高电平。	R/W
b31 to b3	—	Reserved	这些位被读取为0。写入值应为0。	R/W

39.2.13 External QSPI Address Register (SFMCNT1)

Address(es): QSPI.SFMCNT1 6400 0804h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	QSPI_EXT[5:0]						—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Symbol	Bit name	Description	R/W
b25 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b31 to b26	QSPI_EXT[5:0]	Bank switching address	When accessing from 6000 0000h to 63FF FFFFh, the address bus is set from QSPI_EXT[5:0] to the upper 6 bits of the internal bus address.	R/W

39.3 Memory Map

39.3.1 Internal Bus Space

The locations of the serial flash and control registers in the AHB space are determined by the address range of the configured area.

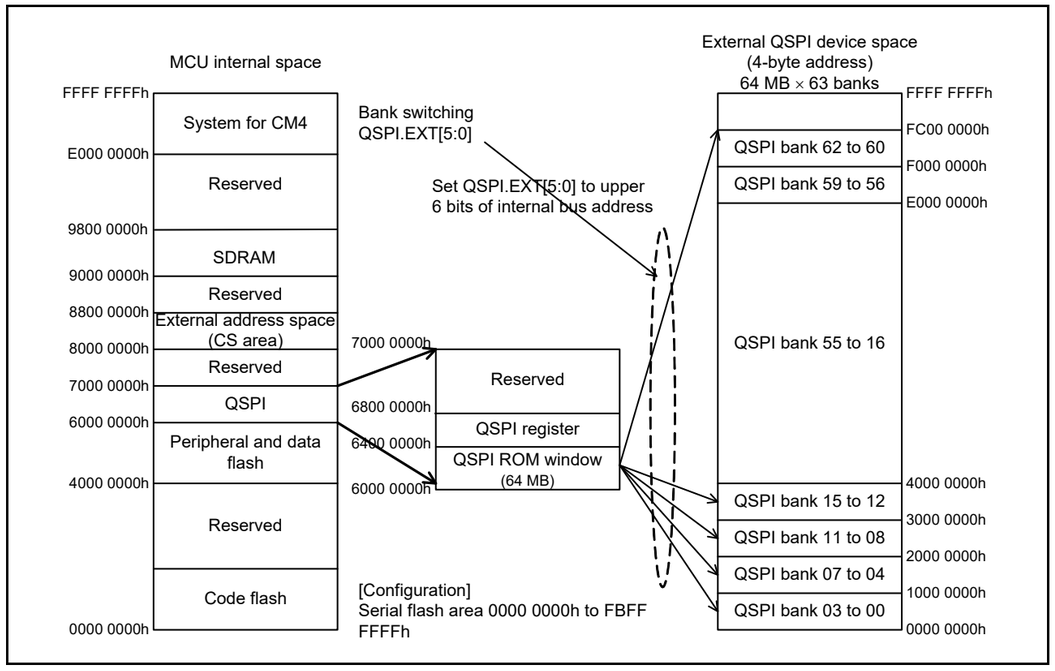


Figure 39.2 Default area setting and AHB space memory map

39.2.13 外部QSPI地址寄存器(SFMCNT1)

Address(es): QSPI.SFMCNT1 6400 0804h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	QSPI_EXT[5:0]						—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bits	Symbol	位名称	Description	R/W
b25 to b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b31 to b26	QSPI_EXT[5:0]	银行转换地址	从60000000h到63FFFFFFh访问时，地址总线设置为从QSPI_EXT[5:0]到内部总线地址的高6位。	R/W

39.3 内存映射

39.3.1 内部总线空间

AHB空间中串行闪存和控制寄存器的位置由配置区域的地址范围决定。

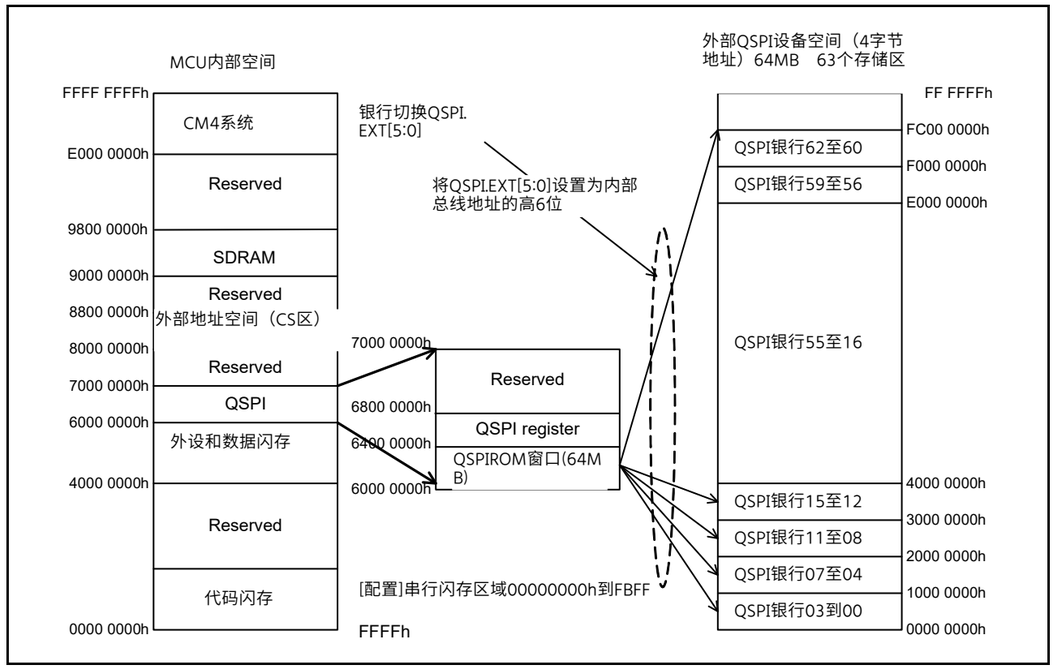


Figure 39.2 默认区域设置和AHB空间内存映射

39.3.2 Address Width of the SPI Space and SPI Bus

The SPI space has a 32-bit address width for referencing the serial flash. When the SPI space is accessed for a read, an SPI bus cycle starts automatically, and data read from the serial flash is returned.

The address width of the SPI space is fixed at 32 bits. However, the address width of the SPI bus is selectable to 8, 16, 24, or 32 bits in the SFMAS[1:0] bits in the SFMSAC register. If 8, 16, or 24 bits is selected as the address width of the SPI bus, only the lower part of the address used to access the SPI space is posted to the serial flash through the SPI bus. As a result, the mirror image of the serial flash corresponding to the address width of the SPI bus repeatedly appears in the SPI space.

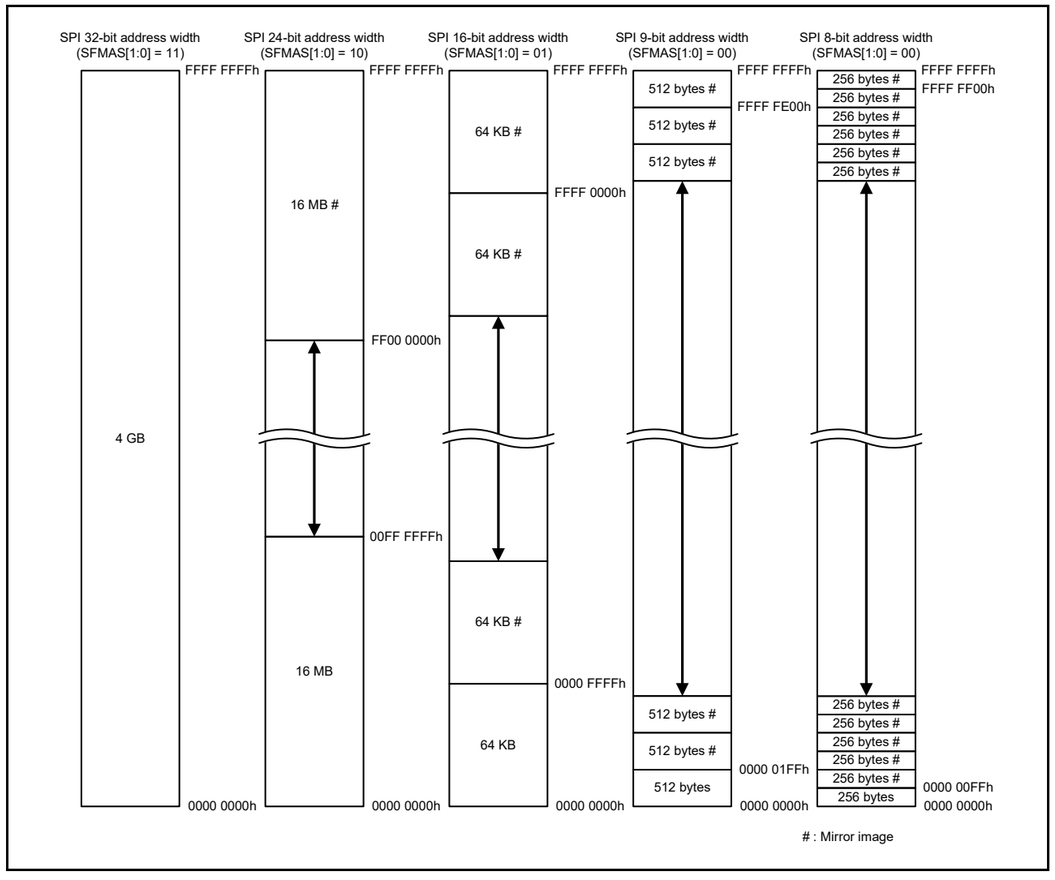


Figure 39.3 Memory map of SPI space

Note: The SPI bus address width is selectable to 8, 16, 24, or 32 bits in the SFMAS[1:0] bits in the SFMSAC register. When an 8-bit address width is selected, the address information of the ninth bit can be embedded in the Read instruction code. The address map in the figures is for the SPI 9-bit address width. For details on the Read instruction, see section 39.6.2, Standard Read Instruction.

39.4 SPI Bus

39.4.1 SPI Protocol

The QSPI supports Extended SPI, Dual SPI, and Quad SPI, in addition to the SPI protocol used for serial flash connection. The initial state is Extended SPI. To change the protocol, set the SFMSPI bit in the SFMSPC register. The Extended SPI protocol always outputs instruction codes from a single QIO0 pin. It performs subsequent address and data

39.3.2 SPI空间和SPI总线的地址宽度

SPI空间具有32位地址宽度，用于引用串行闪存。当SPI空间被访问以进行读取时，一个SPI总线周期自动启动，并返回从串行闪存读取的数据。

SPI空间的地址宽度固定为32位。但是，SPI总线的地址宽度可以在SFMSAC寄存器的SFMAS[1:0]位中选择为8、16、24或32位。如果选择8、16或24位作为SPI总线的地址宽度，则只有用于访问SPI空间的地址的低部分通过SPI总线发布到串行闪存。结果，对应于SPI总线地址宽度的串行闪存的镜像在SPI空间中反复出现。

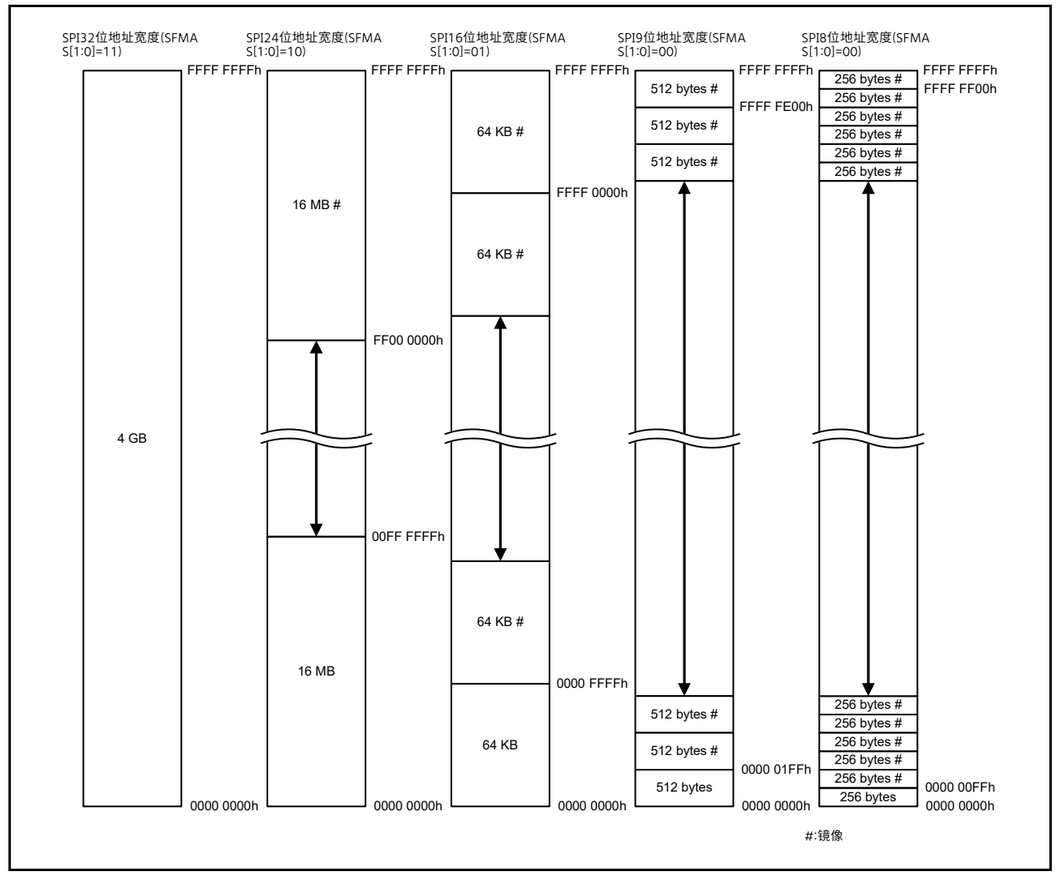


Figure 39.3 SPI空间的内存映射

Note: SPI总线地址宽度可在SFMSAC寄存器的SFMAS[1:0]位中选择为8、16、24或32位。Whenan8-bitaddresswidthis selected theaddressinformationoftheninthbitcanbeembeddedintheReadinstructioncode.图中的地址映射是针对SPI9位地址宽度的。有关读取指令的详细信息，请参阅第39.6.2节，标准读取指令。

39.4 SPI总线

39.4.1 SPI协议

除了用于串行闪存连接的SPI协议外，QSPI还支持扩展SPI、双SPI和四通道SPI。初始状态是扩展SPI。要更改协议，请设置SFMSPC寄存器中的SFMSPI位。扩展SPI协议始终从单个QIO0引脚输出指令代码。它执行后续的地址和数据

I/O operations using one to four pins, depending on the instruction code format.

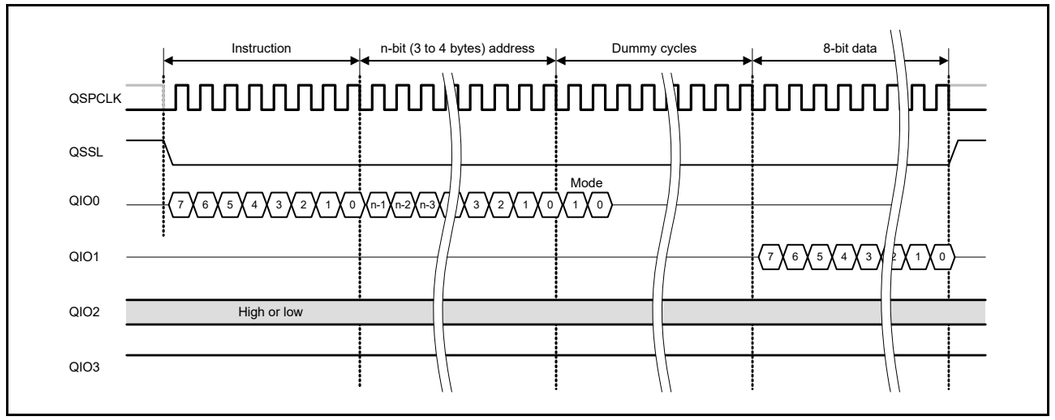


Figure 39.4 Extended SPI protocol example 1 for Fast Read

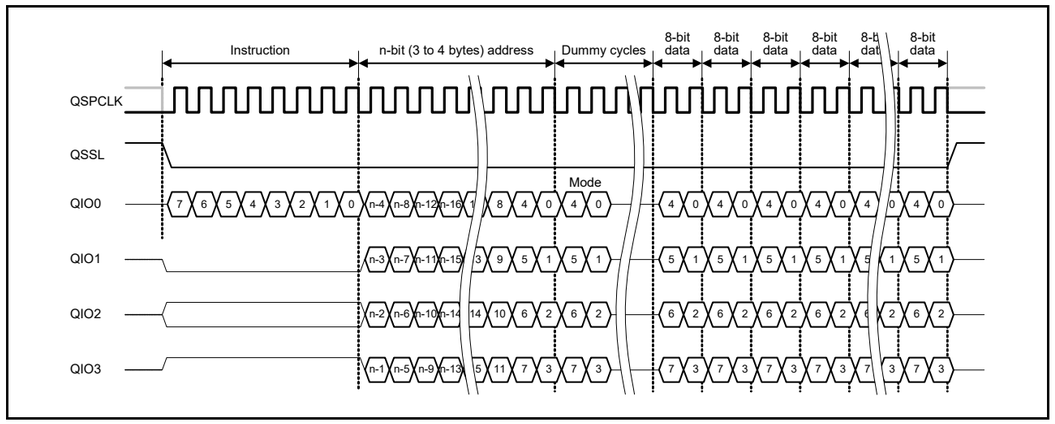


Figure 39.5 Extended SPI protocol example 2 for Fast Read Quad I/O

The Dual SPI protocol performs I/O operation of all signals such as instruction codes, addresses, and data using two pins, QIO0 and QIO1.

IO操作使用一到四个引脚，具体取决于指令代码格式。

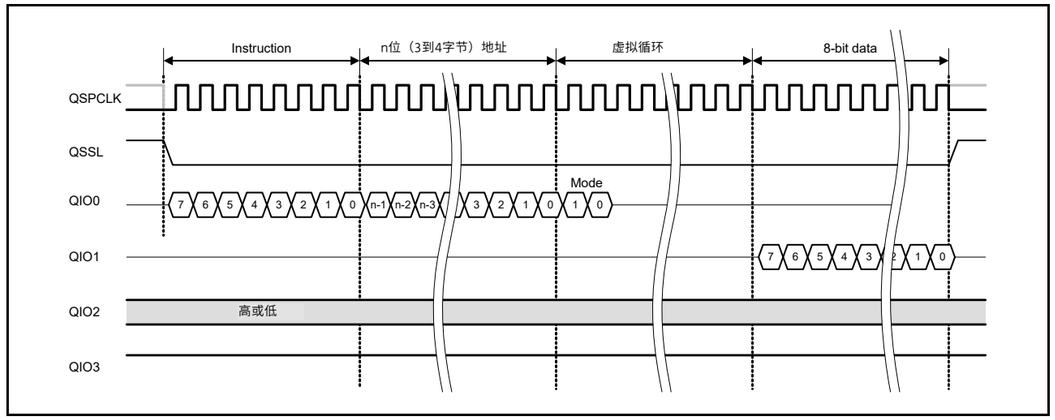


Figure 39.4 用于快速读取的扩展SPI协议示例1

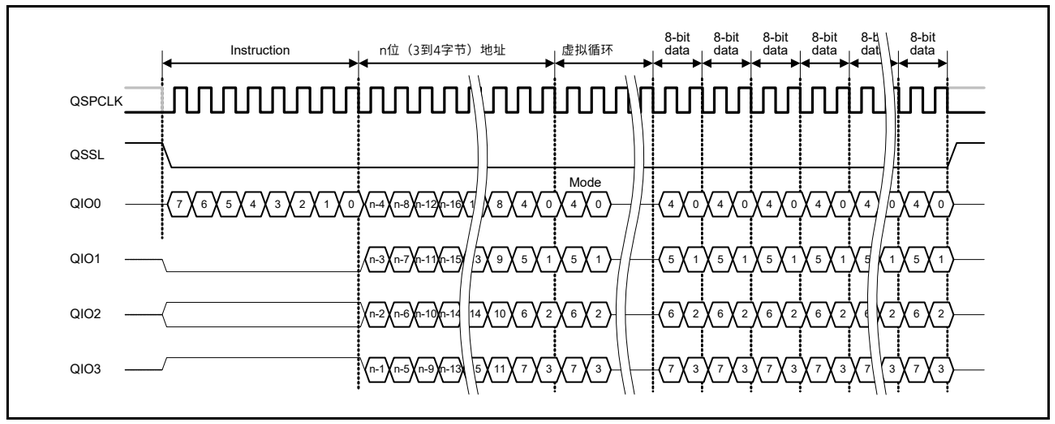


Figure 39.5 用于快速读取QuadIO的扩展SPI协议示例2

DualSPI协议使用两个引脚执行指令代码、地址和数据等所有信号的IO操作，
QIO0 and QIO1.

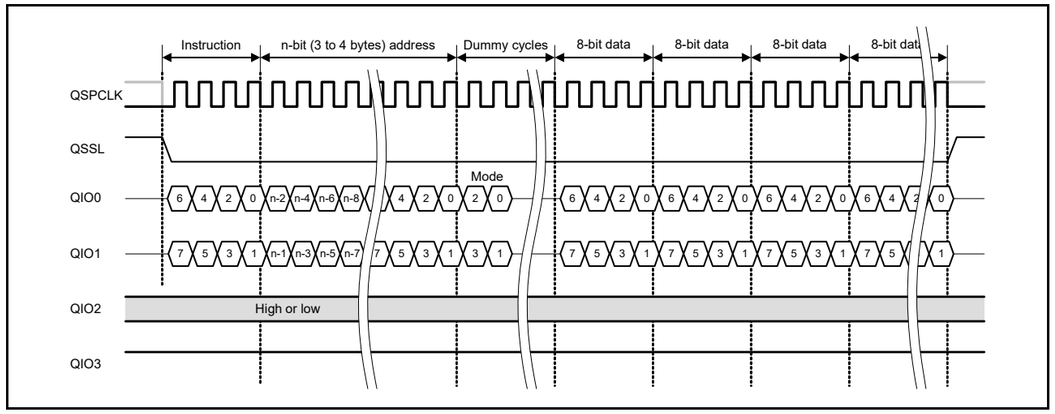


Figure 39.6 Dual SPI protocol example for Fast Read

The Quad SPI protocol performs I/O operation of all signals such as instruction codes, addresses, and data using four pins, QIO0, QIO1, QIO2, and QIO3.

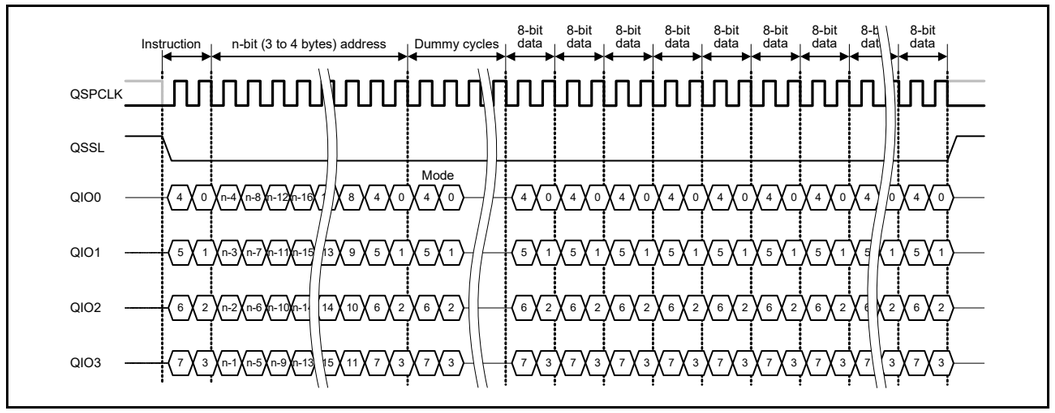


Figure 39.7 Quad SPI protocol example for Fast Read

39.4.2 SPI Mode

Either SPI mode 0 or SPI mode 3 can be selected as the SPI mode. This can be switched by changing the register setting during operation. The difference between SPI modes 0 and 3 is the standby level of the QSPCLK signal. The standby level of the QSPCLK signal in SPI mode 0 is low, and high in SPI mode 3.

Serial data is output from the QSPI on a falling edge of the serial clock and is read into the external flash on a rising edge of the serial clock. Serial data is output from the external flash on a falling edge of the serial clock and is read into the QSPI on the next falling edge of the serial clock.

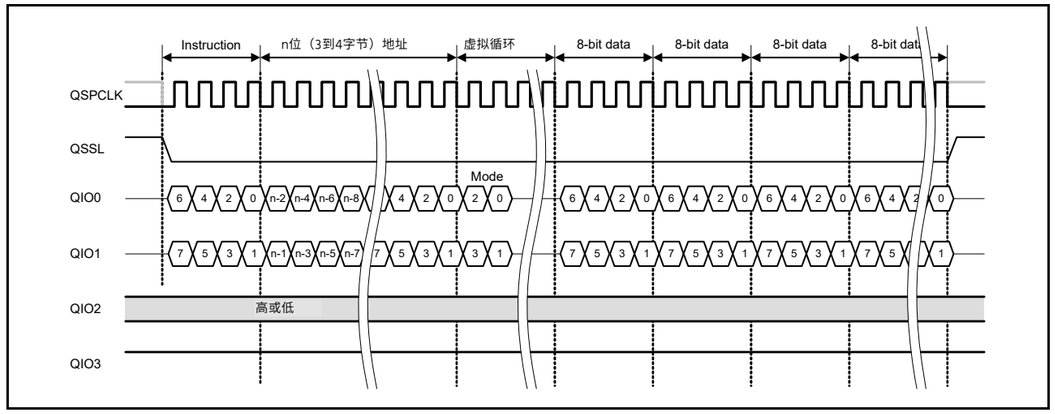


Figure 39.6 用于快速读取的双SPI协议示例

QuadSPI协议使用四个引脚QIO0、QIO1、QIO2和QIO3对指令代码、地址和数据等所有信号执行IO操作。

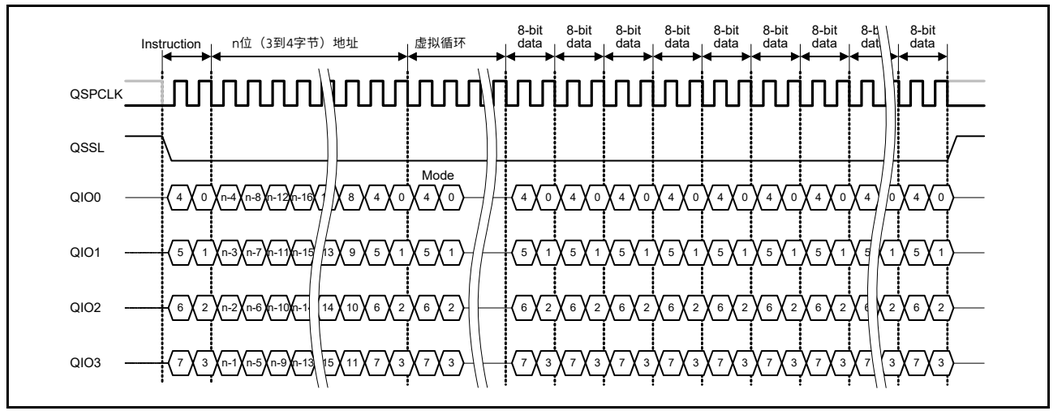


Figure 39.7 用于快速读取的QuadSPI协议示例

39.4.2 SPI模式

SPI模式0或SPI模式3均可选择为SPI模式。这可以通过在操作期间更改寄存器设置来切换。SPI模式0和3的区别在于QSPCLK信号的待机电平。QSPCLK信号在SPI模式0中的待机电平为低，在SPI模式3中为高。

串行数据在串行时钟的下降沿从QSPI输出，并在串行时钟的上升沿读入外部闪存。串行数据在串行时钟的下降沿从外部闪存输出，并在串行时钟的下一个下降沿读入QSPI。

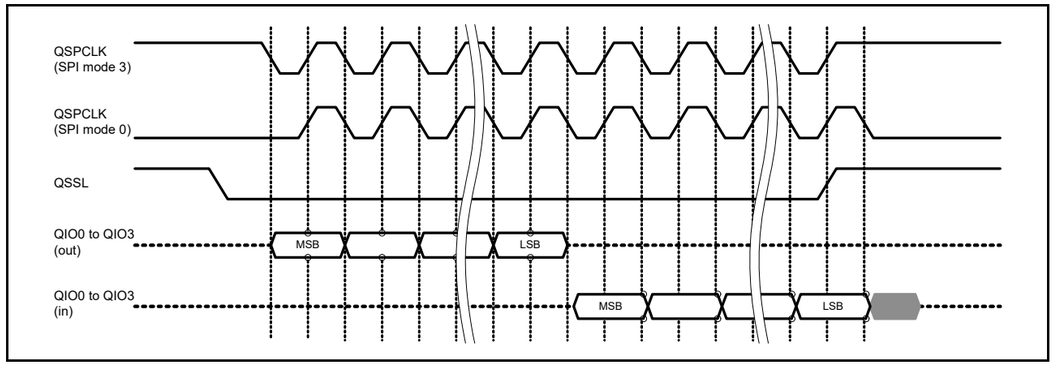


Figure 39.8 Basic serial interface timing

39.5 SPI Bus Timing Adjustment

The timing of the SPI bus signal can be adjusted in the registers. The configured timing is applied to all SPI bus accesses, for both ROM access and direct communication.

39.5.1 SPI Bus Reference Cycles

The SPI bus operates on reference cycles obtained by multiplying PCLKA by an integer. The reference cycles are selectable within the range of PCLKA multiplied by 2 to 48 in the SFMDV[4:0] bits in the SFMSKC register.

Table 39.3 Relationship among SFMDV[4:0] bits, cycle multiplier, and serial clock frequencies (1 of 2)

SFMDV[4:0]	Cycle multiplier	PCLKA frequency (MHz)
		120
11111	48	2.50
11110	46	2.61
11101	44	2.73
11100	42	2.86
11011	40	3.00
11010	38	3.16
11001	36	3.33
11000	34	3.53
10111	32	3.75
10110	30	4.00
10101	28	4.29
10100	26	4.62
10011	24	5.00
10010	22	5.45
10001	20	6.00
10000	18	6.67
01111	17	7.06
01110	16	7.50
01101	15	8.00
01100	14	8.57
01011	13	9.23
01010	12	10.00

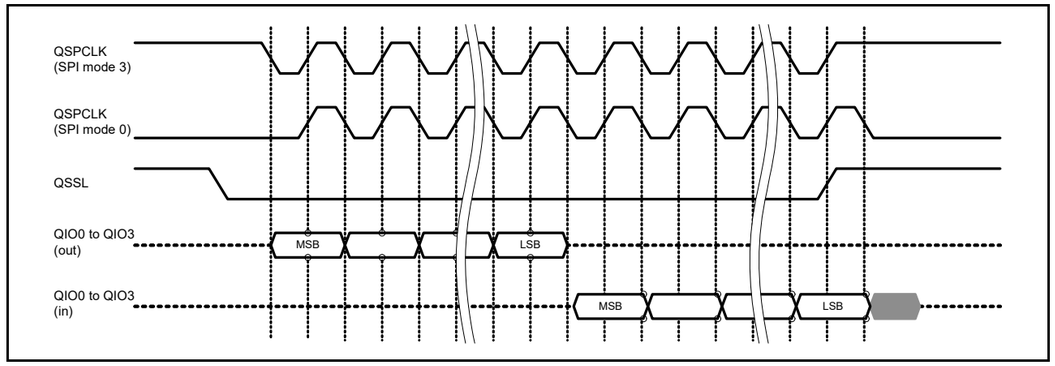


Figure 39.8 基本串行接口时序

39.5 SPI总线时序调整

SPI总线信号的时序可以在寄存器中调整。配置的时序适用于所有SPI总线访问，包括ROM访问和直接通信。

39.5.1 SPI总线参考周期

SPI总线在通过将PCLKA乘以一个整数获得的参考周期上运行。参考周期可在SFMSKC寄存器的SFMDV[4:0]位中的PCLKA乘以2到48的范围内选择。

Table 39.3 SFMDV[4:0]位、周期乘数和串行时钟频率之间的关系（1of2）

SFMDV[4:0]	循环乘数	PCLKA frequency (MHz)
		120
11111	48	2.50
11110	46	2.61
11101	44	2.73
11100	42	2.86
11011	40	3.00
11010	38	3.16
11001	36	3.33
11000	34	3.53
10111	32	3.75
10110	30	4.00
10101	28	4.29
10100	26	4.62
10011	24	5.00
10010	22	5.45
10001	20	6.00
10000	18	6.67
01111	17	7.06
01110	16	7.50
01101	15	8.00
01100	14	8.57
01011	13	9.23
01010	12	10.00

Table 39.3 Relationship among SFMDV[4:0] bits, cycle multiplier, and serial clock frequencies (2 of 2)

SFMDV[4:0]	Cycle multiplier	PCLKA frequency (MHz)
		120
01001	11	10.91
01000	10	12.00
00111	9	13.33
00110	8	15.00
00101	7	17.14
00100	6	20.00
00011	5	24.00
00010	4	30.00
00001	3	40.00
00000	2	60.00

39.5.2 QSPCLK Signal Duty Ratio

When the reference clock is configured as PCLKA multiplied by an even number, the high- and low-level widths of the QSPCLK signal match each other. When PCLKA is multiplied by an odd number, however, the high-level width is longer than the low-level width by 1 PCLKA.

To make the duty ratio of the QSPCLK signal close to 50% when PCLKA multiplied by an odd number is the reference clock, set the SFMDTY bit in the SFMSKC register to 1. With this setting, the rising edge of the QSPCLK output signal is delayed by one-half PCLKA cycle to perform an interface operation equivalent to a duty ratio of 50%.

When the reference clock is PCLKA multiplied by an even number, the SFMDTY setting in the SFMSKC register is ignored.

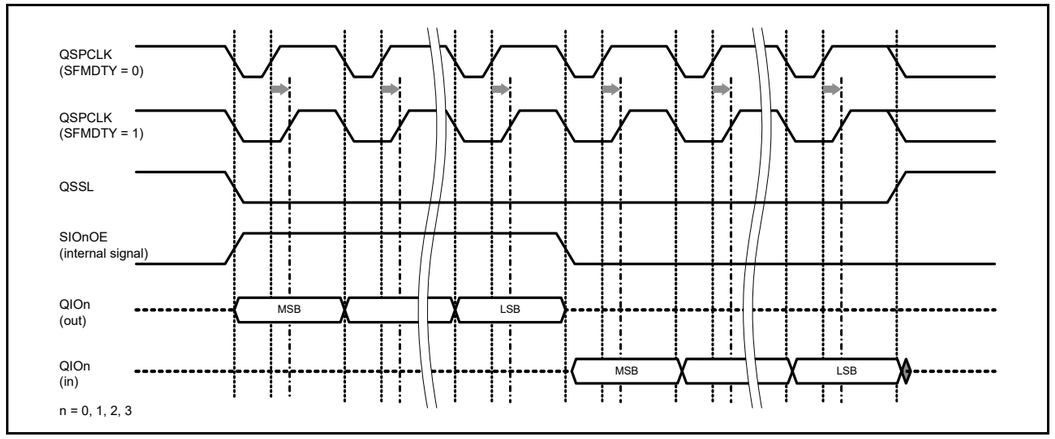


Figure 39.9 Example correction of the QSPCLK signal duty ratio using the SFMDTY bit, when PCLKA is multiplied by 3

39.5.3 Minimum High-Level Width for the QSSL Signal

Between adjacent SPI bus cycles, the QSSL signal must be held high (inactive) for a sufficient time to satisfy the deselect time required by the serial flash. The minimum high-level width of the QSSL output signal is selectable as the reference cycle multiplied by an integer from 1 to 16 in the SFMSW[3:0] bits in the SFMSSC register.

39.5.4 QSSL Signal Setup Time

When the QSPCLK signal first rises after the QSSL signal is driven low, the QSSL signal setup time can be configured to satisfy the serial flash requirements. The setup time can be selectable as 0.5 QSPCLK or 1.5 QSPCLK in the SFMSLD

Table 39.3 SFMDV[4:0]位、周期乘数和串行时钟频率之间的关系(2of2)

SFMDV[4:0]	循环乘数	PCLKA frequency (MHz)
		120
01001	11	10.91
01000	10	12.00
00111	9	13.33
00110	8	15.00
00101	7	17.14
00100	6	20.00
00011	5	24.00
00010	4	30.00
00001	3	40.00
00000	2	60.00

39.5.2 QSPCLK信号占空比

当参考时钟配置为PCLKA乘以偶数时，
QSPCLK信号相互匹配。然而，当PCLKA乘以奇数时，高电平宽度比低电平宽度长1个PCLKA。

当PCLKA乘以奇数作为参考时钟时，为了使QSPCLK信号的占空比接近50%，请将SFMSKC寄存器中的SFMDTY位设置为1。通过此设置，QSPCLK输出信号的上升沿被延迟通过半个PCLKA周期来执行相当于50%占空比的接口操作。

当参考时钟是PCLKA乘以偶数时，SFMSKC寄存器中的SFMDTY设置将被忽略。

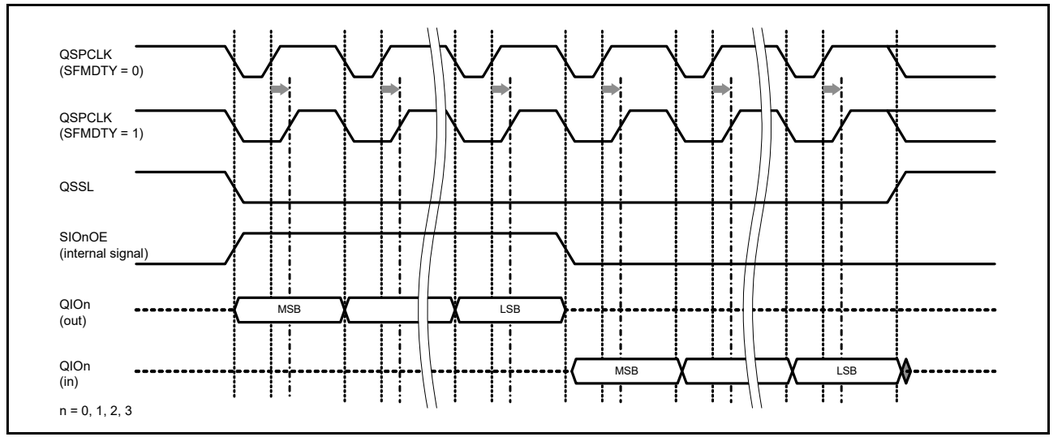


Figure 39.9 当PCLKA乘以3时，使用SFMDTY位校正QSPCLK信号占空比的示例

39.5.3 QSSL信号的最小高电平宽度

在相邻的SPI总线周期之间，QSSL信号必须保持高电平（无效）足够长的时间，以满足串行闪存所需的取消选择时间。QSSL输出信号的最小高电平宽度可选择为参考周期乘以SFMSSC寄存器中SFMSW[3:0]位中1到16的整数。

39.5.4 QSSL信号建立时间

当QSSL信号被驱动为低电平后QSPCLK信号首次上升时，可以配置QSSL信号建立时间以满足串行闪存的要求。建立时间可以在SFMSLD中选择为0.5QSPCLK或1.5QSPCLK

bit in the SFMSSC register.

The SFMSLD setting in the SFMSSC register is also applied to the allocate a setup time from the output of the serial data output enable signal (QIO0OE, QIO1OE, QIO2OE, or QIO3OE) until the first rising edge of the QSPCLK signal. Set a value that meets the most constrained timing condition for your application.

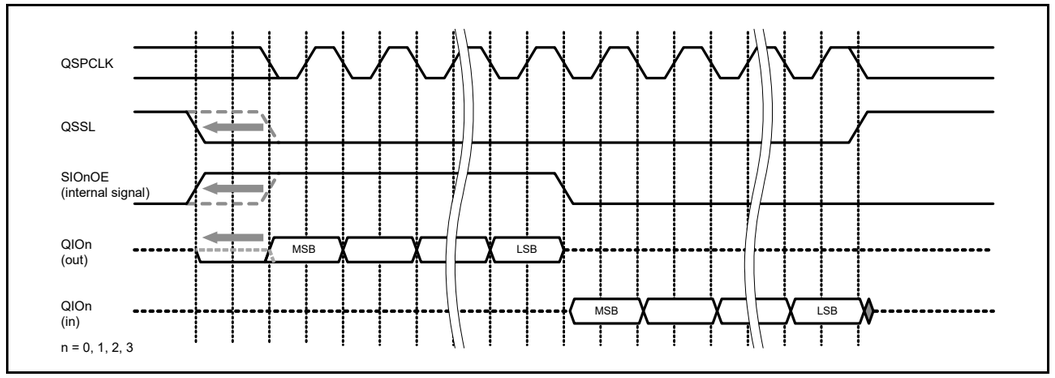


Figure 39.10 Setup time adjustment for the QSSL signal using the SFMSLD bit

39.5.5 QSSL Signal Hold Time

When the QSSL signal is driven high after the last rising edge of the QSPCLK signal, the QSSL signal hold time can be configured to satisfy the device requirements. The hold time is selectable as 0.5 QSPCLK or 1.5 QSPCLK in the SFMSHD bit in the SFMSSC register.

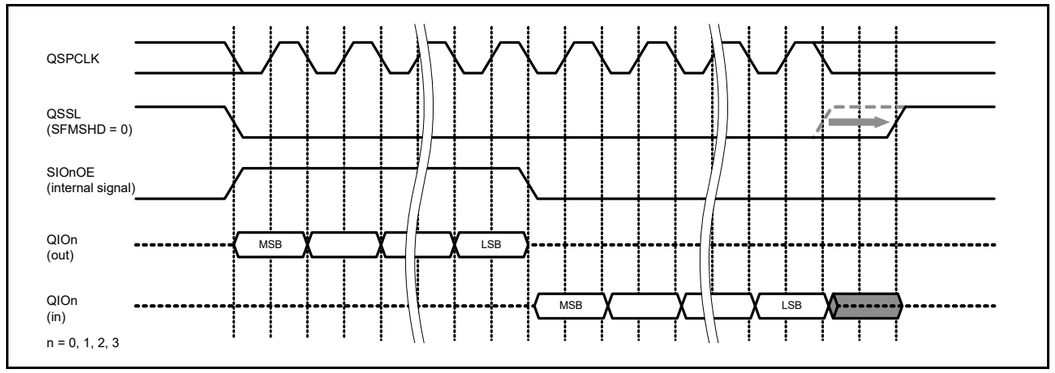


Figure 39.11 Hold time adjustment for the QSSL signal using the SFMSHD bit

39.5.6 Hold Time of the Serial Data Output Enable

The buffer output enable of the QIO0, QIO1, QIO2, or QIO3 pin can be extended by 1 QSPCLK using the SFMOEX bit in the SFMSMD register. The target extension signals include only the output enable signals: QIO0E, QIO1OE, QIO2OE, and QIO3OE. They do not include the output data signals: QIO0O, QIO1O, QIO2O, or QIO3O.

SFMSSC寄存器中的位。

SFMSSC寄存器中的SFMSLD设置也用于分配从串行数据输出使能信号（QIO0OE、QIO1OE、QIO2OE或QIO3OE）输出到QSPCLK信号的第一个上升沿的建立时间。为您的应用设置一个满足最受约束的时序条件的值。

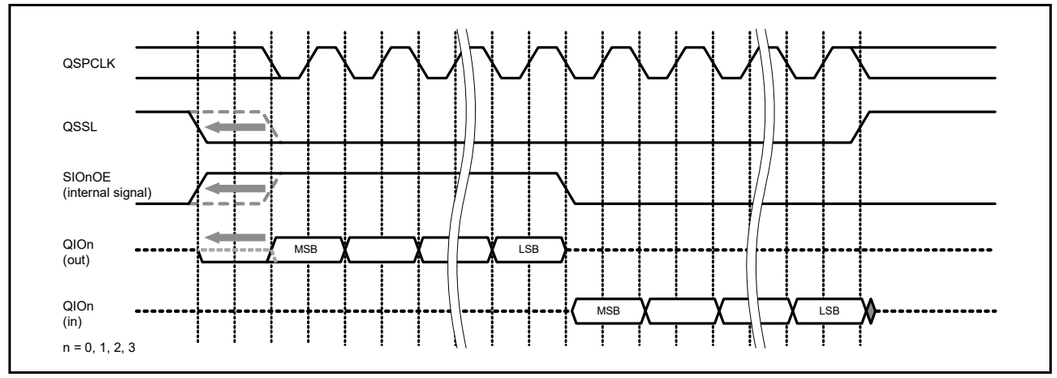


Figure 39.10 使用SFMSLD位调整QSSL信号的建立时间

39.5.5 QSSL信号保持时间

当QSSL信号在QSPCLK信号的最后一个上升沿后被驱动为高电平时，可以配置QSSL信号保持时间以满足器件要求。保持时间可在SFMSSC寄存器的SFMSHD位中选择为0.5QSPCLK或1.5QSPCLK。

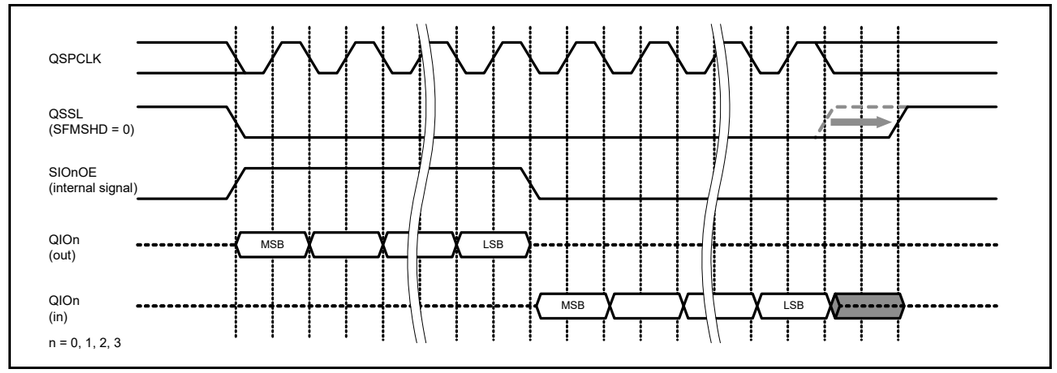


Figure 39.11 使用SFMSHD位调整QSSL信号的保持时间

39.5.6 串行数据输出使能的保持时间

可以使用SFMSMD寄存器中的SFMOEX位将QIO0、QIO1、QIO2或QIO3引脚的缓冲器输出使能扩展1个QSPCLK。目标扩展信号仅包括输出使能信号：QIO0E、QIO1OE、QIO2OE和QIO3OE。它们不包括输出数据信号：QIO0O、QIO1O、QIO2O或QIO3O。

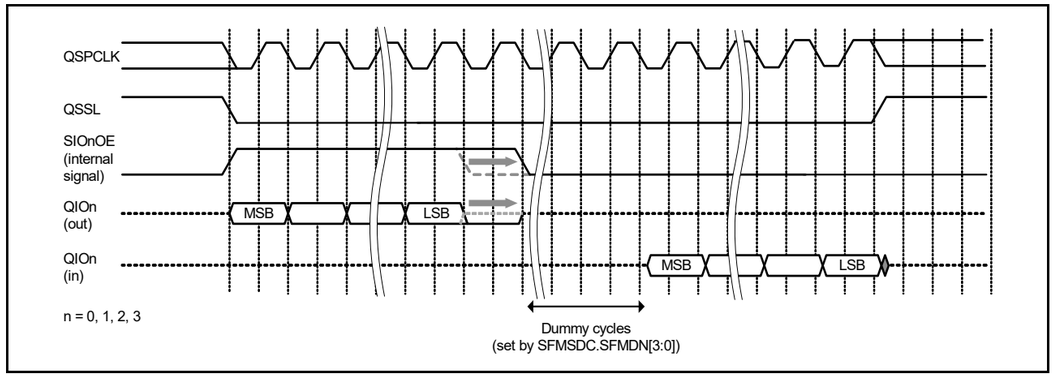


Figure 39.12 Hold time adjustment for output enable using the SFMOEX bit

39.5.7 Setup Time for Serial Data Output

When a command or address is transmitted to the serial flash, the setup time begins on serial data output and ends when the QSPCLK signal rises. If this setup time is insufficient, it can be extended by 1 PCLKA using the SFMOSW bit in the SFMSMD register. When SFMOSW is 1, the low-level width of QSPCLK during serial data transmission is extended by 1 PCLKA while data is being output from the QSPI. This function has no effect on serial data reception.

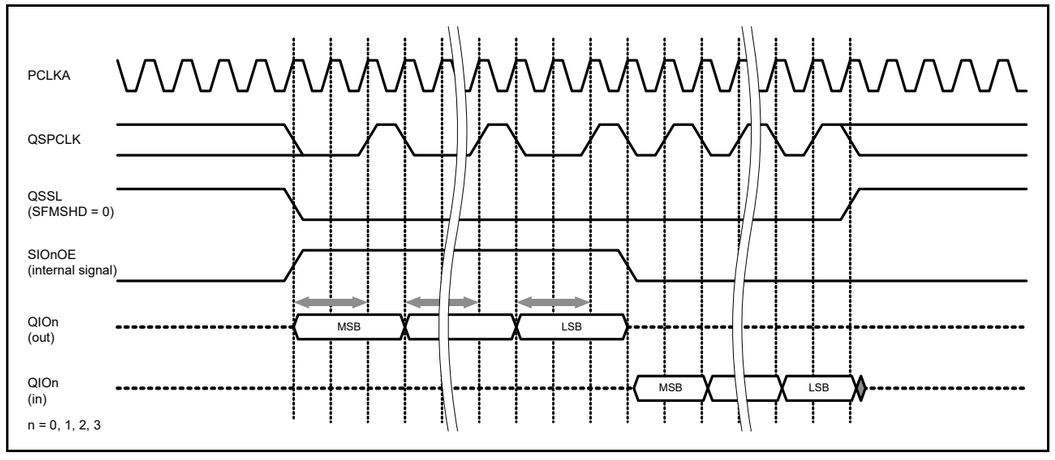


Figure 39.13 Setup time adjustment for serial data output using the SFMOSW bit

39.5.8 Hold Time for Serial Data Output

When a command or address is transmitted to the serial flash, the hold time begins on the rising edge of QSPCLK and ends when the serial data makes another transmission. If this hold time is insufficient, it can be extended by 1 PCLKA using the SFMOHW bit in the SFMSMD register. When SFMOSW is 1, the high-level width of QSPCLK during serial data transmission is extended by 1 PCLKA while data is being output from the QSPI. This function has no effect on serial data reception.

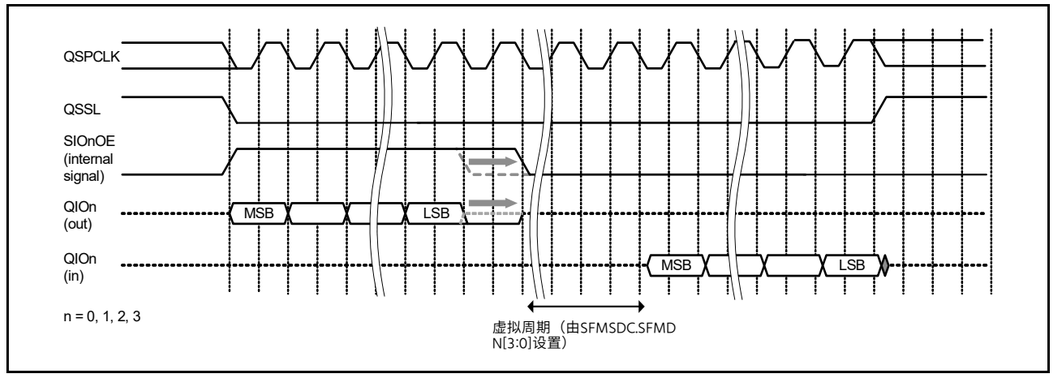


Figure 39.12 使用SFMOEX位调整输出使能的保持时间

39.5.7 串行数据输出的建立时间

当命令或地址传输到串行闪存时，设置时间从串行数据输出开始，到QSPCLK信号上升时结束。如果此建立时间不足，可以使用SFMSMD寄存器中的SFMOSW位将其延长1个PCLKA。当SFMOSW为1时，在从QSPI输出数据时，串行数据传输期间QSPCLK的低电平宽度扩展1PCLKA。该功能对串行数据接收没有影响。

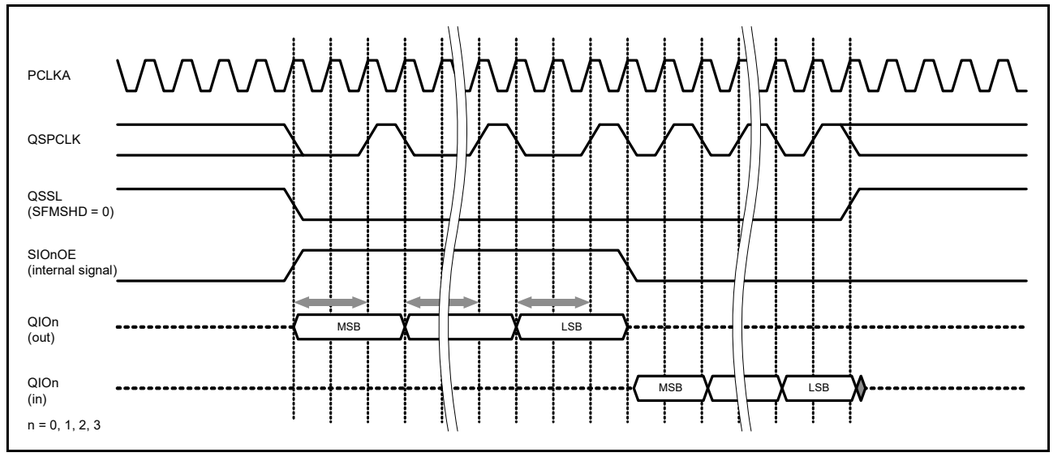


Figure 39.13 使用SFMOSW位调整串行数据输出的建立时间

39.5.8 串行数据输出的保持时间

当命令或地址传输到串行闪存时，保持时间从QSPCLK的上升沿开始，并在串行数据进行另一次传输时结束。如果该保持时间不足，可以使用SFMSMD寄存器中的SFMOHW位将其延长1个PCLKA。当SFMOSW为1时，在从QSPI输出数据时，串行数据传输期间QSPCLK的高电平宽度扩展1PCLKA。该功能对串行数据接收没有影响。

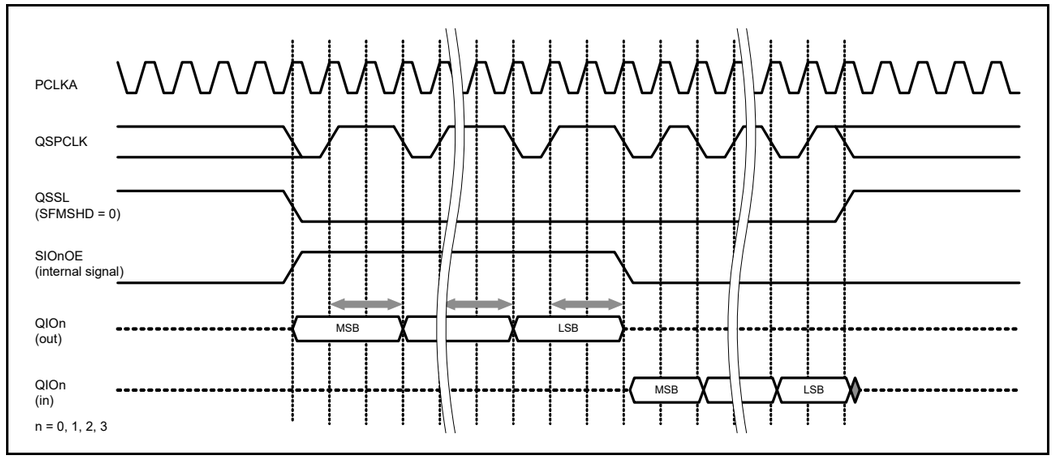


Figure 39.14 Hold time adjustment for serial data output using the SFMOHW bit

39.6 SPI Instruction Set Used for Flash Access

39.6.1 SPI Instructions That Are Automatically Generated

When the serial flash is accessed, an SPI bus cycle using one of the instructions described in Table 39.4 to Table 39.8 is automatically generated based on the settings in the SFMAS[1:0] bits in the SFMSAC register and in the SFMSMD register.

Table 39.4 SPI instructions automatically generated when SFMAS[1:0] = 00b

Instruction format	Instruction code	Address bytes	Dummy cycles	Data bytes	Remarks
Read	03h*1	1	—	1 to ∞	Required: SFMRM[2:0] = 000, A8 = 0
	0Bh*1	1	—	1 to ∞	Required: SFMRM[2:0] = 000, A8 = 1

Note 1. If the SFMSMD.SFMCCE bit is set to 1, the SFMSIC.SFMCIC[7:0] setting is used as an instruction code.

Table 39.5 SPI instructions automatically generated when SFMAS[1:0] = 01b

Instruction format	Instruction code	Address bytes	Dummy cycles	Data bytes	Remarks
Read	03h*1	2	—	1 to ∞	Required: SFMRM[2:0] = 000

Note 1. If the SFMSMD.SFMCCE bit is set to 1, the SFMSIC.SFMCIC[7:0] setting is used as an instruction code.

Table 39.6 SPI instructions automatically generated when SFMAS[1:0] = 10b (1 of 2)

Instruction format	Instruction code	Address bytes	Dummy cycles	Data bytes	Remarks
Read	03h*1	3	—	1 to ∞	Required: SFMRM[2:0] = 000
Fast Read	0Bh*1	3	8*2	1 to ∞	Selectable: SFMRM[2:0] = 001
Fast Read Dual Output	3Bh*1	3	8*2	1 to ∞	Selectable: SFMRM[2:0] = 010
Fast Read Dual I/O	BBh*1	3	4*2	1 to ∞	Selectable: SFMRM[2:0] = 011
Fast Read Quad Output	6Bh*1	3	8*2	1 to ∞	Selectable: SFMRM[2:0] = 100
Fast Read Quad I/O	EBh*1	3	6*2	1 to ∞	Selectable: SFMRM[2:0] = 101

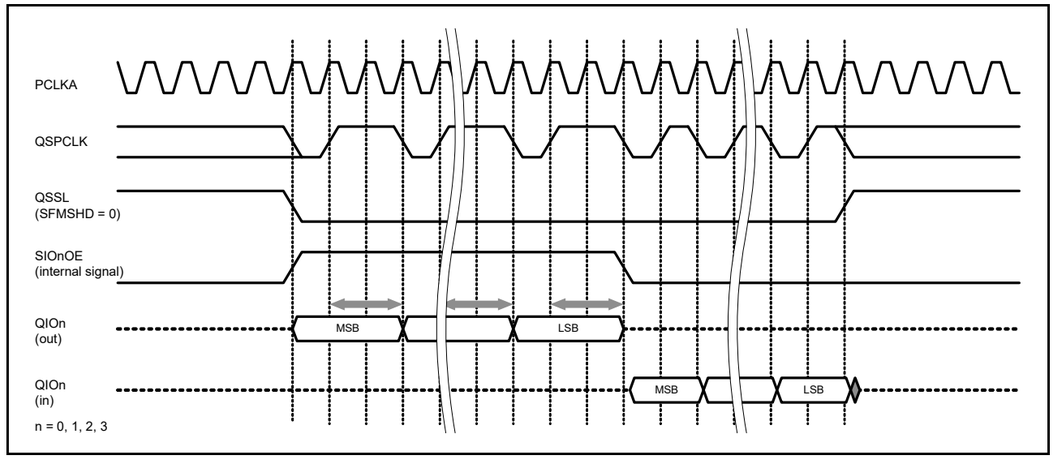


Figure 39.14 使用SFMOHW位调整串行数据输出的保持时间

39.6 用于闪存访问的SPI指令集

39.6.1 自动生成的SPI指令

访问串行闪存时，会根据SFMSAC寄存器和SFMSMD寄存器中的SFMAS[1:0]位的设置自动生成使用表39.4至表39.8中描述的指令之一的SPI总线周期。

Table 39.4 SFMAS[1:0]=00b时自动生成SPI指令

指令格式	指令码	地址字节	虚拟循环	数据字节	Remarks
Read	03h*1	1	—	1 to ∞	Required: SFMRM[2:0] = 000, A8 = 0
	0Bh*1	1	—	1 to ∞	Required: SFMRM[2:0] = 000, A8 = 1

Note 1. 如果SFMSMD.SFMCCE位设置为1，则SFMSIC.SFMCIC[7:0]设置用作指令代码。

Table 39.5 SFMAS[1:0]=01b时自动生成SPI指令

指令格式	指令码	地址字节	虚拟循环	数据字节	Remarks
Read	03h*1	2	—	1 to ∞	Required: SFMRM[2:0] = 000

Note 1. 如果SFMSMD.SFMCCE位设置为1，则SFMSIC.SFMCIC[7:0]设置用作指令代码。

Table 39.6 当SFMAS[1:0]=10b(1of2)时自动生成SPI指令

指令格式	指令码	地址字节	虚拟循环	数据字节	Remarks
Read	03h*1	3	—	1 to ∞	Required: SFMRM[2:0] = 000
快速阅读	0Bh*1	3	8*2	1 to ∞	Selectable: SFMRM[2:0] = 001
快速读取双输出	3Bh*1	3	8*2	1 to ∞	Selectable: SFMRM[2:0] = 010
快速读取双IO	BBh*1	3	4*2	1 to ∞	Selectable: SFMRM[2:0] = 011
快速读取四路输出	6Bh*1	3	8*2	1 to ∞	Selectable: SFMRM[2:0] = 100
快速读取四路IO	EBh*1	3	6*2	1 to ∞	Selectable: SFMRM[2:0] = 101

Table 39.6 SPI instructions automatically generated when SFMAS[1:0] = 10b (2 of 2)

Instruction format	Instruction code	Address bytes	Dummy cycles	Data bytes	Remarks
Write Enable	06h	—	—	—	Selectable: ENEX4B[1:0] = 10
Exit 4-Byte Mode	E9h	—	—	—	Selectable: ENEX4B[1:0] = 01,10

Note 1. If the SFMSMD.SFMCCE bit is set to 1, the SFMSIC.SFMCIC[7:0] setting is used as an instruction code.
Note 2. The number of dummy cycles is configurable in SFMSDC.SFMDN[3:0].

Table 39.7 SPI instructions automatically generated when SFMAS[1:0] = 11b and SFM4BC = 0

Instruction format	Instruction code	Address bytes	Dummy cycles	Data bytes	Remarks
Read	03h*1	4	—	1 to ∞	Required: SFMRM[2:0] = 000
Fast Read	0Bh*1	4	8*2	1 to ∞	Selectable: SFMRM[2:0] = 001
Fast Read Dual Output	3Bh*1	4	8*2	1 to ∞	Selectable: SFMRM[2:0] = 010
Fast Read Dual I/O	BBh*1	4	4*2	1 to ∞	Selectable: SFMRM[2:0] = 011
Fast Read Quad Output	6Bh*1	4	8*2	1 to ∞	Selectable: SFMRM[2:0] = 100
Fast Read Quad I/O	EBh*1	4	6*2	1 to ∞	Selectable: SFMRM[2:0] = 101
Write Enable	06h	—	—	—	Selectable: ENEX4B[1:0] = 10
Enter 4-Byte Mode	B7h	—	—	—	Selectable: ENEX4B[1:0] = 01,10

Note 1. If the SFMSMD.SFMCCE bit is set to 1, the SFMSIC.SFMCIC[7:0] setting is used as an instruction code.
Note 2. The number of dummy cycles is configurable in SFMSDC.SFMDN[3:0].

Table 39.8 SPI instructions automatically generated when SFMAS[1:0] = 11b and SFM4BC = 1

Instruction format	Instruction code	Address bytes	Dummy cycles	Data bytes	Remarks
Read	13h*1	4	—	1 to ∞	Required: SFMRM[2:0] = 000
Fast Read	0Ch*1	4	8*2	1 to ∞	Selectable: SFMRM[2:0] = 001
Fast Read Dual Output	3Ch*1	4	8*2	1 to ∞	Selectable: SFMRM[2:0] = 010
Fast Read Dual I/O	BCh*1	4	4*2	1 to ∞	Selectable: SFMRM[2:0] = 011
Fast Read Quad Output	6Ch*1	4	8*2	1 to ∞	Selectable: SFMRM[2:0] = 100
Fast Read Quad I/O	ECh*1	4	6*2	1 to ∞	Selectable: SFMRM[2:0] = 101
Write Enable	06h	—	—	—	Selectable: ENEX4B[1:0] = 10
Enter 4-Byte Mode	B7h	—	—	—	Selectable: ENEX4B[1:0] = 01,10

Note 1. If the SFMSMD.SFMCCE bit is set to 1, the SFMSIC.SFMCIC[7:0] setting is used as an instruction code.
Note 2. The number of dummy cycles is configurable in SFMSDC.SFMDN[3:0].

39.6.2 Standard Read Instruction

The standard Read instruction is a common read instruction supported by most serial flash. When an SPI bus cycle starts, the serial flash select signal is asserted, and the instruction code (03h/13h)*1 is output. Next, an address with a width of 1 to 4 bytes, specified in the SFMAS[1:0] bits in the SFMSAC register, is transmitted. Data is then received.

This standard Read instruction is selected in the initial QSPI settings.

Note 1. Many 4-Kb serial flash devices have an address field not larger than 1 byte (A7-A0) to minimize the overhead and to receive A8 information from bit 3 of the Read instruction code. To support these devices, the QSPI only outputs A8 (address bit 8) to bit [3] of the standard Read instruction code when an address width of 1 byte is specified (SFMAS[1:0] = 00). This means that 0Bh might be output instead of 03h as the standard Read instruction code. This code duplicates the Fast Read instruction code. However, for most of the 2-Kb or smaller serial flash devices, with an address width of 1 byte, bit 3 of a command is designed to be excluded from

Table 39.6 当SFMAS[1:0]=10b(2of2)时自动生成SPI指令

指令格式	指令码	地址字节	虚拟循环	数据字节	Remarks
写使能	06h	—	—	—	Selectable: ENEX4B[1:0] = 10
退出4字节模式	E9h	—	—	—	Selectable: ENEX4B[1:0] = 01,10

Note 1. 如果SFMSMD.SFMCCE位设置为1，则SFMSIC.SFMCIC[7:0]设置用作指令代码。
Note 2. 虚拟周期数可在SFMSDC.SFMDN[3:0]中配置。

Table 39.7 当SFMAS[1:0]=11b和SFM4BC=0时自动生成SPI指令

指令格式	指令码	地址字节	虚拟循环	数据字节	Remarks
Read	03h*1	4	—	1 to ∞	Required: SFMRM[2:0] = 000
快速阅读	0Bh*1	4	8*2	1 to ∞	Selectable: SFMRM[2:0] = 001
快速读取双输出	3Bh*1	4	8*2	1 to ∞	Selectable: SFMRM[2:0] = 010
快速读取双IO	BBh*1	4	4*2	1 to ∞	Selectable: SFMRM[2:0] = 011
快速读取四路输出	6Bh*1	4	8*2	1 to ∞	Selectable: SFMRM[2:0] = 100
快速读取四路IO	EBh*1	4	6*2	1 to ∞	Selectable: SFMRM[2:0] = 101
写使能	06h	—	—	—	Selectable: ENEX4B[1:0] = 10
进入4字节模式	B7h	—	—	—	Selectable: ENEX4B[1:0] = 01,10

Note 1. 如果SFMSMD.SFMCCE位设置为1，则SFMSIC.SFMCIC[7:0]设置用作指令代码。
Note 2. 虚拟周期数可在SFMSDC.SFMDN[3:0]中配置。

Table 39.8 当SFMAS[1:0]=11b和SFM4BC=1时自动生成SPI指令

指令格式	指令码	地址字节	虚拟循环	数据字节	Remarks
Read	13h*1	4	—	1 to ∞	Required: SFMRM[2:0] = 000
快速阅读	0Ch*1	4	8*2	1 to ∞	Selectable: SFMRM[2:0] = 001
快速读取双输出	3Ch*1	4	8*2	1 to ∞	Selectable: SFMRM[2:0] = 010
快速读取双IO	BCh*1	4	4*2	1 to ∞	Selectable: SFMRM[2:0] = 011
快速读取四路输出	6Ch*1	4	8*2	1 to ∞	Selectable: SFMRM[2:0] = 100
快速读取四路IO	ECh*1	4	6*2	1 to ∞	Selectable: SFMRM[2:0] = 101
写使能	06h	—	—	—	Selectable: ENEX4B[1:0] = 10
进入4字节模式	B7h	—	—	—	Selectable: ENEX4B[1:0] = 01,10

Note 1. 如果SFMSMD.SFMCCE位设置为1，则SFMSIC.SFMCIC[7:0]设置用作指令代码。
Note 2. 虚拟周期数可在SFMSDC.SFMDN[3:0]中配置。

39.6.2 标准阅读说明

标准读指令是大多数串行闪存支持的常见读指令。当一个SPI总线周期开始时，串行闪存选择信号被置位，并输出指令代码(03h13h)*1。接下来，发送宽度为1到4字节的地址，在SFMSAC寄存器的SFMAS[1:0]位中指定。然后接收数据。

在初始QSPI设置中选择此标准读取指令。

注1.许多4-Kb串行闪存设备具有不大于1字节(A7-A0)的地址字段，以最大限度地减少开销并从读取指令代码的第3位接收A8信息。为了支持这些器件，当指定地址宽度为1字节（SFMAS[1:0]=00）时，QSPI仅将A8（地址位8）输出到标准读指令代码的位[3]。这意味着可能会输出0Bh而不是03h作为标准读取指令代码。此代码复制了快速读取指令代码。但是，对于大多数2-Kb或更小的串行闪存设备，地址宽度为1字节，命令的第3位被设计为从

decoding as a don't-care bit, so such a Read instruction code is recognized correctly as the standard Read instruction code. In rare cases, some serial flash devices allow bit 3 to be decoded. When such a serial flash is connected, configure your application to avoid access resulting in A8 = 1.

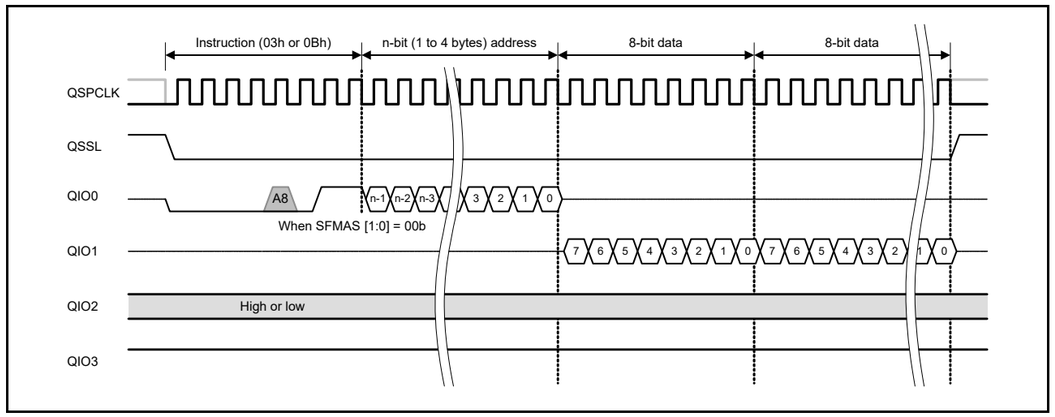


Figure 39.15 Standard Read bus cycle

39.6.3 Fast Read Instruction

The Fast Read instruction is a read instruction that supports a higher communication clock speed than the standard Read instruction. When an SPI bus cycle starts, the serial flash select signal is asserted, and the instruction code (0Bh/0Ch) is output. Next, an address with a width of 1 to 4 bytes, specified in the SFMAS[1:0] bits in SFMSAC, and a certain number of dummy cycles, specified in the SFMSDC register, are transmitted. Data is then received.

The first two dummy cycles are used to select or deselect the XIP mode. When the XIP mode is selected, the same instruction used this time is applied to the next SPI bus cycle, and the instruction code is not output the next SPI bus cycle. For details on the XIP mode, see section 39.8, XIP Control.

Switching to the Fast Read instruction is controlled in the SFMSMD register.

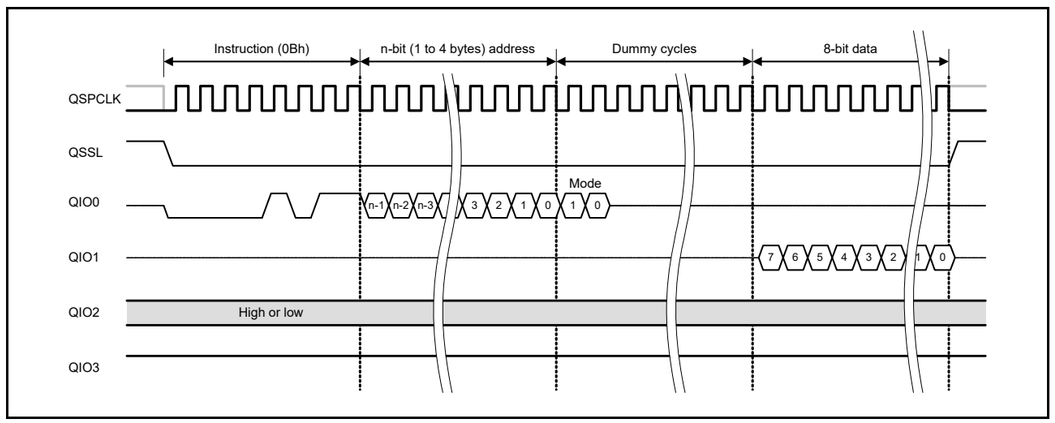


Figure 39.16 Fast Read bus cycle

解码为无关位，因此这样的读取指令代码被正确识别为标准读取指令代码。在极少数情况下，一些串行闪存设备允许对第3位进行解码。连接此类串行闪存时，配置您的应用程序以避免访问导致A8=1。

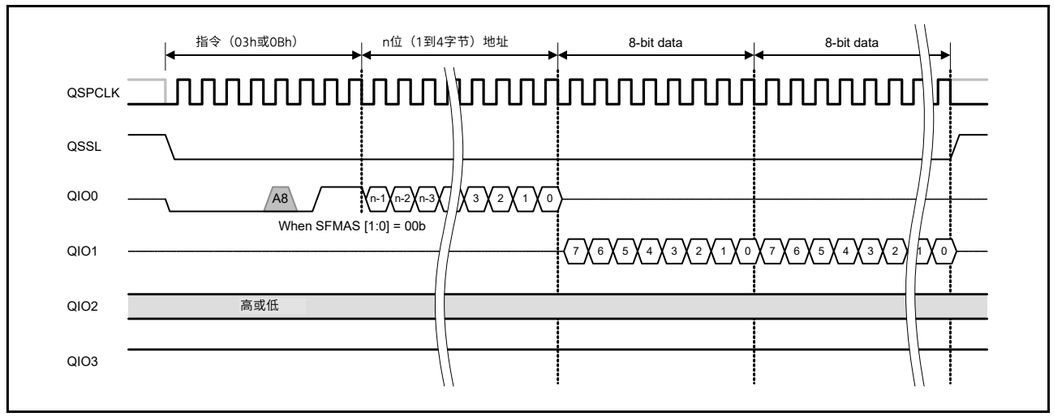


Figure 39.15 标准读总线周期

39.6.3 快速阅读说明

快速读取指令是一种读取指令，它支持比标准读取指令更高的通信时钟速度。当一个SPI总线周期开始时，串行闪存选择信号被置位，并输出指令代码（0Bh0Ch）。接下来，发送宽度为1到4字节的地址，在SFMSAC中的SFMAS[1:0]位中指定，以及在SFMSDC寄存器中指定的一定数量的虚拟周期被发送。然后接收数据。

前两个虚拟周期用于选择或取消选择XIP模式。选择XIP模式时，此时间使用的相同指令将应用于下一个SPI总线周期，并且指令代码未输出下一个SPIBUS周期。有关XIP模式的详细信息，请参阅第39.8节，XIP控制。

切换到快速读取指令在SFMSMD寄存器中进行控制。

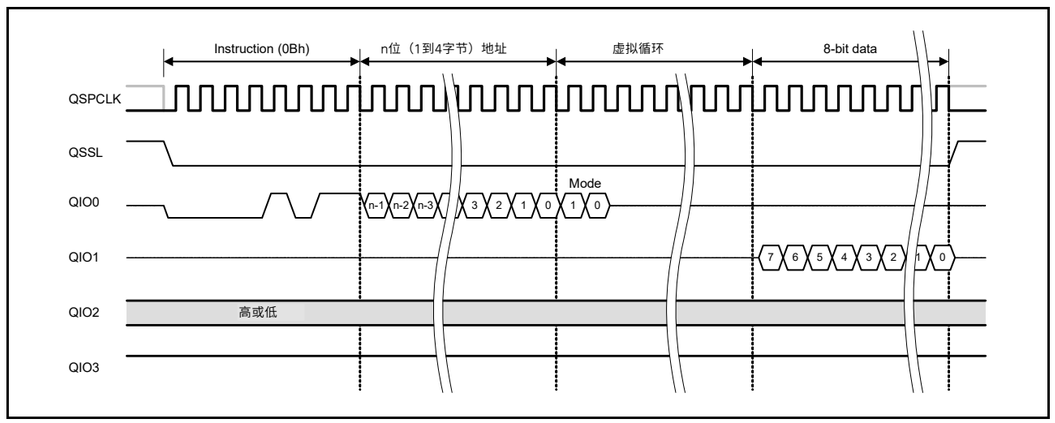


Figure 39.16 快速读取总线周期

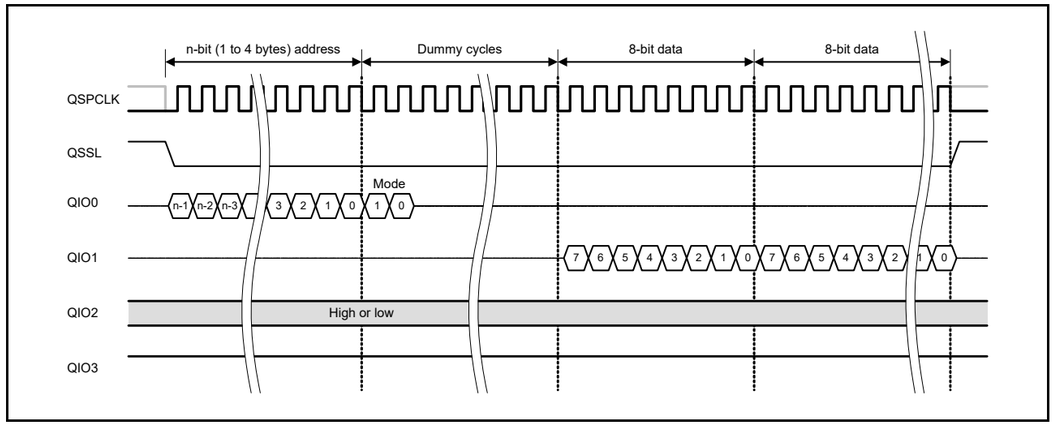


Figure 39.17 Fast Read bus cycle in XIP mode

Note: To use the Fast Read instruction, a serial flash device that supports Fast Read transfers is required.

39.6.4 Fast Read Dual Output Instruction

The Fast Read Dual Output instruction is a read instruction that uses two signal lines to receive data. When the SPI bus cycle starts, the serial flash select signal is asserted. The instruction code (3Bh/3Ch) and an address with a width of 1 to 4 bytes, specified in the SFMAS[1:0] bits in the SFMSAC register, are transmitted from the QIO0 pin. Next, a certain number of dummy cycles, specified in the SFMSDC register, is generated. Data is then received through the QIO0 and QIO1 pins. Even bit data is received from the QIO0 pin and odd bit data is received from the QIO1 pin.

The first two dummy cycles are used to select or deselect the XIP mode. When the XIP mode is selected, the same instruction used this time is applied to the next SPI bus cycle, and the instruction code is not output the next SPI bus cycle. For details on the XIP mode, see section 39.8, XIP Control.

Switching to Fast Read Dual Output is controlled in the SFMSMD register.

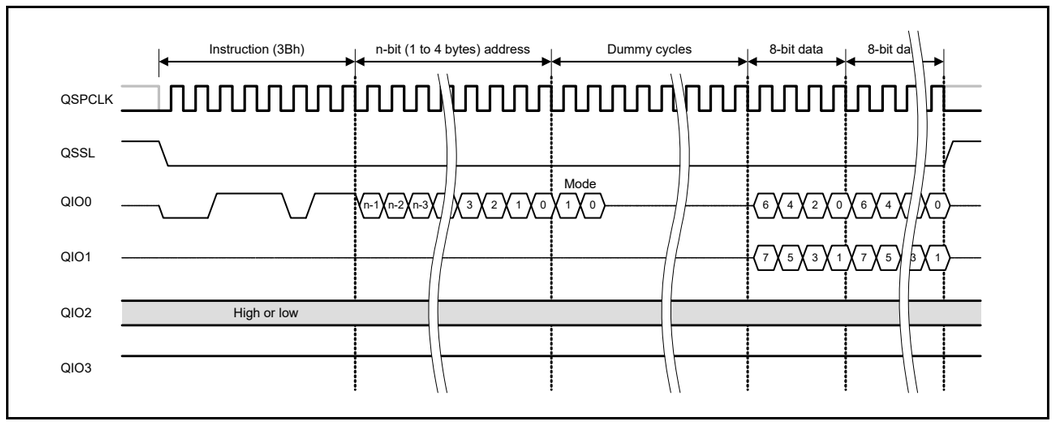


Figure 39.18 Fast Read Dual Output bus cycle

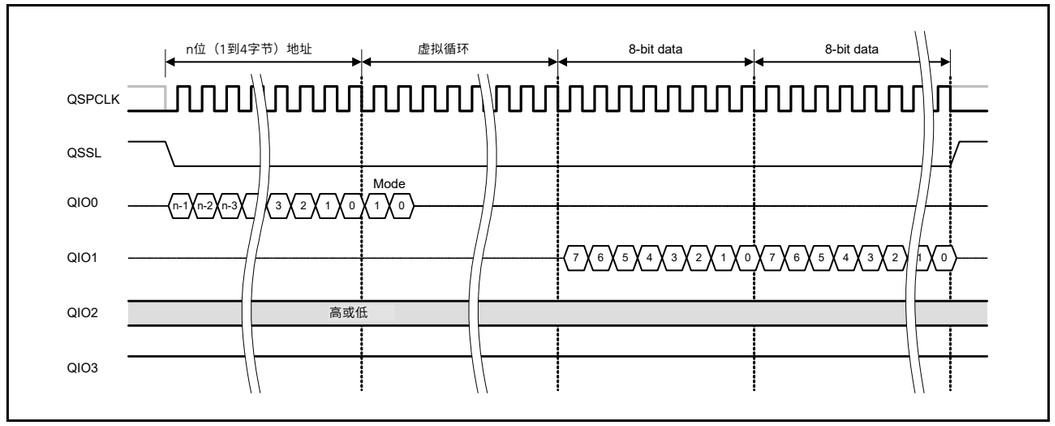


Figure 39.17 XIP模式下的快速读取总线周期

Note: 要使用快速读取指令，需要支持快速读取传输的串行闪存设备。

39.6.4 快速读取双输出指令

快速读取双输出指令是使用两条信号线接收数据的读取指令。当SPI总线周期开始时，串行闪存选择信号被置位。指令代码(3Bh3Ch)和宽度为1到4字节的地址，在SFMSAC寄存器的SFMAS[1:0]位中指定，从QIO0引脚发送。接下来，生成在SFMSDC寄存器中指定的一定数量的虚拟周期。然后通过QIO0和QIO1引脚接收数据。从QIO0引脚接收偶数位数据，从QIO1引脚接收奇数位数据。

前两个虚拟周期用于选择或取消选择XIP模式。选择XIP模式时，此时间使用的相同指令将应用于下一个SPI总线周期，并且指令代码未输出下一个SPIBUS周期。有关XIP模式的详细信息，请参阅第39.8节，XIP控制。

切换到快速读取双路输出由SFMSMD寄存器控制。

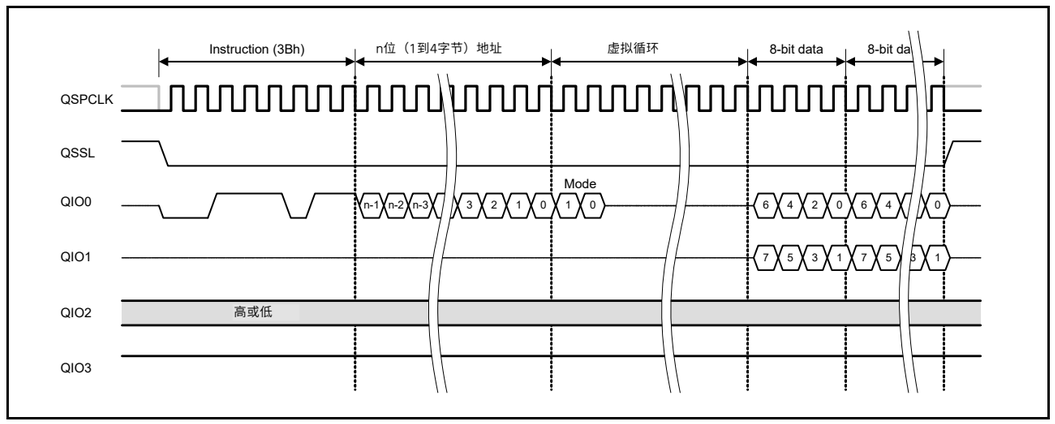


Figure 39.18 快速读取双输出总线周期

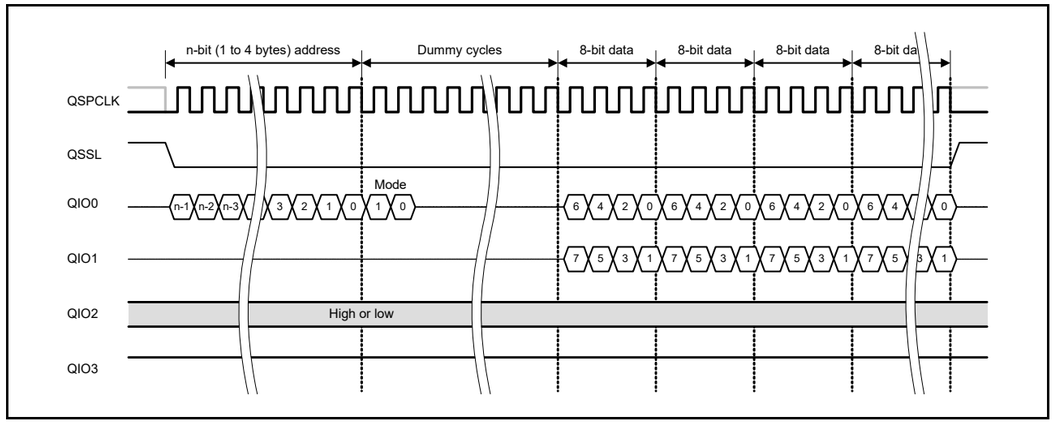


Figure 39.19 Fast Read Dual Output bus cycle in XIP mode

Note: To use the Fast Read Dual Output instruction, a serial flash device that supports Fast Read Dual Output transfers is required.

39.6.5 Fast Read Dual I/O Instruction

The Fast Read Dual I/O instruction is a read instruction that uses two signal lines to transmit an address and receive data. When the SPI bus cycle starts, the serial flash select signal is asserted, and the instruction code (BBh/BCh) is output from the QIO0 pin. Next, an address with a width of 1 to 4 bytes, specified in the SFMAS[1:0] bits in the SFMSAC register, is transmitted through the QIO0 and QIO1 pins, and a certain number of dummy cycles, specified in the SFMSDC register, is generated. Data is then is received through the QIO0 and QIO1 pins. Address and dummy cycle transmission and data reception are performed through the QIO0 pin for even bits and through the QIO1 pin for odd bits.

The first two dummy cycles are used to select or deselect the XIP mode. When the XIP mode is selected, the same instruction used this time is applied to the next SPI bus cycle, and the instruction code is not output the next SPI bus cycle. For details on the XIP mode, see section 39.8, XIP Control.

Switching to Fast Read Dual I/O is controlled in the SFMSMD register.

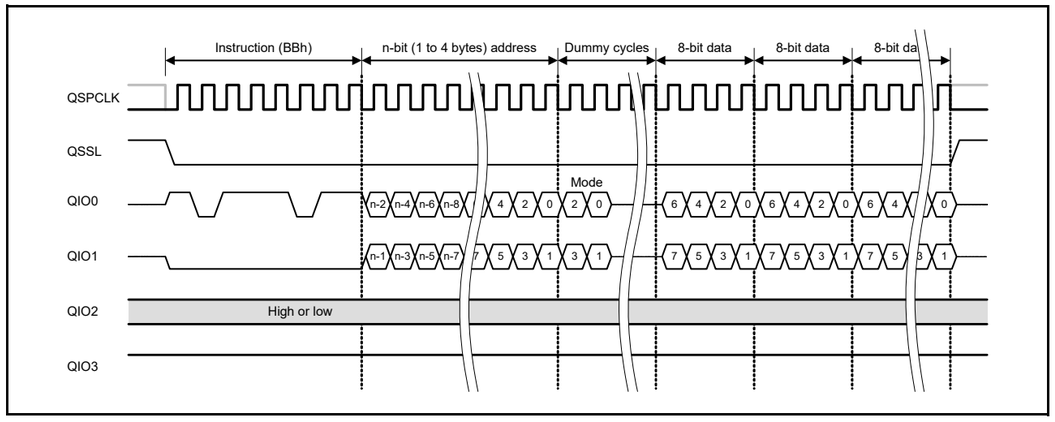


Figure 39.20 Fast Read Dual I/O bus cycle

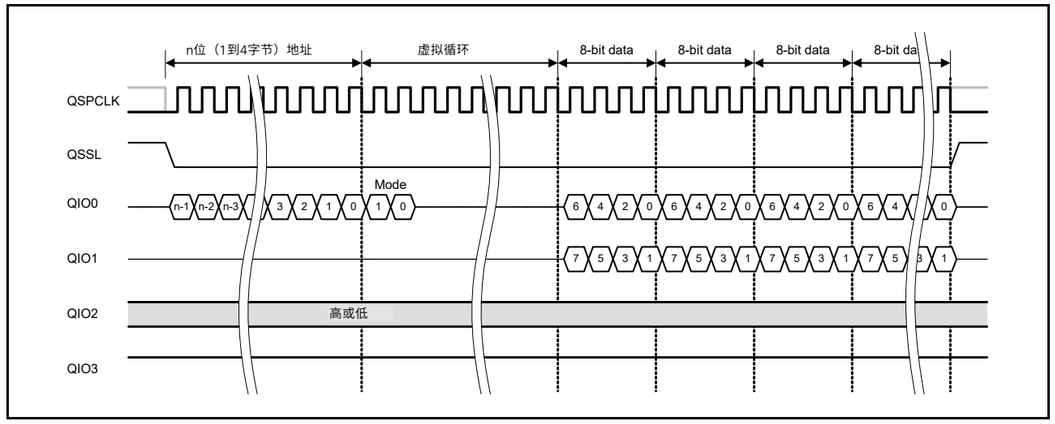


Figure 39.19 XIP模式下的快速读取双输出总线周期

Note: 要使用快速读取双输出指令，需要支持快速读取双输出传输的串行闪存设备。

39.6.5 快速读取双IO指令

FastReadDualIO指令是使用两条信号线传输地址和接收数据的读取指令。当SPI总线周期开始时，串行闪存选择信号被置位，指令代码（BBhBCh）从QIO0引脚输出。接下来，在SFMSAC寄存器的SFMAS[1:0]位中指定的1到4字节宽度的地址通过QIO0和QIO1引脚以及在SFMSDC寄存器中指定的一定数量的空周期发送 生成。然后通过QIO0和QIO1引脚接收数据。地址和虚拟周期的发送和数据接收通过QIO0引脚（偶数位）和QIO1引脚（奇数位）执行。

前两个虚拟周期用于选择或取消选择XIP模式。选择XIP模式时，此时间使用的相同指令将应用于下一个SPI总线周期，并且指令代码未输出下一个SPIBUS周期。有关XIP模式的详细信息，请参阅第39.8节，XIP控制。

切换到快速读取双IO由SFMSMD寄存器控制。

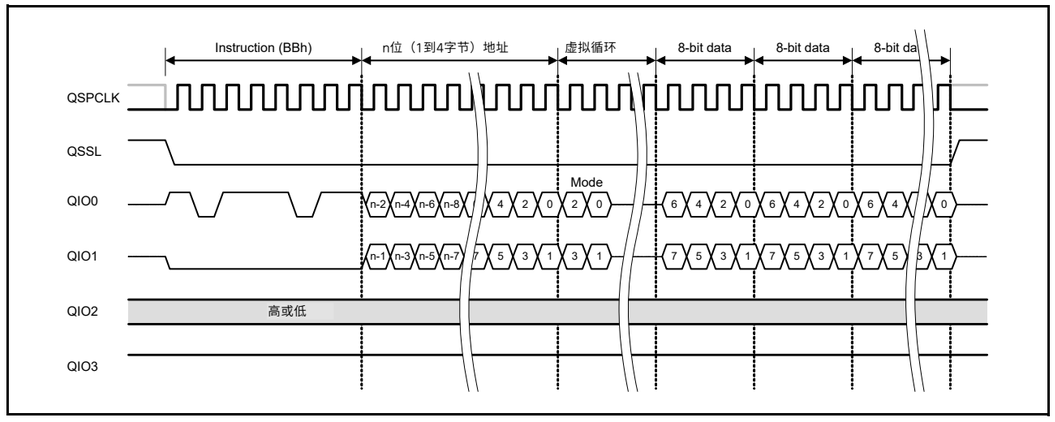


Figure 39.20 快速读取双IO总线周期

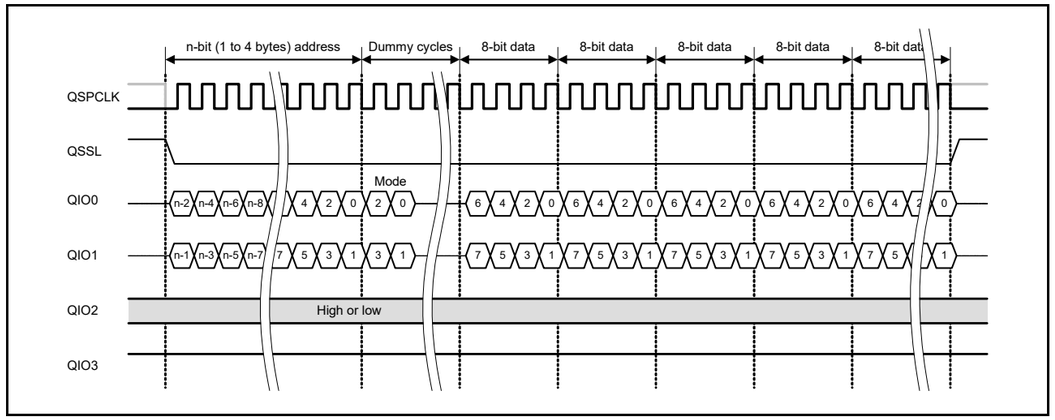


Figure 39.21 Fast Read Dual I/O bus cycle in XIP mode

Note: To use the Fast Read Dual I/O instruction, a serial flash device that supports Fast Read Dual I/O transfers is required.

39.6.6 Fast Read Quad Output Instruction

The Fast Read Quad Output instruction is a read instruction that uses four signal lines to receive data. When the SPI bus cycle starts, the serial flash select signal is asserted. The instruction code (6Bh/6Ch) and an address with a width of 1 to 4 bytes, specified in the SFMAS[1:0] bits in the SFMSAC register, are output from the QIO0 pin. Next, a certain number of dummy cycles, specified in the SFMDN[3:0] bits in the SFMSMD register, are generated. Data is then received through the QIO0, QIO1, QIO2, and QIO3 pins.

The first two dummy cycles are used to select or deselect the XIP mode. When the XIP mode is selected, the same instruction used this time is applied to the next SPI bus cycle, and the instruction code is not output the next SPI bus cycle. For details on the XIP mode, see section 39.8, XIP Control.

Switching to Fast Read Quad Output is controlled in the SFMSMD register.

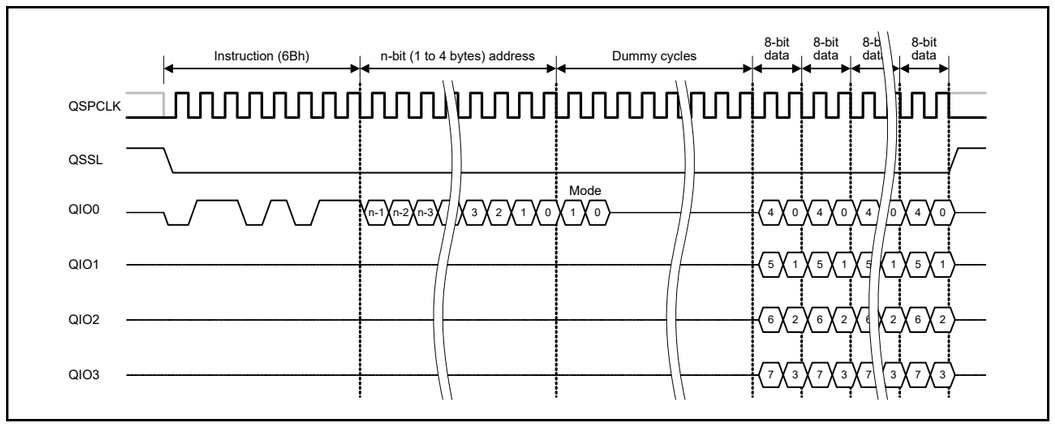


Figure 39.22 Fast Read Quad Output bus cycle

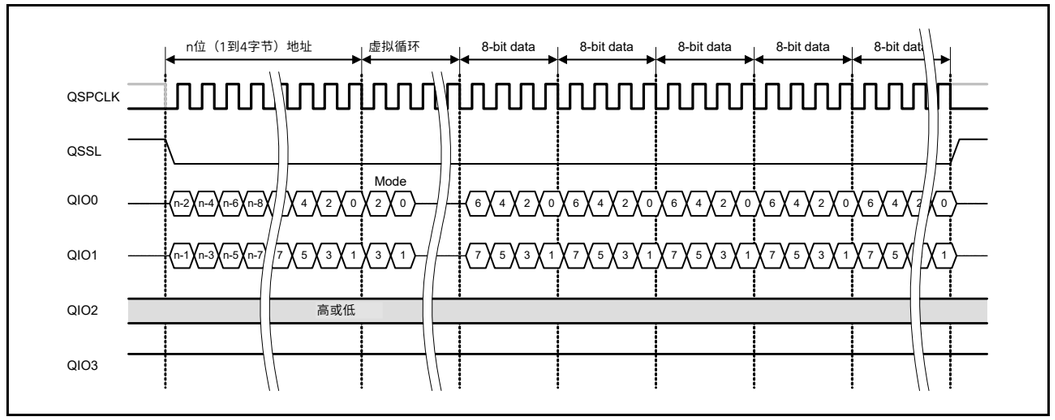


Figure 39.21 XIP模式下的快速读取双IO总线周期

Note: 要使用快速读取双IO指令，需要支持快速读取双IO传输的串行闪存设备。

39.6.6 快速读取四路输出指令

快速读取四路输出指令是使用四根信号线接收数据的读取指令。当SPI总线周期开始时，串行闪存选择信号被置位。指令代码(6Bh6Ch)和宽度为1到4字节的地址（在SFMSAC寄存器的SFMAS[1:0]位中指定）从QIO0引脚输出。接下来，生成一定数量的空周期，在SFMSMD寄存器的SFMDN[3:0]位中指定。然后通过QIO0、QIO1、QIO2和QIO3引脚接收数据。

前两个虚拟周期用于选择或取消选择XIP模式。选择XIP模式时，此时间使用的相同指令将应用于下一个SPI总线周期，并且指令代码未输出下一个SPIBUS周期。有关XIP模式的详细信息，请参阅第39.8节，XIP控制。

切换到快速读取四路输出由SFMSMD寄存器控制。

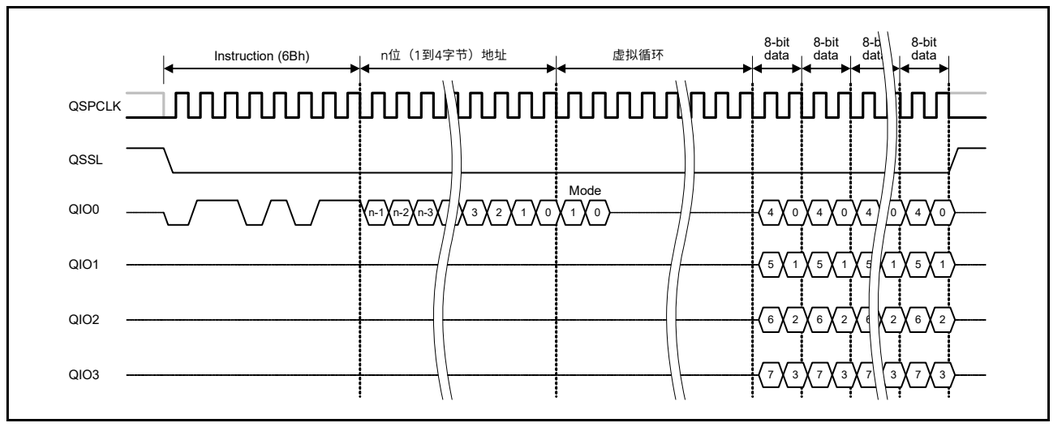


Figure 39.22 快速读取四路输出总线周期

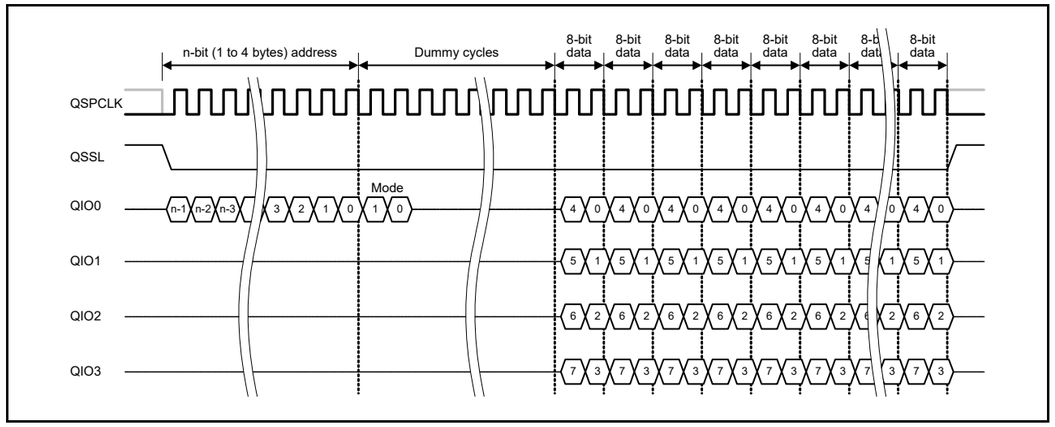


Figure 39.23 Fast Read Quad Output bus cycle in XIP mode

Note: To use Fast Read Quad Output, a serial flash that supports Fast Read Quad Output transfer is required.

39.6.7 Fast Read Quad I/O Instruction

The Fast Read Quad I/O instruction is a read instruction that uses four signal lines to transmit an address and receive data. When the SPI bus cycle starts, the serial flash select signal is asserted, and the instruction code (EBh/ECh) is output. Next, an address with a width of 1 to 4 bytes, specified in the SFMAS[1:0] bits in the SFMSAC register, is transmitted through the QIO0, QIO1, QIO2, and QIO3 pins, and a certain number of dummy cycles, specified in the SFMDN[3:0] bits in the SFMSMD register, is generated. Data is then received through the QIO0, QIO1, QIO2, and QIO3 pins.

The first two dummy cycles are used to select or deselect the XIP mode. When the XIP mode is selected, the same instruction used this time is applied to the next SPI bus cycle, and the instruction code is not output the next SPI bus cycle. For details on the XIP mode, see section 39.8, XIP Control.

Switching to Fast Read Quad I/O is controlled in the SFMSMD register.

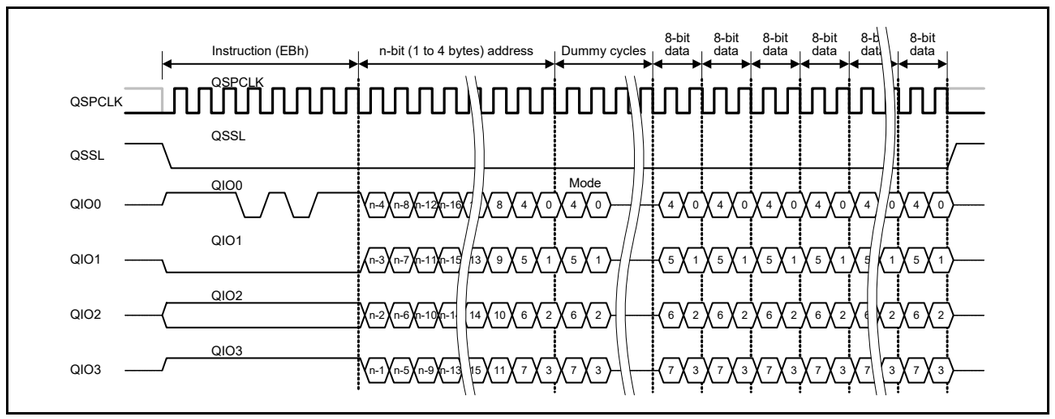


Figure 39.24 Fast Read Quad I/O bus cycle

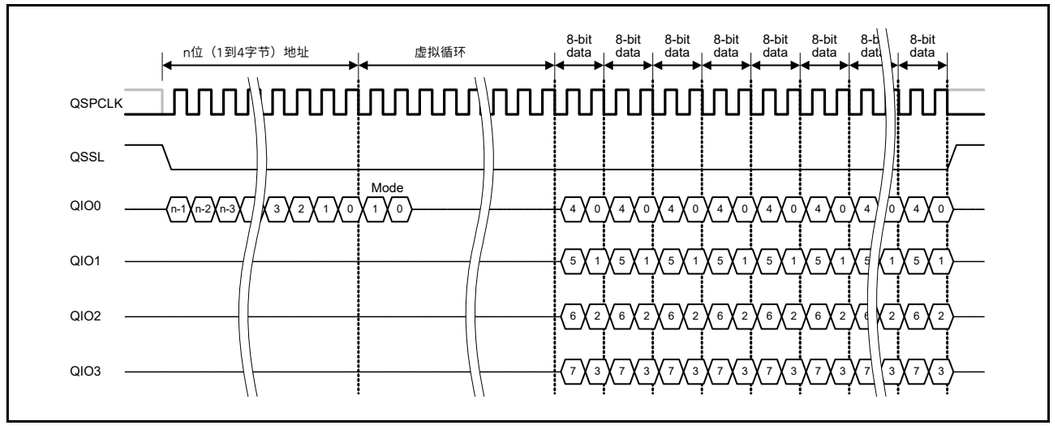


Figure 39.23 XIP模式下的快速读取四路输出总线周期

Note: 要使用快速读取四路输出，需要支持快速读取四路输出传输的串行闪存。

39.6.7 快速读取QuadIO指令

FastReadQuadIO指令是使用四根信号线传输地址和接收数据的读取指令。当SPI总线周期开始时，串行闪存选择信号被置位，并输出指令代码（EBhECh）。接下来，在SFMSAC寄存器的SFMAS[1:0]位中指定的1到4字节宽度的地址通过QIO0、QIO1、QIO2和QIO3引脚和一定数量的空周期传输，在SFMSMD寄存器的SFMDN[3:0]位中指定的，生成。然后通过QIO0、QIO1、QIO2和

QIO3 pins.

前两个虚拟周期用于选择或取消选择XIP模式。选择XIP模式时，此时间使用的相同指令将应用于下一个SPI总线周期，并且指令代码未输出下一个SPIBUS周期。有关XIP模式的详细信息，请参阅第39.8节，XIP控制。

切换到快速读取四线IO由SFMSMD寄存器控制。

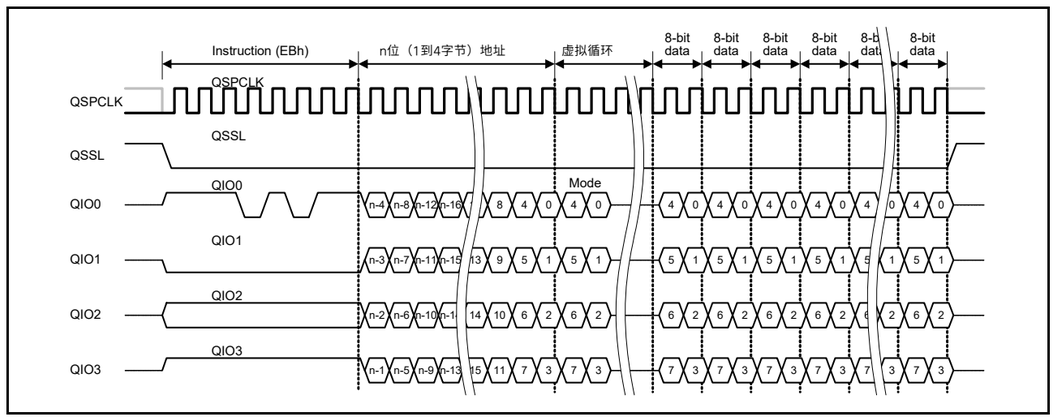


Figure 39.24 快速读取四IO总线周期

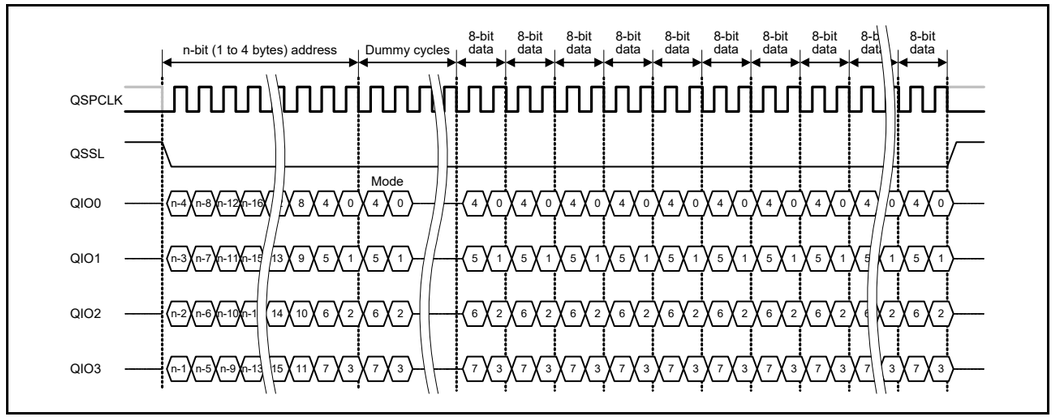


Figure 39.25 Fast Read Quad I/O bus cycle in XIP mode

Note: To use the Fast Read Quad I/O instruction, a serial flash device that supports Fast Read Quad I/O transfers is required.

39.6.8 Enter 4-Byte Mode Instruction

The Enter 4-Byte Mode instruction sets the serial flash address width to 4 bytes. When the SPI bus cycle starts, the serial flash select signal is asserted, and the instruction code (B7h) is output.

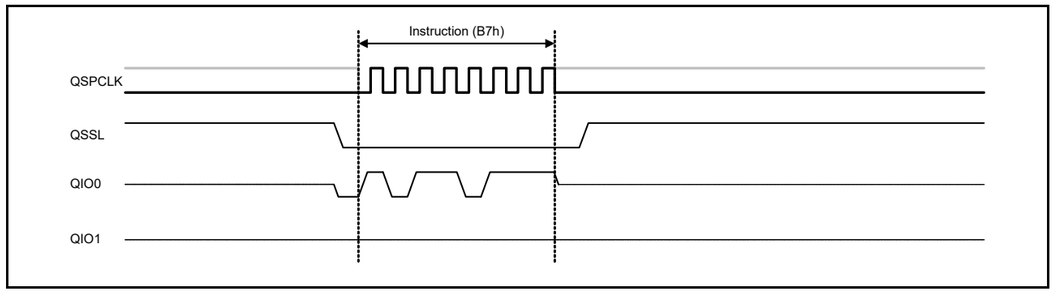


Figure 39.26 Enter 4-Byte Mode bus cycle

Note: The Enter 4-Byte Mode instruction is issued regardless of whether the serial flash is in 3- or 4-byte mode.

39.6.9 Exit 4-Byte Mode Instruction

The Exit 4-Byte Mode instruction sets the serial flash address width to 3 bytes. When the SPI bus cycle starts, the serial flash select signal is asserted, and the instruction code (E9h) is output.

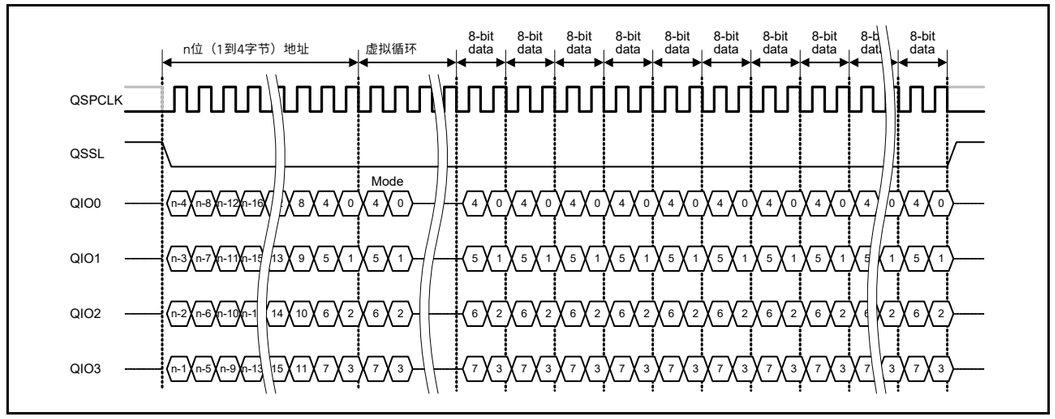


Figure 39.25 XIP模式下的快速读取QuadIO总线周期

Note: 要使用FastReadQuadIO指令，需要支持FastReadQuadIO传输的串行闪存设备。

39.6.8 进入4字节模式指令

进入4字节模式指令将串行闪存地址宽度设置为4字节。当SPI总线周期开始时，串行闪存选择信号被置位，并输出指令代码（B7h）。

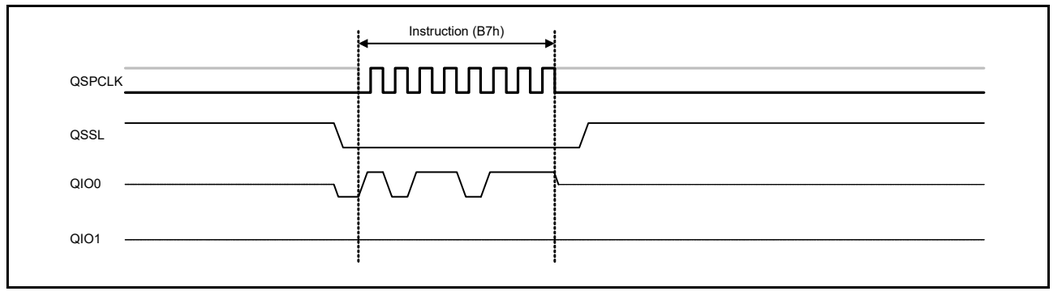


Figure 39.26 进入4字节模式总线周期

Note: 无论串行闪存是处于3字节模式还是4字节模式，都会发出进入4字节模式指令。

39.6.9 退出4字节模式指令

退出4字节模式指令将串行闪存地址宽度设置为3字节。当SPI总线周期开始时，串行闪存选择信号被置位，并输出指令代码（E9h）。

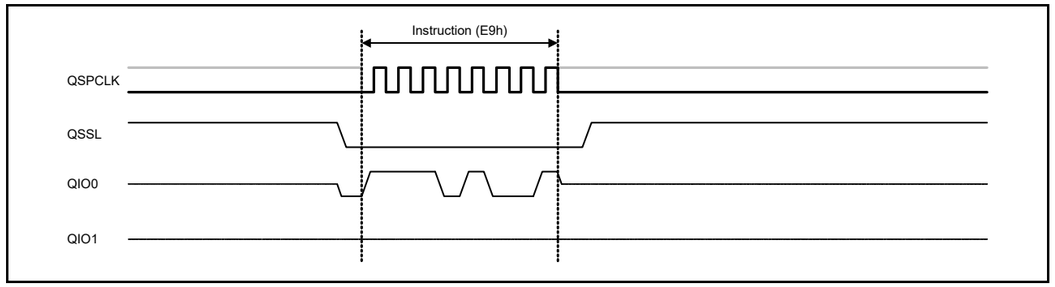


Figure 39.27 Exit 4-Byte Mode bus cycle

Note: The Exit 4-Byte Mode instruction is issued regardless of whether the serial flash is in 3- or 4-byte mode.

39.6.10 Write Enable Instruction

The Write Enable instruction enables changing of the serial flash address width. When the SPI bus cycle starts, the serial flash select signal is asserted, and the instruction code (06h) is output.

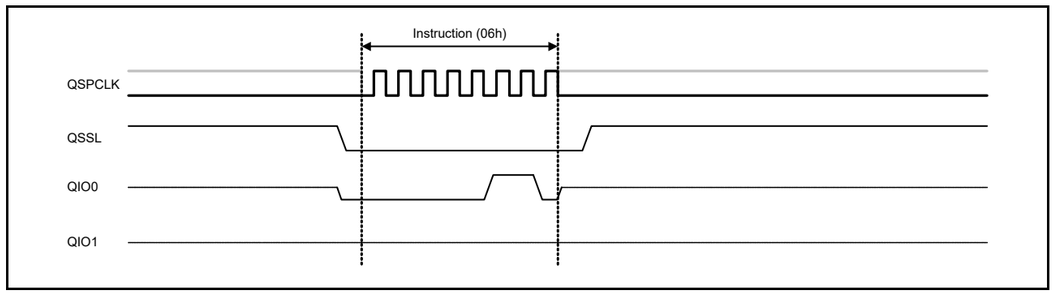


Figure 39.28 Write Enable bus cycle

39.7 SPI Bus Cycle Arrangement

39.7.1 Flash Read Based on Individual Conversion

ROM read internal bus cycles are individually converted to SPI bus cycles on a one-to-one basis. When a ROM read bus cycle is detected, the QSSL signal is asserted, and an SPI bus cycle starts. When data is received from the serial flash, the QSSL signal is deasserted, and the SPI bus cycle is complete.

When another ROM read bus cycle is detected, the QSSL signal is reasserted after ensuring the minimum high-level width of the QSSL signal is reached. Then another SPI bus cycle starts.

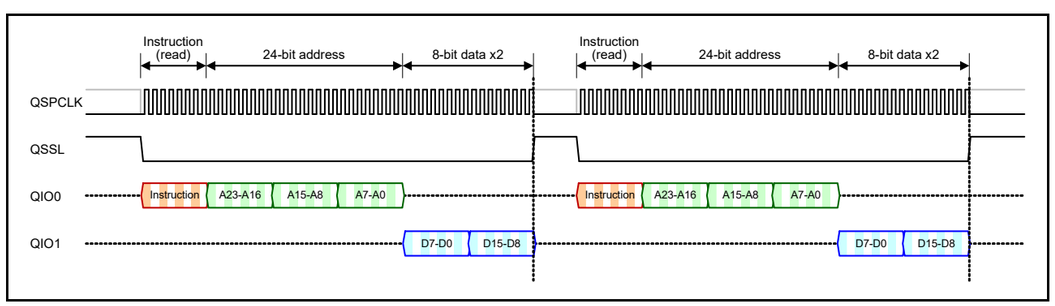


Figure 39.29 Successive data read operations based on individual conversion

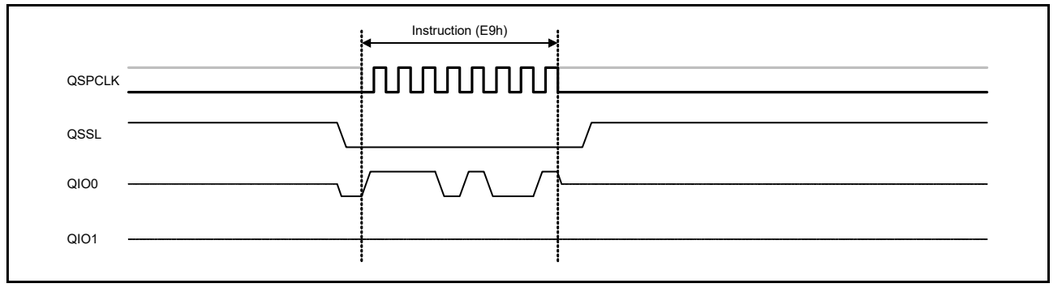


Figure 39.27 退出4字节模式总线周期

Note: 无论串行闪存是处于3字节模式还是4字节模式，都会发出退出4字节模式指令。

39.6.10 写使能指令

写使能指令可以改变串行闪存地址宽度。当SPI总线周期开始时，串行闪存选择信号被置位，并输出指令代码（06h）。

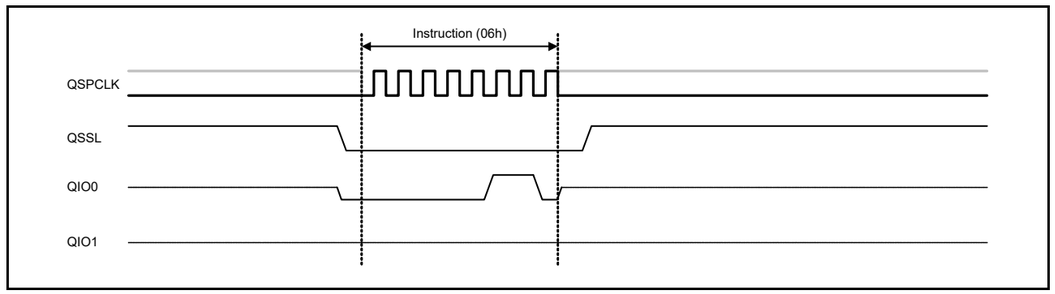


Figure 39.28 写使能总线周期

39.7 SPI总线周期安排

39.7.1 基于单个转换的闪存读取

ROM读取内部总线周期会以一对一的方式单独转换为SPI总线周期。当检测到ROM读取总线周期时，QSSL信号被置位，并且SPI总线周期开始。当从串行闪存接收到数据时，QSSL信号被置低，并且SPI总线周期完成。

当检测到另一个ROM读取总线周期时，在确保达到QSSL信号的最小高电平宽度后，重新置位QSSL信号。然后另一个SPI总线周期开始。

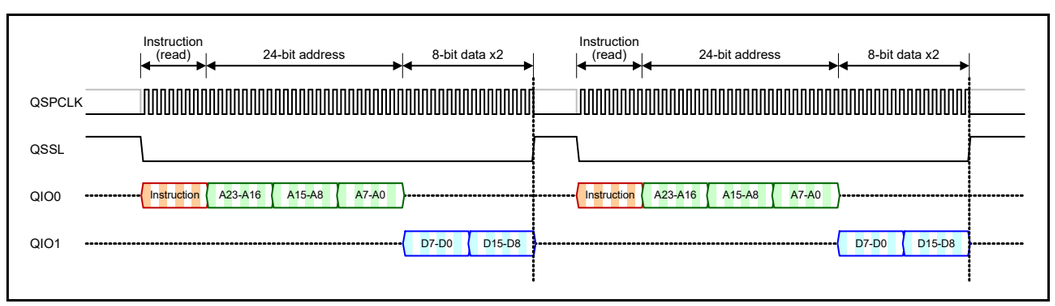


Figure 39.29 基于单独转换的连续数据读取操作

39.7.2 Flash Read Using the Prefetch Function

In operations such as CPU instruction execution and block data transfer, data is often read in ascending order from contiguous flash addresses. Serial flash provides the ability to repeat data reception without reissuing an instruction code and address. However, if bus cycles issued by the MCU are individually converted, SPI bus cycles are separated from each other, resulting in a failure to take advantage of this feature of serial flash. The QSPI contains a prefetch function to ensure the use of this capability.

To enable the prefetch function, set the SFMPFE bit in the SFMSMD register to 1. When the prefetch function is enabled, data is received continuously and stored in the buffer, without waiting for another flash read request. When the MCU performs a flash read operation, an address check is made. If an address match is confirmed, the data in the buffer is passed to the MCU. If an address mismatch is found, the data in the buffer is discarded, and a new SPI bus cycle is issued.

The buffer for prefetching is 18 bytes long. When this buffer is full, the SPI bus cycle is ended. When the buffer data is read to create free space, a new SPI bus cycle is automatically started to resume prefetching.

The prefetch function allows for efficient transfer operations when data is read in ascending order from contiguous addresses, as in instruction fetch and block data transfer.

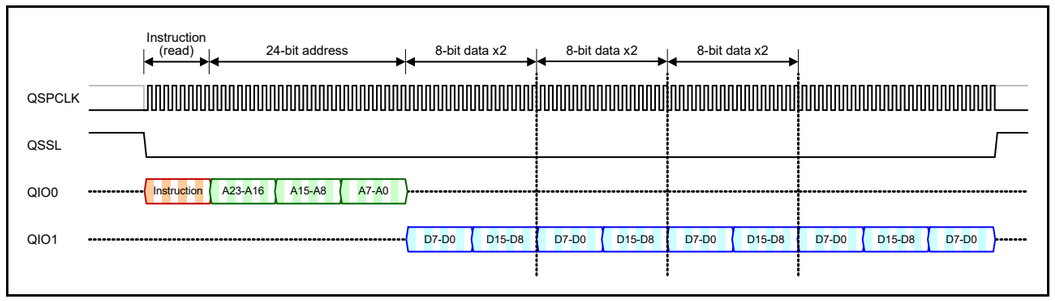


Figure 39.30 Successive data read operations using the prefetch function

39.7.3 Halt of Prefetching

If a ROM read bus cycle for reading from another address occurs during a serial transfer for prefetching, the unnecessary serial transfer being made is halted and a new SPI bus cycle is started. Usually, such a halt of serial transfer occurs on data reception byte boundaries. However, if the SFMPAE bit in the SFMSMD register is set to 1, the halt can occur on locations other than byte boundaries. To use this function, the serial flash device must support halts not on byte boundaries.

39.7.4 Direct Specification of Prefetch Destination

When the SFMPFE bit is set and the QSPI receives internal bus write access to the QSPI window area, the system obtains it as a prefetch address and starts to prefetch. Internal bus write access to the QSPI window area can only be used to obtain prefetch address data. Writes to serial flash cannot be performed.

Combining this function with the prefetch state polling function described in section 39, Prefetch State Polling, can reduce the load on the internal bus when data is read from a low-speed serial flash.

Note: When writing to the QSPI window area to indicate a prefetch destination, write to the first byte of the address where prefetching is to be started. Writes to the QSPI window area with a data size of 2 bytes or more return an ERROR response.

39.7.5 Prefetch State Polling

Reading data from a low-speed serial flash increases system load, because the internal bus enters a wait state until the SPI reception bus cycle is complete. The prefetch state polling function is provided to reduce this load.

The PFOFF bit in the SFMSST register indicates the state of the prefetch function, and the PFCNT[4:0] bits in the SFMSST register indicate the number of data bytes already prefetched. This allows the prefetch status to be determined

39.7.2 使用预取功能进行闪存读取

在CPU指令执行和块数据传输等操作中，通常会从连续的闪存地址以升序读取数据。串行闪存提供了重复数据接收而无需重新发出指令代码和地址的能力。但是，如果将MCU发出的总线周期单独转换，则SPI总线周期会相互分离，导致无法利用串行闪存的这一特性。QSPI包含一个预取功能以确保使用此功能。

要使能预取功能，请将SFMSMD寄存器中的SFMPFE位设置为1。当使能预取功能时，数据会连续接收并存储在缓冲区中，而无需等待另一个flash读取请求。当MCU执行闪存读取操作时，会进行地址检查。如果确认地址匹配，则将缓冲区中的数据传递给MCU。如果发现地址不匹配，则丢弃缓冲区中的数据，并发出新的SPI总线周期。

用于预取的缓冲区为18字节长。当此缓冲区满时，SPI总线周期结束。当缓冲区数据被读取以创建空闲空间时，会自动启动一个新的SPI总线周期以恢复预取。

当从连续地址以升序读取数据时，预取功能允许有效的传输操作，如在指令取指和块数据传输中。

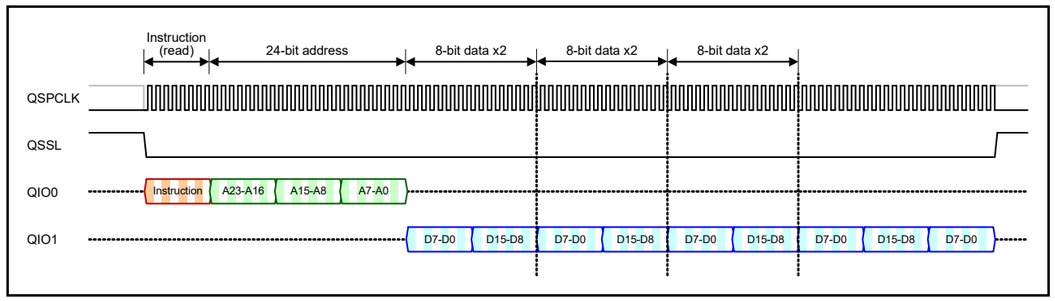


Figure 39.30 使用预取功能的连续数据读取操作

39.7.3 停止预取

如果在用于预取的串行传输期间发生用于从另一个地址读取的ROM读取总线周期，则停止进行的不必要的串行传输并开始新的SPI总线周期。通常，这种串行传输的停止发生在数据接收字节边界上。但是，如果SFMSMD寄存器中的SFMPAE位设置为1，则停止可能发生在字节边界以外的位置。要使用此功能，串行闪存设备必须支持不在字节边界上的暂停。

39.7.4 直接指定预取目的地

当SFMPFE位置位并且QSPI接收到对QSPI窗口区域的内部总线写访问时，系统将其作为预取地址并开始预取。对QSPI窗口区域的内部总线写访问只能用于获取预取地址数据。无法执行对串行闪存的写入。

将此功能与第39节“预取状态轮询”中描述的预取状态轮询功能相结合，可以在从低速串行闪存读取数据时减少内部总线的负载。

Note: 当写入QSPI窗口区域以指示预取目标时，写入要开始预取的地址的第一个字节。写入数据大小为2字节或更多字节的QSPI窗口区域会返回ERROR响应。

39.7.5 预取状态轮询

从低速串行闪存读取数据会增加系统负载，因为内部总线进入等待状态，直到SPI接收总线周期完成。提供了预取状态轮询功能来减少这种负载。

SFMSST寄存器中的PFOFF位指示预取功能的状态，而寄存器中的PFCNT[4:0]位指示预取功能的状态。SFMSST寄存器指示已经预取的数据字节数。这允许确定预取状态

with a single CPU operation.

```
//
// copy 1K byte (32bit x 256 word) data from serial flash to SDRAM
//
unsigned long *sptr;                    // pointer for the serial flash
unsigned long *dptr;                    // pointer for the SDRAM
int i;

SFMSMD |= 0x0040;                       // set SFMPFE bit to enable prefetch
*( (volatile unsigned char *) sptr ) = 0;    // make the TAG valid to start prefetch

for ( i = 0 ; i < 256 ; i++ ){
while ( ( SFMSST & 0x00FF ) < 0x04 ){};   // waiting for 4-byte data to be received
*(dptr++) = *(sptr++);
}
```

Note: When executing a polling program, place the program outside of the serial flash or enable the instruction cache. If the polling program is executed when the program is on the serial flash or is executed without using the instruction cache, the prefetch target frequently switches to an instruction code. This eliminates the effect of polling, and an infinite loop can result because the prefetch buffer is not filled.

39.7.6 Flash Read Using the SPI Bus Cycle Extension Function

If the SFMSE[1:0] bits in the SFMSMD register are set to a value other than 00b, the QSPI waits for next flash read, suspending the SPI bus cycle, while stopping the QSPCLK signal and holding the QSSL signal low even after data is obtained from the serial flash.

If the address of the next flash read is contiguous in ascending order, the toggling of the QSPCLK signal is restarted to continue reception of subsequent data. If the address of the next flash read is not contiguous in ascending order, the QSSL signal is driven high once to end the SPI bus cycle being suspended. A new SPI bus cycle is then started.

When data is read intermittently from ascending order contiguous addresses, this function enables an efficient transfer operation to be performed by reducing the overhead for instruction code and address transmission.

The SPI bus cycle extension time is selectable in the SFMSE[1:0] bits in the SFMSMD register. When the specified extension time elapses, the QSSL signal returns to the high level to automatically end the SPI bus cycle being suspended. If the SFMSE[1:0] bits are set to 11b, QSSL is extended infinitely. This increases the power consumption of the serial flash, so the system must be designed accordingly.

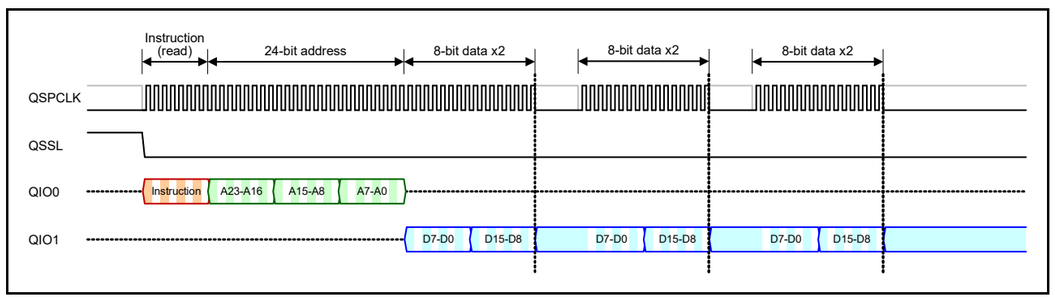


Figure 39.31 Successive data read operations using the SPI bus cycle extension

39.8 XIP Control

Some serial flash devices allow latencies to be reduced by skipping instruction code reception for flash reads. This instruction code skip function is selected in mode data received during the dummy cycle period of the previous serial bus cycle.

In the dummy cycle of the Fast Read instructions, the QSPI controls the XIP mode of the serial flash by using the serial data signal to send the mode data set in the SFMXD[7:0] bits in the SFMSDC register during the first 2 cycles, as shown

单CPU操作。

```
将1K字节（32位x256字）数据从      串行闪存复制到SDRAM

无符号长*sptr;串行闪存指针unsignedlong*dptr;SDRAMinti的指
针;



SFMSMD=0x0040；设置SFMPFE位以启用预取*((volatileunsignedchar*)sptr)=
0;使TAG有效以开始预取

for(i=0;i<256;i++){而((SFMSST&0x00FF)<0x04){ ;等待接收4字节数据*(dptr++)=*(s
ptr++);

}
```

Note: 执行轮询程序时，将程序置于串行闪存之外或启用指令缓存。
如果轮询程序在程序在串行闪存上时执行或在不使用指令缓存的情况下执行，则预取目标频繁切换到指令代码。这消除了轮询的影响，并且由于未填充预取缓冲区可能导致无限循环。

39.7.6 使用SPI总线周期扩展功能读取Flash

如果SFMSMD寄存器中的SFMSE[1:0]位设置为00b以外的值，则QSPI等待下一次闪存读取，暂停SPI总线周期，同时停止QSPCLK信号并将QSSL信号保持在低电平，即使在数据之后是从串行闪存中获得的。

如果下一次闪存读取的地址按升序连续，则重新启动QSPCLK信号的翻转以继续接收后续数据。如果下一次flash读取的地址升序不连续，则QSSL信号被驱动一次高电平以结束暂停的SPI总线周期。然后开始一个新的SPI总线周期。

当从升序连续地址间歇性地读取数据时，该功能通过减少指令代码和地址传输的开销来实现高效的传输操作。

SPI总线周期延长时间可在SFMSMD寄存器的SFMSE[1:0]位中选择。当指定的延长时间过去后，QSSL信号返回高电平，自动结束暂停的SPI总线周期。如果SFMSE[1:0]位设置为11b，QSSL将无限扩展。这增加了串行闪存的功耗，因此必须对系统进行相应的设计。

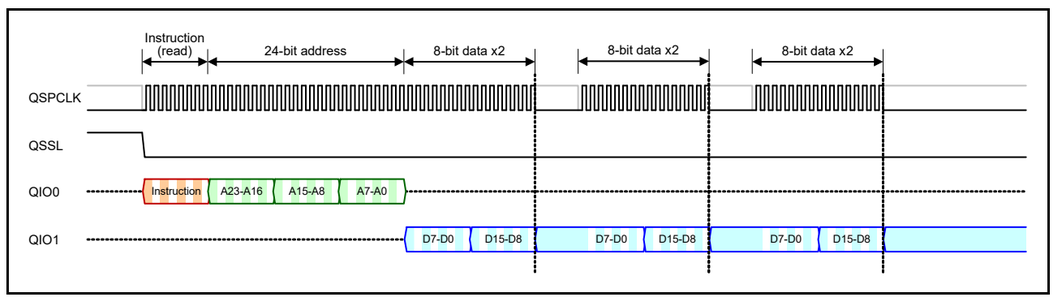


Figure 39.31 使用SPI总线周期扩展的连续数据读取操作

39.8 XIP Control

一些串行闪存设备允许通过跳过闪存读取的指令代码接收来减少延迟。在前一个串行总线周期的虚拟周期期间接收到的模式数据中选择此指令代码跳过功能。

在快速读取指令的空周期内，QSPI在前2个周期内通过串行数据信号发送SFMSDC寄存器的SFMXD[7:0]位中设置的模式数据来控制串行闪存的XIP模式，如图所示

in Figure 39.32.

The mode data to enable the XIP mode differs for each serial flash. Accordingly, set the appropriate mode data in the SFMXD[7:0] bits.

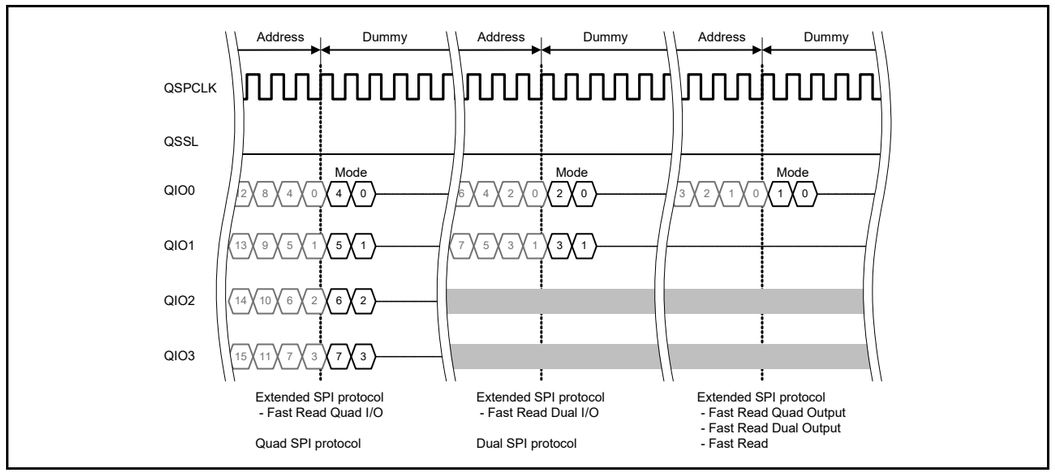


Figure 39.32 XIP mode control data

39.8.1 Selecting the XIP Mode

To select the XIP mode, specify the XIP mode configuration for the serial flash device in the SFMXD[7:0] bits in the SFMSDC register, and set the SFMXEN bit to 1. In the dummy cycle of the next Fast Read instruction, the mode data specified in the SFMXD[7:0] bits is transferred to the serial flash device. From that point, the XIP mode is enabled in both the serial flash controller and the serial flash device. To confirm completion of the XIP mode select procedure, read 1 from the SFMXST bit in the SFMSDC register.

Note: Set the SFMXD[7:0] bits in the SFMSDC register to the XIP mode setting data specified for the actual serial flash device. The XIP mode of the serial flash controller is only enabled in the SFMXEN bit, regardless of the SFMXD[7:0] setting in the SFMSDC register.

39.8.2 Releasing the XIP Mode

To release the XIP mode, specify the release configuration for the serial flash in the SFMXD[7:0] bits in the SFMSDC register, and clear the SFMXEN bit to 0. In the dummy cycle of the next Fast Read instruction, the mode data specified in the SFMXD[7:0] bits is transferred to the serial flash during the first two-cycle period. From that point, the XIP mode is disabled in both the QSPI and the serial flash device. To confirm completion of the XIP mode release procedure, read 0 from the SFMXST bit in the SFMSDC register

Note: Set the SFMXD[7:0] bits in the SFMSDC register to the XIP mode setting data specified for the actual serial flash device. The XIP mode of the serial flash controller is only disabled in the SFMXEN bit, regardless of the SFMXD[7:0] setting in the SFMSDC register.

39.9 QIO2 and QIO3 Pin States

The QIO2 and QIO3 pin states depend on the serial interface read mode specified in the SFMRM[2:0] bits in the SFMSMD register.

在图39.32中。

启用XIP模式的模式数据因串行闪存而异。因此，在
SFMXD[7:0] bits.

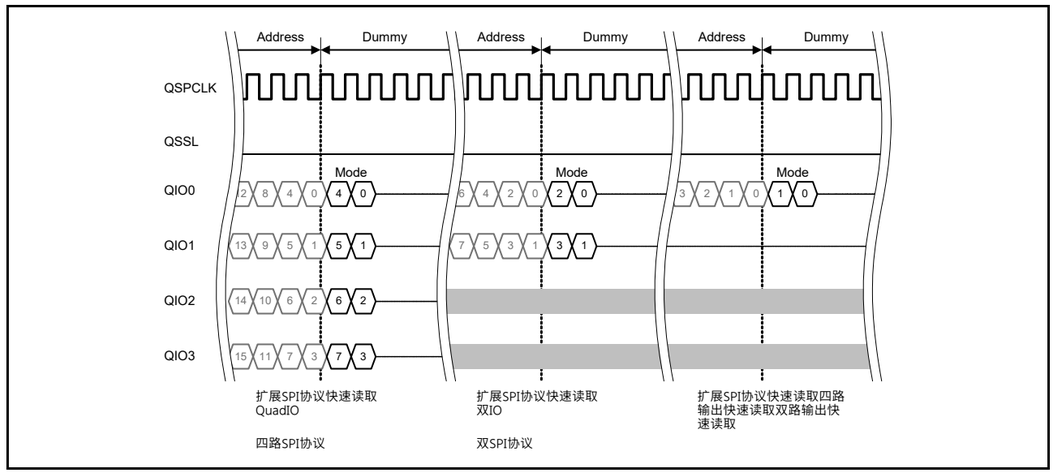


Figure 39.32 XIP模式控制数据

39.8.1 选择XIP模式

要选择XIP模式，请在SFMSDC寄存器的SFMXD[7:0]位中指定串行闪存设备的XIP模式配置，并将SFMXEN位设置为1。在下一条快速读取指令的空周期中，SFMXD[7:0]位中指定的模式数据被传输到串行闪存设备。从那时起，串行闪存控制器和串行闪存设备都启用了XIP模式。要确认XIP模式选择过程的完成，请从SFMSDC寄存器中的SFMXST位读取1。

Note: 将SFMSDC寄存器中的SFMXD[7:0]位设置为为实际串行闪存设备指定的XIP模式设置数据。串行闪存控制器的XIP模式仅在SFMXEN位中启用，与SFMSDC寄存器中的SFMXD[7:0]设置无关。

39.8.2 释放XIP模式

要释放XIP模式，请在SFMSDC寄存器的SFMXD[7:0]位中指定串行闪存的释放配置，并将SFMXEN位清除为0。在下一条快速读取指令的空周期中，模式数据在前两个周期期间，SFMXD[7:0]位中指定的数据被传输到串行闪存。从那时起，XIP模式在QSPI和串行闪存设备中都被禁用。要确认XIP模式释放过程完成，请从SFMSDC寄存器中的SFMXST位读取0

Note: 将SFMSDC寄存器中的SFMXD[7:0]位设置为为实际串行闪存设备指定的XIP模式设置数据。串行闪存控制器的XIP模式仅在SFMXEN位中被禁用，而与SFMSDC寄存器中的SFMXD[7:0]设置无关。

39.9 QIO2和QIO3引脚状态

QIO2和QIO3引脚状态取决于在SFMRM[2:0]位中指定的串行接口读取模式
SFMSMD register.

Table 39.9 QIO2 and QIO3 pin states

SFMSMD.SFMRM[2:0] bits	QIO2 pin state*1	QIO3 pin state*2	Remarks
111	Setting prohibited		
110			
101	Input or output as a serial data signal (standby level is Hi-Z)	Input or output as serial data signal (standby level is Hi-Z)	Fast Read Quad I/O
100			Fast Read Quad Output
011	Output SFMWPL bit variable of SFMPMD register (initial output variable is low level)	Output high level	Fast Read Dual I/O
010			Fast Read Dual Output
001			Fast Read
000			Read (Initial State)

Note 1. The serial flash can also use the QIO2 pin for the WP function.
Note 2. The serial flash can also use the QIO3 pin for the HOLD or RESET function.

39.10 Direct Communication Mode

39.10.1 About Direct Communication

The QSPI can read the serial flash contents by automatically converting a ROM read bus cycle to an SPI bus cycle. However, serial flash devices have many different functions in addition to memory data read, including ID information read, erase, programming, and status information read. There is no standardized instruction set for using these functions, and more functions are being added rapidly by different vendors to different devices. It is difficult to support these functions by hardware control.

The QSPI flexibly supports these serial flash devices by providing a means for the software to directly communicate with the serial flash, so that the software can create any SPI bus cycle required.

39.10.2 Using Direct Communication Mode

To communicate directly with serial flash, transition to direct communication mode by setting the DCOM bit in the SFMCMD register to 1. While direct communication mode is selected, ordinary flash read operation is disabled. For ordinary flash access after direct communication, terminate direct communication mode by setting the DCOM bit in the SFMCMD register to 0.

Note: If the QSPI is set to the XIP mode, you must terminate the XIP mode before starting direct communication mode.

39.10.3 Generating the SPI Bus Cycle during Direct Communication

The SPI bus cycle in direct communication starts on the first access to the SFMCOM port and ends with a write to the SFMCMD register, after a series of I/O operations is performed through the SFMCOM port. At that point, a write to the SFMCOM port is converted to a one-byte transmission to the SPI bus, and a read from the SFMCOM port is converted to a one-byte reception from the SPI bus.

During the period from the first access to the SFMCOM port to the last write operation to the SFMCMD register, the serial flash select signal is held active to notify the serial flash that a series of SPI bus cycles is in progress.

Note: In direct communication mode, all writes to registers other than SFMCMD and SFMCOM (including SFMSMD, SFMSSC, SFMSKC, SFMSST, SFMCST, SFMSIC, SFMSAC, SFMSDC, SFMSPC, and SFMPMD) are disabled, and setting value are invalid. With this circuit configuration, writing to a register area other than the SFMCOM port terminates the SPI bus cycle. However, do not write to a register area other than SFMCMD as a way to terminate the SPI bus cycle. This operation is not guaranteed as a normal function.

The following is an example program for direct communication.

Table 39.9 QIO2和QIO3引脚状态

SFMSMD.SFMRM[2:0] bits	QIO2引脚状态*1	QIO3引脚状态*2	Remarks
111	禁止设定		
110			
101	作为串行数据信号输入或输出（待机电平为Hi-Z）	作为串行数据信号输入或输出（待机电平为Hi-Z）	快速读取四路IO
100			快速读取四路输出
011	输出SFMPMD寄存器的SFMWPL位变量（初始输出变量为低电平）	输出高电平	快速读取双IO
010			快速读取双输出
001			快速阅读
000			Read (Initial State)

Note 1. 串行闪存也可以将QIO2引脚用于WP功能。
Note 2. 串行闪存也可以将QIO3引脚用于HOLD或RESET功能。

39.10 直接通讯方式

39.10.1 关于直接沟通

QSPI可以通过自动将ROM读取总线周期转换为SPI总线周期来读取串行闪存内容。
然而，串行闪存设备除了读取存储器数据外，还有许多不同的功能，包括ID信息读取、擦除、编程和状态信息读取。使用这些功能没有标准化的指令集，更多的功能正在由不同的供应商迅速添加到不同的设备中。很难通过硬件控制来支持这些功能。

QSPI通过为软件提供一种直接与串行闪存通信的方法来灵活地支持这些串行闪存设备，以便软件可以创建所需的任何SPI总线周期。

39.10.2 使用直接通信模式

要与串行闪存直接通信，通过将SFMCMD寄存器中的DCOM位设置为1转换到直接通信模式。选择直接通信模式时，普通闪存读取操作被禁用。对于直接通信后的普通闪存访问，通过将SFMCMD寄存器中的DCOM位设置为0来终止直接通信模式。

Note: 如果QSPI设置为XIP模式，则必须在启动直接通信模式之前终止XIP模式。

39.10.3 在直接通信期间生成SPI总线周期

直接通信中的SPI总线周期从第一次访问SFMCOM端口开始，并以对SFMCOM端口的写入结束。
SFMCMD寄存器，通过SFMCOM端口进行一系列IO操作后。此时，对SFMCOM端口的写入将转换为向SPI总线发送的一字节，从SFMCOM端口读取的数据将转换为从SPI总线接收的一字节。

在从第一次访问SFMCOM端口到最后一次对SFMCMD寄存器的写操作期间，串行闪存选择信号保持有效，以通知串行闪存一系列SPI总线周期正在进行中。

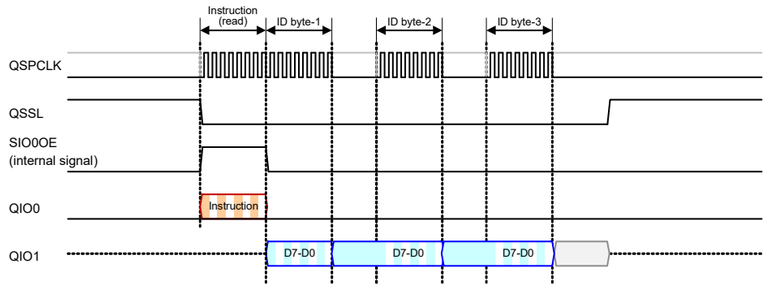
Note: 在直接通信模式下，所有写入除SFMCMD和SFMCOM以外的寄存器（包括SFMSMD、SFMSSC SFMSKC SFMSST SFMCST SFMSIC SFMSAC SFMSDC SFMSPC SFMPMD)无效，设定值无效。使用这种电路配置，写入SFMCOM端口以外的寄存器区域会终止SPI总线周期。但是，不要将写入SFMCMD以外的寄存器区域作为终止SPI总线周期的方法。此操作不能保证为正常功能。

以下是直接通信的示例程序。

```
//### CAUTION! ### This code must be outside the serial flash that is going to be controlled.

// Define specific instruction codes of the target serial flash device.
#define  Instruction_FREAD  0x0B // Fast Read
#define  Instruction_RDSR   0x05 // Read Status register
#define  Instruction_RDID   0x9F // Read Identification
#define  Instruction_WREN   0x06 // Write Enable
#define  Instruction_CERA   0xC7 // Chip Erase

unsigned char  mfid, mtype, mcap, data, temp;

SFMCMD = 0x01; // Enable direct operation

// Get the device identification assigned by JEDEC.
SFMCOM = Instruction_RDID; // put “Read Identification” instruction (open SPI bus cycle)
mfid   = (unsigned char) SFMCOM; // get “Manufacturer Identification”
mtype  = (unsigned char) SFMCOM; // get “Memory Type”
mcap   = (unsigned char) SFMCOM; // get “Memory Capacity”
SFMCMD = 0x01h; // close SPI bus cycle

// Get one byte from the address 0x012345h.
SFMCOM = Instruction_FREAD; // put “Fast Read” instruction (open SPI bus cycle)
SFMCOM = 0x01; // put upper byte of the address 0x012345
SFMCOM = 0x23; // put middle byte of the target address 0x012345
SFMCOM = 0x45; // put lower byte of the target address 0x012345
temp   = (unsigned char) SFMCOM; // get one byte dummy code for FAST READ transaction
data   = (unsigned char) SFMCOM; // get the data
SFMCMD = 0x01; // close SPI bus cycle

// Erase All contents.
SFMCOM = Instruction_WREN; // put “Write Enable” instruction (open SPI bus cycle)
SFMCMD = 0x01; // close SPI bus cycle
SFMCOM = Instruction_CERA; // put “Chip Erase” instruction (open SPI bus cycle)
SFMCMD = 0x01; // close SPI bus cycle
SFMCOM = Instruction_RDSR; // put “Read Status Register” instruction (open SPI bus cycle)
while (SFMCOM & 0x01){}; // Polling “Write Progress Bit” until completion
SFMCMD = 0x01; // close SPI bus cycle

SFMCMD = 0x00; // Disable direct operation
```



```
###注意！###此代码必须在要控制的串行闪存之外。

定义目标串行闪存设备的具体指令代码。#defineInstruction_FREA
D0x0B快速读取#defineInstruction_RDSR0x05读取状态寄存器#de
fineInstruction_RDID0x9F读取标识#defineInstruction_WREN0x06
写使能#defineInstruction_CERA0xC7芯片擦除



无符号字符mfid、mtype、mcap、数据、温度；

SFMCMD=0x01；启用直接操作

获取JEDEC分配的设备标识。SFMCOM=指令_RDID；放“读取标识”指令（打开SPI总线周期
）mfid=(unsignedchar)SFMCOM；获取“制造商标识”mtype=(unsignedchar)SFMCOM;获取“
内存类型”mcap=(unsignedchar)SFMCOM;获得“内存容量”SFMCMD=0x01h；关闭SPI总线
周期



从地址0x012345h获取一个字节。SFMCOM=指令_FREAD；放“快速读取”指令（打
开SPI总线周期）
SFMCOM=0x01；把地址的高字节0x012345
SFMCOM=0x23；把目标地址的中间字节0x012345SFMCOM=0x45;把目标地址的低字节0x01
2345temp=(unsignedchar)SFMCOM;获取FASTREAD交易数据的一字节虚拟代码=(unsignedch
ar)SFMCOM;获取数据SFMCMD=0x01;关闭SPI总线周期



删除所有内容。SFMCOM=指令_WREN；放“写使能”指令（打开SPI总线周期）

SFMCMD=0x01；关闭SPI总线周期SFMCOM=Instruction_CERA;放“芯片擦除”指令（
打开SPI总线周期）
SFMCMD=0x01；关闭SPI总线周期
SFMCOM=指令_RDSR；将“读取状态寄存器”指令（打开SPI总线周期）while(SFMCOM&0x01){
;轮询”写进度位”直到完成SFMCMD=0x01;关闭SPI总线周期



SFMCMD=0x00；禁用直接操作
```




```
(1) SFMCMD = 01h;                  // Enable direct operation
                                   // Get the device identification assigned by JEDEC
(2) SFMCOM = Instruction_RDID;     // Put “Read Identification” instruction (open the transaction)
(3) mfid = (unsigned char) SFMCOM; // Get ID byte-1 “Manufacturer Identification”
(4) mtype = (unsigned char)
    SFMCOM;                        // Get ID byte-2 “Memory Type”
(5) mcap = (unsigned char) SFMCOM; // Get ID byte-3 “Memory Capacity”
(6) SFMCMD = 01h;                  // Close the transaction
(7) SFMCMD = 00h;                  // Disable direct operation
```

Figure 39.33 Example of direct communication timing for ID read

Note: When Extended SPI protocol is used in direct communication mode, the standard Read or Fast Read instruction must be used to reference the contents of the serial flash. The QSPI does not support Fast Read Dual Output, Fast Read Dual I/O, Fast Read Quad Output, or Fast Read Quad I/O transfers in this configuration. When these high-speed read operations are required, use ordinary flash access.

39.11 Operation

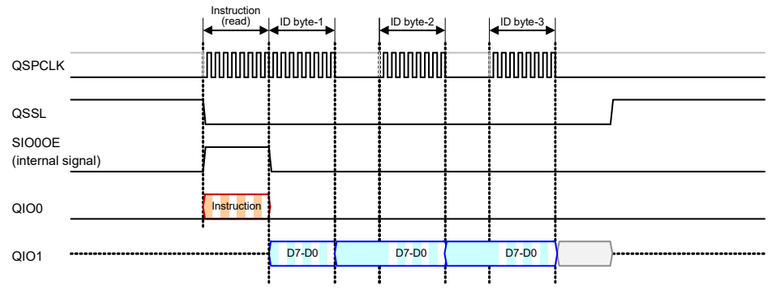
39.11.1 Procedure for Changing Settings in Multiple Control Registers

The settings of the QSPI control registers can be changed dynamically during system operation. However, when the settings of multiple control registers are changed sequentially, an SPI bus cycle might occur before all of the registers are updated. The register setting sequence must be carefully designed so that the SPI bus timing specification is satisfied at all stages of register setting changes.

```
//
// Making QSPCLK faster
//
SFMSMD = 0x0041; // SFMPAE: 0 SFMPFE: 1 SFMSE:00 SFMRM:01 (prefetch enable fast read)
SFMSSC = 0x04; // SFMSLD: 0 SFMSHD: 0 SFMSW:4 (minimum QSSL high width = 5 sck)
SFMSKC = 0x00; // SFMDTY: 0 SFMDV: 0 (1/2 mode)  ### switch clock speed last ###

//
// Making QSPCLK slower
//
SFMSKC = 0x06; // SFMDTY: 0 SFMDV:6 (1/8 mode)  ### switch clock speed first ###
SFMSSC = 0x01; // SFMSLD: 0 SFMSHD:0 SFMSW: 1 (minimum QSSL high width = 2 sck)
SFMSMD = 0x0040; // SFMPAE: 0 SFMPFE:1 SFMSE: 00 SFMRM:00 (prefetch enable, standard read)
```

39.12 Interrupts

When the EROMR bit in the SFMCST register sets to 1, the QSPI requests an interrupt. The EROMR bit sets to 1 when a ROM read access is detected in direct communication mode. Interrupt requests are retained until the EROMR bit is cleared by a 0 write. For details, see section 14, Interrupt Controller Unit (ICU).




```
(1) SFMCMD = 01h;                  Enabledirectoperation获取JEDEC分配的设备标识
(2) SFMCOM = Instruction_RDID;     输入“读取标识”指令（打开交易）
(3) mfid = (unsigned char) SFMCOM; 获取IDbyte-1“制造商标识”
(4) mtype = (unsigned char)
    SFMCOM;                        获取IDbyte-2“内存类型”
(5) mcap = (unsigned char) SFMCOM; 获取IDbyte-3“内存容量”
(6) SFMCMD = 01h;                  关闭交易
(7) SFMCMD = 00h;                  禁用直接操作
```

Figure 39.33 ID读取的直接通信时序示例

Note: 在直接通信模式下使用扩展SPI协议时，必须使用标准读取或快速读取指令来引用串行闪存的内容。在此配置中，QSPI不支持快速读取双输出、快速读取双IO、快速读取四输出或快速读取四IO传输。当需要这些高速读取操作时，请使用普通闪存访问。

39.11 Operation

39.11.1 更改多个控制寄存器中的设置的步骤

QSPI控制寄存器的设置可以在系统运行期间动态更改。但是，当多个控制寄存器的设置依次更改时，可能会在所有寄存器更新之前发生一个SPI总线周期。必须仔细设计寄存器设置顺序，以便在寄存器设置更改的所有阶段都满足SPI总线时序规范。

```
使QSPCLK更快SFMSMD=0x0041;SFMPAE:0SFMPFE:1SFMSE:00SFMRM:01（预取使能快速读取）



SFMSSC=0x04；SFMSLD：0SFMSHD：0SFMSW：4（最小QSSL高宽度=5sck）
SFMSKC=0x00；SFMDTY:0SFMDV:0(12模式)###最后切换时钟速度###

使QSPCLK变慢SFMSKC=0x06;SFMDTY:0SFMDV:6(18模式)###先切换时钟速度###



SFMSSC=0x01；SFMSLD：0SFMSHD：0SFMSW：1（最小QSSL高宽度=2sck）
SFMSMD=0x0040；SFMPAE:0SFMPFE:1SFMSE:00SFMRM:00（预取使能，标准读取）
```

39.12 Interrupts

当SFMCST寄存器中的EROMR位设置为1时，QSPI请求中断。当在直接通信模式下检测到ROM读访问时，EROMR位设置为1。中断请求被保留，直到EROMR位被0写入清除。有关详细信息，请参阅第14节，中断控制器单元(ICU)。

39.13 Usage Notes

39.13.1 Settings for the Module-Stop Function

QSPI operation can be disabled or enabled using Module Stop Control Register B (MSTPCRB). The QSPI is initially stopped after reset. Releasing the module-stop state enables access to the registers. For details, see section 11, Low Power Modes.

39.13 使用说明

39.13.1 模块停止功能的设置

可以使用模块停止控制寄存器B(MSTPCRB)禁用或启用QSPI操作。QSPI在复位后最初停止。释放模块停止状态可以访问寄存器。有关详细信息，请参阅第11节，低功耗模式。

40. Cyclic Redundancy Check (CRC) Calculator

40.1 Overview

The Cyclic Redundancy Check (CRC) calculator generates CRC codes to detect errors in the data. The bit order of CRC calculation results can be switched for LSB- or MSB-first communication. Additionally, various CRC generation polynomials are available for your application. The snoop function allows monitoring of reads from and writes to specific addresses. This function is useful in applications that require CRC code to be generated automatically in certain events, such as monitoring writes to the serial transmit buffer and reads from the serial receive buffer.

Table 40.1 lists the CRC calculator specifications and Figure 40.1 shows a block diagram.

Table 40.1 CRC calculator specifications

Parameter	Specifications for 8-bit data	Specifications for 32-bit data
Data size	8-bit	32-bit
Data for CRC calculation*1	CRC code generated for data in 8n-bit units (where n is a whole number)	CRC code generated for data in 32n-bit units (where n is a whole number)
CRC processor unit	Operation executed on 8 bits in parallel	Operation executed on 32 bits in parallel
CRC generating polynomial	One of three generating polynomials selectable [8-bit CRC] • $X^8 + X^2 + X + 1$ (CRC-8) [16-bit CRC] • $X^{16} + X^{15} + X^2 + 1$ (CRC-16) • $X^{16} + X^{12} + X^5 + 1$ (CRC-CCITT)	One of two generating polynomials selectable [32-bit CRC] • $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$ (CRC-32) • $X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$ (CRC-32C)
CRC calculation switching	The bit order of CRC calculation results can be switched for LSB- or MSB-first communication	
Module-stop function	Module-stop state can be set to reduce power consumption	
CRC snoop	Monitor reads from and writes to a certain register address	—

Note 1. The circuit cannot divide data used in CRC calculations. Write data in 8-bit or 32-bit units.

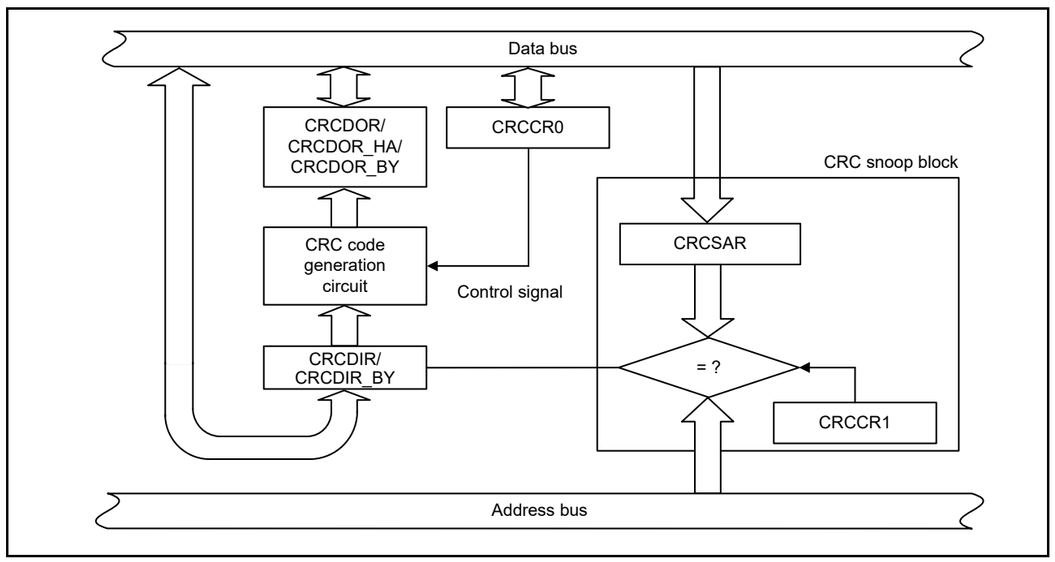


Figure 40.1 CRC calculator block diagram

40. 循环冗余校验(CRC)计算器

40.1 Overview

循环冗余校验(CRC)计算器生成CRC代码以检测数据中的错误。对于LSB或MSB优先的通信，可以切换CRC计算结果的位顺序。此外，您的应用程序还可以使用各种CRC生成多项式。snoop功能允许监视对特定地址的读取和写入。此功能在需要在某些事件中自动生成CRC代码的应用中很有用，例如监视对串行发送缓冲区的写入和从串行接收缓冲区的读取。

表40.1列出了CRC计算器规格，图40.1显示了框图。

Table 40.1 CRC计算器规格

Parameter	8位数据规格	32位数据规格
数据大小	8-bit	32-bit
CRC计算数据*1	为8n位单元中的数据生成的CRC码（其中n是整数）	为32n位单元中的数据生成的CRC码（其中n是整数）
CRC处理器单元	在8位上并行执行的操作	在32位上并行执行的操作
CRC生成多项式	三个生成多项式之一可选[8位CRC] X8+X2+X+1(CRC-8)[16位CRC] X16+X15+X2+1(CRC-16) X+X12+X5+1(CRC-CCITT)	可选的两个生成多项式之一[32位CRC] X32+X26+X23+X22+X16+X12+X11+X10+X8+X7+X5+X4+X2+X+1(CRC-32) X32+X28+X27+X26+X25+X23+X22+X20+X19+X18+X14+X13+X11+X10+X9+X8+X6+1(CRC-32C)
CRC计算切换	CRC计算结果的位顺序可以切换为LSB或MSB优先的通信	
Module-stop function	可设置模块停止状态以降低功耗	
CRC snoop	监视器读取和写入某个寄存器地址	—

Note 1. 该电路不能划分用于CRC计算的数据。以8位或32位为单位写入数据。

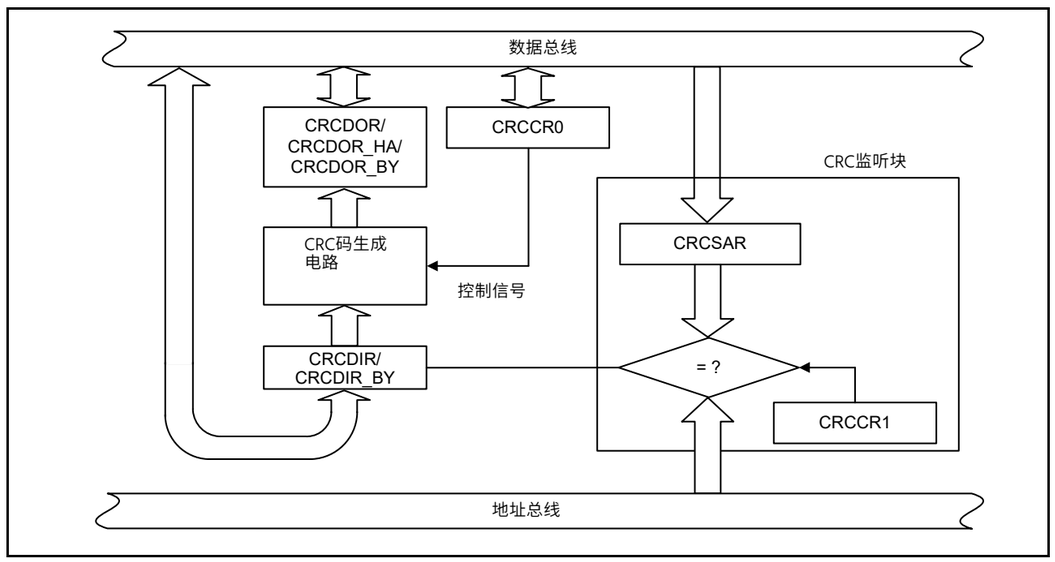


Figure 40.1 CRC计算器框图

40.2 Register Descriptions

40.2.1 CRC Control Register 0 (CRCCR0)

Address(es): CRC.CRCCR0 4007 4000h

	b7	b6	b5	b4	b3	b2	b1	b0
	DORCLR	LMS	—	—	—	GPS[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	GPS[2:0]	CRC Generating Polynomial Switching	b2 b0 0 0 0: Do not calculate 0 0 1: 8-bit CRC-8 ($X^8 + X^2 + X + 1$) 0 1 0: 16-bit CRC-16 ($X^{16} + X^{15} + X^2 + 1$) 0 1 1: 16-bit CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$) 1 0 0: 32-bit CRC-32 ($X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$) 1 0 1: 32-bit CRC-32C ($X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$) Other: Do not calculate.	R/W
b5 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6	LMS	CRC Calculation Switching	0: Generate CRC for LSB-first communication 1: Generate CRC for MSB-first communication.	R/W
b7	DORCLR	CRCDOR/CRCDOR_HA/CRCDOR_BY Register Clear	1: Clear the CRCDOR/CRCDOR_HA/CRCDOR_BY register. This bit is read as 0.	W*1

Note 1. This bit must always be set to 1 when writing to this register.

DORCLR bit (CRCDOR/CRCDOR_HA/CRCDOR_BY)

Write 1 to the DORCLR bit to clear the CRCDOR/CRCDOR_HA/CRCDOR_BY register to 0000_0000h. This bit is read as 0. Only 1 can be written.

LMS bit (CRC Calculation Switching)

The LMS bit selects the bit order of generated CRC code. Transmit the lower-order byte of the CRC code first for LSB-first communication and the higher-order byte first for MSB-first communication. For details on transmitting and receiving CRC code, see section 40.3, Operation.

GPS[2:0] bits (CRC Generating Polynomial Switching)

The GPS[2:0] bits select the CRC generating polynomial.

40.2.2 CRC Control Register 1 (CRCCR1)

Address(es): CRC.CRCCR1 4007 4001h

	b7	b6	b5	b4	b3	b2	b1	b0
	CRCSEN	CRCSWR	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b5 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6	CRCSWR	Snoop-On-Write/Read Switch	0: Snoop-on-read 1: Snoop-on-write.	R/W

40.2 注册说明

40.2.1 CRC控制寄存器0(CRCCR0)

Address(es): CRC.CRCCR0 4007 4000h

	b7	b6	b5	b4	b3	b2	b1	b0
	DORCLR	LMS	—	—	—	GPS[2:0]		
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b2 to b0	GPS[2:0]	CRC生成多项式Switching	b2 b0 0 0 0：不计算 0 0 1: 8-bit CRC-8 ($X^8 + X^2 + X + 1$) 0 1 0: 16-bit CRC-16 ($X^{16} + X^{15} + X^2 + 1$) 0 1 1: 16-bit CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$) 1 0 0: 32-bit CRC-32 ($X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$) 1 0 1: 32-bit CRC-32C ($X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$) 其他：不计算。	R/W
b5 to b3	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b6	LMS	CRC计算切换	0：为LSB-first通信生成CRC1：为MSB-first通信生成CRC。	R/W
b7	DORCLR	CRCDOR/CRCDOR_HA/CRCDOR_BY寄存器清除	1：清除CRCDORCRCDOR_HACRCDOR_BY寄存器。该位读为0。	W*1

Note 1. 写入该寄存器时，该位必须始终设置为1。

DORCLR bit (CRCDOR/CRCDOR_HA/CRCDOR_BY)

向DORCLR位写入1可将CRCDORCRCDOR_HACRCDOR_BY寄存器清零为0000_0000h。该位读为0。只能写入1。

LMS位（CRC计算切换）

LMS位选择生成的CRC码的位顺序。对于LSBfirst通信，首先发送CRC码的低位字节，对于MSBfirst通信，首先发送高位字节。有关发送和接收CRC码的详细信息，请参阅第40.3节，操作。

GPS[2:0]位（CRC生成多项式切换）

GPS[2:0]位选择CRC生成多项式。

40.2.2 CRC控制寄存器1(CRCCR1)

Address(es): CRC.CRCCR1 4007 4001h

	b7	b6	b5	b4	b3	b2	b1	b0
	CRCSEN	CRCSWR	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b5 to b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b6	CRCSWR	Snoop-On-Write/Read Switch	0: Snoop-on-read 1: Snoop-on-write.	R/W

Bit	Symbol	Bit name	Description	R/W
b7	CRCSEN	Snoop Enable	0: Disabled 1: Enabled.	R/W

CRCSWR bit (Snoop-On-Write/Read Switch)

The CRCSWR bit selects the direction of the access in the address monitoring function. When the bit is set to 0 (initial value), the CRC snoop operation to read a specific register address is enabled. When the bit is set to 1, the CRC snoop operation to write to a specific register address is enabled.

CRCSEN bit (Snoop Enable)

When the CRCSEN bit is set to 1, CRC snoop operation is enabled. When the bit is set to 0, CRC snoop operation is disabled.

40.2.3 CRC Data Input Register (CRCDIR/CRCDIR_BY)

Address(es): CRC.CRCDIR/CRCDIR_BY 4007 4004h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CRCDIR is a 32-bit read/write register to write data to for CRC-32 or CRC-32C calculation. CRCDIR_BY is an 8-bit read/write register to write data to for CRC-8, CRC-16, or CRC-CCITT calculation.

40.2.4 CRC Data Output Register (CRCDOR/CRCDOR_HA/CRCDOR_BY)

Address(es): CRC.CRCDOR/CRCDOR_HA/CRCDOR_BY 4007 4008h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CRCDOR is a 32-bit read/write register for CRC-32 or CRC-32C. CRCDOR_HA is a 16-bit read/write register for CRC-16 or CRC-CCITT. CRCDOR_BY is an 8-bit read/write register for CRC-8. Because its initial value is 0000_0000h, rewrite the CRCDOR/CRCDOR_HA/CRCDOR_BY register to perform the calculations using a value other than the initial value.

Data written to the CRCDIR/CRCDIR_BY register is CRC-calculated, and the result is stored in the CRCDOR/CRCDOR_HA/CRCDOR_BY register. If the CRC code is calculated following transferred data and the result is 0000_0000h, there is no CRC error.

When an 8-bit CRC ($X^8 + X^2 + X + 1$ polynomial) is in use, the valid CRC code is obtained in CRCDOR_BY.

When a 16-bit CRC ($X^{16} + X^{15} + X^2 + 1$ or $X^{16} + X^{12} + X^5 + 1$ polynomial) is in use, the valid CRC code is obtained in CRCDOR_HA.

Bit	Symbol	位名称	Description	R/W
b7	CRCSEN	侦听启用	0：禁用1 ：启用。	R/W

CRCSWR位（Snoop-On-Write读开关）

CRCSWR位选择地址监控功能中的访问方向。当该位设置为0（初始值）时，启用读取特定寄存器地址的CRC监听操作。当该位设置为1时，将启用写入特定寄存器地址的CRC侦听操作。

CRCSEN位（侦听启用）

当CRCSEN位设置为1时，启用CRC侦听操作。当该位设置为0时，CRC侦听操作被禁用。

40.2.3 CRC数据输入寄存器(CRCDIRCRCDIR_BY)

Address(es): CRC.CRCDIR/CRCDIR_BY 4007 4004h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CRCDIR是一个32位读写寄存器，用于写入数据以进行CRC-32或CRC-32C计算。CRCDIR_BY是一个8位读写寄存器，用于写入数据以进行CRC-8、CRC-16或CRC-CCITT计算。

40.2.4 CRC数据输出寄存器(CRCDORCRCDOR_HACRCDOR_BY)

Address(es): CRC.CRCDOR/CRCDOR_HA/CRCDOR_BY 4007 4008h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

CRCDOR是CRC-32或CRC-32C的32位读写寄存器。CRCDOR_HA是CRC16或CRC-CCITT的16位读写寄存器。CRCDOR_BY是CRC-8的8位读写寄存器。由于其初始值为0000_0000h，因此重写CRCDORCRCDOR_HACRCDOR_BY寄存器以使用初始值以外的值执行计算。

写入CRCDIRCRCDIR_BY寄存器的数据经过CRC计算，结果存储在CRCDORCRCDOR_HACRCDOR_BY寄存器。如果在传输数据后计算CRC码，结果为0000_0000h，则没有CRC错误。

当使用8位CRC（X8+X2+X+1多项式）时，在CRCDOR_BY中获得有效的CRC码。

当使用16位CRC（X16+X15+X2+1或X16+X12+X5+1多项式）时，有效的CRC码在CRCDOR_HA.

40.2.5 Snoop Address Register (CRCSAR)

Address(es): CRC.CRCSAR 4007 400Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	CRCSA[13:0]													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b13 to b0	CRCSA[13:0]	Register Snoop Address	These bits store the TDR or RDR address in the SCI module to snoop.	R/W
b15, b14	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

CRCSA[13:0] bits (Register Snoop Address)

The CRCSA[13:0] bits specify the lower 14 bits of the register address monitored by the CRC snoop operation. Only the following addresses can be used for the CRCSA[13:0] bits:

- 4007 0003h: SCI0.TDR, 4007 0005h: SCI0.RDR
- 4007 0023h: SCI1.TDR, 4007 0025h: SCI1.RDR
- 4007 0043h: SCI2.TDR, 4007 0045h: SCI2.RDR
- 4007 0063h: SCI3.TDR, 4007 0065h: SCI3.RDR
- 4007 0083h: SCI4.TDR, 4007 0085h: SCI4.RDR
- 4007 00A3h: SCI5.TDR, 4007 00A5h: SCI5.RDR
- 4007 00C3h: SCI6.TDR, 4007 00C5h: SCI6.RDR
- 4007 00E3h: SCI7.TDR, 4007 00E5h: SCI7.RDR
- 4007 0103h: SCI8.TDR, 4007 0105h: SCI8.RDR
- 4007 0123h: SCI9.TDR, 4007 0125h: SCI9.RDR
- 4007 000Fh: SCI0.FTDRL, 4007 0011h: SCI0.FRDRL
- 4007 002Fh: SCI1.FTDRL, 4007 0031h: SCI1.FRDRL
- 4007 004Fh: SCI2.FTDRL, 4007 0051h: SCI2.FRDRL
- 4007 006Fh: SCI3.FTDRL, 4007 0071h: SCI3.FRDRL
- 4007 008Fh: SCI4.FTDRL, 4007 0091h: SCI4.FRDRL
- 4007 00AFh: SCI5.FTDRL, 4007 00B1h: SCI5.FRDRL
- 4007 00CFh: SCI6.FTDRL, 4007 00D1h: SCI6.FRDRL
- 4007 00EFh: SCI7.FTDRL, 4007 00F1h: SCI7.FRDRL
- 4007 010Fh: SCI8.FTDRL, 4007 0111h: SCI8.FRDRL
- 4007 012Fh: SCI9.FTDRL, 4007 0131h: SCI9.FRDRL.

40.3 Operation

40.3.1 Basic Operation

The CRC calculator generates CRC codes for use in LSB- or MSB-first transfers.

The following examples illustrate CRC code generation for input data (F0h) using the 16-bit CRC-CCITT-generating polynomial ($X^{16} + X^{12} + X^5 + 1$). In these examples, the value of the CRC Data Output Register (CRCDOR_HA) is

40.2.5 监听地址寄存器(CRCSAR)

Address(es): CRC.CRCSAR 4007 400Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	CRCSA[13:0]													
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b13 to b0	CRCSA[13:0]	注册监听地址	这些位存储SCI模块中的TDR或RDR地址以进行监听。	R/W
b15, b14	—	Reserved	这些位被读取为0。写入值应为0。	R/W

CRCSA[13:0]位（寄存器监听地址）

CRCSA[13:0]位指定由CRC侦听操作监视的寄存器地址的低14位。CRCSA[13:0]位只能使用以下地址：

- 4007 0003h: SCI0.TDR, 4007 0005h: SCI0.RDR
- 4007 0023h: SCI1.TDR, 4007 0025h: SCI1.RDR
- 4007 0043h: SCI2.TDR, 4007 0045h: SCI2.RDR
- 4007 0063h: SCI3.TDR, 4007 0065h: SCI3.RDR
- 4007 0083h: SCI4.TDR, 4007 0085h: SCI4.RDR
- 4007 00A3h: SCI5.TDR, 4007 00A5h: SCI5.RDR
- 4007 00C3h: SCI6.TDR, 4007 00C5h: SCI6.RDR
- 4007 00E3h: SCI7.TDR, 4007 00E5h: SCI7.RDR
- 4007 0103h: SCI8.TDR, 4007 0105h: SCI8.RDR
- 4007 0123h: SCI9.TDR, 4007 0125h: SCI9.RDR
- 4007 000Fh: SCI0.FTDRL, 4007 0011h: SCI0.FRDRL
- 4007 002Fh: SCI1.FTDRL, 4007 0031h: SCI1.FRDRL
- 4007 004Fh: SCI2.FTDRL, 4007 0051h: SCI2.FRDRL
- 4007 006Fh: SCI3.FTDRL, 4007 0071h: SCI3.FRDRL
- 4007 008Fh: SCI4.FTDRL, 4007 0091h: SCI4.FRDRL
- 4007 00AFh: SCI5.FTDRL, 4007 00B1h: SCI5.FRDRL
- 4007 00CFh: SCI6.FTDRL, 4007 00D1h: SCI6.FRDRL
- 4007 00EFh: SCI7.FTDRL, 4007 00F1h: SCI7.FRDRL
- 4007 010Fh: SCI8.FTDRL, 4007 0111h: SCI8.FRDRL
- 4007 012Fh: SCI9.FTDRL, 4007 0131h: SCI9.FRDRL.

40.3 Operation

40.3.1 基本操作

CRC计算器生成用于LSB或MSB优先传输的CRC代码。

以下示例说明了使用16位CRC-CCITT生成多项式(X16+X12+X5+1)为输入数据(F0h)生成CRC码。在这些示例中，CRC数据输出寄存器(CRCDOR_HA)的值为

cleared before CRC calculation.

When an 8-bit CRC (with the polynomial $X^8 + X^2 + X + 1$) is in use, the valid bits of the CRC code are obtained in CRCDOR_BY. When an 32-bit CRC is in use, the valid bits of the CRC code are obtained in CRCDOR.

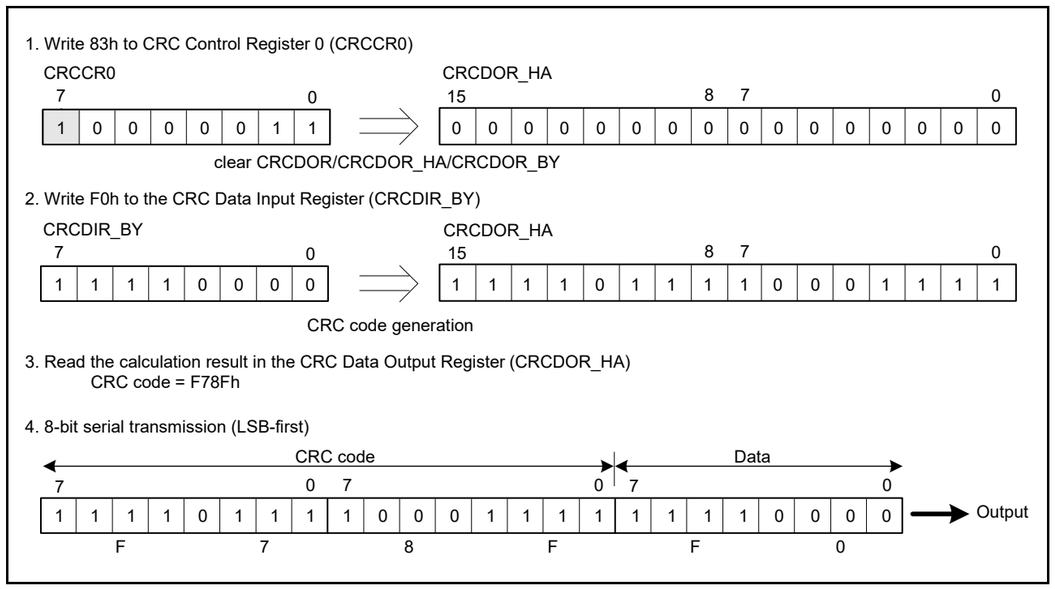


Figure 40.2 LSB-first data transmission

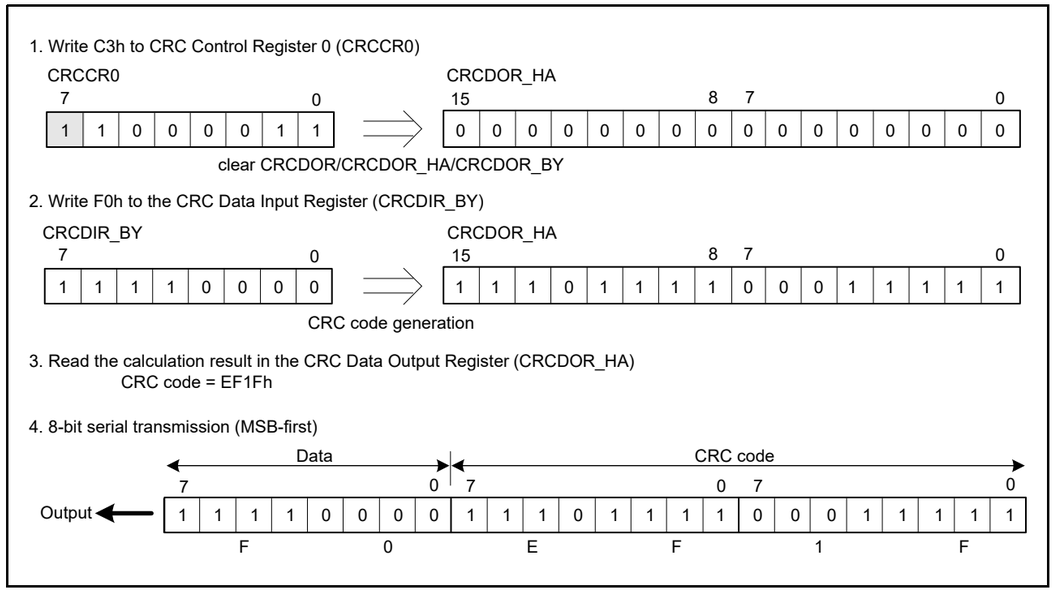


Figure 40.3 MSB-first data transmission

CRC计算前清零。

当使用8位CRC（多项式X8+X2+X+1）时，CRC码的有效位在CRCDOR_BY。当使用32位CRC时，在CRCDOR中获取CRC码的有效位。

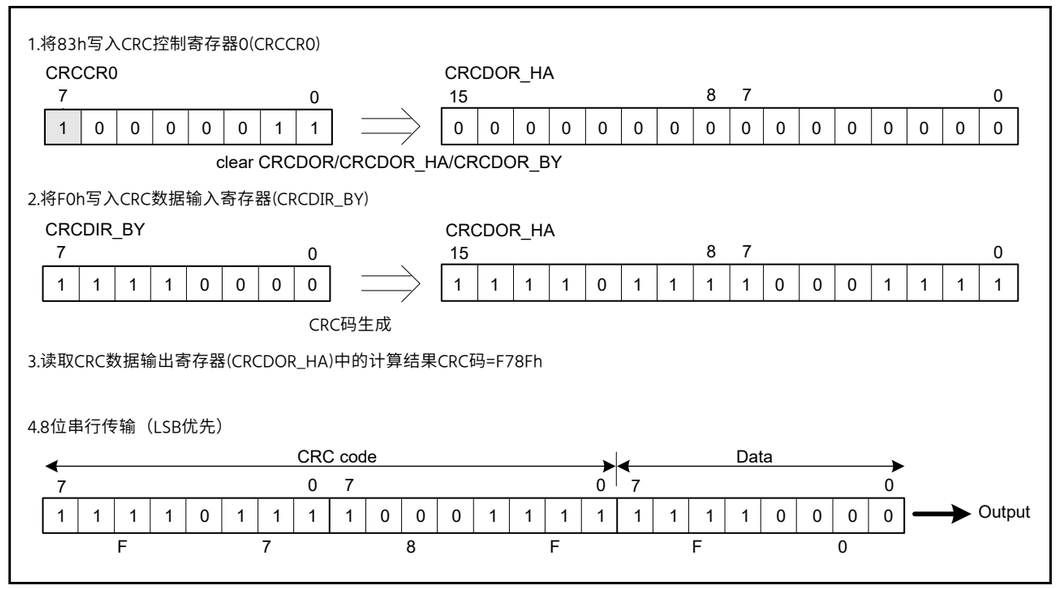


Figure 40.2 LSB−first数据传输

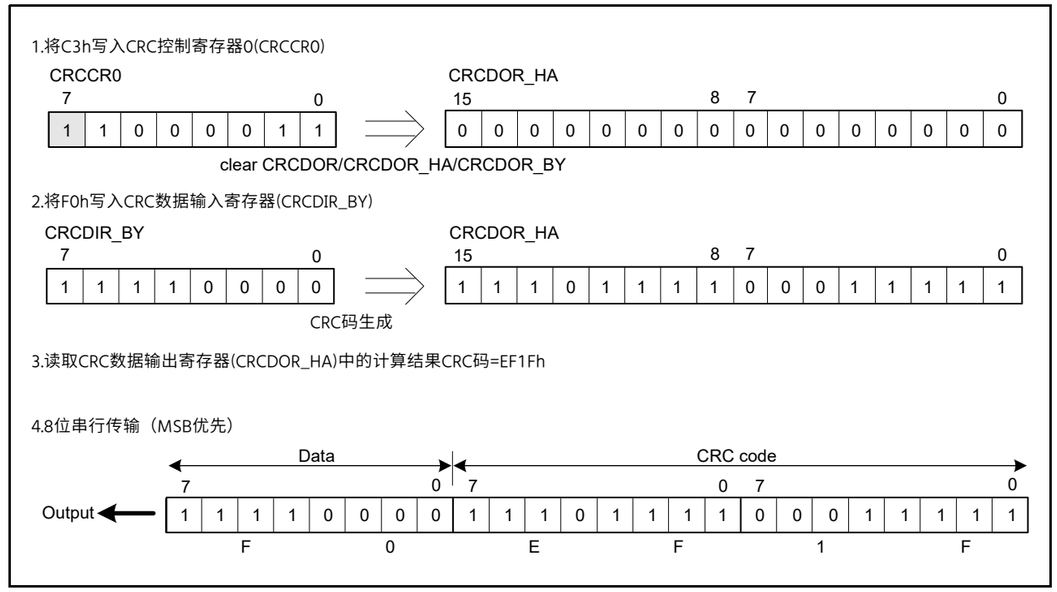
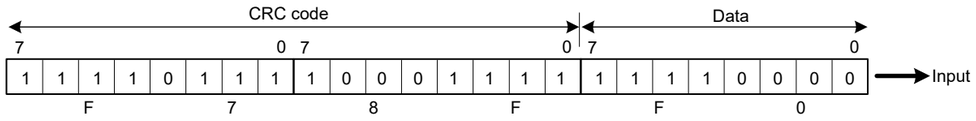
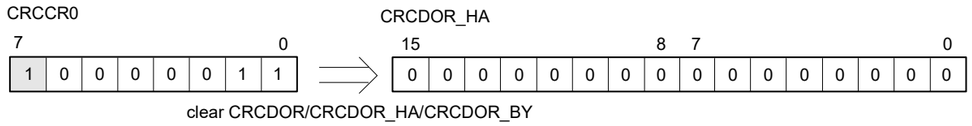


Figure 40.3 MSB优先数据传输

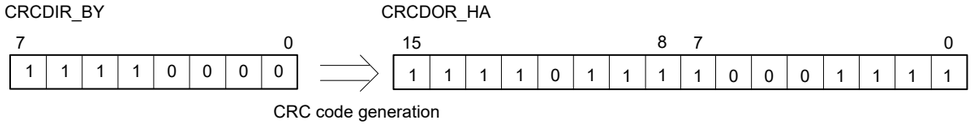
1. 8-bit serial reception (LSB-first)



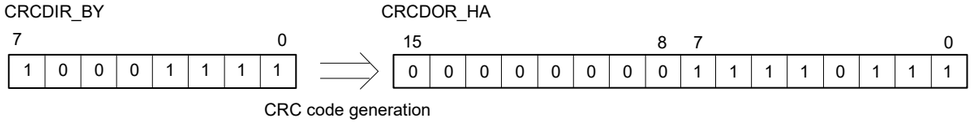
2. Write 83h to CRC Control Register 0 (CRCCR0)



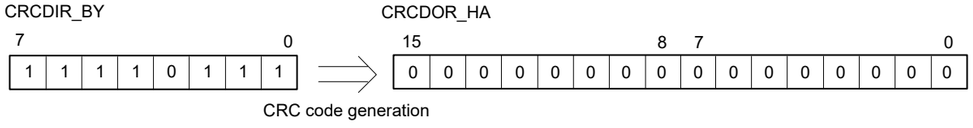
3. Write F0h to the CRC Data Input Register (CRCDIR_BY)



4. Write 8Fh to the CRC Data Input Register (CRCDIR_BY)



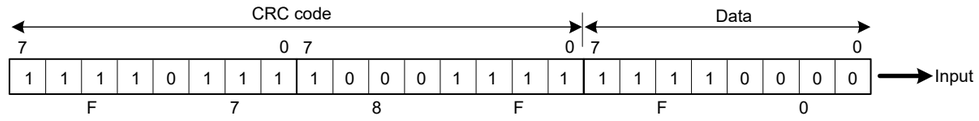
5. Write F7h to the CRC Data Input Register (CRCDIR_BY)



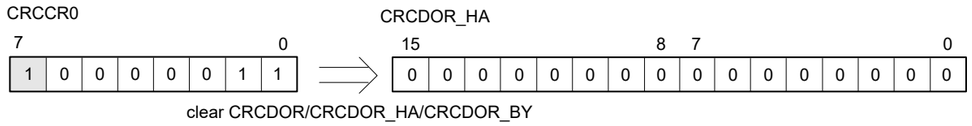
6. Read the calculation result in the CRC Data Output Register (CRCDOR_HA)
CRC code = 0000h → no error

Figure 40.4 LSB-first data reception

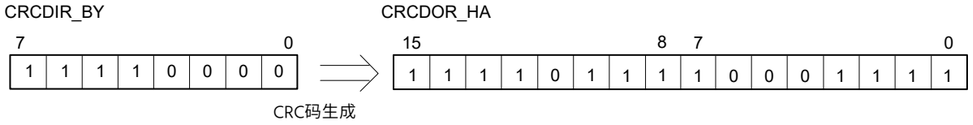
1.8位串行接收（LSB优先）



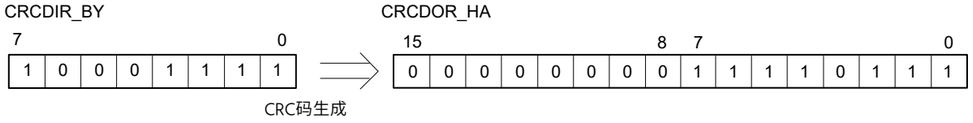
2.将83h写入CRC控制寄存器0(CRCCR0)



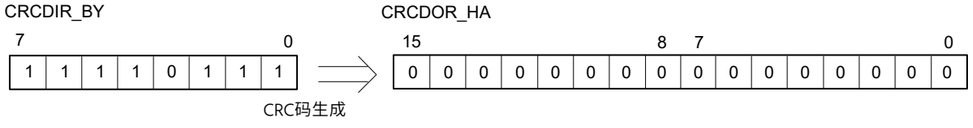
3.将F0h写入CRC数据输入寄存器(CRCDIR_BY)



4.将8Fh写入CRC数据输入寄存器(CRCDIR_BY)



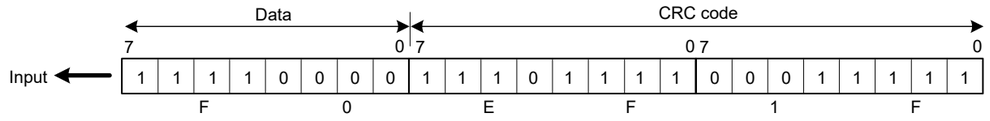
5.将F7h写入CRC数据输入寄存器(CRCDIR_BY)



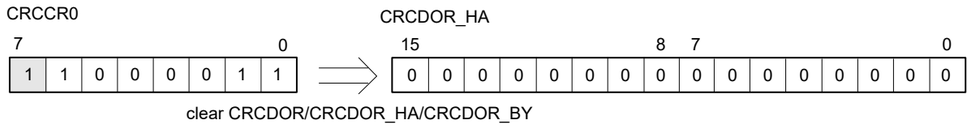
6.读取CRC数据输出寄存器（CRCDOR_HA）中的计算结果CRC码=0000h 无错误

Figure 40.4 LSB−first数据接收

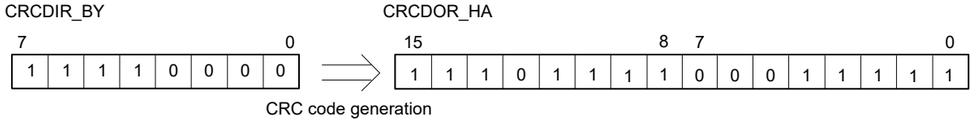
1. 8-bit serial reception (MSB-first)



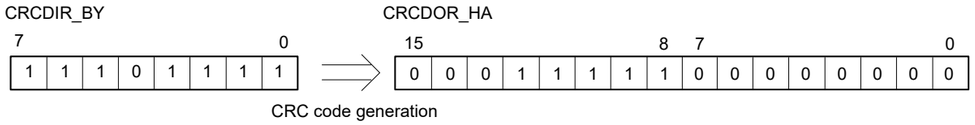
2. Write C3h to CRC Control Register 0 (CRCCR0)



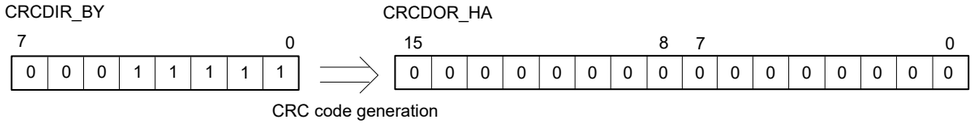
3. Write F0h to the CRC Data Input Register (CRCDIR_BY)



4. Write EFh to the CRC Data Input Register (CRCDIR_BY)



5. Write 1Fh to the CRC Data Input Register (CRCDIR_BY)



6. Read the calculation result in the CRC Data Output Register (CRCDOR_HA)
CRC code = 0000h → no error

Figure 40.5 MSB-first data reception

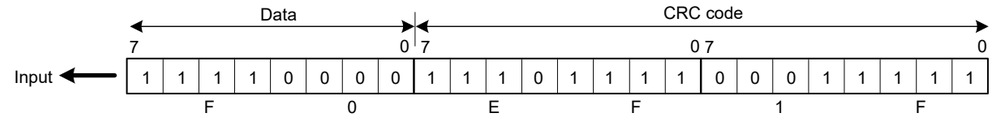
40.3.2 CRC Snoop

The CRC snoop function monitors reads from and writes to a specified I/O register address and performs CRC calculation on the data read from and written to the register address automatically. Because the CRC snoop recognizes writes to and reads from a specific register address as a trigger to automatically perform CRC calculation, writing data to the CRCDIR_BY register is not required. All I/O register addresses specified in section 40.2.5, Snoop Address Register (CRCSAR) are subject to the CRC snoop. The CRC snoop is useful in monitoring writes to the serial transmit buffer, and reads from the serial receive buffer.

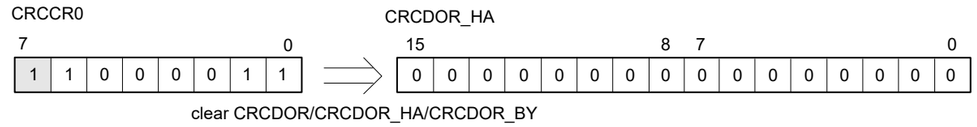
To use this function, write a target I/O register address to the CRCSA13 to CRCSA0 bits in the CRCSAR register, and set the CRCSEN bit in the CRCCR1 register to 1. Then set the CRCSWR bit in the CRCCR1 register to 1 to enable snooping on writes to the target address, or set the CRCSWR bit in the CRCCR1 register to 0 to enable snooping on reads from the target address.

When both the CRCSEN and CRCSWR bits are set to 1 and data is written to a target I/O register address in a bus master module (including the CPU, DMAC, and DTC), the CRC calculator stores the data in the CRCDIR_BY register and performs CRC calculation. Similarly, when the CRCSEN bit is set to 1 and the CRCSWR bit to 0, and data is read from

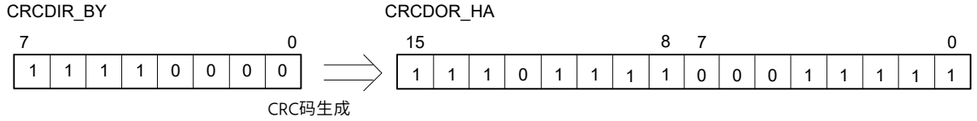
1.8位串行接收（MSB优先）



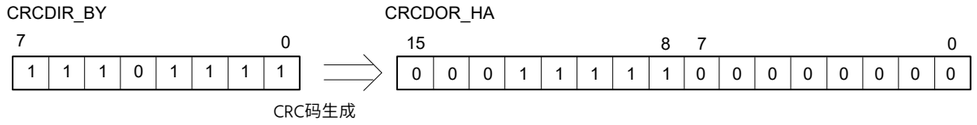
2.将C3h写入CRC控制寄存器0(CRCCR0)



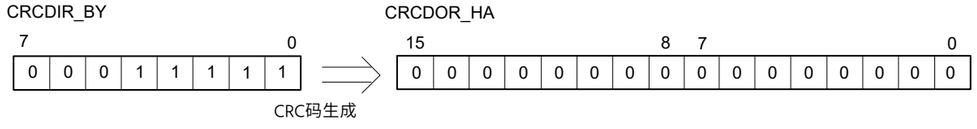
3.将F0h写入CRC数据输入寄存器(CRCDIR_BY)



4.将EFh写入CRC数据输入寄存器(CRCDIR_BY)



5.将1Fh写入CRC数据输入寄存器(CRCDIR_BY)



6.读取CRC数据输出寄存器（CRCDOR_HA）中的计算结果CRC码=0000h 无错误

Figure 40.5 MSB优先数据接收

40.3.2 CRC Snoop

CRCsnoop功能监视对指定IO寄存器地址的读取和写入，并自动对读取和写入该寄存器地址的数据进行CRC计算。由于CRCsnoop将特定寄存器地址的写入和读取识别为触发以自动执行CRC计算，因此不需要将数据写入CRCDIR_BY寄存器。第40.2.5节中指定的所有IO寄存器地址，侦听地址寄存器(CRCSAR)均受CRC侦听。CRCsnoop在监视对串行发送缓冲区的写入和从串行接收缓冲区读取时很有用。

要使用此功能，请将目标IO寄存器地址写入CRCSAR寄存器中的CRCSA13到CRCSA0位，并将CRCCR1寄存器中的CRCSEN位设置为1。然后将CRCCR1寄存器中的CRCSWR位设置为1，以启用写监听到目标地址，或将CRCCR1寄存器中的CRCSWR位设置为0，以启用对目标地址读取的侦听。

当CRCSEN和CRCSWR位都设置为1并且数据写入总线主控模块（包括CPU、DMAC和DTC）中的目标IO寄存器地址时，CRC计算器将数据存储在CRCDIR_BY寄存器中并执行CRC计算。同样，当CRCSEN位设置为1且CRCSWR位设置为0时，从

a target I/O register address in a bus master module (including the CPU, DMAC, and DTC), the CRC calculator stores the data in the CRCDIR_BY register and performs CRC calculation.

CRC calculation is performed 1 byte at a time. When the target I/O register address is accessed in words (16 bits) or long words (32 bits), CRC code is generated on the lower byte (1 byte) of data.

40.4 Usage Notes

40.4.1 Settings for the Module-Stop Function

CRC calculator operation can be disabled or enabled using Module Stop Control Register C (MSTPCRC). The CRC calculator is initially stopped after reset. Releasing the module-stop state enables access to the registers. For details, see section 11, Low Power Modes.

40.4.2 Note on Transmission

The transmission sequence for the CRC code differs depending on whether transmission is LSB-first or MSB-first.

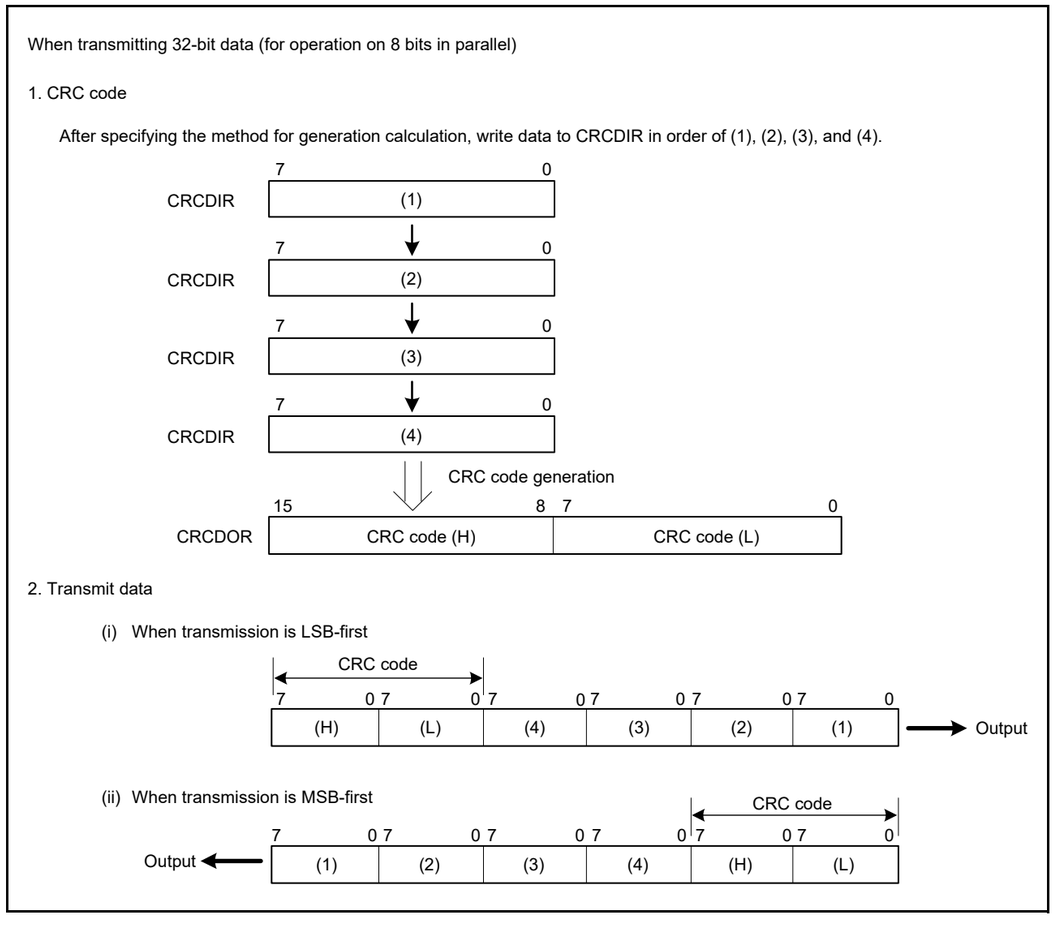


Figure 40.6 LSB-first and MSB-first data transmission

总线主控模块（包括CPU、DMAC和DTC）中的目标IO寄存器地址，CRC计算器将数据存储在CRCDIR_BY寄存器中并进行CRC计算。

每次执行1个字节的CRC计算。当以字（16位）或长字（32位）访问目标IO寄存器地址时，会在数据的低字节（1字节）上生成CRC码。

40.4 使用说明

40.4.1 模块停止功能的设置

可以使用模块停止控制寄存器C(MSTPCRC)禁用或启用CRC计算器操作。CRC计算器在复位后最初停止。释放模块停止状态可以访问寄存器。有关详细信息，请参阅第11节，低功耗模式。

40.4.2 传输注意事项

CRC码的传输顺序根据传输是LSB优先还是MSB优先而有所不同。

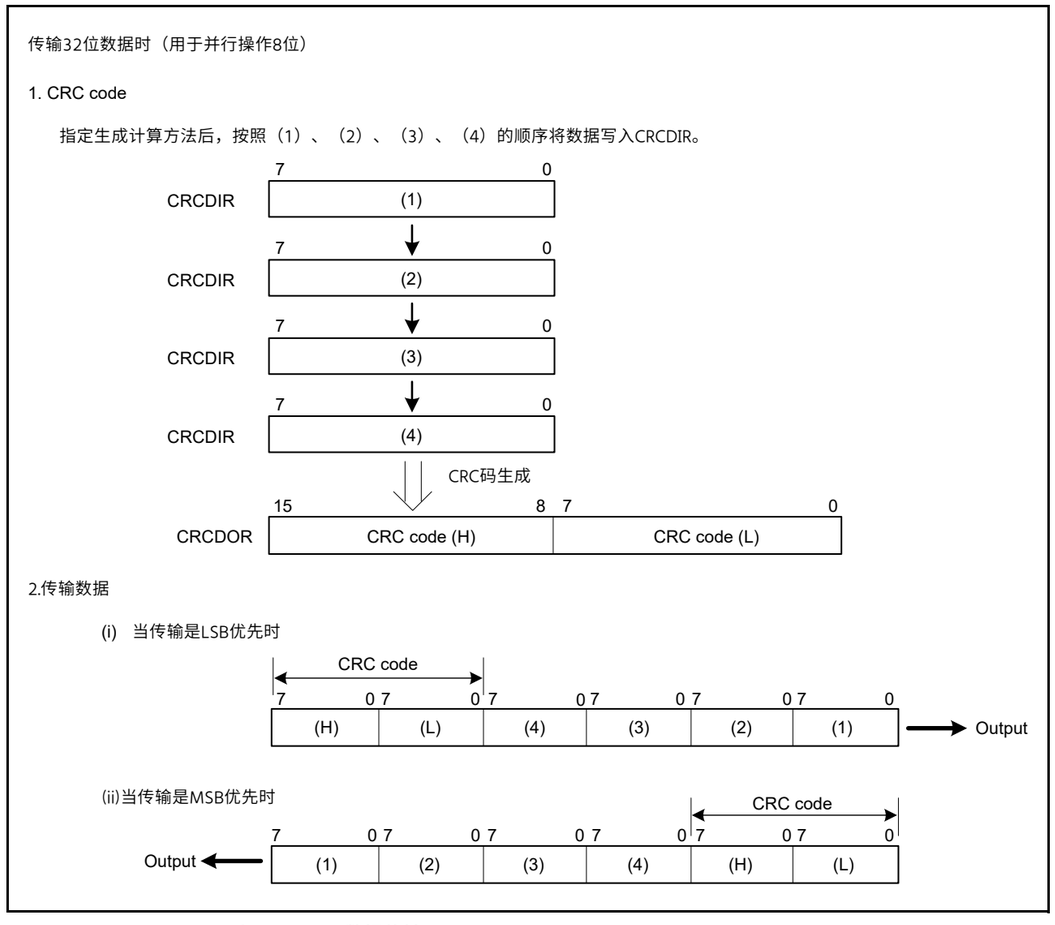


Figure 40.6 LSB−first和MSB−first数据传输

41. Serial Sound Interface Enhanced (SSIE)

41.1 Overview

The Serial Sound Interface Enhanced (SSIE) can transmit and receive audio data to and from various devices that support any of audio data formats, such as I2S, monaural, and TDM.

41.2 Features

Table 41.1 Features of SSIE

Parameter		Description
Number of channels		Two channels, SSIE0 and SSIE1
Communication mode		• Master/slave • Transmission/reception(SSIE0 full-duplex communication) • Transmission/reception(SSIE1 half-duplex communication)
Communication format		• I2S format • Monaural format • TDM format
Serial data		• MSB first • Data can be left-justified or right-justified. • Data delay (1 clock cycle) or no delay selectable for the period from SSILRCK/SSIFS to SSITXD0/SSIRXD0/SSIDATA1 • System word length: 8, 16, 24, 32, 48, 64, 128, or 256 bits • Data word length: 8, 16, 18, 20, 22, 24, or 32 bits • Padding polarity: Low or high
Bit clock (SSIBCK)	In master mode	• Two clock sources available (AUDIO_CLK/GPT output (GTIOC1A)) • Clock source division ratio: 1/1, 1/2, 1/4, 1/6, 1/8, 1/12, 1/16, 1/24, 1/32, 1/48, 1/64, 1/96, and 1/128. • Supply/stop is selectable while communication is halted.
	In master/slave mode	• Polarity (rising edge or falling edge) selectable
LR clock/frame synchronization (SSILRCK/SSIFS)	In master mode	• Polarity (low level or high level) selectable • Supply/stop is selectable while communication is halted.
Transmit data (SSITXD0/SSIDATA1) and receive data (SSIRXD0/SSIDATA1)	Transmission	• Muting method (transmission of transmit FIFO data or transmission of data fixed to 0) selectable
FIFO	Capacity	• Transmit FIFO/receive FIFO: 4 bytes × 32 stages
	Data alignment	• Data alignment method (left-justification or right-justification) selectable for the data transfer between FIFO and shift register
Interrupt	Interrupt output	• Communication error/idle mode • Receive data full • Transmit data empty
Low power consumption function		• Whether to supply the audio clock selectable in master mode
Module stop function		• Module stop state can be set to reduce power consumption.

The following table lists and defines the terms used for the communication formats SSIE can use:

Table 41.2 Definition of terms

Term	Definition
Start trigger	First edge of the signal on the SSILRCK/SSIFS pin when the signal is set to the value specified in LRCKP to enable communication
Frame boundary	Point where SSIE starts transferring the first data of a frame or the point where SSIE ends transferring the last data of the frame

41. 串行声音接口增强(SSIE)

41.1 Overview

增强型串行声音接口(SSIE)可以向各种支持任何音频数据格式（例如I2S、单声道和TDM）的设备发送和接收音频数据。

41.2 Features

Table 41.1 SSIE的特点

Parameter		Description
通道数		两个通道，SSIE0和SSIE1
通讯方式		• Master/slave • Transmission/reception(SSIE0 full-duplex communication) • Transmission/reception(SSIE1 half-duplex communication)
通讯格式		• I2S format • Monaural format • TDM format
串行数据		MSB优先 数据可以左对齐或右对齐。 从SSILRCKSSIFS到SSITXD0SSIRXD0SSIDATA1期间可选择数据延迟（1个时钟周期）或无延迟 系统字长：8、16、24、32、48、64、128或256位 数据字长：8、16、18、20、22、24或32位 填充极性：低或高
位时钟(SSIBCK)	在主模式	两个时钟源可用（AUDIO_CLKGPT输出(GTIOC1A)） 时钟源分频比：11、12、14、16、18、112、116、124、132、148、164、196和1128。 通信停止时可选择停止供电。
	在主从模式	极性（上升沿或下降沿）可选
LR clock/frame synchronization (SSILRCK/SSIFS)	在主模式	极性（低电平或高电平）可选 通信停止时可选择停止供电。
发送数据(SSITXD0SSIDATA1)和接收数据(SSIRXD0SSIDATA1)	Transmission	可选择静音方法（传输传输FIFO数据或传输固定为0的数据）
FIFO	Capacity	发送FIFO接收FIFO：4字节×32级
	数据对齐	数据对齐方式（左对齐或右对齐）可选择用于FIFO和移位寄存器之间的数据传输
Interrupt	中断输出	通信错误空闲模式 接收数据已满 传输数据空
低功耗功能		是否提供在主模式下可选择的音频时钟
模块停止功能		可设置模块停止状态以降低功耗。

下表列出并定义了用于SSIE可以使用的通信格式的术语：

Table 41.2 术语定义

Term	Definition
启动触发器	当信号设置为LRCKP中指定的值以启用通信时，SSILRCKSSIFS引脚上的信号的第一个边沿
框架边界	SSIE开始传输帧的第一个数据的点或SSIE结束传输帧的最后一个数据的点

Table 41.2 Definition of terms

Term	Definition
Frame word number	Number of sound channels per frame
System word length	Number of bits per channel
Data word length	Number of significant bits per channel
Control bits for communication formats	• SSICR register: FRM, DWL, SWL, LRCKP, SPDP, SDTA, PDTA, and DEL bits • SSIFCR register: BSW bit • SSIOFR register: OMOD bit • SSISCR register: TDES and RDFS bits

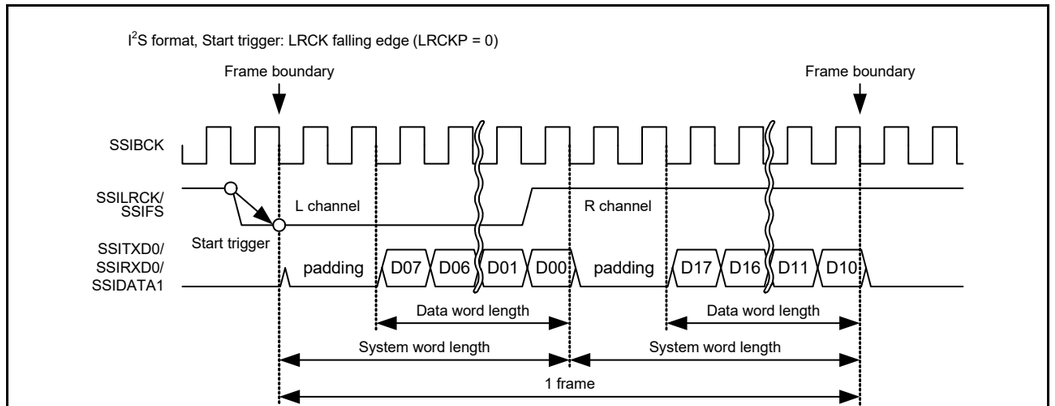


Figure 41.1 Definition of communication format

41.3 Block Diagram

Figure 41.2 and Figure 41.3 show a block diagram of SSIE.

Table 41.2 术语定义

Term	Definition
帧字数	每帧声道数
系统字长	每个通道的位数
数据字长	每个通道的有效位数
通信格式的控制位	SSICR寄存器：FRM、DWL、SWL、LRCKP、SPDP、SDTA、PDTA和DEL位 SSIFCR寄存器：BSW位 SSIOFR寄存器：OMOD位 SSISCR寄存器：TDES和RDFS位

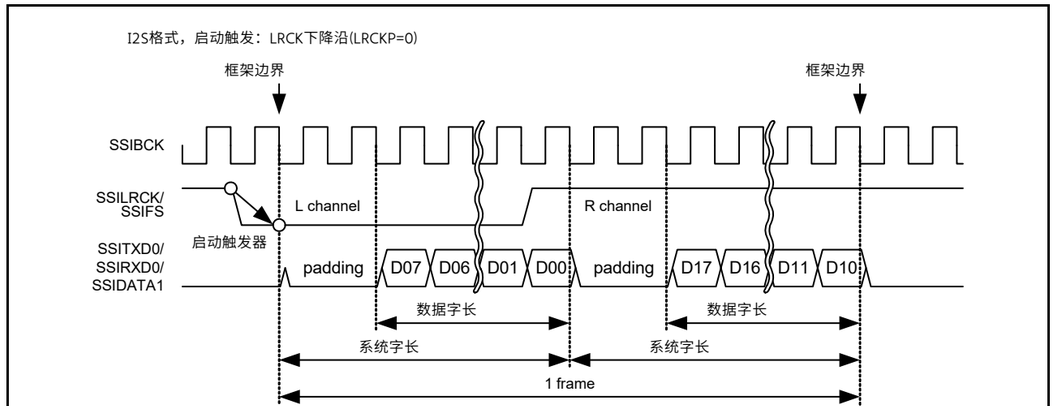


Figure 41.1 通讯格式的定义

41.3 框图

图41.2和图41.3显示了SSIE的框图。

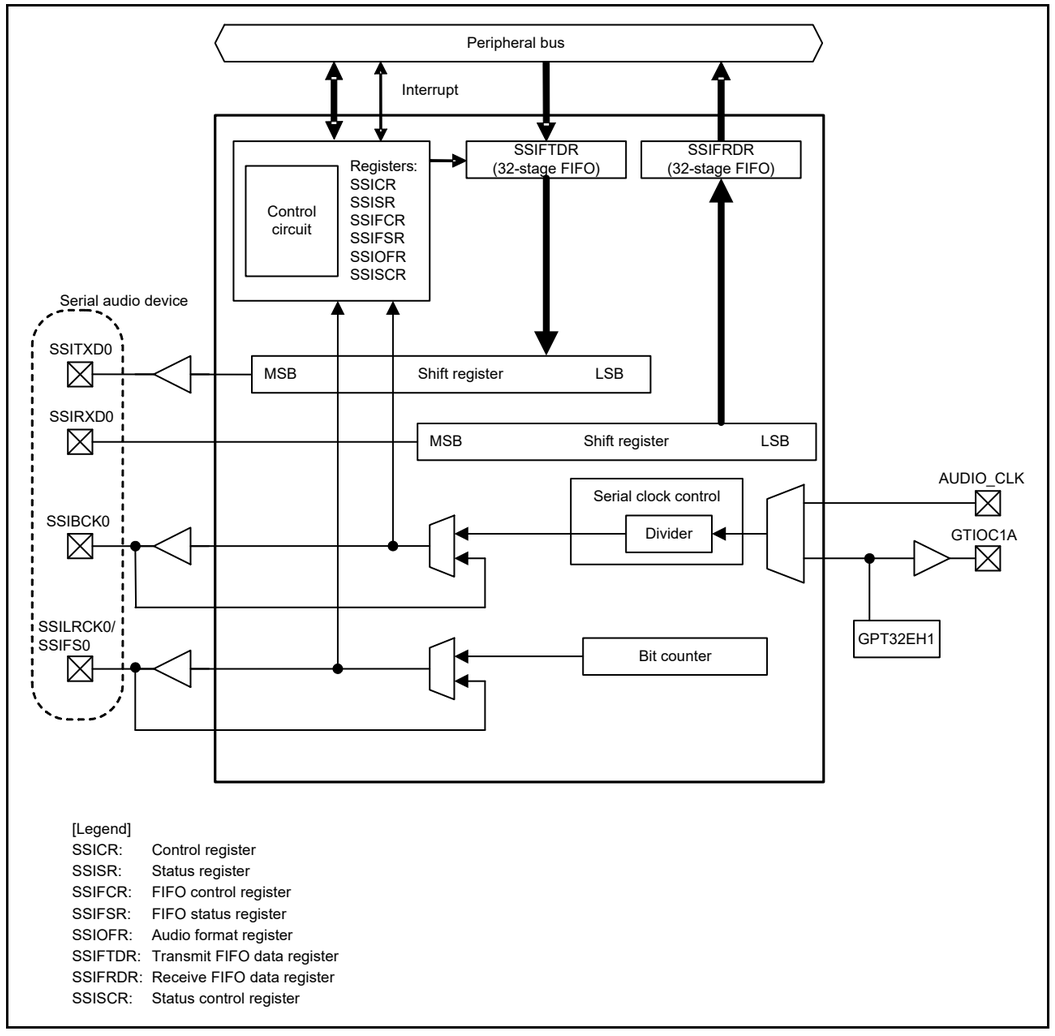


Figure 41.2 SSIE block diagram (SSIE0)

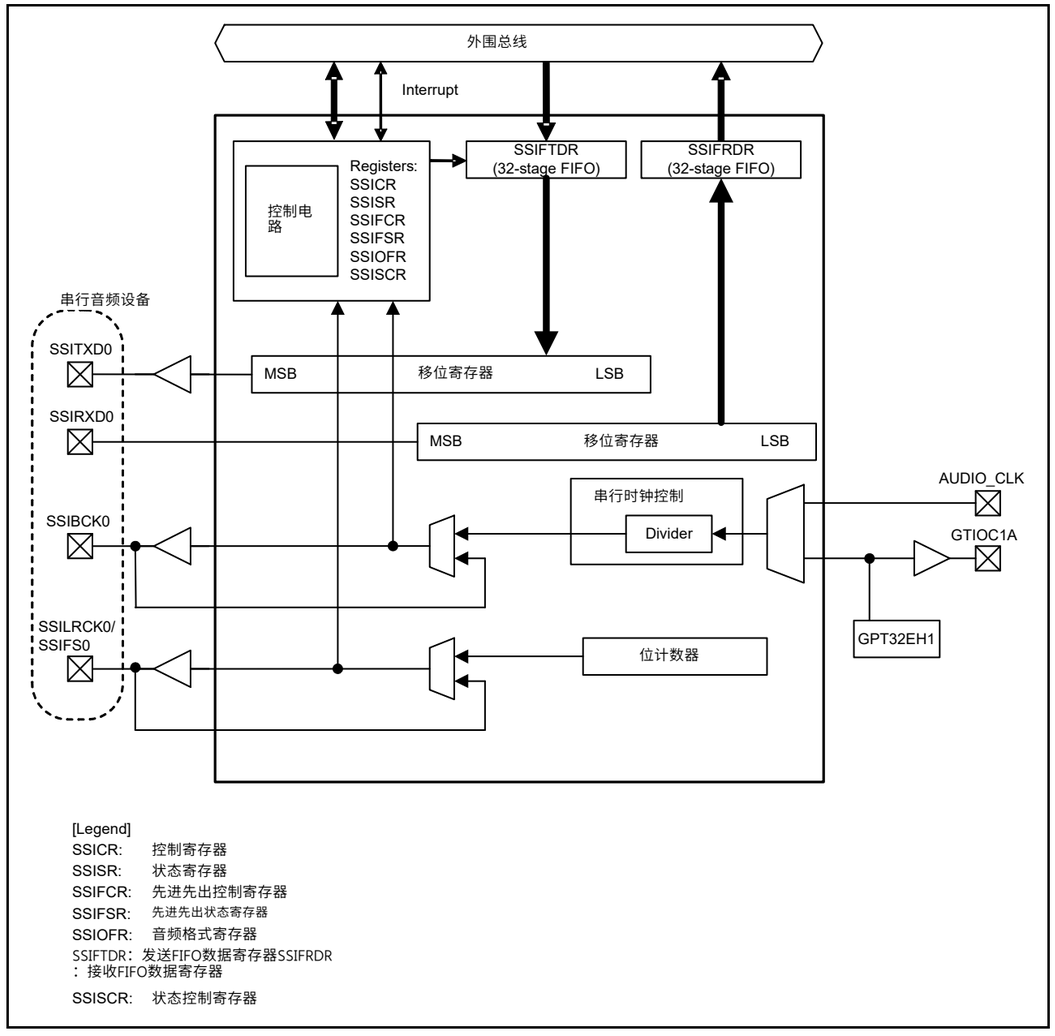


Figure 41.2 SSIE框图(SSIE0)

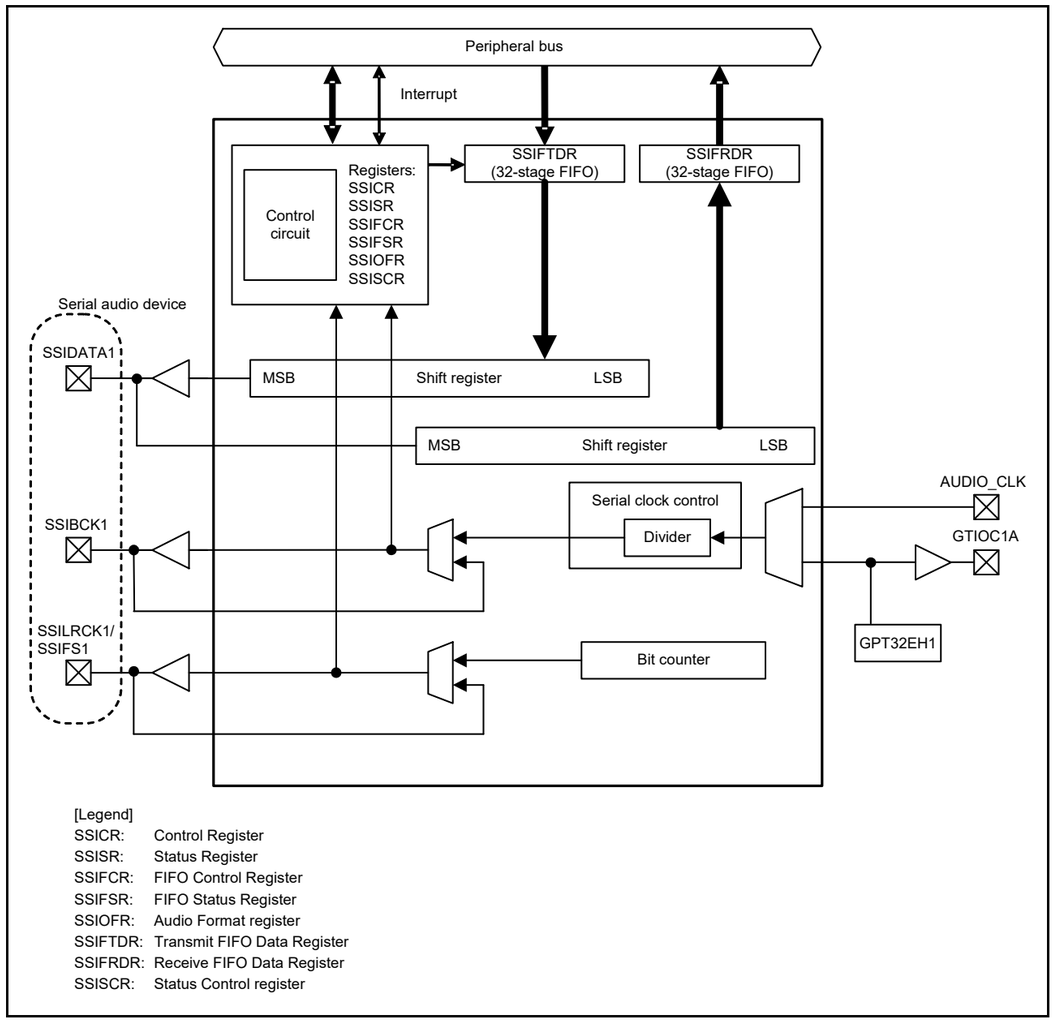


Figure 41.3 SSIE block diagram (SSIE1)

Figure 41.4 shows the clock configuration of SSIE.

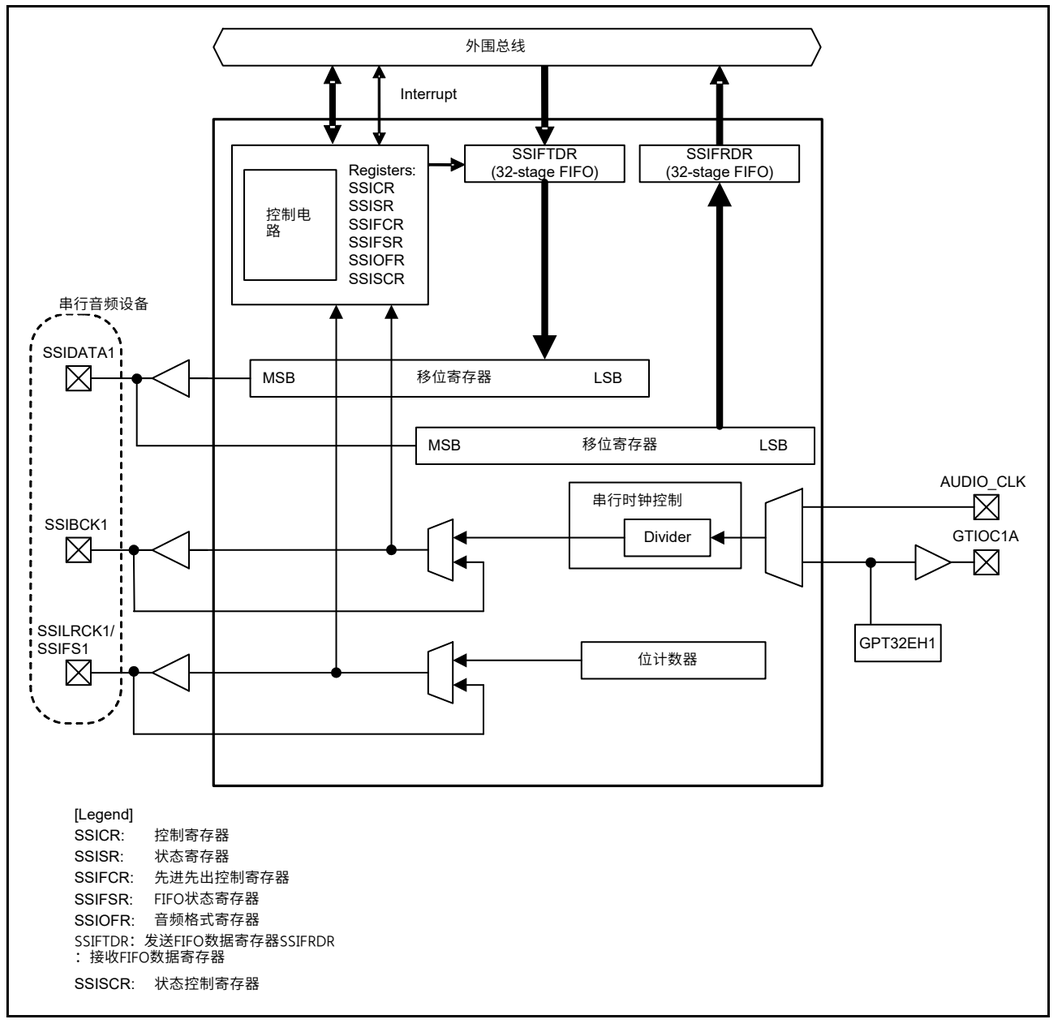


Figure 41.3 SSIE框图(SSIE1)

图41.4显示了SSIE的时钟配置。

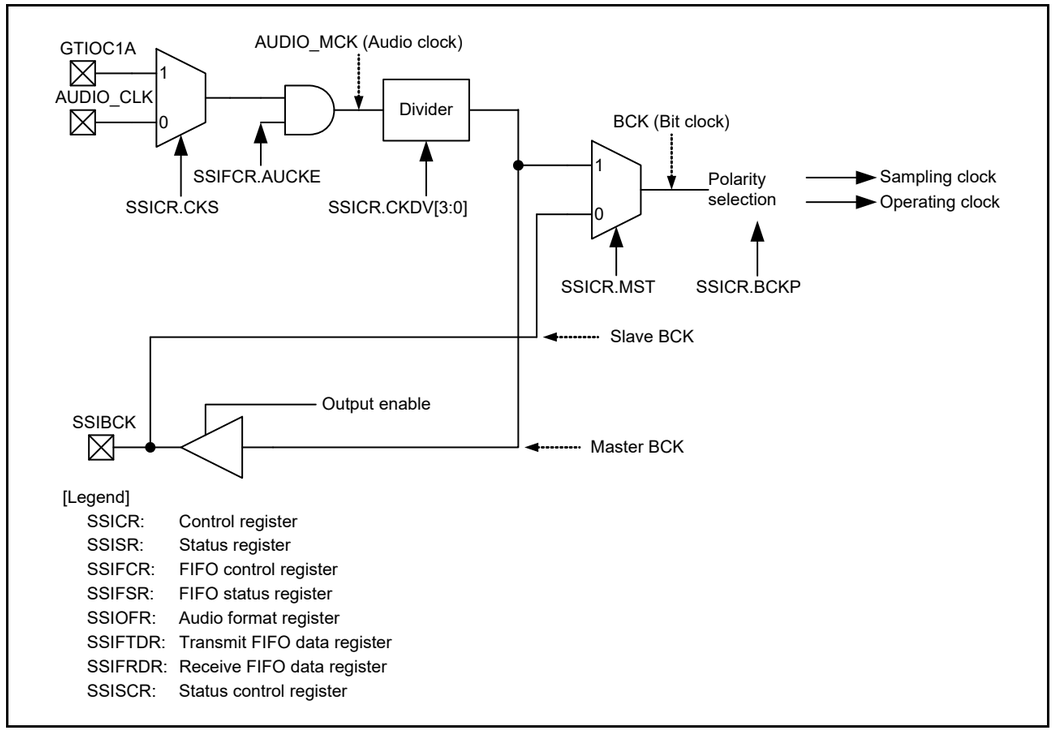


Figure 41.4 SSIE clock configuration

41.4 Register Descriptions

41.4.1 Control Register (SSICR)

Address(es): SSIE0.SSICR 4004 E000h, SSIE1.SSICR 4004 E100h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	CKS	TUIEN	TOIEN	RUIEN	ROIEN	IIEN	—	FRM[1:0]		DWL[2:0]			SWL[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	MST	BCKP	LRCKP	SPDP	SDTA	PDTA	DEL	CKDV[3:0]				MUEN	—	TEN	REN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	REN	Transmission and Reception Enable*2	00: Disables transmission and reception 01: Enables reception (starts reception) 10: Enables transmission (starts transmission) 11: Enables transmission and reception (starts transmission and reception).	R/W
b1	TEN			
b2	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b3	MUEN	Mute Enable	0: Disables muting on the next frame boundary 1: Enables muting on the next frame boundary.	R/W

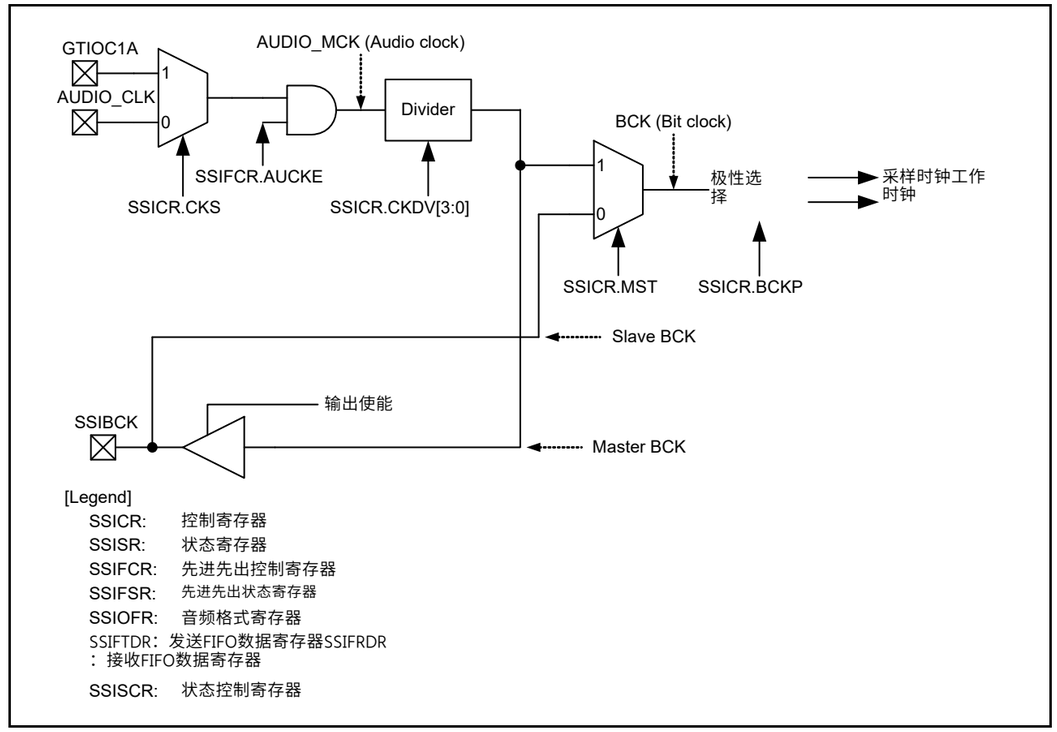


Figure 41.4 SSIE时钟配置

41.4 注册说明

41.4.1 控制寄存器(SSICR)

Address(es): SSIE0.SSICR 4004 E000h, SSIE1.SSICR 4004 E100h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	CKS	TUIEN	TOIEN	RUIEN	ROIEN	IIEN	—	FRM[1:0]		DWL[2:0]			SWL[2:0]		
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	MST	BCKP	LRCKP	SPDP	SDTA	PDTA	DEL	CKDV[3:0]				MUEN	—	TEN	REN
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	REN	传输和接收 Enable*2	00：禁止发送和接收01：允许接收（开始接收）10：允许发送（开始发送）11：允许发送和接收（开始发送和接收）。	R/W
b1	TEN			
b2	—	Reserved	该位读取为0。写入值应为0。	R/W
b3	MUEN	静音启用	0：在下一帧边界禁用静音1：在下一帧边界启用静音。	R/W

Bit	Symbol	Bit name	Description	R/W
b7 to b4	CKDV[3:0]	Selects Bit Clock Division Ratio*1	b7 b4 0 0 0 0: AUDIO_MCK 0 0 0 1: AUDIO_MCK/2 0 0 1 0: AUDIO_MCK/4 0 0 1 1: AUDIO_MCK/8 0 1 0 0: AUDIO_MCK/16 0 1 0 1: AUDIO_MCK/32 0 1 1 0: AUDIO_MCK/64 0 1 1 1: AUDIO_MCK/128 1 0 0 0: AUDIO_MCK/6 1 0 0 1: AUDIO_MCK/12 1 0 1 0: AUDIO_MCK/24 1 0 1 1: AUDIO_MCK/48 1 1 0 0: AUDIO_MCK/96 1 1 0 1: Setting prohibited 1 1 1 0: Setting prohibited 1 1 1 1: Setting prohibited.	R/W
b8	DEL	Selects Serial Data Delay*1	0: Delay of 1 cycle of SSIBCK between SSILRCK/SSIFS and SSITXD0/SSIRXD0/SSIDATA1 1: No delay between SSILRCK/SSIFS and SSITXD0/SSIRXD0/SSIDATA1 In the monaural format, this bit controls the waveform of SSILRCK/SSIFS. For details, see section 41.5.2, Monaural Format.	R/W
b9	PDTA	Selects Placement Data Alignment*1	0: Left-justifies placement data (SSIFTDR, SSIFRDR) 1: Right-justifies placement data (SSIFTDR, SSIFRDR).	R/W
b10	SDTA	Selects Serial Data Alignment *1	0: Transmits and receives serial data first and then padding bits 1: Transmit and receives padding bits first and then serial data.	R/W
b11	SPDP	Selects Serial Padding Polarity*1	0: Padding data is at a low level 1: Padding data is at a high level.	R/W
b12	LRCKP	Selects the Initial Value and Polarity of LR Clock/Frame Synchronization Signal*1	0: The initial value is at a high level The start trigger for a frame is synchronized with a falling edge of SSILRCK/SSIFS 1: The initial value is at a low level The start trigger for a frame is synchronized with a rising edge of SSILRCK/SSIFS.	R/W
b13	BCKP	Selects Bit Clock Polarity*1	0: SSILRCK/SSIFS and SSITXD0/SSIRXD0/SSIDATA1 change at a falling edge (SSILRCK/SSIFS and SSIRXD0/SSIDATA1 are sampled at a rising edge of SSIBCK) 1: SSILRCK/SSIFS and SSITXD0/SSIRXD0/SSIDATA1 change at a rising edge (SSILRCK/SSIFS and SSIRXD0/SSIDATA1 are sampled at a falling edge of SSIBCK).	R/W
b14	MST	Master Enable*1	0: Slave-mode communication 1: Master-mode communication.	R/W
b15	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b18 to b16	SWL[2:0]	Selects System Word Length *1	b18 b16 0 0 0: 8 bits 0 0 1: 16 bits 0 1 0: 24 bits 0 1 1: 32 bits 1 0 0: 48 bits 1 0 1: 64 bits 1 1 0: 128 bits 1 1 1: 256 bits.	R/W
b21 to b19	DWL[2:0]	Selects Data Word Length*1	b21 b19 0 0 0: 8 bits 0 0 1: 16 bits 0 1 0: 18 bits 0 1 1: 20 bits 1 0 0: 22 bits 1 0 1: 24 bits 1 1 0: 32 bits 1 1 1: Setting prohibited.	R/W

Bit	Symbol	位名称	Description	R/W
b7 to b4	CKDV[3:0]	选择位时钟分频 Ratio*1	b7b40000：AUDIO_MCK0001：AUDIO_MCK20010：AUDIO_MCK40011：AUDIO_MCK80100：AUDIO_MCK160101：AUDIO_MCK320110：AUDIO_MCK640111：AUDIO_MCK1281000：AUDIO_MCK61001：AUDIO_MCK121010：AUDIO_MCK241011：AUDIO_MCK481100：AUDIO_MCK961101：禁止设置1110：禁止设置1111：禁止设置。	R/W
b8	DEL	选择串行数据延迟*1	0：在SSILRCKSSIFS和SSITXD0SSIRXD0SSIDATA1之间延迟1个SSIBCK周期1：在SSILRCKSSIFS和SSITXD0SSIRXD0SSIDATA1之间没有延迟 在单声道格式中，该位控制SSILRCK/SSIFS. 有关详细信息，请参阅第41.5.2节，单声道格式。	R/W
b9	PDTA	选择放置数据 Alignment*1	0：左对齐放置数据（SSIFTDR、SSIFRDR）1：右对齐放置数据（SSIFTDR、SSIFRDR）。	R/W
b10	SDTA	选择串行数据对齐*1	0：先发送和接收串行数据，然后是填充位1：先发送和接收填充位，然后是串行数据。	R/W
b11	SPDP	选择串行填充 Polarity*1	0：填充数据为低电平1：填充数据为高电平。	R/W
b12	LRCKP	选择LR时钟帧的初始值和极性 Synchronization Signal*1	0：初始值为高电平 帧的开始触发与SSILRCK的下降沿同步SSIFS1：初始值为低电平 帧的开始触发与SSILRCKSSIFS的上升沿同步。	R/W
b13	BCKP	选择位时钟极性*1	0：SSILRCKSSIFS和SSITXD0SSIRXD0SSIDATA1在下降沿变化（SSILRCKSSIFS和SSIRXD0SSIDATA1在SSIBCK的上升沿采样）1：SSILRCKSSIFS和SSITXD0SSIRXD0SSIDATA1在上升沿变化（SSILRCKSSIFS和SSIRXD0SSIDATA1在上升沿采样SSIBCK的下降沿）。	R/W
b14	MST	Master Enable*1	0: Slave-mode communication 1: Master-mode communication.	R/W
b15	—	Reserved	该位读取为0。写入值应为0。	R/W
b18 to b16	SWL[2:0]	选择系统字长*1	b18 b16 0 0 0: 8 bits 0 0 1: 16 bits 0 1 0: 24 bits 0 1 1: 32 bits 1 0 0: 48 bits 1 0 1: 64 bits 1 1 0: 128 bits 1 1 1: 256 bits.	R/W
b21 to b19	DWL[2:0]	选择数据字长*1	b21b19000：8位001：16位010：18位011：20位100：22位101：24位110：32位111：禁止设置.	R/W

Bit	Symbol	Bit name	Description	R/W
b23, b22	FRM[1:0]	Selects Frame Word Number *1		R/W

	Communication format (SSIOFR.OMOD[1:0])		
FRM[1:0]	I²S (00b)	Monaural (10b)	TDM (01b)
00b	2	1	Setting prohibited
01b	Setting prohibited	Setting prohibited	4
10b			6
11B			8

b24	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b25	IIEN	Idle Mode Interrupt Output Enable	0: Disables idle mode interrupt output 1: Enables idle mode interrupt output.	R/W
b26	ROIEN	Receive Overflow Interrupt Output Enable	0: Disables receive overflow interrupt output 1: Enables receive overflow interrupt output.	R/W
b27	RUIEN	Receive Underflow Interrupt Output Enable	0: Disables receive underflow interrupt output 1: Enables receive underflow interrupt output.	R/W
b28	TOIEN	Transmit Overflow Interrupt Output Enable	0: Disables transmit overflow interrupt output 1: Enables transmit overflow interrupt output.	R/W
b29	TUIEN	Transmit Underflow Interrupt Output Enable	0: Disables transmit underflow interrupt output 1: Enables transmit underflow interrupt output.	R/W
b30	CKS	Selects an Audio Clock for Master-mode Communication *1	0: Selects the AUDIO_CLK input 1: Selects the GTIOC1A (GPT output).	R/W
b31	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Note 1. Writing to these bits while SSIE is in a communication state (SSISR.IIRQ = 0) is prohibited. If the value of these bits is changed by rewriting, subsequent operation is unpredictable.

Note 2. If the TEN bit or REN bit is rewritten, make sure that the SSISR.IIRQ bit is in the desired status. If the value of the TEN or REN bit is changed by rewriting, subsequent operation is unpredictable. For example, when transmission or reception is enabled, check that SSISR.IIRQ is 0; when transmission or reception is disabled, check that SSISR.IIRQ is 1.

With this register, select an audio clock, control interrupt requests, select data formats, and set an operation mode.

TEN and REN bits (Transmission and Reception Enable)

These bits enable/disable transmission and reception. When 1 is written to one of these bits, the corresponding communication operation starts in synchronization with a start trigger by the SSILRCK/SSIFS signal. For details, see section 41.8.2 to section 41.8.4. When 0 is written to this bit, the current communication operation stops at the next frame boundary. To use SSIE for both transmission and reception, always write 1 to these bits together. When stopping the communication using SSIE, always disable both transmission and reception (write 0 to the TEN and REN bits).

If you want to stop SSIE before a frame boundary is reached, perform a software reset procedure.

MUEN bit (Mute Enable)

This bit sets/clears the mute function for the data output from the SSITXD0/SSIDATA1 pin. When this bit is set to 1 in the middle of a frame, the SSITXD0/SSIDATA1 output changes to 0 at the next frame boundary. When this bit is set to 0 in the middle of a frame, the SSITXD0/SSIDATA1 output changes to the data of transmit FIFO data register at the next frame boundary. Note that this bit controls data only. Status flags and interrupt signals are normally generated.

Changing the value of this bit must be performed only after setting the communication format to be used.

Bit	Symbol	位名称	Description	R/W
b23, b22	FRM[1:0]	选择帧字数*1		R/W

	通讯格式（SSIOFR.OMOD[1:0]）		
FRM[1:0]	I²S (00b)	Monaural (10b)	TDM (01b)
00b	2	1	禁止设定
01b	禁止设定	禁止设定	4
10b			6
11B			8

b24	—	Reserved	该位读取为0。写入值应为0。	R/W
b25	IIEN	空闲模式中断输出 Enable	0：禁用空闲模式中断输出1：启用空闲模式中断输出。	R/W
b26	ROIEN	接收溢出中断输出使能	0：禁止接收溢出中断输出1：使能接收溢出中断输出。	R/W
b27	RUIEN	接收下溢中断输出使能	0：禁止接收下溢中断输出1：使能接收下溢中断输出。	R/W
b28	TOIEN	发送溢出中断输出使能	0：禁止发送溢出中断输出1：使能发送溢出中断输出。	R/W
b29	TUIEN	发送下溢中断输出使能	0：禁止发送下溢中断输出1：使能发送下溢中断输出。	R/W
b30	CKS	选择一个音频时钟 Master-mode Communication *1	0：选择AUDIO_CLK输入1：选择GTIOC1A（GPT输出）。	R/W
b31	—	Reserved	该位读取为0。写入值应为0。	R/W

Note 1. 禁止在SSIE处于通信状态(SSISR.IIRQ=0)时写入这些位。如果这些位的值通过重写而改变，后续的操作是不可预知的。

Note 2. 如果TEN位或REN位被重写，请确保SSISR.IIRQ位处于所需状态。如果TEN或REN位的值因重写而改变，后续操作将无法预测。例如，启用发送或接收时，检查SSISR.IIRQ是否为0；当发送或接收被禁用时，检查SSISR.IIRQ是否为1。

使用该寄存器，选择音频时钟、控制中断请求、选择数据格式和设置操作模式。

TEN和REN位（发送和接收使能）

这些位启用禁用发送和接收。当这些位之一写入1时，相应的通信操作与SSILRCKSSIFS信号的开始触发同步开始。有关详细信息，请参阅第41.8.2节至第41.8.4节。当向该位写入0时，当前通信操作在下一帧边界处停止。要同时使用SSIE进行发送和接收，请始终将1一起写入这些位。使用SSIE停止通信时，始终禁用发送和接收（将0写入TEN和REN位）。

如果要在达到帧边界之前停止SSIE，请执行软件复位程序。

MUEN位（静音使能）

该位设置清除SSITXD0SSIDATA1引脚数据输出的静音功能。当该位在帧中间设置为1时，SSITXD0SSIDATA1输出在下一帧边界变为0。当该位在帧中间设置为0时，SSITXD0SSIDATA1输出在下一帧边界变为发送FIFO数据寄存器的数据。请注意，该位仅控制数据。通常会产生状态标志和中断信号。

只有在设置要使用的通信格式后才能更改该位的值。

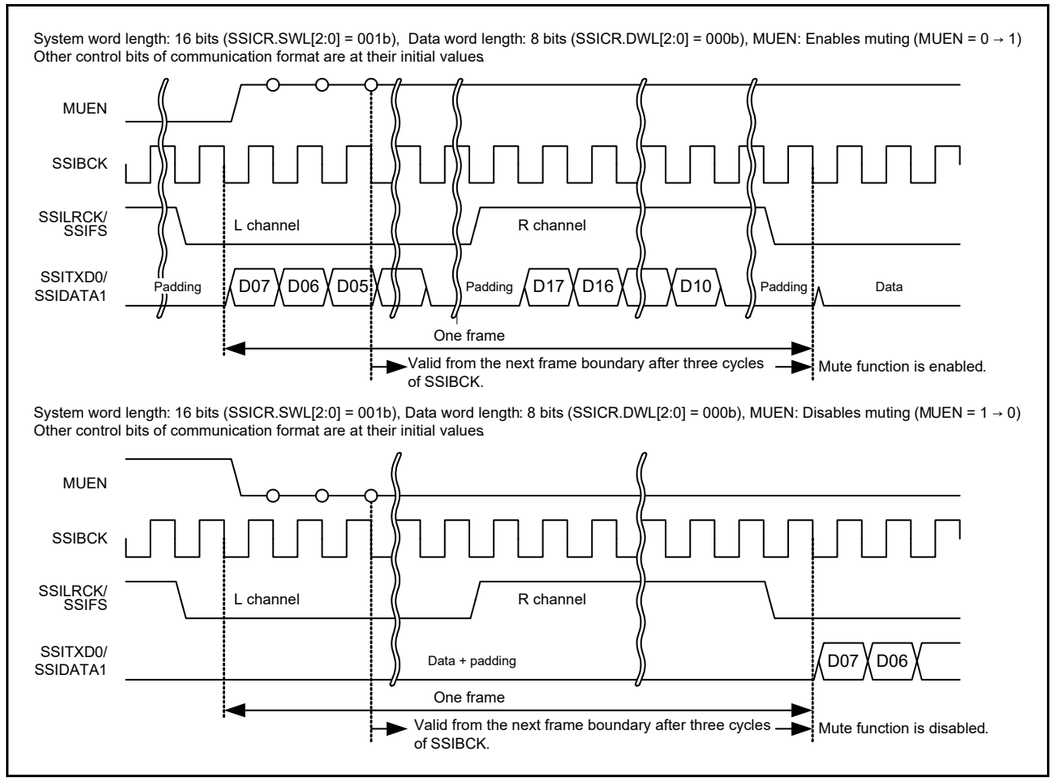


Figure 41.5 Transmit data with the mute function set

CKDV[3:0] bits (Selects Bit Clock Division Ratio)

These bits set the division ratio of the bit clock based on AUDIO_MCK in master-mode communication (MST = 1). In slave-mode communication (MST = 0), setting of these bits are invalid.

Writing to this bit must be performed when the supply of AUDIO_MCK is stopped. For details about the timing, see the detailed description of the AUCKE bit in SSIFCR.

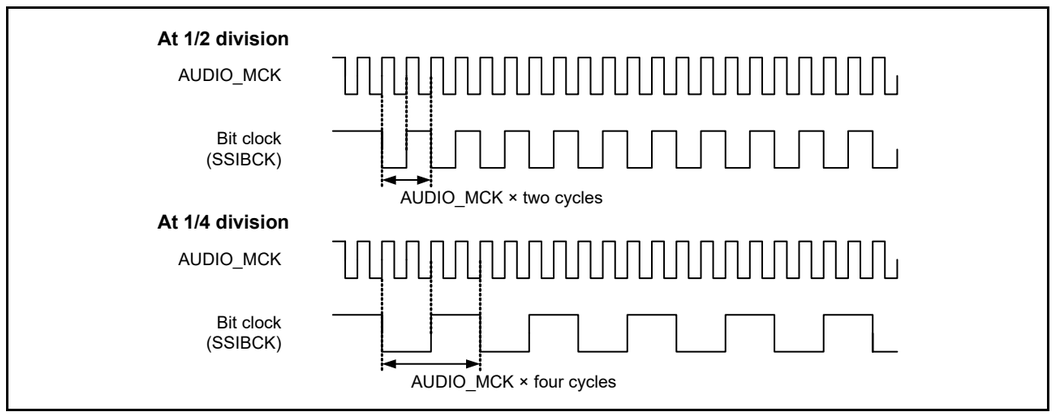


Figure 41.6 Sampling frequencies in master-mode communication

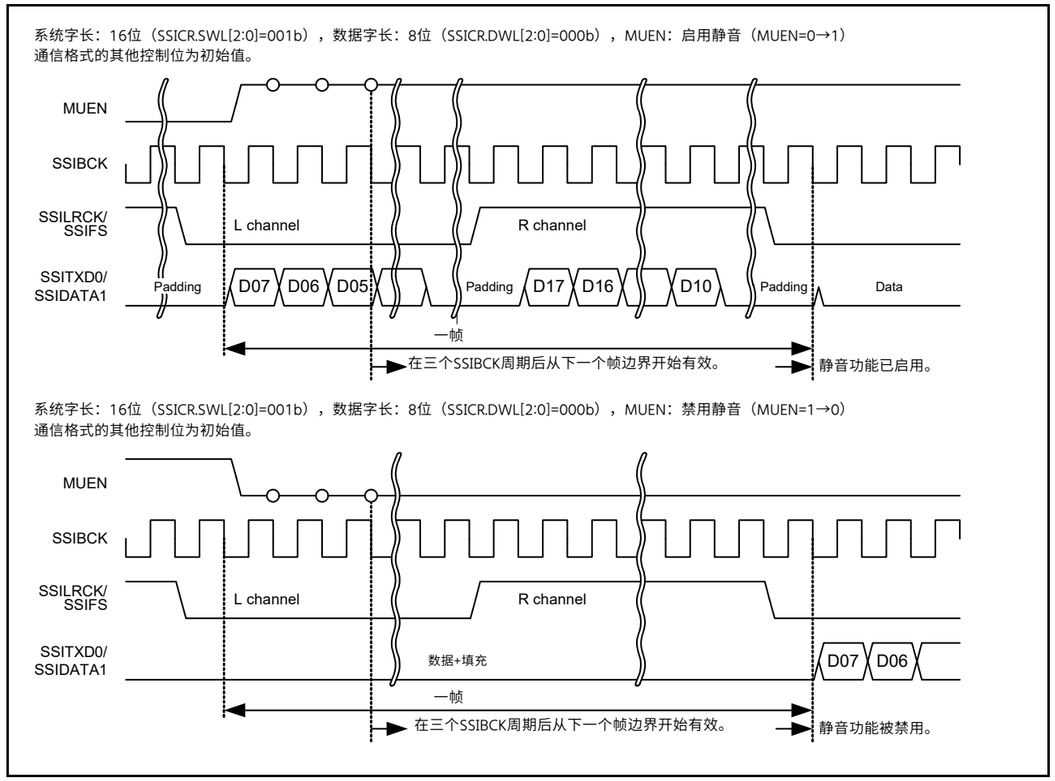


Figure 41.5 设置静音功能传输数据

CKDV[3:0]位（选择位时钟分频比）

这些位在主模式通信(MST=1)中根据AUDIO_MCK设置位时钟的分频比。在从机模式通信(MST=0)中，这些位的设置无效。

当停止提供AUDIO_MCK时，必须执行写入该位。有关时序的详细信息，请参见SSIFCR中AUCKE位的详细说明。

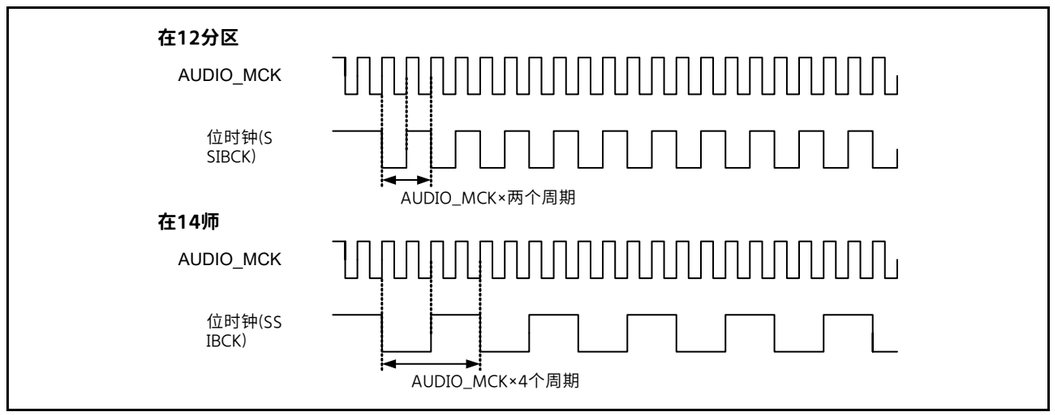


Figure 41.6 主模式通信中的采样频率

DEL bit (Selects Serial Data Delay)

This bit sets whether or not there will be a delay between SSILRCK/SSIFS and SSITXD0/SSIRXD0/SSIDATA1.

For the I²S or TDM format, set the DEL bit to 0. When the monaural format is used, setting of this bit changes the high period width of SSILRCK/SSIFS. For details, see section 41.5.2, Monaural Format. When using a compatible communication format, specify a setting of this bit that enables communication.

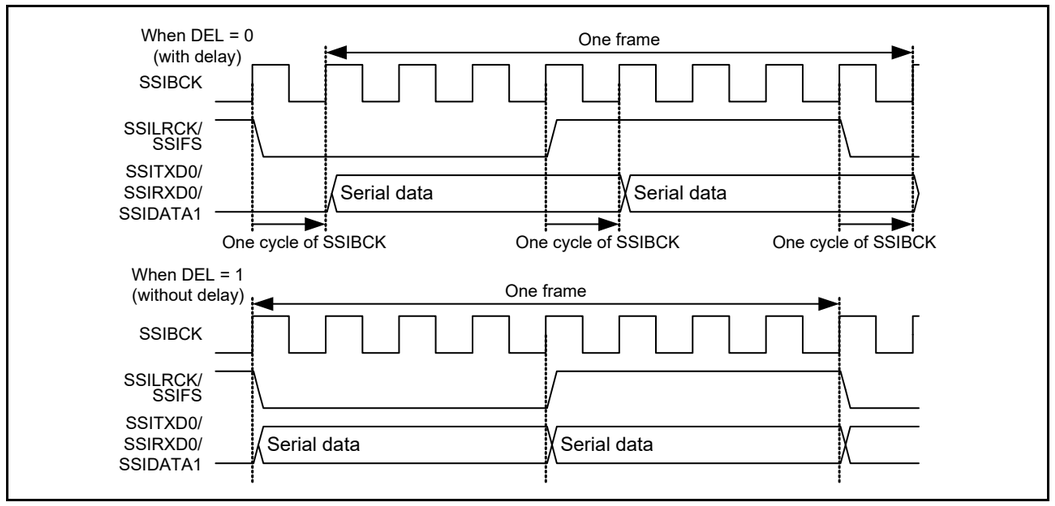


Figure 41.7 Setting of delay in serial data

PDTA bit (Selects Placement Data Alignment)

This bit sets how to align placement data. With the setting of data word length as 32 bits (SSICR.DWL[2:0] = 110b), this bit is invalid.

At transmission, see Figure 41.8.

DEL位（选择串行数据延迟）

该位设置SSILRCKSSIFS和SSITXD0SSIRXD0SSIDATA1之间是否会有延迟。

对于I2S或TDM格式，将DEL位设置为0。当使用单声道格式时，该位的设置会改变SSILRCKSSIFS的高周期宽度。有关详细信息，请参阅第41.5.2节，单声道格式。使用兼容的通信格式时，指定该位的设置以启用通信。

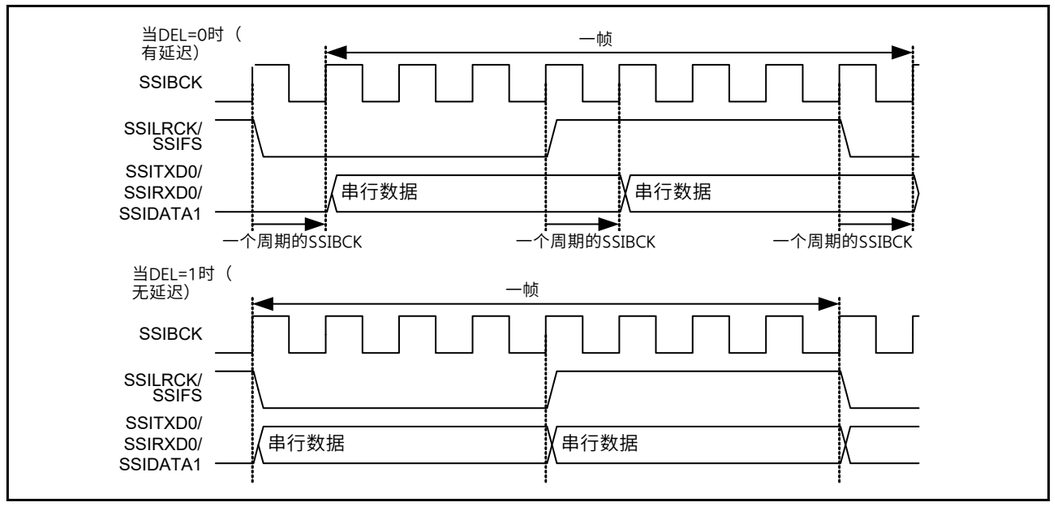


Figure 41.7 串行数据延迟设置

PDTA位（选择布局数据对齐）

该位设置如何对齐布局数据。数据字长设置为32位（SSICR.DWL[2:0]=110b）时，该位无效。

传输时，见图41.8。

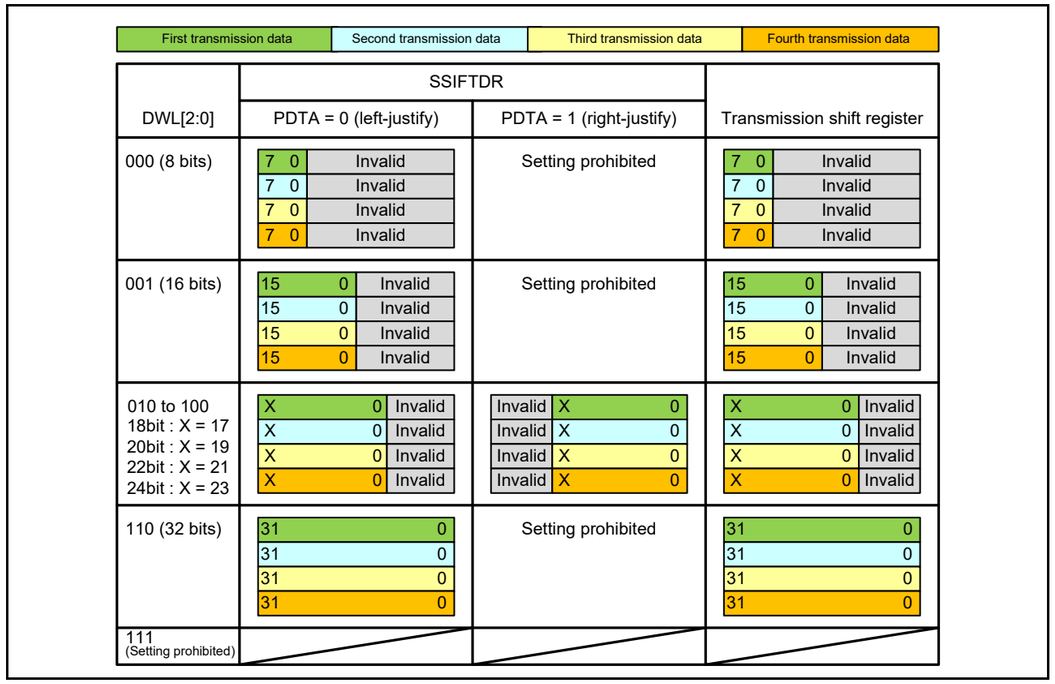


Figure 41.8 Alignment of placement data at transmission

At reception, see Figure 41.9.

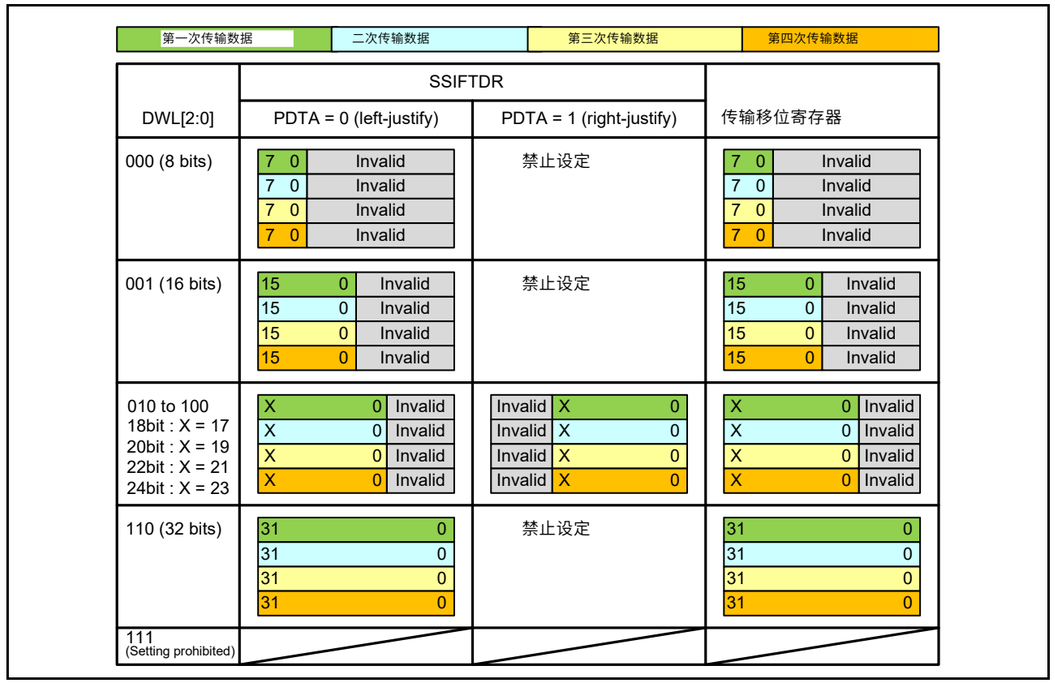


Figure 41.8 在传输时对齐放置数据

在接待处，见图41.9。

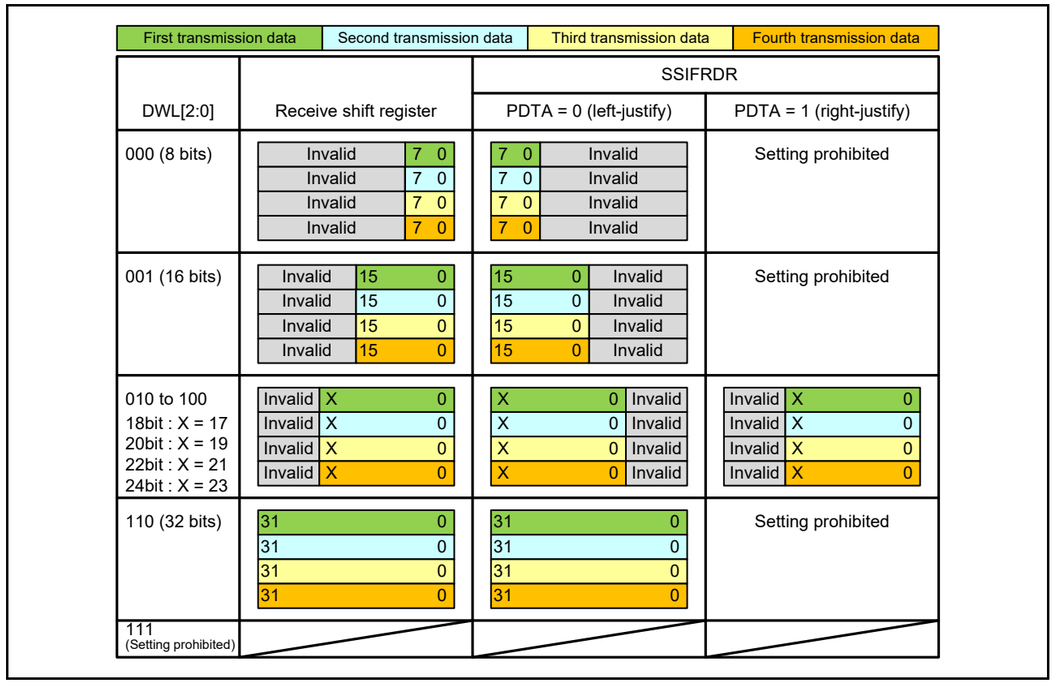


Figure 41.9 Alignment of placement data at reception

SDTA bit (Selects Serial Data Delay)

This bit sets how to align serial data and padding bits. For communication without padding bits, this bit is invalid.

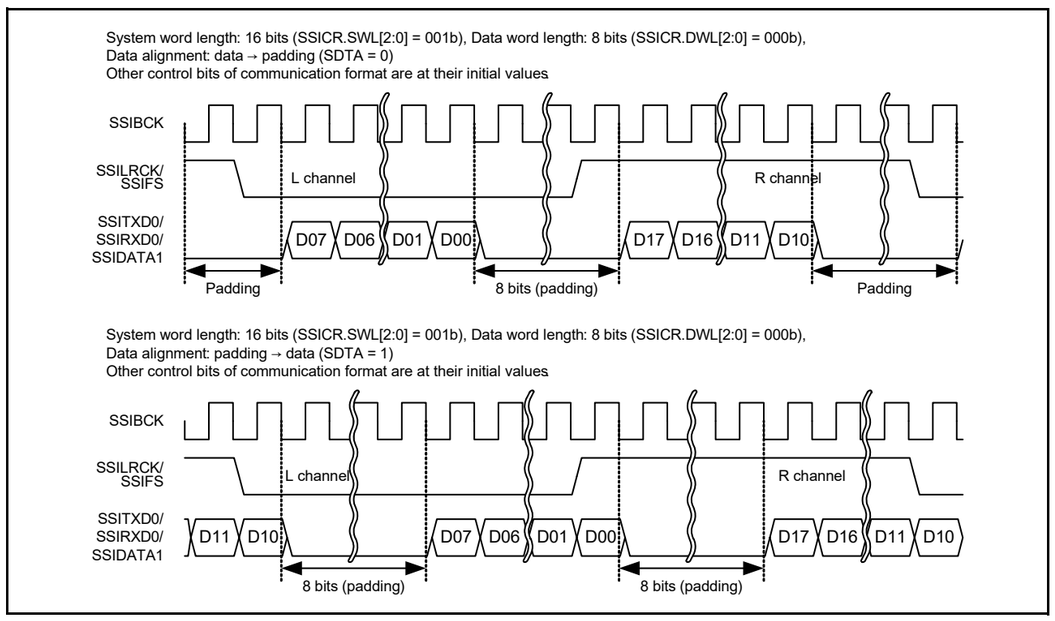


Figure 41.10 Alignment setting of serial data with padding bits

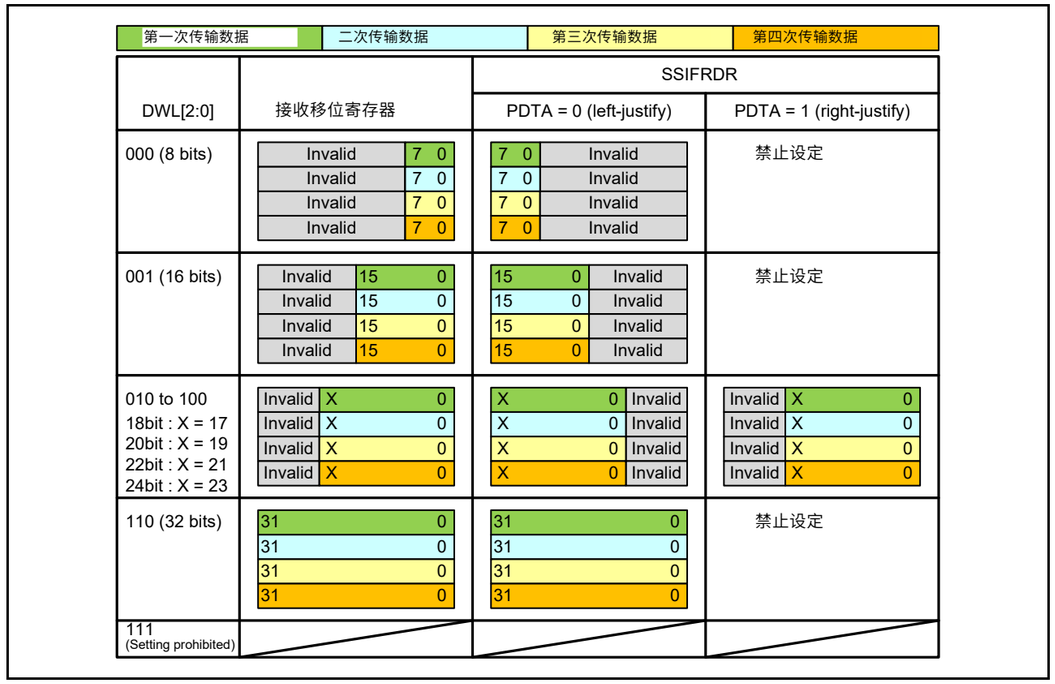


Figure 41.9 在接收时对齐放置数据

SDTA位（选择串行数据延迟）

该位设置如何对齐串行数据和填充位。对于没有填充位的通信，该位无效。

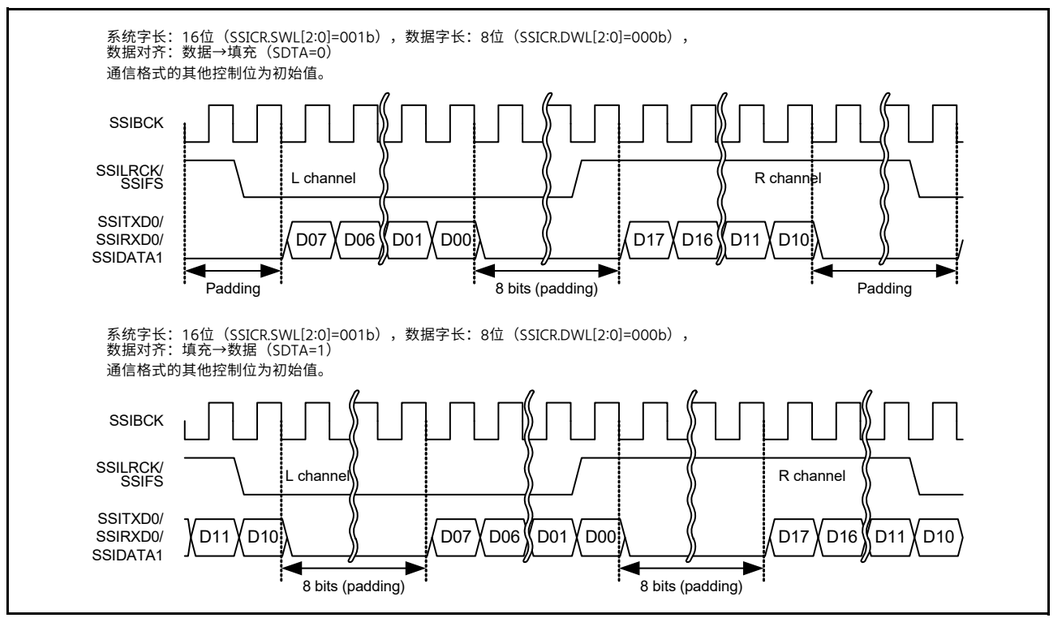


Figure 41.10 串行数据的对齐设置与填充位

SPDP bit (Selects Serial Padding Polarity)

This bit sets polarity of padding bits.

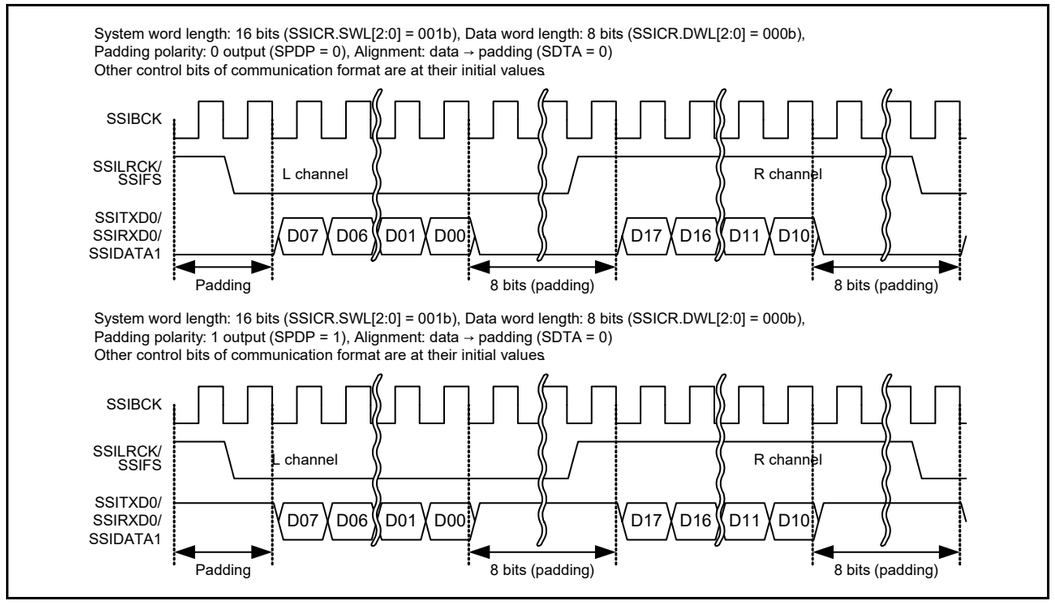


Figure 41.11 Padding bit polarity

LRCKP bit (Selects the Initial Value and Polarity of LR Clock/Frame Synchronization Signal)

This bit sets the initial value and polarity of SSILRCK/SSIFS. Set this bit according to the communication format to be used in SSIE. See Table 41.3 Initial output value and polarity of SSILRCK/SSIFS pin. For the slave-mode communication (MST = 0), only the start trigger is used.

Writing to these bits must be performed when the LR clock supply to the SSILRCK/SSIFS pin is stopped. For details about the output of LR clock, see the detailed description of the LRCONT bit in SSIOFR.

Table 41.3 Initial output value and polarity of SSILRCK/SSIFS pin

Communication Format	Expected Initial State	Setting Value of LRCKP
I^2S	High	0
Monaural	Low	1
TDM	Low	1

Note: When the format to be used is compatible with the I^2S, monaural, or TDM format, specify settings to enable communication with the respective formats.

SPDP位（选择串行填充极性）

该位设置填充位的极性。

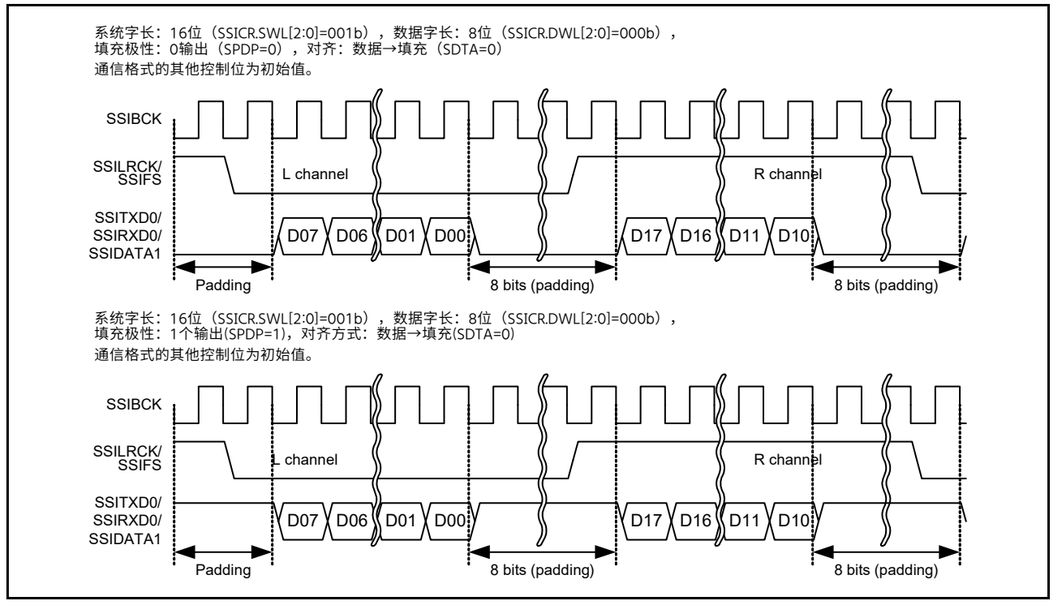


Figure 41.11 填充位极性

LRCKP位（选择LR时钟帧同步信号的初始值和极性）

该位设置SSILRCKSSIFS的初始值和极性。根据要在SSIE中使用的通信格式设置该位。请参见表41.3SSILRCKSSIFS引脚的初始输出值和极性。对于从模式通信(MST=0)，仅使用启动触发器。

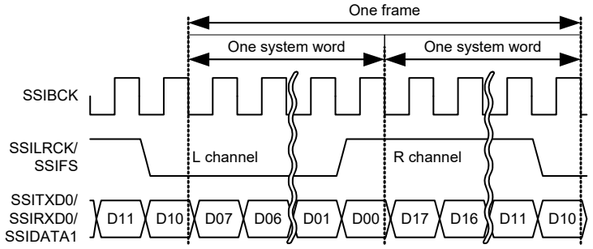
当向SSILRCKSSIFS引脚提供LR时钟停止时，必须执行写入这些位。LR时钟的输出详见SSIOFR中LRCONT位的详细说明。

Table 41.3 SSILRCKSSIFS管脚的初始输出值和极性

通讯格式	预期的初始状态	LRCKP设定值
I^2S	High	0
Monaural	Low	1
TDM	Low	1

Note: 当要使用的格式与I2S、单声道或TDM格式兼容时，指定设置以启用与相应格式的通信。

System word length: 8 bits (SSICR.SWL[2:0] = 000b), Data word length: 8 bits (SSICR.DWL[2:0] = 000b),
LR clock polarity: L channel = Low, R channel = High (LRCKP = 0)
Other control bits of communication format are at their initial values.



System word length: 8 bits (SSICR.SWL[2:0] = 000b), Data word length: 8 bits (SSICR.DWL[2:0] = 000b),
LR clock polarity: L channel = High, R channel = Low (LRCKP = 1)
Other control bits of communication format are at their initial values.

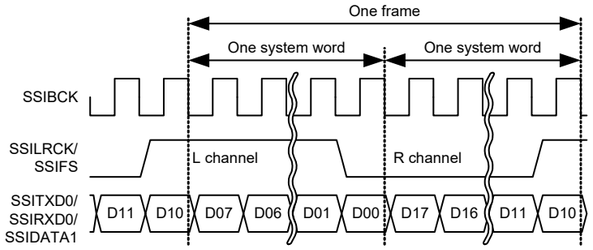


Figure 41.12 LR clock/frame synchronization polarity setting

BCKP bit (Selects Bit Clock Polarity)

This bit sets the bit clock polarity.

Writing to this bit must be performed when the supply of AUDIO_MCK is stopped. For details about the timing, see the detailed description of the AUCKE bit in section 41.4.3, FIFO Control Register (SSIFCR).

Table 41.4 Bit clock polarity

Communication	Master/Slave	Timing	BCKP = 0	BCKP = 1
Reception	Slave	At SSILRCK/SSIFS sampling	SSIBCK rising edge	SSIBCK falling edge
	Master/slave	At SSIRXD0/SSIDATA1 sampling	SSIBCK rising edge	SSIBCK falling edge
Transmission	Master	At change of SSILRCK/SSIFS output	SSIBCK falling edge	SSIBCK rising edge
	Master/slave	At change of SSITXD0/SSIDATA1 output	SSIBCK falling edge	SSIBCK rising edge

MST bit (Master Enable)

This bit sets master-/slave-mode communication.

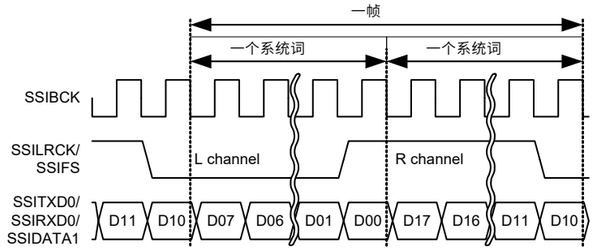
Writing to this bit must be performed when the supply of AUDIO_MCK is stopped. For details about the timing, see the detailed description of the AUCKE bit in section 41.4.3, FIFO Control Register (SSIFCR).

SWL[2:0] bits (Selects System Word Length)

These bits set the number of bits in one system word. Padding bits are sent and received in relation with one data word set with DWL[2:0]. See Table 41.11 for details.

Writing to these bits must be performed when the LR clock supply to the SSILRCK/SSIFS pin is stopped. For details about the output of LR clock, see the detailed description of the LRCONT bit in section 41.4.7, Audio Format Register (SSIOFR).

系统字长：8位（SSICR.SWL[2:0]=000b），数据字长：8位（SSICR.DWL[2:0]=000b），
LR时钟极性：L通道=低，R通道=高（LRCKP=0）通信格式的其他控
制位为其初始值。



系统字长：8位（SSICR.SWL[2:0]=000b），数据字长：8位（SSICR.DWL[2:0]=000b），
LR时钟极性：L通道=高，R通道=低（LRCKP=1）通信格式的其他控
制位为其初始值。

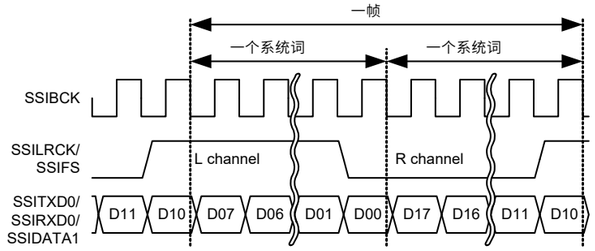


Figure 41.12 LR时钟帧同步极性设置

BCKP位（选择位时钟极性）

该位设置位时钟极性。

当停止提供AUDIO_MCK时，必须执行写入该位。有关时序的详细信息，请参见第41.4.3节FIFO控制寄存器(SSIFCR)中对AUCKE位的详细说明。

Table 41.4 位时钟极性

Communication	Master/Slave	Timing	BCKP = 0	BCKP = 1
Reception	Slave	在SSILRCKSSIFS采样	SSIBCK上升沿	SSIBCK下降沿
	Master/slave	在SSIRXD0SSIDATA1采样	SSIBCK上升沿	SSIBCK下降沿
Transmission	Master	在改变SSILRCKSSIFS输出时	SSIBCK下降沿	SSIBCK上升沿
	Master/slave	在SSITXD0SSIDATA1输出变化时	SSIBCK下降沿	SSIBCK上升沿

MST位（主使能）

该位设置主从模式通信。

当停止提供AUDIO_MCK时，必须执行写入该位。有关时序的详细信息，请参见第41.4.3节FIFO控制寄存器(SSIFCR)中对AUCKE位的详细说明。

SWL[2:0]位（选择系统字长）

这些位设置一个系统字中的位数。填充位的发送和接收与使用DWL[2:0]设置的一个数据字相关。详见表41.11
。

当向SSILRCKSSIFS引脚提供LR时钟停止时，必须执行写入这些位。关于LR时钟输出的详细信息，请参见第41.4
.7节，音频格式寄存器(SSIOFR)中对LRCONT位的详细说明。

DWL[2:0] bits (Selects Data Word Length)

These bits set the number of bits in one data word. The data word length (number of bits per data word) must not exceed the system word length (number of bits per system word). For details, see Table 41.11.

FRM[1:0] bits (Selects Frame Word Number)

These bits set the frame word number in individual communication formats.

Writing to these bits must be performed when the LR clock supply to the SSILRCK/SSIFS pin is stopped. For details about the output of LR clock, see the detailed description of the LRCONT bit in SSIOFR.

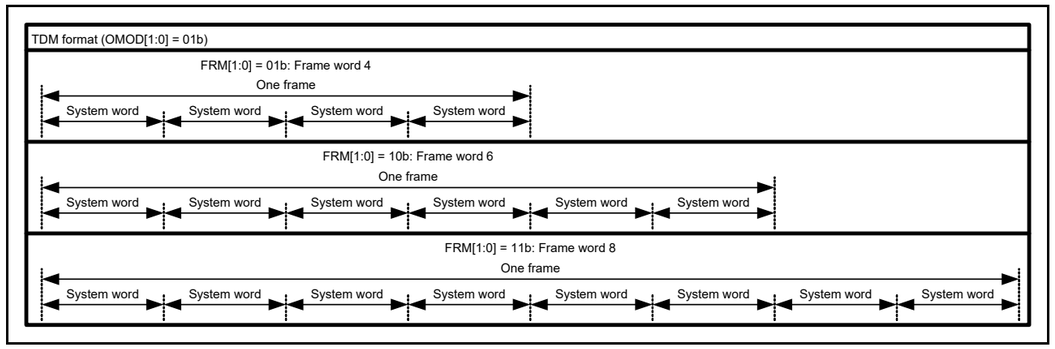


Figure 41.13 Frame word number

IIEN bit (Idle Mode Interrupt Output Enable)

This bit enables/disables output of idle mode interrupts. By enabling this bit (set it to 1), an interrupt is output at a rising edge of SSISR.IIRQ = 1. An interrupt is also output when this bit is changed from 0 to 1 while SSISR.IIRQ = 1.

ROIEN bit (Receive Overflow Interrupt Output Enable)

This bit enables/disables output of receive overflow interrupts. By enabling this bit (set it to 1), an interrupt is output at a rising edge of SSISR.ROIRQ = 1. An interrupt is also output when this bit is changed from 0 to 1 while SSISR.ROIRQ = 1.

RUIEN bit (Receive Underflow Interrupt Output Enable)

This bit enables/disables output of receive underflow interrupts. By enabling this bit (set it to 1), an interrupt is output at a rising edge of SSISR.RUIRQ = 1. An interrupt is also output when this bit is changed from 0 to 1 while SSISR.RUIRQ = 1.

TOIEN bit (Transmit Overflow Interrupt Output Enable)

This bit enables/disables output of transmit overflow interrupts. By enabling this bit (set it to 1), an interrupt is output at a rising edge of SSISR.TOIRQ = 1. An interrupt is also output when this bit is changed from 0 to 1 while SSISR.TOIRQ = 1.

TUIEN bit (Transmit Underflow Interrupt Output Enable)

This bit enables/disables output of transmit underflow interrupts. By enabling this bit (set it to 1), an interrupt is output at a rising edge of SSISR.TUIRQ = 1. An interrupt is also output when this bit is changed from 0 to 1 while SSISR.TUIRQ = 1.

CKS bit (Selects an Audio Clock for Master-mode Communication)

This bit sets the audio clock in master-mode communication (MST = 1). In slave-mode communication (MST = 0), setting of this bit is invalid.

Writing to this bit must be performed when the supply of AUDIO_MCK is stopped. For details about the timing, see the detailed description of the AUCKE bit in SSIFCR.

DWL[2:0]位（选择数据字长）

这些位设置一个数据字中的位数。数据字长（每个数据字的位数）不得超过系统字长（每个系统字的位数）。详见表41.11。

FRM[1:0]位（选择帧字号）

这些位设置各个通信格式中的帧字号。

当向SSILRCKSSIFS引脚提供LR时钟停止时，必须执行写入这些位。LR时钟的输出详见SSIOFR中LRCONT位的详细说明。

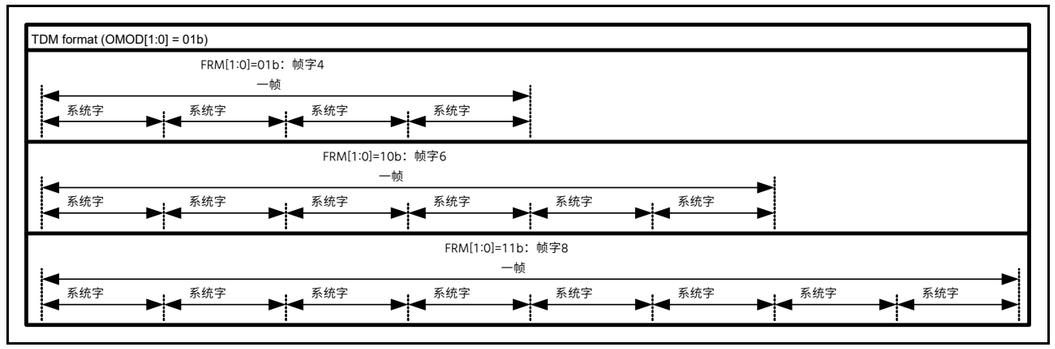


Figure 41.13 帧字数

IIEN位（空闲模式中断输出使能）

该位使能禁用空闲模式中断的输出。通过启用该位（将其设置为1），在SSISR.IIRQ=1的上升沿输出中断。当SSISR.IIRQ=1时该位从0变为1时也会输出中断。

ROIEN位（接收溢出中断输出使能）

该位使能禁止接收溢出中断的输出。通过启用该位（将其设置为1），在SSISR.ROIRQ=1的上升沿输出中断。当SSISR.ROIRQ=1时该位从0变为1时也会输出中断。

RUIEN位（接收下溢中断输出使能）

该位使能禁用接收下溢中断的输出。通过启用该位（将其设置为1），在SSISR.RUIRQ=1的上升沿输出中断。当SSISR.RUIRQ=1时该位从0变为1时也会输出中断。

TOIEN位（发送溢出中断输出使能）

该位使能禁用发送溢出中断的输出。通过启用该位（将其设置为1），在SSISR.TOIRQ=1的上升沿输出中断。当SSISR.TOIRQ=1时该位从0变为1时也会输出中断。

TUIEN位（发送下溢中断输出使能）

该位使能禁用发送下溢中断的输出。通过启用该位（将其设置为1），在SSISR.TUIRQ=1的上升沿输出中断。当SSISR.TUIRQ=1时该位从0变为1时也会输出中断。

CKS位（选择主模式通信的音频时钟）

该位设置主模式通信（MST=1）中的音频时钟。在从机模式通信(MST=0)中，该位的设置无效。

当停止提供AUDIO_MCK时，必须执行写入该位。有关时序的详细信息，请参见SSIFCR中AUCKE位的详细说明。

41.4.2 Status Register (SSISR)

Address(es): SSIE0.SSISR 4004 E004h, SSIE1.SSISR 4004 E104h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	TUIRQ	TOIRQ	RUIRQ	ROIRQ	IIRQ	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b24 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b25	IIRQ	Idle Mode Status Flag	0: In the communication state 1: In the idle state.	R
b26	ROIRQ	Receive Overflow Error Status Flag	0: No receive overflow error is generated 1: A receive overflow error is generated.	R/W
b27	RUIRQ	Receive Underflow Error Status Flag	0: No receive underflow error is generated 1: A receive underflow error is generated.	R/W
b28	TOIRQ	Transmit Overflow Error Status Flag	0: No transmit overflow error is generated 1: A transmit overflow error is generated.	R/W
b29	TUIRQ	Transmit Underflow Error Status flag	0: No transmit underflow error is generated 1: A transmit underflow error is generated.	R/W
b31, b30	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

This register is configured with status flags that indicate SSIE operational state.

IIRQ bit (Idle Mode Status Flag)

This is a status flag that indicates the idle state. It indicates whether SSIE is in the idle state or communication state.

For details, see Figure 41.14 and Figure 41.15.

41.4.2 状态寄存器(SSISR)

Address(es): SSIE0.SSISR 4004 E004h, SSIE1.SSISR 4004 E104h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	TUIRQ	TOIRQ	RUIRQ	ROIRQ	IIRQ	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b24 to b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b25	IIRQ	空闲模式状态标志	0：处于通信状态1：处于空闲状态。	R
b26	ROIRQ	接收溢出错误状态Flag	0：不产生接收溢出错误1：产生接收溢出错误。	R/W
b27	RUIRQ	接收下溢错误状态Flag	0：不产生接收下溢错误1：产生接收下溢错误。	R/W
b28	TOIRQ	发送溢出错误状态Flag	0：不产生发送溢出错误1：产生发送溢出错误。	R/W
b29	TUIRQ	发送下溢错误状态标志	0：不产生发送下溢错误1：产生发送下溢错误。	R/W
b31, b30	—	Reserved	这些位被读取为0。写入值应为0。	R/W

该寄存器配置有指示SSIE操作状态的状态标志。

IIRQ位（空闲模式状态标志）

这是指示空闲状态的状态标志。它指示SSIE是处于空闲状态还是通信状态。

详见图41.14和图41.15。

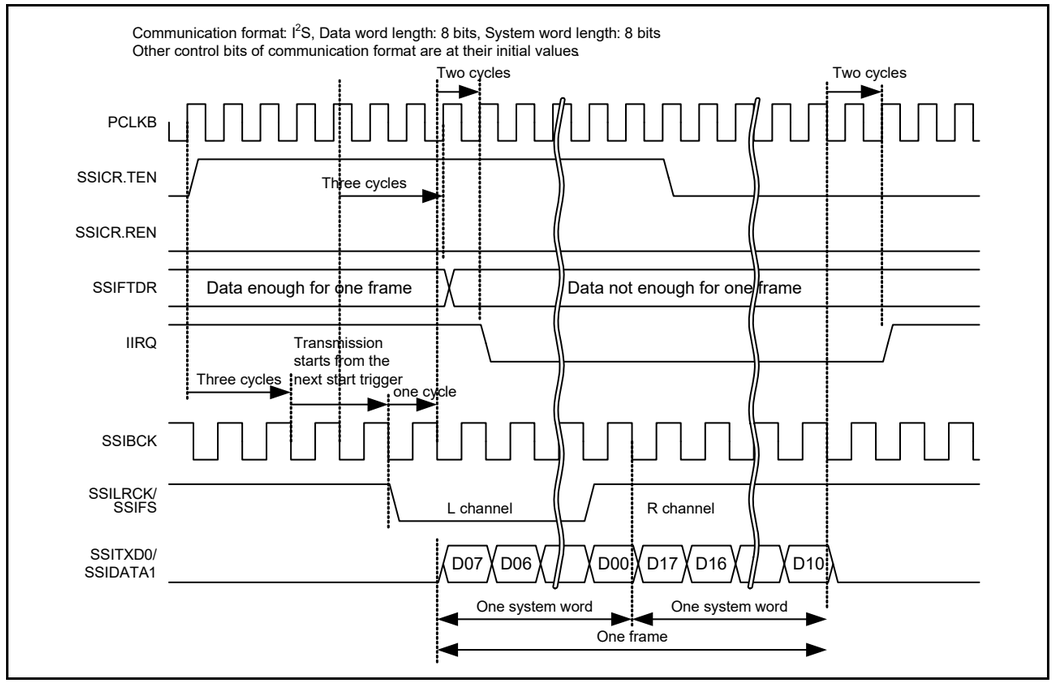


Figure 41.14 IIRQ setting timing (transmission)

- Transmitter (dedicated to transmission)

[Clearing condition]

While transmission was enabled (SSICR.TEN = 1 and SSICR.REN = 0), the transmit data for a transmission frame was written to the SSIFTDR register, and a start trigger was generated by the SSILRCK/SSIFS signal.

[Clearing timing]

1 SSIBCK cycle + 2 PCLKB cycles after generation of the start trigger that is the clearing condition.

[Setting condition]

While transmission and reception were disabled (SSICR.TEN = 0 and SSICR.REN = 0), transmission of one frame was complete.

[Setting timing]

2 PCLKB cycles after the end of transmission (at a frame boundary) that is the setting condition.

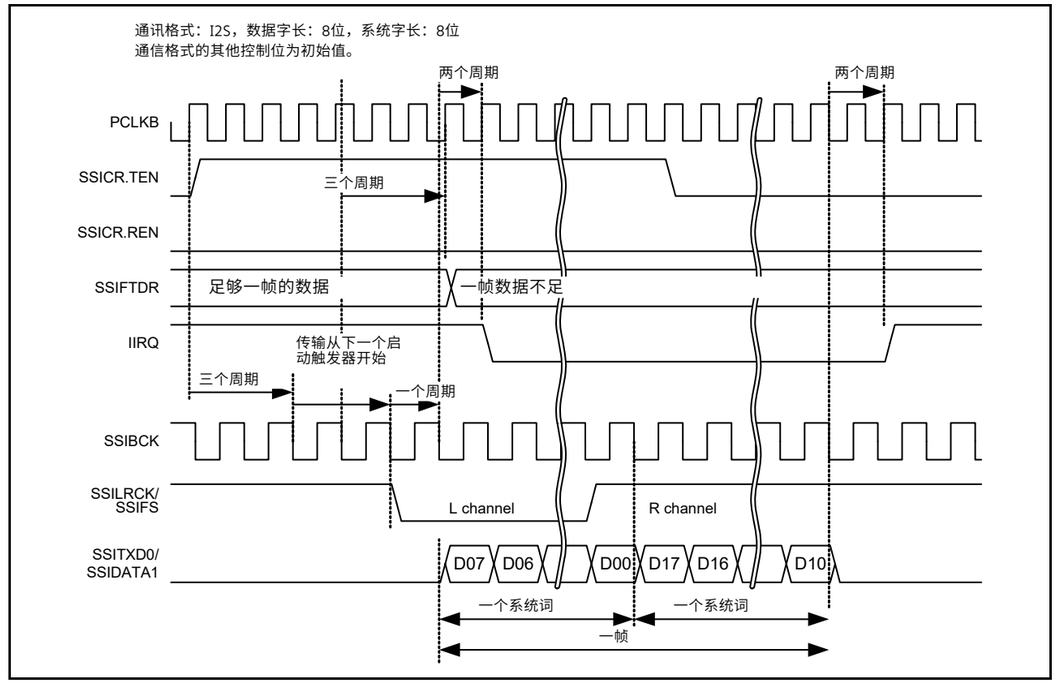


Figure 41.14 IIRQ设置时序（传输）

- 发射器（专用于传输）

[Clearing condition]

启用传输时（SSICR.TEN=1和SSICR.REN=0），传输帧的传输数据被写入SSIFTDR寄存器，并由SSILRCKSSIFS信号生成启动触发。

[Clearing timing]

1个SSIBCK周期+2个PCLKB周期在产生作为清除条件的启动触发之后。

[Setting condition]

当发送和接收被禁用时（SSICR.TEN=0和SSICR.REN=0），一帧的发送完成。

[Setting timing]

在作为设置条件的传输结束后（在帧边界处）的2个PCLKB周期。

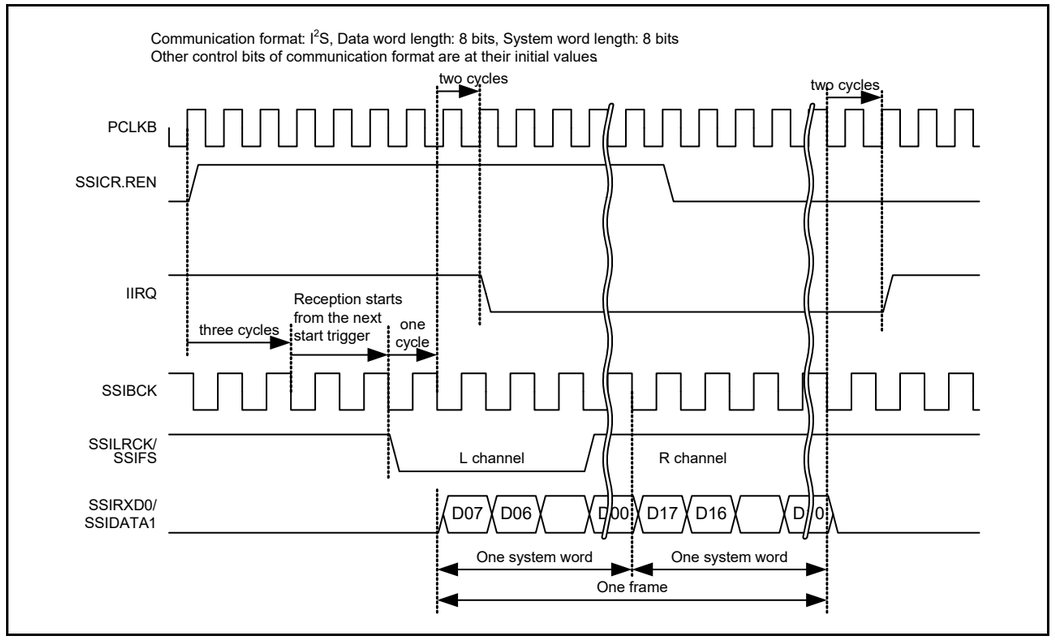


Figure 41.15 IIRQ setting timing (reception)

- Receiver (dedicated to reception)

[Clearing condition]

While reception was enabled (SSICR.TEN = 0 and SSICR.REN = 01, a start trigger was generated by the SSILRCK/SSIFS signal.

[Clearing timing]

1 SSIBCK cycle + 2 PCLKB cycles after generation of the start trigger that is the clearing condition.

[Setting condition]

While transmission and reception were disabled (SSICR.TEN = 0 and SSICR.REN = 0), reception of one frame was complete.

[Setting timing]

2 PCLKB cycles after the end of reception (at a frame boundary) that is the setting condition.

- Transceiver (transmission and reception)

[Clearing condition]

While transmission and reception were enabled (SSICR.TEN = 1 and SSICR.REN = 1), the transmit data for a transmission frame was written to the SSIFTDR register, and a start trigger is generated by the SSILRCK/SSIFS signal.

[Clearing timing]

1 SSIBCK cycle + 2 PCLKB cycles after generation of the start trigger that is the clearing condition.

[Setting condition]

While transmission and reception were disabled (SSICR.TEN = 0 and SSICR.REN = 0), transmission of one frame was complete.

[Setting timing]

2 PCLKB cycles after the end of transmission (at a frame boundary) that is the setting condition.

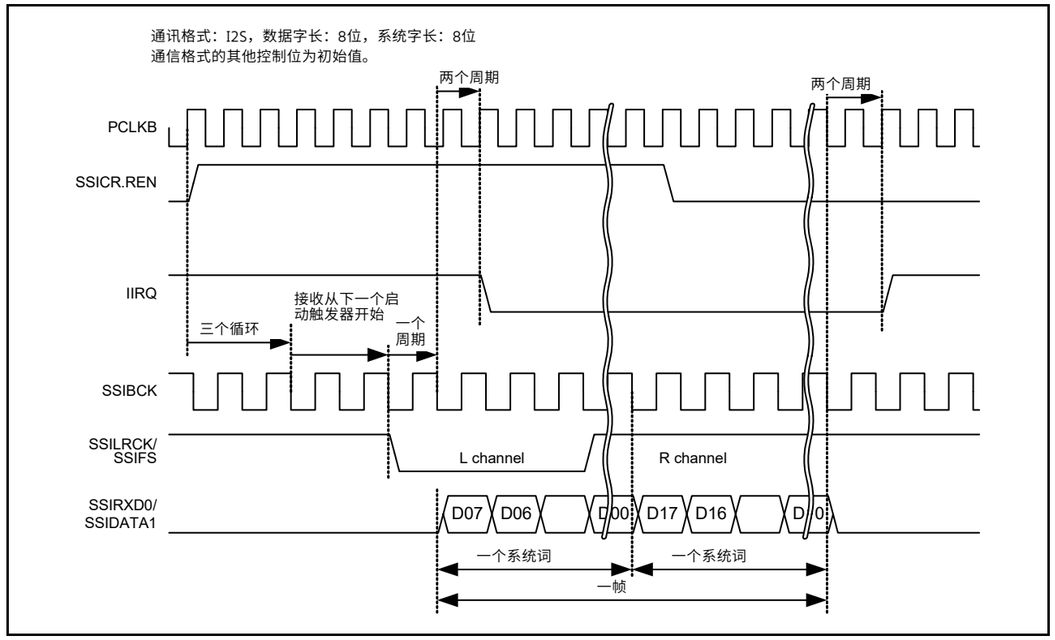


Figure 41.15 IIRQ设置时序（接收）

- 接收器（专用于接收）

[Clearing condition]

启用接收时（SSICR.TEN=0和SSICR.REN=01，启动触发由
SSILRCK/SSIFS signal.

[Clearing timing]

1个SSIBCK周期+2个PCLKB周期在产生作为清除条件的启动触发之后。

[Setting condition]

当发送和接收被禁用时（SSICR.TEN=0和SSICR.REN=0），一帧的接收完成。

[Setting timing]

在作为设置条件的接收结束（在帧边界）之后的2个PCLKB周期。

- 收发器（发送和接收）

[Clearing condition]

在使能发送和接收时（SSICR.TEN=1和SSICR.REN=1），发送帧的发送数据被写入SSIFTDR寄存器，并由SSILRC KSSIFS信号生成开始触发。

[Clearing timing]

1个SSIBCK周期+2个PCLKB周期在产生作为清除条件的启动触发之后。

[Setting condition]

当发送和接收被禁用时（SSICR.TEN=0和SSICR.REN=0），一帧的发送完成。

[Setting timing]

在作为设置条件的传输结束后（在帧边界处）的2个PCLKB周期。

ROIRQ bit (Receive Overflow Error Status Flag)

This is a status flag that indicates a receive overflow error. This flags is set by automatic determination but it must be cleared by register access. This flag indicates that received data is supplied at a higher rate than requested. Data is not transferred from the receive shift register to SSIFRDR where a receive overflow error is generated. For the procedure to recover from the overflow error, see section 41.8.6, Error Handling. This flag is not cleared by a receive FIFO data register reset (SSIFCR.RFRST).

[Priority order for setting and clearing]

Setting is prioritized.*1

[Clearing condition]

When either of the following operations is done:

1. Writing 0 to this bit after reading 1 from this bit*2
2. Enabling communication (changing SSICR.REN from 0 to 1).

[Clearing timing]

Clearing timing corresponding to the above clearing condition:

1. When 0 is written to this bit after reading 1 from this bit (same as the timing in Figure 41.19)
2. 1 PCLKB cycle after writing 1 to SSICR.REN.*3

Note 1. This bit is cleared by a software reset (SSIFCR.SSIRST = 1). The software reset has priority over all the clearing conditions described above.
Note 2. After reading 1 from this bit, this bit is cleared when one of the following three conditions is met:
- A software reset (SSIFCR.SSIRST = 1) is done.
- After 1 has been read, writing of 0 is complete.
- 1 PCLKB cycle passes after 1 has been written to SSICR.REN.
Note 3. After communication is enabled (by changing the value of SSICR.REN bit from 0 to 1), the reception error flags (RUIRQ and ROIRQ in the SSISR register) are cleared. If, however, the SSISR register is read continuously, the cleared status of the reception error flags might be unable to be read.

[Setting condition]

At completion of receiving new data while SSIFRDR is full.

[Setting timing]

3 cycles of PCLKB after reception is completed.

ROIRQ位（接收溢出错误状态标志）

这是指示接收溢出错误的状态标志。该标志由自动确定设置，但必须通过寄存器访问清除。该标志表示接收到的数据以高于请求的速率提供。数据不会从接收移位寄存器传送到产生接收溢出错误的SSIFRDR。有关从溢出错误中恢复的过程，请参阅第41.8.6节，错误处理。该标志不会被接收FIFO数据寄存器复位(SSIFCR.RFRST)清除。

[设置和清除的优先顺序]

设置优先。*1

[Clearing condition]

完成以下任一操作时：

1. 从该位读取1后向该位写入0*2
2. 启用通信（将SSICR.REN从0更改为1）。

[Clearing timing]

与上述清零条件对应的清零时机：

1. 当从该位读取1后向该位写入0时（与图41.19中的时序相同）
2. 向SSICR.REN写入1后的1个PCLKB周期。*3

注1.该位通过软件复位(SSIFCR.SSIRST=1)清零。软件复位优先于上述所有清除条件。注2.从该位读取1后，当满足以下三个条件之一时，该位被清除：软件复位(SSIFCR.SSIRST=1)完成。读取1后，写入0完成。在将1写入SSICR.REN后经过1个PCLKB周期。注3.使能通信后（通过将SSICR.REN位的值从0更改为1），接收错误标志（SSISR寄存器中的RUIRQ和ROIRQ）被清除。但是，如果连续读取SSISR寄存器，则可能无法读取接收错误标志的清除状态。

[Setting condition]

在SSIFRDR已满时完成接收新数据。

[Setting timing]

接收完成后的3个PCLKB周期。

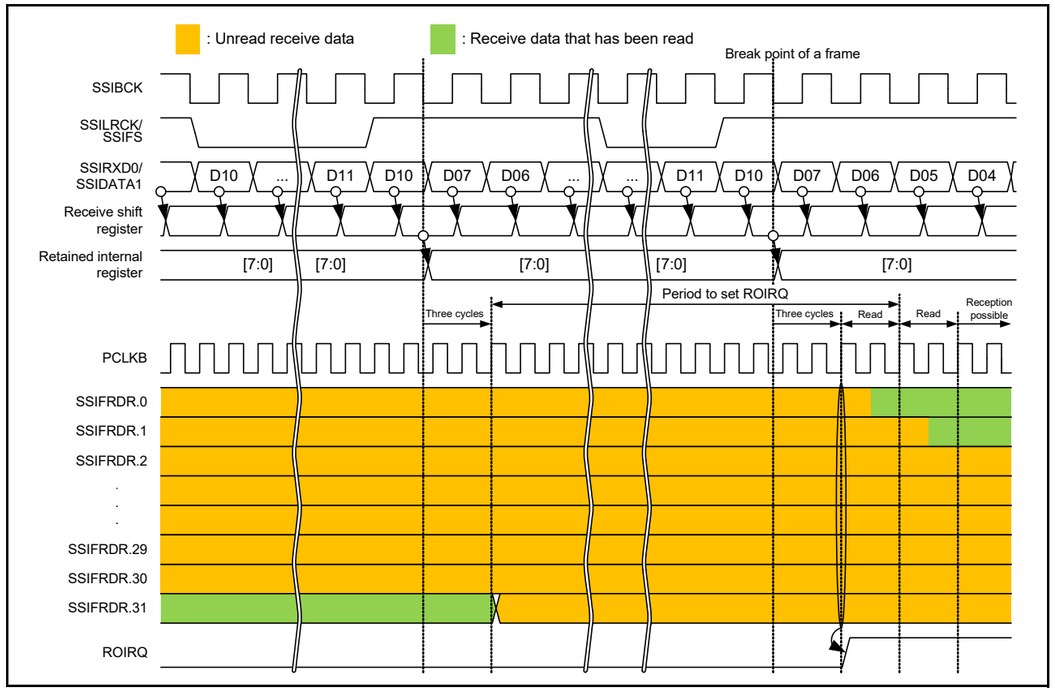


Figure 41.16 ROIRQ setting timing

RUIRQ bit (Receive Underflow Error Status Flag)

This is a status flag that indicates a receive underflow error. This flags is set by automatic determination but it must be cleared by register access. This flag indicates that SSIFRDR is read while it is empty. Data read from SSIFRDR where a receive underflow error is generated is invalid. See section 41.8.6, Error Handling for the error recovery procedure. This flag is not cleared by a receive FIFO data register reset (SSIFCR.RFRST). Note, however, that this flag is not set even if the SSIFRDR register is read while the receive FIFO data register is reset (by setting SSIFCR.RFRST to 1).

[Priority order for setting and clearing]

Setting is prioritized.*1

[Clearing condition]

When either of the following operations is done:

1. Writing 0 to this bit after reading 1 from this bit*2
2. Enabling communication (changing SSICR.REN from 0 to 1).

[Clearing timing]

Clearing timing corresponding to the above clearing condition

1. When 0 is written to this bit after reading 1 from this bit (same as the timing in Figure 41.19)
2. 1 PCLKB cycle after writing 1 to SSICR.REN.*3

Note 1. This bit is cleared by a software reset (SSIFCR.SSIRST = 1). The software reset has priority over all the clearing conditions described above.

Note 2. After reading 1 from this bit, this bit is cleared when one of the following three conditions is met:
- A software reset (SSIFCR.SSIRST = 1) is done.
- After 1 has been read, writing of 0 is complete.
- 1 PCLKB cycle passes after 1 has been written to SSICR.REN.

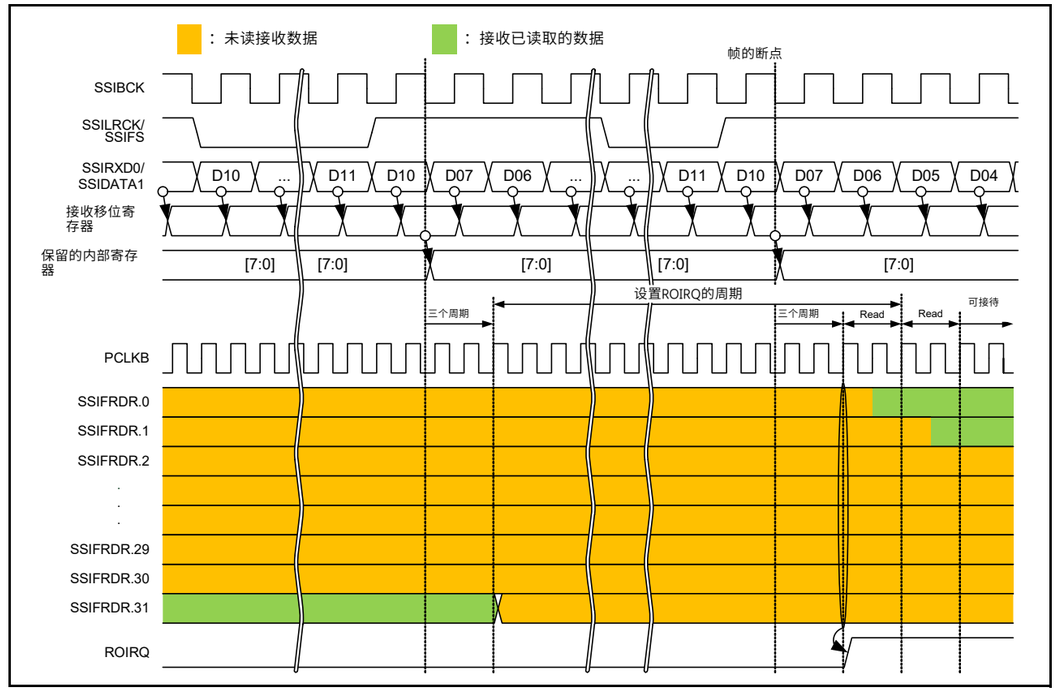


Figure 41.16 ROIRQ设置时序

RUIRQ位（接收下溢错误状态标志）

这是指示接收下溢错误的状态标志。该标志由自动确定设置，但必须通过寄存器访问清除。此标志指示SSIFRDR在为空时被读取。从产生接收下溢错误的SSIFRDR读取的数据无效。有关错误恢复过程，请参见第41.8.6节，错误处理。该标志不会被接收FIFO数据寄存器复位(SSIFCR.RFRST)清除。但是请注意，即使在接收FIFO数据寄存器复位（通过将SSIFCR.RFRST设置为1）时读取SSIFRDR寄存器，该标志也不会设置。

[设置和清除的优先顺序]

设置优先。*1

[Clearing condition]

完成以下任一操作时：

1. 从该位读取1后向该位写入0*2
2. 启用通信（将SSICR.REN从0更改为1）。

[Clearing timing]

与上述清零条件对应的清零时机

1. 当从该位读取1后向该位写入0时（与图41.19中的时序相同）
2. 向SSICR.REN写入1后的1个PCLKB周期。*3

注1.该位通过软件复位(SSIFCR.SSIRST=1)清零。软件复位优先于上述所有清除条件。注2.从该位读取1后，当满足以下三个条件之一时，该位被清除：软件复位(SSIFCR.SSIRST=1)完成。读取1后，写入0完成。在将1写入SSICR.REN后经过1个PCLKB周期。

Note 3. After communication is enabled (by changing the value of SSICR.REN bit from 0 to 1), the reception error flags (RUIRQ and ROIRQ in the SSISR register) are cleared. If, however, the SSISR register is read continuously, the cleared status of the reception error flags might be unable to be read.

[Setting condition]

Reading from SSIFRDR while it is empty.

[Setting timing]

At completion of reading from SSIFRDR. See Figure 41.17.

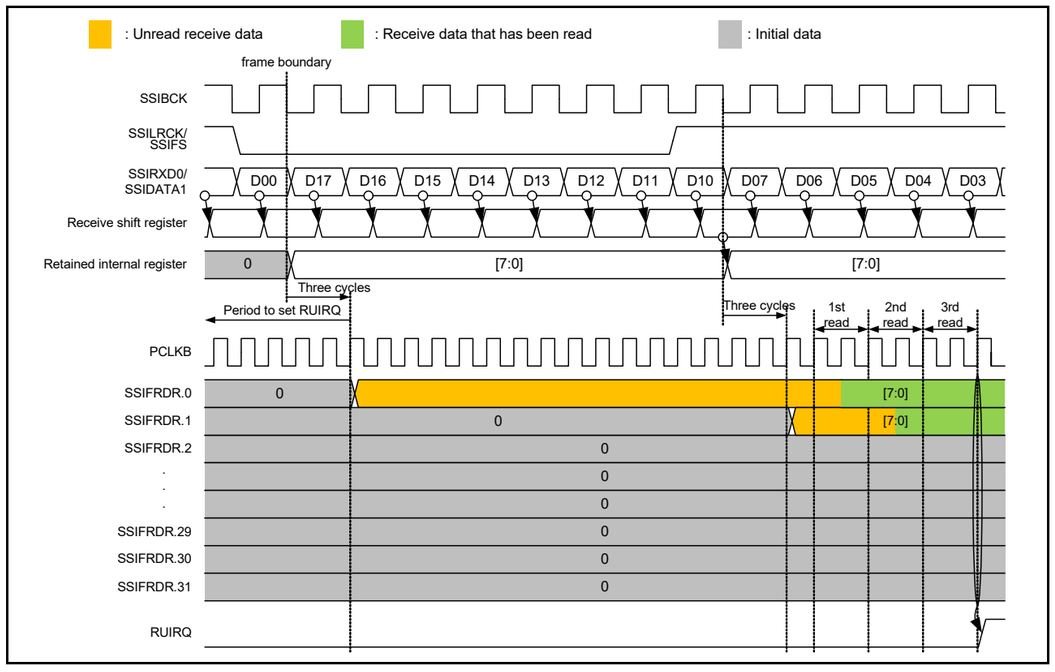


Figure 41.17 RUIRQ setting timing

TOIRQ bit (Transmit Overflow Error Status Flag)

This is a status flag that indicates a transmit overflow error. This flag is set by automatic determination but it must be cleared by register access. This flag indicates that an attempt has been made to write data to the SSIFTDR register when the register is full of data. The data writing that causes a transmit overflow is ignored. For the procedure to recover from the overflow error, see section 41.8.6, Error Handling. This flag is not cleared by a transmit FIFO data register reset (SSIFCR.TFRST).

[Priority order for setting and clearing]

Setting is prioritized.*1

[Clearing condition]

When either of the following operations is done:

(1) Writing 0 to this bit after reading 1 from this bit*2

(2) Enabling communication (changing SSICR.TEN from 0 to 1).

[Clearing timing]

Clearing timing corresponding to the above clearing condition

注3.使能通信后（通过将SSICR.REN位的值从0更改为1），接收错误标志（SSISR寄存器中的RUIRQ和ROIRQ）被清除。但是，如果连续读取SSISR寄存器，则可能无法读取接收错误标志的清除状态。

[Setting condition]

在SSIFRDR为空时读取。

[Setting timing]

从SSIFRDR读取完成时。请参见图41.17。

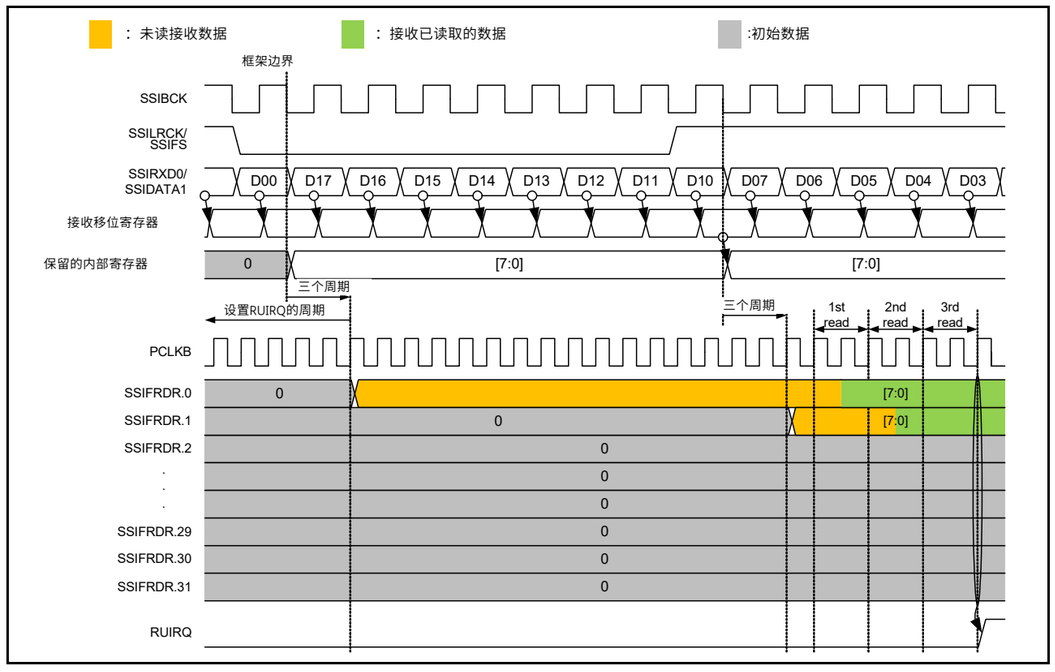


Figure 41.17 RUIRQ设置时序

TOIRQ位（发送溢出错误状态标志）

这是指示传输溢出错误的状态标志。该标志由自动确定设置，但必须通过寄存器访问清除。该标志表明当寄存器已满时尝试将数据写入SSIFTDR寄存器。导致发送溢出的数据写入将被忽略。有关从溢出错误中恢复的过程，请参阅第41.8.6节，错误处理。该标志不会被发送FIFO数据寄存器复位(SSIFCR.TFRST)清除。

[设置和清除的优先顺序]

设置优先。*1

[Clearing condition]

完成以下任一操作时：

(1)从该位读取1后向该位写入0*2

(2)启用通信（将SSICR.TEN从0更改为1）。

[Clearing timing]

与上述清零条件对应的清零时机

(1) When 0 is written to this bit after reading 1 from this bit (same as the timing in Figure 41.19)

(2) 1 PCLKB cycle after writing 1 to SSICR.TEN.*3

Note 1. This bit is cleared by a software reset (SSIFCR.SSIRST = 1). The software reset has priority over all the clearing conditions described above.

Note 2. After reading 1 from this bit, this bit is cleared when one of the following three conditions is met:
- A software reset (SSIFCR.SSIRST = 1) is done.
- After 1 has been read, writing of 0 is complete.
- 1 PCLKB cycle passes after 1 has been written to SSICR.TEN.

Note 3. After communication is enabled (by changing the value of SSICR.TEN bit from 0 to 1), the transmission error flags (TOIRQ and TUIRQ in the SSISR register) are cleared. If, however, the SSISR register is read continuously, the cleared status of the transmission error flags might be unable to be read.

[Setting condition]

An attempt was made to write data to the SSIFTDR register when the register is full of data.

[Setting timing]

At completion of writing to SSIFTDR. For details, see Figure 41.18.

(1)从该位读取1后向该位写入0时（与图41.19中的时序相同）

(2)向SSICR.TEN写入1后的1个PCLKB周期。*3

注1.该位通过软件复位(SSIFCR.SSIRST=1)清零。软件复位优先于上述所有清除条件。注2.从该位读取1后，当满足以下三个条件之一时，该位被清除：软件复位(SSIFCR.SSIRST=1)完成。读取1后，写入0完成。在将1写入SSICR.TEN之后经过1个PCLKB周期。注3.启用通讯后（通过将SSICR.TEN位的值从0更改为1），传输错误

标志（SSISR寄存器中的TOIRQ和TUIRQ）被清除。但是，如果连续读取SSISR寄存器，则可能无法读取传输错误标志的清除状态。

[Setting condition]

当寄存器已满时，尝试将数据写入SSIFTDR寄存器。

[Setting timing]

完成对SSIFTDR的写入。详见图41.18。

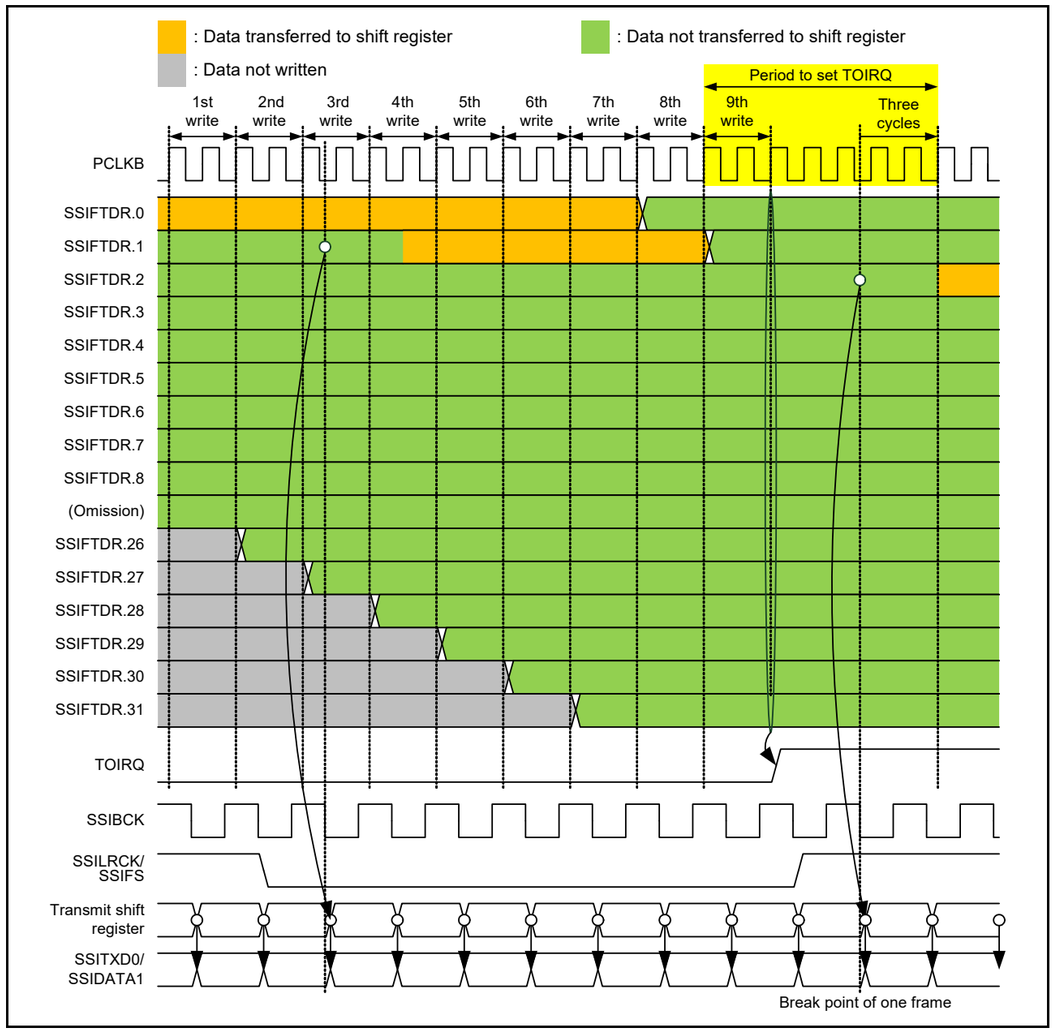


Figure 41.18 TOIRQ setting timing

TUIRQ bit (Transmit Underflow Error Status flag)

This is a status flag that indicates a transmit underflow error. This flag is set by automatic determination but it must be cleared by register access. This flag indicates that writing the serial data required for a frame to SSIFTDR did not catch up with transmission of the frame. Even if this flag is cleared after it has been set, the SSITXD0/SSIDATA1 output remains to be 0. To output the data written to the transmit FIFO data register (SSIFTDR) to the SSITXD0/SSIDATA1 pin, follow the communication stop procedure in Figure 41.56 and error-handling procedure in Figure 41.57. For the procedure to recover from an error, see section 41.8.6, Error Handling. This flag is not cleared by a reset of transmit FIFO data register (by the SSIFCR.TFRST signal).

[Priority order for setting and clearing]

Setting is prioritized.*1

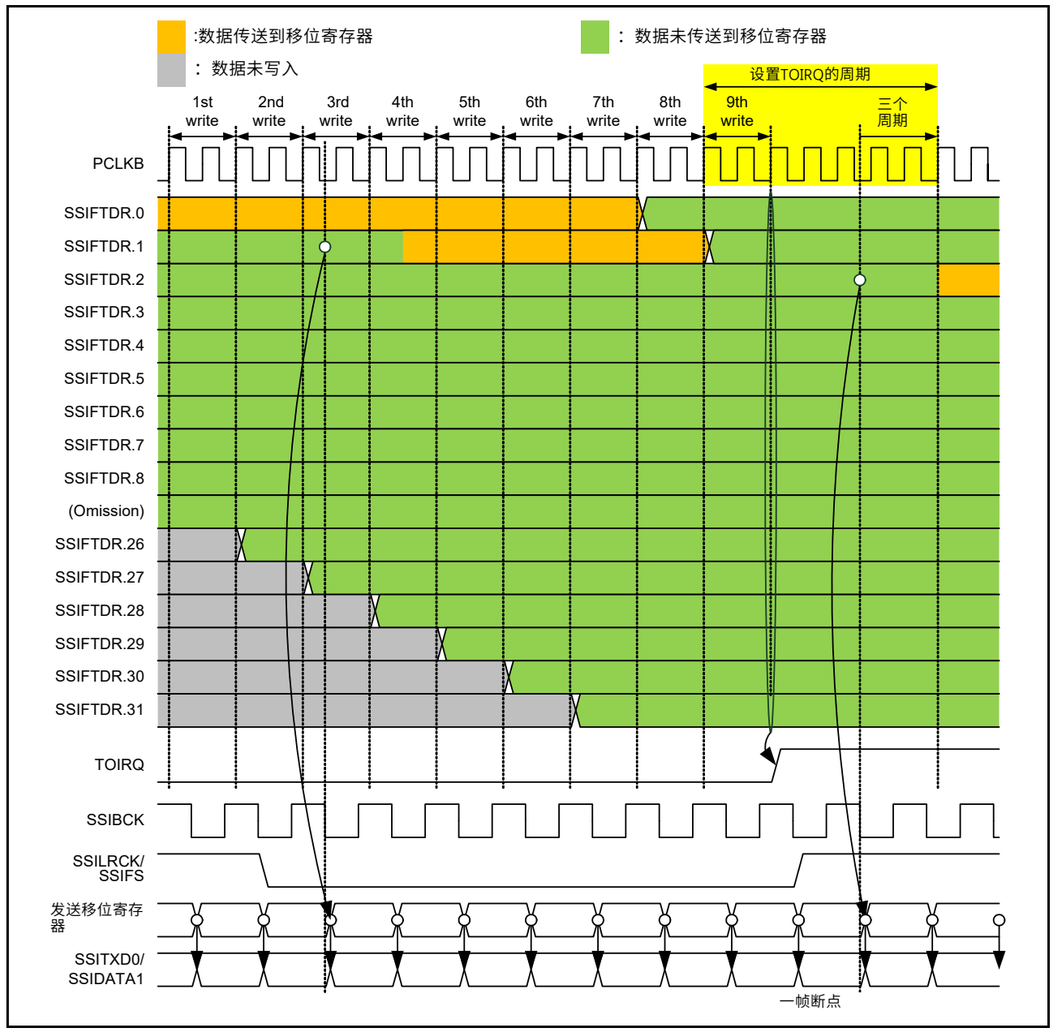


Figure 41.18 TOIRQ设置时序

TUIRQ位（发送下溢错误状态标志）

这是指示发送下溢错误的状态标志。该标志由自动确定设置，但必须通过寄存器访问清除。该标志表示将帧所需的串行数据写入SSIFTDR没有赶上帧的传输。即使该标志在设置后被清除，SSITXD0SSIDATA1输出仍保持为0。要将写入发送FIFO数据寄存器(SSIFTDR)的数据输出到SSITXD0SSIDATA1引脚，请遵循图41.56中的通信停止程序并图41.57中的错误处理过程。有关从错误中恢复的过程，请参阅第41.8.6节，错误处理。该标志不会通过发送FIFO数据寄存器的复位（通过SSIFCR.TFRST信号）清除。

[设置和清除的优先顺序]

设置优先。*1

[Clearing condition]

When either of the following operations is done:

1. Writing 0 to this bit after reading 1 from this bit*2
2. Enabling communication (changing SSICR.TEN from 0 to 1).

[Clearing timing]

Clearing timing corresponding to the above clearing condition

1. When 0 is written to this bit after reading 1 from this bit
2. 1 PCLKB cycle after writing 1 to SSICR.TEN.*3

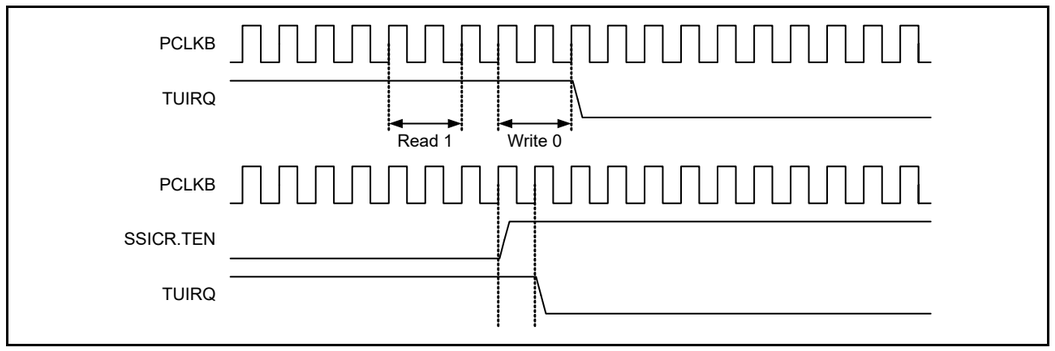


Figure 41.19 TUIRQ clearing timing

Note 1. This bit is cleared by a software reset (SSIFCR.SSIRST = 1). The software reset has priority over all the clearing conditions described above.

Note 2. After reading 1 from this bit, this bit is cleared when one of the following three conditions is met:
- A software reset (SSIFCR.SSIRST = 1) is done.
- After 1 has been read, writing of 0 is complete.
- 1 PCLKB cycle passes after 1 has been written to SSICR.TEN.

Note 3. After communication is enabled (by changing the value of SSICR.TEN bit from 0 to 1), the transmission error flags (TOIRQ and TUIRQ in the SSISR register) are cleared. If, however, the SSISR register is read continuously, the cleared status of the transmission error flags might be unable to be read.

[Setting condition]

When communication continues over a frame boundary, the transmit data required for the next frame has not been written to SSIFTDR. For details, see Figure 41.20 and Figure 41.21.

[Setting timing]

3 PCLKB cycles after the frame boundary. For details, see Figure 41.20.

[Clearing condition]

完成以下任一操作时：

1. 从该位读取1后向该位写入0*2
2. 启用通信（将SSICR.TEN从0更改为1）。

[Clearing timing]

与上述清零条件对应的清零时机

1. 当从该位读取1后向该位写入0
2. 向SSICR.TEN写入1后的1个PCLKB周期。*3

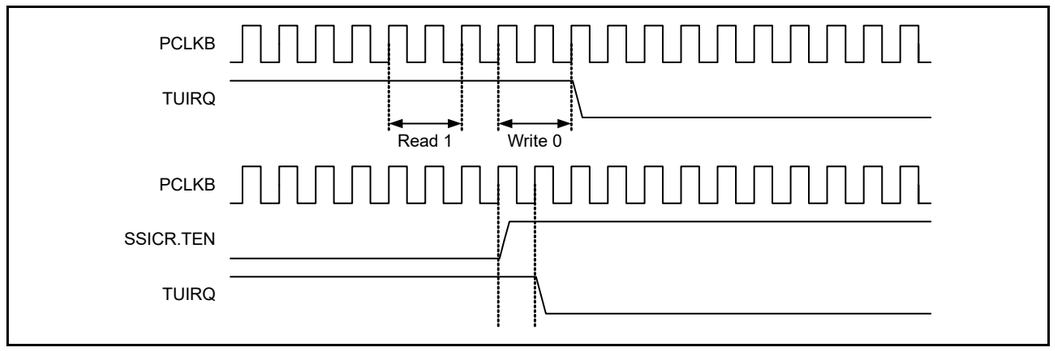


Figure 41.19 TUIRQ清零时机

注1.该位通过软件复位(SSIFCR.SSIRST=1)清零。软件复位优先于上述所有清除条件。注2.从该位读取1后，当满足以下三个条件之一时，该位被清除：软件复位(SSIFCR.SSIRST=1)完成。读取1后，写入0完成。在将1写入SSICR.TEN之后经过1个PCLKB周期。注3.启用通讯后（通过将SSICR.TEN位的值从0更改为1），传输错误

标志（SSISR寄存器中的TOIRQ和TUIRQ）被清除。但是，如果连续读取SSISR寄存器，则可能无法读取传输错误标志的清除状态。

[Setting condition]

当通信继续通过帧边界时，下一帧所需的传输数据尚未写入SSIFTDR。详见图41.20和图41.21。

[Setting timing]

帧边界后3个PCLKB周期。详见图41.20。

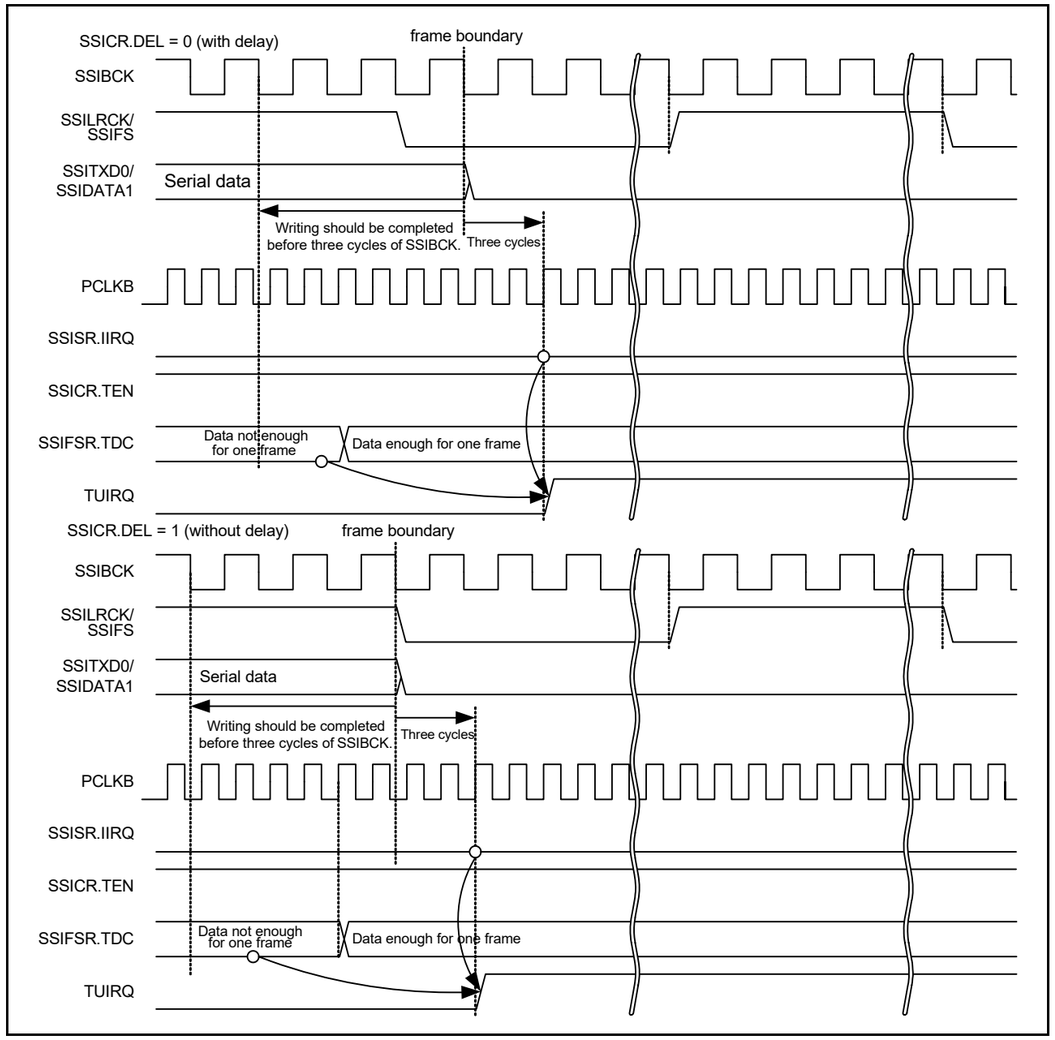


Figure 41.20 TUIRQ setting timing (when communication continues)

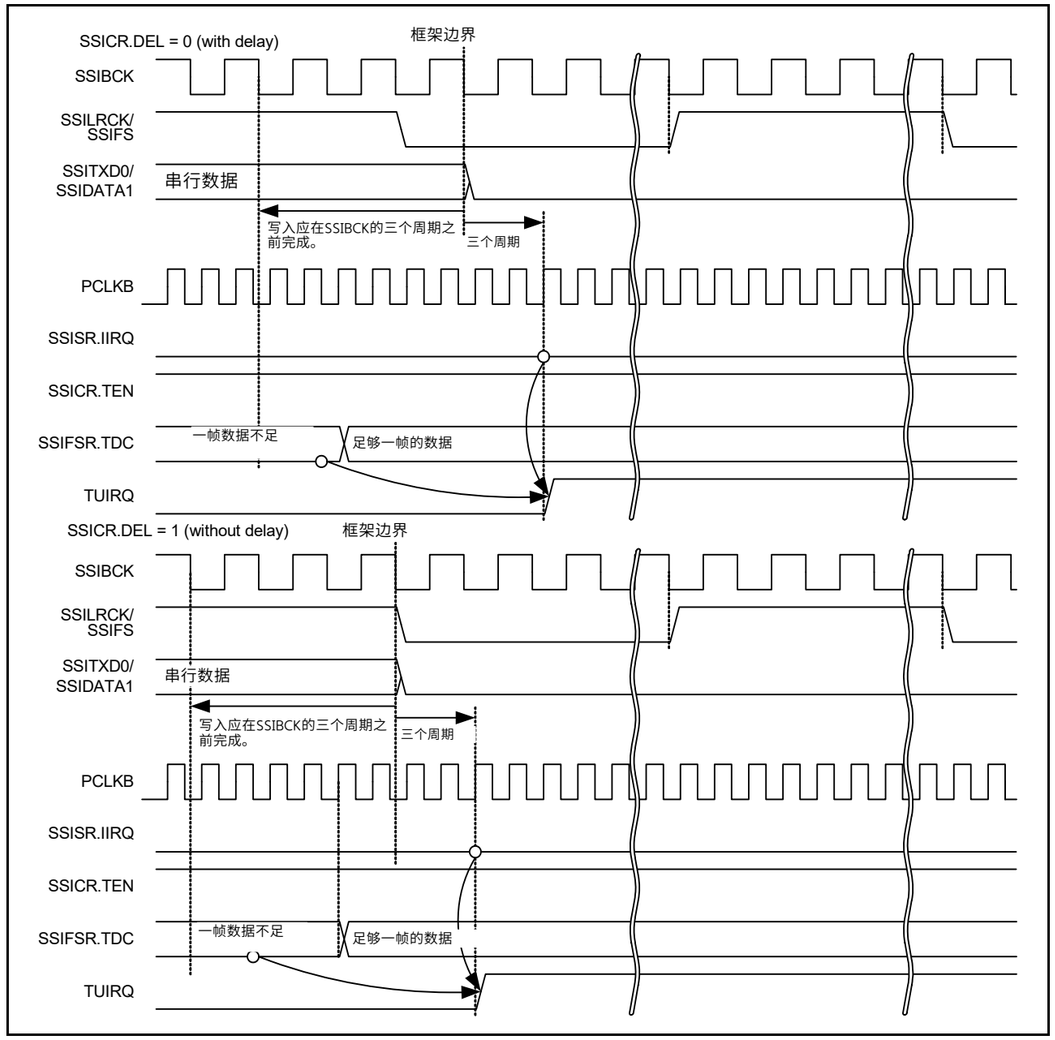


Figure 41.20 TUIRQ设置时间（通信继续时）

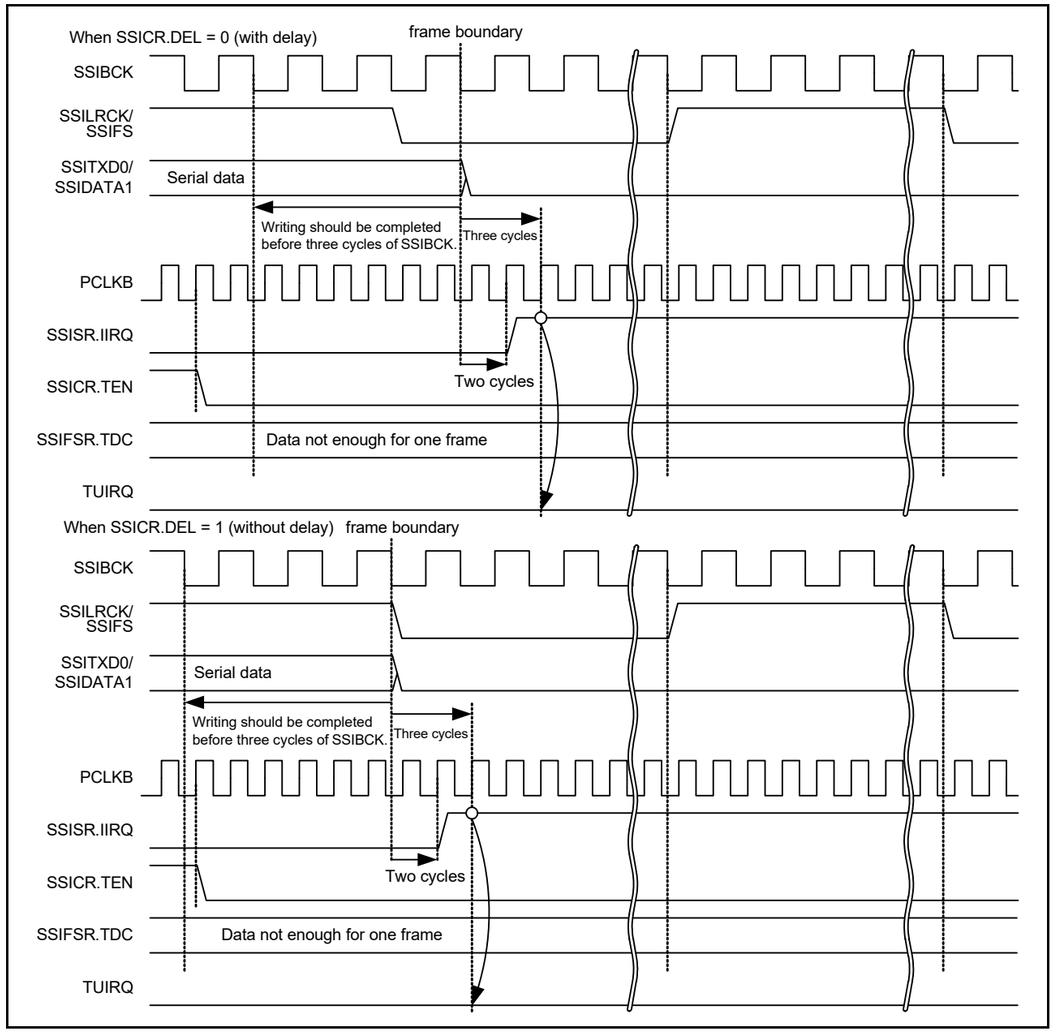


Figure 41.21 TUIRQ setting timing (when communication stops)

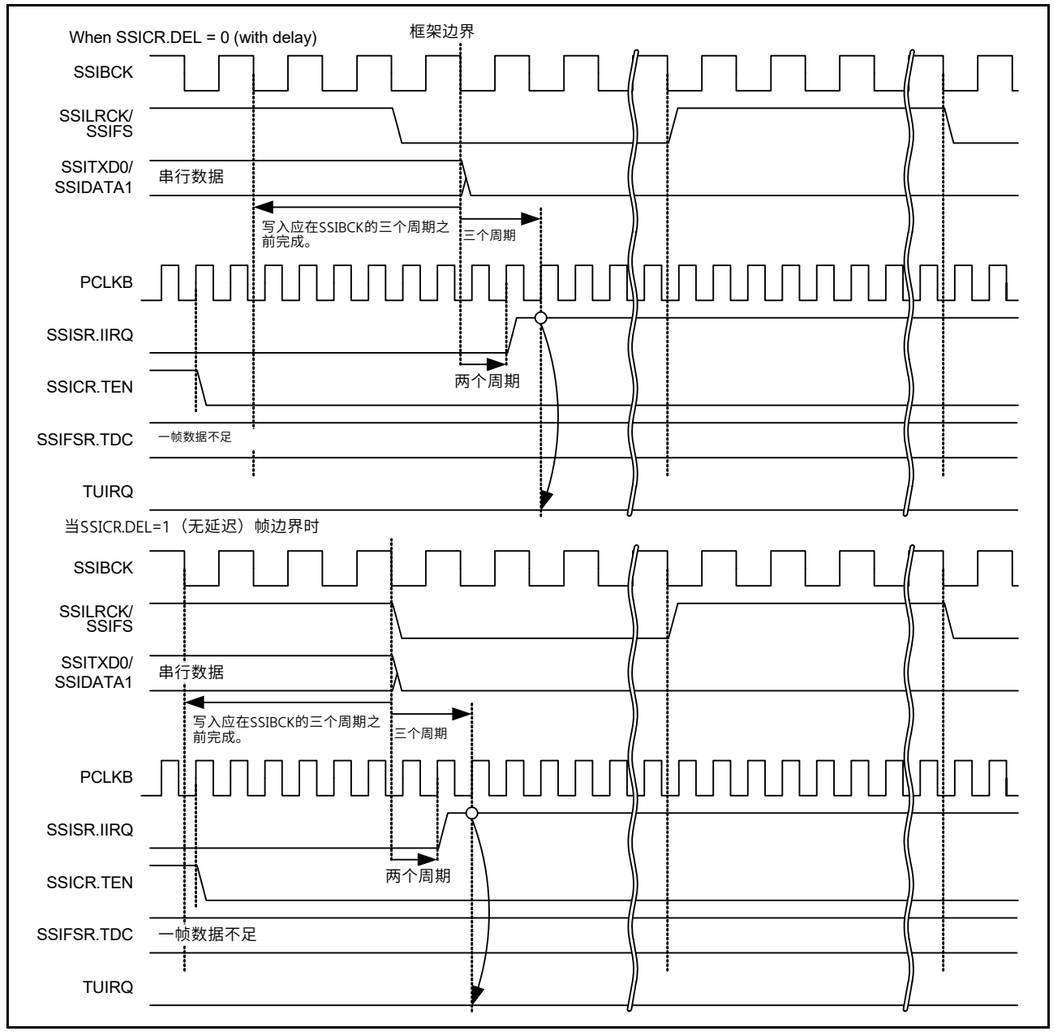


Figure 41.21 TUIRQ设置时间（通信停止时）

41.4.3 FIFO Control Register (SSIFCR)

Address(es): SSIE0.SSIFCR 4004 E010h, SSIE1.SSIFCR 4004 E110h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	AUCKE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SSIRST
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	BSW	—	—	—	—	—	—	—	TIE	RIE	TFRST	RFRST
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	RFRST	Receive FIFO Data Register Reset*1	0: Clears a receive data FIFO reset condition 1: Sets a receive data FIFO reset condition.	R/W
b1	TFRST	Transmit FIFO Data Register Reset*1	0: Clears a transmit data FIFO reset condition 1: Sets a transmit data FIFO reset condition.	R/W
b2	RIE	Receive Data Full Interrupt Output Enable	0: Disables receive data full interrupts 1: Enables receive data full interrupts.	R/W
b3	TIE	Transmit Data Empty Interrupt Output Enable	0: Disables transmit data empty interrupts 1: Enables transmit data empty interrupts.	R/W
b10 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b11	BSW	Byte Swap Enable*1	0: Disables byte swap 1: Enables byte swap.	R/W
b15 to b12	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b16	SSIRST	Software Reset	0: Clears a software reset condition 1: Sets a software reset condition.	R/W
b30 to b17	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b31	AUCKE	AUDIO_MCK Enable in Master-mode Communication*1	0: Disables supply of AUDIO_MCK 1: Enables supply of AUDIO_MCK.	R/W

Note 1. Writing to these bits while SSIE is in a communication state (SSISR.IIRQ = 0) is prohibited. If the value of these bits is changed by rewriting, subsequent operation is unpredictable.

This register sets a software reset, byte swap, and enable/disable of interrupt requests.

RFRST bit (Receive FIFO Data Register Reset)

This bit sets a software reset of the receive FIFO data register (SSIFRDR). Writing 1 to this bit initializes the internal state related to SSIFRDR. The register bits subject to the software reset triggered by this bit are indicated by shading in Table 41.5. Because this bit is not automatically cleared after it has been set, write 0 to this bit to release the register bits from the software reset. After writing 0 to this bit, be sure to check that this bit is 0 before starting the next procedural step.

This bit is subject to the software reset by the SSIRST bit. Because the software reset by the SSIRST bit has priority over the reset by this bit, setting this bit is ignored when the SSIRST bit is set.

41.4.3 FIFO控制寄存器(SSIFCR)

Address(es): SSIE0.SSIFCR 4004 E010h, SSIE1.SSIFCR 4004 E110h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	AUCKE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SSIRST
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	BSW	—	—	—	—	—	—	—	TIE	RIE	TFRST	RFRST
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	RFRST	接收FIFO数据寄存器 Reset*1	0：清除接收数据FIFO复位条件1：设置接收数据FIFO复位条件。	R/W
b1	TFRST	发送FIFO数据寄存器 Reset*1	0：清除发送数据FIFO复位条件1：设置发送数据FIFO复位条件。	R/W
b2	RIE	接收数据满中断输出使能	0：禁止接收数据满中断1：使能接收数据满中断。	R/W
b3	TIE	发送数据空中断输出使能	0：禁用传输数据空中断1：启用传输数据空中断。	R/W
b10 to b4	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b11	BSW	字节交换使能 *1	0：禁用字节交换1：启用字节交换。	R/W
b15 to b12	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b16	SSIRST	软件复位	0：清除软件复位条件1：设置软件复位条件。	R/W
b30 to b17	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b31	AUCKE	AUDIO_MCK在主模式通信中启用	0：禁用AUDIO_MCK供应1：启用AUDIO_MCK供应。	R/W

Note 1. 禁止在SSIE处于通信状态(SSISR.IIRQ=0)时写入这些位。如果这些位的值通过重写而改变，后续的操作是不可预知的。

该寄存器设置软件复位、字节交换和中断请求的启用禁用。

RFRST位（接收FIFO数据寄存器复位）

该位设置接收FIFO数据寄存器(SSIFRDR)的软件复位。向该位写入1初始化与SSIFRDR相关的内部状态。受该位触发的软件复位的寄存器位在表41.5中用阴影表示。由于该位在被设置后不会自动清零，因此向该位写入0以从软件复位中释放寄存器位。向该位写入0后，请务必在开始下一个程序步骤之前检查该位是否为0。

该位受SSIRST位软件复位的影响。由于SSIRST位的软件复位优先于该位的复位，所以当SSIRST位置位时，该位的设置将被忽略。

Table 41.5 Bits subject to software reset by the RFRST bit

Symbol	Address (BASE+)		+0								+1							
			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSICR	00h	+0	—	CKS	TUIEN	TOIEN	RUIEN	ROIEN	IIEN	—	FRM[1:0]		DWL[2:0]			SWL[2:0]		
		+2	—	MST	BCKP	LRCKP	SPDP	SDTA	PDTA	DEL	CKDV[3:0]				MUEN	—	TEN	REN
SSISR	04h	+0	—	—	TUIRQ	TOIRQ	RUIRQ	ROIRQ	IIRQ	—	—	—	—	—	—	—	—	—
		+2	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
SSIFCR	10h	+0	AUCKE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SSIRST
		+2	—	—	—	—	BSW	—	—	—	—	—	—	—	TIE	RIE	TFRST	RFRST
SSIFSR	14h	+0	—	—	TDC[5:0]						—	—	—	—	—	—	—	TDE
		+2	—	—	RDC[5:0]						—	—	—	—	—	—	—	RDF
SSIFTDR	18h	+0	FTDR[31:16]															
		+2	FTDR[15:0]															
SSIFRDR	1ch	+0	FRDR[31:16]															
		+2	FRDR[15:0]															
SSIOFR	20h	+0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		+2	—	—	—	—	—	—	BCKASTP	LRCONT	—	—	—	—	—	—	OMOD[1:0]	
SSISCR	24h	+0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		+2	—	—	—	TDES[4:0]					—	—	—	RDFS[4:0]				

TFRST bit (Transmit FIFO Data Register Reset)

This bit sets a software reset of the transmit FIFO data register (SSIFTDR). Writing 1 to this bit initializes the internal state related to SSIFTDR. The register bits subject to the software reset triggered by this bit are indicated by shading in Table 41.6. Because this bit is not automatically cleared after it has been set, write 0 to this bit to release the register bits from the software reset. After writing 0 to this bit, be sure to check that this bit is 0 before starting the next procedural step.

This bit is subject to the software reset by the SSIRST bit. Because the software reset by the SSIRST bit has priority over the reset by this bit, setting this bit is ignored when the SSIRST bit is set.

Table 41.5 受RFRST位软件复位的位

Symbol	Address (BASE+)		+0								+1							
			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSICR	00h	+0	—	CKS	途恩	托伊恩	瑞恩	投资回报率CN	IIEN	—	FRM[1:0]		DWL[2:0]			SWL[2:0]		
		+2	—	MST	BCKP	LRCKP	SPDP	SDTA	PDTA	DEL	CKDV[3:0]				穆恩	—	TEN	REN
SSISR	04h	+0	—	—	TUIRQ	TOIRQ	RUIRQ	ROIRQ	IIRQ	—	—	—	—	—	—	—	—	—
		+2	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
SSIFCR	10h	+0	AUCKE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SSIRST
		+2	—	—	—	—	BSW	—	—	—	—	—	—	—	TIE	RIE	TFRST	RFRST
SSIFSR	14h	+0	—	—	TDC[5:0]						—	—	—	—	—	—	—	TDE
		+2	—	—	RDC[5:0]						—	—	—	—	—	—	—	RDF
SSIFTDR	18h	+0	FTDR[31:16]															
		+2	FTDR[15:0]															
SSIFRDR	1ch	+0	FRDR[31:16]															
		+2	FRDR[15:0]															
SSIOFR	20h	+0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		+2	—	—	—	—	—	—	BCKASTP	LRCONT	—	—	—	—	—	—	OMOD[1:0]	
SSISCR	24h	+0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		+2	—	—	—	TDES[4:0]					—	—	—	RDFS[4:0]				

TFRST位（发送FIFO数据寄存器复位）

该位设置发送FIFO数据寄存器(SSIFTDR)的软件复位。向该位写入1初始化与SSIFTDR相关的内部状态。受该位触发的软件复位的寄存器位在表41.6中用阴影表示。由于该位在被设置后不会自动清零，因此向该位写入0以从软件复位中释放寄存器位。向该位写入0后，请务必在开始下一个程序步骤之前检查该位是否为0。

该位受SSIRST位软件复位的影响。由于SSIRST位的软件复位优先于该位的复位，所以当SSIRST位置位时，该位的设置将被忽略。

Table 41.6 Bits subject to software reset by the TFRST bit

Symbol	Address (BASE+)		+0								+1							
			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSICR	00h	+0	—	CKS	TUIEN	TOIEN	RUIEN	ROIEN	IIEN	—	FRM[1:0]		DWL[2:0]			SWL[2:0]		
		+2	—	MST	BCKP	LRCKP	SPDP	SDTA	PDTA	DEL	CKDV[3:0]				MUEN	—	TEN	REN
SSISR	04h	+0	—	—	TUIRQ	TOIRQ	RUIRQ	ROIRQ	IIRQ	—	—	—	—	—	—	—	—	—
		+2	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
SSIFCR	10h	+0	AUCKE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SSIRST
		+2	—	—	—	—	BSW	—	—	—	—	—	—	—	TIE	RIE	TFRST	RFRST
SSIFSR	14h	+0	—	—	TDC[5:0]						—	—	—	—	—	—	—	TDE
		+2	—	—	RDC[5:0]						—	—	—	—	—	—	—	RDF
SSIFTDR	18h	+0	FTDR[31:16]															
		+2	FTDR[15:0]															
SSIFRDR	1ch	+0	FRDR[31:16]															
		+2	FRDR[15:0]															
SSIOFR	20h	+0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		+2	—	—	—	—	—	—	BCKASTP	LRCONT	—	—	—	—	—	—	OMOD[1:0]	
SSISCR	24h	+0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		+2	—	—	—	TDES[4:0]					—	—	—	RDFS[4:0]				

RIE bit (Receive Data Full Interrupt Output Enable)

This bit enables/disables output of receive data full interrupts. Use a receive data full interrupt as an interrupt to trigger data reading from the receive FIFO data register. Write 1 to this bit after specifying the setting condition for receive data full interrupt (by using the SSISCR.RDFS bit). Figure 41.22 shows the timing of generating the receive data full interrupt.

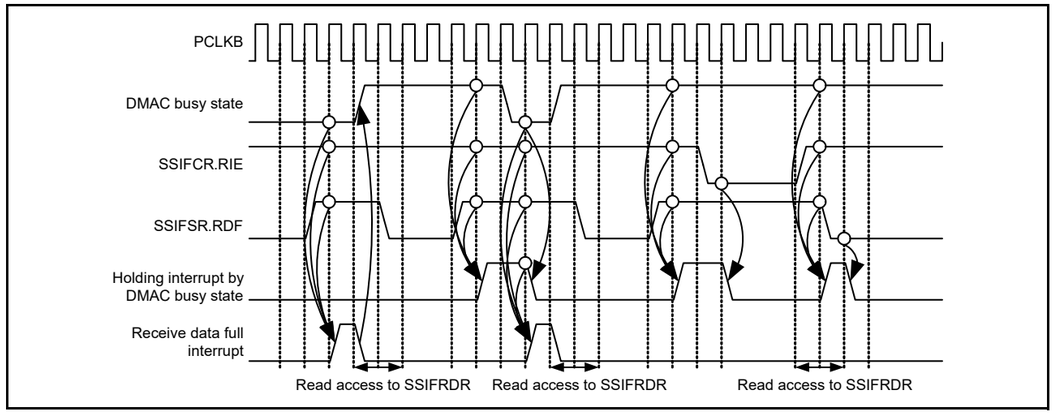


Figure 41.22 Timing of receive data full interrupt

TIE bit (Transmit Data Empty Interrupt Output Enable)

This bit enables/disables output of transmit data empty interrupts. Use a transmit data empty interrupt as an interrupt to

Table 41.6 受TFRST位软件复位的位

Symbol	Address (BASE+)		+0								+1							
			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSICR	00h	+0	—	CKS	途恩	托伊恩	瑞恩	投资回报率CN	IIEN	—	FRM[1:0]		DWL[2:0]			SWL[2:0]		
		+2	—	MST	BCKP	LRCKP	SPDP	SDTA	PDTA	DEL	CKDV[3:0]				穆恩	—	TEN	REN
SSISR	04h	+0	—	—	TUIRQ	TOIRQ	RUIRQ	ROIRQ	IIRQ	—	—	—	—	—	—	—	—	—
		+2	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
SSIFCR	10h	+0	AUCKE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SSIRST
		+2	—	—	—	—	BSW	—	—	—	—	—	—	—	TIE	RIE	TFRST	RFRST
SSIFSR	14h	+0	—	—	TDC[5:0]						—	—	—	—	—	—	—	TDE
		+2	—	—	RDC[5:0]						—	—	—	—	—	—	—	RDF
SSIFTDR	18h	+0	FTDR[31:16]															
		+2	FTDR[15:0]															
SSIFRDR	1ch	+0	FRDR[31:16]															
		+2	FRDR[15:0]															
SSIOFR	20h	+0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		+2	—	—	—	—	—	—	BCKASTP	LRCONT	—	—	—	—	—	—	OMOD[1:0]	
SSISCR	24h	+0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		+2	—	—	—	TDES[4:0]					—	—	—	RDFS[4:0]				

RIE位（接收数据满中断输出使能）

该位使能禁用接收数据满中断的输出。使用接收数据满中断作为中断来触发从接收FIFO数据寄存器读取数据。指定接收数据满中断的设置条件后（通过使用SISSCR.RDFS位）向该位写入1。图41.22显示了产生接收数据满中断的时序。

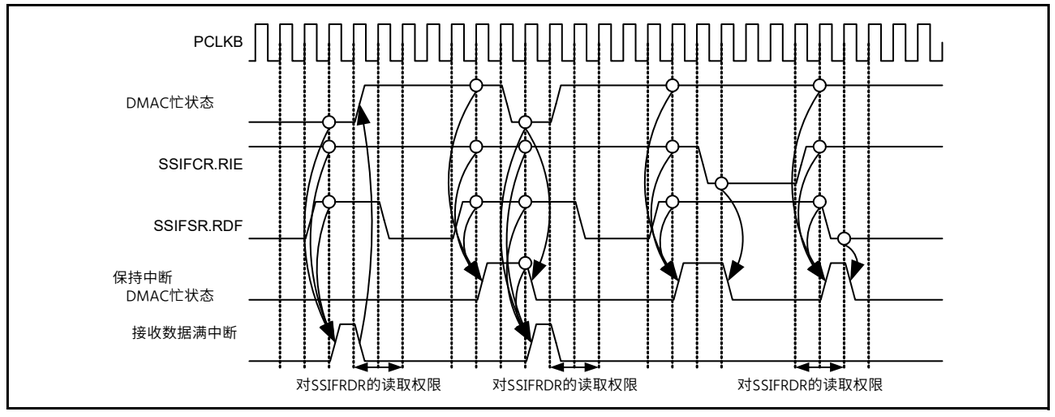


Figure 41.22 接收数据满中断的时序

TIE位（发送数据空中断输出使能）

该位使能禁用发送数据空中断的输出。使用发送数据空中断作为中断

trigger data writing to the transmit FIFO data register. Write 1 to this bit after specifying the setting condition for transmit data empty interrupt (by using the SSISCR.TDES bit). Figure 41.23 shows the timing of generating the transmit data empty interrupt.

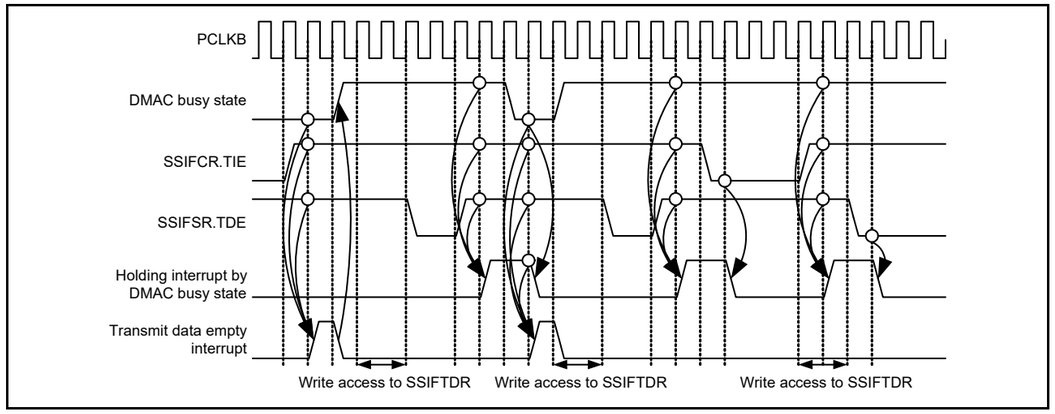


Figure 41.23 Timing of transmit data empty interrupt

BSW bit (Byte Swap Enable)

This bit enables/disables byte swap of register access for the transmit FIFO data register (SSIFTDR) and the receive FIFO data register (SSIFRDR). This bit is valid only with 16-bit access or 32-bit access to SSIFTDR and SSIFRDR. For details, see Figure 41.24.

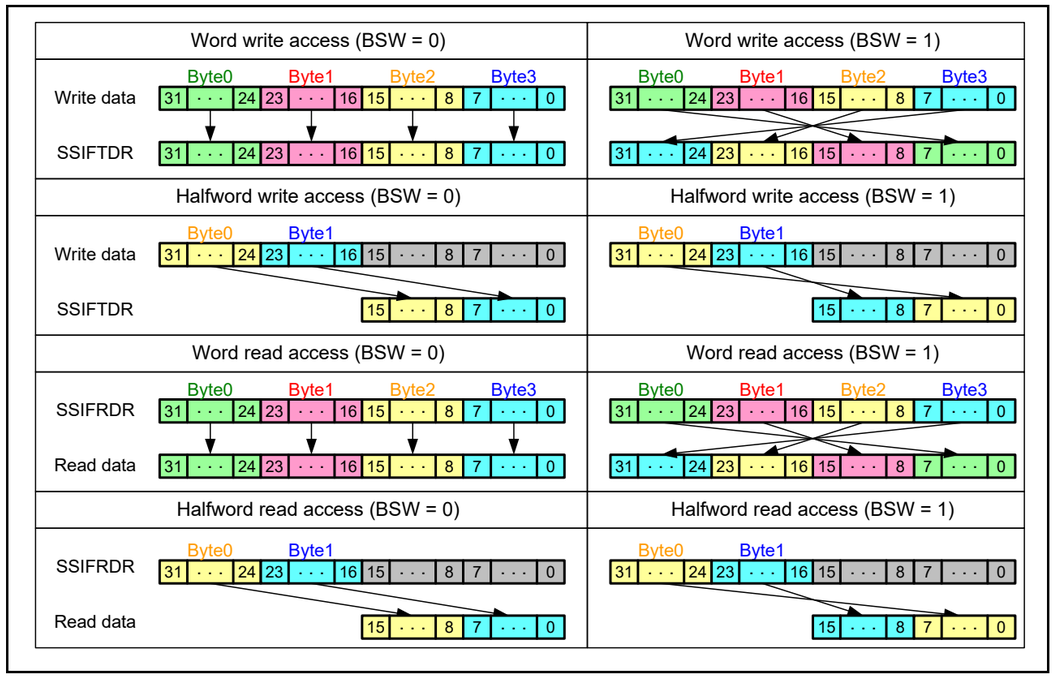


Figure 41.24 Operation example of byte swap

触发数据写入发送FIFO数据寄存器。在指定发送数据空中断的设置条件后（通过使用SISSCR.TDES位）向该位写入1。图41.23显示了产生发送数据空中断的时序。

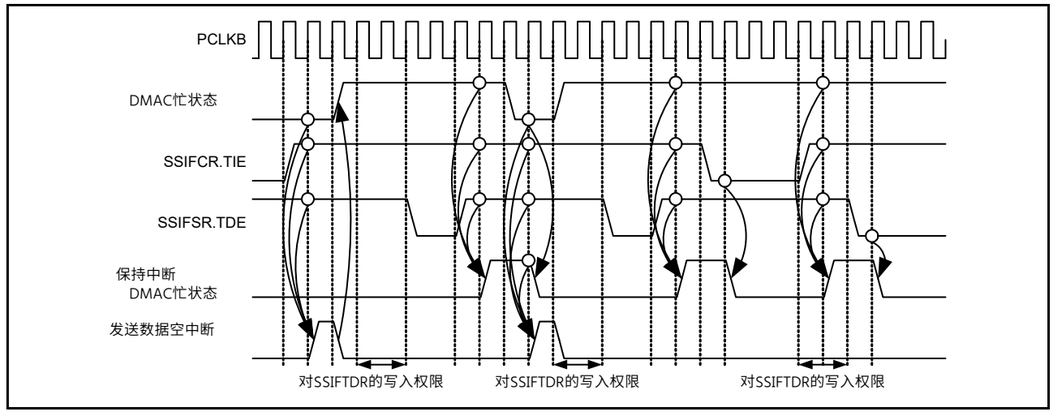


Figure 41.23 发送数据空中断的时序

BSW位（字节交换使能）

该位启用禁用发送FIFO数据寄存器(SSIFTDR)和接收寄存器访问的字节交换
FIFO数据寄存器(SSIFRDR)。该位仅对SSIFTDR和SSIFRDR的16位访问或32位访问有效。详见图41.24。

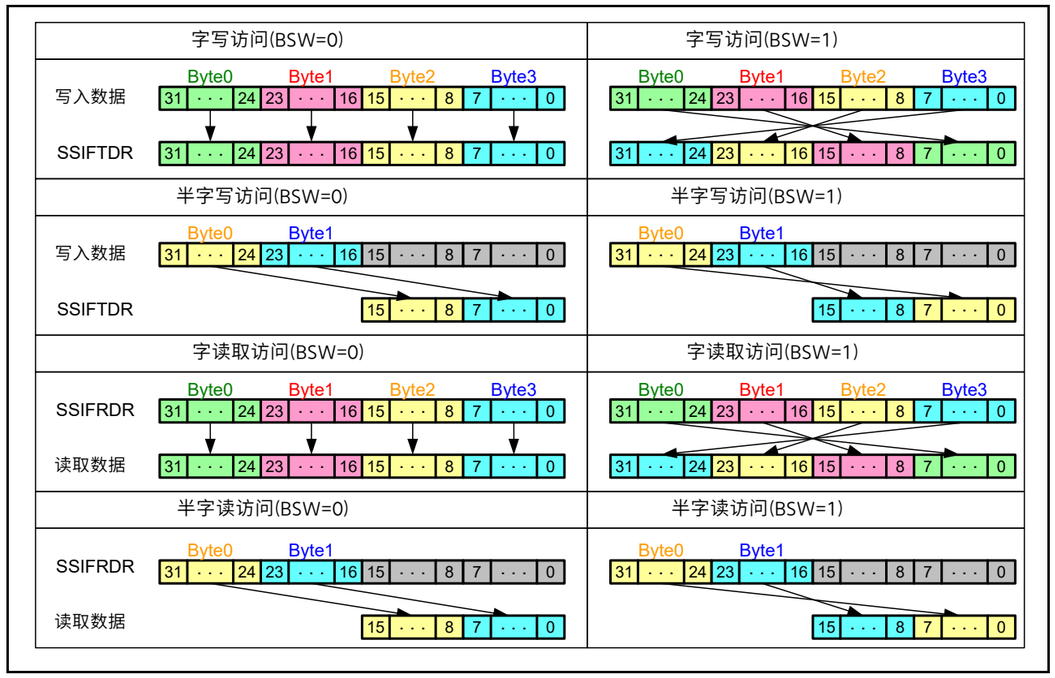


Figure 41.24 字节交换操作示例

SSIRST bit (Software Reset)

This bit sets a software reset of SSIE. Writing 1 to this bit initializes the internal state of SSIE. The register bits subject to the software reset triggered by this bit are indicated by shading in Table 41.7. Because this bit is not automatically cleared after it has been set, write 0 to this bit to release the register bits from the software reset. After writing 0 to this bit, be sure to check that this bit is 0 before starting the next procedural step.

To stop communication of SSIE immediately, after turning off the peripheral functions, write 1 to this bit. Initialization by a software reset is performed without any relation with the bit clock.

Table 41.7 Bits subject to software reset by the SSIRST bit

Symbol	Address (BASE+)		+0								+1							
			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSICR	00h	+0	—	CKS	TUIEN	TOIEN	RUIEN	ROIEN	IIEN	—	FRM[1:0]		DWL[2:0]			SWL[2:0]		
		+2	—	MST	BCKP	LRCKP	SPDP	SDTA	PDTA	DEL	CKDV[3:0]				MUEN	—	TEN	REN
SSISR	04h	+0	—	—	TUIRQ	TOIRQ	RUIRQ	ROIRQ	IIRQ	—	—	—	—	—	—	—	—	—
		+2	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
SSIFCR	10h	+0	AUCKE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SSIRST
		+2	—	—	—	—	BSW	—	—	—	—	—	—	—	TIE	RIE	TFRST	RFRST
SSIFSR	14h	+0	—	—	TDC[5:0]						—	—	—	—	—	—	—	TDE
		+2	—	—	RDC[5:0]						—	—	—	—	—	—	—	RDF
SSIFTDR	18h	+0	FTDR[31:16]															
		+2	FTDR[15:0]															
SSIFRDR	1ch	+0	FRDR[31:16]															
		+2	FRDR[15:0]															
SSIOFR	20h	+0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		+2	—	—	—	—	—	—	BCKASTP	LRCONT	—	—	—	—	—	—	OMOD[1:0]	
SSISCR	24h	+0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		+2	—	—	—	TDES[4:0]					—	—	—	RDFS[4:0]				

AUCKE bit (AUDIO_MCK Enable in Master-mode Communication)

This bit enables/disables supply to AUDIO_MCK while in master-mode communication (MST = 1).

Changing the value of this bit must be performed only after specifying the settings related to AUDIO_MCK (by using the CKS, MST, BCKP, and CKDV bits in the SSICR register).

SSIRST位（软件复位）

该位设置SSIE的软件复位。向该位写入1初始化SSIE的内部状态。受该位触发的软件复位的寄存器位在表41.7中用阴影表示。由于该位在被设置后不会自动清零，因此向该位写入0以从软件复位中释放寄存器位。向该位写入0后，请务必在开始下一个程序步骤之前检查该位是否为0。

要立即停止SSIE通信，请在关闭外围功能后，向该位写入1。通过软件复位进行的初始化与位时钟没有任何关系。

Table 41.7 受SSIRST位软件复位的位

Symbol	Address (BASE+)		+0								+1							
			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSICR	00h	+0	—	CKS	途恩	托伊恩	瑞恩	投资回报率CN	IIEN	—	FRM[1:0]		DWL[2:0]			SWL[2:0]		
		+2	—	MST	BCKP	LRCKP	SPDP	SDTA	PDTA	DEL	CKDV[3:0]				穆恩	—	TEN	REN
SSISR	04h	+0	—	—	TUIRQ	TOIRQ	RUIRQ	ROIRQ	IIRQ	—	—	—	—	—	—	—	—	—
		+2	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
SSIFCR	10h	+0	AUCKE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SSIRST
		+2	—	—	—	—	BSW	—	—	—	—	—	—	—	TIE	RIE	TFRST	RFRST
SSIFSR	14h	+0	—	—	TDC[5:0]						—	—	—	—	—	—	—	TDE
		+2	—	—	RDC[5:0]						—	—	—	—	—	—	—	RDF
SSIFTDR	18h	+0	FTDR[31:16]															
		+2	FTDR[15:0]															
SSIFRDR	1ch	+0	FRDR[31:16]															
		+2	FRDR[15:0]															
SSIOFR	20h	+0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		+2	—	—	—	—	—	—	BCKASTP	LRCONT	—	—	—	—	—	—	OMOD[1:0]	
SSISCR	24h	+0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		+2	—	—	—	TDES[4:0]					—	—	—	RDFS[4:0]				

AUCKE位（在主模式通信中启用AUDIO_MCK）

在主模式通信(MST=1)时，该位使能禁用对AUDIO_MCK的供电。

只有在指定与AUDIO_MCK相关的设置后才能更改该位的值（通过使用SSICR寄存器中的CKS、MST、BCKP和CKDV位）。

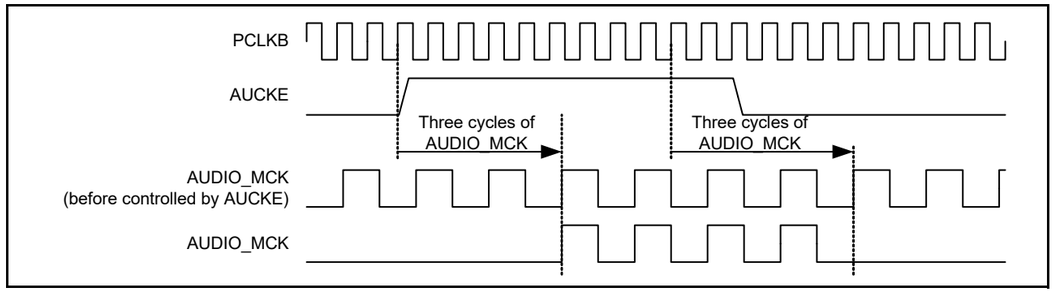


Figure 41.25 Stop/resume of AUDIO_MCK

Note: In slave-mode communication (SSICR.MST = 0), SSIE needs supply of SSIBCK. To stop BCK on the master side, make sure that SSIE is in the idle state (SSISR.IIRQ = 1). If BCK is stopped before SSIE becomes idle, take the procedure to start communication in Figure 41.52 or wait for an idle state by taking the procedure to resume communication in Figure 41.58.
In master-mode communication (SSICR.MST = 1), SSIE operates with the audio clock (AUDIO_MCK). To stop SSIE completely, make sure that SSIE is in the idle state (SSISR.IIRQ = 1) and then write 0 to SSIFCR.ADCKE. If 0 is written to SSIFCR.ADCKE before SSIE becomes idle, take the procedure to start communication in Figure 41.52.

Figure 41.26 and Figure 41.27 show the timings of signal operation in the period from setting this bit to 1 to the output to the SSIBCK pin.

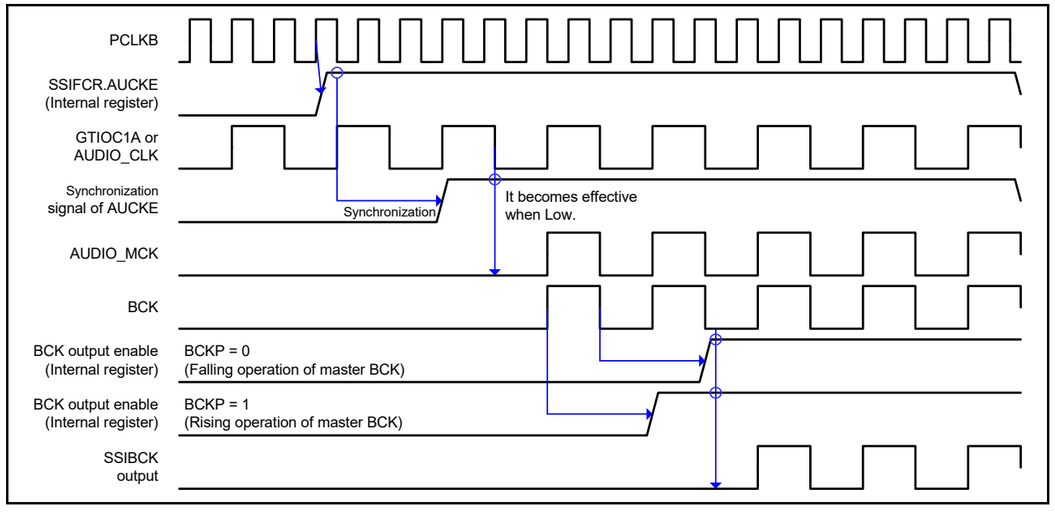


Figure 41.26 Timing diagram for the operation from system reset to start of master-mode communication

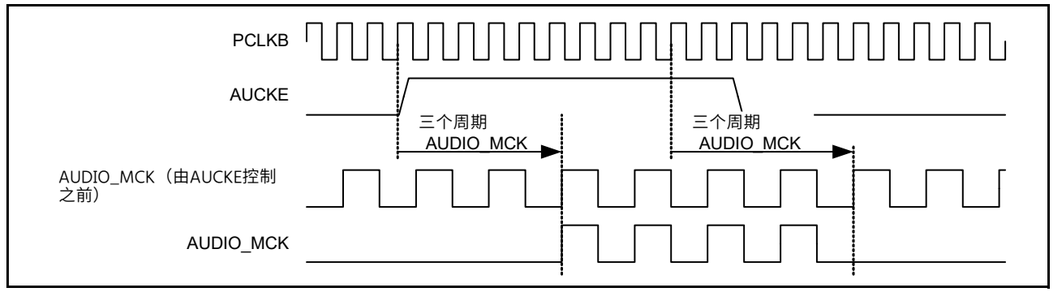


Figure 41.25 Stop/resume of AUDIO_MCK

Note: 在从模式通信(SSICR.MST=0)中，SSIE需要提供SSIBCK。要在主设备端停止BCK，请确保SSIE处于空闲状态(SSISR.IIRQ=1)。如果BCK在SSIE变为空闲之前停止，则按照图41.52中的程序开始通信或按照图41.58中的程序恢复通信等待空闲状态。在主模式通信(SSICR.MST=1)中，SSIE使用音频时钟(AUDIO_MCK)运行。要完全停止SSIE，请确保SSIE处于空闲状态(SSISR.IIRQ=1)，然后将0写入SSIFCR.ADCKE。如果在SSIE空闲之前将0写入SSIFCR.ADCKE，则按照图41.52中的过程开始通信。

图41.26和图41.27显示了从将该位设置为1到输出到SSIBCK引脚期间的信号操作时序。

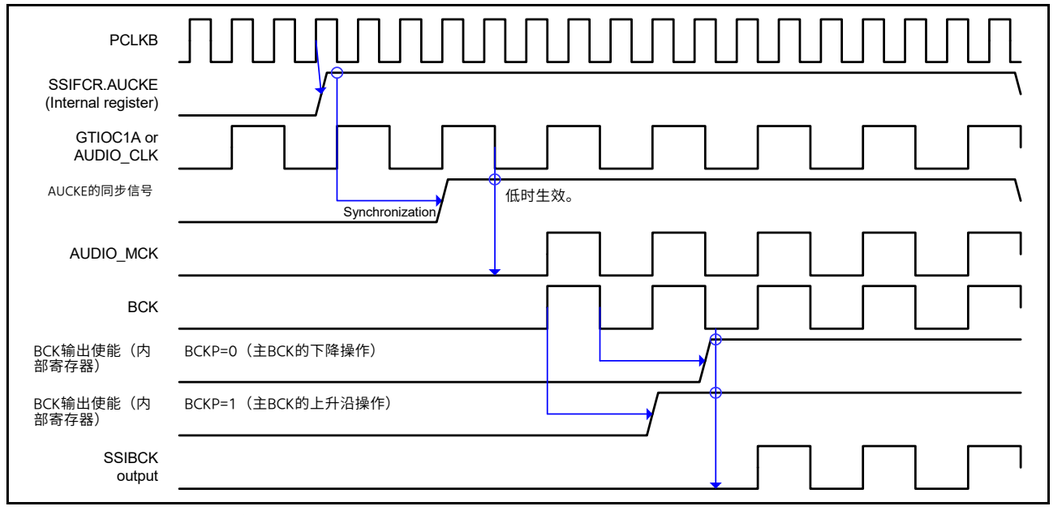


Figure 41.26 从系统复位到主模式通信开始的时序图

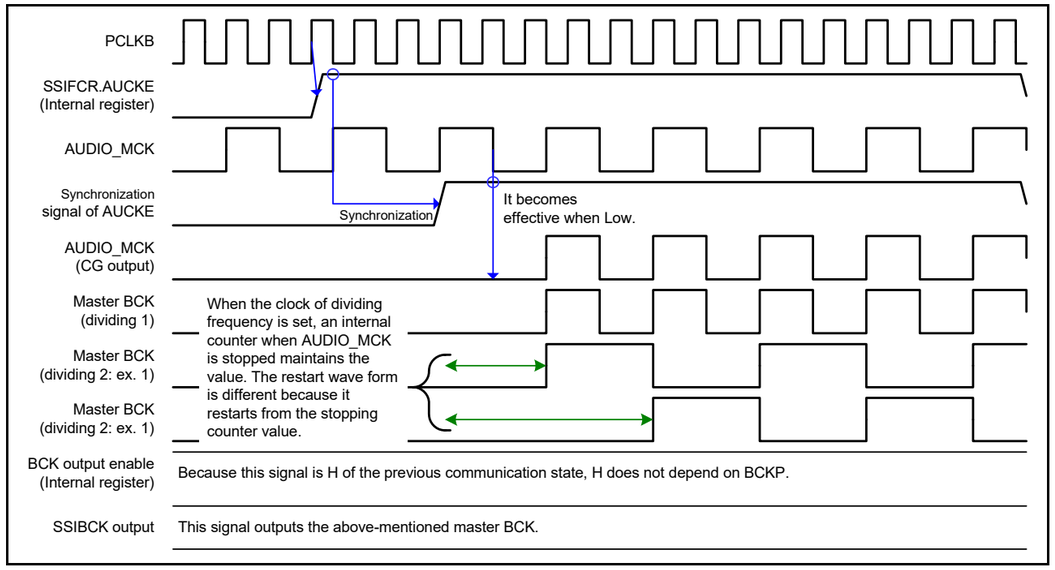


Figure 41.27 Timing diagram for the operation from stop of communication to start of master-mode communication

Note: If the supply of AUDIO_MCK stops, the value of the SSIBCK pin is held. Therefore, the SSIBCK signal might stop in the H (high level) state.

41.4.4 FIFO Status Register (SSIFSR)

Address(es): SSIE0.SSIFSR 4004 E014h, SSIE1.SSIFSR 4004 E114h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	TDC[5:0]						—	—	—	—	—	—	—	TDE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	RDC[5:0]						—	—	—	—	—	—	—	RDF
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	RDF	Receive Data Full Flag	0: The size of received data in SSIFRDR is not more than the value of SSISCR.RDFS 1: The size of received data in SSIFRDR is not less than the value of SSISCR.RDFS plus one.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b13 to b8	RDC[5:0]	Number of Receive FIFO Data Indication Flag	Number of receive FIFO data indication flag.	R
b15, b14	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b16	TDE	Transmit Data Empty Flag	0: The free space of SSIFTDR is not more than the value of SSISCR.TDES 1: The free space of SSIFTDR is not less than the value of SSISCR.TDES plus one.	R/W
b23 to b17	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

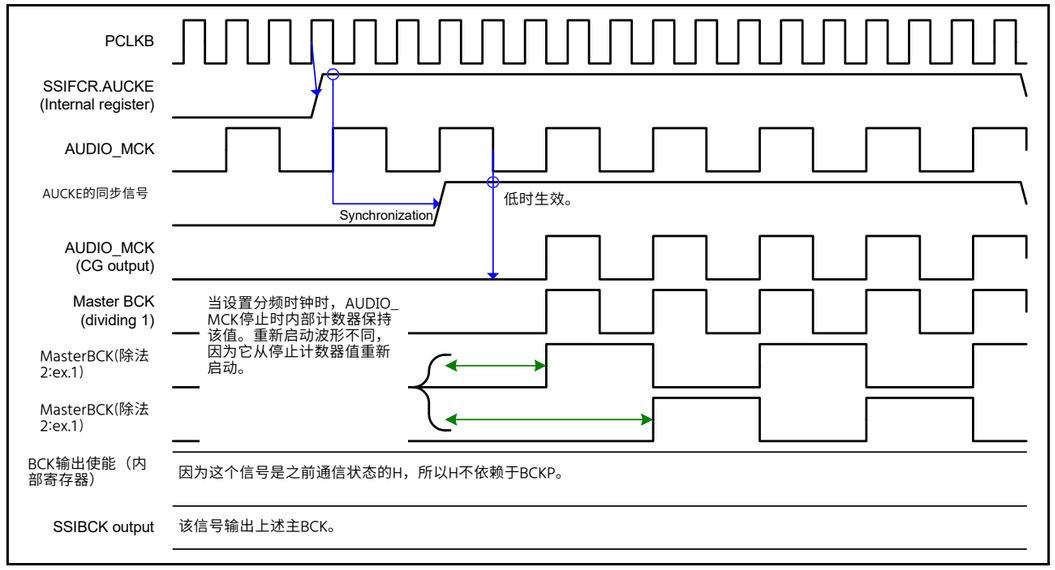


Figure 41.27 从停止通信到开始主模式通信的操作时序图

Note: 如果停止提供AUDIO_MCK，则保持SSIBCK引脚的值。因此，SSIBCK信号可能会停止在H（高电平）状态。

41.4.4 FIFO状态寄存器(SSIFSR)

Address(es): SSIE0.SSIFSR 4004 E014h, SSIE1.SSIFSR 4004 E114h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	TDC[5:0]						—	—	—	—	—	—	—	TDE
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	RDC[5:0]						—	—	—	—	—	—	—	RDF
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	RDF	接收数据满标志	0：SSIFRDR中接收数据的大小不大于SSISCR.RDFS的值1：SSIFRDR中的接收数据的大小不小于SSISCR.RDFS的值加一。	R/W
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b13 to b8	RDC[5:0]	接收FIFO数据的数量指示标志	接收FIFO数据指示标志的数量。	R
b15, b14	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b16	TDE	传输数据空标志	0：SSIFTDR的可用空间不大于SSISCR.TDES的值1：SSIFTDR的可用空间不小于SISSCR.TDES的值加一。	R/W
b23 to b17	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Bit	Symbol	Bit name	Description	R/W
b29 to b24	TDC[5:0]	Number of Transmit FIFO Data Indication Flag	Number of transmit FIFO data indication flag.	R
b31, b30	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

This register is configured with status flags that indicate the status of the transmit FIFO data register and the receive FIFO data register.

RDF bit (Receive Data Full Flag)

This bit indicates that the receive FIFO data register (SSIFRDR) has unread received data not less than the amount set with the SSISCR.RDFS bit plus one. This flag is set by automatic determination but it must be cleared by register access.

[Priority order for setting and clearing]

Clearing is prioritized.

[Clearing condition]

Either of the following two:*1

1. Writing 0 to this bit after reading 1 from this bit (CPU operation)*2
2. Last access (DTC/DMAC operation) to read data from SSIFRDR by an interrupt routine using the DTC and DMAC.

[Clearing timing]

Clearing timing corresponding to the above clearing condition

1. When 0 is written to this bit after reading 1 from this bit (same as the timing in Figure 41.19)
2. After the PCLKB cycle in which the last access instruction is issued to read data from SSIFRDR by an interrupt routine using the DTC and DMAC.

Note 1. These bits are cleared by a software reset (SSIFCR.SSIRST = 1) and receive FIFO data register reset (SSIFCR.RFRST = 1). Reset conditions available for these bits are the software reset and receive FIFO data register reset as well as the clearing conditions described above.

Note 2. After reading 1 from this bit, this bit is cleared when one of the following four conditions is met:
- A software reset is done (SSIFCR.SSIRST = 1).
- A receive FIFO data register reset is done (SSIFCR.RFRST = 1).
- After 1 has been read, writing of 0 is complete.
- Last access is performed to read data from SSIFRDR by an interrupt routine using the DTC and DMAC.

[Setting condition]

SSIFRDR has data not less than the amount set with the SSISCR.RDFS bit plus one.

[Setting timing]

At completion of transfer from the shift register that results in SSIFRDR having data not less than the amount set with the SSISCR.RDFS bit plus one.

Bit	Symbol	位名称	Description	R/W
b29 to b24	TDC[5:0]	发送FIFO数据的数量指示标志	发送FIFO数据指示标志的数量。	R
b31, b30	—	Reserved	这些位被读取为0。写入值应为0。	R/W

该寄存器配置有状态标志，指示发送FIFO数据寄存器和接收
先进先出数据寄存器。

RDF位（接收数据满标志）

该位指示接收FIFO数据寄存器(SSIFRDR)的未读接收数据不少于SSISCR.RDFS位设置的数量加一。该标志由自动确定设置，但必须通过寄存器访问清除。

[设置和清除的优先顺序]

清算优先。

[Clearing condition]

以下两种之一：*1

1. 从该位读取1后向该位写入0（CPU操作）*2
2. 最后一次访问（DTCDMAC操作）通过使用DTC的中断例程从SSIFRDR读取数据和DMAC.

[Clearing timing]

与上述清零条件对应的清零时机

1. 当从该位读取1后向该位写入0时（与图41.19中的时序相同）
2. 在发出最后一个访问指令以通过使用DTC和DMAC的中断例程从SSIFRDR读取数据的PCLKB周期之后。

注1.这些位通过软件复位(SSIFCR.SSIRST=1)和接收FIFO数据寄存器复位清零
（SSIFCR.RFRST=1）。这些位可用的复位条件是软件复位和接收FIFO数据寄存器复位以及上述清除条件。注2.从该位读取1后，当满足以下四个条件之一时，该位被清除：软件复位完成(SSIFCR.SSIRST=1)。完成接收FIFO数据寄存器复位(SSIFCR.RFRST=1)。读取1后，写入0完成。通过使用DTC和DMAC的中断例程执行最后一次访问以从SSIFRDR读取数据。

[Setting condition]

SSIFRDR的数据量不少于用SISSCR.RDFS位加一设置的数量。

[Setting timing]

在完成从移位寄存器的传输时，导致SSIFRDR的数据不少于由SSISCR.RDFS位设置的数量加一。

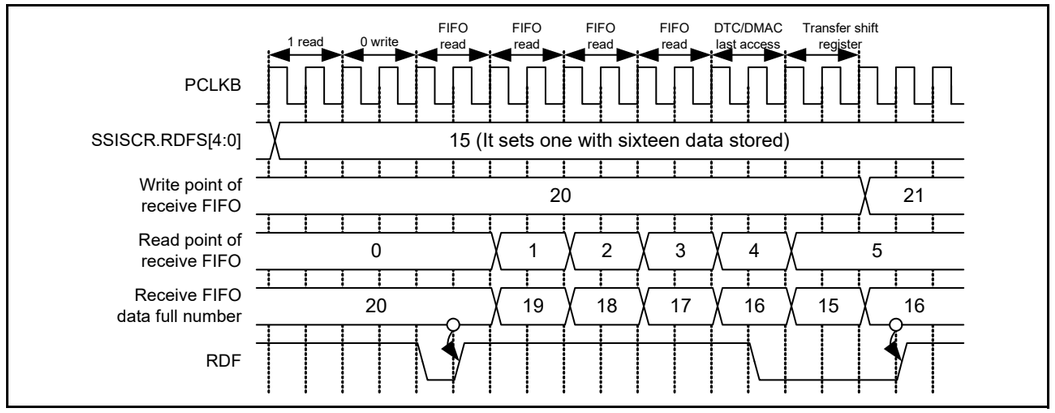


Figure 41.28 Timing diagram for setting and clearing RDF

RDC[5:0] bits (Number of Receive FIFO Data Indication Flag)

These bits indicate the number of valid data that are stored in the receive FIFO data register (SSIFRDR). With this flag as 0h, there is no received data. With 20h, the register is filled with received data and there is no free space.

TDE bit (Transmit Data Empty Flag)

This bit indicates that the transmit FIFO data register (SSIFTDR) has free space not less than the amount set with the SSIFCR.TTRG bit plus one. This flag is set by automatic determination but it must be cleared by register access.

[Priority order for setting and clearing]

Clearing is prioritized.*1

[Clearing condition]

Either of the following two:

1. Writing 0 to this bit after reading 1 from this bit (CPU operation)*2
2. Last access (DTC/DMAC operation) to write data to SSIFTDR by an interrupt routine using the DTC and DMAC.

[Clearing timing]

Clearing timing corresponding to the above clearing condition

(1) When 0 is written to this bit after reading 1 from this bit (same as the timing in Figure 41.19)

(2) Last access (DTC/DMAC operation) to write data to SSIFTDR by an interrupt routine using the DTC and DMAC.

Note 1. This bit is cleared by a software reset (SSIFCR.SSIRST = 1) and transmit FIFO data register reset (SSIFCR.TFRST = 1). The software reset and transmit FIFO data register reset have priority over all the clearing conditions described above.

Note 2. After reading 1 from this bit, this bit is cleared when one of the following four conditions is met:
- A software reset is done (SSIFCR.SSIRST = 1).
- A transmit FIFO data register reset is done (SSIFCR.TFRST = 1).
- After 1 has been read, writing of 0 is complete.
- Last access is performed to write data to SSIFTDR by an interrupt routine using the DTC and DMAC.

[Setting condition]

SSIFTDR has free space not less than the amount set with the SSIFCR.TTRG bit plus one.

[Setting timing]

While operating on PCLKB, SSIFTDR is found to have free space not less than “size set in the SSISCR.TDES bits + 1.”

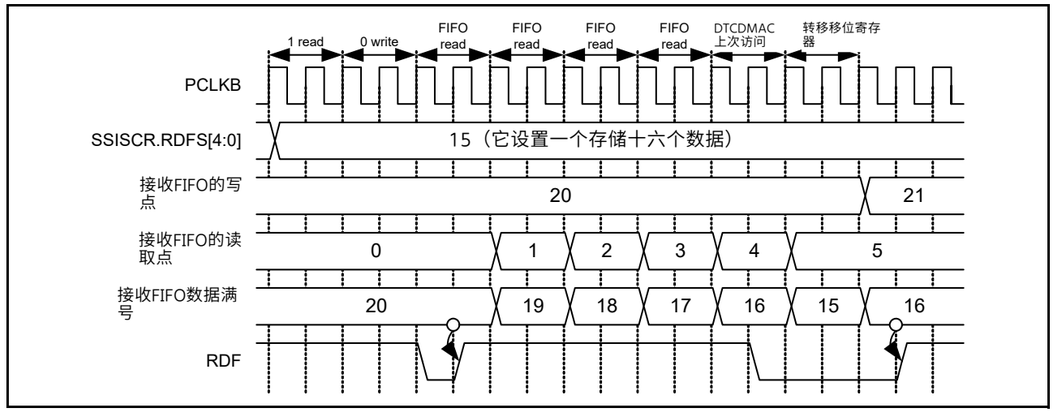


Figure 41.28 设置和清除RDF的时序图

RDC[5:0]位（接收FIFO数据指示标志数）

这些位指示存储在接收FIFO数据寄存器(SSIFRDR)中的有效数据的数量。此标志为0h时，没有接收到数据。20h，寄存器被接收到的数据填满，没有空闲空间。

TDE位（发送数据空标志）

该位表示发送FIFO数据寄存器(SSIFTDR)的可用空间不小于用
SSIFCR.TTRG位加一。该标志由自动确定设置，但必须通过寄存器访问清除。

[设置和清除的优先顺序]

清算优先。*1

[Clearing condition]

以下两种之一：

1. 从该位读取1后向该位写入0（CPU操作）*2
2. 最后一次访问（DTCDMAC操作）通过使用DTC和DMAC的中断例程将数据写入SSIFTDR。

[Clearing timing]

与上述清零条件对应的清零时机

(1)从该位读取1后向该位写入0时（与图41.19中的时序相同）

(2)最后访问（DTCDMAC操作）通过使用DTC和DMAC的中断例程将数据写入SSIFTDR。

注1.该位通过软件复位(SSIFCR.SSIRST=1)和发送FIFO数据寄存器复位清零
（SSIFCR.TFRST=1）。软件复位和发送FIFO数据寄存器复位优先于上述所有清除条件。注2.从该位读取1后，当满足以下四个条件之一时，该位被清除：软件复位完成(SSIFCR.SSIRST=1)。发送FIFO数据寄存器复位完成(SSIFCR.TFRST=1)。读取1后，写入0完成。通过使用DTC和DMAC的中断例程执行最后一次访问以将数据写入SSIFTDR。

[Setting condition]

SSIFTDR的可用空间不小于SSIFCR.TTRG位设置的数量加一。

[Setting timing]

在PCLKB上运行时，发现SSIFTDR的可用空间不小于“SSISCR.TDES位中设置的大小+1”。

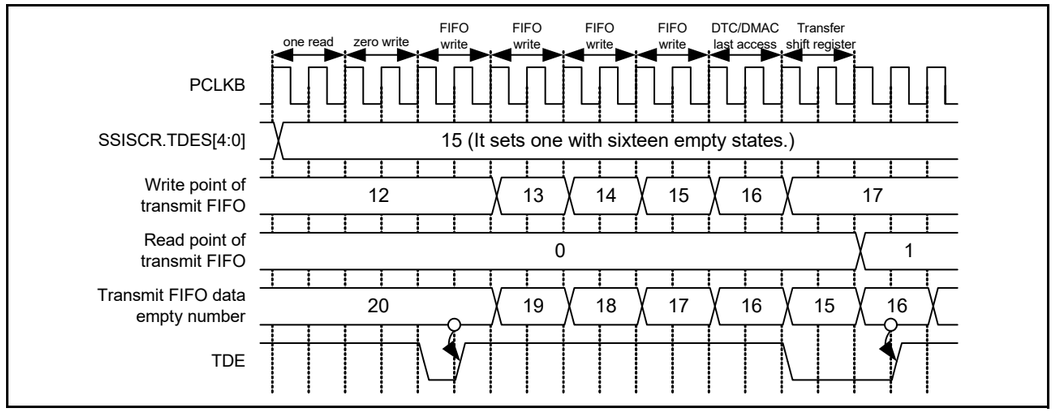


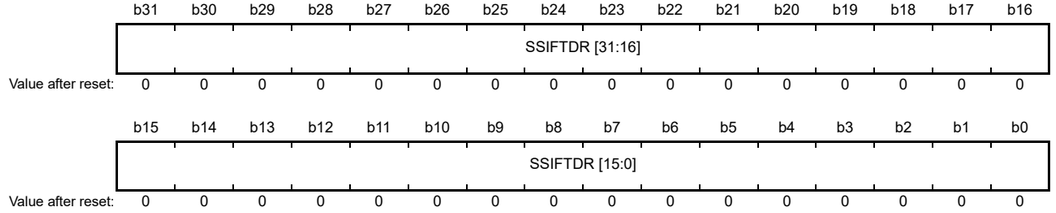
Figure 41.29 Timing diagram for setting and clearing TDE

TDC[5:0] bits (Number of Transmit FIFO Data Indication Flag)

These bits indicate the number of valid data that are stored in the transmit FIFO data register (SSIFTDR). With this flag as 0h, there is no data to be transmitted. With 20h, there is no space to write data.

41.4.5 Transmit FIFO Data Register (SSIFTDR)

Address(es): SSIE0.SSIFTDR 4004 E018h, SSIE1.SSIFTDR 4004 E118h



Bit	Symbol	Bit name	Description	R/W
b31 to b0	SSIFTDR[31:0]	Transmit FIFO Data	Transmit FIFO data.	W

This register stores data to be serially transmitted. 0 is returned when this register is read.

When you use this register for transmission, specify data writing to this register as the DTC/DMAC operation that is triggered by a transmit data empty interrupt. Determine the access size to this register according to the data word length to be communicated in Table 41.8.

Table 41.8 Register access restriction to FIFOs

		Access Size		
SSICR.DWL[2:0]	Data Word Length	Byte	Halfword	Word
000b	8	√	—	—
001b	16	—	√	—
010b	18	—	—	√
011b	20	—	—	√
100b	22	—	—	√
101b	24	—	—	√

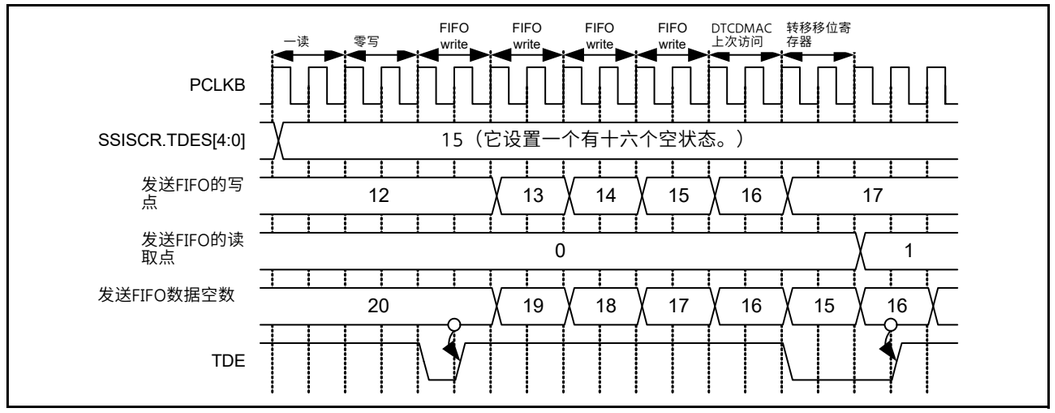


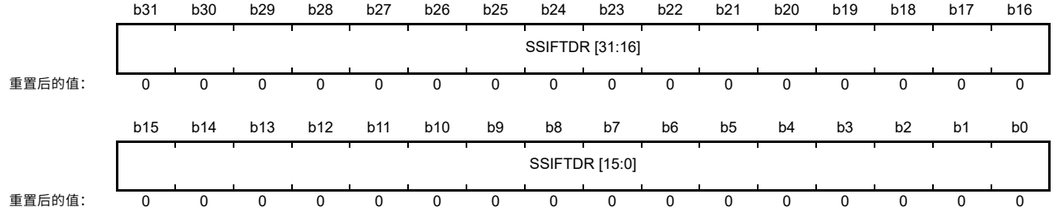
Figure 41.29 设置和清除TDE的时序图

TDC[5:0]位（发送FIFO数据指示标志数）

这些位指示存储在发送FIFO数据寄存器(SSIFTDR)中的有效数据的数量。该标志为0h时，没有要发送的数据。有了20h，就没有写数据的空间了。

41.4.5 发送FIFO数据寄存器(SSIFTDR)

Address(es): SSIE0.SSIFTDR 4004 E018h, SSIE1.SSIFTDR 4004 E118h



Bit	Symbol	位名称	Description	R/W
b31 to b0	SSIFTDR[31:0]	发送FIFO数据	发送FIFO数据。	W

该寄存器存储要串行传输的数据。读取该寄存器时返回0。

当您使用该寄存器进行传输时，将数据写入该寄存器指定为由传输数据空中断触发的DTCDMAC操作。根据表41.8中要通信的数据字长确定对该寄存器的访问大小。

Table 41.8 寄存器对FIFO的访问限制

		访问大小		
SSICR.DWL[2:0]	数据字长	Byte	Halfword	Word
000b	8	√	—	—
001b	16	—	√	—
010b	18	—	—	√
011b	20	—	—	√
100b	22	—	—	√
101b	24	—	—	√

Table 41.8 Register access restriction to FIFOs

	Access Size			
SSICR.DWL[2:0]	Data Word Length	Byte	Halfword	Word
110b	32	—	—	√
111b	Setting prohibited	—	—	—

Figure 41.30 shows register access to the transmit FIFO data register.

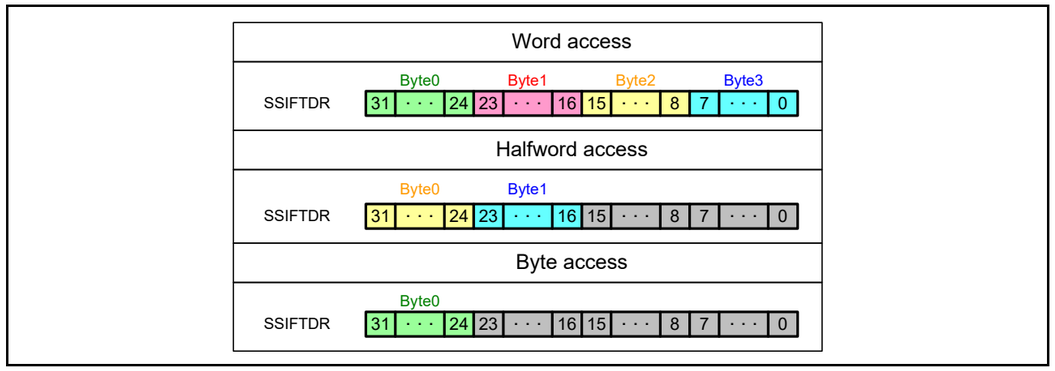


Figure 41.30 Example of register access to the transmit FIFO data register

Figure 41.31 shows the configurations and operation examples of the transmit FIFO data register and transmit shift register. The configurations are for storing data to FIFO and not related with communication.

Table 41.8 寄存器对FIFO的访问限制

	访问大小			
SSICR.DWL[2:0]	数据字长	Byte	Halfword	Word
110b	32	—	—	√
111b	禁止设定	—	—	—

图41.30显示了对发送FIFO数据寄存器的寄存器访问。

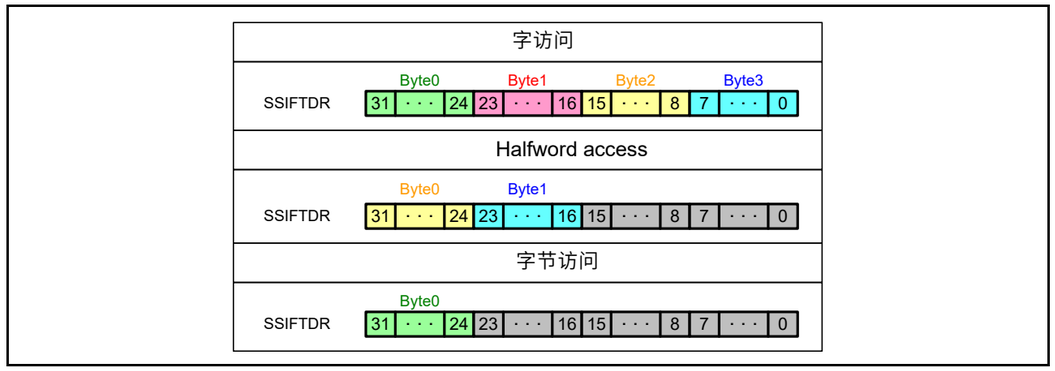


Figure 41.30 对发送FIFO数据寄存器的寄存器访问示例

图41.31显示了发送FIFO数据寄存器和发送移位寄存器的配置和操作示例。该配置用于将数据存储到FIFO，与通信无关。

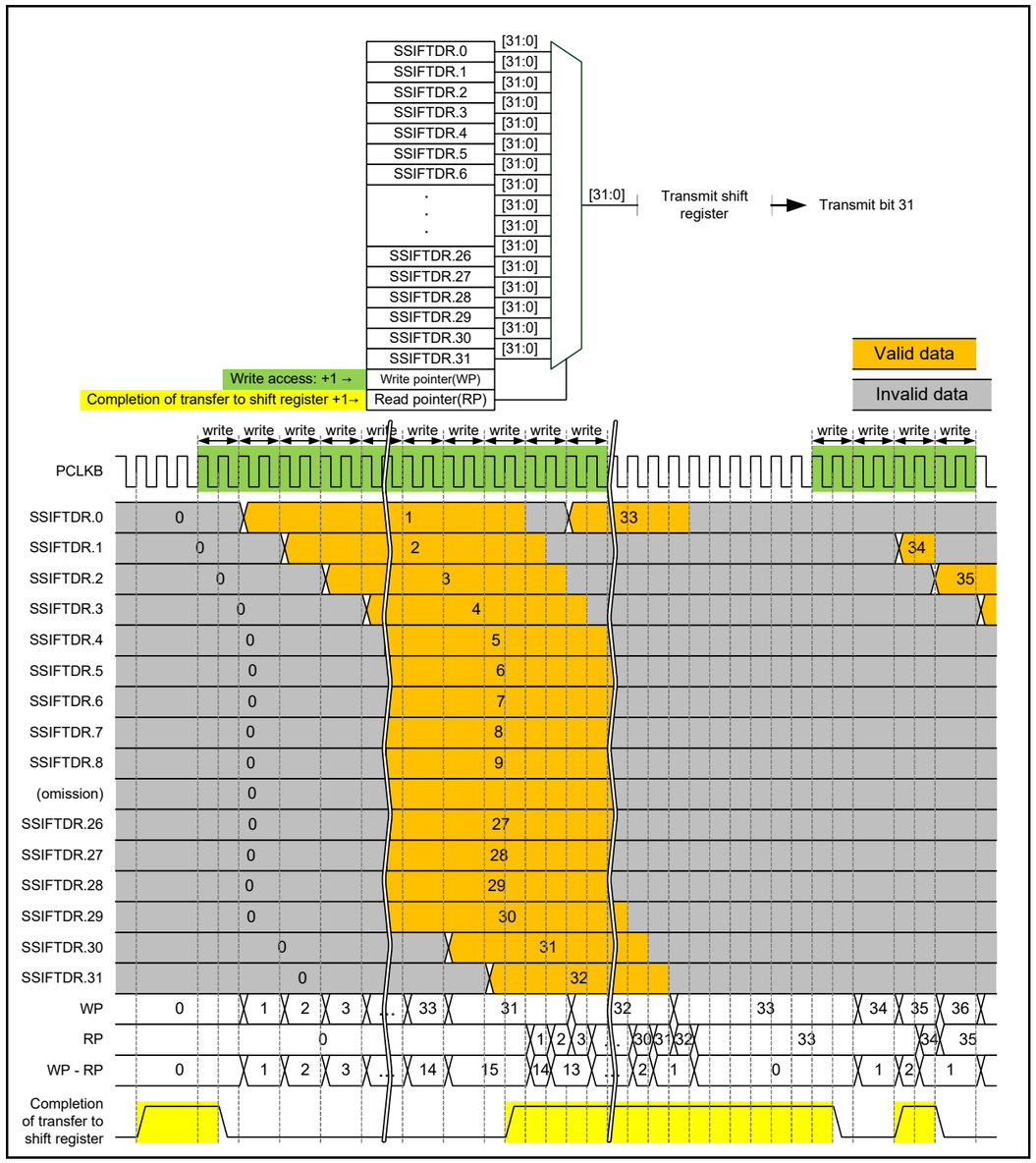


Figure 41.31 Configuration of the transmit FIFO data register and transmit shift register, and FIFO operation example

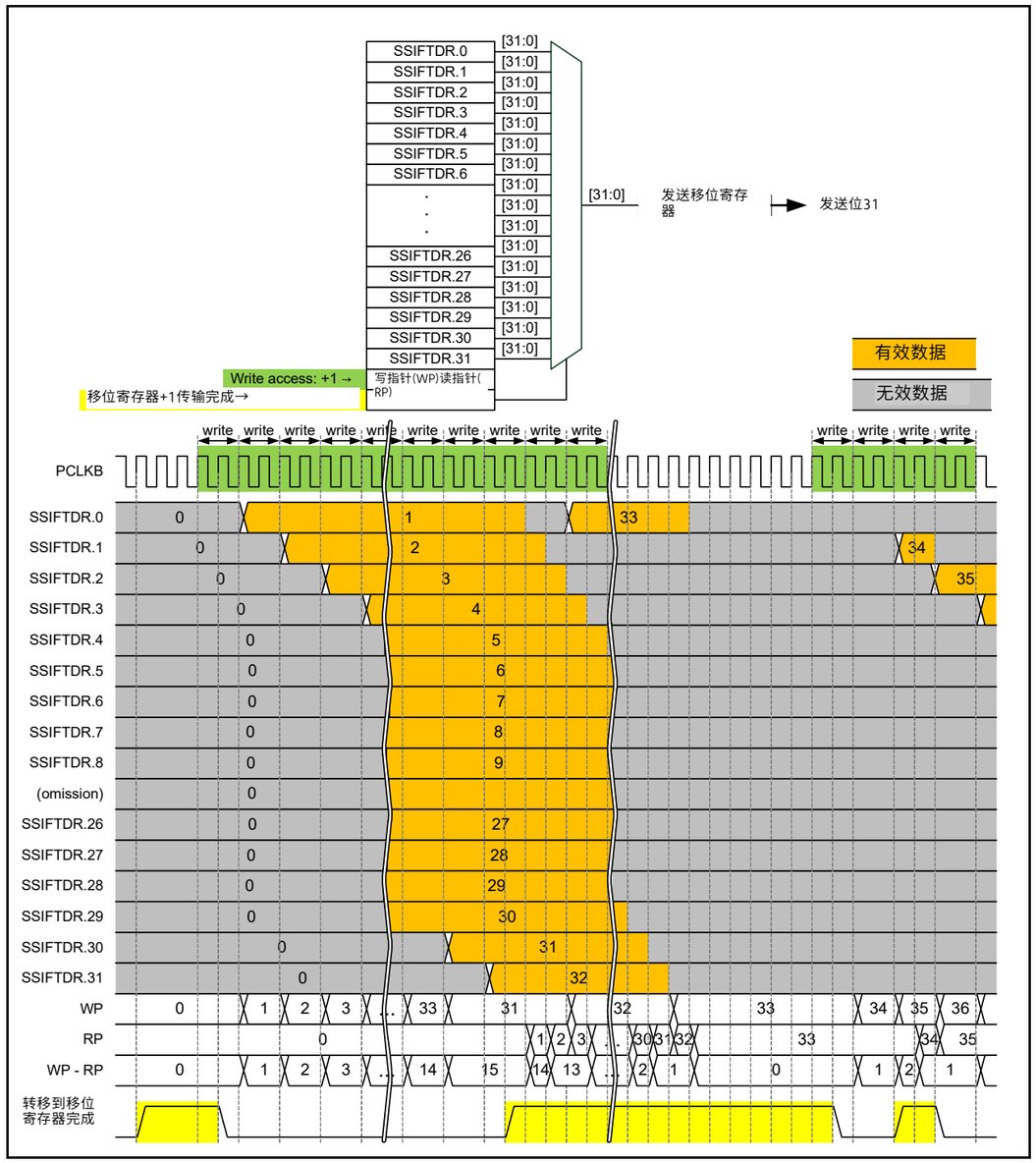


Figure 41.31 发送FIFO数据寄存器和发送移位寄存器的配置，以及FIFO操作示例

41.4.6 Receive FIFO Data Register (SSIFRDR)

Address(es): SSIE0.SSIFRDR 4004 E01Ch, SSIE1.SSIFRDR 4004 E11Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	SSIFRDR [31:16]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SSIFRDR [15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b31 to b0	SSIFRDR[31:0]	Receive FIFO Data	Receive FIFO data.	R

When you use this register for reception, specify data reading from this register as the DTC/DMAC operation that is triggered by a receive data full interrupt. Determine the access size to this register according to the data word length to be communicated in Table 41.8.

Register access to the receive FIFO data register is same as for the transmit FIFO data register.

Figure 41.31 shows the configurations and operation examples of the receive FIFO data register and receive shift register.

41.4.6 接收FIFO数据寄存器(SSIFRDR)

Address(es): SSIE0.SSIFRDR 4004 E01Ch, SSIE1.SSIFRDR 4004 E11Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	SSIFRDR [31:16]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SSIFRDR [15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b31 to b0	SSIFRDR[31:0]	接收FIFO数据	接收FIFO数据。	R

当您使用该寄存器进行接收时，将从该寄存器读取的数据指定为由接收数据满中断触发的DTCDMAC操作。根据表41.8中要通信的数据字长确定对该寄存器的访问大小。

对接收FIFO数据寄存器的寄存器访问与对发送FIFO数据寄存器的访问相同。

图41.31显示了接收FIFO数据寄存器和接收移位寄存器的配置和操作示例。

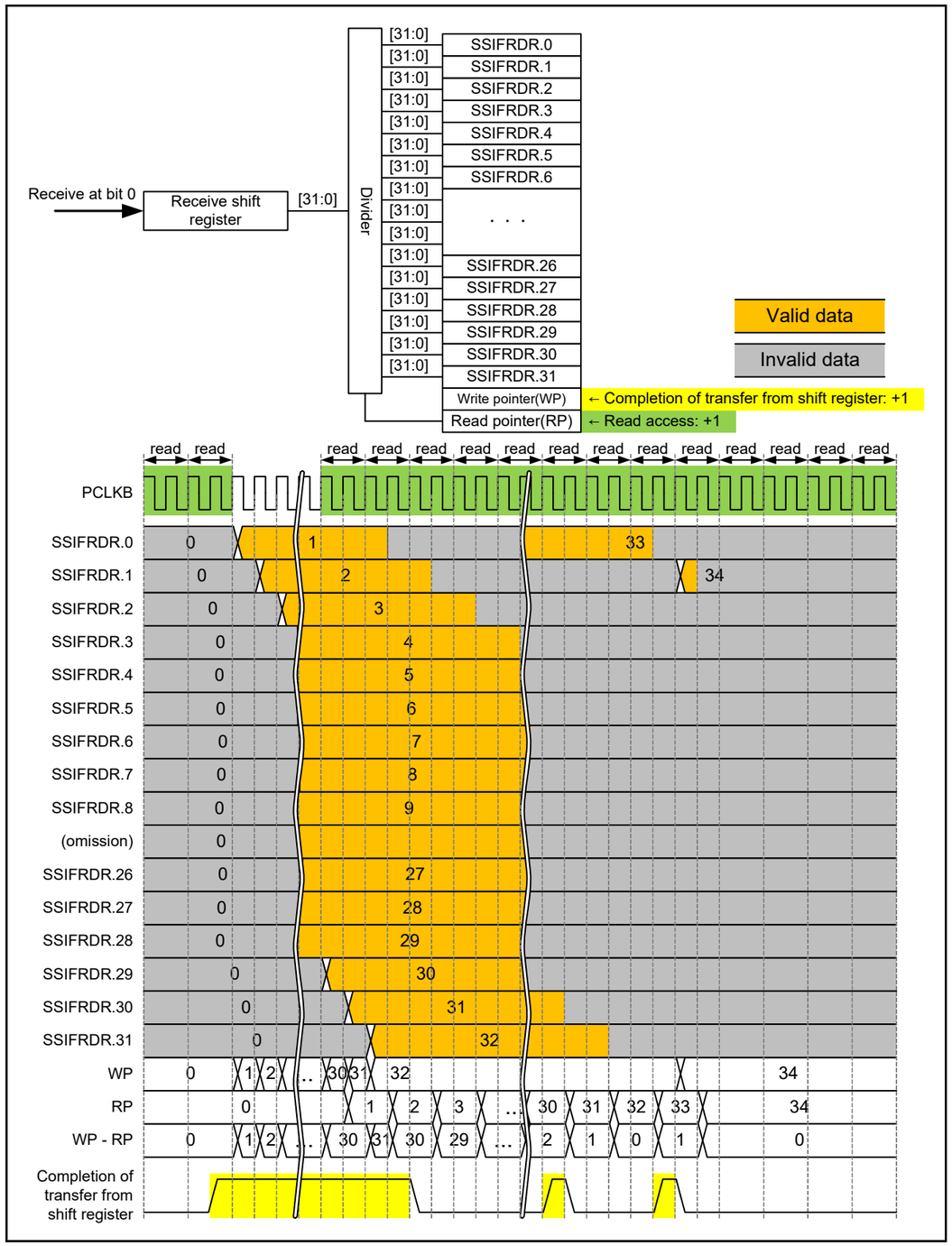


Figure 41.32 Configuration of the transmit FIFO data register and transmit shift register, and FIFO operation example

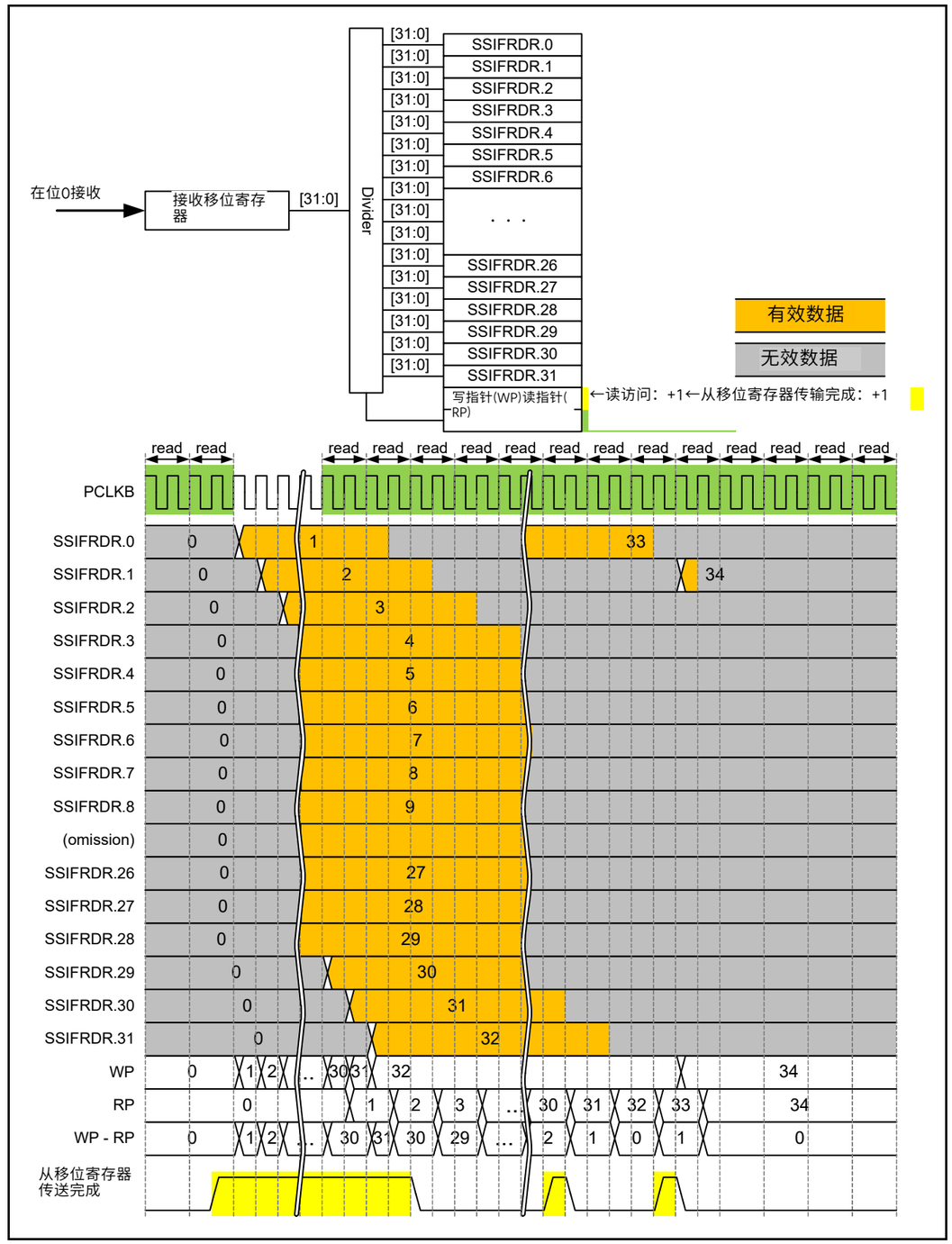


Figure 41.32 发送FIFO数据寄存器和发送移位寄存器的配置，以及FIFO操作示例

41.4.7 Audio Format Register (SSIOFR)

Address(es): SSIE0.SSIOFR 4004 E020h, SSIE1.SSIOFR 4004 E120h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	BCKASTP	LRCONT	—	—	—	—	—	—	OMOD[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	OMOD[1:0]	Audio Format Select*3, *4	00: I²S format 01: TDM format 10: Monaural format 11: Setting prohibited.	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	LRCONT	Whether to Enable LRCK/FS Continuation*1, *2	0: Disables LRCK/FS continuation 1: Enables LRCK/FS continuation.	R/W
b9	BCKASTP	Whether to Enable Stopping BCK Output When SSIE is in Idle Status*1, *2	0: Always outputs BCK to the SSIBCK pin 1: Automatically controls output of BCK to the SSIBCK pin.	R/W
b31 to b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. This bit is valid only in master-mode communication (SSICR.MST = 1). The setting is invalid in slave-mode communication (SSICR.MST = 0).
Note 2. The BCKASTP and LRCONT bits must not be set to 1 together.
Note 3. While SSIE is communicating (SSISR.IIRQ = 0), writing to these bits is prohibited. If the value of these bits is changed by writing, subsequent operation is unpredictable.
Note 4. If the communication format of other-party device is compatible with a communication format of SSIE, specify and use the communication format that enables communication with the other-party device.

This register is used to set an audio format (which involves the settings of communication format, LR clock/frame synchronization continuation mode, and BCK output stop).

OMOD[1:0] bits (Audio Format Select)

These bits set an audio format. Writing to these bits must be performed when the LR clock supply to the SSILRCK/SSIFS pin is stopped. For details about the output of LR clock, see the detailed description of the LRCONT bit in reference 41.4.7.

LRCONT bit (Whether to Enable LRCK/FS Continuation)

This bit enables or disables the output from SSILRCK/SSIFS pin when the communication mode is master-mode communication (SSICR.MST = 1) and SSIE is in the idle state (SSISR.IIRQ = 1).

Even in the idle state, a signal can output from the SSILRCK/SSIFS pin when this bit is set to 1 (to enable LR clock/frame synchronization continuation) in master mode (SSICR.MST = 1).

41.4.7 音频格式寄存器(SSIOFR)

Address(es): SSIE0.SSIOFR 4004 E020h, SSIE1.SSIOFR 4004 E120h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	BCKASTP	LRCONT	—	—	—	—	—	—	OMOD[1:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b1, b0	OMOD[1:0]	音频格式选择*3 *4	00：I2S格式01：TDM格式10：单声道格式11：禁止设置。	R/W
b7 to b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b8	LRCONT	是否开启LRCKFS Continuation*1, *2	0：禁用LRCKFS延续1：启用LRCKFS延续。	R/W
b9	BCKASTP	SSIE时是否使能停止BCK输出 Idle Status*1, *2	0：始终向SSIBCK引脚输出BCK1：自动控制向SSIBCK引脚输出BCK。	R/W
b31 to b10	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 该位仅在主模式通信(SSICR.MST=1)中有效。该设置在从模式通信中无效(SSICR.MST=0)。
Note 2. BCKASTP和LRCONT位不能一起设置为1。
Note 3. 在SSIE通信时(SSISR.IIRQ=0)，禁止写入这些位。如果这些位的值通过写来改变，后续的操作是不可预知的。
Note 4. 如果对方设备的通信格式与SSIE的通信格式兼容，请指定并使用能够与对方设备进行通信的通信格式。

该寄存器用于设置音频格式（涉及通信格式、LR时钟帧同步持续模式、BCK输出停止的设置）。

OMOD[1:0]位（音频格式选择）

这些位设置音频格式。当LR时钟提供给SSILRCKSSIFS引脚停止。LR时钟输出的详细信息请参见参考文献41.4.7中LRCONT位的详细说明。

LRCONT位（是否启用LRCKFSContinuation）

当通信模式为主机模式通信(SSICR.MST=1)且SSIE处于空闲状态(SSISR.IIRQ=1)时，该位启用或禁用SSILRCKSSIFS引脚的输出。

即使在空闲状态下，当该位在主模式(SSICR.MST=1)下设置为1（以启用LR时钟帧同步继续）时，也可以从SSILRCKSSIFS引脚输出信号。

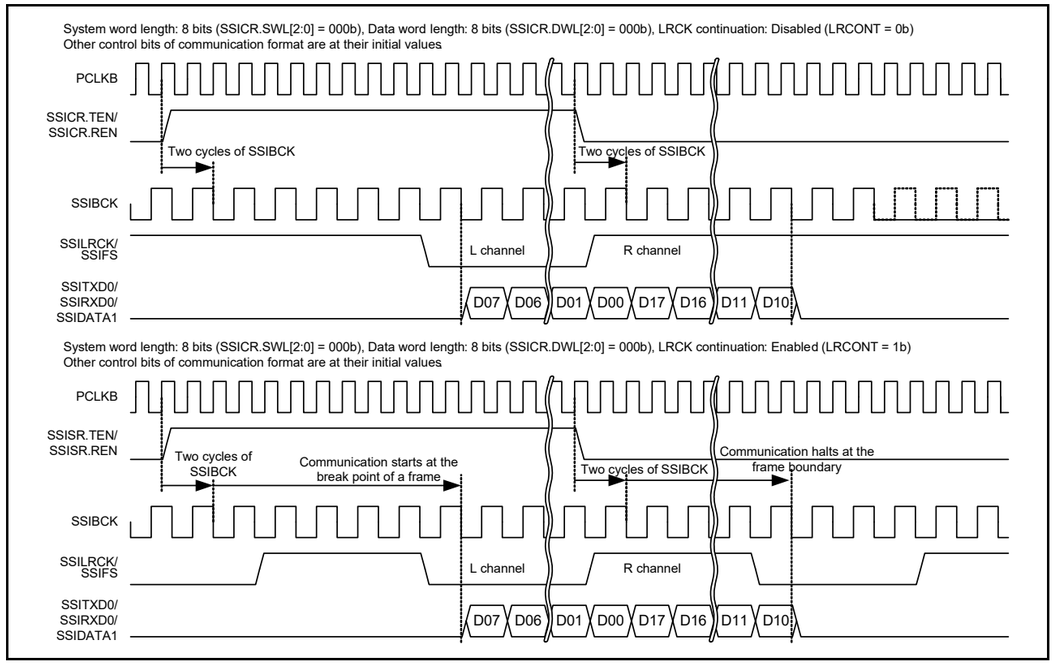


Figure 41.33 Example of LR clock/frame synchronization continuation operation

BCKASTP bit (Whether to Enable Stopping BCK Output When SSIE is in Idle Status)

This bit turns on or off the function to output BCK to the SSIBCK pin according to the communication shown in Figure 41.34 and Figure 41.35 in master-mode communication (SSICR.MST = 1).

Changing the value of this bit must be performed only after setting the communication format to be used.

This bit must be used in the following way:

Write 0 to the BCKASTP bit, and then start communication. During the communication, write 1 to the BCKASTP bit. By this operation, the bit clock output to the SSIBCK pin stops automatically when the communication stops. To resume the communication, set SSIE to the idle state (SSICR.IIRQ = 1), enable the supply of AUDIO_MCK (SSIFCR.AUCKE = 1), and then write 0 to the BCKASTP bit.

When the communication mode is master-mode communication (SSICR.MST = 1) and SSIE is in the idle state (SSICR.IIRQ = 1):

Table 41.9 BCKASTP bit status and SSIBCK pin output

BCKASTP Bit	SSIBCK Pin Output Status
0	Output
1	Stopped

Note: The BCKASTP bit cannot be used when the other-party device (which is a slave) requires the clock output from the SSIBCK pin before and during communication. In such a case, use the BCKASTP bit to stop the clock only after communication. For the timing of enabling the clock stop function, see Figure 41.34.

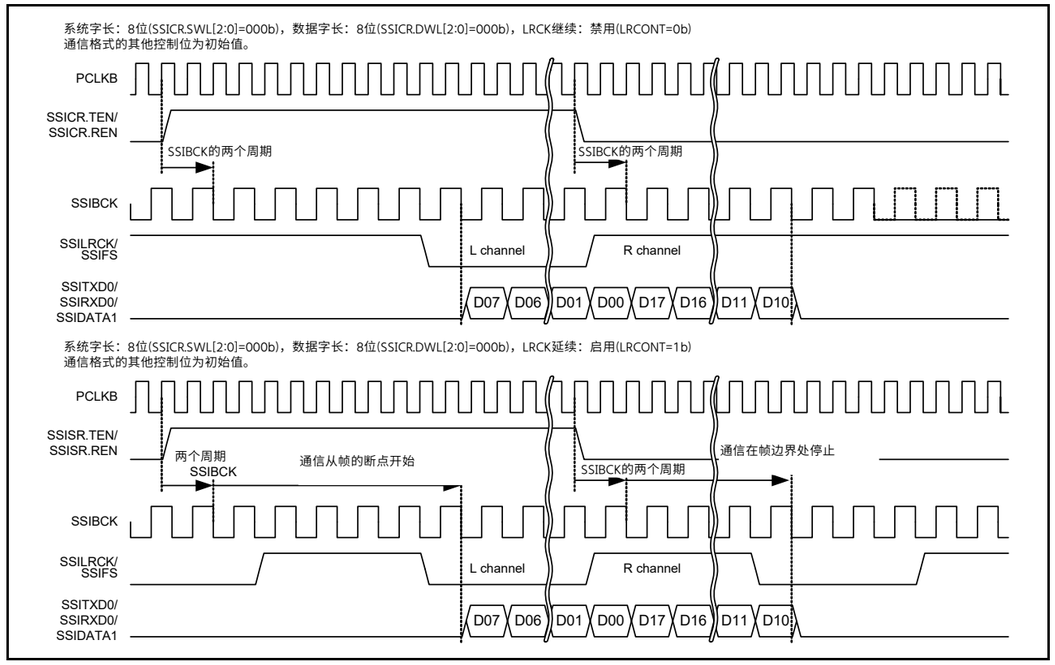


Figure 41.33 LR时钟帧同步继续操作示例

BCKASTP位（SSIE空闲时是否使能停止BCK输出）

该位根据图41.34和图41.35所示的通信在主模式通信(SSICR.MST=1)中打开或关闭将BCK输出到SSIBCK引脚的功能。

只有在设置要使用的通信格式后才能更改该位的值。

该位必须按以下方式使用：

将0写入BCKASTP位，然后开始通信。在通信期间，将1写入BCKASTP位。
通过该操作，当通信停止时，向SSIBCK引脚输出的位时钟自动停止。要恢复通信，请将SSIE设置为空闲状态(SSICR.IIRQ=1)，启用AUDIO_MCK电源(SSIFCR.AUCKE=1)，然后将0写入BCKASTP位。

当通信模式为主模式通信（SSICR.MST=1）且SSIE处于空闲状态（SSICR.IIRQ=1）时：

Table 41.9 BCKASTP位状态和SSIBCK引脚输出

BCKASTP Bit	SSIBCK引脚输出状态
0	Output
1	Stopped

Note: 当对方设备（作为从设备）在通信之前和通信期间需要从SSIBCK引脚输出时钟时，不能使用BCKASTP位。在这种情况下，仅在通信后使用BCKASTP位停止时钟。时钟停止功能的开启时序见图41.34。

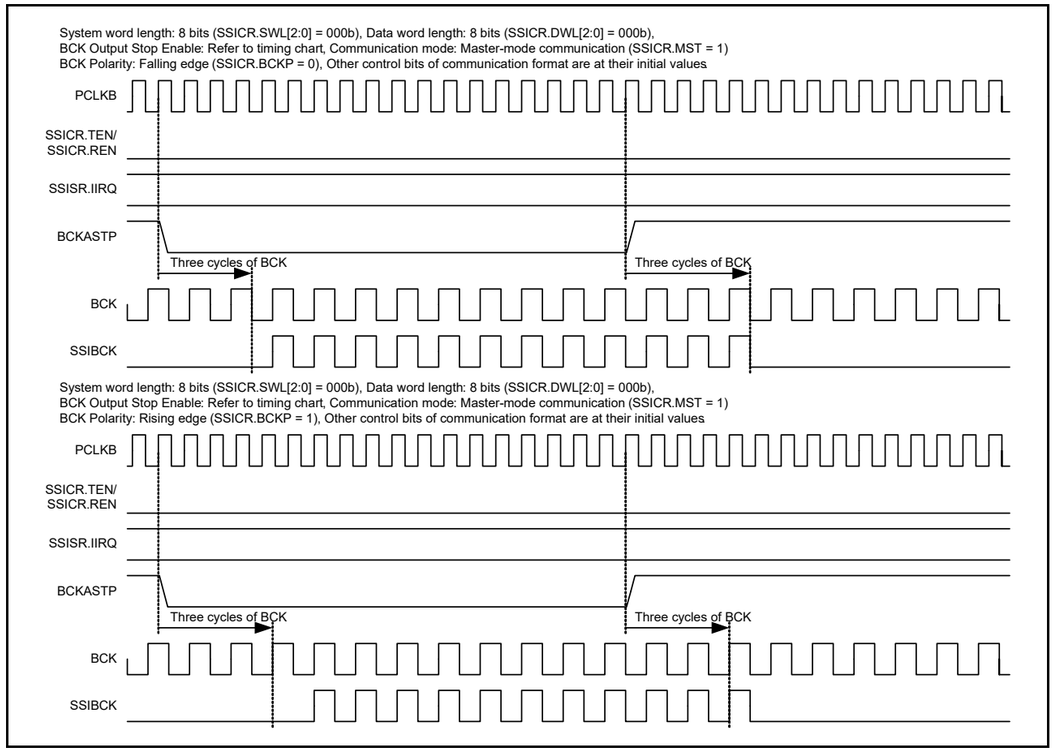


Figure 41.34 Example operation of the BCKASTP bit (idle state)

When the communication mode is master-mode communication (SSICR.MST = 1) and the BCK output stop function is enabled (BCKASTP = 1):

Details of the BCK output to the SSIBCK pin are as follows:

Output start timing: BCK is output in appropriate timing so that a valid edge is generated when the LR clock/frame synchronization signal shifts to a valid value.

Output stop timing: 1 to 1.5 clock cycles after a frame boundary.

For details about the timings, see the timing diagram in Figure 41.35.

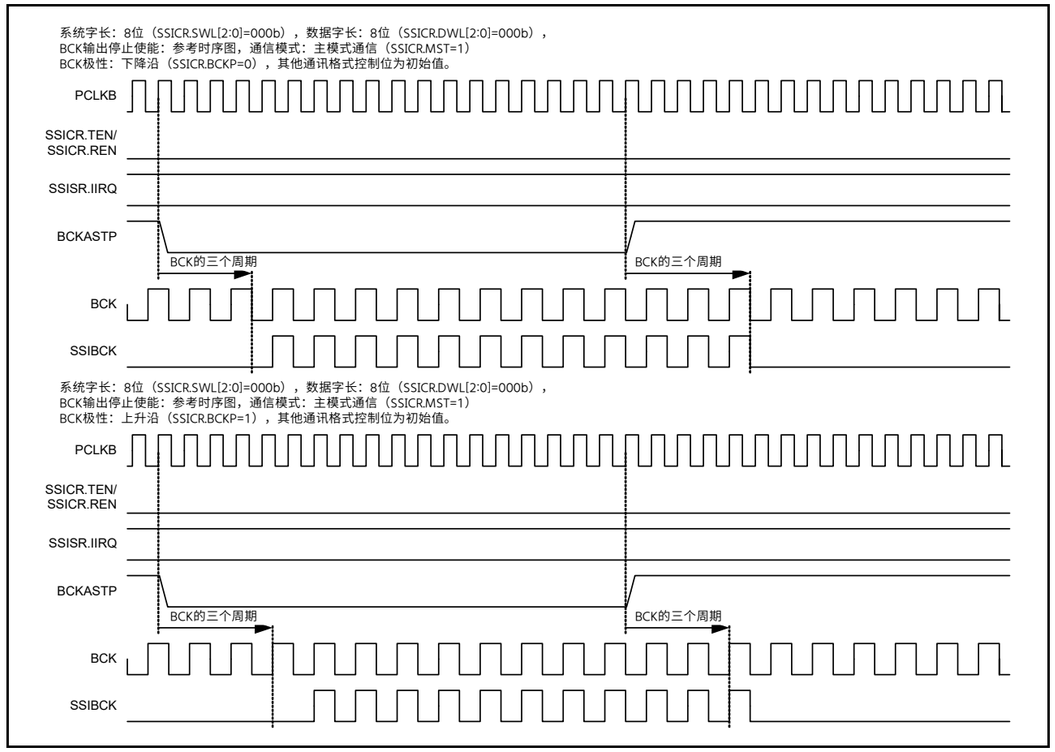


Figure 41.34 BCKASTP位的示例操作（空闲状态）

当通信模式为主机模式通信(SSICR.MST=1)且BCK输出停止功能启用(BCKASTP=1)时：

BCK输出到SSIBCK引脚的详细信息如下：

输出开始时序：在适当的时序输出BCK，以便在LR时钟帧同步信号移位到有效值时产生有效边沿。

输出停止时序：帧边界后1到1.5个时钟周期。

有关时序的详细信息，请参见图41.35中的时序图。

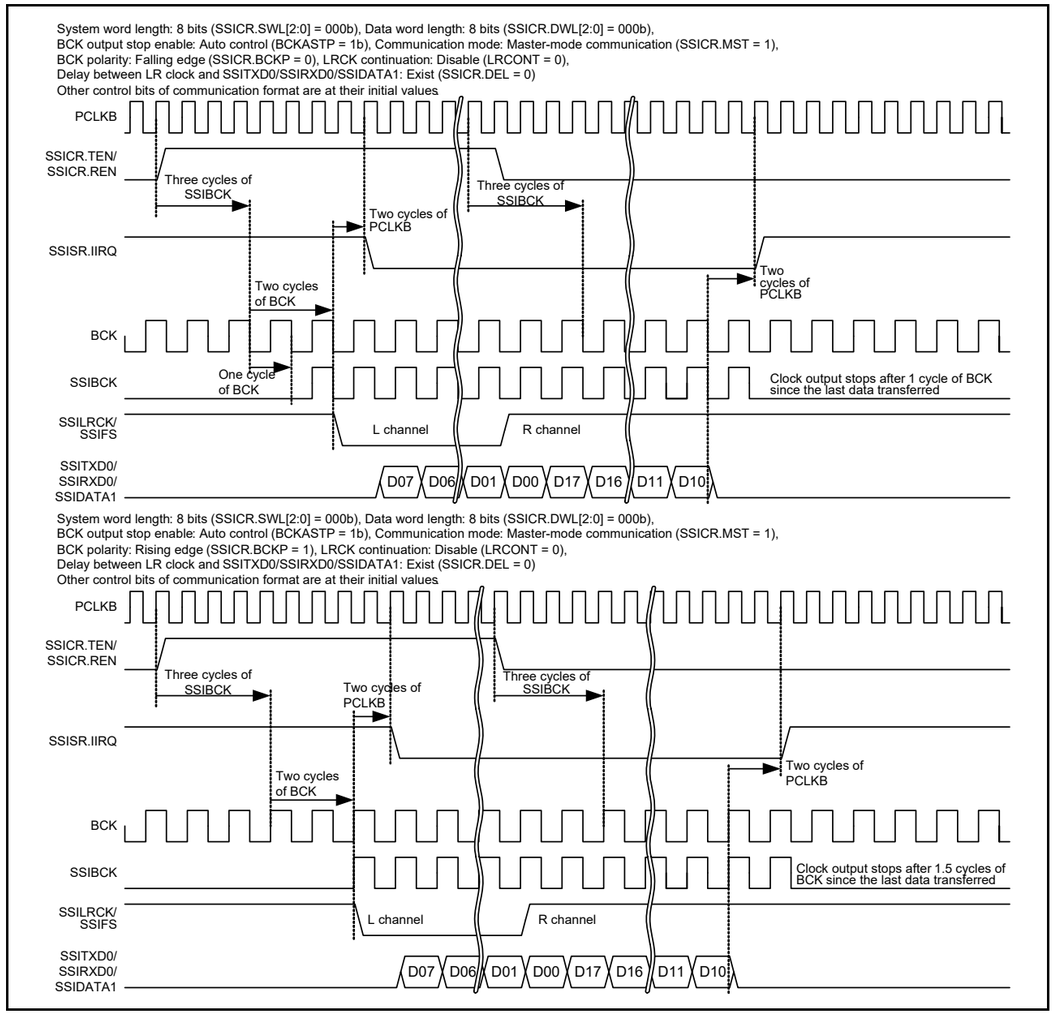


Figure 41.35 Example operation of the BCKASTP bit (communication operation with BCKASTP = 1)

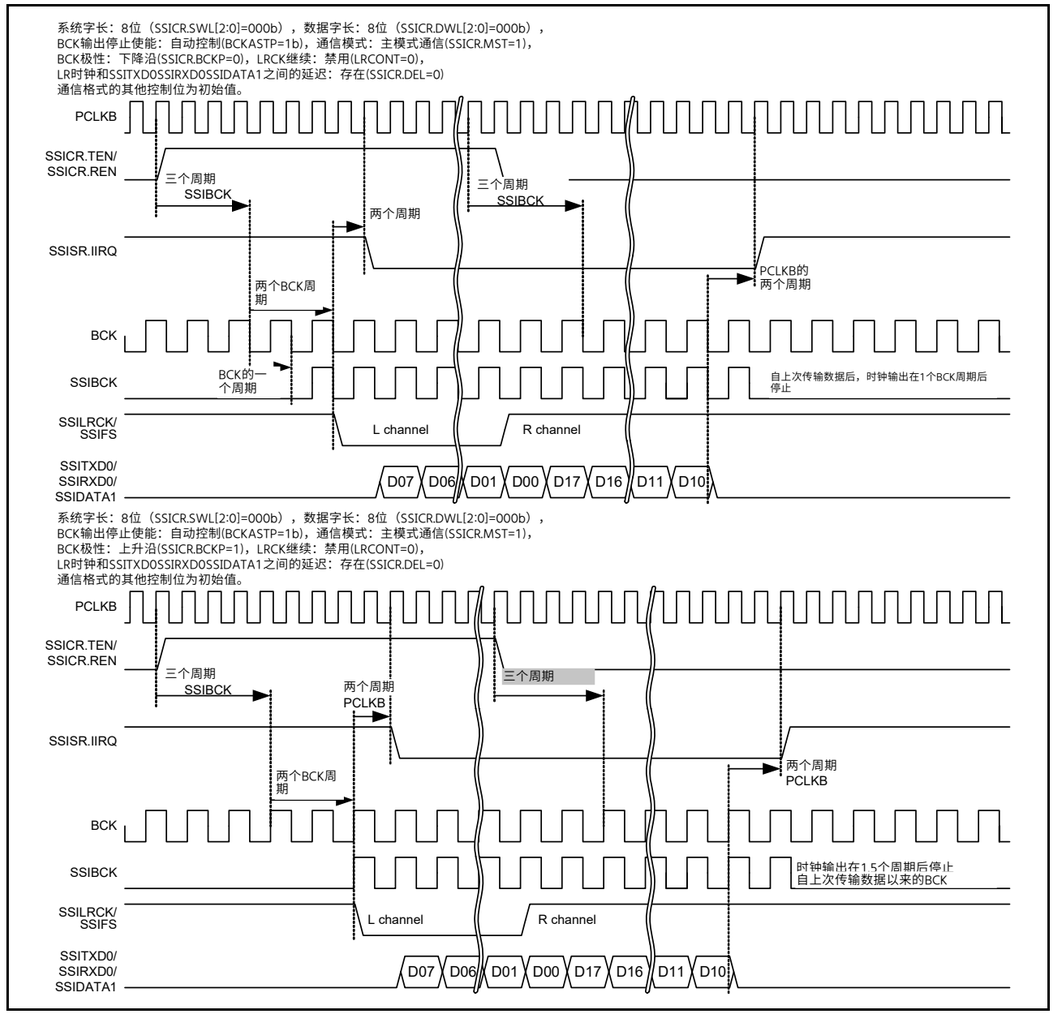


Figure 41.35 BCKASTP位的示例操作（BCKASTP=1的通信操作）

41.4.8 Status Control Register (SSISCR)

Address(es): SSIE0.SSISCR 4004 E024h, SSIE1.SSISCR 4004 E124h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	TDES[4:0]					—	—	—	RDFS[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b4 to b0	RDFS[4:0]	RDF Setting Condition Select*1	b4 b0 0 0 0 0 0: SSIFRDR has one stage or more data size 0 0 0 0 1: SSIFRDR has two stages or more data size (snip) … 1 1 1 1 0: SSIFRDR has thirty-one stages or more data size 1 1 1 1 1: SSIFRDR has thirty-two stages or more data size.	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b12 to b8	TDES[4:0]	TDE Setting Condition Select*1	b12 b8 0 0 0 0 0: SSIFTDR has one stage or more free space 0 0 0 0 1: SSIFTDR has two stages or more free space (snip) … 1 1 1 1 0: SSIFTDR has thirty-one stages or more free space 1 1 1 1 1: SSIFTDR has thirty-two stages or more free space.	R/W
b31 to b13	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Writing to these bits while SSIE is in a communication state (SSISR.IIRQ = 0) is prohibited. If written, the operation performed immediately after writing is not guaranteed.

RDFS[4:0] bits (RDF Setting Condition Select)

These bits set the setting condition of the receive data full flag (RDF).

TDES[4:0] bits (TDE Setting Condition Select)

These bits set the setting condition of the transmit data empty flag (TDE).

41.5 Communication Formats

SSIE supports three communication formats. Table 41.10 shows supported communication formats.

Table 41.10 Supported communication formats

Communication Format	SSIOFR.OMOD[1:0]
I²S format	00
TDM format	01
Monaural format	10

The following describes the serial data structure shared by communication formats. A serial data structure is defined by the system word length (set in SSICR.SWL[2:0]) and the data word length (set in SSICR.DWL[2:0]). If the data word length is shorter than the system word length, padding bits are transferred in the serial data. For details, see Figure 41.36.

41.4.8 状态控制寄存器(SISSCR)

Address(es): SSIE0.SSISCR 4004 E024h, SSIE1.SSISCR 4004 E124h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	TDES[4:0]					—	—	—	RDFS[4:0]				
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b4 to b0	RDFS[4:0]	RDF设置条件 Select*1	b4b000000：SSIFRDR具有一级或更多数据大小00001：SSIFRDR具有两级或更多数据大小（片段）……11110：SSIFRDR具有三十一级或更多数据大小11111：SSIFRDR具有32级或更多数据大小。	R/W
b7 to b5	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b12 to b8	TDES[4:0]	TDE设定条件 Select*1	b12b800000：SSIFTDR有1级或更多可用空间00001：SSIFTDR有2级或更多可用空间(snip)…11110：SSIFTDR有31级或更多可用空间11111：SSIFTDR有32级或更多可用空间。	R/W
b31 to b13	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 禁止在SSIE处于通信状态(SSISR.IIRQ=0)时写入这些位。如果写入，则不保证写入后立即执行的操作。

RDFS[4:0]位（RDF设置条件选择）

这些位设置接收数据满标志(RDF)的设置条件。

TDES[4:0]位（TDE设置条件选择）

这些位设置发送数据空标志(TDE)的设置条件。

41.5 通讯格式

SSIE支持三种通信格式。表41.10显示了支持的通信格式。

Table 41.10 支持的通讯格式

通讯格式	SSIOFR.OMOD[1:0]
I²S format	00
TDM format	01
Monaural format	10

下面介绍通信格式共享的串行数据结构。串行数据结构由系统字长（在SSICR.SWL[2:0]中设置）和数据字长（在SSICR.DWL[2:0]中设置）定义。如果数据字长短于系统字长，则在串行数据中传输填充位。详见图41.36。

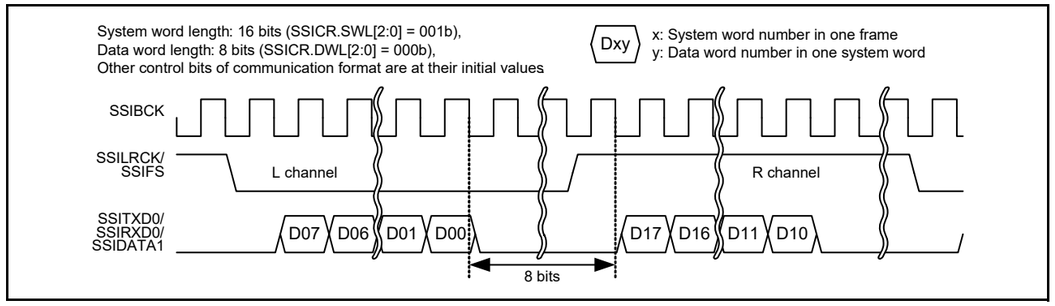


Figure 41.36 Example of padding bit transfer (I²S format: system word length > data word length)

Table 41.11 lists the number of padding bits to be transferred with each combination of system word length (SSICR.SWL[2:0]) and data word length (SSICR.DWL[2:0]). "-" indicates that the setting is prohibited.

Table 41.11 Number of padding bits

	SSICR.DWL[2:0]	000b	001b	010b	011b	100b	101b	110b	111b
SSICR.SWL[2:0]	System Word Length	8	16	18	20	22	24	32	Setting prohibited
000b	8	0	—	—	—	—	—	—	—
001b	16	8	0	—	—	—	—	—	—
010b	24	16	8	6	4	2	0	—	—
011b	32	24	16	14	12	10	8	0	—
100b	48	40	32	30	28	26	24	16	—
101b	64	56	48	46	44	42	40	32	—
110b	128	120	112	110	108	106	104	96	—
111b	256	248	240	238	236	234	232	224	—

41.5.1 I²S Format

The I²S format is a communication format used for connection with I²S-compatible serial devices. With this format setting (SSIOFR.OMOD[1:0] = 00b), one frame is configured with two system words, one for the channel L and the other for channel R. The SSILRCK/SSIFS signals are at a low level for the channel L and at a high level for the channel R. Set the polarity of the signals with the SSICR.LRCKP bit. Figure 41.37 shows the I²S format without padding. See Figure 41.36 for the format with padding.

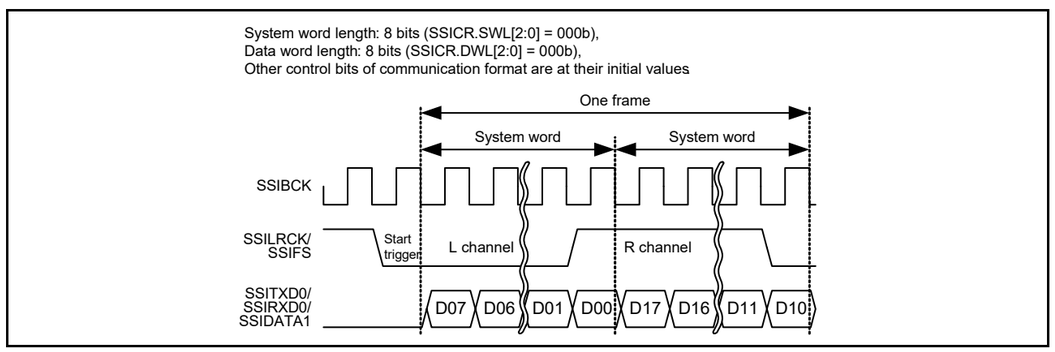


Figure 41.37 I²S format (without padding: system word length = data word length)

For the state of external pins when SSIE is in the idle state, see reference 41.7.1.

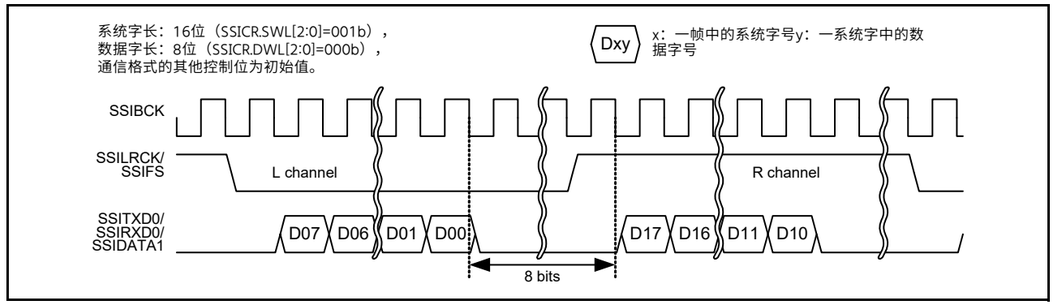


Figure 41.36 填充位传输示例（I2S格式：系统字长>数据字长）

表41.11列出了使用系统字长(SSICR.SWL[2:0])和数据字长(SSICR.DWL[2:0])的每种组合传输的填充位数。"–"表示禁止设置。

Table 41.11 填充位数

	SSICR.DWL[2:0]	000b	001b	010b	011b	100b	101b	110b	111b
SSICR.SWL[2:0]	系统字 Length	8	16	18	20	22	24	32	禁止设置
000b	8	0	—	—	—	—	—	—	—
001b	16	8	0	—	—	—	—	—	—
010b	24	16	8	6	4	2	0	—	—
011b	32	24	16	14	12	10	8	0	—
100b	48	40	32	30	28	26	24	16	—
101b	64	56	48	46	44	42	40	32	—
110b	128	120	112	110	108	106	104	96	—
111b	256	248	240	238	236	234	232	224	—

41.5.1 I²S Format

I2S格式是用于连接I2S兼容串行设备的通信格式。使用此格式设置(SSIOFR.OMOD[1:0]=00b)，一帧配置有两个系统字，一个用于通道L，另一个用于通道R。SSILRCKSSIFS信号对于通道处于低电平L和通道R为高电平。使用SSICR.LRCKP位设置信号的极性。图41.37显示了没有填充的I2S格式。看

图41.36为带有填充的格式。

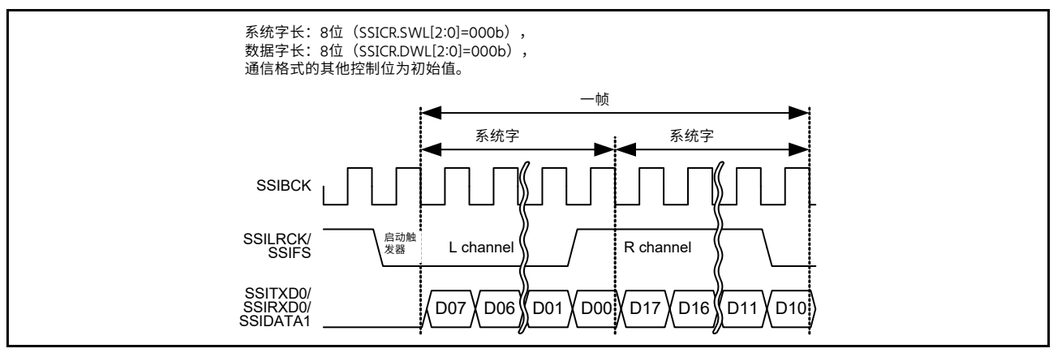


Figure 41.37 I2S格式（无填充：系统字长=数据字长）

SSIE处于空闲状态时外部管脚的状态见参考41.7.1。

Note: SSIE has the SSILRCK/SSIFS pin, which indicates the synchronization of communication. When SSIE is in slave mode (SSICR.MST = 0), the communication format SSIE uses must match that of the other-party device to communicate. SSIE uses the signal input by the SSILRCK/SSIFS pin only as a trigger to start communication.

41.5.2 Monaural Format

The monaural format is a communication format used for connection with monaural-compatible serial devices. When the monaural format is specified (SSIOFR.OMOD[1:0] = 10b) for use, one frame consists of one system word. Also, a rising edge of the SSILRCK/SSIFS signal indicates a communication start trigger. Figure 41.38 and Figure 41.39 respectively show the monaural formats without and with padding.

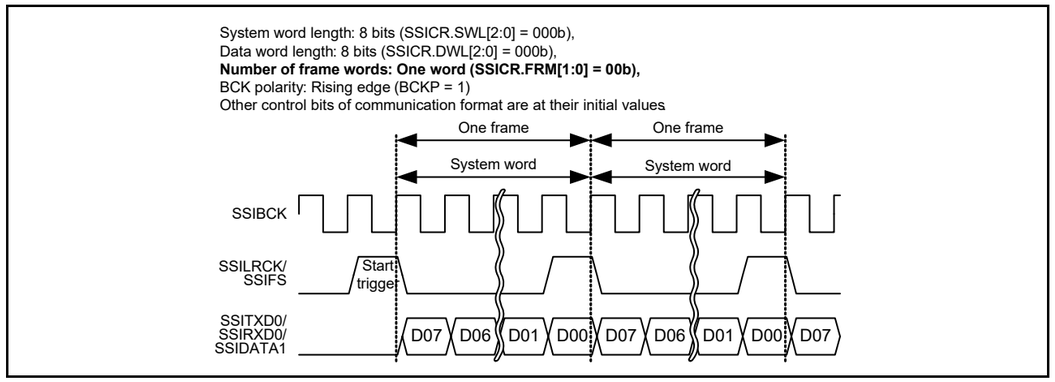


Figure 41.38 Short frame in monaural format (without padding: system word length = data word length)

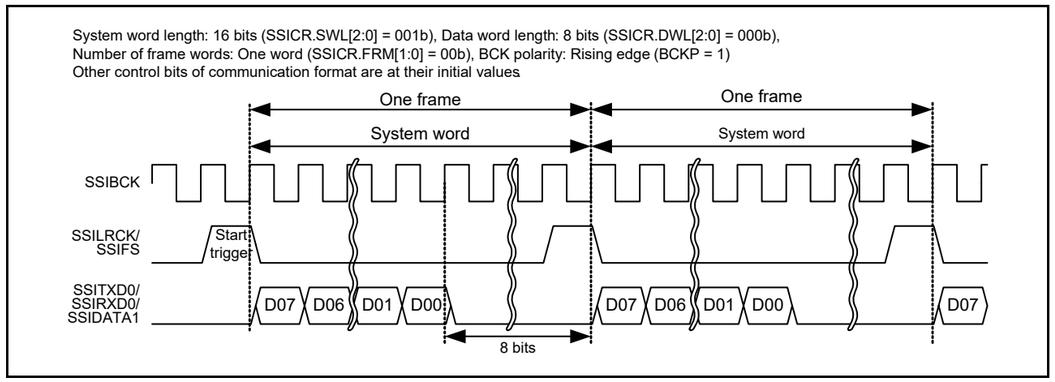


Figure 41.39 Short frame in monaural format (with padding: system word length > data word length)

The monaural formats supported by SSIE consist of short frames and long frames. See reference 41.5.2.1 and reference 41.5.2.2 for the difference between these two frames.

For the state of external pins state when SSIE is in the idle state, see reference 41.7.1.

Note: SSIE has the SSILRCK/SSIFS pin, which indicates the synchronization of communication. When SSIE is in slave mode (SSICR.MST = 0), the communication format SSIE uses must match that of the other-party device to communicate. SSIE uses the signal input by the SSILRCK/SSIFS pin only as a trigger to start communication.

41.5.2.1 Short frame

When a short frame is used (SSICR.DEL = 0), the SSILRCK/SSIFS signal indicating the start of serial data is set to high level only for 1 cycle of SSIBCK. Data transfer starts at the falling edge of the signal.

Note: SSIE有SSILRCKSSIFS引脚，表示通信同步。当SSIE处于从机模式（SSICR.MST=0）时，SSIE使用的通信格式必须与对方设备的通信格式相匹配。SSIE仅使用SSILRCKSSIFS引脚输入的信号作为启动通信的触发器。

41.5.2 Monaural Format

单声道格式是用于连接单声道兼容串行设备的通信格式。当指定使用单声道格式(SSIOFR.OMOD[1:0]=10b)时，一帧由一个系统字组成。此外，SSILRCKSSIFS信号的上升沿表示通信开始触发。图41.38和图41.39分别显示了没有和有填充的单声道格式。

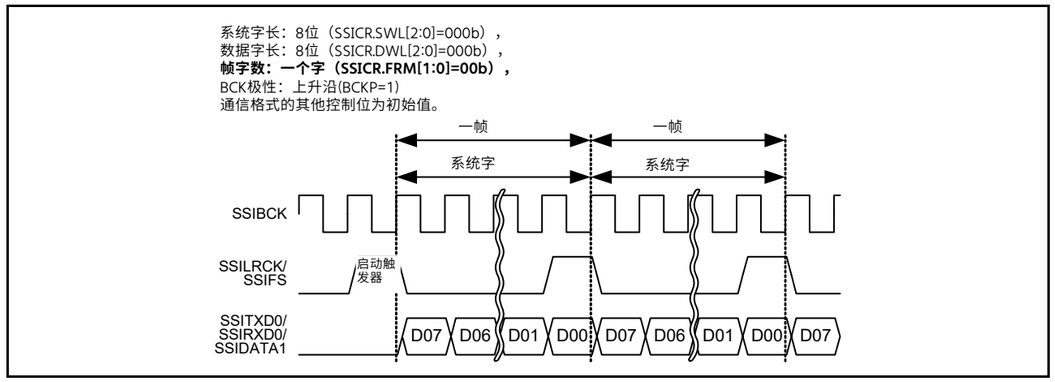


Figure 41.38 单声道格式的短帧（无填充：系统字长=数据字长）

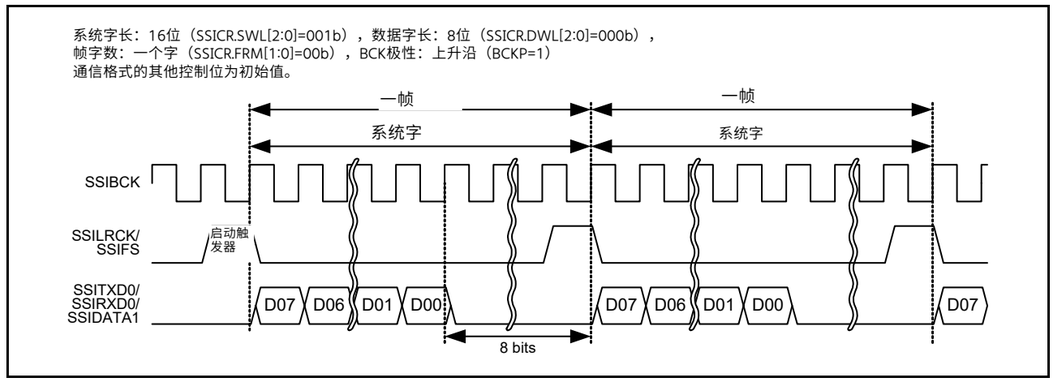


Figure 41.39 单声道格式的短帧（带填充：系统字长>数据字长）

SSIE支持的单声道格式包括短帧和长帧。这两个帧之间的区别参见参考41.5.2.1和参考41.5.2.2。

SSIE处于空闲状态时外部管脚状态的状态见参考41.7.1。

Note: SSIE有SSILRCKSSIFS引脚，表示通信同步。当SSIE处于从机模式（SSICR.MST=0）时，SSIE使用的通信格式必须与对方设备的通信格式相匹配。SSIE仅使用SSILRCKSSIFS引脚输入的信号作为启动通信的触发器。

41.5.2.1 短框

当使用短帧时（SSICR.DEL=0），指示串行数据开始的SSILRCKSSIFS信号仅在SSIBCK的1个周期内设置为高电平。数据传输从信号的下降沿开始。

41.5.2.2 Long frame

When a long frame is used (SSICR.DEL = 1), the SSILRCK/SSIFS signal indicating the start of serial data is set to high level only for 2 cycles of SSIBCK. See Figure 41.40. Data transfer starts at the rising edge of the signal.

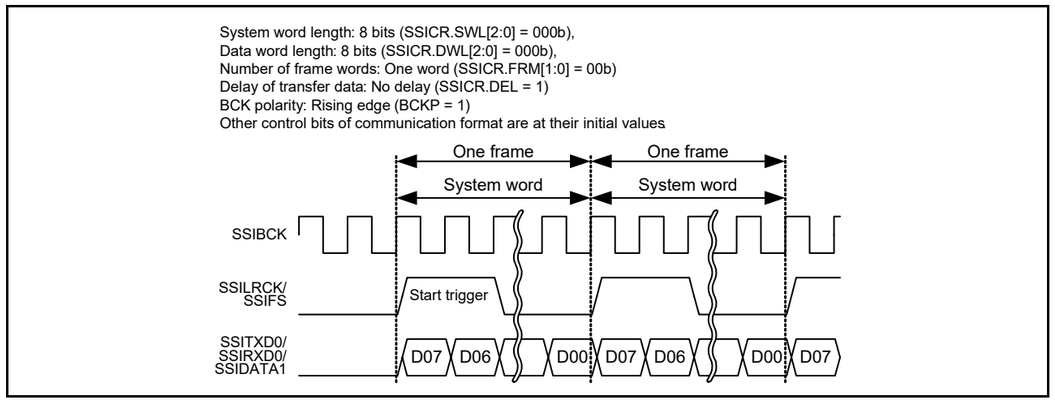


Figure 41.40 Long frame in monaural format (without padding)

41.5.3 TDM Format

The TDM format is a communication format used for connection with TDM-compatible multi-channel devices. With this format setting (SSIOFR.OMOD[1:0] = 01b), one frame is configured with four to eight system words set with the SSICR.FRM[1:0] bits. With this format, the SSILRCK/SSIFS signal is at a high level for the first one system word and at a low level for the rest. The pulse generated on the SSILRCK/SSIFS signal is defined as the SYNC pulse and its rising edge means a start of one frame. Figure 41.41 and Figure 41.42 respectively show the TDM formats without and with padding.

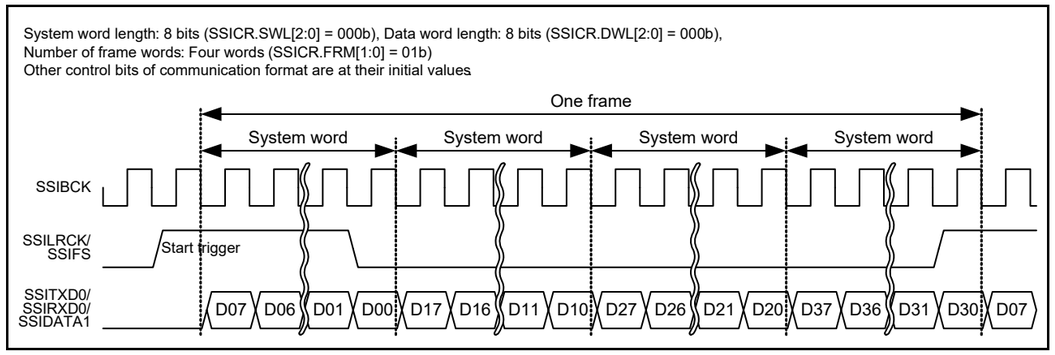


Figure 41.41 TDM format (without padding: system word length = data word length)

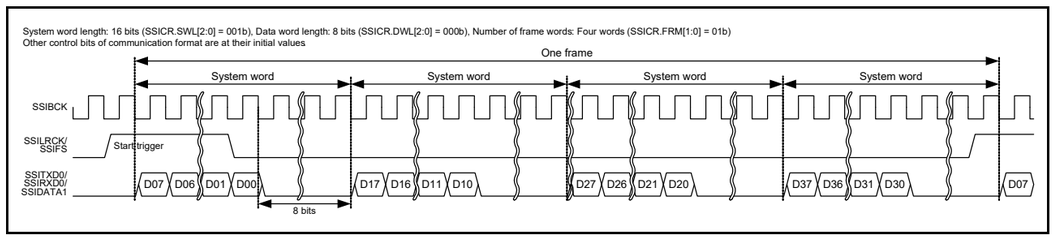


Figure 41.42 TDM format (with padding: system word length > data word length)

41.5.2.2 长框

当使用长帧时（SSICR.DEL=1），指示串行数据开始的SSILRCKSSIFS信号仅在SSIBCK的2个周期内设置为高电平。请参见图41.40。数据传输从信号的上升沿开始。

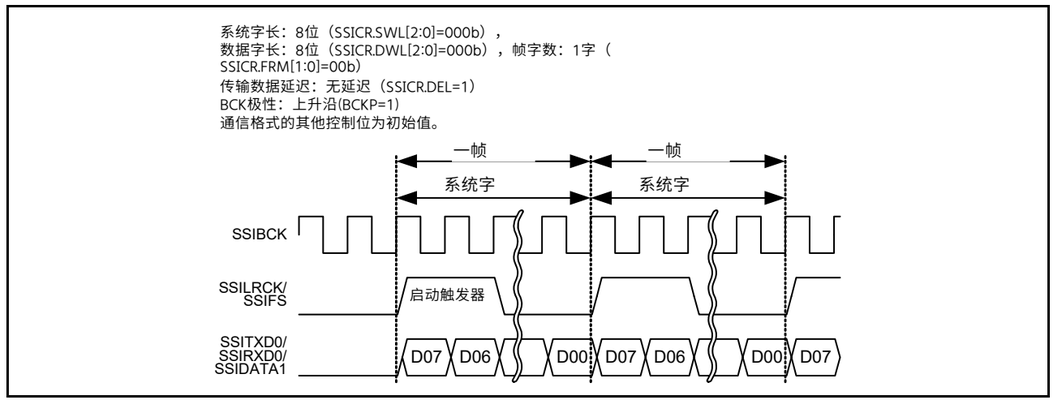


Figure 41.40 单声道格式的长帧（无填充）

41.5.3 TDM Format

TDM格式是一种用于与兼容TDM的多通道设备连接的通信格式。使用此格式设置(SSIOFR.OMOD[1:0]=01b)，一帧配置有四到八个通过SSICR.FRM[1:0]位设置的系统字。使用这种格式，SSILRCKSSIFS信号对于第一个系统字处于高电平，而对于其余系统字处于低电平。SSILRCKSSIFS信号上产生的脉冲被定义为SYNC脉冲，其上升沿表示一帧的开始。图41.41和图41.42分别显示了没有和有填充的TDM格式。

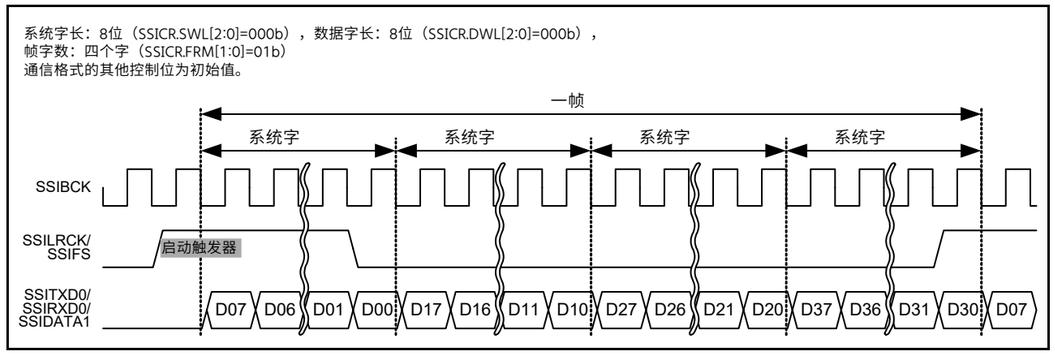


Figure 41.41 TDM格式（无填充：系统字长=数据字长）

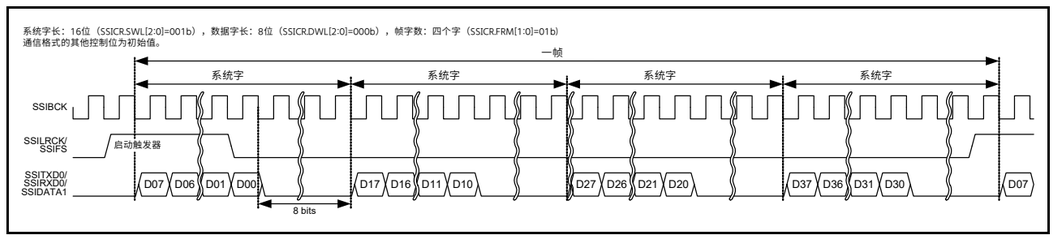


Figure 41.42 TDM格式（带填充：系统字长>数据字长）

For the state of external pins when SSIE is in the idle state, see reference 41.7.1.

Note: SSIE has the SSILRCK/SSIFS pin, which indicates the synchronization of communication. When SSIE is in slave mode (SSICR.MST = 0), the communication format SSIE uses must match that of the other-party device to communicate. SSIE uses the signal input by the SSILRCK/SSIFS pin only as a trigger to start communication.

41.6 Communication Modes

SSIE supports the following communication modes. Table 41.13 lists the control bits that are not available with each communication mode. See reference 41.6.1 to reference 41.6.5 for details of these communication modes.

Table 41.12 Communication modes

Communication Mode	SSICR.MST Bit	SSICR.REN Bit	SSICR.TEN Bit
Slave-mode transmission	0	0	1
Slave-mode reception	0	1	0
Slave-mode transmission and reception	0	1	1
Master-mode transmission	1	0	1
Master-mode reception	1	1	0
Master-mode transmission and reception	1	1	1

Table 41.13 Control bits that cannot be used in each communication mode

Communication Mode / Control Bit	Slave-mode Reception	Slave-mode Transmission	Slave-mode Transmission and Reception	Master-mode Reception	Master-mode Transmission	Master-mode Transmission and Reception
SSICR.CKS	Invalid	Invalid	Invalid	Available	Available	Available
SSICR.CKDV	Invalid	Invalid	Invalid	Available	Available	Available
SSICR.MUEN	Invalid	Available	Available	Invalid	Available	Available
SSICR.TEN	Invalid	Available	Available	Invalid	Available	Available
SSICR.REN	Available	Invalid	Available	Available	Invalid	Available
SSIFCR.AUCKEN	Invalid	Invalid	Invalid	Available	Available	Available
SSIFCR.TIE	Invalid	Available	Available	Invalid	Available	Available
SSIFCR.RIE	Available	Invalid	Available	Available	Invalid	Available
SSIFCR.TFRST	Invalid	Available	Available	Invalid	Available	Available
SSIFCR.RFRST	Available	Invalid	Available	Available	Invalid	Available
SSIOFR.BCKASTP	Invalid	Invalid	Invalid	Available	Available	Available
SSIOFR.LRCONT	Invalid	Invalid	Invalid	Available	Available	Available
SSIOFR.OMOD	Available	Available	Available	Available	Available	Available
SSISCR.TDES	Invalid	Available	Available	Invalid	Available	Available
SSISCR.RDFS	Available	Invalid	Available	Available	Invalid	Available

“Invalid” means it has no effect on operation. Writing is possible.

41.6.1 Slave-mode Communication

SSIE operates in slave mode with SSICR.MST = 0. The SSIBCK and SSILRCK/SSIFS signals to be used for serial-data communication must be supplied from an external device. If these signals do not match the communication format set for SSIE, operation is not guaranteed.

SSIE处于空闲状态时外部管脚的状态见参考41.7.1。

Note: SSIE有SSILRCKSSIFS引脚，表示通信同步。当SSIE处于从机模式（SSICR.MST=0）时，SSIE使用的通信格式必须与对方设备的通信格式相匹配。SSIE仅使用SSILRCKSSIFS引脚输入的信号作为启动通信的触发器。

41.6 通讯方式

SSIE支持以下通信模式。表41.13列出了每种通信模式不可用的控制位。有关这些通信模式的详细信息，请参见参考41.6.1至参考41.6.5。

Table 41.12 通讯方式

通讯方式	SSICR.MST Bit	SSICR.REN Bit	SSICR.TEN Bit
Slave-mode transmission	0	0	1
Slave-mode reception	0	1	0
从模式发送和接收	0	1	1
Master-mode transmission	1	0	1
Master-mode reception	1	1	0
主模式传输和接收	1	1	1

Table 41.13 不能在每种通信模式下使用的控制位

通讯方式 / 控制位	Slave-mode Reception	Slave-mode Transmission	Slave-mode 传输和接收	Master-mode Reception	Master-mode Transmission	主模式传输和接收
SSICR.CKS	Invalid	Invalid	Invalid	Available	Available	Available
SSICR.CKDV	Invalid	Invalid	Invalid	Available	Available	Available
SSICR.MUEN	Invalid	Available	Available	Invalid	Available	Available
SSICR.TEN	Invalid	Available	Available	Invalid	Available	Available
SSICR.REN	Available	Invalid	Available	Available	Invalid	Available
SSIFCR.AUCKEN	Invalid	Invalid	Invalid	Available	Available	Available
SSIFCR.TIE	Invalid	Available	Available	Invalid	Available	Available
SSIFCR.RIE	Available	Invalid	Available	Available	Invalid	Available
SSIFCR.TFRST	Invalid	Available	Available	Invalid	Available	Available
SSIFCR.RFRST	Available	Invalid	Available	Available	Invalid	Available
SSIOFR.BCKASTP	Invalid	Invalid	Invalid	Available	Available	Available
SSIOFR.LRCONT	Invalid	Invalid	Invalid	Available	Available	Available
SSIOFR.OMOD	Available	Available	Available	Available	Available	Available
SSISCR.TDES	Invalid	Available	Available	Invalid	Available	Available
SSISCR.RDFS	Available	Invalid	Available	Available	Invalid	Available

“无效”是指对操作没有影响。写作是可能的。

41.6.1 Slave-mode Communication

SSIE在SSICR.MST=0的从机模式下运行。用于串行数据通信的SSIBCK和SSILRCKSSIFS信号必须由外部设备提供。如果这些信号与为SSIE设置的通信格式不匹配，则无法保证操作。

41.6.2 Master-mode Communication

SSIE operates in master mode with SSICR.MST = 1. The SSIBCK and SSILRCK/SSIFS signals to be used for serial-data communication must be internally generated from the audio clock. These signals use the format according to the setting of SSIE. If the communication format the slave device uses does not match the communication format set for SSIE, the operation is unpredictable.

41.6.3 Transmission

SSIE transmits serial data to the other-party device when the SSICR.TEN bit is 1 and the SSICR.REN bit is 0. If the communication format the other-party device uses does not match the communication format set for SSIE, the operation is unpredictable.

41.6.4 Reception

SSIE receives serial data from the other-party device when the SSICR.TEN bit is 0 and the SSICR.REN bit is 1. If the communication format the other-party device uses does not match the communication format set for SSIE, the operation is unpredictable.

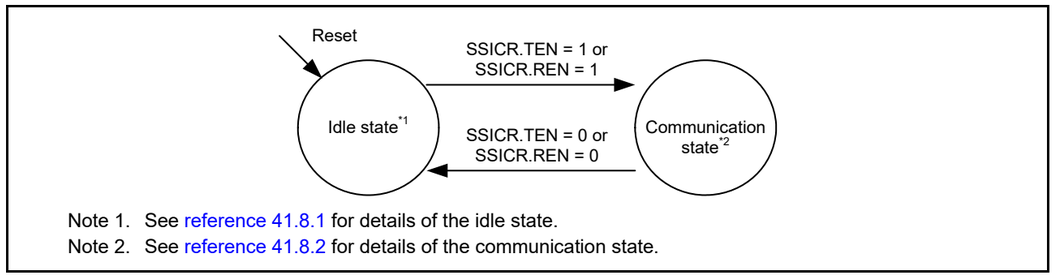
41.6.5 Transmission and Reception

SSIE transmits and receives serial data to and from the other-party device when the SSICR.TEN bit is 1 and the SSICR.REN bit is 1. If the communication format the other-party device uses does not match the communication format set for SSIE, the operation is unpredictable.

41.7 Operation

SSIE has the following two main operation states Figure 41.43 shows SSIE state transition.

- Idle state (SSISR.IIRQ = 1)
- Communication state (SSISR.IIRQ = 0).



Note 1. See reference 41.8.1 for details of the idle state.
Note 2. See reference 41.8.2 for details of the communication state.

Figure 41.43 SSIE state transition

41.7.1 Idle State

In this state, communication of SSIE is halted. If, however, the SSICR.MST bit is 1, output of the BCK and LR clock/frame synchronization signals to external pins can be controlled according to the settings of SSIOFR.BCKASTP and SSIOFR.LRCONT bits. This function is common to all formats. For details, see Table 41.14.

Table 41.14 Output from external pins in the idle state

SSICR.MST	SSIOFR.BCKASTP	SSIOFR.LRCONT	Output from Pins		
			SSIBCK	SSILRCK/SSIFS	SSITXD0/SSIDATA1
0	—	—	Stop	Stop	Stop
1	0	0	Supply	Stop	Stop
1	0	1	Supply	Supply	Stop
1	1	0	Stop	Stop	Stop

41.6.2 Master-mode Communication

SSIE在SSICR.MST=1的主模式下运行。用于串行数据通信的SSIBCK和SSILRCKSSIFS信号必须由音频时钟在内部生成。这些信号根据SSIE的设置使用格式。如果从设备使用的通信格式与为SSIE设置的通信格式不匹配，则操作是不可预测的。

41.6.3 Transmission

当SSICR.TEN位为1且SSICR.REN位为0时，SSIE向对方设备发送串口数据。如果对方设备使用的通信格式与为SSIE设置的通信格式不匹配，则操作为不可预料的。

41.6.4 Reception

当SSICR.TEN位为0且SSICR.REN位为1时，SSIE从对方设备接收串行数据。如果对方设备使用的通信格式与为SSIE设置的通信格式不匹配，则操作为不可预料的。

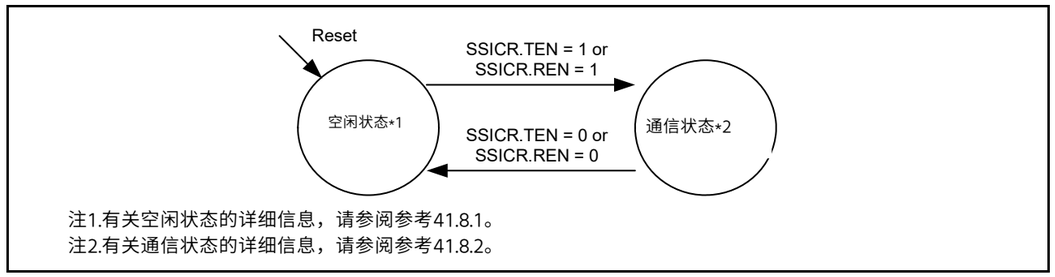
41.6.5 传输和接收

当SSICR.TEN位为1且
SSICR.REN位为1。如果对方设备使用的通信格式与为SSIE设置的通信格式不匹配，则操作不可预知。

41.7 Operation

SSIE有以下两个主要操作状态图41.43显示了SSIE状态转换。

- 空闲状态(SSISR.IIRQ=1)
- 通信状态(SSISR.IIRQ=0)。



注1.有关空闲状态的详细信息，请参阅参考41.8.1。
注2.有关通信状态的详细信息，请参阅参考41.8.2。

Figure 41.43 SSIE状态转换

41.7.1 空闲状态

在这种状态下，SSIE的通信停止。但是，如果SSICR.MST位为1，则可以根据SSIOFR.BCKASTP和SSIOFR.LRCONT位的设置来控制向外部引脚输出BCK和LR时钟帧同步信号。此功能适用于所有格式。详见表41.14。

Table 41.14 空闲状态下外部引脚的输出

SSICR.MST	SSIOFR.BCKASTP	SSIOFR.LRCONT	引脚输出		
			SSIBCK	SSILRCK/SSIFS	SSITXD0/SSIDATA1
0	—	—	Stop	Stop	Stop
1	0	0	Supply	Stop	Stop
1	0	1	Supply	Supply	Stop
1	1	0	Stop	Stop	Stop

Table 41.14 Output from external pins in the idle state

			Output from Pins		
SSICR.MST	SSIOFR.BCKASTP	SSIOFR.LRCONT	SSIBCK	SSILRCK/SSIFS	SSITXD0/SSIDATA1
1	1	1	Stop	Supply	Stop

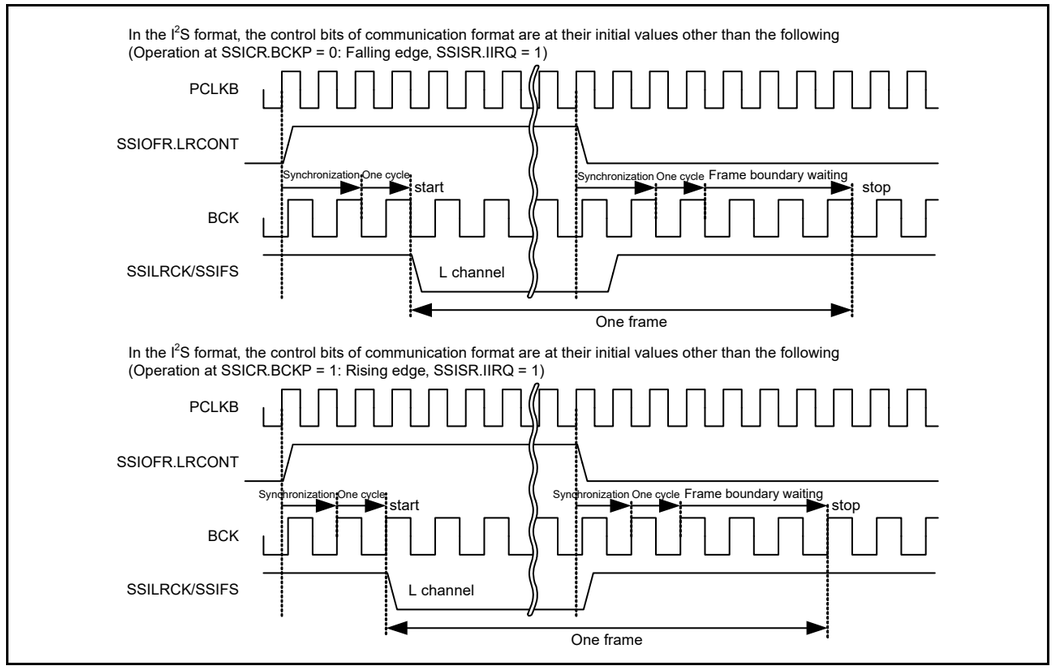


Figure 41.44 Example of disabling LR clock/frame synchronization continuation by SSIOFR.LRCONT

Note: To stop the output to the SSILRCK/SSIFS pin with SSIOFR.LRCONT when SSIE is in the idle state in master-mode communication (SSICR.MST = 1), note the following: The output stops when the value of the SSIOFR.LRCONT bit is changed from 1 to 0. Make sure that the other-party device is not affected.

Table 41.14 空闲状态下外部引脚的输出

			引脚输出		
SSICR.MST	SSIOFR.BCKASTP	SSIOFR.LRCONT	SSIBCK	SSILRCK/SSIFS	SSITXD0/SSIDATA1
1	1	1	Stop	Supply	Stop

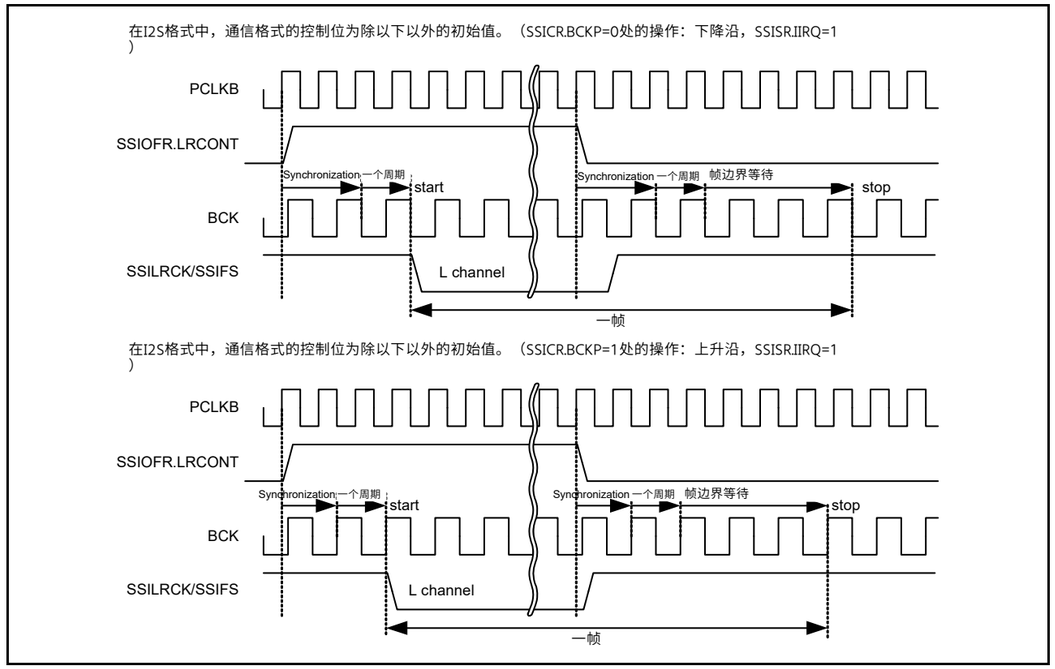


Figure 41.44 通过SSIOFR.LRCONT禁用LR时钟帧同步继续的示例

Note: 要在主模式通信(SSICR.MST=1)中SSIE处于空闲状态时使用SSIOFR.LRCONT停止向SSILRCKSSIFS引脚的输出，请注意以下几点：更改SSIOFR.LRCONT位的值时停止输出从1到0。确保对方设备不受影响。

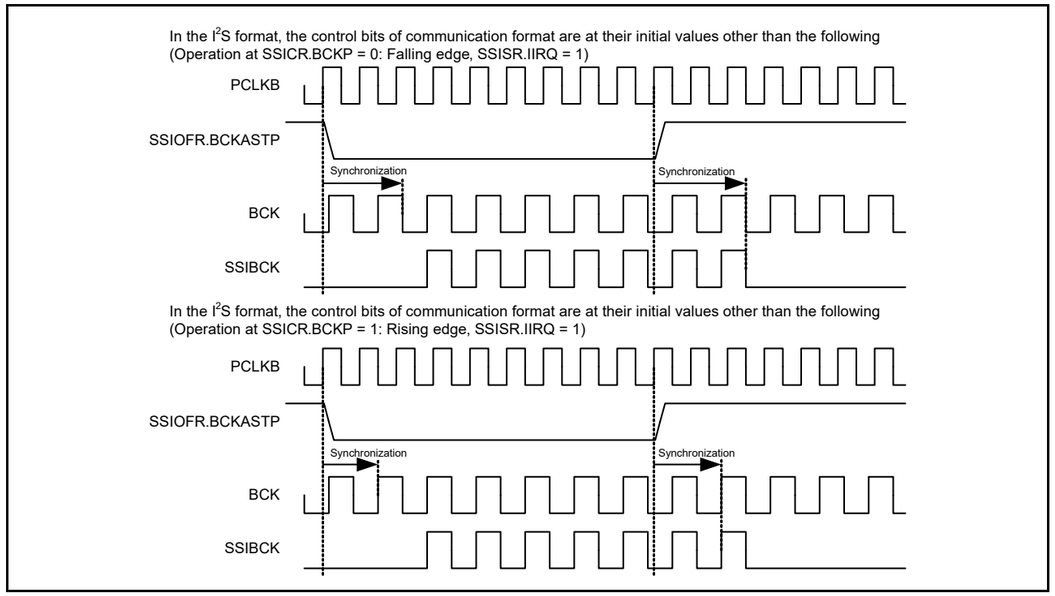


Figure 41.45 Example of stopping SSIBCK with SSIOFR.BCKASTP

Note: To stop the output to the SSIBCK pin with SSIOFR.BCKASTP in master-mode communication (SSICR.MST = 1) and while SSIE is in the idle state, note the following: The output stops when the value of the SSIOFR.BCKASTP bit is changed from 0 to 1. So, make sure that the other-party device is not affected.

41.7.2 Communication States

In this state, SSIE is during communication. Figure 41.46 shows transitions of communication states and Table 41.15 lists the conditions for transition. If the transition condition is not satisfied, the state does not transit.

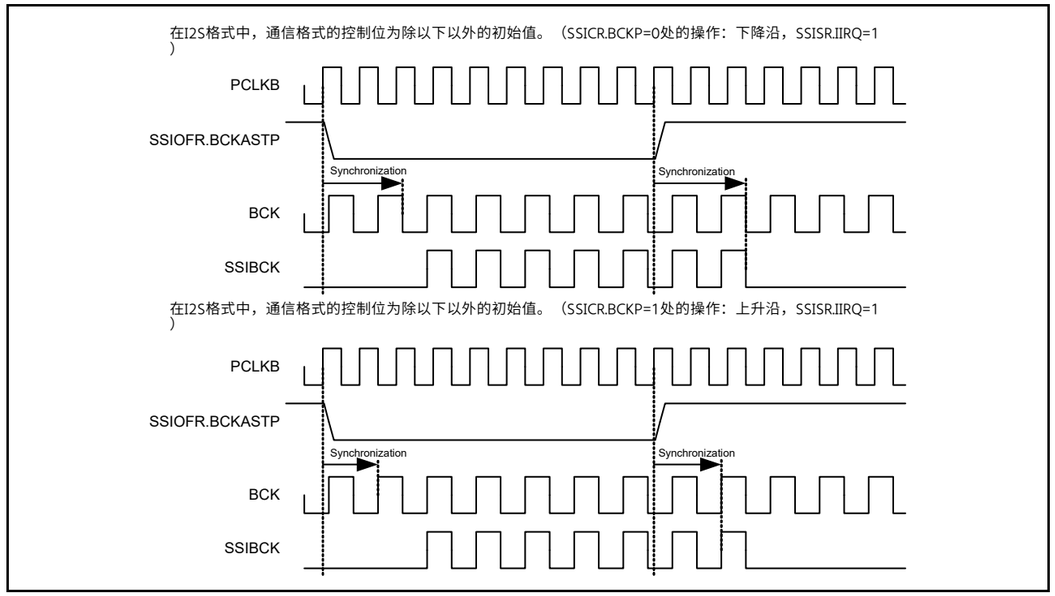


Figure 41.45 使用SSIOFR.BCKASTP停止SSIBCK的示例

Note: 要在主模式通信(SSICR.MST=1)和SSIE处于空闲状态时使用SSIOFR.BCKASTP停止向SSIBCK引脚的输出，请注意以下事项：当SSIOFR.BCKASTP位的值为从0变为1。因此，请确保对方设备不受影响。

41.7.2 通讯状态

在此状态下，SSIE处于通信过程中。图41.46显示了通信状态的转换，表41.15列出了转换的条件。如果不满足转移条件，则状态不转移。

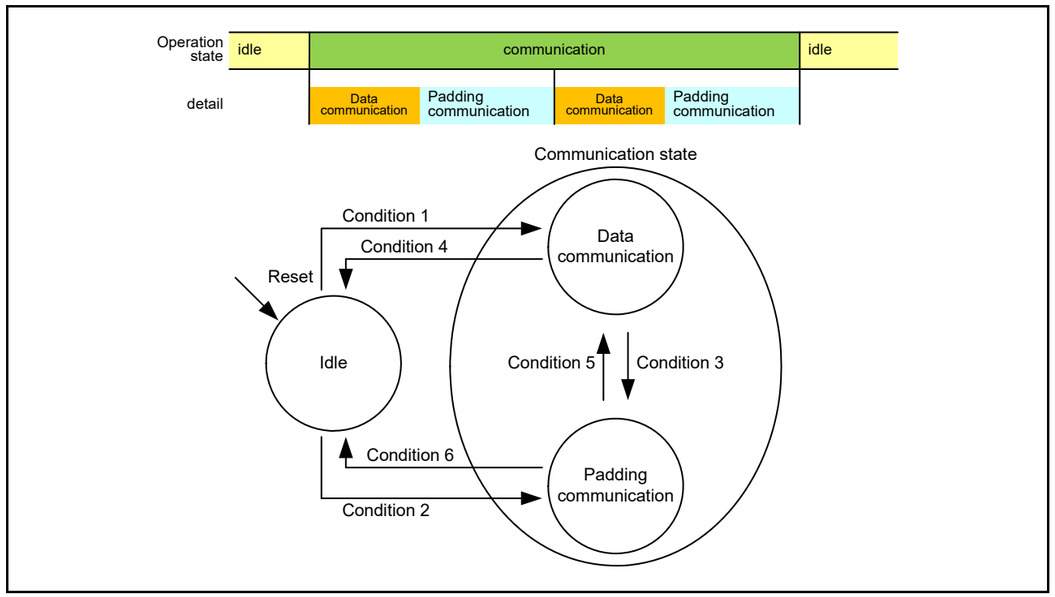


Figure 41.46 Communication state transition

Table 41.15 Condition for communication state transition

Condition Number	Condition for Transition
1	Writing SSICR.TEN = 1 or SSICR.REN = 1 while SSICR.SDTA = 0 or in the setting without padding bits.
2	Writing SSICR.TEN = 1 or SSICR.REN = 1 while SSICR.SDTA = 1 and in the setting with padding bits.
3	The following three conditions are all met: • SSICR.TEN = 1 or SSICR.REN = 1 • In the setting with padding bits • The last bit of the data words has been transferred.
4	Both the following two conditions are met: • SSICR.SDTA = 1 or without padding bits • While SSICR.TEN = 0 and SSICR.REN = 0, the last bit of the data words in a frame has been transferred.
5	Transfer of the last padding bit is completed while SSICR.TEN = 1 or SSICR.REN = 1
6	Both the following two conditions are met: • SSICR.SDTA = 0 and with padding bits • While SSICR.TEN = 0 and SSICR.REN = 0, the last padding bit has been transferred.

See Table 41.11 for the setting with/without padding bits.

41.7.2.1 Data communication state

In this state, SSIE is during communication. Data of the data word length set with the SSICR.DWL[2:0] bits is transmitted, received, or transmitted and received.

- State Transition in the Setting without Padding Bits

During communication (SSISR.IIRQ = 0), SSIE is during data communication for all the time. By disabling transmission and reception (SSICR.TEN = 0, SSICR.REN = 0), SSIE transits to the idle state. For details, see Figure 41.47 and Figure 41.48.

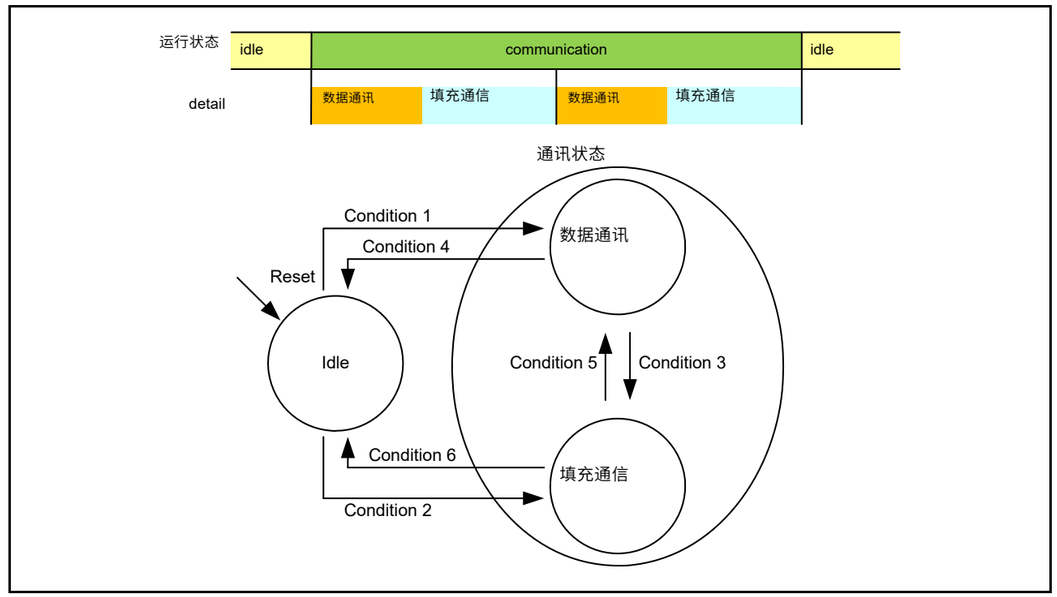


Figure 41.46 通信状态转换

Table 41.15 通信状态转移的条件

Condition Number	过渡条件
1	在SSICR.SDTA=0或在没有填充位的设置中写入SSICR.TEN=1或SSICR.REN=1。
2	写入SSICR.TEN=1或SSICR.REN=1而SSICR.SDTA=1并在设置中使用填充位。
3	以下三个条件都满足： SSICR.TEN=1或SSICR.REN=1 在带有填充位的设置中 数据字的最后一位已传输。
4	满足以下两个条件： SSICR.SDTA=1或没有填充位 当SSICR.TEN=0和SSICR.REN=0时，帧中数据字的最后一位已传输。
5	当SSICR.TEN=1或SSICR.REN=1时，最后一个填充位的传输完成
6	满足以下两个条件： SSICR.SDTA=0和填充位 当SSICR.TEN=0和SSICR.REN=0时，已传输最后一个填充位。

有关不带填充位的设置，请参见表41.11。

41.7.2.1 数据通讯状态

在此状态下，SSIE处于通信过程中。使用SSICR.DWL[2:0]位设置的数据字长的数据被发送、接收或发送和接收。

- 没有填充位的设置中的状态转换

在通信期间（SSISR.IIRQ=0），SSIE一直处于数据通信期间。通过禁用发送和接收（SSICR.TEN=0，SSICR.REN=0），SSIE转换到空闲状态。详见图41.47和图41.48。

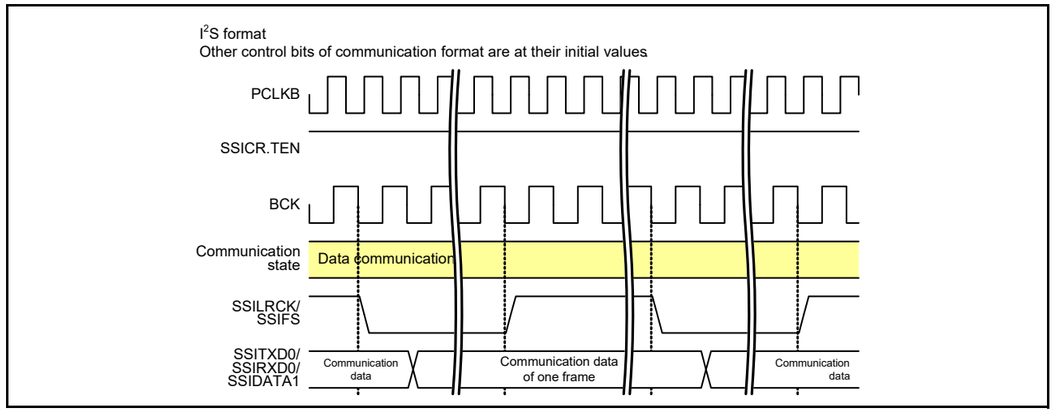


Figure 41.47 Continuation of the data communication

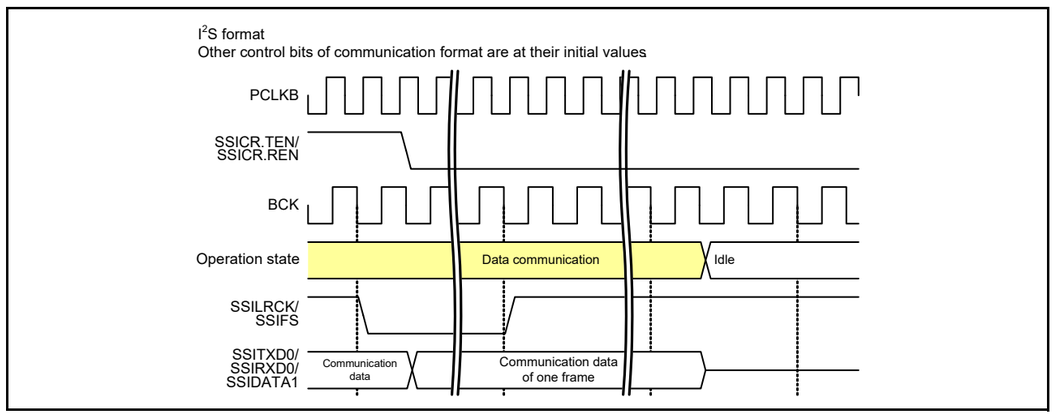


Figure 41.48 Halt from the data communication (without padding bits)

- State Transition in the Setting with Padding Bits

When SSIE ends transfer of the last bit of a data word during communication (SSISR.IIRQ = 0), SSIE transitions from the data communication state to the padding communication state in Figure 41.49. Except in the status with SSICR.SDTA = 1 and transmission and reception disabled (SSICR.TEN = 0 and SSICR.REN = 0), SSIE transitions from the data communication state to the idle state when it stops communication in Figure 41.51.

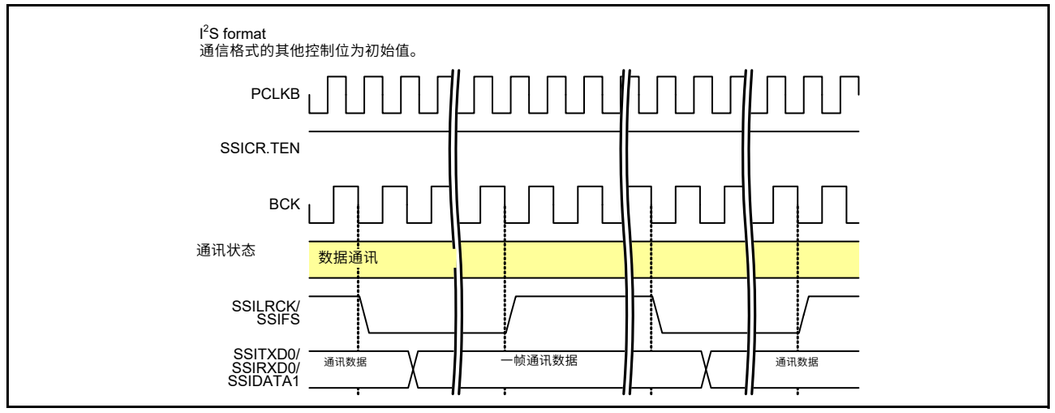


Figure 41.47 继续数据通信

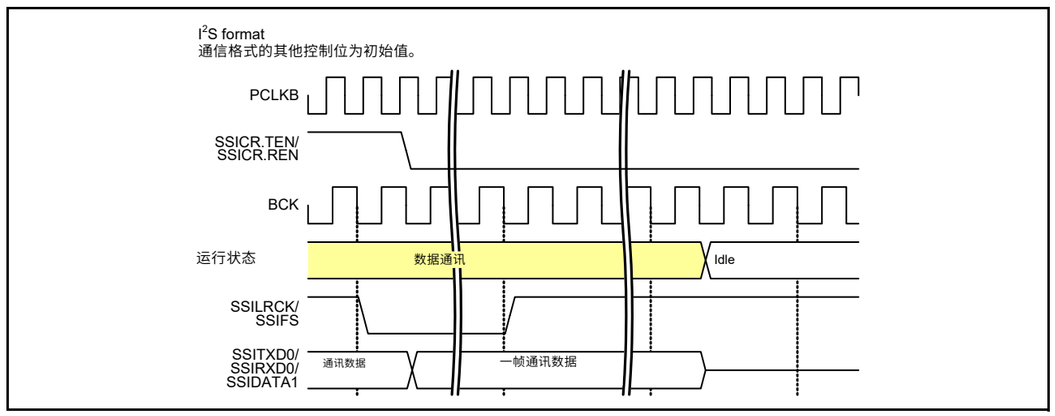


Figure 41.48 停止数据通信（无填充位）

- 具有填充位的设置中的状态转换

当SSIE在通信期间结束数据字的最后一位传输时（SSISR.IIRQ=0），SSIE从数据通信状态转换到图41.49中的填充通信状态。除了在SSICR.SDTA=1和发送和接收禁用的状态下（SSICR.TEN=0和SSICR.REN=0），SSIE在图41.51中停止通信时会从数据通信状态转换到空闲状态。

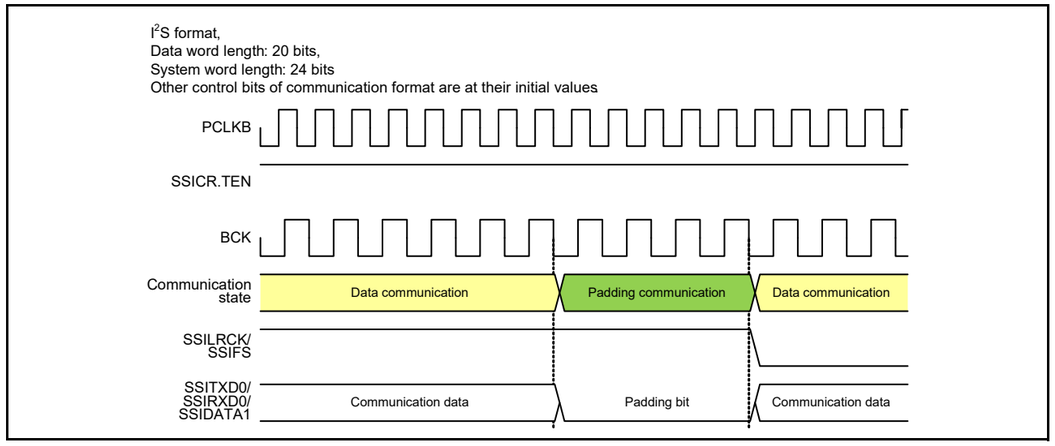


Figure 41.49 Transition from data communication to padding communication

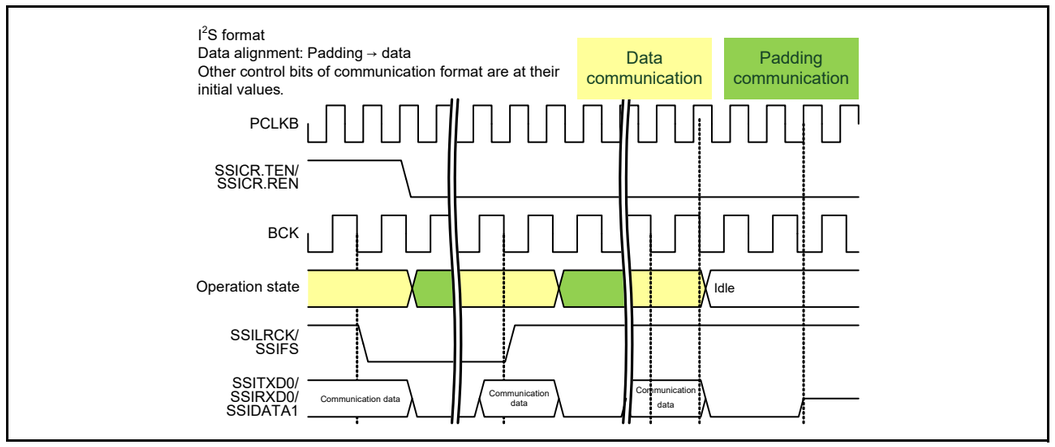


Figure 41.50 Halt from data communication (with padding bits)

41.7.2.2 Padding communication

In this state, SSIE is during communication. The padding bits set with the SSICR.SWL[2:0] bits and SSICR.DWL[2:0] bits are transmitted, received, or transmitted and received.

- State Transition in the Setting with Padding Bits

When SSIE ends transfer of the last padding bit during communication (SSISR.IIRQ = 0), SSIE transitions to the data communication state in Figure 41.49. If SSIE is in the status with SSICR.SDTA = 0 and transmission and reception disabled (SSICR.TEN = 0 and SSICR.REN = 0), SSIE transitions from the padding communication state to the idle state when it stops communication in Figure 41.51.

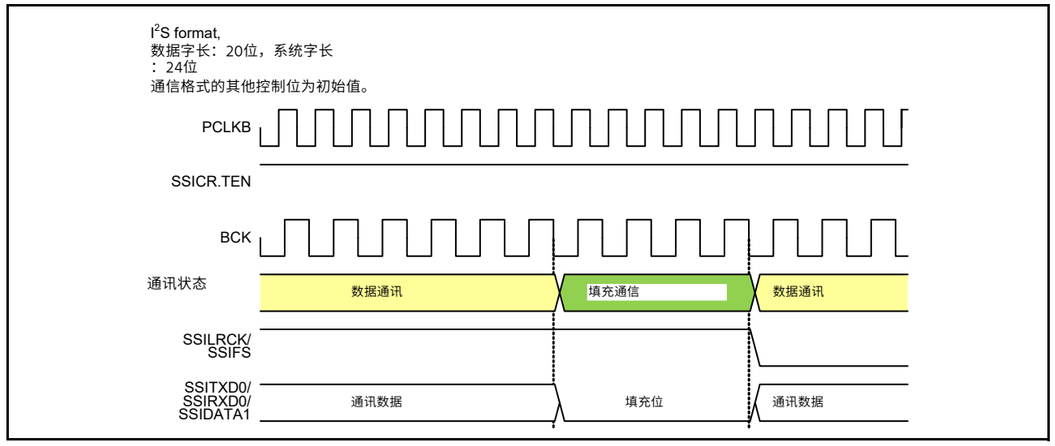


Figure 41.49 从数据通信过渡到填充通信

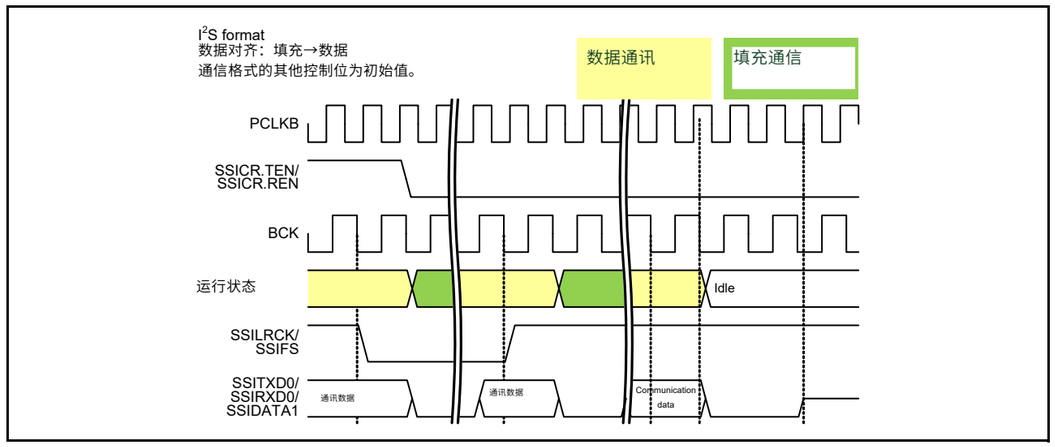


Figure 41.50 停止数据通信（使用填充位）

41.7.2.2 填充通信

在此状态下，SSIE处于通信过程中。使用SSICR.SWL[2:0]位和SSICR.DWL[2:0]位设置的填充位被发送、接收或发送和接收。

- 具有填充位的设置中的状态转换

当SSIE在通信期间结束最后一个填充位的传输（SSISR.IIRQ=0）时，SSIE转换到图41.49中的数据通信状态。如果SSIE处于SSICR.SDTA=0且发送和接收禁用的状态（SSICR.TEN=0和SSICR.REN=0），则SSIE在图41.51中停止通信时从填充通信状态转换为空闲状态。

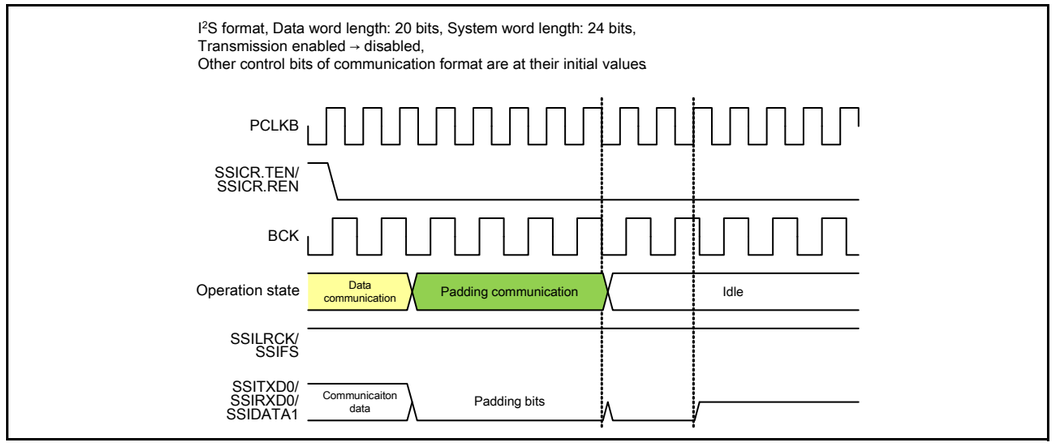


Figure 41.51 Halt from the padding communication

41.8 Communication Operation

Figure 41.52 shows the communication flow of SSIE.

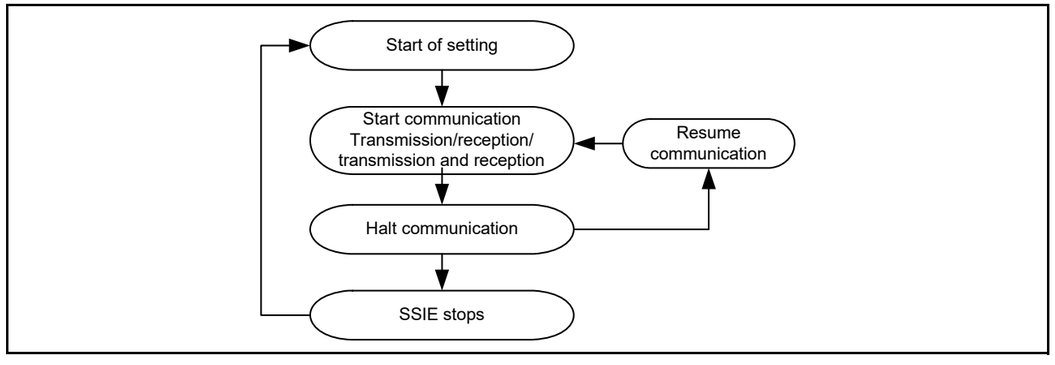


Figure 41.52 SSIE communication operation

The procedure of each operation is described from reference 41.8.1 to reference 41.8.7.

41.8.1 Start Communication

This section describes how to start communication of SSIE. Figure 41.53 shows the procedure to start communication. Be sure to follow the procedure. See reference 41.8.2 for transmission operation and reference 41.8.3 for reception operation.

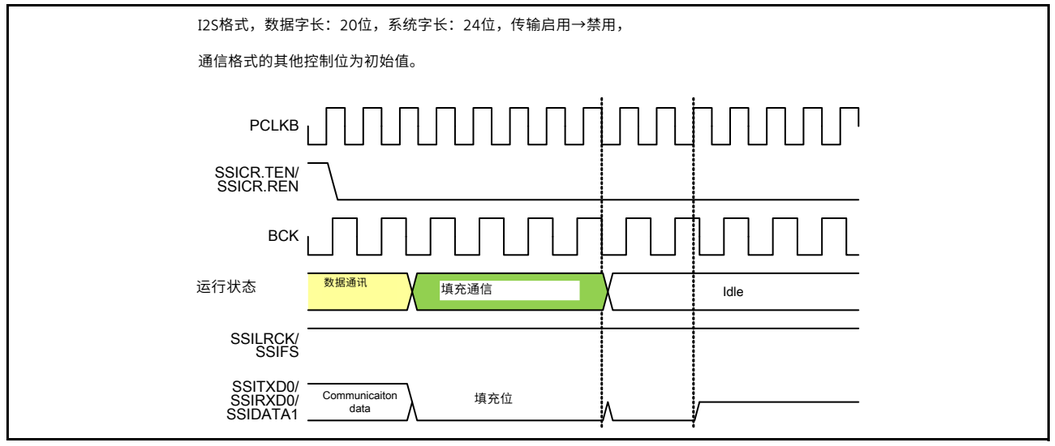


Figure 41.51 从填充通信中停止

41.8 通讯操作

图41.52显示了SSIE的通信流程。

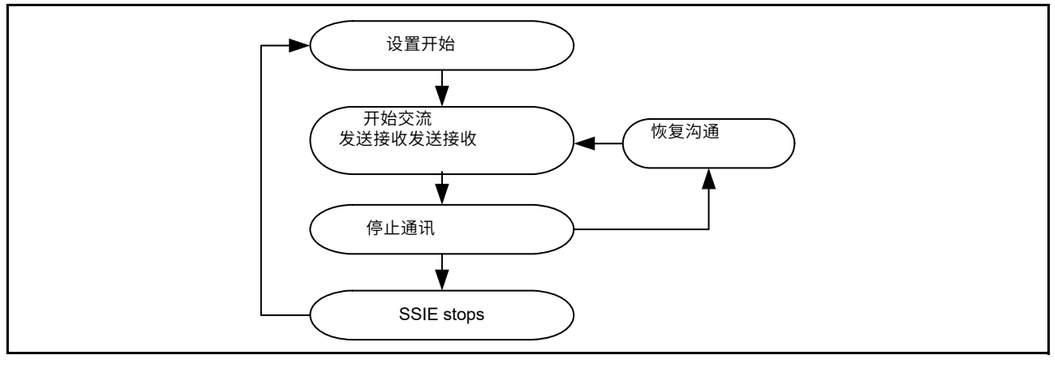
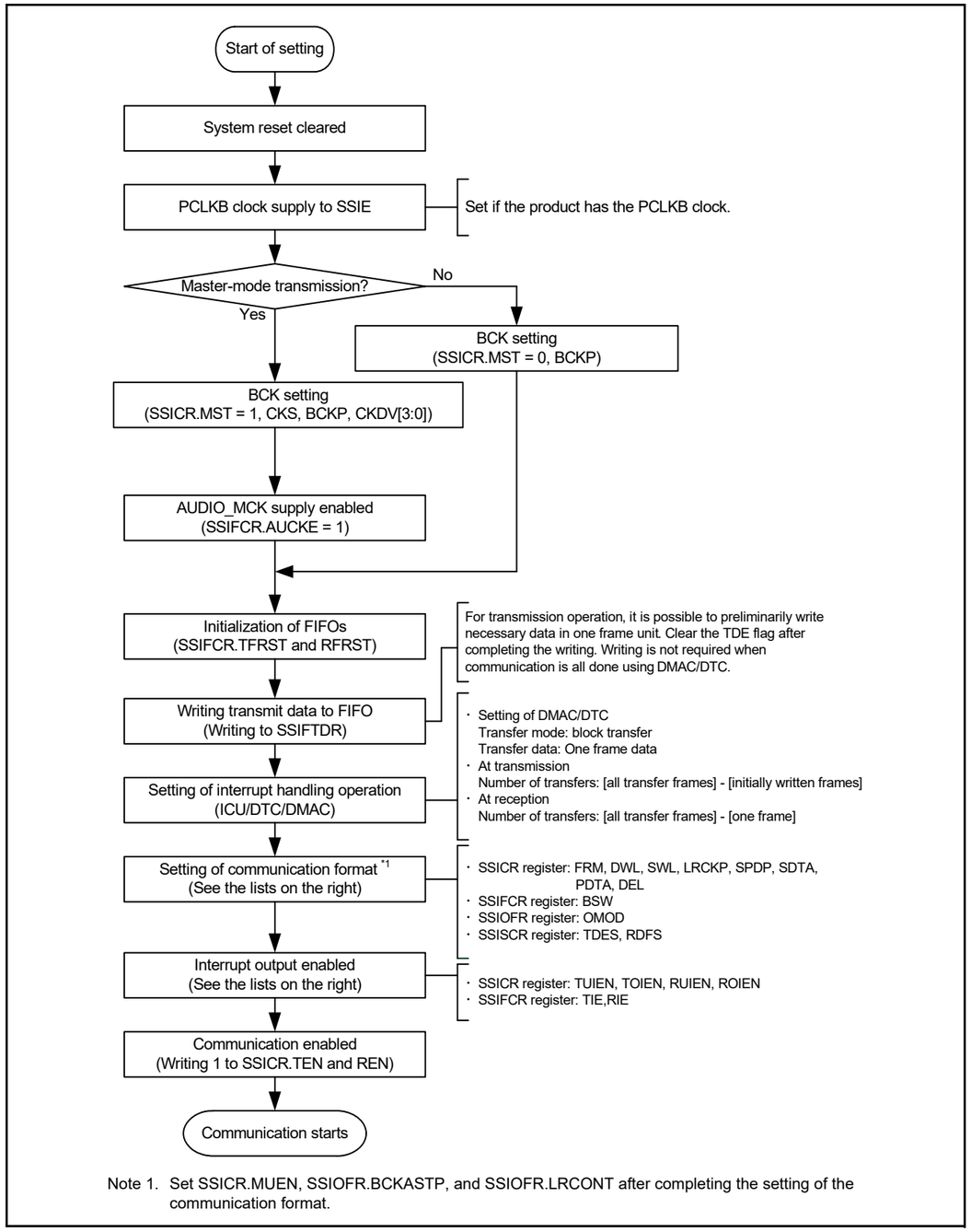


Figure 41.52 SSIE通信操作

从参考41.8.1到参考41.8.7描述了每个操作的过程。

41.8.1 开始沟通

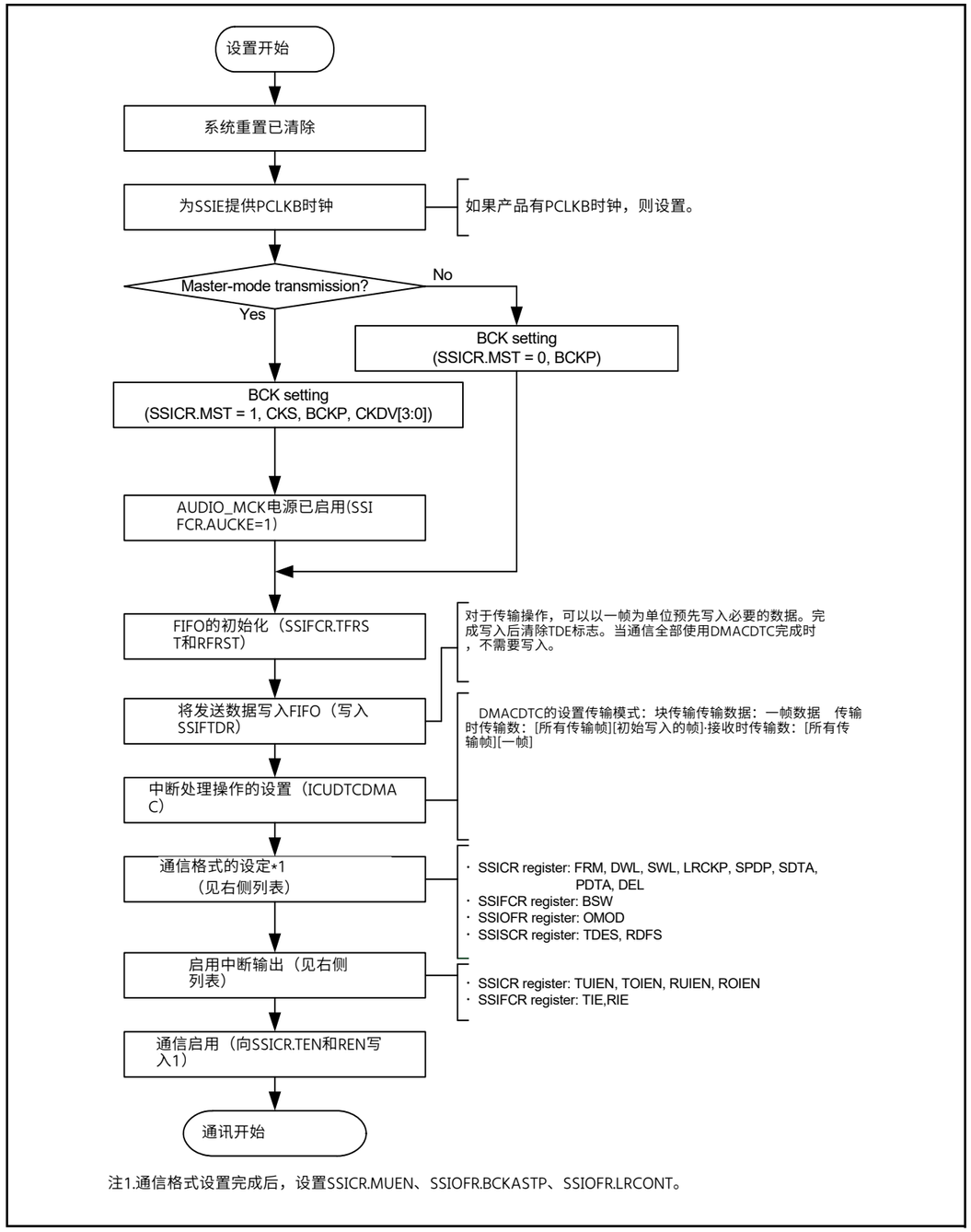
本节介绍如何启动SSIE通信。图41.53显示了开始通信的过程。
请务必遵守程序。发送操作参见参考41.8.2，接收操作参见参考41.8.3。



Note 1. Set SSICR.MUEN, SSIOFR.BCKASTP, and SSIOFR.LRCONT after completing the setting of the communication format.

Figure 41.53 Procedure to start communication (CPU operation procedure)

SSIE can perform continuous communication based on interrupts by the DTC/DMAC. For transmission, write 1 to SSIFCR.TIE, SSICR.TUIEN, and SSICR.TOIEN. For reception, write 1 to SSIFCR.RIE, SSICR.RUIEN, and SSICR.ROIEN.



注1.通信格式设置完成后，设置SSICR.MUEN、SSIOFR.BCKASTP、SSIOFR.LRCONT。

Figure 41.53 开始通信的步骤（CPU操作步骤）

SSIE可以根据DTCDMAC的中断执行连续通信。对于传输，写入1到SSIFCR.TIE、SSICR.TUIEN和SSICR.TOIEN。对于接收，将1写入SSIFCR.RIE、SSICR.RUIEN和SSICR.ROIEN.

41.8.2 Transmission

The transmission procedure in Figure 41.54 must be followed throughout a transmission operation.

After transmission is enabled (SSICR.TEN = 1 and SSICR.REN = 0), SSIE starts transmission when a start trigger is generated by SSILRCK/SSIFS with the serial data for at least a frame contained in the transmit FIFO data register (SSIFTDR). SSIE outputs a transmit data empty interrupt to the DTC/DMAC according to the TDE setting condition (SSISCR.TDES) and the status of transmit data empty interrupt enable (SSIFCR.TIE) bit specified in the communication start procedure. This interrupt requests writing to the transmit FIFO data register (SSIFTDR). In the communication start procedure, specify writing to the transmit FIFO data register (SSIFTDR) as the DTC/DMAC operation in response to the transmit data empty interrupt. With this setting, SSIE can continuously transmit data not through the CPU. The transmit data empty interrupt is generated when the free space size of transmit FIFO data register reaches the value set in SSISCR.TDES. The number of times of writing must be specified in accordance with the free space size of the transmit FIFO data register indicated by the transmit data empty interrupt. If an error occurs, perform the error-handling procedure as instructed in the communication stop procedure.

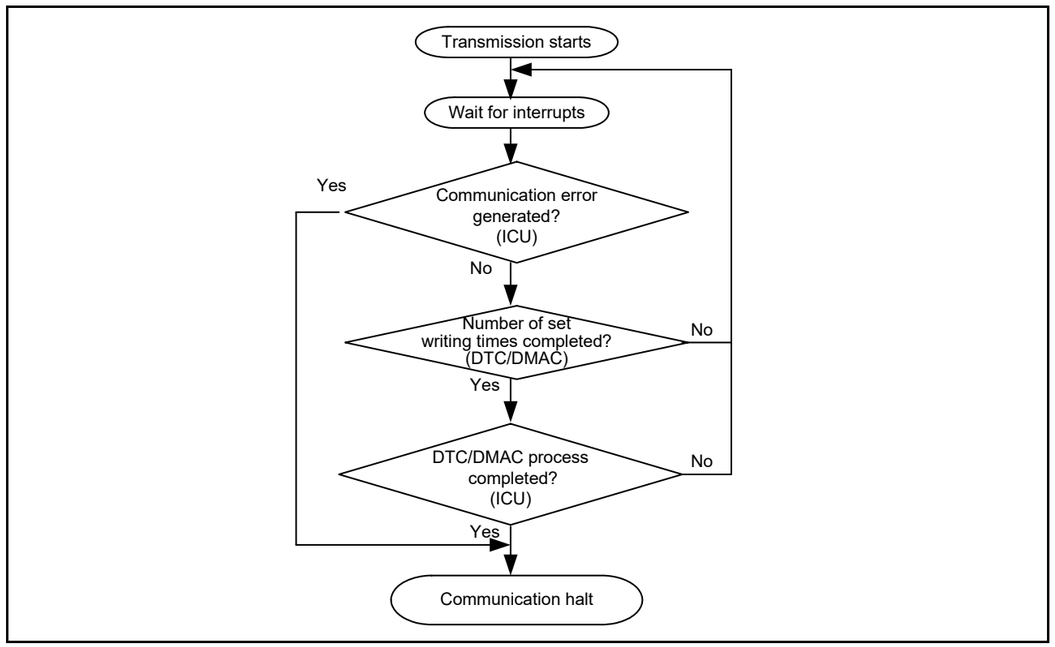


Figure 41.54 Transmission procedure

Note: The communication flow defined in SSIE uses the DTC/DMAC. If you do not use the DTC/DMAC, perform polling of the value 1 of SSIFSR.TDE to write data to SSIFTDR. The number of times of writing data to SSIFTDR by detecting the value 1 of SSIFSR.TDE must be in accordance with the free space size of the transmit FIFO data register specified by SSISCR.TDES. After as much transmit data as the free space size is written to SSIFTDR, the SSIFSR.TDE flag must be cleared. Continuous transmission is enabled by repeating data writing. If the SSIFSR.TDE flag is not cleared, the flag is not cleared automatically.

41.8.3 Reception

The reception procedure in Figure 41.55 must be followed throughout a reception operation.

After reception is enabled (SSICR.TEN = 0 and SSICR.REN = 1), SSIE starts reception when a start trigger is generated by SSILRCK/SSIFS. SSIE outputs a receive data full interrupt to the DTC/DMAC according to the RDF setting condition (SSISCR.RDFS) and the status of receive data full interrupt enable (SSIFCR.RIE) bit specified in the communication start procedure. This interrupt requests data reading from the receive FIFO data register (SSIFRDR). In the communication start procedure, specify reading from the receive FIFO data register (SSIFRDR) as the DTC/DMAC

41.8.2 Transmission

在整个传输操作中必须遵循图41.54中的传输过程。

使能传输后（SSICR.TEN=1和SSICR.REN=0），当SSILRCKSSIFS使用包含在传输FIFO数据寄存器(SSIFTDR)中的至少一帧的串行数据生成启动触发时，SSIE开始传输。SSIE根据通信启动过程中指定的TDE设置条件(SSISCR.TDES)和发送数据空中断使能(SSIFCR.TIE)位的状态，向DTCDMAC输出一个发送数据空中断。该中断请求写入发送FIFO数据寄存器(SSIFTDR)。在通信开始过程中，将写入发送FIFO数据寄存器(SSIFTDR)指定为DTCDMAC操作以响应发送数据空中断。使用此设置，SSIE可以不通过CPU连续传输数据。当发送FIFO数据寄存器的可用空间大小达到SISSCR.TDES中设置的值时，将产生发送数据空中断。必须根据发送的空闲空间大小指定写入次数

FIFO数据寄存器由发送数据空中断指示。如果发生错误，请按照通信停止程序中的说明执行错误处理程序。

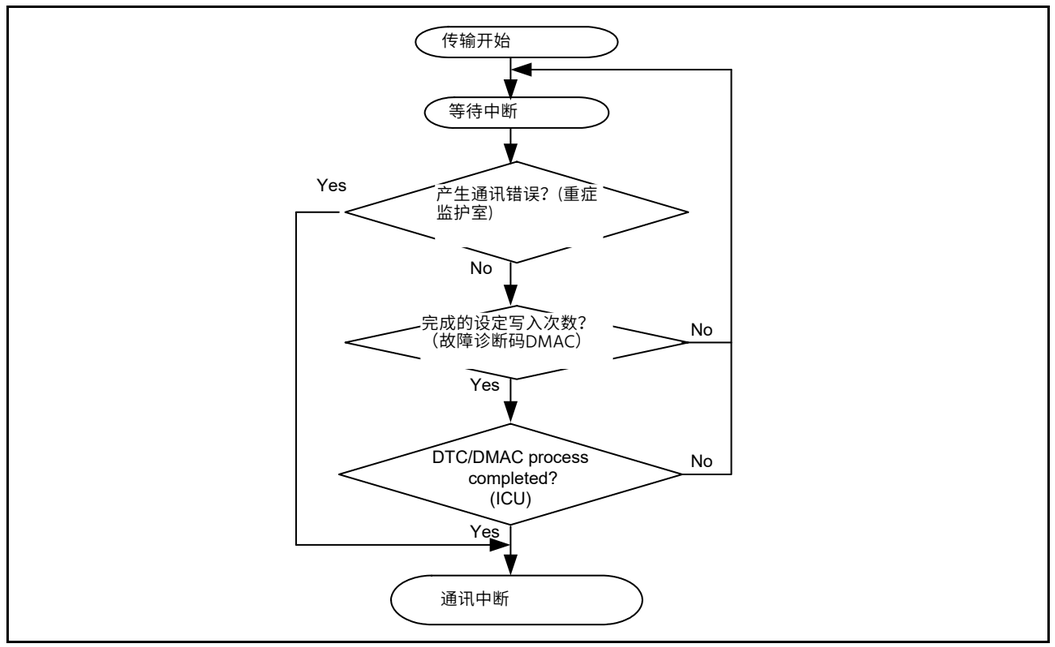


Figure 41.54 传输程序

Note: SSIE中定义的通信流使用DTCDMAC。如果不使用DTCDMAC，则轮询SSIFSR.TDE的值1以将数据写入SSIFTDR。通过检测SSIFSR.TDE的值为1向SSIFTDR写入数据的次数必须与SSIFSR.TDES指定的发送FIFO数据寄存器的空闲空间大小一致。在将与可用空间大小一样多的传输数据写入SSIFTDR后，必须清除SSIFSR.TDE标志。通过重复数据写入启用连续传输。如果未清除SSIFSR.TDE标志，则不会自动清除该标志。

41.8.3 Reception

在整个接收操作中必须遵循图41.55中的接收程序。

使能接收后（SSICR.TEN=0和SSICR.REN=1），当SSILRCKSSIFS产生一个开始触发信号时，SSIE开始接收。SSIE根据RDF设置条件(SSISCR.RDFS)和通信开始过程中指定的接收数据满中断使能(SSIFCR.RIE)位的状态向DTCDMAC输出一个接收数据满中断。该中断请求从接收FIFO数据寄存器(SSIFRDR)读取数据。在通信开始过程中，指定从接收FIFO数据寄存器(SSIFRDR)读取作为DTCDMAC

operation in response to the receive data full interrupt. With this setting, SSIE can continuously read data not through the CPU. The receive data full interrupt is generated when data as much as the capacity of receive FIFO data register has been stored. The number of times of reading must be specified in accordance with the data size of the receive FIFO data register indicated by the receive data full interrupt. If an error occurs, perform the error-handling procedure as instructed in the communication stop procedure.

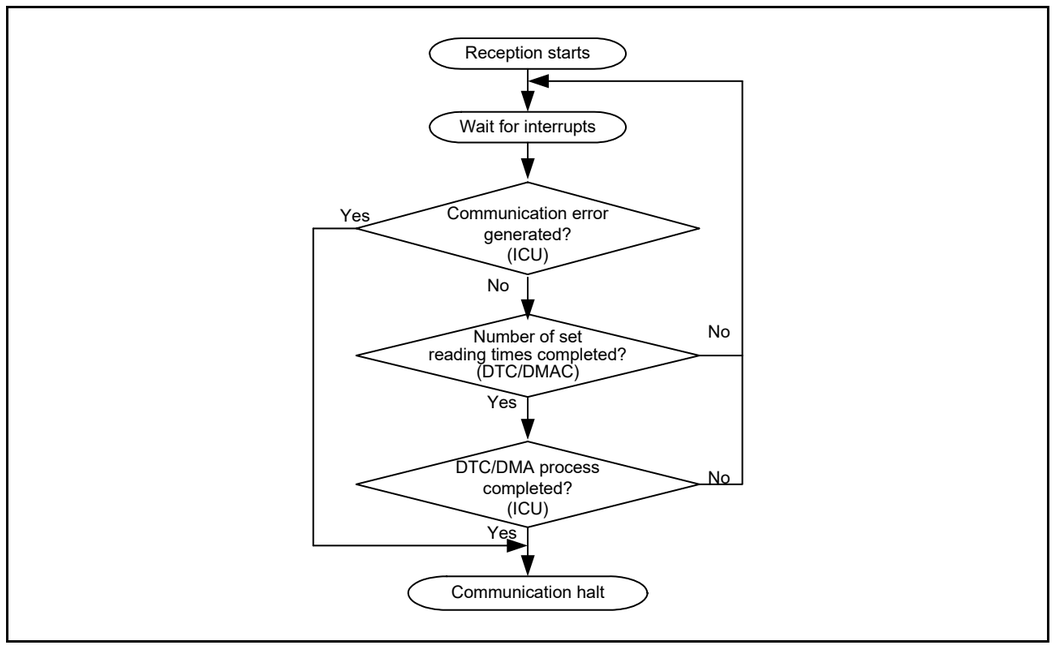


Figure 41.55 Reception procedure

Note: The communication flow defined in SSIE uses the DTC/DMAC. If you do not use the DTC/DMAC, perform polling of the value 1 of SSIFSR.RDF to read data from SSIFRDR. The number of times of reading data from SSIFRDR by detecting the value 1 of SSIFSR.RDF must be in accordance with the receive data storage capacity of the receive FIFO data register specified by SSISCR.RDFS. After received data is read from SSIFRDR, the SSIFSR.RDF flag must be cleared. Continuous reception is enabled by repeating data reading. If the SSIFSR.RDF flag is not cleared, the flag is not cleared automatically.

41.8.4 Transmission and Reception

After transmission and reception are enabled (SSICR.TEN = 1 and SSICR.REN = 1), SSIE starts transmission and reception when a start trigger is generated by SSILRCK/SSIFS with the serial data for at least a frame contained in the transmit FIFO data register (SSIFTDR). SSIE can continuously transmit and receive data by performing the procedures described in reference 41.8.2 and reference 41.8.3, respectively. For how to stop transmission and reception, see reference 41.8.5.

41.8.5 Halt Communication

This section describes how to halt communication of SSIE. Figure 41.56 shows the procedure to halt communication. Be sure to follow the procedure.

操作以响应接收数据完全中断。通过此设置，SSIE可以不通过CPU连续读取数据。当数据达到接收FIFO数据寄存器的容量时，产生接收数据满中断。读取次数必须根据接收数据满中断指示的接收FIFO数据寄存器的数据大小来指定。如果发生错误，请按照通信停止程序中的说明执行错误处理程序。

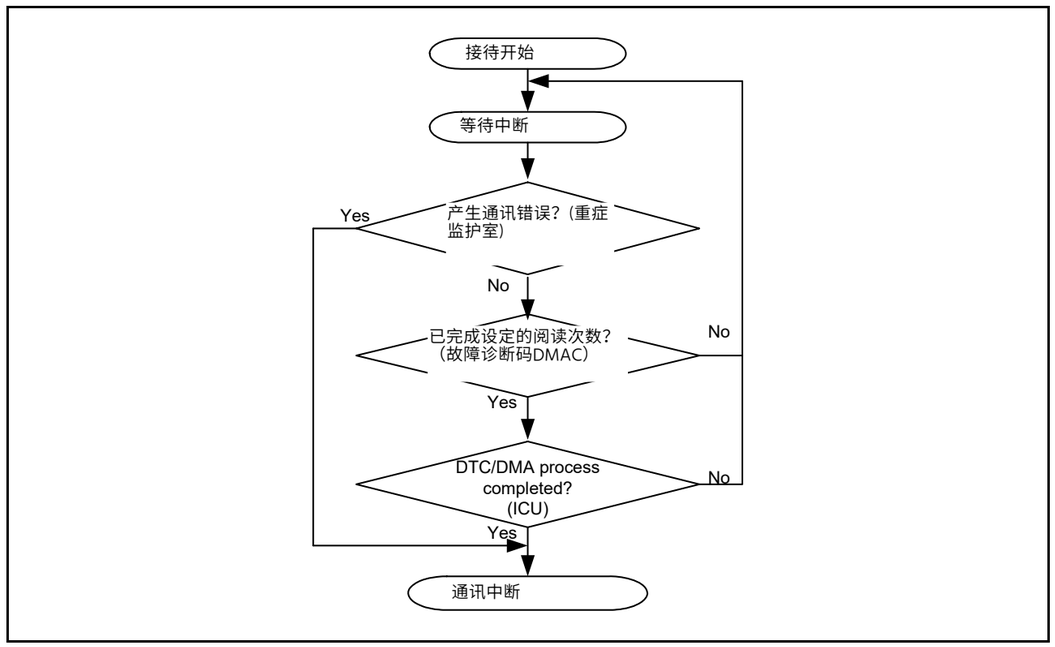


Figure 41.55 接待程序

Note: SSIE中定义的通信流使用DTCDMAC。如果不使用DTCDMAC，则轮询SSIFSR.RDF的值1以从SSIFRDR读取数据。通过检测SSIFSR.RDF的值为1从SSIFRDR读取数据的次数必须与SSISCR.RDFS指定的接收FIFO数据寄存器的接收数据存储容量一致。从SSIFRDR读取接收到的数据后，必须清除SSIFSR.RDF标志。通过重复数据读取启用连续接收。如果

SSIFSR.RDF标志不清除，该标志不会自动清除。

41.8.4 传输和接收

启用发送和接收后（SSICR.TEN=1和SSICR.REN=1），当SSILRCKSSIFS使用发送FIFO数据寄存器中包含的至少一帧的串行数据产生开始触发时，SSIE开始发送和接收(SSIFTDR)。SSIE可以通过分别执行参考41.8.2和参考41.8.3中描述的过程来连续发送和接收数据。关于如何停止发送和接收，请参见参考41.8.5。

41.8.5 停止通讯

本节介绍如何停止SSIE的通信。图41.56显示了停止通信的过程。请务必遵守程序。

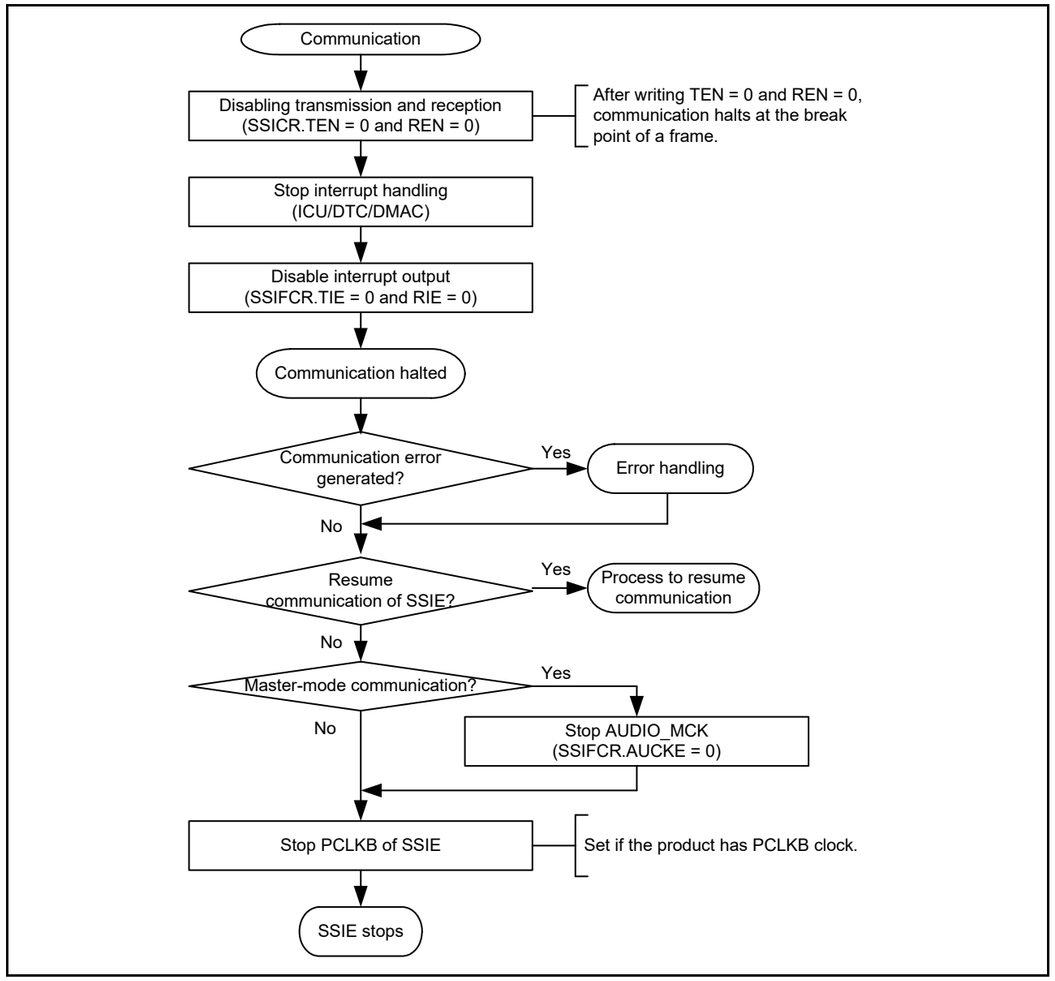


Figure 41.56 Procedure to halt communication (CPU operation procedure)

To halt the communication of SSIE, supply of the following clocks are required until the SSISR.IIRQ bit indicates an idle state.

- Input clock from the SSIBCK pin when SSICR.MST = 0
- AUDIO_MCK when SSICR.MST = 1

  To resume communication of SSIE in the previous setting, see reference 41.8.7.

Note: When communication of SSIE is halted according to the procedure to halt communication in Figure 41.56, resume communication according to the procedure to resume communication in Figure 41.58.

41.8.6 Error Handling

SSIE has the following four errors.

- Transmit underflow error
- Transmit overflow error
- Receive underflow error

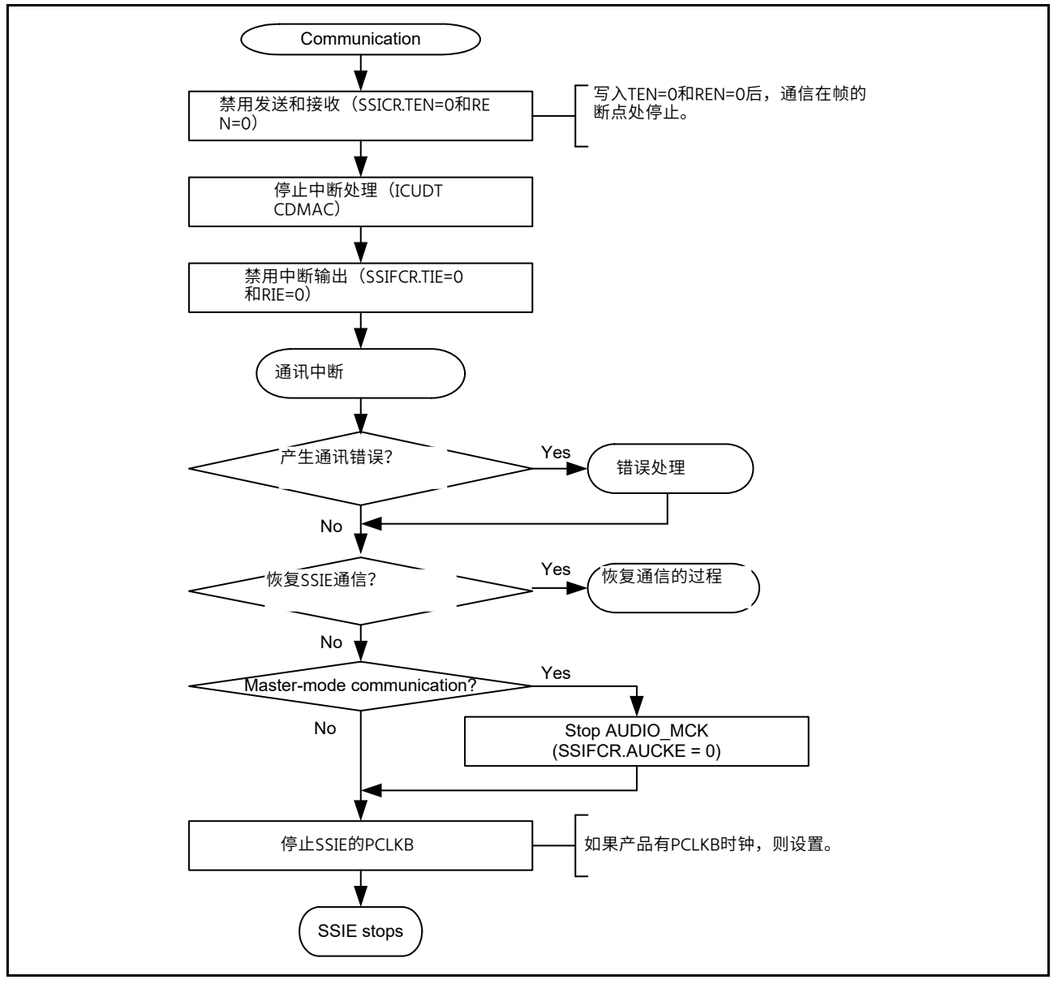


Figure 41.56 停止通信的步骤（CPU操作步骤）

要停止SSIE的通信，需要提供以下时钟，直到SSISR.IIRQ位指示空闲状态。

- 当SSICR.MST=0时，来自SSIBCK引脚的输入时钟
- AUDIO_MCK when SSICR.MST = 1

  要在之前的设置中恢复SSIE通信，请参阅参考41.8.7。

Note: 当SSIE的通信按照图41.56中的停止通信程序停止时，按照图41.58中的恢复通信程序恢复通信。

41.8.6 错误处理

SSIE有以下四个错误。

- 发送下溢错误
- 传输溢出错误
- 接收下溢错误

- Receive overflow error.

When an underflow error or overflow error is generated, SSIE need to be restarted. Follow the procedure to halt communication in Figure 41.56 and error-handling procedure in Figure 41.57.

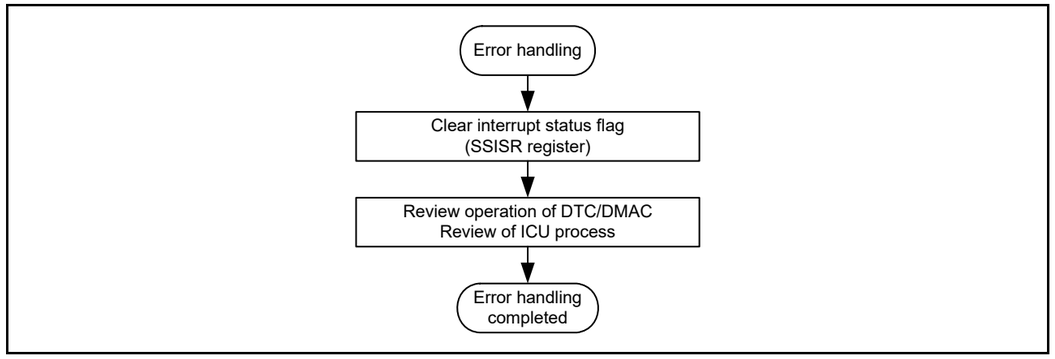


Figure 41.57 Error-handling procedure

Four error operations are described as follows. When the interrupt output enable bit of the SSICR register is enabled and error flags are set, an error interrupt is generated. See descriptions of flags in reference 41.4.2 for the setting conditions of error flags.

(1) Transmit Underflow Error

If a transmit underflow error occurs, review the number of times of writing data to the transmit FIFO data register (SSIFTDR) in response to a transmit data empty interrupt. After a transmit underflow error occurs, SSIE outputs 0s as data. To normally output the serial data written to the transmit FIFO data register (SSIFTDR) to the SSITXD0/SSIDATA1 pin, follow the procedure to halt communication in Figure 41.56 and error-handling procedure in Figure 41.57. After this error occurs, serial data is consumed as usual. If you resume communication, write the serial data from the beginning.

(2) Transmit Overflow Error

If a transmit overflow error occurs, review the number of times of writing data to the transmit FIFO data register (SSIFTDR) in response to transmit data empty interrupts. The serial data written to the transmit FIFO data register (SSIFTDR) that caused the transmit overflow error becomes invalid. This error can occur regardless of whether a transmission operation is being done. To recover from the error, follow the procedure to halt communication in Figure 41.56 and error-handling procedure in Figure 41.57. When you resume communication, deal with the invalid serial data appropriately.

(3) Receive Underflow Error

If a receive underflow error occurs, review the number of times of reading data from the receive FIFO data register (SSIFRDR) in response to receive data full interrupts. The values read from the receive FIFO data register (SSIFRDR) that caused the receive underflow error are undefined. This error can occur regardless of whether a reception operation is being done. To recover from the error, follow the procedure to halt communication in Figure 41.56 and error-handling procedure in Figure 41.57.

(4) Receive Overflow Error

If a receive overflow error occurs, review the number of times of reading data from the receive FIFO data register (SSIFRDR) in response to receive data full interrupts. The receive data that caused the receive overflow error cannot be stored in the receive FIFO data register (SSIFRDR). To recover from the error, follow the procedure to halt communication in Figure 41.56 and error-handling procedure in Figure 41.57.

41.8.7 Resume Communication

When you resume the communication using SSIE, follow the communication resume procedure in Figure 41.58. The communication resume procedure is designed on the assumption that you resume the communication stopped by the

- 接收溢出错误。

当产生下溢错误或上溢错误时，需要重启SSIE。按照图41.56中的程序停止通信和图41.57中的错误处理程序。

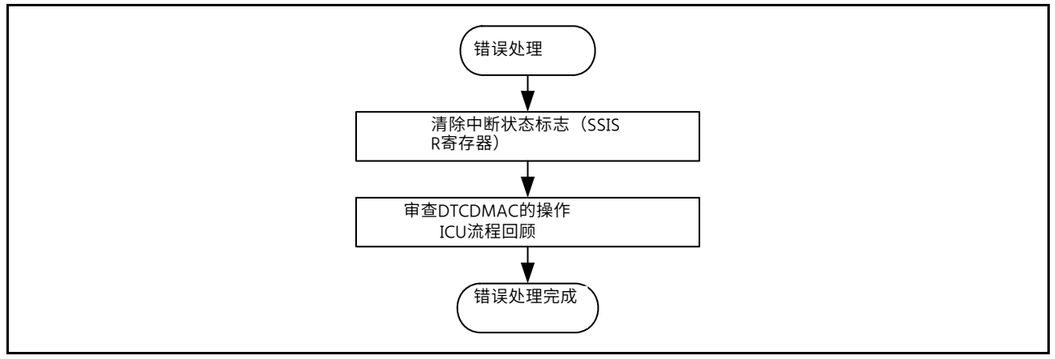


Figure 41.57 Error-handling procedure

四种错误操作描述如下。当SSICR寄存器的中断输出使能位使能且错误标志置位时，将产生错误中断。错误标志的设置条件见参考41.4.2中标志的描述。

(1) 发送下溢错误

如果发生发送下溢错误，请查看响应发送数据空中断而将数据写入发送FIFO数据寄存器(SSIFTDR)的次数。发生发送下溢错误后，SSIE输出0作为数据。要将写入发送FIFO数据寄存器(SSIFTDR)的串行数据正常输出到SSITXD0 SSIDATA1引脚，请按照图41.56中的程序停止通信和图41.57中的错误处理程序进行操作。发生此错误后，串行数据将照常使用。如果您恢复通信，请从头开始写入串行数据。

(2) 传输溢出错误

如果发生发送溢出错误，请查看响应发送数据空中断而将数据写入发送FIFO数据寄存器(SSIFTDR)的次数。写入导致发送溢出错误的发送FIFO数据寄存器(SSIFTDR)的串行数据变为无效。无论是否正在执行传输操作，都可能发生此错误。要从错误中恢复，请按照图41.56中的程序停止通信和图41.57中的错误处理程序。当您恢复通信时，请适当处理无效的串行数据。

(3) 接收下溢错误

如果发生接收下溢错误，请检查从接收FIFO数据寄存器(SSIFRDR)读取数据以响应接收数据满中断的次数。从导致接收下溢错误的接收FIFO数据寄存器(SSIFRDR)读取的值未定义。无论是否正在执行接收操作，都可能发生此错误。要从错误中恢复，请按照图41.56中的程序停止通信和图41.57中的错误处理程序。

(4) 接收溢出错误

如果发生接收溢出错误，请检查从接收FIFO数据寄存器(SSIFRDR)读取数据以响应接收数据满中断的次数。导致接收溢出错误的接收数据不能存储在接收FIFO数据寄存器(SSIFRDR)中。要从错误中恢复，请按照图41.56中的程序停止通信和图41.57中的错误处理程序。

41.8.7 恢复沟通

当您使用SSIE恢复通信时，请遵循图41.58中的通信恢复过程。通信恢复过程的设计假设您恢复了由

communication stop procedure without changing any settings. If you want to change clock and slave/master settings, use and follow the communication start procedure in Figure 41.53. For details about the transmission operation and reception operation after starting communication, see reference 41.8.2 and reference 41.8.3, respectively.

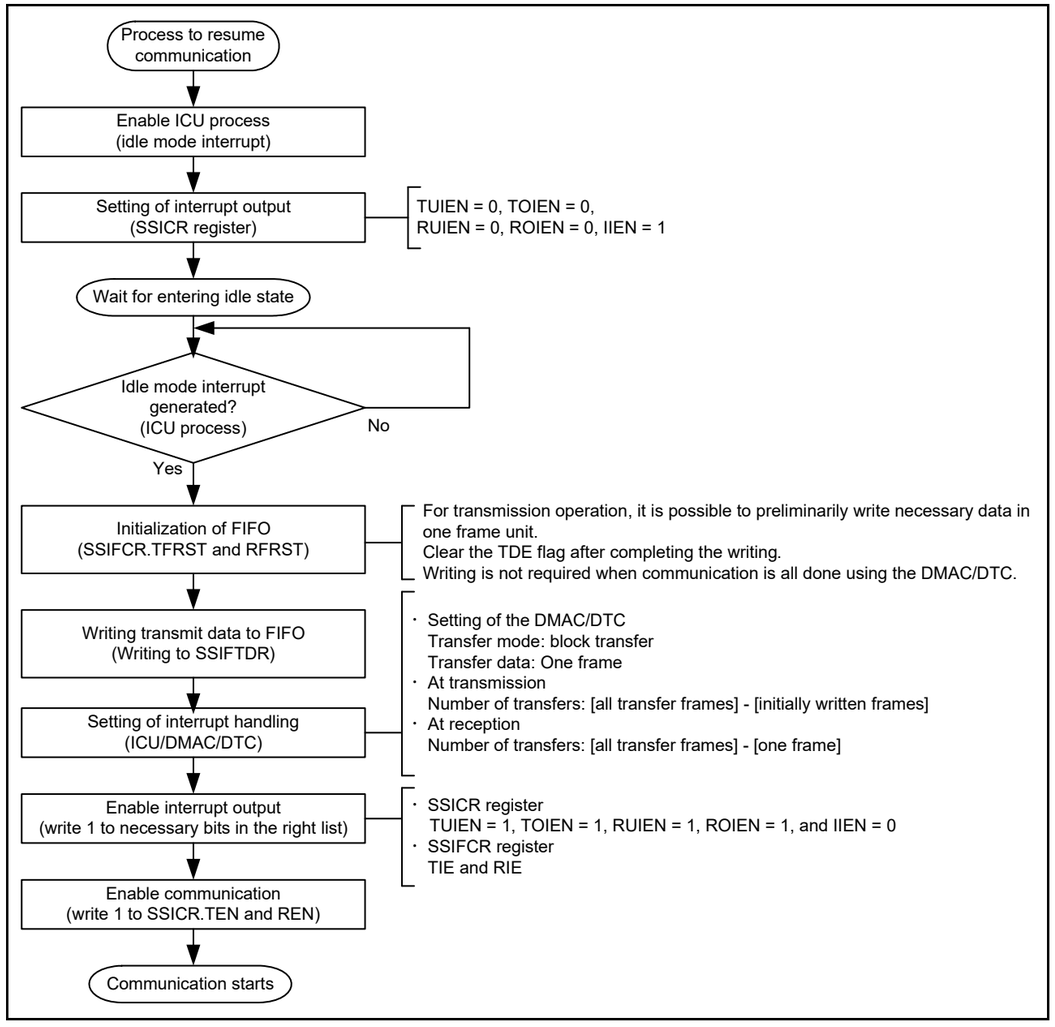


Figure 41.58 Procedure to resume communication (CPU operation procedure)

41.9 Interrupts

Table 41.16 lists the interrupt sources. Set enable/disable of interrupt output of each source with the TUIEN, TOIEN, RUIEN, ROIEN, and IIEN bits in the SSICR register and the TIE and RIE bits in the SSIFCR register.

通信停止程序，无需更改任何设置。如果要更改时钟和从主机设置，请使用并遵循图41.53中的通信启动程序。关于开始通信后的发送操作和接收操作的详细信息，请分别参见参考41.8.2和参考41.8.3。

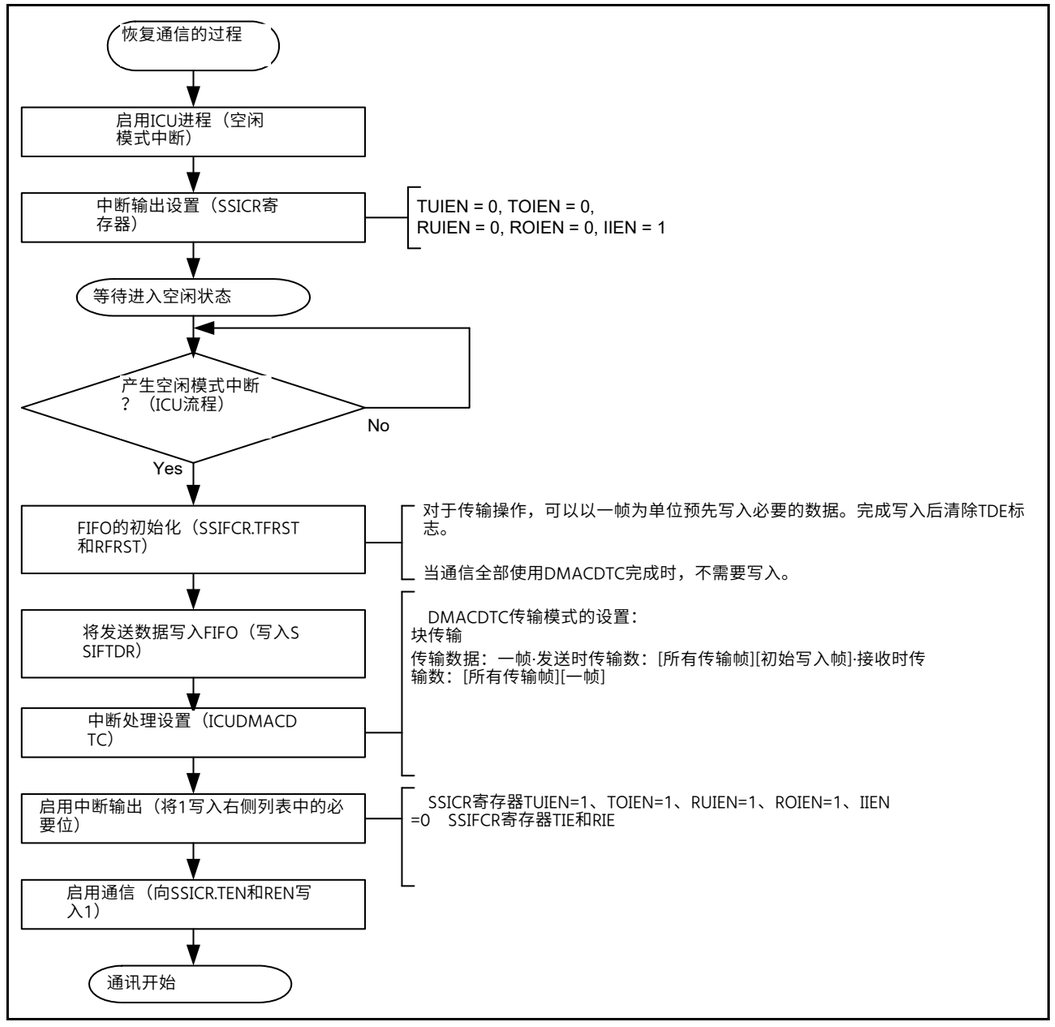


Figure 41.58 恢复通信的步骤（CPU操作步骤）

41.9 Interrupts

表41.16列出了中断源。使用TUIEN、TOIEN、SSICR寄存器中的RUIEN、ROIEN和IIEN位以及SSIFCR寄存器中的TIE和RIE位。

Table 41.16 SSIE interrupt sources

Channel	Interrupt source	Description	Interrupt flag	DMAC/DTC activation
SSIE0	SSIE0_SSIF	• Transmit underflow interrupt • Transmit overflow interrupt • Receive underflow interrupt • Receive overflow interrupt • Idle interrupt	SSISR.TUIRQ SSISR.TOIRQ SSISR.RUIRQ SSISR.ROIRQ SSISR.IIRQ	Not possible
	SSIE0_SSIRXI	Receive data full interrupt	SSIFSR.RDF	Possible
	SSIE0_SSITXI	Transmit data empty interrupt	SSIFSR.TDE	Possible
SSIE1	SSIE1_SSIF	• Transmit underflow interrupt • Transmit overflow interrupt • Receive underflow interrupt • Receive overflow interrupt • Idle interrupt	SSISR.TUIRQ SSISR.TOIRQ SSISR.RUIRQ SSISR.ROIRQ SSISR.IIRQ	Not possible
	SSIE1_SSIRT	• Receive data full interrupt • Transmit data empty interrupt	SSIFSR.RDF/ SSIFSR.TDE	Possible

41.9.1 SSIEn_SSIF Interrupt

This interrupt source combines five interrupts. Enable output of necessary interrupts before using SSIE. The five interrupts are operated by using the flags assigned to individual interrupts and interrupt output enable bits. To clear an interrupt, set the interrupt enable to 0 or clear the interrupt flag to 0.

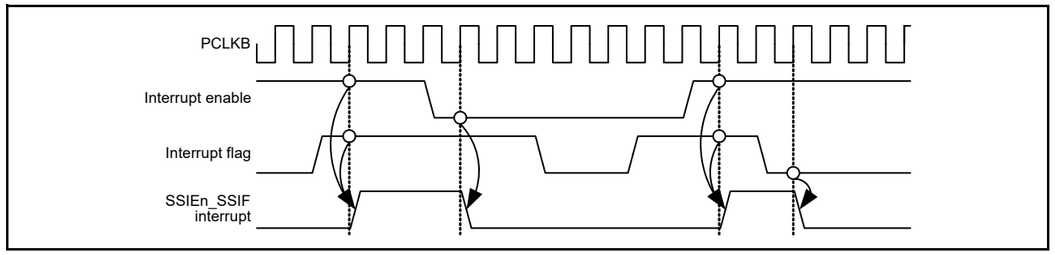


Figure 41.59 Timing Diagram of the common interrupt source, SSIEn_SSIF

- Transmit underflow interrupt

As the transmit underflow interrupt, SSISR.TUIRQ is output while SSICR.TUIEN = 1. When you use SSIE for transmission, enable the output of this interrupt (SSICR.TUIRQ = 1). If this interrupt occurs, follow instructions in the procedure to halt communication in Figure 41.56 and error-handling procedure in Figure 41.57.

- Transmit overflow interrupt

As the transmit overflow interrupt, SSISR.TOIRQ is output while SSICR.TOIRQ = 1. When you use SSIE for transmission, enable the output of this interrupt (SSICR.TOIRQ = 1). If this interrupt occurs, follow instructions in the procedure to halt communication in Figure 41.56 and error-handling procedure in Figure 41.57.

- Receive underflow interrupt

As the receive underflow interrupt, SSISR.RUIRQ is output while SSICR.RUIRQ = 1. When you use SSIE for reception, enable the output of this interrupt (SSICR.RUIRQ = 1). If this interrupt occurs, follow instructions in the procedure to halt communication in Figure 41.56 and error-handling procedure in Figure 41.57.

- Receive overflow interrupt

As the receive overflow interrupt, SSISR.ROIRQ is output while SSICR.ROIRQ = 1. When you use SSIE for reception, enable the output of this interrupt (SSICR.ROIRQ = 1). If this interrupt occurs, follow instructions in the procedure to halt communication in Figure 41.56 and error-handling procedure in Figure 41.57.

- Idle mode interrupt

Table 41.16 SSIE中断源

Channel	中断源	Description	中断标志	DMAC/DTC activation
SSIE0	SSIE0_SSIF	发送下溢中断 发送上溢中断 接收下溢中断 接收上溢中断 空闲中断	SSISR.TUIRQ SSISR.TOIRQ SSISR.RUIRQ SSISR.ROIRQ SSISR.IIRQ	不可能
	SSIE0_SSIRXI	接收数据满中断	SSIFSR.RDF	Possible
	SSIE0_SSITXI	发送数据空中断	SSIFSR.TDE	Possible
SSIE1	SSIE1_SSIF	发送下溢中断 发送上溢中断 接收下溢中断 接收上溢中断 空闲中断	SSISR.TUIRQ SSISR.TOIRQ SSISR.RUIRQ SSISR.ROIRQ SSISR.IIRQ	不可能
	SSIE1_SSIRT	接收数据满中断 发送数据空中断	SSIFSR.RDF/ SSIFSR.TDE	Possible

41.9.1 SSIEn_SSIF Interrupt

该中断源结合了五个中断。在使用SSIE之前启用必要中断的输出。通过使用分配给各个中断的标志和中断输出使能位来操作五个中断。要清除中断，请将中断使能设置为0或将中断标志清除为0。

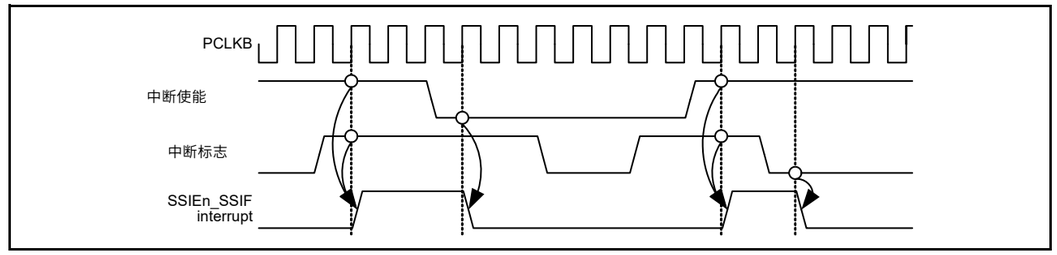


Figure 41.59 公共中断源SSIEn_SSIF的时序图

- 发送下溢中断

作为发送下溢中断，在SSICR.TUIEN=1时输出SSISR.TUIRQ。当使用SSIE进行发送时，使能该中断的输出（SSICR.TUIRQ=1）。如果发生此中断，请按照图41.56中的停止通信过程和图41.57中的错误处理过程中的说明进行操作。

- 发送溢出中断

作为发送溢出中断，在SSICR.TOIRQ=1时输出SSISR.TOIRQ。当使用SSIE进行发送时，使能该中断的输出（SSICR.TOIRQ=1）。如果发生此中断，请按照图41.56中的停止通信过程和图41.57中的错误处理过程中的说明进行操作。

- 接收下溢中断

作为接收下溢中断，在SSICR.RUIRQ=1时输出SSISR.RUIRQ。当使用SSIE进行接收时，使能该中断的输出（SSICR.RUIRQ=1）。如果发生此中断，请按照图41.56中的停止通信过程和图41.57中的错误处理过程中的说明进行操作。

- 接收溢出中断

作为接收溢出中断，在SSICR.ROIRQ=1时输出SSISR.ROIRQ。当使用SSIE进行接收时，使能该中断的输出（SSICR.ROIRQ=1）。如果发生此中断，请按照图41.56中的停止通信过程和图41.57中的错误处理过程中的说明进行操作。

- 空闲模式中断

As the idle mode interrupt, SSISR.IIRQ is output while SSICR.IIEN = 1. This interrupt is used to make sure that communication has stopped fully.

41.9.2 SSIE0_SSITXI Interrupt [Full-duplex communication]

The transmit data empty interrupt is a pulse interrupt that is output when the following condition is met:

- SSIFCR.TIE = 1 and SSIFSR.TDE = 1

  SSIE operation: When the value of SSIFSR.TDE changes from 0 to 1 while the value of SSIFCR.TIE is 1
  CPU instruction: When the value of SSIFCR.TIE changes from 0 to 1 while the value of SSIFSR.TDE is 1

This interrupt is subject to the interrupt suppression function. If an interrupt condition for this interrupt occurs when the DTC/DMAC is busy (when the DTC/DMAC cannot accept interrupts), the interrupt suppression function holds the output of this interrupt. The held interrupt will be output after the DTC/DMAC is enabled to accept interrupts. For details, see Figure 41.60.

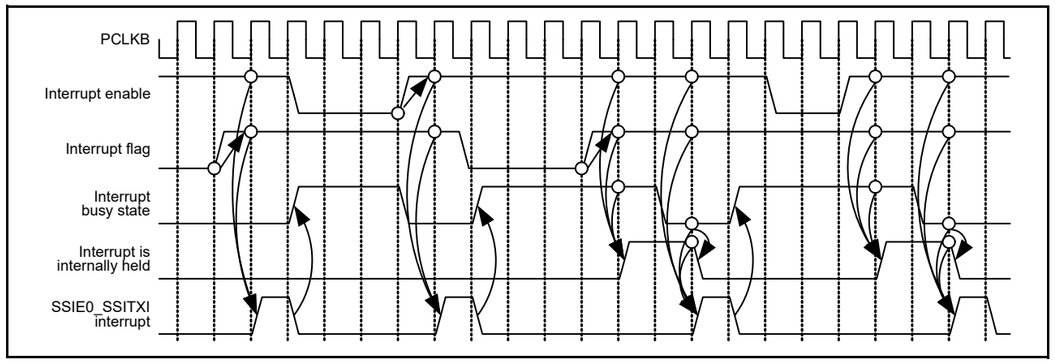


Figure 41.60 SSIE0_SSITXI interrupt timing diagram

41.9.3 SSIE0_SSIRXI Interrupt [Full-duplex communication]

The receive data full interrupt is a pulse interrupt that is output when the following condition is met:

- SSIFCR.RIE = 1 and SSIFSR.RDF = 1.

  SSIE operation: When the value of SSIFSR.RDF changes from 0 to 1 while the value of SSIFCR.RIE is 1
  CPU instruction: When the value of SSIFCR.RIE changes from 0 to 1 while the value of SSIFSR.RDE is 1

This interrupt is subject to the interrupt suppression function. If an interrupt condition for this interrupt occurs when the DTC/DMAC is busy (when the DTC/DMAC cannot accept interrupts), the interrupt suppression function holds the output of this interrupt. The held interrupt will be output after the DTC/DMAC is enabled to accept interrupts. The behavior of this interrupt is the same as the behavior shown in Figure 41.60.

41.9.4 SSIE1_SSIRT Interrupt [Half-duplex communication]

This interrupt is output by two sources, transmit data empty interrupt and receive data full interrupt. When this interrupt is generated, read the interrupt flag and specify the interrupt source.

This interrupt is subject to the interrupt suppression function. If an interrupt condition for this interrupt occurs when the DTC/DMAC is busy (when the DTC/DMAC cannot accept interrupts), the interrupt suppression function holds the output of this interrupt. The held interrupt will be output after the DTC/DMAC is enabled to accept interrupts. For details, see Figure 41.61.

作为空闲模式中断，在SSICR.IIEN=1时输出SSISR.IIRQ。此中断用于确保通信已完全停止。

41.9.2 SSIE0_SSITXI Interrupt [Full-duplex communication]

发送数据空中断是一个脉冲中断，当满足以下条件时输出：

- SSIFCR.TIE = 1 and SSIFSR.TDE = 1

  SSIE操作：当SSIFSR.TDE的值从0变为1且SSIFCR.TIE的值为1时CPU指令：当SSIFCR.TIE的值从0变为1且SSIFSR.TDE的值为1时

该中断受中断抑制功能影响。如果此中断的中断条件发生时，
DTCDMAC忙（当DTCDMAC不能接受中断时），中断抑制功能保持该中断的输出。在DTCDMAC使能接受中断后，将输出保持的中断。详见图41.60。

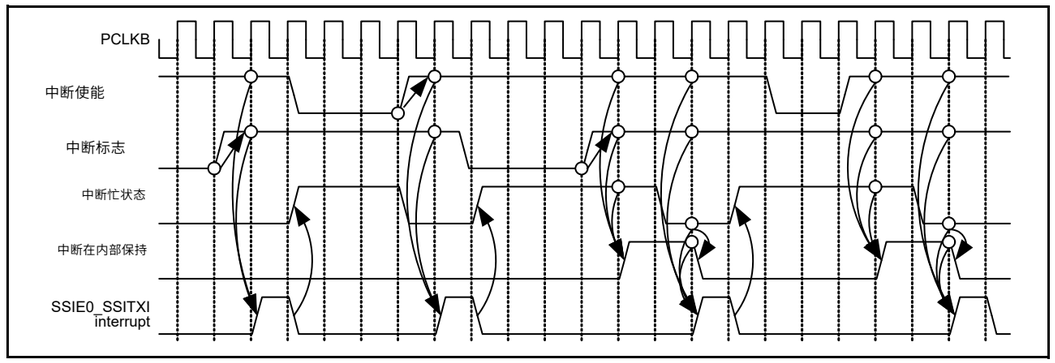


Figure 41.60 SSIE0_SSITXI中断时序图

41.9.3 SSIE0_SSIRXI Interrupt [Full-duplex communication]

接收数据满中断是一个脉冲中断，当满足以下条件时输出：

- SSIFCR.RIE = 1 and SSIFSR.RDF = 1.

  SSIE操作：当SSIFSR.RDF的值从0变为1且SSIFCR.RIE的值为1时CPU指令：当SSIFCR.RIE的值从0变为1且SSIFSR.RDE的值为1时

该中断受中断抑制功能影响。如果此中断的中断条件发生时，
DTCDMAC忙（当DTCDMAC不能接受中断时），中断抑制功能保持该中断的输出。在DTCDMAC使能接受中断后，将输出保持的中断。此中断的行为与图41.60中所示的行为相同。

41.9.4 SSIE1_SSIRT Interrupt [Half-duplex communication]

该中断由两个源输出，发送数据空中断和接收数据满中断。当该中断产生时，读取中断标志并指定中断源。

该中断受中断抑制功能影响。如果此中断的中断条件发生时，
DTCDMAC忙（当DTCDMAC不能接受中断时），中断抑制功能保持该中断的输出。在DTCDMAC使能接受中断后，将输出保持的中断。详见图41.61。

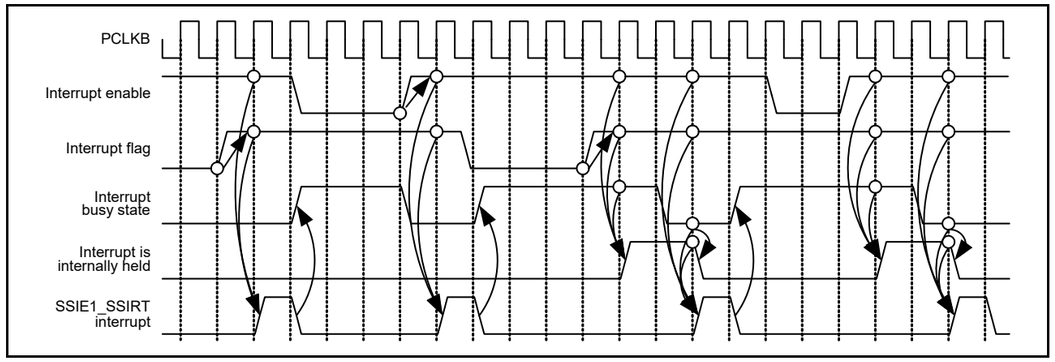


Figure 41.61 SSIE1_SSIRT interrupt timing diagram

41.10 Software Resets

SSIE has three software reset bits to reset its states.

- SSIE software reset (SSIFCR.SSIRST)
- Transmit FIFO data register reset (SSIFCR.TFRST)
- Receive FIFO data register reset (SSIFCR.RFRST).

This section describes the procedures for the three types of software resets.

41.10.1 Software Reset Procedure

(1) SSIE Software Reset

For the SSIE software reset bit (SSIFCR.SSIRST), follow the procedure shown in Figure 41.62. After a reset, the same setting is applied when it is resumed. To change the settings of clocks and slave/master mode, follow the procedure to start communication in Figure 41.53. See reference 41.8.2 and reference 41.8.3 respectively for transmission and reception after communication is resumed.

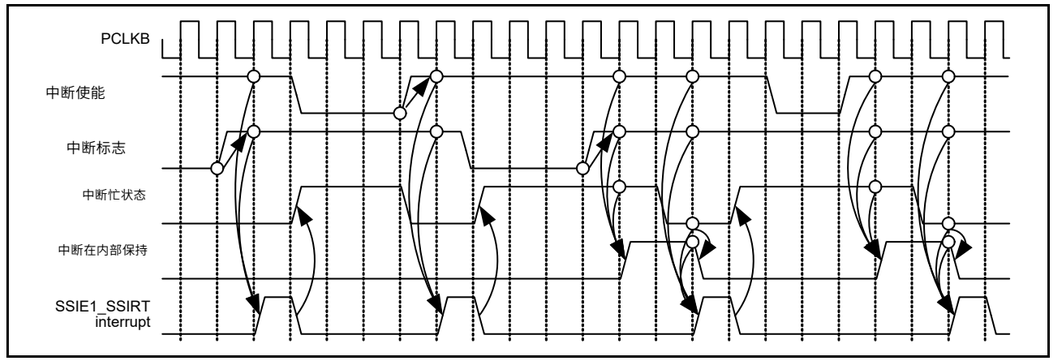


Figure 41.61 SSIE1_SSIRT中断时序图

41.10 软件复位

SSIE具有三个软件复位位来复位其状态。

- SSIE软件复位(SSIFCR.SSIRST)
- 发送FIFO数据寄存器复位(SSIFCR.TFRST)
- 接收FIFO数据寄存器复位(SSIFCR.RFRST)。

本节介绍三种软件复位的过程。

41.10.1 软件复位程序

(1) SSIE软件复位

对于SSIE软件复位位(SSIFCR.SSIRST)，请按照图41.62中所示的过程。重置后，恢复时应用相同的设置。要更改时钟和从主模式的设置，请按照图41.53中的步骤开始通信。恢复通信后的发送和接收分别参见参考41.8.2和参考41.8.3。

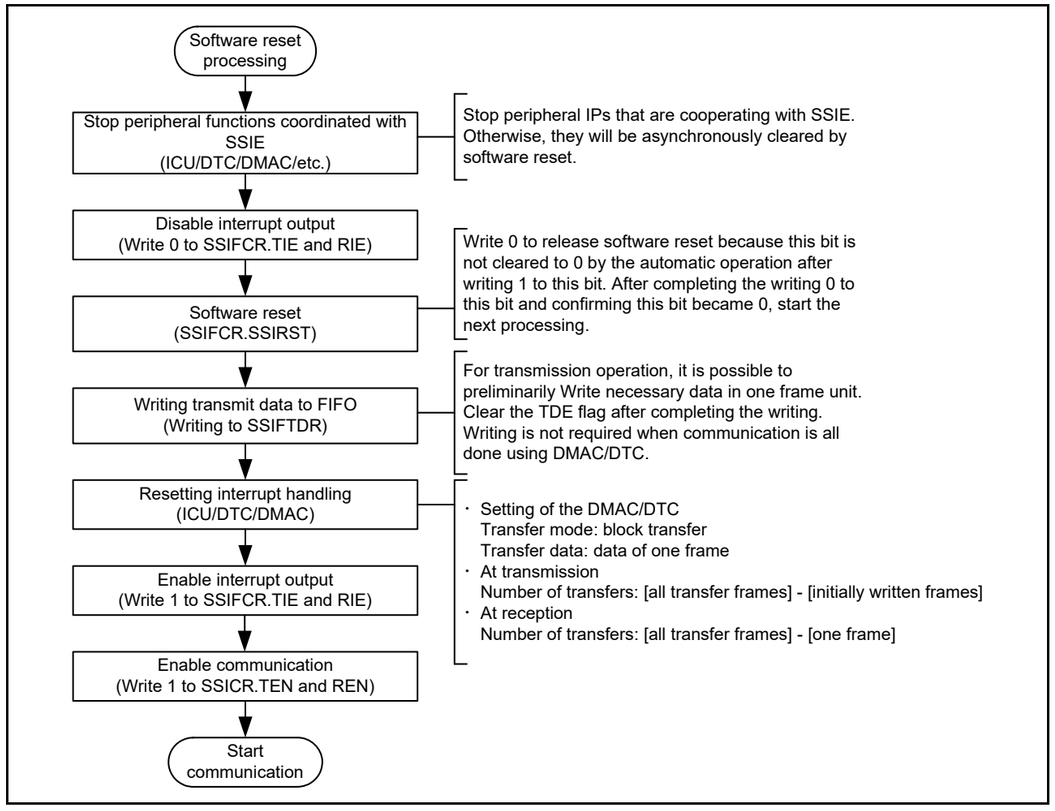


Figure 41.62 Software reset procedure (CPU operation procedure)

(2) Transmit FIFO data register reset

To perform a transmit FIFO data register reset, follow instructions in the procedure to start communication in Figure 41.53 and procedure to resume communication in Figure 41.58.

(3) Receive FIFO data register reset

To perform a receive FIFO data register reset, follow instructions in the procedure to start communication in Figure 41.53 and procedure to resume communication in Figure 41.58.

41.11 Notes

41.11.1 Notes for Slave-mode Communication

41.11.1.1 ADCKE control

In slave-mode communication (SSICR.MST = 0), SSIE needs supply of SSIBCK. To stop BCK on the master side, make sure that SSIE is in the idle state (SSISR.IIRQ = 1). If BCK is stopped before SSIE becomes idle, take the procedure to start communication in Figure 41.53 or wait for an idle state by taking the procedure to resume communication in Figure 41.58.

41.11.1.2 SSILRCK/SSIFS pin

SSIE has the SSILRCK/SSIFS pin, which indicates the synchronization of communication. When SSIE is in slave mode (SSICR.MST = 0), the communication format SSIE uses must match that of the other-party device to communicate. SSIE uses the signal input by the SSILRCK/SSIFS pin only as a trigger to start communication.

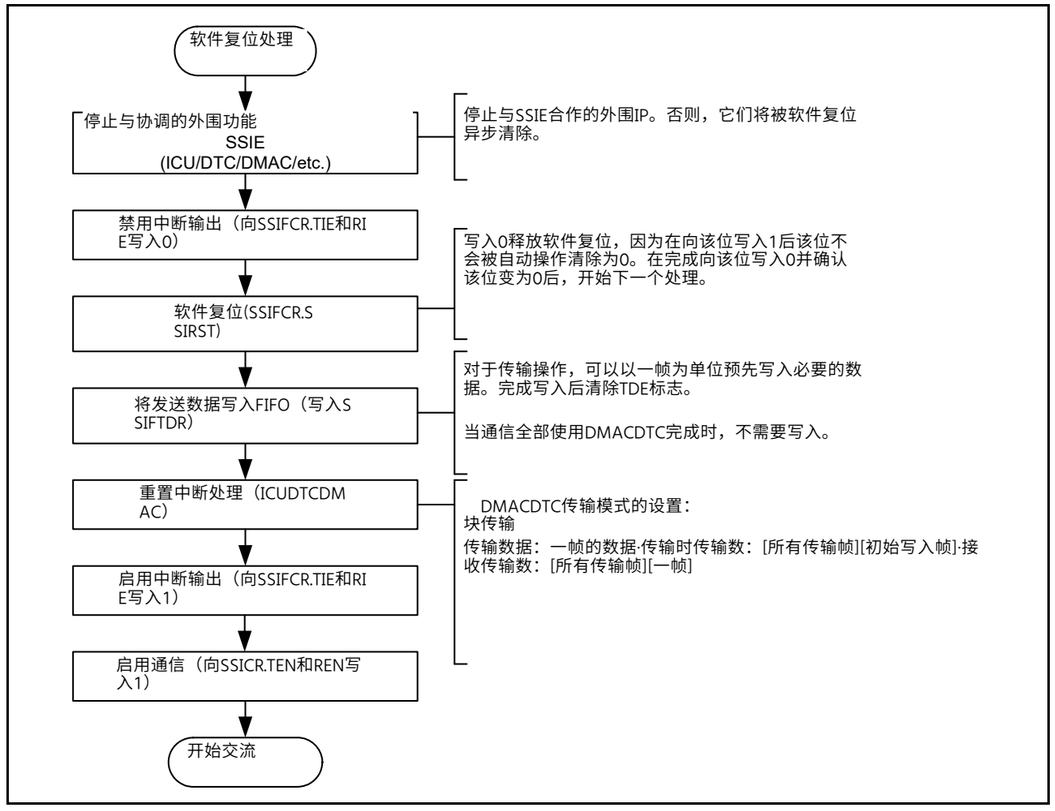


Figure 41.62 软件复位程序（CPU操作程序）

(2) 发送FIFO数据寄存器复位

要执行发送FIFO数据寄存器复位，请按照图41.53中的开始通信过程和图41.58中恢复通信的过程中的说明进行操作。

(3) 接收FIFO数据寄存器复位

要执行接收FIFO数据寄存器复位，请按照图41.53中的开始通信过程和图41.58中恢复通信的过程中的说明进行操作。

41.11 Notes

41.11.1 从模式通信注意事项

41.11.1.1 ADCKE control

在从模式通信(SSICR.MST=0)中，SSIE需要提供SSIBCK。要在主设备端停止BCK，请确保SSIE处于空闲状态(SSISR.IIRQ=1)。如果BCK在SSIE空闲之前停止，则按照图41.53中的程序开始通信，或者按照图41.58中的程序恢复通信等待空闲状态。

41.11.1.2 SSILRCK/SSIFS pin

SSIE有SSILRCKSSIFS引脚，表示通信同步。当SSIE处于从机模式（SSICR.MST=0）时，SSIE使用的通信格式必须与对方设备的通信格式相匹配。SSIE仅使用SSILRCKSSIFS引脚输入的信号作为启动通信的触发器。

41.11.2 Notes for Master-mode Communication

41.11.2.1 ADCKE control

In master-mode communication (SSICR.MST = 1), SSIE operates with the audio clock (AUDIO_MCK). To stop SSIE completely, make sure that SSIE is in the idle state (SSISR.IIRQ = 1) and then write 0 to SSIFCR.ADCKE.

41.11.2.2 LRCONT control

To stop the output to the SSILRCK/SSIFS pin with SSIOFR.LRCONT when SSIE is in the idle state in master-mode communication (SSICR.MST = 1), note the following: The output stops when the value of the SSIOFR.LRCONT bit is changed from 1 to 0. Make sure that the other-party device is not affected. For details, see Figure 41.44.

41.11.2.3 BCKASTP control

To stop the output to the SSIBCK pin with SSIOFR.BCKASTP in master-mode communication (SSICR.MST = 1) and while SSIE is in the idle state, note the following: The output stops when the value of the SSIOFR.BCKASTP bit is changed from 0 to 1. So, make sure that the other-party device is not affected. For details, see Figure 41.45.

The BCKASTP bit cannot be used when the other-party device (which is a slave) requires the clock output from the SSIBCK pin before and during communication.

41.11.3 Notes for Communication Flow

41.11.3.1 When an error interrupt is generated

SSIE has the following four errors.

- Transmit underflow error
- Transmit overflow error
- Receive underflow error
- Receive overflow error.

When an underflow error or overflow error is generated, SSIE need to be restarted. Follow the procedure to halt communication in Figure 41.56 and error-handling procedure in Figure 41.57.

(1) Transmit Underflow Error

If a transmit underflow error occurs, review the number of times of writing data to the transmit FIFO data register (SSIFTDR) in response to a transmit data empty interrupt. After a transmit underflow error occurs, SSIE outputs 0s as data. To normally output the serial data written to the transmit FIFO data register (SSIFTDR) to the SSITXD0/SSIDATA1 pin, follow the procedure to halt communication in Figure 41.56 and error-handling procedure in Figure 41.57. After this error occurs, serial data is consumed as usual. If you resume communication, write the serial data from the beginning.

(2) Transmit Overflow Error

If a transmit overflow error occurs, review the number of times of writing data to the Transmit FIFO Data Register (SSIFTDR) in response to transmit data empty interrupts. The serial data written to the Transmit FIFO Data Register (SSIFTDR) that caused the transmit overflow error becomes invalid. This error can occur regardless of whether a transmission operation is being done. To recover from the error, follow the procedure to halt communication in Figure 41.56 and error-handling procedure in Figure 41.57. When you resume communication, deal with the invalid serial data appropriately.

(3) Receive Underflow Error

If a receive underflow error occurs, review the number of times of reading data from the receive FIFO data register (SSIFRDR) in response to receive data full interrupts. The values read from the receive FIFO data register (SSIFRDR) that caused the receive underflow error are undefined. This error can occur regardless of whether a reception operation is being done. To recover from the error, follow the procedure to halt communication in Figure 41.56 and error-handling procedure in Figure 41.57.

41.11.2 主模式通信注意事项

41.11.2.1 ADCKE control

在主模式通信(SSICR.MST=1)中，SSIE使用音频时钟(AUDIO_MCK)运行。要完全停止SSIE，请确保SSIE处于空闲状态(SSISR.IIRQ=1)，然后将0写入SSIFCR.ADCKE。

41.11.2.2 LRCONT control

当SSIE处于主模式通信中的空闲状态（SSICR.MST=1）时，要使用SSIOFR.LRCONT停止向SSILRCKSSIFS引脚的输出，请注意以下几点：当SSIOFR.LRCONT位的值为从1变为0。确保对方设备不受影响。详见图41.44。

41.11.2.3 BCKASTP control

要在主模式通信(SSICR.MST=1)和SSIE处于空闲状态时使用SSIOFR.BCKASTP停止向SSIBCK引脚的输出，请注意以下事项：当SSIOFR.BCKASTP位的值为从0变为1。因此，请确保对方设备不受影响。详见图41.45。

当对方设备（从设备）需要时钟输出时，不能使用BCKASTP位
SSIBCK引脚在通信之前和期间。

41.11.3 通信流程注意事项

41.11.3.1 产生错误中断时

SSIE有以下四个错误。

- 发送下溢错误
- 传输溢出错误
- 接收下溢错误
- 接收溢出错误。

当产生下溢错误或上溢错误时，需要重启SSIE。按照图41.56中的程序停止通信和图41.57中的错误处理程序。

(1) 发送下溢错误

如果发生发送下溢错误，请查看响应发送数据空中断而将数据写入发送FIFO数据寄存器(SSIFTDR)的次数。发生发送下溢错误后，SSIE输出0作为数据。要将写入发送FIFO数据寄存器(SSIFTDR)的串行数据正常输出到SSITXD0 SSIDATA1引脚，请按照图41.56中的程序停止通信和图41.57中的错误处理程序进行操作。发生此错误后，串行数据将照常使用。如果您恢复通信，请从头开始写入串行数据。

(2) 传输溢出错误

如果发生发送溢出错误，请检查向发送FIFO数据寄存器(SSIFTDR)写入数据以响应发送数据空中断的次数。导致发送溢出错误的写入发送FIFO数据寄存器(SSIFTDR)的串行数据变为无效。无论是否正在执行传输操作，都可能发生此错误。要从错误中恢复，请按照图41.56中的程序停止通信和图41.57中的错误处理程序。当您恢复通信时，请适当处理无效的串行数据。

(3) 接收下溢错误

如果发生接收下溢错误，请检查从接收FIFO数据寄存器(SSIFRDR)读取数据以响应接收数据满中断的次数。从导致接收下溢错误的接收FIFO数据寄存器(SSIFRDR)读取的值未定义。无论是否正在执行接收操作，都可能发生此错误。要从错误中恢复，请按照图41.56中的程序停止通信和图41.57中的错误处理程序。

(4) Receive Overflow Error

If a receive overflow error occurs, review the number of times of reading data from the receive FIFO data register (SSIFRDR) in response to receive data full interrupts. The receive data that caused the receive overflow error cannot be stored in the receive FIFO data register (SSIFRDR). To recover from the error, follow the procedure to halt communication in Figure 41.56 and error-handling procedure in Figure 41.57.

41.11.3.2 Transmit data empty interrupt

The communication flow defined in SSIE uses the DTC/DMAC. If you do not use the DTC/DMAC, perform polling of the value 1 of SSIFSR.TDE to write data to SSIFTDR. The number of times of writing data to SSIFTDR by detecting the value 1 of SSIFSR.TDE must be in accordance with the free space size of the transmit FIFO data register specified by SSISCR.TDES. After as much transmit data as the free space size is written to SSIFTDR, the SSIFSR.TDE flag must be cleared. Continuous transmission is enabled by repeating data writing. If the SSIFSR.TDE flag is not cleared, the flag is not cleared automatically.

41.11.3.3 Receive data full interrupt

The communication flow defined in SSIE uses the DTC/DMAC. If you do not use the DTC/DMAC, perform polling of the value 1 of SSIFSR.RDF to read data from SSIFRDR. The number of times of reading data from SSIFRDR by detecting the value 1 of SSIFSR.RDF must be in accordance with the receive data storage capacity of the receive FIFO data register specified by SSISCR.RDFS. After received data is read from SSIFRDR, the SSIFSR.RDF flag must be cleared. Continuous reception is enabled by repeating data reading. If the SSIFSR.RDF flag is not cleared, the flag is not cleared automatically.

41.11.3.4 Switching transfer modes

1. For state transition from transmission, reception, and transmission and reception, disable transmission and reception (SSICR.TEN = 0, SSICR.REN = 0).
2. Confirm it is in the idle state (SSISR.IIRQ = 1).
3. In the idle state, set the SSICR.TEN bit and the SSICR.REN bit again and resume transfer.

41.11.3.5 Resume communication after halting SSIE

When communication of SSIE is halted according to the procedure to halt communication in Figure 41.56, resume communication according to the procedure to resume communication in Figure 41.58.

41.11.4 Write Access Restriction

41.11.4.1 SSICR register

If the TEN bit or REN bit is rewritten, make sure that the SSISR.IIRQ bit is in the desired status. If the value of the TEN or REN bit is changed by rewriting, subsequent operation is unpredictable. For example, when transmission or reception is enabled, check that SSISR.IIRQ is 0; when transmission or reception is disabled, check that SSISR.IIRQ is 1.

(1) TEN Bit and REN Bit

These bits enable/disable transmission and reception. When 1 is written to one of these bits, the corresponding communication operation starts in synchronization with a start trigger by the SSILRCK/SSIFS signal. For details, see reference 41.8.2, reference 41.8.3, and reference 41.8.4. When 0 is written to this bit, the current communication operation stops at the next frame boundary. To use SSIE for both transmission and reception, always write 1 to these bits together. When stopping the communication using SSIE, always disable both transmission and reception (write 0 to the TEN and REN bits).

41.11.4.2 SSISR register

(1) Clearing TUIRQ and TOIRQ

After communication is enabled (by changing the value of SSICR.TEN bit from 0 to 1), the transmission error flags (TOIRQ and TUIRQ in the SSISR register) are cleared. If, however, the SSISR register is read continuously, the cleared status of the transmission error flags might be unable to be read.

(4) 接收溢出错误

如果发生接收溢出错误，请检查从接收FIFO数据寄存器(SSIFRDR)读取数据以响应接收数据满中断的次数。导致接收溢出错误的接收数据不能存储在接收FIFO数据寄存器(SSIFRDR)中。要从错误中恢复，请按照图41.56中的程序停止通信和图41.57中的错误处理程序。

41.11.3.2 发送数据空中断

SSIE中定义的通信流使用DTCDMAC。如果不使用DTCDMAC，则轮询SSIFSR.TDE的值1以将数据写入SSIFTDR。通过检测SSIFSR.TDE的值为1向SSIFTDR写入数据的次数必须与SSIFSR.TDES指定的发送FIFO数据寄存器的空闲空间大小一致。在将与可用空间大小一样多的传输数据写入SSIFTDR后，必须清除SSIFSR.TDE标志。通过重复数据写入启用连续传输。如果未清除SSIFSR.TDE标志，则不会自动清除该标志。

41.11.3.3 接收数据满中断

SSIE中定义的通信流使用DTCDMAC。如果不使用DTCDMAC，则轮询SSIFSR.RDF的值1以从SSIFRDR读取数据。检测SSIFSR.RDF的值为1从SSIFRDR读取数据的次数必须与SSISCR.RDFS指定的接收FIFO数据寄存器的接收数据存储容量一致。从SSIFRDR读取接收到的数据后，必须清除SSIFSR.RDF标志。通过重复数据读取启用连续接收。如果SSIFSR.RDF标志未清除，则该标志不会自动清除。

41.11.3.4 切换传输模式

1. 对于从发送、接收和发送和接收的状态转换，禁用发送和接收（SSICR.TEN=0，SSICR.REN=0）。
2. 确认它处于空闲状态(SSISR.IIRQ=1)。
3. 在空闲状态下，再次设置SSICR.TEN位和SSICR.REN位并恢复传输。

41.11.3.5 停止SSIE后恢复通信

当SSIE的通信按照图41.56中的停止通信程序停止时，按照图41.58中的恢复通信程序恢复通信。

41.11.4 写访问限制

41.11.4.1 SSICR register

如果TEN位或REN位被重写，请确保SSISR.IIRQ位处于所需状态。如果TEN或REN位的值因重写而改变，后续操作将无法预测。例如，启用发送或接收时，检查SSISR.IIRQ是否为0；当发送或接收被禁用时，检查SSISR.IIRQ是否为1。

(1) 十位和仁位

这些位启用禁用发送和接收。当这些位之一写入1时，相应的通信操作与SSILRCKSSIFS信号的开始触发同步开始。有关详细信息，请参阅参考41.8.2、参考41.8.3和参考41.8.4。当向该位写入0时，当前通信操作在下一帧边界处停止。要同时使用SSIE进行发送和接收，请始终将1一起写入这些位。使用SSIE停止通信时，始终禁用发送和接收（将0写入TEN和REN位）。

41.11.4.2 SSISR register

(1) 清除TUIRQ和TOIRQ

启用通信后（通过将SSICR.TEN位的值从0更改为1），传输错误标志（SSISR寄存器中的TOIRQ和TUIRQ）被清除。但是，如果连续读取SSISR寄存器，则可能无法读取传输错误标志的清除状态。

(2) Clearing RUIRQ and ROIRQ

After communication is enabled (by changing the value of SSICR.REN bit from 0 to 1), the reception error flags (RUIRQ and ROIRQ in the SSISR register) are cleared. If, however, the SSISR register is read continuously, the cleared status of the reception error flags might be unable to be read.

41.11.4.3 Communication state

Writing to the bits with orange-shaded area in Table 41.17 is prohibited. If written, the operation performed immediately after writing is not guaranteed.

(2) 清除RUIRQ和ROIRQ

启用通信后（通过将SSICR.REN位的值从0更改为1），接收错误标志（SSISR寄存器中的RUIRQ和ROIRQ）被清除。但是，如果连续读取SSISR寄存器，则可能无法读取接收错误标志的清除状态。

41.11.4.3 通讯状态

禁止写入表41.17中橙色阴影区域的位。如果写入，则不保证写入后立即执行的操作。

Table 41.17 Bits protected from writing during communication

Symbol	Address (BASE+)		+0								+1							
			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSICR	00h	+0	—	CKS	TUIEN	TOIEN	RUIEN	ROIEN	IIEN	—	FRM[1:0]		DWL[2:0]			SWL[2:0]		
		+2	—	MST	BCKP	LRCKP	SPDP	SDTA	PDTA	DEL	CKDV[3:0]				MUEN	—	TEN	REN
SSISR	04h	+0	—	—	TUIRQ	TOIRQ	RUIRQ	ROIRQ	IIRQ	—	—	—	—	—	—	—	—	—
		+2	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
SSIFCR	10h	+0	AUCKE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SSIRST
		+2	—	—	—	—	BSW	—	—	—	—	—	—	—	TIE	RIE	TFRST	RFRST
SSIFSR	14h	+0	—	—	TDC[5:0]						—	—	—	—	—	—	—	TDE
		+2	—	—	RDC[5:0]						—	—	—	—	—	—	—	RDF
SSIFTDR	18h	+0	FTDR[31:16]															
		+2	FTDR[15:0]															
SSIFRDR	1ch	+0	FRDR[31:16]															
		+2	FRDR[15:0]															
SSIOFR	20h	+0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		+2	—	—	—	—	—	—	BCKASTP	LRCONT	—	—	—	—	—	—	OMOD[1:0]	
SSISCR	24h	+0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		+2	—	—	—	TDES[4:0]					—	—	—	RDFS[4:0]				

Table 41.17 通信期间防止写入的位

Symbol	Address (BASE+)		+0								+1							
			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SSICR	00h	+0	—	CKS	途恩	托伊恩	瑞恩	投资回报率CN	IIEN	—	FRM[1:0]		DWL[2:0]			SWL[2:0]		
		+2	—	MST	BCKP	LRCKP	SPDP	SDTA	PDTA	DEL	CKDV[3:0]				穆恩	—	TEN	REN
SSISR	04h	+0	—	—	TUIRQ	TOIRQ	RUIRQ	ROIRQ	IIRQ	—	—	—	—	—	—	—	—	—
		+2	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
SSIFCR	10h	+0	AUCKE	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SSIRST
		+2	—	—	—	—	BSW	—	—	—	—	—	—	—	TIE	RIE	TFRST	RFRST
SSIFSR	14h	+0	—	—	TDC[5:0]						—	—	—	—	—	—	—	TDE
		+2	—	—	RDC[5:0]						—	—	—	—	—	—	—	RDF
SSIFTDR	18h	+0	FTDR[31:16]															
		+2	FTDR[15:0]															
SSIFRDR	1ch	+0	FRDR[31:16]															
		+2	FRDR[15:0]															
SSIOFR	20h	+0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		+2	—	—	—	—	—	—	BCKASTP	LRCONT	—	—	—	—	—	—	OMOD[1:0]	
SSISCR	24h	+0	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
		+2	—	—	—	TDES[4:0]					—	—	—	RDFS[4:0]				

42. Sampling Rate Converter (SRC)

42.1 Overview

The Sampling Rate Converter (SRC) is used to convert the sampling rate of data produced by various audio decoders, including WMA, MP3, and AAC. Both 16-bit stereo and monaural data are supported. The sampling rate of the input signal can be one of the following (in kHz): 8, 11.025, 12, 16, 22.05, 24, 32, 44.1, or 48 kHz. The sampling rate of the output signal can be one of the following (in kHz): 8, 16, 32, 44.1, or 48 kHz. Independent FIFOs are provided for input and output. In a typical application, a DMA controller can be used to transfer PCM audio data from the SRAM (for example) to the SRC. Sample-converted audio data from the SRC can then be transferred using the DMA Controller to the SSIE interface, from where it can be transmitted to an external audio codec.

Table 42.1 shows the SRC specifications and Figure 42.1 shows a block diagram.

Table 42.1 SRC specifications

Parameter		Specifications
Data size		16 bits (stereo/monaural)
Sampling rates	Input	Selectable to 8, 11.025, 12, 16, 22.05, 24, 32, 44.1, or 48 kHz
	Output	Selectable to 8*1, 16*1, 32, 44.1, or 48 kHz
Processing capacity		Maximum of 7.7 µs for one sample output interval (PCLKB = 60 MHz, 462 clocks)
SNR		80 db or higher
Interrupt sources		Five Input FIFO empty, output FIFO full, output FIFO overflow, output FIFO underflow, and conversion end
DMA transfer sources		Two Input FIFO empty and output FIFO full
Module-stop function		Module-stop state can be set to reduce power consumption

Note 1. Only when input of 44.1 kHz is selected.

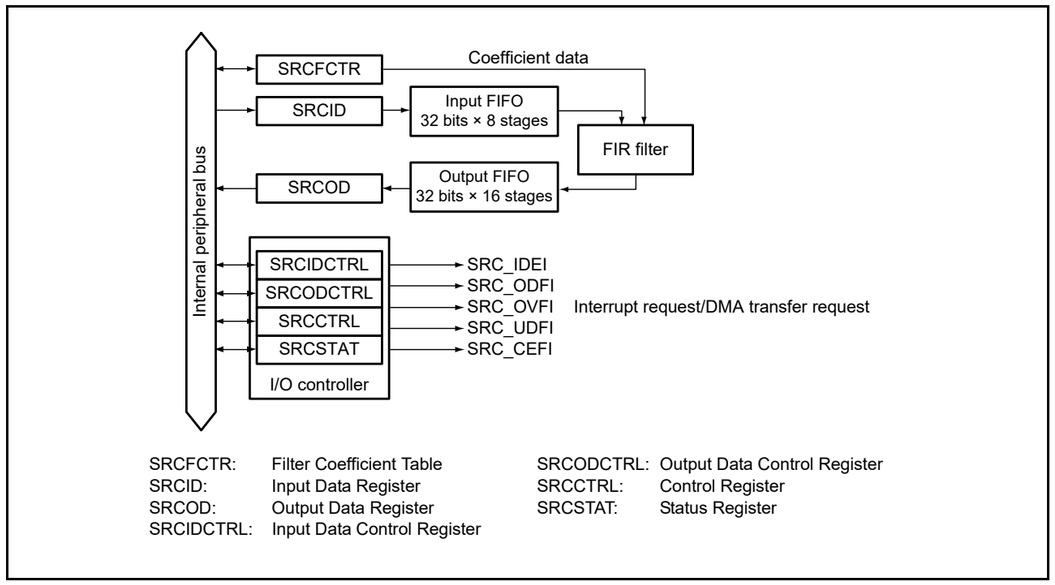


Figure 42.1 SRC block diagram

42. 采样率转换器(SRC)

42.1 Overview

采样率转换器(SRC)用于转换各种音频解码器（包括WMA、MP3和AAC）产生的数据的采样率。支持16位立体声和单声道数据。输入信号的采样率可以是以下之一（以kHz为单位）：8、11.025、12、16、22.05、24、32、44.1或48kHz。输出信号的采样率可以是以下之一（以kHz为单位）：8、16、32、44.1或48kHz。为输入和输出提供了独立的FIFO。在典型应用中，DMA控制器可用于将PCM音频数据从SRAM（例如）传输到SRC。然后，可以使用DMA控制器将来自SRC的样本转换音频数据传输到SSIE接口，然后再将其传输到外部音频编解码器。

表42.1显示了SRC规范，图42.1显示了框图。

Table 42.1 SRC specifications

Parameter		Specifications
数据大小		16 bits (stereo/monaural)
采样率	Input	可选择8、11.025、12、16、22.05、24、32、44.1或48kHz
	Output	可选择8*1、16*1、32、44.1或48kHz
处理能力		1个采样输出间隔的最大值为7.7µs（PCLKB=60MHz，462个时钟）
SNR		80分贝或更高
中断源		Five 输入FIFO空，输出FIFO满，输出FIFO上溢，输出FIFO下溢，转换结束
DMA传输源		Two 输入FIFO为空，输出FIFO已满
Module-stop function		可设置模块停止状态以降低功耗

Note 1. Onlywheninputof44.1kHzisselected.

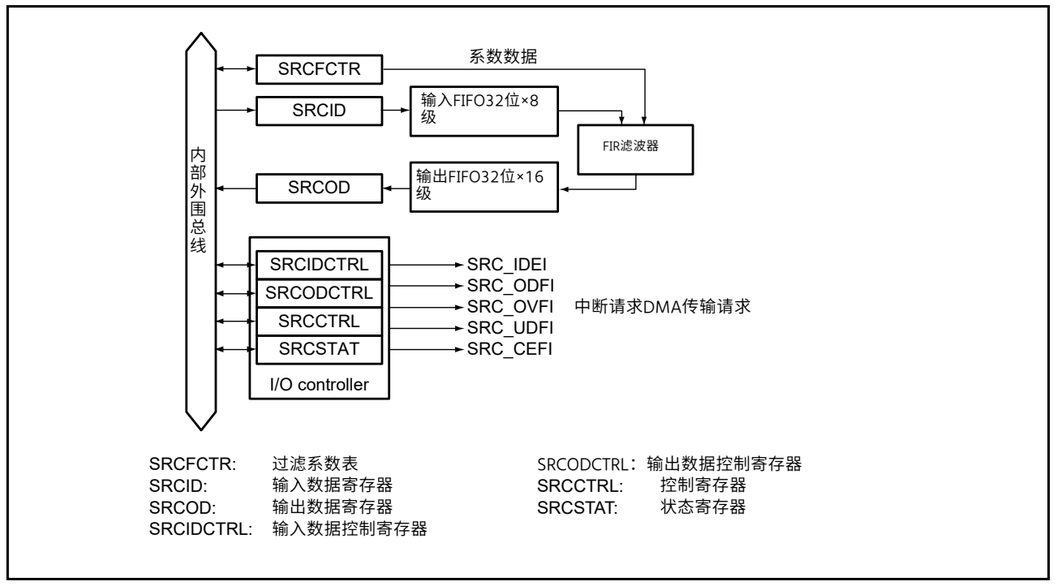


Figure 42.1 SRC框图

42.2 Register Descriptions

42.2.1 Input Data Register (SRCID)

Address(es): SRC.SRCID 4004 DFF0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The SRCID register is a 32-bit write-only register used to input the data before sampling rate conversion. All the bits are read as 0. The data input to SRCID is stored in the 8-stage input FIFO. When the number of data units in the input FIFO is 8, writing to SRCID has no effect.

For stereo data, bits [31:16] are for Lch data, and bits [15:0] are for Rch data. For monaural data, data in bits [31:16] is valid, and data in bits 15 to 0 is invalid.

The data subject to sampling rate conversion is aligned differently depending on the IED setting in SRCIDCTRL. Table 42.2 shows the correspondence between the IED setting and data alignment.

Table 42.2 Data alignment before sampling rate conversion

IED	Lch[15:8]	Lch[7:0]	Rch[15:8]	Rch[7:0]
0	SRCID[31:24]	SRCID[23:16]	SRCID[15:8]	SRCID[7:0]
1	SRCID[23:16]	SRCID[31:24]	SRCID[7:0]	SRCID[15:8]

42.2.2 Output Data Register (SRCOD)

Address(es): SRC.SRCOD 4004 DFF4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The SRCOD register is a 32-bit read-only register used to output the data after sampling rate conversion. The data in the 16-stage output FIFO is read through SRCOD. When the output FIFO is empty after the start of conversion, the value previously read is read again.

The data in SRCOD is aligned differently depending on the OCH and OED settings in SRCODCTRL. Table 42.3 shows the correspondence between the OCH and OED settings and data alignment in SRCOD.

Table 42.3 Data alignment in SRCOD (1 of 2)

OCH	OED	SRCOD[31:24]	SRCOD[23:16]	SRCOD[15:8]	SRCOD[7:0]
0	0	Lch[15:8]	Lch[7:0]	Rch[15:8]*1	Rch[7:0]*1
	1	Lch[7:0]	Lch[15:8]	Rch[7:0]*1	Rch[15:8]*1

42.2 注册说明

42.2.1 输入数据寄存器(SRCID)

Address(es): SRC.SRCID 4004 DFF0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SRCID寄存器是一个32位只写寄存器，用于在采样率转换之前输入数据。所有位都读为0。输入到SRCID的数据存储在8级输入FIFO中。当输入FIFO中的数据单元数为8时，写入SRCID无效。

对于立体声数据，位[31:16]用于Lch数据，位[15:0]用于Rch数据。对于单声道数据，bits[31:16]中的数据有效，bits15到0中的数据无效。

根据SRCIDCTRL中的IED设置，进行采样率转换的数据的排列方式不同。表42.2显示了IED设置和数据对齐之间的对应关系。

Table 42.2 采样率转换前的数据对齐

IED	Lch[15:8]	Lch[7:0]	Rch[15:8]	Rch[7:0]
0	SRCID[31:24]	SRCID[23:16]	SRCID[15:8]	SRCID[7:0]
1	SRCID[23:16]	SRCID[31:24]	SRCID[7:0]	SRCID[15:8]

42.2.2 输出数据寄存器(SRCOD)

Address(es): SRC.SRCOD 4004 DFF4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

SRCOD寄存器是一个32位只读寄存器，用于输出采样率转换后的数据。通过SRCOD读取16级输出FIFO中的数据。当转换开始后输出FIFO为空时，再次读取之前读取的值。

SRCOD中的数据根据 SRCODCTRL中的OCH和OED设置以不同方式对齐。表42.3显示了OCH和OED设置与SRCOD中数据对齐之间的对应关系。

Table 42.3 SRCOD中的数据对齐(1of2)

OCH	OED	SRCOD[31:24]	SRCOD[23:16]	SRCOD[15:8]	SRCOD[7:0]
0	0	Lch[15:8]	Lch[7:0]	Rch[15:8]*1	Rch[7:0]*1
	1	Lch[7:0]	Lch[15:8]	Rch[7:0]*1	Rch[15:8]*1

Table 42.3 Data alignment in SRCOD (2 of 2)

OCH	OED	SRCOD[31:24]	SRCOD[23:16]	SRCOD[15:8]	SRCOD[7:0]
1*2	0	Rch[15:8]	Rch[7:0]	Lch[15:8]	Lch[7:0]
	1	Rch[7:0]	Rch[15:8]	Lch[7:0]	Lch[15:8]

Note 1. When processing monaural data, the data in these bits is invalid. Discard the invalid data after reading from SRCOD in 32-bit units.
Note 2. When processing monaural data, the data in these bits is invalid.

42.2.3 Input Data Control Register (SRCIDCTRL)

Address(es): SRC.SRCIDCTRL 4004 DFF8h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	IED	IEN	—	—	—	—	—	—	IFTRG[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	IFTRG[1:0]	Input FIFO Data Triggering Number	b1 b0 0 0: 0 0 1: 2 1 0: 4 1 1: 6.	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	IEN	Input FIFO Empty Interrupt Enable	0: Disable input FIFO empty interrupts 1: Enable input FIFO empty interrupts.	R/W
b9	IED	Input Data Endian*1	0: Little endian 1: Big endian.	R/W
b15 to b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Only rewrite this bit while the SRCCTRL.SRCEN bit is 0.

The SRCIDCTRL register is a 16-bit read/write register that specifies the endian format of input data, enables or disables the interrupt requests, and specifies the triggering number of data units.

IFTRG[1:0] bits (Input FIFO Data Triggering Number)

The IFTRG[1:0] bits specify the data unit count at which the IINT flag in the Status Register (SRCSTAT) sets to 1. When the number of data units stored in the input FIFO becomes equal to or less than the specified triggering number, the IINT flag sets to 1.

IEN bit (Input FIFO Empty Interrupt Enable)

The IEN bit enables or disables issuing of the input FIFO empty interrupt request when the number of data units in the input FIFO becomes equal to or less than the triggering number specified in the IFTRG[1:0] bits, resulting in the IINT flag in the Status Register (SRCSTAT) setting to 1.

IED bit (Input Data Endian)

The IED bit specifies the endian format of the input data.

Table 42.3 SRCOD中的数据对齐(2of2)

OCH	OED	SRCOD[31:24]	SRCOD[23:16]	SRCOD[15:8]	SRCOD[7:0]
1*2	0	Rch[15:8]	Rch[7:0]	Lch[15:8]	Lch[7:0]
	1	Rch[7:0]	Rch[15:8]	Lch[7:0]	Lch[15:8]

Note 1. 处理单声道数据时，这些位中的数据无效。以32位为单位从SRCOD读取后丢弃无效数据。

Note 2. 处理单声道数据时，这些位中的数据无效。

42.2.3 输入数据控制寄存器(SRCIDCTRL)

Address(es): SRC.SRCIDCTRL 4004 DFF8h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	IED	IEN	—	—	—	—	—	—	IFTRG[1:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b1, b0	IFTRG[1:0]	输入FIFO数据触发数	b1 b0 0 0: 0 0 1: 2 1 0: 4 1 1: 6.	R/W
b7 to b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b8	IEN	输入FIFO空中断使能	0：禁用输入FIFO空中断1：启用输入FIFO空中断。	R/W
b9	IED	输入数据字节序 *1	0：小端1：大端。	R/W
b15 to b10	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 仅在SRCCTRL.SRCEN位为0时重写该位。

SRCIDCTRL寄存器是一个16位的读写寄存器，指定输入数据的字节序格式，启用或禁用中断请求，并指定数据单元的触发数量。

IFTRG[1:0]位（输入FIFO数据触发数）

IFTRG[1:0]位指定状态寄存器(SRCSTAT)中的IINT标志设置为1时的数据单元计数。当存储在输入FIFO中的数据单元数等于或小于指定的触发数时，IINT标志设置为1。

IEN位（输入FIFO空中断使能）

当输入FIFO中的数据单元数等于或小于IFTRG[1:0]位中指定的触发数时，IEN位启用或禁用输入FIFO空中断请求的发出，从而导致IINT标志状态寄存器(SRCSTAT)设置为1。

IED位（输入数据字节序）

IED位指定输入数据的字节序格式。

42.2.4 Output Data Control Register (SRCODCTRL)

Address(es): SRC.SRCODCTRL 4004 DFFAh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	OCH	OED	OEN	—	—	—	—	—	—	OFTRG[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	OFTRG[1:0]	Output FIFO Data Trigger Number	b1 b0 0 0: 1 0 1: 4 1 0: 8 1 1: 12.	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	OEN	Output FIFO Full Interrupt Enable	0: Disable output FIFO full interrupts 1: Enable output FIFO full interrupts.	R/W
b9	OED	Output Data Endian	0: Little endian 1: Big endian.	R/W
b10	OCH	Output Data Channel Exchange *1	0: Do not exchange channels (use same order as data input) 1: Exchange channels (use opposite order from data input).	R/W
b15 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Only rewrite this bit while the SRCCTRL.SRCEN bit is 0.

The SRCODCTRL register is a 16-bit read/write register that specifies whether to exchange the channels for the output data, specifies the endian format of output data, enables or disables the interrupt requests, and specifies the triggering number of data units.

OFTRG[1:0] bits (Output FIFO Data Trigger Number)

The OFTRG[1:0] bits specify the data unit count at which the OINT flag in the Status Register (SRCSTAT) sets to 1. When the number of data units in the output FIFO becomes equal to or greater than the specified triggering number, the OINT flag sets to 1.

OEN bit (Output FIFO Full Interrupt Enable)

The OEN bit enables or disables issuing of the output FIFO full interrupt request when the number of data units in the output FIFO becomes equal to or greater than the number specified in the OFTRG[1:0] bits, resulting in the OINT flag in the Status Register (SRCSTAT) setting to 1.

OED bit (Output Data Endian)

The OED bit specifies the endian format of the output data.

OCH bit (Output Data Channel Exchange)

The OCH bit specifies whether to exchange the channels for the Output Data Register (SRCOD). Do not set this bit to 1 when processing monaural data.

42.2.4 输出数据控制寄存器(SRCODCTRL)

Address(es): SRC.SRCODCTRL 4004 DFFAh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	OCH	OED	OEN	—	—	—	—	—	—	OFTRG[1:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b1, b0	OFTRG[1:0]	输出FIFO数据触发Number	b1 b0 0 0: 1 0 1: 4 1 0: 8 1 1: 12.	R/W
b7 to b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b8	OEN	输出FIFO满中断Enable	0：禁止输出FIFO满中断1：使能输出FIFO满中断。	R/W
b9	OED	输出数据字节序	0：小端1：大端。	R/W
b10	OCH	输出数据通道交换*1	0：不交换通道（使用与数据输入相同的顺序）1：交换通道（使用与数据输入相反的顺序）。	R/W
b15 to b11	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 仅在SRCCTRL.SRCEN位为0时重写该位。

SRCODCTRL寄存器是一个16位读写寄存器，指定是否为输出数据交换通道，指定输出数据的字节序格式，启用或禁用中断请求，并指定数据单元的触发数量。

OFTRG[1:0]位（输出FIFO数据触发数）

OFTRG[1:0]位指定状态寄存器(SRCSTAT)中的OINT标志设置为1的数据单元计数。
当输出FIFO中的数据单元数等于或大于指定的触发数时，
OINT标志设置为1。

OEN位（输出FIFO完全中断使能）

当输出FIFO中的数据单元数等于或大于OFTRG[1:0]位中指定的数量时，OEN位使能或禁止发出输出FIFO满中断请求，从而在状态寄存器(SRCSTAT)设置为1。

OED位（输出数据字节序）

OED位指定输出数据的字节序格式。

OCH位（输出数据通道交换）

OCH位指定是否为输出数据寄存器(SRCOD)交换通道。处理单声道数据时不要将此位设置为1。

42.2.5 Control Register (SRCCTRL)

Address(es): SRC.SRCCTRL 4004 DFFCh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	FICRAE	—	CEEN	SRCEN	UDEN	OVEN	FL	CL	IFS[3:0]				—	OFS[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	OFS[2:0]	Output Sampling Rate	b2 b0 0 0 0: 44.1 kHz 0 0 1: 48.0 kHz 0 1 0: 32.0 kHz 0 1 1: Setting prohibited 1 0 0: 8.0 kHz*1 1 0 1: 16.0 kHz.*1 Other settings are prohibited.	R/W
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b7 to b4	IFS[3:0]	Input Sampling Rate	b7 b4 0 0 0 0: 8.0 kHz 0 0 0 1: 11.025 kHz 0 0 1 0: 12.0 kHz 0 0 1 1: Setting prohibited 0 1 0 0: 16.0 kHz 0 1 0 1: 22.05 kHz 0 1 1 0: 24.0 kHz 0 1 1 1: Setting prohibited 1 0 0 0: 32.0 kHz 1 0 0 1: 44.1 kHz 1 0 1 0: 48.0 kHz. Other settings are prohibited.	R/W
b8	CL	Internal Work Memory Clear	Writing 1 to this bit clears the input FIFO, output FIFO, input buffer memory, intermediate memory, and accumulator.	R/W
b9	FL	Internal Work Memory Flush	Writing 1 to this bit starts conversion of the sampling rate for all data in the input FIFO, input buffer memory, and intermediate memory (flush processing).	R/W
b10	OVEN	Output FIFO Overflow Interrupt Enable	0: Disable output FIFO overflow interrupts 1: Enable output FIFO overflow interrupts.	R/W
b11	UDEN	Output FIFO Underflow Interrupt Enable	0: Disable output FIFO underflow interrupts 1: Enable output FIFO underflow interrupts.	R/W
b12	SRCEN	Module Enable	0: Disable SRC module operation 1: Enable SRC module operation.*2	R/W
b13	CEEN	Conversion End Interrupt Enable	0: Disable conversion end interrupts 1: Enable conversion end interrupts.	R/W
b14	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b15	FICRAE	Filter Coefficient Table Access Enable	0: Disable reads to and writes from filter coefficient table RAM 1: Enable reads to and writes from filter coefficient table RAM.	R/W

Note 1. Only valid when the IFS[3:0] bits are 1001b.
Note 2. When SRCEN = 1, do not change the settings of the following bits:
IED bit in SRCIDCTRL, OED and OCH bits in SRCODCTRL, OFS[2:0], IFS[3:0], and FICRAE bits in SRCCTRL.

The SRCCTRL register is a 16-bit read/write register that enables or disables access to the Filter Coefficient Table, module operations, and interrupt requests, and specifies flush processing, clear processing of the internal work memory, and the input and output sampling rates.

OFS[2:0] bits (Output Sampling Rate)

The OFS[2:0] bits specify the output sampling rate.

42.2.5 控制寄存器(SRCCTRL)

Address(es): SRC.SRCCTRL 4004 DFFCh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	FICRAE	—	CEEN	SRCEN	UDEN	OVEN	FL	CL	IFS[3:0]				—	OFS[2:0]		
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b2 to b0	OFS[2:0]	输出采样率	b2 b0 0 0 0: 44.1 kHz 0 0 1: 48.0 kHz 0 1 0: 32.0 kHz 0 1 1：禁止设置 1 0 0: 8.0 kHz*1 01：16.0kHz。*1禁止其他设置。	R/W
b3	—	Reserved	该位读取为0。写入值应为0。	R/W
b7 to b4	IFS[3:0]	输入采样率	b7 b4 0 0 0 0: 8.0 kHz 0 0 0 1: 11.025 kHz 0 0 1 0: 12.0 kHz 0 0 1 1：禁止设置 0 1 0 0: 16.0 kHz 0 1 0 1: 22.05 kHz 0 1 1 0: 24.0 kHz 0 1 1 1：禁止设置 1 0 0 0: 32.0 kHz 1 0 0 1: 44.1 kHz 10：48.0kHz。禁止其他设置。	R/W
b8	CL	内部工作记忆清除	向该位写入1将清除输入FIFO、输出FIFO、输入缓冲存储器、中间存储器和累加器。	R/W
b9	FL	内部工作记忆刷新	向该位写入1开始转换输入FIFO、输入缓冲存储器和中间存储器中所有数据的采样率（刷新处理）。	R/W
b10	OVEN	输出FIFO溢出中断Enable	0：禁止输出FIFO溢出中断1：使能输出FIFO溢出中断。	R/W
b11	UDEN	输出FIFO下溢中断Enable	0：禁止输出FIFO下溢中断1：使能输出FIFO下溢中断。	R/W
b12	SRCEN	模块启用	0：禁用SRC模块操作1：启用SRC模块操作。*2	R/W
b13	CEEN	转换结束中断Enable	0：禁止转换结束中断1：使能转换结束中断。	R/W
b14	—	Reserved	该位读取为0。写入值应为0。	R/W
b15	FICRAE	过滤系数表访问Enable	0：禁止对滤波器系数表RAM进行读写。1：允许对滤波器系数表RAM进行读写。	R/W

Note 1. 仅当IFS[3:0]位为1001b时有效。
Note 2. 当SRCEN=1时，请勿更改以下位的设置：
SRCIDCTRL中的IED位、SRCODCTRL中的OED和OCH位、SRCCTRL中的OFS[2:0]、IFS[3:0]和FICRAE位。

SRCCTRL寄存器是一个16位读写寄存器，用于启用或禁用对滤波器系数表的访问、模块操作和中断请求，并指定内部工作存储器的刷新处理、清除处理以及输入和输出采样率。

OFS[2:0]位（输出采样率）

OFS[2:0]位指定输出采样率。

IFS[3:0] bits (Input Sampling Rate)

The IFS[3:0] bits specify the input sampling rate.

CL bit (Internal Work Memory Clear)

Writing 1 to the CL bit clears the input FIFO, output FIFO, input buffer memory, intermediate buffer memory, and accumulator, and then the CL bit clears to 0. This bit is read as 0. Even if SRCEN = 0, writing 1 to this bit clears the processing.

FL bit (Internal Work Memory Flush)

Writing 1 to the FL bit initiates flush processing by starting conversion of the sampling rate of all the data in the input FIFO, input buffer memory, and intermediate memory. This bit is read as 0. When SRCEN = 0, writing 1 to this bit does not trigger flush processing.

In addition, when 1 is written to the FL bit while the number of data units in the input buffer memory is less than the values shown in Table 42.6, valid output data cannot be received. The internal work memory is cleared without triggering the flush processing.

OVEN bit (Output FIFO Overflow Interrupt Enable)

The OVEN bit enables or disables issuing of the output FIFO overflow interrupt request when the OVF flag in the Status Register (SRCSTAT) is set to 1.

When OVEN = 1: Conversion processing stops until the OVF flag is cleared by the CPU accessing SRCSTAT when the output FIFO overflow interrupt is generated. Writing of conversion results to the output FIFO also stops.

When OVEN = 0: The OVF flag automatically clears when the output FIFO has space, and conversion processing can be continued.

UDEN bit (Output FIFO Underflow Interrupt Enable)

The UDEN bit enables or disables issuing of the output FIFO underflow interrupt request when the output FIFO is read and the UDF flag in the Status Register (SRCSTAT) sets to 1 while the number of data units in the output FIFO is zero.

SRCEN bit (Module Enable)

The SRCEN bit enables or disables SRC operation. Writing 1 to these bits while SRCEN = 0 clears the internal work memory.

CEEN bit (Conversion End Interrupt Enable)

The CEEN bit enables or disables issuing of a conversion end interrupt request when the CEF flag in the Status Register (SRCSTAT) sets to 1 after flush processing is complete and all the output data is read.

FICRAE bit (Filter Coefficient Table Access Enable)

The FICRAE bit enables or disables access to the filter coefficient table RAM. After flush processing is complete, the number of output data units obtained as a result of conversion can be calculated using the following formulas:

$$\frac{\text{Number of output data units} - 1}{\text{Output sampling rate}} = \frac{\text{Number of input data units} \times n - 1}{\text{Input sampling rate} \times n}$$

$$\text{Number of output data units} = \left[(\text{Number of input data units} \times n - 1) \times \frac{\text{Output sampling rate}}{\text{Input sampling rate} \times n} \right] + 1$$

The value of n can be obtained from Table 42.4. The number of input data units must be equal to or greater than the values in Table 42.5.

IFS[3:0]位（输入采样率）

IFS[3:0]位指定输入采样率。

CL位（内部工作存储器清除）

向CL位写入1清除输入FIFO、输出FIFO、输入缓冲存储器、中间缓冲存储器和累加器，然后CL位清除为0。该位读为0。即使SRCEN=0，写入1到该位清除处理。

FL位（内部工作内存刷新）

将1写入FL位通过开始转换输入中所有数据的采样率来启动刷新处理
FIFO、输入缓冲存储器和中间存储器。该位读为0。当SRCEN=0时，向该位写入1不会触发刷新处理。

此外，当输入缓冲存储器中的数据单元数小于表42.6中所示的值时，当向FL位写入1时，将无法接收有效的输出数据。在不触发刷新处理的情况下清除内部工作内存。

OVEN位（输出FIFO溢出中断使能）

当状态中的OVF标志位时，OVEN位启用或禁用输出FIFO溢出中断请求的发出
寄存器(SRCSTAT)设置为1。

当OVEN=1时：转换处理停止，直到产生输出FIFO溢出中断时CPU访问SRCSTAT清除OVF标志。将转换结果写入输出FIFO也会停止。

当OVEN=0时：当输出FIFO有空间时，OVF标志自动清零，可以继续进行转换处理。

UDEN位（输出FIFO下溢中断使能）

当读取输出FIFO并且状态寄存器(SRCSTAT)中的UDF标志设置为1而输出FIFO中的数据单元数为零时，UDEN位启用或禁用输出FIFO下溢中断请求的发出。

SRCEN位（模块使能）

SRCEN位启用或禁用SRC操作。当SRCEN=0时向这些位写入1会清除内部工作存储器。

CEEN位（转换结束中断使能）

在刷新处理完成并读取所有输出数据后，当状态寄存器(SRCSTAT)中的CEF标志设置为1时，CEEN位允许或禁止发出转换结束中断请求。

FICRAE位（滤波器系数表访问使能）

FICRAE位启用或禁用对滤波器系数表RAM的访问。在flush处理完成后，转换后得到的输出数据单元个数可以用以下公式计算：

$$\frac{\text{输出数据单元数}-1}{\text{输出采样率}} = \frac{\text{输入数据单元数}\times n-1}{\text{输入采样率}\times n}$$

$$\text{输出数据单元数} = \left[(\text{输入数据单元数}\times n-1) \times \frac{\text{输出采样率}}{\text{输入采样率}\times n} \right] + 1$$

n的值可以从表42.4中获得。输入数据单元的数量必须等于或大于表42.5中的值。

Table 42.4 Sampling rate settings and value of n

OFS[2:0] setting (output sampling rate [kHz])	IFS[3:0] setting (input sampling rate [kHz])								
	0000b (8.0)	0001b (11.025)	0010b (12.0)	0100b (16.0)	0101b (22.05)	0110b (24.0)	1000b (32.0)	1001b (44.1)	1010b (48.0)
000b (44.1)	6	4	4	3	2	2	3	—	1
001b (48.0)	6	4	4	3	2	2	3	1	—
010b (32.0)	4	8	4	2	4	2	—	2	1
100b (8.0)	—	—	—	—	—	—	—	1	—
101b (16.0)	—	—	—	—	—	—	—	1	—

Conversion processing does not start, and so output data is not obtained, until the specified number of data units are input. The minimum number of input data units necessary for obtaining the first output data depends on the IFS and OFS bit settings. Table 42.5 shows the relation between the settings in the IFS and OFS bits and the number of initial input data required. Table 42.6 shows the relation between the settings in the IFS and OFS bits and the number of initial input data required for processing.

Table 42.5 Relation between sampling rate settings and number of initial input data units required

OFS[2:0] setting (output sampling rate [kHz])	IFS[3:0] setting (input sampling rate [kHz])								
	0000b (8.0)	0001b (11.025)	0010b (12.0)	0100b (16.0)	0101b (22.05)	0110b (24.0)	1000b (32.0)	1001b (44.1)	1010b (48.0)
000b (44.1)	38	40	40	43	48	48	43	—	63
001b (48.0)	38	40	40	43	48	48	43	32	—
010b (32.0)	40	37	40	48	40	48	—	48	63
100b (8.0)	—	—	—	—	—	—	—	63	—
101b (16.0)	—	—	—	—	—	—	—	63	—

Table 42.6 Relation between sampling rate settings and number of input data units required for flush processing

OFS[2:0] setting (output sampling rate [kHz])	IFS[3:0] setting (input sampling rate [kHz])								
	0000b (8.0)	0001b (11.025)	0010b (12.0)	0100b (16.0)	0101b (22.05)	0110b (24.0)	1000b (32.0)	1001b (44.1)	1010b (48.0)
000b (44.1)	27	24	24	22	16	16	22	—	1
001b (48.0)	27	24	24	22	16	16	22	32	—
010b (32.0)	24	29	24	16	24	16	—	16	1
100b (8.0)	—	—	—	—	—	—	—	1	—
101b (16.0)	—	—	—	—	—	—	—	1	—

Table 42.4 采样率设置和n值

OFS[2:0]设置（输出采样率[kHz]）	IFS[3:0]设置（输入采样率[kHz]）								
	0000b (8.0)	0001b (11.025)	0010b (12.0)	0100b (16.0)	0101b (22.05)	0110b (24.0)	1000b (32.0)	1001b (44.1)	1010b (48.0)
000b (44.1)	6	4	4	3	2	2	3	—	1
001b (48.0)	6	4	4	3	2	2	3	1	—
010b (32.0)	4	8	4	2	4	2	—	2	1
100b (8.0)	—	—	—	—	—	—	—	1	—
101b (16.0)	—	—	—	—	—	—	—	1	—

转换处理不会开始，因此不会获得输出数据，直到输入指定数量的数据单元。获得第一个输出数据所需的输入数据单元的最小数量取决于IFS和OFS位设置。表42.5显示了IFS和OFS位的设置与所需的初始输入数据数量之间的关系。表42.6显示了IFS和OFS位的设置与处理所需的初始输入数据数量之间的关系。

Table 42.5 采样率设置与所需的初始输入数据单元数之间的关系

OFS[2:0]设置（输出采样率[kHz]）	IFS[3:0]设置（输入采样率[kHz]）								
	0000b (8.0)	0001b (11.025)	0010b (12.0)	0100b (16.0)	0101b (22.05)	0110b (24.0)	1000b (32.0)	1001b (44.1)	1010b (48.0)
000b (44.1)	38	40	40	43	48	48	43	—	63
001b (48.0)	38	40	40	43	48	48	43	32	—
010b (32.0)	40	37	40	48	40	48	—	48	63
100b (8.0)	—	—	—	—	—	—	—	63	—
101b (16.0)	—	—	—	—	—	—	—	63	—

Table 42.6 采样率设置与刷新处理所需的输入数据单元数之间的关系

OFS[2:0]设置（输出采样率[kHz]）	IFS[3:0]设置（输入采样率[kHz]）								
	0000b (8.0)	0001b (11.025)	0010b (12.0)	0100b (16.0)	0101b (22.05)	0110b (24.0)	1000b (32.0)	1001b (44.1)	1010b (48.0)
000b (44.1)	27	24	24	22	16	16	22	—	1
001b (48.0)	27	24	24	22	16	16	22	32	—
010b (32.0)	24	29	24	16	24	16	—	16	1
100b (8.0)	—	—	—	—	—	—	—	1	—
101b (16.0)	—	—	—	—	—	—	—	1	—

42.2.6 Status Register (SRCSTAT)

Address(es): SRC.SRCSTAT 4004 DFFEh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	OFDN[4:0]					IFDN[3:0]				—	CEF	FLF	UDF	OVF	IINT	OINT
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bit	Symbol	Bit name	Description	R/W
b0	OINT	Output FIFO Full Interrupt Request Flag	0: Number of data units in output FIFO has not become equal to or greater than specified triggering number 1: Number of data units in output FIFO has become equal to or greater than specified triggering number.	R/(W) *1
b1	IINT	Input FIFO Empty Interrupt Request Flag	0: Number of data units in input FIFO has not become equal to or smaller than specified triggering number 1: Number of data units in input FIFO has become equal to or smaller than specified triggering number.	R/(W) *1
b2	OVF	Output FIFO Overflow Interrupt Request Flag	0: No output FIFO overflow occurred 1: Output FIFO overflow occurred.	R/(W) *1
b3	UDF	Output FIFO Underflow Interrupt Request Flag	0: No output FIFO underflow occurred 1: Output FIFO underflow occurred.	R/(W) *1
b4	FLF	Flush Processing Status Flag	0: Flush processing complete 1: Flush processing in progress.	R
b5	CEF	Conversion End Flag	0: Not all output data read 1: All output data read.	R/(W) *1
b6	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b10 to b7	IFDN[3:0]	Input FIFO Data Count	Indicates the number of data units in the input FIFO.	R
b15 to b11	OFDN[4:0]	Output FIFO Data Count	Indicates the number of data units in the output FIFO.	R

Note 1. Only 0 can be written after having read as 1.

The SRCSTAT register is a 16-bit read/write register that indicates the number of data units in the input and output FIFOs, whether the various interrupt sources were generated, and the flush processing status.

OINT flag (Output FIFO Full Interrupt Request Flag)

The OINT flag indicates that the number of data units in the output FIFO has become equal to or greater than the triggering number specified in the OFTRG[1:0] bits in the Output Data Control Register (SRCODCTRL).

[Setting condition]

- When the number of data units in the output FIFO becomes equal to or greater than the specified triggering number.

[Clearing conditions]

- Writing 0 to the OINT flag after reading it as 1
- When the last DMA transfer is executed
- Writing 1 to the SRCCTRL.CL bit
- Writing 1 to the SRCCTRL.SRCEN bit while it is 0.

IINT flag (Input FIFO Empty Interrupt Request Flag)

The IINT flag indicates that the number of data units in the input FIFO has become equal to or smaller than the triggering number specified in the IFTRG[1:0] bits in the Input Data Control Register (SRCIDCTRL).

[Setting conditions]

- When the number of data units in the input FIFO becomes equal to or smaller than the specified triggering number

42.2.6 状态寄存器(SRCSTAT)

Address(es): SRC.SRCSTAT 4004 DFFEh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	OFDN[4:0]					IFDN[3:0]				—	CEF	FLF	UDF	OVF	IINT	OINT
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bit	Symbol	位名称	Description	R/W
b0	OINT	输出FIFO满中断请求标志	0：输出FIFO中的数据单元数未等于或大于指定的触发数1：输出FIFO中的数据单元数已等于或大于指定的触发数。	R/(W) *1
b1	IINT	输入FIFO空中断请求标志	0：输入FIFO中的数据单元数未等于或小于指定的触发数1：输入FIFO中的数据单元数已等于或小于指定的触发数。	R/(W) *1
b2	OVF	输出FIFO溢出中断请求标志	0：未发生输出FIFO溢出1：发生输出FIFO溢出。	R/(W) *1
b3	UDF	输出FIFO下溢中断请求标志	0：未发生输出FIFO下溢1：发生输出FIFO下溢。	R/(W) *1
b4	FLF	刷新处理状态标志	0：冲洗处理完成1：冲洗处理中。	R
b5	CEF	转换结束标志	0：不读取所有输出数据1：读取所有输出数据。	R/(W) *1
b6	—	Reserved	该位读取为0。写入值应为0。	R/W
b10 to b7	IFDN[3:0]	输入FIFO数据计数	指示输入FIFO中的数据单元数。	R
b15 to b11	OFDN[4:0]	输出FIFO数据计数	指示输出FIFO中的数据单元数。	R

Note 1. 读为1后只能写0。

SRCSTAT寄存器是一个16位读写寄存器，指示输入和输出中数据单元的数量FIFO，是否产生了各种中断源，以及刷新处理状态。

OINT标志（输出FIFO满中断请求标志）

OINT标志表示输出FIFO中的数据单元数已等于或大于输出数据控制寄存器(SRCODCTRL)中的OFTRG[1:0]位中指定的触发数。

[Setting condition]

- 当输出FIFO中的数据单元数等于或大于指定的触发数时。

[Clearing conditions]

- 读取为1后将0写入OINT标志
- 执行最后一次DMA传输时
- 将1写入SRCCTRL.CL位
- SRCCTRL.SRCEN位为0时写入1。

IINT标志（输入FIFO空中断请求标志）

IINT标志表示输入FIFO中的数据单元数已等于或小于输入数据控制寄存器(SRCIDCTRL)中IFTRG[1:0]位中指定的触发数。

[Setting conditions]

- 当输入FIFO中的数据单元数等于或小于指定触发数时

- Writing 1 to the SRCCTRL.CL bit
- Writing 1 to the SRCCTRL.SRCEN bit while it is 0.

[Clearing conditions]

- Writing 0 to the IINT flag after reading is as 1
- When the last DMA transfer is executed.

OVF flag (Output FIFO Overflow Interrupt Request Flag)

The OVF flag indicates that the sampling rate conversion for the next data completes when the output FIFO is full. The conversion stops until the OVF flag is cleared.

[Setting condition]

- When the sampling rate conversion for the next data completes when the output FIFO is full.

[Clearing conditions]

- Writing 0 to the OVF flag after reading it as 1 while the SRCCTRL.OVEN bit is 1
- When the number of data units in the output FIFO decreases after reading SRCOD while the SRCCTRL.OVEN bit is 0
- Writing 1 to the SRCCTRL.CL bit
- Writing 1 to the SRCCTRL.SRCEN bit while it is 0.

UDF flag (Output FIFO Underflow Interrupt Request Flag)

The UDF flag indicates that the output FIFO is read when the number of data units in the output FIFO is zero.

[Setting condition]

- When the output FIFO is read while the number of data units in the output FIFO is zero.

[Clearing conditions]

- Writing 0 to the UDF flag after reading it as 1
- Writing 1 to the SRCCTRL.CL bit
- Writing 1 to the SRCCTRL.SRCEN bit while it is 0.

FLF flag (Flush Processing Status Flag)

The FLF flag indicates whether flush processing is in progress or not.

[Setting condition]

- Writing 1 to the SRCCTRL.FL bit
  (When flush processing is not in progress, however, FLF does not set to 1.)

[Clearing conditions]

- When flush processing completes
- Writing 1 to the SRCCTRL.CL bit
- Writing 1 to the SRCCTRL.SRCEN bit while it is 0.

CEF flag (Conversion End Flag)

The CEF flag indicates that all the output data is read after flush processing completes.

[Setting condition]

- When the number of data units in the output FIFO is zero on completion of flush processing.

[Clearing conditions]

- Writing 0 to the CEF flag after reading it as 1.

- 将1写入SRCCTRL.CL位
- SRCCTRL.SRCEN位为0时写入1。

[Clearing conditions]

- 读取后向IINT标志写入0为1
- 执行最后一次DMA传输时。

OVF标志（输出FIFO溢出中断请求标志）

OVF标志表示当输出FIFO已满时，下一个数据的采样率转换完成。转换停止，直到OVF标志被清除。

[Setting condition]

- 当输出FIFO已满时，下一个数据的采样率转换完成。

[Clearing conditions]

- 在SRCCTRL.OVEN位为1时将OVF标志读取为1后写入0
- 当SRCCTRL.OVEN位为0时读取SRCOD后输出FIFO中的数据单元数减少
- 将1写入SRCCTRL.CL位
- SRCCTRL.SRCEN位为0时写入1。

UDF标志（输出FIFO下溢中断请求标志）

UDF标志表示当输出FIFO中的数据单元数为零时读取输出FIFO。

[Setting condition]

- 当输出FIFO中的数据单元数为零时读取输出FIFO。

[Clearing conditions]

- 读为1后将0写入UDF标志
- 将1写入SRCCTRL.CL位
- SRCCTRL.SRCEN位为0时写入1。

FLF标志（刷新处理状态标志）

FLF标志指示刷新处理是否正在进行。

[Setting condition]

- 将1写入SRCCTRL.FL位（但是，当未进行刷新处理时，FLF不会设置为1。）

[Clearing conditions]

- 刷新处理完成时
- 将1写入SRCCTRL.CL位
- SRCCTRL.SRCEN位为0时写入1。

CEF标志（转换结束标志）

CEF标志指示在刷新处理完成后读取所有输出数据。

[Setting condition]

- 当刷新处理完成时输出FIFO中的数据单元数为零时。

[Clearing conditions]

- 读为1后将0写入CEF标志。

- Writing 1 to the SRCCTRL.CL bit
- Writing 1 to the SRCCTRL.SRCEN bit while it is 0.

IFDN[3:0] bits (Input FIFO Data Count)

The IFDN[3:0] bits indicate the number of data units in the input FIFO.

OFDN[4:0] bits (Output FIFO Data Count)

The OFDN[4:0] bits indicate the number of data units in the output FIFO.

42.2.7 Filter Coefficient Table n (SRCFCTRn) (n = 0 to 5551)

Address(es): SRCRAM.SRCFCTR0 to 5551 4004 8000h to 4004 D6BFh

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	SRCFCOE[21:16]					
Value after reset:	0	0	0	0	0	0	0	0	0	0	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SRCFCOE[15:0]															
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b21 to b0	SRCFCOE[21:0]	Filter Coefficient Table	Stores the filter coefficient value.	R/W
b31 to b22	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

SRCFCTR0 to SRCFCTR5551 are 32-bit read/write SRAM modules that store the filter coefficients to be used for sampling rate conversion. This SRAM can be read from and written to through the peripheral bus only when the FICRAE bit is 1 and the SRCEN bit is 0 in SRCCTRL. Bits 31 to 22 are reserved and are read as 0, and their write values should be 0. Bits 21 to 0 are used for storage of the filter coefficient values, whose initial values are undefined.

42.3 Operation

42.3.1 Initial Settings

Figure 42.2 shows an example flow for the initial settings. After the module-stop state is released, the filter coefficient data stored in the flash and other areas must be transferred to the Filter Coefficient Table (SRCFCTR) before SRC conversion starts. When a filter coefficient value is already stored in the Filter Coefficient Table, skip this transfer and set the required parameters to start the conversion.

- 将1写入SRCCTRL.CL位
- SRCCTRL.SRCEN位为0时写入1。

IFDN[3:0]位（输入FIFO数据计数）

IFDN[3:0]位指示输入FIFO中数据单元的数量。

OFDN[4:0]位（输出FIFO数据计数）

OFDN[4:0]位指示输出FIFO中数据单元的数量。

42.2.7 滤波器系数表n(SRCFCTRn)（n=0至5551）

Address(es): SRCRAM.SRCFCTR0 to 5551 4004 8000h to 4004 D6BFh

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	SRCFCOE[21:16]					
重置后的值：	0	0	0	0	0	0	0	0	0	0	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	SRCFCOE[15:0]															
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

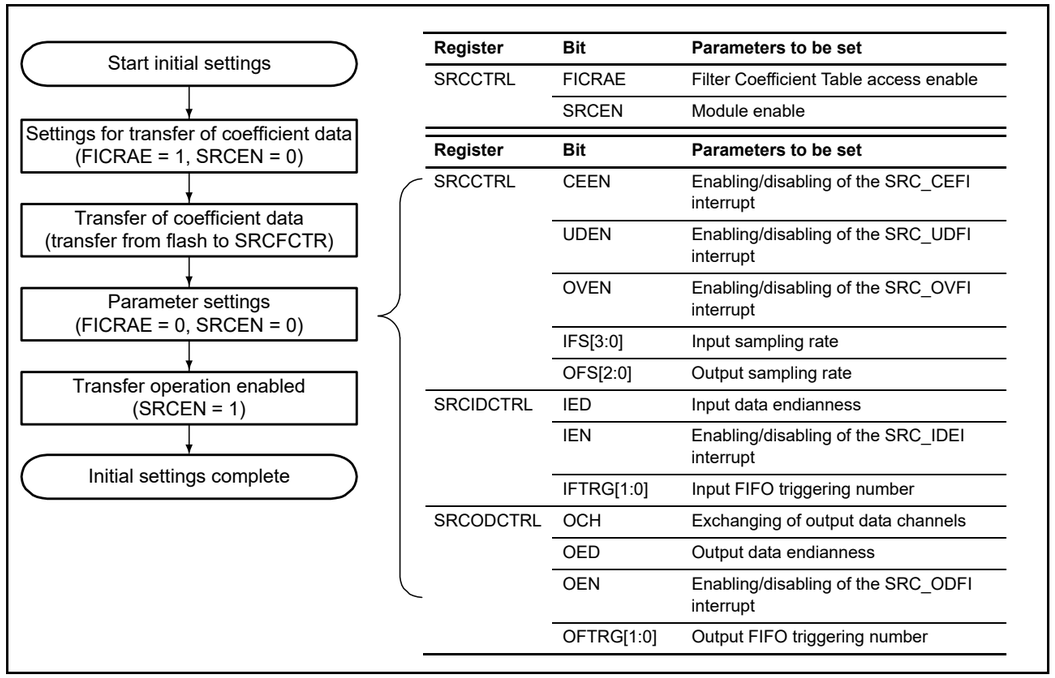
Bit	Symbol	位名称	Description	R/W
b21 to b0	SRCFCOE[21:0]	过滤系数表	存储滤波器系数值。	R/W
b31 to b22	—	Reserved	这些位被读取为0。写入值应为0。	R/W

SRCFCTR0至SRCFCTR5551是32位读写SRAM模块，用于存储用于采样率转换的滤波器系数。只有当SRCCTRL中的FICRAE位为1且SRCEN位为0时，该SRAM才能通过外设总线读写。第31到22位保留，读为0，写入值应为0。第21到0位用于存储滤波器系数值，初始值未定义。

42.3 Operation

42.3.1 初始设置

图42.2显示了初始设置的示例流程。模块停止状态释放后，存储在闪存和其他区域的滤波器系数数据必须在SRC转换开始前传输到滤波器系数表(SRCFCTR)。当滤波器系数值已经存储在滤波器系数表中时，跳过此传输并设置所需的参数以开始转换。



Register	Bit	Parameters to be set
SRCCTRL	FICRAE	Filter Coefficient Table access enable
	SRCEN	Module enable

Register	Bit	Parameters to be set
SRCCTRL	CEEN	Enabling/disabling of the SRC_CEFI interrupt
	UDEN	Enabling/disabling of the SRC_UDFI interrupt
	OVEN	Enabling/disabling of the SRC_OVFI interrupt
	IFS[3:0]	Input sampling rate
	OFS[2:0]	Output sampling rate
SRCIDCTRL	IED	Input data endianness
	IEN	Enabling/disabling of the SRC_IDEI interrupt
	IFTRG[1:0]	Input FIFO triggering number
SRCODCTRL	OCH	Exchanging of output data channels
	OED	Output data endianness
	OEN	Enabling/disabling of the SRC_ODFI interrupt
	OFTRG[1:0]	Output FIFO triggering number

Figure 42.2 Example flow for initial settings

42.3.2 Data Input

Figure 42.3 shows an example flow for data input.

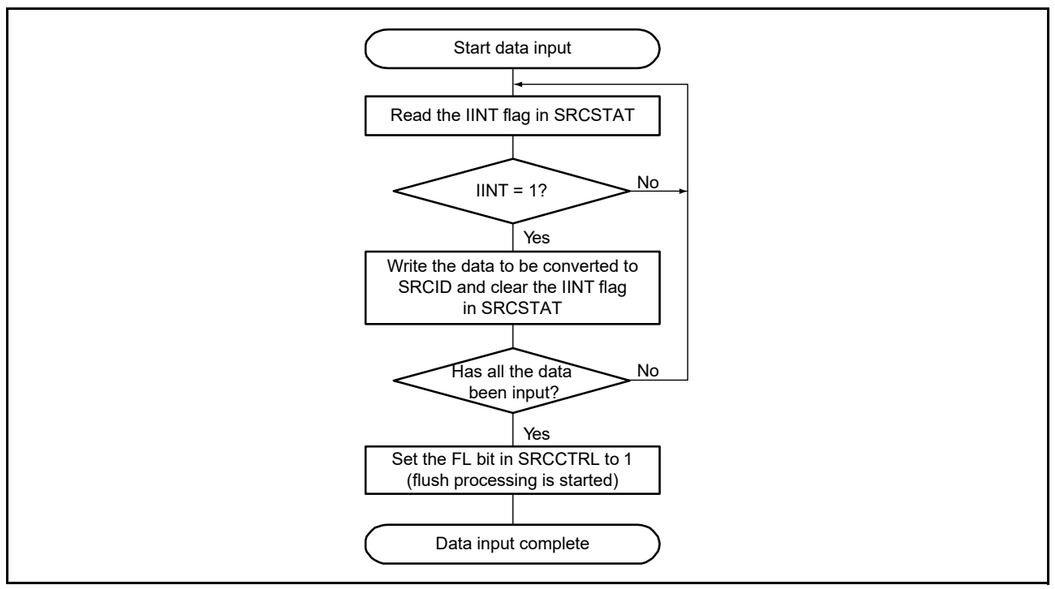
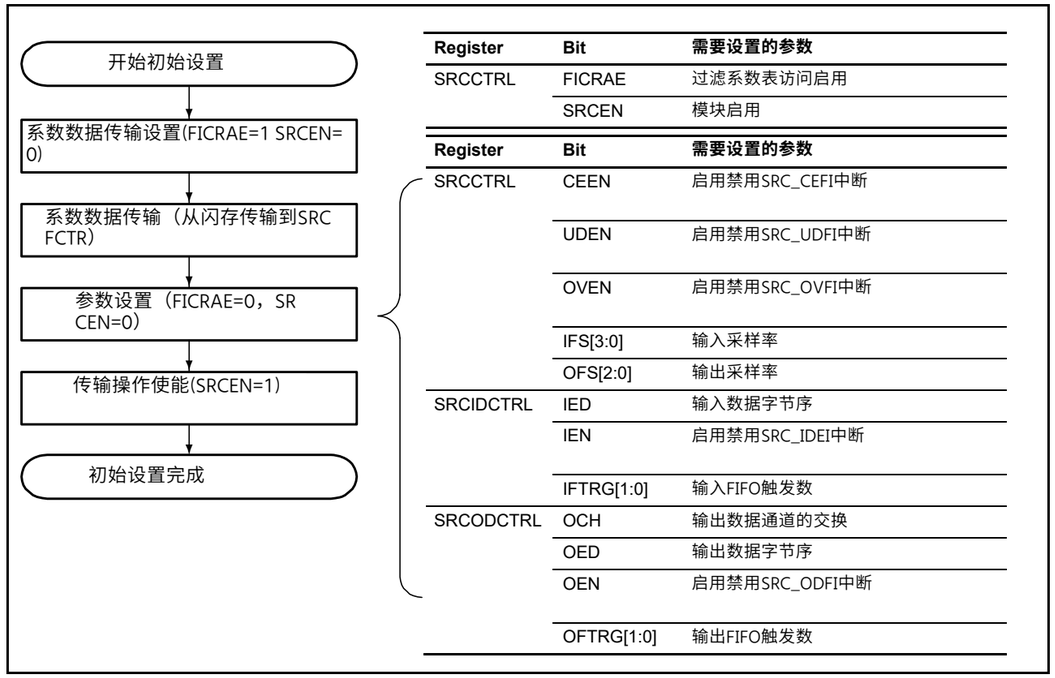


Figure 42.3 Data input flow



Register	Bit	需要设置的参数
SRCCTRL	FICRAE	过滤系数表访问启用
	SRCEN	模块启用

Register	Bit	需要设置的参数
SRCCTRL	CEEN	启用禁用SRC_CEFI中断
	UDEN	启用禁用SRC_UDFI中断
	OVEN	启用禁用SRC_OVFI中断
	IFS[3:0]	输入采样率
	OFS[2:0]	输出采样率
SRCIDCTRL	IED	输入数据字节序
	IEN	启用禁用SRC_IDEI中断
	IFTRG[1:0]	输入FIFO触发数
SRCODCTRL	OCH	输出数据通道的交换
	OED	输出数据字节序
	OEN	启用禁用SRC_ODFI中断
	OFTRG[1:0]	输出FIFO触发数

Figure 42.2 初始设置的示例流程

42.3.2 数据输入

图42.3显示了数据输入的示例流程。

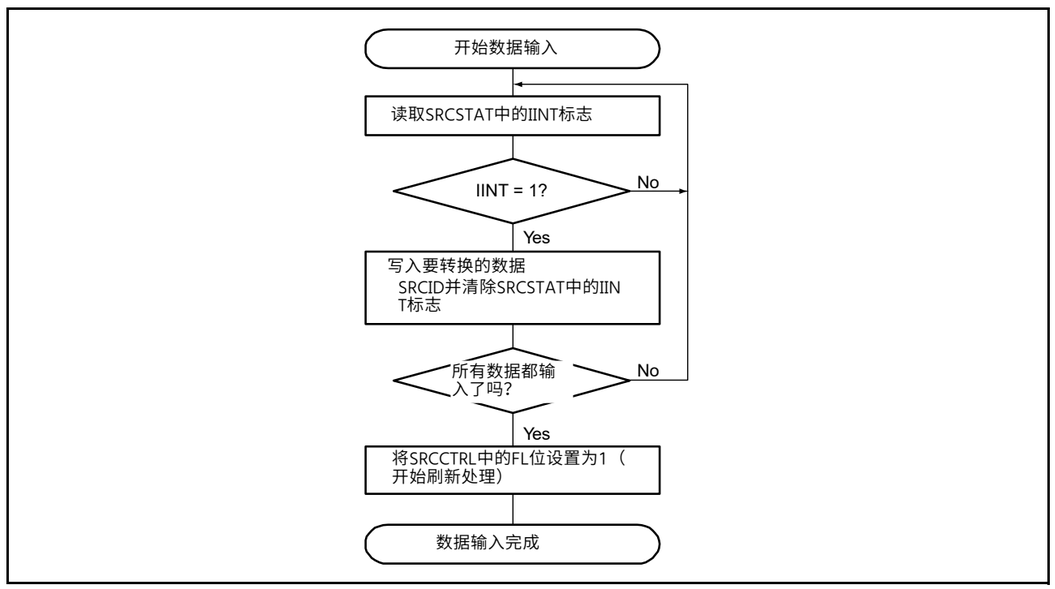


Figure 42.3 数据输入流程

(1) When issuing interrupts to the CPU

1. Set the IEN bit in SRCIDCTRL to 1.
2. When the IINT flag in SRCSTAT sets to 1, the IDEI interrupt request is issued. In the interrupt processing routine, read the IINT flag and confirm that it is 1, write data to SRCID, and write 0 to the IINT flag. Then return from the interrupt processing routine.
3. Repeat step 2 until all the data is input, and write 1 to the FL bit in SRCCTRL.

(2) When using interrupts to activate the DMAC

1. Assign the SRC_IDEI interrupt of the SRC to one channel of the DMAC.
2. Set the IEN bit in SRCIDCTRL to 1.
3. When the IINT flag in SRCSTAT sets to 1, the SRC_IDEI interrupt request is issued, activating the DMAC. When data is written to the SRCID register using DMA transfer, and when the number of data units in the input FIFO exceeds the triggering number specified in the IFTRG[1:0] bits in SRCIDCTRL, the IINT flag in SRCSTAT clears to 0.
4. Repeat step 3 until all the data is input, and write 1 to the FL bit in SRCCTRL.

(3) When using SSIE interface interrupts to activate the DMAC to transfer input data from the SSIE interface

1. Assign the SSIE interface to one channel of the DMAC as a DMA transfer request source. Set SSIFRDR of the SSIE interface as a transfer source and SRCID of the SRC as a transfer destination, and set the SSIE interface to enable reception operation.
2. When the RDF bit in SSIFSR sets to 1, the SSIE interface issues an interrupt request, activating the DMAC. The DMAC then reads data from SSIFRDR and writes the data to SRCID.
3. Repeat step 2 until all the data is input, and write 1 to the FL bit in SRCCTRL.

Note: The input FIFO has eight stages. The number of data units that can be transferred (the empty space in the FIFO) when an SRC_IDEI interrupt request is issued depends on the settings in the IFTRG[1:0] bits in SRCIDCTRL. Because the input FIFO is not equipped with a function to prevent or detect overflow, the transferred data is destroyed when overflow occurs. To prevent this, take the settings in the IFTRG[1:0] bits in SRCCTRL into consideration when setting the number of data units to be continuously transferred by the DMA.

42.3.3 Data Output

Figure 42.4 shows an example flow for data output.

(1) 向CPU发出中断时

1. 将SRCIDCTRL中的IEN位设置为1。
2. 当SRCSTAT中的IINT标志设置为1时，会发出IDEI中断请求。在中断处理程序中，读取IINT标志并确认为1，将数据写入SRCID，将0写入IINT标志。然后从中断处理程序返回。
3. 重复步骤2直到输入所有数据，然后将1写入SRCCTRL中的FL位。

(2) 使用中断激活DMAC时

1. 将SRC的SRC_IDEI中断分配给DMAC的一个通道。
2. 将SRCIDCTRL中的IEN位设置为1。
3. 当SRCSTAT中的IINT标志设置为1时，发出SRC_IDEI中断请求，激活DMAC。当使用DMA传输将数据写入SRCID寄存器时，并且当输入FIFO中的数据单元数超过SRCIDCTRL中的IFTRG[1:0]位中指定的触发数时，SRCSTAT中的IINT标志清零。
4. 重复步骤3直到输入所有数据，然后将1写入SRCCTRL中的FL位。

(3) 当使用SSIE接口中断激活DMAC以从SSIE interface

1. 将SSIE接口分配给DMAC的一个通道作为DMA传输请求源。将SSIE接口的SSIFRDR设置为传输源，将SRC的SRCID设置为传输目标，并设置SSIE接口使能接收操作。
2. 当SSIFSR中的RDF位设置为1时，SSIE接口发出中断请求，激活DMAC。这然后DMAC从SSIFRDR读取数据并将数据写入SRCID。
3. 重复步骤2直到输入所有数据，然后将1写入SRCCTRL中的FL位。

Note: 输入FIFO有8个阶段。发出SRC_IDEI中断请求时可传输的数据单元数（FIFO中的空白空间）取决于SRCIDCTRL中IFTRG[1:0]位的设置。由于输入FIFO没有配备防止或检测溢出的功能，所以当溢出发生时，传输的数据会被破坏。为防止这种情况，在设置DMA连续传输的数据单元数时，请考虑SRCCTRL中IFTRG[1:0]位的设置。

42.3.3 数据输出

图42.4显示了数据输出的示例流程。

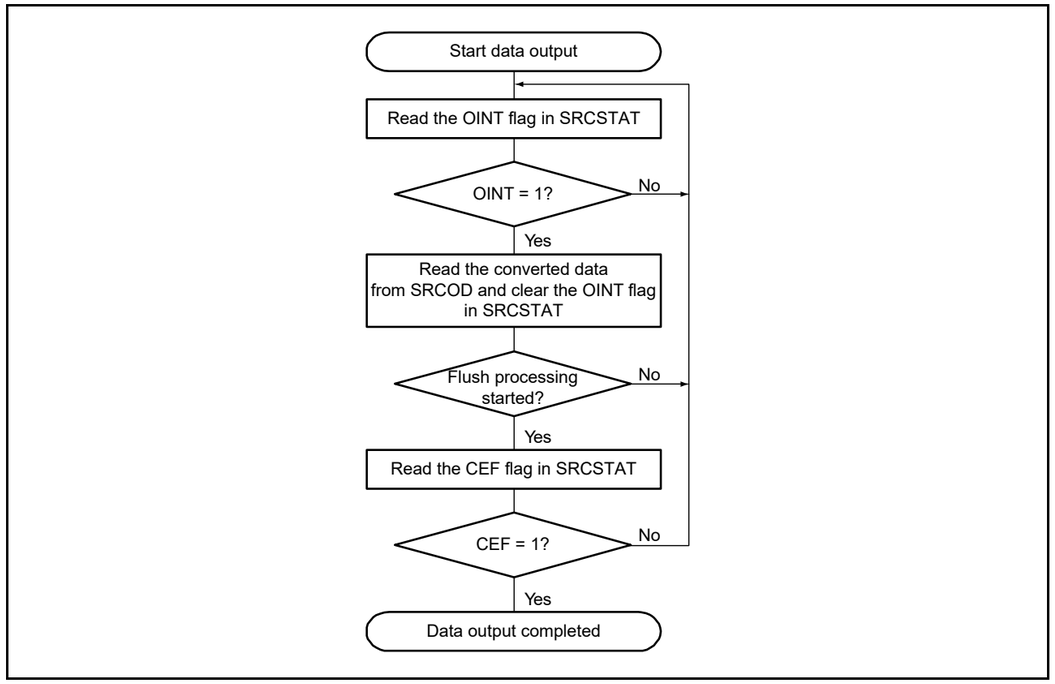


Figure 42.4 Data output flow

(1) When issuing interrupts to the CPU

1. Set the OEN bit in SRCODCTRL to 1.
2. When the OINT flag in SRCSTAT sets to 1, the SRC_ODFI interrupt request is issued. In the interrupt processing routine, read the OINT flag and confirm that it is 1, read data from SRCOD, and write 0 to the OINT flag. Then return from the interrupt processing routine.
3. After flush processing starts, repeat step 2 until the CEF flag in SRCSTAT is read as 1.

(2) When using interrupts to activate the DMAC

1. Assign the SRC_ODFI interrupt of the SRC to one channel of the DMAC.
2. Set the OEN bit in SRCODCTRL to 1.
3. When the OINT flag in SRCSTAT sets to 1, the SRC_ODFI interrupt request is issued, activating the DMAC. When data is read from SRCOD using DMA transfer, and when the number of data units in the output data FIFO becomes equal to or less than the triggering number specified in the OFTRG[1:0] bits, the OINT flag in SRCSTAT clears to 0.
4. After flush processing starts, repeat step 3 until the FLF flag in SRCSTAT is read as 0.

(3) When using SSIE interface interrupts to activate the DMAC to transfer output data to the SSIE interface

1. Set the OVEN bit in SRCCTRL to 0 to disable SRC_OVFI interrupt request generation.
2. Assign the SSIE interface to one channel of the DMAC as a DMA transfer request source. Set SRCID of the SRC as a transfer source and SSIFTDR of the SSIE interface as a transfer destination, and set the SSIE interface to enable transmission operation.
3. When the TDE bit in SSIFSR sets to 1, the SSIE interface issues an interrupt request, activating the DMAC. The DMAC then reads data from SRCOD and writes the data to SSIFTDR.

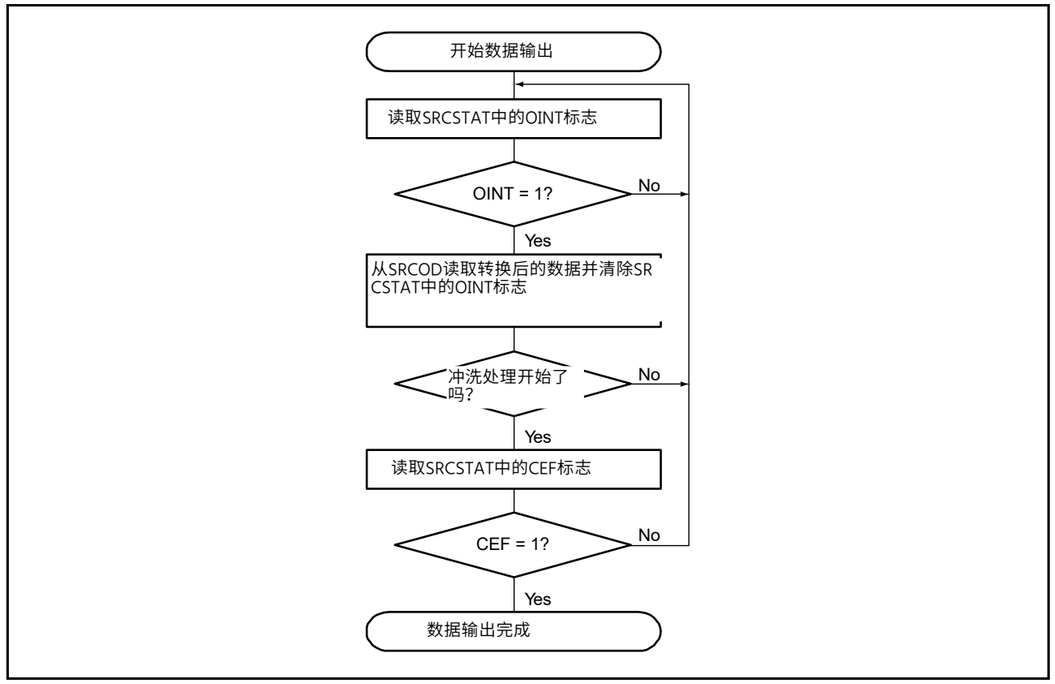


Figure 42.4 数据输出流

(1) 向CPU发出中断时

1. 将SRCODCTRL中的OEN位设置为1。
2. 当SRCSTAT中的OINT标志设置为1时，发出SRC_ODFI中断请求。在中断处理程序中，读取OINT标志并确认其为1，从SRCOD读取数据，并将0写入OINT标志。然后从中断处理程序返回。
3. 刷新处理开始后，重复步骤2，直到SRCSTAT中的CEF标志被读取为1。

(2) 使用中断激活DMAC时

1. 将SRC的SRC_ODFI中断分配给DMAC的一个通道。
2. 将SRCODCTRL中的OEN位设置为1。
3. 当SRCSTAT中的OINT标志设置为1时，发出SRC_ODFI中断请求，激活DMAC。当使用DMA传输从SRCOD读取数据时，当输出数据FIFO中的数据单元数等于或小于OFTRG[1:0]位中指定的触发数时，SRCSTAT中的OINT标志清零.
4. 刷新处理开始后，重复步骤3，直到SRCSTAT中的FLF标志被读取为0。

(3) 当使用SSIE接口中断激活DMAC以将输出数据传输到SSIE接口时

1. 将SRCCTRL中的OVEN位设置为0以禁用SRC_OVFI中断请求生成。
2. 将SSIE接口分配给DMAC的一个通道作为DMA传输请求源。将SRC的SRCID设置为传输源，将SSIE接口的SSIFTDR设置为传输目标，并设置SSIE接口使能传输操作。
3. 当SSIFSR中的TDE位设置为1时，SSIE接口发出中断请求，激活DMAC。这然后DMAC从SRCOD读取数据并将数据写入SSIFTDR。

4. After flush processing starts, repeat step 3 until the CEF flag in SRCSTAT is read as 1.

Note 1. The output FIFO has 16 stages. The conversion stops when no data is read and an overflow occurs in the output FIFO. Even in an overflow state, data can be read from the output FIFO, but the procedure to restart conversion might be required depending on the settings. (For details, see the OVEN bit in SRCCTRL.)

Note 2. When the number of data units in the output FIFO is zero, incorrect data is read. To prevent this, take the settings of the OFTRG[1:0] bits into consideration when setting the number of data units to be continuously transferred by the DMAC.

42.4 Interrupts

The SRC interrupt sources include:

- Input FIFO empty (SRC_IDEI)
- Output FIFO full (SRC_ODFI)
- Output FIFO overflow (SRC_OVFI)
- Output FIFO underflow (SRC_UDFI)
- Conversion end (SRC_CEFI).

Table 42.7 lists the interrupt request types and generation conditions.

Table 42.7 Interrupt requests and generation conditions

Interrupt request	Abbreviation	Interrupt condition	DMAC activation
Input FIFO empty	SRC_IDEI	IINT = 1, IEN = 1, and SRCEN = 1	Possible
Output FIFO full	SRC_ODFI	OINT = 1, OEN = 1, and SRCEN = 1	Possible
Output FIFO overflow	SRC_OVFI	OVF = 1, OVEN = 1, and SRCEN = 1	Not possible
Output FIFO underflow	SRC_UDFI	UDF = 1, UDEN = 1, and SRCEN = 1	Not possible
Conversion end	SRC_CEFI	CEF = 1, CEEN = 1, and SRCEN = 1	Not possible

When an interrupt condition is satisfied, the CPU executes the interrupt exception handling routine. Clear the interrupt source flags during this routine.

The SRC_IDEI and SRC_ODFI interrupts can activate the DMAC. If the DMAC is activated, the interrupts from the SRC are not sent to the CPU.

Do not clear the IINT and OINT flags through a write by the CPU (writing 0 after reading 1) during the DMA transfer.

42.5 Usage Notes

42.5.1 Notes on Accessing Registers

The following writes to SRCCTRL require 3 cycles of the peripheral clock (PCLKB) for the values to be updated in SRCSTAT:

- Writes of 1 to the FL bit in SRCCTRL, for the FLF flag in SRCSTAT to set
- Writes of 1 to the CL bit in SRCCTRL, for each bit in SRCSTAT to initialize
- Writes of 1 to the SRCEN bit in SRCCTRL while the SRCEN bit is 0, for each bit in SRCSTAT to initialized.

However, because the CPU executes any subsequent instruction without waiting for the completion of writes to a register, the updated state of SRCSTAT cannot be correctly read by an instruction immediately after the write instruction to SRCCTRL. To check the updated state of SRCSTAT, perform a dummy read of SRCCTRL or SRCSTAT after the instruction used to write to SRCCTRL.

42.5.2 Notes on Flush Processing

When 1 is written to the FL bit in the SRC Control Register (SRCCTRL), the SRC continues conversion processing by adding 0-data to the input data endpoint. Because of this, only execute flush processing when the audio data endpoint is

4. 刷新处理开始后，重复步骤3，直到SRCSTAT中的CEF标志被读取为1。

注1.输出FIFO有16个阶段。当没有数据被读取并且在输出中发生溢出时转换停止
先进先出。即使在溢出状态下，也可以从输出FIFO中读取数据，但根据设置，可能需要重新启动转换的过程。（详见SRCCTRL中的OVEN位。）注2.当输出FIFO中的数据单元数为零时，读取的数据不正确。为防止这种情况，在设置DMAC连续传输的数据单元数时，请考虑OFTRG[1:0]位的设置。

42.4 Interrupts

SRC中断源包括：

- 输入FIFO为空(SRC_IDEI)
- 输出FIFO已满(SRC_ODFI)
- 输出FIFO溢出(SRC_OVFI)
- Output FIFO underflow (SRC_UDFI)
- 转换结束(SRC_CEFI)。

表42.7列出了中断请求类型和产生条件。

Table 42.7 中断请求和生成条件

中断请求	Abbreviation	中断条件	DMAC activation
输入FIFO为空	SRC_IDEI	IINT = 1, IEN = 1, and SRCEN = 1	Possible
输出FIFO已满	SRC_ODFI	OINT=1，OEN=1，SRCEN=1	Possible
输出FIFO溢出	SRC_OVFI	OVF=1，OVEN=1，SRCEN=1	不可能
Output FIFO underflow	SRC_UDFI	UDF = 1, UDEN = 1, and SRCEN = 1	不可能
转换结束	SRC_CEFI	CEF = 1, CEEN = 1, and SRCEN = 1	不可能

当满足中断条件时，CPU执行中断异常处理程序。在此例程中清除中断源标志。

SRC_IDEI和SRC_ODFI中断可以激活DMAC。如果DMAC被激活，则来自
SRC不发送到CPU。

在DMA传输过程中，不要通过CPU写（读1后写0）清除IINT和OINT标志。

42.5 使用说明

42.5.1 访问寄存器的注意事项

以下对SRCCTRL的写入需要3个外设时钟(PCLKB)周期才能在
SRCSTAT:

- 将1写入SRCCTRL中的FL位，以设置SRCSTAT中的FLF标志
- 将1写入SRCCTRL中的CL位，用于初始化SRCSTAT中的每个位
- 当SRCEN位为0时，将1写入SRCCTRL中的SRCEN位，以初始化SRCSTAT中的每个位。

但是，由于CPU无需等待寄存器写入完成就执行任何后续指令，因此在向SRCCTRL写入指令后立即执行的指令无法正确读取SRCSTAT的更新状态。要检查SRCSTAT的更新状态，请在用于写入SRCCTRL的指令之后执行SRCCTRL或SRCSTAT的虚拟读取。

42.5.2 冲洗处理注意事项

当将1写入SRC控制寄存器(SRCCTRL)中的FL位时，SRC通过将0数据添加到输入数据端点来继续进行转换处理。因此，仅在音频数据端点为

input and there is no subsequent data.

To perform conversion again after flush processing, clear the internal work memory in either of the following ways.

- Write 1 to the CL bit in SRCCTRL
- Write 0 and then 1 to the SRCEN bit in SRCCTRL.

42.5.3 Notes on DMAC or DTC Transfer

When the DMAC or DTC is used for data transfer to the I/O data registers (SRCID and SRCOD), do not clear the IINT and OINT flags in the Status Register (SRCSTAT) by the CPU (writing 0 after reading 1) during transfer by the DMAC or DTC.

42.5.4 Notes on SRC Operation

Do not access the Filter Coefficient Table while the SRC is operating (SRCCTRL.SRCEN = 1).

42.5.5 Settings for the Module-Stop Function

SRC operation can be disabled or enabled using Module Stop Control Register C (MSTPCRC). The SRC module is initially stopped after reset. Releasing the module-stop state enables access to the registers. For details, see section 11, Low Power Modes.

输入，没有后续数据。

要在刷新处理后再次执行转换，请通过以下任一方式清除内部工作存储器。

- 将1写入SRCCTRL中的CL位
- 将0和1写入SRCCTRL中的SRCEN位。

42.5.3 关于DMAC或DTC传输的注意事项

当DMAC或DTC用于向IO数据寄存器（SRCID和SRCOD）传输数据时，CPU在传输过程中不要清除状态寄存器（SRCSTAT）中的IINT和OINT标志（读1后写0）。DMAC或DTC。

42.5.4 SRC操作注意事项

请勿在SRC运行时访问滤波器系数表(SRCCTRL.SRCEN=1)。

42.5.5 模块停止功能的设置

可以使用模块停止控制寄存器C(MSTPCRC)禁用或启用SRC操作。SRC模块在复位后最初停止。释放模块停止状态可以访问寄存器。有关详细信息，请参阅第11节，低功耗模式。

43. SD/MMC Host Interface (SDHI)

43.1 Overview

The Secure Digital Host Interface (SDHI) and MultiMediaCard (MMC) Interface provide the functionality required to connect a variety of external memory cards with the MCU. The SDHI supports both 1-bit and 4-bit buses for connecting different memory cards that support SD, SDHC, and SDXC formats. When developing host devices that are compliant with the SD Specifications, you must comply with the SD Host/Ancillary Product License Agreement (SD HALA).

The MMC interface supports 1-bit, 4-bit, and 8-bit MMC buses that provide eMMC 4.51 (JEDEC Standard JESD 84-B451) device access. This interface also provides backward compatibility and supports for high-speed SDR transfer modes.

Table 43.1 lists the SD/MMC Host Interface specifications and Figure 43.1 shows a block diagram.

Table 43.1 SD/MMC Host Interface specifications

Interface	Parameter	Specifications
SD	SD bus interface	• Compatible with SD memory card and SDIO card • Transfer bus mode selectable from 4-bit wide bus mode or 1-bit default bus mode • Compatible with SD, SDHC, and SDXC formats
SD and MMC shared	SDHI clock frequency	The SDHI clock is generated by dividing PCLKA by 2^n (n = 1 to 9).
	Error check functions	CRC7 (command/response), CRC16 (transfer data)
	Interrupt sources	Card access interrupt (SDHI_MMCn_ACCS), SDIO access interrupt (SDHI_MMCn_SDIO), Card detection interrupt (SDHI_MMCn_CARD) (n = 0 to 1)
	DMA transfer sources	DMAC and DTC triggerable by the SBFAI interrupt SD buffer is read and write accessible using the DMAC
	Other functions	• Card detect function • Write protect support
MMC	MMC bus interface	Transfer bus mode selectable from 1-bit, 4-bit, or 8-bit
	Transfer modes	Backward compatible mode or high-speed SDR mode selectable
	Other functions	e.MMC device access supported

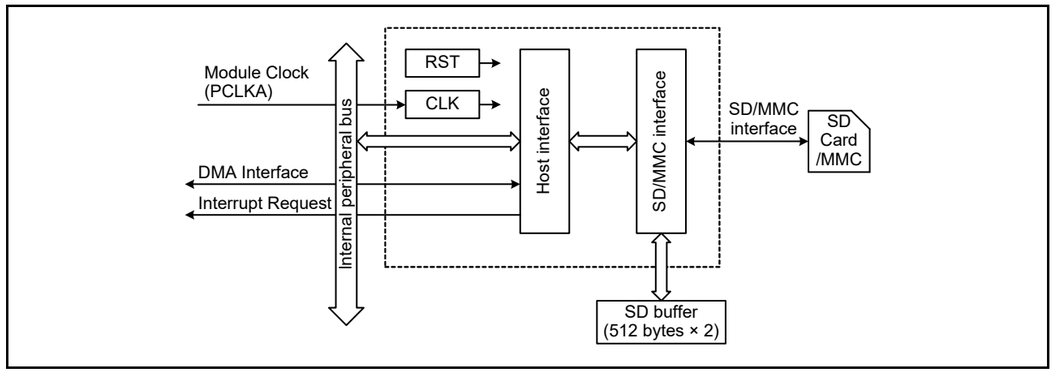


Figure 43.1 SD/MMC Host Interface block diagram

43. SDMMC主机接口(SDHI)

43.1 Overview

安全数字主机接口(SDHI)和多媒体卡(MMC)接口提供了将各种外部存储卡与MCU连接所需的功能。SDHI支持1位和4位总线，用于连接支持SD、SDHC和SDXC格式的不同存储卡。在开发符合SD规范的主机设备时，您必须遵守SD主机辅助产品许可协议(SDHALA)。

MMC接口支持提供eMMC4.51（JEDEC标准JESD84B451）器件访问的1位、4位和8位MMC总线。该接口还提供向后兼容性并支持高速SDR传输模式。

表43.1列出了SDMMC主机接口规范，图43.1显示了框图。

Table 43.1 SDMMC主机接口规格

Interface	Parameter	Specifications
SD	SD总线接口	兼容SD存储卡和SDIO卡 传输总线模式可选择4位宽总线模式或1位默认总线模式 兼容SD、SDHC和SDXC格式
SD和MMC共享	SDHI时钟频率	SDHI时钟是通过将PCLKA除以2n(n=1到9)生成的。
	错误检查功能	CRC7 (command/response), CRC16 (transfer data)
	中断源	卡访问中断(SDHI_MMCn_ACCS)、SDIO访问中断(SDHI_MMCn_SDIO)、卡检测中断(SDHI_MMCn_CARD)(n=0to1)
	DMA传输源	SBFAI中断可触发DMAC和DTC SD缓冲区可使用DMAC进行读写访问
	其他功能	卡检测功能 写保护支持
MMC	MMC总线接口	传输总线模式可选择1位、4位或8位
	传输模式	向后兼容模式或高速SDR模式可选
	其他功能	支持e.MMC设备访问

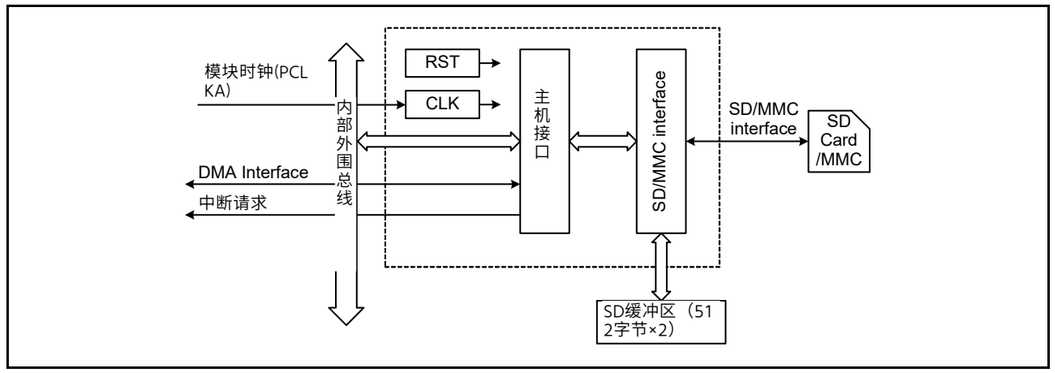


Figure 43.1 SDMMC主机接口框图

Table 43.2 SDHI I/O pins

Channel	Pin name	I/O	Description
Ch 0	SD0CLK	Output	SDHI clock
	SD0CMD	I/O	Command output, response input
	SD0DAT0	I/O	Data 0 (DAT0)
	SD0DAT1	I/O	Data 1 (DAT1), SDIO interrupt
	SD0DAT2	I/O	Data 2 (DAT2), SDIO Read wait
	SD0DAT3	I/O	Data 3 (DAT3), SD Card detect
	SD0DAT4	I/O	MMC Data 4 (DAT4)
	SD0DAT5	I/O	MMC Data 5 (DAT5)
	SD0DAT6	I/O	MMC Data 6 (DAT6)
	SD0DAT7	I/O	MMC Data 7 (DAT7)
	SD0CD	Input	SD card detection
	SD0WP	Input	SD card write protection
Ch 1	SD1CLK	Output	SDHI clock
	SD1CMD	I/O	Command output, response input
	SD1DAT0	I/O	Data 0 (DAT0)
	SD1DAT1	I/O	Data 1 (DAT1), SDIO interrupt
	SD1DAT2	I/O	Data 2 (DAT2), SDIO Read wait
	SD1DAT3	I/O	Data 3 (DAT3), SD Card detect
	SD1DAT4	I/O	MMC Data 4 (DAT4)
	SD1DAT5	I/O	MMC Data 5 (DAT5)
	SD1DAT6	I/O	MMC Data 6 (DAT6)
	SD1DAT7	I/O	MMC Data 7 (DAT7)
	SD1CD	Input	SD card detection
	SD1WP	Input	SD card write protection

43.2 Register Descriptions

43.2.1 Command Type Register (SD_CMD)

Address(es): SDHI0.SD_CMD 4006 2000h, SDHI1.SD_CMD 4006 2400h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CMD12AT[1:0]		TRSTP	CMDRW	CMDTP	RSPTP[2:0]			ACMD[1:0]		CMDIDX[5:0]					
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b5 to b0	CMDIDX[5:0]	Command Index Field Value Select	These bits configure the command index field value. The examples shown include the bit values for the ACMD[1:0] bits. b7 b0 0 0 0 0 0 1 1 0: CMD6 0 0 0 1 0 0 1 0: CMD18 0 1 0 0 1 1 0 1: ACMD13	R/W

Table 43.2 SDHI I/O pins

Channel	引脚名称	I/O	Description
Ch 0	SD0CLK	Output	SDHI clock
	SD0CMD	I/O	命令输出，响应输入
	SD0DAT0	I/O	Data 0 (DAT0)
	SD0DAT1	I/O	数据1(DAT1)，SDIO中断
	SD0DAT2	I/O	数据2(DAT2)，SDIO读取等待
	SD0DAT3	I/O	数据3(DAT3)，SD卡检测
	SD0DAT4	I/O	MMC Data 4 (DAT4)
	SD0DAT5	I/O	MMC Data 5 (DAT5)
	SD0DAT6	I/O	MMC Data 6 (DAT6)
	SD0DAT7	I/O	MMC Data 7 (DAT7)
	SD0CD	Input	SD卡检测
	SD0WP	Input	SD卡写保护
Ch 1	SD1CLK	Output	SDHI clock
	SD1CMD	I/O	命令输出，响应输入
	SD1DAT0	I/O	Data 0 (DAT0)
	SD1DAT1	I/O	数据1(DAT1)，SDIO中断
	SD1DAT2	I/O	数据2(DAT2)，SDIO读取等待
	SD1DAT3	I/O	数据3(DAT3)，SD卡检测
	SD1DAT4	I/O	MMC Data 4 (DAT4)
	SD1DAT5	I/O	MMC Data 5 (DAT5)
	SD1DAT6	I/O	MMC Data 6 (DAT6)
	SD1DAT7	I/O	MMC Data 7 (DAT7)
	SD1CD	Input	SD卡检测
	SD1WP	Input	SD卡写保护

43.2 注册说明

43.2.1 命令类型寄存器(SD_CMD)

Address(es): SDHI0.SD_CMD 4006 2000h, SDHI1.SD_CMD 4006 2400h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CMD12AT[1:0]		TRSTP	CMDRW	CMDTP	RSPTP[2:0]			ACMD[1:0]		CMDIDX[5:0]					
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b5 to b0	CMDIDX[5:0]	命令索引字段值选择	这些位配置命令索引字段值。所示示例包括ACMD[1:0]位的位值。 b7b000000110：CMD600010010：CMD18 01001101：ACMD13	R/W

Bit	Symbol	Bit name	Description	R/W
b7, b6	ACMD[1:0]	Command Type Select	b7 b6 0 0: CMD 0 1: ACMD. Other settings are prohibited.	R/W
b10 to b8	RSPTP[2:0]	Response Type Select*1	b10 b8 0 0 0: Normal mode Depending on the command, the response type and transfer method are selected in the ACMD[1:0] and CMDIDX[5:0] bits. At this time, the values for b15 to b11 in this register are invalid. 0 1 1: Extended mode and no response 1 0 0: Extended mode and R1, R5, R6, or R7 response 1 0 1: Extended mode and R1b response 1 1 0: Extended mode and R2 response 1 1 1: Extended mode and R3 or R4 response. Other settings are prohibited.	R/W
b11	CMDTP	Data Transfer Select*2	0: Do not include data transfer (bc, bcr, or ac) in command 1: Include data transfer (adtc) in command.	R/W
b12	CMDRW	Data Transfer Direction Select*3	0: Write (SD/MMC Host Interface → SD card/MMC) 1: Read (SD/MMC Host Interface ← SD card/MMC).	R/W
b13	TRSTP	Block Transfer Select*3	0: Single block transfer 1: Multiple blocks transfer.	R/W
b15, b14	CMD12AT[1:0]	CMD12 Automatic Issue Select*4	b15 b14 0 0: Automatically issue CMD12 during multiblock transfer 0 1: Do not automatically issue CMD12 during multiblock transfer. Other settings are prohibited.	R/W
b31 to b16	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Some commands cannot be used in normal mode.
Note 2. The CMDTP bit is only valid when the RSPTP[2:0] bits are 011b, 100b, 101b, 110b, or 111b.
Note 3. Bits CMDRW and TRSTP are only valid when the RSPTP[2:0] bits are 011b, 100b, 101b, 110b, or 111b, and the CMDTP bit is 1.
Note 4. The CMD12AT[1:0] bits are only valid when the RSPTP[2:0] bits are 011b, 100b, 101b, 110b, or 111b, and the TRSTP bit is 1.

The command type and response type are set in the SD_CMD register. The command type and transfer mode must be set when the RSPTP[2:0] bits are 011b, 100b, 101b, 110b, or 111b. The sequence starts when a value is written to this register. See Table 43.8 and Table 43.9 for setting examples. Do not write to the SD_CMD register when the SD_INFO2.CBSY flag is 1.

43.2.2 SD Command Argument Register (SD_ARG)

Address(es): SDHI0.SD_ARG 4006 2008h, SDHI1.SD_ARG 4006 2408h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b31 to b0	—	—	These bits specify command format[39:8] (argument).	R/W

The SD_ARG register is used for setting the argument field value. Set the SD_ARG register before setting the SD_CMD register. The argument field value of the automatically issued CMD12 is 0000_0000h regardless of the SD_ARG register value.

Bit	Symbol	位名称	Description	R/W
b7, b6	ACMD[1:0]	命令类型选择	b7b600：CMD01：ACMD。 禁止其他设置。	R/W
b10 to b8	RSPTP[2:0]	响应类型选择*1	b10 b8 0 0 0：正常模式 根据命令，在ACMD[1:0]和CMDIDX[5:0]位中选择响应类型和传输方法。此时，该寄存器中b15到b11的值无效。 0 1 1：扩展模式无响应 1 0 0：扩展模式和R1、R5、R6或R7响应 1 0 1：扩展模式和R1b响应 1 1 0：扩展模式和R2响应 11：扩展模式和R3或R4响应。禁止其他设置。	R/W
b11	CMDTP	数据传输选择*2	0：在命令中不包括数据传输（bc、bcr或ac）1：在命令中包括数据传输（adtc）。	R/W
b12	CMDRW	数据传输方向Select*3	0：写入（SDMMC主机接口→SD卡MMC）1：读取（SDMMC主机接口←SD卡MMC）。	R/W
b13	TRSTP	块传输选择*3	0：单块传输1：多块传输 。	R/W
b15, b14	CMD12AT[1:0]	CMD12自动发行Select*4	b15 b14 0 0：在多块传输过程中自动发出CMD12 01：在多块传输期间不自动发出CMD12。禁止其他设置。	R/W
b31 to b16	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 有些命令不能在正常模式下使用。
Note 2. CMDTP位仅在RSPTP[2:0]位为011b、100b、101b、110b或111b时有效。
Note 3. 仅当RSPTP[2:0]位为011b、100b、101b、110b或111b且CMDTP位为1时，位CMDRW和TRSTP才有效。
Note 4. CMD12AT[1:0]位仅在RSPTP[2:0]位为011b、100b、101b、110b或111b且TRSTP位为1时有效。

命令类型和响应类型在SD_CMD寄存器中设置。当RSPTP[2:0]位为011b、100b、101b、110b或111b时，必须设置命令类型和传输模式。当一个值被写入该寄存器时，序列开始。设置示例见表43.8和表43.9。当SD_INFO2.CBSY标志为1时，不要写入SD_CMD寄存器。

43.2.2 SD命令参数寄存器(SD_ARG)

Address(es): SDHI0.SD_ARG 4006 2008h, SDHI1.SD_ARG 4006 2408h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b31 to b0	—	—	这些位指定命令格式[39:8]（参数）。	R/W

SD_ARG寄存器用于设置参数字段值。在设置SD_CMD寄存器之前设置SD_ARG寄存器。无论SD_ARG寄存器的值如何，自动发出的CMD12的参数字段值为0000_0000h。

43.2.3 SD Command Argument Register 1 (SD_ARG1)

Address(es): SDHI0.SD_ARG1 4006 200Ch, SDHI1.SD_ARG1 4006 240Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b15 to b0	—	—	These bits specify command format[39:24] (argument).	R/W
b31 to b16	—	Reserved	These bits are read as 0.	R

The SD_ARG1 register is used for setting the argument field value. Set the SD_ARG1 register before setting the SD_CMD register. The argument field value of the automatically issued CMD12 is 0000_0000h regardless of the SD_ARG1 register value.

43.2.4 Data Stop Register (SD_STOP)

Address(es): SDHI0.SD_STOP 4006 2010h, SDHI1.SD_STOP 4006 2410h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	SEC	—	—	—	—	—	—	—	STP
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	STP	Transfer Stop	Data transfer stops when this bit is set to 1.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	SEC	Block Count Register Value Select *1	0: Disable SD_SECCNT register value 1: Enable SD_SECCNT register value.	R/W
b31 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Do not rewrite this bit when the SD_INFO2.CBSY flag is 1.

The SD_STOP register stops data transfer. During a multiblock transfer sequence, the SD_SECCNT register value (number of blocks to be transferred) can be set to valid or invalid by setting the SD_STOP register.

STP bit (Transfer Stop)

When the STP bit is set to 1 during multiple block transfer, CMD12 is issued to halt the transfer through the SDHI. However, if a command sequence is halted because of a communications error or timeout, CMD12 is not issued. Although continued buffer access is possible even after STP is set to 1, the buffer access error bit (ILR or ILW) in SD_INFO2 is set accordingly.

When STP is set to 1 during transfer for single block write, the access end flag sets when SD_BUF becomes empty, and CMD12 is not issued. If SD_BUF does contain data, the access end flag sets on completion of reception of the busy state

43.2.3 SD命令参数寄存器1(SD_ARG1)

Address(es): SDHI0.SD_ARG1 4006 200Ch, SDHI1.SD_ARG1 4006 240Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b15 to b0	—	—	这些位指定命令格式[39:24]（参数）。	R/W
b31 to b16	—	Reserved	这些位读为0。	R

SD_ARG1寄存器用于设置参数字段值。在设置SD_CMD寄存器之前设置SD_ARG1寄存器。自动发出的CMD12的参数字段值是0000_0000h与
SD_ARG1寄存器值。

43.2.4 数据停止寄存器(SD_STOP)

Address(es): SDHI0.SD_STOP 4006 2010h, SDHI1.SD_STOP 4006 2410h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	SEC	—	—	—	—	—	—	—	STP
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	STP	中转站	当该位设置为1时，数据传输停止。	R/W
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b8	SEC	块计数寄存器值选择*1	0：禁用SD_SECCNT寄存器值1：启用SD_SECCNT寄存器值。	R/W
b31 to b9	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 当SD_INFO2.CBSY标志为1时，不要重写该位。

SD_STOP寄存器停止数据传输。在多块传输序列期间，可以通过设置SD_STOP寄存器将SD_SECCNT寄存器值（要传输的块数）设置为有效或无效。

STP位（传输停止）

在多块传输期间STP位设置为1时，发出CMD12以停止通过SDHI的传输。但是，如果命令序列由于通信错误或超时而停止，则不会发出CMD12。
尽管即使在STP设置为1后仍可以继续访问缓冲区，但缓冲区访问错误位（ILR或ILW）在SD_INFO2相应设置。

在单块写入的传输过程中将STP设置为1时，当SD_BUF为空时设置访问结束标志，并且不发出CMD12。如果SD_BUF确实包含数据，则在完成接收繁忙状态时设置访问结束标志

without CMD12 being issued.

When STP is set to 1 during transfer for single block read, the access end flag sets immediately after the STP bit is set, and CMD12 is not issued.

When STP is set to 1 during reception of the busy state after an R1b response, the access end flag sets on completion of reception of the busy state without CMD12 being issued.

When STP is set to 1 after a command sequence is completed, CMD12 is not issued and the access end flag does not set.

Set STP to 1 after the response end flag sets.

Set STP to 0 after the access end flag sets.

SEC bit (Block Count Register Value Select)

When SD_CMD is set in the following section to start the command sequence while the SEC bit is set to 1, CMD12 is automatically issued to stop multiblock transfer with the number of blocks set in SD_SECCNT.

CMD18 or CMD25 in normal mode (SD_CMD[10:8] = 000)

SD_CMD[15:13] = 001 in extended mode (CMD12 is automatically issued, multiple block transfer)

When the command sequence is halted because of a communications error or timeout, CMD12 is not automatically issued.

43.2.5 Block Count Register (SD_SECCNT)

Address(es): SDHI0.SD_SECCNT 4006 2014h, SDHI1.SD_SECCNT 4006 2414h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

When performing a multiblock transfer, SD_SECCNT is a read/write register used to set the number of blocks to be transferred. For example, when the register value is 0000_0001h, 1 block is transferred. When the register value is 0000_FFFFh, 65,535 blocks are transferred and when the register value is FFFF_FFFFh, 4,294,967,295 blocks are transferred. Do not set this register to 0000_0000h. Do not rewrite the SD_SECCNT register when the SD_INFO2.CBSY flag is 1.

43.2.6 SD Card Response Register 10 (SD_RSP10), SD Card Response Register 32 (SD_RSP32), SD Card Response Register 54 (SD_RSP54)

Address(es): SDHI0.SD_RSP10 4006 2018h, SDHI1.SD_RSP10 4006 2418h, SDHI0.SD_RSP32 4006 2020h, SDHI1.SD_RSP32 4006 2420h SDHI0.SD_RSP54 4006 2028h, SDHI1.SD_RSP54 4006 2428h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

没有发出CMD12。

在单块读取传输期间STP设置为1时，在设置STP位后立即设置访问结束标志，并且不发出CMD12。

当在R1b响应后的忙状态接收期间STP设置为1时，访问结束标志在忙状态接收完成时设置，而不发出CMD12。

当命令序列完成后STP设置为1时，不发出CMD12并且不设置访问结束标志。

设置响应结束标志后将STP设置为1。

设置访问结束标志后将STP设置为0。

SEC位（块计数寄存器值选择）

当在以下部分中设置SD_CMD以启动命令序列而SEC位设置为1时，将自动发出CMD12以停止多块传输，其中块数在SD_SECCNT中设置。

正常模式下的CMD18或CMD25(SD_CMD[10:8]=000)

SD_CMD[15:13]=001扩展模式（CMD12自动下发，多块传输）

当命令序列由于通信错误或超时而停止时，不会自动发出CMD12。

43.2.5 块计数寄存器(SD_SECCNT)

Address(es): SDHI0.SD_SECCNT 4006 2014h, SDHI1.SD_SECCNT 4006 2414h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

执行多块传输时，SD_SECCNT是一个读写寄存器，用于设置要传输的块数。例如，当寄存器值为0000_0001h时，传输1个块。当寄存器值为0000_FFFFh时，传送65 535个块，当寄存器值为FFFF_FFFFh时，传送4 294 967 295个块。不要将此寄存器设置为0000_0000h。当SD_INFO2.CBSY标志为1时，不要重写SD_SECCNT寄存器。

43.2.6 SD卡响应寄存器10(SD_RSP10)、SD卡响应寄存器32(SD_RSP32)、SD卡响应寄存器54(SD_RSP54)

Address(es): SDHI0.SD_RSP10 4006 2018h, SDHI1.SD_RSP10 4006 2418h, SDHI0.SD_RSP32 4006 2020h, SDHI1.SD_RSP32 4006 2420h SDHI0.SD_RSP54 4006 2028h, SDHI1.SD_RSP54 4006 2428h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

43.2.7 SD Card Response Register 1 (SD_RSP1), SD Card Response Register 3 (SD_RSP3), SD Card Response Register 5 (SD_RSP5)

Address(es): SDHI0.SD_RSP1 4006 201Ch, SDHI1.SD_RSP1 4006 241Ch, SDHI0.SD_RSP3 4006 2024h, SDHI1.SD_RSP3 4006 2424h, SDHI0.SD_RSP5 4006 202Ch, SDHI1.SD_RSP5 4006 242Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b15 to b0	—	—	These bits store the response from the SD card/MMC.	R
b31 to b16	—	Reserved	These bits are read as 0.	R

43.2.8 SD Card Response Register 76 (SD_RSP76)

Address(es): SDHI0.SD_RSP76 4006 2030h, SDHI1.SD_RSP76 4006 2430h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b23 to b0	—	—	These bits store the response from the SD card/MMC.	R
b31 to b24	—	Reserved	These bits are read as 0.	R

43.2.9 SD Card Response Register 7 (SD_RSP7)

Address(es): SDHI0.SD_RSP7 4006 2034h, SDHI1.SD_RSP7 4006 2434h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	—	—	These bits store the response from the SD card/MMC.	R

43.2.7 SD卡响应寄存器1(SD_RSP1)、SD卡响应寄存器3(SD_RSP3)、SD卡响应寄存器5(SD_RSP5)

Address(es): SDHI0.SD_RSP1 4006 201Ch, SDHI1.SD_RSP1 4006 241Ch, SDHI0.SD_RSP3 4006 2024h, SDHI1.SD_RSP3 4006 2424h, SDHI0.SD_RSP5 4006 202Ch, SDHI1.SD_RSP5 4006 242Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b15 to b0	—	—	这些位存储来自SD卡MMC的响应。	R
b31 to b16	—	Reserved	这些位读为0。	R

43.2.8 SD卡响应寄存器76(SD_RSP76)

Address(es): SDHI0.SD_RSP76 4006 2030h, SDHI1.SD_RSP76 4006 2430h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—								
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b23 to b0	—	—	这些位存储来自SD卡MMC的响应。	R
b31 to b24	—	Reserved	这些位读为0。	R

43.2.9 SD卡响应寄存器7(SD_RSP7)

Address(es): SDHI0.SD_RSP7 4006 2034h, SDHI1.SD_RSP7 4006 2434h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—								
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b7 to b0	—	—	这些位存储来自SD卡MMC的响应。	R

Bit	Symbol	Bit name	Description	R/W
b31 to b8	—	Reserved	These bits are read as 0.	R

SD_RSP10, SD_RSP32, SD_RSP54, SD_RSP1, SD_RSP3, SD_RSP5, SD_RSP76, and SD_RSP7 are read-only registers that store the response from the SD card/MMC. Depending on the type of response from the SD card/MMC, the SD/MMC Host Interface divides and stores the response among the four registers.

Table 43.3 lists the correspondence between the response type and its storage destination.

Table 43.3 Correspondence between response type and storage destination

Response type	SD_RSP10 register	SD_RSP32 register	SD_RSP54 register	SD_RSP1 register	SD_RSP3 register	SD_RSP5 register	SD_RSP76 register	SD_RSP7 register
R1	[39:8]	—	[39:8]*1	—	—	—	—	—
R1b	[39:8]	—	[39:8]*1	—	—	—	—	—
R2	[39:8]	[71:40]	[103:72]	—	—	—	[127:104]	—
R3	[39:8]	—	—	—	—	—	—	—
R4	[39:8]	—	—	—	—	—	—	—
R5	[39:8]	—	—	—	—	—	—	—
R6	[39:8]	—	—	—	—	—	—	—
R7	[39:8]	—	—	—	—	—	—	—

Note 1. The responses for CMD18 and CMD25 are stored in registers SD_RSP10 and SD_RSP54. Therefore, even if the SD_RSP10 register is overwritten with the response for the automatically issued CMD12, the response for CMD18 or CMD25 can be confirmed by reading the SD_RSP54 register.

43.2.10 SD Card Interrupt Flag Register 1 (SD_INFO1)

Address(es): SDHI0.SD_INFO1 4006 2038h, SDHI1.SD_INFO1 4006 2438h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	SDD3MON	SDD3IN	SDD3RM	SDWPMON	—	SDCDMON	SDCDIN	SDCDRM	ACEND	—	RSPENDD
Value after reset:	0	0	0	0	0	x	0	0	x	0	x	0	0	0*1	0	0*1

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b0	RSPEND	Response End Detection Flag	0: Response end not detected 1: Response end detected.	R(/W)*2
b1	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b2	ACEND	Access End Detection Flag	0: Access end not detected 1: Access end detected.	R(/W)*2
b3	SDCDRM	SDnCD Removal Flag	0: SD card/MMC removal not detected by the SDnCD pin 1: SD card/MMC removal detected by the SDnCD pin.	R(/W)*2
b4	SDCDIN	SDnCD Insertion Flag	0: SD card/MMC insertion not detected by the SDnCD pin 1: SD card/MMC insertion detected by the SDnCD pin.	R(/W)*2
b5	SDCDMON	SDnCD Pin Monitor Flag	0: SDnCD pin level is high*3 1: SDnCD pin level is low.*3	R
b6	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b7	SDWPMON	SDnWP Pin Monitor Flag	0: SDnWP pin level is high 1: SDnWP pin level is low.	R

Bit	Symbol	位名称	Description	R/W
b31 to b8	—	Reserved	这些位读为0。	R

SD_RSP10、SD_RSP32、SD_RSP54、SD_RSP1、SD_RSP3、SD_RSP5、SD_RSP76和SD_RSP7是只读寄存器，用于存储来自SD卡MMC的响应。根据SD卡MMC的响应类型，SDMMC主机接口在四个寄存器之间划分和存储响应。

表43.3列出了响应类型与其存储目的地的对应关系。

Table 43.3 响应类型与存储目的地的对应关系

响应类型	SD_RSP10 register	SD_RSP32 register	SD_RSP54 register	SD_RSP1 register	SD_RSP3 register	SD_RSP5 register	SD_RSP76 register	SD_RSP7 register
R1	[39:8]	—	[39:8]*1	—	—	—	—	—
R1b	[39:8]	—	[39:8]*1	—	—	—	—	—
R2	[39:8]	[71:40]	[103:72]	—	—	—	[127:104]	—
R3	[39:8]	—	—	—	—	—	—	—
R4	[39:8]	—	—	—	—	—	—	—
R5	[39:8]	—	—	—	—	—	—	—
R6	[39:8]	—	—	—	—	—	—	—
R7	[39:8]	—	—	—	—	—	—	—

Note 1. CMD18和CMD25的响应存储在寄存器SD_RSP10和SD_RSP54中。因此，即使SD_RSP10寄存器被自动发出的CMD12的响应覆盖，CMD18或CMD25的响应也可以通过读取SD_RSP54寄存器来确认。

43.2.10 SD卡中断标志寄存器1(SD_INFO1)

Address(es): SDHI0.SD_INFO1 4006 2038h, SDHI1.SD_INFO1 4006 2438h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	SDD3MON	SDD3IN	SDD3RM	SDWPMON	—	SDCDMON	SDCDIN	SDCDRM	ACEND	—	RSPENDD
重置后的值:	0	0	0	0	0	x	0	0	x	0	x	0	0	0*1	0	0*1

x: Undefined

Bit	Symbol	位名称	Description	R/W
b0	RSPEND	响应结束检测标志	0：未检测到响应结束1：检测到响应结束。	R(/W)*2
b1	—	Reserved	该位读取为0。写入值应为0。	R/W
b2	ACEND	访问结束检测标志	0：未检测到访问结束1：检测到访问结束。	R(/W)*2
b3	SDCDRM	SDnCD删除标志	0：SDnCD引脚未检测到SD卡MMC移除1：SDnCD引脚检测到SD卡MMC移除。	R(/W)*2
b4	SDCDIN	SDnCD插入标志	0：SDnCD引脚未检测到SD卡MMC插入1：SDnCD引脚检测到SD卡MMC插入。	R(/W)*2
b5	SDCDMON	SDnCD引脚监控标志	0：SDnCD引脚高电平*31：SDnCD引脚低电平*3	R
b6	—	Reserved	该位读取为0。写入值应为0。	R/W
b7	SDWPMON	SDnWP引脚监控标志	0：SDnWP引脚高电平1：SDnWP引脚低电平。	R

Bit	Symbol	Bit name	Description	R/W
b8	SDD3RM	SDnDAT3 Removal Flag	0: SD card/MMC removal not detected by the SDnDAT3 pin 1: SD card/MMC removal detected by the SDnDAT3 pin.	R(/W)*2
b9	SDD3IN	SDnDAT3 Insertion Flag	0: SD card/MMC insertion not detected by the SDnDAT3 pin 1: SD card/MMC insertion detected by the SDnDAT3 pin.	R(/W)*2
b10	SDD3MON	SDnDAT3 Pin Monitor Flag	0: SDnDAT3 pin level is low 1: SDnDAT3 pin level is high.	R
b31 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. The value is initialized by a reset and also on reset triggered by the SOFT_RST.SDRST flag.
Note 2. The flag does not change even if set to 1. Writing 0 changes the flag value to 0.
Note 3. The flag changes when the pin level continues for the period set in the SD_OPTION.CTOP[3:0] bits or longer.

The SD_INFO1 register indicates the detection of a response end or access end for a command sequence. The SD_INFO1 register also indicates the detection SD card/MMC insertion/removal and the write protection status.

During a multiblock transfer sequence, if CMD12 or CMD52 (SDIO abort) is issued, the ACEND flag sets to 1, but the RSPEND flag remains set to 0.

If the command sequence is stopped because of a communication error or timeout, the ACEND flag or RSPEND flag sets to 1.

After a reset is canceled, the SDD3MON bit, SDD3IN flag, and SDD3RM flag values are changed in accordance with the status of the SDnDAT3 (n = 0, 1) pin, and their values are changed when data is being transferred in wide bus mode. These 3 bits are used only for SD card. Set flags to be cleared to 0. Set flags that are not being cleared to 1.

RSPEND flag (Response End Detection Flag)

The RSPEND flag indicates that a response end was detected.

[Setting conditions]

- When reception of the response is completed
- When transmission of a command without response is completed
- When reception of the busy state after R1b response is completed
- When reception of the response to CMD52 that was issued by setting the C52PUB bit to 1 is completed for transfer of multiple block read
- When reception of the response to CMD52 that was issued by setting the C52PUB bit to 1 is completed for transfer of multiple block write
- This bit is set when a command sequence is halted because of a communications error or timeout.

[Clearing conditions]

- When 0 is written to RSPEND
- When a command without data is issued.

Note: When a command is issued in absence of data transfer, the RSPEND flag becomes 1 after the command sequence ends.

ACEND flag (Access End Detection Flag)

The ACEND flag indicates that an access end was detected.

[Setting conditions]

- When read access to the buffer is completed for transfer of single block read
- When read access to the buffer for the last block of data is completed for transfer of multiple block read
- When read access to the buffer and reception of the response to CMD12 are completed for transfer of multiple block read with automatic issuing of CMD12
- When reception of the busy state after reception of the CRC status is completed for transfer of single block write

Bit	Symbol	位名称	Description	R/W
b8	SDD3RM	SDnDAT3删除标志	0：SDnDAT3引脚未检测到SD卡MMC移除1：SDnDAT3引脚检测到SD卡MMC移除。	R(/W)*2
b9	SDD3IN	SDnDAT3插入标志	0：SDnDAT3引脚未检测到SD卡MMC插入1：SDnDAT3引脚检测到SD卡MMC插入。	R(/W)*2
b10	SDD3MON	SDnDAT3引脚监控标志	0：SDnDAT3引脚低电平1： SDnDAT3引脚高电平。	R
b31 to b11	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 该值由复位初始化，也由SOFT_RST.SDRST标志触发复位。
Note 2. 即使设置为1，标志也不会改变。写入0会将标志值更改为0。
Note 3. 当引脚电平持续SD_OPTION.CTOP[3:0]位中设置的周期或更长时间时，该标志会发生变化。

SD_INFO1寄存器指示对命令序列的响应结束或访问结束的检测。这
SD_INFO1寄存器还指示检测SD卡MMC插入移除和写保护状态。

在多块传输序列期间，如果发出CMD12或CMD52（SDIO中止），则ACEND标志设置为1，但
RSPEND标志保持设置为0。

如果命令序列由于通信错误或超时而停止，则ACEND标志或RSPEND标志设置为1。

复位取消后，SDD3MON位、SDD3IN标志和SDD3RM标志值根据SDnDAT3(n=0 1)引脚的状态而改变，并且在宽总线模式下传输数据时改变它们的值.这3位仅用于SD卡。将要清除的标志设置为0。将未清除的标志设置为1。

RSPEND标志（响应结束检测标志）

RSPEND标志表示检测到响应结束。

[Setting conditions]

- 响应接收完成时
- 当无响应的命令传输完成时
- 当R1b响应后忙状态的接收完成时
- 将C52PUB位设置为1发出的对CMD52的响应的接收完成时，用于传输多块读取
- 多块写入传送的C52PUB位为1的CMD52响应接收完成时
- 当命令序列由于通信错误或超时而停止时，该位被设置。

[Clearing conditions]

- 当0写入RSPEND时
- 发出没有数据的命令时。

Note: 当在没有数据传输的情况下发出命令时，RSPEND标志在命令序列结束后变为1。

ACEND标志（访问结束检测标志）

ACEND标志表示检测到访问结束。

[Setting conditions]

- 当完成对缓冲区的读取访问以传输单块读取时
- 当完成对最后一个数据块的缓冲区的读取访问以传输多块读取时
- 当对缓冲区的读取访问和对CMD12的响应的接收完成时，通过自动发出CMD12传输多块读取
- 接收CRC状态后的忙碌状态接收完成时，用于单块写入的传输

- When reception of the busy state after reception of the CRC status of the last block of data is completed for transfer of multiple block write
- When reception of the response busy state for CMD12 is completed for transfer of multiple block write with automatic issuing of CMD12
- When reception of the response to CMD12 that was issued by setting the STP bit to1 is completed for transfer of multiple block read
- When reception of the response busy state for CMD12 that was issued by setting the STP bit to1 is completed for transfer of multiple block write
- When reception of the response to CMD52 that was issued by setting the IOABT bit to 1 is completed for transfer of multiple block read
- When reception of the response to CMD52 that was issued by setting the IOABT bit to1 is completed for transfer of multiple block write
- This bit is set when a command sequence is halted because of a communications error or timeout.

[Clearing conditions]

- When 0 is written to ACEND
- When the access end bit is set to 1.

Note: The ACEND flag becomes 1 after the command sequence ends.

SDCDRM flag (SDnCD Removal Flag)

The SDCDRM flag indicates that SDnCD was removed.

[Setting condition]

- After a change in SDnCD from 0 to 1, Mcycle elapsed with SDnCD held at 1.

[Clearing conditions]

- When 0 is written to SDCDRM.

Note: Mcycle is set in bits [3:0] in SD_OPTION.

SDCDIN flag (SDnCD Insertion Flag)

The SDCDIN flag indicates that SDnCD was inserted.

[Setting condition]

- After a change in SDnCD from 1 to 0, Mcycle elapsed with SDnCD held at 0.

[Clearing conditions]

- When 0 is written to SDCDIN.

Note: Mcycle is set in bits [3:0] in SD_OPTION.

SDD3RM flag (SDnDAT3 Removal Flag)

The SDD3RM flag indicates that SDnDAT3 was removed.

[Setting condition]

- After a change in SDnDAT3 from 1 to 0, two cycles of PCLKA elapsed with SDnDAT3 held at 0.

[Clearing condition]

- When 0 is written to SDD3RM.

SDD3IN flag (SDnDAT3 Insertion Flag)

The SDD3IN flag indicates that SDnDAT3 was inserted.

[Setting condition]

- 当接收到最后一个数据块的CRC状态后的忙碌状态接收完成时，用于传输多块写入
- 当CMD12的响应忙状态接收完成时，用于传输多块写入并自动发出CMD12
- 当通过将STP位设置为1发出的对CMD12的响应的接收完成时，用于传输多块读取
- 当通过将STP位设置为1发出的CMD12的响应忙状态接收完成时，用于传输多块写入
- 将IOABT位设置为1发出的对CMD52的响应的接收完成时，用于传输多块读取
- 将IOABT位设置为1发出的对CMD52的响应的接收完成时，用于传输多块写入
- 当命令序列由于通信错误或超时而停止时，该位被设置。

[Clearing conditions]

- 当0写入ACEND时
- 当访问结束位设置为1时。

Note: 命令序列结束后ACEND标志变为1。

SDCDRM标志（SDnCD移除标志）

SDCDRM标志表明SDnCD已被删除。

[Setting condition]

- 在SDnCD从0变为1后，Mcycle过去了，而SDnCD保持在1。

[Clearing conditions]

- 当0写入SDCDRM时。

Note: Mcycle在SD_OPTION的位[3:0]中设置。

SDCDIN标志（SDnCD插入标志）

SDCDIN标志表明SDnCD已插入。

[Setting condition]

- 在SDnCD从1变为0后，Mcycle过去了，而SDnCD保持在0。

[Clearing conditions]

- 当0写入SDCDIN时。

Note: Mcycle在SD_OPTION的位[3:0]中设置。

SDD3RM标志（SDnDAT3移除标志）

SDD3RM标志表示SDnDAT3已被删除。

[Setting condition]

- 在SDnDAT3从1变为0后，经过两个PCLKA周期，SDnDAT3保持在0。

[Clearing condition]

- 当0写入SDD3RM时。

SDD3IN标志（SDnDAT3插入标志）

SDD3IN标志表示SDnDAT3已插入。

[Setting condition]

- After a change in SDnDAT3 from 0 to 1, two cycles of PCLKA elapsed with SDnDAT3 held at 1.

[Clearing condition]

- When 0 is written to SDD3IN.

43.2.11 SD Card Interrupt Flag Register 2 (SD_INFO2)

Address(es): SDHI0.SD_INFO2 4006 203Ch, SDHI1.SD_INFO2 4006 243Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ILA	CBSY	SD_CLK_CTRLEN	—	—	—	BWE	BRE	SDD0MON	RSPTO	ILR	ILW	DTO	ENDE	CRCE	CMDE
Value after reset:	0*1	0*1	1*1	0	0	0	0*1	0*1	x	0*1	0*1	0*1	0*1	0*1	0*1	0*1

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b0	CMDE	Command Error Detection Flag	0: Command error not detected 1: Command error detected.	R/W*1
b1	CRCE	CRC Error Detection Flag	0: CRC error not detected 1: CRC error detected.	R/W*1
b2	ENDE	End Bit Error Detection Flag	0: End bit error not detected 1: End bit error detected.	R/W*1
b3	DTO	Data Timeout Detection Flag	0: Data timeout not detected 1: Data timeout detected.	R/W*1
b4	ILW	SD_BUF0 Illegal Write Access Detection Flag	0: Illegal write access to the SD_BUF0 register not detected 1: Illegal write access to the SD_BUF0 register detected.	R/W*1
b5	ILR	SD_BUF0 Illegal Read Access Detection Flag	0: Illegal read access to the SD_BUF0 register not detected 1: Illegal read access to the SD_BUF0 register detected.	R/W*1
b6	RSPTO	Response Timeout Detection Flag	0: Response timeout not detected 1: Response timeout detected.	R/W*1
b7	SDD0MON	SDHI_D0 Pin Status Flag	0: SDnDAT0 pin is low 1: SDnDAT0 pin is high.	R
b8	BRE	SD_BUF0 Read Enable Flag	0: Disable read access to the SD_BUF0 register 1: Enable read access to the SD_BUF0 register.	R/W*1
b9	BWE	SD_BUF0 Write Enable Flag	0: Disable write access to the SD_BUF0 register 1: Enable write access to the SD_BUF0 register.	R/W*1
b12 to b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b13	SD_CLK_CTRLEN	SD_CLK_CTRL Write Enable Flag	0: SD/MMC bus (CMD and DAT lines) is busy, so write access to the SD_CLK_CTRL.CLKEN and CLKSEL[7:0] bits is disabled 1: SD/MMC bus (CMD and DAT lines) is not busy, so write access to the SD_CLK_CTRL.CLKEN and CLKSEL[7:0] bits is enabled.	R
b14	CBSY	Command Sequence Status Flag	0: Command sequence complete 1: Command sequence in progress (busy).	R
b15	ILA	Illegal Access Error Detection Flag	0: Illegal access error not detected 1: Illegal access error detected.	R/W*1
b31 to b16	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. The flag does not change even if set to 1. Writing 0 changes the flag value to 0.

The SD_INFO2 register indicates the status of the SD buffer and the status of the SD card/MMC. Set flags to be cleared

- 在SDnDAT3从0变为1后，经过两个PCLKA周期，SDnDAT3保持在1。

[Clearing condition]

- 当0写入SDD3IN时。

43.2.11 SD卡中断标志寄存器2(SD_INFO2)

Address(es): SDHI0.SD_INFO2 4006 203Ch, SDHI1.SD_INFO2 4006 243Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ILA	CBSY	SD_CLK_CTRLEN	—	—	—	BWE	BRE	SDD0MON	RSPTO	ILR	ILW	DTO	ENDE	CRCE	CMDE
重置后的值:	0*1	0*1	1*1	0	0	0	0*1	0*1	x	0*1	0*1	0*1	0*1	0*1	0*1	0*1

x: Undefined

Bit	Symbol	位名称	Description	R/W
b0	CMDE	命令错误检测标志	0：未检测到命令错误1：检测到命令错误。	R/W*1
b1	CRCE	CRC错误检测标志	0：未检测到CRC错误1：检测到CRC错误。	R/W*1
b2	ENDE	结束位错误检测标志	0：未检测到结束位错误1：检测到结束位错误。	R/W*1
b3	DTO	数据超时检测标志	0：未检测到数据超时1：检测到数据超时。	R/W*1
b4	ILW	SD_BUF0非法写访问检测标志	0：未检测到对SD_BUF0寄存器的非法写访问1：检测到对SD_BUF0寄存器的非法写访问。	R/W*1
b5	ILR	SD_BUF0非法读取访问检测标志	0：未检测到对SD_BUF0寄存器的非法读访问1：检测到对SD_BUF0寄存器的非法读访问。	R/W*1
b6	RSPTO	响应超时检测Flag	0：未检测到响应超时1：检测到响应超时。	R/W*1
b7	SDD0MON	SDHI_D0引脚状态标志	0：SDnDAT0引脚为低电平1：SDnDAT0引脚为高电平。	R
b8	BRE	SD_BUF0读使能标志	0：禁用对SD_BUF0寄存器的读取访问1：启用对SD_BUF0寄存器的读取访问。	R/W*1
b9	BWE	SD_BUF0写使能标志	0：禁用对SD_BUF0寄存器的写访问1：启用对SD_BUF0寄存器的写访问。	R/W*1
b12 to b10	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b13	SD_CLK_CTRLEN	SD_CLK_CTRL写使能Flag	0：SDMMC总线（CMD和DAT线）忙，所以写对SD_CLK_CTRL.CLKEN和CLKSEL[7:0]位的访问被禁用1：SDMMC总线（CMD和DAT线）不忙，因此对SD_CLK_CTRL.CLKEN和CLKSEL[7:0]位的写访问被启用。	R
b14	CBSY	命令序列状态Flag	0：命令序列完成1：命令序列正在进行中（忙碌）。	R
b15	ILA	非法访问错误检测Flag	0：未检测到非法访问错误1：检测到非法访问错误。	R/W*1
b31 to b16	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 即使设置为1，标志也不会改变。写入0会将标志值更改为0。

SD_INFO2寄存器指示SD缓冲区的状态和SD卡MMC的状态。设置要清除的标志

to 0. Set flags that are not being cleared to 1.

CMDE flag (Command Error Detection Flag)

The CMDE flag indicates that a command error was detected. The command sequence stops when a command error occurs. When the SDIO_MODE.C52PUB bit is set to 1 and CMD52 is automatically issued, if a communication error or response timeout occurs, the command sequence is not completed. Perform the error processing shown in section section 43.3.12, IO_RW_EXTENDED Command (SD: CMD53/Multiple Block Read) or section 43.3.13, IO_RW_EXTENDED Command (SD: CMD53/Multiple Block Write), and complete the command sequence.

[Setting conditions]

- The command index of the transmitted command differs from the command index of the received response.
- The command index of a command issued within a command sequence differs from the command index of the received response.

[Clearing condition]

- When 0 is written to CMDE.

CRCE flag (CRC Error Detection Flag)

The CRCE flag indicates that a CRC error was detected. The command sequence stops when a CRC error occurs. When the SDIO_MODE.C52PUB bit is set to 1 and CMD52 is automatically issued, if a communication error or response timeout occurs, the command sequence is not completed. Perform the error processing shown in section 43.3.12, IO_RW_EXTENDED Command (SD: CMD53/Multiple Block Read) or section 43.3.13, IO_RW_EXTENDED Command (SD: CMD53/Multiple Block Write), and complete the command sequence.

[Setting conditions]

- When an error occurs in the CRC status.
- When a CRC error occurs in the read data.
- When a CRC error occurs in the response.
- A CRC error in the response to a command issued within a command sequence.

[Clearing condition]

- When 0 is written to CRCE.

ENDE flag (End Bit Error Detection Flag)

The ENDE flag indicates that an end bit error was detected. The command sequence is stopped when an end bit error occurs. When the SDIO_MODE.C52PUB bit is set to 1 and CMD52 is automatically issued, if a communication error or response timeout occurs, the command sequence is not completed. Perform the error processing shown in section 43.3.12, IO_RW_EXTENDED Command (SD: CMD53/Multiple Block Read) or section 43.3.13, IO_RW_EXTENDED Command (SD: CMD53/Multiple Block Write), and complete the command sequence.

[Setting conditions]

- When an error occurs in the response length (and the end bit is not detected).
- When an error occurs in the read data length (and the end bit is not detected among the valid bits).
- When an error occurs in the CRC status length (and the end bit is not detected).
- An error in the length of a response to a command issued within a command sequence, for example when the end bit is not detected.

[Clearing condition]

- When 0 is written to ENDE.

DTO flag (Data Timeout Detection Flag)

The DTO flag indicates that a data timeout was detected. The command sequence stops when a data timeout occurs.

[Setting conditions]

为0。将未清除的标志设置为1。

CMDE标志（命令错误检测标志）

CMDE标志指示检测到命令错误。发生命令错误时命令序列停止。当SDIO_MODE.C52PUB位设置为1并自动发出CMD52时，如果发生通信错误或响应超时，则命令序列未完成。执行第43.3.12节，IO_RW_EXTENDED命令（SD：CMD53多块读取）或43.3.13节，IO_RW_EXTENDED命令（SD：CMD53多块写入）中所示的错误处理，并完成命令序列。

[Setting conditions]

- 发送命令的命令索引与接收响应的命令索引不同。
- 在命令序列中发出的命令的命令索引与接收到的响应的命令索引不同。

[Clearing condition]

- 当0写入CMDE时。

CRCE标志（CRC错误检测标志）

CRCE标志表示检测到CRC错误。当发生CRC错误时，命令序列停止。当SDIO_MODE.C52PUB位设置为1并自动发出CMD52时，如果发生通信错误或响应超时，则命令序列未完成。执行第43.3.12节，IO_RW_EXTENDED命令（SD：CMD53多块读取）或第43.3.13节，IO_RW_EXTENDED中所示的错误处理

命令（SD：CMD53MultipleBlockWrite），完成命令序列。

[Setting conditions]

- CRC状态发生错误时。
- 当读取的数据发生CRC错误时。
- 当响应中出现CRC错误时。
- 对命令序列中发出的命令的响应中的CRC错误。

[Clearing condition]

- 当0写入CRCE时。

ENDE标志（结束位错误检测标志）

ENDE标志表示检测到结束位错误。当发生结束位错误时，命令序列停止。当SDIO_MODE.C52PUB位设置为1并自动发出CMD52时，如果发生通信错误或响应超时，则命令序列未完成。执行43.3.12节，IO_RW_EXTENDED命令（SD：CMD53多块读取）或43.3.13节，IO_RW_EXTENDED命令（SD：CMD53多块写入）中所示的错误处理，并完成命令序列。

[Setting conditions]

- 响应长度发生错误时（未检测到结束位）。
- 当读取数据长度发生错误时（有效位中未检测到结束位）。
- CRC状态长度发生错误时（未检测到结束位）。
- 对命令序列中发出的命令的响应长度错误，例如未检测到结束位时。

[Clearing condition]

- 当0写入ENDE时。

DTO标志（数据超时检测标志）

DTO标志表示检测到数据超时。当发生数据超时时，命令序列停止。

[Setting conditions]

- After R1b response, the busy state (SDnDAT0 = 0) continues for longer than Ncycle.
- After CRC status, the busy state (SDnDAT0 = 0) continues for longer than Ncycle.
- After write data, the CRC status is not received though Ncycle has elapsed.
- After read command, read data is not received though a time longer than Ncycle has elapsed.
- After CMD12 is issued within a command sequence, the busy state (SDnDAT0 = 0) for longer than Ncycle continues.
- After the reception of read data, read data for the next block are not received though a time longer than Ncycle has elapsed.
- After release of the read wait state, read data for the next block are not received though a time longer than Ncycle has elapsed.

Note: Ncycle is set in bits [7:4] in SD_OPTION.

[Clearing condition]

- When 0 is written to DTO.

ILW flag (SD_BUF0 Illegal Write Access Detection Flag)

The ILW flag indicates that an SD_BUF0 illegal write access was detected.

[Setting conditions]

- When data is written to SD_BUF0 while it is not in the data read/write command state.
- When data is written to SD_BUF0 while SD_BUF is full.
- When data is written to SD_BUF0 while an error occurs in the CRC status or CRC status length.
- When data is written to SD_BUF0 while a busy state after the CRC status continues for longer than Ncycle.

Note: Ncycle is set in bits [7:4] in SD_OPTION.

[Clearing condition]

- When 0 is written to ILW.

ILR flag (SD_BUF0 Illegal Read Access Detection Flag)

The ILR flag indicates that an SD_BUF0 illegal read access was detected.

[Setting conditions]

- When SD_BUF is empty while SD_BUF0 is read.
- When data with a CRC error or END error is read from SD_BUF0.

[Clearing condition]

- When 0 is written to ILR.

RSPTO flag (Response Timeout Detection Flag)

The RSPTO flag indicates that a response timeout was detected. The command sequence is stopped when a response timeout occurs. When the SDIOMD.C52PUB bit is set to 1 and CMD52 is automatically issued, if a communication error or response timeout occurs, the command sequence is not completed. Perform the error processing shown in section 43.3.12, IO_RW_EXTENDED Command (SD: CMD53/Multiple Block Read) or section 43.3.13, IO_RW_EXTENDED Command (SD: CMD53/Multiple Block Write), and complete the command sequence.

[Setting condition]

- When a response is not received though a time longer than 640 cycles of SD/MMC clock has elapsed (including a response to a command issued within a command sequence).

[Clearing condition]

- When 0 is written to RSPTO.

- 在R1b响应后，忙碌状态(SDnDAT0=0)持续时间超过Ncycle。
- 在CRC状态之后，忙碌状态(SDnDAT0=0)持续时间超过Ncycle。
- 写入数据后，虽然Ncycle已过，但未收到CRC状态。
- 在读取命令之后，虽然经过了超过Ncycle的时间，但没有接收到读取数据。
- 在命令序列内发出CMD12后，忙碌状态(SDnDAT0=0)持续时间超过Ncycle。
- 在接收到读取数据后，虽然经过了Ncycle以上的时间，但没有接收到下一个块的读取数据。
- 读取等待状态解除后，虽然经过了Ncycle以上的时间，但未接收到下一个块的读取数据。

Note: Ncycle在SD_OPTION的位[7:4]中设置。

[Clearing condition]

- 当0写入DTO时。

ILW标志（SD_BUF0非法写访问检测标志）

ILW标志表示检测到SD_BUF0非法写访问。

[Setting conditions]

- 当数据写入SD_BUF0而不是数据读写命令状态时。
- 当SD_BUF已满时将数据写入SD_BUF0。
- 当数据写入SD_BUF0且CRC状态或CRC状态长度发生错误时。
- 当数据写入SD_BUF0时，CRC状态后的忙碌状态持续时间超过Ncycle。

Note: Ncycle在SD_OPTION的位[7:4]中设置。

[Clearing condition]

- 当0写入ILW时。

ILR标志（SD_BUF0非法读访问检测标志）

ILR标志表示检测到SD_BUF0非法读取访问。

[Setting conditions]

- 当SD_BUF为空而SD_BUF0被读取时。
- 当从SD_BUF0读取具有CRC错误或END错误的数据时。

[Clearing condition]

- 当0写入ILR时。

RSPTO标志（响应超时检测标志）

RSPTO标志表示检测到响应超时。当发生响应超时时，命令序列停止。当SDIOMD.C52PUB位设置为1并自动发出CMD52时，如果发生通信错误或响应超时，则命令序列未完成。执行43.3.12节，IO_RW_EXTENDED命令（SD：CMD53多块读取）或43.3.13节，IO_RW_EXTENDED命令（SD：CMD53多块写入）中所示的错误处理，并完成命令序列。

[Setting condition]

- 超过640个SDMMC时钟周期后仍未收到响应时（包括对命令序列内发出的命令的响应）。

[Clearing condition]

- 当0写入RSPTO时。

SDD0MON flag (SDHI_D0 Pin Status Flag)

The SDD0MON flag indicates the status of the SDHI_D0 pin. If the data timeout (DTO) is set but the response timeout (RSPTO) is not set after the Erase command is issued, the end of the Erase sequence (SDD0MON = 1) is confirmed by polling DAT0.

If a communication error or timeout occurs during a write sequence, the DAT0 bit might retain the value 0.

While the SD/MMC clock is stopped, the DAT0 bit retains the value before the clock is stopped.

BRE flag (SD_BUF0 Read Enable Flag)

The BRE flag indicates that SD_BUF0 is enabled for reading.

[Setting conditions]

- When data set in SD_SIZE is stored in SD_BUF0 at single block transfer.
- When data set in SD_SIZE is stored in either bank 1 or bank 2 of SD_BUF0 at multiple block transfer.

[Clearing conditions]

- When 0 is written to BRE
- Reading of a block of data from SD_BUF0 by DMA transfer

When data is read from SD_BUF0 by the CPU, clear BRE then read the amount of data specified in SD_SIZE.

Even if a CRC error or an END error occurs while block data is read, data is stored in SD_BUF0 and BRE is set.

BWE flag (SD_BUF0 Write Enable Flag)

The BWE flag indicates that SD_BUF0 is enabled for writing.

[Setting conditions]

- When SD_BUF0 is empty at single block transfer.
- When either bank 1 or bank 2 of SD_BUF0 is empty at multiple block transfer.

[Clearing conditions]

- When 0 is written to BWE.
- Writing of a block of data to SD_BUF0 by DMA transfer.

When data is written to SD_BUF0 by the CPU, clear BWE and then write the amount of data specified in SD_SIZE.

SD_CLK_CTRLEN flag (SD_CLK_CTRL Write Enable Flag)

When a command sequence is started by writing to SD_CMD, the CBSY bit is set to 1 and, at the same time, the SD_CLK_CTRLEN bit is set to 0. The SD_CLK_CTRLEN bit is set to 1 after 8 cycles of SDCLK have elapsed after the CBSY bit clears to 0 on completion of the command sequence.

ILA flag (Illegal Access Error Detection Flag)

The ILA flag indicates that an illegal access error was detected.

[Setting conditions]

- Writing of data to SD_CMD within a command sequence (CBSY = 1).
- When SD_CMD[11] = 1 (command with data transfer) and SD_CMD[7:0] = 0000 1100b (CMD12) are set in SD_CMD.

[Clearing condition]

- When 0 is written to ILA.

SDD0MON标志（SDHI_D0引脚状态标志）

SDD0MON标志指示SDHI_D0引脚的状态。如果在发出擦除命令后设置了数据超时(DTO)但未设置响应超时(RSPTO)，则通过轮询DAT0确认擦除序列的结束(SDD0MON=1)。

如果在写入序列期间发生通信错误或超时，则DAT0位可能会保留值0。

SDMMC时钟停止时，DAT0位保持时钟停止前的值。

BRE标志（SD_BUF0读使能标志）

BRE标志指示SD_BUF0已启用读取。

[Setting conditions]

- 当SD_SIZE中设置的数据在单块传输时存储在SD_BUF0中时。
- 当SD_SIZE中设置的数据在多块传输时存储在SD_BUF0的bank1或bank2中时。

[Clearing conditions]

- 当0写入BRE
- 通过DMA传输从SD_BUF0读取数据块

当CPU从SD_BUF0读取数据时，清除BRE，然后读取SD_SIZE中指定的数据量。

即使在读取块数据时发生CRC错误或END错误，数据也会存储在SD_BUF0中并设置BRE。

BWE标志（SD_BUF0写使能标志）

BWE标志指示SD_BUF0已启用写入。

[Setting conditions]

- 当SD_BUF0在单块传输时为空时。
- 当SD_BUF0的bank1或bank2在多块传输中为空时。

[Clearing conditions]

- 当0写入BWE时。
- 通过DMA传输将数据块写入SD_BUF0。

当CPU将数据写入SD_BUF0时，清除BWE，然后写入SD_SIZE中指定的数据量。

SD_CLK_CTRLEN标志（SD_CLK_CTRL写使能标志）

当通过写入SD_CMD启动命令序列时，CBSY位设置为1，同时，SD_CLK_CTRLEN位设置为0。SD_CLK_CTRLEN位在SDCLK 的8个周期后设置为1。CBSY位在命令序列完成时清零。

ILA标志（非法访问错误检测标志）

ILA标志表示检测到非法访问错误。

[Setting conditions]

- 在命令序列(CBSY=1)内将数据写入SD_CMD。
- 当SD_CMD[11]=1（带数据传输的命令）且SD_CMD[7:0]=00001100b(CMD12)设置为SD_CMD.

[Clearing condition]

- 当0写入ILA时。

43.2.12 SD INFO1 Interrupt Mask Register (SD_INFO1_MASK)

Address(es): SDHI0.SD_INFO1_MASK 4006 2040h, SDHI1.SD_INFO1_MASK 4006 2440h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	SDD3INM	SDD3RMM	—	—	—	SDCDINM	SDCDRMM	ACENDM	—	RSPENDM
Value after reset:	0	0	0	0	0	0	1	1	0	0	0	1	1	1	0	1

Bit	Symbol	Bit name	Description	R/W
b0	RSPENDM	Response End Interrupt Request Mask	0: Do not mask response end interrupt request 1: Mask response end interrupt request.	R/W
b1	—	Reserved	This bit is read as 0 and cannot be modified.	R
b2	ACENDM	Access End Interrupt Request Mask	0: Do not mask access end interrupt request 1: Mask access end interrupt request.	R/W
b3	SDCDRMM	SDnCD Removal Interrupt Request Mask	0: Do not mask SD card/MMC removal interrupt request by the SDnCD pin 1: Mask SD card/MMC removal interrupt request by the SDnCD pin.	R/W
b4	SDCDINM	SDnCD Insertion Interrupt Request Mask	0: Do not mask SD card/MMC insertion interrupt request by the SDnCD pin 1: Mask SD card/MMC insertion interrupt request by the SDnCD pin.	R/W
b7 to b5	—	Reserved	These bits are read as 0. Writing to these bits has no effect.	R
b8	SDD3RMM	SDnDAT3 Removal Interrupt Request Mask	0: Do not mask SD card/MMC removal interrupt request by the SDnDAT3 pin 1: Mask SD card/MMC removal interrupt request by the SDnDAT3 pin.	R/W
b9	SDD3INM	SDnDAT3 Insertion Interrupt Request Mask	0: Do not mask SD card/MMC insertion interrupt request by the SDnDAT3 pin 1: Mask SD card/MMC insertion interrupt request by the SDnDAT3 pin.	R/W
b31 to b10	—	Reserved	These bits are read as 0. Writing to these bits has no effect.	R

The SD_INFO1_MASK register enables or disables interrupt requests from the status flags in the SD_INFO1 register. See Table 43.5, Interrupt sources, for details on the relationship between the status flags and the requested interrupt source.

43.2.12 SDINFO1中断屏蔽寄存器(SD_INFO1_MASK)

Address(es): SDHI0.SD_INFO1_MASK 4006 2040h, SDHI1.SD_INFO1_MASK 4006 2440h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	SDD3INM	SDD3RMM	—	—	—	SDCDINM	SDCDRMM	ACENDM	—	RSPENDM
重置后的值:	0	0	0	0	0	0	1	1	0	0	0	1	1	1	0	1

Bit	Symbol	位名称	Description	R/W
b0	RSPENDM	响应结束中断请求掩码	0：不屏蔽响应结束中断请求1：屏蔽响应结束中断请求。	R/W
b1	—	Reserved	该位读为0，不能修改。	R
b2	ACENDM	访问结束中断请求Mask	0：不屏蔽访问结束中断请求1：屏蔽访问结束中断请求。	R/W
b3	SDCDRMM	SDnCD移除中断请求掩码	0：不通过SDnCD引脚屏蔽SD卡MMC移除中断请求1：通过SDnCD引脚屏蔽SD卡MMC移除中断请求。	R/W
b4	SDCDINM	SDnCD插入中断请求掩码	0：不通过SDnCD引脚屏蔽SD卡MMC插入中断请求1：通过SDnCD引脚屏蔽SD卡MMC插入中断请求。	R/W
b7 to b5	—	Reserved	这些位被读取为0。写入这些位无效。	R
b8	SDD3RMM	SDnDAT3删除中断请求掩码	0：不通过SDnDAT3引脚屏蔽SD卡MMC移除中断请求1：通过SDnDAT3引脚屏蔽SD卡MMC移除中断请求。	R/W
b9	SDD3INM	SDnDAT3插入中断请求掩码	0：不通过SDnDAT3引脚屏蔽SD卡MMC插入中断请求1：通过SDnDAT3引脚屏蔽SD卡MMC插入中断请求。	R/W
b31 to b10	—	Reserved	这些位被读取为0。写入这些位无效。	R

SD_INFO1_MASK寄存器启用或禁用来自SD_INFO1寄存器中状态标志的中断请求。
有关状态标志和请求的中断源之间关系的详细信息，请参见表43.5，中断源。

43.2.13 SD INFO2 Interrupt Mask Register (SD_INFO2_MASK)

Address(es): SDHI0.SD_INFO2_MASK 4006 2044h, SDHI1.SD_INFO2_MASK 4006 2444h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ILAM	—	—	—	—	—	BWEM	BREM	—	RSPTOM	ILRM	ILWM	DTOM	ENDEM	CRCEM	CMDEM
Value after reset:	1	0	0	0	1	0	1	1	0	1	1	1	1	1	1	1

Bit	Symbol	Bit name	Description	R/W
b0	CMDEM	Command Error Interrupt Request Mask	0: Do not mask command error interrupt request 1: Mask command error interrupt request.	R/W
b1	CRCEM	CRC Error Interrupt Request Mask	0: Do not mask CRC error interrupt request 1: Mask CRC error interrupt request.	R/W
b2	ENDEM	End Bit Error Interrupt Request Mask	0: Do not mask end bit detection error interrupt request 1: Mask end bit detection error interrupt request.	R/W
b3	DTOM	Data Timeout Interrupt Request Mask	0: Do not mask data timeout interrupt request 1: Mask data timeout interrupt request.	R/W
b4	ILWM	SD_BUF0 Register Illegal Write Interrupt Request Mask	0: Do not mask illegal write detection interrupt request for the SD_BUF0 register 1: Mask illegal write detection interrupt request for the SD_BUF0 register.	R/W
b5	ILRM	SD_BUF0 Register Illegal Read Interrupt Request Mask	0: Do not mask illegal read detection interrupt request for the SD_BUF0 register 1: Mask illegal read detection interrupt request for the SD_BUF0 register.	R/W
b6	RSPTOM	Response Timeout Interrupt Request Mask	0: Do not mask response timeout interrupt request 1: Mask response timeout interrupt request.	R/W
b7	—	Reserved	This bit is 0 when read and cannot be modified.	R
b8	BREM	BRE Interrupt Request Mask	0: Do not mask read enable interrupt request for the SD buffer 1: Mask read enable interrupt request for the SD buffer.	R/W
b9	BWEM	BWE Interrupt Request Mask	0: Do not mask write enable interrupt request for the SD_BUF0 register 1: Mask write enable interrupt request for the SD_BUF0 register.	R/W
b10	—	Reserved	This bit is read as 0.	R
b11	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b14 to b12	—	Reserved	These bits are read as 0.	R
b15	ILAM	Illegal Access Error Interrupt Request Mask	0: Do not mask illegal access error interrupt request 1: Mask illegal access error interrupt request.	R/W
b31 to b16	—	Reserved	These bits are read as 0. The write value should be 0.	R

Note 1. When the SD_INFO2_MASK.BWEM bit is 0 or the SD_INFO2_MASK.BREM bit is 0, set the SD_DMAEN.DMAEN bit to 0. When the SD_DMAEN.DMAEN bit is 1, set the SD_INFO2_MASK.BWEM bit to 1 and the SD_INFO2_MASK.BREM bit to 1.

The SD_INFO2_MASK register enables or disables interrupt requests from the status flags in the SD_INFO2 register. See Table 43.5 for details on the relationship between the status flags and the requested interrupt source.

43.2.13 SDINFO2中断屏蔽寄存器(SD_INFO2_MASK)

Address(es): SDHI0.SD_INFO2_MASK 4006 2044h, SDHI1.SD_INFO2_MASK 4006 2444h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ILAM	—	—	—	—	—	BWEM	BREM	—	RSPTOM	ILRM	ILWM	DTOM	ENDEM	CRCEM	CMDEM
重置后的值:	1	0	0	0	1	0	1	1	0	1	1	1	1	1	1	1

Bit	Symbol	位名称	Description	R/W
b0	CMDEM	命令错误中断 请求掩码	0：不屏蔽命令错误中断请求1：屏蔽命令错误中断请求。	R/W
b1	CRCEM	CRC错误中断请求 Mask	0：不屏蔽CRC错误中断请求1：屏蔽CRC错误中断请求。	R/W
b2	ENDEM	结束位错误中断请求 Mask	0：不屏蔽结束位检测错误中断请求1：屏蔽结束位检测错误中断请求。	R/W
b3	DTOM	数据超时中断请求 Mask	0：不屏蔽数据超时中断请求1：屏蔽数据超时中断请求。	R/W
b4	ILWM	SD_BUF0寄存器非法写入中断请求掩码	0：不屏蔽SD_BUF0寄存器的非法写检测中断请求1：屏蔽SD_BUF0寄存器的非法写检测中断请求。	R/W
b5	ILRM	SD_BUF0寄存器非法读取中断请求掩码	0：不屏蔽SD_BUF0寄存器的非法读检测中断请求1：屏蔽SD_BUF0寄存器的非法读检测中断请求。	R/W
b6	RSPTOM	响应超时中断 请求掩码	0：不屏蔽响应超时中断请求1：屏蔽响应超时中断请求。	R/W
b7	—	Reserved	该位读取时为0，不能修改。	R
b8	BREM	BRE中断请求掩码	0：不屏蔽SD缓冲区的读使能中断请求1：屏蔽SD缓冲区的读使能中断请求。	R/W
b9	BWEM	BWE中断请求掩码	0：不屏蔽SD_BUF0寄存器的写使能中断请求1：屏蔽SD_BUF0寄存器的写使能中断请求。	R/W
b10	—	Reserved	该位读为0。	R
b11	—	Reserved	该位读取为1。写入值应为1。	R/W
b14 to b12	—	Reserved	这些位读为0。	R
b15	ILAM	非法访问错误中断 请求掩码	0：不屏蔽非法访问错误中断请求1：屏蔽非法访问错误中断请求。	R/W
b31 to b16	—	Reserved	这些位被读取为0。写入值应为0。	R

Note 1. 当SD_INFO2_MASK.BWEM位为0或SD_INFO2_MASK.BREM位为0时，将SD_DMAEN.DMAEN位设置为0。当SD_DMAEN.DMAEN位为1时，将SD_INFO2_MASK.BWEM位设置为1，SD_INFO2_MASK.BREM位设置为1.

SD_INFO2_MASK寄存器启用或禁用来自SD_INFO2寄存器中状态标志的中断请求。
有关状态标志和请求中断源之间关系的详细信息，请参见表43.5。

43.2.14 SD Clock Control Register (SD_CLK_CTRL)

Address(es): SDHI0.SD_CLK_CTRL 4006 2048h, SDHI1.SD_CLK_CTRL 4006 2448h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	CLKCTRLEN	CLKEN	CLKSEL[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	CLKSEL[7:0]	SDHI Clock Frequency Select*1	b7 b0 0 0 0 0 0 0 0 0: PCLKA/2 0 0 0 0 0 0 0 1: PCLKA/4 0 0 0 0 0 0 1 0: PCLKA/8 0 0 0 0 0 1 0 0: PCLKA/16 0 0 0 0 1 0 0 0: PCLKA/32 0 0 0 1 0 0 0 0: PCLKA/64 0 0 1 0 0 0 0 0: PCLKA/128 0 1 0 0 0 0 0 0: PCLKA/256 1 0 0 0 0 0 0 0: PCLKA/512. Other settings are prohibited.	R/W
b8	CLKEN	SD/MMC Clock Output Control*1	0: Disable SD/MMC clock output (fix SDnCLK signal low) 1: Enable SD/MMC clock output.	R/W
b9	CLKCTRLEN	SD/MMC Clock Output Automatic Control Select	0: Disable automatic control of SD/MMC clock output 1: Enable automatic control of SD/MMC clock output.	R/W
b31 to b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Bits CLKSEL[7:0] and CLKEN cannot be write accessed when the SD_INFO2.SD_CLK_CTRLEN flag is 0.

The SDCLKCTRL register controls the SD/MMC clock frequency settings and output. Set the CLKEN bit to 1 before writing to the SD_CMD register to start a command sequence. Do not write to the SDCLKCTRL register when the SD_INFO2.SD_CLK_CTRLEN flag is 0.

CLKCTRLEN bit (SD/MMC Clock Output Automatic Control Select)

The CLKCTRLEN bit enables or disables the automatic control function for SD/MMC clock output, which causes the SD/MMC clock to output only within a command sequence.

The timing with which SD/MMC clock output starts and stops is as follows:

- SD/MMC clock output starts after writing to SD_CMD
- SD/MMC clock output stops when 8 cycles of SD/MMC clock have elapsed after the end of the command sequence.

In addition, SD/MMC clock is fixed to 0 while CLKEN of SD_CLK_CTRL is 0, regardless of the value of this bit.

43.2.14 SD时钟控制寄存器(SD_CLK_CTRL)

Address(es): SDHI0.SD_CLK_CTRL 4006 2048h, SDHI1.SD_CLK_CTRL 4006 2448h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	CLKCTRLEN	CLKEN	CLKSEL[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b7 to b0	CLKSEL[7:0]	SDHI时钟频率 Select*1	b7b000000000：PCLKA200 000001：PCLKA400000010 ：PCLKA800000100：PCLK A1600001000：PCLKA3200 010000：PCLKA640010000 0：PCLKA12801000000：P CLKA25610000000：PCLKA 512.禁止其他设置。	R/W
b8	CLKEN	SDMMC时钟输出 Control*1	0：禁用SDMMC时钟输出（固定SDnCLK信号为低电平） 1：启用SDMMC时钟输出。	R/W
b9	CLKCTRLEN	SDMMC时钟输出自动控制选择	0：禁止SDMMC时钟输出自动控制1：使能SDMMC时钟输出自动控制。	R/W
b31 to b10	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 当SD_INFO2.SD_CLK_CTRLEN标志为0时，不能写访问位CLKSEL[7:0]和CLKEN。

SDCLK CTRL寄存器控制SDMMC时钟频率设置和输出。在写入SD_CMD寄存器以启动命令序列之前，将CLKEN位设置为1。当SD_INFO2.SD_CLK_CTRLEN标志为0时，不要写入SDCLK CTRL寄存器。

CLKCTRLEN位（SDMMC时钟输出自动控制选择）

CLKCTRLEN位启用或禁用SDMMC时钟输出的自动控制功能，这会导致SDMMC时钟仅在命令序列内输出。

SDMMC时钟输出开始和停止的时序如下：

- SDMMC时钟输出在写入SD_CMD后开始
- 在命令序列结束后经过8个SDMMC时钟周期时，SDMMC时钟输出停止。

此外，SDMMC时钟固定为0，而SD_CLK_CTRL的CLKEN为0，与该位的值无关。

43.2.15 Transfer Data Length Register (SD_SIZE)

Address(es): SDHI0.SD_SIZE 4006 204Ch, SDHI1.SD_SIZE 4006 244Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	LEN[9:0]									
Value after reset:	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b9 to b0	LEN[9:0]	Transfer Data Size Setting	These bits specify the transfer data size.*1	R/W
b31 to b10	—	Reserved	These bits are read as 0. The write value should be 0.	R

Note 1. Do not rewrite these bits when the SD_INFO2.CBSY flag is 1.

The SD_SIZE register sets the transfer data size.

LEN[9:0] bits (Transfer Data Size Setting)

When using single block transfer, the transfer data size can be set in the LEN[9:0] bits from 1 byte to 512 bytes. When CMD12 is automatically issued during a multiblock transfer sequence (CMD18 and CMD25), the transfer data size can only be set to 512 bytes. When CMD12 is not automatically issued during a multiblock transfer sequence, the transfer data size can be set to 32, 64, 128, 256, or 512 bytes. However, a 32-, 64-, 128-, or 256-byte multiblock read transfer can only be performed during an SDIO multiblock transfer (CMD53). Do not set these bits to 0 when using a command that includes data transfer.

43.2.16 SD Card Access Control Option Register (SD_OPTION)

Address(es): SDHI0.SD_OPTION 4006 2050h, SDHI1.SD_OPTION 4006 2450h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	WIDTH	—	WIDTH8	—	—	—	—	TOUTMASK	TOP[3:0]				CTOP[3:0]			
Value after reset:	0*2	1	0*2	0	0	0	0	0*2	1*2	1*2	1*2	0*2	1*2	1*2	1*2	0*2

Bit	Symbol	Bit name	Description	R/W
b3 to b0	CTOP[3:0]	Card Detection Time Counter *1	b3 b0 0 0 0 0: PCLKA × 2^{10} 0 0 0 1: PCLKA × 2^{11} 0 0 1 0: PCLKA × 2^{12} 0 0 1 1: PCLKA × 2^{13} 0 1 0 0: PCLKA × 2^{14} 0 1 0 1: PCLKA × 2^{15} 0 1 1 0: PCLKA × 2^{16} 0 1 1 1: PCLKA × 2^{17}. 1 0 0 0: PCLKA × 2^{18} 1 0 0 1: PCLKA × 2^{19} 1 0 1 0: PCLKA × 2^{20} 1 0 1 1: PCLKA × 2^{21} 1 1 0 0: PCLKA × 2^{22} 1 1 0 1: PCLKA × 2^{23} 1 1 1 0: PCLKA × 2^{24} 1 1 1 1: Setting prohibited.	R/W

43.2.15 传输数据长度寄存器(SD_SIZE)

Address(es): SDHI0.SD_SIZE 4006 204Ch, SDHI1.SD_SIZE 4006 244Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	LEN[9:0]									
重置后的值:	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b9 to b0	LEN[9:0]	传输数据大小设置	这些位指定传输数据大小。*1	R/W
b31 to b10	—	Reserved	这些位被读取为0。写入值应为0。	R

Note 1. 当SD_INFO2.CBSY标志为1时，不要重写这些位。

SD_SIZE寄存器设置传输数据大小。

LEN[9:0]位（传输数据大小设置）

使用单块传输时，传输数据大小可以在LEN[9:0]位中设置，从1字节到512字节。在多块传输序列（CMD18和CMD25）期间自动发出CMD12时，传输数据大小只能设置为512字节。在多块传输序列期间未自动发出CMD12时，传输数据大小可设置为32、64、128、256或512字节。但是，只能在SDIO多块传输(CMD53)期间执行32、64、128或256字节的多块读取传输。使用包含数据传输的命令时，请勿将这些位设置为0。

43.2.16 SD卡访问控制选项寄存器(SD_OPTION)

Address(es): SDHI0.SD_OPTION 4006 2050h, SDHI1.SD_OPTION 4006 2450h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	WIDTH	—	WIDTH8	—	—	—	—	TOUTMASK	TOP[3:0]				CTOP[3:0]			
重置后的值:	0*2	1	0*2	0	0	0	0	0*2	1*2	1*2	1*2	0*2	1*2	1*2	1*2	0*2

Bit	Symbol	位名称	Description	R/W
b3 to b0	CTOP[3:0]	卡片检测时间计数器*1	b3 b0 0 0 0 0: PCLKA × 2^{10} 0 0 0 1: PCLKA × 2^{11} 0 0 1 0: PCLKA × 2^{12} 0 0 1 1: PCLKA × 2^{13} 0 1 0 0: PCLKA × 2^{14} 0 1 0 1: PCLKA × 2^{15} 0 1 1 0: PCLKA × 2^{16} 0 1 1 1: PCLKA × 2^{17}. b3b01000：PCLKA×2181 001：PCLKA×2191010： PCLKA×2201011：PCLKA ×2211100：PCLKA×2221 101：PCLKA×2231110： PCLKA×2241111：禁止设 置。	R/W

Bit	Symbol	Bit name	Description	R/W
b7 to b4	TOP[3:0]	Timeout Counter*1	b7 b4 0 0 0 0: SDHI clock × 2^{13} 0 0 0 1: SDHI clock × 2^{14} 0 0 1 0: SDHI clock × 2^{15} 0 0 1 1: SDHI clock × 2^{16} 0 1 0 0: SDHI clock × 2^{17} 0 1 0 1: SDHI clock × 2^{18} 0 1 1 0: SDHI clock × 2^{19} 0 1 1 1: SDHI clock × 2^{20}. b7 b4 1 0 0 0: SDHI clock × 2^{21} 1 0 0 1: SDHI clock × 2^{22} 1 0 1 0: SDHI clock × 2^{23} 1 0 1 1: SDHI clock × 2^{24} 1 1 0 0: SDHI clock × 2^{25} 1 1 0 1: SDHI clock × 2^{26} 1 1 1 0: SDHI clock × 2^{27} 1 1 1 1: Setting prohibited.	R/W
b8	TOUTMASK	Timeout Mask	0: Activate timeout 1: Inactivate timeout (do not set RSPTO and DTO bits of SD_INFO2 or E6 to E0 bits of SDERRSTS2). When timeout occurs because of an inactivated timeout, execute a software reset to terminate the command sequence.	R/W
b12 to b9	—	Reserved	These bits are read as 0.	R
b13	WIDTH8*2	Bus Width	See bit 15 WIDTH bit.	R/W
b14	—	Reserved	This bit is read as 1.	R
b15	WIDTH	Bus Width*2	b15 b13 0 1: 8-bit width 0 0: 4-bit width 1 0: 1-bit width 1 1: 1-bit width. For 1-byte write transfers, set 4-bit or 1-bit width. Do not set 8-bit width.	R/W
b31 to b16	—	Reserved	These bits are read as 0.	R

Note 1. Do not rewrite these bits when the SD_INFO2.CBSY flag is 1.
Note 2. The initial value is applied at a reset and when the SOFT_RST.SDRST flag is 0.
The SD bus width and timeout counter are set in the SD_OPTION register.

43.2.17 SD Error Status Register 1 (SD_ERR_STS1)

Address(es): SDHI0.SD_ERR_STS1 4006 2058h, SDHI1.SD_ERR_STS1 4006 2458h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	CRCTK[2:0]			CRCTK E	RDCR CE	RSPCR CE1	RSPCR CE0	—	—	CRCLE NE	RDLEN E	RSPLE NE1	RSPLE NE0	CMDE1	CMDE0
Value after reset:	0	0*3	1*3	0*3	0*3	0*3	0*3	0*3	0	0	0*3	0*3	0*3	0*3	0*3	0*3

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b0	CMDE0	Command Error Flag 0	0: No error exists in command index field value of a command*1 response 1: Error exists in command index field value of a command*1 response.	R
b1	CMDE1	Command Error Flag 1	0: No error exists in command index field value of a command*2 response 1: Error exists in command index field value of a command*2 response (with SD_CMD.CMDIDX[5:0] setting, an error that occurs with CMD12 issue is indicated in the CMDE0 flag).	R
b2	RSPLENE0	Response Length Error Flag 0	0: No error exists in command*1 response length 1: Error exists in command*1 response length.	R

Bit	Symbol	位名称	Description	R/W
b7 to b4	TOP[3:0]	Timeout Counter*1	b7 b4 0 0 0 0: SDHI clock × 2^{13} 0 0 0 1: SDHI clock × 2^{14} 0 0 1 0: SDHI clock × 2^{15} 0 0 1 1: SDHI clock × 2^{16} 0 1 0 0: SDHI clock × 2^{17} 0 1 0 1: SDHI clock × 2^{18} 0 1 1 0: SDHI clock × 2^{19} 0 1 1 1: SDHI clock × 2^{20}. b7b41000：SDHI时钟×2211001：SDHI时钟×2221010：SDHI时钟×2231011：SDHI时钟×2241100：SDHI时钟×2251101：SDHI时钟×2261110：SDHI时钟×2271111：禁止设置。	R/W
b8	TOUTMASK	超时掩码	0：激活超时1：禁用超时（不要将SD_INFO2的RSPTO和DTO位或SDERRSTS2的E6设置为E0位）。 当由于未激活超时而发生超时时，执行软件复位以终止命令序列。	R/W
b12 to b9	—	Reserved	这些位读为0。	R
b13	WIDTH8*2	总线宽度	请参见位15WIDTH位。	R/W
b14	—	Reserved	该位读为1。	R
b15	WIDTH	Bus Width*2	b15b1301：8位宽00：4位宽10：1位宽11：1位宽。对于1字节写传输，设置4位或1位宽度。不要设置8位宽度。	R/W
b31 to b16	—	Reserved	这些位读为0。	R

Note 1. 当SD_INFO2.CBSY标志为1时，不要重写这些位。
Note 2. 初始值在复位时和SOFT_RST.SDRST标志为0时应用。
SD总线宽度和超时计数器在SD_OPTION寄存器中设置。

43.2.17 SD错误状态寄存器1(SD_ERR_STS1)

Address(es): SDHI0.SD_ERR_STS1 4006 2058h, SDHI1.SD_ERR_STS1 4006 2458h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	CRCTK[2:0]			CRCTK E	RDCR CE	RSPCR CE1	RSPCR CE0	—	—	CRCLE NE	RDLEN E	RSPLE NE1	RSPLE NE0	CMDE1	CMDE0
重置后的值:	0	0*3	1*3	0*3	0*3	0*3	0*3	0*3	0	0	0*3	0*3	0*3	0*3	0*3	0*3

x: Undefined

Bit	Symbol	位名称	Description	R/W
b0	CMDE0	命令错误标志0	0：命令*1响应的命令索引字段值不存在错误1：命令*1响应的命令索引字段值存在错误。	R
b1	CMDE1	命令错误标志1	0：命令的命令索引字段值不存在错误*2响应1：命令的命令索引字段值存在错误*2响应（使用SD_CMD.CMDIDX[5:0]设置，CMD12问题发生的错误在CMDE0标志中指示）。	R
b2	RSPLENE0	响应长度错误标志0	0：命令*1响应长度中不存在错误1：命令*1响应长度中存在错误。	R

Bit	Symbol	Bit name	Description	R/W
b3	RSPLENE1	Response Length Error Flag 1	0: No error exists in command*2 response length 1: Error exists in command*2 response length (with SD_CMD.CMDIDX[5:0] setting, an error that occurs with CMD12 issue is indicated in the RSPLENE0 flag).	R
b4	RDLENE	Read Data Length Error Flag	0: No read data length error occurred 1: Read data length error occurred.	R
b5	CRCLENE	CRC Status Token Length Error Flag	0: No CRC status token length error occurred 1: CRC status token length error occurred.	R
b7, b6	—	Reserved	These bits are read as 0.	R
b8	RSPCRCE0	Response CRC Error Flag 0	0: No CRC error detected in command*1 response 1: CRC error detected in command*1 response.	R
b9	RSPCRCE1	Response CRC Error Flag 1	0: No CRC error detected in command*2 response (with SD_CMD.CMDIDX[5:0] setting, an error that occurs with CMD12 issue is indicated in the RSPCRCE0 flag) 1: CRC error detected in command*2 response.	R
b10	RDCRCE	Read Data CRC Error Flag	0: No CRC error detected in read data 1: CRC error detected in read data.	R
b11	CRCTKE	CRC Status Token Error Flag	0: No error detected in CRC status token 1: Error detected in CRC status token.	R
b14 to b12	CRCTK[2:0]	CRC Status Token	These bits store the CRC status token value (normal value is 010b).	R
b15	—	Reserved	This bit is read as 0	R
b31 to b16	—	Reserved	These bits are read as undefined	R

Note 1. CMD other than CMD12 when automatic issuing is enabled for multiple block transfer by the setting in SD_CMD, CMD12 when the STP bit in SD_STOP is set to 1, or CMD52 when the C52PUB or IOABT bit in SDIO_MODE is set to 1.
Note 2. CMD12 when automatic issuing is enabled for multiple block transfer by the setting in SD_CMD, CMD12 when the STP bit in SD_STOP is set to 1, or CMD52 when the C52PUB or IOABT bit in SDIO_MODE is set to 1.
Note 3. The initial value is applied at a reset and when the SOFT_RST.SDRST flag is 0.

The SD_ERR_STS1 register indicates the CRC status token, CRC error, end bit error, and command error.

43.2.18 SD Error Status Register 2 (SD_ERR_STS2)

Address(es): SDHI0.SD_ERR_STS2 4006 205Ch, SDHI1.SD_ERR_STS2 4006 245Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	CRCBSYTO	CRCTO	RDTO	BSYTO1	BSYTO0	RSPTO1	RSPTO0
Value after reset:	0	0	0	0	0	0	0	0	0	0*4	0*4	0*4	0*4	0*4	0*4	0*4

Bit	Symbol	Bit name	Description	R/W
b0	RSPTO0	Response Timeout Flag 0	0: After command*1 was issued, response was received in less than 640 cycles of the SD/MMC clock 1: After command*1 was issued, response was not received in 640 or more cycles of the SD/MMC clock.	R
b1	RSPTO1	Response Timeout Flag 1	0: After command*2 was issued, response was received in less than 640 cycles of the SD/MMC clock 1: After command*2 was issued, response was not received after 640 or more cycles of the SD/MMC clock (with SD_CMD.CMDIDX[5:0] setting, an error that occurs with CMD12 issue is indicated in the RSPTO0 flag).	R

Bit	Symbol	位名称	Description	R/W
b3	RSPLENE1	响应长度错误标志1	0：命令中不存在错误*2响应长度1：命令中存在错误*2响应长度（带SD_CMD.CMDIDX[5:0]设置，出现错误CMD12问题在RSPLENE0标志中指示）。	R
b4	RDLENE	读取数据长度错误标志	0：未发生读取数据长度错误1：发生读取数据长度错误。	R
b5	CRCLENE	CRC状态令牌长度错误标志	0：未发生CRC状态令牌长度错误1：发生CRC状态令牌长度错误。	R
b7, b6	—	Reserved	这些位读为0。	R
b8	RSPCRCE0	响应CRC错误标志0	0：在命令*1个响应中未检测到CRC错误1：在命令*1个响应中检测到CRC错误。	R
b9	RSPCRCE1	响应CRC错误标志1	0：在命令*2响应中未检测到CRC错误（带有SD_CMD.CMDIDX[5:0]设置，出现错误CMD12问题在RSPCRCE0标志中指示）1：在命令*2响应中检测到CRC错误。	R
b10	RDCRCE	读取数据CRC错误标志	0：读取数据中未检测到CRC错误1：读取数据中检测到CRC错误。	R
b11	CRCTKE	CRC状态令牌错误标志	0：在CRC状态令牌中未检测到错误1：在CRC状态令牌中检测到错误。	R
b14 to b12	CRCTK[2:0]	CRC状态令牌	这些位存储CRC状态令牌值（正常值为010b）。	R
b15	—	Reserved	该位读为0	R
b31 to b16	—	Reserved	这些位被读取为未定义	R

Note 1. 通过SD_CMD中的设置为多块传输启用自动发布时的CMD12以外的CMD，当SD_STOP中的STP位设置为1时为CMD12，或者当SDIO_MODE中的C52PUB或IOABT位设置为1时为CMD52。
Note 2. 通过SD_CMD中的设置为多块传输启用自动发布时的CMD12，当STP位中的CMD12 SD_STOP设置为1，或当SDIO_MODE中的C52PUB或IOABT位设置为1时为CMD52。
Note 3. 初始值在复位时和SOFT_RST.SDRST标志为0时应用。

SD_ERR_STS1寄存器指示CRC状态令牌、CRC错误、结束位错误和命令错误。

43.2.18 SD错误状态寄存器2(SD_ERR_STS2)

Address(es): SDHI0.SD_ERR_STS2 4006 205Ch, SDHI1.SD_ERR_STS2 4006 245Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	CRCBSYTO	CRCTO	RDTO	BSYTO1	BSYTO0	RSPTO1	RSPTO0
重置后的值：	0	0	0	0	0	0	0	0	0	0*4	0*4	0*4	0*4	0*4	0*4	0*4

Bit	Symbol	位名称	Description	R/W
b0	RSPTO0	响应超时标志0	0：发出命令*1后，在SDMMC时钟的640个周期内收到响应1：发出命令*1后，在SDMMC时钟的640或更多周期内未收到响应。	R
b1	RSPTO1	响应超时标志1	0：发出命令*2后，在SDMMC时钟的640个周期内收到响应1：发出命令*2后，在SDMMC时钟的640个或更多周期后未收到响应（使用SD_CMD.CMDIDX[5:0]设置，在RSPTO0标志中指示CMD12问题发生的错误）。	R

Bit	Symbol	Bit name	Description	R/W
b2	BSYTO0	Busy Timeout Flag 0	0: After R1b response was received, SD/MMC was released from the busy state during the specified period*3 1: After R1b response was received, SD/MMC was in the busy state after the specified period*3 elapsed.	R
b3	BSYTO1	Busy Timeout Flag 1	0: After CMD12 was automatically issued, SD/MMC was released from the busy state during the specified period*3 1: After CMD12 was automatically issued, SD/MMC was in the busy state after the specified period*3 elapsed (with SD_CMD.CMDIDX[5:0] setting, an error that occurs with CMD12 issue is indicated in the BSYTO0 flag).	R
b4	RDTO	Read Data Timeout Flag	When a read command is issued, this flag sets to 1 when read data is not received after the specified period*3 elapses. When read data is received, this flag sets to 1 when the next block of read data is not received after the specified period*3 elapses. When the SD/MMC exits the read wait state, this flag sets to 1 when the next block of read data is not received after the specified period*3 elapses.	R
b5	CRCTO	CRC Status Token Timeout Flag	0: After CRC data was written to the SD card/MMC, a CRC status token was received during the specified period*3 1: After CRC data was written to the SD card/MMC, a CRC status token was not received after the specified period*3 elapsed.	R
b6	CRCBSYTO	CRC Status Token Busy Timeout Flag	0: After a CRC status token was received, the SD/MMC was released from the busy state during the specified period*3 1: After a CRC status token was received, the SD/MMC was in the busy state after the specified period*3 elapsed.	R
b31 to b7	—	Reserved	These bits are read as 0.	R

Note 1. CMD other than CMD12 when automatic issuing is enabled for multiple block transfer by the setting in SD_CMD, CMD12 when the STP bit in SD_STOP is set to 1, or CMD52 when the C52PUB or IOABT bit in SDIO_MODE is set to 1.
Note 2. CMD12 when automatic issuing is enabled for multiple block transfer by the setting in SD_CMD, CMD12 when the STP bit in SD_STOP is set to 1, or CMD52 when the C52PUB or IOABT bit in SDIO_MODE is set to 1.
Note 3. Set the SD_OPTION.TOP[3:0] bits to select the number of *n* cycles.
Note 4. The initial value is applied at a reset and when the SOFT_RST.SDRST flag is 0.

The SD_ERR_STS2 register indicates the timeout status.

43.2.19 SD Buffer Register (SD_BUF0)

Address(es): SDHI0.SD_BUF0 4006 2060h, SDHI1.SD_BUF0 4006 2460h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

When writing to the SD card, the write data is written to this register. When reading from the SD card, the read data is read from this register. This register is internally connected to two 512-byte buffers.

If both buffers are not empty when executing multiple block read, the SD card/MMC clock is stopped to suspend receiving data. When one of the buffers is empty, the SD card/MMC clock is supplied to resume receiving data.

Bit	Symbol	位名称	Description	R/W
b2	BSYTO0	忙超时标志0	0：收到R1b响应后，SDMMC在指定时间段内从忙状态释放*31：收到R1b响应后，SDMMC在指定时间段后处于忙状态*3过去。	R
b3	BSYTO1	忙超时标志1	0：CMD12自动下发后，SDMMC在指定时间段内从忙状态释放*31：CMD12自动下发后，SDMMC在指定时间段后处于忙状态*3过去（带SD_CMD.CMDIDX[5:0]设置，在BSYTO0标志中指示CMD12问题发生的错误）。	R
b4	RDTO	读取数据超时标志	当发出读取命令时，如果在指定时间段*3过去后未接收到读取数据，则此标志设置为1。当接收到读取数据时，如果经过指定的时间*3后没有接收到下一个读取数据块，则此标志设置为1。当SDMMC退出读取等待状态时，如果经过指定时间*3后未接收到下一个读取数据块，此标志设置为1。	R
b5	CRCTO	CRC状态令牌超时标志	0：CRC数据写入SD卡MMC后，在指定时间段内收到CRC状态令牌*31：CRC数据写入SD卡MMC后，在指定时间段内未收到CRC状态令牌*3过去了。	R
b6	CRCBSYTO	CRC状态令牌忙超时标志	0：收到CRC状态令牌后，SDMMC在指定时间段内从忙碌状态释放*31：在收到CRC状态令牌后，SDMMC在指定时间段后处于忙碌状态*3已过.	R
b31 to b7	—	Reserved	这些位读为0。	R

Note 1. 通过SD_CMD中的设置为多块传输启用自动发布时的CMD12以外的CMD，当SD_STOP中的STP位设置为1时为CMD12，或者当SDIO_MODE中的C52PUB或IOABT位设置为1时为CMD52。
Note 2. 通过SD_CMD中的设置为多块传输启用自动发布时的CMD12，当STP位中的CMD12 SD_STOP设置为1，或当SDIO_MODE中的C52PUB或IOABT位设置为1时为CMD52。
Note 3. 设置SD_OPTION.TOP[3:0]位以选择n个周期数。
Note 4. 初始值在复位时和SOFT_RST.SDRST标志为0时应用。

SD_ERR_STS2寄存器指示超时状态。

43.2.19 SD缓冲寄存器(SD_BUF0)

Address(es): SDHI0.SD_BUF0 4006 2060h, SDHI1.SD_BUF0 4006 2460h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

x: Undefined

写入SD卡时，写入数据写入该寄存器。从SD卡读取时，从该寄存器读取读取的数据。该寄存器在内部连接到两个512字节的缓冲区。

如果执行多块读取时两个缓冲区都不为空，则停止SD卡MMC时钟以暂停接收数据。当其中一个缓冲区为空时，提供SD卡MMC时钟以恢复接收数据。

43.2.20 SDIO Mode Control Register (SDIO_MODE)

Address(es): SDHI0.SDIO_MODE 4006 2068h, SDHI1.SDIO_MODE 4006 2468h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	C52PUB	IOABT	—	—	—	—	—	RWREQ	—	INTEN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	INTEN	SDIO Interrupt Acceptance Enable*1	0: Disable SDIO interrupt acceptance 1: Enable SDIO interrupt acceptance.	R/W
b1	—	Reserved	This bit is read as 0.	R
b2	RWREQ	Read Wait Request	0: Allow SD/MMC to exit read wait state 1: Request for SD/MMC to enter read wait state.	R/W
b7 to b3	—	Reserved	These bits are read as 0.	R
b8	IOABT	SDIO Abort	If this bit is set to 1 during multiblock transfer triggered by CMD53, CMD52 is immediately issued, and the command sequence is aborted.	R/W
b9	C52PUB	SDIO None Abort	If this bit is set to 1 during multiblock transfer triggered by CMD53, CMD52 is issued after the transfer process is complete, and the command sequence is completed.	R/W
b31 to b10	—	Reserved	These bits are read as 0.	R

Note 1. Do not rewrite this bit when the SD_INFO2.CBSY flag is 1.

The SDIO_MODE register controls reception of the SDIO interrupt, CMD52 issuance during multiblock transfer, and read wait request. Do not set bits C52PUB and IOABT to 1 at the same time.

RWREQ bit (Read Wait Request)

When RWREQ is set to 1 in the CMD53 (multiple block) read sequence, the block transfer enters the read wait state between blocks.

[Read wait state releasing]

- The read wait state is released, when RWREQ is cleared to 0 in the read wait state.
- When IOABT is set to 1 in the read wait state, RWREQ is automatically cleared to 0 after CMD52 is issued, and then the read wait state is released.
- When C52PUB and RWREQ are set to 1 simultaneously in the CMD53 (multiple block) read sequence, the read wait state is not automatically released. Therefore, after the CMD52 response is received, clear RWREQ. You must set RWREQ and C52PUB simultaneously.

When RWREQ is set to 1 while the last block in the CMD53 (multiple block) read sequence is transferred, the read wait state is not entered and RWREQ is automatically cleared to 0 by setting access end. Set RWREQ to 1 after the response end flag sets.

IOABT bit (SDIO Abort)

When the IOABT bit is set to 1 in a CMD53 (multiple block) sequence, the CMD53 sequence is halted and CMD52 is issued. However, if a command sequence is halted because of a communication error or timeout, CMD52 is not issued. Although continued buffer access is possible even after IOABT is set to 1, the buffer access error bit (ILR or ILW) in SD_INFO2 is set accordingly. Set SD_ARG before setting IOABT to 1.

43.2.20 SDIO模式控制寄存器(SDIO_MODE)

Address(es): SDHI0.SDIO_MODE 4006 2068h, SDHI1.SDIO_MODE 4006 2468h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	C52PUB	IOABT	—	—	—	—	—	RWREQ	—	INTEN
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	INTEN	SDIO中断接受Enable*1	0：禁止SDIO中断接受1：使能SDIO中断接受。	R/W
b1	—	Reserved	该位读为0。	R
b2	RWREQ	读取等待请求	0：允许SDMMC退出读取等待状态1：请求SDMMC进入读取等待状态。	R/W
b7 to b3	—	Reserved	这些位读为0。	R
b8	IOABT	SDIO Abort	如果在CMD53触发的多块传输期间该位设置为1，立即发出CMD52，并中止命令序列。	R/W
b9	C52PUB	SDIO无中止	如果在CMD53触发的多块传输期间该位设置为1，传输过程完成后发出CMD52，命令序列完成。	R/W
b31 to b10	—	Reserved	这些位读为0。	R

Note 1. 当SD_INFO2.CBSY标志为1时，不要重写该位。

SDIO_MODE寄存器控制SDIO中断的接收、多块传输期间CMD52的发布和读取等待请求。不要同时将位C52PUB和IOABT设置为1。

RWREQ位（读取等待请求）

当CMD53（多块）读取序列中RWREQ设置为1时，块传输进入块之间的读取等待状态。

[读取等待状态释放]

- 当RWREQ在读等待状态下被清除为0时，读等待状态被释放。
- 当IOABT在读等待状态下置1时，RWREQ在发出CMD52后自动清0，然后解除读等待状态。
- 当C52PUB和RWREQ在CMD53（多块）读取序列中同时设置为1时，读取等待状态不会自动释放。因此，在收到CMD52响应后，清除RWREQ。您必须同时设置RWREQ和C52PUB。

当RWREQ设置为1时CMD53（多块）读取序列中的最后一个块被传输时，不会进入读取等待状态，并且通过设置访问结束将RWREQ自动清除为0。设置响应结束标志后将RWREQ设置为1。

IOABT位（SDIO中止）

当CMD53（多块）序列中的IOABT位设置为1时，CMD53序列停止并发出CMD52。但是，如果命令序列由于通信错误或超时而停止，则不会发出CMD52。尽管即使在IOABT设置为1后仍可以继续访问缓冲区，但缓冲区访问错误位（ILR或ILW）在

SD_INFO2相应设置。在将IOABT设置为1之前设置SD_ARG。

When IOABT is set to 1 during transfer for a single block write, the access end flag sets when SD_BUF0 becomes empty, and CMD52 is not issued. If SD_BUF0 contains data, the access end flag sets on completion of reception of the busy state without CMD52 being issued.

When IOABT is set to 1 during transfer for single block read, the access end flag sets immediately after IOABT is set, and CMD52 is not issued.

When IOABT is set to 1 during reception of the busy state after an R1b response, the access end flag sets on completion of reception of the busy state without CMD52 being issued.

When IOABT is set to 1 after a command sequence is completed, CMD52 is not issued and the access end flag does not set.

Set IOABT to 1 after the response end flag sets.

Set IOABT to 0 after the access end flag sets.

C52PUB bit (SDIO None Abort)

When the C52PUB bit is set to 1 in the CMD53 (multiple block) write sequence, CMD52 is automatically issued between blocks if SD_BUF0 becomes empty. C52PUB is automatically cleared to 0 after reception of the response to CMD52 is completed. Additionally, if C52PUB is set to 1 while the last block is being transferred, CMD52 is not issued. In this case, C52PUB is automatically cleared to 0 after the access end flag sets to 1.

When C52PUB and RWREQ are set to 1 in the CMD53 (multiple block) read sequence, the block transfer enters the read wait state between blocks and CMD52 is automatically issued. C52PUB is automatically cleared to 0 after reception of the response to CMD52 is completed. Additionally, if C52PUB is set to 1 while the last block is being transferred, CMD52 is not issued. In this case, C52PUB is automatically cleared to 0 after the access end flag sets to 1.

If C52PUB is set to 1 in the CMD53 (multiple block) read sequence, you must set RWREQ to 1 in addition to C52PUB.

Set SD_ARG before setting C52PUB to 1.

Set C52PUB to 1 after the response end flag sets.

43.2.21 SDIO Interrupt Flag Register (SDIO_INFO1)

Address(es): SDHI0.SDIO_INFO1 4006 206Ch, SDHI1.SDIO_INFO1 4006 246Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	EXWT	EXPUB52	—	—	—	—	—	—	—	—	—	—	—	—	—	IOIRQ
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	x	x	0

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b0	IOIRQ	SDIO Interrupt Status Flag	0: No SDIO interrupt detected 1: SDIO interrupt detected.	R(/W)*1
b2, b1	—	Reserved	The read value is undefined. The write value should be 1.	R/W
b13 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b14	EXPUB52	EXPUB52 Status Flag	Indicates the status of the EXPUB52.	R(/W)*1
b15	EXWT	EXWT Status Flag	Indicates the status of the EXWT.	R(/W)*1
b31 to b16	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Only 0 can be written to clear the bit.

The SDIO_INFO1 register indicates the status of the SDIO card access. Set flags to be cleared to 0. Set flags that are not

当IOABT在单块写入传输期间设置为1时，SD_BUF0变为空时设置访问结束标志，并且不发出CMD52。如果SD_BUF0包含数据，则在未发出CMD52的忙状态接收完成时设置访问结束标志。

当IOABT在单块读取传输期间设置为1时，在设置IOABT后立即设置访问结束标志，并且不发出CMD52。

如果在R1b响应后接收忙碌状态期间将IOABT设置为1，则在没有发出CMD52的情况下完成忙碌状态接收时设置访问结束标志。

当命令序列完成后IOABT设置为1时，不发出CMD52并且不设置访问结束标志。

设置响应结束标志后将IOABT设置为1。

设置访问结束标志后将IOABT设置为0。

C52PUB位（SDIO无中止）

在CMD53（多块）写入序列中将C52PUB位设置为1时，如果SD_BUF0为空，则在块之间自动发出CMD52。C52PUB在接收到对CMD52的响应完成后自动清零。此外，如果在传输最后一个块时将C52PUB设置为1，则不会发出CMD52。

在这种情况下，访问结束标志设置为1后，C52PUB自动清零。

当CMD53（多块）读序列中C52PUB和RWREQ置1时，块传输进入块间读等待状态，自动发出CMD52。C52PUB在接收到对CMD52的响应完成后自动清零。此外，如果在传输最后一个块时将C52PUB设置为1，则不会发出CMD52。在这种情况下，访问结束标志设置为1后，C52PUB自动清零。

如果在CMD53（多块）读取序列中将C52PUB设置为1，则除了C52PUB之外，还必须将RWREQ设置为1。

在将C52PUB设置为1之前设置SD_ARG。

在响应结束标志设置后将C52PUB设置为1。

43.2.21 SDIO中断标志 寄存器(SDIO_INFO1)

Address(es): SDHI0.SDIO_INFO1 4006 206Ch, SDHI1.SDIO_INFO1 4006 246Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	EXWT	EXPUB52	—	—	—	—	—	—	—	—	—	—	—	—	—	IOIRQ
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	x	x	0

x: Undefined

Bit	Symbol	位名称	Description	R/W
b0	IOIRQ	SDIO中断状态标志	0：未检测到SDIO中断1：检测到SDIO中断。	R(/W)*1
b2, b1	—	Reserved	读取值未定义。写入值应为1。	R/W
b13 to b3	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b14	EXPUB52	EXPUB52状态标志	指示EXPUB52的状态。	R(/W)*1
b15	EXWT	EXWT状态标志	指示EXWT的状态。	R(/W)*1
b31 to b16	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 只能写入0以清除该位。

SDIO_INFO1寄存器指示SDIO卡访问的状态。将要清除的标志设置为0。设置未清除的标志

being cleared to 1.

IOIRQ flag (SDIO Interrupt Status Flag)

The IOIRQ flag indicates that an SDIO interrupt occurred.

[Setting condition]

- When SDIO interrupt from an SDIO card is received while INTEN in SDIO_MODE is set to 1.

[Clearing condition]

- When 0 is written to IOIRQ.*1

Note 1. Before clearing this bit, access the SDIO card to negate the SDIO interrupt signal from the SDIO card. If the interrupt signal is not negated, this bit can be set again.

EXPUB52 flag (EXPUB52 Status Flag)

The EXPUB52 flag indicates the EXPUB52 status.

[Setting conditions]

- While the last block in the CMD53 (multiple block) sequence is transferred, C52PUB in SDIO_MODE is set to 1.
- While C52PUB is set to 1 in the CMD53 (multiple block) write sequence, the last block is transferred.

[Clearing condition]

- When 0 is written to EXPUB52.

EXWT flag (EXWT Status Flag)

The EXWT flag indicates the EXWT status.

[Setting condition]

- While the last block in the CMD53 (multiple block) read sequence is transferred, RWREQ in SDIO_MODE is set to 1.

[Clearing condition]

- When 0 is written to EXWT.

43.2.22 SDIO INFO1 Interrupt Mask Register (SDIO_INFO1_MASK)

Address(es): SDHI0.SDIO_INFO1_MASK 4006 2070h, SDHI1.SDIO_INFO1_MASK 4006 2470h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	EXWTM	EXPUB52M	—	—	—	—	—	—	—	—	—	—	—	—	—	IOIRQM
Value after reset:	1	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bit	Symbol	Bit name	Description	R/W
b0	IOIRQM	IOIRQ Interrupt Mask Control	0: Do not mask IOIRQ interrupts 1: Mask IOIRQ interrupts.	R/W
b2, b1	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b13 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b14	EXPUB52M	EXPUB52 Interrupt Request Mask Control	0: Do not mask EXPUB52 interrupt requests 1: Mask EXPUB52 interrupt requests.	R/W

被清除为1。

IOIRQ标志（SDIO中断状态标志）

IOIRQ标志表示发生了SDIO中断。

[Setting condition]

- 当SDIO_MODE中的INTEN设置为1时接收到来自SDIO卡的SDIO中断。

[Clearing condition]

- 当0写入IOIRQ时。*1

注1.在清除该位之前，访问SDIO卡以否定来自SDIO卡的SDIO中断信号。如果中断信号没有被否定，这个位可以被重新设置。

EXPUB52标志（EXPUB52状态标志）

EXPUB52标志指示EXPUB52状态。

[Setting conditions]

- 在传输CMD53（多块）序列中的最后一个块时，SDIO_MODE中的C52PUB设置为1。
- 当C52PUB在CMD53（多块）写入序列中设置为1时，传输最后一个块。

[Clearing condition]

- 当0写入EXPUB52时。

EXWT标志（EXWT状态标志）

EXWT标志指示EXWT状态。

[Setting condition]

- 在传输CMD53（多块）读取序列中的最后一个块时，SDIO_MODE中的RWREQ设置为1。

[Clearing condition]

- 当0写入EXWT时。

43.2.22 SDIOINFO1中断屏蔽寄存器(SDIO_INFO1_MASK)

Address(es): SDHI0.SDIO_INFO1_MASK 4006 2070h, SDHI1.SDIO_INFO1_MASK 4006 2470h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	EXWTM	EXPUB52M	—	—	—	—	—	—	—	—	—	—	—	—	—	IOIRQM
重置后的值:	1	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bit	Symbol	位名称	Description	R/W
b0	IOIRQM	IOIRQ中断屏蔽控制	0：不屏蔽IOIRQ中断1：屏蔽IOIRQ中断。	R/W
b2, b1	—	Reserved	这些位被读取为1。写入值应为1。	R/W
b13 to b3	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b14	EXPUB52M	EXPUB52中断请求掩码控制	0：不屏蔽EXPUB52中断请求1：屏蔽EXPUB52中断请求。	R/W

Bit	Symbol	Bit name	Description	R/W
b15	EXWTM	EXWT Interrupt Request Mask Control	0: Do not mask EXWT interrupt requests 1: Mask EXWT interrupt requests.	R/W
b31 to b16	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The SDIO_INFO1_MASK register enables or disables interrupt requests from the status flags in the SDIO_INFO1 register. See Table 43.5, Interrupt sources for details on the relationship between the status flags and the requested interrupt source.

43.2.23 DMA Mode Enable Register (SD_DMAEN)

Address(es): SDHI0.SD_DMAEN 4006 21B0h, SDHI1.SD_DMAEN 4006 25B0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DMAEN	—
Value after reset:	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	—	Reserved	This bit is read as 0.	R
b1	DMAEN	DMA Transfer Enable*1, *2	0: Disable use of DMA transfer to access SD_BUF0 register 1: Enable use of DMA transfer to access SD_BUF0 register.	R/W
b3, b2	—	Reserved	These bits are read as 0.	R
b4	—	Reserved	This bit is read as 1.	R
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b7, b6	—	Reserved	These bits are read as 0.	R
b9, b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b11, b10	—	Reserved	These bits are read as 0.	R
b12	—	Reserved	This bit is read as 1.	R
b31 to b13	—	Reserved	These bits are read as 0.	R

Note 1. Do not rewrite this bit when the SD_INFO2.CBSY bit is 1.
Note 2. When the SD_INFO2_MASK.BWEM bit is 0 or the SD_INFO2_MASK.BREM bit is 0, set the SD_DMAEN.DMAEN bit to 0. When the SD_DMAEN.DMAEN bit is 1, set the SD_INFO2_MASK.BWEM bit to 1 and the SD_INFO2_MASK.BREM bit to 1.

The SD_DMAEN register enables or disables DMA transfers.

DMAEN bit (DMA Transfer Enable)

When using DMA transfer to access the SD buffer, set the DMAEN bit to 1 before setting the SD_CMD register.

Bit	Symbol	位名称	Description	R/W
b15	EXWTM	EXWT中断请求掩码 Control	0：不屏蔽EXWT中断请求1：屏蔽EXWT中断请求。	R/W
b31 to b16	—	Reserved	这些位被读取为0。写入值应为0。	R/W

SDIO_INFO1_MASK寄存器启用或禁用来自SDIO_INFO1寄存器中状态标志的中断请求。有关状态标志和请求的中断源之间关系的详细信息，请参见表43.5，中断源。

43.2.23 DMA模式使能寄存器(SD_DMAEN)

Address(es): SDHI0.SD_DMAEN 4006 21B0h, SDHI1.SD_DMAEN 4006 25B0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DMAEN	—
重置后的值：	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0

Bit	Symbol	位名称		Description	R/W
b0	—	Reserved		该位读为0。	R
b1	DMAEN	DMA传输使能	*1, *2	0：禁止使用DMA传输访问SD_BUF0寄存器1：启用使用DMA传输访问SD_BUF0寄存器。	R/W
b3, b2	—	Reserved		这些位读为0。	R
b4	—	Reserved		该位读为1。	R
b5	—	Reserved		该位读取为0。写入值应为0。	R/W
b7, b6	—	Reserved		这些位读为0。	R
b9, b8	—	Reserved		这些位被读取为0。写入值应为0。	R/W
b11, b10	—	Reserved		这些位读为0。	R
b12	—	Reserved		该位读为1。	R
b31 to b13	—	Reserved		这些位读为0。	R

注1.当SD_INFO2.CBSY位为1时，请勿重写该位。
注2.当SD_INFO2_MASK.BWEM位为0或SD_INFO2_MASK.BREM位为0时，设置SD_DMAEN.DMAEN位为0。当SD_DMAEN.DMAEN位为1时，将SD_INFO2_MASK.BWEM位设置为1，将SD_INFO2_MASK.BREM位设置为1。

SD_DMAEN寄存器启用或禁用DMA传输。

DMAEN位（DMA传输使能）

使用DMA传输访问SD缓冲区时，在设置SD_CMD寄存器之前将DMAEN位设置为1。

43.2.24 Software Reset Register (SOFT_RST)

Address(es): SDHI0.SOFT_RST 4006 21C0h, SDHI1.SOFT_RST 4006 25C0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SDRST
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bit	Symbol	Bit name	Description	R/W
b0	SDRST	Software Reset Control	0: Reset SD/MMC Host Interface software 1: Cancel reset of SD/MMC Host Interface software.	R/W
b2, b1	—	Reserved	These bits are read as 1.	R
b31 to b3	—	Reserved	These bits are read as 0.	R

Table 43.4 lists the bits and flags initialized by SD/MMC Host Interface software reset.

Table 43.4 Bits and flags initialized by SD/MMC Host Interface software reset

Register	Bit/flag
SD_STOP	SEC
SD_INFO1	RSPEND, ACEND
SD_INFO2	CMDE, CRCE, ENDE, DTO, ILW, ILR, RSPTO, SDD0MON, BRE, BWE, SD_CLK_CTRLEN, ILA
SD_CLK_CTRL	CLKEN
SD_OPTION	CTOP[3:0], TOP[3:0], WIDTH Bits b8 and b13 in the SD_OPTION register are also initialized by the SDHI software reset.
SD_ERR_STS1	CMDE0, CMDE1, RSPLENE0, RSPLENE1, RDLENE, CRCLENE, RSPCRCE0, RSPCRCE1, RDCRCE, CRCTKE, CRCTK[2:0]
SD_ERR_STS2	RSPTO0, RSPTO1, BSYTO0, BSYTO1, RDTO, CRCTO, CRCBSYTO
SDIO_INFO1	IOIRQ, EXPUB52, EXWT

43.2.25 SD Interface Mode Setting Register (SDIF_MODE)

Address(es): SDHI0.SDIF_MODE 4006 21CCh, SDHI1.SDIF_MODE 4006 25CCh

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	NOCHKCR	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

43.2.24 软件复位寄存器(SOFT_RST)

Address(es): SDHI0.SOFT_RST 4006 21C0h, SDHI1.SOFT_RST 4006 25C0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SDRST
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

Bit	Symbol	位名称	Description	R/W
b0	SDRST	软件复位控制	0：复位SDMMC主机接口软件1：取消SDMMC主机接口软件的复位。	R/W
b2, b1	—	Reserved	这些位读为1。	R
b31 to b3	—	Reserved	这些位读为0。	R

表43.4列出了SDMMC主机接口软件复位初始化的位和标志。

Table 43.4 由SDMMC主机接口软件复位初始化的位和标志

Register	Bit/flag
SD_STOP	SEC
SD_INFO1	RSPEND, ACEND
SD_INFO2	CMDE、CRCE、ENDE、DTO、ILW、ILR、RSPTO、SDD0MON、BRE、BWE、SD_CLK_CTRLEN、ILA
SD_CLK_CTRL	CLKEN
SD_OPTION	CTOP[3:0], TOP[3:0], WIDTH SD_OPTION寄存器中的位b8和b13也由SDHI软件复位初始化。
SD_ERR_STS1	CMDE0, CMDE1, RSPLENE0, RSPLENE1, RDLENE, CRCLENE, RSPCRCE0, RSPCRCE1, RDCRCE, CRCTKE, CRCTK[2:0]
SD_ERR_STS2	RSPTO0, RSPTO1, BSYTO0, BSYTO1, RDTO, CRCTO, CRCBSYTO
SDIO_INFO1	IOIRQ, EXPUB52, EXWT

43.2.25 SD接口模式设置寄存器(SDIF_MODE)

Address(es): SDHI0.SDIF_MODE 4006 21CCh, SDHI1.SDIF_MODE 4006 25CCh

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	NOCHKCR	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b7 to b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Bit	Symbol	Bit name	Description	R/W
b8	NOCHKCR	CRC Check Mask	CRC check mask bit for MMC test commands. Set when CRC16 or CRC status value check is not executed. 0: Enable CRC check 1: Disable CRC Check (ignore CRC16 valued when reading and ignore CRC status value when writing).	R/W
b31 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

NOCHKCR bit (CRC Check Mask)

The NOCHKCR bit is used for MMC test commands. This bit is set when CRC16 or CRC status value check is not executed.

43.2.26 Swap Control Register (EXT_SWAP)

Address(es): SDHI0.EXT_SWAP 4006 21E0h, SDHI1.EXT_SWAP 4006 25E0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	BRSWP	BWSWP	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	—	Reserved	This bit is read as 0 and cannot be modified.	R
b1	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b2	—	Reserved	This bit is read as 0 and cannot be modified.	R
b4, b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b5	—	Reserved	This bit is read as 0 and cannot be modified.	R
b6	BWSWP	SD_BUF0 Swap Write*1	0: Normal write operation 1: Swap the byte endian order before writing to SD_BUF0 register.	R/W
b7	BRSWP	SD_BUF0 Swap Read*1	0: Normal read operation 1: Swap the byte endian order before reading SD_BUF0 register.	R/W
b10 to b8	—	Reserved	These bits are read as 0. Writing to these bits has no effect.	R
b12, b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b14, b13	—	Reserved	These bits are read as 0. Writing to these bits has no effect.	R
b15	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b31 to b16	—	Reserved	These bits are read as 0. Writing to these bits has no effect.	R

Note 1. Do not rewrite this bit when the SD_INFO2.CBSY flag is 1.

The EXT_SWAP register selects whether or not the byte endian order is swapped when accessing the SD_BUF0 register. See section 43.3.1 for details on the differences in accessing the SD_BUF0 register based on the EXT_SWAP register value.

43.3 Operation

43.3.1 SD/MMC Interface

When data is read from the SD card/MMC, the process is as follows:

1. The SD/MMC Host Interface receives data from the SD card/MMC through the SDnDAT signal (see Figure 43.2 and Figure 43.3).

Bit	Symbol	位名称	Description	R/W
b8	NOCHKCR	CRC校验掩码	MMC测试命令的CRC校验掩码位。不执行CRC16或CRC状态值检查时置位。0：启用CRC校验1：禁用CRC校验（读取时忽略CRC16值，写入时忽略CRC状态值）。	R/W
b31 to b9	—	Reserved	这些位被读取为0。写入值应为0。	R/W

NOCHKCR位（CRC校验掩码）

NOCHKCR位用于MMC测试命令。当不执行CRC16或CRC状态值检查时，该位置位。

43.2.26 交换控制寄存器(EXT_SWAP)

Address(es): SDHI0.EXT_SWAP 4006 21E0h, SDHI1.EXT_SWAP 4006 25E0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	BRSWP	BWSWP	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	—	Reserved	该位读为0，不能修改。	R
b1	—	Reserved	该位读取为0。写入值应为0。	R/W
b2	—	Reserved	该位读为0，不能修改。	R
b4, b3	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b5	—	Reserved	该位读为0，不能修改。	R
b6	BWSWP	SD_BUF0 Swap Write*1	0：正常写操作1：在写入SD_BUF0寄存器之前交换字节顺序。	R/W
b7	BRSWP	SD_BUF0 Swap Read*1	0：正常读取操作1：在读取SD_BUF0寄存器之前交换字节顺序。	R/W
b10 to b8	—	Reserved	这些位被读取为0。写入这些位无效。	R
b12, b11	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b14, b13	—	Reserved	这些位被读取为0。写入这些位无效。	R
b15	—	Reserved	该位读取为0。写入值应为0。	R/W
b31 to b16	—	Reserved	这些位被读取为0。写入这些位无效。	R

Note 1. 当SD_INFO2.CBSY标志为1时，不要重写该位。

EXT_SWAP寄存器选择在访问SD_BUF0寄存器时是否交换字节顺序。
有关根据EXT_SWAP寄存器值访问SD_BUF0寄存器的差异的详细信息，请参见第43.3.1节。

43.3 Operation

43.3.1 SD/MMC Interface

从SD卡MMC读取数据时，流程如下：

1. SDMMC主机接口通过SDnDAT信号从SD卡MMC接收数据（参见图43.2和图43.3）。

2. The received data is stored in SD_BUF of the MMC Host Interface (see Figure 43.4).
3. The data stored in SD_BUF is read from SD_BUF0 (see Figure 43.5).

When data is written to the SD card/MMC, the specified procedure is reversed.

When accessing SD_BUF0, pay attention to the transfer order in SDnDAT and the store order in SD_BUF. If required, you can change the byte endian of the data read from or written to SD_BUF0 using the SDSWAP register. See Figure 43.6.

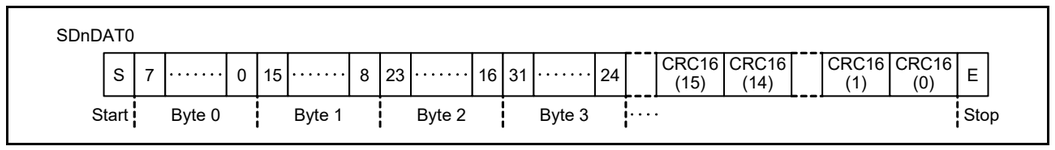


Figure 43.2 SDnDAT in 1-bit width mode

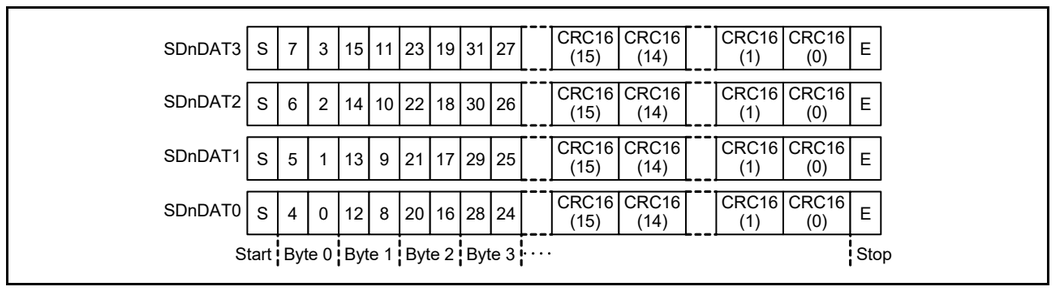


Figure 43.3 SDnDAT in 4-bit width mode

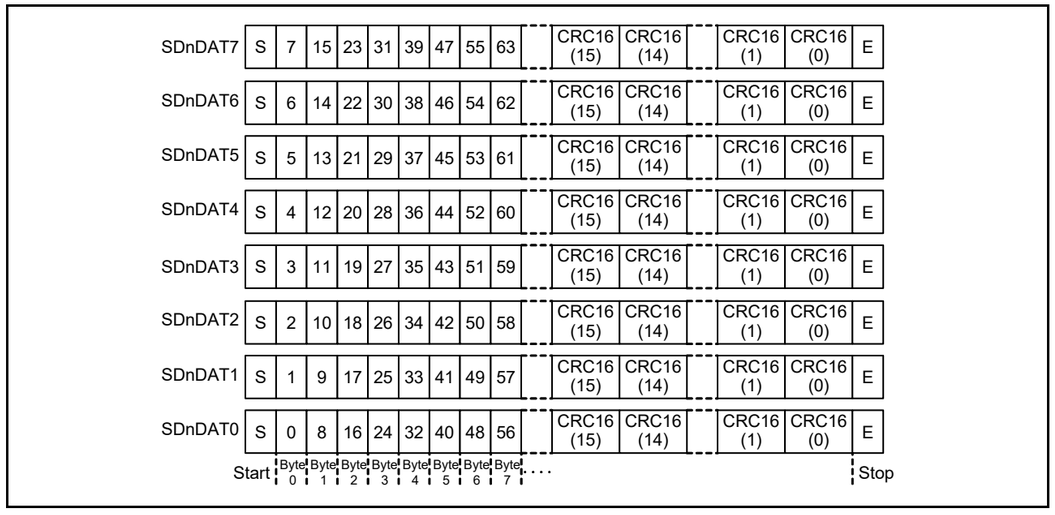


Figure 43.4 SDnDAT in 8-bit width mode

2. 接收到的数据存储在MMC主机接口的SD_BUF中（见图43.4）。
3. SD_BUF中存储的数据从SD_BUF0中读取（参见图43.5）。

当数据写入SD卡MMC时，指定的过程相反。

访问SD_BUF0时，注意SDnDAT中的传输顺序和SD_BUF中的存储顺序。如果需要，您可以使用SDSWAP寄存器更改从SD_BUF0读取或写入数据的字节字节序。请参见图43.6。

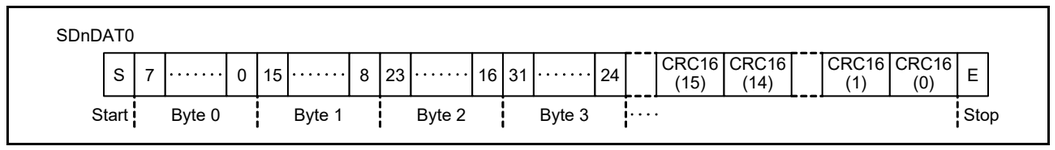


Figure 43.2 SDnDAT在1位宽模式下

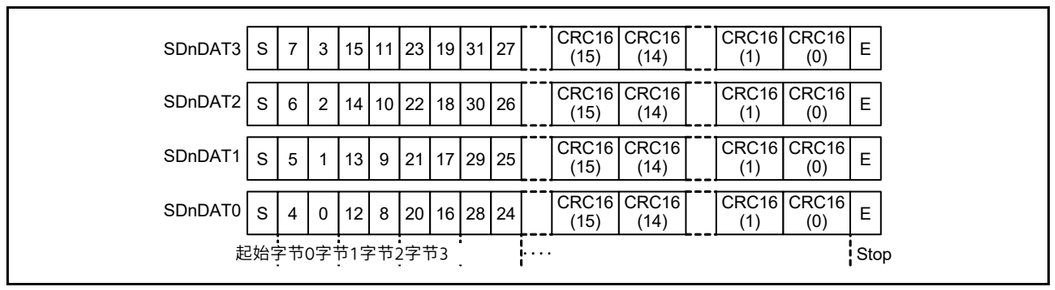


Figure 43.3 SDnDAT在4位宽模式下

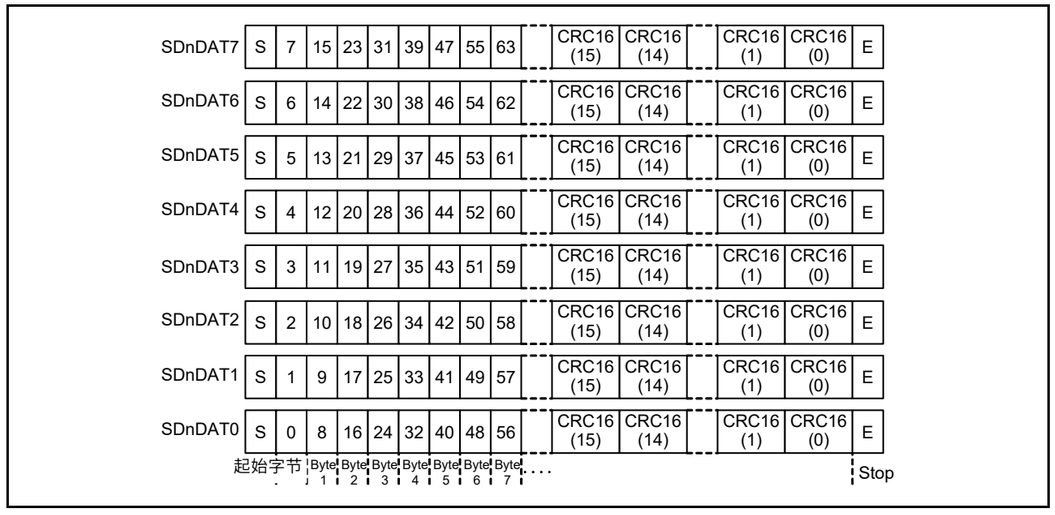


Figure 43.4 SDnDAT在8位宽度模式下

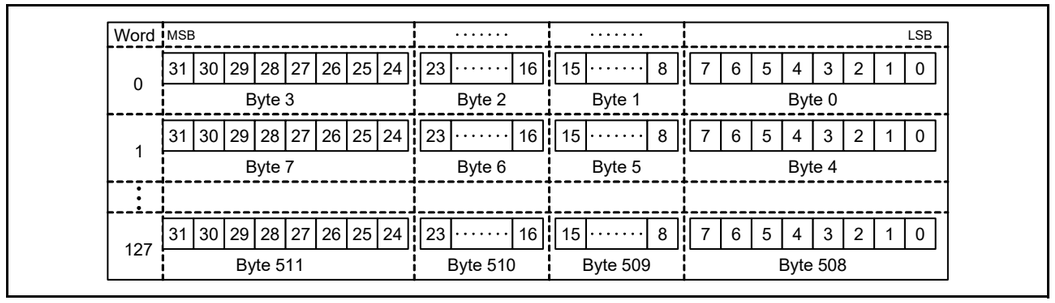


Figure 43.5 SD_BUF store data

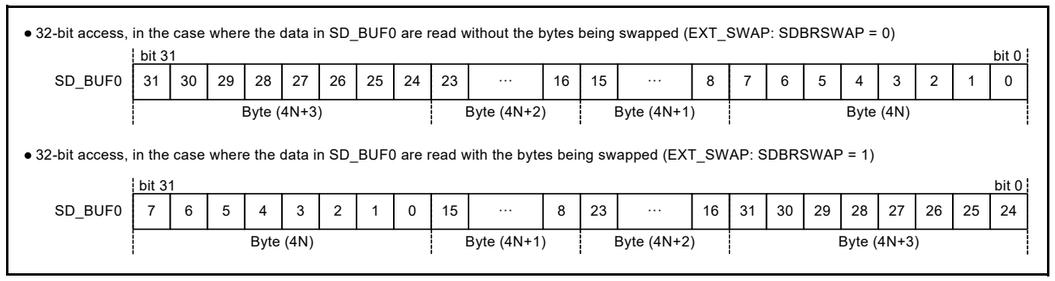


Figure 43.6 Read from SD_BUF0

43.3.2 Card Detect/Write Protect

43.3.2.1 Card detect

The SD/MMC Host Interface has two types of card detect functions.

(1) Card detect with SDnCD (n = 0, 1)

Figure 43.7 shows the timing for card detect using SDnCD. SDnCD is connected to the card socket and pulled up on the host device. The resistance of the pull-up resistor is determined by the specification of the SD/MMC host device.

(2) Card insertion

SDnCD is pulled down when a card is inserted. At this point, if SDnCD is pulled down for the Mcycle period (set in SD_OPTION), SDCDIN in SD_INFO1 is set to 1. It is cleared by writing 0.

(3) Card removal

SDnCD is pulled up when a card is removed. At this point, if SDnCD is pulled up for the Mcycle period (set in SD_OPTION), SDCDRM in SD_INFO1 is set to 1. It is cleared by writing 0.

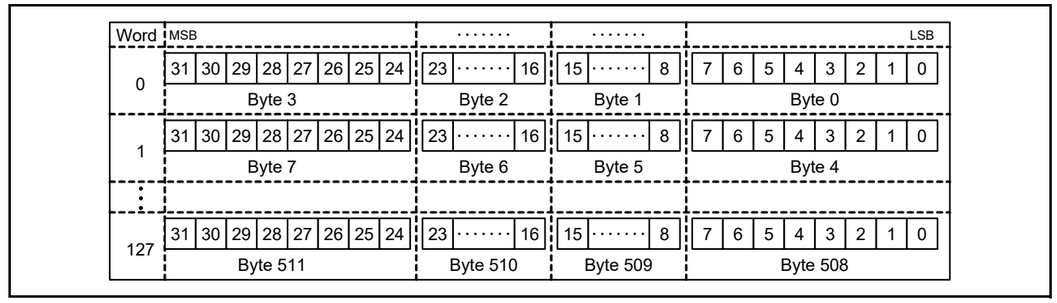


Figure 43.5 SD_BUF存储数据

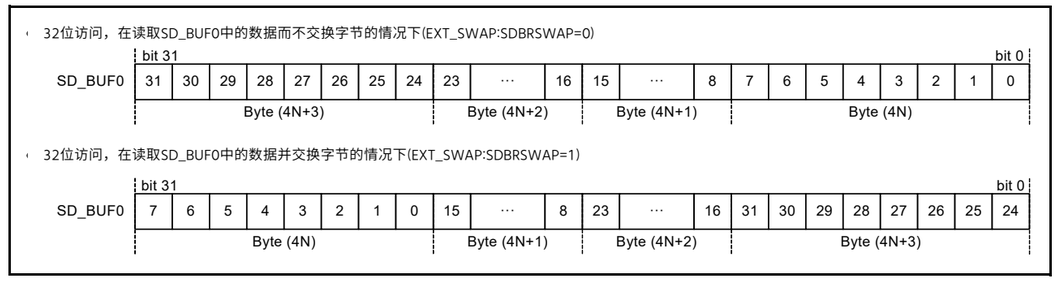


Figure 43.6 从SD_BUF0读取

43.3.2 卡检测写保护

43.3.2.1 卡检测

SDMMC主机接口有两种类型的卡检测功能。

(1) SDnCD卡检测(n=0 1)

图43.7显示了使用SDnCD进行卡检测的时序。SDnCD连接到卡插槽并在主机设备上拉高。上拉电阻的阻值由SD MMC主机设备的规格决定。

(2) 插卡

SDnCD在插入卡时被拉下。此时，如果SDnCD被下拉Mcycle周期（设置在SD_OPTION)，SD_INFO1中的SDCDIN设置为1。写入0清除。

(3) 取卡

取出卡时，SDnCD被拉起。此时，如果SDnCD被拉高了Mcycle周期（设置在SD_OPTION)，SD_INFO1中的SDCDRM设置为1，写入0清零。

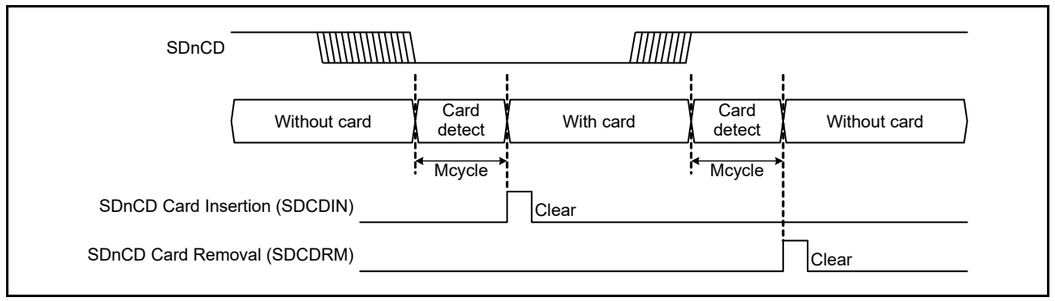


Figure 43.7 Example of card detect with SDnCD

(4) SD card detect with SDnDAT3 (n = 0, 1)

Figure 43.8 shows the timing when the SD card is detected with SDnDAT3. In addition, SDnDAT3 is pulled down by the host device, and the resistance value for pulling down is determined by the specification of the SD host device.

(5) Card insertion

When an SD card is inserted, SDnDAT3 is pulled up and SDD3IN in SD_INFO1 is set to 1. It is cleared by writing 0.

(6) Card removal

When an SD card is removed, SDnDAT3 is pulled down and SDD3RM in SD_INFO1 is set to 1. It is cleared by writing 0.

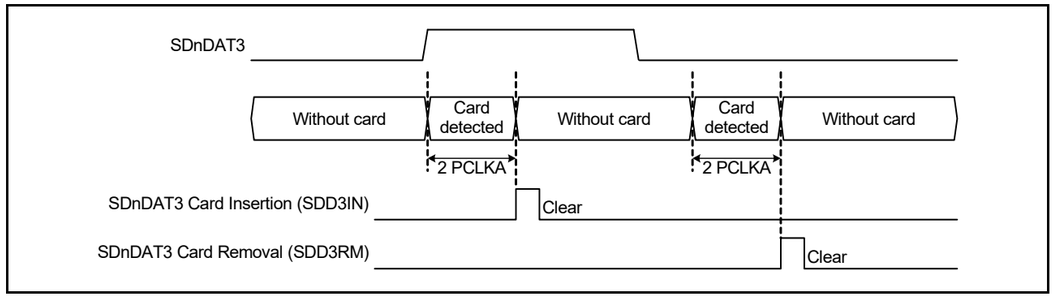


Figure 43.8 SD card detect with SDnDAT3

43.3.2.2 Write protect

The SD/MMC Host Interface has two types of write protect functions.

(1) Write protect with SDnWP (n = 0, 1)

SDnWP is connected to the card socket and pulled up or pulled down by the card insertion. The selection of pulling up or pulling down and the resistance value is determined by the specification of the SD host device. When the SDnWP state is reflected to SDWPMON in SD_INFO1, the write protect state is set after the SD card is inserted.

(2) Write protect with command

The internal write protection of the card and the lock/unlock operation of the card are realized by the command.

43.3.3 Interrupt Request and DMA Transfer Request

43.3.3.1 Interrupts

Table 43.5 lists the SDHI interrupt sources. The SDHI requests an interrupt when:

- The status flags in registers SD_INFO1, SD_INFO2, and SDIO_INFO1 set to 1

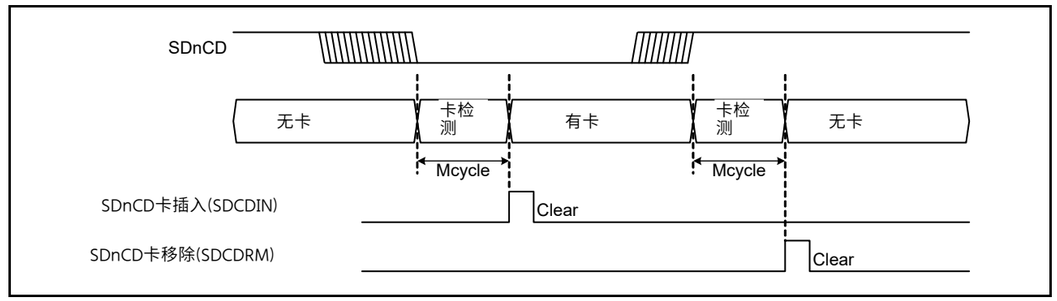


Figure 43.7 SDnCD卡检测示例

(4) 使用SDnDAT3检测SD卡(n=0 1)

图43.8显示了使用SDnDAT3检测到SD卡的时序。此外，SDnDAT3由主机设备下拉，下拉电阻值由SD主机设备的规格决定。

(5) 插卡

插入SD卡时，SDnDAT3上拉，SD_INFO1中的SDD3IN置1，写0清零。

(6) 取卡

拔出SD卡时，SDnDAT3被拉低，SD_INFO1中的SDD3RM置1，写入0清零。

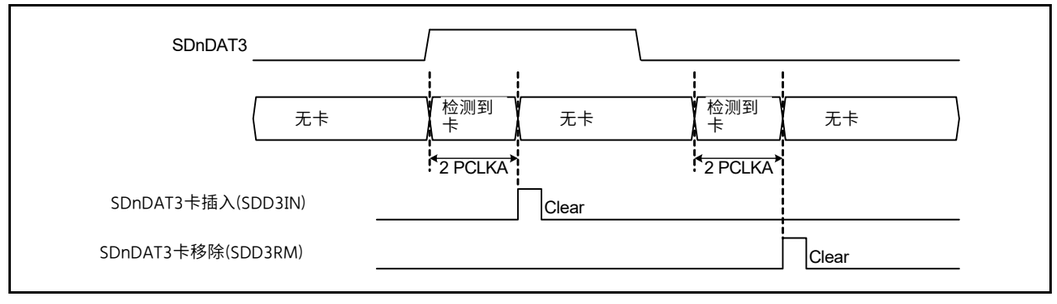


Figure 43.8 使用SDnDAT3检测SD卡

43.3.2.2 写保护

SDMMC主机接口有两种类型的写保护功能。

(1) 使用SDnWP进行写保护(n=0 1)

SDnWP与卡座相连，通过插卡进行上拉或下拉。上拉或下拉的选择和阻值由SD主机设备的规格决定。当SDnWP状态反映到SD_INFO1中的SDWPMON时，插入SD卡后设置写保护状态。

(2) 用命令写保护

卡的内部写保护和卡的开锁操作都是通过命令实现的。

43.3.3 中断请求和DMA传输请求

43.3.3.1 Interrupts

表43.5列出了SDHI中断源。SDHI在以下情况下请求中断：

- 寄存器SD_INFO1、SD_INFO2和SDIO_INFO1中的状态标志设置为1

- The associated bits in the SD_INFO1_MASK, SD_INFO2_MASK, and SDIO_INFO1_MASK registers are 0.

When clearing the status flags in registers SD_INFO1, SD_INFO2, and SDIO_INFO1, write 0 to the status flags to be cleared and write 1 to the status flags that are not being cleared.

Table 43.5 Interrupt sources

Interrupt sources	Status flag register		Interrupt mask register		Interrupt name	
	Register symbol	Bit symbol	Register symbol	Bit symbol	Ch 0	Ch 1
Card Access Interrupt (CACI)	SD_INFO1	ACEND	SD_INFO1_MASK	ACENDM	SDHI_MMC0_ACCS	SDHI_MMC1_ACCS
		RSPEND		RSPENDM		
	SD_INFO2	ILA	SD_INFO2_MASK	ILAM		
		BWE		BWEM		
		BRE		BREM		
		RSPTO		RSPTOM		
		ILR		ILRM		
		ILW		ILWM		
		DTO		DTOM		
		ENDE		ENDEM		
		CRCE		CRCEM		
		CMDE		CMDEM		
SDIO Access Interrupt (SDACI)	SDIO_INFO1	EXWT	SDIO_INFO1_MASK	EXWTM	SDHI_MMC0_SDIO	SDHI_MMC1_SDIO
		EXPUB52		EXPUB52M		
		IOIRQ		IOIRQM		
Card Detect Interrupt (CDETI)	SD_INFO1	SDD3IN	SD_INFO1_MASK	SDD3INM	SDHI_MMC0_CARD	SDHI_MMC1_CARD
		SDD3RM		SDD3RMM		
		SDCDIN		SDCDINM		
		SDCDRM		SDCDRMM		

43.3.3.2 DMA transfer requests (SDHI_MMCn_ODMSDBREQ, n = 0 to 1)

The SD/MMC Host Interface has two types of DMA transfer requests.

(1) SD_BUF write DMA transfer request

- When the BWE bit in SD_INFO2 is set to 1 while the DMAEN bit in SD_DMAEN is set to 1, the SD_BUF write DMA transfer request is asserted.
- The SD_BUF write DMA transfer request is negated when the last data in one block (based on the transfer data size set in SD_SIZE) is transferred. The SD_BUF write DMA transfer request is also negated by clearing the SDRST bit in SOFT_RST to 0 or setting the STP bit in SD_STOP to 1. However, if a communications error or timeout occurs at the DMA transfer, the SD_BUF write DMA transfer request is not negated.
- The BWE bit in SD_INFO2 is cleared after transfer of the last data in one block following a request for writing to SD_BUF by DMA transfer.
- The number of DMA transfers must be n x one block. (n = integer, one block = the transfer data size set in SD_SIZE)
- When the IOABT bit in SDIO_MODE is set to 1, the SD_BUF write DMA transfer request is negated.
- The DMA transfer request is also negated by clearing the DMAEN bit to 0. However, the DMA transfer request is asserted again when the DMAEN bit is set to 1 before writing to SD_CMD.
- Because the BWE bit in SD_INFO2 is not cleared in response to setting the STP/IOABT bit, or to a communications error or timeout, clear the bit to 0 before issuing the next command. The next request to write to SD_BUF by DMA transfer is not issued while the BWE bit is set.

- SD_INFO1_MASK、SD_INFO2_MASK和SDIO_INFO1_MASK寄存器中的相关位为0。

清除寄存器SD_INFO1、SD_INFO2和SDIO_INFO1中的状态标志时，将要清除的状态标志写入0，将未清除的状态标志写入1。

Table 43.5 中断源

中断源	状态标志寄存器		中断屏蔽寄存器		中断名称	
	注册符号	位符号	注册符号	位符号	Ch 0	Ch 1
卡访问中断(CACI)	SD_INFO1	ACEND	SD_INFO1_MASK	ACENDM	SDHI_MMC0_ACCS	SDHI_MMC1_ACCS
		RSPEND		RSPENDM		
	SD_INFO2	ILA	SD_INFO2_MASK	ILAM		
		BWE		BWEM		
		BRE		BREM		
		RSPTO		RSPTOM		
		ILR		ILRM		
		ILW		ILWM		
		DTO		DTOM		
		ENDE		ENDEM		
		CRCE		CRCEM		
		CMDE		CMDEM		
SDIO Access Interrupt (SDACI)	SDIO_INFO1	EXWT	SDIO_INFO1_MASK	EXWTM	SDHI_MMC0_SDIO	SDHI_MMC1_SDIO
		EXPUB52		EXPUB52M		
		IOIRQ		IOIRQM		
卡检测中断(CDETI)	SD_INFO1	SDD3IN	SD_INFO1_MASK	SDD3INM	SDHI_MMC0_CARD	SDHI_MMC1_CARD
		SDD3RM		SDD3RMM		
		SDCDIN		SDCDINM		
		SDCDRM		SDCDRMM		

43.3.3.2 DMA传输请求（SDHI_MMCn_ODMSDBREQ，n=0到1）

SDMMC主机接口有两种类型的DMA传输请求。

(1) SD_BUF写DMA传输请求

- 当SD_INFO2中的BWE位设置为1而SD_DMAEN中的DMAEN位设置为1时，SD_BUF写DMA传输请求被断言。
- 当一个块中的最后一个数据（基于SD_SIZE中设置的传输数据大小）被传输时，SD_BUF写DMA传输请求被否定。SD_BUF写DMA传输请求也可以通过将SOFT_RST中的SDRST位清0或将SD_STOP中的STP位设置为1来取消。但是，如果DMA传输发生通信错误或超时，则SD_BUF写DMA传输请求不会被取消。否定。
- SD_INFO2中的BWE位在通过DMA传输请求写入SD_BUF后传输一个块中的最后一个数据后被清除。
- DMA传输的数量必须是nx一个块。（n=整数，1块=中设置的传输数据大小SD_SIZE)
- 当SDIO_MODE中的IOABT位设置为1时，SD_BUF写DMA传输请求被否定。
- DMA传输请求也可以通过将DMAEN位清除为0来取消。但是，当DMAEN位在写入SD_CMD之前设置为1时，DMA传输请求会再次有效。
- 因为SD_INFO2中的BWE位不会在设置STPIOABT位或通信错误或超时时被清除，所以在发出下一个命令之前将该位清除为0。当BWE位置位时，不会发出通过DMA传输写入SD_BUF的下一个请求。

(2) SD_BUF read DMA transfer request

- When the BRE bit in SD_INFO2 is set to 1 while the DMAEN bit in the SD_DMAEN register is set to 1, the SD_BUF read DMA transfer request is asserted.
- The SD_BUF read DMA transfer request is negated when the last data in one block (based on the transfer data size set in SD_SIZE) is transferred. The SD_BUF read DMA transfer request is also negated by clearing the SDRST bit in SOFT_RST to 0 or setting the STP bit in SD_STOP to 1. However, if a communications error or timeout occurs at the DMA transfer, the SD_BUF read DMA transfer request is not negated.
- The BRE bit in SD_INFO2 is cleared after transfer of the last data in one block following a request to write to SD_BUF by DMA transfer.
- The number of DMA transfers must be n x one block. (n = integer, one block = the transfer data size set in SD_SIZE)
- When the IOABT bit in SDIO_MODE is set to 1, the SD_BUF read DMA transfer request is negated.
- The DMA transfer request is also negated by clearing the DMAEN bit to 0. However, the DMA transfer request is asserted again when the DMAEN bit is set to 1 before writing to SD_CMD.
- Because the BRE bit in SD_INFO2 is not cleared in response to setting the STP/IOABT bit or in response to a communications error or timeout, clear the bit to 0 before issuing the next command. The next request to write to SD_BUF by DMA transfer is not issued while the BRE bit is set.

43.3.4 Communication Errors and Timeouts

When a communication error or timeout error occurs, depending on the type of error, the associated status flag in the SD_INFO2 register sets to 1. Also, depending on the source of the error, the associated flag in the SD_ERR_STS1 or SD_ERR_STS2 register sets to 1.

The status flags in registers SD_ERR_STS1 and SD_ERR_STS2 clear to 0 by writing to the SD_CMD register, or by setting the SOFT_RST.SDRST bit to 0.

Table 43.6 Communication errors

Communication error	Interrupt flag register: Register symbol	Interrupt flag register: Bit symbol	Error status register: Register symbol	Error status register: Bit symbol	This occurs when...
End bit error	SD_INFO2	ENDE	SD_ERR_STS1	CRCLENE	The CRC status token length is in error
				RDLENE	The read data length is in error
				RSPLENE1	The response length is in error*1
				RSPLENE0	The response length is in error*2
CRC error		CRCE		CRCTKE	The CRC status token is in error
				RDCRCE	There is a CRC error in the read data
				RSPCRCE1	There is a CRC error in the response*1
				RSPCRCE0	There is a CRC error in the response*2
Command error		CMDE		CMDE1	The command index field value for the transmitted command and received response do not match*1
				CMDE0	The command index field value for the transmitted command and received response do not match*2

Note 1. CMD12 when automatic issuing is enabled for multiple block transfer by the setting in SD_CMD, CMD12 when the STP bit in SD_STOP is set to 1, or CMD52 when the C52PUB or IOABT bit in SDIO_MODE is set to 1.
Note 2. CMD other than CMD12 when automatic issuing is enabled for multiple block transfer by the setting in SD_CMD, CMD12 when the STP bit in SD_STOP is set to 1, or CMD52 when the C52PUB or IOABT bit in SDIO_MODE is set to 1.

(2) SD_BUF读取DMA传输请求

- 当SD_INFO2中的BRE位设置为1而SD_DMAEN寄存器中的DMAEN位设置为1时，SD_BUF读取DMA传输请求被断言。
- 当传输一个块中的最后一个数据（基于SD_SIZE中设置的传输数据大小）时，会取消SD_BUF读取DMA传输请求。SD_BUF读DMA传输请求也可以通过将SOFT_RST中的SDRST位清0或将SD_STOP中的STP位设置为1来否定。但是，如果DMA传输发生通信错误或超时，则SD_BUF读DMA传输请求不会否定。
- SD_INFO2中的BRE位在一个块中的最后一个数据传输后被清除SD_BUF通过DMA传输。
- DMA传输的数量必须是nx一个块。（n=整数，1块=中设置的传输数据大小SD_SIZE)
- 当SDIO_MODE中的IOABT位设置为1时，SD_BUF读取DMA传输请求被否定。
- DMA传输请求也可以通过将DMAEN位清除为0来取消。但是，当DMAEN位在写入SD_CMD之前设置为1时，DMA传输请求会再次有效。
- 因为SD_INFO2中的BRE位不会在设置STPIOABT位或响应通信错误或超时时被清除，所以在发出下一个命令之前将该位清除为0。当BRE位置位时，不会发出下一个通过DMA传输写入SD_BUF的请求。

43.3.4 通信错误和超时

当发生通信错误或超时错误时，根据错误类型，SD_INFO2寄存器中的相关状态标志设置为1。此外，根据错误源，SD_ERR_STS1中的相关标志或SD_ERR_STS2寄存器设置为1。

通过写入SD_CMD寄存器或将SOFT_RST.SDRST位设置为0，寄存器SD_ERR_STS1和SD_ERR_STS2中的状态标志清零。

Table 43.6 通讯错误

通信故障	中断标志寄存器: 注册符号	中断标志寄存器: 位符号	错误状态寄存器: 注册符号	错误状态寄存器: 位符号	这发生在...
结束位错误	SD_INFO2	ENDE	SD_ERR_STS1	CRCLENE	CRC状态令牌长度错误
				RDLENE	读取数据长度错误
				RSPLENE1	响应长度错误*1
				RSPLENE0	响应长度错误*2
CRC error		CRCE		CRCTKE	CRC状态令牌错误
				RDCRCE	读取数据有CRC错误
				RSPCRCE1	响应中有CRC错误*1
				RSPCRCE0	响应中有CRC错误*2
命令错误		CMDE		CMDE1	发送命令和接收响应的命令索引字段值不匹配*1
				CMDE0	发送命令和接收响应的命令索引字段值不匹配*2

Note 1. 通过SD_CMD中的设置为多块传输启用自动发布时的CMD12，当STP位中的CMD12 SD_STOP设置为1，或当SDIO_MODE中的C52PUB或IOABT位设置为1时为CMD52。
Note 2. 通过SD_CMD中的设置为多块传输启用自动发布时的CMD12以外的CMD，当SD_STOP中的STP位设置为1时为CMD12，或者当SDIO_MODE中的C52PUB或IOABT位设置为1时为CMD52。

Table 43.7 Timeouts

Timeout	Interrupt flag register		Error status register		This occurs when...
	Register symbol	Bit symbol	Register symbol	Bit symbol	
Response timeout	SD_INFO2	RSPTO	SD_ERR_STS2	RSPTO1	A response is not received even after a minimum of 640 SDHI clock cycles elapse*1
				RSPTO0	A response is not received even after a minimum of 640 SDHI clock cycles elapse*2
Data timeout (excluding response timeout)		DTO		CRCBSYTO	After the CRC status token is received, the SDHI is busy for at least the period set*3
				CRCTO	After the write data is transmitted, the CRC status token is not received even after at least the period set*3 elapses
				RDTO	After the read command is issued, the read data is not received even after at least the period set*3 elapses
					After the read data is received, the next block read data is not received even after at least the period set*3 elapses
					After the SDHI exits the read wait state, the next block read data is not received even after at least the period set*3 elapses
				BSYTO1	After CMD12 is issued during the command sequence, the SDHI is busy for at least the period set*3
				BSYTO0	After the R1b response is received, the SDHI is busy for at least the period set*3 (a command other than CMD12 is issued during the command sequence)

Note 1. CMD12 when automatic issuing is enabled for multiple block transfer by the setting in SD_CMD, CMD12 when the STP bit in SD_STOP is set to 1, or CMD52 when the C52PUB or IOABT bit in SDIO_MODE is set to 1.
Note 2. CMD other than CMD12 when automatic issuing is enabled for multiple block transfer by the setting in SD_CMD, CMD12 when the STP bit in SD_STOP bit is set to 1, or CMD52 when the C52PUB or IOABT bit in SDIO_MODE is set to 1.
Note 3. The period is set in the SD_OPTION.TOP[3:0] bits.

43.3.5 Command without Data Transfer (SD/MMC)

Figure 43.9 and Figure 43.10 show example flows.

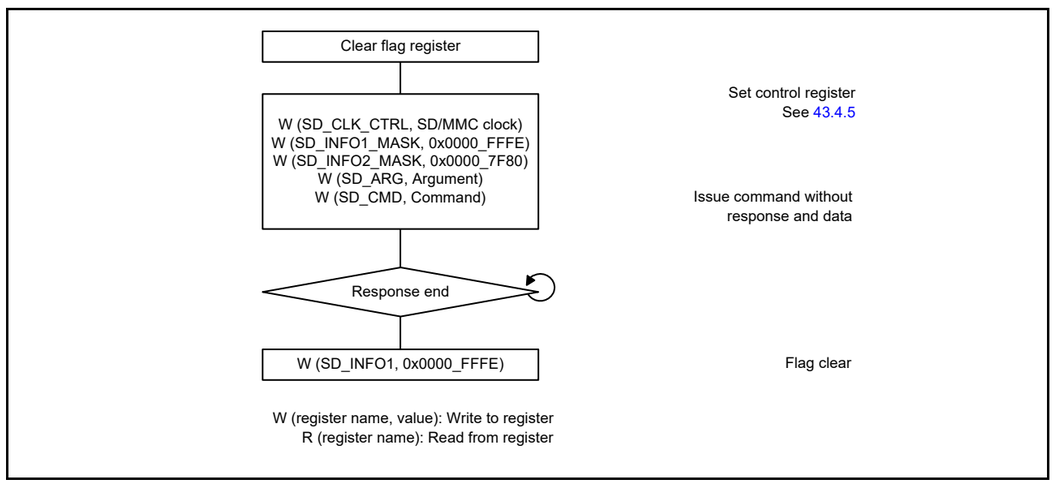


Figure 43.9 Example flow of command without response and data

Table 43.7 Timeouts

Timeout	中断标志寄存器		错误状态寄存器		这发生在...
	注册符号	位符号	注册符号	位符号	
响应超时	SD_INFO2	RSPTO	SD_ERR_STS2	RSPTO1	即使经过至少640个SDHI时钟周期，也没有收到响应*1
				RSPTO0	即使经过至少640个SDHI时钟周期，也没有收到响应*2
数据超时（不包括响应超时）		DTO		CRCBSYTO	收到CRC状态令牌后，SDHI至少在设置的时间段内处于忙碌状态*3
				CRCTO	写入数据发送后，即使经过至少设置的周期*3后也未收到CRC状态令牌
				RDTO	发出读取命令后，即使经过至少设置的时间段*3也未接收到读取数据
					接收到读取数据后，即使经过至少设置的时间段*3也不会接收到下一个块读取数据
					SDHI退出读取等待状态后，即使经过至少设置的时间段*3也不会接收到下一个块读取数据
				BSYTO1	在命令序列期间发出CMD12后，SDHI至少在设置的时间段内处于忙碌状态*3
				BSYTO0	收到R1b响应后，SDHI至少忙了一段时间set*3（在命令序列期间发出CMD12以外的命令）

Note 1. 通过SD_CMD中的设置为多块传输启用自动发布时的CMD12，当STP位中的CMD12 SD_STOP设置为1，或当SDIO_MODE中的C52PUB或IOABT位设置为1时为CMD52。
Note 2. 通过SD_CMD中的设置为多块传输启用自动发布时的CMD12以外的CMD、SD_STOP位中的STP位设置为1时的CMD12或SDIO_MODE中的C52PUB或IOABT位设置为1时的CMD52。
Note 3. 周期在SD_OPTION.TOP[3:0]位中设置。

43.3.5 无数据传输的命令(SDMMC)

图43.9和图43.10显示了示例流程。

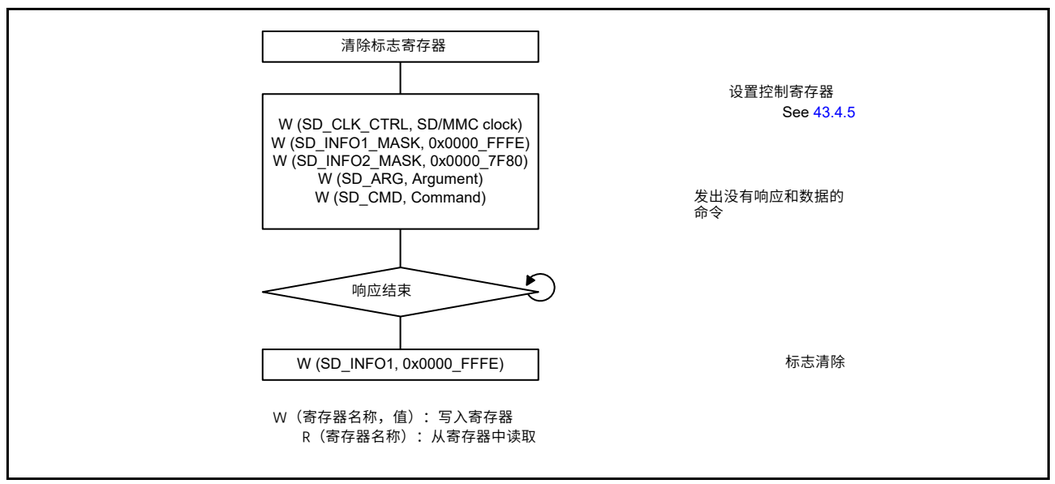


Figure 43.9 没有响应和数据的命令流示例

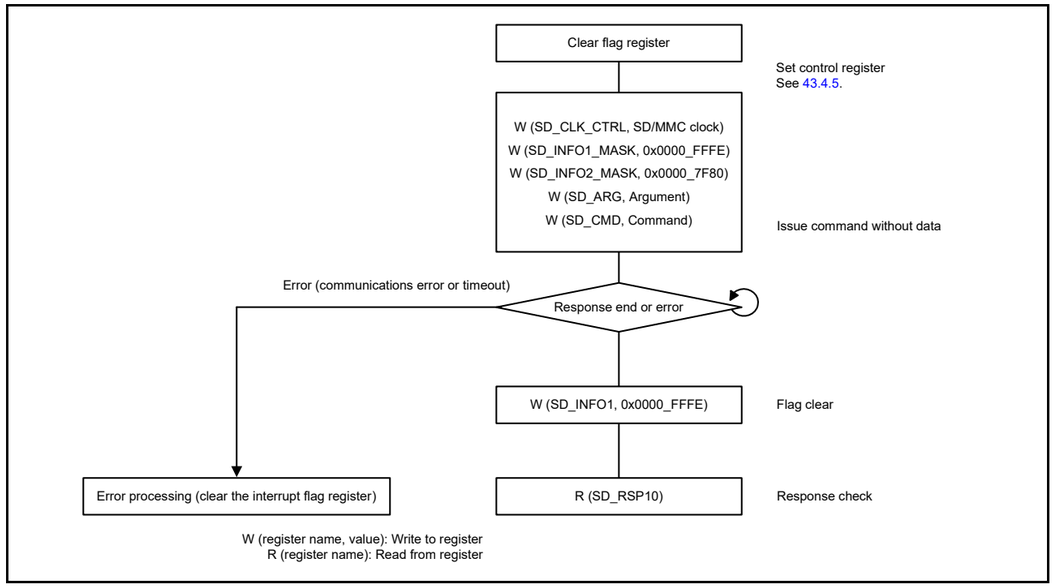


Figure 43.10 Example flow of command without data

43.3.5.1 Operation for command without data transfer

The following legend is used for description of register read/write.

W (register name, value): Write to register

R (register name): Read from register

The operation is described in the following section.

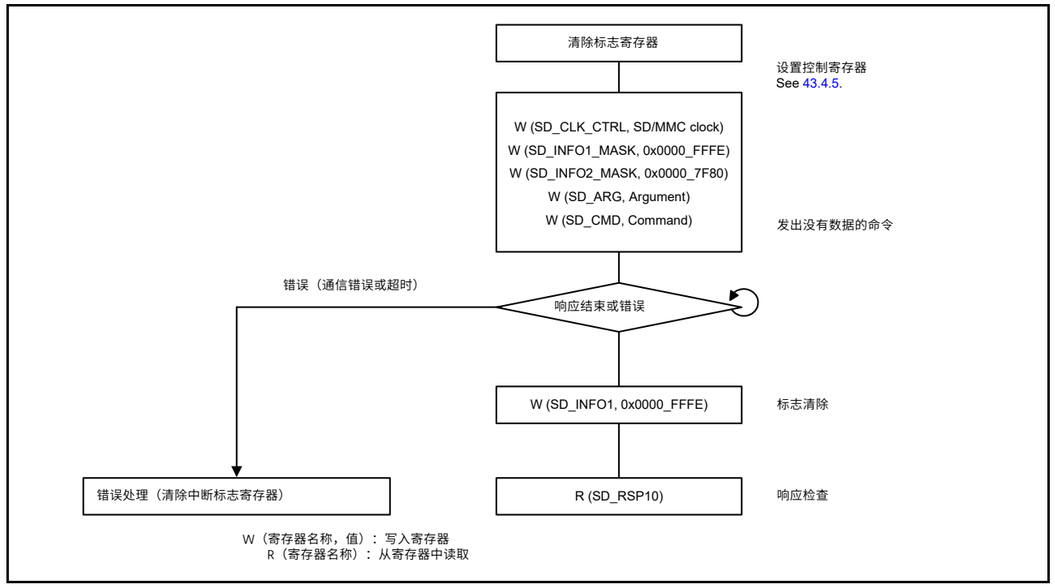


Figure 43.10 没有数据的命令流示例

43.3.5.1 无数据传输的命令操作

以下图例用于描述寄存器读写。

W（寄存器名称，值）：写入寄存器

R（寄存器名称）：从寄存器中读取

该操作在下一节中描述。

(1) Command without response and data

a. Flag register clear
First, clear the bits in the flag register. (SD_INFO1 and SD_INFO2)

b. Control register set
Set the SD/MMC clock and interrupt masking. (SD_CLK_CTRL, SD_INFO1_MASK, and SD_INFO2_MASK)

c. Command issue
Set CMD argument in SD_ARG and write to SD_CMD.
Accordingly, CMD is issued, and the operation is started.

d. Flag clear
When transmission of a command is completed, RSPEND (response end) in SD_INFO1 is set to 1 to generate an interrupt. Clear RSPEND to 0.

(2) Command without data

a. Flag register clear
First, clear the bits in the flag register. (SD_INFO1 and SD_INFO2)

b. Control register set
Set the SD/MMC clock and interrupt masking. (SD_CLK_CTRL, SD_INFO1_MASK, and SD_INFO2_MASK)

c. Command issue
Set CMD argument in SD_ARG and write to the SD_CMD.
Accordingly, CMD is issued, and the operation is started.

d. Flag clear
When a response is received, RSPEND (response end) in SD_INFO1 is set to 1 to generate an interrupt. Clear RSPEND to 0.

e. Read a response from SD_RSP10. Additionally, perform error processing (clear the interrupt flag register) if a communication error or timeout occurs.

43.3.6 Single Block Read (SD/MMC)

Figure 43.11 shows an example flow of a single block read operation.

(1) 没有响应和数据的命令

一个。标志寄存器清除
首先，清除标志寄存器中的位。（SD_INFO1和SD_INFO2）

湾。控制寄存器组
设置SDMMC时钟和中断屏蔽。（SD_CLK_CTRL、SD_INFO1_MASK和SD_INFO2_MASK）

C。命令问题
在SD_ARG中设置CMD参数并写入SD_CMD。因此，
发出CMD，并开始操作。

d。标志清除
当命令传输完成时，SD_INFO1中的RSPEND（响应结束）设置为1以产生中断。将RSPEND清除为0。

(2) 没有数据的命令

一个。标志寄存器清除
首先，清除标志寄存器中的位。（SD_INFO1和SD_INFO2）

湾。控制寄存器组
设置SDMMC时钟和中断屏蔽。（SD_CLK_CTRL、SD_INFO1_MASK和SD_INFO2_MASK）

C。命令问题
在SD_ARG中设置CMD参数并写入SD_CMD。
因此，发出CMD，并开始操作。

d。标志清除
当收到响应时，SD_INFO1中的RSPEND（响应结束）置1以产生中断。清除
RSPEND to 0.

e.从SD_RSP10读取响应。此外，如果发生通信错误或超时，请执行错误处理（清除中断标志寄存器）。

43.3.6 单块读取(SDMMC)

图43.11显示了单块读取操作的示例流程。

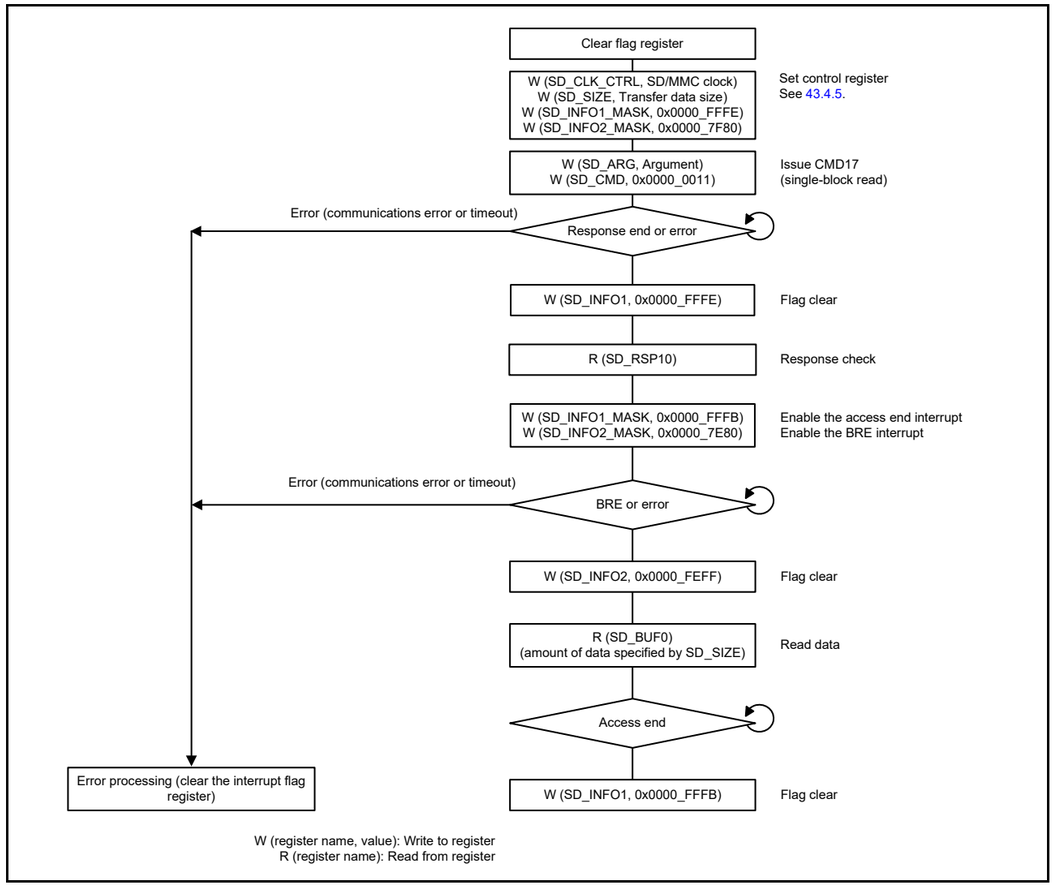


Figure 43.11 Example flow of single block read operation

43.3.6.1 Single block read operation

The operation of the single block read is described as follows:

a. Flag register clear
First, clear the bits in the flag register (SD_INFO1 and SD_INFO2).

b. Control register set
Set the SD/MMC clock, transfer data size, interrupt mask (SD_CLK_CTRL, SD_SIZE, SD_INFO1_MASK, and SD_INFO2_MASK).

c. Command issue (CMD17)
Set CMD17 argument in SD_ARG and write 0x0000_0011 to SD_CMD. CMD17 is issued and the single block read operation is started.

d. Response check
On receiving the response, RSPEND (response end) in SD_INFO1 is set to 1 to generate an interrupt. Clear RSPEND to 0 and read the response from SD_RSP10. If the result of response decoding is an error, the command sequence can be halted by setting the STP bit in SD_STP or the IOABT bit in SDIO_MODE to 1. In addition, this causes CMD12 and CMD52 to not be issued. If the ACEND bit (access end) in SD_INFO1 is set, halting the command sequence also leads to the generation of an interrupt.

e. Data receive from SD card/MMC and data read
Write 0x0000_FFFB to SD_INFO1_MASK to enable the access end interrupt. In addition, write 0x0000_7E80

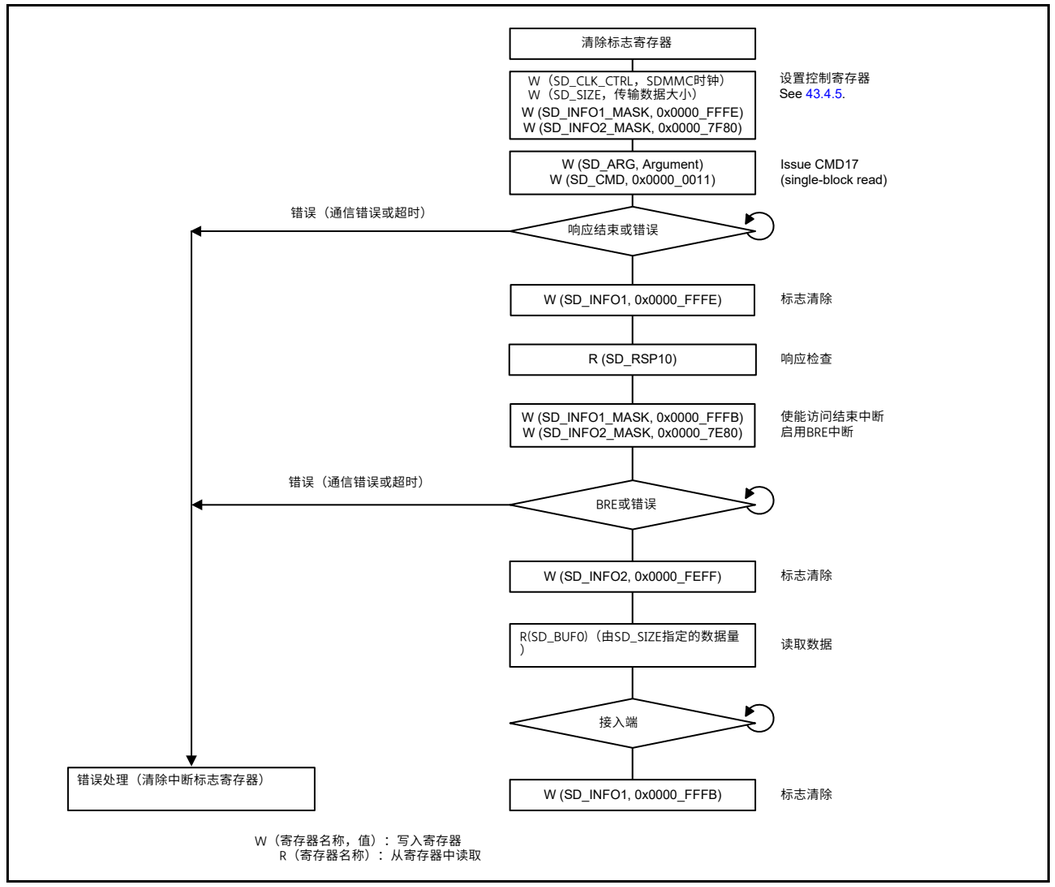


Figure 43.11 单块读操作示例流程

43.3.6.1 单块读操作

单块读取的操作描述如下：

一个。标志寄存器清除
首先，清除标志寄存器（SD_INFO1和SD_INFO2）中的位。

湾。控制寄存器组
设置SDMMC时钟、传输数据大小、中断屏蔽（SD_CLK_CTRL、SD_SIZE、SD_INFO1_MASK和SD_INFO2_MASK).

C。命令问题(CMD17)
在SD_ARG中设置CMD17参数并将0x0000_0011写入SD_CMD。发出CMD17并开始单块读取操作。

d。响应检查
收到响应后，SD_INFO1中的RSPEND（响应结束）置1以产生中断。清除RSPEND为0并从SD_RSP10读取响应。如果响应解码的结果是错误的，可以通过将SD_STP中的STP位或SDIO_MODE中的IOABT位设置为1来暂停命令序列。此外，这会导致CMD12和CMD52不发出。如果SD_INFO1中的ACEND位（访问结束）被设置，停止命令序列也会导致产生中断。

e.从SD卡MMC接收数据并读取数据
将0x0000_FFFB写入SD_INFO1_MASK以使能访问结束中断。另外，写入0x0000_7E80

to SD_INFO2_MASK to enable the BRE interrupt. When the data received from the SD card/MMC is completed, the BRE bit in SD_INFO2 is set to 1 to generate an interrupt. Clear the BRE bit to 0 and read the amount of data specified in SD_SIZE from SD_BUF0.
A communication error or timeout might be generated if data is being received while reading of SD_BUF0 is in progress.

f. Operation complete
When the data read from SD_BUF0 is completed, ACEND (access end) in SD_INFO1 is set to 1 to generate an interrupt. Clear ACEND to 0 to end the single block read operation.
Additionally, perform error processing (clear the interrupt flag register) if a communication error or timeout occurs.

43.3.7 Single Block Write (SD/MMC)

Figure 43.12 shows an example flow of a single block write operation.

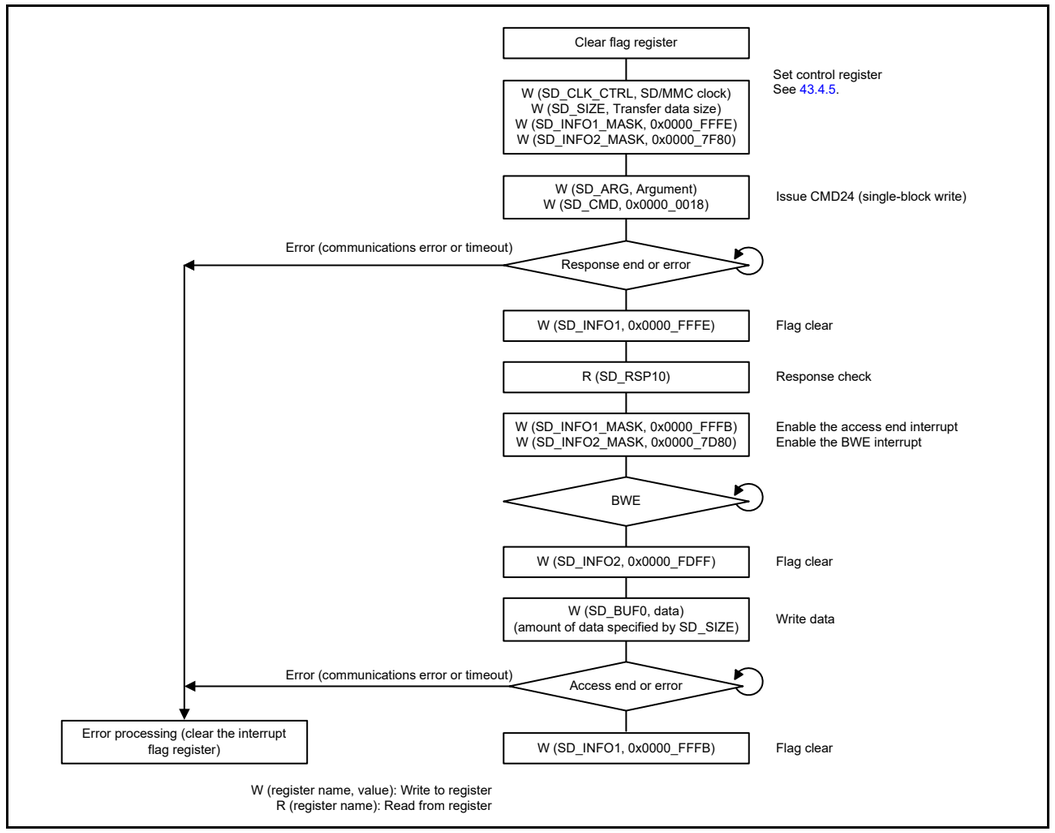


Figure 43.12 Example of single block write operation

到SD_INFO2_MASK以启用BRE中断。当从SD卡MMC接收到数据完成时，SD_INFO2中的BRE位设置为1以产生中断。将BRE位清0并从SD_BUF0中读取SD_SIZE中指定的数据量。如果在读取SD_BUF0时正在接收数据，则可能会产生通信错误或超时。

F。操作完成
当从SD_BUF0读取数据完成后，SD_INFO1中的ACEND（访问结束）置1以产生中断。将ACEND清0结束单块读操作。此外，如果发生通信错误或超时，请执行错误处理（清除中断标志寄存器）。

43.3.7 单块写入(SDMMC)

图43.12显示了单个块写入操作的示例流程。

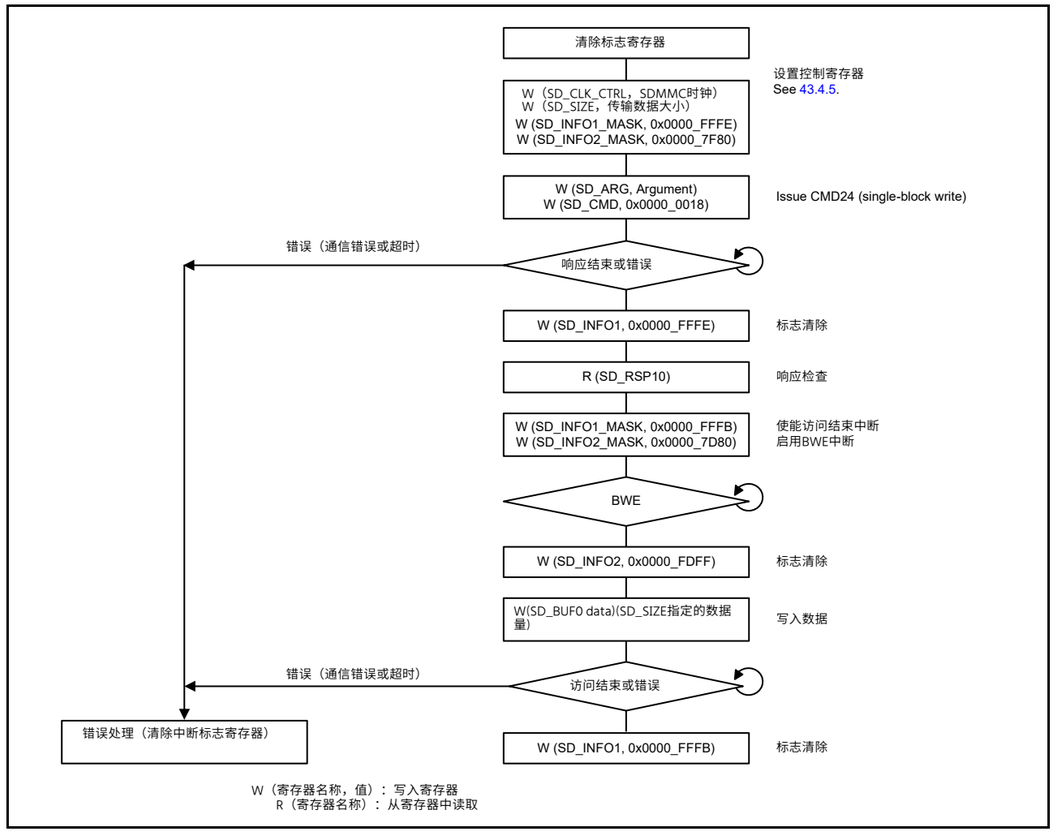


Figure 43.12 单块写操作示例

43.3.7.1 Single block write operation

The operation of the single block write is described as follows:

a. Flag register clear
First, clear the bits in the flag register (SD_INFO1 and SD_INFO2).

b. Control register set
Set the SD/MMC clock, transfer data size, interrupt mask (SD_CLK_CTRL, SD_SIZE, SD_INFO1_MASK, and SD_INFO2_MASK).

c. Command issue (CMD24)
Set CMD24 argument in SD_ARG and write 0x0000_0018 to SD_CMD. CMD24 is issued and the single block write operation is started.

d. Response check
On receiving the response, RSPEND (response end) in SD_INFO1 is set to 1 to generate an interrupt. Clear RSPEND to 0 and read the response from SD_RSP10. If the result of response decoding is an error, the command sequence can be halted by setting the STP bit in SD_STP or the IOABT bit in SDIO_MODE to 1. In addition, this causes CMD12 and CMD52 to not be issued. If the ACEND bit (access end) in SD_INFO is set, halting the command sequence also leads to the generation of an interrupt.

e. Data write and data transmit to SD card/MMC
Write 0x0000_FFFB to SD_INFO1_MASK to enable the access end interrupt. In addition, write 0x0000_7D80 to SD_INFO2_MASK to enable the BWE interrupt. When SD_BUF0 is ready for the data to be written, the BWE bit in SD_INFO2 is set to 1 to generate an interrupt. Clear the BWE bit to 0 and write the amount of data specified in SD_SIZE to SD_BUF0. When the data write to SD_BUF0 is completed, data is transmitted to the SD card. Then, the CRC status and busy state are received from the SD card/MMC.
However, a communications error or timeout might be generated if data is being transmitted after writing to SD_BUF0.

f. Operation complete
When the CRC status and busy state are received from the SD card/MMC, ACEND (access end) in SD_INFO1 is set to 1 to generate an interrupt. Clear the ACEND bit to 0 to end the single block write operation.
In addition, perform error processing (clear the interrupt flag register) if a communication error or timeout occurs.

43.3.8 Multiple Block Read (SD/MMC)

Figure 43.13 shows an example flow of a multiple block read operation.

43.3.7.1 单块写操作

单块写操作描述如下：

一个。标志寄存器清除
首先，清除标志寄存器（SD_INFO1和SD_INFO2）中的位。

湾。控制寄存器组
设置SDMMC时钟、传输数据大小、中断屏蔽（SD_CLK_CTRL、SD_SIZE、SD_INFO1_MASK和SD_INFO2_MASK).

C。命令问题(CMD24)
在SD_ARG中设置CMD24参数并将0x0000_0018写入SD_CMD。发出CMD24并开始单块写入操作。

d。响应检查
收到响应后，SD_INFO1中的RSPEND（响应结束）置1以产生中断。清除RSPEND为0并从SD_RSP10读取响应。如果响应解码的结果是错误的，可以通过将SD_STP中的STP位或SDIO_MODE中的IOABT位设置为1来暂停命令序列。此外，这会导致CMD12和CMD52不发出。如果SD_INFO中的ACEND位（访问结束）被设置，停止命令序列也会导致中断的产生。

e.数据写入和数据传输到SD卡MMC
将0x0000_FFFB写入SD_INFO1_MASK以使能访问结束中断。此外，将0x0000_7D80写入SD_INFO2_MASK以启用BWE中断。当SD_BUF0准备好写入数据时，SD_INFO2中的BWE位设置为1以产生中断。将BWE位清除为0，并将SD_SIZE中指定的数据量写入SD_BUF0。数据写入SD_BUF0完成后，将数据传输到SD卡。然后，从SD卡MMC接收CRC状态和忙状态。

但是，如果在写入后正在传输数据，则可能会产生通信错误或超时
SD_BUF0.

F。操作完成
当从SD卡MMC接收到CRC状态和忙状态时，SD_INFO1中的ACEND（访问端）置1以产生中断。将ACEND位清0以结束单块写操作。此外，如果发生通信错误或超时，请执行错误处理（清除中断标志寄存器）。

43.3.8 多块读取(SDMMC)

图43.13显示了多块读取操作的示例流程。

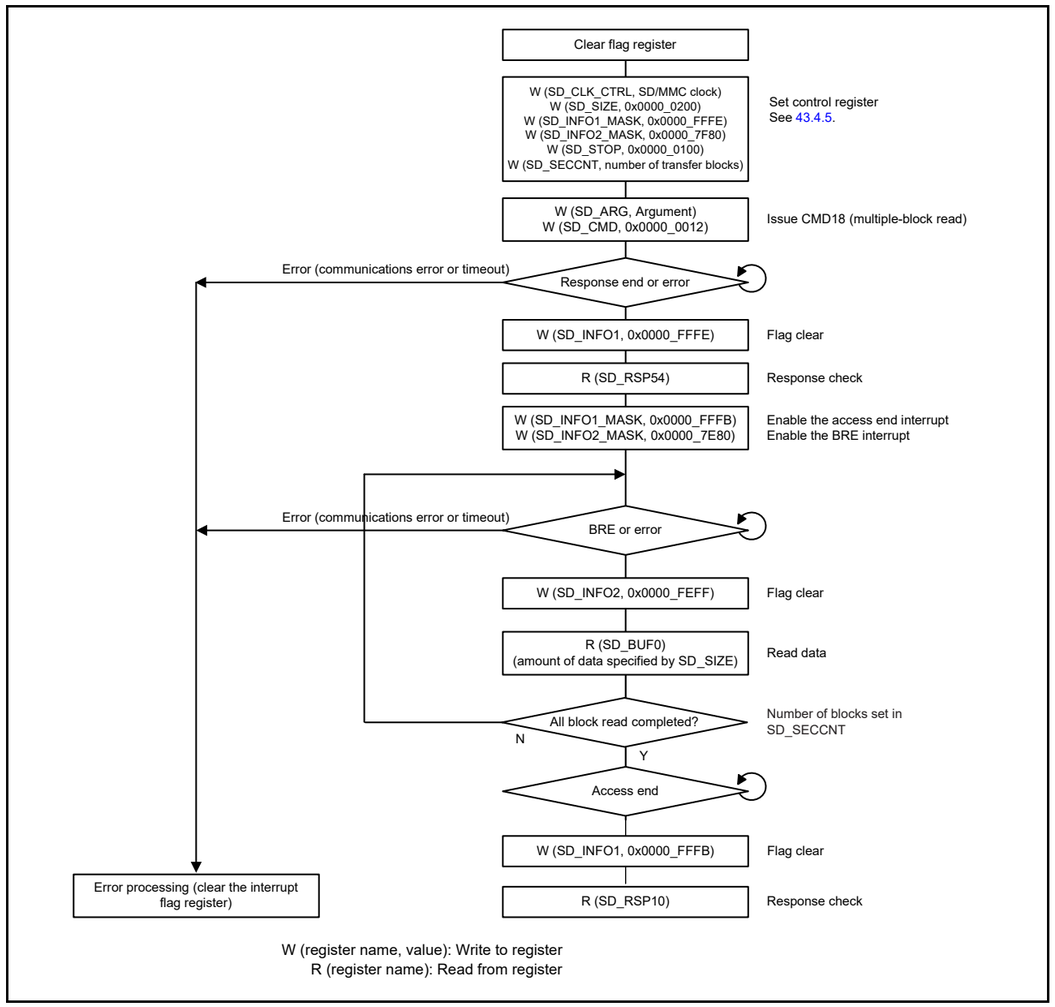


Figure 43.13 Example of multiple block read operation

43.3.8.1 Multiple block read operation

The operation of the multiple block read is described as follows:

a. Flag register clear
First, clear the bits in the flag register (SD_INFO1 and SD_INFO2).

b. Control register set
Set the SD/MMC clock, transfer data size, interrupt mask (SD_CLK_CTRL, SD_SIZE, SD_INFO1_MASK, and SD_INFO2_MASK).
Set SEC in SD_STOP to 1, and set the number of transfer blocks in SD_SECCNT.

c. Command issue (CMD18)
Set CMD18 argument in SD_ARG and write 0x0000_0012 to SD_CMD. CMD18 is issued and the multiple block read operation is started.

d. Response check
On receiving the response, RSPEND (response end) in SD_INFO1 is set to 1 to generate an interrupt. Clear

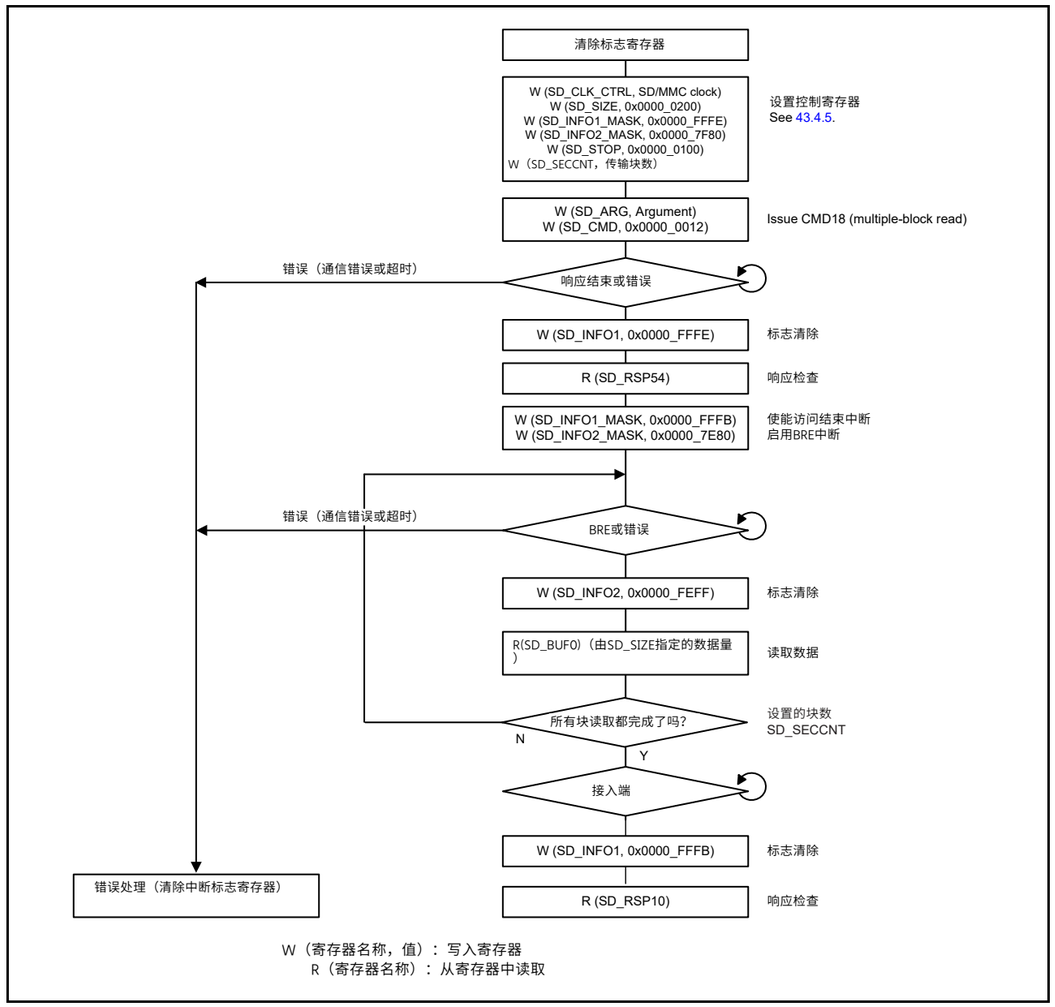


Figure 43.13 多块读取操作示例

43.3.8.1 多块读操作

多块读取的操作描述如下：

一个。标志寄存器清除
首先，清除标志寄存器（SD_INFO1和SD_INFO2）中的位。

湾。控制寄存器组
设置SDMMC时钟、传输数据大小、中断屏蔽（SD_CLK_CTRL、SD_SIZE、SD_INFO1_MASK和SD_INFO2_MASK).
将SD_STOP中的SEC设置为1，并在SD_SECCNT中设置传输块数。

C。命令问题(CMD18)
在SD_ARG中设置CMD18参数并将0x0000_0012写入SD_CMD。发出CMD18并开始多块读取操作。

d。响应检查
收到响应后，SD_INFO1中的RSPEND（响应结束）置1以产生中断。清除

RSPEND to 0 and read the response from SD_RSP54. If the result of response decoding is an error, the command sequence can be halted by setting the STP bit in SD_STP to 1. Setting the STP bit to 1 also causes CMD12 to be issued and the response received. If the command sequence is halted because the access end interrupt is enabled, an interrupt is generated when the ACEND bit (access end) bit in SD_INFO1 sets to 1 on completion of response reception. Clear the ACEND bit to 0 and read the response.

e. Data receive from SD card/MMC and data read
Write 0x0000_FFFB to SD_INFO1_MASK to enable the access end interrupt. In addition, write 0x0000_7E80 to SD_INFO2_MASK to enable the BRE interrupt. When one-block data received from the SD card/MMC is completed, the BRE bit in SD_INFO2 is set to 1 to generate an interrupt. Clear the BRE bit to 0 and read the amount of data specified in SD_SIZE from SD_BUF0. Doing this repeats transfer of the number of blocks set in SD_SECCNT. However, a communication error or timeout might be generated if data is being received while reading of SD_BUF0 is in progress. CMD12 is automatically issued to stop multiblock transfer with the number of blocks that is set to SD_SECCNT and the response is received. At this point, CMD12 argument is automatically set to 0x0000_0000.

f. Operation complete
When all-block data read and the CMD12 response received are completed, ACEND (access end) in SD_INFO1 is set to 1 to generate an interrupt. Clear ACEND to 0 to read the response. This is the end of multiple block read operation. In addition, perform error processing (clear the interrupt flag register) if a communication error or timeout occurs.

43.3.9 Multiple Block Write (SD/MMC Using Internal Timer)

Figure 43.14 shows an example flow of a multiple block write using internal timer.

RSPEND为0并从SD_RSP54读取响应。如果响应解码的结果是错误的，可以通过将SD_STP中的STP位设置为1来暂停命令序列。将STP位设置为1也会导致发出CMD12并接收响应。如果由于使能访问结束中断而暂停命令序列，则在完成响应接收时SD_INFO1中的ACEND位（访问结束）位设置为1时产生中断。将ACEND位清0并读取响应。

e.从SD卡MMC接收数据并读取数据
将0x0000_FFFB写入SD_INFO1_MASK以使能访问结束中断。此外，将0x0000_7E80写入SD_INFO2_MASK以启用BRE中断。当从SD卡MMC接收到单块数据完成时，SD_INFO2中的BRE位被设置为1以产生中断。将BRE位清0并从SD_BUF0中读取SD_SIZE中指定的数据量。这样做会重复传输SD_SECCNT中设置的块数。但是，如果在读取SD_BUF0时正在接收数据，则可能会产生通信错误或超时。自动发出CMD12以停止多块传输，块数设置为SD_SECCNT并接收响应。此时，CMD12参数自动设置为0x0000_0000。

F。操作完成
当全块数据读取和接收到的CMD12响应完成时，SD_INFO1中的ACEND（访问结束）置1以产生中断。将ACEND清除为0以读取响应。这是多块读取操作的结束。此外，如果发生通信错误或超时，请执行错误处理（清除中断标志寄存器）。

43.3.9 多块写入（使用内部定时器的SDMMC）

图43.14显示了使用内部定时器进行多块写入的示例流程。

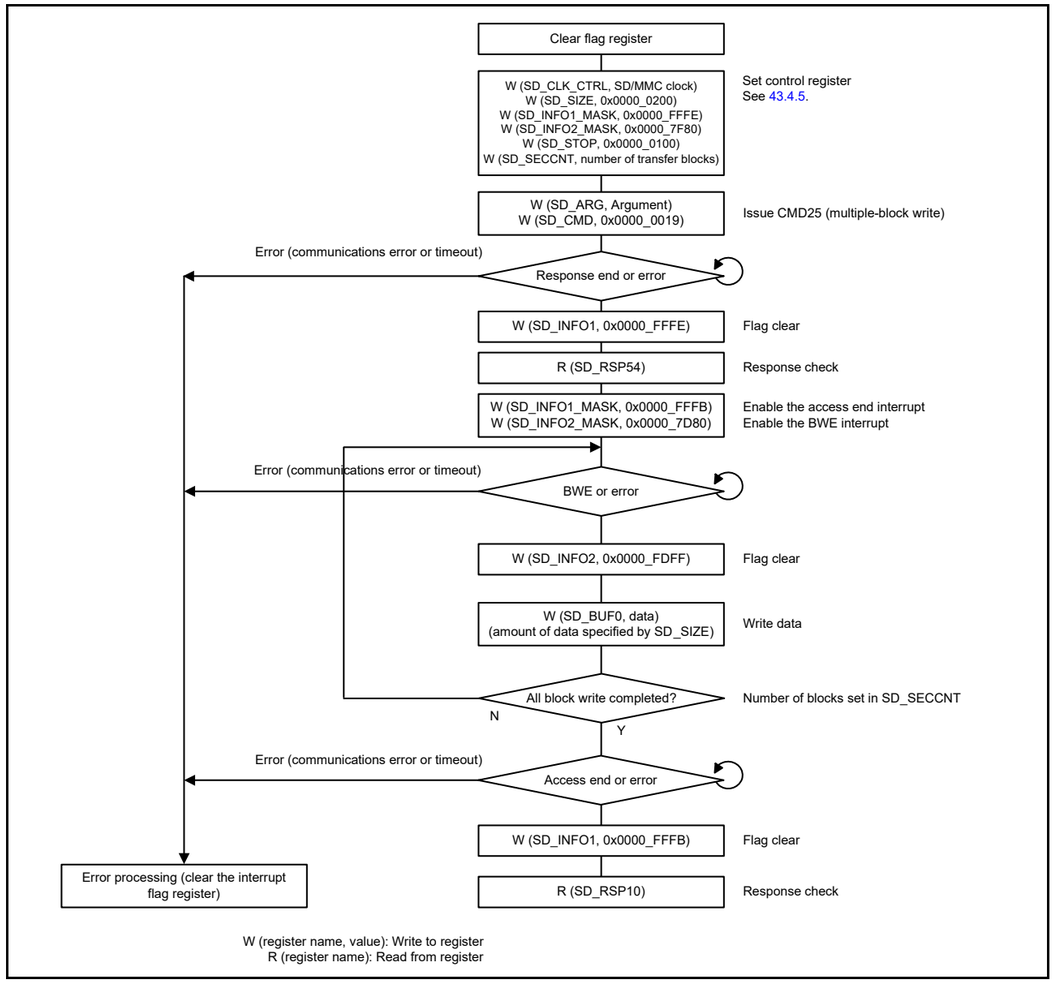


Figure 43.14 Example of multiple block write operation using internal timer

43.3.9.1 Multiple block write operation using internal timer

The operation of the multiple block write is described as follows:

a. Flag register clear
First, clear the bits in the flag register (SD_INFO1 and SD_INFO2).

b. Control register set
Set the SD/MMC clock, transfer data size, interrupt mask (SD_CLK_CTRL, SD_SIZE, SD_INFO1_MASK, and SD_INFO2_MASK).
Set the SEC bit in SD_STOP to 1, and set the number of transfer blocks in SD_SECCNT.

c. Command issue (CMD25)
Set CMD25 argument in SD_ARG and write 0x0000_0019 to SD_CMD. CMD25 is issued and the multiple block write operation is started.

d. Response check
On receiving the response, the RSPEND bit (response end) in SD_INFO1 is set to 1 to generate an interrupt.
Clear the RSPEND bit to 0 and read the response from SD_RSP54. If the result of response decoding is an error,

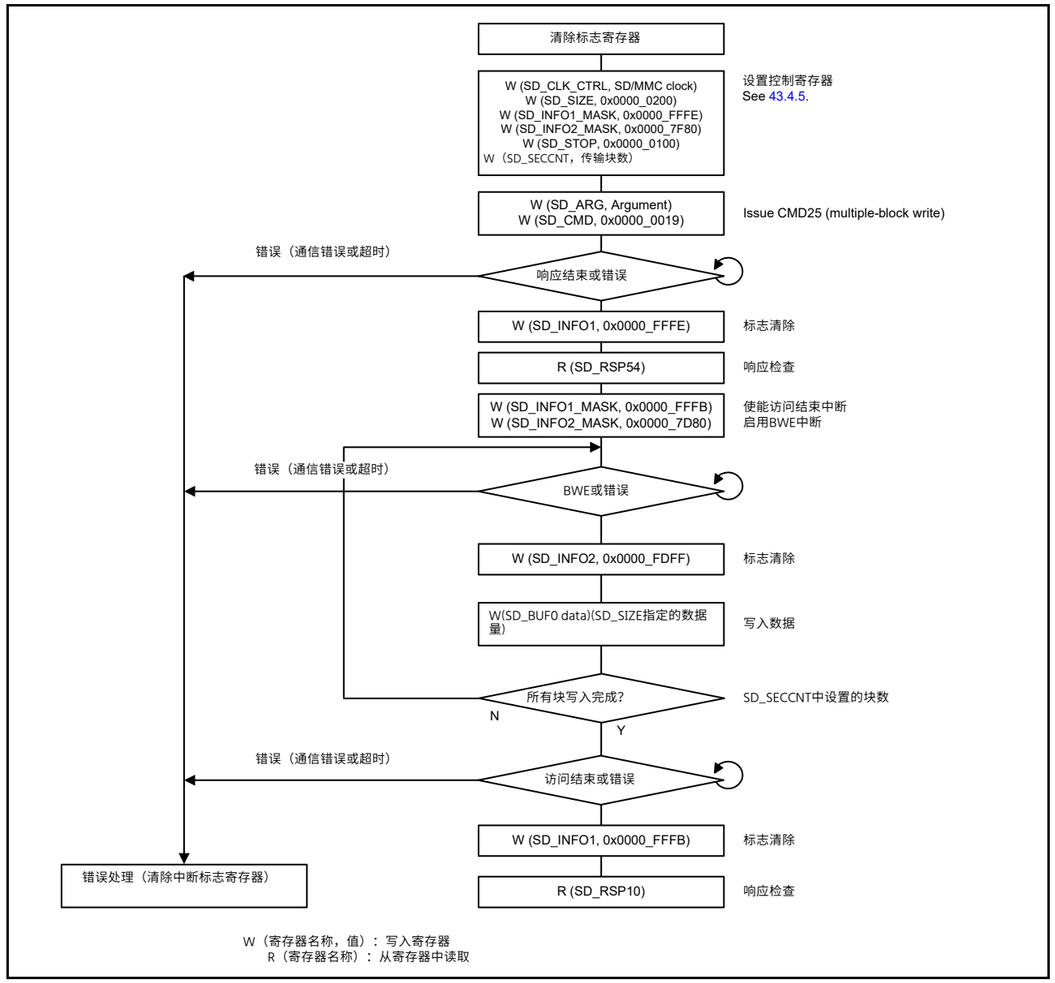


Figure 43.14 使用内部定时器的多块写入操作示例

43.3.9.1 使用内部定时器的多块写操作

多块写入的操作描述如下：

一个。标志寄存器清除
首先，清除标志寄存器（SD_INFO1和SD_INFO2）中的位。

湾。控制寄存器组
设置SDMMC时钟、传输数据大小、中断屏蔽（SD_CLK_CTRL、SD_SIZE、SD_INFO1_MASK和SD_INFO2_MASK).
将SD_STOP中的SEC位设置为1，并在SD_SECCNT中设置传输块数。

C。命令问题(CMD25)
在SD_ARG中设置CMD25参数并将0x0000_0019写入SD_CMD。发出CMD25并开始多块写入操作。

d。响应检查
收到响应后，SD_INFO1中的RSPEND位（响应结束）置1以产生中断。
将RSPEND位清0并从SD_RSP54读取响应。如果响应解码的结果是错误的，

the command sequence can be halted by setting the STP bit in SD_STP to 1. Setting the STP bit to 1 also causes CMD12 to be issued and the response received. If the command sequence is halted because the access end interrupt is enabled, an interrupt is generated by when the ACEND bit (access end) bit in SD_INFO1 sets to 1 on completion of response reception. Clear the ACEND bit to 0 and read the response.

e. Data write and data transmit to SD card/MMC
Write 0x0000_FFFB to SD_INFO1_MASK to enable the access end interrupt. In addition, write 0x0000_7D80 to SD_INFO2_MASK to enable the BWE interrupt. When SD_BUF0 is ready for the data to be written, the BWE bit in the SD_INFO2 resister is set to 1 to generate an interrupt. Clear the BWE bit to 0 and write the amount of data specified in SD_SIZE to SD_BUF0. When the data write to SD_BUF0 is completed, data is transmitted to the SD card/MMC. The CRC status and busy state are received from the SD card/MMC. This repeats transfer of the number of blocks set in SD_SECCNT. However, a communication error or timeout might be generated if data is being received while writing to SD_BUF0 is in progress. CMD12 is automatically issued to stop multiblock transfer with the number of blocks which is set to SD_SECCNT and the response is received. At this point, CMD12 argument is automatically set to 0x0000_0000.

f. Operation complete
When all-block data transmit and the CRC status receive are completed, the ACEND bit (access end) in SD_INFO1 is set to 1 to generate an interrupt. Clear the ACEND bit to 0 to read the response. This is the end of multiple block write operation. Additionally, perform error processing (clear the interrupt flag register) if a communications error or timeout occurs.

43.3.10 Multiple Block Write (MMC using external timer)

Figure 43.15 shows an example flow of a multiple block write using an external timer.

可以通过将SD_STP中的STP位设置为1来停止命令序列。将STP位设置为1也会导致发出CMD12并接收响应。如果由于使能访问结束中断而暂停命令序列，则在完成响应接收时SD_INFO1中的ACEND位（访问结束）位设置为1时产生中断。将ACEND位清0并读取响应。

e.数据写入和数据传输到SD卡MMC
将0x0000_FFFB写入SD_INFO1_MASK以使能访问结束中断。此外，将0x0000_7D80写入SD_INFO2_MASK以启用BWE中断。当SD_BUF0准备好写入数据时，SD_INFO2寄存器中的BWE位设置为1以产生中断。将BWE位清除为0，并将SD_SIZE中指定的数据量写入SD_BUF0。当数据写入SD_BUF0完成后，数据被传输到SD卡MMC。从SD卡MMC接收CRC状态和忙状态。这将重复传输SD_SECCNT中设置的块数。但是，如果在写入SD_BUF0时正在接收数据，则可能会产生通信错误或超时。自动发出CMD12以停止多块传输，块数设置为SD_SECCNT并接收响应。此时，CMD12参数自动设置为0x0000_0000。

F。操作完成
当全块数据发送和CRC状态接收完成时，ACEND位（访问结束）在
SD_INFO1设置为1以产生中断。将ACEND位清0以读取响应。这是多块写操作的结束。此外，如果发生通信错误或超时，请执行错误处理（清除中断标志寄存器）。

43.3.10 多块写入（使用外部定时器的MMC）

图43.15显示了使用外部定时器进行多块写入的示例流程。

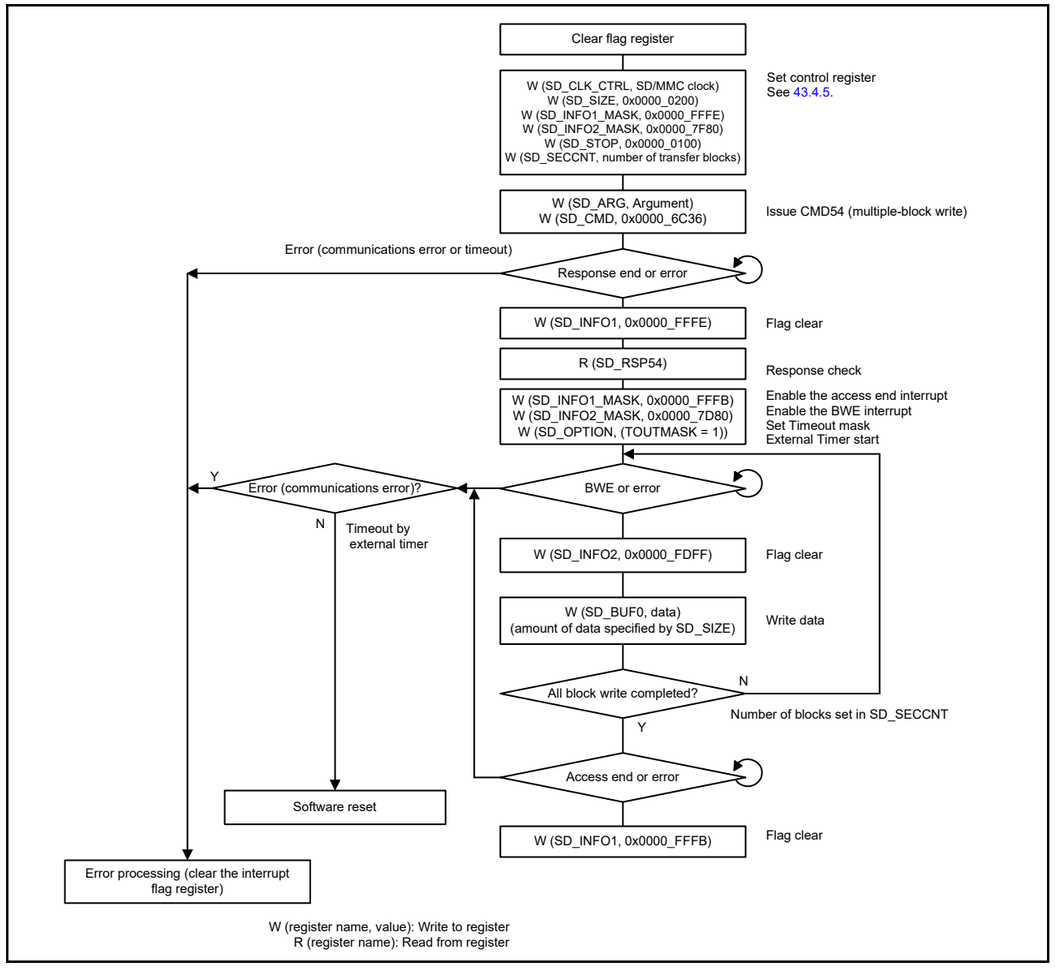


Figure 43.15 Example of multiple block write operation using external timer

43.3.10.1 Multiple block write operation using external timer

The operation of the multiple block write is described as follows:

a. Flag register clear
First, clear the bits in the flag register (SD_INFO1 and SD_INFO2).

b. Control register set
Set the MMC clock, transfer data size, interrupt mask (SD_CLK_CTRL, SD_SIZE, SD_INFO1_MASK, and SD_INFO2_MASK).
Set the SEC bit in SD_STOP to 1, and set the number of transfer blocks in SD_SECCNT.

c. Command issue (CMD54)
Set CMD54 Argument in SD_ARG and write 0x0000_6C36 to SD_CMD. CMD54 is issued and the multiple block write operation is started.

d. Response check
On receiving the response, the RSPEND bit (response end) in SD_INFO1 is set to 1 to generate an interrupt. Clear the RSPEND bit to 0 and read the response from SD_RSP54. If the result of response decoding is an error, the command sequence can be halted by setting the STP bit in SD_STP to 1. Setting the STP bit to 1 also causes

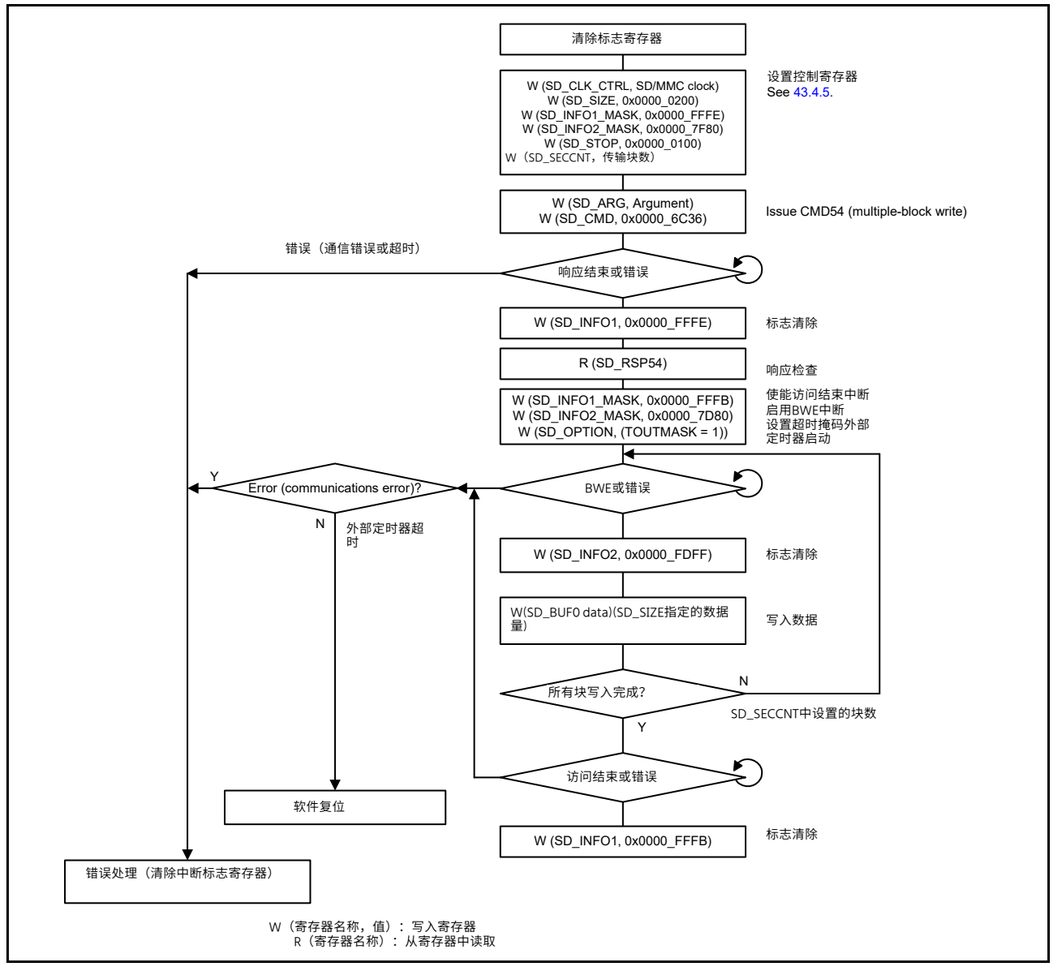


Figure 43.15 使用外部定时器的多块写入操作示例

43.3.10.1 使用外部定时器的多块写操作

多块写入的操作描述如下：

一个。标志寄存器清除
首先，清除标志寄存器（SD_INFO1和SD_INFO2）中的位。

湾。控制寄存器组
设置MMC时钟、传输数据大小、中断屏蔽（SD_CLK_CTRL、SD_SIZE、SD_INFO1_MASK和SD_INFO2_MASK).
将SD_STOP中的SEC位设置为1，并在SD_SECCNT中设置传输块数。

C。命令问题(CMD54)
在SD_ARG中设置CMD54参数并将0x0000_6C36写入SD_CMD。发出CMD54并开始多块写入操作。

d。响应检查
收到响应后，SD_INFO1中的RSPEND位（响应结束）置1以产生中断。
将RSPEND位清0并从SD_RSP54读取响应。如果响应解码的结果是错误的，可以通过将SD_STP中的STP位设置为1来暂停命令序列。将STP位设置为1也会导致

CMD12 to be issued and the response received. If the command sequence is halted because the access end interrupt is enabled, an interrupt is generated by when the ACEND bit (access end) bit in SD_INFO1 sets to 1 on completion of response reception. Clear the ACEND bit to 0 and read the response.

e. Data write and data transmit to MMC
Write 0x0000_FFFB to SD_INFO1_MASK to enable the access end interrupt, write 0x0000_7D80 to SD_INFO2_MASK to enable the BWE interrupt and set 1 to TOUTMASK of SD_OPTION to inactivate timeout. In addition, start external timer. When SD_BUF0 is ready for the data to be written, the BWE bit in the SD_INFO2 resister is set to 1 to generate an interrupt. Clear the BWE bit to 0 and write the amount of data specified in SD_SIZE to SD_BUF0. When the data write to SD_BUF0 is completed, data is transmitted to the MMC. The CRC status and busy state are received from the MMC. Doing this repeats transfer of the number of blocks set in SD_SECCNT. However, a communication error or timeout might be generated if data is being received while writing to SD_BUF0 is in progress.

f. Operation complete
When all-block data transmit and the CRC status receive are completed, the ACEND bit (access end) in SD_INFO1 is set to 1 to generate an interrupt. Clear the ACEND bit to 0 to read the response. This is the end of multiple block write operation. Additionally, perform error processing (clear the interrupt flag register) if a communications error or timeout occurs when receiving response. Execute software reset if a timeout by external timer occurs when transmitting data.

43.3.11 IO_RW_DIRECT Command (SD: CMD52)

Figure 43.16 shows an example flow of an IO_DIRECT command (CMD52) operation.

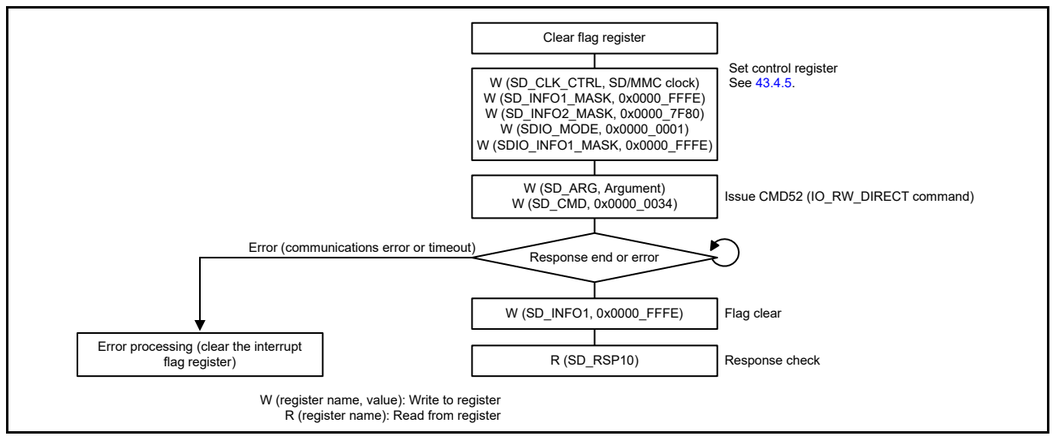


Figure 43.16 Example of IO_RW_DIRECT command (CMD52) operation

43.3.12 IO_RW_EXTENDED Command (SD: CMD53/Multiple Block Read)

Figure 43.17 shows an example flow for a CMD53 multiple block read operation.

发出CMD12并收到响应。如果由于使能访问结束中断而暂停命令序列，则在完成响应接收时SD_INFO1中的ACEND位（访问结束）位设置为1时产生中断。将ACEND位清0并读取响应。

e.数据写入和数据传输到MMC
向SD_INFO1_MASK写入0x0000_FFFB使能访问结束中断，向SD_INFO1_MASK写入0x0000_7D80
SD_INFO2_MASK启用BWE中断并将SD_OPTION的TOUTMASK设置为1以禁用超时。另外，启动外部定时器。当SD_BUF0准备好写入数据时，SD_INFO2寄存器中的BWE位设置为1以产生中断。将BWE位清除为0，并将SD_SIZE中指定的数据量写入SD_BUF0。当数据写入SD_BUF0完成后，数据被传输到MMC。从MMC接收CRC状态和忙碌状态。这样做会重复传输SD_SECCNT中设置的块数。但是，如果在写入SD_BUF0时正在接收数据，则可能会产生通信错误或超时。

F。操作完成
当全块数据发送和CRC状态接收完成时，ACEND位（访问结束）在
SD_INFO1设置为1以产生中断。将ACEND位清0以读取响应。这是多块写操作的结束。此外，如果在接收响应时发生通信错误或超时，请执行错误处理（清除中断标志寄存器）。如果在传输数据时发生外部定时器超时，则执行软件复位。

43.3.11 IO_RW_DIRECT Command (SD: CMD52)

图43.16显示了IO_DIRECT命令(CMD52)操作的示例流程。

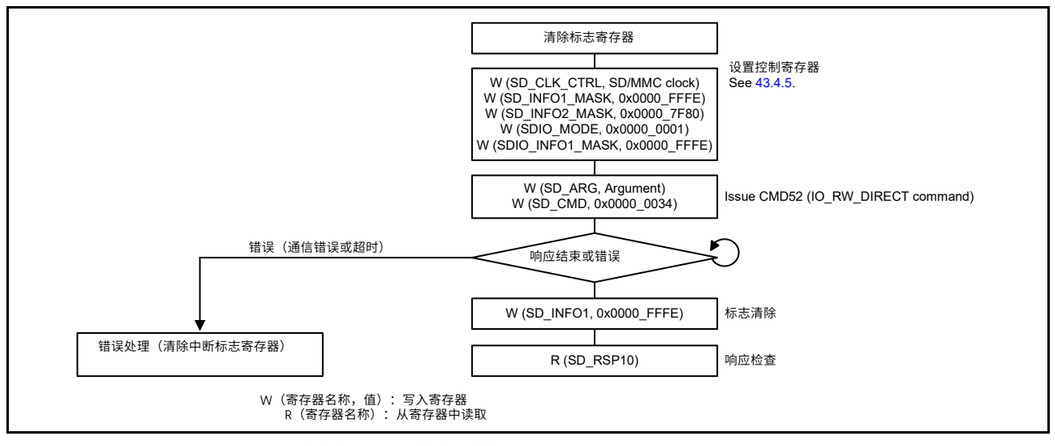


Figure 43.16 IO_RW_DIRECT命令(CMD52)操作示例

43.3.12 IO_RW_EXTENDED命令（SD：CMD53多块读取）

图43.17显示了CMD53多块读取操作的示例流程。

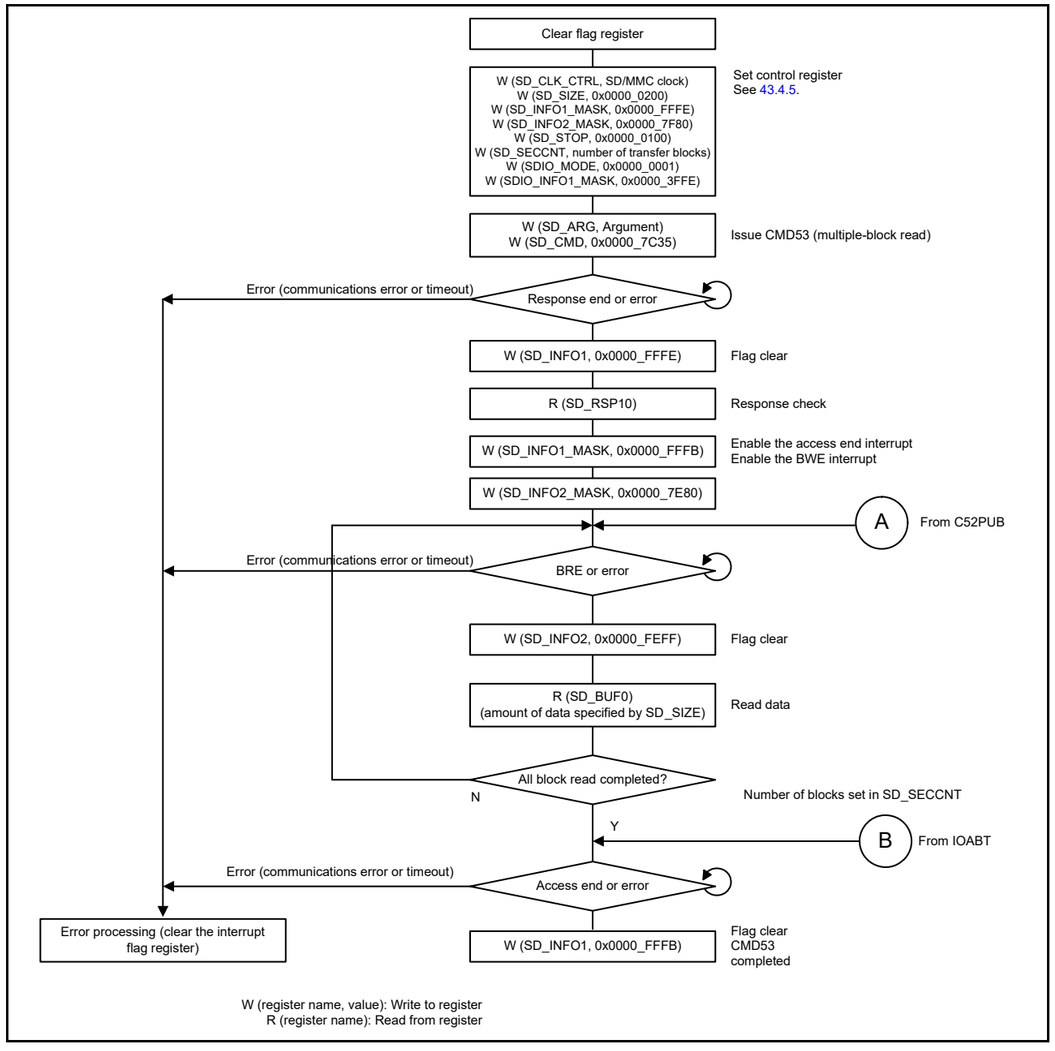


Figure 43.17 Example of IO_RW_EXTENDED command (CMD53) for multiple block read operation

Figure 43.18 shows an example flow when CMD52 (SDIO abort) is issued during a CMD53 multiple block read.

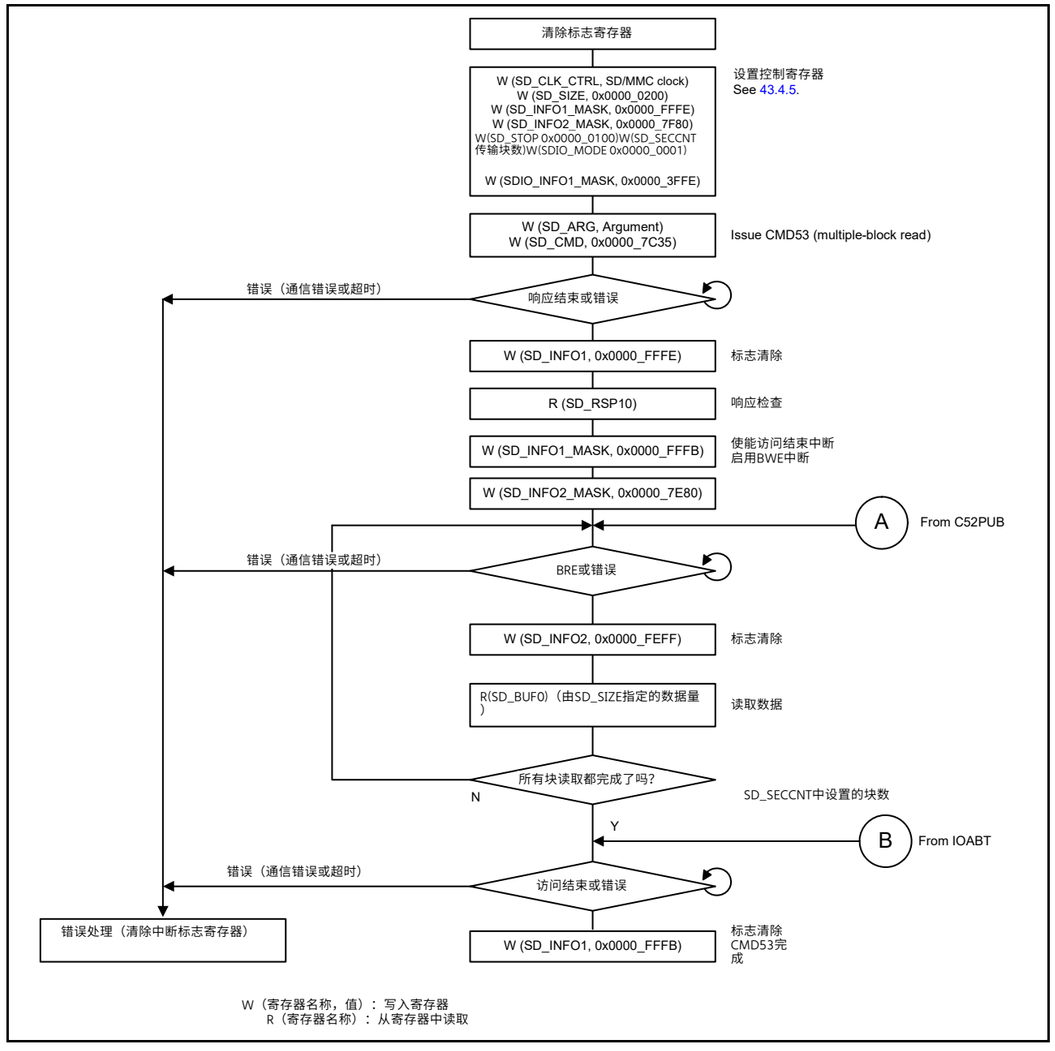


Figure 43.17 用于多块读取操作的IO_RW_EXTENDED命令(CMD53)示例

图43.18显示了在CMD53多块读取期间发出CMD52（SDIO中止）的示例流程。

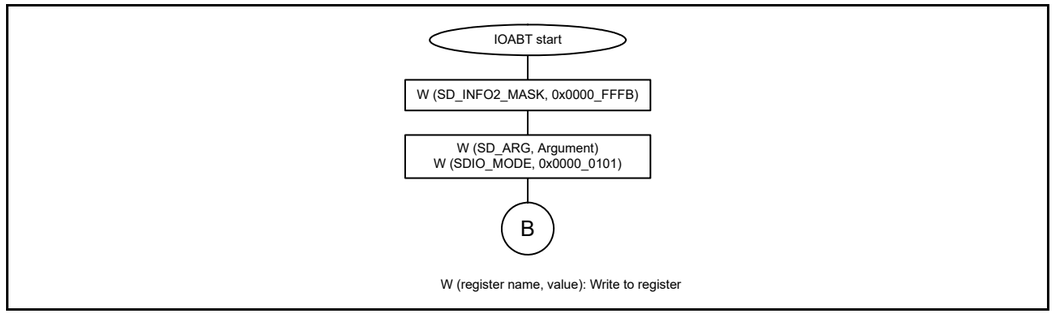


Figure 43.18 Flow when CMD52 (SDIO abort) is issued during a CMD53 multiple block read

Figure 43.19 shows an example flow when CMD52 (SDIO none abort) is issued at a CMD53 multiple block read while the SDHI is in the read wait state.

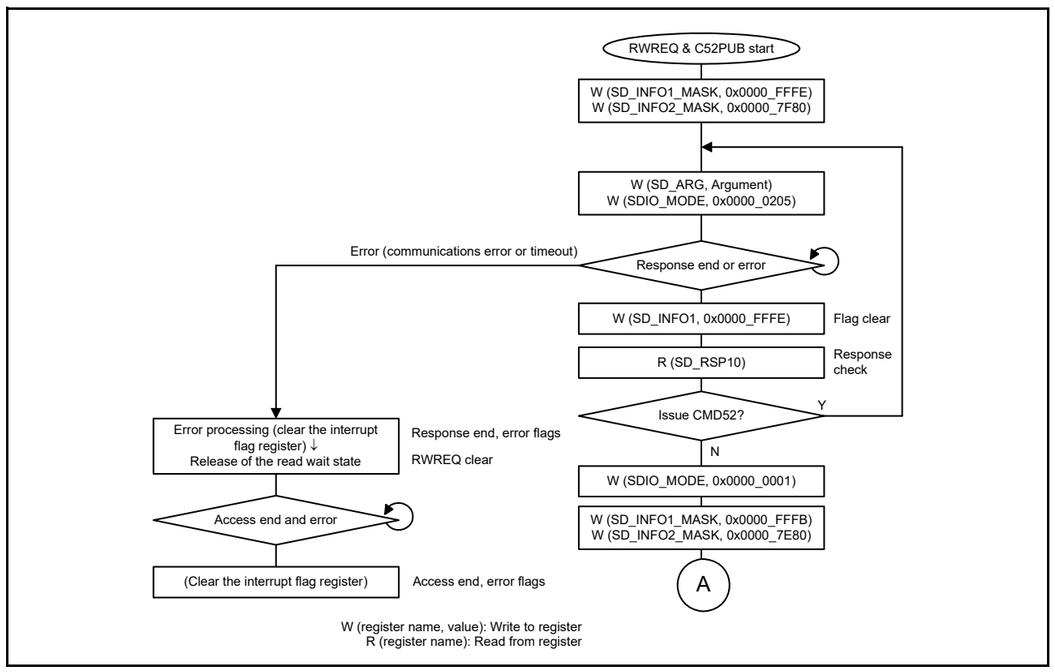


Figure 43.19 Flow when CMD52 (SDIO no abort) is issued during a CMD53 multiple block read while the SD Host Interface is in read wait state

43.3.13 IO_RW_EXTENDED Command (SD: CMD53/Multiple Block Write)

Figure 43.20 shows an example flow for a CMD53 multiple block write.

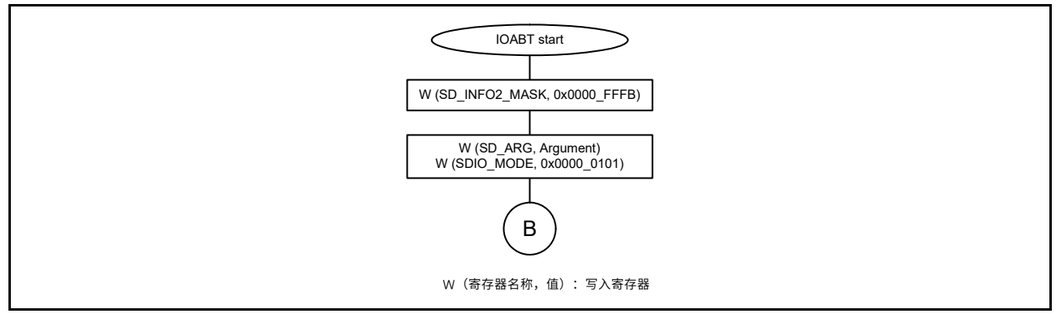


Figure 43.18 在CMD53多块读取期间发出CMD52（SDIO中止）时的流程

图43.19显示了一个示例流程，当SDHI处于读取等待状态时，在CMD53多块读取时发出CMD52（SDIO无中止）。

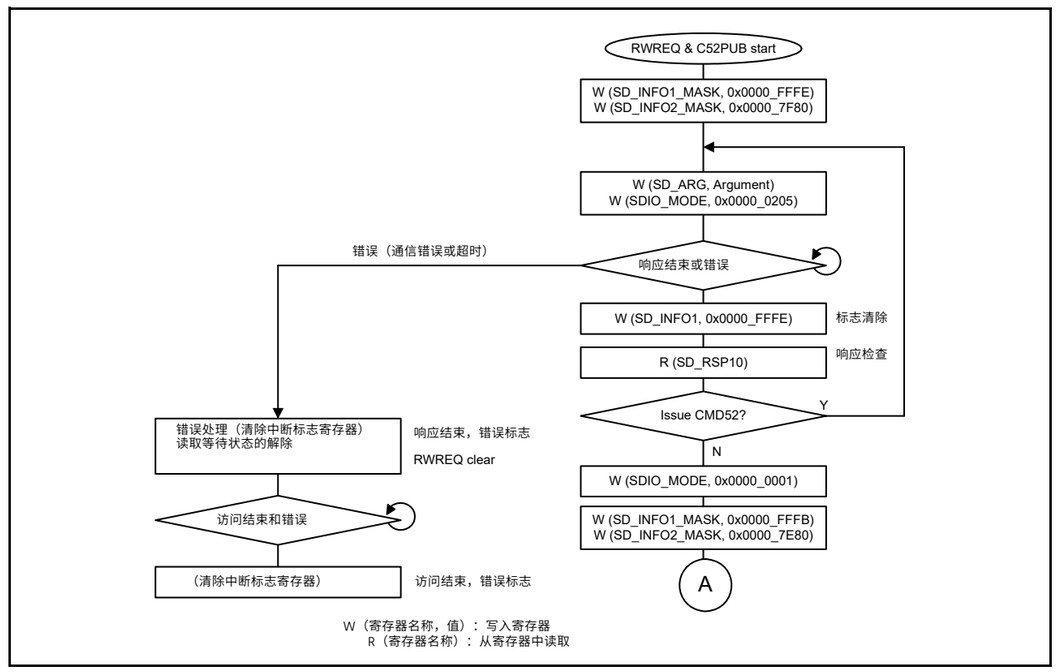


Figure 43.19 在CMD53多块读取期间发出CMD52（SDIO无中止）时的流程，而SD主机接口处于读取等待状态

43.3.13 IO_RW_EXTENDED命令（SD：CMD53多块写入）

图43.20显示了CMD53多块写入的示例流程。

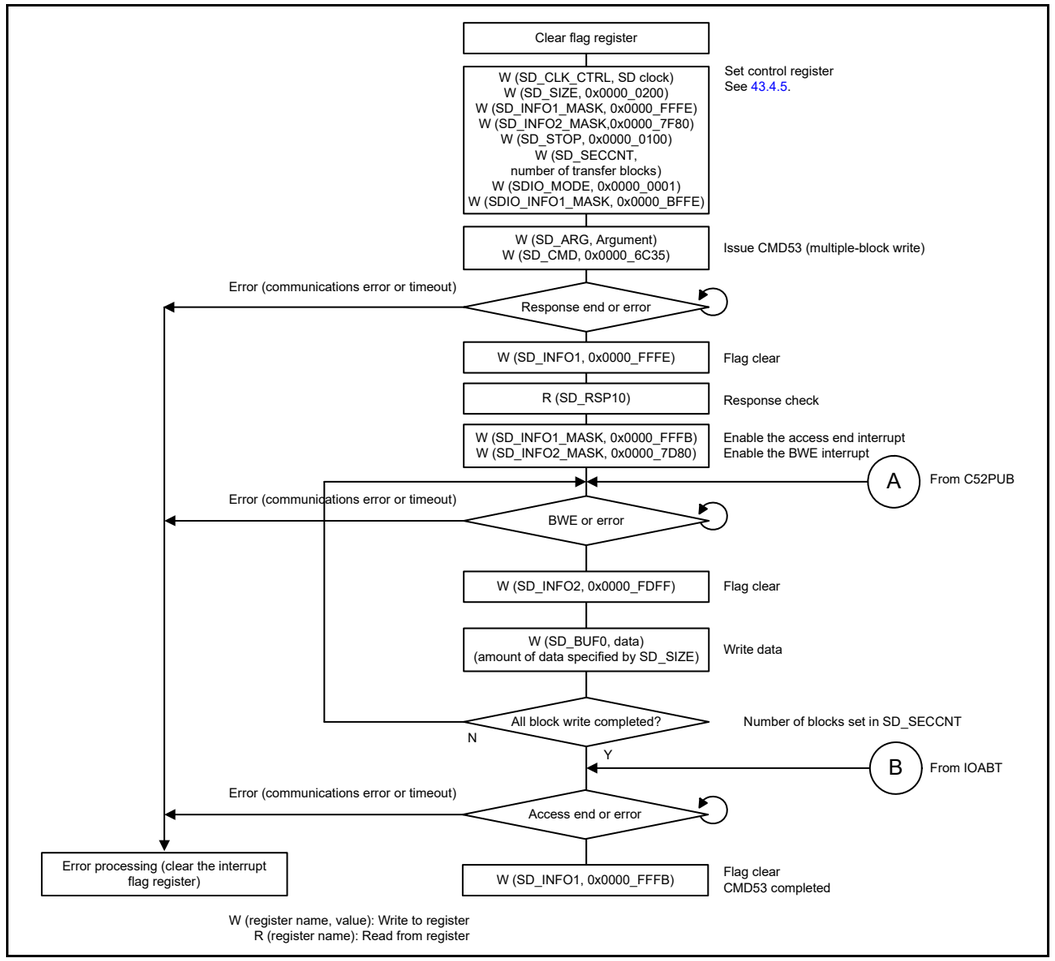


Figure 43.20 Example of IO_RW_EXTENDED command during a CMD53 multiple block write operation

Figure 43.21 shows an example flow when CMD52 (SDIO abort) is issued at CMD53 multiple block write.

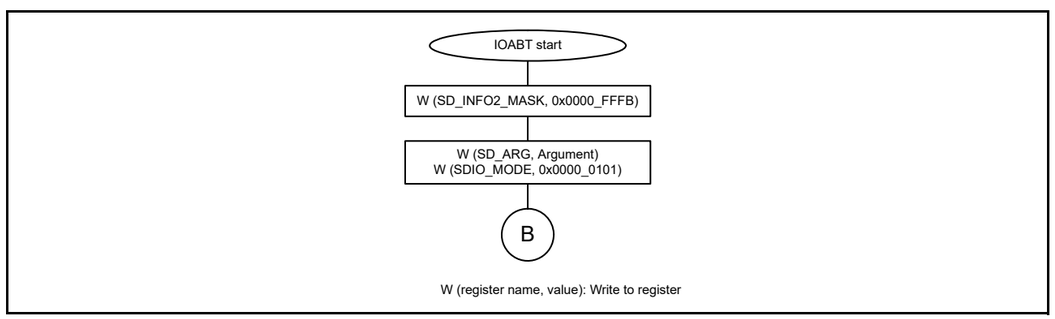


Figure 43.21 Flow when CMD52 (SDIO Abort) is issued during a CMD53 multiple block write

Figure 43.22 shows an example flow when CMD52 (SDIO none abort) is issued at CMD53 multiple block write.

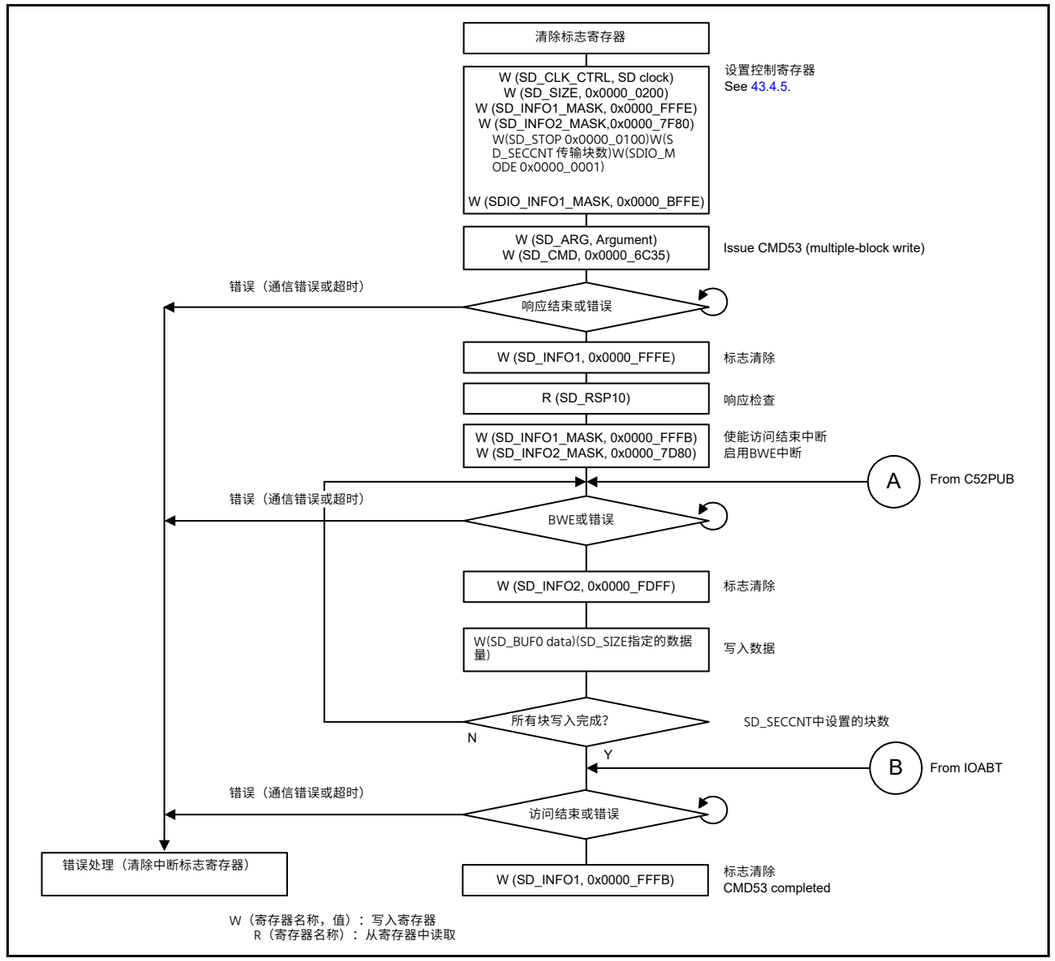


Figure 43.20 CMD53多块写入操作期间的IO_RW_EXTENDED命令示例

图43.21显示了在CMD53多块写入时发出CMD52（SDIO中止）的示例流程。

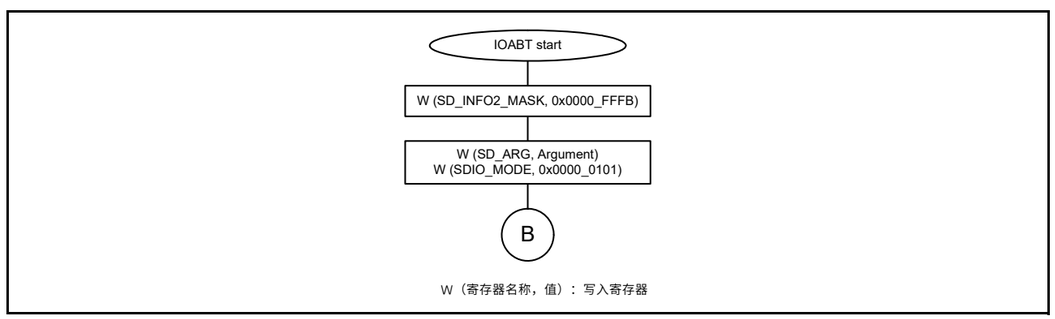


Figure 43.21 在CMD53多块写入期间发出CMD52（SDIO中止）时的流程

图43.22显示了在CMD53多块写入时发出CMD52（SDIO无中止）的示例流程。

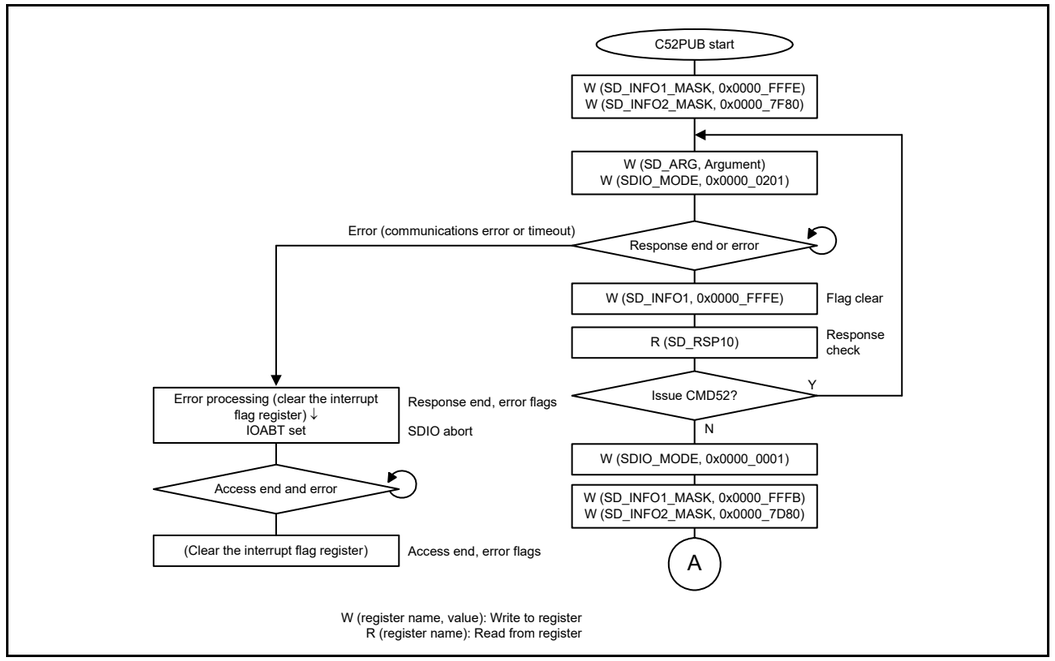


Figure 43.22 Flow when CMD52 (SDIO no abort) is issued during a CMD53 multiple block write

43.3.14 DMA Transfer (SD/MMC)

43.3.14.1 SD_BUF DMA transfer

Figure 43.23 shows an example flow for SD_BUF DMA read when CMD18 multiple block read is issued.

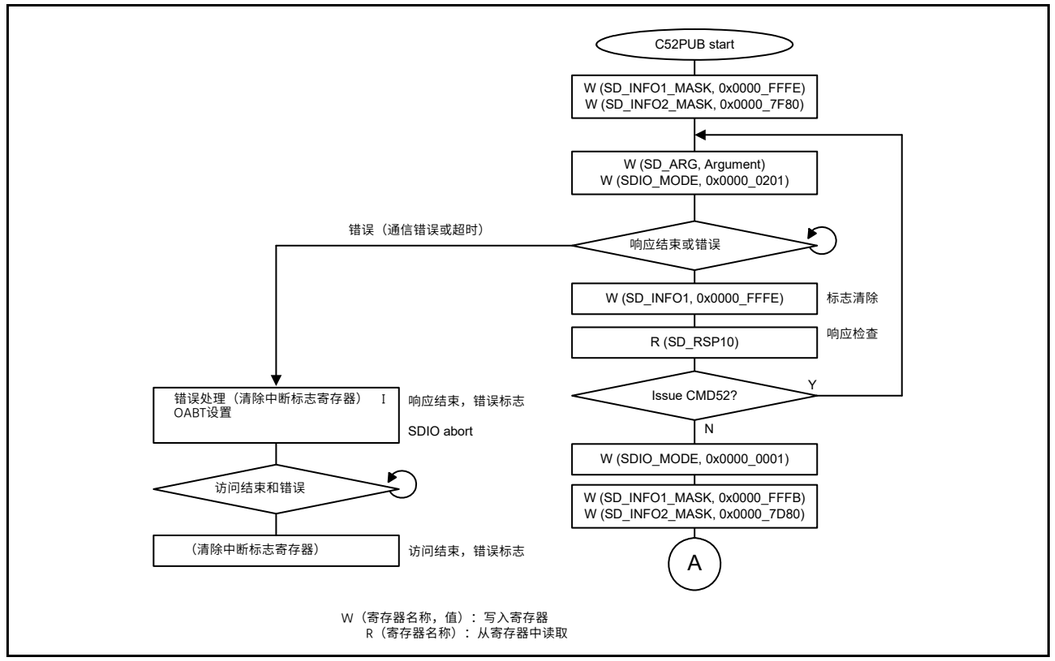


Figure 43.22 在CMD53多块写入期间发出CMD52（SDIO无中止）时的流程

43.3.14 DMA Transfer (SD/MMC)

43.3.14.1 SD_BUF DMA transfer

图43.23显示了发出CMD18多块读取时SD_BUFDMA读取的示例流程。

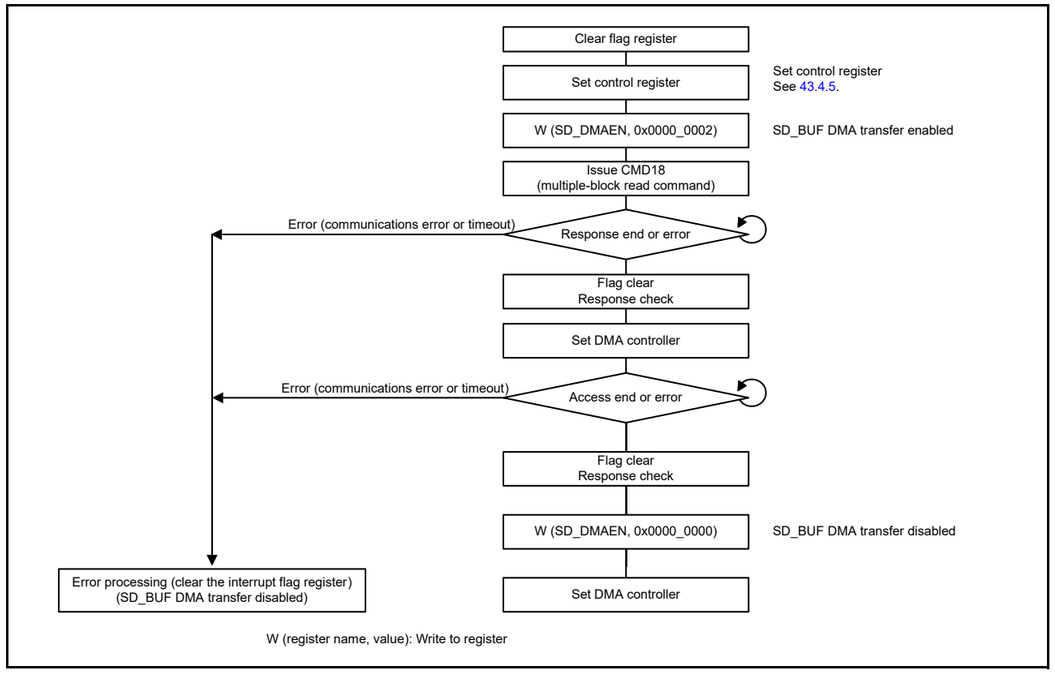


Figure 43.23 Example of SD_BUF_DMA read operation

Figure 43.24 shows an example flow for SD_BUF DMA write when CMD25 multiple block write is issued.

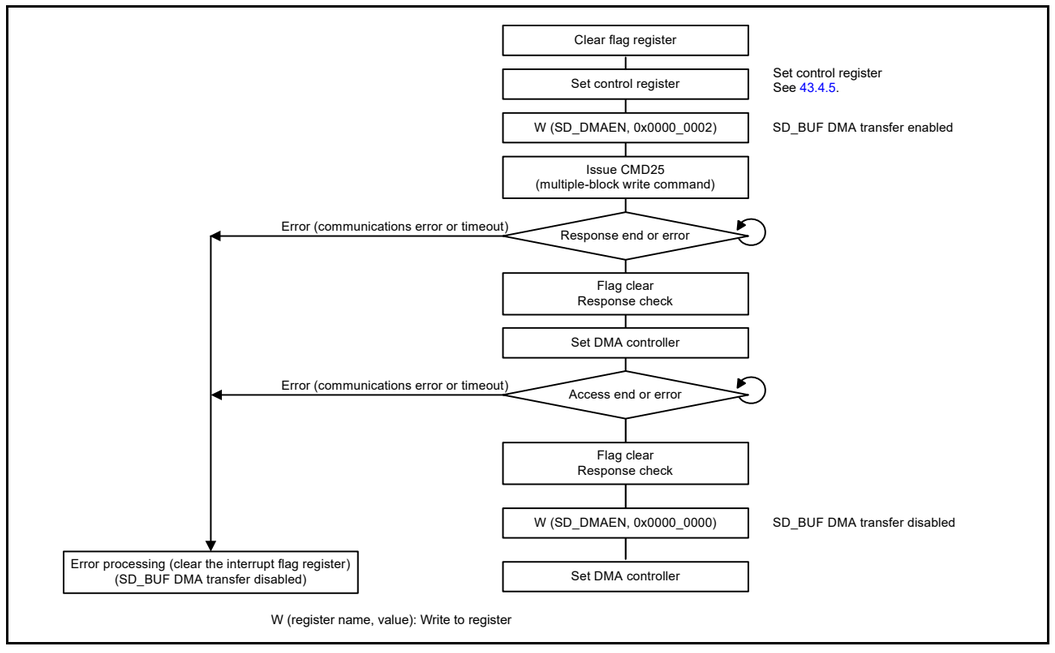


Figure 43.24 Example of SD_BUF_DMA write operation

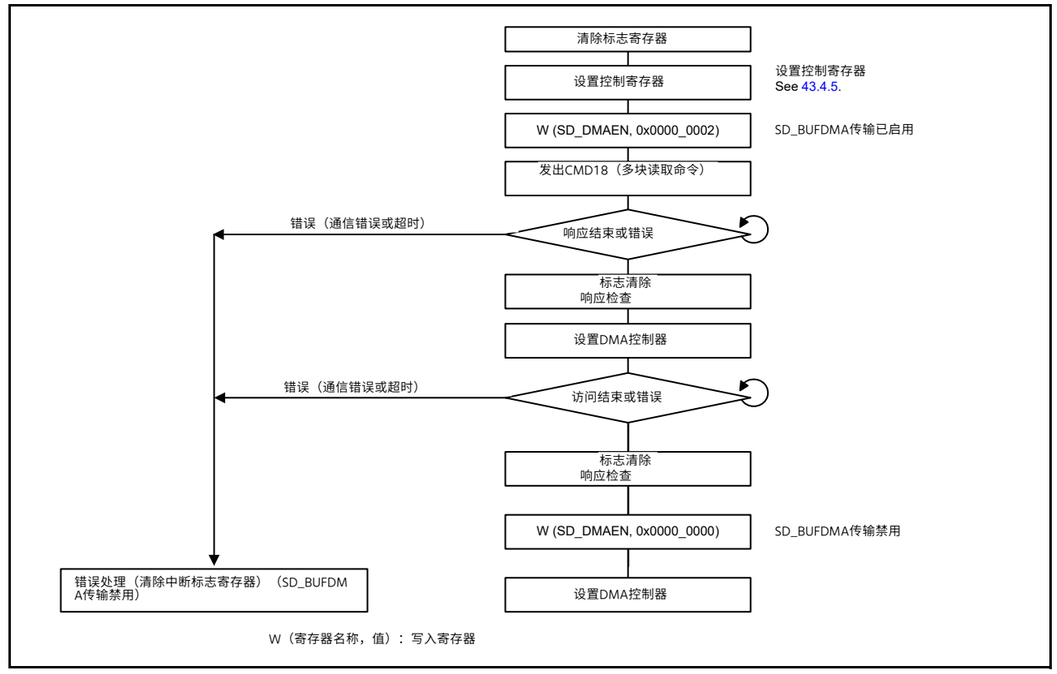


Figure 43.23 SD_BUF_DMA读取操作示例

图43.24显示了发出CMD25多块写入时SD_BUFDMA写入的示例流程。

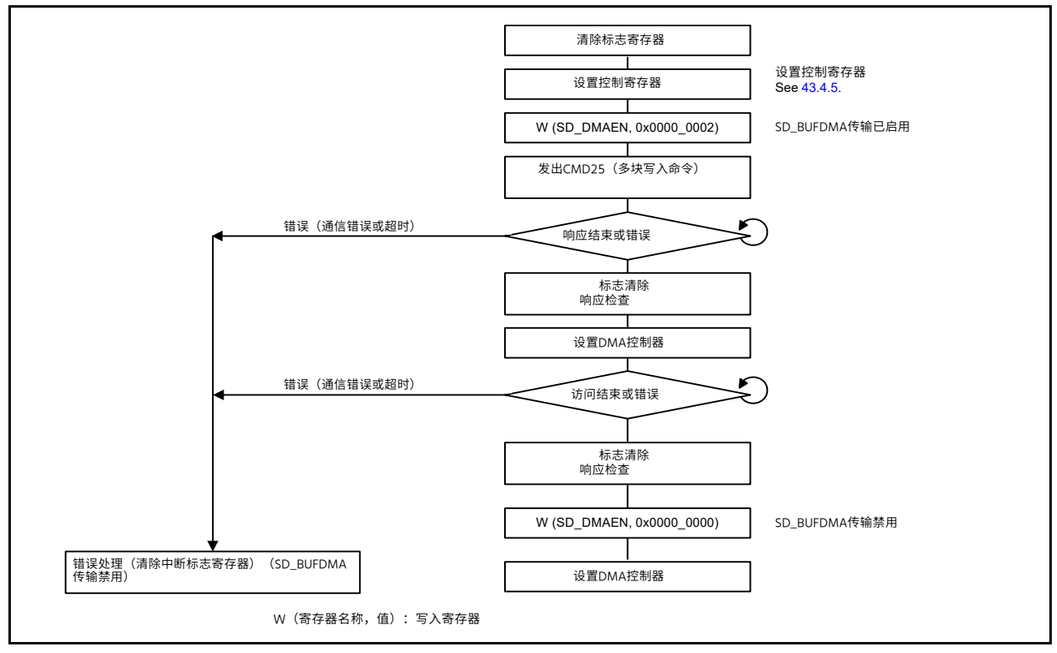


Figure 43.24 SD_BUF_DMA写操作示例

43.3.15 Example of SD_CMD Register Setting

Table 43.8 and Table 43.9 list the SD_CMD register setting.

Table 43.8 Example SD_CMD register settings for SD (1 of 2)

Type	Commamd	Example SD_CMD register setting	Remark
CMD	CMD0	0000_0000h	
	CMD2	0000_0002h	
	CMD3	0000_0003h	
	CMD4	0000_0004h	
	CMD5	0000_0705h or 0000_0005h	
	CMD6	0000_1C06h or 0000_0006h	
	CMD7	0000_0007h	When the card is placed in the deselected state, the response timeout flag sets because there is no response.
	CMD8	0000_0408h or 0000_0008h	
	CMD9	0000_0009h	
	CMD10	0000_000Ah	
	CMD11	0000_040Bh or 0000_000Bh	
	CMD12	0000_000Ch	
	CMD13	0000_000Dh	
	CMD15	0000_000Fh	
	CMD16	0000_0010h	
	CMD17	0000_0011h	
	CMD18	0000_0012h	With automatic CMD12
	CMD20	0000_0514h or 0000_0014h	
	CMD24	0000_0018h	
	CMD25	0000_0019h	With automatic CMD12
	CMD27	0000_001Bh	
	CMD28	0000_001Ch	
	CMD29	0000_001Dh	
	CMD30	0000_001Eh	
	CMD32	0000_0020h	
	CMD33	0000_0021h	
	CMD38	0000_0026h	
	CMD42	0000_002Ah	
	CMD52	0000_0434h or 0000_0034h	
	CMD53	0000_1C35h	Single read
		0000_0C35h	Single write
		0000_7C35h	Multiple read
		0000_6C35h	Multiple write
		0000_0035h	The value on the left can be set for both single and multiple operations. However, the CF39 bit in SD_ARG must be set as follows. Read: 0 Write: 1
	CMD55	0000_0037h	
	CMD56	0000_0038h	

43.3.15 SD_CMD寄存器设置示例

表43.8和表43.9列出了SD_CMD寄存器设置。

Table 43.8 SD的示例SD_CMD寄存器设置（1of2）

Type	Commamd	示例SD_CMD寄存器设置	Remark
CMD	CMD0	0000_0000h	
	CMD2	0000_0002h	
	CMD3	0000_0003h	
	CMD4	0000_0004h	
	CMD5	0000_0705h or 0000_0005h	
	CMD6	0000_1C06h or 0000_0006h	
	CMD7	0000_0007h	当卡被置于取消选择状态时，响应超时标志设置，因为没有响应。
	CMD8	0000_0408h or 0000_0008h	
	CMD9	0000_0009h	
	CMD10	0000_000Ah	
	CMD11	0000_040Bh or 0000_000Bh	
	CMD12	0000_000Ch	
	CMD13	0000_000Dh	
	CMD15	0000_000Fh	
	CMD16	0000_0010h	
	CMD17	0000_0011h	
	CMD18	0000_0012h	带自动CMD12
	CMD20	0000_0514h or 0000_0014h	
	CMD24	0000_0018h	
	CMD25	0000_0019h	带自动CMD12
	CMD27	0000_001Bh	
	CMD28	0000_001Ch	
	CMD29	0000_001Dh	
	CMD30	0000_001Eh	
	CMD32	0000_0020h	
	CMD33	0000_0021h	
	CMD38	0000_0026h	
	CMD42	0000_002Ah	
	CMD52	0000_0434h or 0000_0034h	
	CMD53	0000_1C35h	单读
		0000_0C35h	单写
		0000_7C35h	多读
		0000_6C35h	多次写入
		0000_0035h	左侧的值可以设置为单个和多个操作。但是，SD_ARG中的CF39位必须如下设置。读：0写：1
	CMD55	0000_0037h	
	CMD56	0000_0038h	

Table 43.8 Example SD_CMD register settings for SD (2 of 2)

Type	Commamd	Example SD_CMD register setting	Remark
ACMD	ACMD6	0000_0046h	
	ACMD13	0000_004Dh	
	ACMD22	0000_0056h	
	ACMD23	0000_0057h	
	ACMD41	0000_0069h	
	ACMD42	0000_006Ah	
	ACMD51	0000_0073h	

Table 43.9 Example SD_CMD register settings for MMC (1 of 2)

Type	Command	Example SD_CMD register setting	Remark
CMD	CMD0	0000_0000h	
	CMD1	0000_0701h	
	CMD2	0000_0002h	
	CMD3	0000_0003h	
	CMD4	0000_0004h	
	CMD5	0000_0505h	
	CMD6	0000_0506h	(with response busy)
		0000_0406h	(without response busy)
	CMD7	0000_0007h	When the card is placed in the deselected state, the response timeout flag sets because there is no response.
	CMD8	0000_1C08h	
	CMD9	0000_0009h	
	CMD10	0000_000Ah	
	CMD12	0000_000Ch	
	CMD13	0000_000Dh	
	CMD14	0000_1C0Eh	Required setting: SD_IFMODE = 0000_0100h (CRC check is invalid)
	CMD15	0000_000Fh	
	CMD16	0000_0010h	
	CMD17	0000_0011h	
	CMD18	0000_7C12h	Pre-defined
	CMD19	0000_0C13h	Required setting: SD_IFMODE = 0000_0100h (CRC check is invalid)
	CMD21	0000_1C15h	DDR mode is inhibited
	CMD23	0000_0017h	
	CMD24	0000_0018h	
	CMD25	0000_6C19h	Pre-defined
	CMD26	0000_0C1Ah	
	CMD27	0000_001Bh	
	CMD28	0000_001Ch	
	CMD29	0000_001Dh	
	CMD30	0000_001Eh	
	CMD31	0000_1C1Fh	

Table 43.8 SD的示例SD_CMD寄存器设置（2个中的2个）

Type	Commamd	示例SD_CMD寄存器设置	Remark
ACMD	ACMD6	0000_0046h	
	ACMD13	0000_004Dh	
	ACMD22	0000_0056h	
	ACMD23	0000_0057h	
	ACMD41	0000_0069h	
	ACMD42	0000_006Ah	
	ACMD51	0000_0073h	

Table 43.9 MMC的示例SD_CMD寄存器设置（1of2）

Type	Command	示例SD_CMD寄存器设置	Remark
CMD	CMD0	0000_0000h	
	CMD1	0000_0701h	
	CMD2	0000_0002h	
	CMD3	0000_0003h	
	CMD4	0000_0004h	
	CMD5	0000_0505h	
	CMD6	0000_0506h	(with response busy)
		0000_0406h	(without response busy)
	CMD7	0000_0007h	当卡被置于取消选择状态时，响应超时标志设置，因为没有响应。
	CMD8	0000_1C08h	
	CMD9	0000_0009h	
	CMD10	0000_000Ah	
	CMD12	0000_000Ch	
	CMD13	0000_000Dh	
	CMD14	0000_1C0Eh	需要设置：SD_IFMODE=0000_0100h（CRC校验无效）
	CMD15	0000_000Fh	
	CMD16	0000_0010h	
	CMD17	0000_0011h	
	CMD18	0000_7C12h	Pre-defined
	CMD19	0000_0C13h	需要设置：SD_IFMODE=0000_0100h（CRC校验无效）
	CMD21	0000_1C15h	DDR模式被禁止
	CMD23	0000_0017h	
	CMD24	0000_0018h	
	CMD25	0000_6C19h	Pre-defined
	CMD26	0000_0C1Ah	
	CMD27	0000_001Bh	
	CMD28	0000_001Ch	
	CMD29	0000_001Dh	
	CMD30	0000_001Eh	
	CMD31	0000_1C1Fh	

Table 43.9 Example SD_CMD register settings for MMC (2 of 2)

Type	Command	Example SD_CMD register setting	Remark
CMD	CMD35	0000_0423h	-
	CMD36	0000_0424h	-
	CMD38	0000_0026h	-
	CMD39	0000_0427h	-
	CMD40	0000_0428h	-
	CMD42	0000_002Ah	-
	CMD49	0000_0C31h	-
	CMD53	0000_7C35h	-
	CMD54	0000_6C36h	-
	CMD55	0000_0037h	-
	CMD56	0000_0038h	-

43.4 Usage Notes

43.4.1 SD_BUF Illegal Write Access (SD/MMC)

When writing data to SD_BUF0 after the single block write or multi block write command is issued, the data of the size specified in SD_SIZE must be written.

If the data exceeds the size specified in SD_SIZE is written, the ERR4 bit in SD_INFO2 is set to 1. In addition, the data written to SD_BUF0 might not be transmitted and the SD_CLK_CTRLEN bit in SD_INFO2 is held at the value of 0. If this occurs, clearing the SDRST bit in SOFT_RST to 0 and then restoring its value to 1 clears the SD_CLK_CTRLEN bit to 1.

However, this does not apply to the single byte or three bytes when the SD_SIZE setting is odd, or to the fraction of bytes when the SD_SIZE setting is even (the 2 bytes that are not in a 4-byte unit), because the portion of dummy data writing is regarded as excess data and ignored.

43.4.2 Block Number Constraint for Multiple Block Read (SD)]

When performing a multiple block read of one or two blocks, depending on the timing with which the SD card response register is read, the response value might not be read properly. To prevent this, do one of the following:

1. When receiving one or two blocks of data, use single block reading.
2. Read the response to CMD18 from SD_RSP54.

43.4.2.1 Mechanism of incorrect reading

Figure 43.25 shows the processing flows of the SDHI (hardware) operation and software operation when a multiple block read is performed on two blocks. As shown in the incorrect operation in Figure 43.25, when an interrupt is generated on reception of the CMD18 response and the timing with which the SD card response register (SD_RSP10) is read by the interrupt is delayed, the data during the CMD12 response reception or the CMD12 response might be read. This problem does not occur for multiple block reads of three or more blocks, because CMD12 is not issued until the block of data is read. The problem also does not occur for multiple block writes, because the CMD25 response is read before the block of data is sent.

Table 43.9 MMC的示例SD_CMD寄存器设置（2个中的2个）

Type	Command	示例SD_CMD寄存器设置	Remark
CMD	CMD35	0000_0423h	-
	CMD36	0000_0424h	-
	CMD38	0000_0026h	-
	CMD39	0000_0427h	-
	CMD40	0000_0428h	-
	CMD42	0000_002Ah	-
	CMD49	0000_0C31h	-
	CMD53	0000_7C35h	-
	CMD54	0000_6C36h	-
	CMD55	0000_0037h	-
	CMD56	0000_0038h	-

43.4 使用说明

43.4.1 SD_BUF非法写访问(SDMMC)

在发出单块写入或多块写入命令后向SD_BUF0写入数据时，必须写入SD_SIZE中指定大小的数据。

如果写入的数据超过SD_SIZE中指定的大小，则SD_INFO2中的ERR4位设置为1。此外，写入SD_BUF0的数据可能不会被传输，并且SD_INFO2中的SD_CLK_CTRLEN位将保持为0。如果这发生时，将SOFT_RST中的SDRST位清除为0，然后将其值恢复为1，将SD_CLK_CTRLEN位清除为1。

但是，这不适用于SD_SIZE设置为奇数时的单个字节或三个字节，或适用于SD_SIZE设置为偶数时的字节部分（不在4字节单元中的2个字节），因为该部分虚拟数据写入的次数被视为多余数据并被忽略。

43.4.2 多块读取（SD）的块号约束]

执行1块或2块的多块读取时，根据读取SD卡响应寄存器的时序，可能无法正确读取响应值。为防止这种情况，请执行以下操作之一：

1. 接收一两块数据时，使用单块读取。
2. 从SD_RSP54读取对CMD18的响应。

43.4.2.1 误读机制

图43.25显示了对两个块执行多块读取时的SDHI（硬件）操作和软件操作的处理流程。如图43.25中的错误操作所示，当接收到CMD18响应时产生中断并且中断读取SD卡响应寄存器（SD_RSP10）的时序延迟时，CMD12响应接收期间的数据或可能会读取CMD12响应。对于三个或更多块的多个块读取不会出现此问题，因为在读取数据块之前不会发出CMD12。多次块写入也不会出现该问题，因为在发送数据块之前读取了CMD25响应。

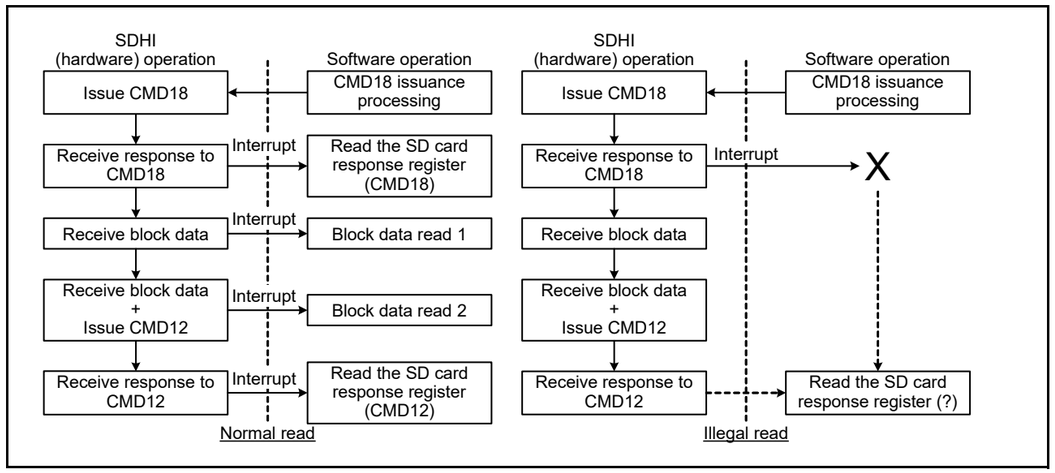


Figure 43.25 Multiple block read operation flow chart (two blocks)

43.4.3 Automatic Control of SD/MMC Clock Output (SD/MMC)

In the SD Card/MMC standard, 74 cycles of SD/MMC clock must be output before initialization of the card. For this reason, use automatic control of SD/MMC clock output after 74 cycles of SD/MMC clock are output. In addition, if automatic control of SD/MMC clock output was in use, SD/MMC clock output is stopped on completion of the sequence for a communications error or timeout. When state transitions within the SD card/MMC are necessary after completion of the sequence, release automatic control of SD/MMC clock output and restart supply of the SD/MMC clock to the SD card/MMC.

43.4.4 Control of the C52PUB Setting for Multiple Block Write (SD)

If the C52PUB bit in SDIO_MODE is set to 1 during a sequence of multiple block write because of CMD53, CMD52 is not issued until SD_BUF becomes empty. For this reason, set the C52PUB bit after suspending writing to SD_BUF by using one of the following procedures, as appropriate:

(a) When DMA transfer is not in use

1. Before setting the C52PUB bit, suspend writing to SD_BUF by making the setting in SD_INFO2 to disable BWE interrupts.
2. Set the C52PUB bit in SDIO_MODE to 1 (so that CMD52 is issued when SD_BUF becomes empty).
3. After the RSPEND interrupt processing in SD_INFO1 because the issuing of CMD52 is completed, restart writing to SD_BUF by making the setting in SD_INFO2 to enable BWE interrupts.

(b) When DMA transfer is in use

1. Every time DMA transfer of the value set in SD_SIZE × n blocks (where n = 1, 2,....) proceeds, suspend writing to SD_BUF by DMA transfer before the C52PUB bit is set.
2. Set the C52PUB bit in SDIO_MODE to 1 (so that CMD52 is issued when SD_BUF becomes empty).
3. After the RSPEND interrupt processing in SD_INFO1 because the issuing of CMD52 is completed, restart writing to SD_BUF by DMA transfer.

43.4.5 Notes on SD_CLK_CTRL Register Settings (SD/MMC)

When the SD_CLK_CTRLEN bit in SD_INFO2 is 0, SD_CLK_CTRL cannot be written to. Before writing to SD_CLK_CTRL, you must check that the SD_CLK_CTRLEN bit in SD_INFO2 is 1.

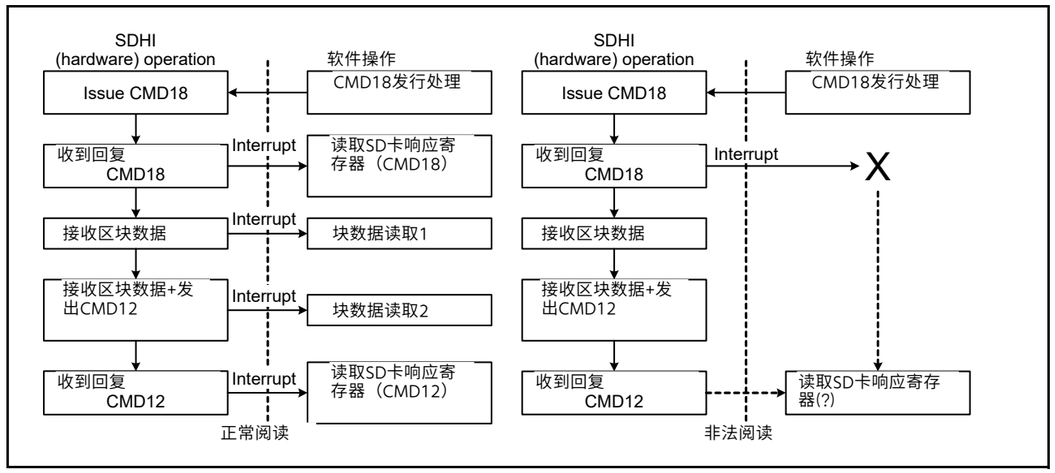


Figure 43.25 多块读取操作流程图（两个块）

43.4.3 SDMMC时钟输出(SDMMC)的自动控制

在SD卡MMC标准中，必须在卡初始化之前输出74个周期的SDMMC时钟。为此，在输出SDMMC时钟的74个周期后使用SDMMC时钟输出的自动控制。此外，如果正在使用SDMMC时钟输出的自动控制，则SDMMC时钟输出会在完成通信错误或超时的序列时停止。当序列完成后需要SD卡MMC内的状态转换时，解除对SDMMC时钟输出的自动控制并重新开始向SD卡MMC提供SDMMC时钟。

43.4.4 控制多块写入(SD)的C52PUB设置

如果SDIO_MODE中的C52PUB位由于CMD53而在多个块写入序列期间设置为1，则在SD_BUF变空之前不会发出CMD52。因此，在暂停写入SD_BUF后，根据需要使用以下过程之一设置C52PUB位：

(a) 不使用DMA传输时

1. 在设置C52PUB位之前，通过在SD_INFO2中进行设置以禁用BWE中断来暂停写入SD_BUF。
2. 将SDIO_MODE中的C52PUB位设置为1（以便在SD_BUF为空时发出CMD52）。
3. 在SD_INFO1中的RSPEND中断处理后，因为CMD52的发出完成，通过在SD_INFO2中进行设置以启用BWE中断，重新开始写入SD_BUF。

(b) 使用DMA传输时

1. 每次DMA传输SD_SIZE n块（其中n=1 2 ....）中设置的值时，暂停写入SD_BUF在C52PUB位被置位之前由DMA传输。
2. 将SDIO_MODE中的C52PUB位设置为1（以便在SD_BUF为空时发出CMD52）。
3. 在SD_INFO1中的RSPEND中断处理后，因为CMD52的发布完成，重新开始通过DMA传输写入SD_BUF。

43.4.5 SD_CLK_CTRL寄存器设置注意事项(SDMMC)

当SD_INFO2中的SD_CLK_CTRLEN位为0时，无法写入SD_CLK_CTRL。在写信之前SD_CLK_CTRL，必须检查SD_INFO2中的SD_CLK_CTRLEN位是否为1。

43.4.6 Specification Limitations

1. The Suspend/Resume operation of the SDIO is not supported.
2. The SPI bus is not supported. (SD/MMC)
3. The shared bus and 8-bit SD bus of the embedded SDIO are not supported.
4. Stream transfer of MMC is not supported.
5. High Priority Interrupt (HPI) of MMC is not supported.
6. Boot Operation/Alternative Boot Operation of MMC is not supported.
7. Open-ended multiple block transfer of MMC is not supported.

43.4.7 STP Bit Setting during Multiple Block Read (SD/MMC)

During execution of multiple block read with automatic CMD12 execution by setting the SEC bit in SD_STOP to 1, even if the STP bit in SD_STOP is set to 1 to forcibly stop the execution, the command sequence might not stop depending on the timing of setting the STP bit.

To avoid this, when setting the STP bit in SD_STOP to 1 during multiple block transfer, clear the SEC bit in SD_STOP to 0 at the same time. (Even when the SD_CLK_CTRLEN bit in SD_INFO2 is 0, change the SEC bit from 1 to 0.)

When the command sequence does not stop because the SEC bit was not cleared to 0, the command sequence can be stopped by clearing the SDRST bit in SOFT_RST to 0.

When forcibly terminating the CMD53 multiple block transfer through the IOABT bit in SDIO_MODE, you must leave the SEC bit in SD_STOP as 1.

43.4.8 Register Setting Notes

1. All registers in section 43.2, Register Descriptions are accessed in 32-bit access-only.
2. When setting registers, set them after the I/O Port Register setting.

43.4.6 规格限制

1. 不支持SDIO的SuspendResume操作。
2. 不支持SPI总线。(标清MMC)
3. 不支持嵌入式SDIO的共享总线和8位SD总线。
4. 不支持MMC的流传输。
5. 不支持MMC的高优先级中断(HPI)。
6. 不支持MMC的引导操作替代引导操作。
7. 不支持MMC的开放式多块传输。

43.4.7 多块读取(SDMMC)期间的STP位设置

在通过将SD_STOP中的SEC位设置为1来执行多个块读取并自动执行CMD12期间，即使将SD_STOP中的STP位设置为1以强制停止执行，命令序列也可能不会停止，具体取决于设置STP位。

为避免这种情况，在多块传输期间将SD_STOP中的STP位设置为1时，同时将SD_STOP中的SEC位清除为0。（即使SD_INFO2中的SD_CLK_CTRLEN位为0，也将SEC位从1更改为0。）

当由于SEC位未清0而导致命令序列未停止时，可通过将SOFT_RST中的SDRST位清0来停止命令序列。

通过SDIO_MODE中的IOABT位强制终止CMD53多块传输时，必须将SD_STOP中的SEC位保留为1。

43.4.8 注册设置注意事项

1. 第43.2节，寄存器描述中的所有寄存器都只能以32位访问方式访问。
2. 设置寄存器时，请在设置IO端口寄存器之后设置。

44. Parallel Data Capture Unit (PDC)

44.1 Overview

The MCU provides one Parallel Data Capture Unit (PDC). The PDC communicates with external I/O devices, including image sensors, and transfers parallel data such as an image output from the external I/O device through the DTC or DMAC to the on-chip SRAM and external address spaces (the CS and SDRAM areas). Table 44.1 lists the PDC specifications, Figure 44.1 shows a block diagram, and Table 44.2 lists the I/O pins.

Table 44.1 PDC specifications

Parameter	Specifications
Capture range	Any amount of parallel data within the following ranges in the vertical and horizontal directions: • Vertical direction: 1 to 4095 lines • Horizontal direction: 4 to 4095 bytes
Parallel transfer clock (PIXCLK)	Operating frequency: 1 to 27 MHz*1
Interrupt sources	• Receive data ready • Frame end • Overrun • Underrun • Error in the setting for the number of lines • Error in setting for the number of bytes per line
Startup of DTC or DMAC	Frame end and receive data ready interrupts can start DTC or DMAC
Parallel transfer clock output (PCKO)	• Operating frequency: 1 to 30 MHz*2 • Clock source: Peripheral module clock B (PCLKB) • Frequency division ratio: Selectable from 2, 4, 6, 8, 10, 12, 14, and 16.
Other functions	• PDC reset function • Selectable active polarity for VSYNC and HSYNC signals • Monitoring of VSYNC and HSYNC signals • Endian order selectable
Module-stop function	Module-stop state can be set to reduce power consumption
Internal bus interface	Internal peripheral bus 5

Note 1. Set the frequency of the parallel data transfer clock (PIXCLK) to a value less than that of 0.6 × PCLKB (peripheral module clock).
Note 2. The operating frequency is 30 MHz when peripheral module clock B (PCLKB) is 60 MHz and the frequency division ratio is 2.

44. 并行数据采集单元(PDC)

44.1 Overview

MCU提供一个并行数据采集单元(PDC)。PDC与外部IO设备（包括图像传感器）通信，并通过DTC或DMAC将并行数据（例如从外部IO设备输出的图像）传输到片上SRAM和外部地址空间（CS和SDRAM区域）。表44.1列出了PDC规格，图44.1显示了框图，表44.2列出了IO引脚。

Table 44.1 PDC specifications

Parameter	Specifications
捕获范围	垂直和水平方向上以下范围内的任意数量的并行数据： 垂直方向：1到4095行 水平方向：4到4095字节
并行传输时钟(PIXCLK)	工作频率：1至27MHz*1
中断源	接收数据就绪 帧结束 溢出 欠载 行数设置错误 每行字节数设置错误
DTC或DMAC的启动	帧结束和接收数据就绪中断可以启动DTC或DMAC
并行传输时钟输出(PCKO)	工作频率：1至30MHz*2 时钟源：外围模块时钟B(PCLKB) 分频比：可从2、4、6、8、10、12、14和16中选择。
其他功能	PDC复位功能 可选择VSYNC和HSYNC信号的有效极性 监控VSYNC和HSYNC信号 Endian顺序可选
Module-stop function	可设置模块停止状态以降低功耗
内部总线接口	内部外围总线5

Note 1. 将并行数据传输时钟(PIXCLK)的频率设置为小于0.6×PCLKB（外围模块时钟）的值。
Note 2. 当外围模块时钟B（PCLKB）为60MHz，分频比为2时，工作频率为30MHz。

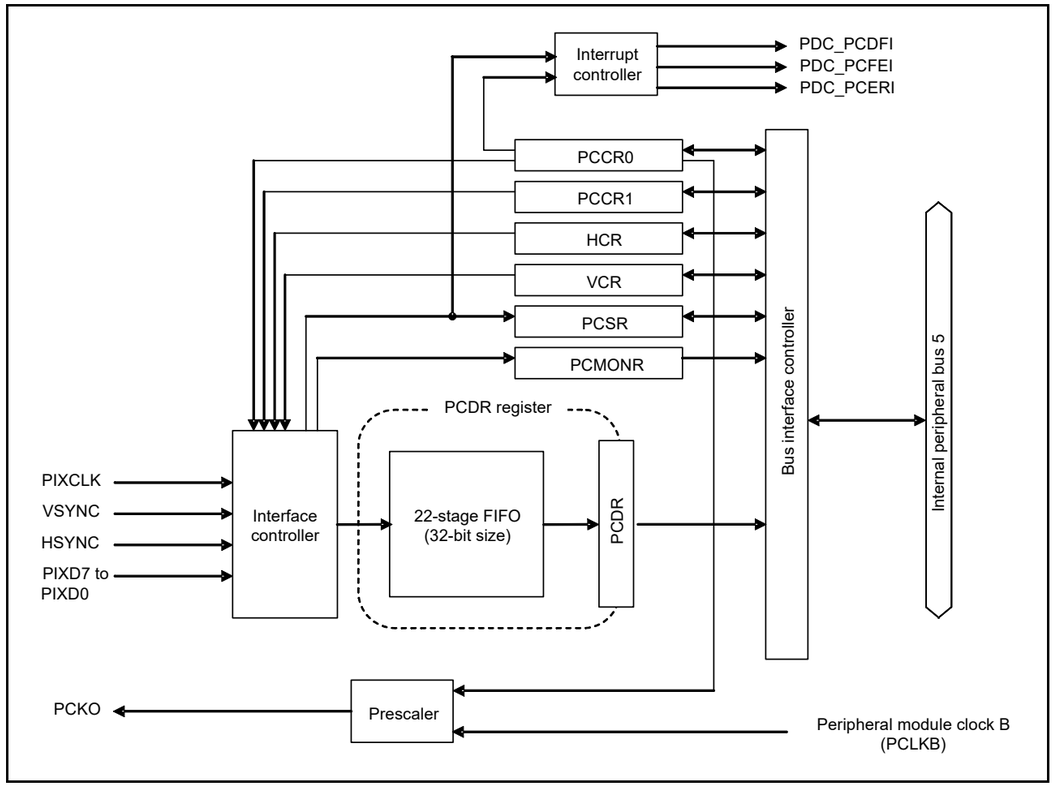


Figure 44.1 PDC block diagram

Table 44.2 PDC I/O pins

Pin name	I/O	Description
PIXCLK	Input	Parallel transfer clock
VSYNC	Input	Vertical synchronization signal
HSYNC	Input	Horizontal synchronization signal
PIXD7 to PIXD0	Input	8-bit data
PCKO	Output	Output for the parallel transfer clock

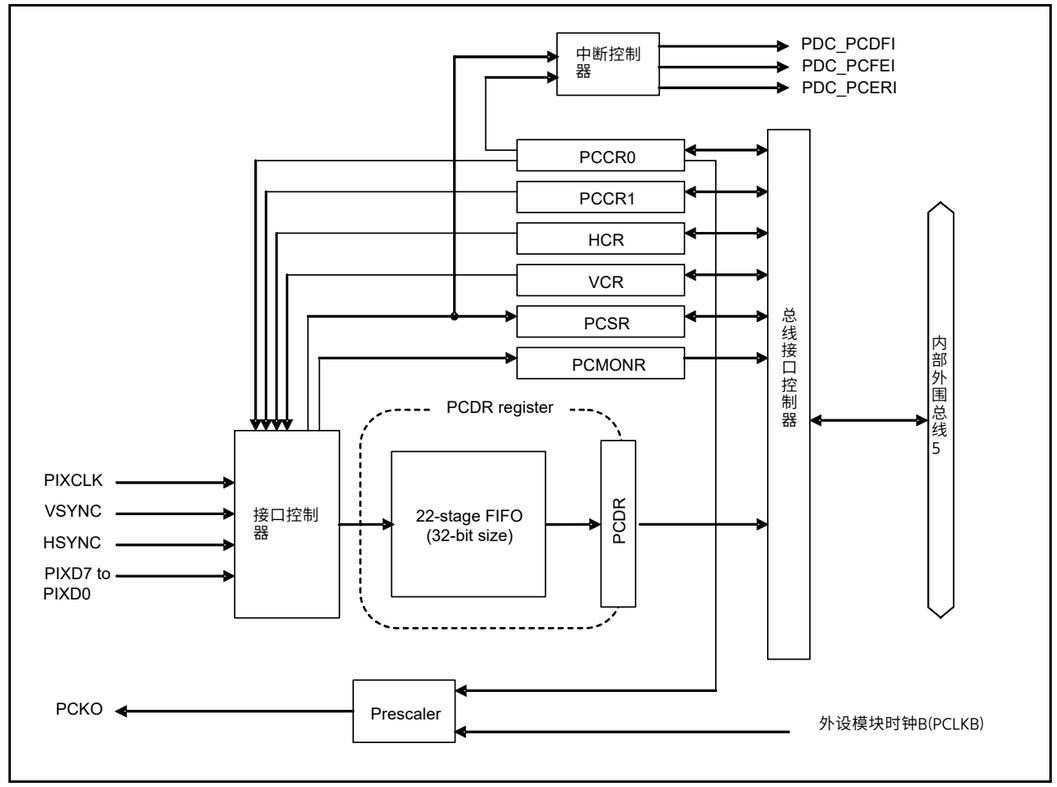


Figure 44.1 配电柜框图

Table 44.2 PDC I/O pins

引脚名称	I/O	Description
PIXCLK	Input	并行传输时钟
VSYNC	Input	垂直同步信号
HSYNC	Input	水平同步信号
PIXD7 to PIXD0	Input	8-bit data
PCKO	Output	并行传输时钟的输出

44.2 Register Descriptions

44.2.1 PDC Control Register 0 (PCCR0)

Address(es): PDC.PCCR0 4009 4000h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	EDS	PCKDIV[2:0]			PCKOE	HERIE	VERIE	UDRIE	OVIE	FEIE	DFIE	PRST	HPS	VPS	PCKE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	PCKE	PIXCLK Input Enable	0: Disable PIXCLK input 1: Enable PIXCLK input.	R/W
b1	VPS	VSYNC Signal Polarity Select	0: Set VSYNC signal to active high 1: Set VSYNC signal to active low.	R/W
b2	HPS	HSYNC Signal Polarity Select	0: Set HSYNC signal to active high 1: Set HSYNC signal to active low.	R/W
b3	PRST	PDC Reset	0: Do not apply PDC reset 1: Reset PDC.	R/(W) *1
b4	DFIE	Receive Data Ready Interrupt Enable	0: Disable receive data ready interrupt requests 1: Enable receive data ready interrupt requests.	R/W
b5	FEIE	Frame End Interrupt Enable	0: Disable frame end interrupt requests 1: Enable frame end interrupt requests.	R/W
b6	OVIE	Overrun Interrupt Enable	0: Disable overrun interrupt requests 1: Enable overrun interrupt requests.	R/W
b7	UDRIE	Underrun Interrupt Enable	0: Disable underrun interrupt requests 1: Enable underrun interrupt requests.	R/W
b8	VERIE	Vertical Line Number Setting Error Interrupt Enable	0: Disable vertical line number setting error interrupt requests 1: Enable vertical line number setting error interrupt requests.	R/W
b9	HERIE	Horizontal Byte Number Setting Error Interrupt Enable	0: Disable horizontal byte number setting error interrupt requests 1: Enable horizontal byte number setting error interrupt requests.	R/W
b10	PCKOE	PCKO Output Enable	0: Disable PCKO output (fix to high level) 1: Enable PCKO output.	R/W
b13 to b11	PCKDIV[2:0]	PCKO Frequency Division Ratio Select	b13 b11 0 0 0: PCLKB/2 0 0 1: PCLKB/4 0 1 0: PCLKB/6 0 1 1: PCLKB/8 1 0 0: PCLKB/10 1 0 1: PCLKB/12 1 1 0: PCLKB/14 1 1 1: PCLKB/16.	R/W
b14	EDS	Endian Select	0: Little endian 1: Big endian.	R/W
b31 to b15	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Only 1 can be written to this bit.

44.2 注册说明

44.2.1 PDC控制寄存器0(PCCR0)

Address(es): PDC.PCCR0 4009 4000h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	EDS	PCKDIV[2:0]			PCKOE	HERIE	VERIE	UDRIE	OVIE	FEIE	DFIE	PRST	HPS	VPS	PCKE
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	PCKE	PIXCLK输入使能	0：禁用PIXCLK输入1： 启用PIXCLK输入。	R/W
b1	VPS	VSYNC信号极性选择	0：将VSYNC信号设置为高电平有效1： 将VSYNC信号设置为低电平有效。	R/W
b2	HPS	HSYNC信号极性选择	0：将HSYNC信号设置为高电平有效1： 将HSYNC信号设置为低电平有效。	R/W
b3	PRST	PDC Reset	0：不应用PDC复位1：复 位PDC。	R/(W) *1
b4	DFIE	接收数据就绪中断使能	0：禁止接收数据就绪中断请求1：使能接收数 据就绪中断请求。	R/W
b5	FEIE	帧结束中断使能	0：禁止帧结束中断请求1：使能帧结 束中断请求。	R/W
b6	OVIE	溢出中断使能	0：禁止溢出中断请求1：使能溢出中 断请求。	R/W
b7	UDRIE	欠载中断使能	0：禁止欠载中断请求1：启用欠载中 断请求。	R/W
b8	VERIE	垂直行号设置错误中断 Enable	0：禁用垂直行号设置错误中断请求1：启用垂直行 号设置错误中断请求。	R/W
b9	HERIE	水平字节数设置错误 中断使能	0：禁用水平字节数设置错误中断请求1：启用 水平字节数设置错误中断请求。	R/W
b10	PCKOE	PCKO输出使能	0：禁用PCKO输出（固定为高电平）1： 启用PCKO输出。	R/W
b13 to b11	PCKDIV[2:0]	PCKO分频比选择	b13 b11 0 0 0: PCLKB/2 0 0 1: PCLKB/4 0 1 0: PCLKB/6 0 1 1: PCLKB/8 1 0 0: PCLKB/10 1 0 1: PCLKB/12 1 1 0: PCLKB/14 1 1 1: PCLKB/16.	R/W
b14	EDS	Endian Select	0：小端1：大 端。	R/W
b31 to b15	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 该位只能写入1。

Only set the PCCR0 register while the PCE bit in the PCCR1 register is 0.

PCKE bit (PIXCLK Input Enable)

The PCKE bit enables or disables input through the PIXCLK pin. Set this bit to 1 before enabling reception. After enabling input through the PIXCLK pin, use the PRST bit to initialize the PDC.

Disable reception operations before setting this bit to 0.

VPS bit (VSYNC Signal Polarity Select)

The VPS bit selects the active polarity of the VSYNC signal.

HPS bit (HSYNC Signal Polarity Select)

The HPS bit selects the active polarity of the HSYNC signal.

PRST bit (PDC Reset)

The PRST bit initializes the internal status of the PDC and the PDC registers targeted by reset. See section 44.3.11, Reset State, for the target registers. Set the PCKE bit to 1 before resetting the PDC.

When 1 is written to the PRST bit, initialization starts in synchronization with the PIXCLK. After initialization completes, the PRST bit clears to 0. After a PDC reset, ensure that the PIXCLK pin has an input signal. Also, after 1 is written to the PRST bit, do not proceed to the next step until verifying that the bit has returned to 0.

For consecutive PDC resets, wait for at least 1 PIXCLK cycle after verifying that the PRST bit has returned to 0.

DFIE bit (Receive Data Ready Interrupt Enable)

The DFIE bit enables or disables the generation of receive data ready interrupt requests.

FEIE bit (Frame End Interrupt Enable)

The FEIE bit enables or disables the generation of frame end interrupt requests.

OVIE bit (Overrun Interrupt Enable)

The OVIE bit enables or disables the generation of overrun interrupt requests.

UDRIE bit (Underrun Interrupt Enable)

The UDRIE bit enables or disables the generation of underrun interrupt requests.

VERIE bit (Vertical Line Number Setting Error Interrupt Enable)

The VERIE bit enables or disables the generation of vertical line number setting error interrupt requests.

HERIE bit (Horizontal Byte Number Setting Error Interrupt Enable)

The HERIE bit enables or disables the generation of horizontal byte number setting error interrupt requests.

PCKOE bit (PCKO Output Enable)

The PCKOE bit enables or disables an output from PCKO. When the PCKOE bit is cleared to 0 during low output of PCKO, it might cause high output on clearing, resulting in corruption of the duty cycle.

PCKDIV[2:0] bits (PCKO Frequency Division Ratio Select)

The PCKDIV[2:0] bits select the frequency division ratio of PCKO. The PCKO output is a clock signal derived by dividing the PCLKB clock signal by a value from 2 to 16, based on the setting in the PCKDIV[2:0] bits. The PCKO operating frequency, the resulting PCLKB division, must fall within the range from 1 to 30 MHz.

EDS bit (Endian Select)

The EDS bit selects the endian order for the captured data.

仅当PCCR1寄存器中的PCE位为0时设置PCCR0寄存器。

PCKE位（PIXCLK输入使能）

PCKE位启用或禁用通过PIXCLK引脚的输入。在启用接收之前将该位设置为1。通过PIXCLK引脚使能输入后，使用PRST位初始化PDC。

在将此位设置为0之前禁用接收操作。

VPS位（VSYNC信号极性选择）

VPS位选择VSYNC信号的有效极性。

HPS位（HSYNC信号极性选择）

HPS位选择HSYNC信号的有效极性。

PRST位（PDC复位）

PRST位初始化PDC和复位目标PDC寄存器的内部状态。请参阅第44.3.11节，重置State，用于目标寄存器。在复位PDC之前将PCKE位设置为1。

当PRST位写入1时，初始化与PIXCLK同步开始。初始化完成后，PRST位清零。在PDC复位后，确保PIXCLK引脚有输入信号。此外，在PRST位写入1后，在验证该位已返回0之前不要进行下一步。

对于连续的PDC复位，请在验证PRST位已返回0后等待至少1个PIXCLK周期。

DFIE位（接收数据就绪中断使能）

DFIE位启用或禁用接收数据就绪中断请求的生成。

FEIE位（帧结束中断允许）

FEIE位启用或禁用帧结束中断请求的生成。

OVIE位（溢出中断使能）

OVIE位启用或禁用溢出中断请求的生成。

UDRIE位（欠载中断使能）

UDRIE位启用或禁用欠载中断请求的生成。

VERIE位（垂直行号设置错误中断使能）

VERIE位启用或禁用垂直行号设置错误中断请求的生成。

HERIE位（水平字节数设置错误中断使能）

HERIE位启用或禁用水平字节数设置错误中断请求的生成。

PCKOE位（PCKO输出使能）

PCKOE位启用或禁用PCKO的输出。当PCKOE位在低输出期间被清除为0 PCKO，它可能会导致清除时的高输出，从而导致占空比损坏。

PCKDIV[2:0]位（PCKO分频比选择）

PCKDIV[2:0]位选择PCKO的分频比。PCKO输出是一个时钟信号，根据PCKDIV[2:0]位的设置，将PCLKB时钟信号除以2到16的值。PCKO工作频率，即产生的PCLKB分频，必须在1到30MHz的范围内。

EDS位（字节序选择）

EDS位选择捕获数据的字节序。

44.2.2 PDC Control Register 1 (PCCR1)

Address(es): PDC.PCCR1 4009 4004h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PCE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	PCE	PDC Operation Enable	0: Disable reception operations 1: Enable reception operations.	R/W
b31 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

PCE bit (PDC Operation Enable)

The PCE bit enables or disables reception operations. When the PCE bit is set to 1 during assertion of the VSYNC signal, the PDC starts reception operations from the next valid edge of the VSYNC signal.

Only clear the PCE bit to 0 while reception or continued reception operations are stopped, including for the frame end interrupt. For more on continued reception, see section 44.3.6, Continued Reception Operations at Frame End.

44.2.3 PDC Status Register (PCSR)

Address(es): PDC.PCSR 4009 4008h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	HERF	VERF	UDRF	OVRF	FEF	FEMPF	FBSY
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bit	Symbol	Bit name	Description	R/W
b0	FBSY	Frame Busy Flag	0: Reception operations are stopped 1: Reception operations are ongoing.	R
b1	FEMPF	FIFO Empty Flag	0: FIFO is not empty 1: FIFO is empty.	R
b2	FEF	Frame End Flag	0: No frame end occurred 1: Frame end occurred.	R/(W) *1
b3	OVRF	Overrun Flag	0: No FIFO overrun occurred 1: FIFO overrun occurred.	R/(W) *1
b4	UDRF	Underrun Flag	0: No underrun occurred 1: Underrun occurred.	R/(W) *1
b5	VERF	Vertical Line Number Setting Error Flag	0: No vertical line number setting error occurred 1: Vertical line number setting error occurred.	R/(W) *1
b6	HERF	Horizontal Byte Number Setting Error Flag	0: No horizontal byte number setting error occurred 1: Horizontal byte number setting error occurred.	R/(W) *1

44.2.2 PDC控制寄存器1(PCCR1)

Address(es): PDC.PCCR1 4009 4004h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PCE
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	PCE	PDC操作使能	0：禁用接收操作1：启用接收操作。	R/W
b31 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

PCE位（PDC操作使能）

PCE位启用或禁用接收操作。在VSYNC信号有效期间PCE位设置为1时，PDC从VSYNC信号的下一个有效边沿开始接收操作。

只有在接收或继续接收操作停止时才将PCE位清零，包括帧结束中断。有关继续接收的更多信息，请参阅第44.3.6节，帧结束时的继续接收操作。

44.2.3 PDC状态寄存器(PCSR)

Address(es): PDC.PCSR 4009 4008h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	HERF	VERF	UDRF	OVRF	FEF	FEMPF	FBSY
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bit	Symbol	位名称	Description	R/W
b0	FBSY	帧忙标志	0：接收操作停止1：接收操作正在进行中。	R
b1	FEMPF	FIFO空标志	0：FIFO不为空1：FIFO为空。	R
b2	FEF	帧结束标志	0：未发生帧结束1：发生帧结束。	R/(W) *1
b3	OVRF	溢出标志	0：未发生FIFO溢出1：发生FIFO溢出。	R/(W) *1
b4	UDRF	Underrun Flag	0：未发生欠载1：发生欠载。	R/(W) *1
b5	VERF	垂直行号设置错误标志	0：未发生垂直行数设置错误1：发生垂直行数设置错误。	R/(W) *1
b6	HERF	水平字节数设置错误标志	0：未发生水平字节数设置错误1：发生水平字节数设置错误。	R/(W) *1

Bit	Symbol	Bit name	Description	R/W
b31 to b7	—	Reserved	These bits are read as 0. The write value should be 0.	R

Note 1. Only 0 can be written to these flags, to clear them after they are read as 1.

FBSY flag (Frame Busy Flag)

The FBSY flag indicates the state of PDC operations.

[Setting condition]

- On detection of the valid edge of the VSYNC signal after the enabling of reception operations.

[Clearing conditions]

- On reception of one frame of data in accordance with the settings in the VCR and HCR registers*1
- When an overrun, underrun, vertical line number setting error, or horizontal byte number setting error occurs
- When the PCCR1.PCE bit is 0.

Note 1. This flag is 0 during continued reception operations.

FEMPF flag (FIFO Empty Flag)

The FEMPF flag indicates the state of the FIFO when a vertical line number setting error or a horizontal byte number setting error occurs. It clears to 0 following an overrun and undefined following an underrun.

[Setting conditions]

- On reading of the PCDR register while the FIFO is empty
- On detection of a valid edge of the VSYNC signal
- On PDC reset.

[Clearing condition]

- On storage of the data captured in the FIFO.

FEF flag (Frame End Flag)

The FEF flag indicates the end of a frame.

[Setting condition]

- Reception of one frame of data in accordance with the settings in the VCR and HCR registers.*1

[Clearing conditions]

- On PDC reset
- When 0 is written to the flag after it is read as 1.

Note 1. For continued reception operations, this flag sets to 1 on their completion.

OVRF flag (Overrun Flag)

The OVRF flag indicates the occurrence of an overrun.

[Setting condition]

- When receive data arrives while the FIFO is full.

[Clearing conditions]

- On PDC reset
- When 0 is written to the flag after it is read as 1.

Bit	Symbol	位名称	Description	R/W
b31 to b7	—	Reserved	这些位被读取为0。写入值应为0。	R

Note 1. 这些标志只能写入0，以在读取为1后清除它们。

FBSY标志（帧忙标志）

FBSY标志指示PDC操作的状态。

[Setting condition]

- 在启用接收操作后检测到VSYNC信号的有效边沿。

[Clearing conditions]

- 根据VCR和HCR寄存器中的设置接收一帧数据时*1
- 发生溢出、欠载、垂直行数设置错误或水平字节数设置错误时
- 当PCCR1.PCE位为0时。

注1.在连续接收操作期间该标志为0。

FEMPF标志（FIFO空标志）

FEMPF标志指示发生垂直行数设置错误或水平字节数设置错误时FIFO的状态。它在溢出后清除为0，在下溢后清除为未定义。

[Setting conditions]

- 在FIFO为空时读取PCDR寄存器
- 检测到VSYNC信号的有效边沿
- 在PDC复位时。

[Clearing condition]

- 关于存储在FIFO中捕获的数据。

FEF标志（帧结束标志）

FEF标志指示帧的结束。

[Setting condition]

- 根据VCR和HCR寄存器中的设置接收一帧数据。*1

[Clearing conditions]

- 在PDC复位
- 当标志位读为1后写入0时。

注1.对于连续接收操作，该标志在完成时设置为1。

OVRF标志（溢出标志）

OVRF标志指示发生溢出。

[Setting condition]

- 当FIFO已满时接收数据到达。

[Clearing conditions]

- 在PDC复位
- 当标志位读为1后写入0时。

UDRF flag (Underrun Flag)

The UDRF flag indicates the occurrence of an underrun.

[Setting condition]

- On reading of the PCDR register while the FIFO is empty.

[Clearing conditions]

- On PDC reset
- When 0 is written to the flag after it is read as 1.

VERF flag (Vertical Line Number Setting Error Flag)

The VERF flag indicates an error in the setting for the number of lines.

[Setting condition]

- When the VSYNC signal is negated because fewer lines were captured than the value in the VCR register.

[Clearing conditions]

- On PDC reset
- When 0 is written to the flag after it is read as 1.

HERF flag (Horizontal Byte Number Setting Error Flag)

The HERF flag indicates an error in the number of bytes in a line.

[Setting condition]

- When the HSYNC signal is negated because fewer bytes in a line were captured than the value in the HCR register.

[Clearing conditions]

- On PDC reset
- When 0 is written to the flag after it is read as 1.

44.2.4 PDC Pin Monitor Register (PCMONR)

Address(es): PDC.PCMONR 4009 400Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	HSYNC	VSYNC
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	VSYNC	VSYNC Signal Status Flag	0: VSYNC signal level is low 1: VSYNC signal level is high.	R
b1	HSYNC	HSYNC Signal Status Flag	0: HSYNC signal level is low 1: HSYNC signal level is high.	R
b31 to b2	—	Reserved	These bits are read as 0.	R

VSYNC flag (VSYNC Signal Status Flag)

The VSYNC flag indicates the state of the VSYNC signal.

UDRF flag (Underrun Flag)

UDRF标志指示发生了欠载。

[Setting condition]

- 在FIFO为空时读取PCDR寄存器。

[Clearing conditions]

- 在PDC复位
- 当标志位读为1后写入0时。

VERF标志（垂直行号设置错误标志）

VERF标志表示行数设置错误。

[Setting condition]

- 当VSYNC信号被否定时，因为捕获的行数少于VCR寄存器中的值。

[Clearing conditions]

- 在PDC复位
- 当标志位读为1后写入0时。

HERF标志（水平字节数设置错误标志）

HERF标志表示一行中的字节数有错误。

[Setting condition]

- 当HSYNC信号被否定时，因为一行中捕获的字节数少于HCR寄存器中的值。

[Clearing conditions]

- 在PDC复位
- 当标志位读为1后写入0时。

44.2.4 PDC引脚监控寄存器(PCMONR)

Address(es): PDC.PCMONR 4009 400Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	HSYNC	VSYNC
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	VSYNC	VSYNC信号状态标志	0：VSYNC信号电平低1：VSYNC信号电平高。	R
b1	HSYNC	HSYNC信号状态标志	0：HSYNC信号电平低1：HSYNC信号电平高。	R
b31 to b2	—	Reserved	这些位读为0。	R

VSYNC标志（VSYNC信号状态标志）

VSYNC标志指示VSYNC信号的状态。

HSYNC flag (HSYNC Signal Status Flag)

The HSYNC flag indicates the state of the HSYNC signal.

44.2.5 PDC Receive Data Register (PCDR)

Address(es): PDC.PCDR 4009 4010h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

The PDC includes a 32-bit-wide, 22-stage FIFO for the storage of captured data. The FIFO is mapped to the 4-byte PCDR register and four bytes of data are read from the PCDR register at a time. The receive data ready flag sets for every 32 bytes of received data, and this also results in a receive data ready interrupt if the DFIE bit in the PCCR0 register is set to 1. When a receive data ready interrupt is generated, read the PCDR register eight times. Figure 44.2 shows a schematic view of the PCDR register.

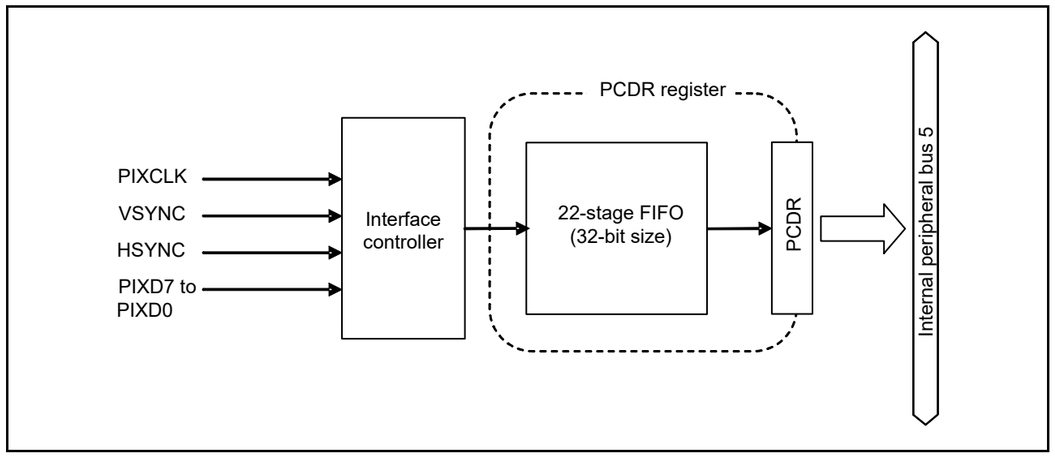


Figure 44.2 Schematic view of PCDR register

For the format of the captured data, either big or little endian can be selected in the EDS bit of the PCCR0 register. Figure 44.3 shows the data arrangements for the endian formats.

HSYNC标志（HSYNC信号状态标志）

HSYNC标志指示HSYNC信号的状态。

44.2.5 PDC接收数据寄存器(PCDR)

Address(es): PDC.PCDR 4009 4010h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

PDC包括一个32位宽、22级FIFO，用于存储捕获的数据。FIFO映射到4字节
一次从PCDR寄存器读取PCDR寄存器和四个字节的数据。每接收32字节数据设置接收数据就绪标志，如果PCCR0寄存器中的DFIE位设置为1，这也会导致接收数据就绪中断。当产生接收数据就绪中断时，读取PCDR寄存器八次。图44.2显示了PCDR寄存器的示意图。

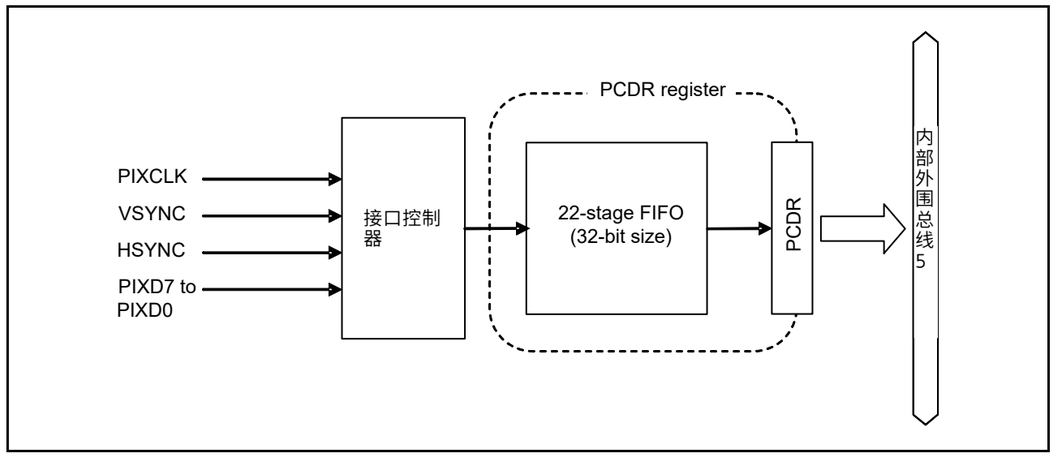


Figure 44.2 PCDR寄存器示意图

对于捕获数据的格式，可以在PCCR0寄存器的EDS位中选择大端或小端。图44.3显示了字节序格式的数据排列。

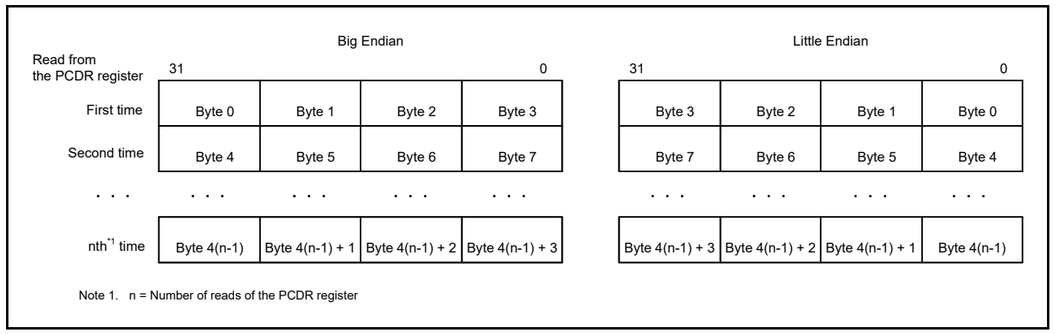


Figure 44.3 Endian formats

44.2.6 Vertical Capture Register (VCR)

Address(es): PDC.VCR 4009 4014h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	VSZ[11:0]											
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	VST[11:0]											

Bit	Symbol	Bit name	Description	R/W
b11 to b0	VST[11:0]	Vertical Capture Start Line Position	These bits specify the number of the line where capture is to start.	R/W
b15 to b12	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b27 to b16	VSZ[11:0]	Vertical Capture Size	These bits specify the number of lines to be captured.	R/W
b31 to b28	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

For the relationship between the VCR register setting and the capture range, see section 44.3.3, VCR and HCR Register Settings and the Capture Range. Only set the VCR register while the PCE bit in the PCCR1 register is 0.

VST[11:0] bits (Vertical Capture Start Line Position)

The VST[11:0] bits specify the number of the line where capture is to start. To set the first line, set these bits to 000h; to set the 4095th line, set them to FFEh. The VST[11:0] setting must be within the range from 000h to FFEh and, in combination with the VSZ[11:0] setting, satisfy the following relationship:

Setting range of the VST[11:0] bits: 1 ≤ VST[11:0] + VSZ[11:0] ≤ FFFh.

VSZ[11:0] bits (Vertical Capture Size)

The VSZ[11:0] bits specify the number of lines to be captured. To set one line, set these bits to 001h; to set 4095 lines, set them to FFFh. The VSZ[11:0] setting must be within the range from 001h to FFFh and, in combination with the VST[11:0] setting, satisfy the following relationship:

Setting range of the VSZ[11:0] bits: 1 ≤ VST[11:0] + VSZ[11:0] ≤ FFFh.

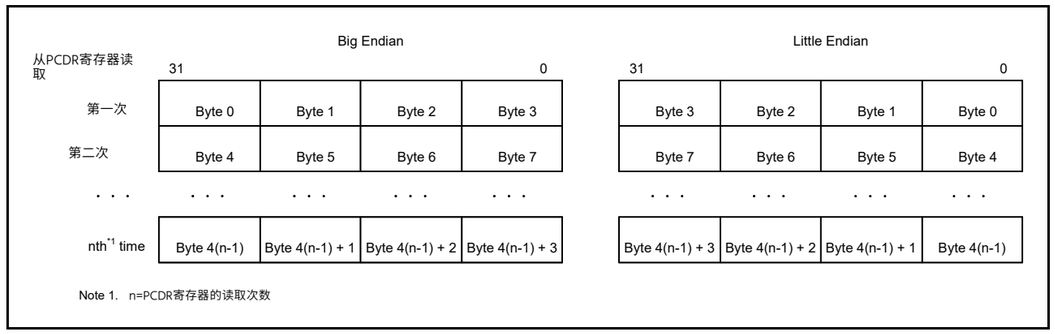


Figure 44.3 Endian formats

44.2.6 垂直捕捉寄存器(VCR)

Address(es): PDC.VCR 4009 4014h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	VSZ[11:0]											
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	VST[11:0]											

Bit	Symbol	位名称	Description	R/W
b11 to b0	VST[11:0]	垂直捕捉起始线位置	这些位指定开始捕获的行号。	R/W
b15 to b12	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b27 to b16	VSZ[11:0]	垂直捕获大小	这些位指定要捕获的行数。	R/W
b31 to b28	—	Reserved	这些位被读取为0。写入值应为0。	R/W

关于VCR寄存器设置和捕捉范围的关系，请参见第44.3.3节，VCR和HCR寄存器设置和捕获范围。仅当PCCR1寄存器中的PCE位为0时设置VCR寄存器。

VST[11:0]位（垂直捕捉起始行位置）

VST[11:0]位指定捕获开始的行号。要设置第一行，请将这些位设置为000h；要设置第4095行，请将它们设置为FFEh。VST[11:0]设置必须在000h到FFEh的范围内，并与VSZ[11:0]设置结合，满足以下关系：

VST[11:0]位的设置范围：1≤VST[11:0]+VSZ[11:0]≤FFFh。

VSZ[11:0]位（垂直捕获大小）

VSZ[11:0]位指定要捕获的行数。要设置一行，请将这些位设置为001h；要设置4095行，请将它们设置为FFFh。VSZ[11:0]设置必须在001h到FFFh的范围内，并与VST[11:0]设置结合，满足以下关系：

VSZ[11:0]位的设置范围：1≤VST[11:0]+VSZ[11:0]≤FFFh。

44.2.7 Horizontal Capture Register (HCR)

Address(es): PDC.HCR 4009 4018h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	HSZ[11:0]											
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	HST[11:0]											
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b11 to b0	HST[11:0]	Horizontal Capture Start Byte Position	These bits specify the horizontal position in bytes where capture is to start.	R/W
b15 to b12	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b27 to b16	HSZ[11:0]	Horizontal Capture Size	These bits specify the number of bytes to be captured horizontally.	R/W
b31 to b28	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

For the relationship between the HCR register setting and the capture range, see section 44.3.3, VCR and HCR Register Settings and the Capture Range. Only set the HCR register while the PCE bit in the PCCR1 register is 0.

HST[11:0] bits (Horizontal Capture Start Byte Position)

The HST[11:0] bits specify the horizontal position in bytes where capture is to start. To set the first byte, set these bits to 000h; to set the 4092th byte, set them to FFBh. The HST[11:0] setting must be within the range from 000h to FFBh and, in combination with the HSZ[11:0] setting, satisfy the following relationship:

Setting range of the HST[11:0] bits: 1 ≤ HST[11:0] + HSZ[11:0] ≤ FFFh.

HSZ[11:0] bits (Horizontal Capture Size)

The HSZ[11:0] bits specify the number of bytes to be captured per line. To set four bytes, set these bits to 004h; to set 4095 bytes, set them to FFFh. The HSZ[11:0] setting must be within the range from 004h to FFFh and, in combination with the HST[11:0] setting, satisfy the following relationship:

Setting range of the HSZ[11:0] bits: 1 ≤ HST[11:0] + HSZ[11:0] ≤ FFFh.

44.3 Operation

44.3.1 Transfer Formats

The PDC supports the four transfer formats shown in Figure 44.4 to Figure 44.7. The format is determined by the settings in the VPS and HPS bits in the PCCR0 register.

44.2.7 水平捕捉寄存器(HCR)

Address(es): PDC.HCR 4009 4018h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	HSZ[11:0]											
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	HST[11:0]											
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b11 to b0	HST[11:0]	水平捕捉起始字节位置	这些位以字节为单位指定开始捕获的水平位置。	R/W
b15 to b12	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b27 to b16	HSZ[11:0]	水平捕捉尺寸	这些位指定要水平捕获的字节数。	R/W
b31 to b28	—	Reserved	这些位被读取为0。写入值应为0。	R/W

关于HCR寄存器设置和捕捉范围的关系，请参见第44.3.3节，VCR和HCR寄存器设置和捕获范围。仅当PCCR1寄存器中的PCE位为0时设置HCR寄存器。

HST[11:0]位（水平捕捉起始字节位置）

HST[11:0]位以字节为单位指定捕获开始的水平位置。要设置第一个字节，请将这些位设置为000h；要设置第4092个字节，请将它们设置为FFBh。HST[11:0]设置必须在000h到FFBh的范围内，并与HSZ[11:0]设置结合，满足以下关系：

HST[11:0]位的设置范围：1≤HST[11:0]+HSZ[11:0]≤FFFh。

HSZ[11:0]位（水平捕获大小）

HSZ[11:0]位指定每行要捕获的字节数。要设置四个字节，请将这些位设置为004h；要设置4095字节，请将它们设置为FFFh。HSZ[11:0]设置必须在004h到FFFh的范围内，并与HST[11:0]设置结合，满足以下关系：

HSZ[11:0]位的设置范围：1≤HST[11:0]+HSZ[11:0]≤FFFh。

44.3 Operation

44.3.1 传输格式

PDC支持图44.4至图44.7所示的四种传输格式。格式由PCCR0寄存器中的VPS和HPS位的设置决定。

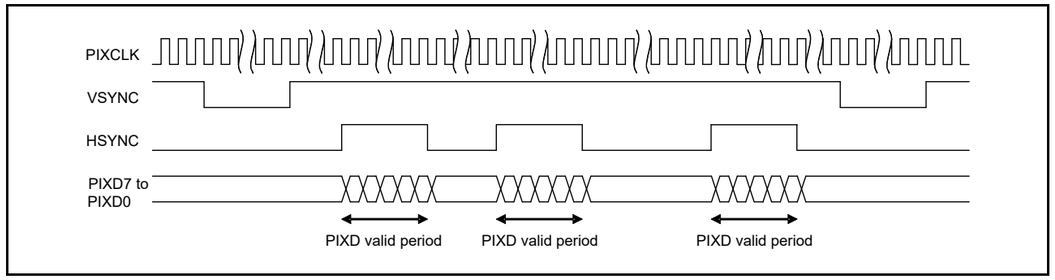


Figure 44.4 PDC transfer format when VPS = 0 and HPS = 0

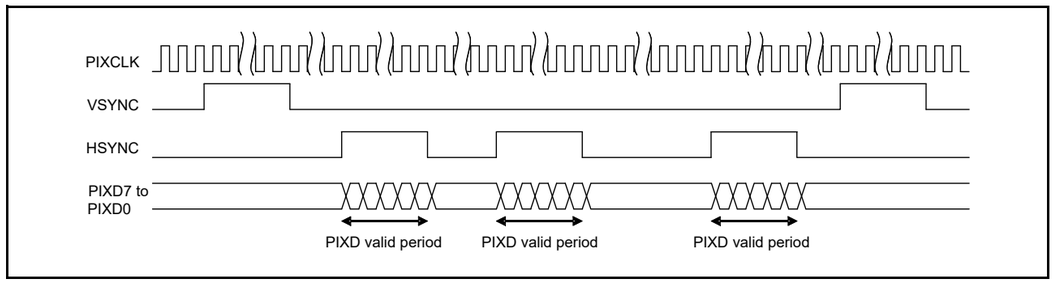


Figure 44.5 PDC transfer format when VPS = 1 and HPS = 0

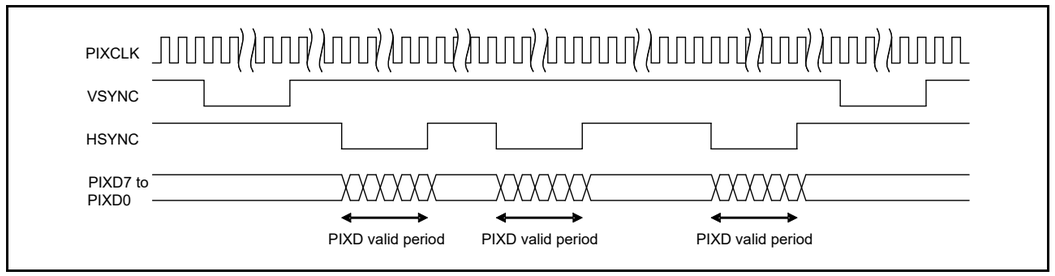


Figure 44.6 PDC transfer format when VPS = 0 and HPS = 1

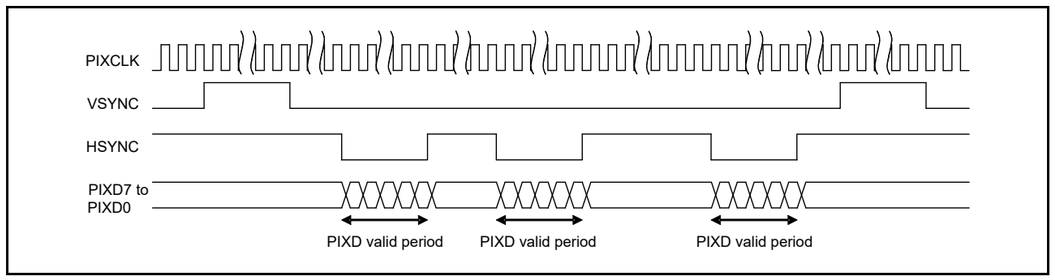


Figure 44.7 PDC transfer format when VPS = 1 and HPS = 1

44.3.2 Transfer Timing

Figure 44.8 and Table 44.3 show the timing of transfers by the PDC.

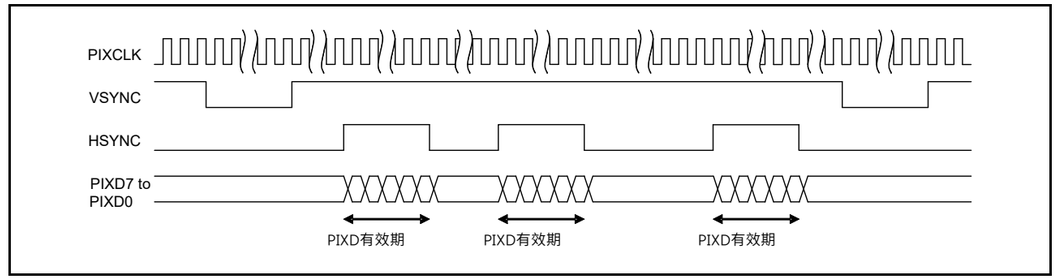


Figure 44.4 VPS=0和HPS=0时的PDC传输格式

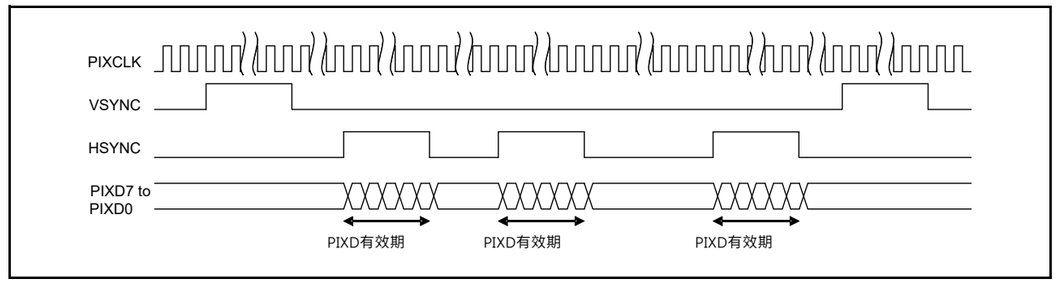


Figure 44.5 VPS=1和HPS=0时的PDC传输格式

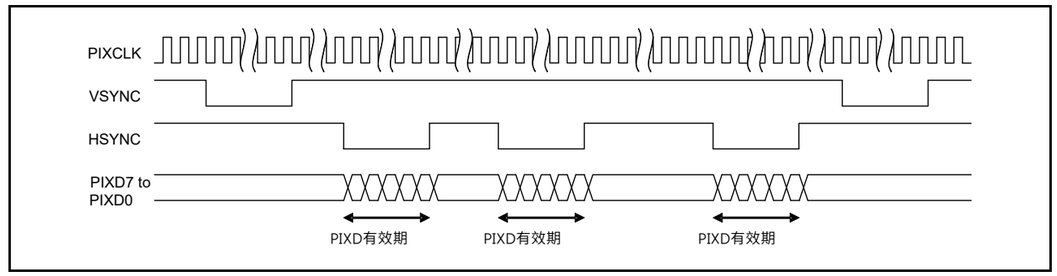


Figure 44.6 VPS=0和HPS=1时的PDC传输格式

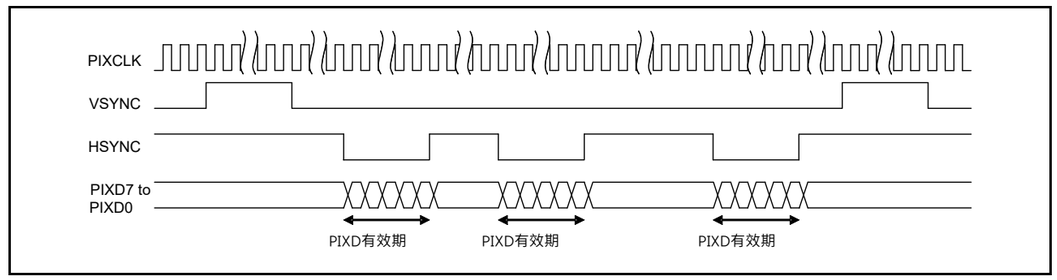


Figure 44.7 VPS=1和HPS=1时的PDC传输格式

44.3.2 传输时间

图44.8和表44.3显示了PDC的传输时间。

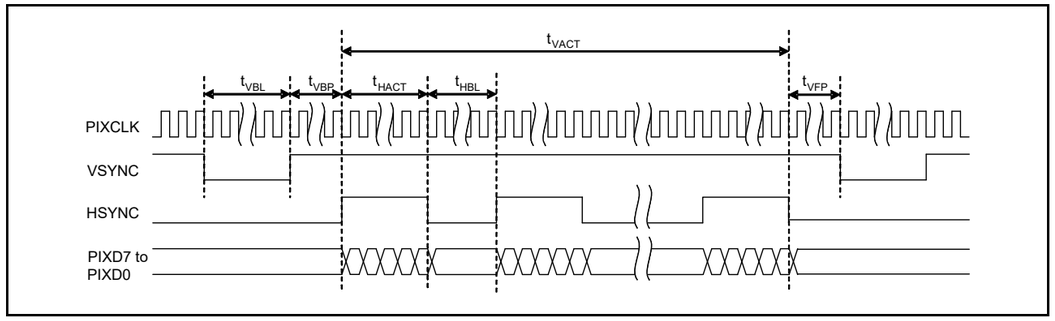


Figure 44.8 PDC transfer timing when VPS = 0 and HPS = 0

Table 44.3 PDC transfer timing when VPS = 0 and HPS = 0

Parameter	Symbol	Min*1	Max	Unit
Vertical blanking period	t_{VBL}	128	-	PIXCLK
Vertical backporch	t_{VBP}	10	-	PIXCLK
Horizontal valid period	t_{HACT}	4	4095	PIXCLK
Horizontal blanking period	t_{HBL}	128	-	PIXCLK
Vertical frontporch	t_{VFP}	10	-	PIXCLK
Vertical valid period	t_{VACT}	1	4095	Line

Note 1. The minimum values are the lowest the PDC is capable of achieving. Operation at these values cannot guarantee the avoidance of overruns, vertical line number setting errors, or horizontal byte number setting errors.

44.3.3 VCR and HCR Register Settings and the Capture Range

Figure 44.9 and Figure 44.10 show the relationship between the settings in the VCR and HCR registers and the capture range.

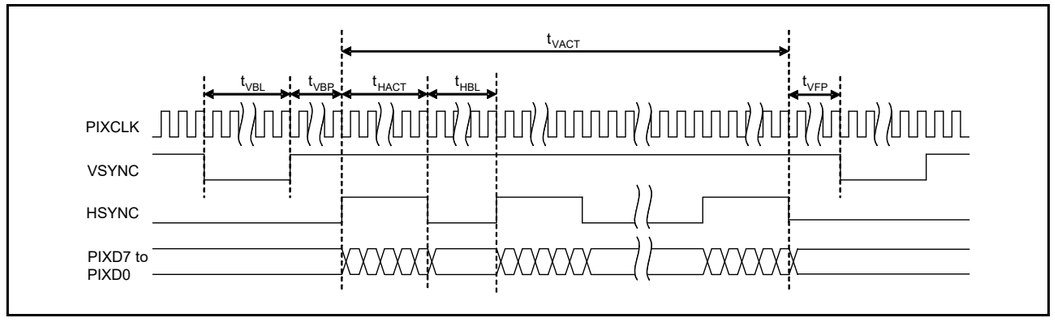


Figure 44.8 VPS=0和HPS=0时的PDC传输时序

Table 44.3 VPS=0和HPS=0时的PDC传输时序

Parameter	Symbol	Min*1	Max	Unit
垂直消隐期	t_{VBL}	128	-	PIXCLK
Vertical backporch	t_{VBP}	10	-	PIXCLK
横向有效期	t_{HACT}	4	4095	PIXCLK
水平消隐期	t_{HBL}	128	-	PIXCLK
Vertical frontporch	t_{VFP}	10	-	PIXCLK
垂直有效期	t_{VACT}	1	4095	Line

Note 1. 最小值是PDC能够达到的最低值。在这些值下操作不能保证避免溢出、垂直行数设置错误或水平字节数设置错误。

44.3.3 VCR和HCR寄存器设置和捕捉范围

图44.9和图44.10显示了VCR和HCR寄存器中的设置与捕获范围之间的关系。

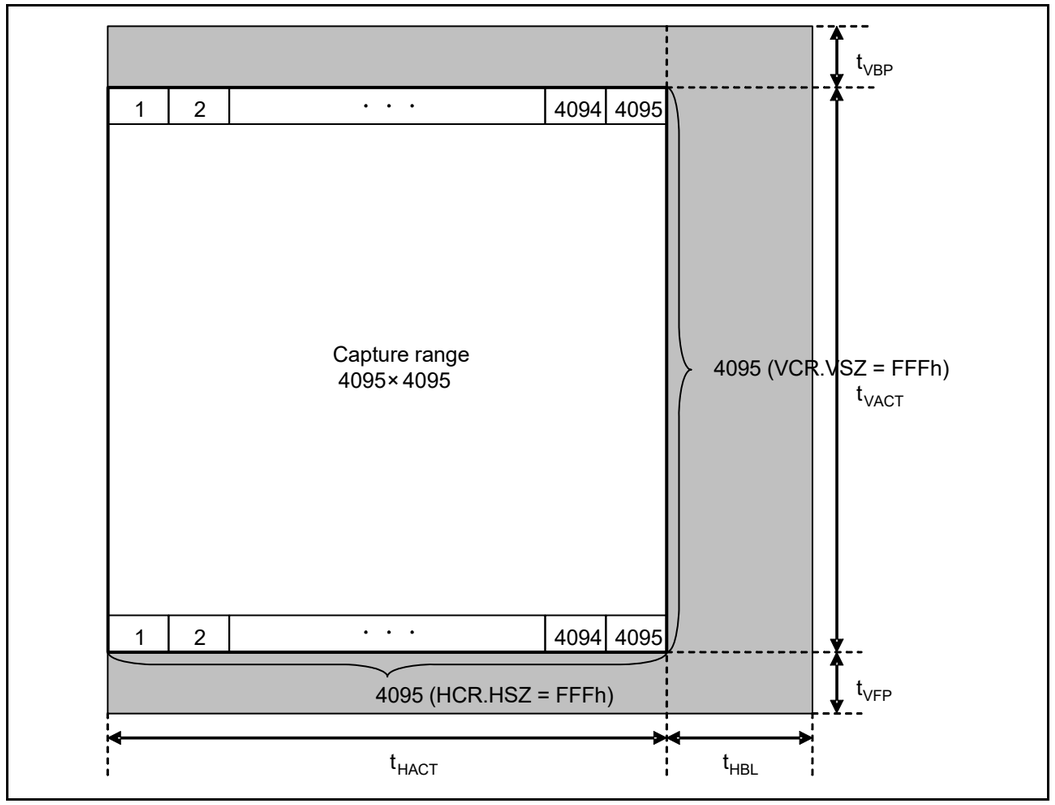


Figure 44.9 Settings in the VCR and HCR registers and the capture range when VCR = 0FFF 0000h and HCR = 0FFF 0000h

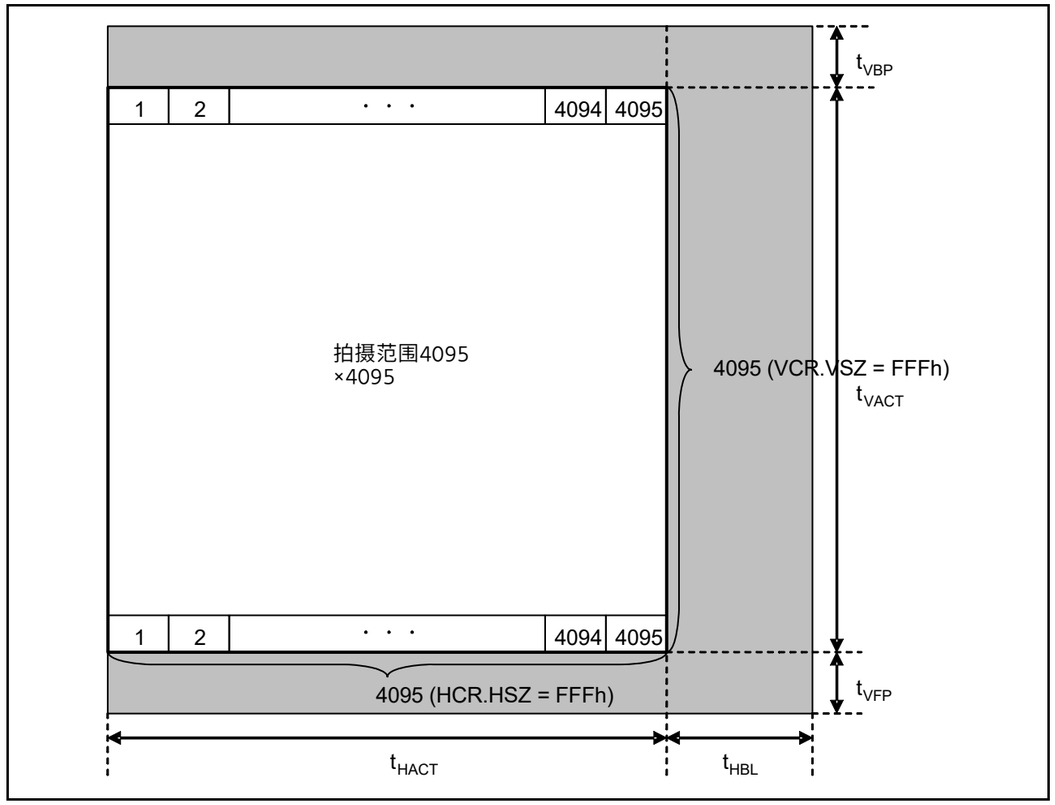


Figure 44.9 VCR和HCR寄存器中的设置以及VCR=0FFF0000h和HCR=0FFF0000h时的捕获范围

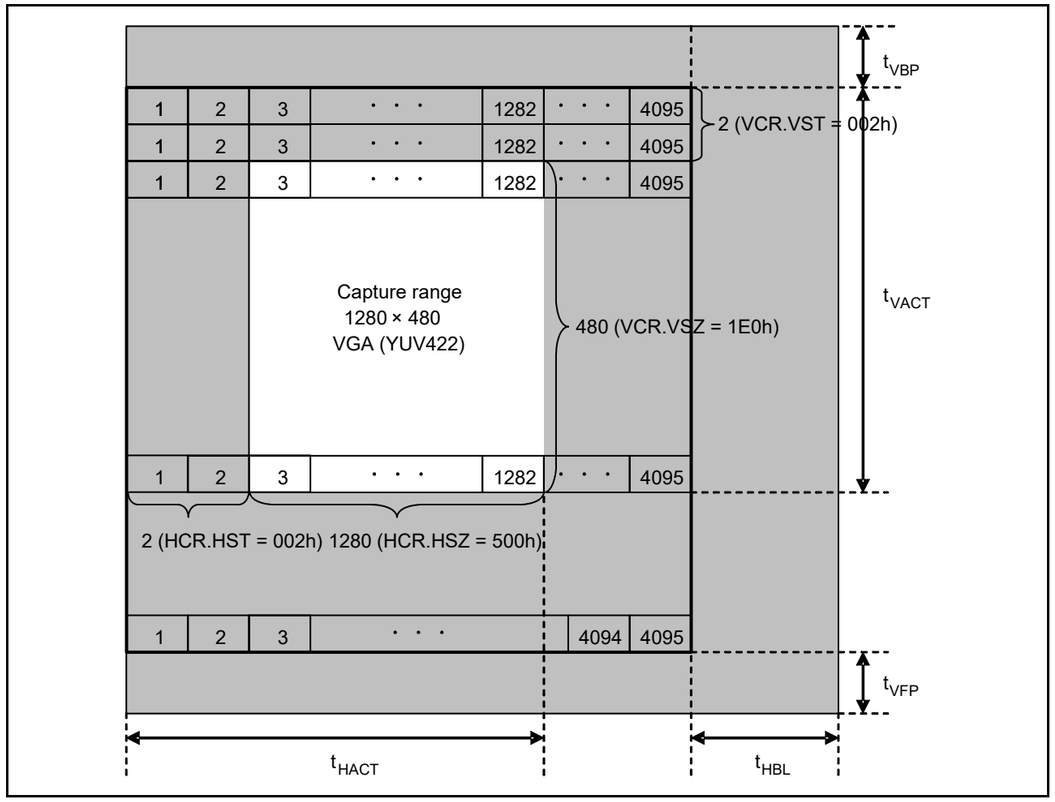


Figure 44.10 Settings in the VCR and HCR registers and the capture range when VCR = 01E0 0002h and HCR = 0500 0002h

44.3.4 Reception Operation

Figure 44.11 shows an example of reception operations when receive data ready interrupts (to start the DTC or DMAC) and frame end interrupts are in use.

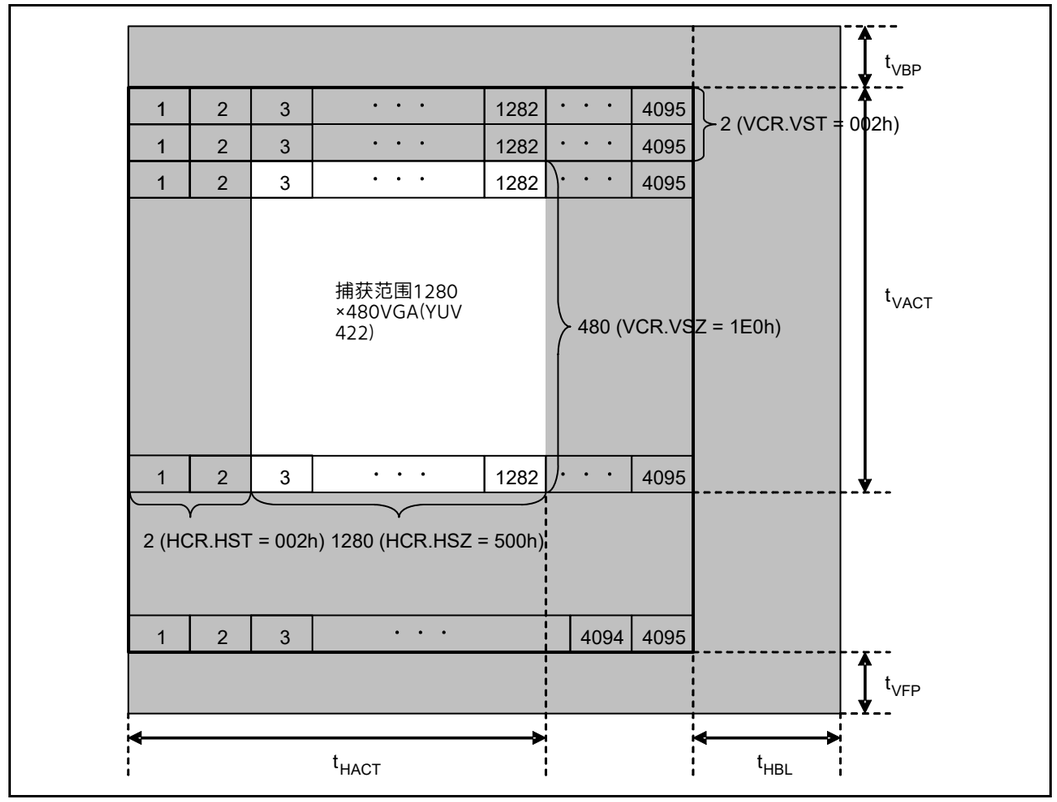


Figure 44.10 VCR和HCR寄存器中的设置以及VCR=01E00002h和HCR=05000002h时的捕获范围

44.3.4 接待操作

图44.11显示了使用接收数据就绪中断（启动DTC或DMAC）和帧结束中断时的接收操作示例。

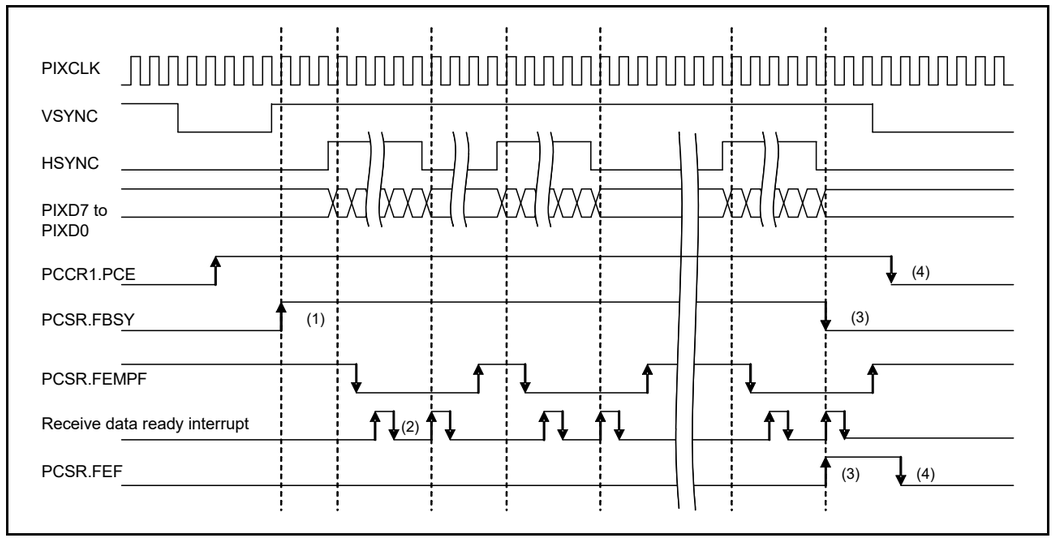


Figure 44.11 Example of reception operations

This section describes the actual operations at the times indicated by (1), (2), (3), and (4) in Figure 44.11.

When a valid edge of the VSYNC signal is detected after the PCE bit in the PCCR1 register is set to 1, the FEMPF flag in the PCSR register sets to 1 and the FIFO is initialized. Concurrently, the FBSY flag in the PCSR register sets to 1 and reception operations start.

When data within the capture range set in the VCR and HCR registers is received, the data is stored in the FIFO. The PDC generates a receive data ready interrupt every time it receives 32 bytes of data, and the interrupt starts transfer of the captured data by the DTC or DMAC to the on-chip SRAM or an external address space. The FIFO is likely to overrun if reading the PCDR register takes more time than reception of the data. Check the OVRF flag in the PCSR register to verify an overrun.

After reception of the last byte of data is complete, the FBSY flag in the PCSR register clears to 0 and the FEF flag in the PCSR register sets to 1 so that a receive data ready interrupt and frame end interrupt are generated.

The FEMPF flag in the PCSR register is polled by the frame end interrupt, after which the program must verify the completion of data transfer by the DTC or DMAC. After the PCE bit in the PCCR1 register is cleared to 0, the FEF flag in the PCSR register also clears to 0, and the reception of one frame of data is complete.

If the FEF flag in the PCSR register sets to 1 before the PCE bit in the PCCR1 register is set to 1, valid edges of the VSYNC signal are not detected and reception operations are not started. Clear the FEF flag in the PCSR register to 0 to start data reception operations.

44.3.5 Operation during Horizontal Blanking Period

If the horizontal blanking period begins but the number of received data bytes has not reached 32 bytes since the previous receive data ready, the count of the received data bytes is retained and carried over to the next valid period. Figure 44.12 shows an example of operation during the horizontal blanking period.

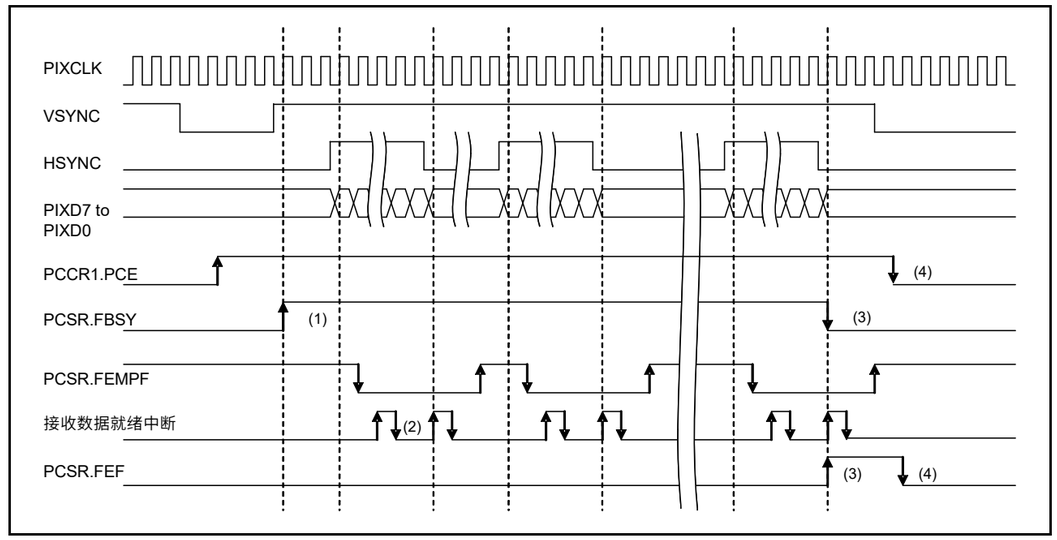


Figure 44.11 接收操作示例

本节介绍图44.11中（1）、（2）、（3）和（4）所示时间的实际操作。

当PCCR1寄存器中的PCE位设置为1后检测到VSYNC信号的有效边沿时，PCSR寄存器中的FEMPF标志设置为1并初始化FIFO。同时，PCSR寄存器中的FBSY标志设置为1，接收操作开始。

当接收到VCR和HCR寄存器中设置的捕获范围内的数据时，数据将存储在FIFO中。这PDC每次接收到32字节数据时产生一个接收数据就绪中断，该中断开始将DTC或DMAC捕获的数据传输到片上SRAM或外部地址空间。如果读取PCDR寄存器的时间比接收数据的时间长，则FIFO可能会溢出。检查PCSR寄存器中的OVRF标志以验证溢出。

接收完最后一个字节的数据后，PCSR寄存器中的FBSY标志清零，FEF标志位在PCSR寄存器中。PCSR寄存器设置为1，以便产生接收数据就绪中断和帧结束中断。

PCSR寄存器中的FEMPF标志由帧结束中断轮询，之后程序必须通过DTC或DMAC验证数据传输是否完成。PCCR1寄存器中的PCE位清0后，PCSR寄存器中的FEF标志位也清0，一帧数据的接收完成。

如果在PCCR1寄存器中的PCE位设置为1之前PCSR寄存器中的FEF标志设置为1，则有效边沿未检测到VSYNC信号且未开始接收操作。将PCSR寄存器中的FEF标志清零，开始数据接收操作。

44.3.5 水平消隐期间的操作

如果水平消隐期开始，但自上次接收数据准备就绪后接收数据字节数未达到32字节，则保留接收数据字节数并结转至下一个有效周期。图44.12显示了水平消隐期间的操作示例。

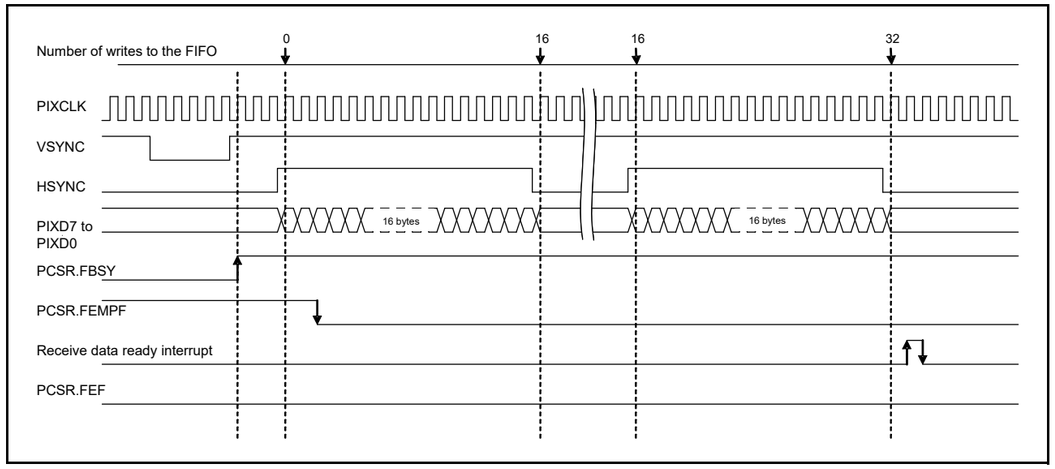


Figure 44.12 Example operation during horizontal blanking period

44.3.6 Continued Reception Operations at Frame End

When the last of the data is received but fewer than 32 bytes of data have been received since the previous receive data ready, the PDC continues to receive data until the number reaches 32, an operation called *continued reception*. When continued reception ends, the PDC generates a receive data ready interrupt and a frame end interrupt. Always input PIXCLK during continued reception. If the data stored in the FIFO is read during this operation, the values are undefined. Figure 44.13 shows an example operation at frame end.

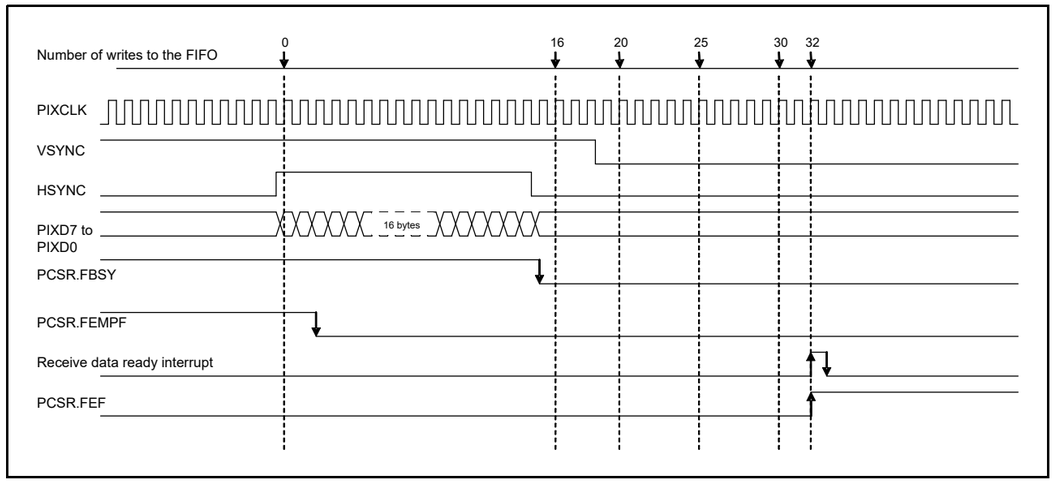


Figure 44.13 Example of continued reception operations at frame end

44.3.7 Error Detection

The PDC provides error detection capabilities, enabling the software to respond to errors during reception operations. Table 44.4 summarizes the conditions for each type of error and the interrupt flags set in response.

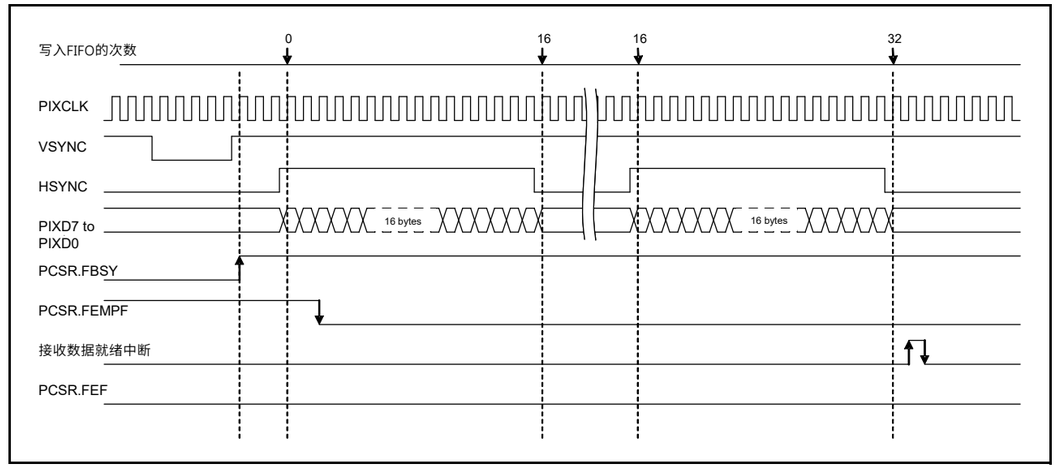


Figure 44.12 水平消隐期间的示例操作

44.3.6 在帧结束时继续接收操作

当接收到最后一个数据，但自上次接收数据就绪后接收到的数据少于32字节时，PDC继续接收数据，直到数量达到32，这种操作称为继续接收。当继续接收结束时，PDC产生一个接收数据就绪中断和一个帧结束中断。在继续接收期间始终输入PIXCLK。如果在此操作期间读取存储在FIFO中的数据，则值未定义。图44.13显示了帧结束时的示例操作。

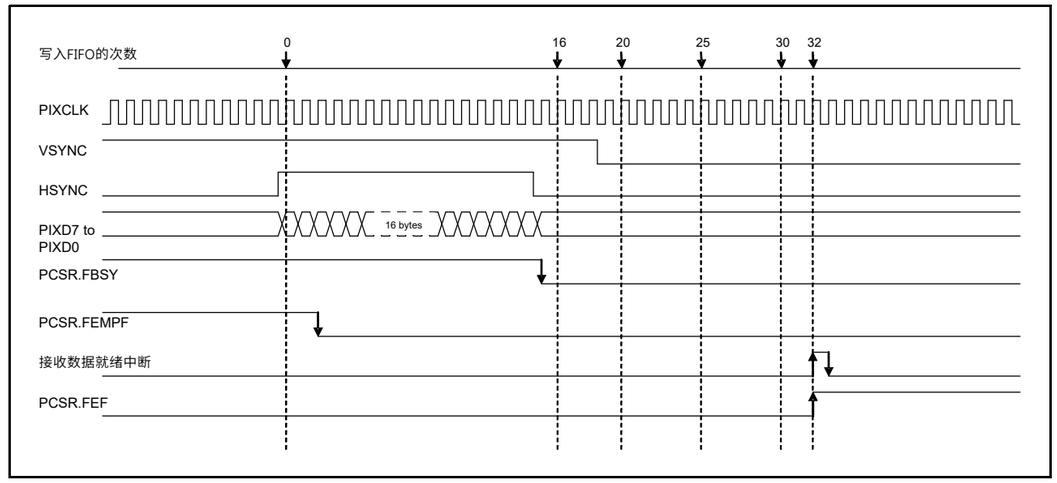


Figure 44.13 帧结束时的连续接收操作示例

44.3.7 错误检测

PDC提供错误检测功能，使软件能够在接收操作期间响应错误。
表44.4总结了每种错误类型的条件和响应设置的中断标志。

Table 44.4 Error detection

Error factor	Conditions for error detection	Interrupt flag	Operation example
Overrun	Receive data arrives while the FIFO is full.*1	PCSR.OVRF	Figure 44.14
Underrun	PCDR register is read while the FIFO is empty.	PCSR.UDRF	Figure 44.15
Vertical line number error	VSYNC signal is negated when the number of captured lines is less than the value set in the VCR register.	PCSR.VERF	Figure 44.16
Horizontal byte number error	HSYNC signal is negated when the number of bytes captured in a line is less than the value set in the HCR register.	PCSR.HERF	Figure 44.17

Note 1. This includes data reception during continued reception operations.

When an error is detected, the PDC sets the associated interrupt flag to 1 to stop reception operations. While the interrupt flag is 1, the PDC does not detect valid edges of the VSYNC signal and does not start reception operations. Clear all error source interrupt flags to 0 to start reception operations.

When an error occurs, data stored in the FIFO is disabled.

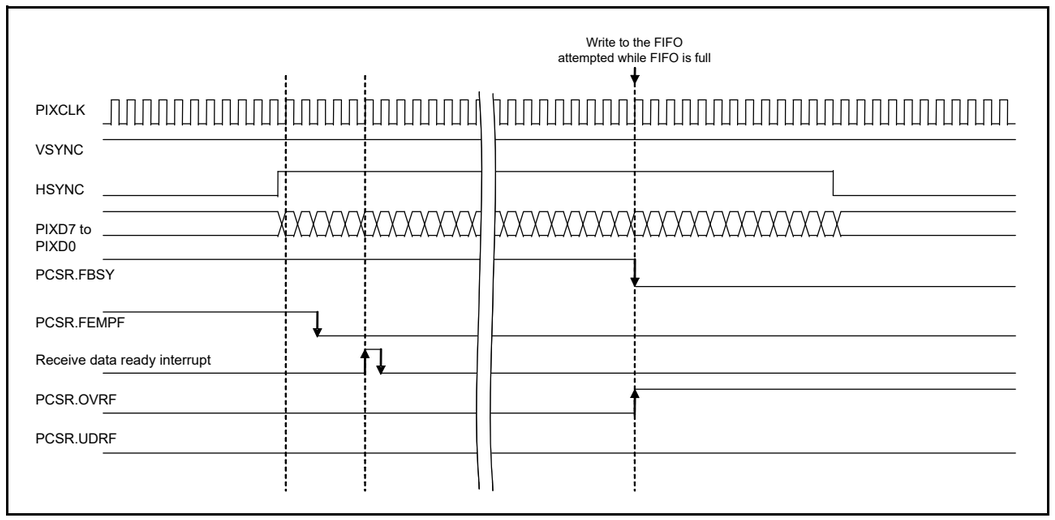


Figure 44.14 Operation when an overrun is detected

Table 44.4 错误检测

误差因素	错误检测的条件	中断标志	操作示例
Overrun	FIFO已满时接收数据到达。*1	PCSR.OVRF	Figure 44.14
Underrun	FIFO为空时读取PCDR寄存器。	PCSR.UDRF	Figure 44.15
垂直行数错误	当捕获的行数小于VCR寄存器中设置的值时，VSYNC信号无效。	PCSR.VERF	Figure 44.16
水平字节数错误	当一行中捕获的字节数小于HCR寄存器中设置的值时，HSYNC信号无效。	PCSR.HERF	Figure 44.17

Note 1. 这包括在连续接收操作期间的数据接收。

当检测到错误时，PDC将相关的中断标志设置为1以停止接收操作。当中断标志为1时，PDC不检测VSYNC信号的有效边沿并且不开始接收操作。将所有错误源中断标志清除为0以开始接收操作。

发生错误时，存储在FIFO中的数据将被禁用。

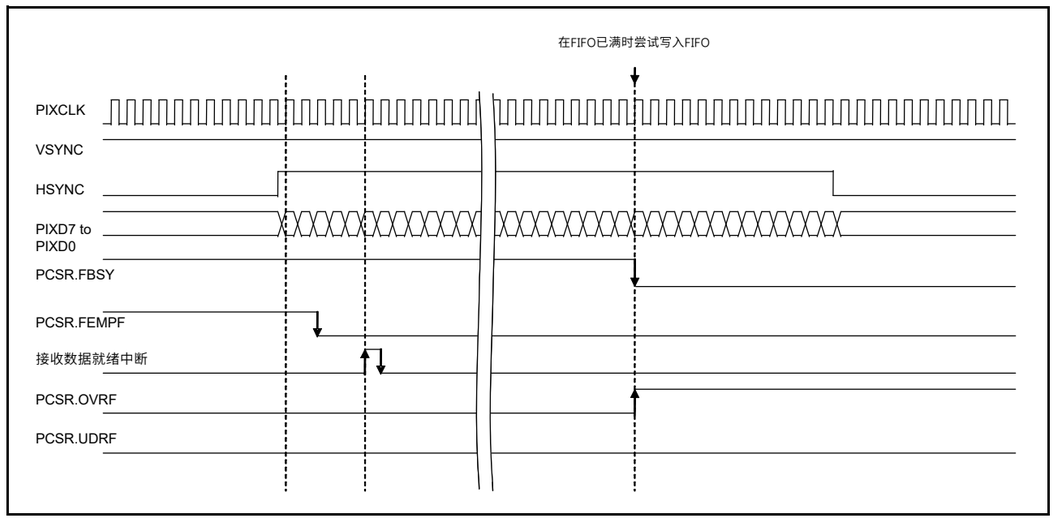


Figure 44.14 检测到溢出时的操作

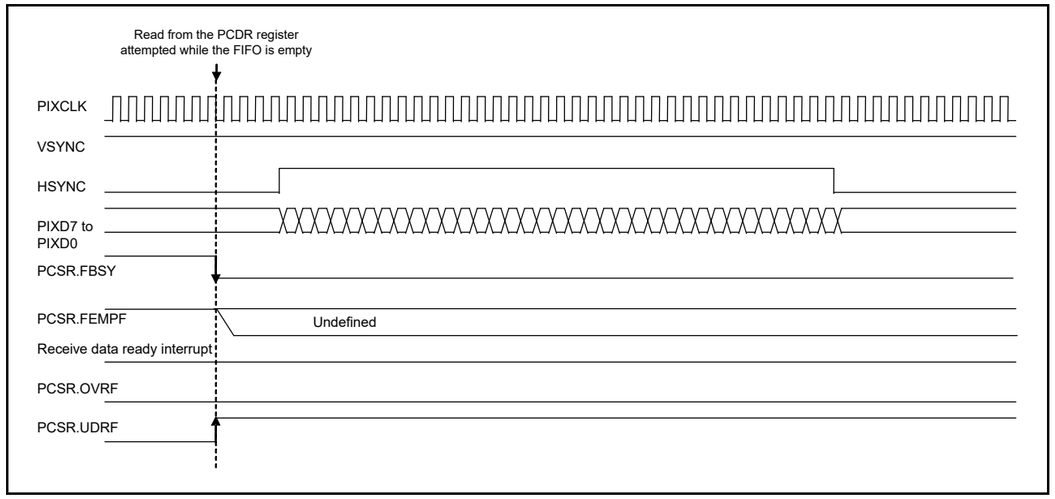


Figure 44.15 Operation when an underrun is detected

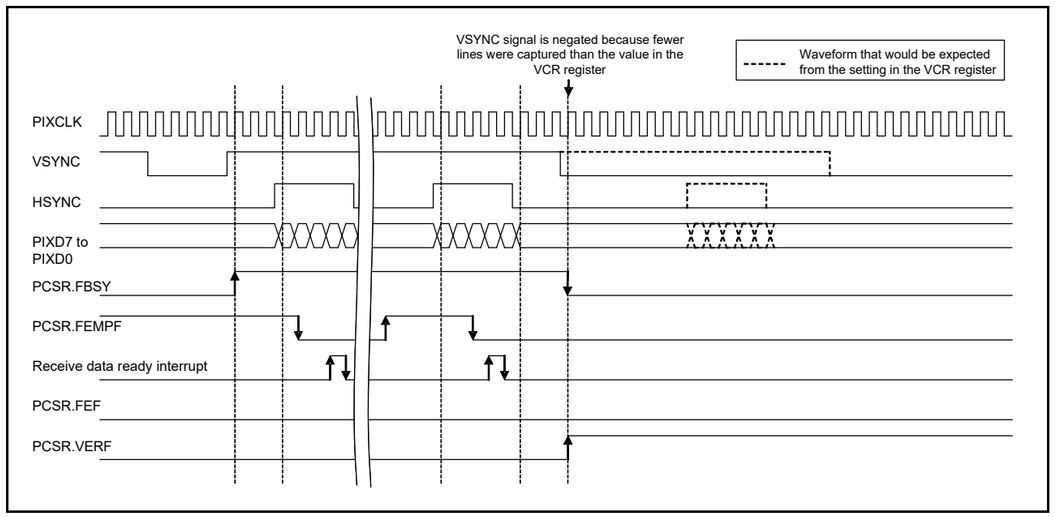


Figure 44.16 Operation when a vertical line number setting error is detected

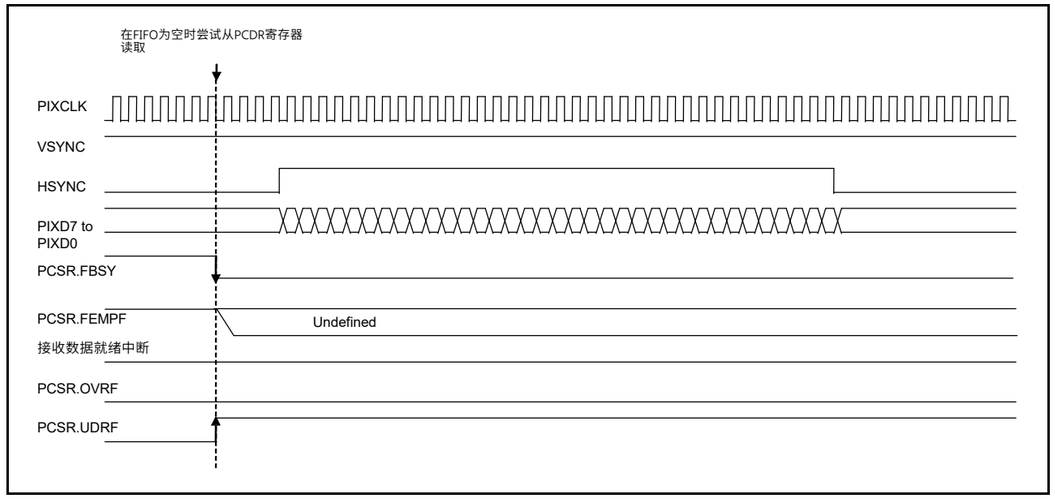


Figure 44.15 检测到欠载时的操作

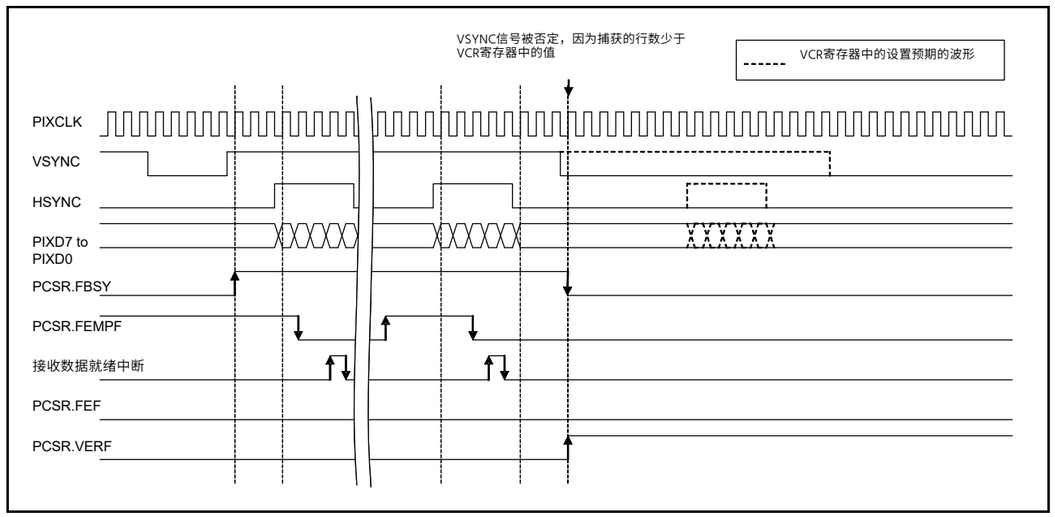


Figure 44.16 检测到垂直行数设置错误时的操作

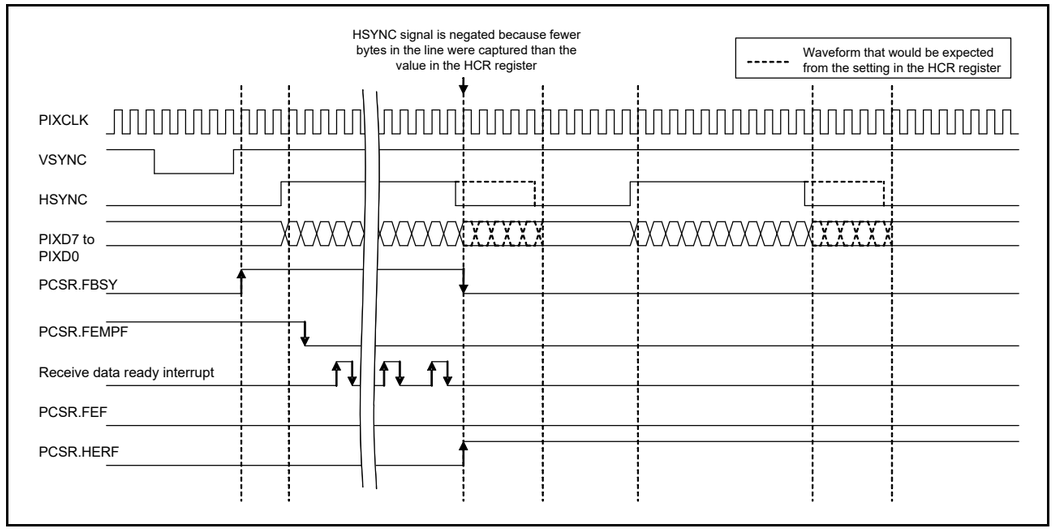


Figure 44.17 Operation when a horizontal byte number setting error is detected

44.3.8 Initial Settings

Figure 44.18 shows an example flow for initial settings. For a description of how to set up the input and output ports and the Interrupt Controller Unit (ICU), see the descriptions given in the sections on the relevant blocks.

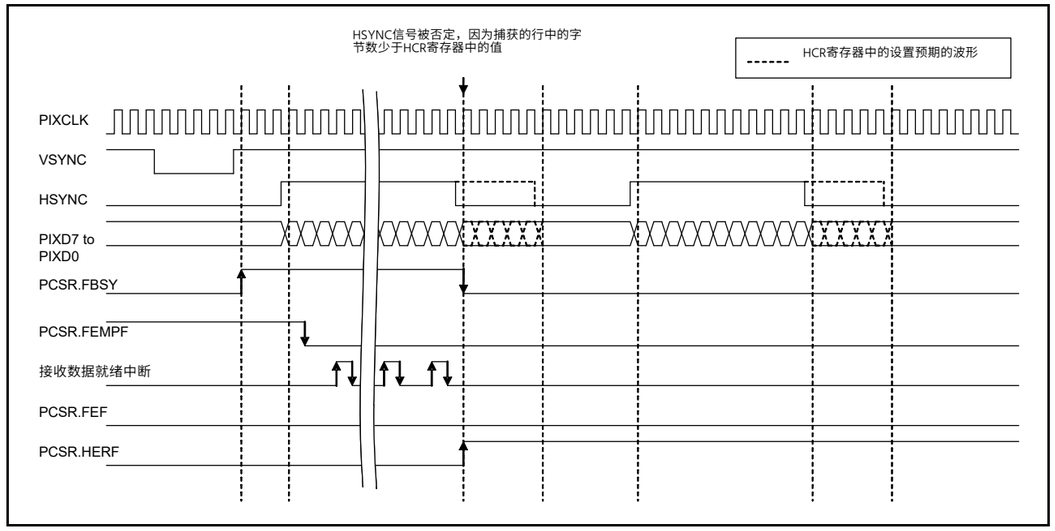


Figure 44.17 检测到水平字节数设置错误时的操作

44.3.8 初始设置

图44.18显示了初始设置的示例流程。有关如何设置输入和输出端口以及中断控制器单元(ICU)的说明，请参阅相关模块部分中的说明。

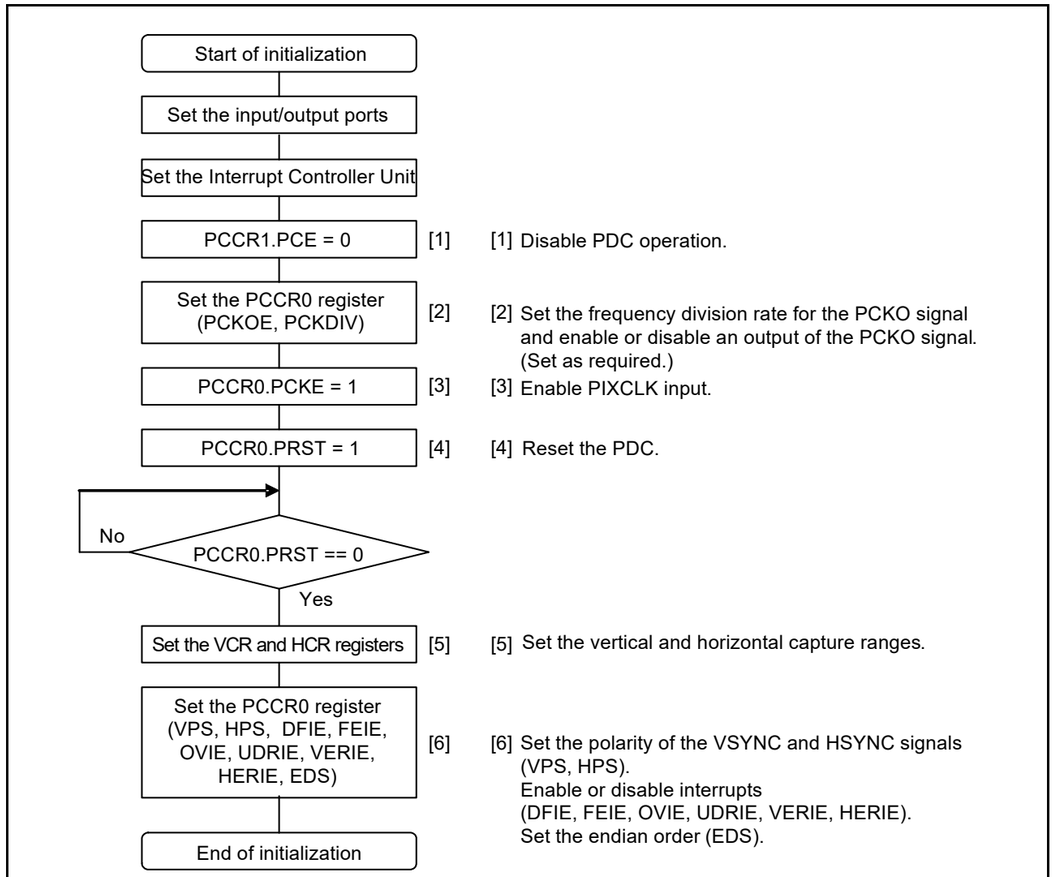


Figure 44.18 Example flow for initial PDC settings

44.3.9 Operation Flows

Figure 44.19 shows an example operation flow when the receive data ready interrupt (to start the DTC or DMAC) and frame end interrupt are in use. For a description of how to set up the DTC or DMAC, see section 17, DMA Controller (DMAC), and section 18, Data Transfer Controller (DTC).

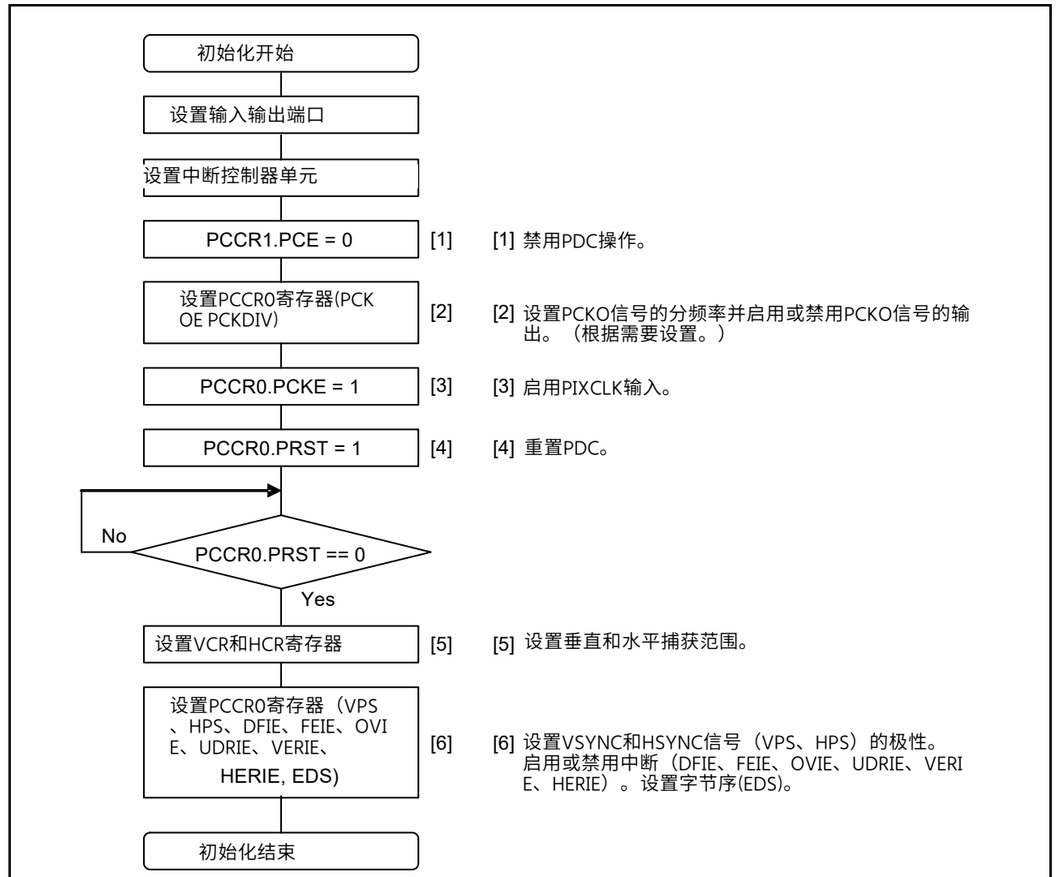
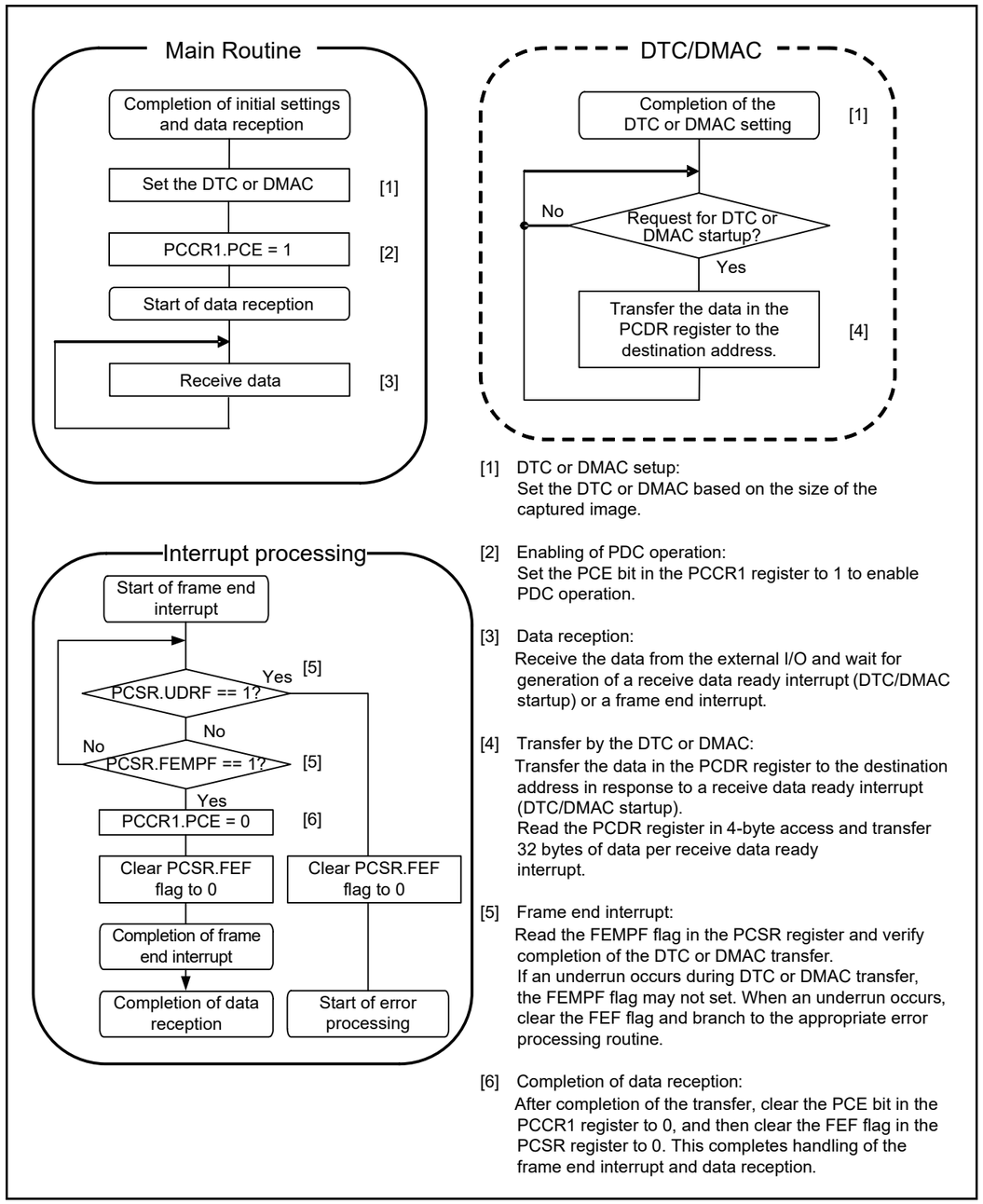


Figure 44.18 初始PDC设置的示例流程

44.3.9 操作流程

图44.19显示了使用接收数据就绪中断（启动DTC或DMAC）和帧结束中断时的示例操作流程。有关如何设置DTC或DMAC的说明，请参阅第17节，DMA控制器(DMAC)和第18节，数据传输控制器(DTC)。



[1] DTC or DMAC setup:
Set the DTC or DMAC based on the size of the captured image.

[2] Enabling of PDC operation:
Set the PCE bit in the PCCR1 register to 1 to enable PDC operation.

[3] Data reception:
Receive the data from the external I/O and wait for generation of a receive data ready interrupt (DTC/DMAC startup) or a frame end interrupt.

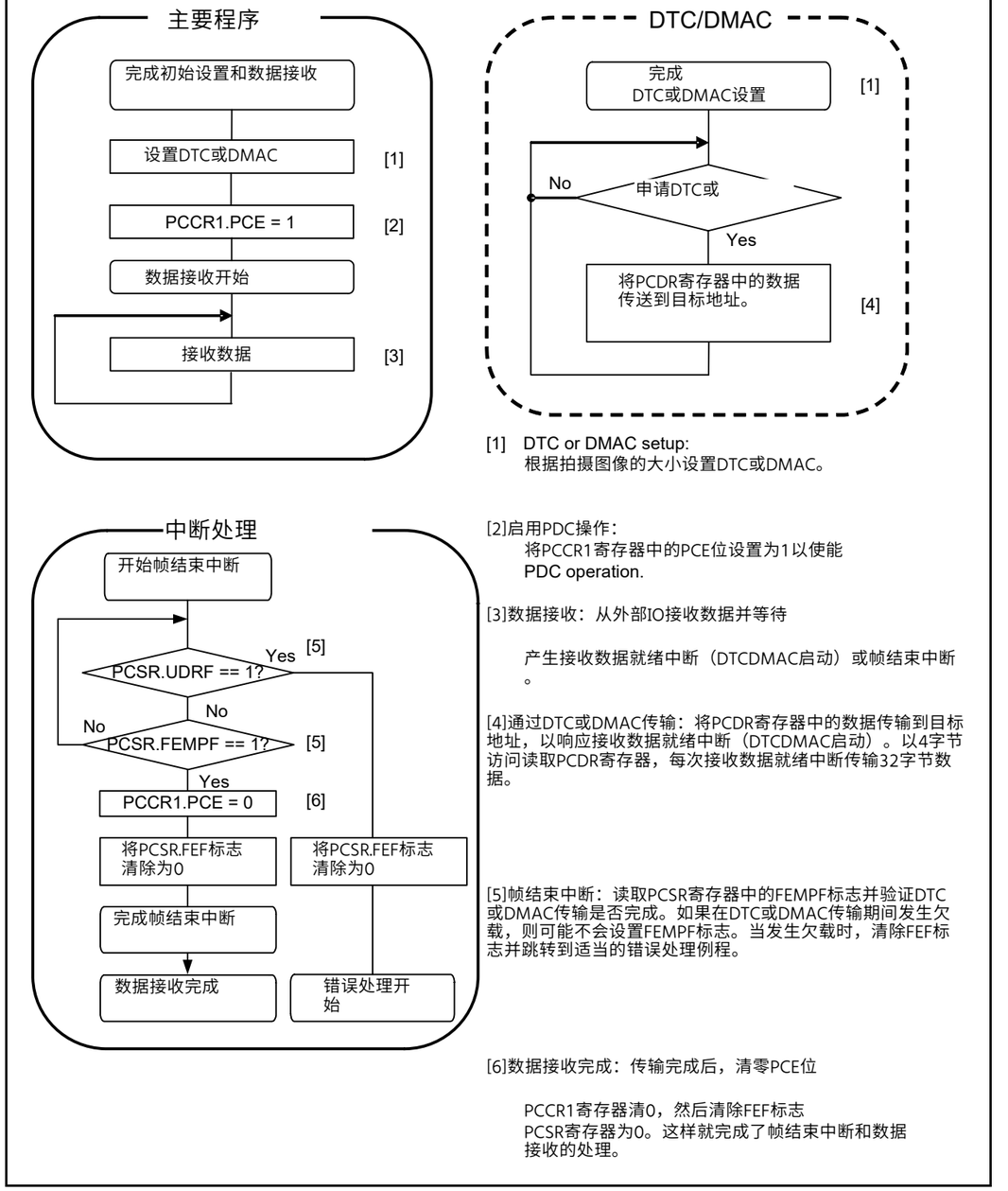
[4] Transfer by the DTC or DMAC:
Transfer the data in the PCDR register to the destination address in response to a receive data ready interrupt (DTC/DMAC startup).
Read the PCDR register in 4-byte access and transfer 32 bytes of data per receive data ready interrupt.

[5] Frame end interrupt:
Read the FEMPF flag in the PCSR register and verify completion of the DTC or DMAC transfer.
If an underrun occurs during DTC or DMAC transfer, the FEMPF flag may not set. When an underrun occurs, clear the FEF flag and branch to the appropriate error processing routine.

[6] Completion of data reception:
After completion of the transfer, clear the PCE bit in the PCCR1 register to 0, and then clear the FEF flag in the PCSR register to 0. This completes handling of the frame end interrupt and data reception.

Figure 44.19 Example operation flow

Figure 44.20 shows an example of the operation flow when responding to an error interrupt.



[1] DTC or DMAC setup:
根据拍摄图像的大小设置DTC或DMAC。

[2]启用PDC操作：
将PCCR1寄存器中的PCE位设置为1以使能PDC operation.

[3]数据接收：从外部IO接收数据并等待

产生接收数据就绪中断（DTCDMAC启动）或帧结束中断。

[4]通过DTC或DMAC传输：将PCDR寄存器中的数据传输到目标地址，以响应接收数据就绪中断（DTCDMAC启动）。以4字节访问读取PCDR寄存器，每次接收数据就绪中断传输32字节数据。

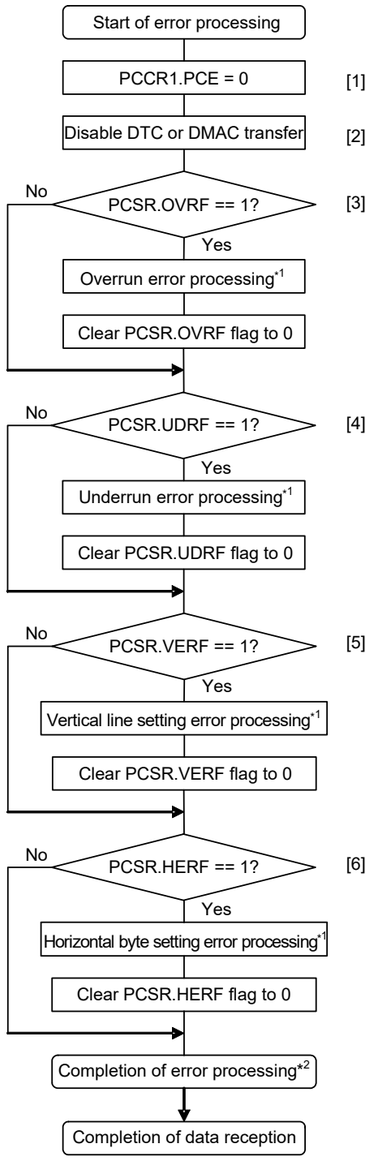
[5]帧结束中断：读取PCSR寄存器中的FEMPF标志并验证DTC或DMAC传输是否完成。如果在DTC或DMAC传输期间发生欠载，则可能不会设置FEMPF标志。当发生欠载时，清除FEF标志并跳转到适当的错误处理例程。

[6]数据接收完成：传输完成后，清零PCE位

PCCR1寄存器清0，然后清除FEF标志
PCSR寄存器为0。这样就完成了帧结束中断和数据接收的处理。

Figure 44.19 示例操作流程

图44.20显示了响应错误中断时的操作流程示例。



[1] Disabling of PDC operation:
Clear the PCE bit in the PCCR1 register to 0 to disable PDC operation.

[2] Disabling of the DTC or DMAC transfer:
Disable the transfer of the DTC or DMAC.

[3] Overrun flag check:
Read the PCSR register to check the state of the OVRF flag. If the flag is set, overrun error handling proceeds, and the flag is then cleared.

[4] Underrun flag check:
Read the PCSR register to check the state of The UDRF flag. If the flag is set, underrun error handling proceeds, and the flag is then cleared.

[5] Check of the vertical line setting error flag:
Read the PCSR register to check the state of the VERF flag. If the flag is set, vertical line setting error handling proceeds, and the flag is then cleared.

[6] Check of the horizontal byte setting error flag:
Read the PCSR register to check the status of the HERF flag. If the flag is set, horizontal byte setting error handling proceeds, and the flag is then cleared.

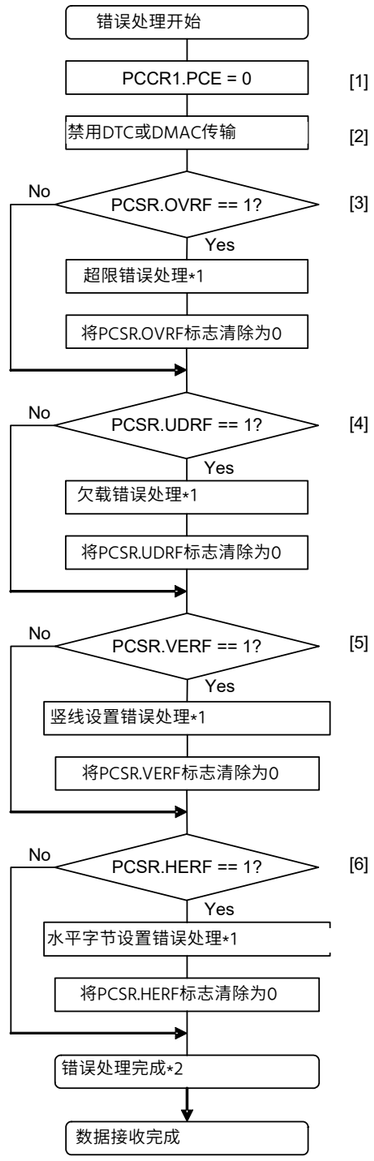
Note 1. Processing for each type of error is defined by the user, so the user needs to prepare error processing for each.
Note 2. If the CPU, DTC, or DMAC reads the PCDR register after an error interrupt occurrs in response to an interrupt source other than an underrun, an underrun may occur.
If an underrun occurs on completion of error processing, run the error processing again and clear the UDRF flag.
Since underruns still require detection after error processing, do not disable the underrun interrupt before the error processing.

Figure 44.20 Example error processing flow

44.3.10 Interrupt Sources

The PDC interrupt sources include:

- Receive data ready
- Frame end
- Overrun



[1]禁用PDC操作：
将PCCR1寄存器中的PCE位清零以禁用PDC操作。

[2]禁用DTC或DMAC传输：禁用DTC或DMAC传输。

[3]溢出标志检查：
读取PCSR寄存器以检查OVRF标志的状态。如果设置了标志，则继续进行溢出错误处理，然后清除标志。

[4] Underrun flag check:
读取PCSR寄存器以检查状态
UDRF标志。如果设置了标志，则继续进行欠载错误处理，然后清除标志。

[5]竖线设置错误标志检查：
读取PCSR寄存器以检查VERF标志的状态。如果设置了标志，则进行垂直线设置错误处理，然后清除标志。

[6]检查水平字节设置错误标志：读取PCSR寄存器以检查HERF标志的状态。如果设置了标志，则进行水平字节设置错误处理，然后清除标志。

注1.每种错误的处理由用户定义，因此用户需要为每种类型准备错误处理。注2.如果CPU、DTC或DMAC在错误中断发生后读取PCDR寄存器以响应欠载以外的中断源，则可能会发生欠载。如果在错误处理完成时发生欠载，请再次运行错误处理并清除UDRF标志。由于在错误处理后仍需要检测欠载，因此在错误处理之前不要禁用欠载中断。

Figure 44.20 错误处理流程示例

44.3.10 中断源

PDC中断源包括：

- 接收数据就绪
- 帧结束
- Overrun

- Underrun
- Vertical line number setting error
- Horizontal byte number setting error.

The PDC can start the DTC or DMAC in response to a receive data ready interrupt request for the transfer of data.

Table 44.5 summarizes the PDC interrupt sources. When an interrupt condition listed in Table 44.5 is satisfied, the associated interrupt is generated. For receive data ready interrupts, the program can clear the interrupt source flag by reading the PCDR register. For the frame end interrupts, clear the FEF flag in the PCSR register. For an overrun, underrun, vertical line number setting error, or a horizontal byte number setting error, the program must check the flags to identify the error source flag, because their interrupt vectors are allocated to the same address by PDC_PCERI. After identifying the source, the program must clear the associated error interrupt source flag (OVRF, UDRF, VERF, or HERF) in the PCSR register.

When the DTC or DMAC module is to handle data transfer, first select the module. After enabling the module for transfers, set up the PDC. For information on setting up the DTC and DMAC, see section 17, DMA Controller (DMAC), and section 18, Data Transfer Controller (DTC).

On completion of output, the request flag clears automatically. An interrupt request signal retained internally can also be cleared by setting the associated interrupt enable bit (the DFIE bit in the PCCR0 register) to 0.

Table 44.5 PDC interrupt sources

Interrupt source	Abbreviation	Interrupt conditions	DTC/DMAC activation
Receive Data Ready	PDC_PCDFI	Receive data ready occurs while the DFIE bit in the PCCR0 register is 1.	Possible
Frame End	PDC_PCFEI	Frame end occurs while the FEIE bit in the PCCR0 register is 1.	Impossible
Errors	PDC_PCERI	• An overrun occurs while the OVIE bit in the PCCR0 register is 1 • An underrun occurs while the UDRIE bit in the PCCR0 register is 1 • A vertical line number setting error occurs while the VERIE bit in the PCCR0 register is 1 • A horizontal byte number setting error occurs while the HERIE bit in the PCCR0 register is 1.	Impossible

44.3.11 Reset State

The PDC has two types of resets: a PDC reset (writing 1 to PCCR0.PRST bit) and other resets.

Other resets include:

- RES pin reset
- Power-on reset
- Voltage monitor reset 0
- Voltage monitor reset 1
- Voltage monitor reset 2
- Deep Software Standby reset
- Independent watchdog timer reset
- Watchdog timer reset
- Software reset
- SRAM parity error reset
- SRAM ECC error reset
- Illegal instruction reset
- Oscillation stop detection reset
- Bus master MPU error reset

- Underrun
- 垂直行数设置错误
- 水平字节数设置错误。

PDC可以启动DTC或DMAC以响应数据传输的接收数据就绪中断请求。

表44.5总结了PDC中断源。当满足表44.5中列出的中断条件时，将产生相关的中断。对于接收数据就绪中断，程序可以通过读取PCDR寄存器来清除中断源标志。对于帧结束中断，清除PCSR寄存器中的FEF标志。对于溢出、欠载、垂直行数设置错误或水平字节数设置错误，程序必须检查标志以识别错误源标志，因为它们的中断向量由PDC_PCERI分配到相同的地址。确定源后，程序必须清除PCSR寄存器中相关的错误中断源标志（OVRF、UDRF、VERF或HERF）。

当DTC或DMAC模块要处理数据传输时，首先选择模块。启用传输模块后，设置PDC。有关设置DTC和DMAC的信息，请参阅第17节，DMA控制器(DMAC)和第18节，数据传输控制器(DTC)。

输出完成后，请求标志自动清除。内部保留的中断请求信号也可以通过将相关的中断使能位（PCCR0寄存器中的DFIE位）设置为0来清除。

Table 44.5 PDC中断源

中断源	Abbreviation	中断条件	DTC/DMAC activation
接收数据就绪	PDC_PCDFI	PCCR0寄存器中的DFIE位为1时发生接收数据准备就绪。	Possible
帧结束	PDC_PCFEI	PCCR0寄存器中的FEIE位为1时发生帧结束。	Impossible
Errors	PDC_PCERI	PCCR0寄存器中的OVIE位为1时发生溢出 PCCR0寄存器中的UDRIE位为1时发生下溢 PCCR0寄存器中的VERIE位为1时发生垂直行数设置错误 水平字节PCCR0寄存器中的HERIE位为1时发生数字设置错误。	Impossible

44.3.11 重置状态

PDC有两种类型的复位：PDC复位（向PCCR0.PRST位写入1）和其他复位。

其他重置包括：

- RES引脚复位
- Power-on reset
- 电压监视器复位0
- 电压监视器复位1
- 电压监视器复位2
- 深度软件待机复位
- 独立看门狗定时器复位
- 看门狗定时器复位
- 软件复位
- SRAM奇偶校验错误复位
- SRAMECC错误复位
- 非法指令复位
- 振荡停止检测复位
- 总线主控MPU错误复位

- Bus slave MPU error reset
- Stack pointer error reset
- Watchdog timer reset in reset sequence.

Table 44.6 shows the register states following the two types of resets.

Table 44.6 Register states on reset

PDC register	PDC reset	Other resets
PCCR0	Retained	Reset
PCCR1	Retained	Reset
PCSR	Reset	Reset
PCMONR	Retained	Reset
PCDR	Retained	Reset
VCR	Retained	Reset
HCR	Retained	Reset

44.4 Usage Notes

44.4.1 Settings for the Module-Stop Function

PDC operation can be disabled or enabled using the MSTPC2 bit in Module Stop Control Register C (MSTPCRC). The PDC is initially stopped (MSTPC2 =1) after reset. Releasing the module-stop state enables access to the registers. For details, see section 11, Low Power Modes.

44.4.2 Constraints on the Low-Power Function

When reducing PDC power consumption by using the low-power function, set the PCE bit in the PCCR1 register to 0 to disable reception operations, and set the PCKE bit in the PCCR0 register to 0 to disable input through the PIXCLK pin. Use the low-power function after these settings are complete.

If the PCKOE bit in the PCCR0 register is set to 1, set it to 0 to stop output of the PCKO signal, in addition to disabling input through the PIXCLK pin in PCKE. Use the low-power function after these settings are complete.

44.4.3 Constraints on Error Interrupts

When an error interrupt occurs, the DTC or DMAC might still be transmitting parallel data, depending on their operation state. Because of this, the error interrupt processing routine must prohibit data transmission by the DTC or DMAC immediately after prohibiting PDC operation (PCCR1.PCE = 0).

44.4.4 Constraints on Using the DTC

When the DTC is used with the receive data ready interrupt, set the DISEL bit in the MRB register to 0 and the SZ bit in the MRA register to 10b.

The maximum number of blocks the DTC can transfer in block transfer mode is 65,536. If 32 bytes are transferred per block transfer, this represents a total of up to 2,097,152 bytes. If more data is to be transferred, set up the DTC again during the horizontal blanking period. For details, see section 18, Data Transfer Controller (DTC).

44.4.5 Constraints on Using the DMAC

When the DMAC is used with the receive data ready interrupt, set the SZ bit in the DMTMD register to 10b, and configure the DESL[8:0] bits in the DELSRn register (n = 0 to 7) appropriately.

The maximum number of blocks the DMAC can transfer in block transfer mode is 65,536. If 32 bytes are transferred per block transfer, this represents a total of up to 2,097,152 bytes. If more data is to be transferred, set up the DMAC again during the horizontal blanking period. For details, see section 14, Interrupt Controller Unit (ICU) and section 17, DMA Controller (DMAC).

- 总线从机MPU错误复位
- 堆栈指针错误复位
- 看门狗定时器按复位顺序复位。

表44.6显示了两种复位后的寄存器状态。

Table 44.6 复位时注册状态

PDC register	PDC reset	其他重置
PCCR0	Retained	Reset
PCCR1	Retained	Reset
PCSR	Reset	Reset
PCMONR	Retained	Reset
PCDR	Retained	Reset
VCR	Retained	Reset
HCR	Retained	Reset

44.4 使用说明

44.4.1 模块停止功能的设置

可以使用模块停止控制寄存器C(MSTPCRC)中的MSTPC2位禁用或启用PDC操作。这
PDC在复位后最初停止(M STPC2=1)。释放模块停止状态可以访问寄存器。有关详细信息，请参阅第11节，低功耗模式。

44.4.2 对低功耗函数的约束

使用低功耗功能降低PDC功耗时，将PCCR1寄存器中的PCE位设置为0以禁用接收操作，并将PCCR0寄存器中的PCKE位设置为0以禁用通过PIXCLK引脚的输入。完成这些设置后使用低功耗功能。

如果PCCR0寄存器中的PCKOE位设置为1，则将其设置为0以停止输出PCKO信号，同时禁止通过PCKE中的PIXCLK引脚输入。完成这些设置后使用低功耗功能。

44.4.3 错误中断的约束

发生错误中断时，DTC或DMAC可能仍在传输并行数据，具体取决于它们的操作状态。因此，错误中断处理程序必须在禁止PDC操作(PCCR1.PCE=0)后立即禁止DTC或DMAC的数据传输。

44.4.4 使用DTC的限制

当DTC与接收数据就绪中断一起使用时，将MRB寄存器中的DISEL位设置为0，并将MRA寄存器中的SZ位设置为10b。

DTC在块传输模式下可以传输的最大块数为65 536。如果每次块传输传输32个字节，则总共最多2 097 152个字节。如果要传输更多数据，请在水平消隐期间再次设置DTC。有关详细信息，请参阅第18节，数据传输控制器(DTC)。

44.4.5 使用DMAC的限制

当DMAC与接收数据就绪中断一起使用时，将DMTMD寄存器中的SZ位设置为10b，并适当配置DELSRn寄存器中的DESL[8:0]位（n=0至7）。

DMAC在块传输模式下可以传输的最大块数为65 536。如果每次块传输传输32个字节，则总共最多2 097 152个字节。如果要传输更多数据，请在水平消隐期间再次设置DMAC。有关详细信息，请参阅第14节，中断控制器单元(ICU)和第17节，DMA控制器(DMAC)。

45. Boundary Scan

45.1 Overview

The boundary scan function provides a serial I/O interface based on the JTAG (Joint Test Action Group), IEEE Std. 1149.1, and IEEE Standard Test Access Port and Boundary Scan Architecture. Table 45.1 lists the boundary scan specifications, Figure 45.1 shows a block diagram, and Table 45.2 lists the I/O pins.

Table 45.1 Boundary scan specifications

Parameter	Specifications
Execution condition	Boundary scan must be executed when the RES pin is driven low.
Test modes	• BYPASS mode • EXTEST mode • SAMPLE/PRELOAD mode • CLAMP mode • HIGHZ mode • IDCODE mode

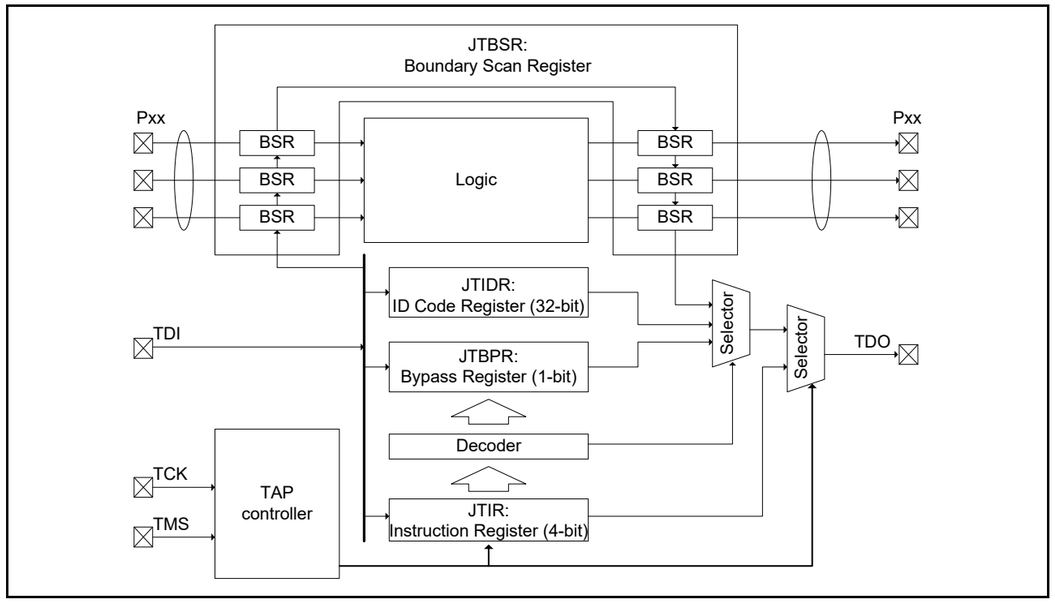


Figure 45.1 Boundary scan function block diagram

Table 45.2 Boundary scan I/O pins

Pin name	I/O	Description
TCK	Input	Test clock input pin Clock signal for boundary scan. The input clock duty cycle is 50% when the boundary scan function is used.
TMS	Input	Test mode select pin
TDI	Input	Test data input pin
TDO	Output	Test data output pin

Note: The MCU does not support the TRST pin for the JTAG interface.

45. 边界扫描

45.1 Overview

边界扫描功能提供基于JTAG（联合测试行动组）、IEEEStd.的串行IO接口。1149.1和IEEE标准测试访问端口和边界扫描架构。表45.1列出了边界扫描规范，图45.1显示了框图，表45.2列出了IO引脚。

Table 45.1 边界扫描规格

Parameter	Specifications
执行条件	当RES引脚驱动为低电平时，必须执行边界扫描。
测试模式	BYPASS模式 EXTEST模式 SAMPLEPRELOAD模式 CLAMP模式 HIGHZ模式 IDCODE模式

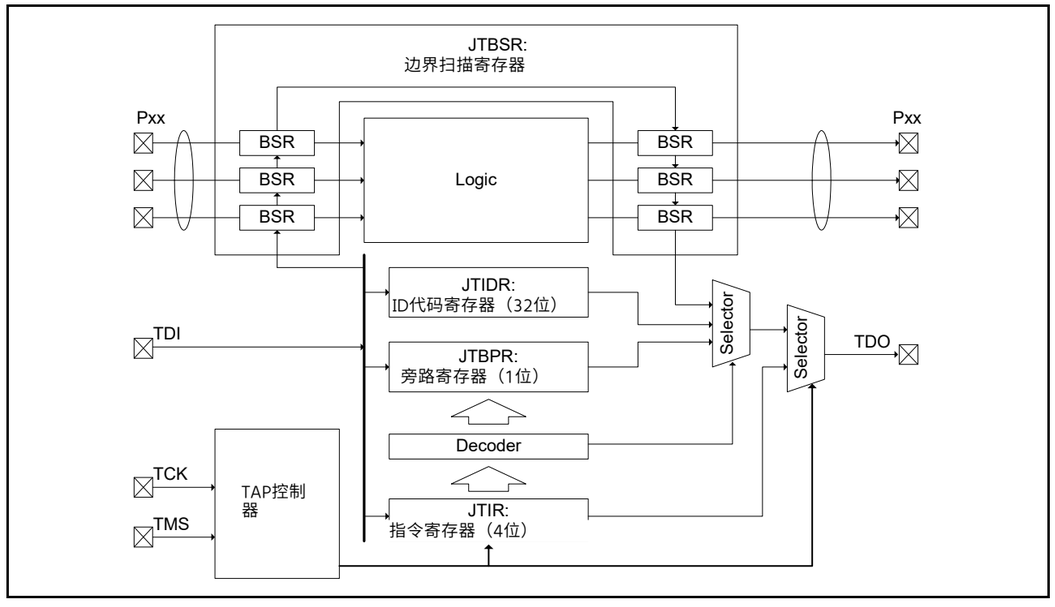


Figure 45.1 边界扫描功能框图

Table 45.2 边界扫描IO引脚

引脚名称	I/O	Description
TCK	Input	测试时钟输入引脚 边界扫描的时钟信号。使用边界扫描功能时，输入时钟占空比为50%。
TMS	Input	测试模式选择引脚
TDI	Input	测试数据输入引脚
TDO	Output	测试数据输出引脚

Note: MCU不支持JTAG接口的TRST引脚。

45.2 Register Descriptions

Table 45.3 lists the boundary scan registers.

Table 45.3 Boundary scan registers

Register name	Symbol	Value after reset
Instruction Register	JTIR	Eh
ID Code Register	JTIDR	0832 9447h
Bypass Register	JTBPR	Undefined
Boundary Scan Register	JTBSR	Undefined

Usage notes for the boundary scan registers:

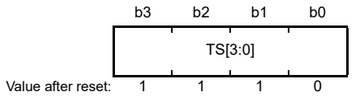
- Instructions can be input to the Instruction Register (JTIR) through the TDI pin by serial transfer.
- The Bypass Register (JTBPR), which is a 1-bit register, is connected between the TDI and TDO pins in BYPASS mode.
- The Boundary Scan Register (JTBSR), which is configured according to the BSDL description, is connected between the TDI and TDO pins when test data is being shifted in.

Table 45.4 shows the availability of serial transfer for the registers.

Table 45.4 Serial transfer for registers

Register name	Serial input	Serial output
Instruction Register (JTIR)	Available	Available
ID Code Register (JTIDR)	Available	Available
Bypass Register (JTBPR)	Available	Available
Boundary Scan Register (JTBSR)	Available	Available

45.2.1 Instruction Register (JTIR)



Bit	Symbol	Bit name	Description	R/W
b3 to b0	TS[3:0]	Test Bit Set	The command configuration for these bits is shown in Table 45.5.	—

Table 45.5 Command configuration

TS3	TS2	TS1	TS0	Instruction
0	0	0	0	EXTEST
0	0	0	1	SAMPLE/PRELOAD
0	0	1	1	IDCODE (Renesas code)
0	1	0	1	CLAMP
0	1	1	0	HIGHZ
1	1	1	1	BYPASS
Other settings				Reserved

JTAG instructions can be transferred to the JTIR register by serial input from the TDI pin. The JTIR register is initialized when a power-on reset occurs, or when the TAP controller is in the Test-Logic-Reset state.

45.2 注册说明

表45.3列出了边界扫描寄存器。

Table 45.3 边界扫描寄存器

注册名称	Symbol	重置后的值
指令寄存器	JTIR	Eh
ID代码寄存器	JTIDR	0832 9447h
绕过寄存器	JTBPR	Undefined
边界扫描寄存器	JTBSR	Undefined

边界扫描寄存器的使用说明：

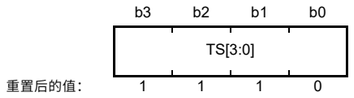
- 指令可以通过串行传输通过TDI引脚输入到指令寄存器(JTIR)。
- 旁路寄存器(JTBPR)是一个1位寄存器，在BYPASS模式下连接在TDI和TDO引脚之间。
- 根据BSDL描述配置的边界扫描寄存器(JTBSR)在移入测试数据时连接在TDI和TDO引脚之间。

表45.4显示了寄存器串行传输的可用性。

Table 45.4 寄存器的串行传输

注册名称	串行输入	串行输出
指令寄存器(JTIR)	Available	Available
ID代码寄存器(JTIDR)	Available	Available
旁路寄存器(JTBPR)	Available	Available
边界扫描寄存器(JTBSR)	Available	Available

45.2.1 指令寄存器(JTIR)



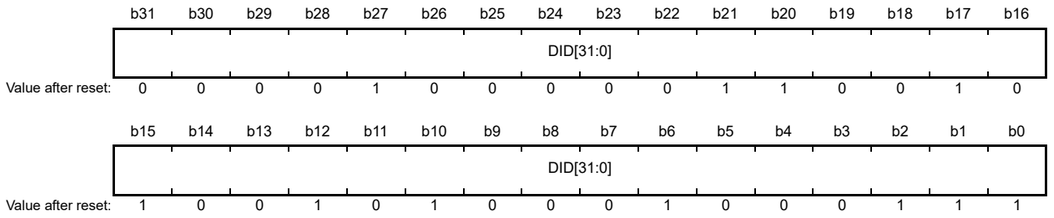
Bit	Symbol	位名称	Description	R/W
b3 to b0	TS[3:0]	测试位组	这些位的命令配置如表45.5所示。	—

Table 45.5 命令配置

TS3	TS2	TS1	TS0	Instruction
0	0	0	0	EXTEST
0	0	0	1	SAMPLE/PRELOAD
0	0	1	1	IDCODE (Renesas code)
0	1	0	1	CLAMP
0	1	1	0	HIGHZ
1	1	1	1	BYPASS
其他设置				Reserved

JTAG指令可以通过TDI引脚的串行输入传输到JTIR寄存器。当发生上电复位或TAP控制器处于Test-Logic-Reset状态时，JTIR寄存器被初始化。

45.2.2 ID Code Register (JTIDR)



Bit	Symbol	Bit name	Description	R/W
b31 to b0	DID[31:0]	Device ID	These bits store the fixed value that indicates the device IDCODE.	—

JTIDR data is output from the TDO pin when the IDCODE instruction is executed. After a reset release, the IDCODE of JTIDR changes into the Arm® debug code. See the *ARM® CoreSight™ SoC-400 Technical Reference Manual* (ARM DDI 0480F).

45.2.3 Bypass Register (JTBPR)

JTBPR is a 1-bit register and is connected between the TDI and TDO pins when the JTIR register is set to BYPASS mode. The JTBPR register cannot be read from or written to by the CPU.

45.2.4 Boundary Scan Register (JTBSR)

JTBSR is a shift register for controlling the external input and output pins of the MCU, and is distributed across the pads. To apply the JTBSR register in boundary-scan testing, issue the EXTEST, SAMPLE/PRELOAD, CLAMP, and HIGHZ instructions. The BSDL file describes the associations between the JTBSR bits and the pins of the MCU. The value after reset is undefined.

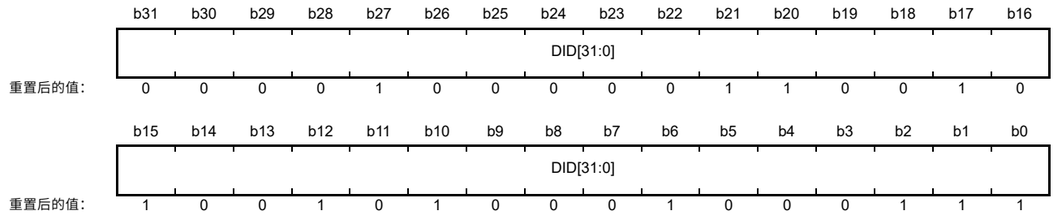
45.3 Operation

During a reset, the JTAG ports, TCK, TMS, TDI, and TDO, are assigned as default pin functions. The TCK, TMS, and TDI pins are pulled up by the pull-up resistors. Boundary scan testing can be executed after the setup time elapses when POR is negated and RES is driven low.

45.3.1 TAP Controller

Figure 45.2 shows the state transition diagram of the TAP controller. All transitions are controlled by the TMS signal.

45.2.2 ID代码寄存器(JTIDR)



Bit	Symbol	位名称	Description	R/W
b31 to b0	DID[31:0]	设备ID	这些位存储指示设备IDCODE的固定值。	—

执行IDCODE指令时，从TDO引脚输出JTIDR数据。复位释放后，IDCODE JTIDR更改为Arm®调试代码。请参阅ARM®CoreSight SoC-400技术参考手册（ARM DDI 0480F).

45.2.3 旁路寄存器(JTBPR)

JTBPR是一个1位寄存器，当JTIR寄存器设置为BYPASS模式时，连接在TDI和TDO引脚之间。CPU无法读取或写入JTBPR寄存器。

45.2.4 边界扫描寄存器(JTBSR)

JTBSR是一个移位寄存器，用于控制MCU的外部输入和输出引脚，分布在各个焊盘上。要在边界扫描测试中应用JTBSR寄存器，请发出EXTEST、SAMPLEPRELOAD、CLAMP和HIGHZ指令。BSDL文件描述了JTBSR位和MCU引脚之间的关联。复位后的值未定义。

45.3 Operation

在复位期间，JTAG端口、TCK、TMS、TDI和TDO被分配为默认引脚功能。TCK、TMS和TDI引脚由上拉电阻上拉。边界扫描测试可以在设置时间过去后执行，当
POR被取反，RES被驱动为低电平。

45.3.1 水龙头控制器

图45.2显示了TAP控制器的状态转换图。所有转换都由TMS信号控制。

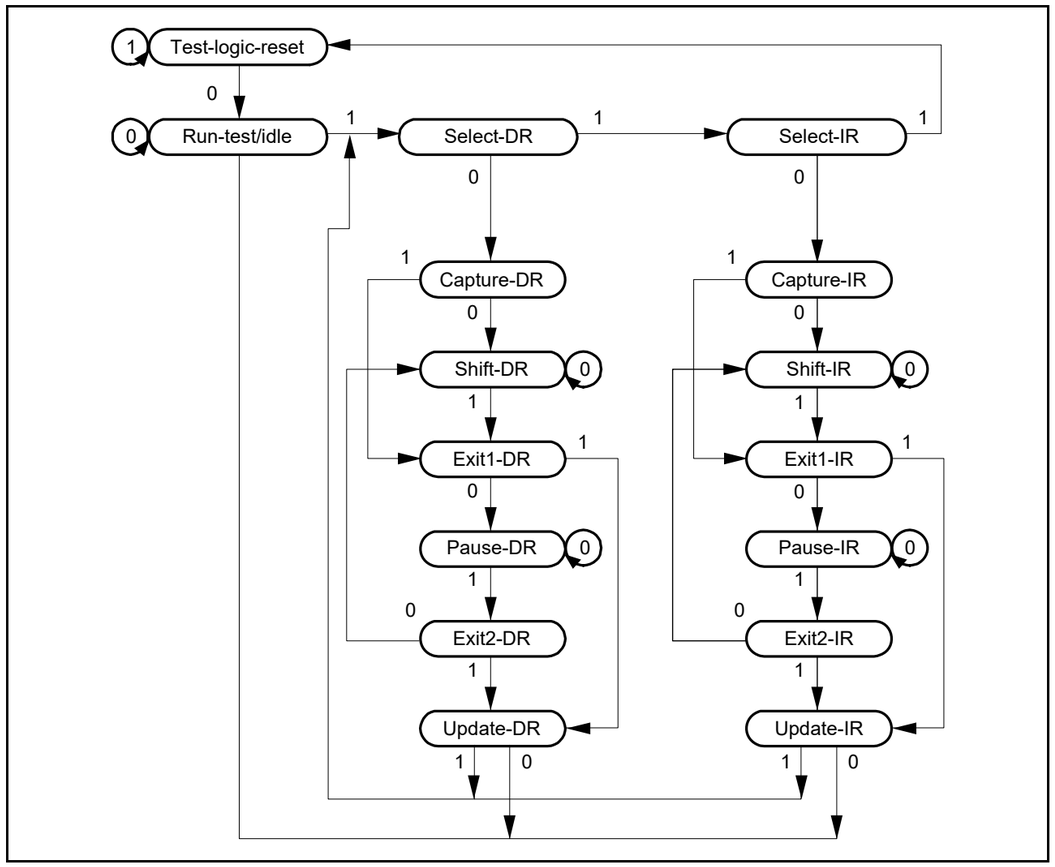


Figure 45.2 State transition diagram of TAP controller

45.3.2 Commands

(1) BYPASS

The BYPASS instruction drives the Bypass Register (JTBPR). This instruction shortens the shift path, facilitating the transfer of serial data to other LSIs on a printed circuit board at higher speeds. While this instruction is being executed, the test circuit has no effect on the system circuits.

The Bypass Register (JTBPR) is connected between the TDI and TDO pins. Bypass operation is initiated from the Shift-DR operation. The TDO is low in the first clock cycle in the Shift-DR state. In the subsequent clock cycles, the TDI signal is output on the TDO pin.

(2) EXTEST

The EXTEST instruction is used to test external circuits when the MCU is installed on the printed circuit board. If this instruction is executed, output pins are used to output test data (specified in the SAMPLE/PRELOAD instruction) from the Boundary Scan Register (JTBSR) to the print circuit board, and input pins are used to input the test result.

(3) SAMPLE/PRELOAD

The SAMPLE/PRELOAD instruction is used to input data from the internal circuits of the MCU to the Boundary Scan Register (JTBSR), output data from the scan path, and reload the data to the scan path. While this instruction is executed, input signals are directly input to the MCU and output signals are also directly output to the external circuits. The MCU system circuit is not affected by this instruction.

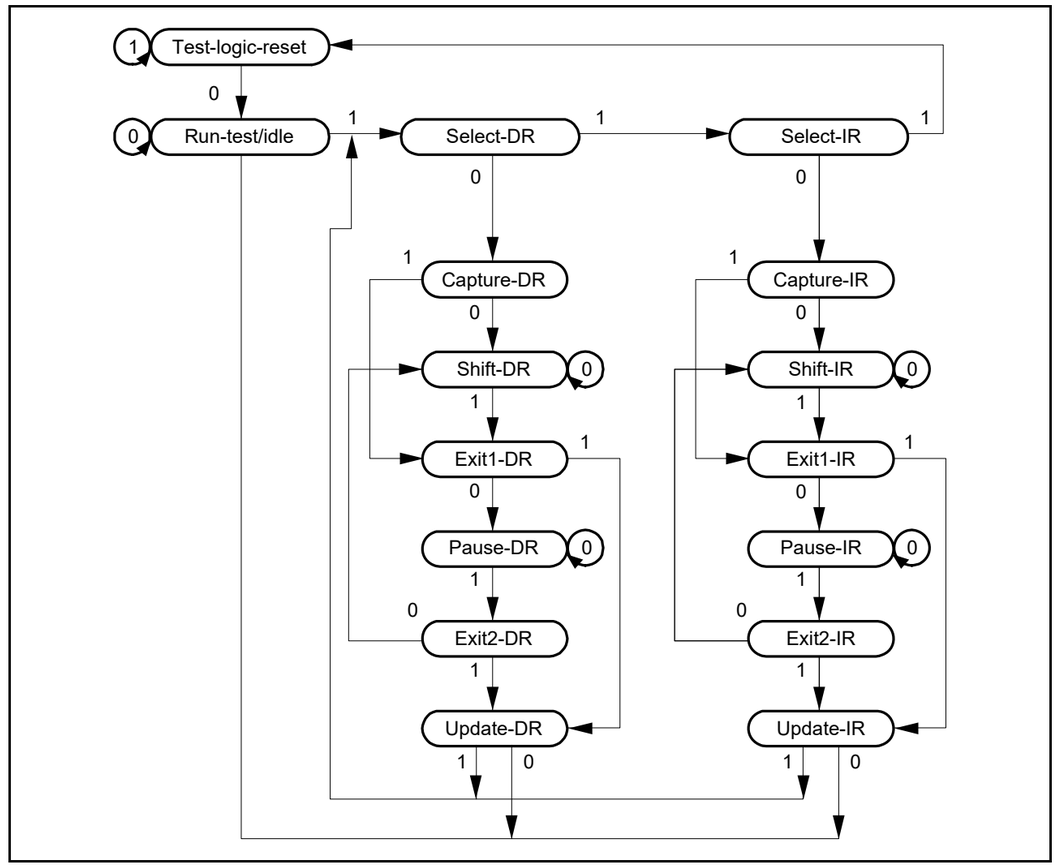


Figure 45.2 TAP控制器的状态转移图

45.3.2 Commands

(1) BYPASS

BYPASS指令驱动旁路寄存器(JTBPR)。该指令缩短了移位路径，便于将串行数据以更高的速度传输到印刷电路板上的其他LSI。在执行该指令时，测试电路对系统电路没有影响。

旁路寄存器(JTBPR)连接在TDI和TDO引脚之间。旁路操作从Shift启动
DR操作。TDO在Shift-DR状态的第一个时钟周期内为低电平。在随后的时钟周期中，TDI信号在TDO引脚上输出。

(2) EXTEST

EXTEST指令用于单片机安装在印刷电路板上时测试外部电路。如果执行该指令，输出引脚用于将测试数据（在SAMPLEPRELOAD指令中指定）从边界扫描寄存器（JTBSR）输出到印刷电路板，输入引脚用于输入测试结果。

(3) SAMPLE/PRELOAD

SAMPLEPRELOAD指令用于将数据从MCU内部电路输入到边界扫描寄存器（JTBSR），从扫描路径输出数据，并将数据重新加载到扫描路径。在执行该指令时，输入信号直接输入到MCU，输出信号也直接输出到外部电路。MCU系统电路不受该指令影响。

In SAMPLE operation, the Boundary Scan Register (JTBSR) latches a snapshot of the data transferred from the input pins to the internal circuit or data transferred from the internal circuit to the output pins. The latched data is read from the scan path. The JTBSR register latches the data snapshot on the rising edge of the TCK pin in the Capture-DR state. The data snapshot is only transferred from the internal circuit to the output pins during a reset.

In PRELOAD operation, the initial value is written from the scan path to the parallel output latch of the Boundary Scan Register (JTBSR) prior to the EXTEST instruction execution. If EXTEST is executed without executing this PRELOAD operation, undefined values are output from the beginning to the end (transfer to the output latch) of the EXTEST sequence. (In the EXTEST instruction, output parallel latches are always output to the output pins.)

(4) IDCODE

When the IDCODE instruction is selected, the ID Code Register (JTIDR) value is output to the TDO pin in the Shift-DR state of the TAP controller. In this case, the JTIDR register value is output LSB-first. During this instruction execution, the test circuit does not affect the system circuit.

(5) CLAMP

When the CLAMP instruction is selected, output pins output the Boundary Scan Register (JTBSR) value that was specified in the SAMPLE/PRELOAD instruction in advance. While the CLAMP instruction is selected, the status of the JTBSR register is maintained regardless of the TAP controller state.

The Bypass Register (JTBPR) is connected between the TDI and TDO pins, leading to the same operation as when the BYPASS instruction is selected.

(6) HIGHZ

When the HIGHZ instruction is selected, all output pins enter high-impedance state. While the HIGHZ instruction is selected, the status of Boundary Scan Register (JTBSR) is maintained regardless of the state of the TAP controller.

The Bypass Register (JTBPR) is connected between the TDI and TDO pins, leading to the same operation as when the BYPASS instruction is selected.

45.4 Usage Notes

The boundary scan function is subject to the following constraints:

- The boundary scan must be executed when the RES pin is driven low
- Serial data input/output is in LSB order, as shown in Figure 45.3.

在SAMPLE操作中，边界扫描寄存器(JTBSR)锁存从输入引脚传输到内部电路的数据或从内部电路传输到输出引脚的数据的快照。从扫描路径读取锁存的数据。在Capture-DR状态下，JTBSR寄存器在TCK引脚的上升沿锁存数据快照。数据快照仅在复位期间从内部电路传输到输出引脚。

在PRELOAD操作中，在执行EXTEST指令之前，将初始值从扫描路径写入边界扫描寄存器(JTBSR)的并行输出锁存器。如果在不执行此PRELOAD操作的情况下执行EXTEST，则从EXTEST序列的开头到结尾（传输到输出锁存器）输出未定义的值。（在EXTEST指令中，输出并行锁存器始终输出到输出引脚。）

(4) IDCODE

WhentheIDCODEinstructionisselected theIDCodeRegister(JTIDR)valueisoutputtotheTDOpinintheShift-DRstateoftheTAPcontroller.在这种情况下，JTIDR寄存器值首先输出LSB。在该指令执行期间，测试电路不影响系统电路。

(5) CLAMP

选择CLAMP指令时，输出引脚输出预先在SAMPLEPRELOAD指令中指定的边界扫描寄存器(JTBSR)值。选择CLAMP指令时，无论TAP控制器状态如何，都将保持JTBSR寄存器的状态。

旁路寄存器(JTBPR)连接在TDI和TDO引脚之间，导致与当
选择了BYPASS指令。

(6) HIGHZ

选择Highz指令时，所有输出引脚都输入高阻抗状态。选择HIGHZ指令时，无论TAP控制器的状态如何，边界扫描寄存器(JTBSR)的状态都会保持不变。

旁路寄存器(JTBPR)连接在TDI和TDO引脚之间，导致与当
选择了BYPASS指令。

45.4 使用说明

边界扫描函数受以下约束：

- 当RES引脚驱动为低电平时，必须执行边界扫描
- 串行数据输入输出按LSB顺序排列，如图45.3所示。

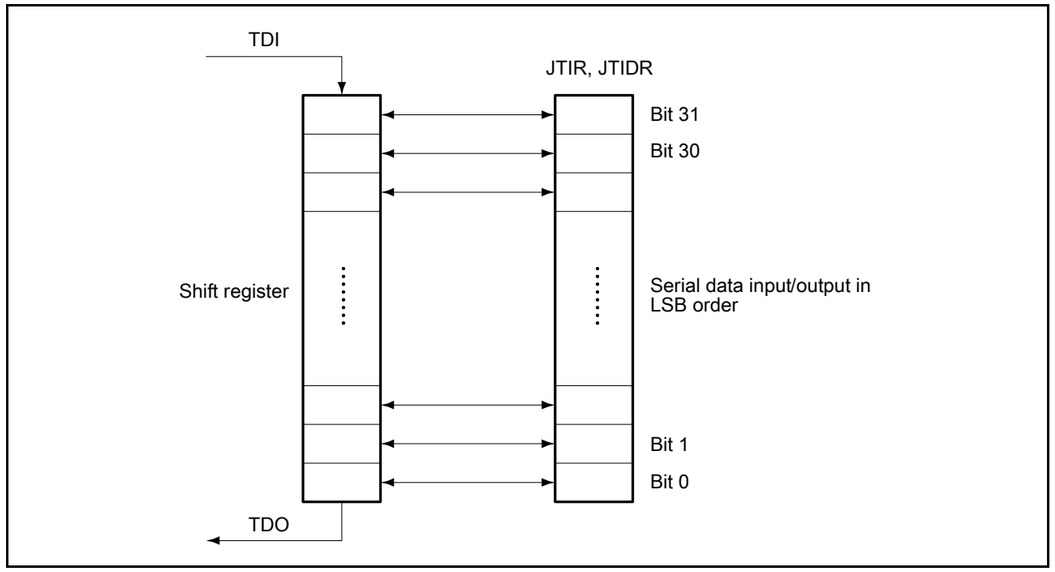


Figure 45.3 Serial data input/output

The following pins cannot be boundary-scanned:

- Power supply pins (VCC, VCL, VCL0, VSS, VBATT, AVCC0, AVSS0, VCC_USB, VSS_USB, AVCC_USBHS, AVSS_USBHS, PVSS_USBHS, VCC_USBHS VSS1_USBHS, and VSS2_USBHS) cannot be boundary-scanned
- Analog reference pins (VREFH0, VREFL0, VREFH, VREFL, USBHS_RREF) cannot be boundary-scanned
- Clock pins (EXTAL, XTAL, XCIN, and XCOUT) cannot be boundary-scanned
- Reset signal (RES) cannot be boundary-scanned
- USB-dedicated pins (USB_DP, USB_DM, USBHS_DP, USBHS_DM) cannot be boundary-scanned
- The boundary-scan pins (TCK, TMS, TDI, and TDO) cannot be boundary-scanned.

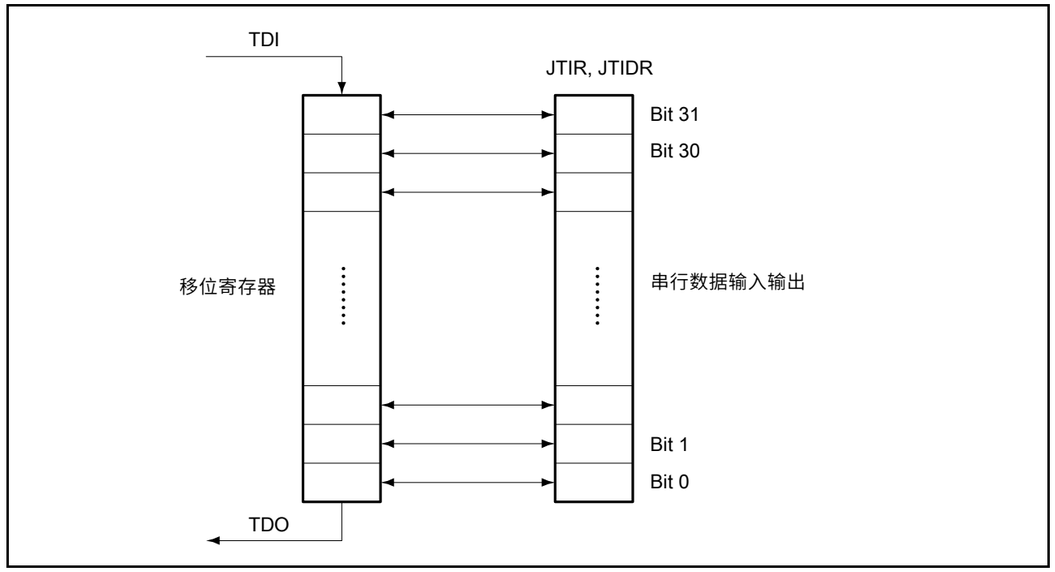


Figure 45.3 串行数据输入输出

以下引脚不能进行边界扫描：

- 电源引脚（VCC、VCL、VCL0、VSS、VBATT、AVCC0、AVSS0、VCC_USB、VSS_USB、AVCC_USBHS、AVSS_USBHS、PVSS_USBHS、VCC_USBHSVSS1_USBHS和VSS2_USBHS）不能进行边界扫描
- 模拟参考引脚（VREFH0、VREFL0、VREFH、VREFL、USBHS_RREF）不能进行边界扫描
- 时钟引脚（EXTAL、XTAL、XCIN和XCOUT）不能进行边界扫描
- 复位信号(RES)不能进行边界扫描
- USB专用引脚（USB_DP、USB_DM、USBHS_DP、USBHS_DM）不能进行边界扫描
- 边界扫描引脚（TCK、TMS、TDI和TDO）不能进行边界扫描。

46. Secure Cryptographic Engine (SCE7)

The MCU incorporates a Secure Cryptographic Engine (SCE7) module to provide security functions. The module consists of an access management circuit, encryption engine, and random number generator.

46.1 Overview

Table 46.1 shows the SCE7 specifications and Figure 46.1 shows the SCE7 block diagram.

Table 46.1 SCE7 specifications (1 of 2)

Parameter	Description
Access control	Access management circuit • In case of irregular access to the SCE7 due to a falsified program or runaway execution of a program, this circuit blocks all subsequent access and stops the output of data from the SCE7.
Encryption engine	Advanced Encryption Standard (AES): Compliant with NIST FIPS PUB 197 algorithm • Key sizes: 128, 192, or 256 bits • Block size: 128 bits • Chaining modes - ECB, CBC, CTR: Compliant with NIST SP 800-38A - GCM: Compliant with NIST SP 800-38D - XTS: Compliant with NIST SP 800-38E - GCTR. • Throughput for 128-bit data - 11 PCLKB cycles for 128-bit key - 15 PCLKB cycles for 256-bit key. AES-GCM • AES-GCM is realized by combining AES-GCTR and GHASH. Triple Data Encryption Standard (3DES): • 168-bit key length • Operates on a fixed 8-byte block of data • Used in legacy Secure Socket Layer (SSL) and Transport Layer Security (TLS) protocols • Throughput for 64-bit data - 16 PCLKB cycles for 56-bit key. Alleged RC4 (ARC4) • 2048-bit key length • Throughput for 128-bit data - 16 PCLKB cycles for 2048-bit key. Key management • Wrapped keys are only valid within the SCE7.
Generation of random numbers	128-bit true random number generator
Signature generation and verification	RSA • Support for 1024-bit and 2048-bit key sizes • Signature generation, signature verification, public-key encryption, private-key decryption. DSA • Support for DSA key sizes: • (1024-bit, 160-bit) • (2048-bit, 224-bit) • (2048-bit, 256-bit). • Signature generation, signature verification. ECC • Support for curve P-192, P-224, P-256, and P-384 • Signature generation, signature verification • Scalar multiplication.
Message digest computation	HASH • SHA1, SHA224, SHA256, and MD5.

46. 安全加密引擎(SCE7)

MCU包含一个安全加密引擎(SCE7)模块以提供安全功能。该模块由访问管理电路、加密引擎和随机数发生器组成。

46.1 Overview

表46.1显示了SCE7规范，图46.1显示了SCE7框图。

Table 46.1 SCE7规范（2个中的1个）

Parameter	Description
访问控制	访问管理电路 如果由于伪造程序或程序执行失控导致对SCE7的非正常访问，该电路将阻止所有后续访问，并停止从SCE7输出数据。
加密引擎	高级加密标准(AES)：符合NISTFIPSPUB197算法 密钥大小：128、192或256位 块大小：128位 链接模式 ECB、CBC、CTR：符合NISTSP800-38AGCM：符合NISTSP800-38DXTS：符合NISTSP800-38EGCTR。 128位数据的吞吐量 128位密钥的11个PCLKB周期256位密钥的15个PCLKB周期。 AES-GCM AES-GCM是通过结合AES-GCTR和GHASH实现的。 三重数据加密标准(3DES)：•1个68位密钥长度•对固定的8字节数据块进行操作•用于传统安全套接字层(SSL)和传输层安全(TLS)协议•64位吞吐量数据 56位密钥的16个PCLKB周期。 所谓的RC4(ARC4) 2048位密钥长度 128位数据的吞吐量 2048位密钥的16个PCLKB周期。 密钥管理 封装的密钥仅在SCE7内有效。
随机数的产生	128位真随机数发生器
签名生成和验证	RSA 支持1024位和2048位密钥大小 签名生成、签名验证、公钥加密、私钥解密。 DSA 支持DSA密钥大小： （1024位、160位） （2048位、224位） （2048位、256位）。签名生成、签名验证。 ECC 支持曲线P-192、P-224、P-256和P-384 签名生成、签名验证 标量乘法。
消息摘要计算	哈希 SHA1、SHA224、SHA256和MD5。

Table 46.1 SCE7 specifications (2 of 2)

Parameter	Description
Unique ID	• A unique ID to the MCU, is accessible from the access management circuit through the dedicated bus • Combining the unique ID with the key generation information prevents the illicit copying of data to another MCU.
Low power consumption	Setting of the module stop state is possible.

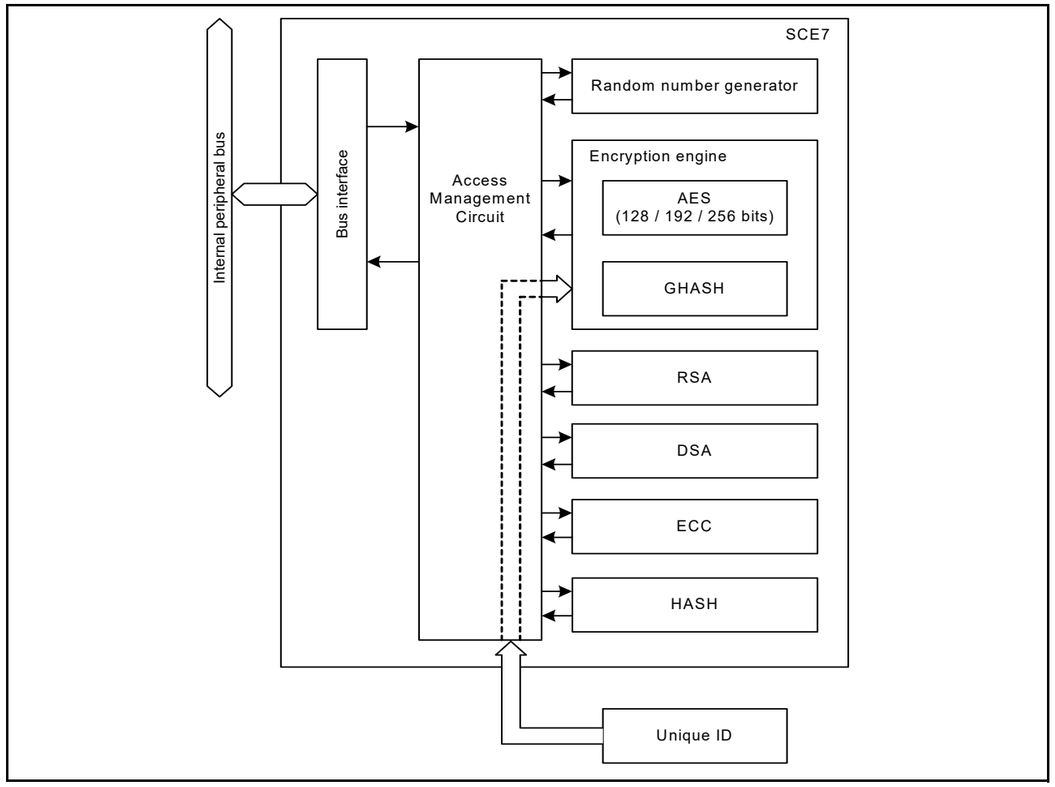


Figure 46.1 SCE7 block diagram

46.2 Operation

46.2.1 Encryption Engine

The encryption engine performs the following operation in hardware, see Figure 46.2:

- Plaintext to ciphertext encryption
- Ciphertext to plaintext decryption.

Table 46.1 SCE7规范（2个中的2个）

Parameter	Description
唯一身份	MCU的唯一ID，可通过专用总线从访问管理电路访问。 将唯一ID与密钥生成信息相结合可防止将数据非法复制到另一个MCU。
低功耗	可以设置模块停止状态。

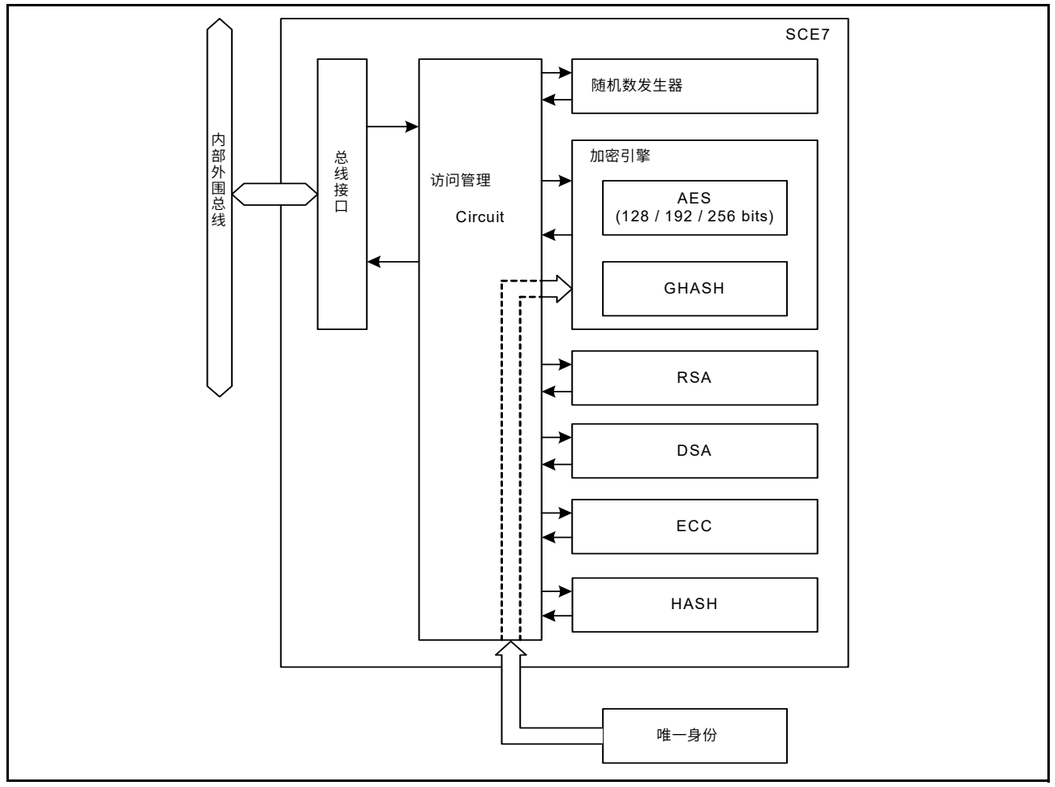


Figure 46.1 SCE7框图

46.2 Operation

46.2.1 加密引擎

加密引擎在硬件中执行以下操作，见图46.2：

- 明文到密文加密
- 密文转明文解密。

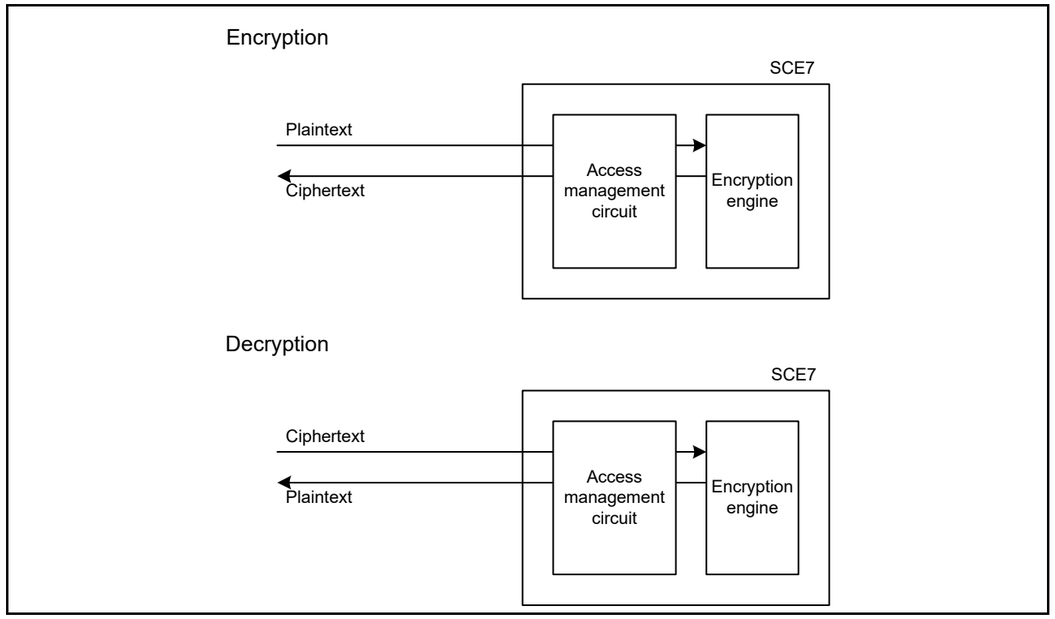


Figure 46.2 Encryption and decryption processes by encryption engine

46.2.2 Encryption and Decryption

To encrypt or decrypt data:

1. Input the data to encrypt or decrypt in the SCE7. The SCE7 converts the plaintext data to ciphertext or ciphertext data to plaintext.
2. Read the converted data.

The encryption engine has an input buffer and an output buffer, enabling encryption/decryption to proceed in parallel with data input/output. Figure 46.3 shows the encryption engine timing.

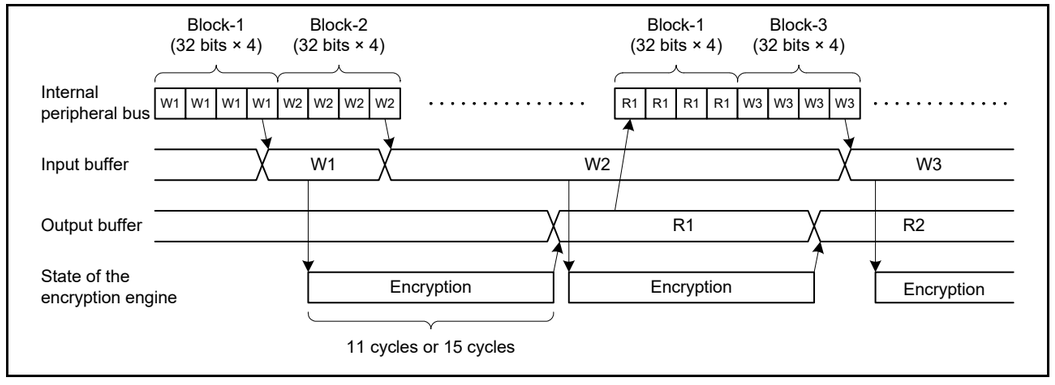


Figure 46.3 Encryption and decryption timing (AES)

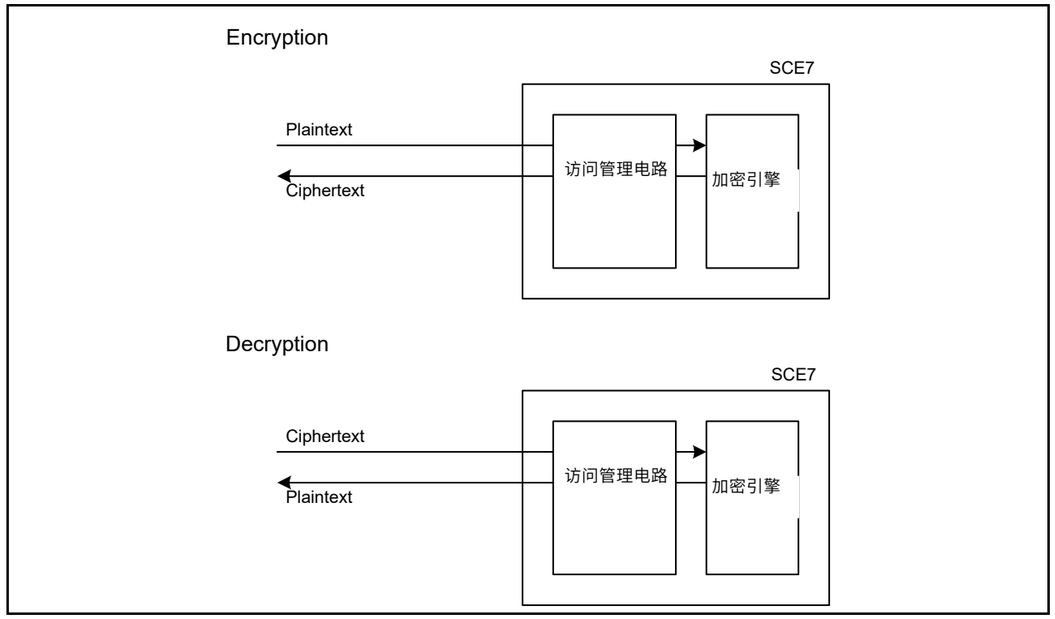


Figure 46.2 加密引擎的加解密过程

46.2.2 加密和解密

要加密或解密数据：

1. 在SCE7中输入要加密或解密的数据。SCE7将明文数据转换为密文或将密文数据转换为明文。
2. 读取转换后的数据。

加密引擎有一个输入缓冲区和一个输出缓冲区，使加密解密与数据输入输出并行进行。图46.3显示了加密引擎的时序。

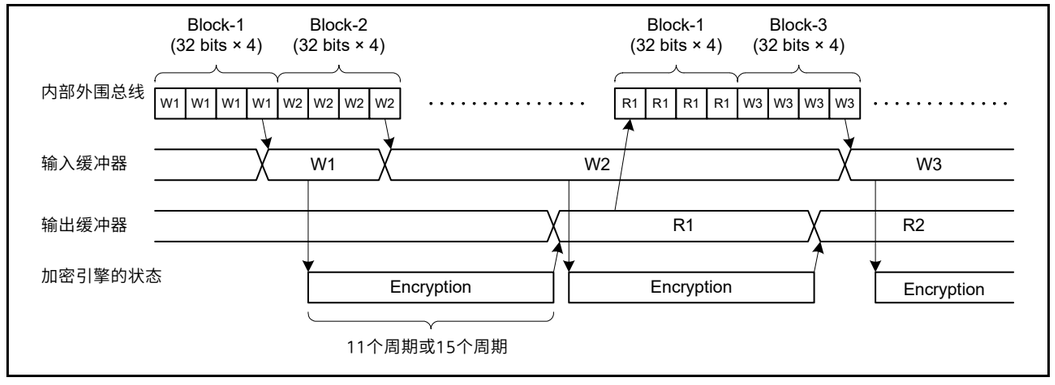


Figure 46.3 加密和解密时序（AES）

46.3 Usage Notes

46.3.1 Software Standby Mode

When Software Standby mode is entered while the encryption engine is in processing, proper processing cannot be resumed after exiting Software Standby mode. Software Standby mode should therefore be entered while the encryption engine is not running.

46.3.2 Settings for the Module-Stop Function

The Module Stop Control Register C (MSTPCRC) can enable or disable SCE7 operation. The SCE7 module is initially stopped after reset. Releasing the module-stop state enables access to the registers.

46.3 使用说明

46.3.1 软件待机模式

当加密引擎正在处理时进入软件待机模式时，退出软件待机模式后无法恢复正常处理。因此，应在加密引擎未运行时进入软件待机模式。

46.3.2 模块停止功能的设置

模块停止控制寄存器C(MSTPCRC)可以启用或禁用SCE7操作。SCE7模块在复位后最初停止。释放模块停止状态可以访问寄存器。

47. 12-Bit A/D Converter (ADC12)

47.1 Overview

The MCU provides two 12-bit successive approximation A/D converter (ADC12) units. In unit 0, up to 13 analog input channels, temperature sensor output, and internal reference voltage are selectable for conversion. In unit 1, up to 11 analog input channels, temperature sensor output, and internal reference voltage are selectable for conversion. The A/D conversion accuracy is selectable from 12-, 10-, and 8-bit conversion, making it possible to optimize the trade-off between speed and resolution in generating a digital value.

ADC12 features include:

- 13 channels (unit 0), 11 channels (unit 1)
- PCLKB = 60 MHz (maximum)
- PCLKC = 60 MHz (maximum)
- Analog channels: AN000 to AN007, AN016 to AN020 (unit 0), AN100 to AN103, AN105 to AN107, AN116 to AN119 (unit 1)
- Resolution: 12-bit, 10-bit, 8-bit
- Dedicated sample-and-hold circuit embedded
- Programmable Gain Amplifier embedded.

The ADC12 supports the following operating modes:

- Single scan mode for converting the analog inputs of arbitrarily selected channels in ascending order of channel number
- Continuous scan mode for sequentially converting analog inputs of arbitrarily selected channels continuously in ascending order of channel number
- Group scan mode for arbitrarily dividing analog inputs of channels into two groups (A and B) and converting the analog input of the selected channel for each group in ascending order of channel number.

In group scan mode, you can start Group A and Group B A/D conversion at different times by individually selecting their scan start conditions. In addition, when a priority control operation for Group A is set, the ADC12 accepts Group A scan starting during Group B A/D conversion, suspending Group B conversion. This allows you to assign higher priority to A/D conversion start for Group A.

In double-trigger mode, the analog input of an arbitrarily selected channel is converted in single scan mode or group scan mode (Group A), and data converted by the first and second A/D conversion start triggers are stored in different registers, providing duplexing of A/D-converted data.

Self-diagnosis is performed once at the beginning of each scan, and one of the three voltage values generated in the ADC12 is A/D-converted.

The temperature sensor output and the internal reference voltage are selectable at the same time as the analog input of the channel. First A/D conversion is performed for the analog input of the channel, next the temperature sensor output, and then the internal reference voltage.

The ADC12 provides a compare function (Window A and Window B). This compare function specifies the upper reference value for Window A and lower reference value for Window B, and outputs an interrupt request when the A/D-converted value of the selected channel meets the comparison conditions.

Table 47.1 lists the ADC12 specifications and Table 47.2 list the functions. Figure 47.1 shows a block diagram of ADC12 unit 0 and Figure 47.2 shows a block diagram of ADC12 unit 1. Table 47.3 lists the I/O pins.

Table 47.1 ADC12 specifications (1 of 3)

Parameter	Specifications
Number of units	Two units, 0 and 1

47. 12-Bit A/D Converter (ADC12)

47.1 Overview

MCU提供两个12位逐次逼近模数转换器(ADC12)单元。在单元0中，可以选择最多13个模拟输入通道、温度传感器输出和内部参考电压进行转换。在单元1中，可以选择多达11个模拟输入通道、温度传感器输出和内部参考电压进行转换。AD转换精度可从12位、10位和8位转换中选择，从而可以在生成数字值时优化速度和分辨率之间的权衡。

ADC12 features include:

- 13 channels (unit 0), 11 channels (unit 1)
- PCLKB = 60 MHz (maximum)
- PCLKC = 60 MHz (maximum)
- 模拟通道：AN000到AN007、AN016到AN020（单元0）、AN100到AN103、AN105到AN107、AN116到AN119 (unit 1)
- Resolution: 12-bit, 10-bit, 8-bit
- 嵌入式专用采样保持电路
- 嵌入式可编程增益放大器。

ADC12支持以下工作模式：

- 单次扫描模式，以通道号升序转换任意选择通道的模拟输入
- 连续扫描模式，用于按通道编号升序连续转换任意选择通道的模拟输入
- 组扫描模式，用于将通道的模拟输入任意分成两组（A和B），并按通道编号的升序转换每组所选通道的模拟输入。

在组扫描模式下，您可以通过单独选择它们的扫描开始条件，在不同的时间开始A组和B组AD转换。此外，当设置A组的优先控制操作时，ADC12在B组AD转换期间接受A组扫描，暂停B组转换。这允许您为A组的AD转换开始分配更高的优先级。

双触发模式下，任意选择通道的模拟输入转换为单扫描模式或组扫描模式（A组），第一次和第二次A/D转换启动触发转换的数据存储在不同的寄存器中，提供双工一个D转换数据。

自诊断在每次扫描开始时执行一次，并在生成的三个电压值之一
ADC12 is A/D-converted.

温度传感器输出和内部参考电压可与通道的模拟输入同时选择。首先对通道的模拟输入进行AD转换，然后是温度传感器输出，然后是内部参考电压。

ADC12提供比较功能（窗口A和窗口B）。该比较函数指定窗口A的上参考值和窗口B的下参考值，并在所选通道的AD转换值满足比较条件时输出中断请求。

表47.1列出了ADC12规格，表47.2列出了功能。图47.1显示了一个框图
ADC12单元0和图47.2显示了ADC12单元1的框图。表47.3列出了IO引脚。

Table 47.1 ADC12规格(1of3)

Parameter	Specifications
单位数量	两个单位，0和1

Table 47.1 ADC12 specifications (2 of 3)

Parameter	Specifications
Input channels	• Unit 0: Up to 13 channels • Unit 1: Up to 11 channels
Extended analog function	Temperature sensor output, internal reference voltage
A/D conversion method	Successive approximation method
Resolution	12 bits, selectable to 12-bit, 10-bit, or 8-bit conversion
Conversion time	0.4 µs/channel, when A/D conversion clock PCLKC (ADCLK) is operating at 60 MHz (See Table 60.40 and Table 60.41 about the condition)
A/D conversion clock	Peripheral module clock PCLKB*1 and A/D conversion clock PCLKC (ADCLK)*1 can be set with the following division ratios: PCLKB to PCLKC (ADCLK) frequency ratios = 1:1, 2:1, 4:1, 8:1, 1:2, 1:4
Data registers	• 24 registers for analog input (13 for unit 0, 11 for unit 1), one for A/D-converted data duplication in double-trigger mode in each unit, and 2 for A/D-converted data duplication in extended operation in double-trigger mode in each unit • One register for temperature sensor output • One register for internal reference voltage • One register for self-diagnosis • Storing of A/D conversion results in A/D data registers • 8-, 10-, and 12-bit accuracy output for A/D conversion results • A/D-converted value addition mode, in which the sum of all A/D conversion results are stored in the in the A/D data registers as the conversion accuracy bit count + 2 bits.*4 • Double-trigger mode (selectable in single scan and group scan modes): The first unit of A/D-converted analog-input data on one selected channel is stored in the data register for the channel, and the second unit is stored in the duplexing register. • Extended operation in double-trigger mode (available for specific triggers): A/D-converted analog-input data on one selected channel is stored in the duplexing register provided for the associated trigger
Operating modes	• Single scan mode: - A/D conversion is performed only once on the analog inputs of arbitrarily selected channels, on the temperature sensor output, and on the internal reference voltage. • Continuous scan mode: - A/D conversion is performed repeatedly on the analog inputs of arbitrarily selected channels, on the temperature sensor output, and on the internal reference voltage. • Group scan mode: - Analog inputs of arbitrarily selected channels, the temperature sensor output, and the internal reference voltage are divided into Group A and Group B, and A/D conversion of the analog input selected on a group basis is performed only once. - The scan start conditions can be independently selected for Group A and Group B, allowing A/D conversion of Group A and Group B to be started independently. • Group scan mode (when Group A is given priority): - If a Group A trigger is input during A/D conversion on Group B, the A/D conversion on Group B stops and A/D conversion is processed on Group A. - Restart (rescan) of Group B conversion after completion of Group A conversion can be set.
Conditions for A/D conversion start	• Software trigger • Synchronous triggers from the Event Link Controller (ELC). • Asynchronous triggering by the external trigger pins, ADTRG0 (unit 0) and ADTRG1 (unit 1)
Functions	• Dedicated sample-and-hold function with optional constant sampling and 3 channels in units 0 and 1 • Variable sampling state count • Self-diagnosis of ADC12 • Selectable A/D-converted value addition mode or average mode • Analog input disconnection detection function (discharge and precharge functions) • Double-trigger mode (duplication of A/D conversion data) • Switching function for 8-, 10-, and 12-bit conversion*2 • Automatic clear function for A/D data registers • Digital comparison of values in the comparison and data registers, and between values in the data registers
Programmable gain amplifier	• Amplification of analog input signals to enable A/D conversion, with 3 channels in units 0 and 1 • Compatible with single-ended input and differential input

Table 47.1 ADC12规格（2个，共3个）

Parameter	Specifications
输入通道	单元0：最多13个通道 单元1：最多11个通道
扩展模拟功能	温度传感器输出，内部参考电压
AD转换方式	逐次逼近法
Resolution	12位，可选择12位、10位或8位转换
转换时间	0.4µs通道，当AD转换时钟PCLKC(ADCLK)以60MHz运行时（有关条件，请参见表60.40和表60.41）
AD转换时钟	外围模块时钟PCLKB*1和AD转换时钟PCLKC(ADCLK)*1可设置为以下分频比：PCLKB与PCLKC(ADCLK)频率比=1:1、2:1、4:1、8:1、1:2 1:4
数据寄存器	24个用于模拟输入的寄存器（13个用于单元0，11个用于单元1），一个用于双触发模式下的AD转换数据复制，以及双触发模式下扩展操作中的AD转换数据复制每个单元中 一个用于温度传感器输出的寄存器 一个用于内部参考电压的寄存器 一个用于自诊断的寄存器 将AD转换结果存储在AD数据寄存器中 用于AD转换的8位、10位和12位精度输出结果 AD转换值加法模式，其中所有AD转换结果的总和作为转换精度位数+2位存储在AD数据寄存器中。*4 双触发模式（在单次扫描中可选和组扫描模式）： 一个选定通道上的AD转换模拟输入数据的第一个单元存储在该通道的数据寄存器中，第二个单元存储在双工寄存器中。 双触发模式下的扩展操作（适用于特定触发）： 一个选定通道上的D转换模拟输入数据存储在为相关触发提供的双工寄存器中
操作模式	单次扫描模式： D转换仅在任意选择通道的模拟输入、温度传感器输出和内部参考电压上执行一次。 连续扫描模式： 对任意选择通道的模拟输入、温度传感器输出和内部参考电压重复执行D转换。 组扫描模式： 任意选择通道的模拟输入、温度传感器输出、内部参考电压分为A组和B组，按组选择的模拟输入只进行一次A/D转换。可以独立选择A组和B组的扫描开始条件，允许A组和B组的AD转换独立启动。 组扫描模式（当A组优先时）： 如果在B组的AD转换期间输入A组触发，则B组的AD转换将停止，并在A组进行AD转换。可以设置A组转换完成后B组转换的重新启动（重新扫描）。
AD转换开始的条件	软件触发器 来自事件链接控制器(ELC)的同步触发器。 通过外部触发引脚ADTRG0（单元0）和ADTRG1（单元1）进行异步触发
Functions	专用采样保持功能，可选恒定采样和3个通道，单元0和1 可变采样状态计数 ADC12自诊断 可选择AD转换值加法模式或平均模式 模拟输入断开检测功能（放电和预充电功能） 双触发模式（AD转换数据的复制） 8位、10位和12位转换的切换功能*2 AD数据寄存器的自动清除功能 比较中的值的数字比较和数据寄存器，以及数据寄存器中的值之间
可编程增益放大器	放大模拟输入信号以实现AD转换，单元0和1具有3个通道 兼容单端输入和差分输入

Table 47.1 ADC12 specifications (3 of 3)

Parameter	Specifications
Interrupt sources and ELC events	• ADC12i_ADI: A/D scan end interrupt • ADC12i_GBADI: A/D scan end interrupt for Group B • ADC12i_CMPAI: Window A compare match • ADC12i_CMPBI: Window B compare match • ADC12i_WCMPM: compare match • ADC12i_WCMPUM: compare mismatch
ELC interface	Scan can be started by a trigger from the ELC
Bus interface	Bus clock synchronized with peripheral clock (PCLKB), maximum frequency = 60 MHz
Reference voltage	• Unit 0: VREFH0 is the high potential reference voltage. VREFL0 is the low potential reference voltage. • Unit 1: VREFH is the high potential reference voltage. VREFL is the low potential reference voltage.
Module-stop function	Module-stop state can be set to reduce power consumption*3

i = 0 for unit 0, and i = 1 for unit 1.

Note 1. Peripheral module clock PCLKB is specified in the SCKDIVCR.PCKB[2:0] bits, and A/D conversion clock ADCLK in the SCKDIVCR.PCKC[2:0] bits in units 0 and 1.
Note 2. Changing the A/D conversion accuracy also changes the A/D conversion time. For details, see section 47.3.6, Analog Input Sampling and Scan Conversion Time.
Note 3. For details, see section 11, Low Power Modes.
Note 4. The number of extended bits for addition varies with the A/D conversion accuracy and the number of addition times. A 2-bit extension is up to 4 times conversion (3 times addition) when the A/D conversion accuracy is 8, 10, or 12 bits. A 4-bit extension is 16 times conversion (15 times addition) when the A/D conversion accuracy is 12 bits.

Table 47.2 ADC12 functions

Parameter			Unit 0 (ADC120)	Unit 1 (ADC121)
Analog input channel			AN000 to AN007, AN016 to AN020 Internal reference voltage Temperature sensor output	AN100 to AN103, AN105 to AN107, AN116 to AN119 Internal reference voltage Temperature sensor output
Conditions for A/D conversion start	Software	Software trigger	Enabled	Enabled
	External trigger	Trigger input pin	ADTRG0	ADTRG1
	Synchronous trigger (trigger from ELC)	ELC trigger	ELC_AD00, ELC_AD01	ELC_AD10, ELC_AD11
Channel-dedicated sample-and-hold function	Target channel		AN000 to AN002	AN100 to AN102
Programmable gain amplifier	Target channel		AN000 to AN002	AN100 to AN102
	Differential input pin		PGAVSS000	PGAVSS100
Interrupt			ADC120_ADI ADC120_GBADI ADC120_CMPAI ADC120_CMPBI	ADC121_ADI ADC121_GBADI ADC121_CMPAI ADC121_CMPBI
Output to ELC			ADC120_ADI ADC120_WCMPM ADC120_WCMPUM	ADC121_ADI ADC121_WCMPM ADC121_WCMPUM
Module-stop function settings*1, *2			MSTPCRD.MSTPD16 bit	MSTPCRD.MSTPD15 bit

Note 1. For details, see section 11, Low Power Modes.
Note 2. Wait for 1 µs or longer to start A/D conversion after release from the module-stop state.

Table 47.1 ADC12规格（3个中的3个）

Parameter	Specifications
中断源和 ELC events	ADC12i_ADI：D扫描结束中断 ADC12i_GBADI：B组的D扫描结束中断 ADC12i_CMPAI：窗口A比较匹配 ADC12i_CMPBI：窗口B比较匹配 ADC12i_WCMPM：比较匹配 ADC12i_WCMPUM：比较不匹配
ELC interface	扫描可以通过来自ELC的触发器启动
总线接口	与外设时钟(PCLKB)同步的总线时钟，最大频率=60MHz
参考电压	• Unit 0: VREFH0是高电位参考电压。VREFL0是低电位参考电压。 单元1： VREFH是高电位参考电压。VREFL是低电位参考电压。
Module-stop function	可设置模块停止状态以降低功耗*3

对于单元0，i=0，对于单元1，i=1。

Note 1. 外围模块时钟PCLKB在SCKDIVCR.PCKB[2:0]位中指定，AD转换时钟ADCLK在SCKDIVCR.PCKC[2:0]位在单元0和1中。
Note 2. 改变AD转换精度也会改变AD转换时间。有关详细信息，请参阅第47.3.6节，模拟输入采样和扫描转换时间。
Note 3. 有关详细信息，请参阅第11节，低功耗模式。
Note 4. 加法的扩展位数随AD转换精度和加法次数而变化。当AD转换精度为8、10或12位时，2位扩展最多可进行4次转换（3次加法）。当AD转换精度为12位时，4位扩展是16次转换（15次加法）。

Table 47.2 ADC12 functions

Parameter			Unit 0 (ADC120)	Unit 1 (ADC121)
模拟输入通道			AN000至AN007、AN016至AN020内部参考电压温度传感器输出	AN100 to AN103, AN105 to AN107, AN116 to AN119 内部参考电压温度传感器输出
AD转换开始的条件	Software	软件触发	Enabled	Enabled
	外部触发	触发输入引脚	ADTRG0	ADTRG1
	同步触发（来自ELC的触发）	ELC trigger	ELC_AD00, ELC_AD01	ELC_AD10, ELC_AD11
Channel-dedicated sample-and-hold function	目标渠道		AN000 to AN002	AN100 to AN102
可编程增益放大器	目标渠道		AN000 to AN002	AN100 to AN102
	差分输入引脚		PGAVSS000	PGAVSS100
Interrupt			ADC120_ADI ADC120_GBADI ADC120_CMPAI ADC120_CMPBI	ADC121_ADI ADC121_GBADI ADC121_CMPAI ADC121_CMPBI
输出到ELC			ADC120_ADI ADC120_WCMPM ADC120_WCMPUM	ADC121_ADI ADC121_WCMPM ADC121_WCMPUM
Module-stop function settings*1, *2			MSTPCRD.MSTPD16 bit	MSTPCRD.MSTPD15 bit

Note 1. 有关详细信息，请参阅第11节，低功耗模式。
Note 2. 从模块停止状态释放后，等待1µs或更长时间开始AD转换。

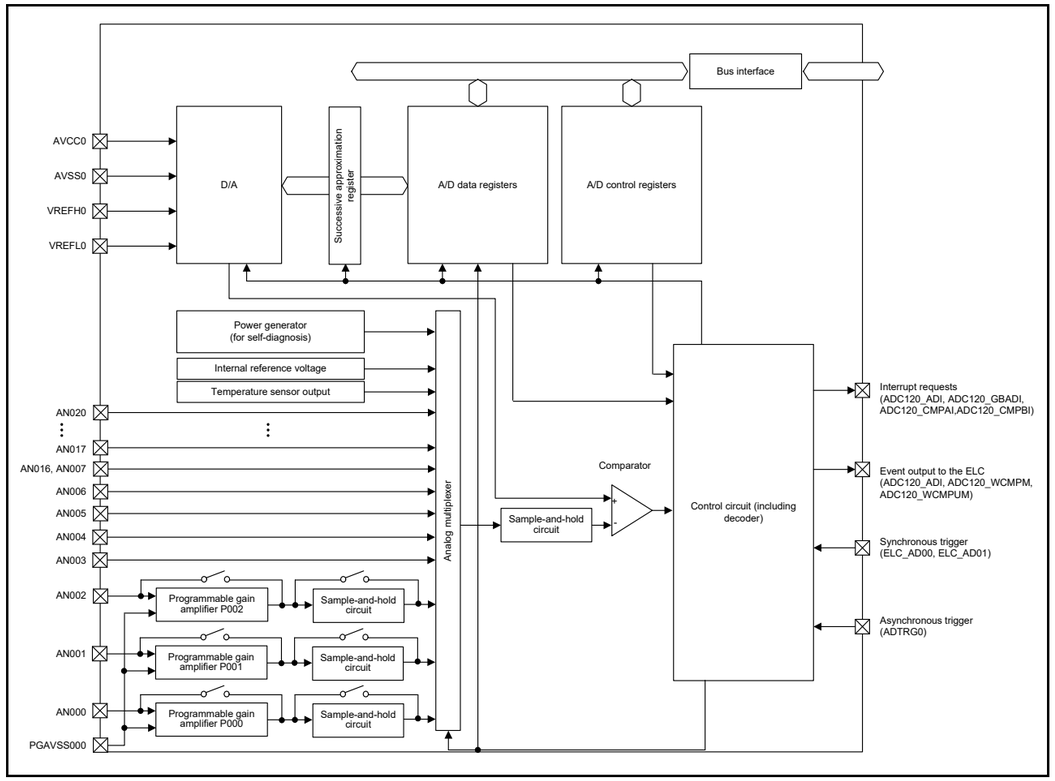


Figure 47.1 ADC12 unit 0 block diagram

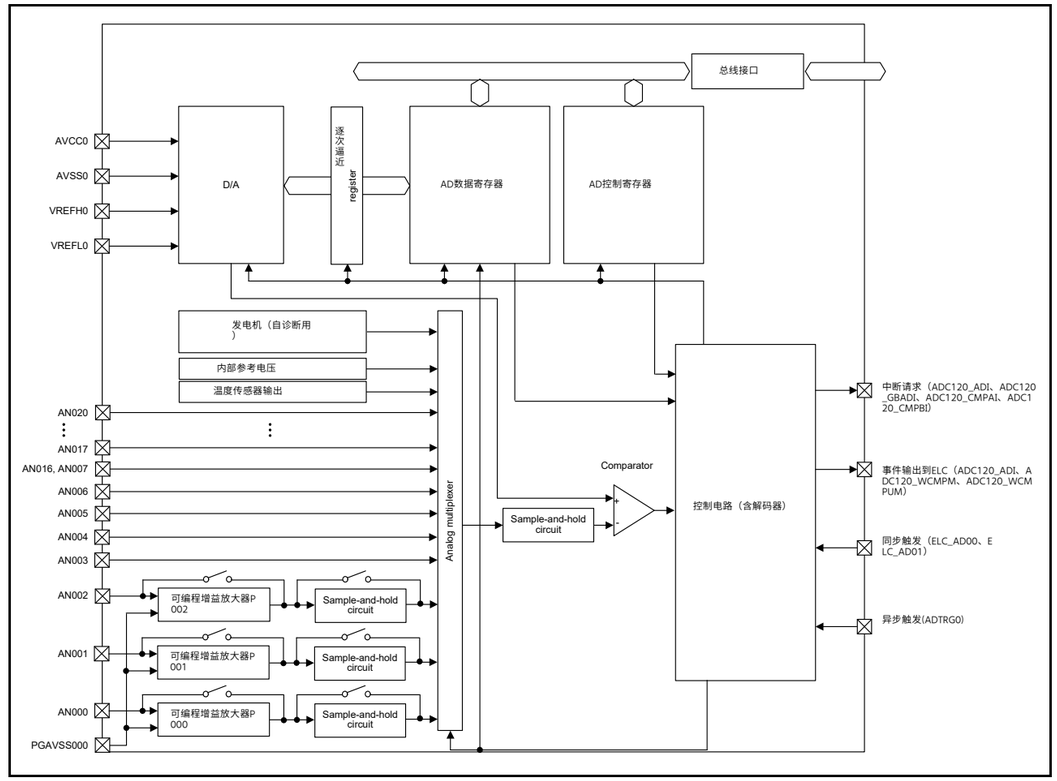


Figure 47.1 ADC12单元0框图

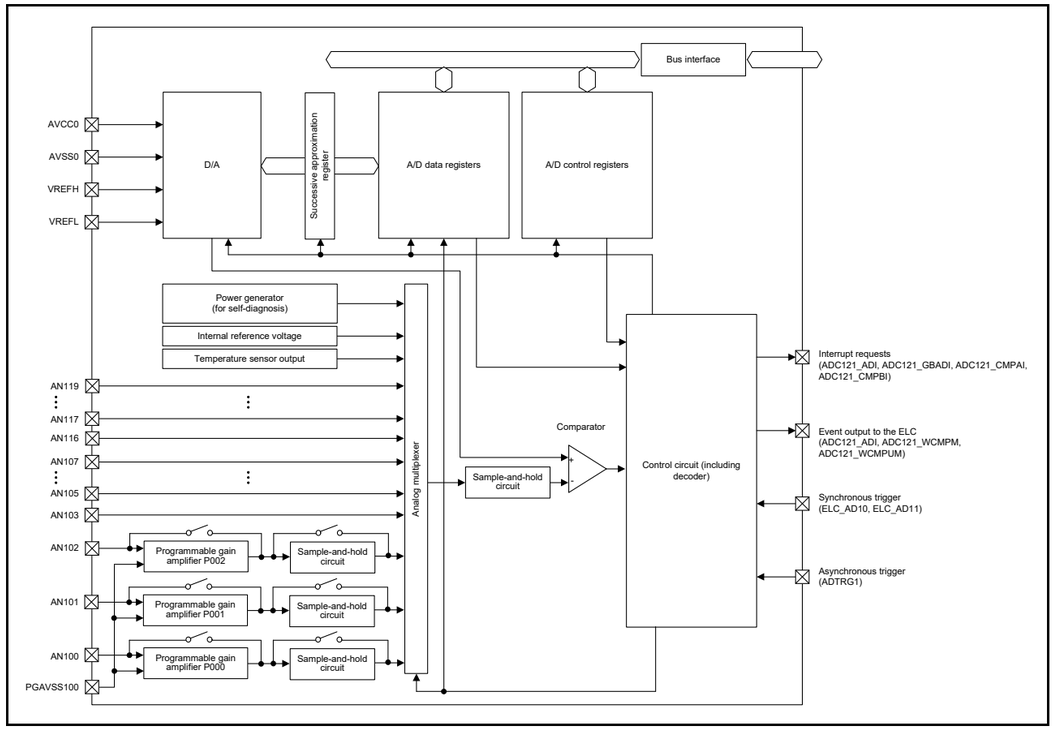


Figure 47.2 ADC12 unit 1 block diagram

Table 47.3 ADC12 I/O pins

Unit	Pin name	I/O	Function
Unit 0	AVCC0	Input	Analog block power supply pin
	AVSS0	Input	Analog block power supply ground pin
	VREFH0	Input	Reference power supply pin
	VREFL0	Input	Reference power supply ground pin
	AN000 to AN007, AN016 to AN020	Input	Analog input pins 0 to 7 and 16 to 20
	ADTRG0	Input	External trigger input pin for starting A/D conversion, active low
	PGAVSS000	Input	Differential input pin
Unit 1	AVCC0	Input	Analog block power supply pin
	AVSS0	Input	Analog block power supply ground pin
	VREFH	Input	Reference power supply pin for ADC12 unit 1 and DAC
	VRELF	Input	Reference power supply ground pin for ADC12 unit 1 and DAC
	AN100 to AN103, AN105 to AN107, AN116 to AN119	Input	Analog input pins 0 to 3, 5 to 7, and 16 to 19
	ADTRG1	Input	External trigger input pin for starting A/D conversion, active low
	PGAVSS100	Input	Differential input pin

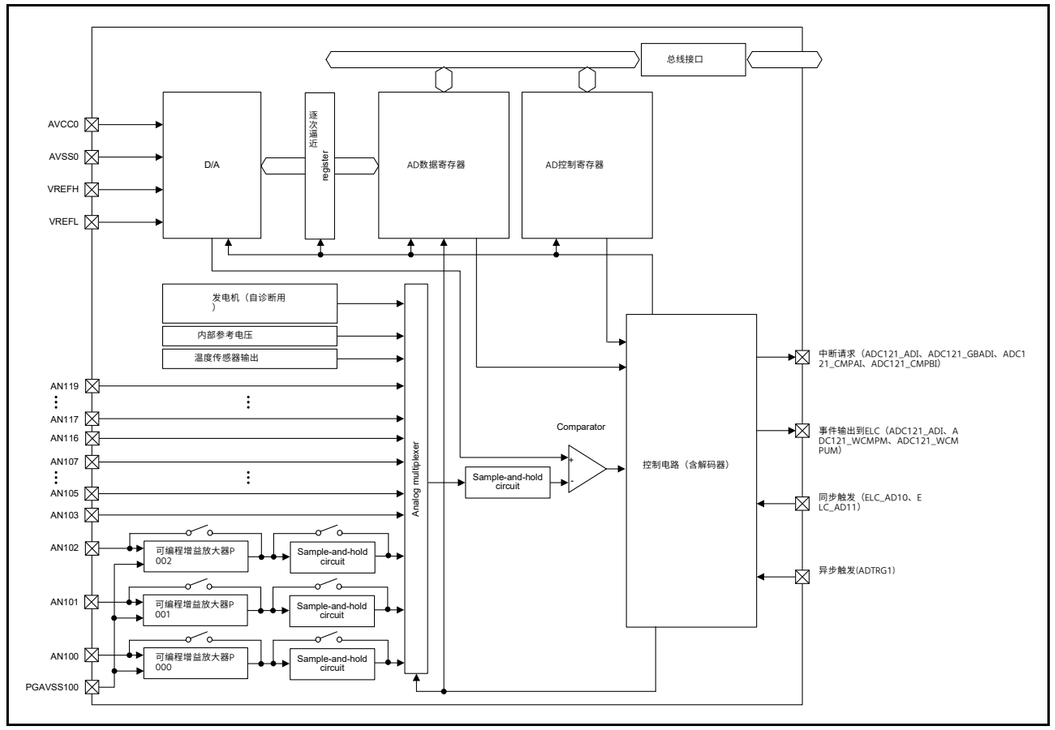


Figure 47.2 ADC12单元1框图

Table 47.3 ADC12 I/O pins

Unit	引脚名称	I/O	Function
Unit 0	AVCC0	Input	模拟模块电源引脚
	AVSS0	Input	模拟模块电源接地引脚
	VREFH0	Input	参考电源引脚
	VREFL0	Input	参考电源接地引脚
	AN000 to AN007, AN016 to AN020	Input	模拟输入引脚0到7和16到20
	ADTRG0	Input	用于启动AD转换的外部触发输入引脚，低电平有效
	PGAVSS000	Input	差分输入引脚
Unit 1	AVCC0	Input	模拟模块电源引脚
	AVSS0	Input	模拟模块电源接地引脚
	VREFH	Input	ADC12单元1和DAC的参考电源引脚
	VRELF	Input	ADC12单元1和DAC的参考电源接地引脚
	AN100 to AN103, AN105 to AN107, AN116 to AN119	Input	模拟输入引脚0至3、5至7和16至19
	ADTRG1	Input	用于启动AD转换的外部触发输入引脚，低电平有效
	PGAVSS100	Input	差分输入引脚

47.2 Register Descriptions

47.2.1 A/D Data Registers y (ADDRy), A/D Data Duplexing Register (ADDBLDR), A/D Data Duplexing Register A (ADDBLDRA), A/D Data Duplexing Register B (ADDBLDRB), A/D Temperature Sensor Data Register (ADTSDR), A/D Internal Reference Voltage Data Register (ADOCDR)

The data registers include:

- ADDRy registers (y = 0 to 7, 16 to 20 in unit 0 and y = 0 to 3, 5 to 7, 16 to 19 in unit 1): 16-bit read-only registers for storing the A/D conversion results
- ADDBLDR register: 16-bit read-only register for storing the A/D conversion results in response to the second trigger in double-trigger mode
- ADDBLDRA and ADDBLDRB registers: 16-bit read-only registers for storing the A/D conversion results in response to the respective triggers during extended operation in double-trigger mode
- ADTSDR register: 16-bit read-only register for storing the A/D conversion result of the temperature sensor output
- ADOCDR register: 16-bit read-only register for storing the A/D result of the internal reference voltage.

The following conditions determine the formats for data in these registers:

- The setting in the A/D Data Register Format Select bit (ADCER.ADRFMT) (flush-left or flush-right setting)
- The setting in the A/D Conversion Accuracy Specify bits (ADCER.ADPRC[1:0]) (8-, 10-, or 12-bit setting).

This section describes the data formats for these conditions in different modes.

(1) When A/D-converted value addition/average mode is not selected

The data formats for each condition are as follows:

Settings for flush-right data with 12-bit accuracy

Address(es): ADC120.ADDR0 4005 C020h to ADC120.ADDR7 4005 C02Eh, ADC120.ADDR16 4005 C040h to ADC120.ADDR20 4005 C048h, ADC120.ADDBLDR 4005 C018h, ADC120.ADDBLDRA 4005 C084h, ADC120.ADDBLDRB 4005 C086h, ADC120.ADTSDR 4005 C01Ah, ADC120.ADOCDR 4005 C01Ch, ADC121.ADDR0 4005 C220h to ADC121.ADDR3 4005 C226h, ADC121.ADDR5 4005 C22Ah to ADC121.ADDR7 4005 C22Eh, ADC121.ADDR16 4005 C240h to ADC121.ADDR19 4005 C246h, ADC121.ADDBLDR 4005 C218h, ADC121.ADDBLDRA 4005 C284h, ADC121.ADDBLDRB 4005 C286h, ADC121.ADTSDR 4005 C21Ah, ADC121.ADOCDR 4005 C21Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	AD[11:0]											
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b11 to b0	AD[11:0]	Converted Value 11 to 0	12-bit A/D-converted value.	R
b15 to b12	—	Reserved	These bits are read as 0.	R

47.2 注册说明

47.2.1 AD数据寄存器y(ADDRy)、AD数据双工寄存器(ADDBLDR)、AD数据双工寄存器A(ADDBLDRA) AD数据双工寄存器B(ADDBLDRB) AD温度传感器数据寄存器(ADTSDR) AD内部参考电压数据寄存器(ADOCDR)

数据寄存器包括：

- ADDRy寄存器（单元0中y=0到7、16到20，单元1中y=0到3、5到7、16到19）：用于存储AD转换结果的16位只读寄存器
- ADDBLDR寄存器：16位只读寄存器，用于存储双触发模式下响应第二次触发的AD转换结果
- ADDBLDRA和ADDBLDRB寄存器：16位只读寄存器，用于存储双触发模式下扩展操作期间响应相应触发的AD转换结果
- ADTSDR寄存器：16位只读寄存器，用于存储温度传感器输出的A/D转换结果
- AOCDR寄存器：16位只读寄存器，用于存储内部参考电压的AD结果。

以下条件决定了这些寄存器中数据的格式：

- AD数据寄存器格式选择位(ADCER.ADRFMT)中的设置（左对齐或右对齐设置）
- AD转换精度指定位(ADCER.ADPRC[1:0])中的设置（8位、10位或12位设置）。

本节介绍不同模式下这些条件的数据格式。

(1) 未选择AD转换值加法平均模式时

每个条件的数据格式如下：

具有12位精度的右冲洗数据设置

Address(es): ADC120.ADDR0 4005 C020h to ADC120.ADDR7 4005 C02Eh, ADC120.ADDR16 4005 C040h to ADC120.ADDR20 4005 C048h, ADC120.ADDBLDR 4005 C018h, ADC120.ADDBLDRA 4005 C084h, ADC120.ADDBLDRB 4005 C086h, ADC120.ADTSDR 4005 C01Ah, ADC120.ADOCDR 4005 C01Ch, ADC121.ADDR0 4005 C220h to ADC121.ADDR3 4005 C226h, ADC121.ADDR5 4005 C22Ah to ADC121.ADDR7 4005 C22Eh, ADC121.ADDR16 4005 C240h to ADC121.ADDR19 4005 C246h, ADC121.ADDBLDR 4005 C218h, ADC121.ADDBLDRA 4005 C284h, ADC121.ADDBLDRB 4005 C286h, ADC121.ADTSDR 4005 C21Ah, ADC121.ADOCDR 4005 C21Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	AD[11:0]											
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b11 to b0	AD[11:0]	将值11转换为0	12-bit A/D-converted value.	R
b15 to b12	—	Reserved	这些位读为0。	R

Settings for flush-right data with 10-bit accuracy

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	AD[9:0]									
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b9 to b0	AD[9:0]	Converted Value 9 to 0	10-bit A/D-converted value.	R
b15 to b10	—	Reserved	These bits are read as 0.	R

Settings for flush-right data with 8-bit accuracy

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	AD[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	AD[7:0]	Converted Value 7 to 0	8-bit A/D-converted value.	R
b15 to b8	—	Reserved	These bits are read as 0.	R

Settings for flush-left data with 12-bit accuracy

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	AD[11:0]												—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	—	Reserved	These bits are read as 0.	R
b15 to b4	AD[11:0]	Converted Value 11 to 0	12-bit A/D-converted value.	R

Settings for flush-left data with 10-bit accuracy

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	AD[9:0]										—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b5 to b0	—	Reserved	These bits are read as 0.	R
b15 to b6	AD[9:0]	Converted Value 9 to 0	10-bit A/D-converted value.	R

具有10位精度的右冲洗数据设置

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	AD[9:0]									
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b9 to b0	AD[9:0]	将值9转换为0	10-bit A/D-converted value.	R
b15 to b10	—	Reserved	这些位读为0。	R

具有8位精度的右对齐数据设置

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	AD[7:0]							
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b7 to b0	AD[7:0]	将值7转换为0	8-bit A/D-converted value.	R
b15 to b8	—	Reserved	这些位读为0。	R

具有12位精度的左对齐数据的设置

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	AD[11:0]												—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b3 to b0	—	Reserved	这些位读为0。	R
b15 to b4	AD[11:0]	将值11转换为0	12-bit A/D-converted value.	R

具有10位精度的左对齐数据的设置

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	AD[9:0]										—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b5 to b0	—	Reserved	这些位读为0。	R
b15 to b6	AD[9:0]	将值9转换为0	10-bit A/D-converted value.	R

Settings for flush-left data with 8-bit accuracy

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	AD[7:0]								—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	—	Reserved	These bits are read as 0.	R
b15 to b8	AD[7:0]	Converted Value 7 to 0	8-bit A/D-converted value.	R

(2) When A/D-converted value average mode is selected

A/D-converted value average mode can be selected when 2 or 4 times is specified in A/D-converted value addition mode. When A/D-converted value average mode is selected, this register indicates the mean of the A/D-converted values on the specified channel. The value is stored in the A/D data register based on the setting in the A/D Data Register Format Select bit in the same way as for normal A/D conversion.

(3) When A/D-converted value addition mode is selected

For 8-, 10-, or 12-bit accuracy (ADPRC bit setting), 1, 2, 3 or 4 times can be selected for A/D-converted value addition. 16 times can also be selected for addition mode, but only with 12-bit accuracy selected. In addition mode, this register indicates the value that is obtained by adding the A/D-converted values on a specific channel. The conversion results sum is retained in the A/D data register as a 2-bit-extended value of the conversion accuracy specified. The value is stored in the A/D data register based on the setting in the A/D Data Register Format Select bit in the same way as for normal A/D conversion.

When converting 1, 2, 3, or 4 times in addition mode with 8-, 10-, or 12-bit accuracy specified, the conversion result is stored in the A/D data register as a 2-bit-extended value of the specified accuracy.

When converting 16 times in addition mode with 12-bit accuracy specified the conversion result is stored in the A/D data register as a 4-bit-extended value of the specified accuracy.

The data formats for each condition are as follows:

Settings for flush-right data with 12-bit accuracy in A/D-converted value addition mode

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	AD[15:0]*1															
	—	—	AD[13:0]*2													
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b15 to b0	AD[15:0]*1	Added Value 15 to 0	16 -bit sum of A/D conversion results.	R

Bit	Symbol	Bit name	Description	R/W
b13 to b0	AD[13:0]*2	Added Value 13 to 0	14-bit sum of A/D conversion results.	R
b15, b14	—	Reserved	These bits are read as 0.	R

Note 1. Used when 16 conversion times is specified in A/D-converted value addition mode.
Note 2. Used when 1, 2, 3, or 4 conversion times is specified in A/D-converted value addition mode.

8位精度的左对齐数据设置

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	AD[7:0]								—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b7 to b0	—	Reserved	这些位读为0。	R
b15 to b8	AD[7:0]	将值7转换为0	8-bit A/D-converted value.	R

(2) 选择AD转换值平均模式时

当在AD转换值相加模式中指定2或4次时，可以选择D转换值平均模式。WhenAD-convertedvalueaveragemodeisselected thisregisterindicatesthemeanoftheAD-convertedvaluesonthespecifiedchannel.该值根据AD数据寄存器格式选择位中的设置以与正常AD转换相同的方式存储在AD数据寄存器中。

(3) 选择AD转换值相加模式时

对于8位、10位或12位精度（ADPRC位设置），可以选择1、2、3或4次进行AD转换值相加。加法模式也可以选择16次，但只能选择12位精度。在加法模式下，该寄存器指示通过将特定通道上的AD转换值相加而获得的值。转换结果和作为指定转换精度的2位扩展值保留在AD数据寄存器中。该值根据AD数据寄存器格式选择位中的设置以与正常AD转换相同的方式存储在AD数据寄存器中。

在指定精度为8位、10位或12位精度的加法模式下转换1、2、3或4次时，转换结果作为指定精度的2位扩展值存储在AD数据寄存器中.

在指定精度的12位加法模式下转换16次时，转换结果作为指定精度的4位扩展值存储在AD数据寄存器中。

每个条件的数据格式如下：

在AD转换值相加模式下以12位精度设置刷新数据

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	AD[15:0]*1															
	—	—	AD[13:0]*2													
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b15 to b0	AD[15:0]*1	附加值15到0	AD转换结果的16位和。	R

Bit	Symbol	位名称	Description	R/W
b13 to b0	AD[13:0]*2	附加值13到0	AD转换结果的14位和。	R
b15, b14	—	Reserved	这些位读为0。	R

Note 1. 在AD转换值加法模式中指定16次转换时使用。
Note 2. 在AD转换值相加模式中指定1、2、3或4转换时间时使用。

Settings for flush-right data with 10-bit accuracy in A/D-converted value addition mode

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	AD[11:0]											
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b11 to b0	AD[11:0]	Added Value 11 to 0	12-bit sum of A/D conversion results.	R
b15 to b12	—	Reserved	These bits are read as 0.	R

Settings for flush-right data with 8-bit accuracy in A/D-converted value addition mode

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	AD[9:0]									
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b9 to b0	AD[9:0]	Added Value 9 to 0	10-bit sum of A/D conversion results	R
b15 to b10	—	Reserved	These bits are read as 0.	R

Settings for flush-left data with 12-bit accuracy in A/D-converted value addition mode

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	AD[15:0]*1															
	AD[13:0]*2														—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b15 to b0	AD[15:0]*1	Added Value 15 to 0	16 -bit sum of A/D conversion results.	R

Bit	Symbol	Bit name	Description	R/W
b1, b0	—	Reserved	These bits are read as 0.	R
b15 to b2	AD[13:0]*2	Added Value 13 o 0	14-bit sum of A/D conversion results.	R

Note 1. Used when 16 conversion times is selected in A/D-converted value addition mode.
Note 2. Used when 1, 2, 3, or 4 conversion times is selected in A/D-converted value addition mode.

AD转换值加法模式下10位精度的右冲洗数据设置

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	AD[11:0]											
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b11 to b0	AD[11:0]	附加值11到0	AD转换结果的12位和。	R
b15 to b12	—	Reserved	这些位读为0。	R

在AD转换值相加模式下以8位精度设置右对齐数据

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	AD[9:0]									
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b9 to b0	AD[9:0]	附加值9到0	AD转换结果的10位和	R
b15 to b10	—	Reserved	这些位读为0。	R

AD转换值相加模式下12位精度的左对齐数据的设置

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	AD[15:0]*1															
	AD[13:0]*2														—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b15 to b0	AD[15:0]*1	附加值15到0	AD转换结果的16位和。	R

Bit	Symbol	位名称	Description	R/W
b1, b0	—	Reserved	这些位读为0。	R
b15 to b2	AD[13:0]*2	附加值13o0	AD转换结果的14位和。	R

Note 1. 在AD转换值相加模式中选择16次转换时使用。
Note 2. 在AD转换值相加模式中选择1、2、3或4转换时间时使用。

Settings for flush-left data with 10-bit accuracy in A/D-converted value addition mode

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	AD[11:0]												—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	—	Reserved	These bits are read as 0.	R
b15 to b4	AD[11:0]	Added Value 11 to 0	12-bit sum of A/D conversion results.	R

Settings for flush-left data with 8-bit accuracy in A/D-converted value addition mode

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	AD[9:0]										—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b5 to b0	—	Reserved	These bits are read as 0.	R
b15 to b6	AD[9:0]	Added Value 9 to 0	10-bit sum of A/D conversion results.	R

47.2.2 A/D Self-Diagnosis Data Register (ADRD)

ADRD is a 16-bit read-only register that holds the A/D conversion results based on the self-diagnosis of the ADC12. In addition to the AD[11:0] bits indicating the A/D-converted value, it includes the self-diagnosis status bit (DIAGST).

The following conditions determine the formats for data in this registers:

- The setting in the A/D Data Register Format Select bit (ADCER.ADRFMT) (flush-left or flush-right setting)
- The setting in the A/D Conversion Accuracy Specify bits (ADCER.ADPRC[1:0]) (8-, 10-, or 12-bit setting).

The A/D-converted value addition and average modes cannot be applied to the A/D self-diagnosis function. For details on self-diagnosis, see section 47.2.11, A/D Control Extended Register (ADCER).

This section describes the data formats for each condition.

Settings for flush-right data with 12-bit accuracy

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	DIAGST[1:0]		—	—	AD[11:0]											
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b11 to b0	AD[11:0]	Converted Value 11 to 0	12-bit A/D-converted value.	R
b13, b12	—	Reserved	These bits are read as 0.	R
b15, b14	DIAGST[1:0]	Self-Diagnosis Status	b15 b14 0 0: Self-diagnosis not executed after power-on 0 1: Self-diagnosis was executed using the 0 V voltage 1 0: Self-diagnosis was executed using the reference power supply*1 voltage x 1/2 1 1: Self-diagnosis was executed using the reference power supply*1 voltage. For details on self-diagnosis, see section 47.2.11, A/D Control Extended Register (ADCER).	R

AD转换值加法模式下10位精度的左对齐数据设置

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	AD[11:0]												—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b3 to b0	—	Reserved	这些位读为0。	R
b15 to b4	AD[11:0]	附加值11到0	AD转换结果的12位和。	R

AD转换值加法模式中8位精度的左对齐数据的设置

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	AD[9:0]										—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b5 to b0	—	Reserved	这些位读为0。	R
b15 to b6	AD[9:0]	附加值9到0	AD转换结果的10位和。	R

47.2.2 AD自诊断数据寄存器(ADRD)

ADRD是一个16位只读寄存器，保存基于ADC12自诊断的AD转换结果。除了指示AD转换值的AD[11:0]位外，它还包括自诊断状态位(DIAGST)。

以下条件决定了该寄存器中数据的格式：

- AD数据寄存器格式选择位(ADCER.ADRFMT)中的设置（左对齐或右对齐设置）
- AD转换精度指定位(ADCER.ADPRC[1:0])中的设置（8位、10位或12位设置）。

AD转换值加法和平均模式不能应用于AD自诊断功能。有关自诊断的详细信息，请参见第47.2.11节，AD控制扩展寄存器(ADCER)。

本节介绍每个条件的数据格式。

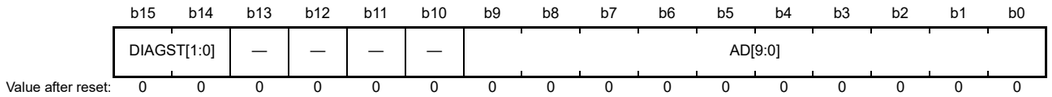
具有12位精度的右冲洗数据设置

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	DIAGST[1:0]		—	—	AD[11:0]											
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b11 to b0	AD[11:0]	将值11转换为0	12-bit A/D-converted value.	R
b13, b12	—	Reserved	这些位读为0。	R
b15, b14	DIAGST[1:0]	Self-Diagnosis Status	b15b1400：上电后不执行自诊断01：使用0V电压执行自诊断10：使用参考电源执行自诊断*1电压x1211：自-使用参考电源*1电压执行诊断。有关自诊断的详细信息，请参阅第47.2.11节，AD控制 扩展寄存器(ADCER)。	R

Note 1. The reference voltage refers to VREFH0 for unit 0 and to VREFH for unit 1.

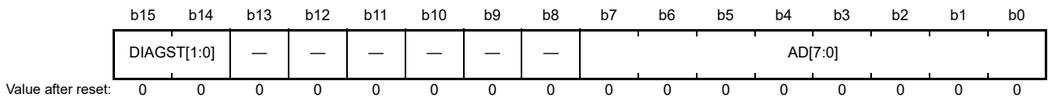
Settings for flush-right data with 10-bit accuracy



Bit	Symbol	Bit name	Description	R/W
b9 to b0	AD[9:0]	Converted Value 9 to 0	10-bit A/D-converted value.	R
b13 to b10	—	Reserved	These bits are read as 0.	R
b15, b14	DIAGST[1:0]	Self-Diagnosis Status	b15 b14 0 0: Self-diagnosis not executed after power-on 0 1: Self-diagnosis was executed using the 0 V voltage 1 0: Self-diagnosis was executed using the reference power supply*1 voltage x 1/2 1 1: Self-diagnosis was executed using the reference power supply*1 voltage For details on self-diagnosis, see section 47.2.11, A/D Control Extended Register (ADCER).	R

Note 1. The reference voltage refers to VREFH0 for unit 0 and to VREFH for unit 1.

Settings for flush-right data with 8-bit accuracy

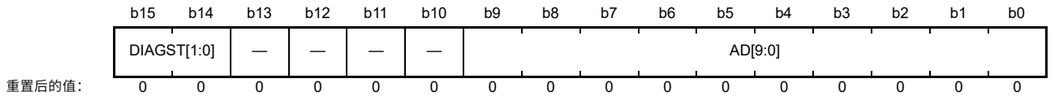


Bit	Symbol	Bit name	Description	R/W
b7 to b0	AD[7:0]	Converted Value 7 to 0	8-bit A/D-converted value	R
b13 to b8	—	Reserved	These bits are read as 0.	R
b15, b14	DIAGST[1:0]	Self-Diagnosis Status	b15 b14 0 0: Self-diagnosis not executed after power-on 0 1: Self-diagnosis was executed using the 0 V voltage 1 0: Self-diagnosis was executed using the reference power supply*1 voltage x 1/2 1 1: Self-diagnosis was executed using the reference power supply*1 voltage. For details on self-diagnosis, see section 47.2.11, A/D Control Extended Register (ADCER).	R

Note 1. The reference voltage refers to VREFH0 for unit 0 and to VREFH for unit 1.

Note 1. 参考电压是指单元0的VREFH0和单元1的VREFH。

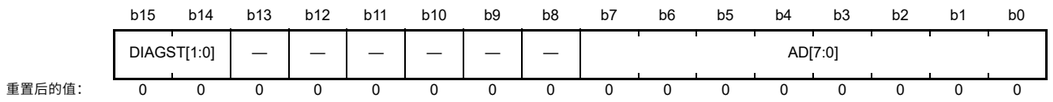
具有10位精度的右冲洗数据设置



Bit	Symbol	位名称	Description	R/W
b9 to b0	AD[9:0]	将值9转换为0	10-bit A/D-converted value.	R
b13 to b10	—	Reserved	这些位读为0。	R
b15, b14	DIAGST[1:0]	Self-Diagnosis Status	b15b1400：上电后不执行自诊断01：使用0V电压执行自诊断10：使用参考电源执行自诊断*1电压x1211：自-使用参考电源执行诊断*1电压有关自诊断的详细信息，请参阅第47.2.11节，AD控制 扩展寄存器(ADCER)。	R

Note 1. 参考电压是指单元0的VREFH0和单元1的VREFH。

具有8位精度的右对齐数据设置



Bit	Symbol	位名称	Description	R/W
b7 to b0	AD[7:0]	将值7转换为0	8-bit A/D-converted value	R
b13 to b8	—	Reserved	这些位读为0。	R
b15, b14	DIAGST[1:0]	Self-Diagnosis Status	b15b1400：上电后不执行自诊断01：使用0V电压执行自诊断10：使用参考电源执行自诊断*1电压x1211：自-使用参考电源*1电压执行诊断。有关自诊断的详细信息，请参阅第47.2.11节，AD控制 扩展寄存器(ADCER)。	R

Note 1. 参考电压是指单元0的VREFH0和单元1的VREFH。

Settings for flush-left data with 12-bit accuracy

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	AD[11:0]												—	—	DIAGST[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	DIAGST[1:0]	Self-Diagnosis Status	b1 b0 0 0: Self-diagnosis not executed after power-on 0 1: Self-diagnosis using the voltage of 0 V was executed 1 0: Self-diagnosis using the voltage of reference power supply*1 × 1/2 was executed 1 1: Self-diagnosis using the voltage of reference power supply*1 was executed. For details on self-diagnosis, see section 47.2.11, A/D Control Extended Register (ADCER).	R
b3, b2	—	Reserved	These bits are read as 0.	R
b15 to b4	AD[11:0]	Converted Value 11 to 0	12-bit A/D-converted value	R

Note 1. The reference voltage refers to VREFH0 for unit 0 and to VREFH for unit 1.

Settings for flush-left data with 10-bit accuracy

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	AD[9:0]										—	—	—	—	DIAGST[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	DIAGST[1:0]	Self-Diagnosis Status	b1 b0 0 0: Self-diagnosis not executed after power-on 0 1: Self-diagnosis was executed using the 0 V voltage 1 0: Self-diagnosis was executed using the reference power supply*1 × 1/2 voltage 1 1: Self-diagnosis was executed using the reference power supply*1 voltage. For details on self-diagnosis, see section 47.2.11, A/D Control Extended Register (ADCER).	R
b5 to b2	—	Reserved	These bits are read as 0.	R
b15 to b6	AD[9:0]	Converted Value 9 to 0	10-bit A/D-converted value.	R

Note 1. The reference voltage refers to VREFH0 for unit 0 and to VREFH for unit 1.

具有12位精度的左对齐数据的设置

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	AD[11:0]												—	—	DIAGST[1:0]	
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b1, b0	DIAGST[1:0]	Self-Diagnosis Status	b1b000：上电后不执行自诊断01：使用0V电压执行自诊断10：使用参考电源电压进行自诊断*1×12执行11:执行了使用参考电源电压*1的自诊断。有关自诊断的详细信息，请参阅第47.2.11节，AD控制扩展寄存器(ADCER)。	R
b3, b2	—	Reserved	这些位读为0。	R
b15 to b4	AD[11:0]	将值11转换为0	12-bit A/D-converted value	R

Note 1. 参考电压是指单元0的VREFH0和单元1的VREFH。

具有10位精度的左对齐数据的设置

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	AD[9:0]										—	—	—	—	DIAGST[1:0]	
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b1, b0	DIAGST[1:0]	Self-Diagnosis Status	b1b000：上电后不执行自诊断01：使用0V电压执行自诊断10：使用参考电源执行自诊断*1×12电压11：自诊断-使用参考电源*1电压执行诊断。有关自诊断的详细信息，请参阅第47.2.11节，AD控制扩展寄存器(ADCER)。	R
b5 to b2	—	Reserved	这些位读为0。	R
b15 to b6	AD[9:0]	将值9转换为0	10-bit A/D-converted value.	R

Note 1. 参考电压是指单元0的VREFH0和单元1的VREFH。

Settings for flush-left data with 8-bit accuracy

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	AD[7:0]								—	—	—	—	—	—	DIAGST[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	DIAGST[1:0]	Self-Diagnosis Status	b1 b0 0 0: Self-diagnosis not executed after power-on 0 1: Self-diagnosis was executed using the 0 V voltage 1 0: Self-diagnosis was executed using the reference power supply*1 × 1/2 voltage 1 1: Self-diagnosis was executed using the reference power supply*1 voltage. For details on self-diagnosis, see section 47.2.11, A/D Control Extended Register (ADCER).	R
b7 to b2	—	Reserved	These bits are read as 0.	R
b15 to b8	AD[7:0]	Converted Value 7 to 0	8-bit A/D-converted value	R

Note 1. The reference voltage refers to VREFH0 for unit 0 and to VREFH for unit 1.

47.2.3 A/D Control Register (ADCSR)

Address(es): ADC120.ADCSR 4005 C000h, ADC121.ADCSR 4005 C200h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ADST	ADCS[1:0]			—		TRGE	EXTRG	DBLE	GBADIE	—	DBLANS[4:0]				
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b4 to b0	DBLANS[4:0]	Double Trigger Channel Select	These bits select one analog input channel for double-triggered operation. The setting is only valid in double-trigger mode.	R/W
b5	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b6	GBADIE	Group B Scan End Interrupt and ELC Event Enable	0: Disable ADC12i_GBADI interrupt generation on Group B scan completion 1: Enable ADC12i_GBADI interrupt generation on Group B scan completion. Group B scan only works in group scan mode.	R/W
b7	DBLE	Double Trigger Mode Select	0: Deselect double-trigger mode 1: Select double-trigger mode.	R/W
b8	EXTRG	Trigger Select*1	0: Start A/D conversion by a synchronous trigger (ELC) 1: Start A/D conversion by the asynchronous trigger (ADTRGi).	R/W
b9	TRGE	Trigger Start Enable	0: Disable A/D conversion to be started by the synchronous or asynchronous trigger 1: Enable A/D conversion to be started by the synchronous or asynchronous trigger.	R/W
b12 to b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b14, b13	ADCS[1:0]	Scan Mode Select	b14 b13 0 0: Single scan mode 0 1: Group scan mode 1 0: Continuous scan mode 1 1: Setting prohibited.	R/W
b15	ADST	A/D Conversion Start	0: Stop A/D conversion process 1: Start A/D conversion process.	R/W

8位精度的左对齐数据设置

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	AD[7:0]								—	—	—	—	—	—	DIAGST[1:0]	
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b1, b0	DIAGST[1:0]	Self-Diagnosis Status	b1b000：上电后不执行自诊断01：使用0V电压执行自诊断10：使用参考电源执行自诊断*1×12电压11：自诊断-使用参考电源*1电压执行诊断。有关自诊断的详细信息，请参阅第47.2.11节，AD控制扩展寄存器(ADCER)。	R
b7 to b2	—	Reserved	这些位读为0。	R
b15 to b8	AD[7:0]	将值7转换为0	8-bit A/D-converted value	R

Note 1. 参考电压是指单元0的VREFH0和单元1的VREFH。

47.2.3 AD控制寄存器(ADCSR)

Address(es): ADC120.ADCSR 4005 C000h, ADC121.ADCSR 4005 C200h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ADST	ADCS[1:0]			—		TRGE	EXTRG	DBLE	GBADIE	—	DBLANS[4:0]				
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b4 to b0	DBLANS[4:0]	双触发通道 Select	这些位选择一个模拟输入通道进行双触发操作。该设置仅在双触发模式下有效。	R/W
b5	—	Reserved	该位读取为0。写入值应为0。	R/W
b6	GBADIE	B组扫描结束中断和ELC事件 Enable	0：在B组扫描完成时禁用ADC12i_GBADI中断生成1：在B组扫描完成时启用ADC12i_GBADI中断生成。B组扫描仅适用于组扫描模式。	R/W
b7	DBLE	双触发模式 Select	0：取消选择双触发模式1：选择双触发模式。	R/W
b8	EXTRG	触发选择 *1	0：通过同步触发（ELC）开始AD转换1：通过异步触发（ADTRGi）开始AD转换。	R/W
b9	TRGE	触发启动启用	0：禁止由同步或异步触发器启动的AD转换1：使能由同步或异步触发器启动的AD转换。	R/W
b12 to b10	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b14, b13	ADCS[1:0]	扫描模式选择	b14b1300：单次扫描模式01：组扫描模式10：连续扫描模式11：禁止设置。	R/W
b15	ADST	AD转换开始	0：停止AD转换过程1：开始AD转换过程。	R/W

i = 0 for unit 0, and i = 1 for unit 1.

Note 1. To start A/D conversion using an external pin (asynchronous trigger):
After a high-level signal is input to the external pin (ADTRG0 in unit 0; ADTRG1 in unit 1), write 1 to both the TRGE and EXTRG bits in ADCSR and drive the external pin signals low. With these settings, the scan conversion process starts on detection of the falling edge of ADTRG0 in unit 0 and ADTRG1 in unit 1. For this configuration, the pulse width of the low-level input must be at least 1.5 PCLKB clock cycles.

DBLANS[4:0] bits (Double Trigger Channel Select)

The DBLANS[4:0] bits select one of the channels for A/D conversion data duplication in double-trigger mode. The A/D conversion results from the specified analog input channel are stored in A/D Data Register y when conversion is started by the first trigger, and in the A/D Data Duplexing Register when started by the second trigger. Table 47.4 shows the channel selection settings for double-triggered operation.

A/D-converted value addition/average mode can be set with double-trigger mode for the channel selected in the DBLANS[4:0] bits by using the ADADS0 and ADADS1 registers. In double-trigger mode, the channels selected in the ADANSA0 and ADANSA1 registers are invalid, and the channel selected in the DBLANS[4:0] bits is A/D-converted instead.

When double-trigger mode is used in group scan mode, double-trigger control is only applied to Group A and not to Group B. This means that multi-channel analog input, temperature sensor output, and internal reference voltage can be selected for Group B even in double-trigger mode.

Only set the DBLANS[4:0] bits while the ADST bit is 0. Do not set them at the same time that you write 1 to the ADST bit.

To enter A/D-converted value addition/average mode when in double-trigger mode, set the channel selected in the DBLANS[4:0] bits in the ADANSA0 and ADANSA1 registers.

Table 47.4 Relationship between DBLANS bit settings and double-trigger enabled channels

Unit 0		Unit 1	
DBLANS[4:0]	Duplication channel	DBLANS[4:0]	Duplication channel
00000	AN000	00000	AN100
00001	AN001	00001	AN101
00010	AN002	00010	AN102
00011	AN003	00011	AN103
00100	AN004	00100	—
00101	AN005	00101	AN105
00110	AN006	00110	AN106
00111	AN007	00111	AN107
Unit 0		Unit 1	
DBLANS[4:0]	Duplication channel	DBLANS[4:0]	Duplication channel
10000	AN016	10000	AN116
10001	AN017	10001	AN117
10010	AN018	10010	AN118
10011	AN019	10011	AN119
10100	AN020	10100	—

Note: A/D-converted data from the self-diagnosis function, temperature sensor output, and internal reference voltage cannot be used in double-trigger mode.
Settings other than those listed in Table 47.4 are prohibited.

GBADIE bit (Group B Scan End Interrupt and ELC Event Enable)

The GBADIE bit enables or disables Group B scan end interrupt (ADC12i_GBADI (i = 0, 1)) in group scan mode.

DBLE bit (Double Trigger Mode Select)

The DBLE bit selects or deselects double-trigger mode. Double-trigger mode can only be operated by the synchronous

对于单元0，i=0，对于单元1，i=1。

Note 1. 使用外部引脚（异步触发）启动AD转换：
向外部引脚（单元0中的ADTRG0；单元1中的ADTRG1）输入高电平信号后，向ADCSR的TRGE和EXTRG位写入1，并将外部引脚信号驱动为低电平。使用这些设置，扫描转换过程在检测到单元0中的ADTRG0和单元1中的ADTRG1的下降沿时开始。对于这种配置，低电平输入的脉冲宽度必须至少为1.5个PCLKB时钟周期。

DBLANS[4:0]位（双触发通道选择）

DBLANS[4:0]位选择通道之一，用于双触发模式下的AD转换数据复制。指定模拟输入通道的AD转换结果在第一次触发开始转换时存储在AD数据寄存器y中，在第二次触发开始时存储在AD数据双工寄存器中。表47.4显示了双触发操作的通道选择设置。

D转换值加法平均模式可以设置为双触发模式用于在
DBLANS[4:0]位通过使用ADADS0和ADADS1寄存器。在双触发模式下，ADANSA0和ADANSA1寄存器中选择的通道无效，DBLANS[4:0]位中选择的通道改为AD转换。

在组扫描模式下使用双触发模式时，双触发控制仅适用于A组，不适用
B组。这意味着即使在双触发模式下，也可以为B组选择多通道模拟输入、温度传感器输出和内部参考电压。

仅在ADST位为0时设置DBLANS[4:0]位。不要在将1写入ADST位的同时设置它们。

要在双触发模式下进入AD转换值加法平均模式，请设置在
ADANSA0和ADANSA1寄存器中的DBLANS[4:0]位。

Table 47.4 DBLANS位设置与双触发启用通道之间的关系

Unit 0		Unit 1	
DBLANS[4:0]	复制通道	DBLANS[4:0]	复制通道
00000	AN000	00000	AN100
00001	AN001	00001	AN101
00010	AN002	00010	AN102
00011	AN003	00011	AN103
00100	AN004	00100	—
00101	AN005	00101	AN105
00110	AN006	00110	AN106
00111	AN007	00111	AN107
Unit 0		Unit 1	
DBLANS[4:0]	复制通道	DBLANS[4:0]	复制通道
10000	AN016	10000	AN116
10001	AN017	10001	AN117
10010	AN018	10010	AN118
10011	AN019	10011	AN119
10100	AN020	10100	—

Note: 自诊断功能、温度传感器输出和内部参考电压的D转换数据不能用于双触发模式。禁止在表47.4中列出以外的设置。

GBADIE位（B组扫描结束中断和ELC事件使能）

GBADIE位在组扫描模式下启用或禁用组B扫描结束中断(ADC12i_GBADI(i=0 1))。

DBLE位（双触发模式选择）

DBLE位选择或取消选择双触发模式。双触发模式只能由同步操作

trigger (ELC) selected in the ADSTRGR.TRSA[5:0] bits.

Double-trigger operation is as follows:

1. The ADC12i_ADI (i = 0, 1) interrupt is not output on completion of the first conversion but on completion of the second conversion.
2. The A/D conversion results from the duplication channel (selected in DBLANS[4:0]) started by the first trigger are stored in A/D Data Register y and those started by the second trigger are stored in the A/D Data Duplexing Register.

When DBLE is set, selecting double-trigger mode, the channels specified in the ADANSA0 and ADANSA1 registers are invalid. Double-trigger mode is deselected by setting DBLE to 0. Setting DBLE to 1 again enables the same double-trigger operation described in 1. and 2. for the first time scanning with the first trigger.

Do not select double-trigger mode in continuous scan mode. Additionally, do not select double-trigger mode for conversion of the temperature sensor output or internal reference voltage except for Group B scan in group scan mode. Software triggering cannot be set in double-trigger mode. Always clear the ADST bit to 0 before setting the DBLE bit. In other words, do not set the DBLE bit at that same time as writing 1 to the ADST bit.

EXTRG bit (Trigger Select)

The EXTRG bit selects the synchronous or asynchronous trigger as the trigger for starting A/D conversion.

TRGE bit (Trigger Start Enable)

The TRGE bit enables or disables A/D conversion by the synchronous and asynchronous triggers. In group scan mode, set this bit to 1.

ADCS[1:0] bits (Scan Mode Select)

The ADCS[1:0] bits select the scan mode.

In single scan mode, A/D conversion is performed for the analog inputs, up to a maximum of 13 channels in unit 0 and 11 channels in unit 1, and selected in the ADANSA0 and ADANSA1 registers in ascending order of channel number. When 1 cycle of A/D conversion completes for all the selected channels, the scan conversion stops. When the temperature sensor output or internal reference voltage is selected, A/D conversion of the designated analog input channels is followed by A/D conversion of the temperature sensor output and the internal reference voltage, in that order.

In continuous scan mode, while the ADCSR.ADST bit is 1, A/D conversion is performed for the analog inputs selected in the ADANSA0 and ADANSA1 registers in ascending order of channel number, and when 1 cycle of A/D conversion completes for all the selected channels, A/D conversion is repeated from the first channel. If the ADCSR.ADST bit is set to 0 during continuous scan, A/D conversion stops even if scanning is in progress. When the temperature sensor output or internal reference voltage is selected, A/D conversion of the designated analog input channels is followed by A/D conversion of the temperature sensor output and the internal reference voltage, in that order.

In group scan mode, scanning is started by the synchronous trigger (ELC) selected in the TRSA[5:0] bits in ADSTRGR. A/D conversion is performed on the Group A analog inputs, up to the maximum channels selected in the ADANSA0 and ADANSA1 registers, in ascending order of channel number. When 1 cycle of A/D conversion completes for all the selected channels, A/D conversion stops. On the same trigger, A/D conversion is also performed on the Group B analog inputs, up to the maximum channels selected in the ADANSB0 and ADANSB1 registers, in ascending order of channel number. When 1 cycle of A/D conversion completes for all the selected channels, A/D conversion stops. If the conversion processes in Group A and Group B occur at the same time, those conversions cannot be controlled separately. In this case, set the Group A Priority Control Setting bit (ADGSPCR.PGS) in the A/D Group Scan Priority Control Register (ADGSPCR) to 1 to give priority to Group A conversion. When the temperature sensor output or internal reference voltage is selected, A/D conversion of the designated analog input channels is followed by A/D conversion of the temperature sensor output and the internal reference voltage, in that order.

In group scan mode, select different channels and triggers for Group A and Group B. Clear the ADST bit to 0 before setting the ADCS[1:0] bits. In other words, do not set the ADCS[1:0] bits at the same time as writing 1 to the ADST bit.

在ADSTRGR.TRSA[5:0]位中选择触发(ELC)。

双触发操作如下：

1. ADC12i_ADI(i=0 1)中断不会在第一次转换完成时输出，而是在第二次转换完成时输出。
2. 由第一个触发器启动的复制通道（在DBLANS[4:0]中选择）的AD转换结果存储在AD数据寄存器y中，由第二个触发器启动的那些存储在AD数据双工寄存器中。

设置DBLE时，选择双触发模式，ADANSA0和ADANSA1寄存器中指定的通道无效。通过将DBLE设置为0来取消选择双触发模式。再次将DBLE设置为1将启用与1.和2.中描述的相同的双触发操作，第一次使用第一个触发进行扫描。

不要在连续扫描模式下选择双触发模式。此外，不要选择双触发模式来转换温度传感器输出或内部参考电压，组扫描模式下的B组扫描除外。双触发模式下不能设置软件触发。在设置DBLE位之前，始终将ADST位清零。换言之，不要在将1写入ADST位的同时设置DBLE位。

EXTRG位（触发选择）

EXTRG位选择同步或异步触发作为启动AD转换的触发。

TRGE位（触发启动使能）

TRGE位通过同步和异步触发启用或禁用AD转换。在组扫描模式下，将此位设置为1。

ADCS[1:0]位（扫描模式选择）

ADCS[1:0]位选择扫描模式。

在单次扫描模式下，对模拟输入进行AD转换，单元0中最多13个通道，单元1中最多11个通道，并在ADANSA0和ADANSA1寄存器中按照通道号的升序进行选择。当所有选定通道的1个AD转换周期完成时，扫描转换停止。Whenthetemperaturesensoroutputorinternalreferencevoltageisselected ADconversionofthedesignatedanaloginputchannelsisfollowedbyADconversionofthetemperaturesensoroutputandtheinternalreferencevoltage inthatorder.

在连续扫描模式下，当ADCSR.ADST位为1时，ADANSA0和ADANSA1寄存器中选择的模拟输入按通道编号升序执行AD转换，当所有选择的通道完成1个周期的AD转换时，从第一个通道重复D转换。如果在连续扫描期间ADCSR.ADST位设置为0，即使扫描正在进行，AD转换也会停止。Whenthetemperaturesensoroutputorinternalreferencevoltageisselected ADconversionofthedesignatedanaloginputchannelsisfollowedbyADconversionofthetemperaturesensoroutputandtheinternalreferencevoltage inthatorder.

在组扫描模式下，扫描由在ADSTRGR的TRSA[5:0]位中选择的同步触发(ELC)启动。AD转换在A组模拟输入上执行，直到ADANSA0和ADANSA1寄存器中选择的最大通道，按通道编号的升序排列。当所有选定通道完成1个AD转换周期时，AD转换停止。在同一个触发器上，B组模拟输入也执行AD转换，直到ADANSB0和ADANSB1寄存器中选择的最大通道，按通道编号的升序排列。当所有选定通道完成1个AD转换周期时，AD转换停止。如果A组和B组的转换过程同时发生，则不能单独控制这些转换。在这种情况下，将AD组扫描优先级控制寄存器(ADGSPCR)中的组A优先级控制设置位(ADGSPCR.PGS)设置为1，以优先于A组转换。Whenthetemperaturesensoroutputorinternalreferencevoltageisselected ADconversionofthedesignatedanaloginputchannelsisfollowedbyADconversionofthetemperaturesensoroutputandtheinternalreferencevoltage inthatorder.

在组扫描模式下，为A组和B组选择不同的通道和触发。在设置ADCS[1:0]位之前，将ADST位清零。换言之，不要在将1写入ADST位的同时设置ADCS[1:0]位。

Table 47.5 Selectable targets for A/D conversion depending on scan and double-trigger mode settings

Scan mode setting	Double-trigger mode setting	Targets for A/D conversion				
		Self-diagnosis	Analog input (including Group A)	Analog input (Group B)	Temperature sensor output	Internal reference voltage
Single scan	DBLE = 0	✓	✓	-	✓	✓
	DBLE = 1	-	✓ (1 ch only)	-	-	-
Continuous scan	DBLE = 0	✓	✓	-	✓	✓
	DBLE = 1	-	-	-	-	-
Group scan	DBLE = 0	✓	✓	✓	✓	✓
	DBLE = 1	-	✓ (1 ch only)	✓	✓	✓

✓: Selectable. -: Not selectable.

ADST bit (A/D Conversion Start)

The ADST bit starts or stops the A/D conversion process. Before setting the ADST bit to 1, set the A/D conversion clock, conversion mode, and analog input for the conversion target.

[Setting conditions]

- 1 is written by software
- The synchronous trigger (ELC) selected in the ADSTRGR.TRSA[5:0] bits is detected when ADCSR.EXTRG is 0 and ADCSR.TRGE is 1
- The synchronous trigger (ELC) selected in the ADSTRGR.TRSB[5:0] bits is detected when ADCSR.TRGE is set to 1 in group scan mode
- The asynchronous trigger is detected when the ADCSR.TRGE and ADCSR.EXTRG bits are set to 1 and the ADSTRGR.TRSA[5:0] bits are set to 000000b
- When Group A priority control operation mode is enabled (ADCSR.ADCS[1:0] bits = 01b and ADGSPCR.PGS bit = 1), the ADGSPCR.GBRP bit is set to 1, and each time A/D conversion of Group B starts.

[Clearing conditions]

- 0 is written by software
- The A/D conversion of all the selected channels, the temperature sensor output or the internal reference voltage completes in single scan mode
- Group A scan completes in group scan mode
- Group B scan completes in group scan mode
- When Group A priority control operation mode is enabled (ADCSR.ADCS[1:0] bits = 01b and ADGSPCR.PGS bit = 1), the ADGSPCR.GBRP bit is set to 1, and each time a scanning of Group B completes.

Note: When Group A priority control operation mode is enabled (ADCSR.ADCS[1:0] bits = 01b and ADGSPCR.PGS bit = 1), do not set the ADST bit to 1.
When Group A priority control operation mode is enabled (ADCSR.ADCS[1:0] bits = 01b and ADGSPCR.PGS bit = 1), do not set the ADST bit to 0. When forcing A/D conversion to terminate, follow the procedure for clearing the ADST bit.

Note: If the single scan continuous function is used (ADGSPCR.GBRP = 1) when the group priority operation mode is enabled (ADCSR.ADCS[1:0] = 01b and ADGSPCR.PGS = 1), the ADST bit is retained to 1.

Table 47.5 AD转换的可选目标取决于扫描和双触发模式设置

扫描模式设置	双触发模式设置	AD转换的目标				
		Self-diagnosis	模拟输入（包括A组）	模拟输入（B组）	温度传感器输出	内部参考电压
单次扫描	DBLE = 0	✓	✓	-	✓	✓
	DBLE = 1	-	✓ (1 ch only)	-	-	-
连续扫描	DBLE = 0	✓	✓	-	✓	✓
	DBLE = 1	-	-	-	-	-
组扫描	DBLE = 0	✓	✓	✓	✓	✓
	DBLE = 1	-	✓ (1 ch only)	✓	✓	✓

：可选择。–：不可选择。

ADST位（AD转换开始）

ADST位启动或停止AD转换过程。在将ADST位设置为1之前，设置转换目标的AD转换时钟、转换模式和模拟输入。

[Setting conditions]

- 1由软件编写
- 当ADCSR.EXTRG为0且ADCSR.TRGE为1时，检测到在ADSTRGR.TRSA[5:0]位中选择的同步触发(ELC)
- 在组扫描模式下，当ADCSR.TRGE设置为1时，检测到在ADSTRGR.TRSB[5:0]位中选择的同步触发(ELC)
- 当ADCSR.TRGE和ADCSR.EXTRG位设置为1并且ADSTRGR.TRSA[5:0]位设置为000000b
- 当A组优先控制操作模式使能时（ADCSR.ADCS[1:0]位=01b和ADGSPCR.PGS位=1），ADGSPCR.GBRP位设置为1，并且每次B组的AD转换开始。

[Clearing conditions]

- 0是软件写的
- 所有选定通道、温度传感器输出或内部参考电压的AD转换在单次扫描模式下完成
- A组扫描在组扫描模式下完成
- B组扫描在组扫描模式下完成
- 当启用A组优先控制操作模式（ADCSR.ADCS[1:0]位=01b且ADGSPCR.PGS位=1）时，ADGSPCR.GBRP位设置为1，并且每次完成B组扫描。

Note: 当启用A组优先控制操作模式时（ADCSR.ADCS[1:0]位=01b和ADGSPCR.PGS位=1），请勿将ADST位设置为1。当启用A组优先控制操作模式时（ADCSR.ADCS[1:0]位=01b和ADGSPCR.PGS位=1），请勿将ADST位设置为0。当强制终止AD转换时，请按照清除ADST位的程序进行。

Note: 如果在启用组优先操作模式（ADCSR.ADCS[1:0]=01b和ADGSPCR.PGS=1）时使用单次扫描连续功能（ADGSPCR.GBRP=1），则ADST位保持为1。

47.2.4 A/D Channel Select Register A0 (ADANSA0)

Address(es): ADC120.ADANSA0 4005 C004h, ADC121.ADANSA0 4005 C204h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	ANSA07	ANSA06	ANSA05	ANSA04	ANSA03	ANSA02	ANSA01	ANSA00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	ANSA07 to ANSA00	A/D Conversion Channels Select	0: Do not select associated input channel 1: Select associated input channel.	R/W
b15 to b8	-	Reserved.	These bits are read as 0. The write value should be 0.	R/W

ANSAn bits (n = 00 to 07) (A/D Conversion Channels Select)

The ADANSA0.ANSAn bits select or deselect the analog input channels for A/D conversion for AN000 to AN007 (unit 0) and AN100 to AN103 and AN105 to AN107 (unit 1). The channels and the number of channels can be set arbitrarily. In unit 0, the ANSA00 bit is associated with AN000 and the ANSA07 bit with AN007. In unit 1, the ANSA00 bit is associated with AN100 and the ANSA07 bit with AN107.

In double-trigger mode, the channel selected in the ADANSA0 register is invalid, and the channel selected in the ADCSR.DBLANS[4:0] bits is selected in Group A instead.

In group scan mode, do not select the channels specified in A/D Channel Select Register B0 (ADANSB0) and A/D Channel Select Register B1 (ADANSB1).

Only set the ADANSA0 register while the ADCSR.ADST bit is 0.

47.2.5 A/D Channel Select Register A1 (ADANSA1)

Address(es): ADC120.ADANSA1 4005 C006h, ADC121.ADANSA1 4005 C206h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	ANSA20	ANSA19	ANSA18	ANSA17	ANSA16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b4 to b0	ANSA20 to ANSA16	A/D Conversion Channels Select	0: Do not select associated input channel 1: Select associated input channel	R/W
b15 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

ANSAn bits (n = 16 to 20) (A/D Conversion Channels Select)

The ADANSA1.ANSAn bits select or deselect the analog input channels for A/D conversion for AN016 to AN020 (unit 0) and AN116 to AN119 (unit 1). The channels and the number of channels can be set arbitrarily. In unit 0, the ANSA16 bit is associated with AN016 and the ANSA20 bit with AN020. In unit 1, the ANSA16 bit is associated with AN116 and the ANSA19 bit with AN119.

In double-trigger mode, the ANSA1[15:0] bits are invalid, and the channel selected in the ADCSR.DBLANS[15:0] bits is selected in Group A instead.

In group scan mode, do not select the channels specified in A/D Channel Select Register B0 (ADANSB0) and A/D Channel Select Register B1 (ADANSB1).

Only set the ADANSA1 register while the ADCSR.ADST bit is 0.

47.2.4 AD通道选择寄存器A0(ADANSA0)

Address(es): ADC120.ADANSA0 4005 C004h, ADC121.ADANSA0 4005 C204h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	ANSA07	ANSA06	ANSA05	ANSA04	ANSA03	ANSA02	ANSA01	ANSA00
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b7 to b0	ANSA07 to ANSA00	AD转换通道选择	0：不选择关联输入通道1：选择关联输入通道。	R/W
b15 to b8	-	Reserved.	这些位被读取为0。写入值应为0。	R/W

ANSAN位（n=00到07）（AD转换通道选择）

ADANSA0.ANSAN位选择或取消选择用于AN000到AN007（单元0）和AN100到AN103和AN105到AN107（单元1）的AD转换的模拟输入通道。通道和通道数可以任意设置。在单元0中，ANSA00位与AN000相关联，ANSA07位与AN007相关联。在单元1中，ANSA00位与AN100相关联，ANSA07位与AN107相关联。

在双触发模式下，ADANSA0寄存器中选择的通道无效，
改为在A组中选择ADCSR.DBLANS[4:0]位。

在组扫描模式下，不要选择AD通道选择寄存器B0(ADANSB0)和AD中指定的通道
通道选择寄存器B1(ADANSB1)。

仅在ADCSR.ADST位为0时设置ADANSA0寄存器。

47.2.5 AD通道选择寄存器A1(ADANSA1)

Address(es): ADC120.ADANSA1 4005 C006h, ADC121.ADANSA1 4005 C206h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	ANSA20	ANSA19	ANSA18	ANSA17	ANSA16
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b4 to b0	ANSA20 to ANSA16	AD转换通道 Select	0：不选择关联输入通道1：选择关联输入通道	R/W
b15 to b5	—	Reserved	这些位被读取为0。写入值应为0。	R/W

ANSAN位（n=16到20）（AD转换通道选择）

ADANSA1.ANSAN位选择或取消选择用于AN016到AN020（单元0）和AN116到AN119（单元1）的AD转换的模拟输入通道。通道和通道数可以任意设置。在单元0中，ANSA16位与AN016相关联，ANSA20位与AN020相关联。在单元1中，ANSA16位与AN116相关联，ANSA19位与AN119相关联。

双触发模式下，ANSA1[15:0]位无效，ADCSR.DBLANS[15:0]位选择的通道改为A组。

在组扫描模式下，不要选择AD通道选择寄存器B0(ADANSB0)和AD中指定的通道
通道选择寄存器B1(ADANSB1)。

仅在ADCSR.ADST位为0时设置ADANSA1寄存器。

47.2.6 A/D Channel Select Register B0 (ADANSB0)

Address(es): ADC120.ADANSB0 4005 C014h, ADC121.ADANSB0 4005 C214h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	ANSB07	ANSB06	ANSB05	ANSB04	ANSB03	ANSB02	ANSB01	ANSB00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	ANSB07 to ANSB00	A/D Conversion Channels Select	0: Do not select associated input channel 1: Select associated input channel.	R/W
b15 to b8	-	Reserved	These bits are read as 0. The write value should be 0.	R/W

ANSBn bits (n = 00 to 07) (A/D Conversion Channels Select)

The ADANSB0.ANSBn bits select the analog input channels for A/D conversion for AN000 to AN007 (unit 0) and AN100 to AN103 and AN105 to AN107 (unit 1) in Group B in group scan mode. The ADANSB0 register is only used for group scan mode, not for any other modes. Exclude the channels specified in Group A (the channels associated with Group A, selected in the ADANSA0 and ADANSA1 registers and the ADCSR.DBLANS[4:0] bits in double-trigger mode), both the selected channels and the number of channels to be set.

In unit 0, the ANSB00 bit is associated with AN000 and the ANSB07 bit with AN007. In unit 1, the ANSB00 bit is associated with AN100 and the ANSB07 bit with AN107.

Only set the ADANSB0 register while the ADCSR.ADST bit is 0.

47.2.7 A/D Channel Select Register B1 (ADANSB1)

Address(es): ADC120.ADANSB1 4005 C016h, ADC121.ADANSB1 4005 C216h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	ANSB20	ANSB19	ANSB18	ANSB17	ANSB16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b4 to b0	ANSB20 to ANSB16	A/D Conversion Channels Select	0: Do not select associated input channel 1: Select associated input channel.	R/W
b15 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

ANSBn bits (n = 16 to 20) (A/D Conversion Channels Select)

The ADANSB1.ANSBn bits select the analog input channels for A/D conversion for AN016 to AN020 (unit 0) and AN116 to AN119 (unit 1) in Group B in group scan mode. The ADANSB1 register is only used for group scan mode, not for any other modes. Exclude the channels specified in Group A (the channels associated with Group A, selected in the ADANSA0 and ADANSA1 registers and the ADCSR.DBLANS[4:0] bits in double-trigger mode), both the selected channels and the number of channels to be set.

In unit 0, the ANSB16 bit is associated with AN016 and the ANSB20 bit with AN020. In unit 1, the ANSB16 bit is associated with AN116 and the ANSB19 bit with AN119.

Only set the ADANSB1 register bits while the ADST bit is 0.

47.2.6 AD通道选择寄存器B0(ADANSB0)

Address(es): ADC120.ADANSB0 4005 C014h, ADC121.ADANSB0 4005 C214h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	ANSB07	ANSB06	ANSB05	ANSB04	ANSB03	ANSB02	ANSB01	ANSB00
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b7 to b0	ANSB07 to ANSB00	AD转换通道 Select	0：不选择关联输入通道1：选择关联输入通道。	R/W
b15 to b8	-	Reserved	这些位被读取为0。写入值应为0。	R/W

ANSBn位（n=00至07）（AD转换通道选择）

ADANSB0.ANSBn位选择用于AN000到AN007（单元0）的AD转换的模拟输入通道，以及组扫描模式下B组中的AN100到AN103和AN105到AN107（单元1）。ADANSB0寄存器仅用于组扫描模式，不用于任何其他模式。排除A组中指定的通道（与A组关联的通道，在ADANSA0和ADANSA1寄存器以及双触发模式下的ADCSR.DBLANS[4:0]位中选择），选择的通道和要被设置。

在单元0中，ANSB00位与AN000相关联，ANSB07位与AN007相关联。在单元1中，ANSB00位与AN100相关联，ANSB07位与AN107相关联。

仅在ADCSR.ADST位为0时设置ADANSB0寄存器。

47.2.7 AD通道选择寄存器B1(ADANSB1)

Address(es): ADC120.ADANSB1 4005 C016h, ADC121.ADANSB1 4005 C216h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	ANSB20	ANSB19	ANSB18	ANSB17	ANSB16
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b4 to b0	ANSB20 to ANSB16	AD转换通道 Select	0：不选择关联输入通道1：选择关联输入通道。	R/W
b15 to b5	—	Reserved	这些位被读取为0。写入值应为0。	R/W

ANSBn位（n=16至20）（AD转换通道选择）

ADANSB1.ANSBn位选择用于AN016到AN020（单元0）的AD转换的模拟输入通道，以及组扫描模式下B组中的AN116至AN119（单元1）。ADANSB1寄存器仅用于组扫描模式，不用于任何其他模式。排除A组中指定的通道（与A组关联的通道，在ADANSA0和ADANSA1寄存器以及双触发模式下的ADCSR.DBLANS[4:0]位中选择），选择的通道和要被设置。

在单元0中，ANSB16位与AN016相关联，ANSB20位与AN020相关联。在单元1中，ANSB16位与AN116相关联，ANSB19位与AN119相关联。

仅当ADST位为0时设置ADANSB1寄存器位。

47.2.8 A/D-Converted Value Addition/Average Channel Select Register 0 (ADADS0)

Address(es): ADC120.ADADS0 4005 C008h, ADC121.ADADS0 4005 C208h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	ADS07	ADS06	ADS05	ADS04	ADS03	ADS02	ADS01	ADS00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	ADS07 to ADS00	A/D-Converted Value Addition/Average Channel Select	0: Do not select associated input channel 1: Select associated input channel	R/W
b15 to b8	-	Reserved	These bits are read as 0. The write value should be 0.	R/W

ADSn bits (n = 00 to 07) (A/D-Converted Value Addition/Average Channel Select)

When the ADSn bit with the same number as the A/D-converted channel selected in the ANSAn bits (n = 00 to 07) in ADANSA0 or the ADCSR.DBLANS[4:0] bits and the ANSBn bits (n = 00 to 07) in ADANSB0 is set to 1, A/D conversion of the analog input of the selected channels is performed successively 1 to 16 times, as specified in the ADC[2:0] bits in ADADC. When the ADADC.AVEE bit is 0, the value obtained by addition (integration) is stored in the A/D data register. When the ADADC.AVEE bit is 1, the mean value of the results obtained by addition (integration) is stored in the A/D data register. For A/D-converted channels for which addition or average mode is not selected, a normal one-time conversion is executed, and the conversion result is stored in the A/D data register.

In unit 0, the ADS00 bit is associated with AN000 and the ADS07 bit with AN007. In unit 1, the ADS00 bit is associated with AN100 and the ADS07 bit with AN107.

Only set the ADADS0 register bits while the ADCSR.ADST bit is 0.

47.2.9 A/D-Converted Value Addition/Average Channel Select Register 1 (ADADS1)

Address(es): ADC120.ADADS1 4005 C00Ah, ADC121.ADADS1 4005 C20Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	ADS20	ADS19	ADS18	ADS17	ADS16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b4 to b0	ADS20 to ADS16	A/D-Converted Value Addition/Average Channel Select	0: Do not select associated input channel 1: Select associated input channel.	R/W
b15 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

ADSn bits (n = 16 to 20) (A/D-Converted Value Addition/Average Channel Select)

When the ADSn bit with the same number as the A/D-converted channel selected in the ANSAn bits (n = 16 to 20) in ADANSA1 or ADCSR.DBLANS[4:0] bits and ANSBn bits (n = 16 to 20) in ADANSB1 is set to 1, A/D conversion of the analog input of the selected channels is performed successively 1 to 16 times, as specified in the ADC[2:0] bits in ADADC. When the ADADC.AVEE bit is 0, the value obtained by addition (integration) is stored in the A/D data register. When the ADADC.AVEE bit is 1, the mean value of the results obtained by addition (integration) is stored in the A/D data register. For A/D-converted channels for which addition/average mode is not selected, a normal one-time conversion is executed and the conversion result is stored in the A/D data register.

In unit 0, the ADS16 bit is associated with AN016 and the ADS20 bit with AN020. In unit 1, the ADS16 bit is associated with AN116 and the ADS19 bit with AN119.

47.2.8 D转换值加法平均通道选择寄存器0(ADADS0)

Address(es): ADC120.ADADS0 4005 C008h, ADC121.ADADS0 4005 C208h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	ADS07	ADS06	ADS05	ADS04	ADS03	ADS02	ADS01	ADS00
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b7 to b0	ADS07 to ADS00	A/D-Converted Value Addition/Average Channel Select	0：不选择关联输入通道1：选择关联输入通道	R/W
b15 to b8	-	Reserved	这些位被读取为0。写入值应为0。	R/W

ADSn位（n=00到07）（AD转换值加法平均通道选择）

当ADSn位与在ANSAn位(n=00至07)中选择的AD转换通道相同时ADANSA0或ADCSR.DBLANS[4:0]位和ADANSB0中的ANSBn位（n=00至07）设置为1，选定通道的模拟输入的AD转换按规定连续执行1至16次在ADADC的ADC[2:0]位中。当ADADC.AVEE位为0时，加法（积分）得到的值存储在AD数据寄存器中。当ADADC.AVEE位为1时，加法（积分）得到的结果的平均值存储在AD数据寄存器中。对于未选择加法或平均模式的AD转换通道，将执行一次正常的一次性转换，并将转换结果存储在AD数据寄存器中。

在单元0中，ADS00位与AN000相关联，ADS07位与AN007相关联。在单元1中，ADS00位与AN100相关联，ADS07位与AN107相关联。

仅在ADCSR.ADST位为0时设置ADADS0寄存器位。

47.2.9 D转换值加法平均通道选择寄存器1(ADADS1)

Address(es): ADC120.ADADS1 4005 C00Ah, ADC121.ADADS1 4005 C20Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	ADS20	ADS19	ADS18	ADS17	ADS16
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b4 to b0	ADS20 to ADS16	A/D-Converted Value Addition/Average Channel Select	0：不选择关联输入通道1：选择关联输入通道。	R/W
b15 to b5	—	Reserved	这些位被读取为0。写入值应为0。	R/W

ADSn位（n=16至20）（AD转换值加法平均通道选择）

当在ADANSA1或ADCSR.DBLANS[4:0]位和ANSBn位（n=16至20）中选择与AD转换通道相同编号的ADSn位时ADANSB1设置为1，所选通道的模拟输入的AD转换连续执行1到16次，具体由ADADC中的ADC[2:0]位指定。当ADADC.AVEE位为0时，加法（积分）得到的值存储在AD数据寄存器中。当ADADC.AVEE位为1时，加法（积分）得到的结果的平均值存储在AD数据寄存器中。对于未选择加法平均模式的AD转换通道，将执行正常的一次性转换，并将转换结果存储在AD数据寄存器中。

在单元0中，ADS16位与AN016相关联，ADS20位与AN020相关联。在单元1中，ADS16位与AN116相关联，ADS19位与AN119相关联。

Only set the ADADS1 register while the ADCSR.ADST bit is 0.

Figure 47.3 shows a scanning operation sequence in which both the ADADS0.ADS02 and ADS06 bits are set to 1.

In this example, addition mode is selected (ADADS.AVEE = 0), the time conversion is set to 4 (ADADC.ADC[1:0] = 11b), and the AN000 to AN006 channels are selected (ADANSA0.ANSA0[15:0] = 007Fh) in continuous scan mode (ADCSR.ADCS[1:0] = 10b). The conversion process begins with AN000. The AN002 conversion is performed successively 4 times, and the added (integrated) value is returned to A/D data register ADDR2. Next, the AN003 conversion process starts. The AN006 conversion is performed successively 4 times and the added (integrated) value is returned to A/D data register ADDR6. After conversion of AN006, the conversion operation is once again performed in the same sequence from AN000.

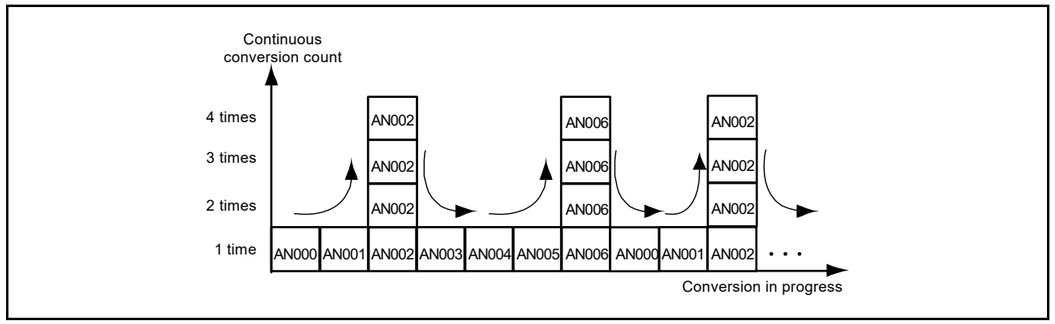


Figure 47.3 Scan conversion sequence with ADADC.ADC[2:0] = 011b, ADADS0.ADS02 = 1, and ADS06 = 1

47.2.10 A/D-Converted Value Addition/Average Count Select Register (ADADC)

Address(es): ADC120.ADADC 4005 C00Ch, ADC121.ADADC 4005 C20Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	AVEE	—	—	—	—	ADC[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	ADC[2:0]	Count Select	b2 b0 0 0 0: 1-time conversion (no addition; same as normal conversion) 0 0 1: 2 time conversion (one addition) 0 1 0: 3-time conversion (two additions) 0 1 1: 4 time conversion (three additions) 1 0 1: 16-time conversion (15 additions). Other settings are prohibited.	R/W
b6 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	AVEE	Average Mode Enable	0: Disable average mode*1 1: Enable average mode.*2	R/W

Note 1. When average mode is deselected by setting the ADADC.AVEE bit to 0, set the addition count to 1, 2, 3, 4 or 16-time conversion. 16-time conversion can only be used with 12-bit accuracy selected.

Note 2. When average mode is selected by setting the ADADC.AVEE bit to 1, set the addition count to 1-, 2-, or 4-time conversion. Do not set the addition count to 3- or 16-time conversion (ADC[2:0] = 010b or 101b).

ADC[2:0] bits (Count Select)

The ADC[2:0] bits set the count for all channels for which A/D conversion and addition/average mode are selected, including the channels selected in double-trigger mode in the ADCSR.DBLANS[4:0] bits. The count also applies to A/D conversion of temperature sensor output and internal reference voltage.

When average mode is selected by setting the ADADC.AVEE bit to 1, do not set the count to 3-time conversion

仅在ADCSR.ADST位为0时设置ADADS1寄存器。

图47.3显示了扫描操作序列，其中ADADS0.ADS02和ADS06位都设置为1。

在本例中，选择了加法模式（ADADS.AVEE=0），时间转换设置为4（ADADC.ADC[1:0]=11b），选择了AN000到AN006通道（ADANSA0.ANSA0[15:0]=007Fh)处于连续扫描模式(ADCSR.ADCS[1:0]=10b)。转换过程从AN000开始。AN002转换连续执行4次，相加（积分）的值返回到AD数据寄存器ADDR2。接下来，AN003转换过程开始。AN006转换连续执行4次，相加（积分）的值返回到AD数据寄存器ADDR6。在AN006转换之后，转换操作从AN000以相同的顺序再次执行。

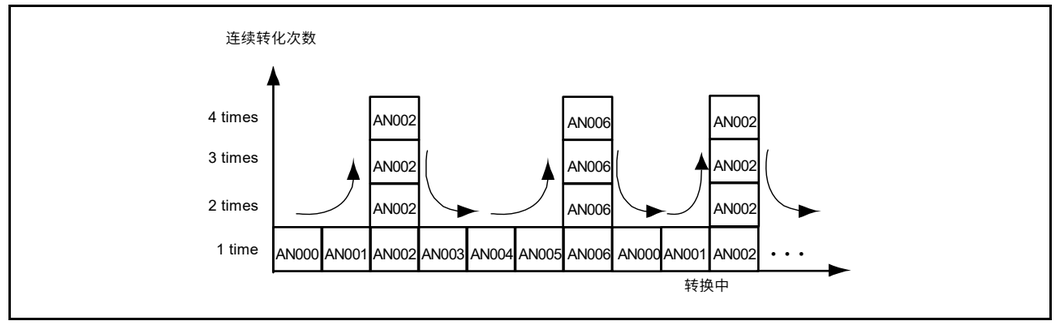


Figure 47.3 使用ADADC.ADC[2:0]=011b、ADADS0.ADS02=1和ADS06=1的扫描转换序列

47.2.10 D转换值加法平均计数选择寄存器(ADADC)

Address(es): ADC120.ADADC 4005 C00Ch, ADC121.ADADC 4005 C20Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	AVEE	—	—	—	—	ADC[2:0]		
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b2 to b0	ADC[2:0]	计数选择	b2 b0 0 0 0：1次转换（不加；同普通转换） 0 0 1：2时间转换（一加） 0 1 0: 3-time conversion (two additions) 0 1 1：4时间转换（三加法） 01：16次转换（15次加法）。禁止其他设置。	R/W
b6 to b3	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b7	AVEE	平均模式启用	0：禁用平均模式*11：启用平均模式。*2	R/W

Note 1. 通过将ADADC.AVEE位设置为0取消选择平均模式时，将加法计数设置为1、2、3、4或16次转换。16次转换只能在选择12位精度的情况下使用。

Note 2. 当通过将ADADC.AVEE位设置为1来选择平均模式时，将加法计数设置为1次、2次或4次转换。不要将加法计数设置为3次或16次转换（ADC[2:0]=010b或101b）。

ADC[2:0]位（计数选择）

ADC[2:0]位设置选择AD转换和加法平均模式的所有通道的计数，包括在ADCSR.DBLANS[4:0]位中以双触发模式选择的通道。该计数也适用于温度传感器输出和内部参考电压的AD转换。

通过将ADADC.AVEE位设置为1选择平均模式时，不要将计数设置为3次转换

(ADADC.ADC[2:0] = 010b). Additionally, the combination of 16-time conversion (ADADC.ADC[2:0] = 101b) with a conversion accuracy setting of 8 or 10 bits (ADCER.ADPRC[1:0] = 10b or 01b) is a prohibited setting, as described in section 47.2.2.

Only set the ADC[2:0] bits while the ADCSR.ADST bit is 0. When self-diagnosis is executed (ADCER.DIAGM = 1), do not set the ADC[2:0] bits to any value other than 000b. When the conversion accuracy is 8 or 10 bits (ADCER.ADPRC[1:0] = 10b or 01b), do not set the ADC[2:0] bits to 101b.

AVEE bit (Average Mode Enable)

The AVEE bit selects addition or average mode for all channels for which A/D conversion and addition/average mode are selected, including the channels selected in double-trigger mode in the ADCSR.DBLANS[4:0] bits, temperature sensor output, and internal reference voltage.

When average mode is selected by setting the ADADC.AVEE bit to 1, do not set the addition count to 3-time conversion (ADADC.ADC[2:0] = 010b).

Only set the AVEE bits while the ADCSR.ADST bit is 0.

47.2.11 A/D Control Extended Register (ADCER)

Address(es): ADC120.ADCER 4005 C00Eh, ADC121.ADCER 4005 C20Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ADRFMT	—	—	—	DIAGM	DIAGLD	DIAGVAL[1:0]		—	—	ACE	—	—	ADPRC[1:0]		—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b2, b1	ADPRC[1:0]	A/D Conversion Accuracy Specify	b2 b1 0 0: 12-bit accuracy 0 1: 10-bit accuracy 1 0: 8-bit accuracy 1 1: Setting prohibited.	R/W
b4, b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b5	ACE	A/D Data Register Automatic Clearing Enable	0: Disable automatic clearing 1: Enable automatic clearing.	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b9, b8	DIAGVAL[1:0]	Self-Diagnosis Conversion Voltage Select	b9 b8 0 0: Setting prohibited when self-diagnosis is enabled 0 1: 0 V 1 0: Reference power supply voltage*1 x 1/2 1 1: Reference power supply voltage.*1	R/W
b10	DIAGLD	Self-Diagnosis Mode Select	0: Select rotation mode for self-diagnosis voltage 1: Select fixed mode for self-diagnosis voltage.	R/W
b11	DIAGM	Self-Diagnosis Enable	0: Disable ADC12 self-diagnosis 1: Enable ADC12 self-diagnosis.	R/W
b14 to b12	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15	ADRFMT	A/D Data Register Format Select	0: Select flush-right for the A/D data register format 1: Select flush-left for the A/D data register format.	R/W

Note 1. The reference voltage refers to VREFH0 for unit 0 and to VREFH for unit 1.

ADPRC[1:0] bits (A/D Conversion Accuracy Specify)

The ADPRC[1:0] bits set the A/D conversion accuracy to 8-, 10-, or 12-bit accuracy. Changing the A/D conversion accuracy also changes the bit width of valid data stored in the result register and the A/D conversion time. For details, see section 47.3.6, Analog Input Sampling and Scan Conversion Time.

（ADADC.ADC[2:0]=010b）。此外，16次转换(ADADC.ADC[2:0]=101b)与8位或10位转换精度设置(ADCER.ADPRC[1:0]=10b或01b)的组合是禁止设置，如第47.2.2节所述。

仅在ADCSR.ADST位为0时设置ADC[2:0]位。执行自诊断时(ADCER.DIAGM=1)，请勿将ADC[2:0]位设置为000b以外的任何值.当转换精度为8位或10位时（ADCER.ADPRC[1:0]=10b或01b），请勿将ADC[2:0]位设置为101b。

AVEE位（平均模式启用）

AVEE位为选择了AD转换和加法平均模式的所有通道选择加法或平均模式，包括在ADCSR.DBLANS[4:0]位、温度传感器输出和内部基准中选择的双触发模式的通道电压。

当通过将ADADC.AVEE位设置为1来选择平均模式时，不要将加法计数设置为3次转换(ADADC.ADC[2:0]=010b)。

仅在ADCSR.ADST位为0时设置AVEE位。

47.2.11 AD控制扩展寄存器(ADCER)

Address(es): ADC120.ADCER 4005 C00Eh, ADC121.ADCER 4005 C20Eh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ADRFMT	—	—	—	DIAGM	DIAGLD	DIAGVAL[1:0]		—	—	ACE	—	—	ADPRC[1:0]		—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	—	Reserved	该位读取为0。写入值应为0。	R/W
b2, b1	ADPRC[1:0]	AD转换精度指定	b2b100：12位精度01：10位精度10：8位精度11：禁止设置。	R/W
b4, b3	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b5	ACE	AD数据寄存器自动清零Enable	0：禁用自动清零1：启用自动清零。	R/W
b7, b6	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b9, b8	DIAGVAL[1:0]	自诊断转换电压Select	b9b800：自诊断有效时禁止设置01：0V10：参考电源电压*1x1211：参考电源电压*1	R/W
b10	DIAGLD	自诊断模式选择	0：自诊断电压选择旋转模式1：自诊断电压选择固定模式。	R/W
b11	DIAGM	Self-Diagnosis Enable	0：禁用ADC12自诊断1：启用ADC12自诊断。	R/W
b14 to b12	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b15	ADRFMT	AD数据寄存器格式选择	0：AD数据寄存器格式选择flush-right1：AD数据寄存器格式选择flush-left。	R/W

Note 1. 参考电压是指单元0的VREFH0和单元1的VREFH。

ADPRC[1:0]位（AD转换精度指定）

ADPRC[1:0]位将AD转换精度设置为8位、10位或12位精度。更改AD转换精度也会更改存储在结果寄存器中的有效数据的位宽和AD转换时间。有关详细信息，请参见第47.3.6节，模拟输入采样和扫描转换时间。

Only set the ADPRC[1:0] bits while the ADCSR.ADST bit is 0.

ACE bit (A/D Data Register Automatic Clearing Enable)

The ACE bit enables or disables automatic clearing (all 0s) of ADDRy, ADRD, ADDBLDR, ADDBLDRA, ADDBLDRB, ADTSDR, or ADOCDR after any of these registers is read by the CPU, DTC, or DMAC. Automatic clearing of the A/D data registers enables detection of failures that do not update the A/D data registers.

DIAGVAL[1:0] bits (Self-Diagnosis Conversion Voltage Select)

The DIAGVAL[1:0] bits select the voltage value used in self-diagnosis fixed voltage mode. For details, see the ADCER.DIAGLD bit description.

Do not execute self-diagnosis by setting the ADCER.DIAGLD bit to 1 when the ADCER.DIAGVAL[1:0] bits are set to 00b.

DIAGLD bit (Self-Diagnosis Mode Select)

The DIAGLD bit selects whether the three voltage values are rotated or fixed voltage is used in self-diagnosis. Setting this bit to 0 allows conversion of the voltages in rotation mode where 0 V, the reference power supply × 1/2, and the reference power supply are converted, in that order. After reset, when the self-diagnosis voltage rotation mode is selected, self-diagnosis is executed from 0 V. The fixed voltage specified in the ADCER.DIAGVAL[1:0] bits is converted when self-diagnosis fixed voltage mode is selected. In self-diagnosis voltage rotation mode, the self-diagnosis voltage value does not return to 0 when scan conversion completes. When scan conversion restarts, rotation starts at the voltage value following the previous value. If fixed mode is switched to rotation mode, rotation starts at the fixed voltage value.

Only set the DIAGLD bit while the ADCSR.ADST bit is 0.

DIAGM bit (Self-Diagnosis Enable)

The DIAGM bit enables or disables self-diagnosis. Self-diagnosis is used to detect a failure of the ADC12. In self-diagnosis mode, one of the internally generated voltage values (0, the reference power supply × 1/2, or the reference power supply) is converted. When conversion completes, information on the converted voltage and the conversion result is stored in the A/D Self-Diagnosis Data Register (ADRD). ADRD can be read by software to determine whether the conversion result falls within the normal range (normal) or not (abnormal). Self-diagnosis is executed once at the beginning of each scan, and one of the three voltages is converted. When the double-trigger mode is set (ADCSR.DBLE = 1), always deselect self-diagnosis (DIAGM = 0). When self-diagnosis is selected in group scan mode, self-diagnosis is executed separately on Group A and Group B.

Only set the DIAGM bit while the ADCSR.ADST bit is 0.

ADRFMT bit (A/D Data Register Format Select)

The ADRFMT bit specifies flush-right or flush-left for the data to be stored in ADDRy, ADDBLDR, ADDBLDRA, ADDBLDRB, ADTSDR, ADOCDR, ADCMPDR0/1, ADWINLLB, ADWINULB, or ADRD.

Only set the ADRFMT bit the ADCSR.ADST bit is 0.

47.2.12 A/D Conversion Start Trigger Select Register (ADSTRGR)

Address(es): ADC120.ADSTRGR 4005 C010h, ADC121.ADSTRGR 4005 C210h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	TRSA[5:0]						—	—	TRSB[5:0]					
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b5 to b0	TRSB[5:0]	A/D Conversion Start Trigger Select for Group B	These bits specify the A/D conversion start trigger for Group B in group scan mode.	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

仅在ADCSR.ADST位为0时设置ADPRC[1:0]位。

ACE位（AD数据寄存器自动清除使能）

ACE位启用或禁用ADDRy、ADRD、ADDBLDR、ADDBLDRA、
在CPU、DTC或DMAC读取任何这些寄存器之后的ADDBLDRB、ADTSDR或ADOCDR。自动清除AD数据寄存器可以检测不更新AD数据寄存器的故障。

DIAGVAL[1:0]位（自诊断转换电压选择）

DIAGVAL[1:0]位选择用于自诊断固定电压模式的电压值。有关详细信息，请参阅ADCER.DIAGLD位描述。

当ADCER.DIAGVAL[1:0]位设置为00b时，不要通过将ADCER.DIAGLD位设置为1来执行自诊断。

DIAGLD位（自诊断模式选择）

DIAGLD位选择是旋转三个电压值还是使用固定电压进行自诊断。将此位设置为0允许在旋转模式下转换电压，其中0V、参考电源×12和参考电源按此顺序转换。Afterreset whentheself-diagnosisvoltagerotationmodeisselected self-diagnosisisexecutedfrom0V.ThefixedvoltagespecifiedintheADCER.DIAGVAL[1:0]bitsisconvertedwhenself-diagnosisfixedvoltagemodeisselected.在自诊断电压旋转模式下，扫描转换完成时自诊断电压值不会返回0。扫描转换重新开始时，从前一个值之后的电压值开始旋转。如果将固定模式切换到旋转模式，则从固定电压值开始旋转。

仅在ADCSR.ADST位为0时设置DIAGLD位。

DIAGM位（自诊断使能）

DIAGM位启用或禁用自诊断。自诊断用于检测ADC12的故障。在自诊断模式下，转换内部产生的电压值之一（0，参考电源×12，或参考电源）。转换完成后，转换电压和转换结果的信息存储在AD自诊断数据寄存器(ADRD)中。ADRD可以通过软件读取来判断转换结果是否在正常范围内（正常）或不在（异常）范围内。自诊断在每次扫描开始时执行一次，并转换三个电压之一。当设置了双触发模式(ADCSR.DBLE=1)时，始终取消选择自诊断(DIAGM=0)。在组扫描模式下选择自诊断时，对A组和B组分别执行自诊断。

仅在ADCSR.ADST位为0时设置DIAGM位。

ADRFMT位（AD数据寄存器格式选择）

ADRFMT位指定要存储在ADDRy、ADDBLDR、ADDBLDRA、
ADDBLDRB, ADTSDR, ADOCDR, ADCMPDR0/1, ADWINLLB, ADWINULB, or ADRD.

仅将ADRFMT位设置为ADCSR.ADST位为0。

47.2.12 AD转换开始触发选择寄存器(ADSTRGR)

Address(es): ADC120.ADSTRGR 4005 C010h, ADC121.ADSTRGR 4005 C210h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	TRSA[5:0]						—	—	TRSB[5:0]					
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b5 to b0	TRSB[5:0]	B组的AD转换开始触发选择	这些位指定AD转换开始触发B组处于组扫描模式。	R/W
b7, b6	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Bit	Symbol	Bit name	Description	R/W
b13 to b8	TRSA[5:0]	A/D Conversion Start Trigger Select	These bits specify the A/D conversion start trigger in single scan mode and continuous mode. In group scan mode, the A/D conversion start trigger for Group A is selected.	R/W
b15, b14	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

TRSB[5:0] bits (A/D Conversion Start Trigger Select for Group B)

The TRSB[5:0] bits select the trigger to start scanning of the analog input selected in Group B. The TRSB[5:0] bits must only be set in group scan mode and are not used in any other scan mode. For the scan conversion start trigger for Group B, setting a software trigger or an asynchronous trigger is prohibited. In group scan mode, set the TRSB[5:0] bits to a value other than 000000b and set the ADCSR.TRGE bit to 1.

When Group A is given priority in group scan mode, setting the ADGSPCR.GBRP bit to 1 allows Group B to continuously operate in single scan mode. When setting the ADGSPCR.GBRP bit to 1, set the TRSB[5:0] bits to 3Fh. The issuance period for a conversion trigger must be more than or equal to the actual scan conversion time (tSCAN). If the issuance period is less than tSCAN, A/D conversion by the trigger might have no effect.

When the trigger from a module operated at 120 MHz (GPT) is selected as an A/D conversion start trigger, a delay for synchronization processing occurs. For details, see section 47.3.6, Analog Input Sampling and Scan Conversion Time.

Table 47.6 lists the A/D conversion startup sources selected in the TRSB[5:0] bits.

TRSA[5:0] bits (A/D Conversion Start Trigger Select)

The TRSA[5:0] bits select the trigger to start A/D conversion in single scan mode and continuous scan mode. In group scan mode, the trigger to start scanning of the analog input selected in Group A is selected. When scanning is executed in group scan mode or double-trigger mode, setting a software trigger or an asynchronous trigger is prohibited.

When using a synchronous trigger (ELC) as the A/D conversion start source, set the TRGE bit in ADCSR to 1 and the EXTRG bit in ADCSR to 0.

When using the asynchronous trigger (ADTRGn), set the TRGE bit in ADCSR to 1 and the EXTRG bit in ADCSR to 1.

The software trigger (ADCSR.ADST) is enabled regardless of the settings in the ADCSR.TRGE bit, the ADCSR.EXTRG bit, or the TRSA[5:0] bits. The issuance period for a conversion trigger must be more than or equal to the actual scan conversion time (tSCAN). If the issuance period is less than tSCAN, A/D conversion by the trigger might have no effect.

When the trigger from a module operated at 120 MHz (GPT) is selected as an A/D conversion start trigger, a delay period for synchronization processing occurs. For details, see section 47.3.6, Analog Input Sampling and Scan Conversion Time.

Table 47.7 lists the A/D conversion start sources selected in the TRSA[5:0] bits.

Table 47.6 Selection of A/D conversion start sources in the TRSB[5:0] bits

Source	Remarks	TRSB[5]	TRSB[4]	TRSB[3]	TRSB[2]	TRSB[1]	TRSB[0]
Trigger source deselected state		1	1	1	1	1	1
ELC_ADC00 (unit 0), ELC_ADC10 (unit 1)	ELC	0	0	1	0	0	1
ELC_ADC01 (unit 0), ELC_ADC11 (unit 1)	ELC	0	0	1	0	1	0
ELC_ADC00/ELC_ADC01 (unit 0) ELC_ADC10/ELC_ADC11 (unit 1)	ELC	0	0	1	0	1	1

Bit	Symbol	位名称	Description	R/W
b13 to b8	TRSA[5:0]	AD转换开始触发选择	这些位指定单次扫描模式和连续模式下的AD转换启动触发。在组扫描模式下，选择A组的AD转换启动触发。	R/W
b15, b14	—	Reserved	这些位被读取为0。写入值应为0。	R/W

TRSB[5:0]位（B组的AD转换开始触发选择）

TRSB[5:0]位选择触发以开始扫描组B中选择的模拟输入。TRSB[5:0]位只能在组扫描模式下设置，不得用于任何其他扫描模式。对于B组的扫描转换开始触发，禁止设置软件触发或异步触发。在组扫描模式下，将TRSB[5:0]位设置为000000b以外的值，并将ADCSR.TRGE位设置为1。

当A组在组扫描模式下具有优先权时，将ADGSPCR.GBRP位设置为1允许B组在单次扫描模式下连续工作。将ADGSPCR.GBRP位设置为1时，将TRSB[5:0]位设置为3Fh。转换触发的发布周期必须大于或等于实际扫描转换时间(tSCAN)。如果发行周期小于tSCAN，触发的AD转换可能无效。

当从120MHz（GPT）操作的模块中选择触发器作为AD转换启动触发器时，会发生同步处理的延迟。有关详细信息，请参见第47.3.6节，模拟输入采样和扫描转换时间。

表47.6列出了在TRSB[5:0]位中选择的AD转换启动源。

TRSA[5:0]位（AD转换开始触发选择）

TRSA[5:0]位选择触发以在单次扫描模式和连续扫描模式下启动AD转换。在组扫描模式下，选择触发开始扫描在组A中选择的模拟输入。在组扫描模式或双触发模式下执行扫描时，禁止设置软件触发或异步触发。

当使用同步触发(ELC)作为AD转换启动源时，将ADCSR中的TRGE位设置为1，然后ADCSR中的EXTRG位为0。

使用异步触发(ADTRGn)时，将ADCSR中的TRGE位设置为1，并将ADCSR中的EXTRG位设置为1。

无论ADCSR.TRGE位的设置如何，软件触发(ADCSR.ADST)都被启用，ADCSR.EXTRG位或TRSA[5:0]位。转换触发的发布周期必须大于或等于实际扫描转换时间(tSCAN)。如果发行周期小于tSCAN，触发的AD转换可能无效。

当从120MHz（GPT）操作的模块中选择触发器作为AD转换启动触发器时，会发生同步处理的延迟期。有关详细信息，请参见第47.3.6节，模拟输入采样和扫描转换时间。

表47.7列出了在TRSA[5:0]位中选择的AD转换启动源。

Table 47.6 在TRSB[5:0]位中选择AD转换起始源

Source	Remarks	TRSB[5]	TRSB[4]	TRSB[3]	TRSB[2]	TRSB[1]	TRSB[0]
触发源取消选择状态		1	1	1	1	1	1
ELC_ADC00 (unit 0), ELC_ADC10 (unit 1)	ELC	0	0	1	0	0	1
ELC_ADC01 (unit 0), ELC_ADC11 (unit 1)	ELC	0	0	1	0	1	0
ELC_ADC00/ELC_ADC01 (unit 0) ELC_ADC10/ELC_ADC11 (unit 1)	ELC	0	0	1	0	1	1

Table 47.7 Selection of A/D activation sources in the TRSA[5:0] bits

Source	Remarks	TRSA[5]	TRSA[4]	TRSA[3]	TRSA[2]	TRSA[1]	TRSA[0]
Trigger source deselected state		1	1	1	1	1	1
ADTRGn	Input pin for the trigger	0	0	0	0	0	0
ELC_ADC00 (unit 0), ELC_ADC10 (unit 1)	ELC	0	0	1	0	0	1
ELC_ADC01 (unit 0), ELC_ADC11 (unit 1)	ELC	0	0	1	0	1	0
ELC_ADC00/ELC_ADC01 (unit 0) ELC_ADC10/ELC_ADC11 (unit 1)	ELC	0	0	1	0	1	1

47.2.13 A/D Conversion Extended Input Control Register (ADEXICR)

Address(es): ADC120.ADEXICR 4005 C012h, ADC121.ADEXICR 4005 C212h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	OCSB	TSSB	OCSA	TSSA	—	—	—	—	—	—	OCSAD	TSSAD
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	TSSAD	Temperature Sensor Output A/D-Converted Value Addition/Average Mode Select	0: Do not select addition/average mode for temperature sensor output 1: Select addition/average mode for temperature sensor output.	R/W
b1	OCSAD	Internal Reference Voltage A/D-Converted Value Addition/Average Mode Select	0: Do not select addition/average mode for internal reference voltage 1: Select addition/average mode for internal reference voltage.	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	TSSA	Temperature Sensor Output A/D Conversion Select	0: Disable A/D conversion of temperature sensor output 1: Enable A/D conversion of temperature sensor output.	R/W
b9	OCSA	Internal Reference Voltage A/D Conversion Select	0: Disable A/D conversion of internal reference voltage 1: Enable A/D conversion of internal reference voltage.	R/W
b10	TSSB	Temperature Sensor Output A/D Conversion Select for Group B	Selection for Group B in group scan mode. 0: Disable A/D conversion of temperature sensor output 1: Enable A/D conversion of temperature sensor output.	R/W
b11	OCSB	Internal Reference Voltage A/D Conversion Select for Group B	Selection for Group B in group scan mode. 0: Disable A/D conversion of internal reference voltage 1: Enable A/D conversion of internal reference voltage.	R/W
b15 to b12	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

TSSAD bit (Temperature Sensor Output A/D-Converted Value Addition/Average Mode Select)

When the TSSAD bit is set to 1, A/D conversion of the temperature sensor output is selected and performed successively the number of times specified in the ADC[2:0] bits in ADADC. The maximum addition count differs depending on the conversion accuracy (see section 47.2.2, A/D Self-Diagnosis Data Register (ADRD)). When the ADADC.AVEE bit is 0, the value obtained by addition (integration) is returned to the A/D Temperature sensor Data Register (ADTSDR). When the ADADC.AVEE bit is 1, the mean value is returned to ADTSDR.

Only set the TSSAD bit while the ADCSR.ADST bit is 0.

Table 47.7 在TRSA[5:0]位中选择AD激活源

Source	Remarks	TRSA[5]	TRSA[4]	TRSA[3]	TRSA[2]	TRSA[1]	TRSA[0]
触发源取消选择状态		1	1	1	1	1	1
ADTRGn	触发器的输入引脚	0	0	0	0	0	0
ELC_ADC00 (unit 0), ELC_ADC10 (unit 1)	ELC	0	0	1	0	0	1
ELC_ADC01 (unit 0), ELC_ADC11 (unit 1)	ELC	0	0	1	0	1	0
ELC_ADC00/ELC_ADC01 (unit 0) ELC_ADC10/ELC_ADC11 (unit 1)	ELC	0	0	1	0	1	1

47.2.13 AD转换扩展输入控制寄存器(ADEXICR)

Address(es): ADC120.ADEXICR 4005 C012h, ADC121.ADEXICR 4005 C212h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	OCSB	TSSB	OCSA	TSSA	—	—	—	—	—	—	OCSAD	TSSAD
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	TSSAD	温度传感器输出AD转换后的增值平均值模式选择	0：温度传感器输出不选择加法平均模式1：温度传感器输出选择加法平均模式。	R/W
b1	OCSAD	内部参考电压AD转换后的增值平均值模式选择	0：内部参考电压不选择加法平均模式1：内部参考电压选择加法平均模式。	R/W
b7 to b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b8	TSSA	温度传感器输出AD转换选择	0：禁止温度传感器输出AD转换1：使能温度传感器输出AD转换。	R/W
b9	OCSA	内部参考电压AD转换选择	0：禁止内部参考电压的AD转换1：使能内部参考电压的AD转换。	R/W
b10	TSSB	温度传感器输出AD B组的转换选择	在组扫描模式下选择B组。0：禁止温度传感器输出AD转换1：使能温度传感器输出AD转换。	R/W
b11	OCSB	B组的内部参考电压AD转换选择	在组扫描模式下选择B组。0：禁止内部参考电压的AD转换1：使能内部参考电压的AD转换。	R/W
b15 to b12	—	Reserved	这些位被读取为0。写入值应为0。	R/W

TSSAD位（温度传感器输出AD转换值加法平均模式选择）

当TSSAD位设置为1时，选择温度传感器输出的AD转换并连续执行ADADC中ADC[2:0]位指定的次数。最大加法计数因转换精度而异（参见第47.2.2节，AD自诊断数据寄存器(ADRD)）。当ADADC.AVEE位为0时，通过加法（积分）获得的值返回到AD温度传感器数据寄存器(ADTSDR)。当ADADC.AVEE位为1时，平均值返回给ADTSDR。

仅在ADCSR.ADST位为0时设置TSSAD位。

OCSAD bit (Internal Reference Voltage A/D-Converted Value Addition/Average Mode Select)

When the OCSAD bit is set to 1, A/D conversion of the internal reference voltage is selected and performed successively the number of times specified in the ADC[2:0] bits in ADADC. The maximum addition count differs depending on the conversion accuracy (see 47.2.2 A/D Self-Diagnosis Data Register (ADRD)). When the ADADC.AVEE bit is 0, the value obtained by addition (integration) is returned to the A/D Internal Reference Voltage Data Register (ADOCDR). When the ADADC.AVEE bit is 1, the mean value is returned to ADOCDR.

Only set the OCSAD bit while the ADCSR.ADST bit is 0.

TSSA bit (Temperature Sensor Output A/D Conversion Select)

The TSSA bit selects A/D conversion of the temperature sensor output for Group A in single scan mode, continuous scan mode, or group scan mode. When A/D conversion of the temperature sensor output is selected and performed, set the ADCSR.DBLE bit to 0.

Only set the TSSA bit while the ADCSR.ADST bit is 0.

OCSA bit (Internal Reference Voltage A/D Conversion Select)

The OCSA bit selects A/D conversion of the internal reference voltage for Group A in single scan mode, continuous scan mode, or group scan mode. When A/D conversion of the internal reference voltage is selected and performed, set the ADCSR.DBLE bit to 0.

Only set the OCSA bit while the ADCSR.ADST bit is 0. In addition, wait for 400 ns or more after the OCSA bit is set to 1 before starting A/D conversion.

TSSB bit (Temperature Sensor Output A/D Conversion Select for Group B)

The TSSB bit selects A/D conversion of the temperature sensor output for Group B in group scan mode.

Only set the TSSB bit while the ADCSR.ADST bit is 0. Do not set the TSSB bit to 1 while the TSSA bit is 1.

OCSB bit (Internal Reference Voltage A/D Conversion Select for Group B)

The OCSB bit selects A/D conversion of the internal reference voltage for Group B in group scan mode.

Only set the OCSB bit while the ADCSR.ADST bit is 0. Do not set the OCSB bit to 1 while the OCSA bit is 1.

Moreover, start the A/D conversion after waiting for 400 ns or more after the OCSB bit is set to 1.

47.2.14 A/D Sampling State Register n (ADSSTRn) (n = 00 to 07, L, T, O)

Address(es): ADC120.ADSSTR00 4005 C0E0h to ADC120.ADSSTR07 4005 C0E7h, ADC120.ADSSTRL 4005 C0DDh, ADC120.ADSSTRT 4005 C0DEh, ADC120.ADSSTRO 4005 C0DFh, ADC121.ADSSTR00 4005 C2E0h to ADC121.ADSSTR03 4005 C2E3h, ADC121.ADSSTR05 4005 C2E5h to ADC121.ADSSTR07 4005 C2E7h, ADC121.ADSSTRL 4005 C2DDh, ADC121.ADSSTRT 4005 C2DEh, ADC121.ADSSTRO 4005 C2DFh

	b7	b6	b5	b4	b3	b2	b1	b0
	SST[7:0]							
Value after reset:	0	0	0	0	1	0	1	1

Bit	Symbol	Bit name	Description	R/W
b7 to b0	SST[7:0]	Sampling Time Setting	These bits set the sampling time in the range from 5 to 255 states.	R/W

The ADSSTRn register sets the sampling time for analog input. If one state is 1 ADCLK (A/D conversion clock) cycle and the ADCLK clock is 60 MHz, one state is 16.7 ns. The initial value is 11 states. The sampling time can be adjusted if the impedance of the analog input signal source is too high to secure sufficient sampling time, or if the ADCLK clock is slow.

Only set the SST[7:0] bits while the ADCSR.ADST bit is 0.

The lower limit of the sampling time setting depends on the frequency ratio, as follows:

- If the frequency ratio of PCLKB to PCLKC(ADCLK) = 1:1, 2:1, 4:1, or 8:1, the sampling time must be set to a

OCSAD位（内部参考电压AD转换值加法平均模式选择）

当OCSAD位设置为1时，选择内部参考电压的AD转换，并按ADADC的ADC[2:0]位指定的次数连续执行。最大加法计数因转换精度而异（参见47.2.2AD自诊断数据寄存器(ADRD)）。当ADADC.AVEE位为0时，通过加法（积分）获得的值返回到AD内部参考电压数据寄存器（ADocDR）。当ADADC.AVEE位为1时，平均值返回给ADOCDR。

仅在ADCSR.ADST位为0时设置OCSAD位。

TSSA位（温度传感器输出AD转换选择）

TSSA位在单次扫描模式、连续扫描模式或组扫描模式下选择A组温度传感器输出的AD转换。WhenADconversionofthetemperaturesensoroutputisselectedandperformed settheADCSR.DBLEbitto0.

仅在ADCSR.ADST位为0时设置TSSA位。

OCSA位（内部参考电压AD转换选择）

OCSA位选择A组内部参考电压在单次扫描模式、连续扫描模式或组扫描模式下的AD转换。WhenADconversionoftheinternalreferencevoltageisselectedandperformed settheADCSR.DBLEbitto0.

仅在ADCSR.ADST位为0时设置OCSA位。此外，在OCSA位设置为1后等待400ns或更长时间，然后再开始AD转换。

TSSB位（B组温度传感器输出AD转换选择）

TSSB位选择组扫描模式下B组温度传感器输出的AD转换。

仅在ADCSR.ADST位为0时设置TSSB位。不要在TSSA位为1时将TSSB位设置为1。

OCSB位（B组的内部参考电压AD转换选择）

OCSB位选择组扫描模式下B组内部参考电压的AD转换。

仅在ADCSR.ADST位为0时设置OCSB位。不要在OCSA位为1时将OCSB位设置为1。

此外，在将OCSB位设置为1后等待400ns或更长时间后开始AD转换。

47.2.14 AD采样状态寄存器n(ADSSTRn)(n=00to07 L T O)

Address(es): ADC120.ADSSTR00 4005 C0E0h to ADC120.ADSSTR07 4005 C0E7h, ADC120.ADSSTRL 4005 C0DDh, ADC120.ADSSTRT 4005 C0DEh, ADC120.ADSSTRO 4005 C0DFh, ADC121.ADSSTR00 4005 C2E0h to ADC121.ADSSTR03 4005 C2E3h, ADC121.ADSSTR05 4005 C2E5h to ADC121.ADSSTR07 4005 C2E7h, ADC121.ADSSTRL 4005 C2DDh, ADC121.ADSSTRT 4005 C2DEh, ADC121.ADSSTRO 4005 C2DFh

	b7	b6	b5	b4	b3	b2	b1	b0
	SST[7:0]							
重置后的值：	0	0	0	0	1	0	1	1

Bit	Symbol	位名称	Description	R/W
b7 to b0	SST[7:0]	采样时间设置	这些位在5到255个状态范围内设置采样时间。	R/W

ADSSTRn寄存器设置模拟输入的采样时间。如果一种状态是1个ADCLK（AD转换时钟）周期并且ADCLK时钟是60MHz，则一种状态是16.7ns。初始值为11个状态。如果模拟输入信号源的阻抗太高而无法保证足够的采样时间，或者如果ADCLK时钟很慢，则可以调整采样时间。

仅在ADCSR.ADST位为0时设置SST[7:0]位。

采样时间设置的下限取决于频率比，如下：

- 如果PCLKB与PCLKC(ADCLK)的频率比=1:1、2:1、4:1或8:1，则必须将采样时间设置为

value of more than 5 states

- If the frequency ratio of PCLKB to PCLKC(ADCLK) = 1:2 or 1:4, the sampling time must be set to a value of more than 6 states.

Table 47.8 shows the relationship between the A/D Sampling State Register and the associated channels.

For details, see section 47.3.6, Analog Input Sampling and Scan Conversion Time.

Table 47.8 Relationship between A/D sampling state register and associated channels

	Associated channels	
Bit name	**Unit 0**	**Unit 1**
ADSSTR00.SST[7:0] bits*1	AN000	AN100
ADSSTR01.SST[7:0] bits	AN001	AN101
ADSSTR02.SST[7:0] bits	AN002	AN102
ADSSTR03.SST[7:0] bits	AN003	AN103
ADSSTR04.SST[7:0] bits	AN004	-
ADSSTR05.SST[7:0] bits	AN005	AN105
ADSSTR06.SST[7:0] bits	AN006	AN106
ADSSTR07.SST[7:0] bits	AN007	AN107
ADSSTRL.SST[7:0] bits	AN016 to AN020	AN116 to AN119
ADSSTRT.SST[7:0] bits	Temperature sensor output	Temperature sensor output
ADSSTRO.SST[7:0] bits	Internal reference voltage	Internal reference voltage

Note 1. When the self-diagnosis function is selected, the sampling time set in the ADSSTR00.SST[7:0] bits is applied.

47.2.15 A/D Sample and Hold Circuit Control Register (ADSHCR)

Address(es): ADC120.ADSHCR 4005 C066h, ADC121.ADSHCR 4005 C266h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	SHANS[2:0]			SSTSH[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	SSTSH[7:0]	Channel-Dedicated Sample-and-Hold Circuit Sampling Time Setting	Sampling time (4 to 255 states).	R/W
b10 to b8	SHANS[2:0]	Channel-Dedicated Sample-and-Hold Circuit Bypass Select	Select whether to use or bypass channel-dedicated sample-and-hold circuits for AN000 to AN002 (unit 0) and AN100 to AN102 (unit 1). 0: Bypass the circuits 1: Use the circuits.	R/W
b15 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

SSTSH[7:0] bits (Channel-Dedicated Sample-and-Hold Circuit Sampling Time Setting)

The SSTSH[7:0] bits set the sampling time for the channel-dedicated sample-and-hold circuits. If one state is 1 ADCLK (A/D conversion clock) cycle and the ADCLK clock is 60 MHz, one state is 16.7 ns. The initial value is 24 states. The sampling time can be adjusted if the impedance of the analog input signal source is too high to secure sufficient sampling time, or if the ADCLK clock is slow.

Only set the SSTSH[7:0] bits while the ADCSR.ADST bit is 0. The sampling time must be set to a value that is 4 states or more and 255 or less.

超过5个州的值

- 如果PCLKB与PCLKC(ADCLK)的频率比=1:2或1:4，则必须将采样时间设置为6个以上状态的值。

表47.8显示了AD采样状态寄存器和相关通道之间的关系。

有关详细信息，请参见第47.3.6节，模拟输入采样和扫描转换时间。

Table 47.8 AD采样状态寄存器与相关通道的关系

	关联频道	
位名称	**Unit 0**	**Unit 1**
ADSSTR00.SST[7:0] bits*1	AN000	AN100
ADSSTR01.SST[7:0] bits	AN001	AN101
ADSSTR02.SST[7:0] bits	AN002	AN102
ADSSTR03.SST[7:0] bits	AN003	AN103
ADSSTR04.SST[7:0] bits	AN004	-
ADSSTR05.SST[7:0] bits	AN005	AN105
ADSSTR06.SST[7:0] bits	AN006	AN106
ADSSTR07.SST[7:0] bits	AN007	AN107
ADSSTRL.SST[7:0] bits	AN016 to AN020	AN116 to AN119
ADSSTRT.SST[7:0] bits	温度传感器输出	温度传感器输出
ADSSTRO.SST[7:0] bits	内部参考电压	内部参考电压

Note 1. 选择自诊断功能时，将应用ADSSTR00.SST[7:0]位中设置的采样时间。

47.2.15 AD采样保持电路控制寄存器(ADSHCR)

Address(es): ADC120.ADSHCR 4005 C066h, ADC121.ADSHCR 4005 C266h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	SHANS[2:0]			SSTSH[7:0]							
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0

Bit	Symbol	位名称	Description	R/W
b7 to b0	SSTSH[7:0]	Channel-Dedicated Sample-and-Hold 电路采样时间设置	采样时间（4到255个状态）。	R/W
b10 to b8	SHANS[2:0]	Channel-Dedicated Sample-and-Hold 电路旁路选择	选择是使用还是绕过AN000至AN002（单元0）和AN100至AN102（单元1）的通道专用采样保持电路。0：绕过电路1：使用电路。	R/W
b15 to b11	—	Reserved	这些位被读取为0。写入值应为0。	R/W

SSTSH[7:0]位（通道专用采样保持电路采样时间设置）

SSTSH[7:0]位设置通道专用采样保持电路的采样时间。如果一种状态是1个ADCLK（AD转换时钟）周期并且ADCLK时钟是60MHz，则一种状态是16.7ns。初始值为24个状态。如果模拟输入信号源的阻抗太高而无法保证足够的采样时间，或者如果ADCLK时钟很慢，则可以调整采样时间。

仅当ADCSR.ADST位为0时设置SSTSH[7:0]位。采样时间必须设置为4个或更多状态且255或更少的值。

SHANS[2:0] bits (Channel-Dedicated Sample-and-Hold Circuit Bypass Select)

The SHANS[2:0] bits select whether to use or bypass the channel-dedicated sample-and-hold circuits for AN000 to AN002 (unit 0) and AN100 to AN102 (unit 1). In unit 0, the SHANS[0] bit is associated with AN000, the SHANS[1] bit with AN001, and the SHANS[2] bit with AN002. In unit 1, the SHANS[0] bit is associated with AN100, the SHANS[1] bit with AN101, and the SHANS[2] bit with AN102.

If any channel from among AN000 to AN002 (unit 0) or AN100 to AD102 (unit 1) is selected for Group B while operation is in group scan mode under Group A priority control, use this setting to bypass the dedicated sample-and-hold circuit of the channel.

Only set the SHANS[2:0] bits while the ADCSR.ADST bit is 0 and the ADSHMSR.SHMD bit is 0.

47.2.16 A/D Sample and Hold Operation Mode Selection Register (ADSHMSR)

Address(es): ADC120.ADSHMSR 4005 C07Ch, ADC121.ADSHMSR 4005 C27Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	SHMD
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	SHMD	Sampling Operation Selection	0: Disable continuous sampling function 1: Enable continuous sampling function.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

SHMD bit (Sampling Operation Selection)

Setting SHMD to 1 enables the constant sampling function of the channel-dedicated sample-and-hold selected in the ADSHCR.SHANS[2:0] bits. Only set the SHMD bit while the ADCSR.ADST bit is 0.

When the sampling function is enabled, the sample-and-hold circuit operates sampling while the ADC12 is not operating, and operates holding while the ADC12 is operating.

Note: The ADCSR.ADST bit must become 1 after 400 ns or more elapses after the SHMD bit is set to 1 (when the permissible signal source impedance is 1 kΩ). The sampling period of the sample-and-hold circuit must be 400 ns or more (when the permissible signal source impedance is 1 kΩ).

47.2.17 A/D Disconnection Detection Control Register (ADDISCR)

Address(es): ADC120.ADDISCR 4005 C07Ah, ADC121.ADDISCR 4005 C27Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	PCHG	ADNDIS[3:0]			
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	ADNDIS[3:0]	Disconnection Detection Assist Setting	b3 - b0 0000: The disconnection detection assist function is disabled 0001: Setting prohibited Others: The number of states for the discharge or precharge period.	R/W
b4	PCHG	Precharge/discharge select	0: Discharge 1: Precharge.	R/W

SHANS[2:0]位（通道专用采样保持电路旁路选择）

SHANS[2:0]位选择是使用还是绕过AN000的通道专用采样保持电路
AN002（单元0）和AN100到AN102（单元1）。在单元0中，SHANS[0]位与AN000相关联，SHANS[1]位与AN001相关联，SHANS[2]位与AN002相关联。在单元1中，SHANS[0]位与AN100相关联，SHANS[1]位与AN101相关联，SHANS[2]位与AN102相关联。

如果在A组优先控制下的组扫描模式下为组B选择AN000至AN002（单元0）或AN100至AD102（单元1）中的任何通道，则使用此设置绕过专用采样保持通道的电路。

仅在ADCSR.ADST位为0且ADSHMSR.SHMD位为0时设置SHANS[2:0]位。

47.2.16 AD采样和保持操作模式选择寄存器(ADSHMSR)

Address(es): ADC120.ADSHMSR 4005 C07Ch, ADC121.ADSHMSR 4005 C27Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	SHMD
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	SHMD	采样操作选择	0：禁用连续采样功能1：启用连续采样功能。	R/W
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

SHMD位（采样操作选择）

将SHMD设置为1启用在
ADSHCR.SHANS[2:0]位。仅在ADCSR.ADST位为0时设置SHMD位。

当采样功能使能时，采样保持电路在ADC12不工作时进行采样，在ADC12工作时进行保持。

Note: ADCSR.ADST位必须在SHMD位设置为1后经过400ns或更长时间后变为1（当允许的信号源阻抗为1kΩ时）。采样保持电路的采样周期必须为400ns或更长（当允许的信号源阻抗为1kΩ时）。

47.2.17 AD断线检测控制寄存器(ADDISCR)

Address(es): ADC120.ADDISCR 4005 C07Ah, ADC121.ADDISCR 4005 C27Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	PCHG	ADNDIS[3:0]			
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b3 to b0	ADNDIS[3:0]	断线检测辅助 Setting	b3b00000：断线检测辅助功能无效0001：设定禁止其他：放电或预充电期间的状态数。	R/W
b4	PCHG	Precharge/discharge select	0: Discharge 1: Precharge.	R/W

Bit	Symbol	Bit name	Description	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The ADDISCR register selects either precharge or discharge, and the period of precharge or discharge for the A/D disconnection detection assist function. Only set the ADDISCR register when the ADCSR.ADST bit is 0.

If any of the following functions are used, the disconnection detection assist function must be disabled:

- The temperature sensor
- The internal reference voltage
- A/D self-diagnosis
- The programmable gain amplifier without bypass enabled.

ADNDIS[3:0] bits (Disconnection Detection Assist Setting)

The ADNDIS[3:0] bits specify the period of precharge or discharge. When ADNDIS[3:0] = 0000b, the disconnection detection assist function is disabled. Setting the ADNDIS[3:0] bits to 0001b is prohibited. Except when ADNDIS[3:0] = 0000b or 0001b, the specified value indicates the number of states for the period of precharge or discharge. When the ADNDIS[3:0] bits are set to any values other than 0000b or 0001b, the disconnection detection assistance function is enabled.

PCHG bit (Precharge/discharge select)

Setting the PCHG bit to 1 selects precharge and setting the PCHG bit to 0 selects discharge.

47.2.18 A/D Group Scan Priority Control Register (ADGSPCR)

Address(es): ADC120.ADGSPCR 4005 C080h, ADC121.ADGSPCR 4005 C280h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	GBRP	—	—	—	—	—	—	—	—	—	—	—	—	—	GBRSCN	PGS
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	PGS	Group A Priority Control Setting*1	0: Operate without Group A priority control 1: Operate with Group A priority control.	R/W
b1	GBRSCN	Group B Restart Setting	(Enabled only when PGS = 1. Reserved when PGS = 0.) 0: Do not restart Group B scanning after it is stopped by Group A priority control 1: Restart Group B scanning after it is stopped by Group A priority control.	R/W
b14 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15	GBRP	Group B Single Scan Continuous Start*2	(Enabled only when PGS = 1. Reserved when PGS = 0.) 0: Do not continuously activate single scan for Group B 1: Continuously activate single scan for Group B.	R/W

Note 1. The ADCSR.ADCS[1:0] bits must be set to 01b (group scan mode) before setting PGS to 1. Operation is not guaranteed if these bits are set to any other value.
Note 2. When the GBRP bit is set to 1, single scan is performed continuously for Group B regardless of the setting in the GBRSCN bit.

PGS bit (Group A Priority Control Setting)

Set the PGS bit to 1 to give priority to operation on Group A. The ADCSR.ADCS[1:0] bits must be set to 01b (group scan mode) before setting the PGS bit to 1. Operation is not guaranteed if the bits are set to any other value.

When the PGS bit is set to 0, a clear operation must be performed by software as described in section 47.6.2, Constraints

Bit	Symbol	位名称	Description	R/W
b7 to b5	—	Reserved	这些位被读取为0。写入值应为0。	R/W

ADDISCR寄存器选择预充电或放电，以及AD断线检测辅助功能的预充电或放电周期。仅当ADCSR.ADST位为0时设置ADDISCR寄存器。

如果使用以下任何功能，则必须禁用断线检测辅助功能：

- 温度传感器
- 内部参考电压
- A/D self-diagnosis
- 未启用旁路的可编程增益放大器。

ADNDIS[3:0]位（断线检测辅助设置）

ADNDIS[3:0]位指定预充电或放电周期。当ADNDIS[3:0]=0000b时，断线检测辅助功能被禁用。禁止将ADNDIS[3:0]位设置为0001b。除了ADNDIS[3:0]=0000b或0001b时，指定值表示预充电或放电期间的状态数。当ADNDIS[3:0]位设置为0000b或0001b以外的任何值时，将启用断线检测辅助功能。

PCHG位（预充电放电选择）

将PCHG位设置为1选择预充电，将PCHG位设置为0选择放电。

47.2.18 AD组扫描优先控制寄存器(ADGSPCR)

Address(es): ADC120.ADGSPCR 4005 C080h, ADC121.ADGSPCR 4005 C280h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	GBRP	—	—	—	—	—	—	—	—	—	—	—	—	—	GBRSCN	PGS
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	PGS	A组优先控制 Setting*1	0：无A组优先控制运行1：有A组优先控制运行。	R/W
b1	GBRSCN	B组重启设置	（仅在PGS=1时有效。PGS=0时保留。）0：B组扫描被A组优先控制停止后不重新启动1：B组扫描被A组优先控制停止后重新启动。	R/W
b14 to b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b15	GBRP	B组单次扫描连续 Start*2	（仅在PGS=1时启用。在PGS=0时保留。）0：不连续激活B组单次扫描1：连续激活B组单次扫描。	R/W

注1.ADCSR.ADCS[1:0]位必须在PGS设置为1之前设置为01b（组扫描模式）。如果这些位设置为任何其他值，则无法保证操作。注2.当GBRP位设置为1时，对B组连续执行单次扫描，而与

GBRSCN bit.

PGS位（A组优先控制设置）

将PGS位设置为1以优先对组A进行操作。在将PGS位设置为1之前，必须将ADCSR.ADCS[1:0]位设置为01b（组扫描模式）。如果这些位不保证操作设置为任何其他值。

当PGS位设置为0时，必须由软件执行清除操作，如第47.6.2节，约束中所述

on Stopping A/D Conversion. When the PGS bit is set to 1, use the settings described in section 47.3.4.3, Operation with group A priority control.

GBRSCN bit (Group B Restart Setting)

The GBRSCN bit controls the restarting of scan operation on Group B when operation on Group A is given priority. If a scan operation on Group B is stopped by a Group A trigger input with the GBRSCN bit set to 1, the scan operation is restarted on completion of the Group A conversion. Also, if a Group B trigger is input during A/D conversion on Group A, the scan operation on Group B is restarted on completion of Group A conversion.

When the GBRSCN bit is set to 0, triggers input during A/D conversion are ignored. Only set the GBRSCN bit while the ADCSR.ADST bit is 0.

The setting in the GBRSCN bit is valid when the PGS bit is 1.

GBRP bit (Group B Single Scan Continuous Start)

Set the GBRP bit to perform a single scan operation continuously on Group B. Setting the GBRP bit to 1 starts a single scan on Group B. On completion of the scan, another single scan on Group B starts automatically. If a Group B conversion stops because of an operation on Group A, the Group A operation takes priority, and single scan on Group B restarts automatically on completion of the Group A conversion.

Disable Group B trigger input before setting the GBRP bit to 1. Setting the GBRP bit to 1 invalidates the setting in the GBRSCN bit. Only set the GBRP bit while the ADCSR.ADST is 0.

The setting in the GBRP bit is valid when the PGS bit is 1.

47.2.19 A/D Compare Function Control Register (ADCMPCR)

Address(es): ADC120.ADCMPCR 4005 C090h, ADC121.ADCMPCR 4005 C290h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CMPAIE	WCMPE	CMPBIE	—	CMPAE	—	CMPBE	—	—	—	—	—	—	—	CMPAB[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	CMPAB[1:0]	Window A/B Composite Conditions Setting	b1 b0 0 0: Output ADC12i_WCMPM when Window A OR Window B comparison conditions are met; otherwise, output ADC12i_WCMPUM 0 1: Output ADC12i_WCMPM when Window A EXOR Window B comparison conditions are met; otherwise, output ADC12i_WCMPUM 1 0: Output ADC12i_WCMPM when Window A AND Window B comparison conditions are met; otherwise, output ADC12i_WCMPUM 1 1: Setting prohibited. These bits are valid when both Window A and Window B are enabled (CMPAE = 1 and CMPBE = 1).	R/W
b8 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b9	CMPBE	Compare Window B Operation Enable	0: Disable compare Window B operation Disable ADC12i_WCMPM and ADC12i_WCMPUM outputs. 1: Enable compare Window B operation.	R/W
b10	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b11	CMPAE	Compare Window A Operation Enable	0: Disable compare Window A operation Disable ADC12i_WCMPM and ADC12i_WCMPUM outputs. 1: Enable compare Window A operation.	R/W
b12	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

关于停止AD转换。当PGS位设置为1时，使用第47.3.4.3节“A组优先控制操作”中描述的设置。

GBRSCN位（B组重启设置）

当A组操作优先时，GBRSCN位控制B组扫描操作的重新启动。如果通过将GBRSCN位设置为1的A组触发输入停止B组的扫描操作，则在A组转换完成后重新开始扫描操作。此外，如果在A组的AD转换期间输入B组触发，则在A组转换完成时重新开始B组的扫描操作。

当GBRSCN位设置为0时，AD转换期间的触发输入将被忽略。仅设置GBRSCN位，而ADCSR.ADST位为0。

当PGS位为1时GBRSCN位中的设置有效。

GBRP位（B组单次扫描连续启动）

设置GBRP位以在B组上连续执行单次扫描操作。将GBRP位设置为1将启动B组的单次扫描。扫描完成后，自动开始B组上的另一次单次扫描。如果由于对A组的操作而导致B组转换停止，则A组操作优先，并且B组的单次扫描会在A组转换完成后自动重新启动。

在将GBRP位设置为1之前禁用B组触发输入。将GBRP位设置为1会使GBRSCN位。仅在ADCSR.ADST为0时设置GBRP位。

GBRP位中的设置在PGS位为1时有效。

47.2.19 AD比较功能控制寄存器(ADCMPCR)

Address(es): ADC120.ADCMPCR 4005 C090h, ADC121.ADCMPCR 4005 C290h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CMPAIE	WCMPE	CMPBIE	—	CMPAE	—	CMPBE	—	—	—	—	—	—	—	CMPAB[1:0]	
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b1, b0	CMPAB[1:0]	窗口AB复合条件设定	b1 b0 0 0：当窗口AOR窗口B比较条件满足时，输出ADC12i_WCMPM；否则，输出ADC12i_WCMPUM 0 1：当WindowAEXORWindowB比较条件满足时输出ADC12i_WCMPM；否则，输出ADC12i_WCMPUM 1 0：当WindowAANDWindowB比较条件满足时输出ADC12i_WCMPM；否则，输出ADC12i_WCMPUM 11：禁止设置。当窗口A和窗口B都使能（CMPAE=1和CMPBE=1）时，这些位有效。	R/W
b8 to b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b9	CMPBE	比较窗口B操作启用	0：禁止比较窗口B操作 禁用ADC12i_WCMPM和ADC12i_WCMPUM输出。1：启用比较窗口B操作。	R/W
b10	—	Reserved	该位读取为0。写入值应为0。	R/W
b11	CMPAE	比较窗口A操作启用	0：禁止比较窗口A操作 禁用ADC12i_WCMPM和ADC12i_WCMPUM输出。1：启用比较窗口A操作。	R/W
b12	—	Reserved	该位读取为0。写入值应为0。	R/W

Bit	Symbol	Bit name	Description	R/W
b13	CMPBIE	Compare B Interrupt Enable	0: Disable ADC12i_CMPBI interrupt when comparison conditions (Window B) are met 1: Enable ADC12i_CMPBI interrupt when comparison conditions (Window B) are met.	R/W
b14	WCMPE	Window Function Setting	0: Disable window function Window A and Window B operate as a comparator to compare the single value on the lower side with the A/D conversion result. 1: Enable window function. Window A and Window B operate as a comparator to compare the two values on the upper and lower sides with the A/D conversion result.	R/W
b15	CMPAIE	Compare A Interrupt Enable	0: Disable ADC12i_CMPAI interrupt when comparison conditions (Window A) are met 1: Enable ADC12i_CMPAI interrupt when comparison conditions (Window A) are met.	R/W

Note: i = 0: unit 0, i = 1: unit 1.

CMPAB[1:0] bits (Window A/B Composite Conditions Setting)

The CMPAB[1:0] bits are valid when both Window A and Window B are enabled (CMPAE = 1 and CMPBE = 1) in single scan mode. These bits specify the compare function match/mismatch event output conditions and monitoring conditions of ADWINMON.MONCONB.

Only set the CMPAB[1:0] bits while the ADCSR.ADST bit is 0.

CMPBE bit (Compare Window B Operation Enable)

The CMPBE bit enables or disables the compare Window B operation. Set the CMPBE bit while the ADCSR.ADST bit is 0.

Set this bit to 0 before setting the following registers:

- A/D Channel Select Registers A0, A1, B0, and B1 (ADANSA0, ADANSA1, ADANSB0, and ADANSB1)
- OCSB, TSSB, OCSA, or TSSA bits in the A/D Conversion Extended Input Control Register (ADEXICR)
- CMPCHB[5:0] bits in the Window B Channel Select Register (ADCMPBNSR).

CMPAE bit (Compare Window A Operation Enable)

The CMPAE bit enables or disables the compare Window A operation. Set the CMPAE bit while the ADCSR.ADST bit is 0.

Set this bit to 0 before setting the following registers:

- A/D Channel Select Registers A0, A1, B0, and B1 (ADANSA0, ADANSA1, ADANSB0, and ADANSB1)
- OCSB, TSSB, OCSA, or TSSA bits in the A/D Conversion Extended Input Control Register (ADEXICR)
- Window A Channel Select Registers 0 and 1 (ADCMPANSR0 and ADCMPANSR1)
- Window A Extended Input Select Register (ADCMPANSER)

CMPBIE bit (Compare B Interrupt Enable)

The CMPBIE bit enables or disables the ADC12i_CMPBI (i = 0, 1) interrupt output when the comparison conditions (Window B) are met.

WCMPE bit (Window Function Setting)

The WCMPE bit enables or disables the window function. Set the WCMPE bit while the ADCSR.ADST bit is 0.

CMPAIE bit (Compare A Interrupt Enable)

The CMPAIE bit enables or disables the ADC12i_CMPAI (i = 0, 1) interrupt output when the comparison conditions (Window A) are met.

Bit	Symbol	位名称	Description	R/W
b13	CMPBIE	比较B中断 Enable	0：当比较条件（窗口B）满足时禁止ADC12i_CMPBI中断1：当比较条件（窗口B）满足时，使能ADC12i_CMPBI中断。	R/W
b14	WCMPE	窗口功能设置	0：关闭窗口功能 窗口A和窗口B用作比较器，将下侧的单个值与AD转换结果进行比较。1：启用窗口功能。 窗口A和窗口B用作比较器，将上下两个值与AD转换结果进行比较。	R/W
b15	CMPAIE	比较中断 Enable	0：当比较条件（窗口A）满足时禁止ADC12i_CMPAI中断1：当比较条件（窗口A）满足时，使能ADC12i_CMPAI中断。	R/W

Note: i = 0: unit 0, i = 1: unit 1.

CMPAB[1:0]位（窗口AB复合条件设置）

当窗口A和窗口B在单次扫描模式下启用（CMPAE=1和CMPBE=1）时，CMPAB[1:0]位有效。这些位指定比较函数匹配不匹配事件输出条件和ADWINMON.MONCONB的监视条件。

仅在ADCSR.ADST位为0时设置CMPAB[1:0]位。

CMPBE位（比较窗口B操作使能）

CMPBE位启用或禁用比较窗口B操作。当ADCSR.ADST位为0时设置CMPBE位。

在设置以下寄存器之前将此位设置为0：

- AD通道选择寄存器A0、A1、B0和B1（ADANSA0、ADANSA1、ADANSB0和ADANSB1）
- AD转换扩展输入控制寄存器(ADEXICR)中的OCSB、TSSB、OCSA或TSSA位
- 窗口B通道选择寄存器(ADCMPBNSR)中的CMPCHB[5:0]位。

CMPAE位（比较窗口A操作使能）

CMPAE位启用或禁用比较窗口A操作。当ADCSR.ADST位为0时设置CMPAE位。

在设置以下寄存器之前将此位设置为0：

- AD通道选择寄存器A0、A1、B0和B1（ADANSA0、ADANSA1、ADANSB0和ADANSB1）
- AD转换扩展输入控制寄存器(ADEXICR)中的OCSB、TSSB、OCSA或TSSA位
- 窗口A通道选择寄存器0和1（ADCMPANSR0和ADCMPANSR1）
- 窗口A扩展输入选择寄存器(ADCMPANSER)

CMPBIE位（比较B中断使能）

当满足比较条件（窗口B）时，CMPBIE位启用或禁用ADC12i_CMPBI(i=0 1)中断输出。

WCMPE位（窗口功能设置）

WCMPE位启用或禁用窗口功能。当ADCSR.ADST位为0时设置WCMPE位。

CMPAIE位（比较中断使能）

当满足比较条件（窗口A）时，CMPAIE位启用或禁用ADC12i_CMPAI(i=0 1)中断输出。

47.2.20 A/D Compare Function Window A Channel Select Register 0 (ADCMPANSR0)

Address(es): ADC120.ADCMPANSR0 4005 C094h, ADC121.ADCMPANSR0 4005 C294h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	CMPCHA07	CMPCHA06	CMPCHA05	CMPCHA04	CMPCHA03	CMPCHA02	CMPCHA01	CMPCHA00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	CMPCHA07 to CMPCHA00	Compare Window A Channel Select	0: Disable compare function for associated input channel 1: Enable compare function for associated input channel In unit 0, bit [7] (CMPCHA07) is associated with to AN007 and bit 0 (CMPCHA00) with AN000. In unit 1, bit [7] (CMPCHA07) is associated with AN107 and bit 0 (CMPCHA00) with AN100.	R/W
b15 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

CMPCHAn bits (n = 00 to 07) (Compare Window A Channel Select)

The compare function is enabled by writing 1 to the CMPCHAn bit with the same number as the A/D conversion channel selected in the ADANSA0.ANSAn bits (n = 00 to 07) and the ADANSB0.ANSBn bits (n = 00 to 07).

Set the CMPCHAn bits while the ADCSR.ADST bit is 0.

47.2.21 A/D Compare Function Window A Channel Select Register 1 (ADCMPANSR1)

Address(es): ADC120.ADCMPANSR1 4005 C096h, ADC121.ADCMPANSR1 4005 C296h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	CMPCHA20	CMPCHA19	CMPCHA18	CMPCHA17	CMPCHA16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b4 to b0	CMPCHA20 to CMPCHA16	Compare Window A Channel Select	0: Disable compare function for associated input channel 1: Enable compare function for associated input channel. In unit 0, bit 4 (CMPCHA20) is associated with AN020 and bit 0 (CMPCHA16) with AN016. In unit 1, bit [3] (CMPCHA19) is associated with AN119 and bit 0 (CMPCHA16) with AN116.	R/W
b15 to b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

CMPCHAn bits (n = 16 to 20) (Compare Window A Channel Select)

The compare function is enabled by writing 1 to the CMPCHAn bit with the same number as the A/D conversion channel selected in the ADANSA1.ANSAn bits (n = 16 to 20) and the ADANSB1.ANSBn bits (n = 16 to 20).

Set the CMPCHAn bits while the ADCSR.ADST bit is 0.

47.2.20 AD比较功能窗口A通道选择寄存器0(ADCMPANSR0)

Address(es): ADC120.ADCMPANSR0 4005 C094h, ADC121.ADCMPANSR0 4005 C294h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	CMPCHA07	CMPCHA06	CMPCHA05	CMPCHA04	CMPCHA03	CMPCHA02	CMPCHA01	CMPCHA00
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b7 to b0	CMPCHA07 to CMPCHA00	比较窗口A通道 Select	0：禁用关联输入通道的比较功能1：启用关联输入通道的比较功能在单元0中，位[7](CMPCHA07)与AN007关联，位0(CMPCHA00)与AN000关联。在单元1中，位[7](CMPCHA07)与AN107相关联，位0(CMPCHA00)与AN100相关联。	R/W
b15 to b8	—	Reserved	这些位被读取为0。写入值应为0。	R/W

CMPCHAn位（n=00至07）（比较窗口A通道选择）

通过向CMPCHAn位写入1来启用比较功能，该位与在ADANSA0.ANSAn位（n=00到07）和ADANSB0.ANSBn位（n=00到07）中选择的AD转换通道的编号相同。

当ADCSR.ADST位为0时，设置CMPCHAn位。

47.2.21 AD比较功能窗口A通道选择寄存器1(ADCMPANSR1)

Address(es): ADC120.ADCMPANSR1 4005 C096h, ADC121.ADCMPANSR1 4005 C296h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	CMPCHA20	CMPCHA19	CMPCHA18	CMPCHA17	CMPCHA16
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b4 to b0	CMPCHA20 to CMPCHA16	比较窗口A通道 Select	0：禁用关联输入通道的比较功能1：启用关联输入通道的比较功能。在单元0中，位4(CMPCHA20)与AN020相关联，位0(CMPCHA16)与AN016相关联。在单元1中，位[3](CMPCHA19)与AN119相关联，位0(CMPCHA16)与AN116相关联。	R/W
b15 to b6	—	Reserved	这些位被读取为0。写入值应为0。	R/W

CMPCHAn位（n=16至20）（比较窗口A通道选择）

通过向CMPCHAn位写入1来启用比较功能，该位与在ADANSA1.ANSAN位（n=16至20）和ADANSB1.ANSBn位（n=16至20）中选择的AD转换通道的编号相同。

当ADCSR.ADST位为0时，设置CMPCHAn位。

47.2.22 A/D Compare Function Window A Extended Input Select Register (ADCMPANSER)

Address(es): ADC120.ADCMPANSER 4005 C092h, ADC121.ADCMPANSER 4005 C292h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	CMPOCA	CMPTSA
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	CMPTSA	Temperature Sensor Output Compare Select	0: Exclude the temperature sensor output from the compare Window A target range 1: Include the temperature sensor output in the compare Window A target range.	R/W
b1	CMPOCA	Internal Reference Voltage Compare Select	0: Exclude the internal reference voltage from the compare Window A target range. 1: Include the internal reference voltage in the compare Window A target range.	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

CMPTSA bit (Temperature Sensor Output Compare Select)

The compare Window A function is enabled by setting the CMPTSA bit to 1 while the ADEXICR.TSSA bit or the ADEXICR.TSSB bit is 1. Set the CMPTSA bit while the ADCSR.ADST bit is 0.

CMPOCA bit (Internal Reference Voltage Compare Select)

The compare Window A function is enabled by setting the CMPOCA bit to 1 while the ADEXICR.OCSA bit or the ADEXICR.OCSB bit is 1. Set the CMPOCA bit while the ADCSR.ADST bit is 0.

47.2.23 A/D Compare Function Window A Comparison Condition Setting Register 0 (ADCMPLR0)

Address(es): ADC120.ADCMPLR0 4005 C098h, ADC121.ADCMPLR0 4005 C298h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	CMPLCHA07	CMPLCHA06	CMPLCHA05	CMPLCHA04	CMPLCHA03	CMPLCHA02	CMPLCHA01	CMPLCHA00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	CMPLCHA07 to CMPLCHA00	Compare Window A Comparison Condition Select	These bits set comparison conditions for channels to which Window A comparison conditions are applied, selected from AN000 to AN007 (unit 0) and AN100 to AN103, AN105 to AN107 (unit 1). Comparison conditions are shown in Figure 47.4. • When window function is disabled (ADCMPCR.WCMPE = 0) 0: ADCMPDR0 value > A/D-converted value 1: ADCMPDR0 value < A/D-converted value. • When window function is enabled (ADCMPCR.WCMPE = 1) 0: A/D-converted value < ADCMPDR0 value, or ADCMPDR1 value < A/D-converted value 1: ADCMPDR0 value < A/D-converted value < ADCMPDR1 value.	R/W
b15 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

47.2.22 AD比较功能窗口A扩展输入选择寄存器(ADCMPANSER)

Address(es): ADC120.ADCMPANSER 4005 C092h, ADC121.ADCMPANSER 4005 C292h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	CMPOCA	CMPTSA
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	CMPTSA	温度感应器输出比较选择	0：将温度传感器输出排除在比较窗口A目标范围之外1：将温度传感器输出包括在比较窗口A目标范围内。	R/W
b1	CMPOCA	内部参考电压比较选择	0：将内部参考电压排除在比较窗口A目标范围之外。1：在比较窗口A目标范围内包含内部参考电压。	R/W
b7 to b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W

CMPTSA位（温度传感器输出比较选择）

比较窗口A功能通过将CMPTSA位设置为1而ADEXICR.TSSA位或ADXICR.TSSB位为1。在ADCSR.ADST位为0时设置CMPTSA位。

CMPOCA位（内部参考电压比较选择）

比较窗口A功能通过将CMPOCA位设置为1而ADEXICR.OCSA位或ADXICR.OCSB位为1。在ADCSR.ADST位为0时设置CMPOCA位。

47.2.23 AD比较功能窗口A比较条件设置寄存器0(ADCMPLR0)

Address(es): ADC120.ADCMPLR0 4005 C098h, ADC121.ADCMPLR0 4005 C298h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	CMPLCHA07	CMPLCHA06	CMPLCHA05	CMPLCHA04	CMPLCHA03	CMPLCHA02	CMPLCHA01	CMPLCHA00
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b7 to b0	CMPLCHA07 to CMPLCHA00	比较窗口A比较条件Select	这些位设置窗口的通道的比较条件 应用比较条件，从AN000中选择到AN007（单元0）和AN100至AN103、AN105至AN107（单元1）。比较条件如图47.4所示。 禁用窗口功能时(ADCMPCR.WCMPE=0)0：ADCMPDR0值>AD转换值1：ADCMPDR0值<AD转换值。 启用窗口功能时(ADCMPCR.WCMPE=1)0：D转换值<ADCMPDR0值，或ADCMPDR1值<AD转换值1：ADCMPDR0值<AD转换值<ADCMPDR1值。	R/W
b15 to b8	—	Reserved	这些位被读取为0。写入值应为0。	R/W

CMPLCHAn bits (n = 00 to 07) (Compare Window A Comparison Condition Select)

The CMPLCHAn bits specify the comparison conditions for channels to which Window A comparison conditions are applied, selected from AN000 to AN007 (unit 0) and AN100 to AN103, AN105 to AN107 (unit 1). These bits can be set for each analog input to be compared. In unit 0, CMPLCHA00 is associated with AN000 and CMPLCHA07 with AN007. In unit 1, CMPLCHA00 is associated with AN100 and CMPLCHA07 with AN107. When the comparison result of each analog input meets the set condition, the ADCMPSR0.CMPSTCHAn flag sets to 1 and a compare interrupt (ADC12i_CMPAI (i = 0, 1)) is generated.

Comparison conditions when the window function is disabled

CMPLCHAn = 0		CMPLCHAn = 1	
ADCMPDR0 value ≤ A/D converted value	Not met	ADCMPDR0 value < A/D converted value	Met
ADCMPDR0 value > A/D converted value	Met	ADCMPDR0 value ≥ A/D converted value	Not met

Comparison conditions when the window function is enabled

CMPLCHAn = 0	
ADCMPDR1 value < A/D converted value	Met
ADCMPDR0 value ≤ A/D converted value ≤ ADCMPDR1 value	Not met
A/D converted value < ADCMPDR0 value	Met

CMPLCHAn = 1	
ADCMPDR1 value ≤ A/D converted value	Not met
ADCMPDR0 value < A/D converted value < ADCMPDR1 value	Met
A/D converted value ≤ ADCMPDR0 value	Not met

Figure 47.4 Explanation of comparison conditions for compare function Window A

CMPLCHAn位（n=00到07）（比较窗口A比较条件选择）

CMPLCHAn位指定应用窗口A比较条件的通道的比较条件，从AN000到AN007（单元0）和AN100到AN103、AN105到AN107（单元1）中选择。可以为要比较的每个模拟输入设置这些位。在单元0中，CMPLCHA00与AN000相关联，CMPLCHA07与AN007相关联。在单元1中，CMPLCHA00与AN100相关联，CMPLCHA07与AN107相关联。当每个模拟输入的比较结果满足设置条件时，ADCMPSR0.CMPSTCHAn标志设置为1，并产生比较中断(ADC12i_CMPAI(i=0 1))。

禁用窗口功能时的比较条件

CMPLCHAn = 0		CMPLCHAn = 1	
ACMPDDR0值　AD转换值	没见过	ACMPDDR0值<AD转换值	Met
ACMPDDR0值>AD转换值	Met	ACMPDDR0值　AD转换值	没见过

启用窗口功能时的比较条件

CMPLCHAn = 0	
ADCMPDDR1值<AD转换值	Met
ADCMPDR0值　AD转换值　ADCMPDR1值	没见过
AD转换值<ADCMPDR0值	Met

CMPLCHAn = 1	
ACMPDDR1值　AD转换值	没见过
ADCMPDR0值<AD转换值<ADCMPDR1值	Met
AD转换值　ADCMPDR0值	没见过

Figure 47.4 比较功能窗口A的比较条件说明

47.2.24 A/D Compare Function Window A Comparison Condition Setting Register 1 (ADCMPLR1)

Address(es): ADC120.ADCMPLR1 4005 C09Ah, ADC121.ADCMPLR1 4005 C29Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	CMPLCHA20	CMPLCHA19	CMPLCHA18	CMPLCHA17	CMPLCHA16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b4 to b0	CMPLCHA20 to CMPLCHA16	Compare Window A Comparison Condition Select	These bits set comparison conditions for channels to which Window A comparison conditions are applied, selected from AN016 to AN020 (unit 0) and AN116 to AN119 (unit 1). Comparison conditions are shown in Figure 47.4. • When window function is disabled (ADCMPCR.WCMPE = 0) 0: ADCMPDR0 value > A/D-converted value 1: ADCMPDR0 value < A/D-converted value. • When window function is enabled (ADCMPCR.WCMPE = 1) 0: A/D-converted value < ADCMPDR0 value, or ADCMPDR1 value < A/D-converted value 1: ADCMPDR0 value < A/D-converted value < ADCMPDR1 value.	R/W
b15 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

CMPLCHAn bits (n = 16 to 20) (Compare Window A Comparison Condition Select)

The CMPLCHAn bits specify the comparison conditions for channels to which Window A comparison conditions are applied, selected from AN016 to AN020 (unit 0) and AN116 to AN119 (unit 1). These bits can be set for each analog input to be compared. In unit 0, CMPLCHA16 is associated with AN016 and CMPLCHA20 with AN020. In unit 1, CMPLCHA16 is associated with AN116 and CMPLCHA19 with AN119. When the comparison result of each analog input meets the set condition, the ADCMPSR1.CMPSTCHAn flag sets to 1 and a compare interrupt (ADC12i_CMPAI (i = 0, 1)) is generated.

47.2.25 A/D Compare Function Window A Extended Input Comparison Condition Setting Register (ADCMPLER)

Address(es): ADC120.ADCMPLER 4005 C093h, ADC121.ADCMPLER 4005 C293h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	CMPLOCA	CMPLTSA
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	CMPLTSA	Compare Window A Temperature Sensor Output Comparison Condition Select	Comparison conditions are shown in Figure 47.4. • When window function is disabled (ADCMPCR.WCMPE = 0) 0: ADCMPDR0 value > A/D-converted value 1: ADCMPDR0 value < A/D-converted value. • When window function is enabled (ADCMPCR.WCMPE = 1) 0: A/D-converted value < ADCMPDR0 value, or A/D-converted value > ADCMPDR1 value 1: ADCMPDR0 value < A/D-converted value < ADCMPDR1 value.	R/W.

47.2.24 AD比较功能窗口A比较条件设置寄存器1(ADCMPLR1)

Address(es): ADC120.ADCMPLR1 4005 C09Ah, ADC121.ADCMPLR1 4005 C29Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	CMPLCHA20	CMPLCHA19	CMPLCHA18	CMPLCHA17	CMPLCHA16
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b4 to b0	CMPLCHA20 to CMPLCHA16	比较窗口A比较条件Select	这些位设置应用窗口A比较条件的通道的比较条件，从AN016到AN020（单元0）和AN116到AN119（单元1）中选择。比较条件如图47.4所示。 禁用窗口功能时(ADCMPCR.WCMPE=0)0：ADCMPDR0值>AD转换值1：ADCMPDR0值<AD转换值。 启用窗口功能时(ADCMPCR.WCMPE=1)0：D转换值<ADCMPDR0值，或ADCMPDR1值<AD转换值1：ADCMPDR0值<AD转换值<ADCMPDR1值。	R/W
b15 to b5	—	Reserved	这些位被读取为0。写入值应为0。	R/W

CMPLCHAn位（n=16到20）（比较窗口A比较条件选择）

CMPLCHAn位指定应用窗口A比较条件的通道的比较条件，从AN016到AN020（单元0）和AN116到AN119（单元1）中选择。可以为要比较的每个模拟输入设置这些位。在单元0中，CMPLCHA16与AN016相关联，CMPLCHA20与AN020相关联。在单元1中，CMPLCHA16与AN116相关联，CMPLCHA19与AN119相关联。当每个模拟输入的比较结果满足设置条件时，ADCMPSR1.CMPSTCHAn标志设置为1，并产生比较中断(ADC12i_CMPAI(i=0 1))。

47.2.25 AD比较功能窗口A扩展输入比较条件设置寄存器(ADCMPLER)

Address(es): ADC120.ADCMPLER 4005 C093h, ADC121.ADCMPLER 4005 C293h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	CMPLOCA	CMPLTSA
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	CMPLTSA	比较窗口A温度传感器输出比较条件选择	比较条件如图47.4所示。 禁用窗口功能时(ADCMPCR.WCMPE=0)0：ADCMPDR0值>AD转换值1：ADCMPDR0值<AD转换值。 启用窗口功能时(ADCMPCR.WCMPE=1)0：D转换值<ADCMPDR0值，或D转换值>ADCMPDR1值1：ADCMPDR0值<AD转换值<ADCMPDR1值。	R/W.

Bit	Symbol	Bit name	Description	R/W
b1	CMPLOCA	Compare Window A Internal Reference Voltage Comparison Condition Select	Comparison conditions are shown in Figure 47.4. • When window function is disabled (ADCMPCR.WCMPE = 0) 0: ADCMPDR0 register value > A/D-converted value 1: ADCMPDR0 register value < A/D-converted value. • When window function is enabled (ADCMPCR.WCMPE = 1) 0: A/D-converted value < ADCMPDR0 register value, or A/D-converted value > ADCMPDR1 register value 1: ADCMPDR0 register value < A/D-converted value < ADCMPDR1 register value.	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R

CMPLTSA bit (Compare Window A Temperature Sensor Output Comparison Condition Select)

The CMPLTSA bit specifies comparison conditions when the temperature sensor output is the target for the Window A comparison condition. When the temperature sensor output comparison result meets the set condition, the ADCMPSER.CMPSTTSA flag sets to 1 and a compare interrupt (ADC12i_CMPAI (i = 0, 1)) is generated.

CMPLOCA bit (Compare Window A Internal Reference Voltage Comparison Condition Select)

The CMPLOCA bit specifies comparison conditions when the internal reference voltage is the target for the Window A comparison condition. When the internal reference voltage comparison result meets the set condition, the ADCMPSER.CMPSTOCA flag sets to 1 and a compare interrupt (ADC12i_CMPAI) is generated.

47.2.26 A/D Compare Function Window A Lower-Side Level Setting Register (ADCMPDR0), A/D Compare Function Window A Upper-Side Level Setting Register (ADCMPDR1), A/D Compare Function Window B Lower-Side Level Setting Register (ADWINLLB), A/D Compare Function Window B Upper-Side Level Setting Register (ADWINULB)

Address(es): ADC120.ADCMPDR0 4005 C09Ch, ADC120.ADCMPDR1 4005 C09Eh, ADC120.ADWINLLB 4005 C0A8h, ADC120.ADWINULB 4005 C0AAh, ADC121.ADCMPDR0 4005 C29Ch, ADC121.ADCMPDR1 4005 C29Eh, ADC121.ADWINLLB 4005 C2A8h, ADC121.ADWINULB 4005 C2AAh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b15 to b0	—	—	Reference value	R/W

The ADCMPDRy (y = 0,1) register specifies the reference data when the compare Window A function is used. ADCMPDR0 sets the lower reference for Window A, and ADCMPDR1 sets the upper reference for Window A.

ADWINULB and ADWINLLB specify the reference data when the compare Window B function is used. ADWINLLB sets the lower reference for Window B, and ADWINULB sets the upper reference for Window B. The ADCMPDRy, ADWINULB, and ADWINLLB are read/write registers.

ADCMPDRy, ADWINULB, and ADWINLLB can be written to even during A/D conversion. The reference data can be dynamically changed by rewriting register values during A/D conversion.

Set these registers so that the upper reference is not less than the lower reference (ADCMPDR1 ≥ ADCMPDR0 and ADWINULBB ≥ ADWINLLB). ADCMPDR1 and ADWINULB are not used when the window function is disabled.

The lower and the upper references are changed when each register is written. For example, when the upper reference value is changed and the lower reference value is being changed, the MCU compares the upper reference (after a rewrite), and the lower reference (before a rewrite) with the A/D conversion result. (See Figure 47.5.) If the comparison during the rewriting of these two references is erroneous, then rewrite these reference values when both ADCSR.ADST

Bit	Symbol	位名称	Description	R/W
b1	CMPLOCA	比较窗口A内部参考电压比较条件选择	比较条件如图47.4所示。 当窗口功能禁用时(ADCMPCR.WCMPE=0)0：ADCMPDR0寄存器值>AD转换值1：ADCMPDR0寄存器值<AD转换值。 启用窗口功能时(ADCMPCR.WCMPE=1)0：D转换值<ADCMPDR0寄存器值，或D转换值>ADCMPDR1寄存器值1：ADCMPDR0寄存器值<AD转换值<ADCMPDR1寄存器值.	R/W
b7 to b2	—	Reserved	这些位被读取为0。写入值应为0。	R

CMPLTSA位（比较窗口A温度传感器输出比较条件选择）

当温度传感器输出是窗口A比较条件的目标时，CMPLTSA位指定比较条件。当温度传感器输出比较结果满足设置条件时，ADCMPSER.CMPSTTSA标志设置为1，并产生比较中断(ADC12i_CMPAI(i=0 1))。

CMPLOCA位（比较窗口A内部参考电压比较条件选择）

当内部参考电压是窗口A比较条件的目标时，CMPLOCA位指定比较条件。当内部参考电压比较结果满足设置条件时，ADCMPSER.CMPSTOCA标志设置为1，并产生比较中断(ADC12i_CMPAI)。

47.2.26 AD比较功能窗口A低端电平设置寄存器(ADCMPDR0) AD比较功能窗口A高端电平设置寄存器(ADCMPDR1) AD比较功能窗口B低端电平设置寄存器(ADWINLLB) AD比较功能窗口B上侧电平设置寄存器(ADWINULB)

Address(es): ADC120.ADCMPDR0 4005 C09Ch, ADC120.ADCMPDR1 4005 C09Eh, ADC120.ADWINLLB 4005 C0A8h, ADC120.ADWINULB 4005 C0AAh, ADC121.ADCMPDR0 4005 C29Ch, ADC121.ADCMPDR1 4005 C29Eh, ADC121.ADWINLLB 4005 C2A8h, ADC121.ADWINULB 4005 C2AAh

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b15 to b0	—	—	参考值	R/W

ADCMPDRy(y=0 1)寄存器指定使用比较窗口A功能时的参考数据。ADCMPDDR0设置窗口A的参考下限，ADCMPDR1设置窗口A的参考上限。

ADWINULB和ADWINLLB指定使用比较窗口B功能时的参考数据。ADWINLLB设置窗口B的下参考，ADWINULB设置窗口B的上参考。ADCMPDRy、ADWINULB和ADWINLLB是读写寄存器。

ADCMPDRy、ADWINULB和ADWINLLB即使在AD转换期间也可以写入。参考数据可以通过在AD转换期间重写寄存器值来动态更改。

设置这些寄存器，使参考上限不小于参考下限（ADCMPDR1 ADCMPDR0和ADWINULBB ADWINLLB）。禁用窗口功能时不使用ACMPDDR1和ADWINULB。

写入每个寄存器时会更改下参考和上参考。例如，当上参考值改变和下参考值改变时，MCU将上参考（重写后）和下参考（重写前）与AD转换结果进行比较。（参见图47.5。）如果在重写这两个引用期间的比较是错误的，那么当两个ADCSR.ADST都重写这些引用值时

and the associated compare window operation enable bit (ADCMPCR.CMPAE or ADCMPCR.CMPBE) is 0.

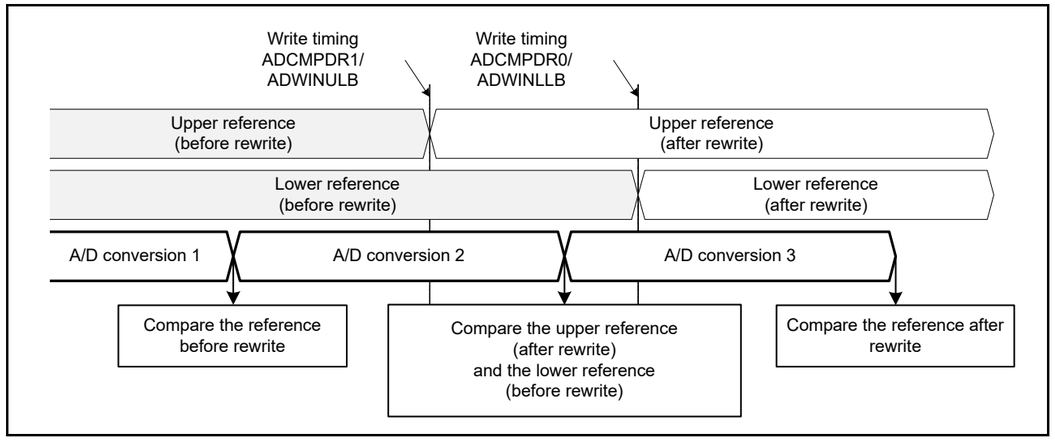


Figure 47.5 Comparison between upper and lower references before and after a rewrite

The ADCMPDRy, ADWINLLB, and ADWINULB registers use different formats depending on the following conditions:

- The value in the A/D Data Register Format Select bit (flush-right or flush-left)
- The value in the A/D Conversion Accuracy Specify bit (12-bit, 10-bit, or 8-bit)
- The value in the A/D-Converted Value Addition/Average Channel Select bits (A/D-converted value addition mode selected or not selected).

The data formats for each condition are as follows:

(1) When A/D-converted value addition mode is not selected

- Flush-right data with 12-bit accuracy: Lower 12 bits ([11:0]) are valid
- Flush-right data with 10-bit accuracy: Lower 10 bits ([9:0]) are valid
- Flush-right data with 8-bit accuracy: Lower 8 bits ([7:0]) are valid
- Flush-left data with 12-bit accuracy: Upper 12 bits ([15:4]) are valid
- Flush-left data with 10-bit accuracy: Upper 10 bits ([15:6]) are valid
- Flush-left data with 8-bit accuracy: Upper 8 bits ([15:8]) are valid.

(2) When A/D-converted value addition mode is selected

- Flush-right data with 12-bit accuracy: Lower 14 bits ([13:0]) are valid
- Flush-right data with 10-bit accuracy: Lower 12 bits ([11:0]) are valid
- Flush-right data with 8-bit accuracy: Lower 10 bits ([9:0]) are valid
- Flush-left data with 12-bit accuracy: Upper 14 bits ([15:2]) are valid
- Flush-left data with 10-bit accuracy: Upper 12 bits ([15:4]) are valid
- Flush-left data with 8-bit accuracy: Upper 10 bits ([15:6]) are valid.

并且相关的比较窗口操作使能位（ADCMPCR.CMPAE或ADCMPCR.CMPBE）为0。

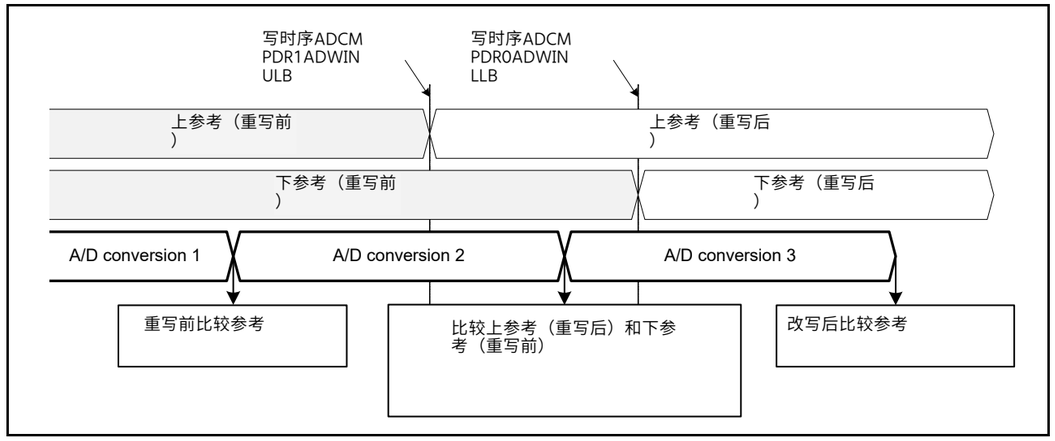


Figure 47.5 重写前后上下引用的比较

ADCMPDRy、ADWINLLB和ADWINULB寄存器根据以下条件使用不同的格式：

- AD数据寄存器格式选择位中的值（右对齐或左对齐）
- AD转换精度指定位（12位、10位或8位）中的值
- AD转换值加法平均通道选择位中的值（选择或未选择AD转换值加法模式）。

每个条件的数据格式如下：

(1) 未选择AD转换值相加模式时

- 12位精度的右冲洗数据：低12位([11:0])有效
- 10位精度的右冲洗数据：低10位([9:0])有效
- 8位精度的右冲洗数据：低8位([7:0])有效
- 12位精度的左刷新数据：高12位([15:4])有效
- 10位精度的左刷新数据：高10位([15:6])有效
- 8位精度的左刷新数据：高8位([15:8])有效。

(2) 选择AD转换值相加模式时

- 12位精度的右冲洗数据：低14位([13:0])有效
- 10位精度的右冲洗数据：低12位([11:0])有效
- 8位精度的右冲洗数据：低10位([9:0])有效
- 12位精度的左刷新数据：高14位([15:2])有效
- 10位精度的左刷新数据：高12位([15:4])有效
- 8位精度的左刷新数据：高10位([15:6])有效。

47.2.27 A/D Compare Function Window A Channel Status Register 0 (ADCMPSR0)

Address(es): ADC120.ADCMPSR0 4005 C0A0h, ADC121.ADCMPSR0 4005 C2A0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	CMPSTCHA07	CMPSTCHA06	CMPSTCHA05	CMPSTCHA04	CMPSTCHA03	CMPSTCHA02	CMPSTCHA01	CMPSTCHA00
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	CMPSTCHA07 to CMPSTCHA00	Compare Window A Flag	When Window A operation is enabled (ADCMPCR.CMPAE = 1b), these bits indicate the comparison result of channels to which Window A comparison conditions are applied, selected from AN000 to AN007 (unit 0) and AN100 to AN103, AN105 to AN107 (unit 1). 0: Comparison conditions are not met 1: Comparison conditions are met.	R/W
b15 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

CMPSTCHAn flags (n = 00 to 07) (Compare Window A Flag)

The CMPSTCHAn flags indicate the comparison results for channels to which Window A comparison conditions are applied, selected from AN000 to AN007 (unit 0) and AN100 to AN103, AN105 to AN107 (unit 1). When a comparison condition set in ADCMPLR0.CMPLCHAn is met at the end of A/D conversion, the associated CMPSTCHAn flag sets to 1. When the ADCMPCR.CMPAIE bit is 1, a compare interrupt request (ADC12i_CMPAI (i = 0, 1)) is generated when this flag sets to 1. In unit 0, CMPSTCHA00 is associated with AN000 and CMPSTCHA07 with AN007. In unit 1, CMPSTCHA00 is associated with AN100 and CMPSTCHA07 with AN107.

Writing 1 to the CMPSTCHAn flags is invalid.

[Setting condition]

- The condition set in ADCMPLR0.CMPLCHAn is met when ADCMPCR.CMPAE = 1.

[Clearing condition]

- Writing 0 after reading 1.

47.2.28 A/D Compare Function Window A Channel Status Register1 (ADCMPSR1)

Address(es): ADC120.ADCMPSR1 4005 C0A2h, ADC121.ADCMPSR1 4005 C2A2h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	CMPSTCHA20	CMPSTCHA19	CMPSTCHA18	CMPSTCHA17	CMPSTCHA16
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b4 to b0	CMPSTCHA20 to CMPSTCHA16	Compare Window A Flag	When Window A operation is enabled (ADCMPCR.CMPAE = 1), these bits indicate the comparison result of channels to which Window A comparison conditions are applied, selected from AN016 to AN020 (unit 0) and AN116 to AN119 (unit 1). 0: Comparison conditions are not met 1: Comparison conditions are met.	R/W
b15 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

CMPSTCHAn flags (n = 16 to 20) (Compare Window A Flag)

The CMPSTCHAn flags indicate the comparison results for channels to which Window A comparison conditions are applied, selected from AN016 to AN020 (unit 0) and AN116 to AN119 (unit 1). When the comparison condition set in

47.2.27 AD比较功能窗口A通道状态寄存器0(ADCMPSR0)

Address(es): ADC120.ADCMPSR0 4005 C0A0h, ADC121.ADCMPSR0 4005 C2A0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	CMPSTCHA07	CMPSTCHA06	CMPSTCHA05	CMPSTCHA04	CMPSTCHA03	CMPSTCHA02	CMPSTCHA01	CMPSTCHA00
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b7 to b0	CMPSTCHA07 to CMPSTCHA00	比较窗口A标志	当窗口A操作使能时（ADCMPCR.CMPAE=1b），这些位指示应用窗口A比较条件的通道的比较结果，从 AN000到AN007（单元0）和AN100到AN103、AN105到AN107（单元1）。0：不满足比较条件1：满足比较条件。	R/W
b15 to b8	—	Reserved	这些位被读取为0。写入值应为0。	R/W

CMPSTCHAn标志（n=00到07）（比较窗口A标志）

CMPSTCHAn标志指示应用窗口A比较条件的通道的比较结果，从AN000到AN007（单元0）和AN100到AN103、AN105到AN107（单元1）中选择。当ADCMPLR0.CMPLCHAn中设置的比较条件在AD转换结束时满足，相关的CMPSTCHAn标志设置为1。当ADCMPCR.CMPAIE位为1时，比较中断请求(ADC12i_CMPAI(i=0 1))为当该标志设置为1时生成。在单元0中，CMPSTCHA00与AN000相关联，CMPSTCHA07与AN007相关联。在单元1中，CMPSTCHA00与AN100相关联，CMPSTCHA07与AN107相关联。

将1写入CMPSTCHAn标志是无效的。

[Setting condition]

- 当ADCMPCR.CMPAE=1时，满足ADCMPLR0.CMPLCHAn中设置的条件。

[Clearing condition]

- 读1后写0。

47.2.28 AD比较功能窗口A通道状态寄存器1(ADCMPSR1)

Address(es): ADC120.ADCMPSR1 4005 C0A2h, ADC121.ADCMPSR1 4005 C2A2h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	CMPSTCHA20	CMPSTCHA19	CMPSTCHA18	CMPSTCHA17	CMPSTCHA16
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b4 to b0	CMPSTCHA20 to CMPSTCHA16	比较窗口A标志	当窗口A操作使能时（ADCMPCR.CMPAE=1），这些位指示应用窗口A比较条件的通道的比较结果，从 AN016至AN020（单元0）和AN116至AN119（单元1）。0：不满足比较条件1：满足比较条件。	R/W
b15 to b5	—	Reserved	这些位被读取为0。写入值应为0。	R/W

CMPSTCHAn标志（n=16到20）（比较窗口A标志）

CMPSTCHAn标志指示应用窗口A比较条件的通道的比较结果，从AN016到AN020（单元0）和AN116到AN119（单元1）中选择。当比较条件设置在

ADCMPLR1.CMPLCHAn is met at the end of A/D conversion, the associated CMPSTCHAn flag sets to 1. When the ADCMPCR.CMPAIE bit is 1, a compare interrupt request (ADC12i_CMPAI (i = 0, 1)) is generated when this flag sets to 1. In unit 0, CMPSTCHA16 is associated with AN016 and CMPSTCHA20 with AN020. In unit 1, CMPSTCHA16 is associated with AN116 and CMPSTCHA19 with AN119.

Writing 1 to the CMPSTCHAn flags is invalid.

[Setting condition]

- The condition set in ADCMPLR1.CMPLCHAn is met when ADCMPCR.CMPAE = 1.

[Clearing condition]

- Writing 0 after reading 1.

47.2.29 A/D Compare Function Window A Extended Input Channel Status Register (ADCMPSER)

Address(es): ADC120.ADCMPSER 4005 C0A4h, ADC121.ADCMPSER 4005 C2A4h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	CMPSTOCA	CMPSTTSA
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	CMPSTTSA	Compare Window A Temperature Sensor Output Compare Flag	When Window A operation is enabled (ADCMPCR.CMPAE = 1), this bit indicates the temperature sensor output comparison result. 0: Comparison conditions are not met. 1: Comparison conditions are met.	R/W
b1	CMPSTOCA	Compare Window A Internal Reference Voltage Compare Flag	When Window A operation is enabled (ADCMPCR.CMPAE = 1), this bit indicates the internal reference voltage comparison result. 0: Comparison conditions are not met. 1: Comparison conditions are met.	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

CMPSTTSA flag (Compare Window A Temperature Sensor Output Compare Flag)

The CMPSTTSA flag indicates the temperature sensor output comparison result. When the comparison condition set in ADCMPLER.CMPLTSA is met at the end of A/D conversion, this flag sets to 1. When the ADCMPCR.CMPAIE bit is 1, a compare interrupt request (ADC12i_CMPAI (i = 0, 1)) is generated when this flag sets to 1.

Writing 1 to the CMPSTTSA flag is invalid.

[Setting condition]

- The condition set in ADCMPLER.CMPLTSA is met when ADCMPCR.CMPAE = 1.

[Clearing condition]

- Writing 0 after reading 1.

CMPSTOCA flag (Compare Window A Internal Reference Voltage Compare Flag)

The CMPSTOCA flag indicates the internal reference voltage comparison result. When the comparison condition set in ADCMPLER.CMPLOCA is met at the end of A/D conversion, this flag sets to 1. When the ADCMPCR.CMPAIE bit is 1, a compare interrupt request (ADC12i_CMPAI) is generated when this flag sets to 1.

Writing 1 to the CMPSTOCA flag is invalid.

[Setting condition]

- The condition set in ADCMPLER.CMPLOCA is met when ADCMPCR.CMPAE = 1.

ADCMPLR1.CMPLCHAn在AD转换结束时满足，相关的CMPSTCHAn标志设置为1。当ADCMPCR.CMPAIE位为1时，当该标志设置为1.在单元0中，CMPSTCHA16与AN016相关联，CMPSTTCHA20与AN020相关联。在单元1中，CMPSTCHA16与AN116相关联，CMPSTTCHA19与AN119相关联。

将1写入CMPSTCHAn标志是无效的。

[Setting condition]

- 当ADCMPCR.CMPAE=1时，满足ADCMPLR1.CMPLCHAn中设置的条件。

[Clearing condition]

- 读1后写0。

47.2.29 AD比较功能窗口A扩展输入通道状态寄存器(ADCMPSER)

Address(es): ADC120.ADCMPSER 4005 C0A4h, ADC121.ADCMPSER 4005 C2A4h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	CMPSTOCA	CMPSTTSA
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	CMPSTTSA	比较窗口A 温度传感器输出比较标志	当窗口A操作使能（ADCMPCR.CMPAE=1）时，该位指示温度传感器输出比较结果。0：不满足比较条件。1：满足比较条件。	R/W
b1	CMPSTOCA	比较窗口A内部参考电压比较 Flag	当窗口A操作使能时（ADCMPCR.CMPAE=1），该位指示内部参考电压比较结果。0：不满足比较条件。1：满足比较条件。	R/W
b7 to b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W

CMPSTTSA标志（比较窗口A温度传感器输出比较标志）

CMPSTTSA标志指示温度传感器输出比较结果。当ADCMPLER.CMPLTSA中设置的比较条件在AD转换结束时满足，该标志设置为1。当ADCMPCR.CMPAIE位为1时，产生比较中断请求(ADC12i_CMPAI(i=0 1))此标志设置为1。

将1写入CMPSTTSA标志无效。

[Setting condition]

- 当ADCMPCR.CMPAE=1时，满足ADCMPLER.CMPLTSA中设置的条件。

[Clearing condition]

- 读1后写0。

CMPSTOCA标志（比较窗口A内部参考电压比较标志）

CMPSTOCA标志指示内部参考电压比较结果。当ADCMPLER.CMPLOCA中设置的比较条件在AD转换结束时满足，该标志设置为1。当ADCMPCR.CMPAIE位为1时，当该标志设置为1时产生比较中断请求(ADC12i_CMPAI)。

将1写入CMPSTOCA标志无效。

[Setting condition]

- 当ADCMPCR.CMPAE=1时，满足ADCMPLER.CMPLOCA中设置的条件。

[Clearing condition]

- Writing 0 after reading 1.

47.2.30 A/D Compare Function Window B Channel Select Register (ADCMPBNSR)

Address(es): ADC120.ADCMPBNSR 4005 C0A6h, ADC121.ADCMPBNSR 4005 C2A6h

	b7	b6	b5	b4	b3	b2	b1	b0
	CMPLB	—	CMPCHB[5:0]					
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b5 to b0	CMPCHB[5:0]	Compare Window B Channel Select	These bits select channels to be compared with the compare Window B conditions. The maximum channel is AN020 in unit 0 and AN119 in unit 1. b5 b0 Unit 0 Unit 1 0 0 0 0 0 0: AN000 AN100 0 0 0 0 0 1: AN001 AN101 0 0 0 0 1 0: AN002 AN102 0 0 0 0 1 1: AN003 AN103 0 0 0 1 0 0: AN004 — 0 0 0 1 0 1: AN005 AN105 0 0 0 1 1 0: AN006 AN106 0 0 0 1 1 1: AN007 AN107 0 1 0 0 0 0: AN016 AN116 : : 0 1 0 0 1 1: AN019 AN119 0 1 0 1 0 0: AN020 — 1 0 0 0 0 0: Temperature sensor 1 0 0 0 0 1: Internal reference voltage 1 1 1 1 1 1: Do no select. Other settings are prohibited.	R/W
b6	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b7	CMPLB	Compare Window B Comparison Condition Setting	This bit sets comparison conditions for channels for Window B. The comparison conditions are shown in Figure 47.6. • When window function is disabled (ADCMPCR.WCMPE = 0) 0: CMPLLB value > A/D-converted value 1: CMPLLB value < A/D-converted value. • When window function is enabled (ADCMPCR.WCMPE = 1) 0: A/D-converted value < CMPLLB value, or CMPULB value < A/D-converted value 1: CMPLLB value < A/D-converted value < CMPULB value.	R/W

CMPCHB[5:0] bits (Compare Window B Channel Select)

The CMPCHB[5:0] bits specify the channels to be compared with the compare Window B conditions from AN000 to AN007 and AN016 to AN020 (unit 0), AN100 to AN103, AN105 to AN107, and AN116 to AN119 (unit 1), the temperature sensor, and the internal reference voltage. The compare Window B function is enabled by specifying the hexadecimal number of the A/D conversion channel selected in the following bits:

Unit 0:

- ADANSA0.ANSA00 to ANSA07 bits
- ADANSA1.ANSA16 to ANSA20 bits
- ADANSB0.ANSB00 to ANSB07 bits
- ADANSB1.ANSB16 to ANSB20 bits.

[Clearing condition]

- 读1后写0。

47.2.30 AD比较功能窗口B通道选择寄存器(ADCMPBNSR)

Address(es): ADC120.ADCMPBNSR 4005 C0A6h, ADC121.ADCMPBNSR 4005 C2A6h

	b7	b6	b5	b4	b3	b2	b1	b0
	CMPLB	—	CMPCHB[5:0]					
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b5 to b0	CMPCHB[5:0]	比较窗口B通道 Select	这些位选择要与比较器进行比较的通道 窗口B条件。最大通道为单元0中的AN020和单元1中的AN119。 b5b0单元0单元1 0 0 0 0 0 0: AN000 AN100 0 0 0 0 0 1: AN001 AN101 0 0 0 0 1 0: AN002 AN102 0 0 0 0 1 1: AN003 AN103 0 0 0 1 0 0: AN004 — 0 0 0 1 0 1: AN005 AN105 0 0 0 1 1 0: AN006 AN106 0 0 0 1 1 1: AN007 AN107 0 1 0 0 0 0: AN016 AN116 : : 0 1 0 0 1 1: AN019 AN119 0 1 0 1 0 0: AN020 — 1 0 0 0 0 0：温度传感器 1 0 0 0 0 1：内部参考电压 11：不选择。禁止其他设置。	R/W
b6	—	Reserved	该位读取为0。写入值应为0。	R/W
b7	CMPLB	比较窗口B 比较条件设置	该位设置窗口B的通道比较条件。比较条件如图47.6所示。 禁用窗口功能时(ADCMPCR.WCMPE=0)0：CMPLLB值>AD转换值1：CMPLLB值<AD转换值。 启用窗口功能时(ADCMPCR.WCMPE=1)0：D转换值<CMPLLB值，或CMPULB值<AD转换值1：CMPLLB值<AD转换值<CMPULB值。	R/W

CMPCHB[5:0]位（比较窗口B通道选择）

CMPCHB[5:0]位指定要与比较窗口B条件比较的通道，从AN000到AN007和AN016到AN020（单元0）、AN100到AN103、AN105到AN107和AN116到AN119（单元1），温度传感器和内部参考电压。通过指定在以下位中选择的AD转换通道的十六进制数来启用比较窗口B功能：

Unit 0:

- ADANSA0.ANSA00到ANSA07位
- ADANSA1.ANSA16到ANSA20位
- ADANSB0.ANSB00至ANSB07位
- ADANSB1.ANSB16到ANSB20位。

Unit 1:

- ADANSA0.ANSA00 to ANSA03 bits
- ADANSA0.ANSA05 to ANSA07 bits
- ADANSA1.ANSA16 to ANSA19 bits
- ADANSB0.ANSB00 to ANSB03 bits
- ADANSB0.ANSB05 to ANSB07 bits
- ADANSB1.ANSB16 to ANSB19 bits.

Set the CMPCHB[5:0] bits while the ADCSR.ADST bit is 0.

CMPLB bit (Compare Window B Comparison Condition Setting)

The CMPLB bit specifies the comparison conditions for channels for Window B. When the comparison result of an analog input meets the set condition, the associated ADCMPBSR.CMPSTB flag sets to 1 and a compare interrupt request (ADC12i_CMPBI) (i = 0, 1)) is generated.

Compare conditions when the window function is disabled

CMPLB = 0		CMPLB = 1	
ADWINLLB value ≤ A/D converted value	Not met	ADWINLLB value < A/D converted value	Met
ADWINLLB value > A/D converted value	Met	ADWINLLB value ≥ A/D converted value	Not met

Compare conditions when the window function is enabled

CMPLB = 0

A/D converted value > ADWINULB value	Met
ADWINLLB value ≤ A/D converted value ≤ ADWINULB value	Not met
A/D converted value < ADWINLLB value	Met

CMPLB = 1

A/D converted value ≥ ADWINULB value	Not met
ADWINLLB value <A/D converted value < ADWINULB value	Met
A/D converted value ≤ ADWINLLB value	Not met

Figure 47.6 Explanation of compare conditions for compare function Window B

Unit 1:

- ADANSA0.ANSA00到ANSA03位
- ADANSA0.ANSA05到ANSA07位
- ADANSA1.ANSA16到ANSA19位
- ADANSB0.ANSB00至ANSB03位
- ADANSB0.ANSB05至ANSB07位
- ADANSB1.ANSB16至ANSB19位。

当ADCSR.ADST位为0时，设置CMPCHB[5:0]位。

CMPLB位（比较窗口B比较条件设置）

CMPLB位指定窗口B的通道比较条件。当模拟输入的比较结果满足设置条件时，相关的ADCMPBSR.CMPSTB标志设置为1，并且比较中断请求(ADC12i_CMPBI)(i=0 1))生成。

比较禁用窗口功能时的条件

CMPLB = 0		CMPLB = 1	
ADWINLLB值 AD转换值	没见过	ADWINLLB值<AD转换值	Met
ADWINLLB值>AD转换值	Met	ADWINLLB值 AD转换值	没见过

启用窗口功能时比较条件

CMPLB = 0

AD转换值>ADWINULB值	Met
ADWINLLB值 AD转换值 ADWINULB值	没见过
AD转换值<ADWINLLB值	Met

CMPLB = 1

AD转换值 ADWINULB值	没见过
ADWINLLB值<AD转换值<ADWINULB值	Met
AD转换值 ADWINLLB值	没见过

Figure 47.6 比较功能窗口B的比较条件说明

47.2.31 A/D Compare Function Window B Status Register (ADCMPBSR)

Address(es): ADC120.ADCMPBSR 4005 C0ACh, ADC121.ADCMPBSR 4005 C2ACh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	CMPSTB
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	CMPSTB	Compare Window B Flag	When Window B operation is enabled (ADCMPCR.CMPBE = 1), this bit indicates the comparison result of channels to which Window B comparison conditions are applied, selected from AN000 to AN007 and AN016 to AN020 (unit 0), AN100 to AN103, AN105 to AN107, and AN116 to AN119 (unit 1), temperature sensor output, and internal reference voltage. 0: Comparison conditions are not met 1: Comparison conditions are met.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

CMPSTB flag (Compare Window B Flag)

The CMPSTB flag indicates the comparison result of channels to which Window B comparison conditions are applied, selected from AN000 to AN007 and AN016 to AN020 (unit 0), AN100 to AN103, AN105 to AN107, and AN116 to AN119 (unit 1), the temperature sensor, and the internal reference voltage. When the comparison condition set in ADCMPBNSR.CMPLB is met at the end of A/D conversion, this flag sets to 1. When the ADCMPCR.CMPBIE bit is 1, a compare interrupt request (ADC12i_CMPBI (i = 0, 1)) is generated when this flag sets to 1.

Writing 1 to the CMPSTB flag is invalid.

[Setting condition]

- The condition set in ADCMPBNSR.CMPLB is met when ADCMPCR.CMPBE = 1.

[Clearing condition]

- Writing 0 after reading 1.

47.2.32 A/D Compare Function Window A/B Status Monitor Register (ADWINMON)

Address(es): ADC120.ADWINMON 4005 C08Ch, ADC121.ADWINMON 4005 C28Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	MONCMPB	MONCMPA	—	—	—	MONCOMB
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	MONCOMB	Combination Result Monitor	This bit indicates the combination result. This bit is valid when both Window A and Window B operations are enabled. 0: Window A/B composite conditions are not met 1: Window A/B composite conditions are met.	R
b3 to b1	—	Reserved	These bits are read as 0.	R
b4	MONCMPA	Comparison Result Monitor A	0: Window A comparison conditions are not met 1: Window A comparison conditions are met.	R
b5	MONCMPB	Comparison Result Monitor B	0: Window B comparison conditions are not met 1: Window B comparison conditions are met.	R
b7, b6	—	Reserved	These bits are read as 0.	R

47.2.31 AD比较功能窗口B状态寄存器(ADCMPBSR)

Address(es): ADC120.ADCMPBSR 4005 C0ACh, ADC121.ADCMPBSR 4005 C2ACh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	CMPSTB
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	CMPSTB	比较窗口B标志	当窗口B操作使能时（ADCMPCR.CMPBE=1），该位指示应用窗口B比较条件的通道的比较结果，从 AN000至AN007和AN016至AN020（单元0）、AN100至AN103、AN105至AN107和AN116至AN119（单元1）、温度传感器输出和内部参考电压。0：不满足比较条件1：满足比较条件。	R/W
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

CMPSTB标志（比较窗口B标志）

CMPSTB标志表示应用窗口B比较条件的通道的比较结果，从AN000到AN007和AN016到AN020（单元0）、AN100到AN103、AN105到AN107和AN116到AN119（单元1）中选择，温度传感器和内部参考电压。当比较条件设置在

ADCMPBNSR.CMPLB在AD转换结束时满足，该标志设置为1。当ADCMPCR.CMPBIE位为1时，当该标志设置为1时产生比较中断请求(ADC12i_CMPBI(i=0 1))。

将1写入CMPSTB标志无效。

[Setting condition]

- 当ADCMPCR.CMPBE=1时，满足ADCMPBNSR.CMPLB中设置的条件。

[Clearing condition]

- 读1后写0。

47.2.32 AD比较功能窗口AB状态监控寄存器(ADWINMON)

Address(es): ADC120.ADWINMON 4005 C08Ch, ADC121.ADWINMON 4005 C28Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	MONCMPB	MONCMPA	—	—	—	MONCOMB
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	MONCOMB	组合结果监视器	该位指示组合结果。当窗口A和窗口B操作都使能时，该位有效。0：不满足窗口AB合成条件1：满足窗口AB合成条件。	R
b3 to b1	—	Reserved	这些位读为0。	R
b4	MONCMPA	比较结果监视器A	0：不满足窗口A比较条件1：满足窗口A比较条件。	R
b5	MONCMPB	比较结果监视器B	0：不满足窗口B比较条件1：满足窗口B比较条件。	R
b7, b6	—	Reserved	这些位读为0。	R

MONCOMB bit (Combination Result Monitor)

The read-only MONCOMB bit indicates the combined result of comparison condition results A and B based on the combination condition set in the ADCMPCR.CMPAB[1:0] bits.

[Setting condition]

- The combined result meets the combination condition set in the ADCMPCR.CMPAB[1:0] bits when ADCMPCR.CMPAE = 1 and ADCMPCR.CMPBE = 1.

[Clearing conditions]

- The combined result does not meet the combination condition set in the ADCMPCR.CMPAB[1:0] bits
- ADCMPCR.CMPAE = 0 or ADCMPCR.CMPBE = 0.

MONCMPA bit (Comparison Result Monitor A)

The read-only MONCMPA bit is read as 1 when the A/D-converted value of the Window A target channel meets the condition set in ADCMPLR0/ADCMPLR1 and ADCMPLER. Otherwise, it is read as 0.

[Setting condition]

- The A/D-converted value meets the condition set in ADCMPLR0.CMPLCHAn when ADCMPCR.CMPAE = 1.

[Clearing conditions]

- The A/D-converted value does not meet the condition set in ADCMPLR0.CMPLCHAn when ADCMPCR.CMPAE = 1
- ADCMPCR.CMPAE = 0 (automatically cleared when the ADCMPCR.CMPAE value changes from 1 to 0).

MONCMPB bit (Comparison Result Monitor B)

The read-only MONCMPB bit is read as 1 when the A/D-converted value of the Window B target channel meets the condition set in the ADCMPBNSR.CMPLB bit. Otherwise, it is read as 0.

[Setting condition]

- The A/D-converted value meets the condition set in ADCMPBNSR.CMPLB when ADCMPCR.CMPBE = 1.

[Clearing conditions]

- The A/D-converted value does not meet the condition set in ADCMPBNSR.CMPLB when ADCMPCR.CMPBE = 1
- ADCMPCR.CMPBE = 0 (automatically cleared when the ADCMPCR.CMPBE value changes from 1 to 0).

47.2.33 A/D Programmable Gain Amplifier Control Register (ADPGACR)

Address(es): ADC120.ADPGACR 4005 C1A0h, ADC121.ADPGACR 4005 C3A0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	P002GEN	P002ENAMP	P002SEL1	P002SEL0	P001GEN	P001ENAMP	P001SEL1	P001SEL0	P000GEN	P000ENAMP	P000SEL1	P000SEL0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	P000SEL0	PGA P000 Amplifier Bypass Enable	0: Do not output the signal in a path bypassing the PGA amplifier 1: Output the signal in a path bypassing the PGA amplifier.	R/W
b1	P000SEL1	PGA P000 Amplifier Transit Enable	0: Do not output the signal in a path through the PGA amplifier 1: Output the signal in a path through the PGA amplifier.	R/W
b2	P000ENAMP	PGA P000 Amplifier Enable	0: Do not use the PGA amplifier 1: Use the PGA amplifier.	R/W
b3	P000GEN	PGA P000 Gain Setting Enable	0: Disable gain setting 1: Enable gain setting.	R/W

MONCOMB位（组合结果监视器）

只读MONCOMB位指示比较条件结果A和B基于ADCMPCR.CMPAB[1:0]位中设置的组合条件的组合结果。

[Setting condition]

- 当组合结果满足ADCMPCR.CMPAB[1:0]位中设置的组合条件时
  ADCMPCR.CMPAE = 1 and ADCMPCR.CMPBE = 1.

[Clearing conditions]

- 组合结果不满足ADCMPCR.CMPAB[1:0]位中设置的组合条件
- ADCMPCR.CMPAE = 0 or ADCMPCR.CMPBE = 0.

MONCMPA位（比较结果监视器A）

当窗口A目标通道的AD转换值满足ADCMPLR0ADCMPLR1和ADCMPLER中设置的条件时，只读MONCMPA位被读取为1。否则，读为0。

[Setting condition]

- 当ADCMPCR.CMPAE=1时，AD转换后的值满足ADCMPLR0.CMPLCHAn中设置的条件。

[Clearing conditions]

- 当ADCMPCR.CMPAE=1时，AD转换后的值不满足ADCMPLR0.CMPLCHAn中设置的条件
- ADCMPCR.CMPAE=0（ADCMPCR.CMPAE值从1变为0时自动清零）。

MONCMPB位（比较结果监视器B）

当窗口B目标通道的AD转换值满足ADCMPBNSR.CMPLB位中设置的条件时，只读MONCMPB位被读取为1。否则，读为0。

[Setting condition]

- 当ADCMPCR.CMPBE=1时，AD转换后的值满足ADCMPBNSR.CMPLB中设置的条件。

[Clearing conditions]

- 当ADCMPCR.CMPBE=
  1
- ADCMPCR.CMPBE=0（ADCMPCR.CMPBE值从1变为0时自动清零）。

47.2.33 AD可编程增益放大器控制寄存器(ADPGACR)

Address(es): ADC120.ADPGACR 4005 C1A0h, ADC121.ADPGACR 4005 C3A0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	P002GEN	P002ENAMP	P002SEL1	P002SEL0	P001GEN	P001ENAMP	P001SEL1	P001SEL0	P000GEN	P000ENAMP	P000SEL1	P000SEL0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	P000SEL0	PGAP000放大器旁路Enable	0：不输出绕过PGA放大器的路径1：输出绕过PGA放大器的路径。	R/W
b1	P000SEL1	PGAP000放大器传输Enable	0：不通过PGA放大器的路径输出信号1：通过PGA放大器的路径输出信号。	R/W
b2	P000ENAMP	PGAP000放大器启用	0：不使用PGA放大器1：使用PGA放大器。	R/W
b3	P000GEN	PGAP000增益设置Enable	0：禁用增益设置1：启用增益设置。	R/W

Bit	Symbol	Bit name	Description	R/W
b4	P001SEL0	PGA P001 Amplifier Bypass Enable	0: Do not output the signal in a path bypassing the PGA amplifier 1: Output the signal in a path bypassing the PGA amplifier.	R/W
b5	P001SEL1	PGA P001 Amplifier Transit Enable	0: Do not output the signal in a path through the PGA amplifier 1: Output the signal in a path through the PGA amplifier.	R/W
b6	P001ENAMP	PGA P001 Amplifier Enable	0: Do not use the PGA amplifier 1: Use the PGA amplifier.	R/W
b7	P001GEN	PGA P001 Gain Setting Enable	0: Disable gain setting 1: Enable gain setting.	R/W
b8	P002SEL0	PGA P002 Amplifier Bypass Enable	0: Do not output the signal in a path bypassing the PGA amplifier 1: Output the signal in a path bypassing the PGA amplifier.	R/W
b9	P002SEL1	PGA P002 Amplifier Transit Enable	0: Do not output the signal in a path through the PGA amplifier 1: Output the signal in a path through the PGA amplifier.	R/W
b10	P002ENAMP	PGA P002 Amplifier Enable	0: Do not use the PGA amplifier 1: Use the PGA amplifier.	R/W
b11	P002GEN	PGA P002 Gain Setting Enable	0: Disable gain setting 1: Enable gain setting.	R/W
b12	—	Reserved	This bit is read as 1. The write value should be 1.	R/W
b14, b13	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b15	—	Reserved	This bit is read as 1. The write value should be 1.	R/W

Note: See section 47.3.12, Programmable Gain Amplifiers, for details on setting these bits.

PnSEL0 bit (PGA Pn Amplifier Bypass Enable) (n = 000 to 002)

The PnSEL0 bit selects whether to output the signal in a path that bypasses the amplifier in the PGA for each programmable gain amplifier Pn.

PnSEL1 bit (PGA Pn Amplifier Transit Enable) (n = 000 to 002)

The PnSEL1 bit selects whether to output the signal in a path through the amplifier in the PGA for each programmable gain amplifier Pn.

PnENAMP bit (PGA Pn Amplifier Enable) (n = 000 to 002)

The PnENAMP bit selects whether to use the amplifier in the PGA for each programmable gain amplifier Pn.

PnGEN bit (PGA Pn Input Resistance Side Gain Selection Signal Enable) (n = 000 to 002)

The PnGEN bit enables or disables the gain setting for each programmable gain amplifier Pn.

Bit	Symbol	位名称	Description	R/W
b4	P001SEL0	PGAP001放大器旁路Enable	0：不输出绕过PGA放大器的路径1：输出绕过PGA放大器的路径。	R/W
b5	P001SEL1	PGAP001放大器传输Enable	0：不通过PGA放大器的路径输出信号1：通过PGA放大器的路径输出信号。	R/W
b6	P001ENAMP	PGAP001放大器启用	0：不使用PGA放大器1：使用PGA放大器。	R/W
b7	P001GEN	PGAP001增益设置Enable	0：禁用增益设置1：启用增益设置。	R/W
b8	P002SEL0	PGAP002放大器旁路Enable	0：不输出绕过PGA放大器的路径1：输出绕过PGA放大器的路径。	R/W
b9	P002SEL1	PGAP002放大器传输Enable	0：不通过PGA放大器的路径输出信号1：通过PGA放大器的路径输出信号。	R/W
b10	P002ENAMP	PGAP002放大器启用	0：不使用PGA放大器1：使用PGA放大器。	R/W
b11	P002GEN	PGAP002增益设置Enable	0：禁用增益设置1：启用增益设置。	R/W
b12	—	Reserved	该位读取为1。写入值应为1。	R/W
b14, b13	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b15	—	Reserved	该位读取为1。写入值应为1。	R/W

Note: 有关设置这些位的详细信息，请参见第47.3.12节，可编程增益放大器。

PnSEL0位（PGAPn放大器旁路使能）（n=000至002）

PnSEL0位为每个可编程增益放大器Pn选择是否在绕过PGA中放大器的路径输出信号。

PnSEL1位（PGAPn放大器传输使能）（n=000至002）

PnSEL1位为每个可编程增益放大器Pn选择是否在通过PGA中的放大器的路径中输出信号。

PnENAMP位（PGAPn放大器启用）（n=000至002）

PnENAMP位为每个可编程增益放大器Pn选择是否使用PGA中的放大器。

PnGEN位（PGAPn输入电阻侧增益选择信号使能）（n=000至002）

PnGEN位启用或禁用每个可编程增益放大器Pn的增益设置。

47.2.34 A/D Programmable Gain Amplifier Gain Setting Register 0 (ADPGAGS0)

Address(es): ADC120.ADPGAGS0 4005 C1A2h, ADC121.ADPGAGS0 4005 C3A2h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	P002GAIN[3:0]				P001GAIN[3:0]				P000GAIN[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	P000GAIN[3:0]	PGA P000 Gain Setting	• When differential input is disabled (ADPGADCR0.PnDEN = 0) 0 0 0 0: × 2.000 0 0 0 1: × 2.500 0 0 1 0: × 2.667 0 0 1 1: × 2.857 0 1 0 0: × 3.077 0 1 0 1: × 3.333 0 1 1 0: × 3.636 0 1 1 1: × 4.000 1 0 0 0: × 4.444 1 0 0 1: × 5.000 1 0 1 0: × 5.714 1 0 1 1: × 6.667 1 1 0 0: × 8.000 1 1 0 1: × 10.000 1 1 1 0: × 13.333. • When differential input is enabled (ADPGADCR0.PnDEN = 1)*1 0 0 0 1: × 1.500 0 1 0 1: × 2.333 1 0 0 1: × 4.000 1 0 1 1: × 5.667. Other settings are prohibited.	R/W
b7 to b4	P001GAIN[3:0]	PGA P001 Gain Setting		R/W
b11 to b8	P002GAIN[3:0]	PGA P002 Gain Setting		R/W
b15 to b12	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. For details on setting these bits, see section 47.3.12, Programmable Gain Amplifiers.

PnGAIN[3:0] bits (PGA Pn Gain Setting) (n = 000 to 002)

The PnGAIN[3:0] bits specify the gain of each PGA amplifier Pn. For differential inputs (ADPGADCR0.PnDEN = 1 and ADPGACR.PnGEN = 1), these bits set the gain in combination with ADPGADCR0.PnDG[1:0].

47.2.34 AD可编程增益放大器增益设置寄存器0(ADPGAGS0)

Address(es): ADC120.ADPGAGS0 4005 C1A2h, ADC121.ADPGAGS0 4005 C3A2h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	P002GAIN[3:0]				P001GAIN[3:0]				P000GAIN[3:0]			
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b3 to b0	P000GAIN[3:0]	PGAP000增益设置	当差分输入禁用时(ADPADCR0.PnDEN=0) 0 0 0 0: × 2.000 0 0 0 1: × 2.500 0 0 1 0: × 2.667 0 0 1 1: × 2.857 0 1 0 0: × 3.077 0 1 0 1: × 3.333 0 1 1 0: × 3.636 0 1 1 1: × 4.000 1 0 0 0: × 4.444 1 0 0 1: × 5.000 1 0 1 0: × 5.714 1 0 1 1: × 6.667 1 1 0 0: × 8.000 1 1 0 1: × 10.000 1 1 1 0: × 13.333. 当启用差分输入时(ADPADCR0.PnDEN=1)*1 0 0 0 1: × 1.500 0 1 0 1: × 2.333 1 0 0 1: × 4.000 11： 5.667。禁止其他设置。	R/W
b7 to b4	P001GAIN[3:0]	PGAP001增益设置		R/W
b11 to b8	P002GAIN[3:0]	PGAP002增益设置		R/W
b15 to b12	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 有关设置这些位的详细信息，请参见第47.3.12节，可编程增益放大器。

PnGAIN[3:0]位（PGAPn增益设置）（n=000至002）

PnGAIN[3:0]位指定每个PGA放大器Pn的增益。对于差分输入（ADPGADCR0.PnDEN=1和ADPGACR.PnGEN=1），这些位与ADPGADCR0.PnDG[1:0]一起设置增益。

47.2.35 A/D Programmable Gain Amplifier Differential Input Control Register (ADPGADCR0)

Address(es): ADC120.ADPGADCR0 4005 C1B0h, ADC121.ADPGADCR0 4005 C3B0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	P002DEN	—	P002DG[1:0]		P001DEN	—	P001DG[1:0]		P000DEN	—	P000DG[1:0]	
Value after reset:	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	P000DG[1:0]	P000 Differential Input Gain Setting	When these bits are used, set {P000DEN, P000GEN} to 11b. b1 b0 0 0: × 1.5 0 1: × 2.333 1 0: × 4.0 1 1: × 5.667.	R/W
b2	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b3	P000DEN	P000 Differential Input Enable	0: Disable differential input 1: Enable differential input.	R/W
b5, b4	P001DG[1:0]	P001 Differential Input Gain Setting	When these bits are used, set {P001DEN, P001GEN} to 11b. b5 b4 0 0: × 1.5 0 1: × 2.333 1 0: × 4.0 1 1: × 5.667.	R/W
b6	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b7	P001DEN	P001 Differential Input Enable	0: Disable differential input 1: Enable differential input.	R/W
b9, b8	P002DG[1:0]	P002 Differential Input Gain Setting	When these bits are used, set {P002DEN, P002GEN} to 11b. b9 b8 0 0: × 1.5 0 1: × 2.333 1 0: × 4.0 1 1: × 5.667	R/W
b10	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b11	P002DEN	P002 Differential Input Enable	0: Disable differential input 1: Enable differential input.	R/W
b15 to b12	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: For details on setting these bits, see section 47.3.12, Programmable Gain Amplifiers.

PnDG[1:0] bits (Pn Differential Input Gain Setting) (n = 000 to 002)

The PnDG[1:0] bits specify the gain of each PGA amplifier Pn when differential inputs are used. These bits are only valid when the PnDEN bit = 1 and the PnGEN bit = 1.

To use the PGA for differential inputs, set the ADPGADCR0.PnDG[1:0] bits in conjunction with the ADPGAGS0.PnGAIN[3:0] bits.

Example: To set the gain to × 1.5 using P000 for differential input, set:
ADPGAGS0.P000GAIN[3:0] = 0001b
ADPGADCR0.P000DG[1:0] = 00b

PnDEN bit (Pn Differential Input Enable) (n = 000 to 002)

The PnDEN bit enables or disables differential inputs for each PGA amplifier Pn.

47.2.35 AD可编程增益放大器差分输入控制寄存器(ADPGADCR0)

Address(es): ADC120.ADPGADCR0 4005 C1B0h, ADC121.ADPGADCR0 4005 C3B0h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	P002DEN	—	P002DG[1:0]		P001DEN	—	P001DG[1:0]		P000DEN	—	P000DG[1:0]	
重置后的值:	1	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0

Bit	Symbol	位名称	Description	R/W
b1, b0	P000DG[1:0]	P000差分输入增益Setting	使用这些位时，将{P000DEN P000GEN 设置为11b。b1b0 0 0: 1.5 0 1: × 2.333 1 0: × 4.0 1 1: × 5.667.	R/W
b2	—	Reserved	该位读取为0。写入值应为0。	R/W
b3	P000DEN	P000差分输入使能	0：禁用差分输入1：启用差分输入。	R/W
b5, b4	P001DG[1:0]	P001差分输入增益Setting	使用这些位时，将{P001DEN P001GEN 设置为11b。b5b4 0 0: 1.5 0 1: × 2.333 1 0: × 4.0 1 1: × 5.667.	R/W
b6	—	Reserved	该位读取为0。写入值应为0。	R/W
b7	P001DEN	P001差分输入使能	0：禁用差分输入1：启用差分输入。	R/W
b9, b8	P002DG[1:0]	P002差分输入增益Setting	使用这些位时，将{P002DEN P002GEN 设置为11b。b9b8 0 0: 1.5 0 1: × 2.333 1 0: × 4.0 1 1: × 5.667	R/W
b10	—	Reserved	该位读取为0。写入值应为0。	R/W
b11	P002DEN	P002差分输入使能	0：禁用差分输入1：启用差分输入。	R/W
b15 to b12	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note: 有关设置这些位的详细信息，请参见第47.3.12节，可编程增益放大器。

PnDG[1:0]位（Pn差分输入增益设置）（n=000至002）

当使用差分输入时，PnDG[1:0]位指定每个PGA放大器Pn的增益。这些位仅在PnDEN位=1且PnGEN位=1时有效。

要将PGA用于差分输入，请将ADPGADCR0.PnDG[1:0]位与ADPGAGS0.PnGAIN[3:0] bits.

示例：要使用P000差分输入将增益设置为 1.5，请设置：
ADPGAGS0.P000GAIN[3:0] = 0001b
ADPGADCR0.P000DG[1:0] = 00b

PnDEN位（Pn差分输入使能）（n=000至002）

PnDEN位启用或禁用每个PGA放大器Pn的差分输入。

47.3 Operation

47.3.1 Scanning Operation

In scanning, A/D conversion is performed sequentially on the analog inputs of the specified channels.

Scan conversion is performed in three operating modes: single scan mode, continuous scan mode, and group scan mode. In single scan mode, one or more specified channels are scanned once. In continuous scan mode, one or more specified channels are scanned repeatedly until the ADCSR.ADST bit is cleared to 0 from 1 by software. In group scan mode, the selected channels in Group A and the selected channels in Group B are scanned once after scan starts in response to the respective synchronous trigger (ELC).

In single scan mode and continuous scan mode, A/D conversion is performed for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n. In group scan mode, A/D conversion is performed for the ANn channels in Group A selected in the ADANSA0 and ADANSA1 registers first, and then for the ANn channels in Group B selected in the ADANSB0 and ADANSB1 registers, starting from the channel with the smallest number n.

When self-diagnosis is selected, it is executed once at the beginning of each scan, and one of the three voltages generated internally in the ADC12 is converted.

The temperature sensor output and internal reference voltage can be selected at the same time as the analog input of the channels, and A/D conversion is performed on the analog input of channels, temperature sensor output, and internal reference voltage, in that order.

Double-trigger mode can be used with single scan mode or group scan mode. With double-trigger mode enabled (ADCSR.DBLE = 1), A/D conversion data of a channel selected in the ADCSR.DBLANS[4:0] bits is duplicated only if the conversion is started by the synchronous trigger (ELC) selected in the TRSA[5:0] bits in ADSTRGR. Only Group A in group scan mode can use the double-trigger mode.

The extended operation of double-trigger mode means the A/D conversion operation is generated from the synchronous trigger combination. This trigger combination is selected in ADSTRGR.TRSA[5:0] in double-trigger mode. ELC_AD00 and ELC_AD01 are associated with unit 0. ELC_AD10 and ELC_AD11 are associated with unit 1.

In the extended operation of double-trigger mode, in addition to normal double-trigger operation, A/D conversion data from the ELC_AD00 (unit 0) and ELC_AD10 (unit 1) triggers is stored in A/D Data Duplexing Register A (ADDBLDRA), and A/D conversion data from the ELC_AD01 (unit 0) and ELC_AD11 (unit 1) triggers is stored in A/D Data Duplexing Register B (ADDBLDRB). In the extended operation of double-trigger mode, when a combination of triggers occurs at the same time, the data duplexing register settings for the specified triggers do not work, and A/D conversion data is stored in A/D Data Duplexing Register B (ADDBLDRB).

When one synchronous trigger is input during the A/D conversion started by another synchronous trigger, the subsequent trigger is input when the other A/D conversion is canceled.

When any of the AN000 to AN002 (unit 0), and AN100 to AN102 (unit 1) channels are set as a channel-dedicated sample-and-hold circuit in the SHANS[2:0] bits in ADSHCR, the target analog input specified is sampled and held before the first A/D conversion of each scan.

47.3.2 Single Scan Mode

47.3.2.1 Basic operation without channel-dedicated sample-and-hold circuits

In basic operation of single scan mode, A/D conversion is performed once on the analog input of the specified channels.

The operation is as follows:

1. When the ADCSR.ADST bit is set to 1 (A/D conversion start) by a software trigger, synchronous trigger input (ELC), or asynchronous trigger input, A/D conversion is performed for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
2. Each time A/D conversion of a single channel completes, the A/D conversion result is stored in the associated A/D data register (ADDRy).
3. When A/D conversion of all the selected channels completes, an ADC12i_ADI (i = 0, 1) interrupt request is generated (no register setting).

47.3 Operation

47.3.1 扫描操作

扫描时，对指定通道的模拟输入依次进行AD转换。

扫描转换以三种操作模式执行：单次扫描模式、连续扫描模式和组扫描模式。在单次扫描模式下，一个或多个指定通道被扫描一次。在连续扫描模式下，重复扫描一个或多个指定通道，直到ADCSR.ADST位由软件从1清零。在组扫描模式下，A组中的选定通道和B组中的选定通道在扫描开始后扫描一次，以响应各自的同步触发(ELC)。

在单次扫描模式和连续扫描模式下，对选择的ANn通道进行AD转换
ADANSA0和ADANSA1寄存器，从编号n最小的通道开始。在组扫描模式下，首先对ADANSA0和ADANSA1寄存器中选择的A组ANn通道进行A/D转换，然后对ADANSB0和ADANSB1寄存器中选择的B组ANn通道进行A/D转换，从编号最小的通道开始n.

选择自诊断时，在每次扫描开始时执行一次，并转换ADC12内部产生的三个电压之一。

温度传感器输出和内部参考电压可以与通道的模拟输入同时选择，通道的模拟输入、温度传感器输出和内部参考电压依次进行AD转换。

双触发模式可与单扫描模式或组扫描模式一起使用。启用双触发模式(ADCSR.DBLE=1)时，仅当转换由在ADSTRGR中的TRSA[5:0]位。只有组扫描模式下的A组可以使用双触发模式。

双触发模式的扩展操作是指A/D转换操作是由同步触发组合产生的。在双触发模式下，此触发组合在ADSTRGR.TRSA[5:0]中选择。ELC_AD00和ELC_AD01与单元0关联。ELC_AD10和ELC_AD11与单元1关联。

在双触发模式的扩展操作中，除了正常的双触发操作外，来自ELC_AD00（单元0）和ELC_AD10（单元1）触发的AD转换数据存储在AD数据双工寄存器A（ADDBLDRA）中，而AD来自ELC_AD01（单元0）和ELC_AD11（单元1）触发器的转换数据存储在AD数据双工寄存器B(ADDBLDRB)中。在双触发模式的扩展操作中，当同时发生多个触发时，指定触发的数据双工寄存器设置不起作用，AD转换数据存储在AD数据双工寄存器B（ADDBLDRB）中。

在由另一个同步触发启动的AD转换期间输入一个同步触发时，在取消另一个AD转换时输入后续触发。

当任何AN000至AN002（单元0）和AN100至AN102（单元1）通道在ADSHCR的SHANS[2:0]位中设置为通道专用采样保持电路时，目标模拟输入指定在每次扫描的第一个AD转换之前被采样和保持。

47.3.2 单次扫描模式

47.3.2.1 无通道专用采样保持电路的基本操作

在单次扫描模式的基本操作中，对指定通道的模拟输入进行一次AD转换。

操作如下：

1. 当通过软件触发、同步触发输入(ELC)或异步触发输入将ADCSR.ADST位设置为1（AD转换开始）时，将从ADANSA0和ADANSA1寄存器中选择的ANn通道执行AD转换，从具有最小编号n的通道。
2. 每次单个通道的AD转换完成时，AD转换结果都会存储在相关的AD数据寄存器(ADDRy)中。
3. 当所有选定通道的AD转换完成时，会产生一个ADC12i_ADI(i=0 1)中断请求（无寄存器设置）。

4. The ADST bit remains 1 (A/D conversion start) during A/D conversion, and is automatically cleared to 0 when A/D conversion of all the selected channels completes. Then the ADC12 enters a wait state.

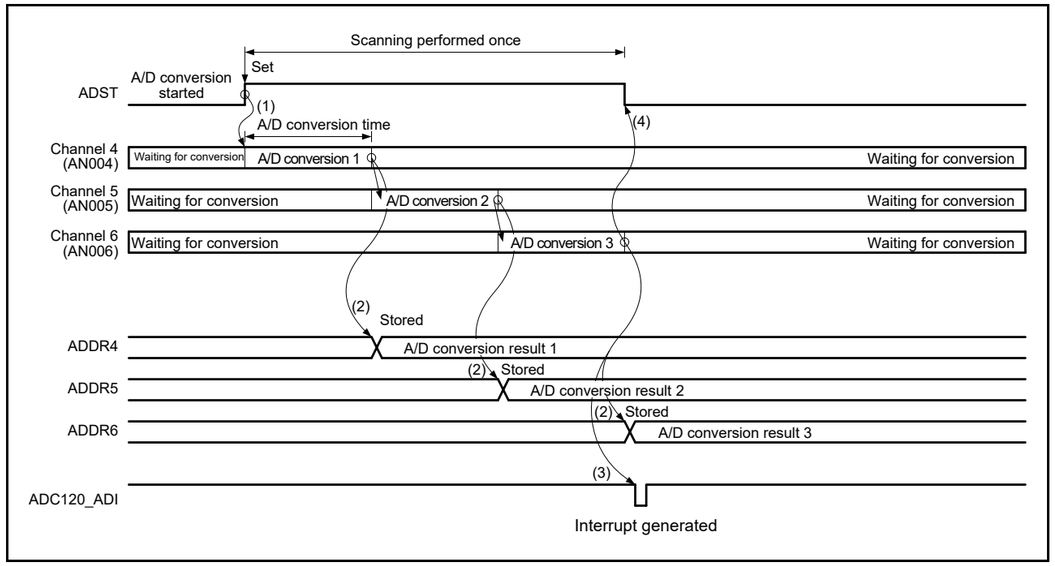


Figure 47.7 Example basic operation in single scan mode when AN004 to AN006 are selected

47.3.2.2 Basic operation with channel-dedicated sample-and-hold circuits and continuous sampling disabled

When the channel-dedicated sample-and-hold circuit is used, sample-and-hold operation is first performed, and then A/D conversion is performed once on the analog input of all the specified channels. The channels whose dedicated sample-and-hold circuit is to be used can be selected in the SHANS[2:0] bits in ADSHCR.

The operation is as follows:

1. Analog input sampling of all channels whose dedicated sample-and-hold circuit is to be used starts when the ADCSR.ADST bit is set to 1 (A/D conversion start) by a software trigger, synchronous trigger input (ELC), or asynchronous trigger input.
2. After sample-and-hold operation, A/D conversion is performed for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
3. Each time A/D conversion of a single channel completes, the A/D conversion result is stored in the associated A/D data register (ADDRy).
4. When A/D conversion of all the selected channels completes, an ADC12i_ADI (i = 0, 1) interrupt request is generated (no register setting).
5. The ADST bit remains 1 (A/D conversion start) during A/D conversion, and is automatically cleared to 0 when A/D conversion of all the selected channels completes. Then the ADC12 enters a wait state.

4. ADST位在AD转换期间保持1（AD转换开始），并在所有选定通道的AD转换完成时自动清零。然后ADC12进入等待状态。

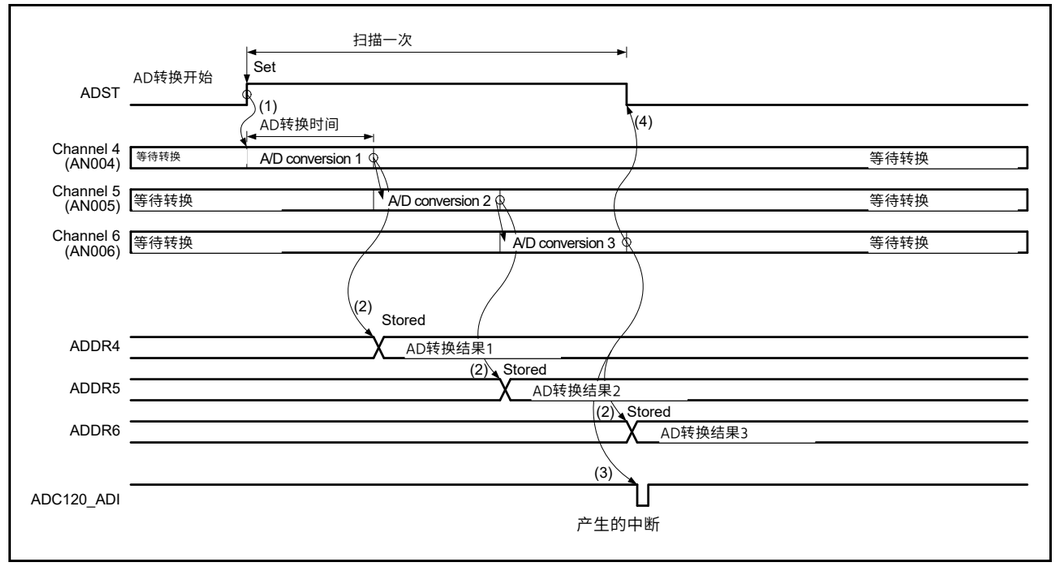


Figure 47.7 选择AN004至AN006时单次扫描模式的基本操作示例

47.3.2.2 通道专用采样保持电路和禁用连续采样的基本操作

当使用通道专用的采样保持电路时，首先进行采样保持操作，然后对所有指定通道的模拟输入进行一次A/D转换。可以在ADSHCR的SHANS[2:0]位中选择要使用专用采样保持电路的通道。

操作如下：

1. 将使用专用采样保持电路的所有通道的模拟输入采样在ADCSR.ADST位通过软件触发、同步触发输入(ELC)或异步触发输入设置为1（AD转换开始）。
2. 采样保持操作后，对ADANSA0和ADANSA1寄存器中选择的ANn通道执行AD转换，从编号n最小的通道开始。
3. 每次单个通道的AD转换完成时，AD转换结果都会存储在相关的AD数据寄存器(ADDRy)中。
4. 当所有选定通道的AD转换完成时，会产生一个ADC12i_ADI(i=0 1)中断请求（无寄存器设置）。
5. ADST位在AD转换期间保持1（AD转换开始），并在所有选定通道的AD转换完成时自动清零。然后ADC12进入等待状态。

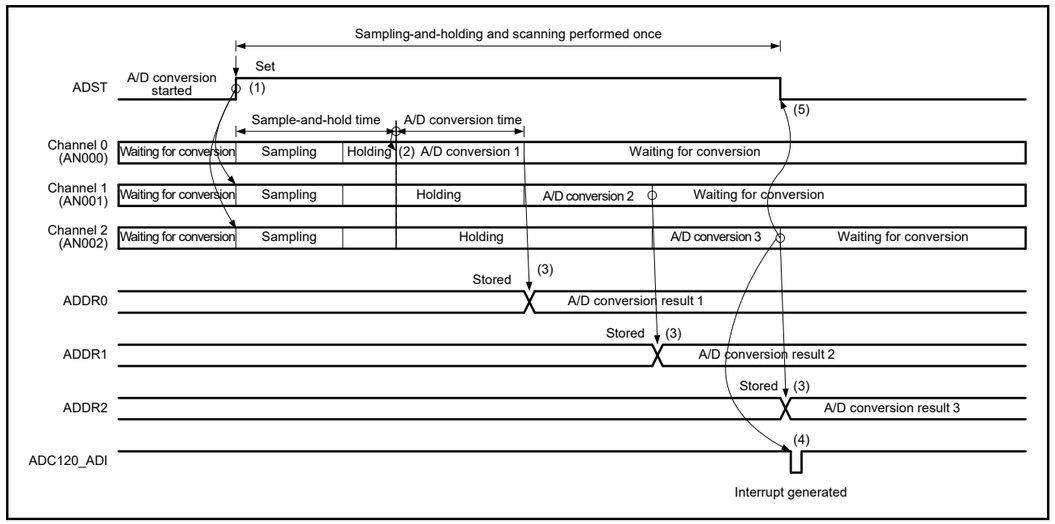


Figure 47.8 Example operation in single scan mode when the channel-dedicated sample-and-hold circuits are used and AN000 to AN002 are selected

47.3.2.3 Basic operation with channel-dedicated sample-and-hold circuits and continuous sampling enabled

When a channel-dedicated sample-and-hold circuit is used while continuous sampling is enabled, sample-and-hold operations are performed first, and this is followed by A/D conversion once of the analog inputs on all selected channels. The ADSHCR.SHANS[2:0] bits specify the channels for which the channel-dedicated sample-and-hold circuits are to be used.

The operation is as follows:

1. When the ADSHMSR.SHMD bit is set to 1, the sample-and-hold circuits selected in the ADSHCR.SHANS[2:0] bits start continuous sampling.
2. Analog input holding starts for all channels for which the channel-dedicated sample-and-hold circuits are to be used when the ADCSR.ADST bit is set to 1 (A/D conversion start) by a software trigger, input of a synchronous trigger signal (ELC), or input of an asynchronous trigger.
3. After the stabilization time of the sample-and-hold circuits elapses, A/D conversion is performed for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
4. Each time A/D conversion of a single channel completes, the A/D conversion result is stored in the associated A/D data register (ADDRy), and the sample-and-hold circuit restarts continuous sampling.
5. When A/D conversion of all the selected channels completes, an ADC12i_ADI (i = 0, 1) interrupt request is generated (no register setting).
6. The ADCSR.ADST bit remains 1 (A/D conversion start) during A/D conversion, and is automatically cleared to 0 when A/D conversion of all the selected channels completes. Then the ADC12 enters a wait state. If this is followed by single scanning, set the continuous sampling time for the sample-and-hold circuits to at least 400 ns (when the permissible signal source impedance is 1 kΩ).
7. When the ADSHMSR.SHMD bit is set to 0, the sample-and-hold circuits stop.

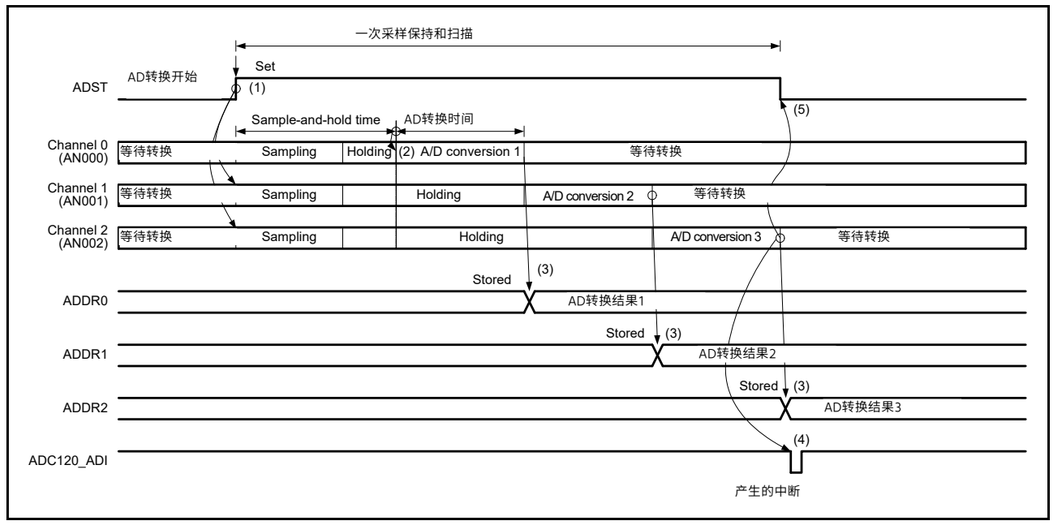


Figure 47.8 使用通道专用采样保持电路并选择AN000至AN002时单扫描模式下的示例操作

47.3.2.3 具有通道专用采样保持电路和连续采样的基本操作

如果在启用连续采样的情况下使用通道专用的采样保持电路，则首先执行采样保持操作，然后对所有选定通道的模拟输入进行一次AD转换。ADSHCR.SHANS[2:0]位指定要使用通道专用采样保持电路的通道。

操作如下：

1. 当ADSHMSR.SHMD位设置为1时，在ADSHCR.SHANS[2:0]位中选择的采样保持电路开始连续采样。
2. 当通过软件触发将ADCSR.ADST位设置为1（AD转换开始）时，将使用通道专用采样保持电路的所有通道开始模拟输入保持，输入同步触发信号(ELC），或异步触发器的输入。
3. 经过采样保持电路的稳定时间后，从编号n最小的通道开始，对ADANSA0和ADANSA1寄存器中选择的ANn通道执行AD转换。
4. 每次完成单通道的AD转换，AD转换结果存储在相关的AD数据寄存器（ADDRy）中，采样保持电路重新开始连续采样。
5. 当所有选定通道的AD转换完成时，会产生一个ADC12i_ADI(i=0 1)中断请求（无寄存器设置）。
6. ADCSR.ADST位在AD转换期间保持1（AD转换开始），并在所有选定通道的AD转换完成时自动清零。然后ADC12进入等待状态。如果随后进行单次扫描，请将采样保持电路的连续采样时间设置为至少400ns（当允许的信号源阻抗为1kΩ时）。
7. 当ADSHMSR.SHMD位设置为0时，采样保持电路停止。

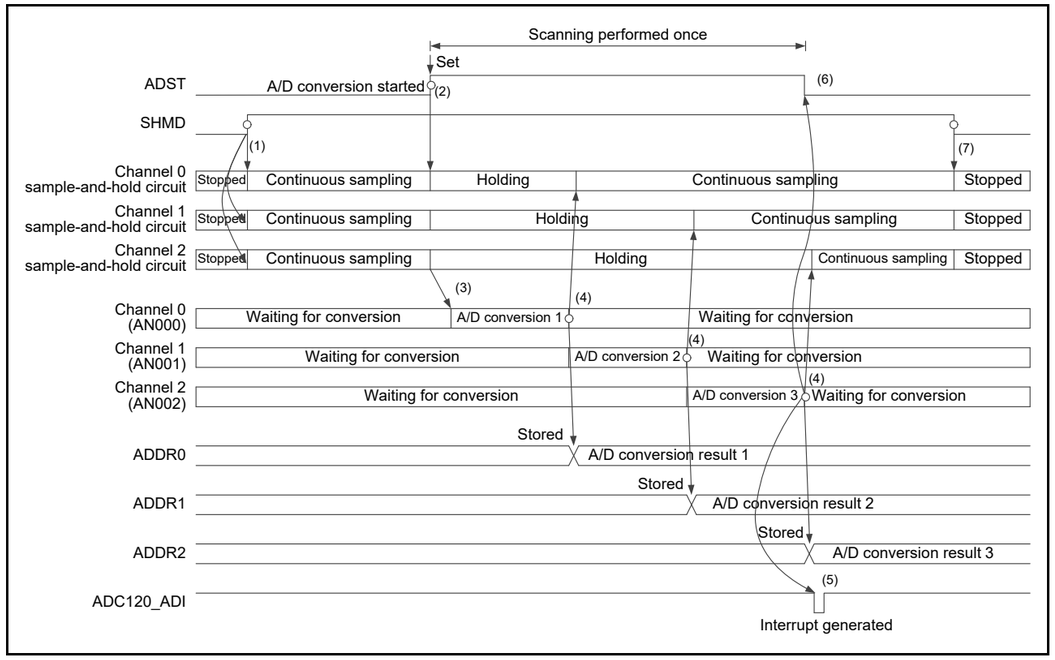


Figure 47.9 Example operation in single scan mode when channel-dedicated sample-and-hold circuits are used, AN000 to AN002 are selected, and continuous sampling is enabled

47.3.2.4 Channel selection and self-diagnosis without channel-dedicated sample-and-hold circuits

When channels and self-diagnosis are selected, A/D conversion is first performed for the reference voltage VREFH0 (unit 0) or VREFH (unit 1) (× 0, × 1/2, or × 1) supplied to the ADC12, and then A/D conversion is performed once on the analog input of the specified channels.

The operation is as follows:

1. A/D conversion for self-diagnosis is first started when the ADCSR.ADST bit is set to 1 (A/D conversion start) by a software trigger, synchronous trigger input (ELC), or asynchronous trigger input.
2. When A/D conversion for self-diagnosis completes, the A/D conversion result is stored in the A/D Self-Diagnosis Data Register (ADRD). A/D conversion is then performed for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
3. Each time A/D conversion of a single channel completes, the A/D conversion result is stored in the associated A/D data register (ADDRy).
4. When A/D conversion of all the selected channels completes, an ADC12i_ADI (i = 0, 1) interrupt request is generated (no register setting).
5. The ADST bit remains 1 (A/D conversion start) during A/D conversion, and is automatically cleared to 0 when A/D conversion of all the selected channels completes. Then the ADC12 enters a wait state.

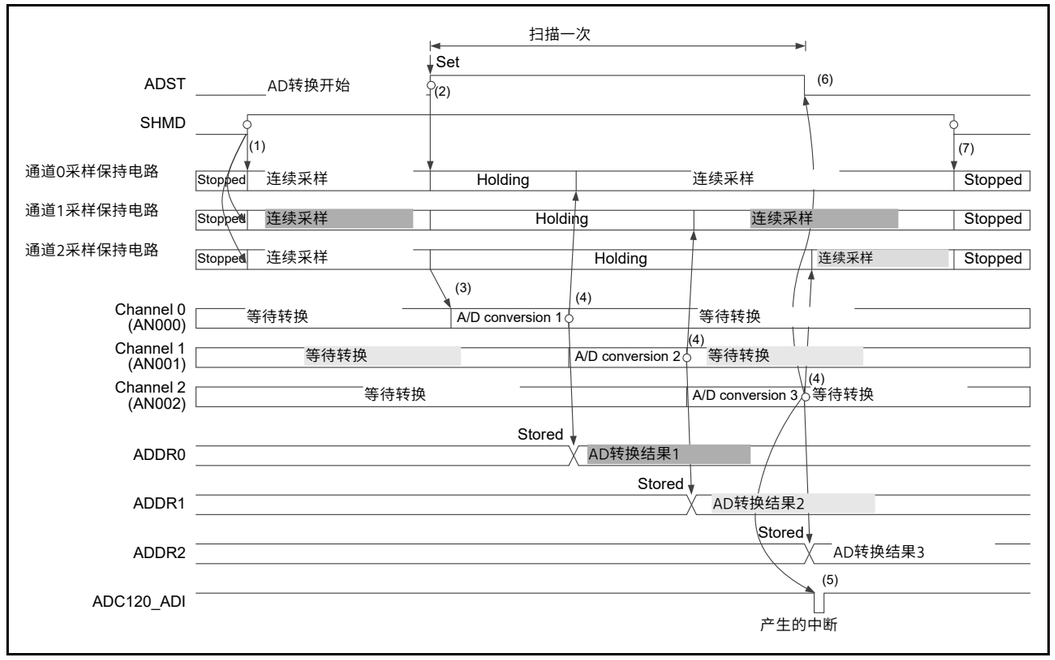


Figure 47.9 使用通道专用采样保持电路、选择AN000至AN002并启用连续采样时的单次扫描模式操作示例

47.3.2.4 通道选择和自诊断，无需通道专用的采样和保持电路

Whenchannelsandself-diagnosisareselected ADconversionisfirstperformedforthereferencevoltageVREFH0(unit0)orVREFH(unit1)(×0 ×12 or×1)suppliedtotheADC12 andthenADconversion在指定通道的模拟输入上执行一次。

操作如下：

1. 通过软件触发、同步触发输入(ELC)或异步触发输入将ADCSR.ADST位设置为1（AD转换开始）时，首先启动用于自诊断的D转换。
2. 自诊断用AD转换完成后，AD转换结果存储在AD自诊断中数据寄存器(ADRD)。然后对ADANSA0中选择的ANn通道执行D转换，并ADANSA1寄存器，从编号n最小的通道开始。
3. 每次单个通道的AD转换完成时，AD转换结果都会存储在相关的AD数据寄存器(ADDRy)中。
4. 当所有选定通道的AD转换完成时，会产生一个ADC12i_ADI(i=0 1)中断请求（无寄存器设置）。
5. ADST位在AD转换期间保持1（AD转换开始），并在所有选定通道的AD转换完成时自动清零。然后ADC12进入等待状态。

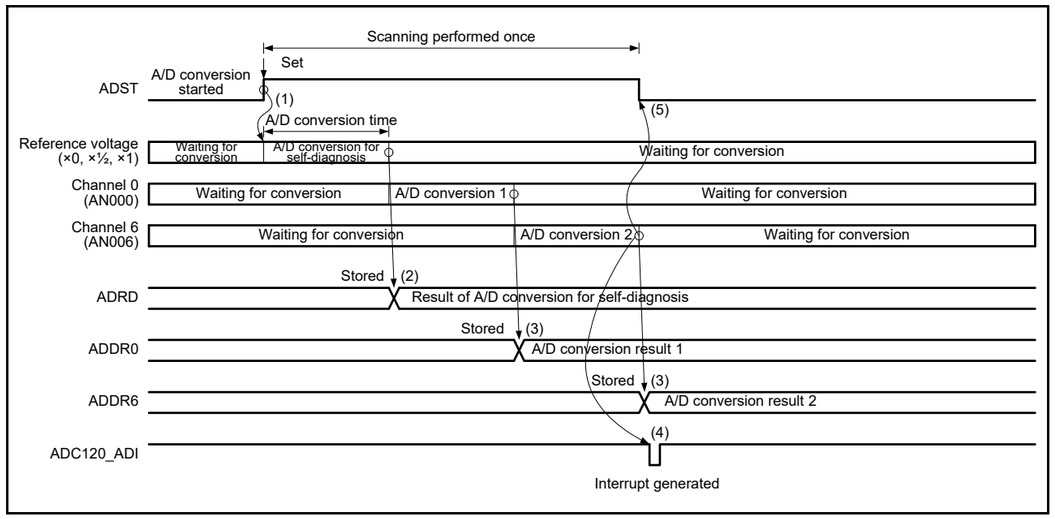


Figure 47.10 Example basic operation in single scan mode when AN000 and AN006 are selected with self-diagnosis

47.3.2.5 Channel selection and self-diagnosis with channel-dedicated sample-and-hold circuits and continuous sampling disabled

When channels and self-diagnosis are selected and a channel-dedicated sample-and-hold circuit is used while continuous sampling is disabled, the sample-and-hold operation is performed first, and then A/D conversion is performed once for the reference voltage VREFH0 (unit 0) or VREFH (unit 1) (×0, ×1/2, or ×1) supplied to the ADC12. After that, A/D conversion is performed only once on the analog input of the selected channels.

The operation is as follows:

1. Analog input sampling starts for all channels whose dedicated sample-and-hold circuit is to be used when the ADCSR.ADST bit is set to 1 (A/D conversion start) by a software trigger, synchronous trigger input (ELC), or asynchronous trigger input.
2. After sample-and-hold operation, A/D conversion for self-diagnosis starts.
3. When A/D conversion for self-diagnosis completes, the A/D conversion result is stored in the A/D Self-Diagnosis Data Register (ADRD). A/D conversion is then performed for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
4. Each time A/D conversion of a single channel completes, the A/D conversion result is stored in the associated A/D Data Register y (ADDRy).
5. When A/D conversion of all the selected channels completes, an ADC12i_ADI (i = 0, 1) interrupt request is generated (no register setting).
6. The ADST bit remains 1 (A/D conversion start) during A/D conversion, and is automatically cleared to 0 when A/D conversion of all the selected channels completes. Then the ADC12 enters a wait state.

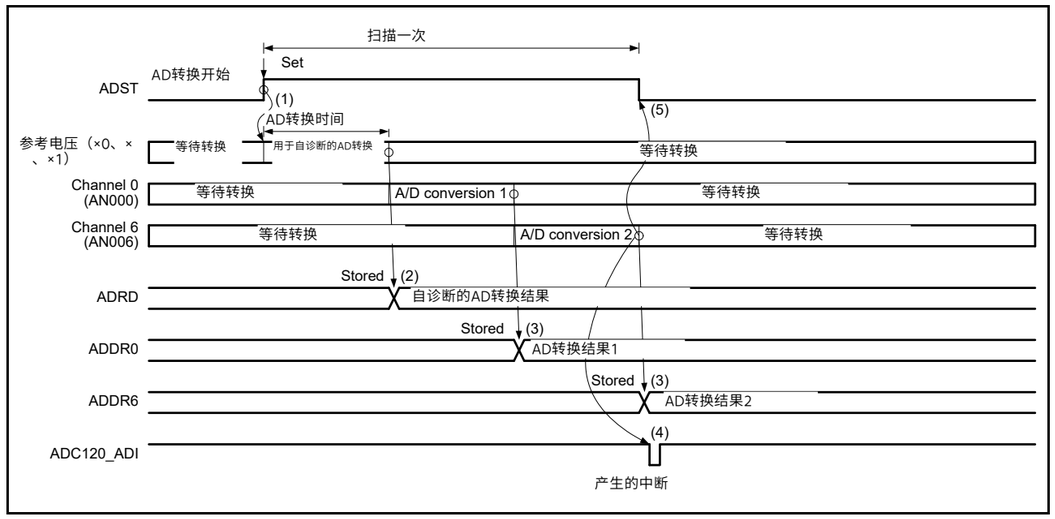


Figure 47.10 使用自诊断选择AN000和AN006时单次扫描模式下的基本操作示例

47.3.2.5 通道专用采样保持电路和禁用连续采样的通道选择和自诊断

Whenchannelsandself-diagnosisareselectedandachannel-dedicatedsample-and-holdcircuitisusedwhileconti nuoussamplingisdisabled thesample-and-holdoperationisperformedfirst andthenADconversionisperformedo nceforthereferencevoltageVREFH0（单元0）或VREFH（单元1）（×0、×12或×1）提供给ADC12。之后，仅对所选通道的模拟输入执行一次AD转换。

操作如下：

1. 模拟输入采样开始于其专用采样保持电路的所有通道，当ADCSR.ADST位通过软件触发、同步触发输入(ELC)或异步触发输入设置为1（AD转换开始）。
2. 采样保持操作后，用于自诊断的AD转换开始。
3. 自诊断用AD转换完成后，AD转换结果存储在AD自诊断中数据寄存器(ADRD)。然后对ADANSA0中选择的ANn通道执行D转换，并ADANSA1寄存器，从编号n最小的通道开始。
4. 每次完成单个通道的AD转换，AD转换结果存储在关联的AD中数据寄存器y(ADDRy)。
5. 当所有选定通道的AD转换完成时，会产生一个ADC12i_ADI(i=0 1)中断请求（无寄存器设置）。
6. ADST位在AD转换期间保持1（AD转换开始），并在所有选定通道的AD转换完成时自动清零。然后ADC12进入等待状态。

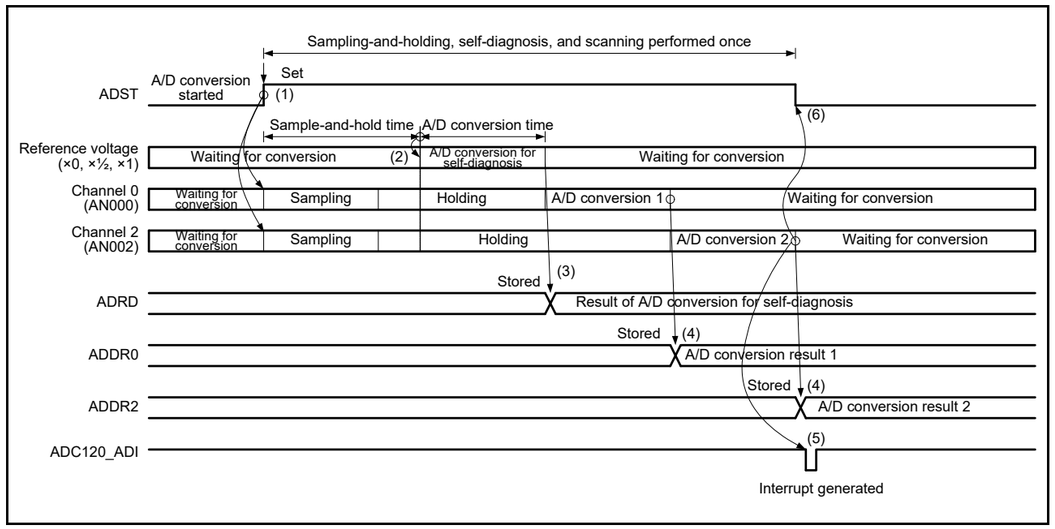


Figure 47.11 Example operation in single scan mode when channel-dedicated sample-and-hold circuits are used, AN000 and AN002 are selected with self-diagnosis, and continuous sampling is disabled

47.3.2.6 Channel selection and self-diagnosis with channel-dedicated sample-and-hold circuits and continuous sampling enabled

When channels and self-diagnosis are selected and a channel-dedicated sample-and-hold circuit is used while continuous sampling is enabled, sample-and-hold operations are performed first, and this is followed by A/D conversion of the reference voltage VREFH0 (unit 0) or VREFH (unit 1) supplied to the ADC12. After that, A/D conversion is performed only once on the analog input of the selected channels.

The operation is as follows:

1. When the ADSHMSR.SHMD bit is set to 1, the sample-and-hold circuits selected in the ADSHCR.SHANS[2:0] bits start continuous sampling.
2. Analog input holding starts for all channels for which the channel-dedicated sample-and-hold circuits are to be used when the ADCSR.ADST bit is set to 1 (A/D conversion start) by a software trigger, input of a synchronous trigger signal (ELC), or input of an asynchronous trigger. Set the ADCSR.ADST bit to 1 after at least 400 ns (when the permissible signal source impedance is 1 kΩ) elapses after the ADSHMSR.SHMD bit is set to 1.
3. After the stabilization time of the sample-and-hold circuits elapses, A/D conversion for self-diagnosis starts.
4. When A/D conversion for self-diagnosis completes, the A/D conversion result is stored in the A/D Self-Diagnosis Data Register (ADRD). A/D conversion is then performed for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
5. Each time A/D conversion of a single channel completes, the A/D conversion result is stored in the associated A/D Data Register y (ADDRy), and the sample-and-hold circuit restarts continuous sampling.
6. When A/D conversion of all the selected channels completes, an ADC12i_ADI (i = 0, 1) interrupt request is generated (no register setting).
7. The ADCSR.ADST bit remains 1 (A/D conversion start) during A/D conversion, and is automatically cleared to 0 when A/D conversion of all the selected channels completes. Then the ADC12 enters a wait state. If this is followed by single scanning, set the continuous sampling time for the sample-and-hold circuits to at least 400 ns (when the permissible signal source impedance is 1 kΩ).
8. When the ADSHMSR.SHMD bit is set to 0, the sample-and-hold circuits stop.

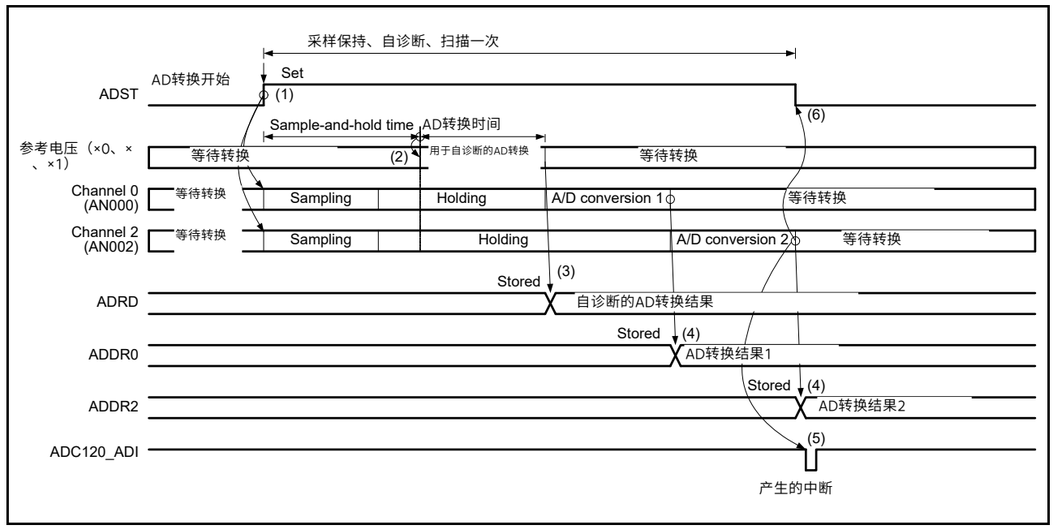


Figure 47.11 使用通道专用采样保持电路、AN000和AN002被选择为具有自诊断功能且连续采样被禁用时的单次扫描模式操作示例

47.3.2.6 通道选择和自诊断，带有通道专用的采样保持电路和连续采样使能

Whenchannelsandself-diagnosisareselectedandachannel-dedicatedsample-and-holdcircuitisusedwhilecontinuoussamplingisenabled sample-and-holdoperationsareperformedfirst andthisisfollowedbyADconversionofthereferencevoltageVREFH0(单元0)或VREFH(单元1)提供给ADC12。之后，仅对所选通道的模拟输入执行一次AD转换。

操作如下：

1. 当ADSHMSR.SHMD位设置为1时，在ADSHCR.SHANS[2:0]位中选择的采样保持电路开始连续采样。
2. 当通过软件触发将ADCSR.ADST位设置为1（AD转换开始）时，将使用通道专用采样保持电路的所有通道开始模拟输入保持，输入同步触发信号(ELC），或异步触发器的输入。在ADSHMSR.SHMD位设置为1后至少经过400ns（当允许的信号源阻抗为1kΩ时）后，将ADCSR.ADST位设置为1。
3. 经过采样保持电路的稳定时间后，开始进行自诊断的A/D转换。
4. 自诊断用AD转换完成后，AD转换结果存储在AD自诊断中数据寄存器(ADRD)。然后对ADANSA0中选择的ANn通道执行D转换，并ADANSA1寄存器，从编号n最小的通道开始。
5. 每次完成单个通道的AD转换，AD转换结果存储在关联的AD中数据寄存器y(ADDRy)，采样保持电路重新开始连续采样。
6. 当所有选定通道的AD转换完成时，会产生一个ADC12i_ADI(i=0 1)中断请求（无寄存器设置）。
7. ADCSR.ADST位在AD转换期间保持1（AD转换开始），并在所有选定通道的AD转换完成时自动清零。然后ADC12进入等待状态。如果随后进行单次扫描，请将采样保持电路的连续采样时间设置为至少400ns（当允许的信号源阻抗为1kΩ时）。
8. 当ADSHMSR.SHMD位设置为0时，采样保持电路停止。

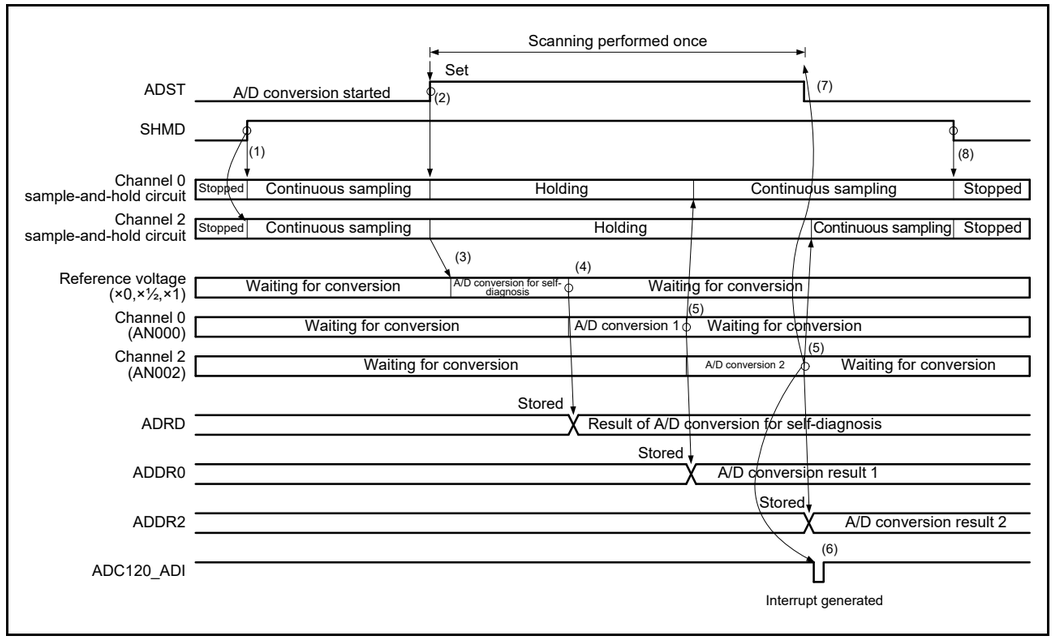


Figure 47.12 Example operation in single scan mode when channel-dedicated sample-and-hold circuits are used, AN000 to AN002 are selected with self-diagnosis, and continuous sampling is enabled

47.3.2.7 A/D conversion of temperature sensor output or internal reference voltage

When the channels and temperature sensor output or internal reference voltage are selected at the same time, A/D conversion is first performed on the analog input of the selected channels, and then A/D conversion is performed once on the temperature sensor output or internal reference voltage. When both temperature sensor output and internal reference voltage are selected, A/D conversion of the temperature sensor output and internal reference voltage is performed, in that order. With the channels deselected, selecting only the temperature sensor output or internal reference voltage is also possible.

The operation is as follows:

1. When a software trigger, synchronous trigger (ELC), or asynchronous trigger sets the ADCSR.ADST bit to 1 (A/D conversion start), A/D conversion is performed for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
2. On completion of A/D conversion on the channels, the result is stored in the associated A/D Data Register y (ADDRy), and then A/D conversion of the temperature sensor output starts.
3. On completion of A/D conversion of the temperature sensor output, the result is stored in the associated A/D Temperature Sensor Data Register (ADTSDR), and then A/D conversion of the internal reference voltage starts.
4. On completion of A/D conversion of the internal reference voltage, the result is stored in the associated A/D Internal Reference Voltage Data Register (ADOCDR), and an ADC12i_ADI (i = 0, 1) interrupt request is generated (no register setting).
5. The ADCSR.ADST bit remains 1 (A/D conversion start) during A/D conversion, and is automatically cleared to 0 on completion of A/D conversion. Then the ADC12 enters a wait state.

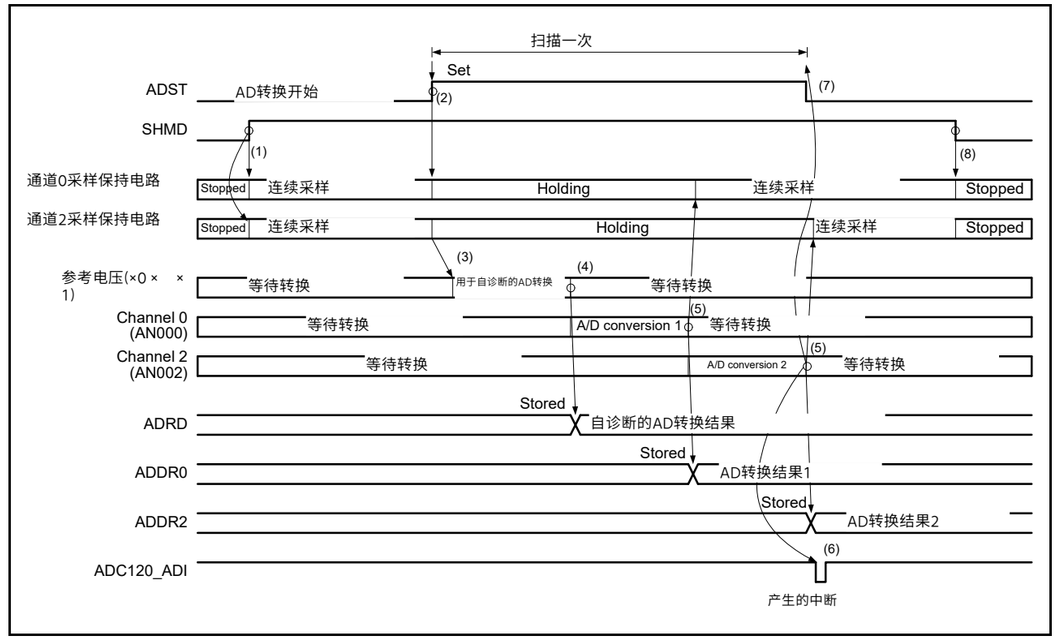


Figure 47.12 使用通道专用采样保持电路、AN000至AN002选择自诊断并启用连续采样时的单次扫描模式操作示例

47.3.2.7 温度传感器输出或内部参考电压的AD转换

当同时选择通道和温度传感器输出或内部参考电压时，首先对所选通道的模拟输入进行AD转换，然后对温度传感器输出或内部参考电压进行一次AD转换。当同时选择温度传感器输出和内部参考电压时，按顺序执行温度传感器输出和内部参考电压的AD转换。取消选择通道后，也可以仅选择温度传感器输出或内部参考电压。

操作如下：

1. 当软件触发、同步触发(ELC)或异步触发将ADCSR.ADST位设置为1（AD转换开始）时，对ADANSA0和ADANSA1寄存器中选择的ANn通道执行AD转换，从具有最小的数n。
2. 在通道上完成AD转换后，结果将存储在相关的AD数据寄存器y(ADDRy)中，然后温度传感器输出的AD转换开始。
3. 温度传感器输出的AD转换完成后，结果存储在相关的AD中
温度传感器数据寄存器(ADTSDR)，然后内部参考电压的AD转换开始。
4. 内部参考电压的AD转换完成后，结果存储在相关的AD中
内部参考电压数据寄存器(AOCDR)，并产生一个ADC12i_ADI(i=0 1)中断请求（无寄存器设置）。
5. ADCSR.ADST位在AD转换期间保持1（AD转换开始），并在AD转换完成时自动清零。然后ADC12进入等待状态。

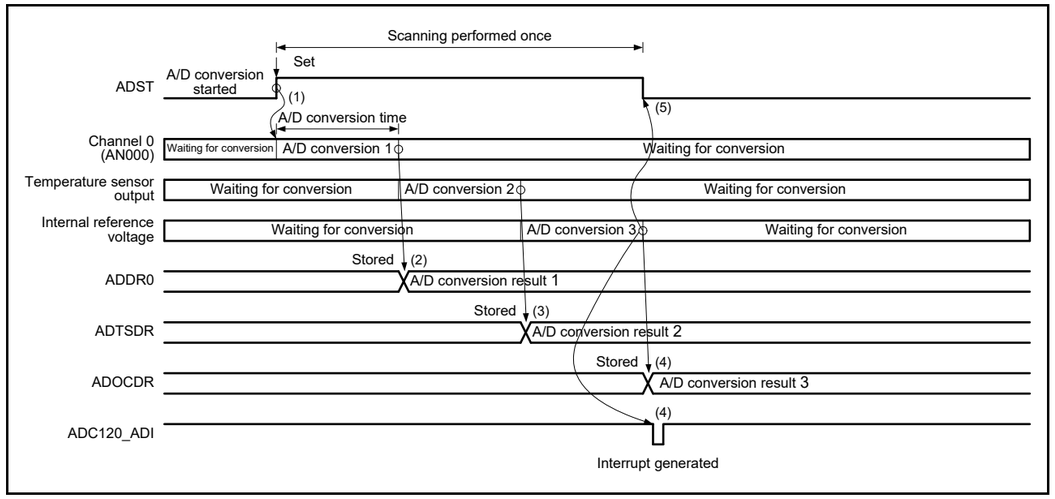


Figure 47.13 Example basic operation in single scan mode when AN000 and temperature sensor output or internal reference voltage are selected

47.3.2.8 A/D conversion in double-trigger mode

When double-trigger mode is selected in single scan mode, two rounds of single scan operation started by a synchronous trigger (ELC) are performed in sequence.

Deselect self-diagnosis, and set the addition/average mode select bits for both temperature sensor output (ADEXICR.TSSA) and internal reference voltage (ADEXICR.OCSA) to 0.

Duplication of A/D conversion data is enabled by setting the channel numbers to be duplicated in the ADCSR.DBLANS[4:0] bits and setting the ADCSR.DBLE to 1. When the ADCSR.DBLE is set to 1, channel selection using the ADANSA0 and ADANSA1 registers is invalid.

In double-trigger mode, select a synchronous trigger (ELC) using the ADSTRGR.TRSA[5:0] bits, and in ADCSR, set the EXTRG bit to 0 and the TRGE bit to 1. Do not use a software trigger.

The operation is as follows:

1. When the ADCSR.ADST bit is set to 1 (A/D conversion start) by a synchronous trigger input (ELC), A/D conversion starts on the single channel selected in the ADCSR.DBLANS[4:0] bits.
2. Each time A/D conversion of a single channel completes, the A/D conversion result is stored in the associated A/D Data Register y (ADDRy).
3. The ADST bit is automatically cleared to 0 and the ADC12 enters a wait state. An ADC12i_ADI (i = 0, 1) interrupt request is not generated.
4. When the ADCSR.ADST bit is set to 1 (A/D conversion start) by the second trigger input, A/D conversion starts on the single channel selected in the ADCSR.DBLANS[4:0] bits.
5. When A/D conversion completes, the result is stored in the A/D Data Duplexing Register (ADDBLDR), which is exclusively used in double-trigger mode.
6. An ADC12i_ADI (i = 0, 1) interrupt request is generated (no register setting).
7. The ADST bit remains 1 (A/D conversion start) during A/D conversion, and is automatically cleared to 0 when A/D conversion completes. Then the ADC12 enters a wait state.

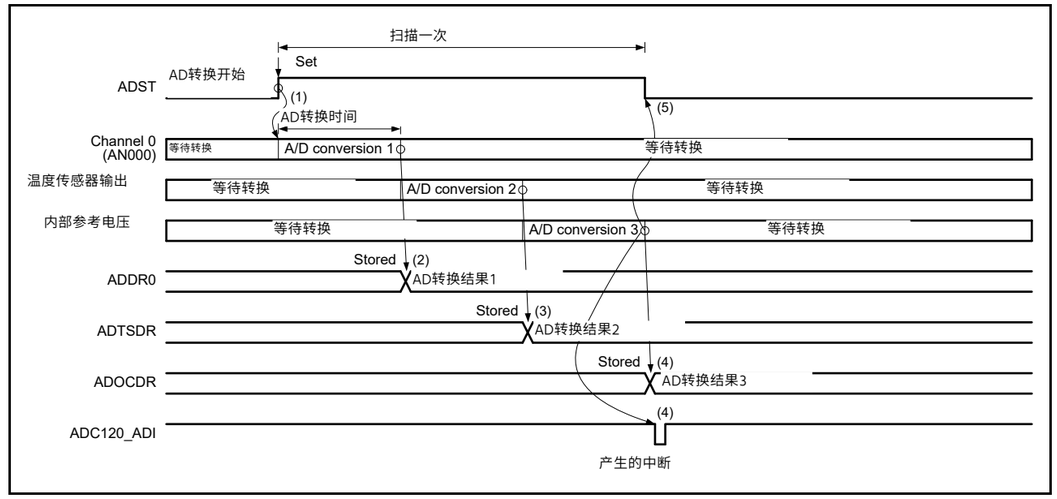


Figure 47.13 选择AN000和温度传感器输出或内部参考电压时单次扫描模式下的基本操作示例

47.3.2.8 双触发模式下的AD转换

在单次扫描模式下选择双触发模式时，由同步触发(ELC)启动的两轮单次扫描操作将依次执行。

取消选择自诊断，并将温度传感器输出(ADEXICR.TSSA)和内部参考电压(ADEXICR.OCSA)的加法平均模式选择位设置为0。

AD转换数据的复制通过在ADCSR.DBLANS[4:0]位并将ADCSR.DBLE设置为1。当ADCSR.DBLE设置为1时，使用ADANSA0和ADANSA1寄存器的通道选择无效。

在双触发模式下，使用ADSTRGR.TRSA[5:0]位选择同步触发(ELC)，在ADCSR中，将EXTRG位设置为0，将TRGE位设置为1。不要使用软件触发。

操作如下：

1. 当同步触发输入(ELC)将ADCSR.ADST位设置为1（AD转换开始）时，AD转换在ADCSR.DBLANS[4:0]位中选择的单个通道上开始。
2. 每次完成单个通道的AD转换，AD转换结果存储在关联的AD中数据寄存器y(ADDRy)。
3. ADST位自动清零，ADC12进入等待状态。不会产生ADC12i_ADI(i=0 1)中断请求。
4. 当第二个触发输入将ADCSR.ADST位设置为1（AD转换开始）时，AD转换在ADCSR.DBLANS[4:0]位中选择的单个通道上开始。
5. 当AD转换完成时，结果存储在AD数据双工寄存器(ADDBLDR)中，该寄存器专用于双触发模式。
6. 产生一个ADC12i_ADI(i=0 1)中断请求（无寄存器设置）。
7. ADST位在AD转换期间保持1（AD转换开始），并在AD转换完成时自动清零。然后ADC12进入等待状态。

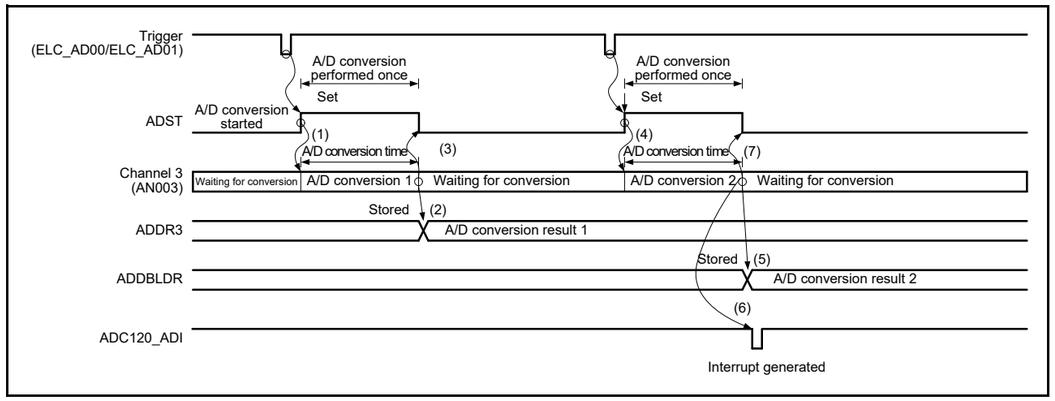


Figure 47.14 Example operation in single scan mode when double-trigger mode is selected and AN003 is duplicated

47.3.2.9 Extended operations when double-trigger mode is selected

When double-trigger mode is selected in single scan mode, and a synchronous trigger (ELC_AD00/ELC_AD01 (unit 0), ELC_AD10/ELC_AD11 (unit 1)) is selected as the trigger for the start of A/D conversion, two rounds of single scan operation are performed.

Deselect self-diagnosis, and set the addition/average mode select bits for both temperature sensor output (ADEXICR.TSSA and ADEXICR.TSSB) and internal reference voltage (ADEXICR.OCSA and ADEXICR.OCSB) to 0.

Duplication of A/D conversion data is enabled by setting the channel numbers to be duplicated in the ADCSR.DBLANS[4:0] bits and setting the ADCSR.DBLE bit to 1. When the ADCSR.DBLE bit is set to 1, channel selection using the ADANSA0 and ADANSA1 registers is invalid.

In extended double-trigger mode, select a synchronous trigger (ELC_AD00/ELC_AD01 (unit 0), ELC_AD10/ELC_AD11 (unit 1)) by setting the ADSTRGR.TRSA[5:0] bits to 0Bh, and in ADCSR, set the EXTRG bit to 0 and the TRGE bit to 1. Do not use a software trigger.

The operation is as follows:

1. When the ADCSR.ADST bit is set to 1 (A/D conversion start) by a synchronous trigger input (ELC_AD00/ELC_AD01 (unit 0), ELC_AD10/ELC_AD11 (unit 1)), A/D conversion starts on the single channel selected in the ADCSR.DBLANS[4:0] bits.
2. When A/D conversion of a single channel completes, the A/D conversion result is stored in the associated A/D Data Register y (ADDRy) and in A/D Data Duplexing Register A (ADDBLDRA) or A/D Data Duplexing Register B (ADDBLDRB) when the trigger of ELC_ADi0 or ELC_ADi1 is input respectively (i=0, 1).
3. The ADCSR.ADST bit is automatically cleared to 0 and the ADC12 enters a wait state. An ADC12i_ADI (i = 0, 1) interrupt request is not generated.
4. When the ADCSR.ADST bit is set to 1 (A/D conversion start) by the second trigger input (ELC_AD00/ELC_AD01 (unit 0), ELC_AD10/ELC_AD11 (unit 1)), A/D conversion starts on the single channel selected in the ADCSR.DBLANS[4:0] bits.
5. When A/D conversion completes, the result is stored in the A/D Data Duplexing Register (ADDBLDR) and in A/D Data Duplexing Register A (ADDBLDRA) or A/D Data Duplexing Register B (ADDBLDRB) when the trigger of ELC_ADi0 or ELC_ADi1 is input respectively (i=0, 1).
6. An ADC12i_ADI (i = 0, 1) interrupt request is generated (no register setting).
7. The ADCSR.ADST bit remains 1 (A/D conversion start) during A/D conversion and is automatically cleared to 0 when A/D conversion completes. Then the ADC12 enters a wait state.

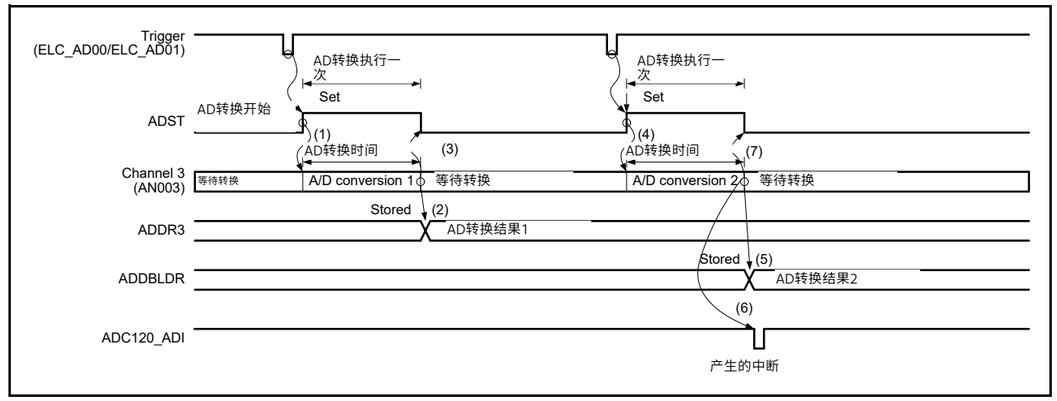


Figure 47.14 选择双触发模式并复制AN003时的单次扫描模式操作示例

47.3.2.9 选择双触发模式时的扩展操作

当在单扫描模式下选择双触发模式时，同步触发（ELC_AD00ELC_AD01（单元0），ELC_AD10ELC_AD11(unit1))被选为AD转换开始的触发器，执行两轮单次扫描操作。

取消选择自诊断，并将温度传感器输出（ADEXICR.TSSA和ADEXICR.TSSB）和内部参考电压（ADEXICR.OCSA和ADEXICR.OCSB）的加法平均模式选择位设置为0。

AD转换数据的复制通过在ADCSR.DBLANS[4:0]位并将ADCSR.DBLE位设置为1。当ADCSR.DBLE位设置为1时，使用ADANSA0和ADANSA1寄存器的通道选择无效。

在扩展双触发模式下，选择同步触发（ELC_AD00ELC_AD01（单元0），ELC_AD10ELC_AD11(unit1))通过将ADSTRGR.TRSA[5:0]位设置为0Bh，并在ADCSR中将EXTRG位设置为0并将TRGE位设置为1。不要使用软件触发。

操作如下：

1. 当同步触发输入（ELC_AD00ELC_AD01（单元0）、ELC_AD10ELC_AD11（单元1））将ADCSR.ADST位设置为1（AD转换开始）时，ADCSR.DBLANS[中选择的单通道上开始AD转换4:0]位。
2. 当单个通道的AD转换完成时，AD转换结果存储在关联的ADData中
   当分别输入ELC_ADi0或ELC_ADi1的触发时(i=0 1)，寄存器y(ADDRy)和AD数据双工寄存器A(ADDBLDRA)或AD数据双工寄存器B(ADDBLDRB)中。
3. ADCSR.ADST位自动清零，ADC12进入等待状态。不会产生ADC12i_ADI(i=0 1)中断请求。
4. 当第二个触发输入（ELC_AD00ELC_AD01（单元0）、ELC_AD10ELC_AD11（单元1））将ADCSR.ADST位设置为1（AD转换开始）时，ADCSR.DBLANS[中选择的单通道开始AD转换4:0]位。
5. 当AD转换完成时，结果存储在AD数据双工寄存器(ADDBLDR)和AD数据双工寄存器A(ADDBLDRA)或AD数据双工寄存器B(ADDBLDRB)中。
   分别输入ELC_ADi0或ELC_ADi1(i=0 1)。
6. 产生一个ADC12i_ADI(i=0 1)中断请求（无寄存器设置）。
7. ADCSR.ADST位在AD转换期间保持1（AD转换开始），并在AD转换完成时自动清零。然后ADC12进入等待状态。

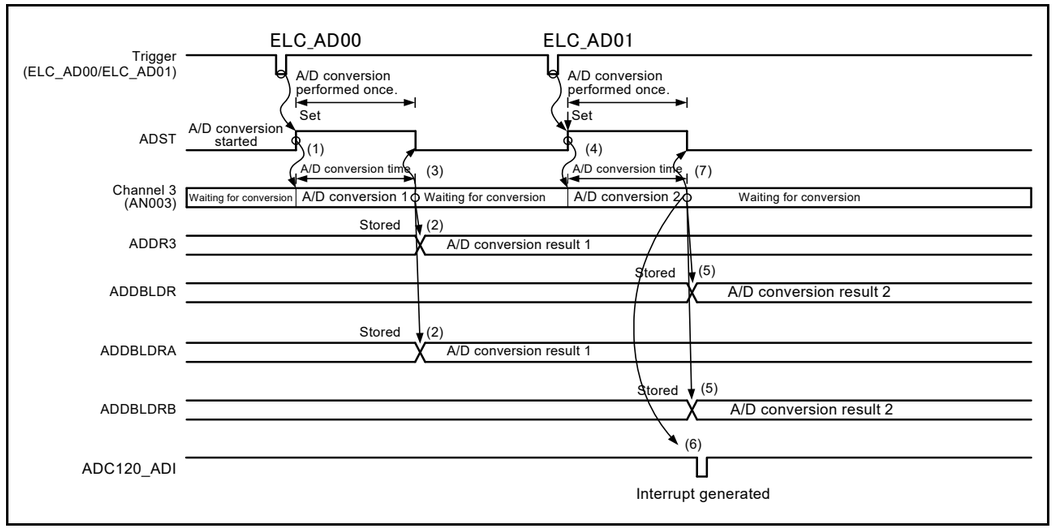


Figure 47.15 Example extended operation in double-trigger mode (1) when duplication is selected for AN003 and ELC_AD00/ELC_AD01 is selected

47.3.3 Continuous Scan Mode

47.3.3.1 Basic operation without channel-dedicated sample-and-hold circuits

In basic operation of continuous scan mode, A/D conversion is performed repeatedly on the analog input of the specified channels.

The operation is as follows:

1. When the ADCSR.ADST bit is set to 1 (A/D conversion start) by a software trigger, synchronous trigger input (ELC), or asynchronous trigger input, A/D conversion is performed for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
2. Each time A/D conversion of a single channel completes, the A/D conversion result is stored in the associated A/D Data Register y (ADDRy).
3. When A/D conversion of all the selected channels completes, an ADC12i_ADI (i = 0,1) interrupt request is generated (no register setting). The ADC12 sequentially starts A/D conversion for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
4. The ADCSR.ADST bit is not automatically cleared, and steps 2 and 3 are repeated as long as the bit remains 1 (A/D conversion start). When the ADCSR.ADST bit is set to 0 (A/D conversion stop), A/D conversion stops and the ADC12 enters a wait state.
5. When the ADST bit is then set to 1 (A/D conversion start), A/D conversion starts again for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.

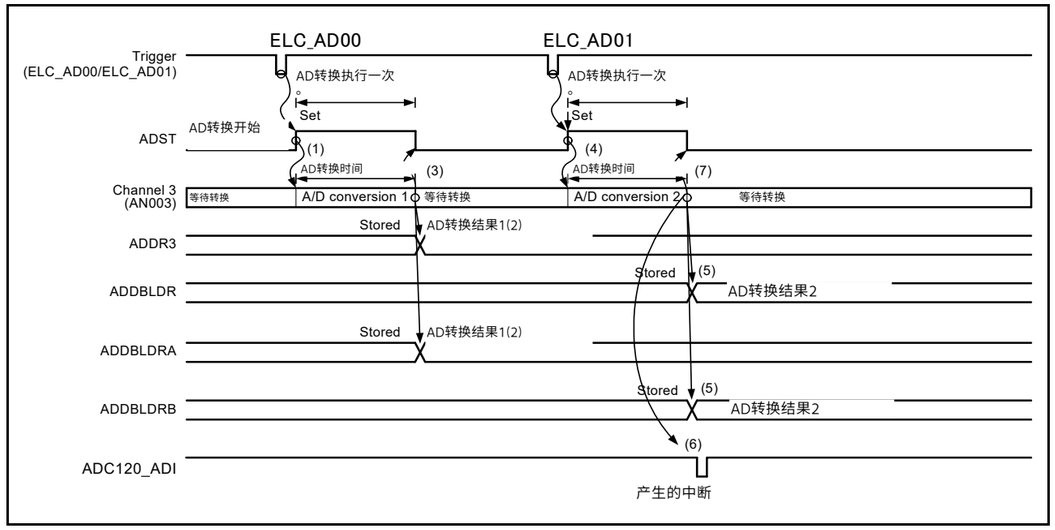


Figure 47.15 当为AN003选择复制并选择ELC_AD00ELC_AD01时，双触发模式下的扩展操作示例(1)

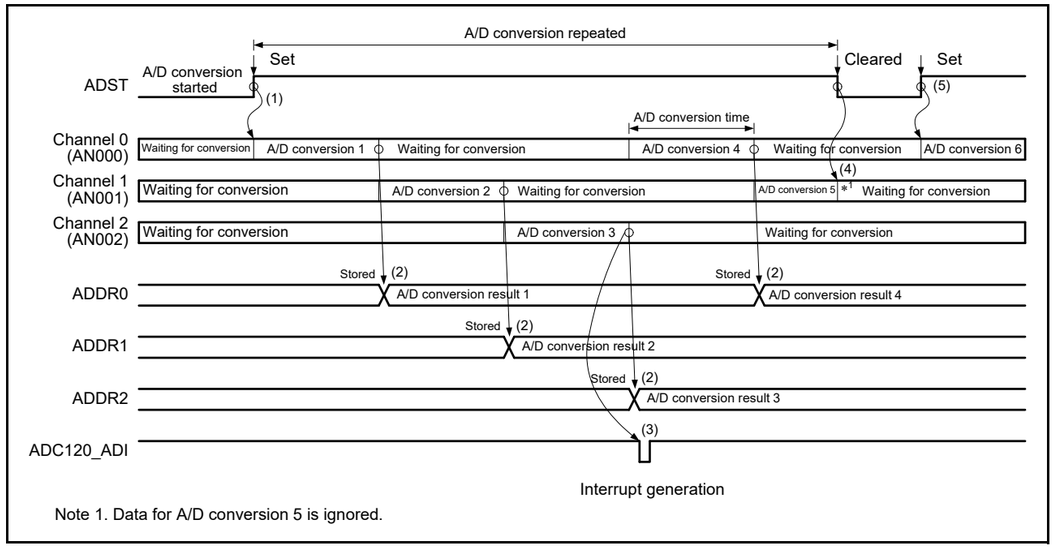
47.3.3 连续扫描模式

47.3.3.1 无通道专用采样保持电路的基本操作

在连续扫描模式的基本操作中，对指定通道的模拟输入重复进行AD转换。

操作如下：

1. 当通过软件触发、同步触发输入(ELC)或异步触发输入将ADCSR.ADST位设置为1（AD转换开始）时，将从ADANSA0和ADANSA1寄存器中选择的ANn通道执行AD转换，从具有最小编号n的通道。
2. 每次完成单个通道的AD转换，AD转换结果存储在关联的AD中数据寄存器y(ADDRy)。
3. 当所有选定通道的AD转换完成时，会产生一个ADC12i_ADI(i=0 1)中断请求（无寄存器设置）。ADC12从编号n最小的通道开始依次启动ADANSA0和ADANSA1寄存器中选择的ANn通道的A/D转换。
4. ADCSR.ADST位不会自动清零，只要该位保持为1（AD转换开始），就会重复步骤2和3。当ADCSR.ADST位设置为0（AD转换停止）时，AD转换停止并且ADC12进入等待状态。
5. 然后当ADST位设置为1（AD转换开始）时，AD转换再次开始在ADANSA0和ADANSA1寄存器中选择的ANn通道，从具有最小编号n的通道开始。



Note 1. Data for A/D conversion 5 is ignored.

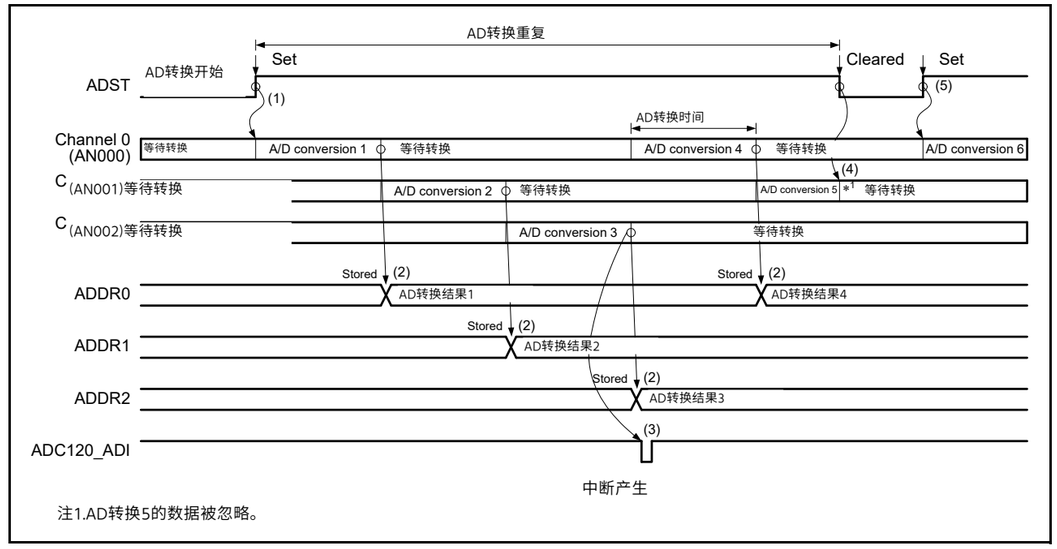
Figure 47.16 Example basic operation in continuous scan mode when AN000 to AN002 are selected

47.3.3.2 Basic operation with channel-dedicated sample-and-hold circuits and continuous sampling disabled

When the channel-dedicated sample-and-hold circuit is used while continuous sampling is disabled, sample-and-hold operation is first performed, and then A/D conversion is repeated on the analog input of all the specified channels. The channels whose dedicated sample-and-hold circuit is to be used can be selected in the SHANS[2:0] bits in ADSHCR.

The operation is as follows:

1. Analog input sampling starts for all channels whose dedicated sample-and-hold circuit is to be used when the ADCSR.ADST bit is set to 1 (A/D conversion start) by a software trigger, synchronous trigger input (ELC), or asynchronous trigger input.
2. After sample-and-hold operation, A/D conversion is performed for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
3. Each time A/D conversion of a single channel completes, the A/D conversion result is stored in the associated A/D Data Register y (ADDRy).
4. When A/D conversion of all the selected channels completes, an ADC12i_ADI (i = 0, 1) interrupt request is generated (no register setting). At the same time, analog input sampling starts for all channels whose dedicated sample-and-hold circuit is to be used.
5. The ADST bit is not automatically cleared, and steps 2 to 4 are repeated as long as the bit remains 1. When the ADST bit is set to 0 (A/D conversion stop), A/D conversion stops and the ADC12 enters a wait state.
6. When the ADST bit is then set to 1 (A/D conversion start), analog input sampling starts again for all channels whose dedicated sample-and-hold circuit is to be used.



注1.AD转换5的数据被忽略。

Figure 47.16 选择AN000至AN002时连续扫描模式下的基本操作示例

47.3.3.2 通道专用采样保持电路和禁用连续采样的基本操作

在禁用连续采样的情况下使用通道专用采样保持电路时，首先执行采样保持操作，然后在所有指定通道的模拟输入上重复AD转换。可以在ADSHCR的SHANS[2:0]位中选择要使用专用采样保持电路的通道。

操作如下：

1. 模拟输入采样开始于其专用采样保持电路的所有通道，当ADCSR.ADST位通过软件触发、同步触发输入(ELC)或异步触发输入设置为1（AD转换开始）。
2. 采样保持操作后，对ADANSA0和ADANSA1寄存器中选择的ANn通道执行AD转换，从编号n最小的通道开始。
3. 每次完成单个通道的AD转换，AD转换结果存储在关联的AD中数据寄存器y(ADDRy)。
4. 当所有选定通道的AD转换完成时，会产生一个ADC12i_ADI(i=0 1)中断请求（无寄存器设置）。同时，对所有要使用专用采样保持电路的通道开始模拟输入采样。
5. ADST位不会自动清零，只要该位保持为1，就会重复步骤2到4。当ADST位设置为0（AD转换停止），AD转换停止，ADC12进入等待状态。
6. 当ADST位随后设置为1（AD转换开始）时，模拟输入采样将重新开始对所有要使用专用采样保持电路的通道进行。

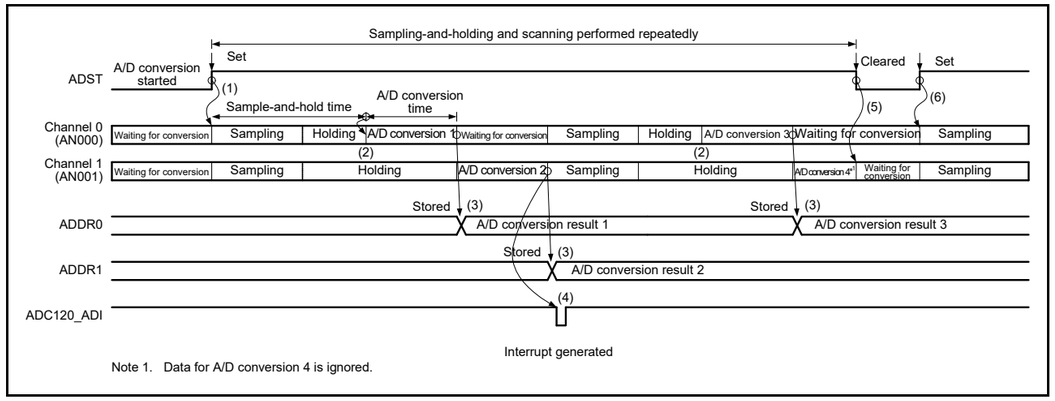


Figure 47.17 Example operation in continuous scan mode when channel-dedicated sample-and-hold circuits are used and AN000 and AN001 are selected

47.3.3.3 Basic operation with channel-dedicated sample-and-hold circuits and continuous sampling enabled

When a channel-dedicated sample-and-hold circuit is used while continuous sampling is enabled, sample-and-hold operations are performed first, after which the analog inputs on all selected channels are A/D-converted as described in this section. The channels for which the channel-dedicated sample-and-hold circuits are to be used can be selected in the ADSHCR.SHANS[2:0] bits.

The operation is as follows:

1. When the ADSHMSR.SHMD bit is set to 1, the sample-and-hold circuits selected in the ADSHCR.SHANS[2:0] bits start continuous sampling.
2. Analog input holding starts for all channels for which the channel-dedicated sample-and-hold circuits are to be used when the ADCSR.ADST bit is set to 1 (A/D conversion start) by a software trigger, input of a synchronous trigger signal (ELC), or input of an asynchronous trigger. Set the ADCSR.ADST bit to 1 after at least 400 ns (when the permissible signal source impedance is 1 kΩ) elapses after the ADSHMSR.SHMD bit is set to 1.
3. After the stabilization time of the sample-and-hold circuits elapses, A/D conversion is performed for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
4. Each time A/D conversion of a single channel completes, the A/D conversion result is stored in the associated A/D Data Register y (ADDRy), and the sample-and-hold circuit restarts continuous sampling.
5. When A/D conversion of all the selected channels completes, an ADC12i_ADI (i = 0, 1) interrupt request is generated (no register setting). Also, analog input holding starts for all channels for which the channel-dedicated sample-and-hold circuits are to be used.
6. The ADCSR.ADST bit is not automatically cleared, and steps 3 to 5 are repeated as long as the bit remains 1. When the ADCSR.ADST bit is set to 0 (A/D conversion stop), A/D conversion stops and the ADC12 enters a wait state.
7. When the ADSHMSR.SHMD bit is set to 0, the sample-and-hold circuits stop.
8. When the ADSHMSR.SHMD bit is then set to 1, the sample-and-hold circuits selected in the ADSHCR.SHANS[2:0] bits start continuous sampling.
9. When the ADCSR.ADST bit is then set to 1 (A/D conversion start), analog input holding starts for all channels for which the channel-dedicated sample-and-hold circuits are to be used.

Note: If continuous scanning is performed when only the channels with the sample-and-hold circuits are selected, time for continuous sampling cannot be secured in the second and subsequent continuous scans. When continuous sampling by the channel-dedicated sample-and-hold circuits is enabled for continuous scanning, select one or more channels among AN003 to AN007 and AN016 to AN020, temperature sensor output, and internal reference voltage for unit 0, and AN103, AN105 to AN107 and AN116 to AN119, temperature sensor output, and internal

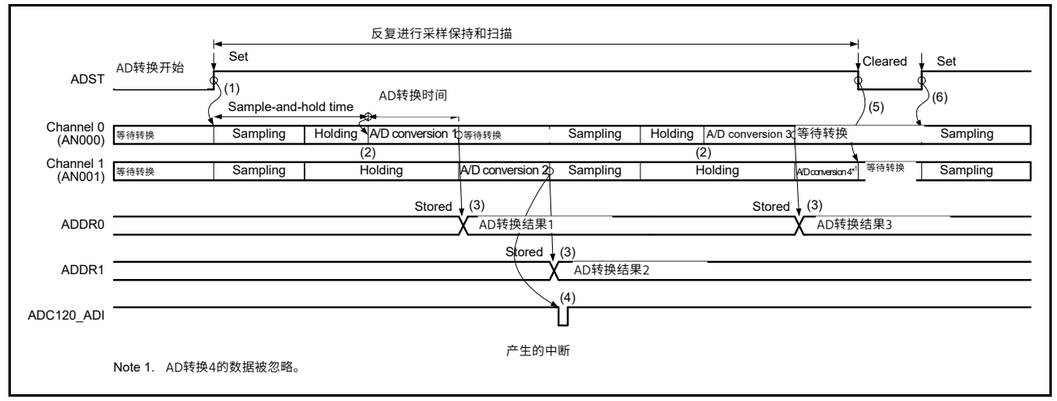


Figure 47.17 使用通道专用采样保持电路并选择AN000和AN001时连续扫描模式下的示例操作

47.3.3.3 具有通道专用采样保持电路和连续采样的基本操作

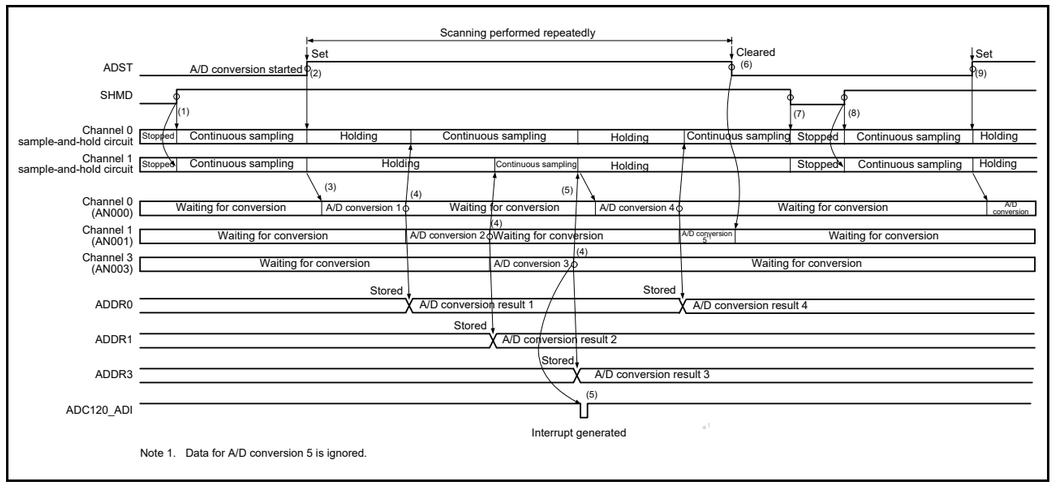
如果在启用连续采样的情况下使用通道专用的采样保持电路，则首先执行采样保持操作，然后将所有选定通道上的模拟输入进行AD转换，如本节所述。可以在ADSHCR.SHANS[2:0]位中选择要使用通道专用采样保持电路的通道。

操作如下：

1. 当ADSHMSR.SHMD位设置为1时，在ADSHCR.SHANS[2:0]位中选择的采样保持电路开始连续采样。
2. 当通过软件触发将ADCSR.ADST位设置为1（AD转换开始）时，将使用通道专用采样保持电路的所有通道开始模拟输入保持，输入同步触发信号(ELC），或异步触发器的输入。在ADSHMSR.SHMD位设置为1后至少经过400ns（当允许的信号源阻抗为1kΩ时）后，将ADCSR.ADST位设置为1。
3. 经过采样保持电路的稳定时间后，从编号n最小的通道开始，对ADANSA0和ADANSA1寄存器中选择的ANn通道执行AD转换。
4. 每次完成单个通道的AD转换，AD转换结果存储在关联的AD中数据寄存器y(ADDRy)，采样保持电路重新开始连续采样。
5. 当所有选定通道的AD转换完成时，会产生一个ADC12i_ADI(i=0 1)中断请求（无寄存器设置）。此外，对于要使用通道专用采样保持电路的所有通道，模拟输入保持开始。
6. ADCSR.ADST位不会自动清零，只要该位保持1，就会重复步骤3到5。当ADCSR.ADST位设置为0（AD转换停止）时，AD转换停止，ADC12进入等待状态。
7. 当ADSHMSR.SHMD位设置为0时，采样保持电路停止。
8. 当ADSHMSR.SHMD位被设置为1时，在ADSHCR.SHANS[2:0]位开始连续采样。
9. 然后，当ADCSR.ADST位设置为1（AD转换开始）时，将开始使用通道专用采样保持电路的所有通道的模拟输入保持。

Note: 如果在仅选择带有采样保持电路的通道时执行连续扫描，则在第二次和随后的连续扫描中无法确保连续采样的时间。当启用通道专用采样保持电路的连续采样以进行连续扫描时，在AN003至AN007和AN016至AN020、温度传感器输出和单元0的内部参考电压以及AN103、AN105中选择一个或多个通道到AN107和AN116到AN119，温度传感器输出和内部

reference voltage for unit 1, and set the continuous sampling time for the sample-and-hold circuits to at least 400 ns (when the permissible signal source impedance is 1 kΩ).



Note 1. Data for A/D conversion 5 is ignored.

Figure 47.18 Example operation in continuous scan mode when channel-dedicated sample-and-hold circuits are used, AN000, AN001, and AN003 are selected, and continuous sampling is enabled

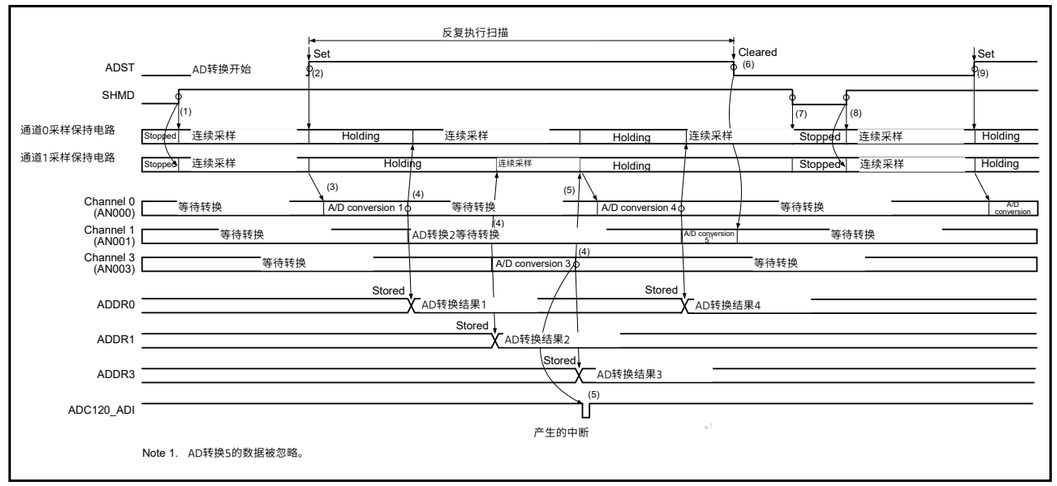
47.3.3.4 Channel selection and self-diagnosis without channel-dedicated sample-and-hold circuits

When channels and self-diagnosis are selected at the same time, A/D conversion is first performed for the reference voltage VREFH0 (unit 0) or VREFH (unit 1) (×0, ×1/2, or ×1) supplied to the ADC12, and then A/D conversion is performed on the analog input of the selected channels, and this sequence is repeated.

The operation is as follows:

1. A/D conversion for self-diagnosis is first started when the ADCSR.ADST bit is set to 1 (A/D conversion start) by a software trigger, synchronous trigger input (ELC), or asynchronous trigger input.
2. When A/D conversion for self-diagnosis completes, the A/D conversion result is stored in the A/D Self-Diagnosis Data Register (ADRD). A/D conversion is then performed for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
3. Each time A/D conversion of a single channel completes, the A/D conversion result is stored in the associated A/D Data Register y (ADDRy).
4. When A/D conversion of all the selected channels completes, an ADC12i_ADI (i = 0, 1) interrupt request is generated (no register setting). At the same time, the ADC12 starts A/D conversion for self-diagnosis and then starts A/D conversion on ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
5. The ADST bit is not automatically cleared, and steps 2 to 4 are repeated as long as the bit remains 1. When the ADST bit is set to 0 (A/D conversion stop), A/D conversion stops and the ADC12 enters a wait state.
6. The ADST bit remains 1 (A/D conversion start) during A/D conversion, and is automatically cleared to 0 when A/D conversion of all the selected channels completes. Then the ADC12 enters a wait state.

单元1的参考电压，并将采样保持电路的连续采样时间设置为至少400ns（当允许的信号源阻抗为1kΩ时）。



Note 1. AD转换5的数据被忽略。

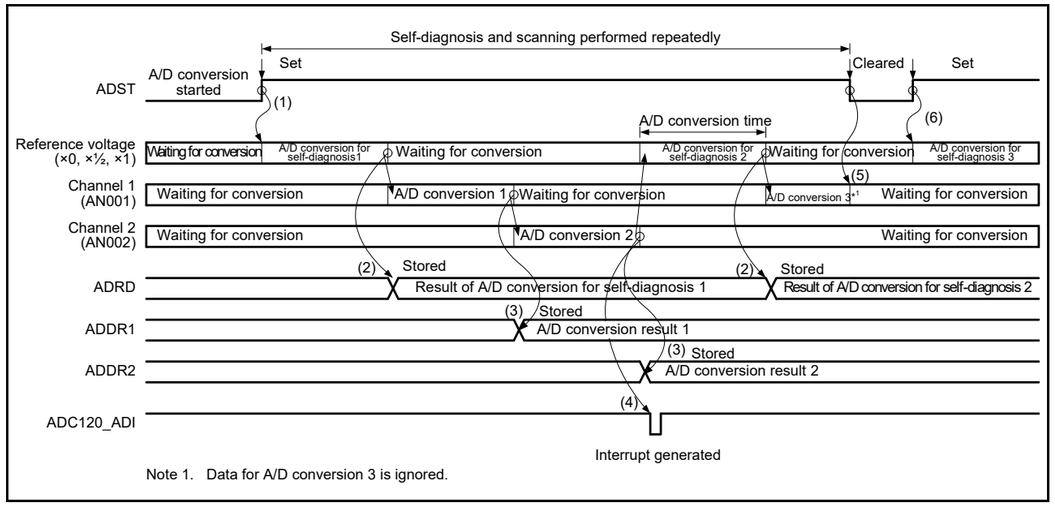
Figure 47.18 使用通道专用采样保持电路、选择AN000、AN001和AN003并启用连续采样时连续扫描模式下的示例操作

47.3.3.4 通道选择和自诊断，无需通道专用的采样和保持电路

当同时选择通道和自诊断时，首先对提供给ADC12的参考电压VREFH0（单元0）或VREFH（单元1）（×0、×12或×1）进行AD转换，然后对所选通道的模拟输入进行AD转换，并重复此序列。

操作如下：

1. 通过软件触发、同步触发输入(ELC)或异步触发输入将ADCSR.ADST位设置为1（AD转换开始）时，首先启动用于自诊断的D转换。
2. 自诊断用AD转换完成后，AD转换结果存储在AD自诊断中
数据寄存器(ADRD)。然后对ADANSA0中选择的ANn通道执行D转换，并
ADANSA1寄存器，从编号n最小的通道开始。
3. 每次完成单个通道的AD转换，AD转换结果存储在关联的AD中
数据寄存器y(ADDRy)。
4. 当所有选定通道的AD转换完成时，会产生一个ADC12i_ADI(i=0 1)中断请求（无寄存器设置）。同时，ADC12启动AD转换以进行自诊断，然后从编号n最小的通道开始对ADANSA0和ADANSA1寄存器中选择的ANn通道进行AD转换。
5. ADST位不会自动清零，只要该位保持为1，就会重复步骤2到4。当
ADST位设置为0（AD转换停止），AD转换停止，ADC12进入等待状态。
6. ADST位在AD转换期间保持1（AD转换开始），并在所有选定通道的AD转换完成时自动清零。然后ADC12进入等待状态。



Note 1. Data for A/D conversion 3 is ignored.

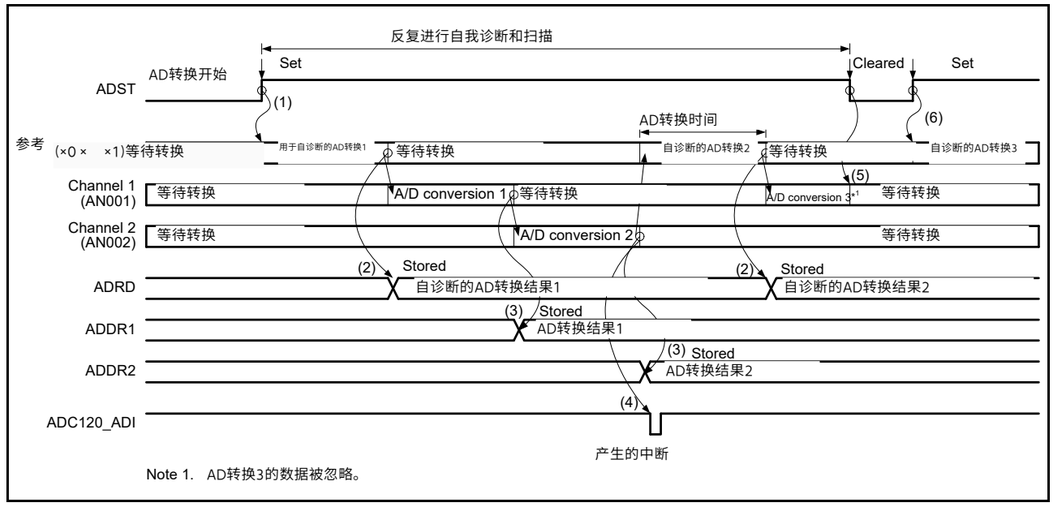
Figure 47.19 Example basic operation in continuous scan mode when AN001 and AN002 are selected with self-diagnosis

47.3.3.5 Channel selection and self-diagnosis with channel-dedicated sample-and-hold circuits and continuous sampling disabled

When channels and self-diagnosis are selected and a channel-dedicated sample-and-hold circuit is used while continuous sampling is disabled, sample-and- hold operation is first performed, and then A/D conversion is performed for the reference voltage VREFH0 (unit 0) or VREFH (unit 1) (×0, ×1/2, or ×1) supplied to the ADC12, and then A/D conversion is performed on the analog input of the selected channels, and this sequence is repeated.

The operation is as follows:

1. Analog input sampling starts for all channels whose dedicated sample-and-hold circuit is to be used when the ADCSR.ADST bit is set to 1 (A/D conversion start) by a software trigger, synchronous trigger input (ELC), or asynchronous trigger input.
2. After sample-and-hold operation, A/D conversion for self-diagnosis starts.
3. When A/D conversion for self-diagnosis completes, the A/D conversion result is stored in the A/D Self-Diagnosis Data Register (ADRD). A/D conversion is then performed for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
4. Each time A/D conversion of a single channel completes, the A/D conversion result is stored in the associated A/D Data Register y (ADDRy).
5. When A/D conversion of all the selected channels completes, an ADC12i_ADI (i = 0, 1) interrupt request is generated (no register setting). At the same time, analog input sampling starts for all channels whose dedicated sample-and-hold circuit is to be used.
6. The ADST bit is not automatically cleared, and steps 2 to 5 are repeated as long as the bit remains 1. When the ADST bit is set to 0 (A/D conversion stop), A/D conversion stops and the ADC12 enters a wait state.
7. When the ADST bit is then set to 1 (A/D conversion start), analog input sampling starts again for all channels whose dedicated sample-and-hold circuit is to be used.



Note 1. AD转换3的数据被忽略。

Figure 47.19 使用自诊断选择AN001和AN002时连续扫描模式下的基本操作示例

47.3.3.5 通道专用采样保持电路和禁用连续采样的通道选择和自诊断

Whenchannelsandself-diagnosisareselectedandachannel-dedicatedsample-and-holdcircuitisusedwhileconti nuoussamplingisdisabled sample-andholdoperationisfirstperformed andthenADconversionisperformedforther eferencevoltageVREFH0(unit0)或VREFH（单元1）（×0、×12或×1）提供给ADC12，然后对所选通道的模拟输入执行AD转换，并重复此序列。

操作如下：

1. 模拟输入采样开始于其专用采样保持电路的所有通道，当ADCSR.ADST位通过软件触发、同步触发输入(ELC)或异步触发输入设置为1（AD转换开始）。
2. 采样保持操作后，用于自诊断的AD转换开始。
3. 自诊断用AD转换完成后，AD转换结果存储在AD自诊断中数据寄存器(ADRD)。然后对ADANSA0中选择的ANn通道执行D转换，并ADANSA1寄存器，从编号n最小的通道开始。
4. 每次完成单个通道的AD转换，AD转换结果存储在关联的AD中数据寄存器y(ADDRy)。
5. 当所有选定通道的AD转换完成时，会产生一个ADC12i_ADI(i=0 1)中断请求（无寄存器设置）。同时，对所有要使用专用采样保持电路的通道开始模拟输入采样。
6. ADST位不会自动清零，只要该位保持为1，就会重复步骤2到5。当ADST位设置为0（AD转换停止），AD转换停止，ADC12进入等待状态。
7. 当ADST位随后设置为1（AD转换开始）时，模拟输入采样将重新开始对所有要使用专用采样保持电路的通道进行。

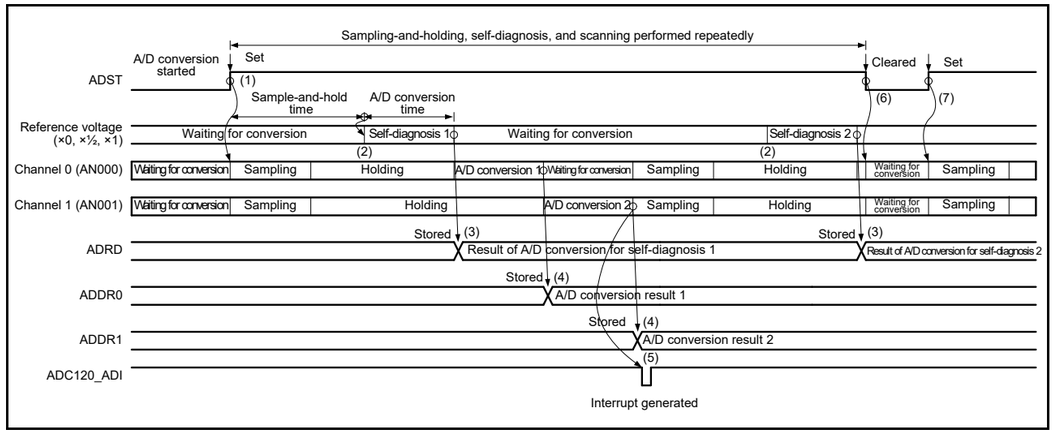


Figure 47.20 Example operation in continuous scan mode when channel-dedicated sample-and-hold circuits are used and AN000 and AN001 are selected with self-diagnosis

47.3.3.6 Channel selection and self-diagnosis with channel-dedicated sample-and-hold circuits and continuous sampling enabled

When channels and self-diagnosis are selected and a channel-dedicated sample-and-hold circuit is used while continuous sampling is enabled, sample-and-hold operation is first performed, and this is followed by A/D conversion of the reference voltage VREFH0 (unit 0) or VREFH (unit 1) (×0, ×1/2, or ×1) supplied to the ADC12. After that, A/D conversion is performed on the analog input of the selected channels, and this sequence is repeated.

The operation is as follows:

1. When the ADSHMSR.SHMD bit is set to 1, the sample-and-hold circuits selected in the ADSHCR.SHANS[2:0] bits start continuous sampling.
2. Analog input holding starts for all channels for which the channel-dedicated sample-and-hold circuits are to be used when the ADCSR.ADST bit is set to 1 (A/D conversion start) by a software trigger, input of a synchronous trigger signal (ELC), or input of an asynchronous trigger. Set the ADCSR.ADST bit to 1 after at least 400 ns (when the permissible signal source impedance is 1 kΩ) elapses after the ADSHMSR.SHMD bit is set to 1.
3. After the stabilization time of the sample-and-hold circuits elapses, A/D conversion for self-diagnosis starts.
4. When A/D conversion for self-diagnosis completes, the A/D conversion result is stored in the A/D Self-Diagnosis Data Register (ADRD). A/D conversion is then performed for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
5. Each time A/D conversion of a single channel completes, the A/D conversion result is stored in the associated A/D Data Register y (ADDRy), and the sample-and-hold circuit restarts continuous sampling.
6. When A/D conversion of all the selected channels completes, an ADC12i_ADI (i = 0, 1) interrupt request is generated (no register setting). Also, analog input holding starts for all channels for which the channel-dedicated sample-and-hold circuits are to be used.
7. The ADCSR.ADST bit is not automatically cleared, and steps 3 to 6 are repeated as long as the bit remains 1. When the ADCSR.ADST bit is set to 0 (A/D conversion stop), A/D conversion stops and the ADC12 enters a wait state.
8. When the ADSHMSR.SHMD bit is set to 0, the sample-and-hold circuits stop.
9. When the ADSHMSR.SHMD bit is then set to 1, the sample-and-hold circuits selected in the ADSHCR.SHANS[2:0] bits start continuous sampling.
10. When the ADCSR.ADST bit is then set to 1 (A/D conversion start), analog input holding starts for all channels for which the channel-dedicated sample-and-hold circuits are to be used.

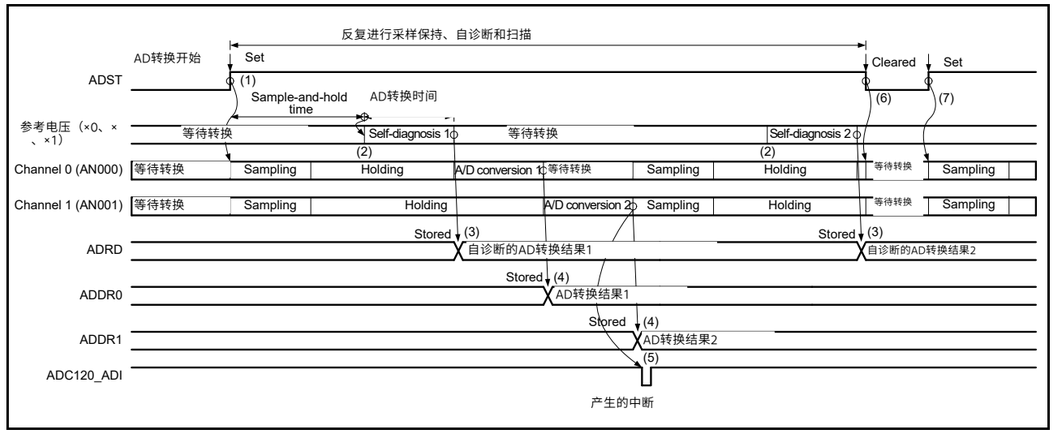


Figure 47.20 使用通道专用采样保持电路并通过自诊断选择AN000和AN001时连续扫描模式下的示例操作

47.3.3.6 通道选择和自诊断，带有通道专用的采样保持电路和连续采样使能

Whenchannelsandself-diagnosisareselectedandachannel-dedicatedsample-and-holdcircuitisusedwhilecontinuoussamplingisenabled sample-and-holdoperationisfirstperformed andthisisfollowedbyADconversionoftheferencevoltageVREFH0(单元0）或VREFH（单元1）（×0、×12或×1）提供给ADC12。之后，对所选通道的模拟输入执行AD转换，并重复此序列。

操作如下：

1. 当ADSHMSR.SHMD位设置为1时，在ADSHCR.SHANS[2:0]位中选择的采样保持电路开始连续采样。
2. 当通过软件触发将ADCSR.ADST位设置为1（AD转换开始）时，将使用通道专用采样保持电路的所有通道开始模拟输入保持，输入同步触发信号(ELC），或异步触发器的输入。在ADSHMSR.SHMD位设置为1后至少经过400ns（当允许的信号源阻抗为1kΩ时）后，将ADCSR.ADST位设置为1。
3. 经过采样保持电路的稳定时间后，开始进行自诊断的A/D转换。
4. 自诊断用AD转换完成后，AD转换结果存储在AD自诊断中数据寄存器(ADRD)。然后对ADANSA0中选择的ANn通道执行D转换，并ADANSA1寄存器，从编号n最小的通道开始。
5. 每次完成单个通道的AD转换，AD转换结果存储在关联的AD中数据寄存器y(ADDRy)，采样保持电路重新开始连续采样。
6. 当所有选定通道的AD转换完成时，会产生一个ADC12i_ADI(i=0 1)中断请求（无寄存器设置）。此外，对于要使用通道专用采样保持电路的所有通道，模拟输入保持开始。
7. ADCSR.ADST位不会自动清零，只要该位保持1，就重复步骤3到6。当ADCSR.ADST位设置为0（AD转换停止）时，AD转换停止，ADC12进入等待状态。
8. 当ADSHMSR.SHMD位设置为0时，采样保持电路停止。
9. 当ADSHMSR.SHMD位被设置为1时，在ADSHCR.SHANS[2:0]位开始连续采样。

10.当ADCSR.ADST位被设置为1（AD转换开始）时，所有通道的模拟输入保持开始，所有通道都将使用通道专用的采样保持电路。

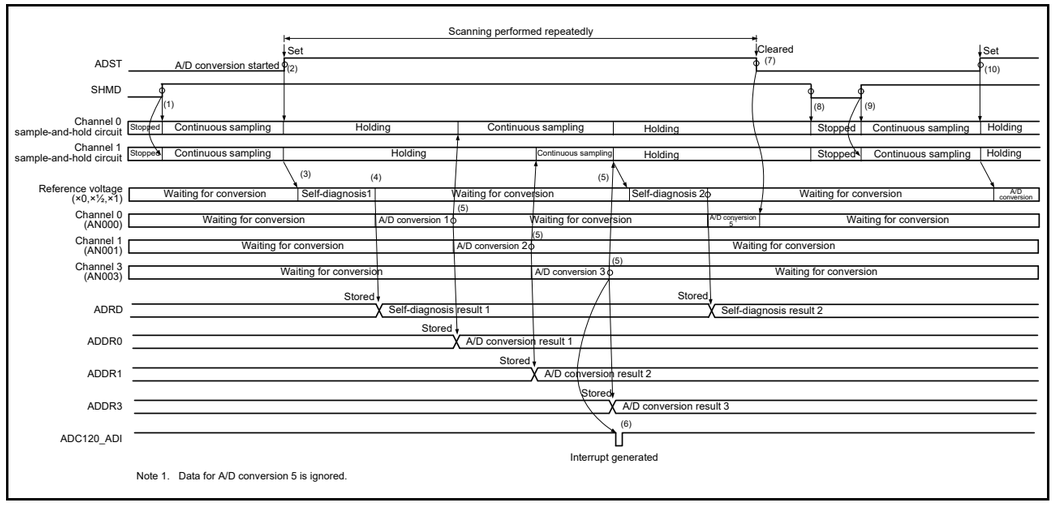


Figure 47.21 Example operation in continuous scan mode when channel-dedicated sample-and-hold circuits are used, AN000, AN001, and AN003 are selected with self-diagnosis, and continuous sampling is enabled

47.3.3.7 A/D conversion of temperature sensor output or internal reference voltage

When the channels and temperature sensor output or internal reference voltage are selected at the same time, A/D conversion is first performed on the analog input of the selected channels, and then A/D conversion of the temperature sensor output or internal reference voltage is repeated. When both temperature sensor output and internal reference voltage are selected, A/D conversion of the temperature sensor output and internal reference voltage is performed, in that order.

With the channels deselected, selecting only the temperature sensor output or internal reference voltage is also possible.

The operation is as follows:

1. When a software trigger, synchronous trigger (ELC), or asynchronous trigger sets the ADCSR.ADST bit to 1 (A/D conversion start), A/D conversion is performed for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the smallest number n.
2. On completion of A/D conversion on the channels, the result is stored in the associated A/D Data Register y (ADDRy), and then A/D conversion of temperature sensor output starts.
3. On completion of A/D conversion of the temperature sensor output, the result is stored in the associated A/D Temperature Sensor Data Register (ADTSDR), and then A/D conversion of internal reference voltage starts.
4. On completion of A/D conversion of the internal reference voltage, the result is stored in the associated A/D Internal Reference Voltage Data Register (ADOCDR), and an ADC12i_ADI interrupt request is generated. In addition, the ADC12 continuously starts A/D conversion for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the lowest number n.
5. The ADCSR.ADST bit is not cleared automatically, and steps 2 to 4 are repeated as long as this bit remains set to 1. When the ADCSR.ADST bit is set to 0 (A/D conversion stop), A/D conversion stops and the ADC12 enters a wait state.
6. When the ADCSR.ADST bit is then set to 1 (A/D conversion start), A/D conversion starts again for the ANn channels selected in the ADANSA0 and ADANSA1 registers, starting from the channel with the lowest number n.

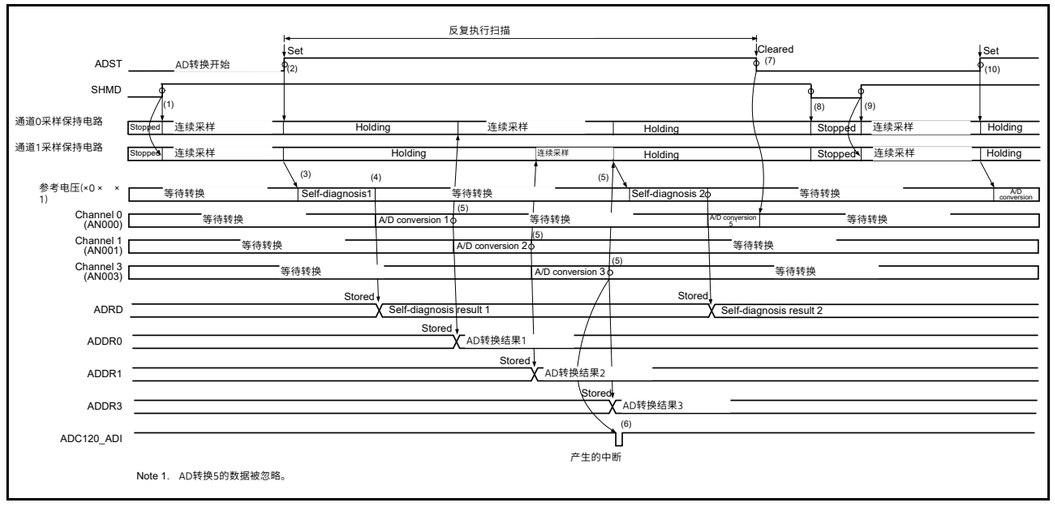


Figure 47.21 使用通道专用采样保持电路、AN000、AN001和AN003选择并进行自诊断并启用连续采样时在连续扫描模式下的示例操作

47.3.3.7 温度传感器输出或内部参考电压的AD转换

当同时选择通道和温度传感器输出或内部参考电压时，首先对所选通道的模拟输入进行AD转换，然后重复温度传感器输出或内部参考电压的AD转换。当同时选择温度传感器输出和内部参考电压时，按顺序执行温度传感器输出和内部参考电压的AD转换。

取消选择通道后，也可以仅选择温度传感器输出或内部参考电压。

操作如下：

1. 当软件触发、同步触发(ELC)或异步触发将ADCSR.ADST位设置为1（AD转换开始）时，对ADANSA0和ADANSA1寄存器中选择的ANn通道执行AD转换，从具有最小的数n。
2. 在通道上完成AD转换后，结果将存储在相关的AD数据寄存器y(ADDRy)中，然后温度传感器输出的AD转换开始。
3. 温度传感器输出的AD转换完成后，结果存储在相关的AD温度传感器数据寄存器(ADTSDR)中，然后内部参考电压的AD转换开始。
4. 内部参考电压的AD转换完成后，结果存储在相关的AD中
内部参考电压数据寄存器(AOCDR)，并产生ADC12i_ADI中断请求。此外，ADC12连续启动ADANSA0和ADANSA1寄存器中选择的ANn通道的AD转换，从编号最小的通道n开始。
5. ADCSR.ADST位不会自动清零，只要该位保持设置为1，就会重复步骤2到4。当ADCSR.ADST位设置为0（AD转换停止）时，AD转换停止并且ADC12进入等待状态。
6. 当ADCSR.ADST位随后设置为1（AD转换开始）时，AD转换再次开始在ADANSA0和ADANSA1寄存器中选择的ANn通道，从编号最小的通道n开始。

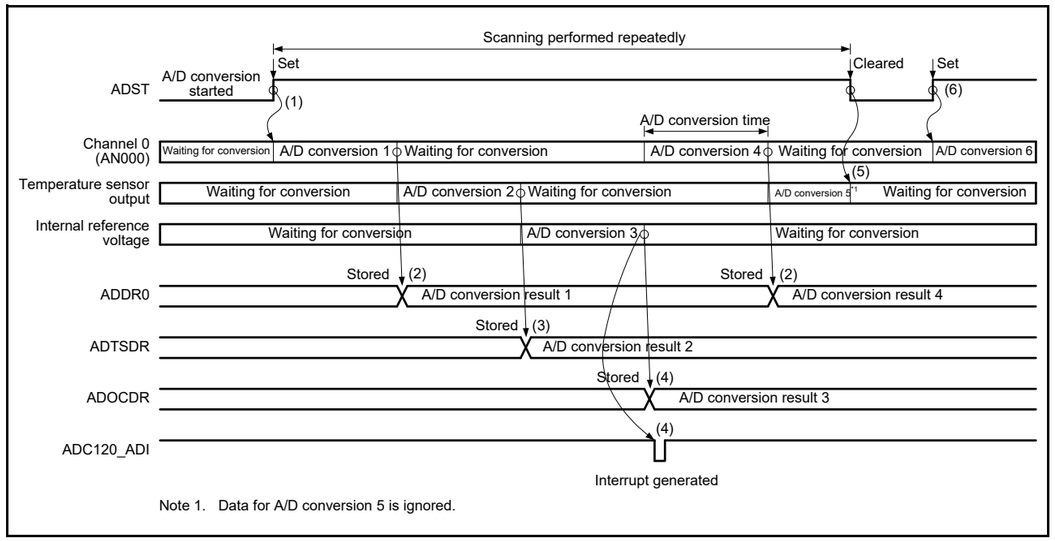


Figure 47.22 Example basic operation in continuous scan mode when AN000 and temperature sensor output or internal reference voltage are selected

47.3.4 Group Scan Mode

47.3.4.1 Basic operation

In group scan mode, A/D conversion is performed once on the analog inputs of all the specified channels in Group A and Group B after scanning is started by a synchronous trigger (ELC). The scan operation of each group is similar to the scan operation in single scan mode.

The synchronous triggers can be selected in the ADSTRGR.TRSA[5:0] bits for Group A and in the ADSTRGR.TRSB[5:0] bits for Group B. Use different triggers for Group A and Group B to prevent simultaneous A/D conversion of the two groups. Do not use a software trigger.

The Group A channels to be A/D-converted are selected using the ADANSA0 and ADANSA1 registers and the ADEXICR.TSSA and OCSA bits, while the Group B channels to be A/D-converted are selected using the ADANSB0 and ADANSB1 registers and the ADEXICR.TSSB and OCSB bits. Group A and Group B cannot use the same channels.

When self-diagnosis is selected in group scan mode, self-diagnosis is separately executed for Group A and Group B.

The following describes operation in group scan mode using a synchronous trigger from the ELC. In this example, the ELC_AD00 and ELC_AD01 (unit 0), and ELC_AD10 and ELC_AD11 (unit 1) triggers from the ELC are used to start conversion of Group A and Group B, respectively. Also, ELC_AD00 and ELC_AD01 (unit 0), and ELC_AD10 and ELC_AD11 (unit 1) are selected for the GPT event in the associated ELC.ELSRn registers.

The operation is as follows:

1. Scanning of Group A is started by ELC_AD00 (unit 0) or ELC_AD10 (unit 1).
2. When Group A scanning completes, an ADC12i_ADI (i = 0, 1) interrupt is generated (no register setting).
3. Scanning of Group B is started by ELC_AD01 (unit 0) or ELC_AD11 (unit 1).
4. When Group B scanning completes, an ADC12i_GBADI interrupt is generated if the ADCSR.GBADIE bit is 1 (ADC12i_GBADI interrupt when scanning completion is enabled).

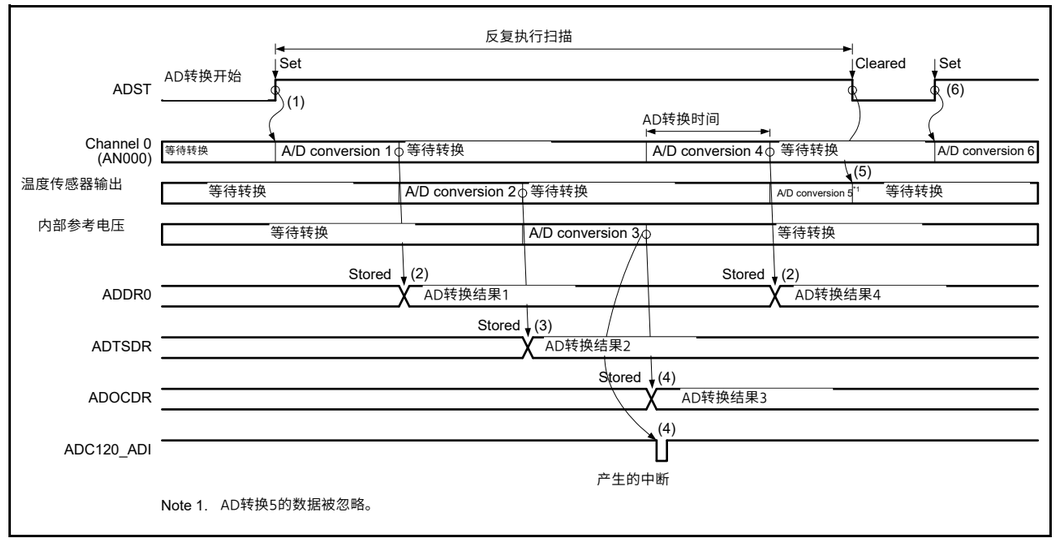


Figure 47.22 选择AN000和温度传感器输出或内部参考电压时连续扫描模式下的基本操作示例

47.3.4 组扫描模式

47.3.4.1 基本操作

在组扫描模式下，由同步触发（ELC）启动扫描后，对A组和B组中所有指定通道的模拟输入进行一次A/D转换。每组的扫描操作类似于单次扫描模式下的扫描操作。

可以在A组的ADSTRGR.TRSA[5:0]位和
B组的ADSTRGR.TRSB[5:0]位。对A组和B组使用不同的触发，以防止两组同时进行AD转换。不要使用软件触发。

使用ADANSA0和ADANSA1寄存器和
ADEXICR.TSSA和OCSA位，而要进行AD转换的B组通道使用ADANSB0和ADANSB1寄存器以及ADEXICR.TSSB和OCSB位进行选择。A组和B组不能使用相同的通道。

在组扫描模式下选择自诊断时，对A组和B组分别执行自诊断。

下面介绍使用来自ELC的同步触发的组扫描模式下的操作。在此示例中，ELC_AD00和ELC_AD01（单元0）以及来自ELC的ELC_AD10和ELC_AD11（单元1）触发器分别用于启动A组和B组的转换。此外，ELC_AD00和ELC_AD01（单元0）以及ELC_AD10和ELC_AD11（单元1）被选择用于相关ELC.ELSRn寄存器中的GPT事件。

操作如下：

1. A组的扫描由ELC_AD00（单元0）或ELC_AD10（单元1）启动。
2. 当A组扫描完成时，会产生ADC12i_ADI(i=0 1)中断（无寄存器设置）。
3. B组的扫描由ELC_AD01（单元0）或ELC_AD11（单元1）启动。
4. 当B组扫描完成时，如果ADCSR.GBADIE位为1（使能扫描完成时ADC12i_GBADI中断），则会产生ADC12i_GBADI中断。

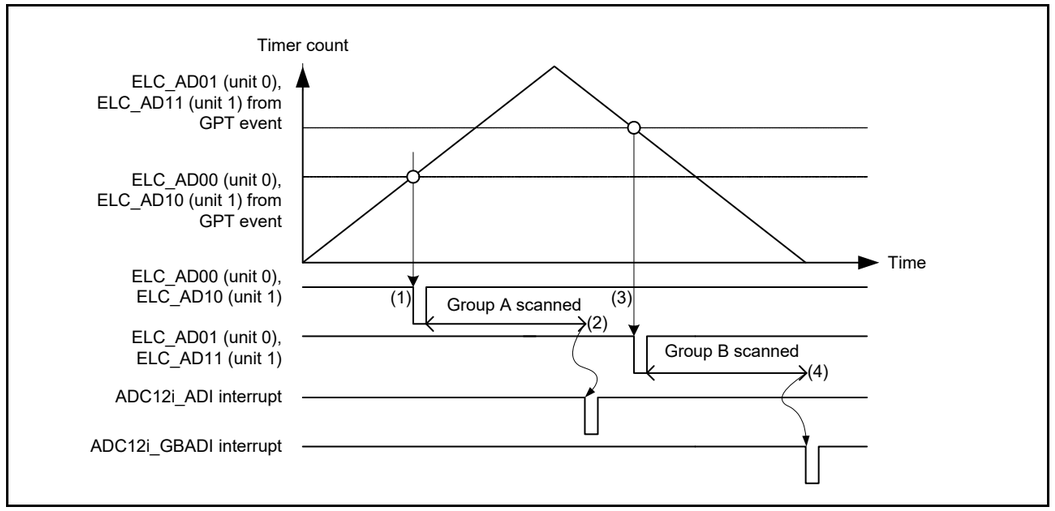


Figure 47.23 Example basic operation in group scan mode when synchronous triggers from the ELC are used

47.3.4.2 A/D conversion in double-trigger mode

When double-trigger mode is selected in group scan mode, two rounds of single scan operation started by a synchronous trigger (ELC) are performed as a sequence for Group A. For Group B, single scan operation started by a synchronous trigger (ELC) is performed once.

In group scan mode, the synchronous triggers can be selected in the TRSA[5:0] bits in ADSTRGR for Group A and in the TRSB[5:0] bits in ADSTRGR for Group B. Use different triggers for Group A and Group B to prevent simultaneous A/D conversion of the two groups. Do not use a software trigger or an asynchronous trigger (ADTRGn).

When ELC_AD00/ELC_AD01 (unit 0), ELC_AD10/ELC_AD11 (unit 1) is selected as the Group A synchronous triggers by setting the ADSTRGR.TRSA[5:0] bits to 0Bh, operation proceeds in extended double-trigger mode.

The channels to be A/D-converted are selected in the DBLANS[4:0] bits in the ADCSR register for Group A and in the ADANSB0 and ADANSB1 registers for Group B. The same channels cannot be selected for both groups.

When double-trigger mode is selected in group scan mode, set the A/D conversion select bits for both the temperature sensor output (ADEXICR.TSSA) and the internal reference voltage (ADEXICR.OCSA) to 0 (deselected). Self-diagnosis cannot be selected when double-trigger mode is selected in group scan mode.

Duplication of A/D conversion data is enabled by setting the channel numbers to be duplicated to the ADCSR.DBLANS[4:0] bits and setting the DBLE bit in ADCSR to 1.

The following describes operation in group scan mode with double-trigger mode using a synchronous trigger from the ELC. In this example, the ELC_AD00 and ELC_AD01 (unit 0), ELC_AD10 and ELC_AD11 (unit 1) triggers from the ELC are used to start conversion of Group A and Group B, respectively. Also, ELC_AD00 and ELC_AD01 (unit 0), ELC_AD10 and ELC_AD11 (unit 1) are selected for the GPT event in the associated ELC.ELSRn registers.

The operation is as follows:

1. Scanning of Group B is started by the ELC_AD00 (unit 0) or ELC_AD10 (unit 1) trigger from the ELC.
2. When Group B scanning completes, an ADC12i_GBADI (i = 0, 1) interrupt is generated if the GBADIE bit in ADCSR is 1 (ADC12i_GBADI interrupt when scanning completion is enabled).
3. The first scan of Group A is started by the first ELC_AD01 (unit 0) or ELC_AD11 (unit 1) trigger.
4. When the first scan of Group A completes, the conversion result is stored in the associated A/D Data Register y (ADDRy); an ADC12i_ADI interrupt request is not generated, regardless of the ADIE bit setting in ADCSR.
5. The second scan of Group A is started by the second ELC_AD01 (unit 0) or ELC_AD11 (unit 1) trigger.

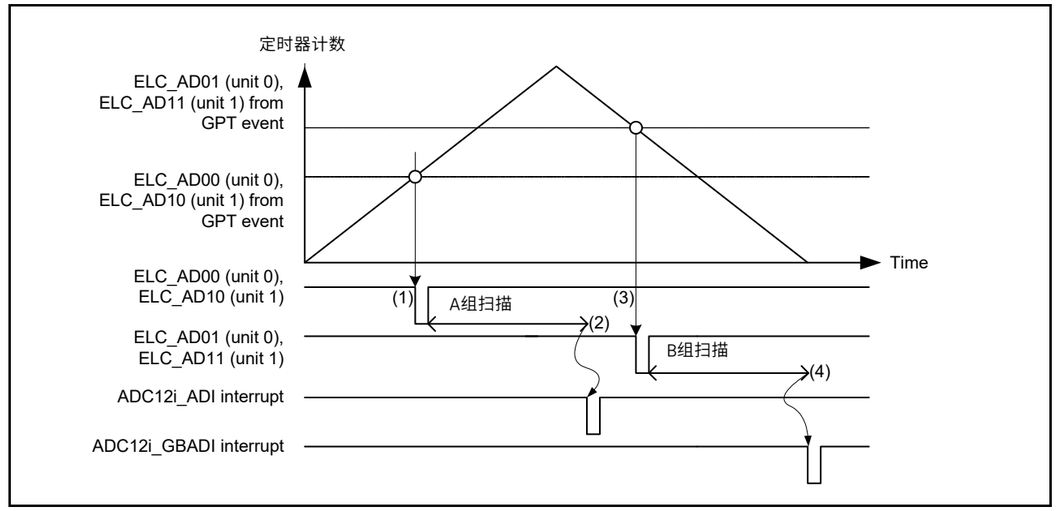


Figure 47.23 使用来自ELC的同步触发时组扫描模式下的基本操作示例

47.3.4.2 双触发模式下的AD转换

在组扫描模式中选择双触发模式时，由同步触发(ELC)启动的两轮单次扫描操作作为A组的顺序执行。对于B组，由同步触发(ELC)启动的单次扫描操作执行一次。

在组扫描模式下，可以在A组的ADSTRGR的TRSA[5:0]位和B组的ADSTRGR的TRSB[5:0]位中选择同步触发。为A组和B组使用不同的触发以防止两组同时进行AD转换。不要使用软件触发或异步触发(ADTRGn)。

当通过将ADSTRGR.TRSA[5:0]位设置为0Bh来选择ELC_AD00ELC_AD01（单元0）、ELC_AD10ELC_AD11（单元1）作为A组同步触发时，操作在扩展双触发模式下进行。

要进行AD转换的通道在A组的ADCSR寄存器的DBLANS[4:0]位和
B组的ADANSB0和ADANSB1寄存器。不能为两个组选择相同的通道。

在组扫描模式下选择双触发模式时，将温度传感器输出(ADEXICR.TSSA)和内部参考电压(ADEXICR.OCSA)的AD转换选择位设置为0（取消选择）。在组扫描模式下选择双触发模式时，不能选择自诊断。

AD转换数据的复制通过将要复制的通道号设置为
ADCSR.DBLANS[4:0]位并将ADCSR中的DBLE位设置为1。

下面介绍使用来自ELC的同步触发的双触发模式的组扫描模式下的操作。在本例中，ELC_AD00和ELC_AD01（单元0）、ELC_AD10和ELC_AD11（单元1）从
ELC分别用于启动A组和B组的转换。此外，ELC_AD00和ELC_AD01（单元0），
在关联的ELC.ELSRn寄存器中为GPT事件选择ELC_AD10和ELC_AD11（单元1）。

操作如下：

1. B组的扫描由来自ELC的ELC_AD00（单元0）或ELC_AD10（单元1）触发器启动。
2. 当B组扫描完成时，如果GBADIE位在
   ADCSR为1（启用扫描完成时ADC12i_GBADI中断）。
3. A组的第一次扫描由第一个ELC_AD01（单元0）或ELC_AD11（单元1）触发器启动。
4. 当A组的第一次扫描完成时，转换结果存储在相关的AD数据寄存器y（ADDRy）中；无论ADCSR中的ADIE位设置如何，都不会产生ADC12i_ADI中断请求。
5. A组的第二次扫描由第二个ELC_AD01（单元0）或ELC_AD11（单元1）触发器启动。

6. When the second scan of Group A completes, the conversion result is stored in ADDBLDR. An ADC12i_ADI interrupt is generated.

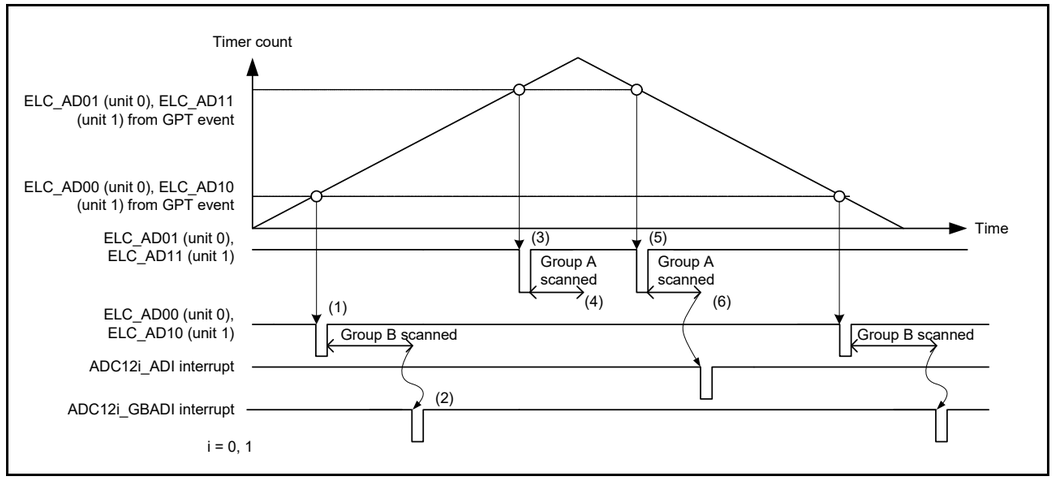


Figure 47.24 Example basic operation in group scan mode with double-trigger mode when synchronous triggers from the ELC are used

47.3.4.3 Operation with group A priority control

Setting the ADGSPCR.PGS bit to 1 in group scan mode makes operation proceed under Group A priority control. When setting the PGS bit in the ADGSPCR register to 1, follow the procedure shown in Figure 47.25. If the procedure is not followed, A/D conversion operation and stored data are not guaranteed.

In basic group scan mode, while A/D conversion is underway for group A or group B, input of the trigger for A/D conversion for the other group is ignored. Under Group A priority control, if a Group A trigger is input during A/D conversion for Group B, A/D conversion for Group B is discontinued and A/D conversion for Group A proceeds. If the setting in the ADGSPCR.GBRSCN bit is 0, the ADC12 enters wait state on completion of the A/D conversion for Group A. If the setting in the ADGSPCR.GBRSCN bit is 1, the ADC12 automatically restarts scanning for Group B from the head of the group after completion of the A/D conversion for Group A. Table 47.9 summarizes operations in response to the input of a trigger during A/D conversion with the settings in the ADGSPCR.GBRSCN bit.

Scan operations in Group A or Group B are the same in single scan mode. Additionally, single scanning continues to proceed if the ADGSPCR.GBRP bit is set to 1 during scanning operations for Group B.

For the trigger settings in group scan mode, select a synchronous trigger for Group A using the ADSTRGR.TRSA[5:0] bits, and select a synchronous trigger for Group B, different from that of Group A, using the ADSTRGR.TRSB[5:0] bits. Set the ADSTRGR.TRSB[5:0] bits to 3Fh when setting the ADGSPCR.GBRP bit to 1.

Additionally, as targets for A/D conversion, select channels for Group A using the ADANSA0 and ADANSA1 registers and the ADEXICR.TSSA and OCSA bits, and for Group B, select channels different from those for Group A using the ADANSB0 and ADANSB1 registers and the ADEXICR.TSSB and OCSB bits.

6. 当A组的第二次扫描完成时，转换结果存储在ADDBLDR中。产生一个ADC12i_ADI中断。

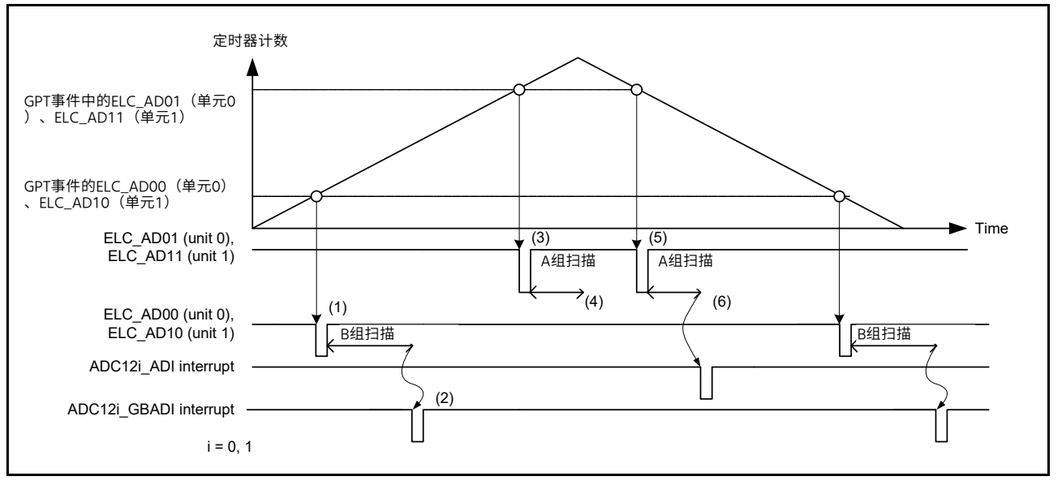


Figure 47.24 当使用来自ELC的同步触发时，具有双触发模式的组扫描模式下的基本操作示例

47.3.4.3 A组优先控制操作

在组扫描模式中将ADGSPCR.PGS位设置为1可使操作在A组优先级控制下进行。将ADGSPCR寄存器中的PGS位设置为1时，请按照图47.25中所示的步骤进行操作。如果不遵循该程序，则无法保证AD转换操作和存储数据。

在基本组扫描模式下，当A组或B组正在进行AD转换时，忽略其他组的AD转换触发输入。在A组优先控制下，如果在B组的AD转换期间输入A组触发，则停止B组的AD转换，继续A组的AD转换。如果ADGSPCR.GBRSCN位设置为0，ADC12在A组AD转换完成时进入等待状态。如果ADGSPCR.GBRSCN位设置为1，ADC12自动从头部重新开始扫描B组组A的AD转换完成后的组。表47.9总结了在ADGSPCR.GBRSCN位中设置的AD转换期间响应触发输入的操作。

A组或B组的扫描操作在单次扫描模式下是相同的。此外，如果在B组的扫描操作期间ADGSPCR.GBRP位设置为1，则单次扫描会继续进行。

对于组扫描模式下的触发设置，使用ADSTRGR.TRSA[5:0]位为A组选择一个同步触发，并使用ADSTRGR.TRSB[为B组选择一个与A组不同的同步触发5:0]位。将ADGSPCR.GBRP位设置为1时，将ADSTRGR.TRSB[5:0]位设置为3Fh。

此外，作为AD转换的目标，使用ADANSA0和ADANSA1寄存器以及ADEXICR.TSSA和OCSA位为A组选择通道，对于B组，使用ADANSB0和ADANSB1寄存器以及ADEXICR选择与A组不同的通道.TSSB和OCSB位。

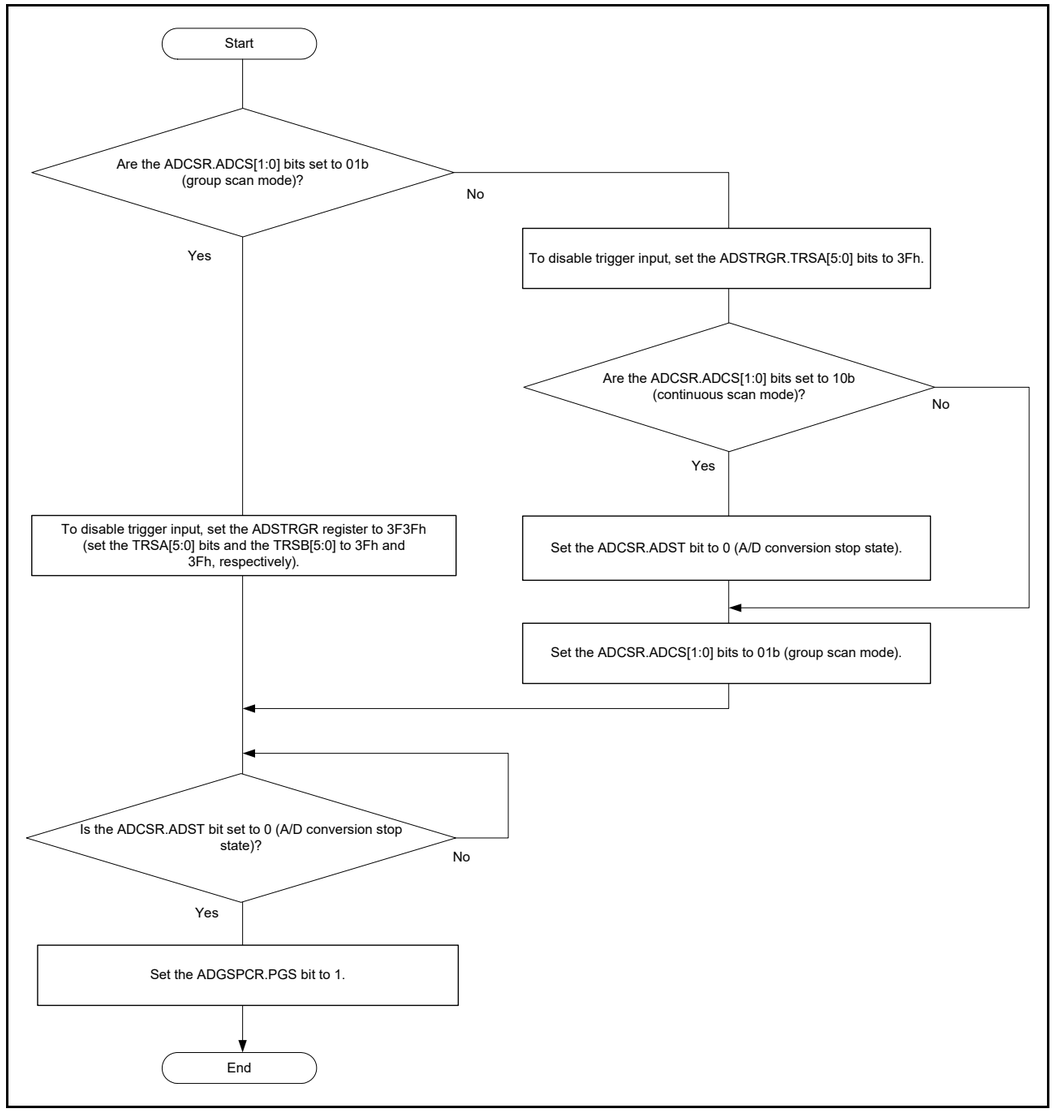


Figure 47.25 Flow for ADGSPCR.PGS bit setting

Table 47.9 Control of A/D conversion operations based on the ADGSPCR.GBRSCN bit settings

A/D conversion operation	Trigger input	ADGSPCR.GBRSCN = 0	ADGSPCR.GBRSCN = 1
When A/D conversion for Group A is in progress	Input of Group A trigger	Trigger input is invalid	Trigger input is invalid
	Input of Group B trigger	Trigger input is invalid	Group B is converted after Group A conversion completes
When A/D conversion for Group B is in progress	Input of Group A trigger	Group B conversion stops and Group A conversion starts	• Group B conversion stops and Group A conversion starts • Group B Conversion starts after Group A conversion completes
	Input of Group B trigger	Trigger input is invalid	Trigger input is invalid

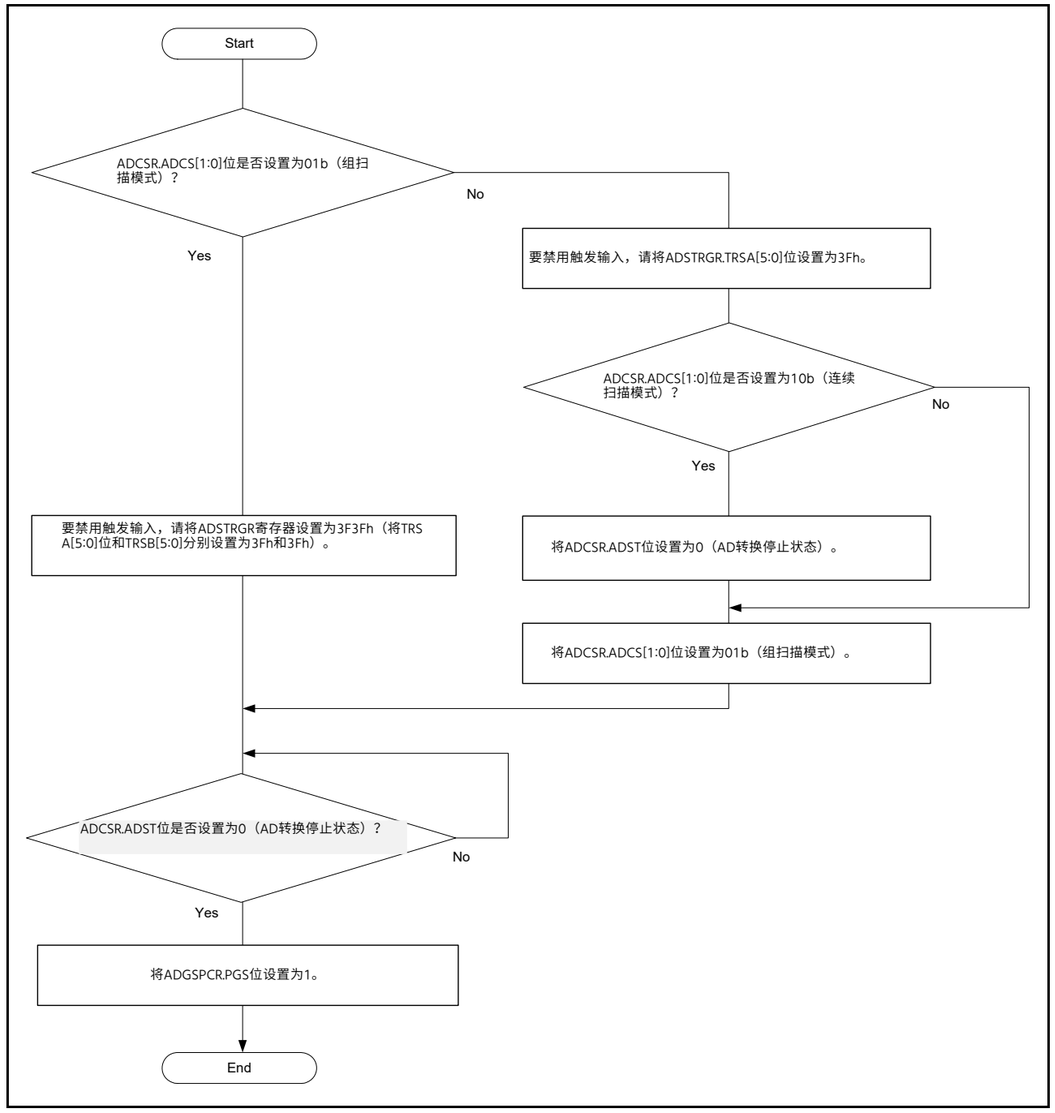


Figure 47.25 ADGSPCR.PGS位设置流程

Table 47.9 根据ADGSPCR.GBRSCN位设置控制AD转换操作

AD转换操作	触发输入	ADGSPCR.GBRSCN = 0	ADGSPCR.GBRSCN = 1
当AD转换为A组进行中	A组触发器输入	触发器输入无效	触发器输入无效
	B组触发输入	触发器输入无效	GroupB在Group之后转换一次转换完成
当AD转换为B组进行中	A组触发器输入	B组转换停止和A组转换开始	B组转换停止，A组转换开始 B组转换在A组转换完成后开始
	B组触发输入	触发器输入无效	触发器输入无效

The following describes the operations in group scan mode under Group A priority control (ADGSPCR.GBRSCN = 1 and ADGSPCR.GBRP = 0) when channel 0 is selected for Group A and channels 1 to 3 are selected for Group B.

The operation is as follows:

1. When input of a trigger for Group B sets the ADCSR.ADST bit to 1 (A/D conversion start), conversion for the ANn channels selected in the ADANSB0 and ADANSB1 registers starts in order from the channel with the smallest number n.
2. On completion of A/D conversion, the result is stored in the associated A/D Data Register y (ADDRy).
3. When a group A trigger is input while A/D conversion for group B is in progress, and A/D conversion for group B is discontinued with the ADCSR.ADST bit remains 1, A/D conversion for the ANn channels selected in the ADANSA0 and ADANSA1 registers starts in order from the channel with the smallest number n. If A/D conversion are not complete when conversion of group B is interrupted, A/D conversion result is not stored in the A/D Data Register (ADDRy).
4. On completion of A/D conversion on a single channel, the result is stored in the associated A/D Data Register y (ADDRy).
5. An ADC12i_ADI (i = 0, 1) interrupt request is generated (no register setting).
6. A/D conversion for the ANn channels in group B selected in the ADANSB0 and ADANSB1 registers restarts in order from the channel with the smallest number n with the ADCSR.ADST bit remains 1.
7. On completion of A/D conversion on a single channel, the result is stored in the associated A/D Data Register y (ADDRy).
8. An ADC12i_GBADI interrupt request is generated if the setting in the ADCSR.GBADIE bit is 1 (ADC12i_GBADI interrupt when Group B scanning completion is enabled).
9. The ADCSR.ADST bit is automatically cleared and ADC12 enters the wait state when A/D conversion completes.

下面介绍在A组优先级控制（ADGSPCR.GBRSCN=1和ADGSPCR.GBRP=0）下，当A组选择通道0，B组选择通道1到3时，组扫描模式下的操作。

操作如下：

1. 当B组的触发输入将ADCSR.ADST位设置为1（AD转换开始）时，ADANSB0和ADANSB1寄存器中选择的ANn通道的转换从编号n最小的通道开始按顺序开始。
2. 完成AD转换后，结果将存储在相关的AD数据寄存器y(ADDRy)中。
3. 如果在B组的AD转换正在进行时输入A组触发，并且B组的AD转换在ADCSR.ADST位保持为1的情况下中断，则在ADANSA0和ADANSA1寄存器中选择的ANn通道的AD转换按顺序开始从具有最小编号n的通道。如果B组转换中断时AD转换未完成，AD转换结果不会存储在AD数据寄存器(ADDRy)中。
4. 在单个通道上完成AD转换后，结果将存储在相关的AD数据寄存器y(ADDRy)中。
5. 产生一个ADC12i_ADI(i=0 1)中断请求（无寄存器设置）。
6. 在ADANSB0和ADANSB1寄存器中选择的B组ANn通道的AD转换从具有最小编号n的通道开始按顺序重新启动，ADCSR.ADST位保持为1。
7. 在单个通道上完成AD转换后，结果将存储在相关的AD数据寄存器y(ADDRy)中。
8. 如果ADCSR.GBADIE位的设置为1（启用B组扫描完成时的ADC12i_GBADI中断），则会产生ADC12i_GBADI中断请求。
9. 当AD转换完成时，ADCSR.ADST位自动清零，ADC12进入等待状态。

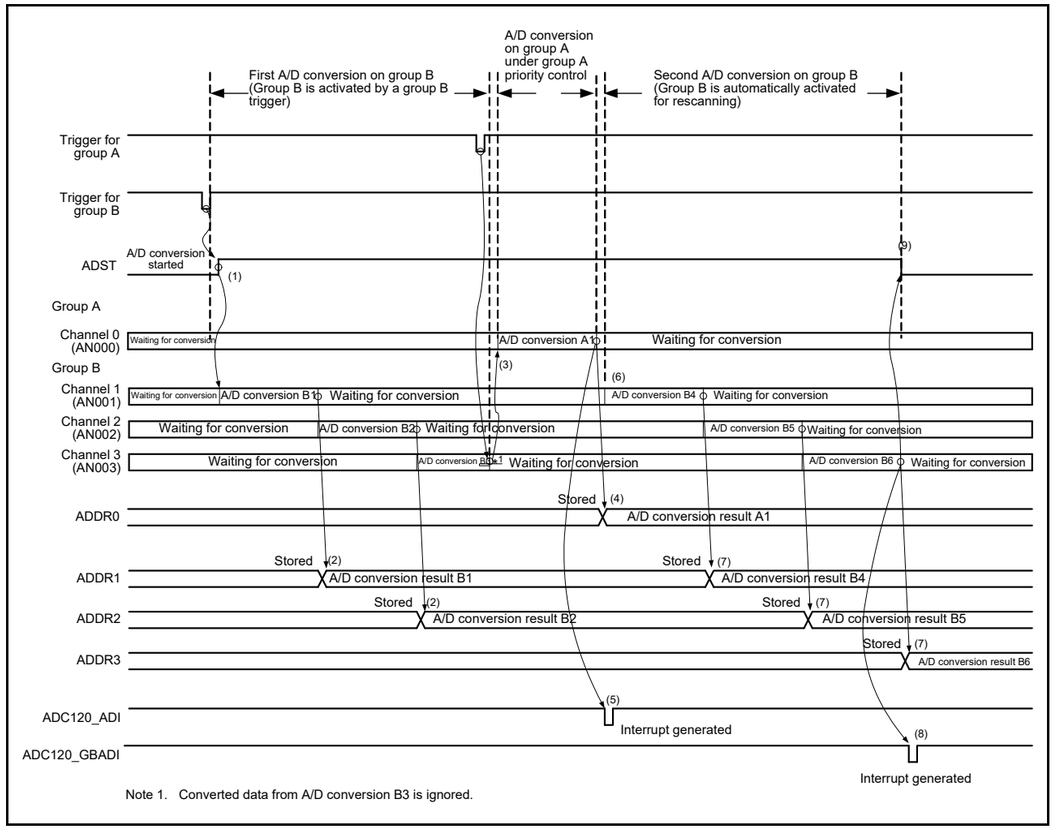


Figure 47.26 Example operation with Group A priority control (1), when ADGSPCR.GBRSCN = 1 and ADGSPCR.GBRP = 0

This section provides an example operation when a Group A trigger is input again during rescanning operation on Group B. In this example, channel 0 is selected for Group A and channels 1 to 3 are selected for Group B when operation on Group A is given priority (ADGSPCR.GBRSCN = 1 and ADGSPCR.GBRP = 0).

The operation is as follows:

1. When a Group B trigger input sets the ADCSR.ADST bit to 1 (A/D conversion start), conversion for the ANn channels in Group B selected in the ADANSB0 and ADANSB1 registers starts in order from the channel with the smallest number n.
2. On completion of A/D conversion on a single channel, the result is stored in the associated A/D Data Register y (ADDRy).
3. When a group A trigger is input while A/D conversion for group B is in progress, and A/D conversion for group B is discontinued with the ADCSR.ADST bit remains 1. If A/D conversion are not complete when the conversion of group B is interrupted, A/D conversion result is not stored in the A/D Data Register (ADDRy).
4. A/D conversion for the ANn Group A channels selected in the ADANSA0 and ADANSA1 registers starts in order from the channel with the smallest number n.
5. On completion of A/D conversion on a single channel, the result is stored in the associated A/D Data Register y (ADDRy).
6. An ADC12i_ADI (i = 0, 1) interrupt request is generated (no register setting).
7. If the ADGSPCR.GBRSCN bit is 1 when the A/D conversion of group A completes, the ADCSR.ADST bit remains

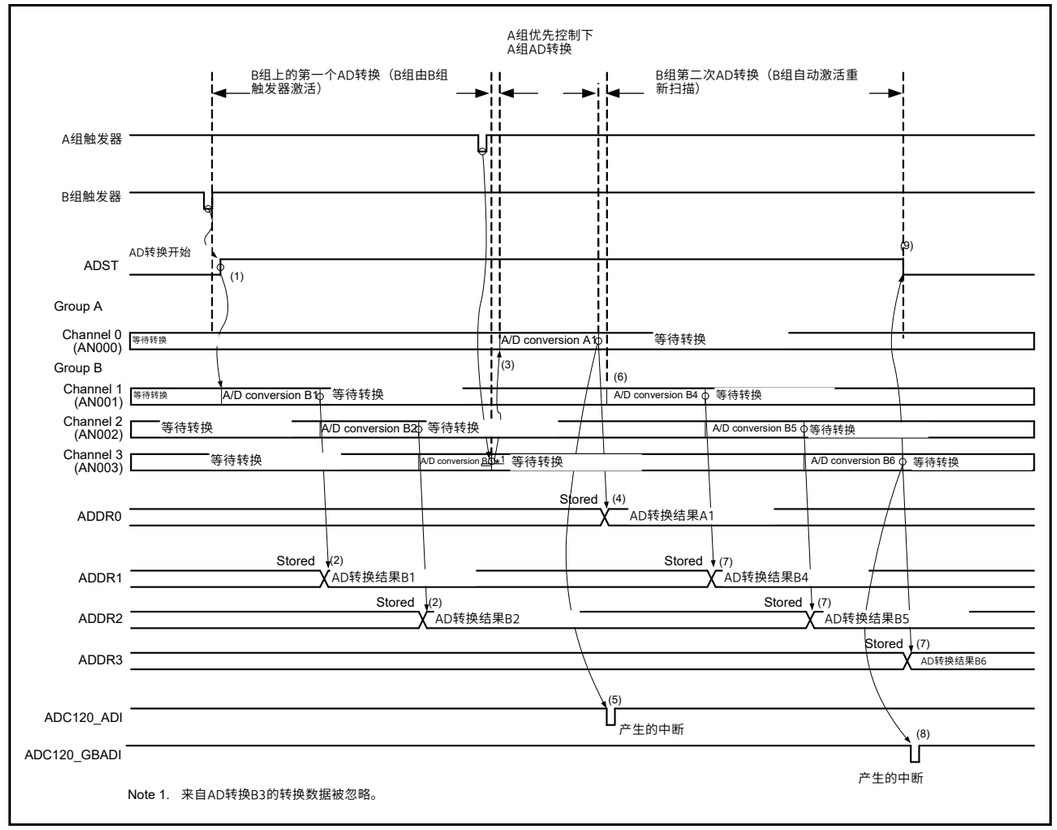


Figure 47.26 使用A组优先级控制(1)的示例操作，当ADGSPCR.GBRSCN=1并且ADGSPCR.GBRP = 0

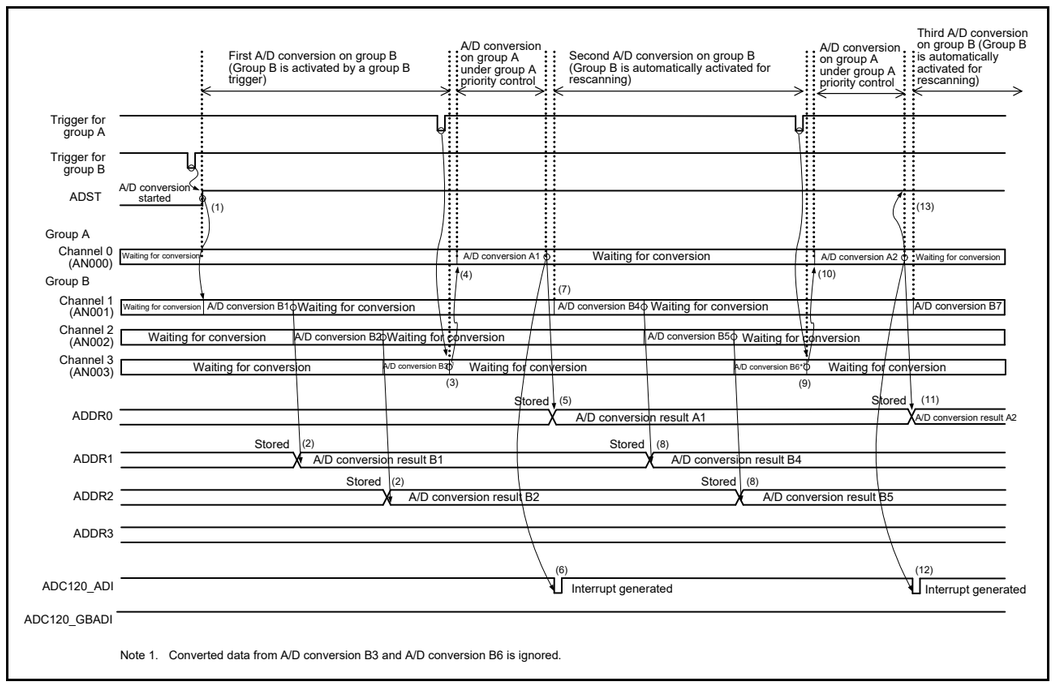
本节提供在对Group进行重新扫描操作期间再次输入GroupA触发器时的示例操作
B.在本例中，A组选择通道0，B组选择通道1到3。
A组具有优先权（ADGSPCR.GBRSCN=1和ADGSPCR.GBRP=0）。

操作如下：

1. 当B组触发输入将ADCSR.ADST位设置为1（AD转换开始）时，ADANSB0和ADANSB1寄存器中选择的B组ANn通道的转换从编号最小的通道开始按顺序开始。
2. 在单个通道上完成AD转换后，结果将存储在相关的AD数据寄存器y(ADDRy)中。
3. 当B组的AD转换正在进行时输入A组触发，并且B组的AD转换中断且ADCSR.ADST位保持1。如果B组的转换中断时AD转换未完成，则AD转换结果不存储在AD数据寄存器(ADDRy)中。
4. 在ADANSA0和ADANSA1寄存器中选择的ANn组A通道的D转换从编号n最小的通道开始。
5. 在单个通道上完成AD转换后，结果将存储在相关的AD数据寄存器y(ADDRy)中。
6. 产生一个ADC12i_ADI(i=0 1)中断请求（无寄存器设置）。
7. 如果A组AD转换完成时ADGSPCR.GBRSCN位为1，则ADCSR.ADST位保持不变

1 and group B is rescanned. A/D conversion for the ANn group B channels selected in the ADANSB0 and ADANSB1 registers starts again in order from the channel with the smallest number n.

8. On completion of A/D conversion on a single channel, the result is stored in the associated A/D Data Register y (ADDRy).
9. If a group A trigger is input during A/D conversion on group B for rescanning, the ADCSR.ADST bit remains 1 and the ongoing A/D conversion on group B is discontinued.
10. The ADCSR.ADST bit is set to 1 automatically, and A/D conversion for the ANn Group A channels selected in the ADANSA0 and ADANSA1 registers starts in order from the channel with the smallest number n.
11. On completion of A/D conversion on a single channel, the result is stored in the associated A/D Data Register y (ADDRy).
12. An ADC12i_ADI interrupt request is generated (no register setting).
13. If the ADGSPCR.GBRSCN bit is 1 when A/D conversion of group A are complete, the ADCSR.ADST bit remains 1 and group B is rescanned. A/D conversion for the ANn group B channels selected in the ADANSB0 and ADANSB1 registers starts again in order from the channel with the smallest number n.
14. If a Group A trigger is input during A/D conversion on Group B for rescanning, steps 9 to 13 are repeated. If a Group A trigger is not input, the ADCSR.ADST bit is cleared automatically on completion of A/D conversion on Group B and ADC12 enters a wait state.



Note 1. Converted data from A/D conversion B3 and A/D conversion B6 is ignored.

Figure 47.27 Example operation with Group A priority control (2), when ADGSPCR.GBRSCN = 1 and ADGSPCR.GBRP = 0

This section provides an example of a rescanning operation in which a Group B trigger is input during A/D conversion on Group A. In this example, channels 1 to 3 are selected for Group A and channel 0 is selected for Group B when operation on Group A is given priority (ADGSPCR.GBRSCN = 1, ADGSPCR.GBRP = 0).

The operation is as follows:

1. When input of a trigger for Group A sets the ADCSR.ADST bit to 1 (A/D conversion start), conversion for the ANn channels selected in the ADANSA0 and ADANSA1 registers starts in order from the channel with the smallest

1组B被重新扫描。ADANSB0和ADANSB1寄存器中选择的ANnB组通道的AD转换从编号n最小的通道重新开始。

8. 在单个通道上完成AD转换后，结果将存储在相关的AD数据寄存器y(ADDRy)中。
9. 如果在B组的AD转换期间输入A组触发以进行重新扫描，则ADCSR.ADST位保持为1，并且停止B组正在进行的AD转换。

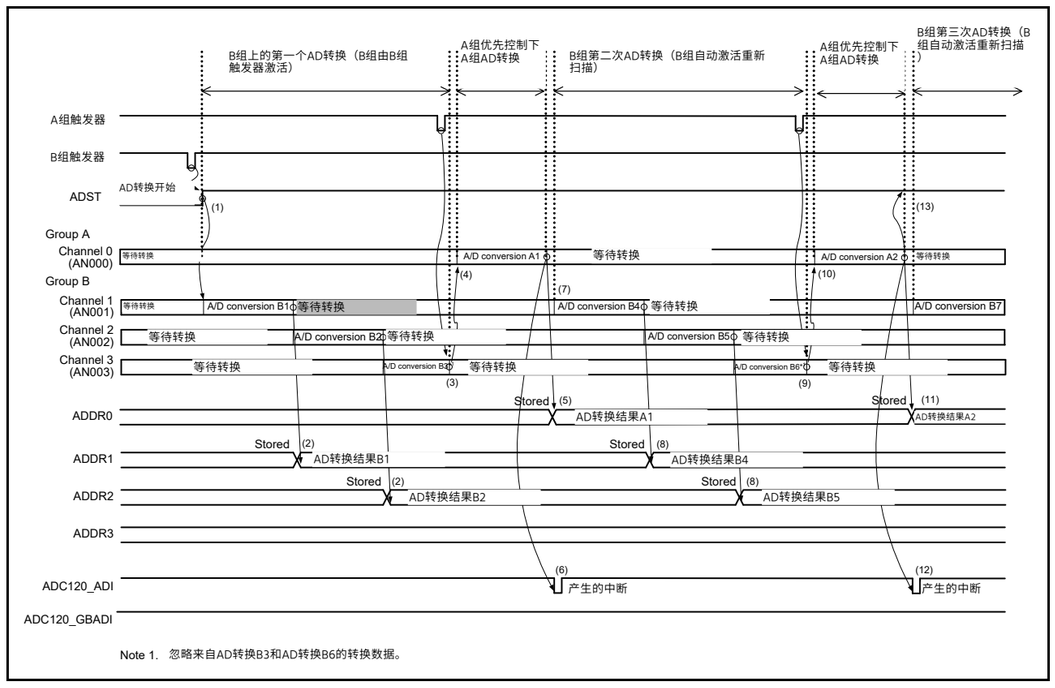
10.ADCSR.ADST位自动设置为1，在ADANSA0和ADANSA1寄存器中选择的ANn组A通道的AD转换从编号n最小的通道开始按顺序开始。

11.在单个通道上完成AD转换后，结果将存储在相关的AD数据寄存器y(ADDRy)中。

12.产生一个ADC12i_ADI中断请求（无寄存器设置）。

13.如果A组AD转换完成时ADGSPCR.GBRSCN位为1，则ADCSR.ADST位保持1并重新扫描B组。ADANSB0和ADANSB1寄存器中选择的ANnB组通道的AD转换从编号n最小的通道重新开始。

14.如果在B组的AD转换期间输入A组触发以进行重新扫描，则重复步骤9至13。如果一个未输入A组触发，ADCSR.ADST位在AD转换完成后自动清零
B组和ADC12进入等待状态。



Note 1. 忽略来自AD转换B3和AD转换B6的转换数据。

Figure 47.27 使用A组优先级控制(2)的示例操作，当ADGSPCR.GBRSCN=1并且ADGSPCR.GBRP = 0

本节提供了重新扫描操作的示例，其中在A组的AD转换期间输入B组触发。在此示例中，为A组选择通道1至3，在A组操作时为B组选择通道0被赋予优先级（ADGSPCR.GBRSCN=1，ADGSPCR.GBRP=0）。

操作如下：

1. 当A组的触发输入将ADCSR.ADST位设置为1（AD转换开始）时，在ADANSA0和ADANSA1寄存器中选择的ANn通道的转换按顺序从最小的通道开始

number n.

2. On completion of A/D conversion on a single channel, the result is stored in the associated A/D Data Register y (ADDRy).
3. If a Group B trigger is input during A/D conversion on Group A, A/D conversion on Group B can be performed after the A/D conversion on Group A completes. (However, if Group A triggers are input continuously, the scan operation on Group B is canceled by Group A and is not performed.)
4. On completion of the A/D conversion on Group A, an ADC12i_ADI (i = 0, 1) interrupt request is generated (no register setting).
5. On completion of group A conversion, the ADCSR.ADST bit remains 1 and group B is rescanned. Next, A/D conversion for the ANn channels of group B selected in the ADANSB0 and ADANSB1 registers starts in order from the channel with the smallest number n.
6. On completion of A/D conversion on a single channel, the result is stored in the associated A/D Data Register y (ADDRy).
7. On completion of the rescanning operation on Group B, an ADC12i_GBADI interrupt request is generated if the setting in the ADCSR.GBADIE bit is 1 (ADC12i_GBADI interrupt when scanning completion is enabled).
8. The ADCSR.ADST bit is automatically cleared and ADC12 enters the wait state when A/D conversion completes.

number n.

2. 在单个通道上完成AD转换后，结果将存储在相关的AD数据寄存器y(ADDRy)中。
3. 如果在A组AD转换期间输入B组触发，则可以在A组AD转换完成后执行B组AD转换。（但是，如果连续输入A组触发，则B组的扫描操作会被A组取消，不会执行。）
4. 完成A组的AD转换后，会产生一个ADC12i_ADI(i=0 1)中断请求（无寄存器设置）。
5. 完成A组转换后，ADCSR.ADST位保持为1，并重新扫描B组。接下来，ADANSB0和ADANSB1寄存器中选择的B组ANn通道的AD转换从编号n最小的通道开始按顺序开始。
6. 在单个通道上完成AD转换后，结果将存储在相关的AD数据寄存器y(ADDRy)中。
7. 完成B组的重新扫描操作后，如果ADCSR.GBADIE位中的设置为1（使能扫描完成时的ADC12i_GBADI中断），则会产生ADC12i_GBADI中断请求。
8. 当AD转换完成时，ADCSR.ADST位自动清零，ADC12进入等待状态。

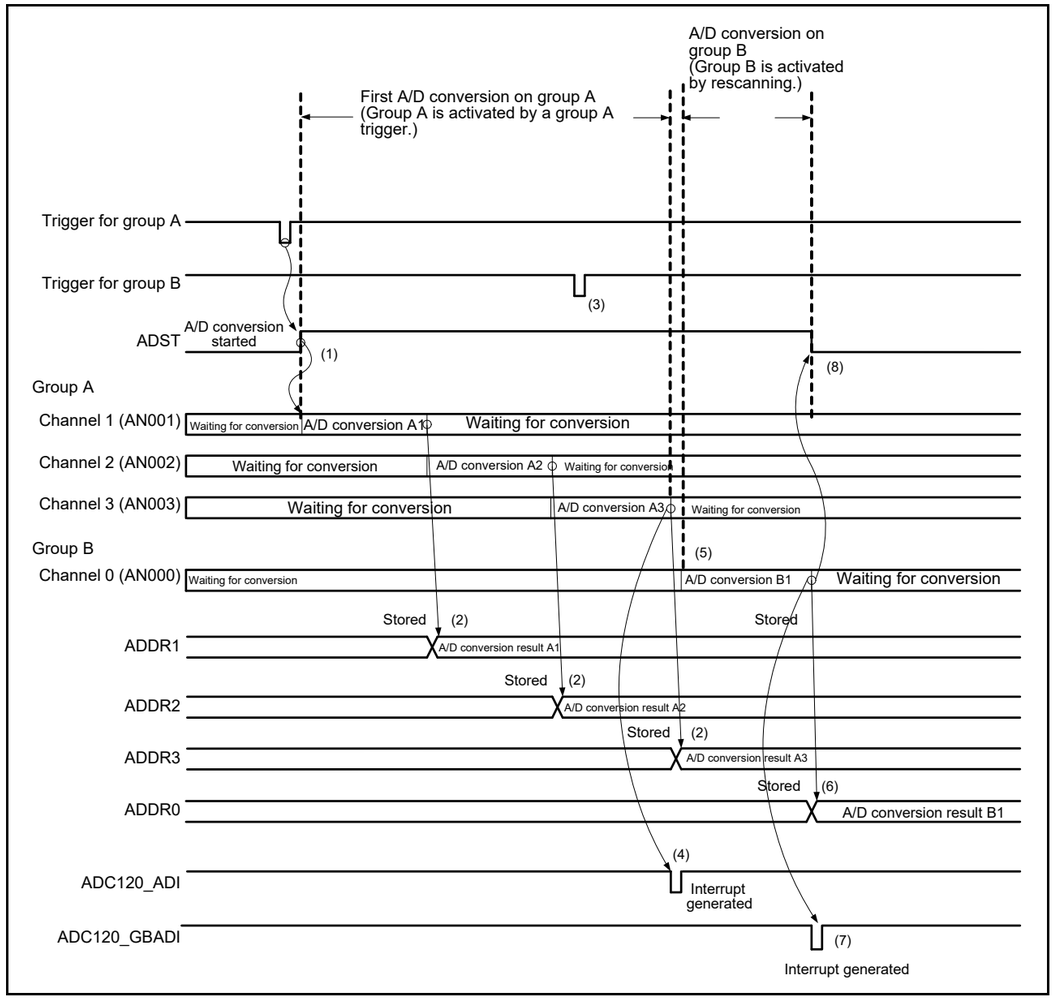


Figure 47.28 Example operation with Group A priority control (3), when ADGSPCR.GBRSCN = 1 and ADGSPCR.GBRP = 0

This section provides an example of operation under Group A priority control in which channel 0 is selected for Group A and channels 1 to 3 are selected for Group B (ADGSPCR.GBRSCN = 0, ADGSPCR.GBRP = 0).

The operation is as follows:

1. When input of a trigger for Group B sets the ADCSR.ADST bit to 1 (A/D conversion start), conversion for the ANn channels selected in the ADANSB0 and ADANSB1 registers starts in order from the channel with the smallest number n.
2. On completion of A/D conversion on a single channel, the result is stored in the associated A/D Data Register y (ADDRy).
3. If a group A trigger is input while A/D conversion for group B is in progress, and A/D conversion for group B is discontinued with the ADCSR.ADST bit remains 1. Next, A/D conversion for the ANn channels selected in the ADANSA0 and ADANSA1 registers starts in order from the channel with the smallest number n.
4. On completion of A/D conversion on a single channel, the result is stored in the associated A/D Data Register y (ADDRy).

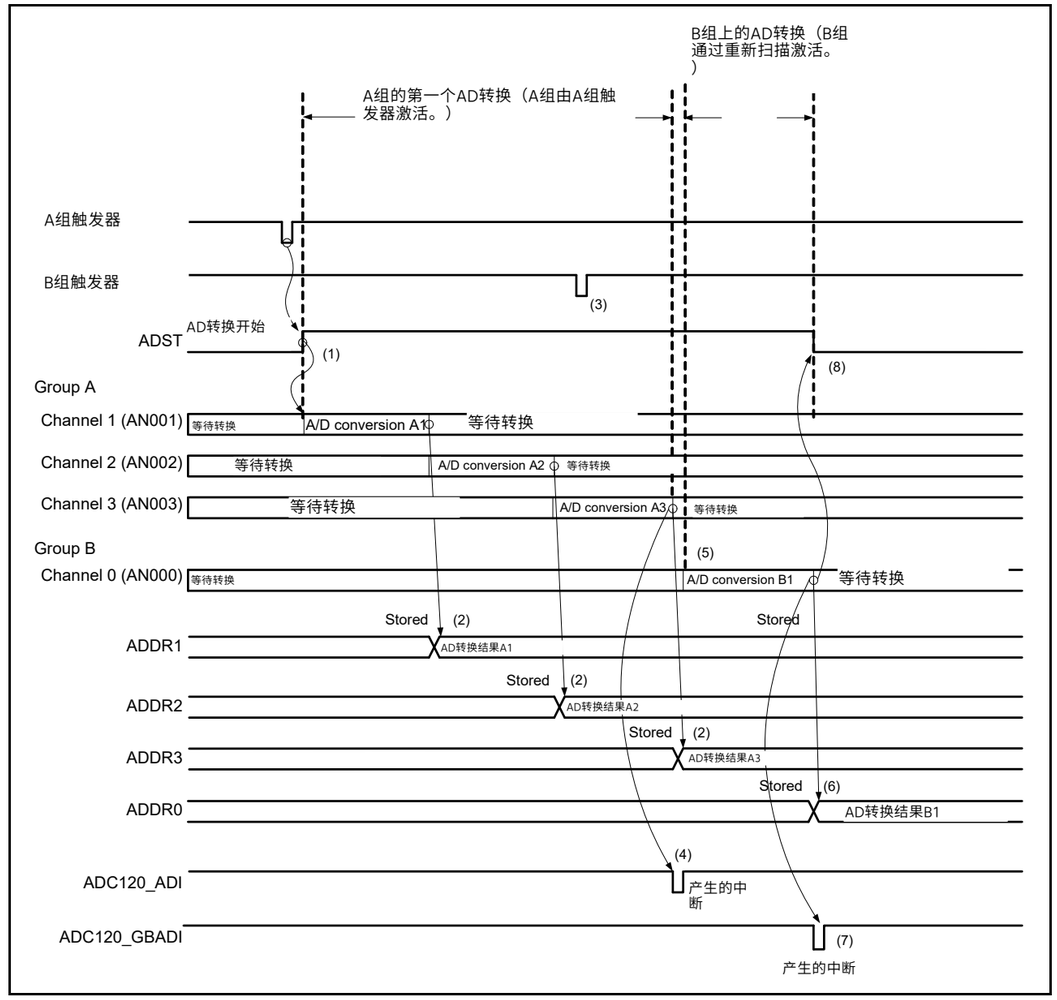


Figure 47.28 使用A组优先级控制(3)的示例操作，当ADGSPCR.GBRSCN=1并且ADGSPCR.GBRP = 0

本节提供了在A组优先级控制下的操作示例，其中为A组选择通道0，为B组选择通道1到3（ADGSPCR.GBRSCN=0，ADGSPCR.GBRP=0）。

操作如下：

1. 当B组的触发输入将ADCSR.ADST位设置为1（AD转换开始）时，ADANSB0和ADANSB1寄存器中选择的ANn通道的转换从编号n最小的通道开始按顺序开始。
2. 在单个通道上完成AD转换后，结果将存储在相关的AD数据寄存器y(ADDRy)中。
3. 如果在B组的AD转换正在进行时输入A组触发，并且B组的AD转换中断且ADCSR.ADST位保持为1。接下来，在ADANSA0和ADANSA1寄存器中选择的ANn通道的AD转换开始从编号n最小的通道开始。
4. 在单个通道上完成AD转换后，结果将存储在相关的AD数据寄存器y(ADDRy)中。

5. An ADC12i_ADI (i = 0, 1) interrupt request is generated (no register setting).
6. The ADCSR.ADST bit is automatically cleared and ADC12 enters the wait state when A/D conversion completes.

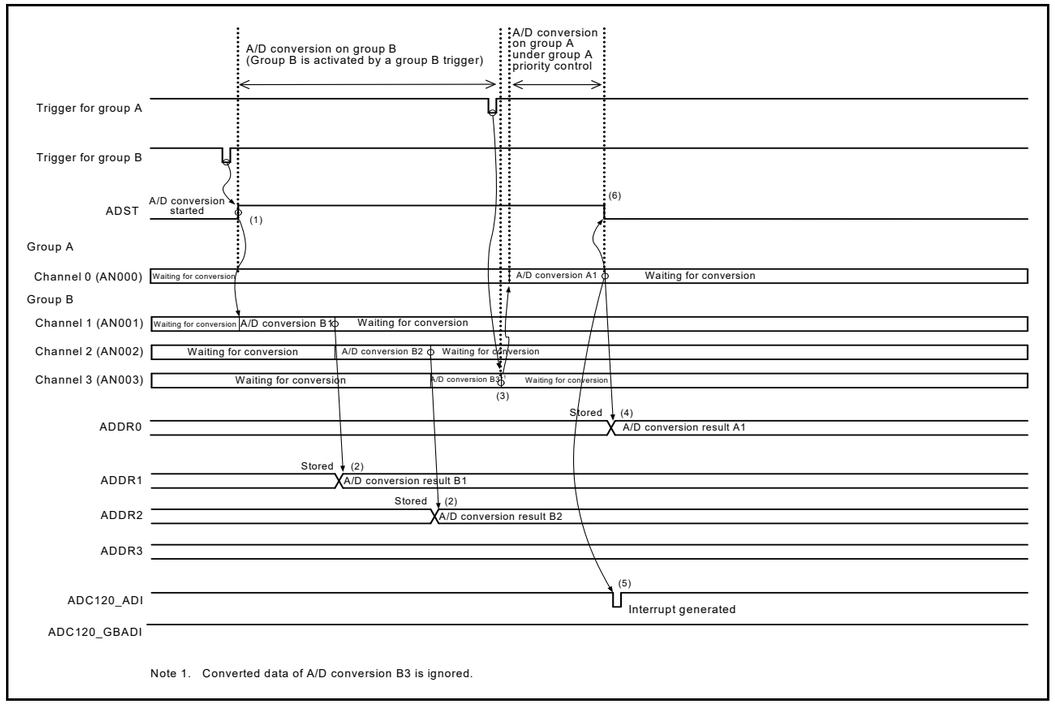


Figure 47.29 Example operation with Group A priority control (4), when ADGSPCR.GBRSCN = 0 and ADGSPCR.GBRP = 0

This section provides an example of operation under Group A priority control in which channel 0 is selected for Group A and channels 1 to 3 are selected for Group B (ADGSPCR.GBRP = 1).

The operation is as follows:

1. The ADCSR.ADST bit is set to 1 (A/D conversion start) when ADGSPCR.GBRP is set to 1, and conversion for the ANn channels selected in the ADANSB0 and ADANSB1 registers starts in order from the channel with the smallest number n.
2. On completion of A/D conversion on a single channel, the result is stored in the associated A/D Data Register y (ADDRy).
3. If a group A trigger is input while A/D conversion for group B is in progress, and A/D conversion for group B is discontinued with the ADCSR.ADST bit remains 1. Next, A/D conversion for the ANn channels selected in the ADANSA0 and ADANSA1 registers starts in order from the channel with the smallest number n.
4. On completion of A/D conversion on a single channel, the result is stored in the associated A/D Data Register y (ADDRy).
5. An ADC12i_ADI (i = 0, 1) interrupt request is generated (no register setting).
6. A/D conversion for the ANn channels in group B selected in the ADANSB0 and ADANSB1 registers restarts in order from the channel with the smallest number n and with the ADCSR.ADST bit remains 1.
7. On completion of A/D conversion on a single channel, the result is stored in the associated A/D Data Register y (ADDRy).
8. An ADC12i_GBADI interrupt request is generated if the setting in the ADCSR.GBADIE bit is 1.

5. 产生一个ADC12i_ADI(i=0 1)中断请求（无寄存器设置）。
6. 当AD转换完成时，ADCSR.ADST位自动清零，ADC12进入等待状态。

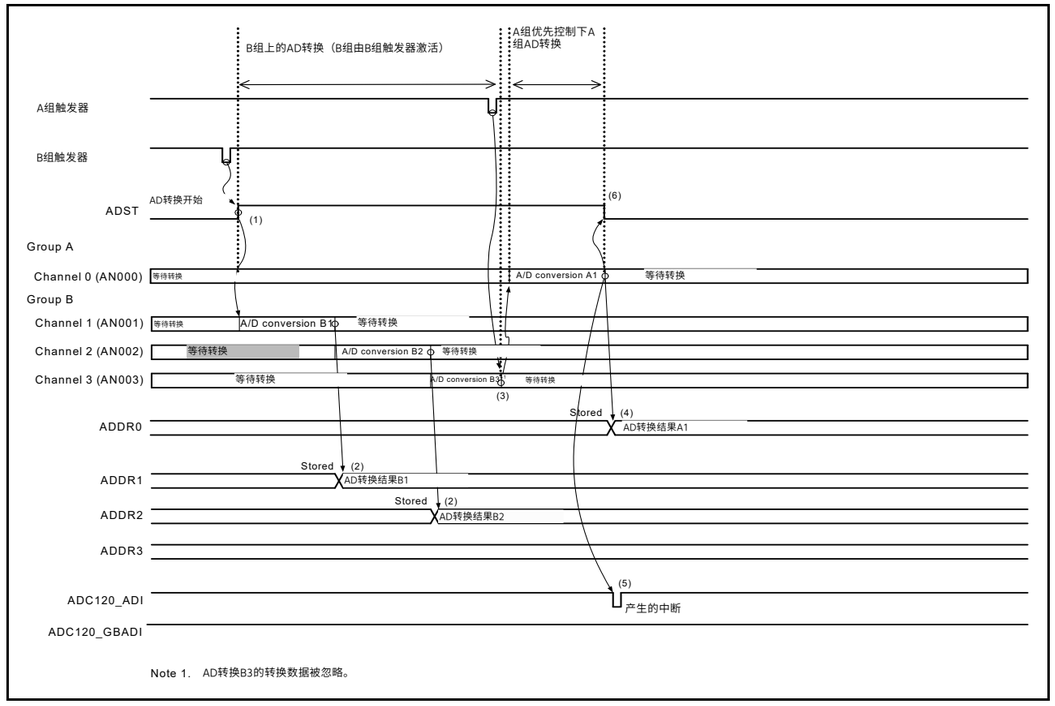


Figure 47.29 使用A组优先级控制(4)的示例操作，当ADGSPCR.GBRSCN=0并且ADGSPCR.GBRP = 0

本节提供A组优先级控制下的操作示例，其中为A组选择通道0，为B组选择通道1至3(ADGSPCR.GBRP=1)。

操作如下：

1. 当ADGSPCR.GBRP设置为1时，ADCSR.ADST位设置为1（AD转换开始），并且ADANSB0和ADANSB1寄存器中选择的ANn通道的转换从编号最小的通道开始按顺序开始。
2. 在单个通道上完成AD转换后，结果将存储在相关的AD数据寄存器y(ADDRy)中。
3. 如果在B组的AD转换正在进行时输入A组触发，并且B组的AD转换中断且ADCSR.ADST位保持为1。接下来，在ADANSA0和ADANSA1寄存器中选择的ANn通道的AD转换开始从编号n最小的通道开始。
4. 在单个通道上完成AD转换后，结果将存储在相关的AD数据寄存器y(ADDRy)中。
5. 产生一个ADC12i_ADI(i=0 1)中断请求（无寄存器设置）。
6. ADANSB0和ADANSB1寄存器中选择的B组ANn通道的AD转换从编号n最小且ADCSR.ADST位保持为1的通道重新开始。
7. 在单个通道上完成AD转换后，结果将存储在相关的AD数据寄存器y(ADDRy)中。
8. 如果ADCSR.GBADIE位中的设置为1，则会产生ADC12i_GBADI中断请求。

9. A/D conversion for the ANn channels selected in the ADANSB0 and ADANSB1 registers starts in order from the channel with the smallest number n. Steps 6 to 9 are repeated as long as the ADGSPCR.GBRP bit remains 1. Clearing of the ADCSR.ADST bit to 0 is prohibited while the ADGSPCR.GBRP bit is set to 1. Follow the procedure for clearing the ADCSR.ADST bit operation by software, shown in Figure 47.40, to force A/D conversion to stop while ADGSPCR.GBRP = 1.

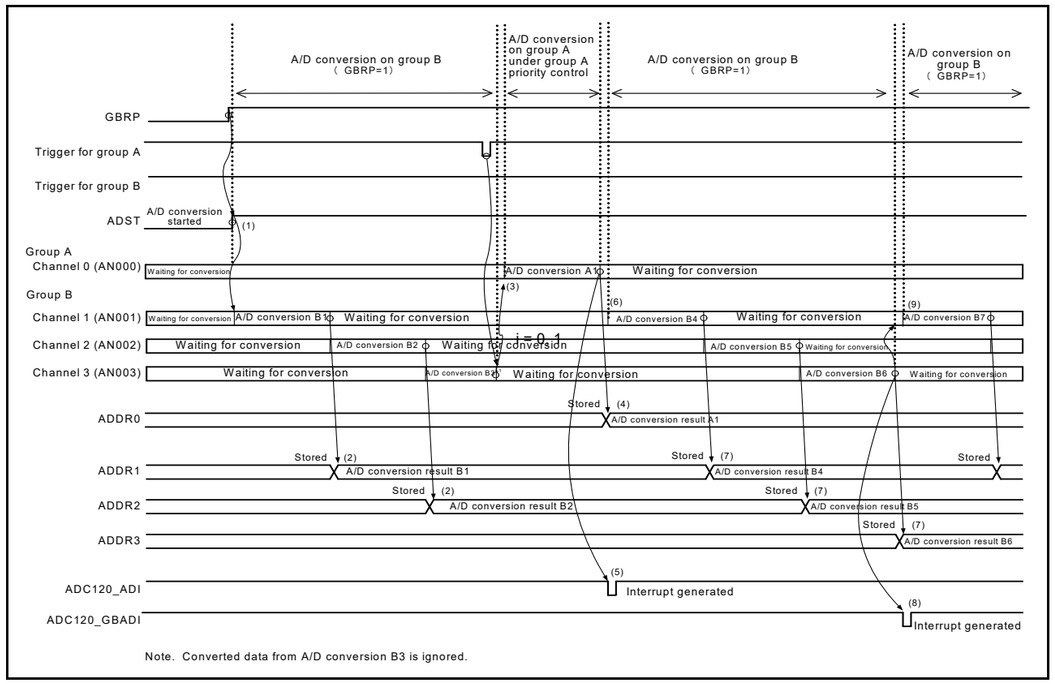


Figure 47.30 Example operation with Group A priority control (5), when ADGSPCR.GBRP = 1

47.3.5 Compare Function for Windows A and B

47.3.5.1 Compare function windows A and B

The compare function compares a reference value with the A/D conversion result. The reference value can be set for Window A and Window B independently. When the compare function is in use, the self-diagnosis function and double-trigger mode cannot be used. The main differences between Window A and Window B are their different interrupt output signals and the constraint on Window B of only one selectable channel.

This section provides an example operation that combines continuous scan mode and the compare function.

The operation is as follows:

1. When the ADCSR.ADST bit is set to 1 (A/D conversion start) by software, a synchronous trigger (ELC) or an asynchronous trigger, A/D conversion starts for the selected channels, temperature sensor, and internal reference voltage.
2. On completion of A/D conversion, the A/D conversion result is stored in the associated A/D Data Register y (ADDRy, ADTSDR, or ADOCDR). When ADCMPCR.CMPAE = 1, if bits in the ADCMPANSRy register or the ADCMPANSER register are set for Window A, the A/D conversion result is compared with the set ADCMPDR0/1 register value. When ADCMPCR.CMPBE = 1, if bits in the ADCMPBNSR register are set for Window B, the A/D conversion result is compared with the ADWINULB/ADWINLLB register setting.
3. As a result of the comparison, when Window A meets the condition set in ADCMPLR0/1 or ADCMPLER, the Compare Window A Flag (ADCMPSR0.CMPSTCHA0n, ADCMPSR1.CMPSTCHA1n, ADCMPSER.CMPSTTSA, or ADCMPSER.CMPSTOCA) sets 1. At this time, if the ADCMPCR.CMPAIE bit is 1,

9. ADANSB0和ADANSB1寄存器中选择的ANn通道的D转换从编号n最小的通道开始按顺序开始。只要ADGSPCR.GBRP位保持为1，就重复步骤6到9。当ADGSPCR.GBRP位设置为1时，禁止将ADCSR.ADST位清除为0。按照清除ADCSR.ADST位操作的程序进行通过软件，如图47.40所示，在ADGSPCR.GBRP=1时强制停止AD转换。

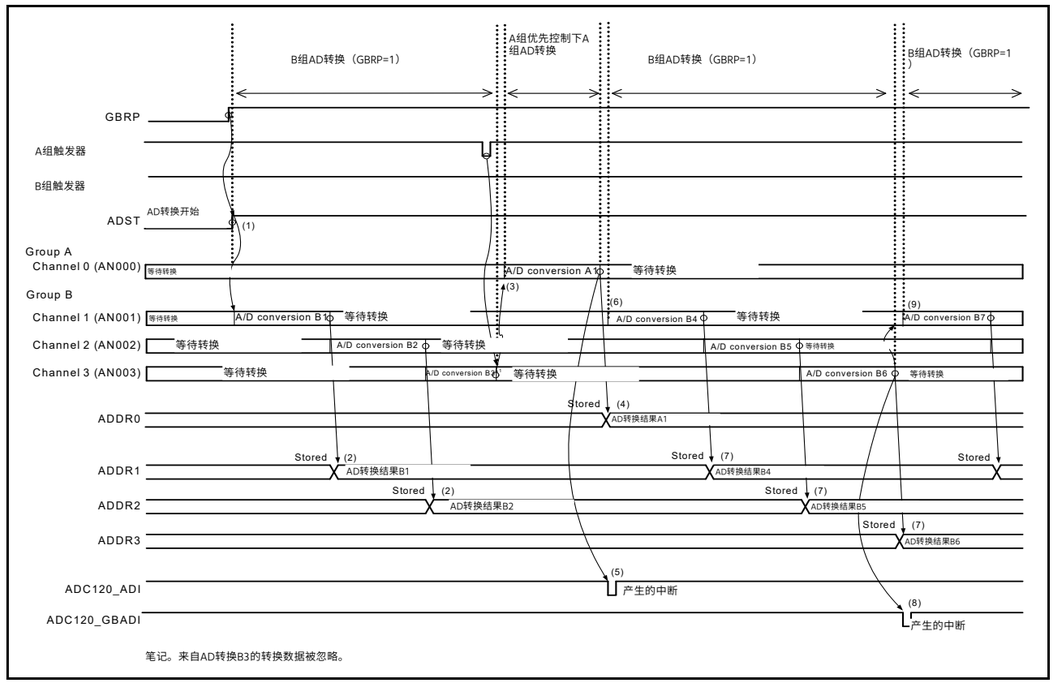


Figure 47.30 当ADGSPCR.GBRP=1时，A组优先级控制(5)的示例操作

47.3.5 比较WindowsA和B的函数

47.3.5.1 比较功能窗口A和B

比较功能将参考值与AD转换结果进行比较。参考值可设置为
窗口A和窗口B独立。使用比较功能时，不能使用自诊断功能和双触发模式。WindowA和WindowB的主要区别在于它们的中断输出信号不同以及WindowB只能选择一个通道的限制。

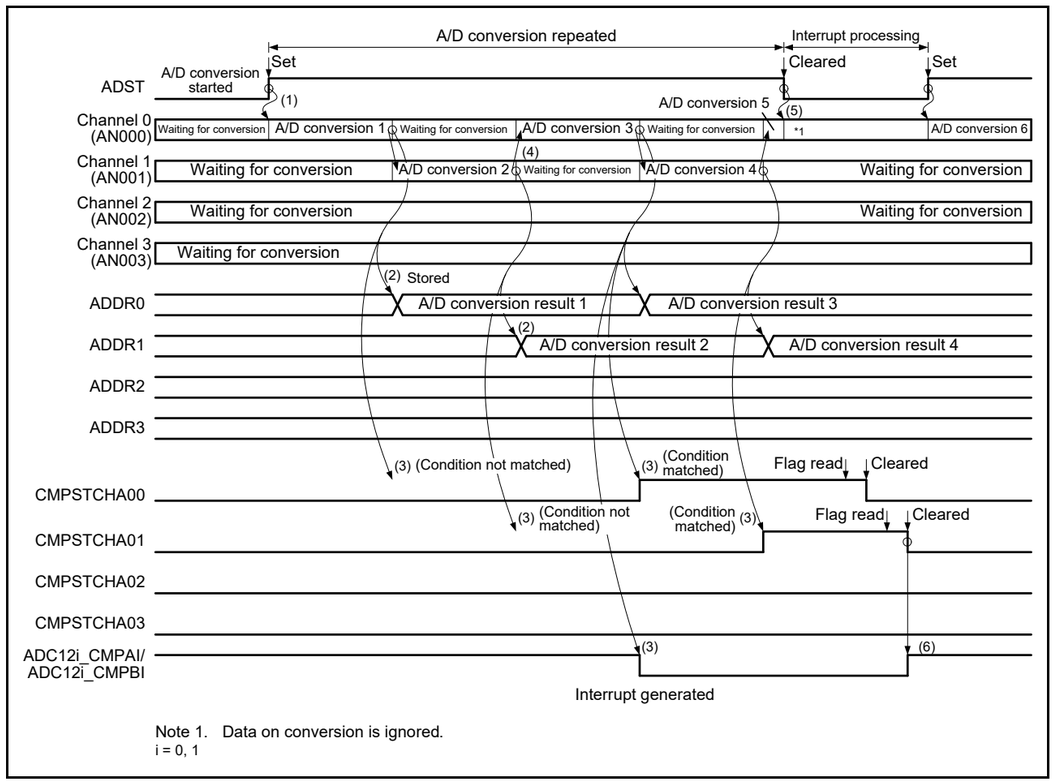
本节提供结合连续扫描模式和比较功能的示例操作。

操作如下：

1. 当ADCSR.ADST位通过软件、同步触发(ELC)或异步触发设置为1（AD转换开始）时，所选通道、温度传感器和内部参考电压的AD转换开始。
2. 完成AD转换后，AD转换结果存储在相关的AD数据寄存器y（ADDRy、ADTSDR或ADOCDR）中。当ADCMPCR.CMPAE=1时，如果ADCMPANSRy寄存器或ADCMPANSER寄存器中的位为窗口A设置，则AD转换结果将与设置的ADCMPDR01寄存器值进行比较。当ADCMPCR.CMPBE=1时，如果ADCMPBNSR寄存器中的位为窗口B设置，则将AD转换结果与ADWINULBADWINLLB寄存器设置进行比较。
3. 作为比较的结果，当窗口A满足ADCMPLR01或ADCMPLER中设置的条件时，比较窗口A标志（ADCMPSR0.CMPSTCHA0n、ADCMPSR1.CMPSTCHA1n、ADCMPSER.CMPSTTSA，或ADCMPSER.CMPSTOCA)设置为1。此时，如果ADCMPCR.CMPAIE位为1，

an ADC12i_CMPAI (i = 0, 1) interrupt request is generated. In the same way, when Window B meets the condition set in ADCMPBNSR.CMPLB, the Compare Window B Flag (ADCMPBSR.CMPSTB) sets to 1. At this time, if the ADCMPCR.CMPBIE bit is 1, an ADC12i_CMPBI interrupt request is generated.

4. On completion of all selected A/D conversions and comparisons, scan restarts.
5. After the ADC12i_CMPAI and ADC12i_CMPBI interrupts are accepted, the ADCSR.ADST bit is set to 0 (A/D conversion stop) and processing is performed for channels for which the compare flag is set to 1.
6. When all compare flags of Window A are cleared, the ADC12i_CMPAI interrupt request is canceled. In the same way, when all compare flags of Window B are cleared, the ADC12i_CMPBI interrupt request is reset. To perform comparison again, restart the A/D conversion.



Note 1. Data on conversion is ignored.
i = 0, 1

Figure 47.31 Example of compare function operation, when AN000 to AN003 are compared

47.3.5.2 Event output of compare function

The event output of compare function specifies the upper reference voltage value for Window A and the lower reference voltage value for Window B, compares the A/D-converted value of the selected channel with the upper and lower reference voltage values, and then outputs the ADC12i_WCMPM and ADC12i_WCMPUM (i = 0, 1) events based on the event conditions (A OR B, A AND B, A XOR B) and comparison results of Window A and Window B.

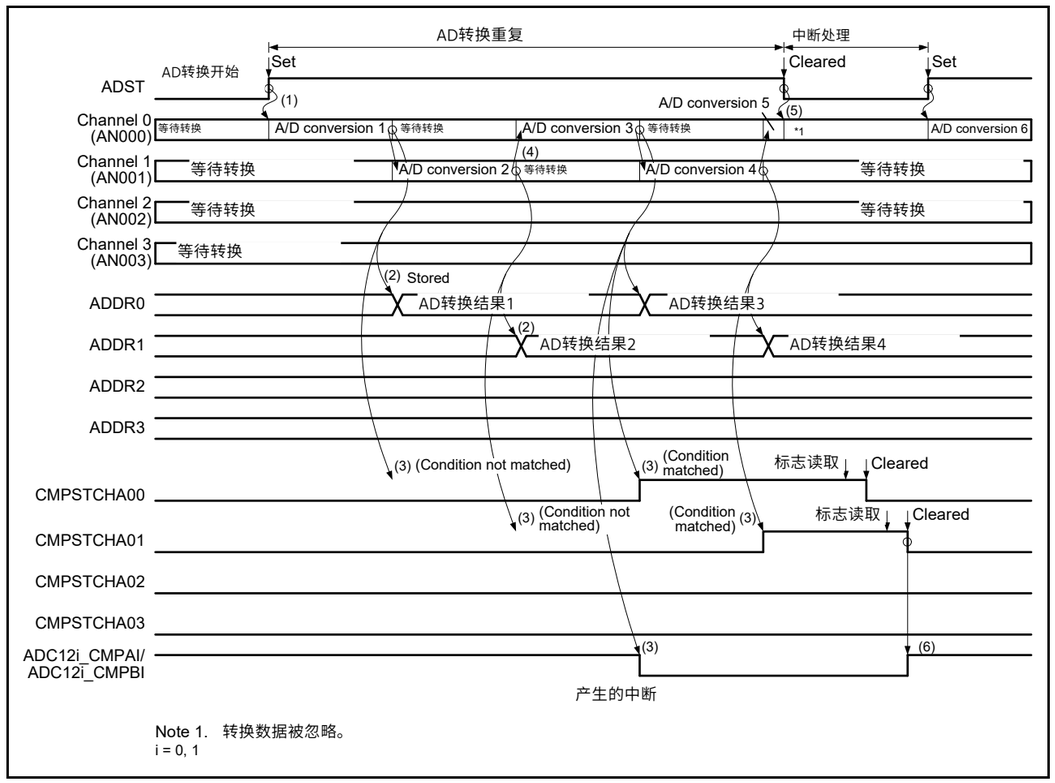
If more than one channel is selected for Window A, and even one channel in Window A meets the comparison condition, the comparison result of Window A becomes met. When using this function, perform A/D conversion in single scan mode. Any channels from AN000 to AN007 and AN016 to AN020 (unit 0), and AN100 to AN103, AN105 to AN107, and AN116 to AN119 (unit 1), internal reference voltage, and temperature sensor output are selectable for Window A.

This section provides the setting procedure and example when using event output of compare function.

To set up event output for the compare function:

产生一个ADC12i_CMPAI(i=0 1)中断请求。同理，当窗口B满足ADCMPBNSR.CMPLB中设置的条件时，比较窗口B标志（ADCMPBSR.CMPSTB）置1。此时如果ADCMPCR.CMPBIE位为1，则产生ADC12i_CMPBI中断请求.

4. 完成所有选定的AD转换和比较后，扫描重新开始。
5. 接受ADC12i_CMPAI和ADC12i_CMPBI中断后，ADCSR.ADST位设置为0（AD转换停止），并对比较标志设置为1的通道执行处理。
6. 当窗口A的所有比较标志被清除时，ADC12i_CMPAI中断请求被取消。同理，当窗口B的所有比较标志都被清除时，ADC12i_CMPBI中断请求被复位。要再次进行比较，请重新开始AD转换。



Note 1. 转换数据被忽略。
i = 0, 1

Figure 47.31 比较功能操作示例，当比较AN000和AN003时

47.3.5.2 比较函数的事件输出

比较函数的事件输出指定窗口A的参考电压上限和窗口B的参考电压下限，将所选通道的AD转换值与上下参考电压值进行比较，然后输出ADC12i_WCMPM和ADC12i_WCMPUM(i=0 1)事件基于事件条件（AORB、AANDB、AXORB）和窗口A和窗口B的比较结果。

如果窗口A选择了多个通道，即使窗口A中的一个通道满足比较条件，窗口A的比较结果也成立。使用此功能时，请在单次扫描模式下进行AD转换。窗口A可选择从AN000到AN007和AN016到AN020（单元0）、AN100到AN103、AN105到AN107和AN116到AN119（单元1）的任何通道、内部参考电压和温度传感器输出。

本节提供使用比较功能的事件输出时的设置步骤和示例。

要为比较功能设置事件输出：

1. Confirm that the value in the ADCSR.ADCS bits is 00b (single scan mode).
2. Select the channel for Window A in ADCMPANSR0/1 and ADCMPANSER. Set window comparison conditions in the ADCMPLR0/1 and ADCMPLER registers. Set the upper and lower reference values in the ADCMPDR0 and 1 registers.
3. Select the channel and comparison conditions for Window B in the ADCMPBNSR register, and set the upper and lower reference values in the ADWINULB and ADWINLLB registers.
4. Set composite conditions for Window A/B, Window A/B operation enable, and interrupt output enable in ADCMPCR.

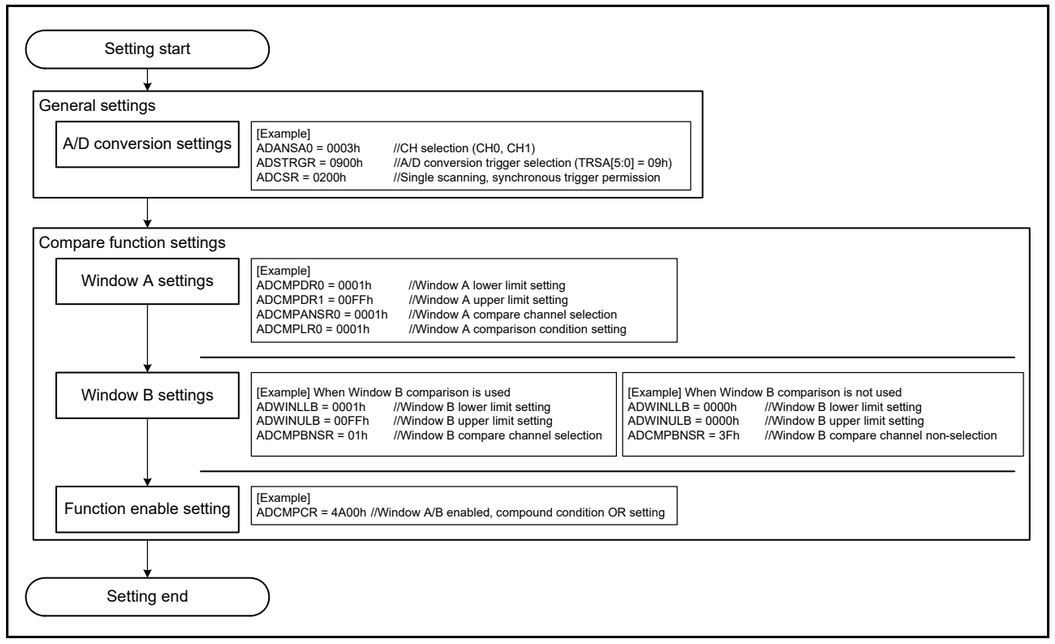


Figure 47.32 Setting example when using the event output of the compare function

Notes on the event output usage when using only the Window A for compare function:

- Enable both Window A and Window B (ADCMPCR.CMPAE = 1, ADCMPCR.CMPBE = 1)
- Set the compound condition of Window A and Window B to “OR condition” (ADCMPCR.CMPAB[1:0] = 00b)
- Set the compared channel of Window B to “Do not select” (ADCMPBNSR.CMPCHB[5:0] = 111111b)
- Set the compare condition of Window B to “0 < results < 0 always means mismatch”. (ADCMPCR.WCMPE = 1, ADWINLLB.CMPLLB[15:0] = ADWINULB.CMPULB[15:0] = 0000h, and ADCMPBNSR.CMPLB = 1)

Figure 47.33 shows the event output operation example of compare function.

A scan end event (ADC12i_ADI) is output with the same timing of one time single scan completion. A match or mismatch event (ADC12i_WCMPM or ADC12i_WCMPUM) is output delayed 1 PCLKB depending on ADCMPCR.CMPAB[1:0] settings.

Note: The match and mismatch events are exclusive, so both events are never output simultaneously.

1. 确认ADCSR.ADCS位中的值为00b（单次扫描模式）。
2. 在ADCMPANSR01和ADCMPANSER中选择窗口A的通道。在ADCMPLR01和ADCMPLER寄存器中设置窗口比较条件。在ADCMPDR0和1寄存器中设置参考值上限和下限。
3. 在ADCMPBNSR寄存器中选择窗口B的通道和比较条件，并在ADWINULB和ADWINLLB寄存器中设置上下参考值。
4. 设置窗口AB、窗口AB操作使能和中断输出使能的复合条件
ADCMPCR.

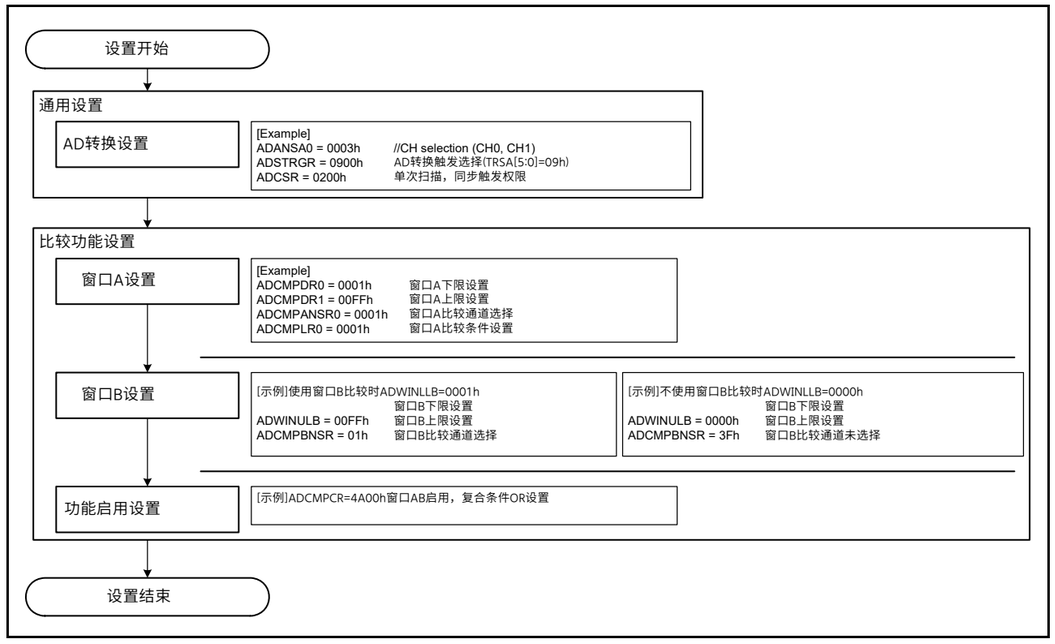


Figure 47.32 使用比较功能的事件输出时的设置示例

仅使用窗口A进行比较功能时的事件输出使用注意事项：

- 启用窗口A和窗口B(ADCMPCR.CMPAE=1 ADCMPCR.CMPBE=1）
- 将窗口A和窗口B的复合条件设置为“或条件”（ADCMPCR.CMPAB[1:0]=00b）
- 将窗口B的比较通道设置为“不选择”（ADCMPBNSR.CMPCHB[5:0]=111111b）
- 将窗口B的比较条件设置为“0<结果<0始终表示不匹配”。（ADCMPCR.WCMPE=1，ADWINLLB.CMPLLB[15:0] = ADWINULB.CMPULB[15:0] = 0000h, and ADCMPBNSR.CMPLB = 1)

图47.33显示了比较功能的事件输出操作示例。

扫描结束事件(ADC12i_ADI)以与一次单次扫描完成相同的时序输出。匹配或不匹配事件（ADC12i_WCMPM或ADC12i_WCMPUM）输出延迟1PCLKB，具体取决于ADCMPCR.CMPAB[1:0]设置。

Note: match和mismatch事件是互斥的，因此这两个事件永远不会同时输出。

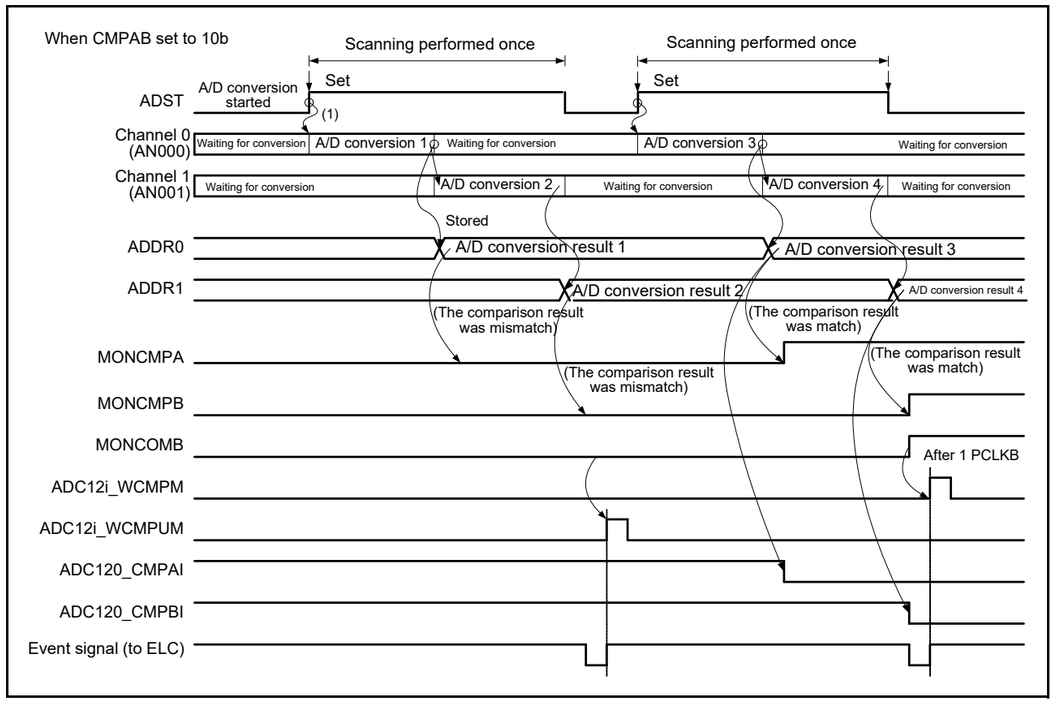


Figure 47.33 Example operation of the compare function event output, when AN000 to AN001 are compared

Note 1. Event output of compare function outputs match/mismatch from the comparison results of Window A and Window B, based on the ADCMPCR.CMPAB[1:0] settings.

Note 2. The comparison result of Window A is the logical addition of the comparison results of the comparison target channels of Window A. The comparison results of Window A and Window B are updated by each A/D conversion, and are kept even when single scan ends. Set ADCMPCR.CMPAE and ADCMPCR.CMPBE to 0 to clear the comparison results to 0.

47.3.5.3 Constraints on the compare function

The following constraints apply for the compare function:

- The compare function cannot be used together with the self-diagnosis function or double-trigger mode. (The compare function is not available for ADRD, ADDBLDR, ADDBLDRA, and ADDBLDRB.)
- Specify single scan mode when using match/mismatch event outputs.
- When the temperature sensor output or internal reference voltage is selected for Window A, Window B operations are disabled.
- When the temperature sensor output or internal reference voltage is selected for Window B, Window A operations are disabled.
- Setting the same channel for Window A and Window B is prohibited.
- Set the reference voltage values so that the high-potential reference voltage value is equal to or larger than the low-potential reference voltage value.

47.3.6 Analog Input Sampling and Scan Conversion Time

Scan conversion can be activated by a software trigger, a synchronous trigger (ELC), or an asynchronous trigger (ADTRGn). After the start-of-scanning-delay (t_D) elapses, processing by the channel-dedicated sample-and-hold circuits, processing for disconnection detection assistance, and processing of conversion for self-diagnosis all proceed,

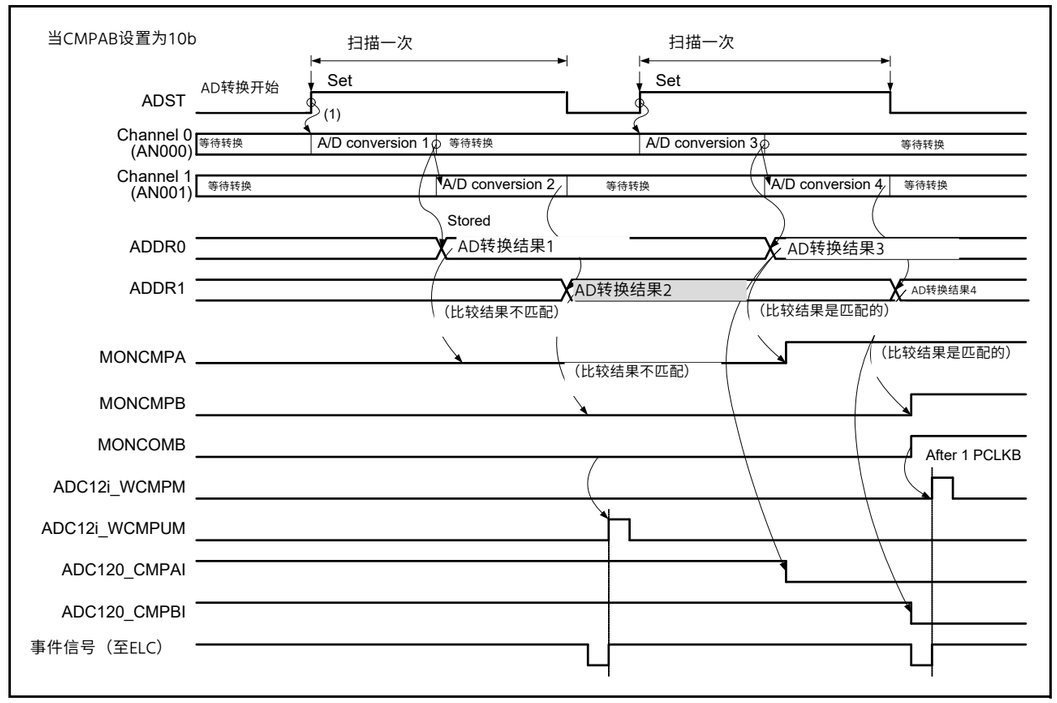


Figure 47.33 比较功能事件输出的示例操作，当AN000与AN001进行比较时

注1.比较函数输出的事件输出matchmismatch来自WindowA和Window的比较结果
B、基于ADCMPCR.CMPAB[1:0]设置。

注2.窗口A的比较结果是窗口A的比较目标通道的比较结果的逻辑相加。窗口A和窗口B的比较结果在每次AD转换时更新，即使单次扫描结束也保持不变.将ADCMPCR.CMPAE和ADCMPCR.CMPBE设置为0，将比较结果清除为0。

47.3.5.3 比较函数的约束

以下约束适用于比较功能：

- 比较功能不能与自诊断功能或双触发模式一起使用。（比较功能不适用于ADRD、ADDBLDR、ADDBLDRA和ADDBLDRB。）
- 使用匹配不匹配事件输出时指定单次扫描模式。
- 当为窗口A选择温度传感器输出或内部参考电压时，窗口B操作被禁用。
- 当为窗口B选择温度传感器输出或内部参考电压时，窗口A操作被禁用。
- 禁止将WindowA和WindowB设置为相同的通道。
- 设置参考电压值，使高电位参考电压值等于或大于低电位参考电压值。

47.3.6 模拟输入采样和扫描转换时间

扫描转换可以通过软件触发、同步触发(ELC)或异步触发(ADTRGn)来激活。在扫描开始延迟(tD)过去之后，通道专用采样保持电路的处理、断线检测辅助处理和自诊断转换处理全部进行，

followed by processing for A/D conversion.

Figure 47.34 shows the scan conversion timing, in which scan conversion is activated by a software trigger or a synchronous trigger (ELC). Figure 47.35 shows the scan conversion timing, in which scan conversion is activated by an asynchronous trigger, ADTRGn. The scan conversion time (t_{SCAN}) includes the start-of-scanning-delay (t_D), channel-dedicated sample-and-hold circuit processing time (t_{SPLSH}),*1 disconnection detection assistance processing time (t_{DIS}),*2 self-diagnosis A/D conversion processing time (t_{DIAG}),*3 A/D conversion processing time (t_{CONV} and t_{DSD}), channel-dedicated sample-and-hold circuit end time (t_{SHED}),*4 and end-of-scanning-delay (t_{ED}).

The A/D conversion processing time (t_{CONV}) consists of the input sampling time (t_{SPL}) and time for conversion by successive approximation (t_{SAM}). The sampling time (t_{SPL}) is used to charge sample-and-hold circuits in the ADC12. If there is not sufficient sampling time because of the high impedance of an analog input signal source, or if the A/D conversion clock (ADCLK) is slow, sampling time can be adjusted using the ADSSTR register.

The time for conversion by successive approximation (t_{SAM}) is 13 ADCLK states with 12-bit accuracy selected, 11 ADCLK states with 10-bit accuracy selected, and 9 ADCLK states with 8-bit accuracy selected.

The scan conversion time (t_{SCAN}) in single scan mode for which the number of selected channels is n can be determined as follows:

$$t_{SCAN} = t_D + t_{SPLSH} + (t_{DIS} \times n) + t_{DIAG} + (t_{CONV} \times n) *5 + t_{ED}$$

The scan conversion time for the first cycle in continuous scan mode is t_{SCAN} for single scan minus t_{ED} plus t_{SHED}. The scan conversion time for the second and subsequent cycles in continuous scan mode is fixed at $t_{SPLSH} + (t_{DIS} \times n) + t_{DIAG} + t_{DSD} + (t_{CONV} \times n) *5 + t_{SHED}$.

Note 1. When no channel-dedicated sample-and-hold circuits are used, $t_{SPLSH} = 0$.
Note 2. When disconnection detection assistance is not selected, $t_{DIS} = 0$.
Note 3. When the self-diagnosis function is not used, $t_{DIAG} = 0$, $t_{DSD} = 0$.
Note 4. When no channel-dedicated sample-and-hold circuits are used, $t_{SHED} = 0$, assuming continuous scan mode is active. In single scan mode and group scan mode, t_{SHED} is included in the end-of-scanning-delay (t_{ED}).
Note 5. When input sampling times (t_{SPL}) of all selected channels are the same, this element equals $t_{CONV} \times n$. If each channel has a different sampling time, this element equals that of t_{SPL} and t_{SAM} set to each selected channel.

然后进行AD转换处理。

图47.34显示了扫描转换时序，其中扫描转换由软件触发或同步触发(ELC)激活。图47.35显示了扫描转换时序，其中扫描转换由异步触发器ADTRGn激活。扫描转换时间(tSCAN)包括扫描开始延迟(tD)、通道专用采样保持电路处理时间(tSPLSH)、*1断线检测辅助处理时间(tDIS)、*2自诊断AD转换处理时间(tDIAG)、*3AD转换处理时间(tCONV和tDSD)、通道专用采样保持电路结束时间(tSHED)、*4和扫描结束–延迟（tED）。

AD转换处理时间(tCONV)由输入采样时间(tSPL)和逐次逼近转换时间(tSAM)组成。采样时间(tSPL)用于为ADC12中的采样保持电路充电。如果由于模拟输入信号源的高阻抗而没有足够的采样时间，或者如果AD转换时钟(ADCLK)很慢，则可以使用ADSSTR寄存器调整采样时间。

逐次逼近转换时间(tSAM)为13个ADCLK状态，选择12位精度，11
选择了10位精度的ADCLK状态，以及选择了8位精度的9个ADCLK状态。

选择通道数为n的单次扫描模式下的扫描转换时间(tSCAN)可以确定如下：

tSCAN=tD+tSPLSH+(tDIS×n)+tDIAG+(tCONV×n)*5+tED

连续扫描模式下第一个周期的扫描转换时间是单次扫描的tSCAN减去tED加上tSHED。连续扫描模式中第二个和后续周期的扫描转换时间固定为tSPLSH+(tDIS×n)+tDIAG+tDSD+(tCONV×n)*5+tSHED。

注1.当不使用通道专用采样保持电路时，tSPLSH=0。
注2.未选择断线检测辅助时，tDIS=0。
注3.不使用自诊断功能时，tDIAG=0，tDSD=0。
注4.当不使用通道专用的采样保持电路时，tSHED=0，假设连续扫描模式处于活动状态。在单扫描模式和组扫描模式中，tSHED包含在扫描结束延迟（tED）中。注5.当所有选定通道的输入采样时间(tSPL)相同时，该元素等于tCONV×n。如果每个

通道具有不同的采样时间，该元素等于为每个选定通道设置的tSPL和tSAM。

Table 47.10 Conversion times during scanning (in numbers of cycles of ADCLK and PCLKB)

Parameter			Symbol		Type/conditions: Synchronous trigger*4	Type/conditions: Asynchronous trigger	Type/conditions: Software trigger	Unit
Scan start processing time*1, *2	A/D conversion on Group A under Group A priority control.	Group B is to be stopped. (Group A is activated after Group B is stopped by of an A/D conversion source from Group A.)	t_D		3 PCLKB + 6 ADCLK 5 PCLKB + 3 ADCLK *5	-	-	Cycles
		Group B is not to be stopped. (Activation by an A/D conversion source from Group A.)			2 PCLKB + 4 ADCLK	-	-	
	A/D conversion when self-diagnosis is enabled	A/D conversion for self-diagnosis is to be started.			2 PCLKB + 6 ADCLK	4 PCLKB + 6 ADCLK	6 ADCLK	
	All other				2 PCLKB + 4 ADCLK	2 PCLKB + 4 ADCLK	4 ADCLK	
Channel-dedicated sample-and-hold processing time*1	Sampling time		t_{SPLSH}	t_{SH}	Without continuous sampling: setting in ADSHCR.SSTSH[7:0] (initial value = 18h × ADCLK) With continuous sampling: 0			
	Wait time between sampling and A/D Conversion			t_W	12			
Disconnection detection assistance processing time			t_{DIS}		Setting in ADNDIS[3:0] (initial value = 0h) × ADCLK			
Self-diagnosis conversion processing time*1	Sampling time		t_{DIAG}	t_{SPL}	Setting in ADSSTR00 (initial value = 0Bh) × ADCLK*3	-	-	
	Time for conversion by successive approximation	12-bit conversion accuracy		t_{SAM}	15 ADCLK	-	-	
		10-bit conversion accuracy			13 ADCLK	-	-	
		8-bit conversion accuracy			11 ADCLK	-	-	
	Wait time between self-diagnosis conversion end and analog channel sampling start			t_{DED}	2 ADCLK			
	Wait time between last channel conversion end and self-diagnosis sampling start in continuous scan mode		t_{DSD}		2 ADCLK			
A/D conversion processing time*1	Sampling time		t_{CONV}	t_{SPL}	Setting in ADSSTRn (n = 00 to 07, L, T, O) (initial value = 0Bh) × ADCLK + 0.5 ADCLK			
	Time for conversion by successive approximation	12-bit conversion accuracy		t_{SAM}	13 ADCLK			
		10-bit conversion accuracy			11 ADCLK			
		8-bit conversion accuracy			9 ADCLK			
Channel-dedicated sample-and-hold end processing time			t_{SHED}		2 ADCLK			
Scan end processing time*1			t_{ED}		1 PCLKB + 3 ADCLK 2 PCLKB + 3 ADCLK*5			

Note 1. See Figure 47.34 and Figure 47.35 for an illustration of times t_D, t_{SPLSH}, t_{DIAG}, t_{CONV}, and t_{ED}.
Note 2. This is the maximum time required from software writing or trigger input to A/D conversion start.
Note 3. The sampling time setting should satisfy the electrical characteristics.
Note 4. This does not include the time consumed in the path from timer output to trigger input.
Note 5. If ADCLK is faster than PCLKB (PCLKB to ADCLK frequency ratio = 1:2 or 1:4), the scan end processing time changes.

Table 47.10 扫描期间的转换时间（以ADCLK和PCLKB的周期数计）

Parameter			Symbol		Type/conditions: Synchronous trigger*4	Type/conditions: 异步触发	Type/conditions: 软件触发	Unit
扫描开始处理时间*1、*2	A组优先控制下A组的AD转换。	B组将被停止。（A组的AD转换源停止B组后激活A组。）	t_D		3 PCLKB + 6 ADCLK 5 PCLKB + 3 ADCLK *5	-	-	Cycles
		B组不要停止。（由A组的AD转换源激活。）			2 PCLKB + 4 ADCLK	-	-	
	启用自诊断时的AD转换	将启动用于自诊断的D转换。			2 PCLKB + 6 ADCLK	4 PCLKB + 6 ADCLK	6 ADCLK	
	所有其他				2 PCLKB + 4 ADCLK	2 PCLKB + 4 ADCLK	4 ADCLK	
通道专用采样保持处理时间*1	采样时间		t_{SPLSH}	t_{SH}	没有连续采样：设置 ADSHCR.SSTSH[7:0] (initial value = 18h × ADCLK) 连续采样：0			
	采样和AD之间的等待时间 Conversion			t_W	12			
断线检测辅助处理时间			t_{DIS}		ADNDIS[3:0]中的设置（初始值=0h）×ADCLK			
自诊断转换处理时间*1	采样时间		t_{DIAG}	t_{SPL}	在ADSSTR00中设置（初始值=0Bh）×ADCLK *3	-	-	
	逐次逼近转换时间	12位转换精度		t_{SAM}	15 ADCLK	-	-	
		10位转换精度			13 ADCLK	-	-	
		8位转换精度			11 ADCLK	-	-	
	自诊断转换结束与模拟通道采样开始之间的等待时间			t_{DED}	2 ADCLK			
	连续扫描模式下最后一次通道转换结束和自诊断采样开始之间的等待时间		t_{DSD}		2 ADCLK			
AD转换处理时间*1	采样时间		t_{CONV}	t_{SPL}	ADSSTRn(n=00to07 L T O)中的设置（初始值=0Bh）×ADCLK+0.5ADCLK			
	逐次逼近转换时间	12位转换精度		t_{SAM}	13 ADCLK			
		10位转换精度			11 ADCLK			
		8位转换精度			9 ADCLK			
通道专用的采样保持结束处理时间			t_{SHED}		2 ADCLK			
扫描结束处理时间*1			t_{ED}		1 PCLKB + 3 ADCLK 2 PCLKB + 3 ADCLK*5			

Note 1. 有关时间tD、tSPLSH、tDIAG、tCONV和tED的说明，请参见图47.34和图47.35。
Note 2. 这是从软件写入或触发输入到AD转换开始所需的最长时间。
Note 3. 采样时间设置应满足电气特性。
Note 4. 这不包括从定时器输出到触发输入的路径中消耗的时间。
Note 5. 如果ADCLK比PCLKB快（PCLKB与ADCLK频率比=1:2或1:4），则扫描结束处理时间会发生变化。

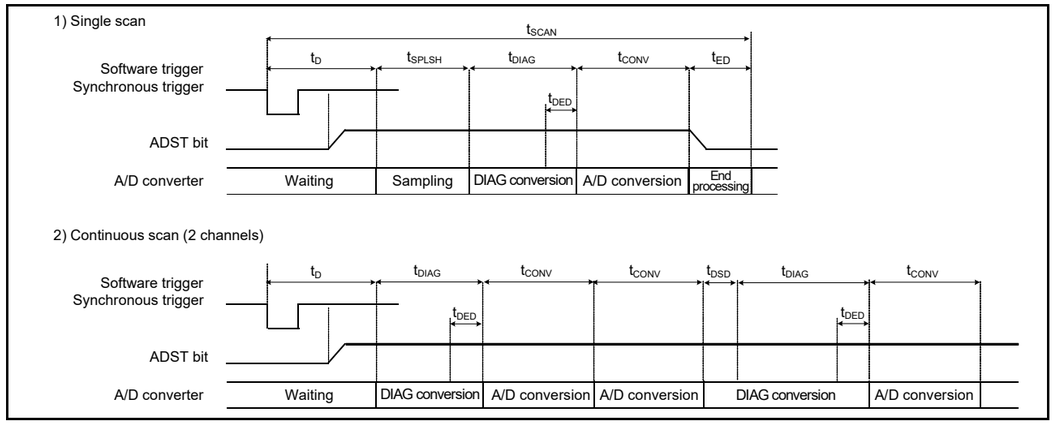


Figure 47.34 Scan conversion timing when activated by software or a synchronous trigger input (ELC)

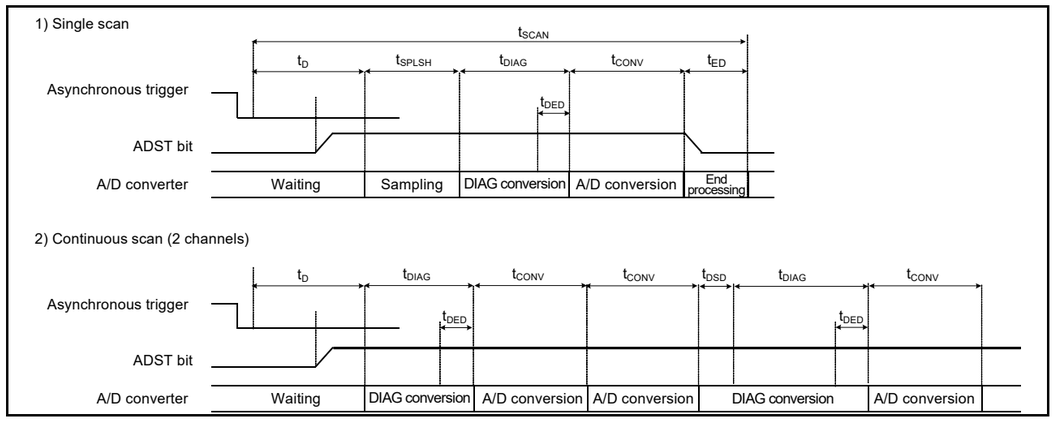


Figure 47.35 Scan conversion timing when activated by an asynchronous trigger input (ADTRG0)

47.3.7 Usage Example of A/D Data Register Automatic Clearing Function

A/D-converted value addition/average mode can be used when A/D conversion of the analog input of the selected channels, temperature sensor output, or internal reference voltage is selected.

Setting the ACE bit in ADCER to 1 automatically clears the data registers (ADDRy, ADRD, ADDBLDR, ADDBLDRA, ADDBLDRB, ADTSDR, and ADOCDR) to 0000h when the data registers are read by the CPU, DTC, or DMAC. This function enables detection of update failures by the data registers. In the following examples, the function to automatically clear the ADDRy register is enabled and disabled.

If the ACE bit in ADCER is 0 (automatic clearing disabled) and for some reason the A/D conversion result (0222h) is not written to the ADDRy register, the ADDRy value retains the old data (0111h). In addition, if this ADDRy value is read into a general-purpose register using an A/D scan end interrupt, the old data (0111h) can be saved in the general-purpose register. When checking whether there is an update failure, it is necessary to frequently save the old data in SRAM or in a general-purpose register.

If the ACE bit in ADCER is 1 (automatic clearing enabled), when ADDRy = 0111h is read by the CPU, DTC, or DMAC, ADDRy is automatically cleared to 0000h. Next, if the A/D conversion result 0222h cannot be transferred to ADDRy for some reason, the cleared data (0000h) remains as the ADDRy value. If this ADDRy value is read into a general-purpose register using an A/D scan end interrupt at this point, 0000h is saved in the general-purpose register. Occurrence of an ADDRy update failure can be determined by checking that the read data value is 0000h.

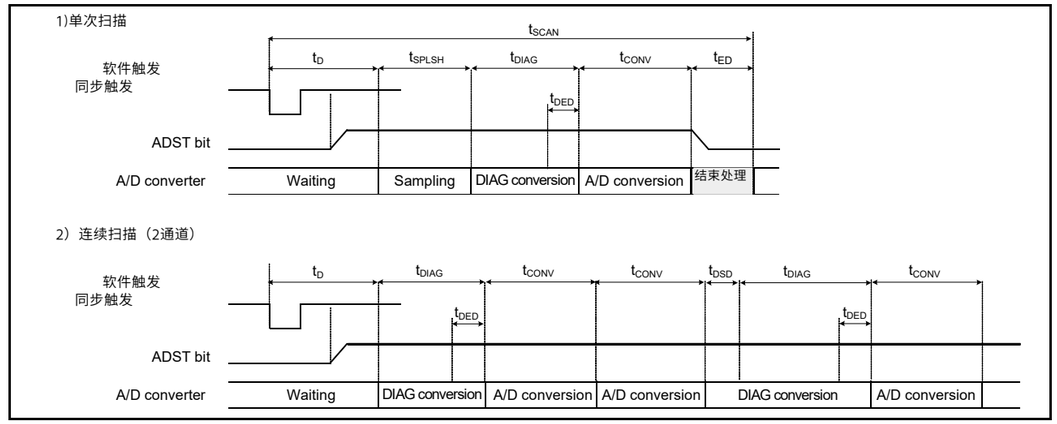


Figure 47.34 由软件或同步触发输入(ELC)激活时的扫描转换时序

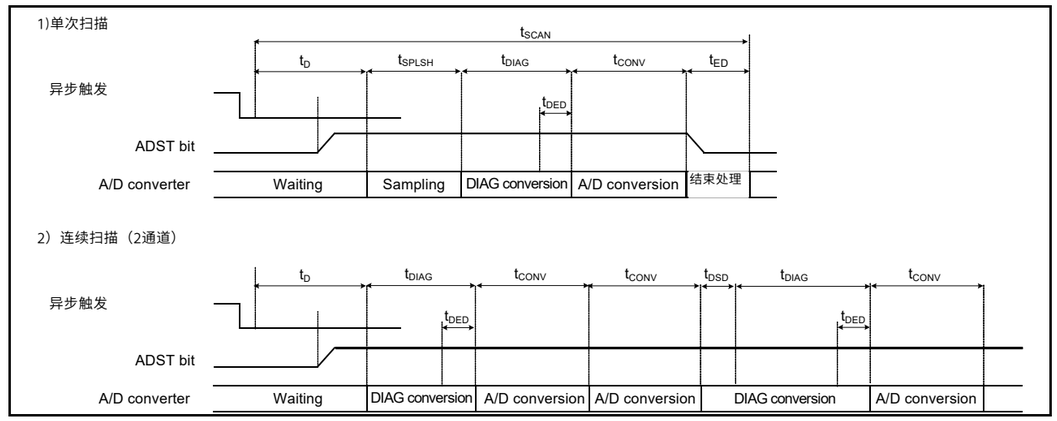


Figure 47.35 由异步触发输入(ADTRG0)激活时的扫描转换时序

47.3.7 AD数据寄存器自动清除功能的使用示例

选择通道的模拟输入、温度传感器输出或内部参考电压的AD转换时，可以使用D转换值加法平均模式。

当CPU、DTC或DMAC读取数据寄存器时，将ADCER中的ACE位设置为1会自动将数据寄存器（ADDRy、ADRD、ADDBLDR、ADDBLDRA、ADDBLDRB、ADTSDR和ADOCDR）清除为0000h。该功能可以通过数据寄存器检测更新失败。在以下示例中，自动清除ADDRy寄存器的功能被启用和禁用。

如果ADCER中的ACE位为0（禁止自动清除）并且由于某种原因AD转换结果（0222h）没有写入ADDRy寄存器，则ADDRy值保留旧数据（0111h）。此外，如果使用AD扫描结束中断将该ADDRy值读入通用寄存器，则可以将旧数据（0111h）保存在通用寄存器中。在检查是否有更新失败时，需要经常将旧数据保存在SRAM或通用寄存器中。

如果ADCER中的ACE位为1（使能自动清零），当CPU、DTC或DMAC读取ADDRy=0111h时，ADDRy会自动清零为0000h。接下来，如果AD转换结果0222h由于某种原因无法传送到ADDRy，则清除的数据(0000h)仍保留为ADDRy值。如果此时使用AD扫描结束中断将该ADDRy值读入通用寄存器，则将0000h保存在通用寄存器中。ADDRy更新失败的发生可以通过检查读取的数据值为0000h来确定。

47.3.8 A/D-Converted Value Addition/Average Mode

In A/D-converted value addition mode, the same channel is A/D-converted 1, 2, 3, 4, or 16*1 consecutive times, and the sum of the converted values is stored in the data register. In A/D-converted value average mode, the same channel is A/D-converted 2 or 4 consecutive times, and the mean of the converted values is stored in the data register. The use of the average of these results can improve the accuracy of A/D conversion, depending on the types of noise components that are present. However, this function cannot always guarantee an improvement in A/D conversion accuracy.

The A/D-converted value addition or average mode can be specified for A/D conversion of the channel select analog input, temperature sensor output, or internal reference voltage.

Note 1. The addition count can be set to 16 only when 12-bit accuracy is selected.

47.3.9 Disconnection Detection Assist Function

This converter incorporates a function that fixes the charge for sampling capacitance to the specified state (VREFH0 or VREFL0 for unit 0, VREFH or VREFL for unit 1) before the start of A/D conversion. This function enables disconnection detection in wiring of analog inputs.

When using the disconnection detection assist function for the channel-dedicated sample-and-hold circuit, set ADSHMSR.SHMD bit to 0 (select disable continuous sampling function).

If any of the following functions are used, the disconnection detection assist function must be disabled:

- The temperature sensor
- The internal reference voltage
- A/D self-diagnosis
- The programmable gain amplifier without bypass enabled.

Figure 47.36 shows the A/D conversion operation when the disconnection detection assist function is used. Figure 47.37 shows an example of disconnection detection when precharge is selected. Figure 47.38 shows an example of disconnection detection when discharge is selected.

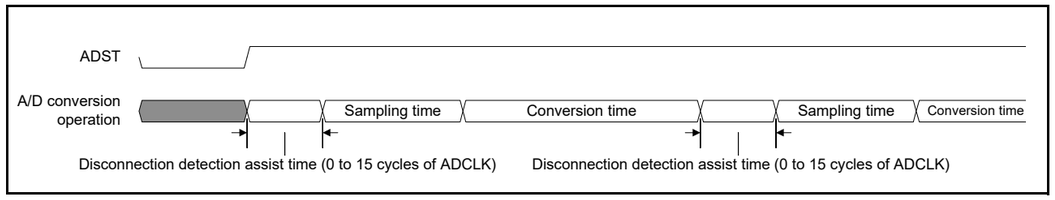


Figure 47.36 A/D conversion operation when the disconnection detection assist function is used

47.3.8 一种D转换的增值平均模式

在AD转换值加法模式下，同一通道连续进行1、2、3、4或16*1次AD转换，并将转换值的总和存储在数据寄存器中。在AD转换值平均模式下，同一通道连续进行2或4次AD转换，转换值的平均值存储在数据寄存器中。根据存在的噪声成分的类型，使用这些结果的平均值可以提高AD转换的精度。但是，该功能不能始终保证AD转换精度的提高。

可以为通道选择模拟输入、温度传感器输出或内部参考电压的AD转换指定AD转换值加法或平均模式。

注1.只有选择12位精度时，才能将加法计数设置为16。

47.3.9 断线检测辅助功能

该转换器包含一个功能，可将采样电容的电荷固定到指定状态（VREFH0或单元0的VREFL0，单元1的VREFH或VREFL）在AD转换开始之前。此功能可在模拟输入接线中进行断线检测。

使用通道专用采样保持电路的断线检测辅助功能时，设置ADSHMSR.SHMD位为0（选择禁用连续采样功能）。

如果使用以下任何功能，则必须禁用断线检测辅助功能：

- 温度传感器
- 内部参考电压
- A/D self-diagnosis
- 未启用旁路的可编程增益放大器。

图47.36显示了使用断线检测辅助功能时的AD转换操作。图47.37显示了选择预充电时的断线检测示例。图47.38显示了选择放电时的断线检测示例。

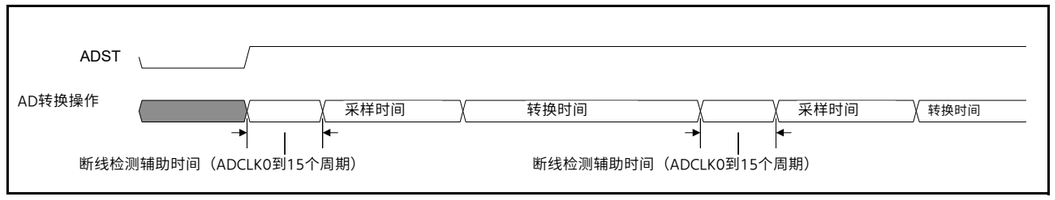
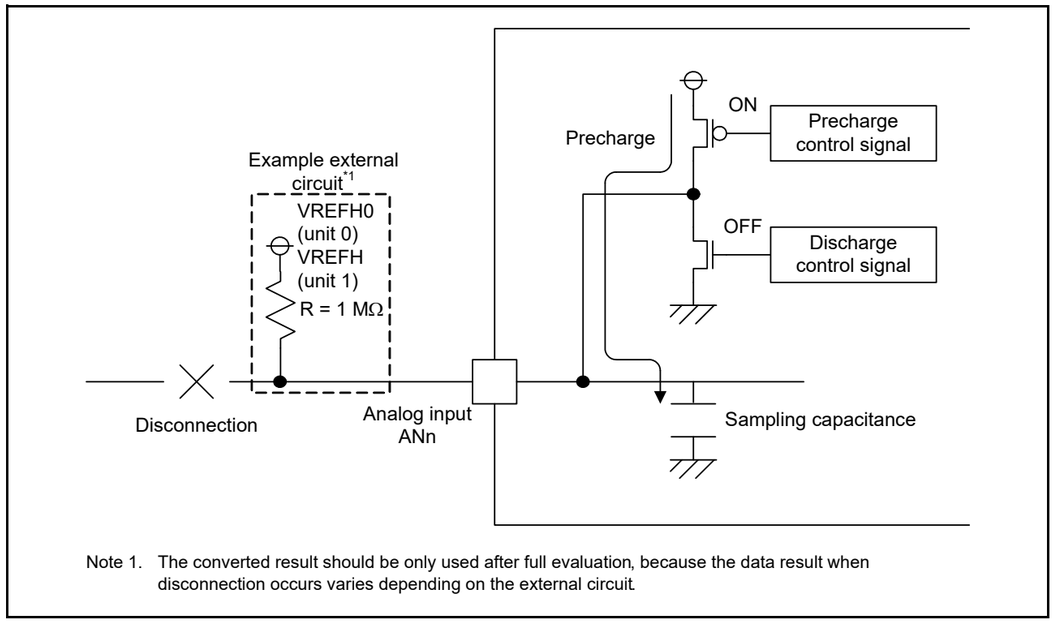
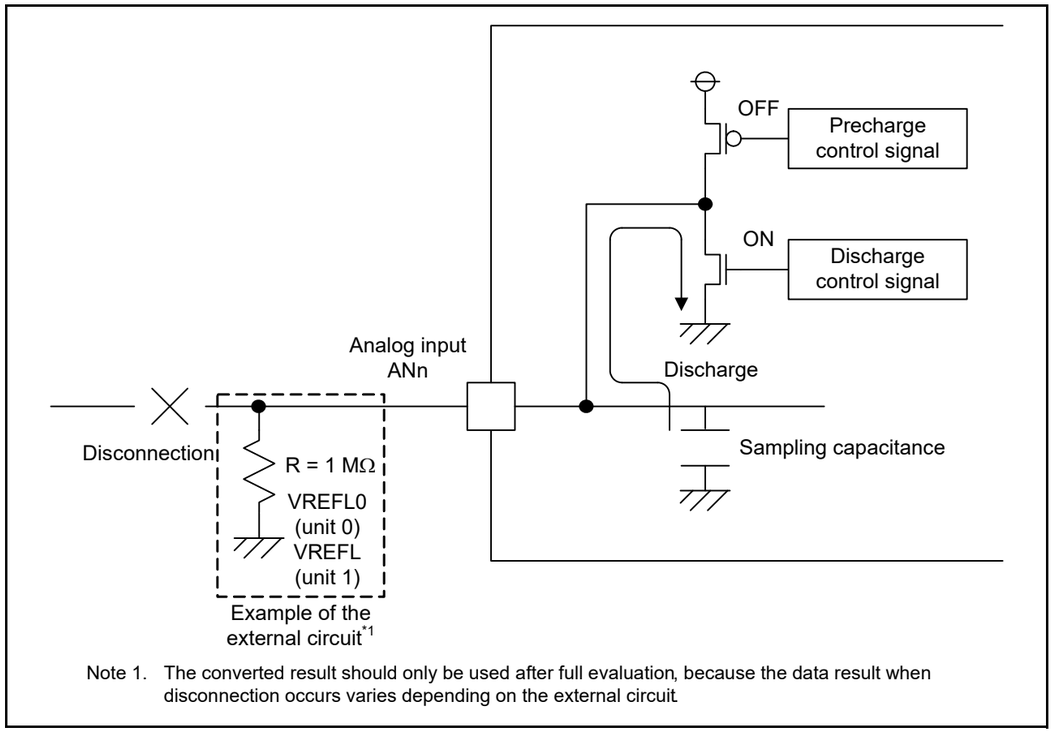


Figure 47.36 使用断线检测辅助功能时的D转换动作



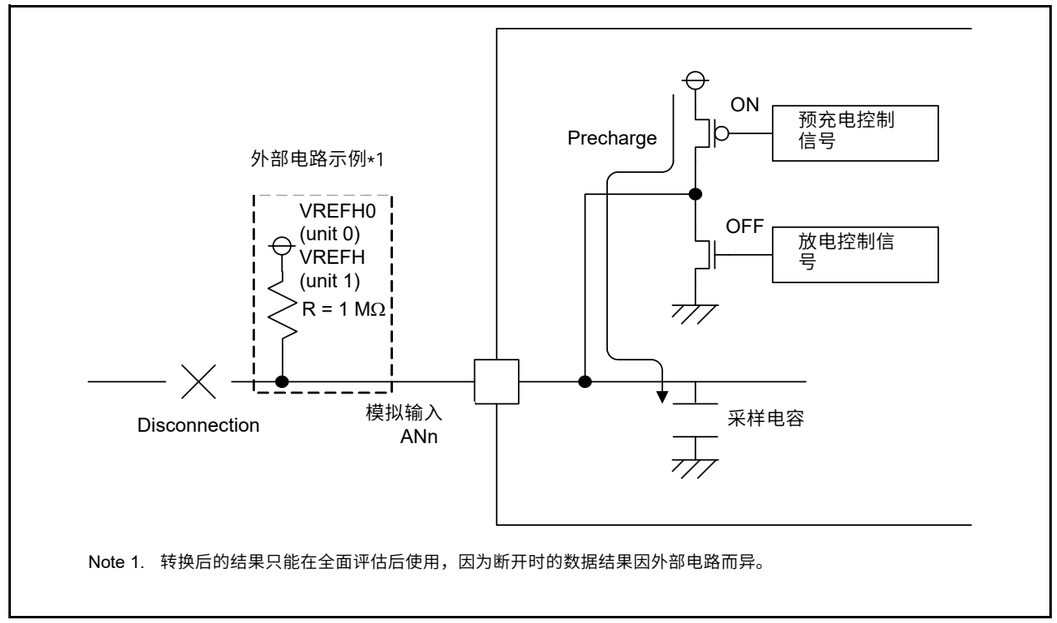
Note 1. The converted result should be only used after full evaluation, because the data result when disconnection occurs varies depending on the external circuit.

Figure 47.37 Example of disconnection detection when precharge is selected



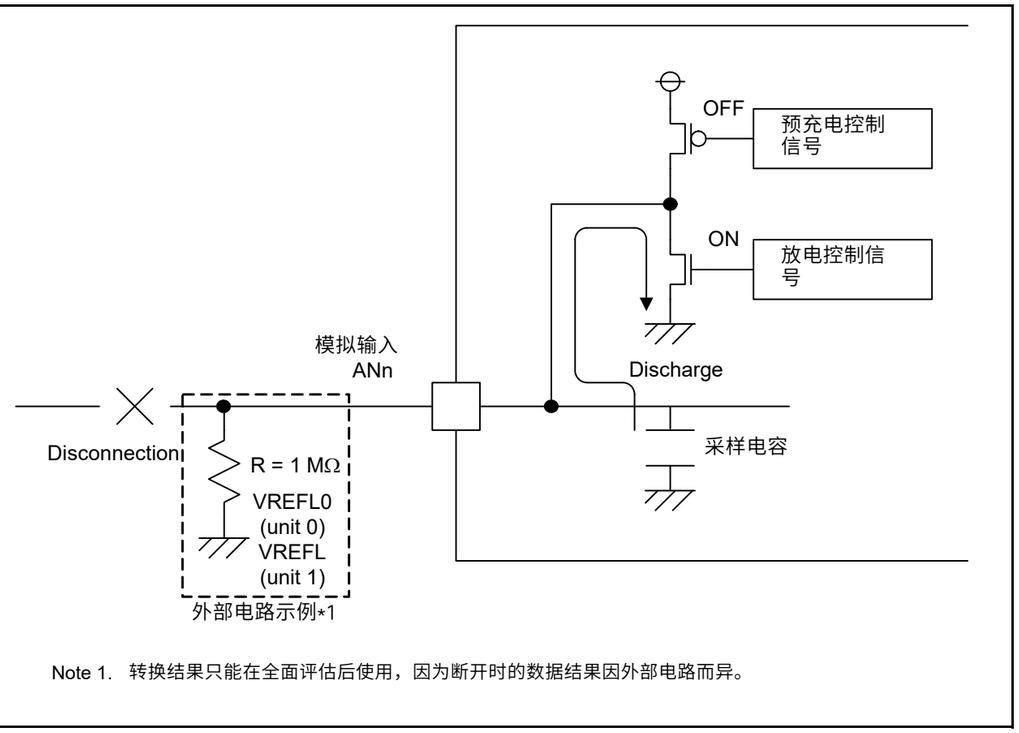
Note 1. The converted result should only be used after full evaluation, because the data result when disconnection occurs varies depending on the external circuit.

Figure 47.38 Example of disconnection detection when discharge is selected



Note 1. 转换后的结果只能在全面评估后使用，因为断开时的数据结果因外部电路而异。

Figure 47.37 选择预充电时的断线检测示例



Note 1. 转换结果只能在全面评估后使用，因为断开时的数据结果因外部电路而异。

Figure 47.38 选择放电时的断线检测示例

47.3.10 Starting A/D Conversion with an Asynchronous Trigger

A/D conversion can be started by the input of an asynchronous trigger. To start the ADC12 by an asynchronous trigger, first set the pin function in the PmnPFS register, next set the A/D Conversion Start Trigger Select bits (ADSTRGR.TRSA[5:0]) to 000000b, and then input a high-level signal to the asynchronous trigger (ADTRGn pin). Finally, set both the ADCSR.TRGE and ADCSR.EXTRG bits to 1. Figure 47.39 shows timing of the asynchronous trigger input.

An asynchronous trigger cannot be selected in the A/D conversion start trigger select bits (ADSTRGR.TRSB[5:0]) for Group B used in group scan mode. For details on setting the pin function, see section 20, I/O Ports.

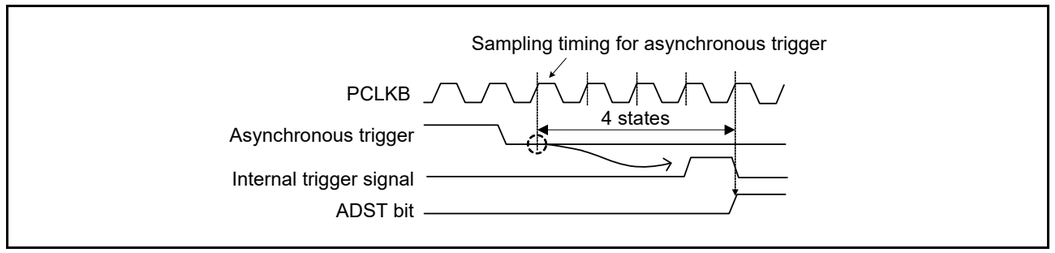


Figure 47.39 Asynchronous trigger input timing

47.3.11 Starting A/D Conversion with a Synchronous Trigger from a Peripheral Module

A/D conversion can be started by a synchronous trigger (ELC). To start the A/D conversion by a synchronous trigger, set the ADCSR.TRGE bit to 1, clear the ADCSR.EXTRG bit to 0, and select the relevant sources in the ADSTRGR.TRSA[5:0] and ADSTRGR.TRSB[5:0] bits.

47.3.12 Programmable Gain Amplifiers

Up to three programmable gain amplifiers (PGAs) can be used in each unit. Select a gain in the ADPGAGS.PnGAIN[3:0] bits (n = 000 to 002) and select an operational amplifier to be used in the ADPGACR.PnSEL bits.

These PGAs accept differential inputs. Pins that accept differential inputs are PGAVSS000 for AN000 to AN002 (unit 0), PGAVSS100 for AN100 to AN102 (unit 1). To use differential inputs, set the differential input gain in the ADPGADCR0.PnDG[2:0] bits, enable the differential input gain setting in the ADPGADCR0.PnGEN bits, and then select the differential input amplifier in the ADPGADCR0.PnDEN bits. The PGA register is selectable as shown in Table 47.11.

Table 47.11 Setting of PGA register and available related functions

Selectable value for each condition	Setting of corresponding Register				related function ✓: available x: unavailable			
	PmnPFS	ADPGACR	ADPGAGS0	ADPGADCR0		ACMPHS*2		
	ASEL*3	PGA P002: bits [11:8] PGA P001: bits [7:4] PGA P000: bit [3:0]	bits [11:8] bits [7:4] bit [3:0]	bits [11:8] bits [7:4] bit [3:0]	Ports*1	IVCMP2	IVCMP3	ADC12
When using Ports	0	Leave these bits with initial values			✓	x	x	x
When using ACMPHS or ADC12(PGA bypass)*4	1	9	0	0	x	✓	x	✓
When using PGA Differential input disabled	1	Eh	0 to Eh	0	x	✓	✓	✓
When using PGA Differential input enabled	1	Eh	1, 5, 9, Bh	8 to Bh	x	x	✓	✓

Note 1. Ports: When using input ports.
Note 2. ACMPHS IVCMP2: When using input through the PGA. ACMPHS IVCMP3: When using input of PGA output.
Note 3. For detail on the configuration of PmnPFS registers, see section 20, I/O Ports.
Note 4. Ports and ACMPHS cannot be used at the same time. Ports and ADC12 cannot be used at the same time.

47.3.10 使用异步触发启动AD转换

可以通过输入异步触发器来启动D转换。要通过异步触发启动ADC12，首先在PmnPFS寄存器中设置引脚功能，然后将AD转换启动触发选择位(ADSTRGR.TRSA[5:0])设置为000000b，然后输入高电平信号到异步触发（ADTRGn引脚）。最后，将ADCSR.TRGE和ADCSR.EXTRG位都设置为1。图47.39显示了异步触发输入的时序。

无法在AD转换开始触发选择位(ADSTRGR.TRSB[5:0])中选择异步触发GroupB用于组扫描模式。有关设置引脚功能的详细信息，请参见第20节，IO端口。

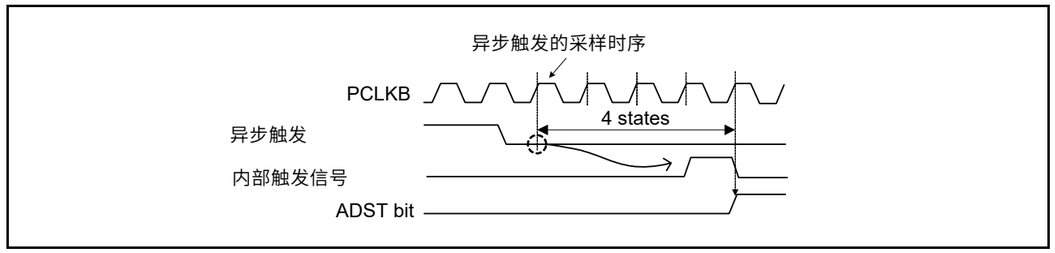


Figure 47.39 异步触发输入时序

47.3.11 使用来自外设模块的同步触发启动AD转换

D转换可以通过同步触发器(ELC)启动。要通过同步触发启动AD转换，请将ADCSR.TRGE位设置为1，将ADCSR.EXTRG位清除为0，并在ADSTRGR.TRSA[5:0]和ADSTRGR.TRSB[5]中选择相关源：0]位。

47.3.12 可编程增益放大器

每个单元最多可使用三个可编程增益放大器(PGA)。选择增益ADPGAGS.PnGAIN[3:0]位（n=000到002）并选择要在ADPGACR.PnSEL位中使用的运算放大器。

这些PGA接受差分输入。接受差分输入的引脚是PGAVSS000，用于AN000到AN002（单元0），PGAVSS100用于AN100至AN102（单元1）。要使用差分输入，设置差分输入增益ADPGADCR0.PnDG[2:0]位，使能ADPGADCR0.PnGEN位中的差分输入增益设置，然后在ADPGADCR0.PnDEN位中选择差分输入放大器。PGA寄存器是可选的，如表47.11所示。

Table 47.11 PGA寄存器的设置和可用的相关功能

每个条件的可选值	对应寄存器的设置				相关功能 ：可用 x：不可用			
	PmnPFS	ADPGACR	ADPGAGS0	ADPGADCR0		ACMPHS*2		
	ASEL*3	PGAP002：位[11:8] PGAP001：位[7:4] PGAP000：位[3:0]	bits [11:8] bits [7:4] bit [3:0]	bits [11:8] bits [7:4] bit [3:0]	Ports*1	IVCMP2	IVCMP3	ADC12
使用端口时	0	将这些位保留为初始值			✓	x	x	x
使用ACMPHS或ADC12（PGA旁路）时*4	1	9	0	0	x	✓	x	✓
使用PGA时 差分输入禁用	1	Eh	0到呃	0	x	✓	✓	✓
使用PGA时 启用差分输入	1	Eh	1, 5, 9, Bh	8 to Bh	x	x	✓	✓

Note 1. 端口：使用输入端口时。
Note 2. ACMPHSIVCMP2：通过PGA使用输入时。ACMPHSIVCMP3：使用PGA输出的输入时。
Note 3. 有关PmnPFS寄存器配置的详细信息，请参见第20节，IO端口。
Note 4. 端口和ACMPHS不能同时使用。端口和ADC12不能同时使用。

Table 47.12 shows the calculation formula for the PGA output voltage.

Table 47.12 PGA output voltage

Mode	PGA output voltage
Single	Gain × Vin
Differential	Gain (Vin - Vs) + 0.5 × AVCC

Vin: AN000 to AN002, AN100 to AN102
Vs: PGAVSS00, PGAVSS001

47.4 Interrupt Sources and DTC/DMAC Transfer Requests

47.4.1 Interrupt Requests

The ADC12 can send scan end interrupt requests, ADC12i_ADI (i = 0, 1) and ADC12i_GBADI, to the CPU. The module also generates the ADC12i_CMPAI and ADC12i_CMPBI interrupts to the CPU in response to matches with a comparison condition.

An ADC12i_ADI interrupt is always generated. An ADC12i_GBADI interrupt can be generated by setting the ADCSR.GBADIE bit to 1. Similarly, ADC12i_CMPAI and ADC12i_CMPBI interrupts can be generated by setting the ADCMPCR.CMPAIE and ADCMPCR.CMPBIE bit to 1.

In addition, the DTC or DMAC can be started when an ADC12i_ADI or ADC12i_GBADI interrupt, or ADC12i_WCMPM or ADC12i_WCMPUM event is generated. Using these interrupts or events to allow the DTC or DMAC to read the converted data enables continuous conversion without burdening the software.

For details on the DTC settings, see section 18, Data Transfer Controller (DTC), and for details on the DMAC settings, see section 17, DMA Controller (DMAC).

Table 47.13 describes the interrupt sources and ELC events available for the ADC12.

PGA输出电压的计算公式如表47.12所示。

Table 47.12 PGA输出电压

Mode	PGA输出电压
Single	增益 Vin
Differential	Gain (Vin - Vs) + 0.5 × AVCC

Vin: AN000 to AN002, AN100 to AN102
Vs: PGAVSS00, PGAVSS001

47.4 中断源和DTCDMAC传输请求

47.4.1 中断请求

ADC12可以向CPU发送扫描结束中断请求ADC12i_ADI(i=0 1)和ADC12i_GBADI。该模块还向CPU生成ADC12i_CMPAI和ADC12i_CMPBI中断，以响应与比较条件的匹配。

始终会产生ADC12i_ADI中断。ADC12i_GBADI中断可以通过设置ADCSR.GBADIE位为1。类似地，ADC12i_CMPAI和ADC12i_CMPBI中断可以通过设置ADCMPCR.CMPAIE和ADCMPCR.CMPBIE位为1。

此外，当ADC12i_ADI或ADC12i_GBADI中断时，可以启动DTC或DMAC，或者生成ADC12i_WCMPM或ADC12i_WCMPUM事件。使用这些中断或事件来允许DTC或读取转换数据的DMAC可以实现连续转换，而不会增加软件负担。

有关DTC设置的详细信息，请参阅第18节，数据传输控制器(DTC)，有关DMAC设置的详细信息，请参阅第17节，DMA控制器(DMAC)。

表47.13描述了ADC12可用的中断源和ELC事件。

Table 47.13 ADC12 events (1 of 2)

✓: available x: unavailable

Operation		Interrupt request or ELC event			Inter-rupt re-quest	DTC/ DMAC activa-tion	ELC event re-quest	Function
Scan mode	Double-trigger mode	Compare function Window A/B	Unit 0	Unit 1				
Single scan mode	Deselected	Deselected	ADC120_ADI	ADC121_ADI	✓	✓	✓	ADC12i_ADI generated at the end of single scan
		Selected	ADC120_ADI	ADC121_ADI	✓	✓	✓	ADC12i_ADI generated at the end of single scan
			ADC120_CMPAI	ADC121_CMPAI	✓	x	x	ADC12i_CMPAI generated on a match comparison condition of Window A
			ADC120_CMPBI	ADC121_CMPBI	✓	x	x	ADC12i_CMPBI generated on a match comparison condition of Window B
			ADC120_WCMPM	ADC121_WCMPM	x	✓	✓	ADC12i_WCMPM generated on a match condition of the Window A/B compare function
			ADC120_WCMPUM	ADC121_WCMPUM	x	✓	✓	ADC12i_WCMPUM generated on a mismatch condition of the Window A/B compare function
	Selected	Deselected	ADC120_ADI	ADC121_ADI	✓	✓	✓	ADC12i_ADI generated at the end of scans in the even-numbered times
Continuous scan mode	Deselected	Deselected	ADC120_ADI	ADC121_ADI	✓	✓	✓	ADC12i_ADI generated at the end of scan of all selected channels
		Selected	ADC120_CMPAI	ADC121_CMPAI	✓	x	x	ADC12i_CMPAI generated on a match comparison condition of Window A
			ADC120_CMPBI	ADC121_CMPBI	✓	x	x	ADC12i_CMPBI generated on a match comparison condition of Window B

Table 47.13 ADC12事件(1of2)

：可用x：不可用

Operation		中断请求或ELC事件			中断请求	DTC/ DMAC activa-tion	ELC事件请求	Function
扫描模式	双触发模式	比较函数窗口AB	Unit 0	Unit 1				
单次扫描模式	Deselected	Deselected	ADC120_ADI	ADC121_ADI	✓	✓	✓	ADC12i_ADI在单次扫描结束时生成
		Selected	ADC120_ADI	ADC121_ADI	✓	✓	✓	ADC12i_ADI在单次扫描结束时生成
			ADC120_CMPAI	ADC121_CMPAI	✓	x	x	在窗口A的匹配比较条件下生成ADC12i_CMPAI
			ADC120_CMPBI	ADC121_CMPBI	✓	x	x	在窗口B的匹配比较条件下生成的ADC12i_CMPBI
			ADC120_WCMPM	ADC121_WCMPM	x	✓	✓	在窗口AB比较功能的匹配条件下生成ADC12i_WCMPM
			ADC120_WCMPUM	ADC121_WCMPUM	x	✓	✓	ADC12i_WCMPUM在窗口AB比较功能的不匹配条件下生成
	Selected	Deselected	ADC120_ADI	ADC121_ADI	✓	✓	✓	在偶数次扫描结束时生成ADC12i_ADI
连续扫描模式	Deselected	Deselected	ADC120_ADI	ADC121_ADI	✓	✓	✓	在所有选定通道的扫描结束时生成ADC12i_ADI
		Selected	ADC120_CMPAI	ADC121_CMPAI	✓	x	x	在窗口A的匹配比较条件下生成ADC12i_CMPAI
			ADC120_CMPBI	ADC121_CMPBI	✓	x	x	在窗口B的匹配比较条件下生成的ADC12i_CMPBI

Table 47.13 ADC12 events (2 of 2)

✓: available x: unavailable

Operation		Interrupt request or ELC event			Inter-rupt re-quest	DTC/ DMAC activa-tion	ELC event re-quest	Function
Scan mode	Double-trigger mode	Compare function Window A/B	Unit 0	Unit 1				
Group scan mode	Deselected	Deselected	ADC120_ADI	ADC121_ADI	✓	✓	✓	ADC12i_ADI generated at the end of Group A scan
			ADC120_GBADI	ADC121_GBADI	✓	✓	x	ADC12i_GBADI dedicated to Group B generated at the end of Group B scan
		Selected	ADC120_ADI	ADC121_ADI	✓	✓	✓	ADC12i_ADI generated at the end of Group A scan
			ADC120_GBADI	ADC121_GBADI	✓	✓	x	ADC12i_GBADI dedicated to Group B generated at the end of Group B scan
			ADC120_CMPAI	ADC121_CMPAI	✓	x	x	ADC12i_CMPAI generated on a match comparison condition of Window A
			ADC120_CMPBI	ADC121_CMPBI	✓	x	x	ADC12i_CMPBI generated on a match comparison condition of Window B
	Selected	Deselected	ADC120_ADI	ADC121_ADI	✓	✓	✓	ADC12i_ADI generated at the end of Group A scans in the even-numbered times
			ADC120_GBADI	ADC121_GBADI	✓	✓	x	ADC12i_GBADI dedicated to Group B generated at the end of Group B scan

Note: i = 0: unit 0, i = 1: unit 1.

47.5 Event Link Function

47.5.1 Event Output to the ELC

The ELC uses the ADC12i_ADI interrupt request signal as an event signal, enabling link operation for the preset module. The ADC12i_GBADI interrupt and ADC12i_CMPAI/ADC12i_CMPBI interrupts cannot be used as event signals. For details, see Table 47.13.

47.5.2 ADC12 Operation through an Event from the ELC

The ADC12 can start A/D conversion by the preset event specified in the ELSRn settings for the ELC as follows:

- Select the ELC_AD00 (unit 0) signal in the ELC.ELSR8 register
- Select the ELC_AD01 (unit 0) signal in the ELC.ELSR9 register
- Select the ELC_AD10 (unit 1) signal in the ELC.ELSR10 register
- Select the ELC_AD11 (unit 1) signal in the ELC.ELSR11 register.

If an ELC_ADi0 or ELC_ADi1 event occurs during A/D conversion, the event is disabled.

Table 47.13 ADC12事件（2个中的2个）

：可用x：不可用

Operation		中断请求或ELC事件			中断请求	DTC/ DMAC activa-tion	ELC事件请求	Function
扫描模式	双触发模式	比较函数窗口AB	Unit 0	Unit 1				
组扫描模式	Deselected	Deselected	ADC120_ADI	ADC121_ADI	✓	✓	✓	ADC12i_ADI在A组扫描结束时生成
			ADC120_GBADI	ADC121_GBADI	✓	✓	x	在B组扫描结束时生成的专用于B组的ADC12i_GBADI
		Selected	ADC120_ADI	ADC121_ADI	✓	✓	✓	ADC12i_ADI在A组扫描结束时生成
			ADC120_GBADI	ADC121_GBADI	✓	✓	x	在B组扫描结束时生成的专用于B组的ADC12i_GBADI
			ADC120_CMPAI	ADC121_CMPAI	✓	x	x	在窗口A的匹配比较条件下生成ADC12i_CMPAI
			ADC120_CMPBI	ADC121_CMPBI	✓	x	x	在窗口B的匹配比较条件下生成的ADC12i_CMPBI
	Selected	Deselected	ADC120_ADI	ADC121_ADI	✓	✓	✓	ADC12i_ADI在A组结束时生成的偶数次扫描
			ADC120_GBADI	ADC121_GBADI	✓	✓	x	在B组扫描结束时生成的专用于B组的ADC12i_GBADI

Note: i = 0: unit 0, i = 1: unit 1.

47.5 事件链接功能

47.5.1 事件输出到ELC

ELC使用ADC12i_ADI中断请求信号作为事件信号，为预设模块启用链接操作。
ADC12i_GBADI中断和ADC12i_CMPAIADC12i_CMPBI中断不能用作事件信号。详见表47.13。

47.5.2 ADC12通过来自ELC的事件进行操作

ADC12可以通过ELC的ELSRn设置中指定的预设事件启动AD转换，如下所示：

- 选择ELC.ELSR8寄存器中的ELC_AD00（单元0）信号
- 选择ELC.ELSR9寄存器中的ELC_AD01（单元0）信号
- 选择ELC.ELSR10寄存器中的ELC_AD10（单元1）信号
- 选择ELC.ELSR11寄存器中的ELC_AD11（单元1）信号。

如果在AD转换期间发生ELC_ADi0或ELC_ADi1事件，则该事件被禁用。

47.6 Usage Notes

47.6.1 Constraints on Reading the Data Registers

The following registers must be read in halfword units:

- A/D Data Registers
- A/D Data Duplexing Register
- A/D Data Duplexing Register A
- A/D Data Duplexing Register B
- A/D Temperature Sensor Data Register
- A/D Internal Reference Voltage Register
- A/D Self-Diagnosis Data Register.

If a register is read twice in byte units, that is, the upper byte and bytes are read separately, the A/D-converted value read initially might disagree with the A/D-converted value read subsequently. To prevent this, never read the data registers in byte units.

47.6.2 Constraints on Stopping A/D Conversion

To stop A/D conversion when an asynchronous trigger or a synchronous trigger is selected as the condition for starting A/D conversion, follow the procedure shown in Figure 47.40.

47.6 使用说明

47.6.1 读取数据寄存器的限制

以下寄存器必须以半字为单位读取：

- AD数据寄存器
- AD数据双工寄存器
- AD数据双工寄存器A
- AD数据双工寄存器B
- AD温度传感器数据寄存器
- AD内部参考电压寄存器
- AD自诊断数据寄存器。

如果以字节为单位读取寄存器两次，即分别读取高字节和字节，则最初读取的AD转换值可能与随后读取的AD转换值不一致。为防止这种情况，切勿以字节为单位读取数据寄存器。

47.6.2 停止AD转换的约束

选择异步触发或同步触发作为启动条件时停止AD转换
AD转换，按照图47.40所示的步骤进行。

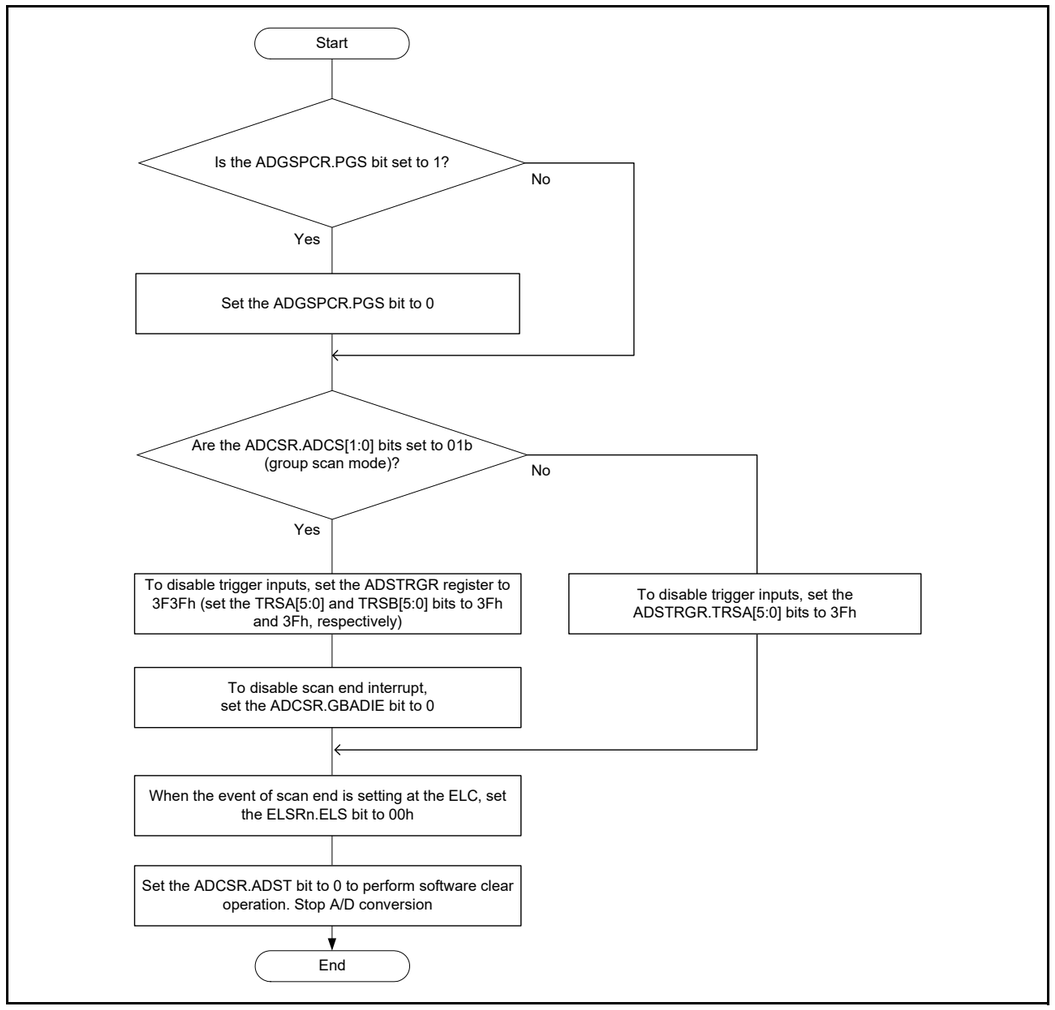


Figure 47.40 Procedures for clearing the ADCSR.ADST bit by software

47.6.3 A/D Conversion Restart and Termination Timing

A maximum of 6 ADCLK cycles is required for the idle analog unit of the ADC12 to restart on setting the ADCSR.ADST bit to 1. A maximum of 2 ADCLK cycles is required for the operating analog unit of the ADC12 to be terminate on setting the ADCSR.ADST bit to 0.

47.6.4 Constraints on Scan End Interrupt Handling

When scanning the same analog input twice using any trigger, the first A/D-converted data is overwritten with the second A/D-converted data if the CPU does not finish reading the A/D-converted data by the time the A/D conversion of the first analog input for the second scan ends after the first scan end interrupt is generated.

47.6.5 Settings for the Module-Stop Function

ADC12 operation can be disabled or enabled using the Module Stop Control Register. The ADC12 is initially stopped after reset. Releasing the module-stop state enables access to the registers. After release from the module-stop state, wait for at least 1 µs before starting A/D conversion. For details, see section 11.4, Module-Stop Function.

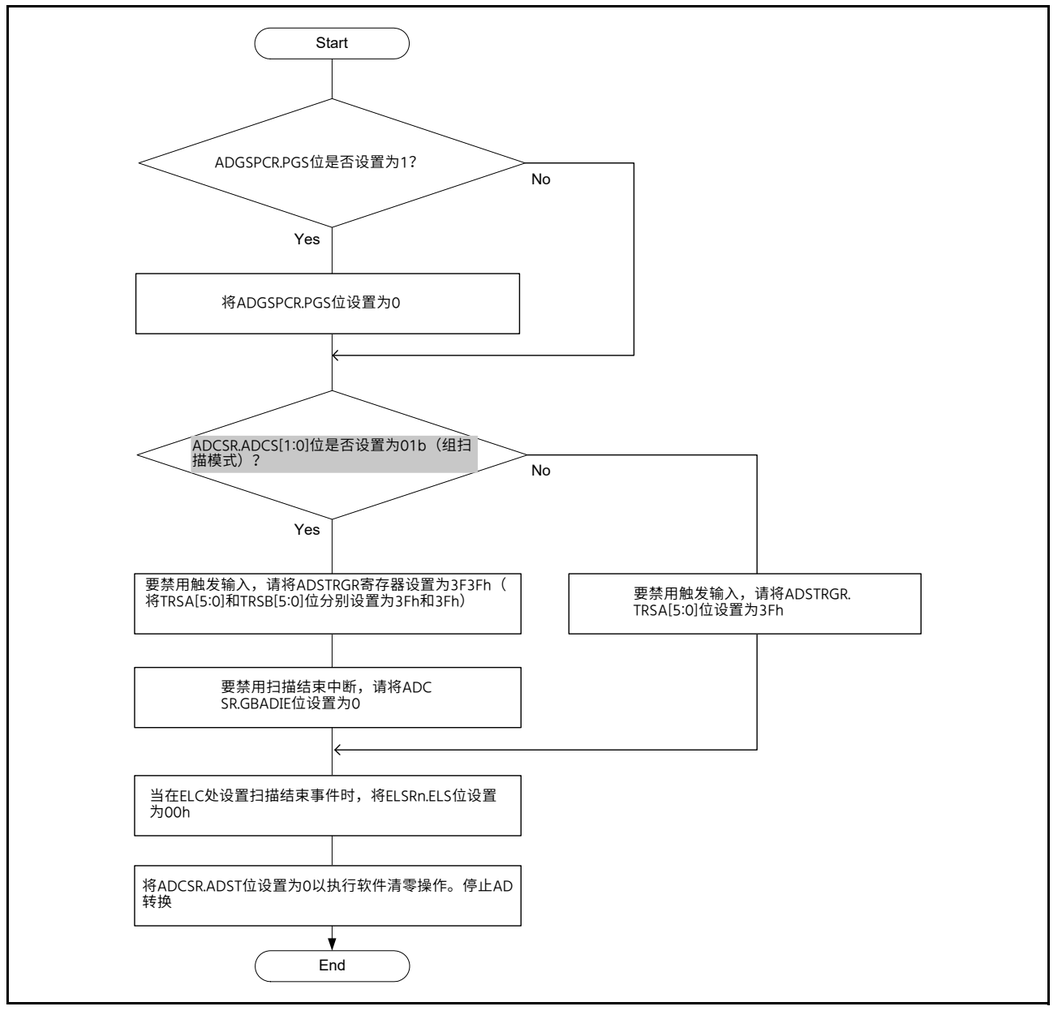


Figure 47.40 通过软件清除ADCSR.ADST位的程序

47.6.3 AD转换重启和终止时序

ADC12的空闲模拟单元最多需要6个ADCLK周期才能在设置时重新启动ADCSR.ADST位为1。ADC12的操作模拟单元最多需要2个ADCLK周期才能在将ADCSR.ADST位设置为0时终止。

47.6.4 扫描结束中断处理的约束

当使用任何触发器扫描相同的模拟输入两次时，如果CPU在第一个AD转换之前没有完成读取AD转换的数据，则第一个AD转换的数据将被第二个AD转换的数据覆盖第二次扫描的模拟输入在第一次扫描结束中断产生后结束。

47.6.5 模块停止功能的设置

可以使用模块停止控制寄存器禁用或启用ADC12操作。ADC12在复位后最初停止。释放模块停止状态可以访问寄存器。从模块停止状态释放后，在开始AD转换之前至少等待1微秒。有关详细信息，请参阅第11.4节，模块停止功能。

47.6.6 Notes on Entering the Low-Power States

Before entering the module-stop state or Software Standby mode, you must stop A/D conversion. Here, set the ADCSR.ADST bit to 0 and secure a period of time until the analog unit of the ADC12 stops.

To secure this time, follow the procedure shown in Figure 47.40 for clearing the ADCSR.ADST bit by software. Next, wait for 2 clock cycles of ADCLK before entering the module-stop state or Software Standby mode.

47.6.7 Error in Absolute Accuracy When Disconnection Detection Assistance Is in Use

Using disconnection detection assistance leads to an error in the absolute accuracy of the ADC12. This error arises because an erroneous voltage is input to the analog input pins because of the resistive voltage division between the pull-up or pull-down resistor (Rp) and the resistance of the signal source (Rs). This error in absolute accuracy is calculated from the following formula.

Maximum error in absolute accuracy (LSB) = $(2^{Resolution} - 1) \times Rs / (Rs + Rp)$, Resolution = 12, 10, 8

Only use disconnection detection assistance after thorough evaluation.

47.6.8 Available Functions and Register Settings of AN000 to AN002, AN007, AN100 to AN102, and AN107

Table 47.14 shows the available functions and register setting of AN000 to AN002, AN007, AN100 to AN102, and AN107. Figure 47.41 shows the setting procedure of registers. To use each function, set the register value shown in Table 47.14.

When the PGA is used with differential input enabled, a negative voltage can be input for AN000 to AN002 and PGAVSS000 for unit 0, and AN100 to AN102 and PGAVSS100 for unit 1 pin after setting the registers.

When the PGA is used with differential input enabled, all PGA amplifiers in each unit must be set to differential input in the ADPGADCR0 register.

When the PGA is used with differential input disabled, the associated PGAVSS pin must be connected to AVSS0. When the PGA is not used, the associated PGAVSS can be used as an input port.

When transitioning to the ADC module-stop state or Software Standby mode from the state of using PGA or sample-and-hold circuit, if 0 is set to the associated bit of ADPGACR or ADSHCR register of each ADC12 before transitioning, power consumption can be reduced.

The initial value of the ASEL bit of P003 and P007 is 1. When these pins are not used as an analog function, to reduce the input leakage current, set the ASEL bit to 0.

Table 47.14 Available functions and register setting

Available functions						Register setting				
						P0nPFS*6		PGA		S/H*3
Ports*1	IRQ*2	S/H*3	PGA-S*4	PGA-D*5	ADC12	ASEL	ISEL	ADPGADCR0*7	ADPGACR*8	ADSHCR*9
✓	-	-	-	-	-	0	0	x	x	x
-	✓	-	-	-	-	0	1	x	x	x
-	-	-	-	-	✓*10	1	x	0	9h	0
-	-	-	-	-	✓*11	1	x	0*11	0 or 9h	0
-	-	✓	-	-	✓	1	x	0	9h	1 (0*13)
-	-	✓	✓	-	✓	1	x	0	Eh (0h*12)	1 (0*13)
-	-	✓	-	✓	✓	1	x	1	Eh (0h*12	1 (0*13)
-	-	-	✓	-	✓	1	x	0	Eh (0h*12	0
-	-	-	-	✓	✓	1	x	1	Eh (0h*12	0

✓: Available
x: Don't care
Note 1. Ports: P000 to P007 can be used as port inputs.
Note 2. IRQ: P000 to P002 and P003 to P005 can be used as IRQ pins.
Note 3. S/H: sample-and-hold circuit.
Note 4. PGA-S: When the PGA setting is Differential input disabled. Corresponding PGAVSS must be set as ASEL to 1,

47.6.6 进入低功耗状态的注意事项

在进入模块停止状态或软件待机模式之前，您必须停止AD转换。在这里，设置ADCSR.ADST位为0并确保一段时间，直到ADC12的模拟单元停止。

为确保该时间，请按照图47.40中所示的过程通过软件清除ADCSR.ADST位。接下来，在进入模块停止状态或软件待机模式之前等待ADCLK的2个时钟周期。

47.6.7 使用断线检测辅助时的绝对精度误差

使用断开检测辅助会导致ADC12的绝对精度出现误差。由于上拉或下拉电阻(Rp)与信号源电阻(Rs)之间的电阻分压，导致错误电压输入到模拟输入引脚，因此会出现此错误。该绝对精度误差由以下公式计算得出。

绝对精度的最大误差(LSB)=(2分辨率−1)×Rs(Rs+Rp)，分辨率=12 10 8

仅在全面评估后使用断线检测辅助。

47.6.8 AN000至AN002、AN007、AN100至AN102和AN107的可用功能和寄存器设置

表47.14显示了AN000至AN002、AN007、AN100至AN102和AN107。图47.41显示了寄存器的设置过程。要使用每个功能，请设置表47.14中所示的寄存器值。

当PGA与差分输入使能时，AN000到AN002可以输入负电压，并且设置寄存器后，单元0为PGAVSS000，单元1引脚为AN100至AN102和PGAVSS100。

当PGA在差分输入使能的情况下使用时，每个单元中的所有PGA放大器都必须在ADPADCR0寄存器中设置为差分输入。

当PGA在差分输入禁用的情况下使用时，相关的PGAVSS引脚必须连接到AVSS0。当不使用PGA时，关联的PGAVSS可以用作输入端口。

当从使用PGA或采样保持电路的状态转换到ADC模块停止状态或软件待机模式时，如果在转换前将每个ADC12的ADPGACR或ADSHCR寄存器的相关位设置为0，则可以降低功耗。

P003和P007的ASEL位初始值为1。当这些引脚不用作模拟功能时，为减小输入漏电流，将ASEL位设置为0。

Table 47.14 可用功能和寄存器设置

可用功能						注册设置				
						P0nPFS*6		PGA		S/H*3
Ports*1	IRQ*2	S/H*3	PGA-S*4	PGA-D*5	ADC12	ASEL	ISEL	ADPGADCR0*7	ADPGACR*8	ADSHCR*9
✓	-	-	-	-	-	0	0	x	x	x
-	✓	-	-	-	-	0	1	x	x	x
-	-	-	-	-	✓*10	1	x	0	9h	0
-	-	-	-	-	✓*11	1	x	0*11	0 or 9h	0
-	-	✓	-	-	✓	1	x	0	9h	1 (0*13)
-	-	✓	✓	-	✓	1	x	0	Eh (0h*12)	1 (0*13)
-	-	✓	-	✓	✓	1	x	1	Eh (0h*12	1 (0*13)
-	-	-	✓	-	✓	1	x	0	Eh (0h*12	0
-	-	-	-	✓	✓	1	x	1	Eh (0h*12	0

：可用x：无关注1.端口：P000至P007可用作端口输入。

注2.IRQ：P000至P002和P003至P005可用作IRQ引脚。
注3.SH：采样保持电路。
注4.PGA-S：当PGA设置为差分输入禁用时。对应的PGAVSS必须设置为ASEL为1，

and connect to AVSS0.

Note 5. PGA-D: When the PGA setting is Differential input enabled. Corresponding PGAVSS must set as ASEL to 1.

Note 6. P0nPFS: Port 0 Pin Function Select register (n = 00 to 07) corresponding to analog input pin.

Note 7. It indicates the corresponding Differential Input Enable bit (bit [11] or bit [7] or bit [3]) in the ADPGADCR0 register.

Note 8. It indicates the corresponding Amplifier Control bits (bits [11:8] or bits [7:4], or bits [3:0]) in the ADPGACR register.

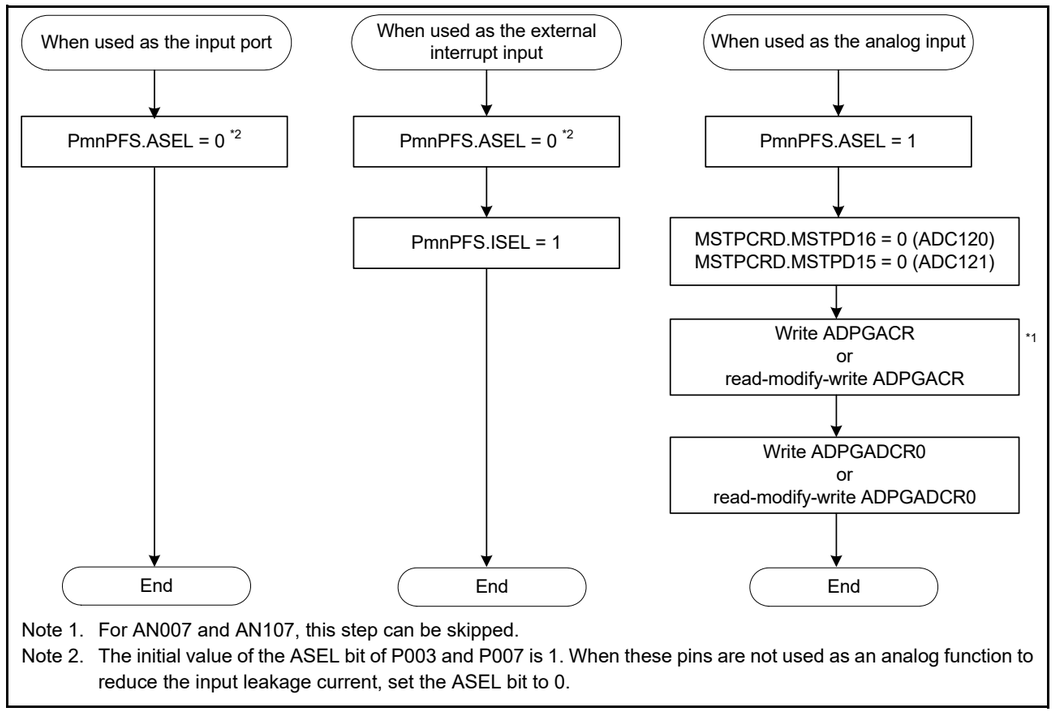
Note 9. It indicates the corresponding Bypass Select bit (bit [10] or bit [9] or bit [8]) in ADSHCR register.

Note 10. When using AN000 to AN002 or AN100 to AN102.

Note 11. When using AN007 or AN107. Set all corresponding bits (ADPGADCR0 bit [11], bit [7], and bit [3] to 0.

Note 12. Power consumption of the PGA can be reduced by setting 0h to the corresponding bit of the ADPGACR register before transitioning to the ADC12 module-stop state or Software Standby mode.

Note 13. Power consumption of the S/H can be reduced by setting 0 to the corresponding bit of the ADSHCR register before transitioning to the ADC12 module-stop state or Software Standby mode.



Note 1. For AN007 and AN107, this step can be skipped.

Note 2. The initial value of the ASEL bit of P003 and P007 is 1. When these pins are not used as an analog function to reduce the input leakage current, set the ASEL bit to 0.

Figure 47.41 Setting procedure of registers

47.6.9 Constraints on Operating Modes and Status Bits

The voltage values in self-diagnosis, the determination of first or second scan in double-trigger mode, and the data buffer pointer and status monitor in the compare function initialize or set it again individually, if required.

- The voltage values in self-diagnosis can be selected in ADCER.DIAGVAL[1:0] after ADCER.DIAGLD is set to 1.
- The double-trigger mode operates as the first scan after ADCSR.DBLE is set to 1 from 0.
- The status monitor bits (MONCMPA, MONCMPB, and MONCOMB) in the compare function are initialized after ADCMPCR.CMPAE and ADCMPCR.CMPBE are cleared to 0.
- The constant sampling function (ADSHMSR.SHMD = 1) is initialized after ADSHMSR.SHMD is cleared to 0. When the constant sampling function is used (setting ADSHMSR.SHMD = 1) again, a wait of 1ADCLK or more waiting is required.

并连接到AVSS0。注5.PGA-D：当PGA设置为差分输入时。对应的PGAVSS必须设置为ASEL为1。

注6.P0nPFS：端口0引脚功能选择寄存器（n=00至07）对应于模拟输入引脚。

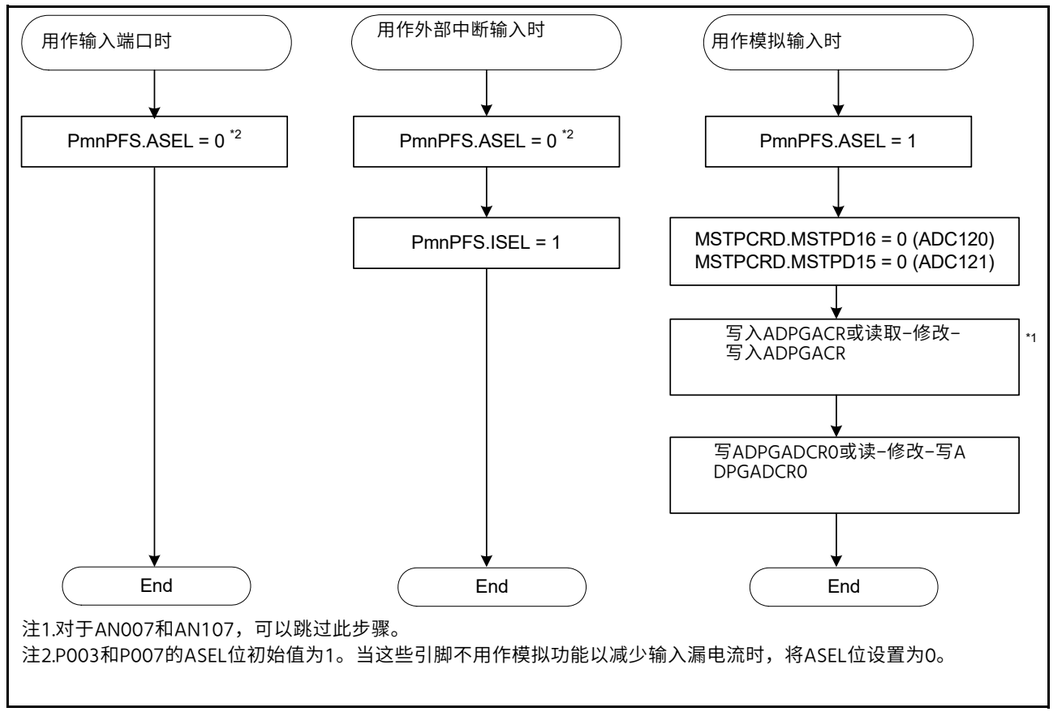
注7.它表示ADPADCR0寄存器中相应的差分输入使能位（位[11]或位[7]或位[3]）。

注8：它表示ADPGACR寄存器中相应的放大器控制位（位[11:8]或位[7:4]或位[3:0]）。注9.它表示ADSHCR寄存器中对应的BypassSelect位（bit[10]或bit[9]或bit[8]）。

注10.使用AN000至AN002或AN100至AN102时。

注11.使用AN007或AN107时。将所有相应位（ADPGADCR0位[11]、位[7]和位[3]）设置为0。

注12.在转换到ADC12模块停止状态或软件待机模式之前，可以通过将ADPGACR寄存器的相应位设置为0h来降低PGA的功耗。注13.在转换到ADC12模块停止状态或软件待机模式之前，可以通过将ADSHCR寄存器的相应位设置为0来降低SH的功耗。



注1.对于AN007和AN107，可以跳过此步骤。

注2.P003和P007的ASEL位初始值为1。当这些引脚不用作模拟功能以减少输入漏电流时，将ASEL位设置为0。

Figure 47.41 寄存器的设置步骤

47.6.9 操作模式和状态位的限制

如果需要，自诊断中的电压值、双触发模式下第一次或第二次扫描的确定以及比较功能中的数据缓冲区指针和状态监视器会单独初始化或重新设置。

- ADCER.DIAGLD设置为1后，可以在ADCER.DIAGVAL[1:0]中选择自诊断中的电压值。
- 双触发模式作为ADCSR.DBLE从0设置为1后的第一次扫描运行。
- 比较函数中的状态监控位（MONCMPA、MONCMPB和MONCOMB）在之后初始化ADCMPCR.CMPAE和ADCMPCR.CMPBE清零。
- 在ADSHMSR.SHMD清零后初始化恒定采样函数(ADSHMSR.SHMD=1)。
  当再次使用恒定采样功能（设置ADSHMSR.SHMD=1）时，需要等待1ADCLK或更多等待。

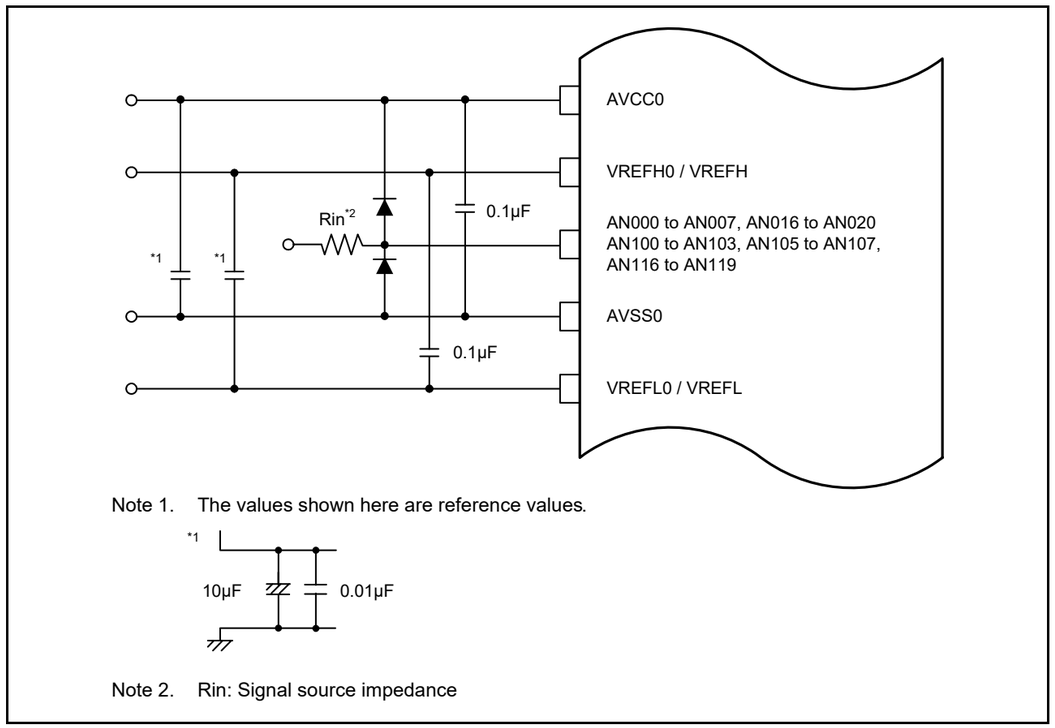
47.6.10 Notes on Board Design

The board should be designed so that digital circuits and analog circuits are separated from each other as far as possible.

In addition, digital circuit signal lines and analog circuit signal lines should not intersect or placed near each other. If these rules are not followed, noise will be produced on analog signals and A/D conversion accuracy will be affected. The analog input pins (AN000 to AN007, AN016 to AN020, AN100 to AN103, AN105 to AN107, AN116 to AN119), reference power supply pin (VREFH0/VREFH), reference ground pin (VREFL0/VREFL), and analog power supply (AVCC0) should be separated from digital circuits using the analog ground (AVSS0). The analog ground (AVSS0) should be connected to a stable digital ground (VSS) on the board (single-point ground plane connection).

47.6.11 Constraints on Noise Prevention

To prevent the analog input pins (AN000 to AN007, AN016 to AN020, AN100 to AN103, AN105 to AN107, and AN116 to AN119) from being destroyed by abnormal voltage such as excessive surges, insert a capacitor between AVCC0 and AVSS0, between VREFH0 and VREFL0, and between VREFH and VREFL, and connect a protection circuit to protect the analog input pins (AN000 to AN007, AN016 to AN020, AN100 to AN103, AN105 to AN107, and AN116 to AN119) as shown Figure 47.42.



Note 1. The values shown here are reference values.

Note 2. Rin: Signal source impedance

Figure 47.42 Example protection circuit for analog inputs

47.6.12 Port Settings When Using the ADC12 Input

When using the high-precision channels, do not use ports 0 as digital output ports. Renesas also recommends not using the digital output that is also used as the A/D analog input, if normal-precision channels is used. If the digital output that is also used as the A/D analog input is used for output signals, perform A/D conversion several times, eliminate the maximum and minimum values, and obtain the average of the other results.

47.6.13 Relationship between ADC12 Units 0 and 1 and the ACMPHS

For the A/D conversion targets in Table 47.15, unit 0 and 1 should not perform A/D conversion at the same time.

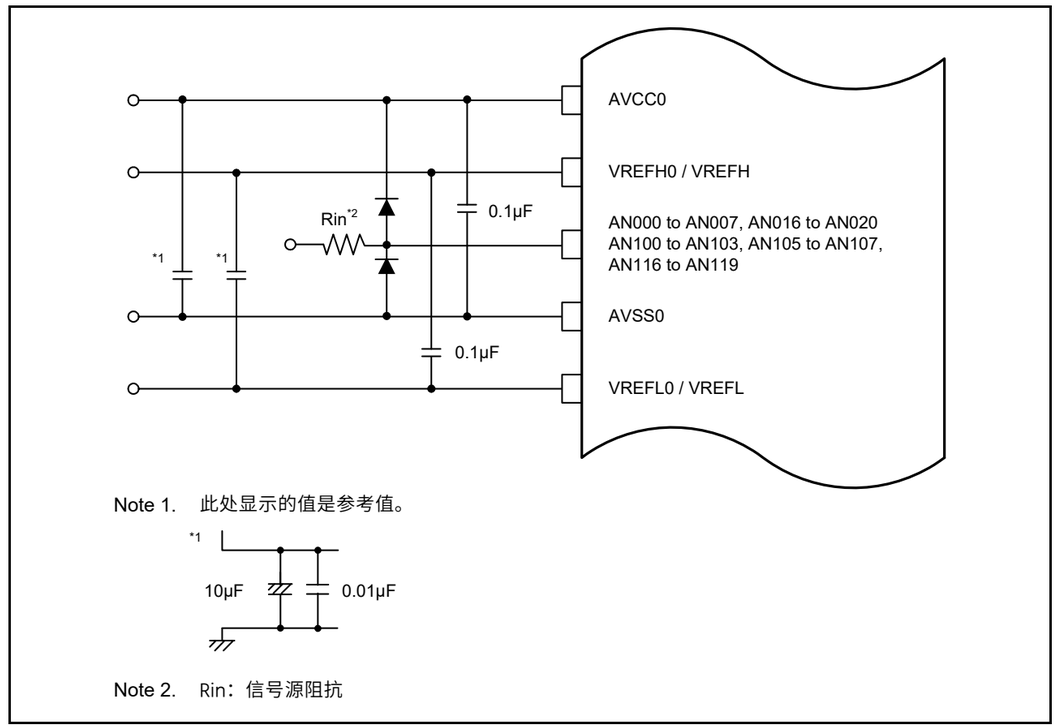
47.6.10 电路板设计注意事项

电路板的设计应使数字电路和模拟电路尽可能分开。

此外，数字电路信号线和模拟电路信号线不应交叉或靠近。如果不遵守这些规则，模拟信号就会产生噪声，影响AD转换精度。模拟输入引脚（AN000至AN007、AN016至AN020、AN100至AN103、AN105至AN107、AN116至AN119）、参考电源引脚（VREFH0VREFH）、参考接地引脚（VREFL0VREFL）和模拟电源（AVCC0）应使用模拟地(AVSS0)与数字电路分开。模拟接地(AVSS0)应连接到板上的稳定数字接地(VSS)（单点接地层连接）。

47.6.11 防止噪音的限制

为防止模拟输入引脚（AN000至AN007、AN016至AN020、AN100至AN103、AN105至AN107和AN116至AN119）被异常电压（如过大浪涌）破坏，请在AVCC0和AVSS0之间、VREFH0和VREFL0和VREFH和VREFL之间，并连接保护电路以保护模拟输入引脚（AN000到AN007、AN016到AN020、AN100到AN103、AN105到AN107和AN116到AN119），如图47.42所示。



Note 1. 此处显示的值是参考值。

Note 2. Rin：信号源阻抗

Figure 47.42 模拟输入保护电路示例

47.6.12 使用ADC12输入时的端口设置

使用高精度通道时，请勿将端口0用作数字输出端口。如果使用标准精度通道，瑞萨还建议不要使用也用作AD模拟输入的数字输出。如果将同时用作AD模拟输入的数字输出用于输出信号，则进行几次AD转换，消除最大值和最小值，取其他结果的平均值。

47.6.13 ADC12单元0和1与ACMPHS之间的关系

对于表47.15中的AD转换目标，单元0和单元1不应同时进行AD转换。

Table 47.15 A/D conversion targets that are mutually exclusive with each other

A/D conversion target	
Unit 0	**Unit 1**
Temperature sensor	
Internal reference voltage	
AN005/DA0	AN105/DA0
AN006/DA1	AN106/DA1

The A/D conversion targets in Table 47.16 should not be selected as ACMPHS input during A/D conversion, because these pins are multiplexed with the ADC12 and ACMPHS.

Table 47.16 A/D conversion targets that are mutually exclusive with ACMPHS

A/D conversion target		
Unit 0	**Unit 1**	**ACMPHS**
AN000	-	ACMPHS0.IVCMP2
AN001	-	ACMPHS1.IVCMP2
AN002	-	ACMPHS2.IVCMP2
PGA P000 output	-	ACMPHS0.IVCMP3
PGA P001 output	-	ACMPHS1.IVCMP3
PGA P002 output	-	ACMPHS2.IVCMP3
AN005/DA0	-	ACMPHS0 to ACMPHS5.IVREF3
AN006/DA1	-	ACMPHS0 to ACMPHS5.IVCMP1
AN016	-	ACMPHS0 to ACMPHS5.IVREF0
AN017	-	ACMPHS0 to ACMPHS5.IVCMP0
Internal reference voltage	-	ACMPHS0 to ACMPHS5.IVREF2
-	AN100	ACMPHS3.IVCMP2
-	AN101	ACMPHS4.IVCMP2
-	AN102	ACMPHS5.IVCMP2
-	PGA P000 output	ACMPHS3.IVCMP3
-	PGA P001 output	ACMPHS4.IVCMP3
-	PGA P002 output	ACMPHS5.IVCMP3
-	AN105/DA0	ACMPHS3 to ACMPHS5.IVREF3
-	AN106/DA1	ACMPHS3 to ACMPHS5.IVCMP1
-	AN116	ACMPHS0 to ACMPHS5.IVREF1
-	Internal reference voltage	ACMPHS0 to ACMPHS5.IVREF2

Table 47.15 相互排斥的AD转换目标

AD转换目标	
Unit 0	**Unit 1**
温度感应器	
内部参考电压	
AN005/DA0	AN105/DA0
AN006/DA1	AN106/DA1

在AD转换期间，不应选择表47.16中的AD转换目标作为ACMPHS输入，因为这些引脚与ADC12和ACMPHS复用。

Table 47.16 与ACMPHS互斥的D转换目标

AD转换目标		
Unit 0	**Unit 1**	**ACMPHS**
AN000	-	ACMPHS0.IVCMP2
AN001	-	ACMPHS1.IVCMP2
AN002	-	ACMPHS2.IVCMP2
PGAP000输出	-	ACMPHS0.IVCMP3
PGAP001输出	-	ACMPHS1.IVCMP3
PGAP002输出	-	ACMPHS2.IVCMP3
AN005/DA0	-	ACMPHS0 to ACMPHS5.IVREF3
AN006/DA1	-	ACMPHS0 to ACMPHS5.IVCMP1
AN016	-	ACMPHS0 to ACMPHS5.IVREF0
AN017	-	ACMPHS0 to ACMPHS5.IVCMP0
内部参考电压	-	ACMPHS0 to ACMPHS5.IVREF2
-	AN100	ACMPHS3.IVCMP2
-	AN101	ACMPHS4.IVCMP2
-	AN102	ACMPHS5.IVCMP2
-	PGAP000输出	ACMPHS3.IVCMP3
-	PGAP001输出	ACMPHS4.IVCMP3
-	PGAP002输出	ACMPHS5.IVCMP3
-	AN105/DA0	ACMPHS3 to ACMPHS5.IVREF3
-	AN106/DA1	ACMPHS3 to ACMPHS5.IVCMP1
-	AN116	ACMPHS0 to ACMPHS5.IVREF1
-	内部参考电压	ACMPHS0 to ACMPHS5.IVREF2

48. 12-Bit D/A Converter (DAC12)

48.1 Overview

The MCU provides a 12-Bit D/A Converter (DAC12) with an output amplifier. Table 48.1 lists the DAC12 specifications, Figure 48.1 shows a block diagram, and Table 48.2 lists the I/O pins.

Table 48.1 DAC12 specifications

Parameter	Specifications
Resolution	12 bits
Output channels	2 channels
Interference reduction between analog modules	Methods provided to minimize interference between D/A and A/D conversion: • D/A converted data update timing is controlled by the ADC12 synchronous D/A conversion enable input signal from the ADC12 (unit 1) • Degradation of A/D conversion accuracy caused by interference is reduced by controlling DAC12 inrush current generation timing with the enable signal
Module-stop function	Module-stop state can be set to reduce power consumption
Event link function (input)	DA0 and DA1 conversion can be started when an event signal is input
D/A output amplifier control function	Controls whether the output amplifier (for both amplifier-through and amplifier-bias controls) is used

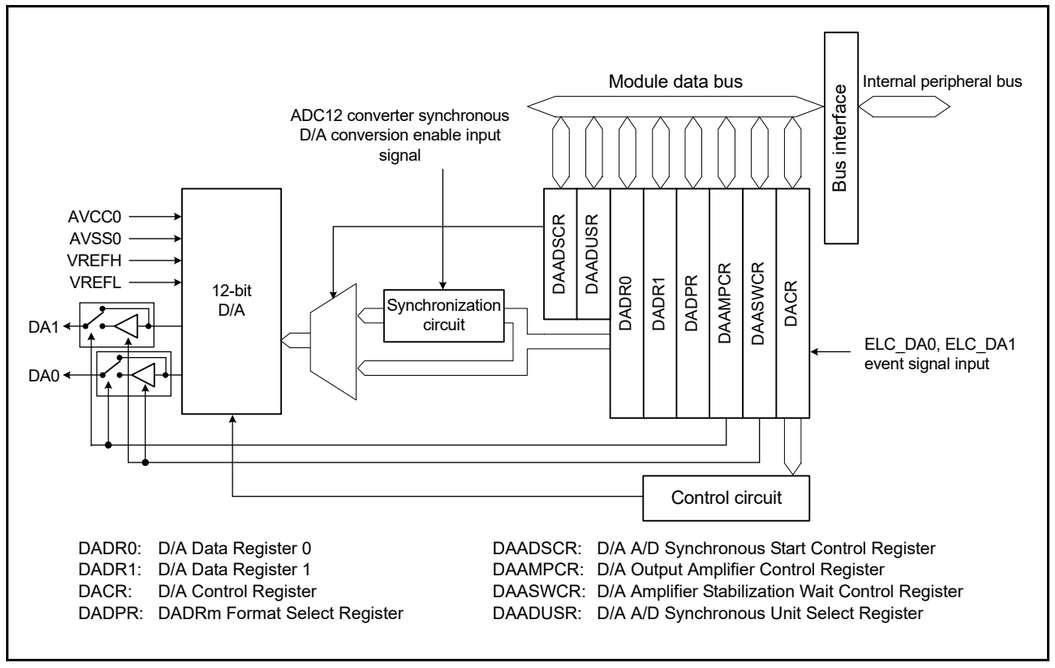


Figure 48.1 DAC12 block diagram

Table 48.2 DAC12 I/O pins (1 of 2)

Pin name	I/O	Function
AVCC0	Input	Analog power supply pin for ADC12, DAC12, and comparator Connect to VCC when these modules are not used.
AVSS0	Input	Analog ground pin for ADC12, DAC12, and comparator Connect to VSS when these modules are not used.

48. 12-Bit D/A Converter (DAC12)

48.1 Overview

MCU提供带输出放大器的12位DA转换器(DAC12)。表48.1列出了DAC12规格，图48.1显示了框图，表48.2列出了IO引脚。

Table 48.1 DAC12 specifications

Parameter	Specifications
Resolution	12 bits
输出通道	2 channels
减少模拟模块之间的干扰	为尽量减少DA和AD转换之间的干扰提供的方法： DA转换数据更新时序由来自ADC12（单元1）的ADC12同步DA转换使能输入信号控制 通过控制DAC12浪涌来减少由干扰引起的AD转换精度下降使能信号的电流产生时序
Module-stop function	可设置模块停止状态以降低功耗
事件链接功能（输入）	输入事件信号时可启动DA0和DA1转换
DA输出放大器控制功能	控制是否使用输出放大器（用于放大器直通和放大器偏置控制）

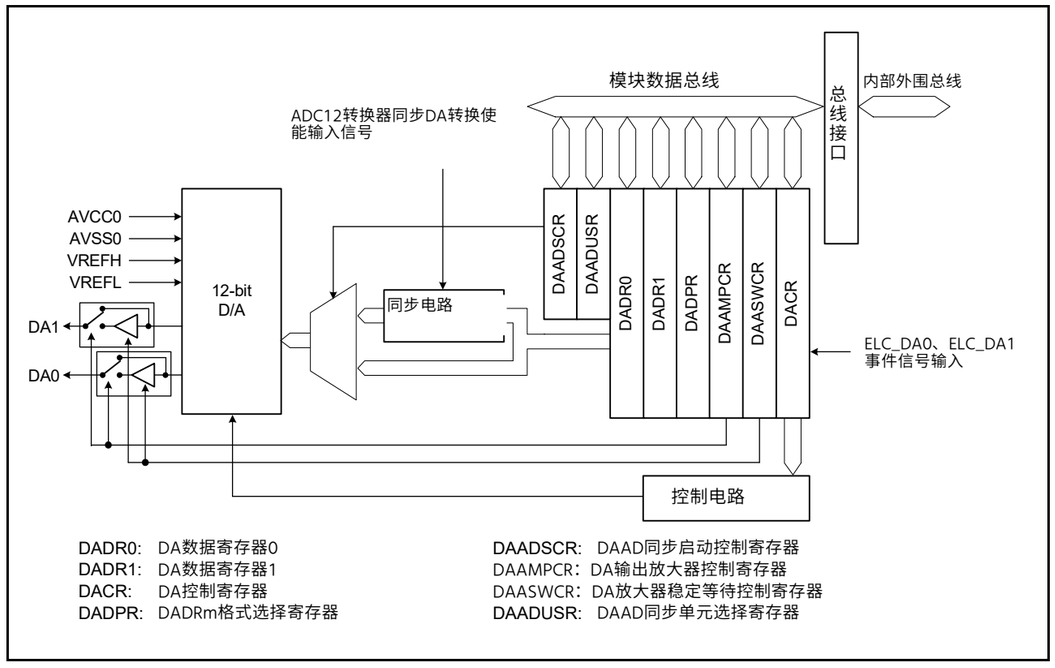


Figure 48.1 DAC12框图

Table 48.2 DAC12IO引脚（2个中的1个）

引脚名称	I/O	Function
AVCC0	Input	ADC12、DAC12和比较器的模拟电源引脚 不使用这些模块时连接到VCC。
AVSS0	Input	ADC12、DAC12和比较器的模拟接地引脚 不使用这些模块时连接到VSS。

Table 48.2 DAC12 I/O pins (2 of 2)

Pin name	I/O	Function
VREFH	Input	Analog reference top voltage supply pin for the ADC12 (unit 1) and the DAC12
VREFL	Input	Analog reference ground pin for the ADC12 (unit 1) and the DAC12
DA0	Output	Channel 0 analog output pin
DA1	Output	Channel 1 analog output pin

48.2 Register Descriptions

48.2.1 D/A Data Register m (DADRm) (m = 0, 1)

Address(es): DAC12.DADR0 4005 E000h, DAC12.DADR1 4005 E002h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DADRm registers are 16-bit read/write registers that store data for D/A conversion. Whenever an analog output is enabled, the values in DADRm are converted and output to the analog output pins.

12-bit data can be formatted as left- or right-justified in the DADPR.DPSEL bit setting. In right-justified format (DADPR.DPSEL = 0), the lower 12 bits, [11:0], are valid. In left-justified format (DADPR.DPSEL = 1), the upper 12 bits, [15:4], are valid.

For information on using the output amplifier, see section 48.6.5, Initialization Procedure with the Output Amplifier.

48.2.2 D/A Control Register (DACR)

Address(es): DAC12.DACR 4005 E004h

	b7	b6	b5	b4	b3	b2	b1	b0
	DAOE1	DAOE0	DAE	—	—	—	—	—
Value after reset:	0	0	0	1	1	1	1	1

Bit	Symbol	Bit name	Description	R/W
b4 to b0	—	Reserved	These bits are read as 1. The write value should be 1.	R/W
b5	DAE	D/A Enable*1	0: Control D/A conversion of channels 0 and 1 individually 1: Control D/A conversion of channels 0 and 1 collectively.	R/W
b6	DAOE0	D/A Output Enable 0	0: Disable analog output of channel 0 (DA0) 1: Enable D/A conversion of channel 0 (DA0).	R/W
b7	DAOE1	D/A Output Enable 1	0: Disable analog output of channel 1 (DA1) 1: Enable D/A conversion of channel 1 (DA1).	R/W

Note 1. This bit controls D/A conversion in combination with the DAOEi bit (i = 0, 1), which controls output of the conversion results. For details, see Table 48.3.

Table 48.2 DAC12IO引脚（2个中的2个）

引脚名称	I/O	Function
VREFH	Input	ADC12（单元1）和DAC12的模拟参考最高电压电源引脚
VREFL	Input	ADC12（单元1）和DAC12的模拟参考接地引脚
DA0	Output	通道0模拟输出引脚
DA1	Output	通道1模拟输出引脚

48.2 注册说明

48.2.1 DA数据寄存器m(DADRm)(m=0 1)

Address(es): DAC12.DADR0 4005 E000h, DAC12.DADR1 4005 E002h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DADRm寄存器是16位读写寄存器，用于存储用于DA转换的数据。每当启用模拟输出时，DADRm中的值都会被转换并输出到模拟输出引脚。

在DADPR.DPSEL位设置中，12位数据可以被格式化为左对齐或右对齐。在右对齐格式(DADPR.DPSEL=0)中，低12位[11:0]有效。在左对齐格式(DADPR.DPSEL=1)中，高12位[15:4]有效。

有关使用输出放大器的信息，请参阅第48.6.5节，使用输出放大器的初始化过程。

48.2.2 DA控制寄存器(DACR)

Address(es): DAC12.DACR 4005 E004h

	b7	b6	b5	b4	b3	b2	b1	b0
	DAOE1	DAOE0	DAE	—	—	—	—	—
重置后的值：	0	0	0	1	1	1	1	1

Bit	Symbol	位名称	Description	R/W
b4 to b0	—	Reserved	这些位被读取为1。写入值应为1。	R/W
b5	DAE	D/A Enable*1	0：分别控制通道0和1的DA转换1：控制通道0和1的DA转换。	R/W
b6	DAOE0	DA输出使能0	0：禁用通道0（DA0）的模拟输出1：启用通道0（DA0）的DA转换。	R/W
b7	DAOE1	DA输出使能1	0：禁用通道1（DA1）的模拟输出1：启用通道1（DA1）的DA转换。	R/W

Note 1. 该位与控制转换结果输出的DAOEi位(i=0 1)一起控制DA转换。详见表48.3。

Table 48.3 D/A conversion controls

b5	b7	b6	
DAE	DAOE1	DAOE0	Description
0	0	0	Disable D/A conversion and analog output pins (DA0, DA1)*1
		1	• Enable D/A conversion of channel 0 and disable D/A conversion of channel 1 • Enable analog output of channel 0 (DA0) and disable analog output of channel 1 (DA1)*1
	1	0	• Disable D/A conversion of channel 0 and enable D/A conversion of channel 1 • Disable analog output of channel 0 (DA0)*1 and enable analog output of channel 1 (DA1)
		1	• Enable D/A conversion of channels 0 and 1 • Enable analog output of channels 0 and 1 (DA0, DA1)
1	x	x	• Enable D/A conversion of channels 0 and 1 • Collective enable analog output of channels 0 and 1 (DA0, DA1)

x: Don't care

Note 1. When analog output is disabled, the analog output signal is placed in the Hi-Z state.

Only set this register while the ADC12 is halted when the DAADSCR.DAADST bit is 1 (interference reduction between D/A and A/D conversion is enabled). Only set DACR while the ADCSR.ADST bit is 0 and after selecting the software trigger, for the ADC12 trigger to securely stop the ADC12. This MCU only supports ADC12 unit 1.

DAE bit (D/A Enable)

The DAE bit controls D/A conversion, amplifier operation, and analog output in combination with the DAOEi bit (i = 0, 1) and the DAMMPCR.DAAMPi bit (i = 0, 1). See Table 48.4.

When interference prevention between D/A and A/D conversions is enabled (DAADSCR.DAADST = 1), set the ADCSR.ADST bit of the ADC12 (unit 1) to 0. Then select the software trigger for the ADC12 (unit 1) trigger to securely stop the ADC12 (unit 1).

DAOEi bit (D/A Output Enable i)

The DAOEi bit (i = 0, 1) controls D/A conversion, amplifier operation, and analog output in combination with the DAE bit and DAMMPCR.DAAMPi bit (i = 0, 1). See Table 48.4.

When both the DAOEi bit (i = 0, 1) and DAE bit are 0, D/A conversion of channel i (i = 0, 1) is not processed, and no conversion result is output.

When interference prevention between D/A and A/D conversions is enabled (DAADSCR.DAADST = 1), set the DAOEi bit while the ADCSR.ADST bit of the ADC12 (unit 1) is set to 0. Then select the software trigger for the ADC12 (unit 1) trigger to securely stop the ADC12 (unit 1).

The event link function can be used to set the DAOEi bit to 1. The DAOE0 bit sets to 1 when the event specified in the ELSR12 register of the ELC (ELC_DA0 event) occurs, and output of the D/A conversion results starts. The DAOE1 bit sets to 1 when the event specified in the ELSR13 register of the ELC (ELC_DA1 event) occurs, and output of the D/A conversion results starts.

Table 48.4 D/A conversion and analog output control (1 of 2)

DACR		DAAMPCR			
DAE	DAOEi	DAAMPi	Channel i operation	Amplifier operation of channel i	Analog output of channel i
0	0	0	Stop	Stop	Hi-Z
		1	Stop	Stop	Hi-Z
	1	0	Run	Stop	Amplifier-through
		1	Run	Run	Amplifier output

Table 48.3 DA转换控制

b5	b7	b6	
DAE	DAOE1	DAOE0	Description
0	0	0	禁用DA转换和模拟输出引脚（DA0、DA1）*1
		1	启用通道0的DA转换并禁用通道1的DA转换 启用通道0(DA0)的模拟输出并禁用通道1(DA1)的模拟输出*1
	1	0	禁用通道0的DA转换并启用通道1的DA转换 禁用通道0(DA0)*1的模拟输出并启用通道1(DA1)的模拟输出
		1	启用通道0和1的DA转换 启用通道0和1（DA0、DA1）的模拟输出
1	x	x	启用通道0和1的DA转换 集体启用通道0和1（DA0、DA1）的模拟输出

x: Don't care

Note 1. 禁用模拟输出时，模拟输出信号置于Hi-Z状态。

仅当DAADSCR.DAADST位为1（启用DA和AD转换之间的干扰减少）时ADC12停止时设置此寄存器。只有在ADCSR.ADST位为0且选择软件触发后设置DACR，ADC12触发才能安全停止ADC12。此MCU仅支持ADC12单元1。

DAE位（DA启用）

DAE位与DAOEi位(i=0 1)和DAMMPCR.DAAMPi位(i=0 1)一起控制DA转换、放大器操作和模拟输出。见表48.4。

当启用DA和AD转换之间的干扰防止(DAADSCR.DAADST=1)时，设置ADC12（单元1）的ADCSR.ADST位为0。然后选择ADC12（单元1）触发的软件触发，以安全地停止ADC12（单元1）。

DAOEi位（DA输出使能i）

DAOEi位(i=0 1)与DAE位和DAMMPCR.DAAMPi位(i=0 1)一起控制DA转换、放大器操作和模拟输出。见表48.4。

当DAOEi位(i=0 1)和DAE位均为0时，通道i(i=0 1)的DA转换不进行处理，也不输出转换结果。

当DA和AD转换之间的干扰防止启用时（DAADSCR.DAADST=1），设置DAOEi位同时ADC12（单元1）的ADCSR.ADST位设置为0。然后选择ADC12的软件触发（单元1)触发以安全地停止ADC12（单元1）。

事件链接功能可用于将DAOEi位设置为1。当ELC的ELSR12寄存器中指定的事件（ELC_DA0事件）发生时，DAOE0位设置为1，并开始输出DA转换结果。当ELC的ELSR13寄存器中指定的事件（ELC_DA1事件）发生时，DAOE1位设置为1，并开始输出DA转换结果。

Table 48.4 DA转换和模拟输出控制(1of2)

DACR		DAAMPCR			
DAE	DAOEi	DAAMPi	通道i操作	通道i的放大器操作	通道i的模拟输出
0	0	0	Stop	Stop	Hi-Z
		1	Stop	Stop	Hi-Z
	1	0	Run	Stop	Amplifier-through
		1	Run	Run	放大器输出

Table 48.4 D/A conversion and analog output control (2 of 2)

DACR		DAAMPCR			
DAE	DAOEi	DAAMPi	Channel i operation	Amplifier operation of channel i	Analog output of channel i
1	0	0	Run	Stop	Amplifier-through
		1	Run	Run	Amplifier output
	1	0	Run	Stop	Amplifier-through
		1	Run	Run	Amplifier output

i = 0, 1

48.2.3 DADRm Format Select Register (DADPR)

Address(es): DAC12.DADPR 4005 E005h

	b7	b6	b5	b4	b3	b2	b1	b0
	DPSEL	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b6 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	DPSEL	DADRm Format Select	0: Right-justified format 1: Left-justified format.	R/W

48.2.4 D/A A/D Synchronous Start Control Register (DAADSCR)

Address(es): DAC12.DAADSCR 4005 E006h

	b7	b6	b5	b4	b3	b2	b1	b0
	DAADST	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b6 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	DAADST	D/A A/D Synchronous Conversion	0: Do not synchronize DAC12 operation with ADC12 (unit 1) operation (disable interference prevention between D/A and A/D conversion) 1: Synchronize DAC12 operation with ADC12 (unit 1) operation (enable interference prevention between D/A and A/D conversion).	R/W

To minimize interference between D/A and A/D conversion, the DAADSCR register enables synchronization of the start timing of D/A conversion with the ADC12 synchronous D/A conversion enable input signal.

Only set this register while the ADC12 (unit 1) is halted, that is, while the ADCSR.ADST bit is 0 after selecting the software trigger as the ADC12 (unit 1) trigger.

Select unit 1 as the target ADC12 unit before setting the DAADST bit to 1.

Set bit [1] in the DAADUSR register to 1 to select unit 1. The MCU only supports ADC12 unit 1.

DAADST bit (D/A A/D Synchronous Conversion)

Setting the DAADST bit to 0 allows the DADRm register value to be converted into analog data at any time. Setting the DAADST bit to 1 allows synchronous D/A conversion with the ADC12 synchronous D/A conversion enable input signal from the ADC12 (unit 1). With this bit set, D/A conversion does not start until the ADC12 (unit 1) completes A/D conversion, even if the DADRm register value is changed.

Table 48.4 DA转换和模拟输出控制(2of2)

DACR		DAAMPCR			
DAE	DAOEi	DAAMPi	通道i操作	通道i的放大器操作	通道i的模拟输出
1	0	0	Run	Stop	Amplifier-through
		1	Run	Run	放大器输出
	1	0	Run	Stop	Amplifier-through
		1	Run	Run	放大器输出

i = 0, 1

48.2.3 DADRm格式选择寄存器(DADPR)

Address(es): DAC12.DADPR 4005 E005h

	b7	b6	b5	b4	b3	b2	b1	b0
	DPSEL	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b6 to b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b7	DPSEL	DADRm格式选择	0: Right-justified format 1: Left-justified format.	R/W

48.2.4 DAAD同步启动控制寄存器(DAADSCR)

Address(es): DAC12.DAADSCR 4005 E006h

	b7	b6	b5	b4	b3	b2	b1	b0
	DAADST	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b6 to b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b7	DAADST	D/A A/D Synchronous Conversion	0：不将DAC12操作与ADC12（单元1）操作同步（禁用DA和AD转换之间的防干扰）1：将DAC12操作与ADC12（单元1）操作同步（启用DA和AD转换之间的防干扰）。	R/W

为了尽量减少DA和AD转换之间的干扰，DAADSCR寄存器使DA转换的开始时序与ADC12同步DA转换使能输入信号同步。

仅在ADC12（单元1）停止时设置该寄存器，即选择软件触发作为ADC12（单元1）触发后ADCSR.ADST位为0。

在将DAADST位设置为1之前，选择单元1作为目标ADC12单元。

将DAADUSR寄存器中的位[1]设置为1以选择单元1。MCU仅支持ADC12单元1。

DAADST位（DAAD同步转换）

将DAADST位设置为0可以随时将DADRm寄存器值转换为模拟数据。将DAADST位设置为1允许使用来自ADC12（单元1）的ADC12同步DA转换使能输入信号进行同步DA转换。设置该位后，即使DADRm寄存器的值发生了变化，ADC12（单元1）完成AD转换后才开始DA转换。

Set this bit while the ADCSR.ADST bit is set to 0. Then select the software trigger for the ADC12 (unit 1) trigger to securely stop the ADC12 (unit 1). Set bit [1] in the DAADUSR register to 1 before setting the DAADST bit to 1.

The event link function cannot be used when the DAADST bit is set to 1. Stop the event link function by setting the ELSR12 and ELSR13 registers of the ELC. The setting of the DAADST bit is shared by channels 0 and 1 of the DAC12.

48.2.5 D/A Output Amplifier Control Register (DAAMPCR)

Address(es): DAC12.DAAMPCR 4005 E008h

	b7	b6	b5	b4	b3	b2	b1	b0
	DAAMP1	DAAMP0	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b5 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6	DAAMP0	Amplifier Control 0	0: Do not use channel 0 output amplifier 1: Use channel 0 output amplifier.	R/W
b7	DAAMP1	Amplifier Control 1	0: Do not use channel 1 output amplifier 1: Use channel 1 output amplifier.	R/W

The DAAMPCR register selects D/A output with or without using the amplifier.

DAAMP0 bit (Amplifier Control 0)

When the DAAMP0 bit is 0, analog values are output for D/A output of channel 0 without using the amplifier. When the DAAMP0 bit is 1, analog values are output for D/A output of channel 0 through the amplifier.

When both the DAE and DAOE0 bits are 0, the amplifier is not used regardless of the setting of the DAAMP0 bit. See Table 48.4 for details.

DAAMP1 bit (Amplifier Control 1)

When the DAAMP1 bit is 0, analog values are output for D/A output of channel 1 without using the amplifier. When the DAAMP1 bit is 1, analog values are output for D/A output of channel 1 through the amplifier.

When both the DAE and DAOE1 bits are 0, the amplifier is not used regardless of the setting of the DAAMP1 bit. See Table 48.4 for details.

48.2.6 D/A Amplifier Stabilization Wait Control Register (DAASWCR)

Address(es): DAC12.DAASWCR 4005 E01C

	b7	b6	b5	b4	b3	b2	b1	b0
	DAASW1	DAASW0	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b5 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b6	DAASW0	D/A Amplifier Stabilization Wait 0	0: Amplifier stabilization wait off (output) for channel 0 1: Amplifier stabilization wait on (high-Z) for channel 0.	R/W
b7	DAASW1	D/A Amplifier Stabilization Wait 1	0: Amplifier stabilization wait off (output) for channel 1 1: Amplifier stabilization wait on (high-Z) for channel 1.	R/W

The DAASWCR register controls D/A output with the output amplifier. This register is used in the initialization procedure to wait for stabilization of the D/A output amplifier. Each bit in DAASWCR should be set to 1 when both the

在ADCSR.ADST位设置为0时设置该位。然后为ADC12（单元1）触发器选择软件触发器以安全地停止ADC12（单元1）。在将DAADST位设置为1之前，将DAADUSR寄存器中的位[1]设置为1。

当DAADST位设置为1时，不能使用事件链接功能。通过设置ELC的ELSR12和ELSR13寄存器。DAADST位的设置由DAC12的通道0和1共享。

48.2.5 DA输出放大器控制寄存器(DAAMPCR)

Address(es): DAC12.DAAMPCR 4005 E008h

	b7	b6	b5	b4	b3	b2	b1	b0
	DAAMP1	DAAMP0	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b5 to b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b6	DAAMP0	放大器控制0	0：不使用通道0输出放大器1：使用通道0输出放大器。	R/W
b7	DAAMP1	放大器控制1	0：不使用通道1输出放大器1：使用通道1输出放大器。	R/W

DAAMPCR寄存器选择使用或不使用放大器的DA输出。

DAAMP0位（放大器控制0）

当DAAMP0位为0时，模拟值输出通道0的DA输出，而不使用放大器。当。。。的时候DAAMP0位为1，模拟值通过放大器输出通道0的DA输出。

当DAE和DAOE0位都为0时，无论DAAMP0位的设置如何，都不会使用放大器。看详细信息见表48.4。

DAAMP1位（放大器控制1）

当DAAMP1位为0时，模拟值输出通道1的DA输出，而不使用放大器。当。。。的时候DAAMP1位为1，模拟值通过放大器输出到通道1的DA输出。

当DAE和DAOE1位都为0时，无论DAAMP1位的设置如何，都不会使用放大器。看详细信息见表48.4。

48.2.6 DA放大器稳定等待控制寄存器(DAASWCR)

Address(es): DAC12.DAASWCR 4005 E01C

	b7	b6	b5	b4	b3	b2	b1	b0
	DAASW1	DAASW0	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b5 to b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b6	DAASW0	DA放大器稳定等待0	0：通道0的放大器稳定等待关闭（输出）1：通道0的放大器稳定等待打开（高阻态）。	R/W
b7	DAASW1	DA放大器稳定等待1	0：通道1的放大器稳定等待关闭（输出）1：通道1的放大器稳定等待打开（高阻态）。	R/W

DAASWCR寄存器通过输出放大器控制DA输出。该寄存器在初始化过程中用于等待DA输出放大器的稳定。DAASWCR中的每一位都应设置为1，当

DAE bit and the DAOEi (i = 0, 1) bit in the DACR register are 0. See section 48.6.5, Initialization Procedure with the Output Amplifier.

DAASW0 bit (D/A Amplifier Stabilization Wait 0)

Set the DAASW0 bit to 1 in the initialization procedure to wait for stabilization of the output amplifier of D/A channel 0. When DAASW0 is set to 1, D/A conversion operates, but the conversion result D/A is not output from channel 0. When the DAASW0 bit is 0, the stabilization wait time stops, and the D/A conversion result of channel 0 is output through the output amplifier.

DAASW1 bit (D/A Amplifier Stabilization Wait 1)

Set the DAASW1 bit to 1 in the initialization procedure to wait for stabilization of the output amplifier of D/A channel 1. When DAASW1 is set to 1, D/A conversion operates, but the conversion result D/A is not output from channel 1. When the DAASW1 bit is 0, the stabilization wait time stops, and the D/A conversion result of channel 1 is output through the output amplifier.

48.2.7 D/A A/D Synchronous Unit Select Register (DAADUSR)

Address(es): DAC12.DAADUSR 4005 F0C0h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	AMADSEL1	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b1	AMADSEL1	A/D Unit 1 Select	0: Do not select unit 1 1: Select unit 1.	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The DAADUSR register selects the target ADC12 unit for D/A and A/D synchronous conversions. Set bit [1] to 1 to select unit 1 as the target synchronous unit for the MCU. When setting the DAADSCR.DAADST bit to 1 for synchronous conversions, select the target unit in this register in advance.

Only set the DAADUSR register while the ADCSR.ADST bit of the ADC12 is set to 0 and the DAADSCR.DAADST bit is set to 0.

48.3 Operation

The DAC12 includes D/A conversion circuits for two channels, each of which can operate independently. When the DAOEn bit (n = 0, 1) in DACR is set to 1, DAC12 is enabled and the conversion result is output.

This following is an example of D/A conversion on channel 0. Figure 48.2 shows the timing of this operation.

To process D/A conversion on channel 0:

1. Set the data for D/A conversion in the DADPR.DPSEL bit and the DADR0 register.
2. Set the DACR.DAOE0 bit to 1 to start D/A conversion. The conversion result is output from the analog output pin DA0 after the conversion time tDCONV elapses. The conversion result continues to be output until DADR0 is written to again or the DAOE0 bit is cleared to 0. The output value (reference) is expressed by the following formula:

$$\frac{\text{Setting in DADRm}}{4096} \times \text{VREFH}$$

3. To start conversion again, write to DADR0 again. The conversion result is output after the conversion time tDCONV elapses.
When the DAADSCR.DAADST bit is 1 (interference prevention between D/A and A/D conversion is enabled), a

DACR寄存器中的DAE位和DAOEi(i=0 1)位为0。请参见第48.6.5节，使用
输出放大器。

DAASW0位（DA放大器稳定等待0）

在初始化过程中将DAASW0位设置为1，等待DA通道0的输出放大器稳定。当DAASW0设置为1时，DA转换操作，但转换结果DA不从通道0输出。当DAASW0位为0，稳定等待时间停止，通道0的数模转换结果通过输出放大器输出。

DAASW1位（DA放大器稳定等待1）

在初始化过程中将DAASW1位设置为1，等待DA通道1的输出放大器稳定。当DAASW1设置为1时，DA转换操作，但转换结果DA不从通道1输出。当DAASW1位为0，稳定等待时间停止，通道1的DA转换结果通过输出放大器输出。

48.2.7 DAAD同步单元选择寄存器(DAADUSR)

Address(es): DAC12.DAADUSR 4005 F0C0h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	AMADSEL1	—
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	—	Reserved	该位读取为0。写入值应为0。	R/W
b1	AMADSEL1	AD单元1选择	0：不选择单元11： 选择单元1。	R/W
b7 to b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W

DAADUSR寄存器为DA和AD同步转换选择目标ADC12单元。将位[1]设置为1以选择单元1作为MCU的目标同步单元。将DAADSCR.DAADST位设置为1以进行同步转换时，请预先在该寄存器中选择目标单位。

仅在ADC12的ADCSR.ADST位设置为0且DAADSCR.DAADST位设置为0时设置DAADUSR寄存器。

48.3 Operation

DAC12包含两个通道的DA转换电路，每个通道都可以独立工作。当。。。的时候
DACR中的DAOEn位(n=0 1)设置为1，使能DAC12并输出转换结果。

以下是通道0上的DA转换示例。图48.2显示了此操作的时序。

在通道0上处理DA转换：

1. 在DADPR.DPSEL位和DADR0寄存器中设置用于DA转换的数据。
2. 将DACR.DAOE0位设置为1以启动DA转换。转换结果从模拟输出引脚输出
转换时间tDCONV过后的DA0。转换结果继续输出，直到再次写入DADR0或DAOE0位清0。输出值（参考值）由以下公式表示：

$$\frac{\text{DADRm4096中的设置}}{} \times \text{VREFH}$$

3. 要再次开始转换，请再次写入DADR0。经过转换时间tDCONV后输出转换结果。当DAADSCR.DAADST位为1（启用DA和AD转换之间的干扰防止）时，a

maximum of one A/D conversion time is required for D/A conversion to start. When ADCLK is faster than the peripheral clock, a longer time period might be required.

4. To disable analog output, set the DAOE0 bit to 0.

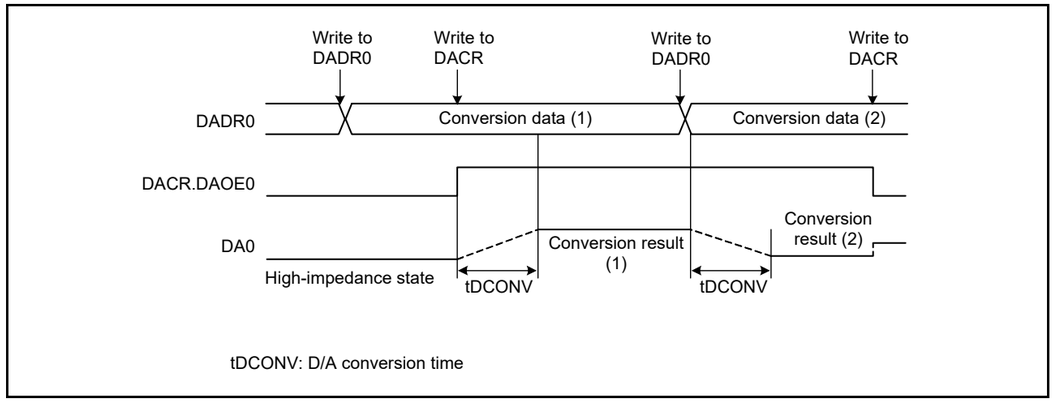


Figure 48.2 Example of DAC12 operation

48.3.1 Reducing Interference between D/A and A/D Conversion

When D/A conversion starts, the DAC12 generates inrush current. Because the same analog power supply is shared by the DAC12 and ADC12 (unit 1), the generated inrush current might interfere with ADC12 (unit 1) operation.

While the DAADSCR.DAADST bit is 1, even if the DADRm register data is changed during ADC12 (unit 1) operation, D/A conversion does not start immediately but starts synchronously with A/D conversion completion. A maximum of one A/D conversion time is required for the DADRm register data update to be reflected as the D/A conversion circuit input. Before reflection, the DADRm register value does not correspond to the analog output value.

When this function is enabled, it is impossible to check by any software means whether the DADRm register value was D/A converted. When the DADRm register data is changed while the ADC12 (unit 1) is halted, D/A conversion starts in 1 PCLKB cycle, even if DAADSCR.DAADST is 1.

The following sequence provides an example of channel 0 D/A conversion, in which the DAC12 operates synchronously with the ADC12 (unit 1).

To process D/A conversion on channel 0 in synchronization with the ADC12 (unit 1):

1. Confirm that the ADC12 (unit 1) is halted and set the DAADUSR.AMADSEL1 bit to 1.
2. Confirm that the ADC12 (unit 1) is halted and set the DAADSCR.DAADST bit to 1.
3. Confirm that the ADC12 (unit 1) is halted and set the DACR.DAOE0 bit to 1.
4. Set the DADR0 register. When ADCLK is faster than the peripheral clock, a period longer than one A/D conversion time might be required.

- If the 12-bit A/D conversion is halted (ADCSR.ADST bit = 0) when the DADR0 register is changed, D/A conversion starts in 1 PCLKB cycle.
- If the 12-bit A/D conversion is in progress (ADCSR.ADST bit = 1) when the DADR0 register is changed, D/A conversion starts on A/D conversion completion. If the DADR0 register is changed twice during A/D conversion, the first update might not be converted.

DA转换开始最多需要一个AD转换时间。当ADCLK比外设时钟快时，可能需要更长的时间周期。

4. 要禁用模拟输出，请将DAOE0位设置为0。

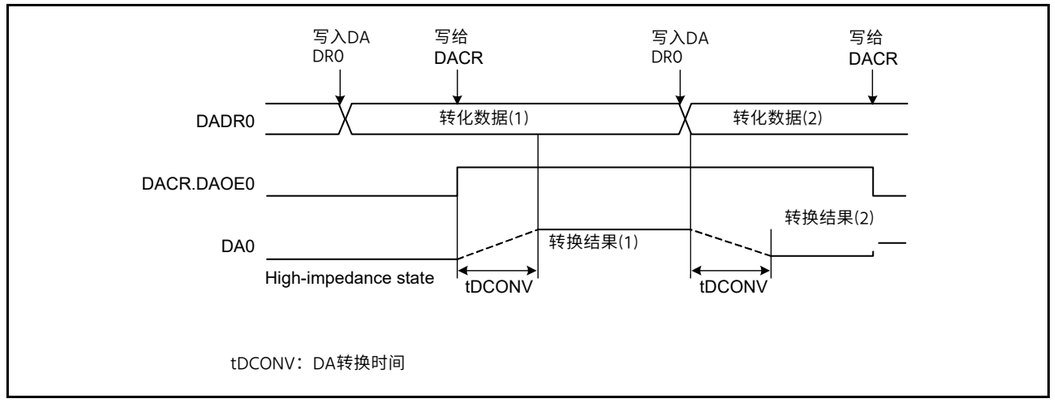


Figure 48.2 DAC12操作示例

48.3.1 减少DA和AD转换之间的干扰

当DA转换开始时，DAC12会产生浪涌电流。由于DAC12和ADC12（单元1）共享相同的模拟电源，所产生的浪涌电流可能会干扰ADC12（单元1）的运行。

当DAADSCR.DAADST位为1时，即使DADRm寄存器数据在ADC12（单元1）操作期间发生变化，DA转换不会立即开始，而是与AD转换完成同步开始。DADRm寄存器数据更新最多需要一个AD转换时间才能反映为DA转换电路输入。反射前，DADRm寄存器值与模拟输出值不对应。

当此功能使能时，任何软件都无法检查DADRm寄存器的值是否经过DA转换。如果在ADC12（单元1）停止时更改DADRm寄存器数据，即使DAADSCR.DAADST为1，DA转换也会在1个PCLKB周期内开始。

以下序列提供了通道0DA转换的示例，其中DAC12与ADC12（单元1）同步运行。

与ADC12（单元1）同步处理通道0上的DA转换：

1. 确认ADC12（单元1）已停止并将DAADUSR.AMADSEL1位设置为1。
2. 确认ADC12（单元1）已停止并将DAADSCR.DAADST位设置为1。
3. 确认ADC12（单元1）已停止并将DACR.DAOE0位设置为1。
4. 设置DADR0寄存器。当ADCLK比外设时钟快时，可能需要比一个AD转换时间更长的周期。

- 如果在DADR0寄存器更改时停止12位AD转换（ADCSR.ADST位=0），则DA转换在1个PCLKB周期内开始。
- 如果DADR0寄存器更改时12位AD转换正在进行（ADCSR.ADST位=1），则DA转换在AD转换完成时开始。如果在AD转换期间DADR0寄存器被更改两次，第一次更新可能不会被转换。

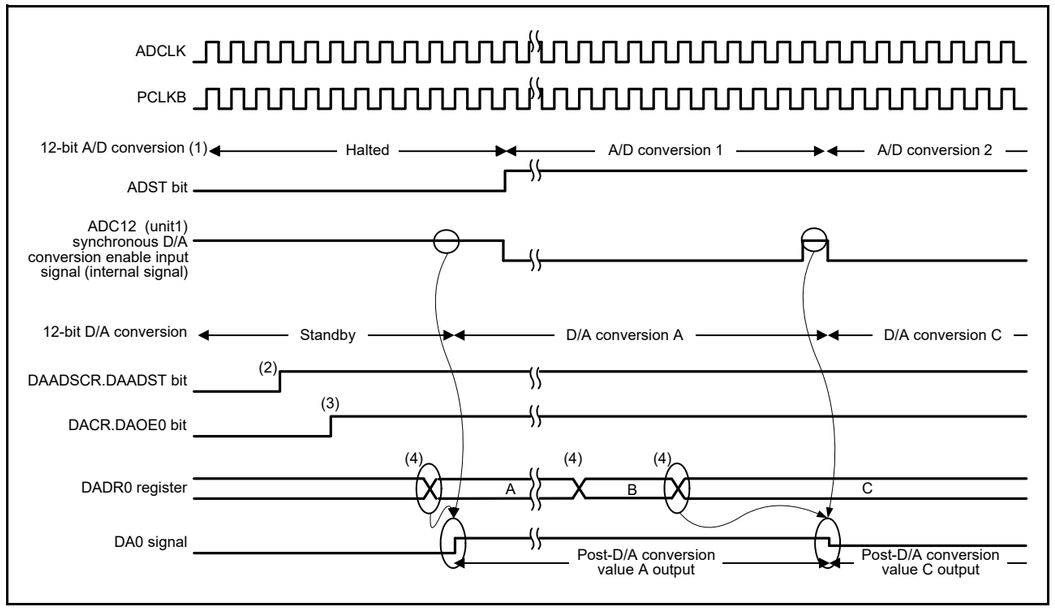


Figure 48.3 Example of conversion when the DAC12 is synchronized with the ADC12

When ADCLK is faster than PCLKB, the DAC12 might not be able to capture an ADC12 (unit 1) synchronous D/A conversion enable input signal for the 1 ADCLK cycle that is output between A/D conversion 1 and A/D conversion 2. Figure 48.4 shows an example of this. In this case, post-D/A conversion value A is continuously output as the DA0 signal.

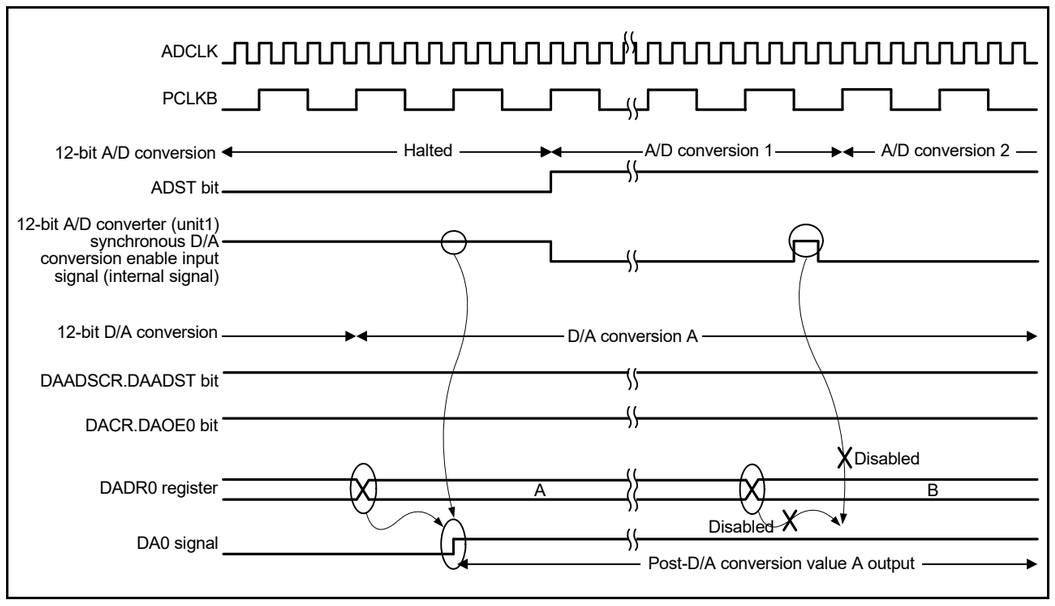


Figure 48.4 Example when the DAC12 cannot capture the synchronous D/A conversion enable input signal from the ADC12 (unit 1)

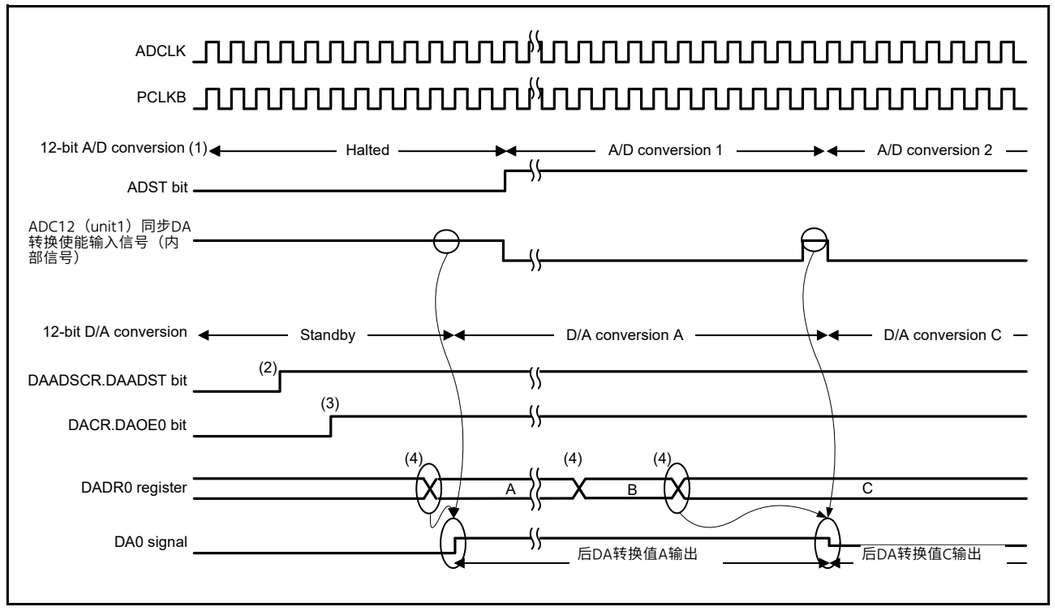


Figure 48.3 DAC12与ADC12同步时的转换示例

当ADCLK比PCLKB快时，DAC12可能无法在AD转换1和AD转换2之间输出的1个ADCLK周期内捕获ADC12（单元1）同步DA转换使能输入信号。图48.4显示了一个示例这个。在这种情况下，后DA转换值A作为DA0信号连续输出。

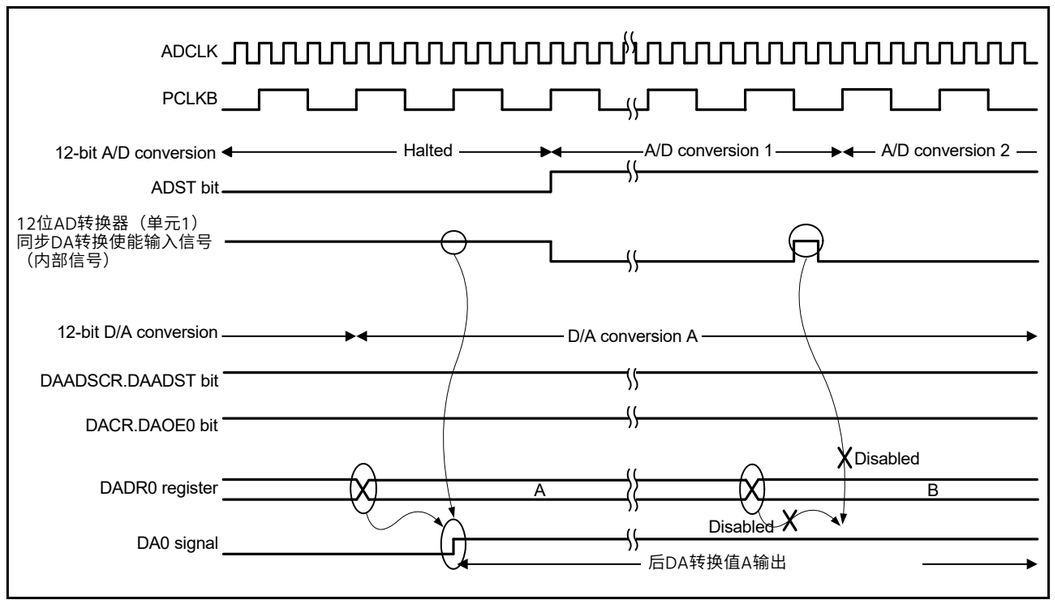


Figure 48.4 DAC12无法捕获来自ADC12（单元1）的同步DA转换使能输入信号时的示例

48.4 Event Link Operation Setting Procedure

This section describes the procedures used in event link operation.

48.4.1 DA0 Event Link Operation Setting Procedure

To set up DA0 event link operation:

1. Set the DADPR.DPSEL bit and set the data for D/A conversion in the DADR0 register.
2. Set the ELC_DA0 event signal to be linked to each peripheral module in the ELSR12 register.
3. Set the ELCR.ELCON bit to 1. This enables event link operation for all modules with the event link function selected.
4. Set the event output source module to activate the event link. After the event is output from the module, the DACR.DAOE0 bit sets to 1, and D/A conversion starts on channel 0.
5. Set the ELSR12.ELS[8:0] bits to 000h to stop event link operation on DAC12 channel 0. All event link operation is stopped when the ELCR.ELCON bit is set to 0.

48.4.2 DA1 Event Link Operation Setting Procedure

To set up DA1 event link operation:

1. Set the DADPR.DPSEL bit and set the data for D/A conversion in the DADR1 register.
2. Set the ELC_DA1 event signal to be linked to each peripheral module in the ELSR13 register.
3. Set the ELCR.ELCON bit to 1. This enables event link operation for all modules with the event link function selected.
4. Set the event output source module to activate the event link. After the event is output from the module, the DACR.DAOE1 bit sets to 1, and D/A conversion starts on channel 1.
5. Set the ELSR13.ELS[8:0] bits to 000h to stop event link operation on DAC12 channel 1. All event link operation is stopped when the ELCR.ELCON bit is set to 0.

48.5 Usage Notes on Event Link Operation

- When the event link function is used, do not use the amplifier output function.
- When the event link function is used, set the DACR.DAE bit to 0.
- When the event specified for the ELC_DA0 event signal is generated while the write cycle is performed on the DACR.DAOE0 bit, the write cycle is stopped, and the generated event takes precedence in setting the bit to 1.
- When the event specified for the ELC_DA1 event signal is generated while the write cycle is performed on the DACR.DAOE1 bit, the write cycle is stopped, and the generated event takes precedence in setting the bit to 1.
- Use of the event link function is prohibited when the DAADSCR.DAADST bit is set to 1 to reduce interference between D/A and A/D conversions.

48.6 Usage Notes

48.6.1 Settings for the Module-Stop Function

DAC12 operation can be disabled or enabled using the Module Stop Control Register. The DAC12 is initially stopped after reset. Releasing the module-stop state enables access to the registers. For details, see section 11, Low Power Modes.

48.6.2 DAC12 Operation in the Module-Stop State

When the MCU enters the module-stop state with D/A conversion enabled, the D/A outputs are retained, and the analog power supply current is the same as during D/A conversion. If the analog power supply current must be reduced in the module-stop state, disable D/A conversion by setting the DACR.DAOE1, DAOE0, and DAE bits to 0.

48.4 事件链接操作设置步骤

本节介绍事件链接操作中使用的过程。

48.4.1 DA0事件链接操作设置步骤

设置DA0事件链接操作：

1. 设置DADPR.DPSEL位并在DADR0寄存器中设置用于DA转换的数据。
2. 将ELC_DA0事件信号设置为链接到ELSR12寄存器中的每个外围模块。
3. 将ELCR.ELCON位设置为1。这将为所有选择了事件链接功能的模块启用事件链接操作。
4. 设置事件输出源模块以激活事件链接。事件从模块输出后，DACR.DAOE0位设置为1，DA转换从通道0开始。
5. 将ELSR12.ELS[8:0]位设置为000h以停止DAC12通道0上的事件链接操作。当ELCR.ELCON位设置为0时，将停止所有事件链接操作。

48.4.2 DA1事件链接操作设置步骤

设置DA1事件链接操作：

1. 设置DADPR.DPSEL位并在DADR1寄存器中设置用于DA转换的数据。
2. 设置ELC_DA1事件信号链接到ELSR13寄存器中的每个外围模块。
3. 将ELCR.ELCON位设置为1。这将为所有选择了事件链接功能的模块启用事件链接操作。
4. 设置事件输出源模块以激活事件链接。事件从模块输出后，DACR.DAOE1位设置为1，DA转换从通道1开始。
5. 将ELSR13.ELS[8:0]位设置为000h以停止DAC12通道1上的事件链接操作。当ELCR.ELCON位设置为0时，将停止所有事件链接操作。

48.5 事件链接操作使用说明

- 使用事件链接功能时，请勿使用放大器输出功能。
- 使用事件链接功能时，将DACR.DAE位设置为0。
- 当对ELC_DA0事件信号指定的事件在执行写入周期时生成DACR.DAOE0位，写周期停止，产生的事件优先将该位设置为1。
- 当在对ELC_DA1事件信号执行写周期时生成指定的事件时DACR.DAOE1位，写周期停止，产生的事件优先将该位设置为1。
- 当DAADSCR.DAADST位设置为1以减少DA和AD转换之间的干扰时，禁止使用事件链接功能。

48.6 使用说明

48.6.1 模块停止功能的设置

可以使用模块停止控制寄存器禁用或启用DAC12操作。DAC12在复位后最初停止。释放模块停止状态可以访问寄存器。有关详细信息，请参阅第11节，低功耗模式。

48.6.2 DAC12在模块停止状态下的操作

当MCU进入模块停止状态并启用DA转换时，DA输出保持不变，模拟电源电流与DA转换时相同。如果在模块停止状态下必须降低模拟电源电流，则通过将DACR.DAOE1、DAOE0和DAE位设置为0来禁用DA转换。

48.6.3 DAC12 Operation in Software Standby Mode

When the MCU enters Software Standby mode with D/A conversion enabled, the D/A outputs are retained, and the analog power supply current is the same as during D/A conversion. If the analog power supply current must be reduced in Software Standby mode, disable D/A conversion by setting the DACR.DAOE1, DAOE0, and DAE bits to 0.

48.6.4 Constraint on Entering Deep Software Standby Mode

When the MCU enters Deep Software Standby mode with D/A conversion enabled, the outputs of the DAC12 are placed in a high impedance state.

48.6.5 Initialization Procedure with the Output Amplifier

Use the following initialization procedures with the output amplifier. The example shows the case for channel 0.

To initialize the DAC12 with the output amplifier:

1. Write 000h to the DADR0 register.
2. Set the DAASWCR.DAASW0 bit to 1.
3. Set the DAAMPCR.DAAMP0 bit to 1.
4. Set the DACR.DAE bit or the DACR.DAOE0 bit to 1 to start operation of the amplifier.
5. Clear the DAASWCR.DAASW0 bit to 0 after waiting D/A conversion time tCONV.
6. Write the value to be converted in the DADR0 register.

While the amplifier is running, clearing the DACR.DAE and DACR.DAOE0 bits to 0 allows the amplifier to stop operation. To use the amplifier again, repeat procedures 1 to 6.

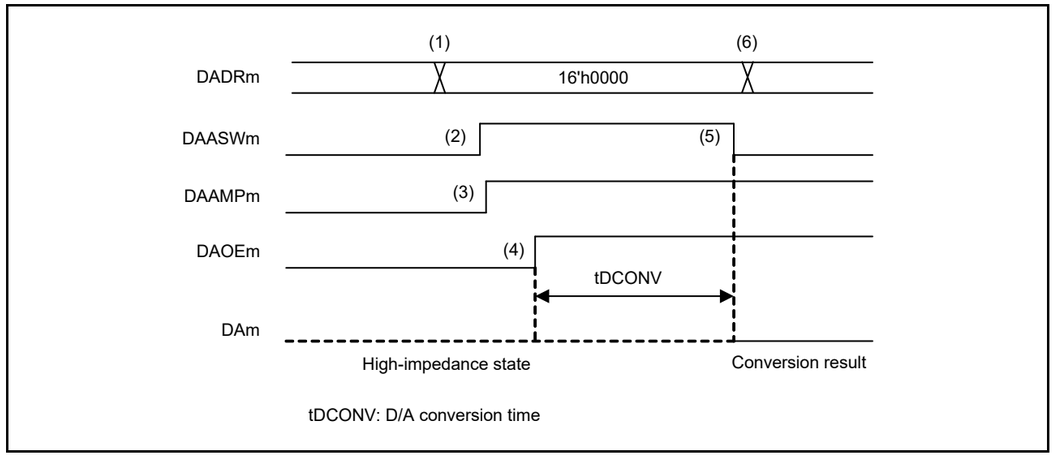


Figure 48.5 Example of the initial flow with the output amplifier in DAC12

48.6.6 Constraints on Usage When Interference Prevention between D/A and A/D Conversion Is Enabled

When the DAADSCR.DAADST bit is 1 (interference prevention between D/A and A/D conversion is enabled), do not place the ADC12 in the module-stop state. This might halt D/A conversion in addition to A/D conversion.

48.6.3 DAC12在软件待机模式下的操作

当MCU进入软件待机模式并启用DA转换时，DA输出保持不变，模拟电源电流与DA转换期间相同。如果在软件待机模式下必须降低模拟电源电流，则通过将DACR.DAOE1、DAOE0和DAE位设置为0来禁用DA转换。

48.6.4 进入深度软件待机模式的限制

当MCU在启用DA转换的情况下进入深度软件待机模式时，DAC12的输出置于高阻抗状态。

48.6.5 输出放大器的初始化程序

对输出放大器使用以下初始化程序。该示例显示了通道0的情况。

使用输出放大器初始化DAC12：

1. 将000h写入DADR0寄存器。
2. 将DAASWCR.DAASW0位设置为1。
3. 将DAAMPCR.DAAMP0位设置为1。
4. 将DACR.DAE位或DACR.DAOE0位设置为1以启动放大器的操作。
5. 等待DA转换时间tCONV后，将DAASWCR.DAASW0位清零。
6. 将要转换的值写入DADR0寄存器。

在放大器运行时，将DACR.DAE和DACR.DAOE0位清零可让放大器停止运行。要再次使用放大器，请重复步骤1至6。

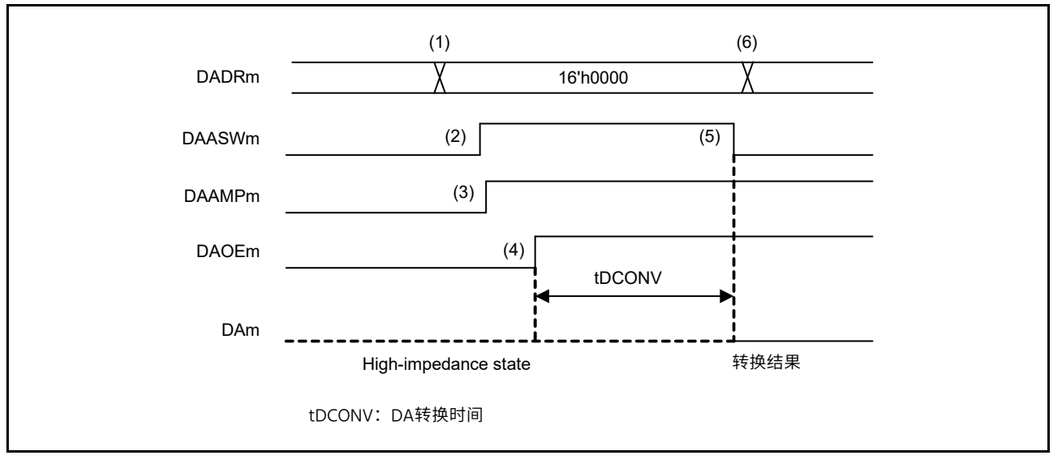


Figure 48.5 DAC12中输出放大器的初始流程示例

48.6.6 DA和AD之间防止干扰时的使用限制转换已启用

当DAADSCR.DAADST位为1（启用DA和AD转换之间的干扰防止）时，不要将ADC12置于模块停止状态。除了AD转换之外，这可能会停止DA转换。

49. Temperature Sensor (TSN)

49.1 Overview

The on-chip temperature sensor can be used to determine and monitor the die temperature for reliable operation of the device. The sensor outputs a voltage directly proportional to the die temperature, and the relationship between the die temperature and the output voltage is fairly linear. The output voltage is provided to the ADC12 for conversion and can also be used by the end application. Table 49.1 lists the temperature sensor specifications and Figure 49.1 shows a block diagram.

Table 49.1 Temperature sensor specifications

Parameter	Specifications
Temperature sensor voltage output	Temperature sensor outputs a voltage to the 12-Bit A/D Converter (ADC12).
Module-stop function	Module-stop state can be set to reduce power consumption
Temperature sensor calibration data	Reference data measured for each MCU at factory shipment is stored

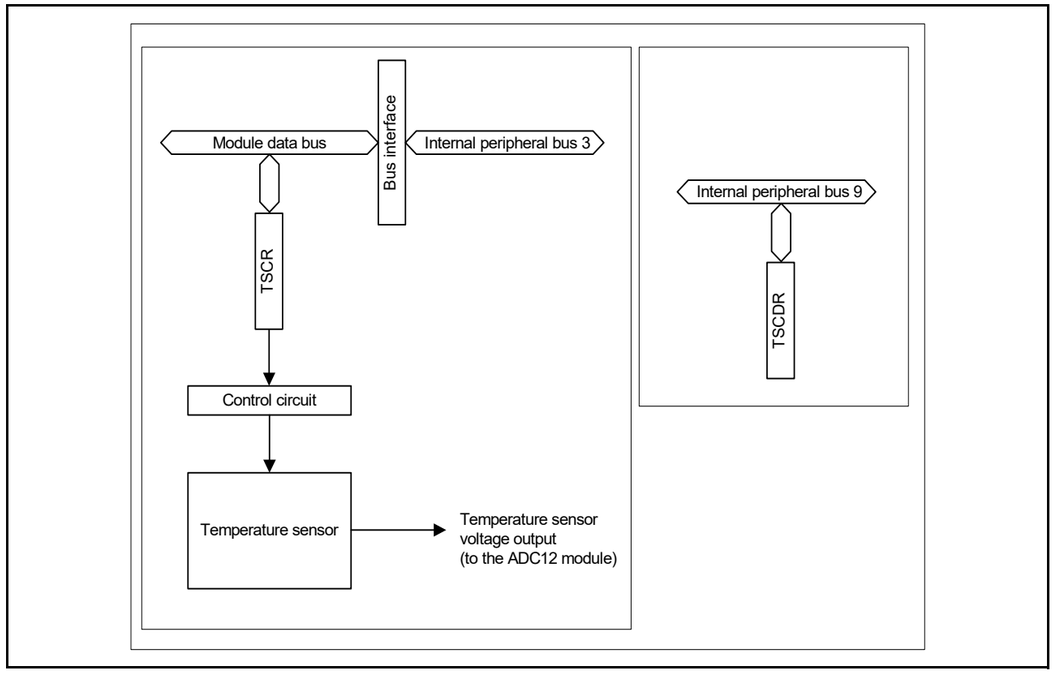


Figure 49.1 Temperature sensor block diagram

49. 温度传感器(TSN)

49.1 Overview

片上温度传感器可用于确定和监控芯片温度，以确保器件可靠运行。传感器输出与管芯温度成正比的电压，管芯温度与输出电压之间的关系相当线性。输出电压提供给ADC12进行转换，也可供最终应用使用。表49.1列出了温度传感器规格，图49.1显示了框图。

Table 49.1 温度传感器规格

Parameter	Specifications
温度传感器电压输出	温度传感器向12位模数转换器(ADC12)输出电压。
Module-stop function	可设置模块停止状态以降低功耗
温度传感器校准数据	存储在出厂时为每个MCU测量的参考数据

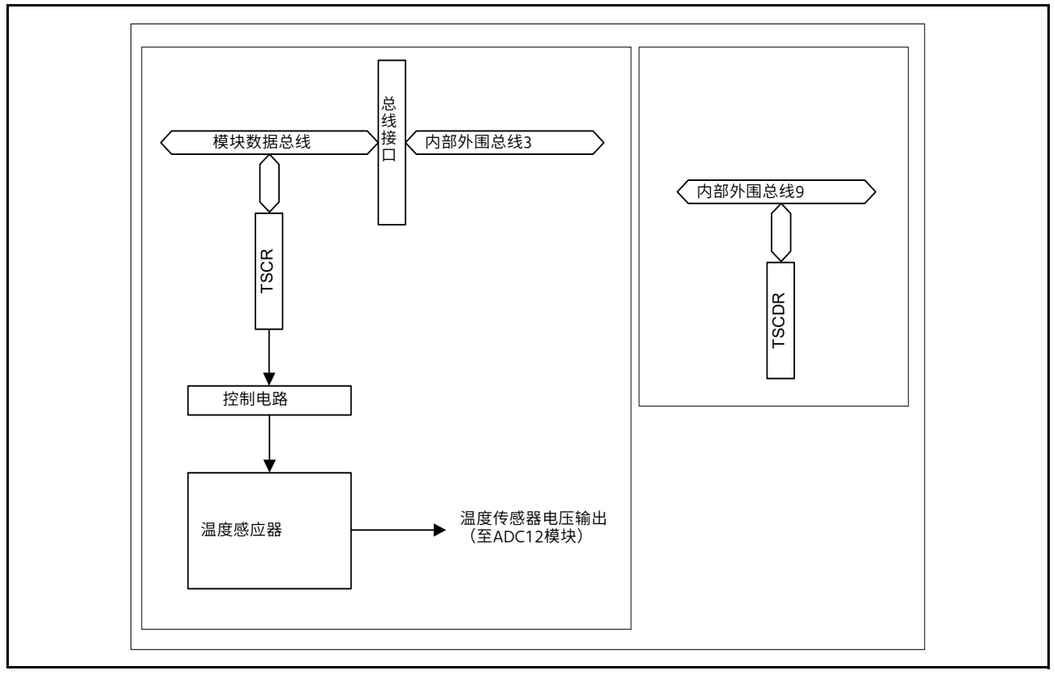


Figure 49.1 温度传感器框图

49.2 Register Descriptions

49.2.1 Temperature Sensor Control Register (TSCR)

Address(es): TSN.TSCR 4005 D000h

	b7	b6	b5	b4	b3	b2	b1	b0
	TSEN	—	—	TSOE	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	TSOE	Temperature Sensor Output Enable	0: Disable output from the temperature sensor to the ADC12 1: Enable output from the temperature sensor to the ADC12.	R/W
b6, b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	TSEN	Temperature Sensor Enable	0: Stop the temperature sensor 1: Start the temperature sensor.	R/W

The timing constraints shown in Figure 49.3 apply to the settings of the TSCR register.

49.2.2 Temperature Sensor Calibration Data Register(TSCDR)

Address(es): TSD.TSCDR 407F B17Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—												
Value after reset:	0	0	0	0	Unique value for each MCU											

The TSCDR register stores temperature sensor calibration data measured for each MCU at factory shipment. Temperature sensor calibration data is a digital value obtained using the 12-bit A/D converter unit 0 to convert the voltage output by the temperature sensor under the condition Ta = Tj = 127°C and AVCC0 = 3.3 V.

The TSCDR register is a 32-bit read-only register and should be read in 32-bit units.

49.3 Using the Temperature Sensor

The temperature sensor outputs a voltage which varies with the temperature. This voltage is converted to a digital value by the ADC12. You can then obtain the die temperature by converting the value into the temperature.

49.3.1 Preparation for Using the Temperature Sensor

The temperature (T) is proportional to the sensor voltage output (Vs), so temperature is calculated with the following formula:

T = (Vs - V1) / Slope + T1

T: Measured temperature (°C)

Vs: Voltage output by the temperature sensor when temperature is measured (V)

T1: Temperature experimentally measured at one point (°C)

49.2 注册说明

49.2.1 温度传感器控制寄存器(TSCR)

Address(es): TSN.TSCR 4005 D000h

	b7	b6	b5	b4	b3	b2	b1	b0
	TSEN	—	—	TSOE	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b3 to b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b4	TSOE	温度传感器输出使能	0：禁用从温度传感器到ADC12的输出1：启用从温度传感器到ADC12的输出。	R/W
b6, b5	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b7	TSEN	温度传感器启用	0：停止温度传感器1：启动温度传感器。	R/W

图49.3所示的时序约束适用于TSCR寄存器的设置。

49.2.2 温度传感器校准数据寄存器(TSCDR)

Address(es): TSD.TSCDR 407F B17Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—												
重置后的值：	0	0	0	0	每个MCU的独特价值											

TSCDR寄存器存储在出厂时为每个MCU测量的温度传感器校准数据。
温度传感器校准数据是使用12位AD转换器单元0在Ta=Tj=127°C和AVCC0=3.3V的条件下转换温度传感器输出的电压得到的数字值。

TSCDR寄存器是一个32位只读寄存器，应该以32位为单位读取。

49.3 使用温度传感器

温度传感器输出随温度变化的电压。该电压由ADC12转换为数字值。然后，您可以通过将该值转换为温度来获得芯片温度。

49.3.1 使用温度传感器的准备工作

温度(T)与传感器电压输出(Vs)成正比，因此使用以下公式计算温度：

T = (Vs - V1) / Slope + T1

T:测量温度(°C)

Vs：测量温度时温度传感器输出的电压（V）

T1：在某一点实验测量的温度(°C)

V1: Voltage output by the temperature sensor when T1 is measured (V)

T2: Temperature at the experimental measurement of another point (°C)

V2: Voltage output by the temperature sensor when T2 is measured (V)

Slope: Temperature gradient of the temperature sensor (V / °C), Slope = (V2 - V1) / (T2 - T1)

Determine the values for formula parameter (V1, T1, Slope) measurement. These values vary from sensor to sensor, and Renesas recommends making the following experimental measurement at two different temperatures to determine the values for these parameters:

1. Use the ADC12 to measure the voltage V1 output by the temperature sensor at temperature T1.
2. Use the ADC12 to measure the voltage V2 output by the temperature sensor at a different temperature T2. Obtain the temperature gradient (Slope = (V2 - V1) / (T2 - T1)) from these results.
3. Obtain subsequent temperatures by substituting the slope into the formula for the temperature characteristic (T = (Vs - V1) / Slope + T1).

If you are using the temperature slope given in Table 60.45 of section 60, Electrical Characteristics, use the 12-bit A/D converter unit 0 to measure the voltage V1 output by the temperature sensor at temperature T1, then calculate the temperature characteristic by using the following formula:

T = (Vs - V1) / Slope + T1

T: Measured temperature (°C)

Vs: Voltage output by the temperature sensor when the temperature is measured (V)

T1: Sample temperature measurement at first point (°C)

V1: Voltage output by the temperature sensor when T1 is measured (V)

Slope: Temperature slope given in Table 60.45 ÷ 1000 (V / °C)

In this MCU, the TSCDR register stores the temperature value (CAL127) of the temperature sensor measured under the condition Ta = Tj = 127°C and AVCC0 = 3.3 V. By using this value as the sample measurement result at the first point, preparation before using the temperature sensor can be omitted.

If V1 is calculated from CAL127:

V1 = 3.3 × CAL127 / 4096 [V]

Using this, the measured temperature can be calculated according to the following formula:

T = (Vs - V1) / Slope + 127 [°C]

T: Measured temperature (°C)

Vs: Voltage output by the temperature sensor when the temperature is measured (V)

V1: Voltage output by the temperature sensor when Ta = Tj = 127°C and AVCC0 = 3.3 V (V)

Slope: Temperature slope given in Table 60.45 ÷ 1000 (V / °C)

49.3.2 Procedures for Using the Temperature Sensor

Figure 49.2 shows the procedure for using the temperature sensor. For the procedure to configure the ADC12, see section 47, 12-Bit A/D Converter (ADC12).

V1：测量T1时温度传感器输出的电压（V）

T2：另一点的实验测量温度（°C）

V2：测量T2时温度传感器输出的电压（V）

斜率：温度传感器的温度梯度（V°C），斜率=（V2V1）（T2T1）

确定公式参数（V1、T1、斜率）测量的值。这些值因传感器而异，并且
瑞萨推荐在两种不同温度下进行以下实验测量以确定这些参数的值：

1. 使用ADC12测量温度传感器在温度T1时输出的电压V1。
2. 使用ADC12测量温度传感器在不同温度T2下输出的电压V2。从这些结果中获得温度梯度(Slope=(V2V1)(T2T1))。
3. 通过将斜率代入温度特性公式(T=(VsV1)Slope+T1)来获得后续温度。

如果您使用第60节，电气特性的表60.45中给出的温度斜率，使用12位AD转换器单元0测量温度传感器在温度T1输出的电压V1，然后使用以下公式计算温度特性公式：

T = (Vs - V1) / Slope + T1

T:测量温度(°C)

Vs：测温时温度传感器输出的电压（V）

T1：第一点的样品温度测量(°C)

V1：测量T1时温度传感器输出的电压（V）

斜率：表60.45÷1000(V°C)中给出的温度斜率

在此MCU中，TSCDR寄存器存储在Ta=Tj=127°C和AVCC0=3.3V条件下测量的温度传感器的温度值(CAL127)。
将此值用作第一点的样本测量结果，准备使用前可以省略温度传感器。

如果V1由CAL127计算得出：

V1 = 3.3 × CAL127 / 4096 [V]

使用它，可以根据以下公式计算测量的温度：

T = (Vs - V1) / Slope + 127 [°C]

T:测量温度(°C)

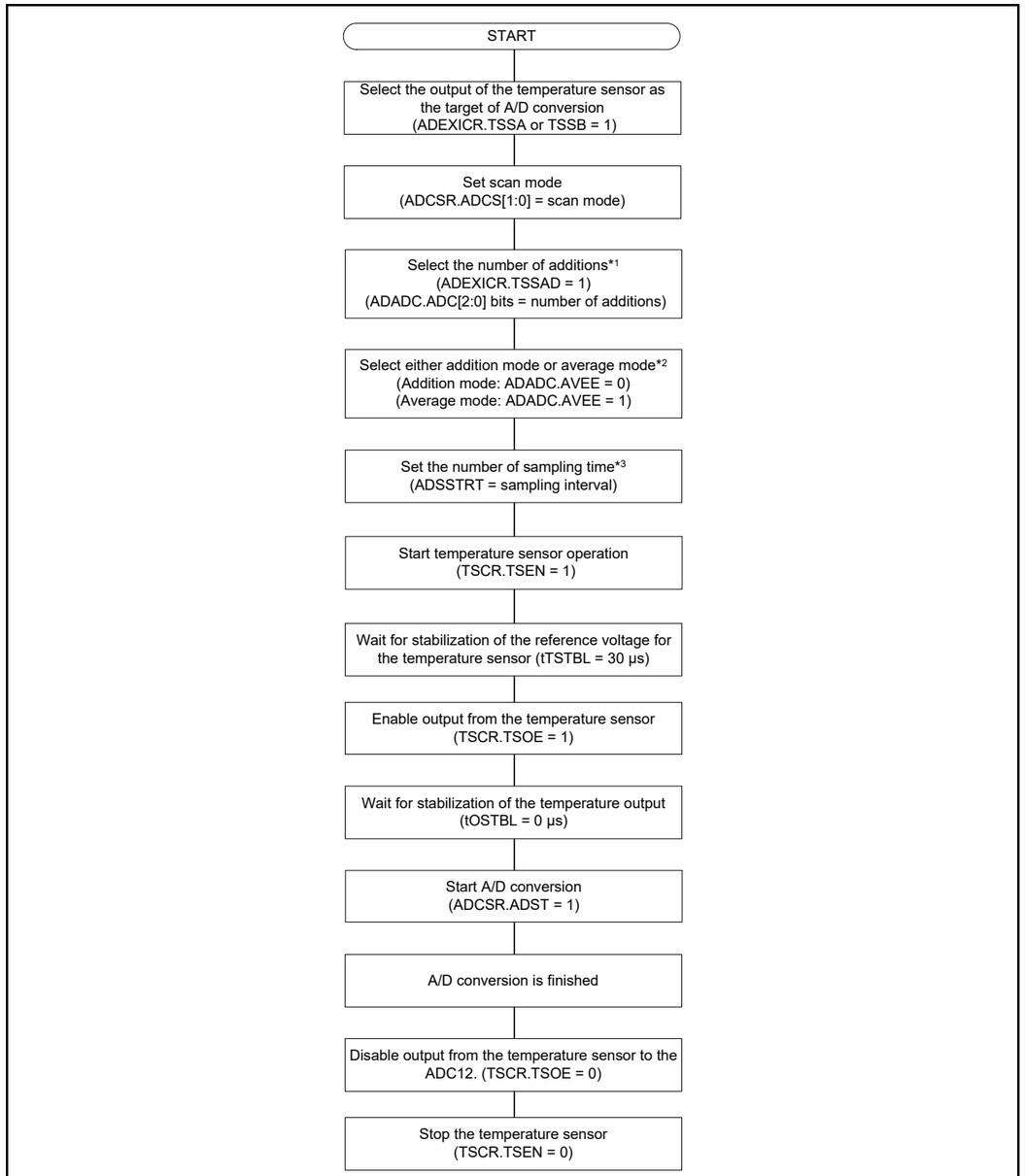
Vs：测温时温度传感器输出的电压（V）

V1：Ta=Tj=127°C且AVCC0=3.3V(V)时温度传感器输出的电压

斜率：表60.45÷1000(V°C)中给出的温度斜率

49.3.2 使用温度传感器的步骤

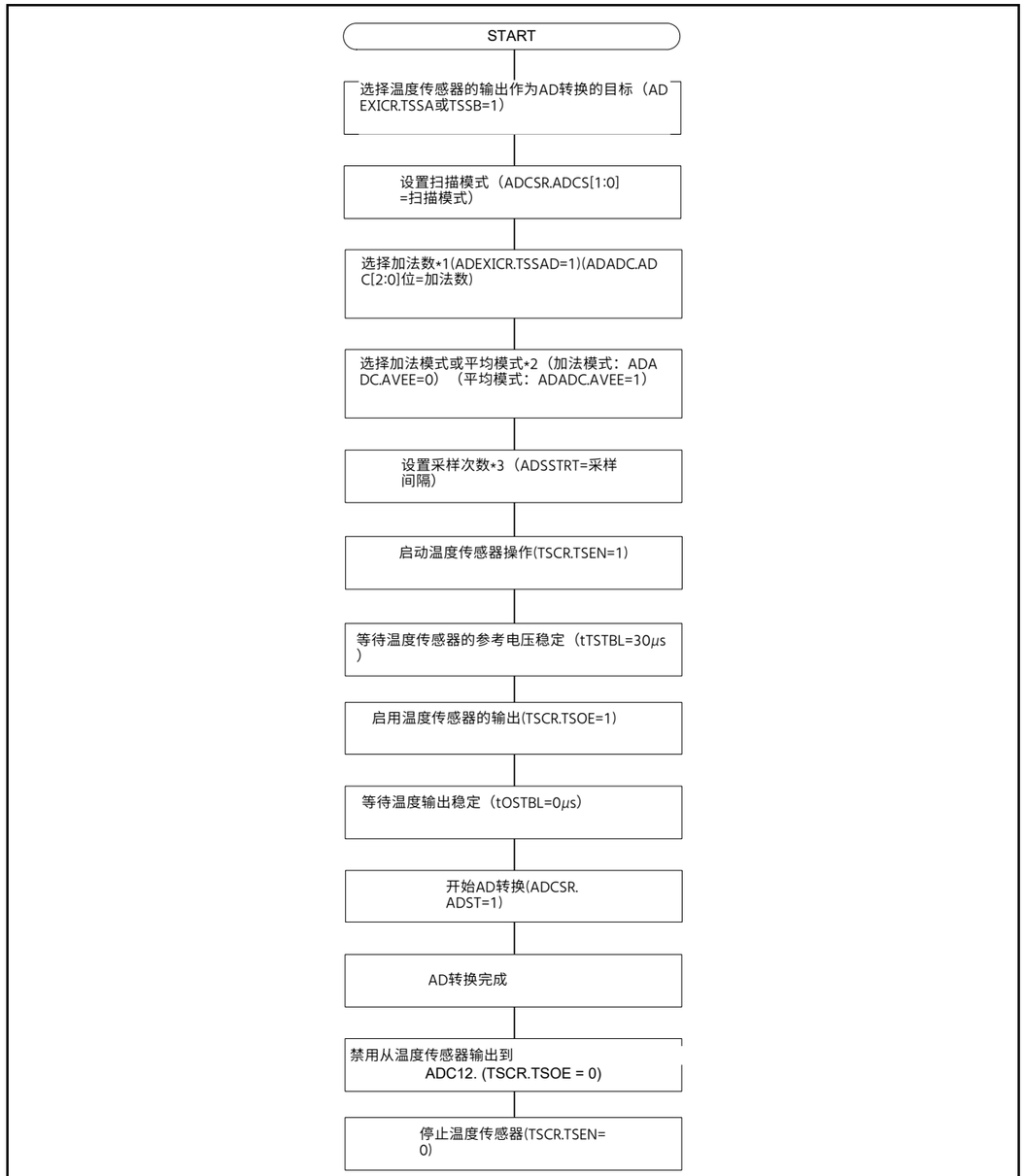
图49.2显示了使用温度传感器的步骤。有关配置ADC12的过程，请参阅第47节，12位AD转换器(ADC12)。



Note 1. The ADADC.ADC[2:0] setting is limited to some values in average mode. For details on available ADADC.ADC[2:0] settings in average mode, see section 47.2.10, A/D-Converted Value Addition/Average Count Select Register (ADADC).
Note 2. This setting is not required if addition/average mode is not set.
Note 3. Set the sampling time to more than the value described in section 60.7, TSN Characteristics.

Figure 49.2 Procedure for using the temperature sensor

Figure 49.3 shows the timing from the start of temperature sensor operation until the completion of A/D conversion when the ADC12 is in single scan mode (the conversion target is the temperature sensor output only). The times shown in the figure are described in Table 49.2.



Note 1. ADADC.ADC[2:0]设置仅限于平均模式下的某些值。有关平均模式下可用ADADC.ADC[2:0]设置的详细信息，请参见第47.2.10节，D转换值加法平均计数选择寄存器(ADADC)。
Note 2. 如果未设置加法平均模式，则不需要此设置。
Note 3. 将采样时间设置为大于第60.7节，TSN特性中描述的值。

Figure 49.2 温度传感器的使用步骤

图49.3显示了当ADC12处于单次扫描模式（转换目标仅为温度传感器输出）时，从温度传感器操作开始到AD转换完成的时序。图中显示的时间在表49.2中描述。

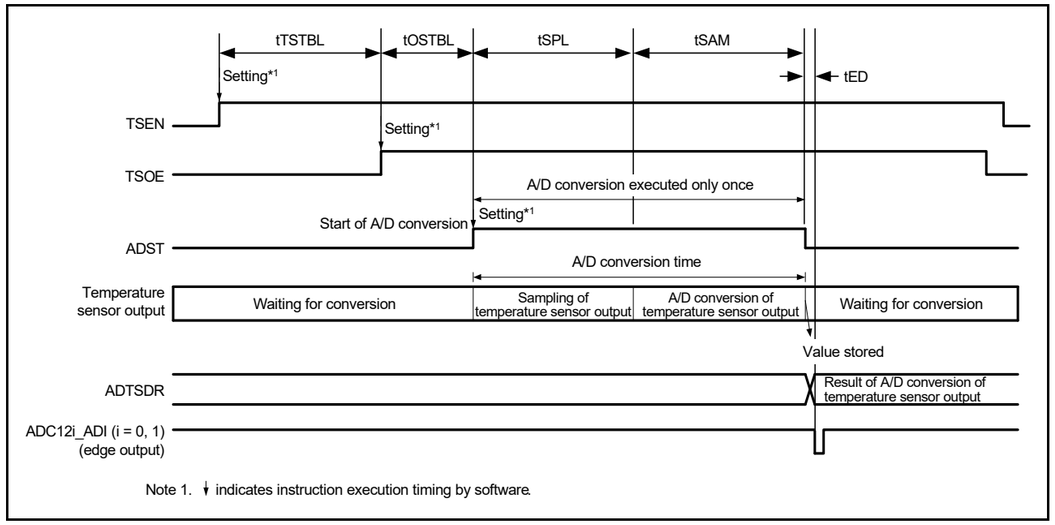


Figure 49.3 Timing from start of temperature sensor operation until completion of A/D conversion

Table 49.2 Time until completion of A/D conversion after start of temperature sensor operation

Parameter	Symbol	Time
Wait time for temperature sensor reference voltage stabilization	tTSTBL	30 µs (min)
Wait time for temperature sensor output stabilization	tOSTBL	0 µs (min)
ADC12 input sampling time	tSPL	ADSSTRT setting × ADCLK cycles
A/D conversion time	tSAM	See Table 47.10, Conversion times during scanning (in numbers of cycles of ADCLK and PCLKB)
Scan conversion end delay	tED	

49.4 Usage Notes

49.4.1 Settings for the Module-Stop Function

Temperature sensor operation can be disabled or enabled using the associated bit in Module Stop Control Register D (MSTPCRD). The temperature sensor is initially stopped after reset. Releasing the module-stop state enables access to the registers. For details, see section 11, Low Power Modes.

49.4.2 Constraints

It is prohibited to use both channels of the ADC12 simultaneously for temperature sensor measurement.

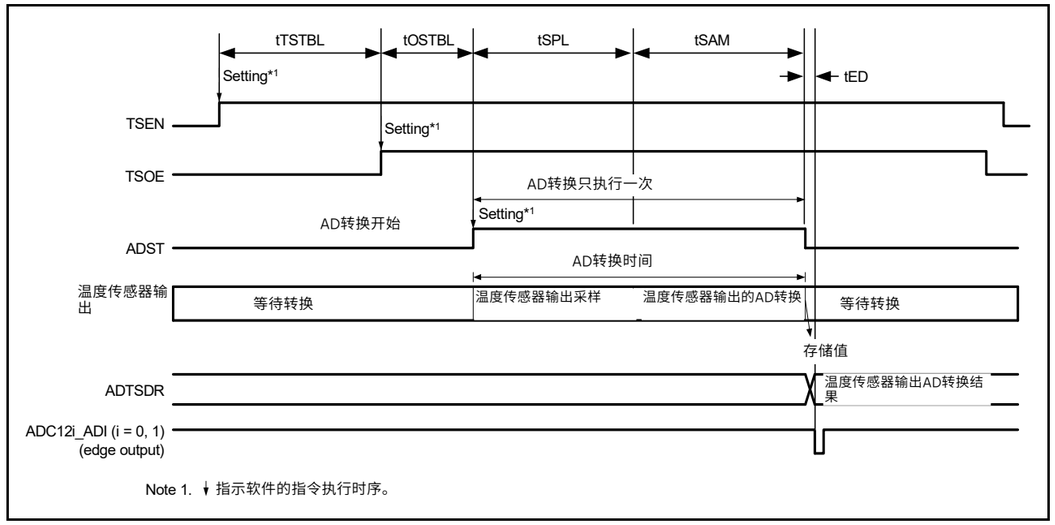


Figure 49.3 从温度传感器操作开始到AD转换完成的时间

Table 49.2 温度传感器动作开始后到AD转换完成的时间

Parameter	Symbol	Time
温度传感器参考电压稳定的等待时间	tTSTBL	30 µs (min)
温度传感器输出稳定的等待时间	tOSTBL	0 µs (min)
ADC12输入采样时间	tSPL	ADSTRT设置×ADCLK周期
AD转换时间	tSAM	请参见表47.10，扫描期间的转换时间（以ADCLK和PCLKB的周期数为单位）
扫描转换结束延迟	tED	

49.4 使用说明

49.4.1 模块停止功能的设置

可以使用模块停止控制寄存器D(MSTPCRD)中的相关位来禁用或启用温度传感器操作。温度传感器在复位后最初停止。释放模块停止状态可以访问寄存器。有关详细信息，请参阅第11节，低功耗模式。

49.4.2 Constraints

禁止同时使用ADC12的两个通道进行温度传感器测量。

50. High-Speed Analog Comparator (ACMPHS)

50.1 Overview

The High-Speed Analog Comparator (ACMPHS) can be used to compare a test voltage with a reference voltage and to provide a digital output based on the result of conversion. Both the test voltage and the reference voltage can be provided to the ACMPHS from internal sources (D/A converter output and internal reference voltage) and an external source (with or without an internal PGA). Such flexibility is useful in applications that require go/no-go comparisons to be performed between analog signals without necessarily requiring A/D conversion.

Table 50.1 lists the ACMPHS specifications, Figure 50.1 shows a block diagram, and Table 50.2 shows the input source configurations.

Table 50.1 ACMPHS 0 to 5 specifications

Parameter	Specifications
Number of channels	6 channels: ACMPHS 0 to ACMPHS 5
Analog input voltage	• Output from internal PGA • Output from internal D/A converter • Input from internal A/D converter input pin (one selectable).
Reference voltage	• Internal reference voltage (Vref) • Output from internal D/A converter • Input from internal A/D converter input pin (one selectable).
ACMPHS output	• Comparison result • Generation of ELC event output • Monitor output from register.
Interrupt request signal	• Interrupt request generated on valid edge detection from comparison result • Selectable to rising edge, falling edge, or both edges.
Digital filter function	• Selectable to one of three sampling frequencies • Not using the filter function is selectable.

50. 高速模拟比较器(ACMPHS)

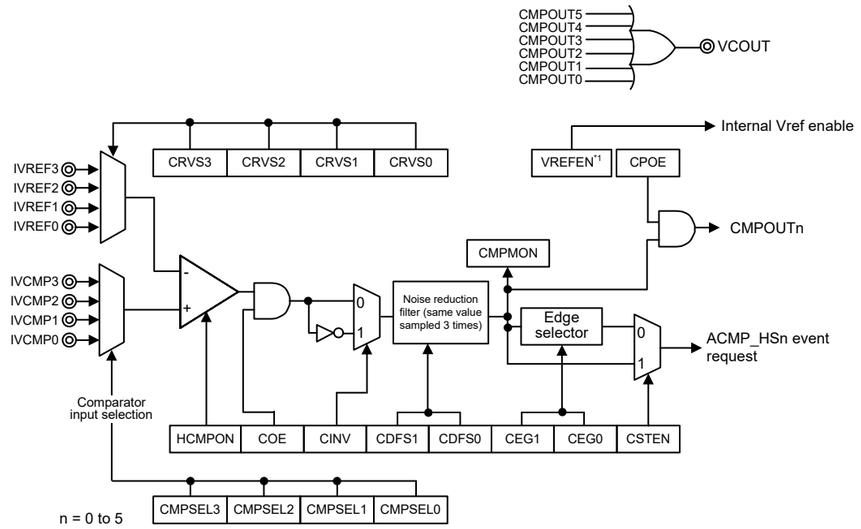
50.1 Overview

高速模拟比较器(ACMPHS)可用于将测试电压与参考电压进行比较，并根据转换结果提供数字输出。测试电压和参考电压都可以从内部源（DA转换器输出和内部参考电压）和外部源（带或不带内部PGA）提供给ACMPHS。这种灵活性在需要在模拟信号之间执行go-no-go比较而不一定需要AD转换的应用中很有用。

表50.1列出了ACMPHS规范，图50.1显示了框图，表50.2显示了输入源配置。

Table 50.1 ACMPHS0到5规格

Parameter	Specifications
通道数	6 channels: ACMPHS 0 to ACMPHS 5
模拟输入电压	来自内部PGA的输出 来自内部DA转换器的输出 来自内部AD转换器输入引脚的输入（一个可选）。
参考电压	内部参考电压(Vref) 来自内部DA转换器的输出 从内部AD转换器输入引脚输入（一个可选）。
ACMPHS output	比较结果 生成ELC事件输出 监控寄存器的输出。
中断请求信号	从比较结果中检测到有效边沿时产生中断请求 可选择上升沿、下降沿或两个边沿。
数字滤波功能	可选择三个采样频率之一。 可选择不使用滤波器功能。



CMPSEL3 to CMPSEL0: Bits in CMPSEL0 register
CRVS3 to CRVS0: Bits in CMPSEL1 register
CPOE, VREFEN: Bits in CPIOC register
CMPMON: Bit in CMPMON register
HCMPON, COE, CINV, CDFS1, CDFS0, CEG1, CEG0, CSTEN: Bits in CMPCTL register

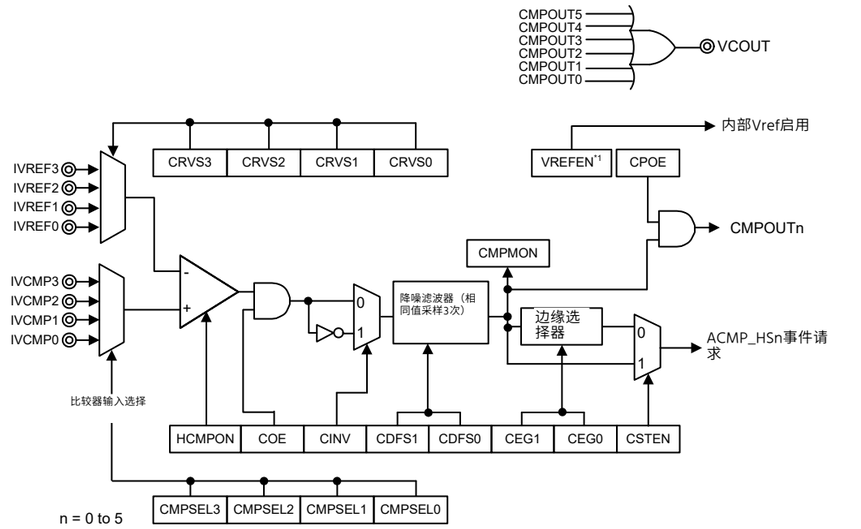
Note: VREFEN exists only in ACMPHS0.

Figure 50.1 ACMPHS block diagram

Table 50.2 Input source configuration of the ACMPHS

	Reference voltage input source				Analog voltage input source				
Comparator	IVREF3	IVREF2	IVREF1	IVREF0	IVCMP3	IVCMP2	IVCMP1	IVCMP0	Output pin
ACMPHS0	DA0*1	Vref*2	AN116	AN016	PGA0 output*6	AN000*3, *6	DA1*4	AN017	VCOUT*5
ACMPHS1	DA0*1	Vref*2	AN116	AN016	PGA1 output*6	AN001*3, *6	DA1*4	AN017	
ACMPHS2	DA0*1	Vref*2	AN116	AN016	PGA2 output*6	AN002*3, *6	DA1*4	AN017	
ACMPHS3	DA0*1	Vref*2	AN116	AN016	PGA3 output*6	AN100*3, *6	DA1*4	AN017	
ACMPHS4	DA0*1	Vref*2	AN116	AN016	PGA4 output*6	AN101*3, *6	DA1*4	AN017	
ACMPHS5	DA0*1	Vref*2	AN116	AN016	PGA5 output*6	AN102*3, *6	DA1*4	AN017	

Note 1. When D/A converter 0 output is not used, the signal can be used as AN005/AN105 analog input.
Note 2. Internal voltage reference.
Note 3. Because input is through PGA, the associated Module Stop bit, MSTPCRD.MSTPD16 (unit 0) or MSTPCRD.MSTPD15 (unit 1) should be set to 0.
Note 4. When D/A converter 1 output is not used, the signal can be used as AN006/AN106 analog input.
Note 5. ACMPHS0 to ACMPHS5 compare outputs are bundled with the VCOUT pin.
Note 6. Setting of the ADC12 is required. For details, see section 47.6.8, Available Functions and Register Settings of AN000 to AN002, AN007, AN100 to AN102, and AN107.



CMPSEL3到CMPSEL0：CMPSEL0寄存器中的位
CRVS3到CRVS0：CMPSEL1寄存器中的位
CPOE、VREFEN：CPIOC寄存器中的位
CMPMON：CMPMON寄存器中的位
HCMPON、COE、CINV、CDFS1、CDFS0、CEG1、CEG0、CSTEN：CMPCTL寄存器中的位

Note: VREFEN仅存在于ACMPHS0中。

Figure 50.1 ACMPHS框图

Table 50.2 ACMPHS的输入源配置

	参考电压输入源				模拟电压输入源				
Comparator	IVREF3	IVREF2	IVREF1	IVREF0	IVCMP3	IVCMP2	IVCMP1	IVCMP0	输出引脚
ACMPHS0	DA0*1	Vref*2	AN116	AN016	PGA0 output*6	AN000*3, *6	DA1*4	AN017	VCOUT*5
ACMPHS1	DA0*1	Vref*2	AN116	AN016	PGA1 output*6	AN001*3, *6	DA1*4	AN017	
ACMPHS2	DA0*1	Vref*2	AN116	AN016	PGA2 output*6	AN002*3, *6	DA1*4	AN017	
ACMPHS3	DA0*1	Vref*2	AN116	AN016	PGA3 output*6	AN100*3, *6	DA1*4	AN017	
ACMPHS4	DA0*1	Vref*2	AN116	AN016	PGA4 output*6	AN101*3, *6	DA1*4	AN017	
ACMPHS5	DA0*1	Vref*2	AN116	AN016	PGA5 output*6	AN102*3, *6	DA1*4	AN017	

Note 1. 当不使用DA转换器0输出时，该信号可用作AN005AN105模拟输入。
Note 2. 内部参考电压。
Note 3. 由于输入是通过PGA进行的，因此相关的模块停止位MSTPCRD.MSTPD16（单元0）或MSTPCRD.MSTPD15（单元1）应设置为0。
Note 4. 当不使用DA转换器1输出时，该信号可用作AN006AN106模拟输入。
Note 5. ACMPHS0到ACMPHS5比较输出与VCOUT引脚捆绑在一起。
Note 6. 需要设置ADC12。有关详细信息，请参阅第47.6.8节，AN000的可用功能和寄存器设置AN002、AN007、AN100至AN102和AN107。

50.2 Register Descriptions

50.2.1 Comparator Control Register (CMPCTL)

Address(es): ACMPHS0.CMPCTL 4008 5000h,ACMPHS1.CMPCTL 4008 5100h, ACMPHS2.CMPCTL 4008 5200h, ACMPHS3.CMPCTL 4008 5300h, ACMPHS4.CMPCTL 4008 5400h, ACMPHS5.CMPCTL 4008 5500h

	b7	b6	b5	b4	b3	b2	b1	b0
	HCMPON	CDFS[1:0]		CEG1	CEG0	CSTEN	COE	CINV
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	CINV	Comparator Output Polarity Selection*2, *3	0: Do not invert comparator output 1: Invert comparator output.	R/W
b1	COE	Comparator Output Enable	0: Disable comparator output (output signal is low level) 1: Enable comparator output.	R/W
b2	CSTEN	Interrupt Select*1	0: Output through the edge selector 1: Output directly.	R/W
b4, b3	CEG1/CEG0	Selection of Valid Edge (Edge Selector)	b4 b3 0 0: Do not detect edge 0 1: Detect rising edge 1 0: Detect falling edge 1 1: Detect both edges.	R/W
b6, b5	CDFS[1:0]	Noise Filter Selection*1, *2, *3, *4	b6 b5 0 0: Do not use noise filter. 0 1: Use noise filter sampling frequency of PCLKB/2[3] 1 0: Use noise filter sampling frequency of PCLKB/2[4] 1 1: Use noise filter sampling frequency of PCLKB/2[5].	R/W
b7	HCMPON	Comparator Operation Control*5	0: Stop operation (comparator outputs a low-level signal) 1: Enable operation (enables input to the comparator pins).	R/W

Note 1. Set the CSTEN bit to 1 and the CDFS[1:0] bits to 00b if the ACMPHS interrupt causes release of Software Standby or Snooze modes. CTSEN is supported only by the ACMPHS0. ACMPHSn.CMPCTL.CTESN (n = 1 to 5) must be set to 0.
Note 2. Disable the ACMPHS output (COE = 0) before changing the CDFS[1:0] and CINV bits.
Note 3. If the CDFS[1:0] and CINV bits are changed, an ACMPHS interrupt request and an ELC event might be generated. Before changing these bits, set the ELSRn register to 0 (the ACMPHS output is not linked). After changing these bits, clear the IR flag in the IELSRn register to 0 to clear the interrupt status.
Note 4. If the CDFS[1:0] bits are changed from 00b (noise filter not used) to a value other than 00b (noise filter used), perform sampling four times and update the filter output, and then use the ACMPHS interrupt request or the ELC event.
Note 5. A stabilization wait time is required to permit ACMPHS operation after enabling it (HCMPON = 1). The operation stabilization wait time for ACMPHS modules 0 to 5 is 300 ns.

The CMPCTL register controls the ACMPHS operation, enables or disables the ACMPHS output, selects the noise filter, selects the valid edge of the interrupt signal, and selects the interrupt. A reset clears this register to 00h.

50.2 注册说明

50.2.1 比较器控制寄存器(CMPCTL)

Address(es): ACMPHS0.CMPCTL 4008 5000h,ACMPHS1.CMPCTL 4008 5100h, ACMPHS2.CMPCTL 4008 5200h, ACMPHS3.CMPCTL 4008 5300h, ACMPHS4.CMPCTL 4008 5400h, ACMPHS5.CMPCTL 4008 5500h

	b7	b6	b5	b4	b3	b2	b1	b0
	HCMPON	CDFS[1:0]		CEG1	CEG0	CSTEN	COE	CINV
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	CINV	比较器输出极性Selection*2, *3	0：不反转比较器输出1：反转比较器输出。	R/W
b1	COE	比较器输出使能	0：禁止比较器输出（输出信号为低电平）1：使能比较器输出。	R/W
b2	CSTEN	Interrupt Select*1	0：通过边沿选择器输出1：直接输出。	R/W
b4, b3	CEG1/CEG0	有效边的选择（边Selector)	b4b300：不检测边沿01：检测上升沿10：检测下降沿11：检测两个边沿。	R/W
b6, b5	CDFS[1:0]	噪声滤波器选择*1、*2、*3、*4	b6b500：不使用噪声滤波器。01：使用PCLKB231的噪声滤波器采样频率0：使用PCLKB241的噪声滤波器采样频率1：使用PCLKB25的噪声滤波器采样频率。	R/W
b7	HCMPON	比较器操作控制*5	0：停止操作（比较器输出低电平信号）1：使能操作（使能输入到比较器引脚）。	R/W

Note 1. 如果ACMPHS中断导致软件待机或贪睡模式的释放，请将CSTEN位设置为1，并将CDFS[1:0]位设置为00b。只有ACMPHS0支持CTSEN。ACMPHSn.CMPCTL.CTESN（n=1到5）必须设置为0。
Note 2. 在更改CDFS[1:0]和CINV位之前禁用ACMPHS输出(COE=0)。
Note 3. 如果CDFS[1:0]和CINV位发生变化，可能会产生ACMPHS中断请求和ELC事件。在更改这些位之前，将ELSRn寄存器设置为0（ACMPHS输出未链接）。更改这些位后，将IELSRn寄存器中的IR标志清零以清除中断状态。
Note 4. 如果CDFS[1:0]位从00b（未使用噪声滤波器）更改为00b以外的值（使用噪声滤波器），执行四次采样并更新滤波器输出，然后使用ACMPHS中断请求或ELC事件。
Note 5. 在启用ACMPHS后，需要一个稳定等待时间来允许其运行(HCMPON=1)。ACMPHS模块0到5的操作稳定等待时间为300ns。

CMPCTL寄存器控制ACMPHS操作，使能或禁用ACMPHS输出，选择噪声滤波器，选择中断信号的有效边沿，选择中断。复位将该寄存器清除为00h。

50.2.2 Comparator Input Select Register (CMPSEL0)

Address(es): ACMPHS0.CMPSEL0 4008 5004h, ACMPHS1.CMPSEL0 4008 5104h, ACMPHS2.CMPSEL0 4008 5204h, ACMPHS3.CMPSEL0 4008 5304h, ACMPHS4.CMPSEL0 4008 5404h, ACMPHS5.CMPSEL0 4008 5504h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	CMPSEL[3:0]			
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	CMPSEL[3:0]	Comparator Input Selection*1	b3 b0 0 0 0 0: Do not input 0 0 0 1: Select IVCMP0*2 0 0 1 0: Select IVCMP1*2 0 1 0 0: Select IVCMP2*2 1 0 0 0: Select IVCMP3.*2 Other settings are prohibited.	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Use the following procedure to change the CMPSEL[3:0] bits. Writing a value other than 0000 0000b while the value of the CMPSEL0 register is not 0000 0000b is invalid. Writing 1 to two or more bits is also invalid. In both cases, the previous value is retained.
To change the CMPSEL[3:0] bits:
1. Set the CMPCTL.COE bit to 0.
2. Set the CMPSEL0 register to 0000 0000b.
3. Set a new value in the CMPSEL[3:0] bits, with 1 set in only one of the bits.
4. Wait for the input switching stabilization wait time (200 ns).
5. Set the CMPCTL.COE bit to 1.
6. Clear the IR flag in the IELSRn register to clear the interrupt status.

Note 2. For details, see Table 50.2.

50.2.3 Comparator Reference Voltage Select Register (CMPSEL1)

Address(es): ACMPHS0.CMPSEL1 4008 5008h, ACMPHS1.CMPSEL1 4008 5108h, ACMPHS2.CMPSEL1 4008 5208h, ACMPHS3.CMPSEL1 4008 5308h, ACMPHS4.CMPSEL1 4008 5408h, ACMPHS5.CMPSEL1 4008 5508h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	CRVS[3:0]			
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	CRVS[3:0]	Reference Voltage Selection*1	b3 b0 0 0 0 0: Do not input 0 0 0 1: Select IVREF0*2 0 0 1 0: Select IVREF1*2 0 1 0 0: Select IVREF2*2 1 0 0 0: Select IVREF3*2 Other settings are prohibited.	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Use the following procedure to change the CRVS[3:0] bits. Writing a value other than 0000 0000b while the value of the CMPSEL1 register is not 0000 0000b is invalid. Writing 1 to two or more bits is also invalid. In both cases, the previous value is retained.
To change the CRVS[3:0] bits:
1. Set the CMPCTL.COE bit to 0.
2. Set the CMPSEL1 register to 0000 0000b.
3. Set a new value to the CRVS[3:0] bits, with 1 set in only one of the bits.
4. Wait for the input switching stabilization wait time (200 ns)
5. Set the CMPCTL.COE bit to 1.

50.2.2 比较器输入选择寄存器(CMPSEL0)

Address(es): ACMPHS0.CMPSEL0 4008 5004h, ACMPHS1.CMPSEL0 4008 5104h, ACMPHS2.CMPSEL0 4008 5204h, ACMPHS3.CMPSEL0 4008 5304h, ACMPHS4.CMPSEL0 4008 5404h, ACMPHS5.CMPSEL0 4008 5504h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	CMPSEL[3:0]			
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b3 to b0	CMPSEL[3:0]	比较器输入选择*1	b3b00000：不输入0001：选择IVCMP0*20010：选择IVCMP1*20100：选择IVCMP2*21000：选择IVCMP3.*2其他设置有禁止。	R/W
b7 to b4	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 使用以下程序更改CMPSEL[3:0]位。写入00000000b以外的值，而CMPSEL0寄存器不是00000000b无效。将1写入两位或更多位也是无效的。在这两种情况下，都会保留先前的值。要更改CMPSEL[3:0]位：1.将CMPCTL.COE位设置为0。2.将CMPSEL0寄存器设置为00000000b。3.在CMPSEL[3:0]位中设置一个新值，其中一个位设置为1。4.等待输入切换稳定等待时间（200ns）。5.将CMPCTL.COE位设置为1。6.清除IELSRn寄存器中的IR标志以清除中断状态。

Note 2. 详见表50.2。

50.2.3 比较器参考电压选择寄存器(CMPSEL1)

Address(es): ACMPHS0.CMPSEL1 4008 5008h, ACMPHS1.CMPSEL1 4008 5108h, ACMPHS2.CMPSEL1 4008 5208h, ACMPHS3.CMPSEL1 4008 5308h, ACMPHS4.CMPSEL1 4008 5408h, ACMPHS5.CMPSEL1 4008 5508h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	CRVS[3:0]			
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b3 to b0	CRVS[3:0]	参考电压选择*1	b3b00000：不输入0001：选择IVREF0*20010：选择IVREF1*20100：选择IVREF2*21000：选择IVREF3*2禁止其他设置.	R/W
b7 to b4	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 使用以下过程更改CRVS[3:0]位。写入00000000b以外的值，而CMPSEL1寄存器不是00000000b无效。将1写入两位或更多位也是无效的。在这两种情况下，都会保留先前的值。要更改CRVS[3:0]位：1.将CMPCTL.COE位设置为0。2.将CMPSEL1寄存器设置为00000000b。3.为CRVS[3:0]位设置一个新值，其中一个位设置为1。4.等待输入开关稳定等待时间(200ns)5.将CMPCTL.COE位设置为1。

6. Clear the IR flag in the IELSRn register to clear the interrupt status.

Note 2. For details, see Table 50.2.

50.2.4 Comparator Output Monitor Register (CMPMON)

Address(es): ACMPHS0.CMPMON 4008 500Ch, ACMPHS1.CMPMON 4008 510Ch, ACMPHS2.CMPMON 4008 520Ch, ACMPHS3.CMPMON 4008 530Ch, ACMPHS4.CMPMON 4008 540Ch, ACMPHS5.CMPMON 4008 550Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	CMPMON
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	CMPMON	Comparator Output Monitor*1	0: Comparator output is low 1: Comparator output is high.	R
b7 to b1	—	Reserved	These bits are read as 0.	R

Note 1. When ACMPHS operation is enabled (HCMPON = COE = 1) but the noise filter is not in use (CDFS[1:0] = 00b), design the software so that the CMPMON bit is read twice and the values are only used after the two consecutive values match.

50.2.5 Comparator Output Control Register (CPIOC)

Address(es): ACMPHS0.CPIOC 4008 5010h, ACMPHS1.CPIOC 4008 5110h, ACMPHS2.CPIOC 4008 5210h, ACMPHS3.CPIOC 4008 5310h, ACMPHS4.CPIOC 4008 5410h, ACMPHS5.CPIOC 4008 5510h

	b7	b6	b5	b4	b3	b2	b1	b0
	VREFEN	—	—	—	—	—	—	CPOE
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	CPOE	Comparator Output Selection	0: Disable VCOUT pin output of the comparator (output signal is low) 1: Enable VCOUT pin output of the comparator.	R/W
b6 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	VREFEN	Internal Vref Enable*1	0: Disable internal Vref 1: Enable internal Vref.	R/W

Note 1. For ACMPHS modules 0 to 5, VREFEN exists only in ACMPHS0.CPIOC. When using the internal Vref in COMP0 to COMP5, set the VREFEN bit in ACMPHS0.CPIOC to 1. Bit [7] in ACMPHS1.CPIOC to ACMPHS5.CPIOC should be 0 regardless of whether or not the internal Vref is used.

50.3 Operation

The ACMPHS compares a reference voltage to an analog input voltage. Operation is not guaranteed when the values of registers are changed during ACMPHS operation. Table 50.3 shows the procedures for setting the registers associated with ACMPHS.

Table 50.3 Procedure for setting registers associated with ACMPHSn (n = 0 to 5) (1 of 2)

Step	Register	Bit	Setting
1	Associated MSTPCRD register	MSTPD28 to MSTPD23	0: Input clock supply.
2	Associated Port mn Pin Function Select register (PmnPFS)	ASEL	1: Select the function of pins IVREF and IVCMP.
3	ACMPHS0.CPIOC	VREFEN	1: When using the internal Vref.

6.清除IELSRn寄存器中的IR标志以清除中断状态。

Note 2. 详见表50.2。

50.2.4 比较器输出监控寄存器(CMPMON)

Address(es): ACMPHS0.CMPMON 4008 500Ch, ACMPHS1.CMPMON 4008 510Ch, ACMPHS2.CMPMON 4008 520Ch, ACMPHS3.CMPMON 4008 530Ch, ACMPHS4.CMPMON 4008 540Ch, ACMPHS5.CMPMON 4008 550Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	CMPMON
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	CMPMON	比较器输出监视器*1	0：比较器输出低1：比较器输出高。	R
b7 to b1	—	Reserved	这些位读为0。	R

Note 1. 当启用ACMPHS操作(HCMPON=COE=1)但未使用噪声滤波器(CDFS[1:0]=00b)时，设计软件以便CMPMON位被读取两次并且值仅在两个连续的值匹配。

50.2.5 比较器输出控制寄存器(CPIOC)

Address(es): ACMPHS0.CPIOC 4008 5010h, ACMPHS1.CPIOC 4008 5110h, ACMPHS2.CPIOC 4008 5210h, ACMPHS3.CPIOC 4008 5310h, ACMPHS4.CPIOC 4008 5410h, ACMPHS5.CPIOC 4008 5510h

	b7	b6	b5	b4	b3	b2	b1	b0
	VREFEN	—	—	—	—	—	—	CPOE
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	CPOE	比较器输出选择	0：禁止比较器的VCOUT引脚输出（输出信号为低电平）1：使能比较器的VCOUT引脚输出。	R/W
b6 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b7	VREFEN	Internal Vref Enable*1	0：禁用内部Vref1：启用内部Vref。	R/W

Note 1. 对于ACMPHS模块0到5，VREFEN仅存在于ACMPHS0.CPIOC中。当使用COMP0到COMP5的内部Vref时，将ACMPHS0.CPIOC中的VREFEN位设置为1。无论是否使用内部Vref，ACMPHS1.CPIOC到ACMPHS5.CPIOC中的位[7]都应为0。

50.3 Operation

ACMPHS将参考电压与模拟输入电压进行比较。如果在ACMPHS操作期间更改寄存器的值，则无法保证操作。表50.3显示了设置与ACMPHS相关的寄存器的过程。

Table 50.3 设置与ACMPHSn相关的寄存器的过程（n=0到5）（1of2）

Step	Register	Bit	Setting
1	相关的MSTPCRD寄存器	MSTPD28 to MSTPD23	0：输入时钟电源。
2	关联端口mn引脚功能选择寄存器(PmnPFS)	ASEL	1：选择引脚IVREF和IVCMP的功能。
3	ACMPHS0.CPIOC	VREFEN	1：使用内部Vref时。

Table 50.3 Procedure for setting registers associated with ACMPHSn (n = 0 to 5) (2 of 2)

Step	Register	Bit	Setting
4	Associated D/A convertor		When using the D/A convertor, select in the register.
5	CMPSEL0, CMPSEL1	CMPSEL0 to CMPSEL3, CRVS0 to CRVS3	Select the ACMPHSn input, with 1 set in only one of the bits.
6	CMPCTL	CDFS[1:0], CEG1, CEG0, and CINV	Set up ACMPHSn control.
		HCMPON	1: Enable ACMPHSn operation.
7	Waiting for the ACMPHS stabilization time (minimum 300 ns).		
8	CMPCTL	COE	1: Enable ACMPHSn output.
9	CPIOC	CPOE	Set the VCOUT output
	Associated Port mn Pin Function Select register (PmnPFS)	PSEL, PMR	Select the VCOUT port function.
10	IELSRn	IR, IELS[8:0]	When using an interrupt, select the interrupt status flag and the ICU event link.*1
11	ELSRn	ELS[8:0]	When using an ELC, select the event link.*2
12	Operation started		
13	CMPCTL	COE	0: When changing IVREF or IVCMP, to disable ACMPHSn output.
14	CMPSEL1	CRVS0 to CRVS3	Change the CMPSEL1 bits as follows: 1. Set bits CMPSEL1 to 0000 0000b. 2. Set a new value to the CMPSEL1 bits, with 1 set in only one of the bits.
	CMPSEL0	CMPSEL0 to CMPSEL3	Change the CMPSEL0 bits as follows: 1. Set bits CMPSEL0 to 0000 0000b. 2. Set a new value to the CMPSEL0 bits, with 1 set in only one of the bits.
15	Waiting for the ACMPHS switching stabilization time (minimum 200 ns).		
16	CMPCTL	COE	1: Enable ACMPHSn output.
17	Operation restarted		

Note 1. After ACMPHSn is set, an unnecessary interrupt might occur until operation becomes stable, so initialize the interrupt flag.
Note 2. After ACMPHSn is set, an unnecessary interrupt might occur until operation becomes stable, so initialize the event link select.

Figure 50.2 shows an example of ACMPHS operation. The VCOUT output becomes 1 when the analog input voltage is higher than the ACMPHS reference input voltage, and the VCOUT output becomes 0 when the analog input voltage is lower than the reference voltage. When the ACMPHS output changes, an interrupt request and an ELC event are output.

Table 50.3 设置与ACMPHSn相关的寄存器的过程（n=0到5）（2之2）

Step	Register	Bit	Setting
4	Associated D/A convertor		使用DA转换器时，在寄存器中选择。
5	CMPSEL0, CMPSEL1	CMPSEL0 to CMPSEL3, CRVS0 to CRVS3	选择ACMPHSn输入，仅其中一位设置为1。
6	CMPCTL	CDFS[1:0], CEG1, CEG0, and CINV	设置ACMPHSn控制。
		HCMPON	1：使能ACMPHSn操作。
7	等待ACMPHS稳定时间（最少300ns）。		
8	CMPCTL	COE	1：使能ACMPHSn输出。
9	CPIOC	CPOE	设置VCOUT输出
	关联端口mn引脚功能 选择寄存器(PmnPFS)	PSEL, PMR	选择VCOUT端口功能。
10	IELSRn	IR, IELS[8:0]	使用中断时，选择中断状态标志和ICU事件链接。*1
11	ELSRn	ELS[8:0]	使用ELC时，请选择事件链接。*2
12	操作开始		
13	CMPCTL	COE	0：改变IVREF或IVCMP时，禁用ACMPHSn输出。
14	CMPSEL1	CRVS0 to CRVS3	如下更改CMPSEL1位：1.将CMPSEL1位设置为00000000b。2.为CMPSEL1位设置一个新值，其中一个位设置为1。
	CMPSEL0	CMPSEL0 to CMPSEL3	如下更改CMPSEL0位：1.将CMPSEL0位设置为00000000b。2.为CMPSEL0位设置一个新值，其中一个位设置为1。
15	等待ACMPHS开关稳定时间（最少200ns）。		
16	CMPCTL	COE	1：使能ACMPHSn输出。
17	操作重新开始		

Note 1. 设置ACMPHSn后，可能会发生不必要的中断，直到运行稳定为止，因此请初始化中断标志。
Note 2. 设置ACMPHSn后，在操作稳定之前可能会发生不必要的中断，因此初始化事件链接选择。

图50.2显示了ACMPHS操作的示例。当模拟输入电压高于ACMPHS参考输入电压时，VCOUT输出变为1，当模拟输入电压低于参考电压时，VCOUT输出变为0。当ACMPHS输出改变时，会输出一个中断请求和一个ELC事件。

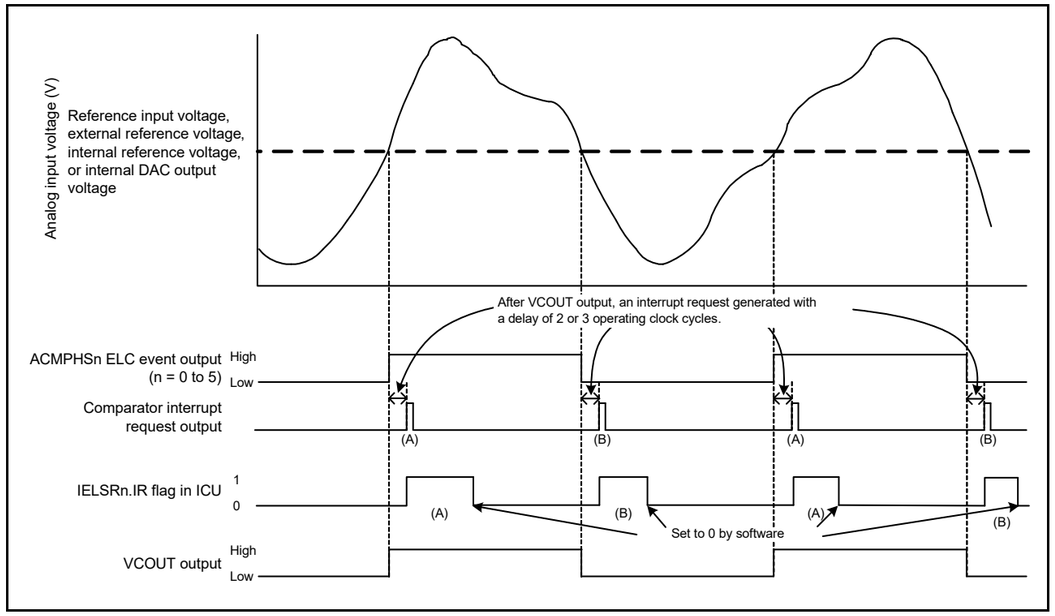


Figure 50.2 ACMPHS operation example

Figure 50.2 applies when CPOE = 1 (pin output enabled), CDFS[1:0] = 00b (filter not used), and CEG1 = CEG0 = 1 (both-edge detection selected). When CINV = 0, CEG0 = 1, and CEG1 = 0 (rising-edge detection selected for non-inversion output signal from the ACMPHS), the IELSR.IR flag changes as shown by (A) only. When CINV = 0, CEG0 = 0, and CEG1 = 1 (falling-edge detection selected for non-inversion output signal from the ACMPHS), the IR flag changes as shown by (B) only. When CPOE = 1, VCOUT directly outputs the ELC event output.

50.4 Noise Filter

The ACMPHS contains a noise filter. The sampling clock can be selected in the CMPCTL.CDFS[1:0] bits. The ACMPHS signal is sampled every sampling clock, and if the same value is sampled three times, the noise filter output at the next sampling clock cycle is used as the ACMPHS output.

Figure 50.3 shows the configuration of the noise filter and edge detector, and Figure 50.4 shows an example of noise filter and interrupt operation.

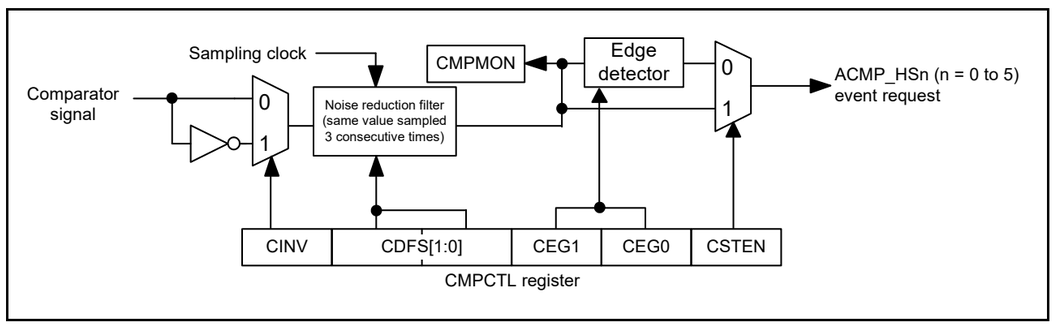


Figure 50.3 Noise filter and edge detection configuration

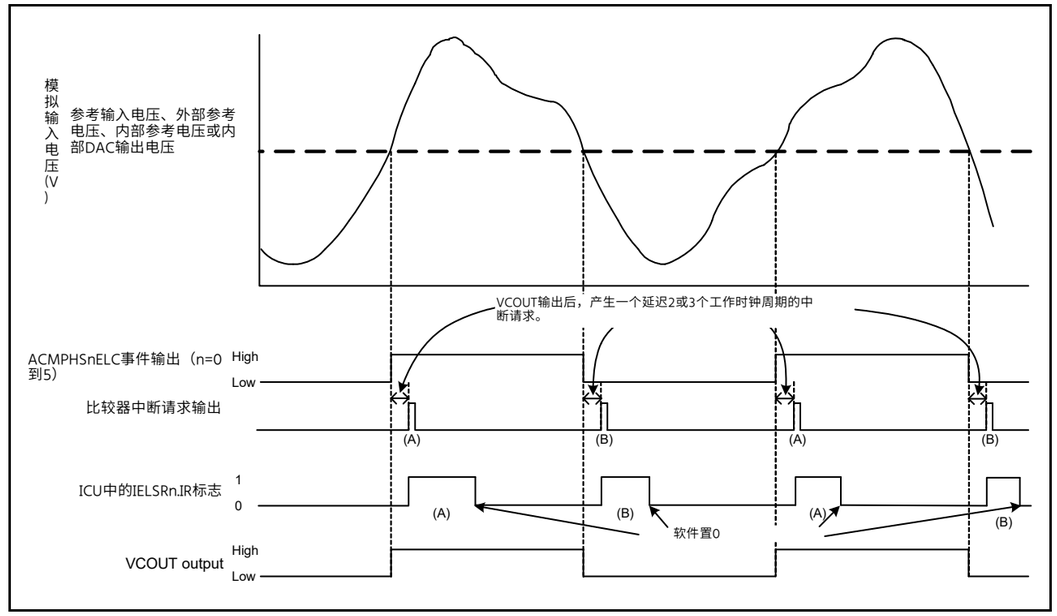


Figure 50.2 ACMPHS操作示例

图50.2适用于CPOE=1（使能引脚输出）、CDFS[1:0]=00b（未使用滤波器）和CEG1=CEG0=1（选择双沿检测）时。当CINV=0、CEG0=1和CEG1=0（为来自ACMPHS的同相输出信号选择上升沿检测）时，IELSR.IR标志仅如(A)所示变化。当CINV=0、CEG0=0和CEG1=1（为来自ACMPHS的非反相输出信号选择下降沿检测）时，IR标志仅如(B)所示变化。当CPOE=1时，VCOUT直接输出ELC事件输出。

50.4 噪声过滤器

ACMPHS包含一个噪声滤波器。可以在CMPCTL.CDFS[1:0]位中选择采样时钟。这
每个采样时钟对ACMPHS信号进行采样，如果采样3次相同的值，则将下一个采样时钟周期的噪声滤波器输出作为ACMPHS输出。

图50.3显示了噪声滤波器和边缘检测器的配置，图50.4显示了噪声滤波器和中断操作的示例。

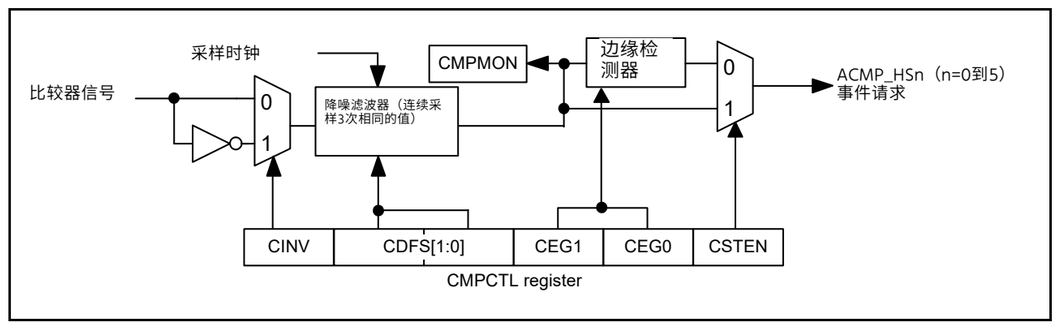


Figure 50.3 噪声过滤器和边缘检测配置

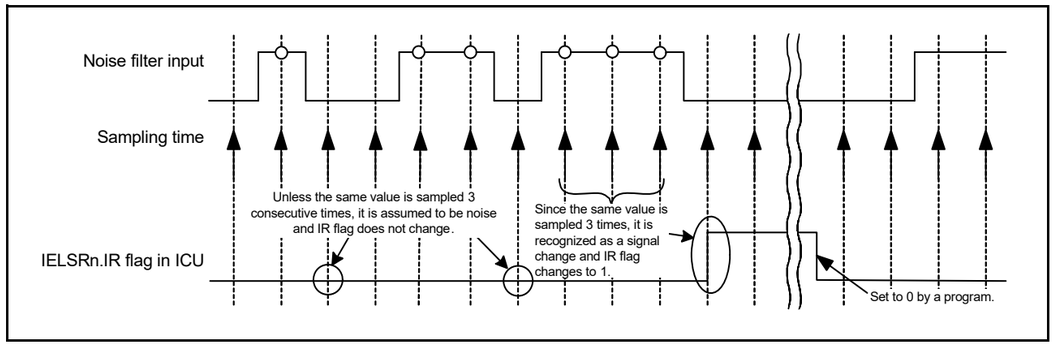


Figure 50.4 Noise filter and interrupt operation example

The operation example in Figure 50.4 applies when the CMPCTL.CDFS[1:0] bits are 01b, 10b, or 11b (noise filter used).

50.5 ACMPHS Interrupts

The ACMPHS generates six interrupt requests from sources ACMPHS0 to ACMPHS5. To use an ACMPHS interrupt, select it in the IELSR register in the Interrupt Controller Unit (ICU). Select the interrupt request in the CMPCTL.CSTEN bit, either through the edge selector, or not.

When using the ACMPHS interrupt through the edge selector, set at least one of the CMPCTL.CEG0 and CMPCTL.CEG1 bits to 1 (to a value other than 00b for no edge selection). In most cases, set the CMPCTL.CSTEN bit to 0 (output through the edge selector). Setting this bit to 1 is only permitted to release Software Standby or Snooze mode.

To use the ACMPHS interrupt in Software Standby or Snooze mode, set the CMPCTL.CSTEN bit to 1 (direct output), set the CMPCTL.CDFS[1:0] bits to 00b (digital noise filter not used), and set CMPCTL.CINV as follows:

- When detecting compare result 0 to 1, set CMPCTL.CINV to 0 (comparator output not inverted)
- When detecting compare result 1 to 0, set CMPCTL.CINV to 1 (comparator output inverted).

An ACMPHS0 interrupt request can be used to release Software Standby or Snooze modes. (ACMPHS1 to ACMPHS5 cannot be used.)

For details on the register settings related to ACMPHS interrupt requests, see section 50.2.1, Comparator Control Register (CMPCTL).

50.6 ACMPHS Output to the Event Link Controller (ELC)

The ELC uses the ACMPHS interrupt request signal as an ELC event signal, enabling link operation for the preset module. To use the ACMPHS ELC event, select them in the ELSRn register in the ELC. When using the ELC event request, set the CMPCTL.CSTEN bit to 0 (output through the edge selector). Also set at least one of the CMPCTL.CEG0 and CMPCTL.CEG1 bits to 1 (to a value other than 00b for no edge selection).

50.7 ACMPHS Pin Output

The comparison result from the ACMPHS can be output to external pins. Use the CMPCTL.CINV and CPIOC.CPOE bits to set the output polarity (non-inverted or inverted output) and enable or disable output. To output the ACMPHS comparison result to the VCOUT output pin, set the associated Port mn Pin Function Select register (PmnPFS) in the I/O register.

50.8 Usage Notes

50.8.1 Settings for the Module-Stop Function

ACMPHS operation can be disabled or enabled using the Module Stop Control Register. The ACMPHS is initially stopped after reset. Releasing the module-stop state enables access to the registers. For details, see section 11, Low Power Modes.

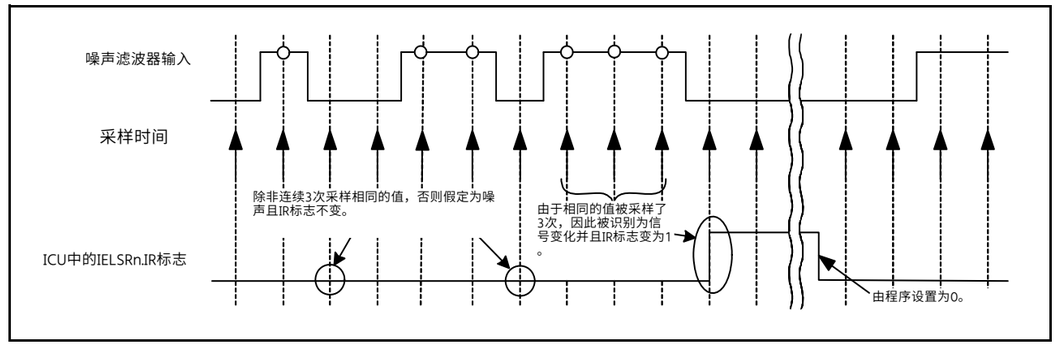


Figure 50.4 噪声滤波器和中断操作示例

图50.4中的操作示例适用于CMPCTL.CDFS[1:0]位为01b、10b或11b（使用噪声滤波器）时。

50.5 ACMPHS Interrupts

ACMPHS从源ACMPHS0到ACMPHS5产生六个中断请求。要使用ACMPHS中断，请在中断控制器单元(ICU)的IELSR寄存器中选择它。通过边沿选择器选择CMPCTL.CSTEN位中的中断请求，或者不选择。

通过边沿选择器使用ACMPHS中断时，至少设置CMPCTL.CEG0和CMPCTL.CEG1位为1（为00b以外的值，无边沿选择）。在大多数情况下，将CMPCTL.CSTEN位设置为0（通过边沿选择器输出）。将该位设置为1仅允许释放软件待机或贪睡模式。

要在软件待机或贪睡模式下使用ACMPHS中断，请将CMPCTL.CSTEN位设置为1（直接输出），将CMPCTL.CDFS[1:0]位设置为00b（未使用数字噪声滤波器），然后设置CMPCTL。CINV如下：

- 检测比较结果0到1时，设置CMPCTL.CINV为0（比较器输出不反相）
- 当检测到比较结果1到0时，将CMPCTL.CINV设置为1（比较器输出反转）。

ACMPHS0中断请求可用于释放软件待机或贪睡模式。（不能使用ACMPHS1到ACMPHS5。）

有关与ACMPHS中断请求相关的寄存器设置的详细信息，请参见第50.2.1节，比较器控制Register (CMPCTL).

50.6 ACMPHS输出到事件链接控制器(ELC)

ELC使用ACMPHS中断请求信号作为ELC事件信号，为预设模块启用链接操作。要使用ACMPHSELC事件，请在ELC的ELSRn寄存器中选择它们。使用ELC事件请求时，将CMPCTL.CSTEN位设置为0（通过边沿选择器输出）。还要将CMPCTL.CEG0和CMPCTL.CEG1位中的至少一个设置为1（设置为00b以外的值以不进行边沿选择）。

50.7 ACMPHS引脚输出

ACMPHS的比较结果可以输出到外部引脚。使用CMPCTL.CINV和CPIOC.CPOE位设置输出极性（非反相或反相输出）并启用或禁用输出。要将ACMPHS比较结果输出到VCOUT输出引脚，请在IO寄存器中设置相关的端口mn引脚功能选择寄存器(PmnPFS)。

50.8 使用说明

50.8.1 模块停止功能的设置

可以使用模块停止控制寄存器禁用或启用ACMPHS操作。ACMPHS在复位后最初停止。释放模块停止状态可以访问寄存器。有关详细信息，请参阅第11节，低功耗模式。

50.8.2 Relationship with the ADC12

Constraints apply on the simultaneous use of ACMPHS analog input and ADC12 analog input. For details, see section 47, Relationship between ADC12 Units 0 and 1 and the ACMPHS.

50.8.2 与ADC12的关系

同时使用ACMPHS模拟输入和ADC12模拟输入有一些限制。有关详细信息，请参阅第47节，ADC12单元0和1与ACMPHS之间的关系。

51. Capacitive Touch Sensing Unit (CTSU)

51.1 Overview

The Capacitive Touch Sensing Unit (CTSU) measures the electrostatic capacitance of the touch sensor. Changes in the electrostatic capacitance are determined by software that enables the CTSU to detect whether a finger is in contact with the touch sensor. The electrode surface of the touch sensor is usually enclosed with an electrical insulator so that a finger does not come into direct contact with the electrode.

As Figure 51.1 shows, electrostatic capacitance (parasitic capacitance) exists between the electrode and the surrounding insulators. Because the human body is an electrical conductor, when a finger is placed close to the electrode, the value of electrostatic capacitance increases.

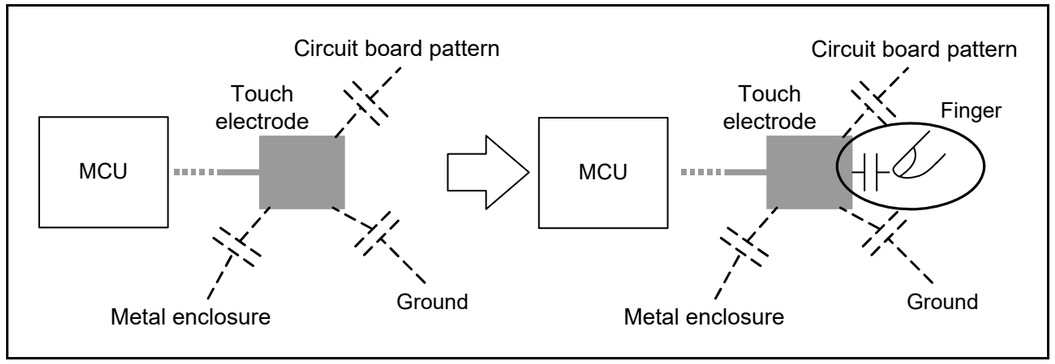


Figure 51.1 Increased electrostatic capacitance because of the presence of a finger

Electrostatic capacitance is detected by the self-capacitance and mutual capacitance methods. In the self-capacitance method, the CTSU detects electrostatic capacitance generated between a finger and a single electrode. In the mutual capacitance method, two electrodes are used as a transmit electrode and a receive electrode, and the CTSU detects the change in the electrostatic capacitance generated between the two when a finger is placed close to them.

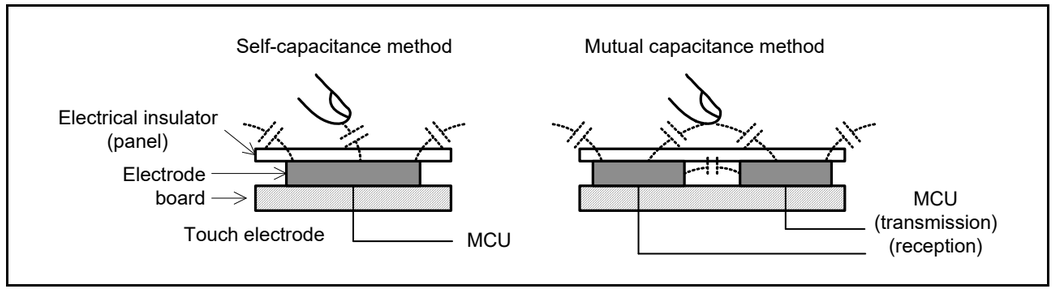


Figure 51.2 Self-capacitance and mutual capacitance methods

Electrostatic capacitance is measured by counting a clock signal whose frequency changes according to the amount of charged or discharged current, for a specified period. For details on the measurement principles of the CTSU, see section 51.3.1, Principles of Measurement Operation. Table 51.1 lists the CTSU specifications and Figure 51.3 shows a block diagram.

Table 51.1 CTSU specifications (1 of 2)

Parameter	Specifications
Operating clock	PCLKB, PCLKB/2, or PCLKB/4

51. 电容式触控感应单元(CTSU)

51.1 Overview

电容式触摸传感单元(CTSU)测量触摸传感器的静电电容。静电电容的变化由软件确定，该软件使CTSU能够检测手指是否与触摸传感器接触。触摸传感器的电极表面通常被电绝缘体包围，因此手指不会直接接触电极。

如图51.1所示，静电电容（寄生电容）存在于电极和周围绝缘体之间。因为人体是电导体，当手指靠近电极时，静电电容值会增加。

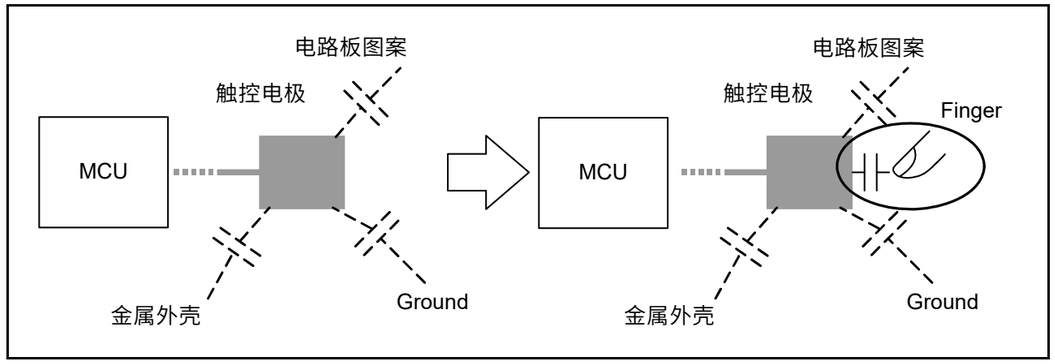


Figure 51.1 由于手指的存在而增加了静电电容

静电电容的检测方法有自电容法和互电容法。在自电容法中，CTSU检测手指和单个电极之间产生的静电电容。在互电容法中，两个电极用作发送电极和接收电极，当手指靠近它们时，CTSU会检测两者之间产生的静电电容的变化。

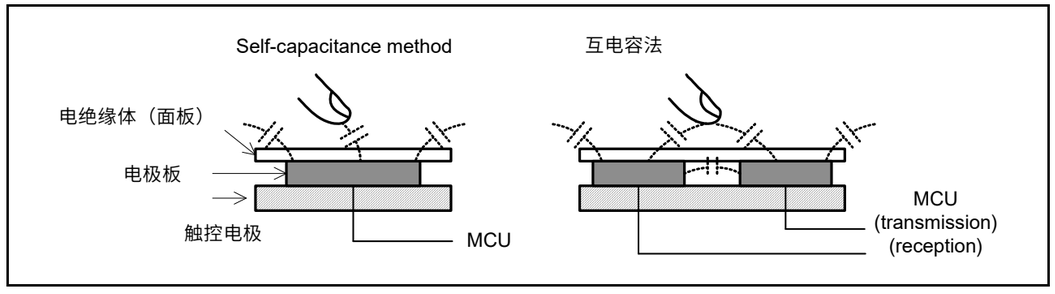


Figure 51.2 自电容和互电容方法

静电电容是通过对时钟信号进行计数来测量的，该时钟信号的频率根据充电或放电电流的大小而变化，在指定的时间段内。有关CTSU测量原理的详细信息，请参见第51.3.1节“测量操作原理”。表51.1列出了CTSU规格，图51.3显示了框图。

Table 51.1 CTSU规格(1of2)

Parameter	Specifications
工作时钟	PCLKB, PCLKB/2, or PCLKB/4

Table 51.1 CTSU specifications (2 of 2)

Parameter		Specifications
Pins	Electrostatic capacitance measurement	18 channels (TS00 to TS17)
	TSCAP	Low Pass Filter (LPF) connection pin
Measurement modes	Self-capacitance single scan mode	Electrostatic capacitance is measured on one channel using the self-capacitance method
	Self-capacitance multiscan mode	Electrostatic capacitance is measured successively on multiple channels using the self-capacitance method
	Mutual capacitance full scan mode	Electrostatic capacitance is measured successively on multiple channels using the mutual capacitance method
Noise prevention		Synchronous noise prevention, high-pass noise prevention
Measurement start conditions		• Software trigger • External trigger (ELC_CTSU from the Event Link Controller (ELC))

As Figure 51.3 shows, the CTSU consists of a status control block, trigger control block, clock control block, channel control block, port control block, sensor drive pulse generator, measurement block, interrupt block, and I/O registers.

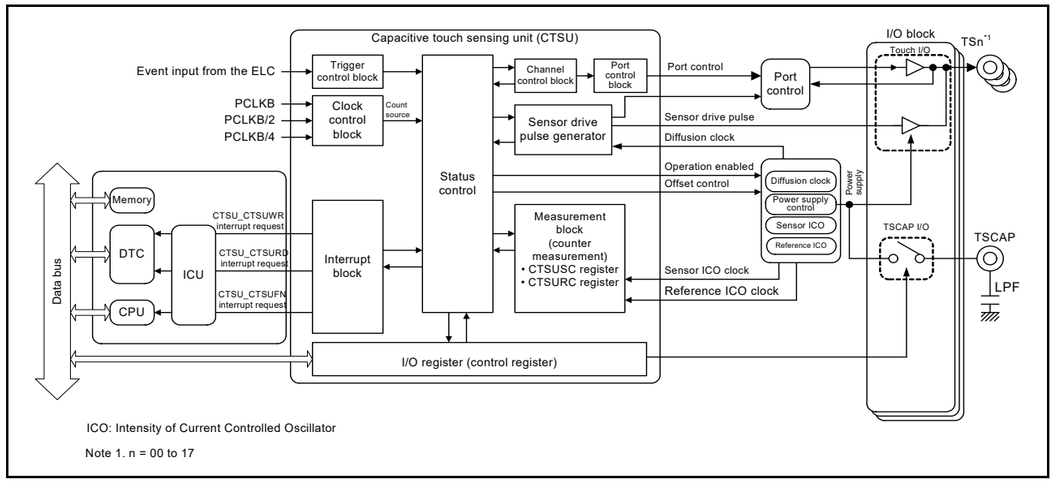


Figure 51.3 CTSU block diagram

Table 51.2 CTSU I/O pins

Pin name	I/O	Function
TS00 to TS17	Input	Electrostatic capacitive measurement pins (touch pins)
TSCAP	-	LPF connection pin

Table 51.1 CTSU规格（2个中的2个）

Parameter		Specifications
Pins	静电电容测量	18通道（TS00至TS17）
	TSCAP	低通滤波器(LPF)连接引脚
测量模式	自电容单次扫描模式	使用自电容法在一个通道上测量静电电容
	Self-capacitance multiscan mode	使用自电容法在多个通道上连续测量静电电容
	互电容全扫描模式	使用互电容法在多个通道上连续测量静电电容
噪音预防		同步防噪、防高通防噪
测量开始条件		软件触发 外部触发（来自事件链接控制器(ELC)的ELC_CTSU）

如图51.3所示，CTSU由状态控制块、触发控制块、时钟控制块、通道控制块、端口控制块、传感器驱动脉冲发生器、测量块、中断块和IO寄存器组成。

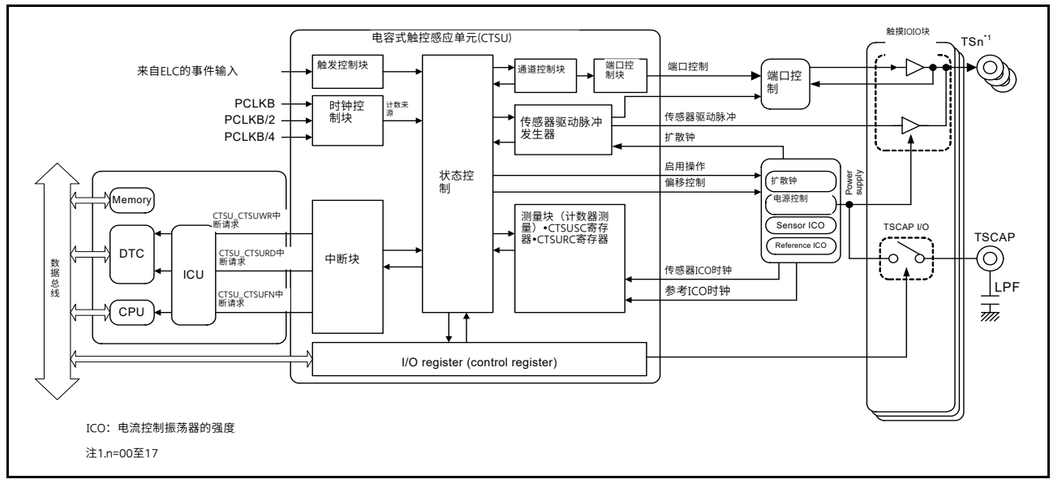


Figure 51.3 CTSU框图

Table 51.2 CTSU I/O pins

引脚名称	I/O	Function
TS00 to TS17	Input	静电电容测量引脚（触摸引脚）
TSCAP	-	LPF连接引脚

51.2 Register Descriptions

51.2.1 CTSU Control Register 0 (CTSUCR0)

Address(es): CTSU.CTSUCR0 4008 1000h

	b7	b6	b5	b4	b3	b2	b1	b0
	CTSUTXVSEL	—	—	CTSUINIT	—	CTSUSNZ	CTSUCAP	CTSUSTRT
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	CTSUSTRT	CTSU Measurement Operation Start	0: Stop measurement operation*1 1: Start measurement operation.	R/W
b1	CTSUCAP	CTSU Measurement Operation Start Trigger Select	0: Software trigger 1: External trigger.	R/W
b2	CTSUSNZ	CTSU Wait State Power-Saving Enable	0: Disable power-saving function during wait state 1: Enable power-saving function during wait state.	R/W
b3	—	Reserved	This bit read as 0. The write value should be 0.	R/W
b4	CTSUINIT	CTSU Control Block Initialization	Writing 1 to this bit initializes the CTSU control block and CTSUSC, CTSURC, CTSUMCH0, CTSUMCH1, and CTSUST registers. This bit is read as 0.	W
b6, b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b7	CTSUTXVSEL	CTSU Transmission Power Supply Select	0: VCC selected 1: Internal logic power supply selected.	R/W

Note 1. When the CTSU is not used, set the value of this bit to 0.

Only set the CTSUCAP and CTSUSNZ bits when the CTSUSTRT bit is 0. These bits can be set at the same time that measurement operation starts.

CTSUSTRT bit (CTSU Measurement Operation Start)

The CTSUSTRT bit specifies whether CTSU operation starts or stops. When the CTSUCAP bit is 0, measurement starts when the software writes 1 to the CTSUSTRT bit (software trigger) and stops when the hardware clears the CTSUSTRT bit to 0. When the CTSUCAP bit is 1, the CTSU waits for an external trigger by writing 1 to the CTSUSTRT bit, and measurement starts on the rising edge of the external trigger. When measurement is stopped, the CTSU waits for the next external trigger and operation continues.

Table 51.3 lists the CTSU states.

Table 51.3 CTSU states

CTSUSTRT bit	CTSUCAP bit	CTSU state
0	0	Stopped
0	1	Stopped
1	0	Measurement in progress
1	1	Measurement in progress and waiting for an external trigger*1

Note 1. The state can be read from the CTSUST.CTSUSTC[2:0] flags as follows:
During measurement: CTSUST.CTSUSTC[2:0] flags ≠ 000b
While waiting for an external trigger: CTSUST.CTSUSTC[2:0] flags = 000b

If the software sets the CTSUSTRT bit to 1 when the bit is already 1, the write is ignored and operation continues. To force operation to stop through the software when the CTSUSTRT bit is 1, set the CTSUSTRT bit to 0 and the CTSUINIT bit to 1 at the same time.

51.2 注册说明

51.2.1 CTSU控制寄存器0(CTSUCR0)

Address(es): CTSU.CTSUCR0 4008 1000h

	b7	b6	b5	b4	b3	b2	b1	b0
	CTSUTXVSEL	—	—	CTSUINIT	—	CTSUSNZ	CTSUCAP	CTSUSTRT
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	CTSUSTRT	CTSU测量操作 Start	0：停止测量操作*11：开始测量操作。	R/W
b1	CTSUCAP	CTSU测量操作 开始触发选择	0：软件触发1： 外部触发。	R/W
b2	CTSUSNZ	CTSU等待状态省电 Enable	0：等待状态下禁用省电功能1：等待状态下启用省电功能。	R/W
b3	—	Reserved	该位读为0。写入值应为0。	R/W
b4	CTSUINIT	CTSU控制块 Initialization	向该位写入1初始化CTSU控制块并CTSUSC, CTSURC, CTSUMCH0, CTSUMCH1, and CTSUST注册。该位读为0。	W
b6, b5	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b7	CTSUTXVSEL	CTSU传输功率 供应选择	0：选择VCC1：选择内部逻辑电源。	R/W

Note 1. 不使用CTSU时，将该位的值设为0。

仅当CTSUSTRT位为0时设置CTSUCAP和CTSUSNZ位。这些位可以在测量操作开始的同时设置。

CTSUSTRT位（CTSU测量操作开始）

CTSUSTRT位指定CTSU操作是开始还是停止。当CTSUCAP位为0时，软件将1写入CTSUSTRT位（软件触发）时开始测量，并在硬件将CTSUSTRT位清为0时停止测量。当CTSUCAP位为1时，CTSU通过写入等待外部触发1到CTSUSTRT位，并在外部触发的上升沿开始测量。当测量停止时，CTSU等待下一个外部触发并继续操作。

表51.3列出了CTSU状态。

Table 51.3 CTSU states

CTSUSTRT bit	CTSUCAP bit	CTSU state
0	0	Stopped
0	1	Stopped
1	0	测量中
1	1	正在进行测量并等待外部触发*1

Note 1. 可以从CTSUST.CTSUSTC[2:0]标志读取状态，如下所示：
测量期间：CTSUST.CTSUSTC[2:0]flags≠000b
等待外部触发时：CTSUST.CTSUSTC[2:0]flags=000b

如果在CTSUSTRT位已经为1时软件将该位设置为1，则忽略写入并继续操作。要在CTSUSTRT位为1时通过软件强制停止操作，请将CTSUSTRT位设置为0，同时将CTSUINIT位设置为1。

CTSUCAP bit (CTSU Measurement Operation Start Trigger Select)

The CTSUCAP bit specifies the measurement start condition. For details, see CTSUSTRT bit (CTSU Measurement Operation Start).

CTSUSNZ bit (CTSU Wait State Power-Saving Enable)

The CTSUSNZ bit enables or disables power-saving operation during a wait state. It can also suspend the CTSU power supply, which decreases power consumption during the wait state. In the suspended state, the CTSU power supply is turned off while the external TSCAP is still charged.

Table 51.4 shows the CTSU power supply state control.

Table 51.4 CTSU power supply state control

CTSUCR1.CTSUPON bit	CTSUSNZ bit	CTSUCAP bit	CTSUSTRT bit	CTSU power supply state
0	0	0	0	Stopped
1	0	—	—	Operating
1	1	0	0	Suspended

Note: Other settings are prohibited.

To start measurement from the suspended state, set the CTSUSNZ bit to 0, and then set the CTSUSTRT bit to 1. To suspend the module after measurement stops, set the CTSUSNZ bit to 1.

CTSUINIT bit (CTSU Control Block Initialization)

Write 1 to the CTSUINIT bit to initialize the internal control registers. To force the current operation to stop, set the CTSUSTRT bit to 0 and the CTSUINIT bit to 1 at the same time. This stops the operation and initializes the internal control registers.

Do not write 1 to the CTSUINIT bit when the CTSUSTRT bit is 1.

CTSUTXVSEL bit (CTSU Transmission Power Supply Select)

This bit is used to switch the power supply for the transmit buffer in mutual capacitance full scan mode. Set this bit to 0 for any other mode or when the VCC voltage is lower than 2.7 V. This bit switches the power supply for touch I/O which is set for transmission by the CTSUCHTRCn registers. Table 51.5 lists the power supply for TSm pin. When the VCC voltage fluctuates greatly due to the switching of the output buffer, switching to the internal logic power supply can reduce the effect on the voltage fluctuation.

Table 51.5 Power supplied to the TSm pins

Setting of CTSUCHTRCn Register	CTSUTXVSEL bit	Power supply of TSm pins
0 (Reception)	*	VCC
1 (Transmission)	0 (VCC)	
	1 (Internal logic power supply)	Internal logic power supply

CTSUCAP位（CTSU测量操作开始触发选择）

CTSUCAP位指定测量开始条件。有关详细信息，请参阅CTSUSTRT位（CTSU测量
Operation Start).

CTSUSNZ位（CTSU等待状态省电使能）

CTSUSNZ位在等待状态期间启用或禁用省电操作。它还可以暂停CTSU电源，从而降低等待状态下的功耗。在挂起状态下，CTSU电源关闭，而外部TSCAP仍在充电。

表51.4显示了CTSU电源状态控制。

Table 51.4 CTSU电源状态控制

CTSUCR1.CTSUPON bit	CTSUSNZ bit	CTSUCAP bit	CTSUSTRT bit	CTSU供电状态
0	0	0	0	Stopped
1	0	—	—	Operating
1	1	0	0	Suspended

Note: 禁止其他设置。

要从暂停状态开始测量，请将CTSUSNZ位设置为0，然后将CTSUSTRT位设置为1。要在测量停止后暂停模块，请将CTSUSNZ位设置为1。

CTSUINIT位（CTSU控制块初始化）

向CTSUINIT位写入1以初始化内部控制寄存器。要强制停止当前操作，同时将CTSUSTRT位设置为0并将CTSUINIT位设置为1。这将停止操作并初始化内部控制寄存器。

当CTSUSTRT位为1时，不要将1写入CTSUINIT位。

CTSUTXVSEL位（CTSU发射电源选择）

该位用于切换互电容全扫描模式下发送缓冲器的电源。对于任何其他模式或当VCC电压低于2.7V时，将该位设置为0。该位切换由CTSUCHTRn寄存器设置为发送的触摸IO的电源。表51.5列出了TSm引脚的电源。当VCC电压由于输出缓冲器的切换而波动很大时，切换到内部逻辑电源可以减少对电压波动的影响。

Table 51.5 为TSm引脚供电

CTSUCHTRn寄存器的设置	CTSUTXVSEL bit	TSm管脚电源
0 (Reception)	*	VCC
1 (Transmission)	0 (VCC)	
	1（内部逻辑电源）	内部逻辑电源

51.2.2 CTSU Control Register 1 (CTSUCR1)

Address(es): CTSU.CTSUCR1 4008 1001h

	b7	b6	b5	b4	b3	b2	b1	b0
	CTSUMD[1:0]		CTSUCLK[1:0]		CTSUATUNE1	—	CTSUCSW	CTSUPON
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	CTSUPON	CTSU Power Supply Enable	0: Power off the CTSU 1: Power on the CTSU.	R/W
b1	CTSUCSW	CTSU LPF Capacitance Charging Control	This bit controls charging of the LPF capacitance connected to the TSCAP pin. 0: Turn off capacitance switch 1: Turn on capacitance switch.	R/W
b2	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b3	CTSUATUNE1	CTSU Power Supply Capacity Adjustment	0: Normal output 1: High-current output.	R/W
b5, b4	CTSUCLK[1:0]	CTSU Operating Clock Select	b5 b4 0 0: PCLKB 0 1: PCLKB/2 (PCLKB divided by 2) 1 0: PCLKB/4 (PCLKB divided by 4) 1 1: Setting prohibited.	R/W
b7, b6	CTSUMD[1:0]	CTSU Measurement Mode Select	b7 b6 0 0: Self-capacitance single scan mode 0 1: Self-capacitance multiscan mode 1 0: Setting prohibited 1 1: Mutual capacitance full scan mode.	R/W

Only set the CTSUCR1 register when the CTSUCR0.CTSUSTRT bit is 0.

CTSUPON bit (CTSU Power Supply Enable)

The CTSUPON bit controls the power supply to the CTSU. Set the CTSUPON and CTSUCSW bits to the same value.

CTSUCSW bit (CTSU LPF Capacitance Charging Control)

The CTSUCSW bit controls charging of the LPF capacitor connected to the TSCAP pin by turning the capacitance switch on or off. After the capacitance switch is turned on, wait until the capacitance connected to the TSCAP pin is charged for the specified time before starting measurement by setting CTSUCR0.CTSUSTRT to 1. Before starting measurement, use an I/O port to output low to the TSCAP pin, and discharge the existing LPF capacitance. Set the CTSUPON and CTSUCSW bits to the same value.

CTSUATUNE1 bit (CTSU Power Supply Capacity Adjustment)

The CTSUATUNE1 bit sets the capacity of the CTSU power supply. Normally, set this bit to 0.

CTSUCLK[1:0] bits (CTSU Operating Clock Select)

The CTSUCLK[1:0] bits select the operating clock.

CTSUMD[1:0] bits (CTSU Measurement Mode Select)

The CTSUMD[1:0] bits set the measurement mode. For details, see section 51.3.2, Measurement Modes.

51.2.2 CTSU控制寄存器1(CTSUCR1)

Address(es): CTSU.CTSUCR1 4008 1001h

	b7	b6	b5	b4	b3	b2	b1	b0
	CTSUMD[1:0]		CTSUCLK[1:0]		CTSUATUNE1	—	CTSUCSW	CTSUPON
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	CTSUPON	CTSU电源使能	0：CTSU断电1：CTSU上电。	R/W
b1	CTSUCSW	CTSULPF电容充电Control	该位控制连接到TSCAP引脚的LPF电容的充电。0：关闭电容开关1：打开电容开关。	R/W
b2	—	Reserved	该位读取为0。写入值应为0。	R/W
b3	CTSUATUNE1	CTSU电源容量Adjustment	0：正常输出1：大电流输出。	R/W
b5, b4	CTSUCLK[1:0]	CTSU工作时钟选择	b5 b4 0 0: PCLKB 0 1：PCLKB2（PCLKB除以2） 1 0：PCLKB4（PCLKB除以4） 1 1：禁止设置。	R/W
b7, b6	CTSUMD[1:0]	CTSU测量模式选择	b7 b6 0 0：自电容单扫描模式 0 1: Self-capacitance multiscan mode 1 0：禁止设定 1 1：互电容全扫描模式。	R/W

仅当CTSUCR0.CTSUSTRT位为0时设置CTSUCR1寄存器。

CTSUPON位（CTSU电源使能）

CTSUPON位控制CTSU的电源。将CTSUPON和CTSUCSW位设置为相同的值。

CTSUCSW位（CTSULPF电容充电控制）

CTSUCSW位通过打开或关闭电容开关来控制连接到TSCAP引脚的LPF电容的充电。电容开关打开后，通过将CTSUCR0.CTSUSTRT设置为1，等到连接到TSCAP引脚的电容充电指定时间后再开始测量。开始测量之前，使用IO端口向TSCAP引脚输出低电平，并对现有的LPF电容进行放电。将CTSUPON和CTSUCSW位设置为相同的值。

CTSUATUNE1位（CTSU电源容量调整）

CTSUATUNE1位设置CTSU电源的容量。通常，将此位设置为0。

CTSUCLK[1:0]位（CTSU工作时钟选择）

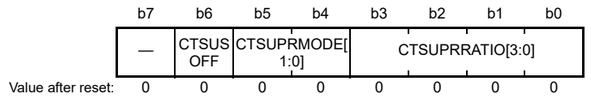
CTSUCLK[1:0]位选择工作时钟。

CTSUMD[1:0]位（CTSU测量模式选择）

CTSUMD[1:0]位设置测量模式。有关详细信息，请参阅第51.3.2节，测量模式。

51.2.3 CTSU Synchronous Noise Reduction Setting Register (CTSUSDPRS)

Address(es): CTSU.CTSUSDPRS 4008 1002h



Bit	Symbol	Bit name	Description	R/W
b3 to b0	CTSUPRRATIO[3:0]	CTSU Measurement Time and Pulse Count Adjustment	These bits set the measurement time and the measurement pulse count setting. Recommended setting: 3 (0011b).	R/W
b5, b4	CTSUPRMODE[1:0]	CTSU Base Period and Pulse Count Setting	These bits set the base pulse count. b5 b4 0 0: 510 pulses 0 1: 126 pulses 1 0: 62 pulses (recommended setting) 1 1: Setting prohibited.	R/W
b6	CTSUSOFF	CTSU High-Pass Noise Reduction Function Off Setting	This bit turns spectrum diffusion on or off to reduce high-pass noise. 0: Turn on 1: Turn off.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Only set the CTSUSDPRS register when the CTSUCR0.CTSUSTRT bit is 0.

CTSUPRRATIO[3:0] bits (CTSU Measurement Time and Pulse Count Adjustment)

The CTSUPRRATIO[3:0] bits are used to determine the measurement time and the measurement pulse count. These values are calculated using the following formulas, where the base pulse count is determined by the CTSUPRMODE[1:0] setting:

Measurement pulse count = base pulse count × (CTSUPRRATIO[3:0] bits + 1)
Measurement time = (base pulse count × (CTSUPRRATIO[3:0] bits + 1) + base pulse count - 2) × 0.25 × base clock cycle

Note: For details on the base clock cycle, see section 51.2.17, CTSU Sensor Offset Register 1 (CTSUSO1).

CTSUPRMODE[1:0] bits (CTSU Base Period and Pulse Count Setting)

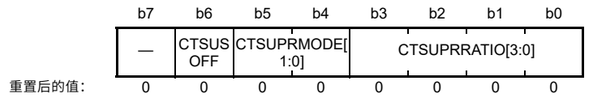
The CTSUPRMODE[1:0] bits select the number of base pulses that occur during measurement.

CTSUSOFF bit (CTSU High-Pass Noise Reduction Function Off Setting)

The CTSUSOFF bit turns on or off the function for reducing high-pass noise. Set this bit to 1 to turn the function off.

51.2.3 CTSU同步降噪设置寄存器(CTSUSDPRS)

Address(es): CTSU.CTSUSDPRS 4008 1002h



Bit	Symbol	位名称	Description	R/W
b3 to b0	CTSUPRRATIO[3:0]	CTSU测量时间和脉冲计数调整	这些位设置测量时间和测量脉冲计数设置。推荐设置：3(0011b)。	R/W
b5, b4	CTSUPRMODE[1:0]	CTSU基本周期和脉冲计数Setting	这些位设置基本脉冲计数。b5b4 0 0: 510 pulses 0 1: 126 pulses 1 0: 62 pulses (recommended setting) 1 1：禁止设置。	R/W
b6	CTSUSOFF	CTSU高通降噪功能关闭设置	该位打开或关闭频谱扩散以减少高通噪声。0：开启 1：关闭。	R/W
b7	—	Reserved	该位读取为0。写入值应为0。	R/W

仅当CTSUCR0.CTSUSTRT位为0时设置CTSUSDPRS寄存器。

CTSURRATIO[3:0]位（CTSU测量时间和脉冲计数调整）

CTSUPRRATIO[3:0]位用于确定测量时间和测量脉冲计数。这些值使用以下公式计算，其中基本脉冲计数由CTSUPRMODE[1:0]设置确定：

测量脉冲数=基本脉冲数×(CTSUPRRATIO[3:0]位+1)
测量时间=(基本脉冲计数×(CTSUPRRATIO[3:0]位+1)+基本脉冲计数2)×0.25×基本时钟周期

Note: 有关基本时钟周期的详细信息，请参见第51.2.17节，CTSU传感器偏移寄存器1(CTSUSO1)。

CTSUPRMODE[1:0]位（CTSU基本周期和脉冲计数设置）

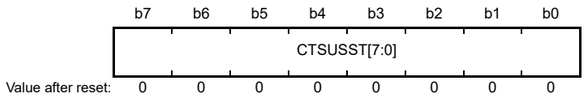
CTSUPRMODE[1:0]位选择测量期间出现的基本脉冲数。

CTSUSOFF位（CTSU高通降噪功能关闭设置）

CTSUSOFF位打开或关闭降低高通噪声的功能。将此位设置为1可关闭该功能。

51.2.4 CTSU Sensor Stabilization Wait Control Register (CTSUSST)

Address(es): CTSU.CTSUSST 4008 1003h



Bit	Symbol	Bit name	Description	R/W
b7 to b0	CTSUSST[7:0]	CTSU Sensor Stabilization Wait Control	Fix the value of these bits to 00010000b.	R/W

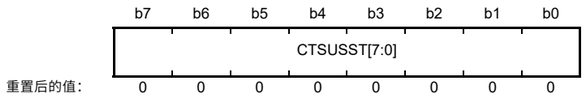
Only set the CTSUSST register when the CTSUCR0.CTSUSTRT bit is 0.

CTSUSST[7:0] bits (CTSU Sensor Stabilization Wait Control)

The CTSUSST[7:0] bits set the stabilization wait time for the TSCAP pin voltage. Always fix these bits to 00010000b. If these bits are not set, the TSCAP voltage will be unstable at the start of measurement, and the CTSU will be unable to obtain correct touch measurement results.

51.2.4 CTSU传感器稳定等待控制寄存器(CTSUSST)

Address(es): CTSU.CTSUSST 4008 1003h



Bit	Symbol	位名称	Description	R/W
b7 to b0	CTSUSST[7:0]	CTSU传感器稳定等待Control	将这些位的值固定为00010000b。	R/W

仅当CTSUCR0.CTSUSTRT位为0时设置CTSUSST寄存器。

CTSUSST[7:0]位（CTSU传感器稳定等待控制）

CTSUSST[7:0]位设置TSCAP引脚电压的稳定等待时间。始终将这些位固定为00010000b。如果未设置这些位，TSCAP电压将在测量开始时不稳定，CTSU将无法获得正确的触摸测量结果。

51.2.5 CTSU Measurement Channel Register 0 (CTSUMCH0)

Address(es): CTSU.CTSUMCH0 4008 1004h

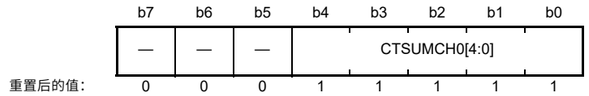
Bit	Symbol	Bit name	Description	R/W
b4 to b0	CTSUMCH0[4:0]	CTSU Measurement Channel 0	In self-capacitance single scan mode, these bits set the channel to be measured. b4 b0 0 0 0 0 0: TS00 0 0 0 0 1: TS01 0 0 0 1 0: TS02 0 0 0 1 1: TS03 0 0 1 0 0: TS04 0 0 1 0 1: TS05 0 0 1 1 0: TS06 0 0 1 1 1: TS07 0 1 0 0 0: TS08 0 1 0 0 1: TS09 0 1 0 1 0: TS10 0 1 0 1 1: TS11 0 1 1 0 0: TS12 0 1 1 0 1: TS13 0 1 1 1 0: TS14 0 1 1 1 1: TS15 1 0 0 0 0: TS16 1 0 0 0 1: TS17. Other than when specified, starting measurement operation by setting CTSUCR0.CTSUSTRT to 1 is prohibited after these bits are set. In other measurement modes, these bits indicate the channel that is currently being measured. b4 b0 0 0 0 0 0: TS00 0 0 0 0 1: TS01 0 0 0 1 0: TS02 0 0 0 1 1: TS03 0 0 1 0 0: TS04 0 0 1 0 1: TS05 0 0 1 1 0: TS06 0 0 1 1 1: TS07 0 1 0 0 0: TS08 0 1 0 0 1: TS09 0 1 0 1 0: TS10 0 1 0 1 1: TS11 0 1 1 0 0: TS12 0 1 1 0 1: TS13 0 1 1 1 0: TS14 0 1 1 1 1: TS15 1 0 0 0 0: TS16 1 0 0 0 1: TS17 1 1 1 1 1: Measurement is being stopped.	R/W*1
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Writing to these bits is only enabled in self-capacitance single scan mode (CTSUCR1.CTSUMD[1:0] bits = 00b).

Only set the CTSUMCH0 register when the CTSUCR0.CTSUSTRT bit is 0.

51.2.5 CTSU测量通道寄存器0(CTSUCH0)

Address(es): CTSU.CTSUMCH0 4008 1004h



Bit	Symbol	位名称	Description	R/W
b4 to b0	CTSUMCH0[4:0]	CTSU测量通道0	在自电容单次扫描模式下，这些位设置要测量的通道。b4b000000：TS0000001：TS0100010：TS0200011：TS0300100：TS0400101：TS0500110：TS0600111：TS0701000：TS0801001：TS0901010：TS1001011：TS1101100：TS1201101：TS1301110：TS1401111：TS1510000：TS1610001：TS17。除非指定，否则在设置这些位后禁止通过将CTSUCR0.CTSUSTRT设置为1来启动测量操作。 在其他测量模式下，这些位指示当前正在测量的通道。b4b000000：TS0000001：TS0100010：TS0200011：TS0300100：TS0400101：TS0500110：TS0600111：TS0701000：TS0801001：TS0901010：TS1001011：TS1101100：TS1201101：TS1301110：TS1401111：TS1510000：TS1610001：TS1711111：正在停止测量。	R/W*1
b7 to b5	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 只有在自电容单次扫描模式下才能写入这些位（CTSUCR1.CTSUMD[1:0]位=00b）。

仅当CTSUCR0.CTSUSTRT位为0时设置CTSUMCH0寄存器。

CTSUMCH0[4:0] bits (CTSU Measurement Channel 0)

In self-capacitance single scan mode, the CTSUMCH0[4:0] bits set the channel to be measured. In this mode, only specify enabled channels (00000b to 10001b). In other modes, these indicate the receive channel that is being measured, and writing to these bits has no effect.

51.2.6 CTSU Measurement Channel Register 1 (CTSUMCH1)

Address(es): CTSU.CTSUMCH1 4008 1005h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	CTSUMCH1[4:0]				
Value after reset:	0	0	0	1	1	1	1	1

Bit	Symbol	Bit name	Description	R/W
b4 to b0	CTSUMCH1[4:0]	CTSU Measurement Channel 1	b4 b0 0 0 0 0 0: TS00 0 0 0 0 1: TS01 0 0 0 1 0: TS02 0 0 0 1 1: TS03 0 0 1 0 0: TS04 0 0 1 0 1: TS05 0 0 1 1 0: TS06 0 0 1 1 1: TS07 0 1 0 0 0: TS08 0 1 0 0 1: TS09 0 1 0 1 0: TS10 0 1 0 1 1: TS11 0 1 1 0 0: TS12 0 1 1 0 1: TS13 0 1 1 1 0: TS14 0 1 1 1 1: TS15 1 0 0 0 0: TS16 1 0 0 0 1: TS17 1 1 1 1 1: Measurement is being stopped.	R
b7 to b5	—	Reserved	These bits are read as 0.	R

CTSUMCH1[4:0] bits (CTSU Measurement Channel 1)

In full scan mode, the CTSUMCH1[4:0] bits indicate the transmit channel that is being measured. They are always 11111b when measurement is stopped, or in self-capacitance single scan and multi-scan modes.

51.2.7 CTSU Channel Enable Control Register 0 (CTSUCHAC0)

Address(es): CTSU.CTSUCHAC0 4008 1006h

	b7	b6	b5	b4	b3	b2	b1	b0
	CTSUCHAC0[7:0]							
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	CTSUCHAC0[7:0]	CTSU Channel Enable Control 0	These bits select whether the associated TS pin is measured. 0: Do not measure 1: Measure. These bits specify the TS00 to TS07 pins.	R/W

Only set the CTSUCHAC0 register when the CTSUCR0.CTSUSTRT bit is 0.

CTSUCH0[4:0]位（CTSU测量通道0）

在自电容单次扫描模式下，CTSUMCH0[4:0]位设置要测量的通道。在此模式下，仅指定启用的通道（00000b到10001b）。在其他模式下，这些表示正在测量的接收通道，写入这些位无效。

51.2.6 CTSU测量通道寄存器1(CTSUCH1)

Address(es): CTSU.CTSUMCH1 4008 1005h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	CTSUMCH1[4:0]				
重置后的值：	0	0	0	1	1	1	1	1

Bit	Symbol	位名称	Description	R/W
b4 to b0	CTSUMCH1[4:0]	CTSU测量通道1	b4b000000：TS0000001：TS0100010：TS0200011：TS0300100：TS0400101：TS0500110：TS0600111：TS0701000：TS0801001：TS0901010：TS1001011：TS1101100：TS1201101：TS1301110：TS1401111：TS1510000：TS1610001：TS1711111：正在停止测量。	R
b7 to b5	—	Reserved	这些位读为0。	R

CTSUCH1[4:0]位（CTSU测量通道1）

在全扫描模式下，CTSUMCH1[4:0]位指示正在测量的发送通道。当测量停止时，它们始终为11111b，或者在自电容单扫描和多扫描模式下。

51.2.7 CTSU通道使能控制寄存器0(CTSUCHAC0)

Address(es): CTSU.CTSUCHAC0 4008 1006h

	b7	b6	b5	b4	b3	b2	b1	b0
	CTSUCHAC0[7:0]							
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b7 to b0	CTSUCHAC0[7:0]	CTSU通道使能控制0	这些位选择是否测量相关的TS引脚。0：不测量1：测量。这些位指定TS00到TS07引脚。	R/W

仅当CTSUCR0.CTSUSTRT位为0时设置CTSUCHAC0寄存器。

CTSUCHAC0[7:0] bits (CTSU Channel Enable Control 0)

The CTSUCHAC0[7:0] bits select the receive and transmit pins whose electrostatic capacitance is to be measured. CTSUCHAC0[0] is associated with TS00 and CTSUCHAC0[7] with TS07.

51.2.8 CTSU Channel Enable Control Register 1 (CTSUCHAC1)

Address(es): CTSU.CTSUCHAC1 4008 1007h

	b7	b6	b5	b4	b3	b2	b1	b0
	CTSUCHAC1[7:0]							
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	CTSUCHAC1[7:0]	CTSU Channel Enable Control 1	These bits select whether the associated TS pin is measured. 0: Do not measure 1: Measure. These bits specify the TS08 to TS15 pins.	R/W

Only set the CTSUCHAC1 register when the CTSUCR0.CTSUSTRT bit is 0.

CTSUCHAC1[7:0] bits (CTSU Channel Enable Control 1)

The CTSUCHAC1[7:0] bits select the receive and transmit pins whose electrostatic capacitance is to be measured. CTSUCHAC1[0] is associated with TS08 and CTSUCHAC1[7] with TS15.

51.2.9 CTSU Channel Enable Control Register 2 (CTSUCHAC2)

Address(es): CTSU.CTSUCHAC2 4008 1008h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	CTSUCHAC2 [1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1 to b0	CTSUCHAC2 [1:0]	CTSU Channel Enable Control 2	These bits select whether the associated TS pin is measured. 0: Do not measure 1: Measure. These bits specify the TS16 to TS17 pins.	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Only set the CTSUCHAC2 register when the CTSUCR0.CTSUSTRT bit = 0.

CTSUCHAC2 [1:0] bits (CTSU Channel Enable Control 2)

The CTSUCHAC2 [1:0] bits select the receive and transmit pins whose electrostatic capacitance is to be measured. CTSUCHAC2[0] is associated with TS16 and CTSUCHAC2[1] with TS17.

CTSUCHAC0[7:0]位（CTSU通道使能控制0）

CTSUCHAC0[7:0]位选择要测量其静电电容的接收和发送引脚。
CTSUCHAC0[0]与TS00相关联，CTSUCHAC0[7]与TS07相关联。

51.2.8 CTSU通道使能控制寄存器1(CTSUCHAC1)

Address(es): CTSU.CTSUCHAC1 4008 1007h

	b7	b6	b5	b4	b3	b2	b1	b0
	CTSUCHAC1[7:0]							
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b7 to b0	CTSUCHAC1[7:0]	CTSU通道使能控制1	这些位选择是否测量相关的TS引脚。0：不测量1：测量。这些位指定TS08到TS15引脚。	R/W

仅当CTSUCR0.CTSUSTRT位为0时设置CTSUCHAC1寄存器。

CTSUCHAC1[7:0]位（CTSU通道使能控制1）

CTSUCHAC1[7:0]位选择要测量其静电电容的接收和发送引脚。
CTSUCHAC1[0]与TS08相关联，CTSUCHAC1[7]与TS15相关联。

51.2.9 CTSU通道使能控制寄存器2(CTSUCHAC2)

Address(es): CTSU.CTSUCHAC2 4008 1008h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	CTSUCHAC2 [1:0]	
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b1 to b0	CTSUCHAC2 [1:0]	CTSU通道启用控制2	这些位选择是否测量相关的TS引脚。0：不测量1：测量。这些位指定TS16到TS17引脚。	R/W
b7 to b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W

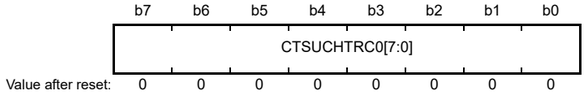
仅当CTSUCR0.CTSUSTRT位=0时设置CTSUCHAC2寄存器。

CTSUCHAC2[1:0]位（CTSU通道使能控制2）

CTSUCHAC2[1:0]位选择要测量其静电电容的接收和发送引脚。
CTSUCHAC2[0]与TS16相关联，CTSUCHAC2[1]与TS17相关联。

51.2.10 CTSU Channel Transmit/Receive Control Register 0 (CTSUCHTRC0)

Address(es): CTSU.CTSUCHTRC0 4008 100Bh



Bit	Symbol	Bit name	Description	R/W
b7 to b0	CTSUCHTRC0[7:0]	CTSU Channel Transmit/Receive Control 0	0: Reception 1: Transmission. These bits specify the TS00 to TS07 pins.	R/W

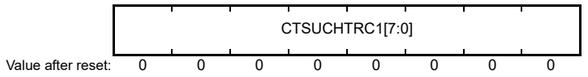
Only set the CTSUCHTRC0 register when the CTSUCR0.CTSUSTRT bit is 0.

CTSUCHTRC0[7:0] bits (CTSU Channel Transmit/Receive Control 0)

In full scan mode, the CTSUCHTRC0[7:0] bits allocate reception or transmission to the associated TS pins. The setting is ignored in self-capacitance single scan and multi-scan modes. CTSUCHTRC0[0] is associated with TS00 and CTSUCHTRC0[7] with TS07.

51.2.11 CTSU Channel Transmit/Receive Control Register 1 (CTSUCHTRC1)

Address(es): CTSU.CTSUCHTRC1 4008 100Ch



Bit	Symbol	Bit name	Description	R/W
b7 to b0	CTSUCHTRC1[7:0]	CTSU Channel Transmit/Receive Control 1	0: Reception 1: Transmission. These bits specify the TS08 to TS15 pins.	R/W

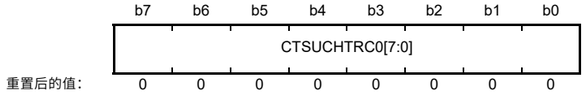
Only set the CTSUCHTRC1 register when the CTSUCR0.CTSUSTRT bit is 0.

CTSUCHTRC1[7:0] bits (CTSU Channel Transmit/Receive Control 1)

In full scan mode, the CTSUCHTRC1[7:0] bits allocate reception or transmission to the associated TS pins. The setting is ignored in self-capacitance single scan and multiscan modes. CTSUCHTRC1[0] is associated with TS08 and CTSUCHTRC1[7] with TS15.

51.2.10 CTSU通道发送接收控制寄存器0(CTSUCHTRC0)

Address(es): CTSU.CTSUCHTRC0 4008 100Bh



Bit	Symbol	位名称	Description	R/W
b7 to b0	CTSUCHTRC0[7:0]	CTSU Channel Transmit/Receive Control 0	0：接收1：发送。这些位指定TS00到TS07引脚。	R/W

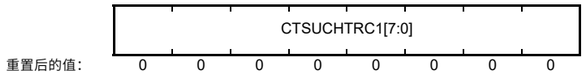
仅在CTSUCR0.CTSUSTRT位为0时设置CTSUCHTRC0寄存器。

CTSUCHTRC0[7:0]位（CTSU通道发送接收控制0）

在全扫描模式下，CTSUCHTRC0[7:0]位将接收或发送分配给相关的TS引脚。在自电容单次扫描和多次扫描模式下，该设置被忽略。CTSUCHTRC0[0]与TS00相关联，CTSUCHTRC0[7]与TS07相关联。

51.2.11 CTSU通道发送接收控制寄存器1(CTSUCHTRC1)

Address(es): CTSU.CTSUCHTRC1 4008 100Ch



Bit	Symbol	位名称	Description	R/W
b7 to b0	CTSUCHTRC1[7:0]	CTSU Channel Transmit/Receive Control 1	0：接收1：发送。这些位指定TS08到TS15引脚。	R/W

仅在CTSUCR0.CTSUSTRT位为0时设置CTSUCHTRC1寄存器。

CTSUCHTRC1[7:0]位（CTSU通道发送接收控制1）

在全扫描模式下，CTSUCHTRC1[7:0]位将接收或发送分配给相关的TS引脚。在自电容单扫描和多扫描模式下，该设置被忽略。CTSUCHTRC1[0]与TS08相关联，CTSUCHTRC1[7]与TS15相关联。

51.2.12 CTSU Channel Transmit/Receive Control Register 2 (CTSUCHTRC2)

Address(es): CTSU.CTSUCHTRC2 4008 100Dh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	CTSUCHTRC2 [1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1 to b0	CTSUCHTRC2 [1:0]	CTSU Channel Transmit/Receive Control 2	0: Reception 1: Transmission. These bits specify the TS16 to TS17 pins.	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Only set the CTSUCHTRC2 register when the CTSUCR0.CTSUSTRT bit is 0.

CTSUCHTRC2 [1:0] bits (CTSU Channel Transmit/Receive Control 2)

In full scan mode, the CTSUCHTRC2 [1:0] bits allocate reception or transmission to the associated TS pins. The setting is ignored in self-capacitance single scan and multiscan modes. CTSUCHTRC2[0] is associated with TS16 and CTSUCHTRC2 [1] with TS17.

51.2.13 CTSU High-Pass Noise Reduction Control Register (CTSUDCLKC)

Address(es): CTSU.CTSUDCLKC 4008 1010h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	CTSUSSCNT[1:0]		—	—	CTSUSSMOD[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	CTSUSSMOD[1:0]	CTSU Diffusion Clock Mode Select	Set these bits to 00b.	R/W
b3, b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b5, b4	CTSUSSCNT[1:0]	CTSU Diffusion Clock Mode Control	Set these bits to 11b.	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Only set the CTSUDCLKC register when the CTSUCR0.CTSUSTRT bit is 0.

CTSUSSMOD[1:0] bits (CTSU Diffusion Clock Mode Select)

The CTSUSSMOD[1:0] bits set the mode of the spectrum diffusion clock for high-pass noise reduction. When using the high-pass function, always fix these bits to 00b. If these bits are not set, the CTSU will be unable to effectively reduce high-pass noise.

CTSUSSCNT[1:0] bits (CTSU Diffusion Clock Mode Control)

The CTSUSSCNT[1:0] bits adjust the amount of spectrum diffusion applied to reduce high-pass noise. When using the high-pass noise reduction function, always fix these bits to 11b. If these bits are not set, touch measurement might be performed incorrectly.

51.2.12 CTSU通道发送接收控制寄存器2(CTSUCHTRC2)

Address(es): CTSU.CTSUCHTRC2 4008 100Dh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	CTSUCHTRC2 [1:0]	
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b1 to b0	CTSUCHTRC2 [1:0]	CTSU Channel Transmit/Receive Control 2	0：接收1：发送。这些位指定TS16到TS17引脚。	R/W
b7 to b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W

仅当CTSUCR0.CTSUSTRT位为0时设置CTSUCHTRC2寄存器。

CTSUCHTRC2[1:0]位（CTSU通道发送接收控制2）

在全扫描模式下，CTSUHTRC2[1:0]位将接收或发送分配给相关的TS引脚。在自电容单扫描和多扫描模式下，该设置被忽略。CTSUCHTRC2[0]与TS16相关联，CTSUCHTRC2[1]与TS17相关联。

51.2.13 CTSU高通降噪控制寄存器(CTSUDCLKC)

Address(es): CTSU.CTSUDCLKC 4008 1010h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	CTSUSSCNT[1:0]		—	—	CTSUSSMOD[1:0]	
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b1, b0	CTSUSSMOD[1:0]	CTSU扩散时钟模式选择	将这些位设置为00b。	R/W
b3, b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b5, b4	CTSUSSCNT[1:0]	CTSU扩散时钟模式控制	将这些位设置为11b。	R/W
b7, b6	—	Reserved	这些位被读取为0。写入值应为0。	R/W

仅当CTSUCR0.CTSUSTRT位为0时设置CTSUDCLKC寄存器。

CTSUSSMOD[1:0]位（CTSU扩散时钟模式选择）

CTSUSSMOD[1:0]位设置频谱扩散时钟的模式以降低高通噪声。使用高通功能时，请始终将这些位固定为00b。如果未设置这些位，CTSU将无法有效降低高通噪声。

CTSUSSCNT[1:0]位（CTSU扩散时钟模式控制）

CTSUSSCNT[1:0]位调整应用的频谱扩散量以减少高通噪声。使用高通降噪功能时，请始终将这些位固定为11b。如果未设置这些位，则可能会错误地执行触摸测量。

51.2.14 CTSU Status Register (CTSUST)

Address(es): CTSU.CTSUST 4008 1011h

	b7	b6	b5	b4	b3	b2	b1	b0
	CTSUPS	CTSUROVF	CTSUSOVF	CTSUDTSR	—	CTSUSTC[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	CTSUSTC[2:0]	CTSU Measurement Status Counter	These counters indicate the current measurement status. b2 b0 0 0 0: Status 0 0 0 1: Status 1 0 1 0: Status 2 0 1 1: Status 3 1 0 0: Status 4 1 0 1: Status 5.	R
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	CTSUDTSR	CTSU Data Transfer Status Flag	This flag indicates whether the measurement result stored in the sensor counter and the reference counter was read. 0: Read 1: Not read.	R
b5	CTSUSOVF	CTSU Sensor Counter Overflow Flag	This flag indicates an overflow on the sensor counter. 0: No overflow occurred 1: Overflow occurred.	R/W
b6	CTSUROVF	CTSU Reference Counter Overflow Flag	This flag indicates an overflow on the reference counter. 0: No overflow occurred 1: Overflow occurred.	R/W
b7	CTSUPS	CTSU Mutual Capacitance Status Flag	This flag indicates the measurement status in mutual capacitance full scan mode. 0: First measurement 1: Second measurement.	R

When using the CTSUCR0.CTSUINIT bit to clear an overflow flag, make sure that the CTSUCR0.CTSUSTRT bit is 0.

CTSUSTC[2:0] flags (CTSU Measurement Status Counter)

The CTSUSTC[2:0] flags are a counter indicating the current measurement status. For details on each status, see section 51.3.2.2, Status counter.

CTSUDTSR flag (CTSU Data Transfer Status Flag)

The CTSUDTSR flag indicates whether the measurement result stored in the sensor counter and the reference counter was read. The flag sets to 1 when measurement completes and 0 when the reference counter is read by software or the DTC. The flag can also be cleared using the CTSUCR0.CTSUINIT bit.

CTSUSOVF flag (CTSU Sensor Counter Overflow Flag)

The CTSUSOVF flag sets to 1 when the sensor counter, CTSUSC, overflows. On overflow, the counter value reads as FFFFh. Measurement processing continues for the specified period.

No interrupt occurs on an overflow. To determine the channel on which the overflow occurred, read the measurement result of each channel after measurement completes, signaled by a measurement end interrupt.

This flag is cleared when 0 is written after 1 is read by software. It can also be cleared using the CTSUCR0.CTSUINIT bit.

51.2.14 CTSU状态寄存器(CTSUST)

Address(es): CTSU.CTSUST 4008 1011h

	b7	b6	b5	b4	b3	b2	b1	b0
	CTSUPS	CTSUROVF	CTSUSOVF	CTSUDTSR	—	CTSUSTC[2:0]		
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b2 to b0	CTSUSTC[2:0]	CTSU测量状态计数器	这些计数器指示当前的测量状态。b2 b0 0 0 0: Status 0 0 0 1: Status 1 0 1 0: Status 2 0 1 1: Status 3 1 0 0: Status 4 1 0 1: Status 5.	R
b3	—	Reserved	该位读取为0。写入值应为0。	R/W
b4	CTSUDTSR	CTSU数据传输状态标志	该标志指示存储在传感器计数器和参考计数器中的测量结果是否被读取。0：读取1：未读取。	R
b5	CTSUSOVF	CTSU传感器计数器溢出标志	该标志表示传感器计数器溢出。0：未发生溢出1：发生溢出。	R/W
b6	CTSUROVF	CTSU参考计数器溢出Flag	该标志表示参考计数器溢出。0：未发生溢出1：发生溢出。	R/W
b7	CTSUPS	CTSU互电容状态Flag	该标志指示互电容全扫描模式下的测量状态。0：第一次测量1：第二次测量。	R

使用CTSUCR0.CTSUINIT位清除溢出标志时，请确保CTSUCR0.CTSUSTRT位为0。

CTSUSTC[2:0]标志（CTSU测量状态计数器）

CTSUSTC[2:0]标志是指示当前测量状态的计数器。有关每个状态的详细信息，请参阅第51.3.2.2节，状态计数器。

CTSUDTSR标志（CTSU数据传输状态标志）

CTSUDTSR标志指示存储在传感器计数器和参考计数器中的测量结果是否被读取。当测量完成时，该标志设置为1，当软件或DTC读取参考计数器时，该标志设置为0。也可以使用CTSUCR0.CTSUINIT位清除该标志。

CTSUSOVF标志（CTSU传感器计数器溢出标志）

当传感器计数器CTSUSC溢出时，CTSUSOVF标志设置为1。溢出时，计数器值读取为FFFFh。测量处理持续指定的时间。

溢出时不发生中断。要确定发生溢出的通道，请在测量完成后读取每个通道的测量结果，由测量结束中断发出信号。

当软件读取1后写入0时清除该标志。它也可以使用CTSUCR0.CTSUINIT位清零。

CTSUROVF flag (CTSU Reference Counter Overflow Flag)

The CTSUROVF flag sets to 1 when the reference counter, CTSURC, overflows. On overflow, the counter value reads as FFFFh. Measurement processing continues for the specified period.

No interrupt occurs on an overflow. To determine the channel on which the overflow occurred, read the measurement result of each channel after measurement completes, signaled by a measurement end interrupt.

This flag is cleared when 0 is written after 1 is read by software. It can also be cleared using the CTSUCR0.CTSUINIT bit.

CTSUPS flag (CTSU Mutual Capacitance Status Flag)

In mutual capacitance full scan mode, when CTSUCR1.CTSUMD[1:0] = 11b, the CTSUPS flag indicates whether the measurement is the first or second of two measurements for each channel. When measurement is stopped or in other measurement modes, this flag is always 0.

51.2.15 CTSU High-Pass Noise Reduction Spectrum Diffusion Control Register (CTSUSSC)

Address(es): CTSU.CTSUSSC 4008 1012h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	CTSUSSDIV[3:0]				—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b11 to b8	CTSUSSDIV[3:0]	CTSU Spectrum Diffusion Frequency Division Setting	These bits specify the spectrum diffusion frequency division setting based on the base clock frequency division setting.	R/W
b15 to b12	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

CTSUSSDIV[3:0] bits (CTSU Spectrum Diffusion Frequency Division Setting)

The CTSUSSDIV[3:0] bits specify the spectrum diffusion frequency derived from the base clock frequency division setting. To calculate the correct setting for CTSUSSDIV[3:0], see the relationship between base clock frequencies and the settings in Table 51.6.

Table 51.6 Relationship between base clock frequencies and CTSUSSDIV[3:0] bit settings (1 of 2)

Base clock frequency fb (MHz)	CTSUSSDIV[3:0] bit setting
4.00 ≤ fb	0000b
2.00 ≤ fb < 4.00	0001b
1.33 ≤ fb < 2.00	0010b
1.00 ≤ fb < 1.33	0011b
0.80 ≤ fb < 1.00	0100b
0.67 ≤ fb < 0.80	0101b
0.57 ≤ fb < 0.67	0110b
0.50 ≤ fb < 0.57	0111b
0.44 ≤ fb < 0.50	1000b
0.40 ≤ fb < 0.44	1001b
0.36 ≤ fb < 0.40	1010b
0.33 ≤ fb < 0.36	1011b
0.31 ≤ fb < 0.33	1100b

CTSUROVF标志（CTSU参考计数器溢出标志）

当参考计数器CTSURC溢出时，CTSUROVF标志设置为1。溢出时，计数器值读取为FFFFh。测量处理持续指定的时间。

溢出时不发生中断。要确定发生溢出的通道，请在测量完成后读取每个通道的测量结果，由测量结束中断发出信号。

当软件读取1后写入0时清除该标志。它也可以使用CTSUCR0.CTSUINIT位清零。

CTSUPS标志（CTSU互电容状态标志）

在互电容全扫描模式下，当CTSUCR1.CTSUMD[1:0]=11b时，CTSUPS标志指示测量是每个通道的两次测量中的第一个还是第二个。当测量停止或处于其他测量模式时，该标志始终为0。

51.2.15 CTSU高通降噪频谱扩散控制寄存器(CTSUSSC)

Address(es): CTSU.CTSUSSC 4008 1012h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	CTSUSSDIV[3:0]				—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b7 to b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b11 to b8	CTSUSSDIV[3:0]	CTSU频谱扩散频分设置	这些位指定基于基本时钟分频设置的频谱扩散分频设置。	R/W
b15 to b12	—	Reserved	这些位被读取为0。写入值应为0。	R/W

CTSUSSDIV[3:0]位（CTSU频谱扩散频分设置）

CTSUSSDIV[3:0]位指定从基本时钟分频设置得出的频谱扩散频率。要计算CTSUSSDIV[3:0]的正确设置，请参见表51.6中基本时钟频率和设置之间的关系。

Table 51.6 基本时钟频率和CTSUSSDIV[3:0]位设置之间的关系(1of2)

基本时钟频率fb(MHz)	CTSUSSDIV[3:0]位设置
4.00 ≤ fb	0000b
2.00 ≤ fb < 4.00	0001b
1.33 ≤ fb < 2.00	0010b
1.00 ≤ fb < 1.33	0011b
0.80 ≤ fb < 1.00	0100b
0.67 ≤ fb < 0.80	0101b
0.57 ≤ fb < 0.67	0110b
0.50 ≤ fb < 0.57	0111b
0.44 ≤ fb < 0.50	1000b
0.40 ≤ fb < 0.44	1001b
0.36 ≤ fb < 0.40	1010b
0.33 ≤ fb < 0.36	1011b
0.31 ≤ fb < 0.33	1100b

Table 51.6 Relationship between base clock frequencies and CTSUSSDIV[3:0] bit settings (2 of 2)

Base clock frequency fb (MHz)	CTSUSSDIV[3:0] bit setting
0.29 ≤ fb < 0.31	1101b
0.27 ≤ fb < 0.29	1110b
fb < 0.27	1111b

51.2.16 CTSU Sensor Offset Register 0 (CTSUSO0)

Address(es): CTSU.CTSUSO0 4008 1014h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CTSUSNUM[5:0]						CTSUSO[9:0]									
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b9 to b0	CTSUSO[9:0]	CTSU Sensor Offset Adjustment	These bits adjust the electronic capacitance when the electrode is not being touched. b9 b0 0 0 0 0 0 0 0 0 0 0: Current offset is 0 0 0 0 0 0 0 0 0 0 1: Current offset is 1 0 0 0 0 0 0 0 0 1 0: Current offset is 2 : : 1 1 1 1 1 1 1 1 1 0: Current offset is 1022 1 1 1 1 1 1 1 1 1 1: Current offset is maximum.	R/W
b15 to b10	CTSUSNUM[5:0]	CTSU Measurement Count Setting	These bits set the number of measurements.	R/W

CTSUSO[9:0] bits (CTSU Sensor Offset Adjustment)

The CTSUSO[9:0] bits offset the sensor ICO input current generated from electrostatic capacitance during touch measurement when the electrode is not being touched. This prevents the CTSU sensor counter from overflowing. Set the TS pin that is to be measured next after a CTSU_CTSUWR interrupt occurs.

CTSUSNUM[5:0] bits (CTSU Measurement Count Setting)

The CTSUSNUM[5:0] bits specify how many times the measurement pulse count specified in the CTSUSDPRS.CTSUPRRATIO[3:0] and CTSUSDPRS.CTSUPRMODE[1:0] bits is repeated during the measurement time. The measurement pulse count is repeated (CTSUSNUM[5:0] bits + 1) times. Set the TS pin that is to be measured next after a CTSU_CTSUWR interrupt is generated.

Table 51.6 基本时钟频率和CTSUSSDIV[3:0]位设置之间的关系(2of2)

基本时钟频率fb(MHz)	CTSUSSDIV[3:0]位设置
0.29 ≤ fb < 0.31	1101b
0.27 ≤ fb < 0.29	1110b
fb < 0.27	1111b

51.2.16 CTSU传感器偏移寄存器0(CTSUSO0)

Address(es): CTSU.CTSUSO0 4008 1014h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CTSUSNUM[5:0]						CTSUSO[9:0]									
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b9 to b0	CTSUSO[9:0]	CTSU传感器偏移调整	这些位在电极未被触摸 时调整电子电容。b9 b000000000000：当前偏移量为000000000001 ：当前偏移量为10000000010：当前偏移量为 2::1111111110：当前偏移为1022111111111 1：当前偏移最大。	R/W
b15 to b10	CTSUSNUM[5:0]	CTSU测量计数	这些位设置测量次数。	R/W

CTSUSO[9:0]位（CTSU传感器偏移调整）

CTSUSO[9:0]位在电极未被触摸 时在触摸测量期间抵消由静电电容产生的传感器ICO输入电流。这可以防止CTSU传感器计数器溢出。在发生CTSU_CTSUWR中断后设置接下来要测量的TS引脚。

CTSUSNUM[5:0]位（CTSU测量计数设置）

CTSUSNUM[5:0]位指定测量脉冲计数的次数
CTSUSDPRS.CTSUPRRATIO[3:0]和CTSUSDPRS.CTSUPRMODE[1:0]位在测量期间重复。测量脉冲计数重复(CTSUSNUM[5:0]位+1)次。在产生CTSU_CTSUWR中断后设置接下来要测量的TS引脚。

51.2.17 CTSU Sensor Offset Register 1 (CTSUSO1)

Address(es): CTSU.CTSUSO1 4008 1016h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	CTSUICOG[1:0]		CTSUSDPA[4:0]					CTSURICOA[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	CTSURICOA[7:0]	CTSU Reference ICO Current Adjustment	These bits adjust the input current of the reference ICO. b7 b0 0 0 0 0 0 0 0 0: Current offset is 0 0 0 0 0 0 0 0 1: Current offset is 1 0 0 0 0 0 0 1 0: Current offset is 2 : : 1 1 1 1 1 1 1 0: Current offset is 254 1 1 1 1 1 1 1 1: Current offset is maximum.	R/W
b12 to b8	CTSUSDPA[4:0]	CTSU Base Clock Setting	These bits are used to generate the base clock. b12 b8 0 0 0 0 0: Operating clock divided by 2*1 0 0 0 0 1: Operating clock divided by 4 0 0 0 1 0: Operating clock divided by 6 0 0 0 1 1: Operating clock divided by 8 0 0 1 0 0: Operating clock divided by 10 0 0 1 0 1: Operating clock divided by 12 0 0 1 1 0: Operating clock divided by 14 0 0 1 1 1: Operating clock divided by 16 0 1 0 0 0: Operating clock divided by 18 0 1 0 0 1: Operating clock divided by 20 0 1 0 1 0: Operating clock divided by 22 0 1 0 1 1: Operating clock divided by 24 0 1 1 0 0: Operating clock divided by 26 0 1 1 0 1: Operating clock divided by 28 0 1 1 1 0: Operating clock divided by 30 0 1 1 1 1: Operating clock divided by 32 1 0 0 0 0: Operating clock divided by 34 1 0 0 0 1: Operating clock divided by 36 1 0 0 1 0: Operating clock divided by 38 1 0 0 1 1: Operating clock divided by 40 1 0 1 0 0: Operating clock divided by 42 1 0 1 0 1: Operating clock divided by 44 1 0 1 1 0: Operating clock divided by 46 1 0 1 1 1: Operating clock divided by 48 1 1 0 0 0: Operating clock divided by 50 1 1 0 0 1: Operating clock divided by 52 1 1 0 1 0: Operating clock divided by 54 1 1 0 1 1: Operating clock divided by 56 1 1 1 0 0: Operating clock divided by 58 1 1 1 0 1: Operating clock divided by 60 1 1 1 1 0: Operating clock divided by 62 1 1 1 1 1: Operating clock divided by 64.	R/W
b14, b13	CTSUICOG[1:0]	CTSU ICO Gain Adjustment	These bits adjust the output frequency gain of the sensor ICO and the reference ICO. b14 b13 0 0: 100% gain 0 1: 66% gain 1 0: 50% gain 1 1: 40% gain.	R/W
b15	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Note 1. Do not set the CTSUSDPA[4:0] bits set to 00000b while the high-pass noise reduction function is turned off (CTSUSDPRS.CTSUSOFF bit = 1) in mutual capacitance full scan mode (CTSUCR1.CTSUMD[1:0] bits = 11b).

51.2.17 CTSU传感器偏移寄存器1(CTSUSO1)

Address(es): CTSU.CTSUSO1 4008 1016h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	CTSUICOG[1:0]		CTSUSDPA[4:0]					CTSURICOA[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b7 to b0	CTSURICOA[7:0]	CTSU参考ICO电流 Adjustment	这些位调整参考ICO的输入电流。b7 b000000000：当前偏移为000000001：当前偏移为100000010：当前偏移为2::1111 1110：当前偏移量为25411111111：当前偏移量最大。	R/W
b12 to b8	CTSUSDPA[4:0]	CTSU基本时钟设置	这些位用于生成基本时钟。b12 b800000：运行时钟除以2*100001：运行时钟除以400010：运行时钟除以600011：运行时钟除以800100：工作时钟除以1000101：工作时钟除以1200110：工作时钟除以1400111：工作时钟除以1601000：工作时钟分频by1801001：运行时钟除以2001010：运行时钟除以2201011：运行时钟除以2401100：运行时钟除以2601101：运行时钟除以2801110：运行时钟除以3001111：运行时钟除以3210000：运行时钟除以3410001：运行时钟除以3610010：运行时钟除以3810011：运行时钟除以4010100：运行时钟除以4210101：运行时钟除以4410110:工作时钟除以4610111：运行时钟除以4811000：运行时钟除以5011001：运行时钟除以5211010：运行时钟除以5411011：运行时钟除以5611100：运行时钟除以5811101：运行时钟除以6011110：运行时钟除以6211111：运行时钟除以64。	R/W
b14, b13	CTSUICOG[1:0]	CTSUICO增益调整	这些位调整传感器ICO和参考ICO的输出频率增益。b14b13 0 0: 100% gain 0 1: 66% gain 1 0: 50% gain 1 1: 40% gain.	R/W
b15	—	Reserved	该位读取为0。写入值应为0。	R/W

Note 1. 在互电容全扫描模式（CTSUCR1.CTSUMD[1:0]位=11b）。

After a CTSU_CTSUWR interrupt occurs, write first to the CTSUSSC register, next to the CTSUSO0 register, and then to the CTSUSO1 register. The write to the CTSUSO1 register causes a transition to Status 3. (See Table 51.7 and Table 51.8.) Set all of the bits in a single operation when writing to the CTSUSO1 register.

CTSURICOA[7:0] bits (CTSU Reference ICO Current Adjustment)

The CTSURICOA[7:0] bits adjust the oscillation frequency using the input current of the reference ICO.

CTSUSDPA[4:0] bits (CTSU Base Clock Setting)

The CTSUSDPA[4:0] bits select the base clock used as the source for the sensor drive pulse by dividing the operating clock. For details on the setting procedure, see section 51.3.2.1, Initial settings flow.

CTSUICOG[1:0] bits (CTSU ICO Gain Adjustment)

The CTSUICOG[1:0] bits adjust the output frequency gain of the sensor ICO and the reference ICO. Normally, set these bits to 00b for the maximum gain. If changes in the capacitance between when the electrode is touched and when it is not touched greatly exceed the dynamic range of the sensor ICO, adjust the gain appropriately with this setting.

51.2.18 CTSU Sensor Counter (CTSUSC)

Address(es): CTSU.CTSUSC 4008 1018h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CTSUSC[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b15 to b0	CTSUSC[15:0]	CTSU Sensor Counter	These bits indicate the measurement result of the sensor ICO. They read FFFFh when an overflow occurs.	R

After a CTSU_CTSURD interrupt occurs, read first from the CTSUSC counter and then from the CTSURC counter.

CTSUSC[15:0] bits (CTSU Sensor Counter)

The CTSUSC[15:0] bits are configured as an increment counter for the sensor ICO clock. Read these bits after a CTSU_CTSURD interrupt occurs. After the CTSURC counter is read, these bits are cleared immediately before the CTSU measurement status counter value changes to Status 4 (the CTSUST.CTSUSTC[2:0] flags changes to 100b) in the next measurement. They can also be cleared using the CTSUCR0.CTSUINIT bit.

51.2.19 CTSU Reference Counter (CTSURC)

Address(es): CTSU.CTSURC 4008 101Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CTSURC[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b15 to b0	CTSURC[15:0]	CTSU Reference Counter	These bits indicate the measurement result of the reference ICO. They read FFFFh when an overflow occurs.	R

After a CTSU_CTSURD interrupt occurs, read first from the CTSUSC counter and then from the CTSURC counter. Status 3 continues until the CTSURC counter is read, even if the stabilization time specified for Status 3 elapses.

发生CTSU_CTSUWR中断后，先写入CTSUSSC寄存器，然后写入CTSUSO0寄存器，然后写入CTSUSO1寄存器。写入CTSUSO1寄存器会导致转换到状态3。（参见表51.7和表51.8。）在写入CTSUSO1寄存器时，在一次操作中设置所有位。

CTSURICOA[7:0]位（CTSU参考ICO电流调整）

CTSURICOA[7:0]位使用参考ICO的输入电流调整振荡频率。

CTSUSDPA[4:0]位（CTSU基本时钟设置）

CTSUSDPA[4:0]位通过对工作时钟进行分频来选择用作传感器驱动脉冲源的基本时钟。有关设置过程的详细信息，请参阅第51.3.2.1节，初始设置流程。

CTSUICOG[1:0]位（CTSUICO增益调整）

CTSUICOG[1:0]位调整传感器ICO和参考ICO的输出频率增益。通常，将这些位设置为00b以获得最大增益。如果触摸电极和未触摸电极之间的电容变化大大超过传感器ICO的动态范围，请使用此设置适当调整增益。

51.2.18 CTSU传感器计数器(CTSUSC)

Address(es): CTSU.CTSUSC 4008 1018h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CTSUSC[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b15 to b0	CTSUSC[15:0]	CTSU传感器计数器	这些位表示传感器ICO的测量结果。它们在发生溢出时读取FFFFh。	R

发生CTSU_CTSURD中断后，先从CTSUSC计数器读取，然后再从CTSURC计数器读取。

CTSUSC[15:0]位（CTSU传感器计数器）

CTSUSC[15:0]位配置为传感器ICO时钟的增量计数器。后读取这些位
CTSU_CTSURD中断发生。读取CTSURC计数器后，这些位在
CTSU测量状态计数器值在下一次测量中更改为状态4（CTSUST.CTSUSTC[2:0]标志更改为100b）。它们也可以使用CTSUCR0.CTSUINIT位清零。

51.2.19 CTSU参考计数器(CTSURC)

Address(es): CTSU.CTSURC 4008 101Ah

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CTSURC[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b15 to b0	CTSURC[15:0]	CTSU参考计数器	这些位表示参考ICO的测量结果。它们在发生溢出时读取FFFFh。	R

发生CTSU_CTSURD中断后，先从CTSUSC计数器读取，然后再从CTSURC计数器读取。
状态3一直持续到读取CTSURC计数器为止，即使为状态3指定的稳定时间已过。

CTSURC[15:0] bits (CTSU Reference Counter)

The CTSURC[15:0] bits are configured as an increment counter for the reference ICO clock. The reference ICO optimizes touch measurement performed by the sensor ICO. There is some deviation depending on the internal sensor ICO and the reference ICO in the CTSU, but both ICOs have almost the same characteristics, including the dynamic range and the current-to-frequency characteristics. The range of current amount that can be set in the reference ICO current adjustment bits is about the same as the dynamic range of both ICOs, and the current amount input to the sensor ICO must be within this dynamic range. To ensure this, use the reference ICO to check the differences between the ICOs and measure the current-to-oscillation frequency characteristics. Because the reference ICO oscillation frequency can be obtained from the reference ICO counter, the ICO oscillation frequency (counter value/measurement time) for the input current amount can be measured by setting the value in the reference ICO current adjustment bits and measuring the reference ICO counter. The reference ICO counter value measured using the maximum value in the reference ICO current adjustment bits is the maximum value of the ICO dynamic range. The current to the sensor ICO must be offset in the offset adjustment bits so that the sensor ICO counter value does not exceed this value.

Read the CTSURC[15:0] bits after a CTSU_CTSURD interrupt occurs. After these bits are read, they are cleared immediately before the CTSU measurement status counter value changes to Status 4 (the CTSUST.CTSUSTC[2:0] flags changes to 100b) in the next measurement. They can also be cleared using the CTSUCR0.CTSUINIT bit.

51.2.20 CTSU Error Status Register (CTSUERRS)

Address(es): CTSU.CTSUERRS 4008 101Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CTSUICOMP	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	x	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b14 to b0	—	Reserved	These bits are read as 0.	R
b15	CTSUICOMP	TSCAP Voltage Error Monitor	This bit monitors the error status of the TSCAP voltage. 0: Normal TSCAP voltage 1: Abnormal TSCAP voltage.*1	R

Note 1. When CTSUCR1.CTSUPON bit is 0, this bit is set to 1.

CTSUICOMP bit (TSCAP Voltage Error Monitor)

If the offset current amount set in the CTSUSO1 register exceeds the sensor ICO input current during touch measurement, the TSCAP voltage becomes abnormal and touch measurement cannot be performed correctly. The CTSUICOMP bit monitors the TSCAP voltage and it sets to 1 if the voltage becomes abnormal.

If the TSCAP voltage becomes abnormal, the sensor ICO counter value becomes undefined, but touch measurement completes normally, so it is difficult to detect an abnormality by reading the sensor ICO counter value. If the CTSU reference ICO current adjustment bits (CTSURICOA[7:0]) in the CTSUSO1 register are set to any value other than 0, always check this bit when touch measurement completes.

This bit is cleared by writing 0 to the CTSUCR1.CTSUPON bit and turning off the power supply.

51.3 Operation

51.3.1 Principles of Measurement Operation

Figure 51.4 shows the measurement circuit.

CTSURC[15:0]位（CTSU参考计数器）

CTSURC[15:0]位配置为参考ICO时钟的增量计数器。参考ICO优化了传感器ICO执行的触摸测量。CTSU中的内部传感器ICO和参考ICO存在一些偏差，但两种ICO具有几乎相同的特性，包括动态范围和电流频率特性。参考ICO电流调整位可设置的电流量范围与两个ICO的动态范围大致相同，输入到传感器ICO的电流量必须在此动态范围内。为确保这一点，请使用参考ICO检查ICO之间的差异并测量电流-振荡频率特性。因为可以从参考ICO计数器获得参考ICO振荡频率，所以可以通过设置参考ICO电流调整位中的值并测量参考ICO计数器来测量输入电流量的ICO振荡频率（计数器值测量时间）.使用参考ICO电流调整位中的最大值测量的参考ICO计数器值是ICO动态范围的最大值。传感器ICO的电流必须在偏移调整位中进行偏移，以使传感器ICO计数器值不超过此值。

在CTSU_CTSURD中断发生后读取CTSURC[15:0]位。读取这些位后，在CTSU测量状态计数器值在下一次测量中立即变为状态4（CTSUST.CTSUSTC[2:0]标志变为100b）之前将它们清零。它们也可以使用CTSUCR0.CTSUINIT位清零。

51.2.20 CTSU错误状态寄存器(CTSUERRS)

Address(es): CTSU.CTSUERRS 4008 101Ch

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CTSUICOMP	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	x	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

x: Undefined

Bit	Symbol	位名称	Description	R/W
b14 to b0	—	Reserved	这些位读为0。	R
b15	CTSUICOMP	TSCAP电压错误监视器	该位监控TSCAP电压的错误状态。0：正常TSCAP电压1：异常TSCAP电压。*1	R

Note 1. 当CTSUCR1.CTSUPON位为0时，该位设置为1。

CTSUICOMP位（TSCAP电压错误监视器）

如果CTSUSO1寄存器中设置的偏移电流量在触摸测量期间超过传感器ICO输入电流，则TSCAP电压会异常，无法正确执行触摸测量。CTSUICOMP位监控TSCAP电压，如果电压异常，它设置为1。

如果TSCAP电压异常，则传感器ICO计数器值变得不确定，但触摸测量正常完成，因此很难通过读取传感器ICO计数器值来检测异常。如果CTSUSO1寄存器中的CTSU参考ICO电流调整位(CTSURICOA[7:0])设置为0以外的任何值，则在触摸测量完成时始终检查该位。

通过向CTSUCR1.CTSUPON位写入0并关闭电源来清除该位。

51.3 Operation

51.3.1 测量操作原理

图51.4显示了测量电路。

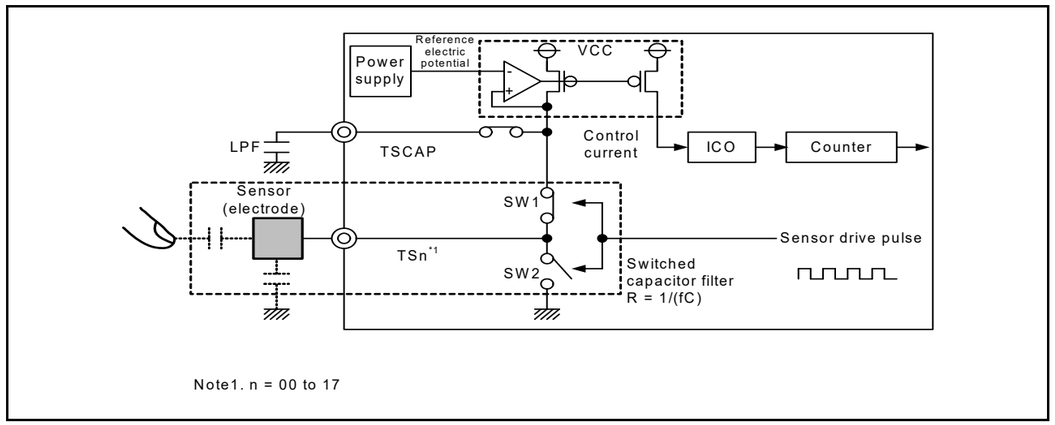


Figure 51.4 Measurement circuit

Figure 51.5 to Figure 51.7 explain the electrostatic capacitance measurement operation principles of the CTSU current frequency conversion method.

The electrostatic capacitance of the electrode is charged by turning SW1 on and SW2 off (Figure 51.5).

The charged capacitance is discharged by turning SW1 off and SW2 on (Figure 51.6).

Current flows to the switched capacitor filter by switching between charging and discharging. At this point, if a finger is in close proximity, the capacitance and the flowing current change. A clock is generated by supplying the control current, which is proportional to the amount of current flowing through the switched capacitor filter, from the circuit that generates the TSCAP power supply to the ICO. The counter measures the clock frequency that changes depending on whether a finger is in close proximity. The software uses the value read from the counter to determine contact with a finger (Figure 51.7).

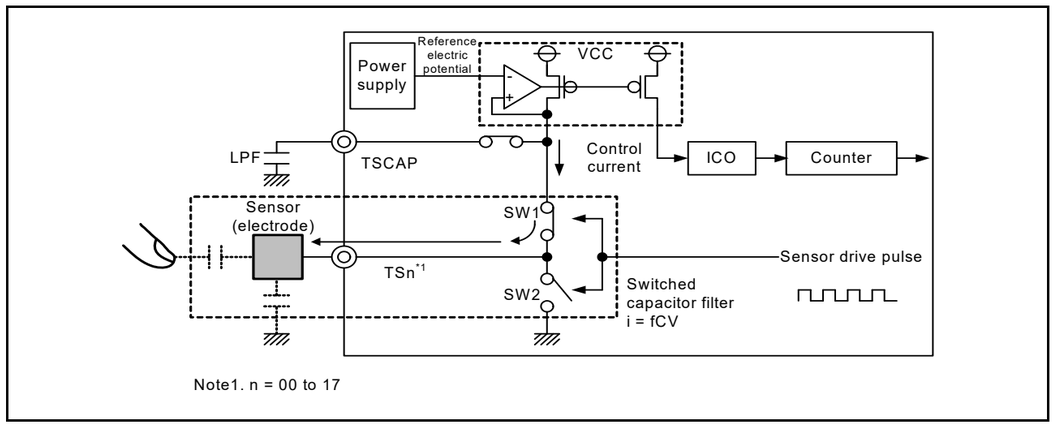


Figure 51.5 Charging operation

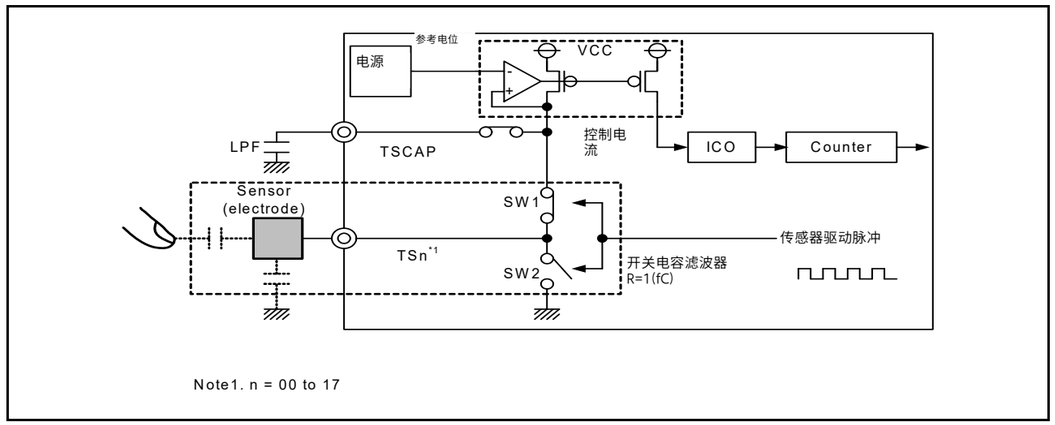


Figure 51.4 测量电路

图51.5至图51.7说明了CTSU电流变频方式的静电电容测量操作原理。

通过打开SW1和关闭SW2对电极的静电电容进行充电（图51.5）。

通过关闭SW1和打开SW2对充电的电容进行放电（图51.6）。

通过在充电和放电之间切换，电流流向开关电容滤波器。此时，如果手指靠近，则电容和流动电流会发生变化。通过从产生TSCAP电源的电路向ICO提供与流过开关电容滤波器的电流量成比例的控制电流来产生时钟。计数器测量时钟频率，该频率根据手指是否靠近而变化。软件使用从计数器读取的值来确定与手指的接触（图51.7）。

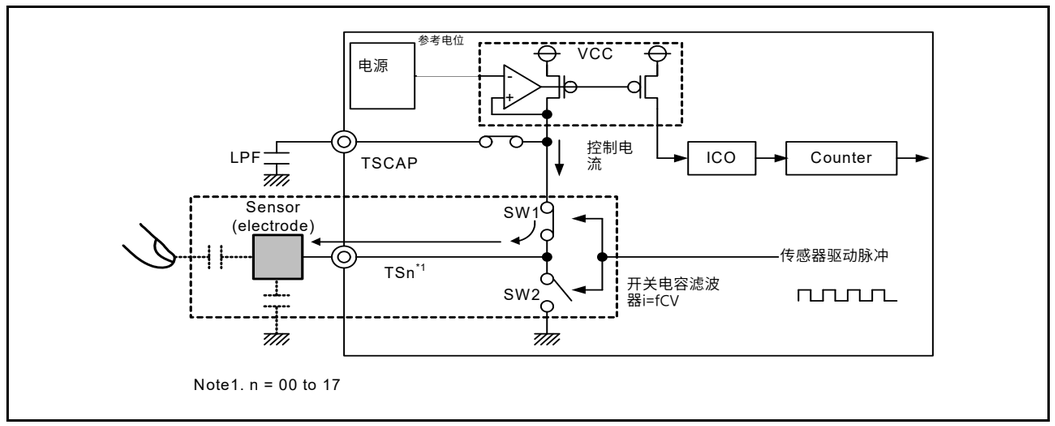


Figure 51.5 充电操作

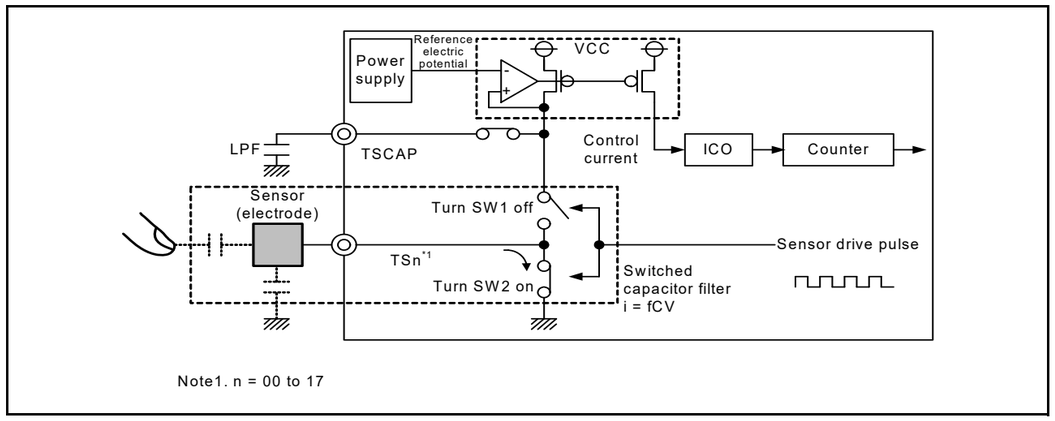


Figure 51.6 Discharging operation

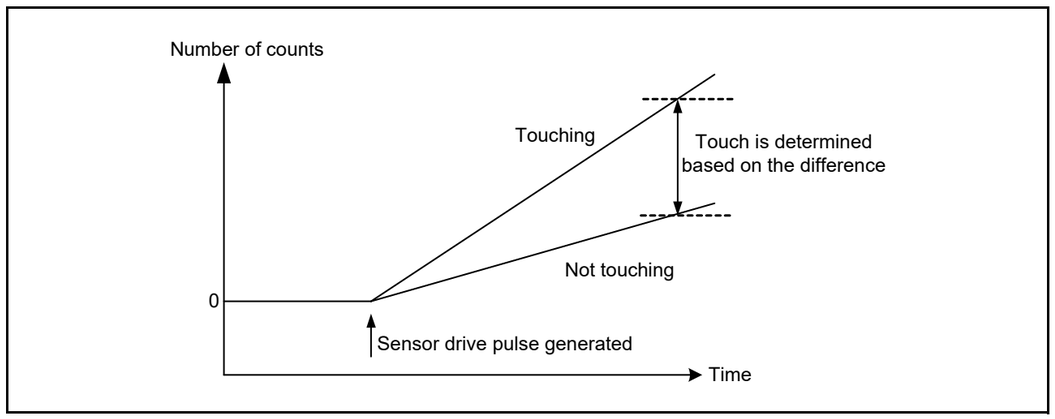


Figure 51.7 Change in measured value when finger is touching and not touching

51.3.2 Measurement Modes

The CTSU supports self-capacitance and mutual capacitance methods. Figure 51.8 illustrates these methods.

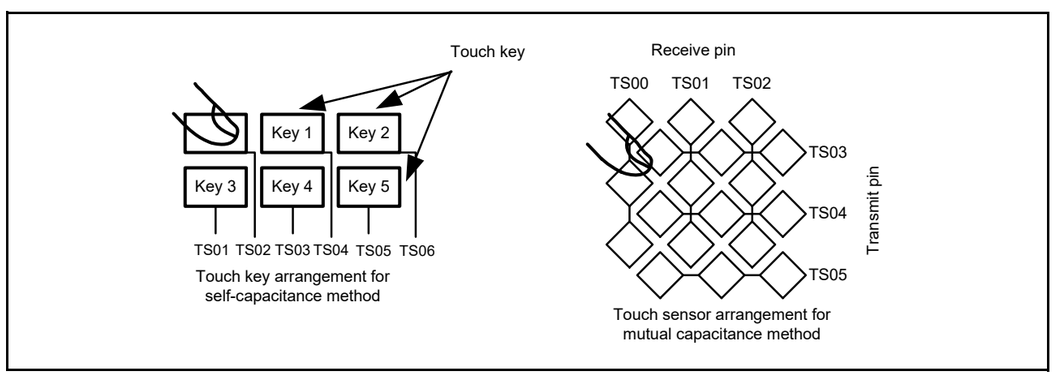


Figure 51.8 Overview of self-capacitance method and mutual capacitance method

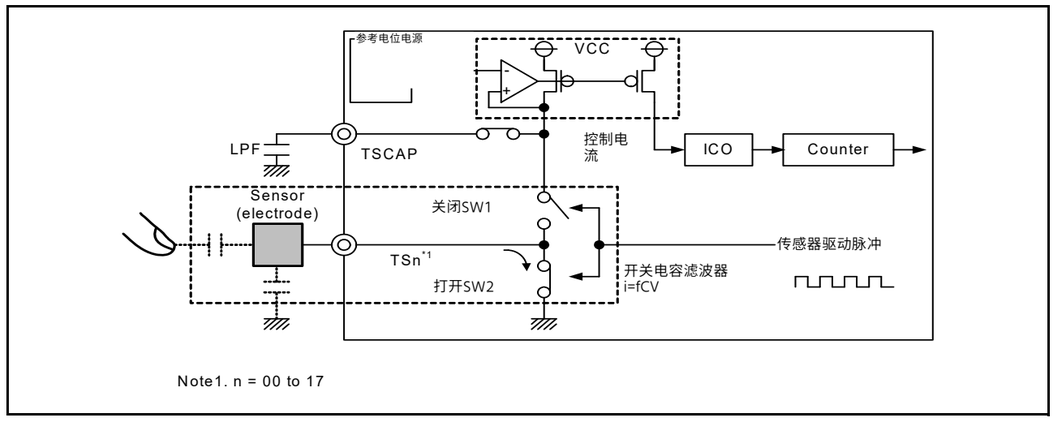


Figure 51.6 卸料作业

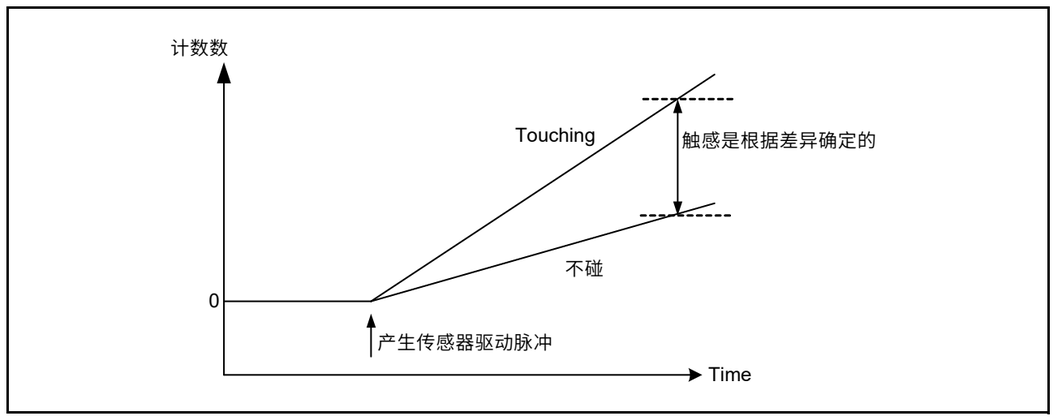


Figure 51.7 手指接触和不接触时测量值的变化

51.3.2 测量模式

CTSU支持自电容和互电容方法。图51.8说明了这些方法。

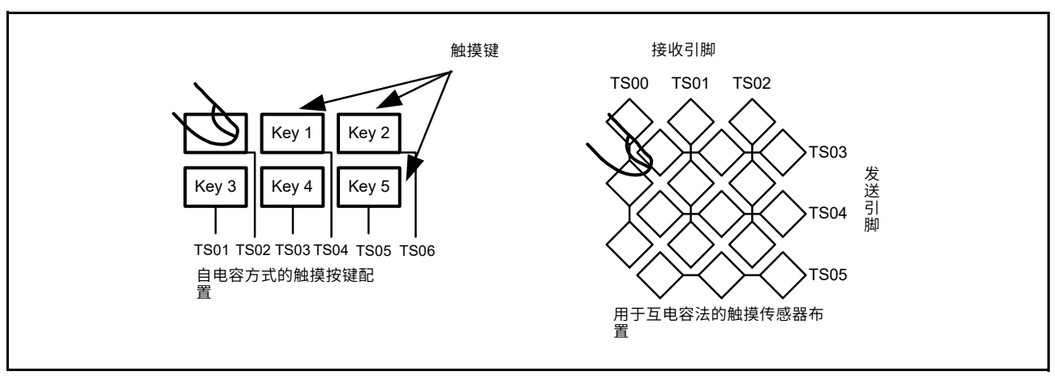


Figure 51.8 自电容法和互电容法概述

In the self-capacitance method, a single touch pin is allocated to a single touch key to measure individual electrostatic capacitance when a finger is in close proximity. In this method, capacitance can be measured in both single scan and multiscan modes. In the mutual capacitance method, the capacitance between two opposing electrodes (transmit and receive pins) is measured.

51.3.2.1 Initial settings flow

Figure 51.9 shows the flow for the CTSU initial settings.

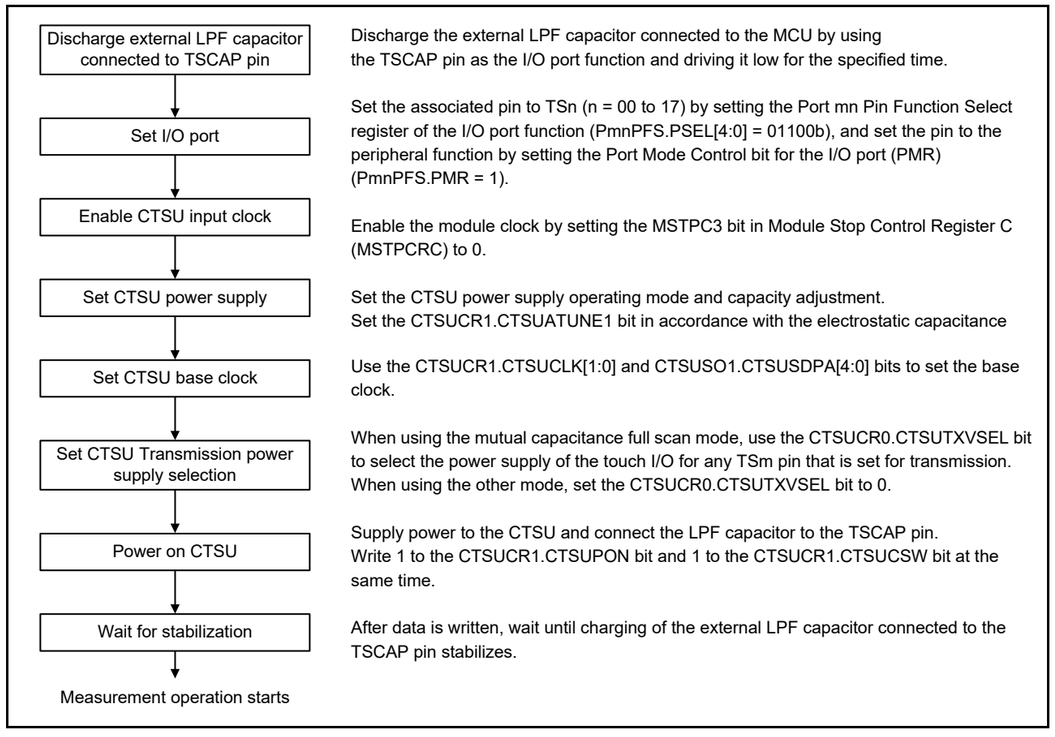


Figure 51.9 CTSU initial settings flow

Figure 51.10 shows the flow for stopping CTSU operation and invoking the standby state.

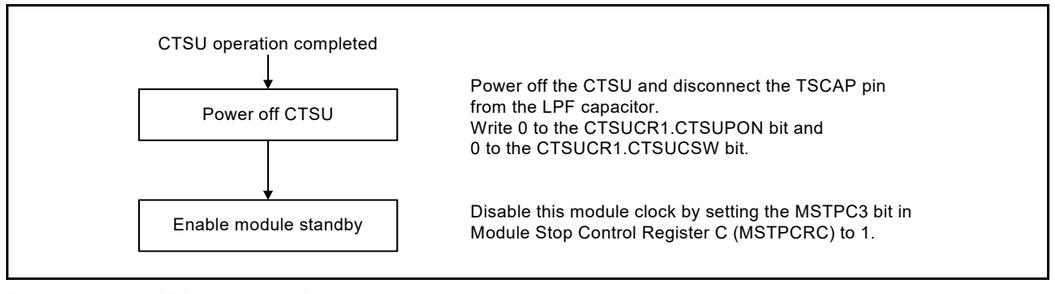


Figure 51.10 CTSU stopping flow

When restarting operation after it stops, follow the initial settings flow shown in Figure 51.9.

在自电容法中，将单个触摸引脚分配给单个触摸键，以在手指靠近时测量单个静电电容。在这种方法中，可以在单扫描和多扫描模式下测量电容。在互电容法中，测量两个相对电极（发送和接收引脚）之间的电容。

51.3.2.1 初始设置流程

图51.9显示了CTSU初始设置的流程。

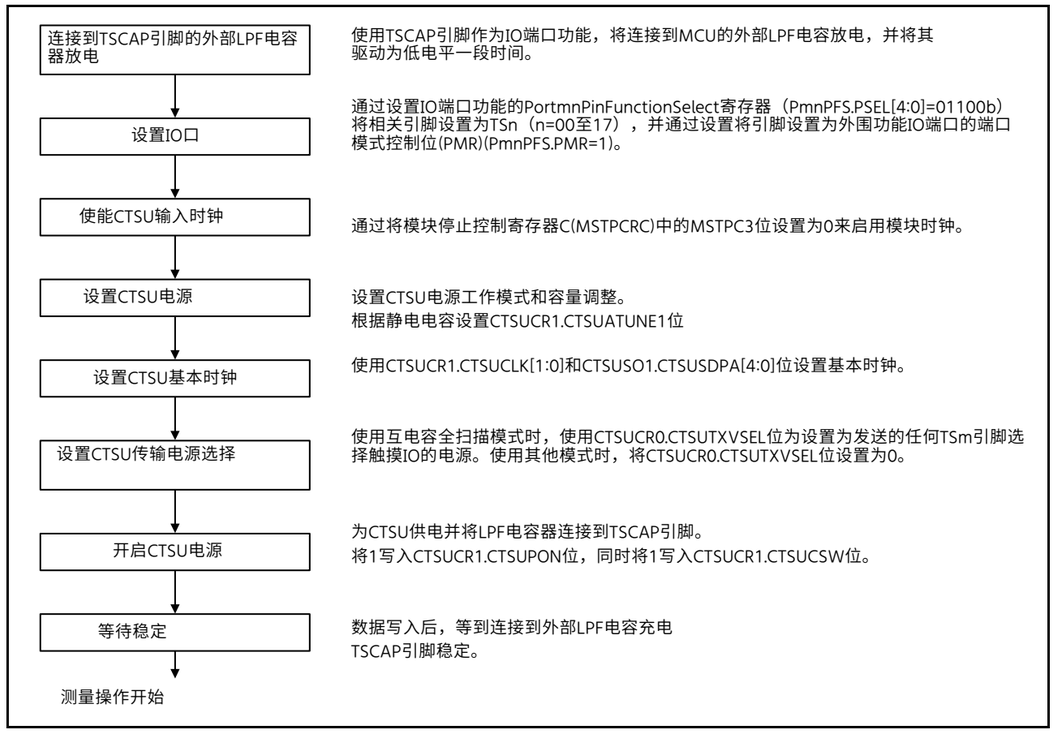


Figure 51.9 CTSU初始设置流程

图51.10显示了停止CTSU操作并调用待机状态的流程。

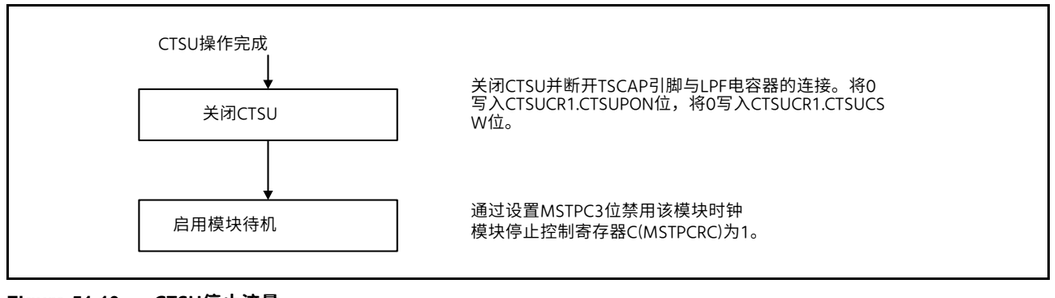


Figure 51.10 CTSU停止流量

停止后重新开始运行时，请按照图51.9所示的初始设置流程进行操作。

51.3.2.2 Status counter

The measurement status counter of the CTSU Status Register (CTSUST) indicates the current measurement status. The measurement status is shared by all three modes. Figure 51.11 shows the status operation transitions.

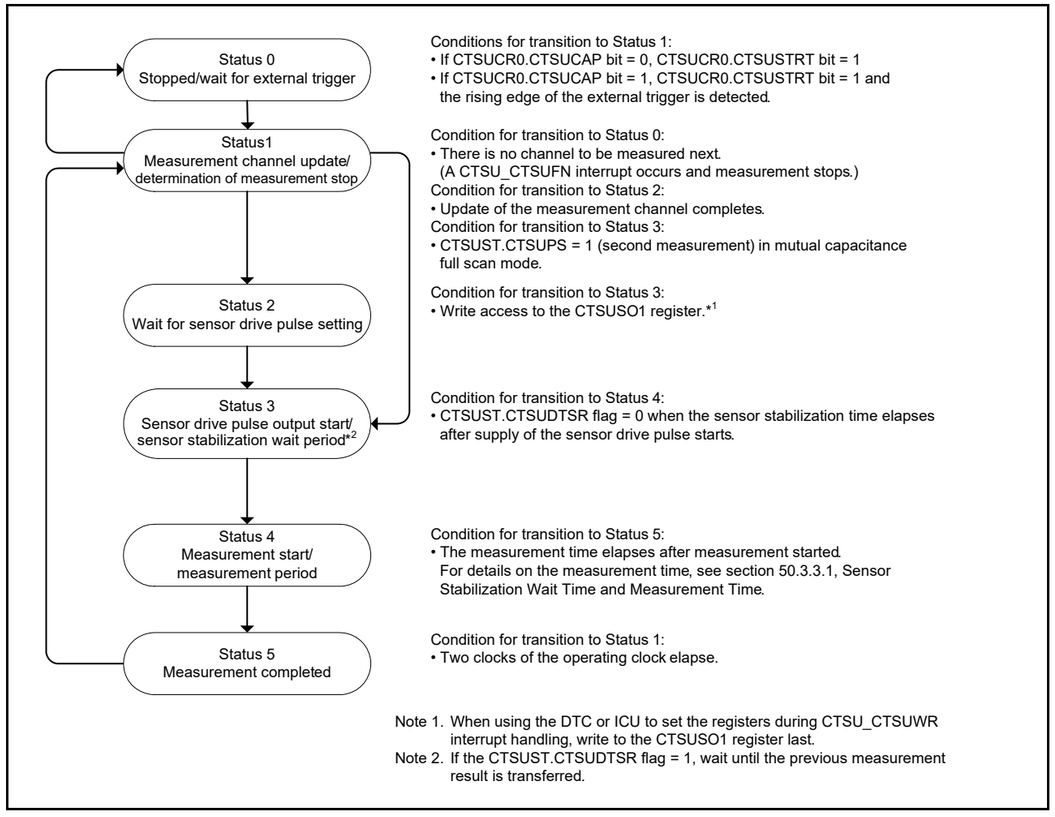


Figure 51.11 Status operation transitions

The status counter transitions to Status 0 when all of the specified measurement channels are measured.

The CTSUCR0.CTSUSTRT bit is cleared to 0 by hardware when a software trigger is used. When an external trigger is used, the value of 1 is retained, and the CTSU waits for the next trigger.

When operation is forced to stop during measurement or the trigger wait state, by a simultaneous 0 write to the CTSUCR0.CTSUSTRT bit and a 1 write to the CTSUCR0.CTSUINIT bit, the status transitions to Status 0 and measurement stops.

If the channel to be measured is not set in the CTSUCHAC0 to CTSUCHAC2 or CTSUCHTRC0 to CTSUCHTRC2 registers, a CTSU_CTSUFN interrupt occurs immediately after a transition to Status 1, and then the status transitions to Status 0.

In the following situations, there is no channel to be measured:

- No measurement target channel is specified in the CTSUCHAC0 to CTSUCHAC2 registers.
- In self-capacitance single scan mode, the channel specified in the CTSUMCH0 register is not a measurement target in the CTSUCHAC0 to CTSUCHAC2 registers.
- In full scan modes, there is no transmit channel or receive channel to be measured based on the combined settings of the CTSUCHAC0 to CTSUCHAC2 and CTSUCHTRC0 to CTSUCHTRC2 registers.

51.3.2.2 状态计数器

CTSU状态寄存器(CTSUST)的测量状态计数器指示当前测量状态。测量状态由所有三种模式共享。图51.11显示了状态操作转换。

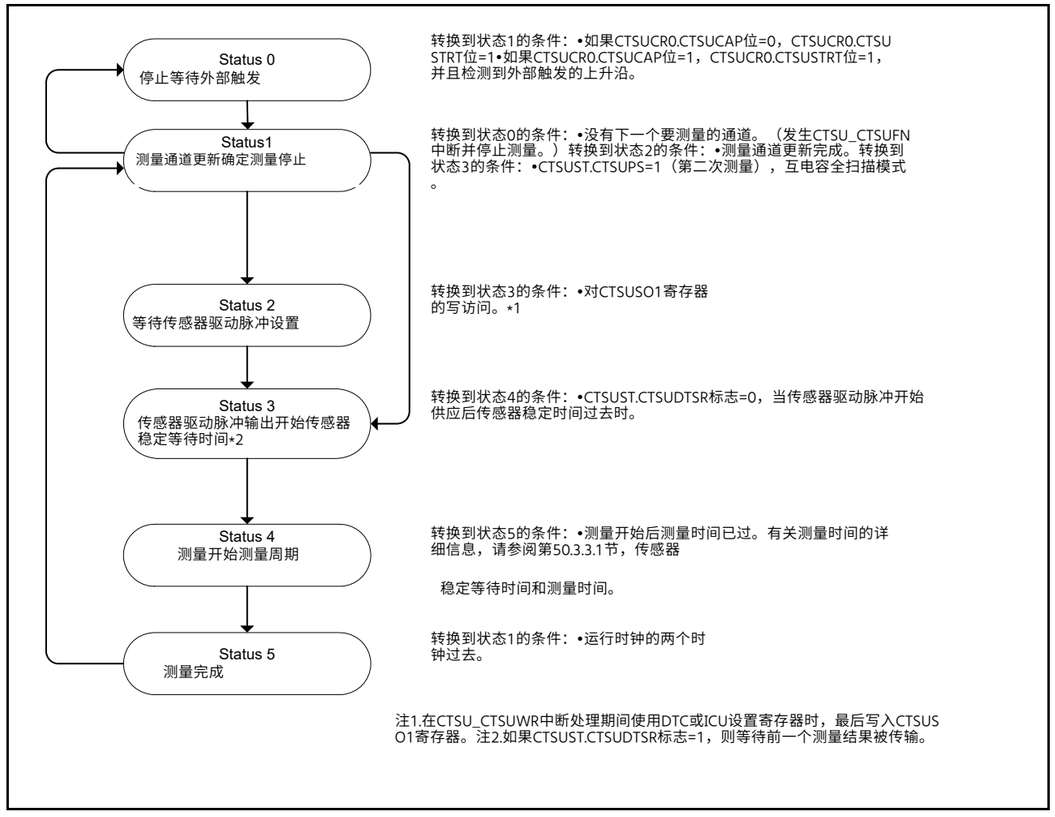


Figure 51.11 状态操作转换

当测量所有指定的测量通道时，状态计数器转换为状态0。

使用软件触发时，CTSUCR0.CTSUSTRT位由硬件清零。使用外部触发时，保留值1，CTSU等待下一次触发。

在测量或触发等待状态期间强制停止操作时，通过同时向CTSUCR0.CTSUSTRT位写入0和向CTSUCR0.CTSUINIT位写入1，状态转换为状态0并停止测量。

如果要测量的通道未在CTSUCHAC0到CTSUCHAC2或CTSUCHTC0到CTSUCHRC2寄存器中设置，则在转换到状态1后立即发生CTSU_CTSUFN中断，然后状态转换到状态0。

在以下情况下，没有要测量的通道：

- CTSUCHAC0至CTSUCHAC2寄存器中未指定测量目标通道。
- 在自电容单次扫描模式下，CTSUCHAC0寄存器中指定的通道不是CTSUCHAC0至CTSUCHAC2寄存器中的测量目标。
- 在全扫描模式下，根据CTSUCHAC0至CTSUCHAC2和CTSUCHTC0至CTSUCHRC2寄存器的组合设置，没有要测量的发送通道或接收通道。

51.3.2.3 Self-capacitance single scan mode operation

In self-capacitance single scan mode, electrostatic capacitance on one channel is measured. Figure 51.12 shows the software flow and an operation example, and Figure 51.13 shows the timing.

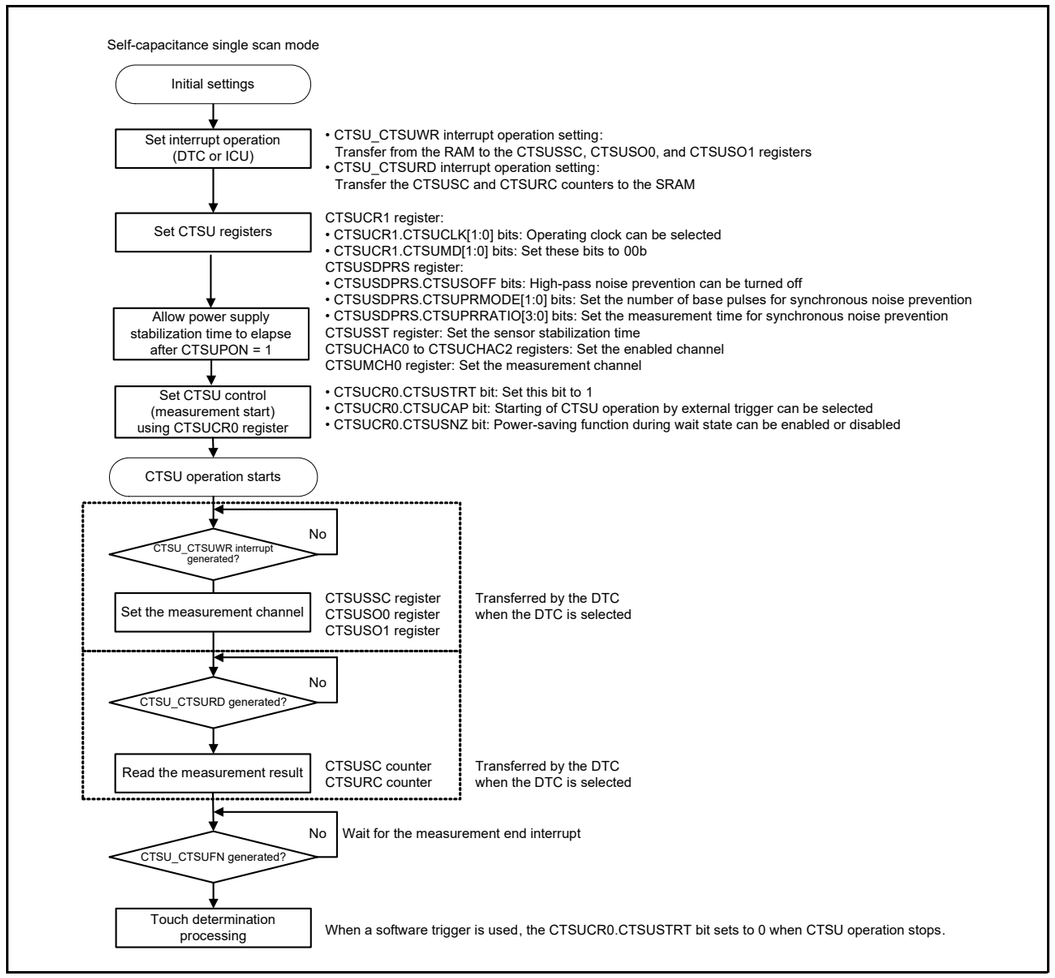


Figure 51.12 Software flow and example operation for self-capacitance single scan mode

51.3.2.3 自电容单次扫描模式操作

在自电容单次扫描模式下，测量一个通道上的静电电容。图51.12显示了软件流程和操作示例，图51.13显示了时序。

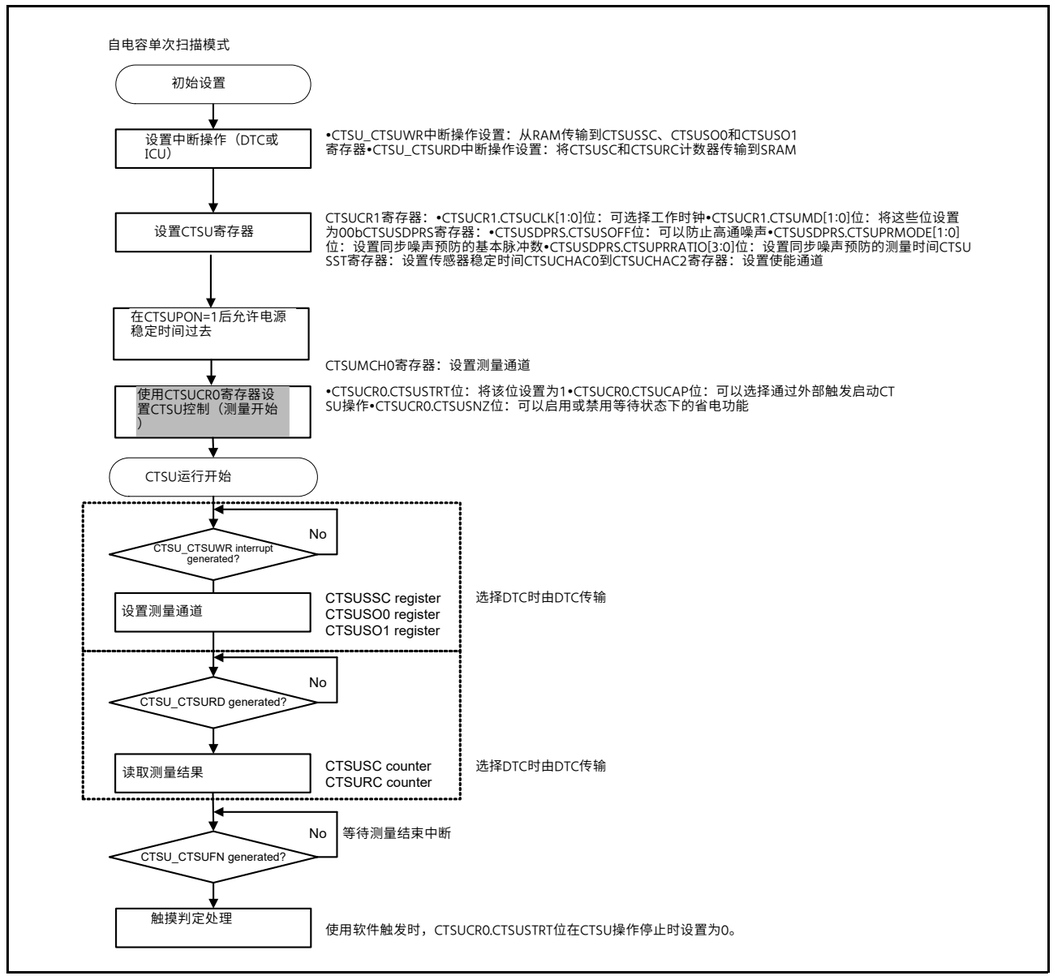


Figure 51.12 自电容单次扫描模式的软件流程和示例操作

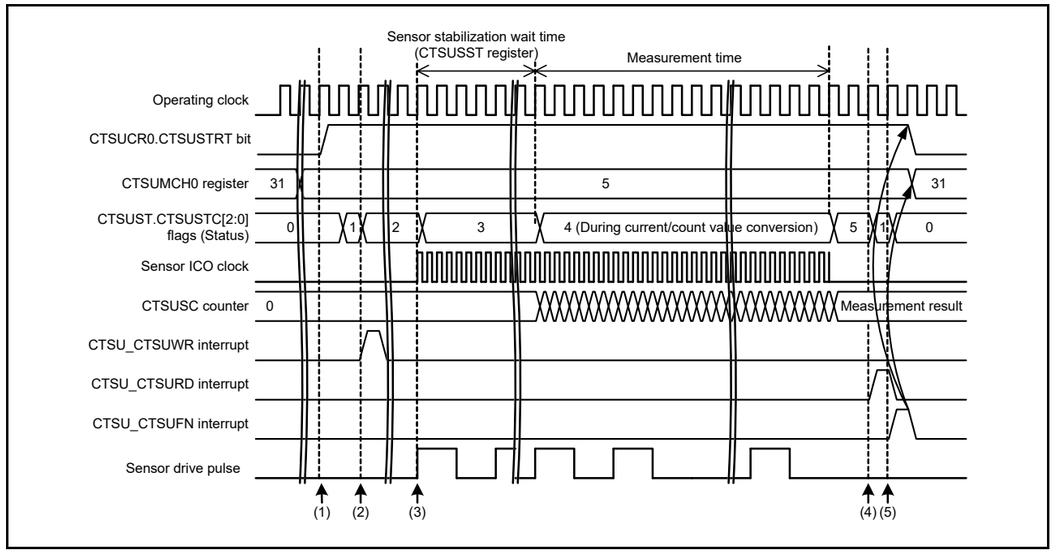


Figure 51.13 Timing of self-capacitance single scan mode when the measurement start condition is a software trigger

The following describes the operation shown in Figure 51.13.

1. After initial settings are made, operation is started by writing 1 to the CTSUCR0.CTSUSTRT bit.
2. After the channel to be measured is determined in accordance with the preset conditions, a request for setting the channel (CTSU_CTSUWR) is output.
3. On completion of writing the measurement channel settings (CTSUSSC, CTSUSO0, and CTSUSO1 registers), the sensor drive pulse is output and the sensor ICO clock and reference ICO clock operate.
4. After the sensor stabilization wait time and the measurement time elapse, and measurement stops, a measurement result read request (CTSU_CTSURD) is output.
5. A measurement end interrupt (CTSU_CTSUFN) is output and measurement stops (transition to Status 0).

Table 51.7 lists the touch pin states in self-capacitance single scan mode.

Table 51.7 Touch pin states in self-capacitance single scan mode

	Touch pin	
Status	**Measured channel**	**Non-measured channel**
0	Low	Low
1	Low	Low
2	Low	Low
3	Pulse	Low
4	Pulse	Low
5	Low	Low

51.3.2.4 Self-capacitance multi-scan mode operation

In self-capacitance multi-scan mode, electrostatic capacitance on all channels that are specified as measurement targets in the CTSUCHAC0 to CTSUCHAC2 registers is measured sequentially in ascending order. Figure 51.14 shows the software flow and an operation example, and Figure 51.15 shows the timing.

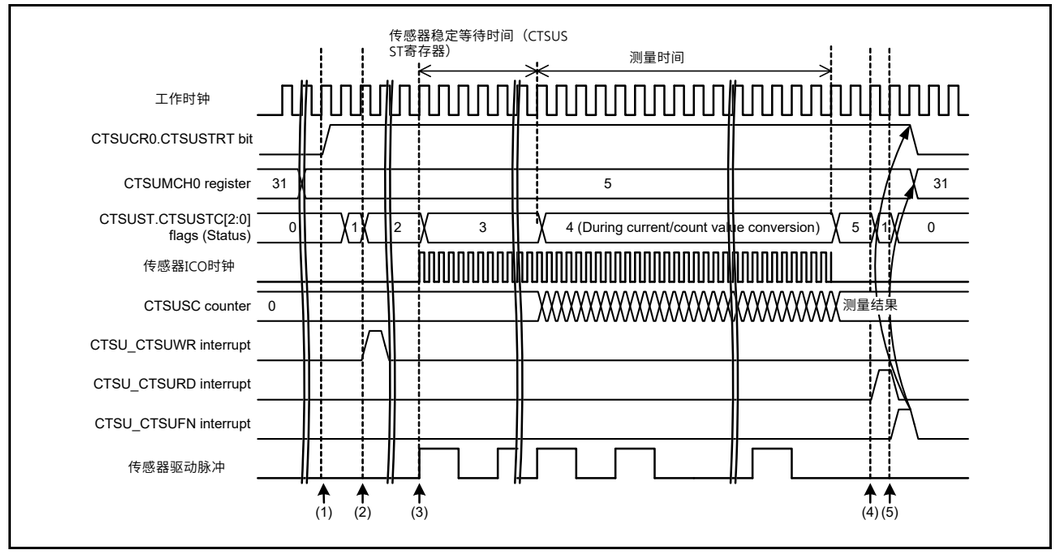


Figure 51.13 测量开始条件为软件触发时的自电容单次扫描模式时序

下面介绍图51.13所示的操作。

1. 进行初始设置后，通过向CTSUCR0.CTSUSTRT位写入1开始操作。
2. 根据预设条件确定待测通道后，输出通道设置请求（CTSU_CTSUWR）。
3. 写入测量通道设置（CTSUSSC、CTSUSO0和CTSUSO1寄存器）完成后，输出传感器驱动脉冲，传感器ICO时钟和参考ICO时钟运行。
4. 在传感器稳定等待时间和测量时间过去，测量停止后，输出测量结果读取请求（CTSU_CTSURD）。
5. 输出测量结束中断(CTSU_CTSUFN)并停止测量（转换到状态0）。

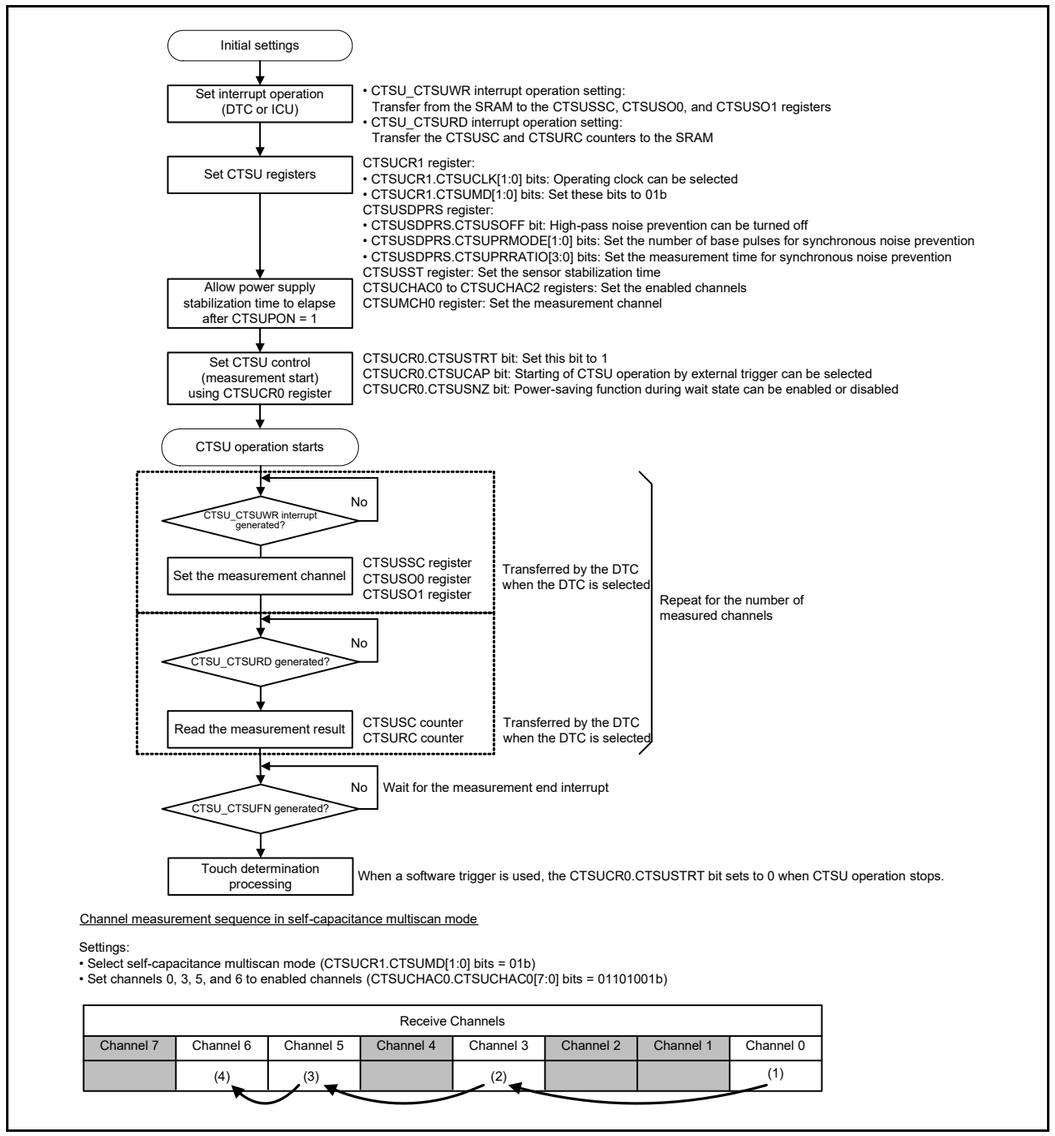
表51.7列出了自电容单次扫描模式下的触摸引脚状态。

Table 51.7 自电容单次扫描模式下的触摸引脚状态

	触摸针	
Status	**测量通道**	**Non-measured channel**
0	Low	Low
1	Low	Low
2	Low	Low
3	Pulse	Low
4	Pulse	Low
5	Low	Low

51.3.2.4 自电容多扫描模式操作

在自电容多重扫描模式下，CTSUCHAC0至CTSUCHAC2寄存器中指定为测量目标的所有通道上的静电电容按升序顺序测量。图51.14显示了软件流程和操作示例，图51.15显示了时序。

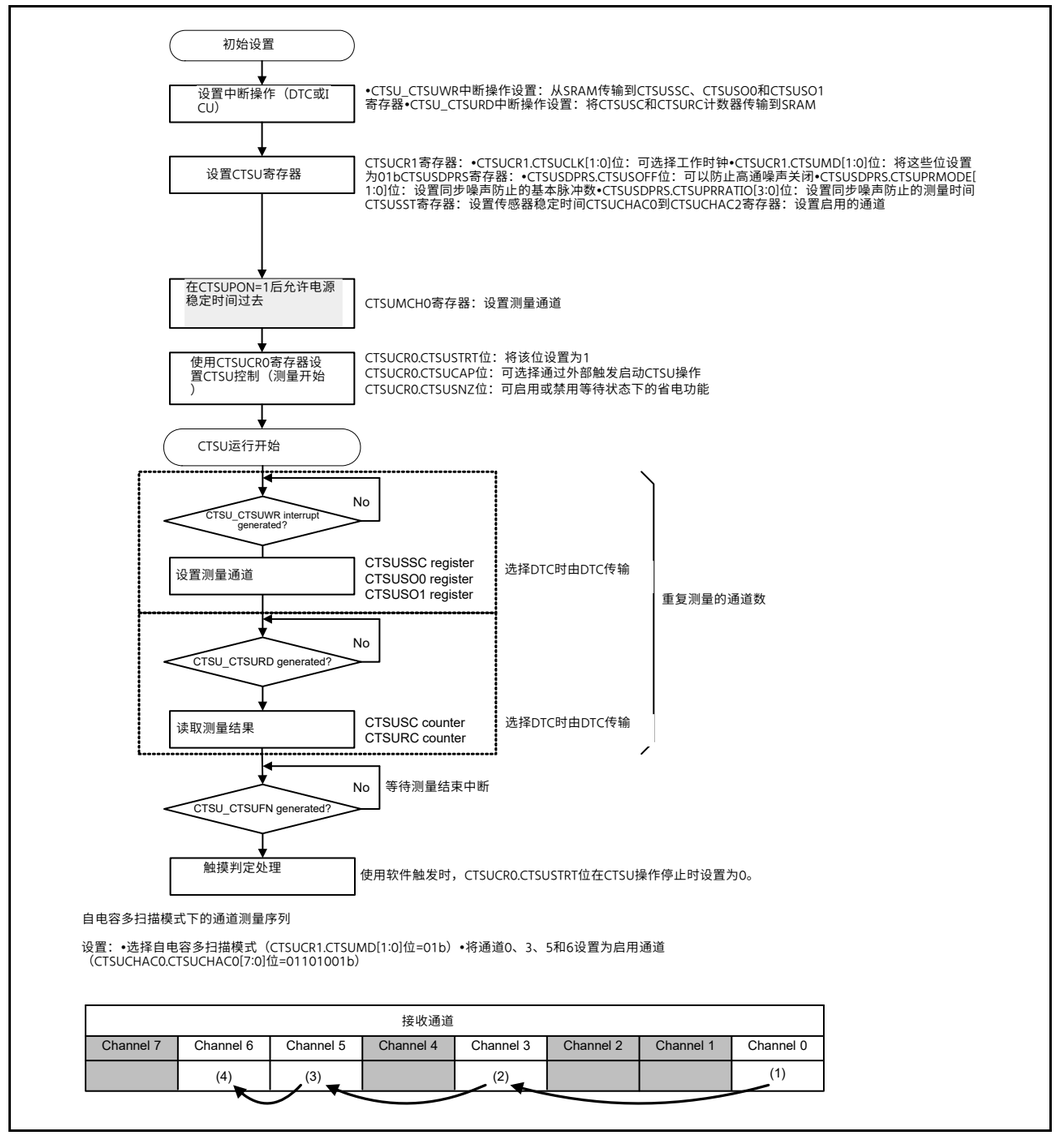


Channel measurement sequence in self-capacitance multiscan mode

Settings:
• Select self-capacitance multiscan mode (CTSUCR1.CTSUMD[1:0] bits = 01b)
• Set channels 0, 3, 5, and 6 to enabled channels (CTSUCHAC0.CTSUCHAC0[7:0] bits = 01101001b)

Receive Channels							
Channel 7	Channel 6	Channel 5	Channel 4	Channel 3	Channel 2	Channel 1	Channel 0
	(4)	(3)		(2)			(1)

Figure 51.14 Software flow and example operation for self-capacitance multi-scan mode



自电容多扫描模式下的通道测量序列

设置：•选择自电容多扫描模式（CTSUCR1.CTSUMD[1:0]位=01b）•将通道0、3、5和6设置为启用通道（CTSUCHAC0.CTSUCHAC0[7:0]位=01101001b）

接收通道							
Channel 7	Channel 6	Channel 5	Channel 4	Channel 3	Channel 2	Channel 1	Channel 0
	(4)	(3)		(2)			(1)

Figure 51.14 自电容多扫描模式的软件流程和示例操作

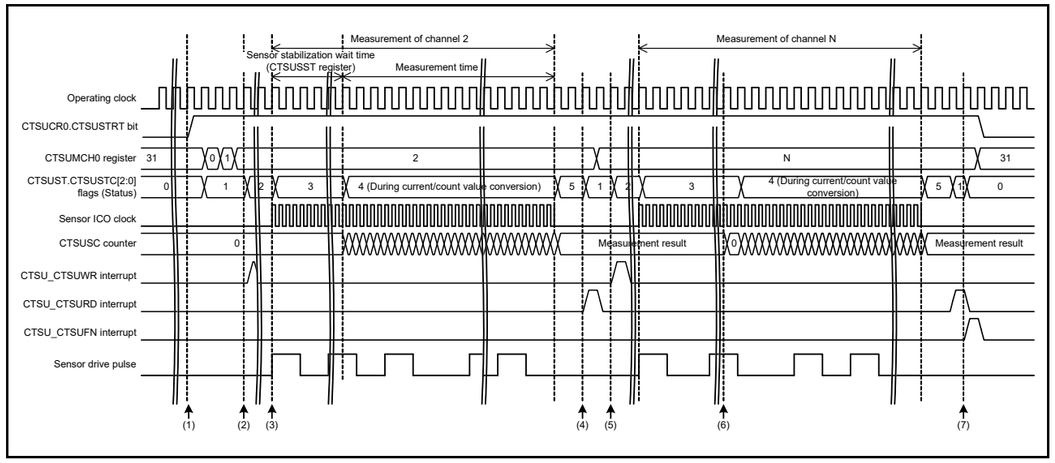


Figure 51.15 Timing of self-capacitance multi-scan mode when the measurement start condition is a software trigger

The following describes the operation shown in Figure 51.15:

1. After initial settings are made, operation is started by writing 1 to the CTSUCR0.CTSUSTRT bit.
2. After the channel to be measured is determined in accordance with the preset conditions, a request for setting the channel (CTSU_CTSUWR) is output.
3. On completion of writing the measurement channel settings (CTSUSSC, CTSUSO0, and CTSUSO1 registers), the sensor drive pulse is output and the sensor ICO clock and the reference ICO clock operate.
4. After the sensor stabilization wait time and the measurement time elapse, and measurement stops, a measurement result read request (CTSU_CTSURD) is output.
5. After the channel to be measured next is determined, a measurement channel setting request (CTSU_CTSUWR) is output.
6. After the stabilization wait time elapses and when the previous measurement is read, the result is cleared and measurement starts.
7. On completion of all measurement channels, a measurement end interrupt (CTSU_CTSUFN) is output and measurement is stopped (transition to Status 0).

Table 51.8 lists the touch pin states in self-capacitance multi-scan mode.

Table 51.8 Touch pin states in self-capacitance multi-scan mode

	Touch pin	
Status	**Measured channel**	**Non-measured channel**
0	Low	Low
1	Low	Low
2	Low	Low
3	Pulse	Low
4	Pulse	Low
5	Low	Low

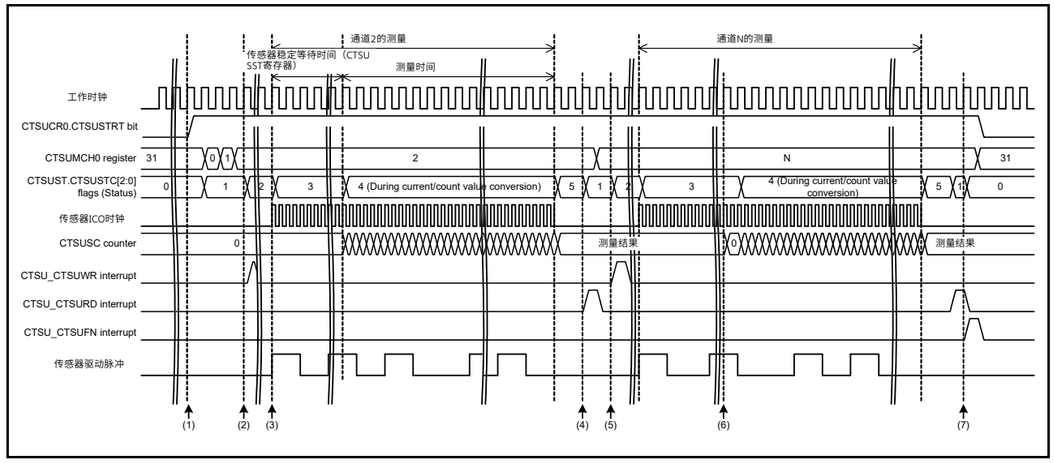


Figure 51.15 测量开始条件为软件触发时的自电容多次扫描模式时序

下面介绍图51.15所示的操作：

1. 进行初始设置后，通过向CTSUCR0.CTSUSTRT位写入1开始操作。
2. 根据预设条件确定待测通道后，输出通道设置请求（CTSU_CTSUWR）。
3. 写入测量通道设置（CTSUSSC、CTSUSO0和CTSUSO1寄存器）完成后，输出传感器驱动脉冲，传感器ICO时钟和参考ICO时钟运行。
4. 在传感器稳定等待时间和测量时间过去，测量停止后，输出测量结果读取请求（CTSU_CTSURD）。
5. 在确定下一个要测量的通道后，输出测量通道设置请求（CTSU_CTSUWR）。
6. 稳定等待时间过去后，当读取前一次测量时，结果将被清除并开始测量。
7. 所有测量通道完成后，将输出测量结束中断(CTSU_CTSUFN)并停止测量（转换到状态0）。

表51.8列出了自电容多扫描模式下的触摸引脚状态。

Table 51.8 自电容多扫描模式下的触摸引脚状态

	触摸针	
Status	**测量通道**	**Non-measured channel**
0	Low	Low
1	Low	Low
2	Low	Low
3	Pulse	Low
4	Pulse	Low
5	Low	Low

51.3.2.5 Mutual capacitance full scan mode operation

In mutual capacitance full scan mode, measurement is performed during the high-level period of the sensor drive pulse on the receive channel by applying the edge to the target transmit channel to be measured. A single measurement target is measured twice, on the rising and falling edges. The difference between the data of these two measurements determines whether or not the electrode was touched, which results in a higher touch sensitivity.

Electrostatic capacitance is measured sequentially on channels set to transmission or reception in the CTSUCHTRC0 to CTSUCHTRC2 registers, and specified as measurement targets in the CTSUCHAC0 to CTSUCHAC2 registers. The capacitance is measured by combining these signals. Figure 51.16 shows the software flow and an operation example, and Figure 51.17 shows the timing.

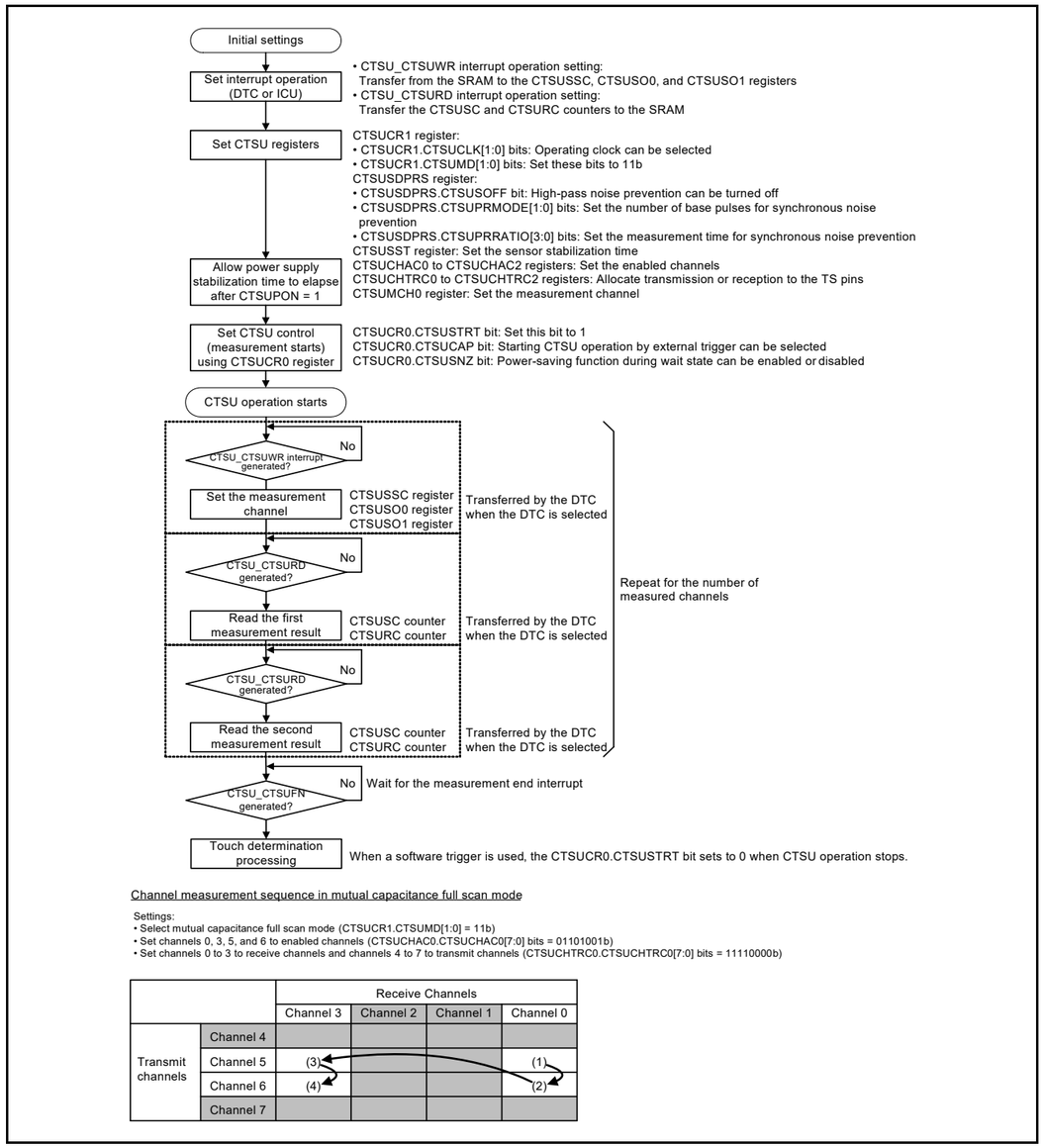


Figure 51.16 Software flow and example operation for mutual capacitance full scan mode

51.3.2.5 互电容全扫描模式操作

在互电容全扫描模式下，在接收通道上的传感器驱动脉冲的高电平期间通过将边沿施加到要测量的目标发送通道来执行测量。在上升沿和下降沿对单个测量目标进行两次测量。这两次测量的数据之间的差异决定了电极是否被触摸，从而导致更高的触摸灵敏度。

在CTSUCHTRC0中设置为发送或接收的通道上依次测量静电电容
CTSUCHAC2寄存器，并在CTSUCHAC0至CTSUCHAC2寄存器中指定为测量目标。通过组合这些信号来测量电容。图51.16显示了软件流程和操作示例，图51.17显示了时序。

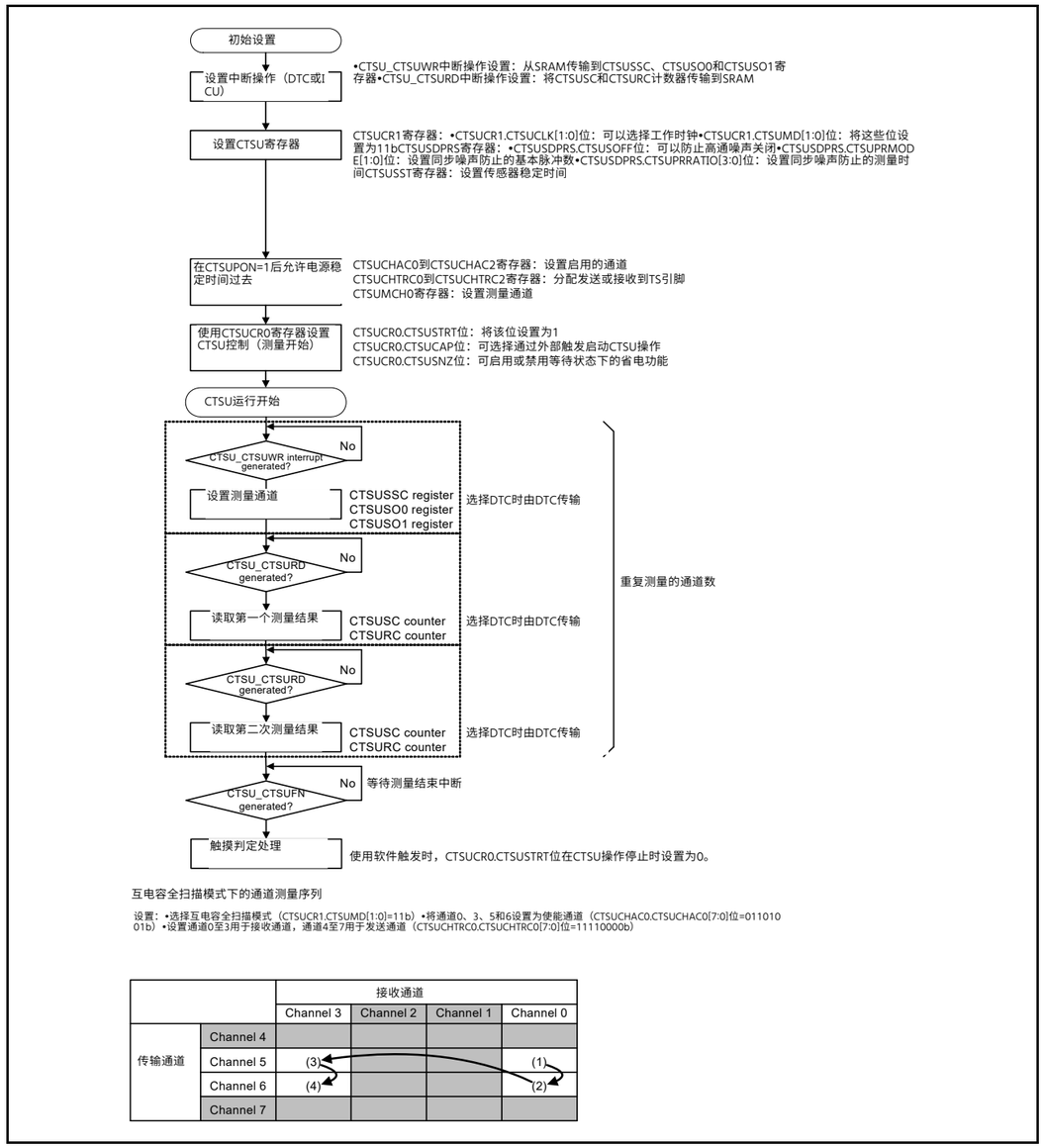


Figure 51.16 互电容全扫描模式的软件流程和示例操作

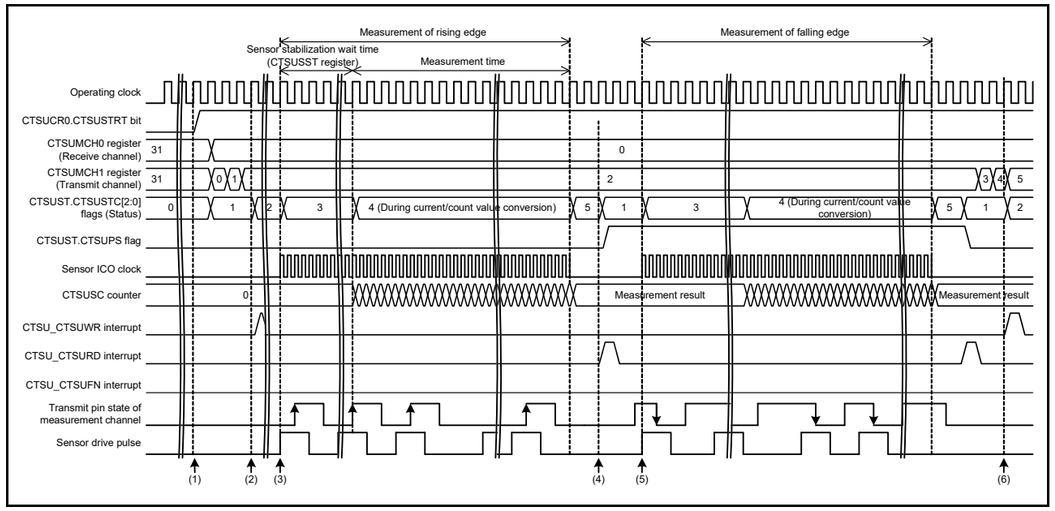


Figure 51.17 Timing of mutual capacitance full scan mode when the measurement start condition is a software trigger

The following describes the operation shown in Figure 51.17.

1. After initial settings are made, operation is started by writing 1 to the CTSUCR0.CTSUSTRT bit.
2. After the channel to be measured is determined in accordance with the preset conditions, a request for setting the channel (CTSU_CTSUWR) is output.
3. On completion of writing the measurement channel settings (CTSUSSC, CTSUSO0, and CTSUSO1 registers), the sensor drive pulse is output and the sensor ICO clock and the reference ICO clock operate. At the same time, a pulse detected on the rising edge is output to the transmit pin on the measurement channel during the high-level period of the sensor drive pulse.
4. After the sensor stabilization wait time and the measurement time elapsed and measurement stops, a measurement result read request (CTSU_CTSURD) is output.
5. The same channel is measured by outputting a pulse detected on the falling edge during the high-level period of the sensor drive pulse.
6. After the same channel is measured twice, the channel to be measured next is determined and measured in the same way.
7. On completion of all measurement channels, a measurement end interrupt (CTSU_CTSUFN) is output and measurement stops (transition to Status 0).

The CTSU mutual capacitance status flag (CTSUST.CTSUPS bit) changes when Status 5 transitions to Status 1.

Table 51.9 lists the touch pin states in mutual capacitance full scan mode.

Table 51.9 Touch pin states in mutual capacitance full scan mode (1 of 2)

Status	Touch pins for receive channels		Touch pins for transmit channels		Remarks
	Measured channel	Non-measured channel	Measured channel	Non-measured channel	
0	Low	Low	Low	Low	-
1	Low	Low	Low/high	Low	-
2	Low	Low	Low	Low	-

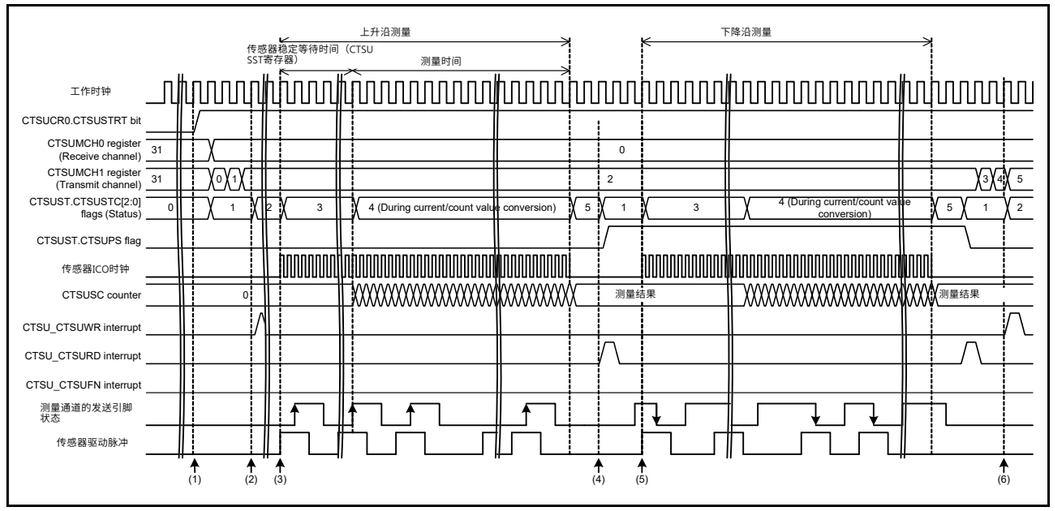


Figure 51.17 测量开始条件为软件触发时互电容全扫描模式的时序

下面介绍图51.17所示的操作。

1. 进行初始设置后，通过向CTSUCR0.CTSUSTRT位写入1开始操作。
2. 根据预设条件确定待测通道后，输出通道设置请求（CTSU_CTSUWR）。
3. 写入测量通道设置（CTSUSSC、CTSUSO0和CTSUSO1寄存器）完成后，输出传感器驱动脉冲，传感器ICO时钟和参考ICO时钟运行。同时，在传感器驱动脉冲的高电平期间，将在上升沿检测到的脉冲输出到测量通道的发送引脚。
4. 在传感器稳定等待时间和测量时间过去并停止测量后，输出测量结果读取请求(CTSU_CTSURD)。
5. 通过在传感器驱动脉冲的高电平期间输出在下降沿检测到的脉冲来测量同一通道。
6. 同一通道测量两次后，确定下一个要测量的通道，以同样的方式进行测量。
7. 所有测量通道完成后，将输出测量结束中断(CTSU_CTSUFN)并停止测量（转换到状态0）。

当状态5转换为状态1时，CTSU互电容状态标志（CTSUST.CTSUPS位）发生变化。

表51.9列出了互电容全扫描模式下的触摸引脚状态。

Table 51.9 互电容全扫描模式下的触摸引脚状态（1of2）

Status	接收通道的触摸引脚		用于传输通道的触摸引脚		Remarks
	测量通道	Non-measured channel	测量通道	Non-measured channel	
0	Low	Low	Low	Low	-
1	Low	Low	Low/high	Low	-
2	Low	Low	Low	Low	-

Table 51.9 Touch pin states in mutual capacitance full scan mode (2 of 2)

Status	Touch pins for receive channels		Touch pins for transmit channels		Remarks
	Measured channel	Non-measured channel	Measured channel	Non-measured channel	
3	Pulse	Low	Pulse	Low	The phase pulse is the same as that of the receive channel on the first measurement and opposite on the second measurement.
4	Pulse	Low	Pulse	Low	-
5	Low	Low	Low	Low	-

51.3.3 Parameters Common to Multiple Modes

51.3.3.1 Sensor stabilization wait time and measurement time

Figure 51.18 shows the timing of the sensor stabilization wait and measurement.

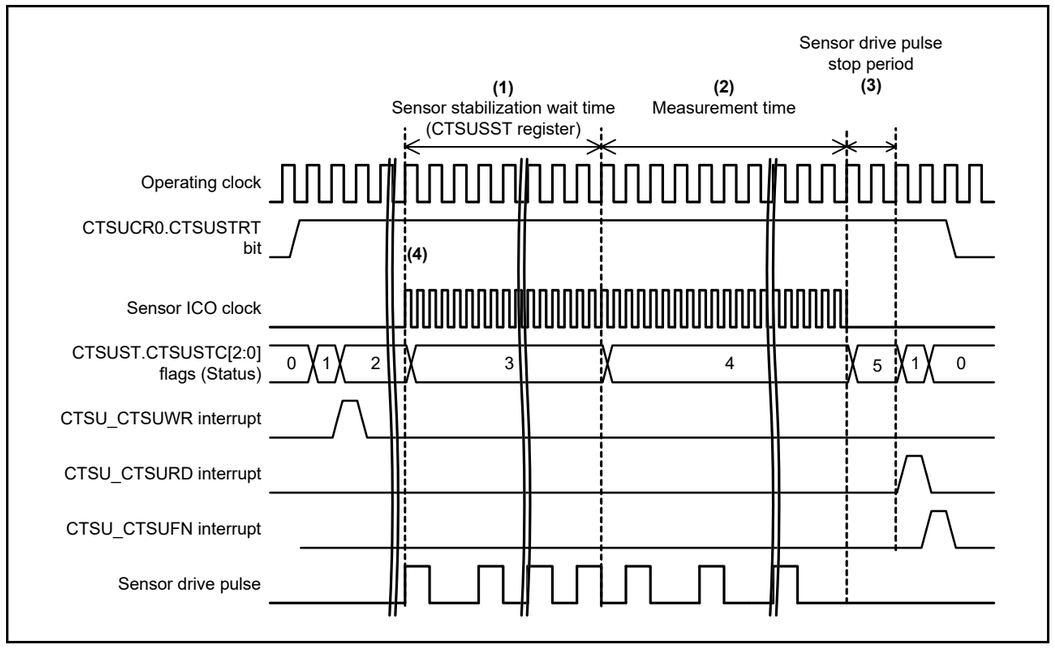


Figure 51.18 Sensor stabilization wait and measurement timing

The following describes the operation shown in Figure 51.18:

1. In response to the CTSU_CTSUWR interrupt request, output of the sensor drive pulse is started by a write access to the CTSUSO1 register. The CTSU waits for the stabilization time set in the CTSUSST register.
2. When the sensor stabilization time elapses and the CTSUST.CTSUDTSR flag clears to 0, measurement starts on transition to Status 4. The measurement time is determined by the base clock cycle setting and the CTSUSDPRS.CTSUPRMODE[1:0], CTSUPRRATIO[3:0], and CTSUSO0.CTSUSNUM[5:0] bits. When the measurement time elapses, measurement of the channel stops.
3. After the measurement time elapses, the status transitions to Status 1 after two operating clock cycles, and a CTSU_CTSURD interrupt occurs. Read the data from the CTSUSC and CTSURC counters. At this time, the sensor drive pulse is output at the low level. When measurement of all specified channels is completed, the CTSUCR0.CTSUSTRT bit clears to 0.
4. The sensor ICO clock oscillates while the CTSUST.CTSUSTC[2:0] flags = 011b (Status 3) or 100b (Status 4).

Table 51.9 互电容全扫描模式下的触摸引脚状态（2个中的2个）

Status	接收通道的触摸引脚		用于传输通道的触摸引脚		Remarks
	测量通道	Non-measured channel	测量通道	Non-measured channel	
3	Pulse	Low	Pulse	Low	相位脉冲在第一次测量时与接收通道的相位脉冲相同，而在第二次测量时则相反。
4	Pulse	Low	Pulse	Low	-
5	Low	Low	Low	Low	-

51.3.3 多种模式共有的参数

51.3.3.1 传感器稳定等待时间和测量时间

图51.18显示了传感器稳定等待和测量的时序。

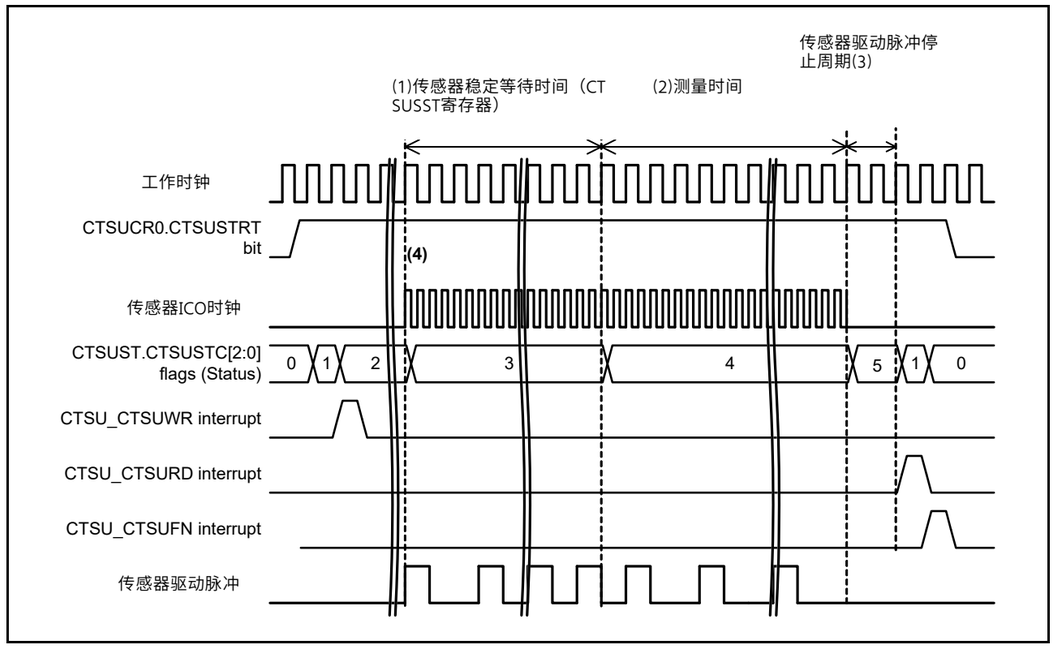


Figure 51.18 传感器稳定等待和测量定时

下面介绍图51.18所示的操作：

1. 响应CTSU_CTSUWR中断请求，通过对CTSUSO1寄存器的写访问开始输出传感器驱动脉冲。CTSU等待CTSUSST寄存器中设置的稳定时间。
2. 当传感器稳定时间过去且CTSUST.CTSUDTSR标志清除为0时，测量开始转换到状态4。测量时间由基本时钟周期设置和CTSUSDPRS.CTSUPRMODE[1:0]、CTSUPRATIO[3:0]和CTSUSO0.CTSUSNUM[5:0]位。当测量时间过去时，通道的测量将停止。
3. 测量时间过去后，状态在两个工作时钟周期后转换为状态1，并且CTSU_CTSURD中断发生。从CTSUSC和CTSURC计数器读取数据。此时，传感器驱动脉冲输出为低电平。完成所有指定通道的测量后，CTSUCR0.CTSUSTRT位清零。
4. 传感器ICO时钟在CTSUST.CTSUSTC[2:0]标志=011b（状态3）或100b（状态4）时振荡。

51.3.3.2 Interrupts

The CTSU supports the following interrupts:

- Write request interrupt for setting registers for each channel (CTSU_CTSUWR)
- Measurement data transfer request interrupt (CTSU_CTSURD)
- Measurement end interrupt (CTSU_CTSUFN).

(1) Write request interrupt for setting registers for each channel (CTSU_CTSUWR)

Store the settings for each measurement channel in the SRAM, and set up the DTC or ICU transfer associated with the CTSU_CTSUWR interrupt in advance. The CTSU_CTSUWR interrupt is output when Status 1 transitions to Status 2. Write the settings for the selected channel from the SRAM to the CTSUSSC, CTSUSO0, and CTSUSO1 registers (Figure 51.19). Because write access to the CTSUSO1 register controls the transition to the next status, you must set this register last.

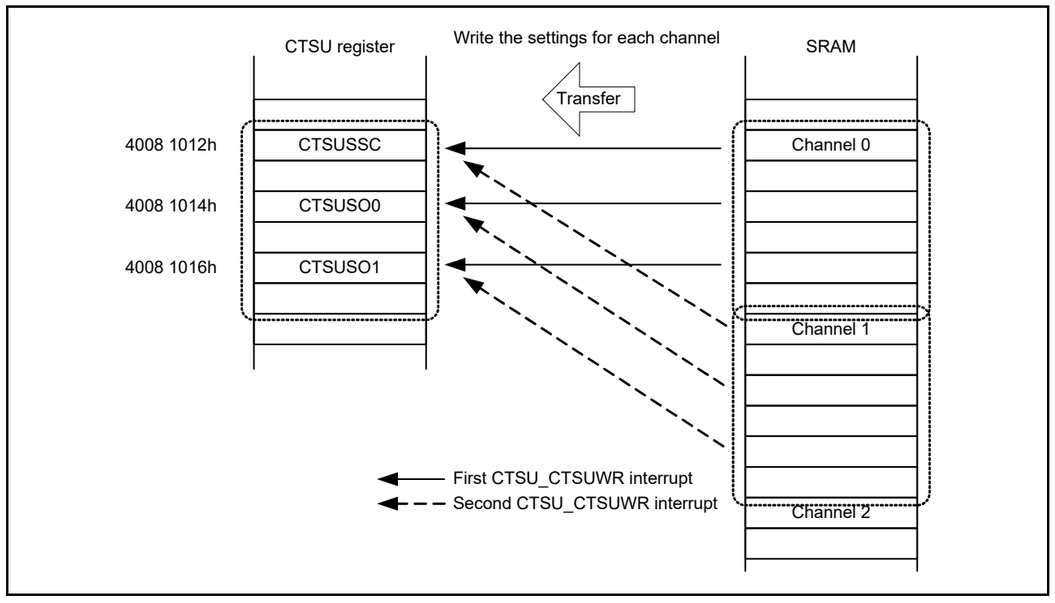


Figure 51.19 Example of DTC transfer operation using the CTSU_CTSUWR interrupt

The registers to be set (CTSUSSC, CTSUSO0, and CTSUSO1) are allocated at sequential addresses. On CTSU_CTSUWR interrupt generation, set up the operation as follows:

- Transfer destination address: CTSUSSC register address
- Handling at the transfer destination address: Transfer 2-byte data three times with a single interrupt. The address of the start byte is fixed
- Transfer source address: CTSUSSC register data storage address for the lowest number channel in the settings stored in the SRAM
- Handling at the transfer source address: Transfer 2-byte data three times with a single interrupt. The address of the first byte is continued from the previous interrupt handling
- Number of transfers per interrupt: Specify the number of measurements.

(2) Measurement data transfer request interrupt (CTSU_CTSURD)

Set up the DTC or ICU transfer associated with the CTSU_CTSURD interrupt in advance. The CTSU_CTSURD interrupt is output when Status 5 transitions to Status 1. Read the measurement result from the CTSUSC and CTSURC counters (Figure 51.20).

51.3.3.2 Interrupts

CTSU支持以下中断：

- 为每个通道设置寄存器的写请求中断(CTSU_CTSUWR)
- 测量数据传输请求中断(CTSU_CTSURD)
- 测量结束中断(CTSU_CTSUFN)。

(1) 为每个通道设置寄存器的写请求中断(CTSU_CTSUWR)

将每个测量通道的设置存储在SRAM中，并提前设置与CTSU_CTSUWR中断相关的DTC或ICU传输。当状态1转换到状态2时输出CTSU_CTSUWR中断。
将所选通道的设置从SRAM写入CTSUSSC、CTSUSO0和CTSUSO1寄存器（图51.19）。因为对CTSUSO1寄存器的写访问控制到下一个状态的转换，所以您必须最后设置该寄存器。

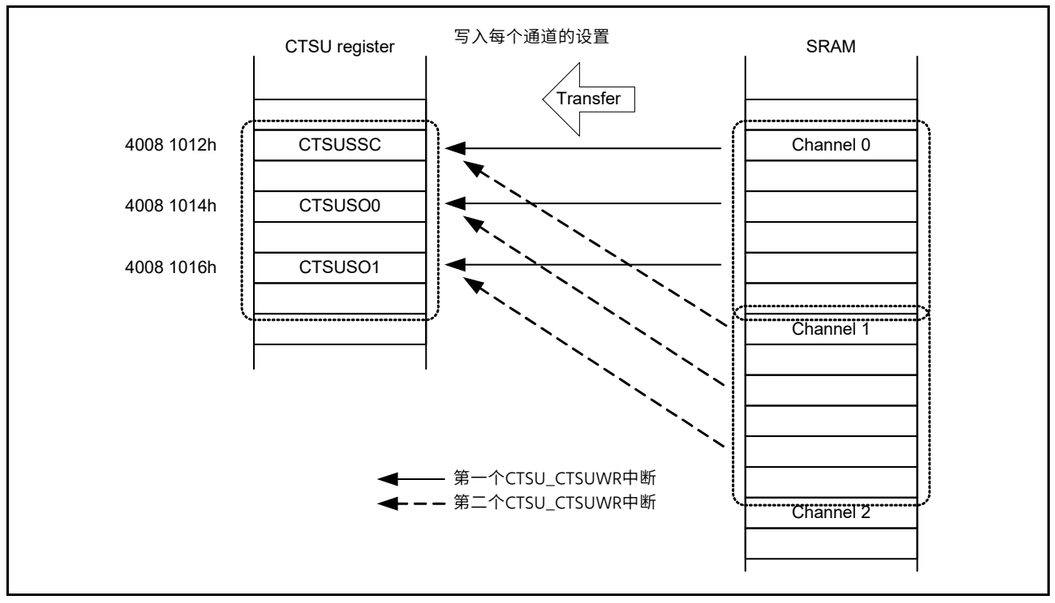


Figure 51.19 使用CTSU_CTSUWR中断的DTC传输操作示例

要设置的寄存器（CTSUSSC、CTSUSO0和CTSUSO1）分配在顺序地址。上
CTSU_CTSUWR中断产生，设置操作如下：

- 传输目标地址：CTSUSSC寄存器地址
- 传送目标地址处的处理：一次中断传送3次2字节数据。起始字节的地址是固定的
- 传输源地址：CTSUSSC寄存器数据存储地址，用于SRAM中存储的设置中编号最小的通道
- 传输源地址处的处理：一次中断传输3次2字节数据。第一个字节的地址从之前的中断处理继续
- 每次中断的传输次数：指定测量次数。

(2) 测量数据传输请求中断(CTSU_CTSURD)

提前设置与CTSU_CTSURD中断相关的DTC或ICU传输。当状态5转换为状态1时输出CTSU_CTSURD中断。从CTSUSC和CTSURC计数器读取测量结果（图51.20）。

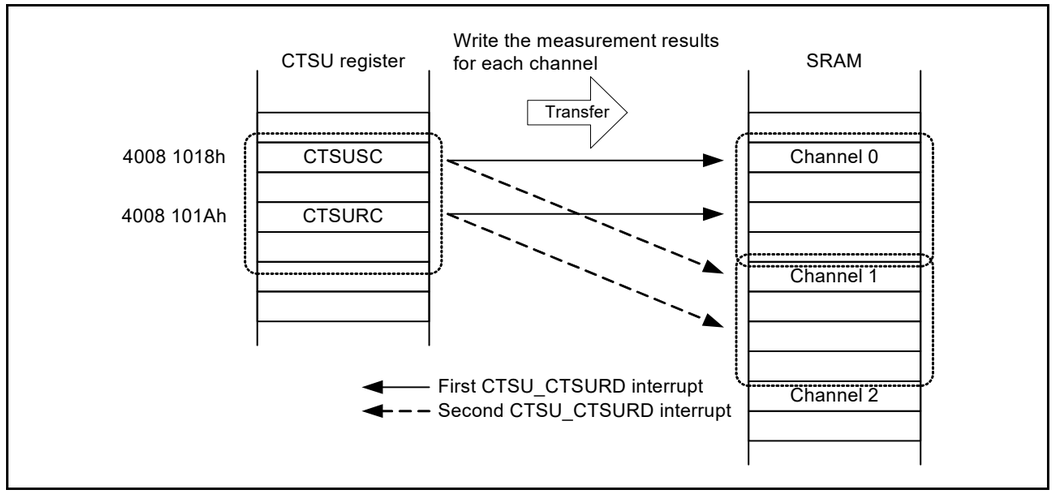


Figure 51.20 Example of DTC transfer operation using the CTSU_CTSURD interrupt

The measurement result registers (CTSUSC and CTSURC counters) used as transfer sources are allocated at sequential addresses. On CTSU_CTSURD interrupt generation, set up the operation as follows:

- Transfer source address: CTSUSC counter address
- Handling at the transfer source address: Transfer 2-byte data twice with a single interrupt. The start address is fixed
- Transfer destination address: CTSUSC counter data storage address for the lowest number channel in the settings stored in the SRAM
- Handling at the transfer destination address: Transfer 2-byte data twice with a single interrupt. The start address is continued from the previous interrupt handling
- Number of transfers per interrupt: Specify the number of measurements.

(3) Measurement end interrupt (CTSU_CTSUFN)

When all channels are measured, an interrupt occurs when Status 1 transitions to Status 0. In the software, check the overflow flags (CTSUST.CTSUSOVF and CTSUROVF) and read the measurement results to determine whether or not the electrode was touched. Interrupt requests are accepted or disabled in the interrupt control block.

51.4 Usage Notes

51.4.1 Measurement Result Data (CTSUSC and CTSURC Counters)

Read access during measurement is prohibited. If the measurement result data is accessed, an incorrect value might be read because of asynchronous operation.

51.4.2 Constraint on Software Trigger

When 10b (PCLKB/4) is selected in the CTSUCR1.CTSUCLK[1:0] bits, to restart measurement by writing 1 to the CTSUR0.CTSUSTRT bit after measurement is complete, wait for at least 3 cycles to elapse after an interrupt occurs, and then write to the CTSUCR0.CTSUSTRT bit.

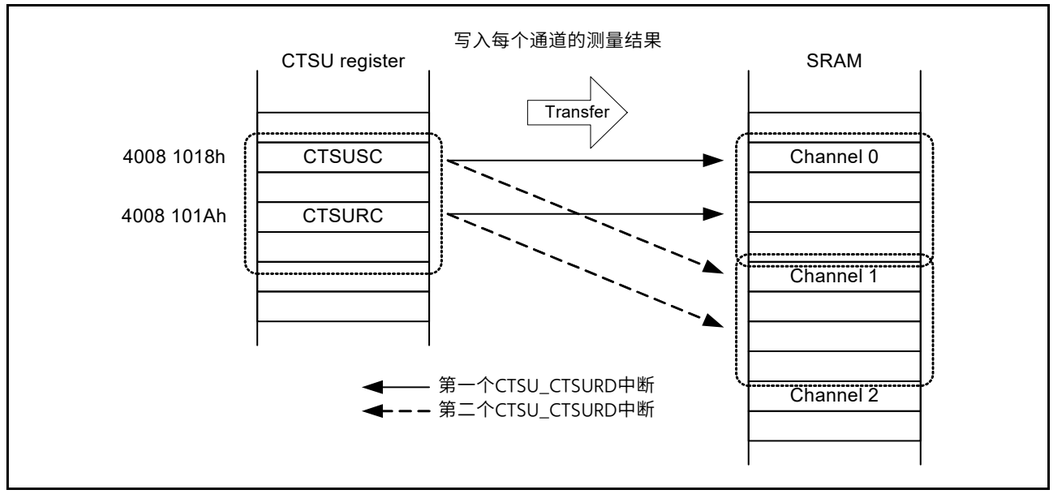


Figure 51.20 使用CTSU_CTSURD中断的DTC传输操作示例

用作传输源的测量结果寄存器（CTSUSC和CTSURC计数器）按顺序分配。在CTSU_CTSURD中断生成时，按如下方式设置操作：

- 传输源地址：CTSUSC计数器地址
- 传输源地址处的处理：用一个中断传输2字节数据两次。起始地址是固定的
- 传送目标地址：SRAM中存储的设置中最小编号通道的CTSUSC计数器数据存储地址
- 传送目标地址处的处理：用一个中断传送2字节数据两次。起始地址从上一个中断处理继续
- 每次中断的传输次数：指定测量次数。

(3) 测量结束中断(CTSU_CTSUFN)

测量所有通道时，状态1转换为状态0时发生中断。在软件中，检查溢出标志（CTSUST.CTSUSOVF和CTSUROVF）并读取测量结果以确定电极是否被触摸。在中断控制块中接受或禁用中断请求。

51.4 使用说明

51.4.1 测量结果数据（CTSUSC和CTSURC计数器）

禁止在测量期间进行读取访问。如果访问测量结果数据，可能会因为异步操作而读取到不正确的值。

51.4.2 软件触发约束

当在CTSUCR1.CTSUCLK[1:0]位中选择10b(PCLKB4)时，通过将1写入
测量完成后CTSUR0.CTSUSTRT位，在发生中断后至少等待3个周期，然后写入CTSUCR0.CTSUSTRT位。

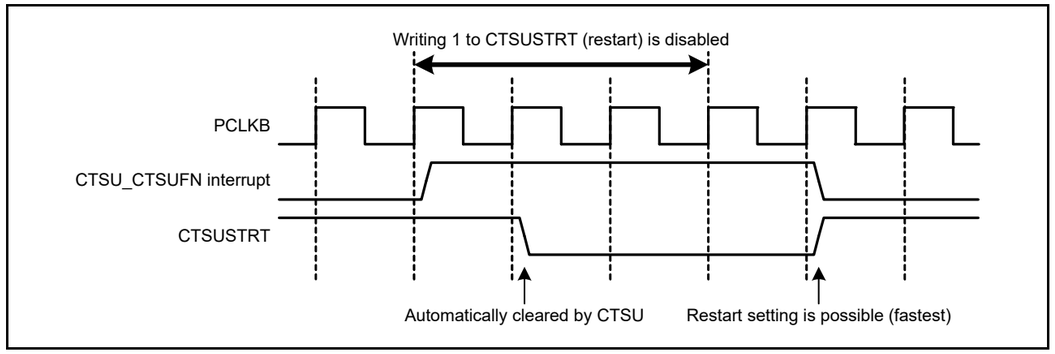


Figure 51.21 Notes on restarting measurement

51.4.3 Constraints on External Triggers

- If an external trigger is input during the measurement time, measurement does not start. The next external event is enabled after 1 cycle of the operating clock when a CTSU_CTSUFN interrupt occurs.
- To stop external trigger mode, write 0 to the CTSUCR0.CTSUSTRT bit and 0 to the CTSUCR0.CTSUINIT bit at the same time (forced stop).

51.4.4 Constraints on Forced Stops

To force the current operation to stop, write 0 to the CTSUCR0.CTSUSTRT bit and 1 to the CTSUCR0.CTSUINIT bit at the same time. After this setting, the operation is stopped and the internal control registers are initialized.

When the CTSUCR0.CTSUINIT bit is used for initialization, the following registers are initialized in addition to the initialization of the internal measurement state.

- CTSUMCH0 register
- CTSUMCH1 register
- CTSUST register
- CTSUSC counter
- CTSURC counter.

If operation is forced to stop, an interrupt request might be generated depending on the internal state. After a forced stop, also perform the processing for stopping and disabling the DTC or ICU. If a DTC transfer is stopped in an installed system for some reason, also perform the processing for forcing stop to and initializing the CTSU.

51.4.5 TSCAP Pin

The TSCAP pin requires an external decoupling capacitor to stabilize CTSU internal voltage. The traces between the TSCAP pin and the capacitor, and the capacitor and ground should be as short and wide as physically possible.

The capacitor connected to the TSCAP pin should be fully discharged using I/O port control to output a low level, before turning on the switch (CTSUCR1.CTSUCSW bit = 1) to establish a connection.

51.4.6 Constraints on Measurement Operation (CTSUCR0.CTSUSTRT Bit = 1)

During measurement (CTSUCR0.CTSUSTRT bit = 1), do not use the settings for stopping the peripheral clock or changing the port settings related to the touch pins (TSn and TSCAP pins) and Transmission power supply selection (CTSUCR0.CTSUTXVSEL) in the higher layers of the system.

If control settings non-compliant with these constraints are made, operation is forced to stop (CTSUCR0.CTSUSTRT bit = 0 and CTSUCR0.CTSUINIT bit = 1), write 0 to the CTSUCR1.CTSUPON bit and 0 to the CTSUCR1.CTSUCSW bit at the same time, and set the CTSUCR0.CTSUSNZ bit to 0. Next, restart from the initial settings flow shown in Figure 51.9.

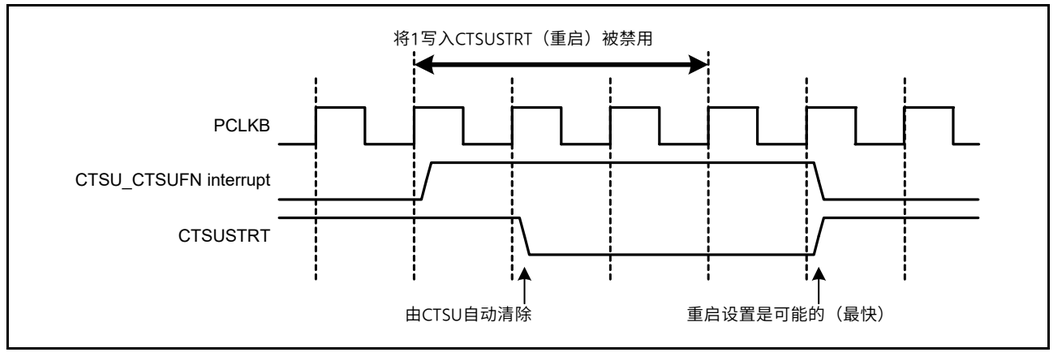


Figure 51.21 重新开始测量的注意事项

51.4.3 外部触发器的约束

- 如果在测量期间输入外部触发，测量不会开始。当CTSU_CTSUFN中断发生时，下一个外部事件在工作时钟的1个周期后启用。
- 要停止外部触发模式，同时向CTSUCR0.CTSUSTRT位写入0和向CTSUCR0.CTSUINIT位写入0（强制停止）。

51.4.4 强制停止的约束

要强制停止当前操作，请同时向CTSUCR0.CTSUSTRT位写入0，向CTSUCR0.CTSUINIT位写入1。设置完成后，操作停止，内部控制寄存器初始化。

当CTSUCR0.CTSUINIT位用于初始化时，除了内部测量状态的初始化之外，还初始化以下寄存器。

- CTSUMCH0 register
- CTSUMCH1 register
- CTSUST register
- CTSUSC counter
- CTSURC counter.

如果操作被强制停止，根据内部状态可能会产生中断请求。强制停止后，还要执行停止和禁用DTC或ICU的处理。如果由于某种原因在已安装的系统中停止了DTC传输，则还要执行强制停止和初始化CTSU的处理。

51.4.5 TSCAP Pin

TSCAP引脚需要一个外部去耦电容来稳定CTSU内部电压。之间的痕迹
TSCAP引脚和电容器，以及电容器和地线应尽可能短且宽。

在打开开关（CTSUCR1.CTSUCSW位=1）建立连接之前，应使用IO端口控制将连接到TSCAP引脚的电容器完全放电以输出低电平。

51.4.6 测量操作的限制（CTSUCR0.CTSUSTRT位=1）

在测量期间（CTSUCR0.CTSUSTRT位=1），请勿使用与触摸引脚（TSn和TSCAP引脚）和发送电源选择（CTSUCR0.CTSUTXVSEL）相关的端口设置停止外围时钟或更改高位系统的层次。

如果进行了不符合这些约束的控制设置，则强制停止操作（CTSUCR0.CTSUSTRT位=0且CTSUCR0.CTSUINIT位=1），将0写入CTSUCR1.CTSUPON位并将0写入CTSUCR1.CTSUCSW位同时，将CTSUCR0.CTSUSNZ位设置为0。接下来，从图51.9所示的初始设置流程重新启动。

52. Data Operation Circuit (DOC)

52.1 Overview

The Data Operation Circuit (DOC) is used to compare, add, and subtract 16-bit data. When a selected condition applies, 16-bit data is compared and an interrupt can be generated. Table 52.1 lists the DOC specifications and Figure 52.1 shows a block diagram.

Table 52.1 DOC specifications

Parameter	Specifications
Data operation function	16-bit data comparison, addition, and subtraction
Module-stop function	Module-stop state can be set to reduce power consumption
Interrupts and event link function (DOC_DOPCI)	An interrupt occurs on the following conditions: • Compared values either match or mismatch • Data addition result is greater than FFFFh • Data subtraction result is less than 0000h

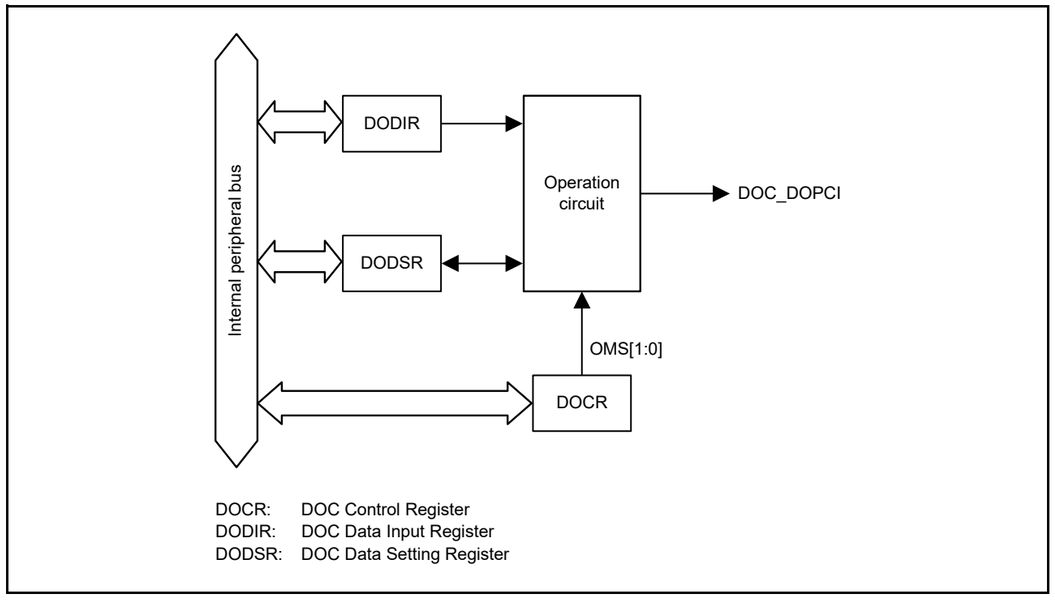


Figure 52.1 DOC block diagram

52. 数据运算电路(DOC)

52.1 Overview

数据运算电路(DOC)用于比较、加和减16位数据。当适用选定条件时，比较16位数据并可以生成中断。表52.1列出了DOC规范，图52.1显示了框图。

Table 52.1 文档规范

Parameter	Specifications
数据运算功能	16位数据比较、加法和减法
Module-stop function	可设置模块停止状态以降低功耗
中断和事件链接功能（DOC_DOPCI）	在以下条件下发生中断： 比较值匹配或不匹配 数据加法结果大于FFFFh 数据减法结果小于0000h

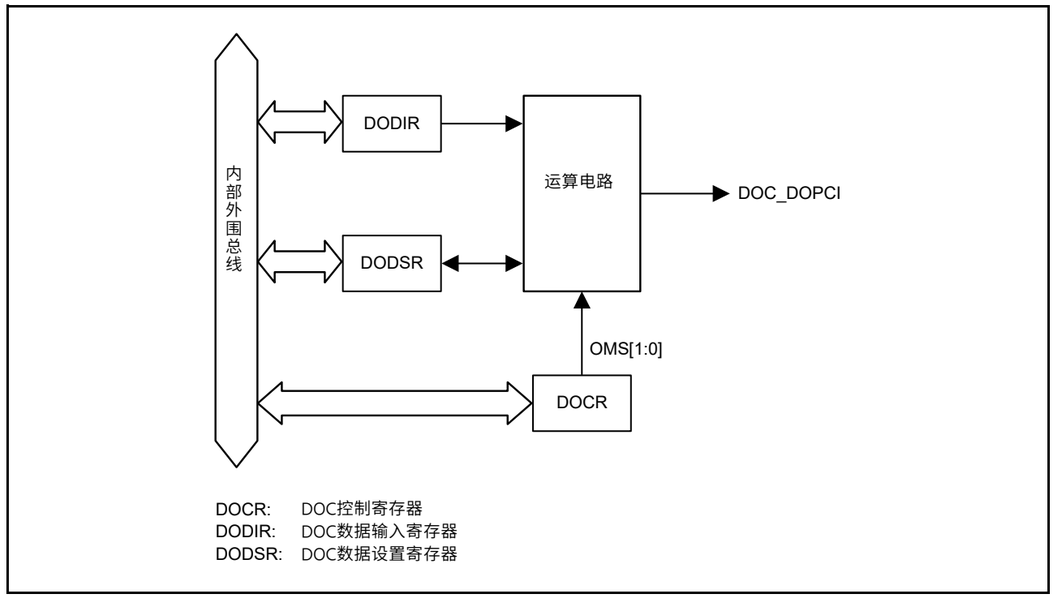


Figure 52.1 文档框图

52.2 Register Descriptions

52.2.1 DOC Control Register (DOCR)

Address(es): DOC.DOCR 4005 4100h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	DOPCFCL	DOPCF	—	—	DCSEL	OMS[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	OMS[1:0]	Operating Mode Select	b1 b0 0 0: Data comparison mode 0 1: Data addition mode 1 0: Data subtraction mode 1 1: Setting prohibited.	R/W
b2	DCSEL*1	Detection Condition Select	0: Set DOPCF when data mismatch detected 1: Set DOPCF when data match detected.	R/W
b4, b3	—	Reserved	There bits are read as 0. The write value should be 0.	R/W
b5	DOPCF	Data Operation Circuit Flag	Indicates the result of an operation.	R
b6	DOPCFCL	DOPCF Clear	0: Retain DOPCF flag state 1: Clear DOPCF flag.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Note 1. Only valid when data comparison mode is selected.

OMS[1:0] bits (Operating Mode Select)

The OMS[1:0] bits select the operating mode of the DOC.

DCSEL bit (Detection Condition Select)

The DCSEL bit selects the detection condition in data comparison mode. This bit is only valid when data comparison mode is selected.

DOPCF flag (Data Operation Circuit Flag)

The DOPCF flag indicates the result of an operation.

[Setting conditions]

- The condition selected in the DCSEL bit is met
- A data addition result is greater than FFFFh
- A data subtraction result is less than 0000h.

[Clearing condition]

- Writing 1 to the DOPCFCL bit.

DOPCFCL bit (DOPCF Clear)

Setting the DOPCFCL bit to 1 clears the DOPCF flag. This bit is read as 0.

52.2 注册说明

52.2.1 DOC控制寄存器(DOCR)

Address(es): DOC.DOCR 4005 4100h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	DOPCFCL	DOPCF	—	—	DCSEL	OMS[1:0]	
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b1, b0	OMS[1:0]	操作模式选择	b1b000：数据比较模式01： 数据加法模式10：数据减法 模式11：禁止设置。	R/W
b2	DCSEL*1	检测条件选择	0：检测到数据不匹配时置位DOPCF1：检测 到数据匹配时置位DOPCF。	R/W
b4, b3	—	Reserved	有位被读取为0。写入值应为0。	R/W
b5	DOPCF	数据运算电路标志	表示操作的结果。	R
b6	DOPCFCL	DOPCF Clear	0：保持DOPCF标志状态1 ：清除DOPCF标志。	R/W
b7	—	Reserved	该位读取为0。写入值应为0。	R/W

Note 1. 仅在选择数据比较模式时有效。

OMS[1:0]位（操作模式选择）

OMS[1:0]位选择DOC的工作模式。

DCSEL位（检测条件选择）

DCSEL位选择数据比较模式下的检测条件。该位仅在选择数据比较模式时有效。

DOPCF标志（数据操作电路标志）

DOPCF标志指示操作的结果。

[Setting conditions]

- 满足在DCSEL位中选择的条件
- 数据相加结果大于FFFFh
- 数据减法结果小于0000h。

[Clearing condition]

- 将1写入DOPCFCL位。

DOPCFCL位（DOPCF清除）

将DOPCFCL位设置为1会清除DOPCF标志。该位读为0。

52.2.2 DOC Data Input Register (DODIR)

Address(es): DOC.DODIR 4005 4102h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DODIR is a 16-bit read/write register that stores 16-bit data used in the operations.

52.2.3 DOC Data Setting Register (DODSR)

Address(es): DOC.DODSR 4005 4104h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DODSR is a 16-bit read/write register that stores 16-bit data used as a reference in data comparison mode. This register also stores the results of operations in data addition and subtraction modes.

52.3 Operation

52.3.1 Data Comparison Mode

Figure 52.2 shows an example of the steps involved in data comparison mode operation by the DOC. The following is an example operation when DCSEL is set to 0 (data mismatch is detected as a result of data comparison):

1. Write 00b to the DOCR.OMS[1:0] bits to select data comparison mode.
2. Set 16-bit reference data in DODSR.
3. Write 16-bit data for comparison to DODIR.
4. Continue writing 16-bit data until all data for comparison is written to DODIR.
5. If a value written to DODIR does not match that in DODSR,*1 the DOCR.DOPCF flag sets to 1.

Note 1. When DOCR.DCSEL = 0

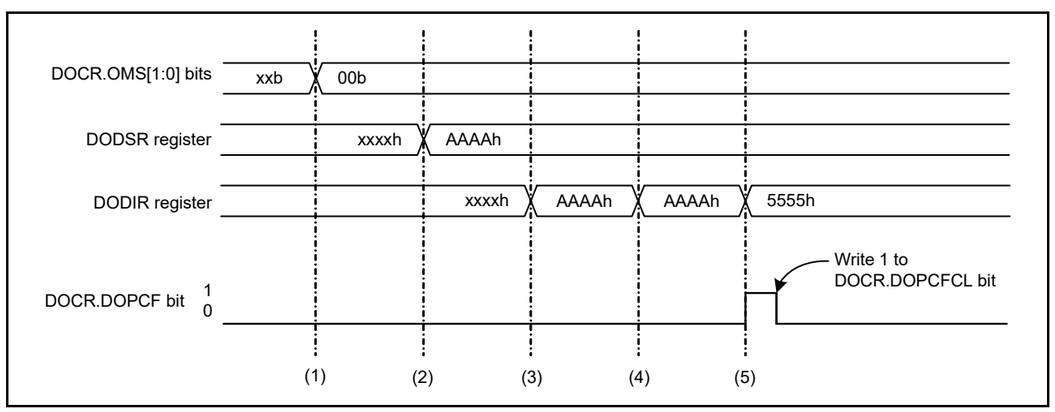


Figure 52.2 Example of operation in data comparison mode

52.2.2 DOC数据输入寄存器(DODIR)

Address(es): DOC.DODIR 4005 4102h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DODIR是一个16位读写寄存器，用于存储操作中使用的16位数据。

52.2.3 DOC数据设置寄存器(DODSR)

Address(es): DOC.DODSR 4005 4104h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

DODSR是一个16位读写寄存器，用于存储16位数据，在数据比较模式下用作参考。该寄存器还存储数据加法和减法模式下的运算结果。

52.3 Operation

52.3.1 数据比较模式

图52.2显示了DOC在数据比较模式操作中涉及的步骤示例。以下是DCSEL设置为0时的示例操作（通过数据比较检测到数据不匹配）：

1. 将00b写入DOCR.OMS[1:0]位以选择数据比较模式。
2. 在DODSR中设置16位参考数据。
3. 写入16位数据以与DODIR进行比较。
4. 继续写入16位数据，直到所有用于比较的数据都写入DODIR。
5. 如果写入DODIR的值与DODSR中的值不匹配，*1DOCR.DOPCF标志设置为1。

注1.当DOCR.DCSEL=0时

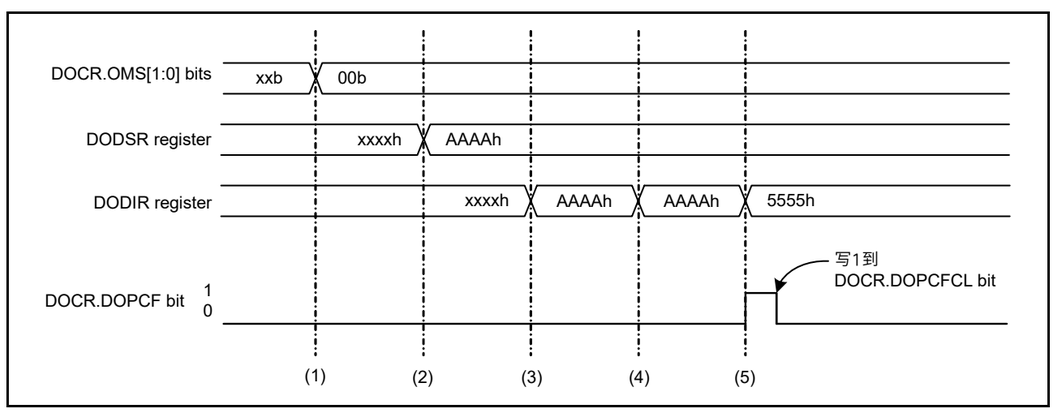


Figure 52.2 数据比较模式的操作示例

52.3.2 Data Addition Mode

Figure 52.3 shows an example of the steps involved in data addition mode operation by the DOC:

1. Write 01b to the DOCR.OMS[1:0] bits to select data addition mode.
2. Set 16-bit data in the DODSR register as the initial value.
3. Write 16-bit data to be added to DODIR. The result of the operation is stored in DODSR.
4. Continue writing 16-bit data until all data for addition is written to DODIR.
5. If the result of an operation is greater than FFFFh, the DOCR.DOPCF flag sets to 1.

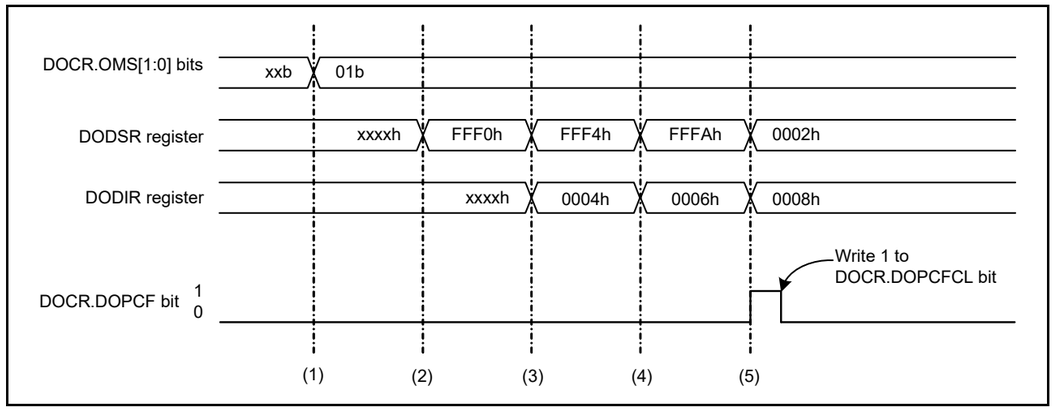


Figure 52.3 Example of operation in data addition mode

52.3.3 Data Subtraction Mode

Figure 52.4 shows an example of the steps involved in data subtraction mode operation by the DOC:

1. Write 10b to the DOCR.OMS[1:0] bits to select data subtraction mode.
2. Set 16-bit data in the DODSR register as the initial value.
3. Write 16-bit data to be subtracted to DODIR. The result of the operation is stored in DODSR.
4. Continue writing 16-bit data until all data for subtraction is written to DODIR.
5. If the result of an operation is less than 0000h, the DOCR.DOPCF flag sets to 1.

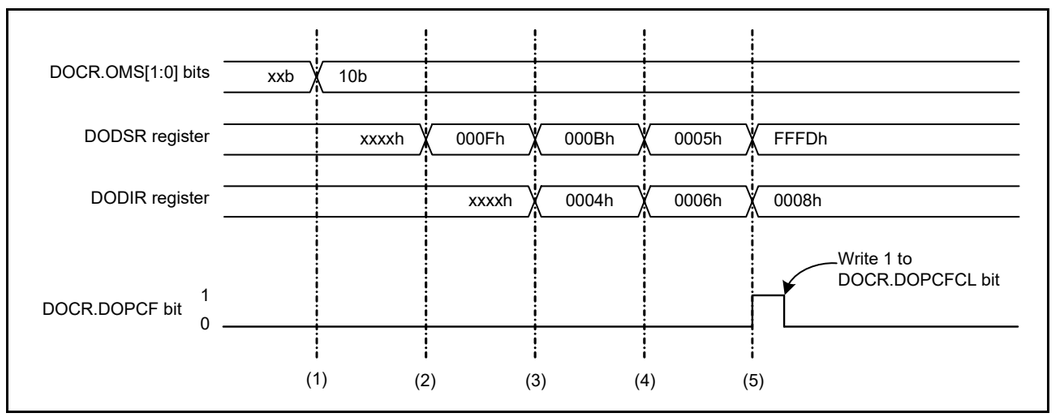


Figure 52.4 Example of operation in data subtraction mode

52.3.2 数据加法模式

图52.3显示了DOC在数据添加模式操作中涉及的步骤示例：

1. 将01b写入DOCR.OMS[1:0]位以选择数据添加模式。
2. 将DODSR寄存器中的16位数据设置为初始值。
3. 写入要添加到DODIR的16位数据。操作结果存储在DODSR中。
4. 继续写入16位数据，直到所有要添加的数据都写入DODIR。
5. 如果运算结果大于FFFFh，则DOCR.DOPCF标志设置为1。

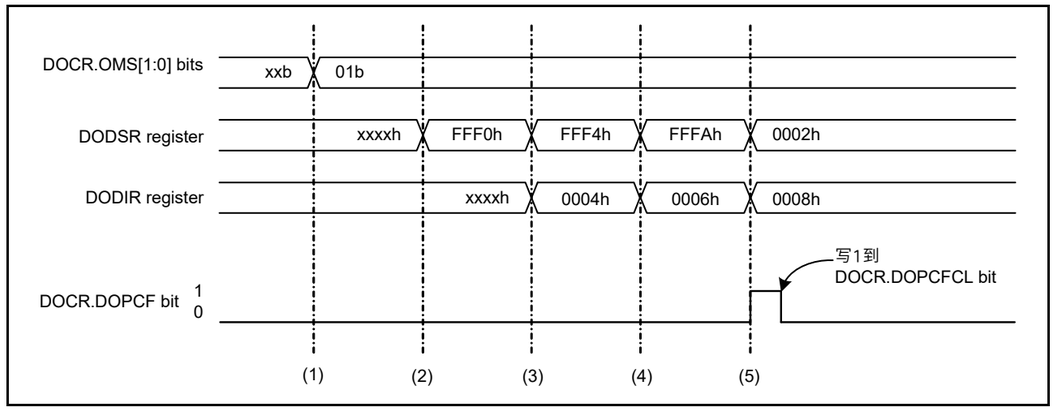


Figure 52.3 数据添加模式中的操作示例

52.3.3 数据减法模式

图52.4显示了DOC在数据减法模式操作中涉及的步骤示例：

1. 将10b写入DOCR.OMS[1:0]位以选择数据减法模式。
2. 将DODSR寄存器中的16位数据设置为初始值。
3. 将要减去的16位数据写入DODIR。操作结果存储在DODSR中。
4. 继续写入16位数据，直到所有减法数据都写入DODIR。
5. 如果运算结果小于0000h，则DOCR.DOPCF标志设置为1。

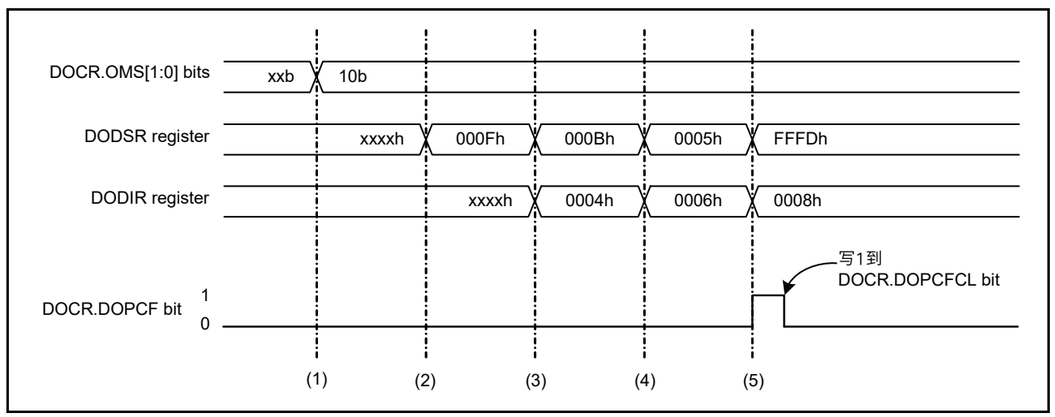


Figure 52.4 数据减法模式下的操作示例

52.4 Interrupt Request and Output to the Event Link Controller (ELC)

The DOC outputs an event signal for the ELC under the following conditions:

- The compared values either match or mismatch
- The data addition result is greater than FFFFh
- The data subtraction result is less than 0000h.

This signal can be used to initiate operations by other modules selected in advance and also can be used as an interrupt request. When an event signal is generated, the Data Operation Circuit Flag (DOCR.DOPCF) sets to 1.

52.5 Usage Notes

52.5.1 Settings for the Module-Stop Function

DOC operation can be disabled or enabled using Module Stop Control Register C (MSTPCRC). The DOC is initially stopped after reset. Releasing the module-stop state enables access to the registers. For details, see section 11, Low Power Modes.

52.4 中断请求和输出到事件链接控制器(ELC)

DOC在以下条件下为ELC输出事件信号：

- 比较的值匹配或不匹配
- 数据相加结果大于FFFFh
- 数据减法结果小于0000h。

该信号可用于启动其他预先选择的模块的操作，也可用作中断请求。生成事件信号时，数据操作电路标志(DOCR.DOPCF)设置为1。

52.5 使用说明

52.5.1 模块停止功能的设置

可以使用模块停止控制寄存器C(MSTPCRC)禁用或启用DOC操作。DOC在复位后最初停止。释放模块停止状态可以访问寄存器。有关详细信息，请参阅第11节，低功耗模式。

53. SRAM

53.1 Overview

The MCU provides on-chip high-speed SRAM modules with either parity-bit checking or ECC (Error Correction Code). The area of the first 32 KB of SRAM0 is subject to ECC. Parity check is performed on other areas. Table 53.1 lists the SRAM specifications.

Table 53.1 SRAM specifications

Parameter	Specifications without ECC	Specifications with ECC	SRAMHS specifications
SRAM capacity	SRAM0: 224 KB SRAM1: 256 KB	SRAM0 (ECC area): 32 KB	SRAMHS: 128 KB
SRAM addresses*2	SRAM0: 2000 8000h to 2003 FFFFh SRAM1: 2004 0000h to 2007 FFFFh	SRAM0 (ECC area): 2000 0000h to 2000 7FFFh	SRAMHS: 1FFE 0000h to 1FFF FFFFh
Access*1	Wait states are inserted into the read cycle by default. If the ICLK frequency is faster than 60 (up to 120) MHz, a wait state is required. If the ICLK frequency is 60 MHz or less, a wait state is not required. For details, see section 53.4, Usage Notes.	Wait states are inserted into the read cycle by default. If the ICLK frequency is faster than 60 (up to 120) MHz, wait state is required. If the ICLK frequency is 60 MHz or less, a wait state is not required. For details, see section 53.4, Usage Notes.	Access to the SRAMHS is always no wait state.
Data retention	Not available in Deep Software Standby mode		
Module-stop function	Module-stop state can be set to reduce power consumption		
Parity	Even-parity (data: 8 bits, parity: 1 bit)	No parity	Even-parity (data: 8 bits, parity: 1 bit)
Error checking	Even-parity error check	Detection up to 2-bit errors	Even-parity error check

Note 1. For details, see section 53.3.7, Access Cycles.

Note 2. The Cortex®-M4 processor supports Arm®v7 unaligned accesses. In this product, SRAMHS and SRAM0 are adjacent to each other and there is an access boundary between them. Therefore, when SRAMHS and SRAM0 are used as a continuous area of memory space, access that straddles the boundary must not be produced as this might lead to access of data other than what is intended. For details, see the *ARM® Cortex®-M4 Processor Technical Reference Manual*.

53.2 Register Descriptions

53.2.1 SRAM Parity Error Operation After Detection Register (PARIOAD)

Address(es): SRAM.PARIOAD 4000 2000h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	OAD
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	OAD	Operation after Detection	1: Reset 0: Non-maskable interrupt.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The PARIOAD register controls the operation on detection of a parity error. The SRAM Protection Register (SRAMPRCR) protects this register against writing. Set the SRAMPRCR bit in the SRAMPRCR register to the enabled setting before writing to this register. Do not write to the PARIOAD register while access to the SRAM is in progress.

OAD bit (Operation after Detection)

The OAD bit specifies generation of either a reset or non-maskable interrupt when a parity error is detected. The OAD

53. SRAM

53.1 Overview

MCU提供带有奇偶校验位检查或ECC（纠错码）的片上高速SRAM模块。
SRAM0的前32KB区域受ECC约束。在其他区域执行奇偶校验。表53.1列出了
SRAM specifications.

Table 53.1 SRAM specifications

Parameter	不带ECC的规格	带ECC的规格	SRAMHS specifications
SRAM capacity	SRAM0: 224 KB SRAM1: 256 KB	SRAM0 (ECC area): 32 KB	SRAMHS: 128 KB
SRAM addresses*2	SRAM0: 2000 8000h to 2003 FFFFh SRAM1: 2004 0000h to 2007 FFFFh	SRAM0 (ECC area): 2000 0000h to 2000 7FFFh	SRAMHS: 1FFE 0000h to 1FFF FFFFh
Access*1	默认情况下，等待状态被插入到读取周期中。如果ICLK频率高于60（最高120）MHz，则需要等待状态。如果ICLK频率为60MHz或更低，则不需要等待状态。有关详细信息，请参阅第53.4节，使用说明。	默认情况下，等待状态被插入到读取周期中。如果ICLK频率高于60（最高120）MHz，则需要等待状态。如果ICLK频率为60MHz或更低，则不需要等待状态。有关详细信息，请参阅第53.4节，使用说明。	访问SRAMHS始终是无等待状态。
数据保留	在深度软件待机模式下不可用		
Module-stop function	可设置模块停止状态以降低功耗		
Parity	Even-parity (data: 8 bits, parity: 1 bit)	无平价	Even-parity (data: 8 bits, parity: 1 bit)
错误检查	偶校验错误检查	检测多达2位错误	偶校验错误检查

Note 1. 有关详细信息，请参阅第53.3.7节，访问周期。

Note 2. Cortex®-M4处理器支持Arm®v7非对齐访问。在本产品中，SRAMHS和SRAM0是相邻的，它们之间存在访问边界。因此，当SRAMHS和SRAM0用作存储空间的连续区域时，不得产生跨越边界的访问，因为这可能会导致访问预期之外的数据。有关详细信息，请参阅ARM®Cortex®-M4处理器技术参考手册。

53.2 注册说明

53.2.1 检测寄存器后的SRAM奇偶校验错误操作(PARIOAD)

Address(es): SRAM.PARIOAD 4000 2000h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	OAD
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	OAD	检测后的操作	1：复位0：不可屏蔽中断 。	R/W
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

PARIOAD寄存器控制检测奇偶校验错误时的操作。SRAM保护寄存器(SRAMPRCR)保护该寄存器不被写入。在写入该寄存器之前，将SRAMPRCR寄存器中的SRAMPRCR位设置为启用设置。在访问SRAM的过程中不要写入PARIOAD寄存器。

OAD位（检测后操作）

OAD位指定在检测到奇偶校验错误时产生复位或不可屏蔽中断。OAD

bit in the PARIOAD register is shared by SRAM0 (without ECC), SRAM1, SRAMHS, and the Standby SRAM.

53.2.2 SRAM Protection Register (SRAMPRCR)

Address(es): SRAM.SRAMPRCR 4000 2004h

	b7	b6	b5	b4	b3	b2	b1	b0
	KW[6:0]							SRAMPRCR
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	SRAMPRCR	Register Write Control	0: Disable writes to protected registers 1: Enable writes to protected registers.	R/W
b7 to b1	KW[6:0]	Write Key Code	These bits enable or disable writing of the SRAMPRCR bit.	R/W

SRAMPRCR bit (Register Write Control)

The SRAMPRCR bit controls the write mode of the SRAMWTSC and PARIOAD registers. When the bit is set to 1, writing to the SRAMWTSC and PARIOAD registers is enabled. When you write to this bit, write 78h to the KW[6:0] bits simultaneously.

KW[6:0] bits (Write Key Code)

The KW[6:0] bits enable or disable writes to the SRAMPRCR bit. When you write to the SRAMPRCR bit, write 78h to the KW[6:0] bits simultaneously. When a value other than 78h is written to KW[6:0], the SRAMPRCR bit is not updated. The KW[6:0] bits are always read as 0.

53.2.3 SRAM Wait State Control Register (SRAMWTSC)

Address(es): SRAM.SRAMWTSC 4000 2008h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	SRAM1WTEN	SRAM0WTEN	SRAM0ERDWTEN	—
Value after reset:	0	0	0	0	1	1	1	0

Bit	Symbol	Bit name	Description	R/W
b0	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b1	SRAM0ERDWTEN	SRAM0 (ECC area) Read Wait Enable	1: Add wait state in read access cycle to SRAM0 (ECC area) 0: Do not add wait state in read access cycle to SRAM0 (ECC area).	R/W
b2	SRAM0WTEN	SRAM0 Wait Enable	1: Add wait state in read access cycle to SRAM0 0: Do not add wait state in read access cycle to SRAM0.	R/W
b3	SRAM1WTEN	SRAM1 Wait Enable	1: Add wait state in read access cycle to SRAM1 0: Do not add wait state in read access cycle to SRAM1.	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The SRAMWTSC register controls the wait states in the SRAM modules. The SRAM Protection Register (SRAMPRCR) protects this register against writing. Set the SRAMPRCR bit in the SRAMPRCR register to the enabled setting before writing to this register. Do not write to the SRAMWTSC register while access to the SRAM is in progress.

SRAM0ERDWTEN bit (SRAM0 (ECC area) Read Wait Enable)

The SRAM0ERDWTEN bit enables the wait cycle for reads from the ECC area in SRAM0. When this bit is set to 1, one

PARIOAD寄存器中的位由SRAM0（无ECC）、SRAM1、SRAMHS和备用SRAM共享。

53.2.2 SRAM保护寄存器(SRAMPRCR)

Address(es): SRAM.SRAMPRCR 4000 2004h

	b7	b6	b5	b4	b3	b2	b1	b0
	KW[6:0]							SRAMPRCR
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	SRAMPRCR	寄存器写控制	0：禁止写入受保护寄存器1：允许写入受保护寄存器。	R/W
b7 to b1	KW[6:0]	编写关键代码	这些位启用或禁用SRAMPRCR位的写入。	R/W

SRAMPRCR位（寄存器写控制）

SRAMPRCR位控制SRAMWTSC和PARIOAD寄存器的写模式。当该位设置为1时，允许写入SRAMWTSC和PARIOAD寄存器。写入该位时，同时将78h写入KW[6:0]位。

KW[6:0]位（写入密钥代码）

KW[6:0]位启用或禁用对SRAMPRCR位的写入。写入SRAMPRCR位时，同时将78h写入KW[6:0]位。当78h以外的值写入KW[6:0]时，SRAMPRCR位不会更新。KW[6:0]位总是读为0。

53.2.3 SRAM等待状态控制寄存器(SRAMWTSC)

Address(es): SRAM.SRAMWTSC 4000 2008h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	SRAM1WTEN	SRAM0WTEN	SRAM0ERDWTEN	—
重置后的值：	0	0	0	0	1	1	1	0

Bit	Symbol	位名称	Description	R/W
b0	—	Reserved	该位读取为0。写入值应为0。	R/W
b1	SRAM0ERDWTEN	SRAM0 (ECC area) Read 等待启用	1：将读访问周期中的等待状态添加到SRAM0（ECC区域）0：不将读访问周期中的等待状态添加到SRAM0（ECC区域）。	R/W
b2	SRAM0WTEN	SRAM0等待使能	1：将读访问周期中的等待状态添加到SRAM00：不将读访问周期中的等待状态添加到SRAM0。	R/W
b3	SRAM1WTEN	SRAM1等待使能	1：将读访问周期中的等待状态添加到SRAM10：不将读访问周期中的等待状态添加到SRAM1。	R/W
b7 to b4	—	Reserved	这些位被读取为0。写入值应为0。	R/W

SRAMWTSC寄存器控制SRAM模块中的等待状态。SRAM保护寄存器(SRAMPRCR)保护该寄存器不被写入。在写入该寄存器之前，将SRAMPRCR寄存器中的SRAMPRCR位设置为启用设置。访问SRAM时不要写入SRAMWTSC寄存器。

SRAM0ERDWTEN位（SRAM0（ECC区域）读取等待使能）

SRAM0ERDWTEN位使能从SRAM0中的ECC区域读取的等待周期。当该位设置为1时，一个

wait cycle is inserted into the read cycle of the ECC area in SRAM0. When the read access frequency is more than 60 MHz, this one-wait cycle setting is required.

SRAM0WTEN bit (SRAM0 Wait Enable)

The SRAM0WTEN bit enables the wait cycle for reads from SRAM0. When this bit is set to 1, one wait cycle is inserted into the read cycle of SRAM0. When the read access frequency is more than 60 MHz, this one-wait cycle setting is required.

SRAM1WTEN bit (SRAM1 Wait Enable)

The SRAM1WTEN bit enables the wait cycle for reads from SRAM1. When this bit is set to 1, one wait cycle is inserted into the read cycle of SRAM1. When the read access frequency is more than 60 MHz, this one-wait cycle setting is required.

53.2.4 ECC Operating Mode Control Register (ECCMODE)

Address(es): SRAM.ECCMODE 4000 20C0h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	ECCMOD[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	ECCMOD[1:0]	ECC Operating Mode Select	b1 b0 0 0: Disable ECC function 0 1: Setting prohibited 1 0: Enable ECC function without error checking 1 1: Enable ECC function with error checking.	R/W
b7 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The ECCMODE register specifies the ECC operating mode. The ECC Protection Register (ECCPRCR) protects this register against writing. Set the ECCPRCR bit in the ECCPRCR register to the enabled setting before writing to this register. Do not write to the ECCMODE register while access to the SRAM is in progress.

ECCMOD[1:0] bit (ECC Operating Mode Select)

The ECCMOD[1:0] bit sets the access mode for the ECC area in SRAM0.

53.2.5 ECC 2-Bit Error Status Register (ECC2STS)

Address(es): SRAM.ECC2STS 4000 20C1h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	ECC2ERR
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	ECC2ERR	ECC 2-Bit Error Status	0: No 2-bit ECC error occurred 1: 2-bit ECC error occurred.	R(/W)*1
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Only 0 can be written to clear the bit.

等待周期被插入到SRAM0中ECC区域的读取周期中。当读访问频率超过60MHz时，需要设置此一等待周期。

SRAM0WTEN位（SRAM0等待使能）

SRAM0WTEN位使能从SRAM0读取的等待周期。当该位设置为1时，插入一个等待周期

进入SRAM0的读周期。当读访问频率超过60MHz时，需要设置此一等待周期。

SRAM1WTEN位（SRAM1等待使能）

SRAM1WTEN位使能从SRAM1读取的等待周期。当该位设置为1时，会在SRAM1的读取周期中插入一个等待周期。当读访问频率超过60MHz时，需要设置此一等待周期。

53.2.4 ECC操作模式控制寄存器(ECCMODE)

Address(es): SRAM.ECCMODE 4000 20C0h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	ECCMOD[1:0]	
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b1, b0	ECCMOD[1:0]	ECC操作模式选择	b1b000：禁用ECC功能01：设置禁止10：启用ECC功能不进行错误检查11：启用ECC功能并进行错误检查。	R/W
b7 to b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W

ECCMODE寄存器指定ECC工作模式。ECC保护寄存器(ECCPRCR)保护该寄存器不被写入。在写入该寄存器之前，将ECPCRR寄存器中的ECPCRR位设置为使能设置。访问SRAM时不要写入ECCMODE寄存器。

ECCMOD[1:0]位（ECC操作模式选择）

ECCMOD[1:0]位设置SRAM0中ECC区域的访问模式。

53.2.5 ECC2位错误状态寄存器(ECC2STS)

Address(es): SRAM.ECC2STS 4000 20C1h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	ECC2ERR
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	ECC2ERR	ECC2位错误状态	0：未发生2位ECC错误1：发生2位ECC错误。	R(/W)*1
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 只能写入0以清除该位。

ECC2ERR bit (ECC 2-Bit Error Status)

The ECC2ERR bit indicates whether a 2-bit ECC error occurred in the ECC area of the SRAM. When ECC operations are enabled and error correction is selected, this bit sets to 1 if a 2-bit error is detected. The SRAM error signal is also asserted. Writing 0 to the ECC2ERR bit negates the SRAM error signal triggered by the 2-bit ECC error.

The SRAM error can be specified as a non-maskable interrupt or reset in the ECCOAD register. Do not access the ECC area in the SRAM while writing 0 to this register.

53.2.6 ECC 1-Bit Error Information Update Enable Register (ECC1STSEN)

Address(es): SRAM.ECC1STSEN 4000 20C2h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	E1STSEN
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	E1STSEN	ECC 1-Bit Error Information Update Enable	0: Disable updating of 1-bit ECC error information 1: Enable updating of 1-bit ECC error information.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The ECC1STSEN register enables or disables updating of the ECC 1-Bit Error Status Register (ECC1STS) in response to a 1-bit ECC error in the SRAM (ECC area). The ECC Protection Register (ECCPRCR) protects this register against writing. Set the ECCPRCR bit in the ECCPRCR register to the enabled setting before writing to this bit.

E1STSEN bit (ECC 1-Bit Error Information Update Enable)

The E1STSEN bit enables or disables updating of the SRAM (ECC area) 1-Bit Error Status Register (ECC1STS) in response to a 1-bit error in the ECC area of SRAM. The register also functions as an interrupt and reset mask.

53.2.7 ECC 1-Bit Error Status Register (ECC1STS)

Address(es): SRAM.ECC1STS 4000 20C3h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	ECC1ERR
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	ECC1ERR	ECC 1-Bit Error Status	0: No 1-bit ECC error occurred 1: 1-bit ECC error occurred.	R(/W)*1
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Only 0 can be written to clear the bit.

ECC1ERR bit (ECC 1-Bit Error Status)

The ECC1ERR bit indicates whether a 1-bit ECC error occurred in the ECC area of the SRAM. When ECC operations are enabled and error correction is selected, and updating of the 1-bit error information is enabled, this bit sets to 1 if a 1-bit error is detected. The SRAM error signal is also asserted. Writing 0 to the ECC1ERR bit negates the SRAM error signal triggered by the 1-bit ECC error.

The SRAM error can be specified as a non-maskable interrupt or reset in the ECCOAD register. Do not access the ECC area in the SRAM while writing 0 to this register.

ECC2ERR位（ECC2位错误状态）

ECC2ERR位指示SRAM的ECC区域是否发生2位ECC错误。当启用ECC操作并选择纠错时，如果检测到2位错误，则该位设置为1。SRAM错误信号也被置位。将0写入ECC2ERR位会否定由2位ECC错误触发的SRAM错误信号。

SRAM错误可以在ECCOAD寄存器中指定为不可屏蔽中断或复位。向该寄存器写入0时不要访问SRAM中的ECC区域。

53.2.6 ECC1位错误信息更新使能寄存器(ECC1STSEN)

Address(es): SRAM.ECC1STSEN 4000 20C2h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	E1STSEN
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	E1STSEN	ECC1位错误信息更新Enable	0：禁止更新1-bitECC错误信息1：允许更新1-bit ECC错误信息。	R/W
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

ECC1STSEN寄存器启用或禁用ECC1位错误状态寄存器(ECC1STS)的更新，以响应SRAM（ECC区域）中的1位ECC错误。ECC保护寄存器(ECCPRCR)保护该寄存器不被写入。在写入该位之前，将ECPCRR寄存器中的ECPCRR位设置为使能设置。

E1STSEN位（ECC1位错误信息更新使能）

E1STSEN位启用或禁用SRAM（ECC区域）1位错误状态寄存器(ECC1STS)的更新，以响应SRAM的ECC区域中的1位错误。该寄存器还用作中断和复位掩码。

53.2.7 ECC1位错误状态寄存器(ECC1STS)

Address(es): SRAM.ECC1STS 4000 20C3h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	ECC1ERR
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	ECC1ERR	ECC1位错误状态	0：未发生1位ECC错误1：发生1位ECC错误。	R(/W)*1
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 只能写入0以清除该位。

ECC1ERR位（ECC1位错误状态）

ECC1ERR位指示SRAM的ECC区域是否发生1位ECC错误。当启用ECC操作并选择纠错并启用1位错误信息更新时，如果检测到1位错误，则该位设置为1。SRAM错误信号也被置位。将0写入ECC1ERR位会否定由1位ECC错误触发的SRAM错误信号。

SRAM错误可以在ECCOAD寄存器中指定为不可屏蔽中断或复位。向该寄存器写入0时不要访问SRAM中的ECC区域。

53.2.8 ECC Protection Register (ECCPRCR)

Address(es): SRAM.ECCPRCR 4000 20C4h

	b7	b6	b5	b4	b3	b2	b1	b0
	KW[6:0]							ECCPRCR
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	ECCPRCR	Registers Write Control	0: Disable writes to protected registers 1: Enable writes to protected registers.	R/W
b7 to b1	KW[6:0]	Write Key Code	These bits enable or disable writes to the ECCPRCR bit.	R/W

ECCPRCR bit (Registers Write Control)

The ECCPRCR bit controls the write mode of the ECCMODE, ECC1STSEN, and ECCOAD registers. When the bit is set to 1, writing to the ECCMODE, ECC1STSEN, and ECCOAD registers is enabled. When you write to this bit, write 78h to the KW[6:0] simultaneously.

KW[6:0] bits (Write Key Code)

The KW[6:0] bits enable or disable writes to the ECCPRCR bit. When you write to the ECCPRCR bit, write 78h to the KW[6:0] bits simultaneously. When a value other than 78h is written to KW[6:0], the ECCPRCR bit is not updated. The KW[6:0] bits are always read as 0.

53.2.9 ECC Test Control Register (ECCETST)

Address(es): SRAM.ECCETST 4000 20D4h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	TSTBYP
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit Name	Description	R/W
b0	TSTBYP	ECC Bypass Select	0: ECC bypass disabled 1: ECC bypass enabled.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The ECC Protection Register (ECCPRCR2) protects this register against writing. Change the ECCPRCR2 bit in the ECCPRCR2 register to the enabled setting before writing to this bit. Do not write to the ECCETST register while access to SRAM is in progress.

TSTBYP bit (ECC Bypass Select)

The TSTBYP bit enables direct access to the ECC code by bypassing ECC function. The ECC bypass function is used with the ECCMOD[1:0] bits in the ECCMODE register to 00b. Access the same address with 32-bit access size as the data that is checked by ECC. The lower 7 bits of 32-bit write data can be written as an ECC code when the ECC bypass is enabled. The higher 25 bits in the write data are then ignored. The lower 7 bits of the 32-bit read data can be used as ECC code. The higher 25 bits in the read data are unknown.

Note: For details of ECC test, see section 53.3.4, ECC Decoder Testing.

53.2.8 ECC保护寄存器(ECPCRR)

Address(es): SRAM.ECCPRCR 4000 20C4h

	b7	b6	b5	b4	b3	b2	b1	b0
	KW[6:0]							ECCPRCR
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	ECCPRCR	寄存器写控制	0：禁止写入受保护寄存器1：允许写入受保护寄存器。	R/W
b7 to b1	KW[6:0]	编写关键代码	这些位启用或禁用写入ECCPRCR bit.	R/W

ECPCRR位（寄存器写控制）

ECPCRR位控制ECCMODE、ECC1STSEN和ECCOAD寄存器的写模式。当该位设置为1时，允许写入ECCMODE、ECC1STSEN和ECCOAD寄存器。写入该位时，同时将78h写入KW[6:0]。

KW[6:0]位（写入密钥代码）

KW[6:0]位启用或禁用对ECPCRR位的写入。写入ECPCRR位时，同时将78h写入KW[6:0]位。当向KW[6:0]写入78h以外的值时，不会更新ECPCRR位。这
KW[6:0]位总是读为0。

53.2.9 ECC测试控制寄存器(ECCETST)

Address(es): SRAM.ECCETST 4000 20D4h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	TSTBYP
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	TSTBYP	ECC旁路选择	0：禁用ECC旁路1：启用ECC旁路。	R/W
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

ECC保护寄存器(ECCPRCR2)保护该寄存器不被写入。改变ECPCRR2位
在写入该位之前，将ECPCRR2寄存器设置为使能设置。访问SRAM时不要写入ECCETST寄存器。

TSTBYP位（ECC旁路选择）

TSTBYP位允许通过绕过ECC功能直接访问ECC代码。ECC旁路功能与ECCMODE寄存器中的ECCMOD[1:0]位为00b一起使用。以32位访问大小访问与ECC检查的数据相同的地址。当ECC旁路使能时，32位写数据的低7位可以写为ECC代码。然后忽略写入数据中的高25位。32位读取数据的低7位可用作ECC码。读取数据中的高25位是未知的。

Note: 有关ECC测试的详细信息，请参阅第53.3.4节，ECC解码器测试。

53.2.10 SRAM ECC Error Operation After Detection Register (ECCOAD)

Address(es): SRAM.ECCOAD 4000 20D8h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	OAD
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	OAD	Operation after Detection	1: Reset 0: Non-maskable interrupt.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

The ECCOAD register controls the operation on detection of a ECC error. The ECC Protection Register (ECCPRCR) protects this register against writing. Set the ECCPRCR bit in the ECCPRCR register to the enabled setting before writing to this register. Do not write to the ECCOAD register while access to the SRAM is in progress.

OAD bit (Operation after Detection)

The OAD bit specifies generation of either a reset or a non-maskable interrupt when a ECC error is detected. The OAD bit in the ECCOAD register is used for the SRAM (ECC area).

53.3 Operation

53.3.1 Low-Power Functions

Power consumption can be reduced by setting Module Stop Control Register A (MSTPCRA) to stop supply of the clock signal to the SRAM. The control bits are as follows for each module:

- Setting both the MSTPA0 and MSTPA6 bits in the MSTPCRA to 1 stops supply of the clock signal to SRAM0*1
- Setting the MSTPA1 bit in the MSTPCRA to 1 stops supply of the clock signal to SRAM1
- Setting the MSTPA5 bit in MSTPCRA to 1 stops supply of the clock signal to the SRAMHS
- Setting the MSTPA7 bit in the MSTPCRA to 1 stops supply of the clock signal to the Standby SRAM.

Stopping the clock signal supply places the SRAM in the module-stop state. The SRAM operates after a reset.

The SRAM is not accessible in the module-stop state. Do not transition to the module-stop state while access to the SRAM is in progress. Access to the SRAM in the module-stop state is prohibited. If access is attempted, correct operation is not guaranteed.

For details on the MSTPCRA register, see section 11, Low Power Modes.

Note 1. The settings in the MSTPA0 and MSTPA6 bits in the MSTPCRA register must be the same.

53.3.2 ECC Function

Enabling and disabling of ECC error correction can be selected through ECCMODE register setting. In the initial state, ECC error correction is disabled. The ECC check type is SEC-DED (Single-Error Correction and Double-Error Detection Code).

When ECC function is enabled, 7-bit check bits are appended to 32-bit data for writing. For reading, 39-bit (data: 32 bits, check bits: 7 bits) data is read out from the SRAM (ECC area).

When ECC function is enabled and error checking is enable, error correction is done if a 1-bit error occurs and the ECC1ERR bit in the ECC1STS register is set to 1 if the E1STSEN bit in the ECC1STSEN register is 1; if a 2-bit error occurs, error detection is done and the ECC2ERR bit in the ECC2STS register is set to 1, though error correction is not performed.

When ECC function is enabled and the error checking is disable, error correction is done if a 1-bit error occurs but

53.2.10 SRAMECC检测后错误操作寄存器(ECCOAD)

Address(es): SRAM.ECCOAD 4000 20D8h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	OAD
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	OAD	检测后的操作	1：复位0：不可屏蔽中断 。	R/W
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

ECCOAD寄存器控制检测到ECC错误时的操作。ECC保护寄存器(ECCPRCR)保护该寄存器不被写入。在写入该寄存器之前，将ECPCRR寄存器中的ECPCRR位设置为使能设置。访问SRAM时不要写入ECCOAD寄存器。

OAD位（检测后操作）

OAD位指定在检测到ECC错误时生成复位或不可屏蔽中断。ECCOAD寄存器中的OAD位用于SRAM（ECC区域）。

53.3 Operation

53.3.1 Low-Power Functions

通过设置模块停止控制寄存器A(MSTPCRA)停止向SRAM提供时钟信号，可以降低功耗。每个模块的控制位如下：

- 将MSTPCRA中的MSTPA0和MSTPA6位都设置为1会停止向SRAM0提供时钟信号*1
- 将MSPCRA中的MSTPA1位设置为1会停止向SRAM1提供时钟信号
- 将MSPCRA中的MSTPA5位设置为1会停止向SRAMHS提供时钟信号
- 将MSPCRA中的MSTPA7位设置为1会停止向待机SRAM提供时钟信号。

停止时钟信号供应会将SRAM置于模块停止状态。SRAM在复位后运行。

SRAM在模块停止状态下不可访问。不要转换到模块停止状态，同时访问
SRAM正在进行中。禁止在模块停止状态下访问SRAM。如果尝试访问，则无法保证正确操作。

有关MSTPCRA寄存器的详细信息，请参见第11节，低功耗模式。

注1.MSTPCRA寄存器中的MSTPA0和MSTPA6位的设置必须相同。

53.3.2 ECC Function

可以通过ECCMODE寄存器设置来选择ECC纠错的启用和禁用。在初始状态下，
ECC纠错已禁用。ECC校验类型是SEC-DED（单纠错和双错误
Detection Code).

当ECC功能使能时，7位校验位被附加到32位数据中进行写入。读取时，从SRAM（ECC区域）中读取39位（数据：32位，校验位：7位）数据。

当启用ECC功能并启用错误检查时，如果发生1位错误并且
如果ECC1STSEN寄存器中的E1STSEN位为1，则ECC1STS寄存器中的ECC1ERR位设置为1；如果发生2位错误，则进行错误检测并将ECC2STS寄存器中的ECC2ERR位设置为1，但不执行错误纠正。

当启用ECC功能且禁用错误检查时，如果发生1位错误，则进行错误纠正，但

ECC1ERR bit in the ECC1STS register is not updated although E1STSEN bit in the ECC1STSEN register is 1; if a 2-bit error occurs, this error is detected but the ECC2ERR bit in the ECC2STS register is not updated, and error correction is not performed.

When ECC function is disable, neither error correction nor error detection is done although 1-bit or 2-bit error occur. So ECC1ERR bit and ECC2ERR bit are not updated.

There is no way to confirm the location where the error was found. Therefore, when after the occurrence of an error, update all the data.

When updating all the data after the occurrence of an error, the only support of 32-bit data writing.

Because the SRAM data is undefined after power on and release from deep software standby mode, accessing the SRAM when ECC function is enabled and error checking is selected causes an ECC error to occur. Therefore, before using ECC function, initial writing with 32-bit data size to the area to be used in the SRAM should be done.

When a read access is executed in a row after a write access, read access is executed with priority. Therefore, during initialization, please do not perform the read access in a row after the write access.

53.3.3 ECC Error Generation

When ECC function is enabled and error checking is applied to the SRAM (ECC area), an ECC error occurs when either the ECC2ERR bit in the ECC2STS register or the ECC1ERR bit in the ECC1STS register becomes 1 to indicate that ECC checking revealed a 2-bit error or a 1-bit error, respectively.

An ECC error is output with a pulse width of ICLK. When the ECC 1-bit error is to be masked, set the ECC1STSEN.E1STSEN bit to 0 to disable updating of the ECC1ERR bit. An ECC error will not be generated while ECC function is disabled or when ECC function is enabled but error checking is not selected.

ECC error can choose non maskable interrupt or reset by ECCOAD register. When set 1 in the OAD bit of the ECCOAD register, ECC error is output to the reset function. When set 0 in the OAD bit of the ECCOAD register, ECC Error interrupt is output to the ICU as non-maskable interrupt.

53.3.4 ECC Decoder Testing

Figure 53.1 shows the ECC decoder testing.

尽管ECC1STSEN寄存器中的E1STSEN位为1，但ECC1STS寄存器中的ECC1ERR位不更新；如果发生2位错误，则会检测到该错误，但不会更新ECC2STS寄存器中的ECC2ERR位，也不会执行错误纠正。

当ECC功能被禁用时，即使发生1位或2位错误，也不会进行纠错或错误检测。所以ECC1ERR位和ECC2ERR位不更新。

无法确认发现错误的位置。因此，当发生错误后，更新所有数据。

发生错误后更新所有数据时，仅支持32位数据写入。

由于SRAM数据在上电并从深度软件待机模式释放后未定义，因此在启用ECC功能并选择错误检查时访问SRAM会导致发生ECC错误。因此，在使用ECC功能之前，应先将32位数据大小写入SRAM中要使用的区域。

在写访问之后连续执行读访问时，优先执行读访问。因此，在初始化过程中，请不要在写访问之后连续进行读访问。

53.3.3 ECC错误生成

当启用ECC功能并对SRAM（ECC区域）应用错误检查时，当ECC2STS寄存器中的ECC2ERR位或ECC1STS寄存器中的ECC1ERR位变为1时发生ECC错误，表示ECC检查显示2-位错误或1位错误，分别。

以ICLK脉冲宽度输出ECC错误。当要屏蔽ECC1位错误时，设置ECC1STSEN.E1STSEN位为0以禁用ECC1ERR位的更新。不会产生ECC错误，同时ECC功能被禁用或ECC功能启用但未选择错误检查时。

ECC错误可以选择不可屏蔽中断或通过ECCOAD寄存器复位。当ECCOAD寄存器的OAD位设置为1时，ECC错误输出到复位功能。当ECCOAD寄存器的OAD位设置为0时，ECC错误中断作为不可屏蔽中断输出到ICU。

53.3.4 ECC解码器测试

图53.1显示了ECC解码器测试。

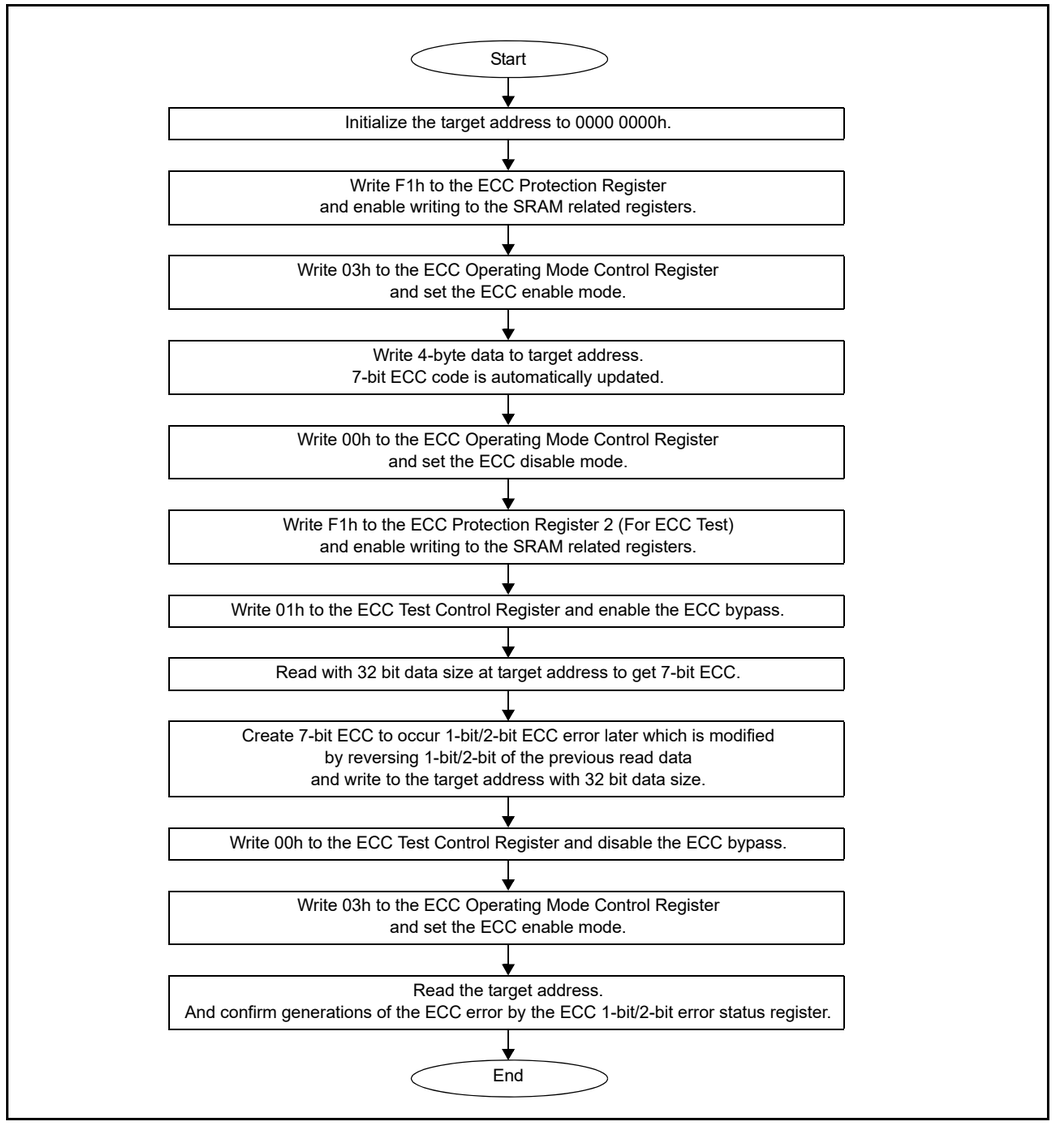


Figure 53.1 ECC Decoder Testing

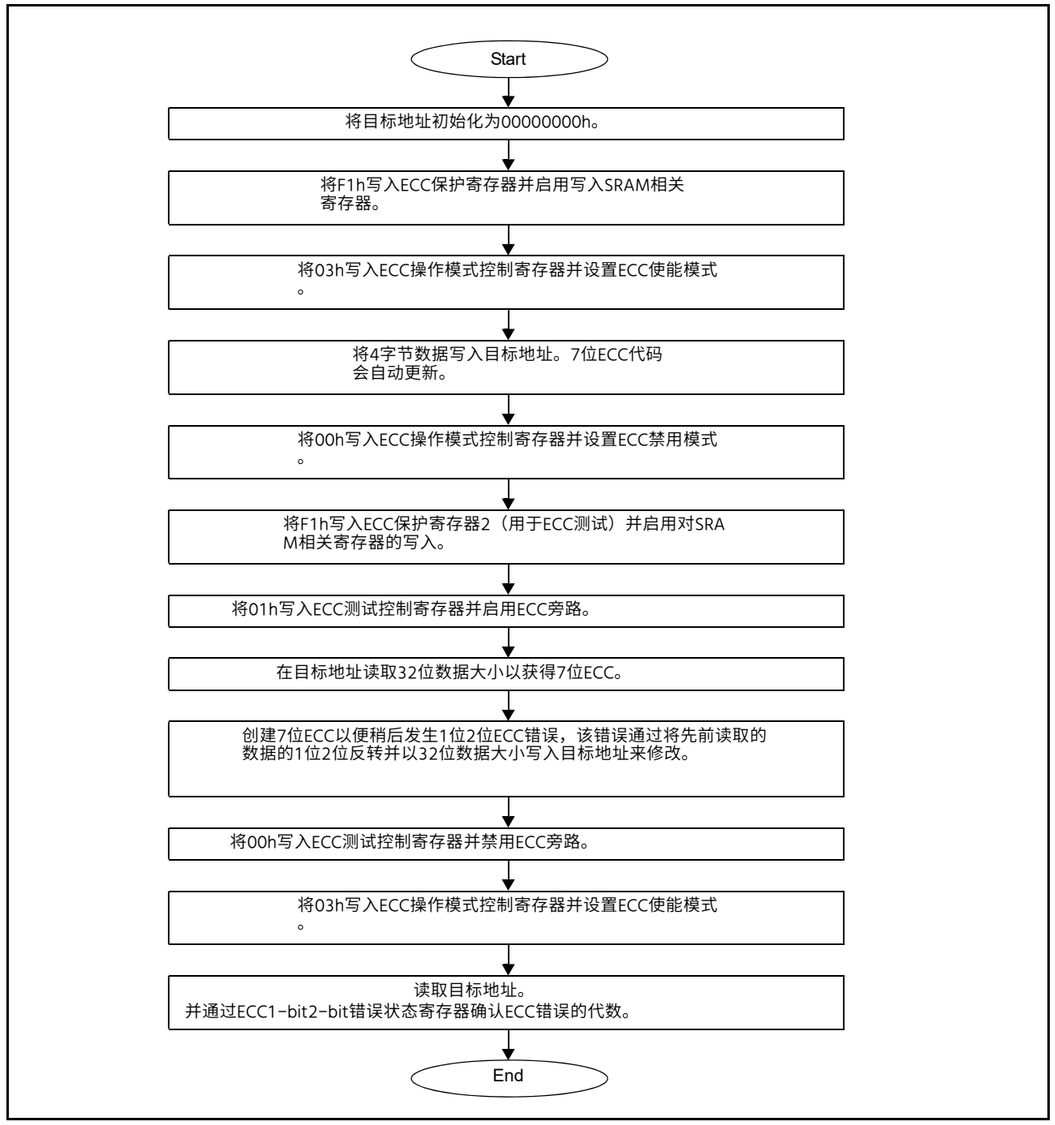


Figure 53.1 ECC解码器测试

53.3.5 Parity Calculation Function

The IEC60730 standard requires the checking of SRAM data. A parity bit is therefore added to every 8-bit data unit in the SRAM modules that have 32-bit data width. With this SRAM parity error detection function, the parity bit is appended when data is written, and the parity is checked when the data is read. When a parity error occurs, a parity-error notification is generated. This function can also be used to trigger a reset. The specification for SRAM0 without ECC, SRAM1, SRAMHS, and Standby SRAM is even parity.

Parity error notification can be specified as either a non-maskable interrupt or reset in the PARIOAD register. When the OAD bit in the PARIOAD register is set to 1, a parity error is output to the reset function. When the OAD bit in the PARIOAD register is set to 0, a parity error is output to the ICU as a non-maskable interrupt.

Parity errors often occur because of noise. To confirm whether the cause is noise or corruption, follow the parity check flows shown in Figure 53.2 and Figure 53.3.

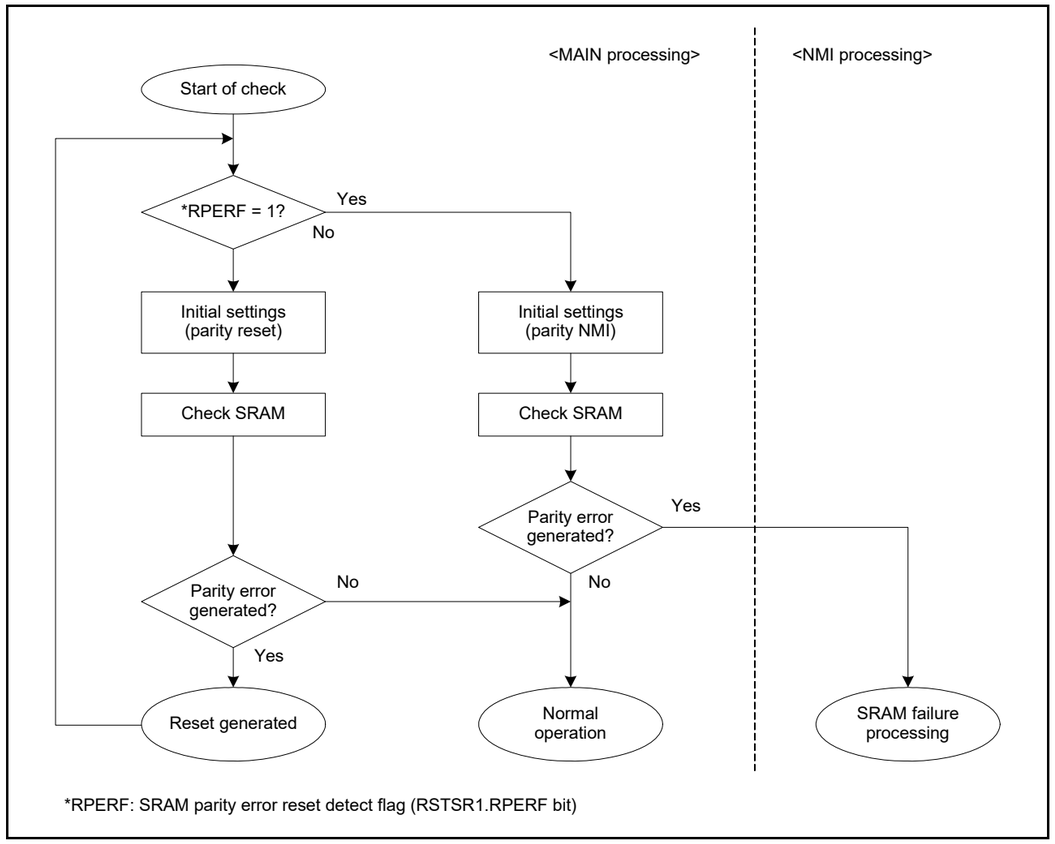


Figure 53.2 Flow of SRAM parity check when SRAM parity reset is enabled

53.3.5 奇偶校验计算功能

IEC60730标准要求检查SRAM数据。因此，具有32位数据宽度的SRAM模块中的每个8位数据单元都会添加一个奇偶校验位。使用该SRAM奇偶校验错误检测功能，写入数据时附加奇偶校验位，读取数据时检查奇偶校验位。当发生奇偶校验错误时，会生成奇偶校验错误通知。此功能也可用于触发复位。无ECC的SRAM0、SRAM1、SRAMHS和备用SRAM的规格是偶校验。

奇偶校验错误通知可以在PARIOAD寄存器中指定为不可屏蔽中断或复位。当。。。的时候PARIOAD寄存器中的OAD位设置为1，奇偶校验错误输出到复位功能。当OAD位在PARIOAD寄存器设置为0，奇偶校验错误作为不可屏蔽中断输出到ICU。

奇偶校验错误经常因噪声而发生。要确认原因是噪声还是损坏，请按照图53.2和图53.3所示的奇偶校验流程进行操作。

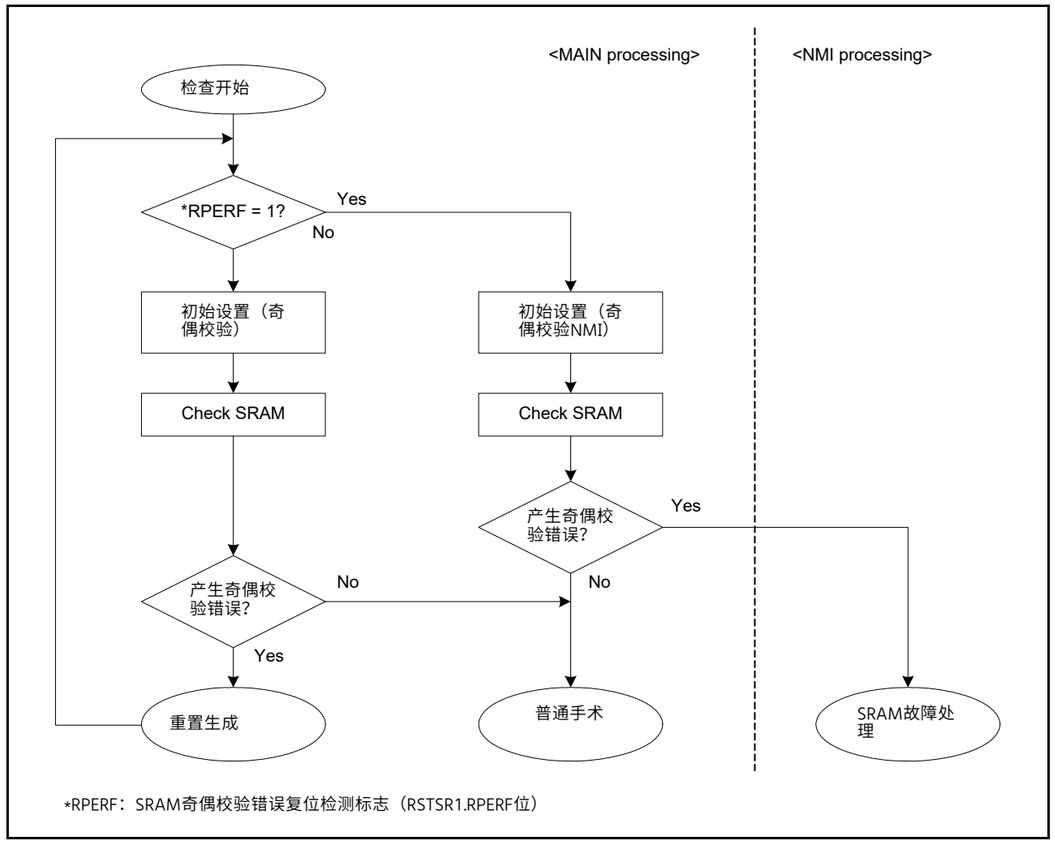


Figure 53.2 启用SRAM奇偶校验复位时的SRAM奇偶校验流程

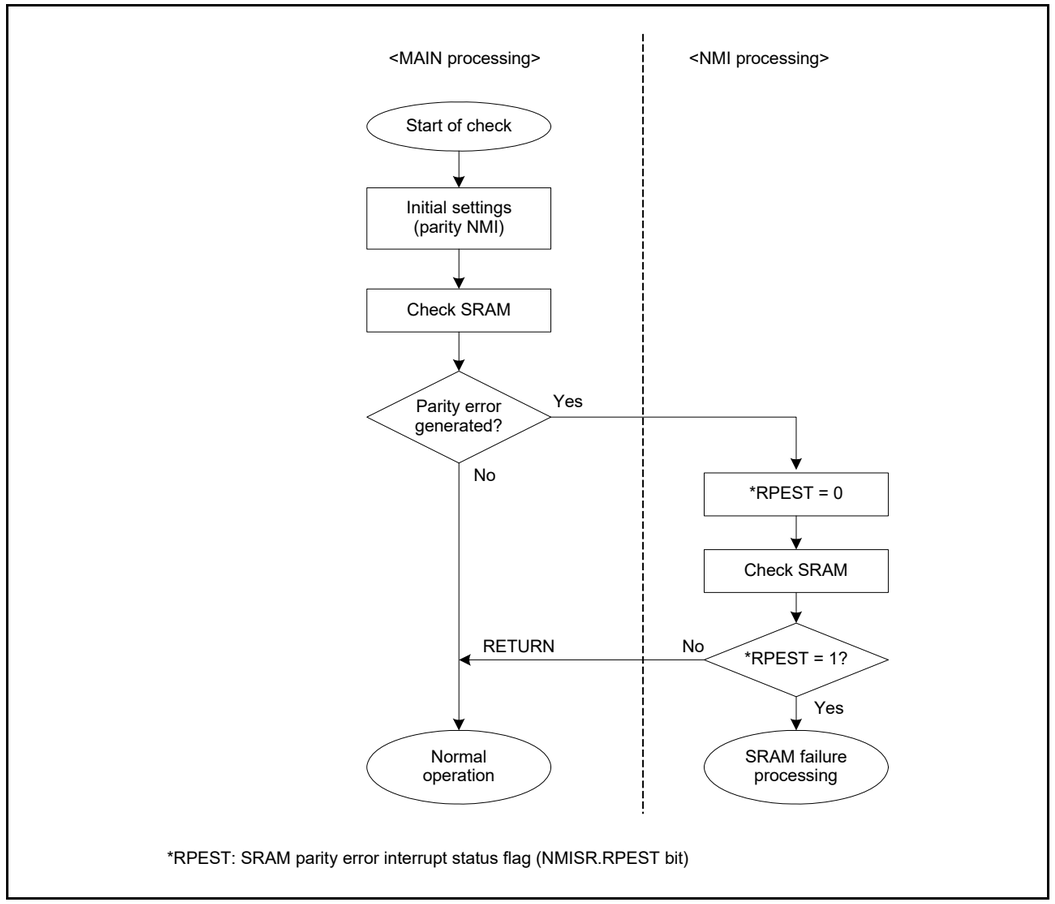


Figure 53.3 Flow of SRAM parity check when SRAM parity interrupt is enabled

53.3.6 SRAM Error Sources

The SRAM error sources are ECC errors and parity errors. ECC errors can be specified as non-maskable interrupts or resets in the OAD bit in the ECCOAD register, and parity errors can be specified as non-maskable interrupts or resets in the PARIOAD register.

Table 53.2 SRAM error sources

Interrupt source	DTC activation	DMAC activation
ECC error (SRAM0 area with ECC)	Not possible	Not possible
Parity error (SRAM0 area without ECC, SRAM1, SRAMHS	Not possible	Not possible

53.3.7 Access Cycles

Table 53.3 SRAMHS (parity area 1FFE 0000h to 1FFF FFFFh)

Read (cycles)		Write (cycles)	
Word access	Halfword/byte access	Word access	Halfword/byte access
2		2	

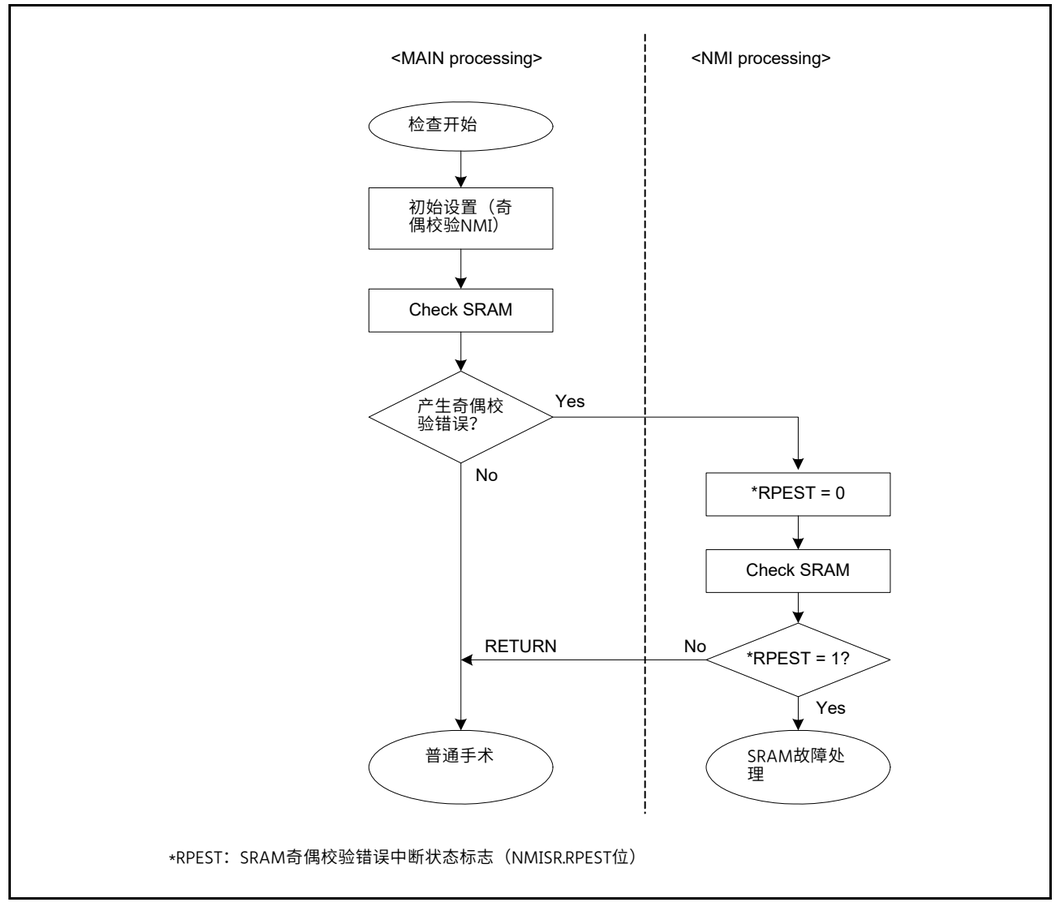


Figure 53.3 启用SRAM奇偶校验中断时的SRAM奇偶校验流程

53.3.6 SRAM错误源

SRAM错误源是ECC错误和奇偶校验错误。ECC错误可在ECCOAD寄存器的OAD位中指定为不可屏蔽中断或复位，奇偶校验错误可在PARIOAD寄存器中指定为不可屏蔽中断或复位。

Table 53.2 SRAM错误源

中断源	DTC activation	DMAC activation
ECC错误（带ECC的SRAM0区域）	不可能	不可能
奇偶校验错误（SRAM0区域无ECC、SRAM1、SRAMHS	不可能	不可能

53.3.7 访问周期

Table 53.3 SRAMHS（奇偶校验区1FFE0000h至1FFFFFFFh）

Read (cycles)		Write (cycles)	
字访问	Halfword/byte access	字访问	Halfword/byte access
2		2	

Table 53.4 SRAM0 (ECC area 2000 0000h to 2000 7FFFh)

Bit settings		Read (cycles)		Write (cycles)	
		Word access	Halfword or byte access	Word access	Halfword or byte access
ECC Off ECCMOD[1] = 0	SRAM0ERDWTEN = 0	2		2	
	SRAM0ERDWTEN = 1	3		2	
ECC On ECCMOD[1] = 1	SRAM0ERDWTEN = 0	2		2	4
	SRAM0ERDWTEN = 1	3		2	4

Table 53.5 SRAM0 (parity area 2000 8000h to 2003 FFFFh)

Bit settings	Read (cycles)		Write (cycles)	
	Word access	Halfword or byte access	Word access	Halfword or byte access
SRAM0WTEN = 0	2		2	
SRAM0WTEN = 1	3		2	

Table 53.6 SRAM1 (parity area 2004 0000h to 2007 FFFFh)

Bit settings	Read (cycles)		Write (cycles)	
	Word access	Halfword or byte access	Word access	Halfword or byte access
SRAM1WTEN = 0	2		2	
SRAM1WTEN = 1	3		2	

53.4 Usage Notes

53.4.1 Wait State Insertion

Set the number of SRAM wait cycles in the SRAMWTSC register based on the following:

- SRAM0, SRAM1
  1 wait: 60 MHz < ICLK ≤ 120 MHz
  No wait: ICLK ≤ 60 MHz

53.4.2 Instruction Fetch from the SRAM Area

When using SRAM0, SRAM1, or the SRAMHS to operate a program, initialize the SRAM area so the CPU can correctly prefetch data. If the CPU prefetches data from an SRAM area that is not initialized, an ECC error or a parity error might occur. Initialize the additional 12-byte area from the end address of the program with the 4-byte boundary. Renesas recommends using the NOP instruction for data initialization.

53.4.3 Store Buffer of SRAM

For fast access between SRAM and CPU, a store buffer is used. When a load instruction is executed from the same address after a store instruction to SRAM, the load instruction might read out data from the buffer instead of data from the SRAM. To read data on the SRAM correctly, use either of the following procedures:

- After writing to the SRAM (address = A), use the NOP instruction, then read the SRAM (address = A)
- After writing to the SRAM (address = A), read data from area other than SRAM (address = A), then read the SRAM (address = A).

Table 53.4 SRAM0（ECC区域20000000h至20007FFFh）

位设置		Read (cycles)		Write (cycles)	
		字访问	半字或字节访问	字访问	半字或字节访问
ECC Off ECCMOD[1] = 0	SRAM0ERDWTEN = 0	2		2	
	SRAM0ERDWTEN = 1	3		2	
ECC On ECCMOD[1] = 1	SRAM0ERDWTEN = 0	2		2	4
	SRAM0ERDWTEN = 1	3		2	4

Table 53.5 SRAM0（奇偶校验区20008000h到2003FFFFh）

位设置	Read (cycles)		Write (cycles)	
	字访问	半字或字节访问	字访问	半字或字节访问
SRAM0WTEN = 0	2		2	
SRAM0WTEN = 1	3		2	

Table 53.6 SRAM1（奇偶校验区20040000h到2007FFFFh）

位设置	Read (cycles)		Write (cycles)	
	字访问	半字或字节访问	字访问	半字或字节访问
SRAM1WTEN = 0	2		2	
SRAM1WTEN = 1	3		2	

53.4 使用说明

53.4.1 等待状态插入

根据以下内容在SRAMWTSC寄存器中设置SRAM等待周期数：

- SRAM0, SRAM1
  1 wait: 60 MHz < ICLK ≤ 120 MHz
  No wait: ICLK ≤ 60 MHz

53.4.2 从SRAM区域取指令

当使用SRAM0、SRAM1或SRAMHS操作程序时，初始化SRAM区域，以便CPU可以正确预取数据。如果CPU从未初始化的SRAM区域预取数据，则可能会发生ECC错误或奇偶校验错误。用4字节边界从程序的结束地址初始化额外的12字节区域。瑞萨推荐使用NOP指令进行数据初始化。

53.4.3 SRAM的存储缓冲区

对于SRAM和CPU之间的快速访问，使用了存储缓冲区。当在对SRAM执行存储指令之后从同一地址执行加载指令时，加载指令可能会从缓冲区中读取数据，而不是从SRAM中读取数据。要正确读取SRAM上的数据，请使用以下任一过程：

- 写入SRAM（地址=A）后，使用NOP指令，然后读取SRAM（地址=A）
- 写入SRAM（地址=A）后，从SRAM以外的区域（地址=A）读取数据，然后读取SRAM（地址=A）。

54. Standby SRAM

54.1 Overview

An on-chip SRAM is provided to retain data in Deep Software Standby mode. Table 54.1 lists the Standby SRAM specifications.

Table 54.1 Standby SRAM specifications

Parameter	Specifications
SRAM capacity	8 KB
SRAM address	200F E000h to 200F FFFFh
Access	The number of access depends on the frequency between ICLK and PCLKB. See section 54.2.4, Access Cycle for details.
Data retention	Data can be retained in Deep Software Standby mode
Parity	Even parity (data: 8 bits, parity: 1 bit)
Module-stop function	Module-stop state can be set to reduce power consumption

54.2 Operation

54.2.1 Data Retention

The power supply to the Standby SRAM in Deep Software Standby mode is enabled by the DPSBYCR.DEEPCUT[1:0] bits. If the DPSBYCR.DEEPCUT[1:0] bits are set to 00b, data in the Standby SRAM is retained in Deep Software Standby mode. See section 11, Low Power Modes, for details on the DPSBYCR.DEEPCUT[1:0] bits.

54.2.2 Low-Power Function

Power consumption can be reduced by setting Module Stop Control Register A (MSTPCRA) to stop supply of the clock signal to the SRAM. Setting the MSTPA7 bit in MSTPCRA to 1 stops supply of the clock signal to the Standby SRAM. The Standby SRAM is then placed in the module-stop state by stopping supply of the clock signals. The Standby SRAM operates after a reset. The Standby SRAM is not accessible if it is in the module-stop state. Do not transition to the module-stop state while access to the Standby SRAM is in progress. For details on the MSTPCRA register, see section 11, Low Power Modes.

54.2.3 Parity Calculation Function

The parity calculation function for Standby SRAM is the same as for SRAM1 or SRAM0 without error correction code (ECC). The function of the OAD bit in the PARIOAD register and the flow of the SRAM parity check are shared by the Standby SRAM modules. For details, see section 53.3.5, Parity Calculation Function and section 53.3.6, SRAM Error Sources.

54.2.4 Access Cycle

Table 54.2 Standby SRAM access cycle

	Read (cycles)		Write (cycles)	
Frequency	Word access	Halfword/byte access	Word access	Halfword/byte access
Same Frequency ICLK = PCLKB	3 ICLK		2 ICLK	
Different Frequency ICLK > PCLKB	1 ICLK + 2 to 3 PCLKB		1 ICLK + 1 to 2 PCLKB	

54. Standby SRAM

54.1 Overview

提供片上SRAM以在深度软件待机模式下保留数据。表54.1列出了备用SRAM规格。

Table 54.1 备用SRAM规格

Parameter	Specifications
SRAM capacity	8 KB
SRAM address	200F E000h to 200F FFFFh
Access	访问次数取决于ICLK和PCLKB之间的频率。 有关详细信息，请参阅第54.2.4节，访问周期。
数据保留	数据可以在深度软件待机模式下保留
Parity	偶校验（数据：8位，奇偶校验：1位）
Module-stop function	可设置模块停止状态以降低功耗

54.2 Operation

54.2.1 数据保留

深度软件待机模式下的待机SRAM电源由DPSBYCR.DEEPCUT[1:0]位启用。如果DPSBYCR.DEEPCUT[1:0]位设置为00b，则待机SRAM中的数据将保留在深度软件待机模式中。有关DPSBYCR.DEEPCUT[1:0]位的详细信息，请参见第11节，低功耗模式。

54.2.2 Low-Power Function

通过设置模块停止控制寄存器A(MSTPCRA)停止向SRAM提供时钟信号，可以降低功耗。将MSPTCRA中的MSTPA7位设置为1会停止向待机SRAM提供时钟信号。然后通过停止提供时钟信号将待机SRAM置于模块停止状态。待机SRAM在复位后运行。如果处于模块停止状态，则无法访问备用SRAM。在访问备用SRAM的过程中不要转换到模块停止状态。有关MSTPCRA寄存器的详细信息，请参见第11节，低功耗模式。

54.2.3 奇偶校验计算功能

StandbySRAM的奇偶校验计算功能与无纠错码(ECC)的SRAM1或SRAM0相同。PARIOAD寄存器中OAD位的功能和SRAM奇偶校验流程由备用SRAM模块共享。有关详细信息，请参阅第53.3.5节，奇偶校验计算函数和第53.3.6节，SRAM错误

Sources.

54.2.4 访问周期

Table 54.2 待机SRAM访问周期

	Read (cycles)		Write (cycles)	
Frequency	字访问	Halfword/byte access	字访问	Halfword/byte access
同频 ICLK = PCLKB	3 ICLK		2 ICLK	
不同频率 ICLK > PCLKB	1 ICLK + 2 to 3 PCLKB		1 ICLK + 1 to 2 PCLKB	

54.3 Usage Notes

54.3.1 Instruction Fetch from the Standby SRAM area

When using Standby SRAM to operate a program, initialize the Standby SRAM area so that the CPU can correctly prefetch data. A parity error might occur if the CPU prefetches from an area that is not initialized. Initialize the additional 12-byte area from the end address of the program with the 4-byte boundary. Renesas recommends using the NOP instruction for data initialization.

54.3 使用说明

54.3.1 从备用SRAM区域取指令

使用StandbySRAM操作程序时，初始化StandbySRAM区域，以便CPU可以正确预取数据。如果CPU从未初始化的区域预取，则可能发生奇偶校验错误。用4字节边界从程序的结束地址初始化额外的12字节区域。瑞萨推荐使用NOP指令进行数据初始化。

55. Flash Memory

55.1 Overview

The MCU provides up to 2-MB code flash memory and 64-KB data flash memory. The Flash Control Unit (FCU) controls programming and erasure of the flash memory. The Flash Application Command Interface (FACI) controls the FCU in accordance with the specified FACI commands.

Table 55.1 lists the specifications of the code flash memory and data flash memory, and Figure 55.1 shows a block diagram of the related modules. Figure 55.2 shows the configuration of the code flash memory, and Figure 55.3 shows the configuration of the data flash memory.

Table 55.1 Specifications of the code flash memory and data flash memory

Parameter	Code flash memory specifications	Data flash memory specifications
Memory capacity	• Up to 2 MB	64 KB
Read cycle	• 80 MHz < ICLK frequency ≤ 120 MHz: Cache hit: 1 cycle Cache miss: 3 cycles • 40 MHz < ICLK frequency ≤ 80 MHz: Cache hit: 1 cycle Cache miss: 2 cycles • ICLK frequency ≤ 40 MHz: Cache hit: 1 cycle Cache miss: 1 cycle	A read operation takes seven cycles of FCLK in words or bytes (FCLK frequency is up to 60 MHz)
Value after erasure	FFh	Undefined
Programming/erasing methods	• Programming and erasing of code and data flash memory handled by FACI commands specified in the FACI command issuing area (407E 0000h) • Programming by dedicated flash-memory programmer transfer through a serial interface (serial programming) • Programming of flash memory by user program (self-programming)	
Security function	Protection against illicit tampering with or reading of data in flash memory	
Protection	Protection against erroneous overwriting of flash memory	
Background operations (BGOs)	• Code flash memory can be read during code flash memory programming*1 • Code flash memory can be read during data flash memory programming • Data flash memory can be read during code flash memory programming	
Units of programming and erasure	• 128-byte units for programming in user area • Block units for erasure in user area	• 4/8/16-byte units for programming in data area • 64/128/256-byte units for erasure in data area
Other functions	Interrupts can be accepted during self-programming	
	An expansion area of flash memory (option bytes) can be set in the initial MCU settings	
On-board programming (four types)	Programming in serial programming mode (SCI boot mode): • Asynchronous serial interface (SCI9) used • Transfer rate adjusted automatically Programming in serial programming mode (USB boot mode): • USBFS used • Dedicated hardware not required, so direct connection to PC is possible Programming in On-chip debug mode: • JTAG or SWD interface used • Dedicated hardware not required Programming by a routine for code and data flash memory programming within the user program: • Allows code and data flash memory programming without resetting the system	

Note 1. Constraints apply to the combinations of ranges in which writing can proceed. See Table 55.11.

55. 闪存

55.1 Overview

MCU提供高达2-MB的代码闪存和64-KB的数据闪存。闪存控制单元(FCU)控制闪存的编程和擦除。Flash应用命令接口(FACI)根据指定的FACI命令控制FCU。

表55.1列出了代码闪存和数据闪存的规格，图55.1给出了相关模块的框图。图55.2显示了代码闪存的配置，图55.3显示了数据闪存的配置。

Table 55.1 代码闪存和数据闪存的规格

Parameter	代码闪存规格	数据闪存规格
内存容量	高达2MB	64 KB
读周期	80MHz<ICLK频率≤120MHz：高速缓存命中：1个周期 缓存未命中：3个周期 40MHz<ICLK频率≤80MHz：缓存命中：1个周期 缓存未命中：2个周期 ICLK频率≤40MHz：缓存命中：1个周期 缓存未命中：1个周期	读取操作需要7个字或字节的FCLK周期（FCLK频率高达60MHz）
擦除后的值	FFh	Undefined
Programming/erasing methods	由FACI命令发出区域(407E0000h)中指定的FACI命令处理的代码和数据闪存的编程和擦除 通过串行接口传输的专用闪存编程器进行编程（串行编程） 通过用户程序对闪存进行编程（自编程）	
安全功能	防止非法篡改或读取闪存中的数据	
Protection	防止错误覆盖闪存	
后台操作(BGO)	代码闪存可以在代码闪存编程期间读取*1 代码闪存可以在数据闪存编程期间读取 数据闪存可以在代码闪存编程期间读取	
编程和擦除单元	128字节单元，用于用户区中的编程 块单元，用于用户区中的擦除	48个16字节单元，用于数据区中的编程 64128256字节单元，用于数据区中的擦除
其他功能	自编程期间可以接受中断	
	可在初始MCU设置中设置闪存的扩展区域（选项字节）	
On-board programming (four types)	在串行编程模式下编程（SCI引导模式）： 使用异步串行接口(SCI9) 自动调整传输速率在串行编程模式下编程（USB引导模式）： 使用USBFS 不需要专用硬件，因此可以直接连接到PC可以在片上调试模式下进行编程： 使用JTAG或SWD接口 不需要专用硬件通过用户程序中的代码和数据闪存编程例程进行编程： 允许在不重置系统的情况下进行代码和数据闪存编程	

Note 1. 约束适用于可以进行写入的范围组合。见表55.11。

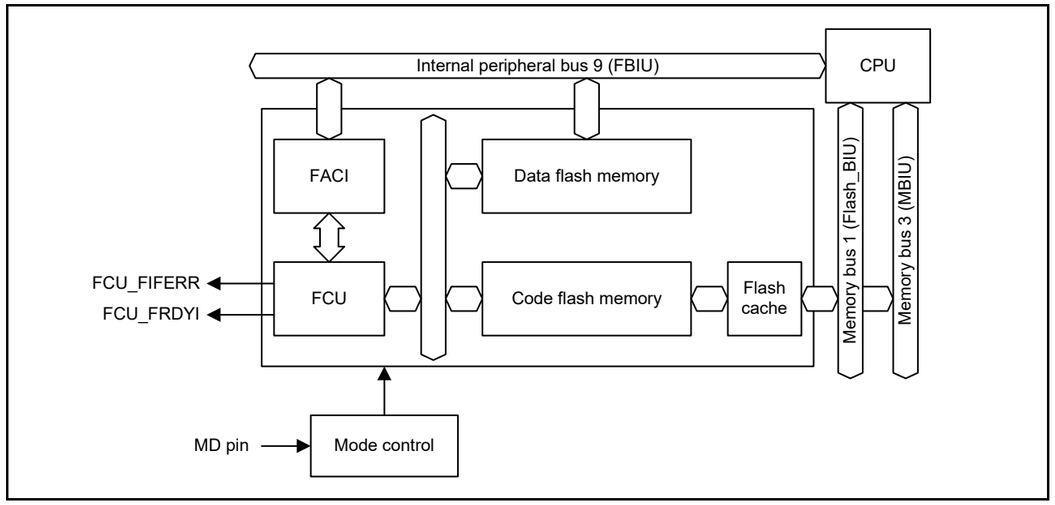


Figure 55.1 Block diagram of flash memory-related modules

55.2 Structure of Memory

Figure 55.2 shows the mapping of the code flash memory, and Table 55.2 shows the read and programming/erasure addresses by product. The user space of the code flash memory is divided into 8- and 32-KB blocks, which serve as the units of erasure. The user area is available for storing the user program.

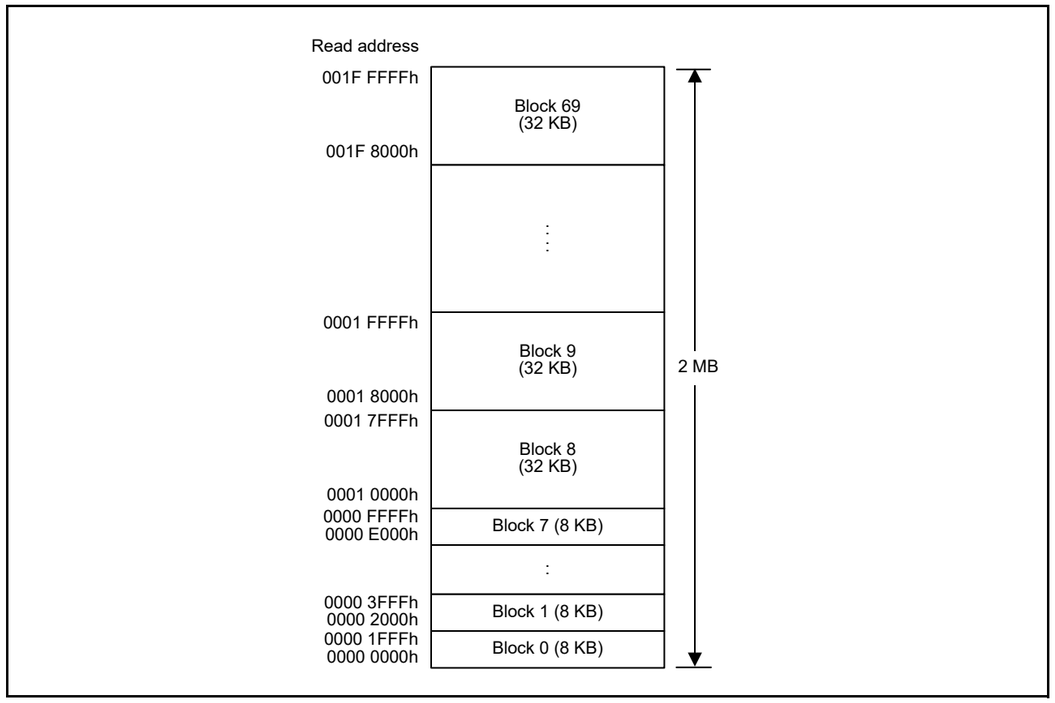


Figure 55.2 Mapping of the code flash memory

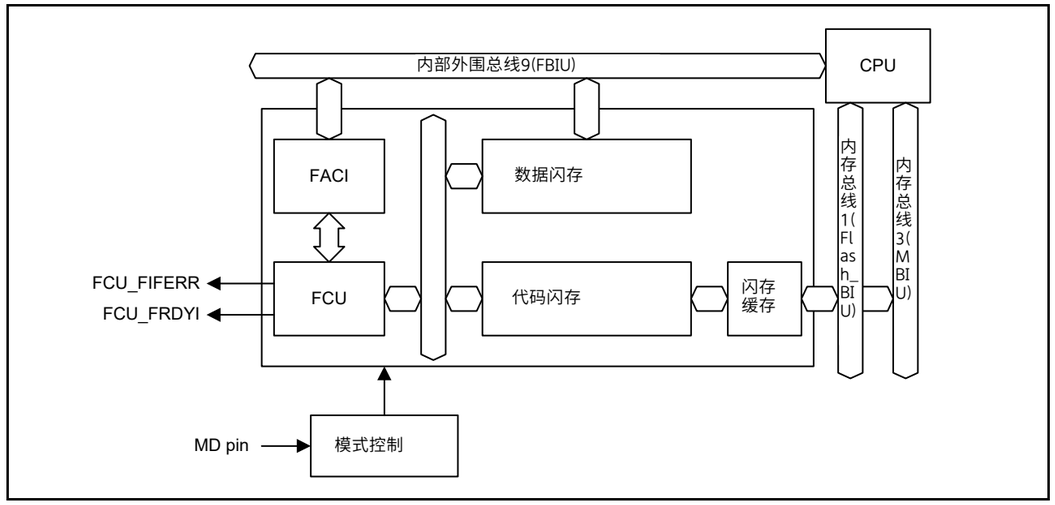


Figure 55.1 闪存相关模块框图

55.2 内存结构

图55.2显示了代码闪存的映射，表55.2显示了按产品划分的读取和编程擦除地址。代码闪存的用户空间分为8KB和32KB块，作为擦除单位。用户区可用于存储用户程序。

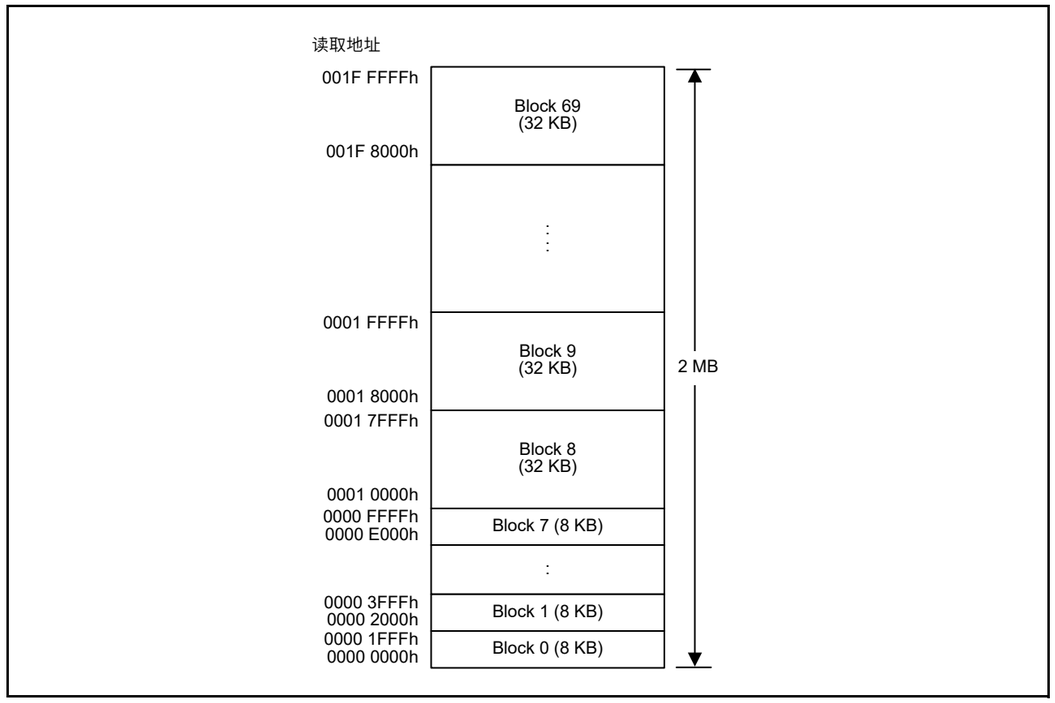


Figure 55.2 代码闪存的映射

Table 55.2 Read and P/E addresses by product for the code flash memory

Product	Read address	P/E address	Number of blocks
2-MB product	0000 0000h to 001F FFFFh	0000 0000h to 001F FFFFh	0 to 69
1-MB product	0000 0000h to 000F FFFFh	0000 0000h to 000F FFFFh	0 to 37

The data area of the data flash memory is divided into 64-byte blocks, with each being a unit for erasure. Figure 55.3 shows the mapping of the data flash memory.

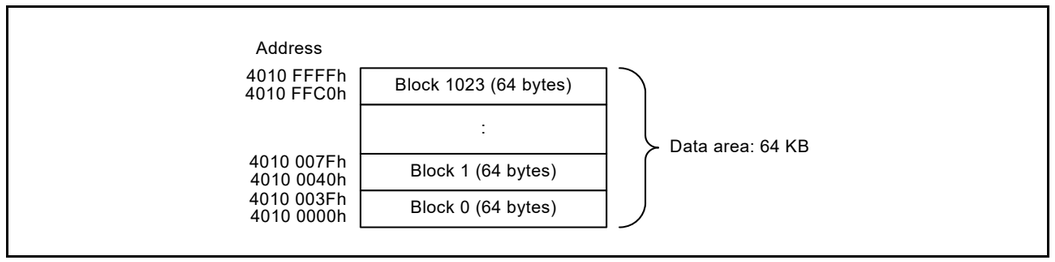


Figure 55.3 Mapping of the data flash memory

55.3 Register Descriptions

55.3.1 Flash Cache Enable Register (FCACHEE)

Address(es): FCACHE.FCACHEE 4001 C100h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FCACHEEN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	FCACHEEN	FCACHE Enable	0: Disable FCACHE 1: Enable FCACHE.	R/W
b15 to b1	—	Reserved	These bits are read as 0.	R

The FCACHEE.FCACHEEN bit enables or disables the flash cache function of FCACHE1, FCACHE2, and FLPF. This bit does not affect FCACHEIV.FCACHEIV. When FCACHE is enabled, the HPROT[3] determines whether it is cacheable or non-cacheable. See section 15.8 for details on HPROT[3].

Table 55.2 代码闪存按产品读取和PE地址

Product	读取地址	P/E address	块数
2-MB product	0000 0000h to 001F FFFFh	0000 0000h to 001F FFFFh	0 to 69
1-MB product	0000 0000h to 000F FFFFh	0000 0000h to 000F FFFFh	0 to 37

数据闪存的数据区被划分为64个字节的块，每个块为一个擦除单元。图55.3显示了数据闪存的映射。

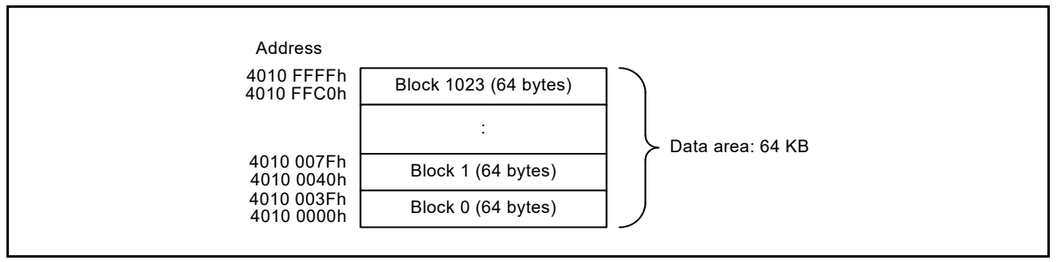


Figure 55.3 数据闪存的映射

55.3 注册说明

55.3.1 闪存缓存启用寄存器(FCACHEE)

Address(es): FCACHE.FCACHEE 4001 C100h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FCACHEEN
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	FCACHEEN	FCACHE Enable	0：禁用FCACHE1： 启用FCACHE。	R/W
b15 to b1	—	Reserved	这些位读为0。	R

FCACHEE.FCACHEEN位启用或禁用FCACHE1、FCACHE2和FLPF的闪存缓存功能。该位不影响FCACHEIV.FCACHEIV。当启用FCACHE时，HPROT[3]确定它是可缓存的还是不可缓存的。有关HPROT[3]的详细信息，请参见第15.8节。

55.3.2 Flash Cache Invalidate Register (FCACHEIV)

Address(es): FCACHE.FCACHEIV 4001 C104h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FCACHEIV
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	FCACHEIV	FCACHE Invalidate	• Reads: 0: Do not invalidate 1: Invalidate. • Writes: When write value is 1, FCACHE is invalidated. When write value is 0, this setting is ignored.	R/W
b15 to b1	—	Reserved	These bits are read as 0.	R

When 1 is written to the FCACHEIV.FCACHEIV bit, the flash cache data in FCACHE1, FCACHE2, and FLPF is invalidated.

55.3.3 Flash Wait Cycle Register (FLWT)

Address(es): FCACHE.FLWT 4001 C11Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	FLWT[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	FLWT[2:0]*1	Flash Wait Cycle	b2 b0 0 0 0: 0 waits (ICLK ≤ 40 MHz) 0 0 1: 1 wait (40 MHz < ICLK ≤ 80 MHz) 0 1 0: 2 waits (80 MHz < ICLK ≤ 120 MHz). Other settings are reserved.	R/W
b15 to b3	—	Reserved	These bits are read as 0.	R

Note 1. Settings other than 000b are prohibited in the SubOSC-speed mode.

The Flash Wait Cycle Register (FLWT) sets the access wait count for the flash memory. For faster clock frequencies, set FLWT.FLWT before changing the clock frequency. For slower clock frequencies, set FLWT.FLWT after changing the clock frequency.

55.3.2 闪存缓存无效寄存器(FCACHEIV)

Address(es): FCACHE.FCACHEIV 4001 C104h

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FCACHEIV
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	FCACHEIV	FCACHE Invalidate	读取：0：不无效1：无效。 写入：当写入值为1时，FCACHE无效。当写入值为0时，忽略此设置。	R/W
b15 to b1	—	Reserved	这些位读为0。	R

当FCACHEIV.FCACHEIV位写入1时，FCACHE1、FCACHE2和FLPF中的闪存缓存数据无效。

55.3.3 闪存等待周期寄存器(FLWT)

Address(es): FCACHE.FLWT 4001 C11Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	FLWT[2:0]		
重置后的值:	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b2 to b0	FLWT[2:0]*1	闪存等待周期	b2b0000：0次等待（ICLK≤40MHz）001：1次等待（40MHz<ICLK≤80MHz）010：2次等待（80MHz<ICLK≤120MHz）。保留其他设置。	R/W
b15 to b3	—	Reserved	这些位读为0。	R

Note 1. 在SubOSC速度模式中禁止设置000b以外的设置。

闪存等待周期寄存器(FLWT)设置闪存的访问等待计数。对于更快的时钟频率，设置
更改时钟频率之前的FLWT.FLWT。对于较慢的时钟频率，请在更改时钟频率后设置FLWT.FLWT。

55.3.4 Factory MCU Information Flash Root Table (FMIFRT)

Address(es): 407F B19Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	Value depends on the product															

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	Value depends on the product															

Bit	Description	R/W
b31 to b0	Base address of unique ID	R

The FMIFRT is a read-only register that stores a base address of the Unique ID register, Part Numbering register and MCU Version register. The FMIFRT should be read in 32-bit units. The base address of the RA6M3 MCU is 0x01007000.

55.3.5 Unique ID Register n (UIDRn) (n = 0 to 3)

Address(es): UIDR0 FMIFRT+14h, UIDR1 FMIFRT+18h, UIDR2 FMIFRT+1Ch, UIDR3 FMIFRT+20h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
Value after reset:	Unique value for each MCU															

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
Value after reset:	Unique value for each MCU															

Bit	Description	R/W
b31 to b0	Unique ID	R

The UIDRn is a read-only register that stores a 16-byte ID code (unique ID) for identifying the individual MCU. The UIDRn register should be read in 32-bit units.

55.3.4 工厂MCU信息闪存根表(FMIFRT)

Address(es): 407F B19Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值：	价值取决于产品															

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	价值取决于产品															

Bit	Description	R/W
b31 to b0	唯一标识的基地址	R

FMIFRT是一个只读寄存器，用于存储唯一ID寄存器的基地址、零件编号寄存器和MCU版本寄存器。FMIFRT应以32位为单位读取。RA6M3MCU的基地址为0x01007000。

55.3.5 唯一ID寄存器n(UIDRn)(n=0到3)

Address(es): UIDR0 FMIFRT+14h, UIDR1 FMIFRT+18h, UIDR2 FMIFRT+1Ch, UIDR3 FMIFRT+20h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
重置后的值：	每个MCU的独特价值															

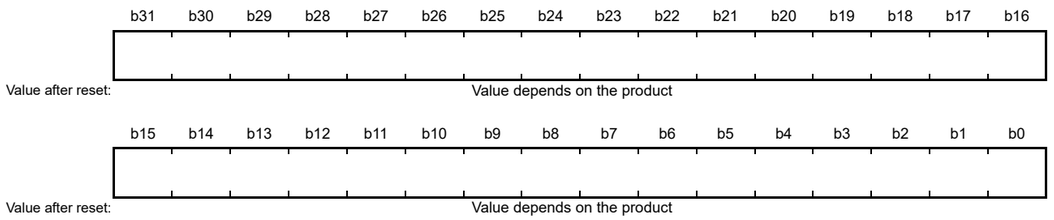
	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
重置后的值：	每个MCU的独特价值															

Bit	Description	R/W
b31 to b0	唯一身份	R

UIDRn是一个只读寄存器，它存储一个16字节的ID代码（唯一ID），用于识别单个MCU。这UIDRn寄存器应以32位为单位读取。

55.3.6 Part Numbering Register n (PNRn) (n = 0 to 3)

Address(es): PNR0 FMIFRT+24h, PNR1 FMIFRT+28h, PNR2 FMIFRT+2Ch, PNR3 FMIFRT+30h

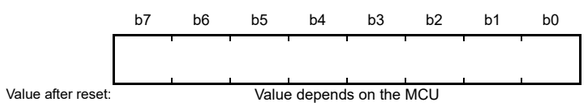


Bit	Description	R/W
b31 to b0	Product part number	R

The PNRn is a read-only register that stores a 16-byte part numbering. The PNRn register should be read in 32-bit units. Each byte corresponds to the ASCII code representation of the product part number as described in Table 1.14, Product list. The first character ("R", 0x52 in ASCII code) of the part number is stored in the byte with the smallest address (FMIFRT + 24h).

55.3.7 MCU Version Register (MCUVER)

Address(es): FMIFRT+44h



Bit	Description	R/W
b7 to b0	MCU version	R

The MCUVER is a read-only register that stores the MCU version. The MCUVER register should be read in 8-bit units. The higher the value, the newer the MCU version.

55.4 Flash Cache

55.4.1 Overview

The flash cache (FCACHE) speeds up read access from the bus master to the flash memory. The FCACHE includes:

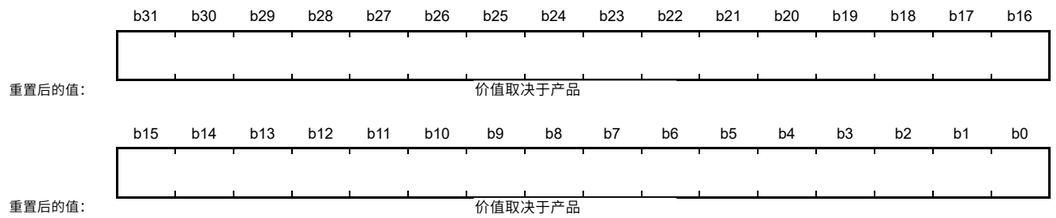
- FCACHE1, for CPU instruction fetches
- FCACHE2, for CPU operand access and DMA
- FLPF, for the prefetch access in CPU instruction fetches.

Table 55.3 Flash cache overview (1 of 2)

Parameter	Flash cache 1 (FCACHE1)	Flash cache 2 (FCACHE2)	Prefetch Buffer (FLPF)
Cache target region	0000 0000h - 001F FFFFh	0000 0000h - 001F FFFFh	0000 0000h - 001F FFFFh

55.3.6 零件编号寄存器n(PNRn)（n=0到3）

Address(es): PNR0 FMIFRT+24h, PNR1 FMIFRT+28h, PNR2 FMIFRT+2Ch, PNR3 FMIFRT+30h

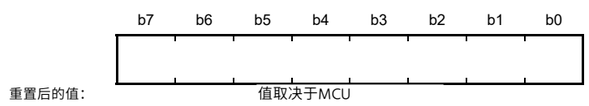


Bit	Description	R/W
b31 to b0	产品部件号	R

PNRn是一个只读寄存器，存储一个16字节的零件编号。PNRn寄存器应以32位为单位读取。每个字节对应于产品部件号的ASCII代码表示，如表1.14，产品列表中所述。零件编号的第一个字符（“R”，ASCII代码中的0x52）存储在地址最小的字节中（FMIFRT+24h）。

55.3.7 MCU版本寄存器(MCUVER)

Address(es): FMIFRT+44h



Bit	Description	R/W
b7 to b0	MCU version	R

MCUVER是一个只读寄存器，用于存储MCU版本。MCUVER寄存器应以8位为单位读取。
值越高，MCU版本越新。

55.4 闪存缓存

55.4.1 Overview

闪存高速缓存(FCACHE)加快了从总线主机到闪存的读取访问。FCACHE包括：

- FCACHE1，用于CPU指令取指
- FCACHE2，用于CPU操作数访问和DMA
- FLPF，用于CPU取指中的预取访问。

Table 55.3 闪存缓存概述(1of2)

Parameter	闪存缓存1(FCACHE1)	闪存缓存2(FCACHE2)	Prefetch Buffer (FLPF)
缓存目标区域	0000 0000h - 001F FFFFh	0000 0000h - 001F FFFFh	0000 0000h - 001F FFFFh

Table 55.3 Flash cache overview (2 of 2)

Parameter	Flash cache 1 (FCACHE1)	Flash cache 2 (FCACHE2)	Prefetch Buffer (FLPF)
Target bus master	CPU instruction fetch	CPU Operand Access and Access from other than CPU	FLPF
Capacity	256 bytes	16 bytes	32 bytes
Associativity	• 8-way set associative • 128 bits/entry (128-bit aligned data) • 2 entries/way	• Fully associative • 128 bits/entry (128-bit aligned data) • 1 entry for FCACHE2	• Fully associative • 128 bits/entry (128-bit aligned data) • 2 entries
Access cycles	• Cache hit: 0 waits • Cache miss: Number of waits set in Flash Wait Cycle Register	• Cache hit: 0 waits • Cache miss: Number of waits set in Flash Wait Cycle Register	• Cache hit: 0 waits • Cache miss: Number of waits set in Flash Wait Cycle Register

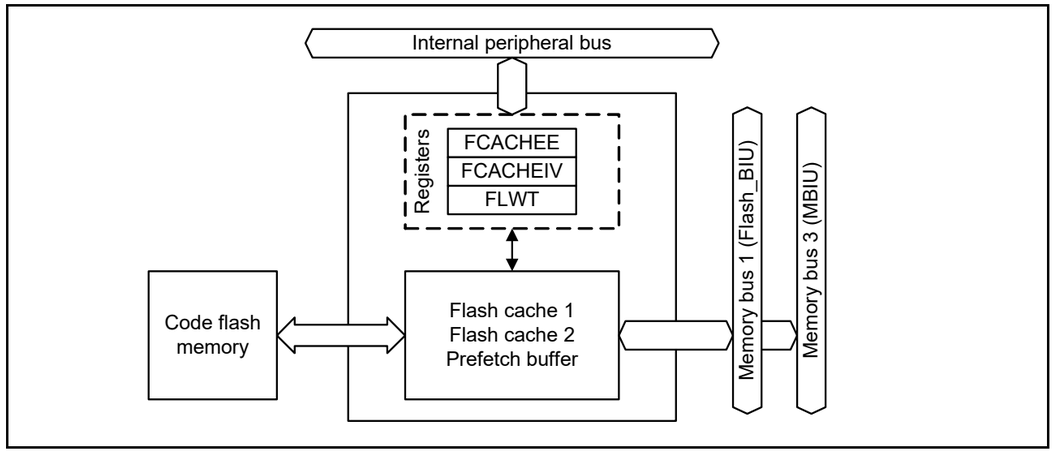


Figure 55.4 FCACHE block diagram

55.5 Operation

Use the FCACHEE register to set up and enable flash operation.

To set up the flash cache and prepare to rewrite the flash memory:

1. Disable the flash cache by resetting FCACHEE.FCACHEEN.*1
2. Invalidate the flash cache by setting FCACHEIV.FCACHEIV.
3. Check that FCACHEIV.FCACHEIV is 0.
4. Enable the flash cache by setting FCACHEE.FCACHEEN.

Note 1. It is not necessary to disable the flash cache on the first setup after reset.

55.5.1 Notice to use Flash Cache

When using Flash cache by access from the CPU, Arm® MPU should also be set to cacheable.

See the ARMv7-M Architecture Reference Manual and the Cortex-M4 Devices Generic User Guide.

55.6 Operating Modes Associated with the Flash Memory

Figure 55.5 shows a diagram of the mode transitions associated with the flash memory. For the procedures for setting the modes, see section 3, Operating Modes.

Table 55.3 闪存缓存概述(2of2)

Parameter	闪存缓存1(FCACHE1)	闪存缓存2(FCACHE2)	Prefetch Buffer (FLPF)
目标总线主机	CPU指令获取	CPU操作数访问和非CPU访问	FLPF
Capacity	256 bytes	16 bytes	32 bytes
Associativity	8路组关联 128位条目（128位对齐数据） 2项方式	完全关联 128位条目（128位对齐数据） FCACHE2的1个条目	完全关联 128位条目（128位对齐数据） 2个条目
访问周期	缓存命中：0次等待 缓存未命中Flash等待周期寄存器中设置的等待数	缓存命中：0次等待 缓存未命中Flash等待周期寄存器中设置的等待数	缓存命中：0次等待 缓存未命中：Flash等待周期寄存器中设置的等待数

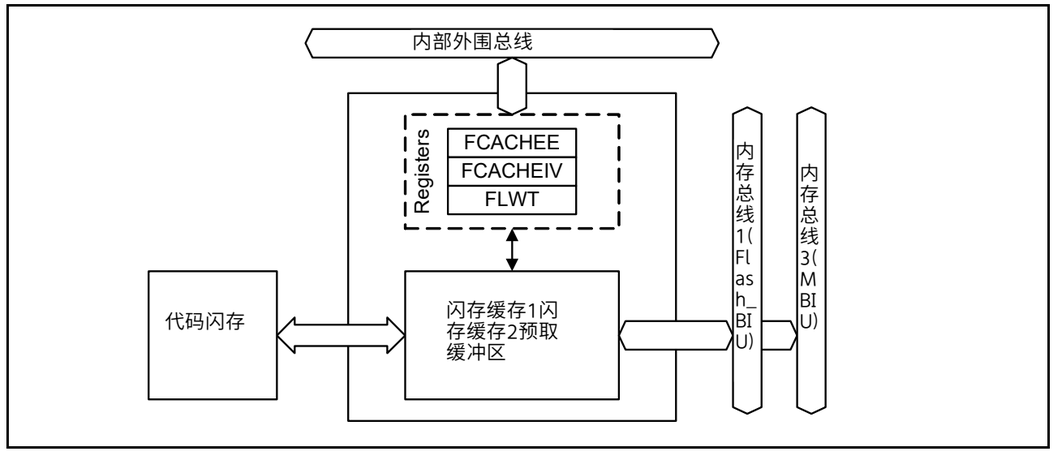


Figure 55.4 FCACHE框图

55.5 Operation

使用FCACHEE寄存器设置和启用闪存操作。

设置闪存缓存并准备重写闪存：

1. 通过重置FCACHEE.FCACHEEN禁用闪存缓存。*1
2. 通过设置FCACHEIV.FCACHEIV使闪存缓存无效。
3. 检查FCACHEIV.FCACHEIV是否为0。
4. 通过设置FCACHEE.FCACHEEN启用闪存缓存。

注1.复位后第一次设置时无需禁用闪存缓存。

55.5.1 使用FlashCache的注意事项

当通过CPU访问使用Flash缓存时，Arm®MPU也应设置为可缓存。

请参阅ARMv7-M架构参考手册和Cortex-M4设备通用用户指南。

55.6 与闪存相关的操作模式

图55.5显示了与闪存相关的模式转换图。有关设置模式的步骤，请参阅第3节，操作模式。

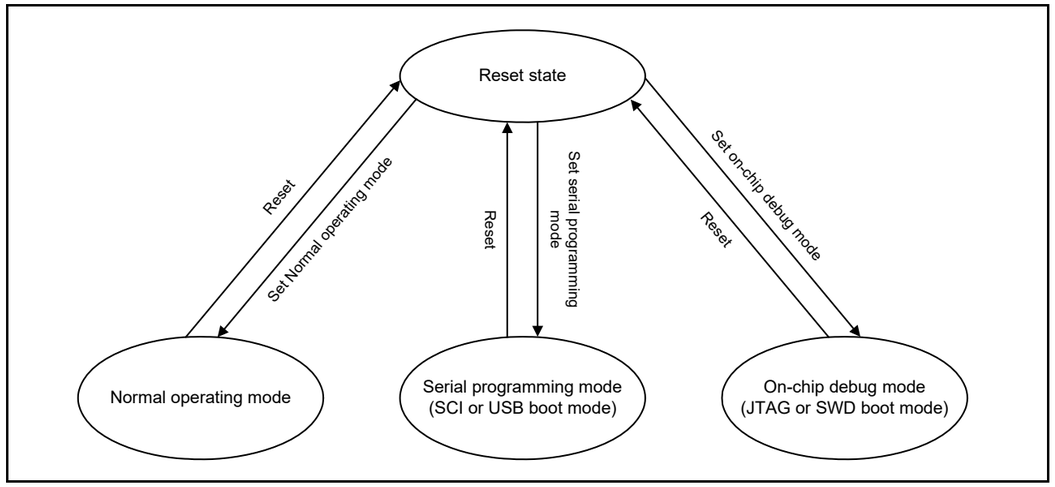


Figure 55.5 Mode transitions associated with flash memory

The flash memory area where programming and erasure are permitted and where the boot program executes after a reset differ with the mode. Table 55.4 shows the differences between the modes.

Table 55.4 Difference between modes

Parameter	Normal operating mode	Serial programming mode (SCI or USB boot mode)	On-chip debug mode (JTAG or SWD boot mode)
Programmable and erasable areas	• Code flash memory • Data flash memory	• Code flash memory • Data flash memory	• Code flash memory • Data flash memory
Erasure in block units	Possible	Possible	Possible
Boot program at a reset	User area program	Embedded program for serial programming	Depends on debug command

55.6.1 ID Code Protection

This function prohibits programming and on-chip debugging. The device validates or invalidates the ID code and determines the ID code based on an ID code stored in the flash memory. When ID code protection is enabled, the ID code sent from the host is compared with the ID code in the flash memory to determine whether they match. Programming and on-chip debugging are enabled only when the two match. The ID code in flash memory consists of four 32-bit words.

ID code bits 127 and 126 determine whether ID code protection is enabled and the method of authentication to use with the host. Table 55.5 shows how the ID code determines the method of authentication.

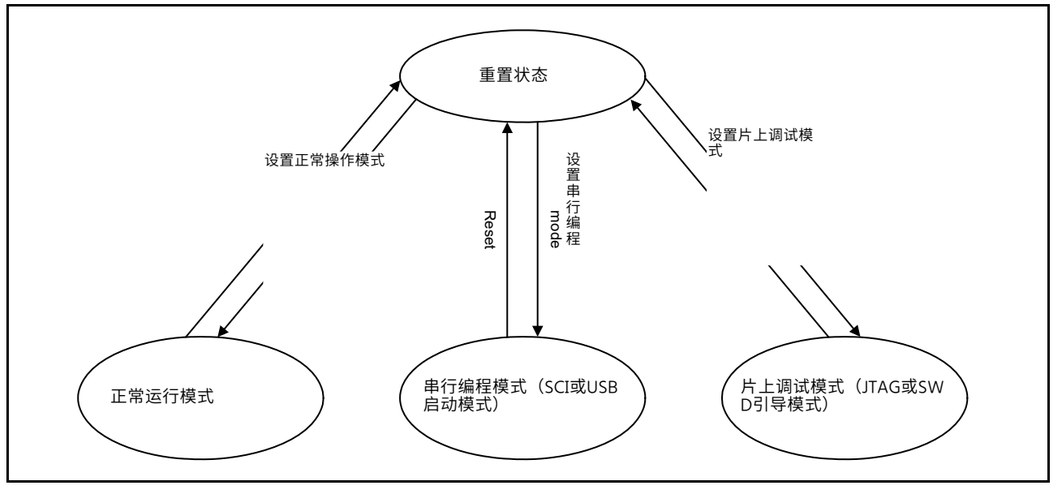


Figure 55.5 与闪存相关的模式转换

允许编程和擦除以及复位后执行引导程序的闪存区域因模式而异。表55.4显示了这些模式之间的差异。

Table 55.4 模式之间的差异

Parameter	正常运行模式	串行编程模式（SCI或USB启动模式）	片上调试模式（JTAG或SWD引导模式）
可编程和可擦除区域	代码闪存 数据闪存	代码闪存 数据闪存	代码闪存 数据闪存
以块为单位擦除	Possible	Possible	Possible
复位时的引导程序	用户区程序	用于串行编程的嵌入式程序	取决于调试命令

55.6.1 ID码保护

该功能禁止编程和片上调试。设备使ID代码有效或无效，并根据存储在闪存中的ID代码确定ID代码。启用ID码保护后，主机发送的ID码与闪存中的ID码进行比较，以确定它们是否匹配。编程和片上调试仅在两者匹配时才启用。闪存中的ID代码由四个32位字组成。

ID代码位127和126确定是否启用ID代码保护以及与主机一起使用的身份验证方法。表55.5显示了ID代码如何确定身份验证方法。

Table 55.5 Specifications for ID code protection

Operating mode on boot up	ID code	State of protection	Operations on connection with the programmer or on-chip debugger
Serial programming mode (SCI/USB boot mode) On-chip debug mode (JTAG/SWD boot mode)	FFh, …, FFh (All bytes = FFh)	Protection disabled	ID code validation is not performed, the ID code always matches, and connection to the programmer or the on-chip debugger is permitted.
	Bit 127 = 1, Bit 126 = 1, and at least one of the 16 bytes is not FFh	Protection enabled	Matching ID code: Authentication ends and connection to the programmer or on-chip debugger is permitted. Non-matching ID code: Additional transition to the ID code protection waiting state. When the ID code sent from the programmer or the on-chip debugger is “ALeRASE” in ASCII code (414C_6552_4153_45FF_FFFF_FFFF_FFFF_FFFFh), the content of the user flash (code and data) area and the configuration area are erased. However, forced erasure is not executed when the AWS.FSPR*1 bit is 0.
	Bit 127 = 1 and bit 126 = 0	Protection enabled	Matching ID code: Authentication ends and connection to the programmer or the on-chip debugger is permitted. Non-matching ID code: Additional transition to the ID code protection waiting state.
	Bit 127 = 0	Protection enabled	ID code validation is not performed, the ID code is always non-matching, and connection to the programmer or the on-chip debugger is prohibited.

Note 1. For details on the AWS.FSPR bit, see section 7.2.3, Access Window Setting Register (AWS).

55.7 Overview of Functions

By using a dedicated flash-memory programmer to program the on-chip flash memory through a serial interface (serial programming) or JTAG/SWD interface (on-chip debug mode), the device can be programmed before or after it is mounted on the target system.

Additionally, security functions to prohibit overwriting of the user program written to the on-chip flash memory are incorporated to prevent tampering by third parties.

Programming by the user program (self-programming) is available for applications that might require updating after system manufacturing or shipment. Protection features for safely overwriting the flash memory area are also provided. Additionally, interrupt processing during self-programming is supported so programming can proceed while processing external communications and other functions. Table 55.6 lists the programming methods and the corresponding operating modes.

Table 55.6 Programming methods (1 of 2)

Programming method	Functional overview	Operating mode
Serial programming	A dedicated flash-memory programmer through the SCI or USBFS interface enables on-board programming of the flash memory after the device is mounted on the target system.	Serial programming mode
	A dedicated flash-memory programmer through the SCI or USBFS interface and a dedicated programming adapter board allow off-board programming of the flash memory, for example, programming of the device before it is mounted on the target system.	

Table 55.5 ID码保护规范

启动时的操作模式	身份证号码	保护状态	与编程器或片上调试器连接的操作
串行编程模式（SCIUSB启动模式）	FFh, …, FFh (All bytes = FFh)	保护已禁用	不执行ID代码验证，ID代码始终匹配，并且允许连接到编程器或片上调试器。
片上调试模式（JTAGSWD引导模式）	Bit127=1，Bit126=1，16个字节中至少有一个不是FFh	启用保护	匹配ID代码：验证结束并允许连接到编程器或片上调试器。ID码不匹配：额外转换到ID码保护等待状态。 当编程器或片上调试器发送的ID码是ASCII码（414C_6552_4153_45FF_FFFF_FFFF_FFFF_FFFFh）中的“ALeRASE”时，用户闪存（代码和数据）区和配置区的内容被擦除。然而，强制擦除不执行时 AWS.FSPR*1位为0。
	位127=1和位126=0	启用保护	匹配ID代码：验证结束，允许连接到编程器或片上调试器。ID码不匹配：额外转换到ID码保护等待状态。
	Bit 127 = 0	启用保护	不执行ID码验证，ID码始终不匹配，禁止连接编程器或片上调试器。

Note 1. 有关AWS.FSPR位的详细信息，请参阅第7.2.3节，访问窗口设置寄存器(AWS)。

55.7 功能概述

通过使用专用闪存编程器通过串行接口（串行编程）或JTAGSWD接口（片上调试模式）对片上闪存进行编程，可以在器件安装到目标之前或之后对其进行编程系统。

此外，还集成了禁止覆盖写入片上闪存的用户程序的安全功能，以防止第三方篡改。

用户程序编程（自编程）可用于在系统制造或发货后可能需要更新的应用程序。还提供了用于安全覆盖闪存区域的保护功能。此外，支持自编程期间的中断处理，因此可以在处理外部通信和其他功能的同时继续编程。表55.6列出了编程方法和相应的操作模式。

Table 55.6 编程方法(1of2)

编程方法	功能概览	操作模式
串行编程	通过SCI或USBFS接口的专用闪存编程器可在器件安装到目标系统后对闪存进行板载编程。	串行编程模式
	通过SCI或USBFS接口的专用闪存编程器和专用编程适配器板允许对闪存进行板外编程，例如，在设备安装到目标系统之前对其进行编程。	

Table 55.6 Programming methods (2 of 2)

Programming method	Functional overview	Operating mode
Self-programming	A user program written to memory in advance of serial programming execution can also program the flash memory. The background operation capability makes it possible to fetch instructions or otherwise read data from the code flash memory while the data flash memory is programmed. As a result, a program resident in the code flash memory can program the data flash memory. Background operation can also be used for reading from and writing to the code flash memory by itself, but only when the address ranges of the code flash memory that are the targets for programming and reading satisfy particular conditions (see Table 55.11). When those conditions are met, a program resident in one half of the code flash memory can be executed to program the other half of the code flash memory. For background operations that are not possible, instructions in the code flash memory cannot be fetched and data cannot be accessed while the code flash memory is being programmed by self-programming. In such cases, a program for programming from the internal SRAM or external memory must be transferred in advance and executed.	Normal operating mode
JTAG or SWD programming	A dedicated flash-memory programmer or an on-chip debugger through JTAG or SWD enables on-board programming of the flash memory after the device is mounted on the target system.	On-chip debug mode
	A dedicated flash-memory programmer or an on-chip debugger through JTAG or SWD and a dedicated programming adapter board allow off-board programming of the flash memory, for example, programming of the device before it is mounted on the target system.	

Table 55.7 lists the functions of the on-chip flash memory. The functions in serial programming are realized by serial programmer commands, while the functions in self-programming are realized by reading of the on-chip flash memory by a FACI command or the user program.

Table 55.7 Basic functions

Function	Functional overview	Availability	
		Serial programming	Self-programming
Blank check	Checks a specified block to ensure that writing to it has not already proceeded. Results of reading from data flash memory to which nothing is written after erasure are not guaranteed, so use blank checking to confirm that writing to memory has not proceeded after erasure.	Not supported	Supported (data flash programming only)
Block erasure	Erases the memory contents in the specified block.	Supported	Supported
Programming	Writes to the specified address.	Supported	Supported
Read	Reads data programmed in the flash memory.	Supported	Not supported (read by user program is possible)
ID code check	Compares the ID code sent by the host with the code stored in the ROM, and if the two match, the FCU enters the wait state for programming and erasure commands from the host.	Supported	Not supported (ID authentication is not performed)
Security configuration	Configures the security function for serial programming.	Supported with conditions (only switching from enabled to disabled configuration is possible)	Supported with conditions (Only switching from enabled to disabled is possible)
Protection configuration	Configures the access window for flash area protection in the code flash memory.	Supported	Supported

The on-chip flash memory supports the ID code security function. Authentication of ID codes is a security function for use with serial programming and with JTAG or SWD programming. Table 55.8 lists the security functions supported by the on-chip flash memory, and Table 55.9 lists available operations and security settings.

Table 55.6 编程方法（2之2）

编程方法	功能概览	操作模式
Self-programming	在串行编程执行之前写入存储器的用户程序也可以对闪存进行编程。后台操作能力使得在对数据闪存进行编程时，可以从代码闪存中获取指令或以其他方式读取数据。结果，驻留在代码闪存中的程序可以对数据闪存进行编程。后台操作也可以单独用于对代码闪存进行读写，但仅当作为编程和读取目标的代码闪存的地址范围满足特定条件时（参见表55.11）。当满足这些条件时，可以执行驻留在一半代码闪存中的程序来对另一半代码闪存进行编程。对于无法进行的后台操作，在通过自编程对代码闪存进行编程时，无法获取代码闪存中的指令并且无法访问数据。在这种情况下，必须预先传输并执行从内部SRAM或外部存储器进行编程的程序。	正常运行模式
JTAG或SWD编程	专用闪存编程器或通过JTAG或SWD的片上调试器可在器件安装到目标系统后对闪存进行板载编程。	片上调试模式
	专用闪存编程器或通过JTAG或SWD的片上调试器和专用编程适配器板允许对闪存进行板外编程，例如，在将器件安装到目标系统之前对其进行编程。	

表55.7列出了片上闪存的功能。串行编程中的功能是通过串行编程器命令实现的，而自编程中的功能是通过FACI命令或用户程序读取片上闪存来实现的。

Table 55.7 基本功能

Function	功能概览	Availability	
		串行编程	Self-programming
空白支票	检查指定的块以确保尚未对其进行写入。无法保证从擦除后没有写入任何内容的数据闪存中读取的结果，因此使用空白检查来确认擦除后没有继续写入内存。	不支持	支持（仅数据闪存编程）
块擦除	擦除指定块中的内存内容。	Supported	Supported
Programming	写入指定地址。	Supported	Supported
Read	读取闪存中编程的数据。	Supported	不支持（可由用户程序读取）
识别码检查	将主机发送的ID代码与存储在ROM中的代码进行比较，如果两者匹配，则FCU进入等待状态，等待来自主机的编程和擦除命令。	Supported	不支持（不进行身份验证）
安全配置	配置串行编程的安全功能。	有条件支持（只能从启用配置切换到禁用配置）	有条件支持（只能从启用切换到禁用）
保护配置	配置代码闪存中闪存区域保护的访问窗口。	Supported	Supported

片上闪存支持ID码安全功能。ID代码验证是一种安全功能，可用于串行编程和JTAG或SWD编程。表55.8列出了片上闪存支持的安全功能，表55.9列出了可用的操作和安全设置。

Table 55.8 Security functions

Function	Description
ID authentication	Result of ID authentication can be used to control the connection of a serial programmer for serial programming.

Table 55.9 Available operations and security settings

	All security settings and erasure, programming, and read operations		Cautions regarding the security setting configuration
Function	Serial programming and on-chip debug mode	Self-programming mode	Self-programming mode
ID authentication	When ID codes do not match: • Block erasure commands: Not supported • Programming commands: Not supported • Read commands: Not supported • Security configuration commands: Not supported • Protection configuration commands: Not supported When ID codes match: • Block erasure commands: Supported • Programming commands: Supported • Read commands: Supported • Security configuration commands: Supported • Protection configuration commands: Supported	(ID authentication is not performed.) • Blank check: Supported • Block erasure: Supported • Programming: Supported • Security configuration: Supported • Protection configuration: Supported	ID authentication is not performed.

55.7.1 Configuration Area Bit Map

Figure 55.6 shows the configuration area bit map. The boot program must use these bits as hexadecimal data.

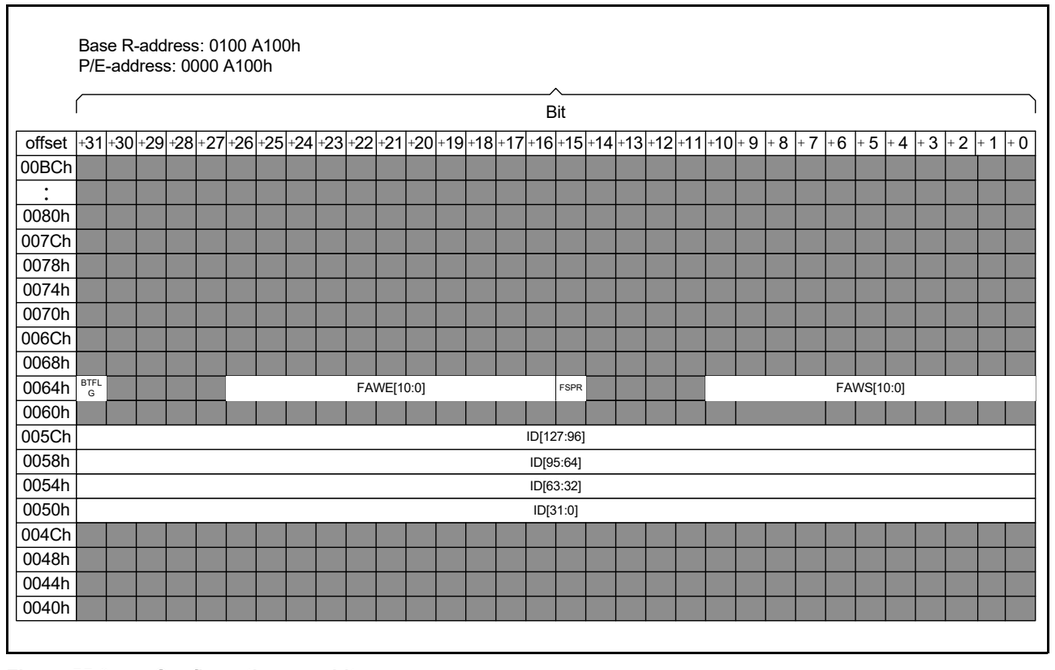


Figure 55.6 Configuration area bit map

Table 55.8 安全功能

Function	Description
身份认证	身份认证的结果可以用来控制串口编程器的连接，进行串口编程。

Table 55.9 可用的操作和安全设置

	所有安全设置和擦除、编程和读取操作		有关安全设置配置的注意事项
Function	串行编程和片上调试模式	Self-programming mode	Self-programming mode
身份认证	当ID代码不匹配时： 块擦除命令：不支持 编程命令（不进行身份验证。） 空白检查：支持 块擦除：支持 编程：支持 安全配置：支持 保护配置：支持 ：不支持 读取命令：不支持 安全配置命令：不支持 保护配置命令：不支持ID代码匹配时： 块擦除命令：支持 编程命令：支持 读取命令：支持 安全配置命令：支持 保护配置命令：支持		不进行身份验证。

55.7.1 配置区位图

图55.6显示了配置区域位图。引导程序必须使用这些位作为十六进制数据。

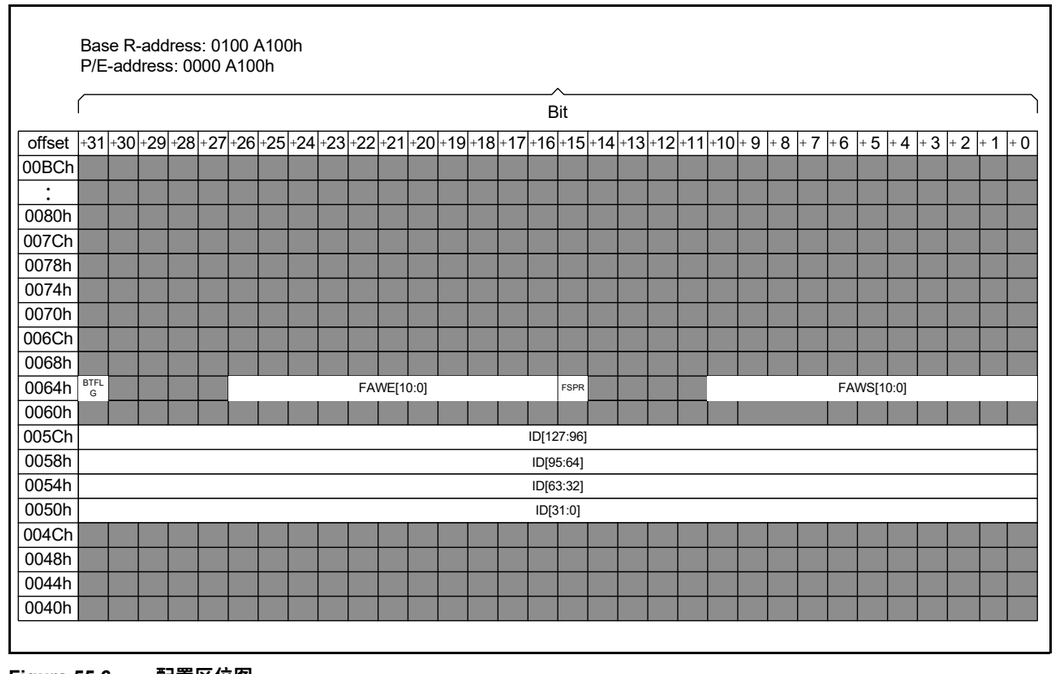
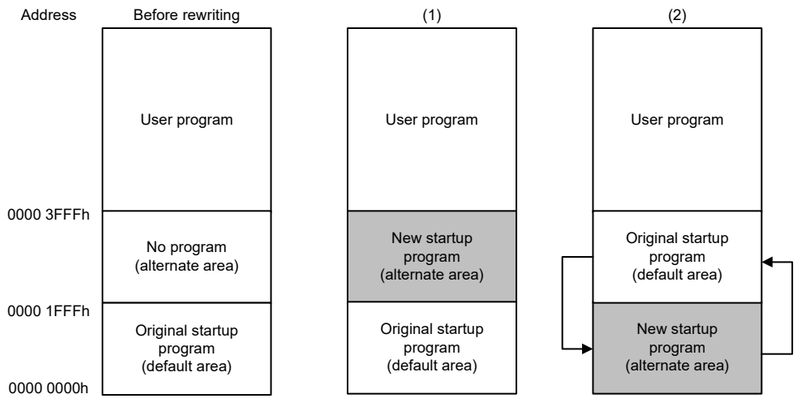


Figure 55.6 配置区位图

55.7.2 Startup Area Select

The startup area select function allows the boot program to be safely updated. The size of the startup area is 8 KB, and the startup area is located in the user area. FACI controls the address of the startup area based on the startup area select flag (AWS.BTFLG) that is located in the configuration area. The startup area can be locked by the AWS.FSPR*1 bit.

Note 1. For the AWS.FSPR bit, see section 7.2.3, Access Window Setting Register (AWS).



(1) Program a new startup program in the alternate area. If the alternate area fails to be rewritten, the new startup program can be rewritten again after starting up using the default area, because the original startup program is in the default area.
(2) After the alternate area is successfully rewritten, the default and alternate areas are switched using the self-programming library. After that, the program in the alternate area starts after a reset.

Figure 55.7 Overview of startup program protection

55.7.3 Protection by Access Window

Issuing the program or block erase command to a flash memory area outside of the access window results in the command-locked state. The access window is only valid in the user area of the code flash memory. The access window provides protection in self-programming mode, serial programming mode, and on-chip debug mode.

The access window is specified in both the AWS.FAWS[10:0] and AWS.FAWE[10:0]*1 bits. The following describes how to set the FAWS and FAWE bits in different conditions:

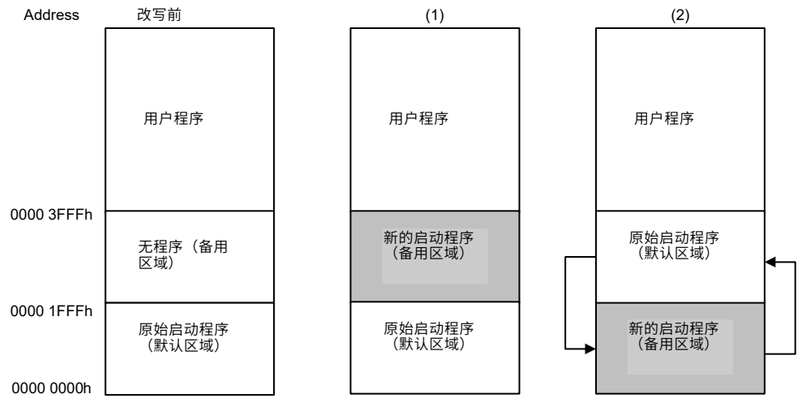
- FAWE = FAWS: The P/E command can execute anywhere in the user area of the code flash memory
- FAWE > FAWS: The P/E command can only execute in the window from the block pointed to by the FAWS bits to one block lower than the one pointed to by the FAWE bits
- FSWE < FAWS: The P/E command cannot execute anywhere in the user area of the code flash memory.

Note 1. For information on the AWS.FAWS and AWS.FAWE bits, see section 7.2.4, OCD/Serial Programmer ID Setting Register (OSIS).

55.7.2 启动区域选择

启动区域选择功能允许安全更新引导程序。启动区大小为8KB，启动区位于用户区。FACI根据位于配置区域中的启动区域选择标志(AWS.BTFLG)控制启动区域的地址。启动区域可以通过AWS.FSPR*1位锁定。

注1.关于AWS.FSPR位，请参见第7.2.3节，访问窗口设置寄存器(AWS)。



⑴在备用区编写一个新的启动程序。如果替换区改写失败，新的启动程序可以在使用默认区启动后重新改写，因为原来的启动程序在默认区。⑵备用区改写成功后，使用自编程库切换默认区和备用区。之后，备用区域中的程序在重置后启动。

Figure 55.7 启动程序保护概述

55.7.3 通过访问窗口保护

向访问窗口之外的闪存区域发出程序或块擦除命令会导致命令锁定状态。访问窗口仅在代码闪存的用户区有效。访问窗口在自编程模式、串行编程模式和片上调试模式下提供保护。

访问窗口在AWS.FAWS[10:0]和AWS.FAWE[10:0]*1位中指定。下面介绍如何在不同条件下设置FAWS和FAWE位：

- FAWE=FAWS：PE命令可以在代码闪存用户区的任何地方执行
- FAWE>FAWS：PE命令只能在窗口中从FAWS位指向的块到比FAWE位指向的块低一个块执行
- FSWE<FAWS：PE命令不能在代码闪存的用户区的任何地方执行。

注1.有关AWS.FAWS和AWS.FAWE位的信息，请参阅第7.2.4节，OCD串行程序员ID设置
Register (OSIS).

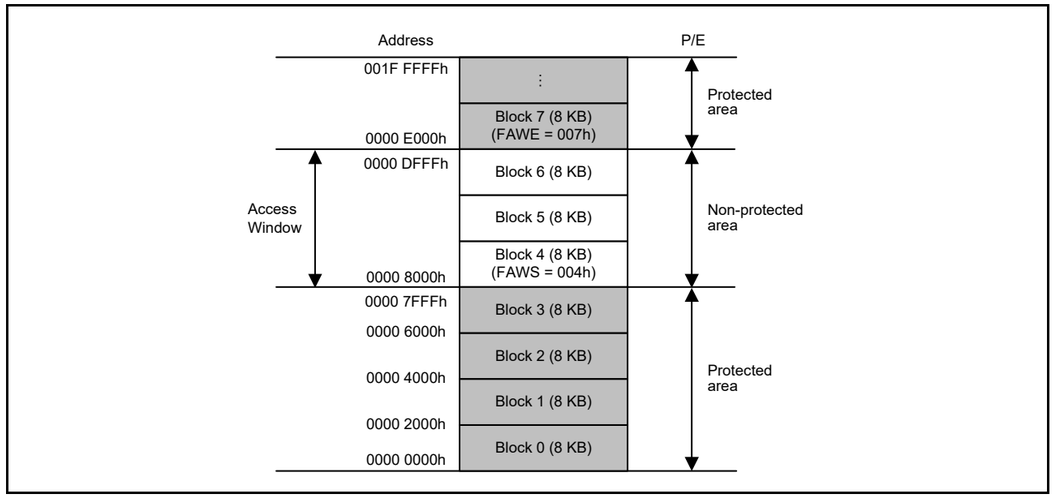


Figure 55.8 Start block address (FAWS) and end block address (FAWE) of access window when the access window only includes the 8-KB block size

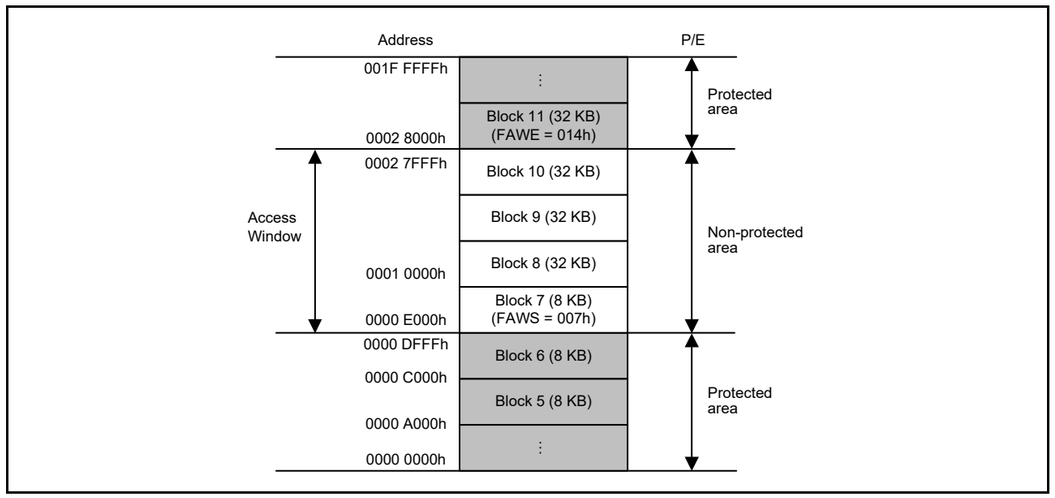


Figure 55.9 Start block address (FAWS) and end block address (FAWE) of access window when the access window includes 8-KB and 32-KB block sizes

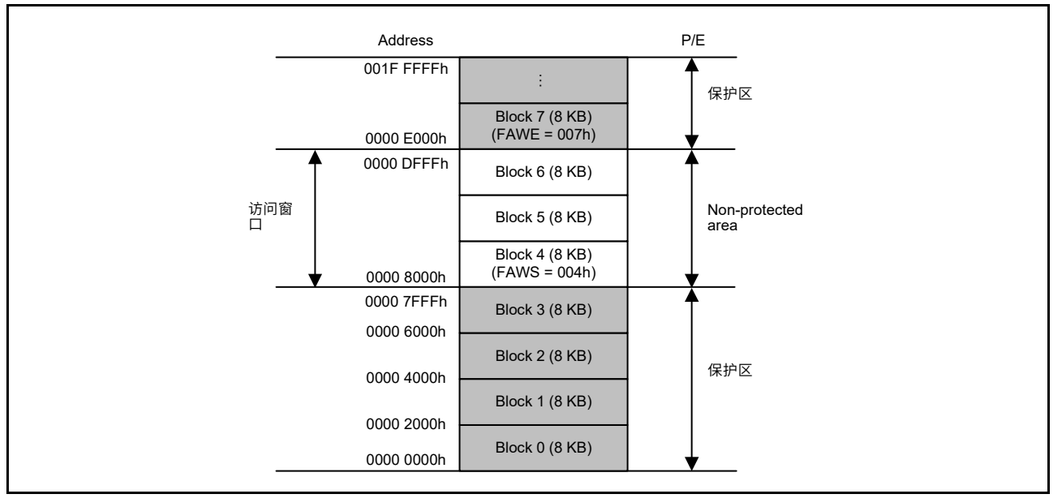


Figure 55.8 当访问窗口仅包含8-KB块大小时访问窗口的起始块地址(FAWS)和结束块地址(FAWE)

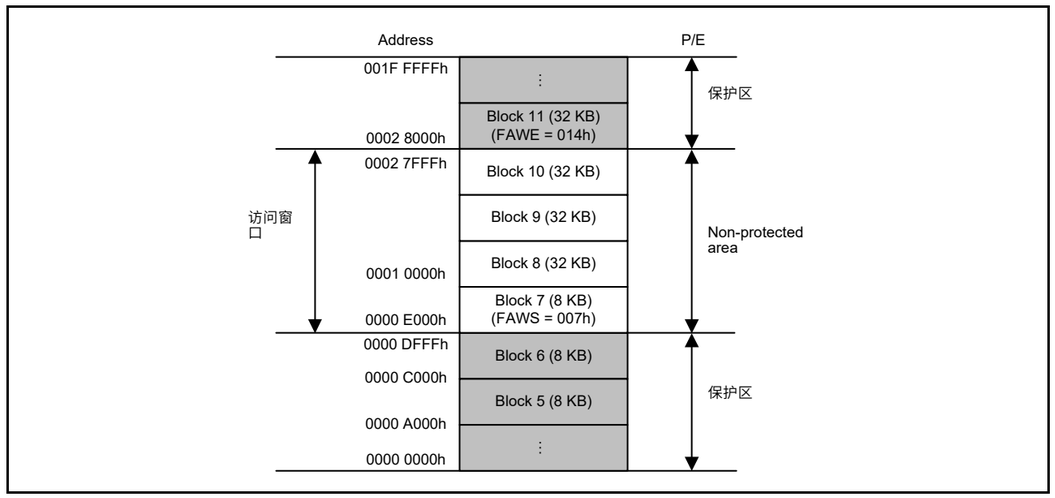


Figure 55.9 当访问窗口包括8-KB和32-KB块大小时访问窗口的起始块地址(FAWS)和结束块地址(FAWE)

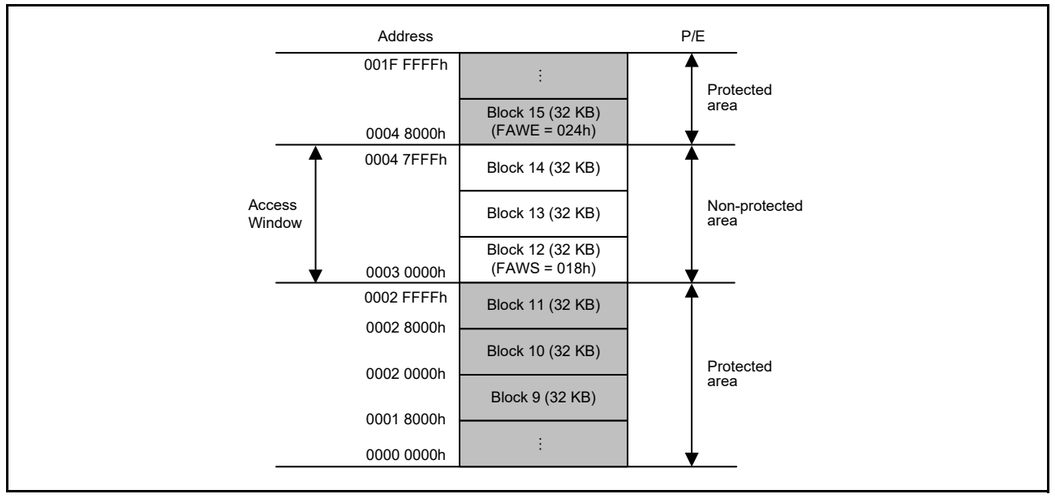


Figure 55.10 Start block address (FAWS) and end block address (FAWE) of access window when the access window only includes the 32-KB block size

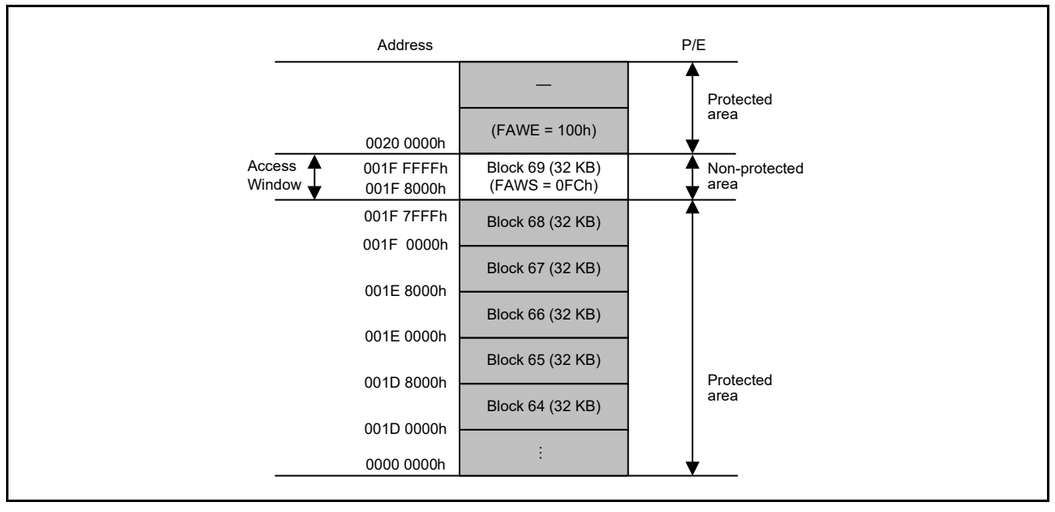


Figure 55.11 Start block address (FAWS) and end block address (FAWE) of access window when the access window only includes the final block

55.8 Programming Commands

The FACI controls the FCU in accordance with the specified FACI commands.

55.9 Suspend Operation

Reading from the code or data flash memory is not possible during programming or erasure when the address ranges do not satisfy the conditions for background operation. When a P/E suspend command is issued to suspend the programming or erasure of the code or data flash memory, reading from the memory is enabled. One suspend command mode is available for programming and two suspend command modes are available for erasure (suspension priority mode and erasure priority mode). The P/E resume command is available for resuming suspended programming or erasure.

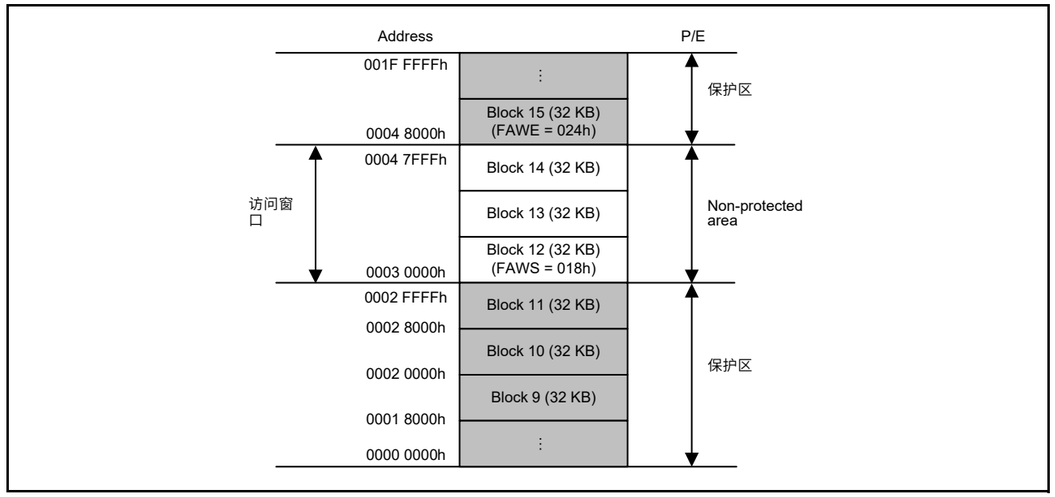


Figure 55.10 当访问窗口仅包含32−KB块大小时访问窗口的起始块地址(FAWS)和结束块地址(FAWE)

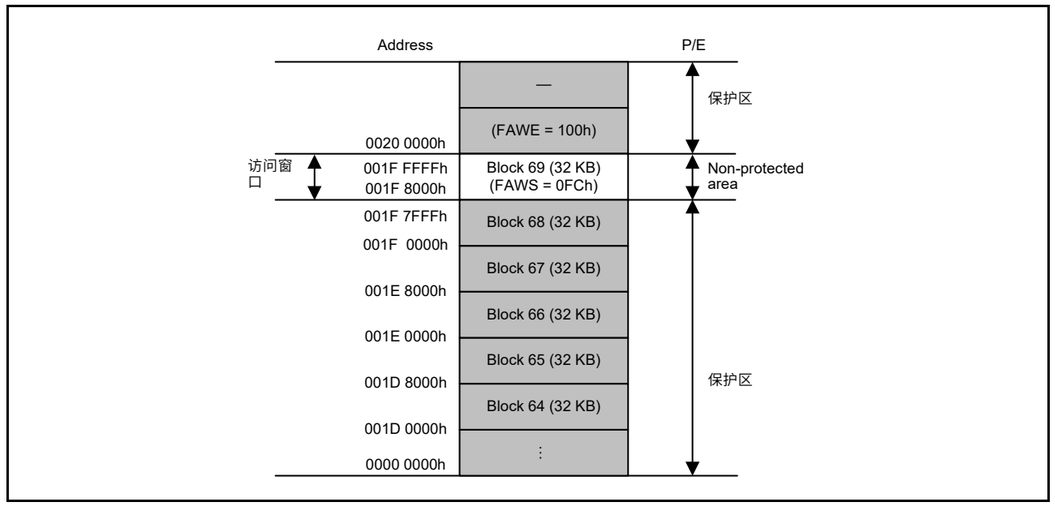


Figure 55.11 访问窗口只包含最终块时访问窗口的起始块地址（FAWS）和结束块地址（FAWE）

55.8 编程命令

FACI根据指定的FACI命令控制FCU。

55.9 暂停操作

当地址范围不满足后台操作条件时，在编程或擦除期间无法读取代码或数据闪存。当发出PE暂停命令以暂停代码或数据闪存的编程或擦除时，将启用从存储器读取。一种挂起命令模式可用于编程，两种挂起命令模式可用于擦除（挂起优先模式和擦除优先模式）。PEresume命令可用于恢复暂停的编程或擦除。

55.10 Protection

Provided types of protection include:

- Software protection
- Error protection
- Boot program protection.

55.11 Serial Programming Mode

The serial programming modes include:

- Boot mode with SCI9
- USB boot mode with the USBFS.

Table 55.10 lists the I/O pins for the flash memory-related modules.

Table 55.10 I/O pins for flash memory-related modules

Pin name	I/O	Applicable modes	Function
MD	Input	SCI boot mode USB boot mode (Serial programming mode)	Selection of operating mode
P110/RXD9	Input	SCI boot mode	For host communication, to receive data through SCI
P109/TXD9	Output		For host communication, to transmit data through SCI
USB_DP, USB_DM	I/O	USB boot mode	USB data I/O
USB_VBUS	Input		Detection of connection and disconnection of USB cables

55.11.1 SCI Boot Mode

In boot mode, the host sends control commands and data for programming, and the code and data flash memory area are programmed or erased accordingly. An on-chip SCI handles transfer between the host and the MCU in asynchronous mode. Tools for transmission of control commands and the data for programming must be prepared in the host.

When the MCU is activated in boot mode, the embedded program for serial programming is executed. This program automatically adjusts the bit rate of the SCI and controls programming and erasure by receiving control commands from the host. The USB cable must not be connected on reset release.

Figure 55.12 shows the system configuration for operations in boot mode.

55.10 Protection

提供的保护类型包括：

- 软件保护
- 错误保护
- 引导程序保护。

55.11 串行编程模式

串行编程模式包括：

- 带有SCI9的引导模式
- USB引导模式与USBFS。

表55.10列出了闪存相关模块的IO引脚。

Table 55.10 闪存相关模块的IO引脚

引脚名称	I/O	适用模式	Function
MD	Input	SCI启动模式USB启动模式（串行编程模式）	操作模式的选择
P110/RXD9	Input	SCI开机模式	用于主机通信，通过SCI接收数据
P109/TXD9	Output		用于主机通信，通过SCI传输数据
USB_DP, USB_DM	I/O	USB启动模式	USB数据输入输出
USB_VBUS	Input		检测USB电缆的连接和断开

55.11.1 SCI启动模式

在引导模式下，主机发送控制命令和数据进行编程，代码和数据闪存区域被相应地编程或擦除。片上SCI以异步模式处理主机和MCU之间的传输。主机中必须准备好用于传输控制命令和编程数据的工具。

当MCU在引导模式下激活时，将执行用于串行编程的嵌入式程序。该程序通过接收来自主机的控制命令自动调整SCI的比特率并控制编程和擦除。复位释放时不得连接USB电缆。

图55.12显示了引导模式下操作的系统配置。

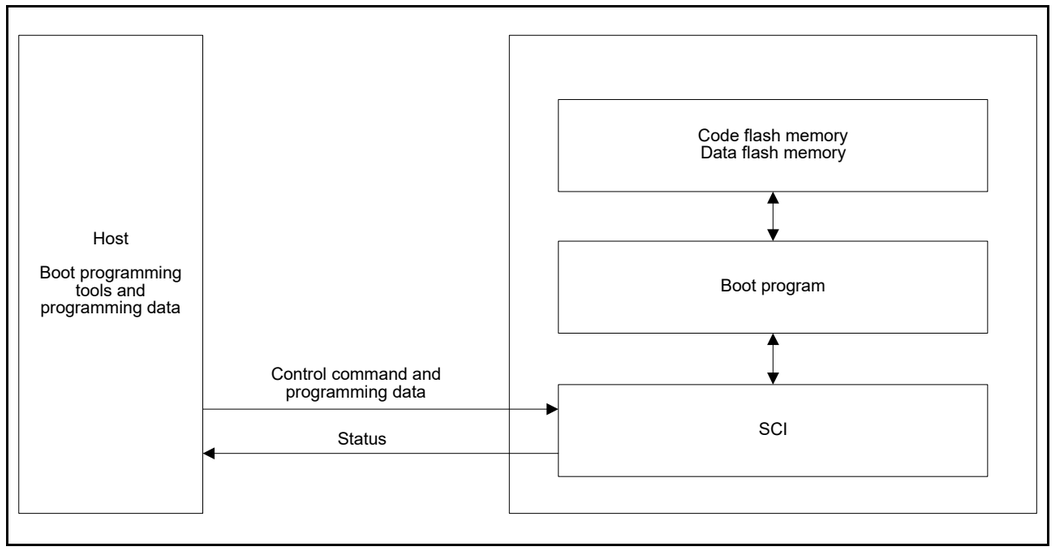


Figure 55.12 System configuration in SCI boot mode

55.11.2 USB Boot Mode

In USB boot mode, the code and data flash memory are programmed or erased by control commands and data for programming transmitted from an externally connected host through the USB interface.

Using USB boot mode requires preparation on the host side of the tools for transmitting control commands and data for programming, and of the data. Figure 55.13 shows the configuration of a system for use in USB boot mode. The USB cable must be connected on reset release.

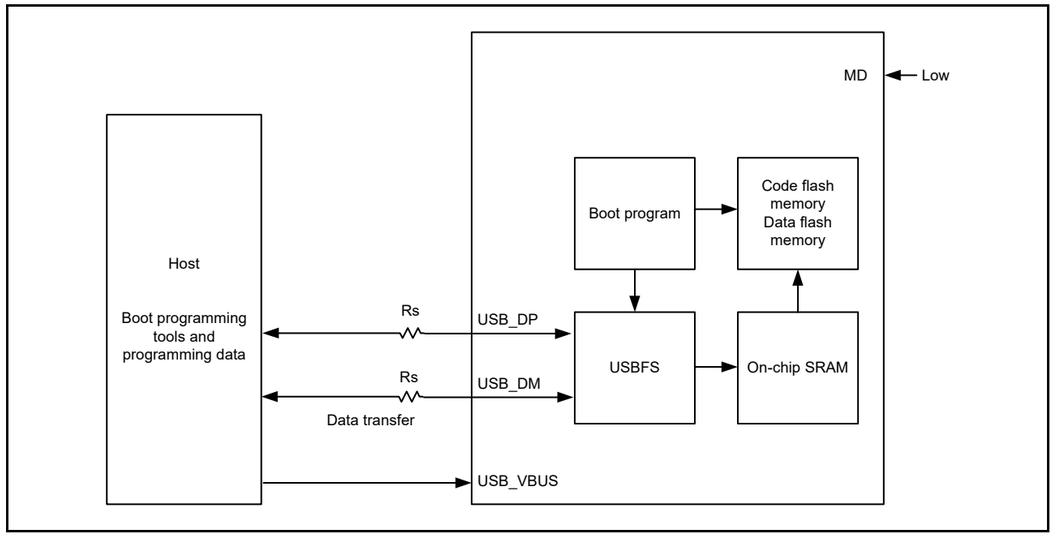


Figure 55.13 System configuration in USB boot mode

55.12 Using a Serial Programmer for Programming

A dedicated flash memory programmer can be used to program the flash memory in serial programming mode.

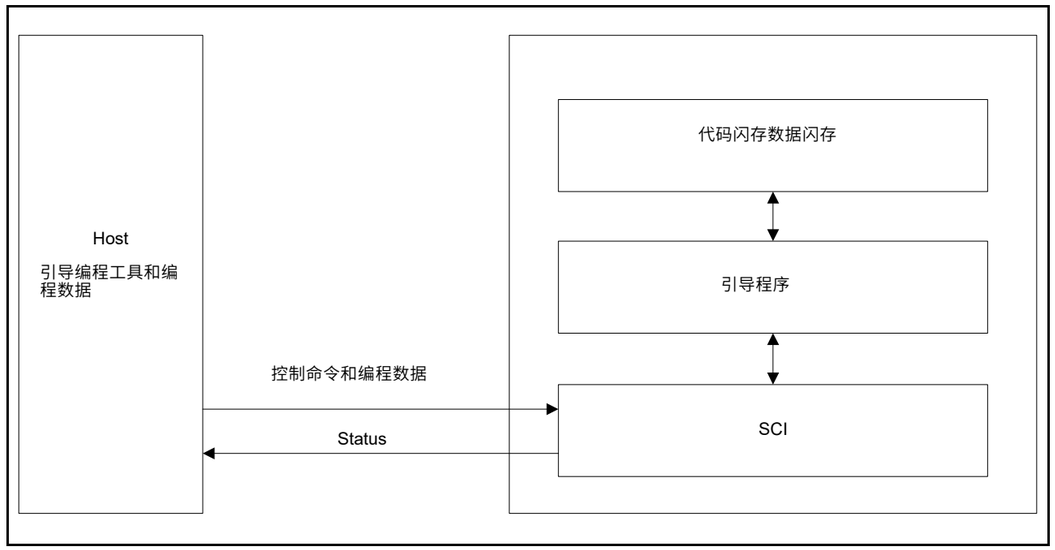


Figure 55.12 SCI引导模式下的系统配置

55.11.2 USB启动模式

在USB引导模式下，代码和数据闪存通过USB接口从外部连接的主机传输的控制命令和用于编程的数据进行编程或擦除。

使用USB引导模式需要在主机端准备用于传输控制命令和数据以进行编程的工具以及数据。图55.13显示了用于USB引导模式的系统配置。USB电缆必须在复位释放时连接。

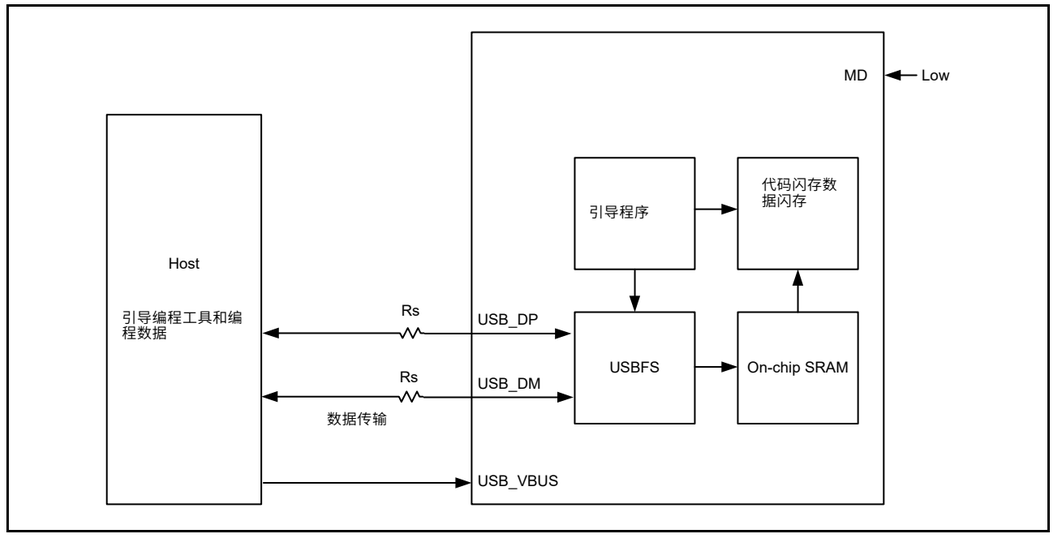


Figure 55.13 USB引导模式下的系统配置

55.12 使用串行编程器进行编程

可以使用专用的闪存编程器在串行编程模式下对闪存进行编程。

55.12.1 Serial Programming

The MCU is mounted on the system board for serial programming. A connector to the board allows programming by the flash memory programmer to proceed.

55.12.2 Programming Environments

Figure 55.14 shows the environments that Renesas recommends for programming the flash memory of the MCU with data.

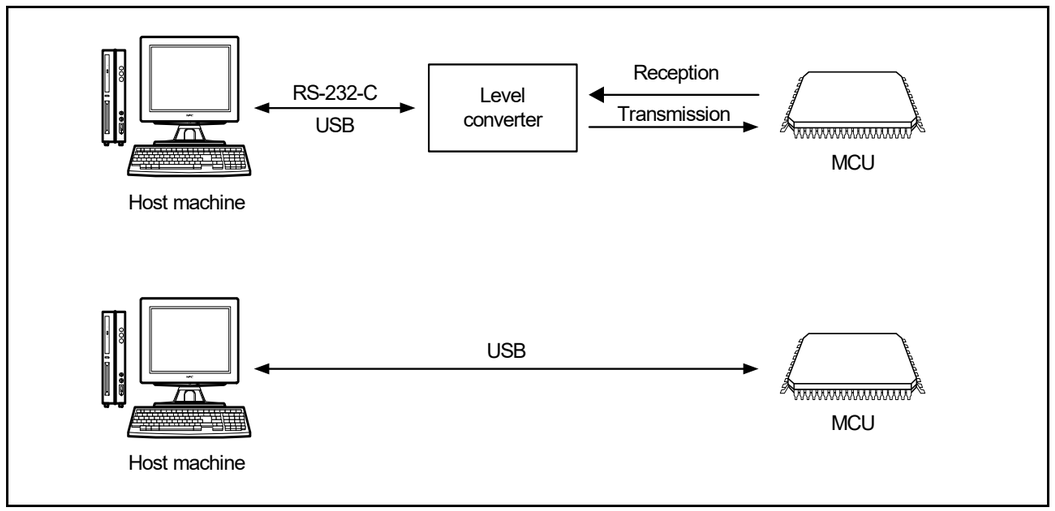


Figure 55.14 Environments for writing programs to the flash memory

55.13 Programming through Self-Programming

55.13.1 Overview

The MCU supports programming of the flash memory by the user program itself. The programming commands can be used with user programs for writing to both the code and data flash memory. This enables upgrading of user programs and overwriting of constant data fields.

For data flash memory programming, the background operation facility makes it possible to program the memory from a programming program in the code flash memory. This programming program can also be copied in advance to and executed from the internal SRAM or external memory.

For code flash memory programming, background operation is available for use when the address ranges of the code flash memory area to be programmed and the code flash memory area to be read satisfy particular conditions (see Table 55.11). For self-programming, a programming program in one half of the code flash memory can be used to program the other half of the code flash memory. This programming program can also be copied in advance to and executed from the internal SRAM or external memory. This is useful when the address ranges do not satisfy the conditions for background operation.

55.12.1 串行编程

MCU安装在系统板上，用于串行编程。板上的连接器允许闪存编程器进行编程。

55.12.2 编程环境

图55.14显示了瑞萨推荐的使用数据对MCU闪存进行编程的环境。

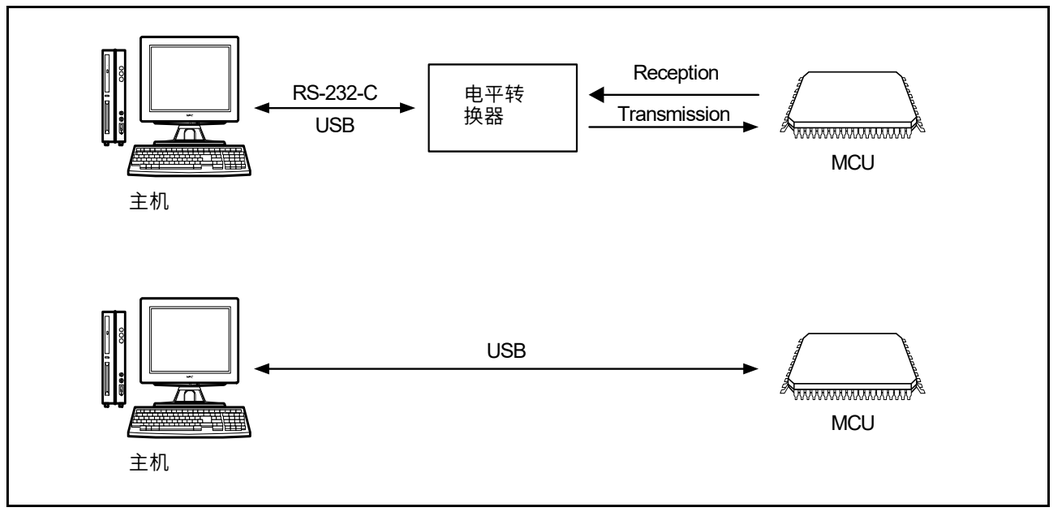


Figure 55.14 将程序写入闪存的环境

55.13 通过自编程进行编程

55.13.1 Overview

MCU支持用户程序本身对闪存进行编程。编程命令可与用户程序一起用于写入代码和数据闪存。这使得用户程序的升级和常量数据字段的覆盖成为可能。

对于数据闪存编程，后台操作工具可以通过代码闪存中的编程程序对存储器进行编程。该编程程序也可以预先复制到内部SRAM或外部存储器中执行。

对于代码闪存编程，当要编程的代码闪存区域和要读取的代码闪存区域的地址范围满足特定条件时，可以使用后台操作（参见表55.11）。对于自编程，可以使用一半代码闪存中的编程程序对另一半代码闪存进行编程。该编程程序也可以预先复制到内部SRAM或外部存储器中执行。当地址范围不满足后台操作的条件时，这很有用。

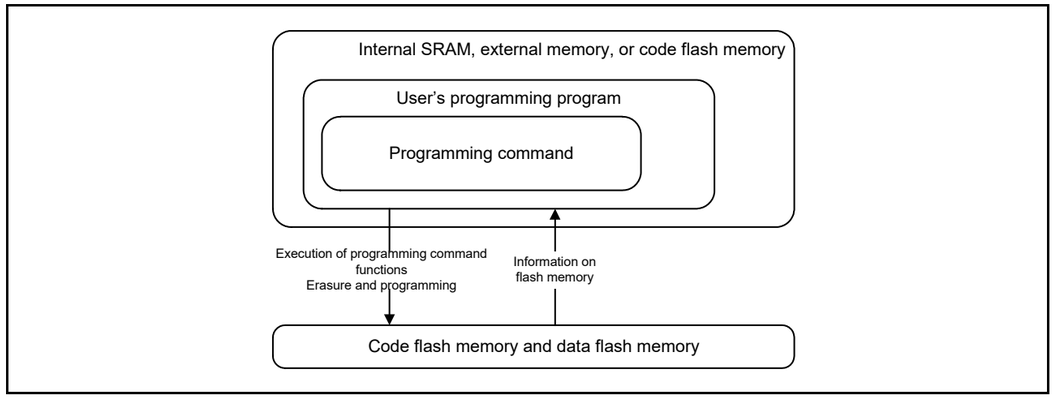


Figure 55.15 Schematic view of self-programming

55.13.2 Background Operation

Background operation can be used when a combination of the flash memory for writing and reading is any of those listed in Table 55.11.

Table 55.11 Conditions under which background operation is available

Product	Range for writing	Range for reading
All products	Data flash memory	Code flash memory
	Code flash memory	Data flash memory
2-MB products	First half (1 MB) of the user area of the code flash memory (addresses 0000 0000h to 000F FFFFh)	Second half (1 MB) of the user area of the code flash memory (addresses 0010 0000h to 001F FFFFh)
	Second half (1 MB) of the user area of the code flash memory (addresses 0010 0000h to 001F FFFFh)	First half (1 MB) of the user area of the code flash memory (addresses 0000 0000h to 000F FFFFh)
1-MB products	First half (0.5 MB) of the user area of the code flash memory (addresses 0000 0000h to 0007 FFFFh)	Second half (0.5 MB) of the user area of the code flash memory (addresses 0008 0000h to 000F FFFFh)
	Second half (0.5 MB) of the user area of the code flash memory (addresses 0008 0000h to 000F FFFFh)	First half (0.5 MB) of the user area of the code flash memory (addresses 0000 0000h to 0007 FFFFh)

55.14 Reading the Flash Memory

55.14.1 Reading the Code Flash Memory

No special settings are required to read the code flash memory in Normal mode. Data can be read through access to addresses in the code flash memory. Values read from code flash memory that was erased but not yet reprogrammed, such as code flash memory in the non-programmed state, are all read as 1s.

55.14.2 Reading the Data Flash Memory

No special settings are required to read the data flash memory in Normal mode. Data can be read through access to addresses in the data flash memory. Values read from data flash memory that was erased but not yet reprogrammed again, such as data flash memory in the non-programmed state, are undefined. Use blank checking to confirm that an area is in the non-programmed state.

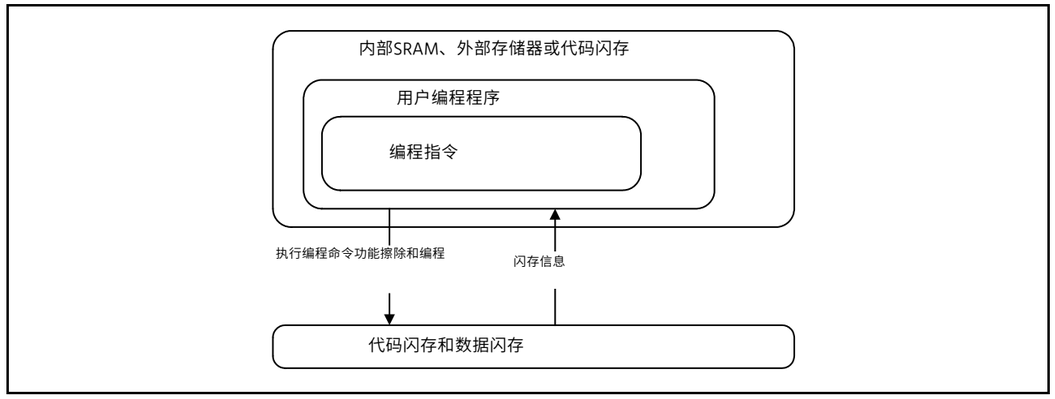


Figure 55.15 自编程示意图

55.13.2 后台操作

当用于写入和读取的闪存组合是表55.11中列出的任何一种时，可以使用后台操作。

Table 55.11 后台操作可用的条件

Product	书写范围	读取范围
所有产品	数据闪存	代码闪存
	代码闪存	数据闪存
2-MB products	代码闪存用户区的前半部分(1MB)（地址00000000h到000FFFFFh）	代码闪存用户区的后半部分(1MB)（地址00100000h到001FFFFFh）
	代码闪存用户区的后半部分(1MB)（地址00100000h到001FFFFFh）	代码闪存用户区的前半部分(1MB)（地址00000000h到000FFFFFh）
1-MB products	代码闪存用户区的前半部分(0.5MB)（地址00000000h到0007FFFFh）	代码闪存用户区的后半部分(0.5MB)（地址00080000h到000FFFFFh）
	代码闪存用户区的后半部分(0.5MB)（地址00080000h到000FFFFFh）	代码闪存用户区的前半部分(0.5MB)（地址00000000h到0007FFFFh）

55.14 读取闪存

55.14.1 读取代码闪存

在正常模式下读取代码闪存不需要特殊设置。可以通过访问代码闪存中的地址来读取数据。从已擦除但尚未重新编程的代码闪存中读取的值，例如处于未编程状态的代码闪存，都被读取为1。

55.14.2 读取数据闪存

在正常模式下读取数据闪存不需要特殊设置。可以通过访问数据闪存中的地址来读取数据。从已擦除但尚未再次重新编程的数据闪存中读取的值（例如处于未编程状态的数据闪存）是未定义的。使用空白检查来确认某个区域处于非编程状态。

55.15 Usage Notes

55.15.1 Reading Areas Where Programming or Erasure Was Interrupted

When programming or erasure of an area of flash memory is interrupted, the data stored in the area become undefined. To avoid reading undefined data, which can be a source of faulty operation, do not fetch instructions or read data from areas where programming or erasure was interrupted.

55.15.2 Constraint on Additional Writes

Other than the configuration area, no other area can be written to twice. After a write to a flash memory area is complete, erase the area before attempting to overwrite data in that area. The configuration area can be overwritten.

55.15.3 Resets during Programming and Erasure

After a reset triggered by a signal assertion on the RES pin during programming and erasure, wait for tRESW until the operating voltage is within the range stipulated in the electrical characteristics before releasing the device from the reset state. For details on tRESW, see section 60.3.3, Reset Timing.

55.15.4 Allocation of Vectors for Interrupts and Other Exceptions during Programming and Erasure

Generation of an interrupt or other exception during programming or erasure might lead to fetching of the vector from the code flash memory. If the vector allocation does not satisfy the conditions for using background operation, set the address for vector fetching to an address that is not in the code flash memory.

55.15.5 Constraints during Programming and Erasure

During programming and erasure, do not:

- Permit the operating voltage from the power supply to go beyond the allowed range
- Change the frequency of the peripheral clock.

55.15.6 Abnormal Termination of Programming and Erasure

When programming or erasure ends abnormally because of the generation of a reset by the RES pin, the programming or erasure state of the flash memory with undefined data cannot be verified or checked. For the area where programming or erasure ends abnormally, the blank check function cannot determine whether the area was erased successfully. Erase the area again to ensure that the corresponding area is completely erased before use.

55.15 使用说明

55.15.1 编程或擦除被中断的阅读区域

当闪存区域的编程或擦除被中断时，存储在该区域中的数据变得不确定。为避免读取可能导致错误操作的未定义数据，请勿从编程或擦除中断的区域获取指令或读取数据。

55.15.2 额外写入的限制

除配置区域外，其他区域不能写入两次。对闪存区域的写入完成后，请先擦除该区域，然后再尝试覆盖该区域中的数据。配置区域可以被覆盖。

55.15.3 编程和擦除期间的复位

在编程和擦除过程中由RES引脚上的信号断言触发复位后，等待tRESW直到工作电压在电气特性规定的范围内，然后再将器件从复位状态释放。有关tRESW的详细信息，请参见第60.3.3节，复位时序。

55.15.4 在编程和擦除期间为中断和其他异常分配向量

在编程或擦除期间产生中断或其他异常可能会导致从代码闪存中获取向量。如果向量分配不满足使用后台操作的条件，则将取向量的地址设置为不在代码闪存中的地址。

55.15.5 编程和擦除期间的约束

在编程和擦除期间，不要：

- 允许来自电源的工作电压超出允许范围
- 改变外设时钟的频率。

55.15.6 烧写异常终止和擦除

当由于RES引脚产生复位而导致编程或擦除异常结束时，无法验证或检查具有未定义数据的闪存的编程或擦除状态。对于编程或擦除异常结束的区域，空白检查功能无法确定该区域是否擦除成功。再次擦除该区域，以确保在使用前将相应区域完全擦除。

56. 2D Drawing Engine (DRW)

56.1 Overview

The 2D Drawing Engine (DRW) provides flexible functions that can support almost any object geometry, rather than being bound to only a few specific geometries such as lines, triangles, or circles. The edges of every object can be independently blurred or anti-aliased.

Rasterization is executed on the bounding box of the object from left to right and top to bottom, and performed one pixel per clock. The 2D Drawing Engine can also raster from bottom to top in certain cases, to optimize the performance. In addition, optimization methods are provided to avoid rasterization of many empty pixels of the bounding box.

The distances to the edges of the object are calculated by a set of edge equations for every pixel of the bounding box. These edge equations can be combined to describe the entire object. If a pixel is inside the object, it is selected for rendering, and if it is outside it is discarded. If it is on the edge, an alpha value can be chosen proportional to the distance of the pixel to the nearest edge for anti-aliasing. Every pixel that is selected for rendering can be textured. The resulting aRGB quadruple can be modified by a general raster operation approach independently for each of the four channels. The aRGB quadruples can then be blended with one of the multiple blend modes of the module.

The 2D Drawing Engine provides two inputs (texture read and framebuffer read) and one output (framebuffer write). The internal color format is always aRGB (8888). The color formats from the inputs are converted to the internal format on read and converted back on write.

Figure 56.1 shows examples of objects that can be drawn in hardware with the 2D Drawing Engine, Figure 56.2 shows a simplified rendering pipeline setup, and Figure 56.3 shows a block diagram of the module.

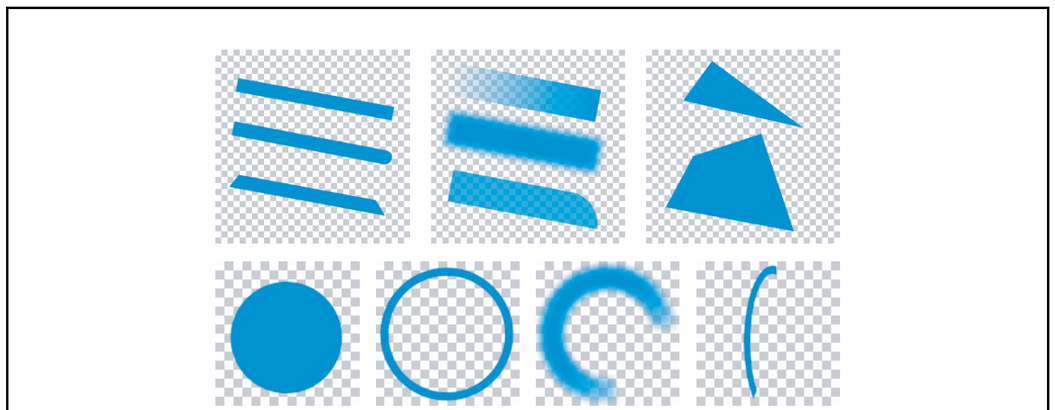


Figure 56.1 Examples of drawing objects

The 2D Drawing Engine also supports a display list mode, which makes it possible to decouple the CPU and graphics controller efficiently and perform rendering in parallel with other CPU activities.

56. 2D绘图引擎(DRW)

56.1 Overview

2D绘图引擎(DRW)提供了灵活的功能，可以支持几乎任何对象几何图形，而不是仅绑定到几个特定的 几何图形，例如线条、三角形或圆形。每个对象的边缘都可以独立模糊或消除锯齿。

光栅化是在物体的边界框上从左到右、从上到下执行的，每个时钟执行一个像素。在某些情况下，2D绘图引擎还可以从下到上进行光栅化，以优化性能。此外，还提供了优化方法来避免边界框的许多空像素的光栅化。

到对象边缘的距离由边界框的每个像素的一组边缘方程计算。
这些边缘方程可以组合起来描述整个物体。如果像素在对象内部，则选择它进行渲染，如果在对象外部，则将其丢弃。如果它在边缘，则可以选择与像素到最近边缘的距离成比例的alpha值以进行抗锯齿。每个被选择用于渲染的像素都可以被纹理化。可以通过通用光栅操作方法对四个通道中的每一个独立地修改得到的aRGB四元组。然后可以将aRGB四元组与模块的多种混合模式之一混合。

2D绘图引擎提供两个输入（纹理读取和帧缓冲区读取）和一个输出（帧缓冲区写入）。内部颜色格式始终为aRGB(8888)。来自输入的颜色格式在读取时转换为内部格式，并在写入时转换回内部格式。

图56.1显示了可以使用2D绘图引擎在硬件中绘制的对象示例，图56.2显示了简化的渲染管道设置，图56.3显示了模块的框图。

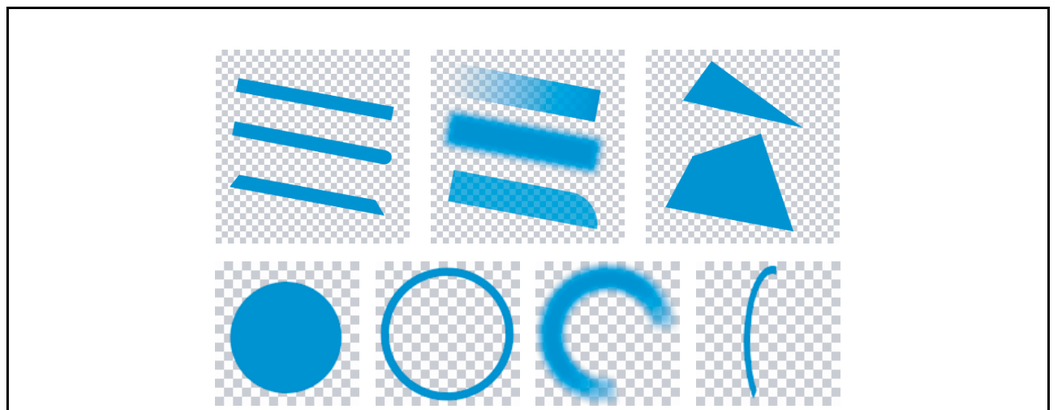


Figure 56.1 绘图对象示例

2D绘图引擎还支持显示列表模式，可以有效地解耦CPU和图形控制器，并与其他CPU活动并行执行渲染。

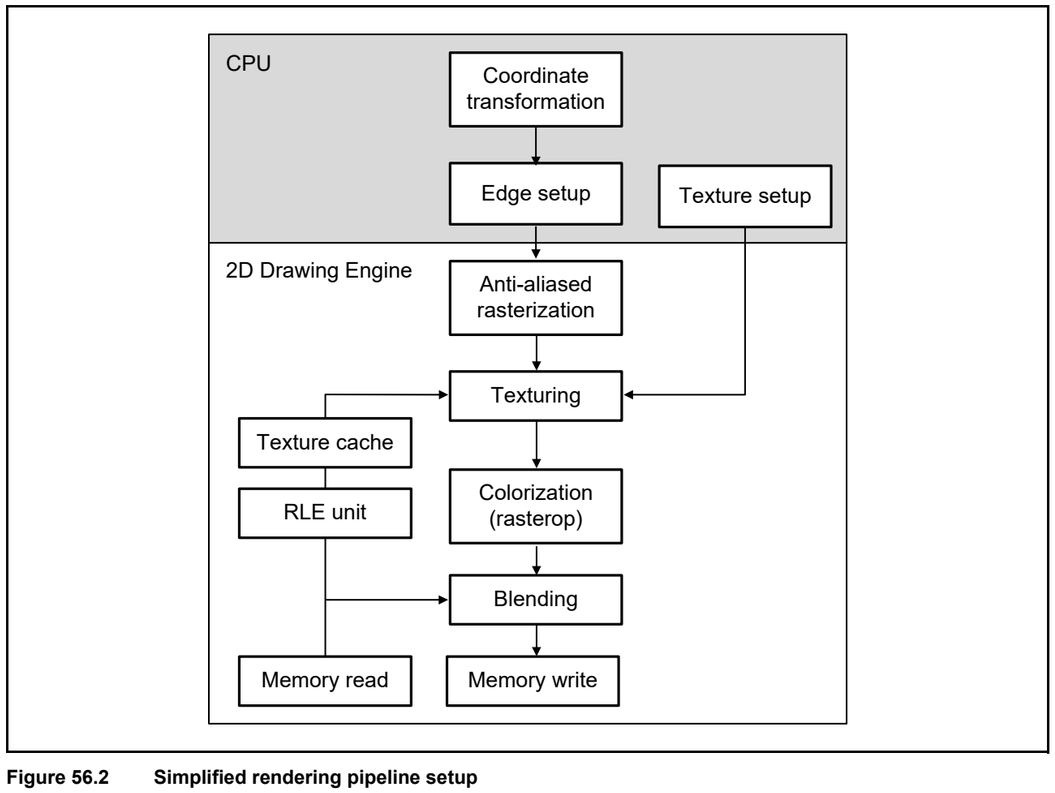


Figure 56.2 Simplified rendering pipeline setup

Note: When using the DRW, set the clock to ICLK = PCLKA.

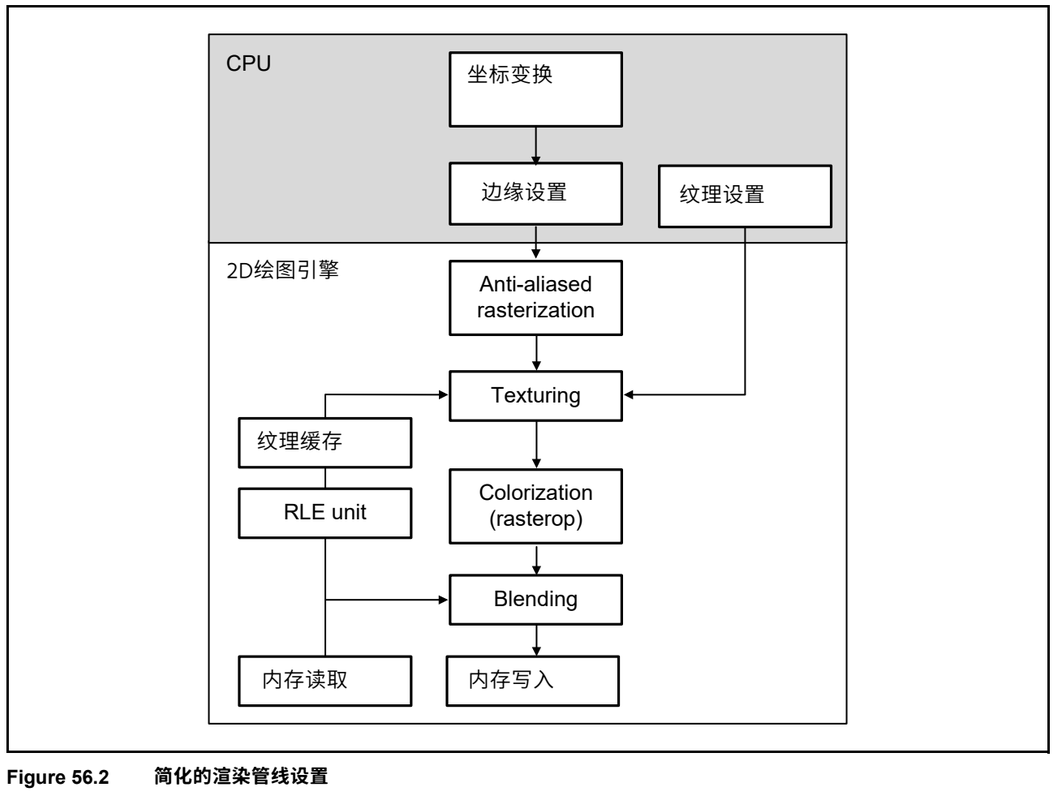


Figure 56.2 简化的渲染管线设置

Note: 使用DRW时，将时钟设置为ICLK=PCLKA。

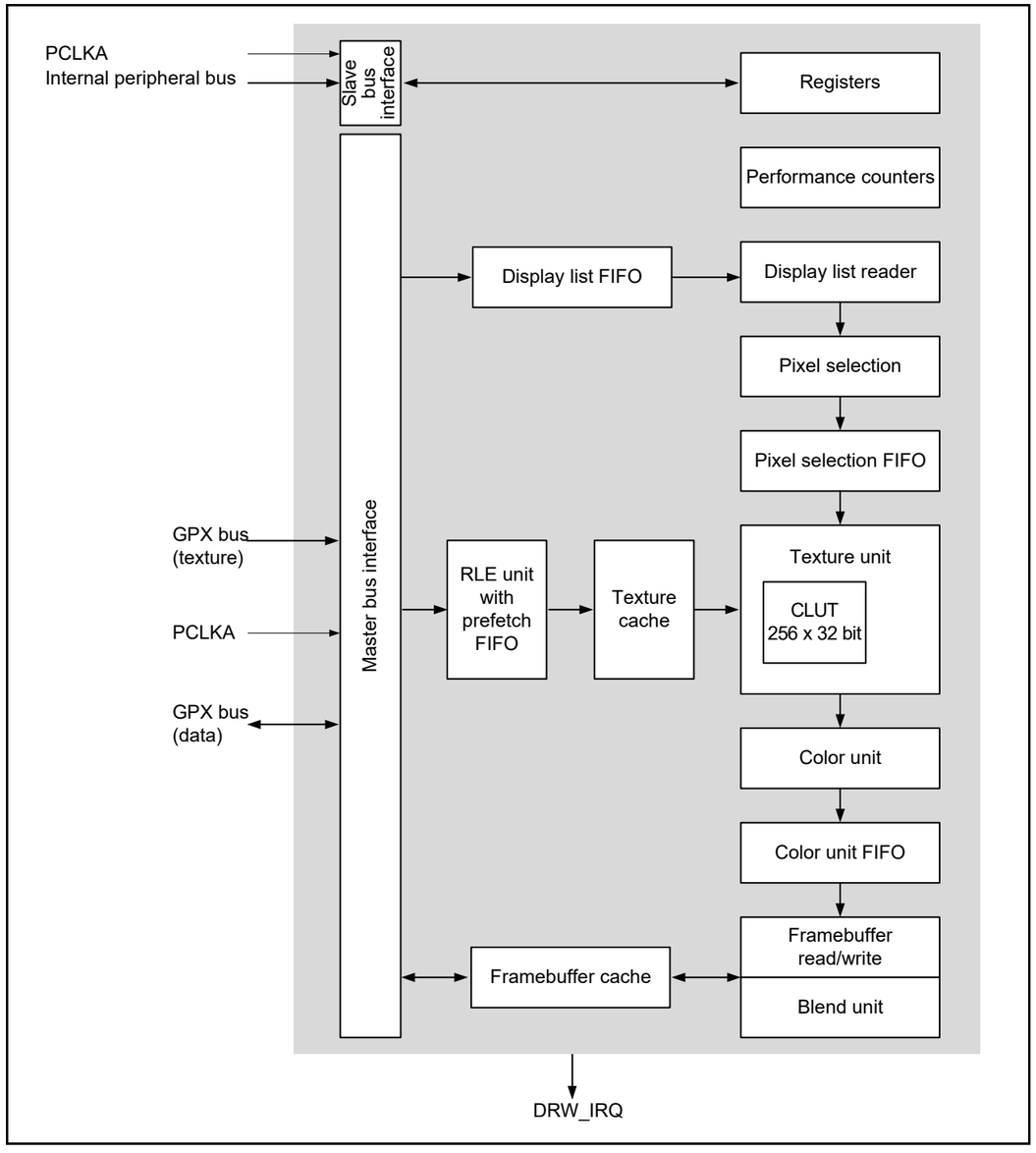


Figure 56.3 Block diagram of the 2D Drawing Engine

The 2D Drawing Engine accesses the GPX bus as bus master through separate caches for:

- Reading and writing pixel data from and to the framebuffer
- Reading textures
- Reading display lists.

The control registers are accessed through the internal peripheral bus interface.

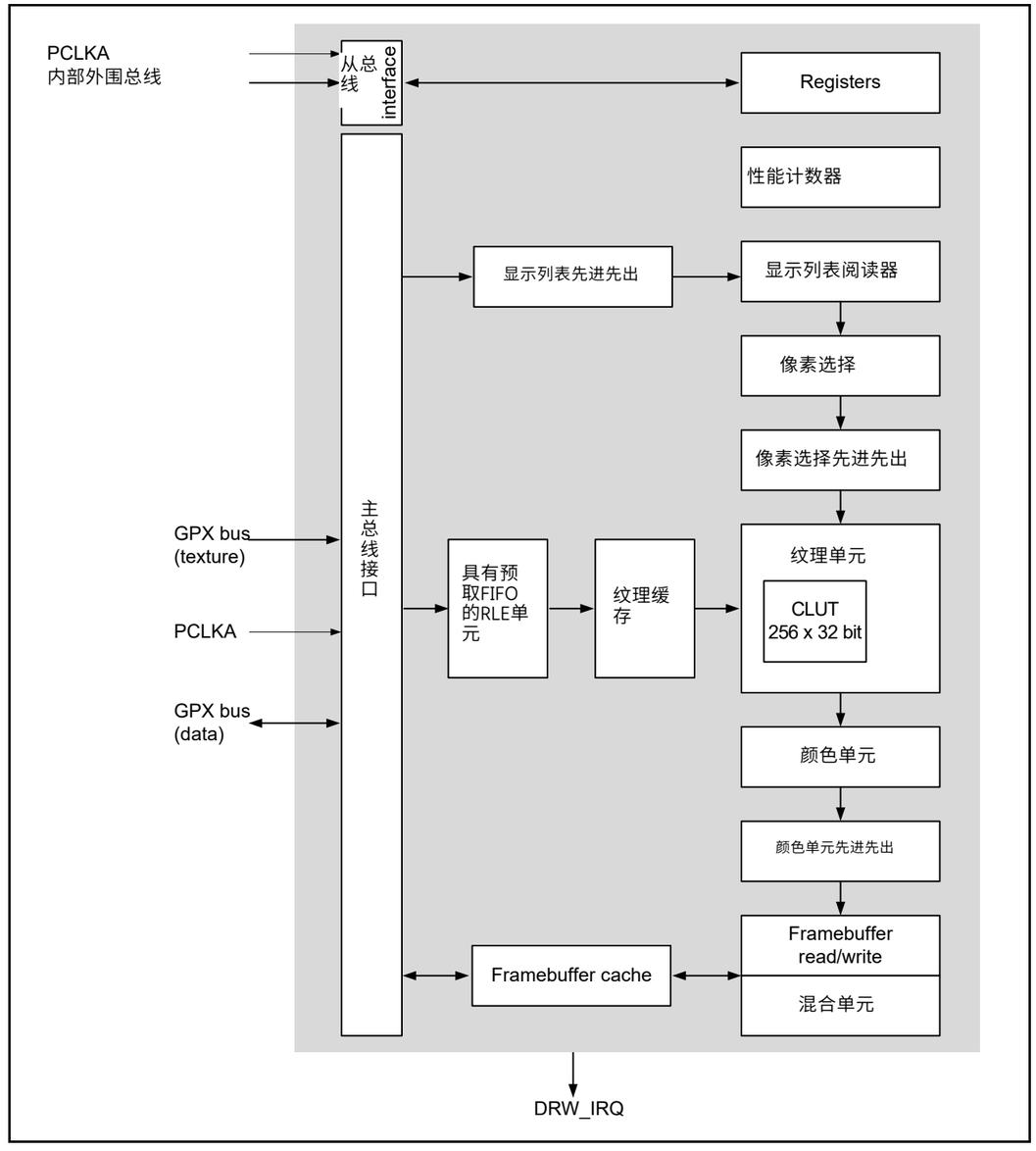


Figure 56.3 二维绘图引擎的框图

2D绘图引擎通过单独的高速缓存作为总线主控器访问GPX总线：

- 从帧缓冲区读取像素数据和向帧缓冲区写入像素数据
- 阅读纹理
- 阅读显示列表。

控制寄存器通过内部外围总线接口访问。

56.2 Register Descriptions

56.2.1 Geometry Control Register (CONTROL)

Address(es): DRW.CONTROL 400E 4000h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	SPAN STORE	SPAN ABORT	UNION CD	UNION AB	UNION 56	UNION 34	UNION 12	BAND2 ENABL
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BAND1 ENABL	LIM6 THRES	LIM5 THRES	LIM4 THRES	LIM3 THRES	LIM2 THRES	LIM1 THRES	QUAD3 ENABL	QUAD2 ENABL	QUAD1 ENABL	LIM6 ENABL	LIM5 ENABL	LIM4 ENABL	LIM3 ENABL	LIM2 ENABL	LIM1 ENABL
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	LIM1 ENABLE	Enable Limiter 1	0: Disable 1: Enable.	W
b1	LIM2 ENABLE	Enable Limiter 2	0: Disable 1: Enable.	W
b2	LIM3 ENABLE	Enable Limiter 3	0: Disable 1: Enable.	W
b3	LIM4 ENABLE	Enable Limiter 4	0: Disable 1: Enable.	W
b4	LIM5 ENABLE	Enable Limiter 5	0: Disable 1: Enable.	W
b5	LIM6 ENABLE	Enable Limiter 6	0: Disable 1: Enable.	W
b6	QUAD1 ENABLE	Enable Quadratic Coupling of Limiters 1 and 2	0: Disable 1: Enable.	W
b7	QUAD2 ENABLE	Enable Quadratic Coupling of Limiters 3 and 4	0: Disable 1: Enable.	W
b8	QUAD3 ENABLE	Enable Quadratic Coupling of Limiters 5 and 6	0: Disable 1: Enable.	W
b9	LIM1 THRESHOLD	Enable Limiter 1 Threshold Mode	0: Disable 1: Enable.	W
b10	LIM2 THRESHOLD	Enable Limiter 2 Threshold Mode	0: Disable 1: Enable.	W
b11	LIM3 THRESHOLD	Enable Limiter 3 Threshold Mode	0: Disable 1: Enable.	W
b12	LIM4 THRESHOLD	Enable Limiter 4 Threshold Mode	0: Disable 1: Enable.	W
b13	LIM5 THRESHOLD	Enable Limiter 5 Threshold Mode	0: Disable 1: Enable.	W
b14	LIM6 THRESHOLD	Enable Limiter 6 Threshold Mode	0: Disable 1: Enable.	W
b15	BAND1 ENABLE	Enable Band Post Process for Limiter 1	0: Disable 1: Enable. (See LnBAND.)	W
b16	BAND2 ENABLE	Enable Band Post Process for Limiter 2	0: Disable 1: Enable. (See LnBAND.)	W
b17	UNION12	Combine Limiter 1 and 2 as Union	0: Select minimum/intersect between limiters 1 and 2 1: Select maximum/union between limiters 1 and 2. (Output is called A.)	W

56.2 注册说明

56.2.1 几何控制寄存器(CONTROL)

Address(es): DRW.CONTROL 400E 4000h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	跨度商店	跨度中止	UNION CD	UNION AB	UNION 56	UNION 34	UNION 12	BAND2 ENABL
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BAND1 ENABL	LIM6 THRES	LIM5 THRES	LIM4 THRES	LIM3 THRES	LIM2 THRES	LIM1 THRES	QUAD3 ENABL	QUAD2 ENABL	QUAD1 ENABL	LIM6 ENABL	LIM5 ENABL	LIM4 ENABL	LIM3 ENABL	LIM2 ENABL	LIM1 ENABL
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	LIM1 ENABLE	启用限制器1	0：禁用1 ：启用。	W
b1	LIM2 ENABLE	启用限制器2	0：禁用1 ：启用。	W
b2	LIM3 ENABLE	启用限制器3	0：禁用1 ：启用。	W
b3	LIM4 ENABLE	启用限制器4	0：禁用1 ：启用。	W
b4	LIM5 ENABLE	启用限制器5	0：禁用1 ：启用。	W
b5	LIM6 ENABLE	启用限制器6	0：禁用1 ：启用。	W
b6	QUAD1 ENABLE	启用二次耦合 限制器1和2	0：禁用1 ：启用。	W
b7	QUAD2 ENABLE	启用二次耦合 限制器3和4	0：禁用1 ：启用。	W
b8	QUAD3 ENABLE	启用二次耦合 限制器5和6	0：禁用1 ：启用。	W
b9	LIM1 THRESHOLD	启用限制器1阈值 Mode	0：禁用1 ：启用。	W
b10	LIM2 THRESHOLD	启用限制器2阈值 Mode	0：禁用1 ：启用。	W
b11	LIM3 THRESHOLD	启用限制器3阈值 Mode	0：禁用1 ：启用。	W
b12	LIM4 THRESHOLD	启用限制器4阈值 Mode	0：禁用1 ：启用。	W
b13	LIM5 THRESHOLD	启用限制器5阈值 Mode	0：禁用1 ：启用。	W
b14	LIM6 THRESHOLD	启用限制器6阈值 Mode	0：禁用1 ：启用。	W
b15	BAND1 ENABLE	启用带后处理 Limiter 1	0：禁用1：启用。（参见LnBAND。）	W
b16	BAND2 ENABLE	启用带后处理 Limiter 2	0：禁用1：启用。（参见LnBAND。）	W
b17	UNION12	将限制器1和2组合为 Union	0：选择限制器1和2之间的最小交集1：选择限制器1和2之间的最大并集。（输出称为A。）	W

Bit	Symbol	Bit name	Description	R/W
b18	UNION34	Combine Limiter 3 & 4 as Union	0: Select minimum/intersect between limiters 3 and 4 1: Select maximum/union between limiters 3 and 4. (Output is called B.)	W
b19	UNION56	Combine Limiter 5 & 6 as Union	0: Select minimum/intersect between limiters 5 and 6 1: Select maximum/union between limiters 5 and 6. (Output is called D.)	W
b20	UNIONAB	Combine Outputs A & B as union	0: Select minimum/intersect between limiters A and B 1: Select maximum/union between limiters A and B. (Output is called C.)	W
b21	UNIONCD	Combine Outputs C & D as Union	0: Select minimum/intersect between limiters C and D 1: Select maximum/union between limiters C and D. (Output is final.)	W
b22	SPANABORT	Spanabort	0: Disable 1: Enable. Shape is horizontally convex, only a single span per scan line. See Spanabortin 56.6.2.6.	W
b23	SPANSTORE	Spanstore	0: Disable 1: Enable. Next line span start is always equal to or left of current-line span start. See Spanstore in 56.6.2.6.	W
b31 to b24	—	Reserved	The write value should be 0.	W

56.2.2 Surface Control Register (CONTROL2)

Address(es): DRW.CONTROL2 400E 4004h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	RLEPIXEL WIDTH[1:0]		BDIA	BSIA	CLUT FORM	COLKEY	CLUT ENABL	RLE ENABL	WRITEALPHA[1:0]		WRITEFORMAT [1:0]		READFORMAT [1:0]		TEXTURE	TEXTURE
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TEXTURE	TEXTURE	BC2	BDI	BSI	BDF	BSF	WRITE FORMAT 2	BDFA	BSFA	READ FORMAT[3:2]		USEACB	PATTERN	TEXTURE	PATTERN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit	Symbol	Bit name	Description	R/W
b0	PATTERN ENABLE	Pattern Color Enable for Pixel Source	Pixel source is a pattern color (blend of COLOR1 and COLOR2 depending on PATTERN and pattern index). 0: Disable pattern 1: Enable pattern. When patterns are used to fill a primitive an index into the pattern bit mask is generated for each pixel with the U limiter. Depending on the pattern bits the color is selected from COLOR1 and COLOR2 registers. Fractional indices can be interpolated between those two values by using TEXTUREFILTERX = 1. The pattern can be wrapped by using TEXTURECLAMPX = 0, and the mask must be set in the TEXMASK register using the mask for u.	W
b1	TEXTURE ENABLE	Texture Enable for Pixel Source	Pixel source is read from texture and used as an alpha to blend between COLOR1 and COLOR2. 0: Disable texture 1: Enable texture.	W
b2	PATTERN SOURCEL5	Limiter 5 Enable for Pattern Index	Limiter 5 is used as pattern index instead of the default U limiter. Limiter 5 can be combined with limiter 6 to form a quadratic limiter that can be used to make quadratic pattern functions to draw radial patterns.	W
b3	USEACB	Alpha Blend Mode	0: Use WRITEALPHA[1:0] mode 1: Use full alpha channel blending mode.	W

Bit	Symbol	位名称	Description	R/W
b18	UNION34	将限制器3和4组合为Union	0：选择限制器3和4之间的最小交集1：选择限制器3和4之间的最大并集。（输出称为B。）	W
b19	UNION56	将限制器5和6组合为Union	0：选择限制器5和6之间的最小交集1：选择限制器5和6之间的最大并集。（输出称为D。）	W
b20	UNIONAB	将输出A和B合并为并集	0：选择限制器A和B之间的最小交集1：选择限制器A和B之间的最大并集。（输出称为C。）	W
b21	UNIONCD	将输出C和D合并为Union	0：选择限制器C和D之间的最小相交1：选择限制器C和D之间的最大并集。（输出为最终值。）	W
b22	SPANABORT	Spanabort	0：禁用1：启用。形状是水平凸的，每条扫描线只有一个跨度。参见56.6.2.6中的Spanabort。	W
b23	SPANSTORE	Spanstore	0：禁用1：启用。下一行跨度开始始终等于或位于当前行跨度开始的左侧。请参阅56.6.2.6中的Spanstore。	W
b31 to b24	—	Reserved	写入值应为0。	W

56.2.2 表面控制寄存器(CONTROL2)

Address(es): DRW.CONTROL2 400E 4004h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	RLEPIXEL WIDTH[1:0]		BDIA	BSIA	CLUT FORM	COLKEY	CLUT ENABL	RLE ENABL	WRITEALPHA[1:0]		WRITEFORMAT [1:0]		READFORMAT [1:0]		TEXTURE	TEXTURE
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TEXTURE	TEXTURE	BC2	BDI	BSI	BDF	BSF	写入格式	BDFA	BSFA	READ FORMAT[3:2]		USEACB	PATTERN	TEXTURE	PATTERN
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

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Bit	Symbol	位名称	Description	R/W
b0	PATTERN ENABLE	为像素源启用图案颜色	像素源是一种图案颜色（COLOR1和COLOR2的混合取决于PATTERN和图案索引）。0：禁用模式1：启用模式。当使用模式填充图元时，使用U限制器为每个像素生成模式位掩码的索引。根据模式位，从COLOR1和COLOR2寄存器中选择颜色。使用TEXTUREFILTERX=1可以在这两个值之间插入小数索引。使用TEXTURECLAMPX=0可以包装模式，并且必须使用u的掩码在TEXMASK寄存器中设置掩码。	W
b1	TEXTURE ENABLE	纹理启用像素源	像素源从纹理中读取并用作alpha以在COLOR1和COLOR2之间混合。0：禁用纹理1：启用纹理。	W
b2	PATTERN SOURCEL5	限制器5启用模式索引	限制器5用作模式索引，而不是默认的U限制器。 限幅器5可与限幅器6组合形成二次限幅器，可用于制作二次图案函数以绘制径向图案。	W
b3	USEACB	阿尔法混合模式	0：使用WRITEALPHA[1:0]模式1：使用全Alpha通道混合模式。	W

Bit	Symbol	Bit name	Description	R/W
b5, b4	READ FORMAT[3:2]	Texture Format Descriptor	Bits [3] and [2] of the texture buffer format. See the detailed description of the READFORMAT[1:0] bit in this section.	W
b6	BSFA	Blend Source Factor for Alpha Channel	Valid in alpha channel blending mode (USEACB = 1). 0: Use 1.0 as blend source factor for alpha channel 1: Use alpha as blend source factor for alpha channel.	W
b7	BDFA	Blend Destination Factor for Alpha Channel	Valid in alpha channel blending mode (USEACB = 1). 0: Use 1.0 as blend destination factor for alpha channel 1: Use alpha as blend destination factor for alpha channel.	W
b8	WRITE FORMAT2	Writeback Framebuffer Format	Bit [2] of framebuffer pixel format. See the description of WRITEFORMAT[1:0] in this section.	W
b9	BSF	Blend Source Factor	Source factor is alpha (factor is 1 per default). 0: Use 1.0 as blend source factor 1: Use alpha as blend source factor.	W
b10	BDF	Blend Destination Factor	Destination factor is alpha (factor is 1 per default). 0: Use 1.0 as blend destination factor 1: Use alpha as blend destination factor.	W
b11	BSI	Blend Source Factor Inverted	Source factor is inverted (meaning 1-a or 1-1 depending on BSF). 0: Use blend factor as specified through BSF 1: Invert blend source factor (1-x).	W
b12	BDI	Blend Destination Factor Inverted	Destination factor is inverted (meaning 1-a or 1-1 depending on BDF). 0: Use blend factor as specified through BDF 1: Invert blend destination factor (1-x).	W
b13	BC2	Blend color 2	Select of blend color 2 instead of framebuffer pixel. 0: Use pixel from framebuffer as destination (DST) 1: Use color 2 as destination (DST).	W
b14	TEXTURE CLAMPX	Calculating U Limiter Outside Used Texture	This bit describes what happens when the U limiter (x direction in texture space) calculates a u value outside of the used texture. 0: Texture wrap mode: Integer part of the calculated value from the U limiter is AND gated with TEXUMASK, resulting in a repetition of texture in the x/u direction 1: Texture clamp mode: Texture color at the border of the texture is taken, resulting in a repetition of texture border color in the x/u direction.	W
b15	TEXTURE CLAMPY	Calculating V Limiter Outside Used Texture	This bit describes what happens when the V limiter (y direction in texture space) calculates a v value outside of the used texture. 0: Texture wrap mode: Integer part of the calculated value from the V limiter is AND gated with TEXVMASK, resulting in a repetition of texture in the y/v direction. 1: Texture clamp mode: Texture color at the border of the texture is taken, resulting in a repetition of texture border color in the y/v direction.	W
b16	TEXTURE FILTERX	Linear Filtering on Texture U Axis	0: No filtering on texture U axis 1: Linear filtering on texture U axis.	W
b17	TEXTURE FILTERY	Linear Filtering on Texture V Axis	0: No filtering on texture V axis 1: Linear filtering on texture V axis.	W
b19, b18	READ FORMAT[1:0]	Texture Format Descriptor	Pixel format of the texture buffer. b5 b4 b19 b18 0 0 0 0: 8 bpp a (8) 0 0 0 1: 16 bpp RGB (565) 0 0 1 0: 32 bpp aRGB (8888) 0 0 1 1: 16 bpp aRGB (4444) 0 1 0 0: 16 bpp aRGB (1555) 0 1 0 1: 8 bpp aCLUT (44), 4 bit alpha and 4 bit indexed color 1 0 0 0: 8 bpp CLUT (8)/I (8), 8 bit indexed color/luminance 1 0 1 0: 4 bpp CLUT (4)/I (4), 4 bit indexed color/luminance 1 0 1 1: 2 bpp CLUT (2)/I (2), 2 bit indexed color/luminance 1 1 0 0: 1 bpp CLUT (1)/I (1), 1 bit indexed color/luminance. Other settings are prohibited.	W

Bit	Symbol	位名称	Description	R/W
b5, b4	READ FORMAT[3:2]	纹理格式 Descriptor	纹理缓冲区格式的位[3]和[2]。请参阅本节中READFORMAT[1:0]位的详细说明。	W
b6	BSFA	Alpha通道的混合源因子	在Alpha通道混合模式下有效(USEACB=1)。0：使用1.0作为Alpha通道的混合源因子1：使用Alpha作为Alpha通道的混合源因子。	W
b7	BDFA	混合目的地Alpha系数 Channel	在Alpha通道混合模式下有效(USEACB=1)。0：使用1.0作为Alpha通道的混合目标因子1：使用Alpha作为Alpha通道的混合目标因子。	W
b8	WRITE FORMAT2	Writeback Framebuffer Format	帧缓冲区像素格式的位[2]。见描述本节中的WRITEFORMAT[1:0]。	W
b9	BSF	混合源因子	源因子为alpha（默认因子为1）。0：使用1.0作为混合源因子1：使用alpha作为混合源因子。	W
b10	BDF	混合目的地 Factor	目标因子为alpha（默认因子为1）。0：使用1.0作为混合目标因子1：使用alpha作为混合目标因子。	W
b11	BSI	混合源因子 Inverted	源因子是倒置的（根据BSF表示1-a或1-1）。0：使用通过BSF指定的混合因子1：反转混合源因子(1-x)。	W
b12	BDI	混合目的地因子倒置	目标因子是倒置的（根据BDF表示1-a或1-1）。0：使用通过BDF指定的混合因子1：反转混合目标因子(1-x)。	W
b13	BC2	混合颜色2	选择混合颜色2而不是帧缓冲区像素。0：使用来自帧缓冲区的像素作为目标(DST)1：使用颜色2作为目标(DST)。	W
b14	TEXTURE CLAMPX	计算使用纹理外的U限制器	该位描述了当U限制器（纹理空间中的x方向）在使用的纹理之外计算u值时会发生什么。0：Texturewrap模式：U限制器的计算值的整数部分与TEXUMASK进行与门，导致xu方向重复纹理1：Textureclamp模式：取纹理边界处的纹理颜色，结果在xu方向重复纹理边框颜色。	W
b15	TEXTURE CLAMPY	计算使用纹理外部的V限制器	该位描述了当V限制器（纹理空间中的y方向）在使用的纹理之外计算v值时会发生什么。0：纹理环绕模式：从V限制器计算的值的整数部分与TEXVMASK进行与门，导致在yv方向上重复纹理。1：纹理钳制模式：取纹理边界处的纹理颜色，导致yv方向纹理边界颜色重复。	W
b16	TEXTURE FILTERX	线性过滤开启纹理U轴	0：在纹理U轴上不进行过滤1：在纹理U轴上进行线性过滤。	W
b17	TEXTURE FILTERY	线性过滤开启纹理V轴	0：纹理V轴无过滤1：纹理V轴线性过滤。	W
b19, b18	READ FORMAT[1:0]	纹理格式 Descriptor	纹理缓冲区的像素格式。b5b4b19b180000：8bppa(8)0001：16bppRGB(565)0010：32bppaRGB(8888)0011：16bppaRGB(4444)0100：16bppaRGB(1555)0101：8bppaCLUT(44)，4位alpha和4位索引颜色1001：8bppCLUT(8)I(8)，8位索引颜色亮度1010：4bppCLUT(4)I(4)，4位索引颜色亮度1011：2bppCLUT(2)I(2)，2位索引颜色亮度1100：1bppCLUT(1)I(1)，1位索引色亮度。禁止其他设置。	W

Bit	Symbol	Bit name	Description	R/W
b21, b20	WRITE FORMAT[1:0]	Writeback Framebuffer Format	Pixel format of the framebuffer. b8 b21 b20 0 0 0: 8 bpp a (8) 0 0 1: 16 bpp RGB (565) 0 1 0: 32 bpp aRGB (8888) 0 1 1: 16 bpp aRGB (4444). Other settings are prohibited.	W
b23, b22	WRITE ALPHA[1:0]	Writeback Alpha Source for Framebuffer	• In non-alpha channel blending mode (USEACB = 0): Sets the alpha source for the framebuffer. b23 b22 0 0: Use alpha from color 2 0 1: Use source alpha (pixel coverage) 1 0: Use 0.0 as alpha 1 1: Use alpha from framebuffer. • In alpha channel blending mode (USEACB = 1): Blends alpha in color 2 instead of framebuffer alpha. 00b: BC2A = 1: Use alpha in color 2 as destination (DST_A) else: BC2A = 0: Use alpha from framebuffer as destination (DST_A).	W
b24	RLE ENABLE	RLE Enable	0: Disable RLE 1: Enable RLE.	W
b25	CLUT ENABLE	CLUT Enable	0: Disable CLUT 1: Enable CLUT. If CLUTENABLE = 0 (CLUT disabled), the index is directly put on the RGB channels.	W
b26	COLKEY ENABLE	Color Keying Enable	0: Disable color keying 1: Enable color keying.	W
b27	CLUT FORMAT	CLUT Format	0: Format CLUT as aRGB (8888) 1: Format CLUT as RGB (565).	W
b28	BSIA	Blend Source Factor Inverted in Alpha Channel	• In alpha channel blending mode (USEACB = 1): 0: Use blend factor as specified through BSFA 1: Invert blend source factor (1-x).	W
b29	BDIA	Blend Destination Factor Inverted in Alpha Channel	• In alpha channel blending mode (USEACB = 1): 0: Use blend factor as specified through BDFA 1: Invert destination blend factor (1-x).	W
b31, 30	RLE PIXEL WIDTH[1:0]	Texel Width for RLE Unit	b31 b30 0 0: 1 byte per texel 0 1: 2 bytes per texel 1 0: 3 bytes per texel 1 1: 4 bytes per texel.	W

56.2.3 Interrupt Control Register (IRQCTL)

Address(es): DRW.IRQCTL 400E 40C0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	BUSIRQCLR	BUSIRQEN	DLISTIRQCLR	ENUMIRQCLR	DLISTIRQEN	ENUMIRQEN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	ENUMIRQEN	ENUMIRQ Interrupt Mask Enable	0: Disable (mask) ENUMIRQ enumeration interrupt 1: Enable (unmask) ENUMIRQ enumeration interrupt.	W
b1	DLISTIRQEN	DLISTIRQ Interrupt Mask Enable	0: Disable (mask) DLISTIRQ display list interrupt 1: Enable (unmask) DLISTIRQ display list interrupt.	W

Bit	Symbol	位名称	Description	R/W
b21, b20	WRITE FORMAT[1:0]	Writeback Framebuffer Format	帧缓冲区的像素格式。b8b21b20000：8bppa(8)001：16bppRGB(565)010：32bppaRGB(8888)011：16bppaRGB(4444)。 禁止其他设置。	W
b23, b22	WRITE ALPHA[1:0]	Writeback Alpha 帧缓冲区的来源	在非Alpha通道混合模式下(USEACB=0)：设置帧缓冲区的Alpha源。b23b2200：使用颜色2中的alpha01：使用源alpha（像素覆盖）10：使用0.0作为alpha11：使用帧缓冲区中的alpha。 在Alpha通道混合模式中(USEACB=1)：混合颜色2中的Alpha，而不是帧缓冲区Alpha。00b:BC2A=1:使用颜色2中的alpha作为目标(DST_A)else:BC2A=0:使用来自帧缓冲区的alpha作为目标(DST_A)。	W
b24	RLE ENABLE	RLE Enable	0：禁用RLE1： 启用RLE。	W
b25	CLUT ENABLE	CLUT Enable	0：禁用CLUT1：启用CLUT。如果CLUTENABLE=0（CLUT禁用），则直接将索引放在 RGB channels.	W
b26	COLKEY ENABLE	颜色键控启用	0：禁用颜色键控1： 启用颜色键控。	W
b27	CLUT FORMAT	CLUT Format	0：将CLUT格式化为aRGB(8888) 1：将CLUT格式化为RGB(565)。	W
b28	BSIA	混合源因子倒置阿尔法Channel	在Alpha通道混合模式下(USEACB=1)：0：使用通过BSFA指定的混合因子1：反转混合源因子(1-x) 。	W
b29	BDIA	混合目标因子倒置 阿尔法通道	在Alpha通道混合模式下(USEACB=1)：0：使用通过BDFA指定的混合因子1：反转目标混合因子(1-x)。	W
b31, 30	RLE PIXEL WIDTH[1:0]	RLE的纹素宽度Unit	b31b3000：每纹素1字节01：每纹素2字节10：每纹素3字节11：每纹素4字节。	W

56.2.3 中断控制寄存器(IRQCTL)

Address(es): DRW.IRQCTL 400E 40C0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	BUSIRQCLR	BUSIRQEN	DLISTIRQCLR	ENUMIRQCLR	DLISTIRQEN	ENUMIRQEN
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	ENUMIRQEN	ENUMIRQ中断屏蔽使能	0：禁用（屏蔽）ENUMIRQ枚举中断1：启用（取消屏蔽）ENUMIRQ枚举中断。	W
b1	DLISTIRQEN	DLISTIRQ中断屏蔽使能	0：禁用（屏蔽）DLISTIRQ显示列表中断1：启用（取消屏蔽）DLISTIRQ显示列表中断。	W

Bit	Symbol	Bit name	Description	R/W
b2	ENUMIRQCLR	Clear ENUMIRQ	0: Do not clear ENUMIRQ enumeration interrupt 1: Clear ENUMIRQ enumeration interrupt.	W
b3	DLISTIRQCLR	Clear DLISTIRQ	0: Do not clear DLISTIRQ display list interrupt 1: Clear DLISTIRQ display list interrupt.	W
b4	BUSIRQEN	BUSIRQ Interrupt Mask Enable	0: Disable (mask) BUSIRQ bus error interrupt 1: Enable (unmask) BUSIRQ bus error interrupt.	W
b5	BUSIRQCLR	Clear BUSIRQ	0: Do not clear BUSIRQ bus error interrupt 1: Clear BUSIRQ bus error interrupt.	W
b31 to b6	—	Reserved	The write value should be 0.	W

56.2.4 Cache Control Register (CACHECTL)

Address(es): DRW.CACHECTL 400E 40C4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	CFLUSHTX	CENABLETX	CFLUSHFX	CENABLEFX
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	CENABLEFX	Framebuffer Cache Enable	0: Disable the framebuffer cache 1: Enable the framebuffer cache.	W
b1	CFLUSHFX	Flush Framebuffer Cache	0: Do not flush the framebuffer cache 1: Flush the framebuffer cache.	W
b2	CENABLETX	Texture Cache Enable	0: Disable the texture cache 1: Enable the texture cache.	W
b3	CFLUSHTX	Flush Texture Cache	0: Do not flush the texture cache 1: Flush the texture cache.	W
b31 to b4	—	Reserved	The write value should be 0.	W

56.2.5 Status Control Register (STATUS)

Address(es): DRW.STATUS 400E 4000h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	BUSERRMDL	BUSERRMTX	BUSERRMFB	—	BUSIRQ	DLISTIRQ	ENUMIRQ	DLISTACTIVE	CACHEDIRTY	BUSYWRITE	BUSYENUM
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	BUSY ENUM	Enumeration Unit Status	0: Enumeration unit idle 1: Enumeration unit is busy, new primitive cannot be started.	R

Bit	Symbol	位名称	Description	R/W
b2	ENUMIRQCLR	Clear ENUMIRQ	0：不清除ENUMIRQ枚举中断1：清除ENUMIRQ枚举中断。	W
b3	DLISTIRQCLR	Clear DLISTIRQ	0：不清除DLISTIRQ显示列表中断1：清除DLISTIRQ显示列表中断。	W
b4	BUSIRQEN	BUSIRQ中断屏蔽使能	0：禁用（屏蔽）BUSIRQ总线错误中断1：启用（取消屏蔽）BUSIRQ总线错误中断。	W
b5	BUSIRQCLR	Clear BUSIRQ	0：不清除BUSIRQ总线错误中断1：清除BUSIRQ总线错误中断。	W
b31 to b6	—	Reserved	写入值应为0。	W

56.2.4 高速缓存控制寄存器(CACHECTL)

Address(es): DRW.CACHECTL 400E 40C4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	CFLUSHTX	CENABLETX	CFLUSHFX	CENABLEFX
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	CENABLEFX	帧缓冲缓存启用	0：禁用帧缓冲缓存1：启用帧缓冲缓存。	W
b1	CFLUSHFX	刷新帧缓冲缓存	0：不刷新帧缓冲缓存1：刷新帧缓冲缓存。	W
b2	CENABLETX	纹理缓存启用	0：禁用纹理缓存1：启用纹理缓存。	W
b3	CFLUSHTX	刷新纹理缓存	0：不刷新纹理缓存1：刷新纹理缓存。	W
b31 to b4	—	Reserved	写入值应为0。	W

56.2.5 状态控制寄存器(STATUS)

Address(es): DRW.STATUS 400E 4000h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	BUSERRMDL	BUSERRMTX	BUSERRMFB	—	BUSIRQ	DLISTIRQ	ENUMIRQ	DLISTACTIVE	缓存脏	忙写	BUSYENUM
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	BUSY ENUM	枚举单元状态	0：枚举单元空闲1：枚举单元忙，无法启动新原语。	R

Bit	Symbol	Bit name	Description	R/W
b1	BUSY WRITE	Framebuffer Writeback Status	0: Framebuffer writeback finished 1: Framebuffer writeback busy, framebuffer type cannot be changed.	R
b2	CACHE DIRTY	Framebuffer Cache Status	0: Framebuffer cache is not dirty 1: Framebuffer cache is dirty, and frame should not be flipped.	R
b3	DLIST ACTIVE	Display List Reader Status	0: Display list reader is idle 1: Display list reader is busy, and no direct write access to registers allowed.	R
b4	ENUM IRQ	Enumeration Interrupt Triggered	0: Enumeration not finished or interrupt disabled 1: Enumeration finished interrupt triggered.	R
b5	DLIST IRQ	Display List Interrupt Triggered	0: Display list not finished or interrupt disabled 1: Display list finished interrupt triggered.	R
b6	BUS IRQ	Bus Error Interrupt Triggered	0: No bus error occurred or interrupt disabled 1: Bus error interrupt triggered.	R
b7	—	Reserved	This bit is read as 0.	R
b8	BUSERR MFB	Framebuffer Bus Error Interrupt Triggered	0: No framebuffer bus error occurred or interrupt disabled 1: Framebuffer bus error interrupt triggered.	R
b9	BUSERR MTXMRL	Texture Bus Error Interrupt Triggered*1	0: No texture bus error occurred or interrupt disabled 1: Texture bus error interrupt triggered.	R
b10	BUSERR MDL	Display List Bus Error Interrupt Triggered	0: No display list bus error occurred or interrupt disabled 1: Display list bus error interrupt triggered.	R
b31 to b11	—	Reserved	These bits are read as 0.	R

Note 1. Because the RLE unit is also reading data through the texture bus, an error during RLE data access is also reflected in this bit.

56.2.6 Hardware Version and Feature Set ID Register (HWREVISION)

Address(es): DRW.HWREVISION 400E 4004h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	ACBLEND	—	COLORKEY	TEXCLUT256	RLEUNIT	—	TEXCLU	PERFCOUNT	TXCACHE	FBCACHE	DLR	—
Value after reset:	0	0	0	0	1	1	1	1	1	0	1	1	1	1	1	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	REV[11:0]											
Value after reset:	0	0	0	0	0	0	0	1	0	0	0	0	0	1	1	1

Bit	Symbol	Bit name	Description	R/W
b11 to b0	REV[11:0]	Revision Number	Revision number.	R
b16 to b12	—	Reserved	These bits are read as 0.	R
b17	DLR	Display List Reader Available	Display list reader is available.	R
b18	FBCACHE	Framebuffer Cache Available	Framebuffer cache is available.	R
b19	TX CACHE	Texture Cache Available	Texture cache is available.	R
b20	PERF COUNT	Two Performance Counter Available	Two performance counter is available.	R
b21	TEXCLUT	Texture CLUT Available	Texture CLUT is available.	R
b22	—	Reserved	This bit is read as 0.	R
b23	RLEUNIT	RLE Unit Available	RLE unit is available.	R

Bit	Symbol	位名称	Description	R/W
b1	忙写	Framebuffer Writeback Status	0：Framebufferwriteback完成1：Framebufferwriteback忙，framebuffer类型不能更改。	R
b2	缓存脏	帧缓冲缓存状态	0：Framebuffer缓存不脏1：Framebuffer缓存脏，帧不应该被翻转。	R
b3	DLIST ACTIVE	显示列表阅读器状态	0：显示列表阅读器空闲1：显示列表阅读器忙，不允许直接写访问寄存器。	R
b4	ENUM IRQ	枚举中断触发	0：枚举未完成或中断禁用1：枚举完成中断触发。	R
b5	DLIST IRQ	显示列表中断触发	0：显示列表未完成或中断禁用1：显示列表完成中断触发。	R
b6	BUS IRQ	触发总线错误中断	0：未发生总线错误或中断禁用1：触发了总线错误中断。	R
b7	—	Reserved	该位读为0。	R
b8	BUSERR MFB	帧缓冲总线错误中断 Triggered	0：未发生帧缓冲区总线错误或中断禁用1：已触发帧缓冲区总线错误中断。	R
b9	BUSERR MTXMRL	纹理总线错误中断 Triggered*1	0：未发生纹理总线错误或中断禁用1：已触发纹理总线错误中断。	R
b10	BUSERR MDL	显示列表总线错误中断 Triggered	0：未发生显示列表总线错误或中断禁用1：已触发显示列表总线错误中断。	R
b31 to b11	—	Reserved	这些位读为0。	R

Note 1. 因为RLE单元也是通过纹理总线读取数据，所以RLE数据访问过程中的错误也反映在该位上。

56.2.6 硬件版本和功能集ID寄存器(HWREVISION)

Address(es): DRW.HWREVISION 400E 4004h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	ACBLEND	—	COLORKEY	TEXCLUT256	RLEUNIT	—	TEXCLU	PERFCOUNT	TXCACHE	FBCACHE	DLR	—
重置后的值：	0	0	0	0	1	1	1	1	1	0	1	1	1	1	1	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	REV[11:0]											
重置后的值：	0	0	0	0	0	0	0	1	0	0	0	0	0	1	1	1

Bit	Symbol	位名称	Description	R/W
b11 to b0	REV[11:0]	修订号	修订号。	R
b16 to b12	—	Reserved	这些位读为0。	R
b17	DLR	显示列表阅读器可用	显示列表阅读器可用。	R
b18	FBCACHE	可用的帧缓冲缓存	帧缓冲缓存可用。	R
b19	TX CACHE	可用的纹理缓存	纹理缓存可用。	R
b20	性能计数	两个性能计数器 Available	有两个性能计数器可用。	R
b21	TEXCLUT	可用的纹理CLUT	纹理CLUT可用。	R
b22	—	Reserved	该位读为0。	R
b23	RLEUNIT	可用的RLE单元	RLE单元可用。	R

Bit	Symbol	Bit name	Description	R/W
b24	TEX CLUT256	Texture CLUT with 16 or 256 Entries Available	Texture CLUT with 16 or 256 entries is available.	R
b25	COLORKEY	Color Key Available	Color key is available.	R
b26	—	Reserved	This bit is read as 1.	R
b27	ACBLEND	Alpha Channel Blending Available	Alpha channel blending is available.	R
b31 to b28	—	Reserved	These bits are read as 0.	R

56.2.7 Base Color Register (COLOR1)

Address(es): DRW.COLOR1 400E 4064h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	COLOR1A[7:0]								COLOR1R[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	COLOR1G[7:0]								COLOR1B[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	COLOR1B[7:0]	Blue Channel of Color 1	Specifies blue channel of color 1.	W
b15 to b8	COLOR1G[7:0]	Green Channel of Color 1	Specifies green channel of color 1.	W
b23 to b16	COLOR1R[7:0]	Red Channel of Color 1	Specifies red channel of color 1.	W
b31 to b24	COLOR1A[7:0]	Alpha Channel of Color 1	Specifies alpha channel of color 1. 00h: Transparent ... FFh: Opaque.	W

56.2.8 Secondary Color Register (COLOR2)

Address(es): DRW.COLOR2 400E 4068h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	COLOR2A[7:0]								COLOR2R[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	COLOR2G[7:0]								COLOR2B[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	COLOR2B[7:0]	Blue Channel of Color 2	Specifies blue channel of color 2.	W
b15 to b8	COLOR2G[7:0]	Green Channel of Color 2	Specifies green channel of color 2.	W
b23 to b16	COLOR2R[7:0]	Red Channel of Color 2	Specifies red channel of color 2.	W
b31 to b24	COLOR2A[7:0]	Alpha Channel of Color 2	Specifies alpha channel of color 2. 00h: Transparent ... FFh: Opaque.	W

Bit	Symbol	位名称	Description	R/W
b24	TEX CLUT256	使用16或256的纹理CLUT可用条目	具有16或256个条目的纹理CLUT可用。	R
b25	COLORKEY	颜色键可用	颜色键可用。	R
b26	—	Reserved	该位读为1。	R
b27	ACBLEND	Alpha通道混合 Available	Alpha通道混合可用。	R
b31 to b28	—	Reserved	这些位读为0。	R

56.2.7 基色寄存器(COLOR1)

Address(es): DRW.COLOR1 400E 4064h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	COLOR1A[7:0]								COLOR1R[7:0]							
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	COLOR1G[7:0]								COLOR1B[7:0]							
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b7 to b0	COLOR1B[7:0]	颜色1的蓝色通道	指定颜色1的蓝色通道。	W
b15 to b8	COLOR1G[7:0]	颜色1的绿色通道	指定颜色1的绿色通道。	W
b23 to b16	COLOR1R[7:0]	颜色1的红色通道	指定颜色1的红色通道。	W
b31 to b24	COLOR1A[7:0]	颜色1的Alpha通道	指定颜色1的Alpha通道。00h：透明…FFh：不透明。	W

56.2.8 二级色彩寄存器(COLOR2)

Address(es): DRW.COLOR2 400E 4068h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	COLOR2A[7:0]								COLOR2R[7:0]							
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	COLOR2G[7:0]								COLOR2B[7:0]							
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b7 to b0	COLOR2B[7:0]	颜色2的蓝色通道	指定颜色2的蓝色通道。	W
b15 to b8	COLOR2G[7:0]	颜色2的绿色通道	指定颜色2的绿色通道。	W
b23 to b16	COLOR2R[7:0]	颜色2的红色通道	指定颜色2的红色通道。	W
b31 to b24	COLOR2A[7:0]	颜色2的Alpha通道	指定颜色2的Alpha通道。00h：透明…FFh：不透明。	W

56.2.9 Pattern Register (PATTERN)

Address(es): DRW.PATTERN 400E 4074h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	PATTERN[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	PATTERN[7:0]	Bitmap of the Pattern	Specifies bitmap of the pattern.	W
b31 to b8	—	Reserved	The write value should be 0.	W

56.2.10 Limiter N Start Value Register (LnSTART)

Address(es): DRW.L1START 400E 4010h, DRW.L2START 400E 4014h, DRW.L3START 400E 4018h, DRW.L4START 400E 401Ch, DRW.L5START 400E 4020h, DRW.L6START 400E 4024h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	LSTART[31:16]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	LSTART[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b31 to b0	LSTART[31:0]	Start Value of the nth Limiter	Specifies start value of the nth limiter.	W

56.2.11 Limiter N X-Axis Increment Register (LnXADD)

Address(es): DRW.L1XADD 400E 4028h, DRW.L2XADD 400E 402Ch, DRW.L3XADD 400E 4030h, DRW.L4XADD 400E 4034h, DRW.L5XADD 400E 4038h, DRW.L6XADD 400E 403Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	LXADD[31:16]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	LXADD[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b31 to b0	LXADD[31:0]	X-Axis Increment	Specifies x-axis increment.	W

56.2.9 模式寄存器(PATTERN)

Address(es): DRW.PATTERN 400E 4074h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	PATTERN[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b7 to b0	PATTERN[7:0]	图案的位图	指定图案的位图。	W
b31 to b8	—	Reserved	写入值应为0。	W

56.2.10 限制器N起始值寄存器(LnSTART)

Address(es): DRW.L1START 400E 4010h, DRW.L2START 400E 4014h, DRW.L3START 400E 4018h, DRW.L4START 400E 401Ch, DRW.L5START 400E 4020h, DRW.L6START 400E 4024h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	LSTART[31:16]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	LSTART[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b31 to b0	LSTART[31:0]	第n个限制器的起始值	指定第n个限制器的起始值。	W

56.2.11 限制器NX轴增量寄存器(LnXADD)

Address(es): DRW.L1XADD 400E 4028h, DRW.L2XADD 400E 402Ch, DRW.L3XADD 400E 4030h, DRW.L4XADD 400E 4034h, DRW.L5XADD 400E 4038h, DRW.L6XADD 400E 403Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	LXADD[31:16]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	LXADD[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b31 to b0	LXADD[31:0]	X-Axis Increment	指定x轴增量。	W

56.2.12 Limiter N Y-Axis Increment Register (LnYADD)

Address(es): DRW.L1YADD 400E 4040h, DRW.L2YADD 400E 4044h, DRW.L3YADD 400E 4048h, DRW.L4YADD 400E 404Ch, DRW.L5YADD 400E 4050h, DRW.L6YADD 400E 4054h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	LYADD[31:16]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	LYADD[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b31 to b0	LYADD[31:0]	Y-Axis Increment	Specifies y-axis increment.	W

56.2.13 Limiter M Band Width Parameter Register (LmBAND)

Address(es): DRW.L1BAND 400E 4058h, DRW.L2BAND 400E 405Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	LBAND[31:16]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	LBAND[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b31 to b0	LBAND[31:0]	Limiter m Band Width Parameter	Specifies limiter m band width parameter.	W

56.2.14 Texture Base Address Register (TEXORIGIN)

Address(es): DRW.TEXORIGIN 400E 40BCh

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	TEXORIGIN[31:16]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TEXORIGIN[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b31 to b0	TEXORIGIN[31:0]	Texture Base Address	Specifies texture base address.	W

56.2.12 限制器NY轴增量寄存器(LnYADD)

Address(es): DRW.L1YADD 400E 4040h, DRW.L2YADD 400E 4044h, DRW.L3YADD 400E 4048h, DRW.L4YADD 400E 404Ch, DRW.L5YADD 400E 4050h, DRW.L6YADD 400E 4054h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	LYADD[31:16]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	LYADD[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b31 to b0	LYADD[31:0]	Y-Axis Increment	指定y轴增量。	W

56.2.13 限制器M带宽参数寄存器(LmBAND)

Address(es): DRW.L1BAND 400E 4058h, DRW.L2BAND 400E 405Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	LBAND[31:16]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	LBAND[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b31 to b0	LBAND[31:0]	限制器m带宽参数	指定限制器m带宽参数。	W

56.2.14 纹理基地址寄存器(TEXORIGIN)

Address(es): DRW.TEXORIGIN 400E 40BCh

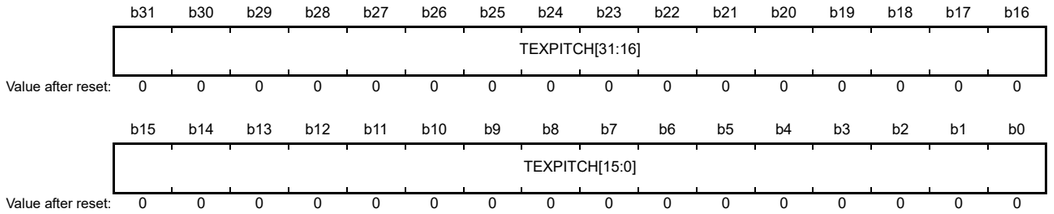
	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	TEXORIGIN[31:16]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TEXORIGIN[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b31 to b0	TEXORIGIN[31:0]	纹理基地址	指定纹理基地址。	W

56.2.15 Texels Per Texture Line Register (TEXPITCH)

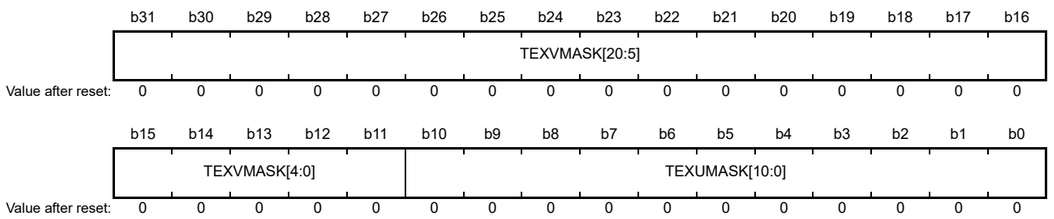
Address(es): DRW.TEXPITCH 400E 40B4h



Bit	Symbol	Bit name	Description	R/W
b31 to b0	TEXPITCH[31:0]	Texels Per Texture Line	Specifies texels per texture line. Valid range: 0 to 2048.	W

56.2.16 Texture Size or Texture Address Mask Register (TEXMASK)

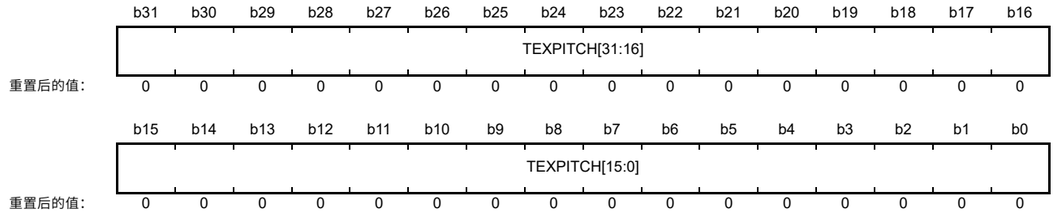
Address(es): DRW.TEXMASK 400E 40B8h



Bit	Symbol	Bit name	Description	R/W
b10 to b0	TEXUMASK[10:0]	U Mask in Texture Mode	Specifies the U mask. Set to texture_width -1. • In texture wrapping mode (CONTROL2.TEXTURECLAMPX = 0): Texture_width must be a power of 2 • In texture clamping mode (CONTROL2.TEXTURECLAMPX = 1): All widths up to 2048 are allowed.	W
b31 to b11	TEXVMASK[20:0]	V Mask in Texture Mode	Specifies the V mask. Set to DRWTEXPITCH (texture_height - 1). • In texture wrapping mode (CONTROL2.TEXTURECLAMPY = 0): Texture_height must be a power of 2 • In texture clamping mode (CONTROL2.TEXTURECLAMPY = 1): All heights up to 1024 are allowed.	W

56.2.15 每个纹理线寄存器的纹素(TEXPITCH)

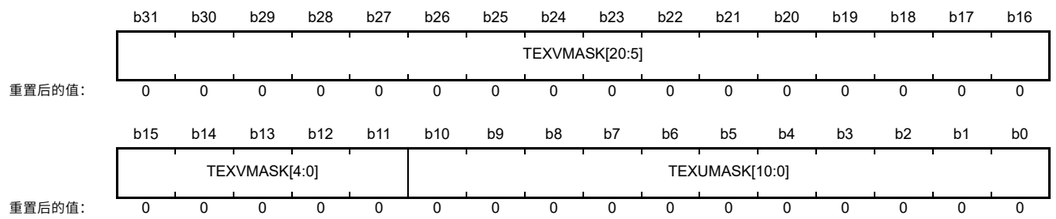
Address(es): DRW.TEXPITCH 400E 40B4h



Bit	Symbol	位名称	Description	R/W
b31 to b0	TEXPITCH[31:0]	每条纹理线的纹素	指定每条纹理线的纹素。有效范围：0到2048。	W

56.2.16 纹理大小或纹理地址掩码寄存器(TEXMASK)

Address(es): DRW.TEXMASK 400E 40B8h



Bit	Symbol	位名称	Description	R/W
b10 to b0	TEXUMASK[10:0]	纹理模式下的U蒙版	指定U掩码。设置为texture_width-1。 在纹理环绕模式下 (CONTROL2.TEXTURECLAMPX=0)：Texture_width必须是2的幂 在纹理钳制模式下 (CONTROL2.TEXTURECLAMPX=1)：允许最大为2048的所有宽度。	W
b31 to b11	TEXVMASK[20:0]	纹理模式下的V蒙版	指定V遮罩。设置为DRWTEXPITCH(texture_height1)。 在纹理环绕模式下 (CONTROL2.TEXTURECLAMPY=0)：Texture_height必须是2的幂 在纹理钳制模式下 (CONTROL2.TEXTURECLAMPY=1)：允许所有高度达到1024。	W

56.2.17 U Limiter Start Value Register (LUSTART)

Address(es): DRW.LUSTART 400E 4090h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	LUSTART[31:16]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	LUSTART[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b31 to b0	LUSTART[31:0]	U Limiter Start Value	Specifies U limiter start value.	W

56.2.18 U Limiter X-Axis Increment Register (LUXADD)

Address(es): DRW.LUXADD 400E 4094h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	LUXADD[31:16]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	LUXADD[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b31 to b0	LUXADD[31:0]	U Limiter X-Axis Increment	Specifies U limiter x-axis increment.	W

56.2.19 U Limiter Y-Axis Increment Register (LUYADD)

Address(es): DRW.LUYADD 400E 4098h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	LUYADD[31:16]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	LUYADD[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b31 to b0	LUYADD[31:0]	U Limiter Y-Axis Increment	Specifies U limiter y-axis increment.	W

56.2.17 U限制器起始值寄存器(LUSTART)

Address(es): DRW.LUSTART 400E 4090h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	LUSTART[31:16]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	LUSTART[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b31 to b0	LUSTART[31:0]	U限制器起始值	指定U限制器起始值。	W

56.2.18 U限制器X轴增量寄存器(LUXADD)

Address(es): DRW.LUXADD 400E 4094h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	LUXADD[31:16]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	LUXADD[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b31 to b0	LUXADD[31:0]	U限制器X轴增量	指定U限制器x轴增量。	W

56.2.19 U限制器Y轴增量寄存器(LUYADD)

Address(es): DRW.LUYADD 400E 4098h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	LUYADD[31:16]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	LUYADD[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b31 to b0	LUYADD[31:0]	U限制器Y轴增量	指定U限制器y轴增量。	W

56.2.20 V Limiter Start Value Integer Part Register (LVSTARTI)

Address(es): DRW.LVSTARTI 400E 409Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	LVSTARTI[31:16]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	LVSTARTI[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit nName	Description	R/W
b31 to b0	LVSTARTI[31:0]	V Limiter Start Value Integer Part	Specifies integer part of V limiter start value.	W

56.2.21 V Limiter Start Value Fractional Part Register (LVSTARTF)

Address(es): DRW.LVSTARTF 400E 40A0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	LVSTARTF[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b15 to b0	LVSTARTF[15:0]	V Limiter Start Value Fractional Part	Specifies fractional part of V limiter start value.	W
b31 to b16	—	Reserved	The write value should be 0.	W

56.2.22 V Limiter X-Axis Increment Integer Part Register (LVXADDI)

Address(es): DRW.LVXADDI 400E 40A4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	LVXADDI[31:16]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	LVXADDI[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b31 to b0	LVXADDI[31:0]	V Limiter X-Axis Increment Integer Part	Specifies integer part of V limiter x-axis increment.	W

56.2.20 V限制器起始值整数部分寄存器(LVSTARTI)

Address(es): DRW.LVSTARTI 400E 409Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	LVSTARTI[31:16]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	LVSTARTI[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit nName	Description	R/W
b31 to b0	LVSTARTI[31:0]	V限制器起始值整数部分	指定V限制器起始值的整数部分。	W

56.2.21 V限制器起始值小数部分寄存器(LVSTARTF)

Address(es): DRW.LVSTARTF 400E 40A0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	LVSTARTF[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b15 to b0	LVSTARTF[15:0]	V限制器起始值小数Part	指定V限制器起始值的小数部分。	W
b31 to b16	—	Reserved	写入值应为0。	W

56.2.22 V限制器X轴增量整数部分寄存器(LVXADDI)

Address(es): DRW.LVXADDI 400E 40A4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	LVXADDI[31:16]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	LVXADDI[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b31 to b0	LVXADDI[31:0]	V限制器X轴增量整数Part	指定V限制器x轴增量的整数部分。	W

56.2.23 V Limiter Y-Axis Increment Integer Part Register (LVYADDI)

Address(es): DRW.LVYADDI 400E 40A8h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	LVYADDI[31:16]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	LVYADDI[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b31 to b0	LVYADDI[31:0]	V Limiter Y-Axis Increment Integer Part	Specifies integer part of V limiter y-axis increment.	W

56.2.24 V Limiter Increment Fractional Parts Register (LVYXADDF)

Address(es): DRW.LVYXADDF 400E 40ACh

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	LVYADDF[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	LVXADDF[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b15 to b0	LVXADDF[15:0]	V Limiter X-Axis Increment Fractional Part	Specifies fractional part of V limiter x-axis increment.	W
b31 to b16	LVYADDF[15:0]	V Limiter Y-Axis Increment Fractional Part	Specifies fractional part of V limiter y-axis increment.	W

56.2.25 CLUT Start Address Register (TEXCLADDR)

Address(es): DRW.TEXCLADDR 400E 40DCh

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	CLADDR[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	CLADDR[7:0]	Texture CLUT Start Address	Specifies texture CLUT start address.	W

56.2.23 V限制器Y轴增量整数部分寄存器(LVYADDI)

Address(es): DRW.LVYADDI 400E 40A8h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	LVYADDI[31:16]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	LVYADDI[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b31 to b0	LVYADDI[31:0]	V限制器Y轴增量整数Part	指定V限制器y轴增量的整数部分。	W

56.2.24 V限制器增量小数部分寄存器(LVYXADDF)

Address(es): DRW.LVYXADDF 400E 40ACh

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	LVYADDF[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	LVXADDF[15:0]															
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b15 to b0	LVXADDF[15:0]	V限制器X轴增量小数Part	指定V限制器x轴增量的小数部分。	W
b31 to b16	LVYADDF[15:0]	V限制器Y轴增量小数Part	指定V限制器y轴增量的小数部分。	W

56.2.25 CLUT起始地址寄存器(TEXCLADDR)

Address(es): DRW.TEXCLADDR 400E 40DCh

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	CLADDR[7:0]							
重置后的值:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b7 to b0	CLADDR[7:0]	纹理CLUT起始地址	指定纹理CLUT起始地址。	W

Bit	Symbol	Bit name	Description	R/W
b31 to b8	—	Reserved	The write value should be 0.	W

56.2.26 CLUT Data Register (TEXCLDATA)

Address(es): DRW.TEXCLDATA 400E 40E0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	CLDATA[31:16]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CLDATA[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b31 to b0	CLDATA[31:0]	Texture CLUT Data	Specifies texture CLUT data.	W

56.2.27 CLUT Offset Register (TEXCLOFFSET)

Address(es): DRW.TEXCLOFFSET 400E 40E4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	CLOFFSET[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	CLOFFSET[7:0]	Texture CLUT Offset	Specifies texture CLUT offset. CLOFFSET[7:0] is OR gated with the original index.	W
b31 to b8	—	Reserved	The write value should be 0.	W

Bit	Symbol	位名称	Description	R/W
b31 to b8	—	Reserved	写入值应为0。	W

56.2.26 CLUT数据寄存器(TEXCLDATA)

Address(es): DRW.TEXCLDATA 400E 40E0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	CLDATA[31:16]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CLDATA[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b31 to b0	CLDATA[31:0]	纹理CLUT数据	指定纹理CLUT数据。	W

56.2.27 CLUT偏移寄存器(TEXCLOFFSET)

Address(es): DRW.TEXCLOFFSET 400E 40E4h

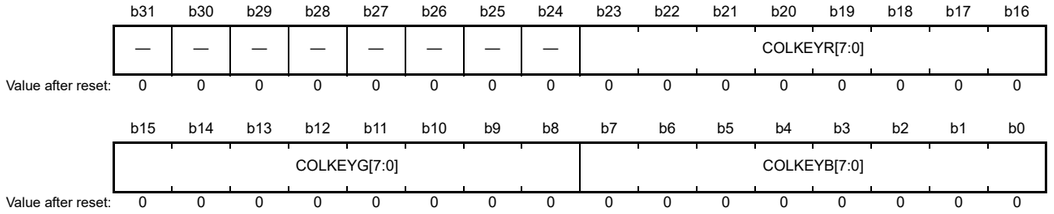
	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	CLOFFSET[7:0]							
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b7 to b0	CLOFFSET[7:0]	纹理CLUT偏移	指定纹理CLUT偏移。CLOFFSET[7:0]是使用原始索引进行或门控。	W
b31 to b8	—	Reserved	写入值应为0。	W

56.2.28 Color Key Register (COLKEY)

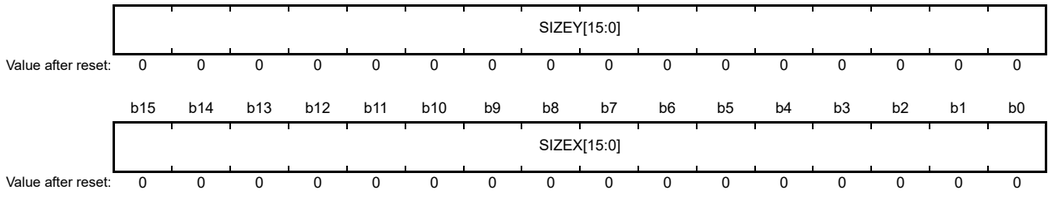
Address(es): DRW.COLKEY 400E 40E8h



Bit	Symbol	Bit name	Description	R/W
b7 to b0	COLKEYB[7:0]	Blue Channel of Color Key	Specifies blue channel of color key.	W
b15 to b8	COLKEYG[7:0]	Green Channel of Color Key	Specifies green channel of color key.	W
b23 to b16	COLKEYR[7:0]	Red Channel of Color Key	Specifies red channel of color key.	W
b31 to b24	—	Reserved	The write value should be 0.	W

56.2.29 Bounding Box Dimension Register (SIZE)

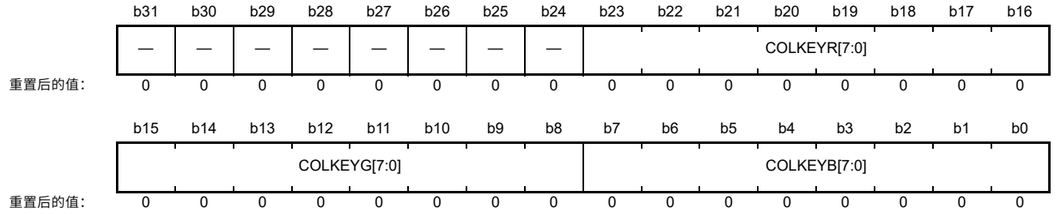
Address(es): DRW.SIZE 400E 4078h



Bit	Symbol	Bit name	Description	R/W
b15 to b0	SIZEX[15:0]	Bounding Box Width	Specifies width of bounding box in pixels. Valid range: 0 to 1024.	W
b31 to b16	SIZEY[15:0]	Bounding Box Height	Specifies height of bounding box in pixels. Valid range: 0 to 1024.	W

56.2.28 颜色键寄存器(COLKEY)

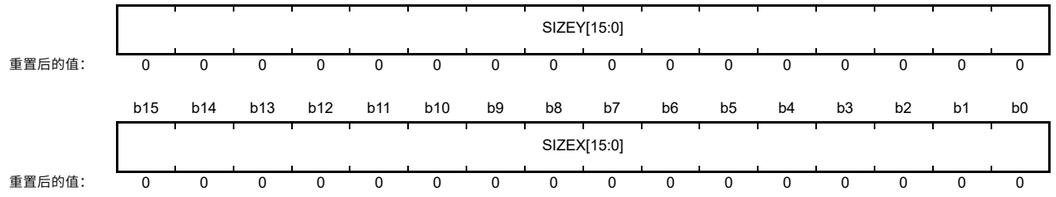
Address(es): DRW.COLKEY 400E 40E8h



Bit	Symbol	位名称	Description	R/W
b7 to b0	COLKEYB[7:0]	颜色键的蓝色通道	指定颜色键的蓝色通道。	W
b15 to b8	COLKEYG[7:0]	颜色键的绿色通道	指定颜色键的绿色通道。	W
b23 to b16	COLKEYR[7:0]	颜色键的红色通道	指定颜色键的红色通道。	W
b31 to b24	—	Reserved	写入值应为0。	W

56.2.29 边界框尺寸寄存器（SIZE）

Address(es): DRW.SIZE 400E 4078h



Bit	Symbol	位名称	Description	R/W
b15 to b0	SIZEX[15:0]	边界框宽度	以像素为单位指定边界框的宽度。有效范围：0到1024。	W
b31 to b16	SIZEY[15:0]	边界框高度	以像素为单位指定边界框的高度。有效范围：0到1024。	W

56.2.30 Framebuffer Pitch And Spanstore Delay Register (PITCH)

Address(es): DRW.PITCH 400E 407Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	SSD[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PITCH[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b15 to b0	PITCH[15:0]	Pitch of the Framebuffer	A negative width can be used to render bottom-up instead of top-down.	W
b31 to b16	SSD[15:0]	Spanstore Delay	Specifies number of scan lines to delay spanstore operations.	W

56.2.31 Framebuffer Base Address Register (ORIGIN)

Address(es): DRW.ORIGIN 400E 4080h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	ORIGIN[31:16]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ORIGIN[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b31 to b0	ORIGIN[31:0]	Address of the First Pixel in Framebuffer	Writing to ORIGIN triggers the start of rendering.	W

56.2.30 帧缓冲间距和跨度存储延迟寄存器(PITCH)

Address(es): DRW.PITCH 400E 407Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	SSD[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PITCH[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b15 to b0	PITCH[15:0]	帧缓冲区的间距	负宽度可用于自下而上而不是自上而下渲染。	W
b31 to b16	SSD[15:0]	Spanstore Delay	指定延迟spanstore操作的扫描行数。	W

56.2.31 帧缓冲基地址寄存器(ORIGIN)

Address(es): DRW.ORIGIN 400E 4080h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	ORIGIN[31:16]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ORIGIN[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b31 to b0	ORIGIN[31:0]	第一个像素的地址 Framebuffer	写入ORIGIN会触发渲染的开始。	W

56.2.32 Display List Start Address Register (DLISTSTART)

Address(es): DRW.DLISTSTART 400E 40C8h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	DLISTSTART[31:16]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	DLISTSTART[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b31 to b0	DLISTSTART[31:0]	Display List Start Address	Setting a new display list base address triggers execution of the new display list. Execution stops only when a new list is set or the current list terminates.	W

56.2.33 Performance Counters Control Register (PERFTRIGGER)

Address(es): DRW.PERFTRIGGER 400E 40D4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	PERFTRIGGER2[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PERFTRIGGER1[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b15 to b0	PERFTRIGGER1[15:0]	Trigger of Performance Counter 1	Selects the internal event that increments the PERFCOUNT1 register. 0: Disable performance counter 1: Select 2D Drawing Engine active cycles 2: Select framebuffer read access 3: Select framebuffer write access 4: Select texture read access 5: Select invisible pixels (enumerated but selected with alpha 0%) 6: Select invisible pixels while internal FIFO is empty (lost cycles) 7: Select display list reader active cycles 8: Select framebuffer read hits 9: Select framebuffer read misses 10: Select framebuffer write hits 11: Select framebuffer write misses 12: Select texture read hits 13: Select texture read misses 31: Select every clock cycle (for use as timer).	W
b31 to b16	PERFTRIGGER2[15:0]	Trigger of Performance Counter 2	Same as for PERFTRIGGER1, but for performance counter 2.	W

56.2.32 显示列表起始地址寄存器(DLISTSTART)

Address(es): DRW.DLISTSTART 400E 40C8h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	DLISTSTART[31:16]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	DLISTSTART[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b31 to b0	DLISTSTART[31:0]	显示列表起始地址	设置新的显示列表基地址会触发新显示列表的执行。仅当设置了新列表或当前列表终止时才停止执行。	W

56.2.33 性能计数器控制寄存器(PERFTRIGGER)

Address(es): DRW.PERFTRIGGER 400E 40D4h

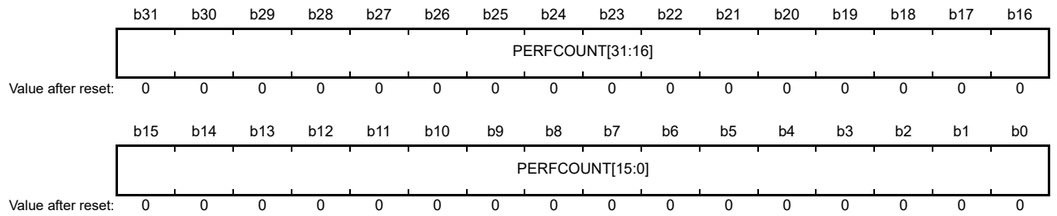
	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	PERFTRIGGER2[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	PERFTRIGGER1[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b15 to b0	PERFTRIGGER1[15:0]	绩效触发器 Counter 1	选择增加PERFCOUNT1寄存器的内部事件。 0：禁用性能计数器1：选择2D绘图引擎活动周期2：选择帧缓冲区读取访问3：选择帧缓冲区写入访问4：选择纹理读取访问5：选择不可见像素（枚举但选择alpha0%）6：选择不可见像素内部FIFO为空（丢失周期）7：选择显示列表读取器活动周期8：选择帧缓冲区读取命中9：选择帧缓冲区读取未命中10：选择帧缓冲区写入命中11：选择帧缓冲区写入未命中12：选择纹理读取命中13：选择纹理读取未命中31：选择每个时钟周期（用作计时器）。	W
b31 to b16	PERFTRIGGER2[15:0]	绩效触发器 Counter 2	与PERFTRIGGER1相同，但针对性能计数器2。	W

56.2.34 Performance Counter k (PERFCOUNTk) (k = 1, 2)

Address(es): DRW.PERFCOUNT1 400E 40CCh, DRW.PERFCOUNT2 400E 40D0h



Bit	Symbol	Bit name	Description	R/W
b31 to b0	PERFCOUNT[31:0]	Performance Counter k Value	Specifies counter k value. The counter is reset by writing PERFCOUNTk = 0000_0000h.	R/W

56.3 Drawing Features

56.3.1 Drawing Features Summary

56.3.1.1 Color formats

Supported color formats are:

Framebuffer formats

- 8-bit: a (8)
- 16-bit: RGB (565), aRGB (4444)
- 32-bit: aRGB (8888).

Texture formats

- 1-bit: CLUT (1)/I (1)
- 2-bit: CLUT (2)/I (2)
- 4-bit: CLUT (4)/I (4)
- 8-bit: a (8), CLUT (8)/I (8), aCLUT (44)
- 16-bit: aRGB (4444), aRGB (1555), RGB (565)
- 24-bit: RGB (888) (run length encoded (RLE) unit)
- 32-bit: aRGB (8888).

CLUT formats use a 256-entry color lookup table.

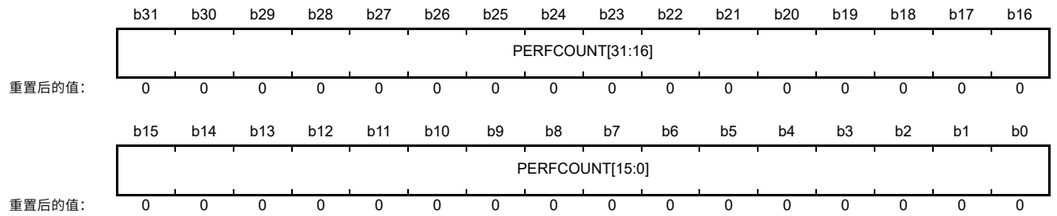
56.3.1.2 BitBLT features

The 2D Drawing Engine supports the BitBLT features using its vector drawing function to draw a rectangle and texture it based on the selected BitBLT function. This approach results in the following BitBLT features:

- Fill
- Copy
- Stretch BitBLT
- Rotate and scale
- Alpha blending

56.2.34 性能计数器k(PERFCOUNTk)(k=1 2)

Address(es): DRW.PERFCOUNT1 400E 40CCh, DRW.PERFCOUNT2 400E 40D0h



Bit	Symbol	位名称	Description	R/W
b31 to b0	PERFCOUNT[31:0]	性能计数器k值	指定计数器k值。通过写入PERFCOUNTk=0000_0000h来复位计数器。	R/W

56.3 绘图功能

56.3.1 绘图功能摘要

56.3.1.1 颜色格式

支持的颜色格式有：

Framebuffer formats

- 8-bit: a (8)
- 16-bit: RGB (565), aRGB (4444)
- 32-bit: aRGB (8888).

纹理格式

- 1-bit: CLUT (1)/I (1)
- 2-bit: CLUT (2)/I (2)
- 4-bit: CLUT (4)/I (4)
- 8-bit: a (8), CLUT (8)/I (8), aCLUT (44)
- 16-bit: aRGB (4444), aRGB (1555), RGB (565)
- 24位：RGB(888)（运行长度编码(RLE)单元）
- 32-bit: aRGB (8888).

CLUT格式使用256项颜色查找表。

56.3.1.2 BitBLT features

2D绘图引擎支持BitBLT功能，使用其矢量绘图功能绘制一个矩形并根据所选的BitBLT函数对其进行纹理化。这种方法产生了以下BitBLT功能：

- Fill
- Copy
- Stretch BitBLT
- 旋转和缩放
- 阿尔法混合

- Bilinear filtering
- Color conversion
- Subpixel exact placement.

56.3.1.3 Vector drawing features

The vector 2D Drawing Engine uses a half-plane rendering approach, which simplifies implementation of edge anti-aliasing and blurring features without much overhead. When combining some of its functional units, the module can draw not only linear primitives such as lines or polygons, but also quadratic equation-based primitives such as circles and ellipsoids. The following primitives are supported:

- Lines
- Polygons
- Circles and ellipses
- Quadratic curves (software driver support)
- 2D texture mapping
- Bilinear filtering of the textures.

56.3.2 Vector Drawing

For a detailed explanation of the algorithms, see section 56.6, Rendering Pipeline. Supported vector drawing includes:

Lines

- Arbitrary width
- Round endpoints
- Truncated endpoints
- Alpha gradients
- Soft edges (blurring)
- Render attribute: color, pattern, or texture.

Polygons

- Triangles and quadrangles (complex polygons are tessellated by software)
- Alpha gradients
- Soft edges (blurring)
- Per edge controls for anti-aliasing
- Render attribute: color, pattern, or texture.

Circles and ellipses

- All conic sections
- Filled or with arbitrary width
- Arcs of 0° to 360°
- Soft edges
- Alpha gradients
- Render attribute: color, pattern, or texture.

Quadratic Bézier

- Approximated by circle arcs
- Arbitrary width

- Bilinear filtering
- 颜色转换
- 亚像素精确位置。

56.3.1.3 矢量绘图功能

矢量2D绘图引擎使用半平面渲染方法，可简化边缘抗锯齿和模糊功能的实现，而无需太多开销。当组合它的一些功能单元时，该模块不仅可以绘制直线或多边形等线性图元，还可以绘制圆和椭圆体等基于二次方程的图元。支持以下原语：

- Lines
- Polygons
- 圆和椭圆
- 二次曲线（软件驱动支持）
- 2D纹理映射
- 纹理的双线性过滤。

56.3.2 矢量绘图

有关算法的详细说明，请参阅第56.6节，渲染管道。支持的矢量图包括：

Lines

- 任意宽度
- Round endpoints
- Truncated endpoints
- 阿尔法渐变
- 软边缘（模糊）
- 渲染属性：颜色、图案或纹理。

Polygons

- 三角形和四边形（复杂的多边形由软件镶嵌）
- 阿尔法渐变
- 软边缘（模糊）
- 用于抗锯齿的每个边缘控制
- 渲染属性：颜色、图案或纹理。

圆和椭圆

- 所有圆锥截面
- 填充或任意宽度
- 0°到360°的弧度
- 软边
- 阿尔法渐变
- 渲染属性：颜色、图案或纹理。

Quadratic Bézier

- 近似圆弧
- 任意宽度

- Round or truncated endpoints
- Outlines, blurring
- Alpha gradients
- Render attribute: color.

Texture mapping

- 2D array of pixels that can be mapped implicitly or explicitly on all primitives provided by the 2D Drawing Engine
- Translation, rotation, and scaling/shearing
- Bilinear filtering of the textures
- 3D-like texturing accomplished with line-by-line mapping, if constant in one axis.

56.3.3 BitBLT

A dedicated BitBLT unit is not required in the 2D Drawing Engine. The rendering pipeline described for vector drawing is used as the BitBLT unit and already provides a 1 pixel/cycle throughput. For details, see section 56.6, Rendering Pipeline.

56.3.3.1 Fill

Any rectangle in the framebuffer can be filled with any value. Possible color formats are any 8-, 16-, or 32-bpp format. The driver optimizes the fill to gain the full benefit of 32-bit parallel rasterization. If the selected color format is less than 32 bpp, the driver corrects the alignment and fills 32 bits per clock, resulting in 2 to 4 times faster fill performance for 8- and 16-bpp formats.

56.3.3.2 Copy

Any rectangle in the framebuffer can be filled with any rectangular data from the texture input. When the texture input points to the framebuffer, copying from framebuffer to framebuffer is possible. To avoid copy problems because of overlapping source and destination areas, the copy start point can be selected from top left to bottom right. Possible color formats are any 8-, 16-, or 32-bpp format.

The driver optimizes the copy to gain the full benefit of 32-bit parallel rasterization. If the selected color format is less than 32 bpp, the driver corrects the alignment and copies 32 bits per clock, resulting in 2 to 4 times faster copy performance for 8- and 16-bpp formats.

56.3.3.3 Stretch BitBLT

This is similar to the normal copy operation. Because the copy is done as a type of texture mapping, the full texture mapping feature set can be used. Any scaling ratios in the x and y directions is selectable, and filtering can be enabled independently for each axis.

56.3.3.4 Rotate and scale

This is similar to the normal copy operation. Because the copy is done as a type of texture mapping, the full texture mapping feature set can be used. Any scaling ratios in the x and y direction and any rotation angle is selectable. The x and y directions can be rotated and scaled independently, and filtering for the scalers can be enabled independently for each axis.

56.3.3.5 Alpha blending

Alpha blending is a fundamental block in the rendering pipeline, so the full alpha blend feature set is available for any BitBLT operation. It is possible to copy an area and blend it over the destination by using any constant global alpha value (register value) or by using an alpha mask. The alpha mask is part of the texture data and can be either a per-pixel value together with a pixel color (aRGB formats) or an alpha-only format using a register color.

In addition to the color channels, the alpha channel can be blended. The formula for the alpha channel can be set independently from the formula for the color channels.

- 圆形或截断端点
- 轮廓，模糊
- 阿尔法渐变
- 渲染属性：颜色。

纹理映射

- 可以在2D绘图引擎提供的所有图元上隐式或显式映射的2D像素数组
- 平移、旋转和缩放剪切
- 纹理的双线性过滤
- 如果在一个轴上保持不变，则通过逐行映射完成类似3D的纹理。

56.3.3 BitBLT

2D绘图引擎中不需要专用的BitBLT单元。矢量绘图所描述的渲染管道用作BitBLT单元，并且已经提供了1个像素周期的吞吐量。有关详细信息，请参阅第56.6节，渲染管道。

56.3.3.1 Fill

帧缓冲区中的任何矩形都可以填充任何值。可能的颜色格式是任何8、16或32-bpp格式。驱动程序优化填充以获得32位并行光栅化的全部优势。如果所选颜色格式小于32bpp，驱动程序会纠正对齐并填充每个时钟32位，从而使8和16-bpp格式的填充性能提高2到4倍。

56.3.3.2 Copy

帧缓冲区中的任何矩形都可以填充来自纹理输入的任何矩形数据。当纹理输入指向帧缓冲区时，可以从帧缓冲区复制到帧缓冲区。为避免由于源区域和目标区域重叠而导致的复制问题，可以从左上角到右下角选择复制起点。可能的颜色格式是任何8、16或32-bpp格式。

驱动程序优化副本以获得32位并行光栅化的全部优势。如果所选颜色格式小于32bpp，驱动程序会纠正对齐并以每时钟32位的速度复制，从而使8和16-bpp格式的复制性能提高2到4倍。

56.3.3.3 Stretch BitBLT

这类似于正常的复制操作。因为复制是作为一种纹理映射完成的，所以可以使用完整的纹理映射特征集。x和y方向上的任何缩放比例都是可选的，并且可以为每个轴独立启用过滤。

56.3.3.4 旋转和缩放

这类似于正常的复制操作。因为复制是作为一种纹理映射完成的，所以可以使用完整的纹理映射特征集。x和y方向上的任何缩放比例以及任何旋转角度都是可选的。x和y方向可以独立旋转和缩放，并且可以为每个轴独立启用缩放器的过滤。

56.3.3.5 阿尔法混合

Alpha混合是渲染管道中的一个基本块，因此完整的Alpha混合功能集可用于任何BitBLT操作。通过使用任何恒定的全局alpha值（寄存器值）或使用alpha掩码，可以复制一个区域并将其混合到目标上。alpha掩码是纹理数据的一部分，可以是每像素值和像素颜色（aRGB格式），也可以是使用寄存器颜色的仅alpha格式。

除了颜色通道，还可以混合Alpha通道。Alpha通道的公式可以独立于颜色通道的公式进行设置。

56.3.3.6 Bilinear filtering

The texture unit can be used to scale, rotate, or shear images. The texturing result can be filtered in the x and y directions independently. When selecting both filters, the result is a bilinear filtered texture. Using the unit twice with two independent textures would generate trilinear filtered bitmaps, improving the visual impression for high dynamic scale ratios.

56.3.3.7 Color conversion

Color conversion is required when using different texture formats than the framebuffer format. For saving texture memory, several formats are supported with less bpp than the framebuffer usually has. The 2D Drawing Engine always operates internally with 32-bpp aRGB (8888). All input data is converted into 32 bpp, and finally is converted back into the framebuffer format.

56.4 Input and Output Data Formats

56.4.1 Source and Destination Data

There are two possible inputs, the framebuffer and the texture or pattern input. The output is always the framebuffer.

Every drawing operation is internally rendered in 32 bpp aRGB (8888). If the input color does not provide an alpha channel, the blue channel is taken as the alpha channel. This alpha can be substituted with any alpha (for example, by an external constant) during the colorization step in the 2D Drawing Engine.

56.4.2 Framebuffer Color Formats

Table 56.1 shows the supported framebuffer color formats.

Table 56.1 Framebuffer color formats

Framebuffer memory occupation	Format	Remarks
8 bpp	a (8)	This color format uses 1 byte per pixel. The alpha channel is internally replicated on the red, blue, and green channels and can be substituted with any color during the color step in the 2D Drawing Engine.
16 bpp	RGB (565)	This color format uses 2 bytes per pixel with 5 bits for red and blue and 6 bits for green. The blue color is taken as the alpha channel during color conversion. The alpha can be substituted with any alpha during the colorization step in the 2D Drawing Engine.
	aRGB (4444)	This color format uses 2 bytes per pixel with 4 bits for each color and alpha channel.
32 bpp	aRGB (8888)	This color format uses 4 bytes per pixel with 8 bits for each color and alpha channel.

The framebuffer color format is selected in the Surface Control Register bits, CONTROL2.READFORMAT[2:0].

56.4.3 Texture Color Formats

Table 56.2 shows the supported texture color formats.

Table 56.2 Texture color formats (1 of 2)

Texture memory occupation	Format	Remarks
1 bpp	CLUT (1)/I (1)	In this mode, a 1-bit index is used to address one of 256 predefined colors in the color lookup table. If the CLUT is not used, the index is taken as a luminance value.
2 bpp	CLUT (2)/I (2)	In this mode, a 2-bit index is used to address one of 256 predefined colors in the color lookup table. If the CLUT is not used, the index is taken as a luminance value.
4 bpp	CLUT (4)/I (4)	In this mode, a 4-bit index is used to address one of 256 predefined colors in the color lookup table. If the CLUT is not used, the index is taken as a luminance value.

56.3.3.6 Bilinear filtering

纹理单元可用于缩放、旋转或剪切图像。纹理结果可以在x和y方向上独立过滤。选择两个过滤器时，结果是双线性过滤纹理。使用具有两个独立纹理的单元两次将生成三线性过滤位图，从而改善高动态比例的视觉印象。

56.3.3.7 颜色转换

当使用与帧缓冲区格式不同的纹理格式时，需要进行颜色转换。为了节省纹理内存，支持多种格式，其bpp比通常的帧缓冲区少。2D绘图引擎始终在内部以32-bppaRGB(8888)运行。所有输入数据都转换为32bpp，最后转换回帧缓冲区格式。

56.4 输入和输出数据格式

56.4.1 源数据和目标数据

有两种可能的输入，帧缓冲区和纹理或图案输入。输出始终是帧缓冲区。

每个绘图操作在内部以32bppaRGB(8888)呈现。如果输入颜色不提供Alpha通道，则将蓝色通道作为Alpha通道。在2D绘图引擎中的着色步骤期间，此alpha可以替换为任何alpha（例如，由外部常量）。

56.4.2 帧缓冲区颜色格式

表56.1显示了支持的帧缓冲区颜色格式。

Table 56.1 帧缓冲区颜色格式

帧缓冲内存占用	Format	Remarks
8 bpp	a (8)	这种颜色格式每个像素使用1个字节。Alpha通道在内部复制到红色、蓝色和绿色通道上，并且可以在2D绘图引擎中的颜色步骤中替换为任何颜色。
16 bpp	RGB (565)	这种颜色格式每个像素使用2个字节，其中5位用于红色和蓝色，6位用于绿色。在颜色转换过程中，蓝色作为Alpha通道。在2D绘图引擎的着色步骤中，可以用任何alpha替换alpha。
	aRGB (4444)	这种颜色格式每个像素使用2个字节，每个颜色和Alpha通道使用4位。
32 bpp	aRGB (8888)	这种颜色格式每个像素使用4个字节，每个颜色和Alpha通道使用8位。

帧缓冲区颜色格式在表面控制寄存器位CONTROL2.READFORMAT[2:0]中选择。

56.4.3 纹理颜色格式

表56.2显示了支持的纹理颜色格式。

Table 56.2 纹理颜色格式(1of2)

纹理内存占用	Format	Remarks
1 bpp	CLUT (1)/I (1)	在此模式下，使用1位索引来寻址颜色查找表中的256种预定义颜色之一。如果不使用CLUT，则将索引作为亮度值。
2 bpp	CLUT (2)/I (2)	在此模式下，使用2位索引来寻址颜色查找表中的256种预定义颜色之一。如果不使用CLUT，则将索引作为亮度值。
4 bpp	CLUT (4)/I (4)	在此模式下，使用4位索引来寻址颜色查找表中的256种预定义颜色之一。如果不使用CLUT，则将索引作为亮度值。

Table 56.2 Texture color formats (2 of 2)

Texture memory occupation	Format	Remarks
8 bpp	CLUT (8)/I (8)	In this mode, an 8-bit index is used to address one of 256 predefined colors in the color lookup table. If the CLUT is not used, the index is taken as a luminance value.
	a (8)	This color format uses 1 byte per pixel. The alpha channel is internally replicated on the red, blue, and green channels and can be substituted with any color during the colorization step in the 2D Drawing Engine.
	aCLUT (44)	This color format uses 1 byte per pixel. 4 bits are used as an alpha value and 4 bits are used as an index to a color palette. This approach saves space if 16 colors are sufficient to describe the image, because the next bigger alpha format would be 2-byte aRGB (4444).
16 bpp	RGB(565)	This color format uses 2 bytes per pixel with 5 bits for red and blue and 6 bits for green. The blue color is taken as the alpha channel during color conversion. The alpha can be substituted with any alpha during the colorization step in the 2D Drawing Engine.
	aRGB (4444)	This color format uses 2 bytes per pixel with 4 bits for each color and alpha channel.
	aRGB (1555)	This color format uses 2 bytes per pixel. Every color channel has 5 bits and the topmost single bit is taken as an alpha value. This can be used to hold an image with a transparency mask.
24 bpp	RGB (888)	This color format uses 3 bytes per pixel with 8 bits for each color channel. This format is only available as run length encoded data (RLE compression).
32 bpp	aRGB (8888)	This color format uses 4 bytes per pixel with 8 bits for each color and alpha channel.

The texture color format is selected in the Surface Control Register bits, CONTROL2.WRITEFORMAT[3:0].

56.5 Texture Data Processing

Figure 56.4 shows the processing of texture data.

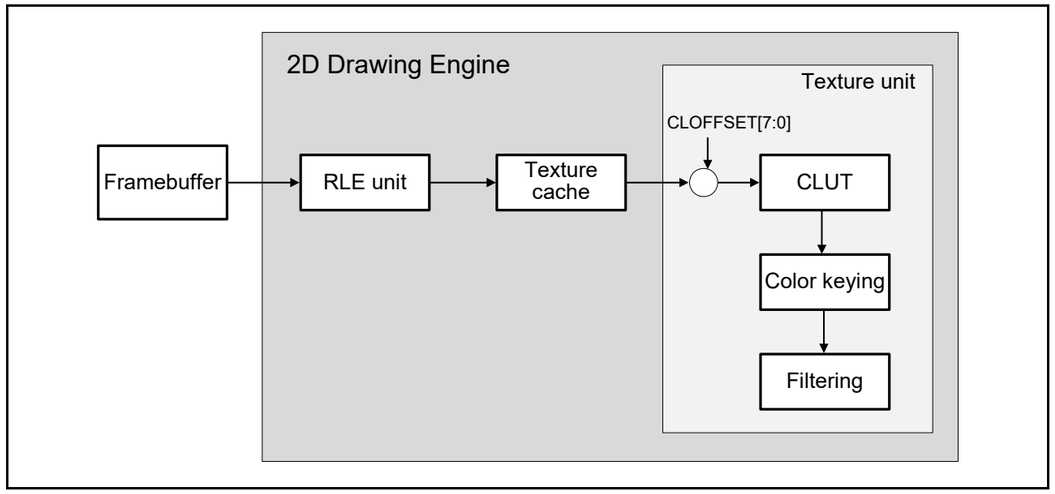


Figure 56.4 Texture data processing

56.5.1 Texture Color Format

Table 56.3 shows the supported texture data formats.

Table 56.2 纹理颜色格式(2of2)

纹理内存占用	Format	Remarks
8 bpp	CLUT (8)/I (8)	在此模式下，使用8位索引来寻址颜色查找表中的256种预定义颜色之一。如果不使用CLUT，则将索引作为亮度值。
	a (8)	这种颜色格式每个像素使用1个字节。Alpha通道在内部复制到红色、蓝色和绿色通道上，并且可以在2D绘图引擎中的着色步骤中替换为任何颜色。
	aCLUT (44)	这种颜色格式每个像素使用1个字节。4位用作alpha值，4位用作调色板的索引。如果16种颜色足以描述图像，这种方法可以节省空间，因为下一个更大的alpha格式将是2字节aRGB(4444)。
16 bpp	RGB(565)	这种颜色格式每个像素使用2个字节，其中5位用于红色和蓝色，6位用于绿色。在颜色转换过程中，蓝色作为Alpha通道。在2D绘图引擎的着色步骤中，可以用任何alpha替换alpha。
	aRGB (4444)	这种颜色格式每个像素使用2个字节，每个颜色和Alpha通道使用4位。
	aRGB (1555)	这种颜色格式每个像素使用2个字节。每个颜色通道有5位，最高的一位作为alpha值。这可用于保存带有透明蒙版的图像。
24 bpp	RGB (888)	这种颜色格式每个像素使用3个字节，每个颜色通道使用8位。此格式仅可用作行程编码数据（RLE压缩）。
32 bpp	aRGB (8888)	这种颜色格式每个像素使用4个字节，每个颜色和Alpha通道使用8位。

纹理颜色格式在表面控制寄存器位CONTROL2.WRITEFORMAT[3:0]中选择。

56.5 纹理数据处理

图56.4显示了纹理数据的处理。

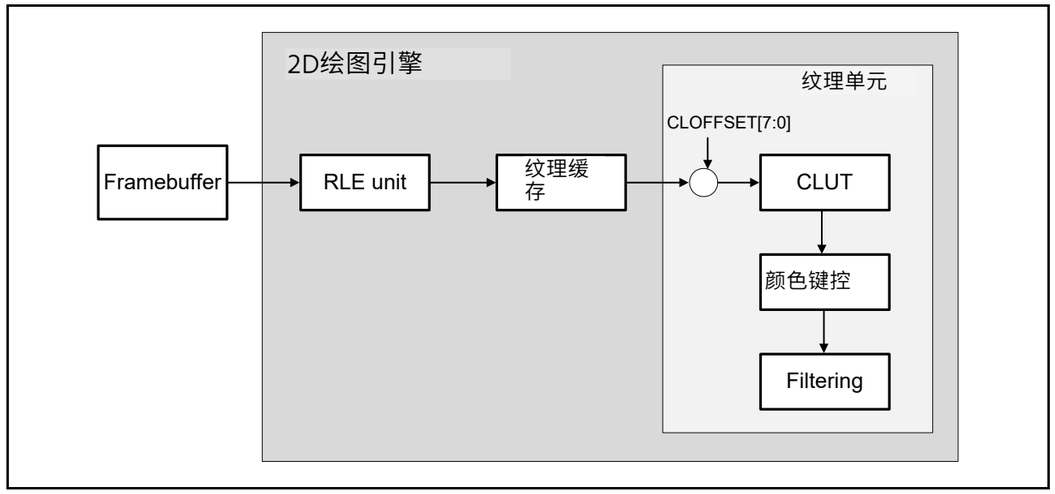


Figure 56.4 纹理数据处理

56.5.1 纹理颜色格式

表56.3显示了支持的纹理数据格式。

Table 56.3 Texture color formats

Texel bit width	Texel format
32 bits	aRGB (8888)
24 bits	RGB (888)
16 bits	aRGB (4444), aRGB (1555), RGB (565)
8 bits	CLUT (8)I (8), a (8), aCLUT (44)
4 bits	CLUT (4)/I (4)
2 bits	CLUT (2)/I (2)
1 bit	CLUT (1)/I (1)

56.5.2 Run Length Encoded (RLE) Unit

The RLE unit decompresses Targa-like compressed textures and hands the decompressed texel data over to the texture unit. The key features are:

- Support for Targa format
- Avoids the additional Targa limitation to scan lines
- Support for clipping of compressed images, in which the 2D Drawing Engine is allowed to copy only a portion of a larger original texture
- Control of the RLE unit in drawing list operation
- Bypassing of the RLE unit logic if uncompressed textures are fetched from the framebuffer.

Texture cache

The RLE unit feeds the texture cache. The texture cache can be disabled by setting CACHECTL.CENABLETX = 0.

Caution: A texture cache flush operation (CACHECTL.CFLUSHTX = 1) is necessary at the beginning and end of every new RLE texture.

The texture cache and the RLE unit can be bypassed by setting CONTROL2.RLEENABLE = 0.

56.5.2.1 RLE Texel formats

Table 56.4 lists the data formats supported by the RLE unit.

Table 56.4 Texel formats supported by the RLE unit (1 of 2)

Memory texel format	RLE parameters	RLE coded unit format (CONTROL2.RLEPIXELWIDTH[1:0])	Delivered format
32-bit aRGB (8888)	Included in Targa and RLE formats	32 bits (11b)	32 bits
24-bit RGB (888)		24 bits (10b)	32 bits *1
16-bit aRGB (4444), aRGB (1555), RGB (565)		16 bits (01b)	16 bits
8-bit CLUT (8)I (8), a (8), aCLUT (44)		8 bits (00b)	8 bits
4-bit CLUT (4)/I (4)	Optional for RLE *2	8 = 2 x 4 bits	4 + 4 bits

Table 56.3 纹理颜色格式

纹素位宽	Texel format
32 bits	aRGB (8888)
24 bits	RGB (888)
16 bits	aRGB (4444), aRGB (1555), RGB (565)
8 bits	CLUT (8)I (8), a (8), aCLUT (44)
4 bits	CLUT (4)/I (4)
2 bits	CLUT (2)/I (2)
1 bit	CLUT (1)/I (1)

56.5.2 运行长度编码(RLE)单元

RLE单元解压缩类似Targa的压缩纹理，并将解压缩的纹素数据交给纹理单元。主要特点是：

- 支持Targa格式
- 避免了对扫描线的额外Targa限制
- 支持剪切压缩图像，其中2D绘图引擎只允许复制较大原始纹理的一部分
- 图纸列表操作中RLE单元的控制
- 如果从帧缓冲区获取未压缩的纹理，则绕过RLE单元逻辑。

纹理缓存

RLE单元提供纹理缓存。可以通过设置CACHECTL.CENABLETX=0来禁用纹理缓存。

Caution: 在每个新RLE纹理的开始和结束时都需要进行纹理缓存刷新操作(CACHECTL.CFLUSHTX=1)。

可以通过设置CONTROL2.RLEENABLE=0绕过纹理缓存和RLE单元。

56.5.2.1 RLE Texel formats

表56.4列出了RLE单元支持的数据格式。

Table 56.4 RLE单元支持的纹素格式(1of2)

内存纹素格式	RLE parameters	RLE编码单元格式(CONTROL2.RLEPIXELWIDTH[1:0])	交付格式
32-bit aRGB (8888)	包含在Targa和RLE格式中	32 bits (11b)	32 bits
24-bit RGB (888)		24 bits (10b)	32 bits *1
16-bit aRGB (4444), aRGB (1555), RGB (565)		16 bits (01b)	16 bits
8-bit CLUT (8)I (8), a (8), aCLUT (44)		8 bits (00b)	8 bits
4-bit CLUT (4)/I (4)	RLE可选*2	8 = 2 x 4 bits	4 + 4 bits

Table 56.4 Texel formats supported by the RLE unit (2 of 2)

Memory texel format	RLE parameters	RLE coded unit format (CONTROL2.RLEPIXELWIDTH[1:0])	Delivered format
2-bit CLUT (2)/I (2)	No RLE		
1-bit CLUT (1)/I (1)			

Note 1. 24-bit RGB (888) encoded texels are delivered as aRGB (8888) with Alpha set to 1.
Note 2. Encoding of textures with 4 bits per texel is not defined by the Targa specification but can be done by:
- Combining two 4-bit texels to one byte
- Padding with 4 zero bits at the end of the file, if the number of texels is odd
- Encoding as with 8-bit texels.

Texel addressing for RLE textures

The address of a texel is the byte address of the first byte of the texel. The origin of the texture is given by the register TEXORIGIN.

Note: The RLE code must begin at a word boundary of the memory.

Caution: When the FIFO is filled, there is no provision to inhibit read access beyond the end of the RLE code. To avoid memory access violations, the RLE code must be padded by 32 memory words, where every bit of each word is set to 1.

56.5.2.2 Targa RLE format

Run-length encoded (RLE) images include two types of data elements:

- Run-length packets
- Raw packets.

The first field (1 byte) of each packet is called the repetition count field. The second field is called the pixel value field (1, 2, 3. or 4 bytes). For run-length packets, the pixel value field contains a single pixel value. For raw packets, the field is a variable number of pixel values.

The highest order bit of the repetition count indicates whether the packet is a raw packet or a run-length packet, as follows:

- If bit [7] of the repetition count is set to 1, the packet is a run-length packet
- If bit [7] of the repetition count is set to zero, the packet is a raw packet.

The lower 7 bits of the repetition count specify how many pixel values are represented by the packet. For a run-length packet, this count indicates how many successive pixels have the pixel value specified in the pixel value field. For raw packets, this count specifies how many pixel values are actually contained in the next field. This 7-bit value is actually encoded as 1 less than the number of pixels in the packet (a value of 0 implies 1 pixel while a value of 7Fh implies 128 pixels).

Run-length packet

Run-length packets are composed of two parts. The first is a repetition count and the second is the pixel value to repeat.

Table 56.5 Run-length packet

Field name	Packet type (must be 1 for run-length)	Pixel count (number of pixels encoded in this packet - 1)	Pixel data (the shared pixel value to be used)
Field size	1 bit	7 bits	Pixel depth (field 5.5)

Raw packet

The raw packet always includes two fields. The first field is the repetition count and the second field is the pixel data field.

Table 56.4 RLE单元支持的纹素格式(2of2)

内存纹素格式	RLE parameters	RLE编码单元格式(CONTROL2.RLEPIXELWIDTH[1:0])	交付格式
2-bit CLUT (2)/I (2)	No RLE		
1-bit CLUT (1)/I (1)			

Note 1. 24位RGB(888)编码的纹素以aRGB(8888)形式提供，Alpha设置为1。
Note 2. Targa规范没有定义每个纹素4位的纹理编码，但可以通过以下方式完成：将两个4位纹素组合为一个字节如果纹素数为奇数，则在文件末尾填充4个零位编码与8位纹素一样。

RLE纹理的Texel寻址

纹素的地址是纹素的第一个字节的字节地址。纹理的来源由寄存器给出TEXORIGIN.

Note: RLE代码必须从存储器的字边界开始。

Caution: 当FIFO被填满时，没有规定禁止在RLE代码结束后进行读取访问。为避免内存访问违规，RLE代码必须填充32个内存字，其中每个字的每一位都设置为1。

56.5.2.2 Targa RLE format

游程编码(RLE)图像包括两种类型的数据元素：

- Run-length packets
- 原始数据包。

每个数据包的第一个字段（1个字节）称为重复计数字段。第二个字段称为像素值字段（1、2、3.或4个字节）。对于游程包，像素值字段包含单个像素值。对于原始数据包，该字段是可变数量的像素值。

重复计数的最高位指示该数据包是原始数据包还是游程数据包，如下所示：

- 如果重复计数的第[7]位设置为1，则数据包是游程数据包
- 如果重复计数的位[7]设置为零，则数据包是原始数据包。

重复计数的低7位指定数据包表示多少像素值。对于游程长度数据包，此计数指示有多少连续像素具有像素值字段中指定的像素值。对于原始数据包，此计数指定下一个字段中实际包含多少像素值。这个7位值实际上被编码为比数据包中的像素数少1（值0表示1个像素，而值7Fh表示128个像素）。

Run-length packet

游程包由两部分组成。第一个是重复计数，第二个是要重复的像素值。

Table 56.5 Run-length packet

字段名称	数据包类型（行程长度必须为1）	像素数（此数据包中编码的像素数1）	像素数据（要使用的共享像素值）
字段大小	1 bit	7 bits	像素深度（5.5场）

原始数据包

原始数据包始终包含两个字段。第一个字段是重复计数，第二个字段是像素数据字段。

Table 56.6 Raw packet

Field name	Packet type (must be 0 for raw packet)	Pixel count (number of pixels encoded by this packet - 1)	Pixel data
Field size	1 bit	7 bits	Pixel depth x pixel count - 1

56.5.3 Color Lookup Table (CLUT)

The color lookup table receives an index that addresses one out of the 256 predefined colors.

The predefined color format can be selected as:

- CONTROL2.CLUTFORMAT = 0: aRGB (8888)
- CONTROL2.CLUTFORMAT = 1: RGB (565).

The CLUT is filled by the use of two registers:

- TEXCLDATA
  The aRGB (8888) color definition is written to this register, while the CLUT address is taken from TEXCLADDR.
- TEXCLADDR.
  This is set to the first address of the CLUT to write to and is automatically incremented after each write to TEXCLDATA.

An offset for indexed formats (CLUT (1), CLUT (2), CLUT (4), and CLUT (8)) can be set up in the TEXCLOFFSET register to allow selecting an offset part of the CLUT. The CLUT index is calculated by CLUT (x) or TEXCLOFFSET.CLOFFSET[7:0].

56.5.3.1 CLUT/I pixel data formats

The following tables explain in which order the pixels are stored within the byte. The left-most pixel is stored at the lowest bit of the memory byte.

CLUT (1)/I (1) format

The CLUT (1)/I (1) format expresses 1 pixel by using a total of 1 bit.

Memory byte	7 (MSB)	6	5	4	3	2	1	0 (LSB)
Pixel	P7	P6	P5	P4	P3	P2	P1	P0

The left-most pixel is stored at lowest bit of the memory byte.

CLUT (2)/I (2) format

The CLUT (2)/I (2) format expresses 1 pixel by using a total of 2 bits.

Memory byte	7 (MSB)	6	5	4	3	2	1	0 (LSB)
Pixel	P3		P2		P1		P0	

The left-most pixel is stored at lowest 2 bits of the memory byte.

CLUT (4)/I (4) format

The CLUT (4)/I (4) format expresses 1 pixel by using a total of 4 bits.

Memory byte	7 (MSB)	6	5	4	3	2	1	0 (LSB)

Table 56.6 原始数据包

字段名称	数据包类型（原始数据包必须为0）	像素数（此数据包编码的像素数1）	像素数据
字段大小	1 bit	7 bits	像素深度x像素数1

56.5.3 颜色查找表(CLUT)

颜色查找表接收一个索引，该索引对256种预定义颜色中的一种进行寻址。

预定义的颜色格式可以选择为：

- CONTROL2.CLUTFORMAT = 0: aRGB (8888)
- CONTROL2.CLUTFORMAT = 1: RGB (565).

CLUT使用两个寄存器填充：

- TEXCLDATA
  aRGB(8888)颜色定义写入该寄存器，而CLUT地址取自TEXCLADDR。
- TEXCLADDR。这设置为要写入的CLUT的第一个地址，并在每次写入后自动递增

  TEXCLDATA.

可以在TEXCLOFFSET寄存器中设置索引格式（CLUT(1)、CLUT(2)、CLUT(4)和CLUT(8)）的偏移量，以允许选择CLUT的偏移量部分。CLUT指数由CLUT(x)或TEXCLOFFSET.CLOFFSET[7:0]计算得出。

56.5.3.1 CLUTI像素数据格式

下表解释了像素在字节中的存储顺序。最左边的像素存储在内存字节的最低位。

CLUT (1)/I (1) format

CLUT(1)I(1)格式通过使用总共1位来表示1个像素。

内存字节	7 (MSB)	6	5	4	3	2	1	0 (LSB)
Pixel	P7	P6	P5	P4	P3	P2	P1	P0

最左边的像素存储在内存字节的最低位。

CLUT (2)/I (2) format

CLUT(2)I(2)格式通过使用总共2位来表示1个像素。

内存字节	7 (MSB)	6	5	4	3	2	1	0 (LSB)
Pixel	P3		P2		P1		P0	

最左边的像素存储在内存字节的最低2位。

CLUT (4)/I (4) format

CLUT(4)I(4)格式通过使用总共4位来表示1个像素。

内存字节	7 (MSB)	6	5	4	3	2	1	0 (LSB)

Pixel	P1	P0

The left-most pixel is stored at lowest 4 bits of the memory byte.

56.5.4 Color Keying

The 2D Drawing Engine provides a color keying unit in front of the texture unit. It operates as follows:

1. If enabled, the incoming color is compared with a transparent color, defined by COLKEY.
2. If the value matches, the alpha and color values are set to 0 to mark the color as transparent and handle it as if alpha was pre-multiplied.
3. If the value does not match, then alpha is set to 1.
4. Additional operations such as alpha_in × alpha_const are still possible.

With this approach, an object such as a round icon can be cut out from a rectangular texture and still can be faded by a constant alpha over the background.

56.6 Rendering Pipeline

56.6.1 Coordinate Transformation

Coordinate transformation such as rotation, translation, projection, and scaling must be done on the application side. This is not part of the 2D Drawing Engine hardware or driver. Because all coordinates fed into the 2D Drawing Engine are in fixed point format, these calculations can be made in fixed point format and do not require a floating point unit.

56.6.2 Rasterization

During rasterization, the vector data of the object must be converted to pixel data. To convert the data, the program sets up the edge interpolation hardware, called a limiter, for each edge of the object that calculates a decision value. The limiter determines which side of the edge the pixel is positioned on. The 2D Drawing Engine includes six internal hardware limiters. In principle, the limiter registers contain the distance between the pixel being processed and the edge.

In the linear setup, a limiter describes a half plane. The intersection of all half planes is the object. If three half planes intersect, a triangle is created as shown in Figure 56.5.

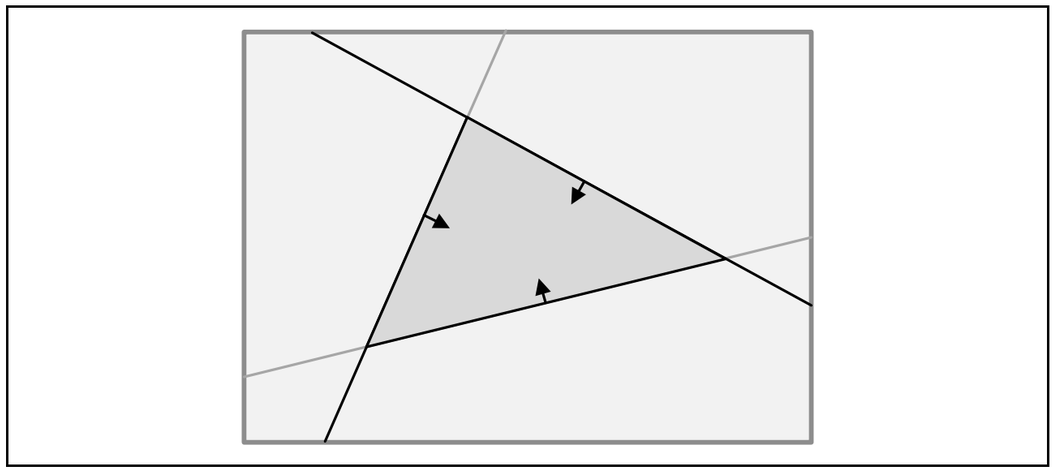


Figure 56.5 Intersection of half planes

The limiter output is clamped to an interval of [0:1]. In limiters 1 and 2 it is possible to apply a band filter before the clamping operation. In this case, the limiter is not describing a half plane but a small band. With this approach, a single limiter can describe a thick line of infinite length.

The output of the different limiters can be combined by the combiner units with a maximum or minimum operation.

Pixel	P1	P0

最左边的像素存储在内存字节的最低4位。

56.5.4 颜色键控

2D绘图引擎在纹理单元之前提供了一个颜色键控单元。它的运作方式如下：

1. 如果启用，则将传入颜色与由COLKEY定义的透明颜色进行比较。
2. 如果该值匹配，则将alpha和颜色值设置为0以将颜色标记为透明并像alpha被预乘一样处理它。
3. 如果值不匹配，则alpha设置为1。
4. 诸如alpha_in×alpha_const之类的附加操作仍然是可能的。

使用这种方法，可以从矩形纹理中剪切出诸如圆形图标之类的对象，并且仍然可以通过背景上的恒定alpha淡化。

56.6 渲染管线

56.6.1 坐标变换

旋转、平移、投影、缩放等坐标变换必须在应用端完成。这不是2D绘图引擎硬件或驱动程序的一部分。因为输入2D绘图引擎的所有坐标都是定点格式，所以这些计算可以定点格式进行，不需要浮点单位。

56.6.2 Rasterization

在光栅化过程中，必须将对象的矢量数据转换为像素数据。为了转换数据，程序为计算决策值的对象的每个边缘设置边缘插值硬件，称为限制器。限制器确定像素位于边缘的哪一侧。2D绘图引擎包括六个内部硬件限制器。原则上，限制寄存器包含正在处理的像素与边缘之间的距离。

在线性设置中，限制器描述了一个半平面。所有半平面的交点就是对象。如果三个半平面相交，则会创建一个三角形，如图56.5所示。

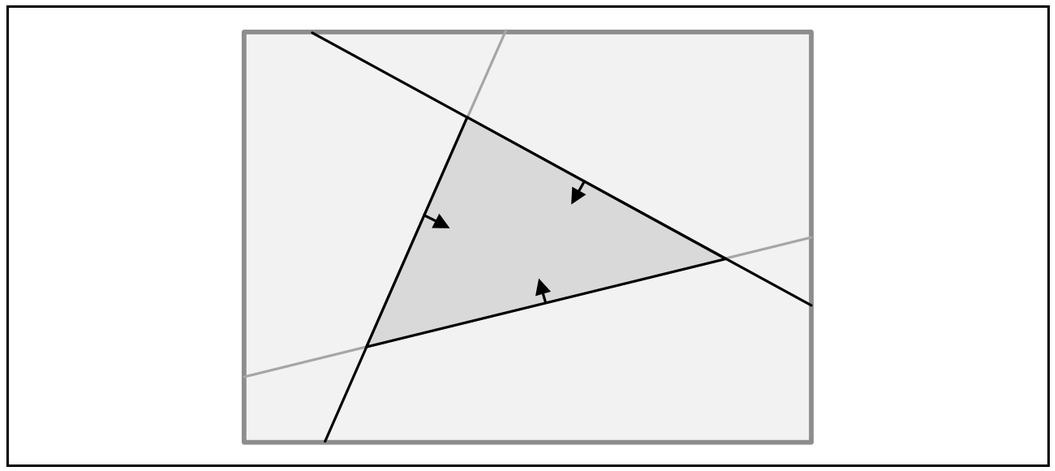


Figure 56.5 半平面的交点

限幅器输出被钳位在[0:1]的间隔内。在限幅器1和2中，可以在钳位操作之前应用带滤波器。在这种情况下，限制器不是描述一个半平面而是一个小带。使用这种方法，单个限制器可以描述无限长的粗线。

不同限制器的输出可以由组合器单元以最大或最小操作进行组合。

Maximum operation describes the union of both half planes, and minimum operation describes the intersection of both half planes. The final output is then used as an alpha value. Edge anti-aliasing can be done with no additional effort with this hardware.

To calculate the decision value for each possible pixel with a limiter, the bounding box of the object must be calculated. Then, the decision value for the top left corner of the bounding box must be calculated for each edge. Finally, the increments for a step in the x direction and a step in the y direction must be calculated. This is done by the CPU in the driver.

With this information, the 2D Drawing Engine scans the whole bounding box and calculates the decision value for every pixel incrementally. For a block diagram of the entire rasterization unit, see section 56.1, Overview.

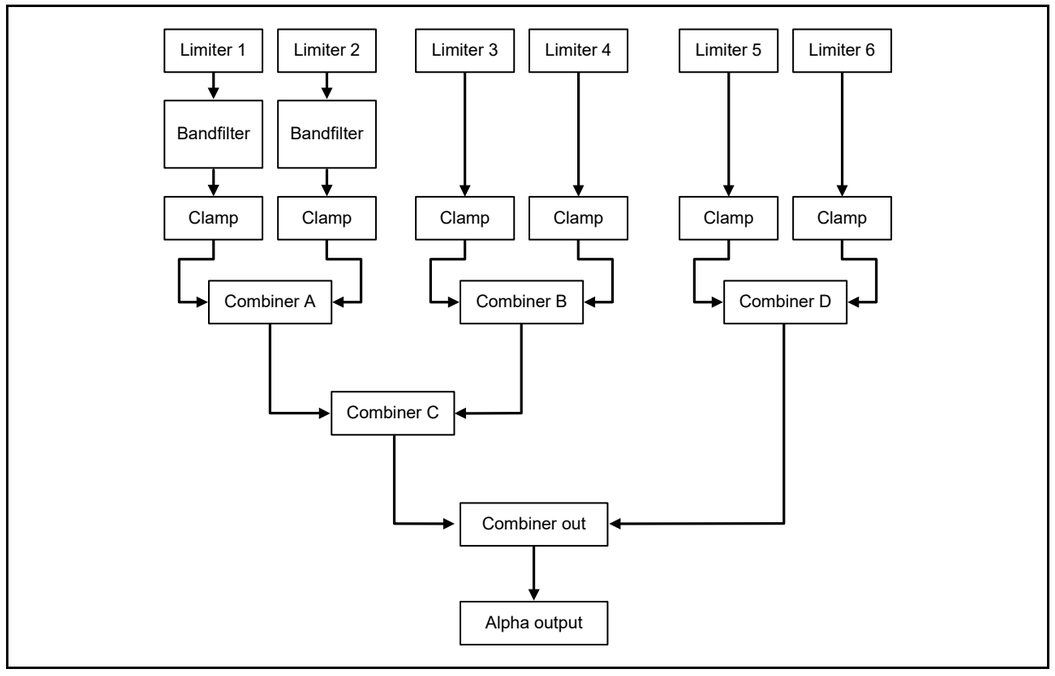


Figure 56.6 Block diagram of rasterization unit

The limiters calculate distances and the combiner units combine them to an alpha value. The combiner units define the conditions for whether or not a pixel is in the bounding box. The alpha value must be greater than 0.

Note: It is possible to have all limiters switched off.

56.6.2.1 Edge setup linear case

(1) Mathematical background

To setup a linear edge, consider the line equation in the classical form:

This can be written as:

$$y = \tilde{a}x + \tilde{b}$$

This can be rewritten as:

$$0 = f(x, y) = \tilde{a}x - y + \tilde{b} = ax + by + c$$

with $a = \tilde{a}$, $b = -1$, $c = \tilde{b}$

This is a more general form. Consider a vector form of this equation:

最大运算描述两个半平面的并集，最小运算描述两个半平面的交集。然后将最终输出用作alpha值。使用此硬件无需额外努力即可完成边缘抗锯齿。

要使用限制器计算每个可能像素的决策值，必须计算对象的边界框。
然后，必须为每条边计算边界框左上角的决策值。最后，必须计算x方向步长和y方向步长的增量。这是由驱动程序中的CPU完成的。

使用此信息，2D绘图引擎扫描整个边界框并逐步计算每个像素的决策值。有关整个光栅化单元的框图，请参阅第56.1节，概述。

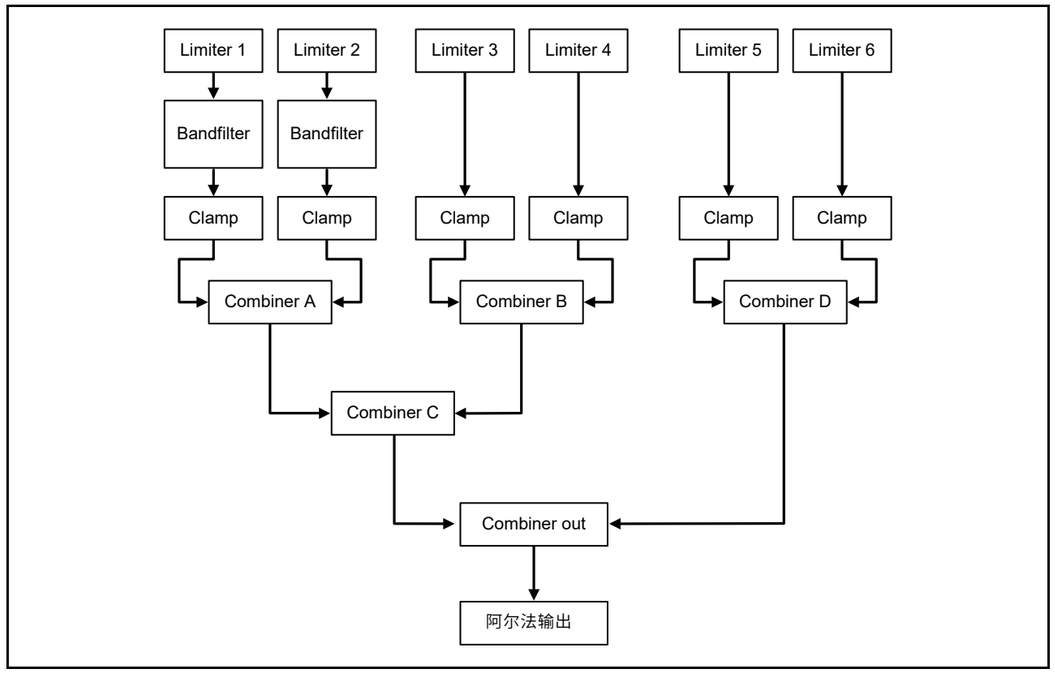


Figure 56.6 光栅化单元框图

限制器计算距离，组合器单元将它们组合成一个alpha值。组合器单元定义像素是否在边界框中的条件。alpha值必须大于0。

Note: 可以关闭所有限制器。

56.6.2.1 边缘设置线性案例

(1) 数学背景

要设置线性边缘，请考虑经典形式的线方程：

这可以写成：

$$y = \tilde{a}x + \tilde{b}$$

这可以重写为：

$$0 = f(x, y) = \tilde{a}x - y + \tilde{b} = ax + by + c$$

with $a = \tilde{a}$, $b = -1$, $c = \tilde{b}$

这是一种更一般的形式。考虑这个方程的向量形式：

$\vec{p} = \begin{pmatrix} x \\ y \end{pmatrix}, \vec{n} = \begin{pmatrix} a \\ b \end{pmatrix} \Rightarrow f(x, y) = ax + by + c = \vec{p} \cdot \vec{n} + c$

If a point $\vec{p}_0$ is on the line:

$0 = f(x, y) = \vec{p}_0 \cdot \vec{n} + c \Rightarrow c = -\vec{p}_0 \cdot \vec{n}$

Rewriting the constant, the equation becomes:

$c = -\vec{p}_0 \cdot \vec{n} \Rightarrow f(x, y) = (\vec{p} - \vec{p}_0) \cdot \vec{n}$

The vector $\vec{n}$ is called the normal vector and is perpendicular to the line. The setup can be seen in Figure 56.7.

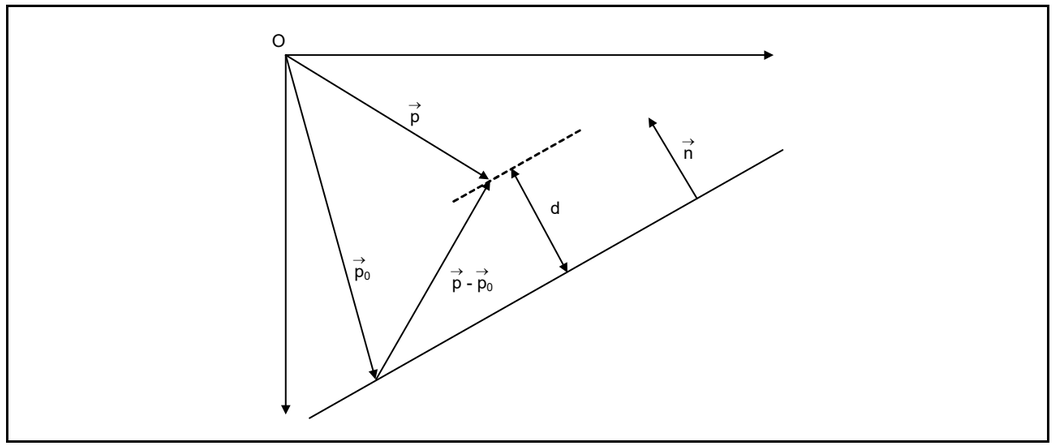


Figure 56.7 Distance of a point to a line

The projection of $\vec{p} - \vec{p}_0$ to $\vec{n}$ is the distance d of the point P to the line. In this case, f (x, y) describes the distance to the line of the pixel with coordinates (x, y).

To calculate the distance of every pixel of the bounding box incrementally, first the distance to the line at origin must be calculated:

$f(0, 0) = -\vec{p}_0 \cdot \vec{n} = c$

Next the increments for a step in the x direction and a step in the y direction must be calculated:

$f(\vec{p} + \vec{e}_x) = (\vec{p} + \vec{e}_x - \vec{p}_0) \cdot \vec{n} = f(\vec{p}) + \vec{e}_x \cdot \vec{n} = f(\vec{p}) + a$

$f(\vec{p} + \vec{e}_y) = (\vec{p} + \vec{e}_y - \vec{p}_0) \cdot \vec{n} = f(\vec{p}) + \vec{e}_y \cdot \vec{n} = f(\vec{p}) + b$

with $\vec{e}_x = \begin{pmatrix} 1 \\ 0 \end{pmatrix}, \vec{e}_y = \begin{pmatrix} 0 \\ 1 \end{pmatrix}$

Consequently, the new distance can be calculated from the old distance with the increments a and b. A step in the x direction changes the distance by a, and a step in the y direction changes the distance by b. The distance of the origin to the line is c.

With this information, the entire bounding box can be scanned. If the bounding box top left corner is not at the origin, an offset must be added.

(2) Limiter operation

The 2D Drawing Engine contains six limiters. Each limiter contains three registers:

- LnSTART
- LnXADD
- LnYADD.

See Figure 56.8 for details. It is possible to drive the limiters in a threshold mode, in which all values above 0.5 are set to 1, and all values below or equal to 0.5 are set to 0. This feature is used when anti-aliasing is not wanted.

$\vec{p} = \begin{pmatrix} x \\ y \end{pmatrix}, \vec{n} = \begin{pmatrix} a \\ b \end{pmatrix} \Rightarrow f(x, y) = ax + by + c = \vec{p} \cdot \vec{n} + c$

如果一个点 $\vec{p}_0$ 上线：

$0 = f(x, y) = \vec{p}_0 \cdot \vec{n} + c \Rightarrow c = -\vec{p}_0 \cdot \vec{n}$

改写常数，方程变为：

$c = -\vec{p}_0 \cdot \vec{n} \Rightarrow f(x, y) = (\vec{p} - \vec{p}_0) \cdot \vec{n}$

向量 $\vec{n}$ 称为法向量，垂直于直线。设置如图56.7所示。

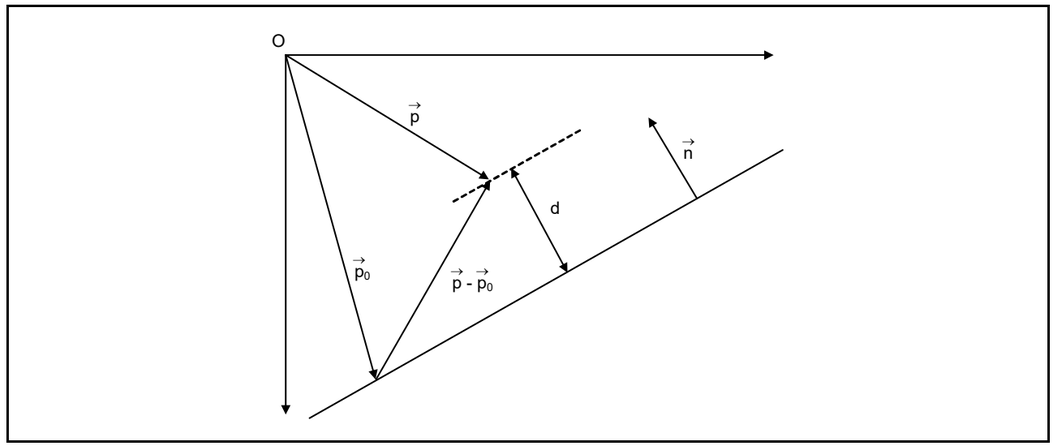


Figure 56.7 点到线的距离

to是点P到直线的距离d。在这种情况下，f(x y)用坐标(x y)描述像素到直线的距离。

要增量计算边界框每个像素的距离，首先必须计算到原点线的距离：

$f(0, 0) = -\vec{p}_0 \cdot \vec{n} = c$

接下来，必须计算x方向的步长和y方向的步长：

$f(\vec{p} + \vec{e}_x) = (\vec{p} + \vec{e}_x - \vec{p}_0) \cdot \vec{n} = f(\vec{p}) + \vec{e}_x \cdot \vec{n} = f(\vec{p}) + a$

$f(\vec{p} + \vec{e}_y) = (\vec{p} + \vec{e}_y - \vec{p}_0) \cdot \vec{n} = f(\vec{p}) + \vec{e}_y \cdot \vec{n} = f(\vec{p}) + b$

with $\vec{e}_x = \begin{pmatrix} 1 \\ 0 \end{pmatrix}, \vec{e}_y = \begin{pmatrix} 0 \\ 1 \end{pmatrix}$

因此，新的距离可以从旧距离以增量a和b计算。在x方向上的一步将距离更改a，在y方向上的一步将距离更改为b。原点到直线的距离为c。

有了这些信息，就可以扫描整个边界框。如果边界框左上角不在原点，则必须添加偏移量。

(2) 限制器操作

2D绘图引擎包含六个限制器。每个限制器包含三个寄存器：

- LnSTART
- LnXADD
- LnYADD.

详见图56.8。可以在阈值模式下驱动限制器，其中所有高于0.5的值都设置为1，所有低于或等于0.5的值都设置为0。当不需要抗锯齿时使用此功能。

Note: In Figure 56.8, the following abbreviations are used:
start = LnSTART
xadd = LnXADD
yadd = LnYADD

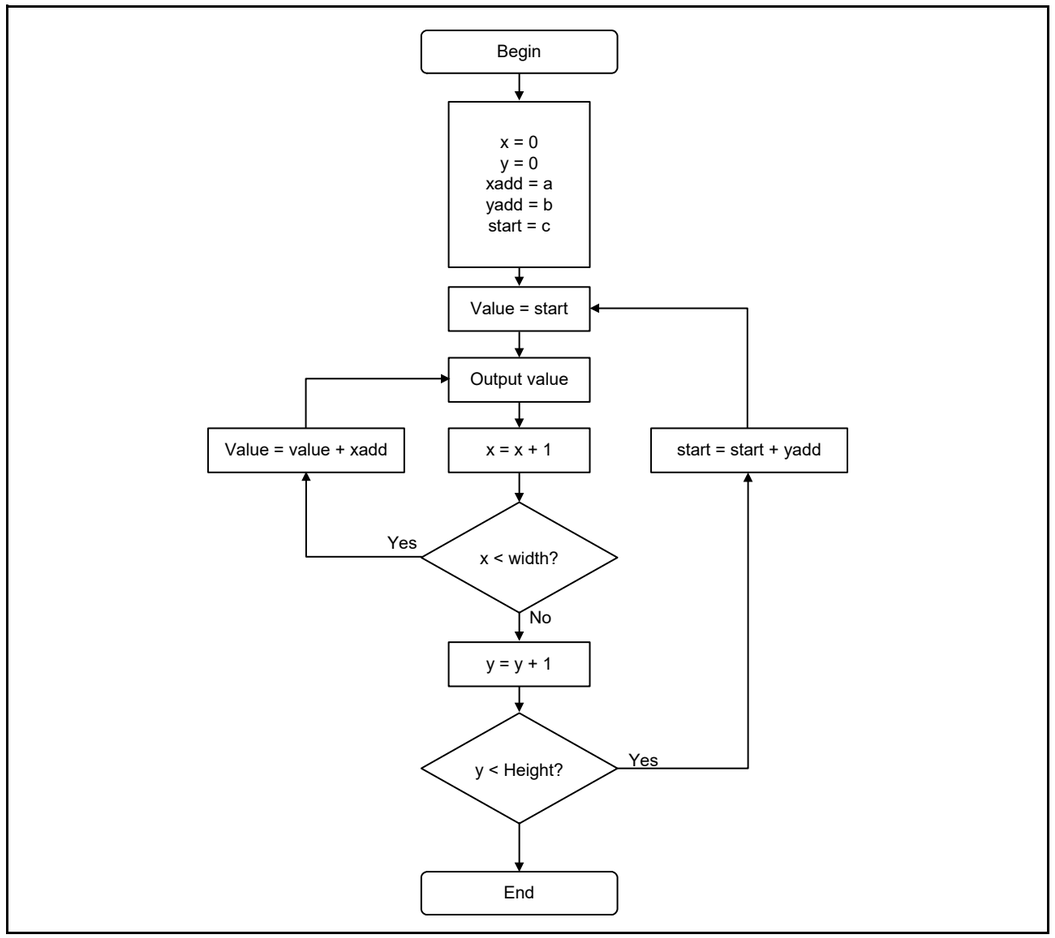


Figure 56.8 Operation flow of the linear limiter

(3) Example

If a straight line is given by the points P0 and P1, then the values are calculated as follows:

$$\Delta\vec{p} = \vec{p}_1 - \vec{p}_0 = \begin{pmatrix} x_1 - x_0 \\ y_1 - y_0 \end{pmatrix} = \begin{pmatrix} \Delta x \\ \Delta y \end{pmatrix}$$

The normal vector (perpendicular but not unit size) is then:

$$\vec{n} = \begin{pmatrix} -\Delta y \\ \Delta x \end{pmatrix}$$

The not normalized distance between edge and origin is then:

$$\vec{p}_0 \cdot \vec{n} = -x_0\Delta y + y_0\Delta x$$

The limiter parameters would be:

$$start = -x_0\Delta y + y_0\Delta x$$

Note: 在图56.8中，使用了以下缩写：start=LnSTARTxadd =LnXADDyadd=LnYADD

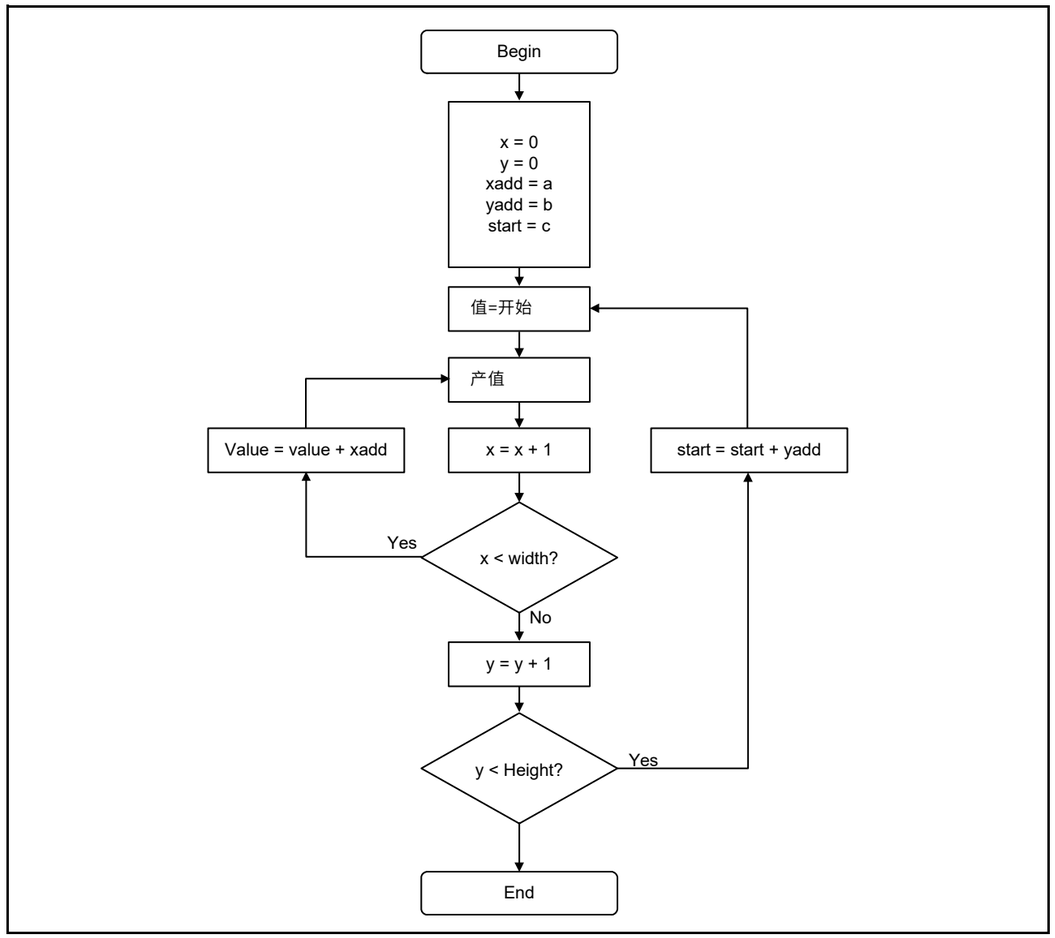


Figure 56.8 线性限幅器的操作流程

(3) Example

如果由点P0和P1给出一条直线，则值计算如下：

$$\Delta\vec{p} = \vec{p}_1 - \vec{p}_0 = \begin{pmatrix} x_1 - x_0 \\ y - y \end{pmatrix} = \begin{pmatrix} \Delta x \\ \Delta y \end{pmatrix}$$

法线向量（垂直但不是单位大小）为：

$$\vec{n} = \begin{pmatrix} -\Delta y \\ \Delta x \end{pmatrix}$$

那么边缘和原点之间的非标准化距离是：

$$\vec{p}_0 \cdot \vec{n} = -x_0\Delta y + y_0\Delta x$$

限制器参数为：

$$start = -x_0\Delta y + y_0\Delta x$$

$xadd = -\Delta y$

$yadd = \Delta x$

In the normalized case, the normal vector is:

$\vec{n} = \begin{pmatrix} -\Delta y \\ \Delta x \end{pmatrix} / (\sqrt{\Delta x^2 + \Delta y^2})$

The distance between edge and origin is:

$\vec{p}_0 \cdot \vec{n} = (-x_0 \cdot \Delta y + y_0 \cdot \Delta x) / (\sqrt{\Delta x^2 + \Delta y^2})$

The limiter parameters would be:

$start = (-x_0 \Delta y + y_0 \Delta x) / (\sqrt{\Delta x^2 + \Delta y^2})$

$xadd = -\Delta y / (\sqrt{\Delta x^2 + \Delta y^2})$

$yadd = \Delta x / (\sqrt{\Delta x^2 + \Delta y^2})$

Normalization is only required if anti-aliasing is used. The driver contains an optimized inverse square root function to speed up the normalization process.

56.6.2.2 Edge setup quadratic case

(1) Mathematical background

It is also possible to set up the limiters to incrementally calculate the following equation:

$f(x, y) = ax^2 + by^2 + cx + dy + f$

At the origin, the value is:

$f(0, 0) = f$

The step in the x direction is:

$f(x + 1, y)$

$= a(x + 1)^2 + by^2 + c(x + 1) + dy + f$

$= ax^2 + 2ax + a + by^2 + cx + c + dy + f$

$= f(x, y) + 2ax + c + a$

$dx(x) = f(x + 1, y) - f(x) = 2ax + c + a$

The step in the y direction is:

$f(x, y + 1)$

$= ax^2 + b(y + 1)^2 + cx + d(y + 1) + f$

$= ax^2 + by^2 + 2by + b + cx + d(y + 1) + f$

$= f(x, y) + 2bx + b$

$dy(y) = f(x + 1, y) - f(x) = 2by + d + b$

In the quadratic case, the increments dx and dy depend on x and y and are not constant. They can be calculated incrementally:

$d^2x = dx(x + 1) - dx(x) = 2a(x + 1) + c + 1 - (2ax + c + 1) = 2a$

$d^2y = dy(y + 1) - dy(y) = 2b(y + 1) + d + 1 - (2by + d + 1) = 2b$

At the origin, the increments are:

$dx(0) = c + 1$ and $dy(0) = d + 1$

By incrementing the value by dx and dy for every step in the x and y direction and incrementing dx, dy by d^2x, and d^2y for every step in the x and y direction, the quadratic equation can be easily calculated for the whole bounding box.

$xadd = -\Delta y$

$yadd = \Delta x$

在归一化的情况下，法向量是：

$\vec{n} = \begin{pmatrix} -\Delta y \\ \Delta x \end{pmatrix} / (\sqrt{\Delta x^2 + \Delta y^2})$

边缘到原点的距离为：

$\vec{p}_0 \cdot \vec{n} = (-x_0 \cdot \Delta y + y_0 \cdot \Delta x) / (\sqrt{\Delta x^2 + \Delta y^2})$

限制器参数为：

$start = (-x_0 \Delta y + y_0 \Delta x) / (\sqrt{\Delta x^2 + \Delta y^2})$

$xadd = -\Delta y / (\sqrt{\Delta x^2 + \Delta y^2})$

$yadd = \Delta x / (\sqrt{\Delta x^2 + \Delta y^2})$

仅当使用抗锯齿时才需要规范化。该驱动程序包含一个优化的平方根反函数，以加快标准化过程。

56.6.2.2 边缘设置二次案例

(1) 数学背景

也可以设置限制器以增量计算以下等式：

$f(x, y) = ax^2 + by^2 + cx + dy + f$

在原点，值为：

$f(0, 0) = f$

x方向的步长为：

$f(x + 1, y)$

$= a(x + 1)^2 + by^2 + c(x + 1) + dy + f$

$= ax^2 + 2ax + a + by^2 + cx + c + dy + f$

$= f(x, y) + 2ax + c + a$

$dx(x) = f(x + 1, y) - f(x) = 2ax + c + a$

y方向的步长为：

$f(x, y + 1)$

$= ax^2 + b(y + 1)^2 + cx + d(y + 1) + f$

$= ax^2 + by^2 + 2by + b + cx + d(y + 1) + f$

$= f(x, y) + 2bx + b$

$dy(y) = f(x + 1, y) - f(x) = 2by + d + b$

在二次情况下，增量dx和dy取决于x和y并且不是常数。它们可以增量计算：

$d^2x = dx(x + 1) - dx(x) = 2a(x + 1) + c + 1 - (2ax + c + 1) = 2a$

$d^2y = dy(y + 1) - dy(y) = 2b(y + 1) + d + 1 - (2by + d + 1) = 2b$

在原点，增量为：

$dx(0) = c + 1$ and $dy(0) = d + 1$

通过在x和y方向上每一步增加dx和dy的值，并在x和y方向上每一步增加dx、dy和d2x和d2y，可以很容易地计算出二次方程整个边界框。

(2) Limiter operation

In the quadratic case, two linear limiters are combined to operate as one quadratic limiter, called limiter 1 and limiter 2. The registers are:

- L1START, L1XADD, L1YADD
- L2START, L2XADD, L2YADD.

See Figure 56.9 for details. The gray box is an addition that performs a different operation, as in the linear setup. It is possible to drive the limiters in a threshold mode, in which all values above 0.5 are set to 1, and all values below or equal to 0.5 are set to 0. This feature is used when anti-aliasing is not wanted.

Note: In Figure 56.9, the following abbreviations are used:

- start1 = L1START, start2 = L2START
- xadd1 = L1XADD, xadd2 = L2XADD
- yadd1 = L1YADD, yadd2 = L2YADD.

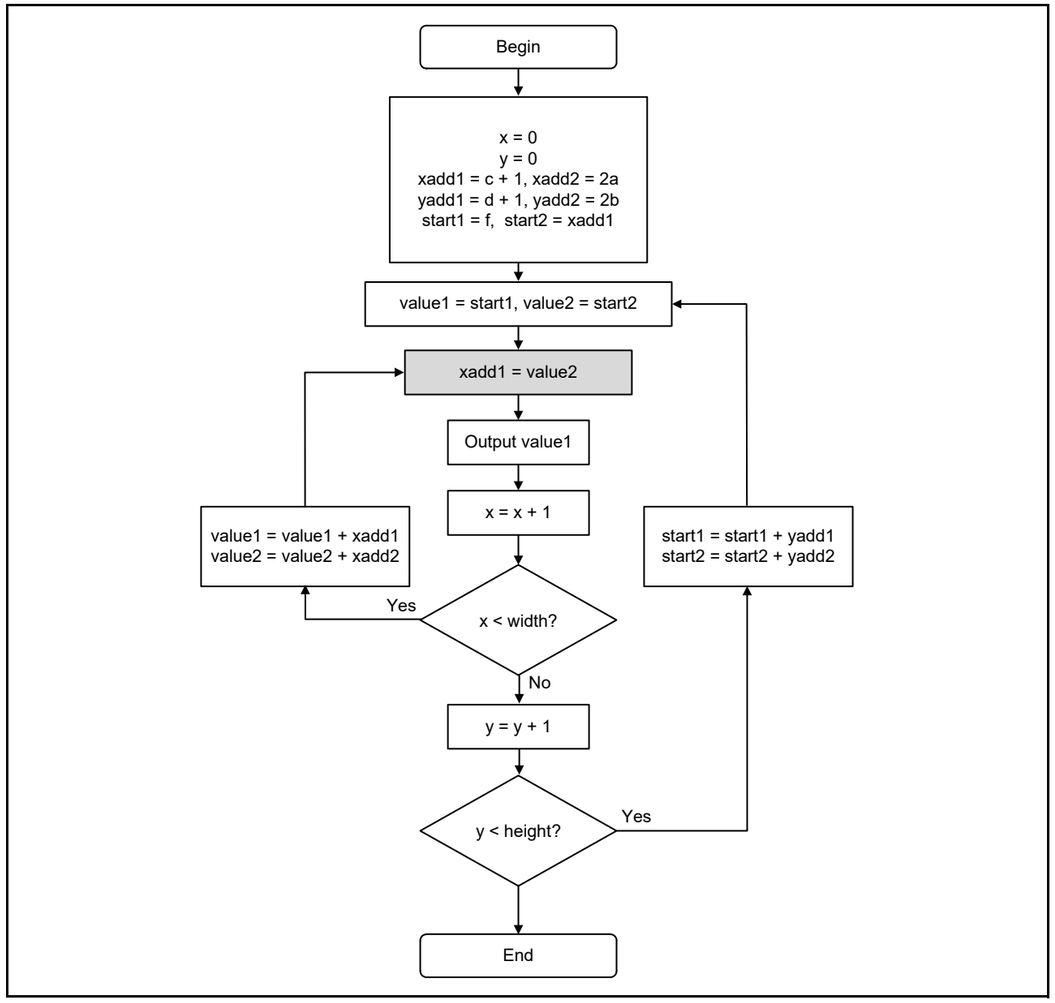


Figure 56.9 Operation flow of the quadratic limiter

(2) 限制器操作

在二次情况下，两个线性限制器组合起来作为一个二次限制器运行，称为限制器1和限制器2。
寄存器是：

- L1START, L1XADD, L1YADD
- L2START, L2XADD, L2YADD.

有关详细信息，请参见图56.9。灰色框是执行不同操作的附加项，如在线性设置中。可以在阈值模式下驱动限制器，其中所有高于0.5的值都设置为1，所有低于或等于0.5的值都设置为0。当不需要抗锯齿时使用此功能。

Note: 在图56.9中，使用了以下缩写：

- start1 = L1START, start2 = L2START
- xadd1 = L1XADD, xadd2 = L2XADD
- yadd1 = L1YADD, yadd2 = L2YADD.

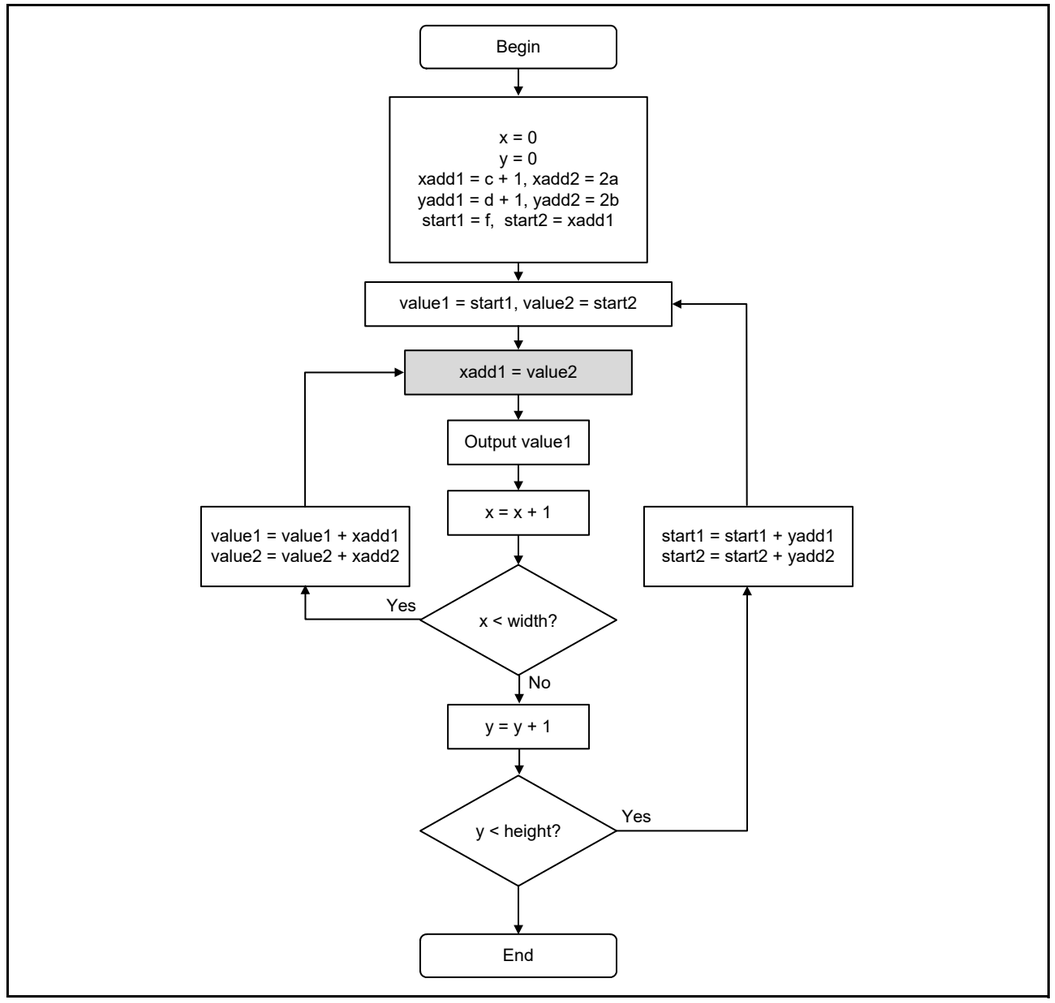


Figure 56.9 二次限幅器的操作流程

(3) Example

Consider the equation for a circle with the center at $\vec{c} = \begin{pmatrix} s \\ t \end{pmatrix}$ and radius r:

$$0 = f(x, y) = (x - s)^2 + (y - t)^2 - r^2$$

This equation can be rewritten as:

$$f(x, y) = x^2 - 2xs + s^2 + y^2 - 2yt + t^2 - r^2$$

This can be sorted to fit to the original equation:

$$f(x, y) = x^2 + y^2 - 2sx - 2ty + (s^2 + t^2 - r^2)$$

With the following assignments, the circle equation can be calculated incrementally:

$$a = 1$$

$$b = 1$$

$$c = -2s$$

$$d = -2t$$

$$f = s^2 + t^2 - r^2$$

For the limiters with the results calculated in (1) Mathematical background, this would result in:

$$start1 = f = s^2 + t^2 - r^2$$

$$xadd1 = c + 1 = -2s + 1$$

$$yadd1 = d + 1 = -2t + 1$$

$$start2 = xadd1$$

$$xadd2 = 2a = 2$$

$$yadd2 = 2b = 2$$

56.6.2.3 Band filter

The output of limiter 1 and 2 can be modified to use a band filter. The band filter has a single filter parameter w.

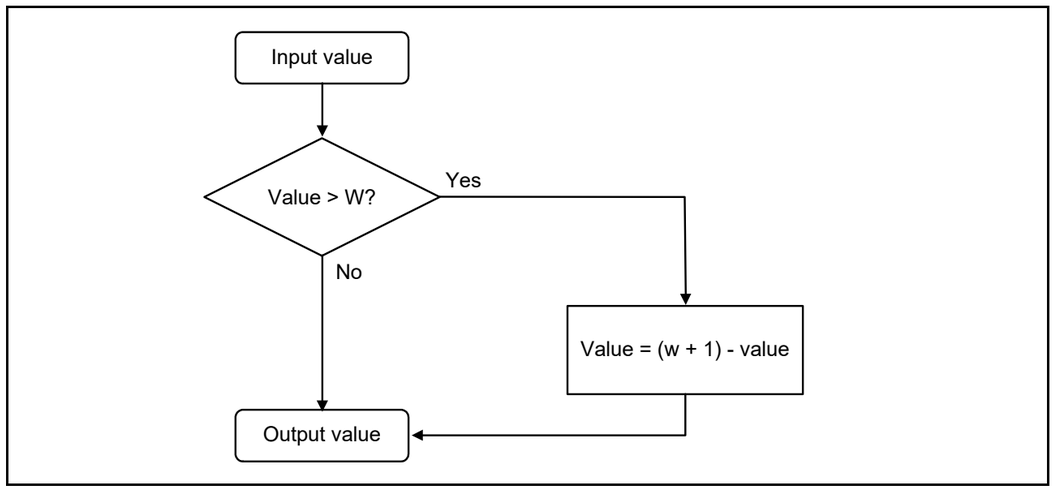


Figure 56.10 Band filter

(3) Example

考虑圆心为的圆的方程 $\vec{c} = \begin{pmatrix} s \\ t \end{pmatrix}$ 和半径r：

$$0 = f(x, y) = (x - s)^2 + (y - t)^2 - r^2$$

这个方程可以改写为：

$$f(x, y) = x^2 - 2xs + s^2 + y^2 - 2yt + t^2 - r^2$$

这可以排序以适合原始方程：

$$f(x, y) = x^2 + y^2 - 2sx - 2ty + (s^2 + t^2 - r^2)$$

通过以下分配，可以增量计算圆方程：

$$a = 1$$

$$b = 1$$

$$c = -2s$$

$$d = -2t$$

$$f = s^2 + t^2 - r^2$$

对于在(1)数学背景中计算结果的限制器，这将导致：

$$start1 = f = s^2 + t^2 - r^2$$

$$xadd1 = c + 1 = -2s + 1$$

$$yadd1 = d + 1 = -2t + 1$$

$$start2 = xadd1$$

$$xadd2 = 2a = 2$$

$$yadd2 = 2b = 2$$

56.6.2.3 带式滤波器

限幅器1和2的输出可以修改为使用带状滤波器。带状滤波器只有一个滤波器参数w。

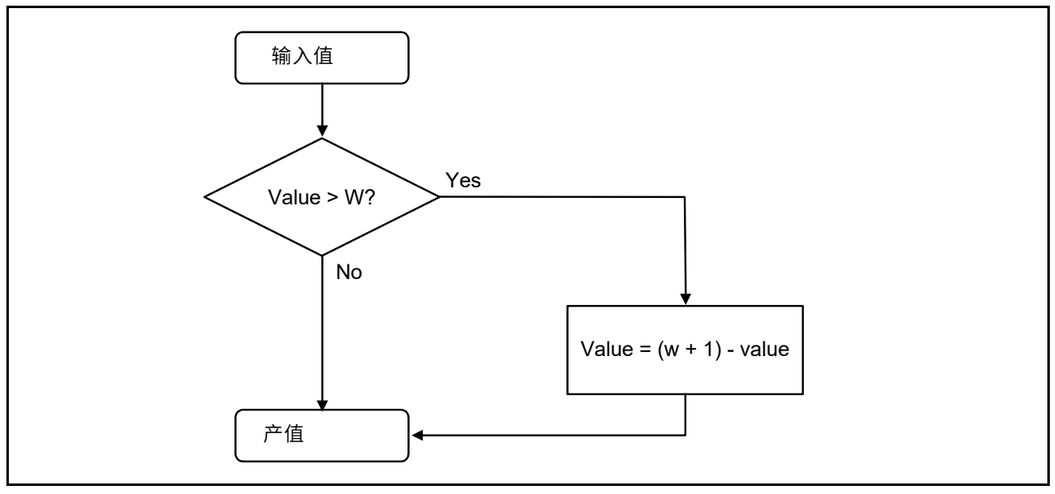


Figure 56.10 带式滤波器

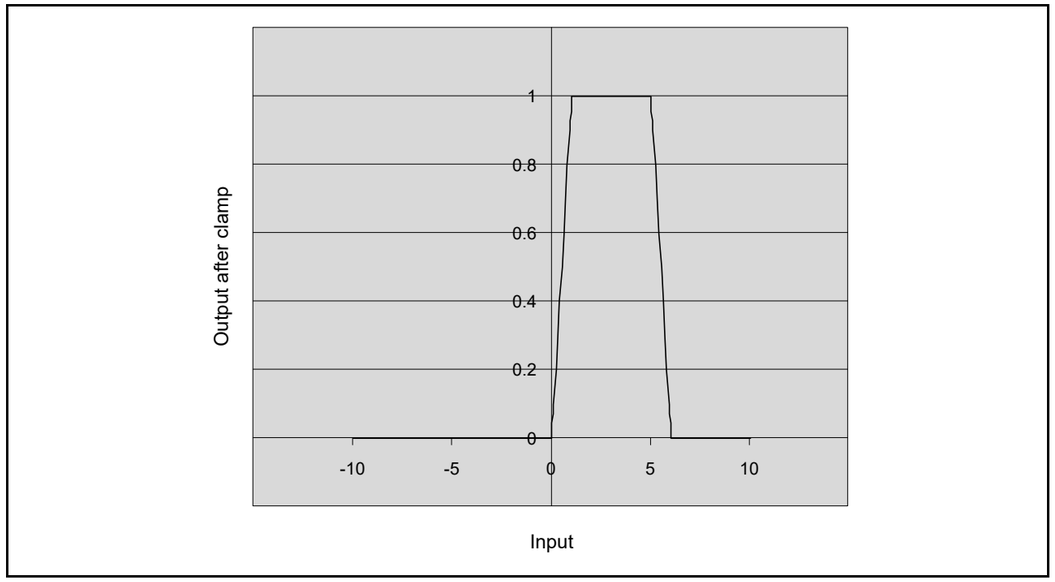


Figure 56.11 Band filter output after clamp with w = 7

56.6.2.4 Clamping unit

The clamping unit cuts the limiter output to the interval [0:1].

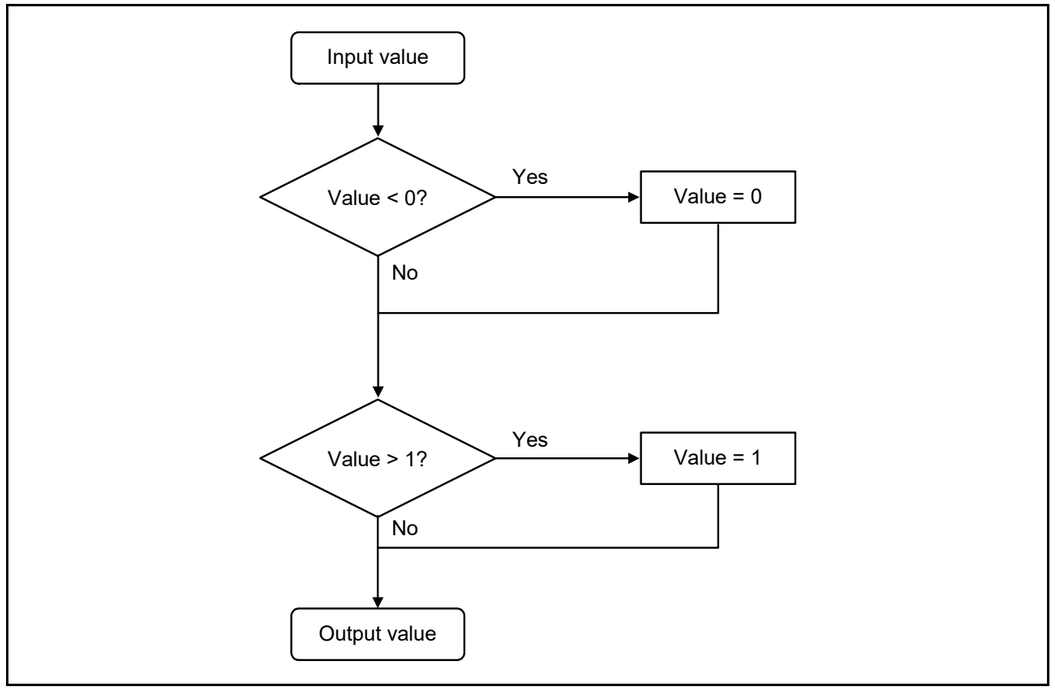


Figure 56.12 Clamping unit

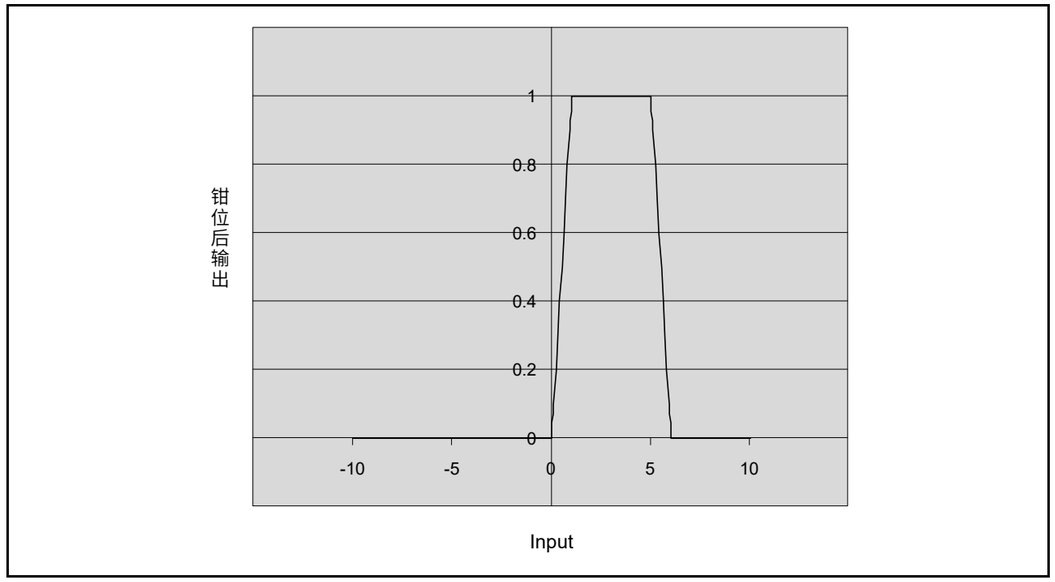


Figure 56.11 w=7钳位后的带状滤波器输出

56.6.2.4 夹紧单元

钳位单元将限制器输出切割到区间[0:1]。

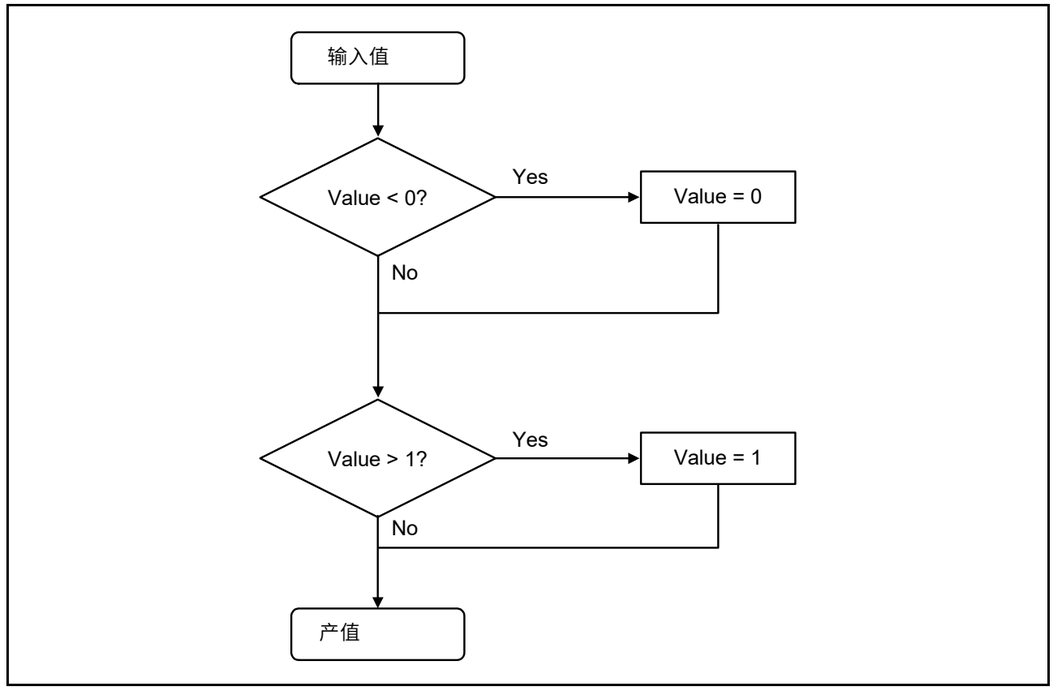


Figure 56.12 夹紧单元

The clamping unit can be put into threshold mode, in which all values greater than 0.5 are set to 1, and all values below or equal to 0.5 are set to 0. This feature is used when anti-aliasing is not wanted, such as for shared edges.

56.6.2.5 Combiner unit

The combiner unit can be operated in minimum mode and in maximum mode. In minimum mode the smaller value is output, and in maximum mode the larger value is output. The minimum mode represents the intersection, and the maximum mode represents the union of the two regions.

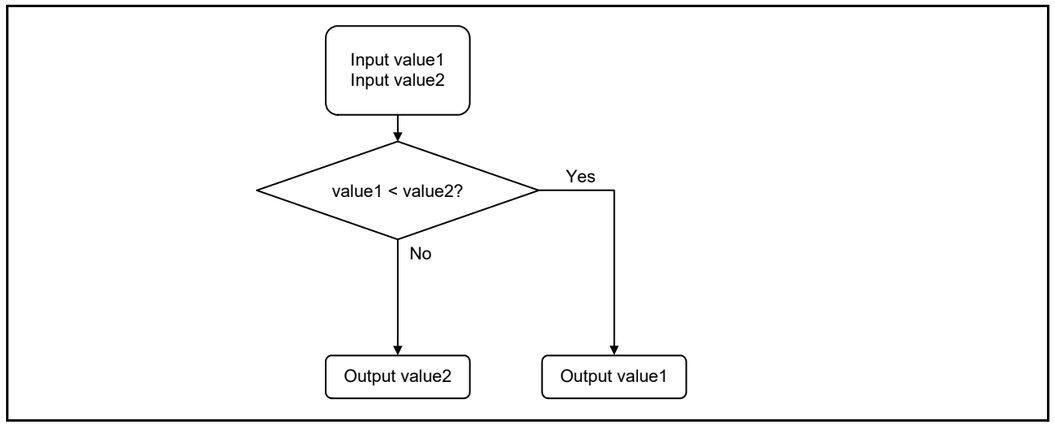


Figure 56.13 Combiner operated in minimum mode with intersection

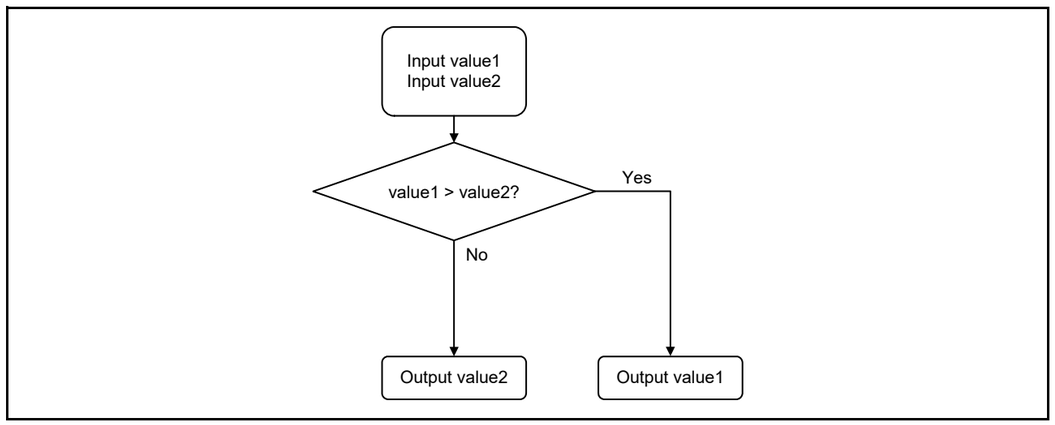


Figure 56.14 Combiner operated in maximum mode with union

56.6.2.6 Rasterization optimization

During rasterization, it is necessary to step through the whole bounding box one pixel at a time. This requirement can lead to an unnecessary number of steps for pixels that are not drawn. The 2D Drawing Engine provides optimization methods designed to reduce the number of steps required during rasterization. One optimization relies on the fact that any convex primitive can have only one span per line (a span is a contiguous horizontal line). This form of optimization detects a span start and saves the information for the next line. Another optimization is to detect a span end and stop rasterization for the current line.

(1) Spanstore

Consider the case in Figure 56.15.

钳位单元可以设置为阈值模式，所有大于0.5的值都设置为1，所有小于或等于0.5的值都设置为0。此功能用于不需要抗锯齿的情况，例如共享边。

56.6.2.5 Combiner unit

组合器单元可以在最小模式和最大模式下运行。在最小模式下输出较小的值，在最大模式下输出较大的值。最小众数代表相交，最大众数代表两个区域的并集。

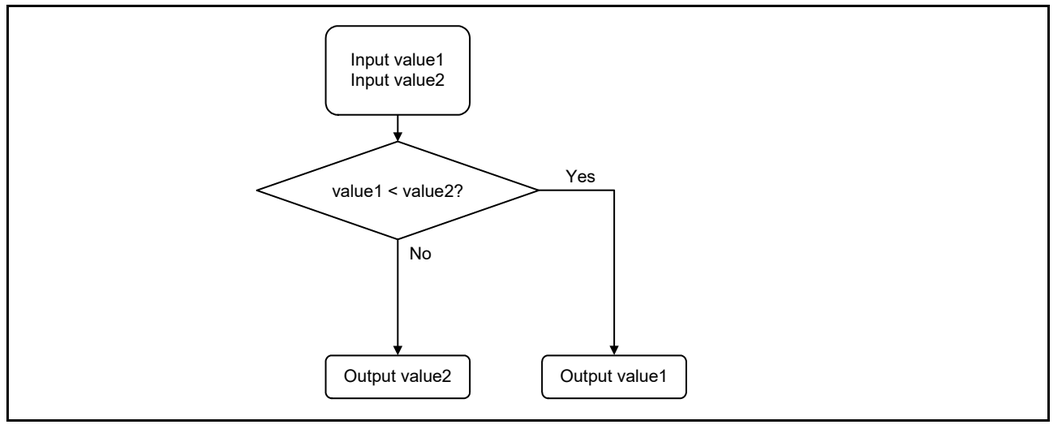


Figure 56.13 合路器以最小模式运行，有交叉口

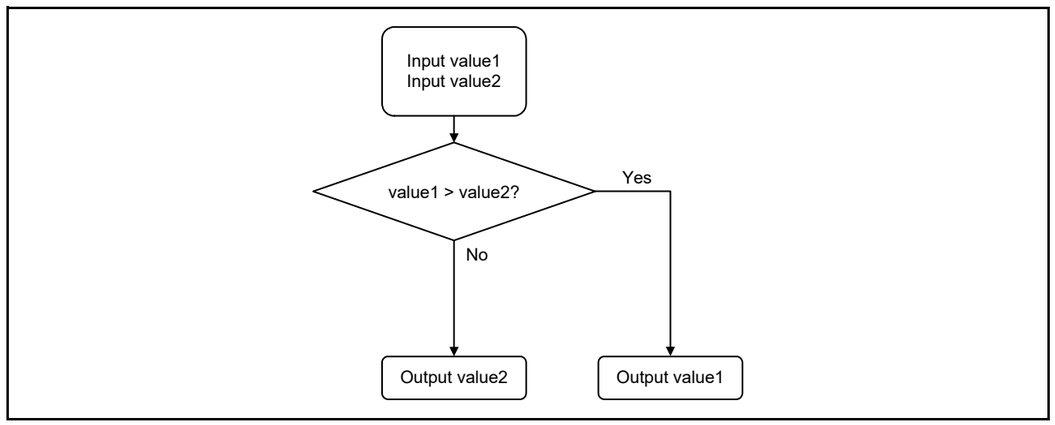


Figure 56.14 组合器在最大模式下运行，带联合

56.6.2.6 Rasterization optimization

在光栅化过程中，需要一次一个像素地遍历整个边界框。对于未绘制的像素，此要求可能会导致不必要的步数。2D绘图引擎提供了旨在减少光栅化过程中所需步骤数量的优化方法。一种优化依赖于这样一个事实，即任何凸图元每条线只能有一个跨度（跨度是一条连续的水平线）。这种优化形式检测跨度开始并保存下一行的信息。另一个优化是检测跨度结束并停止当前行的光栅化。

(1) Spanstore

考虑图56.15中的情况。

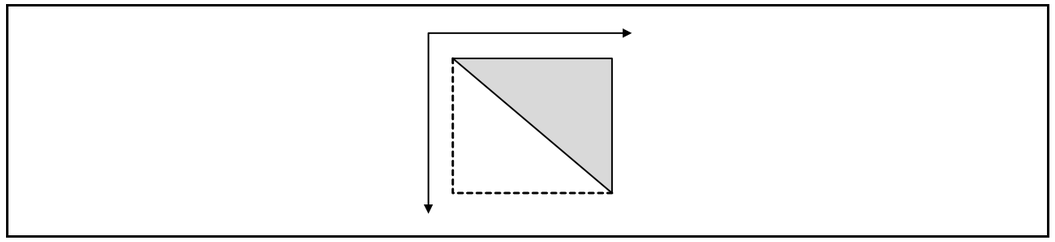


Figure 56.15 Triangle where the first edge is monotone growing

If the gray triangle must be rendered, half of the pixels processed by the rendering engine in the dotted bounding box would not be drawn. This situation can be optimized with the spanstore operation. When spanstore is activated and a span start is detected, the x position of the span start is detected.

In the next line the rendering starts with the stored x position. This only works if the edge is monotonically increasing ($y_1 > y_2 \Rightarrow x_1 \geq x_2$).

Consider the case in Figure 56.16.

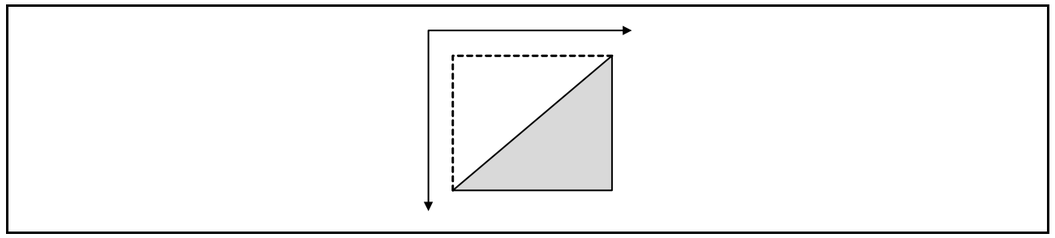


Figure 56.16 Triangle where the first edge is monotone falling

In this case, the normal spanstore operation cannot be performed. For this, the y direction of the rendering is reversed, and spanstore can operate again.

Consider the last case in Figure 56.17.

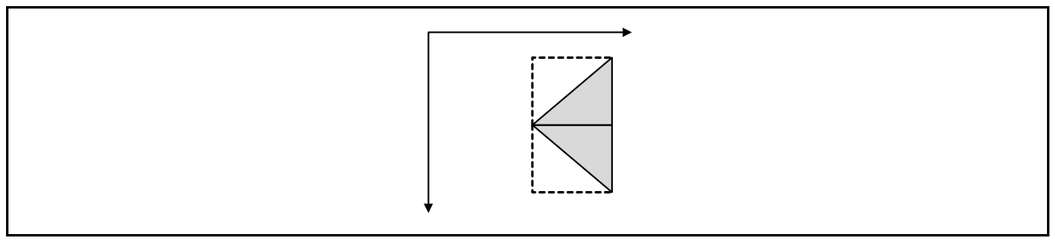


Figure 56.17 Triangle where the first edge is first monotone falling and then monotone growing

In this case, the triangle must be split and rendered as two parts for the spanstore optimization to work.

It is also possible to delay spanstore activation for a number of lines. This approach is used for rasterizing circles, as shown in Figure 56.18.

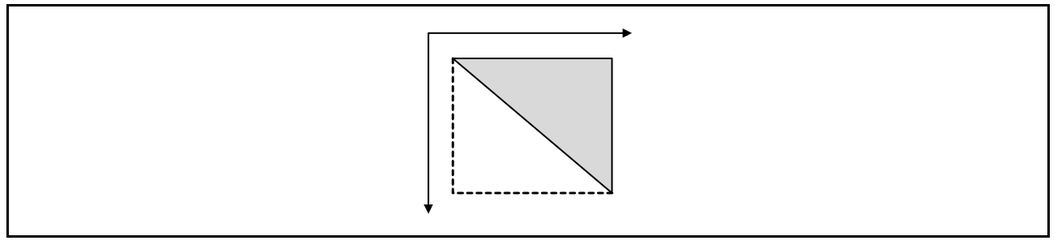


Figure 56.15 第一条边单调增长的三角形

如果必须渲染灰色三角形，虚线框内的渲染引擎处理过的像素有一半不会被绘制出来。这种情况可以通过spanstore操作进行优化。当spanstore被激活并检测到spanstart时，将检测到spanstart的x位置。

在下一行中，渲染从存储的x位置开始。这仅适用于边缘单调递增(y1>y2=>x1　x2)。

考虑图56.16中的情况。

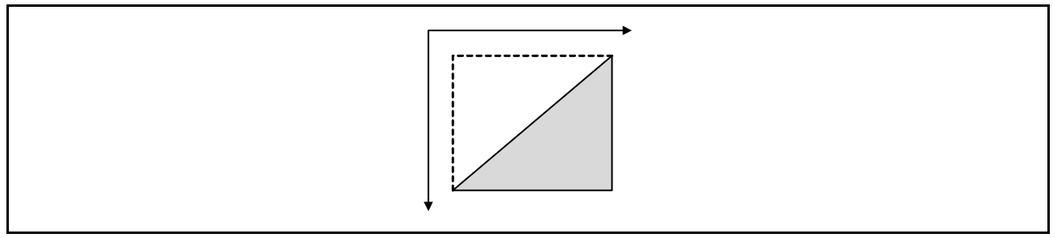


Figure 56.16 第一个边单调下降的三角形

在这种情况下，无法执行正常的spanstore操作。为此，将渲染的y方向反转，spanstore可以再次操作。

考虑图56.17中的最后一种情况。

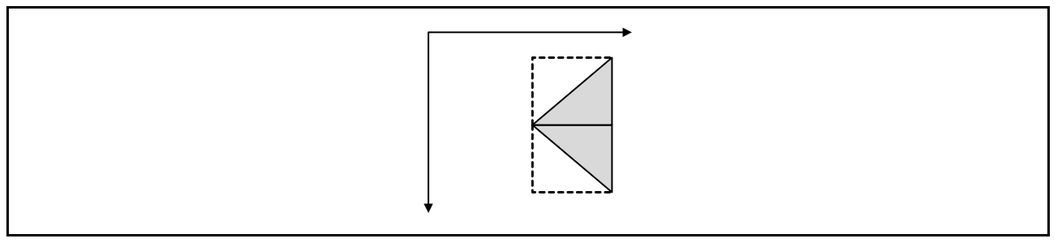


Figure 56.17 第一个边先单调下降然后单调增长的三角形

在这种情况下，必须将三角形分割并渲染为两部分，才能使spanstore优化起作用。

也可以延迟多行的spanstore激活。这种方法用于光栅化圆，如图56.18所示。

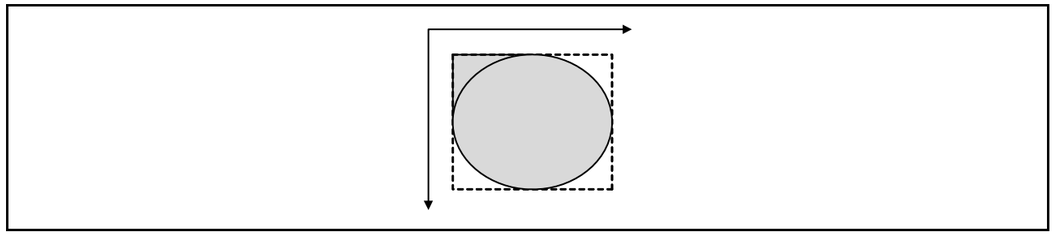


Figure 56.18 Full circle where the first edge is monotone falling for the first half and monotone growing for the second half

In this case, spanstore cannot be activated in the top left corner but can be activated in the bottom left corner. The empty corners in the top right and the bottom right cannot be rasterized because of the spanabort optimization.

(2) Spanabort

The second optimization assumes that the object that must be drawn is convex, which means there is only one span per scan line to be drawn. A non-convex object includes an object such as a triangle that is not filled and only consists of a thick border.

For a convex object, the rasterization can be stopped when the end of the first span is detected. No other constraints apply to this optimization for convex objects.

(3) Optimization efficiency

The efficiency of the optimizations can be seen for a typical case in Figure 56.19. In this case, the triangle is always rendered as single piece and is not separated into multiple triangles for higher optimizations. For this, the spanstore delay is used.

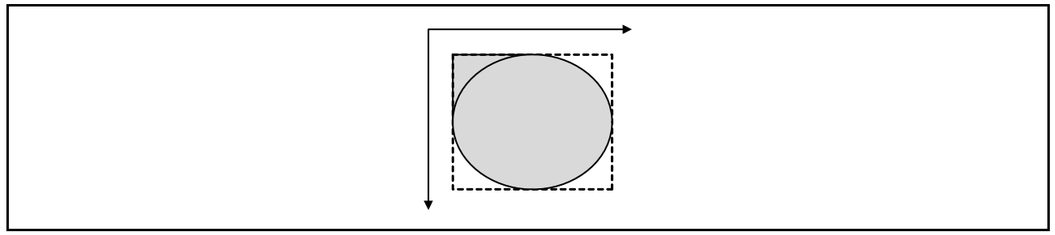


Figure 56.18 第一个边缘是前半部分单调下降和后半部分单调增长的完整圆

在这种情况下，spanstore不能在左上角激活，但可以在左下角激活。由于spanabort优化，右上角和右下角的空角无法栅格化。

(2) Spanabort

第二个优化假设必须绘制的对象是凸的，这意味着每条扫描线只有一个跨度要绘制。非凸对象包括诸如未填充且仅由粗边框组成的三角形的对象。

对于凸对象，当检测到第一个跨度结束时，可以停止光栅化。没有其他约束适用于凸对象的这种优化。

(3) 优化效率

对于图56.19中的典型案例，可以看到优化的效率。在这种情况下，三角形始终呈现为单件，并且不会分成多个三角形以进行更高的优化。为此，使用了spanstore延迟。

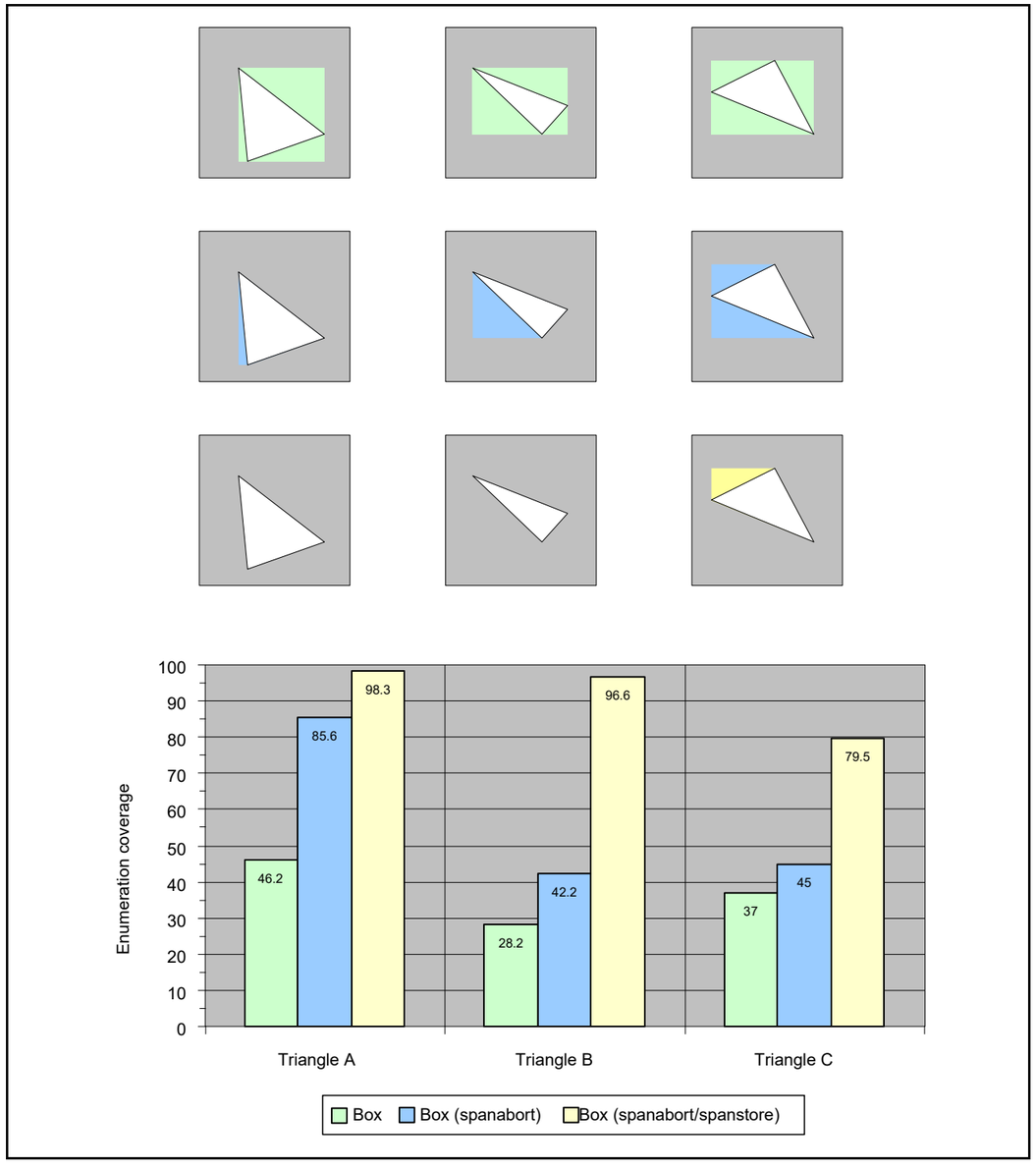


Figure 56.19 Efficiency of spanstore and spanabort optimizations with enumeration coverage equal to {pixels of primitive/pixels of bounding box}

56.6.3 Texturing

The texture unit can cover any primitive with a picture. The picture can be stretched, sheared, rotated, and translated in one step. To avoid aliasing, the result can be filtered bilinear in the u and v directions.

56.6.3.1 Mathematical background

The arbitrary mapping problem is completely determined by a mapping from 3 points in the object space (x, y) to 3 points in the texture space (u, v).

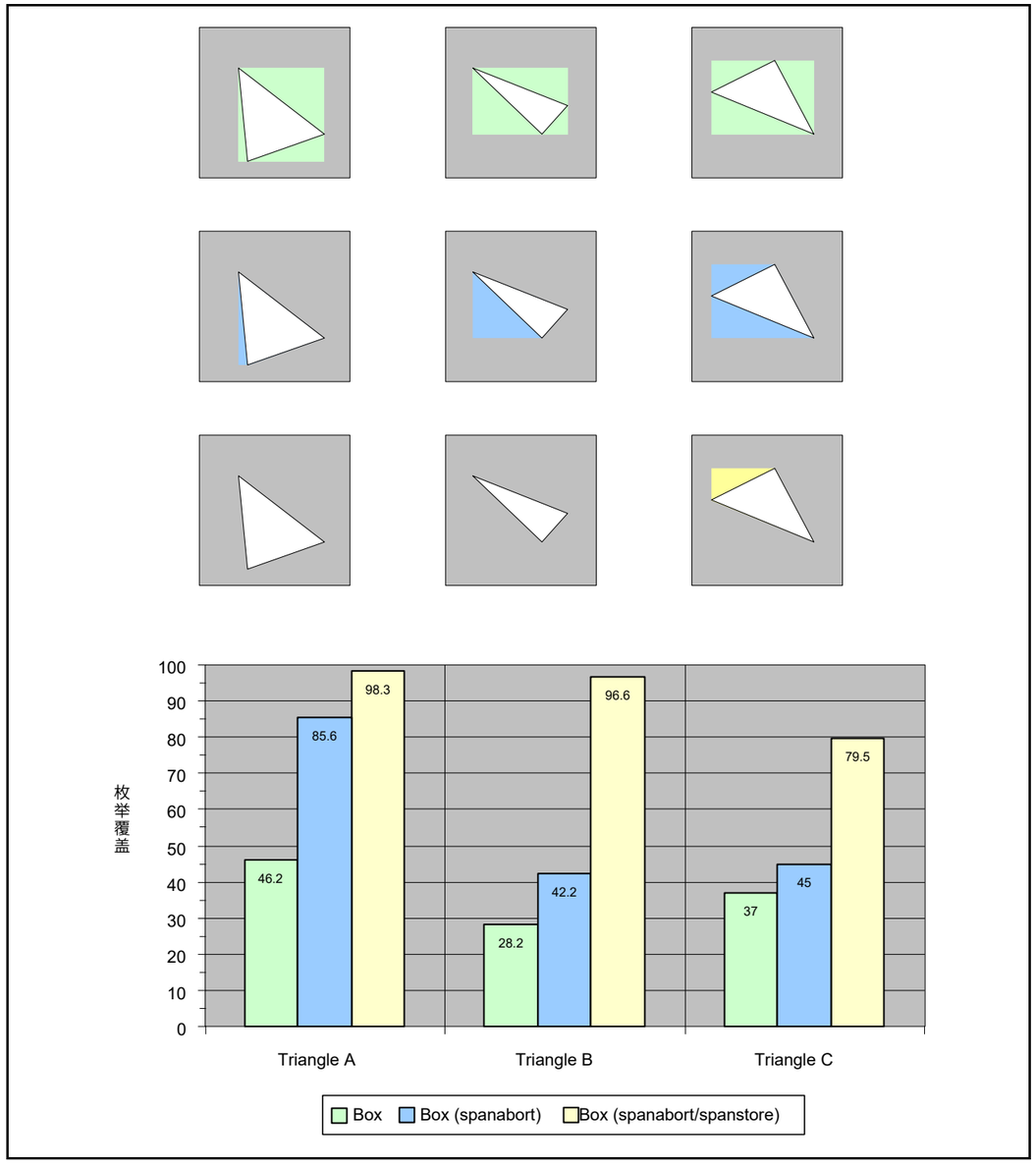


Figure 56.19 枚举覆盖率等于{boundingbox的原始像素的像素 的spanstore和spanabort优化的效率

56.6.3 Texturing

纹理单元可以覆盖任何带有图片的图元。图片可以在一个步骤中进行拉伸、剪切、旋转和平移。为了避免混叠，可以在u和v方向对结果进行双线性过滤。

56.6.3.1 数学背景

任意映射问题完全由对象空间中的3个点(x y)到纹理空间中的3个点(u v)的映射决定。

Consider the following mapping:

$$\vec{p}_0 = \begin{pmatrix} x_0 \\ y_0 \end{pmatrix} \Rightarrow (\tilde{\vec{p}}_0) = \begin{pmatrix} u_0 \\ v_0 \end{pmatrix} = \begin{pmatrix} 0 \\ 0 \end{pmatrix}$$

$$\vec{p}_1 = \begin{pmatrix} x_1 \\ y_1 \end{pmatrix} \Rightarrow (\tilde{\vec{p}}_1) = \begin{pmatrix} u_1 \\ v_1 \end{pmatrix} = \begin{pmatrix} w \\ 0 \end{pmatrix}$$

$$\vec{p}_2 = \begin{pmatrix} x_2 \\ y_2 \end{pmatrix} \Rightarrow (\tilde{\vec{p}}_2) = \begin{pmatrix} u_2 \\ v_2 \end{pmatrix} = \begin{pmatrix} 0 \\ h \end{pmatrix}$$

where w is the width of the texture and h is the height of the texture.

Examine Figure 56.20 in the object space. To simplify calculations the difference vectors are taken as calculations:

$$\vec{d}_1 = \vec{p}_1 - \vec{p}_0$$

$$\vec{d}_2 = \vec{p}_2 - \vec{p}_0$$

This is equivalent to transforming from coordinate system O to coordinate system O’.

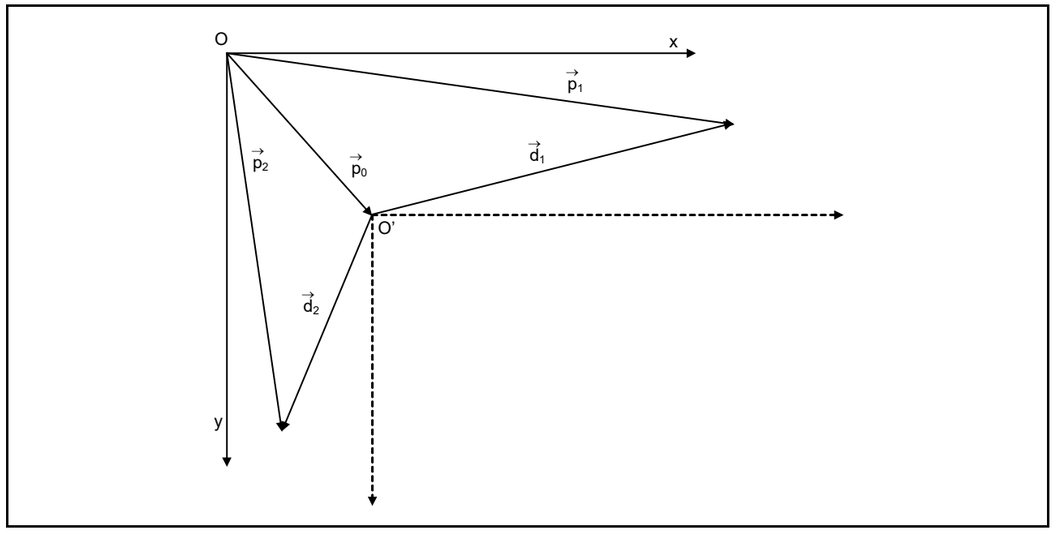


Figure 56.20 Texture mapping, object space, and transformation from coordinate system O to O’ to simplify calculations

考虑以下映射：

$$\vec{p}_0 = \begin{pmatrix} x_0 \\ y_0 \end{pmatrix} \Rightarrow (\tilde{\vec{p}}_0) = \begin{pmatrix} u_0 \\ v_0 \end{pmatrix} = \begin{pmatrix} 0 \\ 0 \end{pmatrix}$$

$$\vec{p}_1 = \begin{pmatrix} x_1 \\ y_1 \end{pmatrix} \Rightarrow (\tilde{\vec{p}}_1) = \begin{pmatrix} u_1 \\ v_1 \end{pmatrix} = \begin{pmatrix} w \\ 0 \end{pmatrix}$$

$$\vec{p}_2 = \begin{pmatrix} x_2 \\ y_2 \end{pmatrix} \Rightarrow (\tilde{\vec{p}}_2) = \begin{pmatrix} u_2 \\ v_2 \end{pmatrix} = \begin{pmatrix} 0 \\ h \end{pmatrix}$$

其中w是纹理的宽度，h是纹理的高度。

检查对象空间中的图56.20。为了简化计算，将差分向量作为计算：

$$\vec{d}_1 = \vec{p}_1 - \vec{p}_0$$

$$\vec{d}_2 = \vec{p}_2 - \vec{p}_0$$

这相当于从坐标系O变换到坐标系O'。

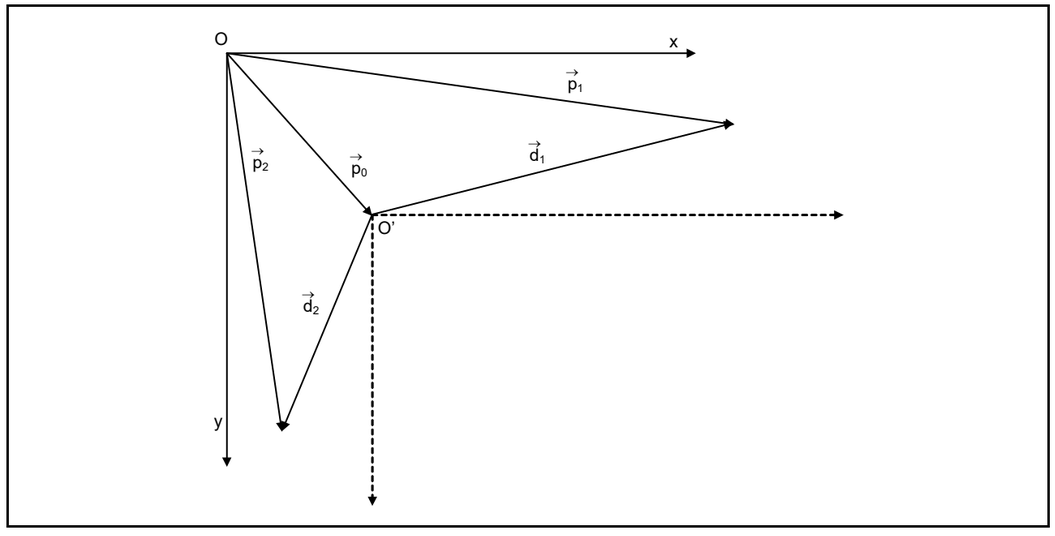


Figure 56.20 纹理映射、对象空间和从坐标系O到O'的转换以简化计算

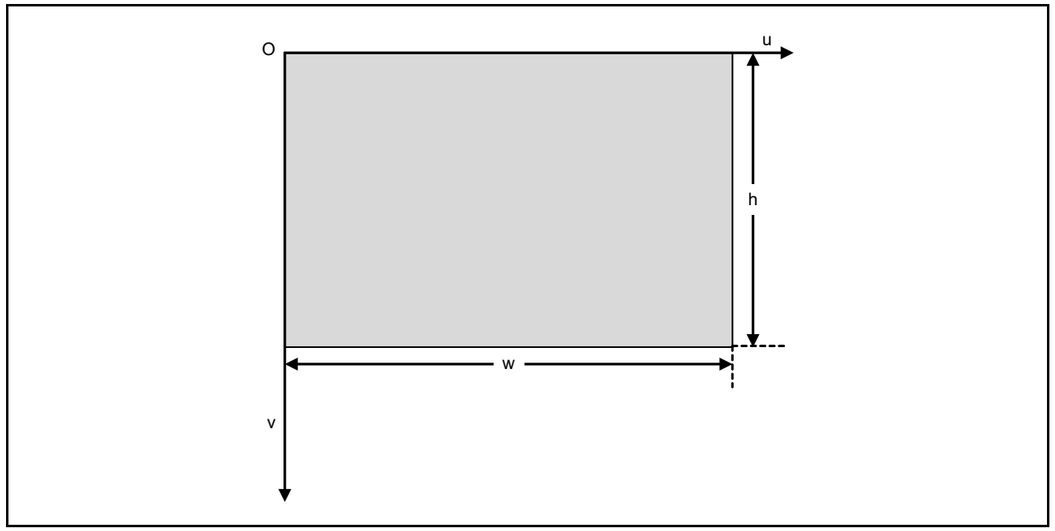


Figure 56.21 Texture mapping, texture space, and texture with width w and height h

In O', the mapping is:

$$\vec{p'}_0 = \begin{pmatrix}0\\0\end{pmatrix} \Rightarrow (\tilde{\vec{p}}_0) = \begin{pmatrix}u_0\\v_0\end{pmatrix} = \begin{pmatrix}0\\0\end{pmatrix}$$

$$\vec{d}_1 = \begin{pmatrix}dx_1\\dy_1\end{pmatrix} \Rightarrow (\tilde{\vec{p}}_1) = \begin{pmatrix}u_1\\v_1\end{pmatrix} = \begin{pmatrix}w\\0\end{pmatrix}$$

$$\vec{d}_2 = \begin{pmatrix}dx_2\\dy_2\end{pmatrix} \Rightarrow (\tilde{\vec{p}}_2) = \begin{pmatrix}u_2\\v_2\end{pmatrix} = \begin{pmatrix}w\\h\end{pmatrix}$$

This is a linear mapping that can be described by a 2 x 2 matrix.

$$(\tilde{\vec{p}}) = M \cdot \vec{p'} = \begin{bmatrix}m_{11} & m_{12}\\m_{21} & m_{22}\end{bmatrix} \cdot \vec{p'}$$

$$\Rightarrow \begin{pmatrix}w\\0\end{pmatrix} = M \cdot \vec{d}_1 \wedge \begin{pmatrix}0\\h\end{pmatrix} = M \cdot \vec{d}_2$$

If the equations are expanded and sorted, the result is two equation systems each with two unknowns. These can be described more easily with a new matrix.

Let $A = \begin{bmatrix}dx_1 & dy_1\\dx_2 & dy_2\end{bmatrix}$ then the equation system can be rewritten as:

$$\begin{pmatrix}w\\0\end{pmatrix} = A \cdot \begin{pmatrix}m_{11}\\m_{12}\end{pmatrix} \wedge \begin{pmatrix}0\\h\end{pmatrix} = A \cdot \begin{pmatrix}m_{21}\\m_{22}\end{pmatrix}$$

This can be easily solved with determinants.

Let $c = \frac{1}{detA} = \frac{1}{dx_1 \cdot dy_2 - dx_2 \cdot dy_1}$

The resulting constants are:

$$m_{11} = c \cdot w \cdot dy_2 = \frac{du}{dx}$$

$$m_{12} = -c \cdot w \cdot dx_2 = \frac{du}{dy}$$

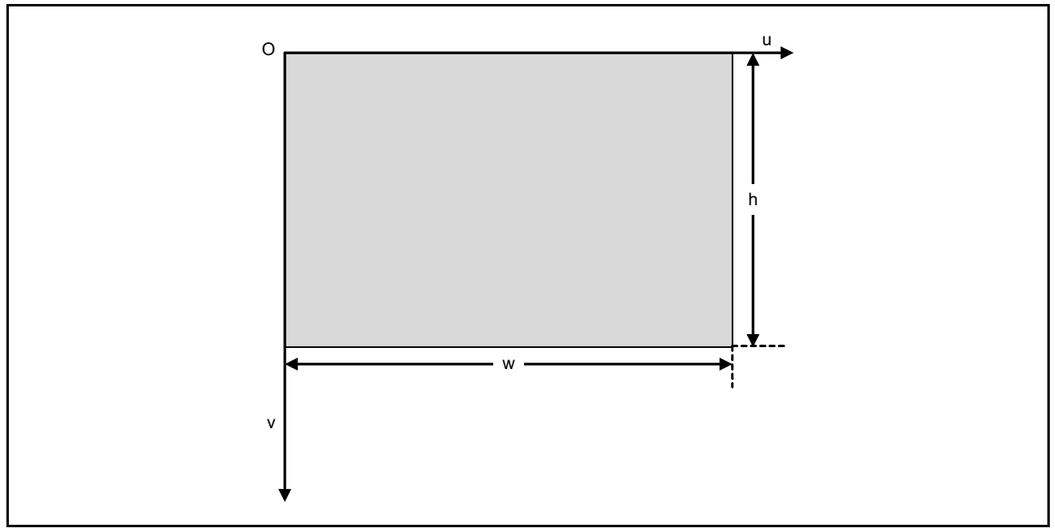


Figure 56.21 纹理映射、纹理空间和宽度为w和高度为h的纹理

在O'中，映射为：

$$\vec{p'}_0 = \begin{pmatrix}0\\0\end{pmatrix} \Rightarrow (\tilde{\vec{p}}_0) = \begin{pmatrix}u_0\\v_0\end{pmatrix} = \begin{pmatrix}0\\0\end{pmatrix}$$

$$\vec{d}_1 = \begin{pmatrix}dx_1\\dy_1\end{pmatrix} \Rightarrow (\tilde{\vec{p}}_1) = \begin{pmatrix}u_1\\v_1\end{pmatrix} = \begin{pmatrix}w\\0\end{pmatrix}$$

$$\vec{d}_2 = \begin{pmatrix}dx_2\\dy_2\end{pmatrix} \Rightarrow (\tilde{\vec{p}}_2) = \begin{pmatrix}u_2\\v_2\end{pmatrix} = \begin{pmatrix}w\\h\end{pmatrix}$$

这是一个可以用2x2矩阵描述的线性映射。

$$(\tilde{\vec{p}}) = M \cdot \vec{p'} = \begin{bmatrix}m_{11} & m_{12}\\m_{21} & m_{22}\end{bmatrix} \cdot \vec{p'}$$

$$\Rightarrow \begin{pmatrix}w\\0\end{pmatrix} = M \cdot \vec{d}_1 \wedge \begin{pmatrix}0\\h\end{pmatrix} = M \cdot \vec{d}_2$$

如果方程被扩展和排序，结果是两个方程组，每个方程组有两个未知数。这些可以用新的矩阵更容易地描述。

Let $A = \begin{bmatrix}dx_1 & dy_1\\dx_2 & dy_2\end{bmatrix}$ 那么方程组可以改写为：

$$\begin{pmatrix}w\\0\end{pmatrix} = A \cdot \begin{pmatrix}m_{11}\\m_{12}\end{pmatrix} \wedge \begin{pmatrix}0\\h\end{pmatrix} = A \cdot \begin{pmatrix}m_{21}\\m_{22}\end{pmatrix}$$

这可以通过行列式轻松解决。

Let $c = \frac{1}{detA} = \frac{1}{dx \cdot dy_2 - dx_2 \cdot dy_1}$

结果常数为：

$$m_{11} = c \cdot w \cdot dy_2 = \frac{du}{dx}$$

$$m_{12} = -c \cdot w \cdot dx_2 = \frac{杜迪}{\text{-----}}$$

$$m_{21} = c \cdot h \cdot dx_1 = \frac{dv}{dx}$$

$$m_{22} = -c \cdot h \cdot dx_2 = \frac{dv}{dy}$$

To calculate the start values for u and v at the top of the bounding box, the transformation from O' to O must be reversed. Let us and vs be the start values, then:

$$\begin{pmatrix} u_s \\ v_s \end{pmatrix} = M \cdot (-\vec{p}_0) = c \cdot \begin{pmatrix} -w \cdot (x_0 \cdot dy_2 - y_0 \cdot dx_2) \\ h \cdot (x_0 \cdot dy_1 - y_0 \cdot dx_1) \end{pmatrix}$$

Examples

U and v are in the texture space. Enter the following into any case:

- Copy case:
  dx1 = 1, dx2 = 0, dy1 = 0, dy1 = 1
- Scaling case x scaling copy case:
  dx1 = f, dx2 = 0, dy1 = 0, dy1 = 1
  with f being the scaling factor in the x direction similar for the y direction
- Rotation case:
  dx1 = cosa, dx2 = -sina, dy1 = sina, dy1 = cosa
  with the angle between d1 and the x axis in the clockwise direction.

56.6.3.2 Limiter operation

The texture limiters operate exactly the same as the spatial limiters shown in Figure 56.8, Operation flow of the linear limiter.

The register layout for the u limiter is the same:

- LUSTART = us
- LUXADD = du/dx
- LUYADD = du/dy.

The register layout for the v limiter is slightly different. TEXPITCH is multiplied to save one hardware multiplier.

- LVSTARTI = floor (vs) • TEXPITCH
  Contains the integer part of the start value.
- LVSTARTF = (vs-floor (vs)) • TEXPITCH
  Contains the fractional part of the start value.
- LVXADDI = floor (dv/dx) • TEXPITCH
  Contains the integer part of dv/dz.
- LVYADD = floor (dv/dy) • TEXPITCH
  Contains the integer part of dv/dy.
- LVYXADDF = (dv/dy - floor (dv/dy)) • TEXPITCH ((dv/dx - floor (dv/dx)) • TEXPITCH)
  Contains the fractional part of dv/dy and dv/dx combined in one register.
- TEXMASK
  Contains a mask for u and v separately to wraparound values of u and v. This is useful for staying inside the limits of the texture or repeat a texture. Wrap around textures have to have a size multiple of 2.
- TEXPITCH
  Contains the width of the texture in pixels in framebuffer memory. This information is required to calculate the new address if stepping to a new line.
- TEXORIGIN.
  Contains the base address of the texture.

$$m_{21} = c \cdot h \cdot dx_1 = \frac{dv}{dx}$$

$$m_{22} = -c \cdot h \cdot dx_2 = \frac{dv}{dy}$$

要计算边界框顶部的u和v的起始值，必须反转从O'到O的转换。
让我们和vs成为起始值，然后：

$$\begin{pmatrix} u_s \\ v_s \end{pmatrix} = M \cdot (-\vec{p}_0) = c \cdot \begin{pmatrix} -w \cdot (x_0 \cdot dy_2 - y_0 \cdot dx_2) \\ h \cdot (x_0 \cdot dy_1 - y_0 \cdot dx_1) \end{pmatrix}$$

Examples

U和v在纹理空间中。在任何情况下输入以下内容：

- Copy case:
  dx1 = 1, dx2 = 0, dy1 = 0, dy1 = 1
- 缩放案例x缩放复制案例：dx1=f dx2=0 dy1=0 dy1=1其中f是x方向的比例因子，类似于y方向
- 旋转情况：dx1=cosa，dx2=−sina，dy1=sina，dy1=cosa，d1与x轴之间的角度为顺时针方向。

56.6.3.2 限制器操作

纹理限制器的操作与图56.8，线性限制器的操作流程中所示的空间限制器完全相同。

u限制器的寄存器布局是相同的：

- LUSTART = us
- LUXADD = du/dx
- LUYADD = du/dy.

v限制器的寄存器布局略有不同。TEXPITCH相乘以节省一个硬件乘数。

- LVSTARTI = floor (vs) • TEXPITCH
  包含起始值的整数部分。
- LVSTARTF = (vs-floor (vs)) • TEXPITCH
  包含起始值的小数部分。
- LVXADDI = floor (dv/dx) • TEXPITCH
  包含dvdz的整数部分。
- LVYADD = floor (dv/dy) • TEXPITCH
  包含dvdy的整数部分。
- LVYXADDF = (dv/dy - floor (dv/dy)) • TEXPITCH ((dv/dx - floor (dv/dx)) • TEXPITCH)
  包含组合在一个寄存器中的dvdy和dvdx的小数部分。
- TEXMASK
  分别包含u和v的掩码以环绕u和v的值。这对于保持在纹理的限制内或重复纹理很有用。环绕纹理的大小必须是2的倍数。
- TEXPITCH
  包含帧缓冲区内存中纹理的宽度（以像素为单位）。如果步进到新行，则需要此信息来计算新地址。
- TEXORIGIN.
  包含纹理的基地址。

56.6.4 Colorization

After a pixel is found to be part of the geometry, its color is calculated. The 2D Drawing Engine supports a very general color calculation scheme, allowing support for several color modes. This color scheme uses an interpolation between two color registers, COLOR1 and COLOR2. See Figure 56.22 for details. COLOR1 and COLOR2 are marked as A, B in the figure for clarity.

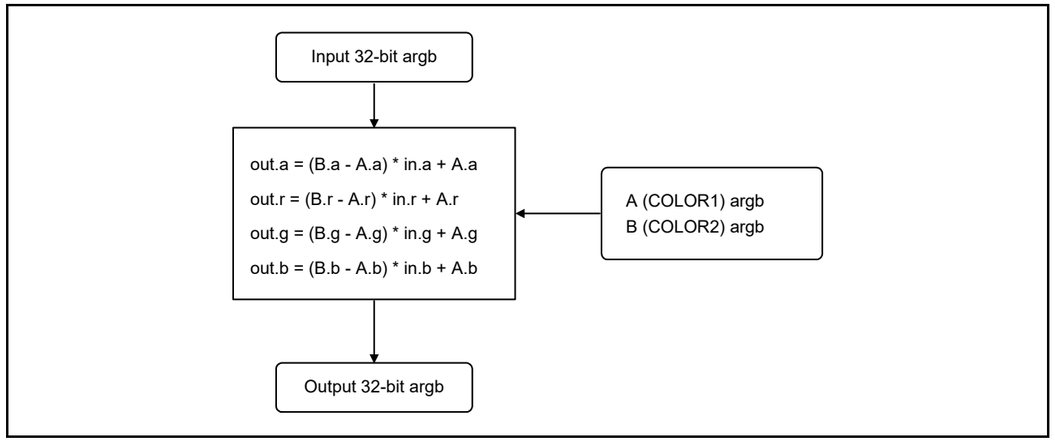


Figure 56.22 Colorization step and interpolation between the two color registers, A (COLOR1) and B (COLOR2)

This general approach can be used to support several different color modes that can be individually applied to any color or alpha channel of the input.

Table 56.7 Colorization operations

Operation	Settings for A and B *1
Copy	A = 0, B = 0xff
Replace with a constant value v	A = v, B = v
Multiply by a constant value v	A = 0, B = v
Colorize an alpha texture with the RGB value v	A.a = 0, A.r = B.r, A.g = B.g, A.b = B.b, B.a = 0xff,B.r = v.r, B.g = v.g, B.b = v.b
Invert a channel	A = 0xff, B = 0
Invert multiply with v	A = v, B = 0
Interpolate between color v and color u	A = v, B = u

Note 1. A = COLOR1, B = COLOR2

56.6.5 Blending

56.6.5.1 Color channel blending

The last step before the pixel is written to the framebuffer is to blend the pixel with the data that is already written to the framebuffer. If blending is activated, the framebuffer, referred to as DST, must be read. SRC is the output from the colorization unit.

The following color blend modes are supported:

- SRC_ZERO
- SRC_ONE
- SRC_ALPHA

56.6.4 Colorization

在发现一个像素是几何图形的一部分后，将计算其颜色。2D绘图引擎支持非常通用的颜色计算方案，允许支持多种颜色模式。此配色方案使用两个颜色寄存器COLOR1和COLOR2之间的插值。详见图56.22。为清楚起见，图中将COLOR1和COLOR2标记为A、B。

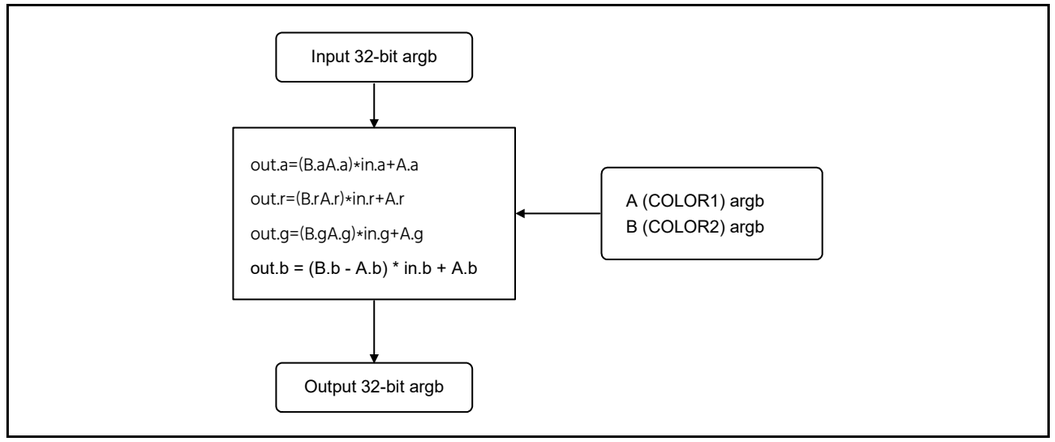


Figure 56.22 两个颜色寄存器A(COLOR1)和B(COLOR2)之间的着色步骤和插值

这种通用方法可用于支持几种不同的颜色模式，这些模式可以单独应用于输入的任何颜色或Alpha通道。

Table 56.7 着色操作

Operation	A和B的设置*1
Copy	A = 0, B = 0xff
替换为常数值v	A = v, B = v
乘以一个常数值v	A = 0, B = v
使用RGB值v为alpha纹理着色	A.a=0 A.r=B.r A.g=B.g A.b=B.b B.a=0xff B.r=v.r B.g=v.g B.b=v.b
反转通道	A = 0xff, B = 0
用v反转乘法	A = v, B = 0
在颜色v和颜色u之间进行插值	A = v, B = u

Note 1. A = COLOR1, B = COLOR2

56.6.5 Blending

56.6.5.1 颜色通道混合

将像素写入帧缓冲区之前的最后一步是将像素与已写入帧缓冲区的数据混合。如果激活了混合，则必须读取称为DST的帧缓冲区。SRC是着色单元的输出。

支持以下颜色混合模式：

- SRC_ZERO
- SRC_ONE
- SRC_ALPHA

- SRC_ONE_MINUS_ALPHA
- DST_ZERO
- DST_ONE
- DST_ALPHA
- DST_ONE_MINUS_ALPHA.

The selection of the color channel blend modes is performed with the following flags:

- BSF: blend source factor is alpha
- BSI: blend source factor invert
- BDF: blend destination factor is alpha
- BDI: blend destination factor invert.

The formula for the blending is:

$dst = src \cdot f_S + dst \cdot f_D$

where:

BSF = 0, BSI = 0 $\Rightarrow f_S = 1$

BSF = 1, BSI = 0 $\Rightarrow f_S = \alpha$

BSF = 0, BSI = 1 $\Rightarrow f_S = 0$

BSF = 1, BSI = 1 $\Rightarrow f_S = 1 - \alpha$

BDF = 0, BDI = 0 $\Rightarrow f_D = 1$

BDF = 1, BDI = 0 $\Rightarrow f_D = \alpha$

BDF = 0, BDI = 1 $\Rightarrow f_D = 0$

BDF = 1, BDI = 1 $\Rightarrow f_D = 1 - \alpha$.

Table 56.8 lists all possible color channel blend modes.

Table 56.8 Color channel blend modes

Mode	BSF	BSI	BDF	BDI	Blend equation
SRC_ONE DST_ONE	0	0	0	0	SRC + DST
SRC_ONE	0	0	0	1	SRC
SRC_ONE DST_ALPHA	0	0	1	0	SRC + DST × ALPHA
SRC_ONE DST_ONE_MINUS_ALPHA	0	0	1	1	SRC + DST × (1 - ALPHA)
SRC_ZERO DST_ONE	0	1	0	0	DST
SRC_ZERO DST_ZERO	0	1	0	1	0
SRC_ZERO DST_ALPHA	0	1	1	0	DST × ALPHA
SRC_ZERO DST_ONE_MINUS_ALPHA	0	1	1	1	DST × (1 - ALPHA)
SRC_ALPHA DST_ONE	1	0	0	0	SRC × ALPHA + DST
SRC_ALPHA	1	0	0	1	SRC × ALPHA
SRC_ALPHA DST_ALPHA	1	0	1	0	SRC × ALPHA + DST × ALPHA
SRC_ALPHA DST_ONE_MINUS_ALPHA	1	0	1	1	SRC × ALPHA + DST × (1 - ALPHA)
SRC_ONE_MINUS_ALPHA DST_ONE	1	1	0	0	SRC × (1 - ALPHA) + DST
SRC_ONE_MINUS_ALPHA	1	1	0	1	SRC × (1 - ALPHA)
SRC_ONE_MINUS_ALPHA DST_ALPHA	1	1	1	0	SRC × (1 - ALPHA) + DST × ALPHA
SRC_ONE_MINUS_ALPHA DST_ONE_MINUS_ALPHA	1	1	1	1	SRC × (1 - ALPHA) + DST × (1 - ALPHA)

- SRC_ONE_MINUS_ALPHA
- DST_ZERO
- DST_ONE
- DST_ALPHA
- DST_ONE_MINUS_ALPHA.

使用以下标志执行颜色通道混合模式的选择：

- BSF：混合源因子为alpha
- BSI：混合源因子反转
- BDF：混合目标因子为alpha
- BDI：混合目标因子反转。

混合公式为：

$dst = src \cdot f_S + dst \cdot f_D$

where:

BSF = 0, BSI = 0 $\Rightarrow f_S = 1$

BSF = 1, BSI = 0 $\Rightarrow f_S = \alpha$

BSF = 0, BSI = 1 $\Rightarrow f_S = 0$

BSF = 1, BSI = 1 $\Rightarrow f_S = 1 - \alpha$

BDF = 0, BDI = 0 $\Rightarrow f_D = 1$

BDF = 1, BDI = 0 $\Rightarrow f_D = \alpha$

BDF = 0, BDI = 1 $\Rightarrow f_D = 0$

BDF = 1, BDI = 1 $\Rightarrow f_D = 1 - \alpha$.

表56.8列出了所有可能的颜色通道混合模式。

Table 56.8 颜色通道混合模式

Mode	BSF	BSI	BDF	BDI	混合方程
SRC_ONE DST_ONE	0	0	0	0	SRC + DST
SRC_ONE	0	0	0	1	SRC
SRC_ONE DST_ALPHA	0	0	1	0	SRC + DST × ALPHA
SRC_ONE DST_ONE_MINUS_ALPHA	0	0	1	1	SRC + DST × (1 - ALPHA)
SRC_ZERO DST_ONE	0	1	0	0	DST
SRC_ZERO DST_ZERO	0	1	0	1	0
SRC_ZERO DST_ALPHA	0	1	1	0	DST × ALPHA
SRC_ZERO DST_ONE_MINUS_ALPHA	0	1	1	1	DST × (1 - ALPHA)
SRC_ALPHA DST_ONE	1	0	0	0	SRC × ALPHA + DST
SRC_ALPHA	1	0	0	1	SRC × ALPHA
SRC_ALPHA DST_ALPHA	1	0	1	0	SRC × ALPHA + DST × ALPHA
SRC_ALPHA DST_ONE_MINUS_ALPHA	1	0	1	1	SRC × ALPHA + DST × (1 - ALPHA)
SRC_ONE_MINUS_ALPHA DST_ONE	1	1	0	0	SRC × (1 - ALPHA) + DST
SRC_ONE_MINUS_ALPHA	1	1	0	1	SRC × (1 - ALPHA)
SRC_ONE_MINUS_ALPHA DST_ALPHA	1	1	1	0	SRC × (1 - ALPHA) + DST × ALPHA
SRC_ONE_MINUS_ALPHA DST_ONE_MINUS_ALPHA	1	1	1	1	SRC × (1 - ALPHA) + DST × (1 - ALPHA)

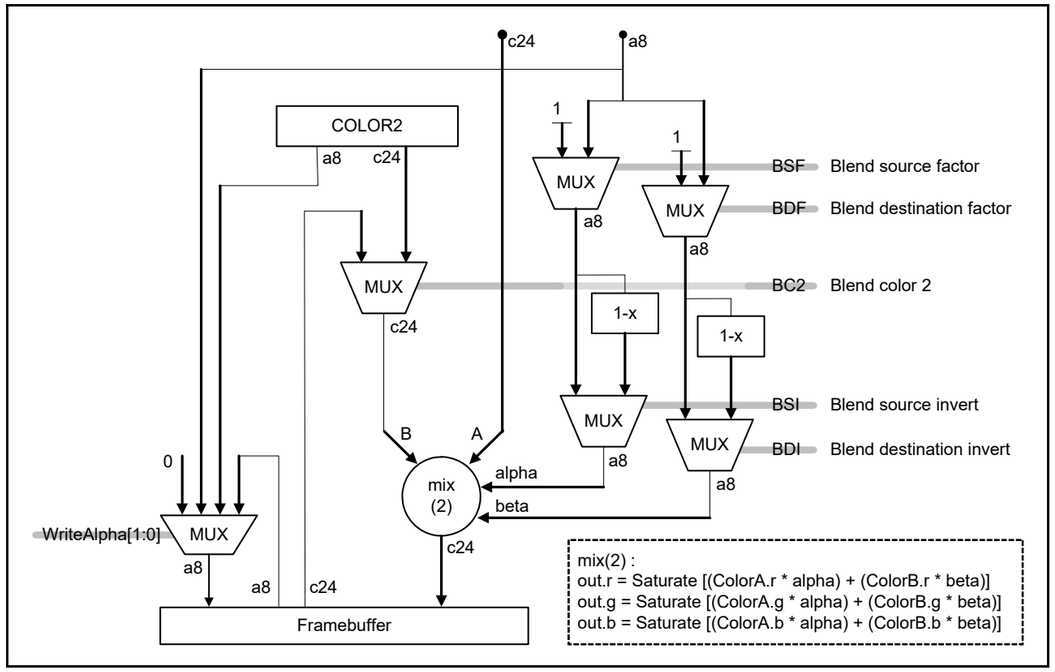


Figure 56.23 Color channel blend unit when CONTROL2.USEACB = 0

56.6.5.2 Alpha channel blending

The alpha channel can be blended in addition to the color channels. Alpha channel blending is enabled by setting CONTROL2.USEACB = 1. Alpha channel blending uses the same formulas and same blend modes as for the color channels. The alpha channel formulas can be set independently from the color channels.

The following alpha channel blend modes are supported:

- SRC_A_ZERO
- SRC_A_ONE
- SRC_A_SRC_A
- SRC_A_ONE_MINUS_SRC_A
- DST_A_ZERO
- DST_A_ONE
- DST_A_SRC_A
- DST_A_ONE_MINUS_SRC_A.

The alpha channel blend modes selected with the following flags:

- BSFA: blend source factor is SRC_A
- BSIA: blend source factor invert
- BDFA: blend destination factor is SRC_A
- BDIA: blend destination factor invert.

The formula for the blending is:

$dst\_alpha = src\_a \cdot f_{S\_a} + dst\_a \cdot f_{D\_a}$

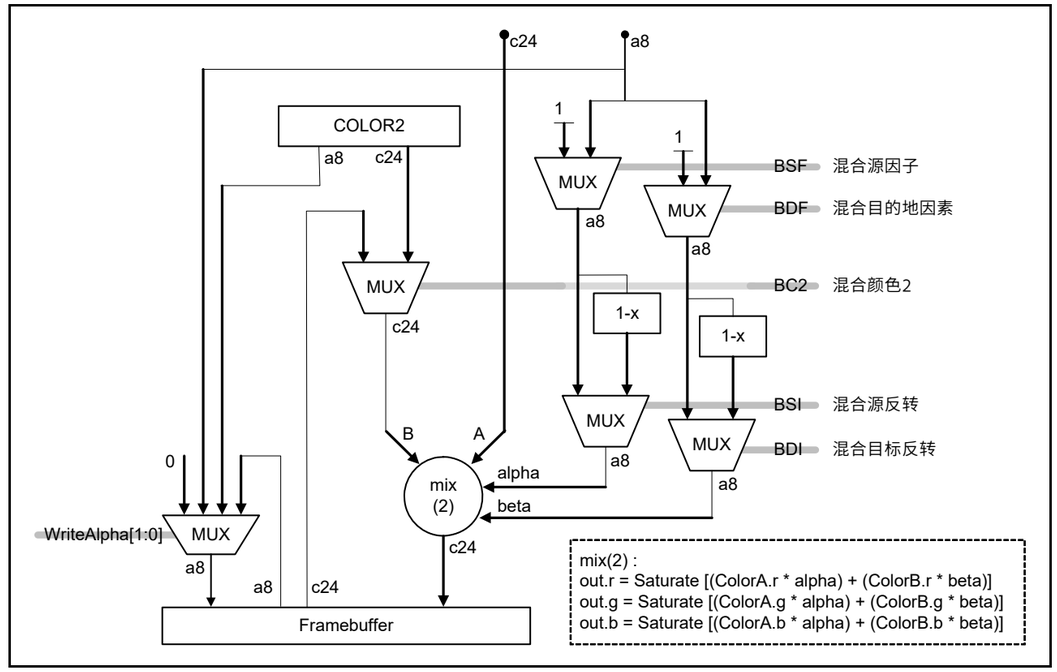


Figure 56.23 CONTROL2.USEACB=0时的颜色通道混合单元

56.6.5.2 Alpha通道混合

除了颜色通道之外，还可以混合Alpha通道。通过设置启用Alpha通道混合CONTROL2.USEACB=1。Alpha通道混合使用与颜色通道相同的公式和混合模式。Alpha通道公式可以独立于颜色通道进行设置。

支持以下Alpha通道混合模式：

- SRC_A_ZERO
- SRC_A_ONE
- SRC_A_SRC_A
- SRC_A_ONE_MINUS_SRC_A
- DST_A_ZERO
- DST_A_ONE
- DST_A_SRC_A
- DST_A_ONE_MINUS_SRC_A.

使用以下标志选择的Alpha通道混合模式：

- BSFA：混合源因子为SRC_A
- BSIA：混合源因子反转
- BDFA：混合目标因子为SRC_A
- BDIA：混合目标因子反转。

混合公式为：

$dst\_alpha = src\_a \cdot f_{S\_a} + dst\_a \cdot f_{D\_a}$

where:

BSFA = 0, BSIA = 0 ⇒ f_{S_a} = 1

BSFA = 1, BSIA = 0 ⇒ f_{S_a} = src_a

BSFA = 0, BSIA = 1 ⇒ f_{S_a} = 0

BSFA = 1, BSIA = 1 ⇒ f_{S_a} = 1 - src_a

BDFA = 0, BDIA = 0 ⇒ f_{D_a} = 1

BDFA = 1, BDIA = 0 ⇒ f_{D_a} = src_a

BDFA = 0, BDIA = 1 ⇒ f_{D_a} = 0

BDFA = 1, BDIA = 1 ⇒ f_{D_a} = 1 - src_a.

Table 56.9 lists all possible alpha channel blend modes.

Table 56.9 Alpha channel blend modes

Mode	BSF	BSI	BDF	BDI	Blend equation
SRC_A_ONE DST_A_ONE	0	0	0	0	SRC_A + DST_A
SRC_A_ONE	0	0	0	1	SRC_A
SRC_A_ONE DST_A_SRC_A	0	0	1	0	SRC_A + DST_A × SRC_A
SRC_A_ONE DST_A_ONE_MINUS_SRC_A	0	0	1	1	SRC_A + DST_A × (1 - SRC_A)
SRC_A_ZERO DST_A_ONE	0	1	0	0	DST_A
SRC_A_ZERO DST_A_ZERO	0	1	0	1	0
SRC_A_ZERO DST_A_SRC_A	0	1	1	0	DST_A × SRC_A
SRC_A_ZERO DST_A_ONE_MINUS_SRC_A	0	1	1	1	DST_A × (1 - SRC_A)
SRC_A_SRC_A DST_A_ONE	1	0	0	0	SRC_A × SRC_A + DST_A
SRC_A_SRC_A	1	0	0	1	SRC_A × SRC_A
SRC_A_SRC_A DST_A_SRC_A	1	0	1	0	SRC_A × SRC_A + DST_A × SRC_A
SRC_A_SRC_A DST_A_ONE_MINUS_SRC_A	1	0	1	1	SRC_A × SRC_A + DST_A × (1 - SRC_A)
SRC_A_ONE_MINUS_SRC_A DST_A_ONE	1	1	0	0	SRC_A × (1 - SRC_A) + DST_A
SRC_A_ONE_MINUS_SRC_A	1	1	0	1	SRC_A × (1 - SRC_A)
SRC_A_ONE_MINUS_SRC_A DST_A_SRC_A	1	1	1	0	SRC_A × (1 - SRC_A) + DST_A × SRC_A
SRC_A_ONE_MINUS_SRC_A DST_A_ONE_MINUS_SRC_A	1	1	1	1	SRC_A × (1 - SRC_A) + DST_A × (1 - SRC_A)

where:

BSFA = 0, BSIA = 0 ⇒ f_{S_a} = 1

BSFA = 1, BSIA = 0 ⇒ f_{S_a} = src_a

BSFA = 0, BSIA = 1 ⇒ f_{S_a} = 0

BSFA = 1, BSIA = 1 ⇒ f_{S_a} = 1 - src_a

BDFA = 0, BDIA = 0 ⇒ f_{D_a} = 1

BDFA = 1, BDIA = 0 ⇒ f_{D_a} = src_a

BDFA = 0, BDIA = 1 ⇒ f_{D_a} = 0

BDFA = 1, BDIA = 1 ⇒ f_{D_a} = 1 - src_a.

表56.9列出了所有可能的Alpha通道混合模式。

Table 56.9 Alpha通道混合模式

Mode	BSF	BSI	BDF	BDI	混合方程
SRC_A_ONE DST_A_ONE	0	0	0	0	SRC_A + DST_A
SRC_A_ONE	0	0	0	1	SRC_A
SRC_A_ONE DST_A_SRC_A	0	0	1	0	SRC_A + DST_A × SRC_A
SRC_A_ONE DST_A_ONE_MINUS_SRC_A	0	0	1	1	SRC_A + DST_A × (1 - SRC_A)
SRC_A_ZERO DST_A_ONE	0	1	0	0	DST_A
SRC_A_ZERO DST_A_ZERO	0	1	0	1	0
SRC_A_ZERO DST_A_SRC_A	0	1	1	0	DST_A × SRC_A
SRC_A_ZERO DST_A_ONE_MINUS_SRC_A	0	1	1	1	DST_A × (1 - SRC_A)
SRC_A_SRC_A DST_A_ONE	1	0	0	0	SRC_A × SRC_A + DST_A
SRC_A_SRC_A	1	0	0	1	SRC_A × SRC_A
SRC_A_SRC_A DST_A_SRC_A	1	0	1	0	SRC_A × SRC_A + DST_A × SRC_A
SRC_A_SRC_A DST_A_ONE_MINUS_SRC_A	1	0	1	1	SRC_A × SRC_A + DST_A × (1 - SRC_A)
SRC_A_ONE_MINUS_SRC_A DST_A_ONE	1	1	0	0	SRC_A × (1 - SRC_A) + DST_A
SRC_A_ONE_MINUS_SRC_A	1	1	0	1	SRC_A × (1 - SRC_A)
SRC_A_ONE_MINUS_SRC_A DST_A_SRC_A	1	1	1	0	SRC_A × (1 - SRC_A) + DST_A × SRC_A
SRC_A_ONE_MINUS_SRC_A DST_A_ONE_MINUS_SRC_A	1	1	1	1	SRC_A × (1 - SRC_A) + DST_A × (1 - SRC_A)

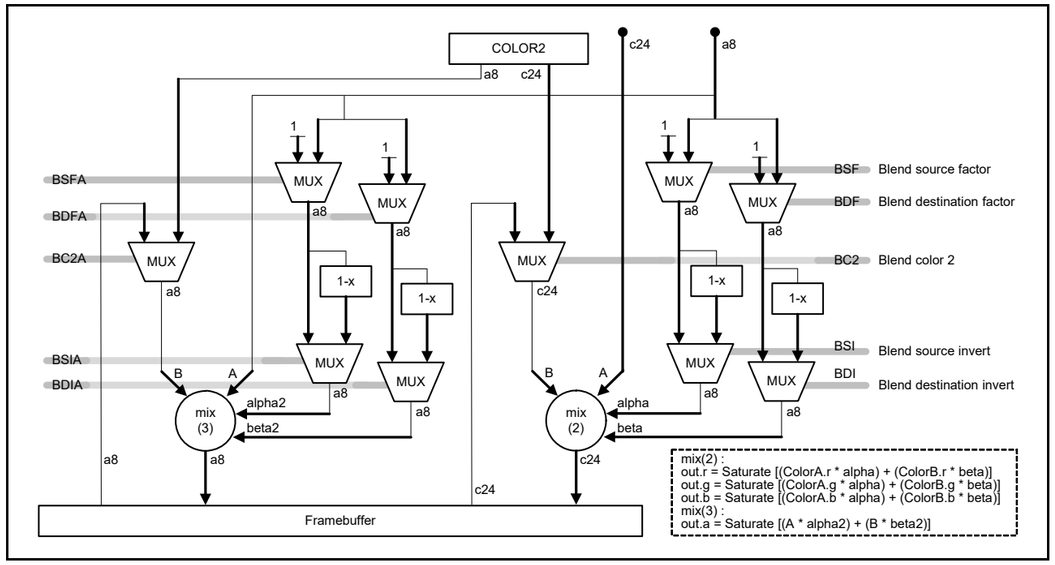


Figure 56.24 Alpha- and color-channel blend unit when CONTROL2.USEACB = 1

56.7 Rendering Modes

The rendering process can be performed in two different modes, register mode and display list mode.

56.7.1 Register Mode

In register mode, when operation is based on register settings, the host CPU configures and initiates each render process separately. To start a new render process, the host CPU must wait until the previous one is completed. In this mode, the host CPU is heavily engaged throughout the entire drawing procedure and is consequently to a large extent unavailable for other tasks.

The host CPU must set up all registers for performing a certain drawing operation before it can start the rendering process. A new register setup can only be started when the previous render process has completed. Before starting a new register setup, make sure that:

- STATUS.DLISTACTIVE = 0: Display list reader is idle
- STATUS.BUSENUM = 0: Pixel selection unit is idle.

Lastly, write the framebuffer start address to the ORIGIN register. This write triggers the 2D Drawing Engine to start rendering.

56.7.2 Display List Mode

In display list mode, the host CPU creates a display list in memory prior to starting the 2D Drawing Engine. Such a display contains a bundle of render operations. When started, the 2D Drawing Engine executes the display list autonomously in parallel with the host CPU, which is not involved with drawing operations most of the time. Use of a display list allows a fully asynchronous operation of the host CPU and the 2D Drawing Engine and offers the best possible system performance.

In this mode, the display list reader reads a memory block containing instructions on how to set the 2D Drawing Engine control registers and executes these control register writes accordingly.

Display list start

To start execution of a display list, which already resides in memory, the start address of the display list is written to the display list start address register DLISTSTART. Because rewriting DLISTSTART also stops any ongoing display list

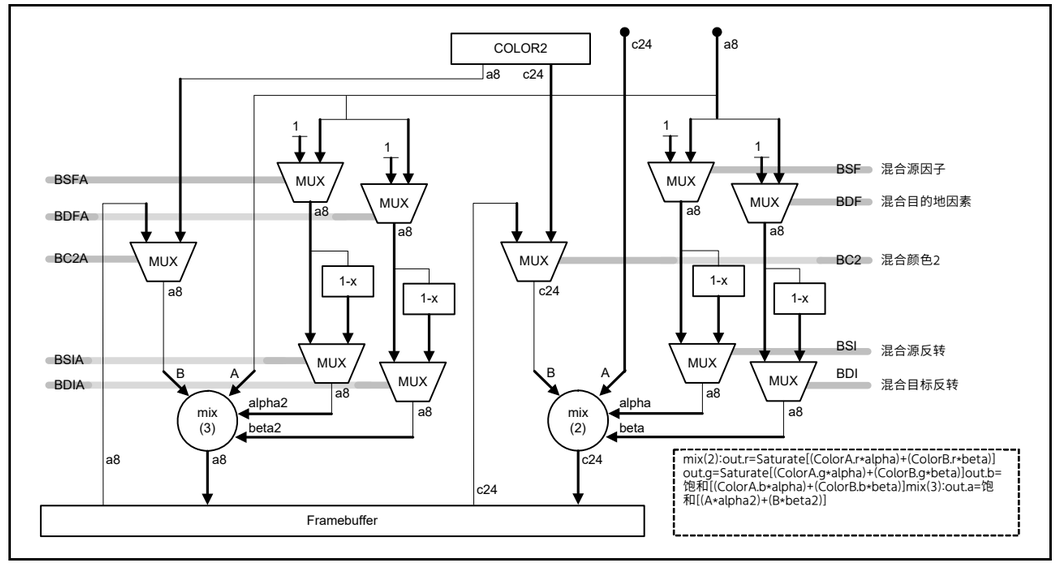


Figure 56.24 CONTROL2.USEACB=1时的Alpha和颜色通道混合单元

56.7 渲染模式

渲染过程可以在两种不同的模式下执行，注册模式和显示列表模式。

56.7.1 注册模式

在寄存器模式下，当操作基于寄存器设置时，主机CPU分别配置和启动每个渲染过程。要开始一个新的渲染进程，主机CPU必须等到前一个渲染完成。在这种模式下，主机CPU在整个绘图过程中都处于繁忙状态，因此在很大程度上无法用于其他任务。

主机CPU必须设置所有寄存器以执行特定的绘图操作，然后才能开始渲染过程。只有在前一个渲染过程完成后才能开始新的寄存器设置。在开始新的寄存器设置之前，请确保：

- STATUS.DLISTACTIVE=0：显示列表阅读器空闲
- STATUS.BUSENUM=0：像素选择单元空闲。

最后，将帧缓冲区起始地址写入ORIGIN寄存器。此写入触发2D绘图引擎开始渲染。

56.7.2 显示列表模式

在显示列表模式下，主机CPU在启动2D绘图引擎之前在内存中创建一个显示列表。这样的显示包含一组渲染操作。启动时，2D绘图引擎与主机CPU并行自主地执行显示列表，大部分时间不参与绘图操作。使用显示列表允许主机CPU和2D绘图引擎的完全异步操作，并提供最佳的系统性能。

在此模式下，显示列表读取器读取包含有关如何设置2D绘图引擎控制寄存器的指令的内存块，并相应地执行这些控制寄存器写入。

显示列表开始

为了开始执行已经驻留在存储器中的显示列表，将显示列表的起始地址写入显示列表起始地址寄存器DLISTSTART。因为重写DLISTSTART也会停止任何正在进行的显示列表

execution, make sure that the previous display list process is completed by either of the following two methods:

- Check that STATUS.DLISTACTIVE = 0, which indicates idle status of the display list reader
- Wait for the display list interrupt DRWDLISTIRQ, which indicates completion of the previous display list process.

Caution: Direct writing to 2D Drawing Engine registers while the display list mode is active (STATUS.DLISTACTIVE = 1) might lead to a 2D Drawing Engine hang-up. To prevent this, always check that the display list reader is idle ((STATUS.DLISTACTIVE = 0) before writing to any 2D Drawing Engine register.

Display list format

Display lists are stored using direct register-to-value mappings, which means that the display list contains a one byte index that addresses a certain register and the value to be written to the register. The register index is derived from the address offset of the register address and can be calculated by dividing the address offset by 4. For the index of each register, see section 56.2, Register Descriptions.

As the 2D Drawing Engine registers are always 32 bits wide, each data unit (called a data word) to be written to a register is of the same size. An address word that contains the indices of the register to be written is stored in a packed notation with up to four indices stored in one 32-bit address word.

A display list command always starts with an address word, followed by up to four data words, one for each register. The indices are read and interpreted from LSB to MSB, so the register of the low byte index is written first.

Example

In the following example:

- DWORD 201A 1930h // start of list address word
- DWORD 0000 0013h // data word 1 (for register 30h)
- DWORD FFFF FFAAh // data word 2 (for register 19h)
- DWORD 4033 6480h // data word 3 (for register 1Ah)
- DWORD 0001 0000h // data word 4 (for register 20h)
- DWORD... // next address word.

This stream of dwords updates the DRW registers as follows:

- Write 0000_0013h to register 30h = 48, which is IRQCTL
- Write FFFF_FFAAh to register 19h = 25, which is COLOR1
- Write 4033_6480h to register 1Ah = 26, which is COLOR2
- Write 0001_0000h to register 20h = 32, which is ORIGIN.

Address word indices

Besides referencing a register, the indices of an address word can also have other meanings, depending on their value.

Table 56.10 Address indices function (1 of 2)

Index	Function	
00h to 7Fh	Register indices Two register indices trigger additional actions:	
	- 20h = 32:	A write to ORIGIN to set a new frame buffer address is delayed until the ongoing frame buffer write-back is complete, when STATUS.BUSYWRITE = 0.
	- 32h = 50:	A write to DLISTSTART sets a new display list start address stops the current display list and starts the new one.
80h	Gap index, which is used to fill unused bytes of an address word. For example, if fewer than four indices are required, the remaining bytes are filled with 80h. In this case, the number of the subsequent data words must be reduced accordingly.	

执行，请确保之前的显示列表过程通过以下两种方法之一完成：

- 检查STATUS.DLISTACTIVE=0，表示显示列表阅读器的空闲状态
- 等待显示列表中断DRWDLISTIRQ，表示上一个显示列表过程完成。

Caution: 在显示列表模式处于活动状态(STATUS.DLISTACTIVE=1)时直接写入2D绘图引擎寄存器可能会导致2D绘图引擎挂起。为了防止这种情况，在写入任何2D绘图引擎寄存器之前，请始终检查显示列表读取器是否处于空闲状态((STATUS.DLISTACTIVE=0)。

显示列表格式

显示列表使用直接寄存器到值的映射来存储，这意味着显示列表包含一个字节索引，该索引对某个寄存器和要写入该寄存器的值进行寻址。寄存器索引由寄存器地址的地址偏移量得出，可以通过将地址偏移量除以4来计算。对于每个寄存器的索引，请参见第56.2节，寄存器说明。

由于2D绘图引擎寄存器始终为32位宽，因此要写入寄存器的每个数据单元（称为数据字）具有相同的大小。包含要写入的寄存器索引的地址字以压缩符号存储，一个32位地址字中最多存储四个索引。

显示列表命令总是以地址字开头，后跟最多四个数据字，每个寄存器一个。索引从LSB读取并解释为MSB，因此首先写入低字节索引的寄存器。

Example

在以下示例中：

- DWORD201A1930h列表地址字的开始
- DWORD00000013h数据字1（用于寄存器30h）
- DWORDFFFFFFAAh数据字2（用于寄存器19h）
- DWORD40336480h数据字3（用于寄存器1Ah）
- DWORD00010000h数据字4（用于寄存器20h）
- DWORD…下一个地址字。

此双字流更新DRW寄存器如下：

- 将0000_0013h写入寄存器30h=48，即IRQCTL
- 将FFFF_FFAAh写入寄存器19h=25，即COLOR1
- 将4033_6480h写入寄存器1Ah=26，即COLOR2
- 将0001_0000h写入寄存器20h=32，即ORIGIN。

地址字索引

除了引用寄存器之外，地址字的索引还可以具有其他含义，具体取决于它们的值。

Table 56.10 地址索引函数(1of2)

Index	Function	
00h to 7Fh	注册索引 两个寄存器索引触发其他操作：	
	- 20h = 32:	当STATUS.BUSYWRITE=0时，延迟写入ORIGIN以设置新的帧缓冲区地址，直到正在进行的帧缓冲区回写完成。
	- 32h = 50:	对DLISTSTART的写入会设置一个新的显示列表起始地址，从而停止当前的显示列表并启动新的显示列表。
80h	间隙索引，用于填充地址字的未使用字节。例如，如果需要的索引少于四个，则剩余字节用80h填充。在这种情况下，必须相应减少后续数据字的数量。	

Table 56.10 Address indices function (2 of 2)

Index	Function	
FFh	If the first index of an address word contains the special index FFh, the subsequent (second) index is interpreted as follows:	
	- Bit [0] set:	Display list end.
	- Bit [1] set:	Issue a full pipeline flush and wait (necessary before flip).
	- Bit [2] set:	Wait for writeback complete (necessary before framebuffer format change).
	- Bits [3:7]	Set all to 0s.
	Bit [1] and [2] settings are mutually exclusive. All indices after the special index FFh are ignored, and the next address word is read, if no display list end (bit [0] = 1) was set.	
	The remaining two indices must be set to 00h.	

Caution: Gap indices 80h must not be placed between other indices, for example as “index1 - 80h - index3 - index4”. Always fill all indices after 80h with the gap index.

Caution: If any of the special indices 80h and FFh are used, no register index can follow after them in the same address word.

Table 56.11 2D Drawing Engine registers overview (1 of 2)

Register function	Symbol	Index
Control registers:		
Geometry control 0	CONTROL	0
Surface control	CONTROL2	1
Interrupt control	IRQCTL	48
Cache control	CACHECTL	49
Status control	STATUS	n.a.*1
Hardware version and feature set ID	HWREVISION	n.a.*1
Color registers:		
Base color	COLOR1	25
Secondary color	COLOR2	26
Pattern	PATTERN	29
Limiter registers:		
Limiter 1 start value	L1START	4
Limiter 2 start value	L2START	5
Limiter 3 start value	L3START	6
Limiter 4 start value	L4START	7
Limiter 5 start value	L5START	8
Limiter 6 start value	L6START	9
Limiter 1 x-axis increment	L1XADD	10
Limiter 2 x-axis increment	L2XADD	11
Limiter 3 x-axis increment	L3XADD	12
Limiter 4 x-axis increment	L4XADD	13
Limiter 5 x-axis increment	L5XADD	14
Limiter 6 x-axis increment	L6XADD	15
Limiter 1 y-axis increment	L1YADD	16
Limiter 2 y-axis increment	L2YADD	17
Limiter 3 y-axis increment	L3YADD	18
Limiter 4 y-axis increment	L4YADD	19
Limiter 5 y-axis increment	L5YADD	20
Limiter 6 y-axis increment	L6YADD	21
Limiter 1 band width parameter	L1BAND	22

Table 56.10 地址索引函数(2of2)

Index	Function	
FFh	如果地址字的第一个索引包含特殊索引FFh，则后续（第二个）索引解释如下：	
	- Bit [0] set:	显示列表结束。
	- Bit [1] set:	发出完整的管道刷新并等待（翻转前必需）。
	- Bit [2] set:	等待写回完成（在帧缓冲区格式更改之前是必需的）。
	- Bits [3:7]	全部设置为0。
	位[1]和[2]设置是互斥的。如果没有设置显示列表结束（位[0]=1），则忽略特殊索引FFh之后的所有索引，并读取下一个地址字。	
	其余两个索引必须设置为00h。	

Caution: 间隙索引80h不得放在其他索引之间，例如“index180hindex3index4”。在80小时后始终使用间隙索引填充所有索引。

Caution: 如果使用了特殊索引80h和FFh中的任何一个，则在同一地址字中不能跟在它们之后。

Table 56.11 2D绘图引擎寄存器概述(1of2)

注册功能	Symbol	Index
Control registers:		
几何控制0	CONTROL	0
表面控制	CONTROL2	1
中断控制	IRQCTL	48
缓存控制	CACHECTL	49
状态控制	STATUS	n.a.*1
硬件版本和功能集ID	HWREVISION	n.a.*1
Color registers:		
基本颜色	COLOR1	25
次要颜色	COLOR2	26
Pattern	PATTERN	29
Limiter registers:		
限制器1起始值	L1START	4
限制器2起始值	L2START	5
限制器3起始值	L3START	6
限制器4起始值	L4START	7
限制器5起始值	L5START	8
限制器6起始值	L6START	9
限制器1x轴增量	L1XADD	10
限制器2x轴增量	L2XADD	11
限制器3x轴增量	L3XADD	12
限制器4x轴增量	L4XADD	13
限制器5x轴增量	L5XADD	14
限制器6x轴增量	L6XADD	15
限制器1y轴增量	L1YADD	16
限制器2y轴增量	L2YADD	17
限制器3y轴增量	L3YADD	18
限制器4y轴增量	L4YADD	19
限制器5y轴增量	L5YADD	20
限制器6y轴增量	L6YADD	21
限制器1带宽参数	L1BAND	22

Table 56.11 2D Drawing Engine registers overview (2 of 2)

Register function	Symbol	Index
Limiter 2 band width parameter	L2BAND	23
Texture registers:		
Texture base address	TEXORIGIN	47
Texels per texture line	TEXPITCH	45
Texture size or texture address mask	TEXMASK	46
U limiter start value	LUSTART	36
U limiter x-axis increment	LUXADD	37
U limiter y-axis increment	LUYADD	38
V limiter start value integer part	LVSTARTI	39
V limiter start value fractional part	LVSTARTF	40
V limiter x-axis increment integer part	LVXADDI	41
V limiter y-axis increment integer part	LVYADDI	42
V limiter increment fractional parts	LVYXADDF	43
Color lookup table start address	TEXCLADDR	55
Write Data to DRWTEXCLADDR; after each data write, DRWTEXCLADDR is incremented by 1.	TEXCLDATA	56
Offset to the index for the indexed texture formats i8, i4, i2, and i1	TEXCLOFFSET	57
Compare value for R,G, B components of internal texel color representation.	COLKEY	58
Miscellaneous registers:		
Bounding box dimension	SIZE	30
Framebuffer pitch and spanstore delay	PITCH	31
Address of the first pixel in framebuffer	ORIGIN	32
Display list start address	DLISTSTART	50
Performance counters control	PERFTRIGGER	53
Performance counter 1	PERFCOUNT1	51
Performance counter 2	PERFCOUNT2	52

Note 1. These registers are read-only and cannot be accessed in display list mode, and they therefore have no index.

56.7.3 Stopping the Render Process

Stopping an ongoing render process requires a specific procedure, which is described in section 56.10, Stopping the 2D Drawing Engine Render Process.

56.8 Interrupts

The 2D Drawing Engine generates three interrupts:

- DRWBUSIRQ
- DRWENUMIRQ
- DRWDLISTIRQ.

56.8.1 Interrupt sources

DRWBUSIRQ

This is the 2D Drawing Engine bus error interrupt. It occurs when the 2D Drawing Engine attempts to access an undefined address range through the following:

- Framebuffer Base Address Register ORIGIN
- Texture Base Address Register TEXORIGIN

Table 56.11 2D绘图引擎寄存器概述(2of2)

注册功能	Symbol	Index
限制器2带宽参数	L2BAND	23
Texture registers:		
纹理基地址	TEXORIGIN	47
每条纹理线的纹素	TEXPITCH	45
纹理大小或纹理地址掩码	TEXMASK	46
U限制器起始值	LUSTART	36
U限制器x轴增量	LUXADD	37
U限制器y轴增量	LUYADD	38
V限制器起始值整数部分	LVSTARTI	39
V限制器起始值小数部分	LVSTARTF	40
V限制器x轴增量整数部分	LVXADDI	41
V限制器y轴增量整数部分	LVYADDI	42
V限制器增量小数部分	LVYXADDF	43
颜色查找表起始地址	TEXCLADDR	55
将数据写入DRWTEXCLADDR；每次数据写入后，DRWTEXCLADDR加1。	TEXCLDATA	56
索引纹理格式i8、i4、i2和i1的索引偏移量	TEXCLOFFSET	57
比较内部纹理颜色表示的R、G、B分量的值。	COLKEY	58
Miscellaneous registers:		
边界框尺寸	SIZE	30
帧缓冲间距和跨度存储延迟	PITCH	31
帧缓冲区中第一个像素的地址	ORIGIN	32
显示列表起始地址	DLISTSTART	50
性能计数器控制	PERFTRIGGER	53
性能计数器1	PERFCOUNT1	51
性能计数器2	PERFCOUNT2	52

Note 1. 这些寄存器是只读的，不能在显示列表模式下访问，因此它们没有索引。

56.7.3 停止渲染过程

停止正在进行的渲染过程需要一个特定的过程，这在第56.10节中描述，停止2D绘图引擎渲染过程。

56.8 Interrupts

2D绘图引擎产生三个中断：

- DRWBUSIRQ
- DRWENUMIRQ
- DRWDLISTIRQ.

56.8.1 中断源

DRWBUSIRQ

这是2D绘图引擎总线错误中断。当2D绘图引擎尝试通过以下方式访问未定义的地址范围时会发生这种情况：

- 帧缓冲基地址寄存器ORIGIN
- 纹理基地址寄存器TEXORIGIN

- Display List Start Address Register (DLISTSTART).

The bus error interrupt DRWBUSIRQ is then generated. The bus error interrupt only serves for debugging purposes. The interrupt source can be determined by the BUSERRMFB, BUSERRMTXMRL, and BUSERRMDL bits of the STATUS register.

Note: After a DRWBUSIRQ occurrence, you must apply a system reset.

DRWENUMIRQ

This is the current render process finished interrupt.

DRWDLISTIRQ

This is the display list interrupt. It is asserted on completion of a display list process. DRWDLISTIRQ is activated if one of the following is true:

- The entire display list is complete
- The display list processing stops because a new display list start is triggered by a write to the Display List Start Address Register (DLISTSTART).

56.8.2 Interrupt Control

The three 2D Drawing Engine interrupts are combined into a single shared interrupt, DRW_IRQ, to the CPU. Each interrupt can be masked (disabled), or unmasked (enabled) by setting its associated enable bit in the Interrupt Control Register (IRQCTL).

The occurrence of an enabled interrupt (one with its mask bit set to 1 in IRQCTL) is monitored in the Status Control Register (STATUS) with its associated interrupt status bit is set to 1. The shared 2D Drawing Engine interrupt DRW_IRQ is then generated.

To clear the interrupt, the host CPU must write 1 to the interrupt clear bit in IRQCTL. The interrupt clear bit returns to 0 automatically.

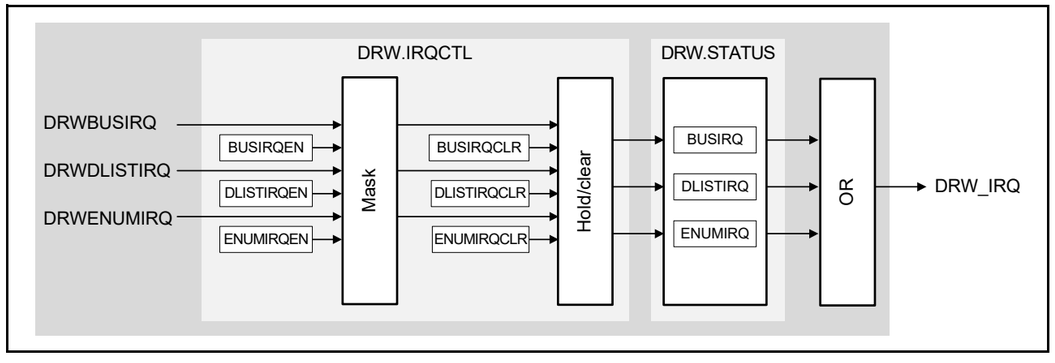


Figure 56.25 Interrupt Controller Unit (ICU)

56.9 Performance Counters

The 2D Drawing Engine features two independent 32-bit performance counter registers (PERFCOUNTk (k = 1, 2)) to count the number of occurrences of a certain event. The events to be counted can be set up independently for each performance counter register with the Performance Counter Control Registers, PERFTRIGGER.PERFTRIGGER2 for PERFCOUNT2 and PERFTRIGGER.PERFTRIGGER1 for PERFCOUNT1.

Table 56.12 lists the performance counter trigger events that can be selected.

- 显示列表起始地址寄存器(DLISTSTART)。

然后产生总线错误中断DRWBUSIRQ。总线错误中断仅用于调试目的。中断源可以由STATUS寄存器的BUSERRMFB、BUSERRMTXMRL和BUSERRMDL位确定。

Note: 发生DRWBUSIRQ后，您必须应用系统复位。

DRWENUMIRQ

这是当前渲染过程完成的中断。

DRWDLISTIRQ

这是显示列表中断。它在显示列表过程完成时被断言。如果以下条件之一为真，则激活DRWDLISTIRQ：

- 整个显示列表完整
- 显示列表处理停止，因为新的显示列表开始是由对显示列表开始的写入触发的地址寄存器(DLISTSTART)。

56.8.2 中断控制

三个2D绘图引擎中断组合成一个共享中断DRW_IRQ，发送给CPU。通过设置中断控制寄存器(IRQCTL)中的相关启用位，可以屏蔽（禁用）或取消屏蔽（启用）每个中断。

在状态控制中监视启用的中断（在IRQCTL中其屏蔽位设置为1）的发生寄存器(STATUS)及其相关的中断状态位设置为1。共享的2D绘图引擎中断然后生成DRW_IRQ。

要清除中断，主机CPU必须将1写入IRQCTL中的中断清除位。中断清除位自动返回0。

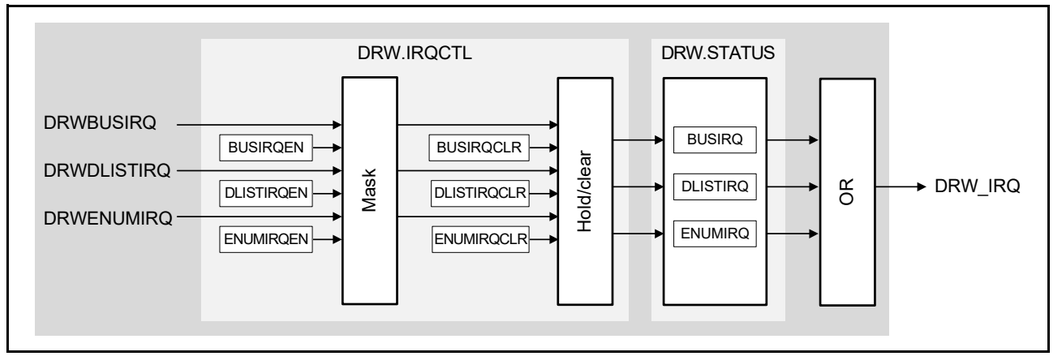


Figure 56.25 中断控制器单元(ICU)

56.9 性能计数器

2D绘图引擎具有两个独立的32位性能计数器寄存器(PERFCOUNTk(k=1 2))，用于计算某个事件的发生次数。可以使用性能计数器控制寄存器为每个性能计数器寄存器单独设置要计数的事件，PERFTRIGGER.PERFTRIGGER2用于PERFCOUNT2，PERFTRIGGER.PERFTRIGGER1用于PERFCOUNT1。

表56.12列出了可以选择的性能计数器触发事件 。

Table 56.12 Performance counter trigger events

PERFTRIGGER.PERFTRIGGERk	Event
0	Disable performance counter
1	2D Drawing Engine active cycles
2	Framebuffer read access
3	Framebuffer write access
4	Texture read access
5	Invisible pixels (enumerated but selected with alpha 0%)
6	Invisible pixels while internal FIFO is empty (lost cycles)
7	Display list reader active cycles
8	Framebuffer read hits
9	Framebuffer read misses
10	Framebuffer write hits
11	Framebuffer write misses
12	Texture read hits
13	Texture read misses
31	Every clock cycle (for use as timer)

56.10 Stopping the 2D Drawing Engine Render Process

If a render process has started either in register or display list mode, the 2D Drawing Engine processes the data autonomously until the render process is finished. Depending on the rendering, this process might take several milliseconds.

If the 2D Drawing Engine is to be disabled because, for example, the MCU enters a low power mode, proceed as follows to stop the ongoing rendering:

1. Set the following registers as follows:

   SIZE = 0001 0001h

   Set bounding box dimensions to 1 pixel x 1 line.

   CONTROL2 = 0000 0000h

   Color format a (8), no texture, CLUT.

   ORIGIN = UnmappedAddress

   The UnmappedAddress is an address that is not available for 2D Drawing Engine access.

   The recommended UnmappedAddress is given here under the key word “UnmappedAddress”.

   Alternatively do the same in display list mode:

   ```
   DWORD 8020 011Eh          // start of “address word” list
   DWORD 0001 0001h          // SIZE = 0001 0001h
   DWORD 0000 0000h          // CONTROL2 = 0000 0000h
   DWORD UnmappedAddress     // ORIGIN = UnmappedAddress
   ```

2. Wait for the Bus Error corresponding to the unmapped address violation, which indicates access to an unmapped address and the stop of the render process.
   UnmappedAddress = FFFF FFF0h

3. Disable the 2D Drawing Engine, if wanted.

Table 56.12 性能计数器触发事件

PERFTRIGGER.PERFTRIGGERk	Event
0	禁用性能计数器
1	2D绘图引擎活动周期
2	帧缓冲区读取访问
3	帧缓冲区写访问
4	纹理读取访问
5	不可见像素（枚举但使用alpha0%选择）
6	内部FIFO为空时不可见像素（丢失周期）
7	显示列表阅读器活动周期
8	帧缓冲读取命中
9	帧缓冲区读取未命中
10	帧缓冲区写入命中
11	帧缓冲区写入未命中
12	纹理读取命中
13	纹理读取未命中
31	每个时钟周期（用作定时器）

56.10 停止2D绘图引擎渲染进程

如果渲染进程已在注册或显示列表模式下启动，则2D绘图引擎会自主处理数据，直到渲染进程完成。
根据渲染，此过程可能需要几毫秒。

如果要禁用2D绘图引擎，例如，MCU进入低功耗模式，请按照以下步骤停止正在进行的渲染：

1. 如下设置以下寄存器：

   SIZE = 0001 0001h
   将边界框尺寸设置为1像素x1行。
   CONTROL2 = 0000 0000h
   颜色格式a(8)，无纹理，CLUT。
   ORIGIN = UnmappedAddress
   UnmappedAddress是不可用于2D绘图引擎访问的地址。
   推荐的UnmappedAddress在关键字“UnmappedAddress”下给出。
   或者在显示列表模式下执行相同操作：
   DWORD8020011Eh“地址字”列表的开始DWORD0001000
   1hSIZE=00010001h

   ```
   DWORD 0000 0000h          // CONTROL2 = 0000 0000h
   DWORD UnmappedAddress     // ORIGIN = UnmappedAddress
   ```

2. 等待未映射地址违规对应的总线错误，表示访问未映射地址并停止渲染进程。未映射地址=FFFFFFF0h

3. 如果需要，禁用2D绘图引擎。

57. JPEG Codec (JPEG)

57.1 Overview

The JPEG Codec conforms to the JPEG baseline compression and decompression standard to provide high-speed compression of image data and high-speed decoding of JPEG data. Table 57.1 lists the JPEG Codec specifications and Figure 57.1 shows a block diagram.

Table 57.1 JPEG Codec specifications

Parameter	Specifications
Compliant standard	Complies with JPEG Baseline standard within the range described in this document. The JPEG Codec does not support the following features: • Scanning with two elements • Non-interleave scanning with multiple elements
Operational precision	Conforms to JPEG Part 2, ISO-IEC10918-2
Image input/output system	Block interleave method
Pixel format	• Compression: YCbCr422 (H = 2:1:1, V = 1:1:1) • Decompression: YCbCr444 (H = 1:1:1, V = 1:1:1), YCbCr422 (H = 2:1:1, V = 1:1:1), YCbCr411 (H = 4:1:1, V = 1:1:1), YCbCr420 (H = 2:1:1, V = 2:1:1) • Output pixel format to the buffer: ARGB8888, RGB565
Quantization table	• Four tables provided
Huffman table	• Four tables provided (two tables for AC coefficients and two tables for DC coefficients)
Markers supported	SOI (start of image), SOF0 (start of frame type 0), SOS (start of scan), DQT (define quantization tables), DHT (define Huffman tables), DRI (define restart interval), RSTm (restart marks), and EOI (end of image)
Processing unit	8-byte address boundary units can be set
Image sizes that can be processed	Sizes divisible by the minimum coded unit (MCU): 8 lines by 8 pixels in YCbCr444, 8 lines by 16 pixels in YCbCr422, 8 lines by 32 pixels in YCbCr411, 16 lines by 16 pixels in YCbCr420

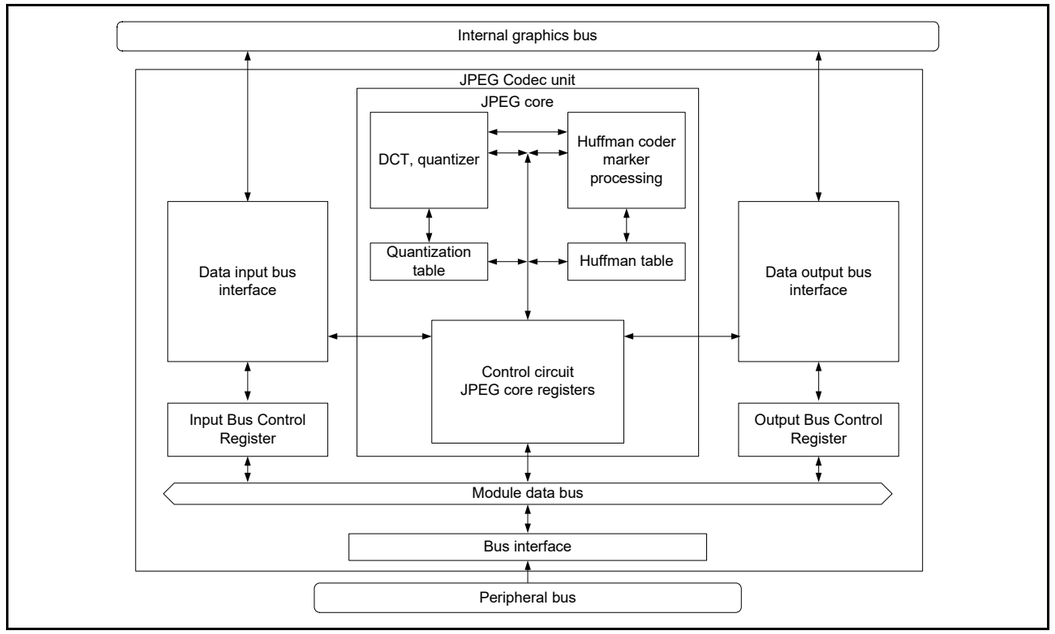


Figure 57.1 JPEG Codec block diagram

Note: When using the JPEG, set the clock to ICLK = PCLKA.

57. JPEG编解码器(JPEG)

57.1 Overview

JPEGCodec符合JPEG基线压缩和解压缩标准，可提供图像数据的高速压缩和JPEG数据的高速解码。表57.1列出了JPEG编解码器规范，图57.1显示了框图。

Table 57.1 JPEG编解码器规格

Parameter	Specifications
符合标准	在本文档描述的范围内符合JPEGBaseline标准。 JPEG编解码器不支持以下功能： 使用两个元素进行扫描 使用多个元素进行非交错扫描
操作精度	符合JPEG第2部分，ISO-IEC10918-2
图像输入输出系统	块交错法
像素格式	压缩：YCbCr422(H=2:1:1 V=1:1:1) 减压：YCbCr444(H=1:1:1 V=1:1:1) YCbCr422(H=2:1):1 V=1:1:1) YCbCr411(H=4:1:1 V=1:1:1) YCbCr420(H=2:1:1 V=2:1:1) 输出像素格式到缓冲区：ARGB8888、RGB565
量化表	提供四张桌子
Huffman table	提供四个表格（两个表格用于交流系数，两个表格用于直流系数）
支持的标记	SOI（图像开始）、SOF0（帧类型0开始）、SOS（扫描开始）、DQT（定义量化表）、DHT（定义霍夫曼表）、DRI（定义重启间隔）、RSTm（重启标记）、和EOI（图片结束）
处理单元	8字节地址边界单元可设置
可处理的图像尺寸	可被最小编码单元(MCU)整除的尺寸：YCbCr444中8行x8像素，YCbCr422中8行x16像素，YCbCr411中8行x32像素，YCbCr420中16行x16像素

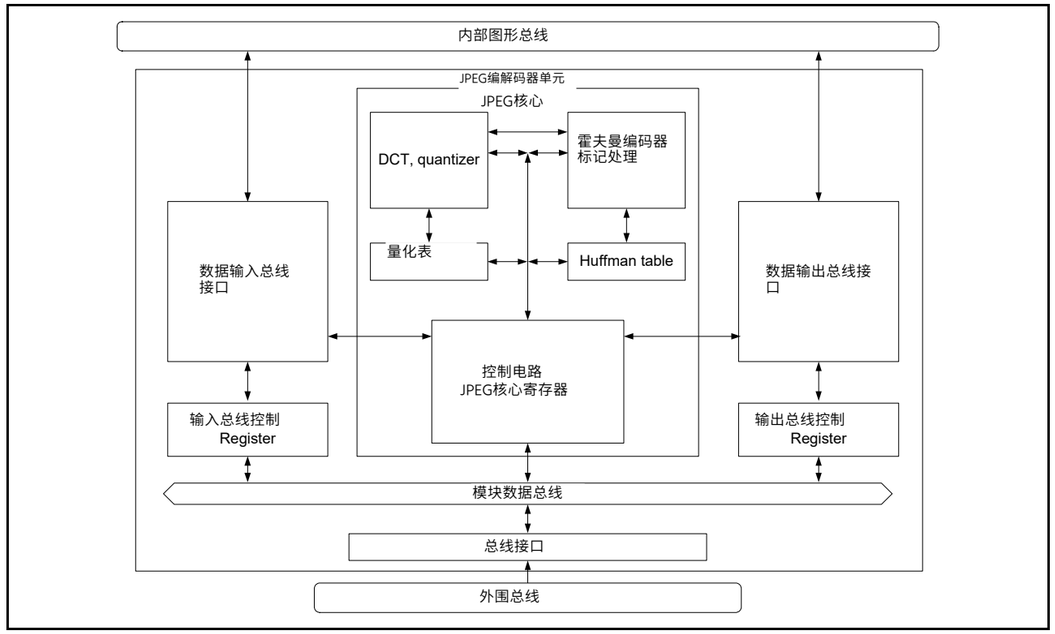


Figure 57.1 JPEG编解码器框图

Note: 使用JPEG时，将时钟设置为ICLK=PCLKA。

57.2 Register Descriptions

57.2.1 JPEG Code Mode Register (JCMOD)

Address(es): JPEG.JCMOD 400E 6000h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	DSP	REDU[2:0]		
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	REDU[2:0]	Pixel Format	• With compression b2 b0 0 0 1: YCbCr422. Other settings are prohibited. • With decompression b2 b0 0 0 0: YCbCr444 0 0 1: YCbCr422 1 1 0: YCbCr411 0 1 0: YCbCr420. Other settings result in an error. The JPEG Codec cannot process them normally.	R/W*2
b3	DSP	Compression/Decompression Set*1	0: Select compression process 1: Select decompression process.	R/W
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. When changing between processing for compression and decompression, you must reset the JPEG Codec in advance by setting the BRST bit in JPEG Code Command Register (JCCMD).
Note 2. In decompression mode, these bits are read-only.

57.2.2 JPEG Code Command Register (JCCMD)

Address(es): JPEG.JCCMD 400E 6001h

	b7	b6	b5	b4	b3	b2	b1	b0
	BRST	—	—	—	—	JEND	JRST	JSRT
Value after reset:	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	Bit name	Description	R/W
b0	JSRT	JPEG Core Process Start Command	Set this bit to 1 to start JPEG core processing. Do not write this bit to 1 again while the JPEG Codec is in operation.	W
b1	JRST	JPEG Core Process Stop Clear Command	Set this bit to 1 to clear the process-stopped state caused by requests to read the image size and pixel format (enabled in the INT3 bit in JINTE0).	W*1
b2	JEND	Interrupt Request Clear Command	Set this bit to 1 to clear an interrupt request. This bit is only valid for the interrupt sources associated with the INS6, INS5, and INS3 bits in JINTS0.	W

57.2 注册说明

57.2.1 JPEG代码模式寄存器(JCMOD)

Address(es): JPEG.JCMOD 400E 6000h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	DSP	REDU[2:0]		
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b2 to b0	REDU[2:0]	像素格式	带压缩b2b0001：YCbCr422。禁止其他设置。 减压b2b000：YCbCr444001：YCbCr422110：YCbCr411010：YCbCr420。其他设置会导致错误。JPEG编解码器无法正常处理它们。	R/W*2
b3	DSP	Compression/Decompression Set*1	0：选择压缩过程1：选择解压缩过程。	R/W
b7 to b4	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 在压缩处理和解压缩处理之间切换时，必须通过设置JPEG代码命令寄存器(JCCMD)中的BRST位来提前复位JPEG编解码器。
Note 2. 在解压缩模式下，这些位是只读的。

57.2.2 JPEG代码命令寄存器(JCCMD)

Address(es): JPEG.JCCMD 400E 6001h

	b7	b6	b5	b4	b3	b2	b1	b0
	BRST	—	—	—	—	JEND	JRST	JSRT
重置后的值：	x	x	x	x	x	x	x	x

x: Undefined

Bit	Symbol	位名称	Description	R/W
b0	JSRT	JPEG核心进程启动命令	将此位设置为1以启动JPEG核心处理。在JPEG编解码器运行时，不要再次将此位写入1。	W
b1	JRST	JPEG核心进程停止清除Command	将此位设置为1以清除因请求读取图像大小和像素格式（在JINTE0的INT3位中启用）导致的进程停止状态。	W*1
b2	JEND	中断请求清除命令	将此位设置为1以清除中断请求。该位仅对与JINTS0中的INS6、INS5和INS3位相关的中断源有效。	W

Bit	Symbol	Bit name	Description	R/W
b6 to b3	—	Reserved	The write value should be 0.	W
b7	BRST	Bus Reset	Set this bit to 1 to reset the JCDTCU, JCDTCM, JCDTCD, JCDERR and JCRST registers. Do not set this bit to 1 while the JPEG Codec is in operation (from setting the JPEG core process start command to writing the last output code and image data). For the bus reset processing, see section 57.5, Bus Reset Processing.	W

Note: Clearing the bits in this register to 0 after setting a command is not required. Multiple commands must not be set simultaneously.
Note 1. In compression mode, this bit is invalid.

57.2.3 JPEG Code Quantization Table Number Register (JCQTN)

Address(es): JPEG.JCQTN 400E 6003h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	QT3[1:0]		QT2[1:0]		QT1[1:0]	
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	QT1[1:0]	Quantization Table Number for the First Color Component	b1 b0 0 0: Quantization table 0 (JCQTBL0) 0 1: Quantization table 1 (JCQTBL1) 1 0: Quantization table 2 (JCQTBL2) 1 1: Quantization table 3 (JCQTBL3).	R/W*1
b3, b2	QT2[1:0]	Quantization Table Number for the Second Color Component	b3 b2 0 0: Quantization table 0 (JCQTBL0) 0 1: Quantization table 1 (JCQTBL1) 1 0: Quantization table 2 (JCQTBL2) 1 1: Quantization table 3 (JCQTBL3).	R/W*1
b5, b4	QT3[1:0]	Quantization Table Number for the Third Color Component	b5 b4 0 0: Quantization table 0 (JCQTBL0) 0 1: Quantization table 1 (JCQTBL1) 1 0: Quantization table 2 (JCQTBL2) 1 1: Quantization table 3 (JCQTBL3).	R/W*1
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. In decompression mode, these bits are read-only.

Bit	Symbol	位名称	Description	R/W
b6 to b3	—	Reserved	写入值应为0。	W
b7	BRST	总线复位	将此位设置为1可复位JCDTCU、JCDTCM、JCDTCD、JCDERR和JCRST寄存器。 在JPEG编解码器运行时（从设置JPEG核心进程启动命令到写入最后的输出代码和图像数据），请勿将此位设置为1。 关于总线复位处理，请参阅第57.5节，总线复位 Processing.	W

Note: 不需要在设置命令后将该寄存器中的位清除为0。不能同时设置多个命令。

Note 1. 在压缩模式下，该位无效。

57.2.3 JPEG码量化表编号寄存器（JCQTN）

Address(es): JPEG.JCQTN 400E 6003h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	QT3[1:0]		QT2[1:0]		QT1[1:0]	
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b1, b0	QT1[1:0]	第一个颜色分量的量化表编号	b1b000：量化表0（JCQTBL0）01：量化表1（JCQTBL1）10：量化表2（JCQTBL2）11：量化表3（JCQTBL3）。	R/W*1
b3, b2	QT2[1:0]	第二颜色分量的量化表编号	b3b200：量化表0（JCQTBL0）01：量化表1（JCQTBL1）10：量化表2（JCQTBL2）11：量化表3（JCQTBL3）。	R/W*1
b5, b4	QT3[1:0]	第三颜色分量的量化表编号	b5b400：量化表0（JCQTBL0）01：量化表1（JCQTBL1）10：量化表2（JCQTBL2）11：量化表3（JCQTBL3）。	R/W*1
b7, b6	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 在解压缩模式下，这些位是只读的。

57.2.4 JPEG Code Huffman Table Number Register (JCHTN)

Address(es): JPEG.JCHTN 400E 6004h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	HTA3	HTD3	HTA2	HTD2	HTA1	HTD1
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	HTD1	Huffman Table Number (DC) for the First Color Component	b1 b0 0 0: DC/AC Huffman table 0 (JCHTBD0 and JCHTBA0) 1 1: DC/AC Huffman table 1 (JCHTBD1 and JCHTBA1). Other settings are prohibited.	R/W*1
b1	HTA1	Huffman Table Number (AC) for the First Color Component		R/W*1
b2	HTD2	Huffman Table Number (DC) for the Second Color Component	b3 b2 0 0: DC/AC Huffman table 0 (JCHTBD0 and JCHTBA0) 1 1: DC/AC Huffman table 1 (JCHTBD1 and JCHTBA1). Other settings are prohibited.	R/W*1
b3	HTA2	Huffman Table Number (AC) for the Second Color Component		R/W*1
b4	HTD3	Huffman Table Number (DC) for the Third Color Component	b5 b4 0 0: DC/AC Huffman table 0 (JCHTBD0 and JCHTBA0) 1 1: DC/AC Huffman table 1 (JCHTBD1 and JCHTBA1). Other settings are prohibited.	R/W*1
b5	HTA3	Huffman Table Number (AC) for the Third Color Component		R/W*1
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. In decompression mode, these bits are read-only.

57.2.5 JPEG Code DRI Upper Register (JCDRIU)

Address(es): JPEG.JCDRIU 400E 6005h

	b7	b6	b5	b4	b3	b2	b1	b0
	DRIU[7:0]							
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	DRIU[7:0]	Upper Bytes of MCUs Preceding RST Marker	Valid settings: 00h to FFh (0 to 255).*1	R/W*2

Note 1. When both JCDRIU = 00h and JCDRID = 00h, neither the DRI nor the RST marker is placed.
Note 2. In decompression mode, these bits are invalid.

57.2.4 JPEG代码霍夫曼表编号寄存器(JCHTN)

Address(es): JPEG.JCHTN 400E 6004h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	HTA3	HTD3	HTA2	HTD2	HTA1	HTD1
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	HTD1	第一个颜色分量的霍夫曼表编号(DC)	b1b000：直流交流霍夫曼表0（JCHTBD0和JCHTBA0） 1：直流交流霍夫曼表1（JCHTBD1和JCHTBA1）。禁止其他设置。	R/W*1
b1	HTA1	第一个颜色分量的霍夫曼表编号(AC)		R/W*1
b2	HTD2	第二个颜色分量的霍夫曼表编号(DC)	b3b200：直流交流霍夫曼表0（JCHTBD0和JCHTBA0） 1：直流交流霍夫曼表1（JCHTBD1和JCHTBA1）。禁止其他设置。	R/W*1
b3	HTA2	第二个颜色分量的霍夫曼表编号(AC)		R/W*1
b4	HTD3	第三个颜色分量的霍夫曼表编号(DC)	b5b400：直流交流霍夫曼表0（JCHTBD0和JCHTBA0） 1：直流交流霍夫曼表1（JCHTBD1和JCHTBA1）。禁止其他设置。	R/W*1
b5	HTA3	第三个颜色分量的霍夫曼表编号(AC)		R/W*1
b7, b6	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 在解压缩模式下，这些位是只读的。

57.2.5 JPEG代码DRI上位寄存器(JCDRIU)

Address(es): JPEG.JCDRIU 400E 6005h

	b7	b6	b5	b4	b3	b2	b1	b0
	DRIU[7:0]							
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b7 to b0	DRIU[7:0]	前面MCU的高字节 RST Marker	有效设置：00h到FFh（0到255）。*1	R/W*2

Note 1. 当JCDRIU=00h和JCDRID=00h时，既不放置DRI也不放置RST标记。
Note 2. 在解压模式下，这些位无效。

57.2.6 JPEG Code DRI Lower Register (JCDRID)

Address(es): JPEG.JCDRID 400E 6006h

	b7	b6	b5	b4	b3	b2	b1	b0
	DRIU[7:0]							
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	DRIU[7:0]	Lower Bytes of MCUs Preceding RST Marker	Valid settings: 00h to FFh (0 to 255).*1	R/W*2

Note 1. When both JCDRIU = 00h and JCDRID = 00h, neither the DRI nor the RST marker is placed.
Note 2. In decompression mode, these bits are invalid.

57.2.7 JPEG Code Vertical Size Upper Register (JCVSZU)

Address(es): JPEG.JCVSZU 400E 6007h

	b7	b6	b5	b4	b3	b2	b1	b0
	VSZU[7:0]							
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	VSZU[7:0]	Upper Bytes of Vertical Image Size	Valid settings: 00h to FFh (0 to 255).*2	R/W*1

Note 1. In decompression mode, these bits are read-only.
Note 2. In the decompression process, a downloaded value from the JPEG coded data is set.

57.2.8 JPEG Code Vertical Size Lower Register (JCVSZD)

Address(es): JPEG.JCVSZD 400E 6008h

	b7	b6	b5	b4	b3	b2	b1	b0
	VSZD[7:0]							
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	VSZD[7:0]	Lower Bytes of Vertical Image Size	Valid settings: 00h to FFh (0 to 255).*2	R/W*1

Note 1. In decompression mode, these bits are read-only.
Note 2. In the decompression process, a downloaded value from the JPEG coded data is set.

57.2.6 JPEG代码DRI低位寄存器(JCDRID)

Address(es): JPEG.JCDRID 400E 6006h

	b7	b6	b5	b4	b3	b2	b1	b0
	DRIU[7:0]							
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b7 to b0	DRIU[7:0]	RST标记之前的MCU的低字节	有效设置：00h到FFh（0到255）。*1	R/W*2

Note 1. 当JCDRIU=00h和JCDRID=00h时，既不放置DRI也不放置RST标记。
Note 2. 在解压模式下，这些位无效。

57.2.7 JPEG代码垂直大小上寄存器(JCVSZU)

Address(es): JPEG.JCVSZU 400E 6007h

	b7	b6	b5	b4	b3	b2	b1	b0
	VSZU[7:0]							
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b7 to b0	VSZU[7:0]	垂直图像大小的高字节	有效设置：00h到FFh（0到255）。*2	R/W*1

Note 1. 在解压缩模式下，这些位是只读的。
Note 2. 在解压缩过程中，设置来自JPEG编码数据的下载值。

57.2.8 JPEG代码垂直大小低位寄存器(JCVSZD)

Address(es): JPEG.JCVSZD 400E 6008h

	b7	b6	b5	b4	b3	b2	b1	b0
	VSZD[7:0]							
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b7 to b0	VSZD[7:0]	垂直图像大小的低字节	有效设置：00h到FFh（0到255）。*2	R/W*1

Note 1. 在解压缩模式下，这些位是只读的。
Note 2. 在解压缩过程中，设置来自JPEG编码数据的下载值。

57.2.9 JPEG Code Horizontal Size Upper Register (JCHSZU)

Address(es): JPEG.JCHSZU 400E 6009h

	b7	b6	b5	b4	b3	b2	b1	b0
	HSZU[7:0]							
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	HSZU[7:0]	Upper Bytes of Horizontal Image Size	Valid settings: 00h to FFh (0 to 255).*2	R/W*1

Note 1. In decompression mode, these bits are read-only.
Note 2. In the decompression process, a downloaded value from the JPEG coded data is set.

57.2.10 JPEG Coded Horizontal Size Lower Register (JCHSZD)

Address(es): JPEG.JCHSZD 400E 600Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	HSZD[7:0]							
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	HSZD[7:0]	Lower Bytes of Horizontal Image Size	Valid settings: 00h to FFh (0 to 255).*2	R/W*1

Note 1. In decompression mode, these bits are read-only.
Note 2. In the decompression process, a downloaded value from the JPEG coded data is set.

57.2.11 JPEG Code Data Count Upper Register (JCDTCU)

Address(es): JPEG.JCDTCU 400E 600Bh

	b7	b6	b5	b4	b3	b2	b1	b0
	DCU[7:0]							
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	DCU[7:0]	Upper Bytes of Counted Amount of Data to Be Compressed	Valid settings: 00h to FFh (0 to 255).	R*2

Note 1. The values in this register are reset before compression starts.
Note 2. In decompression mode, these bits are invalid.

57.2.9 JPEG代码水平尺寸上限寄存器(JCHSZU)

Address(es): JPEG.JCHSZU 400E 6009h

	b7	b6	b5	b4	b3	b2	b1	b0
	HSZU[7:0]							
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b7 to b0	HSZU[7:0]	水平图像大小的高字节	有效设置：00h到FFh（0到255）。*2	R/W*1

Note 1. 在解压缩模式下，这些位是只读的。
Note 2. 在解压缩过程中，设置来自JPEG编码数据的下载值。

57.2.10 JPEG编码水平尺寸低位寄存器(JCHSZD)

Address(es): JPEG.JCHSZD 400E 600Ah

	b7	b6	b5	b4	b3	b2	b1	b0
	HSZD[7:0]							
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b7 to b0	HSZD[7:0]	水平图像大小的低字节	有效设置：00h到FFh（0到255）。*2	R/W*1

Note 1. 在解压缩模式下，这些位是只读的。
Note 2. 在解压缩过程中，设置来自JPEG编码数据的下载值。

57.2.11 JPEG代码数据计数高位寄存器(JCDTCU)

Address(es): JPEG.JCDTCU 400E 600Bh

	b7	b6	b5	b4	b3	b2	b1	b0
	DCU[7:0]							
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b7 to b0	DCU[7:0]	待计数数据量的高字节 Compressed	有效设置：00h到FFh（0到255）。	R*2

Note 1. 该寄存器中的值在压缩开始前被复位。
Note 2. 在解压模式下，这些位无效。

57.2.12 JPEG Code Data Count Middle Register (JCDTCM)

Address(es): JPEG.JCDTCM 400E 600Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	DCM[7:0]							
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	DCM[7:0]	Middle Bytes of Counted Amount of Data to Be Compressed	Valid settings: 00h to FFh (0 to 255).	R*2

Note 1. The values in this register are reset before compression starts.
Note 2. In decompression mode, these bits are invalid.

57.2.13 JPEG Code Data Count Lower Register (JCDTCD)

Address(es): JPEG.JCDTCD 400E 600Dh

	b7	b6	b5	b4	b3	b2	b1	b0
	DCD[7:0]							
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	DCD[7:0]	Lower Bytes of Counted Amount of Data to Be Compressed	Valid settings: 00h to FFh (0 to 255).	R*2

Note 1. The values in this register are reset before compression starts.
Note 2. In decompression mode, these bits are invalid.

57.2.14 JPEG Interrupt Enable Register 0 (JINTE0)

Address(es): JPEG.JINTE0 400E 600Eh

	b7	b6	b5	b4	b3	b2	b1	b0
	INT7	INT6	INT5	—	INT3	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b3	INT3	Interrupt Request Signal INS3 Enable Control	Enables interrupt generation when determined that image size and pixel format of compressed data can be read by analyzing the data.	R/W*2
b4	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b5	INT5	Interrupt Request Last MCU Data Number Error Enable Control	Enables interrupt generation when final number of MCU data units in Huffman-coding segment is not correct in decompression. When this bit is not set to enable, no error code is returned.	R/W*2
b6	INT6	Interrupt Request Total Number Error Enable Control	Enables interrupt generation when total number of data units in Huffman-coding segment is not correct in decompression. When this bit is not set to enable, no error code is returned.	R/W*2

57.2.12 JPEG代码数据计数中间寄存器(JCDTCM)

Address(es): JPEG.JCDTCM 400E 600Ch

	b7	b6	b5	b4	b3	b2	b1	b0
	DCM[7:0]							
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b7 to b0	DCM[7:0]	待统计数据量的中间字节 Compressed	有效设置：00h到FFh（0到255）。	R*2

Note 1. 该寄存器中的值在压缩开始前被复位。
Note 2. 在解压模式下，这些位无效。

57.2.13 JPEG代码数据计数低位寄存器(JCDTCD)

Address(es): JPEG.JCDTCD 400E 600Dh

	b7	b6	b5	b4	b3	b2	b1	b0
	DCD[7:0]							
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b7 to b0	DCD[7:0]	计数数据量的低字节 Compressed	有效设置：00h到FFh（0到255）。	R*2

Note 1. 该寄存器中的值在压缩开始前被复位。
Note 2. 在解压模式下，这些位无效。

57.2.14 JPEG中断使能寄存器0(JINTE0)

Address(es): JPEG.JINTE0 400E 600Eh

	b7	b6	b5	b4	b3	b2	b1	b0
	INT7	INT6	INT5	—	INT3	—	—	—
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b2 to b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b3	INT3	中断请求信号INS3 启用控制	当确定可以通过分析数据读取压缩数据的图像大小和像素格式时，启用中断生成。	R/W*2
b4	—	Reserved	该位读取为0。写入值应为0。	R/W
b5	INT5	中断请求最后MCU数据编号 错误使能 Control	当Huffman编码段中的最终MCU数据单元数在解压缩中不正确时，启用中断生成。当该位未设置为使能时，不返回错误代码。	R/W*2
b6	INT6	中断请求总数 错误启用控制	当数据单元总数在 Huffman编码段在解压时不正确。 当该位未设置为使能时，不返回错误代码。	R/W*2

Bit	Symbol	Bit name	Description	R/W
b7	INT7	Interrupt Request Restart Interval Data Number Error Enable Control	Enables interrupt generation when number of data units in restart interval of Huffman-coding segment is not correct in decompression. When this bit is not set to enable, no error code is returned.	R/W*2

Note 1. When any of the bits from INT7 to INT5 sets to 1, the INS5 bit in the JINTS0 register indicates 1 as the error status on occurrence of the compression data error, and the ERR[3:0] bits in the JCDERR register indicate the specific error code.
Note 2. In compression mode, these bits are invalid.

57.2.15 JPEG Interrupt Status Register 0 (JINTS0)

Address(es): JPEG.JINTS0 400E 600Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	INS6	INS5	—	INS3	—	—	—
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b3	INS3	Request for Reading the Image Size and Pixel Format	This bit sets to 1 when image size and pixel format can be read. When an interrupt occurs, the JPEG Codec stops processing and the state is indicated in the JCRST register. To resume module processing, set the JPEG Core Process Stop Clear Command Bit (JRST) in JCCMD.	R/W*2, *3
b4	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b5	INS5	JPEG Decompression Error Occurrence	This bit sets to 1 when a compressed data error occurs.	R/W*2, *3
b6	INS6	JPEG Decompression Process End	This bit sets to 1 when the JPEG Codec completes compression process normally.	R/W*2
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Note 1. The interrupt sources in this register should be cleared by clearing the associated interrupt status bits to 0 and setting the relevant bit in JCCMD appropriately.
Note 2. Clear this bit by writing 0 to it. Do not write 1 to this bit.
Note 3. In compression mode, these bits are invalid.

57.2.16 JPEG Code Decode Error Register (JCDERR)

Address(es): JPEG.JCDERR 400E 6010h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	ERR[3:0]			
Value after reset:	0	0	0	0	1	0	1	0

Bit	Symbol	Bit name	Description	R/W
b3 to b0	ERR[3:0]	Error Code	See Table 57.3 and Table 57.4. for error codes.	R/W*2
b7 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. The values in this register are reset before the JPEG Codec starts decompression.
Note 2. In compression mode, these bits are invalid.

Bit	Symbol	位名称	Description	R/W
b7	INT7	中断请求重启 间隔数据编号错误 启用控制	当Huffman编码段的重新启动间隔中的数据单元数在解压缩时不正确时，启用中断生成。当该位未设置为使能时，不返回错误代码。	R/W*2

Note 1. 当INT7到INT5中的任何一位设置为1时，JINTS0寄存器中的INS5位指示1作为发生压缩数据错误时的错误状态，JCDERR寄存器中的ERR[3:0]位指示具体错误代码。
Note 2. 在压缩模式下，这些位无效。

57.2.15 JPEG中断状态寄存器0(JINTS0)

Address(es): JPEG.JINTS0 400E 600Fh

	b7	b6	b5	b4	b3	b2	b1	b0
	—	INS6	INS5	—	INS3	—	—	—
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b2 to b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b3	INS3	请求阅读 图像尺寸和像素 Format	当可以读取图像大小和像素格式时，该位设置为1。 发生中断时，JPEG编解码器停止处理并在JCRST寄存器中指示状态。要恢复模块处理，请在JCCMD中设置JPEG核心进程停止清除命令位(JRST)。	R/W*2, *3
b4	—	Reserved	该位读取为0。写入值应为0。	R/W
b5	INS5	JPEG解压 错误发生	当发生压缩数据错误时，该位设置为1。	R/W*2, *3
b6	INS6	JPEG解压 流程结束	当JPEGCodec正常完成压缩过程时，该位设置为1。	R/W*2
b7	—	Reserved	该位读取为0。写入值应为0。	R/W

Note 1. 该寄存器中的中断源应通过将相关中断状态位清除为0并适当设置JCCMD中的相关位来清除。

Note 2. 通过向该位写入0来清除该位。不要向该位写入1。
Note 3. 在压缩模式下，这些位无效。

57.2.16 JPEG代码解码错误寄存器(JCDERR)

Address(es): JPEG.JCDERR 400E 6010h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	ERR[3:0]			
重置后的值：	0	0	0	0	1	0	1	0

Bit	Symbol	位名称	Description	R/W
b3 to b0	ERR[3:0]	错误代码	见表57.3和表57.4。对于错误代码。	R/W*2
b7 to b4	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 该寄存器中的值在JPEG编解码器开始解压缩之前复位。
Note 2. 在压缩模式下，这些位无效。

57.2.17 JPEG Code Reset Register (JCRST)

Address(es): JPEG.JCRST 400E 6011h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	RST
Value after reset:	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	RST	Operating State	0: All other states 1: Suspended state caused by JINTE0 interrupt sources.	R*2
b7 to b1	—	Reserved	These bits are read as 0.	R

Note 1. To resume processing, set the JPEG core process stop clear command bit (JRST) in JCCMD.
Note 2. In compression mode, this bit is invalid.

57.2.18 JPEG Interface Compression Control Register (JIFECNT)

Address(es): JPEG.JIFECNT 400E 6040h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	JOUTSWAP[2:0]		—	DINRINI	DINRCMD	DINLC	—	DINSWAP[2:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	DINSWAP[2:0]	Byte/Halfword/Word Swap	Swaps input image data in compression. b2 b0 0 0 0: (1) (2) (3) (4) (5) (6) (7) (8) 0 0 1: (2) (1) (4) (3) (6) (5) (8) (7) [Byte swap] 0 1 0: (3) (4) (1) (2) (7) (8) (5) (6) [Halfword swap] 0 1 1: (4) (3) (2) (1) (8) (7) (6) (5) [Halfword - byte swap] 1 0 0: (5) (6) (7) (8) (1) (2) (3) (4) [Word swap] 1 0 1: (6) (5) (8) (7) (2) (1) (4) (3) [Word - byte swap] 1 1 0: (7) (8) (5) (6) (3) (4) (1) (2) [Word - halfword swap] 1 1 1: (8) (7) (6) (5) (4) (3) (2) (1) [Word - halfword - byte swap].	R/W*1
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	DINLC	Count Mode Setting for Stopping Input Image Data Lines	0: Turn off count mode for stopping input of image data lines 1: Turn on count mode for stopping input of image data lines.	R/W*1
b5	DINRCMD	Input Image Data Lines Resume Command	Set this bit to 1 to resume reading of input image data. This bit is only valid when the count mode for stopping input of image data lines is on. This bit is always read as 0.	W*1
b6	DINRINI	Address Initialization when Resuming Input of Image Data Lines	This bit is only valid when the count mode for stopping input of image data lines is on. Set this bit before writing 1 to the data-line resume command bit. 0: Do not initialize transfer address when input of image data lines restarts 1: Initialize transfer address when input of image data lines restarts.	R/W*1
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

57.2.17 JPEG代码重置寄存器(JCRST)

Address(es): JPEG.JCRST 400E 6011h

	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	RST
重置后的值：	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	RST	工作状态	0：所有其他状态1：由JINTE0中断源引起的挂起状态。	R*2
b7 to b1	—	Reserved	这些位读为0。	R

Note 1. 要恢复处理，请在JCCMD中设置JPEG核心进程停止清除命令位(JRST)。
Note 2. 在压缩模式下，该位无效。

57.2.18 JPEG接口压缩控制寄存器(JIFECNT)

Address(es): JPEG.JIFECNT 400E 6040h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	JOUTSWAP[2:0]		—	DINRINI	DINRCMD	DINLC	—	DINSWAP[2:0]			
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b2 to b0	DINSWAP[2:0]	Byte/Halfword/Word Swap	交换压缩中的输入图像数据。b2b0000:(1)(2)(3)(4)(5)(6)(7)(8)001:(2)(1)(4)(3)(6)(5)(8)(7)[字节交换]010:(3)(4)(1)(2)(7)(8)(5)(6)[半字交换]011:(4)(3)(2)(1)(8)(7)(6)(5)[半字字节交换]100:(5)(6)(7)(8)(1)(2)(3)(4)[字交换]101:(6)(5)(8)(7)(2)(1)(4)(3)[字字节交换]110:(7)(8)(5)(6)(3)(4)(1)(2)[字半字交换]111:(8)(7)(6)(5)(4)(3)(2)(1)[字半字字节交换]。	R/W*1
b3	—	Reserved	该位读取为0。写入值应为0。	R/W
b4	DINLC	计数模式设置 停止输入图像 数据线	0：关闭计数模式，停止输入图像数据线1：打开计数模式， 停止输入图像数据线。	R/W*1
b5	DINRCMD	输入图像数据线 恢复命令	将此位设置为1以恢复读取输入图像数据。 该位仅在停止输入图像数据线的计数模式打开时有效。该位始终读为0。	W*1
b6	DINRINI	恢复输入图像数据行时的地址初始化	该位仅在停止输入图像数据线的计数模式打开时有效。在将1写入数据线恢复命令位之前设置该位。0：重新输入图像数据线时不初始化传输地址1：重新输入图像数据线时初始化传输地址。	R/W*1
b7	—	Reserved	该位读取为0。写入值应为0。	R/W

Bit	Symbol	Bit name	Description	R/W
b10 to b8	JOUTSWAP[2:0]	Byte/Halfword/Word Swap	Swaps output coded data in compression. b10 b8 0 0 0: (1) (2) (3) (4) (5) (6) (7) (8) 0 0 1: (2) (1) (4) (3) (6) (5) (8) (7) [Byte swap] 0 1 0: (3) (4) (1) (2) (7) (8) (5) (6) [Halfword swap] 0 1 1: (4) (3) (2) (1) (8) (7) (6) (5) [Halfword - byte swap] 1 0 0: (5) (6) (7) (8) (1) (2) (3) (4) [Word swap] 1 0 1: (6) (5) (8) (7) (2) (1) (4) (3) [Word - byte swap] 1 1 0: (7) (8) (5) (6) (3) (4) (1) (2) [Word - halfword swap] 1 1 1: (8) (7) (6) (5) (4) (3) (2) (1) [Word - halfword - byte swap].	R/W*1
b31 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. In decompression mode, these bits are invalid.

57.2.19 JPEG Interface Compression Source Address Register (JIFESA)

Address(es): JPEG.JIFESA 400E 6044h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	ESA[31:16]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ESA[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	ESA[2:0]	Input Image Data Source Address	The lower three bits should be set to 0. These bits are read as 0.	R/W
b31 to b3	ESA[31:3]		Input image data source address in 8-byte units.	R/W*2

Note 1. This register must be set in 8-byte units.
Note 2. In decompression mode, these bits are invalid.

57.2.20 JPEG Interface Compression Line Offset Register (JIFESOFST)

Address(es): JPEG.JIFESOFST 400E 6048h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	ESMW[14:0]														
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	ESMW[2:0]	Input Image Data Lines Offset	The lower three bits should be set to 0. These bits are read as 0.	R/W*2
b14 to b3	ESMW[14:3]		Input image data lines offset in 8-byte units.	R/W*2
b31 to b15	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. This register must be set in 8-byte units.

Bit	Symbol	位名称	Description	R/W
b10 to b8	JOUTSWAP[2:0]	Byte/Halfword/Word Swap	交换压缩中的输出编码数据。b10b8000:(1)(2)(3)(4)(5)(6)(7)(8)001:(2)(1)(4)(3)(6)(5)(8)(7)[字节交换]010:(3)(4)(1)(2)(7)(8)(5)(6)[半字交换]011:(4)(3)(2)(1)(8)(7)(6)(5)[半字字节交换]100:(5)(6)(7)(8)(1)(2)(3)(4)[字交换]101:(6)(5)(8)(7)(2)(1)(4)(3)[字字节交换]110:(7)(8)(5)(6)(3)(4)(1)(2)[字半字交换]111:(8)(7)(6)(5)(4)(3)(2)(1)[字半字字节交换]。	R/W*1
b31 to b11	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 在解压模式下，这些位无效。

57.2.19 JPEG接口压缩源地址寄存器(JIFESA)

Address(es): JPEG.JIFESA 400E 6044h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	ESA[31:16]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	ESA[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b2 to b0	ESA[2:0]	输入图像数据源 Address	低三位应设置为0。这些位被读取为0。	R/W
b31 to b3	ESA[31:3]		以8字节为单位输入图像数据源地址。	R/W*2

Note 1. 该寄存器必须以8字节为单位进行设置。
Note 2. 在解压模式下，这些位无效。

57.2.20 JPEG接口压缩线偏移寄存器(JIFESOFST)

Address(es): JPEG.JIFESOFST 400E 6048h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	ESMW[14:0]														
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b2 to b0	ESMW[2:0]	输入图像数据线偏移	低三位应设置为0。这些位被读取为0。	R/W*2
b14 to b3	ESMW[14:3]		输入图像数据行以8字节为单位偏移。	R/W*2
b31 to b15	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 该寄存器必须以8字节为单位进行设置。

Note 2. In decompression mode, these bits are invalid.

57.2.21 JPEG Interface Compression Destination Address Register (JIFEDA)

Address(es): JPEG.JIFEDA 400E 604Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	EDA[31:16]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	EDA[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	EDA[2:0]	Output Coded Data Destination Address	The lower three bits should be set to 0. These bits are read as 0.	R/W*2
b31 to b3	EDA[31:3]		Output coded data destination address in 8-byte units.	R/W*2

Note 1. This register must be set in 8-byte units.
Note 2. In decompression mode, these bits are invalid.

57.2.22 JPEG Interface Compression Source Line Count Register (JIFESLC)

Address(es): JPEG.JIFESLC 400E 6050h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	LINES[15:0]															
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	LINES[2:0]	Number of Input Image Data Lines to Be Read	The lower three bits should be set to 0. These bits are read as 0.	R/W*2
b15 to b3	LINES[15:3]		Number of input image data lines to be read, in 8-line units.	R/W*2
b18 to b16	—	Reserved	These bits are read as undefined. The write value should be 0.	R/W
b31 to b19	—	Reserved	These bits are read as undefined. The write value should be 1	R

Note 1. This register must be set in 8-byte units.
Note 2. In decompression mode, these bits are invalid.

Note 2. 在解压模式下，这些位无效。

57.2.21 JPEG接口压缩目标地址寄存器(JIFEDA)

Address(es): JPEG.JIFEDA 400E 604Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	EDA[31:16]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	EDA[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b2 to b0	EDA[2:0]	输出编码数据目的地 Address	低三位应设置为0。这些位被读取为0。	R/W*2
b31 to b3	EDA[31:3]		以8字节为单位输出编码数据目标地址。	R/W*2

Note 1. 该寄存器必须以8字节为单位进行设置。
Note 2. 在解压模式下，这些位无效。

57.2.22 JPEG接口压缩源行计数寄存器(JIFESLC)

Address(es): JPEG.JIFESLC 400E 6050h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	LINES[15:0]															
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0

Bit	Symbol	位名称	Description	R/W
b2 to b0	LINES[2:0]	输入图像数据数要阅读的行	低三位应设置为0。这些位被读取为0。	R/W*2
b15 to b3	LINES[15:3]		要读取的输入图像数据行数，以8行为单位。	R/W*2
b18 to b16	—	Reserved	这些位被读取为未定义。写入值应为0。	R/W
b31 to b19	—	Reserved	这些位被读取为未定义。写入值应为1	R

Note 1. 该寄存器必须以8字节为单位进行设置。
Note 2. 在解压模式下，这些位无效。

57.2.23 JPEG Interface Decompression Control Register (JIFDCNT)

Address(es): JPEG.JIFDCNT 400E 6058h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	VINTER[1:0]		HINTER[1:0]		OPF[1:0]		—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	JINRINI	JINRC MD	JINC	—	JINSWAP[2:0]			—	DOUTR INI	DOUTR CMD	DOUTL C	—	DOUTSWAP[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	DOUTSWAP[2:0]	Byte/Halfword/Word Swap	Swaps output image data in decompression. b2 b0 0 0 0: (1) (2) (3) (4) (5) (6) (7) (8) 0 0 1: (2) (1) (4) (3) (6) (5) (8) (7) [Byte swap] 0 1 0: (3) (4) (1) (2) (7) (8) (5) (6) [Halfword swap] 0 1 1: (4) (3) (2) (1) (8) (7) (6) (5) [Halfword - byte swap] 1 0 0: (5) (6) (7) (8) (1) (2) (3) (4) [Word swap] 1 0 1: (6) (5) (8) (7) (2) (1) (4) (3) [Word - byte swap] 1 1 0: (7) (8) (5) (6) (3) (4) (1) (2) [Word - halfword swap] 1 1 1: (8) (7) (6) (5) (4) (3) (2) (1) [Word - halfword - byte swap].	R/W*1
b3	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b4	DOUTLC	Count Mode for Stopping Output Image Data Lines	0: Turn off count mode for stopping output of image data lines 1: Turn on count mode for stopping output of image data lines.	R/W*1
b5	DOUTRCMD	Output Image Data Lines Resume Command	Set this bit to 1 to resume writing of image data. This bit is only valid when the count mode for stopping output of image data lines is on. This bit is always read as 0.	W*1
b6	DOUTRINI	Address Initialization When Resuming Output of Image Data Lines	This bit is only valid when the count mode for stopping output of image data lines is on. Set this bit before writing 1 to the data-line resume command bit. 0: Do not initialize transfer address when output of image data lines restarts 1: Initialize transfer address when output of image data lines restarts.	R/W*1
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b10 to b8	JINSWAP[2:0]	Byte/Halfword/Word Swap	Swaps input coded data in decompression. b10 b8 0 0 0: (1) (2) (3) (4) (5) (6) (7) (8) 0 0 1: (2) (1) (4) (3) (6) (5) (8) (7) [Byte swap] 0 1 0: (3) (4) (1) (2) (7) (8) (5) (6) [Halfword swap] 0 1 1: (4) (3) (2) (1) (8) (7) (6) (5) [Halfword - byte swap] 1 0 0: (5) (6) (7) (8) (1) (2) (3) (4) [Word swap] 1 0 1: (6) (5) (8) (7) (2) (1) (4) (3) [Word - byte swap] 1 1 0: (7) (8) (5) (6) (3) (4) (1) (2) [Word - halfword swap] 1 1 1: (8) (7) (6) (5) (4) (3) (2) (1) [Word - halfword - byte swap].	R/W*1
b11	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b12	JINC	Count Mode Setting for Stopping Input Coded Data	0: Turn off count mode for stopping input of coded data 1: Turn on count mode for stopping input of coded data.	R/W*1
b13	JINRCMD	Input Coded Data Resume Command	Set this bit to 1 to resume reading of input coded data. This bit is only valid when the count mode for stopping input of coded data is on. This bit is always read as 0.	W*1

57.2.23 JPEG接口解压缩控制寄存器(JIFDCNT)

Address(es): JPEG.JIFDCNT 400E 6058h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	VINTER[1:0]		HINTER[1:0]		OPF[1:0]		—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	JINRINI	JINRC MD	JINC	—	JINSWAP[2:0]			—	DOUTR INI	DOUTR CMD	DOUTL C	—	DOUTSWAP[2:0]		
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b2 to b0	DOUTSWAP[2:0]	Byte/Halfword/Word Swap	在解压缩中交换输出图像数据。b2b0000:(1)(2)(3)(4)(5)(6)(7)(8)001:(2)(1)(4)(3)(6)(5)(8)(7)[字节交换]010:(3)(4)(1)(2)(7)(8)(5)(6)[半字交换]011:(4)(3)(2)(1)(8)(7)(6)(5)[半字字节交换]100:(5)(6)(7)(8)(1)(2)(3)(4)[字交换]101:(6)(5)(8)(7)(2)(1)(4)(3)[字字节交换]110:(7)(8)(5)(6)(3)(4)(1)(2)[字半字交换]111:(8)(7)(6)(5)(4)(3)(2)(1)[字半字字节交换]。	R/W*1
b3	—	Reserved	该位读取为0。写入值应为0。	R/W
b4	DOUTLC	停止输出图像数据线的计数模式	0：关闭计数模式，停止输出图像数据线1：打开计数模式，停止输出图像数据线。	R/W*1
b5	DOUTRCMD	输出图像数据线 恢复命令	将此位设置为1以恢复图像数据的写入。 该位仅在停止输出图像数据线的计数模式打开时有效。该位始终读为0。	W*1
b6	DOUTRINI	恢复输出图像时的地址初始化 数据线	该位仅在停止输出图像数据线的计数模式打开时有效。在将1写入数据线恢复命令位之前设置该位。0：重新开始输出图像数据线时不初始化传输地址1：重新开始输出图像数据线时初始化传输地址。	R/W*1
b7	—	Reserved	该位读取为0。写入值应为0。	R/W
b10 to b8	JINSWAP[2:0]	Byte/Halfword/Word Swap	在解压缩中交换输入编码数据。b10b8000:(1)(2)(3)(4)(5)(6)(7)(8)001:(2)(1)(4)(3)(6)(5)(8)(7)[字节交换]010:(3)(4)(1)(2)(7)(8)(5)(6)[半字交换]011:(4)(3)(2)(1)(8)(7)(6)(5)[半字字节交换]100:(5)(6)(7)(8)(1)(2)(3)(4)[字交换]101:(6)(5)(8)(7)(2)(1)(4)(3)[字字节交换]110:(7)(8)(5)(6)(3)(4)(1)(2)[字半字交换]111:(8)(7)(6)(5)(4)(3)(2)(1)[字半字字节交换]。	R/W*1
b11	—	Reserved	该位读取为0。写入值应为0。	R/W
b12	JINC	计数模式设置 停止输入编码数据	0：关闭计数模式，停止输入编码数据1：打开计数模式，停止输入编码数据。	R/W*1
b13	JINRCMD	输入编码数据简历 Command	将此位设置为1以恢复读取输入编码数据。 该位仅在停止输入编码数据的计数模式打开时有效。该位始终读为0。	W*1

Bit	Symbol	Bit name	Description	R/W
b14	JINRINI	Address Initialization When Input Coded Data is Resumed	This bit is only valid when the count mode for stopping input of coded data is on. Set this bit before writing 1 to the data resume command bit. 0: Do not initialize transfer address when input of coded data restarts 1: Initialize transfer address when input of coded data restarts.	R/W*1
b23 to b15	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b25, b24	OPF[1:0]	Specifies Output Image Data Pixel Format*2	b25 b24 0 0: Setting prohibited 0 1: ARGB8888 1 0: RGB565 1 1: Setting prohibited.	R/W*1
b27, b26	HINTER[1:0]	Horizontal Subsampling	Subsamples horizontal output image data. b27 b26 0 0: No subsampling 0 1: Subsample output data into 1/2 1 0: Subsample output data into 1/4 1 1: Subsample output data into 1/8.	R/W*1
b29, b28	VINTER[1:0]	Vertical Subsampling	Subsamples vertical output image data. b29 b28 0 0: No subsampling 0 1: Subsample output data into 1/2 1 0: Subsample output data into 1/4 1 1: Subsample output data into 1/8.	R/W*1
b31 to b30	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. In compression mode, these bits are invalid.
Note 2. Operation with the initial value is prohibited. Set these bits to 01b or 10b before starting operation.

57.2.24 JPEG Interface Decompression Source Address Register (JIFDSA)

Address(es): JPEG.JIFDSA 400E 605Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	DSA[31:16]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	DSA[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	DSA[2:0]	Input Coded Data Source Address	The lower three bits should be set to 0. These bits are read as 0.	R/W*2
b31 to b3	DSA[31:3]		Input coded data source address in 8-byte units.	R/W*2

Note 1. This register must be set in 8-byte units.
Note 2. In compression mode, these bits are invalid.

Bit	Symbol	位名称	Description	R/W
b14	JINRINI	地址初始化时间 输入编码数据是 Resumed	该位仅在停止输入编码数据的计数模式打开时有效。在将1写入数据恢复命令位之前设置该位。0：重新输入编码数据时不初始化传输地址1：重新输入编码数据时初始化传输地址。	R/W*1
b23 to b15	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b25, b24	OPF[1:0]	指定输出图像 数据像素格式*2	b25b2400：禁止设置01 ：ARGB888810：RGB5 6511：禁止设置。	R/W*1
b27, b26	HINTER[1:0]	Horizontal Subsampling	对水平输出图像数据进行二次采样。b27b 2600：无二次采样01：二次采样输出数据 到1210：二次采样输出数据到1411：二 次采样输出数据到18。	R/W*1
b29, b28	VINTER[1:0]	Vertical Subsampling	对垂直输出图像数据进行二次采样。b2 9b2800：无二次采样01：二次采样输 出数据到1210：二次采样输出数据到1 411：二次采样输出数据到18。	R/W*1
b31 to b30	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 在压缩模式下，这些位无效。
Note 2. 禁止以初始值操作。在开始操作之前将这些位设置为01b或10b。

57.2.24 JPEG接口解压源地址寄存器(JIFDSA)

Address(es): JPEG.JIFDSA 400E 605Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	DSA[31:16]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	DSA[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b2 to b0	DSA[2:0]	输入编码数据源 Address	低三位应设置为0。这些位被读取为0。	R/W*2
b31 to b3	DSA[31:3]		以8字节为单位输入编码数据源地址。	R/W*2

Note 1. 该寄存器必须以8字节为单位进行设置。
Note 2. 在压缩模式下，这些位无效。

57.2.25 JPEG Interface Decompression Line Offset Register (JIFDDOFST)

Address(es): JPEG.JIFDDOFST 400E 6060h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	DDMW[14:0]														
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	DDMW[2:0]	Output Image Data Lines Offset	The lower three bits should be set to 0. These bits are read as 0.	R/W*2
b14 to b3	DDMW[14:3]		Output image data lines offset in 8-byte units.	R/W*2
b31 to b15	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. This register must be set in 8-byte units.
Note 2. In compression mode, these bits are invalid.

57.2.26 JPEG Interface Decompression Destination Address Register (JIFDDA)

Address(es): JPEG.JIFDDA 400E 6064h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	DDA[31:16]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	DDA[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	DDA[2:0]	Output Image Data Destination Address	The lower three bits should be set to 0. These bits are read as 0.	R/W*2
b31 to b3	DDA[31:3]		Output image data destination address in 8-byte units.	R/W*2

Note 1. This register must be set in 8-byte units.
Note 2. In compression mode, these bits are invalid.

57.2.25 JPEG接口解压缩行偏移寄存器(JIDFDOFST)

Address(es): JPEG.JIFDDOFST 400E 6060h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	DDMW[14:0]														
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b2 to b0	DDMW[2:0]	输出图像数据线偏移	低三位应设置为0。这些位被读取为0。	R/W*2
b14 to b3	DDMW[14:3]		输出图像数据行以8字节为单位偏移。	R/W*2
b31 to b15	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 该寄存器必须以8字节为单位进行设置。
Note 2. 在压缩模式下，这些位无效。

57.2.26 JPEG接口解压目标地址寄存器(JIFDDA)

Address(es): JPEG.JIFDDA 400E 6064h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	DDA[31:16]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	DDA[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b2 to b0	DDA[2:0]	输出图像数据目的地Address	低三位应设置为0。这些位被读取为0。	R/W*2
b31 to b3	DDA[31:3]		以8字节为单位输出图像数据目标地址。	R/W*2

Note 1. 该寄存器必须以8字节为单位进行设置。
Note 2. 在压缩模式下，这些位无效。

57.2.27 JPEG Interface Decompression Source Data Count Register (JIFDSDC)

Address(es): JPEG.JIFDSDC 400E 6068h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	JDATAS[15:0]															
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	JDATAS[2:0]	Amount of Input Coded Data to Be Read	The lower three bits should be set to 0. These bits are read as 0.	R/W*2
b15 to b3	JDATAS[15:3]		Amount of input coded data to be read, in 8-byte units.	R/W*2
b18 to b16	—	Reserved	These bits are read as undefined. The write value should be 0.	R/W
b31 to b19	—	Reserved	These bits are read as undefined. The write value should be 1.	R

Note 1. This register must be set in 8-byte units.
Note 2. In compression mode, these bits are invalid.

57.2.28 JPEG Interface Decompression Destination Line Count Register (JIFDDLC)

Address(es): JPEG.JIFDDLC 400E 606Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	LINES[15:0]															
Value after reset:	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	LINES[2:0]	Number of Output Image Data Lines to Be Written	The lower three bits should be set to 0. These bits are read as 0.	R/W*2
b15 to b3	LINES[15:3]		Specifies number of lines of output image data to be written. Set the value so that the output image data line count matches the MCU unit. For YCbCr444, YCbCr422, and YCbCr411 output, the setting value × 1 is equal to the output image data line count. For YCbCr420 output, the setting value × 2 is equal to the output image data line count.	R/W*2
b18 to b16	—	Reserved	These bits are read as undefined. The write value should be 0.	R/W
b31 to b19	—	Reserved	These bits are read as undefined. The write value should be 1.	R

Note 1. Set this register so that the output image data line count matches the MCU unit.
Note 2. In compression mode, these bits are invalid.

57.2.27 JPEG接口解压缩源数据计数寄存器(JIFDSDC)

Address(es): JPEG.JIFDSDC 400E 6068h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	JDATAS[15:0]															
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0

Bit	Symbol	位名称	Description	R/W
b2 to b0	JDATAS[2:0]	要读取的输入编码数据量	低三位应设置为0。这些位被读取为0。	R/W*2
b15 to b3	JDATAS[15:3]		要读取的输入编码数据量，以8字节为单位。	R/W*2
b18 to b16	—	Reserved	这些位被读取为未定义。写入值应为0。	R/W
b31 to b19	—	Reserved	这些位被读取为未定义。写入值应为1。	R

Note 1. 该寄存器必须以8字节为单位进行设置。
Note 2. 在压缩模式下，这些位无效。

57.2.28 JPEG接口解压缩目标行计数寄存器(JIFDDLC)

Address(es): JPEG.JIFDDLC 400E 606Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	LINES[15:0]															
重置后的值：	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0

Bit	Symbol	位名称	Description	R/W
b2 to b0	LINES[2:0]	要写入的输出图像数据行数	低三位应设置为0。这些位被读取为0。	R/W*2
b15 to b3	LINES[15:3]		指定要写入的输出图像数据的行数。设置该值以使输出图像数据行数与MCU单元匹配。 对于YCbCr444、YCbCr422和YCbCr411输出，设置值×1等于输出图像数据行数。对于YCbCr420输出，设置值×2等于输出图像数据行数。	R/W*2
b18 to b16	—	Reserved	这些位被读取为未定义。写入值应为0。	R/W
b31 to b19	—	Reserved	这些位被读取为未定义。写入值应为1。	R

Note 1. 设置该寄存器，使输出图像数据行数与MCU单元匹配。
Note 2. 在压缩模式下，这些位无效。

57.2.29 JPEG Interface Decompression alpha Set Register (JIFDADT)

Address(es): JPEG.JIFDADT 400E 6070h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	ALPHA[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	ALPHA[7:0]	Alpha Value for Adding to ARGB8888 Format	Alpha value setting for output in ARGB8888 format.	R/W*1
b31 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. In compression mode, these bits are invalid.

57.2.30 JPEG Interrupt Enable Register 1 (JINTE1)

Address(es): JPEG.JINTE1 400E 608Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	CBTEN	DINLEN	—	—	DBTEN	JINEN	DOUTLEN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	DOUTLEN	Interrupt Request Bit DOUTLF Enable Control	Enables or disables a data transfer processing interrupt request (JPEG_JDTI) when the DOUTLF bit in JINTS1 sets to 1. 0: Disable interrupt request 1: Enable interrupt request.	R/W*1
b1	JINEN	Interrupt Request Bit JINF Enable Control	Enables or disables a data transfer processing interrupt request (JPEG_JDTI) when the JINF bit in JINTS1 sets to 1. 0: Disable interrupt request 1: Enable interrupt request.	R/W*1
b2	DBTEN	Interrupt Request Bit DBTF Enable Control	Enables or disables a data transfer processing interrupt request (JPEG_JDTI) when the DBTF bit in JINTS1 sets to 1. 0: Disable interrupt request 1: Enable interrupt request.	R/W*1
b4, b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b5	DINLEN	Interrupt Request Bit DINLF Enable Control	Enables or disables a data transfer processing interrupt request (JPEG_JDTI) when the DINLF bit in JINTS1 sets to 1. 0: Disable interrupt request 1: Enable interrupt request.	R/W*2

57.2.29 JPEG接口解压alpha设置寄存器(JIFDADT)

Address(es): JPEG.JIFDADT 400E 6070h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	ALPHA[7:0]							
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b7 to b0	ALPHA[7:0]	添加到的Alpha值 ARGB8888 Format	ARGB8888格式输出的Alpha值设置。	R/W*1
b31 to b8	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 在压缩模式下，这些位无效。

57.2.30 JPEG中断使能寄存器1(JINTE1)

Address(es): JPEG.JINTE1 400E 608Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	CBTEN	DINLEN	—	—	DBTEN	JINEN	DOUTLEN
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	DOUTLEN	中断请求位DOUTLF 启用控制	当JINTS1中的DOUTLF位设置为1时，启用或禁用数据传输处理中断请求(JPEG_JDTI)。0：禁用中断请求1：启用中断请求。	R/W*1
b1	JINEN	中断请求位JINF 启用控制	当JINTS1中的JINF位设置为1时，启用或禁用数据传输处理中断请求(JPEG_JDTI)。0：禁用中断请求1：启用中断请求。	R/W*1
b2	DBTEN	中断请求位DBTF 启用控制	当JINTS1中的DBTF位设置为1时，启用或禁用数据传输处理中断请求(JPEG_JDTI)。0：禁用中断请求1：启用中断请求。	R/W*1
b4, b3	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b5	DINLEN	中断请求位DINLF 启用控制	当JINTS1中的DINLF位设置为1时，启用或禁用数据传输处理中断请求(JPEG_JDTI)。0：禁用中断请求1：启用中断请求。	R/W*2

Bit	Symbol	Bit name	Description	R/W
b6	CBTEN	Interrupt Request Bit CBTF Enable Control	Enables or disables a data transfer processing interrupt request (JPEG_JDTI) when the CBTF bit in JINTS1 sets to 1. 0: Disable interrupt request 1: Enable interrupt request.	R/W*2
b31 to b7	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. In compression mode, these bits are invalid.
Note 2. In decompression mode, these bits are invalid.

57.2.31 JPEG Interrupt Status Register 1 (JINTS1)

Address(es): JPEG.JINTS1 400E 6090h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	CBTF	DINLF	—	—	DBTF	JINF	DOUTLF
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	DOUTLF	Request for Decompressed Data Output Line Finish	In decompression, this bit sets to 1 when the number of lines of output image data indicated in JIFDDLC is written. This bit is only valid when the DOUTLC bit in JIFDCNT is set to 1.	R/W*1,*2,*3
b1	JINF	Request for JPEG Input Finish	This bit sets to 1 when the amount of input coded data indicated in JIFDSDC is read in decompression. This bit is only valid when the JINC bit in JIFDCNT is set to 1.	R/W*1,*2,*3
b2	DBTF	Request for Decompressed Data Bottom Finish	This bit sets to 1 when the last output image data is written in decompression.	R/W*1,*2,*3
b4, b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b5	DINLF	Request for Data Input Line Finish	This bit sets to 1 when the number of input image data lines indicated in JIFESLC is read in compression. This bit is only valid when the DINLC bit in JIFECNT is set to 1.	R/W*1,*2,*4
b6	CBTF	Request for Compressed Data Bottom Finish	This bit sets to 1 when the last output coded data is written in compression.	R/W*1,*2,*4
b31 to b7	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Clear the interrupt sources of this register by writing 0s to this register.
Note 2. When the bit is read as 1, write 0 to clear it. When the bit is read as 0, write 1 to set it.
Note 3. In compression mode, these bits are invalid.
Note 4. In decompression mode, these bits are invalid.

57.3 Operation

57.3.1 Compression

This section describes the compression process flows.

(1) Processing overview

The compression process overview is as follows:

1. The JPEG core is activated. A marker is output, after which, image data can be input. Approximately 30,000 cycles are required (for generating the SOI to SOS markers).

Bit	Symbol	位名称	Description	R/W
b6	CBTEN	中断请求位CBTF 启用控制	当JINTS1中的CBTF位设置为1时，启用或禁用数据传输处理中断请求(JPEG_JDTI)。0：禁用中断请求1：启用中断请求。	R/W*2
b31 to b7	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 在压缩模式下，这些位无效。
Note 2. 在解压模式下，这些位无效。

57.2.31 JPEG中断状态寄存器1(JINTS1)

Address(es): JPEG.JINTS1 400E 6090h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	CBTF	DINLF	—	—	DBTF	JINF	DOUTLF
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	DOUTLF	解压请求 数据输出线完成	在解压缩中，当写入JIFDDLC中指示的输出图像数据的行数时，该位设置为1。该位仅在JIFDCNT中的DOUTLC位设置为1时有效。	R/W*1,*2,*3
b1	JINF	请求JPEG输入 Finish	当在解压缩中读取JIFDSDC中指示的输入编码数据量时，该位设置为1。该位仅在JIFDCNT中的JINC位设置为1时有效。	R/W*1,*2,*3
b2	DBTF	解压请求 数据底部完成	当最后一个输出图像数据以解压缩方式写入时，该位设置为1。	R/W*1,*2,*3
b4, b3	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b5	DINLF	数据输入线请求 Finish	当在压缩中读取JIFESLC中指示的输入图像数据行数时，该位设置为1。该位仅在JIFECNT中的DINLC位设置为1时有效。	R/W*1,*2,*4
b6	CBTF	压缩请求 数据底部完成	当最后一个输出编码数据以压缩方式写入时，该位设置为1。	R/W*1,*2,*4
b31 to b7	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 通过向该寄存器写入0来清除该寄存器的中断源。
Note 2. 当该位读取为1时，写入0将其清除。当该位被读取为0时，写入1来设置它。
Note 3. 在压缩模式下，这些位无效。
Note 4. 在解压模式下，这些位无效。

57.3 Operation

57.3.1 Compression

本节介绍压缩处理流程。

(1) 处理概述

压缩过程概述如下：

1. JPEG核心被激活。输出标记后，可以输入图像数据。大约需要30 000个周期（用于生成SOI到SOS标记）。

2. Image data is transferred in MCUs from the external buffer to the JPEG Codec.
   - If the count mode for stopping the input of image data lines is on, reading stops each time the number of lines set in JIFESLC is read. To resume reading, set the DINRCMD bit in JIFECNT to 1.
   - When the DINRINI bit in JIFECNT is 0, the addresses for reading on resumption are continued from the addresses in the previous round of transfer.
   - When the DINRINI bit is 1, the address set in JIFESA is used on resumption.
   - Reading is also stopped when one frame of image data is completely transferred.
   - If the count mode for stopping the input of image data lines is off, reading continues until one frame of image data is completely transferred.
3. Image data is input to the JPEG core. The input data is processed in MCUs at any time in the JPEG core.
4. Coded data is transferred from the JPEG Codec to the external buffer.
5. Compression is complete after one frame of data is processed completely.

(2) Compression flow

(a) Initial settings

To set the initial settings for compression:

After completing the JPEG core settings and input/output buffer settings and transferring image data to the external buffer, activate the JPEG Codec by setting the JSRT bit in JCCMD to 1. After the JPEG Codec is activated, the JPEG markers (SOI to SOS) are generated and output. Generating the markers takes approximately 30,000 cycles.

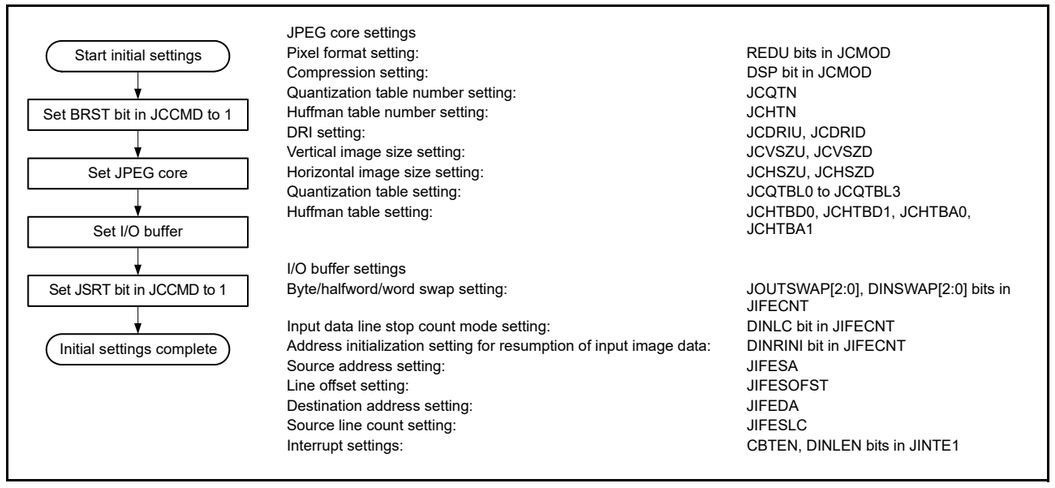


Figure 57.2 Flow of compression initial settings

(b) Compression process

The compression process flow is as follows:

1. When JPEG compression process is completed, the INS6 bit in JINTS0 sets to 1. However, the JPEG Codec continues processing, because the coded data remains to be transferred. The CBTF bit in JINTS1 sets to 1 when the last coded data is transferred. The interrupt source is cleared by a 0 write to the INS6 bit. However, the interrupt request asserted by this interrupt source cannot be cleared by a 0 write to the INS6 bit. Set an interrupt request clear command (by setting the JEND bit in JCCMD to 1) to clear the interrupt request.
2. When the JPEG Codec has completed compression and all coded data is transferred, the CBTF flag in JINTS1 sets to 1. When the CBTEN bit in JINTE1 is 1 here, an interrupt is generated. The interrupt source is cleared by a 0 write to the CBTF flag.

2. 图像数据在MCU中从外部缓冲区传输到JPEG编解码器。
   - 如果停止输入图像数据线的计数模式打开，则每次读取JIFESLC中设置的线数时停止读取。要恢复读取，请将JIFECNT中的DINRCMD位设置为1。
   - 当JIFECNT的DINRINI位为0时，恢复读取的地址从上一轮传输的地址继续。
   - 当DINRINI位为1时，在恢复时使用JIFESA中设置的地址。
   - 当一帧图像数据完全传输时，读取也会停止。
   - 如果停止输入图像数据线的计数模式关闭，则继续读取直到一帧图像数据传输完毕。
3. 图像数据被输入到JPEG核心。输入数据在JPEG内核中随时在MCU中处理。
4. 编码数据从JPEG编解码器传输到外部缓冲区。
5. 完成一帧数据处理后，即完成压缩。

(2) 压缩流量

(a) 初始设置

要设置压缩的初始设置：

完成JPEG核心设置和输入输出缓冲区设置并将图像数据传输到外部缓冲区后，通过将JCCMD中的JSRT位设置为1来激活JPEG编解码器。激活JPEG编解码器后，JPEG标记（SOI到SOS）为生成并输出。生成标记大约需要30 000个循环。

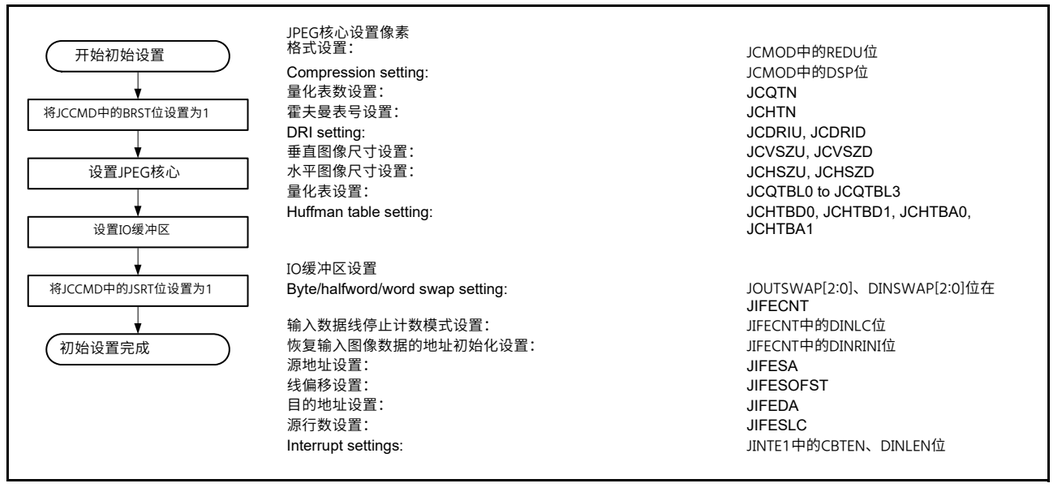


Figure 57.2 压缩初始设定流程

(b) 压缩过程

压缩处理流程如下：

1. 当JPEG压缩过程完成时，JINTS0中的INS6位设置为1。但是，JPEG编解码器继续处理，因为编码数据仍有待传输。当传输最后一个编码数据时，JINTS1中的CBTF位设置为1。向INS6位写入0可清除中断源。但是，此中断源发出的中断请求不能通过向INS6位写入0来清除。设置中断请求清除命令（通过将JCCMD中的JEND位设置为1）来清除中断请求。
2. 当JPEGCodec完成压缩并传输所有编码数据时，JINTS1中的CBTF标志设置为1。当此处JINTE1中的CBTEN位为1时，产生中断。将0写入CBTF标志清除中断源。

3. If the count mode for stopping image data lines is on, when the specified number of image data lines set in JIFESLC is read, the DINLF flag in JINTS1 sets to 1, and reading stops. When the DINLEN bit in JINTE1 is 1 here, an interrupt is generated. An interrupt source is cleared by a 0 write to the DINLEN bit. Setting the DINRCMD bit in JIFECNT to 1 resumes reading.
   - When the DINRINI bit in JIFECNT is 0, the addresses for reading on resumption are continued from the addresses in the previous round of transfer.
   - When the DINRINI bit is 1, the address set in JIFESA is used on resumption.

(c) Data correction

After the output coded data is divided by 8, if the remainder is 1 to 6 bytes, transfer of bytes 1 to 6 of the remainder might not complete successfully. If the transfer is unsuccessful, bytes 1 to 6 of the remainder are written to the address specified in the JPEG interface compression destination address register (JIFEDA), overwriting the existing data.*1

For this reason, it is necessary to check whether the output coded data was transferred successfully and, if not, to perform data correction.

Note 1. The JPEG Codec handles the output of coded data in 16-bit units. For this reason, if the coded data has an odd code length, the final code output is D9FFh. (FFh is appended.) When the remainder is 1, 3, or 5 bytes, the remainder data (1, 3, or 5 bytes) + FFh is written to the address specified in JIFEDA, overwriting the existing data.

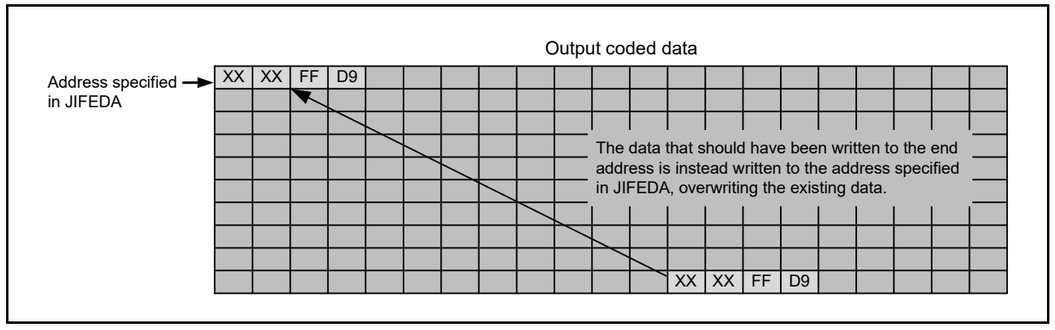


Figure 57.3 Conceptual diagram of abnormal transfer of output coded data

3. 如果停止图像数据线的计数模式打开，当读取JIFESLC中设置的指定数量的图像数据线时，JINTS1中的DINLF标志设置为1，并且读取停止。这里当JINTE1的DINLEN位为1时，产生中断。向DINLEN位写入0可清除中断源。将JIFECNT中的DINRCMD位设置为1可恢复读取。
   - 当JIFECNT的DINRINI位为0时，恢复读取的地址从上一轮传输的地址继续。
   - 当DINRINI位为1时，在恢复时使用JIFESA中设置的地址。

(c) 数据修正

输出编码数据除以8后，如果余数为1到6个字节，则余数的1到6字节的传输可能无法成功完成。如果传输不成功，则将剩余的字节1到6写入JPEG接口压缩目标地址寄存器(JIFEDA)中指定的地址，覆盖现有数据。*1

为此，有必要检查输出的编码数据是否传输成功，如果没有，则进行数据校正。

注1JPEG编解码器以16位为单位处理编码数据的输出。因此，如果编码数据的码长为奇数，则最终码输出为D9FFh。（附加FFh。）当余数为1、3或5字节时，将余数数据（1、3或5字节）+FFh写入JIFEDA中指定的地址，覆盖现有数据。

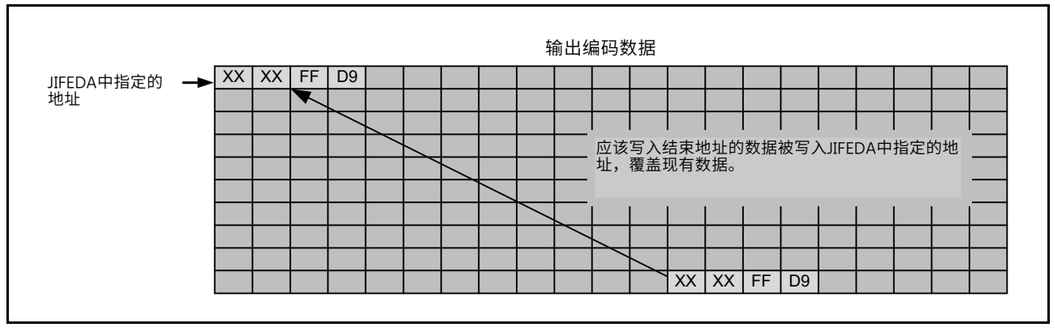


Figure 57.3 输出编码数据异常传输示意图

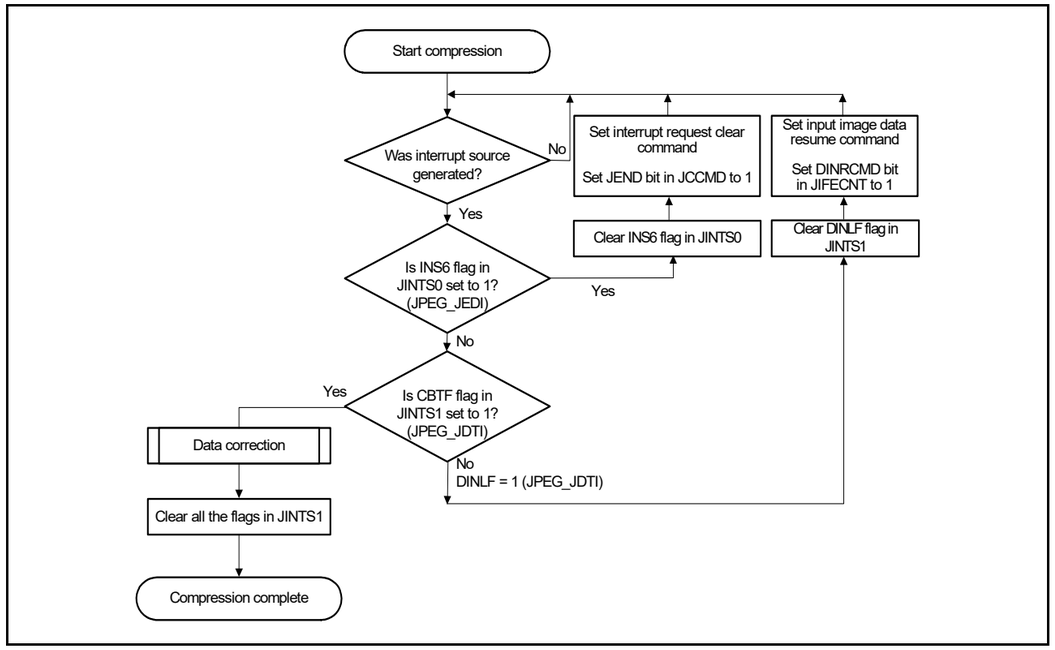


Figure 57.4 Compression process flow

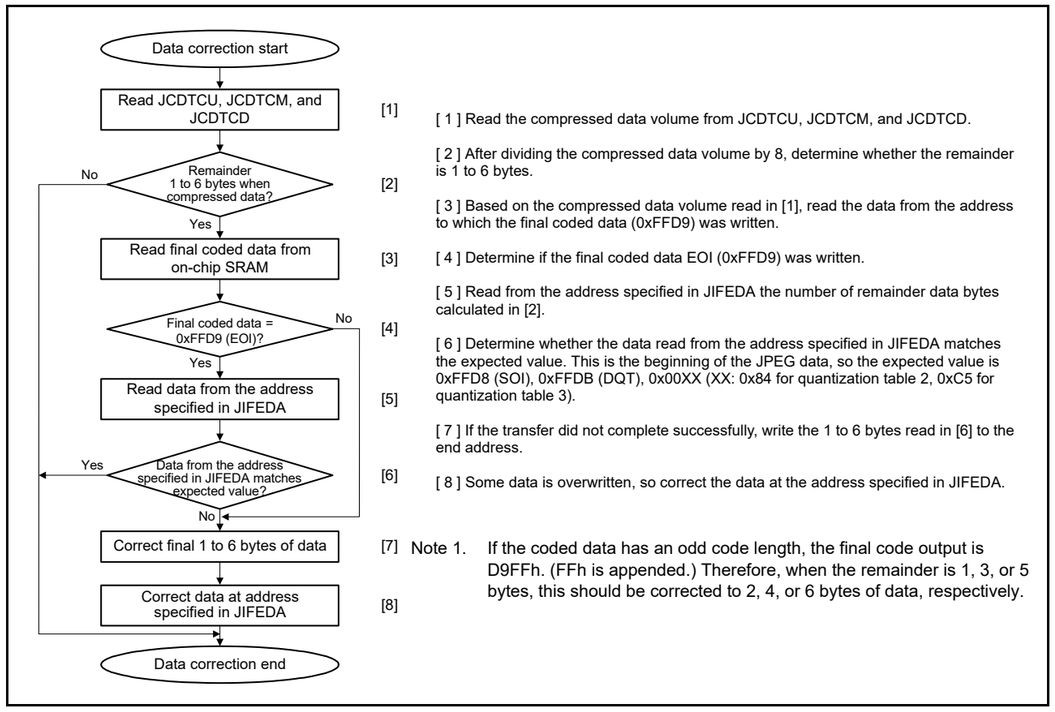


Figure 57.5 Data correction flow

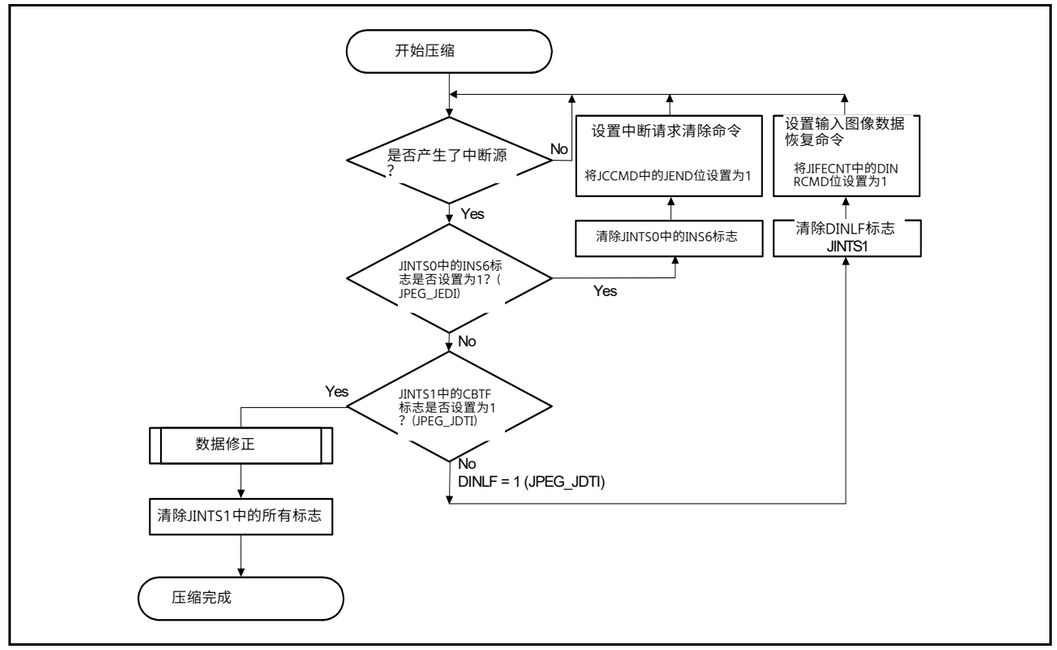


Figure 57.4 压缩工艺流程

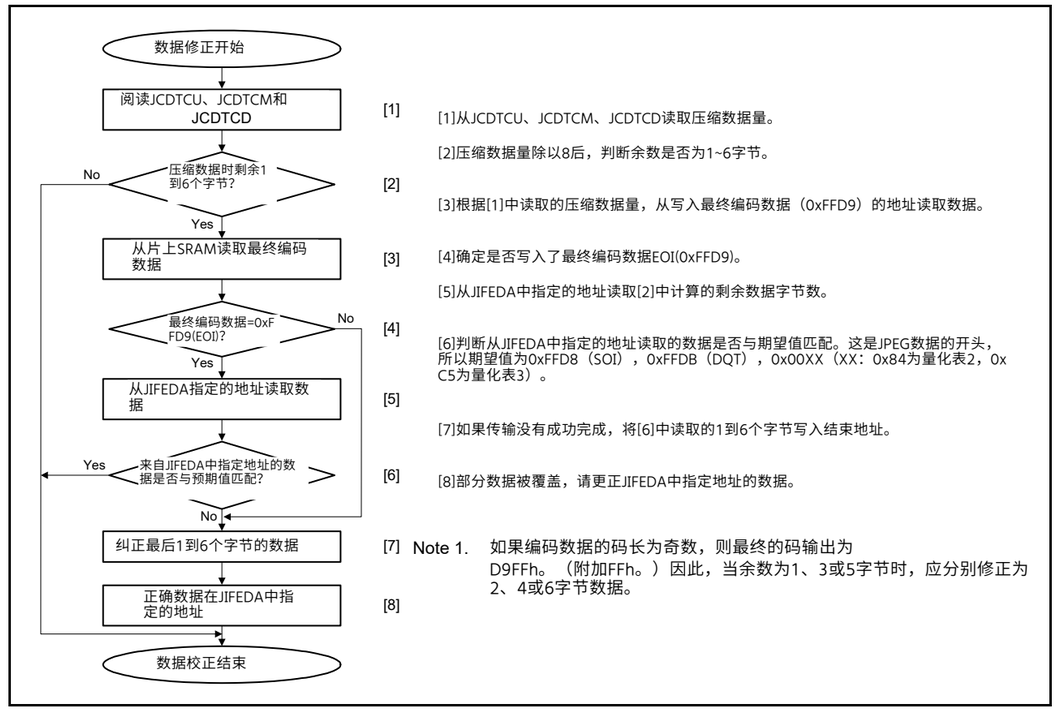


Figure 57.5 数据校正流程

(3) JPEG coded data format

Figure 57.6 shows the data output stream in compression. The amount of coded data from SOI to EOI is indicated in JCDTCU, JCDTCM, and JCDTCD. When both JCDRIU and JCDRID are set to 0000_0000h, the following markers are not output:

- DRI marker
- RST marker (in compressed image data).

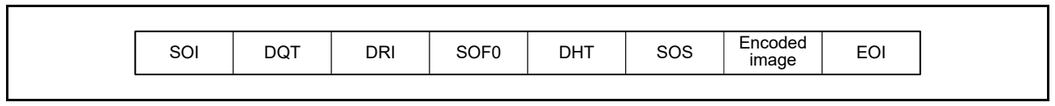


Figure 57.6 JPEG coded data format

- DQT: Not output for unused table
- DHT: Output in the order DC0, AC0, DC1, and AC1. Not output for unused tables
- SOF0: Component identifiers are C1 = first color component, C2 = second color component, and C3 = third color component
- SOS: Scan component selectors are CS1 = first color component, CS2 = second color component, and CS3 = third color component.

Header volume (reference)

- SOI: 2 bytes (FFD8)
- DQT: 134 bytes when two quantization tables are used, 199 bytes when three quantization tables are used (±65 bytes/table increase or decrease)
- DRI: 6 bytes
- SOF0: 19 bytes (4:2:2)
- DHT: 420 bytes (two tables are used)
- SOS: 14 bytes (4:2:2)
- EOI: 2 bytes (FFD9).

(4) Table setting

(a) Quantization table specification

The order of addresses shown in 8 × 8 blocks corresponds to that of the register addresses. Do not access this table while the JPEG Codec is processing.

Table 57.2 Quantization table

00	01	02	03	04	05	06	07
08	09	0A	0B	0C	0D	0E	0F
10	11	12	13	14	15	16	17
18	19	1A	1B	1C	1D	1E	1F
20	21	22	23	24	25	26	27
28	29	2A	2B	2C	2D	2E	2F
30	31	32	33	34	35	36	37
38	39	3A	3B	3C	3D	3E	3F

JCQTBL0 (400E 6100h) = 00h
JCQTBL0 (400E 6101h) = 01h
JCQTBL0 (400E 6102h) = 02h

(3) JPEG编码数据格式

图57.6显示了压缩后的数据输出流。从SOI到EOI的编码数据量在JCDTCU、JCDTCM和JCDTCD。当JCDRIU和JCDRID都设置为0000_0000h时，不输出以下标记：

- DRI标记
- RST标记（在压缩图像数据中）。

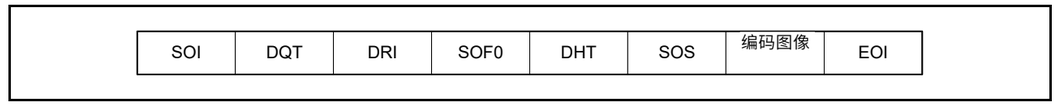


Figure 57.6 JPEG编码数据格式

- DQT：未使用的表不输出
- DHT：按DC0、AC0、DC1和AC1的顺序输出。未使用的表不输出
- SOF0：分量标识符为C1=第一个颜色分量，C2=第二个颜色分量，C3=第三个颜色分量
- SOS：扫描分量选择器是CS1=第一个颜色分量、CS2=第二个颜色分量和CS3=第三个颜色分量。

标头卷（参考）

- SOI: 2 bytes (FFD8)
- DQT：使用两个量化表时134字节，使用三个量化表时199字节（±65字节表增加或减少）
- DRI: 6 bytes
- SOF0: 19 bytes (4:2:2)
- DHT：420字节（使用两个表）
- SOS: 14 bytes (4:2:2)
- EOI: 2 bytes (FFD9).

(4) 桌面设置

(a) 量化表规范

8×8块中显示的地址顺序对应于寄存器地址的顺序。当JPEG编解码器正在处理时，请勿访问此表。

Table 57.2 量化表

00	01	02	03	04	05	06	07
08	09	0A	0B	0C	0D	0E	0F
10	11	12	13	14	15	16	17
18	19	1A	1B	1C	1D	1E	1F
20	21	22	23	24	25	26	27
28	29	2A	2B	2C	2D	2E	2F
30	31	32	33	34	35	36	37
38	39	3A	3B	3C	3D	3E	3F

JCQTBL0 (400E 6100h) = 00h
JCQTBL0 (400E 6101h) = 01h
JCQTBL0 (400E 6102h) = 02h

JCQTBL0 (400E 6103h) = 03h
:
JCQTBL0 (400E 613Fh) = 3Fh
JCQTBL1 (400E 6140h) = 40h
JCQTBL1 (400E 6141h) = 41h
JCQTBL1 (400E 6142h) = 42h
JCQTBL1 (400E 6143h) = 43h
:
JCQTBL1 (400E 617Fh) = 7Fh
JCQTBL2 (400E 6180h) = 80h
JCQTBL2 (400E 6181h) = 81h
JCQTBL2 (400E 6182h) = 82h
JCQTBL2 (400E 6183h) = 83h
:
JCQTBL2 (400E 61BFh) = BFh
JCQTBL3 (400E 61C0h) = C0h
JCQTBL3 (400E 61C1h) = C1h
JCQTBL3 (400E 61C2h) = C2h
JCQTBL3 (400E 61C3h) = C3h
:
JCQTBL3 (400E 61FFh) = FFh

(b) Huffman table specification

This section provides examples of the Huffman table specification given in the ITU-T T81 Annex K.3.3 recommended by JPEG. In compression, the following settings must be specified for all the codes so that Huffman codes can be generated for all the group numbers.

- DC Huffman table: The number of codes for each code length is 12, and the group numbers in the order of frequency of occurrence are 12.
- AC Huffman table: The number of codes for each code length is 162, and the zero run length/group numbers in the order of frequency of occurrence are 162.

Do not access the following tables while the JPEG Codec is processing. In particular, read access is prohibited.

- Table K.3/T81

  JCHTBD0 (400E 6200h) = 00h
  JCHTBD0 (400E 6201h) = 01h
  JCHTBD0 (400E 6202h) = 05h
  JCHTBD0 (400E 6203h) = 01h
  :
  JCHTBD0 (400E 621Bh) = 0Bh

- Table K.4/T81

  JCHTBD1 (400E 6300h) = 00h
  JCHTBD1 (400E 6301h) = 03h
  JCHTBD1 (400E 6302h) = 01h
  JCHTBD1 (400E 6303h) = 01h
  :
  JCHTBD1 (400E 631Bh) = 0Bh

- Table K.5/T81

  JCHTBA0 (400E 6220h) = 00h

JCQTBL0 (400E 6103h) = 03h
:
JCQTBL0 (400E 613Fh) = 3Fh
JCQTBL1 (400E 6140h) = 40h
JCQTBL1 (400E 6141h) = 41h
JCQTBL1 (400E 6142h) = 42h
JCQTBL1 (400E 6143h) = 43h
:
JCQTBL1 (400E 617Fh) = 7Fh
JCQTBL2 (400E 6180h) = 80h
JCQTBL2 (400E 6181h) = 81h
JCQTBL2 (400E 6182h) = 82h
JCQTBL2 (400E 6183h) = 83h
:
JCQTBL2 (400E 61BFh) = BFh
JCQTBL3 (400E 61C0h) = C0h
JCQTBL3 (400E 61C1h) = C1h
JCQTBL3 (400E 61C2h) = C2h
JCQTBL3 (400E 61C3h) = C3h
:
JCQTBL3 (400E 61FFh) = FFh

(b) 霍夫曼表规范

本节提供了JPEG推荐的ITU-TT81附件K.3.3中给出的霍夫曼表规范的示例。在压缩中，必须为所有代码指定以下设置，以便可以为所有组号生成霍夫曼代码。

- DCHuffman表：每个码长的码数为12，按出现频率排序的组号为12。
- ACHuffman表：每个码长的码数为162，零游程组数按出现频率排序为162。

当JPEG编解码器正在处理时，请勿访问下表。特别是，禁止读取访问。

- Table K.3/T81

  JCHTBD0 (400E 6200h) = 00h
  JCHTBD0 (400E 6201h) = 01h
  JCHTBD0 (400E 6202h) = 05h
  JCHTBD0 (400E 6203h) = 01h
  :
  JCHTBD0 (400E 621Bh) = 0Bh

- Table K.4/T81

  JCHTBD1 (400E 6300h) = 00h
  JCHTBD1 (400E 6301h) = 03h
  JCHTBD1 (400E 6302h) = 01h
  JCHTBD1 (400E 6303h) = 01h
  :
  JCHTBD1 (400E 631Bh) = 0Bh

- Table K.5/T81

  JCHTBA0 (400E 6220h) = 00h

JCHTBA0 (400E 6221h) = 02h
JCHTBA0 (400E 6222h) = 01h
JCHTBA0 (400E 6223h) = 03h
:
JCHTBA0 (400E 62D1h) = FAh

- Table K.6/T81

JCHTBA1 (400E 6320h) = 00h
JCHTBA1 (400E 6321h) = 02h
JCHTBA1 (400E 6322h) = 01h
JCHTBA1 (400E 6323h) = 02h
:
JCHTBA1 (400E 63D1h) = FAh

(5) Input pixel format

Image data in the YCbCr422 format can be input to the JPEG Codec. Allocation of data in the YCbCr422 format can be changed by the DINSWAP[2:0] bits in JIFECNT as shown in the following diagrams.

- When the DINSWAP[2:0] bits = 000b

b63 b56	b55 b48	b47 b40	b39 b32	b31 b24	b23 b16	b15 b8	b7 b0
Y0 8 bits	Cb0 8 bits	Y1 8 bits	Cr0 8 bits	Y2 8 bits	Cb1 8 bits	Y3 8 bits	Cr1 8 bits

- When the DINSWAP[2:0] bits = 001b

b63 b56	b55 b48	b47 b40	b39 b32	b31 b24	b23 b16	b15 b8	b7 b0
Cb0 8 bits	Y0 8 bits	Cr0 8 bits	Y1 8 bits	Cb1 8 bits	Y2 8 bits	Cr1 8 bits	Y3 8 bits

- When the DINSWAP[2:0] bits = 010b

b63 b56	b55 b48	b47 b40	b39 b32	b31 b24	b23 b16	b15 b8	b7 b0
Y1 8 bits	Cr0 8 bits	Y0 8 bits	Cb0 8 bits	Y3 8 bits	Cr1 8 bits	Y2 8 bits	Cb1 8 bits

- When the DINSWAP[2:0] bits = 100b

b63 b56	b55 b48	b47 b40	b39 b32	b31 b24	b23 b16	b15 b8	b7 b0
Y2 8 bits	Cb1 8 bits	Y3 8 bits	Cr1 8 bits	Y0 8 bits	Cb0 8 bits	Y1 8 bits	Cr0 8 bits

- When the DINSWAP[2:0] bits = 101b

b63 b56	b55 b48	b47 b40	b39 b32	b31 b24	b23 b16	b15 b8	b7 b0
Cb1 8 bits	Y2 8 bits	Cr1 8 bits	Y3 8 bits	Cb0 8 bits	Y0 8 bits	Cr0 8 bits	Y1 8 bits

- When the DINSWAP[2:0] bits = 110b

b63 b56	b55 b48	b47 b40	b39 b32	b31 b24	b23 b16	b15 b8	b7 b0
Y3 8 bits	Cr1 8 bits	Y2 8 bits	Cb1 8 bits	Y1 8 bits	Cr0 8 bits	Y0 8 bits	Cb0 8 bits

- When the DINSWAP[2:0] bits = 111b

b63 b56	b55 b48	b47 b40	b39 b32	b31 b24	b23 b16	b15 b8	b7 b0
Cr1 8 bits	Y3 8 bits	Cb1 8 bits	Y2 8 bits	Cr0 8 bits	Y1 8 bits	Cb0 8 bits	Y0 8 bits

(6) Output coded data

For compression, coded data is output. The JPEG Codec handles the output of coded data in 16-bit units. For this reason, if the coded data has an odd code length such as fractional, the final code for output is D9FFh.

The JOUTSWAP[2:0] bits in JIFECNT can be used to alter the arrangement of coded data in output.

57.3.2 Decompression

This section describes the decompression process flows.

JCHTBA0 (400E 6221h) = 02h
JCHTBA0 (400E 6222h) = 01h
JCHTBA0 (400E 6223h) = 03h
:
JCHTBA0 (400E 62D1h) = FAh

- Table K.6/T81

JCHTBA1 (400E 6320h) = 00h
JCHTBA1 (400E 6321h) = 02h
JCHTBA1 (400E 6322h) = 01h
JCHTBA1 (400E 6323h) = 02h
:
JCHTBA1 (400E 63D1h) = FAh

(5) 输入像素格式

YCbCr422格式的图像数据可以输入到JPEG编解码器。如下图所示，可以通过JIFECNT中的DINSWAP[2:0]位更改YCbCr422格式的数据分配。

- 当DINSWAP[2:0]位=000b

b63 b56	b55 b48	b47 b40	b39 b32	b31 b24	b23 b16	b15 b8	b7 b0
Y0 8 bits	Cb0 8 bits	Y1 8 bits	Cr0 8 bits	Y2 8 bits	Cb1 8 bits	Y3 8 bits	Cr1 8 bits

- 当DINSWAP[2:0]位=001b

b63 b56	b55 b48	b47 b40	b39 b32	b31 b24	b23 b16	b15 b8	b7 b0
Cb0 8 bits	Y0 8 bits	Cr0 8 bits	Y1 8 bits	Cb1 8 bits	Y2 8 bits	Cr1 8 bits	Y3 8 bits

- 当DINSWAP[2:0]位=010b

b63 b56	b55 b48	b47 b40	b39 b32	b31 b24	b23 b16	b15 b8	b7 b0
Y1 8 bits	Cr0 8 bits	Y0 8 bits	Cb0 8 bits	Y3 8 bits	Cr1 8 bits	Y2 8 bits	Cb1 8 bits

- 当DINSWAP[2:0]位=100b

b63 b56	b55 b48	b47 b40	b39 b32	b31 b24	b23 b16	b15 b8	b7 b0
Y2 8 bits	Cb1 8 bits	Y3 8 bits	Cr1 8 bits	Y0 8 bits	Cb0 8 bits	Y1 8 bits	Cr0 8 bits

- 当DINSWAP[2:0]位=101b

b63 b56	b55 b48	b47 b40	b39 b32	b31 b24	b23 b16	b15 b8	b7 b0
Cb1 8 bits	Y2 8 bits	Cr1 8 bits	Y3 8 bits	Cb0 8 bits	Y0 8 bits	Cr0 8 bits	Y1 8 bits

- 当DINSWAP[2:0]位=110b

b63 b56	b55 b48	b47 b40	b39 b32	b31 b24	b23 b16	b15 b8	b7 b0
Y3 8 bits	Cr1 8 bits	Y2 8 bits	Cb1 8 bits	Y1 8 bits	Cr0 8 bits	Y0 8 bits	Cb0 8 bits

- 当DINSWAP[2:0]位=111b

b63 b56	b55 b48	b47 b40	b39 b32	b31 b24	b23 b16	b15 b8	b7 b0
Cr1 8 bits	Y3 8 bits	Cb1 8 bits	Y2 8 bits	Cr0 8 bits	Y1 8 bits	Cb0 8 bits	Y0 8 bits

(6) 输出编码数据

为了压缩，输出编码数据。JPEG编解码器以16位为单位处理编码数据的输出。因此，如果编码数据的码长为小数等奇数，则输出的最终码为D9FFh。

JIFECNT中的JOUTSWAP[2:0]位可用于改变输出中编码数据的排列。

57.3.2 Decompression

本节介绍解压流程。

(1) Processing overview

The decompression process overview is as follows:

1. The JPEG core is activated.
2. Coded data is transferred from the external buffer to the JPEG Codec.
   - If the count mode for stopping the input of coded data is on, reading stops each time the amount of coded data set in JIFDSLC is read. To resume reading, set the JINRCMD bit in JIFDCNT to 1.
   - When the JINRINI bit in JIFDCNT is 0, the addresses for reading on resumption are continued from the addresses in the previous round of transfer.
   - When the JINRINI bit is 1, the address set in JIFDSA is used on resumption.
   - Reading stops when the end of the coded data is detected.
   - If the count mode for stopping the input of coded data is off, reading continues until the end of code is detected. With this JPEG Codec, more coded data can be read than the coded data size because coded data reading continues until the end of code is detected.
3. Coded data is input to the JPEG core. The input data is processed in MCUs at any time in the JPEG core.
4. Image data is transferred in MCUs from the JPEG Codec to the external buffer.
   - If the count mode for stopping the output of image data lines is on, writing stops each time the number of image data lines set in JIFDDLC is written. To resume writing, set the DOUTRCMD bit in JIFDCNT to 1.
   - When the DOUTRINI bit in JIFDCNT is 0, the addresses for writing on resumption are continued from the addresses in the previous round of transfer.
   - When the DOUTRINI bit is 1, the address set in JIFDDA is used on resumption.
   - Writing stops when one frame of image data is completely transferred.
   - If the count mode for stopping the output of image data lines is off, writing continues until one frame of image data is completely transferred.
5. Decompression is complete after one frame of data is processed completely.

(a) Initial settings

To set the initial settings for decompression:

1. When the INT3 bit in JINTE0 is 0:
   After completing the JPEG core settings and input/output buffer settings and transferring coded data to the external buffer, activate the JPEG Codec by setting the JSRT bit in JCCMD to 1.
2. When the INT3 bit in JINTE0 is 1:
   a. After completing the JPEG core settings and input buffer settings and transferring coded data to the external buffer, activate the JPEG Codec by setting the JSRT bit in JCCMD to 1.
   b. When the image size and pixel format become readable after the coded data is decompressed, the INS3 bit in JINTS0 is set. At this time, decompression stops temporarily.
   c. After the image size and pixel format are read, set the output buffer.
   d. After interrupt handling, set the JRST bit in JCCMD to 1 to resume decompression.

(1) 处理概述

解压过程概览如下：

1. JPEG核心被激活。
2. 编码数据从外部缓冲区传输到JPEG编解码器。
   - 如果停止输入编码数据的计数模式打开，则每次读取JIFDSLC中设置的编码数据量时，读取停止。要恢复读取，请将JIFDCNT中的JINRCMD位设置为1。
   - 当JIFDCNT的JINRINI位为0时，恢复读取的地址从上一轮传输的地址开始继续。
   - 当JINRINI位为1时，在JIFDSA中设置的地址在恢复时使用。
   - 检测到编码数据结束时停止读取。
   - 如果停止输入编码数据的计数模式关闭，则继续读取直到检测到编码结束。
     使用此JPEG编解码器，可以读取比编码数据大小更多的编码数据，因为编码数据读取会持续到检测到代码结尾。
3. 编码数据输入到JPEG核心。输入数据在JPEG内核中随时在MCU中处理。
4. 图像数据在MCU中从JPEG编解码器传输到外部缓冲区。
   - 如果停止输出图像数据线的计数模式打开，则每次写入JIFDDLC中设置的图像数据线数时，写入停止。要恢复写入，请将JIFDCNT中的DOUTRCMD位设置为1。
   - 当JIFDCNT的DOUTRINI位为0时，恢复写入的地址从上一轮传输的地址开始继续。
   - 当DOUTRINI位为1时，在恢复时使用JIFDDA中设置的地址。
   - 当一帧图像数据传输完毕时，写入停止。
   - 如果停止输出图像数据线的计数模式为关闭，则继续写入直到一帧图像数据传输完毕。
5. 完成一帧数据处理后，解压完成。

(a) 初始设置

要设置减压的初始设置：

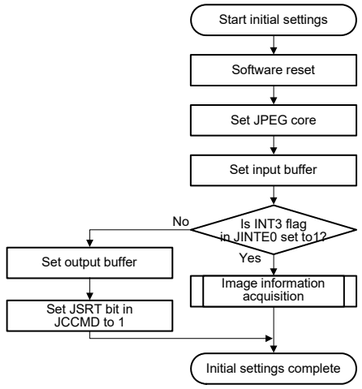
1. 当JINTE0的INT3位为0时：
   完成JPEG核心设置和输入输出缓冲区设置并将编码数据传输到外部缓冲区后，通过将JCCMD中的JSRT位设置为1来激活JPEG编解码器。
2. 当JINTE0的INT3位为1时：

   一个。完成JPEG核心设置和输入缓冲区设置并将编码数据传输到外部缓冲区后，通过将JCCMD中的JSRT位设置为1来激活JPEG编解码器。

   湾。当编码数据解压缩后图像大小和像素格式变得可读时，设置JINTS0中的INS3位。此时，减压暂时停止。

   C。读取图像大小和像素格式后，设置输出缓冲区。

   d。中断处理后，将JCCMD中的JRST位设置为1以恢复解压。



Software reset
Reset the JPEG Codec in advance by setting the BRST bit in the JCCMD register.

JPEG core settings

Compression setting:	DSP bit in JCMOD
JPEG size clear:	JCVSZU, JCVSZD, JCHSZU, and JCHSZD are set to 0
Decompression setting:	DSP bit in JCMOD
Interrupt setting:	INT7 to INT5 and INT3 flags in JINTE0

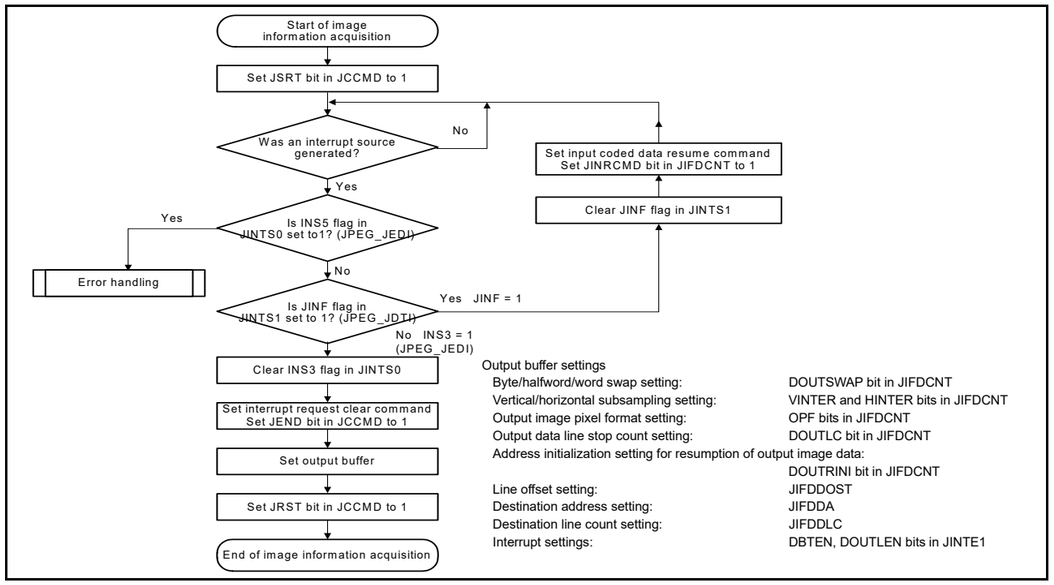
Input buffer settings

Byte/halfword/word swap setting:	JINSWAP bit in JIFDCNT
Input coded data stop count setting:	JINC bit in JIFDCNT
Address initialization setting for resumption of input coded data:	JINRINI bit in JIFDCNT
Source address setting:	JIFDSA
Source count setting:	JIFDSDC
Interrupt setting:	JINF bit in JINTS1 is set to 0 JINEN bit in JINTE1

Output buffer settings

Byte/halfword/word swap setting:	DOUTSWAP bit in JIFDCNT
Vertical/horizontal subsampling setting:	VINTER and HINTER bits in JIFDCNT
Output image pixel format setting:	OPF bits in JIFDCNT
Output data line stop count setting:	DOUTLC bit in JIFDCNT
Address initialization setting for resumption of output image data:	DOUTRINI bit in JIFDCNT
Line offset setting:	JIFDDOFST
Destination address setting:	JIFDDA
Destination line count setting:	JIFDDLC
Interrupt setting:	DBTF bit in JINTS1 is set to 0 DOUTLF bit in JINTS1 is set to 0 DBTEN, DOUTLEN bits in JINTE1

Figure 57.7 Flow of decompression initial settings



Output buffer settings

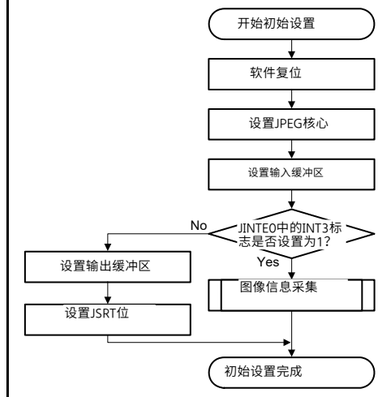
Byte/halfword/word swap setting:	DOUTSWAP bit in JIFDCNT
Vertical/horizontal subsampling setting:	VINTER and HINTER bits in JIFDCNT
Output image pixel format setting:	OPF bits in JIFDCNT
Output data line stop count setting:	DOUTLC bit in JIFDCNT
Address initialization setting for resumption of output image data:	DOUTRINI bit in JIFDCNT
Line offset setting:	JIFDDOFST
Destination address setting:	JIFDDA
Destination line count setting:	JIFDDLC
Interrupt settings:	DBTEN, DOUTLEN bits in JINTE1

Figure 57.8 Flow of image information acquisition

(b) Decompression process

The decompression process flow is as follows:

1. When JPEG decompression process is completed, the INS6 bit in JINTS0 sets to 1. However, the JPEG Codec continues processing, because the image data remains to be transferred. The DBTF bit in JINTS1 sets to 1 when the last image data is transferred. The interrupt source is cleared by a 0 write to the INS6 bit. However, the interrupt request asserted by this interrupt source cannot be cleared by a 0 write to the INS6 bit. Set an interrupt request clear



软件复位
通过设置JCCMD寄存器中的BRST位提前复位JPEG编解码器。

JPEG核心设置

Compression setting:	JCMOD中的DSP位
JPEG尺寸清晰：	JCVSZU, JCVSZD, JCHSZU, and JCHSZD设置为0
Decompression setting:	JCMOD中的DSP位
Interrupt setting:	JINTE0中的INT7到INT5和INT3标志

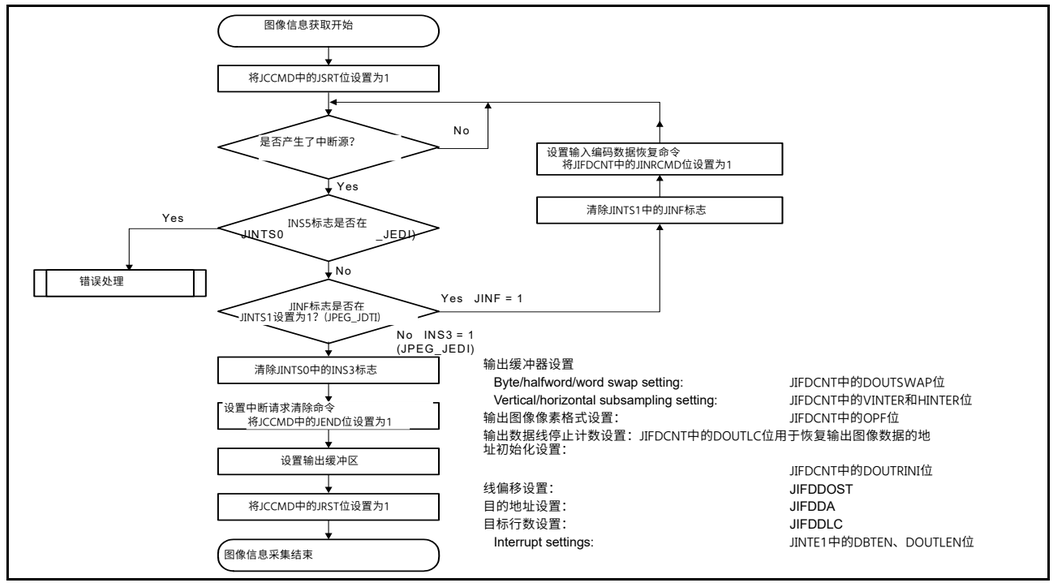
输入缓冲区设置

Byte/halfword/word swap setting:	JIFDCNT中的JINSWAP位
输入编码数据停止计数设置：	JIFDCNT中的JINC位
恢复输入编码数据的地址初始化设置：	JIFDCNT中的JINRINI位
源地址设置：	JIFDSA
源计数设置：	JIFDSDC
Interrupt setting:	JINTS1中的JINF位设置为0 JINTE1中的JINEN钻头

输出缓冲器设置

Byte/halfword/word swap setting:	JIFDCNT中的DOUTSWAP位
Vertical/horizontal subsampling setting:	JIFDCNT中的VINTER和HINTER位
输出图像像素格式设置：	JIFDCNT中的OPF位
输出数据线停止计数设置：	JIFDCNT中的DOUTLC位
恢复输出图像数据的地址初始化设置：	JIFDCNT中的DOUTRINI位
线偏移设置：	JIFDDOFST
目的地址设置：	JIFDDA
目标行数设置：	JIFDDLC
Interrupt setting:	JINTS1中的DBTF位设置为0 JINTS1中的DOUTLF位设置为0DBTEN，JINTE1中的DOUTLEN位

Figure 57.7 减压初始设定流程



输出缓冲器设置

Byte/halfword/word swap setting:	JIFDCNT中的DOUTSWAP位
Vertical/horizontal subsampling setting:	JIFDCNT中的VINTER和HINTER位
输出图像像素格式设置：	JIFDCNT中的OPF位
输出数据线停止计数设置：JIFDCNT中的DOUTLC位用于恢复输出图像数据的地址初始化设置：	JIFDCNT中的DOUTRINI位
线偏移设置：	JIFDDOFST
目的地址设置：	JIFDDA
目标行数设置：	JIFDDLC
Interrupt settings:	JINTE1中的DBTEN、DOUTLEN位

Figure 57.8 图像信息获取流程

(b) 解压过程

解压过程流程如下：

1. 当JPEG解压缩过程完成时，JINTS0中的INS6位设置为1。但是，JPEGCodec继续处理，因为图像数据还有待传输。当传输最后一个图像数据时，JINTS1中的DBTF位设置为1。向INS6位写入0可清除中断源。但是，此中断源发出的中断请求不能通过向INS6位写入0来清除。设置中断请求清除

command (by setting the JEND bit in JCCMD to 1) to clear the interrupt request.

2. When the JPEG Codec has completed decompression and all image data is transferred, the DBTF flag in JINTS1 sets to 1. When the DBTEN bit in JINTE1 is 1 here, an interrupt is generated. The interrupt source is cleared by a 0 write to the DBTF flag.
3. If the count mode for stopping input coded data is on, when the specified amount of coded data set in JIFDSDC is read, the JINF flag in JINTS1 sets to 1, and reading stops. When the JINEN bit in JINTE1 is 1 here, an interrupt is generated. An interrupt source is cleared by a 0 write to the JINF bit. Setting the JINRCMD bit in JIFDCNT to 1 resumes reading.
   - When the JINRINI bit in JIFDCNT is 0, the addresses for reading on resumption are continued from the addresses in the previous round of transfer.
   - When the JINRINI bit is 1, the address set in JIFDSA is used on resumption.
4. If the count mode for stopping the output image data is on, when the specified number of image data lines set in JIFDDLC is written, the DOUTLF flag in JINT1 sets to 1 and writing stops. When the DOUTLEN bit in JINTE1 is 1 here, an interrupt is generated. An interrupt source is cleared by a 0 write to the DOUTLF bit. Setting the DOUTRCMD bit in JIFDCNT to 1 resumes writing.
   - When the DOUTRINI bit in JIFDCNT is 0, the addresses for writing on resumption are continued from the addresses in the previous round of transfer.
   - When the DOUTRINI bit is 1, the address set in JIFDDA is used on resumption.

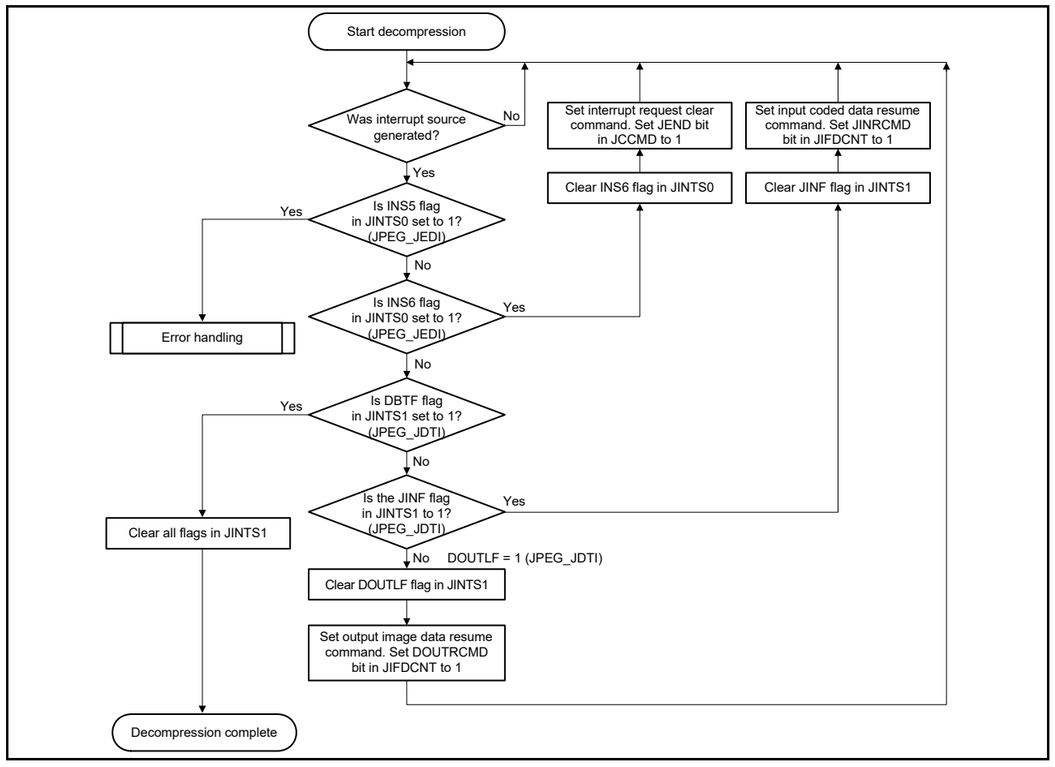


Figure 57.9 Decompression process flow

(c) Error handling

If the INS5 bit in JINTS0 is 1, it indicates that there is an error in the input JPEG coded data and that the decompression process by the JPEG Codec has ended. Read the ERR[3:0] bits in JCDERR to determine the cause of the error. Interrupt

命令（通过将JCCMD中的JEND位设置为1）来清除中断请求。

2. 当JPEGCodec完成解压并传输所有图像数据时，JINTS1中的DBTF标志置1。当JINTE1中的DBTEN位为1时，产生中断。中断源通过向DBTF标志写入0来清除。
3. 如果停止输入编码数据的计数模式打开，则当读取JIFDSDC中设置的指定数量的编码数据时，JINTS1中的JINF标志设置为1，并且读取停止。这里当JINTE1中的JINEN位为1时，产生中断。向JINF位写入0可清除中断源。将JIFDCNT中的JINRCMD位设置为1可恢复读取。
   - 当JIFDCNT的JINRINI位为0时，恢复读取的地址从上一轮传输的地址开始继续。
   - 当JINRINI位为1时，在JIFDSA中设置的地址在恢复时使用。
4. 如果停止输出图像数据的计数模式打开，当指定的图像数据行数设置在写入JIFDDLC，JINT1中的DOUTLF标志设置为1，写入停止。这里当JINTE1的DOUTLEN位为1时，产生中断。向DOUTLF位写入0可清除中断源。将JIFDCNT中的DOUTRCMD位设置为1可恢复写入。
   - 当JIFDCNT的DOUTRINI位为0时，恢复写入的地址从上一轮传输的地址开始继续。
   - 当DOUTRINI位为1时，在恢复时使用JIFDDA中设置的地址。

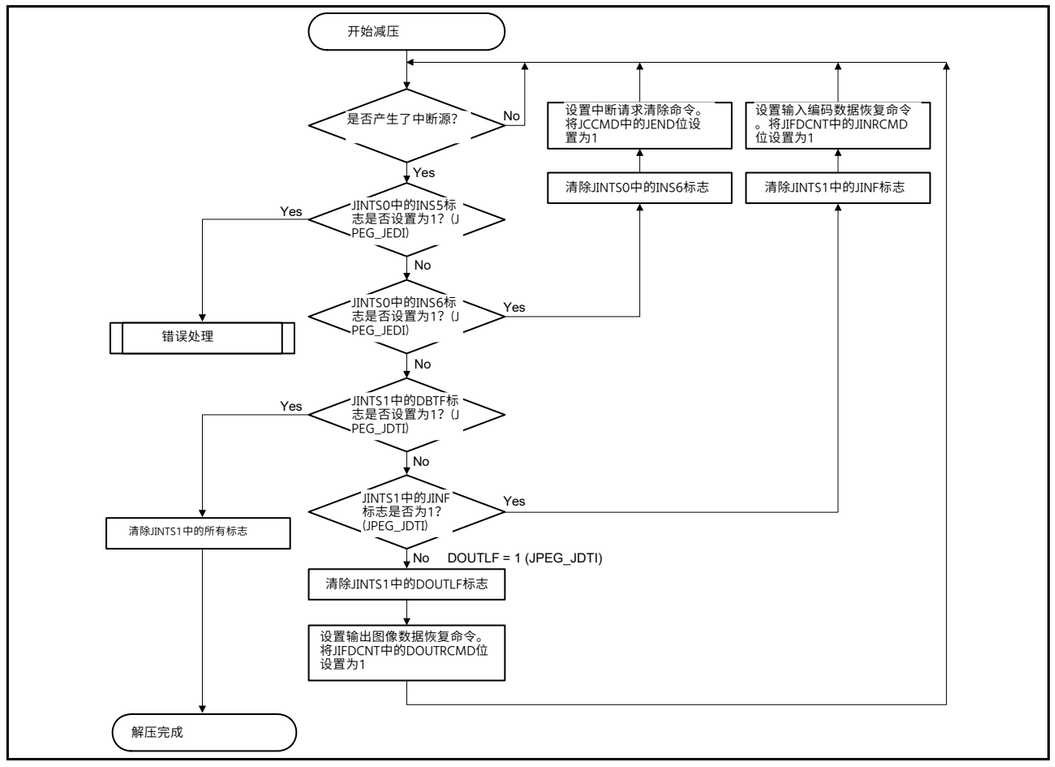


Figure 57.9 减压工艺流程

(c) 错误处理

如果JINTS0中的INS5位为1，则表示输入的JPEG编码数据有错误，JPEGCodec的解压过程已经结束。读取JCDERR中的ERR[3:0]位以确定错误原因。打断

signals asserted because of the interrupt source indicated in the INS5 bit cannot be negated by clearing the interrupt status with a 0 write. To clear the interrupt request, you must set the interrupt request clear command (by setting the JEND bit in JCCMD to 1). To perform decompression or compression processing after error handling finishes, start the processing from the initial settings.

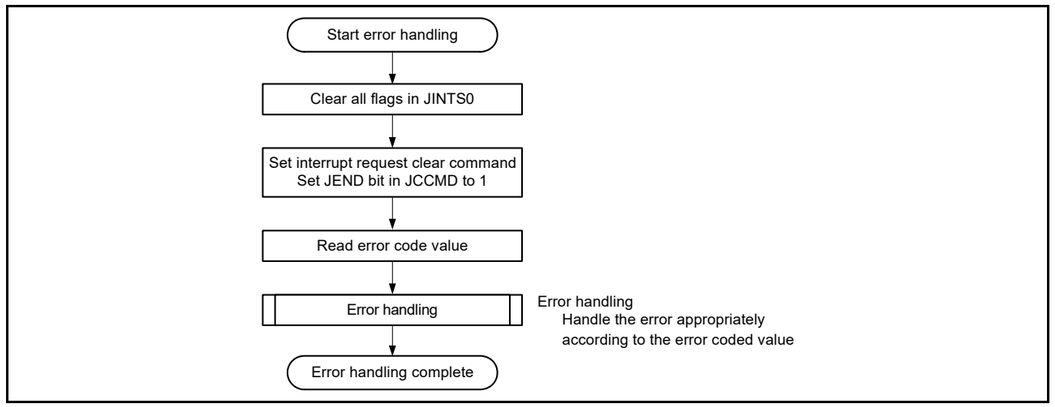


Figure 57.10 Error handling flow

(2) Input JPEG coded data

The markers to be processed in decompression are SOI, SOF0, SOS, DQT, DHT, DRI, RSTm, and EOI. Except for the error markers shown in Table 57.3, other markers are ignored even if they are read.

The JINSWAP[2:0] bits in JIFDCNT can be used to alter the arrangement for the input of coded data.

(3) JPEG decompression errors

(a) Error markers

If a marker error is found during analysis of compressed data for decompression, the code to identify the error type (shown in Table 57.3) is set to the ERR[3:0] bits in JCDERR. When an error is detected, the JPEG Codec generates an interrupt signal and terminates decoding. The stored code value is set to 1010b (default value) at the start of processing of the next frame or after a bus reset.

Table 57.3 Decompression error codes (1 of 2)

Code	Description
0000b	Normal
0001b	SOI not detected: SOI not detected until EOI detected
0010b	SOF1 to SOFF detected
0011b	Unprovided pixel format detected
0100b	SOF accuracy error: Value other than 8 detected
0101b	DQT accuracy error: Value other than 0 detected
0110b	Component error 1: Number of SOF0 header components detected is value other than 1, 3, or 4
0111b	Component error 2: Number of components differs between SOF0 header and SOS
1000b	SOF0, DQT, and DHT not detected when SOS detected
1001b	SOS not detected: SOS not detected until EOI detected
1010b	EOI not detected (default)
1011b	Restart interval data number error detected
1100b	Image size error detected
1101b	Last MCU data number error detected

由于INS5位中指示的中断源而断言的信号不能通过用0写入清除中断状态来否定。要清除中断请求，必须设置中断请求清除命令（通过将JCCMD中的JEND位设置为1）。要在错误处理完成后执行解压缩或压缩处理，请从初始设置开始处理。

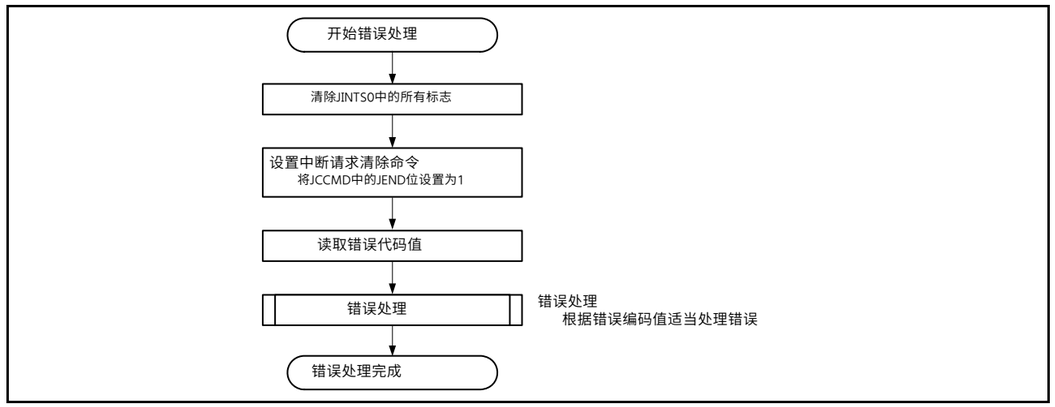


Figure 57.10 错误处理流程

(2) 输入JPEG编码数据

解压需要处理的标记有SOI、SOF0、SOS、DQT、DHT、DRI、RSTm、EOI。除了表57.3中所示的错误标记外，其他标记即使被读取也会被忽略。

JIFDCNT中的JINSWAP[2:0]位可用于更改编码数据输入的排列。

(3) JPEG解压缩错误

(a) 错误标记

如果在解压压缩数据分析过程中发现标记错误，则将识别错误类型的代码（如表57.3所示）设置为JCDERR中的ERR[3:0]位。当检测到错误时，JPEG编解码器生成中断信号并终止解码。存储的代码值在下一帧处理开始时或总线复位后设置为1010b（默认值）。

Table 57.3 解压错误代码(1of2)

Code	Description
0000b	Normal
0001b	未检测到SOI：在检测到EOI之前未检测到SOI
0010b	检测到SOF1到SOFF
0011b	检测到未提供的像素格式
0100b	SOF精度错误：检测到8以外的值
0101b	DQT精度错误：检测到非0值
0110b	组件错误1：检测到的SOF0标头组件的数量是1、3或4以外的值
0111b	组件错误2：SOF0标头和SOS之间的组件数量不同
1000b	检测到SOS时未检测到SOF0、DQT和DHT
1001b	未检测到SOS：在检测到EOI之前未检测到SOS
1010b	未检测到意向书（默认）
1011b	检测到重启间隔数据数错误
1100b	检测到图像尺寸错误
1101b	检测到最后一个MCU数据编号错误

Table 57.3 Decompression error codes (2 of 2)

Code	Description
1110b	Block data number error detected

(b) Huffman coded segment error

During the compression data analysis in decompression operation, if there is an increase or decrease in the decoded data count because of an error resulting from bit reversal or missing data in the Huffman-coded segment, determine the error type, and set the error code in the ERR[3:0] bits in JCDERR. Table Table 57.4 lists the segment error codes. The error code is set, an interrupt signal is issued, and the process ends only if the INT7 to INT5 bit in JINTE0 associated with the detected error is set to 1. The set code value returns to the default value (1010h) at the start of processing of the next frame or after a bus reset. However, in this error detection if an error in the Huffman-coded segment does not result in an alteration in the decoded data count, the error is undetected.

Figure 57.11 shows an example of the number of data units in a Huffman coded segment with pixel format setting YCbCr422, DRI = 2, X = 80 pixels, and Y = 8 pixels.

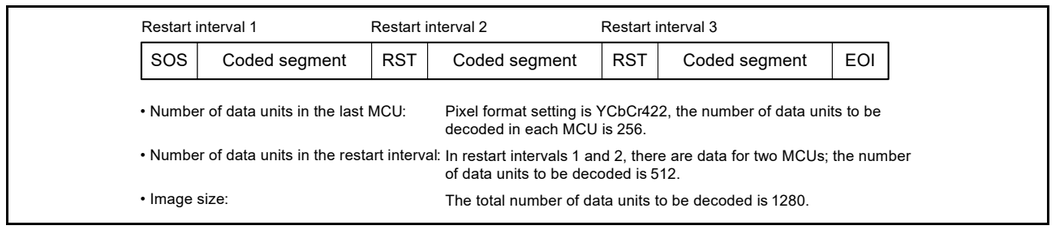


Figure 57.11 Huffman coded segment

Table 57.4 Segment error codes

Code	Description
0000h	Normal
1011h	Restart interval data number error: The number of data units in each interval is compared with the number of data units specified by the DRI marker. If an interval has more or less data than is specified by the DRI marker, the decompression error code (1011) is set. The last interval which is shorter than the restart interval is not compared. If the DRI marker segment is not placed or the specified number is 00, an error is not detected even if the RSTm marker is placed. Also, an m indicating the order of RSTm marker modulo 8 (m = 0 to 7) is exempt from the error detection analysis. When the INT7 bit in JINTE0 sets to 0, this error is not detected.
1100h	Image size error: The number of data units in an image that is calculated from the number of lines specified by the frame parameter and the number of samples per line is compared with the total number of data units from SOS to EOI (in pixel units). If the numbers of data units do not match, the decompression error code (1100) is set. When the INT6 bit in JINTE0 sets to 0, this error is not detected. The number of data units in an image is shown in MCUs. As a result, the number of lines and the number of samples per line for calculation must be shown in MCUs.
1101h	Last MCU data number error: Whether the number of data units in MCUs on EOI detection is shown in MCU units is checked and fractions are detected. If error (1100) occurs simultaneously with another error, error (1100) has priority. When the INT5 bit in JINTE0 sets to 0, this error is not detected.
1110h	Block data number error: Whether a block is an 8 × 8 array is checked and fractions are detected. When the INT7 to INT5 bits in JINTE0 are all set to 0, this error is not detected.

57.3.3 Output Pixel Format in Decompression

The JPEG Codec is capable of decompressing JPEG encoded data created in the YCbCr444, YCbCr422, YCbCr411, and YCbCr420 formats. The pixel format of the output image is ARGB8888 or RGB565. Figure 57.12 shows the flow of converting decompressed data to the given output pixel format.

Table 57.3 解压错误代码(2of2)

Code	Description
1110b	检测到块数据编号错误

(b) 霍夫曼编码段错误

在解压操作中进行压缩数据分析时，如果由于Huffman编码段位反转或丢失数据导致解码数据计数增加或减少，则判断错误类型，并将错误代码设置为JCDERR中的ERR[3:0]位。表57.4列出了段错误代码。设置错误代码，发出中断信号，只有当与检测到的错误相关的JINTE0中的INT7到INT5位设置为1时，该过程才结束。设置的代码值在开始时返回默认值（1010h）处理下一帧或总线复位后。然而，在该错误检测中，如果霍夫曼编码段中的错误不导致解码数据计数的改变，则错误未被检测到。

图57.11显示了具有像素格式设置的霍夫曼编码段中数据单元数量的示例
YCbCr422，DRI=2，X=80像素，Y=8像素。

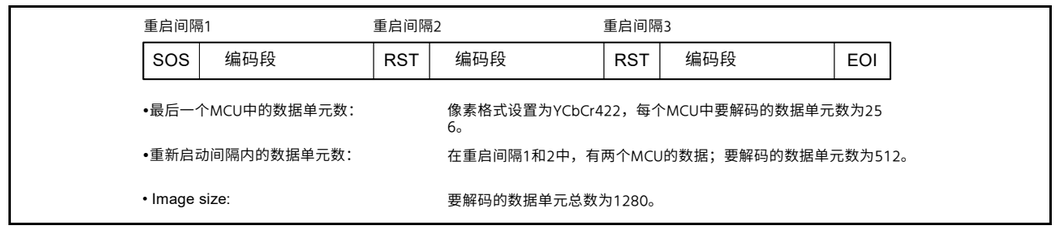


Figure 57.11 霍夫曼编码段

Table 57.4 段错误代码

Code	Description
0000h	Normal
1011h	重启间隔数据数错误： 将每个区间中的数据单元数与DRI标记指定的数据单元数进行比较。如果间隔的数据多于或少于DRI标记指定的数据，则设置解压缩错误代码(1011)。不比较比重新启动间隔短的最后一个间隔。如果没有放置DRI标记段或指定编号为00，即使 放置RSTm标记。此外，指示RSTm标记模8（m=0到7）的阶数的m不属于错误检测分析。当JINTE0中的INT7位设置为0时，不会检测到此错误。
1100h	图片尺寸错误： 将根据帧参数指定的行数和每行的样本数计算出的图像中的数据单元数与从SOS到EOI的数据单元总数（以像素为单位）进行比较。如果数据单元的数量不匹配，则设置解压缩错误代码（1100）。当JINTE0中的INT6位设置为0时，不会检测到该错误。图像中的数据单元数量显示在MCU中。因此，必须在MCU中显示用于计算的行数和每行的采样数。
1101h	最后MCU数据编号错误： 检查EOI检测时MCU中数据单元的数量是否以MCU为单位显示，并检测分数。如果错误(1100)与另一个错误同时发生，则错误(1100)具有优先权。当JINTE0中的INT5位设置为0时，不会检测到此错误。
1110h	块数据编号错误： 检查块是否为8×8数组并检测分数。当JINTE0中的INT7到INT5位都设置为0时，不会检测到该错误。

57.3.3 解压输出像素格式

JPEG编解码器能够解压缩在YCbCr444、YCbCr422、YCbCr411和
YCbCr420格式。输出图像的像素格式为ARGB8888或RGB565。图57.12显示了将解压缩数据转换为给定输出像素格式的流程。

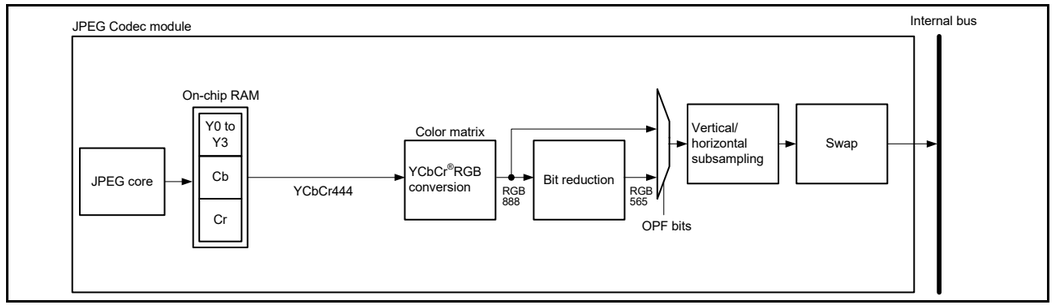


Figure 57.12 Output pixel format conversion in decompression block diagram

(1) On-chip SRAM

Data decoded by the JPEG core is stored in MCUs on SRAM in the JPEG Codec.

(2) YCbCr → RGB conversion

Data in the YCbCr444 format is converted to the RGB888 format. The following formulas are used:

R = 1.000Y + 1.402Cr
G = 1.000Y - 0.344Cb - 0.714Cr
B = 1.000Y + 1.772Cb

(3) Bit reduction

RGB888 data is reduced to RGB565 data. The lower three bits of red and blue, and lower two bits of green are removed.

(4) Output pixel format selection

The pixel format to be output is selected in the OPF[1:0] bits in JIFDCNT. When the DOUTSWAP[2:0] bits in JIFDCNT = 000b, allocation of data in the pixel format is as follows:

- ARGB8888 (32 bits/pixel)

b31 b24	b23 b16	b15 b8	b7 b0
*1	Red 8 bits	Green 8 bits	Blue 8 bits

Note 1. This value is determined by the ALPHA[7:0] bits in JIFDADT.

- RGB565 (16 bits/pixel)

b15 b11	b10 b5	b4 b0
Red 5 bits	Green 6 bits	Blue 5 bits

(5) Vertical and horizontal subsampling

The output data can be horizontally and vertically subsampled based on the VINTER[1:0] and HINTER[1:0] settings in JIFDCNT. Figure 57.13 to Figure 57.15 show the line subsampling modes. In the figures, for the ARGB8888 and RGB565 output formats, one cell represents one pixel. Because sub-sampling is carried out in minimum coded units (MCUs), the numbers of the horizontal and vertical block units vary based on the decompressed pixel format.

Table 57.5 and Table 57.6 show the values of n and m in the figures.

Horizontal

Table 57.5 Number of horizontal blocks (1 of 2)

Compression format	Output format	n
YCbCr444	ARGB8888, RGB565	1
YCbCr422	ARGB8888, RGB565	2

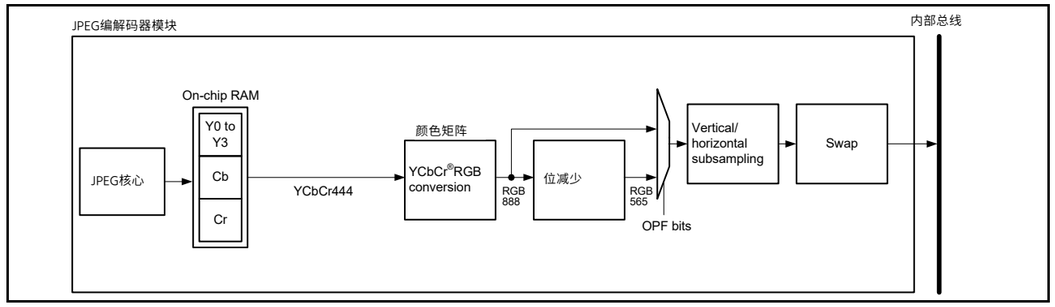


Figure 57.12 解压框图中的输出像素格式转换

(1) On-chip SRAM

JPEG内核解码的数据存储在JPEG编解码器中SRAM上的MCU中。

(2) YCbCr → RGB conversion

YCbCr444格式的数据转换为RGB888格式。使用以下公式：

R = 1.000Y + 1.402Cr
G = 1.000Y - 0.344Cb - 0.714Cr
B = 1.000Y + 1.772Cb

(3) 位减少

RGB888数据减少为RGB565数据。红色和蓝色的低三位以及绿色的低两位被移除。

(4) 输出像素格式选择

要输出的像素格式在JIFDCNT的OPF[1:0]位中选择。当JIFDCNT中的DOUTSWAP[2:0]位=000b时，像素格式的数据分配如下：

- ARGB8888 (32 bits/pixel)

b31 b24	b23 b16	b15 b8	b7 b0
*1	红色8位	绿色8位	蓝色8位

注1.该值由JIFDADT中的ALPHA[7:0]位确定。

- RGB565 (16 bits/pixel)

b15 b11	b10 b5	b4 b0
红色5位	绿色6位	蓝色5位

(5) 垂直和水平二次采样

输出数据可以根据VINTER[1:0]和HINTER[1:0]设置进行水平和垂直二次采样JIFDCNT。图57.13到图57.15显示了线二次采样模式。在图中，对于ARGB8888和RGB565输出格式，一个单元格代表一个像素。由于子采样是在最小编码单元(MCU)中执行的，因此水平和垂直块单元的数量会根据解压缩的像素格式而有所不同。

表57.5和表57.6显示了图中n和m的值。

Horizontal

Table 57.5 水平块数（2个中的1个）

压缩格式	输出格式	n
YCbCr444	ARGB8888, RGB565	1
YCbCr422	ARGB8888, RGB565	2

Table 57.5 Number of horizontal blocks (2 of 2)

Compression format	Output format	n
YCbCr411	ARGB8888, RGB565	4
YCbCr420	ARGB8888, RGB565	2

Vertical

Table 57.6 Number of vertical blocks

Compression format	Output format	m
YCbCr444	ARGB8888, RGB565	1
YCbCr422	ARGB8888, RGB565	1
YCbCr411	ARGB8888, RGB565	1
YCbCr420	ARGB8888, RGB565	2

- Sub-sampling into 1/2

  Even lines are skipped by sub-sampling.

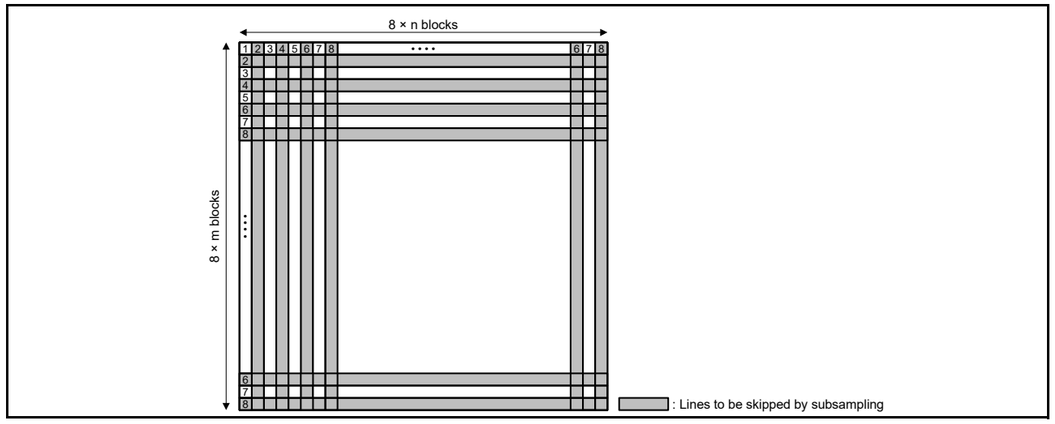


Figure 57.13 MCU when sub-sampling into 1/2 is selected

- Sub-sampling into 1/4

  The second, third, and fourth lines are skipped by sub-sampling.

Table 57.5 水平块数（2个中的2个）

压缩格式	输出格式	n
YCbCr411	ARGB8888, RGB565	4
YCbCr420	ARGB8888, RGB565	2

Vertical

Table 57.6 垂直块数

压缩格式	输出格式	m
YCbCr444	ARGB8888, RGB565	1
YCbCr422	ARGB8888, RGB565	1
YCbCr411	ARGB8888, RGB565	1
YCbCr420	ARGB8888, RGB565	2

- Sub-sampling into 1/2

  子采样甚至跳过了行。

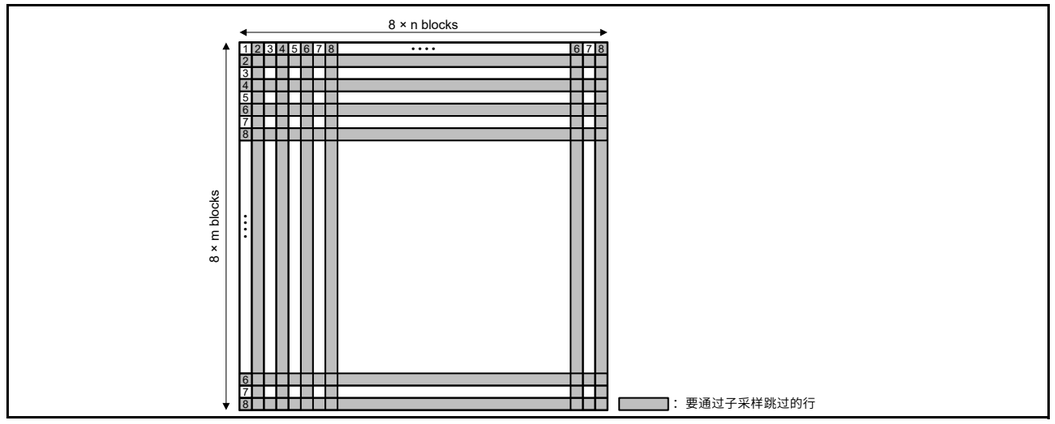


Figure 57.13 选择子采样到12时的MCU

- Sub-sampling into 1/4

  第二、第三和第四行通过子采样跳过。

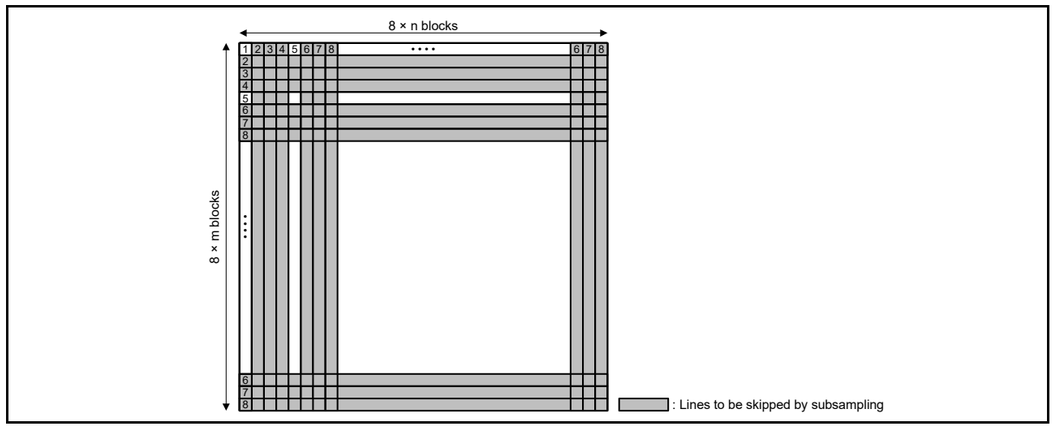


Figure 57.14 MCU when sub-sampling into 1/4 is selected

- Sub-sampling into 1/8

  The second, third, fourth, fifth, sixth, seventh, and eighth lines are skipped by sub-sampling.

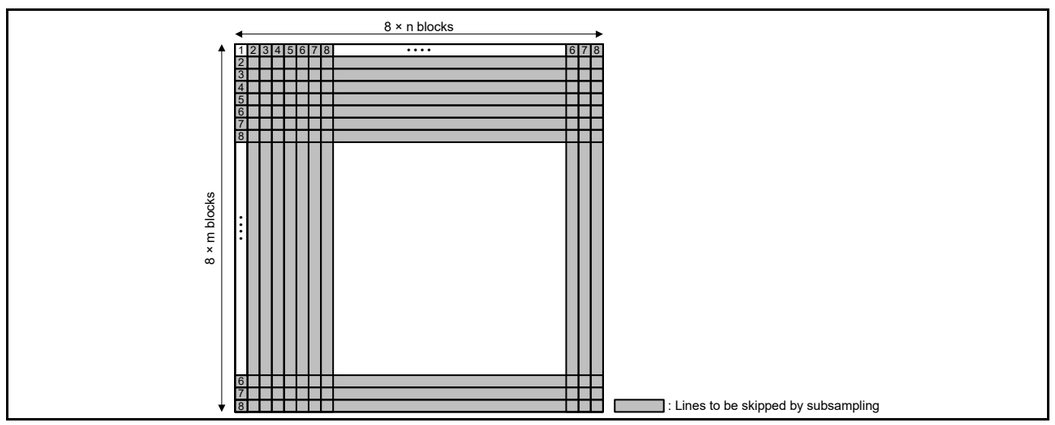


Figure 57.15 MCU when sub-sampling into 1/8 is selected

(6) Swap

Allocation of data can be changed using the DOUTSWAP[2:0] bits in JIFDCNT.

57.3.4 Storing Image Data

Figure 57.16 shows the buffer area for storing the image data.

- Start address
  - Compression: JIFESA
  - Decompression: JIFDDA
- Horizontal size
  - Compression, decompression: JCHSZU, JCHSZD
- Vertical size
  - Compression, decompression: JCVSAU, JCVSZD

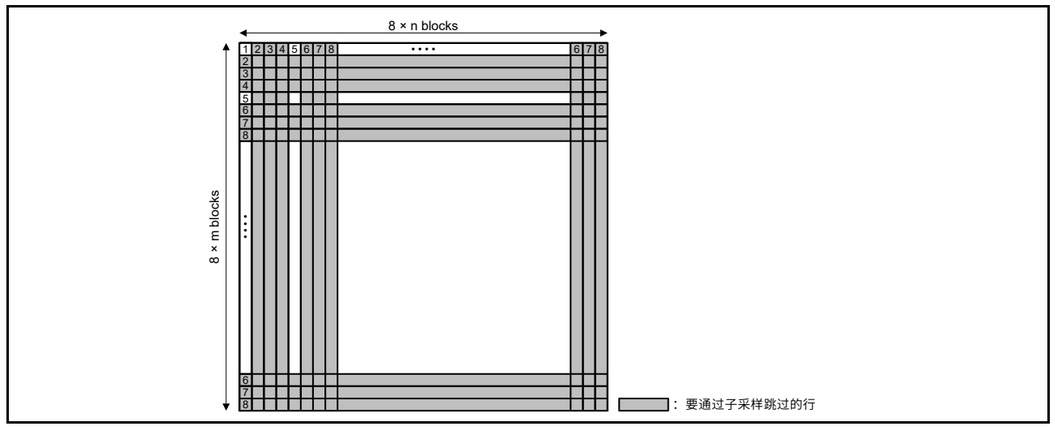


Figure 57.14 选择子采样到14时的MCU

- Sub-sampling into 1/8

  第二、三、四、五、六、七、八行通过二次采样跳过。

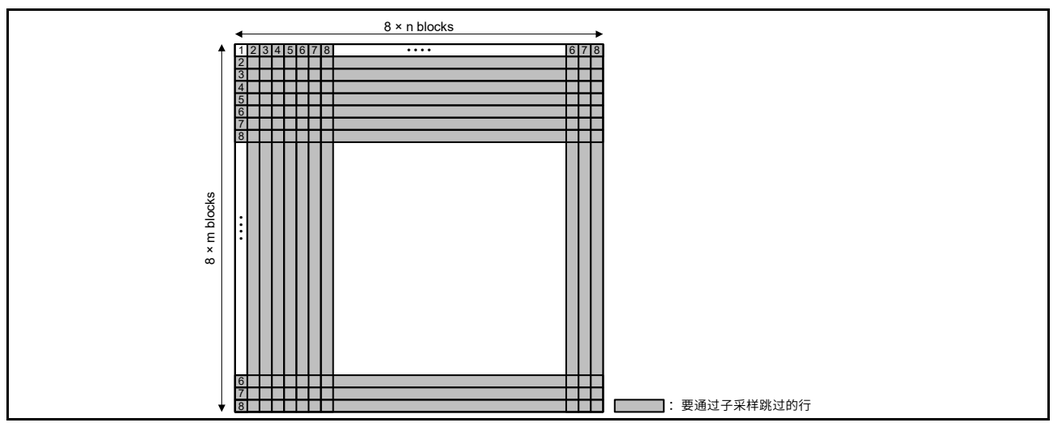


Figure 57.15 选择子采样到18时的MCU

(6) Swap

可以使用JIFDCNT中的DOUTSWAP[2:0]位更改数据分配。

57.3.4 存储图像数据

图57.16显示了用于存储图像数据的缓冲区。

- 起始地址
  - Compression: JIFESA
  - Decompression: JIFDDA
- 水平尺寸
  - Compression, decompression: JCHSZU, JCHSZD
- 垂直尺寸
  - Compression, decompression: JCVSAU, JCVSZD

- Offset
  - Compression: JIFESOFST
  - Decompression: JIFDDOFST

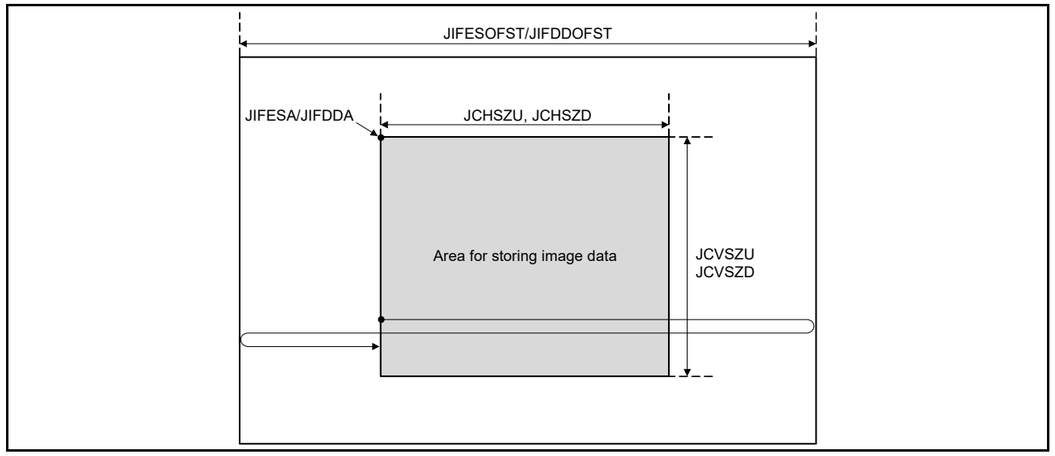


Figure 57.16 Conceptual diagram of image data storing

57.4 Interrupts

Two types of interrupt requests, compression/decompression process interrupt requests (JPEG_JEDI) and data transfer interrupt requests (JPEG_JDTI), are available in the JPEG Codec. The two types of interrupt requests are each related to multiple sources. The interrupt request cancellation methods differ depending on the source of the interrupt request.

57.4.1 Compression/Decompression Process Interrupt Request (JPEG_JEDI)

The flags in JINTS0 indicate compression and decompression-related sources. The interrupt requests asserted by these interrupt sources cannot be negated by clearing the associated interrupt status bits to 0. Issue an interrupt request clear command (by setting the JEND bit in JCCMD to 1) to clear the interrupt request. When a flag in JINTS0 sets to 1, a compression/decompression process interrupt request is sent to the Interrupt Controller Unit (ICU).

(1) Compression

- JPEG compression process end

  When the INS6 bit in JINTS0 is 1, the JPEG compression process completed successfully. After all of the coded data is transferred, the JPEG Codec completes compression.

(2) Decompression

- JPEG decompression process end

  When the INS6 bit in JINTS0 is 1, the JPEG decompression process completed successfully. After all of the image data is transferred, the JPEG Codec completes decompression.
- JPEG decompression error occurrence

  When the INS5 bit in JINTS0 is 1, the input JPEG coded data has an error and the JPEG Codec has stopped the decompression process. Read the error code (ERR[3:0] bits in JCDERR) and identify the error source. This interrupt occurs when any of the INT7 to INT5 bits in JINTE0 is 1.
- Request for reading the image size and pixel format

  When the INS3 bit in JINTS0 is 1, JPEG coded data is input, and information regarding the image size and pixel format can be read. Because the JPEG decompression process is suspended, resume the JPEG decompression process by setting the process stop clear command after accessing the required registers. This interrupt occurs when

- Offset
  - Compression: JIFESOFST
  - Decompression: JIFDDOFST

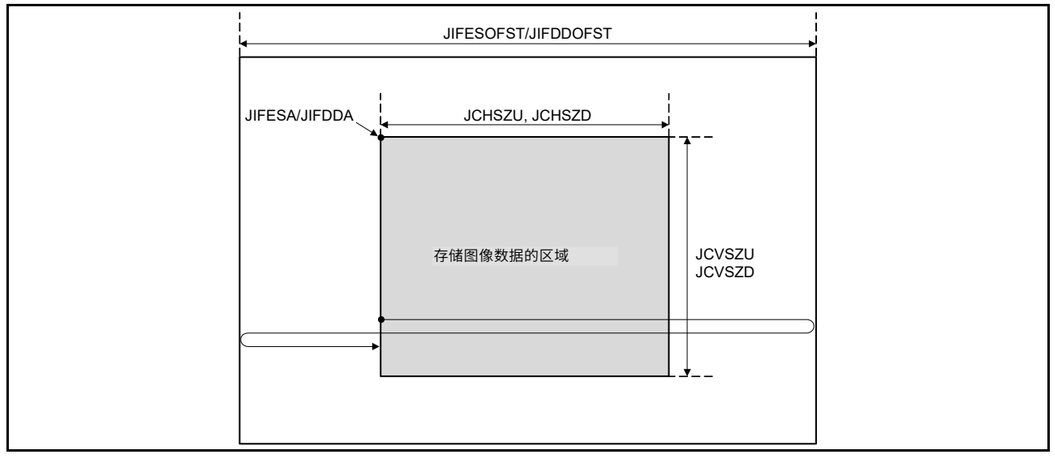


Figure 57.16 图像数据存储概念图

57.4 Interrupts

JPEG编解码器中提供了两种类型的中断请求，压缩解压缩过程中断请求(JPEG_JEDI)和数据传输中断请求(JPEG_JDTI)。这两种类型的中断请求都与多个源相关。中断请求取消方法因中断请求的来源而异。

57.4.1 压缩解压缩过程中断请求(JPEG_JEDI)

JINTS0中的标志指示与压缩和解压缩相关的源。这些中断源发出的中断请求不能通过将相关中断状态位清除为0来取消。发出中断请求清除命令（通过将JCCMD中的JEND位设置为1）来清除中断请求。当JINTS0中的标志设置为1时，向中断控制器单元(ICU)发送压缩解压缩过程中断请求。

(1) Compression

- JPEG压缩处理结束

  当JINTS0中的INS6位为1时，JPEG压缩过程成功完成。传输完所有编码数据后，JPEG编解码器完成压缩。

(2) Decompression

- JPEG解压过程结束

  当JINTS0中的INS6位为1时，JPEG解压过程成功完成。传输完所有图像数据后，JPEGCodec完成解压缩。

- JPEG解压错误发生

  当JINTS0中的INS5位为1时，输入的JPEG编码数据有错误，JPEGCodec已停止解压过程。读取错误代码（JCDERR中的ERR[3:0]位）并识别错误源。当JINTE0中的任何INT7到INT5位为1时，将发生此中断。

- 请求读取图像大小和像素格式

  当JINTS0的INS3位为1时，输入JPEG编码数据，可以读取图像大小和像素格式的信息。由于JPEG解压过程暂停，请在访问所需寄存器后通过设置processstopclear命令恢复JPEG解压过程。此中断发生时

the INT3 bit in JINTE0 is 1.

57.4.2 Data Transfer Interrupt Request (JPEG_JDTI)

The flags in JINTS1 are the interrupt sources for transferring the image data and coded data. The interrupt requests asserted by these interrupt sources can be negated by clearing the associated interrupt status bits to 0.

(1) Compression

- Interrupt request generated after the specified number of input image data lines is read

  When the DINLF bit in JINTS1 is 1, the number of image data lines specified in JIFESLC is transferred. Transfer the rest of the image data to the external buffer and resume transferring the data from the external buffer. A data transfer interrupt request is sent when the DINLEN bit in JINTE1 is 1.
- Interrupt request generated after all processes are complete

  When the CBTF bit in JINTS1 is 1, the JPEG Codec has completed compression and transferred all of the coded data. The data transfer interrupt request is sent when the CBTEN bit in JINTE1 is set to 1.

(2) Decompression

- Interrupt request generated after the specified number of output image data lines is written to

  When the DOUTLF bit in the JINTS1 is 1, the number of image data lines specified in JIFDDLC is transferred. Secure a space for the next coded data in the external buffer and resume the transfer process. A data transfer interrupt request is sent when the DOUTLEN bit in JINTE1 is 1.
- Interrupt request generated after the specified amount of input coded data is read

  The JINF bit in JINTS1 sets to 1 when the amount of coded data specified in JIFDSDC is transferred. Secure the next coded data in the external buffer and resume the transfer process. A data transfer interrupt is also sent at this time if the JINEN bit in JINTE1 is 1.
- Interrupt request generated after all processes are completed

  The DBTF bit in JINTS1 sets to 1 when the JPEG Codec has completed decompression and transferred all of the coded data. A data transfer interrupt request is also sent at this time if the DBTEN bit in JINTE1 is set to 1.

57.5 Bus Reset Processing

Issuing the bus reset command (setting the BRST bit in JCCMD to 1) causes a bus reset. Do not issue the bus reset command while the JPEG Codec is operating. The following registers are initialized by a bus reset:

- JPEG Code Data Count Upper Register (JCDTCU)
- JPEG Code Data Count Middle Register (JCDTCM)
- JPEG Code Data Count Lower Register (JCDTCD)
- JPEG Interrupt Status Register 0 (JINTS0)
- JPEG Code Decode Error Register (JCDERR)
- JPEG Code Reset Register (JCRST).

57.6 Usage Notes

57.6.1 Notes on the Decompression Process

Renesas recommends that a timeout detection mechanism be implemented through software or through the operating system to prevent locking of the module in case invalid JPEG code data is detected. This timeout detection mechanism is recommended especially when setting JIFDCNT.JINC bit to 1 because the decompression process might not be complete depending on the timing of the JPEG code data input. If a timeout error occurs while decoding the image, reset the JPEG Codec by setting the BRST bit in the JCCMD register first, then follow the flow for decompression initial settings as shown in Figure 57.7.

JINTE0中的INT3位为1。

57.4.2 数据传输中断请求(JPEG_JDTI)

JINTS1中的标志位是传输图像数据和编码数据的中断源。这些中断源发出的中断请求可以通过将相关的中断状态位清除为0来取消。

(1) Compression

- 读取指定数量的输入图像数据线后产生的中断请求

  JINTS1中的DINLF位为1时，传送JIFESLC中指定的图像数据行数。将剩余的图像数据传输到外部缓冲区并从外部缓冲区继续传输数据。当JINTE1的DINLEN位为1时，发送数据传输中断请求。

- 所有进程完成后产生的中断请求

  当JINTS1中的CBTF位为1时，JPEGCodec已完成压缩并传输所有编码数据。当JINTE1中的CBTEN位设置为1时，发送数据传输中断请求。

(2) Decompression

- 写入指定数量的输出图像数据线后产生的中断请求

  当JINTS1中的DOUTLF位为1时，传输JIFDDLC中指定的图像数据行数。
  为外部缓冲区中的下一个编码数据保留一个空间并恢复传输过程。当JINTE1的DOUTLEN位为1时，发送数据传输中断请求。

- 读取指定数量的输入编码数据后产生的中断请求

  当传输JIFDSDC中指定的编码数据量时，JINTS1中的JINF位设置为1。保护外部缓冲区中的下一个编码数据并恢复传输过程。如果JINTE1中的JINEN位为1，此时也会发送数据传输中断。

- 所有进程完成后产生的中断请求

  当JPEGCodec完成解压缩并传输所有编码数据时，JINTS1中的DBTF位设置为1。如果JINTE1中的DBTEN位设置为1，此时也会发送数据传输中断请求。

57.5 总线复位处理

发出总线复位命令（将JCCMD中的BRST位设置为1）会导致总线复位。不要在JPEG编解码器运行时发出总线复位命令。以下寄存器由总线复位初始化：

- JPEG代码数据计数高位寄存器(JCDTCU)
- JPEG代码数据计数中间寄存器(JCDTCM)
- JPEG代码数据计数低位寄存器(JCDTCD)
- JPEG中断状态寄存器0(JINTS0)
- JPEG代码解码错误寄存器(JCDERR)
- JPEG代码复位寄存器(JCRST)。

57.6 使用说明

57.6.1 解压过程注意事项

瑞萨建议通过软件或操作系统实现超时检测机　　制，以防止在检测到无效JPEG代码数据时锁定模块。建议使用这种超时检测机　　制，尤其是在将JIFDCNT.JINC位设置为1时，因为根据JPEG代码数据输入的时序，解压缩过程可能无法完成。如果在解码图像时发生超时错误，首先通过设置JCCMD寄存器中的BRST位来复位JPEGCodec，然后按照图57.7所示的流程进行解压初始设置。

58. Graphics LCD Controller (GLCDC)

The multifunctional Graphics LCD Controller (GLCDC) supports multiple data formats and panels. Key GLCDC features include:

- GPX bus master function for accessing graphics data
- Superimposition of three planes (single color background plane, graphics 1 plane, and graphics 2 plane)
- Supports many types of 32- and 16-bit/pixel graphics data and 8-, 4-, and 1-bit LUT data formats
- Digital interface signal output supporting the video image size of WVGA.

Figure 58.1 shows a block diagram of the GLCDC.

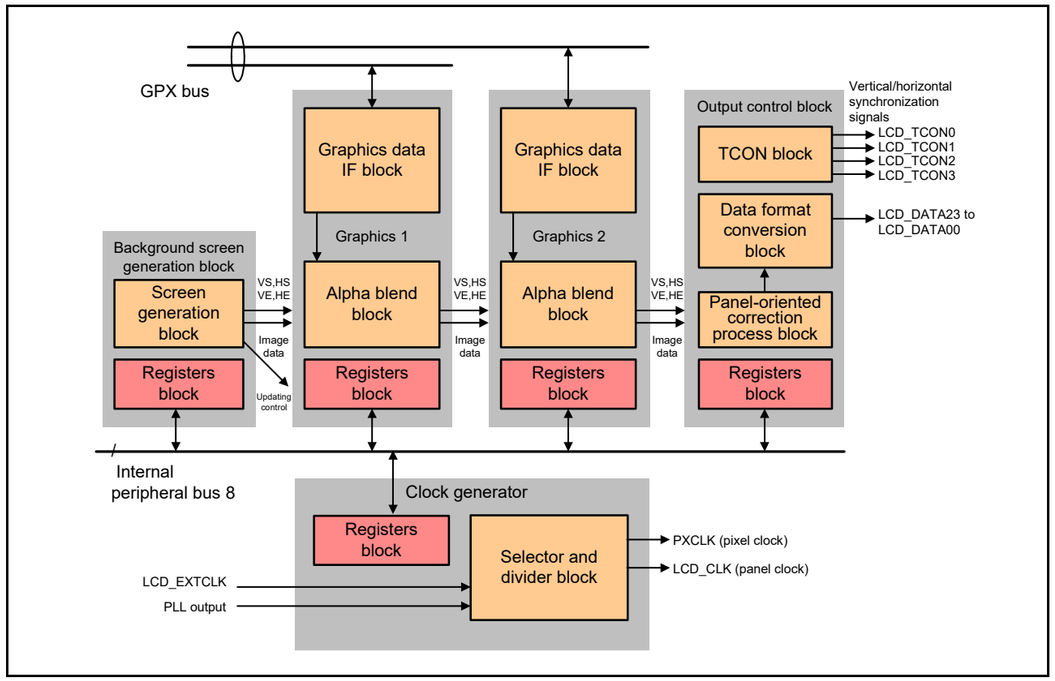


Figure 58.1 GLCDC block diagram

Note: When using the GLCDC, set the clock to ICLK = PCLKA.

Table 58.1 GLCDC I/O pins (1 of 2)

Pin name	I/O	Function
LCD_EXTCLK	Input	Panel clock source input pin
LCD_CLK	Output	Panel clock output pin
LCD_DATA23 to LCD_DATA00	Output	LCD signal output pins RGB888 signal R/G/B: 8 bits each (unsigned) RGB666 signal R/G/B: 6 bits each (unsigned) RGB565 signal R/B: 5 bits each (unsigned) G: 6 bits (unsigned) Serial RGB signal R/G/B/-: 8 bits (unsigned)
LCD_TCON3	Output	LCD_TCON3 output signal pin
LCD_TCON2	Output	LCD_TCON2 output signal pin
LCD_TCON1	Output	LCD_TCON1 output signal pin

58. 图形LCD控制器(GLCDC)

多功能图形LCD控制器(GLCDC)支持多种数据格式和面板。关键GLCDC功能包括：

- 用于访问图形数据的GPX总线主控功能
- 三平面叠加（单色背景平面、图形1平面、图形2平面）
- 支持多种类型的32位和16位像素图形数据以及8位、4位和1位LUT数据格式
- 支持WVGA视频图像尺寸的数字接口信号输出。

图58.1显示了GLCDC的框图。

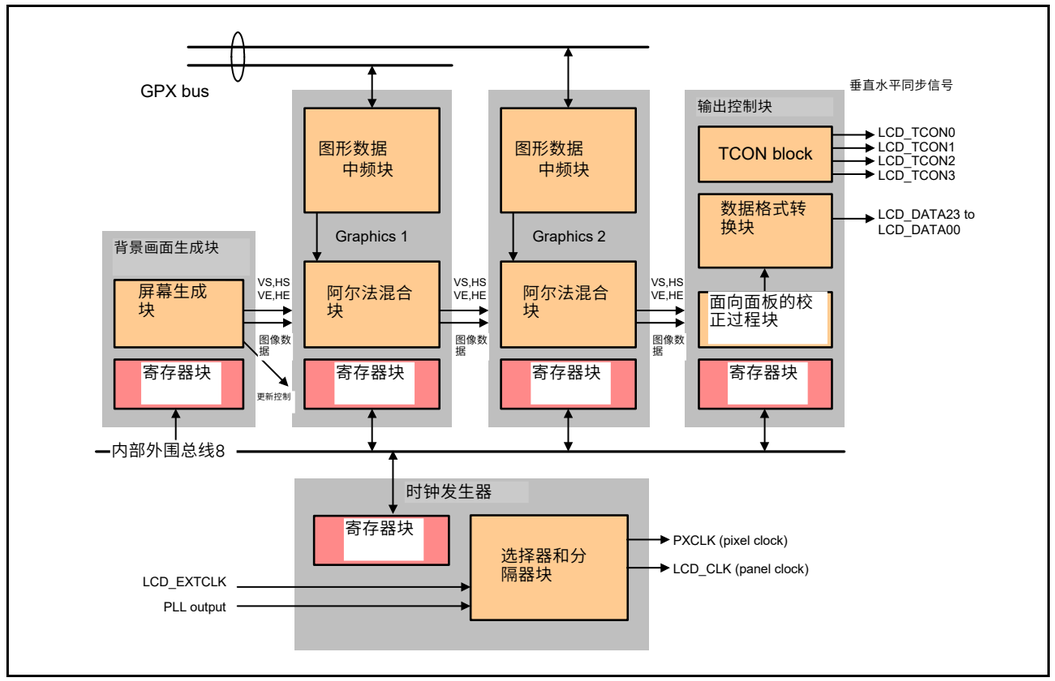


Figure 58.1 GLCDC框图

Note: 使用GLCDC时，将时钟设置为ICLK=PCLKA。

Table 58.1 GLCDCIO引脚（2个中的1个）

引脚名称	I/O	Function
LCD_EXTCLK	Input	面板时钟源输入引脚
LCD_CLK	Output	面板时钟输出引脚
LCD_DATA23 to LCD_DATA00	Output	LCD信号输出引脚 RGB888信号RGB：各8位（无符号）RGB666信号RGB：各6位（无符号） RGB565信号RB：各5位（无符号）G：6位（无符号） 串行RGB信号RGB-：8位（无符号）
LCD_TCON3	Output	LCD_TCON3输出信号引脚
LCD_TCON2	Output	LCD_TCON2输出信号管脚
LCD_TCON1	Output	LCD_TCON1输出信号引脚

Table 58.1 GLCDC I/O pins (2 of 2)

Pin name	I/O	Function
LCD_TCON0	Output	LCD_TCON0 output signal pin

58.1 Functional Overview

Table 58.2 provides a functional overview of GLCDC.

Table 58.2 Functional overview of GLCDC (1 of 2)

Parameter		Function
Graphics	Graphics planes	• Single color background (lowest layer) and two graphics planes • Graphics planes can be alpha-blended with the lower-layer plane
	Pixel format	• RGB-888 progressive format (-: 8 bits, R: 8 bits, G: 8 bits, B: 8 bits; 32 bits in total) • ARGB8888 progressive format (A: 8 bits, R: 8 bits, G: 8 bits, B: 8 bits; 32 bits in total) • RGB565 progressive format (A: None, R: 5 bits, G: 6 bits, B: 5 bits; 16 bits in total) • ARGB1555 progressive format (CLUT: 1 bit, R: 5 bits, G: 5 bits, B: 5 bits; 16 bits in total) • ARGB4444 progressive format (A: 4 bits, R: 4 bits, G: 4 bits, B: 4 bits; 16 bits in total) • CLUT8 progressive format (color palette address: 8 bits) • CLUT4 progressive format (color palette address: 4 bits) • CLUT1 progressive format (color palette address: 1 bit) • CLUT memory: 512 words × 32 bits per graphics plane (ARGB8888)
	Frame buffer control	The following parameters can be set for the frame buffer: • Base address: Start address of the frame buffer, aligned with a 64-byte boundary (burst transfer size) • Macro line offset: Offset address from the start address to the next macro line, aligned with a 64-byte boundary (burst transfer size) • Frame offset: Offset address from the start address to the next frame, aligned with a 64-byte boundary (burst transfer size) • Number of data transfers: Number of data transfers of a macro line • Number of macro lines: Number of macro lines in a single frame
	Alpha blending	• Alpha blending in rectangular area (blending ratio: 256 gradation levels) • Alpha blending in pixel units (blending ratio: 256 gradation levels) • RGB-index chroma key (replaced with the specified color when the object color agrees with the preset value)
Internal video image format		• Total number of vertical lines: Up to 1024 lines • Number of valid vertical lines: 16 to 1020 lines (resolution: 1 line) • Vertical front porch: 2 lines (minimum) • Vertical back porch: 1 line (minimum) • Vertical synchronization (VS) pulse width: 1 line (fixed) • Total number of horizontal pixels: Up to 1024 pixels • Number of valid horizontal pixels: 16 to 1016 pixels (resolution: 2 pixels) • Horizontal front porch: 3 pixels (minimum) • Horizontal back porch: 1 pixel (minimum) • Horizontal synchronization (HS) pulse width: 4 pixels
Data format conversion	Output video image size	• From 16 lines × 16 pixels to 1020 lines × 1016 pixels
	Data format	• RGB888 (parallel 24 bits) • RGB666 (parallel 18 bits) • RGB565 (parallel 16 bits) • RGB888 (serial 8 bits); clock cycle is four times the pixel clock • Bit endian order change and B/R signal swap
	Dither processing	• Reduces 10-bit signals (output after panel-oriented correction) to 8-, 6-, or 5-bit signals (output data format) • Supports the following modes: - Truncate mode - Round-off mode - 2×2 pattern dither mode

Table 58.1 GLCDCIO引脚（2个中的2个）

引脚名称	I/O	Function
LCD_TCON0	Output	LCD_TCON0输出信号引脚

58.1 功能概述

表58.2提供了GLCDC的功能概览。

Table 58.2 GLCDC的功能概述(1of2)

Parameter		Function
Graphics	图形平面	单色背景（最低层）和两个图形平面 图形平面可以与下层平面进行alpha混合
	像素格式	RGB-888逐行格式（-：8位，R：8位，G：8位，B：8位；总共32位） ARGB8888逐行格式（A：8位，R：8位，G：8位，B：8位；共32位）RGB565逐行格式（A：无，R：5位，G：6位，B：5位；共16位）ARGB1555逐行格式（CLUT：1位）R：5位，G：5位，B：5位；共16位） ARGB4444逐行格式（A：4位，R：4位，G：4位，B：4位；共16位)CLUT8逐行格式（调色板地址：8位）CLUT4逐行格式（调色板地址：4位）CLUT1逐行格式（调色板地址：1位）CLUT内存：每个图形平面512字×32位ARGB8888）
	帧缓冲控制	可为帧缓冲区设置以下参数： 基地址：帧缓冲区的起始地址，与64字节边界对齐（突发传输大小） 宏行偏移：从起始地址到下一个宏行的偏移地址，与64字节边界对齐（突发传输大小） 帧偏移：从起始地址到下一帧的偏移地址，与64字节边界对齐（突发传输大小） 数据传输次数：数据传输次数宏行数宏行数：单帧中的宏行数
	阿尔法混合	矩形区域的Alpha混合（混合比：256级） 以像素为单位的Alpha混合（混合比：256级） RGB索引色度键（当对象颜色与预设值一致时替换为指定颜色）
内部视频图像格式		垂直总行数：最多1024行 有效垂直行数：16到1020行（分辨率：1行） 垂直前廊：2行（最少） 垂直后廊：1行（最少） 垂直同步(VS)脉冲宽度：1行（固定） 水平像素总数：最多1024个像素 有效水平像素数：16到1016个像素（分辨率：2个像素） 水平前沿：3个像素（最小） 水平后沿：1像素（最小值） 水平同步(HS)脉冲宽度：4像素
数据格式转换	输出视频图像尺寸	从16行×16像素到1020行×1016像素
	数据格式	RGB888（并行24位） RGB666（并行18位） RGB565（并行16位） RGB888（串行8位）；时钟周期是像素时钟的四倍 位端顺序更改和BR信号交换
	抖动处理	将10位信号（面向面板校正后输出）减少为8位、6位或5位信号（输出数据格式）支持以下模式：截断模式舍入模式2×2模式抖动模式

Table 58.2 Functional overview of GLCDC (2 of 2)

Parameter		Function
Timing control signal	Signal generation	5 timing signals (STVA, STVB, STHA, STHB, and DE) can be generated from HS / VS: • Vertical synchronization signal (variable) • Horizontal synchronization signal (variable) • Data enable signal
	Signal select	• Signals generated by the signal generation circuit can be output from LCD_TCONn pins (n = 0 to 3)
Output control panel-oriented correction processing	Brightness and contrast	• 10-bit internal processing; the sequence of this processing and gamma correction can be swapped. • Brightness: DC value adjustment range: from -512[LSB] to +512[LSB] • Contrast: gain value adjustment range: from 0 to 2 times (from 0/128 to 255/128)
	Gamma correction	• Sixteen areas; input/output: 10 bits • Gain value adjustment range in the area: From 0 to 2 times (from 0/1024 to 2047/1024)
Interrupts		• Number of specified lines interrupt (GLCDC_VPOS) • Graphics 1 buffer underflow interrupt (GLCDC_L1UNDF) • Graphics 2 buffer underflow interrupt (GLCDC_L2UNDF)

58.1.1 GLCDC Configuration

Figure 58.2 shows the configuration of the GLCDC.

The GLCDC includes the following blocks:

- Background screen generation block: Generates the background screen (including the blanking interval), selects the background color, and generates the synchronization signals for controlling the screens.
- Graphics data interface blocks (2 blocks): Convert the graphics data/CLUT data read through the GPX bus into ARGB (8888) data for internal processing, and transfer the clocks (PCLKA → PXCLK).
- Alpha blending blocks (2 blocks): Superimpose graphics data on the lower-layer screen and perform alpha blending based on the register settings and the alpha blending values for the current screen graphics data.
- TCON block: Generates the vertical and horizontal synchronization and enable signals suited for the specifications of the connected panel, from the internal vertical and horizontal synchronization signals.
- Data format conversion block: Processes data into the specific internal RGB888 format into the data of the specific format suited for the specifications of the panel with dither correction for output image data length.
- Panel-oriented correction processing block: Corrects brightness and contrast, and performs gamma correction suited for the characteristics of the connected panel, allowing either brightness and contrast correction or gamma correction to be performed first.
- Clock generator block: Generates the pixel and the panel clocks on a specific frequency from either LCD_EXTCLK or PLL output.

Table 58.2 GLCDC的功能概述(2of2)

Parameter		Function
定时控制信号	信号产生	可以从HSVS生成5个定时信号（STVA、STVB、STHA、STHB和DE）： 垂直同步信号（可变） 水平同步信号（可变） 数据使能信号
	信号选择	信号发生电路产生的信号可以从LCD_TCONn引脚（n=0到3）输出
面向输出控制面板的校正处理	亮度和对比度	10位内部处理；该处理和伽马校正的顺序可以互换。 亮度：DC值调整范围：从-512[LSB]到+512[LSB] 对比度：增益值调整范围：从0到2倍（从0128到255128）
	伽玛校正	十六个领域；输入输出：10位区域内增益值调整范围：从0到2倍（从01024到20471024）
Interrupts		指定行数中断(GLCDC_VPOS) 图形1缓冲区下溢中断(GLCDC_L1UNDF) 图形2缓冲区下溢中断(GLCDC_L2UNDF)

58.1.1 GLCDC Configuration

图58.2显示了GLCDC的配置。

GLCDC包括以下模块：

- 背景画面生成模块：生成背景画面（包括消隐间隔），选择背景颜色，生成控制画面的同步信号。
- 图形数据接口块（2块）：将通过GPX总线读取的图形数据CLUT数据转换成ARGB(8888)数据用于内部处理，并传输时钟(PCLKA→PXCLK)。
- Alphablendingblocks（2个block）：将图形数据叠加到下层屏幕上，根据寄存器设置和当前屏幕图形数据的alphablending值进行alphablending。
- TCON模块：根据内部垂直和水平同步信号，生成适合所连接面板规格的垂直和水平同步和使能信号。
- 数据格式转换块：将内部特定RGB888格式的数据处理成适合面板规格的特定格式的数据，输出图像数据长度的抖动校正。
- 面向面板的校正处理块：校正亮度和对比度，并执行适合所连接面板特性的伽马校正，允许首先进行亮度和对比度校正或伽马校正。
- 时钟发生器模块：从LCD_EXTCLK或PLL输出以特定频率生成像素和面板时钟。

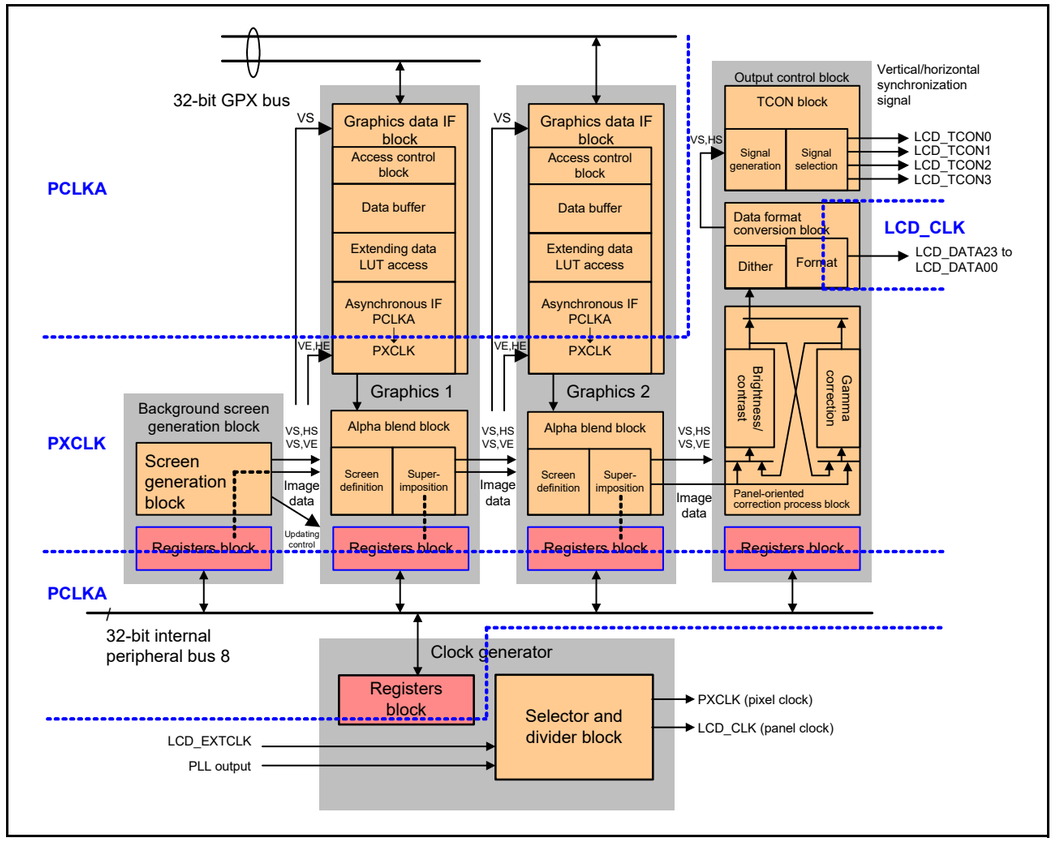


Figure 58.2 GLCDC configuration

58.1.2 Screen Format

Figure 58.3 shows the screen format overview of the GLCDC.

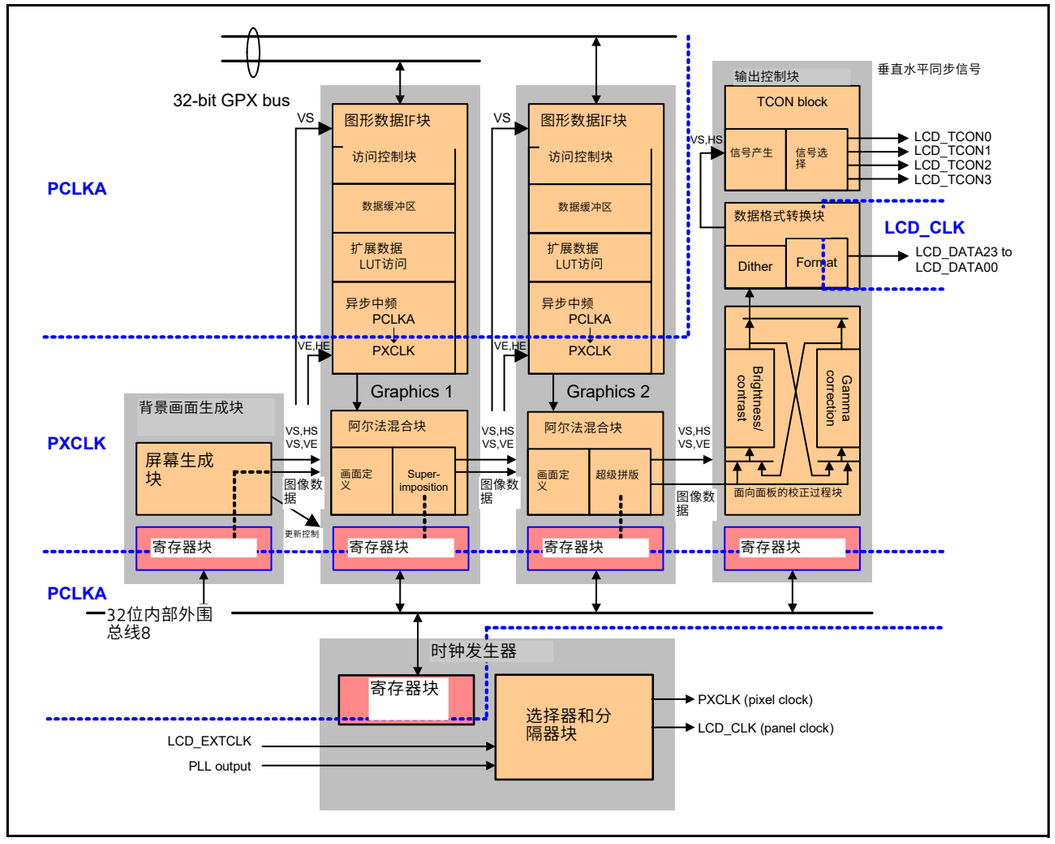


Figure 58.2 GLCDC configuration

58.1.2 屏幕格式

图58.3显示了GLCDC的屏幕格式概览。

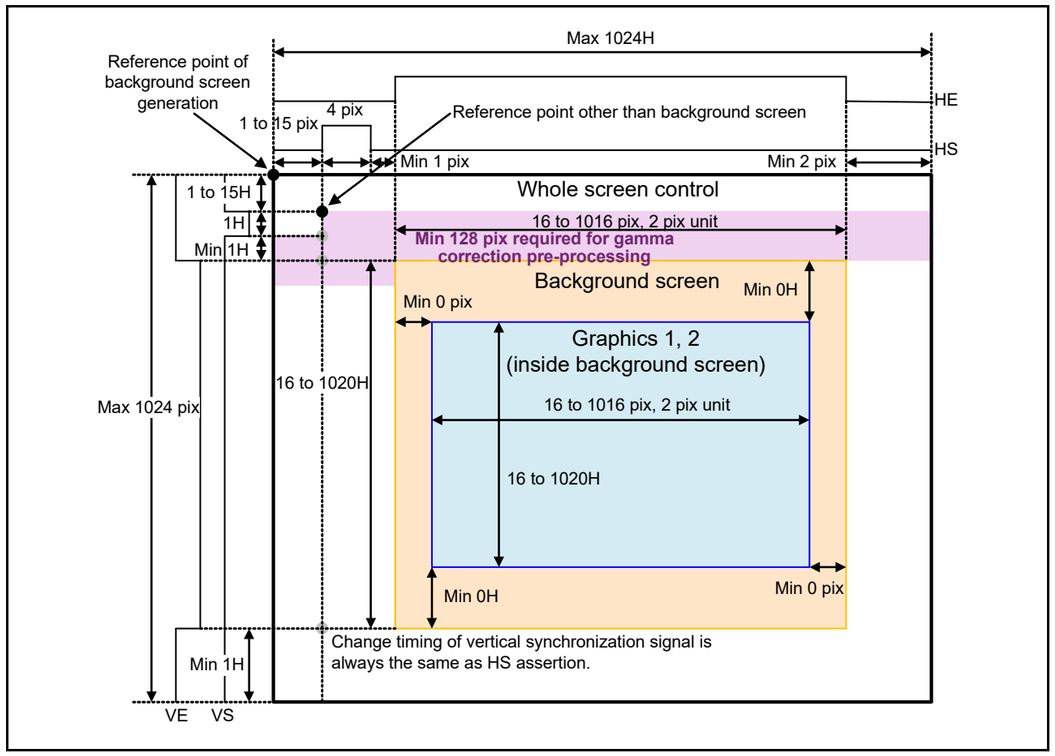


Figure 58.3 Internal screen format

The background screen generation block generates the essential timing signals for operations in the module as a whole. The graphics data interface blocks, alpha blending blocks, gamma correction block, output control block, and TCON block operate based on the synchronization and enable signals, which are sequentially transferred from the background screen generation block.

58.1.3 Graphics and Color Palette (CLUT) Data Formats

The GLCDC handles three display screens, one of which is a background screen. For the background screen, frame data is RGB888 graphics data stored in the registers, and for the other two screens, frame data is stored in the memory connected to the GPX bus as 32- or 16-bit/pixel graphics data or 8-, 4-, or 1-bit/pixel color palette (CLUT) data. The frame data of the relevant screen is read by the graphics data interface block, read into the GLCDC, and extended (converted) into ARGB8888 data for superimposition and blending. Figure 58.4 shows the frame data formats.

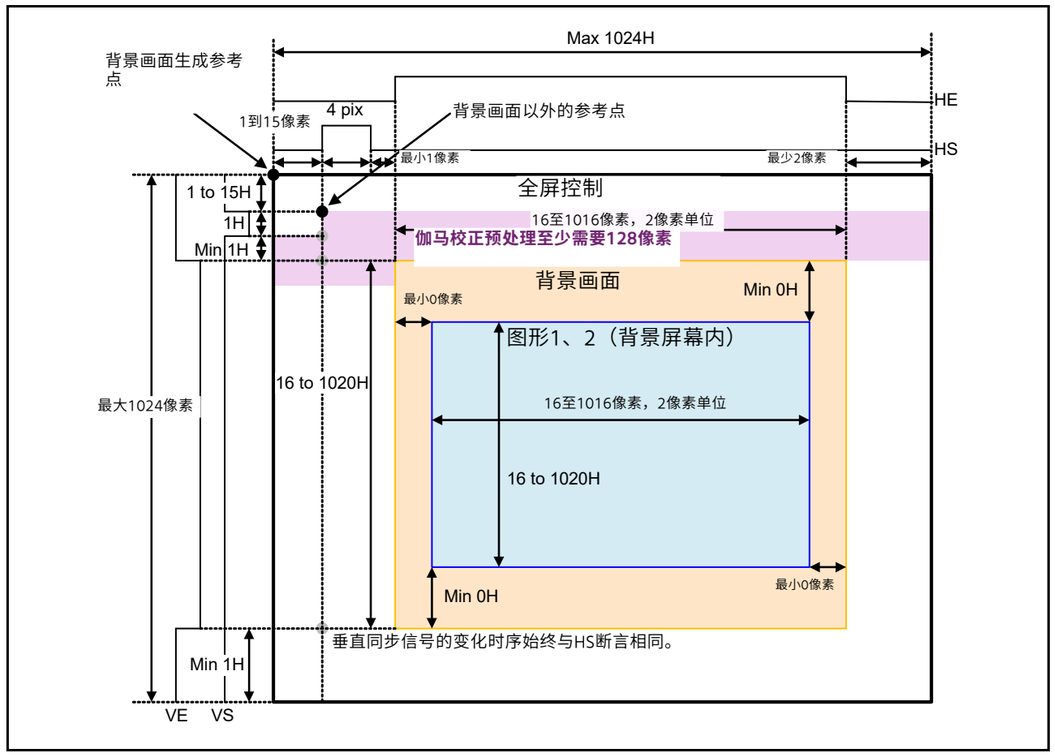


Figure 58.3 内部屏幕格式

背景屏幕生成块为整个模块中的操作生成必要的时序信号。图形数据接口块、阿尔法混合块、伽马校正块、输出控制块和TCON块基于从背景屏幕生成块顺序传输的同步和使能信号进行操作。

58.1.3 图形和调色板(CLUT)数据格式

GLCDC处理三个显示屏幕，其中一个是背景屏幕。对于背景屏幕，帧数据是存储在寄存器中的RGB888图形数据，而对于其他两个屏幕，帧数据作为32位或16位像素图形数据或8-、4-、或1位像素调色板(CLUT)数据。相关画面的帧数据 由图形数据接口块读取，读入GLCDC，扩展（转换）为ARGB8888数据进行叠加混合。图58.4显示了帧数据格式。

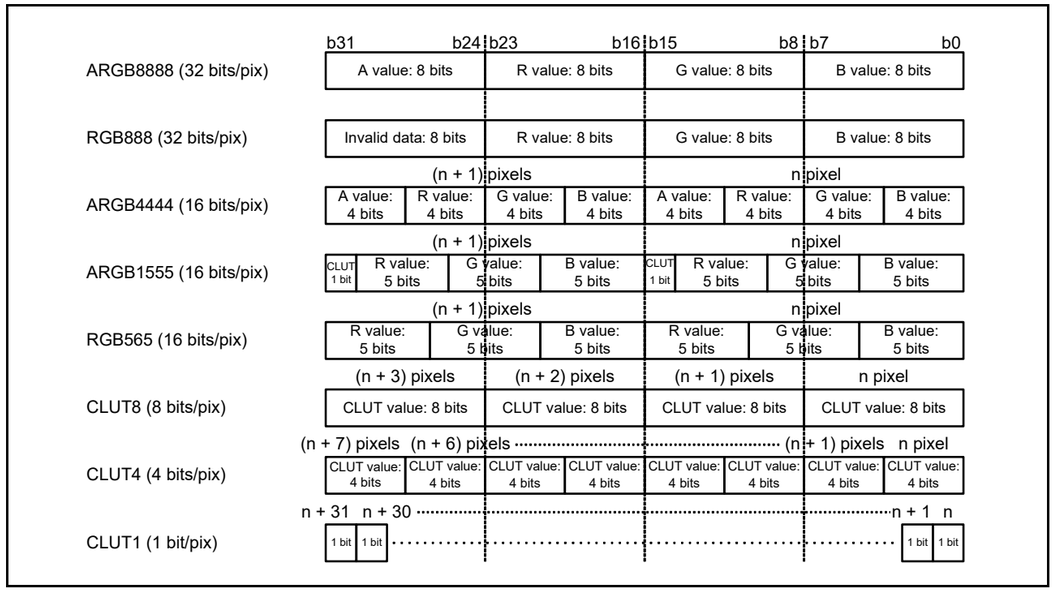


Figure 58.4 Frame data format

The A value (alpha blending value) represents the blending ratio of pixel data for displaying the lower-layer and current graphics screens after superimposition. The blending process is performed in accordance with the equations given in section 58.1.7, Graphics Data Interface. The CLUT value represents the color palette memory address (plane 0 or 1 is selected in the registers), and the data in the color palette is ARGB8888 (32 bits/pixel) graphics data. Addresses 01h/00h are accessed with CLUT1, 0Fh to 00h with CLUT4, and FFh to 00h with CLUT8. Addresses 80h/00h are accessed with ARGB1555 data.

58.1.4 Output Control for Data Format

The GLCDC can output data in accordance with the following formats and register settings:

- Data formats
  - Parallel: RGB888, RGB666, and RGB565
  - Serial: RGB888
  - Lower bits are processed in one of the following modes when 10-bit signals are reduced to 8-, 6-, and 5- bit signals:
    - — Truncate mode
    - — Round-off mode
    - — 2×2 pattern dither processing + truncate mode.
- Pixel arrangement
  - RGB
  - BGR.
- Scan direction select for serial RGB888
  - Forward scan
  - Reverse scan.
- Data output delay of serial RGB888

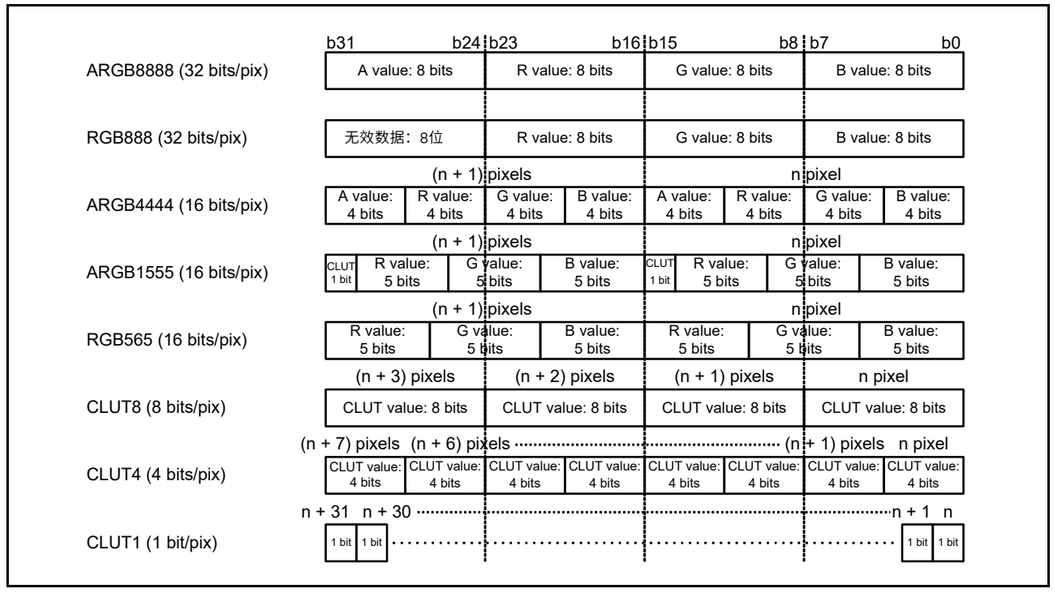


Figure 58.4 帧数据格式

A值(alphablendingvalue)表示叠加后显示下层和当前图形画面的像素数据的混合比例。根据第58.1.7节"图形数据接口"中给出的公式执行混合过程。CLUT值代表调色板内存地址（寄存器中选择平面0或1），调色板中的数据为ARGB8888（32位像素）图形数据。使用CLUT1访问地址01h00h，使用CLUT4访问地址0Fh到00h，使用CLUT8访问FFh到00h。使用ARGB1555数据访问地址80h00h。

58.1.4 数据格式的输出控制

GLCDC可以按照以下格式和寄存器设置输出数据：

- 数据格式
  - Parallel: RGB888, RGB666, and RGB565
  - Serial: RGB888
  - 当10位信号缩减为8位、6位和5位信号时，低位将按以下模式之一进行处理：
    - — Truncate mode
    - — Round-off mode
    - —2×2模式抖动处理+截断模式。
- 像素排列
  - RGB
  - BGR.
- 串行RGB888的扫描方向选择
  - 前向扫描
  - 反向扫描。
- 串口RGB888的数据输出延迟

- 0 to 3 clock cycles.

- Pin assignment.
  - Little endian
  - Big endian.

For details on dither processing, see section 58.2.48, Output Control Block Panel Dither Correction Register (OUT_PDTHA).

Bit assignment of LCD signals for parallel RGB888 format

Table 58.3 shows RGB signal inputs assigned to the LCD signal outputs for the parallel RGB888 output format.

Table 58.3 Bit assignment of RGB signal inputs for parallel RGB888 format

Pin assignment	Pixel arrangement			
	RGB, little endian	RGB, big endian	BGR, little endian	BGR, big endian
LCD_DATA23	R[7]	R[0]	B[7]	B[0]
LCD_DATA22	R[6]	R[1]	B[6]	B[1]
LCD_DATA21	R[5]	R[2]	B[5]	B[2]
LCD_DATA20	R[4]	R[3]	B[4]	B[3]
LCD_DATA19	R[3]	R[4]	B[3]	B[4]
LCD_DATA18	R[2]	R[5]	B[2]	B[5]
LCD_DATA17	R[1]	R[6]	B[1]	B[6]
LCD_DATA16	R[0]	R[7]	B[0]	B[7]
LCD_DATA15	G[7]	G[0]	G[7]	G[0]
LCD_DATA14	G[6]	G[1]	G[6]	G[1]
LCD_DATA13	G[5]	G[2]	G[5]	G[2]
LCD_DATA12	G[4]	G[3]	G[4]	G[3]
LCD_DATA11	G[3]	G[4]	G[3]	G[4]
LCD_DATA10	G[2]	G[5]	G[2]	G[5]
LCD_DATA09	G[1]	G[6]	G[1]	G[6]
LCD_DATA08	G[0]	G[7]	G[0]	G[7]
LCD_DATA07	B[7]	B[0]	R[7]	R[0]
LCD_DATA06	B[6]	B[1]	R[6]	R[1]
LCD_DATA05	B[5]	B[2]	R[5]	R[2]
LCD_DATA04	B[4]	B[3]	R[4]	R[3]
LCD_DATA03	B[3]	B[4]	R[3]	R[4]
LCD_DATA02	B[2]	B[5]	R[2]	R[5]
LCD_DATA01	B[1]	B[6]	R[1]	R[6]
LCD_DATA00	B[0]	B[7]	R[0]	R[7]

Note: R[7:0], G[7:0], and B[7:0] are RGB pixel data that is internally processed.

Bit assignment of LCD signals for parallel RGB666 format

Table 58.4 shows RGB signal inputs assigned to the LCD signal outputs for the parallel RGB666 output format.

Table 58.4 Bit assignment of RGB signal inputs for parallel RGB666 format (1 of 2)

Pin assignment	Pixel arrangement			
	RGB, little endian	RGB, big endian	BGR, little endian	BGR, big endian
LCD_DATA23	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0

- 0到3个时钟周期。

- 引脚分配。
  - Little endian
  - Big endian.

有关抖动处理的详细信息，请参阅第58.2.48节，输出控制块面板抖动校正寄存器(OUT_PDTHA)。

并行RGB888格式的LCD信号的位分配

表58.3显示了分配给并行RGB888输出格式的LCD信号输出的RGB信号输入。

Table 58.3 并行RGB888格式的RGB信号输入的位分配

引脚分配	像素排列			
	RGB, little endian	RGB, big endian	BGR, little endian	BGR, big endian
LCD_DATA23	R[7]	R[0]	B[7]	B[0]
LCD_DATA22	R[6]	R[1]	B[6]	B[1]
LCD_DATA21	R[5]	R[2]	B[5]	B[2]
LCD_DATA20	R[4]	R[3]	B[4]	B[3]
LCD_DATA19	R[3]	R[4]	B[3]	B[4]
LCD_DATA18	R[2]	R[5]	B[2]	B[5]
LCD_DATA17	R[1]	R[6]	B[1]	B[6]
LCD_DATA16	R[0]	R[7]	B[0]	B[7]
LCD_DATA15	G[7]	G[0]	G[7]	G[0]
LCD_DATA14	G[6]	G[1]	G[6]	G[1]
LCD_DATA13	G[5]	G[2]	G[5]	G[2]
LCD_DATA12	G[4]	G[3]	G[4]	G[3]
LCD_DATA11	G[3]	G[4]	G[3]	G[4]
LCD_DATA10	G[2]	G[5]	G[2]	G[5]
LCD_DATA09	G[1]	G[6]	G[1]	G[6]
LCD_DATA08	G[0]	G[7]	G[0]	G[7]
LCD_DATA07	B[7]	B[0]	R[7]	R[0]
LCD_DATA06	B[6]	B[1]	R[6]	R[1]
LCD_DATA05	B[5]	B[2]	R[5]	R[2]
LCD_DATA04	B[4]	B[3]	R[4]	R[3]
LCD_DATA03	B[3]	B[4]	R[3]	R[4]
LCD_DATA02	B[2]	B[5]	R[2]	R[5]
LCD_DATA01	B[1]	B[6]	R[1]	R[6]
LCD_DATA00	B[0]	B[7]	R[0]	R[7]

Note: R[7:0]、G[7:0]和B[7:0]是内部处理的RGB像素数据。

并行RGB666格式的LCD信号的位分配

表58.4显示了分配给并行RGB666输出格式的LCD信号输出的RGB信号输入。

Table 58.4 并行RGB666格式的RGB信号输入的位分配（1of2）

引脚分配	像素排列			
	RGB, little endian	RGB, big endian	BGR, little endian	BGR, big endian
LCD_DATA23	固定为0	固定为0	固定为0	固定为0

Table 58.4 Bit assignment of RGB signal inputs for parallel RGB666 format (2 of 2)

Pin assignment	Pixel arrangement			
	RGB, little endian	RGB, big endian	BGR, little endian	BGR, big endian
LCD_DATA22	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0
LCD_DATA21	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0
LCD_DATA20	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0
LCD_DATA19	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0
LCD_DATA18	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0
LCD_DATA17	R[7]	R[2]	B[7]	B[2]
LCD_DATA16	R[6]	R[3]	B[6]	B[3]
LCD_DATA15	R[5]	R[4]	B[5]	B[4]
LCD_DATA14	R[4]	R[5]	B[4]	B[5]
LCD_DATA13	R[3]	R[6]	B[3]	B[6]
LCD_DATA12	R[2]	R[7]	B[2]	B[7]
LCD_DATA11	G[7]	G[2]	G[7]	G[2]
LCD_DATA10	G[6]	G[3]	G[6]	G[3]
LCD_DATA09	G[5]	G[4]	G[5]	G[4]
LCD_DATA08	G[4]	G[5]	G[4]	G[5]
LCD_DATA07	G[3]	G[6]	G[3]	G[6]
LCD_DATA06	G[2]	G[7]	G[2]	G[7]
LCD_DATA05	B[7]	B[2]	R[7]	R[2]
LCD_DATA04	B[6]	B[3]	R[6]	R[3]
LCD_DATA03	B[5]	B[4]	R[5]	R[4]
LCD_DATA02	B[4]	B[5]	R[4]	R[5]
LCD_DATA01	B[3]	B[6]	R[3]	R[6]
LCD_DATA00	B[2]	B[7]	R[2]	R[7]

Note: R[7:2], G[7:2], and B[7:2] are RGB pixel data that is internally processed.

Bit assignment of LCD signals for parallel RGB565 format

Table 58.5 shows RGB signal inputs assigned to the LCD signal outputs for the parallel RGB565 output format.

Table 58.5 Bit assignment of RGB signal inputs for parallel RGB565 format (1 of 2)

Pin assignment	Pixel arrangement			
	RGB, little endian	RGB, big endian	BGR, little endian	BGR, big endian
LCD_DATA23	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0
LCD_DATA22	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0
LCD_DATA21	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0
LCD_DATA20	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0
LCD_DATA19	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0
LCD_DATA18	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0
LCD_DATA17	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0
LCD_DATA16	Fixed to 0	Fixed to 0	Fixed to 0	Fixed to 0
LCD_DATA15	R[7]	R[3]	B[7]	B[3]
LCD_DATA14	R[6]	R[4]	B[6]	B[4]
LCD_DATA13	R[5]	R[5]	B[5]	B[5]
LCD_DATA12	R[4]	R[6]	B[4]	B[6]
LCD_DATA11	R[3]	R[7]	B[3]	B[7]

Table 58.4 并行RGB666格式的RGB信号输入的位分配（2个中的2个）

引脚分配	像素排列			
	RGB, little endian	RGB, big endian	BGR, little endian	BGR, big endian
LCD_DATA22	固定为0	固定为0	固定为0	固定为0
LCD_DATA21	固定为0	固定为0	固定为0	固定为0
LCD_DATA20	固定为0	固定为0	固定为0	固定为0
LCD_DATA19	固定为0	固定为0	固定为0	固定为0
LCD_DATA18	固定为0	固定为0	固定为0	固定为0
LCD_DATA17	R[7]	R[2]	B[7]	B[2]
LCD_DATA16	R[6]	R[3]	B[6]	B[3]
LCD_DATA15	R[5]	R[4]	B[5]	B[4]
LCD_DATA14	R[4]	R[5]	B[4]	B[5]
LCD_DATA13	R[3]	R[6]	B[3]	B[6]
LCD_DATA12	R[2]	R[7]	B[2]	B[7]
LCD_DATA11	G[7]	G[2]	G[7]	G[2]
LCD_DATA10	G[6]	G[3]	G[6]	G[3]
LCD_DATA09	G[5]	G[4]	G[5]	G[4]
LCD_DATA08	G[4]	G[5]	G[4]	G[5]
LCD_DATA07	G[3]	G[6]	G[3]	G[6]
LCD_DATA06	G[2]	G[7]	G[2]	G[7]
LCD_DATA05	B[7]	B[2]	R[7]	R[2]
LCD_DATA04	B[6]	B[3]	R[6]	R[3]
LCD_DATA03	B[5]	B[4]	R[5]	R[4]
LCD_DATA02	B[4]	B[5]	R[4]	R[5]
LCD_DATA01	B[3]	B[6]	R[3]	R[6]
LCD_DATA00	B[2]	B[7]	R[2]	R[7]

Note: R[7:2]、G[7:2]和B[7:2]是内部处理的RGB像素数据。

并行RGB565格式的LCD信号的位分配

表58.5显示了分配给并行RGB565输出格式的LCD信号输出的RGB信号输入。

Table 58.5 并行RGB565格式的RGB信号输入的位分配（1of2）

引脚分配	像素排列			
	RGB, little endian	RGB, big endian	BGR, little endian	BGR, big endian
LCD_DATA23	固定为0	固定为0	固定为0	固定为0
LCD_DATA22	固定为0	固定为0	固定为0	固定为0
LCD_DATA21	固定为0	固定为0	固定为0	固定为0
LCD_DATA20	固定为0	固定为0	固定为0	固定为0
LCD_DATA19	固定为0	固定为0	固定为0	固定为0
LCD_DATA18	固定为0	固定为0	固定为0	固定为0
LCD_DATA17	固定为0	固定为0	固定为0	固定为0
LCD_DATA16	固定为0	固定为0	固定为0	固定为0
LCD_DATA15	R[7]	R[3]	B[7]	B[3]
LCD_DATA14	R[6]	R[4]	B[6]	B[4]
LCD_DATA13	R[5]	R[5]	B[5]	B[5]
LCD_DATA12	R[4]	R[6]	B[4]	B[6]
LCD_DATA11	R[3]	R[7]	B[3]	B[7]

Table 58.5 Bit assignment of RGB signal inputs for parallel RGB565 format (2 of 2)

Pin assignment	Pixel arrangement			
	RGB, little endian	RGB, big endian	BGR, little endian	BGR, big endian
LCD_DATA10	G[7]	G[2]	G[7]	G[2]
LCD_DATA09	G[6]	G[3]	G[6]	G[3]
LCD_DATA08	G[5]	G[4]	G[5]	G[4]
LCD_DATA07	G[4]	G[5]	G[4]	G[5]
LCD_DATA06	G[3]	G[6]	G[3]	G[6]
LCD_DATA05	G[2]	G[7]	G[2]	G[7]
LCD_DATA04	B[7]	B[3]	R[7]	R[3]
LCD_DATA03	B[6]	B[4]	R[6]	R[4]
LCD_DATA02	B[5]	B[5]	R[5]	R[5]
LCD_DATA01	B[4]	B[6]	R[4]	R[6]
LCD_DATA00	B[3]	B[7]	R[3]	R[7]

Note: R[7:3], G[7:2], and B[7:3] are RGB pixel data that is internally processed.

Bit assignment of RGB signal inputs for serial RGB888 format

Table 58.6 and Table 58.7 show RGB signal inputs assigned to the LCD signal outputs for the serial RGB888 output format.

Table 58.6 Bit assignment of RGB signal inputs for serial RGB888 format, RGB arrangement

Pin assignment	Pixel arrangement, scan direction select, and cycle															
	RGB, little endian								RGB, big endian							
	Reverse scan				Forward scan				Reverse scan				Forward scan			
	1st	2nd	3rd	4th	1st	2nd	3rd	4th	1st	2nd	3rd	4th	1st	2nd	3rd	4th
LCD_DATA23	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
⋮	⋮				⋮				⋮				⋮			
LCD_DATA08	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
LCD_DATA07	Undefined	B[7]	G[7]	R[7]	R[7]	G[7]	B[7]	Undefined	Undefined	B[0]	G[0]	R[0]	R[0]	G[0]	B[0]	Undefined
LCD_DATA06	Undefined	B[6]	G[6]	R[6]	R[6]	G[6]	B[6]	Undefined	Undefined	B[1]	G[1]	R[1]	R[1]	G[1]	B[1]	Undefined
LCD_DATA05	Undefined	B[5]	GI5]	R[5]	R[5]	GI5]	B[5]	Undefined	Undefined	B[2]	G[2]	R[2]	R[2]	G[2]	B[2]	Undefined
LCD_DATA04	Undefined	B[4]	G[4]	R[4]	R[4]	G[4]	B[4]	Undefined	Undefined	B[3]	G[3]	R[3]	R[3]	G[3]	B[3]	Undefined
LCD_DATA03	Undefined	B[3]	G[3]	R[3]	R[3]	G[3]	B[3]	Undefined	Undefined	B[4]	G[4]	R[4]	R[4]	G[4]	B[4]	Undefined
LCD_DATA02	Undefined	B[2]	G[2]	R[2]	R[2]	G[2]	B[2]	Undefined	Undefined	B[5]	G[5]	R[5]	R[5]	G[5]	B[5]	Undefined
LCD_DATA01	Undefined	B[1]	G[1]	R[1]	R[1]	G[1]	B[1]	Undefined	Undefined	B[6]	G[6]	R[6]	R[6]	G[6]	B[6]	Undefined
LCD_DATA00	Undefined	B[0]	G[0]	R[0]	R[0]	G[0]	B[0]	Undefined	Undefined	B[7]	G[7]	R[7]	R[7]	G[7]	B[7]	Undefined

Note: R[7:0], G[7:0], and B[7:0] are RGB pixel data that is internally processed.

Table 58.5 并行RGB565格式的RGB信号输入的位分配(2of2)

引脚分配	像素排列			
	RGB, little endian	RGB, big endian	BGR, little endian	BGR, big endian
LCD_DATA10	G[7]	G[2]	G[7]	G[2]
LCD_DATA09	G[6]	G[3]	G[6]	G[3]
LCD_DATA08	G[5]	G[4]	G[5]	G[4]
LCD_DATA07	G[4]	G[5]	G[4]	G[5]
LCD_DATA06	G[3]	G[6]	G[3]	G[6]
LCD_DATA05	G[2]	G[7]	G[2]	G[7]
LCD_DATA04	B[7]	B[3]	R[7]	R[3]
LCD_DATA03	B[6]	B[4]	R[6]	R[4]
LCD_DATA02	B[5]	B[5]	R[5]	R[5]
LCD_DATA01	B[4]	B[6]	R[4]	R[6]
LCD_DATA00	B[3]	B[7]	R[3]	R[7]

Note: R[7:3]、G[7:2]和B[7:3]是内部处理的RGB像素数据。

串行RGB888格式的RGB信号输入的位分配

表58.6和表58.7显示了分配给串行RGB888输出格式的LCD信号输出的RGB信号输入。

Table 58.6 用于串行RGB888格式、RGB排列的RGB信号输入的位分配

引脚分配	像素排列、扫描方向选择和循环															
	RGB, little endian								RGB, big endian							
	反向扫描				前向扫描				反向扫描				前向扫描			
	1st	2nd	3rd	4th	1st	2nd	3rd	4th	1st	2nd	3rd	4th	1st	2nd	3rd	4th
LCD_DATA23	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
⋮	⋮				⋮				⋮				⋮			
LCD_DATA08	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
LCD_DATA07	Undefined	B[7]	G[7]	R[7]	R[7]	G[7]	B[7]	Undefined	Undefined	B[0]	G[0]	R[0]	R[0]	G[0]	B[0]	Undefined
LCD_DATA06	Undefined	B[6]	G[6]	R[6]	R[6]	G[6]	B[6]	Undefined	Undefined	B[1]	G[1]	R[1]	R[1]	G[1]	B[1]	Undefined
LCD_DATA05	Undefined	B[5]	GI5]	R[5]	R[5]	GI5]	B[5]	Undefined	Undefined	B[2]	G[2]	R[2]	R[2]	G[2]	B[2]	Undefined
LCD_DATA04	Undefined	B[4]	G[4]	R[4]	R[4]	G[4]	B[4]	Undefined	Undefined	B[3]	G[3]	R[3]	R[3]	G[3]	B[3]	Undefined
LCD_DATA03	Undefined	B[3]	G[3]	R[3]	R[3]	G[3]	B[3]	Undefined	Undefined	B[4]	G[4]	R[4]	R[4]	G[4]	B[4]	Undefined
LCD_DATA02	Undefined	B[2]	G[2]	R[2]	R[2]	G[2]	B[2]	Undefined	Undefined	B[5]	G[5]	R[5]	R[5]	G[5]	B[5]	Undefined
LCD_DATA01	Undefined	B[1]	G[1]	R[1]	R[1]	G[1]	B[1]	Undefined	Undefined	B[6]	G[6]	R[6]	R[6]	G[6]	B[6]	Undefined
LCD_DATA00	Undefined	B[0]	G[0]	R[0]	R[0]	G[0]	B[0]	Undefined	Undefined	B[7]	G[7]	R[7]	R[7]	G[7]	B[7]	Undefined

Note: R[7:0]、G[7:0]和B[7:0]是内部处理的RGB像素数据。

Table 58.7 Bit assignment of RGB signal inputs for serial RGB888 format, BGR arrangement

Pin assignment	Pixel arrangement, scan direction select, and cycle															
	BGR, little endian								BGR, big endian							
	Reverse scan				Forward scan				Reverse scan				Forward scan			
	1st	2nd	3rd	4th	1st	2nd	3rd	4th	1st	2nd	3rd	4th	1st	2nd	3rd	4th
LCD_DATA23	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
⋮	⋮				⋮				⋮				⋮			
LCD_DATA08	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
LCD_DATA07	Undefined	R[7]	G[7]	B[7]	B[7]	G[7]	R[7]	Undefined	Undefined	R[0]	G[0]	B[0]	B[0]	G[0]	R[0]	Undefined
LCD_DATA06	Undefined	R[6]	G[6]	B[6]	B[6]	G[6]	R[6]	Undefined	Undefined	R[1]	G[1]	B[1]	B[1]	G[1]	R[1]	Undefined
LCD_DATA05	Undefined	R[5]	GI5]	B[5]	B[5]	GI5]	R[5]	Undefined	Undefined	R[2]	G[2]	B[2]	B[2]	G[2]	R[2]	Undefined
LCD_DATA04	Undefined	R[4]	G[4]	B[4]	B[4]	G[4]	R[4]	Undefined	Undefined	R[3]	G[3]	B[3]	B[3]	G[3]	R[3]	Undefined
LCD_DATA03	Undefined	R[3]	G[3]	B[3]	B[3]	G[3]	R[3]	Undefined	Undefined	R[4]	G[4]	B[4]	B[4]	G[4]	R[4]	Undefined
LCD_DATA02	Undefined	R[2]	G[2]	B[2]	B[2]	G[2]	R[2]	Undefined	Undefined	R[5]	G[5]	B[5]	B[5]	G[5]	R[5]	Undefined
LCD_DATA01	Undefined	R[1]	G[1]	B[1]	B[1]	G[1]	R[1]	Undefined	Undefined	R[6]	G[6]	B[6]	B[6]	G[6]	R[6]	Undefined
LCD_DATA00	Undefined	R[0]	G[0]	B[0]	B[0]	G[0]	R[0]	Undefined	Undefined	R[7]	G[7]	B[7]	B[7]	G[7]	R[7]	Undefined

Note: R[7:0], G[7:0], and B[7:0] are RGB pixel data that is internally processed.

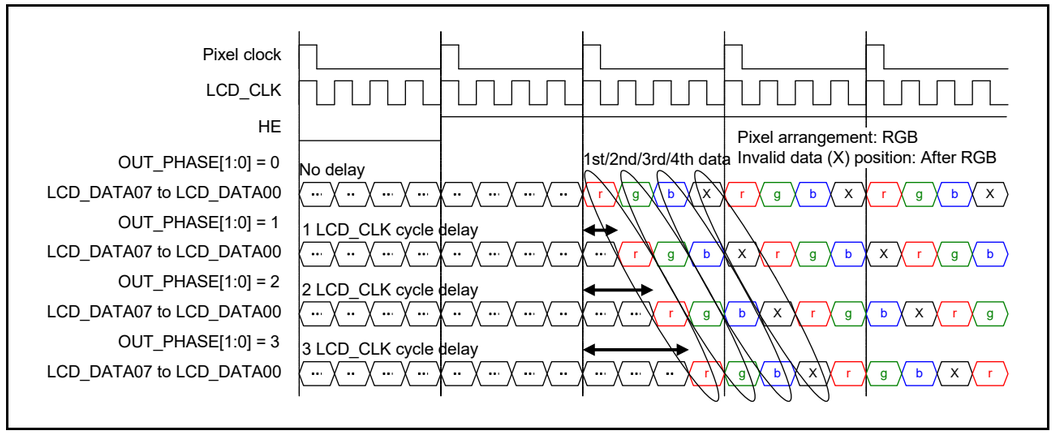


Figure 58.5 Serial RGB888 (4x speed) output timing

58.1.5 Output Control for Panel-Oriented Correction Process

The following panel-oriented correction processes are provided:

- Brightness correction
- Contrast correction
- RGB gamma correction.

Brightness correction always precedes contrast correction, but RGB gamma correction can either precede or follow brightness and contrast correction, based on the register settings. In panel-oriented correction, 10-bit RGB data obtained by extending 8-bit RGB data output from graphics 2 is used, and 10-bit RGB data is also output to the output control (data format conversion) block. Figure 58.6 shows the configuration of the panel-oriented correction circuit.

Table 58.7 用于串行RGB888格式、BGR排列的RGB信号输入的位分配

引脚分配	像素排列、扫描方向选择和循环															
	BGR, little endian								BGR, big endian							
	反向扫描				前向扫描				反向扫描				前向扫描			
	1st	2nd	3rd	4th	1st	2nd	3rd	4th	1st	2nd	3rd	4th	1st	2nd	3rd	4th
LCD_DATA23	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
⋮	⋮				⋮				⋮				⋮			
LCD_DATA08	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
LCD_DATA07	Undefined	R[7]	G[7]	B[7]	B[7]	G[7]	R[7]	Undefined	Undefined	R[0]	G[0]	B[0]	B[0]	G[0]	R[0]	Undefined
LCD_DATA06	Undefined	R[6]	G[6]	B[6]	B[6]	G[6]	R[6]	Undefined	Undefined	R[1]	G[1]	B[1]	B[1]	G[1]	R[1]	Undefined
LCD_DATA05	Undefined	R[5]	GI5]	B[5]	B[5]	GI5]	R[5]	Undefined	Undefined	R[2]	G[2]	B[2]	B[2]	G[2]	R[2]	Undefined
LCD_DATA04	Undefined	R[4]	G[4]	B[4]	B[4]	G[4]	R[4]	Undefined	Undefined	R[3]	G[3]	B[3]	B[3]	G[3]	R[3]	Undefined
LCD_DATA03	Undefined	R[3]	G[3]	B[3]	B[3]	G[3]	R[3]	Undefined	Undefined	R[4]	G[4]	B[4]	B[4]	G[4]	R[4]	Undefined
LCD_DATA02	Undefined	R[2]	G[2]	B[2]	B[2]	G[2]	R[2]	Undefined	Undefined	R[5]	G[5]	B[5]	B[5]	G[5]	R[5]	Undefined
LCD_DATA01	Undefined	R[1]	G[1]	B[1]	B[1]	G[1]	R[1]	Undefined	Undefined	R[6]	G[6]	B[6]	B[6]	G[6]	R[6]	Undefined
LCD_DATA00	Undefined	R[0]	G[0]	B[0]	B[0]	G[0]	R[0]	Undefined	Undefined	R[7]	G[7]	B[7]	B[7]	G[7]	R[7]	Undefined

Note: R[7:0]、G[7:0]和B[7:0]是内部处理的RGB像素数据。

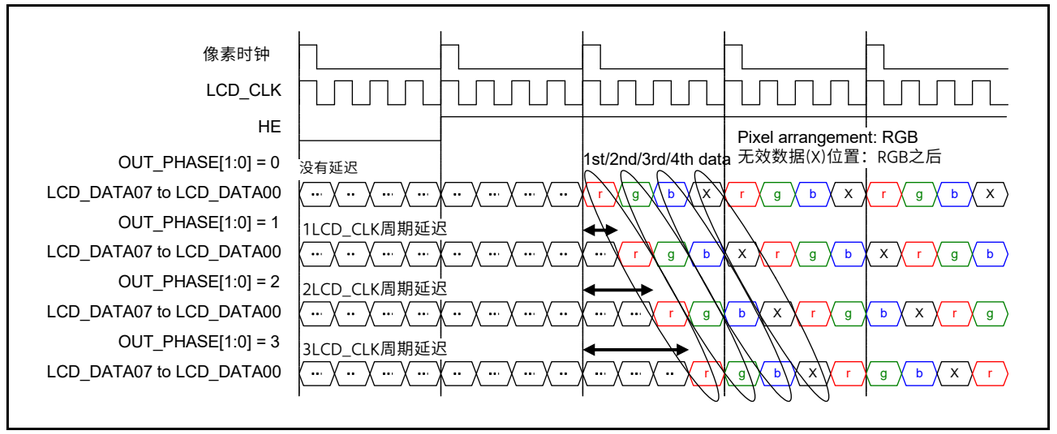


Figure 58.5 串行RGB888（4倍速）输出时序

58.1.5 面向面板的校正过程的输出控制

提供以下面向面板的校正过程：

- 亮度校正
- 对比度校正
- RGB伽马校正。

亮度校正始终先于对比度校正，但RGB伽马校正可以根据寄存器设置在亮度和对比度校正之前或之后进行。在面向面板的校正中，使用通过扩展从图形2输出的8位RGB数据获得的10位RGB数据，并且10位RGB数据也被输出到输出控制（数据格式转换）块。图58.6显示了面向面板的校正电路的配置。

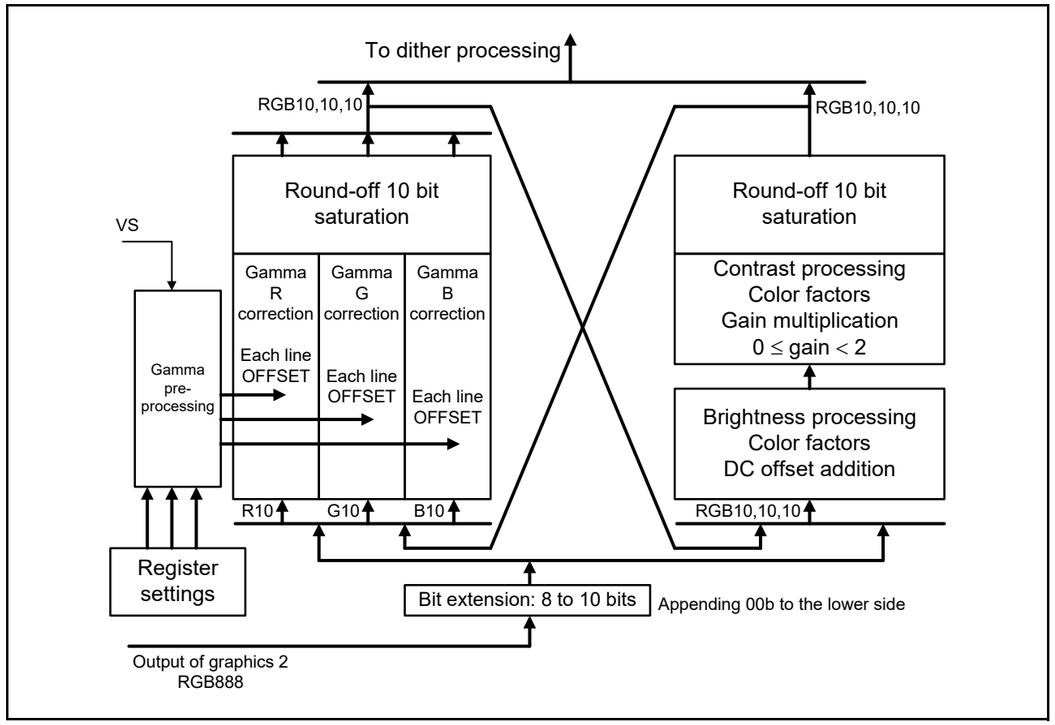


Figure 58.6 Configuration of panel-oriented correction circuit

58.1.6 Output Control for TCON

Any of the four signals generated from the internal vertical and horizontal synchronization signals (STVA, STVB, STHA, and STHB) that have passed through the data format conversion block can be selected for output on four pins, LCD_TCON0, LCD_TCON1, LCD_TCON2, and LCD_TCON3. The generated signals are completely independent of the image data. They are not affected by the output image format or any internal data process, and no register settings for signal generation affect the output image format or any internal data process. The data enable signal DE, which is to be generated by the TCON block, is the logical AND of the two signals STVB and STHB, which were previously generated by the TCON block. Consequently, three signals in total can actually be generated if DE is to be output.

58.1.7 Graphics Data Interface

Two circuit systems are provided for reading graphics data (graphics 1 and 2), each of which incorporates an access control block, data buffer, CLUT memory, data extension block, and asynchronous interface block.

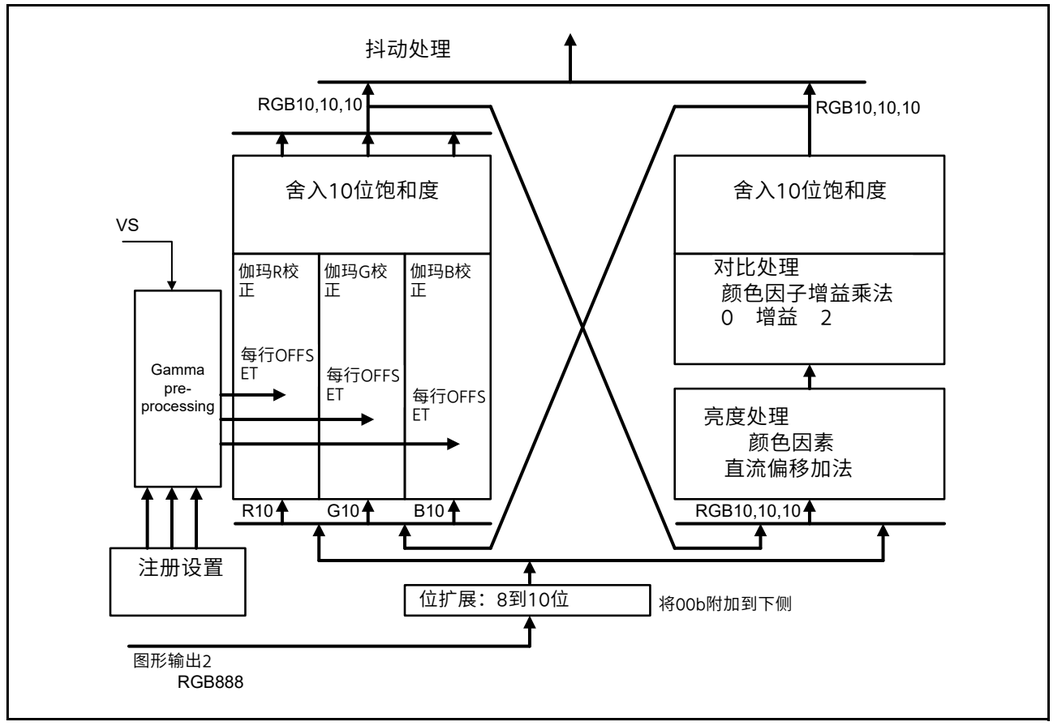


Figure 58.6 面向面板的校正电路的构成

58.1.6 TCON的输出控制

从内部垂直和水平同步信号（STVA、STVB、
通过数据格式转换模块的STHA和STHB)可以选择在四个引脚上输出，
LCD_TCON0、LCD_TCON1、LCD_TCON2和LCD_TCON3。生成的信号完全独立于图像数据。它们不受输出图像格式或任何内部数据处理的影响，并且没有用于信号生成的寄存器设置影响输出图像格式或任何内部数据处理。将由TCON块产生的数据使能信号DE是先前由TCON块产生的两个信号STVB和STHB的逻辑与。因此，如果要输出DE，实际上总共可以产生三个信号。

58.1.7 图形数据接口

提供了两个用于读取图形数据（图形1和2）的电路系统，每个系统都包含访问控制块、数据缓冲器、CLUT存储器、数据扩展块和异步接口块。

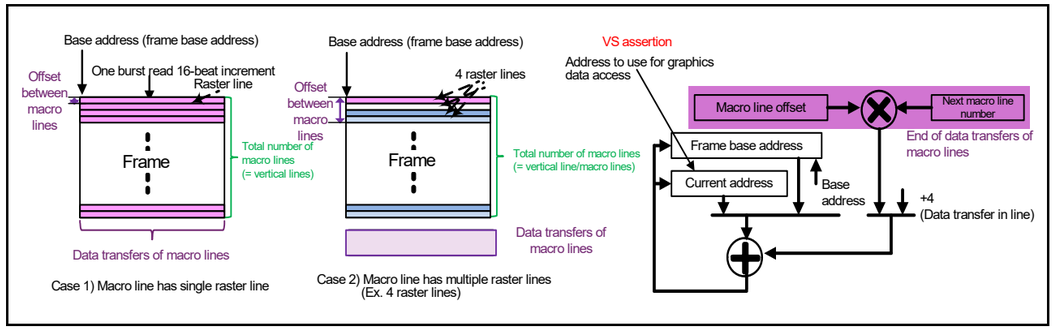


Figure 58.7 Calculation of graphics data access address

Graphics (or CLUT) data is accessed and output to the pixel operation block as ARGB8888 data (32 bits/pixel).

The GPX bus is accessed in word (32-bit) units in 16-beat increment burst reads, in accordance with the preset parameters in the two-dimensional addressing mode, in which the macro line structure is accounted for as shown in Figure 58.7, and data is stored in the data buffer. Even if invalid data is at the macro line end, all the data is stored in the data buffer, and the invalid data is skipped when data is read internally. Regardless of the format of the graphics data, data is extended to ARGB8888 data before being output to the alpha blending blocks.

58.1.8 Blending

The following processes are performed for the graphics areas specified in the registers. The lower-layer graphics plane is output without any processing to the display area outside the graphics area.

- Display plane selection
- RGB-index chroma-key
- Alpha blending.

Figure 58.8 shows the relationship between the graphics display selection and rectangular alpha blending area.

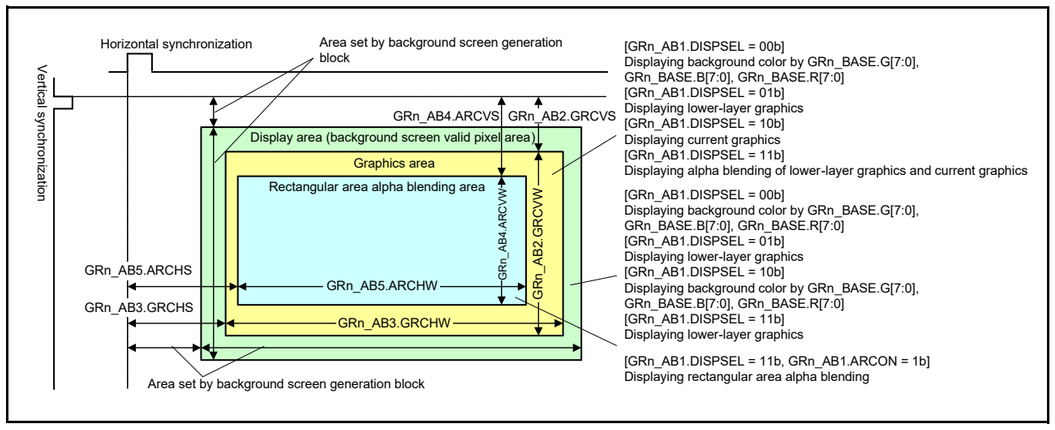


Figure 58.8 Graphics display selection

(1) Display plane selection

Based on the register settings, the following data is output to the graphics area:

- Background color:
  - RGB data specified in the registers.

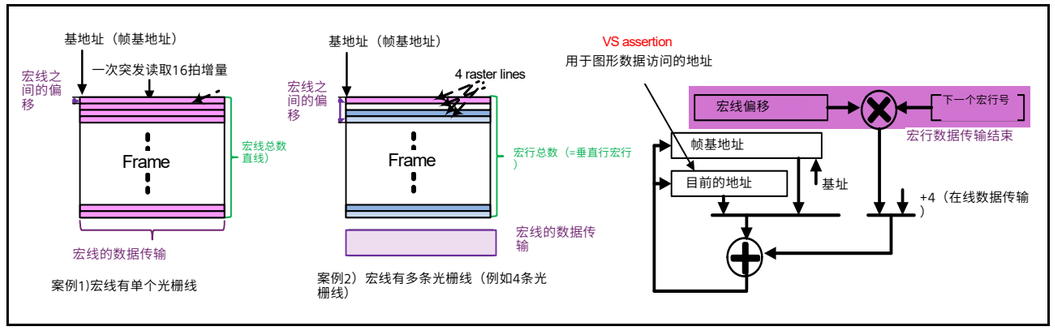


Figure 58.7 计算图形数据访问地址

图形（或CLUT）数据被访问并作为ARGB8888数据（32位像素）输出到像素操作块。

GPX总线以16-beat增量突发读取为单位，按照二维寻址方式中的预设参数，以字（32位）为单位进行访问，其中宏线结构如图58.7所示，数据存储在数据缓冲区中。即使无效数据在宏行结束，所有数据都存储在数据缓冲区中，内部读取数据时会跳过无效数据。无论图形数据的格式如何，在输出到alpha混合块之前，数据都被扩展为ARGB8888数据。

58.1.8 Blending

对寄存器中指定的图形区域执行以下处理。下层图形平面不经过任何处理就输出到图形区域外的显示区域。

- 显示平面选择
- RGB-index chroma-key
- 阿尔法混合。

图58.8显示了图形显示选择和矩形alpha混合区域之间的关系。

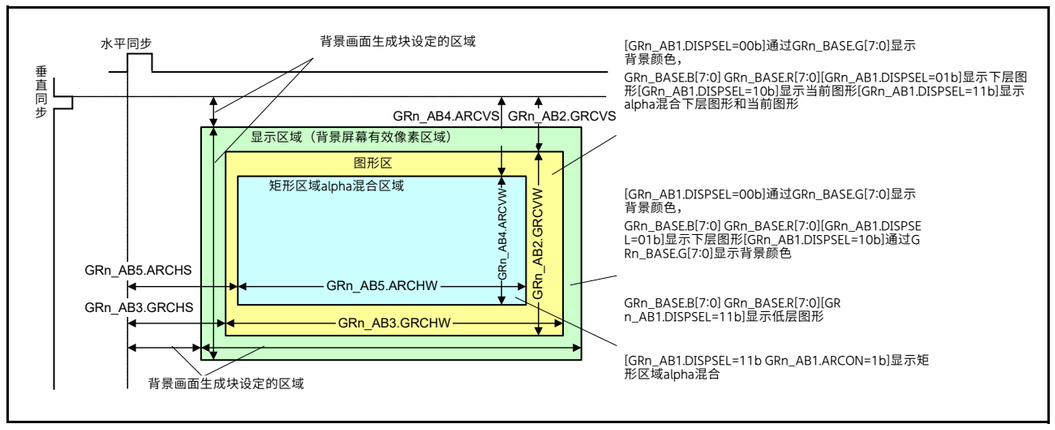


Figure 58.8 图形显示选择

(1) 显示平面选择

根据寄存器设置，将以下数据输出到图形区域：

- Background color:
  - 寄存器中指定的RGB数据。

- Lower-layer graphics:
  - RGB data input from the previous module
  - Output from the background screen generation block for graphics 1
  - Output from graphics 1 for graphics 2.
- Current graphics:
  - RGB data obtained by the graphics data interface block extending the graphics data read by the graphics 1 or 2 module through the GPX bus or CLUT data to ARGB8888 format data.
- Blending:
  - RGB data obtained by blending the lower-layer graphics data and current graphics data obtained by the graphics data interface block extension to ARGB8888 format data, based on the alpha blending values or the register settings.

It is possible to modify the register values related to these functions while display operation is in progress, and to allow reflection of the updates to the internal operations when the VS (vertical synchronization signal) is asserted, if reflection of the register settings to the internal operations on vertical synchronization is enabled.

(2) RGB-index chroma-key

If the RGB value of the ARGB8888 data input from the graphics data interface block agrees with the value set in the GRn_AB8 register, the ARGB8888 data is entirely replaced with the value preset in the GRn_AB9 register. All the ARGB8888 data input from the graphics data interface block is subject to this process. If your application excludes CLUT memory output from this process, you must disable the corresponding process in GRn_AB7.CKON.

(3) Alpha blending

If blending is selected in the selected display plane, lower-layer graphics and current graphics are alpha-blended based on the register settings using either of the following two functions.

(a) Alpha-blending in a rectangular area

The following process is performed for the rectangular area (in the graphics area) preset in the registers:

1. Lower-layer graphics and current graphics planes are blended in accordance with the A value set in the registers.
2. After the number of frames set in the registers passes, the A value is updated to the A value + Δ (register setting).
3. The lower-layer graphics and current graphics planes are blended in accordance with this updated A value.
4. The process of updating the A value after the number of frames set in the registers passes is repeated (A value: min/max value saturation).

(b) Alpha-blending in pixel units

The lower-layer graphics and current graphics planes are blended in accordance with the A value of the ARGB8888 data input from the graphics data interface block.

Figure 58.9 shows the update of the alpha blending value in the rectangular alpha blending area.

- Lower-layer graphics:
  - 从上一个模块输入的RGB数据
  - 图形1的背景屏幕生成块的输出
  - 图形2的图形1输出。
- Current graphics:
  - 图形数据接口块将图形1或2模块通过GPX总线读取的图形数据或CLUT数据扩展为ARGB8888格式数据得到的RGB数据。
- Blending:
  - 根据alpha混合值或寄存器设置，将下层图形数据和图形数据接口块扩展得到的当前图形数据混合为ARGB8888格式数据得到的RGB数据。

可以在显示操作进行时修改与这些功能相关的寄存器值，并允许在VS（垂直同步信号）置位时将更新反映到内部操作，如果将寄存器设置反映到内部启用垂直同步操作。

(2) RGB-index chroma-key

如果从图形数据接口块输入的ARGB8888数据的RGB值与GRn_AB8寄存器，ARGB8888数据全部替换为GRn_AB9寄存器中预设的值。所有从图形数据接口块输入的ARGB8888数据都要经过这个过程。如果您的应用程序不包括此进程的CLUT内存输出，必须在GRn_AB7.CKON中禁用相应进程。

(3) 阿尔法混合

如果在选定的显示平面中选择了混合，则下层图形和当前图形使用以下两个功能之一根据寄存器设置进行alpha混合。

(a) 矩形区域中的Alpha混合

对寄存器中预设的矩形区域（图形区域内）进行如下处理：

1. 下层图形和当前图形平面按照寄存器中设置的A值进行混合。
2. 在寄存器中设置的帧数通过后，A值更新为A值+Δ（寄存器设置）。
3. 下层图形和当前图形平面按照这个更新的A值进行混合。
4. 在寄存器中设置的帧数通过后更新A值的过程被重复（A值：最小最大值饱和）。

(b) 以像素为单位的Alpha混合

下层图形和当前图形平面按照从图形数据接口块输入的ARGB8888数据的A值进行混合。

图58.9显示了矩形alpha混合区域中alpha混合值的更新。

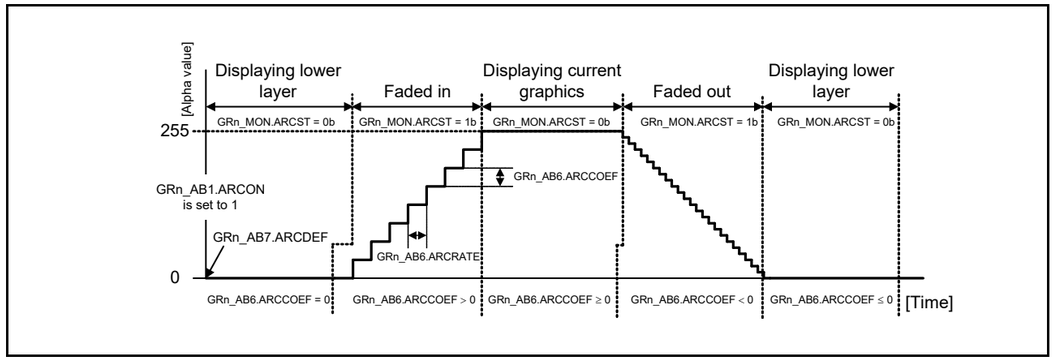


Figure 58.9 Updating of alpha blending value

Alpha blending is based on the following formulas:

When A value = 255
Rout/Gout/Bout = current graphics data
When A value ≠ 255
Rout = (Rin1 × A + Rin0 × (256 - A))/256
Gout = (Gin1 × A + Gin0 × (256 - A))/256
Bout = (Bin1 × A + Bin0 × (256 - A))/256

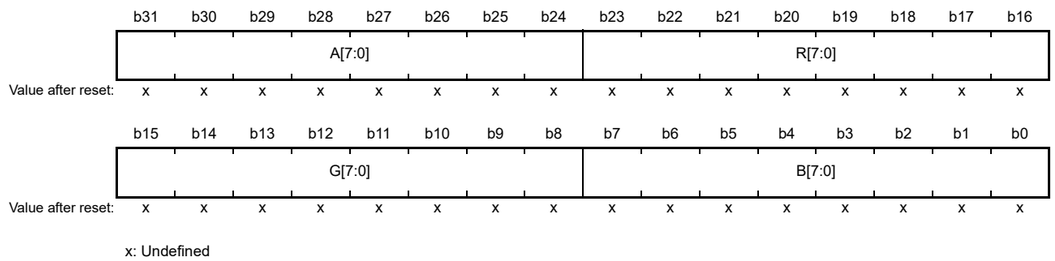
where,

A: alpha blending value
Rin1/Gin1/Bin1: current graphics data
Rin0/Gin0/Bin0: lower-layer graphics data

58.2 Register Descriptions

58.2.1 Color Palette (CLUT)

- Color Palette 0 Plane for Graphics 1 Plane 0 to Color Palette 0 Plane for Graphics 1 Plane 255 (GR1_CLUT0[0] to GR1_CLUT0[255])
  Address(es): GLCDC.GR1_CLUT0[0] 400E 0000h to GLCDC.GR1_CLUT0[255] 400E 03FCh
- Color Palette 1 Plane for Graphics 1 Plane 0 to Color Palette 1 Plane for Graphics 1 Plane 255 (GR1_CLUT1[0] to GR1_CLUT1[255])
  Address(es): GLCDC.GR1_CLUT1[0] 400E 0400h to GLCDC.GR1_CLUT1[255] 400E 07FCh
- Color Palette 0 Plane for Graphics 2 Plane 0 to Color Palette 0 Plane for Graphics 2 Plane 255 (GR2_CLUT0[0] to GR2_CLUT0[255])
  Address(es): GLCDC.GR2_CLUT0[0] 400E 0800h to GLCDC.GR2_CLUT0[255] 400E 0BFCh
- Color Palette 1 Plane for Graphics 2 Plane 0 to Color Palette 1 Plane for Graphics 2 Plane 255 (GR2_CLUT1[0] to GR2_CLUT1[255])
  Address(es): GLCDC.GR2_CLUT1[0] 400E 0C00h to GLCDC.GR2_CLUT1[255] 400E 0FFCh



x: Undefined

Bit	Symbol	Bit name	Description	R/W
b7 to b0	B[7:0]	B Value of Color Palette n Plane for Graphics m Plane	B value of color palette n plane for graphics m plane. Unsigned 8-bit integer.	R/W

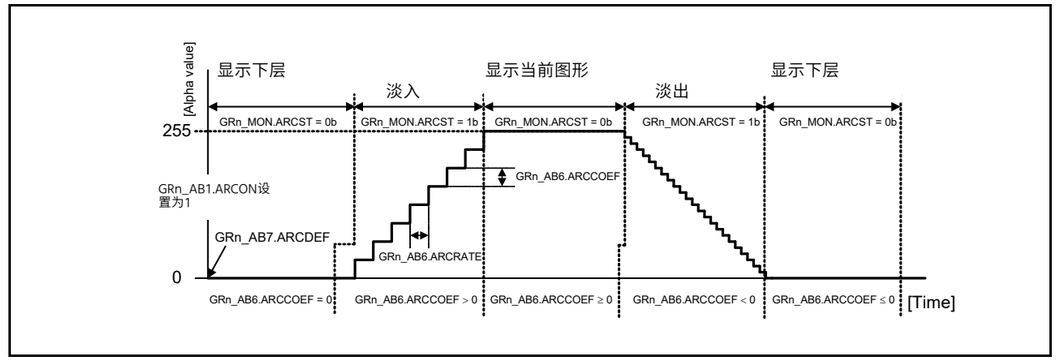


Figure 58.9 更新alpha混合值

Alpha混合基于以下公式：

当A值=255RoutGoutBout=当前图形数据

A值≠255时

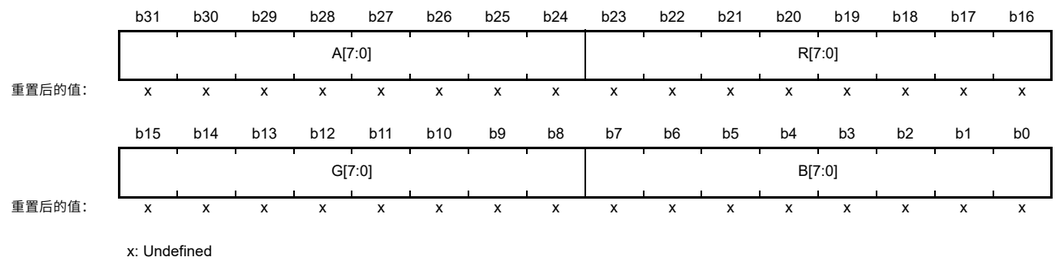
Rout=(Rin1×A+Rin0×(256A))256Gout=(Gin1×A+Gin0×(256A))256Bout=(Bin1×A+Bin0×(256A))256其中，

A：阿尔法混合值
Rin1Gin1Bin1：当前图形数据
Rin0Gin0Bin0：下层图形数据

58.2 注册说明

58.2.1 调色板(CLUT)

调色板0平面用于图形1平面0到调色板0平面用于图形1平面255（GR1_CLUT0[0]到GR1_CLUT0[255]）
Address(es): GLCDC.GR1_CLUT0[0] 400E 0000h to GLCDC.GR1_CLUT0[255] 400E 03FCh
图形1平面0到调色板1平面图形1平面255的调色板1平面（GR1_CLUT1[0]到GR1_CLUT1[255]）
Address(es): GLCDC.GR1_CLUT1[0] 400E 0400h to GLCDC.GR1_CLUT1[255] 400E 07FCh
调色板0平面用于图形2平面0到调色板0平面用于图形2平面255（GR2_CLUT0[0]到GR2_CLUT0[255]）
Address(es): GLCDC.GR2_CLUT0[0] 400E 0800h to GLCDC.GR2_CLUT0[255] 400E 0BFCh
用于图形2平面0的调色板1平面到用于图形2平面255的调色板1平面（GR2_CLUT1[0]到GR2_CLUT1[255]）
Address(es): GLCDC.GR2_CLUT1[0] 400E 0C00h to GLCDC.GR2_CLUT1[255] 400E 0FFCh



x: Undefined

Bit	Symbol	位名称	Description	R/W
b7 to b0	B[7:0]	图形m平面的调色板n平面的B值	图形m平面的调色板n平面的B值。无符号8位整数。	R/W

Bit	Symbol	Bit name	Description	R/W
b15 to b8	G[7:0]	G Value of Color Palette n Plane for Graphics m Plane	G value of color palette n plane for graphics m plane. Unsigned 8-bit integer.	R/W
b23 to b16	R[7:0]	R Value of Color Palette n Plane for Graphics m Plane	R value of color palette n plane for graphics m plane. Unsigned 8-bit integer.	R/W
b31 to b24	A[7:0]	Alpha Blending Value of Color Palette n Plane for Graphics m Plane	Alpha blending value of color palette n plane for graphics m plane. Unsigned 8-bit integer.	R/W

B[7:0] bits (B Value of Color Palette n Plane for Graphics m Plane)

The B[7:0] bits set the B value when this color palette is used.

G[7:0] bits (G Value of Color Palette n Plane for Graphics m Plane)

The G[7:0] bits set the G value when this color palette is used.

R[7:0] bits (R Value of Color Palette n Plane for Graphics m Plane)

The R[7:0] bits set the R value when this color palette is used.

A[7:0] bits (Alpha Blending Value of Color Palette n Plane for Graphics m Plane)

The A[7:0] bits set the alpha blending value when this color palette is used.

All the planes can always be accessed through the register access bus (internal peripheral bus 8), regardless of the plane specified to be used by the graphics data access block. The updates are reflected to the internal operations directly, not in synchronization with the vertical synchronization signal. To keep reflection of the CLUT memory contents to the internal operations in synchronization with the vertical synchronization signal, first write data through the register access bus to the plane that is not being used for internal operations, and then modify the GRn_CLUTINT.SEL bit for controlling the plane that is to be used.

58.2.2 Background Plane Setting Operation Control Register (BG_EN)

Address(es): GLCDC.BG_EN 400E 1000h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SWRST
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	VEN	—	—	—	—	—	—	—	EN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	EN	Background Plane Operation Enable	0: Disable background plane operation 1: Enable background plane operation.	R/W
b7 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	VEN	Control of GLCDC Internal Register Value Reflection to Internal Operations	0: Disable GLCDC register values from being reflected in internal operations at start of screen generation 1: Enable GLCDC register values to be reflected in internal operations at start of screen generation. This bit is cleared to 0 by an internal source.	R/W
b15 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b16	SWRST	Software Reset Control	0: Place entire module in software reset state 1: Release entire module from software reset state.	R/W
b31 to b17	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Bit	Symbol	位名称	Description	R/W
b15 to b8	G[7:0]	图形m平面的调色板n平面的G值	图形m平面的调色板n平面的G值。 无符号8位整数。	R/W
b23 to b16	R[7:0]	图形m平面的调色板n平面的R值	图形m平面的调色板n平面的R值。 无符号8位整数。	R/W
b31 to b24	A[7:0]	图形m的调色板n平面的Alpha混合值 Plane	图形m平面的调色板n平面的Alpha混合值。无符号8位整数。	R/W

B[7:0]位（图形m平面的调色板n平面的B值）

当使用此调色板时，B[7:0]位设置B值。

G[7:0]位（图形m平面的调色板n平面的G值）

当使用此调色板时，G[7:0]位设置G值。

R[7:0]位（图形m平面的调色板n平面的R值）

当使用此调色板时，R[7:0]位设置R值。

A[7:0]位（图形m平面的调色板n平面的Alpha混合值）

当使用此调色板时，A[7:0]位设置alpha混合值。

所有平面总是可以通过寄存器访问总线（内部外围总线8）访问，而与图形数据访问块指定使用的平面无关。更新直接反映到内部操作，而不是与垂直同步信号同步。为了保持CLUT内存内容与垂直同步信号同步地反映到内部操作，首先通过寄存器访问总线将数据写入不用于内部操作的平面，然后修改GRn_CLUTINT.SEL位进行控制要使用的飞机。

58.2.2 后台平面设置操作控制寄存器（BG_EN）

Address(es): GLCDC.BG_EN 400E 1000h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SWRST
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	VEN	—	—	—	—	—	—	—	EN
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	EN	后台平面操作 Enable	0：关闭后台平面操作1：开启后台平面操作。	R/W
b7 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b8	VEN	控制GLCDC内部寄存器值反射到 内部运营	0：禁止GLCDC寄存器值在屏幕生成开始时反映在内部操作中1：使GLCDC寄存器值在屏幕生成开始时反映在内部操作中。该位由内部源清零。	R/W
b15 to b9	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b16	SWRST	软件复位控制	0：将整个模块置于软件复位状态1：将整个模块从软件复位状态释放。	R/W
b31 to b17	—	Reserved	这些位被读取为0。写入值应为0。	R/W

EN bit (Background Plane Operation Enable)

The EN bit enables or disables the operation of the background plane generation module. When the operation is stopped (this bit is cleared to 0) after the operation is enabled (set to 1), the operation is stopped at the end of screen generation, unlike when a software reset occurs.

When setting this bit to 1, set the BG_EN.VEN bit to 1 simultaneously to enable register value reflection to internal operations. When clearing this bit to 0, also clear the BG_EN.VEN bit to 0 simultaneously. Before clearing this bit to 0, confirm that the BG_MON.VEN bit is cleared to 0, to make sure that the signal for controlling reflection of the register values to internal operations is negated. Operation is not guaranteed if this bit and the BG_EN.VEN bit are set to 1, or if the settings in other registers are modified before the BG_MON.EN bit is cleared to 0.

VEN bit (Control of GLCDC Internal Register Value Reflection to Internal Operations)

The VEN bit enables or disables reflection of the GLCDC internal register to the GLCDC internal operation on assertion of the vertical synchronization signal (input). When this bit is set to 1, the signal of GLCDC internal register values reflection control is set to 1 at the immediate start of the screen, and are automatically cleared to 0 at the end of the vertical valid pixel of the same screen. Set this bit to 1 only when 0. Operation is not guaranteed if this bit is set to 1 when 1. Also, while this bit is 1, do not modify any register whose value is reflected to the internal operations at the start of the screen in the GLCDC or on assertion of the vertical synchronization signal (input). Otherwise, operation is not guaranteed.

SWRST bit (Software Reset Control)

The SWRST bit controls a software reset of the entire GLCDC, not only the background plane generation module. When this bit is cleared to 0, the GLCDC enters the reset state from any operation state. This bit must be set to 1 before the registers are set or operation enabled. Although the registers (except the CLUT memory and the some of the operation control registers) can be set while this bit is set to 1 (immediately after), before accessing the CLUT memory, enabling operation, or reflecting the register values to the internal operation by the vertical synchronization signal, confirm that PXCLK/LCD_CLK and PCLKA are supplied and that the BG_MON.SWRST bit, which monitors the entire module software reset state, is set to 1. Operation is not guaranteed if the software accesses CLUT memory, enables operation, or reflects the register vales to the internal operation on the vertical synchronization signal while PXCLK/LCD_CLK and PCLKA are not supplied or the BG_MON.SWRST bit is not set to 1. The peripheral bus clock (PCLKA) must be supplied to the GLCDC when this bit is used to apply or cancel a software reset. If PCLKA is not supplied, writing to this bit is impossible.

The bits in this register control the GLCDC states. The internal states can be read from the associated bits in the status monitor registers and BG_EN.VEN (this register). Because the GLCDC, which operates on multiple clock signals, requires a certain period for state transition, you must confirm that the internal state has stabilized (state transition is complete) when settings are modified. Operation is not guaranteed if settings are modified again before the internal state stabilizes (state transition is complete). However, clearing a software reset to 0 immediately makes the whole GLCDC reset, setting it to 1 releases the reset state. These operations do not require the clock supply of PXCLK.

EN位（后台平面操作使能）

EN位启用或禁用后台平面生成模块的操作。当操作使能（设置为1）后停止操作（该位清零）时，操作在屏幕生成结束时停止，这与发生软件复位时不同。

将此位设置为1时，同时将BG_EN.VEN位设置为1，以使寄存器值反映到内部操作。将该位清0时，同时将BG_EN.VEN位清0。在将该位清零之前，请确认BG_MON.VEN位清零，以确保控制寄存器值反映到内部操作的信号被取反。如果该位和BG_EN.VEN位设置为1，或者如果在BG_MON.EN位清零之前修改了其他寄存器中的设置，则无法保证操作。

VEN位（控制GLCDC内部寄存器值反映到内部操作）

VEN位启用或禁用GLCDC内部寄存器在垂直同步信号（输入）断言时反射到GLCDC内部操作。当该位设置为1时，GLCDC内部寄存器值反射控制的信号在屏幕的立即开始时设置为1，并在同一屏幕的垂直有效像素结束时自动清零。仅在0时将此位设置为1。如果此位在1时设置为1，则不保证操作。此外，当此位为1时，请勿修改其值反映到屏幕开始时的内部操作的任何寄存器在GLCDC或垂直同步信号（输入）的断言。否则，无法保证操作。

SWRST位（软件复位控制）

SWRST位控制整个GLCDC的软件复位，而不仅仅是后台平面生成模块。当该位清0时，GLCDC从任何操作状态进入复位状态。在设置寄存器或启用操作之前，该位必须设置为1。虽然寄存器（除了CLUT存储器和一些操作控制寄存器）可以在该位设置为1时（紧接之后）设置，但在访问CLUT存储器、启用操作或将寄存器值反映到内部操作之前通过垂直同步信号，确认提供了PXCLKLCD_CLK和PCLKA，并且监控整个模块软件复位状态的BG_MON.SWRST位设置为1。如果软件访问CLUT存储器，使能操作，则无法保证操作，或在未提供PXCLKLCD_CLK和PCLKA或BG_MON.SWRST位未设置为1时将寄存器值反映到垂直同步信号上的内部操作。当此位时，必须向GLCDC提供外围总线时钟(PCLKA)用于应用或取消软件复位。如果未提供PCLKA，则无法写入该位。

该寄存器中的位控制GLCDC状态。可以从状态监视器寄存器和BG_EN.VEN（此寄存器）中的相关位读取内部状态。由于GLCDC对多个时钟信号进行操作，因此需要一定的状态转换周期，因此在修改设置时必须确认内部状态已稳定（状态转换完成）　　。如果在内部状态稳定（状态转换完成）　　之前再次修改设置，则无法保证操作。但是，将软件复位清除为0会立即使整个GLCDC复位，将其设置为1会释放复位状态。这些操作不需要PXCLK的时钟供应。

58.2.3 Background Plane Setting Free-Running Period Register (BG_PERI)

Address(es): GLCDC.BG_PERI 400E 1004h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	FV[10:0]										
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	FH[10:0]										
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1

Bit	Symbol	Bit name	Description	R/W
b10 to b0	FH[10:0]	Background Plane Horizontal Synchronization Signal Period	Period based on pixel clocks (PXCLK). 017h: 24 cycles (pixels) 3FFh: 1024 cycles (pixels). Other settings are prohibited.	R/W
b15 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b26 to b16	FV[10:0]	Background Plane Vertical Synchronization Signal Period	Period based on lines. 013h: 20 lines 3FFh: 1024 lines. Other settings are prohibited.	R/W
b31 to b27	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Rewriting these bits is prohibited during operation. Set the required settings before enabling operation. Operation is not guaranteed if the bit is rewritten during operation.

FH[10:0] bits (Background Plane Horizontal Synchronization Signal Period)

The FH[10:0] bits set the horizontal synchronization signal period of the background plane. This field contains 11 bits and can be set to any number from 000h to 7FFh. However, the valid range is 017h to 3FFh. Operation is not guaranteed if a value outside the valid range is set.

FV[10:0] bits (Background Plane Vertical Synchronization Signal Period)

The FV[10:0] bits set the vertical synchronization signal period of the background plane. This field contains 11 bits and can be set to any number from 000h to 7FFh. However, the valid range is 013h to 3FFh. Operation is not guaranteed if a value outside the valid range is set.

58.2.3 后台平面设置自由运行周期寄存器（BG_PERI）

Address(es): GLCDC.BG_PERI 400E 1004h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	FV[10:0]										
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	FH[10:0]										
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1

Bit	Symbol	位名称	Description	R/W
b10 to b0	FH[10:0]	背景平面水平同步信号周期	基于像素时钟(PXCLK)的周期。017h：24个周期（像素）3FFh：1024个周期（像素）。禁止其他设置。	R/W
b15 to b11	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b26 to b16	FV[10:0]	背景平面垂直同步信号周期	基于行的周期。013h：20行 3FFh：1024行。禁止其他设置。	R/W
b31 to b27	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note: 操作期间禁止改写这些位。在启用操作之前设置所需的设置。如果在操作期间重写该位，则无法保证操作。

FH[10:0]位（背景平面水平同步信号周期）

FH[10:0]位设置背景平面的水平同步信号周期。该字段包含11位，可以设置为从000h到7FFh的任何数字。但是，有效范围是017h到3FFh。如果设置了有效范围之外的值，则无法保证操作。

FV[10:0]位（背景平面垂直同步信号周期）

FV[10:0]位设置背景平面的垂直同步信号周期。该字段包含11位，可以设置为从000h到7FFh的任何数字。但是，有效范围是013h到3FFh。如果设置了有效范围之外的值，则无法保证操作。

58.2.4 Background Plane Setting Synchronization Position Register (BG_SYNC)

Address(es): GLCDC.BG_SYNC 400E 1008h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	VP[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	HP[3:0]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	Bit name	Description	R/W
b3 to b0	HP[3:0]	Background Plane Horizontal Synchronization Signal Assertion Position	Position based on pixel clocks (PXCLK). 0h: Setting prohibited 1h: 1st cycle (pixel) : Fh: 15th cycle (pixel).	R/W
b15 to b4	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b19 to b16	VP[3:0]	Background Plane Vertical Synchronization Assertion Position	Position based on lines. 0h: Setting prohibited 1h: 1st line : Fh: 15th line.	R/W
b31 to b20	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Rewriting these bits is prohibited during operation. Set the required settings before enabling operation. Operation is not guaranteed if the bit is rewritten during operation.

HP[3:0] bits (Background Plane Horizontal Synchronization Signal Assertion Position)

The HP[3:0] bits set the horizontal synchronization signal assertion position of the background plane. The signal is held asserted for a 4-pixel clock width.

VP[3:0] bits (Background Plane Vertical Synchronization Assertion Position)

The VP[3:0] bits set the vertical synchronization signal assertion position of the background plane. The signal is held asserted for a 1H width, and the assertion timing within a single horizontal line is specified in BG_SYNC.HP[3:0].

58.2.4 后台平面设置同步位置寄存器（BG_SYNC）

Address(es): GLCDC.BG_SYNC 400E 1008h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	VP[3:0]			
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	HP[3:0]			
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1

Bit	Symbol	位名称	Description	R/W
b3 to b0	HP[3:0]	背景平面水平 同步信号断言 Position	基于像素时钟(PXCLK)的位置。0h：禁止 设置1h：第1周期（像素） : Fh: 15th cycle (pixel).	R/W
b15 to b4	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b19 to b16	VP[3:0]	背景平面垂直同步断言 Position	基于线条的位置。0h： 禁止设置1h：第一行 : Fh: 15th line.	R/W
b31 to b20	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note: 操作期间禁止改写这些位。在启用操作之前设置所需的设置。如果在操作期间重写该位，则无法保证操作。

HP[3:0]位（背景平面水平同步信号断言位置）

HP[3:0]位设置背景平面的水平同步信号断言位置。该信号在4像素时钟宽度内保持有效。

VP[3:0]位（背景平面垂直同步断言位置）

VP[3:0]位设置背景平面的垂直同步信号断言位置。该信号被保持为1H宽度，并且单个水平线内的断言时序在BG_SYNC.HP[3:0]中指定。

58.2.5 Background Plane Setting Full Image Vertical Size Register (BG_VSIZE)

Address(es): GLCDC.BG_VSIZE 400E 100Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	VP[10:0]										
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	VW[10:0]										
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b10 to b0	VW[10:0]	Background Plane Vertical Valid Pixel Width	Width based on lines. 010h: 16 lines : 3FCh: 1020 lines. Other settings are prohibited.	R/W
b15 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b26 to b16	VP[10:0]	Background Plane Vertical Valid Pixel Start Position	Position based on of lines. 003h: 3rd line : 3EFh: 1007th lines Other settings are prohibited.	R/W
b31 to b27	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Rewriting these bits is prohibited during operation. Set the required settings before enabling operation. Operation is not guaranteed if the bit is rewritten during operation.

VW[10:0] bits (Background Plane Vertical Valid Pixel Width)

The VW[10:0] bits set the vertical valid pixel width of the background plane. This field contains 11 bits and can be set to any number from 000h to 7FFh. However, the valid range is 010h to 3FCh. Operation is not guaranteed if a value outside the valid range is set.

VP[10:0] bits (Background Plane Vertical Valid Pixel Start Position)

The VP[10:0] bits set the vertical valid pixel start position of the background plane. This field contains 11 bits and can be set to any number from 000h to 7FFh. However, the valid range is 003h to 3EFh. Operation is not guaranteed if a value outside the valid range is set.

Specify the vertical valid pixel area between the assertion position of the vertical synchronization signal + 2 and the (background plane end - 1)th line. Operation is not guaranteed if the area is specified outside this range.

58.2.5 背景平面设置全图垂直尺寸寄存器（BG_VSIZE）

Address(es): GLCDC.BG_VSIZE 400E 100Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	VP[10:0]										
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	VW[10:0]										
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b10 to b0	VW[10:0]	背景平面垂直有效像素宽度	基于线条的宽度。010h：16行 :3FCh:1020行。禁止其他设置。	R/W
b15 to b11	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b26 to b16	VP[10:0]	背景平面垂直有效像素起始位置	基于行的位置。003h：第三行 :3EFh:第1007行禁止其他设置。	R/W
b31 to b27	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note: 操作期间禁止改写这些位。在启用操作之前设置所需的设置。如果在操作期间重写该位，则无法保证操作。

VW[10:0]位（背景平面垂直有效像素宽度）

VW[10:0]位设置背景平面的垂直有效像素宽度。该字段包含11位，可以设置为从000h到7FFh的任何数字。但是，有效范围是010h到3FCh。如果设置了有效范围之外的值，则无法保证操作。

VP[10:0]位（背景平面垂直有效像素起始位置）

VP[10:0]位设置背景平面的垂直有效像素起始位置。该字段包含11位，可以设置为从000h到7FFh的任何数字。但是，有效范围是003h到3EFh。如果设置了有效范围之外的值，则无法保证操作。

指定垂直同步信号+2的断言位置和第（背景平面端1）行之间的垂直有效像素区域。如果指定的区域超出此范围，则无法保证操作。

58.2.6 Background Plane Setting Full Image Horizontal Size Register (BG_HSIZE)

Address(es): GLCDC.BG_HSIZE 400E 1010h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	HP[10:0]										
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	HW[10:0]										
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b10 to b0	HW[10:0]	Background Plane Horizontal Valid Pixel Width	Width based on pixel clocks (PXCLK). 010h: 16 cycles : 3F8h: 1016 cycles. Other settings are prohibited.	R/W
b15 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b26 to b16	HP[10:0]	Background Plane Horizontal Valid Pixel Start Position	Position based on pixel clocks (PXCLK). 006h: 6th cycle (pixel) : 3EEh: 1006th cycle (pixel). Other settings are prohibited.	R/W
b31 to b27	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Rewriting these bits is prohibited during operation. Set the required settings before enabling operation. Operation is not guaranteed if the bit is rewritten during operation.

HW[10:0] bits (Background Plane Horizontal Valid Pixel Width)

The HW[10:0] bits set the horizontal valid pixel width of the background plane. This field contains 11 bits and can be set to any number from 000h to 7FFh. However, the valid range is 010h to 3F8h. Operation is not guaranteed if a value outside the valid range is set. When serial RGB is selected as the output format for the output control block, add two to the horizontal valid pixel width and set the resulting value to these bits.

HP[10:0] bits (Background Plane Horizontal Valid Pixel Start Position)

The HP[10:0] bits set the horizontal valid pixel start position of the background plane. This field contains 11 bits and can be set to any number from 000h to 7FFh. However, the valid range is 006h to 3EEh. Operation is not guaranteed if a value outside the valid range is set.

Specify the horizontal valid pixel area between the assertion position of the horizontal synchronization signal + 5 and pixel number (line end - 2). Operation is not guaranteed if the area is specified outside this range.

The background plane generation module outputs the values that are specified in the Background Color Register (BG_BGC) for the area defined by the Full Image Vertical Size Register (BG_VSIZE) and Full Image Horizontal Size Register (BG_HSIZE), and it outputs 00h as the RGB values for the blanking interval area.

58.2.6 背景平面设置全图水平尺寸寄存器（BG_HSIZE）

Address(es): GLCDC.BG_HSIZE 400E 1010h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	HP[10:0]										
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	HW[10:0]										
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b10 to b0	HW[10:0]	背景平面水平 有效像素宽度	基于像素时钟(PXCLK)的宽度。010h ：16个周期 :3F8h:1016个周期。禁止其 他设置。	R/W
b15 to b11	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b26 to b16	HP[10:0]	背景平面水平 有效像素起始位置	基于像素时钟(PXCLK)的位置。006h：第 6个周期（像素） :3EEh:第1006个周期（像素 ）。禁止其他设置。	R/W
b31 to b27	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note: 操作期间禁止改写这些位。在启用操作之前设置所需的设置。如果在操作期间重写该位，则无法保证操作。

HW[10:0]位（背景平面水平有效像素宽度）

HW[10:0]位设置背景平面的水平有效像素宽度。该字段包含11位，可以设置为从000h到7FFh的任何数字。但是，有效范围是010h到3F8h。如果设置了有效范围之外的值，则无法保证操作。WhenserialRGBisselectedastheoutputformatfortheoutputcontrolblock addtwotothehorizo ntalvalidpixelwidthandsettheresultingvaluetothesebits.

HP[10:0]位（背景平面水平有效像素起始位置）

HP[10:0]位设置背景平面的水平有效像素起始位置。该字段包含11位，可以设置为从000h到7FFh的任何数字。但是，有效范围是006h到3EEh。如果设置了有效范围之外的值，则无法保证操作。

指定水平同步信号的断言位置+5和像素数（行尾2）之间的水平有效像素区域。如果指定的区域超出此范围，则无法保证操作。

背景平面生成模块输出背景颜色寄存器(BG_BGC)中指定的值，用于由全图像垂直大小寄存器(BG_VSIZE)和全图像水平大小寄存器(BG_HSIZE)定义的区域，并输出00h作为RGB消隐区间区域的值。

58.2.7 Background Plane Setting Background Color Register (BG_BGC)

Address(es): GLCDC.BG_BGC 400E 1014h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	R[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	G[7:0]								B[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	B[7:0]	Background Plane Valid Pixel Area B Value	B value for background plane valid pixel area. Unsigned 8-bit integer.	R/W
b15 to b8	G[7:0]	Background Plane Valid Pixel Area G Value	G value for background plane valid pixel area. Unsigned 8-bit integer.	R/W
b23 to b16	R[7:0]	Background Plane Valid Pixel Area R Value	R value for background plane valid pixel area. Unsigned 8-bit integer.	R/W
b31 to b24	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

B[7:0] bits (Background Plane Valid Pixel Area B Value)

The B[7:0] bits set the B value of image data to be output to the valid pixel area of the background plane.

G[7:0] bits (Background Plane Valid Pixel Area G Value)

The G[7:0] bits set the G value of image data to be output to the valid pixel area of the background plane.

R[7:0] bits (Background Plane Valid Pixel Area R Value)

The R[7:0] bits set the R value of image data to be output to the valid pixel area of the background plane.

58.2.8 Background Plane Setting Status Monitor Register (BG_MON)

Address(es): GLCDC.BG_MON 400E 1018h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SWRST
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	VEN	—	—	—	—	—	—	—	EN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	EN	Background Plane Operation Monitor	0: Operation is stopped 1: Operation is in progress.	R
b7 to b1	—	Reserved	These bits are read as 0.	R

58.2.7 背景平面设置背景颜色寄存器（BG_BGC）

Address(es): GLCDC.BG_BGC 400E 1014h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	R[7:0]							
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	G[7:0]								B[7:0]							
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b7 to b0	B[7:0]	背景平面有效像素B区价值	背景平面有效像素区域的B值。无符号8位整数。	R/W
b15 to b8	G[7:0]	背景平面有效像素G区价值	背景平面有效像素区域的G值。无符号8位整数。	R/W
b23 to b16	R[7:0]	背景平面有效像素面积R值	背景平面有效像素区域的R值。无符号8位整数。	R/W
b31 to b24	—	Reserved	这些位被读取为0。写入值应为0。	R/W

B[7:0]位（背景平面有效像素区域B值）

B[7:0]位设置要输出到背景平面的有效像素区域的图像数据的B值。

G[7:0]位（背景平面有效像素区域G值）

G[7:0]位设置要输出到背景平面的有效像素区域的图像数据的G值。

R[7:0]位（背景平面有效像素区域R值）

R[7:0]位设置要输出到背景平面的有效像素区域的图像数据的R值。

58.2.8 后台平面设置状态监控寄存器（BG_MON）

Address(es): GLCDC.BG_MON 400E 1018h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SWRST
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	VEN	—	—	—	—	—	—	—	EN
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	EN	后台平面运行监控	0：停止运行1：运行中。	R
b7 to b1	—	Reserved	这些位读为0。	R

Bit	Symbol	Bit name	Description	R/W
b8	VEN	Entire Module Internal Operation Reflection Control Signal Monitor	0: Signal for controlling reflection of the register values to internal operations on assertion of vertical synchronization signal is negated 1: Signal for controlling reflection of the register values to internal operations on assertion of vertical synchronization signal is asserted.	R
b15 to b9	—	Reserved	These bits are read as 0.	R
b16	SWRST	Entire Module SW Reset State Monitor	0: Entire module is in software reset state 1: Entire module is released from software reset state.	R
b31 to b17	—	Reserved	These bits are read as 0.	R

EN bit (Background Plane Operation Monitor)

The EN bit indicates whether the background plane generation module is operating or not. To stop the operation of the background plane generation module by clearing BG_EN.EN to 0, read this bit to confirm that the operation of the background plane is complete. Clearing BG_EN.EN to 0 does not stop the operation until completion of the background plane, unlike when BG_EN.SWRST is cleared to 0.

VEN bit (Entire Module Internal Operation Reflection Control Signal Monitor)

The VEN bit indicates the value of the signal for controlling reflection of the GLCDC internal register values to the internal operations. This signal is asserted at the start of a screen immediately after setting BG_EN.VEN to 1 and negated at the VE negate timing output from the background screen generation block.

SWRST bit (Entire Module SW Reset State Monitor)

The SWRST bit indicates the software reset state of the entire module when PXCLK is supplied. This bit value indicates the result of the peripheral module clock A (PCLKA) resampling the result of the pixel clock (PXCLK) sampling the BG_EN.SWRST bit. Even if PXCLK is not supplied, clearing the BG_EN.SWRST to 0 clears this bit to 0.

58.2.9 Graphics 1 Register Update Control Register (GR1_VEN) Graphics 2 Register Update Control Register (GR2_VEN)

Address(es): GLCDC.GR1_VEN 400E 1100h, GLCDC.GR2_VEN 400E 1200h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PVEN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	PVEN	Control of Graphics n Register Value Reflection to Internal Pixel Operations	0: Disable reflection of register values to internal operations on assertion of vertical synchronization signal (VS) 1: Enable reflection of register values to internal operations on assertion of the vertical synchronization signal (VS). This bit is cleared to 0 by an internal source.	R/W
b31 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

PVEN bit (Control of Graphics n Register Value Reflection to Internal Pixel Operations)

The PVEN bit enables or disables reflection of the register values to the internal operations of the pixel operation circuit on assertion of the vertical synchronization signal (input). When this bit is set to 1, the register values are immediately reflected to the internal operations on assertion of the vertical synchronization signal (input), and are automatically cleared to 0. Set this bit to 1 only when 0. Operation is not guaranteed if this bit is set to 1 when 1. Also, if the signal

Bit	Symbol	位名称	Description	R/W
b8	VEN	整个模块内部操作反射控制信号监视器	0：控制寄存器值的反射信号 垂直同步信号断言的内部操作被否定1：用于控制寄存器值反射的信号 断言垂直同步信号的内部操作被断言。	R
b15 to b9	—	Reserved	这些位读为0。	R
b16	SWRST	整个模块软件复位状态监视器	0：整个模块处于软件复位状态1：整个模块从软件复位状态释放。	R
b31 to b17	—	Reserved	这些位读为0。	R

EN位（后台平面操作监视器）

EN位指示后台平面生成模块是否正在运行。要通过将BG_EN.EN清为0来停止后台平面生成模块的操作，请读取该位以确认后台平面的操作已完成。与BG_EN.SWRST清零不同，将BG_EN.EN清零不会停止操作，直到后台平面完成。

VEN位（整个模块内部操作反射控制信号监视器）

VEN位指示用于控制GLCDC内部寄存器值反映到内部操作的信号值。该信号在将BG_EN.VEN设置为1后立即在屏幕开始时置位，并在后台屏幕生成模块的VE否定时序输出时被否定。

SWRST位（整个模块SW复位状态监视器）

SWRST位指示提供PXCLK时整个模块的软件复位状态。该位值表示外围模块时钟A(PCLKA)对像素时钟(PXCLK)对BG_EN.SWRST位进行采样的结果进行重采样的结果。即使未提供PXCLK，将BG_EN.SWRST清除为0也会将该位清除为0。

58.2.9 图形1寄存器更新控制寄存器(GR1_VEN)图形2寄存器更新控制寄存器(GR2_VEN)

Address(es): GLCDC.GR1_VEN 400E 1100h, GLCDC.GR2_VEN 400E 1200h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PVEN
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	PVEN	图形控制n将值反射注册到内部像素操作	0：禁止在垂直同步信号(VS)断言时将寄存器值反映到内部操作1：启用在垂直同步信号(VS)断言时将寄存器值反映到内部操作。该位由内部源清零。	R/W
b31 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

PVEN位（控制图形n寄存器值反映到内部像素操作）

PVEN位启用或禁用寄存器值在垂直同步信号（输入）断言时反映到像素操作电路的内部操作。当该位设置为1时，寄存器值在垂直同步信号（输入）置位时立即反映到内部操作，并自动清零。仅当为0时将该位设置为1。如果出现以下情况，则不保证操作此位在1时设置为1。此外，如果信号

output is asserted from the background plane generation module that controls reflection of the register values to the internal operations of all the modules, the register values are always reflected to the internal operations on assertion of the vertical synchronization signal (input), regardless of the value of this bit. While this bit is 1, do not modify any register whose value is reflected to the internal operations on assertion of the vertical synchronization signal (input) in this block. Otherwise, operation is not guaranteed.

This bit must not be 1 at the same time as the BG_EN.VEN bit (control of background plane register value reflection to internal operations) in the Operation Control Register (BG_EN), one of the background plane setting registers. Otherwise, operation is not guaranteed.

58.2.10 Graphics 1 Frame Buffer Read Control Register (GR1_FLMRD) Graphics 2 Frame Buffer Read Control Register (GR2_FLMRD)

Address(es): GLCDC.GR1_FLMRD 400E 1104h, GLCDC.GR2_FLMRD 400E 1204h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RENB
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	RENB	Graphics Data Read Enable	0: Disable reading 1: Enable reading. Graphics data is the frame buffer data.	R/W
b31 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: This setting is reflected to the internal operations on assertion of the vertical synchronization signal (input) when GRn_VEN.PVEN = 1 or when the register value reflection control signal to internal operations for all the modules is asserted.

RENB bit (Graphics Data Read Enable)

The RENB bit enables or disables reading of the graphics data (frame buffer data in memory connected through the GPX bus). If the current graphics data is required, data read must be enabled (GRn_FLMRD.RENB = 1) before the background panel operation is enabled, register value internal operation reflection control is enabled, or the register value internal operation reflection control of graphics 1 and 2 is enabled.

If the current graphics data is not required, data read must be disabled (GRn_FLMRD.RENB = 0) before the background panel operation is enabled, register value internal operation reflection control is enabled, or the register value internal operation reflection control of graphics 1 and 2 is enabled.

输出从后台平面生成模块断言，该模块控制寄存器值对所有模块的内部操作的反映，无论值如何，寄存器值总是在垂直同步信号（输入）断言时反映到内部操作这一点。当该位为1时，不要修改任何寄存器，其值反映到该模块中垂直同步信号（输入）置位时的内部操作。否则，无法保证操作。

该位不能与后台平面设置寄存器之一的操作控制寄存器(BG_EN)中的BG_EN.VEN位（控制后台平面寄存器值反映到内部操作）同时为1。否则，无法保证操作。

58.2.10 图形1帧缓冲区读取控制寄存器(GR1_FLMRD)图形2帧缓冲区读取控制寄存器(GR2_FLMRD)

Address(es): GLCDC.GR1_FLMRD 400E 1104h, GLCDC.GR2_FLMRD 400E 1204h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RENB
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	RENB	图形数据读取启用	0：禁用读取1：启用读取。图形数据是帧缓冲数据。	R/W
b31 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note: 此设置反映到垂直同步信号（输入）断言的内部操作时GRn_VEN.PVEN=1或当所有模块的内部操作的寄存器值反射控制信号被断言时。

RENB位（图形数据读取启用）

RENB位启用或禁用图形数据（通过GPX总线连接的内存中的帧缓冲区数据）的读取。如果需要当前图形数据，则必须在后台面板操作使能之前启用数据读取（GRn_FLMRD.RENB=1），使能寄存器值内部操作反射控制，或者图形1和2的寄存器值内部操作反射控制已启用。

如果不需要当前图形数据，则必须先禁用数据读取（GRn_FLMRD.RENB=0），然后才能启用后台面板操作，启用寄存器值内部操作反射控制，或者图形1和图形的寄存器值内部操作反射控制2已启用。

58.2.11 Graphics 1 Frame Buffer Control Register 1 (GR1_FLM1)
Graphics 2 Frame Buffer Control Register 1 (GR2_FLM1)

Address(es): GLCDC.GR1_FLM1 400E 1108h, GLCDC.GR2_FLM1 400E 1208h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	BSTMD[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bit	Symbol	Bit name	Description	R/W
b1, b0	BSTMD[1:0]	Burst Transfer Control for Graphics Data Access	b1 b0 0 0: Setting prohibited 0 1: Setting prohibited 1 0: Setting prohibited 1 1: 16-beat increment burst transfer (64-byte boundary). Graphics data is the frame buffer data.	R/W
b31 to b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: This setting is reflected to the internal operations on assertion of the vertical synchronization signal (input) when GRn_VEN.PVEN = 1 or when the register value reflection control signal to internal operations for all the modules is asserted.

BSTMD[1:0] bits (Burst Transfer Control for Graphics Data Access)

The BSTMD[1:0] bits control burst transfers for accessing the graphics data (frame buffer data in memory connected to memory through the GPX bus). In this GLCDC, these bits are fixed to 11b. Operation is not guaranteed if these bits are set to any other value.

58.2.12 Graphics 1 Frame Buffer Control Register 2 (GR1_FLM2)
Graphics 2 Frame Buffer Control Register 2 (GR2_FLM2)

Address(es): GLCDC.GR1_FLM2 400E 110Ch, GLCDC.GR2_FLM2 400E 120Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	BASE[31:16]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BASE[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b31 to b0	BASE[31:0]	Base Address for Accessing Graphics Data	Start address in the frame buffer where graphics data is to be stored. Fix GRn_FLM2.BASE[5:0] to 0 during 64-byte burst transfer.	R/W

Note: This setting is reflected to the internal operations on assertion of the vertical synchronization signal (input) when GRn_VEN.PVEN = 1 or when the register value reflection control signal to internal operations for all the modules is asserted.

58.2.11 图形1帧缓冲区控制寄存器1(GR1_FLM1)图形2帧缓冲区控制寄存器1(GR2_FLM1)

Address(es): GLCDC.GR1_FLM1 400E 1108h, GLCDC.GR2_FLM1 400E 1208h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	BSTMD[1:0]	
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1

Bit	Symbol	位名称	Description	R/W
b1, b0	BSTMD[1:0]	突发传输控制 图形数据访问	b1b000：设置禁止01：设置禁止10：设置禁止11：16节拍增量突发传输（64字节边界）。图形数据是帧缓冲数据。	R/W
b31 to b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note: 此设置反映到垂直同步信号（输入）断言的内部操作时
GRn_VEN.PVEN=1或当所有模块的内部操作的寄存器值反射控制信号被断言时。

BSTMD[1:0]位（图形数据访问的突发传输控制）

BSTMD[1:0]位控制用于访问图形数据（通过GPX总线连接到内存的内存中的帧缓冲区数据）的突发传输。在此GLCDC中，这些位固定为11b。如果这些位设置为任何其他值，则无法保证操作。

58.2.12 图形1帧缓冲区控制寄存器2(GR1_FLM2)图形2帧缓冲区控制寄存器2(GR2_FLM2)

Address(es): GLCDC.GR1_FLM2 400E 110Ch, GLCDC.GR2_FLM2 400E 120Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	BASE[31:16]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	BASE[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b31 to b0	BASE[31:0]	访问的基地址 图形数据	帧缓冲区中要存储图形数据的起始地址。在64字节突发传输期间将GRn_FLM2.BASE[5:0]修复为0。	R/W

Note: 此设置反映到垂直同步信号（输入）断言的内部操作时
GRn_VEN.PVEN=1或当所有模块的内部操作的寄存器值反射控制信号被断言时。

BASE[31:0] bits (Base Address for Accessing Graphics Data)

The BASE[31:0] bits specify the base address (start address in the first frame buffer) for graphics data access. Because the GLCDC only supports the 16-beat increment burst transfer mode, in which data is aligned with a 64-byte boundary, the lower 6 bits (GRn_FLM2.BASE[5:0]) must be fixed to 0.

58.2.13 Graphics 1 Frame Buffer Control Register 3 (GR1_FLM3)
Graphics 2 Frame Buffer Control Register 3 (GR2_FLM3)

Address(es): GLCDC.GR1_FLM3 400E 1110h, GLCDC.GR2_FLM3 400E 1210h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	LNOFF[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b15 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b31 to b16	LNOFF[15:0]	Macro Line Offset Address for Accessing Graphics Data	Macro line offset address for accessing graphics data (frame buffer data). Signed, 16-bit integer.	R/W

Note: This setting is reflected to the internal operations on assertion of the vertical synchronization signal (input) when GRn_VEN.PVEN = 1 or when the register value reflection control signal to internal operations for all the modules is asserted.

LNOFF[15:0] bits (Macro Line Offset Address for Accessing Graphics Data)

The LNOFF[15:0] bits specify the macro line offset address for accessing graphics data (offset to be added to the current address at the macro line end for calculating the start address of the next macro line). Because the GLCDC only supports the 16-beat increment burst transfer mode, in which data is aligned with a 64-byte boundary, the lower 6 bits (GRn_FLM3.LNOFF[5:0]) must be fixed to 0.

BASE[31:0]位（访问图形数据的基地址）

BASE[31:0]位指定图形数据访问的基地址（第一个帧缓冲区中的起始地址）。由于GLCDC仅支持16拍增量突发传输模式，其中数据与64字节边界对齐，因此低6位(GRn_FLM2.BASE[5:0])必须固定为0。

58.2.13 图形1帧缓冲区控制寄存器3(GR1_FLM3)图形2帧缓冲区控制寄存器3(GR2_FLM3)

Address(es): GLCDC.GR1_FLM3 400E 1110h, GLCDC.GR2_FLM3 400E 1210h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	LNOFF[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b15 to b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b31 to b16	LNOFF[15:0]	宏行偏移地址 访问图形数据	访问图形数据（帧缓冲数据）的宏行偏移地址。有符号的16位整数。	R/W

Note: 此设置反映到垂直同步信号（输入）断言的内部操作时GRn_VEN.PVEN=1或当所有模块的内部操作的寄存器值反射控制信号被断言时。

LNOFF[15:0]位（用于访问图形数据的宏行偏移地址）

LNOFF[15:0]位指定访问图形数据的宏行偏移地址（在宏行结束时添加到当前地址的偏移，用于计算下一个宏行的起始地址）。由于GLCDC仅支持16拍增量突发传输模式，其中数据与64字节边界对齐，因此低6位(GRn_FLM3.LNOFF[5:0])必须固定为0。

58.2.14 Graphics 1 Frame Buffer Control Register 5 (GR1_FLM5)
Graphics 2 Frame Buffer Control Register 5 (GR2_FLM5)

Address(es): GLCDC.GR1_FLM5 400E 1118h, GLCDC.GR2_FLM5 400E 1218h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	LNNUM[10:0]										
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	DATANUM[15:0]															
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b15 to b0	DATANUM[15:0]	Number of Data Transfer Times Per Line for Accessing Graphics Data	Number of data transfers per macro line for accessing graphics data (frame buffer data), where one transfer is defined as 16-beat burst access (64-byte boundary). 0000h: Once : FFFFh: 65536 times.	R/W
b26 to b16	LNNUM[10:0]	Number of Lines Per Frame for Accessing Graphics Data	Number of macro lines per frame for accessing graphics data (frame buffer data). 000h: 1 macro line : 3FBh: 1020 macro lines. Other settings are prohibited.	R/W
b31 to b27	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: This setting is reflected to the internal operations on assertion of the vertical synchronization signal (input) when GRn_VEN.PVEN = 1 or when the register value reflection control signal to internal operations for all the modules is asserted.

DATANUM[15:0] bits (Number of Data Transfer Times Per Line for Accessing Graphics Data)

The DATANUM[15:0] bits specify the number of data transfers per macro line for accessing graphics data, where one transfer is defined as a 16-beat burst access through the GPX bus. For all the data transfers, at least 2 bytes of valid pixel data are required (16 pixels in LUT1 format and 16 pixels or more in the other formats). If the number of bytes per macro line cannot be divided by 64 (4 bytes × 16-beat), DATANUM is obtained by rounding up to the whole number.

LNNUM[10:0] bits (Number of Lines Per Frame for Accessing Graphics Data)

The LNNUM[10:0] bits specify the number of lines per frame for accessing graphics data. When graphics data for the number of lines set to these bits is read, it signals the end of the frame and the base address is loaded.

The following are two use cases for macro lines. In these use cases, the frame size is 480 pixels × 272 lines and the pixel format is RGB565 (16 bpp).

Case 1) One macro line is configured to be equivalent to the frame raster width. The number of macro lines is equivalent to the number of vertical lines.

DATANUM: 000Eh (15 times = 16 × 480 / 512)
LNNUM: 10Fh (272 macro lines = 272 / 1)

Case 2) One macro line is configured to be repeated during the display frame. The number of macro lines is not equivalent to the number of vertical lines. In the example, one macro line has 16 times the raster width.

DATANUM: 00EFh (240 times = 16 × 480 / 512 × 16)
LNNUM: 010h (17 macro lines = 272 / 16)

58.2.14 图形1帧缓冲区控制寄存器5(GR1_FLM5)图形2帧缓冲区控制寄存器5(GR2_FLM5)

Address(es): GLCDC.GR1_FLM5 400E 1118h, GLCDC.GR2_FLM5 400E 1218h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	LNNUM[10:0]										
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	DATANUM[15:0]															
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b15 to b0	DATANUM[15:0]	每行的数据传输次数 访问图形数据	用于访问图形数据（帧缓冲区数据）的每条宏线的数据传输次数，其中一次传输定义为16拍突发访问（64字节边界）。0000h：一次 : FFFFh: 65536 times.	R/W
b26 to b16	LNNUM[10:0]	每帧访问的行数 图形数据	用于访问图形数据（帧缓冲区数据）的每帧宏行数。000h：1条宏线 :3FBh:1020宏线。禁止其他设置。	R/W
b31 to b27	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note: 此设置反映到垂直同步信号（输入）断言的内部操作时
GRn_VEN.PVEN=1或当所有模块的内部操作的寄存器值反射控制信号被断言时。

DATANUM[15:0]位（访问图形数据的每行数据传输次数）

DATANUM[15:0]位指定用于访问图形数据的每条宏线的数据传输次数，其中一次传输定义为通过GPX总线的16拍突发访问。对于所有数据传输，至少需要2个字节的有效像素数据（LUT1格式为16个像素，其他格式为16个或更多像素）。如果每个宏行的字节数不能除以64（4字节×16-beat），则通过四舍五入获得DATANUM。

LNNUM[10:0]位（访问图形数据的每帧行数）

LNNUM[10:0]位指定用于访问图形数据的每帧的行数。当读取设置为这些位的行数的图形数据时，它表示帧结束并加载基地址。

以下是宏行的两个用例。在这些用例中，帧大小为480像素×272行，像素格式为RGB565(16bpp)。

案例1)一条宏线被配置为与帧光栅宽度相等。宏行数等于垂直行数。

DATANUM: 000Eh (15 times = 16 × 480 / 512)
LNNUM：10Fh（272宏行=2721）

情况2)一个宏行被配置为在显示帧期间重复。宏行数不等于垂直行数。在该示例中，一条宏线具有光栅宽度的16倍。

DATANUM: 00EFh (240 times = 16 × 480 / 512 × 16)
LNNUM：010h（17行宏=27216）

58.2.15 Graphics 1 Frame Buffer Control Register 6 (GR1_FLM6) Graphics 2 Frame Buffer Control Register 6 (GR2_FLM6)

Address(es): GLCDC.GR1_FLM6 400E 111Ch, GLCDC.GR2_FLM6 400E 121Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	FORMAT[2:0]			—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b27 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b30 to b28	FORMAT[2:0]	Data Format for Accessing Graphics Data	Data format for accessing graphics data (frame buffer data). b30 b28 0 0 0: RGB565 (16 bits/pixel) 0 0 1: RGB888 (32 bits/pixel, 8 bits on the MSB side are invalid) 0 1 0: ARGB1555 (16 bits/pixel, 1 bit of A is LUT data) 0 1 1: ARGB4444 (16 bits/pixel) 1 0 0: ARGB8888 (32 bits/pixel) 1 0 1: CLUT8 (8 bits/pixel) 1 1 0: CLUT4 (4 bits/pixel) 1 1 1: CLUT1 (1 bit/pixel).	R/W
b31	—	Reserved	This bit is read as 0. The write value should be 0.	R/W

Note: This setting is reflected to the internal operations on assertion of the vertical synchronization signal (input) when GRn_VEN.PVEN = 1 or when the register value reflection control signal to internal operations for all the modules is asserted.

FORMAT[2:0] bits (Data Format for Accessing Graphics Data)

The FORMAT[2:0] bits specify the data format for accessing graphics data. CLUT1, CLUT4, CLUT8 contain the addresses 01h or 00h, 0Fh to 00h, and FFh to 00h, respectively, for accessing the color palette. ARGB1555 contains the address for accessing the color palette (80h or 00h) in the MSB and RGB data in the other bits. ARGB8888 and ARGB4444 contain the upper 8-bit or 4-bit alpha blending values and RGB data. RGB888 and RGB565 contain RGB data only.

58.2.15 图形1帧缓冲区控制寄存器6(GR1_FLM6)图形2帧缓冲区控制寄存器6(GR2_FLM6)

Address(es): GLCDC.GR1_FLM6 400E 111Ch, GLCDC.GR2_FLM6 400E 121Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	FORMAT[2:0]			—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b27 to b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b30 to b28	FORMAT[2:0]	访问数据格式 图形数据	用于访问图形数据（帧缓冲区数据）的数据格式。b30b28 00：RGB565（16位像素）001：RGB888（32位像素，MSB侧8位无效）010：ARGB1555（16位像素，A的1位为LUT数据）011：ARGB4444（16位像素）100：ARGB8888（32位像素）101：CLUT8（8位像素）110：CLUT4（4位像素）111：CLUT1（1位像素）。	R/W
b31	—	Reserved	该位读取为0。写入值应为0。	R/W

Note: 此设置反映到垂直同步信号（输入）断言的内部操作时
GRn_VEN.PVEN=1或当所有模块的内部操作的寄存器值反射控制信号被断言时。

FORMAT[2:0]位（访问图形数据的数据格式）

FORMAT[2:0]位指定访问图形数据的数据格式。CLUT1、CLUT4、CLUT8分别包含地址01h或00h、0Fh到00h和FFh到00h，用于访问调色板。ARGB1555在MSB中包含用于访问调色板（80h或00h）的地址，在其他位中包含RGB数据。ARGB8888和ARGB4444包含高8位或4位alpha混合值和RGB数据。RGB888和RGB565仅包含RGB数据。

58.2.16 Graphics 1 Alpha Blending Control Register 1 (GR1_AB1)
Graphics 2 Alpha Blending Control Register 1 (GR2_AB1)

Address(es): GLCDC.GR1_AB1 400E 1120h, GLCDC.GR2_AB1 400E 1220h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	ARCON	—	—	—	ARCDISPON	—	—	—	GRCDISPON	—	—	DISPSEL[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	DISPSEL[1:0]	Graphics Display Plane Control	b1 b0 0 0: Background color display (value set in the GRn_BASE register) 0 1: Lower-layer graphics display 1 0: Current graphics display 1 1: Blended display of lower-layer graphics (input image from the previous stage) and current graphics (data read from the GPX bus).	R/W
b3, b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	GRCDISPON	Graphics Image Area Border Display Control	0: Turn display off 1: Turn display on.	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	ARCDISPON	Image Area Border Display Control for Rectangular Area Alpha Blending	0: Turn display off 1: Turn display on.	R/W
b11 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b12	ARCON	Rectangular Area Alpha Blending Control	0: Turn blending off 1: Turn blending on.	R/W
b31 to b13	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: This setting is reflected to the internal operations on assertion of the vertical synchronization signal (input) when GRn_VEN.PVEN = 1 or when the register value reflection control signal to internal operations for all the modules is asserted.

DISPSEL[1:0] bits (Graphics Display Plane Control)

The DISPSEL[1:0] bits control the graphics display plane. When the plane is selected as the lower-layer graphics, the image input from the previous stage is displayed (the background plane for GR1, and output from GR1 for GR2); as the background color, the background color specified in the GLCDC registers is displayed; and as the current graphics, the ARGB8888 data obtained by expanding the graphics data read by the GLCDC from the GPX bus is displayed. When the current graphics display is selected (these bits are set to 10b), RGB888 data is displayed, regardless of the alpha blending value in the pixel. Table 58.8 and Figure 58.10 show the relationship between the register setting and display area.

GRCDISPON bit (Graphics Image Area Border Display Control)

The GRCDISPON bit turns on or off the border display for the graphics image area. When the display is turned on (this bit is set to 1), the graphics image area is bordered with the preset color. The border is 1 pixel wide on the outermost periphery of the area with the display data set as FFh for each RGB color.

ARCDISPON bit (Image Area Border Display Control for Rectangular Area Alpha Blending)

The ARCDISPON bit turns on or off the border display for the image area where rectangular area alpha blending is performed. When the display is turned on (this bit is set to 1), the image area for the rectangular alpha blending is bordered with the preset color. The border is 1 pixel wide on the outermost periphery of the area and the display data set

58.2.16 图形1Alpha混合控制寄存器1(GR1_AB1)图形2Alpha混合控制寄存器1(GR2_AB1)

Address(es): GLCDC.GR1_AB1 400E 1120h, GLCDC.GR2_AB1 400E 1220h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	ARCON	—	—	—	ARCDISPON	—	—	—	GRCDISPON	—	—	DISPSEL[1:0]	
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b1, b0	DISPSEL[1:0]	图形显示平面 Control	b1b000：背景色显示（GRn_BASE寄存器中设置的值）01：下层图形显示10：当前图形显示11：下层图形（前一阶段的输入图像）和当前图形混合显示图形（从GPX总线读取的数据）。	R/W
b3, b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b4	GRCDISPON	图形图像区域边框显示控件	0：关闭显示1：打开显示。	R/W
b7 to b5	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b8	ARCDISPON	图像区域边框显示控件 矩形区域Alpha Blending	0：关闭显示1：打开显示。	R/W
b11 to b9	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b12	ARCON	矩形区域Alpha混合控制	0：关闭混合1：打开混合。	R/W
b31 to b13	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note: 此设置反映到垂直同步信号（输入）断言的内部操作时
GRn_VEN.PVEN=1或当所有模块的内部操作的寄存器值反射控制信号被断言时。

DISPSEL[1:0]位（图形显示平面控制）

DISPSEL[1:0]位控制图形显示平面。选择平面作为下层图形时，显示上一阶段输入的图像（GR1为背景平面，GR2为GR1输出）；作为背景颜色，显示在GLCDC寄存器中指定的背景颜色；将GLCDC从GPX总线读取的图形数据展开后得到的ARGB8888数据作为当前图形显示。选择当前图形显示时（这些位设置为10b），无论像素中的alpha混合值如何，都会显示RGB888数据。表58.8和图58.10显示了寄存器设置和显示区域之间的关系。

GRCDISPON位（图形图像区域边框显示控制）

GRCDISPON位打开或关闭图形图像区域的边框显示。开启显示时（该位设置为1），图形图像区域以预设颜色为边框。该区域最外围的边界为1个像素宽，显示数据设置为每种RGB颜色的FFh。

ARCDISPON位（矩形区域Alpha混合的图像区域边框显示控制）

ARCDISPON位打开或关闭执行矩形区域Alpha混合的图像区域的边框显示。当显示器打开时（该位设置为1），矩形alpha混合的图像区域以预设颜色为边框。区域最外围1像素宽的边框和显示数据集

as FFh for each RGB color.

ARCON bit (Rectangular Area Alpha Blending Control)

The ARCON bit turns on or off alpha blending in a rectangular area. When alpha blending is turned on (this bit is set to 1), pixels are processed in accordance with the alpha blending control specified in the relevant registers for the specified rectangular area, not in accordance with the alpha value input from the graphics data interface for each pixel. In the areas outside the rectangular area in the graphics area, pixels are processed in accordance with the alpha value input from the graphics data interface for each pixel.

Table 58.8 Display selections

GRn_AB1. DISPSEL[1:0] (display plane)	GRn_AB1. ARCON (rectangular)	GRn_AB7. CKON (chroma key)	Within rectangular alpha blending area	Outside rectangular alpha blending area within graphics area	Outside graphics area within display area	Outside display area
00b	0	0	-	Background color	Background color	Lower layer R = G = B = 00h
01b	0	0	-	Lower layer	Lower layer	Lower layer R = G = B = 00h
10b	0	0	-	Current	Background color	Lower layer R = G = B = 00h
11b	0	0	-	Current + alpha blending in pixel units	Lower layer	Lower layer R = G = B = 00h
11b	0	1	-	Current + RGB-index chroma key + alpha blending in pixel units	Lower layer	Lower layer R = G = B = 00h
11b	1	0	Current + rectangular alpha blending	Current + alpha blending in pixel units	Lower layer	Lower layer R = G = B = 00h
11b	1	1	Current + rectangular alpha blending	Current + RGB-index chroma key + alpha blending in pixel units	Lower layer	Lower layer R = G = B = 00h

Note: Operation is not guaranteed when any other value is set.

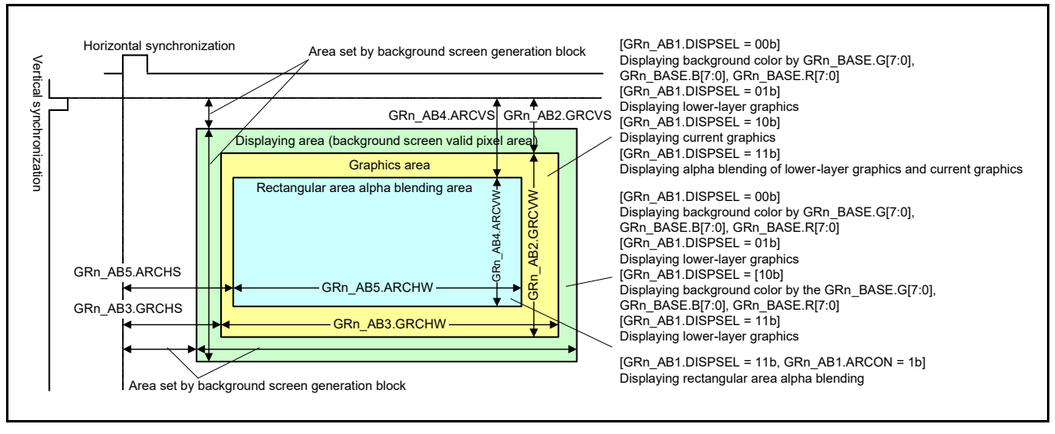


Figure 58.10 Selection of graphics display plane

作为每种RGB颜色的FFh。

ARCON位（矩形区域Alpha混合控制）

ARCON位打开或关闭矩形区域中的alpha混合。开启alphablending时（该位设置为1），像素按照指定矩形区域的相关寄存器中指定的alphablending控制进行处理，而不是按照从图形数据接口输入的alpha值进行处理。每个像素。在图形区域的矩形区域以外的区域，按照每个像素从图形数据接口输入的阿尔法值对像素进行处理。

Table 58.8 显示选择

GRn_AB1. DISPSEL[1:0] (display plane)	GRn_AB1. ARCON (rectangular)	GRn_AB7. CKON (chroma key)	在矩形Alpha混合区域内	图形区域内的外部矩形Alpha混合区域	显示区域内的外部图形区域	外展区
00b	0	0	-	背景颜色	背景颜色	下层 R = G = B = 00h
01b	0	0	-	下层	下层	下层 R = G = B = 00h
10b	0	0	-	Current	背景颜色	下层 R = G = B = 00h
11b	0	0	-	以像素为单位的电流+alpha混合	下层	下层 R = G = B = 00h
11b	0	1	-	当前+RGB索引色度键+以像素为单位的alpha混合	下层	下层 R = G = B = 00h
11b	1	0	当前+矩形Alpha混合	以像素为单位的电流+alpha混合	下层	下层 R = G = B = 00h
11b	1	1	当前+矩形Alpha混合	当前+RGB索引色度键+以像素为单位的alpha混合	下层	下层 R = G = B = 00h

Note: 当设置任何其他值时，不保证操作。

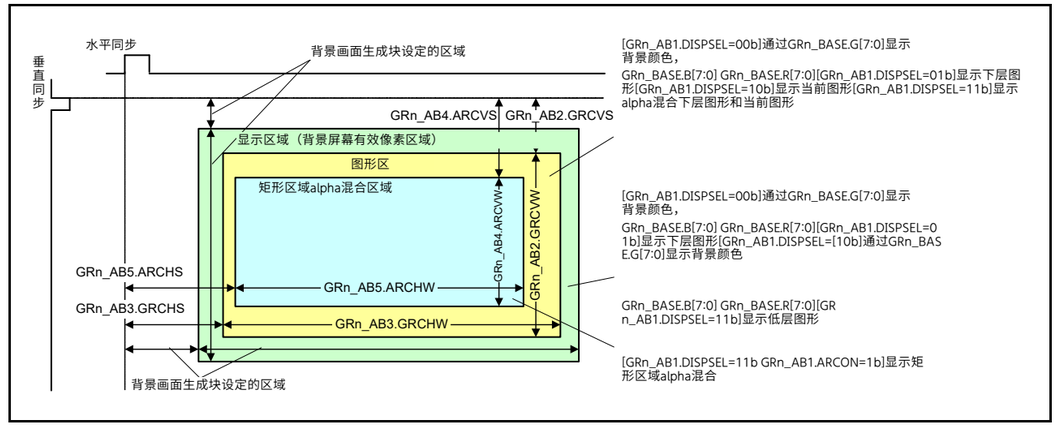


Figure 58.10 图形显示平面的选择

58.2.17 Graphics 1 Alpha Blending Control Register 2 (GR1_AB2) Graphics 2 Alpha Blending Control Register 2 (GR2_AB2)

Address(es): GLCDC.GR1_AB2 400E 1124h, GLCDC.GR2_AB2 400E 1224h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	GRCVS[10:0]										
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	GRCVW[10:0]										
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b10 to b0	GRCVW[10:0]	Vertical Width of Graphics Image Area	Width in lines. 010h: 16 lines : 3FCh: 1020 lines. Other settings are prohibited.	R/W
b15 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b26 to b16	GRCVS[10:0]	Vertical Start Position of Graphics Image Area	Position in lines. 002h: 2nd line : 3EEh: 1006th line. Other settings are prohibited.	R/W
b31 to b27	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: This setting is reflected to the internal operations on assertion of the vertical synchronization signal (input) when GRn_VEN.PVEN = 1 or when the register value reflection control signal to internal operations for all the modules is asserted.

GRCVW[10:0] bits (Vertical Width of Graphics Image Area)

The GRCVW[10:0] bits specify the vertical width of the graphics image area.

GRCVS[10:0] bits (Vertical Start Position of Graphics Image Area)

The GRCVS[10:0] bits specify the vertical start position of the graphics image area, in reference to assertion of the vertical synchronization signal (VS). For the relationship with the graphics display plane, see Figure 58.10.

58.2.17 图形1Alpha混合控制寄存器2(GR1_AB2)图形2Alpha混合控制寄存器2(GR2_AB2)

Address(es): GLCDC.GR1_AB2 400E 1124h, GLCDC.GR2_AB2 400E 1224h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	GRCVS[10:0]										
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	GRCVW[10:0]										
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b10 to b0	GRCVW[10:0]	图形的垂直宽度 图像区	线宽。010h ：16行 :3FCh:1020行。禁止其他设置。	R/W
b15 to b11	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b26 to b16	GRCVS[10:0]	垂直起始位置 图形图像区	排成一行。002 h：第二行 :3EEh:第1006行。禁止其他设置。	R/W
b31 to b27	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note: 此设置反映到垂直同步信号（输入）断言的内部操作时
GRn_VEN.PVEN=1或当所有模块的内部操作的寄存器值反射控制信号被断言时。

GRCVW[10:0]位（图形图像区域的垂直宽度）

GRCVW[10:0]位指定图形图像区域的垂直宽度。

GRCVS[10:0]位（图形图像区域的垂直起始位置）

GRCVS[10:0]位指定图形图像区域的垂直起始位置，参考垂直同步信号(VS)的断言。与图形显示平面的关系见图58.10。

58.2.18 Graphics 1 Alpha Blending Control Register 3 (GR1_AB3) Graphics 2 Alpha Blending Control Register 3 (GR2_AB3)

Address(es): GLCDC.GR1_AB3 400E 1128h, GLCDC.GR2_AB3 400E 1228h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	GRCHS[10:0]										
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	GRCHW[10:0]										
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b10 to b0	GRCHW[10:0]	Horizontal Width of Graphics Image Area	Width in pixels. 010h: 16 pixels : 3F8h: 1016 pixels. Other settings are prohibited.	R/W
b15 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b26 to b16	GRCHS[10:0]	Horizontal Start Position of Graphics Image Area	Position in pixels. 005h: 5th pixel : 3EDh: 1005th pixel. Other settings are prohibited.	R/W
b31 to b27	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: This setting is reflected to the internal operations on assertion of the vertical synchronization signal (input) when GRn_VEN.PVEN = 1 or when the register value reflection control signal to internal operations for all the modules is asserted.

GRCHW[10:0] bits (Horizontal Width of Graphics Image Area)

The GRCHW[10:0] bits specify the horizontal width of the graphics image area.

GRCHS[10:0] bits (Horizontal Start Position of Graphics Image Area)

The GRCHS[10:0] bits specify the horizontal start position of the graphics image area, in reference to assertion of the horizontal synchronization signal (VS). For the relationship with the graphics display plane, see Figure 58.10.

58.2.18 图形1Alpha混合控制寄存器3(GR1_AB3)图形2Alpha混合控制寄存器3(GR2_AB3)

Address(es): GLCDC.GR1_AB3 400E 1128h, GLCDC.GR2_AB3 400E 1228h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	GRCHS[10:0]										
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	GRCHW[10:0]										
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b10 to b0	GRCHW[10:0]	水平宽度 图形图像区	以像素为单位的宽度。010h：16像素 :3F8h:1016像素。禁止其他设置。	R/W
b15 to b11	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b26 to b16	GRCHS[10:0]	的水平起始位置 图形图像区	以像素为单位的位置。 005h：第5个像素 :3EDh:第1005个像素。禁止其他设置。	R/W
b31 to b27	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note: 此设置反映到垂直同步信号（输入）断言的内部操作时
GRn_VEN.PVEN=1或当所有模块的内部操作的寄存器值反射控制信号被断言时。

GRCHW[10:0]位（图形图像区域的水平宽度）

GRCHW[10:0]位指定图形图像区域的水平宽度。

GRCHS[10:0]位（图形图像区域的水平起始位置）

GRCHS[10:0]位指定图形图像区域的水平起始位置，参考水平同步信号(VS)的断言。与图形显示平面的关系见图58.10。

58.2.19 Graphics 1 Alpha Blending Control Register 4 (GR1_AB4) Graphics 2 Alpha Blending Control Register 4 (GR2_AB4)

Address(es): GLCDC.GR1_AB4 400E 112Ch, GLCDC.GR2_AB4 400E 122Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	ARCVS[10:0]										
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	ARCVW[10:0]										
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b10 to b0	ARCVW[10:0]	Vertical Width of Rectangular Area Alpha Blending Image Area	Width in lines. 001h: 1 line : 3FCh: 1020 lines. Other settings are prohibited.	R/W
b15 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b26 to b16	ARCVS[10:0]	Vertical Start Position of Rectangular Area Alpha Blending Image Area	Position in lines. 002h: 2nd line : 3EEh: 1006th line. Other settings are prohibited.	R/W
b31 to b27	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: This setting is reflected to the internal operations on assertion of the vertical synchronization signal (input) when GRn_VEN.PVEN = 1 or when the register value reflection control signal to internal operations for all the modules is asserted.

ARCVW[10:0] bits (Vertical Width of Rectangular Area Alpha Blending Image Area)

The ARCVW[10:0] bits specify the vertical width of the rectangular area alpha blending image area.

ARCVS[10:0] bits (Vertical Start Position of Rectangular Area Alpha Blending Image Area)

The ARCVS[10:0] bits specify the vertical start position of the rectangular area alpha blending image area, in reference to assertion of the vertical synchronization signal (VS). For the relationship with the graphics display plane, see Figure 58.10.

58.2.19 图形1Alpha混合控制寄存器4(GR1_AB4)图形2Alpha混合控制寄存器4(GR2_AB4)

Address(es): GLCDC.GR1_AB4 400E 112Ch, GLCDC.GR2_AB4 400E 122Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	ARCVS[10:0]										
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	ARCVW[10:0]										
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b10 to b0	ARCVW[10:0]	垂直宽度 矩形区域Alpha 混合图像区域	线宽。001h ：1行 :3FCh:1020行。禁止其他设置。	R/W
b15 to b11	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b26 to b16	ARCVS[10:0]	矩形区域Alpha的垂直起始位置 混合图像区域	排成一行。002 h：第二行 :3EEh:第1006行。禁止其他设置。	R/W
b31 to b27	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note: 此设置反映到垂直同步信号（输入）断言的内部操作时
GRn_VEN.PVEN=1或当所有模块的内部操作的寄存器值反射控制信号被断言时。

ARCVW[10:0]位（矩形区域Alpha混合图像区域的垂直宽度）

ARCVW[10:0]位指定矩形区域alpha混合图像区域的垂直宽度。

ARCVS[10:0]位（矩形区域Alpha混合图像区域的垂直起始位置）

ARCVS[10:0]位指定矩形区域alpha混合图像区域的垂直起始位置，参考垂直同步信号(VS)的断言。与图形显示平面的关系见图58.10。

58.2.20 Graphics 1 Alpha Blending Control Register 5 (GR1_AB5)
Graphics 2 Alpha Blending Control Register 5 (GR2_AB5)

Address(es): GLCDC.GR1_AB5 400E 1130h, GLCDC.GR2_AB5 400E 1230h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	ARCHS[10:0]										
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	ARCHW[10:0]										
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b10 to b0	ARCHW[10:0]	Horizontal Width of Rectangular Area Alpha Blending Image Area	Width in pixels. 001h: 1 pixel : 3F8h: 1016 pixels. Other settings are prohibited.	R/W
b15 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b26 to b16	ARCHS[10:0]	Horizontal Start Position of Rectangular Area Alpha Blending Image Area	Position in pixels. 005h: 5th pixel : 3EDh: 1005th pixel. Other settings are prohibited.	R/W
b31 to b27	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: This setting is reflected to the internal operations on assertion of the vertical synchronization signal (input) when GRn_VEN.PVEN = 1 or when the register value reflection control signal to internal operations for all the modules is asserted.

ARCHW[10:0] bits (Horizontal Width of Rectangular Area Alpha Blending Image Area)

The ARCHW[10:0] bits specify the horizontal width of the rectangular area alpha blending image area.

ARCHS[10:0] bits (Horizontal Start Position of Rectangular Area Alpha Blending Image Area)

The ARCHS[10:0] bits specify the horizontal start position of the rectangular area alpha blending image area, in reference to assertion of the horizontal synchronization signal (HS). For the relationship with the graphics display plane, see Figure 58.10.

58.2.20 图形1Alpha混合控制寄存器5(GR1_AB5)图形2Alpha混合控制寄存器5(GR2_AB5)

Address(es): GLCDC.GR1_AB5 400E 1130h, GLCDC.GR2_AB5 400E 1230h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	ARCHS[10:0]										
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	ARCHW[10:0]										
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b10 to b0	ARCHW[10:0]	水平宽度 矩形区域Alpha 混合图像区域	以像素为单位的宽度。001h：1像素 :3F8h:1016像素。禁止其他设置。	R/W
b15 to b11	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b26 to b16	ARCHS[10:0]	的水平起始位置 矩形区域Alpha 混合图像区域	以像素为单位的位置。 005h：第5个像素 :3EDh:第1005个像素。禁止其他设置。	R/W
b31 to b27	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note: 此设置反映到垂直同步信号（输入）断言的内部操作时
GRn_VEN.PVEN=1或当所有模块的内部操作的寄存器值反射控制信号被断言时。

ARCHW[10:0]位（矩形区域Alpha混合图像区域的水平宽度）

ARCHW[10:0]位指定矩形区域alpha混合图像区域的水平宽度。

ARCHS[10:0]位（矩形区域Alpha混合图像区域的水平起始位置）

ARCHS[10:0]位指定矩形区域alpha混合图像区域的水平起始位置，参考水平同步信号(HS)的断言。与图形显示平面的关系见图58.10。

58.2.21 Graphics 1 Alpha Blending Control Register 6 (GR1_AB6)
Graphics 2 Alpha Blending Control Register 6 (GR2_AB6)

Address(es): GLCDC.GR1_AB6 400E 1134h, GLCDC.GR2_AB6 400E 1234h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	ARCCOEF[8:0]								
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	ARCRATE[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	ARCRATE[7:0]	Frame Rate for Alpha Blending in Rectangular Area	00h: 1 frame : FFh: 256 frames.	R/W
b15 to b8	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b24 to b16	ARCCOEF[8:0]	Alpha Coefficient for Alpha Blending in Rectangular Area	Valid settings: -255 to 255. Bit [8]: Sign 0: Add 1: Subtract. Bits [7:0]: Variation, as an absolute value.	R/W
b31 to b25	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: This setting is reflected to the internal operations on assertion of the vertical synchronization signal (input) when GRn_VEN.PVEN = 1 or when the register value reflection control signal to internal operations for all the modules is asserted.

ARCRATE[7:0] bits (Frame Rate for Alpha Blending in Rectangular Area)

The ARCRATE[7:0] bits specify the frame rate for alpha blending in a rectangular area.

ARCCOEF[8:0] bits (Alpha Coefficient for Alpha Blending in Rectangular Area)

The ARCCOEF[8:0] bits specify the alpha coefficient for alpha blending in a rectangular area.

In alpha blending in a rectangular area, current graphics are faded in or out with the GRn_AB7.ARCDEF[7:0], GRn_AB6.ARCCOEF[8:0], and GRn_AB6.ARCRATE[7:0] settings. If the alpha value is set in the GR_ARC_DEF[7:0] bits, the GR_ARC_DEF[7:0] bits and the alpha blending in a rectangular area are turned on. Each time the vertical synchronization signal (VS) rises the number of times set in the GR_ARC_RATE[7:0] bits, the value in GR_ARC_COEF[8:0] is added to or subtracted from the alpha value. Figure 58.11 shows change in the alpha value.

58.2.21 图形1Alpha混合控制寄存器6(GR1_AB6)图形2Alpha混合控制寄存器6(GR2_AB6)

Address(es): GLCDC.GR1_AB6 400E 1134h, GLCDC.GR2_AB6 400E 1234h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	ARCCOEF[8:0]								
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	ARCRATE[7:0]							
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b7 to b0	ARCRATE[7:0]	Alpha的帧速率 混合矩形 Area	00h: 1 frame : FFh: 256 frames.	R/W
b15 to b8	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b24 to b16	ARCCOEF[8:0]	Alpha的Alpha系数 混合矩形 Area	有效设置：-255到255。 Bit[8]：符号0：加1：减。位[7:0]：变化，作为绝对值。	R/W
b31 to b25	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note: 此设置反映到垂直同步信号（输入）断言的内部操作时
GRn_VEN.PVEN=1或当所有模块的内部操作的寄存器值反射控制信号被断言时。

ARCRATE[7:0]位（矩形区域中Alpha混合的帧速率）

ARCRATE[7:0]位指定矩形区域中alpha混合的帧速率。

ARCCOEF[8:0]位（矩形区域中Alpha混合的Alpha系数）

ARCCOEF[8:0]位指定矩形区域中alpha混合的alpha系数。

在矩形区域的alpha混合中，当前图形使用GRn_AB7.ARCDEF[7:0]淡入或淡出，GRn_AB6.ARCCOEF[8:0]和GRn_AB6.ARCRATE[7:0]设置。如果在GR_ARC_DEF[7:0]位中设置了alpha值，则GR_ARC_DEF[7:0]位和矩形区域中的alpha混合将打开。每次垂直同步信号(VS)上升GR_ARC_RATE[7:0]位中设置的次数时，都会将GR_ARC_COEF[8:0]中的值添加到alpha值或从alpha值中减去。图58.11显示了alpha值的变化。

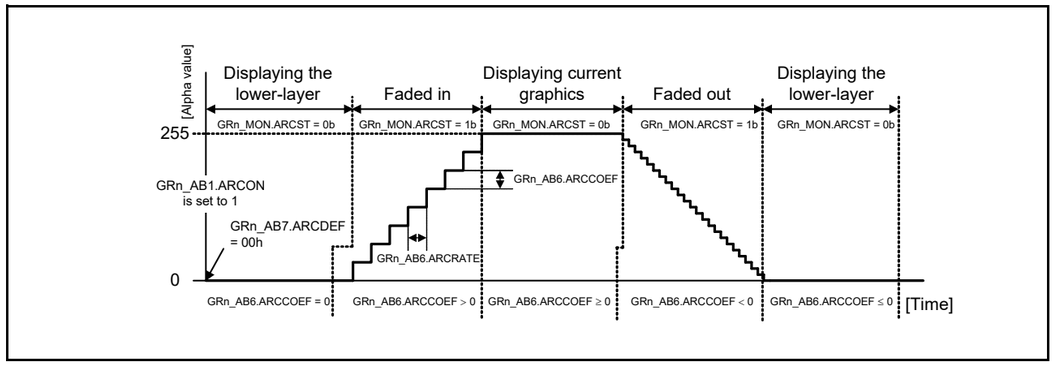


Figure 58.11 Changes in alpha value

58.2.22 Graphics 1 Alpha Blending Control Register 7 (GR1_AB7) Graphics 2 Alpha Blending Control Register 7 (GR2_AB7)

Address(es): GLCDC.GR1_AB7 400E 1138h, GLCDC.GR2_AB7 400E 1238h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	ARCDEF[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CKON
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	CKON	RGB-Index Chroma-Key Processing Control	0: Disable chroma-key processing 1: Enable chroma-key processing.	R/W
b15 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b23 to b16	ARCDEF[7:0]	Initial Alpha Value for Alpha Blending in Rectangular Area	Initial alpha value for alpha blending in rectangular area.	R/W
b31 to b24	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: This setting is reflected to the internal operations on assertion of the vertical synchronization signal (input) when GRn_VEN.PVEN = 1 or when the register value reflection control signal to internal operations for all the modules is asserted.

CKON bit (RGB-Index Chroma-Key Processing Control)

The CKON bit turns RGB-index chroma-key processing on or off. This function is enabled only if this bit is 1 when the graphics display plane is the blended display (GRn_AB1.DISPSEL[1:0] = 11b). And it is reflected to the graphics area except alpha blending in a rectangular area. For details, see Table 58.8.

ARCDEF[7:0] bits (Initial Alpha Value for Alpha Blending in Rectangular Area)

The ARCDEF[7:0] bits specify the initial alpha value for alpha blending in a rectangular area. For changes in the alpha value during fade-in or fade-out of the current graphics using this bit, see Figure 58.11.

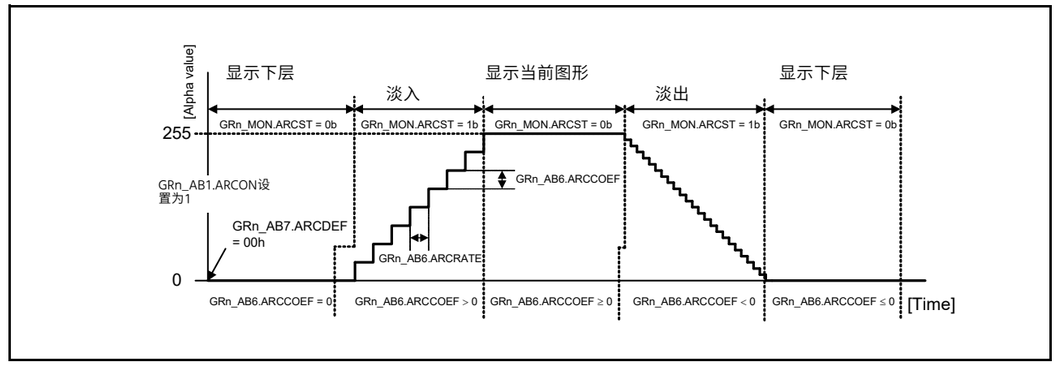


Figure 58.11 alpha值的变化

58.2.22 图形1Alpha混合控制寄存器7(GR1_AB7)图形2Alpha混合控制寄存器7(GR2_AB7)

Address(es): GLCDC.GR1_AB7 400E 1138h, GLCDC.GR2_AB7 400E 1238h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	ARCDEF[7:0]							
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CKON
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	CKON	RGB-Index Chroma-Key 加工控制	0：禁用色度键处理1：启用色度键处理。	R/W
b15 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b23 to b16	ARCDEF[7:0]	Alpha的初始Alpha值混合矩形 Area	矩形区域中Alpha混合的初始Alpha值。	R/W
b31 to b24	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note: 此设置反映到垂直同步信号（输入）断言的内部操作时 GRn_VEN.PVEN=1或当所有模块的内部操作的寄存器值反射控制信号被断言时。

CKON位（RGB索引色度键处理控制）

CKON位打开或关闭RGB索引色度键处理。仅当图形显示平面为混合显示(GRn_AB1.DISPSEL[1:0]=11b)时该位为1，才启用此功能。并且它反映到图形区域，除了矩形区域中的alpha混合。详见表58.8。

ARCDEF[7:0]位（矩形区域中Alpha混合的初始Alpha值）

ARCDEF[7:0]位指定矩形区域中alpha混合的初始alpha值。对于使用该位在当前图形的淡入或淡出过程中alpha值的变化，请参见图58.11。

58.2.23 Graphics 1 Alpha Blending Control Register 8 (GR1_AB8) Graphics 2 Alpha Blending Control Register 8 (GR2_AB8)

Address(es): GLCDC.GR1_AB8 400E 113Ch, GLCDC.GR2_AB8 400E 123Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	CKKG[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CKKB[7:0]								CKKR[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	CKKR[7:0]	R Signal for RGB-Index Chroma-Key Processing	R signal for RGB-index chroma-key processing. Unsigned 8-bit value.	R/W
b15 to b8	CKKB[7:0]	B Signal for RGB-Index Chroma-Key Processing	B signal for RGB-index chroma-key processing. Unsigned 8-bit value.	R/W
b23 to b16	CKKG[7:0]	G Signal for RGB-Index Chroma-Key Processing	G signal for RGB-index chroma-key processing. Unsigned 8-bit value.	R/W
b31 to b24	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: This setting is reflected to the internal operations on assertion of the vertical synchronization signal (input) when GRn_VEN.PVEN = 1 or when the register value reflection control signal to internal operations for all the modules is asserted.

If RGB-index chroma-key processing is enabled when the RGB values of the current bit graphics agree with the values of the associated chroma-key bits, the image data of the current graphics (ARGB8888, including the alpha blending values) is replaced by the values in the GRn_AB9 register. In alpha blending in pixel units at later stages, the latest alpha values are used.

CKKR[7:0] bits (R Signal for RGB-Index Chroma-Key Processing)

The CKKR[7:0] bits specify the value to be compared with the R value of the current graphics in the RGB-index chroma-key processing.

CKKB[7:0] bits (B Signal for RGB-Index Chroma-Key Processing)

The CKKB[7:0] bits specify the value to be compared with the B value of the current graphics in the RGB-index chroma-key processing.

CKKG[7:0] bits (G Signal for RGB-Index Chroma-Key Processing)

The CKKG[7:0] bits specify the value to be compared with the G value of the current graphics in the RGB-index chroma-key processing.

58.2.23 图形1Alpha混合控制寄存器8(GR1_AB8)图形2Alpha混合控制寄存器8(GR2_AB8)

Address(es): GLCDC.GR1_AB8 400E 113Ch, GLCDC.GR2_AB8 400E 123Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	CKKG[7:0]							
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CKKB[7:0]								CKKR[7:0]							
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b7 to b0	CKKR[7:0]	用于RGB索引色度键处理的R信号	用于RGB索引色度键处理的R信号。无符号8位值。	R/W
b15 to b8	CKKB[7:0]	用于RGB索引色度键处理的B信号	B信号用于RGB索引色度键处理。无符号8位值。	R/W
b23 to b16	CKKG[7:0]	用于RGB索引色度键处理的G信号	G信号用于RGB索引色度键处理。无符号8位值。	R/W
b31 to b24	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note: 此设置反映到垂直同步信号（输入）断言的内部操作时GRn_VEN.PVEN=1或当所有模块的内部操作的寄存器值反射控制信号被断言时。

如果在当前位图形的RGB值与相关色度键位的值一致时启用RGB-index色度键处理，则当前图形的图像数据（ARGB8888，包括alpha混合值）替换为GRn_AB9寄存器中的值。在后期以像素为单位的alpha混合中，使用最新的alpha值。

CKKR[7:0]位（用于RGB索引色度键处理的R信号）

CKKR[7:0]位指定在RGB索引色键处理中要与当前图形的R值进行比较的值。

CKKB[7:0]位（用于RGB索引色度键处理的B信号）

CKKB[7:0]位指定在RGB索引色键处理中要与当前图形的B值进行比较的值。

CKKG[7:0]位（用于RGB索引色度键处理的G信号）

CKKG[7:0]位指定在RGB-index色度键处理中要与当前图形的G值进行比较的值。

58.2.24 Graphics 1 Alpha Blending Control Register 9 (GR1_AB9) Graphics 2 Alpha Blending Control Register 9 (GR2_AB9)

Address(es): GLCDC.GR1_AB9 400E 1140h, GLCDC.GR2_AB9 400E 1240h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	CKA[7:0]								CKG[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CKB[7:0]								CKR[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	CKR[7:0]	R Value after RGB-Index Chroma-Key Processing Replacement	R value after RGB-index chroma-key processing replacement. Unsigned 8-bit value.	R/W
b15 to b8	CKB[7:0]	B Value after RGB-Index Chroma-Key Processing Replacement	B value after RGB-index chroma-key processing replacement. Unsigned 8-bit value.	R/W
b23 to b16	CKG[7:0]	G Value after RGB-Index Chroma-Key Processing Replacement	G value after RGB-index chroma-key processing replacement. Unsigned 8-bit value.	R/W
b31 to b24	CKA[7:0]	A Value after RGB-Index Chroma-Key Processing Replacement	A value after RGB-index chroma-key processing replacement.	R/W

Note: This setting is reflected to the internal operations on assertion of the vertical synchronization signal (input) when GRn_VEN.PVEN = 1 or when the register value reflection control signal to internal operations for all the modules is asserted.

If the RGB-index chroma-key processing is enabled and the pixel data is to be replaced (the RGB values of the current graphics agree with the GRn_AB8 values), alpha blending in pixel units is performed in later stages in accordance with this image data.

CKR[7:0] bits (R Value after RGB-Index Chroma-Key Processing Replacement)

The CKR[7:0] bits specify the R value after RGB-index chroma-key processing replacement.

CKB[7:0] bits (B Value after RGB-Index Chroma-Key Processing Replacement)

The CKB[7:0] bits specify the B value after RGB-index chroma-key processing replacement.

CKG[7:0] bits (G Value after RGB-Index Chroma-Key Processing Replacement)

The CKG[7:0] bits specify the G value after RGB-index chroma-key processing replacement.

CKA[7:0] bits (A Value after RGB-Index Chroma-Key Processing Replacement)

The CKA[7:0] bits specify the A value after RGB-index chroma-key processing replacement.

58.2.24 图形1Alpha混合控制寄存器9(GR1_AB9)图形2Alpha混合控制寄存器9(GR2_AB9)

Address(es): GLCDC.GR1_AB9 400E 1140h, GLCDC.GR2_AB9 400E 1240h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	CKA[7:0]								CKG[7:0]							
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CKB[7:0]								CKR[7:0]							
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b7 to b0	CKR[7:0]	RGB-IndexChroma-Key后的R值加工更换	RGB索引色度键处理替换后的R值。无符号8位值。	R/W
b15 to b8	CKB[7:0]	RGB-IndexChroma-Key后的B值加工更换	RGB索引色度键处理替换后的B值。无符号8位值。	R/W
b23 to b16	CKG[7:0]	RGB-IndexChroma-Key后的G值加工更换	RGB索引色度键处理替换后的G值。无符号8位值。	R/W
b31 to b24	CKA[7:0]	RGB-IndexChroma-Key之后的值加工更换	RGB索引色度键处理替换后的值。	R/W

Note: 此设置反映到垂直同步信号（输入）断言的内部操作时GRn_VEN.PVEN=1或当所有模块的内部操作的寄存器值反射控制信号被断言时。

如果启用RGB-indexchroma-key处理并且要替换像素数据（当前图形的RGB值与GRn_AB8值一致），则在后期根据该图像数据进行像素单元的alphablending.

CKR[7:0]位（RGB-IndexChroma-KeyProcessingReplacement后的R值）

CKR[7:0]位指定RGB索引色度键处理替换后的R值。

CKB[7:0]bits(RGB-IndexChroma-KeyProcessingReplacement后的B值)

CKB[7:0]位指定RGB索引色度键处理替换后的B值。

CKG[7:0]bits(RGB-IndexChroma-KeyProcessingReplacement后的G值)

CKG[7:0]位指定RGB索引色度键处理替换后的G值。

CKA[7:0]位（RGB-IndexChroma-KeyProcessingReplacement后的A值）

CKA[7:0]位指定RGB索引色度键处理替换后的A值。

58.2.25 Graphics 1 Background Color Control Register (GR1_BASE) Graphics 2 Background Color Control Register (GR2_BASE)

Address(es): GLCDC.GR1_BASE 400E 114Ch, GLCDC.GR2_BASE 400E 124Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	G[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	B[7:0]								R[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	R[7:0]	Background Color R Value	Background color R value. Unsigned 8-bit value.	R/W
b15 to b8	B[7:0]	Background Color B Value	Background color B value. Unsigned 8-bit value.	R/W
b23 to b16	G[7:0]	Background Color G Value	Background color G value. Unsigned 8-bit value.	R/W
b31 to b24	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: This setting is reflected to the internal operations on assertion of the vertical synchronization signal (input) when GRn_VEN.PVEN = 1 or when the register value reflection control signal to internal operations for all the modules is asserted.

When the background color is selected in the display selection (GRn_AB1.DISPSEL[1:0] = 00b), this RGB data is output to the entire display image area. When the current graphics setting is selected (GRn_AB1.DISPSEL[1:0] = 10b), the RGB data is output to the outside of the graphics image area within the display image area.

R[7:0] bits (Background Color R Value)

The R[7:0] bits specify the background color R value.

B[7:0] bits (Background Color B Value)

The B[7:0] bits specify the background color B value.

G[7:0] bits (Background Color G Value)

The G[7:0] bits specify the background color G value.

58.2.25 图形1背景颜色控制寄存器(GR1_BASE)图形2背景颜色控制寄存器(GR2_BASE)

Address(es): GLCDC.GR1_BASE 400E 114Ch, GLCDC.GR2_BASE 400E 124Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	G[7:0]							
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	B[7:0]								R[7:0]							
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b7 to b0	R[7:0]	背景颜色R值	背景颜色R值。无符号8位值。	R/W
b15 to b8	B[7:0]	背景颜色B值	背景颜色B值。无符号8位值。	R/W
b23 to b16	G[7:0]	背景颜色G值	背景颜色G值。无符号8位值。	R/W
b31 to b24	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note: 此设置反映到垂直同步信号（输入）断言的内部操作时
GRn_VEN.PVEN=1或当所有模块的内部操作的寄存器值反射控制信号被断言时。

当在显示选择中选择背景颜色时（GRn_AB1.DISPSEL[1:0]=00b），这个RGB数据被输出到整个显示图像区域。
Whenthecurrentgraphicssettingisselected(GRn_AB1.DISPSEL[1:0]=10b) theRGBdataisoutputtotheoutsideofthegraphicsimageareawithinthedisplayimagearea.

R[7:0]位（背景颜色R值）

R[7:0]位指定背景颜色R值。

B[7:0]位（背景颜色B值）

B[7:0]位指定背景颜色B值。

G[7:0]位（背景颜色G值）

G[7:0]位指定背景颜色G值。

58.2.26 Graphics 1 CLUT Table Interrupt Control Register (GR1_CLUTINT) Graphics 2 CLUT Table Interrupt Control Register (GR2_CLUTINT)

Address(es): GLCDC.GR1_CLUTINT 400E 1150h, GLCDC.GR2_CLUTINT 400E 1250h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SEL
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	LINE[10:0]										
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b10 to b0	LINE[10:0]	Number of Detection Lines	000h: 1 line : 3FFh: 1024 lines. Other settings are prohibited.	R/W
b15 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b16	SEL	CLUT Table Control	0: Select CLUT table 0 1: Select CLUT table 1.	R/W
b31 to b17	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: This setting is reflected to the internal operations on assertion of the vertical synchronization signal (input) when GRn_VEN.PVEN = 1 or when the register value reflection control signal to internal operations for all the modules is asserted.

LINE[10:0] bits (Number of Detection Lines)

The LINE[10:0] bits specify the number of lines to be detected. When the number of lines specified in this bit are detected, the event is recognized outside the module on the HS assertion. To retain the status of the recognized event and assert the GLCDC interrupt request signal, set the prescribed value to the State Detection Control Register (SYSCNT_DTCTEN) and Interrupt Request Enable Control Register (SYSCNT_INTEN), which are system control registers. Although this function is provided to both graphics 1 and 2, it is only enabled in graphics 2 in this GLCDC.

SEL bit (CLUT Table Control)

The SEL bit controls the CLUT plane to be used for internal operations. Access to the color palette (CLUT) through the register access bus is always valid for both planes 0 and 1, regardless of the setting in this bit, and the written value is immediately reflected to the internal operations (not in synchronization with the vertical synchronization signal).

To keep reflection of the CLUT memory contents to the internal operations in synchronization with the vertical synchronization signal, first write data through the register access bus to the plane that is not being used for the internal operations, and then modify the bits intended for controlling the plane that is to be used for the internal operations.

58.2.26 图形1CLUT表中断控制寄存器(GR1_CLUTINT)图形2CLUT表中断控制寄存器(GR2_CLUTINT)

Address(es): GLCDC.GR1_CLUTINT 400E 1150h, GLCDC.GR2_CLUTINT 400E 1250h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SEL
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	LINE[10:0]										
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b10 to b0	LINE[10:0]	检测线数	000h: 1 line :3FFh:1024行。禁止其他设置。	R/W
b15 to b11	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b16	SEL	CLUT表控件	0：选择CLUT表01：选择CLUT表1。	R/W
b31 to b17	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note: 此设置反映到垂直同步信号（输入）断言的内部操作时GRn_VEN.PVEN=1或当所有模块的内部操作的寄存器值反射控制信号被断言时。

LINE[10:0]位（检测线数）

LINE[10:0]位指定要检测的行数。当检测到该位中指定的行数时，在模块外部通过HS断言识别事件。要保留已识别事件的状态并断言GLCDC中断请求信号，请将规定值设置为系统控制寄存器状态检测控制寄存器(SYSCNT_DTCTEN)和中断请求使能控制寄存器(SYSCNT_INTEN)。虽然此功能同时提供给图形1和2，但它仅在此GLCDC中的图形2中启用。

SEL位（CLUT表控制）

SEL位控制要用于内部操作的CLUT平面。通过寄存器访问总线访问调色板（CLUT）对于平面0和平面1始终有效，无论该位的设置如何，写入的值立即反映到内部操作（与垂直同步不同步）信号）。

为了保持CLUT存储器内容与垂直同步信号同步地反映到内部操作，首先通过寄存器访问总线将数据写入未用于内部操作的平面，然后修改用于控制用于内部操作的平面。

58.2.27 Graphics 1 Status Monitor Register (GR1_MON) Graphics 2 Status Monitor Register (GR2_MON)

Address(es): GLCDC.GR1_MON 400E 1154h, GLCDC.GR2_MON 400E 1254h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	UNDFLST
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ARCST
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	ARCST	Status Monitor for Alpha Blending in Rectangular Area	0: Fade-in/fade-out not in progress 1: Fade-in/fade-out in progress.	R
b15 to b1	—	Reserved	These bits are read as 0.	R
b16	UNDFLST	Underflow Status Monitor	0: No underflow occurred in internal operations 1: Underflow occurred in internal operations.	R
b31 to b17	—	Reserved	These bits are read as 0.	R

ARCST bit (Status Monitor for Alpha Blending in Rectangular Area)

The ARCST bit indicates whether or not alpha blending (fade-in/fade-out) in a rectangular area is in progress. When alpha blending in a rectangular area is turned on (GRn_AB1.ARCON is set to 1) and the register value is to be reflected to the internal operations on assertion of the vertical synchronization signal (VS), this bit sets to 1 immediately on assertion of the vertical synchronization signal. When alpha blending in a rectangular area is turned off (GRn_AB1.ARCON cleared to 0) or when the alpha blending (fade-in/fade-out) in a rectangular area is complete (alpha blended value reaches the minimum or maximum value), this bit clears to 0. If the alpha coefficient for the alpha blending in a rectangular area (GRn_AB6.ARCCOEF[8:0]) is set to 000h and the initial alpha value for alpha blending in a rectangular area (GRn_AB7.ARCDEF[7:0]) is set to any value other than FFh or 00h, the alpha blending value does not reach the minimum or maximum value, and this bit remains 1 (no timeout processing is performed).

UNDFLST bit (Underflow Status Monitor)

The UNDFLST bit indicates whether or not an underflow has occurred in the internal operations. The underflow interrupt request flag sets when an underflow occurs, and retains its value until it is cleared by software. However, this bit monitors the internal status, and so the flag automatically clears to 0 when the graphics data bus interface initializes on assertion of the vertical synchronization signal. Even when the current graphics data is not required (GRn_AB1.DISPSEL[1:0] = 0xb), this bit sets to 1 during the period from the graphics image valid area start to the next frame vertical synchronization signal (VS) assertion timing set in the registers.

58.2.27 图形1状态监视器寄存器(GR1_MON)图形2状态监视器寄存器(GR2_MON)

Address(es): GLCDC.GR1_MON 400E 1154h, GLCDC.GR2_MON 400E 1254h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	UNDFLST
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ARCST
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	ARCST	Alpha状态监视器 在矩形区域中混合	0：淡入淡出未进行1：淡入淡出进行中。	R
b15 to b1	—	Reserved	这些位读为0。	R
b16	UNDFLST	下溢状态监视器	0：内部操作未发生下溢1：内部操作发生下溢。	R
b31 to b17	—	Reserved	这些位读为0。	R

ARCST位（矩形区域中Alpha混合的状态监视器）

ARCST位指示矩形区域中的alpha混合（淡入淡出）是否正在进行。当矩形区域中的alpha混合打开（GRn_AB1.ARCON设置为1）并且寄存器值要在垂直同步信号(VS)断言时反映到内部操作时，该位在断言时立即设置为1的垂直同步信号。当矩形区域的alpha混合关闭（GRn_AB1.ARCON清为0）或矩形区域的alpha混合（淡入淡出）完成（alpha混合值达到最小值或最大值）时，此位清除为0。如果矩形区域中alpha混合的alpha系数(GRn_AB6.ARCCOEF[8:0])设置为000h，并且矩形区域中alpha混合的初始alpha值(GRn_AB7.ARCDEF[7:0])设置为FFh或00h以外的任何值，alpha混合值未达到最小值或最大值，该位保持1（不执行超时处理）。

UNDFLST位（下溢状态监视器）

UNDFLST位指示内部操作中是否发生下溢。下溢中断请求标志在发生下溢时置位，并保持其值直到被软件清除。然而，该位监视内部状态，因此当图形数据总线接口在垂直同步信号的断言上初始化时，该标志自动清除为0。即使不需要当前图形数据(GRn_AB1.DISPSEL[1:0]=0xb)，在从图形图像有效区域开始到下一帧垂直同步信号(VS)断言时序设置期间，该位设置为1在寄存器中。

58.2.28 Gamma G Register Update Control Register (GAMG_LATCH) Gamma B Register Update Control Register (GAMB_LATCH) Gamma R Register Update Control Register (GAMR_LATCH)

Address(es): GLCDC.GAMG_LATCH 400E 1300h, GLCDC.GAMB_LATCH 400E 1340h, GLCDC.GAMR_LATCH 400E 1380h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VEN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	VEN	Control of Gamma Correction x Module Register Value Reflection to Internal Operations	0: Disable reflection of register values to internal operations on assertion of vertical synchronization signal (VS) 1: Enable reflection of register values to internal operations on assertion of the vertical synchronization signal (VS).	R/W
b31 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

VEN bit (Control of Gamma Correction x Module Register Value Reflection to Internal Operations)

The VEN bit enables or disables reflection of the register values to the internal operations in the gamma correction circuit on assertion of the vertical synchronization signal (input). When this bit is set to 1, the register values are immediately reflected to the internal operations on assertion of the vertical synchronization signal (input), and then this bit automatically clears to 0. Also, if the signal is asserted that controls reflection of the register values to the internal operations of all the modules output from the background plane generation module, the register values are reflected to the internal operations on assertion of the vertical synchronization signal (input), regardless of the value of this bit. While this bit is 1, do not modify any register whose value is reflected to the internal operations on assertion of the vertical synchronization signal (input) in the GLCDC. Otherwise, operation is not guaranteed.

This bit must not be 1 at the same time as the BG_EN.VEN bit (control of background plane register value reflection to internal operations) in the Operation Control Register (BG_EN), one of the background plane setting registers. Otherwise, operation is not guaranteed.

Although there are three VEN bits, one for each G, R, and B color, only the GAMG_LATCH.VEN bit controls the gamma correction with the reflection of the GAM_SW.GAMON bit. To enable gamma correction, set the GAMG_LATCH.VEN bit once after setting the GAM_SW.GAMON bit.

The VEN bit is set to 1 by writing 1, and automatically clears to 0 immediately on assertion of the vertical synchronization signal.

58.2.28 GammaG寄存器更新控制寄存器(GAMG_LATCH)GammaB寄存器更新控制寄存器(GAMB_LATCH)GammaR寄存器更新控制寄存器(GAMR_LATCH)

Address(es): GLCDC.GAMG_LATCH 400E 1300h, GLCDC.GAMB_LATCH 400E 1340h, GLCDC.GAMR_LATCH 400E 1380h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VEN
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	VEN	伽玛校正控制x 模块寄存器值反映到内部操作	0：禁止将寄存器值反映到内部 垂直同步信号(VS)断言操作1：启用寄存器值反映到垂直同步信号(VS)断言的内部操作。	R/W
b31 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

VEN位（Gamma校正x模块寄存器值反映到内部操作的控制）

VEN位启用或禁用寄存器值在垂直同步信号（输入）置位时反映到伽马校正电路的内部操作。当该位设置为1时，寄存器值立即反映到垂直同步信号（输入）置位时的内部操作，然后该位自动清除为0。此外，如果控制反射的信号被置位寄存器值反映到后台平面生成模块输出的所有模块的内部操作，无论该位的值如何，寄存器值都反映到垂直同步信号（输入）置位时的内部操作。当该位为1时，不要修改其值反映到GLCDC中垂直同步信号（输入）断言的内部操作的任何寄存器。否则，无法保证操作。

该位不能与后台平面设置寄存器之一的操作控制寄存器(BG_EN)中的BG_EN.VEN位（控制后台平面寄存器值反映到内部操作）同时为1。否则，无法保证操作。

虽然有三个VEN位，每个G、R和B颜色一个，但只有GAMG_LATCH.VEN位通过GAM_SW.GAMON位的反射来控制伽马校正。要启用伽马校正，请在设置GAM_SW.GAMON位后设置一次GAMG_LATCH.VEN位。

VEN位通过写入1设置为1，并在垂直同步信号有效时立即自动清除为0。

58.2.29 Gamma Correction Block Function Switch Register (GAM_SW)

Address(es): GLCDC.GAM_SW 400E 1304h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	GAMON
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	GAMON	Gamma Correction On/Off Control	0: Turn off gamma correction 1: Turn on gamma correction.	R/W
b31 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: This setting is reflected to the internal operations on assertion of the vertical synchronization signal (input) when GAMG_LATCH.VEN = 1 or when the register value reflection control signal to internal operations for all the modules is asserted.

GAMON bit (Gamma Correction On/Off Control)

The GAMON bit turns on or off gamma correction.

58.2.30 Gamma G Correction Block Table Setting Register 1 (GAMG_LUT1)
Gamma B Correction Block Table Setting Register 1 (GAMB_LUT1)
Gamma R Correction Block Table Setting Register 1 (GAMR_LUT1)

Address(es): GLCDC.GAMG_LUT1 400E 1308h, GLCDC.GAMB_LUT1 400E 1348h, GLCDC.GAMR_LUT1 400E 1388h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	GAIN00[10:0]										
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	GAIN01[10:0]										
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b10 to b0	GAIN01[10:0]	Gain Value of Area 1	Unsigned 11-bit fixed point value. 000h: 0.000 (0/1024) : 400h: 1.000 (1024/1024) : 7FFh: 1.999 (2047/1024).	R/W
b15 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b26 to b16	GAIN00[10:0]	Gain Value of Area 0	Unsigned 11-bit fixed point value. 000h: 0.000 (0/1024) : 400h: 1.000 (1024/1024) : 7FFh: 1.999 (2047/1024).	R/W

58.2.29 伽玛校正模块功能切换寄存器(GAM_SW)

Address(es): GLCDC.GAM_SW 400E 1304h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	GAMON
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	GAMON	伽马校正开关控制	0：关闭伽马校正1：打开伽 马校正。	R/W
b31 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note: 此设置反映到垂直同步信号（输入）断言的内部操作时
GAMG_LATCH.VEN=1或当所有模块的内部操作的寄存器值反射控制信号被断言时。

GAMON位（Gamma校正开关控制）

GAMON位打开或关闭伽马校正。

58.2.30 GammaG校正块表设置寄存器1(GAMG_LUT1)GammaB校正块表设置寄存器1(GAMB_LUT1)GammaR校正块表设置寄存器1(GAMR_LUT1)

Address(es): GLCDC.GAMG_LUT1 400E 1308h, GLCDC.GAMB_LUT1 400E 1348h, GLCDC.GAMR_LUT1 400E 1388h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	GAIN00[10:0]										
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	GAIN01[10:0]										
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b10 to b0	GAIN01[10:0]	区域1的增益值	无符号11位定点值。000h:0.000(01024) : 400h: 1.000 (1024/1024) : 7FFh: 1.999 (2047/1024).	R/W
b15 to b11	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b26 to b16	GAIN00[10:0]	0区增益值	无符号11位定点值。000h:0.000(01024) : 400h: 1.000 (1024/1024) : 7FFh: 1.999 (2047/1024).	R/W

Bit	Symbol	Bit name	Description	R/W
b31 to b27	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: This setting is reflected to the internal operations on assertion of the vertical synchronization signal (input) when GAMx_LATCH.VEN = 1 or when the register value reflection control signal to internal operations for all the modules is asserted.

Gamma correction for each color is carried out as follows:

- Din (input signal): 10 bits. To correct the output of graphics 2, 00b is appended as the lower 2 bits for extension
- Dout (output signal): 10 bits
- TH (threshold): 10 bits (register setting); up to 15 can be set
- GAIN (gain): 0/1024 to 2047/1024 for each area (register setting), can be set for up to 16 areas
- OFFSET (offset value): 21 bits (result of internal calculation; calculation of up to 15 points)

The following is automatically calculated from the assertion of the vertical synchronization signal (VS) to the start of valid pixel data internally:

- Dout = ((Din - TH(n)) × GAIN(n) + OFFSET(n))
- OFFSET(n) = OFFSET(n - 1) + (TH(n) - TH(n - 1)) × GAIN(n - 1), where OFFSET(0) = 0

Note: Because the gain is a positive number (≥ 0), the correction line shows a monotonic increase.

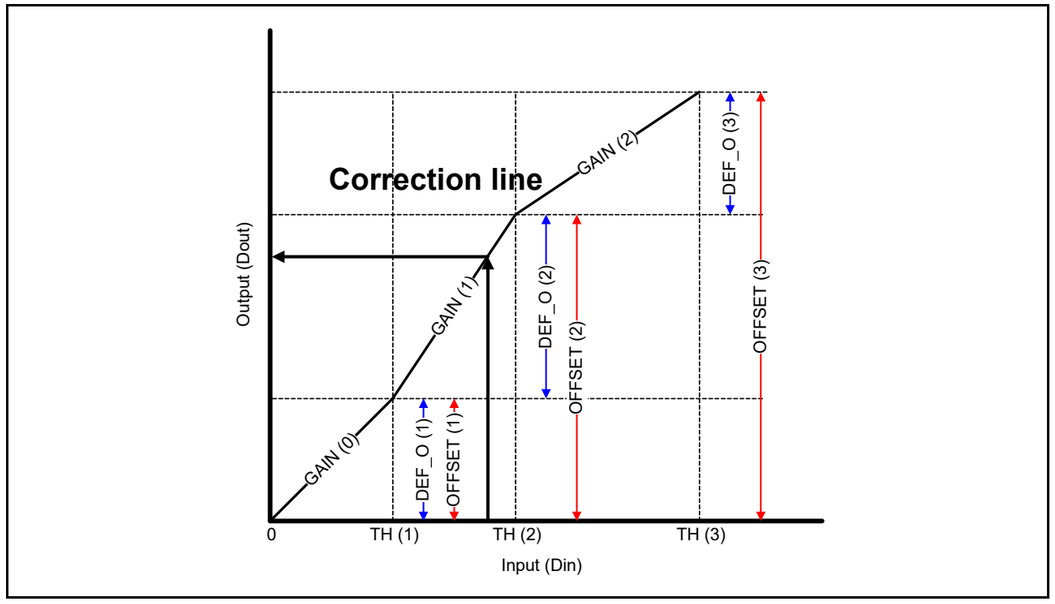


Figure 58.12 Calculation of gamma correction value

GAIN01[10:0] bits (Gain Value of Area 1)

The GAIN01[10:0] bits specify the gain value of area 1 to be used for gamma correction in terms of an unsigned 11-bit fixed point (0/1024 to 2047/1024). The location of the decimal point is between bits [10] and [11].

GAIN00[10:0] bits (Gain Value of Area 0)

The GAIN00[10:0] bits specify the gain value of area 0 to be used for gamma correction in terms of an unsigned 11-bit fixed point (0/1024 to 2047/1024). The location of the decimal point is between bits [10] and [11].

Bit	Symbol	位名称	Description	R/W
b31 to b27	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note: 此设置反映到垂直同步信号（输入）断言的内部操作时
GAMx_LATCH.VEN=1或当所有模块的内部操作的寄存器值反射控制信号被断言时。

每种颜色的Gamma校正如下进行：

- Din（输入信号）：10位。为了更正图形2的输出，00b被附加为低2位用于扩展
- Dout (output signal): 10 bits
- TH（阈值）：10位（寄存器设置）；最多可设置15个
- GAIN（增益）：01024到20471024每个区域（寄存器设置），最多可设置16个区域
- OFFSET（偏移值）：21位（内部计算结果；最多计算15个点）

以下是从垂直同步信号(VS)的断言到内部有效像素数据开始的自动计算：

- Dout = ((Din - TH(n)) × GAIN(n) + OFFSET(n))
- OFFSET(n) = OFFSET(n - 1) + (TH(n) - TH(n - 1)) × GAIN(n - 1), where OFFSET(0) = 0

Note: 因为增益是正数（ 0），所以校正线显示出单调增加。

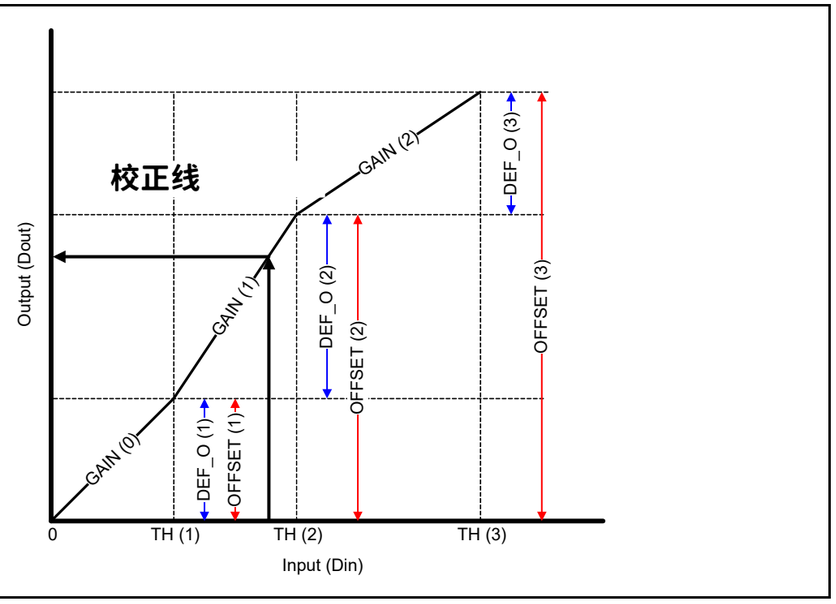


Figure 58.12 伽马校正值的计算

GAIN01[10:0]位（区域1的增益值）

GAIN01[10:0]位指定区域1的增益值，用于以无符号11位定点（01024到20471024）的形式进行伽马校正。小数点的位置在位[10]和[11]之间。

GAIN00[10:0]位（区域0的增益值）

GAIN00[10:0]位指定区域0的增益值，用于以无符号11位定点（01024到20471024）的形式进行伽马校正。小数点的位置在位[10]和[11]之间。

58.2.31 Gamma G Correction Block Table Setting Register 2 (GAMG_LUT2) Gamma B Correction Block Table Setting Register 2 (GAMB_LUT2) Gamma R Correction Block Table Setting Register 2 (GAMR_LUT2)

Address(es): GLCDC.GAMG_LUT2 400E 130Ch, GLCDC.GAMB_LUT2 400E 134Ch, GLCDC.GAMR_LUT2 400E 138Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	GAIN02[10:0]										
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	GAIN03[10:0]										
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b10 to b0	GAIN03[10:0]	Gain Value of Area 3	Unsigned 11-bit fixed point value. 000h: 0.000 (0/1024) : 400h: 1.000 (1024/1024) : 7FFh: 1.999 (2047/1024).	R/W
b15 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b26 to b16	GAIN02[10:0]	Gain Value of Area 2	Unsigned 11-bit fixed point value. 000h: 0.000 (0/1024) : 400h: 1.000 (1024/1024) : 7FFh: 1.999 (2047/1024).	R/W
b31 to b27	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: This setting is reflected to the internal operations on assertion of the vertical synchronization signal (input) when GAMx_LATCH.VEN = 1 or when the register value reflection control signal to internal operations for all the modules is asserted.

GAIN03[10:0] bits (Gain Value of Area 3)

The GAIN03[10:0] bits specify the gain value of area 3 to be used for gamma correction in terms of an unsigned 11-bit fixed point (0/1024 to 2047/1024). The location of the decimal point is between bits [10] and [11].

GAIN02[10:0] bits (Gain Value of Area 2)

The GAIN02[10:0] bits specify the gain value of area 2 to be used for gamma correction in terms of an unsigned 11-bit fixed point (0/1024 to 2047/1024). The location of the decimal point is between bits [10] and [11].

58.2.31 GammaG校正块表设置寄存器2(GAMG_LUT2)GammaB校正块表设置寄存器2(GAMB_LUT2)GammaR校正块表设置寄存器2(GAMR_LUT2)

Address(es): GLCDC.GAMG_LUT2 400E 130Ch, GLCDC.GAMB_LUT2 400E 134Ch, GLCDC.GAMR_LUT2 400E 138Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	GAIN02[10:0]										
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	GAIN03[10:0]										
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b10 to b0	GAIN03[10:0]	区域3的增益值	无符号11位定点值。000h:0.000(01024) : 400h: 1.000 (1024/1024) : 7FFh: 1.999 (2047/1024).	R/W
b15 to b11	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b26 to b16	GAIN02[10:0]	区域2的增益值	无符号11位定点值。000h:0.000(01024) : 400h: 1.000 (1024/1024) : 7FFh: 1.999 (2047/1024).	R/W
b31 to b27	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note: 此设置反映到垂直同步信号（输入）断言的内部操作时
GAMx_LATCH.VEN=1或当所有模块的内部操作的寄存器值反射控制信号被断言时。

GAIN03[10:0]位（区域3的增益值）

GAIN03[10:0]位指定区域3的增益值，用于以无符号11位定点（01024到20471024）的形式进行伽马校正。小数点的位置在位[10]和[11]之间。

GAIN02[10:0]位（区域2的增益值）

GAIN02[10:0]位指定区域2的增益值，用于以无符号11位定点（01024到20471024）的形式进行伽马校正。小数点的位置在位[10]和[11]之间。

58.2.32 Gamma G Correction Block Table Setting Register 3 (GAMG_LUT3)
Gamma B Correction Block Table Setting Register 3 (GAMB_LUT3)
Gamma R Correction Block Table Setting Register 3 (GAMR_LUT3)

Address(es): GLCDC.GAMG_LUT3 400E 1310h, GLCDC.GAMB_LUT3 400E 1350h, GLCDC.GAMR_LUT3 400E 1390h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	GAIN04[10:0]										
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	GAIN05[10:0]										
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b10 to b0	GAIN05[10:0]	Gain Value of Area 5	Unsigned 11-bit fixed point value. 000h: 0.000 (0/1024) : 400h: 1.000 (1024/1024) : 7FFh: 1.999 (2047/1024).	R/W
b15 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b26 to b16	GAIN04[10:0]	Gain Value of Area 4	Unsigned 11-bit fixed point value. 000h: 0.000 (0/1024) : 400h: 1.000 (1024/1024) : 7FFh: 1.999 (2047/1024).	R/W
b31 to b27	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: This setting is reflected to the internal operations on assertion of the vertical synchronization signal (input) when GAMx_LATCH.VEN = 1 or when the register value reflection control signal to internal operations for all the modules is asserted.

GAIN05[10:0] bits (Gain Value of Area 5)

The GAIN05[10:0] bits specify the gain value of area 5 to be used for gamma correction in terms of an unsigned 11-bit fixed point (0/1024 to 2047/1024). The location of the decimal point is between bits [10] and [11].

GAIN04[10:0] bits (Gain Value of Area 4)

The GAIN04[10:0] bits specify the gain value of area 4 to be used for gamma correction in terms of an unsigned 11-bit fixed point (0/1024 to 2047/1024). The location of the decimal point is between bits [10] and [11].

58.2.32 GammaG校正块表设置寄存器3(GAMG_LUT3)GammaB校正块表设置寄存器3(GAMB_LUT3)GammaR校正块表设置寄存器3(GAMR_LUT3)

Address(es): GLCDC.GAMG_LUT3 400E 1310h, GLCDC.GAMB_LUT3 400E 1350h, GLCDC.GAMR_LUT3 400E 1390h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	GAIN04[10:0]										
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	GAIN05[10:0]										
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b10 to b0	GAIN05[10:0]	5区增益值	无符号11位定点值。000h:0.000(01024) : 400h: 1.000 (1024/1024) : 7FFh: 1.999 (2047/1024).	R/W
b15 to b11	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b26 to b16	GAIN04[10:0]	区域4的增益值	无符号11位定点值。000h:0.000(01024) : 400h: 1.000 (1024/1024) : 7FFh: 1.999 (2047/1024).	R/W
b31 to b27	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note: 此设置反映到垂直同步信号（输入）断言的内部操作时
GAMx_LATCH.VEN=1或当所有模块的内部操作的寄存器值反射控制信号被断言时。

GAIN05[10:0]位（区域5的增益值）

GAIN05[10:0]位指定区域5的增益值，用于以无符号11位定点（01024到20471024）的形式进行伽马校正。小数点的位置在位[10]和[11]之间。

GAIN04[10:0]位（区域4的增益值）

GAIN04[10:0]位指定区域4的增益值，用于以无符号11位定点（01024到20471024）的形式进行伽马校正。小数点的位置在位[10]和[11]之间。

58.2.33 Gamma G Correction Block Table Setting Register 4 (GAMG_LUT4) Gamma B Correction Block Table Setting Register 4 (GAMB_LUT4) Gamma R Correction Block Table Setting Register 4 (GAMR_LUT4)

Address(es): GLCDC.GAMG_LUT4 400E 1314h, GLCDC.GAMB_LUT4 400E 1354h, GLCDC.GAMR_LUT4 400E 1394h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	GAIN06[10:0]										
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	GAIN07[10:0]										
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b10 to b0	GAIN07[10:0]	Gain Value of Area 7	Unsigned 11-bit fixed point value. 000h: 0.000 (0/1024) : 400h: 1.000 (1024/1024) : 7FFh: 1.999 (2047/1024).	R/W
b15 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b26 to b16	GAIN06[10:0]	Gain Value of Area 6	Unsigned 11-bit fixed point value. 000h: 0.000 (0/1024) : 400h: 1.000 (1024/1024) : 7FFh: 1.999 (2047/1024).	R/W
b31 to b27	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: This setting is reflected to the internal operations on assertion of the vertical synchronization signal (input) when GAMx_LATCH.VEN = 1 or when the register value reflection control signal to internal operations for all the modules is asserted.

GAIN07[10:0] bits (Gain Value of Area 7)

The GAIN07[10:0] bits specify the gain value of area 7 to be used for gamma correction in terms of an unsigned 11-bit fixed point (0/1024 to 2047/1024). The location of the decimal point is between bits [10] and [11].

GAIN06[10:0] bits (Gain Value of Area 6)

The GAIN06[10:0] bits specify the gain value of area 6 to be used for gamma correction in terms of an unsigned 11-bit fixed point (0/1024 to 2047/1024). The location of the decimal point is between bits [10] and [11].

58.2.33 GammaG校正块表设置寄存器4(GAMG_LUT4)GammaB校正块表设置寄存器4(GAMB_LUT4)GammaR校正块表设置寄存器4(GAMR_LUT4)

Address(es): GLCDC.GAMG_LUT4 400E 1314h, GLCDC.GAMB_LUT4 400E 1354h, GLCDC.GAMR_LUT4 400E 1394h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	GAIN06[10:0]										
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	GAIN07[10:0]										
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b10 to b0	GAIN07[10:0]	7区的增益值	无符号11位定点值。000h:0.000(01024) : 400h: 1.000 (1024/1024) : 7FFh: 1.999 (2047/1024).	R/W
b15 to b11	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b26 to b16	GAIN06[10:0]	区域6的增益值	无符号11位定点值。000h:0.000(01024) : 400h: 1.000 (1024/1024) : 7FFh: 1.999 (2047/1024).	R/W
b31 to b27	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note: 此设置反映到垂直同步信号（输入）断言的内部操作时
GAMx_LATCH.VEN=1或当所有模块的内部操作的寄存器值反射控制信号被断言时。

GAIN07[10:0]位（区域7的增益值）

GAIN07[10:0]位指定区域7的增益值，用于以无符号11位定点（01024到20471024）的形式进行伽马校正。小数点的位置在位[10]和[11]之间。

GAIN06[10:0]位（区域6的增益值）

GAIN06[10:0]位指定区域6的增益值，用于以无符号11位定点（01024到20471024）的形式进行伽马校正。小数点的位置在位[10]和[11]之间。

58.2.34 Gamma G Correction Block Table Setting Register 5 (GAMG_LUT5)
Gamma B Correction Block Table Setting Register 5 (GAMB_LUT5)
Gamma R Correction Block Table Setting Register 5 (GAMR_LUT5)

Address(es): GLCDC.GAMG_LUT5 400E 1318h, GLCDC.GAMB_LUT5 400E 1358h, GLCDC.GAMR_LUT5 400E 1398h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	GAIN08[10:0]										
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	GAIN09[10:0]										
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b10 to b0	GAIN09[10:0]	Gain Value of Area 9	Unsigned 11-bit fixed point value. 000h: 0.000 (0/1024) : 400h: 1.000 (1024/1024) : 7FFh: 1.999 (2047/1024).	R/W
b15 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b26 to b16	GAIN08[10:0]	Gain Value of Area 8	Unsigned 11-bit fixed point value. 000h: 0.000 (0/1024) : 400h: 1.000 (1024/1024) : 7FFh: 1.999 (2047/1024).	R/W
b31 to b27	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: This setting is reflected to the internal operations on assertion of the vertical synchronization signal (input) when GAMx_LATCH.VEN = 1 or when the register value reflection control signal to internal operations for all the modules is asserted.

GAIN09[10:0] bits (Gain Value of Area 9)

The GAIN09[10:0] bits specify the gain value of area 9 to be used for gamma correction in terms of an unsigned 11-bit fixed point (0/1024 to 2047/1024). The location of the decimal point is between bits [10] and [11].

GAIN08[10:0] bits (Gain Value of Area 8)

The GAIN08[10:0] bits specify the gain value of area 8 to be used for gamma correction in terms of an unsigned 11-bit fixed point (0/1024 to 2047/1024). The location of the decimal point is between bits [10] and [11].

58.2.34 GammaG校正块表设置寄存器5(GAMG_LUT5)GammaB校正块表设置寄存器5(GAMB_LUT5)GammaR校正块表设置寄存器5(GAMR_LUT5)

Address(es): GLCDC.GAMG_LUT5 400E 1318h, GLCDC.GAMB_LUT5 400E 1358h, GLCDC.GAMR_LUT5 400E 1398h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	GAIN08[10:0]										
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	GAIN09[10:0]										
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b10 to b0	GAIN09[10:0]	区域9的增益值	无符号11位定点值。000h:0.000(01024) : 400h: 1.000 (1024/1024) : 7FFh: 1.999 (2047/1024).	R/W
b15 to b11	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b26 to b16	GAIN08[10:0]	8区增益值	无符号11位定点值。000h:0.000(01024) : 400h: 1.000 (1024/1024) : 7FFh: 1.999 (2047/1024).	R/W
b31 to b27	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note: 此设置反映到垂直同步信号（输入）断言的内部操作时
GAMx_LATCH.VEN=1或当所有模块的内部操作的寄存器值反射控制信号被断言时。

GAIN09[10:0]位（区域9的增益值）

GAIN09[10:0]位指定区域9的增益值，用于以无符号11位定点（01024到20471024）的形式进行伽马校正。小数点的位置在位[10]和[11]之间。

GAIN08[10:0]位（区域8的增益值）

GAIN08[10:0]位指定区域8的增益值，用于以无符号11位定点（01024到20471024）的形式进行伽马校正。小数点的位置在位[10]和[11]之间。

58.2.35 Gamma G Correction Block Table Setting Register 6 (GAMG_LUT6)
Gamma B Correction Block Table Setting Register 6 (GAMB_LUT6)
Gamma R Correction Block Table Setting Register 6 (GAMR_LUT6)

Address(es): GLCDC.GAMG_LUT6 400E 131Ch, GLCDC.GAMB_LUT6 400E 135Ch, GLCDC.GAMR_LUT6 400E 139Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	GAIN10[10:0]										
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	GAIN11[10:0]										
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b10 to b0	GAIN11[10:0]	Gain Value of Area 11	Unsigned 11-bit fixed point value. 000h: 0.000 (0/1024) : 400h: 1.000 (1024/1024) : 7FFh: 1.999 (2047/1024).	R/W
b15 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b26 to b16	GAIN10[10:0]	Gain Value of Area 10	Unsigned 11-bit fixed point value. 000h: 0.000 (0/1024) : 400h: 1.000 (1024/1024) : 7FFh: 1.999 (2047/1024).	R/W
b31 to b27	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: This setting is reflected to the internal operations on assertion of the vertical synchronization signal (input) when GAMx_LATCH.VEN = 1 or when the register value reflection control signal to internal operations for all the modules is asserted.

GAIN11[10:0] bits (Gain Value of Area 11)

The GAIN11[10:0] bits specify the gain value of area 11 to be used for gamma correction in terms of an unsigned 11-bit fixed point (0/1024 to 2047/1024). The location of the decimal point is between bits [10] and [11].

GAIN10[10:0] bits (Gain Value of Area 10)

The GAIN10[10:0] bits specify the gain value of area 10 to be used for gamma correction in terms of an unsigned 11-bit fixed point (0/1024 to 2047/1024). The location of the decimal point is between bits [10] and [11].

58.2.35 GammaG校正块表设置寄存器6(GAMG_LUT6)GammaB校正块表设置寄存器6(GAMB_LUT6)GammaR校正块表设置寄存器6(GAMR_LUT6)

Address(es): GLCDC.GAMG_LUT6 400E 131Ch, GLCDC.GAMB_LUT6 400E 135Ch, GLCDC.GAMR_LUT6 400E 139Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	GAIN10[10:0]										
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	GAIN11[10:0]										
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b10 to b0	GAIN11[10:0]	11区的增益值	无符号11位定点值。000h:0.000(01024) : 400h: 1.000 (1024/1024) : 7FFh: 1.999 (2047/1024).	R/W
b15 to b11	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b26 to b16	GAIN10[10:0]	10区的增益值	无符号11位定点值。000h:0.000(01024) : 400h: 1.000 (1024/1024) : 7FFh: 1.999 (2047/1024).	R/W
b31 to b27	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note: 此设置反映到垂直同步信号（输入）断言的内部操作时
GAMx_LATCH.VEN=1或当所有模块的内部操作的寄存器值反射控制信号被断言时。

GAIN11[10:0]位（区域11的增益值）

GAIN11[10:0]位指定区域11的增益值，用于以无符号11位定点（01024到20471024）的形式进行伽马校正。小数点的位置在位[10]和[11]之间。

GAIN10[10:0]位（区域10的增益值）

GAIN10[10:0]位指定区域10的增益值，用于以无符号11位定点（01024到20471024）的形式进行伽马校正。小数点的位置在位[10]和[11]之间。

58.2.36 Gamma G Correction Block Table Setting Register 7 (GAMG_LUT7) Gamma B Correction Block Table Setting Register 7 (GAMB_LUT7) Gamma R Correction Block Table Setting Register 7 (GAMR_LUT7)

Address(es): GLCDC.GAMG_LUT7 400E 1320h, GLCDC.GAMB_LUT7 400E 1360h, GLCDC.GAMR_LUT7 400E 13A0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	GAIN12[10:0]										
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	GAIN13[10:0]										
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b10 to b0	GAIN13[10:0]	Gain Value of Area 13	Unsigned 11-bit fixed point value. 000h: 0.000 (0/1024) : 400h: 1.000 (1024/1024) : 7FFh: 1.999 (2047/1024).	R/W
b15 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b26 to b16	GAIN12[10:0]	Gain Value of Area 12	Unsigned 11-bit fixed point value. 000h: 0.000 (0/1024) : 400h: 1.000 (1024/1024) : 7FFh: 1.999 (2047/1024).	R/W
b31 to b27	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: This setting is reflected to the internal operations on assertion of the vertical synchronization signal (input) when GAMx_LATCH.VEN = 1 or when the register value reflection control signal to internal operations for all the modules is asserted.

GAIN13[10:0] bits (Gain Value of Area 13)

The GAIN13[10:0] bits specify the gain value of area 13 to be used for gamma correction in terms of an unsigned 11-bit fixed point (0/1024 to 2047/1024). The location of the decimal point is between bits [10] and [11].

GAIN12[10:0] bits (Gain Value of Area 12)

The GAIN12[10:0] bits specify the gain value of area 12 to be used for gamma correction in terms of an unsigned 11-bit fixed point (0/1024 to 2047/1024). The location of the decimal point is between bits [10] and [11].

58.2.36 GammaG校正块表设置寄存器7(GAMG_LUT7)GammaB校正块表设置寄存器7(GAMB_LUT7)GammaR校正块表设置寄存器7(GAMR_LUT7)

Address(es): GLCDC.GAMG_LUT7 400E 1320h, GLCDC.GAMB_LUT7 400E 1360h, GLCDC.GAMR_LUT7 400E 13A0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	GAIN12[10:0]										
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	GAIN13[10:0]										
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b10 to b0	GAIN13[10:0]	13区的增益值	无符号11位定点值。000h:0.000(01024) : 400h: 1.000 (1024/1024) : 7FFh: 1.999 (2047/1024).	R/W
b15 to b11	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b26 to b16	GAIN12[10:0]	12区的增益值	无符号11位定点值。000h:0.000(01024) : 400h: 1.000 (1024/1024) : 7FFh: 1.999 (2047/1024).	R/W
b31 to b27	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note: 此设置反映到垂直同步信号（输入）断言的内部操作时
GAMx_LATCH.VEN=1或当所有模块的内部操作的寄存器值反射控制信号被断言时。

GAIN13[10:0]位（区域13的增益值）

GAIN13[10:0]位指定区域13的增益值，用于以无符号11位定点（01024到20471024）的形式进行伽马校正。小数点的位置在位[10]和[11]之间。

GAIN12[10:0]位（区域12的增益值）

GAIN12[10:0]位指定区域12的增益值，用于以无符号11位定点（01024到20471024）的形式进行伽马校正。小数点的位置在位[10]和[11]之间。

58.2.37 Gamma G Correction Block Table Setting Register 8 (GAMG_LUT8) Gamma B Correction Block Table Setting Register 8 (GAMB_LUT8) Gamma R Correction Block Table Setting Register 8 (GAMR_LUT8)

Address(es): GLCDC.GAMG_LUT8 400E 1324h, GLCDC.GAMB_LUT8 400E 1364h, GLCDC.GAMR_LUT8 400E 13A4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	GAIN14[10:0]										
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	GAIN15[10:0]										
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b10 to b0	GAIN15[10:0]	Gain Value of Area 15	Unsigned 11-bit fixed point value. 000h: 0.000 (0/1024) : 400h: 1.000 (1024/1024) : 7FFh: 1.999 (2047/1024).	R/W
b15 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b26 to b16	GAIN14[10:0]	Gain Value of Area 14	Unsigned 11-bit fixed point value. 000h: 0.000 (0/1024) : 400h: 1.000 (1024/1024) : 7FFh: 1.999 (2047/1024).	R/W
b31 to b27	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: This setting is reflected to the internal operations on assertion of the vertical synchronization signal (input) when GAMx_LATCH.VEN = 1 or when the register value reflection control signal to internal operations for all the modules is asserted.

GAIN15[10:0] bits (Gain Value of Area 15)

The GAIN15[10:0] bits specify the gain value of area 15 to be used for gamma correction in terms of an unsigned 11-bit fixed point (0/1024 to 2047/1024). The location of the decimal point is between bits [10] and [11].

GAIN14[10:0] bits (Gain Value of Area 14)

The GAIN14[10:0] bits specify the gain value of area 14 to be used for gamma correction in terms of an unsigned 11-bit fixed point (0/1024 to 2047/1024). The location of the decimal point is between bits [10] and [11].

58.2.37 GammaG校正块表设置寄存器8(GAMG_LUT8)GammaB校正块表设置寄存器8(GAMB_LUT8)GammaR校正块表设置寄存器8(GAMR_LUT8)

Address(es): GLCDC.GAMG_LUT8 400E 1324h, GLCDC.GAMB_LUT8 400E 1364h, GLCDC.GAMR_LUT8 400E 13A4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	GAIN14[10:0]										
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	GAIN15[10:0]										
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b10 to b0	GAIN15[10:0]	15区的增益值	无符号11位定点值。000h:0.000(01024) : 400h: 1.000 (1024/1024) : 7FFh: 1.999 (2047/1024).	R/W
b15 to b11	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b26 to b16	GAIN14[10:0]	14区的增益值	无符号11位定点值。000h:0.000(01024) : 400h: 1.000 (1024/1024) : 7FFh: 1.999 (2047/1024).	R/W
b31 to b27	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note: 此设置反映到垂直同步信号（输入）断言的内部操作时
GAMx_LATCH.VEN=1或当所有模块的内部操作的寄存器值反射控制信号被断言时。

GAIN15[10:0]位（区域15的增益值）

GAIN15[10:0]位指定区域15的增益值，用于以无符号11位定点（01024到20471024）的形式进行伽马校正。小数点的位置在位[10]和[11]之间。

GAIN14[10:0]位（区域14的增益值）

GAIN14[10:0]位指定区域14的增益值，用于以无符号11位定点（01024到20471024）的形式进行伽马校正。小数点的位置在位[10]和[11]之间。

58.2.38 Gamma G Correction Block Area Setting Register 1 (GAMG_AREA1) Gamma B Correction Block Area Setting Register 1 (GAMB_AREA1) Gamma R Correction Block Area Setting Register 1 (GAMR_AREA1)

Address(es): GLCDC.GAMG_AREA1 400E 1328h, GLCDC.GAMB_AREA1 400E 1368h, GLCDC.GAMR_AREA1 400E 13A8h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	TH01[9:0]										TH02[9:6]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TH02[5:0]						TH03[9:0]									
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b9 to b0	TH03[9:0]	Start Threshold of Area 3	Start threshold of area 3. Unsigned 10-bit integer.	R/W
b19 to b10	TH02[9:0]	Start Threshold of Area 2	Start threshold of area 2. Unsigned 10-bit integer.	R/W
b29 to b20	TH01[9:0]	Start Threshold of Area 1	Start threshold of area 1. Unsigned 10-bit integer.	R/W
b31 to b30	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: This setting is reflected to the internal operations on assertion of the vertical synchronization signal (input) when GAMx_LATCH.VEN = 1 or when the register value reflection control signal to internal operations for all the modules is asserted.

Set the start threshold TH(n) of area n (n = 0 to 15) to satisfy the following conditions. Otherwise, operation is not guaranteed.

TH (n) < TH (n + 1)
n = 0 to 15 and TH (0) = 000h, TH (16) = 3FFh
TH (n) = TH (n + 1) is valid only if TH (n) = 3FFh.

For details on calculation of the gamma correction value, see section 58.2.30, Gamma G Correction Block Table Setting Register 1 (GAMG_LUT1) Gamma B Correction Block Table Setting Register 1 (GAMB_LUT1) Gamma R Correction Block Table Setting Register 1 (GAMR_LUT1), and Figure 58.12.

TH03[9:0] bits (Start Threshold of Area 3)

The TH03[9:0] bits specify the start threshold of area 3 to be used for gamma correction in terms of an unsigned 10-bit integer.

TH02[9:0] bits (Start Threshold of Area 2)

The TH02[9:0] bits specify the start threshold of area 2 to be used for gamma correction in terms of an unsigned 10-bit integer.

TH01[9:0] bits (Start Threshold of Area 1)

The TH01[9:0] bits specify the start threshold of area 1 to be used for gamma correction in terms of an unsigned 10-bit integer.

58.2.38 GammaG校正块区域设置寄存器1(GAMG_AREA1)GammaB校正块区域设置寄存器1(GAMB_AREA1)GammaR校正块区域设置寄存器1(GAMR_AREA1)

Address(es): GLCDC.GAMG_AREA1 400E 1328h, GLCDC.GAMB_AREA1 400E 1368h, GLCDC.GAMR_AREA1 400E 13A8h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	TH01[9:0]										TH02[9:6]			
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TH02[5:0]						TH03[9:0]									
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b9 to b0	TH03[9:0]	区域3的起始阈值	区域3的起始阈值。无符号10位整数。	R/W
b19 to b10	TH02[9:0]	区域2的起始阈值	区域2的起始阈值。无符号10位整数。	R/W
b29 to b20	TH01[9:0]	区域1的起始阈值	区域1的起始阈值。无符号10位整数。	R/W
b31 to b30	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note: 此设置反映到垂直同步信号（输入）断言的内部操作时
GAMx_LATCH.VEN=1或当所有模块的内部操作的寄存器值反射控制信号被断言时。

设置区域n(n=0到15)的起始阈值TH(n)以满足以下条件。否则，无法保证操作。

TH(n)<TH(n+1)n=0到15并且TH(0)=000h TH(16)
=3FFhTH(n)=TH(n+1)只有当TH(n)=时才有效3FF
h。

有关伽马校正值计算的详细信息，请参阅第58.2.30节，伽马G校正块表设置寄存器1(GAMG_LUT1)伽玛B校正块表设置寄存器1(GAMB_LUT1)伽玛R校正
块表设置寄存器1(GAMR_LUT1)和图58.12。

TH03[9:0]位（区域3的起始阈值）

TH03[9:0]位指定区域3的起始阈值，用于以无符号10位整数形式进行伽马校正。

TH02[9:0]位（区域2的起始阈值）

TH02[9:0]位以无符号10位整数的形式指定要用于伽马校正的区域2的起始阈值。

TH01[9:0]位（区域1的起始阈值）

TH01[9:0]位以无符号10位整数的形式指定用于伽马校正的区域1的起始阈值。

58.2.39 Gamma G Correction Block Area Setting Register 2 (GAMG_AREA2) Gamma B Correction Block Area Setting Register 2 (GAMB_AREA2) Gamma R Correction Block Area Setting Register 2 (GAMR_AREA2)

Address(es): GLCDC.GAMG_AREA2 400E 132Ch, GLCDC.GAMB_AREA2 400E 136Ch, GLCDC.GAMR_AREA2 400E 13ACh

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	TH04[9:0]										TH05[9:6]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TH05[5:0]						TH06[9:0]									
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b9 to b0	TH06[9:0]	Start Threshold of Area 6	Start threshold of area 6. Unsigned 10-bit integer.	R/W
b19 to b10	TH05[9:6], TH08[5:0]	Start Threshold of Area 5	Start threshold of area 5. Unsigned 10-bit integer.	R/W
b29 to b20	TH04[9:0]	Start Threshold of Area 4	Start threshold of area 4. Unsigned 10-bit integer.	R/W
b31 to b30	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: This setting is reflected to the internal operations on assertion of the vertical synchronization signal (input) when GAMx_LATCH.VEN = 1 or when the register value reflection control signal to internal operations for all the modules is asserted.

TH06[9:0] bits (Start Threshold of Area 6)

The TH06[9:0] bits specify the start threshold of area 6 to be used for gamma correction in terms of an unsigned 10-bit integer.

TH05[9:0] bits (Start Threshold of Area 5)

The TH05[9:0] bits specify the start threshold of area 5 to be used for gamma correction in terms of an unsigned 10-bit integer.

TH04[9:0] bits (Start Threshold of Area 4)

The TH04[9:0] bits specify the start threshold of area 4 to be used for gamma correction in terms of an unsigned 10-bit integer.

58.2.39 GammaG校正块区域设置寄存器2(GAMG_AREA2)GammaB校正块区域设置寄存器2(GAMB_AREA2)GammaR校正块区域设置寄存器2(GAMR_AREA2)

Address(es): GLCDC.GAMG_AREA2 400E 132Ch, GLCDC.GAMB_AREA2 400E 136Ch, GLCDC.GAMR_AREA2 400E 13ACh

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	TH04[9:0]										TH05[9:6]			
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TH05[5:0]						TH06[9:0]									
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b9 to b0	TH06[9:0]	区域6的起始阈值	区域6的起始阈值。无符号10位整数。	R/W
b19 to b10	TH05[9:6], TH08[5:0]	区域5的起始阈值	区域5的起始阈值。无符号10位整数。	R/W
b29 to b20	TH04[9:0]	区域4的起始阈值	区域4的起始阈值。无符号10位整数。	R/W
b31 to b30	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note: 此设置反映到垂直同步信号（输入）断言的内部操作时
GAMx_LATCH.VEN=1或当所有模块的内部操作的寄存器值反射控制信号被断言时。

TH06[9:0]位（区域6的起始阈值）

TH06[9:0]位以无符号10位整数的形式指定要用于伽马校正的区域6的起始阈值。

TH05[9:0]位（区域5的起始阈值）

TH05[9:0]位以无符号10位整数的形式指定要用于伽马校正的区域5的起始阈值。

TH04[9:0]位（区域4的起始阈值）

TH04[9:0]位以无符号10位整数的形式指定要用于伽马校正的区域4的起始阈值。

58.2.40 Gamma G Correction Block Area Setting Register 3 (GAMG_AREA3) Gamma B Correction Block Area Setting Register 3 (GAMB_AREA3) Gamma R Correction Block Area Setting Register 3 (GAMR_AREA3)

Address(es): GLCDC.GAMG_AREA3 400E 1330h, GLCDC.GAMB_AREA3 400E 1370h, GLCDC.GAMR_AREA3 400E 13B0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	TH07[9:0]										TH08[9:6]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TH08[5:0]						TH09[9:0]									
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b9 to b0	TH09[9:0]	Start Threshold of Area 9	Start threshold of area 9. Unsigned 10-bit integer.	R/W
b19 to b10	TH05[9:6], TH08[5:0]	Start Threshold of Area 8	Start threshold of area 8. Unsigned 10-bit integer.	R/W
b29 to b20	TH07[9:0]	Start Threshold of Area 7	Start threshold of area 7. Unsigned 10-bit integer.	R/W
b31 to b30	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: This setting is reflected to the internal operations on assertion of the vertical synchronization signal (input) when GAMx_LATCH.VEN = 1 or when the register value reflection control signal to internal operations for all the modules is asserted.

TH09[9:0] bits (Start Threshold of Area 9)

The TH09[9:0] bits specify the start threshold of area 9 to be used for gamma correction in terms of an unsigned 10-bit integer.

TH08[5:0] bits (Start Threshold of Area 8)

The TH08[9:0] bits specify the start threshold of area 8 to be used for gamma correction in terms of an unsigned 10-bit integer.

TH07[9:0] bits (Start Threshold of Area 7)

The TH07[9:0] bits specify the start threshold of area 7 to be used for gamma correction in terms of an unsigned 10-bit integer.

58.2.40 GammaG校正块区域设置寄存器3(GAMG_AREA3)GammaB校正块区域设置寄存器3(GAMB_AREA3)GammaR校正块区域设置寄存器3(GAMR_AREA3)

Address(es): GLCDC.GAMG_AREA3 400E 1330h, GLCDC.GAMB_AREA3 400E 1370h, GLCDC.GAMR_AREA3 400E 13B0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	TH07[9:0]										TH08[9:6]			
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TH08[5:0]						TH09[9:0]									
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b9 to b0	TH09[9:0]	区域9的起始阈值	区域9的起始阈值。无符号10位整数。	R/W
b19 to b10	TH05[9:6], TH08[5:0]	8区开始门槛	区域8的起始阈值。无符号10位整数。	R/W
b29 to b20	TH07[9:0]	区域7的起始阈值	区域7的起始阈值。无符号10位整数。	R/W
b31 to b30	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note: 此设置反映到垂直同步信号（输入）断言的内部操作时
GAMx_LATCH.VEN=1或当所有模块的内部操作的寄存器值反射控制信号被断言时。

TH09[9:0]位（区域9的起始阈值）

TH09[9:0]位以无符号10位整数的形式指定用于伽马校正的区域9的起始阈值。

TH08[5:0]位（区域8的起始阈值）

TH08[9:0]位以无符号10位整数的形式指定要用于伽马校正的区域8的起始阈值。

TH07[9:0]位（区域7的起始阈值）

TH07[9:0]位以无符号10位整数的形式指定要用于伽马校正的区域7的起始阈值。

58.2.41 Gamma G Correction Block Area Setting Register 4 (GAMG_AREA4) Gamma B Correction Block Area Setting Register 4 (GAMB_AREA4) Gamma R Correction Block Area Setting Register 4 (GAMR_AREA4)

Address(es): GLCDC.GAMG_AREA4 400E 1334h, GLCDC.GAMB_AREA4 400E 1374h, GLCDC.GAMR_AREA4 400E 13B4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	TH10[9:0]										TH11[9:6]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TH11[5:0]						TH12[9:0]									
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b9 to b0	TH12[9:0]	Start Threshold of Area 12	Start threshold of area 12. Unsigned 10-bit integer.	R/W
b19 to b10	TH08[9:6], TH11[5:0]	Start Threshold of Area 11	Start threshold of area 11. Unsigned 10-bit integer.	R/W
b29 to b20	TH10[9:0]	Start Threshold of Area 10	Start threshold of area 10. Unsigned 10-bit integer.	R/W
b31, b30	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: This setting is reflected to the internal operations on assertion of the vertical synchronization signal (input) when GAMx_LATCH.VEN = 1 or when the register value reflection control signal to internal operations for all the modules is asserted.

TH12[9:0] bits (Start Threshold of Area 12)

The TH12[9:0] bits specify the start threshold of area 12 to be used for gamma correction in terms of an unsigned 10-bit integer.

TH11[5:0] bits (Start Threshold of Area 11)

The TH11[9:0] bits specify the start threshold of area 11 to be used for gamma correction in terms of an unsigned 10-bit integer.

TH10[9:0] bits (Start Threshold of Area 10)

The TH10[9:0] bits specify the start threshold of area 10 to be used for gamma correction in terms of an unsigned 10-bit integer.

58.2.41 GammaG校正块区域设置寄存器4(GAMG_AREA4)GammaB校正块区域设置寄存器4(GAMB_AREA4)GammaR校正块区域设置寄存器4(GAMR_AREA4)

Address(es): GLCDC.GAMG_AREA4 400E 1334h, GLCDC.GAMB_AREA4 400E 1374h, GLCDC.GAMR_AREA4 400E 13B4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	TH10[9:0]										TH11[9:6]			
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TH11[5:0]						TH12[9:0]									
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b9 to b0	TH12[9:0]	12区开始门槛	区域12的起始阈值。无符号10位整数。	R/W
b19 to b10	TH08[9:6], TH11[5:0]	11区开始门槛	区域11的起始阈值。无符号10位整数。	R/W
b29 to b20	TH10[9:0]	区域10的起始阈值	区域10的起始阈值。无符号10位整数。	R/W
b31, b30	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note: 此设置反映到垂直同步信号（输入）断言的内部操作时
GAMx_LATCH.VEN=1或当所有模块的内部操作的寄存器值反射控制信号被断言时。

TH12[9:0]位（区域12的起始阈值）

TH12[9:0]位以无符号10位整数的形式指定用于伽马校正的区域12的起始阈值。

TH11[5:0]位（区域11的起始阈值）

TH11[9:0]位以无符号10位整数的形式指定要用于伽马校正的区域11的起始阈值。

TH10[9:0]位（区域10的起始阈值）

TH10[9:0]位以无符号10位整数的形式指定要用于伽马校正的区域10的起始阈值。

58.2.42 Gamma G Correction Block Area Setting Register 5 (GAMG_AREA5) Gamma B Correction Block Area Setting Register 5 (GAMB_AREA5) Gamma R Correction Block Area Setting Register 5 (GAMR_AREA5)

Address(es): GLCDC.GAMG_AREA5 400E 1338h, GLCDC.GAMB_AREA5 400E 1378h, GLCDC.GAMR_AREA5 400E 13B8h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	TH13[9:0]										TH14[9:6]			
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TH14[5:0]						TH15[9:0]									
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b9 to b0	TH15[9:0]	Start Threshold of Area 15	Start threshold of area 15. Unsigned 10-bit integer.	R/W
b19 to b10	TH11[9:6], TH14[5:0]	Start Threshold of Area 14	Start threshold of area 14. Unsigned 10-bit integer.	R/W
b29 to b20	TH13[9:0]	Start Threshold of Area 13	Start threshold of area 13. Unsigned 10-bit integer.	R/W
b31, b30	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: This setting is reflected to the internal operations on assertion of the vertical synchronization signal (input) when GAMx_LATCH.VEN = 1 or when the register value reflection control signal to internal operations for all the modules is asserted.

TH15[9:0] bits (Start Threshold of Area 15)

The TH15[9:0] bits specify the start threshold of area 15 to be used for gamma correction in terms of an unsigned 10-bit integer.

TH14[9:0] bits (Start Threshold of Area 14)

The TH14[9:0] bits specify the start threshold of area 14 to be used for gamma correction in terms of an unsigned 10-bit integer.

TH13[9:0] bits (Start Threshold of Area 13)

The TH13[9:0] bits specify the start threshold of area 13 to be used for gamma correction in terms of an unsigned 10-bit integer.

58.2.42 GammaG校正块区域设置寄存器5(GAMG_AREA5)GammaB校正块区域设置寄存器5(GAMB_AREA5)GammaR校正块区域设置寄存器5(GAMR_AREA5)

Address(es): GLCDC.GAMG_AREA5 400E 1338h, GLCDC.GAMB_AREA5 400E 1378h, GLCDC.GAMR_AREA5 400E 13B8h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	TH13[9:0]										TH14[9:6]			
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	TH14[5:0]						TH15[9:0]									
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b9 to b0	TH15[9:0]	15区开始门槛	区域15的起始阈值。无符号10位整数。	R/W
b19 to b10	TH11[9:6], TH14[5:0]	14区开始门槛	区域14的起始阈值。无符号10位整数。	R/W
b29 to b20	TH13[9:0]	13区开始门槛	区域13的起始阈值。无符号10位整数。	R/W
b31, b30	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note: 此设置反映到垂直同步信号（输入）断言的内部操作时
GAMx_LATCH.VEN=1或当所有模块的内部操作的寄存器值反射控制信号被断言时。

TH15[9:0]位（区域15的起始阈值）

TH15[9:0]位以无符号10位整数的形式指定用于伽马校正的区域15的起始阈值。

TH14[9:0]位（区域14的起始阈值）

TH14[9:0]位以无符号10位整数的形式指定要用于伽马校正的区域14的起始阈值。

TH13[9:0]位（区域13的起始阈值）

TH13[9:0]位以无符号10位整数的形式指定用于伽马校正的区域13的起始阈值。

58.2.43 Output Control Block Register Update Control Register (OUT_VLATCH)

Address(es): GLCDC.OUT_VLATCH 400E 13C0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VEN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	VEN	Control of Output Control Module Register Value Reflection to Internal Operations	0: Disable reflection of register values to internal operations on assertion of vertical synchronization signal (VS) 1: Enable reflection of register values to internal operations on assertion of vertical synchronization signal (VS).	R/W
b31 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

VEN bit (Control of Output Control Module Register Value Reflection to Internal Operations)

The VEN bit enables or disables reflection of the register values to the internal operations in the output control circuit on assertion of the vertical synchronization signal (input). When this bit is set to 1, the register values are immediately reflected to the internal operations on assertion of the vertical synchronization signal (input), and then this bit automatically clears to 0. Also, if the signal is asserted that controls reflection of the register values to the internal operations of all the modules output from the ground plane generation module, the register values are reflected to the internal operations on assertion of the vertical synchronization signal (input), regardless of the value of this bit. While this bit is 1, do not modify any register whose value is reflected to the internal operations on assertion of the vertical synchronization signal (input) in the GLCDC. Otherwise, operation is not guaranteed.

This bit must not be 1 at the same time as the BG_EN.VEN bit (control of background plane register value reflection to internal operations) in the Operation Control Register (BG_EN), one of the background plane setting registers. Otherwise, operation is not guaranteed.

58.2.43 输出控制块寄存器更新控制寄存器(OUT_VLATCH)

Address(es): GLCDC.OUT_VLATCH 400E 13C0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VEN
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	VEN	输出控制模块的控制 注册值反射到 内部运营	0：禁止将寄存器值反映到内部 垂直同步信号(VS)1的断言操作：启用寄存器值到内部的反射 垂直同步信号（VS）的断言操作。	R/W
b31 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

VEN位（输出控制模块寄存器值反映到内部操作的控制）

VEN位启用或禁用寄存器值在垂直同步信号（输入）置位时反映到输出控制电路中的内部操作。当该位设置为1时，寄存器值立即反映到垂直同步信号（输入）断言的内部操作，然后该位自动清除为0。此外，如果该信号被断言，控制反射寄存器值反映到地平面生成模块输出的所有模块的内部操作，无论该位的值如何，寄存器值都反映到垂直同步信号（输入）有效时的内部操作。当该位为1时，不要修改其值反映到GLCDC中垂直同步信号（输入）断言的内部操作的任何寄存器。否则，无法保证操作。

该位不能与后台平面设置寄存器之一的操作控制寄存器(BG_EN)中的BG_EN.VEN位（控制后台平面寄存器值反映到内部操作）同时为1。否则，无法保证操作。

58.2.44 Output Control Block Output Interface Register (OUT_SET)

Address(es): GLCDC.OUT_SET 400E 13C4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	ENDIANON	—	—	—	SWAPON	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	FORMAT[1:0]		—	—	FRQSEL[1:0]		—	—	—	DIRSEL	—	—	PHASE[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	PHASE[1:0]	Data Output Delay Control in Serial RGB Format	Data delay in LCD_CLK cycles. b1 b0 0 0: 0 cycle 0 1: 1 cycle 1 0: 2 cycles 1 1: 3 cycles.	R/W
b3, b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	DIRSEL	Scan Direction Select of Serial RGB Format	0: Forward scan 1: Reverse scan.	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b9, b8	FRQSEL[1:0]	Clock Frequency Division Control	b9 b8 0 0: No frequency division, parallel RGB 0 1: Setting prohibited 1 0: Quarter frequency (serial RGB) 1 1: Setting prohibited.	R/W
b11, b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b13, b12	FORMAT[1:0]	Output Format Select	b13 b12 0 0: RGB888; select RGB888 as dither output format 0 1: RGB666; select RGB666 as dither output format 1 0: RGB565; select RGB565 as dither output format 1 1: Serial RGB; select RGB888 as dither output format. Select dither output format in OUT_PDTHA.FORM[1:0].	R/W
b23 to b14	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b24	SWAPON	Pixel Order Control	0: RGB order 1: BGR order.	R/W
b27 to b25	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b28	ENDIANON	Bit Endian Control	0: Descending order (little endian) 1: Ascending order (big endian).	R/W
b31 to b29	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Rewriting these bits is prohibited during operation. Set the settings before operation is enabled. Operation is not guaranteed if the bit is rewritten during operation.

For details on assignment of pixel data to the output pins (LCD_DATA23 to LCD_DATA00) by setting these bits (except for OUT_SET.FRQSEL[1:0]), see Figure 58.3 to Figure 58.6.

PHASE[1:0] bits (Data Output Delay Control in Serial RGB Format)

The PHASE[1:0] bits control data output delay in serial RGB format. When the delay is 0 cycles (these bits are 00b), pixel data (R, B, or invalid data, depending on the setting in this register) is output one pixel clock (PXCLK) cycle after the horizontal data enable signal (HE). When any value other than 00b is set to OUT_SET.PHASE[1:0], pixel data output is delayed for a preset number of LCD_CLK cycles.

58.2.44 输出控制块输出接口寄存器(OUT_SET)

Address(es): GLCDC.OUT_SET 400E 13C4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	ENDIANON	—	—	—	换上	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	FORMAT[1:0]		—	—	FRQSEL[1:0]		—	—	—	DIRSEL	—	—	PHASE[1:0]	
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b1, b0	PHASE[1:0]	数据输出延迟控制 串行RGB格式	LCD_CLK周期中的数据延迟。b 1b000：0周期01：1周期10： 2周期11：3周期。	R/W
b3, b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b4	DIRSEL	串行扫描方向选择 RGB Format	0：正向扫描1： 反向扫描。	R/W
b7 to b5	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b9, b8	FRQSEL[1:0]	时钟分频 Control	b9b800：不分频，并行RGB01：禁止设置 10：四分之一频率（串行RGB）11：禁止 设置。	R/W
b11, b10	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b13, b12	FORMAT[1:0]	输出格式选择	b13b1200：RGB888；选择RGB888作为抖动输出格式01：RGB666；选择RGB666作为抖动输出格式10：RGB565；选择RGB565作为抖动输出格式11：串行RGB；选择RGB888作为抖动输出格式。在OUT_PDTHA.FORM[1:0]中选择抖动输出格式。	R/W
b23 to b14	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b24	SWAPON	像素顺序控制	0: RGB order 1: BGR order.	R/W
b27 to b25	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b28	ENDIANON	位字节序控制	0：降序（小端）1：升序（大端 ）。	R/W
b31 to b29	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note: 操作期间禁止改写这些位。在启用操作之前进行设置。如果在操作期间重写该位，则无法保证操作。

有关通过设置这些位（OUT_SET.FRQSEL[1:0]除外）将像素数据分配到输出引脚（LCD_DATA23至LCD_DATA00）的详细信息，请参见图58.3至图58.6。

PHASE[1:0]位（串行RGB格式的数据输出延迟控制）

PHASE[1:0]位控制串行RGB格式的数据输出延迟。当延迟为0个周期（这些位为00b）时，像素数据（R、B或无效数据，取决于此寄存器中的设置）在水平数据使能信号(HE)后一个像素时钟(PXCLK)周期输出.当00b以外的任何值设置为OUT_SET.PHASE[1:0]时，像素数据输出会延迟预设数量的LCD_CLK周期。

DIRSEL bit (Scan Direction Select of Serial RGB Format)

The DIRSEL bit controls the data arrangement of the serial RGB format. When this bit is set to 1, the serial RGB data is arranged in reverse direction, and when it is 0, the serial RGB is arranged in forward direction.

FRQSEL[1:0] bits (Clock Frequency Division Control)

The FRQSEL[1:0] bits control clock frequency division of LCD_CLK (panel output clock) and PXCLK (pixel clock for internal operations). Set these bits to 10b only for the serial RGB format (OUT_SET.FORMAT[1:0] = 11b), so that PXCLK has a quarter frequency of the LCD_CLK frequency and synchronizes with LCD_CLK. Set these bits to 00b for the parallel RGB format (OUT_SET.FORMAT[1:0] = 10b, 01b, or 00b), so that PXCLK has the same frequency as the LCD_CLK frequency and synchronizes with LCD_CLK. Otherwise, operation is not guaranteed.

FORMAT[1:0] bits (Output Format Select)

The FORMAT[1:0] bits select the output format of RGB data. Set these bits in accordance with the output format select bits in the Panel Dither Correction Register (OUT_PDTHA.FORM[1:0]). For serial RGB format (these bits are 11b), set OUT_PDTHA.FORM[1:0] to 00b. Otherwise, operation is not guaranteed.

SWAPON bit (Pixel Order Control)

The SWAPON bit controls the pixel order of RGB data output. When this bit is set to 1, internally processed data is assigned to the output pins in BGR order, and when this bit is 0, data is assigned in the RGB order. Data is assigned to the output pins (LCD_DATA23 to LCD_DATA00) with the MSB first for the RGB parallel format, and serially for the RGB serial format.

ENDIANON bit (Bit Endian Control)

The ENDIANON bit controls the bit order of RGB data output. When this bit is set to 1, internally processed data is assigned to the output pins in ascending order (big endian), and when this bit is 0, data is assigned in descending order (little endian).

58.2.45 Output Control Block Brightness Correction Register 1 (OUT_BRIGHT1)

Address(es): GLCDC.OUT_BRIGHT1 400E 13C8h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	BRTG[9:0]									
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b9 to b0	BRTG[9:0]	Brightness Adjustment of G Signal	Brightness (DC) adjustment of G signal. Unsigned 10-bit integer; +512 with offset.	R/W
b31 to b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: This setting is reflected to the internal operations on assertion of the vertical synchronization signal (input) when OUT_VLATCH.VEN = 1 or when the register value reflection control signal to internal operations for all the modules is asserted.

BRTG[9:0] bits (Brightness Adjustment of G Signal)

The BRTG[9:0] bits specify the brightness (DC) adjustment of the G signal.

Brightness correction of the G signal is performed as follows:

- Gout: Output of brightness correction (input of contrast correction); unsigned; 10 bits

DIRSEL位（串行RGB格式的扫描方向选择）

DIRSEL位控制串行RGB格式的数据排列。该位为1时，串行RGB数据反向排列，为0时，串行RGB数据正向排列。

FRQSEL[1:0]位（时钟分频控制）

FRQSEL[1:0]位控制LCD_CLK（面板输出时钟）和PXCLK（用于内部操作的像素时钟）的时钟分频。仅针对串行RGB格式(OUT_SET.FORMAT[1:0]=11b)将这些位设置为10b，以便PXCLK具有LCD_CLK频率的四分之一频率并与LCD_CLK同步。对于并行RGB格式（OUT_SET.FORMAT[1:0]=10b、01b或00b）将这些位设置为00b，以便PXCLK与LCD_CLK频率具有相同的频率并与LCD_CLK同步。否则，无法保证操作。

FORMAT[1:0]位（输出格式选择）

FORMAT[1:0]位选择RGB数据的输出格式。根据面板抖动校正寄存器(OUT_PDTHA.FORM[1:0])中的输出格式选择位设置这些位。对于串行RGB格式（这些位为11b），将OUT_PDTHA.FORM[1:0]设置为00b。否则，无法保证操作。

SWAPON位（像素顺序控制）

SWAPON位控制RGB数据输出的像素顺序。当此位设置为1时，内部处理的数据按BGR顺序分配给输出引脚，当此位为0时，数据按RGB顺序分配。对于RGB并行格式，数据分配到输出引脚（LCD_DATA23到LCD_DATA00），MSB在前，对于RGB串行格式，数据以串行方式分配。

ENDIANON位（位字节序控制）

ENDIANON位控制RGB数据输出的位顺序。当该位设置为1时，内部处理的数据按升序（大端）分配给输出引脚，当该位为0时，数据按降序（小端）分配。

58.2.45 输出控制块亮度校正寄存器1(OUT_BRIGHT1)

Address(es): GLCDC.OUT_BRIGHT1 400E 13C8h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	BRTG[9:0]									
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b9 to b0	BRTG[9:0]	G信号亮度调节	G信号的亮度（DC）调整。无符号10位整数；+512带偏移量。	R/W
b31 to b10	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note: 此设置反映到垂直同步信号（输入）断言的内部操作时
OUT_VLATCH.VEN=1或当所有模块的内部操作的寄存器值反射控制信号被断言时。

BRTG[9:0]位（G信号亮度调节）

BRTG[9:0]位指定G信号的亮度(DC)调整。

G信号的亮度校正如下进行：

- Gout：亮度校正的输出（对比度校正的输入）；未签名；10位

- Gin: Input of brightness correction; unsigned; 10 bits
- BRTG: Setting in this bit
- Gout = Gin + BRTG - 512.

58.2.46 Output Control Block Brightness Correction Register 2 (OUT_BRIGHT2)

Address(es): GLCDC.OUT_BRIGHT2 400E 13CCh

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	BRTB[9:0]									
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	BRTR[9:0]									
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b9 to b0	BRTR[9:0]	Brightness Adjustment of R Signal	Brightness (DC) adjustment of R signal. Unsigned 10-bit integer; +512 with offset.	R/W
b15 to b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b25 to b16	BRTB[9:0]	Brightness Adjustment of B Signal	Brightness (DC) adjustment of B signal. Unsigned 10-bit integer; +512 with offset.	R/W
b31 to b26	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: This setting is reflected to the internal operations on assertion of the vertical synchronization signal (input) when OUT_VLATCH.VEN = 1 or when the register value reflection control signal to internal operations for all the modules is asserted.

BRTR[9:0] bits (Brightness Adjustment of R Signal)

The BRTR[9:0] bits specify the brightness (DC) adjustment of the R signal.

Brightness correction of the R signal is performed as follows:

- Rout: Output of brightness correction (input of contrast correction); unsigned; 10 bits
- Rin: Input of brightness correction; unsigned; 10 bits
- BRTR: Setting in this bit
- Rout = Rin + BRTR - 512.

BRTB[9:0] bits (Brightness Adjustment of B Signal)

The BRTB[9:0] bits specify the brightness (DC) adjustment of the B signal.

Brightness correction of the B signal is performed as follows:

- Bout: Output of brightness correction (input of contrast correction); unsigned; 10 bits
- Bin: Input of brightness correction; unsigned; 10 bits
- BRTB: Setting in this bit
- Bout = Bin + BRTB - 512.

- Gin：亮度校正的输入；未签名；10位
- BRTG：在该位设置
- 痛风=杜松子酒+BRTG512。

58.2.46 输出控制块亮度校正寄存器2(OUT_BRIGHT2)

Address(es): GLCDC.OUT_BRIGHT2 400E 13CCh

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	BRTB[9:0]									
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	BRTR[9:0]									
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b9 to b0	BRTR[9:0]	R信号的亮度调整	R信号的亮度(DC)调整。无符号10位整数；+512带偏移量。	R/W
b15 to b10	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b25 to b16	BRTB[9:0]	B信号亮度调节	B信号的亮度(DC)调整。无符号10位整数；+512带偏移量。	R/W
b31 to b26	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note: 此设置反映到垂直同步信号（输入）断言的内部操作时
OUT_VLATCH.VEN=1或当所有模块的内部操作的寄存器值反射控制信号被断言时。

BRTR[9:0]位（R信号亮度调整）

BRTR[9:0]位指定R信号的亮度(DC)调整。

R信号的亮度校正如下执行：

- Rout：亮度校正的输出（对比度校正的输入）；未签名；10位
- Rin：亮度校正输入；未签名；10位
- BRTR：在该位设置
- Rout=Rin+BRTR512。

BRTB[9:0]位（B信号亮度调节）

BRTB[9:0]位指定B信号的亮度(DC)调整。

B信号的亮度校正如下进行：

- Bout：亮度校正的输出（对比度校正的输入）；未签名；10位
- Bin：亮度校正输入；未签名；10位
- BRTB：在该位设置
- 布特=斌+BRTB512。

58.2.47 Output Control Block Contrast Correction Register (OUT_CONTRAST)

Address(es): GLCDC.OUT_CONTRAST 400E 13D0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	CONTG[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CONTB[7:0]								CONTR[7:0]							
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b7 to b0	CONTR[7:0]	Contrast Adjustment of R Signal	Unsigned 8-bit fixed point value adjusting GAIN on R signal. 00h: 0/128 = 0.000 : 80h: 128/128 = 1.000 : FFh: 255/128 = 1.992.	R/W
b15 to b8	CONTB[7:0]	Contrast Adjustment of B Signal	Unsigned 8-bit fixed point value adjusting GAIN on B signal. 00h: 0/128 = 0.000 : 80h: 128/128 = 1.000 : FFh: 255/128 = 1.992.	R/W
b23 to b16	CONTG[7:0]	Contrast Adjustment of G Signal	Unsigned 8-bit fixed point value adjusting GAIN on G signal. 00h: 0/128 = 0.000 : 80h: 128/128 = 1.000 : FFh: 255/128 = 1.992.	R/W
b31 to b24	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: This setting is reflected to the internal operations on assertion of the vertical synchronization signal (input) when OUT_VLATCH.VEN = 1 or when the register value reflection control signal to internal operations for all the modules is asserted.

CONTR[7:0] bits (Contrast Adjustment of R Signal)

The CONTR[7:0] bits specify the contrast (GAIN) adjustment of R signal. The location of the decimal point is between bit [7] and [6].

CONTB[7:0] bits (Contrast Adjustment of B Signal)

The CONTB[7:0] bits specify the contrast (GAIN) adjustment of B signal. The location of the decimal point is between bit [7] and [6].

CONTG[7:0] bits (Contrast Adjustment of G Signal)

The CONTG[7:0] bits specify the contrast (GAIN) adjustment of G signal. The location of the decimal point is between bit [7] and [6].

Contrast correction of each pixel is performed as follows (x = R, G, B):

- Dxout: Output of contrast correction; unsigned; 10 bits
- Dxin: Input of contrast correction (output of brightness correction); unsigned; 10 bits
- CONTx: Setting in this bit

58.2.47 输出控制块对比度校正寄存器(OUT_CONTRAST)

Address(es): GLCDC.OUT_CONTRAST 400E 13D0h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	CONTG[7:0]							
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	CONTB[7:0]								CONTR[7:0]							
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b7 to b0	CONTR[7:0]	R信号的对比度调整	在R信号上调整GAIN的无符号8位定点值。00h：0128=0.000 : 80h: 128/128 = 1.000 : FFh: 255/128 = 1.992.	R/W
b15 to b8	CONTB[7:0]	B信号的对比度调整	在B信号上调整增益的无符号8位定点值。00h：0128=0.000 : 80h: 128/128 = 1.000 : FFh: 255/128 = 1.992.	R/W
b23 to b16	CONTG[7:0]	G信号的对比度调整	在G信号上调整GAIN的无符号8位定点值。00h：0128=0.000 : 80h: 128/128 = 1.000 : FFh: 255/128 = 1.992.	R/W
b31 to b24	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note: 此设置反映到垂直同步信号（输入）断言的内部操作时
OUT_VLATCH.VEN=1或当所有模块的内部操作的寄存器值反射控制信号被断言时。

CONTR[7:0]位（R信号的对比度调整）

CONTR[7:0]位指定R信号的对比度(GAIN)调整。小数点的位置在位[7]和[6]之间。

CONTB[7:0]位（B信号对比度调整）

CONTB[7:0]位指定B信号的对比度(GAIN)调整。小数点的位置在位[7]和[6]之间。

CONTG[7:0]位（G信号对比度调整）

CONTG[7:0]位指定G信号的对比度(GAIN)调整。小数点的位置在位[7]和[6]之间。

每个像素的对比度校正执行如下（x=R，G，B）：

- Dxout：对比度校正的输出；未签名；10位
- Dxin：对比度校正的输入（亮度校正的输出）；未签名；10位
- CONTx：在该位中设置

- Dxout = Dxin × CONTx.

58.2.48 Output Control Block Panel Dither Correction Register (OUT_PDTHA)

Address(es): GLCDC.OUT_PDTHA 400E 13D4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	SEL[1:0]		—	—	FORM[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	PA[1:0]		—	—	PB[1:0]		—	—	PC[1:0]		—	—	PD[1:0]	
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b1, b0	PD[1:0]	Pattern Value (D) of 2×2 Pattern Dither	Pattern value (D) of 2×2 pattern dither. Unsigned 2-bit integer.	R/W
b3, b2	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b5, b4	PC[1:0]	Pattern Value (C) of 2×2 Pattern Dither	Pattern value (C) of 2×2 pattern dither. Unsigned 2-bit integer.	R/W
b7, b6	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b9, b8	PB[1:0]	Pattern Value (B) of 2×2 Pattern Dither	Pattern value (B) of 2×2 pattern dither. Unsigned 2-bit integer.	R/W
b11, b10	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b13, b12	PA[1:0]	Pattern Value (A) of 2×2 Pattern Dither	Pattern value (A) of 2×2 pattern dither. Unsigned 2-bit integer.	R/W
b15, b14	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b17, b16	FORM[1:0]	Output Format Select	b17 b16 0 0: RGB888; select RGB888 or serial RGB as output interface format 0 1: RGB666; select RGB666 as output interface format 1 0: RGB565; select RGB565 as output interface format 1 1: Setting prohibited. Select output interface format in OUT_SET.FORMAT[1:0].	R/W
b19, b18	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b21, b20	SEL[1:0]	Operation Mode	b21 b20 0 0: Truncate 0 1: Round-off 1 0: 2×2 pattern dither 1 1: Setting prohibited.	R/W
b31 to b22	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: This setting is reflected to the internal operations on assertion of the vertical synchronization signal (input) when OUT_VLATCH.VEN = 1 or when the register value reflection control signal to internal operations for all the modules is asserted.

PA[1:0], PB[1:0], PC[1:0], PD[1:0] bits (Pattern Value (A, B, C, D) of 2×2 Pattern Dither)

The PA[1:0], PB[1:0], PC[1:0], and PD[1:0] bits specify the pattern value A, B, C, and D of 2×2 pattern dither. Figure 58.13 shows the configuration of the dither correction block.

FORM[1:0] bits (Output Format Select)

The FORM[1:0] bits specify the output format of the dither process. These bits must be set in accordance with the OUT_SET.FORMAT[1:0] bits of the Output Interface Register. For serial RGB (OUT_SET.FORMAT[1:0] = 11b), set these bits to 00b. Otherwise, operation is not guaranteed.

- Dxout = Dxin × CONTx.

58.2.48 输出控制块面板抖动校正寄存器(OUT_PDTHA)

Address(es): GLCDC.OUT_PDTHA 400E 13D4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	SEL[1:0]		—	—	FORM[1:0]	
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	PA[1:0]		—	—	PB[1:0]		—	—	PC[1:0]		—	—	PD[1:0]	
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b1, b0	PD[1:0]	2×2图案的图案值（D）Dither	2×2图案抖动的图案值(D)。无符号2位整数。	R/W
b3, b2	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b5, b4	PC[1:0]	2×2图案的图案值（C）Dither	2×2图案抖动的图案值(C)。无符号2位整数。	R/W
b7, b6	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b9, b8	PB[1:0]	2×2图案的图案值（B）Dither	2×2图案抖动的图案值(B)。无符号2位整数。	R/W
b11, b10	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b13, b12	PA[1:0]	2×2图案的图案值（A）Dither	2×2图案抖动的图案值(A)。无符号2位整数。	R/W
b15, b14	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b17, b16	FORM[1:0]	输出格式选择	b17b1600：RGB888；选择RGB888或串行RGB作为输出接口格式01：RGB666；选择RGB666作为输出接口格式10：RGB565；输出接口格式选择RGB56511：禁止设置。在OUT_SET.FORMAT[1:0]中选择输出接口格式。	R/W
b19, b18	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b21, b20	SEL[1:0]	操作模式	b21b2000：截断01：舍入10：2×2图案抖动11：禁止设置。	R/W
b31 to b22	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note: 此设置反映到垂直同步信号（输入）断言的内部操作时
OUT_VLATCH.VEN=1或当所有模块的内部操作的寄存器值反射控制信号被断言时。

PA[1:0] PB[1:0] PC[1:0] PD[1:0]bits(2×2PatternDither的PatternValue(A B C D))

PA[1:0]、PB[1:0]、PC[1:0]和PD[1:0]位指定2×2模式抖动的模式值A、B、C和D。图58.13显示了抖动校正模块的配置。

FORM[1:0]位（输出格式选择）

FORM[1:0]位指定抖动过程的输出格式。这些位必须按照
输出接口寄存器的OUT_SET.FORMAT[1:0]位。对于串行RGB(OUT_SET.FORMAT[1:0]=11b)，将这些位设置为00b。否则，无法保证操作。

SEL[1:0] bits (Operation Mode)

The SEL[1:0] bits specify the dither operation mode. The dither process is performed for the bits equal to or shorter than the pixel data length selected in the output format select bits (OUT_PDTHA.FORM[1:0]). OUT_PDTHA.PA[1:0], PB[1:0], PC[1:0], and PD[1:0] are used for 2×2 pattern dither.

Figure 58.13 shows the configuration of the dither correction block.

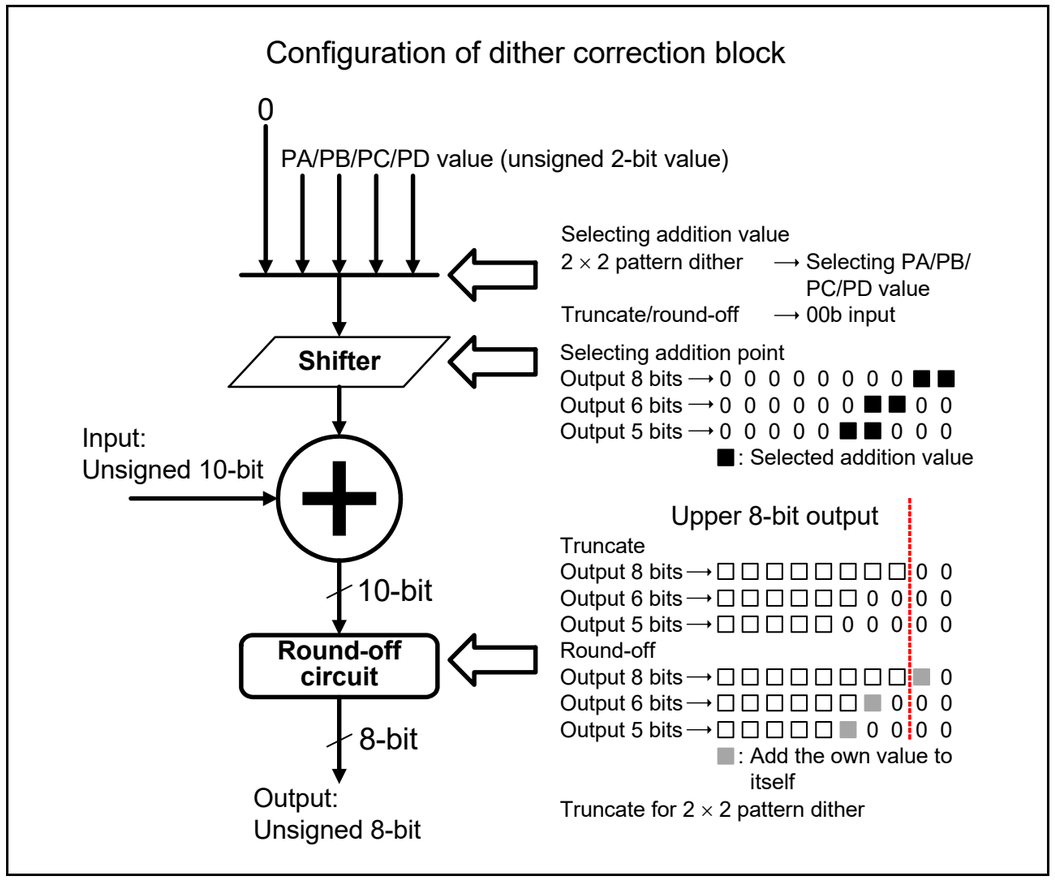


Figure 58.13 Configuration of dither correction block

Figure 58.14 shows the addition value selection method for 2×2 pattern dither.

SEL[1:0]位（操作模式）

SEL[1:0]位指定抖动操作模式。对等于或短于在输出格式选择位(OUT_PDTHA.FORM[1:0])中选择的像素数据长度的位执行抖动处理。OUT_PDTHA.PA[1:0]、PB[1:0]、PC[1:0]和PD[1:0]用于2×2模式抖动。

图58.13显示了抖动校正模块的配置。

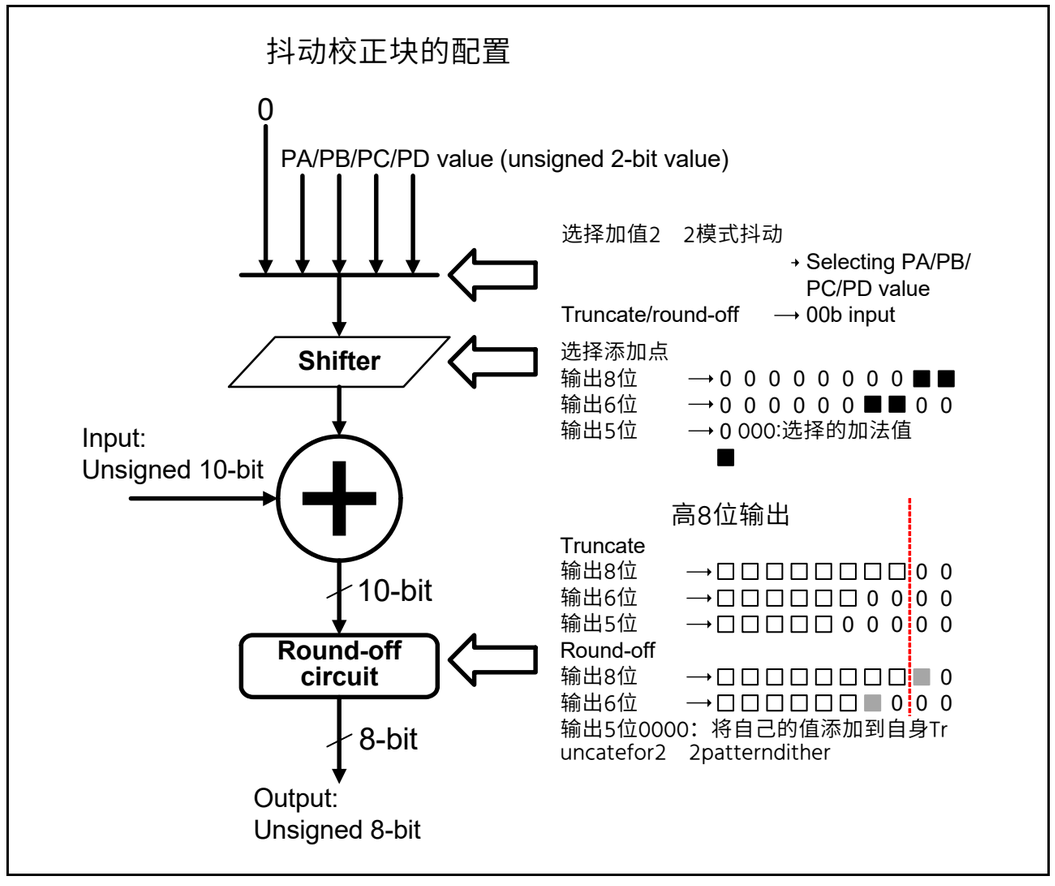


Figure 58.13 抖动校正块的配置

图58.14显示了2×2模式抖动的加值选择方法。

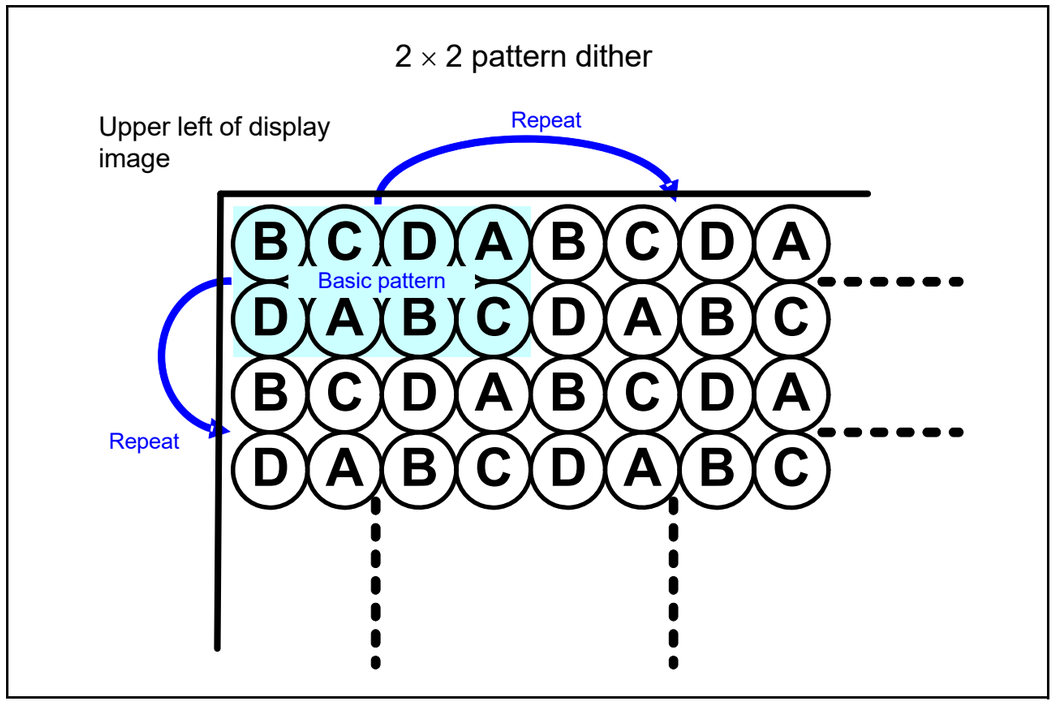
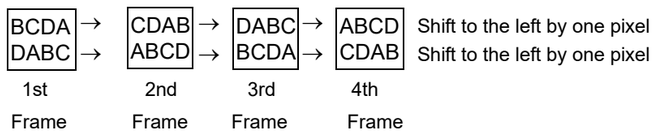


Figure 58.14 Addition value selection method for 2×2 pattern dither

A basic pattern is repeated as follows. Four frames constitute 1 cycle.



- A: Value obtained after OUT_PDTHA.PA[1:0] bit value is shifted in accordance with the output format
- B: Value obtained after OUT_PDTHA.PB[1:0] bit value is shifted in accordance with the output format
- C: Value obtained after OUT_PDTHA.PC[1:0] bit value is shifted in accordance with the output format
- D: Value obtained after OUT_PDTHA.PD[1:0] bit value is shifted in accordance with the output format

Renesas recommends setting the bits as follows: PA[1:0] = 11b, PB[1:0] = 00b, PC[1:0] = 10b, PD[1:0] = 01b

When 2×2 pattern dither (OUT_PDTHA.SEL[1:0] = 10b) is to be set, the valid pixel area of the background plane must be an integer multiple of the basic pattern. If serial RGB is selected as the output format for the output control block, add two to the horizontal valid pixel width and set the resulting value to the background plane horizontal valid pixel width bits (BG_HSIZE.HW[10:0]).

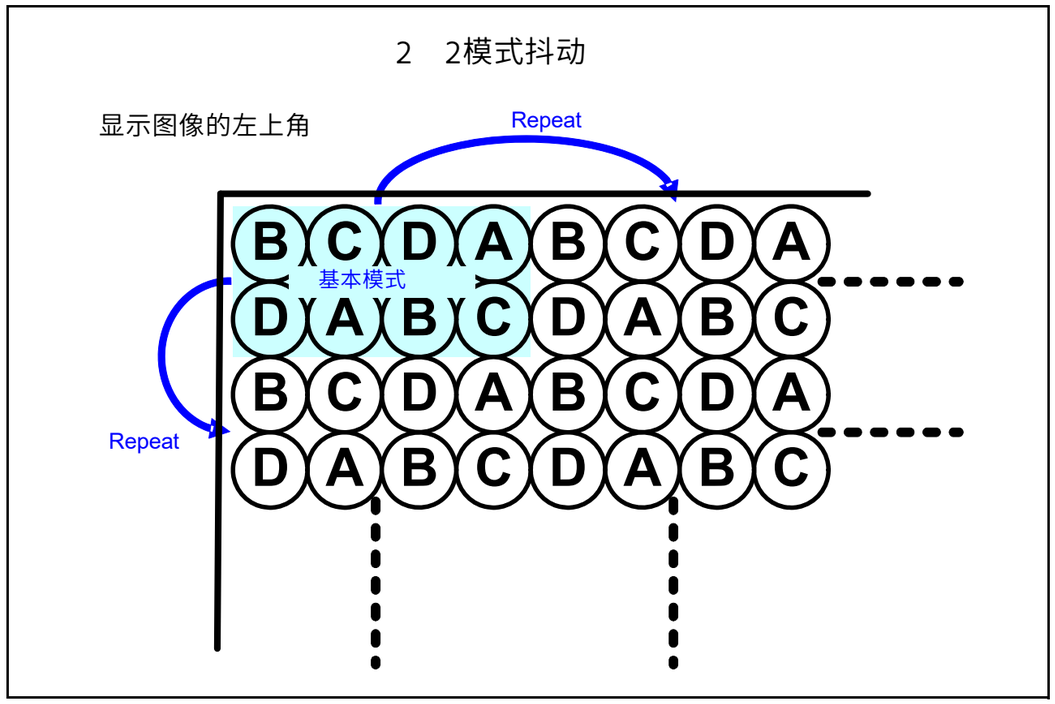
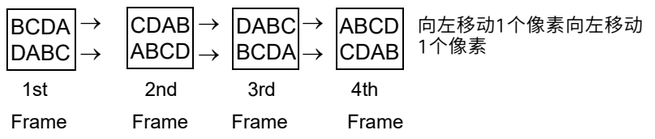


Figure 58.14 2×2图案抖动的加值选择方法

如下重复基本模式。四帧构成1个周期。



- A：OUT_PDTHA.PA[1:0]位值按照输出格式移位后得到的值
- B：OUT_PDTHA.PB[1:0]位值按照输出格式移位后得到的值
- C：OUT_PDTHA.PC[1:0]位值按照输出格式移位后得到的值
- D：OUT_PDTHA.PD[1:0]位值按照输出格式移位后得到的值

瑞萨推荐如下设置这些位：PA[1:0]=11b PB[1:0]=00b PC[1:0]=10b PD[1:0]=01b

当设置2×2图案抖动（OUT_PDTHA.SEL[1:0]=10b）时，背景平面的有效像素区域必须是基本图案的整数倍。如果选择串行RGB作为输出控制块的输出格式，则将水平有效像素宽度加2，并将结果值设置为背景平面水平有效像素宽度位(BG_HSIZE.HW[10:0])。

58.2.49 Output Control Block Output Phase Control Register (OUT_CLKPHASE)

Address(es): GLCDC.OUT_CLKPHASE 400E 13E4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	FRONTGAM	—	—	—	LCDEDGE	—	TCON0EDGE	TCON1EDGE	TCON2EDGE	TCON3EDGE	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b3	TCON3EDGE	LCD_TCON3 Output Phase Control	0: Synchronize output with rising edge of LCD_CLK 1: Synchronize output with falling edge of LCD_CLK.	R/W
b4	TCON2EDGE	LCD_TCON2 Output Phase Control	0: Synchronize output with rising edge of LCD_CLK 1: Synchronize output with falling edge of LCD_CLK.	R/W
b5	TCON1EDGE	LCD_TCON1 Output Phase Control	0: Synchronize output with rising edge of LCD_CLK 1: Synchronize output with falling edge of LCD_CLK.	R/W
b6	TCON0EDGE	LCD_TCON0 Output Phase Control	0: Synchronize output with rising edge of LCD_CLK 1: Synchronize output with falling edge of LCD_CLK.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b8	LCDEDGE	LCD_DATA Output Phase Control	0: Synchronize output with rising edge of LCD_CLK 1: Synchronize output with falling edge of LCD_CLK.	R/W
b11 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b12	FRONTGAM	Correction Control	0: Process brightness/contrast correction followed by gamma correction 1: Process gamma correction followed by brightness/contrast correction.	R/W
b31 to b13	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: This setting is reflected to the internal operations on assertion of the vertical synchronization signal (input) when OUT_VLATCH.VEN = 1 or when the register value reflection control signal to internal operations for all the modules is asserted.

TCON3EDGE bit (LCD_TCON3 Output Phase Control)

The TCON3EDGE bit controls the output phase of LCD_TCON3. When this bit is set to 1, LCD_TCON3 is output in synchronization with the falling edge of LCD_CLK, and when it is cleared to 0, LCD_TCON3 is output in synchronization with the rising edge.

TCON2EDGE bit (LCD_TCON2 Output Phase Control)

The TCON2EDGE bit controls the output phase of LCD_TCON2. When this bit is set to 1, LCD_TCON2 is output in synchronization with the falling edge of LCD_CLK, and when it is cleared to 0, LCD_TCON2 is output in synchronization with the rising edge.

TCON1EDGE bit (LCD_TCON1 Output Phase Control)

The TCON1EDGE bit controls the output phase of LCD_TCON1. When this bit is set to 1, LCD_TCON1 is output in synchronization with the falling edge of LCD_CLK, and when it is cleared to 0, LCD_TCON1 is output in synchronization with the rising edge.

TCON0EDGE bit (LCD_TCON0 Output Phase Control)

The TCON0EDGE bit controls the output phase of LCD_TCON0. When this bit is set to 1, LCD_ TCON0 is output in synchronization with the falling edge of LCD_CLK, and when it is cleared to 0, LCD_TCON0 is output in

58.2.49 输出控制模块输出相位控制寄存器(OUT_CLKPHASE)

Address(es): GLCDC.OUT_CLKPHASE 400E 13E4h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	前游戏	—	—	—	LCDEDGE	—	TCON0EDGE	TCON1EDGE	TCON2EDGE	TCON3EDGE	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b2 to b0	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b3	TCON3EDGE	LCD_TCON3输出相位 Control	0：与LCD_CLK的上升沿同步输出1：与LCD_CLK的下降沿同步输出。	R/W
b4	TCON2EDGE	LCD_TCON2输出相位 Control	0：与LCD_CLK的上升沿同步输出1：与LCD_CLK的下降沿同步输出。	R/W
b5	TCON1EDGE	LCD_TCON1输出相位 Control	0：与LCD_CLK的上升沿同步输出1：与LCD_CLK的下降沿同步输出。	R/W
b6	TCON0EDGE	LCD_TCON0输出相位 Control	0：与LCD_CLK的上升沿同步输出1：与LCD_CLK的下降沿同步输出。	R/W
b7	—	Reserved	该位读取为0。写入值应为0。	R/W
b8	LCDEDGE	LCD_DATA输出相位 Control	0：与LCD_CLK的上升沿同步输出1：与LCD_CLK的下降沿同步输出。	R/W
b11 to b9	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b12	FRONTGAM	校正控制	0：处理亮度对比度校正，然后进行伽马校正1：处理伽马校正，然后进行亮度对比度校正。	R/W
b31 to b13	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note: 此设置反映到垂直同步信号（输入）断言的内部操作时
OUT_VLATCH.VEN=1或当所有模块的内部操作的寄存器值反射控制信号被断言时。

TCON3EDGE位（LCD_TCON3输出相位控制）

TCON3EDGE位控制LCD_TCON3的输出相位。该位置1时，LCD_TCON3与LCD_CLK的下降沿同步输出，清0时，LCD_TCON3与上升沿同步输出。

TCON2EDGE位（LCD_TCON2输出相位控制）

TCON2EDGE位控制LCD_TCON2的输出相位。该位设置为1时，LCD_TCON2与LCD_CLK的下降沿同步输出，清为0时，LCD_TCON2与上升沿同步输出。

TCON1EDGE位（LCD_TCON1输出相位控制）

TCON1EDGE位控制LCD_TCON1的输出相位。当该位设置为1时，LCD_TCON1与LCD_CLK的下降沿同步输出，当清零时，LCD_TCON1与上升沿同步输出。

TCON0EDGE位（LCD_TCON0输出相位控制）

TCON0EDGE位控制LCD_TCON0的输出相位。该位置1时，LCD_TCON0与LCD_CLK下降沿同步输出，清0时，LCD_TCON0输出

synchronization with the rising edge.

LCDEDGE bit (LCD_DATA Output Phase Control)

The LCDEDGE bit controls the output phase of the LCD_DATA pins (LCD_DATA23 to LCD_DATA00). When this bit is set to 1, the LCD_DATA pins are output in synchronization with the falling edge of LCD_CLK, and when it is cleared to 0, the LCD_DATA pins are output in synchronization with the rising edge.

FRONTGAM bit (Correction Control)

The FRONTGAM bit controls the correction sequence. When this bit is set to 1, gamma correction is followed by brightness and contrast correction, and when it is cleared to 0, gamma correction follows brightness and contrast correction. In both cases, each RGB data output from the graphics 2 module is extended from 8 bits to 10 bits (with 00b appended to the lower side), and is input to the preceding stage of the correction circuit. The output is rounded to 10 bits and is input to the dither correction circuit. Although the sequence of RGB gamma correction and brightness/contrast correction can be reversed using this bit, brightness correction always precedes contrast correction.

58.2.50 TCON Reference Timing Setting Register (TCON_TIM)

Address(es): GLCDC.TCON_TIM 400E 1404h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	HALF[10:0]										
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	OFFSET[10:0]										
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b10 to b0	OFFSET[10:0]	Horizontal Synchronization Signal Generation Reference Timing	Offset from the assertion of the internal horizontal synchronization signal in pixels. 000h: 1 pixel : 3FFh: 1024 pixels. Other settings are prohibited.	R/W
b15 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b26 to b16	HALF[10:0]	Vertical Synchronization Signal Generation Change Timing	Delay from the assertion of the internal horizontal synchronization signal in pixels. 000h: 1 pixel (no delay) : 3FFh: 1024 pixels. Other settings are prohibited.	R/W
b31 to b27	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Rewriting these bits is prohibited during operation. Set the required settings before enabling operation. Operation is not guaranteed if the bit is rewritten during operation.

OFFSET[10:0] bits (Horizontal Synchronization Signal Generation Reference Timing)

The OFFSET[10:0] bits specify the reference timing to be used when the horizontal synchronization signal is generated in the TCON. Set the offset from the assertion of the internal horizontal synchronization signal (HS) in terms of pixels. Figure 58.15 shows the horizontal synchronization signal generation reference timing in the TCON.

与上升沿同步。

LCDEDGE位（LCD_DATA输出相位控制）

LCDEDGE位控制LCD_DATA引脚（LCD_DATA23至LCD_DATA00）的输出相位。当该位设置为1时，LCD_DATA引脚与LCD_CLK的下降沿同步输出，当它清为0时，LCD_DATA引脚与上升沿同步输出。

FRONTGAM位（校正控制）

FRONTGAM位控制校正序列。当该位设置为1时，伽马校正跟随亮度和对比度校正，当它清零时，伽马校正跟随亮度和对比度校正。在这两种情况下，图形2模块输出的每个RGB数据都从8位扩展到10位（下侧附加00b），并输入到校正电路的前级。输出四舍五入到10位并输入到抖动校正电路。尽管使用该位可以颠倒RGB伽马校正和亮度对比度校正的顺序，但亮度校正总是先于对比度校正。

58.2.50 TCON参考时序设置寄存器(TCON_TIM)

Address(es): GLCDC.TCON_TIM 400E 1404h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	HALF[10:0]										
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	OFFSET[10:0]										
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b10 to b0	OFFSET[10:0]	水平同步信号 生成参考时序	与内部水平同步信号断言的偏移量（以像素为单位）。000h：1像素 :3FFh:1024像素。禁止其他设置。	R/W
b15 to b11	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b26 to b16	HALF[10:0]	垂直同步信号 代换时间	内部水平同步信号的断言延迟（以像素为单位）。000h：1像素（无延迟） :3FFh:1024像素。禁止其他设置。	R/W
b31 to b27	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note: 操作期间禁止改写这些位。在启用操作之前设置所需的设置。如果在操作期间重写该位，则无法保证操作。

OFFSET[10:0]位（水平同步信号生成参考时序）

OFFSET[10:0]位指定在TCON中生成水平同步信号时要使用的参考时序。以像素为单位设置内部水平同步信号(HS)断言的偏移量。图58.15显示了TCON中的水平同步信号生成参考时序。

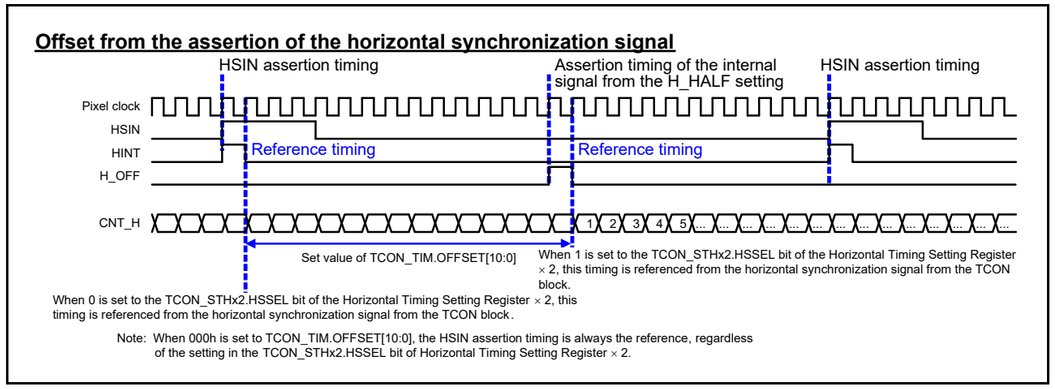


Figure 58.15 Reference timing in the TCON for horizontal synchronization signal generation

HALF[10:0] bits (Vertical Synchronization Signal Generation Change Timing)

The HALF[10:0] bits specify the vertical synchronization signal change timing when the signal is generated in the TCON. Set the change timing as a delay from the assertion of the internal horizontal synchronization signal (HS) in terms of pixels. Figure 58.16 shows the vertical synchronization signal change timing in the TCON.

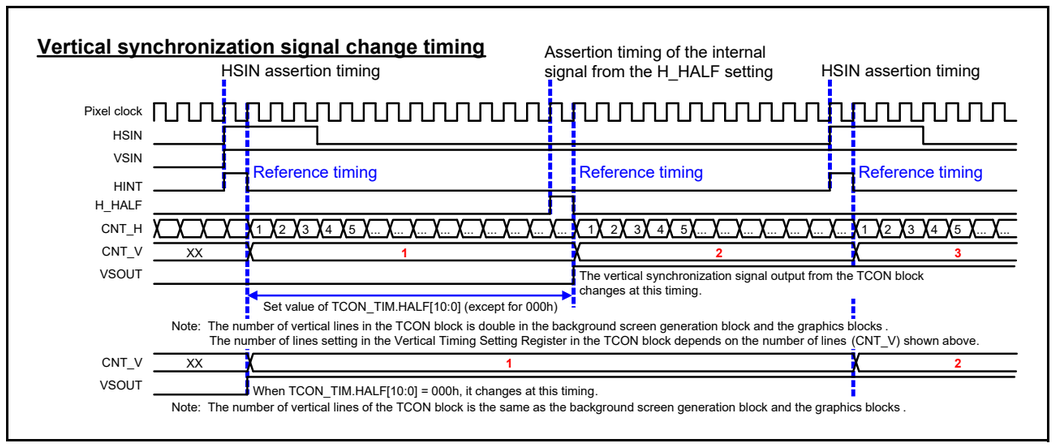


Figure 58.16 Timing in the TCON for vertical synchronization signal change

It is possible to change the vertical synchronization signal at any time within a horizontal line by setting this bit to the appropriate value.

Also, Figure 58.17 shows the relationship between the TCON block and the output format block in the output control block. These blocks are based on shared control signals (same timing) and image data, and the internal delay is the same. The delay difference specified in the register settings is the source of the timing differences on the external pins.

- TCON block: 3 cycles delay of the pixel clock (PXCLK)
- Data Format Block:
  - Parallel RGB: 3 cycles delay of the pixel clock (PXCLK)
  - Serial RGB: 3 cycles delay of the pixel clock (PXCLK)
    - The delay of the pixel head data including invalid data
    - No delay of the serial RGB data.

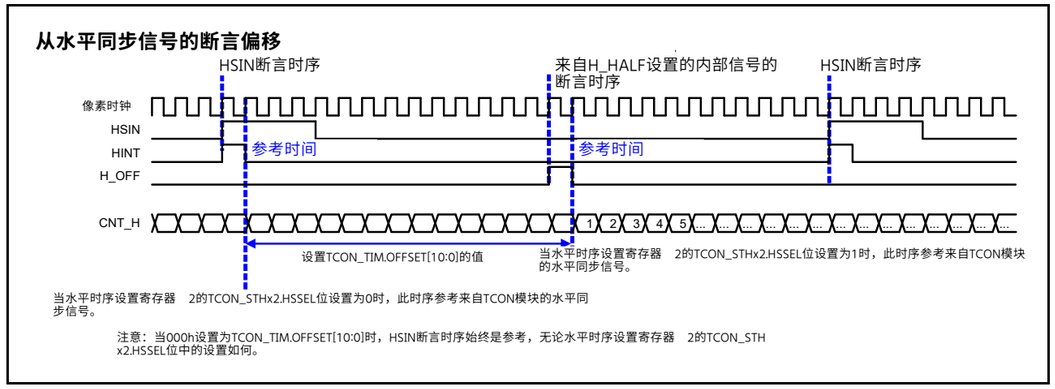


Figure 58.15 TCON中用于水平同步信号生成的参考时序

HALF[10:0]位（垂直同步信号发生变化时序）

HALF[10:0]位指定当信号在
TCON。以像素为单位，将更改时序设置为内部水平同步信号(HS)断言的延迟。图58.16显示了TCON中的垂直同步信号变化时序。

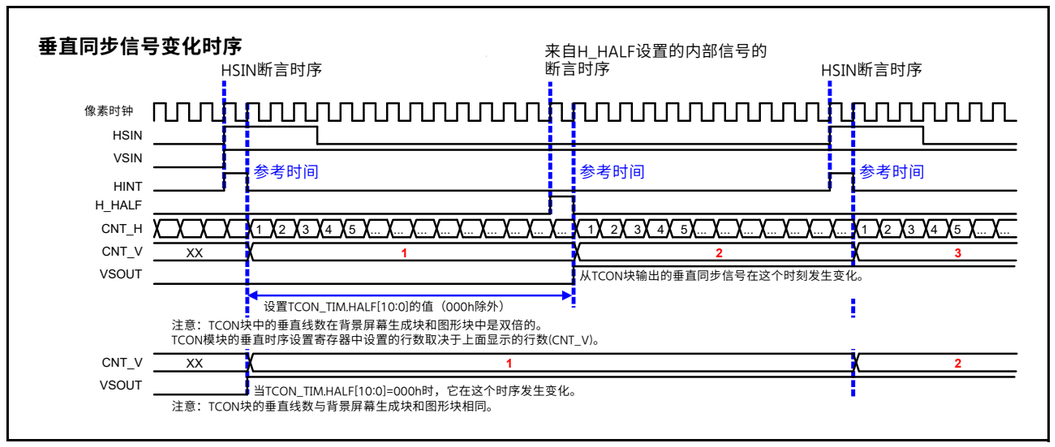


Figure 58.16 TCON中用于垂直同步信号变化的时序

通过将此位设置为适当的值，可以随时在水平行内更改垂直同步信号。

此外，图58.17显示了TCON块和输出控制块中的输出格式块之间的关系。这些块基于共享的控制信号（相同的时序）和图像数据，内部延迟相同。寄存器设置中指定的延迟差异是外部引脚上的时序差异的来源。

- TCON块：像素时钟(PXCLK)的3个周期延迟
- 数据格式块：
  - 并行RGB：像素时钟(PXCLK)的3个周期延迟
  - 串行RGB：像素时钟(PXCLK)的3个周期延迟

    包含无效数据的像素头数据延迟

    串行RGB数据无延迟。

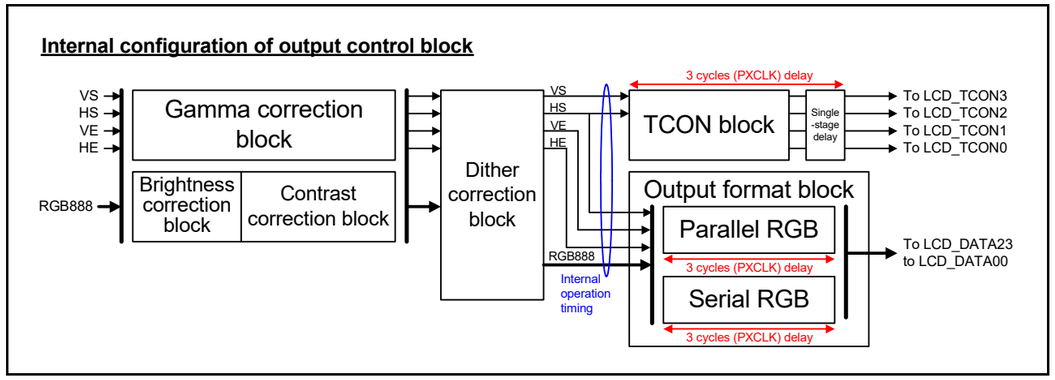


Figure 58.17 Internal configuration of output control block

58.2.51 TCON Vertical Timing Setting Register A1 (TCON_STVA1) TCON Vertical Timing Setting Register B1 (TCON_STVB1)

Address(es): GLCDC.TCON_STVA1 400E 1408h, GLCDC.TCON_STVB1 400E 1410h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	VS[10:0]										
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	VW[10:0]										
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b10 to b0	VW[10:0]	Vertical Synchronization Signal STVx1 Second Change Timing	Signal assertion width in lines. 000h: 0 line (no vertical synchronization signal assertion) : 7FFh: 2047 lines.	R/W
b15 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b26 to b16	VS[10:0]	Vertical Synchronization Signal STVx1 First Change Timing	Signal delay in lines. 000h: 0 line (no delay) : 7FFh: 2047 lines.	R/W
b31 to b27	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Rewriting these bits is prohibited during operation. Set the required settings before enabling operation. Operation is not guaranteed if the bit is rewritten during operation.

The vertical timing setting registers (TCON_STVA1/TCON_STVB1 and TCON_STVA2/TCON_STVB2) have the same configuration, and x is either A or B in the descriptions.

VW[10:0] bits (Vertical Synchronization Signal STVx1 Second Change Timing)

The VW[10:0] bits specify the second change (negation) timing of the vertical synchronization signal STVx1, which is generated in the TCON. Set the second change timing as a delay from the first change point in terms of lines. The change position in a horizontal line is defined in TCON_TIM.HALF[10:0] in the Reference Timing Setting Register (TCON_TIM), as is the first change timing.

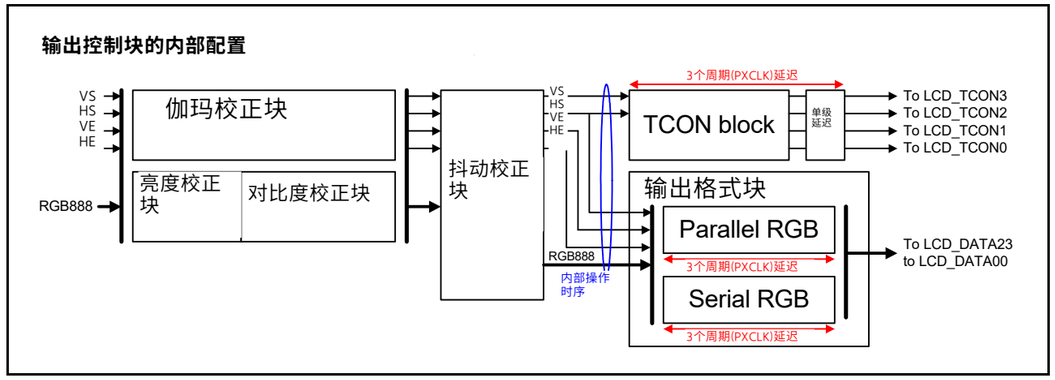


Figure 58.17 输出控制块的内部配置

58.2.51 TCON垂直时序设置寄存器A1(TCON_STVA1)TCON垂直时序设置寄存器B1(TCON_STVB1)

Address(es): GLCDC.TCON_STVA1 400E 1408h, GLCDC.TCON_STVB1 400E 1410h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	VS[10:0]										
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	VW[10:0]										
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b10 to b0	VW[10:0]	垂直同步信号STVx1秒变化时序	以行为单位的信号断言宽度。000h：0行（无垂直同步信号断言） : 7FFh: 2047 lines.	R/W
b15 to b11	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b26 to b16	VS[10:0]	垂直同步信号 STVx1首次更改时间	线路中的信号延迟。0 00h：0线（无延迟） : 7FFh: 2047 lines.	R/W
b31 to b27	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note: 操作期间禁止改写这些位。在启用操作之前设置所需的设置。如果在操作期间重写该位，则无法保证操作。

垂直时序设置寄存器（TCON_STVA1TCON_STVB1和TCON_STVA2TCON_STVB2）具有相同的配置，在说明中x为A或B。

VW[10:0]位（垂直同步信号STVx1秒变化时序）

VW[10:0]位指定在TCON中生成的垂直同步信号STVx1的第二次改变（否定）时序。将第二个更改时间设置为从第一个更改点以线为单位的延迟。水平线的变化位置在参考时序设置寄存器(TCON_TIM)的TCON_TIM.HALF[10:0]中定义，第一个变化时序也是如此。

VS[10:0] bits (Vertical Synchronization Signal STVx1 First Change Timing)

The VS[10:0] bits specify the first change (assertion) timing of the vertical synchronization signal STVx1, which is generated in the TCON. Set the change timing as a delay from the input vertical synchronization signal (VSIN) in terms of lines. The change position in a horizontal line is defined in TCON_TIM.HALF[10:0] in the Reference Timing Setting Register (TCON_TIM), as is the first change timing.

Figure 58.18 shows the change timing of vertical synchronization signal to be generated.

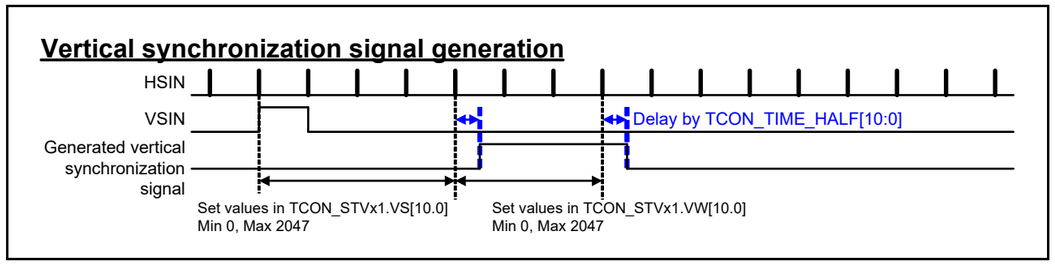


Figure 58.18 Generation of vertical synchronization signal

58.2.52 TCON Vertical Timing Setting Register A2 (TCON_STVA2) TCON Vertical Timing Setting Register B2 (TCON_STVB2)

Address(es): GLCDC.TCON_STVA2 400E 140Ch, GLCDC.TCON_STVB2 400E 1414h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	INV	—	SEL[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	SEL[2:0]	Output Signal Select Control for VSOUT/VEOUT Pin	Output signal select for LCD_TCON0 pin (controlled in TCON_STVA2 register) and LCD_TCON1 pin (controlled in TCON_STVB2 register). b2 b0 0 0 0: STVA 0 0 1: STVB 0 1 0: STHA 0 1 1: STHB 1 0 0: Setting prohibited 1 0 1: Setting prohibited 1 1 0: Setting prohibited 1 1 1: DE.	R/W
b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	INV	Vertical Synchronization Signal STVx Polarity Inversion Control	0: Do not invert 1: Invert.	R/W
b31 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Rewriting these bits is prohibited during operation. Set the required settings before enabling operation. Operation is not guaranteed if the bit is rewritten during operation.

The vertical timing setting registers (TCON_STVA1/TCON_STVB1 and TCON_STVA2/TCON_STVB2) have the same configuration, and x is either A or B in the descriptions.

VS[10:0]位（垂直同步信号STVx1首次变化时序）

VS[10:0]位指定在TCON中生成的垂直同步信号STVx1的第一个变化（断言）时序。将变化时序设置为从输入垂直同步信号(VSIN)到线的延迟。水平线的变化位置在参考时序设置寄存器(TCON_TIM)的TCON_TIM.HALF[10:0]中定义，第一个变化时序也是如此。

图58.18显示了要生成的垂直同步信号的变化时序。

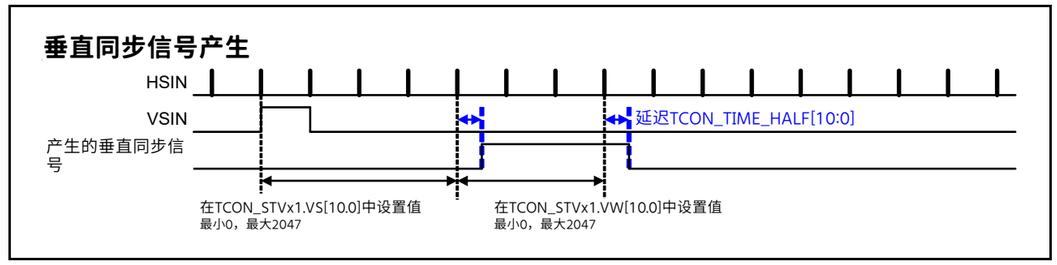


Figure 58.18 垂直同步信号的产生

58.2.52 TCON垂直时序设置寄存器A2(TCON_STVA2)TCON垂直时序设置寄存器B2(TCON_STVB2)

Address(es): GLCDC.TCON_STVA2 400E 140Ch, GLCDC.TCON_STVB2 400E 1414h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	INV	—	SEL[2:0]		
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b2 to b0	SEL[2:0]	输出信号选择控制 VSOUT/VEOUT Pin	LCD_TCON0引脚的输出信号选择（控制在TCON_STVA2寄存器）和LCD_TCON1引脚（在TCON_STVB2寄存器中控制）。b2b0000：STVA001：STVB010：STHA011：STHB100：禁止设置101：禁止设置110：禁止设置111：DE。	R/W
b3	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b4	INV	垂直同步信号STVx 极性反转控制	0：不反转1： 反转。	R/W
b31 to b5	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note: 操作期间禁止改写这些位。在启用操作之前设置所需的设置。如果在操作期间重写该位，则无法保证操作。

垂直时序设置寄存器（TCON_STVA1TCON_STVB1和TCON_STVA2TCON_STVB2）具有相同的配置，在说明中x为A或B。

SEL[2:0] bits (Output Signal Select Control for VSOUT/VEOUT Pin)

The SEL[2:0] bits control output signal select for the LCD_TCON0/LCD_TCON1 pin. Figure 58.19 shows the configuration of the inversion control and output signal select.

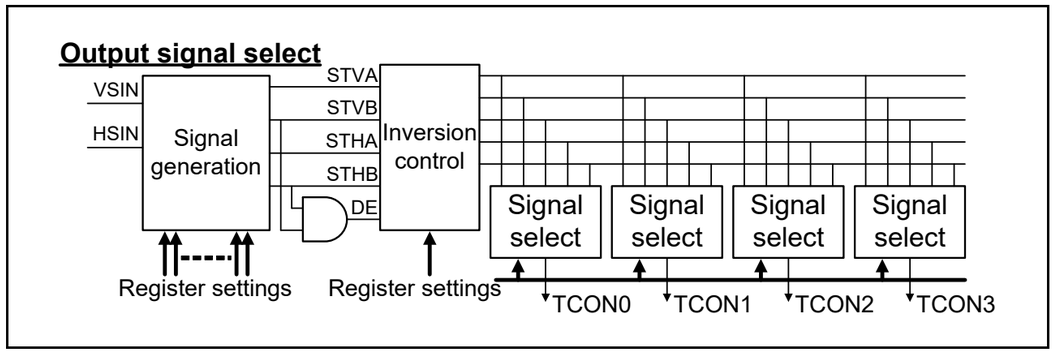


Figure 58.19 Configuration of inversion control and output signal selects

INV bit (Vertical Synchronization Signal STVx Polarity Inversion Control)

The INV bit controls polarity inversion of the vertical synchronization signal (STVx).

58.2.53 TCON Horizontal Timing Setting Register STHA1 (TCON_STHA1) TCON Horizontal Timing Setting Register STHB1 (TCON_STHB1)

Address(es): GLCDC.TCON_STHA1 400E 1418h, GLCDC.TCON_STHB1 400E 1420h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	HS[10:0]										
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	HW[10:0]										
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b10 to b0	HW[10:0]	Horizontal Synchronization Signal STHx1 Second Change Timing	Signal assertion width in pixels. 000h: 0 pixel (no horizontal synchronization signal assertion) : 3FFh: 1023 pixels. Other settings are prohibited.	R/W
b15 to b11	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b26 to b16	HS[10:0]	Horizontal Synchronization Signal STHx1 First Change Timing	Signal delay in pixels. 000h: 0 pixel (no delay) : 3FFh: 1023 pixels. Other settings are prohibited.	R/W
b31 to b27	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Rewriting these bits is prohibited during operation. Set the required settings before enabling operation. Operation is not guaranteed if the bit is rewritten during operation.

The horizontal timing setting registers (TCON_STHA1/TCON_STHB1 and TCON_STHA2/TCON_STHB2) have the same configuration, and x is either A or B in the descriptions.

SEL[2:0]位（VSOUTVEOUT引脚的输出信号选择控制）

SEL[2:0]位控制LCD_TCON0LCD_TCON1引脚的输出信号选择。图58.19显示了反转控制和输出信号选择的配置。

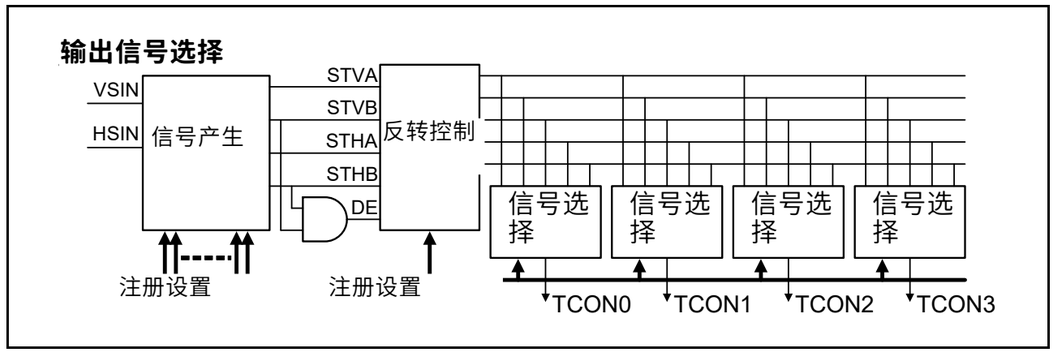


Figure 58.19 逆变控制配置和输出信号选择

INV位（垂直同步信号STVx极性反转控制）

INV位控制垂直同步信号(STVx)的极性反转。

58.2.53 TCON水平时序设置寄存器STHA1(TCON_STHA1)TCON水平时序设置寄存器STHB1(TCON_STHB1)

Address(es): GLCDC.TCON_STHA1 400E 1418h, GLCDC.TCON_STHB1 400E 1420h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	HS[10:0]										
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	HW[10:0]										
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b10 to b0	HW[10:0]	水平同步信号 STHx1秒变化时间	信号断言宽度（以像素为单位）。000h：0像素（无水平同步信号断言） :3FFh:1023像素。禁止其他设置。	R/W
b15 to b11	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b26 to b16	HS[10:0]	水平同步信号 STHx1首次更改时序	以像素为单位的信号延迟。000h：0像素（无延迟） :3FFh:1023像素。禁止其他设置。	R/W
b31 to b27	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note: 操作期间禁止改写这些位。在启用操作之前设置所需的设置。如果在操作期间重写该位，则无法保证操作。

水平时序设置寄存器（TCON_STHA1TCON_STHB1和TCON_STHA2TCON_STHB2）具有相同的配置，在说明中x为A或B。

HW[10:0] bits (Horizontal Synchronization Signal STHx1 Second Change Timing)

The HW[10:0] bits specify the second change (negation) timing of the horizontal synchronization signal STHx1, which is generated in the TCON. Set the second change timing as a distance from the first change point in terms of pixels.

HS[10:0] bits (Horizontal Synchronization Signal STHx1 First Change Timing)

The HS[10:0] bits specify the first change (assertion) timing of the horizontal synchronization signal STHx1, which is generated in the TCON. Set the change timing as a distance from the input horizontal synchronization signal (HSIN) or the reference timing based on the offset specified in the TCON_TIM.OFFSET[10:0] bit (horizontal synchronization signal generation reference timing) in terms of pixels.

Figure 58.20 shows the horizontal synchronization signal generation timing if the input horizontal synchronization signal (HSIN) is based on the negated edge reference of the HINT signal. Figure 58.21 shows the horizontal synchronization signal generation timing after offset. By setting the TCON_TIM.OFFSET[10:0] bit (horizontal synchronization generation reference timing) and these horizontal synchronization bits appropriately, it is possible to generate a signal that is asserted before HSIN and negated after HSIN, where HSIN is the horizontal synchronization signal input to the TCON.

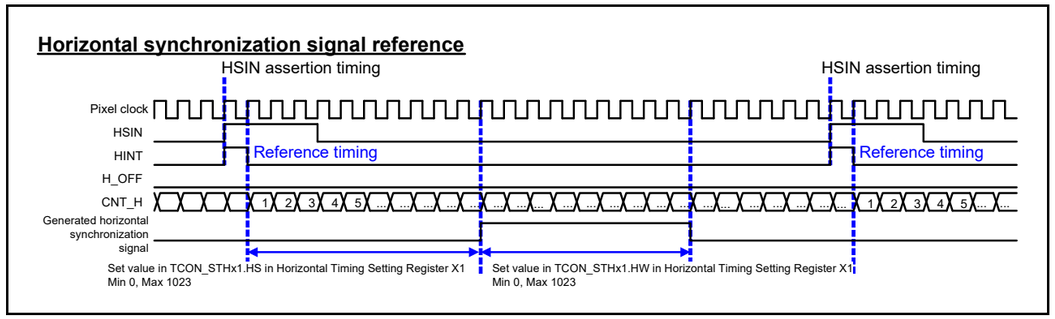


Figure 58.20 Signal generation based on input horizontal synchronization signal (HSIN)

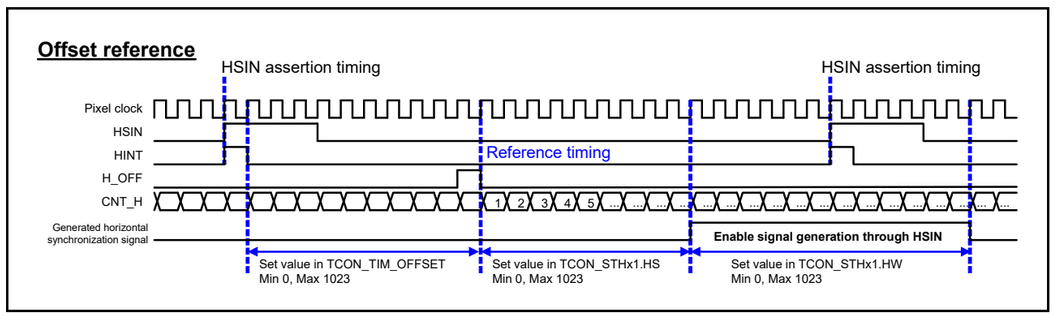


Figure 58.21 Horizontal synchronization signal generation based on offset

When generating the signal across HSIN on the offset reference, the horizontal synchronization signal of the last line of the frame spans the first line of the next frame. Even if the BG_EN.EN bit is cleared to 0 and the GLCDC operation is stopped, the horizontal synchronization signal across HSIN is not cleared at the frame end and retains the predetermined value until the second change timing set in the registers. If BG_EN.SWRST is cleared to 0, the signal returns to the initial state immediately.

HW[10:0]位（水平同步信号STHx1秒变化时序）

HW[10:0]位指定在TCON中生成的水平同步信号STHx1的第二次变化（否定）时序。以像素为单位将第二个变化时间设置为与第一个变化点的距离。

HS[10:0]位（水平同步信号STHx1首次变化时序）

HS[10:0]位指定在TCON中生成的水平同步信号STHx1的第一个变化（断言）时序。根据TCON_TIM.OFFSET[10:0]位（水平同步信号生成参考定时）以像素为单位指定的偏移量，将更改定时设置为距输入水平同步信号(HSIN)或参考定时的距离。

图58.20显示了如果输入水平同步信号(HSIN)基于HINT信号的取反边沿参考，则水平同步信号生成时序。图58.21显示了偏移后的水平同步信号生成时序。通过适当地设置TCON_TIM.OFFSET[10:0]位（水平同步生成参考时序）和这些水平同步位，可以生成一个在HSIN之前断言并在HSIN之后取反的信号，其中HSIN是水平同步信号输入到TCON。

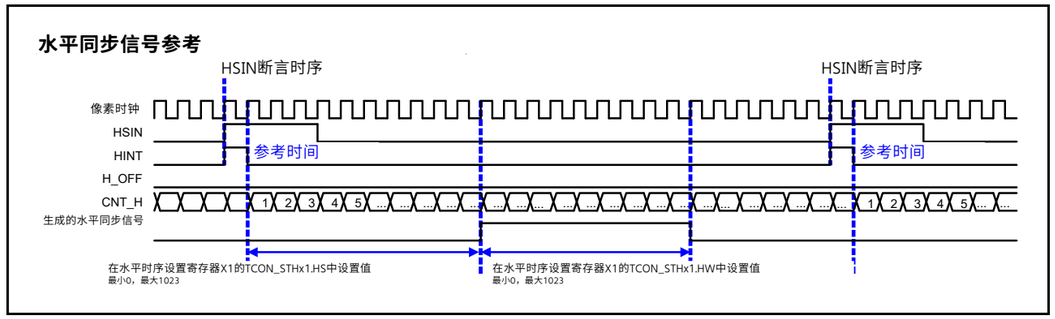


Figure 58.20 基于输入水平同步信号(HSIN)的信号生成

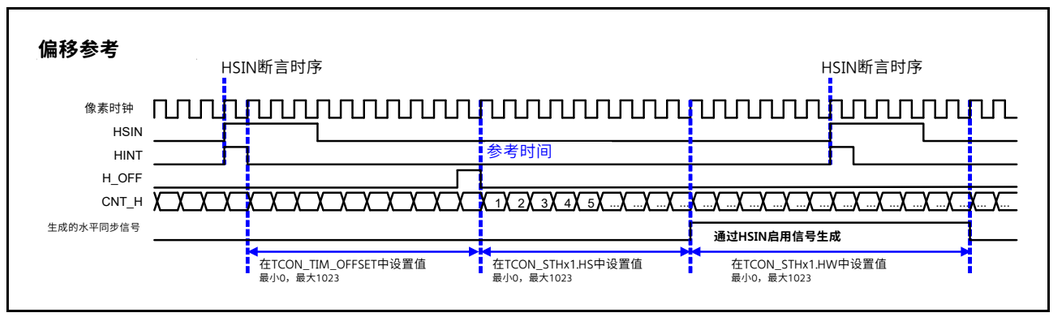


Figure 58.21 基于偏移的水平同步信号生成

当在偏移参考上生成跨HSIN的信号时，帧最后一行的水平同步信号跨越下一帧的第一行。即使BG_EN.EN位清0并停止GLCDC操作，HSIN两端的水平同步信号在帧结束时也不会被清除，并保持预定值直到寄存器中设置的第二次更改时序。如果BG_EN.SWRST清零，信号立即返回初始状态。

58.2.54 TCON Horizontal Timing Setting Register STHA2 (TCON_STHA2) TCON Horizontal Timing Setting Register STHB2 (TCON_STHB2)

Address(es): GLCDC.TCON_STHA2 400E 141Ch, GLCDC.TCON_STHB2 400E 1424h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	HSSEL	—	—	—	INV	—	SEL[2:0]		
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b2 to b0	SEL[2:0]	Output Signal Select Control for LCD_TCON2/LCD_TCON3 Pin	Output signal select for LCD_TCON2 pin (controlled in TCON_STHA2 register) and LCD_TCON3 pin (controlled in TCON_STHB2 register). b2 b0 0 0 0: STVA 0 0 1: STVB 0 1 0: STHA 0 1 1: STHB 1 0 0: Setting prohibited 1 0 1: Setting prohibited 1 1 0: Setting prohibited 1 1 1: DE.	R/W
b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b4	INV	Horizontal Synchronization Signal STHx Polarity Inversion Control	0: Do not invert 1: Invert.	R/W
b7 to b5	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b8	HSSEL	Horizontal Synchronization Signal STHx Reference Timing Control	0: Select input horizontal synchronization signal (HSIN) as reference for signal generation 1: Select offset specified in TCON_TIM.OFFSET[10:0] (horizontal synchronization generation reference timing) as reference for signal generation.	R/W
b31 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Rewriting these bits is prohibited during operation. Set the required settings before enabling operation. Operation is not guaranteed if the bit is rewritten during operation.

The horizontal timing setting registers (TCON_STHA1/TCON_STHB1 and TCON_STHA2/TCON_STHB2) have the same configuration, and x is either A or B in the descriptions.

SEL[2:0] bits (Output Signal Select Control for LCD_TCON2/LCD_TCON3 Pin)

The SEL[2:0] bits control the output signal select for the LCD_TCON2/LCD_TCON3 pins.

INV bit (Horizontal Synchronization Signal STHx Polarity Inversion Control)

The INV bit controls polarity inversion of the horizontal synchronization signal (STHx).

HSSEL bit (Horizontal Synchronization Signal STHx Reference Timing Control)

The HSSEL bit selects the reference timing for generating the horizontal synchronization signal STHx. For details on the signal to be generated, see Figure 58.20 and Figure 58.21. For the configuration of the inversion control and output signal select, see Figure 58.19.

58.2.54 TCON水平时序设置寄存器STHA2(TCON_STHA2)TCON水平时序设置寄存器STHB2(TCON_STHB2)

Address(es): GLCDC.TCON_STHA2 400E 141Ch, GLCDC.TCON_STHB2 400E 1424h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	HSSEL	—	—	—	INV	—	SEL[2:0]		
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b2 to b0	SEL[2:0]	LCD_TCON2LCD_TCON3引脚的输出信号选择控制	LCD_TCON2引脚的输出信号选择（控制在TCON_STHA2寄存器）和LCD_TCON3引脚（控制在TCON_STHB2寄存器）。 b2b0000：STVA001：STVB010：STHA011：STHB100：禁止设置101：禁止设置110：禁止设置111：DE。	R/W
b3	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b4	INV	水平同步信号STHx极性反转控制	0：不反转1：反转。	R/W
b7 to b5	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b8	HSSEL	水平同步信号STHx参考时序控制	0：选择输入水平同步信号(HSIN)作为信号生成的参考1：选择TCON_TIM.OFFSET[10:0]中指定的偏移 （水平同步生成参考定时）作为信号生成的参考。	R/W
b31 to b9	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note: 操作期间禁止改写这些位。在启用操作之前设置所需的设置。如果在操作期间重写该位，则无法保证操作。

水平时序设置寄存器（TCON_STHA1TCON_STHB1和TCON_STHA2TCON_STHB2）具有相同的配置，在说明中x为A或B。

SEL[2:0]位（LCD_TCON2LCD_TCON3引脚的输出信号选择控制）

SEL[2:0]位控制LCD_TCON2LCD_TCON3引脚的输出信号选择。

INV位（水平同步信号STHx极性反转控制）

INV位控制水平同步信号(STHx)的极性反转。

HSSEL位（水平同步信号STHx参考时序控制）

HSSEL位选择用于生成水平同步信号STHx的参考时序。关于要生成的信号的详细信息，请参见图58.20和图58.21。反转控制和输出信号选择的配置见图58.19。

58.2.55 TCON Data Enable Polarity Setting Register (TCON_DE)

Address(es): GLCDC.TCON_DE 400E 1428h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	INV
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	INV	Data Enable Signal DE Polarity Inversion Control	0: Do not invert 1: Invert.	R/W
b31 to b1	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note: Rewriting these bits is prohibited during operation. Set the required settings before enabling operation. Operation is not guaranteed if the bit is rewritten during operation.

INV bit (Data Enable Signal DE Polarity Inversion Control)

The INV bit controls polarity inversion of the data enable signal DE. The data enable signal DE generated in the TCON is the logical AND of the STVB and STHB signals.

58.2.56 System Control Block State Detection Control Register (SYSCNT_DTCTEN)

Address(es): GLCDC.SYSCNT_DTCTEN 400E 1440h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	L2UNDFDTC	L1UNDFDTC	VPOSDTC
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	VPOSDTC	Specified Line Detection Control	0: Disable detection of specified line 1: Enable detection of specified line*1.	R/W
b1	L1UNDFDTC	Graphics 1 Underflow Detection Control	0: Disable detection of graphics 1 underflow 1: Enable detection of graphics 1 underflow*2.	R/W
b2	L2UNDFDTC	Graphics 2 Underflow Detection Control	0: Disable detection of graphics 2 underflow 1: Enable detection of graphics 2 underflow*2.	R/W
b31 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. Set the VPOSDTC bit to 1 after setting the BG_EN.EN bit to 1.

Note 2. When setting the LnUNDFDTC (n = 1, 2) bit to 1 and when the BG_SYNC.VP[3:0] bits are set to a value greater than 5h, an unexpected GLCDC_LnUNDF (n = 1, 2) interrupt is generated after the GLCDC starts.Therefore, set the SYSCNT_STCLR.LnUNDFCLR (n = 1, 2) bit to 1, then set the SYSCNT_STMON.LnUNDF (n = 1, 2) bit to 0 to clear the unexpected GLCDC_LnUNDF (n = 1, 2) interrupt.

58.2.55 TCON数据使能极性设置寄存器(TCON_DE)

Address(es): GLCDC.TCON_DE 400E 1428h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	INV
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	INV	数据使能信号DE极性反转控制	0：不反转1：反转。	R/W
b31 to b1	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note: 操作期间禁止改写这些位。在启用操作之前设置所需的设置。如果在操作期间重写该位，则无法保证操作。

INV位（数据使能信号DE极性反转控制）

INV位控制数据使能信号DE的极性反转。TCON中产生的数据使能信号DE是STVB和STHB信号的逻辑与。

58.2.56 系统控制块状态检测控制寄存器(SYSCNT_DTCTEN)

Address(es): GLCDC.SYSCNT_DTCTEN 400E 1440h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	L2UNDFDTC	L1UNDFDTC	VPOSDTC
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	VPOSDTC	指定线路检测控制	0：禁止检测指定线路1：允许检测指定线路*1。	R/W
b1	L1UNDFDTC	图形1下溢检测Control	0：禁用检测图形1下溢1：启用检测图形1下溢*2。	R/W
b2	L2UNDFDTC	图形2下溢检测Control	0：禁用检测图形2下溢1：启用检测图形2下溢*2。	R/W
b31 to b3	—	Reserved	这些位被读取为0。写入值应为0。	R/W

注1.将BG_EN.EN位设置为1后，将VPOSDTC位设置为1。

注2.当将LnUNDFDTC(n=1 2)位设置为1并且将BG_SYNC.VP[3:0]位设置为大于5h的值时，会发生意外的GLCDC_LnUNDF(n=1 2)中断在GLCDC启动后生成。因此，将SYSCNT_STCLR.LnUNDFCLR(n=1 2)位设置为1，然后将SYSCNT_STMON.LnUNDF(n=1 2)位设置为0以清除意外的GLCDC_LnUNDF(n=1 2)中断。

VPOSDTC bit (Specified Line Detection Control)

The VPOSDTC bit enables or disables detection of the specified line. When this bit is set to 1, the associated bit in the SYSCNT_STMON register sets to 1 on event notification from graphics 2. When it is cleared to 0, the associated bit in the SYSCNT_STMON register does not set to 1 even on event notification from graphics 2.

L1UNDFDTC bit (Graphics 1 Underflow Detection Control)

The L1UNDFDTC bit enables or disables detection of the graphics 1 underflow. When this bit is set to 1, the associated bit in the SYSCNT_STMON register sets to 1 when an underflow occurs in graphics 1. When it is cleared to 0, the associated bit in the SYSCNT_STMON register does not set to 1 even when an underflow occurs in graphics 1. The underflow state in graphics 1 is automatically cleared on assertion of the vertical synchronization signal (VS) regardless of the value of this bit, and normal operation is recovered.

L2UNDFDTC bit (Graphics 2 Underflow Detection Control)

The L2UNDFDTC bit enables or disables detection of the graphics 2 underflow. When this bit is set to 1, the associated bit in the SYSCNT_STMON register sets to 1 when an underflow occurs in graphics 2. When it is cleared to 0, the associated bit in the SYSCNT_STMON register does not set to 1 even when an underflow occurs in graphics 2. The underflow state in graphics 2 is automatically cleared on assertion of the vertical synchronization signal (VS) regardless of the value of this bit, and normal operation is recovered.

58.2.57 System Control Block Interrupt Request Enable Control Register (SYSCNT_INTEN)

Address(es): GLCDC.SYSCNT_INTEN 400E 1444h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	L2UNDFINTEN	L1UNDFINTEN	VPOSINTEN
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	VPOSINTEN	Interrupt Request Signal GLCDC_VPOS Enable Control	0: Disable GLCDC_VPOS output 1: Enable GLCDC_VPOS output.	R/W
b1	L1UNDFINTEN	Interrupt Request Signal GLCDC_L1UNDF Enable Control	0: Disable GLCDC_L1UNDF output 1: Enable GLCDC_L1UNDF output.	R/W
b2	L2UNDFINTEN	Interrupt Request Signal GLCDC_L2UNDF Enable Control	0: Disable GLCDC_L2UNDF output 1: Enable GLCDC_L2UNDF output.	R/W
b31 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

VPOSINTEN bit (Interrupt Request Signal GLCDC_VPOS Enable Control)

The VPOSINTEN bit enables or disables the interrupt request signal GLCDC_VPOS. When this bit is set to 1, the interrupt request signal GLCDC_VPOS is asserted when the associated status monitor flag SYSCNT_STMON[0] sets. When it is cleared to 0, the interrupt request signal GLCDC_VPOS is not asserted even when the associated status monitor flag SYSCNT_STMON[0] sets. If this bit is cleared during GLCDC_VPOS assertion, the associated status monitor flag SYSCNT_STMON[0] does not change, but the interrupt request signal GLCDC_VPOS is negated.

L1UNDFINTEN bit (Interrupt Request Signal GLCDC_L1UNDF Enable Control)

The L1UNDFINTEN bit enables or disables the interrupt request signal GLCDC_L1UNDF. When this bit is set to 1, the interrupt request signal GLCDC_L1UNDF is asserted when the associated status monitor flag SYSCNT_STMON[1] sets. When it is cleared to 0, the interrupt request signal GLCDC_L1UNDF is not asserted even when the associated status monitor flag SYSCNT_STMON[1] sets. If this bit is cleared during GLCDC_L1UNDF assertion, the associated

VPOSDTC位（指定线路检测控制）

VPOSDTC位启用或禁用对指定线路的检测。当该位设置为1时，SYSCNT_STMON寄存器中的相关位在来自图形2的事件通知时设置为1。当它清零时，即使在来自图形的事件通知时，SYSCNT_STMON寄存器中的相关位也不会设置为12.

L1UNDFDTC位（图形1下溢检测控制）

L1UNDFDTC位启用或禁用图形1下溢检测。当该位设置为1时，当图形1中发生下溢时，SYSCNT_STMON寄存器中的相关位设置为1。当它清零时，即使发生下溢，SYSCNT_STMON寄存器中的相关位也不会设置为1在图形1中。图形1中的下溢状态在垂直同步信号(VS)置位时自动清除，无论该位的值如何，恢复正常操作。

L2UNDFDTC位（图形2下溢检测控制）

L2UNDFDTC位启用或禁用图形2下溢检测。当该位设置为1时，当图形2中发生下溢时，SYSCNT_STMON寄存器中的相关位设置为1。当它清零时，即使发生下溢，SYSCNT_STMON寄存器中的相关位也不会设置为1在图2中。图2中的下溢状态在垂直同步信号(VS)置位时自动清除，无论该位的值如何，恢复正常操作。

58.2.57 系统控制块中断请求使能控制寄存器(SYSCNT_INTEN)

Address(es): GLCDC.SYSCNT_INTEN 400E 1444h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	L2UNDFINTEN	L1UNDFINTEN	VPOSINTEN
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	VPOSINTEN	中断请求信号 GLCDC_VPOS启用控制	0：禁用GLCDC_VPOS输出1：启用GLCDC_VPOS输出。	R/W
b1	L1UNDFINTEN	中断请求信号 GLCDC_L1UNDF启用控制	0：禁用GLCDC_L1UNDF输出1：启用GLCDC_L1UNDF输出。	R/W
b2	L2UNDFINTEN	中断请求信号 GLCDC_L2UNDF启用控制	0：禁用GLCDC_L2UNDF输出1：启用GLCDC_L2UNDF输出。	R/W
b31 to b3	—	Reserved	这些位被读取为0。写入值应为0。	R/W

VPOSINTEN位（中断请求信号GLCDC_VPOS使能控制）

VPOSINTEN位启用或禁用中断请求信号GLCDC_VPOS。当该位设置为1时，在相关状态监控标志SYSCNT_STMON[0]设置时，中断请求信号GLCDC_VPOS被置位。当它被清除为0时，即使相关的状态监控标志SYSCNT_STMON[0]设置，中断请求信号GLCDC_VPOS也不会被断言。如果在GLCDC_VPOS断言期间该位被清除，则相关的状态监控标志SYSCNT_STMON[0]不会改变，但中断请求信号GLCDC_VPOS被否定。

L1UNDFINTEN位（中断请求信号GLCDC_L1UNDF使能控制）

L1UNDFINTEN位启用或禁用中断请求信号GLCDC_L1UNDF。当该位设置为1时，中断请求信号GLCDC_L1UNDF在相关状态监控标志SYSCNT_STMON[1]设置时被断言。当它被清除为0时，即使相关的状态监视标志SYSCNT_STMON[1]设置，中断请求信号GLCDC_L1UNDF也不会被断言。如果在GLCDC_L1UNDF断言期间清除该位，则相关的

status monitor flag SYSCNT_STMON[1] does not change, but the interrupt request signal GLCDC_L1UNDF is negated.

L2UNDFINTEN bit (Interrupt Request Signal GLCDC_L2UNDF Enable Control)

The L2UNDFINTEN bit enables or disables the interrupt request signal GLCDC_L2UNDF. When this bit is set to 1, the interrupt request signal GLCDC_L2UNDF is asserted when the associated status monitor flag SYSCNT_STMON[2] sets. When it is cleared to 0, the interrupt request signal GLCDC_L2UNDF is not asserted even when the associated status monitor flag SYSCNT_STMON[2] sets. If this bit is cleared during GLCDC_L2UNDF assertion, the associated status monitor flag SYSCNT_STMON[2] does not change, but the interrupt request signal GLCDC_L2UNDF is negated.

58.2.58 System Control Block Status Clear Register (SYSCNT_STCLR)

Address(es): GLCDC.SYSCNT_STCLR 400E 1448h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	L2UNDFCLR	L1UNDFCLR	VPOSCLR
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	VPOSCLR	Graphics 2 Specified Line Detection Flag Clear	0: No operation 1: Clear the graphics 2 specified line detection flag.	R/W*1
b1	L1UNDFCLR	Graphics 1 Underflow Detection Flag Clear	0: No operation 1: Clear the graphics 1 underflow detection flag.	R/W*1
b2	L2UNDFCLR	Graphics 2 Underflow Detection Flag Clear	0: No operation 1: Clears the graphics 2 underflow detection flag.	R/W*1
b31 to b3	—	Reserved	These bits are read as 0. The write value should be 0.	R/W

Note 1. These bits are read as 0.

VPOSCLR bit (Graphics 2 Specified Line Detection Flag Clear)

Writing 1 to the VPOSCLR bit clears the graphics 2 specified line detection flag. Clearance of the flag by this bit is only valid for the associated flag, and does not directly affect the other states and interrupt request signals. However, an interrupt request signal might be negated by clearing the detection flag.

L1UNDFCLR bit (Graphics 1 Underflow Detection Flag Clear)

Writing 1 to the L1UNDFCLR bit clears the graphics 1 underflow detection flag. Clearance of the flag by this bit is only valid for the associated flag, and does not directly affect the other states and interrupt request signals. However, an interrupt request signal might be negated by clearing the detection flag.

L2UNDFCLR bit (Graphics 2 Underflow Detection Flag Clear)

Writing 1 to the L2UNDFCLR bit clears the graphics 2 underflow detection flag. Clearance of the flag by this bit is only valid for the associated flag, and does not directly affect the other states and interrupt request signals. However, an interrupt request signal might be negated by clearing the detection flag.

状态监控标志SYSCNT_STMON[1]不改变，但中断请求信号GLCDC_L1UNDF被否定。

L2UNDFINTEN位（中断请求信号GLCDC_L2UNDF使能控制）

L2UNDFINTEN位启用或禁用中断请求信号GLCDC_L2UNDF。当该位设置为1时，中断请求信号GLCDC_L2UNDF在相关状态监控标志SYSCNT_STMON[2]设置时被断言。当它被清除为0时，即使相关状态监视标志SYSCNT_STMON[2]设置，中断请求信号GLCDC_L2UNDF也不会被断言。如果在GLCDC_L2UNDF断言期间清除该位，则相关的状态监控标志SYSCNT_STMON[2]不会改变，但中断请求信号GLCDC_L2UNDF被否定。

58.2.58 系统控制块状态清除寄存器(SYSCNT_STCLR)

Address(es): GLCDC.SYSCNT_STCLR 400E 1448h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	L2UNDFCLR	L1UNDFCLR	VPOSCLR
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	VPOSCLR	图形2指定线检测标记清除	0：无操作1：清除图形2指定线检测标志。	R/W*1
b1	L1UNDFCLR	图形1下溢检测标志Clear	0：无操作1：清除图形1下溢检测标志。	R/W*1
b2	L2UNDFCLR	图形2下溢检测标志Clear	0：无操作1：清除图形2下溢检测标志。	R/W*1
b31 to b3	—	Reserved	这些位被读取为0。写入值应为0。	R/W

Note 1. 这些位读为0。

VPOSCLR位（图形2指定行检测标志清零）

将1写入VPOSCLR位将清除图形2指定线检测标志。该位清零标志只对相关标志有效，不直接影响其他状态和中断请求信号。但是，可以通过清除检测标志来否定中断请求信号。

L1UNDFCLR位（图形1下溢检测标志清零）

将1写入L1UNDFCLR位会清除图形1下溢检测标志。该位清零标志只对相关标志有效，不直接影响其他状态和中断请求信号。但是，可以通过清除检测标志来否定中断请求信号。

L2UNDFCLR位（图形2下溢检测标志清除）

将1写入L2UNDFCLR位可清除图形2下溢检测标志。该位清零标志只对相关标志有效，不直接影响其他状态和中断请求信号。但是，可以通过清除检测标志来否定中断请求信号。

58.2.59 System Control Block Status Monitor Register (SYSCNT_STMON)

Address(es): GLCDC.SYSCNT_STMON 400E 144Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	L2UNDF	L1UNDF	VPOS
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b0	VPOS	Graphics 2 Specified Line Detection Flag	0: Specified line notification not detected in graphics 2 1: Specified line notification detected in graphics 2.	R
b1	L1UNDF	Graphics 1 Underflow Detection Flag	0: No underflow detected in graphics 1 1: Underflow detected in graphics 1.	R
b2	L2UNDF	Graphics 2 Underflow Detection Flag	0: No underflow detected in graphics 2 1: Underflow detected in graphics 2.	R
b31 to b3	—	Reserved	These bits are read as 0.	R

VPOS flag (Graphics 2 Specified Line Detection Flag)

The VPOS flag indicates that the specified line notification was detected in graphics 2. When this flag is 1, it indicates that the specified line notification was detected in graphics 2 at some time in the past. It does not necessarily mean that graphics 2 is currently processing the specified line. When this flag is 0, it indicates that no specified line notification was detected after the module operation was enabled. When the interrupt request signal is enabled and is cleared while this flag is 1, the associated interrupt request signal GLCDC_VPOS is negated, but this does not affect the state of graphics 2.

L1UNDF flag (Graphics 1 Underflow Detection Flag)

The L1UNDF flag indicates that an underflow was detected in graphics 1. When this flag is 1, it indicates that an underflow was detected in graphics 1 at some time in the past. It does not necessarily mean that graphics 1 is currently in the underflow state. When this flag is 0, it indicates that no underflow was detected after the module operation was enabled. When the interrupt request signal is enabled and is cleared while this flag is 1, the associated interrupt request signal GLCDC_L1UNDF is negated, but this does not affect the state of graphics 1.

Even if the current graphics data is not required (GR1_AB1.DISPSEL[1:0] = 0xb), if the SYSCNT_DTCTEN.L1UNDFDTC flag (graphics 1 underflow detection control) is 1 and detection is enabled, this flag sets to 1 at the start of the graphics image valid area. To avoid unnecessary detection flag settings or interrupt request signal assertions, when the display does not require the current graphics data, clear the SYSCNT_DTCTEN.L1UNDFDTC flag and the SYSCNT_INTEN.L1UNDFINTEN bit (interrupt request signal GLCDC_L1UNDF enable control) to 0.

L2UNDF flag (Graphics 2 Underflow Detection Flag)

The L2UNDF flag indicates that an underflow was detected in graphics 2. When this flag is 1, it indicates that an underflow was detected in graphics 2 at some time in the past. It does not necessarily mean that graphics 2 is currently in the underflow state. When this flag is 0, it indicates that no underflow was detected after the module operation was enabled. When the interrupt request signal is enabled and is cleared while this flag is 1, the associated interrupt request signal GLCDC_L2UNDF is negated, but this does not affect the state of graphics 2.

Even if the current graphics data is not required (GR2_AB1.DISPSEL[1:0] = 0xb), if the SYSCNT_DTCTEN.L2UNDFDTC flag (graphics 2 underflow detection control) is 1 and detection is enabled, this flag sets to 1 at the start of the graphics image valid area. To avoid the unnecessary detection flag settings or interrupt request signal assertions, when the display does not require the current graphics data, clear the SYSCNT_DTCTEN.L2UNDFDTC flag and the SYSCNT_INTEN.L2UNDFINTEN bit (interrupt request signal

58.2.59 系统控制块状态监视器寄存器(SYSCNT_STMON)

Address(es): GLCDC.SYSCNT_STMON 400E 144Ch

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	—	—	—	—	—	—	—	—	—	—	L2UNDF	L1UNDF	VPOS
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b0	VPOS	图形2指定线检测 Flag	0：在图形2中未检测到指定线路通知1：在图形2中检测到指定线路通知。	R
b1	L1UNDF	图形1下溢检测标志	0：在图形1中未检测到下溢1：在图形1中检测到下溢。	R
b2	L2UNDF	图形2下溢检测标志	0：在图形2中未检测到下溢1：在图形2中检测到下溢。	R
b31 to b3	—	Reserved	这些位读为0。	R

VPOS标志（图形2指定行检测标志）

VPOS标志表示在图形2中检测到指定线路通知。当该标志为1时，表示在过去某个时间在图形2中检测到指定线路通知。这并不一定意味着图形2当前正在处理指定的行。当该标志为0时，表示启用模块操作后未检测到指定线路通知。当该标志为1时中断请求信号被使能并被清除时，相关的中断请求信号GLCDC_VPOS被否定，但这并不影响图形2的状态。

L1UNDF标志（图形1下溢检测标志）

L1UNDF标志表示在图形1中检测到下溢。当该标志为1时，它表示在过去某个时间在图形1中检测到下溢。这并不一定意味着图形1当前处于下溢状态。该标志为0时，表示模块操作使能后未检测到下溢。当该标志为1时中断请求信号被使能并被清除时，相关的中断请求信号GLCDC_L1UNDF被否定，但这并不影响图形1的状态。

即使不需要当前图形数据（GR1_AB1.DISPSEL[1:0]=0xb），如果SYSCNT_DTCTEN.L1UNDFDTC标志（图形1下溢检测控制）为1并启用检测，该标志在图形图像有效区域开始时设置为1。为避免不必要的检测标志设置或中断请求信号断言，当显示不需要当前图形数据时，清除SYSCNT_DTCTEN.L1UNDFDTC标志和SYSCNT_INTEN.L1UNDFINTEN位（中断请求信号

GLCDC_L1UNDF启用控制）为0。

L2UNDF标志（图形2下溢检测标志）

L2UNDF标志表示在图形2中检测到下溢。当该标志为1时，表示在过去某个时间在图形2中检测到下溢。这并不一定意味着图形2当前处于下溢状态。该标志为0时，表示模块操作使能后未检测到下溢。当该标志为1时中断请求信号被使能并被清除时，相关的中断请求信号GLCDC_L2UNDF被否定，但这并不影响图形2的状态。

即使不需要当前图形数据（GR2_AB1.DISPSEL[1:0]=0xb），如果SYSCNT_DTCTEN.L2UNDFDTC标志（图形2下溢检测控制）为1并启用检测，该标志在图形图像有效区域开始时设置为1。为避免不必要的检测标志设置或中断请求信号断言，当显示不需要当前图形数据时，清除SYSCNT_DTCTEN.L2UNDFDTC标志和SYSCNT_INTEN.L2UNDFINTEN位（中断请求信号

GLCDC_L2UNDF enable control) to 0.

58.2.60 System Control Block Version and Panel Clock Control Register (SYSCNT_PANEL_CLK)

Address(es): GLCDC.SYSCNT_PANEL_CLK 400E 1450h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	VER[15:0]															
Value after reset:	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	PIXSEL	—	—	—	CLKSEL	—	CLKEN	DCDR[5:0]					
Value after reset:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	Bit name	Description	R/W
b5 to b0	DCDR[5:0]	Clock Division Ratio Setting Control	See Table 58.9 for details on these settings.	R/W
b6	CLKEN	Panel Clock Output Enable Control	0: Disable panel clock output 1: Enable panel clock output. Before changing the PIXSEL, CLKSEL, or DCDR bit, this bit must be set to 0.	R/W
b7	—	Reserved	This bit is read as 0. The write value should be 0.	R/W
b8	CLKSEL	Panel Clock Supply Source Control	0: Select external clock (LCD_EXTCLK) 1: Select PLL output.	R/W
b11 to b9	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b12	PIXSEL	Pixel Clock Select Control	0: Select no frequency division, parallel RGB 1: Select quarter frequency, serial RGB. This setting must have the same value as OUT_SET.FRQSEL[1].	R/W
b15 to b13	—	Reserved	These bits are read as 0. The write value should be 0.	R/W
b31 to b16	VER[15:0]	Version Information	Version information of the GLCDC.	R

The configuration of the pixel and panel clock generator circuits are shown in Figure 9.1, Clock generation circuit block diagram.

DCDR[5:0] bits (Clock Division Ratio Setting Control)

The DCDR[5:0] bits control the setting of the panel clock division ratio. The division ratio bit can only be set to the values listed in Table 58.9. Operation is not guaranteed for values not listed.

Table 58.9 Input clock division (1 of 2)

DCDR[5:0]	Clock division ratio	CLKSEL = 0, LCD_EXTCLK(≤ 60 MHz)	CLKSEL = 1, PLL output (120 to 240 MHz)
000000b	1/2	LCD_EXTCLK/2	PLL output/2*1
000001b	1/1	LCD_EXTCLK*1	PLL output*1
000010b	1/2	LCD_EXTCLK/2	PLL output/2*1
000011b	1/3	LCD_EXTCLK/3	PLL output/3*1
000100b	1/4	LCD_EXTCLK/4	PLL output/4*1
000101b	1/5	LCD_EXTCLK/5	PLL output/5
000110b	1/6	LCD_EXTCLK/6	PLL output/6
000111b	1/7	LCD_EXTCLK/7	PLL output/7
001000b	1/8	LCD_EXTCLK/8	PLL output/8

GLCDC_L2UNDF启用控制）为0。

58.2.60 系统控制块版本和面板时钟控制寄存器(SYSCNT_PANEL_CLK)

Address(es): GLCDC.SYSCNT_PANEL_CLK 400E 1450h

	b31	b30	b29	b28	b27	b26	b25	b24	b23	b22	b21	b20	b19	b18	b17	b16
	VER[15:0]															
重置后的值：	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0

	b15	b14	b13	b12	b11	b10	b9	b8	b7	b6	b5	b4	b3	b2	b1	b0
	—	—	—	PIXSEL	—	—	—	CLKSEL	—	CLKEN	DCDR[5:0]					
重置后的值：	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Bit	Symbol	位名称	Description	R/W
b5 to b0	DCDR[5:0]	时钟分频比设置 Control	有关这些设置的详细信息，请参见表58.9。	R/W
b6	CLKEN	面板时钟输出使能 Control	0：禁用面板时钟输出1：启用面板时钟输出。在更改PIXSEL、CLKSEL或DCDR位之前，该位必须设置为0。	R/W
b7	—	Reserved	该位读取为0。写入值应为0。	R/W
b8	CLKSEL	面板时钟电源 Control	0：选择外部时钟(LCD_EXTCLK)1：选择PLL输出。	R/W
b11 to b9	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b12	PIXSEL	像素时钟选择控制	0：选择不分频，并行RGB1：选择四分之一频率，串行RGB。此设置的值必须与 OUT_SET.FRQSEL[1].	R/W
b15 to b13	—	Reserved	这些位被读取为0。写入值应为0。	R/W
b31 to b16	VER[15:0]	版本信息	GLCDC的版本信息。	R

像素和面板时钟发生器电路的配置如图9.1时钟发生器电路框图所示。

DCDR[5:0]位（时钟分频比设置控制）

DCDR[5:0]位控制面板时钟分频比的设置。分频比位只能设置为表58.9中列出的值。对于未列出的值，不保证操作。

Table 58.9 输入时钟分频（1of2）

DCDR[5:0]	时钟分频比	CLKSEL = 0, LCD_EXTCLK(≤ 60 MHz)	CLKSEL=1，PLL输出（120至240MHz）
000000b	1/2	LCD_EXTCLK/2	PLL output/2*1
000001b	1/1	LCD_EXTCLK*1	PLL output*1
000010b	1/2	LCD_EXTCLK/2	PLL output/2*1
000011b	1/3	LCD_EXTCLK/3	PLL output/3*1
000100b	1/4	LCD_EXTCLK/4	PLL output/4*1
000101b	1/5	LCD_EXTCLK/5	PLL output/5
000110b	1/6	LCD_EXTCLK/6	PLL output/6
000111b	1/7	LCD_EXTCLK/7	PLL output/7
001000b	1/8	LCD_EXTCLK/8	PLL output/8

Table 58.9 Input clock division (2 of 2)

DCDR[5:0]	Clock division ratio	CLKSEL = 0, LCD_EXTCLK(≤ 60 MHz)	CLKSEL = 1, PLL output (120 to 240 MHz)
001001b	1/9	LCD_EXTCLK/9	PLL output/9
001100b	1/12	LCD_EXTCLK/12	PLL output/12
010000b	1/16	LCD_EXTCLK/16	PLL output/16
011000b	1/24	LCD_EXTCLK/24	PLL output/24
100000b	1/32	LCD_EXTCLK/32	PLL output/32

Note 1. The panel clock is output as the LCD_CLK output clock. This setting may be prohibited because LCD_EXTCLK and LCD_CLK have limited frequencies. See section 60, Electrical Characteristics.

To set the panel clock:

1. After setting the input source of the panel clock in the CLKSEL bit, set the division ratio in the DCDR[5:0] bits and the pixel clock selection.
2. Set the CLKEN bit to 1.

CLKEN bit (Panel Clock Output Enable Control)

The CLKEN bit enables or disables the panel clock output. When enabling the panel clock output and operating the panel clock block, set this bit to 1. When changing the PIXSEL, CLKSEL, or DCDR bit, you must set this bit to 0 once and stop the panel clock output. Operation is not guaranteed if any setting is changed while the panel clock is being output.

CLKSEL bit (Panel Clock Supply Source Control)

The CLKSEL bit controls the selection of the panel clock supply source from either the external clock pin (LCD_EXTCLK) or PLL output. When the external clock is selected, set this bit to 0. When PLL output is selected, set this bit to 1.

PIXSEL bit (Pixel Clock Select Control)

The PIXSEL bit controls the selection of the pixel clock output. When selecting parallel RGB, set this bit to 0 to output the same frequency as the panel clock (no frequency division). When selecting serial RGB, set this bit to 1 to output the quarter frequency of the panel clock as the pixel clock.

This bit must be synchronized with the OUT_SET.FRQSEL[1:0] setting. You must set the same value as in FRQSEL[1]. Otherwise, operation is not guaranteed.

VER[15:0] bits (Version Information)

The VER[15:0] bits provide GLCDC version information.

58.3 Operation

58.3.1 Overall Control

The GLCDC consists of six modules as shown in Figure 58.22, each of which functions independently. The four modules handling image data are interconnected by the vertical and horizontal synchronization signals VS, HS, VE, and HE, and image data (RGB888), as shown in Figure 58.23. The processing of image data is carried out with the pixel clock (PXCLK). LCD_CLK synchronizes with PXCLK (also in phase with each other), and has the same or quadruple frequency (for serial RGB888 output). The registers controlling operation and setting parameters are connected with the internal peripheral bus 8 and operate on PCLKA. The circuits, including the data buffer and the CLUT memory, operate on PCLKA to read graphics data from the GPX bus, access the color palette (CLUT) memory, and expand graphics data into the ARGB8888 format.

Table 58.9 输入时钟分频（2之2）

DCDR[5:0]	时钟分频比	CLKSEL = 0, LCD_EXTCLK(≤ 60 MHz)	CLKSEL=1，PLL输出（120至240MHz）
001001b	1/9	LCD_EXTCLK/9	PLL output/9
001100b	1/12	LCD_EXTCLK/12	PLL output/12
010000b	1/16	LCD_EXTCLK/16	PLL output/16
011000b	1/24	LCD_EXTCLK/24	PLL output/24
100000b	1/32	LCD_EXTCLK/32	PLL output/32

Note 1. 面板时钟作为LCD_CLK输出时钟输出。此设置可能会被禁止，因为LCD_EXTCLK和LCD_CLK的频率有限。请参见第60节，电气特性。

设置面板时钟：

1. 在CLKSEL位设置面板时钟的输入源后，在DCDR[5:0]位设置分频比和像素时钟选择。
2. 将CLKEN位设置为1。

CLKEN位（面板时钟输出使能控制）

CLKEN位启用或禁用面板时钟输出。当使能面板时钟输出并操作面板时钟模块时，将该位设置为1。当更改PIXSEL、CLKSEL或DCDR位时，必须将该位设置为0一次并停止面板时钟输出。如果在面板时钟输出期间更改任何设置，则无法保证操作。

CLKSEL位（面板时钟电源控制）

CLKSEL位控制来自外部时钟引脚(LCD_EXTCLK)或PLL输出的面板时钟供应源的选择。Whentheexternalclockisselected setthisbitto0.WhenPLLoutputisselected setthisbitto1.

PIXSEL位（像素时钟选择控制）

PIXSEL位控制像素时钟输出的选择。选择并行RGB时，将此位设置为0以输出与面板时钟相同的频率（不分频）。选择串行RGB时，将此位设置为1，以输出面板时钟的四分之一频率作为像素时钟。

该位必须与OUT_SET.FRQSEL[1:0]设置同步。您必须设置与FRQSEL[1]中相同的值。
否则，无法保证操作。

VER[15:0]位（版本信息）

VER[15:0]位提供GLCDC版本信息。

58.3 Operation

58.3.1 整体控制

GLCDC由如图58.22所示的六个模块组成，每个模块独立运行。处理图像数据的四个模块通过垂直和水平同步信号VS、HS、VE、HE和图像数据（RGB888）相互连接，如图58.23所示。图像数据的处理是通过像素时钟(PXCLK)进行的。LCD_CLK与PXCLK同步（彼此同相），并具有相同或四倍的频率（用于串行RGB888输出）。控制操作和设置参数的寄存器与内部外围总线8相连，在PCLKA上操作。这些电路，包括数据缓冲器和CLUT内存，在PCLKA上运行以从GPX总线读取图形数据，访问调色板(CLUT)内存，并将图形数据扩展为ARGB8888格式。

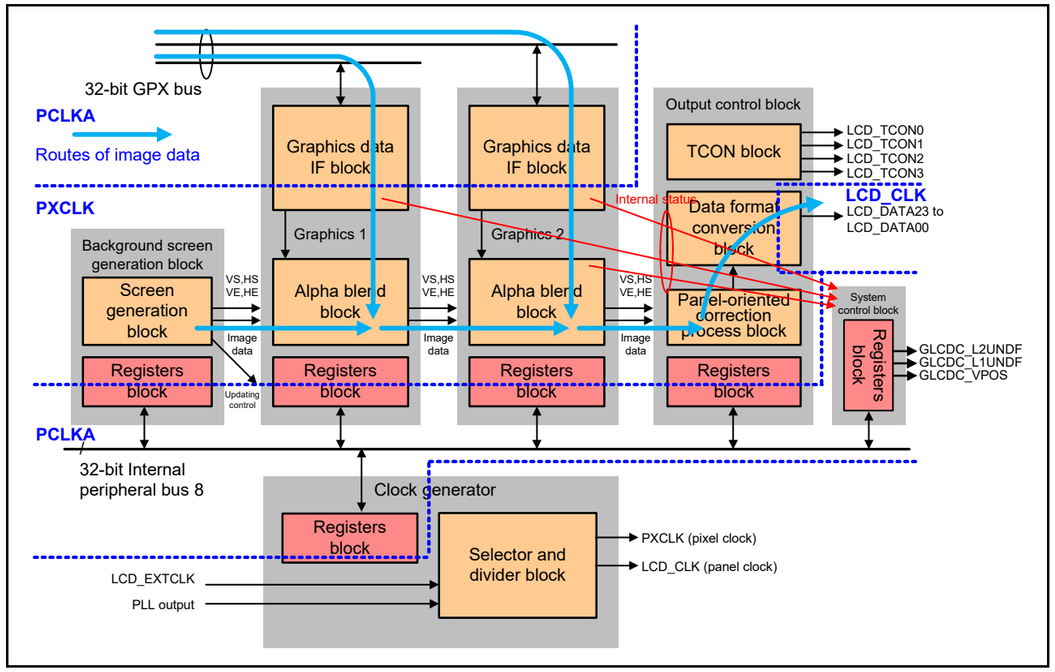


Figure 58.22 GLCDC configuration

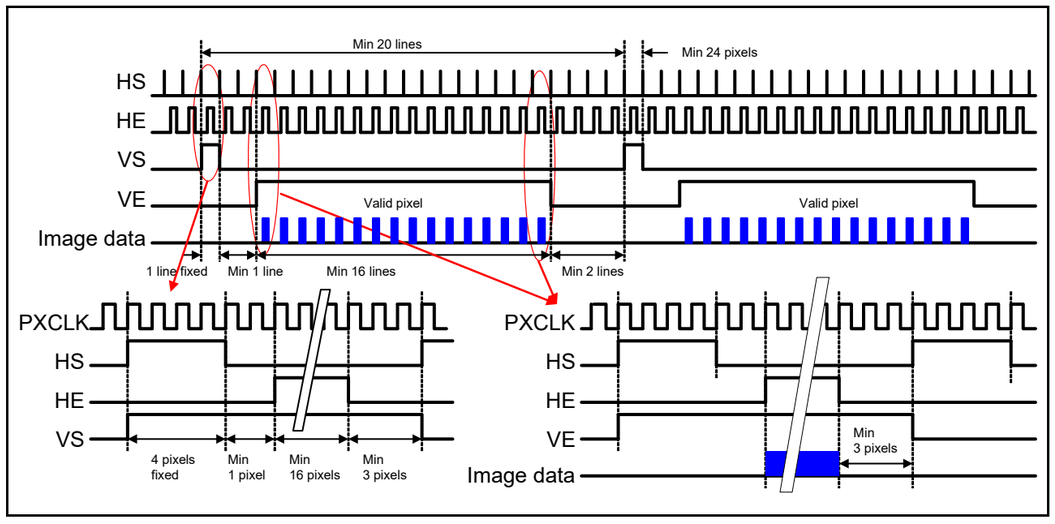


Figure 58.23 Image data carrier signals in the GLCDC

The graphics 1, graphics 2, and output control modules have no individual operation enable bits. By clearing the software reset state in the background screen generation module, these modules wait for vertical and horizontal synchronization signals VS, HS,VE, and HE, and image data (RGB888) to be input, detect assertion of the vertical synchronization signal VS, and start operation for each frame based on the values preset in the registers. For the system control module, clearing the software reset state in the background screen generation module allows it to monitor the status of graphics 1 and 2 in accordance with the register settings and assert interrupt request signals. These status flags are intended for observing the internal status and exert no influence on the internal operation. The operation between startup and stop of the GLCDC is

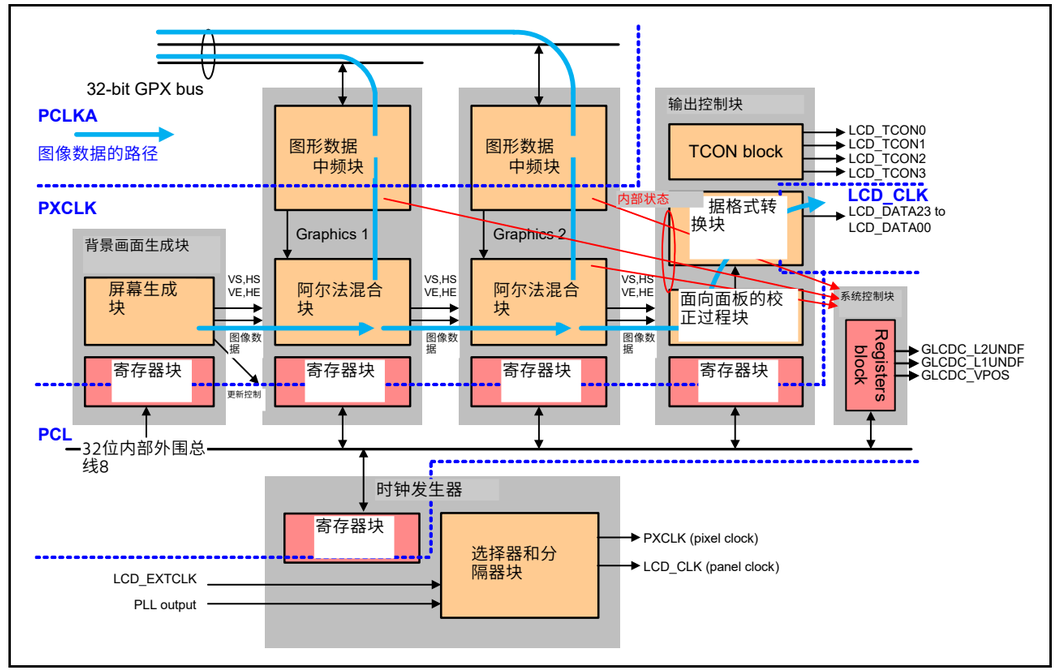


Figure 58.22 GLCDC configuration

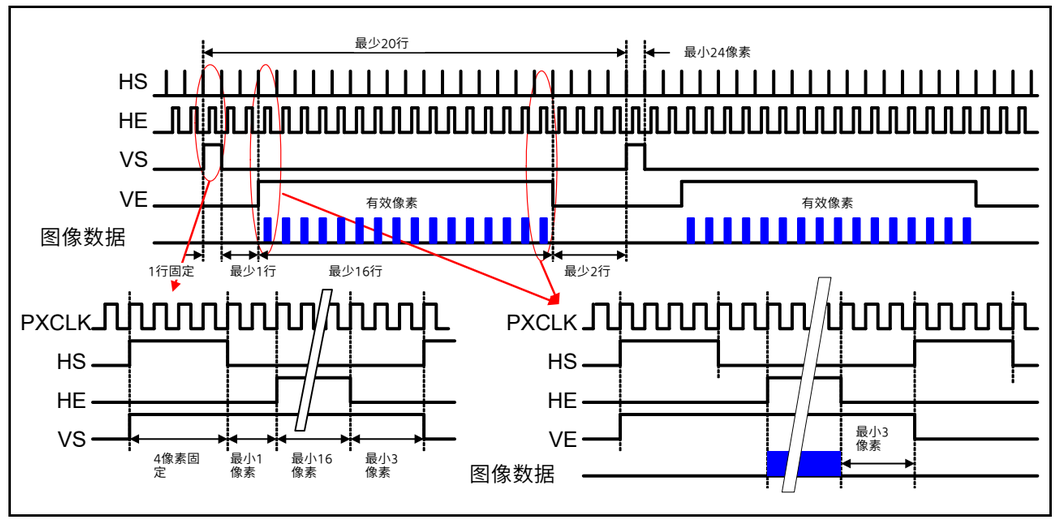


Figure 58.23 GLCDC中的图像数据载体信号

图形1、图形2和输出控制模块没有单独的操作使能位。通过清除后台屏幕生成模块中的软件复位状态，这些模块等待垂直和水平同步信号VS、HS、VE和HE以及图像数据（RGB888）的输入，检测垂直同步信号VS的断言，并根据寄存器中预设的值开始每一帧的操作。对于系统控制模块，清除后台画面生成模块中的软件复位状态，可以根据寄存器设置监控图形1和2的状态，并断言中断请求信号。这些状态标志用于观察内部状态，不影响内部操作。GLCDC启动和停止之间的操作是

outlined in this section.

(1) Startup

To start GLCDC operation:

1. Confirm that PCLKA is supplied to the GLCDC and that the reset is negated. When setting LCD_CLK to the same frequency as PXCLK or LCD_CLK to the quadruple speed clock, the setting must be consistent with the value in the register specified in the subsequent stage. The quadruple speed clock is required only when the output format is serial RGB888. Operation is not guaranteed if the quadruple speed clock is supplied to LCD_CLK in other output formats than serial RGB888.
2. Set 1 to the BG_EN.SWRST bit to release the entire GLCDC from a software reset.
3. Set parameters necessary for operation in each register. Although registers of any module can be set first, while the BG_EN.VEN bit (control of GLCDC internal register value reflection to internal operations), BG_EN.EN bit (background plane operation enable) of the background screen generation module, and the VEN bit in the register update control register of each module remain cleared to 0, confirm that PCLKA and PXCLK/LCD_CLK are supplied and the BG_MON.SWRST bit (entire module software reset state monitor) is set to 1.
4. When displaying the graphics data read by graphics 1 and 2 through the GPX bus, set 1 to the GRn_FLMRD.RENB bit (graphics data read enable).
5. Write the color palette data of graphics 1 and 2 (0 and 1 planes) to the CLUT memory through the register access bus (internal peripheral bus 8) as required. This is necessary for the LUT1, LUT4, LUT8, and ARGB1555 data formats. ARGB1555 uses addresses 80h and 00h on the two planes, LUT1 uses 01h and 00h, LUT4 uses the addresses from 0Fh to 00h, and LUT8 uses the addresses from FFh to 00h.
6. Set 1 to the BG_EN.VEN bit (control of background plane register value reflection to internal operations) and the BG_EN.EN bit (background plane operation enable) of the background screen generation module at the same time. This setting allows output of the vertical and horizontal synchronization signals VS, HS, VE, and HE, and the image data (RGB888) from the background screen generation module. When the pixel data is valid (both VE and HE are 1), output from the background screen generation module uses the value in the BG_BGC register. The data value is 00 0000h for pixels that are not valid.
7. Each module detects the assertion of the vertical synchronization signal (VS) output from its previous stage (background screen generation module for graphics 1, graphics 1 for graphics 2, and graphics 2 for the output control module) and starts operation in accordance with its register settings. All the modules control the operation in frame units. When the assertion of the vertical synchronization signal (VS) is detected, the current frame is taken as the frame head and the status is initialized. If necessary (when the VEN bits in the register update control registers are 1), the register values read through the register access bus are reflected to the internal operation.

(2) Changing parameters during operation

With the GLCDC, it is possible to update parameters of each module and reflect the updates to the internal operations during operation, without preventing graphics data to be read by the background screen generation module, graphics 1, or graphics 2. By setting 1 to the VEN bits of the modules, including the background screen generation module, almost all parameters are reflected to the internal operations at the start of the following frame (at the start of the control screen for the background screen generation module, and immediately after the VS assertion of the previous stage for the other modules). However, if the CLUT plane being used for internal operations (determined in the GRn_CLUTINT.SEL[1:0] bits) is modified, the updates are reflected to the internal operations immediately without waiting for the following VS assertion. To circumvent this immediate reflection of the CLUT plane modification to the internal operations, first write all the image data (ARGB8888) necessary for the CLUT plane that is not being used for internal operations, next modify the GRn_CLUTINT.SEL[1:0] bits, and finally set 1 to the VEN bit of the background screen generation module or the target module.

To modify parameters during operation:

1. Confirm that the VEN bit of each module is 0. Operation is not guaranteed if the target registers are modified when the VEN bit of the module to which the register values are to be reflected to the internal operations, or the VEN bit of the background screen generation module is 1.
2. Modify the value of the target registers.
3. If only a particular module is to be the target, set 1 to the VEN bit of the target module. If multiple modules or the

本节概述。

(1) Startup

启动GLCDC操作：

1. 确认PCLKA被提供给GLCDC并且复位被否定。将LCD_CLK设置为与PXCLK相同的频率或将LCD_CLK设置为四倍速时钟时，设置必须与后续阶段指定的寄存器中的值一致。仅当输出格式为串行RGB888时才需要四倍速时钟。如果以串行RGB888以外的其他输出格式向LCD_CLK提供四倍速时钟，则无法保证操作。
2. 将BG_EN.SWRST位设置为1以从软件复位中释放整个GLCDC。
3. 在每个寄存器中设置操作所需的参数。虽然可以先设置任意模块的寄存器，但是后台画面生成模块的BG_EN.VEN位（控制GLCDC内部寄存器值反映到内部操作）、BG_EN.EN位（后台平面操作使能）、VEN位在每个模块的寄存器更新控制寄存器中保持清零，确认PCLKA和PXCLKLCD_CLK已供电且BG_MON.SWRST位（整个模块软件复位状态监视器）设置为1。
4. 当显示图形1和2通过GPX总线读取的图形数据时，将GRn_FLMRD.RENB位设置为1（图形数据读取使能）。
5. 根据需要通过寄存器访问总线（内部外围总线8）将图形1和2（0和1平面）的调色板数据写入CLUT内存。这对于LUT1、LUT4、LUT8和ARGB1555数据格式是必需的。ARGB1555在两个平面上使用地址80h和00h，LUT1使用01h和00h，LUT4使用0Fh到00h的地址，LUT8使用FFh到00h的地址。
6. 同时将背景画面生成模块的BG_EN.VEN位（控制背景平面寄存器值反映到内部操作）和BG_EN.EN位（背景平面操作使能）置1。此设置允许输出垂直和水平同步信号VS、HS、VE和HE，以及来自背景屏幕生成模块的图像数据(RGB888)。当像素数据有效时（VE和HE均为1），背景画面生成模块的输出使用BG_BGC寄存器中的值。无效像素的数据值为000000h。
7. 每个模块检测从其前一级输出的垂直同步信号（VS）的断言（图形1的背景屏幕生成模块，图形2的图形1和输出控制模块的图形2）并根据其寄存器开始操作设置。所有模块都以帧为单位控制操作。当检测到垂直同步信号（VS）有效时，将当前帧作为帧头并初始化状态。如有必要（当寄存器更新控制寄存器中的VEN位为1时），通过寄存器访问总线读取的寄存器值反映到内部操作。

(2) 在运行期间更改参数

使用GLCDC，可以在运行期间更新每个模块的参数并将更新反映到内部操作，而不会阻止背景屏幕生成模块、图形1或图形2读取图形数据。通过将1设置为模块的VEN位，包括背景画面生成模块，几乎所有参数都反映到下一帧开始时的内部操作（背景画面生成模块的控制画面开始时，VS断言后立即）其他模块的前一阶段）。但是，如果用于内部操作的CLUT平面（在GRn_CLUTINT.SEL[1:0]位中确定）被修改，则更新会立即反映到内部操作，而无需等待以下VS断言。为了避免CLUT平面修改对内部操作的直接反映，首先写入未用于内部操作的CLUT平面所需的所有图像数据(ARGB8888)，然后修改GRn_CLUTINT.SEL[1:0]位，最后将后台画面生成模块或目标模块的VEN位设置为1。

在运行过程中修改参数：

1. 确认每个模块的VEN位为0。如果要反映寄存器值的模块的VEN位被修改为内部操作，或者后台屏幕的VEN位被修改，则不保证操作生成模块为1。
2. 修改目标寄存器的值。
3. 如果仅将特定模块作为目标，则将目标模块的VEN位设置为1。如果多个模块或

background screen generation module are to be the targets, set 1 to the VEN bit of the background screen generation module. In this case, all the modules are included as targets, not only the background screen generation module.

4. Confirm that the VEN bit to which 1 was set is 0. If the bit is cleared to 0, the target register contents are reflected to the internal operations. If the bit remains 1, however, the target register contents might not yet be reflected to the internal operations. The VEN bit of each module is cleared to 0 immediately after the target register values are internally reflected. However, the VEN bit of the background screen generation module is not cleared to 0 until the module output VE is negated (with all the modules, sufficient delay is secured in reference to the VS assertion of the background screen generation module so that the register values are reflected to the internal operations for the same frame). Figure 58.24 shows the operation of the signals output by the background screen generation module and the monitor bits.

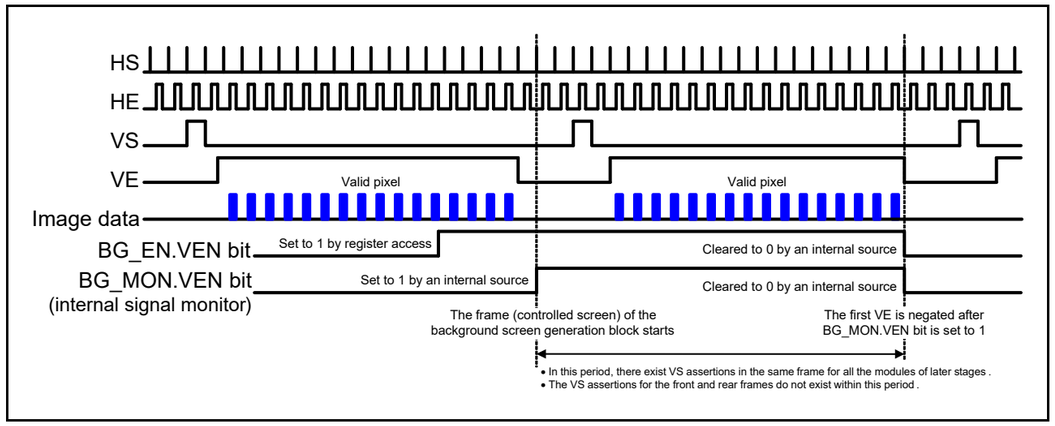


Figure 58.24 Control signals for register value reflection to internal operations

(3) Stopping and restarting in normal operation

To stop the GLCDC:

1. Confirm that the VEN bit of each module is cleared to 0.
2. Clear the BG_EN.EN bit (background plane operation enable) of the background screen generation module to 0.
3. Confirm that the BG_MON.EN bit (background plane operation monitor) of the background screen generation module has changed to 0. This bit is cleared to 0 only after operation has stopped. It is cleared at the frame end of the background screen generation module, not when the operations of all the modules are complete (not at the frame end of the output control module). If it is necessary to wait for all the modules to complete operations, a certain period (for example, a period equivalent to one line) is required.
4. Usually, a software reset can be safely applied (clearing of the BG_EN.SWRST bit) after confirming that the BG_MON.EN bit of the background screen generation module has changed to 0. (Even if the output signal returns to the initial value, no problems occur because the GLCDC has already entered the vertical blanking interval.)
5. When restarting the GLCDC by setting the relevant registers without applying a software reset, wait until sufficient time elapses after the BG_MON.EN bit becomes 0 (when the output control module output is the frame end) before starting the GLCDC. The GLCDC itself is not affected by this because the GLCDC starts operating after recognizing the assertion of the VS of the previous stage as the frame head. However, operation of some connected devices might be affected if a blanking interval or a period equivalent to one line is too short. For details, check the specifications of the connected device. When a software reset is applied, the register values are also initialized and almost all of the registers must be set again. Only the color palette data (CLUT memory content) is retained (only for a software reset after normal end).

Figure 58.25 shows the changes in signal lines and bits for the stop and restart in normal operation. Even if the background screen generation module is stopped by a clearing of the BG_EN.EN bit to 0, the GLCDC stops because of an abnormal operation sequence, not normal operation, if the GPX bus access is not complete at the frame end because of an underflow in graphics 1 or 2, inappropriate setting of graphics data access, or other undesirable conditions.

背景画面生成模块作为对象，将背景画面生成模块的VEN位设为1。在这种情况下，所有模块都作为目标包括在内，而不仅仅是背景屏幕生成模块。

4. 确认设置为1的VEN位为0。如果该位被清除为0，则目标寄存器内容反映到内部操作中。但是，如果该位保持为1，则目标寄存器内容可能尚未反映到内部操作中。每个模块的VEN位在目标寄存器值在内部反映后立即清零。但是，背景屏幕生成模块的VEN位不会被清除为0，直到模块输出VE被取反（对于所有模块，参考背景屏幕生成模块的VS断言确保足够的延迟，以便寄存器值反映到同一帧的内部操作）。图58.24显示了背景屏幕生成模块和监视器位输出的信号的操作。

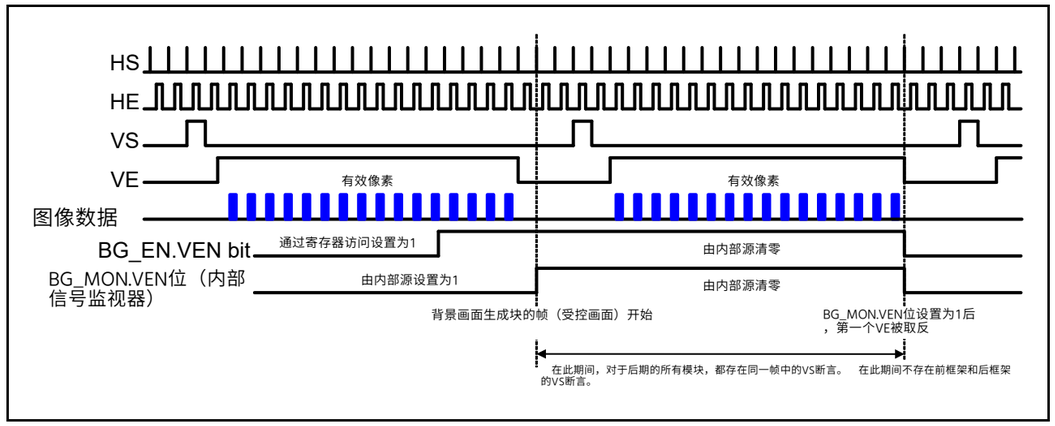


Figure 58.24 寄存器值反映到内部操作的控制信号

(3) 正常运行中的停止和重新启动

要停止GLCDC：

1. 确认各模块的VEN位清零。
2. 将后台画面生成模块的BG_EN.EN位（后台平面操作使能）清0。
3. 确认后台画面生成模块的BG_MON.EN位（后台平面操作监视器）已变为0。只有在操作停止后，该位才清为0。在后台画面生成模块的帧尾清零，而不是在所有模块操作完成时（不是在输出控制模块的帧尾）。如果需要等待所有模块完成操作，则需要一定的周期（例如，相当于一行的周期）。
4. 通常，在确认背景画面生成模块的BG_MON.EN位已变为0后，可以安全地应用软件复位（清除BG_EN.SWRST位）。（即使输出信号恢复到初始值，也不会出现问题是因为GLCDC已经进入垂直消隐区间。）
5. 在不应用软件复位的情况下通过设置相关寄存器重新启动GLCDC时，请等到BG_MON.EN位变为0（当输出控制模块输出为帧结束时）经过足够的时间后，再启动GLCDC。GLCDC本身不受此影响，因为GLCDC在将前一级的VS的断言识别为帧头后开始运行。但是，如果消隐间隔或相当于一条线的周期太短，可能会影响某些连接设备的操作。有关详细信息，请检查所连接设备的规格。当应用软件复位时，寄存器值也被初始化并且几乎所有的寄存器都必须重新设置。仅保留调色板数据（CLUT内存内容）（仅用于正常结束后的软件复位）。

图58.25显示了正常操作中停止和重启的信号线和位的变化。即使背景屏幕生成模块通过将BG_EN.EN位清除为0来停止，如果GPX总线访问在帧结束时由于图形1或2中的下溢、图形数据访问设置不当或其他不良情况。

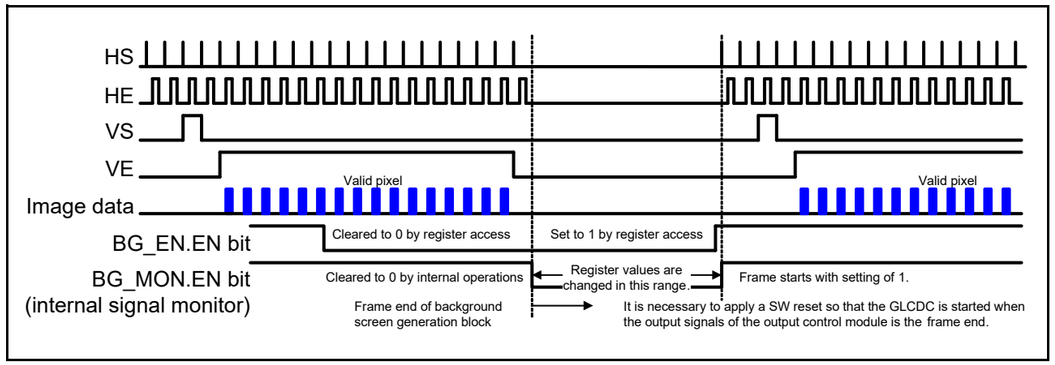


Figure 58.25 Stop and restart in normal operation

(4) Stopping and restarting in abnormal operation

Stop in abnormal operation occurs in the following cases:

- When during operation (BG_EN.EN or BG_MON.EN is set to 1), a software reset (BG_EN.SWRST bit is cleared to 0) or a reset is applied
- When unnecessary (unintended) access to the GPX bus occurs and a data cycle is not completed, even though the BG_EN.EN bit is cleared to 0 and so the BG_MON.EN bit is also cleared to 0.

In both cases, the GLCDC is internally initialized and the register access bus can be accessed normally (except for a hardware reset). However, the GPX bus might write unintended graphics data to the GLCDC. Therefore, it is advisable to apply a software reset (clear the BG_EN.SWRST bit to 0) and confirm that there is no unintended access to the GPX bus, even after confirming that both the BG_EN.EN and BG_MON.EN bits are cleared to 0. Next release the GLCDC from the software reset (set the BG_EN.SWRST bit to 1), set the relevant registers, and set the BG_EN.En and BG_EN.VEN bits in the background screen generation module to 1 to restart the GLCDC. For the procedure for checking the GPX bus state, see the *Arm® AHB Specification*. Use this procedure even after a reset when the GPX bus, a target device, or a target controller is not initialized. If these are initialized on a reset assertion for the GLCDC, a normal startup procedure can be used without checking the GPX bus state.

58.3.2 Screen Definition

The essential signals for GLCDC operations are generated by the background screen generation module, and the graphics 1 and 2 modules and output control module operate based on the sequentially transferred vertical and horizontal synchronization signals (VS and HS) and vertical and horizontal pixel enable signals (VE and HE). The reference point (frame start point) of the background screen cannot be determined by the output signals. The point shown in the figures is virtual and provided only for register settings. The reference points (frame start points) of the graphics 1 and 2 modules and output control module are the assertion of the vertical synchronization signal (VS), which is input (output) from the previous stage. Each module defines the valid pixel display area and special processing area for pixel data (rectangular areas for graphics 1 and 2) according to the position and width based on this reference point. Figure 58.26 shows the definition of the background screen, and Figure 58.27 shows the definition of the graphics 1 and 2 screen. The output control module performs correction for the entire valid pixel area (when both VE and HE are 1) output from the previous stage (graphics 2). (No registers are provided in the output control module for setting the correction area.) TCON in the output control module generates the control signals to be output based on the internal vertical and horizontal synchronization signals (VS and HS), and the change timing of the output signals can be freely modified within the valid setting range specifiable in the registers.

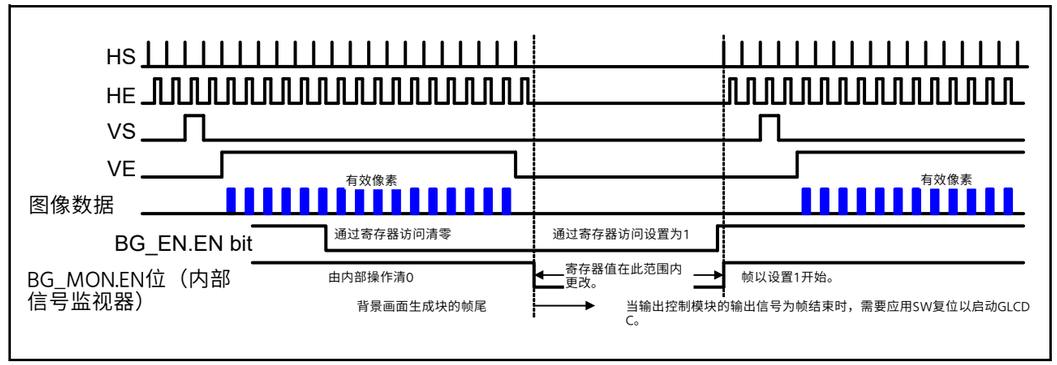


Figure 58.25 在正常运行中停止和重新启动

(4) 异常运行中的停止和重新启动

在以下情况下会出现异常停止：

- 操作期间（BG_EN.EN或BG_MON.EN设置为1）时，软件复位（BG_EN.SWRST位清零）或应用复位
- 当发生对GPX总线的不必要（意外）访问且数据周期未完成时，即使BG_EN.EN位清零，因此BG_MON.EN位也清零。

在这两种情况下，GLCDC都在内部进行了初始化，并且可以正常访问寄存器访问总线（硬件复位除外）。但是，GPX总线可能会将意外的图形数据写入GLCDC。因此，建议应用软件复位（将BG_EN.SWRST位清0）并确认没有意外访问GPX总线，即使在确认BG_EN.EN和BG_MON.EN位都被清零之后0.接下来从软件复位中释放GLCDC（将BG_EN.SWRST位设置为1），设置相关寄存器，并将后台屏幕生成模块中的BG_EN.En和BG_EN.VEN位设置为1，重新启动GLCDC。有关检查GPX总线状态的过程，请参阅Arm®AHB规范。即使在GPX总线、目标设备或目标控制器未初始化时重置后，也可以使用此过程。如果这些在GLCDC的复位断言上被初始化，则可以使用正常启动过程而不检查GPX总线状态。

58.3.2 屏幕定义

GLCDC操作的基本信号由背景屏幕生成模块产生，图形1和2模块和输出控制模块根据顺序传输的垂直和水平同步信号（VS和HS）和垂直和水平像素使能信号（VE和他）。背景画面的参考点（帧开始点）不能由输出信号确定。图中显示的点是虚拟的，仅用于寄存器设置。图形1和2模块和输出控制模块的参考点（帧起点）是垂直同步信号（VS）的断言，它是从前一级输入（输出）的。每个模块根据这个参考点的位置和宽度，定义了像素数据的有效像素显示区域和特殊处理区域（图形1和2的矩形区域）。图58.26显示了背景屏幕的定义，图58.27显示了图形1和2屏幕的定义。输出控制模块对前一阶段输出的整个有效像素区域（当VE和HE均为1时）进行校正（图2）。（输出控制模块中没有提供设置校正区域的寄存器。）输出控制模块中的TCON根据内部垂直和水平同步信号（VS和HS）产生控制信号输出，以及输出信号可以在寄存器指定的有效设置范围内自由修改。

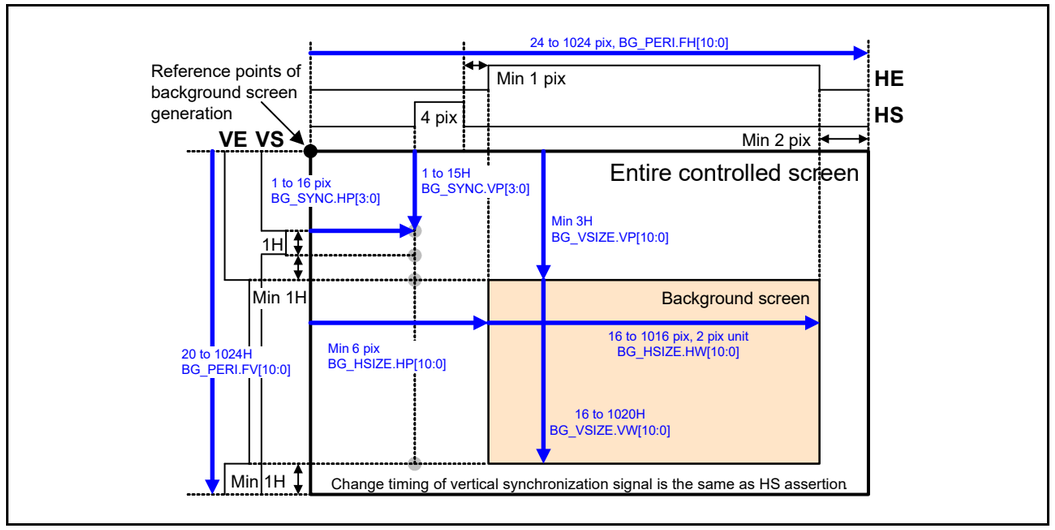


Figure 58.26 Internal definition of background screen

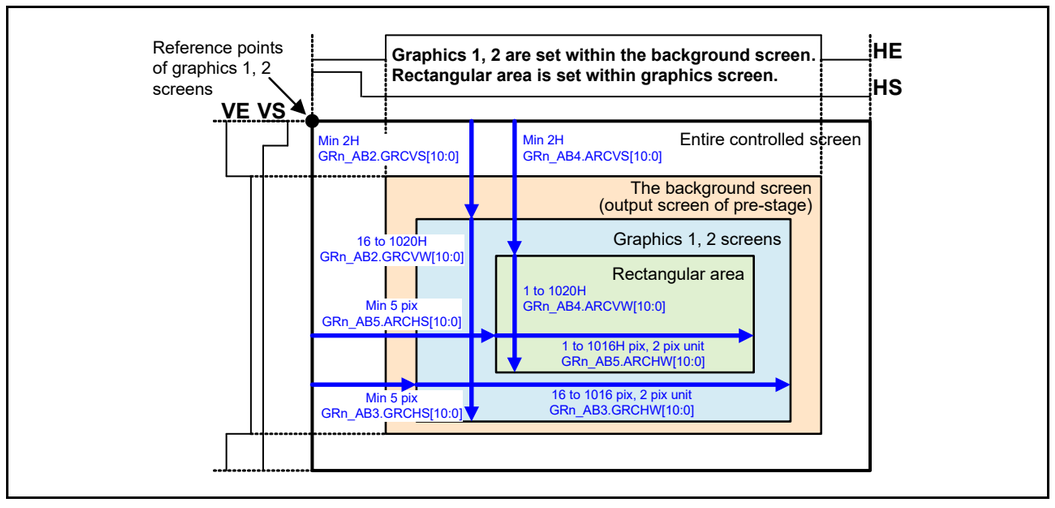


Figure 58.27 Internal definition of graphics 1 and 2 screens

58.3.3 Underflow and Interrupts

The GLCDC can detect the three types of status conditions described in this section. To detect each status condition, set the associated bit in the Status Detection Control Register (SYSCNT_DTCTEN) to 1.

58.3.3.1 Graphics 2 underflow detection

This function detects underflows in the graphics data interface block for graphics 2. The SYSCNT_STMON.L2UNDF flag sets to 1 if the graphics data cannot be read from the graphics data interface block (if valid data is not stored in the 4-stage ring buffer). The underflow is cleared as an internal state of graphics 2 on the VS (vertical synchronization) signal assertion of the previous stage. However, to clear the relevant bit in the Status Monitor Register of the system control block, the software must set the associated bit in the Status Clear Register to 1.

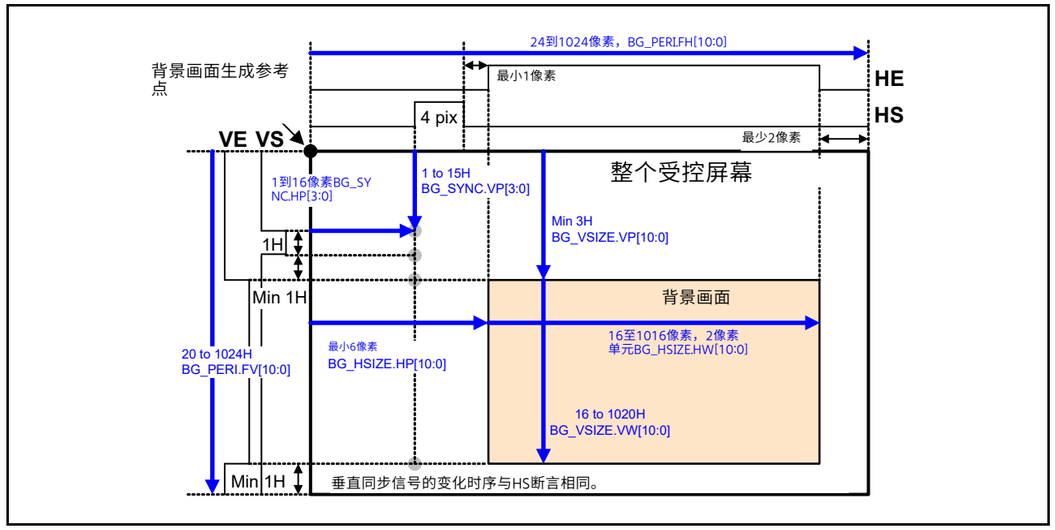


Figure 58.26 背景画面的内部定义

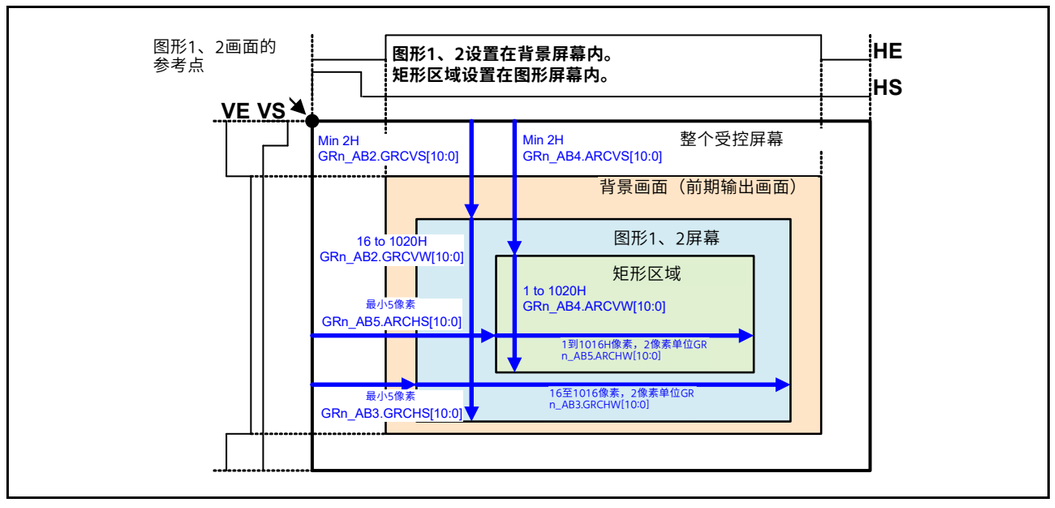


Figure 58.27 图形1和2屏幕的内部定义

58.3.3 下溢和中断

GLCDC可以检测本节中描述的三种状态条件。要检测每个状态条件，请将状态检测控制寄存器(SYSCNT_DTCTEN)中的相关位设置为1。

58.3.3.1 图形2下溢检测

此函数检测图形2的图形数据接口块中的下溢。如果无法从图形数据接口块中读取图形数据（如果有效数据未存储在4级环形缓冲区中），则SYSCNT_STMON.L2UNDF标志设置为1。在前一阶段的VS（垂直同步）信号断言上，下溢作为图形2的内部状态被清除。但是，要清除系统控制块的状态监视器寄存器中的相关位，软件必须将状态清除寄存器中的相关位设置为1。

58.3.3.2 Graphics 1 underflow detection

This function detects underflows in the graphics data interface block for graphics 1. The SYSCNT_STMON.L1UNDF flag is set to 1 if the graphics data cannot be read from the graphics data interface block (if valid data is not stored in the 4-stage ring buffer). The underflow is cleared as an internal state of graphics 1 on the VS (vertical synchronization) signal assertion of the previous stage. However, to clear the relevant bit in the Status Monitor Register of the system control block, the software must set the associated bit in the Status Clear Register to 1.

58.3.3.3 Graphics 2 line detection

This function detects that the number of lines specified in the GR2_CLUTINT.LINE[10:0] bit was processed. The detection is performed on the HS (horizontal synchronization) signal assertion of the previous stage, not when valid pixels start to be processed. Each time the number of detected lines reach the value specified for graphics 2, the SYSCNT_STMON.VPOS flag sets to 1. As with underflow detection, to clear the relevant bit in the Status Monitor Register of the system control block, the software must set the associated bit in the Status Clear Register to 1.

58.3.3.4 Interrupts

The GLCDC provides three interrupt request output signals (GLCDC_L2UNDF, GLCDC_L1UNDF, and GLCDC_VPOS) that correspond to detection of the three status conditions. The GLCDC_L2UNDF, GLCDC_L1UNDF, and GLCDC_VPOS signals are associated with graphics 2 underflow detection, graphics 1 underflow detection, and graphics 2 line detection, respectively. Each of the interrupt request signals is asserted by setting the associated bit in the Interrupt Request Enable Register (SYSCNT_INTEN) to 1. Detecting the status and enabling the associated interrupt request can be controlled separately. Even if detection is enabled, the interrupt request signal is not asserted unless the interrupt request output signal is enabled. In addition, if the Status Monitor Register (SYSCNT_STMON) clears while the interrupt request output signal is asserted (the associated bit in the Status Clear Register (SYSCNT_STCLR) is set to 1), or if the associated bit in the Interrupt Request Enable Register (SYSCNT_INTEN) is cleared to 0, the interrupt request signal is negated. The interrupt request signal generation circuit is configured as shown in Figure 58.28. This circuit is glitch-free except for reset-induced glitches.

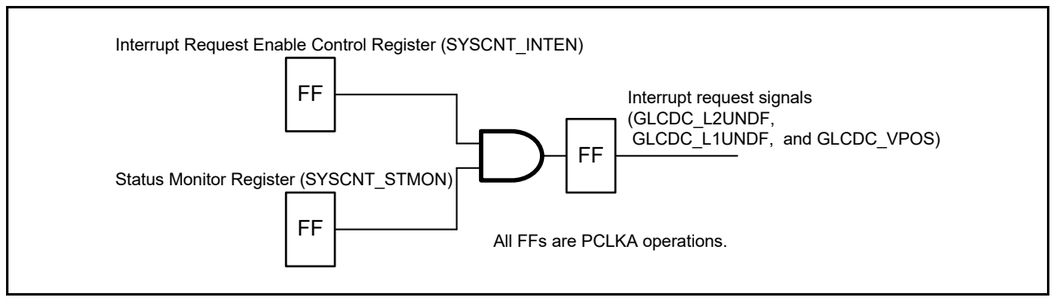


Figure 58.28 Interrupt request signal generation circuit

58.3.3.2 图形1下溢检测

此函数检测图形1的图形数据接口块中的下溢。如果无法从图形数据接口块中读取图形数据（如果有效数据未存储在4级环形缓冲区中，则SYSCNT_STMON.L1UNDF标志设置为1）。在前一阶段的VS（垂直同步）信号断言上，下溢作为图形1的内部状态被清除。但是，要清除系统控制块的状态监视器寄存器中的相关位，软件必须将状态清除寄存器中的相关位设置为1。

58.3.3.3 图形2线检测

此函数检测到在GR2_CLUTINT.LINE[10:0]位中指定的行数已被处理。检测是在前一阶段的HS（水平同步）信号断言上执行的，而不是在开始处理有效像素时执行的。每次检测到的线数达到为图形2指定的值时，SYSCNT_STMON.VPOS标志设置为1。与下溢检测一样，清除状态监视器中的相关位

系统控制块的寄存器，软件必须将状态清除寄存器中的相关位设置为1。

58.3.3.4 Interrupts

GLCDC提供三个中断请求输出信号（GLCDC_L2UNDF、GLCDC_L1UNDF和GLCDC_VPOS)对应于三种状态条件的检测。GLCDC_L2UNDF、GLCDC_L1UNDF和GLCDC_VPOS信号分别与图形2下溢检测、图形1下溢检测和图形2线检测相关联。每个中断请求信号通过将中断请求使能寄存器(SYSCNT_INTEN)中的相关位设置为1来置位。检测状态和启用相关中断请求可以单独控制。即使使能检测，除非使能中断请求输出信号，否则不会断言中断请求信号。此外，如果状态监视器寄存器(SYSCNT_STMON)在中断请求输出信号有效时清除（状态清除寄存器(SYSCNT_STCLR)中的相关位设置为1），或者如果中断请求使能寄存器中的相关位(SYSCNT_INTEN)清零，中断请求信号无效。中断请求信号发生电路的结构如图58.28所示。除了复位引起的毛刺外，该电路没有毛刺。

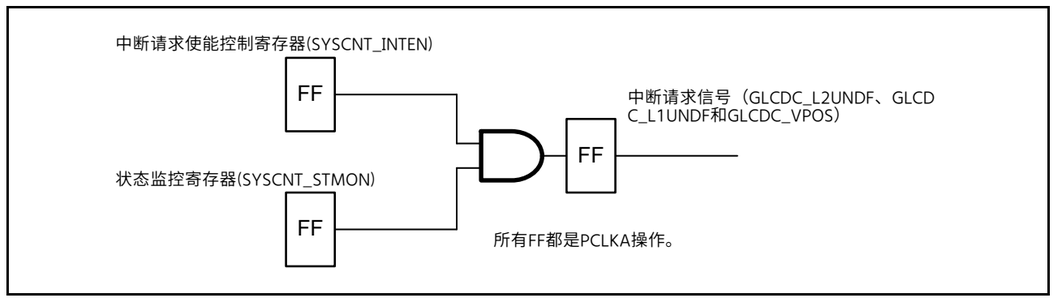


Figure 58.28 中断请求信号发生电路

59. Internal Voltage Regulator

59.1 Overview

The MCU includes a linear regulator (LDO) that supplies voltage to the internal circuits and memory except for I/O, analog, USB, and battery backup power domain.

59.2 Operation

Table 59.1 lists the setting descriptions for the LDO mode pins, and Figure 59.1 shows the LDO mode settings. In LDO mode, the internal voltage is generated from VCC.

Table 59.1 Setting descriptions for the LDO mode pins

Parameter	Description
All VCC pins	• Connect each pin to the system power supply. • Connect each pin to VSS through a 0.1-µF multilayer ceramic capacitor. Place the capacitor close to the pin.
VCL and VCL0 pins	Connect each pin to VSS through a 0.1-µF multilayer ceramic capacitor. Place the capacitor close to the pin.

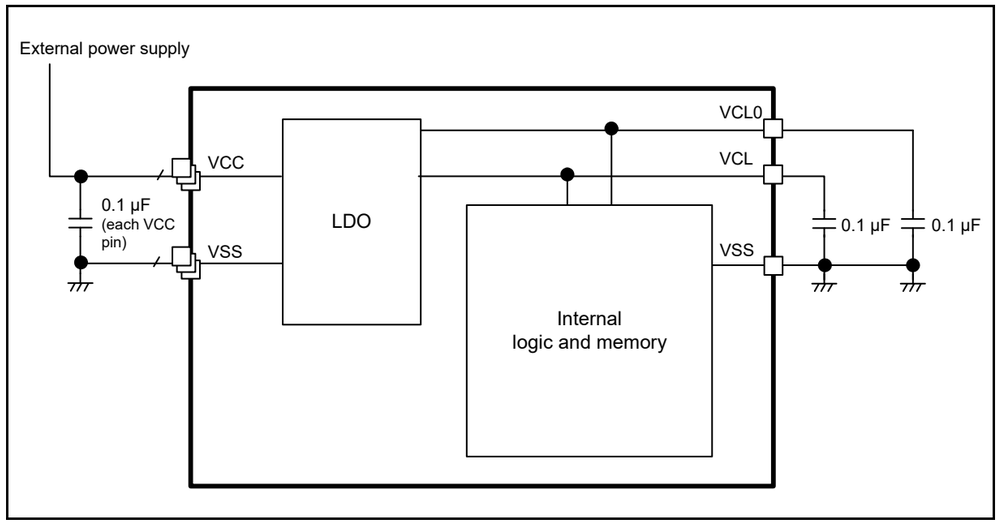


Figure 59.1 LDO mode settings

59. 内部稳压器

59.1 Overview

MCU包含一个线性稳压器(LDO)，可为除IO、模拟、USB和电池备用电源域之外的内部电路和存储器提供电压。

59.2 Operation

表59.1列出了LDO模式引脚的设置说明，图59.1显示了LDO模式设置。在LDO模式下，内部电压由VCC产生。

Table 59.1 LDO模式引脚的设置说明

Parameter	Description
所有VCC引脚	将每个引脚连接到系统电源。 通过一个0.1µF多层陶瓷电容器将每个引脚连接到VSS。将电容器靠近引脚放置。
VCL和VCL0引脚	通过一个0.1µF多层陶瓷电容器将每个引脚连接到VSS。将电容器靠近引脚放置。

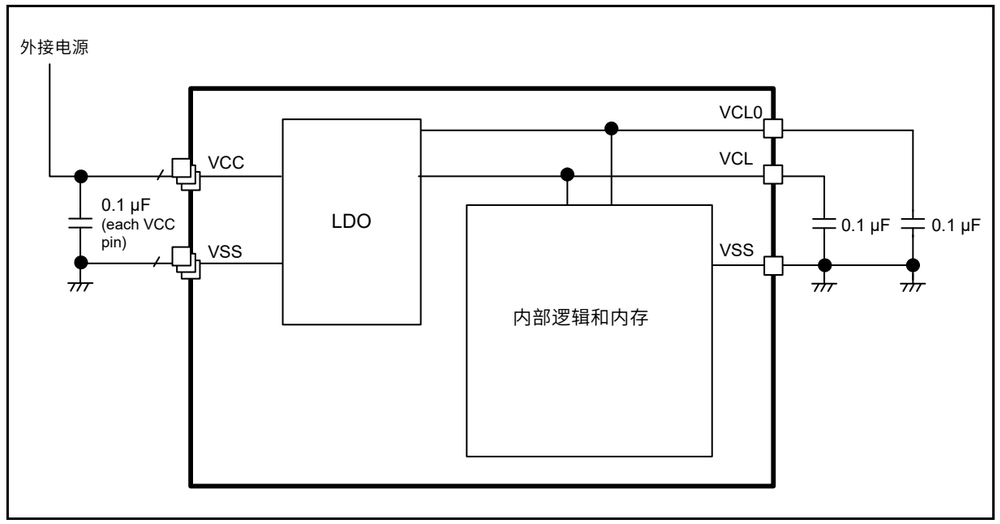


Figure 59.1 LDO模式设置

60. Electrical Characteristics

Unless otherwise specified, the electrical characteristics of the MCU are defined under the following conditions:

VCC = AVCC0 = VCC_USB = VBATT = 2.7 to 3.6 V, 2.7 ≤ VREFH0/VREFH ≤ AVCC0, VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V, VSS = AVSS0 = VREFL0/VREFL = VSS_USB = VSS1_USBHS = VSS2_USBHS = PVSS_USBHS = AVSS_USBHS = 0 V, Ta = Topr.

Figure 60.1 shows the timing conditions.

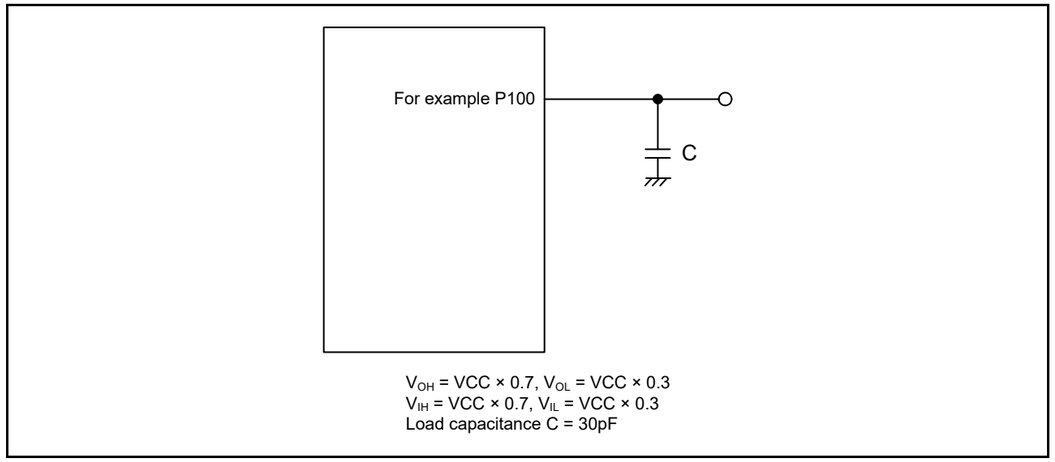


Figure 60.1 Input or output timing measurement conditions

The measurement conditions of timing specification in each peripherals are recommended for the best peripheral operation, however make sure to adjust driving abilities of each pins to meet your conditions.

60.1 Absolute Maximum Ratings

Table 60.1 Absolute maximum ratings

Parameter	Symbol	Value	Unit
Power supply voltage	VCC, VCC_USB *2	-0.3 to +4.0	V
VBATT power supply voltage	VBATT	-0.3 to +4.0	V
Input voltage (except for 5V-tolerant ports*1)	V_{in}	-0.3 to VCC + 0.3	V
Input voltage (5V-tolerant ports*1)	V_{in}	-0.3 to + VCC + 4.0 (max 5.8)	V
Reference power supply voltage	VREFH/VREFH0	-0.3 to AVCC0 + 0.3	V
Analog power supply voltage	AVCC0 *2	-0.3 to +4.0	V
USBHS power supply voltage	VCC_USBHS	-0.3 to +4.0	V
USBHS analog power supply voltage	AVCC_USBHS	-0.3 to +4.0	V
Analog input voltage (except for P000 to P007)	V_{AN}	-0.3 to AVCC0 + 0.3	V
Analog input voltage (P000 to P007) when PGA differential input is disabled	V_{AN}	-0.3 to AVCC0 + 0.3	V
Analog input voltage (P000 to P002, P004 to P006) when PGA differential input is enabled	V_{AN}	-1.3 to AVCC0 + 0.3	V
Analog input voltage (P003, P007) when PGA differential input is enabled	V_{AN}	-0.8 to AVCC0 + 0.3	V
Operating temperature*3,*4,*5	T_{opr}	-40 to +85 -40 to +105	°C
Storage temperature	T_{stg}	-55 to +125	°C

60. 电气特性

除非另有规定，MCU的电气特性在以下条件下定义：

VCC = AVCC0 = VCC_USB = VBATT = 2.7 to 3.6 V, 2.7 ≤ VREFH0/VREFH ≤ AVCC0, VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V, VSS = AVSS0 = VREFL0/VREFL = VSS_USB = VSS1_USBHS = VSS2_USBHS = PVSS_USBHS = AVSS_USBHS = 0 V, Ta = Topr.

图60.1显示了时序条件。

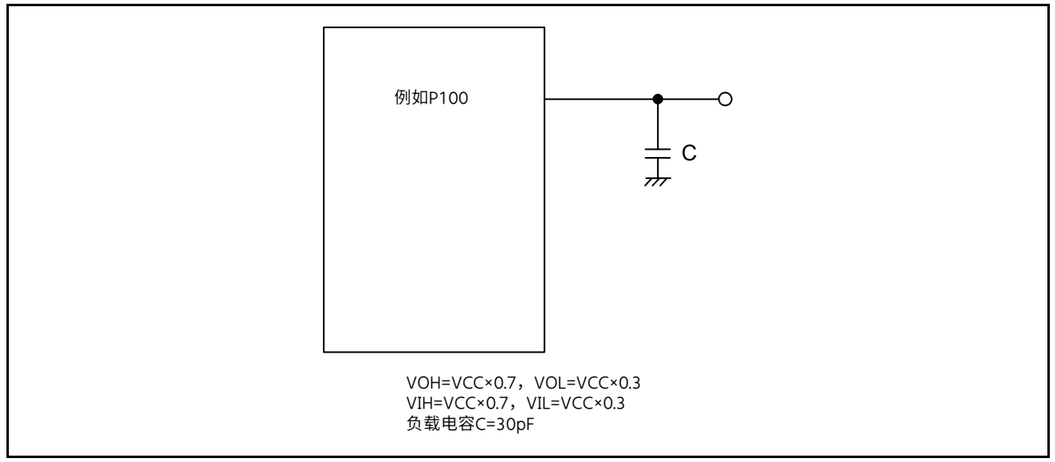


Figure 60.1 输入或输出定时测量条件

每个外设的时序规范的测量条件是推荐的，以获得最佳的外设操作，但请确保调整每个引脚的驱动能力以满足您的条件。

60.1 绝对最大额定值

Table 60.1 绝对最大额定值

Parameter	Symbol	Value	Unit
电源电压	VCC, VCC_USB *2	-0.3 to +4.0	V
VBATT电源电压	VBATT	-0.3 to +4.0	V
输入电压（5V耐受端口除外*1）	V_{in}	-0.3 to VCC + 0.3	V
输入电压（5V容限端口*1）	V_{in}	-0.3 to + VCC + 4.0 (max 5.8)	V
参考电源电压	VREFH/VREFH0	-0.3 to AVCC0 + 0.3	V
模拟电源电压	AVCC0 *2	-0.3 to +4.0	V
USBHS电源电压	VCC_USBHS	-0.3 to +4.0	V
USBHS模拟电源电压	AVCC_USBHS	-0.3 to +4.0	V
模拟输入电压（P000至P007除外）	V_{AN}	-0.3 to AVCC0 + 0.3	V
PGA差分输入禁用时的模拟输入电压（P000至P007）	V_{AN}	-0.3 to AVCC0 + 0.3	V
启用PGA差分输入时的模拟输入电压（P000至P002、P004至P006）	V_{AN}	-1.3 to AVCC0 + 0.3	V
PGA差分输入启用时的模拟输入电压(P003 P007)	V_{AN}	-0.8 to AVCC0 + 0.3	V
Operating temperature*3,*4,*5	T_{opr}	-40 to +85 -40 to +105	°C
贮存温度	T_{stg}	-55 to +125	°C

Caution: Permanent damage to the MCU might result if absolute maximum ratings are exceeded.

Note 1. Ports P205, P206, P400, P401, P407 to P415, P511, P512, P708 to P713, and PB01 are 5V-tolerant.
Note 2. Connect AVCC0 and VCC_USB to VCC.
Note 3. See section 60.2.1, T_j/T_a Definition.
Note 4. Contact a Renesas Electronics sales office for information on derating operation when T_a = +85°C to +105°C. Derating is the systematic reduction of load for improved reliability.
Note 5. The upper limit of operating temperature is 85°C or 105°C, depending on the product. For details, see section 1.3, Part Numbering.

Table 60.2 Recommended operating conditions

Parameter	Symbol	Value	Min	Typ	Max	Unit
Power supply voltages	VCC	When USB/SDRAM is not used	2.7	-	3.6	V
		When USB/SDRAM is used	3.0	-	3.6	V
	VSS		-	0	-	V
USB power supply voltages	VCC_USB, VCC_USBHS		-	VCC	-	V
	VSS_USB, AVSS_USBHS, PVSS_USBHS, VSS1_USBHS, VSS2_USBHS		-	0	-	V
VBATT power supply voltage	VBATT		1.8	-	3.6	V
Analog power supply voltages	AVCC0*1		-	VCC	-	V
	AVSS0		-	0	-	V

Note 1. Connect AVCC0 to VCC. When neither the A/D converter nor the D/A converter nor the comparator is in use, do not leave the AVCC0, VREFH/VREFH0, AVSS0, and VREFL/VREFL0 pins open. Connect the AVCC0 and VREFH/VREFH0 pins to VCC, and the AVSS0 and VREFL/VREFL0 pins to VSS, respectively.

60.2 DC Characteristics

60.2.1 T_j/T_a Definition

Table 60.3 DC characteristics
Conditions: Products with operating temperature (T_a) -40 to +105°C

Parameter	Symbol	Typ	Max	Unit	Test conditions
Permissible junction temperature	T_j	-	125	°C	High-speed mode Low-speed mode Subosc-speed mode
			105*1		

Note: Make sure that $T_j = T_a + \theta ja \times$ total power consumption (W), where total power consumption = $(VCC - V_{OH}) \times \Sigma I_{OH} + V_{OL} \times \Sigma I_{OL} + I_{CC}max \times VCC$.
Note 1. The upper limit of operating temperature is 85°C or 105°C, depending on the product. For details, see section 1.3, Part Numbering. If the part number shows the operation temperature to 85°C, then Tj max is 105°C, otherwise, 125°C.

Caution: 如果超过绝对最大额定值，可能会对MCU造成永久性损坏。

Note 1. 端口P205、P206、P400、P401、P407至P415、P511、P512、P708至P713和PB01可承受5V。
Note 2. 将AVCC0和VCC_USB连接到VCC。
Note 3. 请参阅第60.2.1节，TjTa定义。
Note 4. 有关在Ta=+85°C至+105°C时降额运行的信息，请联系瑞萨电子销售办事处。降额是系统地减少负载以提高可靠性。
Note 5. 工作温度上限为85°C或105°C，具体取决于产品。有关详细信息，请参阅第1.3节，部分Numbering.

Table 60.2 推荐工作条件

Parameter	Symbol	Value	Min	Typ	Max	Unit
电源电压	VCC	不使用USBSDRAM时	2.7	-	3.6	V
		使用USBSDRAM时	3.0	-	3.6	V
	VSS		-	0	-	V
USB电源电压	VCC_USB, VCC_USBHS		-	VCC	-	V
	VSS_USB, AVSS_USBHS, PVSS_USBHS, VSS1_USBHS, VSS2_USBHS		-	0	-	V
VBATT电源电压	VBATT		1.8	-	3.6	V
模拟电源电压	AVCC0*1		-	VCC	-	V
	AVSS0		-	0	-	V

Note 1. 将AVCC0连接到VCC。当AD转换器、DA转换器和比较器均未使用时，请勿将AVCC0、VREFHVREFH0、AVSS0和VREFLVREFL0引脚悬空。将AVCC0和VREFHVREFH0引脚分别连接到VCC，将AVSS0和VREFLVREFL0引脚分别连接到VSS。

60.2 DC Characteristics

60.2.1 T_j/T_a Definition

Table 60.3 DC characteristics
条件：工作温度(Ta)−40至+105°C的产品

Parameter	Symbol	Typ	Max	Unit	测试条件
允许结温	T_j	-	125	°C	High-speed mode Low-speed mode Subosc-speed mode
			105*1		

Note: 确保Tj=Ta+θja×总功耗(W)，其中总功耗=(VCCVOH)×ΣIOH+VOL×ΣIOL+ICCmax×VCC。
Note 1. 工作温度上限为85°C或105°C，具体取决于产品。有关详细信息，请参阅第1.3节，部分编号。如果部件号显示工作温度为85°C，则Tjmax为105°C，否则为125°C。

60.2.2 I/O V_{IH}, V_{IL}

Table 60.4 I/O V_{IH}, V_{IL}

Parameter				Symbol	Min	Typ	Max	Unit
Input voltage (except for Schmitt trigger input pins)	Peripheral function pin	EXTAL(external clock input), WAIT, SPI (except RSPCK)		V_{IH}	VCC × 0.8	-	-	V
				V_{IL}	-	-	VCC × 0.2	
		D00 to D15, DQ00 to DQ15		V_{IH}	VCC × 0.7	-	-	
				V_{IL}	-	-	VCC × 0.3	
		ETHERC		V_{IH}	2.3	-	-	
				V_{IL}	-	-	VCC × 0.2	
		IIC (SMBus)*1		V_{IH}	2.1	-	-	
				V_{IL}	-	-	0.8	
		IIC (SMBus)*2		V_{IH}	2.1	-	VCC + 3.6 (max 5.8)	
				V_{IL}	-	-	0.8	
Schmitt trigger input voltage		IIC (except for SMBus)*1		V_{IH}	VCC × 0.7	-	-	
				V_{IL}	-	-	VCC × 0.3	
				ΔV_T	VCC × 0.05	-	-	
		IIC (except for SMBus)*2		V_{IH}	VCC × 0.7	-	VCC + 3.6 (max 5.8)	
				V_{IL}	-	-	VCC × 0.3	
				ΔV_T	VCC × 0.05	-	-	
		5V-tolerant ports*3, *7		V_{IH}	VCC × 0.8	-	VCC + 3.6 (max 5.8)	
				V_{IL}	-	-	VCC × 0.2	
				ΔV_T	VCC × 0.05	-	-	
		RTCIC0, RTCIC1, RTCIC2	When using the Battery Backup Function	When VBATT power supply is selected	V_{IH}	V_{BATT} × 0.8	-	V_{BATT} + 0.3
					V_{IL}	-	-	V_{BATT} × 0.2
					ΔV_T	V_{BATT} × 0.05	-	-
				When VCC power supply is selected	V_{IH}	VCC × 0.8	-	Higher voltage either VCC + 0.3 V or V_{BATT} + 0.3 V
					V_{IL}	-	-	VCC × 0.2
					ΔV_T	VCC × 0.05	-	-
			When not using the Battery Backup Function		V_{IH}	VCC × 0.8	-	VCC + 0.3
					V_{IL}	-	-	VCC × 0.2
					ΔV_T	VCC × 0.05	-	-
		Other input pins*4			V_{IH}	VCC × 0.8	-	-
					V_{IL}	-	-	VCC × 0.2
					ΔV_T	VCC × 0.05	-	-
	Ports	5V-tolerant ports*5, *7			V_{IH}	VCC × 0.8	-	VCC + 3.6 (max 5.8)
					V_{IL}	-	-	VCC × 0.2
		Other input pins*6			V_{IH}	VCC × 0.8	-	-
					V_{IL}	-	-	VCC × 0.2

Note 1. SCL0_B (P204), SCL1_B, SDA1_B (total 3 pins).
Note 2. SCL0_A, SDA0_A, SCL0_B (P408), SDA0_B, SCL1_A, SDA1_A, SCL2, SDA2 (total 8 pins).
Note 3. RES and peripheral function pins associated with P205, P206, P400, P401, P407 to P415, P511, P512, P708 to P713, PB01 (total 23 pins).

60.2.2 IOVIH

Table 60.4 IOVIH

Parameter				Symbol	Min	Typ	Max	Unit
输入电压（施密特触发器输入引脚除外）	外设功能引脚	EXTAL（外部时钟输入）、WAIT、SPI（除RSPCK）		V_{IH}	VCC × 0.8	-	-	V
				V_{IL}	-	-	VCC × 0.2	
		D00 to D15, DQ00 to DQ15		V_{IH}	VCC × 0.7	-	-	
				V_{IL}	-	-	VCC × 0.3	
		ETHERC		V_{IH}	2.3	-	-	
				V_{IL}	-	-	VCC × 0.2	
		IIC (SMBus)*1		V_{IH}	2.1	-	-	
				V_{IL}	-	-	0.8	
		IIC (SMBus)*2		V_{IH}	2.1	-	VCC + 3.6 (max 5.8)	
				V_{IL}	-	-	0.8	
施密特触发器输入电压		IIC (except for SMBus)*1		V_{IH}	VCC × 0.7	-	-	
				V_{IL}	-	-	VCC × 0.3	
				ΔV_T	VCC × 0.05	-	-	
		IIC (except for SMBus)*2		V_{IH}	VCC × 0.7	-	VCC + 3.6 (max 5.8)	
				V_{IL}	-	-	VCC × 0.3	
				ΔV_T	VCC × 0.05	-	-	
		5V-tolerant ports*3, *7		V_{IH}	VCC × 0.8	-	VCC + 3.6 (max 5.8)	
				V_{IL}	-	-	VCC × 0.2	
				ΔV_T	VCC × 0.05	-	-	
		RTCIC0, RTCIC1, RTCIC2	使用备用电池时 Function	选择VBATT电源时	V_{IH}	V_{BATT} × 0.8	-	V_{BATT} + 0.3
					V_{IL}	-	-	V_{BATT} × 0.2
					ΔV_T	V_{BATT} × 0.05	-	-
				选择VCC电源时	V_{IH}	VCC × 0.8	-	更高的电压VCC+0.3V或VBATT+0.3V
					V_{IL}	-	-	VCC × 0.2
					ΔV_T	VCC × 0.05	-	-
			不使用备用电池时 Function		V_{IH}	VCC × 0.8	-	VCC + 0.3
					V_{IL}	-	-	VCC × 0.2
					ΔV_T	VCC × 0.05	-	-
		其他输入引脚*4			V_{IH}	VCC × 0.8	-	-
					V_{IL}	-	-	VCC × 0.2
					ΔV_T	VCC × 0.05	-	-
	Ports	5V-tolerant ports*5, *7			V_{IH}	VCC × 0.8	-	VCC + 3.6 (max 5.8)
					V_{IL}	-	-	VCC × 0.2
		其他输入引脚*6			V_{IH}	VCC × 0.8	-	-
					V_{IL}	-	-	VCC × 0.2

Note 1. SCL0_B (P204), SCL1_B, SDA1_B (total 3 pins).
Note 2. SCL0_A, SDA0_A, SCL0_B (P408), SDA0_B, SCL1_A, SDA1_A, SCL2, SDA2 (total 8 pins).
Note 3. RES和与P205、P206、P400、P401、P407至P415、P511、P512、P708至P713、PB01相关的外围功能引脚（共23个引脚）。

Note 4. All input pins except for the peripheral function pins already described in the table.
Note 5. P205, P206, P400, P401, P407 to P415, P511, P512, P708 to P713, PB01 (total 22 pins).
Note 6. All input pins except for the ports already described in the table.
Note 7. When VCC is less than 2.7 V, the input voltage of 5 V-tolerant ports should be less than 3.6 V, otherwise breakdown might occur because the 5 V-tolerant ports are electrically controlled to not violate the breakdown voltage.

60.2.3 I/O I_{OH}, I_{OL}

Table 60.5 I/O I_{OH}, I_{OL}

Parameter			Symbol	Min	Typ	Max	Unit
Permissible output current (average value per pin)	Ports P008 to P010, P201	-	I_{OH}	-	--	-2.0	mA
			I_{OL}	-	-	2.0	mA
	Ports P014, P015	-	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
	Ports P205, P206, P407 to P415, P602, P708 to P713, PB01 (total 19 pins)	Low drive*1	I_{OH}	-	-	-2.0	mA
			I_{OL}	-	-	2.0	mA
		Middle drive*2	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
		High drive*3	I_{OH}	-	-	-20	mA
			I_{OL}	-	-	20	mA
	Other output pins*4	Low drive*1	I_{OH}	-	-	-2.0	mA
			I_{OL}	-	-	2.0	mA
		Middle drive*2	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
		High drive*3	I_{OH}	-	-	-16	mA
			I_{OL}	-	-	16	mA
Permissible output current (max value per pin)	Ports P008 to P010, P201	-	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
	Ports P014, P015	-	I_{OH}	-	-	-8.0	mA
			I_{OL}	-	-	8.0	mA
	Ports P205, P206, P407 to P415, P602, P708 to P713, PB01 (total 19 pins)	Low drive*1	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
		Middle drive*2	I_{OH}	-	-	-8.0	mA
			I_{OL}	-	-	8.0	mA
		High drive*3	I_{OH}	-	-	-40	mA
			I_{OL}	-	-	40	mA
	Other output pins*4	Low drive*1	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
		Middle drive*2	I_{OH}	-	-	-8.0	mA
			I_{OL}	-	-	8.0	mA
		High drive*3	I_{OH}	-	-	-32	mA
			I_{OL}	-	-	32	mA
Permissible output current (max value total pins)	Maximum of all output pins		ΣI_{OH} (max)	-	-	-80	mA
			ΣI_{OL} (max)	-	-	80	mA

Caution: To protect the reliability of the MCU, the output current values should not exceed the values in this table. The average output current indicates the average value of current measured during 100 µs.

Note 1. This is the value when low driving ability is selected in the port drive capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.
Note 2. This is the value when middle driving ability is selected in the port drive capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.
Note 3. This is the value when high driving ability is selected in the port drive capability bit in the PmnPFS register. The selected driving ability is retained in Deep Software Standby mode.

Note 4. 除表中已描述的外围功能引脚外的所有输入引脚。
Note 5. P205, P206, P400, P401, P407 to P415, P511, P512, P708 to P713, PB01 (total 22 pins).
Note 6. 除表中已描述的端口外的所有输入引脚。
Note 7. 当VCC小于2.7V时，耐5V端口的输入电压应小于3.6V，否则可能发生击穿，因为5V耐压端口被电控不超过击穿电压。

60.2.3 我爱我哦

Table 60.5 我爱我哦

Parameter			Symbol	Min	Typ	Max	Unit
允许输出电流（每个引脚的平均值）	端口P008至P010、P201	-	I_{OH}	-	--	-2.0	mA
			I_{OL}	-	-	2.0	mA
	Ports P014, P015	-	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
	端口P205、P206、P407至P415、P602、P708至P713、PB01（共19针）	低驱*1	I_{OH}	-	-	-2.0	mA
			I_{OL}	-	-	2.0	mA
		中驱*2	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
		高驱*3	I_{OH}	-	-	-20	mA
			I_{OL}	-	-	20	mA
	其他输出引脚*4	低驱*1	I_{OH}	-	-	-2.0	mA
			I_{OL}	-	-	2.0	mA
		中驱*2	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
		高驱*3	I_{OH}	-	-	-16	mA
			I_{OL}	-	-	16	mA
允许输出电流（每个引脚的最大值）	端口P008至P010、P201	-	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
	Ports P014, P015	-	I_{OH}	-	-	-8.0	mA
			I_{OL}	-	-	8.0	mA
	端口P205、P206、P407至P415、P602, P708 to P713, PB01 (total 19 pins)	低驱*1	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
		中驱*2	I_{OH}	-	-	-8.0	mA
			I_{OL}	-	-	8.0	mA
		高驱*3	I_{OH}	-	-	-40	mA
			I_{OL}	-	-	40	mA
	其他输出引脚*4	低驱*1	I_{OH}	-	-	-4.0	mA
			I_{OL}	-	-	4.0	mA
		中驱*2	I_{OH}	-	-	-8.0	mA
			I_{OL}	-	-	8.0	mA
		高驱*3	I_{OH}	-	-	-32	mA
			I_{OL}	-	-	32	mA
允许输出电流（最大总引脚数）	所有输出引脚的最大值		ΣI_{OH} (max)	-	-	-80	mA
			ΣI_{OL} (max)	-	-	80	mA

Caution: 为保护单片机的可靠性，输出电流值不应超过此表中的值。平均输出电流是指在100µs内测得的电流平均值。

Note 1. 这是在PmnPFS寄存器的端口驱动能力位中选择低驱动能力时的值。在深度软件待机模式下会保留所选的驾驶能力。
Note 2. 这是在PmnPFS寄存器的端口驱动能力位中选择中等驱动能力时的值。在深度软件待机模式下会保留所选的驾驶能力。
Note 3. 这是在PmnPFS寄存器的端口驱动能力位中选择高驱动能力时的值。在深度软件待机模式下会保留所选的驾驶能力。

Note 4. Except for P000 to P007, P200, which are input ports.

60.2.4 I/O V_{OH}, V_{OL}, and Other Characteristics

Table 60.6 I/O V_{OH}, V_{OL}, and other characteristics

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Output voltage	IIC		V_{OL}	-	-	0.4	V	I_{OL} = 3.0 mA
			V_{OL}	-	-	0.6		I_{OL} = 6.0 mA
	IIC*1		V_{OL}	-	-	0.4		I_{OL} = 15.0 mA (ICFER.FMPE = 1)
			V_{OL}	-	0.4	-		I_{OL} = 20.0 mA (ICFER.FMPE = 1)
	ETHERC		V_{OH}	VCC - 0.5	-	-		I_{OH} = -1.0 mA
			V_{OL}	-	-	0.4		I_{OL} = 1.0 mA
	Ports P205, P206, P407 to P415, P602, P708 to P713, PB01 (total 19 pins)*2		V_{OH}	VCC - 1.0	-	-		I_{OH} = -20 mA VCC = 3.3 V
			V_{OL}	-	-	1.0		I_{OL} = 20 mA VCC = 3.3 V
	Other output pins		V_{OH}	VCC - 0.5	-	-		I_{OH} = -1.0 mA
			V_{OL}	-	-	0.5		I_{OL} = 1.0 mA
Input leakage current	RES		$\|I_{in}\|$	-	-	5.0	μA	V_{in} = 0 V V_{in} = 5.5 V
	Ports P000 to P002, P004 to P006, P200			-	-	1.0		V_{in} = 0 V V_{in} = VCC
	Ports P003, P007	Before initialization*3		-	-	45.0		V_{in} = 0 V V_{in} = VCC
		After initialization*4		-	-	1.0		V_{in} = 0 V V_{in} = VCC
Three-state leakage current (off state)	5V-tolerant ports		$\|I_{TSI}\|$	-	-	5.0	μA	V_{in} = 0 V V_{in} = 5.5 V
	Other ports (except for ports P000 to P007, P200)			-	-	1.0		V_{in} = 0 V V_{in} = VCC
Input pull-up MOS current	Ports P0 to PB (except for ports P000 to P007)		I_p	-300	-	-10	μA	VCC = 2.7 to 3.6 V V_{in} = 0 V
Input capacitance	USB_DP, USB_DM, and ports P003, P007, P014, P015, P400, P401, P511, P512		C_{in}	-	-	16	pF	Vbias = 0V Vamp = 20mV f = 1 MHz T_a = 25°C
	Other input pins			-	-	8		

Note 1. SCL0_A, SDA0_A (total 2 pins).
Note 2. This is the value when high driving ability is selected in the port drive capability bit in the PmnPFS register.
The selected driving ability is retained in Deep Software Standby mode.
Note 3. P0nPFS.ASEL (n = 3 or 7) = 1.
Note 4. P0nPFS.ASEL (n = 3 or 7) = 0.

Note 4. 除了P000至P007、P200为输入端口。

60.2.4 IOVOH VOL和其他特性

Table 60.6 IOVOH、VOL和其他特性

Parameter			Symbol	Min	Typ	Max	Unit	测试条件
输出电压	IIC		V_{OL}	-	-	0.4	V	我OL=3.0毫安
			V_{OL}	-	-	0.6		我OL=6.0毫安
	IIC*1		V_{OL}	-	-	0.4		IOL=15.0mA(ICFER.FMPE=1)
			V_{OL}	-	0.4	-		IOL=20.0mA(ICFER.FMPE=1)
	ETHERC		V_{OH}	VCC - 0.5	-	-		IOH=-1.0毫安
			V_{OL}	-	-	0.4		我OL=1.0毫安
	端口P205、P206、P407至P415、P602, P708 to P713, PB01 (total 19 pins)*2		V_{OH}	VCC - 1.0	-	-		我OH=-20毫安VCC=3.3V
			V_{OL}	-	-	1.0		我OL=20毫安VCC=3.3V
	其他输出引脚		V_{OH}	VCC - 0.5	-	-		IOH=-1.0毫安
			V_{OL}	-	-	0.5		我OL=1.0毫安
输入漏电流	RES		$\|I_{in}\|$	-	-	5.0	μA	V_{in} = 0 V V_{in} = 5.5 V
	端口P000至P002、P004至P006、P200			-	-	1.0		V_{in} = 0 V V_{in} = VCC
	Ports P003, P007	Before initialization*3		-	-	45.0		V_{in} = 0 V V_{in} = VCC
		After initialization*4		-	-	1.0		V_{in} = 0 V V_{in} = VCC
三态漏电流（关闭状态）	5V-tolerant ports		$\|I_{TSI}\|$	-	-	5.0	μA	V_{in} = 0 V V_{in} = 5.5 V
	其他端口（端口P000至P007、P200除外）			-	-	1.0		V_{in} = 0 V V_{in} = VCC
输入上拉MOS电流	端口P0到PB（端口除外P000 to P007)		I_p	-300	-	-10	μA	VCC = 2.7 to 3.6 V V_{in} = 0 V
输入电容	USB_DP、USB_DM和端口P003, P007, P014, P015, P400, P401, P511, P512		C_{in}	-	-	16	pF	Vbias = 0V Vamp = 20mV f = 1 MHz T_a = 25°C
	其他输入引脚			-	-	8		

Note 1. SCL0_A, SDA0_A (total 2 pins).
Note 2. 这是在PmnPFS寄存器的端口驱动能力位中选择高驱动能力时的值。
在深度软件待机模式下会保留所选的驾驶能力。
Note 3. P0nPFS.ASEL (n = 3 or 7) = 1.
Note 4. P0nPFS.ASEL (n = 3 or 7) = 0.

60.2.5 Operating and Standby Current

Table 60.7 Operating and standby current (1 of 2)

Parameter				Symbol	Min	Typ	Max	Unit	Test conditions
Supply current*1	High-speed mode	Maximum*2		I_{CC}*3	-	-	137*2	mA	ICLK = 120 MHz PCLKA = 120 MHz*7 PCLKB = 60 MHz PCLKC = 60 MHz PCLKD = 120 MHz FCLK = 60 MHz BCLK = 120 MHz
		CoreMark®*5			-	21	-		
		Normal mode	All peripheral clocks enabled, while (1) code executing from flash*4		-	34	-		
			All peripheral clocks disabled, while (1) code executing from flash*5, *6		-	14	-		
		Sleep mode*5, *6			-	12	46		
		Increase during BGO operation	Data flash P/E		-	6	-		
			Code flash P/E		-	8	-		
	Low-speed mode*5				-	2.4	-		ICLK = 1 MHz
	Subosc-speed mode*5				-	2	-		ICLK = 32.768 kHz
	Software Standby mode				-	1.8	18		Ta ≤ 85°C
					-	1.8	28		Ta ≤ 105°C
	Deep Software Standby mode	Power supplied to Standby SRAM and USB resume detecting unit			-	30	79	µA	Ta ≤ 85°C
					-	30	113	µA	Ta ≤ 105°C
		Power not supplied to SRAM or USB resume detecting unit	Power-on reset circuit low-power function disabled		-	13	33	µA	Ta ≤ 85°C
					-	13	40		Ta ≤ 105°C
			Power-on reset circuit low-power function enabled		-	6.3	28		Ta ≤ 85°C
					-	6.3	34		Ta ≤ 105°C
		Increase when the RTC and AGT are operating	When the low-speed on-chip oscillator (LOCO) is in use		-	5	-		-
			When a crystal oscillator for low clock loads is in use		-	1.0	-		-
			When a crystal oscillator for standard clock loads is in use		-	1.5	-		-
		RTC operating while VCC is off (with the battery backup function, only the RTC and sub-clock oscillator operate)	When a crystal oscillator for low clock loads is in use		-	0.9	-		V_{BATT} = 1.8 V, VCC = 0 V
					-	1.3	-		V_{BATT} = 3.3 V, VCC = 0 V
			When a crystal oscillator for standard clock loads is in use		-	1.1	-		V_{BATT} = 1.8 V, VCC = 0 V
					-	1.8	-		V_{BATT} = 3.3 V, VCC = 0 V
Analog power supply current	During 12-bit A/D conversion			AI_{CC}	-	0.8	1.1	mA	-
	During 12-bit A/D conversion with S/H amp				-	2.3	3.3	mA	-
	PGA (1ch)				-	1	3	mA	-
	ACMPHS (1unit)				-	100	150	µA	-
	Temperature sensor				-	0.1	0.2	mA	-
	During D/A conversion (per unit)		Without AMP output		-	0.1	0.2	mA	-
			With AMP output		-	0.6	1.1	mA	-
	Waiting for A/D, D/A conversion (all units)				-	0.9	1.6	mA	-
	ADC12, DAC12 in standby modes (all units)*8				-	2	8	µA	-
Reference power supply current (VREFH0)	During 12-bit A/D conversion (unit 0)			AI_{REFH0}	-	70	120	µA	-
	Waiting for 12-bit A/D conversion (unit 0)				-	0.07	0.5	µA	-
	ADC12 in standby modes (unit 0)				-	0.07	0.5	µA	-
Reference power supply current (VREFH)	During 12-bit A/D conversion (unit 1)			AI_{REFH}	-	70	120	µA	-
	During D/A conversion (per unit)		Without AMP output		-	0.1	0.4	mA	-
			With AMP ouput		-	0.1	0.4	mA	-
	Waiting for 12-bit A/D (unit 1), D/A (all units) conversion				-	0.07	0.8	µA	-
	ADC12 unit 1 in standby modes				-	0.07	0.8	µA	-

60.2.5 工作和待机电流

Table 60.7 工作和待机电流(1of2)

Parameter				Symbol	Min	Typ	Max	Unit	测试条件
供电电流*1	High-speed mode	Maximum*2		I_{CC}*3	-	-	137*2	mA	ICLK = 120 MHz PCLKA = 120 MHz*7 PCLKB = 60 MHz PCLKC = 60 MHz PCLKD = 120 MHz FCLK = 60 MHz BCLK = 120 MHz
		CoreMark®*5			-	21	-		
		正常模式	启用所有外设时钟，同时(1)代码从闪存执行*4		-	34	-		
			禁用所有外设时钟，同时(1)代码从闪存执行*5、*6		-	14	-		
		睡眠模式*5、*6			-	12	46		
		BGO运行期间增加	数据闪存PE		-	6	-		
			代码闪存PE		-	8	-		
	Low-speed mode*5				-	2.4	-		ICLK = 1 MHz
	Subosc-speed mode*5				-	2	-		ICLK = 32.768 kHz
	软件待机模式				-	1.8	18		Ta ≤ 85°C
					-	1.8	28		Ta ≤ 105°C
	深度软件待机模式	为备用SRAM和USB恢复检测单元供电			-	30	79	µA	Ta ≤ 85°C
					-	30	113	µA	Ta ≤ 105°C
		未向SRAM或USB恢复检测单元供电	上电复位电路低功耗功能禁用		-	13	33	µA	Ta ≤ 85°C
					-	13	40		Ta ≤ 105°C
			上电复位电路低功耗功能启用		-	6.3	28		Ta ≤ 85°C
					-	6.3	34		Ta ≤ 105°C
		RTC和AGT运行时增加	使用低速片上振荡器(LOCO)时		-	5	-		-
			当使用用于低时钟负载的晶体振荡器时		-	1.0	-		-
			当使用标准时钟负载的晶体振荡器时		-	1.5	-		-
		VCC关闭时RTC运行（具有电池备份功能，只有RTC和副时钟振荡器运行）	当使用用于低时钟负载的晶体振荡器时		-	0.9	-		V_{BATT} = 1.8 V, VCC = 0 V
					-	1.3	-		V_{BATT} = 3.3 V, VCC = 0 V
			当使用标准时钟负载的晶体振荡器时		-	1.1	-		V_{BATT} = 1.8 V, VCC = 0 V
					-	1.8	-		V_{BATT} = 3.3 V, VCC = 0 V
模拟电源电流	在12位AD转换期间			AI_{CC}	-	0.8	1.1	mA	-
	在使用SHamp进行12位AD转换期间				-	2.3	3.3	mA	-
	PGA (1ch)				-	1	3	mA	-
	ACMPHS (1unit)				-	100	150	µA	-
	温度感应器				-	0.1	0.2	mA	-
	DA转换期间（每单位）		无AMP输出		-	0.1	0.2	mA	-
			带AMP输出		-	0.6	1.1	mA	-
	等待AD、DA转换（所有单位）				-	0.9	1.6	mA	-
	ADC12、DAC12处于待机模式（所有单元）*8				-	2	8	µA	-
参考电源电流(VREFH0)	在12位AD转换期间（单元0）			AI_{REFH0}	-	70	120	µA	-
	等待12位AD转换（单元0）				-	0.07	0.5	µA	-
	ADC12处于待机模式（单元0）				-	0.07	0.5	µA	-
参考电源电流(VREFH)	在12位AD转换期间（单元1）			AI_{REFH}	-	70	120	µA	-
	DA转换期间（每单位）		无AMP输出		-	0.1	0.4	mA	-
			带AMP输出		-	0.1	0.4	mA	-
	等待12位AD（单元1）、DA（所有单元）转换				-	0.07	0.8	µA	-
	ADC12单元1处于待机模式				-	0.07	0.8	µA	-

Table 60.7 Operating and standby current (2 of 2)

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
USB operating current	Low speed	USB	$I_{CCUSBLS}$	-	3.5	6.5	mA	VCC_USB
		USBHS		-	10.5	13.5	mA	VCC_USBHS = AVCC_USBHS (PHYSET.HSEB = 0)
		USBHS		-	2.8	3.6	mA	VCC_USBHS = AVCC_USBHS (PHYSET.HSEB = 1)
	Full speed	USB	$I_{CCUSBFS}$	-	4.0	10.0	mA	VCC_USB
		USBHS		-	14	22	mA	VCC_USBHS = AVCC_USBHS (PHYSET.HSEB = 0)
		USBHS		-	6.5	13.0	mA	VCC_USBHS = AVCC_USBHS (PHYSET.HSEB = 1)
	High speed	USBHS	$I_{CCUSBHS}$	-	50	65	mA	VCC_USBHS = AVCC_USBHS
	Standby mode (direct power down)	USBHS	$I_{CCUSBSBY}$	-	0.5	4.5	µA	VCC_USBHS = AVCC_USBHS

Note 1. Supply current values are with all output pins unloaded and all input pull-up MOS transistors in the off state.
Note 2. Measured with clocks supplied to the peripheral functions. This does not include the BGO operation.
Note 3. ICC depends on f (ICLK) as follows. (ICLK:PCLKA:PCLKB:PCLKC:PCLKD:BCK:EBCLK = 2:2:1:1:2:1:1)
ICC Max. = 0.84 × f + 37 (max. operation in High-speed mode)
ICC Typ. = 0.09 × f + 3.7 (normal operation in High-speed mode)
ICC Typ. = 0.6 × f + 1.8 (Low-speed mode 1)
ICC Max. = 0.08 × f + 37 (Sleep mode).
Note 4. This does not include the BGO operation.
Note 5. Supply of the clock signal to peripherals is stopped in this state. This does not include the BGO operation.
Note 6. FCLK, BCLK, PCLKA, PCLKB, PCLKC, and PCLKD are set to divided by 64 (3.75 MHz).
Note 7. When using ETHERC, GLCDC, DRW, and JPEG, PCLKA frequency is such that PCLKA = ICLK.
Note 8. When the MCU is in Software Standby mode or the MSTPCRD.MSTPD16 (ADC120 Module Stop bit) and MSTPCRD.MSTPD15 (ADC121 Module Stop bit) are in the module-stop state. See section 47.6.8, Available Functions and Register Settings of AN000 to AN002, AN007, AN100 to AN102, and AN107.

Table 60.7 工作和待机电流(2of2)

Parameter			Symbol	Min	Typ	Max	Unit	测试条件
USB工作电流	低速	USB	$I_{CCUSBLS}$	-	3.5	6.5	mA	VCC_USB
		USBHS		-	10.5	13.5	mA	VCC_USBHS = AVCC_USBHS (PHYSET.HSEB = 0)
		USBHS		-	2.8	3.6	mA	VCC_USBHS = AVCC_USBHS (PHYSET.HSEB = 1)
	全速	USB	$I_{CCUSBFS}$	-	4.0	10.0	mA	VCC_USB
		USBHS		-	14	22	mA	VCC_USBHS = AVCC_USBHS (PHYSET.HSEB = 0)
		USBHS		-	6.5	13.0	mA	VCC_USBHS = AVCC_USBHS (PHYSET.HSEB = 1)
	高速	USBHS	$I_{CCUSBHS}$	-	50	65	mA	VCC_USBHS = AVCC_USBHS
	待机模式（直接断电）	USBHS	$I_{CCUSBSBY}$	-	0.5	4.5	µA	VCC_USBHS = AVCC_USBHS

Note 1. 电源电流值是在所有输出引脚空载且所有输入上拉MOS晶体管处于关闭状态的情况下。
Note 2. 使用提供给外围功能的时钟进行测量。这不包括BGO操作。
Note 3. ICC取决于f(ICLK)，如下所示。（ICLK:PCLKA:PCLKB:PCLKC:PCLKD:BCK:EBCLK=2:2:1:1:2:1:1）
ICC最大值=0.84×f+37（高速模式下的最大操作）
ICC典型值。=0.09×f+3.7（高速模式下的正常操作）
ICC Typ. = 0.6 × f + 1.8 (Low-speed mode 1)
ICC Max. = 0.08 × f + 37 (Sleep mode).
Note 4. 这不包括BGO操作。
Note 5. 在该状态下停止向外围设备提供时钟信号。这不包括BGO操作。
Note 6. FCLK、BCLK、PCLKA、PCLKB、PCLKC和PCLKD设置为64分频(3.75MHz)。
Note 7. 当使用ETHERC、GLCDC、DRW和JPEG时，PCLKA频率使得PCLKA=ICLK。
Note 8. 当MCU处于软件待机模式或MSTPCRD.MSTPD16（ADC120模块停止位）和MSTPCRD.MSTPD15（ADC121模块停止位）处于模块停止状态。请参阅第47.6.8节，可用功能和AN000至AN002、AN007、AN100至AN102和AN107的寄存器设置。

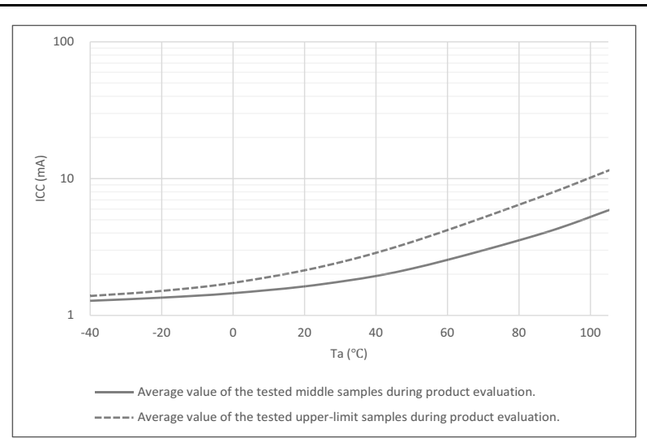


Figure 60.2 Temperature dependency in Software Standby mode (reference data)

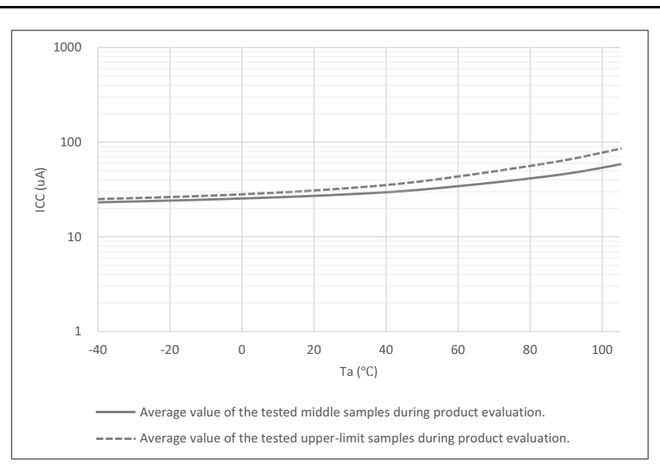


Figure 60.3 Temperature dependency in Deep Software Standby mode, power supplied to standby SRAM and USB resume detecting unit (reference data)

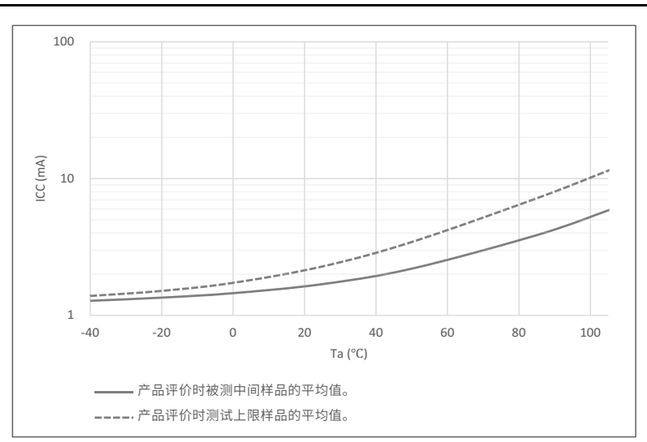


Figure 60.2 软件待机模式下的温度依赖性（参考数据）

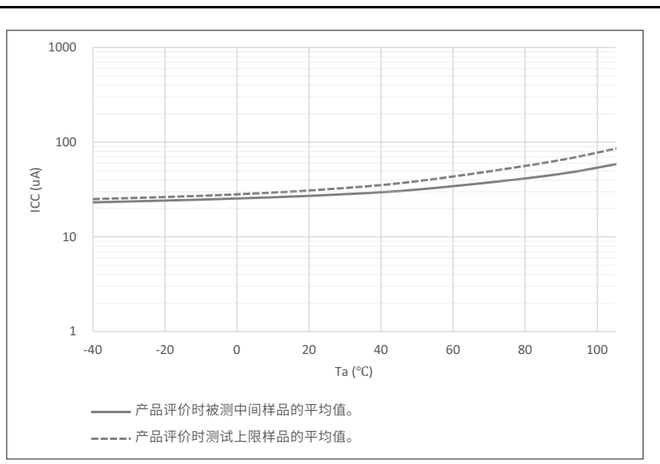


Figure 60.3 深度软件待机模式下的温度依赖性，为待机SRAM供电和USB恢复检测单元（参考数据）

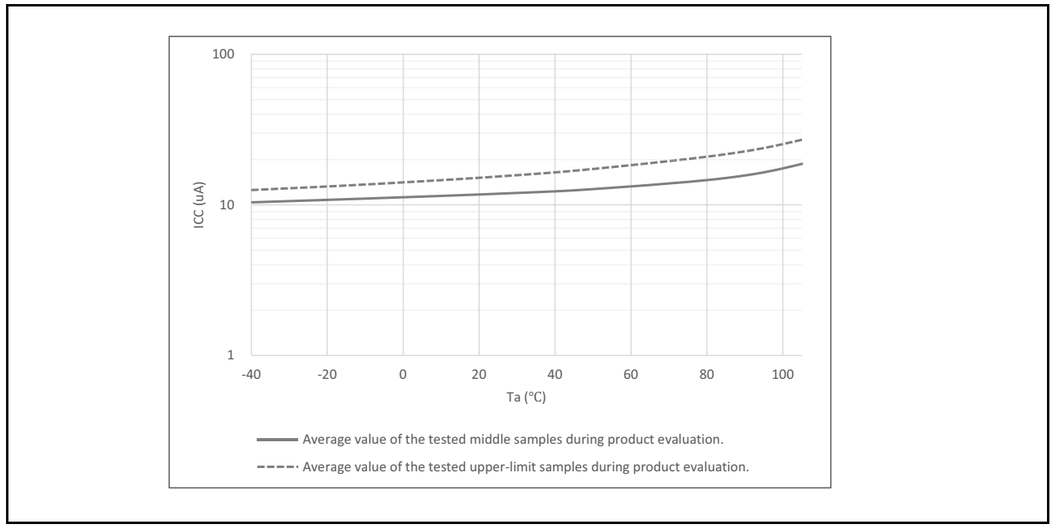


Figure 60.4 Temperature dependency in Deep Software Standby mode, power not supplied to SRAM or USB resume detecting unit, power-on reset circuit low-power function disabled (reference data)

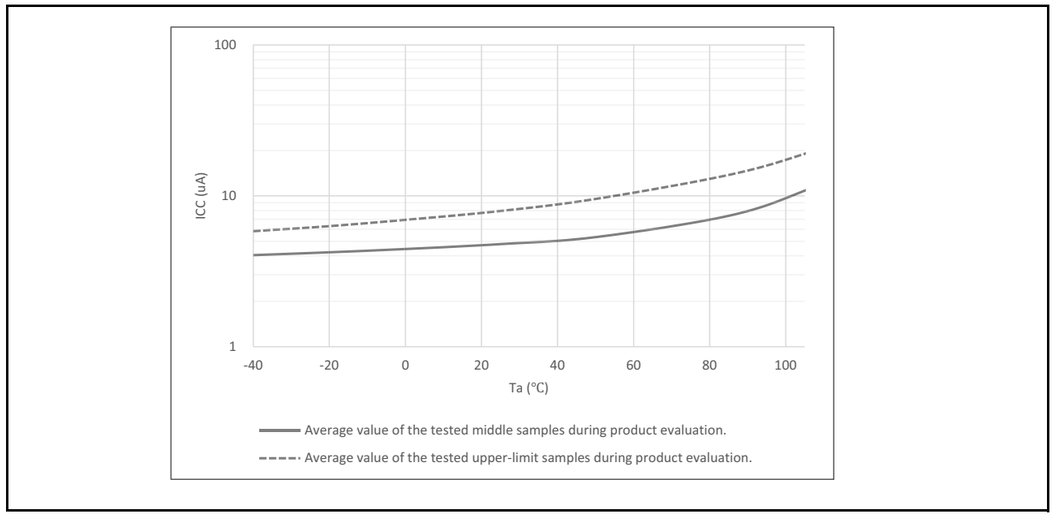


Figure 60.5 Temperature dependency in Deep Software Standby mode, power not supplied to SRAM or USB resume detecting unit, power-on reset circuit low-power function enabled (reference data)

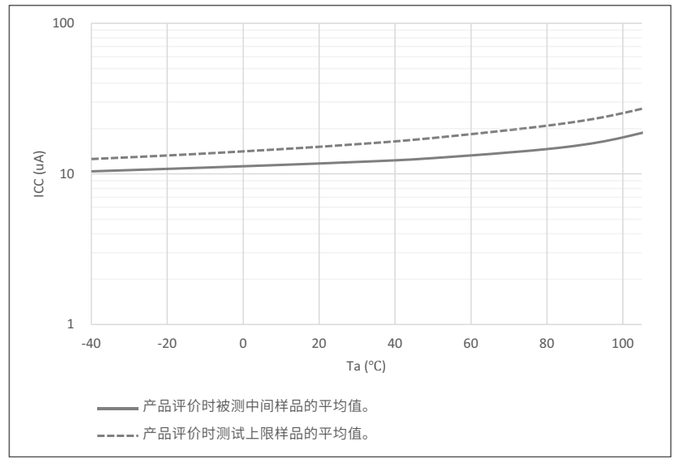


Figure 60.4 深度软件待机模式下的温度依赖性，未向SRAM或USB恢复检测单元供电，上电复位电路低功耗功能禁用（参考数据）

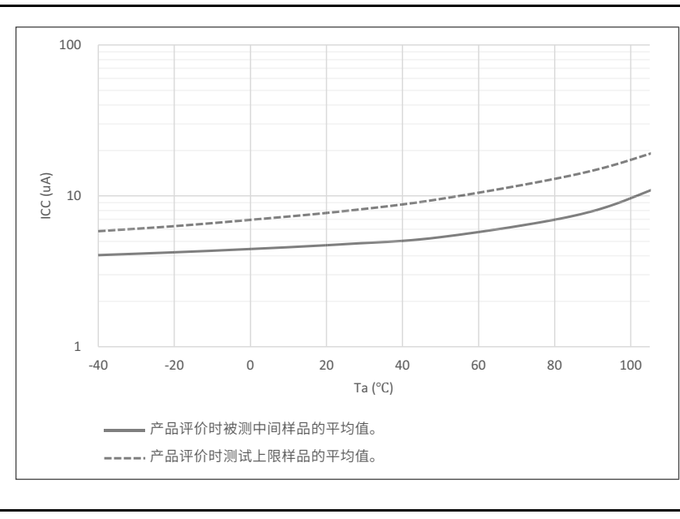


Figure 60.5 深度软件待机模式下的温度依赖性，不向SRAM或USB恢复检测单元供电，启用上电复位电路低功耗功能（参考数据）

60.2.6 VCC Rise and Fall Gradient and Ripple Frequency

Table 60.8 Rise and fall gradient characteristics

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
VCC rising gradient	Voltage monitor 0 reset disabled at startup	SrVCC	0.0084	-	20	ms/V	-
	Voltage monitor 0 reset enabled at startup		0.0084	-	-		-
	SCI/USB boot mode*1		0.0084	-	20		-
VCC falling gradient*2		SfVCC	0.0084	-	-	ms/V	-

Note 1. At boot mode, the reset from voltage monitor 0 is disabled regardless of the value of OFS1.LVDAS bit.
Note 2. This applies when VBATT is used.

Table 60.9 Rise and fall gradient and ripple frequency characteristics
The ripple voltage must meet the allowable ripple frequency $f_{r(VCC)}$ within the range between the VCC upper limit (3.6 V) and lower limit (2.7 V). When the VCC change exceeds VCC ±10%, the allowable voltage change rising and falling gradient dt/dVCC must be met.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Allowable ripple frequency	$f_{r (VCC)}$	-	-	10	kHz	Figure 60.6 $V_{r (VCC)}$ ≤ VCC × 0.2
		-	-	1	MHz	Figure 60.6 $V_{r (VCC)}$ ≤ VCC × 0.08
		-	-	10	MHz	Figure 60.6 $V_{r (VCC)}$ ≤ VCC × 0.06
Allowable voltage change rising and falling gradient	dt/dVCC	1.0	-	-	ms/V	When VCC change exceeds VCC ±10%

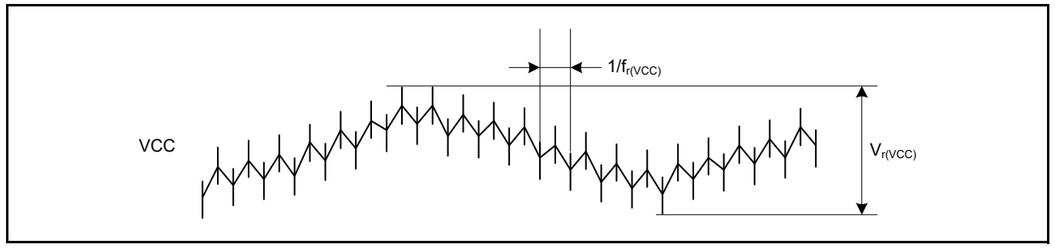


Figure 60.6 Ripple waveform

60.3 AC Characteristics

60.3.1 Frequency

Table 60.10 Operation frequency value in high-speed mode

Parameter			Symbol	Min	Typ	Max	Unit
Operation frequency	System clock (ICLK*2)		f	-	-	120	MHz
	Peripheral module clock (PCLKA)*2			-	-	120	
	Peripheral module clock (PCLKB)*2			-	-	60	
	Peripheral module clock (PCLKC)*2			-*3	-	60	
	Peripheral module clock (PCLKD)*2			-	-	120	
	Flash interface clock (FCLK)*2			-*1	-	60	
	External bus clock (BCLK)*2			-	-	120	
	EBCLK pin output			-	-	60	
	SDCLK pin output	VCC ≥ 3.0 V		-	-	120	

60.2.6 VCC上升和下降梯度和纹波频率

Table 60.8 上升和下降梯度特性

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
VCC上升梯度	启动时禁用电压监视器0复位	SrVCC	0.0084	-	20	ms/V	-
	启动时启用电压监视器0复位		0.0084	-	-		-
	SCI/USB boot mode*1		0.0084	-	20		-
VCC falling gradient*2		SfVCC	0.0084	-	-	ms/V	-

Note 1. 在引导模式下，无论OFS1.LVDAS位的值如何，电压监视器0的复位均被禁用。
Note 2. 这适用于使用VBATT时。

Table 60.9 升降梯度和纹波频率特性
纹波电压必须在VCC上限(3.6V)和下限(2.7V)之间的范围内满足允许的纹波频率fr(VCC)。当VCC变化超过VCC±10%时，必须满足允许的电压变化上升和下降梯度dtdVCC。

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
允许纹波频率	$f_{r (VCC)}$	-	-	10	kHz	Figure 60.6 $V_{r (VCC)}$ ≤ VCC × 0.2
		-	-	1	MHz	Figure 60.6 $V_{r (VCC)}$ ≤ VCC × 0.08
		-	-	10	MHz	Figure 60.6 $V_{r (VCC)}$ ≤ VCC × 0.06
允许电压变化上升下降梯度	dt/dVCC	1.0	-	-	ms/V	当VCC变化超过VCC±10%

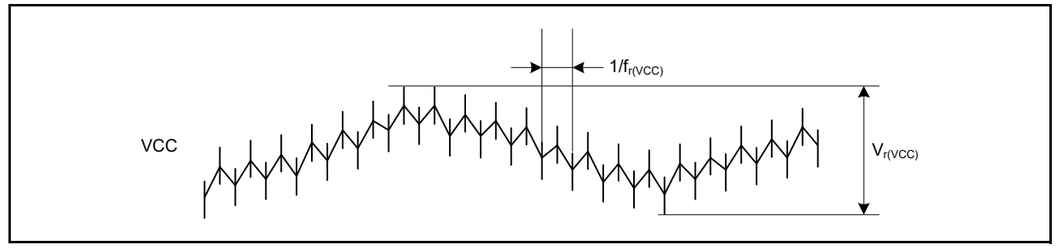


Figure 60.6 纹波波形

60.3 交流特性

60.3.1 Frequency

Table 60.10 高速模式下的运行频率值

Parameter			Symbol	Min	Typ	Max	Unit
运行频率	系统时钟(ICLK*2)		f	-	-	120	MHz
	外设模块时钟(PCLKA)*2			-	-	120	
	外设模块时钟(PCLKB)*2			-	-	60	
	外设模块时钟(PCLKC)*2			-*3	-	60	
	外设模块时钟(PCLKD)*2			-	-	120	
	闪存接口时钟(FCLK)*2			-*1	-	60	
	外部总线时钟(BCLK)*2			-	-	120	
	EBCLK引脚输出			-	-	60	
	SDCLK 引脚输出	VCC ≥ 3.0 V		-	-	120	

Note 1. FCLK must run at a frequency of at least 4 MHz when programming or erasing the flash memory.
Note 2. See section 9, Clock Generation Circuit for the relationship between the ICLK, PCLKA, PCLKB, PCLKC, PCLKD, FCLK, and BCLK frequencies.
Note 3. When the ADC12 is used, the PCLKC frequency must be at least 1 MHz.

Table 60.11 Operation frequency value in low-speed mode

Parameter		Symbol	Min	Typ	Max	Unit
Operation frequency	System clock (ICLK)*2	f	-	-	1	MHz
	Peripheral module clock (PCLKA)*2		-	-	1	
	Peripheral module clock (PCLKB)*2		-	-	1	
	Peripheral module clock (PCLKC)*2,*3		-*3	-	1	
	Peripheral module clock (PCLKD)*2		-	-	1	
	Flash interface clock (FCLK)*1, *2		-	-	1	
	External bus clock (BCLK)		-	-	1	
	EBCLK pin output		-	-	1	

Note 1. Programming or erasing the flash memory is disabled in low-speed mode.
Note 2. See section 9, Clock Generation Circuit for the relationship between the ICLK, PCLKA, PCLKB, PCLKC, PCLKD, FCLK, and BCLK frequencies.
Note 3. When the ADC12 is used, the PCLKC frequency must be set to at least 1 MHz.

Table 60.12 Operation frequency value in Subosc-speed mode

Parameter		Symbol	Min	Typ	Max	Unit
Operation frequency	System clock (ICLK)*2	f	27.8	-	37.7	kHz
	Peripheral module clock (PCLKA)*2		-	-	37.7	
	Peripheral module clock (PCLKB)*2		-	-	37.7	
	Peripheral module clock (PCLKC)*2,*3		-	-	37.7	
	Peripheral module clock (PCLKD)*2		-	-	37.7	
	Flash interface clock (FCLK)*1, *2		27.8	-	37.7	
	External bus clock (BCLK)*2		-	-	37.7	
	EBCLK pin output		-	-	37.7	

Note 1. Programming or erasing the flash memory is disable in Subosc-speed mode.
Note 2. See section 9, Clock Generation Circuit for the relationship between the ICLK, PCLKA, PCLKB, PCLKC, PCLKD, FCLK, and BCLK frequencies.
Note 3. The ADC12 cannot be used.

60.3.2 Clock Timing

Table 60.13 Clock timing except for sub-clock oscillator (1 of 2)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
EBCLK pin output cycle time	t_{Bcyc}	16.6	-	-	ns	Figure 60.7
EBCLK pin output high pulse width	t_{CH}	3.3	-	-	ns	
EBCLK pin output low pulse width	t_{CL}	3.3	-	-	ns	
EBCLK pin output rise time	t_{Cr}	-	-	5.0	ns	
EBCLK pin output fall time	t_{Cf}	-	-	5.0	ns	
SDCLK pin output cycle time	t_{SDcyc}	8.33	-	-	ns	
SDCLK pin output high pulse width	t_{CH}	1.0	-	-	ns	
SDCLK pin output low pulse width	t_{CL}	1.0	-	-	ns	
SDCLK pin output rise time	t_{Cr}	-	-	3.0	ns	
SDCLK pin output fall time	t_{Cf}	-	-	3.0	ns	

Note 1. 在对闪存进行编程或擦除时，FCLK必须以至少4MHz的频率运行。
Note 2. 有关ICLK、PCLKA、PCLKB、PCLKC、PCLKD、FCLK和BCLK frequencies.
Note 3. 使用ADC12时，PCLKC频率必须至少为1MHz。

Table 60.11 低速模式下的运行频率值

Parameter		Symbol	Min	Typ	Max	Unit
运行频率	系统时钟(ICLK)*2	f	-	-	1	MHz
	外设模块时钟(PCLKA)*2		-	-	1	
	外设模块时钟(PCLKB)*2		-	-	1	
	外设模块时钟(PCLKC)*2 *3		-*3	-	1	
	外设模块时钟(PCLKD)*2		-	-	1	
	Flash接口时钟(FCLK)*1 *2		-	-	1	
	外部总线时钟(BCLK)		-	-	1	
	EBCLK引脚输出		-	-	1	

Note 1. 在低速模式下禁止对闪存进行编程或擦除。
Note 2. 有关ICLK、PCLKA、PCLKB、PCLKC、PCLKD、FCLK和BCLK frequencies.
Note 3. 使用ADC12时，PCLKC频率必须设置为至少1MHz。

Table 60.12 Subosc-speed模式下的运行频率值

Parameter		Symbol	Min	Typ	Max	Unit
运行频率	系统时钟(ICLK)*2	f	27.8	-	37.7	kHz
	外设模块时钟(PCLKA)*2		-	-	37.7	
	外设模块时钟(PCLKB)*2		-	-	37.7	
	外设模块时钟(PCLKC)*2 *3		-	-	37.7	
	外设模块时钟(PCLKD)*2		-	-	37.7	
	Flash接口时钟(FCLK)*1 *2		27.8	-	37.7	
	外部总线时钟(BCLK)*2		-	-	37.7	
	EBCLK引脚输出		-	-	37.7	

Note 1. 在Subosc速度模式下，禁止对闪存进行编程或擦除。
Note 2. 有关ICLK、PCLKA、PCLKB、PCLKC、PCLKD、FCLK和BCLK frequencies.
Note 3. ADC12不能使用。

60.3.2 时钟时序

Table 60.13 除副时钟振荡器外的时钟时序（2个中的1个）

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
EBCLK引脚输出周期时间	t_{Bcyc}	16.6	-	-	ns	Figure 60.7
EBCLK引脚输出高脉冲宽度	t_{CH}	3.3	-	-	ns	
EBCLK引脚输出低脉冲宽度	t_{CL}	3.3	-	-	ns	
EBCLK引脚输出上升时间	t_{Cr}	-	-	5.0	ns	
EBCLK引脚输出下降时间	t_{Cf}	-	-	5.0	ns	
SDCLK 引脚输出周期时间	t_{SDcyc}	8.33	-	-	ns	
SDCLK 引脚输出高脉冲宽度	t_{CH}	1.0	-	-	ns	
SDCLK 引脚输出低脉冲宽度	t_{CL}	1.0	-	-	ns	
SDCLK 引脚输出上升时间	t_{Cr}	-	-	3.0	ns	
SDCLK 引脚输出下降时间	t_{Cf}	-	-	3.0	ns	

Table 60.13 Clock timing except for sub-clock oscillator (2 of 2)

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
EXTAL external clock input cycle time		t_{EXcyc}	41.66	-	-	ns	Figure 60.8
EXTAL external clock input high pulse width		t_{EXH}	15.83	-	-	ns	
EXTAL external clock input low pulse width		t_{EXL}	15.83	-	-	ns	
EXTAL external clock rise time		t_{EXr}	-	-	5.0	ns	
EXTAL external clock fall time		t_{EXf}	-	-	5.0	ns	
Main clock oscillator frequency		f_{MAIN}	8	-	24	MHz	-
Main clock oscillation stabilization wait time (crystal) *1		$t_{MAINOSCWT}$	-	-	-*1	ms	Figure 60.9
LOCO clock oscillation frequency		f_{LOCO}	27.8528	32.768	37.6832	kHz	-
LOCO clock oscillation stabilization wait time		t_{LOCOWT}	-	-	60.4	µs	Figure 60.10
ILOCO clock oscillation frequency		f_{ILOCO}	12.75	15	17.25	kHz	-
MOCO clock oscillation frequency		F_{MOCO}	6.8	8	9.2	MHz	-
MOCO clock oscillation stabilization wait time		t_{MOCOWT}	-	-	15.0	µs	-
HOCO clock oscillator oscillation frequency	Without FLL	f_{HOCO16}	15.78	16	16.22	MHz	-20 ≤ Ta ≤ 105°C
		f_{HOCO18}	17.75	18	18.25		
		f_{HOCO20}	19.72	20	20.28		
		f_{HOCO16}	15.71	16	16.29		-40 ≤ Ta ≤ -20°C
		f_{HOCO18}	17.68	18	18.32		
		f_{HOCO20}	19.64	20	20.36		
	With FLL	f_{HOCO16}	15.955	16	16.045		-40 ≤ Ta ≤ 105°C Sub-clock frequency accuracy is ±50 ppm.
		f_{HOCO18}	17.949	18	18.051		
		f_{HOCO20}	19.944	20	20.056		
HOCO clock oscillation stabilization wait time*2		t_{HOCOWT}	-	-	64.7	µs	-
FLL stabilization wait time		t_{FLLWT}	-	-	1.8	ms	-
PLL clock frequency		f_{PLL}	120	-	240	MHz	-
PLL clock oscillation stabilization wait time		t_{PLLWT}	-	-	174.9	µs	Figure 60.11

Note 1. When setting up the main clock oscillator, ask the oscillator manufacturer for an oscillation evaluation and use the results as the recommended oscillation stabilization time. Set the MOSCWTCR register to a value equal to or greater than the recommended value.
After changing the setting in the MOSCCR.MOSTP bit to start main clock operation, read the OSCSF.MOSCSF flag to confirm that it is 1, and then start using the main clock oscillator.

Note 2. This is the time from release from reset state until the HOCO oscillation frequency (fHOCO) reaches the range for guaranteed operation.

Table 60.14 Clock timing for the sub-clock oscillator

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Sub-clock frequency	f_{SUB}	-	32.768	-	kHz	-
Sub-clock oscillation stabilization wait time	$t_{SUBOSCWT}$	-	-	*1	s	Figure 60.12

Note 1. When setting up the sub-clock oscillator, ask the oscillator manufacturer for an oscillation evaluation and use the results as the recommended oscillation stabilization time.
After changing the setting in the SOSCCR.SOSTP bit to start sub-clock operation, only start using the sub-clock oscillator after the sub-clock oscillation stabilization time elapses with an adequate margin. Two times the value shown is recommended.

Table 60.13 除副时钟振荡器外的时钟时序(2of2)

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
EXTAL外部时钟输入周期时间		t_{EXcyc}	41.66	-	-	ns	Figure 60.8
EXTAL外部时钟输入高脉冲宽度		t_{EXH}	15.83	-	-	ns	
EXTAL外部时钟输入低脉冲宽度		t_{EXL}	15.83	-	-	ns	
EXTAL外部时钟上升时间		t_{EXr}	-	-	5.0	ns	
EXTAL外部时钟下降时间		t_{EXf}	-	-	5.0	ns	
主时钟振荡器频率		f_{MAIN}	8	-	24	MHz	-
主时钟振荡稳定等待时间（晶振）*1		$t_{MAINOSCWT}$	-	-	-*1	ms	Figure 60.9
LOCO时钟振荡频率		f_{LOCO}	27.8528	32.768	37.6832	kHz	-
LOCO时钟振荡稳定等待时间		t_{LOCOWT}	-	-	60.4	µs	Figure 60.10
ILOCO时钟振荡频率		f_{ILOCO}	12.75	15	17.25	kHz	-
MOCO时钟振荡频率		F_{MOCO}	6.8	8	9.2	MHz	-
MOCO时钟振荡稳定等待时间		t_{MOCOWT}	-	-	15.0	µs	-
HOCO时钟振荡器振荡频率	Without FLL	f_{HOCO16}	15.78	16	16.22	MHz	-20 ≤ Ta ≤ 105°C
		f_{HOCO18}	17.75	18	18.25		
		f_{HOCO20}	19.72	20	20.28		
		f_{HOCO16}	15.71	16	16.29		-40 ≤ Ta ≤ -20°C
		f_{HOCO18}	17.68	18	18.32		
		f_{HOCO20}	19.64	20	20.36		
	With FLL	f_{HOCO16}	15.955	16	16.045		−40≤Ta≤105°C副时钟频率精度为±50ppm。
		f_{HOCO18}	17.949	18	18.051		
		f_{HOCO20}	19.944	20	20.056		
HOCO时钟振荡稳定等待时间*2		t_{HOCOWT}	-	-	64.7	µs	-
FLL稳定等待时间		t_{FLLWT}	-	-	1.8	ms	-
锁相环时钟频率		f_{PLL}	120	-	240	MHz	-
PLL时钟振荡稳定等待时间		t_{PLLWT}	-	-	174.9	µs	Figure 60.11

Note 1. 设置主时钟振荡器时，请向振荡器制造商索取振荡评估，并将结果作为推荐的振荡稳定时间。将MOSCWTCR寄存器设置为等于或大于推荐值的值。更改MOSCCR.MOSTP位的设置以启动主时钟操作后，读取OSCSF.MOSCSF标志以确认其为1，然后开始使用主时钟振荡器。

Note 2. 这是从复位状态释放到HOCO振荡频率(fHOCO)达到保证工作范围的时间。

Table 60.14 副时钟振荡器的时钟时序

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
Sub-clock frequency	f_{SUB}	-	32.768	-	kHz	-
副时钟振荡稳定等待时间	$t_{SUBOSCWT}$	-	-	*1	s	Figure 60.12

Note 1. 设置副时钟振荡器时，请向振荡器制造商索取振荡评估，并将结果作为推荐的振荡稳定时间。更改SOSCCR.SOSTP位的设置以启动副时钟操作后，只有在副时钟振荡稳定时间过去并留有足够余量后才开始使用副时钟振荡器。建议使用显示值的两倍。

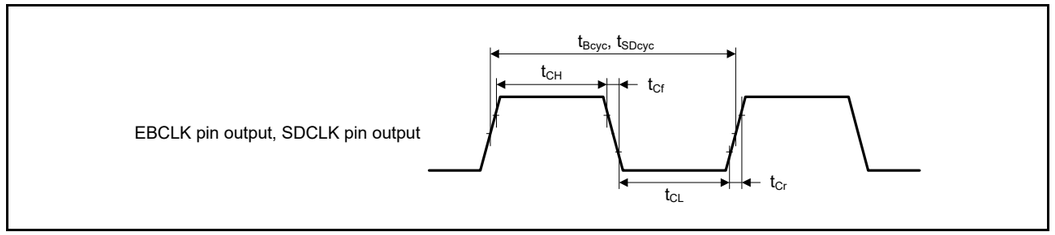


Figure 60.7 EBCLK and SDCLK output timing

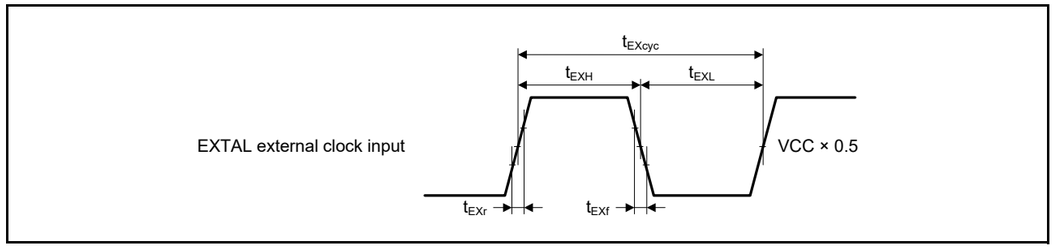


Figure 60.8 EXTAL external clock input timing

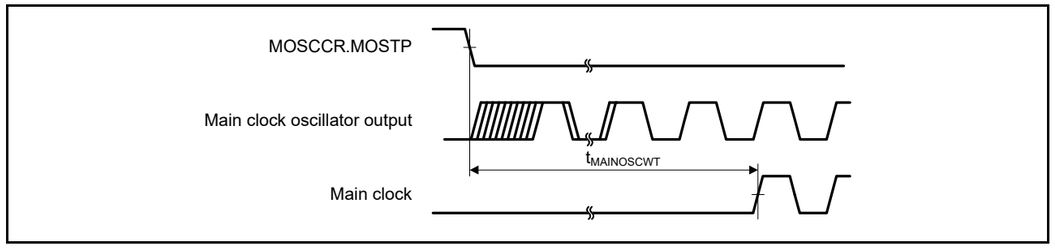


Figure 60.9 Main clock oscillation start timing

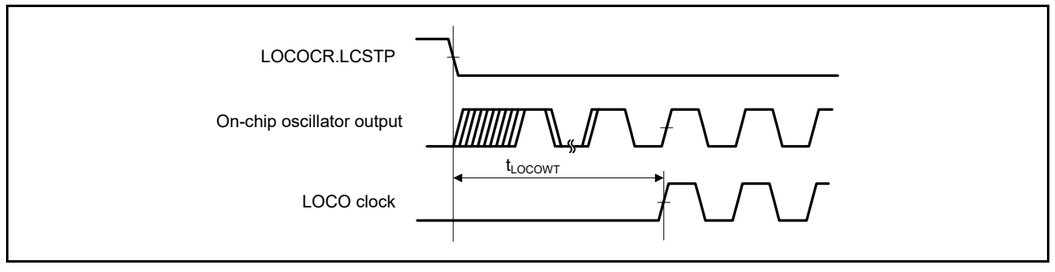


Figure 60.10 LOCO clock oscillation start timing

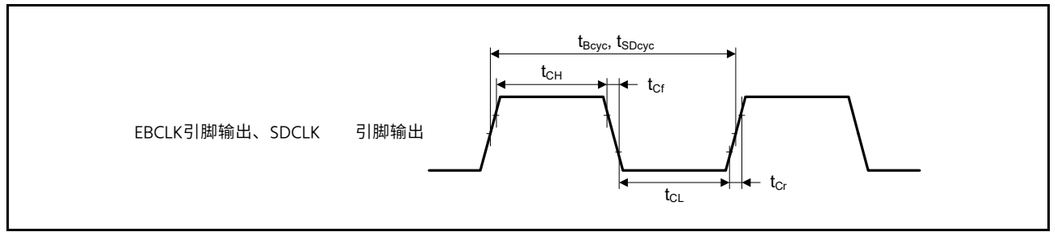


Figure 60.7 EBCLK和SDCLK 输出时序

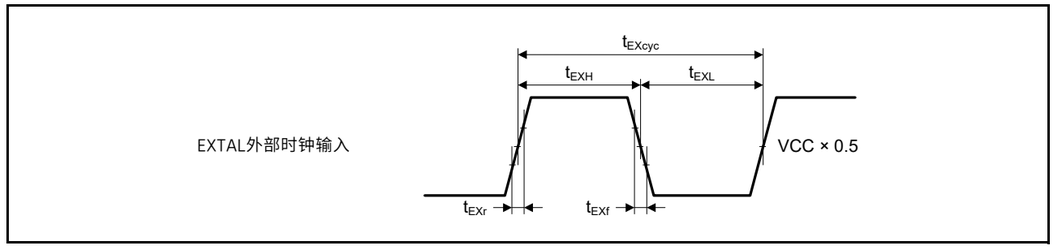


Figure 60.8 EXTAL外部时钟输入时序

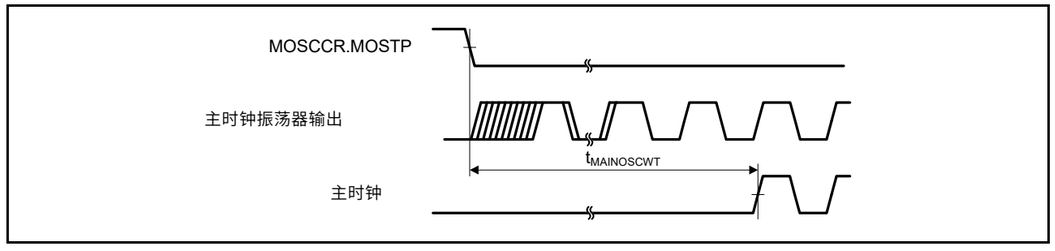


Figure 60.9 主时钟振荡开始时序

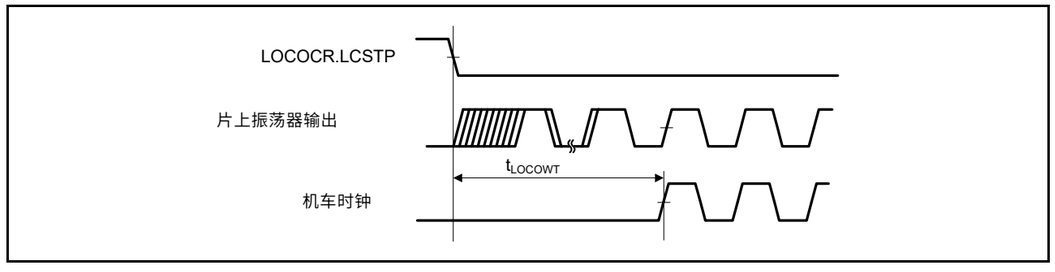


Figure 60.10 LOCO时钟振荡开始时序

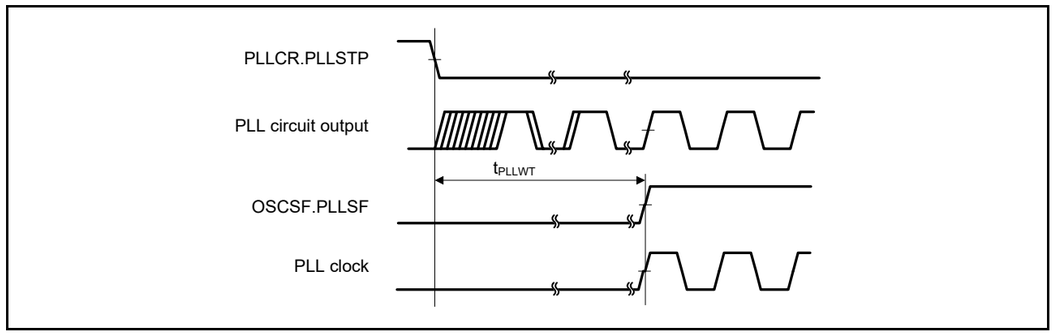


Figure 60.11 PLL clock oscillation start timing

Note: Only operate the PLL is operated after main clock oscillation has stabilized.

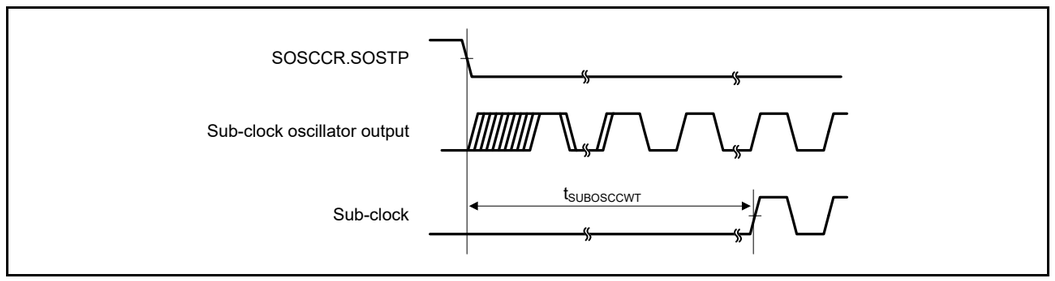


Figure 60.12 Sub-clock oscillation start timing

60.3.3 Reset Timing

Table 60.15 Reset timing

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
RES pulse width	Power-on	t_{RESWP}	1	-	-	ms	Figure 60.13
	Deep Software Standby mode	t_{RESWD}	0.6	-	-	ms	Figure 60.14
	Software Standby mode, Subosc-speed mode	t_{RESWS}	0.3	-	-	ms	
	All other	t_{RESW}	200	-	-	µs	
Wait time after RES cancellation		t_{RESWT}	-	29	33	µs	Figure 60.13
Wait time after internal reset cancellation (IWDT reset, WDT reset, software reset, SRAM parity error reset, SRAM ECC error reset, bus master MPU error reset, bus slave MPU error reset, stack pointer error reset)		t_{RESW2}	-	320	408	µs	-

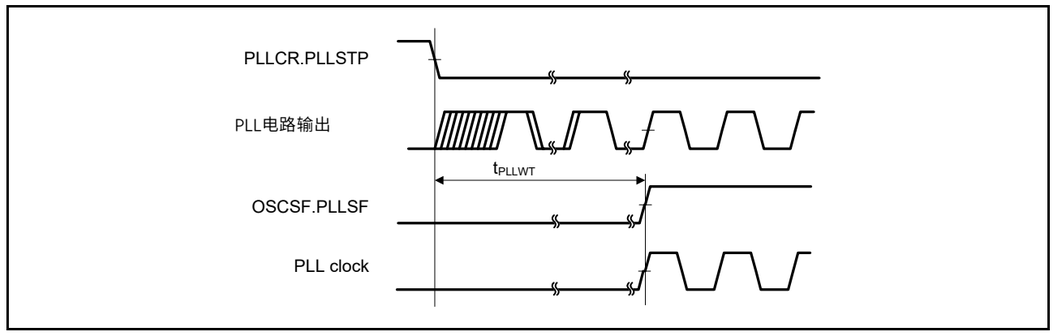


Figure 60.11 PLL时钟振荡开始时序

Note: 仅在主时钟振荡稳定后操作PLL。

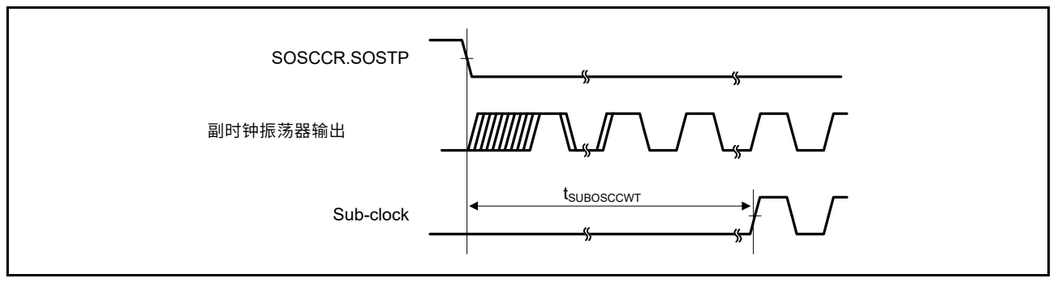


Figure 60.12 副时钟振荡开始时序

60.3.3 重置时间

Table 60.15 重置时间

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
RES脉冲宽度	Power-on	t_{RESWP}	1	-	-	ms	Figure 60.13
	深度软件待机模式	t_{RESWD}	0.6	-	-	ms	Figure 60.14
	软件待机模式，Subosc速度模式	t_{RESWS}	0.3	-	-	ms	
	所有其他	t_{RESW}	200	-	-	µs	
RES取消后的等待时间		t_{RESWT}	-	29	33	µs	Figure 60.13
内部复位取消后的等待时间（IWDT复位、WDT复位、软件复位、SRAM奇偶校验错误复位、SRAMECC错误复位、总线主MPU错误复位、总线从MPU错误复位、堆栈指针错误复位）		t_{RESW2}	-	320	408	µs	-

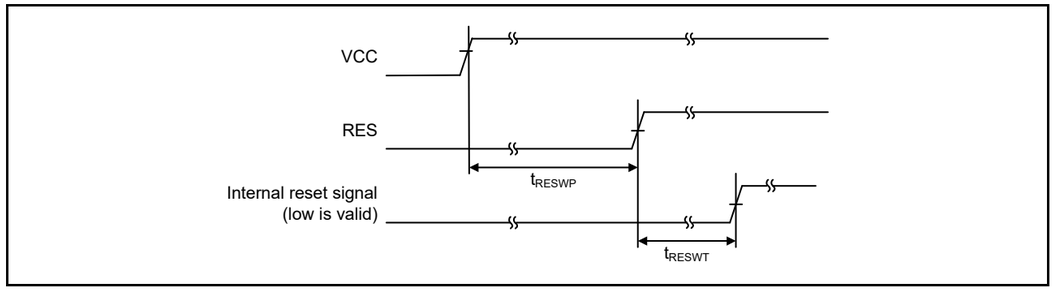


Figure 60.13 Power-on reset timing

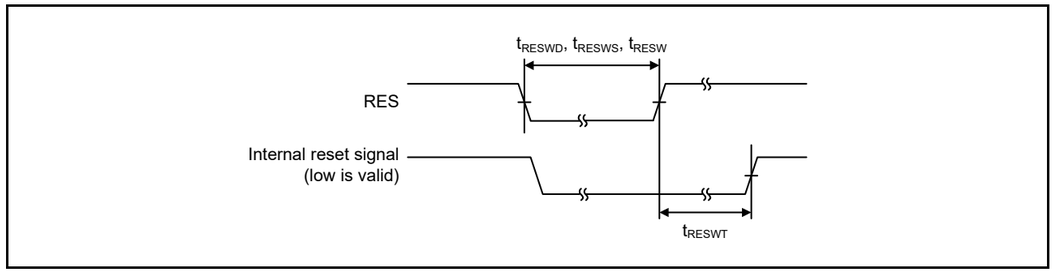


Figure 60.14 Reset input timing

60.3.4 Wakeup Timing

Table 60.16 Timing of recovery from low power modes

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Recovery time from Software Standby mode*1	Crystal resonator connected to main clock oscillator	System clock source is main clock oscillator*2	t_{SBYMC}	-	2.4*9	2.8*9	ms	Figure 60.15 The division ratio of all oscillators is 1.
		System clock source is PLL with main clock oscillator*3	t_{SBYPC}	-	2.7*9	3.2*9	ms	
	External clock input to main clock oscillator	System clock source is main clock oscillator*4	t_{SBYEX}	-	230*9	280*9	µs	
		System clock source is PLL with main clock oscillator*5	t_{SBYPE}	-	570*9	700*9	µs	
	System clock source is sub-clock oscillator*8		t_{SBYSC}	-	1.2*9	1.3*9	ms	
	System clock source is LOCO*8		t_{SBYLO}	-	1.2*9	1.4*9	ms	
	System clock source is HOCO clock oscillator*6		t_{SBYHO}	-	240*9, *10	310 *9, *10	µs	
	System clock source is MOCO clock oscillator*7		t_{SBYMO}	-	220*9	300*9	µs	
Recovery time from Deep Software Standby mode			t_{DSBY}	-	0.65	1.0	ms	Figure 60.16
Wait time after cancellation of Deep Software Standby mode			t_{DSBYWT}	34	-	35	t_{cyc}	
Recovery time from Software Standby mode to Snooze mode	High-speed mode when system clock source is HOCO (20 MHz)		t_{SNZ}	-	35*9, *10	71 *9, *10	µs	Figure 60.17
	High-speed mode when system clock source is MOCO (8 MHz)		t_{SNZ}	-	11*9	14*9	µs	

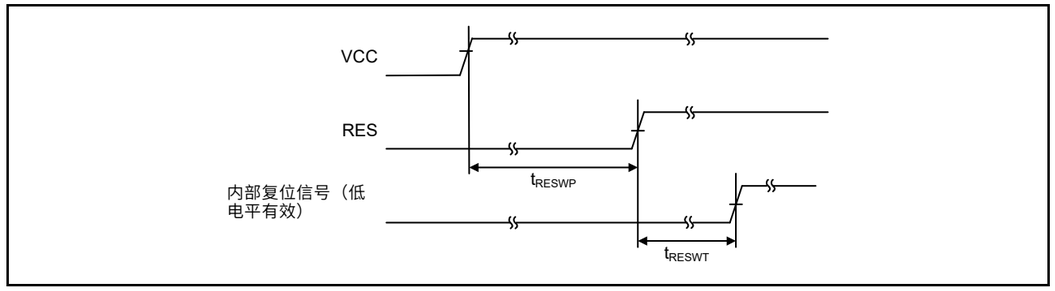


Figure 60.13 上电复位时序

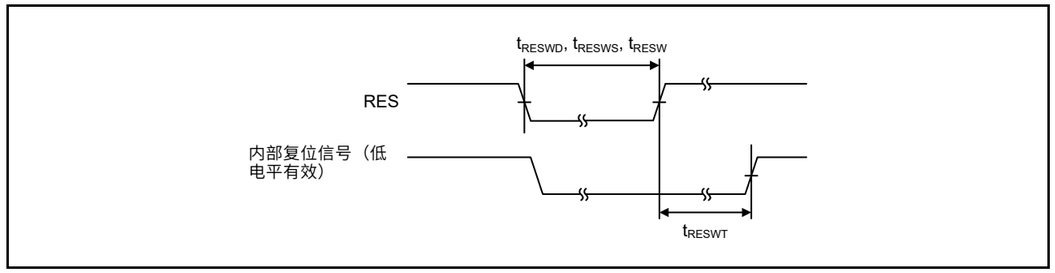


Figure 60.14 复位输入时序

60.3.4 唤醒时间

Table 60.16 从低功耗模式恢复的时间

Parameter			Symbol	Min	Typ	Max	Unit	测试条件
从软件待机模式恢复时间*1	连接到主时钟振荡器的晶体谐振器	系统时钟源为主时钟振荡器*2	t_{SBYMC}	-	2.4*9	2.8*9	ms	图60.15所有振荡器的分频比为1。
		系统时钟源是带有主时钟振荡器的PLL*3	t_{SBYPC}	-	2.7*9	3.2*9	ms	
	主时钟振荡器的外部时钟输入	系统时钟源为主时钟振荡器*4	t_{SBYEX}	-	230*9	280*9	µs	
		系统时钟源是带有主时钟振荡器*5的PLL	t_{SBYPE}	-	570*9	700*9	µs	
	系统时钟源为副时钟振荡器*8		t_{SBYSC}	-	1.2*9	1.3*9	ms	
	系统时钟源为LOCO*8		t_{SBYLO}	-	1.2*9	1.4*9	ms	
	系统时钟源为HOCO时钟振荡器*6		t_{SBYHO}	-	240*9, *10	310 *9, *10	µs	
	系统时钟源为MOCO时钟振荡器*7		t_{SBYMO}	-	220*9	300*9	µs	
从深度软件待机模式恢复时间			t_{DSBY}	-	0.65	1.0	ms	Figure 60.16
取消深度软件待机模式后的等待时间			t_{DSBYWT}	34	-	35	t_{cyc}	
从软件待机模式恢复到	系统时钟源为HOCO(20MHz)时的高速模式		t_{SNZ}	-	35*9, *10	71 *9, *10	µs	Figure 60.17
贪睡模式	系统时钟源为MOCO(8MHz)时的高速模式		t_{SNZ}	-	11*9	14*9	µs	

Note 1. The recovery time is determined by the system clock source. When multiple oscillators are active, the recovery time can be determined with the following equation:
Total recovery time = recovery time for an oscillator as the system clock source + the longest oscillation stabilization time of any oscillators requiring longer stabilization times than the system clock source + 2 LOCO cycles (when LOCO is operating) + 3 SOSC cycles (when Subosc is oscillating and MSTPC0 = 0 (CAC module stop)).

Note 2. When the frequency of the crystal is 24 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 05h). For other settings (MOSCWTCR is set to Xh), the recovery time can be determined with the following equation:
t_{SBYMC} (MOSCWTCR = Xh) = t_{SBYMC} (MOSCWTCR = 05h) + ($t_{MAINOSCWT}$ (MOSCWTCR = Xh) - $t_{MAINOSCWT}$ (MOSCWTCR = 05h))

Note 3. When the frequency of PLL is 240 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 05h). For other settings (MOSCWTCR is set to Xh), the recovery time can be determined with the following equation:
t_{SBYMC} (MOSCWTCR = Xh) = t_{SBYMC} (MOSCWTCR = 05h) + ($t_{MAINOSCWT}$ (MOSCWTCR = Xh) - $t_{MAINOSCWT}$ (MOSCWTCR = 05h))

Note 4. When the frequency of the external clock is 24 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 01h). For other settings (MOSCWTCR is set to Xh), the recovery time can be determined with the following equation:
t_{SBYMC} (MOSCWTCR = Xh) = t_{SBYMC} (MOSCWTCR = 01h) + ($t_{MAINOSCWT}$ (MOSCWTCR = Xh) - $t_{MAINOSCWT}$ (MOSCWTCR = 01h))

Note 5. When the frequency of PLL is 240 MHz (Main Clock Oscillator Wait Control Register (MOSCWTCR) is set to 01h). For other settings (MOSCWTCR is set to Xh), the recovery time can be determined with the following equation:
t_{SBYMC} (MOSCWTCR = Xh) = t_{SBYMC} (MOSCWTCR = 01h) + ($t_{MAINOSCWT}$ (MOSCWTCR = Xh) - $t_{MAINOSCWT}$ (MOSCWTCR = 01h))

Note 6. The HOCO frequency is 20 MHz.

Note 7. The MOCO frequency is 8 MHz.

Note 8. In Subosc-speed mode, the sub-clock oscillator or LOCO continues oscillating in Software Standby mode.

Note 9. When the SNZCR.RXDREQEN bit is set to 0, the following time is added as the power supply recovery time:
STCONR.STCON[1:0] = 00b:16 µs (typical), 34 µs (maximum)
STCONR.STCON[1:0] = 11b:16 µs (typical), 104 µs (maximum).

Note 10. When the SNZCR.RXDREQEN bit is set to 0, 16 µs (typical) or 18 µs (maximum) is added as the HOCO wait time.

Note 1. 恢复时间由系统时钟源决定。当多个振荡器处于活动状态时，恢复时间可以通过以下公式确定：总恢复时间=振荡器作为系统时钟源的恢复时间+任何需要比系统时钟源更长稳定时间的振荡器的最长振荡稳定时间+2个LOCO周期（当LOCO运行时）+3个SOSC周期（当Subosc正在振荡且MSTPC0=0（CAC模块停止）时）。

Note 2. 当晶振频率为24MHz时（主时钟振荡器等待控制寄存器（MOSCWTCR）设置为05h）。对于其他设置（MOSCWTCR设置为Xh），可以使用以下公式确定恢复时间：tSBYMC(MOSCWTCR=Xh)=tSBYMC(MOSCWTCR=05h)+(tMAINOSCWT(MOSCWTCR=Xh)tMAINOSCWT(MOSCWTCR=05h))

Note 3. 当PLL的频率为240MHz时（主时钟振荡器等待控制寄存器（MOSCWTCR）设置为05h）。对于其他设置（MOSCWTCR设置为Xh），可以使用以下公式确定恢复时间：tSBYMC(MOSCWTCR=Xh)=tSBYMC(MOSCWTCR=05h)+(tMAINOSCWT(MOSCWTCR=Xh)tMAINOSCWT(MOSCWTCR=05h))

Note 4. 当外部时钟频率为24MHz时（主时钟振荡器等待控制寄存器（MOSCWTCR）设置为01h）。对于其他设置（MOSCWTCR设置为Xh），可以使用以下公式确定恢复时间：tSBYMC(MOSCWTCR=Xh)=tSBYMC(MOSCWTCR=01h)+(tMAINOSCWT(MOSCWTCR=Xh)tMAINOSCWT(MOSCWTCR=01h))

Note 5. 当PLL的频率为240MHz时（主时钟振荡器等待控制寄存器（MOSCWTCR）设置为01h）。对于其他设置（MOSCWTCR设置为Xh），可以使用以下公式确定恢复时间：tSBYMC(MOSCWTCR=Xh)=tSBYMC(MOSCWTCR=01h)+(tMAINOSCWT(MOSCWTCR=Xh)tMAINOSCWT(MOSCWTCR=01h))

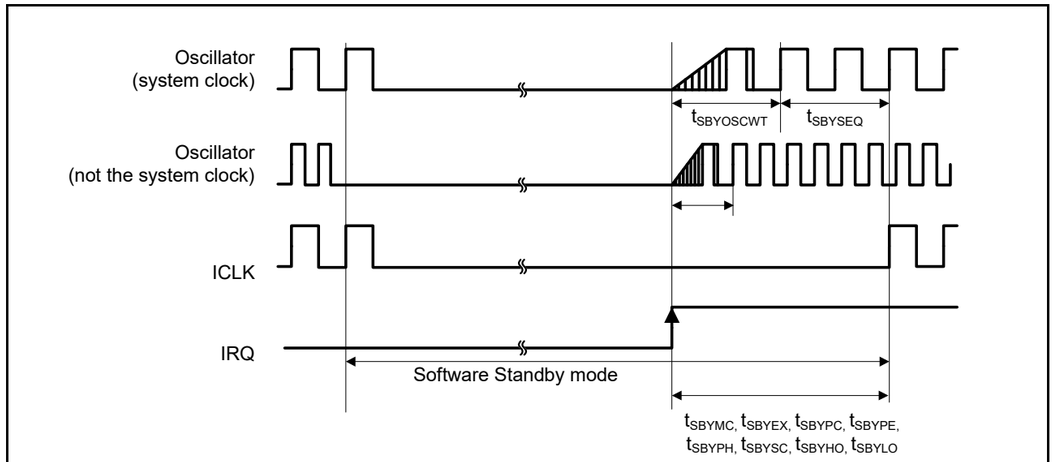
Note 6. HOCO频率为20MHz。

Note 7. MOCO频率为8MHz。

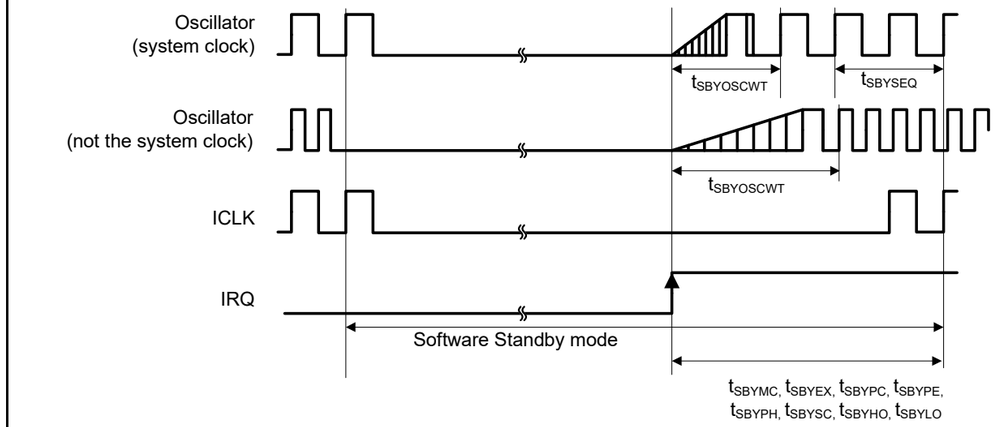
Note 8. 在Subosc速度模式下，副时钟振荡器或LOCO在软件待机模式下继续振荡。

Note 9. 当SNZCR.RXDREQEN位设置为0时，添加以下时间作为电源恢复时间：
STCONR.STCON[1:0] = 00b:16 µs (typical), 34 µs (maximum)
STCONR.STCON[1:0] = 11b:16 µs (typical), 104 µs (maximum).

注10.当SNZCR.RXDREQEN位设置为0时，添加16µs（典型值）或18µs（最大值）作为HOCO等待时间。

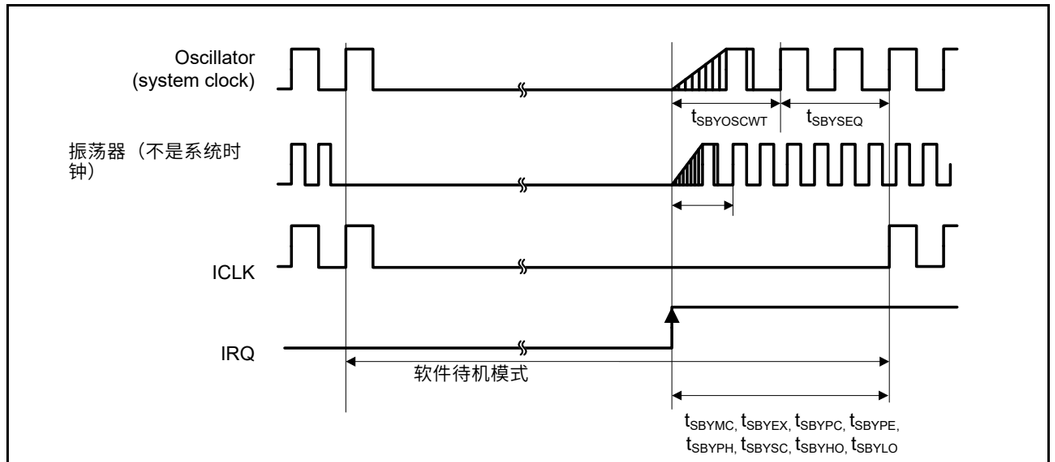


When stabilization of the system clock oscillator is slower

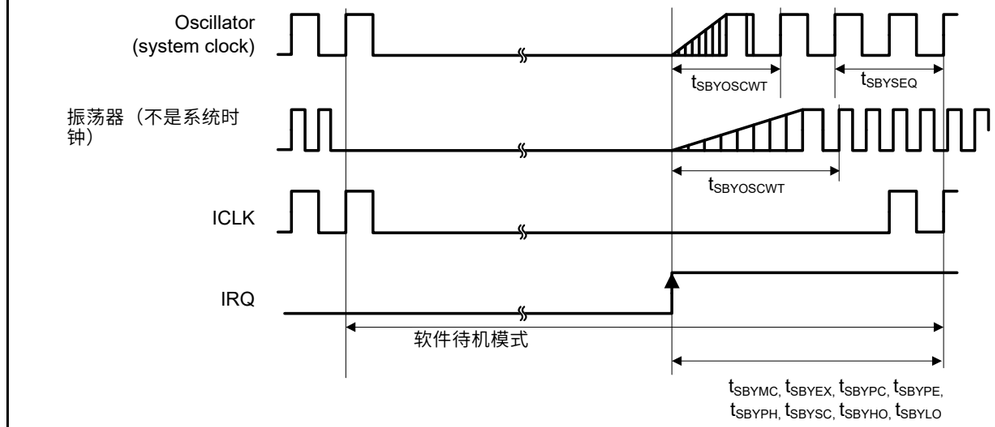


When stabilization of an oscillator other than the system clock is slower

Figure 60.15 Software Standby mode cancellation timing



当系统时钟振荡器的稳定速度较慢时



当系统时钟以外的振荡器稳定较慢时

Figure 60.15 软件待机模式取消时序

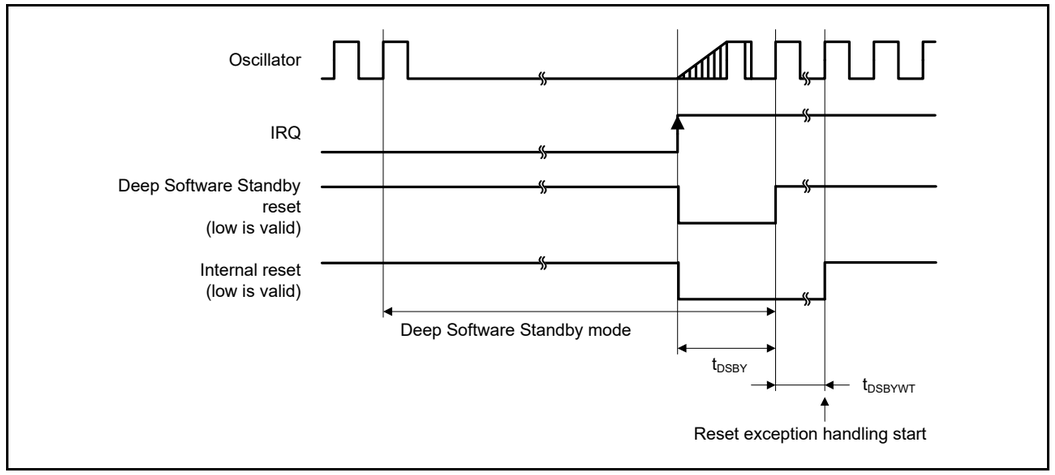
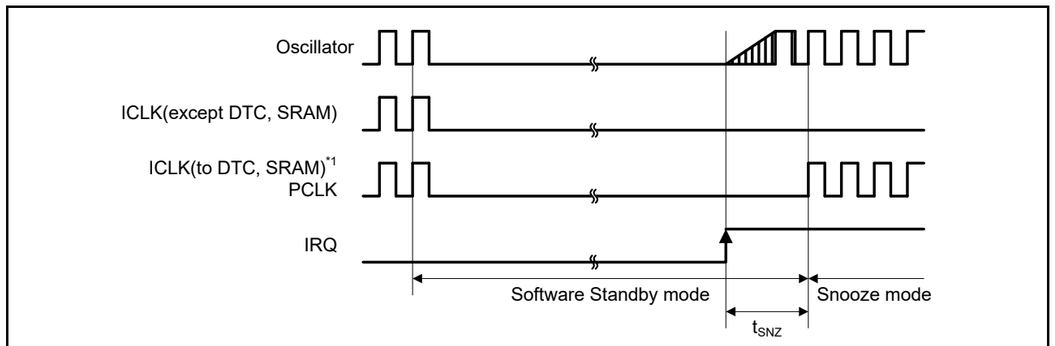


Figure 60.16 Deep Software Standby mode cancellation timing



Note 1. When SNZCR.SNZDTCEN is set to 1, ICLK is supplied to DTC and SRAM.

Figure 60.17 Recovery timing from Software Standby mode to Snooze mode

60.3.5 NMI and IRQ Noise Filter

Table 60.17 NMI and IRQ noise filter

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions	
NMI pulse width	t_{NMIW}	200	-	-	ns	NMI digital filter disabled	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2$*1	-	-			$t_{Pcyc} \times 2 > 200$ ns
		200	-	-		NMI digital filter enabled	$t_{NMICK} \times 3 \leq 200$ ns
		$t_{NMICK} \times 3.5$*2	-	-			$t_{NMICK} \times 3 > 200$ ns
IRQ pulse width	t_{IRQW}	200	-	-	ns	IRQ digital filter disabled	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2$*1	-	-			$t_{Pcyc} \times 2 > 200$ ns
		200	-	-		IRQ digital filter enabled	$t_{IRQCK} \times 3 \leq 200$ ns
		$t_{IRQCK} \times 3.5$*3	-	-			$t_{IRQCK} \times 3 > 200$ ns

Note: 200 ns minimum in Software Standby mode.
Note: If the clock source is switched, add 4 clock cycles of the switched source.

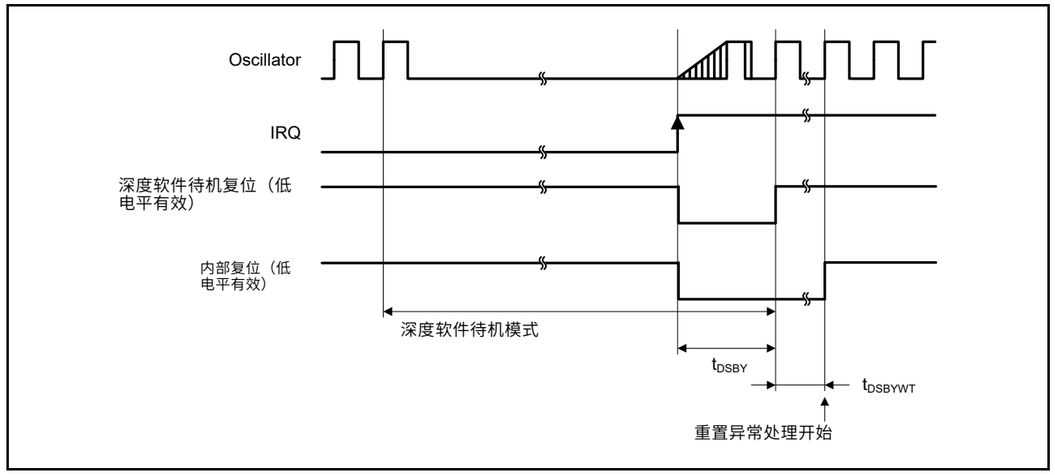
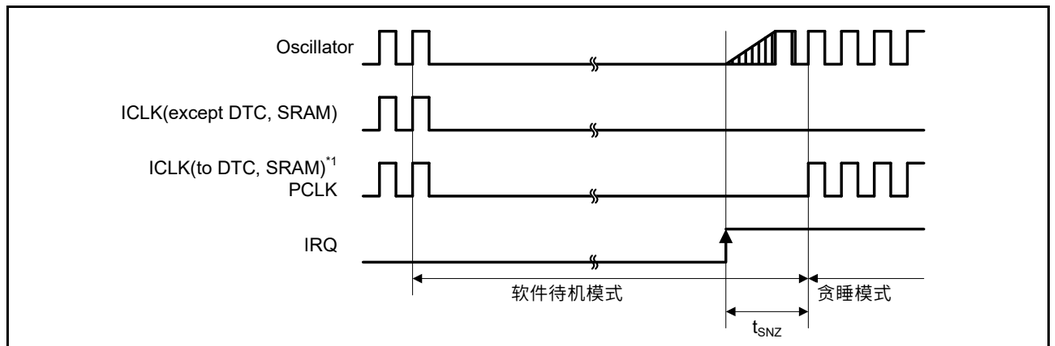


Figure 60.16 深度软件待机模式取消时序



注1.当SNZCR.SNZDTCEN设置为1时，ICLK提供给DTC和SRAM。

Figure 60.17 从软件待机模式到贪睡模式的恢复时间

60.3.5 NMI和IRQ噪声滤波器

Table 60.17 NMI和IRQ噪声滤波器

Parameter	Symbol	Min	Typ	Max	Unit	测试条件	
NMI脉冲宽度	t_{NMIW}	200	-	-	ns	NMI数字滤波器禁用	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2$*1	-	-			$t_{Pcyc} \times 2 > 200$ ns
		200	-	-		启用NMI数字滤波器	$t_{NMICK} \times 3 \leq 200$ ns
		$t_{NMICK} \times 3.5$*2	-	-			$t_{NMICK} \times 3 > 200$ ns
IRQ脉冲宽度	t_{IRQW}	200	-	-	ns	IRQ数字滤波器禁用	$t_{Pcyc} \times 2 \leq 200$ ns
		$t_{Pcyc} \times 2$*1	-	-			$t_{Pcyc} \times 2 > 200$ ns
		200	-	-		启用IRQ数字滤波器	$t_{IRQCK} \times 3 \leq 200$ ns
		$t_{IRQCK} \times 3.5$*3	-	-			$t_{IRQCK} \times 3 > 200$ ns

Note: 软件待机模式下最少200ns。
Note: 如果时钟源切换，则增加切换源的4个时钟周期。

Note 1. t_{Pcyc} indicates the PCLKB cycle.
Note 2. t_{NMICK} indicates the cycle of the NMI digital filter sampling clock.
Note 3. t_{IRQCK} indicates the cycle of the IRQi digital filter sampling clock.

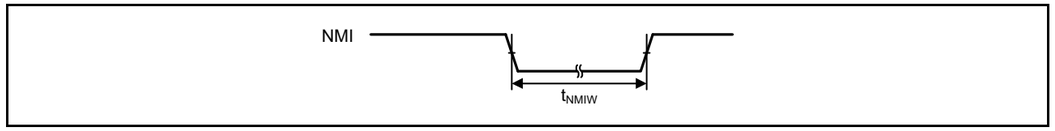


Figure 60.18 NMI interrupt input timing

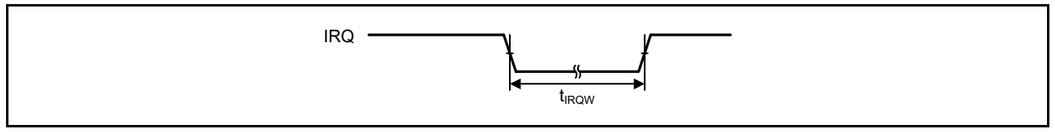


Figure 60.19 IRQ interrupt input timing

60.3.6 Bus Timing

Table 60.18 Bus timing (1 of 2)
Condition 1: When using the CS area controller (CSC).
BCLK = 8 to 120 MHz, EBCLK = 8 to 60 MHz
VCC = AVCC0 = VCC_USB = VBATT = 2.7 to 3.6 V, VREFH/VREFH0 = 2.7 V to AVCC0,
VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V
Output load conditions: VOH = VCC × 0.5, VOL = VCC × 0.5, C = 30 pF
EBCLK: High drive output is selected in the port drive capability bit in the PmnPFS register.
Others: Middle drive output is selected in the port drive capability bit in the PmnPFS register.

Condition 2: When using the SDRAM area controller (SDRAMC).
BCLK = SDCLK = 8 to 120 MHz
VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6 V, VREFH/VREFH0 = 3.0 V to AVCC0,
VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V
Output load conditions: VOH = VCC × 0.5, VOL = VCC × 0.5, C = 15 pF
High drive output is selected in the port drive capability bit in the PmnPFS register.

Condition 3: When using the SDRAM area controller (SDRAMC) and CS area controller (CSC) simultaneously.
BCLK = SDCLK = 8 to 60 MHz
VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6 V, VREFH/VREFH0 = 3.0 V to AVCC0,
VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V
Output load conditions: VOH = VCC × 0.5, VOL = VCC × 0.5, C = 15 pF
High drive output is selected in the port drive capability bit in the PmnPFS register.

Parameter	Symbol	Min	Max	Unit	Test conditions
Address delay	t_{AD}	-	12.5	ns	Figure 60.20 to Figure 60.25
Byte control delay	t_{BCD}	-	12.5	ns	
CS delay	t_{CSD}	-	12.5	ns	
ALE delay time	t_{ALED}	-	12.5	ns	
RD delay	t_{RSD}	-	12.5	ns	
Read data setup time	t_{RDS}	12.5	-	ns	
Read data hold time	t_{RDH}	0	-	ns	
WR/WRn delay	t_{WRD}	-	12.5	ns	
Write data delay	t_{WDD}	-	12.5	ns	
Write data hold time	t_{WDH}	0	-	ns	
WAIT setup time	t_{WTS}	12.5	-	ns	Figure 60.26
WAIT hold time	t_{WTH}	0	-	ns	

Note 1. tPcyc表示PCLKB周期。
Note 2. tNMICK表示NMI数字滤波器采样时钟的周期。
Note 3. tIRQCK表示IRQi数字滤波器采样时钟的周期。

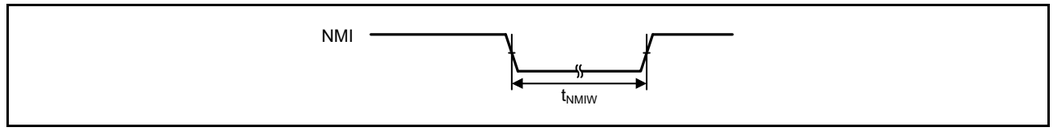


Figure 60.18 NMI中断输入时序

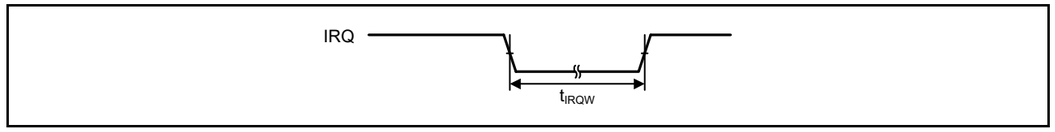


Figure 60.19 IRQ中断输入时序

60.3.6 巴士时间

Table 60.18 巴士计时（1of2）
条件1：使用CS区域控制器(CSC)时。
BCLK = 8 to 120 MHz, EBCLK = 8 to 60 MHz
VCC = AVCC0 = VCC_USB = VBATT = 2.7 to 3.6 V, VREFH/VREFH0 = 2.7 V to AVCC0,
VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V
输出负载条件：VOH=VCC×0.5，VOL=VCC×0.5，C=30pF
EBCLK：在PmnPFS寄存器的端口驱动能力位中选择高驱动输出。其他：中间驱动输出在PmnPFS寄存器的端口驱动能力位中选择。

条件2：使用SDRAM区域控制器(SDRAMC)时。
BCLK = SDCLK = 8 to 120 MHz
VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6 V, VREFH/VREFH0 = 3.0 V to AVCC0,
VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V
输出负载条件：VOH=VCC×0.5，VOL=VCC×0.5，C=15pF
在PmnPFS寄存器的端口驱动能力位中选择高驱动输出。

条件3：同时使用SDRAM区域控制器(SDRAMC)和CS区域控制器(CSC)时。
BCLK = SDCLK = 8 to 60 MHz
VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6 V, VREFH/VREFH0 = 3.0 V to AVCC0,
VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V
输出负载条件：VOH=VCC×0.5，VOL=VCC×0.5，C=15pF
在PmnPFS寄存器的端口驱动能力位中选择高驱动输出。

Parameter	Symbol	Min	Max	Unit	测试条件
地址延迟	t_{AD}	-	12.5	ns	图60.20至 Figure 60.25
字节控制延迟	t_{BCD}	-	12.5	ns	
CS delay	t_{CSD}	-	12.5	ns	
ALE延迟时间	t_{ALED}	-	12.5	ns	
RD delay	t_{RSD}	-	12.5	ns	
读取数据建立时间	t_{RDS}	12.5	-	ns	
读取数据保持时间	t_{RDH}	0	-	ns	
WR/WRn delay	t_{WRD}	-	12.5	ns	
写数据延迟	t_{WDD}	-	12.5	ns	
写数据保持时间	t_{WDH}	0	-	ns	
等待设置时间	t_{WTS}	12.5	-	ns	Figure 60.26
WAIT保持时间	t_{WTH}	0	-	ns	

Table 60.18 Bus timing (2 of 2)

Condition 1: When using the CS area controller (CSC).
BCLK = 8 to 120 MHz, EBCLK = 8 to 60 MHz
VCC = AVCC0 = VCC_USB = VBATT = 2.7 to 3.6 V, VREFH/VREFH0 = 2.7 V to AVCC0,
VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V
Output load conditions: VOH = VCC × 0.5, VOL = VCC × 0.5, C = 30 pF
EBCLK: High drive output is selected in the port drive capability bit in the PmnPFS register.
Others: Middle drive output is selected in the port drive capability bit in the PmnPFS register.

Condition 2: When using the SDRAM area controller (SDRAMC).
BCLK = SDCLK = 8 to 120 MHz
VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6 V, VREFH/VREFH0 = 3.0 V to AVCC0,
VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V
Output load conditions: VOH = VCC × 0.5, VOL = VCC × 0.5, C = 15 pF
High drive output is selected in the port drive capability bit in the PmnPFS register.

Condition 3: When using the SDRAM area controller (SDRAMC) and CS area controller (CSC) simultaneously.
BCLK = SDCLK = 8 to 60 MHz
VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6 V, VREFH/VREFH0 = 3.0 V to AVCC0,
VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V
Output load conditions: VOH = VCC × 0.5, VOL = VCC × 0.5, C = 15 pF
High drive output is selected in the port drive capability bit in the PmnPFS register.

Parameter	Symbol	Min	Max	Unit	Test conditions
Address delay 2 (SDRAM)	t_{AD2}	0.8	6.8	ns	Figure 60.27 to Figure 60.33
CS delay 2 (SDRAM)	t_{CSD2}	0.8	6.8	ns	
DQM delay (SDRAM)	t_{DQMD}	0.8	6.8	ns	
CKE delay (SDRAM)	t_{CKED}	0.8	6.8	ns	
Read data setup time 2 (SDRAM)	t_{RDS2}	2.9	-	ns	
Read data hold time 2 (SDRAM)	t_{RDH2}	1.5	-	ns	
Write data delay 2 (SDRAM)	t_{WDD2}	-	6.8	ns	
Write data hold time 2 (SDRAM)	t_{WDH2}	0.8	-	ns	
WE delay (SDRAM)	t_{WED}	0.8	6.8	ns	
RAS delay (SDRAM)	t_{RASD}	0.8	6.8	ns	
CAS delay (SDRAM)	t_{CASD}	0.8	6.8	ns	

Table 60.18 巴士计时（2之2）

条件1：使用CS区域控制器(CSC)时。
BCLK = 8 to 120 MHz, EBCLK = 8 to 60 MHz
VCC = AVCC0 = VCC_USB = VBATT = 2.7 to 3.6 V, VREFH/VREFH0 = 2.7 V to AVCC0,
VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V
输出负载条件：VOH=VCC×0.5，VOL=VCC×0.5，C=30pF
EBCLK：在PmnPFS寄存器的端口驱动能力位中选择高驱动输出。其他：中间驱动输出在PmnPFS寄存器的端口驱动能力位中选择。

条件2：使用SDRAM区域控制器(SDRAMC)时。
BCLK = SDCLK = 8 to 120 MHz
VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6 V, VREFH/VREFH0 = 3.0 V to AVCC0,
VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V
输出负载条件：VOH=VCC×0.5，VOL=VCC×0.5，C=15pF
在PmnPFS寄存器的端口驱动能力位中选择高驱动输出。

条件3：同时使用SDRAM区域控制器(SDRAMC)和CS区域控制器(CSC)时。
BCLK = SDCLK = 8 to 60 MHz
VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6 V, VREFH/VREFH0 = 3.0 V to AVCC0,
VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V
输出负载条件：VOH=VCC×0.5，VOL=VCC×0.5，C=15pF
在PmnPFS寄存器的端口驱动能力位中选择高驱动输出。

Parameter	Symbol	Min	Max	Unit	测试条件
地址延迟2(SDRAM)	t_{AD2}	0.8	6.8	ns	图60.27至 Figure 60.33
CS delay 2 (SDRAM)	t_{CSD2}	0.8	6.8	ns	
DQM delay (SDRAM)	t_{DQMD}	0.8	6.8	ns	
CKE delay (SDRAM)	t_{CKED}	0.8	6.8	ns	
读取数据建立时间2(SDRAM)	t_{RDS2}	2.9	-	ns	
读取数据保持时间2(SDRAM)	t_{RDH2}	1.5	-	ns	
写入数据延迟2(SDRAM)	t_{WDD2}	-	6.8	ns	
写数据保持时间2(SDRAM)	t_{WDH2}	0.8	-	ns	
WE延迟(SDRAM)	t_{WED}	0.8	6.8	ns	
RAS延迟(SDRAM)	t_{RASD}	0.8	6.8	ns	
CAS延迟(SDRAM)	t_{CASD}	0.8	6.8	ns	

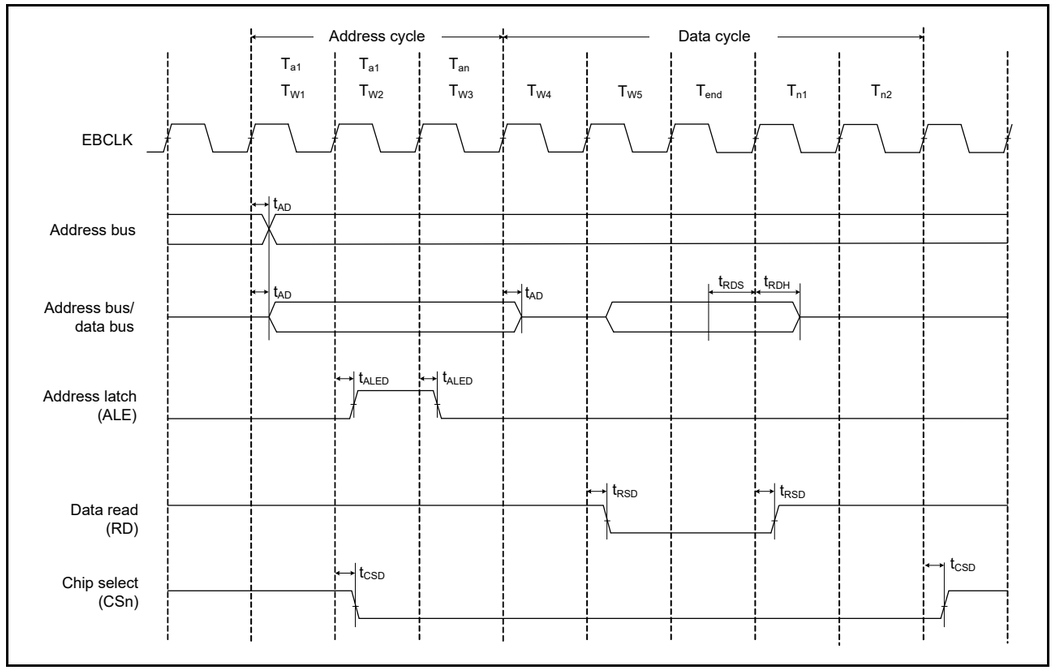


Figure 60.20 Address/data multiplexed bus read access timing

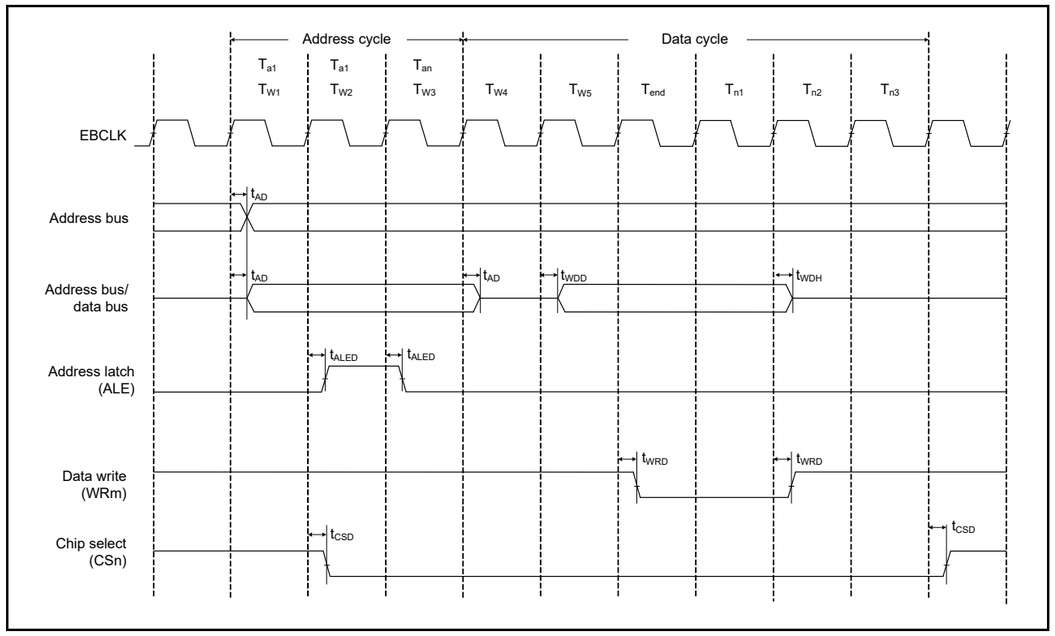


Figure 60.21 Address/data multiplexed bus write access timing

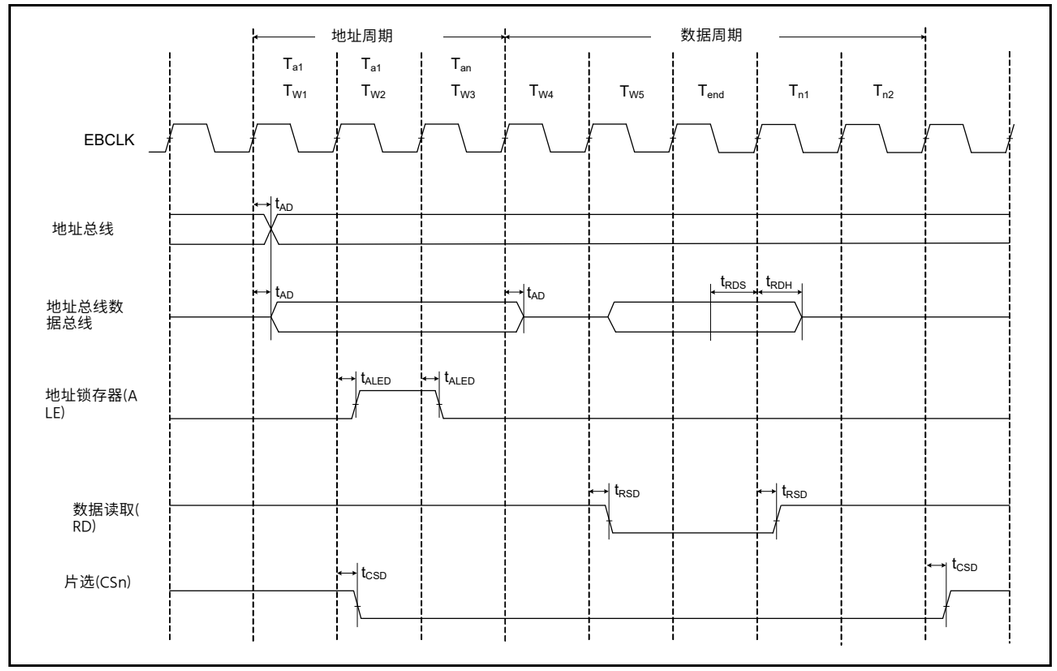


Figure 60.20 地址数据复用总线读访问时序

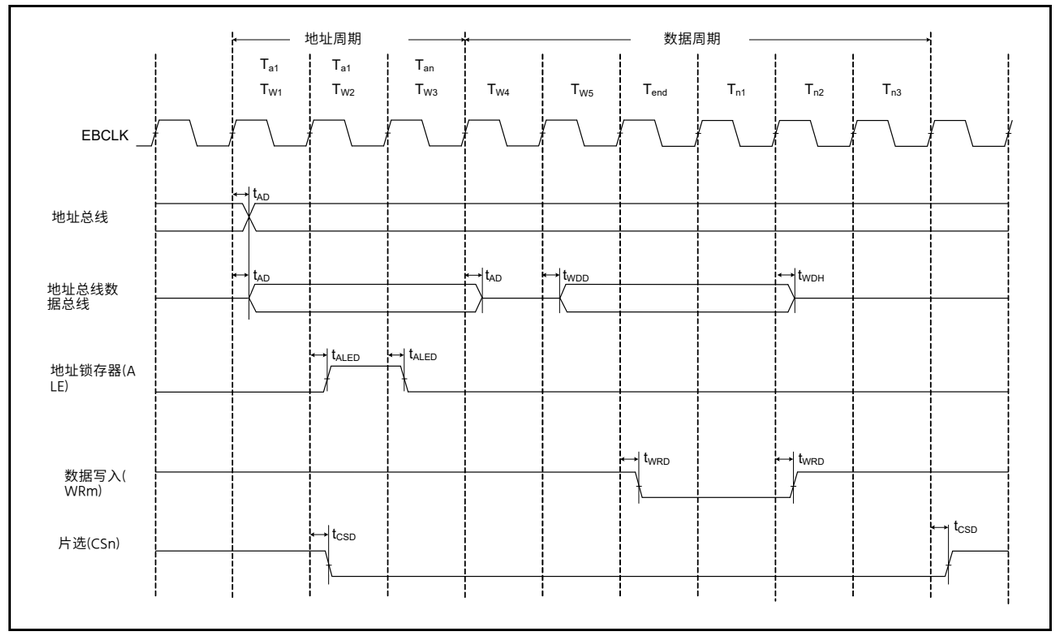


Figure 60.21 地址数据复用总线写访问时序

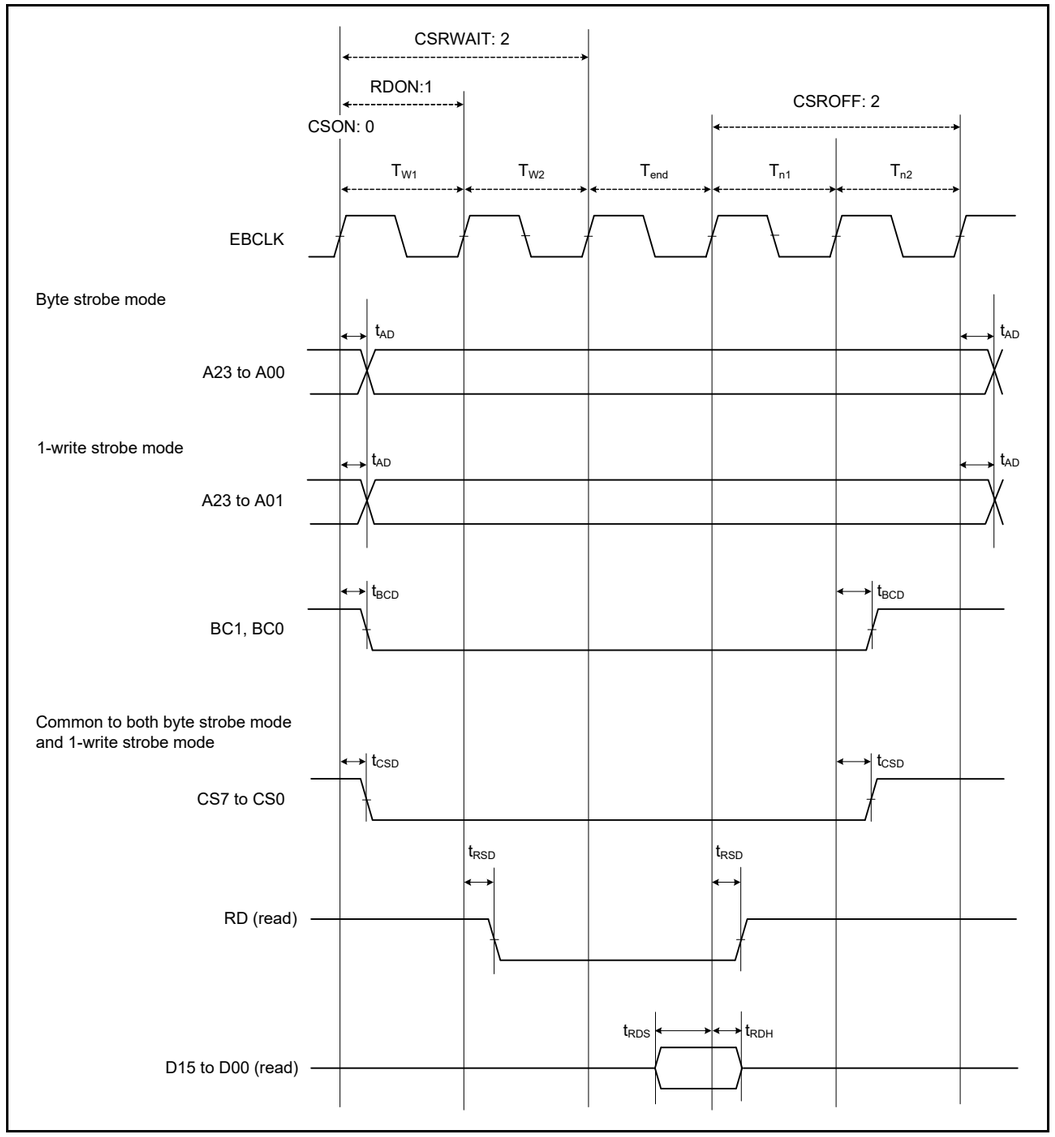


Figure 60.22 External bus timing for normal read cycle with bus clock synchronized

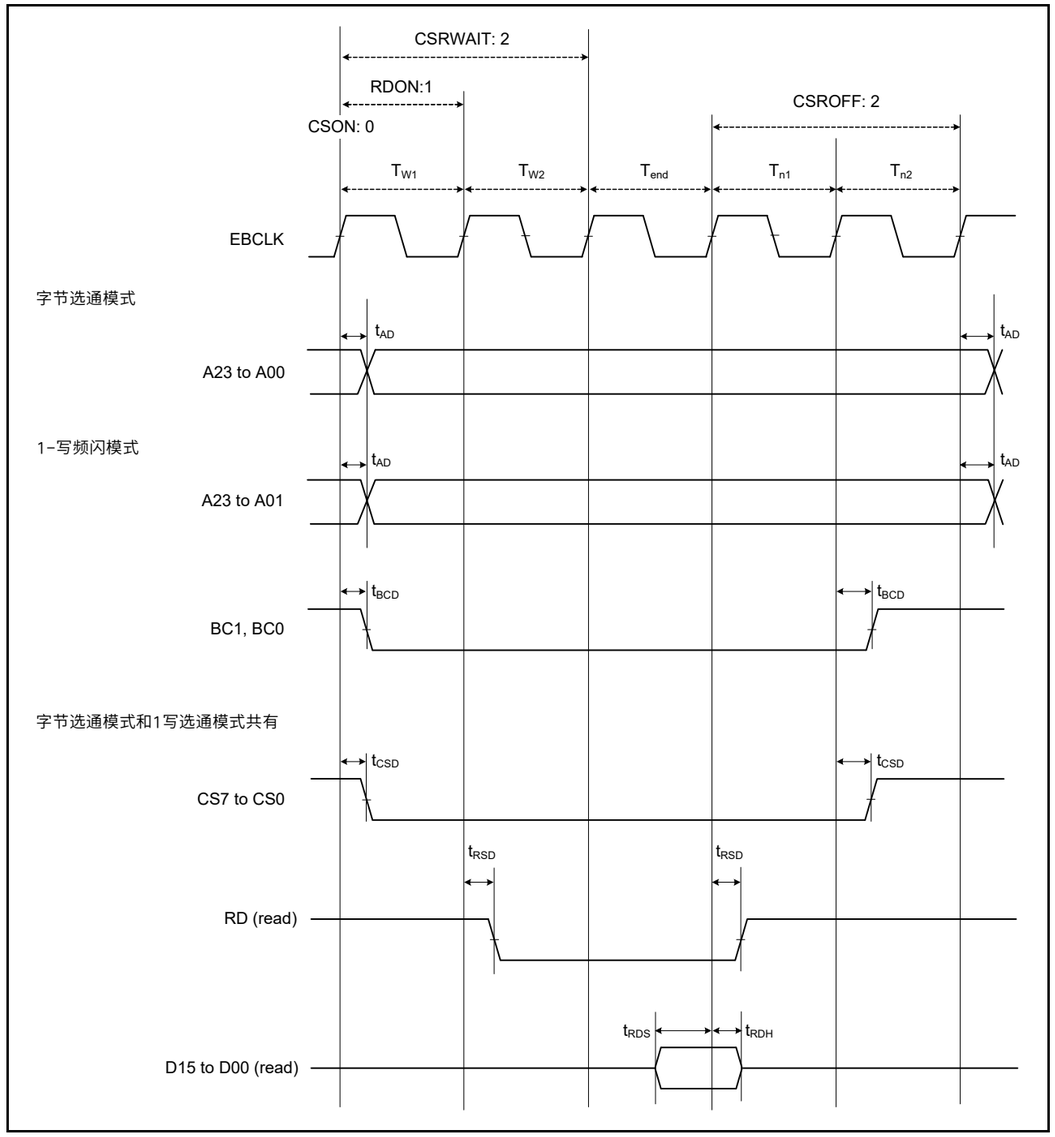
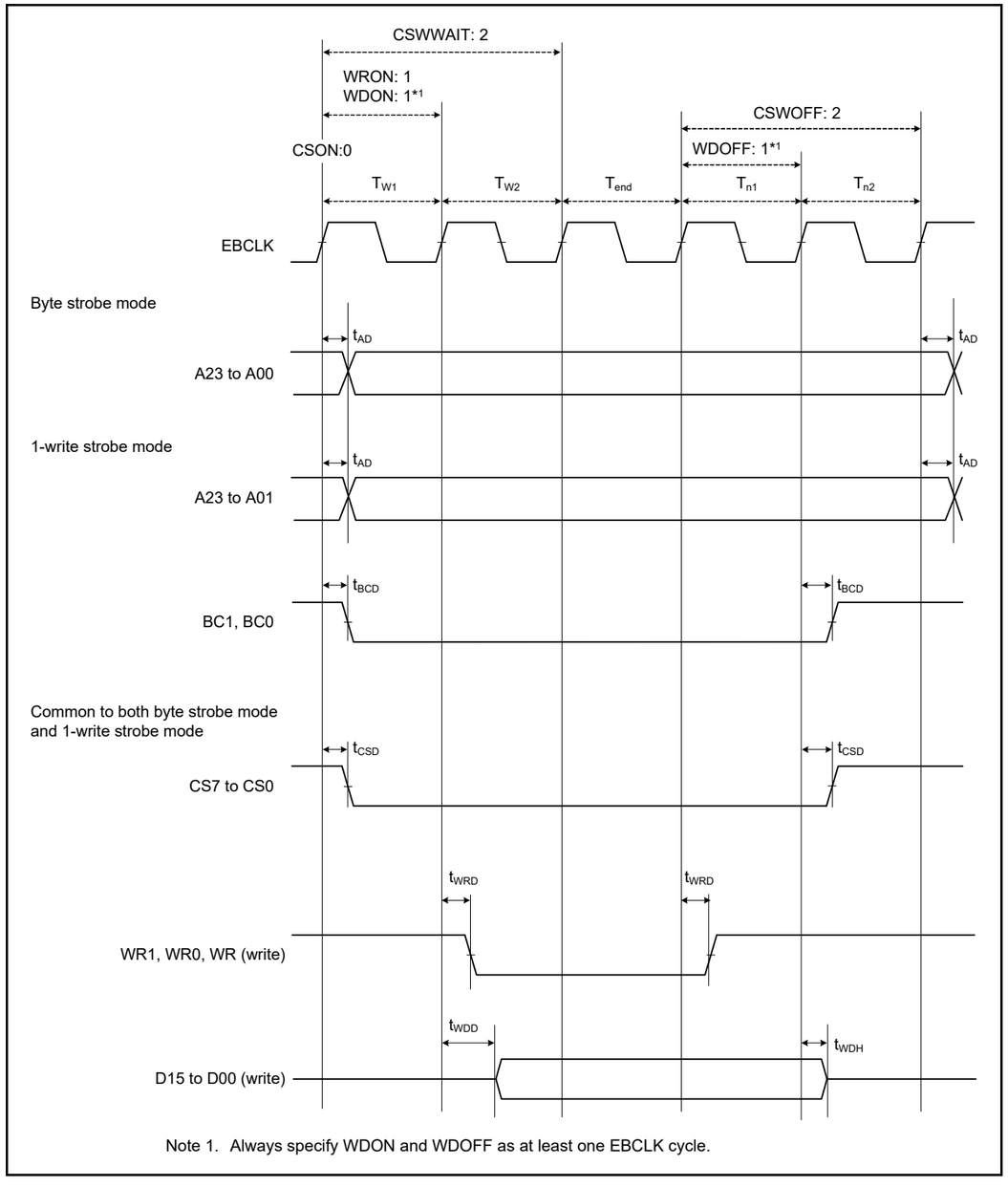
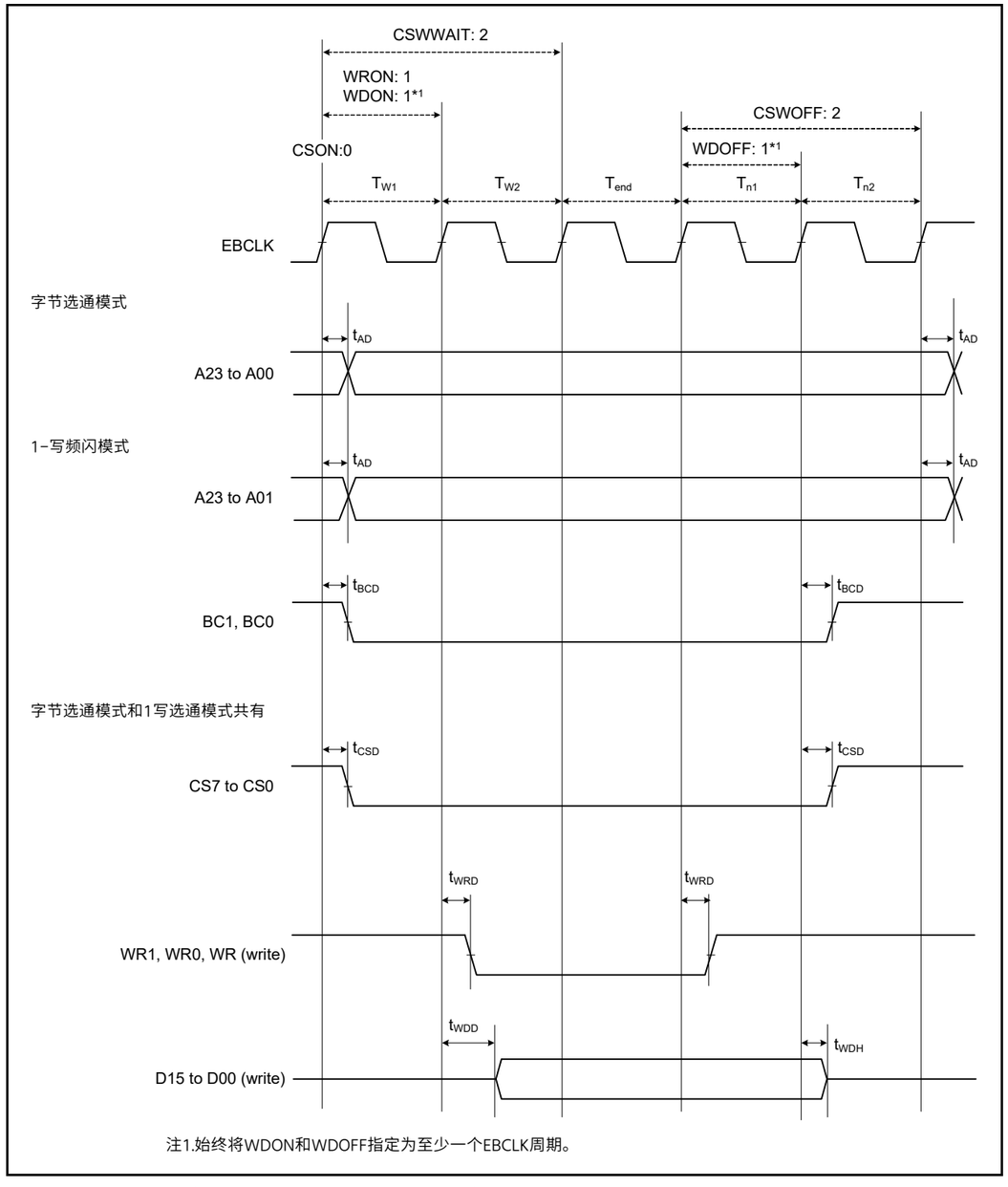


Figure 60.22 正常读取周期的外部总线时序与总线时钟同步



Note 1. Always specify WDON and WDOFF as at least one EBCLK cycle.

Figure 60.23 External bus timing for normal write cycle with bus clock synchronized



注1.始终将WDON和WDOFF指定为至少一个EBCLK周期。

Figure 60.23 与总线时钟同步的正常写周期的外部总线时序

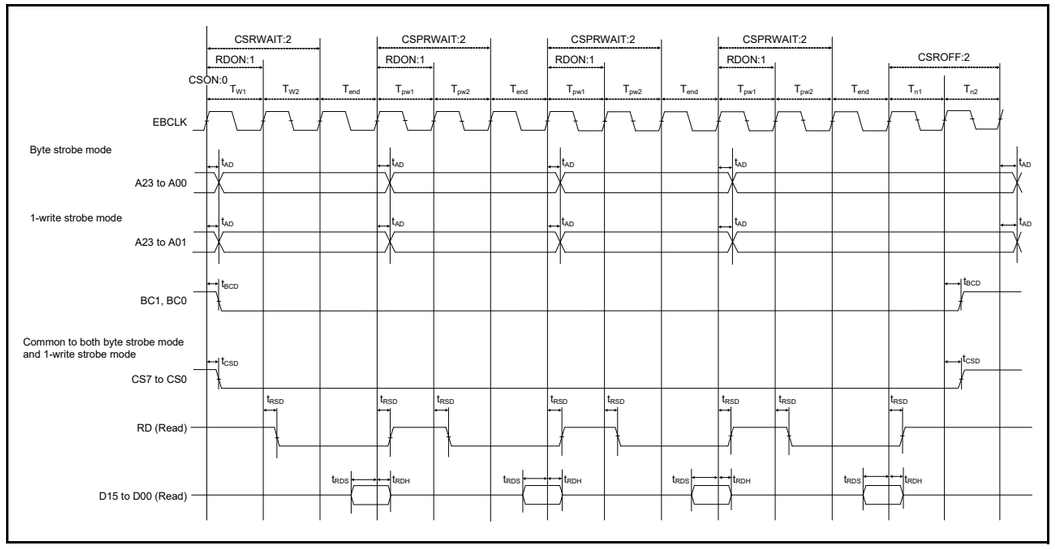


Figure 60.24 External bus timing for page read cycle with bus clock synchronized

Note 1. Always specify WDON and WDOFF as at least one EBCLK cycle.

Figure 60.25 External bus timing for page write cycle with bus clock synchronized

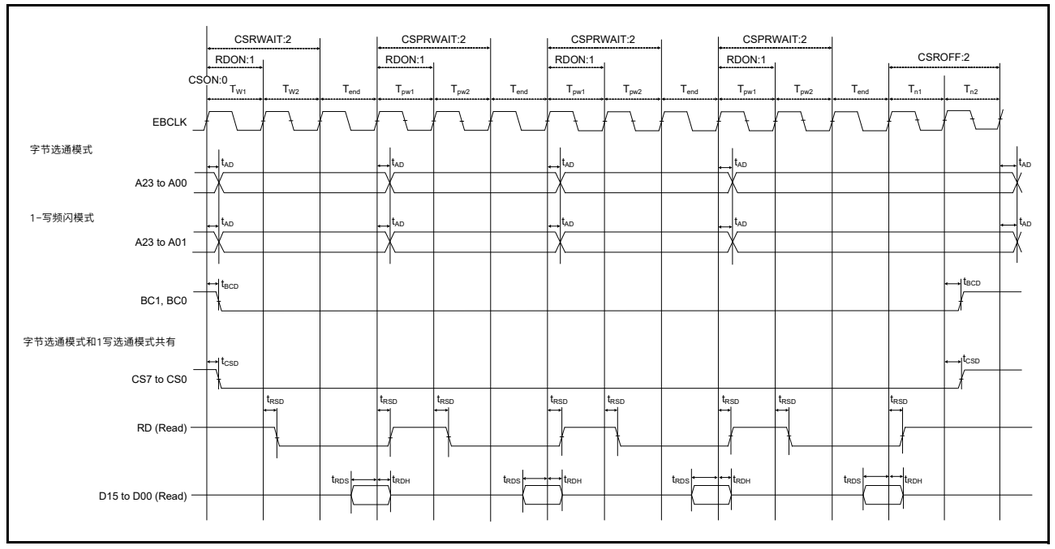
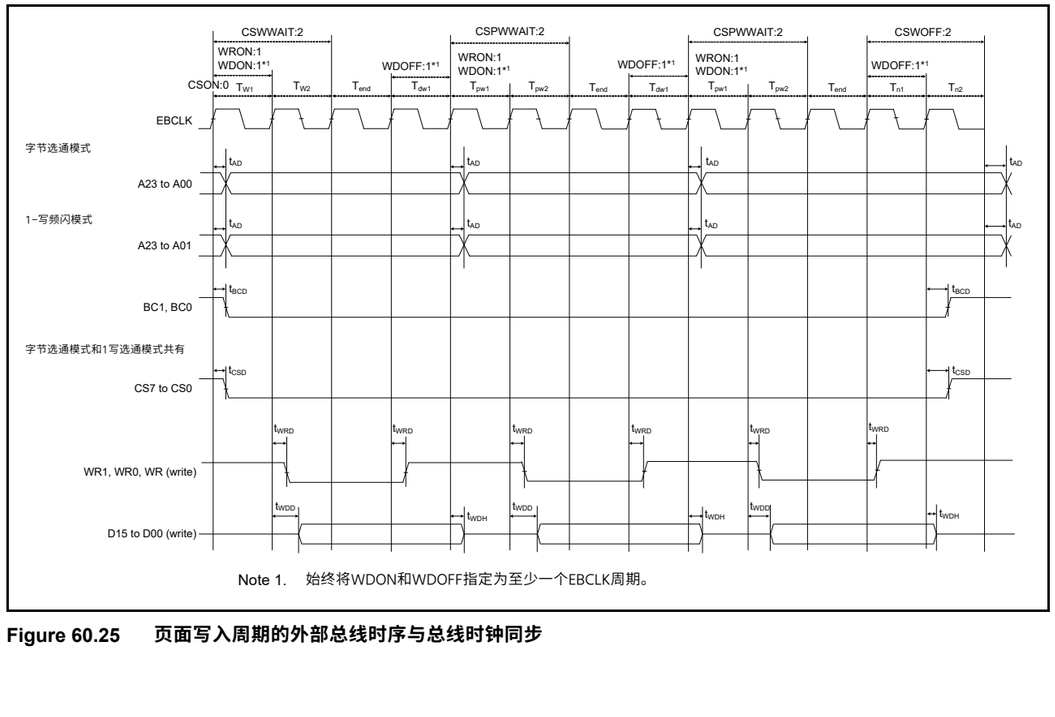


Figure 60.24 页面读取周期的外部总线时序与总线时钟同步



Note 1. 始终将WDON和WDOFF指定为至少一个EBCLK周期。

Figure 60.25 页面写入周期的外部总线时序与总线时钟同步

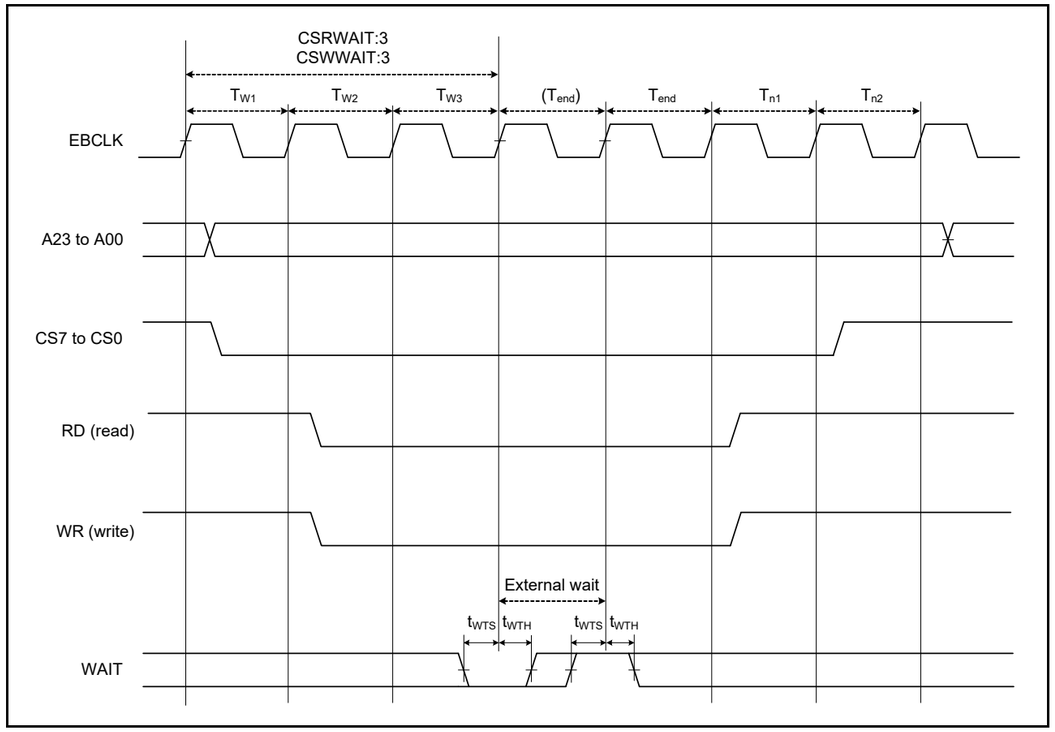


Figure 60.26 External bus timing for external wait control

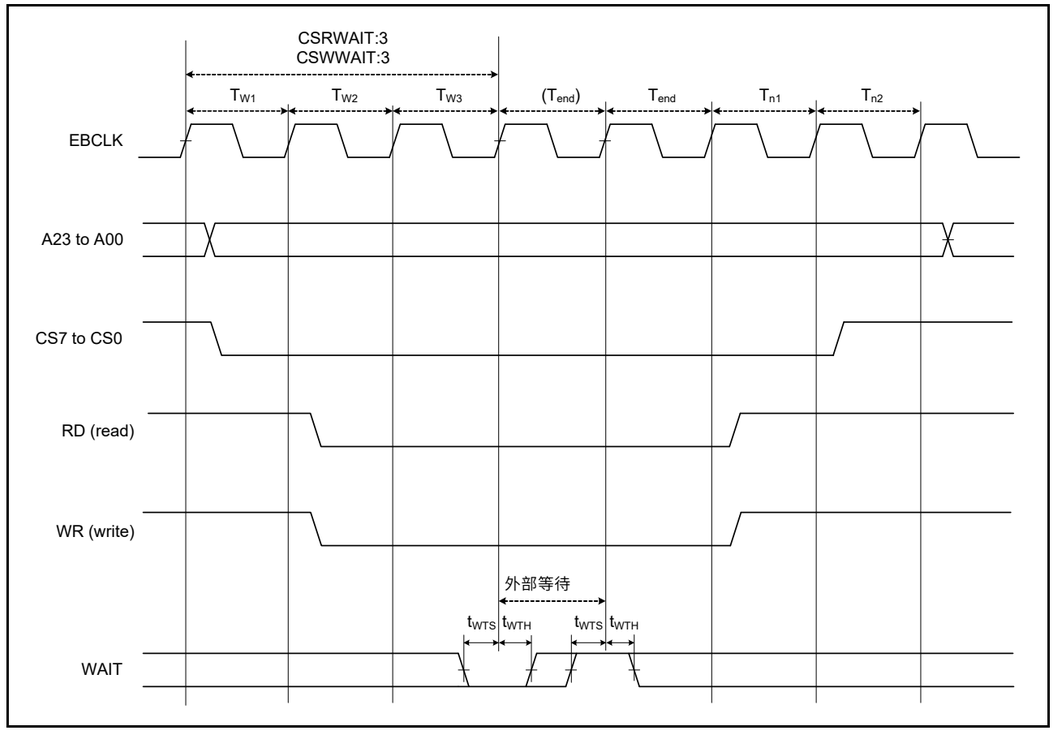
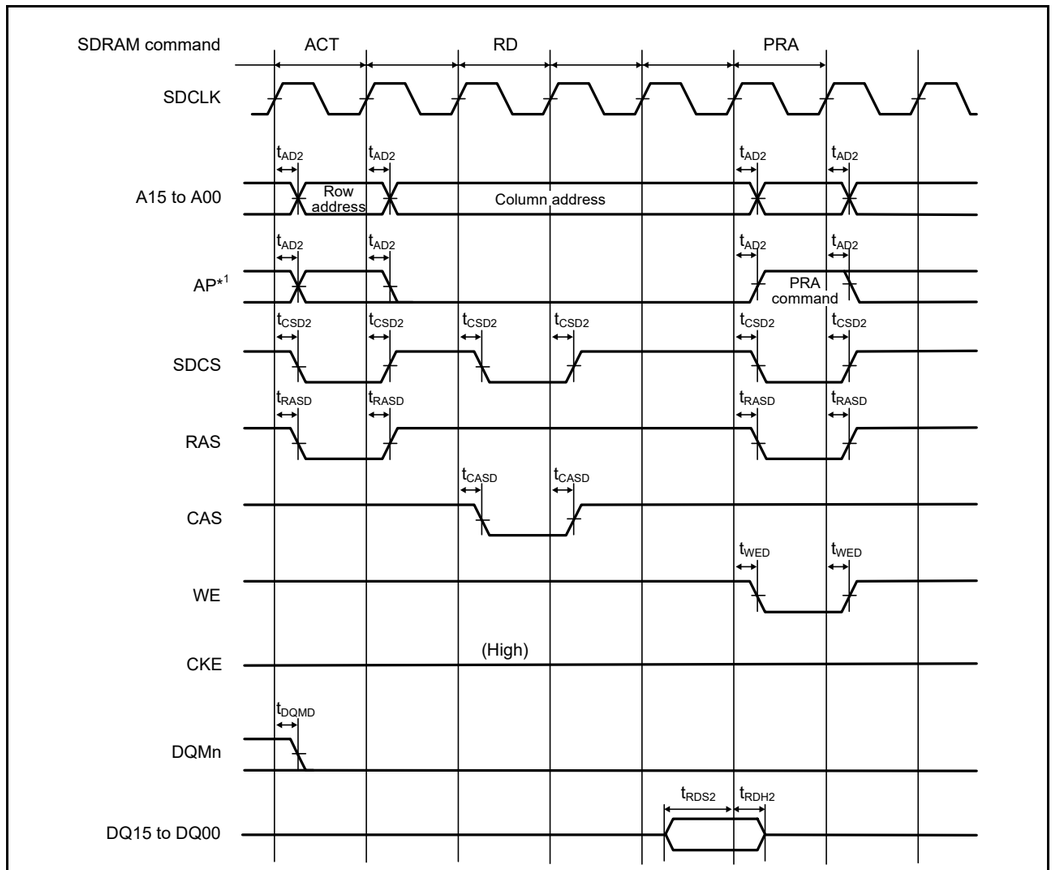
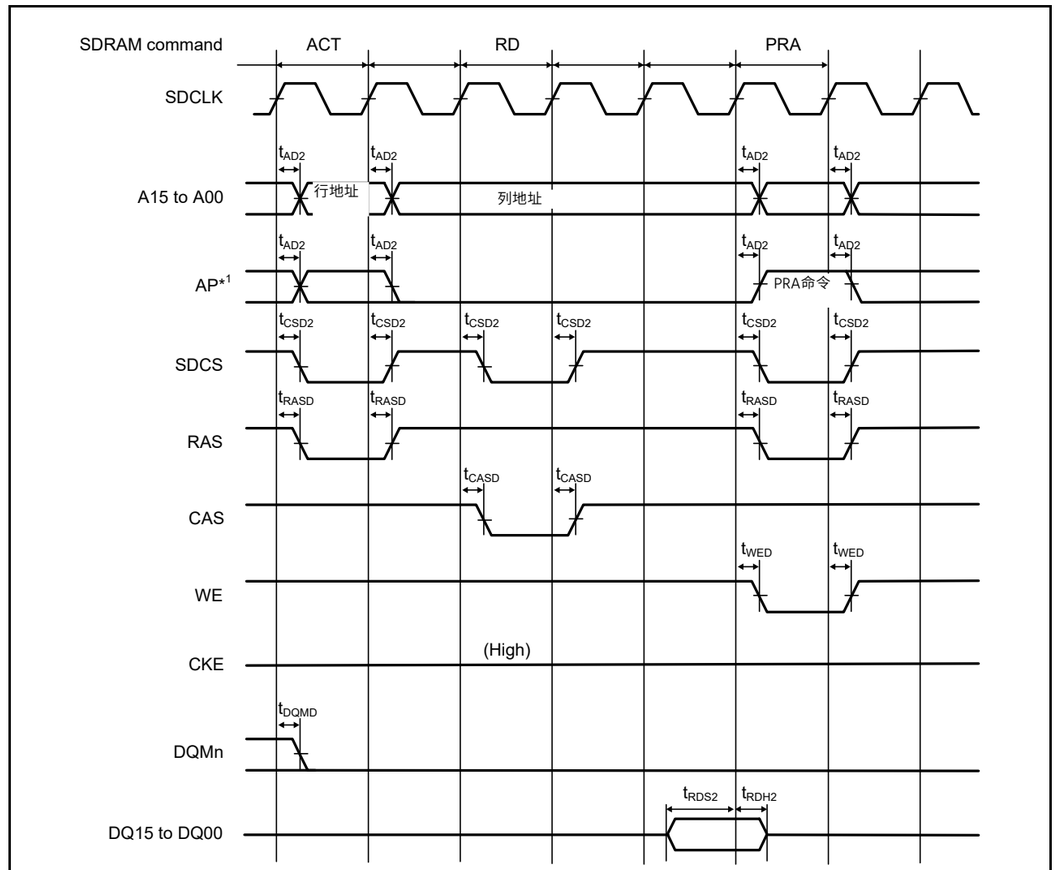


Figure 60.26 外部等待控制的外部总线时序



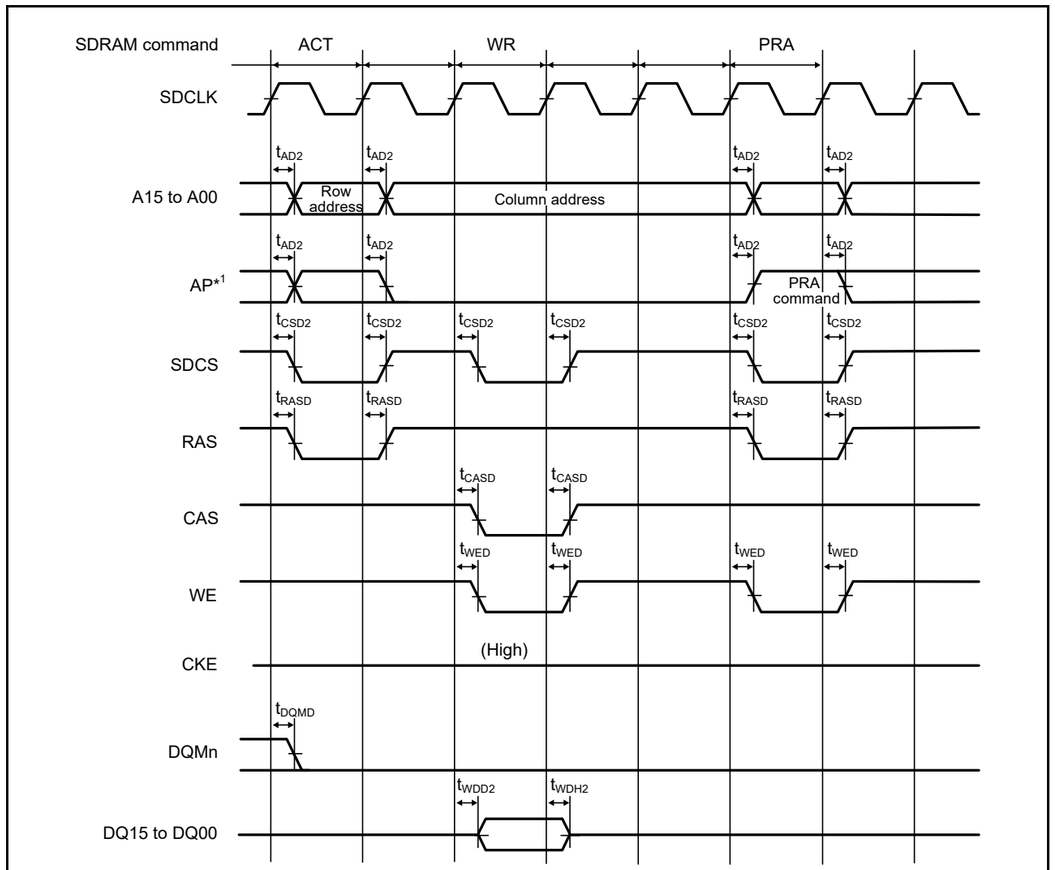
Note 1. Address pins are for output of the precharge-select command (Precharge-sel) for the SDRAM.

Figure 60.27 SDRAM single read timing



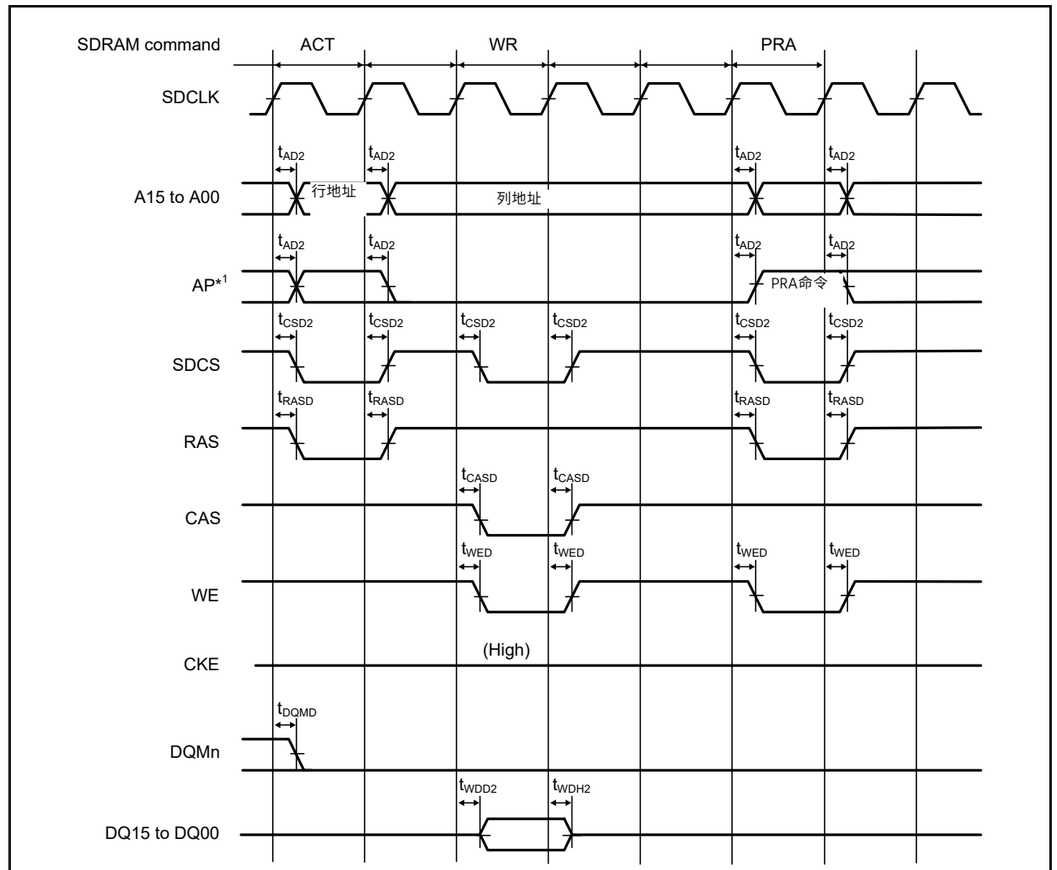
注1.地址引脚用于输出SDRAM的预充电选择命令(Precharge-sel)。

Figure 60.27 SDRAM单次读取时序



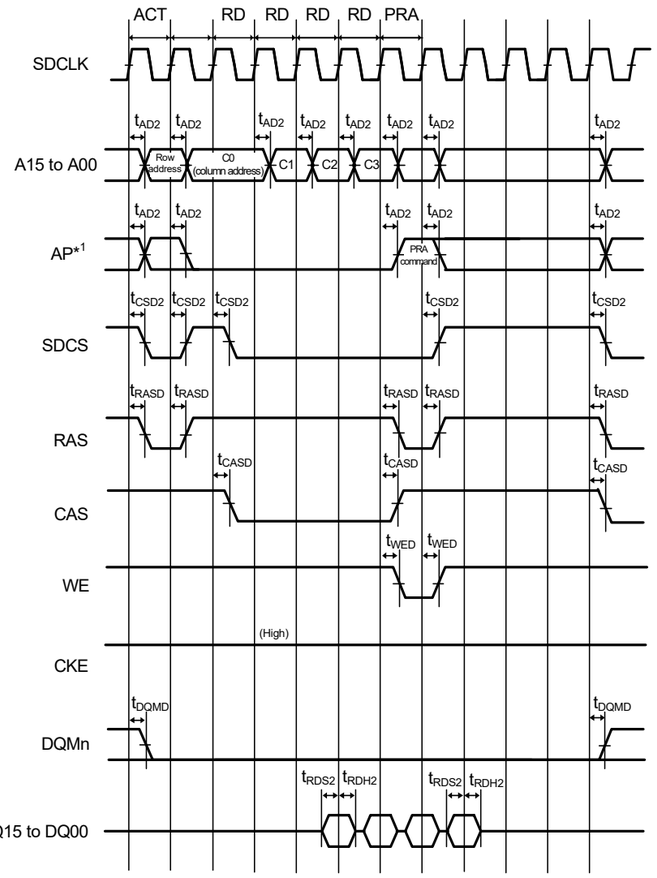
Note 1. Address pins are for output of the precharge-select command (Precharge-sel) for the SDRAM.

Figure 60.28 SDRAM single write timing



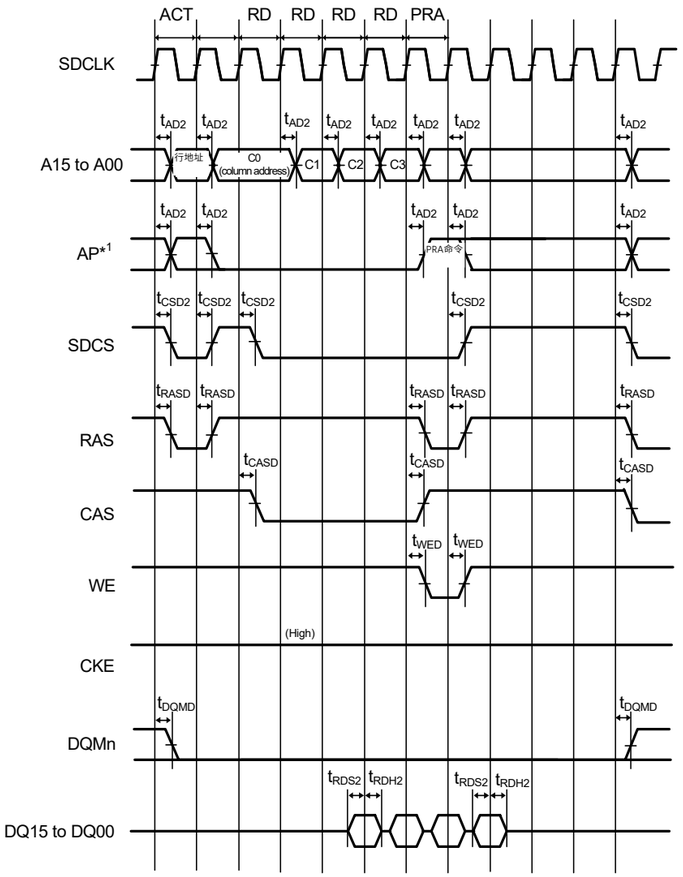
注1.地址引脚用于输出SDRAM的预充电选择命令(Precharge-sel)。

Figure 60.28 SDRAM单次写入时序



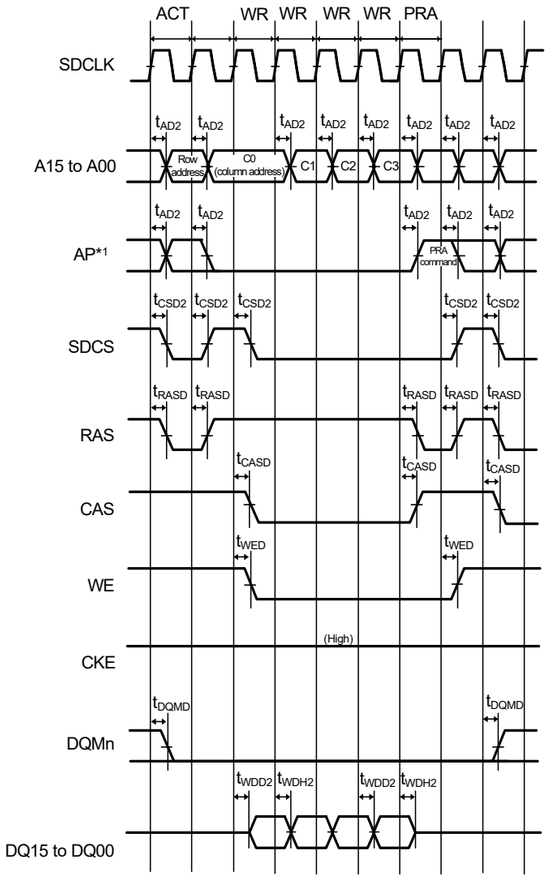
Note 1. Address pins are for output of the precharge-select command (Precharge-sel) for the SDRAM.

Figure 60.29 SDRAM multiple read timing



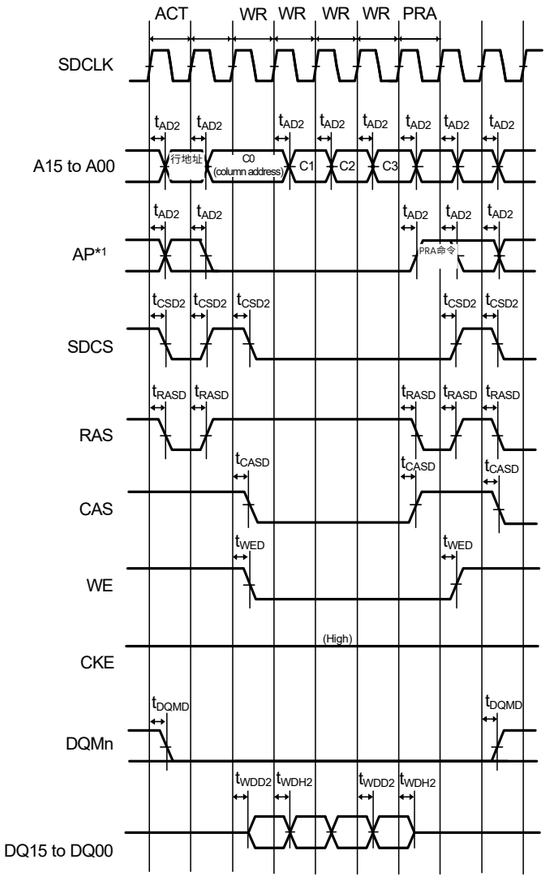
注1.地址引脚用于输出SDRAM的预充电选择命令(Precharge-sel)。

Figure 60.29 SDRAM多读时序



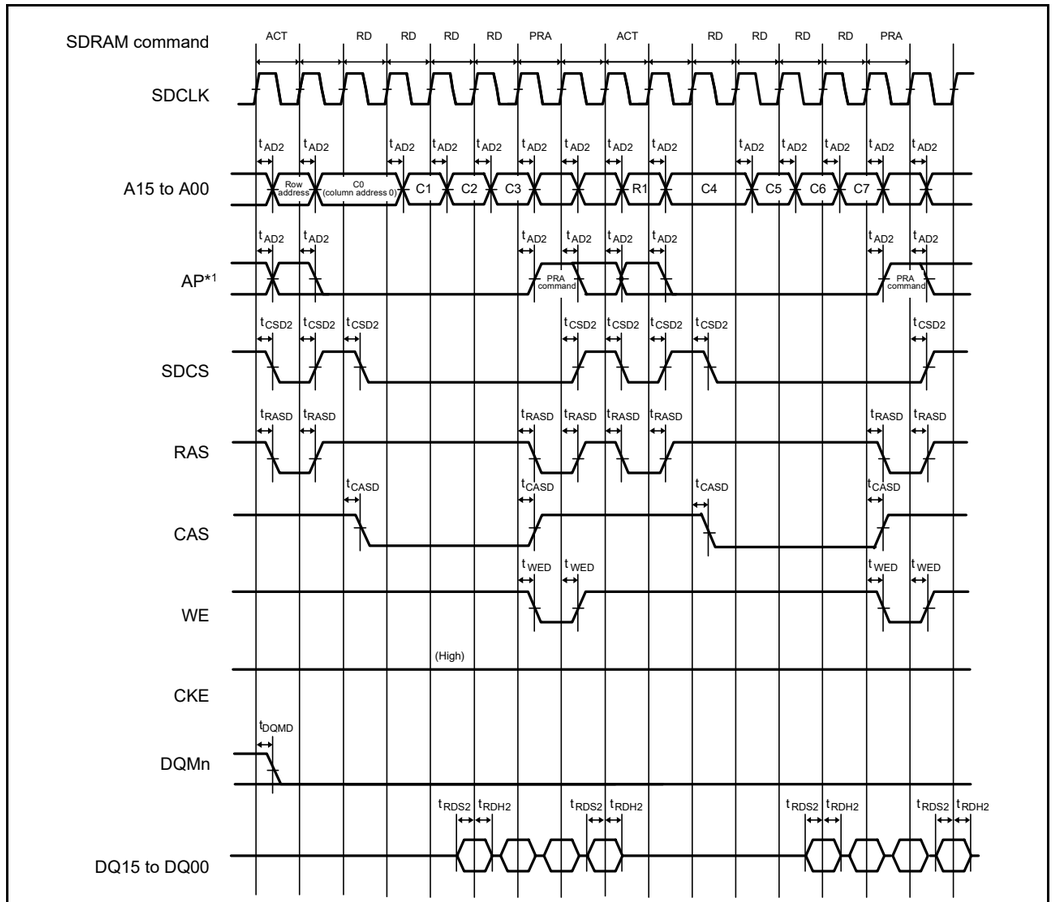
Note 1. Address pins are for output of the precharge-select command (Precharge-sel) for the SDRAM.

Figure 60.30 SDRAM multiple write timing



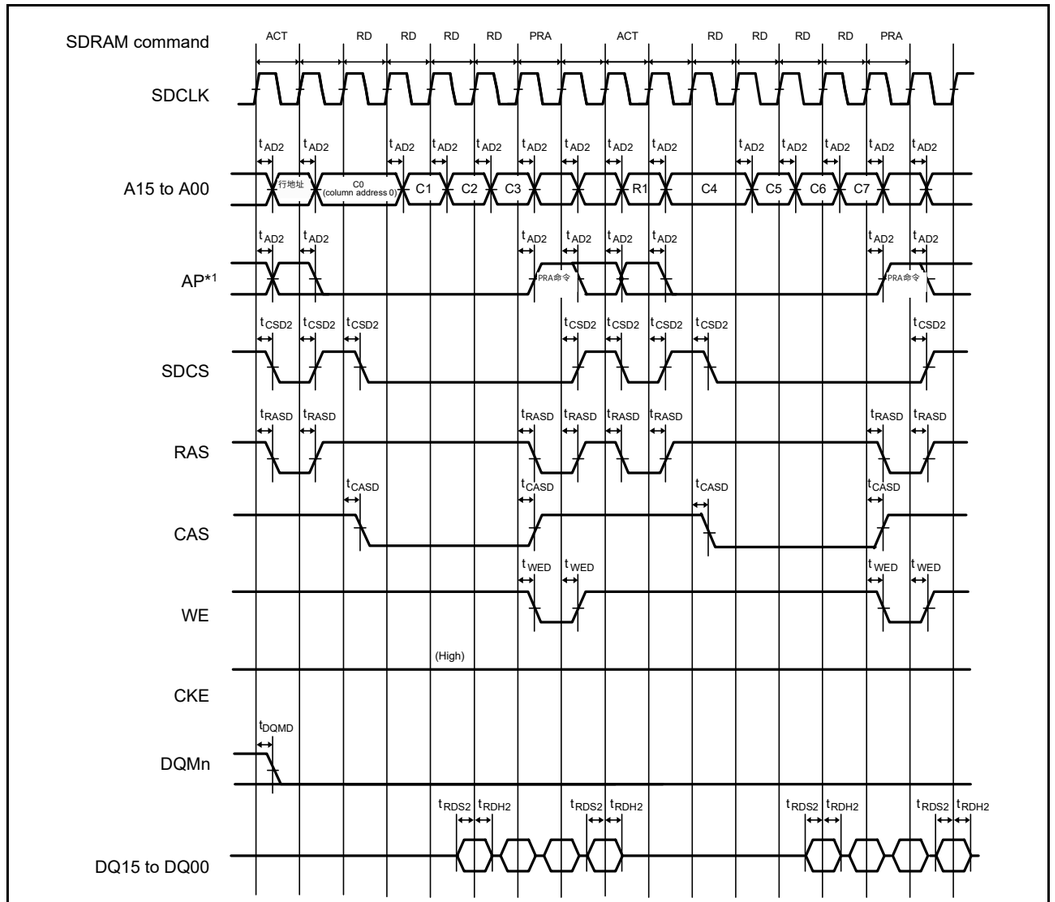
注1.地址引脚用于输出SDRAM的预充电选择命令(Precharge-sel)。

Figure 60.30 SDRAM多次写入时序



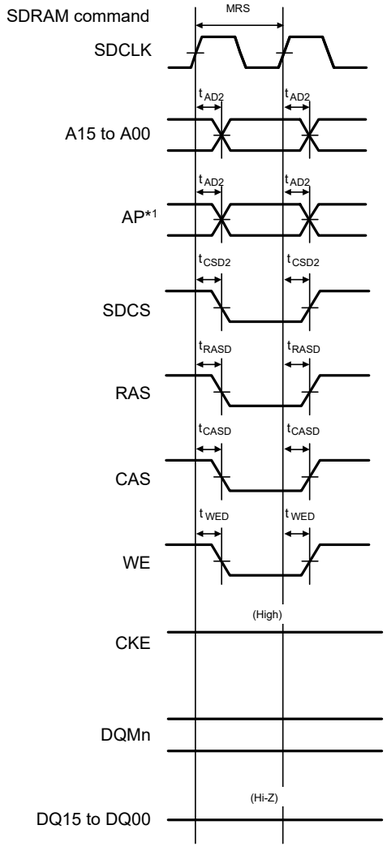
Note 1. Address pins are for output of the precharge-select command (Precharge-sel) for the SDRAM.

Figure 60.31 SDRAM multiple read line stride timing



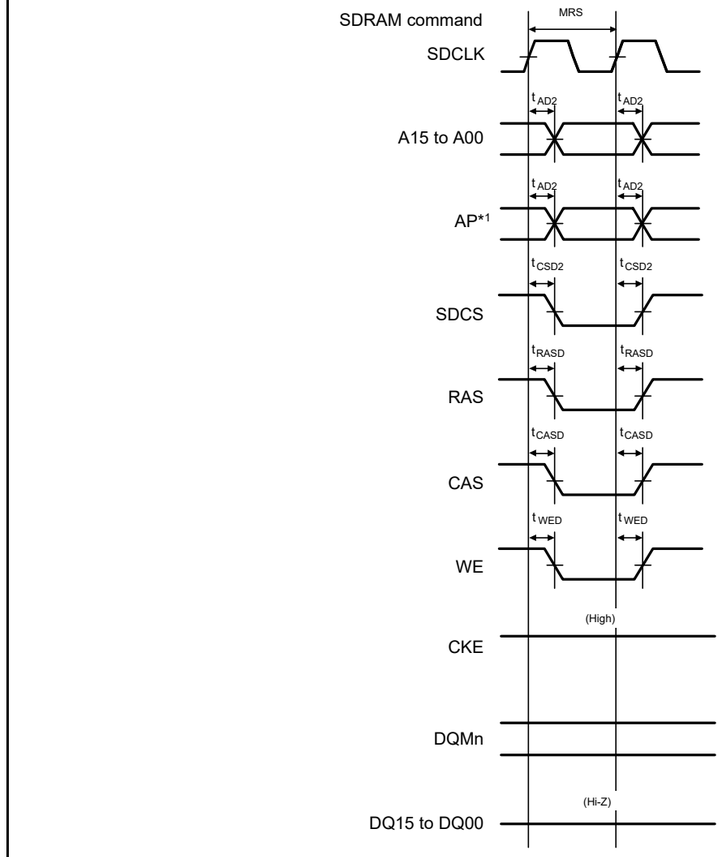
注1.地址引脚用于输出SDRAM的预充电选择命令(Precharge-sel)。

Figure 60.31 SDRAM多条读取线步幅时序



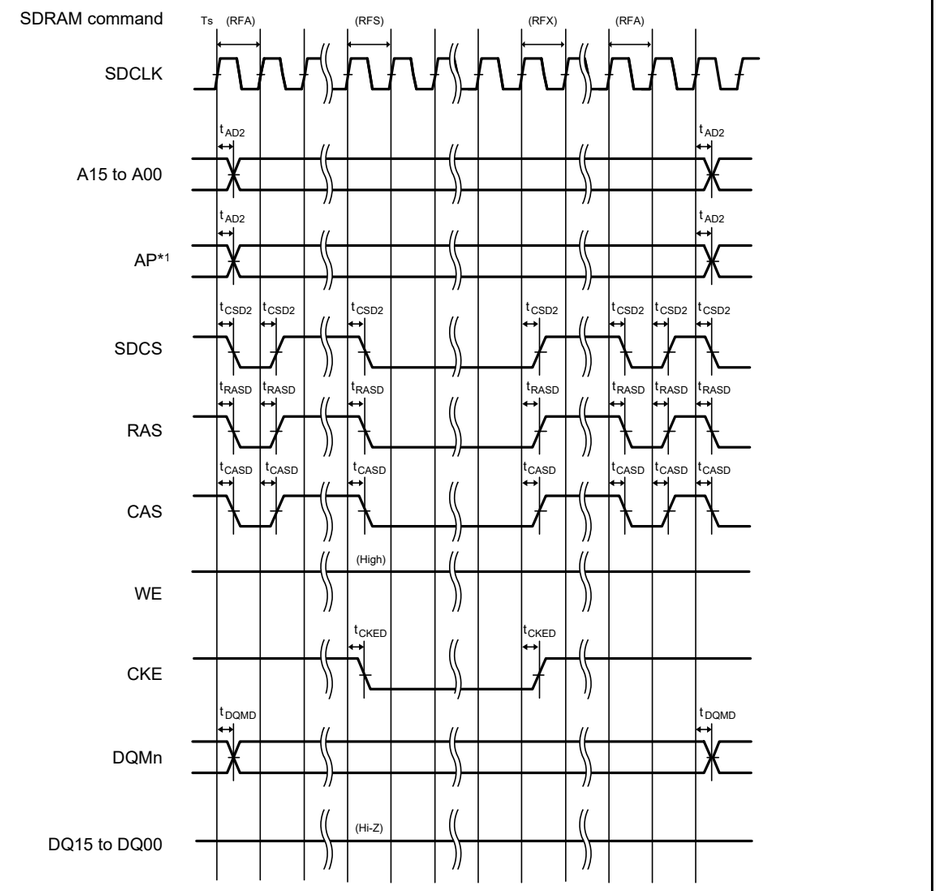
Note 1. Address pins are for output of the precharge-select command (Precharge-sel) for the SDRAM.

Figure 60.32 SDRAM mode register set timing



注1.地址引脚用于输出SDRAM的预充电选择命令(Precharge-sel)。

Figure 60.32 SDRAM模式寄存器设置时序



Note 1. Address pins are for output of the precharge-select command (Precharge-sel) for the SDRAM.

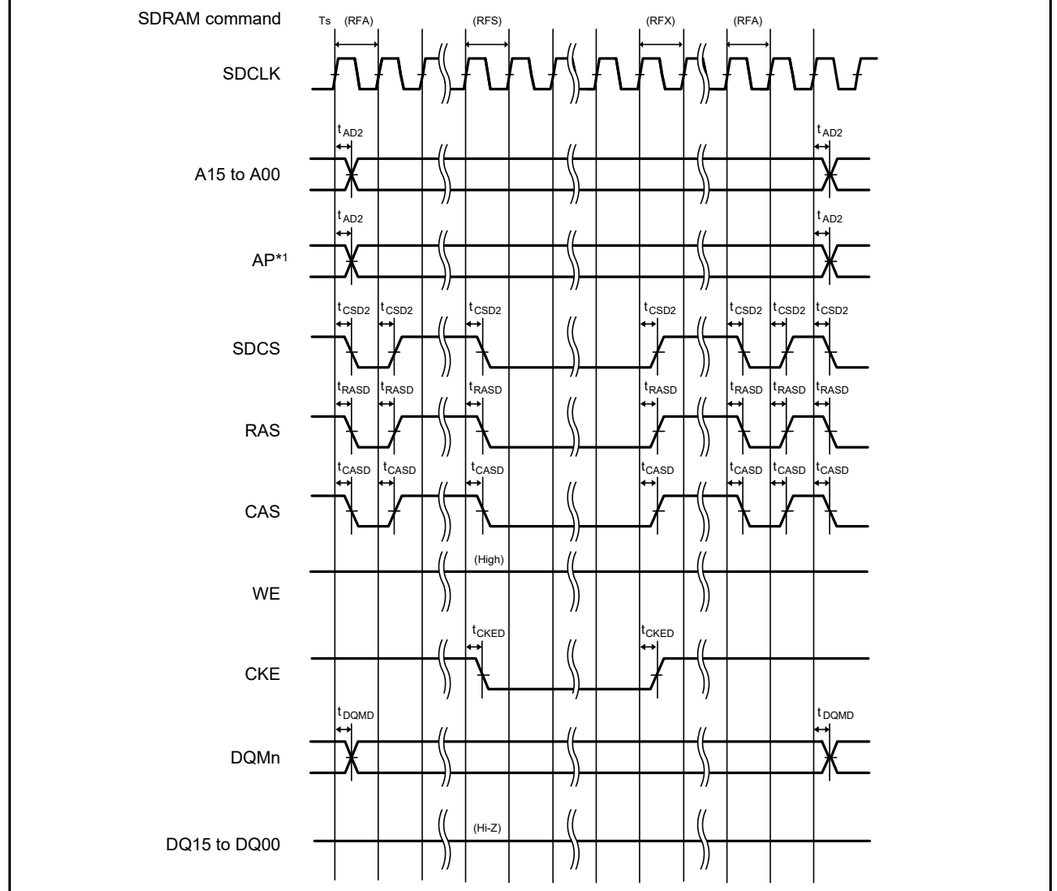
Figure 60.33 SDRAM self-refresh timing

60.3.7 I/O Ports, POEG, GPT32, AGT, KINT, and ADC12 Trigger Timing

Table 60.19 I/O ports, POEG, GPT32, AGT, KINT, and ADC12 trigger timing (1 of 2)
GPT32 Conditions:
High drive output is selected in the port drive capability bit in the PmnPFS register.

AGT Conditions:
Middle drive output is selected in the port drive capability bit in the PmnPFS register.

Parameter		Symbol	Min	Max	Unit	Test conditions
I/O ports	Input data pulse width	t_{PRW}	1.5	-	t_{Pcyc}	Figure 60.34
POEG	POEG input trigger pulse width	t_{POEW}	3	-	t_{Pcyc}	Figure 60.35



注1.地址引脚用于输出SDRAM的预充电选择命令(Precharge-sel)。

Figure 60.33 SDRAM self-refresh timing

60.3.7 IO端口、POEG、GPT32、AGT、KINT和ADC12触发时序

Table 60.19 IO端口、POEG、GPT32、AGT、KINT和ADC12触发时序（1of2）
GPT32 Conditions:
在PmnPFS寄存器的端口驱动能力位中选择高驱动输出。

AGT Conditions:
中间驱动输出在PmnPFS寄存器的端口驱动能力位中选择。

Parameter		Symbol	Min	Max	Unit	测试条件
I/O ports	输入数据脉冲宽度	t_{PRW}	1.5	-	t_{Pcyc}	Figure 60.34
POEG	POEG输入触发脉冲宽度	t_{POEW}	3	-	t_{Pcyc}	Figure 60.35

Table 60.19 I/O ports, POEG, GPT32, AGT, KINT, and ADC12 trigger timing (2 of 2)
GPT32 Conditions:
High drive output is selected in the port drive capability bit in the PmnPFS register.

AGT Conditions:
Middle drive output is selected in the port drive capability bit in the PmnPFS register.

Parameter			Symbol	Min	Max	Unit	Test conditions
GPT32	Input capture pulse width	Single edge	t_{GTICW}	1.5	-	t_{PDcyc}	Figure 60.36
		Dual edge		2.5	-		
	GTIOCxY output skew (x = 0 to 7, Y= A or B)	Middle drive buffer	t_{GTISK}*1	-	4	ns	Figure 60.37
		High drive buffer		-	4		
	GTIOCxY output skew (x = 8 to 13, Y = A or B)	Middle drive buffer		-	4		
		High drive buffer		-	4		
	GTIOCxY output skew (x = 0 to 13, Y = A or B)	Middle drive buffer		-	6		
		High drive buffer		-	6		
	OPS output skew GTOUUP, GTOULO, GTOVUP, GTOVLO, GTOWUP, GTOWLO		t_{GTOSK}	-	5	ns	Figure 60.38
GPT(PWM Delay Generation Circuit)	GTIOCxY_Z output skew (x = 0 to 3, Y = A or B, Z = A)		t_{HRSK}*2	-	2.0	ns	Figure 60.39
AGT	AGTIO, AGTEE input cycle		t_{ACYC}*3	100	-	ns	Figure 60.40
	AGTIO, AGTEE input high width, low width		t_{ACKWH}, t_{ACKWL}	40	-	ns	
	AGTIO, AGTO, AGTOA, AGTOB output cycle		t_{ACYC2}	62.5	-	ns	
ADC12	ADC12 trigger input pulse width		t_{TRGW}	1.5	-	t_{Pcyc}	Figure 60.41
KINT	KRn (n = 00 to 07) pulse width		t_{KR}	250	-	ns	Figure 60.42

Note: t_{Pcyc}: PCLKB cycle, t_{PDcyc}: PCLKD cycle.
Note 1. This skew applies when the same driver I/O is used. If the I/O of the middle and high drivers is mixed, operation is not guaranteed.
Note 2. The load is 30 pF.
Note 3. Constraints on input cycle:
When not switching the source clock: $t_{Pcyc} \times 2 < t_{ACYC}$ should be satisfied.
When switching the source clock: $t_{Pcyc} \times 6 < t_{ACYC}$ should be satisfied.

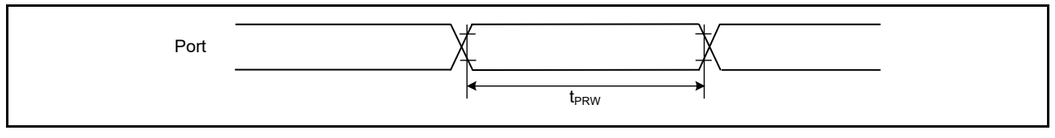


Figure 60.34 I/O ports input timing

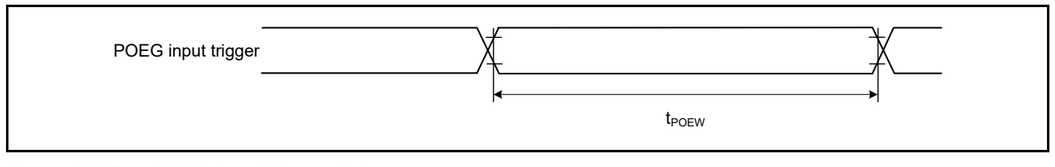


Figure 60.35 POEG input trigger timing

Table 60.19 IO端口、POEG、GPT32、AGT、KINT和ADC12触发时序(2of2)
GPT32 Conditions:
在PmnPFS寄存器的端口驱动能力位中选择高驱动输出。

AGT Conditions:
中间驱动输出在PmnPFS寄存器的端口驱动能力位中选择。

Parameter			Symbol	Min	Max	Unit	测试条件
GPT32	输入捕捉脉冲宽度	单边	t_{GTICW}	1.5	-	t_{PDcyc}	Figure 60.36
		双刃		2.5	-		
	GTIOCxY输出偏移（x=0到7，Y=A或B）	中间驱动缓冲器	t_{GTISK}*1	-	4	ns	Figure 60.37
		高驱动缓冲器		-	4		
	GTIOCxY输出偏差（x=8到13，Y=A或B）	中间驱动缓冲器		-	4		
		高驱动缓冲器		-	4		
	GTIOCxY输出偏差（x=0到13，Y=A或B）	中间驱动缓冲器		-	6		
		高驱动缓冲器		-	6		
	OPS输出偏差 GTOUUP, GTOULO, GTOVUP, GTOVLO, GTOWUP, GTOWLO		t_{GTOSK}	-	5	ns	Figure 60.38
GPT(PWM 延迟产生 Circuit)	GTIOCxY_Z输出偏移（x=0到3，Y=A或B，Z=A）		t_{HRSK}*2	-	2.0	ns	Figure 60.39
AGT	AGTIO、AGTEE输入周期		t_{ACYC}*3	100	-	ns	Figure 60.40
	AGTIO、AGTEE输入高宽、低宽		t_{ACKWH}, t_{ACKWL}	40	-	ns	
	AGTIO、AGTO、AGTOA、AGTOB输出周期		t_{ACYC2}	62.5	-	ns	
ADC12	ADC12触发输入脉冲宽度		t_{TRGW}	1.5	-	t_{Pcyc}	Figure 60.41
KINT	KRn(n=00to07)脉冲宽度		t_{KR}	250	-	ns	Figure 60.42

Note: t_{Pcyc}: PCLKB cycle, t_{PDcyc}: PCLKD cycle.
Note 1. 当使用相同的驱动程序IO时，此偏差适用。如果中高驱动器的IO混合使用，则无法保证运行。

Note 2. 负载为30pF。
Note 3. 输入周期的约束：
不切换源时钟时：tPcyc×2<tACYC应满足。
切换源时钟时：tPcyc×6<tACYC应满足。

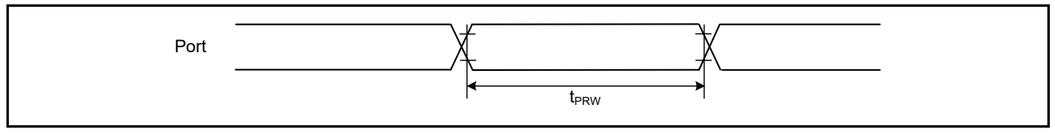


Figure 60.34 IO端口输入时序

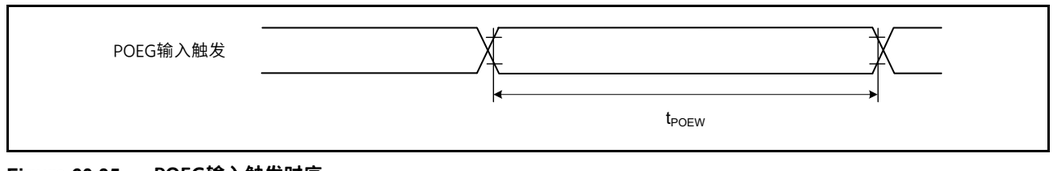


Figure 60.35 POEG输入触发时序

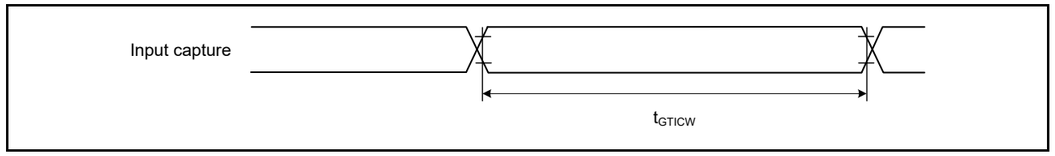


Figure 60.36 GPT32 input capture timing

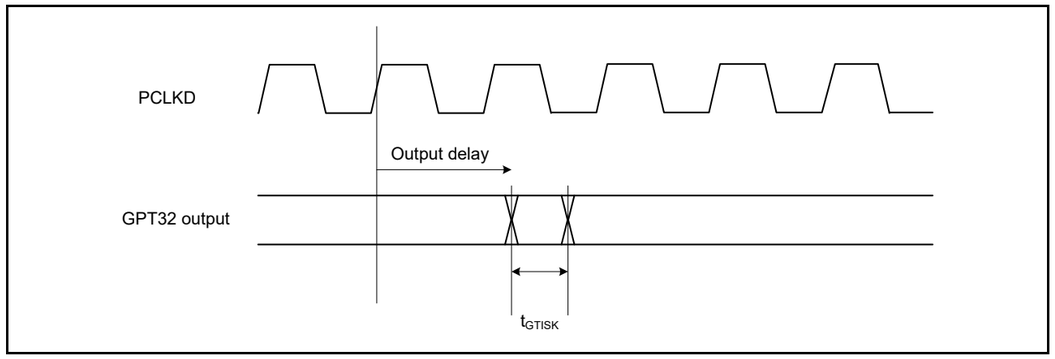


Figure 60.37 GPT32 output delay skew

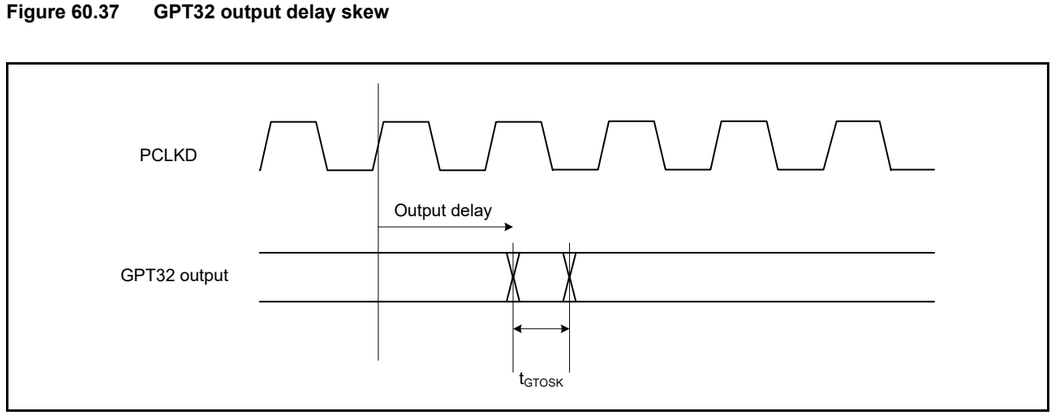


Figure 60.38 GPT32 output delay skew for OPS

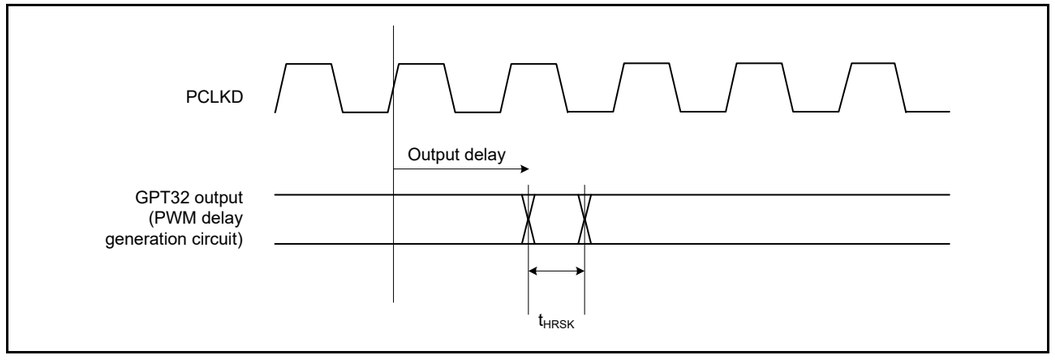


Figure 60.39 GPT32 (PWM Delay Generation Circuit) output delay skew

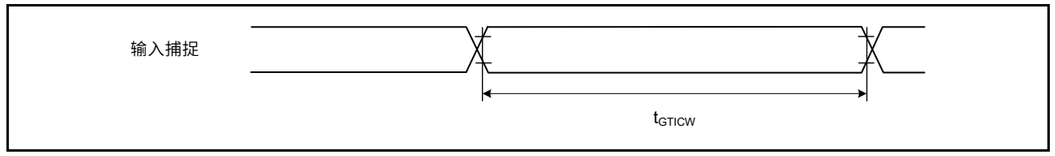


Figure 60.36 GPT32输入捕捉时序

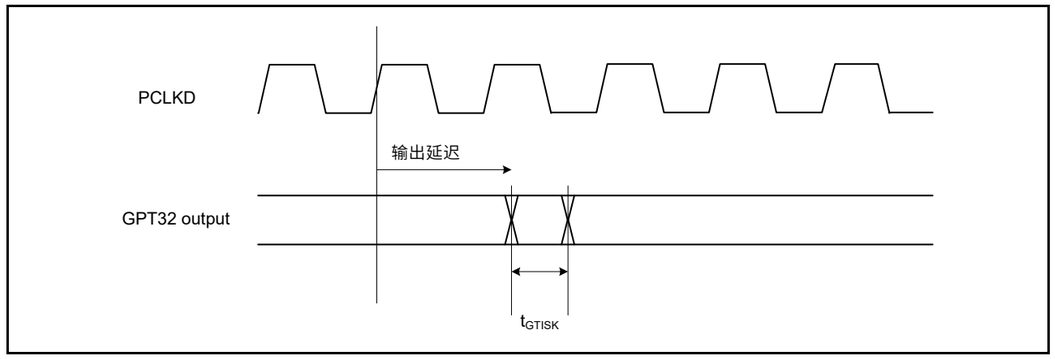


Figure 60.37 GPT32输出延迟偏移

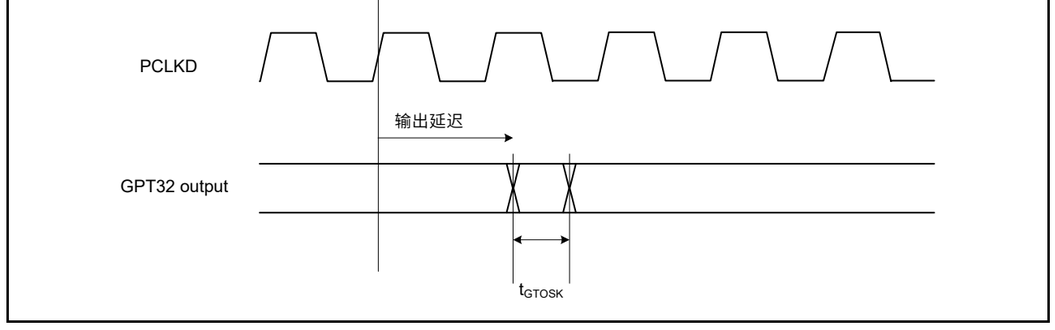


Figure 60.38 用于OPS的GPT32输出延迟偏移

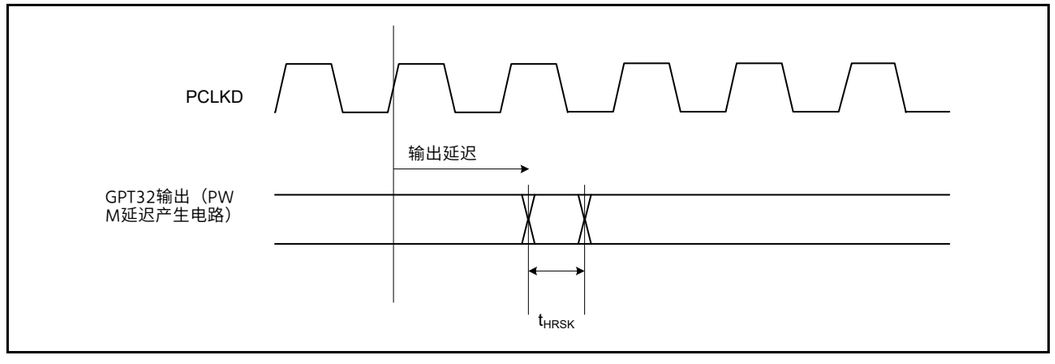


Figure 60.39 GPT32（PWM延迟生成电路）输出延迟偏移

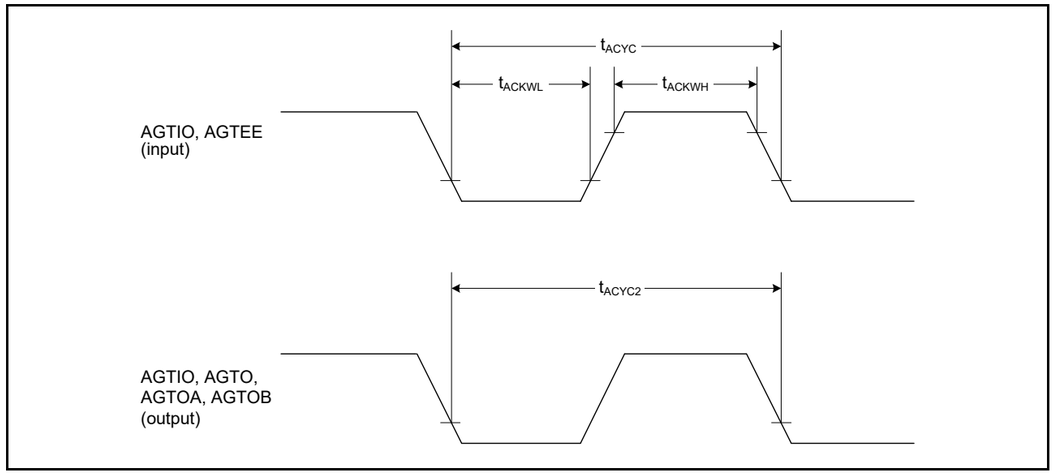


Figure 60.40 AGT input/output timing

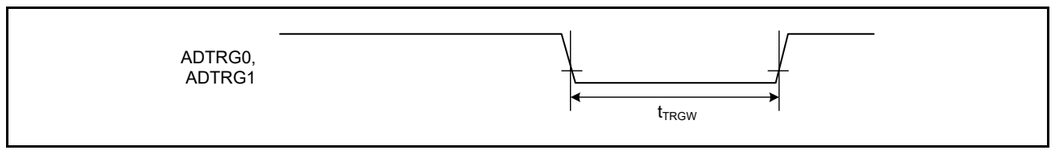


Figure 60.41 ADC12 trigger input timing

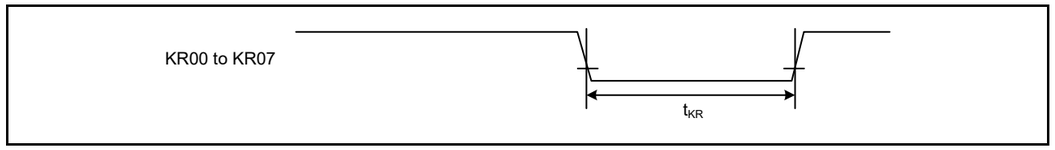


Figure 60.42 Key interrupt input timing

60.3.8 PWM Delay Generation Circuit Timing

Table 60.20 PWM Delay Generation Circuit timing

Parameter	Min	Typ	Max	Unit	Test conditions
Operation frequency	80	-	120	MHz	-
Resolution	-	260	-	ps	PCLKD = 120 MHz
DNL*1	-	±2.0	-	LSB	-

Note 1. This value normalizes the differences between lines in 1-LSB resolution.

60.3.9 CAC Timing

Table 60.21 CAC timing

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
CAC	CACREF input pulse width	$t_{PBcyc} \le tcac$*2	t_{CACREF}	$4.5 \times t_{cac} + 3 \times t_{PBcyc}$	-	-	ns	-
		$t_{PBcyc} > tcac$*2		$5 \times t_{cac} + 6.5 \times t_{PBcyc}$	-	-	ns	

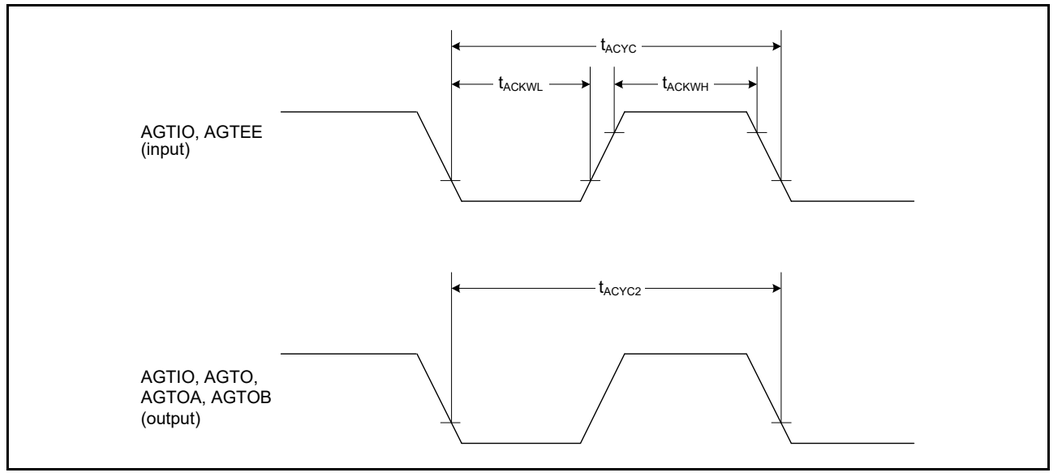


Figure 60.40 AGT input/output timing

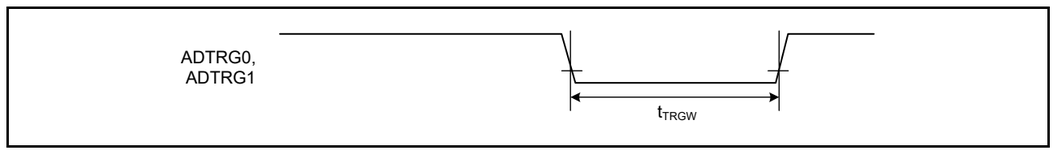


Figure 60.41 ADC12触发输入时序

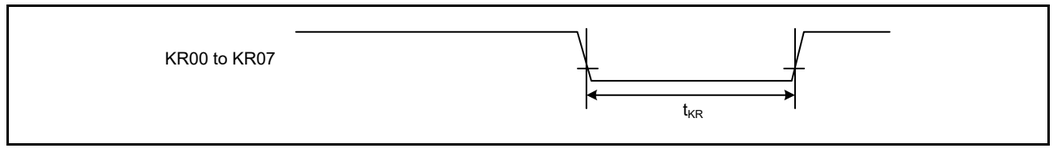


Figure 60.42 按键中断输入时序

60.3.8 PWM延迟产生电路时序

Table 60.20 PWM延迟产生电路时序

Parameter	Min	Typ	Max	Unit	测试条件
运行频率	80	-	120	MHz	-
Resolution	-	260	-	ps	PCLKD = 120 MHz
DNL*1	-	±2.0	-	LSB	-

Note 1. 此值标准化1-LSB分辨率中的行之间的差异。

60.3.9 CAC时序

Table 60.21 CAC计时

Parameter			Symbol	Min	Typ	Max	Unit	测试条件
CAC	CACREF输入脉冲宽度	$t_{PBcyc} \le tcac$*2	t_{CACREF}	$4.5 \times t_{cac} + 3 \times t_{PBcyc}$	-	-	ns	-
		$t_{PBcyc} > tcac$*2		$5 \times t_{cac} + 6.5 \times t_{PBcyc}$	-	-	ns	

Note 1. t_{PBcyc}: PCLKB cycle.
Note 2. t_{cac}: CAC count clock source cycle.

60.3.10 SCI Timing

Table 60.22 SCI timing (1)
Conditions: High drive output is selected in the port drive capability bit in the PmnPFS register for the following pins: SCK0 to SCK9.
For other pins, middle drive output is selected in the port drive capability bit in the PmnPFS register.

Parameter			Symbol	Min	Max	Unit*1	Test conditions
SCI	Input clock cycle	Asynchronous	t_{Scyc}	4	-	t_{Pcyc}	Figure 60.43
		Clock synchronous		6	-		
	Input clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Input clock rise time		t_{SCKr}	-	5	ns	
	Input clock fall time		t_{SCKf}	-	5	ns	
	Output clock cycle	Asynchronous	t_{Scyc}	6	-	t_{Pcyc}	
		Clock synchronous		4	-		
	Output clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
	Output clock rise time		t_{SCKr}	-	5	ns	
	Output clock fall time		t_{SCKf}	-	5	ns	
	Transmit data delay	Clock synchronous	t_{TXD}	-	25	ns	Figure 60.44
	Receive data setup time	Clock synchronous	t_{RXS}	15	-	ns	
	Receive data hold time	Clock synchronous	t_{RXH}	5	-	ns	

Note 1. t_{Pcyc}: PCLKA cycle.

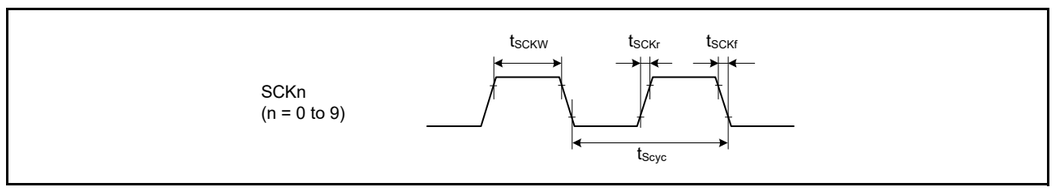


Figure 60.43 SCK clock input/output timing

Note 1. t_{PBcyc}: PCLKB cycle.
Note 2. tcac:CAC计数时钟源周期。

60.3.10 SCI时序

Table 60.22 SCI时序（1）
条件：在PmnPFS寄存器的端口驱动能力位中为以下引脚选择高驱动输出：SCK0至SCK9。
对于其他引脚，在PmnPFS寄存器的端口驱动能力位中选择中间驱动输出。

Parameter			Symbol	Min	Max	Unit*1	测试条件
SCI	输入时钟周期	Asynchronous	t_{Scyc}	4	-	t_{Pcyc}	Figure 60.43
		时钟同步		6	-		
	输入时钟脉冲宽度		t_{SCKW}	0.4	0.6	t_{Scyc}	
	输入时钟上升时间		t_{SCKr}	-	5	ns	
	输入时钟下降时间		t_{SCKf}	-	5	ns	
	输出时钟周期	Asynchronous	t_{Scyc}	6	-	t_{Pcyc}	
		时钟同步		4	-		
	输出时钟脉冲宽度		t_{SCKW}	0.4	0.6	t_{Scyc}	
	输出时钟上升时间		t_{SCKr}	-	5	ns	
	输出时钟下降时间		t_{SCKf}	-	5	ns	
	传输数据延迟	时钟同步	t_{TXD}	-	25	ns	Figure 60.44
	接收数据建立时间	时钟同步	t_{RXS}	15	-	ns	
	接收数据保持时间	时钟同步	t_{RXH}	5	-	ns	

Note 1. t_{Pcyc}: PCLKA cycle.

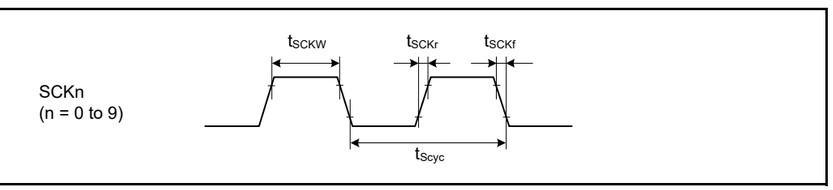


Figure 60.43 SCK时钟输入输出时序

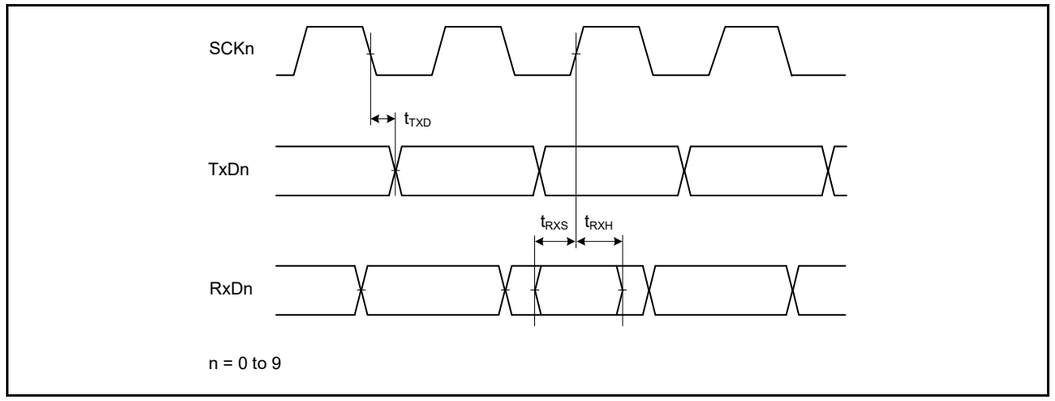


Figure 60.44 SCI input/output timing in clock synchronous mode

Table 60.23 SCI timing (2)
Conditions: High drive output is selected in the port drive capability bit in the PmnPFS register for the following pins: SCK0 to SCK9.
For other pins, middle drive output is selected in the port drive capability bit in the PmnPFS register.

Parameter		Symbol	Min	Max	Unit	Test conditions
Simple SPI	SCK clock cycle output (master)	t_{SPcyc}	4 (PCLKA ≤ 60 MHz) 8 (PCLKA > 60 MHz)	65536	t_{Pcyc}	Figure 60.45
	SCK clock cycle input (slave)	-	6 (PCLKA ≤ 60 MHz) 12 (PCLKA > 60 MHz)	65536		
	SCK clock high pulse width	t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK clock low pulse width	t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK clock rise and fall time	t_{SPCKr}, t_{SPCKf}	-	20	ns	
	Data input setup time	t_{SU}	33.3	-	ns	Figure 60.46 to Figure 60.49
	Data input hold time	t_{H}	33.3	-	ns	
	SS input setup time	t_{LEAD}	1	-	t_{SPcyc}	
	SS input hold time	t_{LAG}	1	-	t_{SPcyc}	
	Data output delay	t_{OD}	-	33.3	ns	
	Data output hold time	t_{OH}	-10	-	ns	
	Data rise and fall time	t_{Dr}, t_{Df}	-	16.6	ns	
	SS input rise and fall time	t_{SSLr}, t_{SSLf}	-	16.6	ns	
	Slave access time	t_{SA}	-	4 (PCLKA ≤ 60 MHz) 8 (PCLKA > 60 MHz)	t_{Pcyc}	Figure 60.49
	Slave output release time	t_{REL}	-	5 (PCLKA ≤ 60 MHz) 10 (PCLKA > 60 MHz)	t_{Pcyc}	

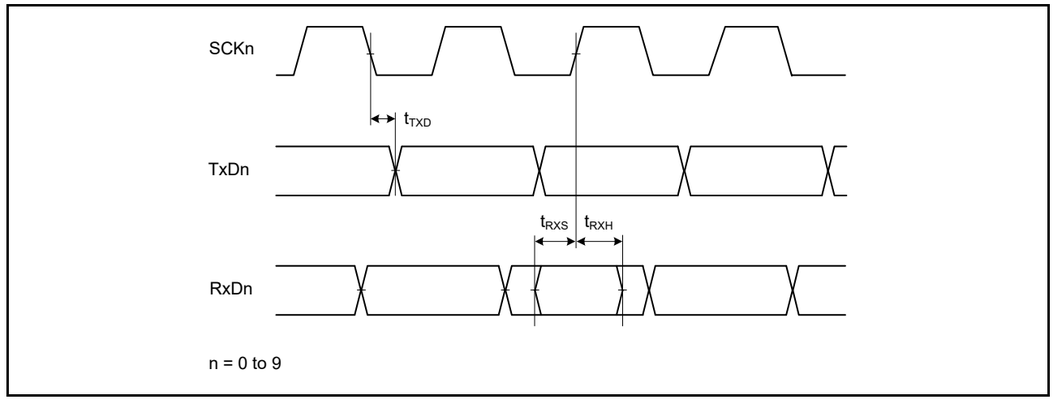


Figure 60.44 时钟同步模式下的SCI输入输出时序

Table 60.23 SCI时序（2）
条件：在PmnPFS寄存器的端口驱动能力位中为以下引脚选择高驱动输出：SCK0至SCK9。
对于其他引脚，在PmnPFS寄存器的端口驱动能力位中选择中间驱动输出。

Parameter		Symbol	Min	Max	Unit	测试条件
Simple SPI	SCK时钟周期输出（主机）	t_{SPcyc}	4 (PCLKA ≤ 60 MHz) 8 (PCLKA > 60 MHz)	65536	t_{Pcyc}	Figure 60.45
	SCK时钟周期输入（从机）	-	6 (PCLKA ≤ 60 MHz) 12 (PCLKA > 60 MHz)	65536		
	SCK时钟高脉冲宽度	t_{SPCKWH}	0.4	0.6	t_{SPcyc}	
	SCK时钟低脉冲宽度	t_{SPCKWL}	0.4	0.6	t_{SPcyc}	
	SCK时钟上升和下降时间	t_{SPCKr}, t_{SPCKf}	-	20	ns	
	数据输入建立时间	t_{SU}	33.3	-	ns	图60.46至Figure 60.49
	数据输入保持时间	t_{H}	33.3	-	ns	
	SS输入建立时间	t_{LEAD}	1	-	t_{SPcyc}	
	SS输入保持时间	t_{LAG}	1	-	t_{SPcyc}	
	数据输出延迟	t_{OD}	-	33.3	ns	
	数据输出保持时间	t_{OH}	-10	-	ns	
	数据上升和下降时间	t_{Dr}, t_{Df}	-	16.6	ns	
	SS输入上升和下降时间	t_{SSLr}, t_{SSLf}	-	16.6	ns	
	从站访问时间	t_{SA}	-	4 (PCLKA ≤ 60 MHz) 8 (PCLKA > 60 MHz)	t_{Pcyc}	Figure 60.49
	从机输出释放时间	t_{REL}	-	5 (PCLKA ≤ 60 MHz) 10 (PCLKA > 60 MHz)	t_{Pcyc}	

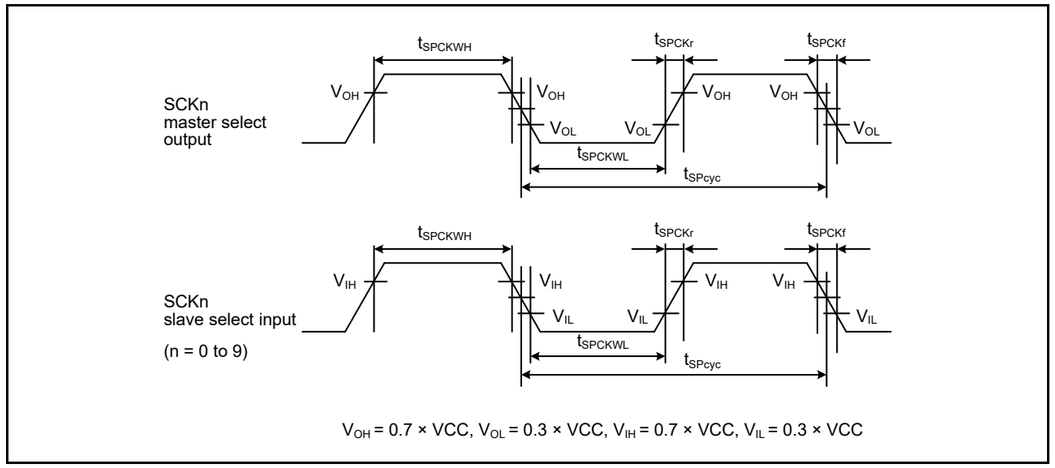


Figure 60.45 SCI simple SPI mode clock timing

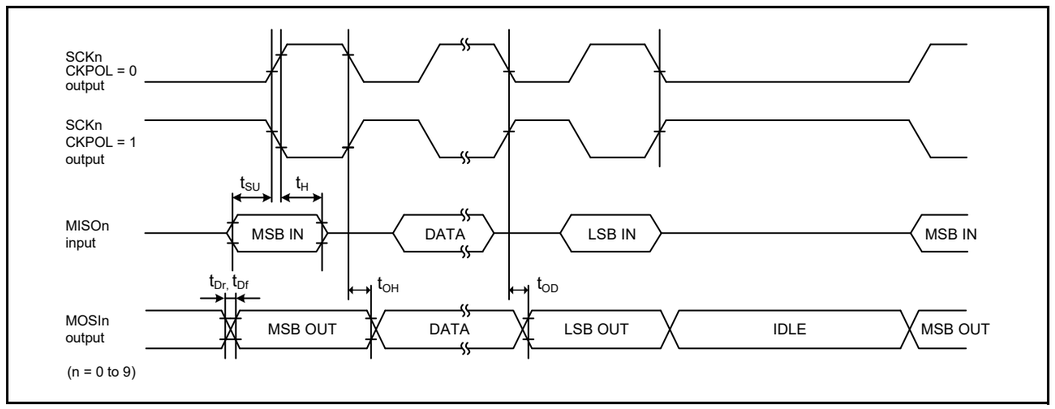


Figure 60.46 SCI simple SPI mode timing for master when CKPH = 1

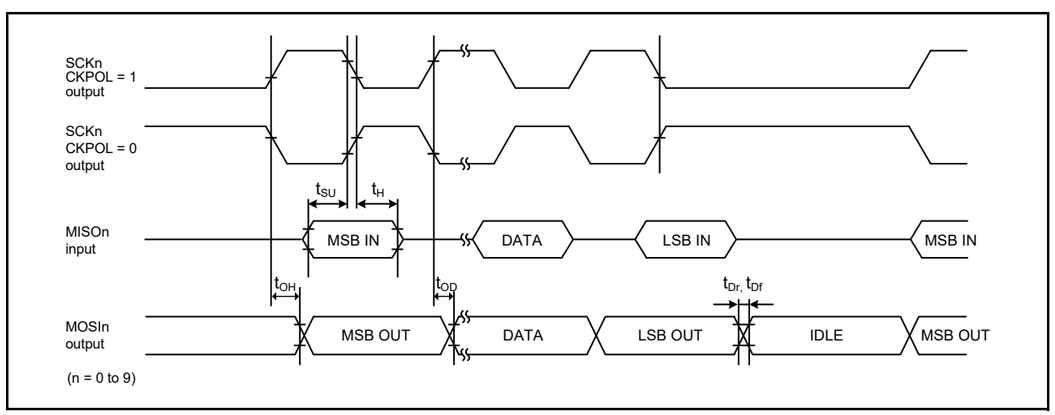


Figure 60.47 SCI simple SPI mode timing for master when CKPH = 0

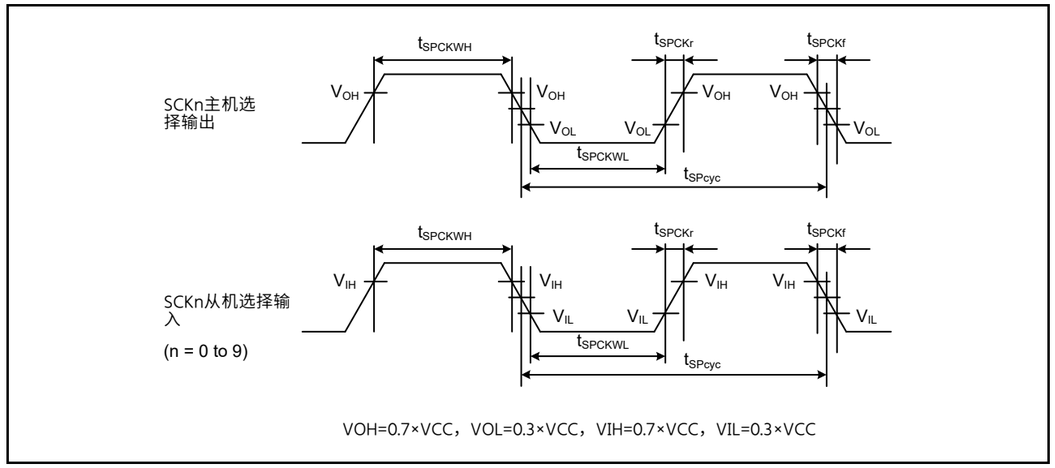


Figure 60.45 SCI简单SPI模式时钟时序

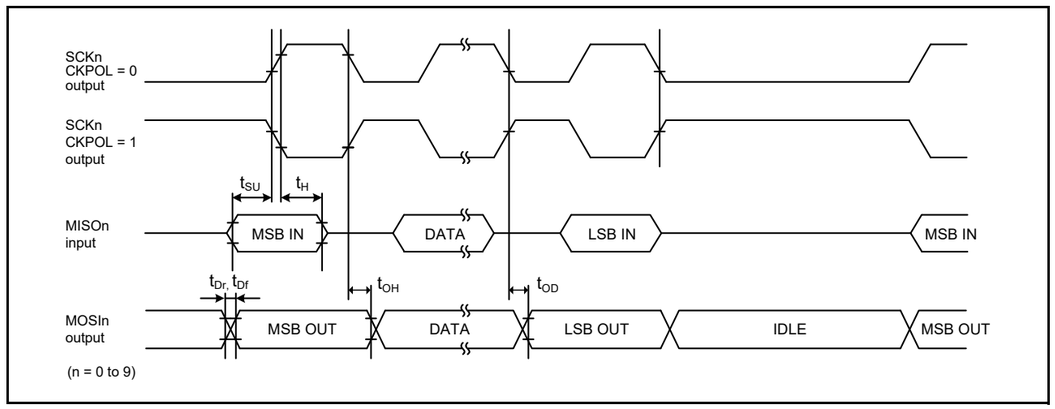


Figure 60.46 CKPH=1时主机的SCI简单SPI模式时序

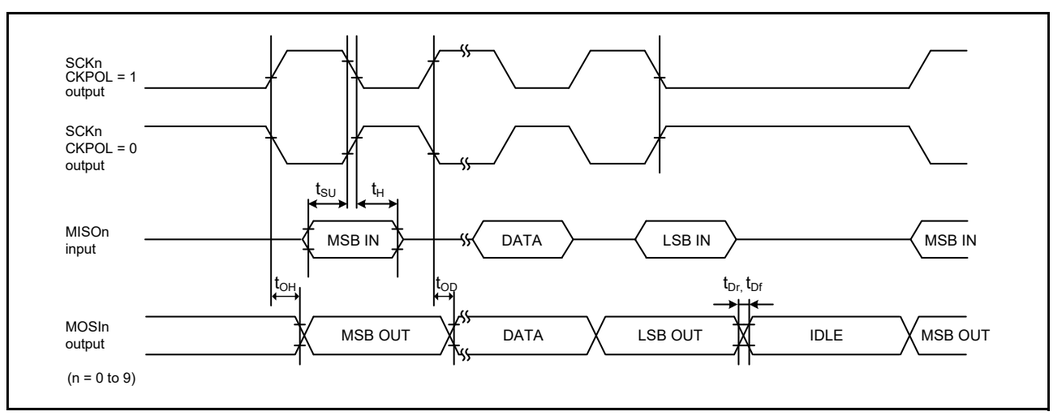


Figure 60.47 CKPH=0时主机的SCI简单SPI模式时序

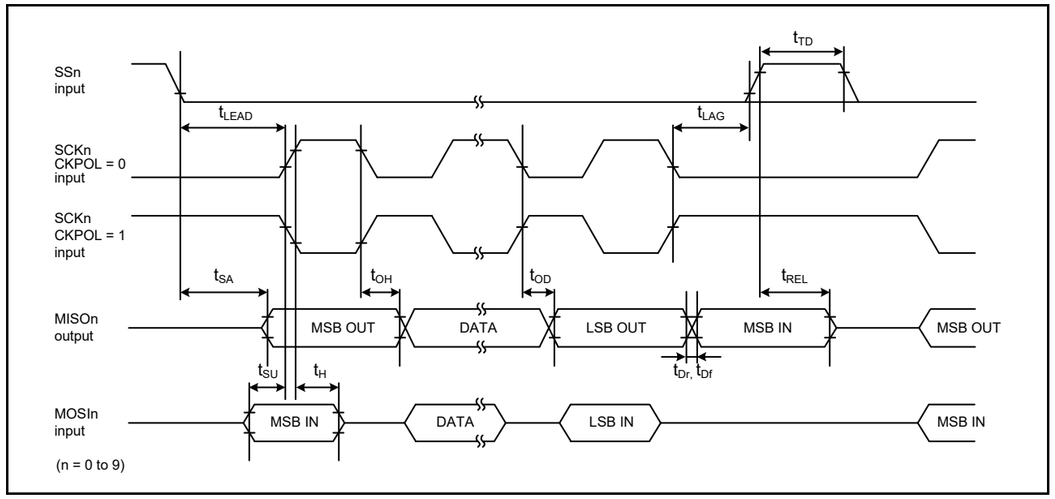


Figure 60.48 SCI simple SPI mode timing for slave when CKPH = 1

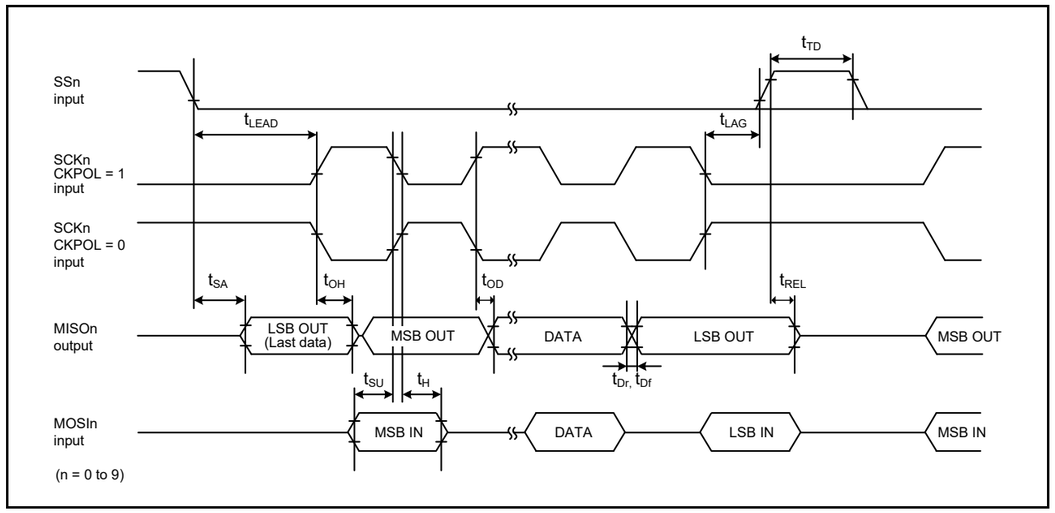


Figure 60.49 SCI simple SPI mode timing for slave when CKPH = 0

Table 60.24 SCI timing (3) (1 of 2)
Conditions: Middle drive output is selected in the port drive capability bit in the PmnPFS register.

Parameter		Symbol	Min	Max	Unit	Test conditions
Simple IIC (Standard mode)	SDA input rise time	t_{Sr}	-	1000	ns	Figure 60.50
	SDA input fall time	t_{Sf}	-	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	4 × t_{IICcyc}	ns	
	Data input setup time	t_{SDAS}	250	-	ns	
	Data input hold time	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b*1	-	400	pF	

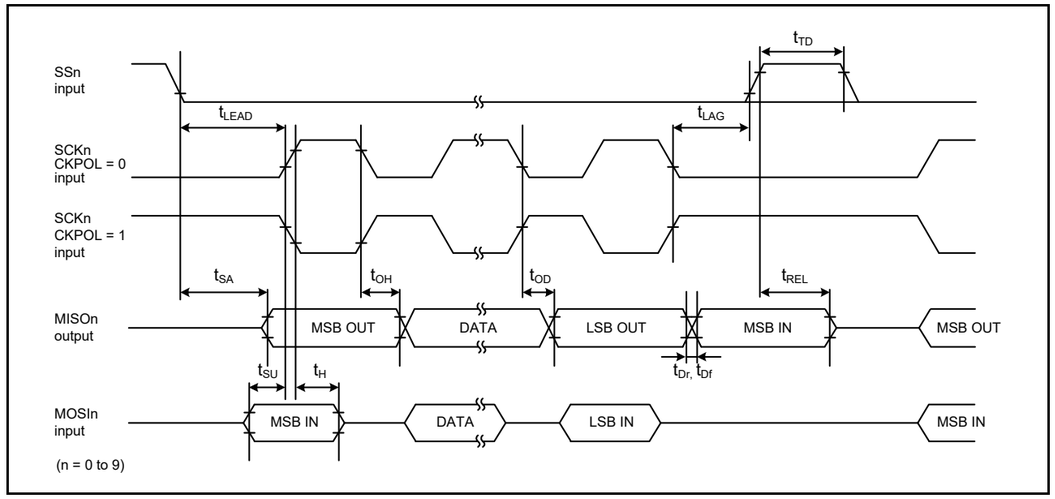


Figure 60.48 CKPH=1时从机的SCI简单SPI模式时序

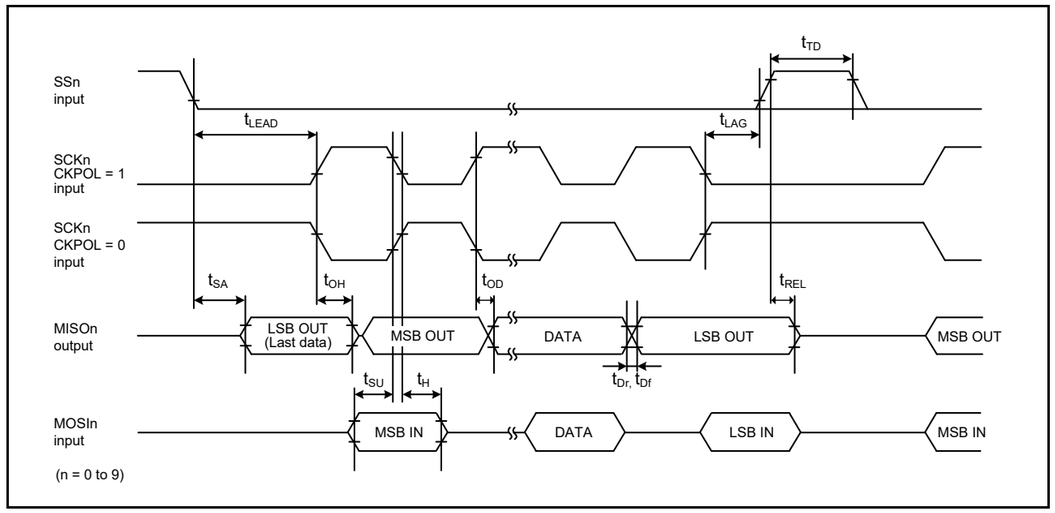


Figure 60.49 CKPH=0时从机的SCI简单SPI模式时序

Table 60.24 SCI计时(3)(1of2)
条件：在PmnPFS寄存器的端口驱动能力位中选择中间驱动输出。

Parameter		Symbol	Min	Max	Unit	测试条件
Simple IIC (Standard mode)	SDA输入上升时间	t_{Sr}	-	1000	ns	Figure 60.50
	SDA输入下降时间	t_{Sf}	-	300	ns	
	SDA输入尖峰脉冲去除时间	t_{SP}	0	4 × t_{IICcyc}	ns	
	数据输入建立时间	t_{SDAS}	250	-	ns	
	数据输入保持时间	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b*1	-	400	pF	

Table 60.24 SCI timing (3) (2 of 2)
Conditions: Middle drive output is selected in the port drive capability bit in the PmnPFS register.

Parameter		Symbol	Min	Max	Unit	Test conditions
Simple IIC (Fast mode)	SDA input rise time	t_{Sr}	-	300	ns	Figure 60.50
	SDA input fall time	t_{Sf}	-	300	ns	
	SDA input spike pulse removal time	t_{SP}	0	4 × t_{IICcyc}	ns	
	Data input setup time	t_{SDAS}	100	-	ns	
	Data input hold time	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b*1	-	400	pF	

Note: t_{IICcyc}: IIC internal reference clock (IICφ) cycle.
Note 1. Cb indicates the total capacity of the bus line.

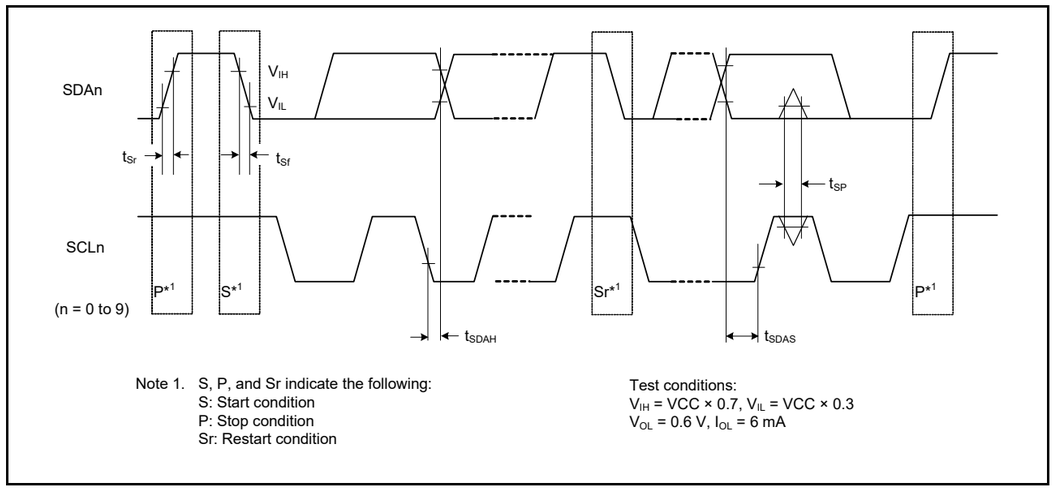


Figure 60.50 SCI simple IIC mode timing

Table 60.24 SCI计时(3)(2of2)
条件：在PmnPFS寄存器的端口驱动能力位中选择中间驱动输出。

Parameter		Symbol	Min	Max	Unit	测试条件
Simple IIC (Fast mode)	SDA输入上升时间	t_{Sr}	-	300	ns	Figure 60.50
	SDA输入下降时间	t_{Sf}	-	300	ns	
	SDA输入尖峰脉冲去除时间	t_{SP}	0	4 × t_{IICcyc}	ns	
	数据输入建立时间	t_{SDAS}	100	-	ns	
	数据输入保持时间	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b*1	-	400	pF	

Note: tIICcyc:IIC内部参考时钟(IICφ)周期。
Note 1. Cb表示公交线路的总容量。

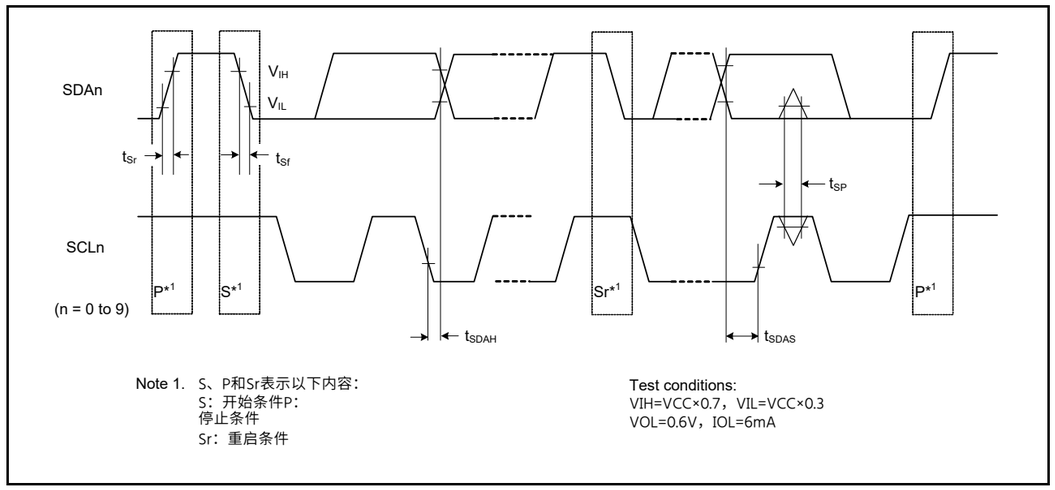


Figure 60.50 SCI简单IIC模式时序

60.3.11 SPI Timing

Table 60.25 SPI timing
Conditions:
For RSPCKA and RSPCKB pins, high drive output is selected with the port drive capability bit in the PmnPFS register.
For other pins, middle drive output is selected in the port drive capability bit in the PmnPFS register.

Parameter			Symbol	Min	Max	Unit*1	Test conditions*2
SPI	RSPCK clock cycle	Master	t_{SPcyc}	2 (PCLKA ≤ 60 MHz) 4 (PCLKA > 60 MHz)	4096	t_{Pcyc}	Figure 60.51 C = 30 pF
		Slave		4	4096		
	RSPCK clock high pulse width	Master	t_{SPCKWH}	(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3	-	ns	
		Slave		2 × t_{Pcyc}	-		
	RSPCK clock low pulse width	Master	t_{SPCKWL}	(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3	-	ns	
		Slave		2 × t_{Pcyc}	-		
	RSPCK clock rise and fall time	Master	t_{SPCKr}, t_{SPCKf}	-	5	ns	
		Slave		-	1	µs	
	Data input setup time	Master	t_{SU}	4	-	ns	Figure 60.52 to Figure 60.57 C = 30 pF
		Slave		5	-		
	Data input hold time	Master (PCLKA division ratio set to 1/2)	t_{HF}	0	-	ns	
		Master (PCLKA division ratio set to a value other than 1/2)	t_H	t_{Pcyc}	-		
		Slave	t_H	20	-		
	SSL setup time	Master	t_{LEAD}	N × t_{SPcyc} - 10*3	N × t_{SPcyc} + 100*3	ns	
		Slave		6 x t_{Pcyc}	-	ns	
	SSL hold time	Master	t_{LAG}	N × t_{SPcyc} - 10 *4	N × t_{SPcyc} + 100*4	ns	
		Slave		6 x t_{Pcyc}	-	ns	
	Data output delay	Master	t_{OD}	-	6.3	ns	
		Slave		-	20		
	Data output hold time	Master	t_{OH}	0	-	ns	
		Slave		0	-		
	Successive transmission delay	Master	t_{TD}	t_{SPcyc} + 2 × t_{Pcyc}	8 × t_{SPcyc} + 2 × t_{Pcyc}	ns	
		Slave		6 × t_{Pcyc}			
	MOSI and MISO rise and fall time	Output	t_{Dr}, t_{Df}	-	5	ns	
		Input		-	1	µs	
	SSL rise and fall time	Output	t_{SSLr}, t_{SSLf}	-	5	ns	
		Input		-	1	µs	
	Slave access time		t_{SA}	-	2 x t_{Pcyc} + 28	ns	Figure 60.56 and Figure 60.57 C = 30pF
	Slave output release time		t_{REL}	-	2 x t_{Pcyc} + 28		

Note 1. t_{Pcyc}: PCLKA cycle.

60.3.11 SPI时序

Table 60.25 SPI时序
Conditions:
对于RSPCKA和RSPCKB引脚，通过PmnPFS寄存器中的端口驱动能力位选择高驱动输出。
对于其他引脚，在PmnPFS寄存器的端口驱动能力位中选择中间驱动输出。

Parameter			Symbol	Min	Max	Unit*1	Test conditions*2
SPI	RSPCK时钟周期	Master	t_{SPcyc}	2 (PCLKA ≤ 60 MHz) 4 (PCLKA > 60 MHz)	4096	t_{Pcyc}	Figure 60.51 C = 30 pF
		Slave		4	4096		
	RSPCK时钟高脉冲宽度	Master	t_{SPCKWH}	(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3	-	ns	
		Slave		2 × t_{Pcyc}	-		
	RSPCK时钟低脉冲宽度	Master	t_{SPCKWL}	(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3	-	ns	
		Slave		2 × t_{Pcyc}	-		
	RSPCK时钟上升和下降时间	Master	t_{SPCKr}, t_{SPCKf}	-	5	ns	
		Slave		-	1	µs	
	数据输入建立时间	Master	t_{SU}	4	-	ns	图60.52至 Figure 60.57 C = 30 pF
		Slave		5	-		
	数据输入保持时间	主控（PCLKA分频比设置为12）	t_{HF}	0	-	ns	
		主控（PCLKA分频比设置为12以外的值）	t_H	t_{Pcyc}	-		
		Slave	t_H	20	-		
	SSL设置时间	Master	t_{LEAD}	N × t_{SPcyc} - 10*3	N × t_{SPcyc} + 100*3	ns	
		Slave		6 x t_{Pcyc}	-	ns	
	SSL保持时间	Master	t_{LAG}	N × t_{SPcyc} - 10 *4	N × t_{SPcyc} + 100*4	ns	
		Slave		6 x t_{Pcyc}	-	ns	
	数据输出延迟	Master	t_{OD}	-	6.3	ns	
		Slave		-	20		
	数据输出保持时间	Master	t_{OH}	0	-	ns	
		Slave		0	-		
	连续传输延迟	Master	t_{TD}	t_{SPcyc} + 2 × t_{Pcyc}	8 × t_{SPcyc} + 2 × t_{Pcyc}	ns	
		Slave		6 × t_{Pcyc}			
	MOSI和MISO上升和下降时间	Output	t_{Dr}, t_{Df}	-	5	ns	
		Input		-	1	µs	
	SSL上升和下降时间	Output	t_{SSLr}, t_{SSLf}	-	5	ns	
		Input		-	1	µs	
	从站访问时间		t_{SA}	-	2 x t_{Pcyc} + 28	ns	图60.56和 Figure 60.57 C = 30pF
	从机输出释放时间		t_{REL}	-	2 x t_{Pcyc} + 28		

Note 1. t_{Pcyc}: PCLKA cycle.

Note 2. Must use pins that have a letter (“_A”, “_B”) to indicate group membership appended to their name as groups. For the SPI interface, the AC portion of the electrical characteristics is measured for each group.
Note 3. N is set to an integer from 1 to 8 by the SPCKD register.
Note 4. N is set to an integer from 1 to 8 by the SSLND register.

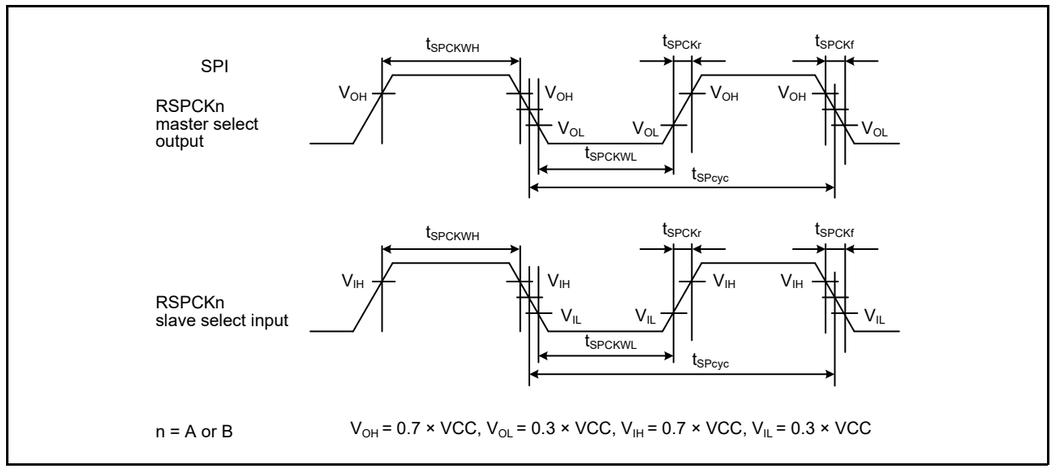


Figure 60.51 SPI clock timing

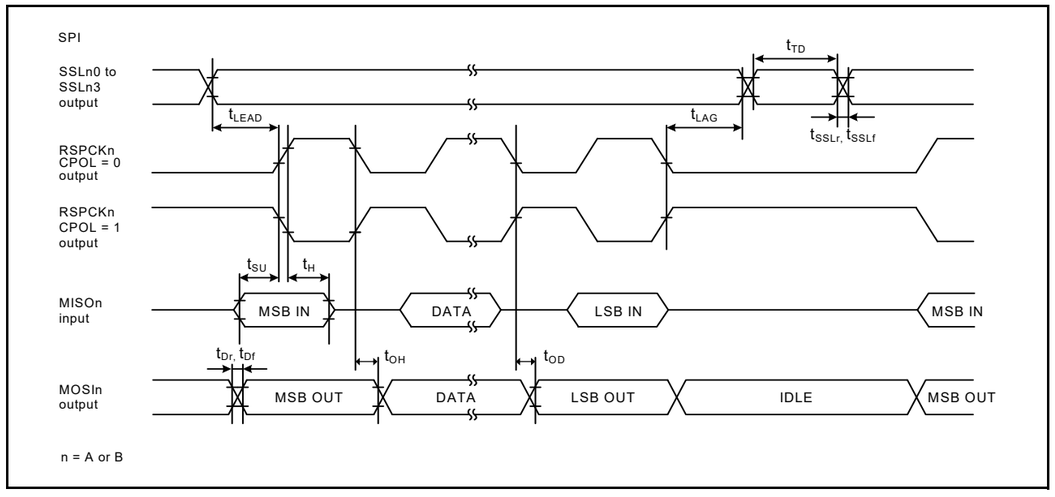


Figure 60.52 SPI timing for master when CPHA = 0

Note 2. 必须使用带有字母（“_A”、“_B”）的引脚来表示作为组附加到其名称的组成员身份。对于SPI接口，测量每组的电气特性的交流部分。
Note 3. N由SPCKD寄存器设置为从1到8的整数。
Note 4. N由SSLND寄存器设置为从1到8的整数。

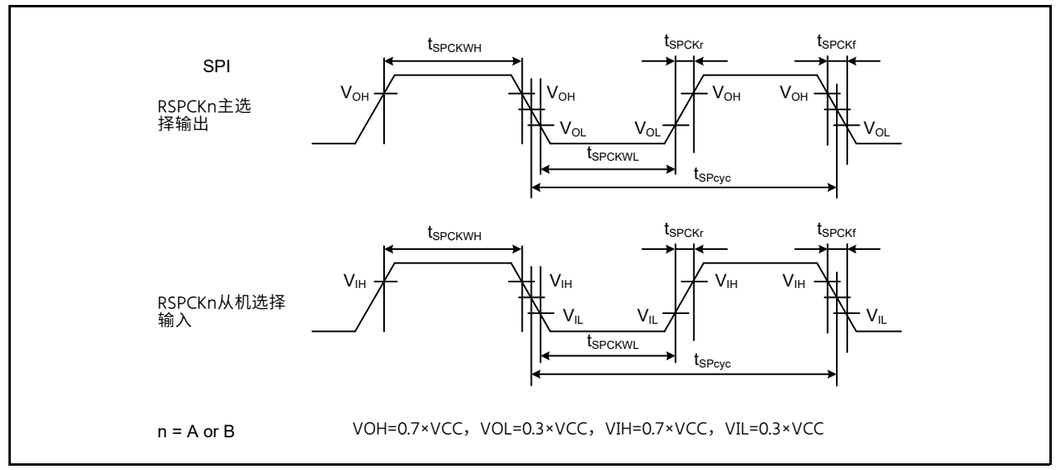


Figure 60.51 SPI时钟时序

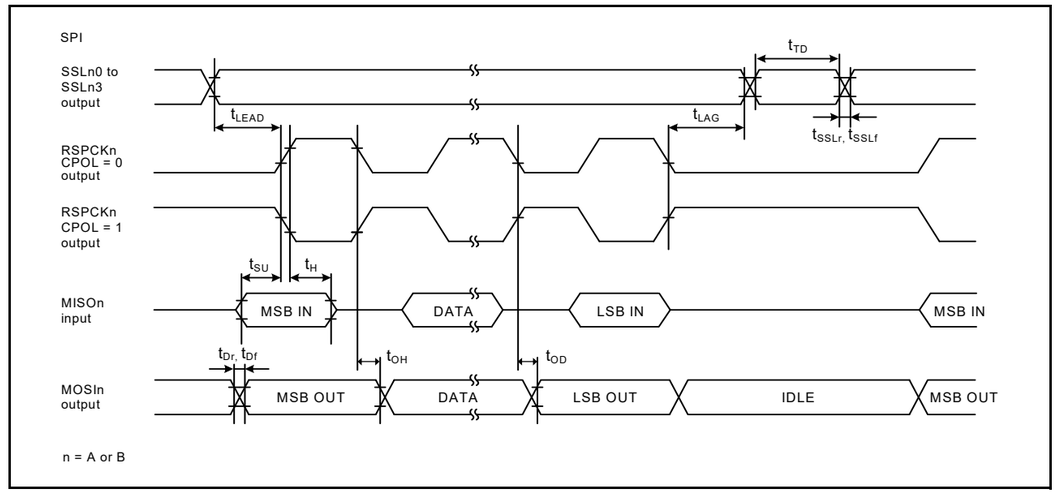


Figure 60.52 CPHA=0时主机的SPI时序

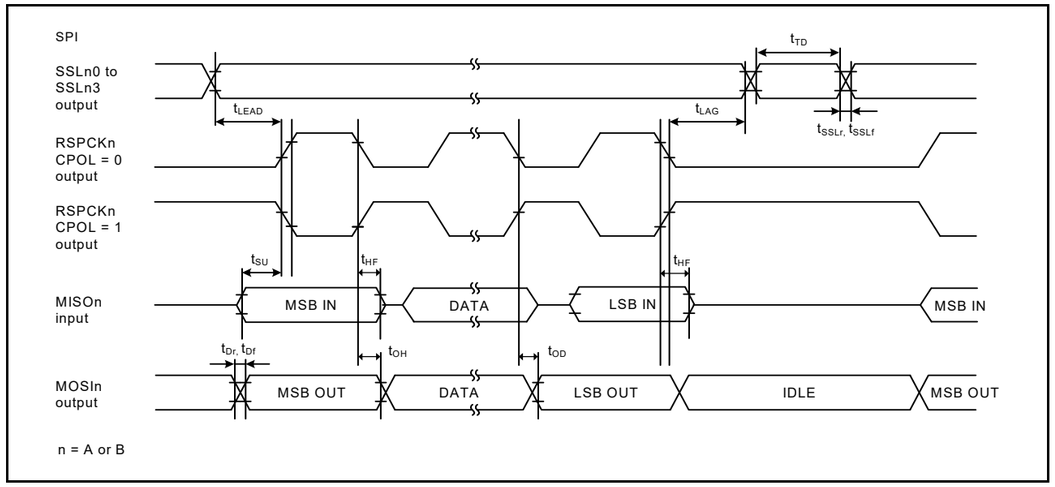


Figure 60.53 SPI timing for master when CPHA = 0 and the bit rate is set to PCLKA/2

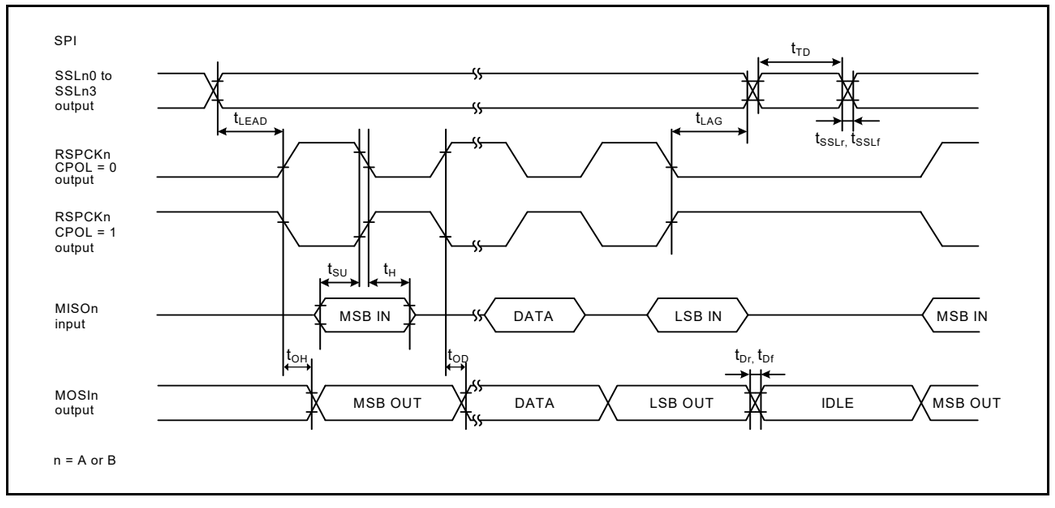


Figure 60.54 SPI timing for master when CPHA = 1

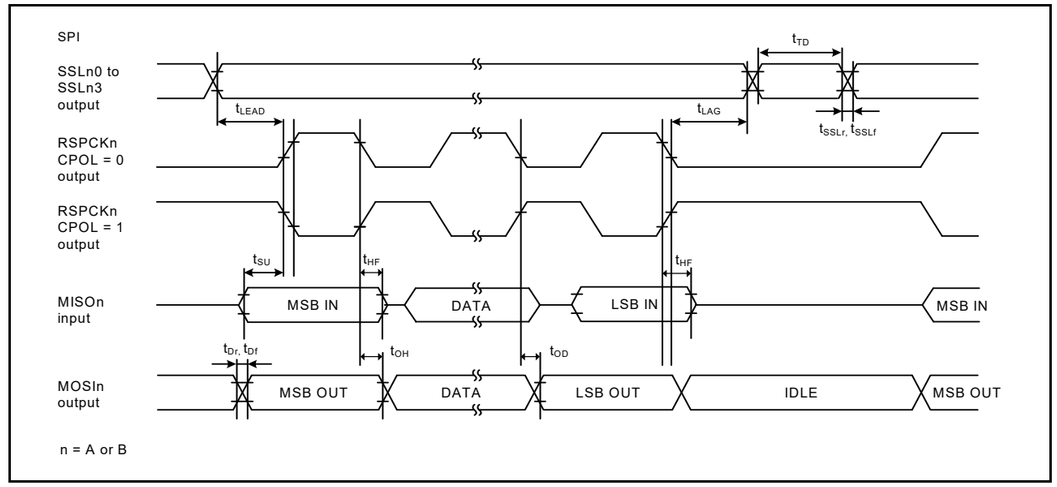


Figure 60.53 当CPHA=0且比特率设置为PCLKA2时主设备的SPI时序

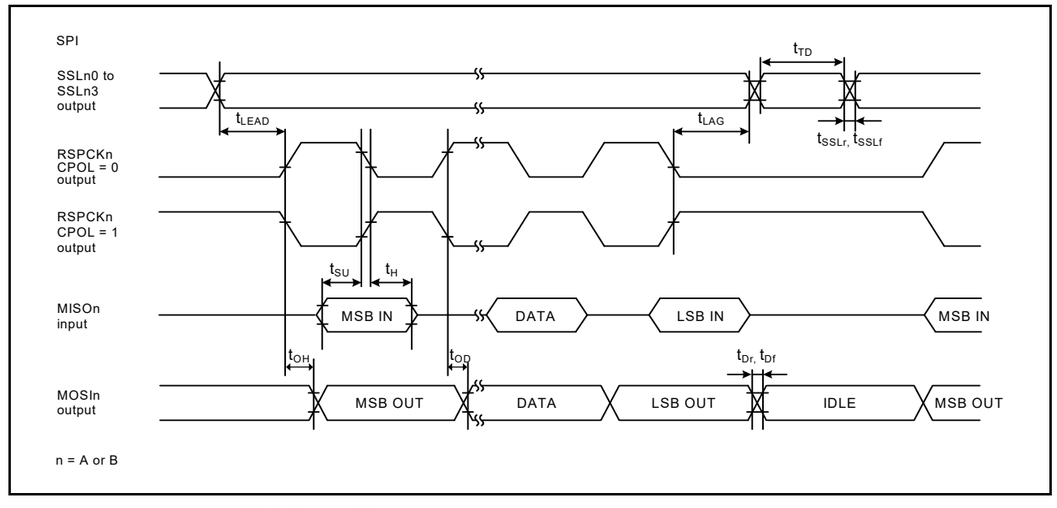


Figure 60.54 CPHA=1时主机的SPI时序

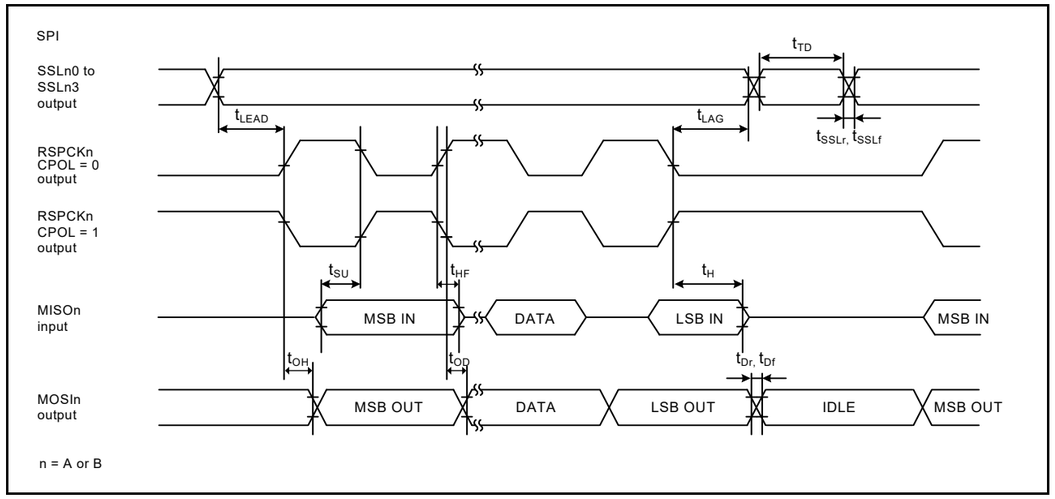


Figure 60.55 RSPI timing for master when CPHA = 1 and the bit rate is set to PCLKA/2

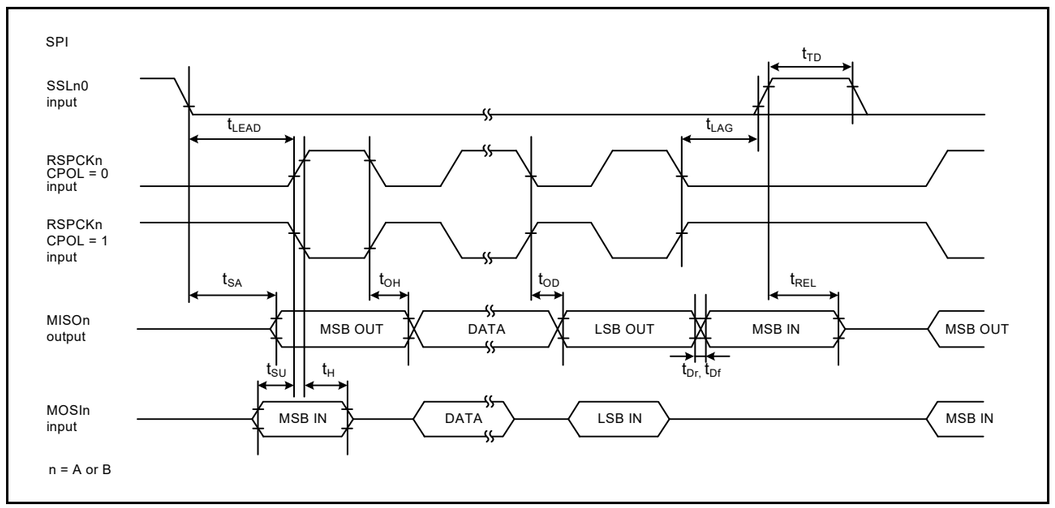


Figure 60.56 SPI timing for slave when CPHA = 0

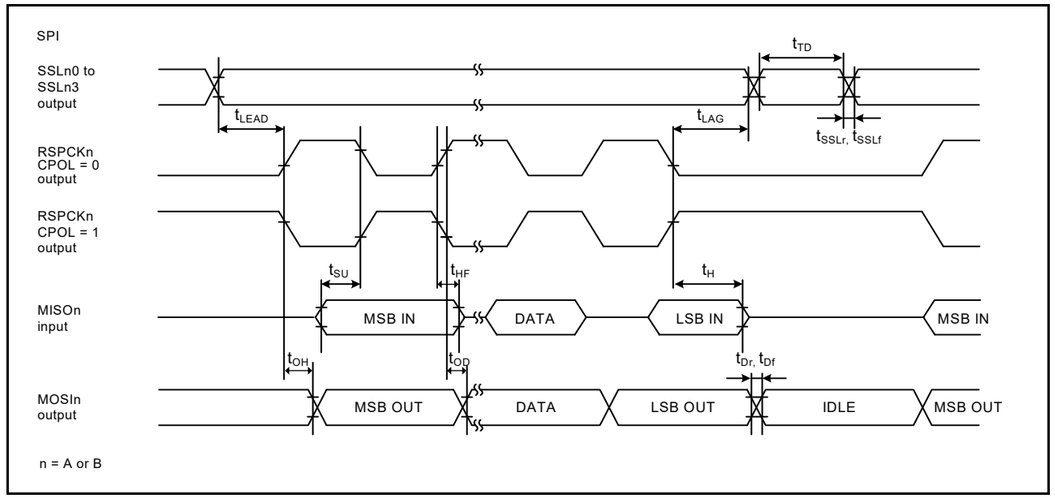


Figure 60.55 当CPHA=1且比特率设置为PCLKA2时，主机的RSPI时序

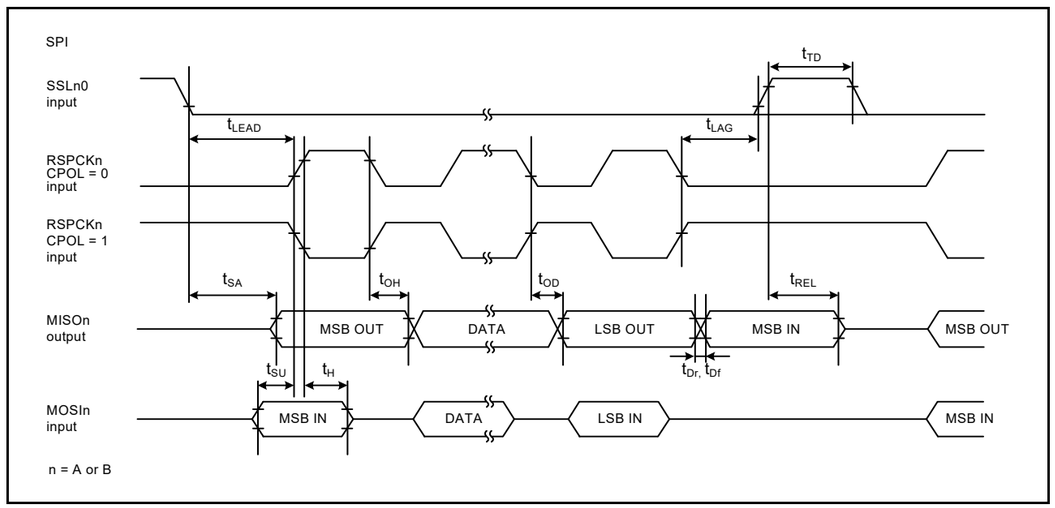


Figure 60.56 CPHA=0时从机的SPI时序

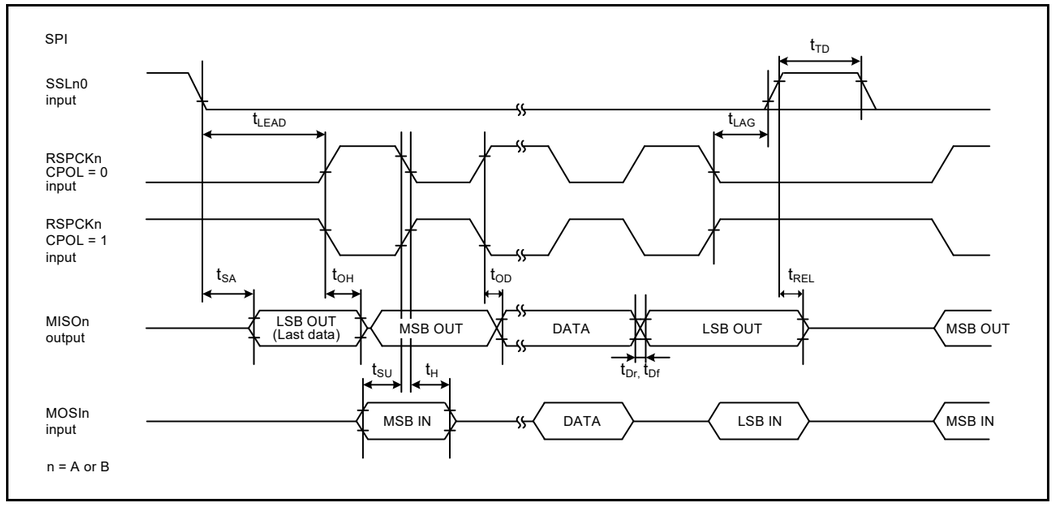


Figure 60.57 SPI timing for slave when CPHA = 1

60.3.12 QSPI Timing

Table 60.26 QSPI timing
Conditions: High drive output is selected in the port drive capability bit in the PmnPFS register.

Parameter		Symbol	Min	Max	Unit*1	Test conditions
QSPI	QSPCK clock cycle	t_{QScyc}	2	48	t_{Pcyc}	Figure 60.58
	QSPCK clock high pulse width	t_{QSWH}	t_{QScyc} × 0.4	-	ns	
	QSPCK clock low pulse width	t_{QSWL}	t_{QScyc} × 0.4	-	ns	
	Data input setup time	t_{Su}	8	-	ns	Figure 60.59
	Data input hold time	t_{IH}	0	-	ns	
	QSSL setup time	t_{LEAD}	(N+0.5) x t_{Qscyc} - 5 *2	(N+0.5) x t_{Qscyc} +100 *2	ns	
	QSSL hold time	t_{LAG}	(N+0.5) x t_{Qscyc} - 5 *3	(N+0.5) x t_{Qscyc} +100 *3	ns	
	Data output delay	t_{OD}	-	4	ns	
	Data output hold time	t_{OH}	-3.3	-	ns	
	Successive transmission delay	t_{TD}	1	16	t_{QScyc}	

Note 1. t_{Pcyc}: PCLKA cycle.
Note 2. N is set to 0 or 1 in SFMSLD.
Note 3. N is set to 0 or 1 in SFMSHD.

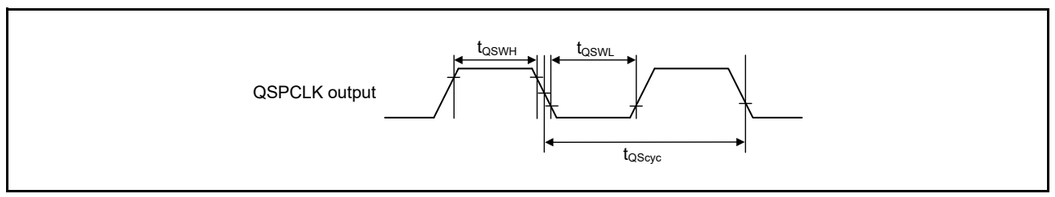


Figure 60.58 QSPI clock timing

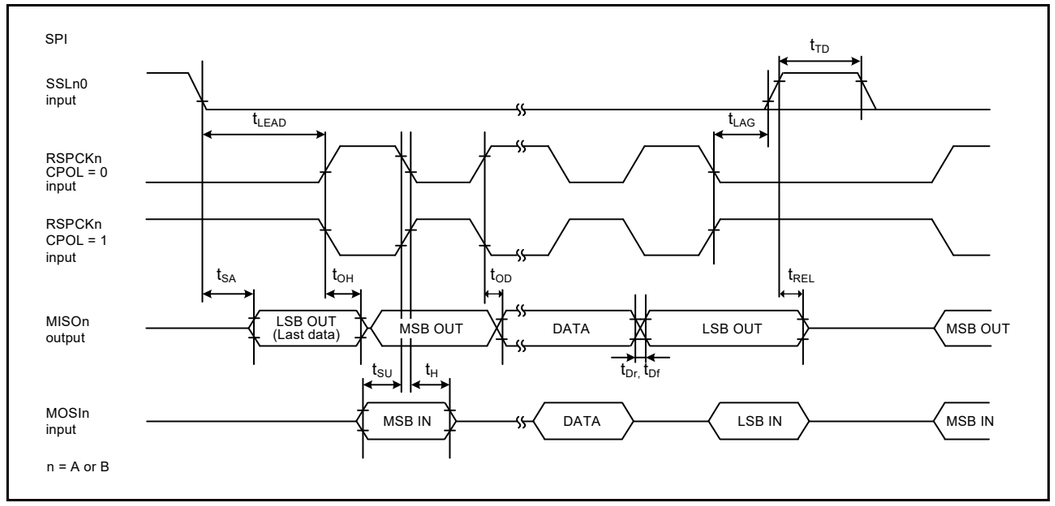


Figure 60.57 CPHA=1时从机的SPI时序

60.3.12 QSPI Timing

Table 60.26 QSPI timing
条件：在PmnPFS寄存器的端口驱动能力位中选择高驱动输出。

Parameter		Symbol	Min	Max	Unit*1	测试条件
QSPI	QSPCK时钟周期	t_{QScyc}	2	48	t_{Pcyc}	Figure 60.58
	QSPCK时钟高脉冲宽度	t_{QSWH}	t_{QScyc} × 0.4	-	ns	
	QSPCK时钟低脉冲宽度	t_{QSWL}	t_{QScyc} × 0.4	-	ns	
	数据输入建立时间	t_{Su}	8	-	ns	Figure 60.59
	数据输入保持时间	t_{IH}	0	-	ns	
	QSSL设置时间	t_{LEAD}	(N+0.5) x t_{Qscyc} - 5 *2	(N+0.5) x t_{Qscyc} +100 *2	ns	
	QSSL保持时间	t_{LAG}	(N+0.5) x t_{Qscyc} - 5 *3	(N+0.5) x t_{Qscyc} +100 *3	ns	
	数据输出延迟	t_{OD}	-	4	ns	
	数据输出保持时间	t_{OH}	-3.3	-	ns	
	连续传输延迟	t_{TD}	1	16	t_{QScyc}	

Note 1. t_{Pcyc}: PCLKA cycle.
Note 2. N在SFMSLD中设置为0或1。
Note 3. N在SFMSHD中设置为0或1。

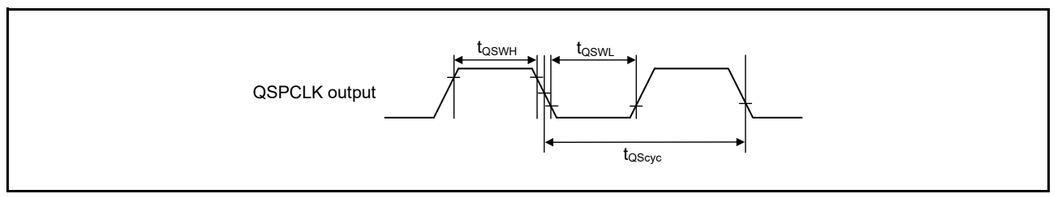


Figure 60.58 QSPI时钟时序

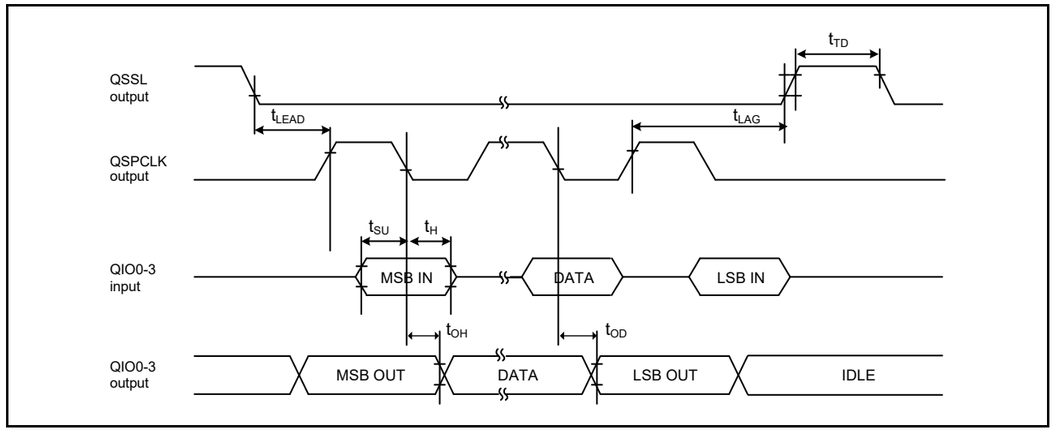


Figure 60.59 Transmit and receive timing

60.3.13 IIC Timing

Table 60.27 IIC timing (1) (1 of 2)
(1) Conditions: Middle drive output is selected in the port drive capability bit in the PmnPFS register for the following pins: SDA0_B, SCL0_B, SDA1_A, SCL1_A, SDA1_B, SCL1_B.
(2) The following pins do not require setting: SCL0_A, SDA0_A, SCL2, SDA2.
(3) Use pins that have a letter appended to their names, for instance "_A" or "_B", to indicate group membership. For the IIC interface, the AC portion of the electrical characteristics is measured for each group.

Parameter		Symbol	Min*1	Max	Unit	Test conditions*3
IIC (Standard mode, SMBus) ICFER.FMPE = 0	SCL input cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 1300	-	ns	Figure 60.60
	SCL input high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	-	ns	
	SCL input low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	-	ns	
	SCL, SDA input rise time	t_{Sr}	-	1000	ns	
	SCL, SDA input fall time	t_{Sf}	-	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA input bus free time when wakeup function is disabled	t_{BUF}	3 (6) × t_{IICcyc} + 300	-	ns	
	SDA input bus free time when wakeup function is enabled	t_{BUF}	3 (6) × t_{IICcyc} + 4 × t_{Pcyc} + 300	-	ns	
	START condition input hold time when wakeup function is disabled	t_{STAH}	t_{IICcyc} + 300	-	ns	
	START condition input hold time when wakeup function is enabled	t_{STAH}	1 (5) × t_{IICcyc} + t_{Pcyc} + 300	-	ns	
	Repeated START condition input setup time	t_{STAS}	1000	-	ns	
	STOP condition input setup time	t_{STOS}	1000	-	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	-	ns	
	Data input hold time	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b	-	400	pF	

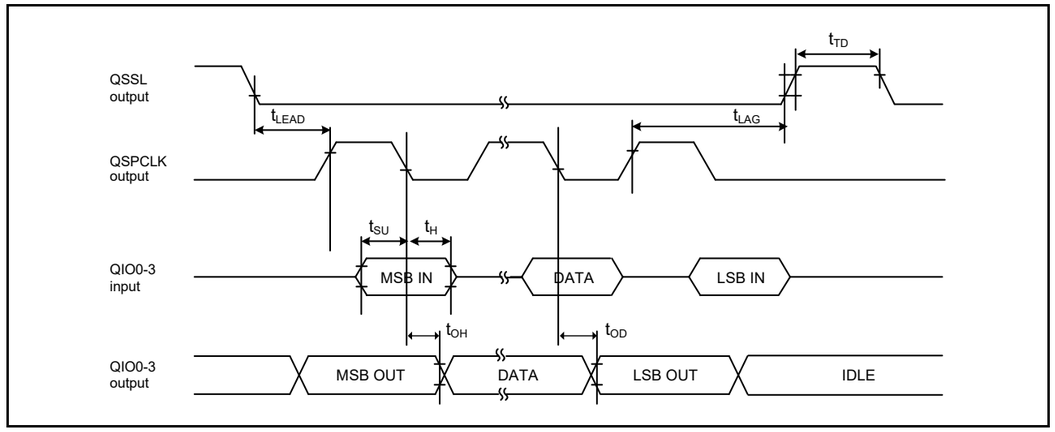


Figure 60.59 发送和接收时序

60.3.13 IIC Timing

表60.27IIC时序(1)(1of2)(1)条件：在PmnPFS寄存器的端口驱动能力位中为以下引脚选择中间驱动输出：SDA0_B、SCL0_B、SDA1_A、SCL1_A、SDA1_B、SCL1_B。(2)以下引脚不需要设置：SCL0_A、SDA0_A、SCL2、SDA2。(3)使用名称后附有字母的图钉，例如"_A"或"_B"，表示组成员身份。对于IIC接口，测量每组的电气特性的交流部分。

Parameter		Symbol	Min*1	Max	Unit	Test conditions*3
IIC (Standard mode, SMBus) ICFER.FMPE = 0	SCL输入周期时间	t_{SCL}	6 (12) × t_{IICcyc} + 1300	-	ns	Figure 60.60
	SCL输入高脉冲宽度	t_{SCLH}	3 (6) × t_{IICcyc} + 300	-	ns	
	SCL输入低脉冲宽度	t_{SCLL}	3 (6) × t_{IICcyc} + 300	-	ns	
	SCL、SDA输入上升时间	t_{Sr}	-	1000	ns	
	SCL、SDA输入下降时间	t_{Sf}	-	300	ns	
	SCL、SDA输入尖峰脉冲去除时间	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	禁用唤醒功能时的SDA输入总线空闲时间	t_{BUF}	3 (6) × t_{IICcyc} + 300	-	ns	
	唤醒功能启用时SDA输入总线空闲时间	t_{BUF}	3 (6) × t_{IICcyc} + 4 × t_{Pcyc} + 300	-	ns	
	禁用唤醒功能时的START条件输入保持时间	t_{STAH}	t_{IICcyc} + 300	-	ns	
	启用唤醒功能时的START条件输入保持时间	t_{STAH}	1 (5) × t_{IICcyc} + t_{Pcyc} + 300	-	ns	
	重复启动条件输入建立时间	t_{STAS}	1000	-	ns	
	STOP条件输入建立时间	t_{STOS}	1000	-	ns	
	数据输入建立时间	t_{SDAS}	t_{IICcyc} + 50	-	ns	
	数据输入保持时间	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b	-	400	pF	

Table 60.27 IIC timing (1) (2 of 2)

(1) Conditions: Middle drive output is selected in the port drive capability bit in the PmnPFS register for the following pins: SDA0_B, SCL0_B, SDA1_A, SCL1_A, SDA1_B, SCL1_B.
(2) The following pins do not require setting: SCL0_A, SDA0_A, SCL2, SDA2.
(3) Use pins that have a letter appended to their names, for instance "_A" or "_B", to indicate group membership. For the IIC interface, the AC portion of the electrical characteristics is measured for each group.

Parameter		Symbol	Min*1	Max	Unit	Test conditions*3
IIC (Fast mode)	SCL input cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 600	-	ns	Figure 60.60
	SCL input high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 300	-	ns	
	SCL input low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 300	-	ns	
	SCL, SDA input rise time	t_{Sr}	20 × (external pullup voltage/5.5V)*2	300	ns	
	SCL, SDA input fall time	t_{Sf}	20 × (external pullup voltage/5.5V)*2	300	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA input bus free time when wakeup function is disabled	t_{BUF}	3 (6) × t_{IICcyc} + 300	-	ns	
	SDA input bus free time when wakeup function is enabled	t_{BUF}	3 (6) × t_{IICcyc} + 4 × t_{Pcyc} + 300	-	ns	
	START condition input hold time when wakeup function is disabled	t_{STAH}	t_{IICcyc} + 300	-	ns	
	START condition input hold time when wakeup function is enabled	t_{STAH}	1 (5) × t_{IICcyc} + t_{Pcyc} + 300	-	ns	
	Repeated START condition input setup time	t_{STAS}	300	-	ns	
	STOP condition input setup time	t_{STOS}	300	-	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 50	-	ns	
	Data input hold time	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b	-	400	pF	

Note: t_{IICcyc}: IIC internal reference clock (IICφ) cycle, t_{Pcyc}: PCLKB cycle.
Note 1. Values in parentheses apply when ICMR3.NF[1:0] is set to 11b while the digital filter is enabled with ICFER.NFE set to 1.
Note 2. Only supported for SCL0_A, SDA0_A, SCL2, and SDA2.
Note 3. Must use pins that have a letter ("_A", "_B") to indicate group membership appended to their name as groups. For the IIC interface, the AC portion of the electrical characteristics is measured for each group.

表60.27IIC时序(1)(2of2)(1)条件：在PmnPFS寄存器的端口驱动能力位中为以下引脚选择中间驱动输出：SDA0_B、SCL0_B、SDA1_A、SCL1_A、SDA1_B、SCL1_B。(2)以下引脚不需要设置：SCL0_A、SDA0_A、SCL2、SDA2。(3)使用名称后附有字母的图钉，例如"_A"或"_B"，表示组成员身份。对于IIC接口，测量每组的电气特性的交流部分。

Parameter		Symbol	Min*1	Max	Unit	Test conditions*3
IIC (Fast mode)	SCL输入周期时间	t_{SCL}	6 (12) × t_{IICcyc} + 600	-	ns	Figure 60.60
	SCL输入高脉冲宽度	t_{SCLH}	3 (6) × t_{IICcyc} + 300	-	ns	
	SCL输入低脉冲宽度	t_{SCLL}	3 (6) × t_{IICcyc} + 300	-	ns	
	SCL、SDA输入上升时间	t_{Sr}	20 × (external pullup voltage/5.5V)*2	300	ns	
	SCL、SDA输入下降时间	t_{Sf}	20 × (external pullup voltage/5.5V)*2	300	ns	
	SCL、SDA输入尖峰脉冲去除时间	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	禁用唤醒功能时的SDA输入总线空闲时间	t_{BUF}	3 (6) × t_{IICcyc} + 300	-	ns	
	唤醒功能启用时SDA输入总线空闲时间	t_{BUF}	3 (6) × t_{IICcyc} + 4 × t_{Pcyc} + 300	-	ns	
	禁用唤醒功能时的START条件输入保持时间	t_{STAH}	t_{IICcyc} + 300	-	ns	
	启用唤醒功能时的START条件输入保持时间	t_{STAH}	1 (5) × t_{IICcyc} + t_{Pcyc} + 300	-	ns	
	重复启动条件输入建立时间	t_{STAS}	300	-	ns	
	STOP条件输入建立时间	t_{STOS}	300	-	ns	
	数据输入建立时间	t_{SDAS}	t_{IICcyc} + 50	-	ns	
	数据输入保持时间	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b	-	400	pF	

Note: tIICcyc：IIC内部参考时钟(IICφ)周期，tPcyc：PCLKB周期。
Note 1. 当ICMR3.NF[1:0]设置为11b且数字滤波器启用且ICFER.NFE设置为1时，括号中的值适用。
Note 2. 仅支持SCL0_A、SDA0_A、SCL2和SDA2。
Note 3. 必须使用带有字母（"_A"、"_B"）的引脚来表示作为组附加到其名称的组成员身份。对于IIC接口，测量每组的电气特性的交流部分。

Table 60.28 IIC timing (2)
Setting of the SCL0_A, SDA0_A pins is not required with the port drive capability bit in the PmnPFS register.

Parameter		Symbol	Min*1,*2	Max	Unit	Test conditions
IIC (Fast-mode+) ICFER.FMPE = 1	SCL input cycle time	t_{SCL}	6 (12) × t_{IICcyc} + 240	-	ns	Figure 60.60
	SCL input high pulse width	t_{SCLH}	3 (6) × t_{IICcyc} + 120	-	ns	
	SCL input low pulse width	t_{SCLL}	3 (6) × t_{IICcyc} + 120	-	ns	
	SCL, SDA input rise time	t_{Sr}	-	120	ns	
	SCL, SDA input fall time	t_{Sf}	-	120	ns	
	SCL, SDA input spike pulse removal time	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	SDA input bus free time when wakeup function is disabled	t_{BUF}	3 (6) × t_{IICcyc} + 120	-	ns	
	SDA input bus free time when wakeup function is enabled	t_{BUF}	3 (6) × t_{IICcyc} + 4 × t_{Pcyc} + 120	-	ns	
	Start condition input hold time when wakeup function is disabled	t_{STAH}	t_{IICcyc} + 120	-	ns	
	START condition input hold time when wakeup function is enabled	t_{STAH}	1 (5) × t_{IICcyc} + t_{Pcyc} + 120	-	ns	
	Restart condition input setup time	t_{STAS}	120	-	ns	
	Stop condition input setup time	t_{STOS}	120	-	ns	
	Data input setup time	t_{SDAS}	t_{IICcyc} + 30	-	ns	
	Data input hold time	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b	-	550	pF	

Note: t_{IICcyc}: IIC internal reference clock (IICφ) cycle, t_{Pcyc}: PCLKB cycle.
Note 1. Values in parentheses apply when ICMR3.NF[1:0] is set to 11b while the digital filter is enabled with ICFER.NFE set to 1.
Note 2. Cb indicates the total capacity of the bus line.

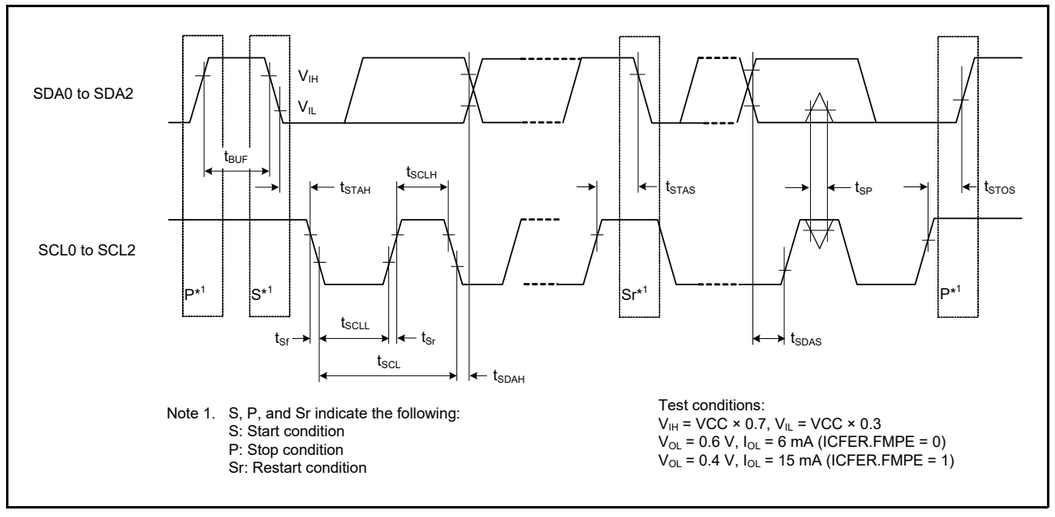


Figure 60.60 I²C bus interface input/output timing

Table 60.28 IIC timing (2)
PmnPFS寄存器中的端口驱动能力位不需要设置SCL0_A、SDA0_A引脚。

Parameter		Symbol	Min*1,*2	Max	Unit	测试条件
IIC (Fast-mode+) ICFER.FMPE = 1	SCL输入周期时间	t_{SCL}	6 (12) × t_{IICcyc} + 240	-	ns	Figure 60.60
	SCL输入高脉冲宽度	t_{SCLH}	3 (6) × t_{IICcyc} + 120	-	ns	
	SCL输入低脉冲宽度	t_{SCLL}	3 (6) × t_{IICcyc} + 120	-	ns	
	SCL、SDA输入上升时间	t_{Sr}	-	120	ns	
	SCL、SDA输入下降时间	t_{Sf}	-	120	ns	
	SCL、SDA输入尖峰脉冲去除时间	t_{SP}	0	1 (4) × t_{IICcyc}	ns	
	禁用唤醒功能时的SDA输入总线空闲时间	t_{BUF}	3 (6) × t_{IICcyc} + 120	-	ns	
	唤醒功能启用时SDA输入总线空闲时间	t_{BUF}	3 (6) × t_{IICcyc} + 4 × t_{Pcyc} + 120	-	ns	
	禁用唤醒功能时的启动条件输入保持时间	t_{STAH}	t_{IICcyc} + 120	-	ns	
	启用唤醒功能时的START条件输入保持时间	t_{STAH}	1 (5) × t_{IICcyc} + t_{Pcyc} + 120	-	ns	
	重启条件输入建立时间	t_{STAS}	120	-	ns	
	停止条件输入建立时间	t_{STOS}	120	-	ns	
	数据输入建立时间	t_{SDAS}	t_{IICcyc} + 30	-	ns	
	数据输入保持时间	t_{SDAH}	0	-	ns	
	SCL, SDA capacitive load	C_b	-	550	pF	

Note: tIICcyc：IIC内部参考时钟(IICφ)周期，tPcyc：PCLKB周期。
Note 1. 当ICMR3.NF[1:0]设置为11b且数字滤波器启用且ICFER.NFE设置为1时，括号中的值适用。
Note 2. Cb表示公交线路的总容量。

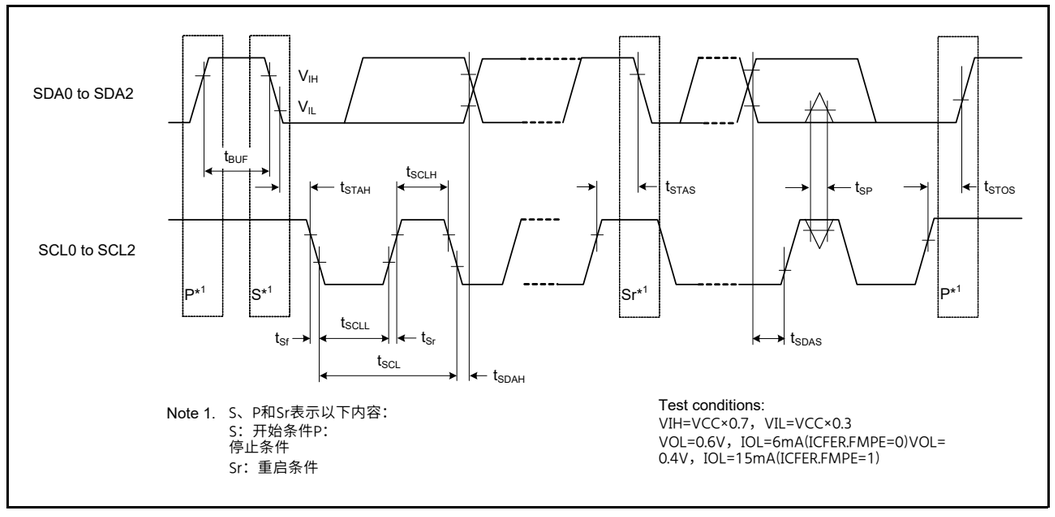


Figure 60.60 I2C总线接口输入输出时序

60.3.14 SSIE Timing

Table 60.29 SSIE timing

(1) High drive output is selected with the port drive capability bit in the PmnPFS register.
(2) Use pins that have a letter appended to their names, for instance "_A" or "_B" to indicate group membership. For the SSIE interface, the AC portion of the electrical characteristics is measured for each group.

Parameter			Symbol	Target specification		Unit	Comments
				Min.	Max.		
SSIBCK	Cycle	Master	t_O	80	-	ns	Figure 60.61
		Slave	t_I	80	-	ns	
	High level/ low level	Master	t_{HC}/t_{LC}	0.35	-	t_O	
		Slave		0.35	-	t_I	
	Rising time/falling time	Master	t_{RC}/t_{FC}	-	0.15	t_O / t_I	
		Slave		-	0.15	t_O / t_I	
SSILRCK/SSIFS, SSITXD0, SSIRXD0, SSIDATA1	Input set up time	Master	t_{SR}	12	-	ns	Figure 60.63, Figure 60.64
		Slave		12	-	ns	
	Input hold time	Master	t_{HR}	8	-	ns	
		Slave		15	-	ns	
	Output delay time	Master	t_{DTR}	-10	5	ns	
		Slave		0	20	ns	Figure 60.63, Figure 60.64
	Output delay time from SSILRCK/SSIFS change	Slave	t_{DTRW}	-	20	ns	Figure 60.65*1
GTIOC1A, AUDIO_CLK	Cycle		t_{EXcyc}	20	-	ns	Figure 60.62
	High level/ low level		t_{EXL}/ t_{EXH}	0.4	0.6	t_{EXcyc}	

Note 1. For slave-mode transmission, SSIE has a path, through which the signal input from the SSILRCK/SSIFS pin is used to generate transmit data, and the transmit data is logically output to the SSITXD0 or SSIDATA1 pin.

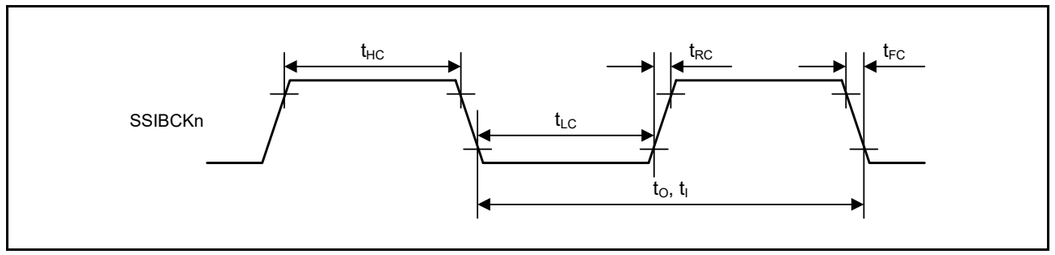


Figure 60.61 SSIE clock input/output timing

60.3.14 SSIE Timing

表60.29SSIE时序(1)通过PmnPFS寄存器中的端口驱动能力位选择高驱动输出。(2)使用名称后附有字母的引脚，例如"_A"或"_B"来表示组成员身份。对于SSIE接口，测量每组的电气特性的交流部分。

Parameter			Symbol	目标规格		Unit	Comments
				Min.	Max.		
SSIBCK	Cycle	Master	t_O	80	-	ns	Figure 60.61
		Slave	t_I	80	-	ns	
	高电平低电平	Master	t_{HC}/t_{LC}	0.35	-	t_O	
		Slave		0.35	-	t_I	
	上升时间下降时间	Master	t_{RC}/t_{FC}	-	0.15	t_O / t_I	
		Slave		-	0.15	t_O / t_I	
SSILRCK/SSIFS, SSITXD0, SSIRXD0, SSIDATA1	输入建立时间	Master	t_{SR}	12	-	ns	Figure 60.63, Figure 60.64
		Slave		12	-	ns	
	输入保持时间	Master	t_{HR}	8	-	ns	
		Slave		15	-	ns	
	输出延迟时间	Master	t_{DTR}	-10	5	ns	
		Slave		0	20	ns	Figure 60.63, Figure 60.64
	从输出延迟时间 SSILRCK/SSIFS change	Slave	t_{DTRW}	-	20	ns	Figure 60.65*1
GTIOC1A, AUDIO_CLK	Cycle		t_{EXcyc}	20	-	ns	Figure 60.62
	高电平低电平		t_{EXL}/ t_{EXH}	0.4	0.6	t_{EXcyc}	

Note 1. 对于从模式传输，SSIE有一个路径，通过该路径，从SSILRCKSSIFS引脚输入的信号用于生成传输数据，传输数据逻辑输出到SSITXD0或SSIDATA1引脚。

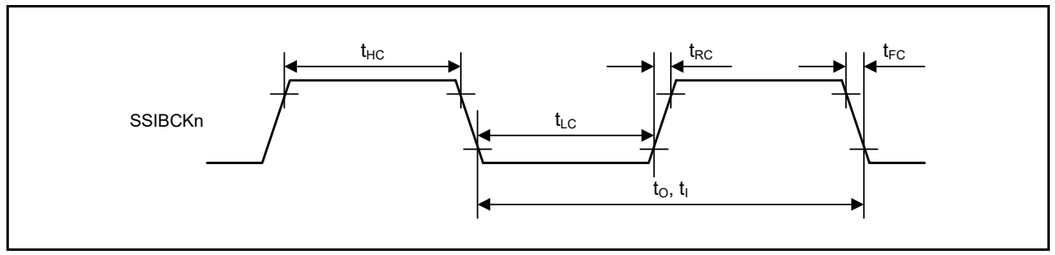


Figure 60.61 SSIE时钟输入输出时序

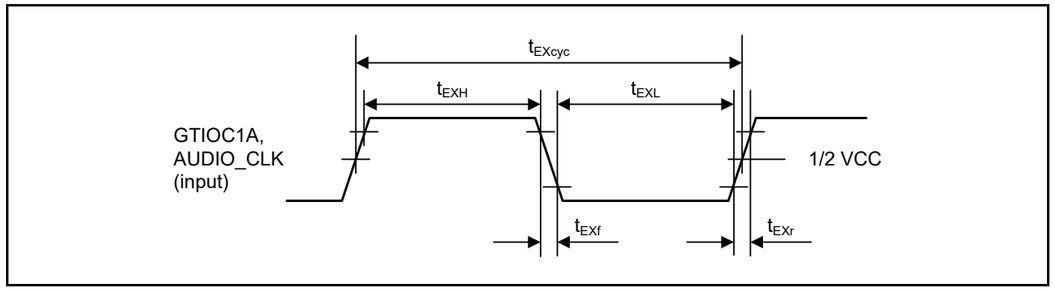


Figure 60.62 Clock input timing

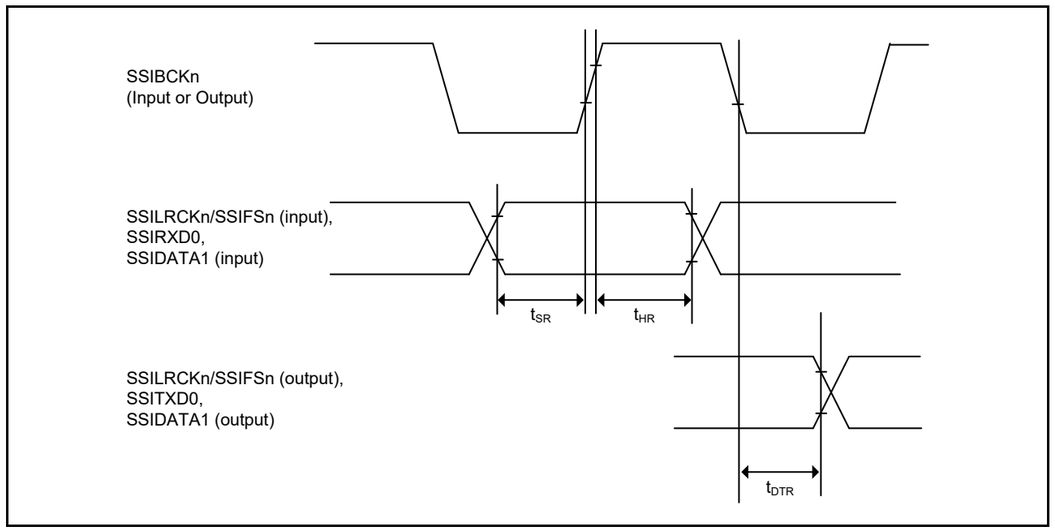


Figure 60.63 SSIE data transmit and receive timing when SSICR.BCKP = 0

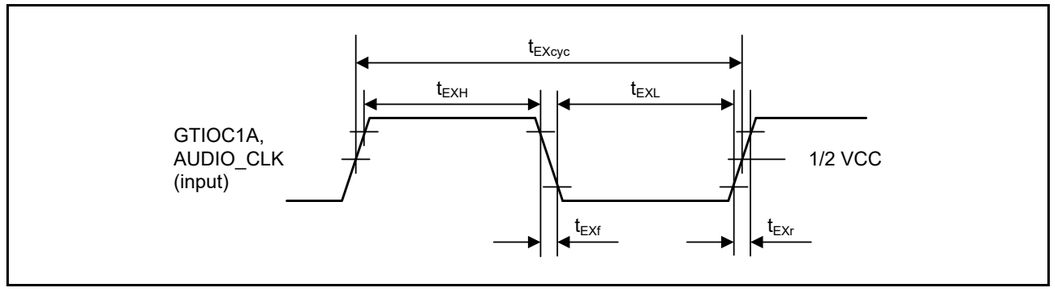


Figure 60.62 时钟输入时序

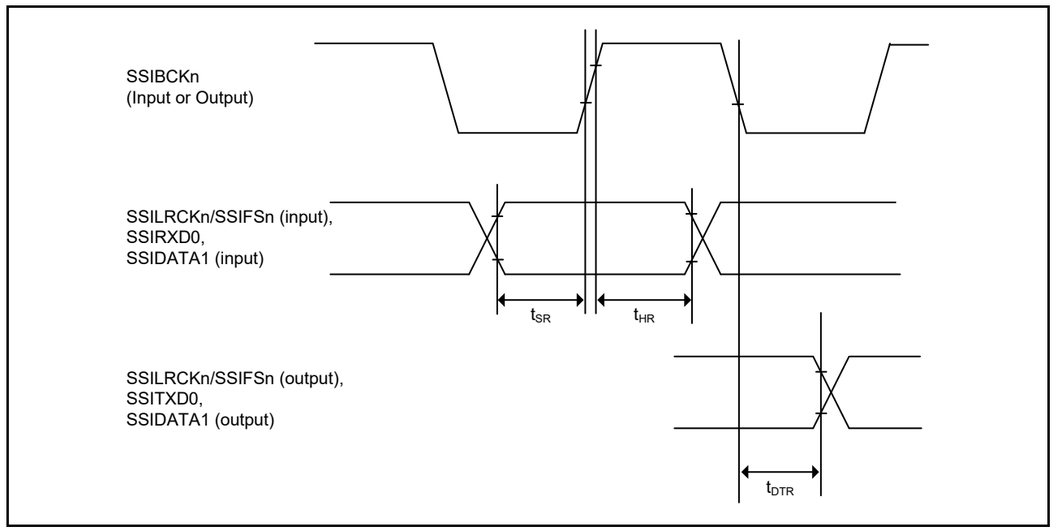


Figure 60.63 SSICR.BCKP=0时的SSIE数据发送和接收时序

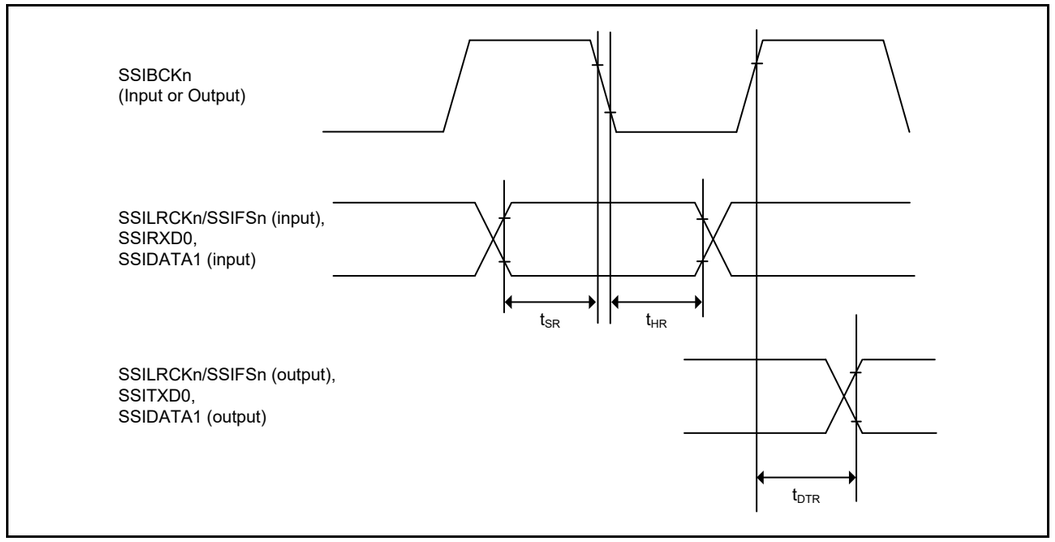


Figure 60.64 SSIE data transmit and receive timing when SSICR.BCKP = 1

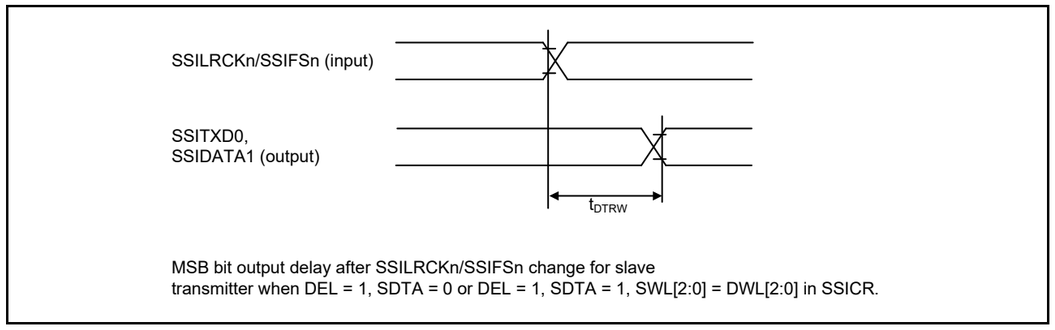


Figure 60.65 SSIE data output delay after SSILRCKn/SSIFSn change

60.3.15 SD/MMC Host Interface Timing

Table 60.30 SD/MMC Host Interface signal timing
Conditions: High drive output is selected in the port drive capability bit in the PmnPFS register.
Clock duty ratio is 50%.

Parameter	Symbol	Min	Max	Unit	Test conditions*1
SDCLK clock cycle	T_{SDCYC}	20	-	ns	Figure 60.66
SDCLK clock high pulse width	T_{SDWH}	6.5	-	ns	
SDCLK clock low pulse width	T_{SDWL}	6.5	-	ns	
SDCLK clock rise time	T_{SDLH}	-	3	ns	
SDCLK clock fall time	T_{SDHL}	-	3	ns	
SDCMD/SDDAT output data delay	T_{SDODLY}	-6	5	ns	
SDCMD/SDDAT input data setup	T_{SDIS}	4	-	ns	
SDCMD/SDDAT input data hold	T_{SDIH}	2	-	ns	

Note 1. Must use pins that have a letter (“_A”, “_B”) to indicate group membership appended to their name as groups. For

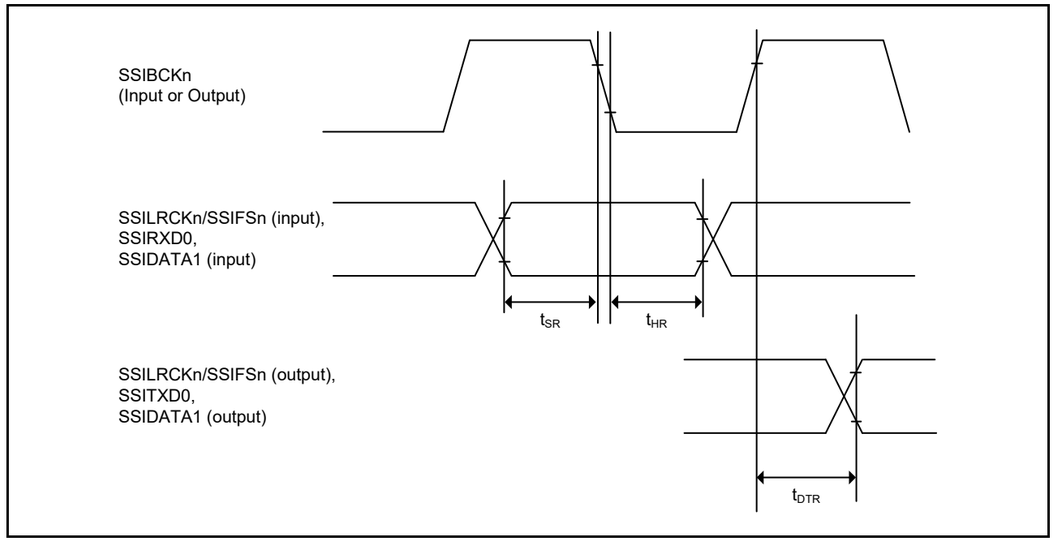


Figure 60.64 SSICR.BCKP=1时的SSIE数据发送和接收时序

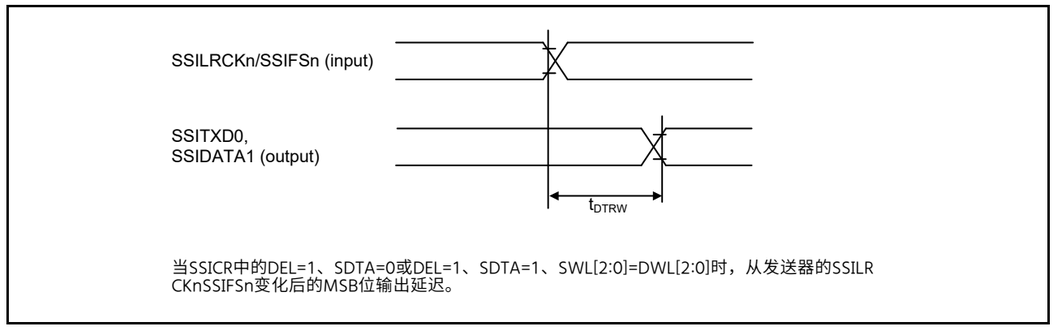


Figure 60.65 SSILRCKnSSIFSn改变后的SSIE数据输出延迟

60.3.15 SDMMC主机接口时序

Table 60.30 SDMMC主机接口信号时序
条件：在PmnPFS寄存器的端口驱动能力位中选择高驱动输出。
时钟占空比为50%。

Parameter		Symbol	Min	Max	Unit	Test conditions*1
SDCLK	时钟周期	T_{SDCYC}	20	-	ns	Figure 60.66
SDCLK	时钟高脉冲宽度	T_{SDWH}	6.5	-	ns	
SDCLK	时钟低脉冲宽度	T_{SDWL}	6.5	-	ns	
SDCLK	时钟上升时间	T_{SDLH}	-	3	ns	
SDCLK	时钟下降时间	T_{SDHL}	-	3	ns	
SDCMDSDDAT输出数据延迟		T_{SDODLY}	-6	5	ns	
SDCMDSDDAT输入数据设置		T_{SDIS}	4	-	ns	
SDCMDSDDAT输入数据保持		T_{SDIH}	2	-	ns	

注1.必须使用带有字母（“_A”、“_B”）的引脚来表示作为组附加在其名称后的组成员身份。为了

the SD/MMC Host interface, the AC portion of the electrical characteristics is measured for each group.

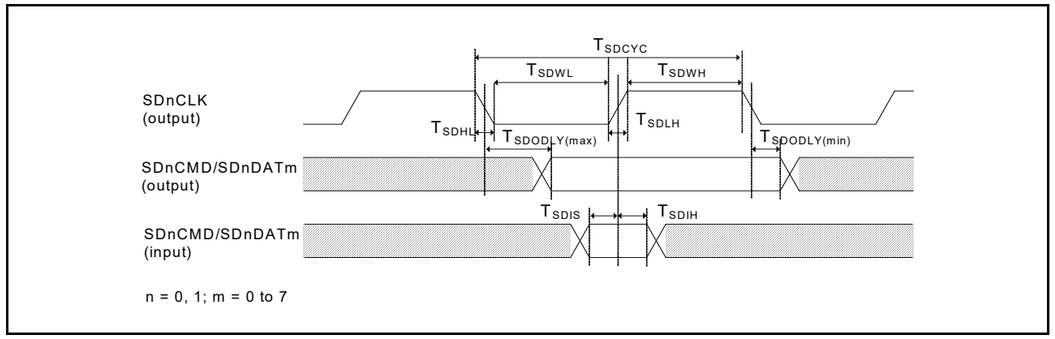


Figure 60.66 SD/MMC Host Interface signal timing

60.3.16 ETHERC Timing

Table 60.31 ETHERC timing
Conditions: ETHERC (RMII): Middle drive output is selected in the port drive capability bit in the PmnPFS register for the following pins: ET0_MDC, ET0_MDIO.
For other pins, high drive output is selected in the port drive capability bit in the PmnPFS register.
ETHERC (MII): Middle drive output is selected in the port drive capability bit in the PmnPFS register.

Parameter		Symbol	Min	Max	Unit	Test conditions*3
ETHERC (RMII)	REF50CK cycle time	T_{ck}	20	-	ns	Figure 60.67 to Figure 60.70
	REF50CK frequency, typical 50 MHz	-	-	50 + 100 ppm	MHz	
	REF50CK duty	-	35	65	%	
	REF50CK rise/fall time	$T_{ckr/ckf}$	0.5	3.5	ns	
	RMII0_xxxx*1 output delay	T_{co}	2.5	12.0	ns	
	RMII0_xxxx*2 setup time	T_{su}	3	-	ns	
	RMII0_xxxx*2 hold time	T_{hd}	1	-	ns	
	RMII0_xxxx*1, *2 rise/fall time	T_r/T_f	0.5	4	ns	
	ET0_WOL output delay	t_{WOLd}	1	23.5	ns	Figure 60.71
ETHERC (MII)	ET0_TX_CLK cycle time	t_{Tcyc}	40	-	ns	-
	ET0_TX_EN output delay	t_{TENd}	1	20	ns	Figure 60.72
	ET0_ETXD0 to ET0_ETXD3 output delay	t_{MTDd}	1	20	ns	
	ET0_CRS setup time	t_{CRSs}	10	-	ns	
	ET0_CRS hold time	t_{CRSh}	10	-	ns	
	ET0_COL setup time	t_{COLs}	10	-	ns	Figure 60.73
	ET0_COL hold time	t_{COLh}	10	-	ns	
	ET0_RX_CLK cycle time	t_{TRcyc}	40	-	ns	-
	ET0_RX_DV setup time	t_{RDVs}	10	-	ns	Figure 60.74
	ET0_RX_DV hold time	t_{RDVh}	10	-	ns	
	ET0_ERXD0 to ET0_ERXD3 setup time	t_{MRDs}	10	-	ns	
	ET0_ERXD0 to ET0_ERXD3 hold time	t_{MRDh}	10	-	ns	
	ET0_RX_ER setup time	t_{RERs}	10	-	ns	Figure 60.75
	ET0_RX_ER hold time	t_{RESh}	10	-	ns	
	ET0_WOL output delay	t_{WOLd}	1	23.5	ns	Figure 60.76

Note 1. RMII0_TXD_EN, RMII0_TXD1, RMII0_TXD0.
Note 2. RMII0_CRS_DV, RMII0_RXD1, RMII0_RXD0, RMII0_RX_ER.

SDMMC主机接口，测量每组电气特性的交流部分。

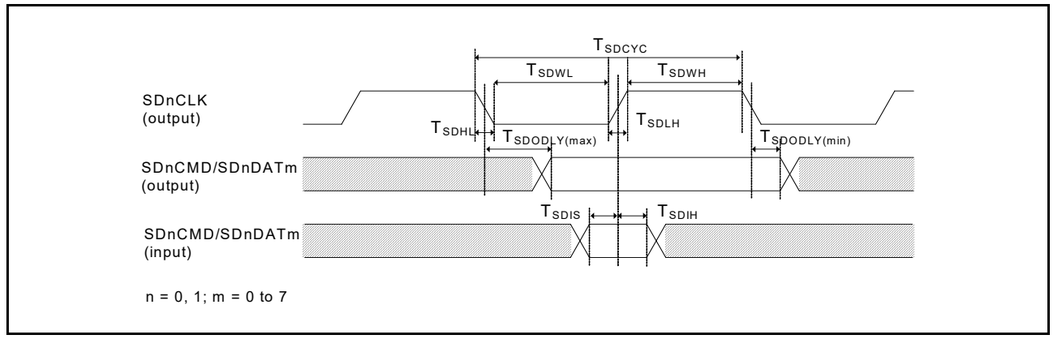


Figure 60.66 SDMMC主机接口信号时序

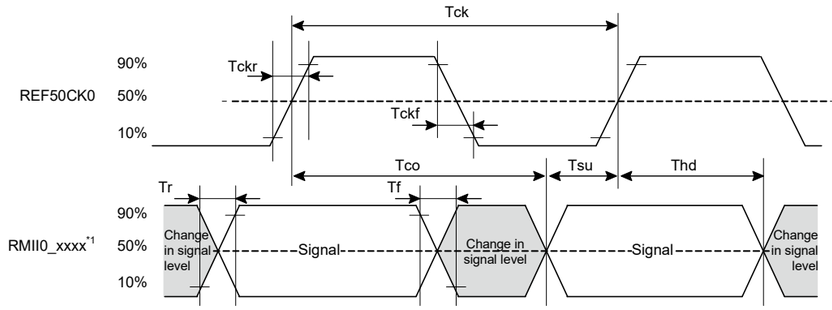
60.3.16 ETHERC Timing

Table 60.31 ETHERC timing
条件：ETHERC(RMII)：在PmnPFS寄存器的端口驱动能力位中为以下引脚选择中间驱动输出：
ET0_MDC, ET0_MDIO.
对于其他引脚，在PmnPFS寄存器的端口驱动能力位中选择高驱动输出。
ETHERC(MII)：在PmnPFS寄存器的端口驱动能力位中选择中间驱动输出。

Parameter		Symbol	Min	Max	Unit	Test conditions*3
ETHERC (RMII)	REF50CK循环时间	T_{ck}	20	-	ns	图60.67至 Figure 60.70
	REF50CK频率，典型值50MHz	-	-	50 + 100 ppm	MHz	
	REF50CK duty	-	35	65	%	
	REF50CK rise/fall time	$T_{ckr/ckf}$	0.5	3.5	ns	
	RMII0_xxxx*1输出延迟	T_{co}	2.5	12.0	ns	
	RMII0_xxxx*2建立时间	T_{su}	3	-	ns	
	RMII0_xxxx*2保持时间	T_{hd}	1	-	ns	
	RMII0_xxxx*1, *2 rise/fall time	T_r/T_f	0.5	4	ns	
	ET0_WOL输出延迟	t_{WOLd}	1	23.5	ns	Figure 60.71
ETHERC (MII)	ET0_TX_CLK周期时间	t_{Tcyc}	40	-	ns	-
	ET0_TX_EN输出延迟	t_{TENd}	1	20	ns	Figure 60.72
	ET0_ETXD0到ET0_ETXD3输出延迟	t_{MTDd}	1	20	ns	
	ET0_CRS建立时间	t_{CRSs}	10	-	ns	
	ET0_CRS保持时间	t_{CRSh}	10	-	ns	
	ET0_COL建立时间	t_{COLs}	10	-	ns	Figure 60.73
	ET0_COL保持时间	t_{COLh}	10	-	ns	
	ET0_RX_CLK周期时间	t_{TRcyc}	40	-	ns	-
	ET0_RX_DV建立时间	t_{RDVs}	10	-	ns	Figure 60.74
	ET0_RX_DV保持时间	t_{RDVh}	10	-	ns	
	ET0_ERXD0到ET0_ERXD3建立时间	t_{MRDs}	10	-	ns	
	ET0_ERXD0到ET0_ERXD3保持时间	t_{MRDh}	10	-	ns	
	ET0_RX_ER建立时间	t_{RERs}	10	-	ns	Figure 60.75
	ET0_RX_ER保持时间	t_{RESh}	10	-	ns	
	ET0_WOL输出延迟	t_{WOLd}	1	23.5	ns	Figure 60.76

Note 1. RMII0_TXD_EN, RMII0_TXD1, RMII0_TXD0.
Note 2. RMII0_CRS_DV, RMII0_RXD1, RMII0_RXD0, RMII0_RX_ER.

Note 3. The following pins, must use pins that have a letter (“_A”, “_B”) to indicate group membership appended to their name as groups. For the ETHERC (RMII) Host interface, the AC portion of the electrical characteristics is measured for each group. REF50CK0_A, REF50CK0_B, RMII0_xxxx_A, RMII0_xxxx_B



Note 1. RMII0_TXD_EN, RMII0_TXD1, RMII0_TXD0, RMII0_CRS_DV, RMII0_RXD1, RMII0_RXD0, RMII0_RX_ER

Figure 60.67 REF50CK0 and RMII signal timing

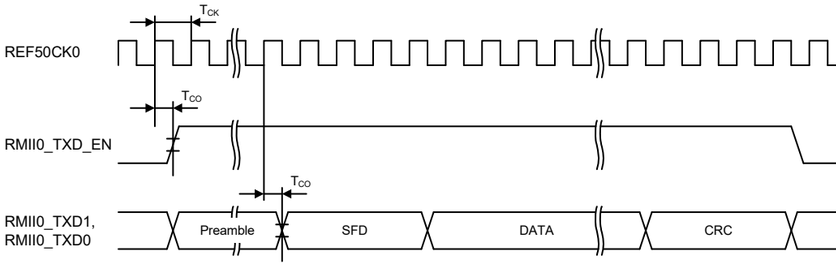


Figure 60.68 RMII transmission timing

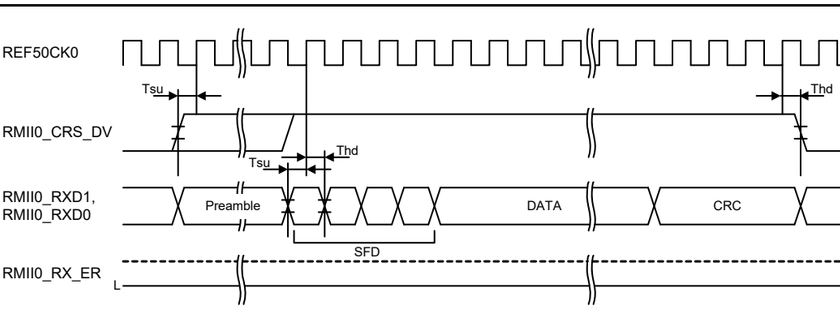
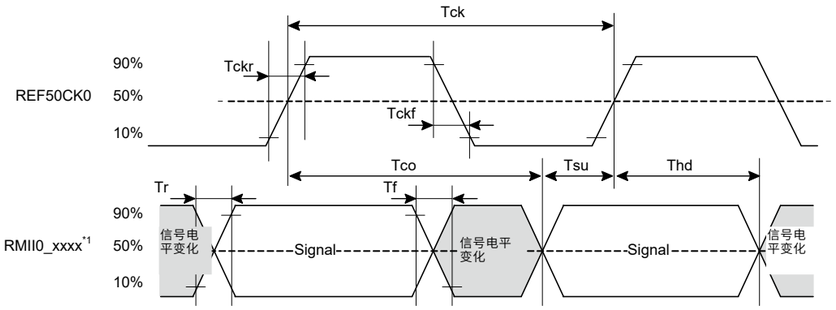


Figure 60.69 RMII reception timing in normal operation

Note 3. 以下管脚必须使用带有字母（“_A”、“_B”）的管脚来表示作为组附加到其名称的组成员身份。对于ETHERC(RMII)主机接口，测量每组的电气特性的交流部分。REF50CK0_A、REF50CK0_B、RMII0_xxxx_A、RMII0_xxxx_B



Note 1. RMII0_TXD_EN, RMII0_TXD1, RMII0_TXD0, RMII0_CRS_DV, RMII0_RXD1, RMII0_RXD0, RMII0_RX_ER

Figure 60.67 REF50CK0和RMII信号时序

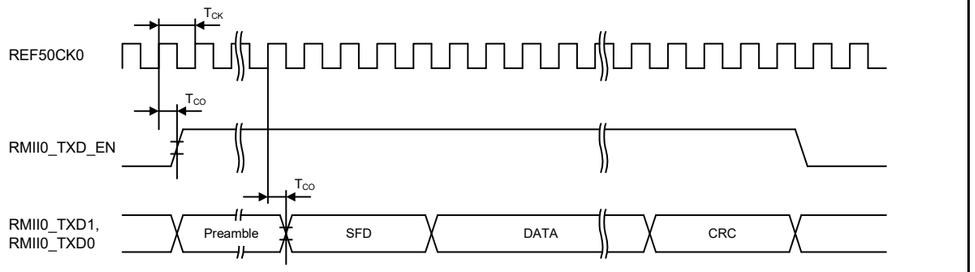


Figure 60.68 RMII传输时序

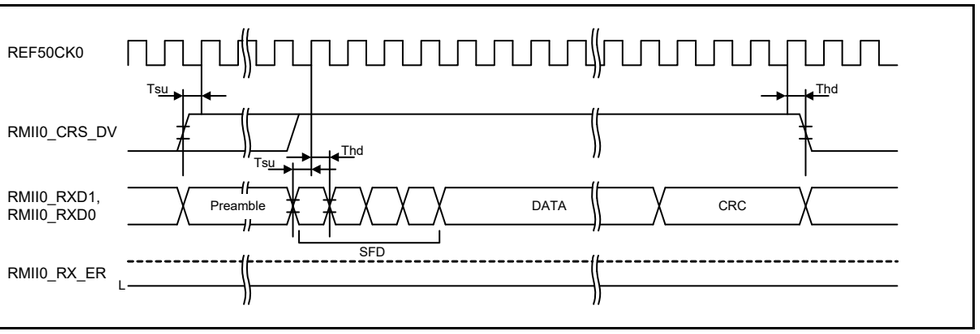


Figure 60.69 正常操作中的RMII接收时序

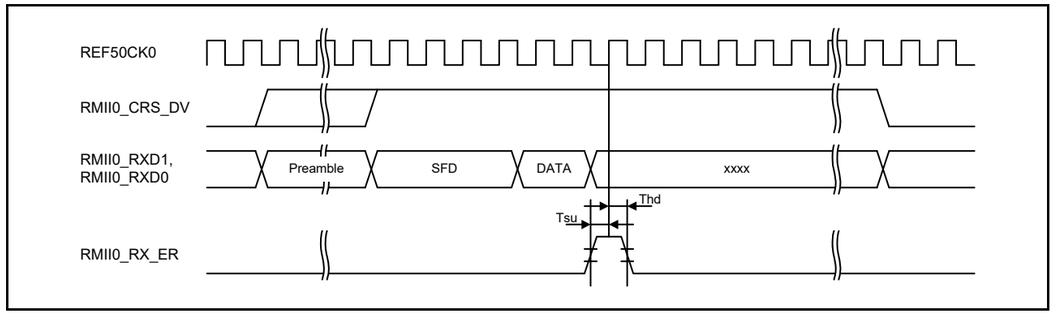


Figure 60.70 RMII reception timing when an error occurs

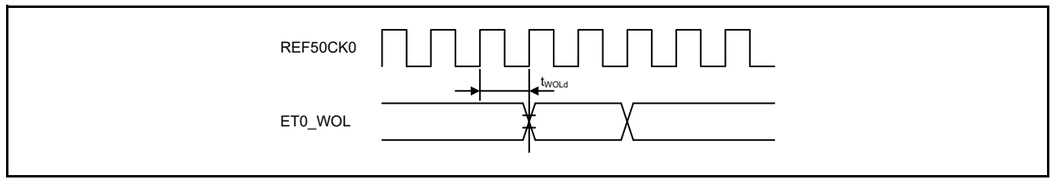


Figure 60.71 WOL output timing for RMII

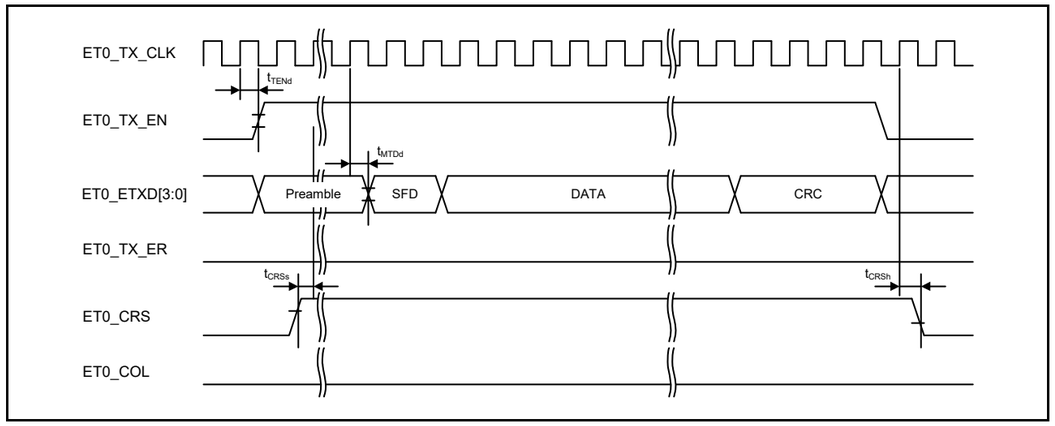


Figure 60.72 MII transmission timing in normal operation

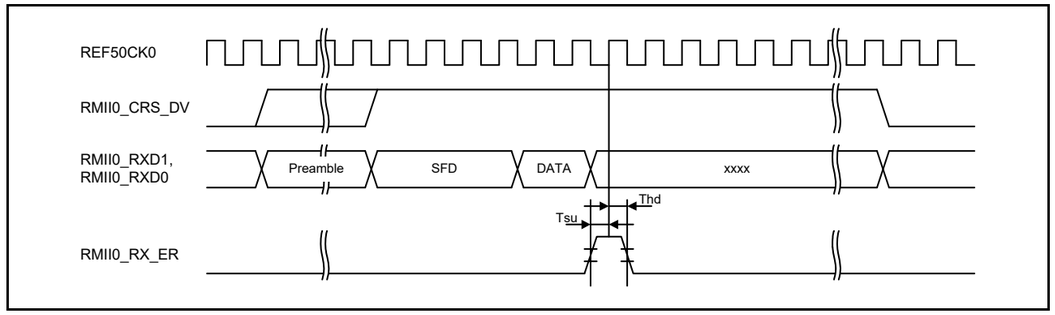


Figure 60.70 发生错误时的RMII接收时序

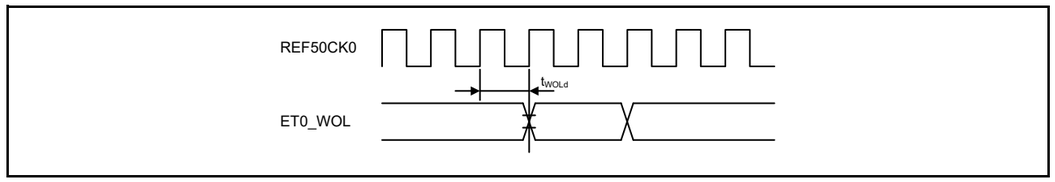


Figure 60.71 RMII的WOL输出时序

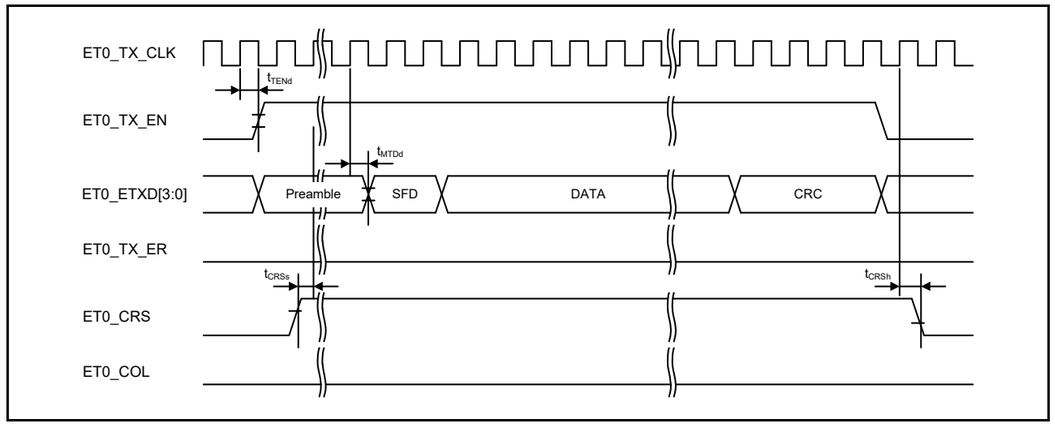


Figure 60.72 正常操作中的MII传输时序

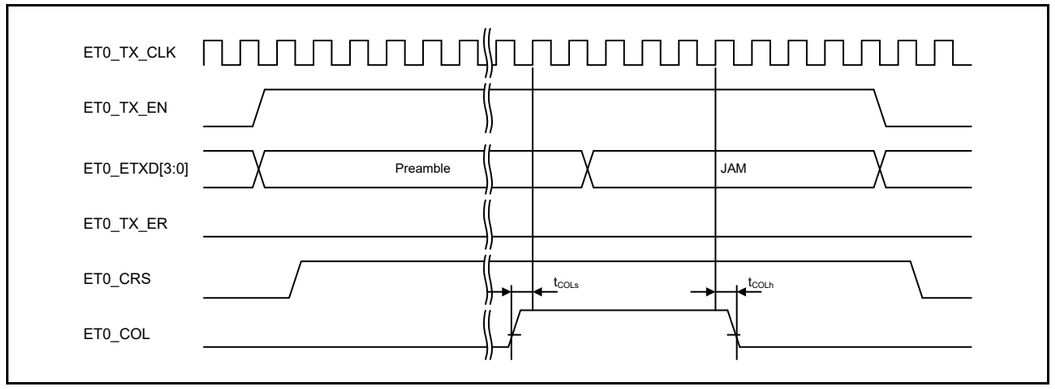


Figure 60.73 MII transmission timing when a conflict occurs

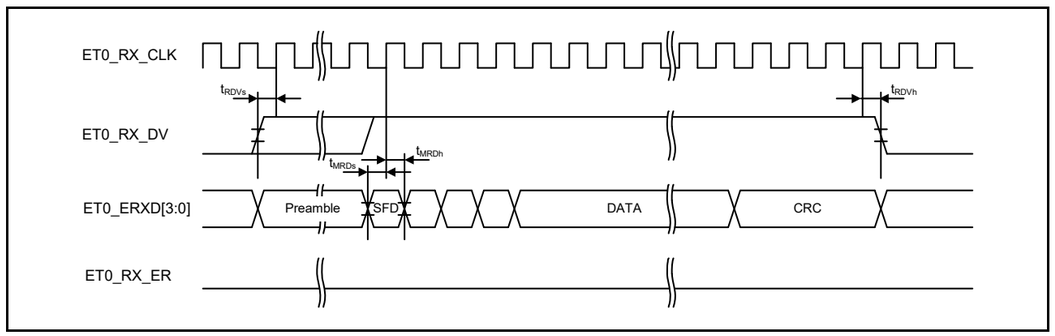


Figure 60.74 MII reception timing in normal operation

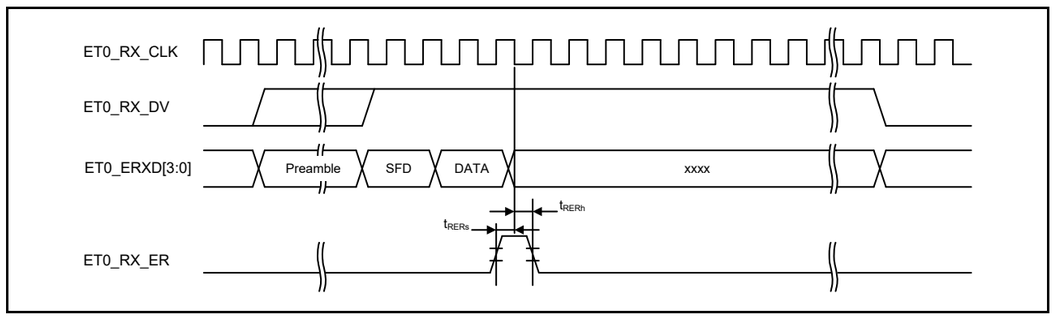


Figure 60.75 MII reception timing when an error occurs

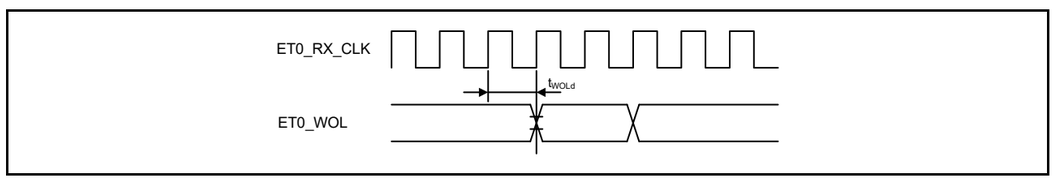


Figure 60.76 WOL output timing for MII

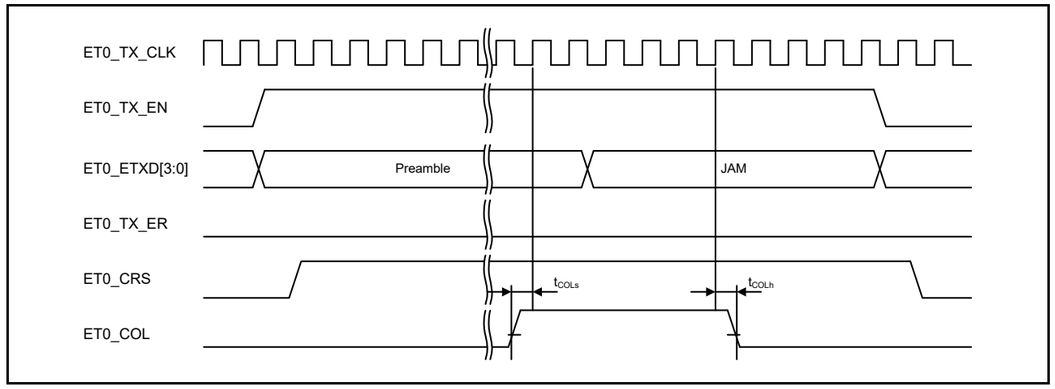


Figure 60.73 发生冲突时的MII传输时序

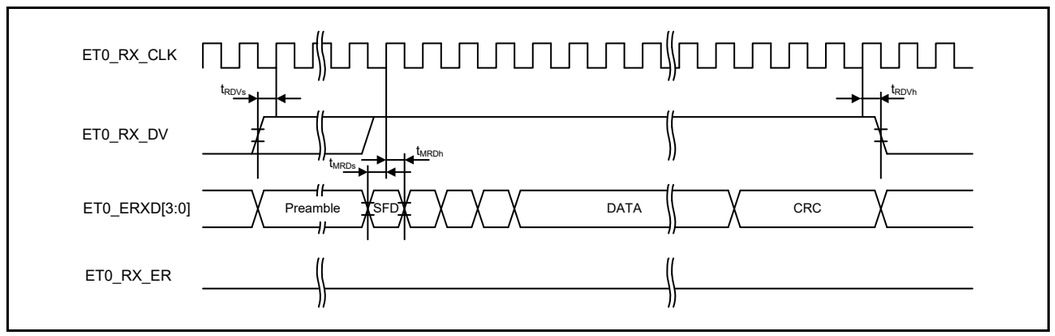


Figure 60.74 正常操作中的MII接收时序

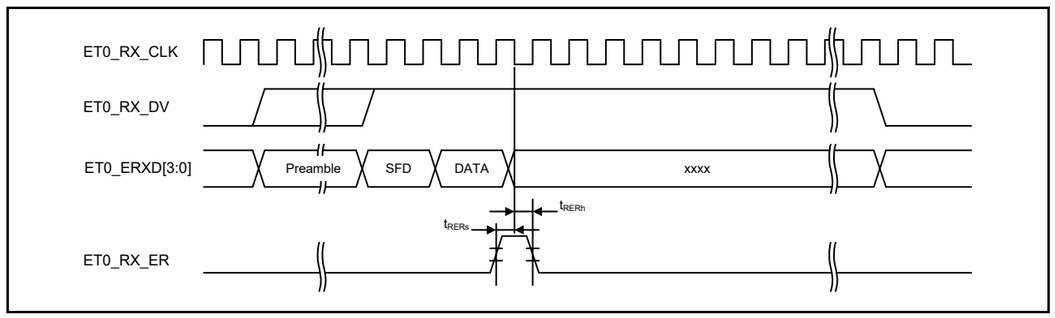


Figure 60.75 发生错误时的MII接收时序

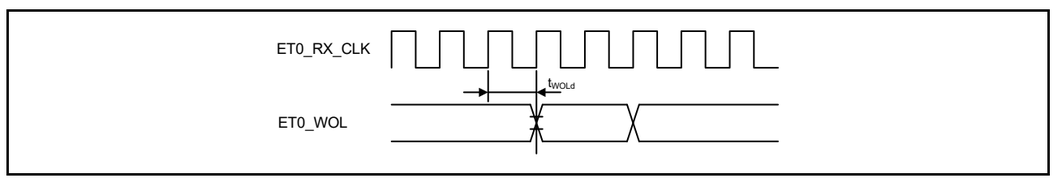


Figure 60.76 MII的WOL输出时序

60.3.17 PDC Timing

Table 60.32 PDC timing
Conditions: Middle drive output is selected in the port drive capability bit in the PmnPFS register.
Output load conditions: V_{OH} = VCC × 0.5, V_{OL} = VCC × 0.5, C = 30 pF

Parameter		Symbol	Min	Max	Unit	Test conditions
PDC	PIXCLK input cycle time	t_{PIXcyc}	37	-	ns	Figure 60.77
	PIXCLK input high pulse width	t_{PIXH}	10	-	ns	
	PIXCLK input low pulse width	t_{PIXL}	10	-	ns	
	PIXCLK rise time	t_{PIXr}	-	5	ns	
	PIXCLK fall time	t_{PIXf}	-	5	ns	
	PCKO output cycle time	t_{PCKcyc}	2 × t_{PBcyc}	-	ns	Figure 60.78
	PCKO output high pulse width	t_{PCKH}	(t_{PCKcyc} - t_{PCKr} - t_{PCKf})/2 - 3	-	ns	
	PCKO output low pulse width	t_{PCKL}	(t_{PCKcyc} - t_{PCKr} - t_{PCKf})/2 - 3	-	ns	
	PCKO rise time	t_{PCKr}	-	5	ns	
	PCKO fall time	t_{PCKf}	-	5	ns	
	VSYNV/HSYNC input setup time	t_{SYNCS}	10	-	ns	Figure 60.79
	VSYNV/HSYNC input hold time	t_{SYNCH}	5	-	ns	
	PIXD input setup time	t_{PIXDS}	10	-	ns	
	PIXD input hold time	t_{PIXDH}	5	-	ns	

Note 1. t_{PBcyc}: PCLKB cycle.

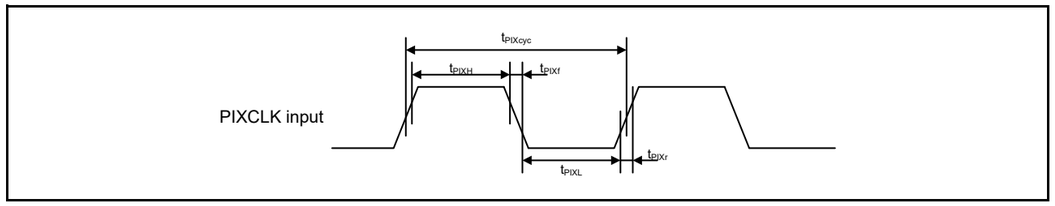


Figure 60.77 PDC input clock timing

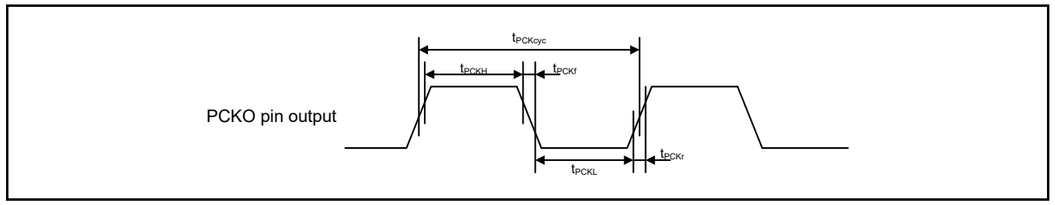


Figure 60.78 PDC output clock timing

60.3.17 PDC Timing

Table 60.32 PDC timing
条件：在PmnPFS寄存器的端口驱动能力位中选择中间驱动输出。
输出负载条件：VOH=VCC×0.5，VOL=VCC×0.5，C=30pF

Parameter		Symbol	Min	Max	Unit	测试条件
PDC	PIXCLK输入周期时间	t_{PIXcyc}	37	-	ns	Figure 60.77
	PIXCLK输入高脉冲宽度	t_{PIXH}	10	-	ns	
	PIXCLK输入低脉冲宽度	t_{PIXL}	10	-	ns	
	PIXCLK上升时间	t_{PIXr}	-	5	ns	
	PIXCLK下降时间	t_{PIXf}	-	5	ns	
	PCKO输出循环时间	t_{PCKcyc}	2 × t_{PBcyc}	-	ns	Figure 60.78
	PCKO输出高脉冲宽度	t_{PCKH}	(t_{PCKcyc} - t_{PCKr} - t_{PCKf})/2 - 3	-	ns	
	PCKO输出低脉冲宽度	t_{PCKL}	(t_{PCKcyc} - t_{PCKr} - t_{PCKf})/2 - 3	-	ns	
	PCKO上升时间	t_{PCKr}	-	5	ns	
	PCKO下降时间	t_{PCKf}	-	5	ns	
	VSYNVHSYNC输入建立时间	t_{SYNCS}	10	-	ns	Figure 60.79
	VSYNVHSYNC输入保持时间	t_{SYNCH}	5	-	ns	
	PIXD输入建立时间	t_{PIXDS}	10	-	ns	
	PIXD输入保持时间	t_{PIXDH}	5	-	ns	

Note 1. t_{PBcyc}: PCLKB cycle.

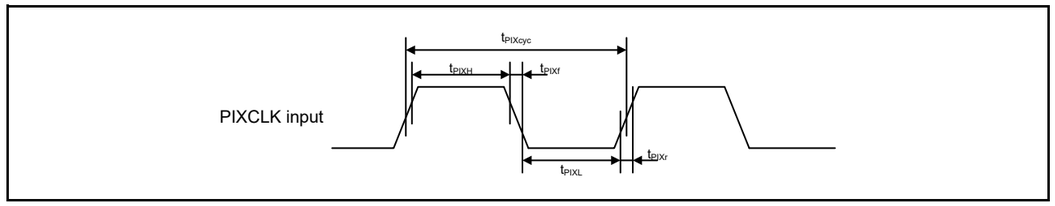


Figure 60.77 PDC输入时钟时序

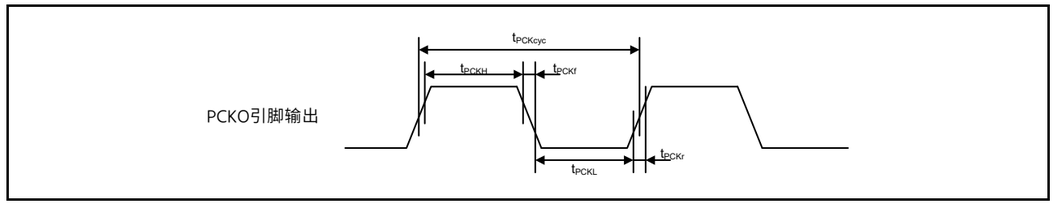


Figure 60.78 PDC输出时钟时序

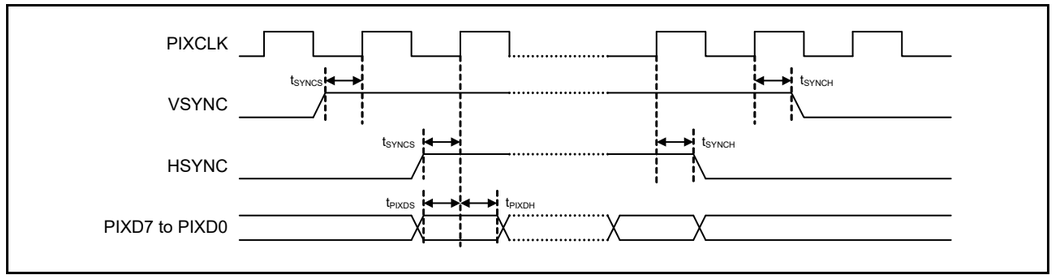


Figure 60.79 PDC AC timing

60.3.18 GLCDC Timing

Table 60.33 GLCDC timing
Conditions:
LCD_CLK: High drive output is selected in the port drive capability bit in the PmnPFS register.
LCD_DATA: Middle drive output is selected in the port drive capability bit in the PmnPFS register.

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
LCD_EXTCLK input clock frequency		t_{Ecyc}	-	-	60*1	MHz	Figure 60.80
LCD_EXTCLK input clock low pulse width		t_{WL}	0.45	-	0.55	t_{Ecyc}	
LCD_EXTCLK input clock high pulse width		t_{WH}	0.45	-	0.55		
LCD_CLK output clock frequency		t_{Lcyc}	-	-	60*1	MHz	Figure 60.81
LCD_CLK output clock low pulse width		t_{LOL}	0.4	-	0.6	t_{Lcyc}	Figure 60.81
LCD_CLK output clock high pulse width		t_{LOH}	0.4	-	0.6	t_{Lcyc}	Figure 60.81
LCD data output delay timing	_A or _B combinations*2	t_{DD}	-3.5	-	4	ns	Figure 60.82
	_A and _B combinations*3		-5.0	-	5.5		

Note 1. Parallel RGB888, 666,565: Maximum 54 MHz
Serial RGB888: Maximum 60 MHz (4x speed)
Note 2. Use pins that have a letter appended to their names, for instance, “_A” or “_B”, to indicate
Note 3. Pins of group “_A” and “_B” combinations are used.

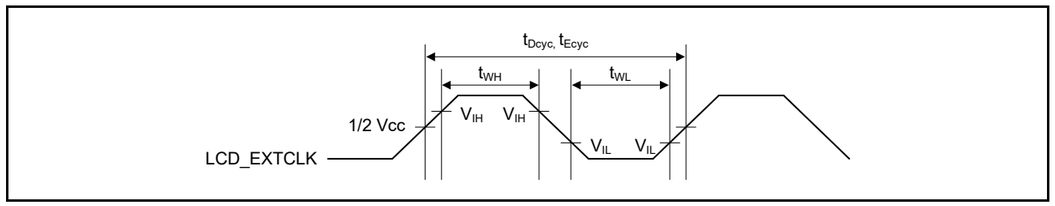


Figure 60.80 LCD_EXTCLK clock input timing

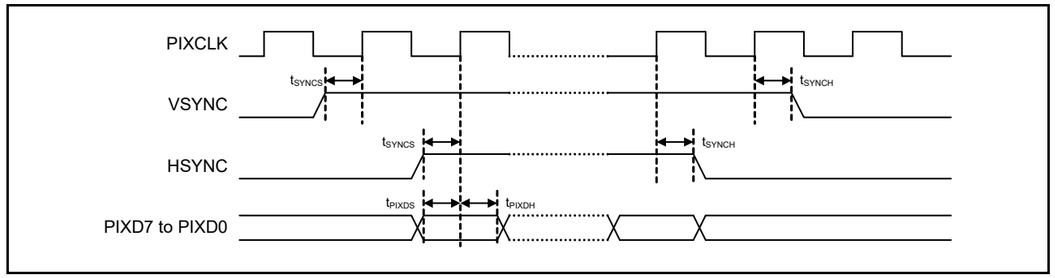


Figure 60.79 PDC交流正时

60.3.18 GLCDC Timing

Table 60.33 GLCDC timing
Conditions:
LCD_CLK：在PmnPFS寄存器的端口驱动能力位中选择高驱动输出。
LCD_DATA：在PmnPFS寄存器的端口驱动能力位中选择中间驱动输出。

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
LCD_EXTCLK输入时钟频率		t_{Ecyc}	-	-	60*1	MHz	Figure 60.80
LCD_EXTCLK输入时钟低脉冲宽度		t_{WL}	0.45	-	0.55	t_{Ecyc}	
LCD_EXTCLK输入时钟高脉冲宽度		t_{WH}	0.45	-	0.55		
LCD_CLK输出时钟频率		t_{Lcyc}	-	-	60*1	MHz	Figure 60.81
LCD_CLK输出时钟低脉冲宽度		t_{LOL}	0.4	-	0.6	t_{Lcyc}	Figure 60.81
LCD_CLK输出时钟高脉冲宽度		t_{LOH}	0.4	-	0.6	t_{Lcyc}	Figure 60.81
LCD数据输出延迟时序	_A or _B combinations*2	t_{DD}	-3.5	-	4	ns	Figure 60.82
	_A and _B combinations*3		-5.0	-	5.5		

Note 1. 并行RGB888、666 565：最大54MHz串行RG
B888：最大60MHz（4倍速）
Note 2. 使用名称后附有字母（例如“_A”或“_B”）的引脚来表示
Note 3. 使用组“_A”和“_B”组合的引脚。

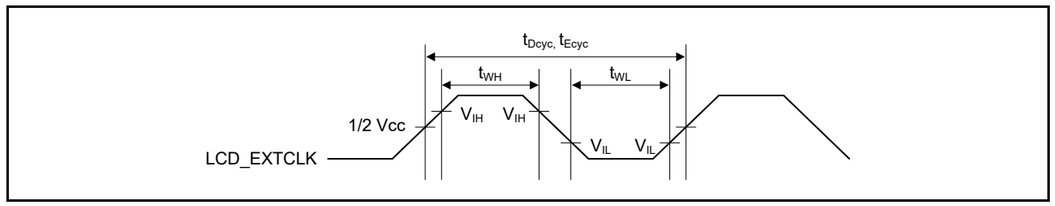


Figure 60.80 LCD_EXTCLK时钟输入时序

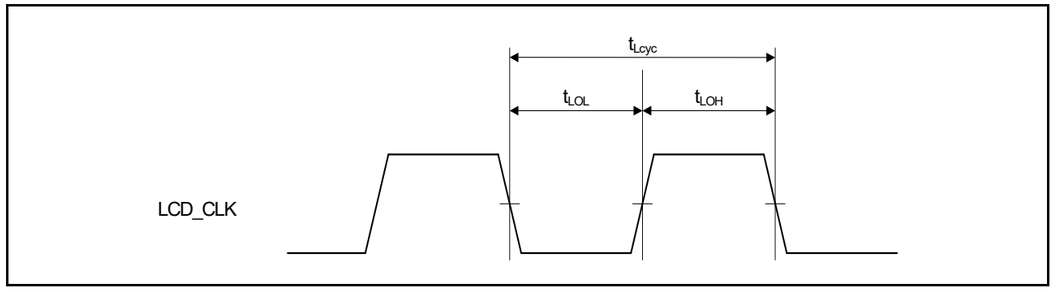


Figure 60.81 LCD_CLK clock output timing

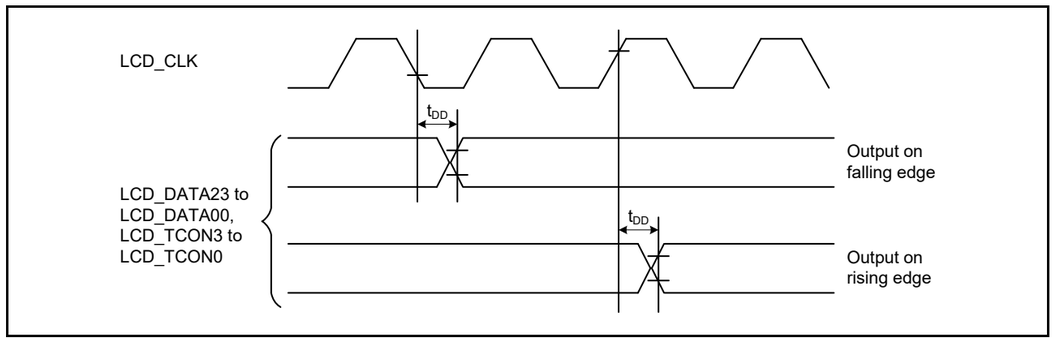


Figure 60.82 Display output timing

60.4 USB Characteristics

60.4.1 USBHS Timing

Table 60.34 USBHS low-speed characteristics for host only (USBHS_DP and USBHS_DM pin characteristics)
Conditions: USBHS_RREF = 2.2 kΩ ± 1%, USBMCLK = 12/20/24 MHz, UCLK = 48 MHz

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions	
Input characteristics	Input high voltage	V_{IH}	2.0	-	-	V	-	-
	Input low voltage	V_{IL}	-	-	0.8	V	-	-
	Differential input sensitivity	V_{DI}	0.2	-	-	V	| USBHS_DP - USBHS_DM |	-
	Differential common-mode range	V_{CM}	0.8	-	2.5	V	-	-
Output characteristics	Output high voltage	V_{OH}	2.8	-	3.6	V	I_{OH} = -200 µA	-
	Output low voltage	V_{OL}	0.0	-	0.3	V	I_{OL}= 2 mA	-
	Cross-over voltage	V_{CRS}	1.3	-	2.0	V	-	Figure 60.83, Figure 60.84
	Rise time	t_{LR}	75	-	300	ns	-	
	Fall time	t_{LF}	75	-	300	ns	-	
	Rise/fall time ratio	t_{LR} / t_{LF}	80	-	125	%	t_{LR} / t_{LF}	-
Pull-up, Pull-down characteristics	USBHS_DP and USBHS_DM pull-down resistors (Host)	R_{pd}	14.25	-	24.80	kΩ	-	

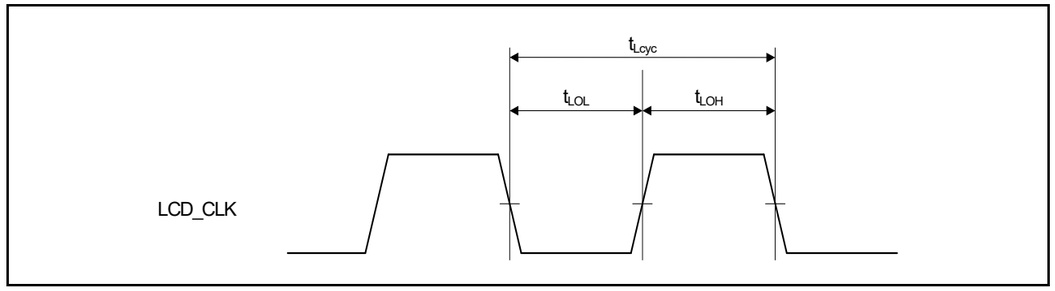


Figure 60.81 LCD_CLK时钟输出时序

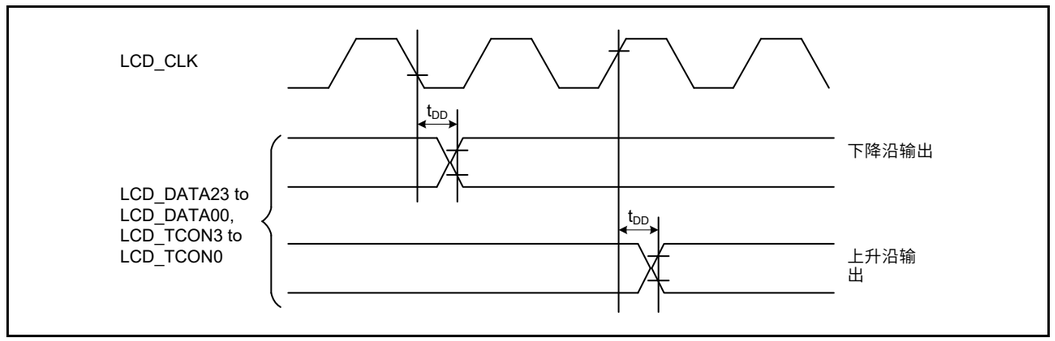


Figure 60.82 显示输出时序

60.4 USB特性

60.4.1 USBHS Timing

Table 60.34 仅主机的USBHS低速特性（USBHS_DP和USBHS_DM引脚特性）
Conditions: USBHS_RREF = 2.2 kΩ ± 1%, USBMCLK = 12/20/24 MHz, UCLK = 48 MHz

Parameter		Symbol	Min	Typ	Max	Unit	测试条件	
输入特性	输入高压	V_{IH}	2.0	-	-	V	-	-
	输入低电压	V_{IL}	-	-	0.8	V	-	-
	差分输入灵敏度	V_{DI}	0.2	-	-	V	| USBHS_DP - USBHS_DM |	-
	差分共模范围	V_{CM}	0.8	-	2.5	V	-	-
输出特性	输出高压	V_{OH}	2.8	-	3.6	V	I_{OH} = -200 µA	-
	输出低电压	V_{OL}	0.0	-	0.3	V	我OL=2毫安	-
	Cross-over voltage	V_{CRS}	1.3	-	2.0	V	-	Figure 60.83, Figure 60.84
	上升时间	t_{LR}	75	-	300	ns	-	
	秋季时间	t_{LF}	75	-	300	ns	-	
	上升下降时间比	t_{LR} / t_{LF}	80	-	125	%	t_{LR} / t_{LF}	-
Pull-up, Pull-down characteristics	USBHS_DP和USBHS_DM下拉电阻（主机）	R_{pd}	14.25	-	24.80	kΩ	-	

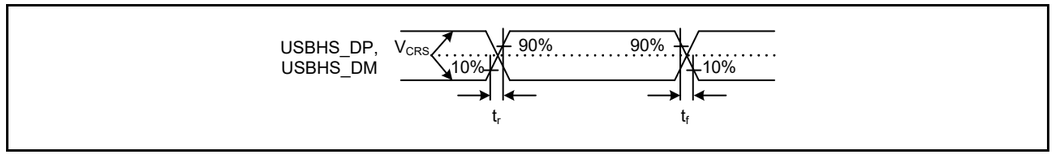


Figure 60.83 USBHS_DP and USBHS_DM output timing in low-speed mode

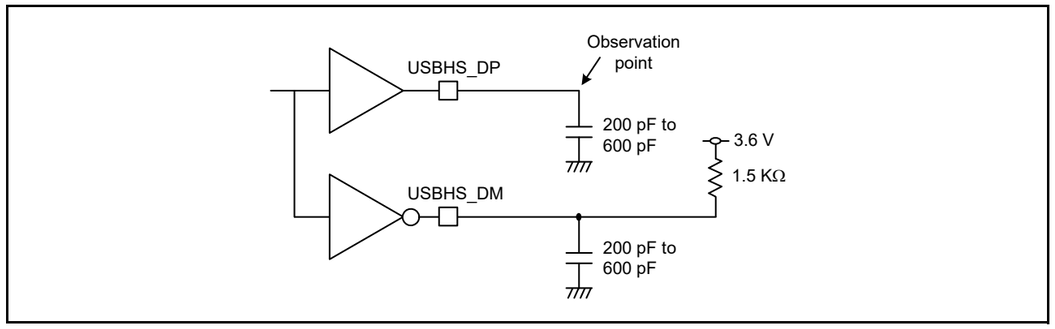


Figure 60.84 Test circuit in low-speed mode

Table 60.35 USBHS full-speed characteristics (USBHS_DP and USBHS_DM pin characteristics)
Conditions: USBHS_RREF = 2.2 kΩ ± 1%, USBMCLK = 12/20/24 MHz, UCLK = 48 MHz

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions	
Input characteristics	Input high voltage	V_{IH}	2.0	-	-	V	-	-
	Input low voltage	V_{IL}	-	-	0.8	V	-	-
	Differential input sensitivity	V_{DI}	0.2	-	-	V	| USBHS_DP - USBHS_DM |	-
	Differential common-mode range	V_{CM}	0.8	-	2.5	V	-	-
Output characteristics	Output high voltage	V_{OH}	2.8	-	3.6	V	I_{OH} = -200 µA	-
	Output low voltage	V_{OL}	0.0	-	0.3	V	I_{OL}= 2 mA	-
	Cross-over voltage	V_{CRS}	1.3	-	2.0	V	-	Figure 60.85, Figure 60.86
	Rise time	t_{LR}	4	-	20	ns	-	
	Fall time	t_{LF}	4	-	20	ns	-	
	Rise/fall time ratio	t_{LR} / t_{LF}	90	-	111.11	%	t_{FR} / t_{FF}	-
	Output resistance	Z_{DRV}	40.5	-	49.5	Ω	Rs Not used (PHYSET.REPSEL[1:0] = 01b and PHYSET. HSEB = 0)	
DC characteristics	USBHS_DM pull-up resistor (device)	R_{pu}	0.900	-	1.575	kΩ	During idle state	
			1.425	-	3.090	kΩ	During transmission and reception	
	USBHS_DP/USBHS_DM pull-down resistor (host)	R_{pd}	14.25	-	24.80	kΩ	-	

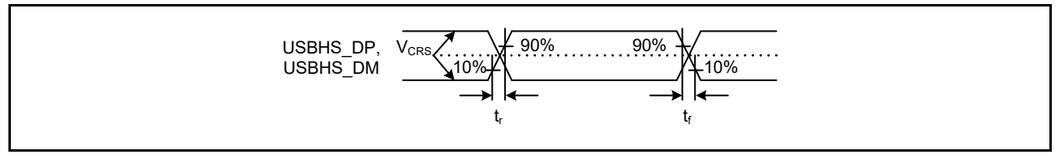


Figure 60.83 低速模式下的USBHS_DP和USBHS_DM输出时序

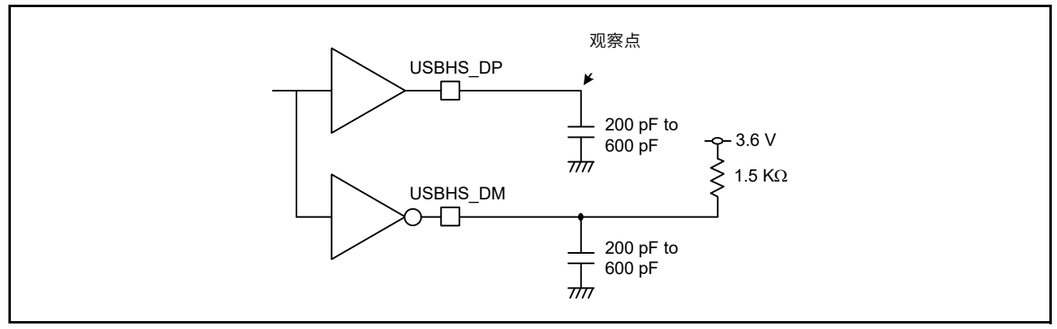


Figure 60.84 低速模式下的测试电路

Table 60.35 USBHS全速特性（USBHS_DP和USBHS_DM引脚特性）
Conditions: USBHS_RREF = 2.2 kΩ ± 1%, USBMCLK = 12/20/24 MHz, UCLK = 48 MHz

Parameter		Symbol	Min	Typ	Max	Unit	测试条件	
输入特性	输入高压	V_{IH}	2.0	-	-	V	-	-
	输入低电压	V_{IL}	-	-	0.8	V	-	-
	差分输入灵敏度	V_{DI}	0.2	-	-	V	| USBHS_DP - USBHS_DM |	-
	差分共模范围	V_{CM}	0.8	-	2.5	V	-	-
输出特性	输出高压	V_{OH}	2.8	-	3.6	V	I_{OH} = -200 µA	-
	输出低电压	V_{OL}	0.0	-	0.3	V	我OL=2毫安	-
	Cross-over voltage	V_{CRS}	1.3	-	2.0	V	-	Figure 60.85, Figure 60.86
	上升时间	t_{LR}	4	-	20	ns	-	
	秋季时间	t_{LF}	4	-	20	ns	-	
	上升下降时间比	t_{LR} / t_{LF}	90	-	111.11	%	t_{FR} / t_{FF}	-
	输出电阻	Z_{DRV}	40.5	-	49.5	Ω	Rs未使用（PHYSET.REPSEL[1:0]=01b和PHYSET.HSEB=0）	
DC characteristics	USBHS_DM pull-up resistor (device)	R_{pu}	0.900	-	1.575	kΩ	空闲状态期间	
			1.425	-	3.090	kΩ	在发送和接收期间	
	USBHS_DP/USBHS_DM pull-down resistor (host)	R_{pd}	14.25	-	24.80	kΩ	-	

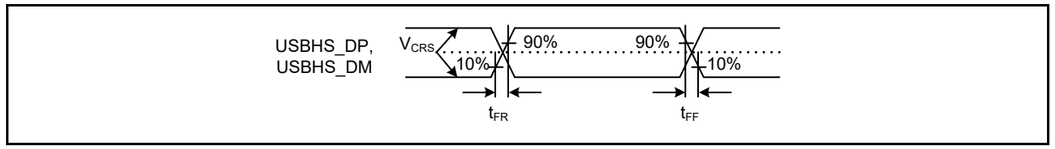


Figure 60.85 USBHS_DP and USBHS_DM output timing in full-speed mode

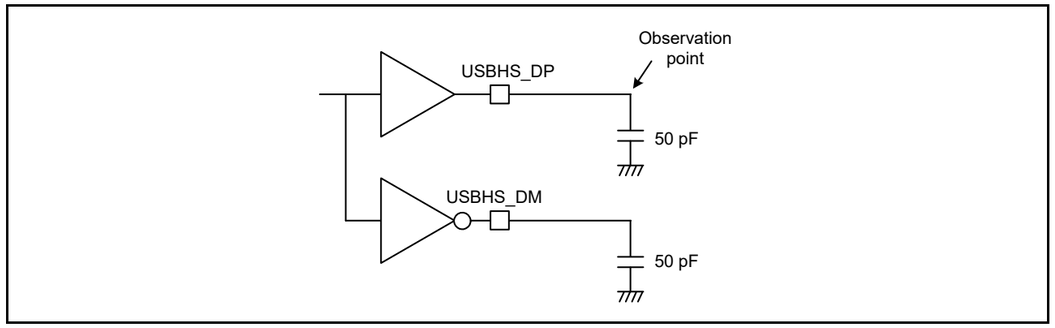


Figure 60.86 Test circuit in full-speed mode

Table 60.36 USBHS high-speed characteristics (USBHS_DP and USBHS_DM pin characteristics)
Conditions: USBHS_RREF = 2.2 kΩ ± 1%, USBMCLK = 12/20/24 MHz

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Input characteristics	Squelch detect sensitivity	V_{HSSQ}	100	-	150	mV	Figure 60.87
	Disconnect detect sensitivity	V_{HSDSC}	525	-	625	mV	Figure 60.88
	Common-mode voltage	V_{HSCM}	-50	-	500	mV	-
Output characteristics	Idle state	V_{HSOI}	-10.0	-	10	mV	-
	Output high voltage	V_{HSOH}	360	-	440	mV	
	Output low voltage	V_{HSOL}	-10.0	-	10	mV	
	Chirp J output voltage (difference)	V_{CHIRPJ}	700	-	1100	mV	
	Chirp K output voltage (difference)	V_{CHIRPK}	-900	-	-500	mV	
AC characteristics	Rise time	t_{HSR}	500	-	-	ps	Figure 60.89
	Fall time	t_{HSF}	500	-	-	ps	
	Output resistance	Z_{HSDRV}	40.5	-	49.5	Ω	-

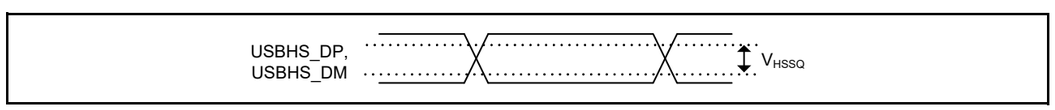


Figure 60.87 USBHS_DP and USBHS_DM squelch detect sensitivity in high-speed mode

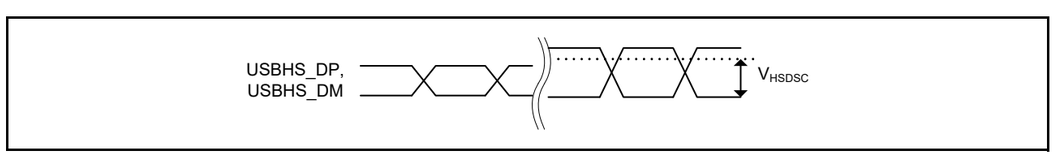


Figure 60.88 USBHS_DP and USBHS_DM disconnect detect sensitivity in high-speed mode

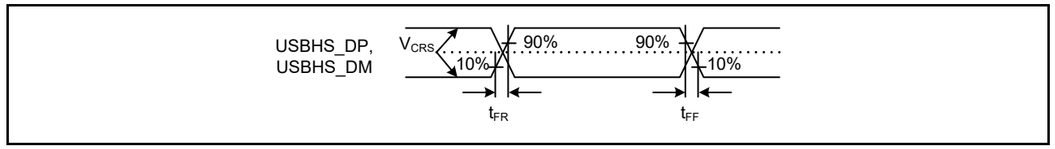


Figure 60.85 全速模式下的USBHS_DP和USBHS_DM输出时序

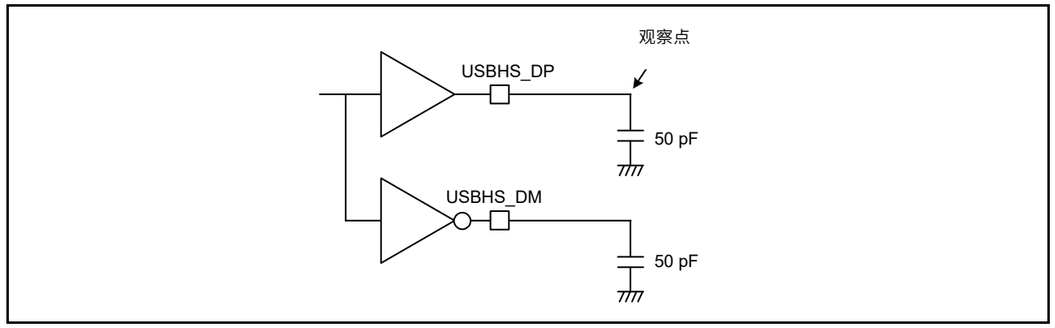


Figure 60.86 全速模式下的测试电路

Table 60.36 USBHS高速特性（USBHS_DP和USBHS_DM引脚特性）
Conditions: USBHS_RREF = 2.2 kΩ ± 1%, USBMCLK = 12/20/24 MHz

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
输入特性	静噪检测灵敏度	V_{HSSQ}	100	-	150	mV	Figure 60.87
	断开检测灵敏度	V_{HSDSC}	525	-	625	mV	Figure 60.88
	Common-mode voltage	V_{HSCM}	-50	-	500	mV	-
输出特性	空闲状态	V_{HSOI}	-10.0	-	10	mV	-
	输出高压	V_{HSOH}	360	-	440	mV	
	输出低电压	V_{HSOL}	-10.0	-	10	mV	
	啁啾J输出电压（差值）	V_{CHIRPJ}	700	-	1100	mV	
	啁啾K输出电压（差）	V_{CHIRPK}	-900	-	-500	mV	
交流特性	上升时间	t_{HSR}	500	-	-	ps	Figure 60.89
	秋季时间	t_{HSF}	500	-	-	ps	
	输出电阻	Z_{HSDRV}	40.5	-	49.5	Ω	-

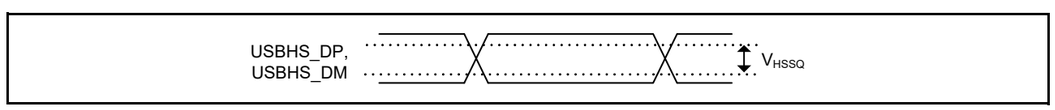


Figure 60.87 USBHS_DP和USBHS_DM静噪检测高速模式下的灵敏度

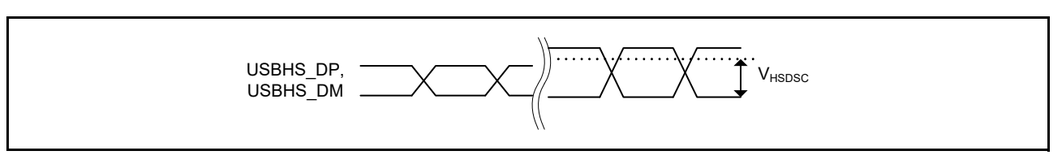


Figure 60.88 USBHS_DP和USBHS_DM断开检测高速模式下的灵敏度

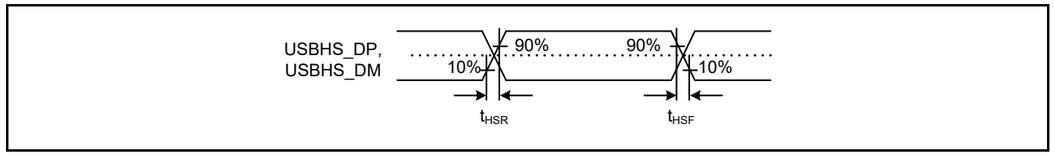


Figure 60.89 USBHS_DP and USBHS_DM output timing in high-speed mode

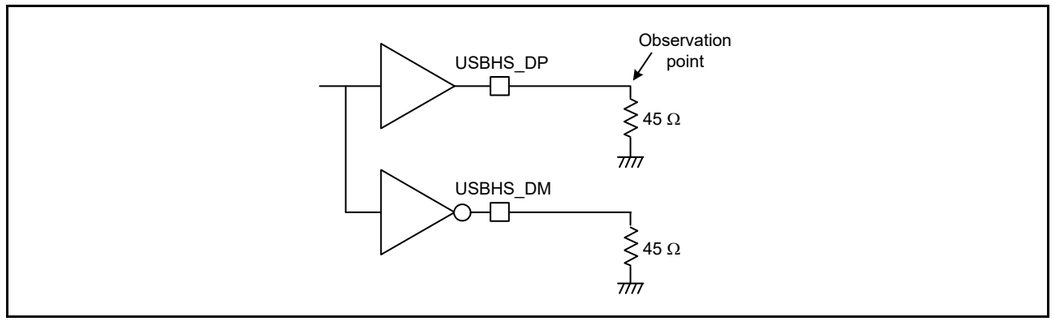


Figure 60.90 Test circuit in high-speed mode

Table 60.37 USBHS high-speed characteristics (USBHS_DP and USBHS_DM pin characteristics)
Conditions: USBHS_RREF = 2.2 kΩ ± 1%, USBMCLK = 12/20/24 MHz

Parameter		Symbol	Min	Max	Unit	Test conditions
Battery Charging Specification	D+ sink current	I_{DP_SINK}	25	175	μA	-
	D- sink current	I_{DM_SINK}	25	175	μA	-
	DCD source current	I_{DP_SRC}	7	13	μA	-
	Data detection voltage	V_{DAT_REF}	0.25	0.4	V	-
	D+ source voltage	V_{DP_SRC}	0.5	0.7	V	Output current = 250 μA
	D- source voltage	V_{DM_SRC}	0.5	0.7	V	Output current = 250 μA

60.4.2 USBFS Timing

Table 60.38 USBFS low-speed characteristics for host only (USB_DP and USB_DM pin characteristics) (1 of 2)
Conditions: VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6V, 2.7 ≤ VREFH0/VREFH ≤ AVCC0, VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V, UCLK = 48 MHz

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Input characteristics	Input high voltage	V_{IH}	2.0	-	-	V	-
	Input low voltage	V_{IL}	-	-	0.8	V	-
	Differential input sensitivity	V_{DI}	0.2	-	-	V	| USB_DP - USB_DM |
	Differential common-mode range	V_{CM}	0.8	-	2.5	V	-
Output characteristics	Output high voltage	V_{OH}	2.8	-	3.6	V	I_{OH} = -200 μA
	Output low voltage	V_{OL}	0.0	-	0.3	V	I_{OL} = 2 mA
	Cross-over voltage	V_{CRS}	1.3	-	2.0	V	Figure 60.91
	Rise time	t_{LR}	75	-	300	ns	
	Fall time	t_{LF}	75	-	300	ns	
	Rise/fall time ratio	t_{LR} / t_{LF}	80	-	125	%	t_{LR}/ t_{LF}

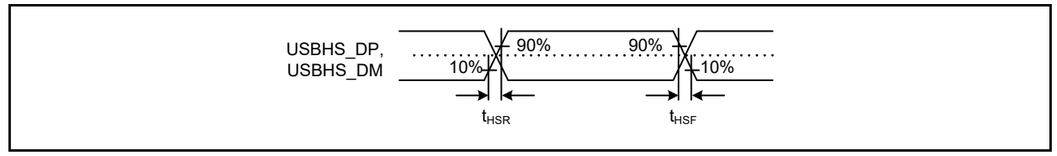


Figure 60.89 高速模式下的USBHS_DP和USBHS_DM输出时序

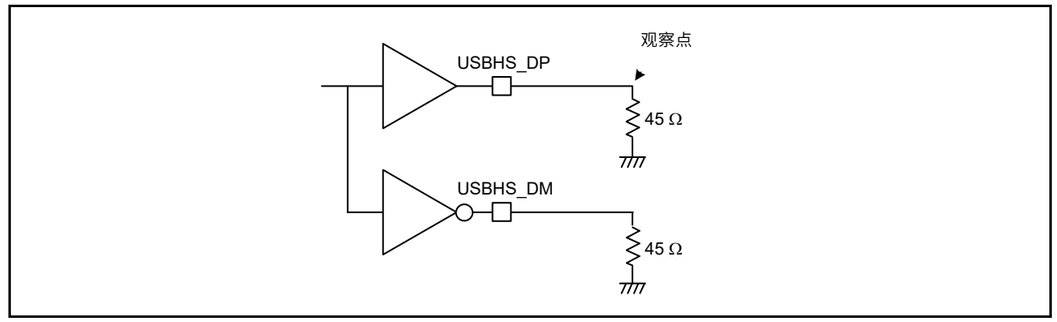


Figure 60.90 高速模式下的测试电路

Table 60.37 USBHS高速特性（USBHS_DP和USBHS_DM引脚特性）
Conditions: USBHS_RREF = 2.2 kΩ ± 1%, USBMCLK = 12/20/24 MHz

Parameter		Symbol	Min	Max	Unit	测试条件
电池充电 Specification	D+灌电流	I_{DP_SINK}	25	175	μA	-
	D- sink current	I_{DM_SINK}	25	175	μA	-
	DCD源电流	I_{DP_SRC}	7	13	μA	-
	数据检测电压	V_{DAT_REF}	0.25	0.4	V	-
	D+源电压	V_{DP_SRC}	0.5	0.7	V	输出电流=250μA
	D- source voltage	V_{DM_SRC}	0.5	0.7	V	输出电流=250μA

60.4.2 USBFS Timing

Table 60.38 仅主机的USBFS低速特性（USB_DP和USB_DM引脚特性）（1of2）
Conditions: VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6V, 2.7 ≤ VREFH0/VREFH ≤ AVCC0, VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V, UCLK = 48 MHz

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
输入特性	输入高压	V_{IH}	2.0	-	-	V	-
	输入低电压	V_{IL}	-	-	0.8	V	-
	差分输入灵敏度	V_{DI}	0.2	-	-	V	| USB_DP - USB_DM |
	差分共模范围	V_{CM}	0.8	-	2.5	V	-
输出特性	输出高压	V_{OH}	2.8	-	3.6	V	I_{OH} = -200 μA
	输出低电压	V_{OL}	0.0	-	0.3	V	我OL=2毫安
	Cross-over voltage	V_{CRS}	1.3	-	2.0	V	Figure 60.91
	上升时间	t_{LR}	75	-	300	ns	
	秋季时间	t_{LF}	75	-	300	ns	
	上升下降时间比	t_{LR} / t_{LF}	80	-	125	%	t_{LR}/ t_{LF}

Table 60.38 USBFS low-speed characteristics for host only (USB_DP and USB_DM pin characteristics) (2 of 2)
Conditions: VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6V, 2.7 ≤ VREFH0/VREFH ≤ AVCC0, VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V, UCLK = 48 MHz

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Pull-up and pull-down characteristics	USB_DP and USB_DM pull-down resistance in host controller mode	R_{pd}	14.25	-	24.80	kΩ	-

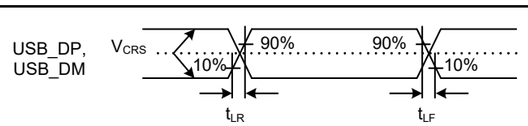


Figure 60.91 USB_DP and USB_DM output timing in low-speed mode

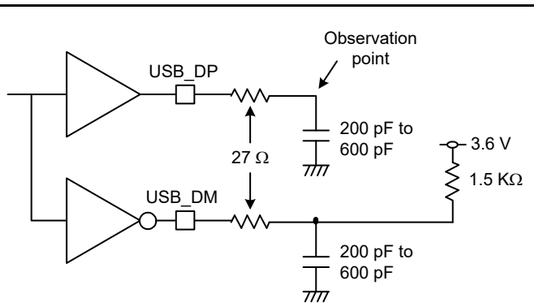


Figure 60.92 Test circuit in low-speed mode

Table 60.39 USBFS full-speed characteristics (USB_DP and USB_DM pin characteristics)
Conditions: VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6 V, 2.7 ≤ VREFH0/VREFH ≤ AVCC0, VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V, UCLK = 48 MHz

Parameter		Symbol	Min	Typ	Max	Unit	Test conditions
Input characteristics	Input high voltage	V_{IH}	2.0	-	-	V	-
	Input low voltage	V_{IL}	-	-	0.8	V	-
	Differential input sensitivity	V_{DI}	0.2	-	-	V	| USB_DP - USB_DM |
	Differential common-mode range	V_{CM}	0.8	-	2.5	V	-
Output characteristics	Output high voltage	V_{OH}	2.8	-	3.6	V	I_{OH} = -200 µA
	Output low voltage	V_{OL}	0.0	-	0.3	V	I_{OL}= 2 mA
	Cross-over voltage	V_{CRS}	1.3	-	2.0	V	Figure 60.93
	Rise time	t_{LR}	4	-	20	ns	
	Fall time	t_{LF}	4	-	20	ns	
	Rise/fall time ratio	t_{LR} / t_{LF}	90	-	111.11	%	t_{FR}/ t_{FF}
	Output resistance	Z_{DRV}	28	-	44	Ω	USBFS: Rs = 27 Ω included
Pull-up and pull-down characteristics	DM pull-up resistance in device controller mode	R_{pu}	0.900	-	1.575	kΩ	During idle state
			1.425	-	3.090	kΩ	During transmission and reception
	USB_DP and USB_DM pull-down resistance in host controller mode	R_{pd}	14.25	-	24.80	kΩ	-

Table 60.38 仅主机的USBFS低速特性（USB_DP和USB_DM引脚特性）（2之2）
Conditions: VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6V, 2.7 ≤ VREFH0/VREFH ≤ AVCC0, VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V, UCLK = 48 MHz

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
上拉和下拉特性	主机控制器模式下的USB_DP和USB_DM下拉电阻	R_{pd}	14.25	-	24.80	kΩ	-

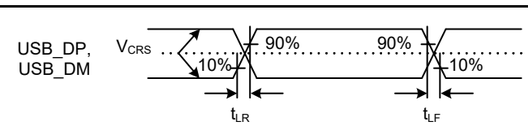


Figure 60.91 低速模式下的USB_DP和USB_DM输出时序

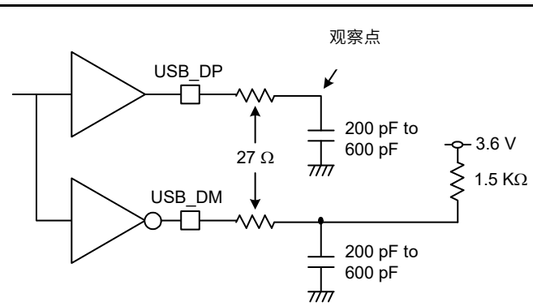


Figure 60.92 低速模式下的测试电路

Table 60.39 USBFS全速特性（USB_DP和USB_DM引脚特性）
Conditions: VCC = AVCC0 = VCC_USB = VBATT = 3.0 to 3.6 V, 2.7 ≤ VREFH0/VREFH ≤ AVCC0, VCC_USBHS = AVCC_USBHS = 3.0 to 3.6 V, UCLK = 48 MHz

Parameter		Symbol	Min	Typ	Max	Unit	测试条件
输入特性	输入高压	V_{IH}	2.0	-	-	V	-
	输入低电压	V_{IL}	-	-	0.8	V	-
	差分输入灵敏度	V_{DI}	0.2	-	-	V	| USB_DP - USB_DM |
	差分共模范围	V_{CM}	0.8	-	2.5	V	-
输出特性	输出高压	V_{OH}	2.8	-	3.6	V	I_{OH} = -200 µA
	输出低电压	V_{OL}	0.0	-	0.3	V	我OL=2毫安
	Cross-over voltage	V_{CRS}	1.3	-	2.0	V	Figure 60.93
	上升时间	t_{LR}	4	-	20	ns	
	秋季时间	t_{LF}	4	-	20	ns	
	上升下降时间比	t_{LR} / t_{LF}	90	-	111.11	%	t_{FR}/ t_{FF}
	输出电阻	Z_{DRV}	28	-	44	Ω	USBFS: Rs = 27 Ω included
上拉和下拉特性	设备控制器模式下的DM上拉电阻	R_{pu}	0.900	-	1.575	kΩ	空闲状态期间
			1.425	-	3.090	kΩ	在发送和接收期间
	主机控制器模式下的USB_DP和USB_DM下拉电阻	R_{pd}	14.25	-	24.80	kΩ	-

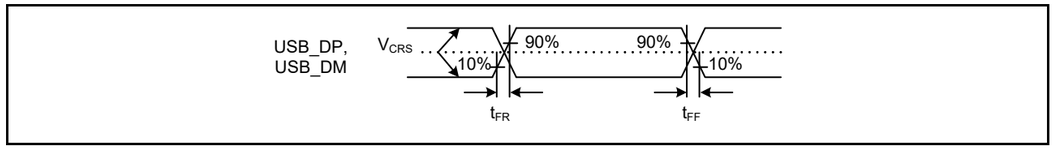


Figure 60.93 USB_DP and USB_DM output timing in full-speed mode

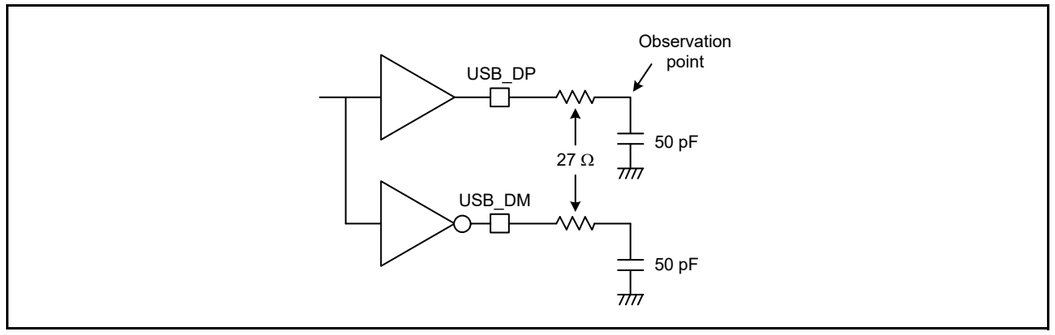


Figure 60.94 Test circuit in full-speed mode

60.5 ADC12 Characteristics

Table 60.40 A/D conversion characteristics for unit 0 (1 of 2)
Conditions: PCLKC = 1 to 60 MHz

Parameter			Min	Typ	Max	Unit	Test conditions
Frequency			1	-	60	MHz	-
Analog input capacitance			-	-	30	pF	-
Quantization error			-	±0.5	-	LSB	-
Resolution			-	-	12	Bits	-
Channel-dedicated sample-and-hold circuits in use (AN000 to AN002)	Conversion time*1 (operation at PCLKC = 60 MHz)	Permissible signal source impedance Max. = 1 kΩ	1.06 (0.4 + 0.25)*2	-	-	µs	• Sampling of channel-dedicated sample-and-hold circuits in 24 states • Sampling in 15 states
	Offset error		-	±1.5	±3.5	LSB	AN000 to AN002 = 0.25 V
	Full-scale error		-	±1.5	±3.5	LSB	AN000 to AN002 = VREFH0- 0.25 V
	Absolute accuracy		-	±2.5	±5.5	LSB	-
	DNL differential nonlinearity error		-	±1.0	±2.0	LSB	-
	INL integral nonlinearity error		-	±1.5	±3.0	LSB	-
	Holding characteristics of sample-and hold circuits		-	-	20	µs	-
	Dynamic range		0.25	-	VREFH 0 - 0.25	V	-
Channel-dedicated sample-and-hold circuits not in use (AN000 to AN002)	Conversion time*1 (operation at PCLKC = 60 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.48 (0.267)*2	-	-	µs	Sampling in 16 states
	Offset error		-	±1.0	±2.5	LSB	-
	Full-scale error		-	±1.0	±2.5	LSB	-
	Absolute accuracy		-	±2.0	±4.5	LSB	-
	DNL differential nonlinearity error		-	±0.5	±1.5	LSB	-
	INL integral nonlinearity error		-	±1.0	±2.5	LSB	-

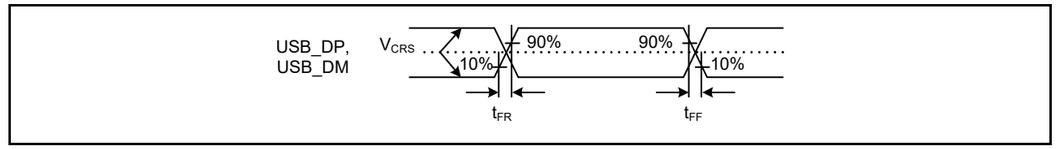


Figure 60.93 全速模式下的USB_DP和USB_DM输出时序

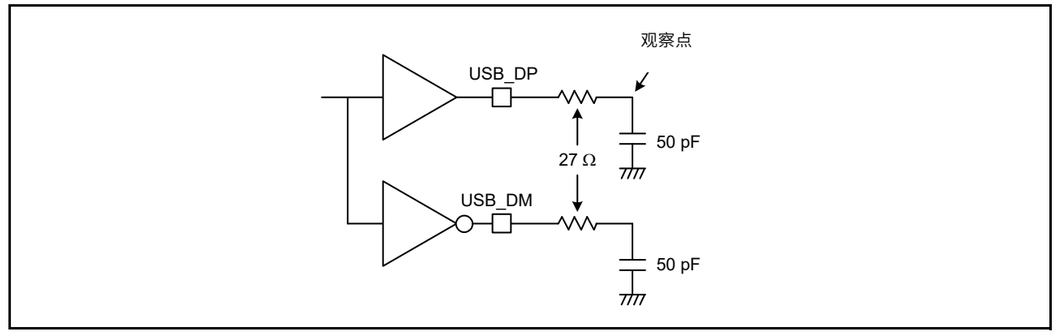


Figure 60.94 全速模式下的测试电路

60.5 ADC12 Characteristics

Table 60.40 单元0(1of2)的AD转换特性
Conditions: PCLKC = 1 to 60 MHz

Parameter			Min	Typ	Max	Unit	测试条件
Frequency			1	-	60	MHz	-
模拟输入电容			-	-	30	pF	-
量化误差			-	±0.5	-	LSB	-
Resolution			-	-	12	Bits	-
使用中的通道专用采样保持电路（AN000至AN002）	转换时间*1（在PCLKC=60MHz下运行）	允许的信号源阻抗Max.=1kΩ	1.06 (0.4 + 0.25)*2	-	-	µs	通道采样 24种状态的专用采样保持电路 15种状态的采样
	偏移误差		-	±1.5	±3.5	LSB	AN000 to AN002 = 0.25 V
	Full-scale error		-	±1.5	±3.5	LSB	AN000 to AN002 = VREFH0- 0.25 V
	绝对精度		-	±2.5	±5.5	LSB	-
	DNL微分非线性误差		-	±1.0	±2.0	LSB	-
	INL积分非线性误差		-	±1.5	±3.0	LSB	-
	采样保持电路的保持特性		-	-	20	µs	-
	动态范围		0.25	-	VREFH 0 - 0.25	V	-
未使用通道专用采样保持电路（AN000至AN002）	转换时间*1（在PCLKC=60MHz下运行）	允许的信号源阻抗Max.=1kΩ	0.48 (0.267)*2	-	-	µs	在16个州进行抽样
	偏移误差		-	±1.0	±2.5	LSB	-
	Full-scale error		-	±1.0	±2.5	LSB	-
	绝对精度		-	±2.0	±4.5	LSB	-
	DNL微分非线性误差		-	±0.5	±1.5	LSB	-
	INL积分非线性误差		-	±1.0	±2.5	LSB	-

Table 60.40 A/D conversion characteristics for unit 0 (2 of 2)
Conditions: PCLKC = 1 to 60 MHz

Parameter			Min	Typ	Max	Unit	Test conditions
High-precision channels (AN003 to AN007)	Conversion time*1 (operation at PCLKC = 60 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.48 (0.267)*2	-	-	µs	Sampling in 16 states
		Max. = 400 Ω	0.40 (0.183)*2	-	-	µs	Sampling in 11 states VCC = AVCC0 = 3.0 to 3.6 V 3.0 V ≤ VREFH0 ≤ AVCC0
	Offset error		-	±1.0	±2.5	LSB	-
	Full-scale error		-	±1.0	±2.5	LSB	-
	Absolute accuracy		-	±2.0	±4.5	LSB	-
	DNL differential nonlinearity error		-	±0.5	±1.5	LSB	-
	INL integral nonlinearity error		-	±1.0	±2.5	LSB	-
Normal-precision channels (AN016 to AN020)	Conversion time*1 (Operation at PCLKC = 60 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.88 (0.667)*2	-	-	µs	Sampling in 40 states
	Offset error		-	±1.0	±5.5	LSB	-
	Full-scale error		-	±1.0	±5.5	LSB	-
	Absolute accuracy		-	±2.0	±7.5	LSB	-
	DNL differential nonlinearity error		-	±0.5	±4.5	LSB	-
	INL integral nonlinearity error		-	±1.0	±5.5	LSB	-

Note: These specification values apply when there is no access to the external bus during A/D conversion. If access occurs during A/D conversion, values might not fall within the indicated ranges.
The use of ports 0 as digital outputs is not allowed when the 12-Bit A/D converter is used.
The characteristics apply when AVCC0, AVSS0, VREFH0, VREFH, VREFL0, VREFL, and 12-bit A/D converter input voltage is stable.
Note 1. The conversion time includes the sampling and comparison times. The number of sampling states is indicated for the test conditions.
Note 2. Values in parentheses indicate the sampling time.

Table 60.41 A/D conversion characteristics for unit 1 (1 of 2)
Conditions: PCLKC = 1 to 60 MHz

Parameter			Min	Typ	Max	Unit	Test conditions
Frequency			1	-	60	MHz	-
Analog input capacitance			-	-	30	pF	-
Quantization error			-	±0.5	-	LSB	-
Resolution			-	-	12	Bits	-
Channel-dedicated sample-and-hold circuits in use (AN100 to AN102)	Conversion time*1 (operation at PCLKC = 60 MHz)	Permissible signal source impedance Max. = 1 kΩ	1.06 (0.4 + 0.25)*2	-	-	µs	• Sampling of channel-dedicated sample-and-hold circuits in 24 states • Sampling in 15 states
	Offset error		-	±1.5	±3.5	LSB	AN100 to AN102 = 0.25 V
	Full-scale error		-	±1.5	±3.5	LSB	AN100 to AN102 = VREFH - 0.25 V
	Absolute accuracy		-	±2.5	±5.5	LSB	-
	DNL differential nonlinearity error		-	±1.0	±2.0	LSB	-
	INL integral nonlinearity error		-	±1.5	±3.0	LSB	-
	Holding characteristics of sample-and hold circuits		-	-	20	µs	-
	Dynamic range		0.25	-	VREFH - 0.25	V	-

Table 60.40 单元0(2of2)的AD转换特性
Conditions: PCLKC = 1 to 60 MHz

Parameter			Min	Typ	Max	Unit	测试条件
高精度通道（AN003至AN007）	转换时间*1（在PCLKC=60MHz下运行）	允许的信号源阻抗Max.=1kΩ	0.48 (0.267)*2	-	-	µs	在16个州进行抽样
		Max. = 400 Ω	0.40 (0.183)*2	-	-	µs	在11个州进行抽样 VCC = AVCC0 = 3.0 to 3.6 V 3.0 V ≤ VREFH0 ≤ AVCC0
	偏移误差		-	±1.0	±2.5	LSB	-
	Full-scale error		-	±1.0	±2.5	LSB	-
	绝对精度		-	±2.0	±4.5	LSB	-
	DNL微分非线性误差		-	±0.5	±1.5	LSB	-
	INL积分非线性误差		-	±1.0	±2.5	LSB	-
普通精度通道（AN016至AN020）	转换时间*1（在PCLKC=60MHz下运行）	允许的信号源阻抗Max.=1kΩ	0.88 (0.667)*2	-	-	µs	在40个州进行抽样
	偏移误差		-	±1.0	±5.5	LSB	-
	Full-scale error		-	±1.0	±5.5	LSB	-
	绝对精度		-	±2.0	±7.5	LSB	-
	DNL微分非线性误差		-	±0.5	±4.5	LSB	-
	INL积分非线性误差		-	±1.0	±5.5	LSB	-

Note: 这些规范值适用于在AD转换期间无法访问外部总线的情况。如果访问发生在D转换，值可能不在指定范围内。
使用12位AD转换器时，不允许将端口0用作数字输出。
这些特性适用于AVCC0、AVSS0、VREFH0、VREFH、VREFL0、VREFL和12位AD转换器输入电压稳定时。

Note 1. 转换时间包括采样时间和比较时间。针对测试条件指示采样状态的数量。
Note 2. 括号中的值表示采样时间。

Table 60.41 单元1的AD转换特性（2个中的1个）
Conditions: PCLKC = 1 to 60 MHz

Parameter			Min	Typ	Max	Unit	测试条件
Frequency			1	-	60	MHz	-
模拟输入电容			-	-	30	pF	-
量化误差			-	±0.5	-	LSB	-
Resolution			-	-	12	Bits	-
使用中的通道专用采样保持电路（AN100至AN102）	转换时间*1（在PCLKC=60MHz下运行）	允许的信号源阻抗Max.=1kΩ	1.06 (0.4 + 0.25)*2	-	-	µs	通道采样 24种状态的专用采样保持电路 15种状态的采样
	偏移误差		-	±1.5	±3.5	LSB	AN100 to AN102 = 0.25 V
	Full-scale error		-	±1.5	±3.5	LSB	AN100 to AN102 = VREFH - 0.25 V
	绝对精度		-	±2.5	±5.5	LSB	-
	DNL微分非线性误差		-	±1.0	±2.0	LSB	-
	INL积分非线性误差		-	±1.5	±3.0	LSB	-
	采样保持电路的保持特性		-	-	20	µs	-
	动态范围		0.25	-	VREFH - 0.25	V	-

Table 60.41 A/D conversion characteristics for unit 1 (2 of 2)
Conditions: PCLKC = 1 to 60 MHz

Parameter			Min	Typ	Max	Unit	Test conditions
Channel-dedicated sample-and-hold circuits not in use (AN100 to AN102)	Conversion time*1 (Operation at PCLKC = 60 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.48 (0.267)*2	-	-	µs	Sampling in 16 states
	Offset error		-	±1.0	±2.5	LSB	-
	Full-scale error		-	±1.0	±2.5	LSB	-
	Absolute accuracy		-	±2.0	±4.5	LSB	-
	DNL differential nonlinearity error		-	±0.5	±1.5	LSB	-
	INL integral nonlinearity error		-	±1.0	±2.5	LSB	-
High-precision channels (AN103, AN105 to AN107)	Conversion time*1 (Operation at PCLKC = 60 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.48 (0.267)*2	-	-	µs	Sampling in 16 states
		Max. = 400 Ω	0.40 (0.183)*2	-	-	µs	Sampling in 11 states VCC = AVCC0 = 3.0 to 3.6 V 3.0 V ≤ VREFH ≤ AVCC0
	Offset error		-	±1.0	±2.5	LSB	-
	Full-scale error		-	±1.0	±2.5	LSB	-
	Absolute accuracy		-	±2.0	±4.5	LSB	-
	DNL differential nonlinearity error		-	±0.5	±1.5	LSB	-
	INL integral nonlinearity error		-	±1.0	±2.5	LSB	-
Normal-precision channels (AN116 to AN119)	Conversion time*1 (Operation at PCLKC = 60 MHz)	Permissible signal source impedance Max. = 1 kΩ	0.88 (0.667)*2	-	-	µs	Sampling in 40 states
	Offset error		-	±1.0	±5.5	LSB	-
	Full-scale error		-	±1.0	±5.5	LSB	-
	Absolute accuracy		-	±2.0	±7.5	LSB	-
	DNL differential nonlinearity error		-	±0.5	±4.5	LSB	-
	INL integral nonlinearity error		-	±1.0	±5.5	LSB	-

Note: These specification values apply when there is no access to the external bus during A/D conversion. If access occurs during A/D conversion, values might not fall within the indicated ranges.
The use of ports 0 as digital outputs is not allowed when the 12-Bit A/D converter is used.
The characteristics apply when AVCC0, AVSS0, VREFH0, VREFH, VREFL0, VREFL, and 12-bit A/D converter input voltage is stable.
Note 1. The conversion time includes the sampling and comparison times. The number of sampling states is indicated for the test conditions.
Note 2. Values in parentheses indicate the sampling time.

Table 60.42 A/D conversion characteristics for simultaneous using of channel-dedicated sample-and-hold circuits in unit0 and unit1
Conditions: PCLKC = 30/60 MHz

Parameter		Min	Typ	Max	Test conditions
Channel-dedicated sample-and-hold circuits in use with continious sampling function enabled (AN000 to AN002)	Offset error	-	±1.5	±5.0	• PCLKC = 60 MHz • Sampling in 15 states
	Full-scale error	-	±2.5	±5.0	
	Absolute accuracy	-	±4.0	±8.0	
Channel-dedicated sample-and-hold circuits in use with continious sampling function enabled (AN100 to AN102)	Offset error	-	±1.5	±5.0	
	Full-scale error	-	±2.5	±5.0	
	Absolute accuracy	-	±4.0	±8.0	
Channel-dedicated sample-and-hold circuits in use with continious sampling function enabled (AN000 to AN002)	Offset error	-	±1.5	±3.5	• PCLKC = 30 MHz • Sampling in 7 states
	Full-scale error	-	±1.5	±3.5	
	Absolute accuracy	-	±3.0	±5.5	
Channel-dedicated sample-and-hold circuits in use with continious sampling function enabled (AN100 to AN102)	Offset error	-	±1.5	±3.5	
	Full-scale error	-	±1.5	±3.5	
	Absolute accuracy	-	±3.0	±5.5	

Table 60.41 单元1的AD转换特性（2个中的2个）
Conditions: PCLKC = 1 to 60 MHz

Parameter			Min	Typ	Max	Unit	测试条件
未使用通道专用采样保持电路（AN100至AN102）	转换时间*1（在PCLKC=60MHz下运行）	允许的信号源阻抗 Max.=1kΩ	0.48 (0.267)*2	-	-	µs	在16个州进行抽样
	偏移误差		-	±1.0	±2.5	LSB	-
	Full-scale error		-	±1.0	±2.5	LSB	-
	绝对精度		-	±2.0	±4.5	LSB	-
	DNL微分非线性误差		-	±0.5	±1.5	LSB	-
	INL积分非线性误差		-	±1.0	±2.5	LSB	-
高精度通道（AN103、AN105至AN107）	转换时间*1（在PCLKC=60MHz下运行）	允许的信号源阻抗 Max.=1kΩ	0.48 (0.267)*2	-	-	µs	在16个州进行抽样
		Max. = 400 Ω	0.40 (0.183)*2	-	-	µs	在11个州进行抽样 VCC = AVCC0 = 3.0 to 3.6 V 3.0 V ≤ VREFH ≤ AVCC0
	偏移误差		-	±1.0	±2.5	LSB	-
	Full-scale error		-	±1.0	±2.5	LSB	-
	绝对精度		-	±2.0	±4.5	LSB	-
	DNL微分非线性误差		-	±0.5	±1.5	LSB	-
	INL积分非线性误差		-	±1.0	±2.5	LSB	-
普通精度通道（AN116至AN119）	转换时间*1（在PCLKC=60MHz下运行）	允许的信号源阻抗 Max.=1kΩ	0.88 (0.667)*2	-	-	µs	在40个州进行抽样
	偏移误差		-	±1.0	±5.5	LSB	-
	Full-scale error		-	±1.0	±5.5	LSB	-
	绝对精度		-	±2.0	±7.5	LSB	-
	DNL微分非线性误差		-	±0.5	±4.5	LSB	-
	INL积分非线性误差		-	±1.0	±5.5	LSB	-

Note: 这些规范值适用于在AD转换期间无法访问外部总线的情况。如果访问发生在D转换，值可能不在指定范围内。
使用12位AD转换器时，不允许将端口0用作数字输出。
这些特性适用于AVCC0、AVSS0、VREFH0、VREFH、VREFL0、VREFL和12位AD转换器输入电压稳定时。

Note 1. 转换时间包括采样时间和比较时间。针对测试条件指示采样状态的数量。

Note 2. 括号中的值表示采样时间。

表60.42在unit0和unit1中同时使用通道专用采样保持电路的AD转换特性条件：PCLKC=3060MHz

Parameter		Min	Typ	Max	测试条件
启用连续采样功能的通道专用采样保持电路（AN000至AN002）	偏移误差	-	±1.5	±5.0	PCLKC=60MHz 15种状态采样
	Full-scale error	-	±2.5	±5.0	
	绝对精度	-	±4.0	±8.0	
启用连续采样功能的通道专用采样保持电路（AN100至AN102）	偏移误差	-	±1.5	±5.0	
	Full-scale error	-	±2.5	±5.0	
	绝对精度	-	±4.0	±8.0	
启用连续采样功能的通道专用采样保持电路（AN000至AN002）	偏移误差	-	±1.5	±3.5	PCLKC=30MHz 7种状态采样
	Full-scale error	-	±1.5	±3.5	
	绝对精度	-	±3.0	±5.5	
启用连续采样功能的通道专用采样保持电路（AN100至AN102）	偏移误差	-	±1.5	±3.5	
	Full-scale error	-	±1.5	±3.5	
	绝对精度	-	±3.0	±5.5	

Note: When simultaneously using channel-dedicated sample-and-hold circuits in unit0 and unit1, setting the ADSHMSR.SHMD bit to 1 is recommended.

Table 60.43 A/D internal reference voltage characteristics

Parameter	Min	Typ	Max	Unit	Test conditions
A/D internal reference voltage	1.13	1.18	1.23	V	-
Sampling time	4.15	-	-	µs	-

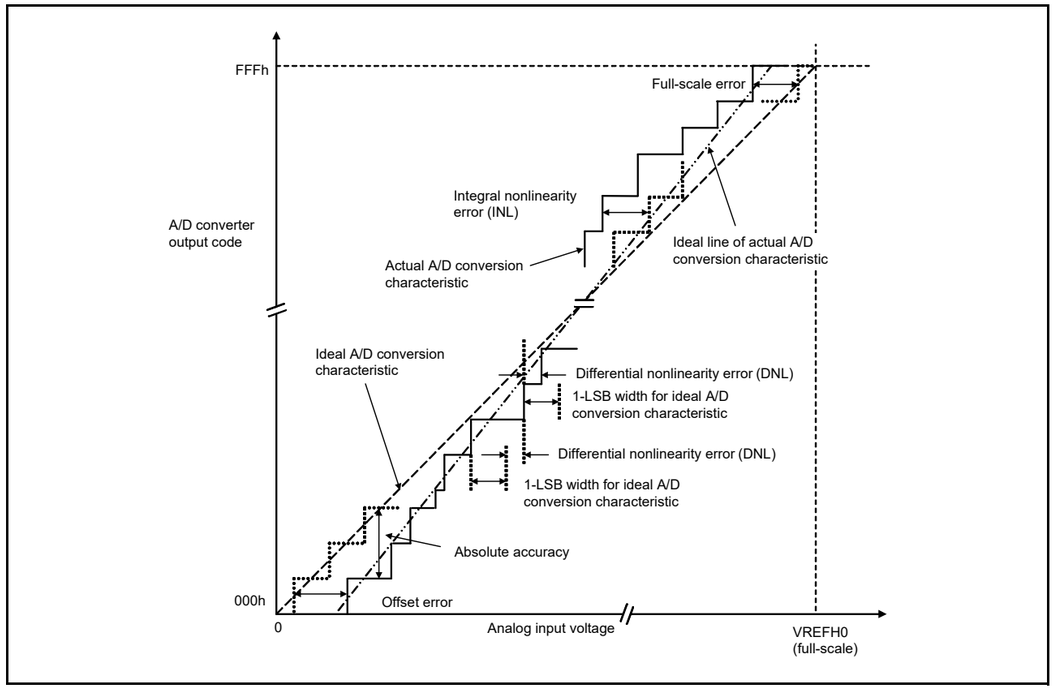


Figure 60.95 Illustration of ADC12 characteristic terms

Absolute accuracy

Absolute accuracy is the difference between output code based on the theoretical A/D conversion characteristics, and the actual A/D conversion result. When measuring absolute accuracy, the voltage at the midpoint of the width of the analog input voltage (1-LSB width), which can meet the expectation of outputting an equal code based on the theoretical A/D conversion characteristics, is used as an analog input voltage. For example, if 12-bit resolution is used and the reference voltage VREFH0 = 3.072 V, then 1-LSB width becomes 0.75 mV, and 0 mV, 0.75 mV, and 1.5 mV are used as the analog input voltages. If the analog input voltage is 6 mV, an absolute accuracy of ±5 LSB means that the actual A/D conversion result is in the range of 003h to 00Dh, though an output code of 008h can be expected from the theoretical A/D conversion characteristics.

Integral nonlinearity error (INL)

Integral nonlinearity error is the maximum deviation between the ideal line when the measured offset and full-scale errors are zeroed, and the actual output code.

Differential nonlinearity error (DNL)

Differential nonlinearity error is the difference between the 1-LSB width based on the ideal A/D conversion characteristics and the width of the actual output code.

Note: 在unit0和unit1中同时使用通道专用采样保持电路时，建议将ADSHMSR.SHMD位设置为1。

Table 60.43 AD内部参考电压特性

Parameter	Min	Typ	Max	Unit	测试条件
AD内部参考电压	1.13	1.18	1.23	V	-
采样时间	4.15	-	-	µs	-

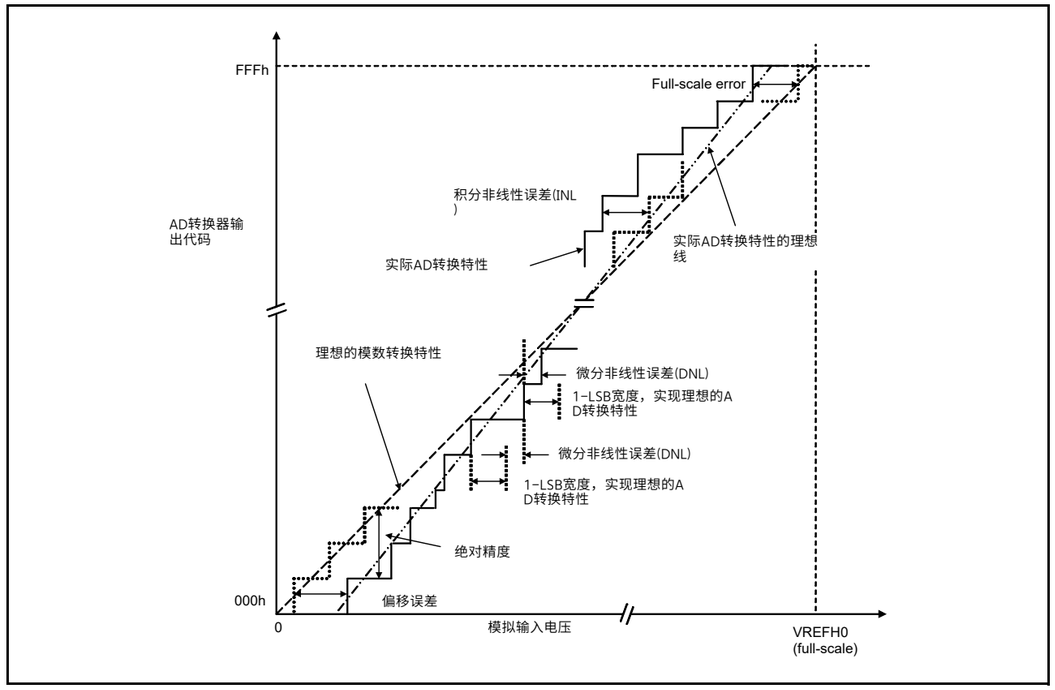


Figure 60.95 ADC12特征项说明

绝对精度

绝对精度是基于理论AD转换特性的输出代码与实际AD转换结果之间的差异。测量绝对精度时，将模拟输入电压宽度（1-LSB宽度）的中点电压作为模拟输入电压，该电压可以满足基于理论模数转换特性输出等码的预期.例如，如果使用12位分辨率并且参考电压VREFH0=3.072V，则1-LSB宽度变为0.75mV，并且使用0mV、0.75mV和1.5mV作为模拟输入电压。如果模拟输入电压为6mV，±5LSB的绝对精度意味着实际的AD转换结果在003h到00Dh的范围内，尽管从理论上的AD转换特性可以预期输出码为008h。

积分非线性误差(INL)

积分非线性误差是测量的偏移和满量程误差为零时的理想线与实际输出代码之间的最大偏差。

微分非线性误差(DNL)

微分非线性误差是基于理想AD转换特性的1-LSB宽度与实际输出码的宽度之差。

Offset error

Offset error is the difference between the transition point of the ideal first output code and the actual first output code.

Full-scale error

Full-scale error is the difference between the transition point of the ideal last output code and the actual last output code.

60.6 DAC12 Characteristics

Table 60.44 D/A conversion characteristics

Parameter	Min	Typ	Max	Unit	Test conditions
Resolution	-	-	12	Bits	-
Without output amplifier					
Absolute accuracy	-	-	±24	LSB	Resistive load 2 MΩ
INL	-	±2.0	±8.0	LSB	Resistive load 2 MΩ
DNL	-	±1.0	±2.0	LSB	-
Output impedance	-	8.5	-	kΩ	-
Conversion time	-	-	3.0	µs	Resistive load 2 MΩ, Capacitive load 20 pF
Output voltage range	0	-	VREFH	V	-
With output amplifier					
INL	-	±2.0	±4.0	LSB	-
DNL	-	±1.0	±2.0	LSB	-
Conversion time	-	-	4.0	µs	-
Resistive load	5	-	-	kΩ	-
Capacitive load	-	-	50	pF	-
Output voltage range	0.2	-	VREFH - 0.2	V	-

60.7 TSN Characteristics

Table 60.45 TSN characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Relative accuracy	-	-	±1.0	-	°C	-
Temperature slope	-	-	4.0	-	mV/°C	-
Output voltage (at 25°C)	-	-	1.24	-	V	-
Temperature sensor start time	t_{START}	-	-	30	µs	-
Sampling time	-	4.15	-	-	µs	-

60.8 OSC Stop Detect Characteristics

Table 60.46 Oscillation stop detection circuit characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Detection time	t_{dr}	-	-	1	ms	Figure 60.96

偏移误差

偏移误差是理想的第一个输出代码的转换点与实际的第一个输出代码之间的差异。

Full-scale error

满量程误差是理想的最后输出代码的转换点与实际的最后输出代码之间的差异。

60.6 DAC12 Characteristics

Table 60.44 DA转换特性

Parameter	Min	Typ	Max	Unit	测试条件
Resolution	-	-	12	Bits	-
无输出放大器					
绝对精度	-	-	±24	LSB	阻性负载2MΩ
INL	-	±2.0	±8.0	LSB	阻性负载2MΩ
DNL	-	±1.0	±2.0	LSB	-
输出阻抗	-	8.5	-	kΩ	-
转换时间	-	-	3.0	µs	电阻负载2MΩ，电容负载20pF
输出电压范围	0	-	VREFH	V	-
带输出放大器					
INL	-	±2.0	±4.0	LSB	-
DNL	-	±1.0	±2.0	LSB	-
转换时间	-	-	4.0	µs	-
阻性负载	5	-	-	kΩ	-
Capacitive load	-	-	50	pF	-
输出电压范围	0.2	-	VREFH - 0.2	V	-

60.7 TSN Characteristics

Table 60.45 TSN characteristics

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
相对精度	-	-	±1.0	-	°C	-
温度斜率	-	-	4.0	-	mV/°C	-
输出电压（25°C时）	-	-	1.24	-	V	-
温度传感器启动时间	t_{START}	-	-	30	µs	-
采样时间	-	4.15	-	-	µs	-

60.8 OSC停止检测特性

Table 60.46 振荡停止检测电路特性

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
检测时间	t_{dr}	-	-	1	ms	Figure 60.96

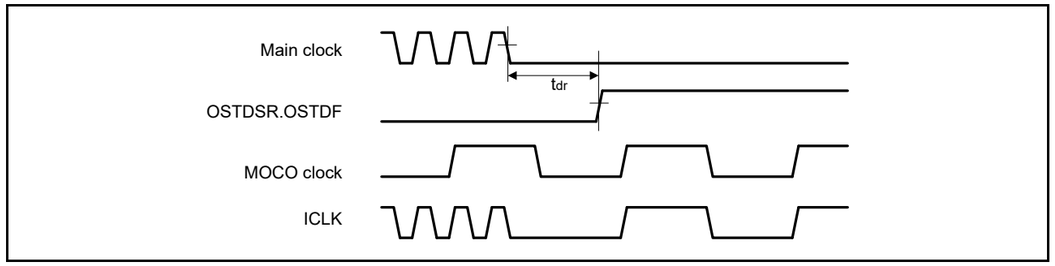


Figure 60.96 Oscillation stop detection timing

60.9 POR and LVD Characteristics

Table 60.47 Power-on reset circuit and voltage detection circuit characteristics

Parameter			Symbol	Min	Typ	Max	Unit	Test conditions
Voltage detection level	Power-on reset (POR)	DPSBYCR.DEEPCUT[1:0] = 00b or 01b	V_{POR}	2.5	2.6	2.7	V	Figure 60.97
		DPSBYCR.DEEPCUT[1:0] = 11b		1.8	2.25	2.7		
	Voltage detection circuit (LVD0)		V_{det0_1}	2.84	2.94	3.04		Figure 60.98
			V_{det0_2}	2.77	2.87	2.97		
			V_{det0_3}	2.70	2.80	2.90		
	Voltage detection circuit (LVD1)		V_{det1_1}	2.89	2.99	3.09		Figure 60.99
			V_{det1_2}	2.82	2.92	3.02		
			V_{det1_3}	2.75	2.85	2.95		
	Voltage detection circuit (LVD2)		V_{det2_1}	2.89	2.99	3.09		Figure 60.100
			V_{det2_2}	2.82	2.92	3.02		
			V_{det2_3}	2.75	2.85	2.95		
Internal reset time	Power-on reset time		t_{POR}	-	4.5	-	ms	Figure 60.97
	LVD0 reset time		t_{LVD0}	-	0.51	-		Figure 60.98
	LVD1 reset time		t_{LVD1}	-	0.38	-		Figure 60.99
	LVD2 reset time		t_{LVD2}	-	0.38	-		Figure 60.100
Minimum VCC down time*1			t_{VOFF}	200	-	-	µs	Figure 60.97, Figure 60.98
Response delay			t_{det}	-	-	200	µs	Figure 60.97 to Figure 60.100
LVD operation stabilization time (after LVD is enabled)			$t_{d(E-A)}$	-	-	10	µs	Figure 60.99, Figure 60.100
Hysteresis width (LVD1 and LVD2)			V_{LVH}	-	70	-	mV	

Note 1. The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR}, V_{det1}, and V_{det2} for POR and LVD.

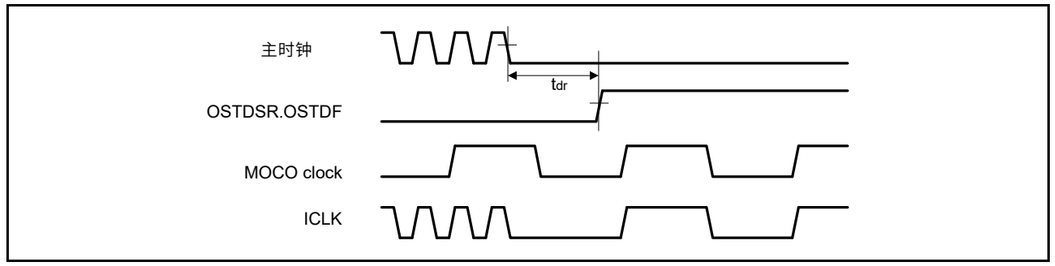


Figure 60.96 振荡停止检测时机

60.9 POR和LVD特性

Table 60.47 上电复位电路及电压检测电路特性

Parameter			Symbol	Min	Typ	Max	Unit	测试条件
电压检测电平	Power-on reset (POR)	DPSBYCR.DEEPCUT[1:0] = 00b or 01b	V_{POR}	2.5	2.6	2.7	V	Figure 60.97
		DPSBYCR.DEEPCUT[1:0] = 11b		1.8	2.25	2.7		
	电压检测电路（LVD0）		V_{det0_1}	2.84	2.94	3.04		Figure 60.98
			V_{det0_2}	2.77	2.87	2.97		
			V_{det0_3}	2.70	2.80	2.90		
	电压检测电路（LVD1）		V_{det1_1}	2.89	2.99	3.09		Figure 60.99
			V_{det1_2}	2.82	2.92	3.02		
			V_{det1_3}	2.75	2.85	2.95		
	电压检测电路（LVD2）		V_{det2_1}	2.89	2.99	3.09		Figure 60.100
			V_{det2_2}	2.82	2.92	3.02		
			V_{det2_3}	2.75	2.85	2.95		
内部复位时间	上电复位时间		t_{POR}	-	4.5	-	ms	Figure 60.97
	LVD0复位时间		t_{LVD0}	-	0.51	-		Figure 60.98
	LVD1复位时间		t_{LVD1}	-	0.38	-		Figure 60.99
	LVD2复位时间		t_{LVD2}	-	0.38	-		Figure 60.100
最短VCC停机时间*1			t_{VOFF}	200	-	-	µs	Figure 60.97, Figure 60.98
响应延迟			t_{det}	-	-	200	µs	图60.97至 Figure 60.100
LVD操作稳定时间（启用LVD后）			$t_{d(E-A)}$	-	-	10	µs	Figure 60.99, Figure 60.100
迟滞宽度（LVD1和LVD2）			V_{LVH}	-	70	-	mV	

Note 1. 最小VCC停机时间表示VCC低于电压检测电平VPOR的最小值的时间，Vdet1和Vdet2用于POR和LVD。

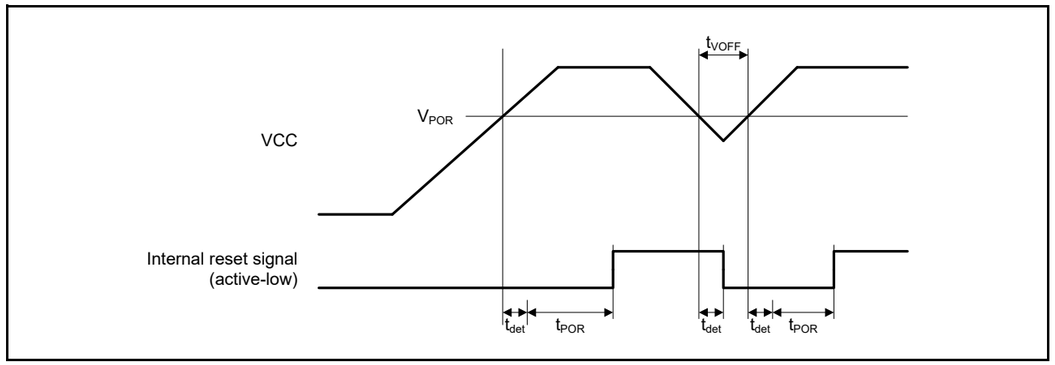


Figure 60.97 Power-on reset timing

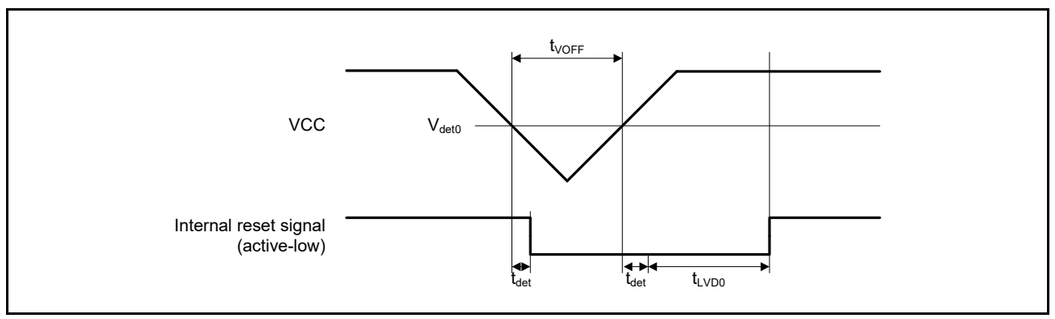


Figure 60.98 Voltage detection circuit timing (V_{det0})

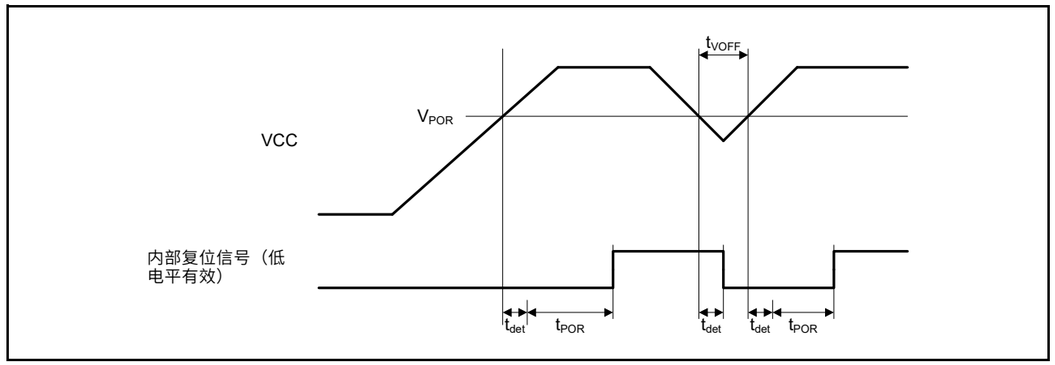


Figure 60.97 上电复位时序

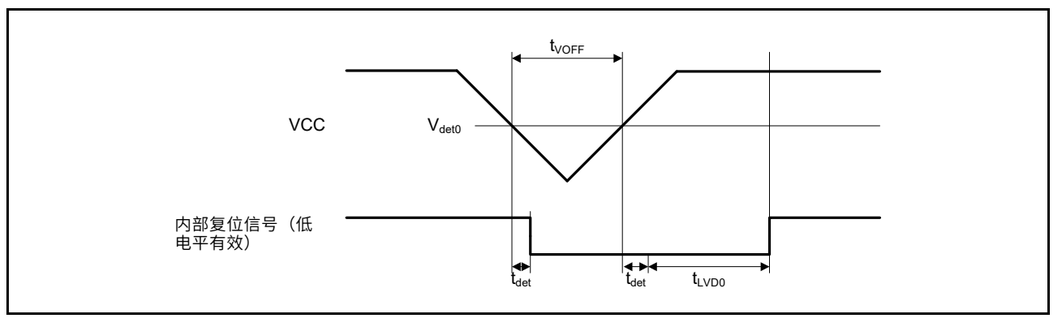


Figure 60.98 电压检测电路时序（Vdet0）

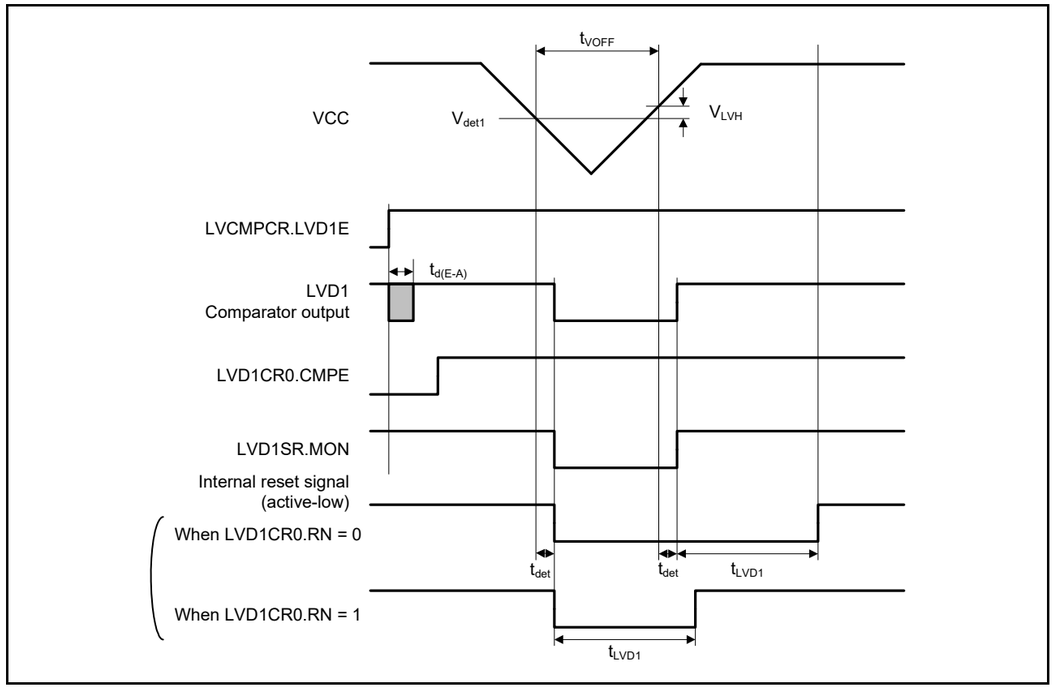


Figure 60.99 Voltage detection circuit timing (V_{det1})

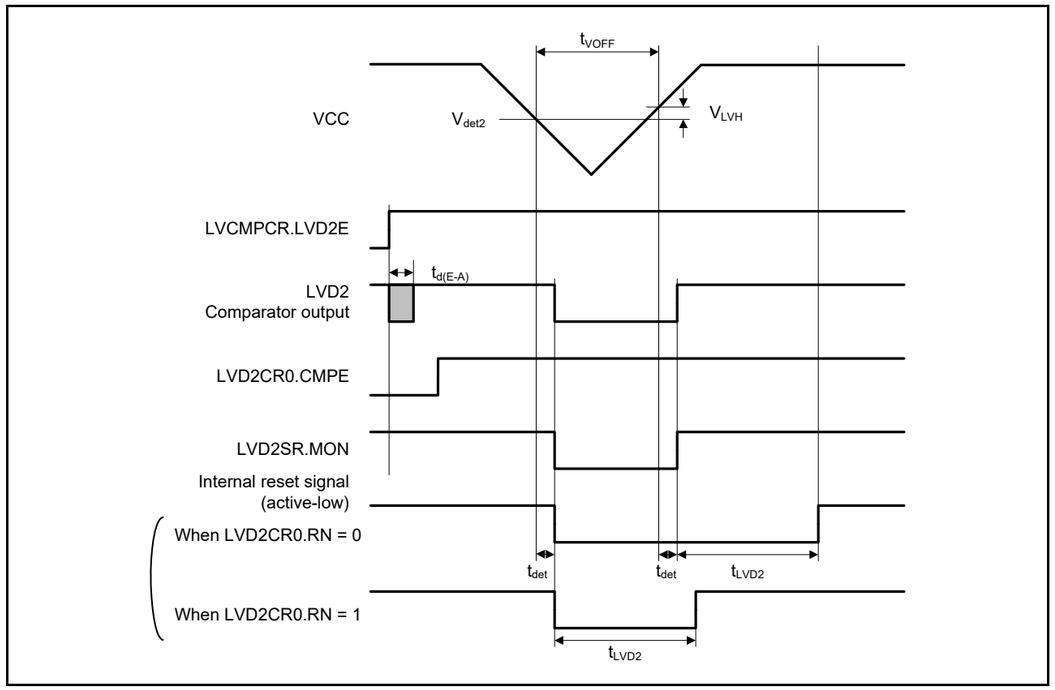


Figure 60.100 Voltage detection circuit timing (V_{det2})

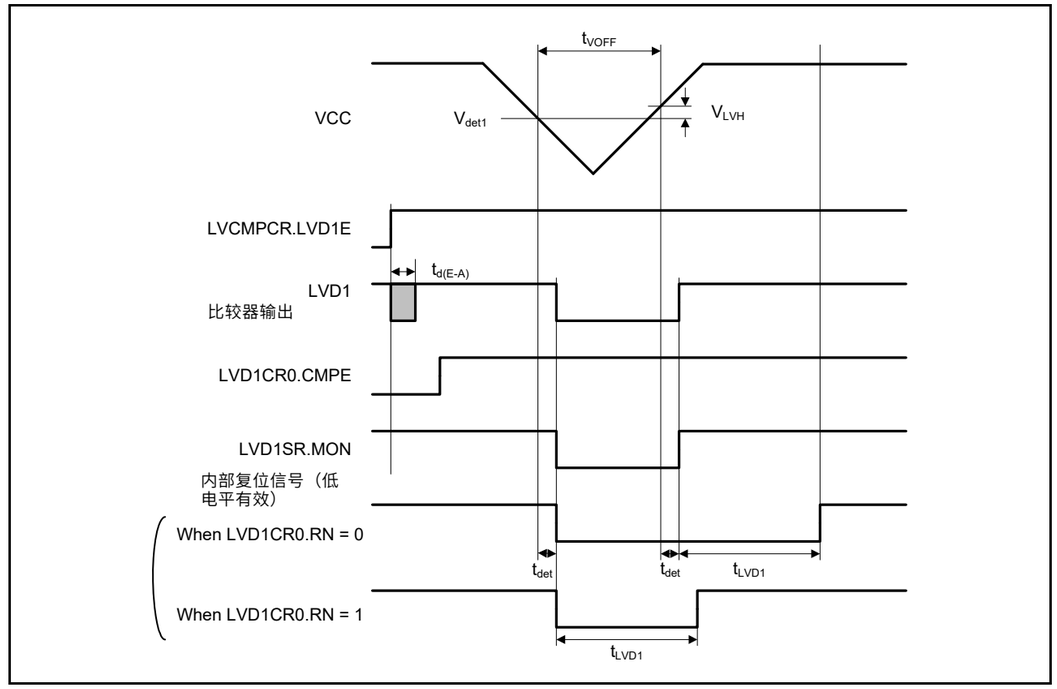


Figure 60.99 电压检测电路时序（Vdet1）

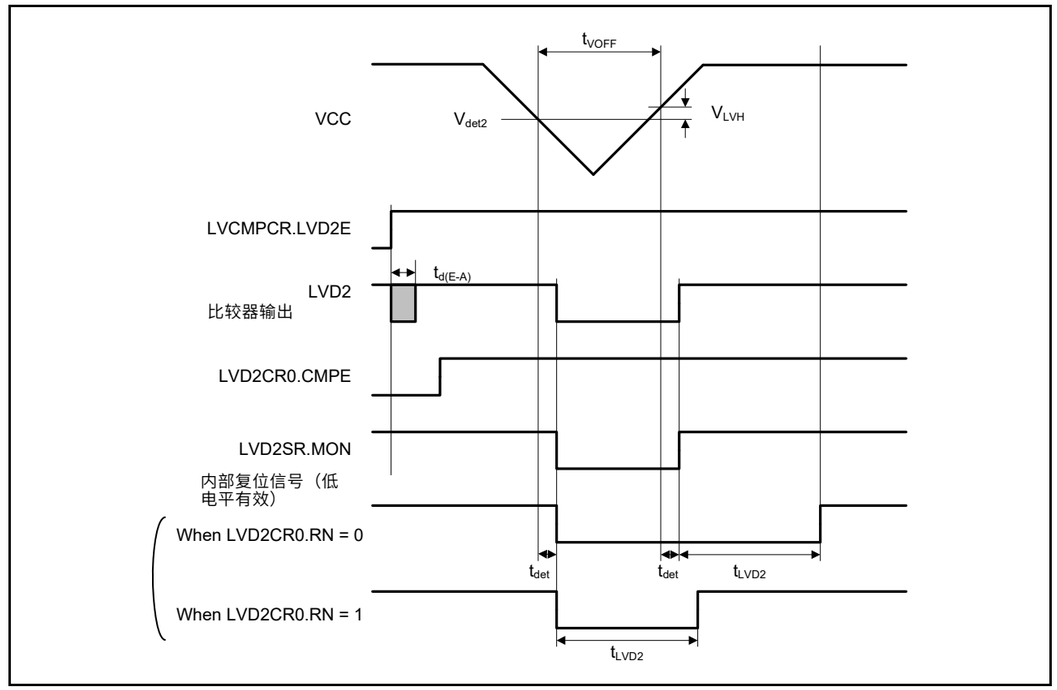


Figure 60.100 电压检测电路时序（Vdet2）

60.10 VBATT Characteristics

Table 60.48 Battery backup function characteristics
Conditions: VCC = AVCC0 = VCC_USB = 2.7 to 3.6 V, 2.7 ≤ VREFH0/VREFH ≤ AVCC0, VBATT = 1.8 to 3.6 V

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Voltage level for switching to battery backup	$V_{DETBATT}$	2.50	2.60	2.70	V	Figure 60.101
Lower-limit VBATT voltage for power supply switching caused by VCC voltage drop	V_{BATTSW}	2.70	-	-	V	
VCC-off period for starting power supply switching	$t_{VOFFBATT}$	200	-	-	µs	

Note: The VCC-off period for starting power supply switching indicates the period in which VCC is below the minimum value of the voltage level for switching to battery backup ($V_{DETBATT}$).

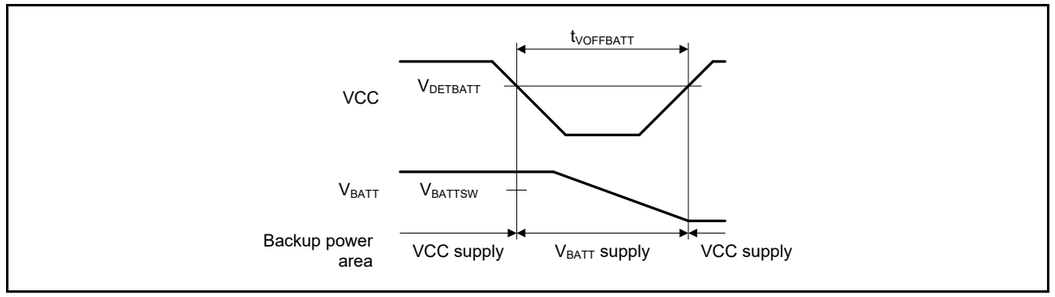


Figure 60.101 Battery backup function characteristics

60.11 CTSU Characteristics

Table 60.49 CTSU characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
External capacitance connected to TSCAP pin	C_{tscap}	9	10	11	nF	-
TS pin capacitive load	C_{base}	-	-	50	pF	-
Permissible output high current	ΣI_{oH}	-	-	-40	mA	When the mutual capacitance method is applied

60.12 ACMPHS Characteristics

Table 60.50 ACMPHS characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
Reference voltage range	VREF	0	-	AVCC0	V	-
Input voltage range	VI	0	-	AVCC0	V	-
Output delay*1	Td	-	50	100	ns	VI = VREF ± 100 mV
Internal reference voltage	Vref	1.13	1.18	1.23	V	-

Note 1. This value is the internal propagation delay.

60.10 VBATT Characteristics

Table 60.48 电池备份功能特点
Conditions: VCC = AVCC0 = VCC_USB = 2.7 to 3.6 V, 2.7 ≤ VREFH0/VREFH ≤ AVCC0, VBATT = 1.8 to 3.6 V

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
切换到备用电池的电压电平	$V_{DETBATT}$	2.50	2.60	2.70	V	Figure 60.101
VCC压降引起的电源切换下限VBATT电压	V_{BATTSW}	2.70	-	-	V	
启动电源切换的VCC-off周期	$t_{VOFFBATT}$	200	-	-	µs	

Note: 开始电源切换的VCC-off周期表示VCC低于切换到备用电池的电压电平最小值(VDETBATT)的周期。

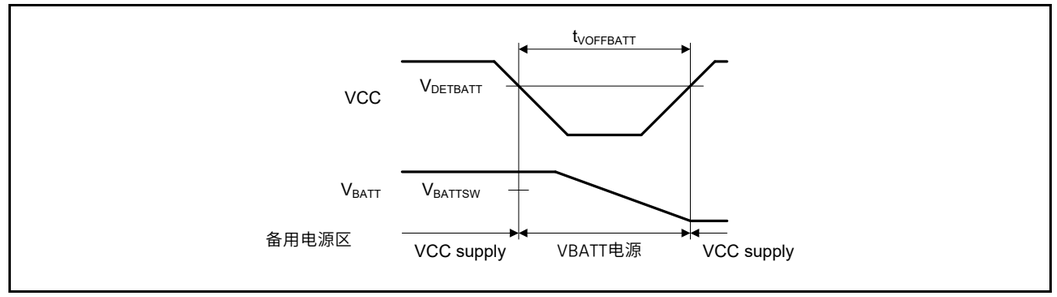


Figure 60.101 电池备份功能特点

60.11 CTSU Characteristics

Table 60.49 CTSU characteristics

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
连接到TSCAP引脚的外部电容	C_{tscap}	9	10	11	nF	-
TS引脚容性负载	C_{base}	-	-	50	pF	-
允许输出大电流	ΣI_{oH}	-	-	-40	mA	应用互电容法时

60.12 ACMPHS Characteristics

Table 60.50 ACMPHS characteristics

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
参考电压范围	VREF	0	-	AVCC0	V	-
输入电压范围	VI	0	-	AVCC0	V	-
Output delay*1	Td	-	50	100	ns	VI = VREF ± 100 mV
内部参考电压	Vref	1.13	1.18	1.23	V	-

Note 1. 该值是内部传播延迟。

60.13 PGA Characteristics

Table 60.51 PGA characteristics in single mode

Parameter	Symbol	Min	Typ	Max	Unit
PGAVSS input voltage range	PGAVSS	0	-	0	V
	AIN0 (G = 2.000)	0.050 × AVCC0	-	0.45 × AVCC0	V
	AIN1 (G = 2.500)	0.047 × AVCC0	-	0.360 × AVCC0	V
	AIN2 (G = 2.667)	0.046 × AVCC0	-	0.337 × AVCC0	V
	AIN3 (G = 2.857)	0.046 × AVCC0	-	0.32 × AVCC0	V
	AIN4 (G = 3.077)	0.045 × AVCC0	-	0.292 × AVCC0	V
	AIN5 (G = 3.333)	0.044 × AVCC0	-	0.265 × AVCC0	V
	AIN6 (G = 3.636)	0.042 × AVCC0	-	0.247 × AVCC0	V
	AIN7 (G = 4.000)	0.040 × AVCC0	-	0.212 × AVCC0	V
	AIN8 (G = 4.444)	0.036 × AVCC0	-	0.191 × AVCC0	V
	AIN9 (G = 5.000)	0.033 × AVCC0	-	0.17 × AVCC0	V
	AIN10 (G = 5.714)	0.031 × AVCC0	-	0.148 × AVCC0	V
	AIN11 (G = 6.667)	0.029 × AVCC0	-	0.127 × AVCC0	V
	AIN12 (G = 8.000)	0.027 × AVCC0	-	0.09 × AVCC0	V
	AIN13 (G = 10.000)	0.025 × AVCC0	-	0.08 × AVCC0	V
	AIN14 (G = 13.333)	0.023 × AVCC0	-	0.06 × AVCC0	V
Gain error	Gerr0 (G = 2.000)	-1.0	-	1.0	%
	Gerr1 (G = 2.500)	-1.0	-	1.0	%
	Gerr2 (G = 2.667)	-1.0	-	1.0	%
	Gerr3 (G = 2.857)	-1.0	-	1.0	%
	Gerr4 (G = 3.077)	-1.0	-	1.0	%
	Gerr5 (G = 3.333)	-1.5	-	1.5	%
	Gerr6 (G = 3.636)	-1.5	-	1.5	%
	Gerr7 (G = 4.000)	-1.5	-	1.5	%
	Gerr8 (G = 4.444)	-2.0	-	2.0	%
	Gerr9 (G = 5.000)	-2.0	-	2.0	%
	Gerr10 (G = 5.714)	-2.0	-	2.0	%
	Gerr11 (G = 6.667)	-2.0	-	2.0	%
	Gerr12 (G = 8.000)	-2.0	-	2.0	%
	Gerr13 (G = 10.000)	-2.0	-	2.0	%
	Gerr14 (G = 13.333)	-2.0	-	2.0	%
Offset error	Voff	-8	-	8	mV

Table 60.52 PGA characteristics in differential mode (1 of 2)

Parameter		Symbol	Min	Typ	Max	Unit
PGAVSS input voltage range		PGAVSS	-0.5	-	0.3	V
Differential input voltage range	G = 1.500	AIN-PGAVSS	-0.5	-	0.5	V
	G = 2.333		-0.4	-	0.4	V
	G = 4.000		-0.2	-	0.2	V
	G = 5.667		-0.15	-	0.15	V

60.13 PGA特性

Table 60.51 单模PGA特性

Parameter	Symbol	Min	Typ	Max	Unit
PGAVSS输入电压范围	PGAVSS	0	-	0	V
	AIN0 (G = 2.000)	0.050 × AVCC0	-	0.45 × AVCC0	V
	AIN1 (G = 2.500)	0.047 × AVCC0	-	0.360 × AVCC0	V
	AIN2 (G = 2.667)	0.046 × AVCC0	-	0.337 × AVCC0	V
	AIN3 (G = 2.857)	0.046 × AVCC0	-	0.32 × AVCC0	V
	AIN4 (G = 3.077)	0.045 × AVCC0	-	0.292 × AVCC0	V
	AIN5 (G = 3.333)	0.044 × AVCC0	-	0.265 × AVCC0	V
	AIN6 (G = 3.636)	0.042 × AVCC0	-	0.247 × AVCC0	V
	AIN7 (G = 4.000)	0.040 × AVCC0	-	0.212 × AVCC0	V
	AIN8 (G = 4.444)	0.036 × AVCC0	-	0.191 × AVCC0	V
	AIN9 (G = 5.000)	0.033 × AVCC0	-	0.17 × AVCC0	V
	AIN10 (G = 5.714)	0.031 × AVCC0	-	0.148 × AVCC0	V
	AIN11 (G = 6.667)	0.029 × AVCC0	-	0.127 × AVCC0	V
	AIN12 (G = 8.000)	0.027 × AVCC0	-	0.09 × AVCC0	V
	AIN13 (G = 10.000)	0.025 × AVCC0	-	0.08 × AVCC0	V
	AIN14 (G = 13.333)	0.023 × AVCC0	-	0.06 × AVCC0	V
增益误差	Gerr0 (G = 2.000)	-1.0	-	1.0	%
	Gerr1 (G = 2.500)	-1.0	-	1.0	%
	Gerr2 (G = 2.667)	-1.0	-	1.0	%
	Gerr3 (G = 2.857)	-1.0	-	1.0	%
	Gerr4 (G = 3.077)	-1.0	-	1.0	%
	Gerr5 (G = 3.333)	-1.5	-	1.5	%
	Gerr6 (G = 3.636)	-1.5	-	1.5	%
	Gerr7 (G = 4.000)	-1.5	-	1.5	%
	Gerr8 (G = 4.444)	-2.0	-	2.0	%
	Gerr9 (G = 5.000)	-2.0	-	2.0	%
	Gerr10 (G = 5.714)	-2.0	-	2.0	%
	Gerr11 (G = 6.667)	-2.0	-	2.0	%
	Gerr12 (G = 8.000)	-2.0	-	2.0	%
	Gerr13 (G = 10.000)	-2.0	-	2.0	%
	Gerr14 (G = 13.333)	-2.0	-	2.0	%
偏移误差	Voff	-8	-	8	mV

Table 60.52 差模下的PGA特性(1of2)

Parameter		Symbol	Min	Typ	Max	Unit
PGAVSS输入电压范围		PGAVSS	-0.5	-	0.3	V
差分输入电压范围	G = 1.500	AIN-PGAVSS	-0.5	-	0.5	V
	G = 2.333		-0.4	-	0.4	V
	G = 4.000		-0.2	-	0.2	V
	G = 5.667		-0.15	-	0.15	V

Table 60.52 PGA characteristics in differential mode (2 of 2)

Parameter		Symbol	Min	Typ	Max	Unit
Gain error	G = 1.500	Gerr	-1.0	-	1.0	%
	G = 2.333		-1.0	-	1.0	
	G = 4.000		-1.0	-	1.0	
	G = 5.667		-1.0	-	1.0	

60.14 Flash Memory Characteristics

60.14.1 Code Flash Memory Characteristics

Table 60.53 Code flash memory characteristics
Conditions: Program or erase: FCLK = 4 to 60 MHz
Read: FCLK ≤ 60 MHz

Parameter		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit	Test conditions
			Min	Typ	Max	Min	Typ	Max		
Programming time $N_{PEC} \leq 100$ times	128-byte	t_{P128}	-	0.75	13.2	-	0.34	6.0	ms	
	8-KB	t_{P8K}	-	49	176	-	22	80	ms	
	32-KB	t_{P32K}	-	194	704	-	88	320	ms	
Programming time $N_{PEC} > 100$ times	128-byte	t_{P128}	-	0.91	15.8	-	0.41	7.2	ms	
	8-KB	t_{P8K}	-	60	212	-	27	96	ms	
	32-KB	t_{P32K}	-	234	848	-	106	384	ms	
Erasure time $N_{PEC} \leq 100$ times	8-KB	t_{E8K}	-	78	216	-	43	120	ms	
	32-KB	t_{E32K}	-	283	864	-	157	480	ms	
Erasure time $N_{PEC} > 100$ times	8-KB	t_{E8K}	-	94	260	-	52	144	ms	
	32-KB	t_{E32K}	-	341	1040	-	189	576	ms	
Reprogramming/erasure cycle*Note:		N_{PEC}	10000*1	-	-	10000*1	-	-	Times	
Suspend delay during programming		t_{SPD}	-	-	264	-	-	120	µs	
First suspend delay during erasure in suspend priority mode		t_{SESD1}	-	-	216	-	-	120	µs	
Second suspend delay during erasure in suspend priority mode		t_{SESD2}	-	-	1.7	-	-	1.7	ms	
Suspend delay during erasure in erasure priority mode		t_{SEED}	-	-	1.7	-	-	1.7	ms	
Forced stop command		t_{FD}	-	-	32	-	-	20	µs	
Data hold time*2		t_{DRP}	10*2, *3	-	-	10*2, *3	-	-	Years	
			30*2, *3	-	-	30*2, *3	-	-		Ta = +85°C

Note: The reprogram/erase cycle is the number of erasures for each block. When the reprogram/erase cycle is n times (n = 10,000), erasing can be performed n times for each block. For example, when 128-byte programming is performed 64 times for different addresses in 8-KB blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address several times as one erasure is not enabled. (Overwriting is prohibited.)
Note 1. This is the minimum number of times to guarantee all the characteristics after reprogramming. The guaranteed range is from 1 to the minimum value.
Note 2. This indicates the minimum value of the characteristic when reprogramming is performed within the specified range.
Note 3. This result is obtained from reliability testing.

Table 60.52 差模下的PGA特性(2of2)

Parameter		Symbol	Min	Typ	Max	Unit
增益误差	G = 1.500	Gerr	-1.0	-	1.0	%
	G = 2.333		-1.0	-	1.0	
	G = 4.000		-1.0	-	1.0	
	G = 5.667		-1.0	-	1.0	

60.14 闪存特性

60.14.1 代码闪存特性

Table 60.53 代码闪存特性
条件：编程或擦除：FCLK=4至60MHz
Read: FCLK ≤ 60 MHz

Parameter		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit	测试条件
			Min	Typ	Max	Min	Typ	Max		
编程时间NPEC 100次	128-byte	t_{P128}	-	0.75	13.2	-	0.34	6.0	ms	
	8-KB	t_{P8K}	-	49	176	-	22	80	ms	
	32-KB	t_{P32K}	-	194	704	-	88	320	ms	
编程时间NPEC>100次	128-byte	t_{P128}	-	0.91	15.8	-	0.41	7.2	ms	
	8-KB	t_{P8K}	-	60	212	-	27	96	ms	
	32-KB	t_{P32K}	-	234	848	-	106	384	ms	
擦除时间 NPEC 100次	8-KB	t_{E8K}	-	78	216	-	43	120	ms	
	32-KB	t_{E32K}	-	283	864	-	157	480	ms	
擦除时间 NPEC>100次	8-KB	t_{E8K}	-	94	260	-	52	144	ms	
	32-KB	t_{E32K}	-	341	1040	-	189	576	ms	
Reprogramming/erasure cycle*Note:		N_{PEC}	10000*1	-	-	10000*1	-	-	Times	
编程期间暂停延迟		t_{SPD}	-	-	264	-	-	120	µs	
挂起优先模式下擦除期间的第一个挂起延迟		t_{SESD1}	-	-	216	-	-	120	µs	
挂起优先模式下擦除期间的第二挂起延迟		t_{SESD2}	-	-	1.7	-	-	1.7	ms	
擦除优先模式下擦除期间的挂起延迟		t_{SEED}	-	-	1.7	-	-	1.7	ms	
强制停止命令		t_{FD}	-	-	32	-	-	20	µs	
数据保持时间*2		t_{DRP}	10*2, *3	-	-	10*2, *3	-	-	Years	
			30*2, *3	-	-	30*2, *3	-	-		Ta = +85°C

Note: 重新编程擦除周期是每个块的擦除次数。当重新编程擦除周期为n次（n=10 000）时，可以对每个块执行n次擦除。例如，当对8KB块中的不同地址执行64次128字节编程，然后擦除整个块时，重新编程擦除周期计为1。但是，不能将同一地址多次编程为一次擦除。（禁止覆盖。）

Note 1. 这是重新编程后保证所有特性的最少次数。保证范围是从1到最小值。

Note 2. 这表示在指定范围内执行重新编程时特性的最小值。
Note 3. 这个结果是从可靠性测试中获得的。

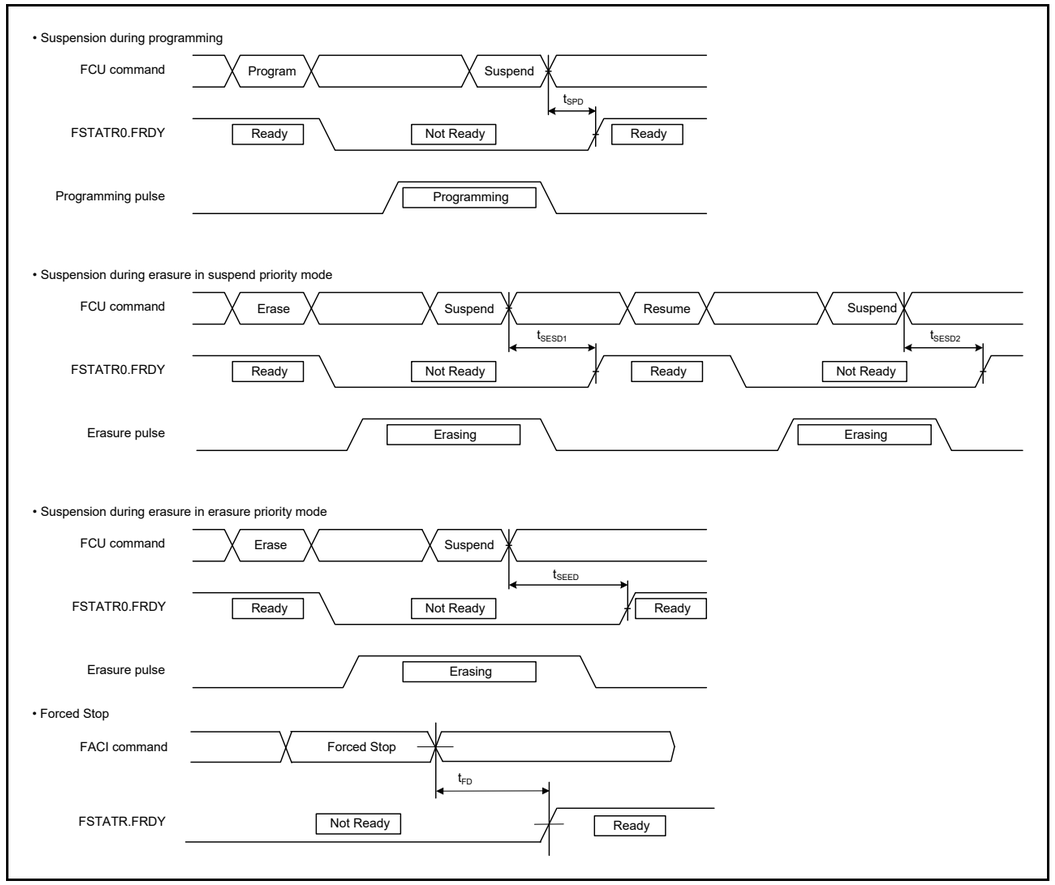


Figure 60.102 Suspension and forced stop timing for flash memory programming and erasure

60.14.2 Data Flash Memory Characteristics

Table 60.54 Data flash memory characteristics (1 of 2)
Conditions: Program or erase: FCLK = 4 to 60 MHz
Read: FCLK ≤ 60 MHz

Parameter		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit	Test conditions
			Min	Typ	Max	Min	Typ	Max		
Programming time	4-byte	t_{DP4}	-	0.36	3.8	-	0.16	1.7	ms	
	8-byte	t_{DP8}	-	0.38	4.0	-	0.17	1.8		
	16-byte	t_{DP16}	-	0.42	4.5	-	0.19	2.0		
Erasure time	64-byte	t_{DE64}	-	3.1	18	-	1.7	10	ms	
	128-byte	t_{DE128}	-	4.7	27	-	2.6	15		
	256-byte	t_{DE256}	-	8.9	50	-	4.9	28		
Blank check time	4-byte	t_{DBC4}	-	-	84	-	-	30	µs	
Reprogramming/erasure cycle*1		N_{DPEC}	125000 *2	-	-	125000 *2	-	-	-	

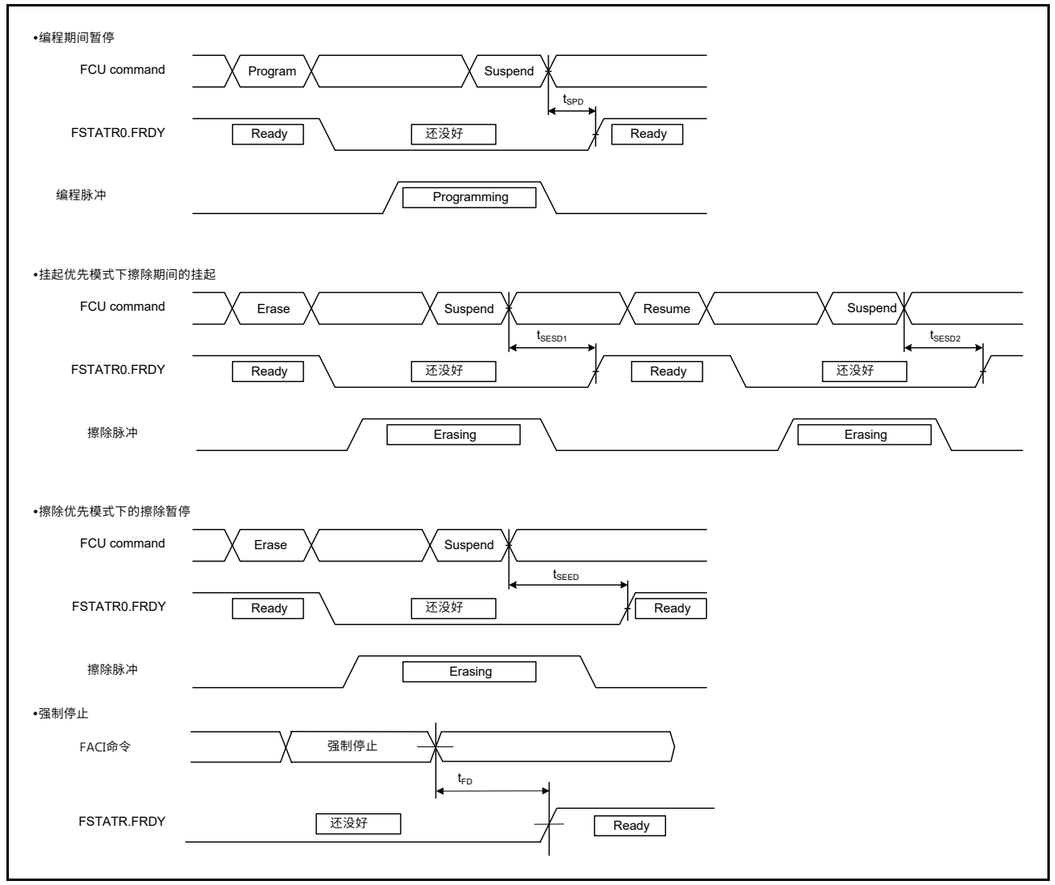


Figure 60.102 闪存编程和擦除的暂停和强制停止时序

60.14.2 数据闪存特性

Table 60.54 数据闪存特性(1of2)
条件：编程或擦除：FCLK=4至60MHz
Read: FCLK ≤ 60 MHz

Parameter		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit	测试条件
			Min	Typ	Max	Min	Typ	Max		
编程时间	4-byte	t_{DP4}	-	0.36	3.8	-	0.16	1.7	ms	
	8-byte	t_{DP8}	-	0.38	4.0	-	0.17	1.8		
	16-byte	t_{DP16}	-	0.42	4.5	-	0.19	2.0		
擦除时间	64-byte	t_{DE64}	-	3.1	18	-	1.7	10	ms	
	128-byte	t_{DE128}	-	4.7	27	-	2.6	15		
	256-byte	t_{DE256}	-	8.9	50	-	4.9	28		
空白检查时间	4-byte	t_{DBC4}	-	-	84	-	-	30	µs	
Reprogramming/erasure cycle*1		N_{DPEC}	125000 *2	-	-	125000 *2	-	-	-	

Table 60.54 Data flash memory characteristics (2 of 2)
Conditions: Program or erase: FCLK = 4 to 60 MHz
Read: FCLK ≤ 60 MHz

Parameter		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit	Test conditions
			Min	Typ	Max	Min	Typ	Max		
Suspend delay during programming	4-byte	t_{DSPD}	-	-	264	-	-	120	µs	
	8-byte		-	-	264	-	-	120		
	16-byte		-	-	264	-	-	120		
First suspend delay during erasure in suspend priority mode	64-byte	t_{DSESD1}	-	-	216	-	-	120	µs	
	128-byte		-	-	216	-	-	120		
	256-byte		-	-	216	-	-	120		
Second suspend delay during erasure in suspend priority mode	64-byte	t_{DSESD2}	-	-	300	-	-	300	µs	
	128-byte		-	-	390	-	-	390		
	256-byte		-	-	570	-	-	570		
Suspend delay during erasing in erasure priority mode	64-byte	t_{DSEED}	-	-	300	-	-	300	µs	
	128-byte		-	-	390	-	-	390		
	256-byte		-	-	570	-	-	570		
Forced stop command		t_{FD}	-	-	32	-	-	20	µs	
Data hold time*3		t_{DRP}	10*3,*4	-	-	10*3,*4	-	-	Year	
			30*3,*4	-	-	30*3,*4	-	-		Ta = +85°C

Note 1. The reprogram/erase cycle is the number of erasures for each block. When the reprogram/erase cycle is n times (n = 125,000), erasing can be performed n times for each block. For example, when 4-byte programming is performed 16 times for different addresses in 64-byte blocks, and then the entire block is erased, the reprogram/erase cycle is counted as one. However, programming the same address several times as one erasure is not enabled. (Overwriting is prohibited.)
Note 2. This is the minimum number of times to guarantee all the characteristics after reprogramming. The guaranteed range is from 1 to the minimum value.
Note 3. This indicates the minimum value of the characteristic when reprogramming is performed within the specified range.
Note 4. This result is obtained from reliability testing.

60.15 Boundary Scan

Table 60.55 Boundary scan characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
TCK clock cycle time	t_{TCKcyc}	100	-	-	ns	Figure 60.103
TCK clock high pulse width	t_{TCKH}	45	-	-	ns	
TCK clock low pulse width	t_{TCKL}	45	-	-	ns	
TCK clock rise time	t_{TCKr}	-	-	5	ns	
TCK clock fall time	t_{TCKf}	-	-	5	ns	
TMS setup time	t_{TMSS}	20	-	-	ns	Figure 60.104
TMS hold time	t_{TMSH}	20	-	-	ns	
TDI setup time	t_{TDIS}	20	-	-	ns	
TDI hold time	t_{TDIH}	20	-	-	ns	
TDO data delay	t_{TDOD}	-	-	40	ns	
Boundary scan circuit startup time*1	T_{BSSTUP}	t_{RESWP}	-	-	-	Figure 60.105

Note 1. Boundary scan does not function until the power-on reset becomes negative.

Table 60.54 数据闪存特性(2of2)
条件：编程或擦除：FCLK=4至60MHz
Read: FCLK ≤ 60 MHz

Parameter		Symbol	FCLK = 4 MHz			20 MHz ≤ FCLK ≤ 60 MHz			Unit	测试条件
			Min	Typ	Max	Min	Typ	Max		
编程期间暂停延迟	4-byte	t_{DSPD}	-	-	264	-	-	120	µs	
	8-byte		-	-	264	-	-	120		
	16-byte		-	-	264	-	-	120		
挂起优先模式下擦除期间的第一个挂起延迟	64-byte	t_{DSESD1}	-	-	216	-	-	120	µs	
	128-byte		-	-	216	-	-	120		
	256-byte		-	-	216	-	-	120		
挂起优先模式下擦除期间的第二挂起延迟	64-byte	t_{DSESD2}	-	-	300	-	-	300	µs	
	128-byte		-	-	390	-	-	390		
	256-byte		-	-	570	-	-	570		
在擦除优先模式下擦除期间暂停延迟	64-byte	t_{DSEED}	-	-	300	-	-	300	µs	
	128-byte		-	-	390	-	-	390		
	256-byte		-	-	570	-	-	570		
强制停止命令		t_{FD}	-	-	32	-	-	20	µs	
数据保持时间*3		t_{DRP}	10*3,*4	-	-	10*3,*4	-	-	Year	
			30*3,*4	-	-	30*3,*4	-	-		Ta = +85°C

Note 1. 重新编程擦除周期是每个块的擦除次数。当重新编程擦除周期为n次（n=125 000）时，可以对每个块执行n次擦除。例如，当对64字节块中的不同地址执行16次4字节编程，然后擦除整个块时，重新编程擦除周期计为1。但是，不能将同一地址多次编程为一次擦除。（禁止覆盖。）
Note 2. 这是重新编程后保证所有特性的最少次数。保证范围是从1到最小值。
Note 3. 这表示在指定范围内执行重新编程时特性的最小值。
Note 4. 这个结果是从可靠性测试中获得的。

60.15 边界扫描

Table 60.55 边界扫描特性

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
TCK时钟周期时间	t_{TCKcyc}	100	-	-	ns	Figure 60.103
TCK时钟高脉冲宽度	t_{TCKH}	45	-	-	ns	
TCK时钟低脉冲宽度	t_{TCKL}	45	-	-	ns	
TCK时钟上升时间	t_{TCKr}	-	-	5	ns	
TCK时钟下降时间	t_{TCKf}	-	-	5	ns	
TMS设置时间	t_{TMSS}	20	-	-	ns	Figure 60.104
TMS保持时间	t_{TMSH}	20	-	-	ns	
TDI建立时间	t_{TDIS}	20	-	-	ns	
TDI保持时间	t_{TDIH}	20	-	-	ns	
TDO数据延迟	t_{TDOD}	-	-	40	ns	
边界扫描电路启动时间*1	T_{BSSTUP}	t_{RESWP}	-	-	-	Figure 60.105

Note 1. 在上电复位变为负值之前，边界扫描不起作用。

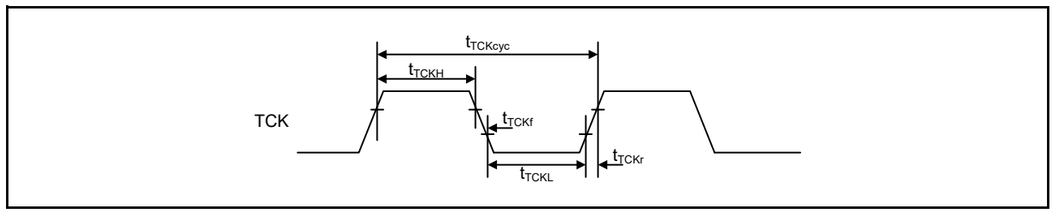


Figure 60.103 Boundary scan TCK timing

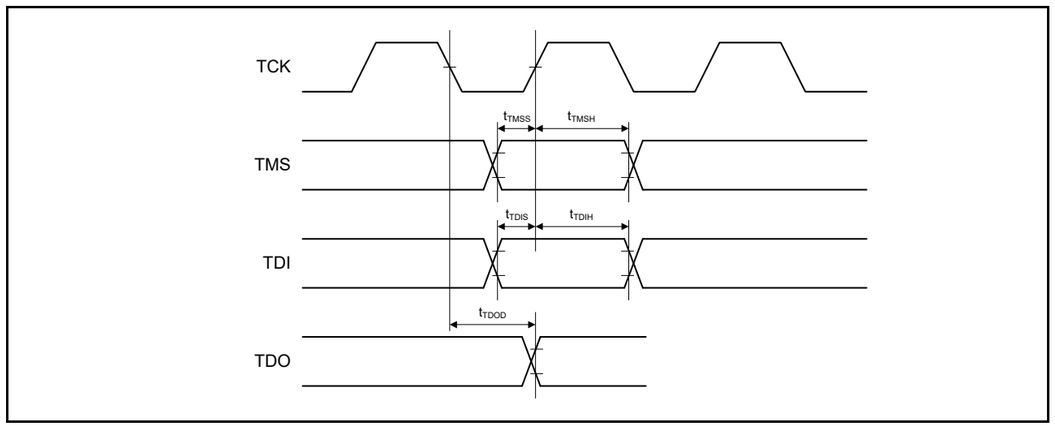


Figure 60.104 Boundary scan input/output timing

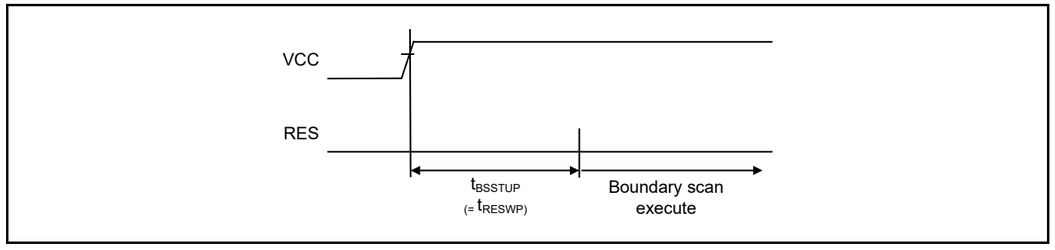


Figure 60.105 Boundary scan circuit startup timing

60.16 Joint Test Action Group (JTAG)

Table 60.56 JTAG

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
TCK clock cycle time	t_{TCKcyc}	40	-	-	ns	Figure 60.103
TCK clock high pulse width	t_{TCKH}	15	-	-	ns	
TCK clock low pulse width	t_{TCKL}	15	-	-	ns	
TCK clock rise time	t_{TCKr}	-	-	5	ns	
TCK clock fall time	t_{TCKf}	-	-	5	ns	

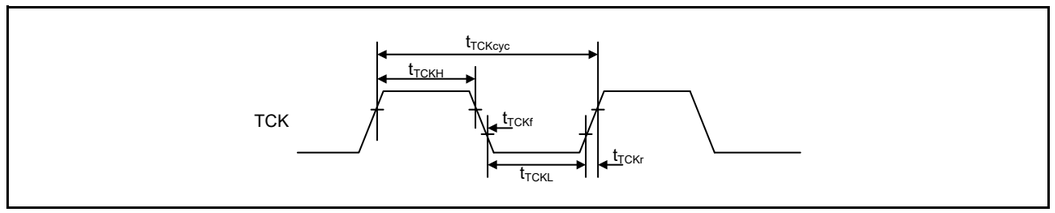


Figure 60.103 边界扫描TCK时序

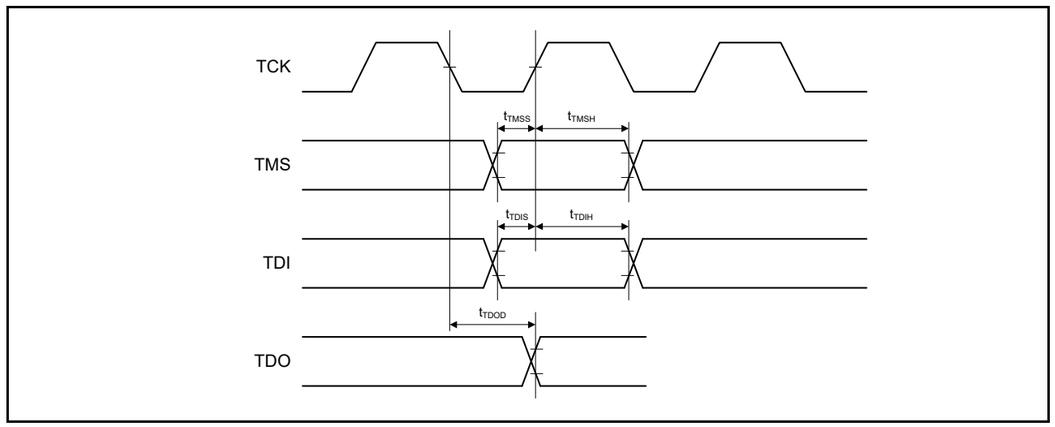


Figure 60.104 边界扫描输入输出时序

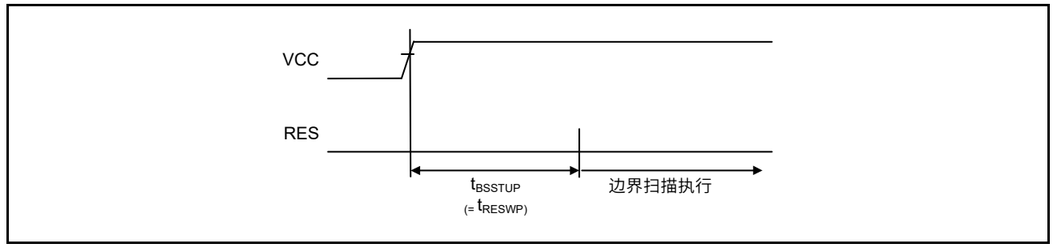


Figure 60.105 边界扫描电路启动时序

60.16 联合测试行动组(JTAG)

Table 60.56 JTAG

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
TCK时钟周期时间	t_{TCKcyc}	40	-	-	ns	Figure 60.103
TCK时钟高脉冲宽度	t_{TCKH}	15	-	-	ns	
TCK时钟低脉冲宽度	t_{TCKL}	15	-	-	ns	
TCK时钟上升时间	t_{TCKr}	-	-	5	ns	
TCK时钟下降时间	t_{TCKf}	-	-	5	ns	

Table 60.56 JTAG

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
TMS setup time	t_{TMSS}	8	-	-	ns	Figure 60.104
TMS hold time	t_{TMSH}	8	-	-	ns	
TDI setup time	t_{TDIS}	8	-	-	ns	
TDI hold time	t_{TDIH}	8	-	-	ns	
TDO data delay time	t_{TDOD}	-	-	20	ns	

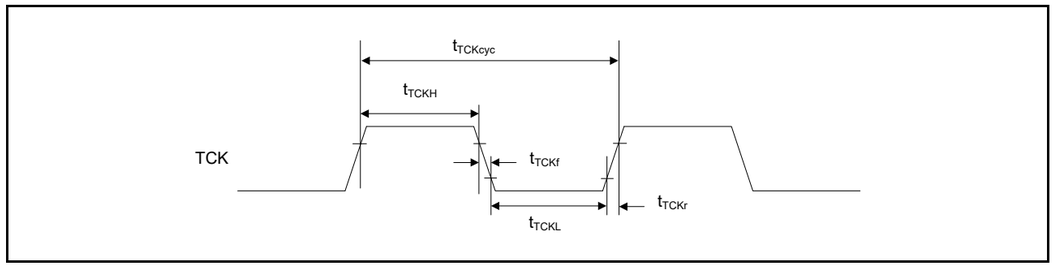


Figure 60.106 JTAG TCK timing

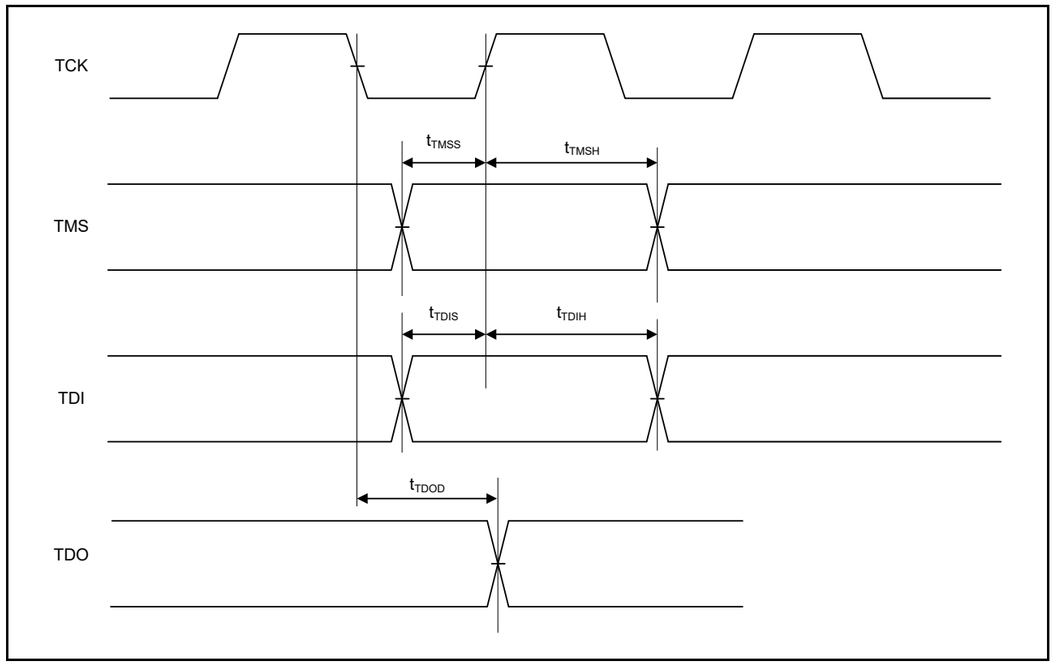


Figure 60.107 JTAG input/output timing

Table 60.56 JTAG

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
TMS设置时间	t_{TMSS}	8	-	-	ns	Figure 60.104
TMS保持时间	t_{TMSH}	8	-	-	ns	
TDI建立时间	t_{TDIS}	8	-	-	ns	
TDI保持时间	t_{TDIH}	8	-	-	ns	
TDO数据延迟时间	t_{TDOD}	-	-	20	ns	

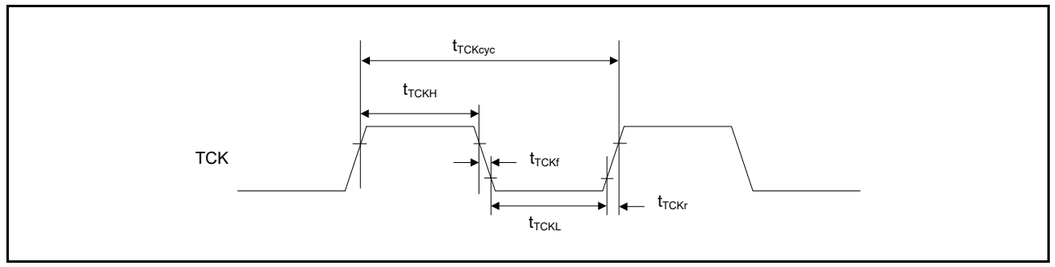


Figure 60.106 JTAG TCK timing

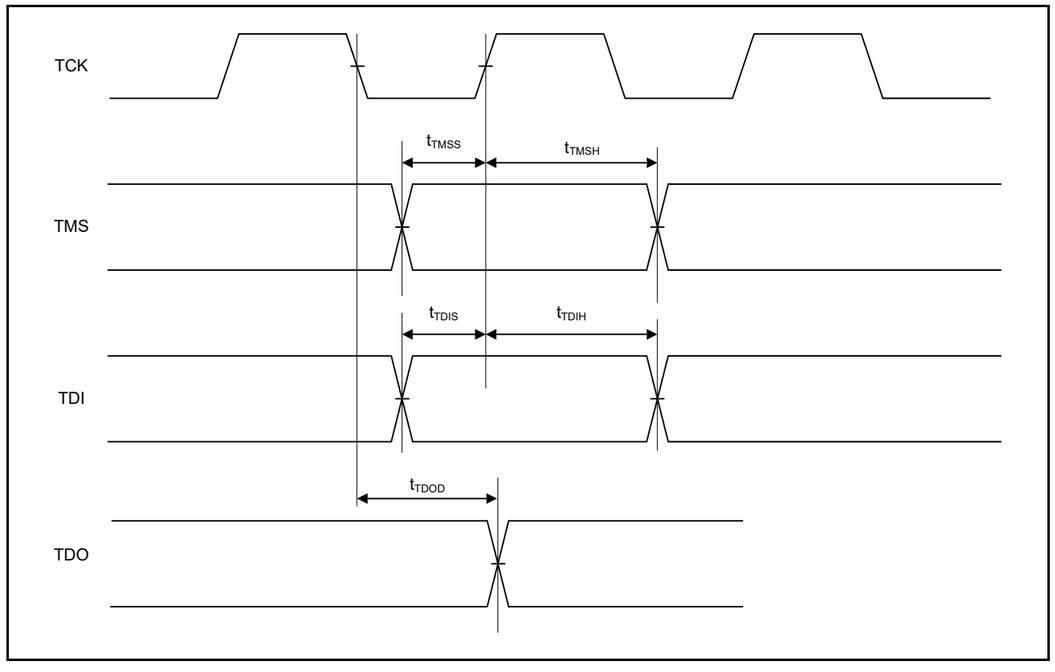


Figure 60.107 JTAG input/output timing

60.17 Serial Wire Debug (SWD)

Table 60.57 SWD

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
SWCLK clock cycle time	$t_{SWCKcyc}$	40	-	-	ns	Figure 60.108
SWCLK clock high pulse width	t_{SWCKH}	15	-	-	ns	
SWCLK clock low pulse width	t_{SWCKL}	15	-	-	ns	
SWCLK clock rise time	t_{SWCKr}	-	-	5	ns	
SWCLK clock fall time	t_{SWCKf}	-	-	5	ns	
SWDIO setup time	t_{SWDS}	8	-	-	ns	Figure 60.109
SWDIO hold time	t_{SWDH}	8	-	-	ns	
SWDIO data delay time	t_{SWDD}	2	-	28	ns	

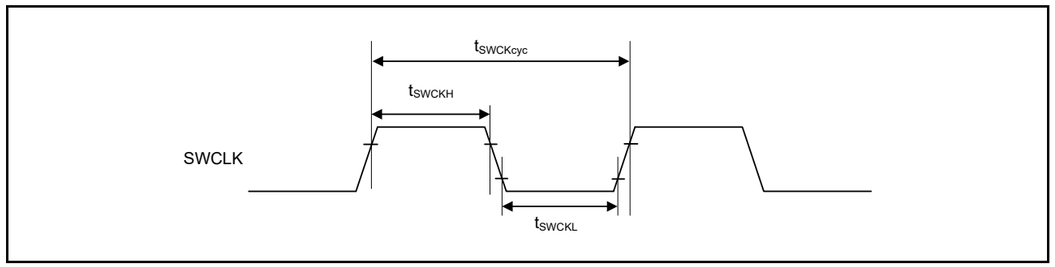


Figure 60.108 SWD SWCLK timing

60.17 串行线调试(SWD)

Table 60.57 SWD

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
SWCLK时钟周期时间	$t_{SWCKcyc}$	40	-	-	ns	Figure 60.108
SWCLK时钟高脉冲宽度	t_{SWCKH}	15	-	-	ns	
SWCLK时钟低脉冲宽度	t_{SWCKL}	15	-	-	ns	
SWCLK时钟上升时间	t_{SWCKr}	-	-	5	ns	
SWCLK时钟下降时间	t_{SWCKf}	-	-	5	ns	
SWDIO设置时间	t_{SWDS}	8	-	-	ns	Figure 60.109
SWDIO保持时间	t_{SWDH}	8	-	-	ns	
SWDIO数据延迟时间	t_{SWDD}	2	-	28	ns	

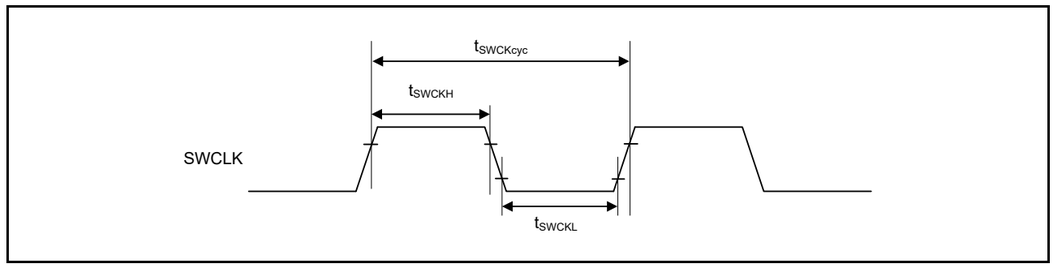


Figure 60.108 SWD SWCLK timing

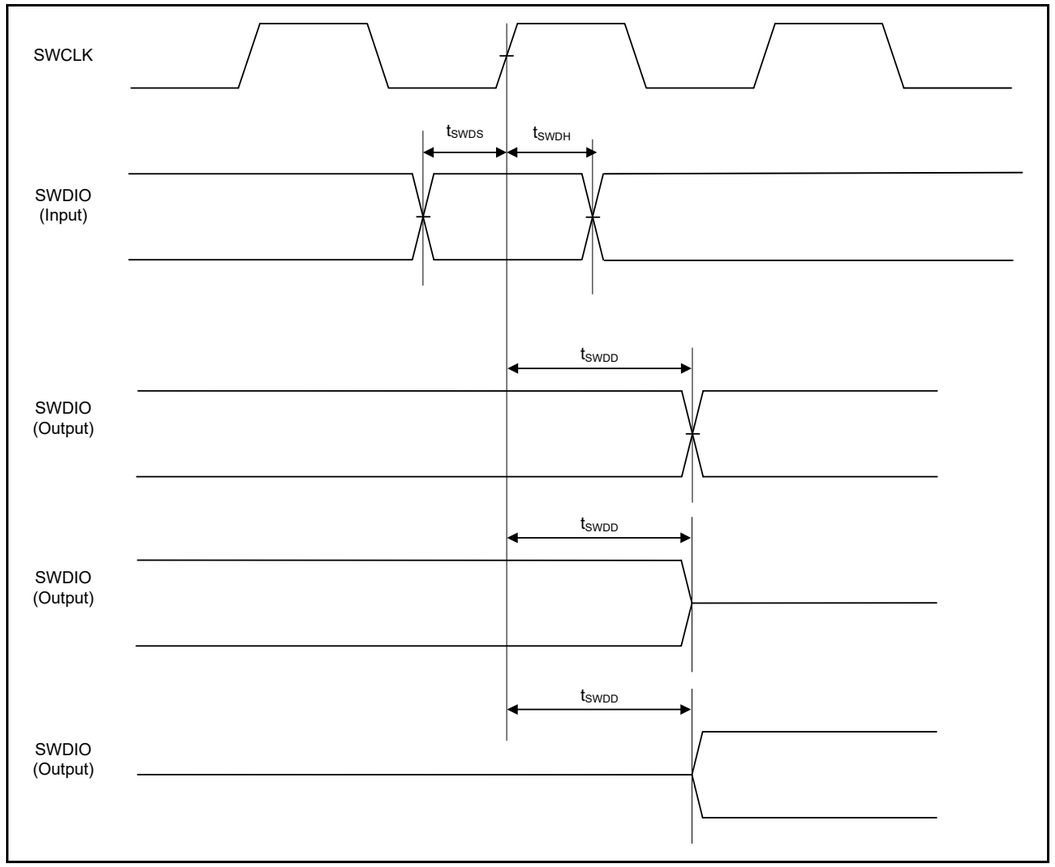


Figure 60.109 SWD input/output timing

60.18 Embedded Trace Macro Interface (ETM)

Table 60.58 ETM
Conditions: High drive output is selected in the port drive capability bit in the PmnPFS register.

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions
TCLK clock cycle time	$t_{TCLKcyc}$	33.3	-	-	ns	Figure 60.110
TCLK clock high pulse width	t_{TCLKH}	13.6	-	-	ns	
TCLK clock low pulse width	t_{TCLKL}	13.6	-	-	ns	
TCLK clock rise time	t_{TCLKr}	-	-	3	ns	
TCLK clock fall time	t_{TCLKf}	-	-	3	ns	
TDATA[3:0] output setup time	t_{TRDS}	3.5	-	-	ns	Figure 60.111
TDATA[3:0] output hold time	t_{TRDH}	2.5	-	-	ns	

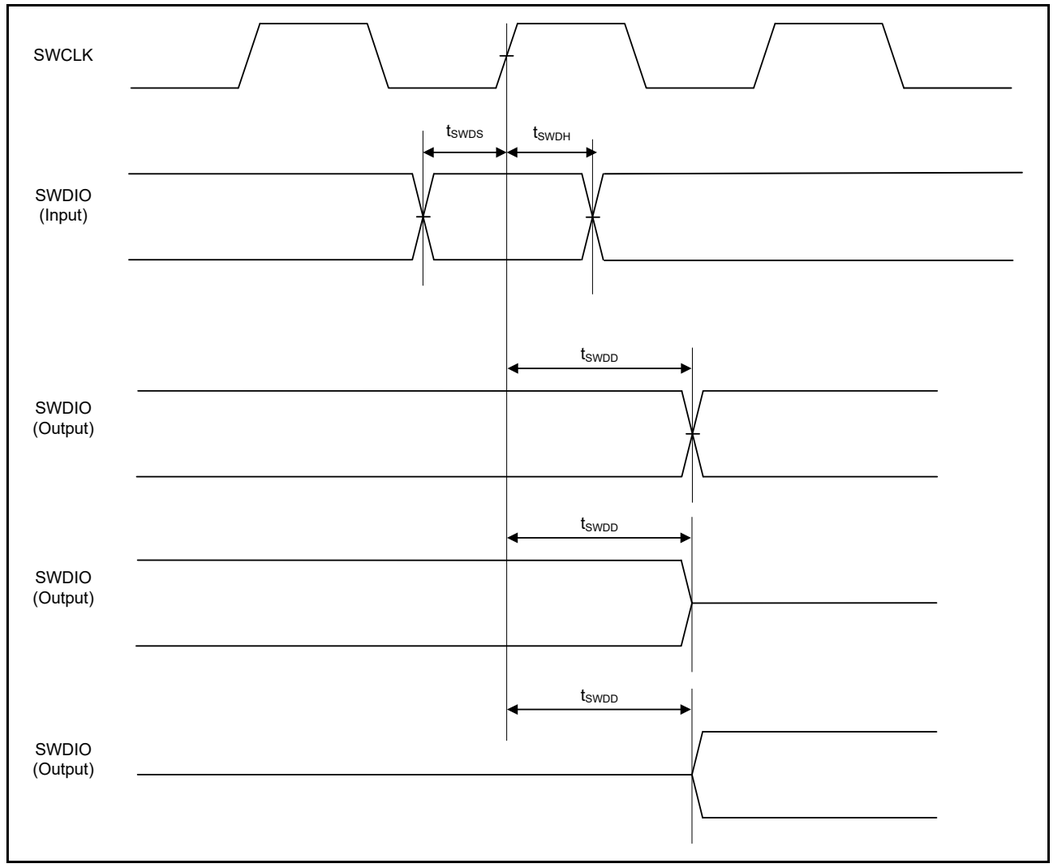


Figure 60.109 SWD input/output timing

60.18 嵌入式跟踪宏接口(ETM)

Table 60.58 ETM
条件：在PmnPFS寄存器的端口驱动能力位中选择高驱动输出。

Parameter	Symbol	Min	Typ	Max	Unit	测试条件
TCLK时钟周期时间	$t_{TCLKcyc}$	33.3	-	-	ns	Figure 60.110
TCLK时钟高脉冲宽度	t_{TCLKH}	13.6	-	-	ns	
TCLK时钟低脉冲宽度	t_{TCLKL}	13.6	-	-	ns	
TCLK时钟上升时间	t_{TCLKr}	-	-	3	ns	
TCLK时钟下降时间	t_{TCLKf}	-	-	3	ns	
TDATA[3:0]输出建立时间	t_{TRDS}	3.5	-	-	ns	Figure 60.111
TDATA[3:0]输出保持时间	t_{TRDH}	2.5	-	-	ns	

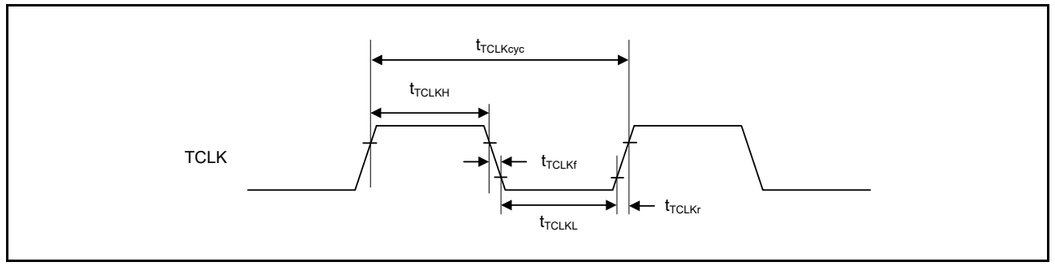


Figure 60.110 ETM TCLK timing

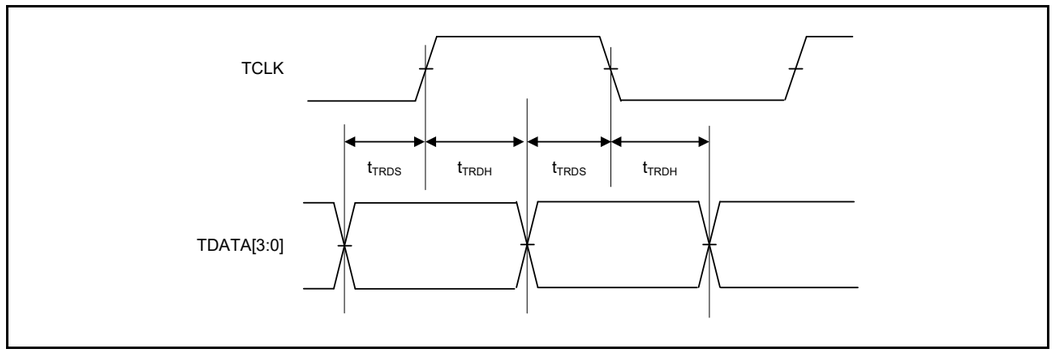


Figure 60.111 ETM output timing

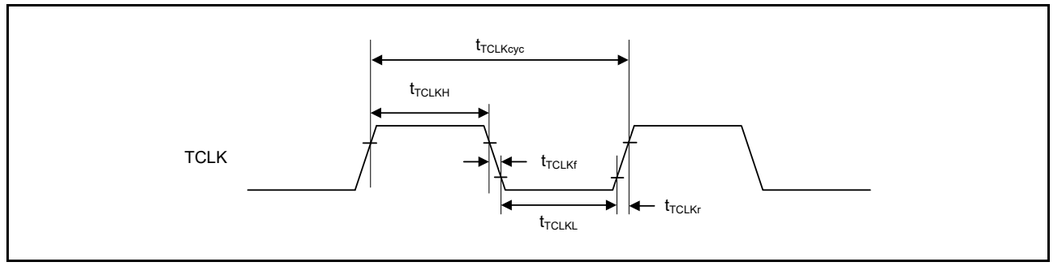


Figure 60.110 ETM TCLK timing

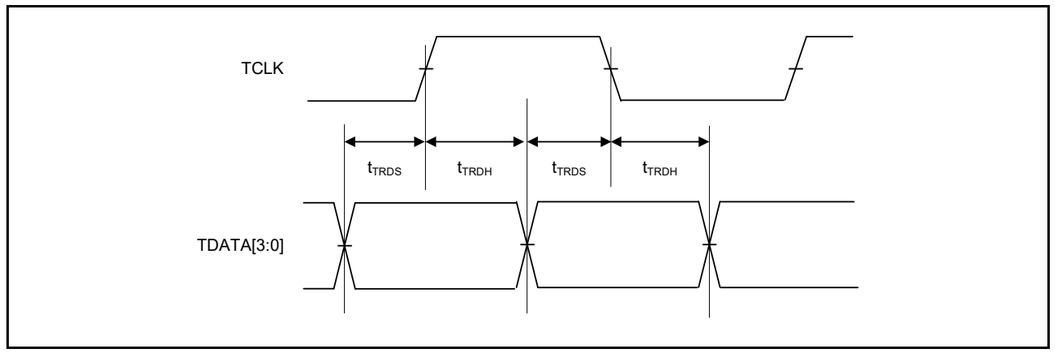


Figure 60.111 ETM输出时序

Appendix 1. Port States in Each Processing Mode

Table 1.1 Port states in each processing state (1 of 6)

Port name	Reset	Software Standby mode		Deep Software Standby mode	After Deep Software Standby mode is canceled (return to startup mode)	
		OPE = 0	OPE = 1		IOKEEP = 0	IOKEEP = 1*1
P000/IRQ6-DS, P001/IRQ7-DS, P002/IRQ8-DS	Hi-Z	Hi-Z*2		Keep-O*3	Hi-Z	Keep
P003	Hi-Z	Hi-Z		Keep	Hi-Z	Keep
P004/IRQ9-DS, P005/IRQ10-DS, P006/IRQ11-DS	Hi-Z	Hi-Z*2		Keep-O*3	Hi-Z	Keep
P007	Hi-Z	Hi-Z		Keep	Hi-Z	Keep
P008/IRQ12-DS, P009/IRQ13-DS, P010/IRQ14-DS	Hi-Z	Keep-O*2		Keep-O*3	Hi-Z	Keep
P014/DA0	Hi-Z	[DA0 output (DAOE0 = 1)] D/A output retained [All other (DAOE0 = 0)] Keep-O		Keep	Hi-Z	Keep
P015/IRQ13/DA1	Hi-Z	[DA1 output (DAOE1 = 1)] D/A output retained [All other (DAOE1 = 0)] Keep-O*2		Keep	Hi-Z	Keep
P100/D00[A00/D00]/ DQ00/KR00/AGTIO0/ RXD0/IRQ2	Hi-Z	[D00 output] Hi-Z [DQ00 output] Hi-Z [All other] Keep-O*2		Keep	Hi-Z	Keep
P101/D01[A01/D01]/ DQ01/KR01/IRQ1	Hi-Z	[D01 output] Hi-Z [DQ01 output] Hi-Z [All other] Keep-O*2		Keep	Hi-Z	Keep
P102/D02[A02/D02]/ DQ02/KR02	Hi-Z	[D02 output] Hi-Z [DQ02 output] Hi-Z [All other] Keep-O*2		Keep	Hi-Z	Keep
P103/D03[A03/D03]/ DQ03/KR03	Hi-Z	[D03 output] Hi-Z [DQ03 output] Hi-Z [All other] Keep-O*2		Keep	Hi-Z	Keep
P104/D04[A04/D04]/ DQ04/KR04/IRQ1	Hi-Z	[D04 output] Hi-Z [DQ04 output] Hi-Z [All other] Keep-O*2		Keep	Hi-Z	Keep
P105/D05[A05/D05]/ DQ05/KR05/IRQ0	Hi-Z	[D05 output] Hi-Z [DQ05 output] Hi-Z [All other] Keep-O*2		Keep	Hi-Z	Keep
P106/D06[A06/D06]/ DQ06/KR06	Hi-Z	[D06 output] Hi-Z [DQ06 output] Hi-Z [All other] Keep-O*2		Keep	Hi-Z	Keep
P107/D07[A07/D07]/ DQ07/KR07	Hi-Z	[D07 output] Hi-Z [DQ07 output] Hi-Z [All other] Keep-O*2		Keep	Hi-Z	Keep
P108/TMS	Pull-up	Keep-O		Keep	Pull-up	Keep

附录1.每种处理模式下的端口状态

Table 1.1 每个处理状态中的端口状态（6个中的1个）

端口名称	Reset	软件待机模式		深度软件待机模式	取消深度软件待机模式后（返回启动模式）	
		OPE = 0	OPE = 1		IOKEEP = 0	IOKEEP = 1*1
P000/IRQ6-DS, P001/IRQ7-DS, P002/IRQ8-DS	Hi-Z	Hi-Z*2		Keep-O*3	Hi-Z	Keep
P003	Hi-Z	Hi-Z		Keep	Hi-Z	Keep
P004/IRQ9-DS, P005/IRQ10-DS, P006/IRQ11-DS	Hi-Z	Hi-Z*2		Keep-O*3	Hi-Z	Keep
P007	Hi-Z	Hi-Z		Keep	Hi-Z	Keep
P008/IRQ12-DS, P009/IRQ13-DS, P010/IRQ14-DS	Hi-Z	Keep-O*2		Keep-O*3	Hi-Z	Keep
P014/DA0	Hi-Z	[DA0输出(DAOE0=1)]DA 输出保留[所有其他(DAOE 0=0)]保持-O		Keep	Hi-Z	Keep
P015/IRQ13/DA1	Hi-Z	[DA1输出(DAOE1=1)]DA 输出保持[所有其他(DAOE 1=0)]Keep-O•2		Keep	Hi-Z	Keep
P100/D00[A00/D00]/ DQ00/KR00/AGTIO0/ RXD0/IRQ2	Hi-Z	[D00 output] Hi-Z [DQ00 output] Hi-Z [All other] Keep-O*2		Keep	Hi-Z	Keep
P101/D01[A01/D01]/ DQ01/KR01/IRQ1	Hi-Z	[D01 output] Hi-Z [DQ01 output] Hi-Z [All other] Keep-O*2		Keep	Hi-Z	Keep
P102/D02[A02/D02]/ DQ02/KR02	Hi-Z	[D02 output] Hi-Z [DQ02 output] Hi-Z [All other] Keep-O*2		Keep	Hi-Z	Keep
P103/D03[A03/D03]/ DQ03/KR03	Hi-Z	[D03 output] Hi-Z [DQ03 output] Hi-Z [All other] Keep-O*2		Keep	Hi-Z	Keep
P104/D04[A04/D04]/ DQ04/KR04/IRQ1	Hi-Z	[D04 output] Hi-Z [DQ04 output] Hi-Z [All other] Keep-O*2		Keep	Hi-Z	Keep
P105/D05[A05/D05]/ DQ05/KR05/IRQ0	Hi-Z	[D05 output] Hi-Z [DQ05 output] Hi-Z [All other] Keep-O*2		Keep	Hi-Z	Keep
P106/D06[A06/D06]/ DQ06/KR06	Hi-Z	[D06 output] Hi-Z [DQ06 output] Hi-Z [All other] Keep-O*2		Keep	Hi-Z	Keep
P107/D07[A07/D07]/ DQ07/KR07	Hi-Z	[D07 output] Hi-Z [DQ07 output] Hi-Z [All other] Keep-O*2		Keep	Hi-Z	Keep
P108/TMS	Pull-up	Keep-O		Keep	Pull-up	Keep

Table 1.1 Port states in each processing state (2 of 6)

Port name	Reset	Software Standby mode		Deep Software Standby mode	After Deep Software Standby mode is canceled (return to startup mode)	
		OPE = 0	OPE = 1		IOKEEP = 0	IOKEEP = 1*1
P109/TDO/ CLKOUT	TDO output	[CLKOUT selected] CLKOUT output [All other] Keep-O		[TDO output] TDO output retained [All other] Keep	[TDO output] TDO output retained [All other] Hi-Z	[TDO output] TDO output retained [All other] Keep
P110/IRQ3/TDI/ VCOUT	Pull-up	[ACMPHS selected] VCOUT output [All other] Keep-O*2		Keep	Pull-up	Keep
P111/A05/IRQ4	Hi-Z	[A05 output] Hi-Z [All other] Keep-O*2	[A05 output] Address output retained [All other] Keep-O*2	Keep	Hi-Z	Keep
P112/A04	Hi-Z	[A04 output] Hi-Z [All other] Keep-O	[A04 output] Address output retained [All other] Keep-O	Keep	Hi-Z	Keep
P113/A03	Hi-Z	[A03 output] Hi-Z [All other] Keep-O	[A03 output] Address output retained [All other] Keep-O	Keep	Hi-Z	Keep
P114/A02	Hi-Z	[A02 output] Hi-Z [All other] Keep-O	[A02 output] Address output retained [All other] Keep-O	Keep	Hi-Z	Keep
P115/A01	Hi-Z	[A01 output] Hi-Z [All other] Keep-O	[A01 output] Address output retained [All other] Keep-O	Keep	Hi-Z	Keep
P200/NMI	Hi-Z	Hi-Z		Keep	Hi-Z	Keep
P201	Pull-up	Keep-O		Keep	Pull-up	Keep
P202/WR1/BC1/ IRQ3-DS	Hi-Z	[WR1/BC1 output] Hi-Z [All other] Keep-O*2	[WR1/BC1 output] H [All other] Keep-O*2	Keep-O*3	Hi-Z	Keep
P203/A19/ IRQ2-DS	Hi-Z	[A19 output] Hi-Z [All other] Keep-O*2	[A19 output] Address output retained [All other] Keep-O*2	Keep-O*3	Hi-Z	Keep
P204/A18/AGTIO1/ SCL0_B/USB_ OVRCURB-DS	Hi-Z	[A18 output] Hi-Z [All other] Keep-O*2	[A18 output] Address output retained [All other] Keep-O*2	Keep-O*3	Hi-Z	Keep
P205/A16/USB_ OVRCURA-DS/ CLKOUT/IRQ1-DS	Hi-Z	[A16 output] Hi-Z [CLKOUT selected] CLKOUT output [All other] Keep-O*2	[A16 output] Address output retained [CLKOUT selected] CLKOUT output [All other] Keep-O*2	Keep-O*3	Hi-Z	Keep
P206/WAIT/IRQ0-DS	Hi-Z	Keep-O*2		Keep-O*3	Hi-Z	Keep
P207/A17	Hi-Z	[A17 output] Hi-Z [All other] Keep-O	[A17 output] Address output retained [All other] Keep-O	Keep	Hi-Z	Keep
P208 to P211	Hi-Z	Keep-O		Keep	Hi-Z	Keep
P212/IRQ3/EXTAL, P213/IRQ2/XTAL	Hi-Z	Keep-O*2		Keep	Hi-Z	Keep
P214	Hi-Z	Keep-O		Keep	Hi-Z	Keep
P300/TCK	Pull-up	Keep-O		Keep	Pull-up	Keep
P301/A06/AGTIO0/ IRQ6	Hi-Z	[A06 output] Hi-Z [All other] Keep-O*2	[A06 output] Address output retained [All other] Keep-O*2	Keep	Hi-Z	Keep
P302/A07/IRQ5	Hi-Z	[A07 output] Hi-Z [All other] Keep-O*2	[A07 output] Address output retained [All other] Keep-O*2	Keep	Hi-Z	Keep
P303/A08	Hi-Z	[A08 output] Hi-Z [All other] Keep-O	[A08 output] Address output retained [All other] Keep-O	Keep	Hi-Z	Keep
P304/A09/IRQ9	Hi-Z	[A09 output] Hi-Z [All other] Keep-O*2	[A09 output] Address output retained [All other] Keep-O*2	Keep	Hi-Z	Keep

Table 1.1 每个处理状态中的端口状态（6个中的2个）

端口名称	Reset	软件待机模式		深度软件待机模式	取消深度软件待机模式后（返回启动模式）	
		OPE = 0	OPE = 1		IOKEEP = 0	IOKEEP = 1*1
P109/TDO/ CLKOUT	TDO输出	[CLKOUT selected] CLKOUT output [All other] Keep-O		[TDO输出]TDO输出保留[所有其他]保留	[TDO输出]TDO输出保留[所有其他]Hi-Z	[TDO输出]TDO输出保留[所有其他]保留
P110/IRQ3/TDI/ VCOUT	Pull-up	[ACMPHS selected] VCOUT output [All other] Keep-O*2		Keep	Pull-up	Keep
P111/A05/IRQ4	Hi-Z	[A05 output] Hi-Z [All other] Keep-O*2	[A05输出]地址输出保持[所有其他]Keep-O*2	Keep	Hi-Z	Keep
P112/A04	Hi-Z	[A04 output] Hi-Z [All other] Keep-O	[A04输出]地址输出保留[所有其他]Keep-O	Keep	Hi-Z	Keep
P113/A03	Hi-Z	[A03 output] Hi-Z [All other] Keep-O	[A03输出]地址输出保留[所有其他]Keep-O	Keep	Hi-Z	Keep
P114/A02	Hi-Z	[A02 output] Hi-Z [All other] Keep-O	[A02输出]地址输出保留[所有其他]Keep-O	Keep	Hi-Z	Keep
P115/A01	Hi-Z	[A01 output] Hi-Z [All other] Keep-O	[A01输出]地址输出保留[所有其他]Keep-O	Keep	Hi-Z	Keep
P200/NMI	Hi-Z	Hi-Z		Keep	Hi-Z	Keep
P201	Pull-up	Keep-O		Keep	Pull-up	Keep
P202/WR1/BC1/ IRQ3-DS	Hi-Z	[WR1/BC1 output] Hi-Z [All other] Keep-O*2	[WR1/BC1 output] H [All other] Keep-O*2	Keep-O*3	Hi-Z	Keep
P203/A19/ IRQ2-DS	Hi-Z	[A19 output] Hi-Z [All other] Keep-O*2	[A19输出]地址输出保持[所有其他]Keep-O*2	Keep-O*3	Hi-Z	Keep
P204/A18/AGTIO1/ SCL0_B/USB_ OVRCURB-DS	Hi-Z	[A18 output] Hi-Z [All other] Keep-O*2	[A18输出]地址输出保持[所有其他]Keep-O*2	Keep-O*3	Hi-Z	Keep
P205/A16/USB_ OVRCURA-DS/ CLKOUT/IRQ1-DS	Hi-Z	[A16 output] Hi-Z [CLKOUT selected] CLKOUT output [All other] Keep-O*2	[A16输出]地址输出保持[CLKOUT选择]CLKOUT输出[所有其他]Keep-O*2	Keep-O*3	Hi-Z	Keep
P206/WAIT/IRQ0-DS	Hi-Z	Keep-O*2		Keep-O*3	Hi-Z	Keep
P207/A17	Hi-Z	[A17 output] Hi-Z [All other] Keep-O	[A17输出]地址输出保留[所有其他]Keep-O	Keep	Hi-Z	Keep
P208 to P211	Hi-Z	Keep-O		Keep	Hi-Z	Keep
P212/IRQ3/EXTAL, P213/IRQ2/XTAL	Hi-Z	Keep-O*2		Keep	Hi-Z	Keep
P214	Hi-Z	Keep-O		Keep	Hi-Z	Keep
P300/TCK	Pull-up	Keep-O		Keep	Pull-up	Keep
P301/A06/AGTIO0/ IRQ6	Hi-Z	[A06 output] Hi-Z [All other] Keep-O*2	[A06输出]地址输出保持[所有其他]Keep-O*2	Keep	Hi-Z	Keep
P302/A07/IRQ5	Hi-Z	[A07 output] Hi-Z [All other] Keep-O*2	[A07输出]地址输出保持[所有其他]Keep-O*2	Keep	Hi-Z	Keep
P303/A08	Hi-Z	[A08 output] Hi-Z [All other] Keep-O	[A08输出]地址输出保留[所有其他]Keep-O	Keep	Hi-Z	Keep
P304/A09/IRQ9	Hi-Z	[A09 output] Hi-Z [All other] Keep-O*2	[A09输出]地址输出保持[所有其他]Keep-O*2	Keep	Hi-Z	Keep

Table 1.1 Port states in each processing state (3 of 6)

Port name	Reset	Software Standby mode		Deep Software Standby mode	After Deep Software Standby mode is canceled (return to startup mode)	
		OPE = 0	OPE = 1		IOKEEP = 0	IOKEEP = 1*1
P305/A10/IRQ8	Hi-Z	[A10 output] Hi-Z [All other] Keep-O*2	[A10 output] Address output retained [All other] Keep-O*2	Keep	Hi-Z	Keep
P306/A11	Hi-Z	[A11 output] Hi-Z [All other] Keep-O	[A11 output] Address output retained [All other] Keep-O	Keep	Hi-Z	Keep
P307/A12	Hi-Z	[A12 output] Hi-Z [All other] Keep-O	[A12 output] Address output retained [All other] Keep-O	Keep	Hi-Z	Keep
P308/A13	Hi-Z	[A13 output] Hi-Z [All other] Keep-O	[A13 output] Address output retained [All other] Keep-O	Keep	Hi-Z	Keep
P309/A14	Hi-Z	[A14 output] Hi-Z [All other] Keep-O	[A14 output] Address output retained [All other] Keep-O	Keep	Hi-Z	Keep
P310/A15	Hi-Z	[A15 output] Hi-Z [All other] Keep-O	[A15 output] Address output retained [All other] Keep-O	Keep	Hi-Z	Keep
P311/CS2/RAS	Hi-Z	[CS2 output] Hi-Z [RAS output] Hi-Z [All other] Keep-O	[CS2 output] H [RAS output] SDSELF.SFEN = 0: H SDSELF.SFEN = 1: L [All other] Keep-O	Keep	Hi-Z	Keep
P312/CS3/CAS	Hi-Z	[CS3 output] Hi-Z [CAS output] Hi-Z [All other] Keep-O	[CS3 output] H [CAS output] SDSELF.SFEN = 0: H SDSELF.SFEN = 1: L [All other] Keep-O	Keep	Hi-Z	Keep
P313/A20	Hi-Z	[A20 output] Hi-Z [All other] Keep-O	[A20 output] Address output retained [All other] Keep-O	Keep	Hi-Z	Keep
P314/A21	Hi-Z	[A21 output] Hi-Z [All other] Keep-O	[A21 output] Address output retained [All other] Keep-O	Keep	Hi-Z	Keep
P315/A22	Hi-Z	[A22 output] Hi-Z [All other] Keep-O	[A22 output] Address output retained [All other] Keep-O	Keep	Hi-Z	Keep
P400/AGTIO1/ SCL0_A/IRQ0	Hi-Z	Keep-O*2		Keep	Hi-Z	Keep
P401/SDA0_A/ IRQ5-DS, P402/IRQ4-DS/ RTCIC0/ AGTIO0/AGTIO1, P403/RTCIC1/ AGTIO0/AGTIO1, P404/RTCIC2	Hi-Z	Keep-O*2		Keep-O*3	Hi-Z	Keep
P405, P406	Hi-Z	Keep-O		Keep	Hi-Z	Keep
P407/AGTIO0/ SDA0_B/USB_VBUS/ RTCOUT	Hi-Z	[RTCOUT selected] RTCOUT output [All other] Keep-O*2		Keep-O*3	Hi-Z	Keep
P408/SCL0_C/IRQ7, P409/IRQ6, P410/RXD0/IRQ5, P411/IRQ4	Hi-Z	Keep-O*2		Keep	Hi-Z	Keep
P412, P413	Hi-Z	Keep-O		Keep	Hi-Z	Keep
P414/IRQ9, P415/IRQ8	Hi-Z	Keep-O*2		Keep	Hi-Z	Keep
P500	Hi-Z	Keep-O		Keep	Hi-Z	Keep

Table 1.1 每个处理状态中的端口状态（3个，共6个）

端口名称	Reset	软件待机模式		深度软件待机模式	取消深度软件待机模式后（返回启动模式）	
		OPE = 0	OPE = 1		IOKEEP = 0	IOKEEP = 1*1
P305/A10/IRQ8	Hi-Z	[A10 output] Hi-Z [All other] Keep-O*2	[A10输出]地址输出保持 [所有其他]Keep-O*2	Keep	Hi-Z	Keep
P306/A11	Hi-Z	[A11 output] Hi-Z [All other] Keep-O	[A11输出]地址输出保留 [所有其他]Keep-O	Keep	Hi-Z	Keep
P307/A12	Hi-Z	[A12 output] Hi-Z [All other] Keep-O	[A12输出]地址输出保留 [所有其他]Keep-O	Keep	Hi-Z	Keep
P308/A13	Hi-Z	[A13 output] Hi-Z [All other] Keep-O	[A13输出]地址输出保留 [所有其他]Keep-O	Keep	Hi-Z	Keep
P309/A14	Hi-Z	[A14 output] Hi-Z [All other] Keep-O	[A14输出]地址输出保留 [所有其他]Keep-O	Keep	Hi-Z	Keep
P310/A15	Hi-Z	[A15 output] Hi-Z [All other] Keep-O	[A15输出]地址输出保留 [所有其他]Keep-O	Keep	Hi-Z	Keep
P311/CS2/RAS	Hi-Z	[CS2 output] Hi-Z [RAS output] Hi-Z [All other] Keep-O	[CS2 output] H [RAS output] SDSELF.SFEN = 0: H SDSELF.SFEN = 1: L [All other] Keep-O	Keep	Hi-Z	Keep
P312/CS3/CAS	Hi-Z	[CS3 output] Hi-Z [CAS output] Hi-Z [All other] Keep-O	[CS3 output] H [CAS output] SDSELF.SFEN = 0: H SDSELF.SFEN = 1: L [All other] Keep-O	Keep	Hi-Z	Keep
P313/A20	Hi-Z	[A20 output] Hi-Z [All other] Keep-O	[A20输出]地址输出保留 [所有其他]Keep-O	Keep	Hi-Z	Keep
P314/A21	Hi-Z	[A21 output] Hi-Z [All other] Keep-O	[A21输出]地址输出保留 [所有其他]Keep-O	Keep	Hi-Z	Keep
P315/A22	Hi-Z	[A22 output] Hi-Z [All other] Keep-O	[A22输出]地址输出保留 [所有其他]Keep-O	Keep	Hi-Z	Keep
P400/AGTIO1/ SCL0_A/IRQ0	Hi-Z	Keep-O*2		Keep	Hi-Z	Keep
P401/SDA0_A/ IRQ5-DS, P402/IRQ4-DS/ RTCIC0/ AGTIO0/AGTIO1, P403/RTCIC1/ AGTIO0/AGTIO1, P404/RTCIC2	Hi-Z	Keep-O*2		Keep-O*3	Hi-Z	Keep
P405, P406	Hi-Z	Keep-O		Keep	Hi-Z	Keep
P407/AGTIO0/ SDA0_B/USB_VBUS/ RTCOUT	Hi-Z	[RTCOUT selected] RTCOUT output [All other] Keep-O*2		Keep-O*3	Hi-Z	Keep
P408/SCL0_C/IRQ7, P409/IRQ6, P410/RXD0/IRQ5, P411/IRQ4	Hi-Z	Keep-O*2		Keep	Hi-Z	Keep
P412, P413	Hi-Z	Keep-O		Keep	Hi-Z	Keep
P414/IRQ9, P415/IRQ8	Hi-Z	Keep-O*2		Keep	Hi-Z	Keep
P500	Hi-Z	Keep-O		Keep	Hi-Z	Keep

Table 1.1 Port states in each processing state (4 of 6)

Port name	Reset	Software Standby mode		Deep Software Standby mode	After Deep Software Standby mode is canceled (return to startup mode)	
		OPE = 0	OPE = 1		IOKEEP = 0	IOKEEP = 1*1
P501/ USB_OVRCURA/ IRQ11, P502/ USB_OVRCURB/ IRQ12	Hi-Z	Keep-O*2		Keep	Hi-Z	Keep
P503	Hi-Z	Keep-O		Keep	Hi-Z	Keep
P504/ALE	Hi-Z	[ALE output] Hi-Z [All other] Keep-O	[ALE output] L [All other] Keep-O	Keep	Hi-Z	Keep
P505/IRQ14, P506/IRQ15	Hi-Z	Keep-O*2		Keep	Hi-Z	Keep
P507, P508	Hi-Z	Keep-O		Keep	Hi-Z	Keep
P511/IRQ15, P512/IRQ14	Hi-Z	Keep-O*2		Keep	Hi-Z	Keep
P513	Hi-Z	Keep-O		Keep	Hi-Z	Keep
P600/RD/CLKOUT	Hi-Z	[RD output] Hi-Z [CLKOUT selected] CLKOUT output [All other] Keep-O	[RD output] H [CLKOUT selected] CLKOUT output [All other] Keep-O	Keep	Hi-Z	Keep
P601/WR0/WR/DQM0	Hi-Z	[WR0/WR output] Hi-Z [DQM0 output] Hi-Z [All other] Keep-O	[WR0/WR output] H [DQM0 output] DQM0 output retained [All other] Keep-O	Keep	Hi-Z	Keep
P602/EBCLK/SDCLK	Hi-Z	[EBCLK output] H [SDCLK output] H [All other] Keep-O		Keep	Hi-Z	Keep
P603/D13[A13/D13]/ DQ13	Hi-Z	[D13 output] Hi-Z [DQ13 output] Hi-Z [All other] Keep-O		Keep	Hi-Z	Keep
P604/D12[A12/D12]/ DQ12	Hi-Z	[D12 output] Hi-Z [DQ12 output] Hi-Z [All other] Keep-O		Keep	Hi-Z	Keep
P605/D11[A11/D11]/ DQ11	Hi-Z	[D11 output] Hi-Z [DQ11 output] Hi-Z [All other] Keep-O		Keep	Hi-Z	Keep
P606, P607	Hi-Z	Keep-O		Keep	Hi-Z	Keep
P608/A00/BC0/DQM1	Hi-Z	[A00 output] Hi-Z [BC0 output] Hi-Z [DQM1 output] Hi-Z [All other] Keep-O	[A00 output] Address output retained [BC0 output] H [DQM1 output] DQM1 output retained [All other] Keep-O	Keep	Hi-Z	Keep
P609/CS1/CKE	Hi-Z	[CS1 output] Hi-Z [CKE output] Hi-Z [All other] Keep-O	[CS1 output] H [CKE output] SDSELF.SFEN = 0: H SDSELF.SFEN = 1: L [All other] Keep-O	Keep	Hi-Z	Keep
P610/CS0/WE	Hi-Z	[CS0 output] Hi-Z [WE output] Hi-Z [All other] Keep-O	[CS0 output] H [WE output] H [All other] Keep-O	Keep	Hi-Z	Keep

Table 1.1 每个处理状态中的端口状态（4个，共6个）

端口名称	Reset	软件待机模式		深度软件待机模式	取消深度软件待机模式后（返回启动模式）	
		OPE = 0	OPE = 1		IOKEEP = 0	IOKEEP = 1*1
P501/ USB_OVRCURA/ IRQ11, P502/ USB_OVRCURB/ IRQ12	Hi-Z	Keep-O*2		Keep	Hi-Z	Keep
P503	Hi-Z	Keep-O		Keep	Hi-Z	Keep
P504/ALE	Hi-Z	[ALE output] Hi-Z [All other] Keep-O	[ALE output] L [All other] Keep-O	Keep	Hi-Z	Keep
P505/IRQ14, P506/IRQ15	Hi-Z	Keep-O*2		Keep	Hi-Z	Keep
P507, P508	Hi-Z	Keep-O		Keep	Hi-Z	Keep
P511/IRQ15, P512/IRQ14	Hi-Z	Keep-O*2		Keep	Hi-Z	Keep
P513	Hi-Z	Keep-O		Keep	Hi-Z	Keep
P600/RD/CLKOUT	Hi-Z	[RD output] Hi-Z [CLKOUT selected] CLKOUT output [All other] Keep-O	[RD output] H [CLKOUT selected] CLKOUT output [All other] Keep-O	Keep	Hi-Z	Keep
P601/WR0/WR/DQM0	Hi-Z	[WR0/WR output] Hi-Z [DQM0 output] Hi-Z [All other] Keep-O	[WR0/WR输出]H[DQM0输出]DQM0输出保持[所有其他]Keep-O	Keep	Hi-Z	Keep
P602/EBCLK/SDCLK	Hi-Z	[EBCLK output] H [SDCLK output] H [All other] Keep-O		Keep	Hi-Z	Keep
P603/D13[A13/D13]/ DQ13	Hi-Z	[D13 output] Hi-Z [DQ13 output] Hi-Z [All other] Keep-O		Keep	Hi-Z	Keep
P604/D12[A12/D12]/ DQ12	Hi-Z	[D12 output] Hi-Z [DQ12 output] Hi-Z [All other] Keep-O		Keep	Hi-Z	Keep
P605/D11[A11/D11]/ DQ11	Hi-Z	[D11 output] Hi-Z [DQ11 output] Hi-Z [All other] Keep-O		Keep	Hi-Z	Keep
P606, P607	Hi-Z	Keep-O		Keep	Hi-Z	Keep
P608/A00/BC0/DQM1	Hi-Z	[A00 output] Hi-Z [BC0 output] Hi-Z [DQM1 output] Hi-Z [All other] Keep-O	[A00输出]地址输出保持[BC0输出]H[DQM1输出]DQM1输出保持[所有其他]Keep-O	Keep	Hi-Z	Keep
P609/CS1/CKE	Hi-Z	[CS1 output] Hi-Z [CKE output] Hi-Z [All other] Keep-O	[CS1 output] H [CKE output] SDSELF.SFEN = 0: H SDSELF.SFEN = 1: L [All other] Keep-O	Keep	Hi-Z	Keep
P610/CS0/WE	Hi-Z	[CS0 output] Hi-Z [WE output] Hi-Z [All other] Keep-O	[CS0 output] H [WE output] H [All other] Keep-O	Keep	Hi-Z	Keep

Table 1.1 Port states in each processing state (5 of 6)

Port name	Reset	Software Standby mode		Deep Software Standby mode	After Deep Software Standby mode is canceled (return to startup mode)	
		OPE = 0	OPE = 1		IOKEEP = 0	IOKEEP = 1*1
P611/SDCS/CLKOUT	Hi-Z	[SDCS output] Hi-Z [CLKOUT selected] CLKOUT output [All Other] Keep-O	[SDCS output] SDSELF.SFEN = 0: H SDSELF.SFEN = 1: L [CLKOUT selected] CLKOUT output [All other] Keep-O	Keep	Hi-Z	Keep
P612/D08[A08/D08]/ DQ08	Hi-Z	[D08 output] Hi-Z [DQ08 output] Hi-Z [All other] Keep-O		Keep	Hi-Z	Keep
P613/D09[A09/D09]/ DQ09	Hi-Z	[D09 output] Hi-Z [DQ09 output] Hi-Z [All other] Keep-O		Keep	Hi-Z	Keep
P614/D10[A10/D10]/ DQ10	Hi-Z	[D10 output] Hi-Z [DQ10 output] Hi-Z [All other] Keep-O		Keep	Hi-Z	Keep
P615	Hi-Z	Keep-O		Keep	Hi-Z	Keep
P700 to P702	Hi-Z	Keep-O		Keep	Hi-Z	Keep
P703/VCOUT	Hi-Z	[ACMPHS selected] VCOUT output [All other] Keep-O		Keep	Hi-Z	Keep
P704	Hi-Z	Keep-O		Keep	Hi-Z	Keep
P705/AGTIO0	Hi-Z	Keep-O*2		Keep	Hi-Z	Keep
P706/ USBHS_OVRCURB/ IRQ7, P707/ USBHS_OVRCURA/ IRQ8	Hi-Z	Keep-O*2		Keep-O*3	Hi-Z	Keep
P708/IRQ11, P709/IRQ10	Hi-Z	Keep-O*2		Keep	Hi-Z	Keep
P710 to P713	Hi-Z	Keep-O		Keep	Hi-Z	Keep
P800/D14[A14/D14]/ DQ14	Hi-Z	[D14 output] Hi-Z [DQ14 output] Hi-Z [All other] Keep-O		Keep	Hi-Z	Keep
P801/D15[A15/D15]/ DQ15	Hi-Z	[D15 output] Hi-Z [DQ15 output] Hi-Z [All other] Keep-O		Keep	Hi-Z	Keep
P802 to P806	Hi-Z	Keep-O		Keep	Hi-Z	Keep
P900/A23	Hi-Z	[A23 output] Hi-Z [All other] Keep-O	[A23 output] Address output retained [All other] Keep-O	Keep	Hi-Z	Keep
P901/AGTIO1	Hi-Z	Keep-O*2		Keep	Hi-Z	Keep
P905/CS4	Hi-Z	[CS4 output] Hi-Z [All other] Keep-O	[CS4 output] H [All other] Keep-O	Keep	Hi-Z	Keep
P906/CS5	Hi-Z	[CS5 output] Hi-Z [All other] Keep-O	[CS5 output] H [All other] Keep-O	Keep	Hi-Z	Keep
P907/CS6	Hi-Z	[CS6 output] Hi-Z [All other] Keep-O	[CS6 output] H [All other] Keep-O	Keep	Hi-Z	Keep

Table 1.1 每个处理状态中的端口状态（5个，共6个）

端口名称	Reset	软件待机模式		深度软件待机模式	取消深度软件待机模式后（返回启动模式）	
		OPE = 0	OPE = 1		IOKEEP = 0	IOKEEP = 1*1
P611/SDCS/CLKOUT	Hi-Z	[SDCS output] Hi-Z [CLKOUT selected] CLKOUT output [All Other] Keep-O	[SDCS output] SDSELF.SFEN = 0: H SDSELF.SFEN = 1: L [CLKOUT selected] CLKOUT output [All other] Keep-O	Keep	Hi-Z	Keep
P612/D08[A08/D08]/ DQ08	Hi-Z	[D08 output] Hi-Z [DQ08 output] Hi-Z [All other] Keep-O		Keep	Hi-Z	Keep
P613/D09[A09/D09]/ DQ09	Hi-Z	[D09 output] Hi-Z [DQ09 output] Hi-Z [All other] Keep-O		Keep	Hi-Z	Keep
P614/D10[A10/D10]/ DQ10	Hi-Z	[D10 output] Hi-Z [DQ10 output] Hi-Z [All other] Keep-O		Keep	Hi-Z	Keep
P615	Hi-Z	Keep-O		Keep	Hi-Z	Keep
P700 to P702	Hi-Z	Keep-O		Keep	Hi-Z	Keep
P703/VCOUT	Hi-Z	[ACMPHS selected] VCOUT output [All other] Keep-O		Keep	Hi-Z	Keep
P704	Hi-Z	Keep-O		Keep	Hi-Z	Keep
P705/AGTIO0	Hi-Z	Keep-O*2		Keep	Hi-Z	Keep
P706/ USBHS_OVRCURB/ IRQ7, P707/ USBHS_OVRCURA/ IRQ8	Hi-Z	Keep-O*2		Keep-O*3	Hi-Z	Keep
P708/IRQ11, P709/IRQ10	Hi-Z	Keep-O*2		Keep	Hi-Z	Keep
P710 to P713	Hi-Z	Keep-O		Keep	Hi-Z	Keep
P800/D14[A14/D14]/ DQ14	Hi-Z	[D14 output] Hi-Z [DQ14 output] Hi-Z [All other] Keep-O		Keep	Hi-Z	Keep
P801/D15[A15/D15]/ DQ15	Hi-Z	[D15 output] Hi-Z [DQ15 output] Hi-Z [All other] Keep-O		Keep	Hi-Z	Keep
P802 to P806	Hi-Z	Keep-O		Keep	Hi-Z	Keep
P900/A23	Hi-Z	[A23 output] Hi-Z [All other] Keep-O	[A23输出]地址输出保留 [所有其他]Keep-O	Keep	Hi-Z	Keep
P901/AGTIO1	Hi-Z	Keep-O*2		Keep	Hi-Z	Keep
P905/CS4	Hi-Z	[CS4 output] Hi-Z [All other] Keep-O	[CS4 output] H [All other] Keep-O	Keep	Hi-Z	Keep
P906/CS5	Hi-Z	[CS5 output] Hi-Z [All other] Keep-O	[CS5 output] H [All other] Keep-O	Keep	Hi-Z	Keep
P907/CS6	Hi-Z	[CS6 output] Hi-Z [All other] Keep-O	[CS6 output] H [All other] Keep-O	Keep	Hi-Z	Keep

Table 1.1 Port states in each processing state (6 of 6)

Port name	Reset	Software Standby mode		Deep Software Standby mode	After Deep Software Standby mode is canceled (return to startup mode)	
		OPE = 0	OPE = 1		IOKEEP = 0	IOKEEP = 1*1
P908/CS7	Hi-Z	[CS7 output] Hi-Z [All other] Keep-O	[CS7 output] H [All other] Keep-O	Keep	Hi-Z	Keep
PA00, PA01	Hi-Z	Keep-O		Keep	Hi-Z	Keep
PA08 to PA10	Hi-Z	Keep-O		Keep	Hi-Z	Keep
PB00	Hi-Z	Keep-O		Keep	Hi-Z	Keep
PB01/USBHS_VBUS	Hi-Z	Keep-O*2		Keep-O*3	Hi-Z	Keep
USB_DP	Hi-Z	Keep-O*4		Hi-Z*3	Hi-Z	
USB_DM	Hi-Z	Keep-O*4		Hi-Z*3	Hi-Z	
USBHS_DP	Hi-Z	Keep-O*4		Hi-Z*5	Hi-Z	
USBHS_DM	Hi-Z	Keep-O*4		Hi-Z*5	Hi-Z	

H: High-level
L: Low-level
Hi-Z: High-impedance
Keep-O: Output pins retain their previous values. Input pins go to high-impedance.
Keep: Pin states are retained during periods in Software Standby mode.

Note 1. Retains the I/O port state until the DPSBYCR.IOKEEP bit is cleared to 0.
Note 2. Input is enabled if the pin is specified as the Software Standby canceling source while it is used as an external interrupt pin.
Note 3. Input is enabled if the pin is specified as the Deep Software Standby canceling source.
Note 4. Input is enabled while the pin is used as an input pin.
Note 5. For host operation, set the USBHS.SYSCFG.DRPD bit to 1 to enable the USBHS_DP and USBHS_DM pull-down resistors.
For device operation, set the USBHS.SYSCFG.DPRPU bit to 1 to enable the DP pull-up resistor.

Table 1.1 每个处理状态中的端口状态（6个中的6个）

端口名称	Reset	软件待机模式		深度软件待机模式	取消深度软件待机模式后（返回启动模式）	
		OPE = 0	OPE = 1		IOKEEP = 0	IOKEEP = 1*1
P908/CS7	Hi-Z	[CS7 output] Hi-Z [All other] Keep-O	[CS7 output] H [All other] Keep-O	Keep	Hi-Z	Keep
PA00, PA01	Hi-Z	Keep-O		Keep	Hi-Z	Keep
PA08 to PA10	Hi-Z	Keep-O		Keep	Hi-Z	Keep
PB00	Hi-Z	Keep-O		Keep	Hi-Z	Keep
PB01/USBHS_VBUS	Hi-Z	Keep-O*2		Keep-O*3	Hi-Z	Keep
USB_DP	Hi-Z	Keep-O*4		Hi-Z*3	Hi-Z	
USB_DM	Hi-Z	Keep-O*4		Hi-Z*3	Hi-Z	
USBHS_DP	Hi-Z	Keep-O*4		Hi-Z*5	Hi-Z	
USBHS_DM	Hi-Z	Keep-O*4		Hi-Z*5	Hi-Z	

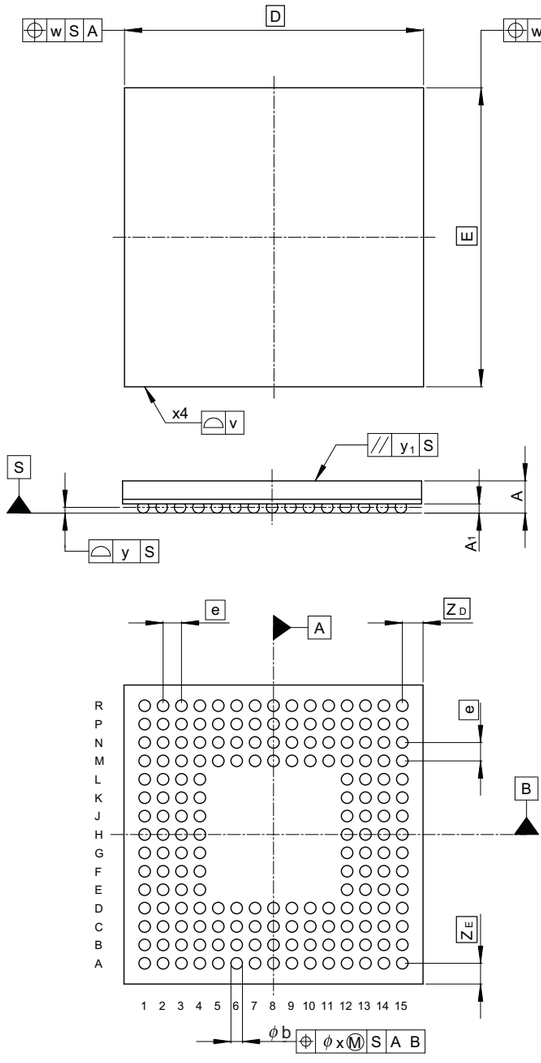
H: High-level
L: Low-level
Hi-Z: High-impedance
Keep-O：输出引脚保留其先前的值。输入引脚变为高阻抗。
保持：在软件待机模式期间保持引脚状态。

Note 1. 保持IO端口状态，直到DPSBYCR.IOKEEP位被清除为0。
Note 2. 如果引脚被指定为软件待机取消源，同时它被用作外部中断引脚，则输入被启用。
Note 3. 如果将引脚指定为深度软件待机取消源，则启用输入。
Note 4. 当引脚用作输入引脚时，输入被启用。
Note 5. 对于主机操作，将USBHS.SYSCFG.DRPD位设置为1以启用USBHS_DP和USBHS_DM下拉电阻。
对于设备操作，将USBHS.SYSCFG.DPRPU位设置为1以启用DP上拉电阻。

Appendix 2.Package Dimensions

For information on the latest version of the package dimensions or mountings, go to “Packages” on the Renesas Electronics Corporation website.

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.)
P-LFBGA176-13x13-0.80	PLBG0176GE-A	176FHS-A	0.45 g



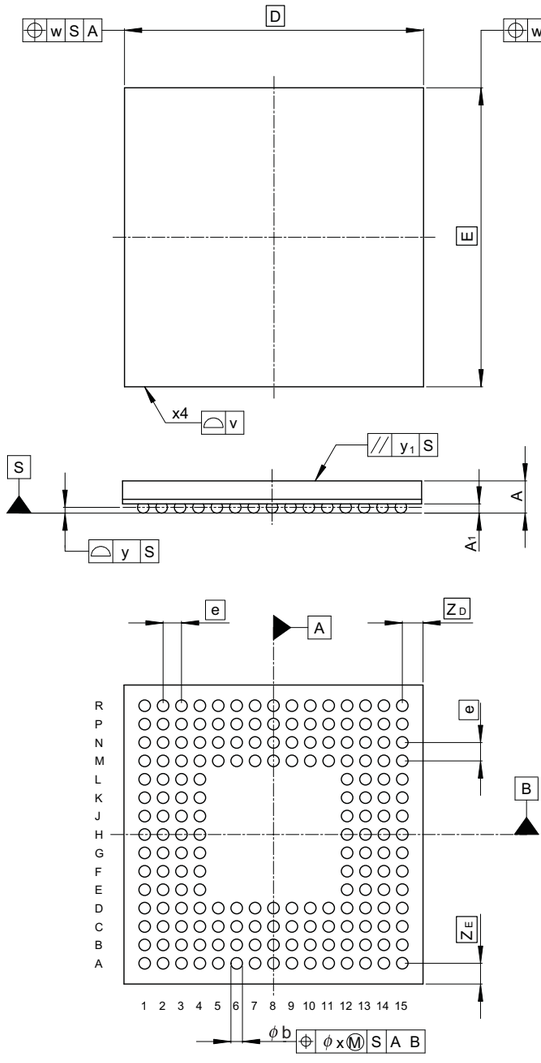
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	——	13.0	——
E	——	13.0	——
v	——	——	0.15
w	——	——	0.20
A	——	——	1.40
A_1	0.35	0.40	0.45
e	——	0.80	——
b	0.45	0.50	0.55
x	——	——	0.08
y	——	——	0.10
y_1	——	——	0.2
S_D	——	——	——
S_E	——	——	——
Z_D	——	0.90	——
Z_E	——	0.90	——

Figure 2.1 176-pin BGA

附录2.包装尺寸

有关最新版本的封装尺寸或安装信息，请访问Renesas上的“封装”电子公司网站。

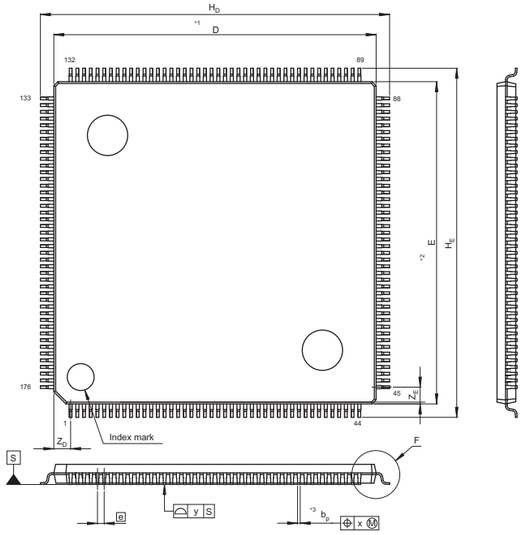
JEITA包装代码	RENESAS Code	以前的代码	MASS (TYP.)
P-LFBGA176-13x13-0.80	PLBG0176GE-A	176FHS-A	0.45 g

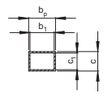


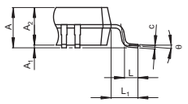
Reference Symbol	以毫米为单位的尺寸		
	Min	Nom	Max
D	——	13.0	——
E	——	13.0	——
v	——	——	0.15
w	——	——	0.20
A	——	——	1.40
A_1	0.35	0.40	0.45
e	——	0.80	——
b	0.45	0.50	0.55
x	——	——	0.08
y	——	——	0.10
y_1	——	——	0.2
S_D	——	——	——
S_E	——	——	——
Z_D	——	0.90	——
Z_E	——	0.90	——

Figure 2.1 176-pin BGA

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP176-24x24-0.50	PLQP0176KB-A	176P6Q-A/FP-176E/FP-176EV	1.8g





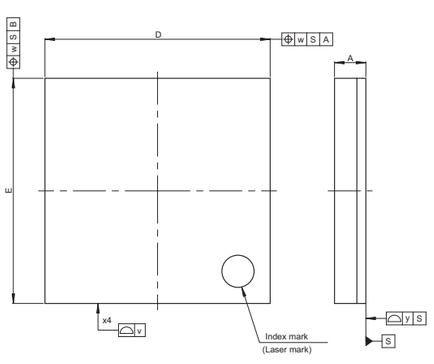


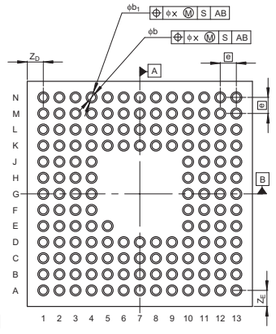
NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	23.9	24.0	24.1
E	23.9	24.0	24.1
A_2	—	1.4	—
H_D	25.8	26.0	26.2
H_E	25.8	26.0	26.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.10
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure 2.2 176-pin LQFP

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-TFLGA145-7x7-0.50	PTLG0145KA-A	145F0G	0.1g

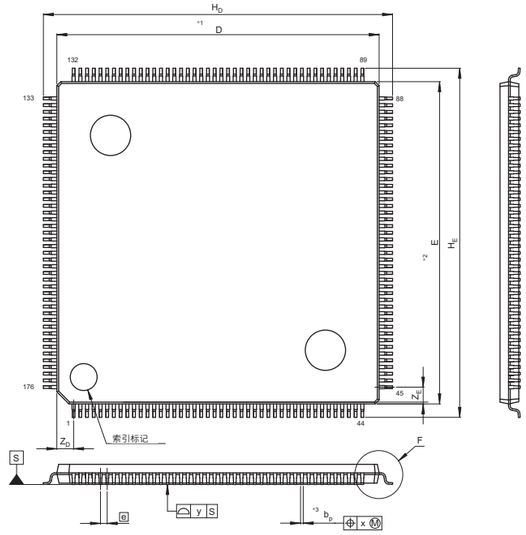


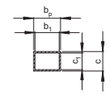


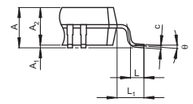
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	7.0	—
E	—	7.0	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.05
e	—	0.5	—
b	0.21	0.25	0.29
b_1	0.29	0.34	0.39
x	—	—	0.08
y	—	—	0.08
Z_D	—	0.5	—
Z_E	—	0.5	—

Figure 2.3 145-pin LGA

JEITA包装代码	RENESAS Code	以前的代码	MASS[Typ.]
P-LFQFP176-24x24-0.50	PLQP0176KB-A	176P6Q-A/FP-176E/FP-176EV	1.8g





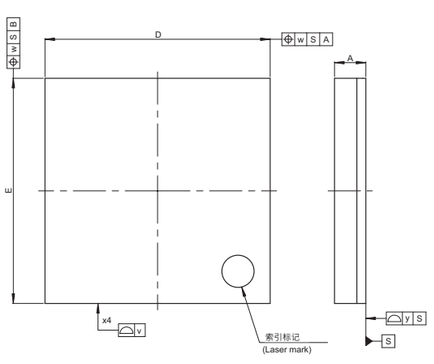


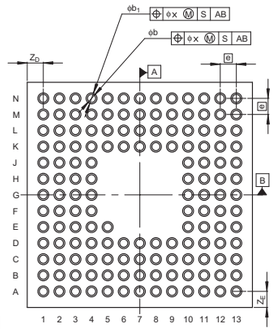
NOTE)
1.尺寸"*1"和"*2"
不包括模具溢料。
2.尺寸"*3"不
包括修剪偏移。

参考符号	以毫米为单位的尺寸		
	Min	Nom	Max
D	23.9	24.0	24.1
E	23.9	24.0	24.1
A_2	—	1.4	—
H_D	25.8	26.0	26.2
H_E	25.8	26.0	26.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.10
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure 2.2 176-pin LQFP

JEITA包装代码	RENESAS Code	以前的代码	MASS[Typ.]
P-TFLGA145-7x7-0.50	PTLG0145KA-A	145F0G	0.1g



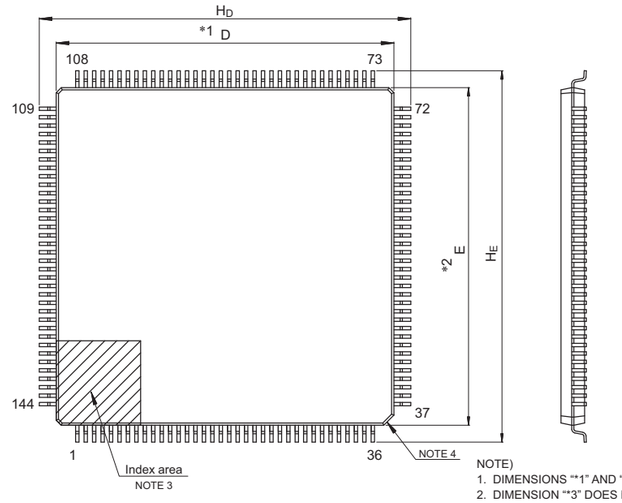


参考符号	以毫米为单位的尺寸		
	Min	Nom	Max
D	—	7.0	—
E	—	7.0	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.05
e	—	0.5	—
b	0.21	0.25	0.29
b_1	0.29	0.34	0.39
x	—	—	0.08
y	—	—	0.08
Z_D	—	0.5	—
Z_E	—	0.5	—

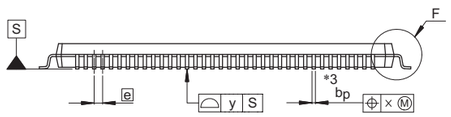
Figure 2.3 145-pin LGA

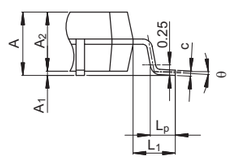
JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP144-20x20-0.50	PLQP0144KA-B	—	1.2

Unit: mm



NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.





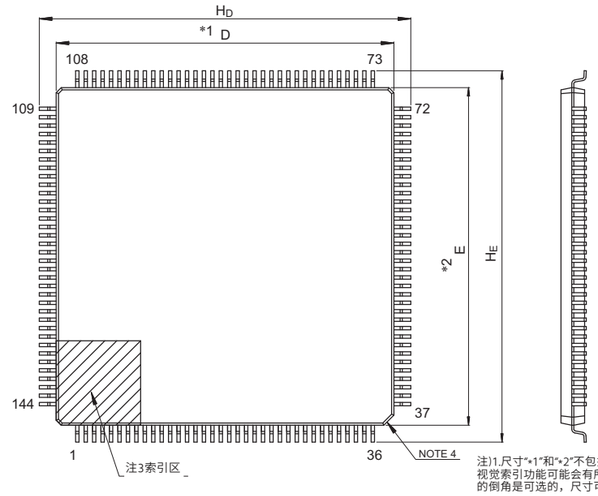
Detail F

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	19.9	20.0	20.1
E	19.9	20.0	20.1
A_2	—	1.4	—
H_D	21.8	22.0	22.2
H_E	21.8	22.0	22.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.17	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.10
L_p	0.45	0.6	0.75
L_1	—	1.0	—

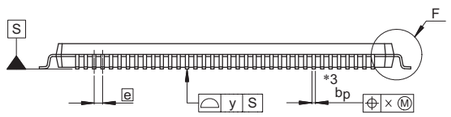
Figure 2.4 144-pin LQFP

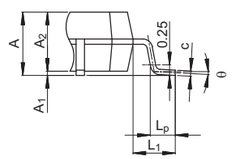
JEITA包装代码	RENESAS Code	以前的代码	MASS (Typ) [g]
P-LFQFP144-20x20-0.50	PLQP0144KA-B	—	1.2

Unit: mm



注)1.尺寸"*1"和"*2"不包括毛边。2.尺寸"*3"不包括微调偏移。3.PIN1视觉索引功能可能会有所不同，但必须位于阴影区域内。4.拐角处的倒角是可选的，尺寸可能会有所不同。





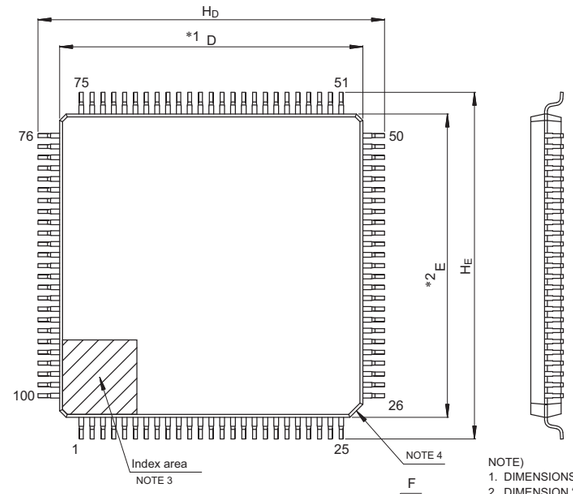
Detail F

参考符号	尺寸以毫米为单位		
	Min	Nom	Max
D	19.9	20.0	20.1
E	19.9	20.0	20.1
A_2	—	1.4	—
H_D	21.8	22.0	22.2
H_E	21.8	22.0	22.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.17	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.10
L_p	0.45	0.6	0.75
L_1	—	1.0	—

Figure 2.4 144-pin LQFP

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP100-14x14-0.50	PLQP0100KB-B	—	0.6

Unit: mm



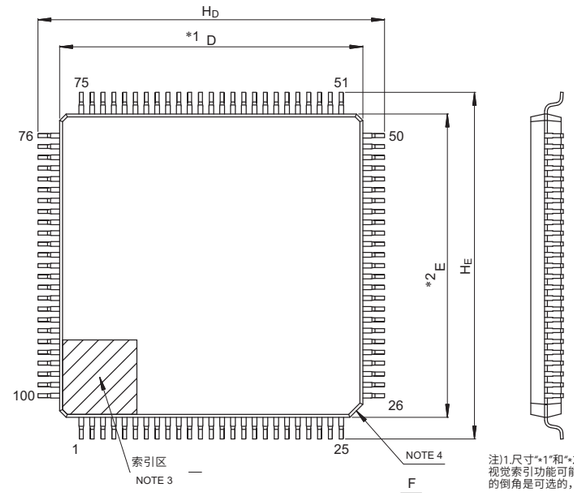
NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

Figure 2.5 100-pin LQFP

JEITA包装代码	RENESAS Code	以前的代码	MASS (Typ) [g]
P-LFQFP100-14x14-0.50	PLQP0100KB-B	—	0.6

Unit: mm



注)1.尺寸"*1"和"*2"不包括毛边。2.尺寸"*3"不包括微调偏移。3.PIN1视觉索引功能可能会有所不同，但必须位于阴影区域内。4.拐角处的倒角是可选的，尺寸可能会有所不同。

参考符号	尺寸以毫米为单位		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	—	0.15
b_p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L_p	0.45	0.6	0.75
L_1	—	1.0	—

Figure 2.5 100-pin LQFP

Appendix 3. I/O Registers

This appendix describes I/O register addresses, access cycles, and reset values by function.

3.1 Peripheral Base Addresses

This section provides the base addresses for peripherals described in this manual.

Table 3.1 shows the name, description, and the base address of each peripheral.

Table 3.1 Peripheral base address (1 of 3)

Name	Description	Base address
MMPU	Bus Master MPU	0x40000000
SMPU	Bus Slave MPU	0x40000C00
SPMON	CPU Stack Pointer Monitor	0x40000D00
MMF	Memory Mirror Function	0x40001000
SRAM	SRAM Control	0x40002000
BUS	Bus Control	0x40003000
DMAC0	Direct Memory Access Controller 0	0x40005000
DMAC1	Direct Memory Access Controller 1	0x40005040
DMAC2	Direct Memory Access Controller 2	0x40005080
DMAC3	Direct Memory Access Controller 3	0x400050C0
DMAC4	Direct Memory Access Controller 4	0x40005100
DMAC5	Direct Memory Access Controller 5	0x40005140
DMAC6	Direct Memory Access Controller 6	0x40005180
DMAC7	Direct Memory Access Controller 7	0x400051C0
DMA	DMAC Module Activation	0x40005200
DTC	Data Transfer Controller	0x40005400
ICU	Interrupt Controller	0x40006000
DBG	Debug Function	0x4001B000
FCACHE	Flash Cache	0x4001C000
SYSTEM	System Control	0x4001E000
PORT0	Port 0 Control Registers	0x40040000
PORT1	Port 1 Control Registers	0x40040020
PORT2	Port 2 Control Registers	0x40040040
PORT3	Port 3 Control Registers	0x40040060
PORT4	Port 4 Control Registers	0x40040080
PORT5	Port 5 Control Registers	0x400400A0
PORT6	Port 6 Control Registers	0x400400C0
PORT7	Port 7 Control Registers	0x400400E0
PORT8	Port 8 Control Registers	0x40040100
PORT9	Port 9 Control Registers	0x40040120
PORTA	Port A Control Registers	0x40040140
PORTB	Port B Control Registers	0x40040160
PFS	Pmn Pin Function Control Register	0x40040800
PMISC	Miscellaneous Port Control Register	0x40040D00
ELC	Event Link Controller	0x40041000
POEG	Port Output Enable Module for GPT	0x40042000
RTC	Realtime Clock	0x40044000
WDT	Watchdog Timer	0x40044200

附录3.IO寄存器

本附录按功能描述了IO寄存器地址、访问周期和复位值。

3.1 外设基地址

本节提供本手册中描述的外设的基地址。

表3.1显示了每个外设的名称、描述和基地址。

Table 3.1 外设基地址(1of3)

Name	Description	基址
MMPU	总线主控MPU	0x40000000
SMPU	总线从MPU	0x40000C00
SPMON	CPU堆栈指针监视器	0x40000D00
MMF	内存镜像功能	0x40001000
SRAM	SRAM Control	0x40002000
BUS	总线控制	0x40003000
DMAC0	直接内存访问控制器0	0x40005000
DMAC1	直接内存访问控制器1	0x40005040
DMAC2	直接内存访问控制器2	0x40005080
DMAC3	直接内存访问控制器3	0x400050C0
DMAC4	直接内存访问控制器4	0x40005100
DMAC5	直接内存访问控制器5	0x40005140
DMAC6	直接内存访问控制器6	0x40005180
DMAC7	直接内存访问控制器7	0x400051C0
DMA	DMAC模块激活	0x40005200
DTC	数据传输控制器	0x40005400
ICU	中断控制器	0x40006000
DBG	调试功能	0x4001B000
FCACHE	闪存缓存	0x4001C000
SYSTEM	系统控制	0x4001E000
PORT0	端口0控制寄存器	0x40040000
PORT1	端口1控制寄存器	0x40040020
PORT2	端口2控制寄存器	0x40040040
PORT3	端口3控制寄存器	0x40040060
PORT4	端口4控制寄存器	0x40040080
PORT5	端口5控制寄存器	0x400400A0
PORT6	端口6控制寄存器	0x400400C0
PORT7	端口7控制寄存器	0x400400E0
PORT8	端口8控制寄存器	0x40040100
PORT9	端口9控制寄存器	0x40040120
PORTA	端口A控制寄存器	0x40040140
PORTB	端口B控制寄存器	0x40040160
PFS	Pmn引脚功能控制寄存器	0x40040800
PMISC	杂项端口控制寄存器	0x40040D00
ELC	事件链接控制器	0x40041000
POEG	GPT端口输出使能模块	0x40042000
RTC	实时时钟	0x40044000
WDT	看门狗定时器	0x40044200

Table 3.1 Peripheral base address (2 of 3)

Name	Description	Base address
IWDT	Independent Watchdog Timer	0x40044400
CAC	Clock Frequency Accuracy Measurement Circuit	0x40044600
MSTP	Module Stop Control B,C,D	0x40047000
SRCRAM	Sampling Rate Converter RAM	0x40048000
SRC	Sampling Rate Converter	0x4004DFF0
SSIE0	Serial Sound Interface Enhanced (SSIE)	0x4004E000
SSIE1	Serial Sound Interface Enhanced (SSIE)	0x4004E100
CAN0	CAN0 Module	0x40050000
CAN1	CAN1 Module	0x40051000
IIC0	Inter-Integrated Circuit 0	0x40053000
IIC1	Inter-Integrated Circuit 1	0x40053100
IIC2	Inter-Integrated Circuit 2	0x40053200
DOC	Data Operation Circuit	0x40054100
ADC120	12bit A/D Converter 0	0x4005C000
ADC121	12bit A/D Converter 1	0x4005C200
TSN	Temperature Sensor	0x4005D000
DAC12	12-bit D/A converter	0x4005E000
USBHS	USB 2.0 High-Speed Module	0x40060000
SDHI0	SD Host Interface 0	0x40062000
SDHI1	SD Host Interface 1	0x40062400
EDMAC0	DMA Controller for the Ethernet Controller Channel 0	0x40064000
ETHERC0	Ethernet Controller Channel 0	0x40064100
PTPEDMAC	DMA Controller for EPTPC	0x40064400
EPTPC_CFG	EPTPC Configuration	0x40064500
EPTPC	PTP Module for the Ethernet Controller	0x40065000
EPTPC0	PTP Module 0 for the Ethernet Controller	0x40065800
SCI0	Serial Communication Interface 0	0x40070000
SCI1	Serial Communication Interface 1	0x40070020
SCI2	Serial Communication Interface 2	0x40070040
SCI3	Serial Communication Interface 3	0x40070060
SCI4	Serial Communication Interface 4	0x40070080
SCI5	Serial Communication Interface 5	0x400700A0
SCI6	Serial Communication Interface 6	0x400700C0
SCI7	Serial Communication Interface 7	0x400700E0
SCI8	Serial Communication Interface 8	0x40070100
SCI9	Serial Communication Interface 9	0x40070120
IRDA	Infrared Data Association	0x40070F00
SPI0	Serial Peripheral Interface 0	0x40072000
SPI1	Serial Peripheral Interface 1	0x40072100
CRC	CRC Calculator	0x40074000
GPT32EH0	General PWM Timer 0 (32-bit Enhanced High Resolution)	0x40078000
GPT32EH1	General PWM Timer 1 (32-bit Enhanced High Resolution)	0x40078100
GPT32EH2	General PWM Timer 2 (32-bit Enhanced High Resolution)	0x40078200
GPT32EH3	General PWM Timer 3 (32-bit Enhanced High Resolution)	0x40078300
GPT32E4	General PWM Timer 4 (32-bit Enhanced)	0x40078400

Table 3.1 外设基地址（2个，共3个）

Name	Description	基址
IWDT	独立看门狗定时器	0x40044400
CAC	时钟频率精度测量电路	0x40044600
MSTP	模块停止控制B C D	0x40047000
SRCRAM	采样率转换器RAM	0x40048000
SRC	采样率转换器	0x4004DFF0
SSIE0	串行声音接口增强(SSIE)	0x4004E000
SSIE1	串行声音接口增强(SSIE)	0x4004E100
CAN0	CAN0 Module	0x40050000
CAN1	CAN1 Module	0x40051000
IIC0	Inter-Integrated Circuit 0	0x40053000
IIC1	Inter-Integrated Circuit 1	0x40053100
IIC2	Inter-Integrated Circuit 2	0x40053200
DOC	数据运算电路	0x40054100
ADC120	12bit A/D Converter 0	0x4005C000
ADC121	12bit A/D Converter 1	0x4005C200
TSN	温度感应器	0x4005D000
DAC12	12-bit D/A converter	0x4005E000
USBHS	USB2.0高速模块	0x40060000
SDHI0	SD主机接口0	0x40062000
SDHI1	SD主机接口1	0x40062400
EDMAC0	以太网控制器通道0的DMA控制器	0x40064000
ETHERC0	以太网控制器通道0	0x40064100
PTPEDMAC	EPTPC的DMA控制器	0x40064400
EPTPC_CFG	EPTPC Configuration	0x40064500
EPTPC	以太网控制器的PTP模块	0x40065000
EPTPC0	以太网控制器的PTP模块0	0x40065800
SCI0	串行通讯接口0	0x40070000
SCI1	串行通讯接口1	0x40070020
SCI2	串行通讯接口2	0x40070040
SCI3	串行通讯接口3	0x40070060
SCI4	串行通讯接口4	0x40070080
SCI5	串行通讯接口5	0x400700A0
SCI6	串行通讯接口6	0x400700C0
SCI7	串行通讯接口7	0x400700E0
SCI8	串行通讯接口8	0x40070100
SCI9	串行通讯接口9	0x40070120
IRDA	红外数据协会	0x40070F00
SPI0	串行外设接口0	0x40072000
SPI1	串行外设接口1	0x40072100
CRC	CRC Calculator	0x40074000
GPT32EH0	通用PWM定时器0（32位增强型高分辨率）	0x40078000
GPT32EH1	通用PWM定时器1（32位增强型高分辨率）	0x40078100
GPT32EH2	通用PWM定时器2（32位增强型高分辨率）	0x40078200
GPT32EH3	通用PWM定时器3（32位增强型高分辨率）	0x40078300
GPT32E4	通用PWM定时器4（32位增强型）	0x40078400

Table 3.1 Peripheral base address (3 of 3)

Name	Description	Base address
GPT32E5	General PWM Timer 5 (32-bit Enhanced)	0x40078500
GPT32E6	General PWM Timer 6 (32-bit Enhanced)	0x40078600
GPT32E7	General PWM Timer 7 (32-bit Enhanced)	0x40078700
GPT328	General PWM Timer 8 (32-bit)	0x40078800
GPT329	General PWM Timer 9 (32-bit)	0x40078900
GPT3210	General PWM Timer 10 (32-bit)	0x40078A00
GPT3211	General PWM Timer 11 (32-bit)	0x40078B00
GPT3212	General PWM Timer 12 (32-bit)	0x40078C00
GPT3213	General PWM Timer 13 (32-bit)	0x40078D00
GPT_OPS	Output Phase Switching Controller	0x40078FF0
GPT_ODC	PWM Delay Generation Circuit	0x4007B000
KINT	Key Interrupt Function	0x40080000
CTSU	Capacitive Touch Sensing Unit	0x40081000
AGT0	Asynchronous General purpose Timer 0	0x40084000
AGT1	Asynchronous General purpose Timer 1	0x40084100
ACMPHS0	High-Speed Analog Comparator 0	0x40085000
ACMPHS1	High-Speed Analog Comparator 1	0x40085100
ACMPHS2	High-Speed Analog Comparator 2	0x40085200
ACMPHS3	High-Speed Analog Comparator 3	0x40085300
ACMPHS4	High-Speed Analog Comparator 4	0x40085400
ACMPHS5	High-Speed Analog Comparator 5	0x40085500
USBFS	USB 2.0 FS Module	0x40090000
PDC	Parallel Data Capture Unit	0x40094000
GLCDC	Graphics LCD Controller	0x400E0000
DRW	2D Drawing Engine	0x400E4000
JPEG	JPEG Codec	0x400E6000
QSPI	Quad-SPI	0x64000000

Name = Peripheral name
Description = Peripheral functionality
Base address = Lowest reserved address or address used by the peripheral

3.2 Access Cycles

This section provides access cycle information for the I/O registers described in this manual.

The following information applies to Table 3.2 and Table 3.3:

- Registers are grouped by associated module
- The number of access cycles indicates the number of cycles based on the specified reference clock
- In the internal I/O area, reserved addresses that are not allocated to registers must not be accessed, otherwise operations cannot be guaranteed
- The number of I/O access cycles depends on bus cycles of the internal peripheral bus, divided clock synchronization cycles, and wait cycles of each module. Divided clock synchronization cycles differ depending on the frequency ratio between ICLK and PCLK.
- When the frequency of ICLK is equal to that of PCLK, the number of divided clock synchronization cycles is always constant.
- When the frequency of ICLK is greater than that of PCLK, at least 1 PCLK cycle is added to the number of divided clock synchronization cycles.

Table 3.1 外设基地址(3of3)

Name	Description	基址
GPT32E5	通用PWM定时器5（32位增强型）	0x40078500
GPT32E6	通用PWM定时器6（32位增强型）	0x40078600
GPT32E7	通用PWM定时器7（32位增强型）	0x40078700
GPT328	通用PWM定时器8（32位）	0x40078800
GPT329	通用PWM定时器9（32位）	0x40078900
GPT3210	通用PWM定时器10（32位）	0x40078A00
GPT3211	通用PWM定时器11（32位）	0x40078B00
GPT3212	通用PWM定时器12（32位）	0x40078C00
GPT3213	通用PWM定时器13（32位）	0x40078D00
GPT_OPS	输出相位切换控制器	0x40078FF0
GPT_ODC	PWM延迟产生电路	0x4007B000
KINT	按键中断功能	0x40080000
CTSU	电容式触控感应单元	0x40081000
AGT0	异步通用定时器0	0x40084000
AGT1	异步通用定时器1	0x40084100
ACMPHS0	高速模拟比较器0	0x40085000
ACMPHS1	高速模拟比较器1	0x40085100
ACMPHS2	高速模拟比较器2	0x40085200
ACMPHS3	高速模拟比较器3	0x40085300
ACMPHS4	高速模拟比较器4	0x40085400
ACMPHS5	高速模拟比较器5	0x40085500
USBFS	USB2.0FS模块	0x40090000
PDC	并行数据采集单元	0x40094000
GLCDC	图形液晶控制器	0x400E0000
DRW	2D绘图引擎	0x400E4000
JPEG	JPEG编解码器	0x400E6000
QSPI	Quad-SPI	0x64000000

名称=外设名称
描述=外围功能
基地址=外设使用的最低保留地址或地址

3.2 访问周期

本节提供本手册中描述的IO寄存器的访问周期信息。

以下信息适用于表3.2和表3.3：

- 寄存器按相关模块分组
- 访问周期数表示基于指定参考时钟的周期数
- 在内部IO区，不能访问未分配给寄存器的保留地址，否则无法保证操作
- IO访问周期数取决于内部外设总线的总线周期、分频时钟同步周期和每个模块的等待周期。分频时钟同步周期取决于ICLK和PCLK之间的频率比。
- 当ICLK的频率等于PCLK的频率时，分频时钟同步周期的数量始终是恒定的。
- 当ICLK的频率大于PCLK的频率时，分频时钟同步周期数至少增加1个PCLK周期。

Note: This applies to the number of cycles when access from the CPU does not conflict with the instruction fetching to the external memory or bus access from other bus masters such as DTC or DMAC.

Table 3.2 Access cycles (1 of 2)

Peripherals	Address		Number of access cycles				Cycle Unit	Related function
			ICLK = PCLK		ICLK > PCLK*1			
	From	To	Read	Write	Read	Write		
MMPU, SMPU, SPMON, MMF, SRAM, BUS, DMACn, DMA, DTC, ICU, DBG, FCACHE	4000 0000h	4001 CFFFh	4				ICLK	Memory Protection Unit, Memory Mirror Function, SRAM, Buses, DMA Controller, Data Transfer Controller, Interrupt Controller, CPU, Flash Memory
SYSTEM	4001 E000h	4001 E3FFh	5				ICLK	Low Power Modes, Resets, Low Voltage Detection, Clock Generation Circuit, Register Write Protection
SYSTEM	4001 E400h	4001 E6FFh	9		5 to 8		PCLKB	Low Power Modes, Resets, Low Voltage Detection, Battery Backup Function
PORTn, PFS, PMISC, ELC, POEG, RTC, WDT, IWDT, CAC, MSTP	4004 0000h	4004 7FFFh	3		2 to 3		PCLKB	I/O Ports, Event Link Controller, Port Output Enable for GPT, Realtime Clock, Watchdog Timer, Independent Watchdog Timer, Clock Frequency Accuracy Measurement Circuit, Module Stop Control
SRCRAM	4004 8000h	4004 DFEFh	4	3	3 to 4	2 to 3	PCLKB	Sampling Rate Converter
SRC	4004 DFF0h	4004 DFF7h	5		4 to 5		PCLKB	
SRC	4004 DFF8h	4004 DFFFh	3		2 to 3		PCLKB	
SSIEn, CANn, IICn, DOC, ADC12n, TSN, DAC12	4004 E000h	4005 FFFFh	3		2 to 3		PCLKB	Serial Sound Interface Enhanced, Controller Area Network Module, I2C Bus Interface, Data Operation Circuit, 12-Bit A/D Converter, Temperature Sensor, 12-Bit D/A Converter
USBHS	4006 0000h	4006 0FFFh	(3+BWAIT)*2		(2+BWAIT) to (3+BWAIT)*2		PCLKA	USB 2.0 High-Speed Module
SDHIn	4006 2000h	4006 2FFFh	3		2 to 3		PCLKA	SD/MMC Host Interface
EDMAC0	4006 4000h	4006 40FFh	4		-		PCLKA	Ethernet DMA Controller
ETHERC0	4006 4100h	4006 41FFh	13		-		PCLKA	Ethernet MAC Controller
PTPEDMAC	4006 4400h	4006 44FFh	4		-		PCLKA	Ethernet DMA Controller
EPTPC_CFG, EPTPC, EPTPC0	4006 4500h	4006 5BFFh	(1+wait cycle)*3		-		PCLKA	Ethernet PTP Controller
SCI0 to SCI9	4007 0000h	4007 0EFFh	3*4		2 to 3*4		PCLKA	Serial Communications Interface
IRDA	4007 0F00h	4007 0FFFh	3		2 to 3		PCLKA	IrDA Interface
SPI0, SPI1	4007 2000h	4007 2FFFh	3*5		2 to 3*5		PCLKA	Serial Peripheral Interface
CRC	4007 4000h	4007 4FFFh	3		2 to 3		PCLKA	CRC Calculator
GPT32EHi, GPT32Ej, GPT32k, GPT_OPS	4007 8000h	4007 8FFFh	5	3	4 to 5	2 to 3	PCLKA	General PWM Timer

Note: 这适用于当来自CPU的访问与从外部存储器获取指令或来自其他总线主控器（例如DTC或DMAC）的总线访问不冲突时的周期数。

Table 3.2 访问周期(1of2)

Peripherals	Address		访问周期数				Cycle Unit	相关功能
			ICLK = PCLK		ICLK > PCLK*1			
	From	To	Read	Write	Read	Write		
MMPU, SMPU, SPMON, MMF, SRAM, BUS, DMACn, DMA, DTC, ICU, DBG, FCACHE	4000 0000h	4001 CFFFh	4				ICLK	内存保护单元、内存镜像功能、SRAM、总线、DMA控制器、数据传输控制器，中断控制器、CPU、闪存Memory
SYSTEM	4001 E000h	4001 E3FFh	5				ICLK	低功耗模式，复位，低电压检测，时钟产生电路，寄存器写保护
SYSTEM	4001 E400h	4001 E6FFh	9		5 to 8		PCLKB	低功耗模式，复位，低电压检测，电池备份功能
PORTn, PFS, PMISC, ELC, POEG, RTC, WDT, IWDT, CAC, MSTP	4004 0000h	4004 7FFFh	3		2 to 3		PCLKB	IO端口，事件链接控制器，GPT端口输出使能，实时时钟、看门狗定时器、独立看门狗定时器、时钟频率精度测量电路、模块停止控制
SRCRAM	4004 8000h	4004 DFEFh	4	3	3 to 4	2 to 3	PCLKB	采样率转换器
SRC	4004 DFF0h	4004 DFF7h	5		4 to 5		PCLKB	
SRC	4004 DFF8h	4004 DFFFh	3		2 to 3		PCLKB	
SSIEn、CANn、IICn、DOC、ADC12n, TSN, DAC12	4004 E000h	4005 FFFFh	3		2 to 3		PCLKB	串行声音接口增强型，控制器局域网模块，I2C总线接口，数据操作电路，12位AD转换器，温度传感器，12位D/A Converter
USBHS	4006 0000h	4006 0FFFh	(3+BWAIT)*2		(2+BWAIT) to (3+BWAIT)*2		PCLKA	USB2.0高速模块
SDHIn	4006 2000h	4006 2FFFh	3		2 to 3		PCLKA	SDMMC主机接口
EDMAC0	4006 4000h	4006 40FFh	4		-		PCLKA	以太网DMA控制器
ETHERC0	4006 4100h	4006 41FFh	13		-		PCLKA	以太网MAC控制器
PTPEDMAC	4006 4400h	4006 44FFh	4		-		PCLKA	以太网DMA控制器
EPTPC_CFG, EPTPC, EPTPC0	4006 4500h	4006 5BFFh	(1+wait cycle)*3		-		PCLKA	以太网PTP控制器
SCI0 to SCI9	4007 0000h	4007 0EFFh	3*4		2 to 3*4		PCLKA	串行通信Interface
IRDA	4007 0F00h	4007 0FFFh	3		2 to 3		PCLKA	IrDA Interface
SPI0, SPI1	4007 2000h	4007 2FFFh	3*5		2 to 3*5		PCLKA	串行外设接口
CRC	4007 4000h	4007 4FFFh	3		2 to 3		PCLKA	CRC Calculator
GPT32EHi, GPT32Ej, GPT32k, GPT_OPS	4007 8000h	4007 8FFFh	5	3	4 to 5	2 to 3	PCLKA	通用PWM定时器

Table 3.2 Access cycles (2 of 2)

Peripherals	Address		Number of access cycles				Cycle Unit	Related function
			ICLK = PCLK		ICLK > PCLK*1			
	From	To	Read	Write	Read	Write		
GPT_ODC	4007 B000h	4007 BFFFh	2		1 to 2		PCLKA	PWM Delay Generation Circuit
KINT, CTSU	4008 0000h	4008 1FFFh	2		1 to 2		PCLKB	Key interrupt Function, Capacitive Touch Sensing Unit
AGTn	4008 4000h	4008 4FFFh	5	3	4 to 5	2 to 3	PCLKB	Asynchronous General Purpose Timer
ACMPHSn	4008 5000h	4008 5FFFh	2		1 to 2		PCLKB	High-Speed Analog Comparator
USBFS	4009 0000h	4009 03FFh	4		3 to 4		PCLKB	USB 2.0 Full-Speed Module
USBFS	4009 0400h	4009 04FFh	2		1 to 2		PCLKB	USB 2.0 Full-Speed Module
PDC	4009 4000h	4009 4FFFh	3		2 to 3		PCLKB	Parallel Data Capture Unit
GLCDC, DRW	400E 0000h	400E 4FFFh	3		-		PCLKA	Graphics LCD Controller 2D Drawing Engine
JPEG	400E 6000h	400E 603Fh	13	5	-		PCLKA	JPEG Codec
JPEG	400E 6040h	400E 6FFFh	5	4	-		PCLKA	JPEG Codec
QSPI	6400 0000h	6400 000Fh	3	13 to *6	2 to 3	12 to *6	PCLKA	Quad Serial Peripheral Interface
QSPI	6400 0010h	6400 0013h	24 to *6	5 to *6	23 to *6	4 to *6	PCLKA	Quad Serial Peripheral Interface
QSPI	6400 0014h	6400 0037h	3	13 to *6	2 to 3	12 to *6	PCLKA	Quad Serial Peripheral Interface
QSPI	6400 0804h	6400 0807h	2	2	1 to 2	1 to 2	PCLKA	Quad Serial Peripheral Interface

Note 1. If the number of PCLK cycles is non-integer (for example 1.5), the minimum value is without the decimal point, and the maximum value is rounded up to the decimal point. For example, 1.5 to 2. 5 is 1 to 3.
Note 2. BWAIT is the number of waits (not cycles) described in the USBHS.BUSWAIT register.
Note 3. The wait cycle refers to the EPTPC chapter (30.6.2 Wait Cycles for Register Access).
Note 4. When accessing a 16-bit register (FTDRHL, FRDRHL, FCR, FDR, LSR, and CDR), access is 2 cycles more than the value shown in Table 3.2. When accessing an 8-bit register (including FTDRH, FTDRL, FRDRH, and FRDRL), the access cycles are as shown in Table 3.2.
Note 5. When accessing the 32-bit register (SPDR), access is 2 cycles more than the value in Table 3.2. When accessing an 8-bit or 16-bit register (SPDR_HA), the access cycles are as shown in Table 3.2.
Note 6. The access cycles depend on the QSPI bus cycles.

3.3 Register Descriptions

This section provides information associated with registers described in this manual.

Table 3.3 shows a list of registers including address offsets, address sizes, access rights, and reset values.

Table 3.3 Register description (1 of 44)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
MMPU	3	0x400	A,B,C	MMPUCTL%s	Bus Master MPU Control Register	0x000	16	read/ write	0x0000	0xFFFF
MMPU	-	-	-	MMPUPTA	Group A Protection of Register	0x102	16	read/ write	0x0000	0xFFFF
MMPU	32	0x010	0-31	MMPUACA%s	Group A Region %s Access Control Register	0x200	32	read/ write	0x00000000	0xFFFFFFFF

Table 3.2 访问周期(2of2)

Peripherals	Address		访问周期数				Cycle Unit	相关功能
			ICLK = PCLK		ICLK > PCLK*1			
	From	To	Read	Write	Read	Write		
GPT_ODC	4007 B000h	4007 BFFFh	2		1 to 2		PCLKA	PWM延迟生成 Circuit
KINT, CTSU	4008 0000h	4008 1FFFh	2		1 to 2		PCLKB	按键中断功能，电容式触控感应 Unit
AGTn	4008 4000h	4008 4FFFh	5	3	4 to 5	2 to 3	PCLKB	异步通用目的定时器
ACMPHSn	4008 5000h	4008 5FFFh	2		1 to 2		PCLKB	High-Speed Analog Comparator
USBFS	4009 0000h	4009 03FFh	4		3 to 4		PCLKB	USB2.0全速模块
USBFS	4009 0400h	4009 04FFh	2		1 to 2		PCLKB	USB2.0全速模块
PDC	4009 4000h	4009 4FFFh	3		2 to 3		PCLKB	并行数据采集单元
GLCDC, DRW	400E 0000h	400E 4FFFh	3		-		PCLKA	图形LCD控制器2D绘图引擎
JPEG	400E 6000h	400E 603Fh	13	5	-		PCLKA	JPEG编解码器
JPEG	400E 6040h	400E 6FFFh	5	4	-		PCLKA	JPEG编解码器
QSPI	6400 0000h	6400 000Fh	3	13 to *6	2 to 3	12 to *6	PCLKA	四路串行外设 Interface
QSPI	6400 0010h	6400 0013h	24 to *6	5 to *6	23 to *6	4 to *6	PCLKA	四路串行外设 Interface
QSPI	6400 0014h	6400 0037h	3	13 to *6	2 to 3	12 to *6	PCLKA	四路串行外设 Interface
QSPI	6400 0804h	6400 0807h	2	2	1 to 2	1 to 2	PCLKA	四路串行外设 Interface

注1.如果PCLK周期数为非整数（例如1.5），则最小值不带小数点，最大值四舍五入到小数点。例如，1.5到2。5是1到3。注2.BWAIT是USBHS.BUSWAIT寄存器中描述的等待数（不是周期数）。

注3.等待周期参考EPTPC章节（30.6.2寄存器访问的等待周期）。
注4.访问16位寄存器（FTDRHL、FRDRHL、FCR、FDR、LSR和CDR）时，访问比表3.2中显示的值多2个周期。访问8位寄存器（包括FTDRH、FTDRL、FRRDH和FRDRL）时，访问周期如表3.2所示。

注5.访问32位寄存器(SPDR)时，访问比表3.2中的值多2个周期。访问8位或16位寄存器（SPDR_HA）时，访问周期如表3.2所示。注6.访问周期取决于QSPI总线周期。

3.3 注册说明

本节提供与本手册中描述的寄存器相关的信息。

表3.3显示了寄存器列表，包括地址偏移、地址大小、访问权限和复位值。

Table 3.3 寄存器说明（44个中的1个）

周边暗淡		昏暗的增量。	暗淡索引寄存器名称		Description	地址偏移	尺寸	访问	重置值	重置蒙版
MMPU	3	0x400	A,B,C	MMPUCTL%s	总线主控MPU控制 Register	0x000	16	read/ write	0x0000	0xFFFF
MMPU	-	-	-	MMPUPTA	A组保护 Register	0x102	16	read/ write	0x0000	0xFFFF
MMPU	32	0x010	0-31	MMPUACA%s	A组区域%s访问权限控制寄存器	0x200	32	read/ write	0x00000000	0xFFFFFFFF

Table 3.3 Register description (2 of 44)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
MMPU	32	0x010	0-31	MMPUSA%s	Group A Region %s Start Address Register	0x204	32	read/ write	0x00000000	0x00000003
MMPU	32	0x010	0-31	MMPUEA%s	Group A Region %s End Address Register	0x208	32	read/ write	0x00000003	0x00000003
MMPU	-	-	-	MMPUPTB	Group B Protection of Register	0x502	16	read/ write	0x0000	0xFFFF
MMPU	8	0x010	0-7	MMPUACB%s	Group B Region %s Access Control Register	0x600	32	read/ write	0x00000000	0xFFFFFFFF
MMPU	8	0x010	0-7	MMPUSB%s	Group B Region %s Start Address Register	0x604	32	read/ write	0x00000000	0x00000003
MMPU	8	0x010	0-7	MMPUEB%s	Group B Region %s End Address Register	0x608	32	read/ write	0x00000003	0x00000003
MMPU	-	-	-	MMPUPTC	Group C protection of register	0x902	16	read/ write	0x0000	0xFFFF
MMPU	8	0x010	0-7	MMPUACC%s	Group C Region %s Access Control Register	0xA00	32	read/ write	0x00000000	0xFFFFFFFF
MMPU	8	0x010	0-7	MMPUSC%s	Group C Region %s Start Address Register	0xA04	32	read/ write	0x00000000	0x00000003
MMPU	8	0x010	0-7	MMPUEC%s	Group C Region %s Start Address Register	0xA08	32	read/ write	0x00000003	0x00000003
SMPU	-	-	-	SMPUCTL	Slave MPU Control Register	0x00	16	read/ write	0x0000	0xFFFF
SMPU	-	-	-	SMPUMBIU	Access Control Register for MBIU	0x10	16	read/ write	0x2000	0xFFFF
SMPU	-	-	-	SMPUFBIU	Access Control Register for FBIU	0x14	16	read/ write	0x00C0	0xFFFF
SMPU	2	0x4	0,1	SMPUSRAM%s	Access Control Register for SRAM%s	0x18	16	read/ write	0x0000	0xFFFF
SMPU	4	0x4	0,2,6,7	SMPUP%sBIU	Access Control Register for P%sBIU	0x20	16	read/ write	0x00F0	0xFFFF
SMPU	-	-	-	SMPUEXBIU	Access Control Register for EXBIU	0x30	16	read/ write	0x0000	0xFFFF
SMPU	-	-	-	SMPUEXBIU2	Access Control Register for EXBIU2	0x34	16	read/ write	0x0000	0xFFFF
SPMON	-	-	-	MSPMPUOAD	Stack Pointer Monitor Operation After Detection Register	0x00	16	read/ write	0x0000	0xFFFF
SPMON	-	-	-	MSPMPUCTL	Stack Pointer Monitor Access Control Register	0x04	16	read/ write	0x0000	0xFFFF
SPMON	-	-	-	MSPMPUPT	Stack Pointer Monitor Protection Register	0x06	16	read/ write	0x0000	0xFFFF
SPMON	-	-	-	MSPMPUSA	Main Stack Pointer Monitor Start Address Register	0x08	32	read/ write	0x00000000	0x00000003
SPMON	-	-	-	MSPMPUEA	Main Stack Pointer Monitor End Address Register	0x0C	32	read/ write	0x00000003	0x00000003
SPMON	-	-	-	PSPMPUOAD	Stack Pointer Monitor Operation After Detection Register	0x10	16	read/ write	0x0000	0xFFFF
SPMON	-	-	-	PSPMPUCTL	Stack Pointer Monitor Access Control Register	0x14	16	read/ write	0x0000	0xFFFF
SPMON	-	-	-	PSPMPUPT	Stack Pointer Monitor Protection Register	0x16	16	read/ write	0x0000	0xFFFF
SPMON	-	-	-	PSPMPUSA	Process Stack Pointer Monitor Start Address Register	0x18	32	read/ write	0x00000000	0x00000003
SPMON	-	-	-	PSPMPUEA	Process Stack Pointer Monitor End Address Register	0x1C	32	read/ write	0x00000003	0x00000003
MMF	-	-	-	MMSFR	MemMirror Special Function Register	0x00	32	read/ write	0x00000000	0xFFFFFFFF

Table 3.3 寄存器说明（44个中的2个）

周边暗淡		昏暗的增量。	暗淡索引寄存器名称		Description	地址偏移	尺寸访问		重置值	重置蒙版
MMPU	32	0x010	0-31	MMPUSA%s	A组地区%s开始地址寄存器	0x204	32	read/ write	0x00000000	0x00000003
MMPU	32	0x010	0-31	MMPUEA%s	A组地区%s结束地址寄存器	0x208	32	read/ write	0x00000003	0x00000003
MMPU	-	-	-	MMPUPTB	B组保护Register	0x502	16	read/ write	0x0000	0xFFFF
MMPU	8	0x010	0-7	MMPUACB%s	B组区域%s访问控制寄存器	0x600	32	read/ write	0x00000000	0xFFFFFFFF
MMPU	8	0x010	0-7	MMPUSB%s	B组地区%s开始地址寄存器	0x604	32	read/ write	0x00000000	0x00000003
MMPU	8	0x010	0-7	MMPUEB%s	B组地区%s结束地址寄存器	0x608	32	read/ write	0x00000003	0x00000003
MMPU	-	-	-	MMPUPTC	C组注册保护	0x902	16	read/ write	0x0000	0xFFFF
MMPU	8	0x010	0-7	MMPUACC%s	C组区域%s访问权限控制寄存器	0xA00	32	read/ write	0x00000000	0xFFFFFFFF
MMPU	8	0x010	0-7	MMPUSC%s	C组地区%s开始地址寄存器	0xA04	32	read/ write	0x00000000	0x00000003
MMPU	8	0x010	0-7	MMPUEC%s	C组地区%s开始地址寄存器	0xA08	32	read/ write	0x00000003	0x00000003
SMPU	-	-	-	SMPUCTL	从机MPU控制寄存器	0x00	16	read/ write	0x0000	0xFFFF
SMPU	-	-	-	SMPUMBIU	访问控制寄存器MBIU	0x10	16	read/ write	0x2000	0xFFFF
SMPU	-	-	-	SMPUFBIU	访问控制寄存器FBIU	0x14	16	read/ write	0x00C0	0xFFFF
SMPU	2	0x4	0,1	SMPUSRAM%s	访问控制寄存器SRAM%s	0x18	16	read/ write	0x0000	0xFFFF
SMPU	4	0x4	0,2,6,7	SMPUP%sBIU	访问控制寄存器P%sBIU	0x20	16	read/ write	0x00F0	0xFFFF
SMPU	-	-	-	SMPUEXBIU	访问控制寄存器EXBIU	0x30	16	read/ write	0x0000	0xFFFF
SMPU	-	-	-	SMPUEXBIU2	访问控制寄存器EXBIU2	0x34	16	read/ write	0x0000	0xFFFF
SPMON	-	-	-	MSPMPUOAD	堆栈指针监视器检测后的操作Register	0x00	16	read/ write	0x0000	0xFFFF
SPMON	-	-	-	MSPMPUCTL	堆栈指针监视器访问控制寄存器	0x04	16	read/ write	0x0000	0xFFFF
SPMON	-	-	-	MSPMPUPT	堆栈指针监视器保护登记册	0x06	16	read/ write	0x0000	0xFFFF
SPMON	-	-	-	MSPMPUSA	主堆栈指针监视器起始地址寄存器	0x08	32	read/ write	0x00000000	0x00000003
SPMON	-	-	-	MSPMPUEA	主堆栈指针监视器结束地址寄存器	0x0C	32	read/ write	0x00000003	0x00000003
SPMON	-	-	-	PSPMPUOAD	堆栈指针监视器检测后的操作Register	0x10	16	read/ write	0x0000	0xFFFF
SPMON	-	-	-	PSPMPUCTL	堆栈指针监视器访问控制寄存器	0x14	16	read/ write	0x0000	0xFFFF
SPMON	-	-	-	PSPMPUPT	堆栈指针监视器保护登记册	0x16	16	read/ write	0x0000	0xFFFF
SPMON	-	-	-	PSPMPUSA	进程堆栈指针监视器起始地址Register	0x18	32	read/ write	0x00000000	0x00000003
SPMON	-	-	-	PSPMPUEA	进程堆栈指针监视器结束地址Register	0x1C	32	read/ write	0x00000003	0x00000003
MMF	-	-	-	MMSFR	MemMirror特殊功能Register	0x00	32	read/ write	0x00000000	0xFFFFFFFF

Table 3.3 Register description (3 of 44)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
MMF	-	-	-	MMEN	MemMirror Enable Register	0x04	32	read/ write	0x00000000	0xFFFFFFFF
SRAM	-	-	-	PARIOAD	SRAM Parity Error Operation After Detection Register	0x00	8	read/ write	0x00	0xFF
SRAM	-	-	-	SRAMPRCR	SRAM Protection Register	0x04	8	read/ write	0x00	0xFF
SRAM	-	-	-	SRAMWTSC	RAM Wait State Control Register	0x08	8	read/ write	0x0E	0xFF
SRAM	-	-	-	ECCMODE	ECCRAM Operating Mode Control Register	0xC0	8	read/ write	0x00	0xFF
SRAM	-	-	-	ECC2STS	ECCRAM 2-Bit Error Status Register	0xC1	8	read/ write	0x00	0xFF
SRAM	-	-	-	ECC1STSEN	ECCRAM 1-Bit Error Information Update Enable Register	0xC2	8	read/ write	0x00	0xFF
SRAM	-	-	-	ECC1STS	ECCRAM 1-Bit Error Status Register	0xC3	8	read/ write	0x00	0xFF
SRAM	-	-	-	ECCPRCR	ECCRAM Protection Register	0xC4	8	read/ write	0x00	0xFF
SRAM	-	-	-	ECCPRCR2	ECCRAM Protection Register 2	0xD0	8	read/ write	0x00	0xFF
SRAM	-	-	-	ECCRAMETST	ECCRAM Test Control Register	0xD4	8	read/ write	0x00	0xFF
SRAM	-	-	-	ECCOAD	RAM ECC Error Operation After Detection Register	0xD8	8	read/ write	0x00	0xFF
BUS	8	0x10	0-7	CS%sMOD	CS%s Mode Register	0x0002	16	read/ write	0x0000	0xFFFF
BUS	8	0x10	0-7	CS%sWCR1	CS%s Wait Control Register 1	0x0004	32	read/ write	0x07070707	0xFFFFFFFF
BUS	8	0x10	0-7	CS%sWCR2	CS%s Wait Control Register 2	0x0008	32	read/ write	0x00000007	0xFFFFFFFF
BUS	-	-	-	CS0CR	CS0 Control Register	0x0802	16	read/ write	0x0021	0xFFFF
BUS	8	0x10	0-7	CS%sREC	CS%s Recovery Cycle Register	0x080A	16	read/ write	0x0000	0xFFFF
BUS	7	0x10	1-7	CS%sCR	CS%s Control Register	0x0812	16	read/ write	0x0000	0xFFFF
BUS	-	-	-	CSRECEN	CS Recovery Cycle Insertion Enable Register	0x0880	16	read/ write	0x3E3E	0xFFFF
BUS	-	-	-	SDCCR	SDC Control Register	0x0C00	8	read/ write	0x00	0xFF
BUS	-	-	-	SDCMOD	SDC Mode Register	0x0C01	8	read/ write	0x00	0xFF
BUS	-	-	-	SDAMOD	SDRAM Access Mode Register	0x0C02	8	read/ write	0x00	0xFF
BUS	-	-	-	SDSELF	SDRAM Self-Refresh Control Register	0x0C10	8	read/ write	0x00	0xFF
BUS	-	-	-	SDRFCR	SDRAM Refresh Control Register	0x0C14	16	read/ write	0x0001	0xFFFF
BUS	-	-	-	SDRFEN	SDRAM Auto-Refresh Control Register	0x0C16	8	read/ write	0x00	0xFF
BUS	-	-	-	SDICR	SDRAM Initialization Sequence Control Register	0x0C20	8	read/ write	0x00	0xFF
BUS	-	-	-	SDIR	SDRAM Initialization Register	0x0C24	16	read/ write	0x0010	0xFFFF
BUS	-	-	-	SDADR	SDRAM Address Register	0x0C40	8	read/ write	0x00	0xFF
BUS	-	-	-	SDTR	SDRAM Timing Register	0x0C44	32	read/ write	0x00000002	0xFFFFFFFF

Table 3.3 注册描述（3/44）

周边暗淡		昏暗的增量。	暗淡索引寄存器名称		Description	地址偏移	尺寸	访问	重置值	重置蒙版
MMF	-	-	-	MMEN	MemMirror启用寄存器	0x04	32	read/ write	0x00000000	0xFFFFFFFF
SRAM	-	-	-	PARIOAD	SRAM奇偶校验错误操作检测后寄存器	0x00	8	read/ write	0x00	0xFF
SRAM	-	-	-	SRAMPRCR	SRAM保护寄存器	0x04	8	read/ write	0x00	0xFF
SRAM	-	-	-	SRAMWTSC	RAM等待状态控制Register	0x08	8	read/ write	0x0E	0xFF
SRAM	-	-	-	ECCMODE	ECCRAM操作模式控制寄存器	0xC0	8	read/ write	0x00	0xFF
SRAM	-	-	-	ECC2STS	ECCRAM2位错误状态Register	0xC1	8	read/ write	0x00	0xFF
SRAM	-	-	-	ECC1STSEN	ECCRAM 1-Bit Error信息更新启用Register	0xC2	8	read/ write	0x00	0xFF
SRAM	-	-	-	ECC1STS	ECCRAM1位错误状态Register	0xC3	8	read/ write	0x00	0xFF
SRAM	-	-	-	ECCPRCR	ECCRAM Protection Register	0xC4	8	read/ write	0x00	0xFF
SRAM	-	-	-	ECCPRCR2	ECCRAM Protection Register 2	0xD0	8	read/ write	0x00	0xFF
SRAM	-	-	-	ECCRAMETST	ECCRAM测试控制Register	0xD4	8	read/ write	0x00	0xFF
SRAM	-	-	-	ECCOAD	RAMECC错误操作检测后寄存器	0xD8	8	read/ write	0x00	0xFF
BUS	8	0x10	0-7	CS%sMOD	CS%s模式寄存器	0x0002	16	read/ write	0x0000	0xFFFF
BUS	8	0x10	0-7	CS%sWCR1	CS%s等待控制寄存器1	0x0004	32	read/ write	0x07070707	0xFFFFFFFF
BUS	8	0x10	0-7	CS%sWCR2	CS%s等待控制寄存器2	0x0008	32	read/ write	0x00000007	0xFFFFFFFF
BUS	-	-	-	CS0CR	CS0控制寄存器	0x0802	16	read/ write	0x0021	0xFFFF
BUS	8	0x10	0-7	CS%sREC	CS%s恢复周期Register	0x080A	16	read/ write	0x0000	0xFFFF
BUS	7	0x10	1-7	CS%sCR	CS%s控制寄存器	0x0812	16	read/ write	0x0000	0xFFFF
BUS	-	-	-	CSRECEN	CS恢复周期插入启用注册	0x0880	16	read/ write	0x3E3E	0xFFFF
BUS	-	-	-	SDCCR	SDC控制寄存器	0x0C00	8	read/ write	0x00	0xFF
BUS	-	-	-	SDCMOD	SDC模式寄存器	0x0C01	8	read/ write	0x00	0xFF
BUS	-	-	-	SDAMOD	SDRAM存取模式Register	0x0C02	8	read/ write	0x00	0xFF
BUS	-	-	-	SDSELF	SDRAM Self-Refresh控制寄存器	0x0C10	8	read/ write	0x00	0xFF
BUS	-	-	-	SDRFCR	SDRAM刷新控制Register	0x0C14	16	read/ write	0x0001	0xFFFF
BUS	-	-	-	SDRFEN	SDRAM Auto-Refresh控制寄存器	0x0C16	8	read/ write	0x00	0xFF
BUS	-	-	-	SDICR	SDRAM Initialization序列控制寄存器	0x0C20	8	read/ write	0x00	0xFF
BUS	-	-	-	SDIR	SDRAM Initialization Register	0x0C24	16	read/ write	0x0010	0xFFFF
BUS	-	-	-	SDADR	SDRAM地址寄存器	0x0C40	8	read/ write	0x00	0xFF
BUS	-	-	-	SDTR	SDRAM时序寄存器	0x0C44	32	read/ write	0x00000002	0xFFFFFFFF

Table 3.3 Register description (4 of 44)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
BUS	-	-	-	SDMOD	SDRAM Mode Register	0x0C48	16	read/ write	0x0000	0xFFFF
BUS	-	-	-	SDSR	SDRAM Status Register	0x0C50	8	read-only	0x00	0xFF
BUS	2	0x4	M4I, M4D	BUSMCNT%s	Master Bus Control Register %s	0x1000	16	read/ write	0x0000	0xFFFF
BUS	-	-	-	BUSMCNTSYS	Master Bus Control Register SYS	0x1008	16	read/ write	0x0000	0xFFFF
BUS	-	-	-	BUSMCNTDMA	Master Bus Control Register DMA	0x100C	16	read/ write	0x0000	0xFFFF
BUS	2	0x4	EDM, GPX	BUSMCNT%s	Master Bus Control Register %s	0x1010	16	read/ write	0x0000	0xFFFF
BUS	2	0x4	FLI,RAMH	BUSSCNT%s	Slave Bus Control Register %s	0x1100	16	read/ write	0x0000	0xFFFF
BUS	-	-	-	BUSSCNTMBIU	Slave Bus Control Register MBIU	0x1108	16	read/ write	0x0000	0xFFFF
BUS	2	0x4	RAM 0,RAM1	BUSSCNT%s	Slave Bus Control Register %s	0x110C	16	read/ write	0x0000	0xFFFF
BUS	4	0x4	P0B, P2B, P3B, P4B	BUSSCNT%s	Slave Bus Control Register %s	0x1114	16	read/ write	0x0000	0xFFFF
BUS	2	0x4	P6B, P7B	BUSSCNT%s	Slave Bus Control Register %s	0x1128	16	read/ write	0x0000	0xFFFF
BUS	4	0x4	FBU, EXT, EXT2 ,GPX	BUSSCNT%s	Slave Bus Control Register %s	0x1130	16	read/ write	0x0000	0xFFFF
BUS	11	0x10	1-11	BUS%sERRADD	Bus Error Address Register %s	0x1800	32	read-only	0x00000000	0x00000000
BUS	11	0x10	1-11	BUS%sERRSTAT	Bus Error Status Register %s	0x1804	8	read-only	0x00	0xFE
DMAC0-7	-	-	-	DMSAR	DMA Source Address Register	0x00	32	read/ write	0x00000000	0xFFFFFFFF
DMAC0-7	-	-	-	DMDAR	DMA Destination Address Register	0x04	32	read/ write	0x00000000	0xFFFFFFFF
DMAC0-7	-	-	-	DMCRA	DMA Transfer Count Register	0x08	32	read/ write	0x00000000	0xFFFFFFFF
DMAC0-7	-	-	-	DMCRB	DMA Block Transfer Count Register	0x0C	16	read/ write	0x0000	0xFFFF
DMAC0-7	-	-	-	DMTMD	DMA Transfer Mode Register	0x10	16	read/ write	0x0000	0xFFFF
DMAC0-7	-	-	-	DMINT	DMA Interrupt Setting Register	0x13	8	read/ write	0x00	0xFF
DMAC0-7	-	-	-	DMAMD	DMA Address Mode Register	0x14	16	read/ write	0x0000	0xFFFF
DMAC0-7	-	-	-	DMOFR	DMA Offset Register	0x18	32	read/ write	0x00000000	0xFFFFFFFF
DMAC0-7	-	-	-	DMCNT	DMA Transfer Enable Register	0x1C	8	read/ write	0x00	0xFF
DMAC0-7	-	-	-	DMREQ	DMA Software Start Register	0x1D	8	read/ write	0x00	0xFF
DMAC0-7	-	-	-	DMSTS	DMAC Module Activation Register	0x1E	8	read/ write	0x00	0xFF
DMA	-	-	-	DMAST	DMA Module Activation Register	0x00	8	read/ write	0x00	0xFF
DTC	-	-	-	DTCCR	DTC Control Register	0x00	8	read/ write	0x08	0xFF

Table 3.3 寄存器说明（44之4）

周边暗淡	昏暗的增量。	暗淡索引寄存器名称	Description	地址偏移	尺寸访问		重置值	重置蒙版
BUS	-	-	-	SDMOD	SDRAM模式寄存器	0x0C48	16	read/ write	0x0000	0xFFFF
BUS	-	-	-	SDSR	SDRAM状态寄存器	0x0C50	8	只读	0x00	0xFF
BUS	2	0x4	M4I, M4D	BUSMCNT%s	主总线控制寄存器%s	0x1000	16	read/ write	0x0000	0xFFFF
BUS	-	-	-	BUSMCNTSYS	主总线控制寄存器 SYS	0x1008	16	read/ write	0x0000	0xFFFF
BUS	-	-	-	BUSMCNTDMA	主总线控制寄存器 DMA	0x100C	16	read/ write	0x0000	0xFFFF
BUS	2	0x4	EDM, GPX	BUSMCNT%s	主总线控制寄存器%s	0x1010	16	read/ write	0x0000	0xFFFF
BUS	2	0x4	FLI,RAMH	BUSSCNT%s	从总线控制寄存器%s	0x1100	16	read/ write	0x0000	0xFFFF
BUS	-	-	-	BUSSCNTMBIU	从总线控制寄存器 MBIU	0x1108	16	read/ write	0x0000	0xFFFF
BUS	2	0x4	RAM 0,RAM1	BUSSCNT%s	从总线控制寄存器%s	0x110C	16	read/ write	0x0000	0xFFFF
BUS	4	0x4	P0B, P2B, P3B, P4B	BUSSCNT%s	从总线控制寄存器%s	0x1114	16	read/ write	0x0000	0xFFFF
BUS	2	0x4	P6B, P7B	BUSSCNT%s	从总线控制寄存器%s	0x1128	16	read/ write	0x0000	0xFFFF
BUS	4	0x4	FBU, EXT, EXT2 ,GPX	BUSSCNT%s	从总线控制寄存器%s	0x1130	16	read/ write	0x0000	0xFFFF
BUS	11	0x10	1-11	BUS%sERRADD	总线错误地址寄存器%s	0x1800	32	只读	0x00000000	0x00000000
BUS	11	0x10	1-11	BUS%sERRSTAT	总线错误状态寄存器%s	0x1804	8	只读	0x00	0xFE
DMAC0-7	-	-	-	DMSAR	DMA源地址 Register	0x00	32	read/ write	0x00000000	0xFFFFFFFF
DMAC0-7	-	-	-	DMDAR	DMA目标地址 Register	0x04	32	read/ write	0x00000000	0xFFFFFFFF
DMAC0-7	-	-	-	DMCRA	DMA传输计数 Register	0x08	32	read/ write	0x00000000	0xFFFFFFFF
DMAC0-7	-	-	-	DMCRB	DMA块传输计数 Register	0x0C	16	read/ write	0x0000	0xFFFF
DMAC0-7	-	-	-	DMTMD	DMA传输模式 Register	0x10	16	read/ write	0x0000	0xFFFF
DMAC0-7	-	-	-	DMINT	DMA中断设置 Register	0x13	8	read/ write	0x00	0xFF
DMAC0-7	-	-	-	DMAMD	DMA地址模式寄存器	0x14	16	read/ write	0x0000	0xFFFF
DMAC0-7	-	-	-	DMOFR	DMA偏移寄存器	0x18	32	read/ write	0x00000000	0xFFFFFFFF
DMAC0-7	-	-	-	DMCNT	DMA传输使能 Register	0x1C	8	read/ write	0x00	0xFF
DMAC0-7	-	-	-	DMREQ	DMA软件启动寄存器	0x1D	8	read/ write	0x00	0xFF
DMAC0-7	-	-	-	DMSTS	DMAC模块激活 Register	0x1E	8	read/ write	0x00	0xFF
DMA	-	-	-	DMAST	DMA模块激活 Register	0x00	8	read/ write	0x00	0xFF
DTC	-	-	-	DTCCR	DTC控制寄存器	0x00	8	read/ write	0x08	0xFF

Table 3.3 Register description (5 of 44)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
DTC	-	-	-	DTCVBR	DTC Vector Base Register	0x04	32	read/ write	0x00000000	0xFFFFFFFF
DTC	-	-	-	DTCST	DTC Module Start Register	0x0C	8	read/ write	0x00	0xFF
DTC	-	-	-	DTCSTS	DTC Status Register	0x0E	16	read-only	0x0000	0xFFFF
ICU	16	0x1	0-15	IRQCR%s	IRQ Control Register %s	0x000	8	read/ write	0x00	0xFF
ICU	-	-	-	NMICR	NMI Pin Interrupt Control Register	0x100	8	read/ write	0x00	0xFF
ICU	-	-	-	NMIER	Non-Maskable Interrupt Enable Register	0x120	16	read/ write	0x0000	0xFFFF
ICU	-	-	-	NMICLR	Non-Maskable Interrupt Status Clear Register	0x130	16	write-only	0x0000	0xFFFF
ICU	-	-	-	NMISR	Non-Maskable Interrupt Status Register	0x140	16	read-only	0x0000	0xFFFF
ICU	-	-	-	WUPEN	Wake Up interrupt enable register	0x1A0	32	read/ write	0x00000000	0xFFFFFFFF
ICU	-	-	-	SELSR0	Event Selection to Cancel Snooze Mode	0x200	16	read/ write	0x0000	0xFFFF
ICU	8	0x4	0-7	DELSR%s	DMAC Event Link Setting Register %s	0x280	32	read/ write	0x00000000	0xFFFFFFFF
ICU	96	0x4	0-95	IELSR%s	INT Event Link Setting Register %s	0x300	32	read/ write	0x00000000	0xFFFFFFFF
DBG	-	-	-	DBGSTR	Debug Status Register	0x000	32	read-only	0x00000000	0xFFFFFFFF
DBG	-	-	-	DBGSTOPCR	Debug Stop Control Register	0x010	32	read/ write	0x00000003	0xFFFFFFFF
DBG	-	-	-	TRACECTR	Trace Control Register	0x020	32	read/ write	0x00000000	0xFFFFFFFF
FCACHE	-	-	-	FCACHEE	Flash Cache Enable Register	0x100	16	read/ write	0x0000	0xFFFF
FCACHE	-	-	-	FCACHEIV	Flash Cache Invalidate Register	0x104	16	read/ write	0x0000	0xFFFF
FCACHE	-	-	-	FLWT	Flash Wait Cycle Register	0x11C	8	read/ write	0x00	0xFF
SYSTEM	-	-	-	SBYCR	Standby Control Register	0x00C	16	read/ write	0x4000	0xFFFF
SYSTEM	-	-	-	MSTPCRA	Module Stop Control Register A	0x01C	32	read/ write	0xFFBFFF1C	0xFFFFFFFF
SYSTEM	-	-	-	SCKDIVCR	System Clock Division Control Register	0x020	32	read/ write	0x22022222	0xFFFFFFFF
SYSTEM	-	-	-	SCKDIVCR2	System Clock Division Control Register 2	0x024	8	read/ write	0x40	0xFF
SYSTEM	-	-	-	SCKSCR	System Clock Source Control Register	0x026	8	read/ write	0x01	0xFF
SYSTEM	-	-	-	PLLCCR	PLL Clock Control Register	0x028	16	read/ write	0x1300	0xFFFF
SYSTEM	-	-	-	PLLCR	PLL Control Register	0x02A	8	read/ write	0x01	0xFF
SYSTEM	-	-	-	BCKCR	External Bus Clock Control Register	0x030	8	read/ write	0x00	0xFF
SYSTEM	-	-	-	MOSCCR	Main Clock Oscillator Control Register	0x032	8	read/ write	0x01	0xFF
SYSTEM	-	-	-	HOCOCR	High-Speed On-Chip Oscillator Control Register	0x036	8	read/ write	0x00	0xFE
SYSTEM	-	-	-	MOCOCR	Middle-Speed On-Chip Oscillator Control Register	0x038	8	read/ write	0x00	0xFF
SYSTEM	-	-	-	FLLCR1	FLL Control Register 1	0x039	8	read/ write	0x00	0xFF

Table 3.3 注册描述（5/44）

周边暗淡		昏暗的增量。	暗淡索引寄存器名称		Description	地址偏移	尺寸	访问	重置值	重置蒙版
DTC	-	-	-	DTCVBR	DTC向量基址寄存器	0x04	32	read/ write	0x00000000	0xFFFFFFFF
DTC	-	-	-	DTCST	DTC模块启动寄存器	0x0C	8	read/ write	0x00	0xFF
DTC	-	-	-	DTCSTS	DTC状态寄存器	0x0E	16	只读	0x0000	0xFFFF
ICU	16	0x1	0-15	IRQCR%s	IRQ控制寄存器%s	0x000	8	read/ write	0x00	0xFF
ICU	-	-	-	NMICR	NMI引脚中断控制 Register	0x100	8	read/ write	0x00	0xFF
ICU	-	-	-	NMIER	Non-Maskable Interrupt 启用注册	0x120	16	read/ write	0x0000	0xFFFF
ICU	-	-	-	NMICLR	Non-Maskable Interrupt 状态清除寄存器	0x130	16	只写	0x0000	0xFFFF
ICU	-	-	-	NMISR	Non-Maskable Interrupt 状态寄存器	0x140	16	只读	0x0000	0xFFFF
ICU	-	-	-	WUPEN	唤醒中断使能寄存器	0x1A0	32	read/ write	0x00000000	0xFFFFFFFF
ICU	-	-	-	SELSR0	要取消的事件选择 贪睡模式	0x200	16	read/ write	0x0000	0xFFFF
ICU	8	0x4	0-7	DELSR%s	DMAC事件链接设置 Register %s	0x280	32	read/ write	0x00000000	0xFFFFFFFF
ICU	96	0x4	0-95	IELSR%s	INT事件链接设置 Register %s	0x300	32	read/ write	0x00000000	0xFFFFFFFF
DBG	-	-	-	DBGSTR	调试状态寄存器	0x000	32	只读	0x00000000	0xFFFFFFFF
DBG	-	-	-	DBGSTOPCR	调试停止控制寄存器0x	010	32	read/ write	0x00000003	0xFFFFFFFF
DBG	-	-	-	TRACECTR	跟踪控制寄存器	0x020	32	read/ write	0x00000000	0xFFFFFFFF
FCACHE	-	-	-	FCACHEE	闪存缓存启用 Register	0x100	16	read/ write	0x0000	0xFFFF
FCACHE	-	-	-	FCACHEIV	闪存缓存失效 Register	0x104	16	read/ write	0x0000	0xFFFF
FCACHE	-	-	-	FLWT	闪存等待周期寄存器	0x11C	8	read/ write	0x00	0xFF
SYSTEM	-	-	-	SBYCR	待机控制寄存器	0x00C	16	read/ write	0x4000	0xFFFF
SYSTEM	-	-	-	MSTPCRA	模块停止控制 Register A	0x01C	32	read/ write	0xFFBFFF1C	0xFFFFFFFF
SYSTEM	-	-	-	SCKDIVCR	系统时钟划分 控制寄存器	0x020	32	read/ write	0x22022222	0xFFFFFFFF
SYSTEM	-	-	-	SCKDIVCR2	系统时钟划分 控制寄存器2	0x024	8	read/ write	0x40	0xFF
SYSTEM	-	-	-	SCKSCR	系统时钟源 控制寄存器	0x026	8	read/ write	0x01	0xFF
SYSTEM	-	-	-	PLLCCR	PLL时钟控制寄存器	0x028	16	read/ write	0x1300	0xFFFF
SYSTEM	-	-	-	PLLCR	锁相环控制寄存器	0x02A	8	read/ write	0x01	0xFF
SYSTEM	-	-	-	BCKCR	外部总线时钟控制 Register	0x030	8	read/ write	0x00	0xFF
SYSTEM	-	-	-	MOSCCR	主时钟振荡器控制 Register	0x032	8	read/ write	0x01	0xFF
SYSTEM	-	-	-	HOCOCR	High-Speed On-Chip 振荡器控制寄存器	0x036	8	read/ write	0x00	0xFE
SYSTEM	-	-	-	MOCOCR	Middle-Speed On-Chip 振荡器控制寄存器	0x038	8	read/ write	0x00	0xFF
SYSTEM	-	-	-	FLLCR1	FLL控制寄存器1	0x039	8	read/ write	0x00	0xFF

Table 3.3 Register description (6 of 44)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
SYSTEM	-	-	-	FLLCR2	FLL Control Register 2	0x03A	16	read/ write	0x0000	0xFFFF
SYSTEM	-	-	-	OSCSF	Oscillation Stabilization Flag Register	0x03C	8	read-only	0x00	0xFE
SYSTEM	-	-	-	CKOCR	Clock Out Control Register	0x03E	8	read/ write	0x00	0xFF
SYSTEM	-	-	-	TRCKCR	Trace Clock Control Register	0x03F	8	read/ write	0x01	0xFF
SYSTEM	-	-	-	OSTDCR	Oscillation Stop Detection Control Register	0x040	8	read/ write	0x00	0xFF
SYSTEM	-	-	-	OSTDSR	Oscillation Stop Detection Status Register	0x041	8	read/ write	0x00	0xFF
SYSTEM	-	-	-	EBCKOCR	External Bus Clock Output Control Register	0x052	8	read/ write	0x00	0xFF
SYSTEM	-	-	-	SDCKOCR	SDRAM Clock Output Control Register	0x053	8	read/ write	0x00	0xFF
SYSTEM	-	-	-	MOCOUTCR	MOCO User Trimming Control Register	0x061	8	read/ write	0x00	0xFF
SYSTEM	-	-	-	HOCOUTCR	HOCO User Trimming Control Register	0x062	8	read/ write	0x00	0xFF
SYSTEM	-	-	-	SNZCR	Snooze Control Register	0x092	8	read/ write	0x00	0xFF
SYSTEM	-	-	-	SNZEDCR	Snooze End Control Register	0x094	8	read/ write	0x00	0xFF
SYSTEM	-	-	-	SNZREQCR	Snooze Request Control Register	0x098	32	read/ write	0x00000000	0xFFFFFFFF
SYSTEM	-	-	-	OPCCR	Operating Power Control Register	0x0A0	8	read/ write	0x00	0xFF
SYSTEM	-	-	-	MOSCWTCR	Main Clock Oscillator Wait Control Register	0x0A2	8	read/ write	0x05	0xFF
SYSTEM	-	-	-	HOCOWTCR	High-speed on-chip oscillator wait control register	0x0A5	8	read/ write	0x02	0xFF
SYSTEM	-	-	-	SOPCCR	Sub Operating Power Control Register	0x0AA	8	read/ write	0x00	0xFF
SYSTEM	-	-	-	RSTSR1	Reset Status Register 1	0x0C0	16	read/ write	0x0000	0xE0F8
SYSTEM	2	0x2	1,2	LVD%sCR1	Voltage Monitor %s Circuit Control Register 1	0x0E0	8	read/ write	0x01	0xFF
SYSTEM	2	0x2	1,2	LVD%sSR	Voltage Monitor %s Circuit Status Register	0x0E1	8	read/ write	0x02	0xFF
SYSTEM	-	-	-	PRCR	Protect Register	0x3FE	16	read/ write	0x0000	0xFFFF
SYSTEM	-	-	-	DPSBYCR	Deep Standby Control Register	0x400	8	read/ write	0x01	0xFF
SYSTEM	-	-	-	DPSIER0	Deep Standby Interrupt Enable Register 0	0x402	8	read/ write	0x00	0xFF
SYSTEM	-	-	-	DPSIER1	Deep Standby Interrupt Enable Register 1	0x403	8	read/ write	0x00	0xFF
SYSTEM	-	-	-	DPSIER2	Deep Standby Interrupt Enable Register 2	0x404	8	read/ write	0x00	0xFF
SYSTEM	-	-	-	DPSIER3	Deep Standby Interrupt Enable Register 3	0x405	8	read/ write	0x00	0xFF
SYSTEM	-	-	-	DPSIFR0	Deep Standby Interrupt Flag Register 0	0x406	8	read/ write	0x00	0xFF
SYSTEM	-	-	-	DPSIFR1	Deep Standby Interrupt Flag Register 1	0x407	8	read/ write	0x00	0xFF
SYSTEM	-	-	-	DPSIFR2	Deep Standby Interrupt Flag Register 2	0x408	8	read/ write	0x00	0xFF
SYSTEM	-	-	-	DPSIFR3	Deep Standby Interrupt Flag Register 3	0x409	8	read/ write	0x00	0xFF

Table 3.3 寄存器描述（6/44）

周边暗淡	昏暗的增量。	暗淡索引寄存器名称		Description	地址偏移	尺寸访问		重置值	重置蒙版
SYSTEM	-	-	FLLCR2	FLL控制寄存器2	0x03A	16	read/ write	0x0000	0xFFFF
SYSTEM	-	-	OSCSF	振荡稳定标志 Register	0x03C	8	只读	0x00	0xFE
SYSTEM	-	-	CKOCR	时钟输出控制寄存器	0x03E	8	read/ write	0x00	0xFF
SYSTEM	-	-	TRCKCR	跟踪时钟控制寄存器0x	03F	8	read/ write	0x01	0xFF
SYSTEM	-	-	OSTDCR	振荡停止检测 控制寄存器	0x040	8	read/ write	0x00	0xFF
SYSTEM	-	-	OSTDSR	振荡停止检测 状态寄存器	0x041	8	read/ write	0x00	0xFF
SYSTEM	-	-	EBCKOCR	外部总线时钟输出 控制寄存器	0x052	8	read/ write	0x00	0xFF
SYSTEM	-	-	SDCKOCR	SDRAM时钟输出 控制寄存器	0x053	8	read/ write	0x00	0xFF
SYSTEM	-	-	MOCOUTCR	MOCO用户修整 控制寄存器	0x061	8	read/ write	0x00	0xFF
SYSTEM	-	-	HOCOUTCR	HOCO用户修整 控制寄存器	0x062	8	read/ write	0x00	0xFF
SYSTEM	-	-	SNZCR	贪睡控制寄存器	0x092	8	read/ write	0x00	0xFF
SYSTEM	-	-	SNZEDCR	贪睡结束控制寄存器0x	094	8	read/ write	0x00	0xFF
SYSTEM	-	-	SNZREQCR	贪睡请求控制 Register	0x098	32	read/ write	0x00000000	0xFFFFFFFF
SYSTEM	-	-	OPCCR	工作功率控制 Register	0x0A0	8	read/ write	0x00	0xFF
SYSTEM	-	-	MOSCWTCR	主时钟振荡器等待 控制寄存器	0x0A2	8	read/ write	0x05	0xFF
SYSTEM	-	-	HOCOWTCR	高速内部振荡器等待控制寄存器	0x0A5	8	read/ write	0x02	0xFF
SYSTEM	-	-	SOPCCR	副作业功率 控制寄存器	0x0AA	8	read/ write	0x00	0xFF
SYSTEM	-	-	RSTSR1	复位状态寄存器1	0x0C0	16	read/ write	0x0000	0xE0F8
SYSTEM	2	0x2	1,2	LVD%sCR1	电压监视器%s电路 控制寄存器1	0x0E0	8	read/ write	0x01	0xFF
SYSTEM	2	0x2	1,2	LVD%sSR	电压监视器%s电路 状态寄存器	0x0E1	8	read/ write	0x02	0xFF
SYSTEM	-	-	-	PRCR	保护寄存器	0x3FE	16	read/ write	0x0000	0xFFFF
SYSTEM	-	-	-	DPSBYCR	深度待机控制 Register	0x400	8	read/ write	0x01	0xFF
SYSTEM	-	-	-	DPSIER0	深度待机中断 启用寄存器0	0x402	8	read/ write	0x00	0xFF
SYSTEM	-	-	-	DPSIER1	深度待机中断 启用寄存器1	0x403	8	read/ write	0x00	0xFF
SYSTEM	-	-	-	DPSIER2	深度待机中断 启用寄存器2	0x404	8	read/ write	0x00	0xFF
SYSTEM	-	-	-	DPSIER3	深度待机中断 启用寄存器3	0x405	8	read/ write	0x00	0xFF
SYSTEM	-	-	-	DPSIFR0	深度待机中断标志 Register 0	0x406	8	read/ write	0x00	0xFF
SYSTEM	-	-	-	DPSIFR1	深度待机中断标志 Register 1	0x407	8	read/ write	0x00	0xFF
SYSTEM	-	-	-	DPSIFR2	深度待机中断标志 Register 2	0x408	8	read/ write	0x00	0xFF
SYSTEM	-	-	-	DPSIFR3	深度待机中断标志 Register 3	0x409	8	read/ write	0x00	0xFF

Table 3.3 Register description (7 of 44)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
SYSTEM	-	-	-	DPSIEGR0	Deep Standby Interrupt Edge Register 0	0x40A	8	read/ write	0x00	0xFF
SYSTEM	-	-	-	DPSIEGR1	Deep Standby Interrupt Edge Register 1	0x40B	8	read/ write	0x00	0xFF
SYSTEM	-	-	-	DPSIEGR2	Deep Standby Interrupt Edge Register 2	0x40C	8	read/ write	0x00	0xFF
SYSTEM	-	-	-	SYOCDCR	System Control OCD Control Register	0x40E	8	read/ write	0x00	0xFE
SYSTEM	-	-	-	STCONR	Standby Condition Register	0x40F	8	read/ write	0xC3	0xFF
SYSTEM	-	-	-	RSTSR0	Reset Status Register 0	0x410	8	read/ write	0x00	0x70
SYSTEM	-	-	-	RSTSR2	Reset Status Register 2	0x411	8	read/ write	0x00	0xFE
SYSTEM	-	-	-	MOMCR	Main Clock Oscillator Mode Oscillation Control Register	0x413	8	read/ write	0x00	0xFF
SYSTEM	-	-	-	FWEPROR	Flash P/E Protect Register	0x416	8	read/ write	0x02	0xFF
SYSTEM	-	-	-	LVCMPCR	Voltage Monitor Circuit Control Register	0x417	8	read/ write	0x00	0xFF
SYSTEM	-	-	-	LVDLVLR	Voltage Detection Level Select Register	0x418	8	read/ write	0xF3	0xFF
SYSTEM	2	0x1	1,2	LVD%sCR0	Voltage Monitor %s Circuit Control Register 0	0x41A	8	read/ write	0x8A	0xF7
SYSTEM	-	-	-	SOSCCR	Sub-clock oscillator control register	0x480	8	read/ write	0x00	0xFF
SYSTEM	-	-	-	SOMCR	Sub Clock Oscillator Mode Control Register	0x481	8	read/ write	0x00	0xFD
SYSTEM	-	-	-	LOCOCR	Low-Speed On-Chip Oscillator Control Register	0x490	8	read/ write	0x00	0xFF
SYSTEM	-	-	-	LOCOUTCR	LOCO User Trimming Control Register	0x492	8	read/ write	0x00	0xFF
SYSTEM	-	-	-	VBTICTLR	VBATT Input Control Register	0x4BB	8	read/ write	0x00	0xF8
SYSTEM	512	0x1	0-511	VBTBKR[%s]	VBATT Backup Register [%s]	0x500	8	read/ write	0x00	0x00
PORT0,5-9,A,B	-	-	-	PCNTR1	Port Control Register 1	0x00	32	read/ write	0x00000000	0xFFFFFFFF
PORT0,5-9,A,B	-	-	-	PODR	Output data register	0x00	16	read/ write	0x0000	0xFFFF
PORT0,5-9,A,B	-	-	-	PDR	Data direction register	0x02	16	read/ write	0x0000	0xFFFF
PORT0,5-9,A,B	-	-	-	PCNTR2	Port Control Register 2	0x04	32	read-only	0x00000000	0xFFFF0000
PORT0,5-9,A,B	-	-	-	PIDR	Input data register	0x06	16	read-only	0x0000	0x0000
PORT0,5-9,A,B	-	-	-	PCNTR3	Port Control Register 3	0x08	32	write-only	0x00000000	0xFFFFFFFF
PORT0,5-9,A,B	-	-	-	PORR	Output reset register	0x08	16	write-only	0x0000	0xFFFF
PORT0,5-9,A,B	-	-	-	POSR	Output set register	0x0A	16	write-only	0x0000	0xFFFF
PORT1-4	-	-	-	PCNTR1	Port Control Register 1	0x00	32	read/ write	0x00000000	0xFFFFFFFF
PORT1-4	-	-	-	PODR	Output data register	0x00	16	read/ write	0x0000	0xFFFF
PORT1-4	-	-	-	PDR	Data direction register	0x02	16	read/ write	0x0000	0xFFFF
PORT1-4	-	-	-	PCNTR2	Port Control Register 2	0x04	32	read-only	0x00000000	0xFFFF0000

Table 3.3 寄存器说明（44个中的7个）

周边暗淡		昏暗的增量。	暗淡索引寄存器名称		Description	地址偏移	尺寸	访问	重置值	重置蒙版
SYSTEM	-	-	-	DPSIEGR0	深度待机中断边缘 Register 0	0x40A	8	read/ write	0x00	0xFF
SYSTEM	-	-	-	DPSIEGR1	深度待机中断边缘 Register 1	0x40B	8	read/ write	0x00	0xFF
SYSTEM	-	-	-	DPSIEGR2	深度待机中断边缘 Register 2	0x40C	8	read/ write	0x00	0xFF
SYSTEM	-	-	-	SYOCDCR	系统控制OCD控制 Register	0x40E	8	read/ write	0x00	0xFE
SYSTEM	-	-	-	STCONR	待机状态寄存器	0x40F	8	read/ write	0xC3	0xFF
SYSTEM	-	-	-	RSTSR0	复位状态寄存器0	0x410	8	read/ write	0x00	0x70
SYSTEM	-	-	-	RSTSR2	复位状态寄存器2	0x411	8	read/ write	0x00	0xFE
SYSTEM	-	-	-	MOMCR	主时钟振荡器模式振荡控制寄存器	0x413	8	read/ write	0x00	0xFF
SYSTEM	-	-	-	FWEPROR	FlashPE保护寄存器	0x416	8	read/ write	0x02	0xFF
SYSTEM	-	-	-	LVCMPCR	电压监控电路 控制寄存器	0x417	8	read/ write	0x00	0xFF
SYSTEM	-	-	-	LVDLVLR	电压检测电平 选择注册	0x418	8	read/ write	0xF3	0xFF
SYSTEM	2	0x1	1,2	LVD%sCR0	电压监视器%s电路 控制寄存器0	0x41A	8	read/ write	0x8A	0xF7
SYSTEM	-	-	-	SOSCCR	副时钟振荡器控制寄存器	0x480	8	read/ write	0x00	0xFF
SYSTEM	-	-	-	SOMCR	副时钟振荡器模式 控制寄存器	0x481	8	read/ write	0x00	0xFD
SYSTEM	-	-	-	LOCOCR	Low-Speed On-Chip 振荡器控制寄存器	0x490	8	read/ write	0x00	0xFF
SYSTEM	-	-	-	LOCOUTCR	LOCO用户修整 控制寄存器	0x492	8	read/ write	0x00	0xFF
SYSTEM	-	-	-	VBTICTLR	VBATT输入控制 Register	0x4BB	8	read/ write	0x00	0xF8
SYSTEM	512	0x1	0-511	VBTBKR[%s]	VBATT备份寄存器[%s]	0x500	8	read/ write	0x00	0x00
PORT0,5-9,A,B	-	-	-	PCNTR1	端口控制寄存器1	0x00	32	read/ write	0x00000000	0xFFFFFFFF
PORT0,5-9,A,B	-	-	-	PODR	输出数据寄存器	0x00	16	read/ write	0x0000	0xFFFF
PORT0,5-9,A,B	-	-	-	PDR	数据方向寄存器	0x02	16	read/ write	0x0000	0xFFFF
PORT0,5-9,A,B	-	-	-	PCNTR2	端口控制寄存器2	0x04	32	只读	0x00000000	0xFFFF0000
PORT0,5-9,A,B	-	-	-	PIDR	输入数据寄存器	0x06	16	只读	0x0000	0x0000
PORT0,5-9,A,B	-	-	-	PCNTR3	端口控制寄存器3	0x08	32	只写	0x00000000	0xFFFFFFFF
PORT0,5-9,A,B	-	-	-	PORR	输出复位寄存器	0x08	16	只写	0x0000	0xFFFF
PORT0,5-9,A,B	-	-	-	POSR	输出设置寄存器	0x0A	16	只写	0x0000	0xFFFF
PORT1-4	-	-	-	PCNTR1	端口控制寄存器1	0x00	32	read/ write	0x00000000	0xFFFFFFFF
PORT1-4	-	-	-	PODR	输出数据寄存器	0x00	16	read/ write	0x0000	0xFFFF
PORT1-4	-	-	-	PDR	数据方向寄存器	0x02	16	read/ write	0x0000	0xFFFF
PORT1-4	-	-	-	PCNTR2	端口控制寄存器2	0x04	32	只读	0x00000000	0xFFFF0000

Table 3.3 Register description (8 of 44)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
PORT1-4	-	-	-	EIDR	Event input data register	0x04	16	read-only	0x0000	0x0000
PORT1-4	-	-	-	PIDR	Input data register	0x06	16	read-only	0x0000	0xFFFF
PORT1-4	-	-	-	PCNTR3	Port Control Register 3	0x08	32	write-only	0x00000000	0xFFFFFFFF
PORT1-4	-	-	-	PORR	Output set register	0x08	16	write-only	0x0000	0xFFFF
PORT1-4	-	-	-	POSR	Output reset register	0x0A	16	write-only	0x0000	0xFFFF
PORT1-4	-	-	-	PCNTR4	Port Control Register 4	0x0C	32	read/write	0x00000000	0xFFFFFFFF
PORT1-4	-	-	-	EORR	Event output set register	0x0C	16	read/write	0x0000	0xFFFF
PORT1-4	-	-	-	EOSR	Event output reset register	0x0E	16	read/write	0x0000	0xFFFF
PFS	-	-	-	P000PFS	P000 Pin Function Control Register	0x000	32	read/write	0x00008000	0xFFFFFFFF
PFS	-	-	-	P000PFS_HA	P000 Pin Function Control Register	0x002	16	read/write	0x8000	0xFFFF
PFS	-	-	-	P000PFS_BY	P000 Pin Function Control Register	0x003	8	read/write	0x00	0xFF
PFS	7	0x4	1-7	P00%sPFS	P00%s Pin Function Control Register	0x004	32	read/write	0x00008000	0xFFFFFFFF
PFS	7	0x4	1-7	P00%sPFS_HA	P00%s Pin Function Control Register	0x006	16	read/write	0x8000	0xFFFF
PFS	7	0x4	1-7	P00%sPFS_BY	P00%s Pin Function Control Register	0x007	8	read/write	0x00	0xFF
PFS	2	0x4	8-9	P00%sPFS	P00%s Pin Function Control Register	0x020	32	read/write	0x00000000	0xFFFFFFFF
PFS	2	0x4	8-9	P00%sPFS_HA	P00%s Pin Function Control Register	0x022	16	read/write	0x0000	0xFFFF
PFS	2	0x4	8-9	P00%sPFS_BY	P00%s Pin Function Control Register	0x023	8	read/write	0x00	0xFF
PFS	6	0x4	10-15	P0%sPFS	P0%s Pin Function Control Register	0x028	32	read/write	0x00000000	0xFFFFFFFF
PFS	6	0x4	10-15	P0%sPFS_HA	P0%s Pin Function Control Register	0x02A	16	read/write	0x0000	0xFFFF
PFS	6	0x4	10-15	P0%sPFS_BY	P0%s Pin Function Control Register	0x02B	8	read/write	0x00	0xFF
PFS	-	-	-	P100PFS	P100 Pin Function Control Register	0x040	32	read/write	0x00000000	0xFFFFFFFF
PFS	-	-	-	P100PFS_HA	P100 Pin Function Control Register	0x042	16	read/write	0x0000	0xFFFF
PFS	-	-	-	P100PFS_BY	P100 Pin Function Control Register	0x043	8	read/write	0x00	0xFF
PFS	7	0x4	1-7	P10%sPFS	P10%s Pin Function Control Register	0x044	32	read/write	0x00000000	0xFFFFFFFF
PFS	7	0x4	1-7	P10%sPFS_HA	P10%s Pin Function Control Register	0x046	16	read/write	0x0000	0xFFFF
PFS	7	0x4	1-7	P10%sPFS_BY	P10%s Pin Function Control Register	0x047	8	read/write	0x00	0xFF
PFS	-	-	-	P108PFS	P108 Pin Function Control Register	0x060	32	read/write	0x00010410	0xFFFFFFFF
PFS	-	-	-	P108PFS_HA	P108 Pin Function Control Register	0x062	16	read/write	0x0410	0xFFFF
PFS	-	-	-	P108PFS_BY	P108 Pin Function Control Register	0x063	8	read/write	0x10	0xFF
PFS	-	-	-	P109PFS	P109 Pin Function Control Register	0x064	32	read/write	0x00010410	0xFFFFFFFF

Table 3.3 寄存器说明（44个中的8个）

周边暗淡	昏暗的增量。	暗淡索引寄存器名称		Description	地址偏移	尺寸	访问	重置值	重置蒙版
PORT1-4	-	-	-	EIDR	事件输入数据寄存器	0x04	16	只读	0x0000	0x0000
PORT1-4	-	-	-	PIDR	输入数据寄存器	0x06	16	只读	0x0000	0xFFFF
PORT1-4	-	-	-	PCNTR3	端口控制寄存器3	0x08	32	只写	0x00000000	0xFFFFFFFF
PORT1-4	-	-	-	PORR	输出设置寄存器	0x08	16	只写	0x0000	0xFFFF
PORT1-4	-	-	-	POSR	输出复位寄存器	0x0A	16	只写	0x0000	0xFFFF
PORT1-4	-	-	-	PCNTR4	端口控制寄存器4	0x0C	32	read/write	0x00000000	0xFFFFFFFF
PORT1-4	-	-	-	EORR	事件输出设置寄存器	0x0C	16	read/write	0x0000	0xFFFF
PORT1-4	-	-	-	EOSR	事件输出复位寄存器	0x0E	16	read/write	0x0000	0xFFFF
PFS	-	-	-	P000PFS	P000引脚功能控制Register	0x000	32	read/write	0x00008000	0xFFFFFFFF
PFS	-	-	-	P000PFS_HA	P000引脚功能控制Register	0x002	16	read/write	0x8000	0xFFFF
PFS	-	-	-	P000PFS_BY	P000引脚功能控制Register	0x003	8	read/write	0x00	0xFF
PFS	7	0x4	1-7	P00%sPFS	P00%s引脚功能控制Register	0x004	32	read/write	0x00008000	0xFFFFFFFF
PFS	7	0x4	1-7	P00%sPFS_HA	P00%s引脚功能控制Register	0x006	16	read/write	0x8000	0xFFFF
PFS	7	0x4	1-7	P00%sPFS_BY	P00%s引脚功能控制Register	0x007	8	read/write	0x00	0xFF
PFS	2	0x4	8-9	P00%sPFS	P00%s引脚功能控制Register	0x020	32	read/write	0x00000000	0xFFFFFFFF
PFS	2	0x4	8-9	P00%sPFS_HA	P00%s引脚功能控制Register	0x022	16	read/write	0x0000	0xFFFF
PFS	2	0x4	8-9	P00%sPFS_BY	P00%s引脚功能控制Register	0x023	8	read/write	0x00	0xFF
PFS	6	0x4	10-15	P0%sPFS	P0%s引脚功能控制Register	0x028	32	read/write	0x00000000	0xFFFFFFFF
PFS	6	0x4	10-15	P0%sPFS_HA	P0%s引脚功能控制Register	0x02A	16	read/write	0x0000	0xFFFF
PFS	6	0x4	10-15	P0%sPFS_BY	P0%s引脚功能控制Register	0x02B	8	read/write	0x00	0xFF
PFS	-	-	-	P100PFS	P100引脚功能控制Register	0x040	32	read/write	0x00000000	0xFFFFFFFF
PFS	-	-	-	P100PFS_HA	P100引脚功能控制Register	0x042	16	read/write	0x0000	0xFFFF
PFS	-	-	-	P100PFS_BY	P100引脚功能控制Register	0x043	8	read/write	0x00	0xFF
PFS	7	0x4	1-7	P10%sPFS	P10%s引脚功能控制Register	0x044	32	read/write	0x00000000	0xFFFFFFFF
PFS	7	0x4	1-7	P10%sPFS_HA	P10%s引脚功能控制Register	0x046	16	read/write	0x0000	0xFFFF
PFS	7	0x4	1-7	P10%sPFS_BY	P10%s引脚功能控制Register	0x047	8	read/write	0x00	0xFF
PFS	-	-	-	P108PFS	P108引脚功能控制Register	0x060	32	read/write	0x00010410	0xFFFFFFFF
PFS	-	-	-	P108PFS_HA	P108引脚功能控制Register	0x062	16	read/write	0x0410	0xFFFF
PFS	-	-	-	P108PFS_BY	P108引脚功能控制Register	0x063	8	read/write	0x10	0xFF
PFS	-	-	-	P109PFS	P109引脚功能控制Register	0x064	32	read/write	0x00010410	0xFFFFFFFF

Table 3.3 Register description (9 of 44)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
PFS	-	-	-	P109PFS_HA	P109 Pin Function Control Register	0x066	16	read/ write	0x0410	0xFFFF
PFS	-	-	-	P109PFS_BY	P109 Pin Function Control Register	0x067	8	read/ write	0x10	0xFF
PFS	-	-	-	P110PFS	P110 Pin Function Control Register	0x068	32	read/ write	0x00010010	0xFFFFFFFF
PFS	-	-	-	P110PFS_HA	P110 Pin Function Control Register	0x06A	16	read/ write	0x0010	0xFFFF
PFS	-	-	-	P110PFS_BY	P110 Pin Function Control Register	0x06B	8	read/ write	0x10	0xFF
PFS	5	0x4	11-15	P1%sPFS	P1%s Pin Function Control Register	0x06C	32	read/ write	0x00000000	0xFFFFFFFF
PFS	5	0x4	11-15	P1%sPFS_HA	P1%s Pin Function Control Register	0x06E	16	read/ write	0x0000	0xFFFF
PFS	5	0x4	11-15	P1%sPFS_BY	P1%s Pin Function Control Register	0x06F	8	read/ write	0x00	0xFF
PFS	-	-	-	P200PFS	P200 Pin Function Control Register	0x080	32	read/ write	0x00000000	0xFFFFFFFF
PFS	-	-	-	P200PFS_HA	P200 Pin Function Control Register	0x082	16	read/ write	0x0000	0xFFFF
PFS	-	-	-	P200PFS_BY	P200 Pin Function Control Register	0x083	8	read/ write	0x00	0xFF
PFS	-	-	-	P201PFS	P201 Pin Function Control Register	0x084	32	read/ write	0x00000010	0xFFFFFFFF
PFS	-	-	-	P201PFS_HA	P201 Pin Function Control Register	0x086	16	read/ write	0x0010	0xFFFF
PFS	-	-	-	P201PFS_BY	P201 Pin Function Control Register	0x087	8	read/ write	0x10	0xFF
PFS	8	0x4	2-9	P20%sPFS	P20%s Pin Function Control Register	0x088	32	read/ write	0x00000000	0xFFFFFFFF
PFS	8	0x4	2-9	P20%sPFS_HA	P20%s Pin Function Control Register	0x08A	16	read/ write	0x0000	0xFFFF
PFS	8	0x4	2-9	P20%sPFS_BY	P20%s Pin Function Control Register	0x08B	8	read/ write	0x00	0xFF
PFS	6	0x4	10-15	P2%sPFS	P2%s Pin Function Control Register	0x0A8	32	read/ write	0x00000000	0xFFFFFFFF
PFS	6	0x4	10-15	P2%sPFS_HA	P2%s Pin Function Control Register	0x0AA	16	read/ write	0x0000	0xFFFF
PFS	6	0x4	10-15	P2%sPFS_BY	P2%s Pin Function Control Register	0x0AB	8	read/ write	0x00	0xFF
PFS	-	-	-	P300PFS	P300 Pin Function Control Register	0x0C0	32	read/ write	0x00010010	0xFFFFFFFF
PFS	-	-	-	P300PFS_HA	P300 Pin Function Control Register	0x0C2	16	read/ write	0x0010	0xFFFF
PFS	-	-	-	P300PFS_BY	P300 Pin Function Control Register	0x0C3	8	read/ write	0x10	0xFF
PFS	9	0x4	1-9	P30%sPFS	P30%s Pin Function Control Register	0x0C4	32	read/ write	0x00000000	0xFFFFFFFF
PFS	9	0x4	1-9	P30%sPFS_HA	P30%s Pin Function Control Register	0x0C6	16	read/ write	0x0000	0xFFFF
PFS	9	0x4	1-9	P30%sPFS_BY	P30%s Pin Function Control Register	0x0C7	8	read/ write	0x00	0xFF
PFS	6	0x4	10-15	P3%sPFS	P3%s Pin Function Control Register	0x0E8	32	read/ write	0x00000000	0xFFFFFFFF
PFS	6	0x4	10-15	P3%sPFS_HA	P30%s Pin Function Control Register	0x0EA	16	read/ write	0x0000	0xFFFF
PFS	6	0x4	10-15	P3%sPFS_BY	P30%s Pin Function Control Register	0x0EB	8	read/ write	0x00	0xFF
PFS	10	0x4	0-9	P40%sPFS	P40%s Pin Function Control Register	0x100	32	read/ write	0x00000000	0xFFFFFFFF

Table 3.3 寄存器说明（44个中的9个）

周边暗淡		昏暗的增量。	暗淡索引寄存器名称		Description	地址偏移	尺寸	访问	重置值	重置蒙版
PFS	-	-	-	P109PFS_HA	P109引脚功能控制 Register	0x066	16	read/ write	0x0410	0xFFFF
PFS	-	-	-	P109PFS_BY	P109引脚功能控制 Register	0x067	8	read/ write	0x10	0xFF
PFS	-	-	-	P110PFS	P110引脚功能控制 Register	0x068	32	read/ write	0x00010010	0xFFFFFFFF
PFS	-	-	-	P110PFS_HA	P110引脚功能控制 Register	0x06A	16	read/ write	0x0010	0xFFFF
PFS	-	-	-	P110PFS_BY	P110引脚功能控制 Register	0x06B	8	read/ write	0x10	0xFF
PFS	5	0x4	11-15	P1%sPFS	P1%s引脚功能控制 Register	0x06C	32	read/ write	0x00000000	0xFFFFFFFF
PFS	5	0x4	11-15	P1%sPFS_HA	P1%s引脚功能控制 Register	0x06E	16	read/ write	0x0000	0xFFFF
PFS	5	0x4	11-15	P1%sPFS_BY	P1%s引脚功能控制 Register	0x06F	8	read/ write	0x00	0xFF
PFS	-	-	-	P200PFS	P200引脚功能控制 Register	0x080	32	read/ write	0x00000000	0xFFFFFFFF
PFS	-	-	-	P200PFS_HA	P200引脚功能控制 Register	0x082	16	read/ write	0x0000	0xFFFF
PFS	-	-	-	P200PFS_BY	P200引脚功能控制 Register	0x083	8	read/ write	0x00	0xFF
PFS	-	-	-	P201PFS	P201引脚功能控制 Register	0x084	32	read/ write	0x00000010	0xFFFFFFFF
PFS	-	-	-	P201PFS_HA	P201引脚功能控制 Register	0x086	16	read/ write	0x0010	0xFFFF
PFS	-	-	-	P201PFS_BY	P201引脚功能控制 Register	0x087	8	read/ write	0x10	0xFF
PFS	8	0x4	2-9	P20%sPFS	P20%s引脚功能控制 Register	0x088	32	read/ write	0x00000000	0xFFFFFFFF
PFS	8	0x4	2-9	P20%sPFS_HA	P20%s引脚功能控制 Register	0x08A	16	read/ write	0x0000	0xFFFF
PFS	8	0x4	2-9	P20%sPFS_BY	P20%s引脚功能控制 Register	0x08B	8	read/ write	0x00	0xFF
PFS	6	0x4	10-15	P2%sPFS	P2%s引脚功能控制 Register	0x0A8	32	read/ write	0x00000000	0xFFFFFFFF
PFS	6	0x4	10-15	P2%sPFS_HA	P2%s引脚功能控制 Register	0x0AA	16	read/ write	0x0000	0xFFFF
PFS	6	0x4	10-15	P2%sPFS_BY	P2%s引脚功能控制 Register	0x0AB	8	read/ write	0x00	0xFF
PFS	-	-	-	P300PFS	P300引脚功能控制 Register	0x0C0	32	read/ write	0x00010010	0xFFFFFFFF
PFS	-	-	-	P300PFS_HA	P300引脚功能控制 Register	0x0C2	16	read/ write	0x0010	0xFFFF
PFS	-	-	-	P300PFS_BY	P300引脚功能控制 Register	0x0C3	8	read/ write	0x10	0xFF
PFS	9	0x4	1-9	P30%sPFS	P30%s引脚功能控制 Register	0x0C4	32	read/ write	0x00000000	0xFFFFFFFF
PFS	9	0x4	1-9	P30%sPFS_HA	P30%s引脚功能控制 Register	0x0C6	16	read/ write	0x0000	0xFFFF
PFS	9	0x4	1-9	P30%sPFS_BY	P30%s引脚功能控制 Register	0x0C7	8	read/ write	0x00	0xFF
PFS	6	0x4	10-15	P3%sPFS	P3%s引脚功能控制 Register	0x0E8	32	read/ write	0x00000000	0xFFFFFFFF
PFS	6	0x4	10-15	P3%sPFS_HA	P30%s引脚功能控制 Register	0x0EA	16	read/ write	0x0000	0xFFFF
PFS	6	0x4	10-15	P3%sPFS_BY	P30%s引脚功能控制 Register	0x0EB	8	read/ write	0x00	0xFF
PFS	10	0x4	0-9	P40%sPFS	P40%s引脚功能控制 Register	0x100	32	read/ write	0x00000000	0xFFFFFFFF

Table 3.3 Register description (10 of 44)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
PFS	10	0x4	0-9	P40%sPFS_HA	P40%s Pin Function Control Register	0x102	16	read/ write	0x0000	0xFFFF
PFS	10	0x4	0-9	P40%sPFS_BY	P40%s Pin Function Control Register	0x103	8	read/ write	0x00	0xFF
PFS	6	0x4	10-15	P4%sPFS	P4%s Pin Function Control Register	0x128	32	read/ write	0x00000000	0xFFFFFFFF
PFS	6	0x4	10-15	P4%sPFS_HA	P4%s Pin Function Control Register	0x12A	16	read/ write	0x0000	0xFFFF
PFS	6	0x4	10-15	P4%sPFS_BY	P4%s Pin Function Control Register	0x12B	8	read/ write	0x00	0xFF
PFS	10	0x4	0-9	P50%sPFS	P50%s Pin Function Control Register	0x140	32	read/ write	0x00000000	0xFFFFFFFF
PFS	10	0x4	0-9	P50%sPFS_HA	P50%s Pin Function Control Register	0x142	16	read/ write	0x0000	0xFFFF
PFS	10	0x4	0-9	P50%sPFS_BY	P50%s Pin Function Control Register	0x143	8	read/ write	0x00	0xFF
PFS	6	0x4	10-15	P5%sPFS	P5%s Pin Function Control Register	0x168	32	read/ write	0x00000000	0xFFFFFFFF
PFS	6	0x4	10-15	P5%sPFS_HA	P5%s Pin Function Control Register	0x16A	16	read/ write	0x0000	0xFFFF
PFS	6	0x4	10-15	P5%sPFS_BY	P5%s Pin Function Control Register	0x16B	8	read/ write	0x00	0xFF
PFS	10	0x4	0-9	P60%sPFS	P60%s Pin Function Control Register	0x180	32	read/ write	0x00000000	0xFFFFFFFF
PFS	10	0x4	0-9	P60%sPFS_HA	P60%s Pin Function Control Register	0x182	16	read/ write	0x0000	0xFFFF
PFS	10	0x4	0-9	P60%sPFS_BY	P60%s Pin Function Control Register	0x183	8	read/ write	0x00	0xFF
PFS	6	0x4	10-15	P6%sPFS	P6%s Pin Function Control Register	0x1A8	32	read/ write	0x00000000	0xFFFFFFFF
PFS	6	0x4	10-15	P6%sPFS_HA	P6%s Pin Function Control Register	0x1AA	16	read/ write	0x0000	0xFFFF
PFS	6	0x4	10-15	P6%sPFS_BY	P6%s Pin Function Control Register	0x1AB	8	read/ write	0x00	0xFF
PFS	10	0x4	0-9	P70%sPFS	P70%s Pin Function Control Register	0x1C0	32	read/ write	0x00000000	0xFFFFFFFF
PFS	10	0x4	0-9	P70%sPFS_HA	P70%s Pin Function Control Register	0x1C2	16	read/ write	0x0000	0xFFFF
PFS	10	0x4	0-9	P70%sPFS_BY	P70%s Pin Function Control Register	0x1C3	8	read/ write	0x00	0xFF
PFS	6	0x4	10-15	P7%sPFS	P7%s Pin Function Control Register	0x1E8	32	read/ write	0x00000000	0xFFFFFFFF
PFS	6	0x4	10-15	P7%sPFS_HA	P7%s Pin Function Control Register	0x1EA	16	read/ write	0x0000	0xFFFF
PFS	6	0x4	10-15	P7%sPFS_BY	P7%s Pin Function Control Register	0x1EB	8	read/ write	0x00	0xFF
PFS	10	0x4	0-9	P80%sPFS	P80%s Pin Function Control Register	0x200	32	read/ write	0x00000000	0xFFFFFFFF
PFS	10	0x4	0-9	P80%sPFS_HA	P80%s Pin Function Control Register	0x202	16	read/ write	0x0000	0xFFFF
PFS	10	0x4	0-9	P80%sPFS_BY	P80%s Pin Function Control Register	0x203	8	read/ write	0x00	0xFF
PFS	6	0x4	10-15	P8%sPFS	P8%s Pin Function Control Register	0x228	32	read/ write	0x00000000	0xFFFFFFFF
PFS	6	0x4	10-15	P8%sPFS_HA	P8%s Pin Function Control Register	0x22A	16	read/ write	0x0000	0xFFFF
PFS	6	0x4	10-15	P8%sPFS_BY	P8%s Pin Function Control Register	0x22B	8	read/ write	0x00	0xFF
PFS	10	0x4	0-9	P90%sPFS	P90%s Pin Function Control Register	0x240	32	read/ write	0x00000000	0xFFFFFFFF

Table 3.3 寄存器说明（44个中的10个）

周边暗淡		昏暗的增量。	暗淡索引寄存器名称		Description	地址偏移	尺寸	访问	重置值	重置蒙版
PFS	10	0x4	0-9	P40%sPFS_HA	P40%s引脚功能控制 Register	0x102	16	read/ write	0x0000	0xFFFF
PFS	10	0x4	0-9	P40%sPFS_BY	P40%s引脚功能控制 Register	0x103	8	read/ write	0x00	0xFF
PFS	6	0x4	10-15	P4%sPFS	P4%s引脚功能控制 Register	0x128	32	read/ write	0x00000000	0xFFFFFFFF
PFS	6	0x4	10-15	P4%sPFS_HA	P4%s引脚功能控制 Register	0x12A	16	read/ write	0x0000	0xFFFF
PFS	6	0x4	10-15	P4%sPFS_BY	P4%s引脚功能控制 Register	0x12B	8	read/ write	0x00	0xFF
PFS	10	0x4	0-9	P50%sPFS	P50%s引脚功能控制 Register	0x140	32	read/ write	0x00000000	0xFFFFFFFF
PFS	10	0x4	0-9	P50%sPFS_HA	P50%s引脚功能控制 Register	0x142	16	read/ write	0x0000	0xFFFF
PFS	10	0x4	0-9	P50%sPFS_BY	P50%s引脚功能控制 Register	0x143	8	read/ write	0x00	0xFF
PFS	6	0x4	10-15	P5%sPFS	P5%s引脚功能控制 Register	0x168	32	read/ write	0x00000000	0xFFFFFFFF
PFS	6	0x4	10-15	P5%sPFS_HA	P5%s引脚功能控制 Register	0x16A	16	read/ write	0x0000	0xFFFF
PFS	6	0x4	10-15	P5%sPFS_BY	P5%s引脚功能控制 Register	0x16B	8	read/ write	0x00	0xFF
PFS	10	0x4	0-9	P60%sPFS	P60%s引脚功能控制 Register	0x180	32	read/ write	0x00000000	0xFFFFFFFF
PFS	10	0x4	0-9	P60%sPFS_HA	P60%s引脚功能控制 Register	0x182	16	read/ write	0x0000	0xFFFF
PFS	10	0x4	0-9	P60%sPFS_BY	P60%s引脚功能控制 Register	0x183	8	read/ write	0x00	0xFF
PFS	6	0x4	10-15	P6%sPFS	P6%s引脚功能控制 Register	0x1A8	32	read/ write	0x00000000	0xFFFFFFFF
PFS	6	0x4	10-15	P6%sPFS_HA	P6%s引脚功能控制 Register	0x1AA	16	read/ write	0x0000	0xFFFF
PFS	6	0x4	10-15	P6%sPFS_BY	P6%s引脚功能控制 Register	0x1AB	8	read/ write	0x00	0xFF
PFS	10	0x4	0-9	P70%sPFS	P70%s引脚功能控制 Register	0x1C0	32	read/ write	0x00000000	0xFFFFFFFF
PFS	10	0x4	0-9	P70%sPFS_HA	P70%s引脚功能控制 Register	0x1C2	16	read/ write	0x0000	0xFFFF
PFS	10	0x4	0-9	P70%sPFS_BY	P70%s引脚功能控制 Register	0x1C3	8	read/ write	0x00	0xFF
PFS	6	0x4	10-15	P7%sPFS	P7%s引脚功能控制 Register	0x1E8	32	read/ write	0x00000000	0xFFFFFFFF
PFS	6	0x4	10-15	P7%sPFS_HA	P7%s引脚功能控制 Register	0x1EA	16	read/ write	0x0000	0xFFFF
PFS	6	0x4	10-15	P7%sPFS_BY	P7%s引脚功能控制 Register	0x1EB	8	read/ write	0x00	0xFF
PFS	10	0x4	0-9	P80%sPFS	P80%s引脚功能控制 Register	0x200	32	read/ write	0x00000000	0xFFFFFFFF
PFS	10	0x4	0-9	P80%sPFS_HA	P80%s引脚功能控制 Register	0x202	16	read/ write	0x0000	0xFFFF
PFS	10	0x4	0-9	P80%sPFS_BY	P80%s引脚功能控制 Register	0x203	8	read/ write	0x00	0xFF
PFS	6	0x4	10-15	P8%sPFS	P8%s引脚功能控制 Register	0x228	32	read/ write	0x00000000	0xFFFFFFFF
PFS	6	0x4	10-15	P8%sPFS_HA	P8%s引脚功能控制 Register	0x22A	16	read/ write	0x0000	0xFFFF
PFS	6	0x4	10-15	P8%sPFS_BY	P8%s引脚功能控制 Register	0x22B	8	read/ write	0x00	0xFF
PFS	10	0x4	0-9	P90%sPFS	P90%s引脚功能控制 Register	0x240	32	read/ write	0x00000000	0xFFFFFFFF

Table 3.3 Register description (11 of 44)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
PFS	10	0x4	0-9	P90%sPFS_HA	P90%s Pin Function Control Register	0x242	16	read/ write	0x0000	0xFFFF
PFS	10	0x4	0-9	P90%sPFS_BY	P90%s Pin Function Control Register	0x243	8	read/ write	0x00	0xFF
PFS	6	0x4	10-15	P9%sPFS	P9%s Pin Function Control Register	0x268	32	read/ write	0x00000000	0xFFFFFFFF
PFS	6	0x4	10-15	P9%sPFS_HA	P9%s Pin Function Control Register	0x26A	16	read/ write	0x0000	0xFFFF
PFS	6	0x4	10-15	P9%sPFS_BY	P9%s Pin Function Control Register	0x26B	8	read/ write	0x00	0xFF
PFS	10	0x4	0-9	PA0%sPFS	PA0%s Pin Function Control Register	0x280	32	read/ write	0x00000000	0xFFFFFFFF
PFS	10	0x4	0-9	PA0%sPFS_HA	PA0%s Pin Function Control Register	0x282	16	read/ write	0x0000	0xFFFF
PFS	10	0x4	0-9	PA0%sPFS_BY	PA0%s Pin Function Control Register	0x283	8	read/ write	0x00	0xFF
PFS	6	0x4	10-15	PA%sPFS	PA%s Pin Function Control Register	0x2A8	32	read/ write	0x00000000	0xFFFFFFFF
PFS	6	0x4	10-15	PA%sPFS_HA	PA%s Pin Function Control Register	0x2AA	16	read/ write	0x0000	0xFFFF
PFS	6	0x4	10-15	PA%sPFS_BY	PA%s Pin Function Control Register	0x2AB	8	read/ write	0x00	0xFF
PFS	8	0x4	0-7	PB0%sPFS	PB0%s Pin Function Control Register	0x2C0	32	read/ write	0x00000000	0xFFFFFFFF
PFS	8	0x4	0-7	PB0%sPFS_HA	PB0%s Pin Function Control Register	0x2C2	16	read/ write	0x0000	0xFFFF
PFS	8	0x4	0-7	PB0%sPFS_BY	PB0%s Pin Function Control Register	0x2C3	8	read/ write	0x00	0xFF
PMISC	-	-	-	PFENET	Ethernet Control Register	0x00	8	read/ write	0x00	0xFF
PMISC	-	-	-	PWPR	Write-Protect Register	0x03	8	read/ write	0x80	0xFF
ELC	-	-	-	ELCR	Event Link Controller Register	0x00	8	read/ write	0x00	0xFF
ELC	2	0x2	0,1	ELSEGR%s	Event Link Software Event Generation Register %s	0x02	8	read/ write	0x80	0xFF
ELC	19	0x4	0-18	ELSR%s	Event Link Setting Register %s	0x10	16	read/ write	0x0000	0xFFFF
POEG	4	0x100	A,B,C ,D	POEGG%s	POEG Group %s Setting Register	0x00	32	read/ write	0x00000000	0xFFFFFFFF
RTC	-	-	-	R64CNT	64-Hz Counter	0x00	8	read-only	0x00	0x80
RTC	-	-	-	RSECCNT	Second Counter	0x02	8	read/ write	0x00	0x00
RTC	-	-	-	BCNT0	Binary Counter 0	0x02	8	read/ write	0x00	0x00
RTC	-	-	-	RMINCNT	Minute Counter	0x04	8	read/ write	0x00	0x00
RTC	-	-	-	BCNT1	Binary Counter 1	0x04	8	read/ write	0x00	0x00
RTC	-	-	-	RHRCNT	Hour Counter	0x06	8	read/ write	0x00	0x00
RTC	-	-	-	BCNT2	Binary Counter 2	0x06	8	read/ write	0x00	0x00
RTC	-	-	-	RWKCNT	Day-of-Week Counter	0x08	8	read/ write	0x00	0x00
RTC	-	-	-	BCNT3	Binary Counter 3	0x08	8	read/ write	0x00	0x00
RTC	-	-	-	RDAYCNT	Day Counter	0x0A	8	read/ write	0x00	0xC0

Table 3.3 寄存器说明（44个中的11个）

周边暗淡		昏暗的增量。	暗淡索引寄存器名称		Description	地址偏移	尺寸	访问	重置值	重置蒙版
PFS	10	0x4	0-9	P90%sPFS_HA	P90%s引脚功能控制 Register	0x242	16	read/ write	0x0000	0xFFFF
PFS	10	0x4	0-9	P90%sPFS_BY	P90%s引脚功能控制 Register	0x243	8	read/ write	0x00	0xFF
PFS	6	0x4	10-15	P9%sPFS	P9%s引脚功能控制 Register	0x268	32	read/ write	0x00000000	0xFFFFFFFF
PFS	6	0x4	10-15	P9%sPFS_HA	P9%s引脚功能控制 Register	0x26A	16	read/ write	0x0000	0xFFFF
PFS	6	0x4	10-15	P9%sPFS_BY	P9%s引脚功能控制 Register	0x26B	8	read/ write	0x00	0xFF
PFS	10	0x4	0-9	PA0%sPFS	PA0%s引脚功能控制 Register	0x280	32	read/ write	0x00000000	0xFFFFFFFF
PFS	10	0x4	0-9	PA0%sPFS_HA	PA0%s引脚功能控制 Register	0x282	16	read/ write	0x0000	0xFFFF
PFS	10	0x4	0-9	PA0%sPFS_BY	PA0%s引脚功能控制 Register	0x283	8	read/ write	0x00	0xFF
PFS	6	0x4	10-15	PA%sPFS	PA%s引脚功能控制 Register	0x2A8	32	read/ write	0x00000000	0xFFFFFFFF
PFS	6	0x4	10-15	PA%sPFS_HA	PA%s引脚功能控制 Register	0x2AA	16	read/ write	0x0000	0xFFFF
PFS	6	0x4	10-15	PA%sPFS_BY	PA%s引脚功能控制 Register	0x2AB	8	read/ write	0x00	0xFF
PFS	8	0x4	0-7	PB0%sPFS	PB0%s引脚功能控制 Register	0x2C0	32	read/ write	0x00000000	0xFFFFFFFF
PFS	8	0x4	0-7	PB0%sPFS_HA	PB0%s引脚功能控制 Register	0x2C2	16	read/ write	0x0000	0xFFFF
PFS	8	0x4	0-7	PB0%sPFS_BY	PB0%s引脚功能控制 Register	0x2C3	8	read/ write	0x00	0xFF
PMISC	-	-	-	PFENET	以太网控制寄存器	0x00	8	read/ write	0x00	0xFF
PMISC	-	-	-	PWPR	Write-Protect Register	0x03	8	read/ write	0x80	0xFF
ELC	-	-	-	ELCR	事件链接控制器 Register	0x00	8	read/ write	0x00	0xFF
ELC	2	0x2	0,1	ELSEGR%s	活动链接软件活动 代寄存器%s	0x02	8	read/ write	0x80	0xFF
ELC	19	0x4	0-18	ELSR%s	事件链接设置寄存器%s	0x10	16	read/ write	0x0000	0xFFFF
POEG	4	0x100	A,B,C ,D	POEGG%s	POEG组%s设置 Register	0x00	32	read/ write	0x00000000	0xFFFFFFFF
RTC	-	-	-	R64CNT	64-Hz Counter	0x00	8	只读	0x00	0x80
RTC	-	-	-	RSECCNT	第二个柜台	0x02	8	read/ write	0x00	0x00
RTC	-	-	-	BCNT0	二进制计数器0	0x02	8	read/ write	0x00	0x00
RTC	-	-	-	RMINCNT	分钟计数器	0x04	8	read/ write	0x00	0x00
RTC	-	-	-	BCNT1	二进制计数器1	0x04	8	read/ write	0x00	0x00
RTC	-	-	-	RHRCNT	小时计数器	0x06	8	read/ write	0x00	0x00
RTC	-	-	-	BCNT2	二进制计数器2	0x06	8	read/ write	0x00	0x00
RTC	-	-	-	RWKCNT	Day-of-Week Counter	0x08	8	read/ write	0x00	0x00
RTC	-	-	-	BCNT3	二进制计数器3	0x08	8	read/ write	0x00	0x00
RTC	-	-	-	RDAYCNT	日计数器	0x0A	8	read/ write	0x00	0xC0

Table 3.3 Register description (12 of 44)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
RTC	-	-	-	RMONCNT	Month Counter	0x0C	8	read/ write	0x00	0xE0
RTC	-	-	-	RYRCNT	Year Counter	0x0E	16	read/ write	0x0000	0xFF00
RTC	-	-	-	RSECAR	Second Alarm Register	0x10	8	read/ write	0x00	0x00
RTC	-	-	-	BCNT0AR	Binary Counter 0 Alarm Register	0x10	8	read/ write	0x00	0x00
RTC	-	-	-	RMINAR	Minute Alarm Register	0x12	8	read/ write	0x00	0x00
RTC	-	-	-	BCNT1AR	Binary Counter 1 Alarm Register	0x12	8	read/ write	0x00	0x00
RTC	-	-	-	RHRAR	Hour Alarm Register	0x14	8	read/ write	0x00	0x00
RTC	-	-	-	BCNT2AR	Binary Counter 2 Alarm Register	0x14	8	read/ write	0x00	0x00
RTC	-	-	-	RWKAR	Day-of-Week Alarm Register	0x16	8	read/ write	0x00	0x00
RTC	-	-	-	BCNT3AR	Binary Counter 3 Alarm Register	0x16	8	read/ write	0x00	0x00
RTC	-	-	-	RDAYAR	Date Alarm Register	0x18	8	read/ write	0x00	0x00
RTC	-	-	-	BCNT0AER	Binary Counter 0 Alarm Enable Register	0x18	8	read/ write	0x00	0x00
RTC	-	-	-	RMONAR	Month Alarm Register	0x1A	8	read/ write	0x00	0x00
RTC	-	-	-	BCNT1AER	Binary Counter 1 Alarm Enable Register	0x1A	8	read/ write	0x00	0x00
RTC	-	-	-	RYRAR	Year Alarm Register	0x1C	16	read/ write	0x0000	0xFF00
RTC	-	-	-	BCNT2AER	Binary Counter 2 Alarm Enable Register	0x1C	16	read/ write	0x0000	0xFF00
RTC	-	-	-	RYRAREN	Year Alarm Enable Register	0x1E	8	read/ write	0x00	0x00
RTC	-	-	-	BCNT3AER	Binary Counter 3 Alarm Enable Register	0x1E	8	read/ write	0x00	0x00
RTC	-	-	-	RCR1	RTC Control Register 1	0x22	8	read/ write	0x00	0x0A
RTC	-	-	-	RCR2	RTC Control Register 2	0x24	8	read/ write	0x00	0x0E
RTC	-	-	-	RCR4	RTC Control Register 4	0x28	8	read/ write	0x00	0xFE
RTC	-	-	-	RFRH	Frequency Register H	0x2A	16	read/ write	0x0000	0xFFFE
RTC	-	-	-	RFRL	Frequency Register L	0x2C	16	read/ write	0x0000	0x0000
RTC	-	-	-	RADJ	Time Error Adjustment Register	0x2E	8	read/ write	0x00	0x00
RTC	3	0x2	0-2	RTCCR%s	Time Capture Control Register %s	0x40	8	read/ write	0x00	0x00
RTC	3	0x10	0-2	RSECCP%s	Second Capture Register %s	0x52	8	read-only	0x00	0x00
RTC	3	0x10	0-2	BCNT0CP%s	BCNT0 Capture Register %s	0x52	8	read-only	0x00	0x00
RTC	3	0x10	0-2	RMINCP%s	Minute Capture Register %s	0x54	8	read-only	0x00	0x00
RTC	3	0x10	0-2	BCNT1CP%s	BCNT1 Capture Register %s	0x54	8	read-only	0x00	0x00
RTC	3	0x10	0-2	RHRCP%s	Hour Capture Register %s	0x56	8	read-only	0x00	0x00

Table 3.3 寄存器描述（44个中的12个）

周边暗淡		昏暗的增量。	暗淡索引寄存器名称		Description	地址偏移	尺寸	访问	重置值	重置蒙版
RTC	-	-	-	RMONCNT	月计数器	0x0C	8	read/ write	0x00	0xE0
RTC	-	-	-	RYRCNT	年计数器	0x0E	16	read/ write	0x0000	0xFF00
RTC	-	-	-	RSECAR	第二报警寄存器	0x10	8	read/ write	0x00	0x00
RTC	-	-	-	BCNT0AR	二进制计数器0报警 Register	0x10	8	read/ write	0x00	0x00
RTC	-	-	-	RMINAR	分钟报警寄存器	0x12	8	read/ write	0x00	0x00
RTC	-	-	-	BCNT1AR	二进制计数器1警报 Register	0x12	8	read/ write	0x00	0x00
RTC	-	-	-	RHRAR	小时报警寄存器	0x14	8	read/ write	0x00	0x00
RTC	-	-	-	BCNT2AR	二进制计数器2报警 Register	0x14	8	read/ write	0x00	0x00
RTC	-	-	-	RWKAR	星期报警寄存器0x 16		8	read/ write	0x00	0x00
RTC	-	-	-	BCNT3AR	二进制计数器3报警 Register	0x16	8	read/ write	0x00	0x00
RTC	-	-	-	RDAYAR	日期报警寄存器	0x18	8	read/ write	0x00	0x00
RTC	-	-	-	BCNT0AER	二进制计数器0报警 启用注册	0x18	8	read/ write	0x00	0x00
RTC	-	-	-	RMONAR	月报警寄存器	0x1A	8	read/ write	0x00	0x00
RTC	-	-	-	BCNT1AER	二进制计数器1警报 启用注册	0x1A	8	read/ write	0x00	0x00
RTC	-	-	-	RYRAR	年报警寄存器	0x1C	16	read/ write	0x0000	0xFF00
RTC	-	-	-	BCNT2AER	二进制计数器2报警 启用注册	0x1C	16	read/ write	0x0000	0xFF00
RTC	-	-	-	RYRAREN	年警报启用寄存器	0x1E	8	read/ write	0x00	0x00
RTC	-	-	-	BCNT3AER	二进制计数器3报警 启用注册	0x1E	8	read/ write	0x00	0x00
RTC	-	-	-	RCR1	RTC控制寄存器1	0x22	8	read/ write	0x00	0x0A
RTC	-	-	-	RCR2	RTC控制寄存器2	0x24	8	read/ write	0x00	0x0E
RTC	-	-	-	RCR4	RTC控制寄存器4	0x28	8	read/ write	0x00	0xFE
RTC	-	-	-	RFRH	频率寄存器H	0x2A	16	read/ write	0x0000	0xFFFE
RTC	-	-	-	RFRL	频率寄存器L	0x2C	16	read/ write	0x0000	0x0000
RTC	-	-	-	RADJ	时间误差调整 Register	0x2E	8	read/ write	0x00	0x00
RTC	3	0x2	0-2	RTCCR%s	时间捕捉控制 Register %s	0x40	8	read/ write	0x00	0x00
RTC	3	0x10	0-2	RSECCP%s	第二个捕获寄存器%s0x52		8	只读	0x00	0x00
RTC	3	0x10	0-2	BCNT0CP%s	BCNT0捕捉寄存器%s0x52		8	只读	0x00	0x00
RTC	3	0x10	0-2	RMINCP%s	分钟捕获寄存器%s	0x54	8	只读	0x00	0x00
RTC	3	0x10	0-2	BCNT1CP%s	BCNT1捕获寄存器%s0x54		8	只读	0x00	0x00
RTC	3	0x10	0-2	RHRCP%s	小时记录寄存器%s	0x56	8	只读	0x00	0x00

Table 3.3 Register description (13 of 44)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
RTC	3	0x10	0-2	BCNT2CP%s	BCNT2 Capture Register %s	0x56	8	read-only	0x00	0x00
RTC	3	0x10	0-2	RDAYCP%s	Date Capture Register %s	0x5A	8	read-only	0x00	0x00
RTC	3	0x10	0-2	BCNT3CP%s	BCNT3 Capture Register %s	0x5A	8	read-only	0x00	0x00
RTC	3	0x10	0-2	RMONCP%s	Month Capture Register %s	0x5C	8	read-only	0x00	0x00
WDT	-	-	-	WDTRR	WDT Refresh Register	0x00	8	read/write	0xFF	0xFF
WDT	-	-	-	WDTCR	WDT Control Register	0x02	16	read/write	0x33F3	0xFFFF
WDT	-	-	-	WDTSR	WDT Status Register	0x04	16	read/write	0x0000	0xFFFF
WDT	-	-	-	WDTRCR	WDT Reset Control Register	0x06	8	read/write	0x80	0xFF
WDT	-	-	-	WDTCSTPR	WDT Count Stop Control Register	0x08	8	read/write	0x80	0xFF
IWDT	-	-	-	IWDTRR	IWDT Refresh Register	0x00	8	read/write	0xFF	0xFF
IWDT	-	-	-	IWDTSR	IWDT Status Register	0x04	16	read/write	0x0000	0xFFFF
CAC	-	-	-	CACR0	CAC Control Register 0	0x00	8	read/write	0x00	0xFF
CAC	-	-	-	CACR1	CAC Control Register 1	0x01	8	read/write	0x00	0xFF
CAC	-	-	-	CACR2	CAC Control Register 2	0x02	8	read/write	0x00	0xFF
CAC	-	-	-	CAICR	CAC Interrupt Control Register	0x03	8	read/write	0x00	0xFF
CAC	-	-	-	CASTR	CAC Status Register	0x04	8	read-only	0x00	0xFF
CAC	-	-	-	CAULVR	CAC Upper-Limit Value Setting Register	0x06	16	read/write	0x0000	0xFFFF
CAC	-	-	-	CALLVR	CAC Lower-Limit Value Setting Register	0x08	16	read/write	0x0000	0xFFFF
CAC	-	-	-	CACNTBR	CAC Counter Buffer Register	0x0A	16	read-only	0x0000	0xFFFF
MSTP	-	-	-	MSTPCRB	Module Stop Control Register B	0x00	32	read/write	0xFFFFFFFF	0xFFFFFFFF
MSTP	-	-	-	MSTPCRC	Module Stop Control Register C	0x04	32	read/write	0xFFFFFFFF	0xFFFFFFFF
MSTP	-	-	-	MSTPCRD	Module Stop Control Register D	0x08	32	read/write	0xFFFFFFFF	0xFFFFFFFF
SRCRAM	5552	0x4	0-5551	SRCFCTR[%s]	Filter Coefficient Table [%s]	0x00	32	read/write	0x00000000	0xFFC00000
SRC	-	-	-	SRCID	Input Data Register	0x00	32	write-only	0x00000000	0xFFFFFFFF
SRC	-	-	-	SRCOD	Output Data Register	0x04	32	read-only	0x00000000	0xFFFFFFFF
SRC	-	-	-	SRCIDCTRL	Input Data Control Register	0x08	16	read/write	0x0000	0xFFFF
SRC	-	-	-	SRCODCTRL	Output Data Control Register	0x0A	16	read/write	0x0000	0xFFFF
SRC	-	-	-	SRCCTRL	Control Register	0x0C	16	read/write	0x0000	0xFFFF
SRC	-	-	-	SRCSTAT	Status Register	0x0E	16	read/write	0x0002	0xFFFF
SSIE0,1	-	-	-	SSICR	Control Register	0x00	32	read/write	0x00000000	0xFFFFFFFF

Table 3.3 寄存器说明（44个中的13个）

周边暗淡	昏暗的增量。	暗淡索引寄存器名称		Description	地址偏移	尺寸访问		重置值	重置蒙版
RTC	3	0x10	0-2	BCNT2CP%s	BCNT2捕捉寄存器%s0x56		8	只读	0x00	0x00
RTC	3	0x10	0-2	RDAYCP%s	日期捕获寄存器%s	0x5A	8	只读	0x00	0x00
RTC	3	0x10	0-2	BCNT3CP%s	BCNT3捕捉寄存器%s0x5A		8	只读	0x00	0x00
RTC	3	0x10	0-2	RMONCP%s	月份捕获寄存器%s	0x5C	8	只读	0x00	0x00
WDT	-	-	-	WDTRR	WDT刷新寄存器	0x00	8	read/write	0xFF	0xFF
WDT	-	-	-	WDTCR	WDT控制寄存器	0x02	16	read/write	0x33F3	0xFFFF
WDT	-	-	-	WDTSR	WDT状态寄存器	0x04	16	read/write	0x0000	0xFFFF
WDT	-	-	-	WDTRCR	WDT复位控制寄存器0x06		8	read/write	0x80	0xFF
WDT	-	-	-	WDTCSTPR	WDT计数停止控制Register	0x08	8	read/write	0x80	0xFF
IWDT	-	-	-	IWDTRR	IWDT刷新寄存器	0x00	8	read/write	0xFF	0xFF
IWDT	-	-	-	IWDTSR	IWDT状态寄存器	0x04	16	read/write	0x0000	0xFFFF
CAC	-	-	-	CACR0	CAC控制寄存器0	0x00	8	read/write	0x00	0xFF
CAC	-	-	-	CACR1	CAC控制寄存器1	0x01	8	read/write	0x00	0xFF
CAC	-	-	-	CACR2	CAC控制寄存器2	0x02	8	read/write	0x00	0xFF
CAC	-	-	-	CAICR	CAC中断控制Register	0x03	8	read/write	0x00	0xFF
CAC	-	-	-	CASTR	CAC状态寄存器	0x04	8	只读	0x00	0xFF
CAC	-	-	-	CAULVR	CAC上限值设置寄存器	0x06	16	read/write	0x0000	0xFFFF
CAC	-	-	-	CALLVR	CAC下限值设置寄存器	0x08	16	read/write	0x0000	0xFFFF
CAC	-	-	-	CACNTBR	CAC计数器缓冲寄存器0x0A		16	只读	0x0000	0xFFFF
MSTP	-	-	-	MSTPCRB	模块停止控制Register B	0x00	32	read/write	0xFFFFFFFF	0xFFFFFFFF
MSTP	-	-	-	MSTPCRC	模块停止控制Register C	0x04	32	read/write	0xFFFFFFFF	0xFFFFFFFF
MSTP	-	-	-	MSTPCRD	模块停止控制Register D	0x08	32	read/write	0xFFFFFFFF	0xFFFFFFFF
SRCRAM	5552	0x4	0-5551	SRCFCTR[%s]	过滤器系数表[%s]	0x00	32	read/write	0x00000000	0xFFC00000
SRC	-	-	-	SRCID	输入数据寄存器	0x00	32	只写	0x00000000	0xFFFFFFFF
SRC	-	-	-	SRCOD	输出数据寄存器	0x04	32	只读	0x00000000	0xFFFFFFFF
SRC	-	-	-	SRCIDCTRL	输入数据控制寄存器	0x08	16	read/write	0x0000	0xFFFF
SRC	-	-	-	SRCODCTRL	输出数据控制寄存器0x0A		16	read/write	0x0000	0xFFFF
SRC	-	-	-	SRCCTRL	控制寄存器	0x0C	16	read/write	0x0000	0xFFFF
SRC	-	-	-	SRCSTAT	状态寄存器	0x0E	16	read/write	0x0002	0xFFFF
SSIE0,1	-	-	-	SSICR	控制寄存器	0x00	32	read/write	0x00000000	0xFFFFFFFF

Table 3.3 Register description (14 of 44)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
SSIE0,1	-	-	-	SSISR	Status Register	0x04	32	read/ write	0x02000013	0x3E00007F
SSIE0,1	-	-	-	SSIFCR	FIFO Control Register	0x10	32	read/ write	0x00000000	0xFFFFFFFF
SSIE0,1	-	-	-	SSIFSR	FIFO Status Register	0x14	32	read/ write	0x00010000	0xFFFFFFFF
SSIE0,1	-	-	-	SSIFTDR	Transmit FIFO Data Register	0x18	32	write-only	0x00000000	0x00000000
SSIE0,1	-	-	-	SSIFRDR	Receive FIFO Data Register	0x1C	32	read-only	0x00000000	0x00000000
SSIE0,1	-	-	-	SSIOFR	Audio Format Register	0x20	32	read/ write	0x00000000	0xFFFFFFFF
SSIE0,1	-	-	-	SSISCR	Status Control Register	0x24	32	read/ write	0x00000000	0xFFFFFFFF
CAN0,1	32	0x10	0-31	MB%s_ID	Mailbox Register	0x200	32	read/ write	0x00000000	0x00000000
CAN0,1	32	0x10	0-31	MB%s_DL	Mailbox Register	0x204	16	read/ write	0x0000	0x0000
CAN0,1	32	0x10	0-31	MB%s_D0	Mailbox Register	0x206	8	read/ write	0x00	0x00
CAN0,1	32	0x10	0-31	MB%s_D1	Mailbox Register	0x207	8	read/ write	0x00	0x00
CAN0,1	32	0x10	0-31	MB%s_D2	Mailbox Register	0x208	8	read/ write	0x00	0x00
CAN0,1	32	0x10	0-31	MB%s_D3	Mailbox Register	0x209	8	read/ write	0x00	0x00
CAN0,1	32	0x10	0-31	MB%s_D4	Mailbox Register	0x20A	8	read/ write	0x00	0x00
CAN0,1	32	0x10	0-31	MB%s_D5	Mailbox Register	0x20B	8	read/ write	0x00	0x00
CAN0,1	32	0x10	0-31	MB%s_D6	Mailbox Register	0x20C	8	read/ write	0x00	0x00
CAN0,1	32	0x10	0-31	MB%s_D7	Mailbox Register	0x20D	8	read/ write	0x00	0x00
CAN0,1	32	0x10	0-31	MB%s_TS	Mailbox Register	0x20E	16	read/ write	0x0000	0x0000
CAN0,1	8	0x4	0-7	MKR[%s]	Mask Register	0x400	32	read/ write	0x00000000	0x00000000
CAN0,1	2	0x4	0,1	FIDCR%s	FIFO Received ID Compare Registers	0x420	32	read/ write	0x00000000	0x00000000
CAN0,1	-	-	-	MKIVLR	Mask Invalid Register	0x428	32	read/ write	0x00000000	0x00000000
CAN0,1	-	-	-	MIER	Mailbox Interrupt Enable Register	0x42C	32	read/ write	0x00000000	0x00000000
CAN0,1	-	-	-	MIER_FIFO	Mailbox Interrupt Enable Register for FIFO Mailbox Mode	0x42C	32	read/ write	0x00000000	0x00000000
CAN0,1	32	0x1	0-31	MCTL_TX[%s]	Message Control Register for Transmit	0x820	8	read/ write	0x00	0xFF
CAN0,1	32	0x1	0-31	MCTL_RX[%s]	Message Control Register for Receive	0x820	8	read/ write	0x00	0xFF
CAN0,1	-	-	-	CTLR	Control Register	0x840	16	read/ write	0x0500	0xFFFF
CAN0,1	-	-	-	STR	Status Register	0x842	16	read-only	0x0500	0xFFFF
CAN0,1	-	-	-	BCR	Bit Configuration Register	0x844	32	read/ write	0x00000000	0xFFFFFFFF
CAN0,1	-	-	-	RFCR	Receive FIFO Control Register	0x848	8	read/ write	0x80	0xFF

Table 3.3 寄存器说明（44个中的14个）

周边暗淡		昏暗的增量。	暗淡索引寄存器名称		Description	地址偏移	尺寸	访问	重置值	重置蒙版
SSIE0,1	-	-	-	SSISR	状态寄存器	0x04	32	read/ write	0x02000013	0x3E00007F
SSIE0,1	-	-	-	SSIFCR	先进先出控制寄存器	0x10	32	read/ write	0x00000000	0xFFFFFFFF
SSIE0,1	-	-	-	SSIFSR	FIFO状态寄存器	0x14	32	read/ write	0x00010000	0xFFFFFFFF
SSIE0,1	-	-	-	SSIFTDR	发送FIFO数据寄存器0x	18	32	只写	0x00000000	0x00000000
SSIE0,1	-	-	-	SSIFRDR	接收FIFO数据寄存器	0x1C	32	只读	0x00000000	0x00000000
SSIE0,1	-	-	-	SSIOFR	音频格式寄存器	0x20	32	read/ write	0x00000000	0xFFFFFFFF
SSIE0,1	-	-	-	SSISCR	状态控制寄存器	0x24	32	read/ write	0x00000000	0xFFFFFFFF
CAN0,1	32	0x10	0-31	MB%s_ID	邮箱注册	0x200	32	read/ write	0x00000000	0x00000000
CAN0,1	32	0x10	0-31	MB%s_DL	邮箱注册	0x204	16	read/ write	0x0000	0x0000
CAN0,1	32	0x10	0-31	MB%s_D0	邮箱注册	0x206	8	read/ write	0x00	0x00
CAN0,1	32	0x10	0-31	MB%s_D1	邮箱注册	0x207	8	read/ write	0x00	0x00
CAN0,1	32	0x10	0-31	MB%s_D2	邮箱注册	0x208	8	read/ write	0x00	0x00
CAN0,1	32	0x10	0-31	MB%s_D3	邮箱注册	0x209	8	read/ write	0x00	0x00
CAN0,1	32	0x10	0-31	MB%s_D4	邮箱注册	0x20A	8	read/ write	0x00	0x00
CAN0,1	32	0x10	0-31	MB%s_D5	邮箱注册	0x20B	8	read/ write	0x00	0x00
CAN0,1	32	0x10	0-31	MB%s_D6	邮箱注册	0x20C	8	read/ write	0x00	0x00
CAN0,1	32	0x10	0-31	MB%s_D7	邮箱注册	0x20D	8	read/ write	0x00	0x00
CAN0,1	32	0x10	0-31	MB%s_TS	邮箱注册	0x20E	16	read/ write	0x0000	0x0000
CAN0,1	8	0x4	0-7	MKR[%s]	掩码寄存器	0x400	32	read/ write	0x00000000	0x00000000
CAN0,1	2	0x4	0,1	FIDCR%s	FIFO接收ID比较 Registers	0x420	32	read/ write	0x00000000	0x00000000
CAN0,1	-	-	-	MKIVLR	屏蔽无效寄存器	0x428	32	read/ write	0x00000000	0x00000000
CAN0,1	-	-	-	MIER	邮箱中断启用 Register	0x42C	32	read/ write	0x00000000	0x00000000
CAN0,1	-	-	-	MIER_FIFO	FIFO邮箱的邮箱中断使能寄存器 Mode	0x42C	32	read/ write	0x00000000	0x00000000
CAN0,1	32	0x1	0-31	MCTL_TX[%s]	用于发送的消息控制寄存器	0x820	8	read/ write	0x00	0xFF
CAN0,1	32	0x1	0-31	MCTL_RX[%s]	接收消息控制寄存器	0x820	8	read/ write	0x00	0xFF
CAN0,1	-	-	-	CTLR	控制寄存器	0x840	16	read/ write	0x0500	0xFFFF
CAN0,1	-	-	-	STR	状态寄存器	0x842	16	只读	0x0500	0xFFFF
CAN0,1	-	-	-	BCR	位配置寄存器	0x844	32	read/ write	0x00000000	0xFFFFFFFF
CAN0,1	-	-	-	RFCR	接收FIFO控制 Register	0x848	8	read/ write	0x80	0xFF

Table 3.3 Register description (15 of 44)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
CAN0,1	-	-	-	RFPCR	Receive FIFO Pointer Control Register	0x849	8	write-only	0x00	0x00
CAN0,1	-	-	-	TFCR	Transmit FIFO Control Register	0x84A	8	read/write	0x80	0xFF
CAN0,1	-	-	-	TFPCR	Transmit FIFO Pointer Control Register	0x84B	8	write-only	0x00	0x00
CAN0,1	-	-	-	EIER	Error Interrupt Enable Register	0x84C	8	read/write	0x00	0xFF
CAN0,1	-	-	-	EIFR	Error Interrupt Factor Judge Register	0x84D	8	read/write	0x00	0xFF
CAN0,1	-	-	-	RECR	Receive Error Count Register	0x84E	8	read-only	0x00	0xFF
CAN0,1	-	-	-	TECR	Transmit Error Count Register	0x84F	8	read-only	0x00	0xFF
CAN0,1	-	-	-	ECSR	Error Code Store Register	0x850	8	read/write	0x00	0xFF
CAN0,1	-	-	-	CSSR	Channel Search Support Register	0x851	8	read/write	0x00	0x00
CAN0,1	-	-	-	MSSR	Mailbox Search Status Register	0x852	8	read-only	0x80	0xFF
CAN0,1	-	-	-	MSMR	Mailbox Search Mode Register	0x853	8	read/write	0x00	0xFF
CAN0,1	-	-	-	TSR	Time Stamp Register	0x854	16	read-only	0x0000	0xFFFF
CAN0,1	-	-	-	AFSR	Acceptance Filter Support Register	0x856	16	read/write	0x0000	0x0000
CAN0,1	-	-	-	TCR	Test Control Register	0x858	8	read/write	0x00	0xFF
IIC0	-	-	-	ICCR1	I2C Bus Control Register 1	0x00	8	read/write	0x1F	0xFF
IIC0	-	-	-	ICCR2	I2C Bus Control Register 2	0x01	8	read/write	0x00	0xFF
IIC0	-	-	-	ICMR1	I2C Bus Mode Register 1	0x02	8	read/write	0x08	0xFF
IIC0	-	-	-	ICMR2	I2C Bus Mode Register 2	0x03	8	read/write	0x06	0xFF
IIC0	-	-	-	ICMR3	I2C Bus Mode Register 3	0x04	8	read/write	0x00	0xFF
IIC0	-	-	-	ICFER	I2C Bus Function Enable Register	0x05	8	read/write	0x72	0xFF
IIC0	-	-	-	ICSER	I2C Bus Status Enable Register	0x06	8	read/write	0x09	0xFF
IIC0	-	-	-	ICIER	I2C Bus Interrupt Enable Register	0x07	8	read/write	0x00	0xFF
IIC0	-	-	-	ICSR1	I2C Bus Status Register 1	0x08	8	read/write	0x00	0xFF
IIC0	-	-	-	ICSR2	I2C Bus Status Register 2	0x09	8	read/write	0x00	0xFF
IIC0	3	0x2	0-2	SARL%s	Slave Address Register L%s	0x0A	8	read/write	0x00	0xFF
IIC0	3	0x2	0-2	SARU%s	Slave Address Register U%s	0x0B	8	read/write	0x00	0xFF
IIC0	-	-	-	ICBRL	I2C Bus Bit Rate Low-Level Register	0x10	8	read/write	0xFF	0xFF
IIC0	-	-	-	ICBRH	I2C Bus Bit Rate High-Level Register	0x11	8	read/write	0xFF	0xFF
IIC0	-	-	-	ICDRT	I2C Bus Transmit Data Register	0x12	8	read/write	0xFF	0xFF
IIC0	-	-	-	ICDRR	I2C Bus Receive Data Register	0x13	8	read-only	0x00	0xFF

Table 3.3 寄存器说明（44中的15）

周边暗淡	昏暗的增量。	暗淡索引寄存器名称		Description	地址偏移	尺寸	访问	重置值	重置蒙版
CAN0,1	-	-	-	RFPCR	接收FIFO指针控制寄存器	0x849	8	只写	0x00	0x00
CAN0,1	-	-	-	TFCR	发送FIFO控制Register	0x84A	8	read/write	0x80	0xFF
CAN0,1	-	-	-	TFPCR	发送FIFO指针控制寄存器	0x84B	8	只写	0x00	0x00
CAN0,1	-	-	-	EIER	错误中断使能Register	0x84C	8	read/write	0x00	0xFF
CAN0,1	-	-	-	EIFR	错误中断因素判断Register	0x84D	8	read/write	0x00	0xFF
CAN0,1	-	-	-	RECR	接收错误计数Register	0x84E	8	只读	0x00	0xFF
CAN0,1	-	-	-	TECR	传输错误计数Register	0x84F	8	只读	0x00	0xFF
CAN0,1	-	-	-	ECSR	错误代码存储寄存器	0x850	8	read/write	0x00	0xFF
CAN0,1	-	-	-	CSSR	频道搜索支持Register	0x851	8	read/write	0x00	0x00
CAN0,1	-	-	-	MSSR	邮箱搜索状态Register	0x852	8	只读	0x80	0xFF
CAN0,1	-	-	-	MSMR	邮箱搜索模式Register	0x853	8	read/write	0x00	0xFF
CAN0,1	-	-	-	TSR	时间戳寄存器	0x854	16	只读	0x0000	0xFFFF
CAN0,1	-	-	-	AFSR	接受过滤器支持Register	0x856	16	read/write	0x0000	0x0000
CAN0,1	-	-	-	TCR	测试控制寄存器	0x858	8	read/write	0x00	0xFF
IIC0	-	-	-	ICCR1	I2C总线控制寄存器1	0x00	8	read/write	0x1F	0xFF
IIC0	-	-	-	ICCR2	I2C总线控制寄存器2	0x01	8	read/write	0x00	0xFF
IIC0	-	-	-	ICMR1	I2C总线模式寄存器1	0x02	8	read/write	0x08	0xFF
IIC0	-	-	-	ICMR2	I2C总线模式寄存器2	0x03	8	read/write	0x06	0xFF
IIC0	-	-	-	ICMR3	I2C总线模式寄存器3	0x04	8	read/write	0x00	0xFF
IIC0	-	-	-	ICFER	I2C总线功能使能Register	0x05	8	read/write	0x72	0xFF
IIC0	-	-	-	ICSER	I2C总线状态启用Register	0x06	8	read/write	0x09	0xFF
IIC0	-	-	-	ICIER	I2C总线中断使能Register	0x07	8	read/write	0x00	0xFF
IIC0	-	-	-	ICSR1	I2C总线状态寄存器1	0x08	8	read/write	0x00	0xFF
IIC0	-	-	-	ICSR2	I2C总线状态寄存器2	0x09	8	read/write	0x00	0xFF
IIC0	3	0x2	0-2	SARL%s	从地址寄存器L%s0x0A		8	read/write	0x00	0xFF
IIC0	3	0x2	0-2	SARU%s	从机地址寄存器U%s0x0B		8	read/write	0x00	0xFF
IIC0	-	-	-	ICBRL	I2C总线比特率低电平Register	0x10	8	read/write	0xFF	0xFF
IIC0	-	-	-	ICBRH	I2C总线比特率高级Register	0x11	8	read/write	0xFF	0xFF
IIC0	-	-	-	ICDRT	I2C总线传输数据Register	0x12	8	read/write	0xFF	0xFF
IIC0	-	-	-	ICDRR	I2C总线接收数据Register	0x13	8	只读	0x00	0xFF

Table 3.3 Register description (16 of 44)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
IIC0	-	-	-	ICWUR	I2C Bus Wake Up Unit Register	0x16	8	read/ write	0x00	0xFF
IIC0	-	-	-	ICWUR2	I2C Bus Wake Up Unit Register 2	0x17	8	read-only	0x03	0xFF
IIC1,2	-	-	-	ICCR1	I2C Bus Control Register 1	0x00	8	read/ write	0x1F	0xFF
IIC1,2	-	-	-	ICCR2	I2C Bus Control Register 2	0x01	8	read/ write	0x00	0xFF
IIC1,2	-	-	-	ICMR1	I2C Bus Mode Register 1	0x02	8	read/ write	0x08	0xFF
IIC1,2	-	-	-	ICMR2	I2C Bus Mode Register 2	0x03	8	read/ write	0x06	0xFF
IIC1,2	-	-	-	ICMR3	I2C Bus Mode Register 3	0x04	8	read/ write	0x00	0xFF
IIC1,2	-	-	-	ICFER	I2C Bus Function Enable Register	0x05	8	read/ write	0x72	0xFF
IIC1,2	-	-	-	ICSER	I2C Bus Status Enable Register	0x06	8	read/ write	0x09	0xFF
IIC1,2	-	-	-	ICIER	I2C Bus Interrupt Enable Register	0x07	8	read/ write	0x00	0xFF
IIC1,2	-	-	-	ICSR1	I2C Bus Status Register 1	0x08	8	read/ write	0x00	0xFF
IIC1,2	-	-	-	ICSR2	I2C Bus Status Register 2	0x09	8	read/ write	0x00	0xFF
IIC1,2	3	0x2	0-2	SARL%s	Slave Address Register L%s	0x0A	8	read/ write	0x00	0xFF
IIC1,2	3	0x2	0-2	SARU%s	Slave Address Register U%s	0x0B	8	read/ write	0x00	0xFF
IIC1,2	-	-	-	ICBRL	I2C Bus Bit Rate Low-Level Register	0x10	8	read/ write	0xFF	0xFF
IIC1,2	-	-	-	ICBRH	I2C Bus Bit Rate High-Level Register	0x11	8	read/ write	0xFF	0xFF
IIC1,2	-	-	-	ICDRT	I2C Bus Transmit Data Register	0x12	8	read/ write	0xFF	0xFF
IIC1,2	-	-	-	ICDRR	I2C Bus Receive Data Register	0x13	8	read-only	0x00	0xFF
DOC	-	-	-	DOCR	DOC Control Register	0x00	8	read/ write	0x00	0xFF
DOC	-	-	-	DODIR	DOC Data Input Register	0x02	16	read/ write	0x0000	0xFFFF
DOC	-	-	-	DODSR	DOC Data Setting Register	0x04	16	read/ write	0x0000	0xFFFF
ADC120	-	-	-	ADCSR	A/D Control Register	0x000	16	read/ write	0x0000	0xFFFF
ADC120	-	-	-	ADANSA0	A/D Channel Select Register A0	0x004	16	read/ write	0x0000	0xFFFF
ADC120	-	-	-	ADANSA1	A/D Channel Select Register A1	0x006	16	read/ write	0x0000	0xFFFF
ADC120	-	-	-	ADADS0	A/D-Converted Value Addition/Average Channel Select Register 0	0x008	16	read/ write	0x0000	0xFFFF
ADC120	-	-	-	ADADS1	A/D-Converted Value Addition/Average Channel Select Register 1	0x00A	16	read/ write	0x0000	0xFFFF
ADC120	-	-	-	ADADC	A/D-Converted Value Addition/Average Count Select Register	0x00C	8	read/ write	0x00	0xFF
ADC120	-	-	-	ADCER	A/D Control Extended Register	0x00E	16	read/ write	0x0000	0xFFFF

Table 3.3 寄存器说明（44个中的16个）

周边暗淡		昏暗的增量。	暗淡索引寄存器名称		Description	地址偏移	尺寸	访问	重置值	重置蒙版
IIC0	-	-	-	ICWUR	I2C总线唤醒单元 Register	0x16	8	read/ write	0x00	0xFF
IIC0	-	-	-	ICWUR2	I2C总线唤醒单元 Register 2	0x17	8	只读	0x03	0xFF
IIC1,2	-	-	-	ICCR1	I2C总线控制寄存器1	0x00	8	read/ write	0x1F	0xFF
IIC1,2	-	-	-	ICCR2	I2C总线控制寄存器2	0x01	8	read/ write	0x00	0xFF
IIC1,2	-	-	-	ICMR1	I2C总线模式寄存器1	0x02	8	read/ write	0x08	0xFF
IIC1,2	-	-	-	ICMR2	I2C总线模式寄存器2	0x03	8	read/ write	0x06	0xFF
IIC1,2	-	-	-	ICMR3	I2C总线模式寄存器3	0x04	8	read/ write	0x00	0xFF
IIC1,2	-	-	-	ICFER	I2C总线功能使能 Register	0x05	8	read/ write	0x72	0xFF
IIC1,2	-	-	-	ICSER	I2C总线状态启用 Register	0x06	8	read/ write	0x09	0xFF
IIC1,2	-	-	-	ICIER	I2C总线中断使能 Register	0x07	8	read/ write	0x00	0xFF
IIC1,2	-	-	-	ICSR1	I2C总线状态寄存器1	0x08	8	read/ write	0x00	0xFF
IIC1,2	-	-	-	ICSR2	I2C总线状态寄存器2	0x09	8	read/ write	0x00	0xFF
IIC1,2	3	0x2	0-2	SARL%s	从地址寄存器L%s0x0A		8	read/ write	0x00	0xFF
IIC1,2	3	0x2	0-2	SARU%s	从机地址寄存器U%s0x0B		8	read/ write	0x00	0xFF
IIC1,2	-	-	-	ICBRL	I2C总线比特率低电平 Register	0x10	8	read/ write	0xFF	0xFF
IIC1,2	-	-	-	ICBRH	I2C总线比特率高级 Register	0x11	8	read/ write	0xFF	0xFF
IIC1,2	-	-	-	ICDRT	I2C总线传输数据 Register	0x12	8	read/ write	0xFF	0xFF
IIC1,2	-	-	-	ICDRR	I2C总线接收数据 Register	0x13	8	只读	0x00	0xFF
DOC	-	-	-	DOCR	DOC控制寄存器	0x00	8	read/ write	0x00	0xFF
DOC	-	-	-	DODIR	DOC数据输入寄存器	0x02	16	read/ write	0x0000	0xFFFF
DOC	-	-	-	DODSR	DOC数据设置寄存器	0x04	16	read/ write	0x0000	0xFFFF
ADC120	-	-	-	ADCSR	AD控制寄存器	0x000	16	read/ write	0x0000	0xFFFF
ADC120	-	-	-	ADANSA0	AD通道选择寄存器 A0	0x004	16	read/ write	0x0000	0xFFFF
ADC120	-	-	-	ADANSA1	AD通道选择寄存器 A1	0x006	16	read/ write	0x0000	0xFFFF
ADC120	-	-	-	ADADS0	A/D-Converted Value Addition/Average Channel 选择寄存器0	0x008	16	read/ write	0x0000	0xFFFF
ADC120	-	-	-	ADADS1	A/D-Converted Value Addition/Average Channel 选择寄存器1	0x00A	16	read/ write	0x0000	0xFFFF
ADC120	-	-	-	ADADC	A/D-Converted Value Addition/Average Count 选择注册	0x00C	8	read/ write	0x00	0xFF
ADC120	-	-	-	ADCER	AD控制扩展 Register	0x00E	16	read/ write	0x0000	0xFFFF

Table 3.3 Register description (17 of 44)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
ADC120	-	-	-	ADSTRGR	A/D Conversion Start Trigger Select Register	0x010	16	read/ write	0x0000	0xFFFF
ADC120	-	-	-	ADEXICR	A/D Conversion Extended Input Control Register	0x012	16	read/ write	0x0000	0xFFFF
ADC120	-	-	-	ADANSB0	A/D Channel Select Register B0	0x014	16	read/ write	0x0000	0xFFFF
ADC120	-	-	-	ADANSB1	A/D Channel Select Register B1	0x016	16	read/ write	0x0000	0xFFFF
ADC120	-	-	-	ADDBLDR	A/D Data Duplication Register	0x018	16	read-only	0x0000	0xFFFF
ADC120	-	-	-	ADTSDR	A/D Temperature Sensor Data Register	0x01A	16	read-only	0x0000	0xFFFF
ADC120	-	-	-	ADOCDR	A/D Internal Reference Voltage Data Register	0x01C	16	read-only	0x0000	0xFFFF
ADC120	-	-	-	ADRD	A/D Self-Diagnosis Data Register	0x01E	16	read-only	0x0000	0xFFFF
ADC120	8	0x2	0-7	ADDR%s	A/D Data Register %s	0x020	16	read-only	0x0000	0xFFFF
ADC120	5	0x2	16-20	ADDR%s	A/D Data Register %s	0x040	16	read-only	0x0000	0xFFFF
ADC120	-	-	-	ADSHCR	A/D Sample and Hold Circuit Control Register	0x066	16	read/ write	0x0018	0xFFFF
ADC120	-	-	-	ADDISCR	A/D Disconnection Detection Control Register	0x07A	8	read/ write	0x00	0xFF
ADC120	-	-	-	ADSHMSR	A/D Sample and Hold Operation Mode Select Register	0x07C	8	read/ write	0x00	0xFF
ADC120	-	-	-	ADGSPCR	A/D Group Scan Priority Control Register	0x080	16	read/ write	0x0000	0xFFFF
ADC120	-	-	-	ADDBLDRA	A/D Data Duplication Register A	0x084	16	read-only	0x0000	0xFFFF
ADC120	-	-	-	ADDBLDRB	A/D Data Duplication Register B	0x086	16	read-only	0x0000	0xFFFF
ADC120	-	-	-	ADWINMON	A/D Compare Function Window A/B Status Monitor Register	0x08C	8	read/ write	0x00	0xFF
ADC120	-	-	-	ADCMPCR	A/D Compare Function Control Register	0x090	16	read/ write	0x0000	0xFFFF
ADC120	-	-	-	ADCMPANSER	A/D Compare Function Window A Extended Input Select Register	0x092	8	read/ write	0x00	0xFF
ADC120	-	-	-	ADCMPLER	A/D Compare Function Window A Extended Input Comparison Condition Setting Register	0x093	8	read/ write	0x00	0xFF
ADC120	-	-	-	ADCMPANSR0	A/D Compare Function Window A Channel Select Register 0	0x094	16	read/ write	0x0000	0xFFFF
ADC120	-	-	-	ADCMPANSR1	A/D Compare Function Window A Channel Select Register 1	0x096	16	read/ write	0x0000	0xFFFF
ADC120	-	-	-	ADCMPLR0	A/D Compare Function Window A Comparison Condition Setting Register 0	0x098	16	read/ write	0x0000	0xFFFF
ADC120	-	-	-	ADCMPLR1	A/D Compare Function Window A Comparison Condition Setting Register 1	0x09A	16	read/ write	0x0000	0xFFFF
ADC120	-	-	-	ADCMPDR0	A/D Compare Function Window A Lower-Side Level Setting Register	0x09C	16	read/ write	0x0000	0xFFFF

Table 3.3 寄存器说明（44个中的17个）

周边暗淡		昏暗的增量。	暗淡索引寄存器名称		Description	地址偏移	尺寸	访问	重置值	重置蒙版
ADC120	-	-	-	ADSTRGR	AD转换开始触发选择注册	0x010	16	read/ write	0x0000	0xFFFF
ADC120	-	-	-	ADEXICR	AD转换扩展输入控制寄存器	0x012	16	read/ write	0x0000	0xFFFF
ADC120	-	-	-	ADANSB0	AD通道选择寄存器B0	0x014	16	read/ write	0x0000	0xFFFF
ADC120	-	-	-	ADANSB1	AD通道选择寄存器B1	0x016	16	read/ write	0x0000	0xFFFF
ADC120	-	-	-	ADDBLDR	AD数据复制Register	0x018	16	只读	0x0000	0xFFFF
ADC120	-	-	-	ADTSDR	AD温度传感器数据寄存器	0x01A	16	只读	0x0000	0xFFFF
ADC120	-	-	-	ADOCDR	AD内部参考电压数据寄存器	0x01C	16	只读	0x0000	0xFFFF
ADC120	-	-	-	ADRD	A/D Self-Diagnosis Data Register	0x01E	16	只读	0x0000	0xFFFF
ADC120	8	0x2	0-7	ADDR%s	AD数据寄存器%s	0x020	16	只读	0x0000	0xFFFF
ADC120	5	0x2	16-20	ADDR%s	AD数据寄存器%s	0x040	16	只读	0x0000	0xFFFF
ADC120	-	-	-	ADSHCR	AD采样保持电路控制寄存器	0x066	16	read/ write	0x0018	0xFFFF
ADC120	-	-	-	ADDISCR	AD断线检测控制寄存器	0x07A	8	read/ write	0x00	0xFF
ADC120	-	-	-	ADSHMSR	AD采样和保持操作模式选择Register	0x07C	8	read/ write	0x00	0xFF
ADC120	-	-	-	ADGSPCR	AD组扫描优先级控制寄存器	0x080	16	read/ write	0x0000	0xFFFF
ADC120	-	-	-	ADDBLDRA	AD数据复制Register A	0x084	16	只读	0x0000	0xFFFF
ADC120	-	-	-	ADDBLDRB	AD数据复制Register B	0x086	16	只读	0x0000	0xFFFF
ADC120	-	-	-	ADWINMON	AD比较功能窗口AB状态监视器Register	0x08C	8	read/ write	0x00	0xFF
ADC120	-	-	-	ADCMPCR	AD比较功能控制寄存器	0x090	16	read/ write	0x0000	0xFFFF
ADC120	-	-	-	ADCMPANSER	AD比较功能窗口A扩展输入选择注册	0x092	8	read/ write	0x00	0xFF
ADC120	-	-	-	ADCMPLER	AD比较功能窗口A扩展输入比较条件设置寄存器	0x093	8	read/ write	0x00	0xFF
ADC120	-	-	-	ADCMPANSR0	AD比较功能窗口A通道选择Register 0	0x094	16	read/ write	0x0000	0xFFFF
ADC120	-	-	-	ADCMPANSR1	AD比较功能窗口A通道选择Register 1	0x096	16	read/ write	0x0000	0xFFFF
ADC120	-	-	-	ADCMPLR0	AD比较功能窗口A比较条件设置寄存器0	0x098	16	read/ write	0x0000	0xFFFF
ADC120	-	-	-	ADCMPLR1	AD比较功能窗口A比较条件设置寄存器1	0x09A	16	read/ write	0x0000	0xFFFF
ADC120	-	-	-	ADCMPDR0	AD比较功能窗口A下层设置寄存器	0x09C	16	read/ write	0x0000	0xFFFF

Table 3.3 Register description (18 of 44)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
ADC120	-	-	-	ADCMPDR1	A/D Compare Function Window A Upper-Side Level Setting Register	0x09E	16	read/ write	0x0000	0xFFFF
ADC120	-	-	-	ADCMPSR0	A/D Compare Function Window A Channel Status Register 0	0x0A0	16	read/ write	0x0000	0xFFFF
ADC120	-	-	-	ADCMPSR1	A/D Compare Function Window A Channel Status Register 1	0x0A2	16	read/ write	0x0000	0xFFFF
ADC120	-	-	-	ADCMPSER	A/D Compare Function Window A Extended Input Channel Status Register	0x0A4	8	read/ write	0x00	0xFF
ADC120	-	-	-	ADCMPBNSR	A/D Compare Function Window B Channel Selection Register	0x0A6	8	read/ write	0x00	0xFF
ADC120	-	-	-	ADWINLLB	A/D Compare Function Window B Lower-Side Level Setting Register	0x0A8	16	read/ write	0x0000	0xFFFF
ADC120	-	-	-	ADWINULB	A/D Compare Function Window B Upper-Side Level Setting Register	0x0AA	16	read/ write	0x0000	0xFFFF
ADC120	-	-	-	ADCMPBSR	A/D Compare Function Window B Status Register	0x0AC	16	read/ write	0x0000	0xFFFF
ADC120	-	-	-	ADSSTRL	A/D Sampling State Register L	0x0DD	8	read/ write	0x0B	0xFF
ADC120	-	-	-	ADSSTRT	A/D Sampling State Register T	0x0DE	8	read/ write	0x0B	0xFF
ADC120	-	-	-	ADSSTRO	A/D Sampling State Register O	0x0DF	8	read/ write	0x0B	0xFF
ADC120	8	0x1	0-7	ADSSTR0%s	A/D Sampling State Register %s (Corresponding Channel is AN00%s)	0x0E0	8	read/ write	0x0B	0xFF
ADC120	-	-	-	ADPGACR	A/D Programmable Gain Amplifier Control Register	0x1A0	16	read/ write	0x9999	0xFFFF
ADC120	-	-	-	ADPGAGS0	A/D Programmable Gain Amplifier Gain Setting Register 0	0x1A2	16	read/ write	0x0000	0xFFFF
ADC120	-	-	-	ADPGADCR0	A/D Programmable Gain Amplifier Differential Input Control Register	0x1B0	16	read/ write	0x0000	0xFFFF
ADC121	-	-	-	ADCSR	A/D Control Register	0x000	16	read/ write	0x0000	0xFFFF
ADC121	-	-	-	ADANSA0	A/D Channel Select Register A0	0x004	16	read/ write	0x0000	0xFFFF
ADC121	-	-	-	ADANSA1	A/D Channel Select Register A1	0x006	16	read/ write	0x0000	0xFFFF
ADC121	-	-	-	ADADS0	A/D-Converted Value Addition/Average Channel Select Register 0	0x008	16	read/ write	0x0000	0xFFFF
ADC121	-	-	-	ADADS1	A/D-Converted Value Addition/Average Channel Select Register 1	0x00A	16	read/ write	0x0000	0xFFFF
ADC121	-	-	-	ADADC	A/D-Converted Value Addition/Average Count Select Register	0x00C	8	read/ write	0x00	0xFF
ADC121	-	-	-	ADCER	A/D Control Extended Register	0x00E	16	read/ write	0x0000	0xFFFF
ADC121	-	-	-	ADSTRGR	A/D Conversion Start Trigger Select Register	0x010	16	read/ write	0x0000	0xFFFF
ADC121	-	-	-	ADEXICR	A/D Conversion Extended Input Control Register	0x012	16	read/ write	0x0000	0xFFFF

Table 3.3 寄存器说明（44中的18）

周边暗淡		昏暗的增量。		暗淡索引寄存器名称	Description	地址偏移	尺寸	访问	重置值	重置蒙版
ADC120	-	-	-	ADCMPDR1	AD比较功能 窗口A上层 设置寄存器	0x09E	16	read/ write	0x0000	0xFFFF
ADC120	-	-	-	ADCMPSR0	AD比较功能 窗口A通道状态 Register 0	0x0A0	16	read/ write	0x0000	0xFFFF
ADC120	-	-	-	ADCMPSR1	AD比较功能 窗口A通道状态 Register 1	0x0A2	16	read/ write	0x0000	0xFFFF
ADC120	-	-	-	ADCMPSER	AD比较功能窗口A扩展输入 通道状态寄存器	0x0A4	8	read/ write	0x00	0xFF
ADC120	-	-	-	ADCMPBNSR	AD比较功能 窗口B通道选择 Register	0x0A6	8	read/ write	0x00	0xFF
ADC120	-	-	-	ADWINLLB	AD比较功能 窗口B下层 设置寄存器	0x0A8	16	read/ write	0x0000	0xFFFF
ADC120	-	-	-	ADWINULB	AD比较功能 窗口B上层 设置寄存器	0x0AA	16	read/ write	0x0000	0xFFFF
ADC120	-	-	-	ADCMPBSR	AD比较功能 窗口B状态寄存器	0x0AC	16	read/ write	0x0000	0xFFFF
ADC120	-	-	-	ADSSTRL	AD采样状态寄存器 L	0x0DD	8	read/ write	0x0B	0xFF
ADC120	-	-	-	ADSSTRT	AD采样状态寄存器 T	0x0DE	8	read/ write	0x0B	0xFF
ADC120	-	-	-	ADSSTRO	AD采样状态寄存器 O	0x0DF	8	read/ write	0x0B	0xFF
ADC120	8	0x1	0-7	ADSSTR0%s	AD采样状态寄存器%s（对应通道为AN00%s）	0x0E0	8	read/ write	0x0B	0xFF
ADC120	-	-	-	ADPGACR	AD可编程增益放大器控制寄存器	0x1A0	16	read/ write	0x9999	0xFFFF
ADC120	-	-	-	ADPGAGS0	AD可编程增益 放大器增益设置 Register 0	0x1A2	16	read/ write	0x0000	0xFFFF
ADC120	-	-	-	ADPGADCR0	AD可编程增益放大器差分输入 控制寄存器	0x1B0	16	read/ write	0x0000	0xFFFF
ADC121	-	-	-	ADCSR	AD控制寄存器	0x000	16	read/ write	0x0000	0xFFFF
ADC121	-	-	-	ADANSA0	AD通道选择寄存器 A0	0x004	16	read/ write	0x0000	0xFFFF
ADC121	-	-	-	ADANSA1	AD通道选择寄存器 A1	0x006	16	read/ write	0x0000	0xFFFF
ADC121	-	-	-	ADADS0	A/D-Converted Value Addition/Average Channel 选择寄存器0	0x008	16	read/ write	0x0000	0xFFFF
ADC121	-	-	-	ADADS1	A/D-Converted Value Addition/Average Channel 选择寄存器1	0x00A	16	read/ write	0x0000	0xFFFF
ADC121	-	-	-	ADADC	A/D-Converted Value Addition/Average Count 选择注册	0x00C	8	read/ write	0x00	0xFF
ADC121	-	-	-	ADCER	AD控制扩展 Register	0x00E	16	read/ write	0x0000	0xFFFF
ADC121	-	-	-	ADSTRGR	AD转换开始触发 选择注册	0x010	16	read/ write	0x0000	0xFFFF
ADC121	-	-	-	ADEXICR	AD转换扩展 输入控制寄存器	0x012	16	read/ write	0x0000	0xFFFF

Table 3.3 Register description (19 of 44)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
ADC121	-	-	-	ADANSB0	A/D Channel Select Register B0	0x014	16	read/ write	0x0000	0xFFFF
ADC121	-	-	-	ADANSB1	A/D Channel Select Register B1	0x016	16	read/ write	0x0000	0xFFFF
ADC121	-	-	-	ADDBLDR	A/D Data Duplication Register	0x018	16	read-only	0x0000	0xFFFF
ADC121	-	-	-	ADTSDR	A/D Temperature Sensor Data Register	0x01A	16	read-only	0x0000	0xFFFF
ADC121	-	-	-	ADOCDR	A/D Internal Reference Voltage Data Register	0x01C	16	read-only	0x0000	0xFFFF
ADC121	-	-	-	ADRD	A/D Self-Diagnosis Data Register	0x01E	16	read-only	0x0000	0xFFFF
ADC121	4	0x2	0-3	ADDR%s	A/D Data Register %s	0x020	16	read-only	0x0000	0xFFFF
ADC121	3	0x2	5-7	ADDR%s	A/D Data Register %s	0x02A	16	read-only	0x0000	0xFFFF
ADC121	4	0x2	16-19	ADDR%s	A/D Data Register %s	0x040	16	read-only	0x0000	0xFFFF
ADC121	-	-	-	ADSHCR	A/D Sample and Hold Circuit Control Register	0x066	16	read/ write	0x0018	0xFFFF
ADC121	-	-	-	ADDISCR	A/D Disconnection Detection Control Register	0x07A	8	read/ write	0x00	0xFF
ADC121	-	-	-	ADSHMSR	A/D Sample and Hold Operation Mode Select Register	0x07C	8	read/ write	0x00	0xFF
ADC121	-	-	-	ADGSPCR	A/D Group Scan Priority Control Register	0x080	16	read/ write	0x0000	0xFFFF
ADC121	-	-	-	ADDBLDRA	A/D Data Duplication Register A	0x084	16	read-only	0x0000	0xFFFF
ADC121	-	-	-	ADDBLDRB	A/D Data Duplication Register B	0x086	16	read-only	0x0000	0xFFFF
ADC121	-	-	-	ADWINMON	A/D Compare Function Window A/B Status Monitor Register	0x08C	8	read/ write	0x00	0xFF
ADC121	-	-	-	ADCMPCR	A/D Compare Function Control Register	0x090	16	read/ write	0x0000	0xFFFF
ADC121	-	-	-	ADCMPANSER	A/D Compare Function Window A Extended Input Select Register	0x092	8	read/ write	0x00	0xFF
ADC121	-	-	-	ADCMPLER	A/D Compare Function Window A Extended Input Comparison Condition Setting Register	0x093	8	read/ write	0x00	0xFF
ADC121	-	-	-	ADCMPANSR0	A/D Compare Function Window A Channel Select Register 0	0x094	16	read/ write	0x0000	0xFFFF
ADC121	-	-	-	ADCMPANSR1	A/D Compare Function Window A Channel Select Register 1	0x096	16	read/ write	0x0000	0xFFFF
ADC121	-	-	-	ADCMPLR0	A/D Compare Function Window A Comparison Condition Setting Register 0	0x098	16	read/ write	0x0000	0xFFFF
ADC121	-	-	-	ADCMPLR1	A/D Compare Function Window A Comparison Condition Setting Register 1	0x09A	16	read/ write	0x0000	0xFFFF
ADC121	-	-	-	ADCMPDR0	A/D Compare Function Window A Lower-Side Level Setting Register	0x09C	16	read/ write	0x0000	0xFFFF
ADC121	-	-	-	ADCMPDR1	A/D Compare Function Window A Upper-Side Level Setting Register	0x09E	16	read/ write	0x0000	0xFFFF

Table 3.3 寄存器描述（44中的19）

周边暗淡		昏暗的增量。	暗淡索引寄存器名称		Description	地址偏移	尺寸	访问	重置值	重置蒙版
ADC121	-	-	-	ADANSB0	AD通道选择寄存器 B0	0x014	16	read/ write	0x0000	0xFFFF
ADC121	-	-	-	ADANSB1	AD通道选择寄存器 B1	0x016	16	read/ write	0x0000	0xFFFF
ADC121	-	-	-	ADDBLDR	AD数据复制 Register	0x018	16	只读	0x0000	0xFFFF
ADC121	-	-	-	ADTSDR	AD温度传感器 数据寄存器	0x01A	16	只读	0x0000	0xFFFF
ADC121	-	-	-	ADOCDR	AD内部参考 电压数据寄存器	0x01C	16	只读	0x0000	0xFFFF
ADC121	-	-	-	ADRD	A/D Self-Diagnosis Data Register	0x01E	16	只读	0x0000	0xFFFF
ADC121	4	0x2	0-3	ADDR%s	AD数据寄存器%s	0x020	16	只读	0x0000	0xFFFF
ADC121	3	0x2	5-7	ADDR%s	AD数据寄存器%s	0x02A	16	只读	0x0000	0xFFFF
ADC121	4	0x2	16-19	ADDR%s	AD数据寄存器%s	0x040	16	只读	0x0000	0xFFFF
ADC121	-	-	-	ADSHCR	AD采样保持电路 控制寄存器	0x066	16	read/ write	0x0018	0xFFFF
ADC121	-	-	-	ADDISCR	AD断线检测 控制寄存器	0x07A	8	read/ write	0x00	0xFF
ADC121	-	-	-	ADSHMSR	AD采样和保持操作模式 选择 Register	0x07C	8	read/ write	0x00	0xFF
ADC121	-	-	-	ADGSPCR	AD组扫描优先级 控制寄存器	0x080	16	read/ write	0x0000	0xFFFF
ADC121	-	-	-	ADDBLDRA	AD数据复制 Register A	0x084	16	只读	0x0000	0xFFFF
ADC121	-	-	-	ADDBLDRB	AD数据复制 Register B	0x086	16	只读	0x0000	0xFFFF
ADC121	-	-	-	ADWINMON	AD比较功能 窗口AB状态监视器 Register	0x08C	8	read/ write	0x00	0xFF
ADC121	-	-	-	ADCMPCR	AD比较功能 控制寄存器	0x090	16	read/ write	0x0000	0xFFFF
ADC121	-	-	-	ADCMPANSER	AD比较功能 窗口A扩展输入 选择注册	0x092	8	read/ write	0x00	0xFF
ADC121	-	-	-	ADCMPLER	AD比较功能窗口A扩展输入 比较条件 设置寄存器	0x093	8	read/ write	0x00	0xFF
ADC121	-	-	-	ADCMPANSR0	AD比较功能 窗口A通道选择 Register 0	0x094	16	read/ write	0x0000	0xFFFF
ADC121	-	-	-	ADCMPANSR1	AD比较功能 窗口A通道选择 Register 1	0x096	16	read/ write	0x0000	0xFFFF
ADC121	-	-	-	ADCMPLR0	AD比较功能窗口A比较 条件设置寄存器0	0x098	16	read/ write	0x0000	0xFFFF
ADC121	-	-	-	ADCMPLR1	AD比较功能窗口A比较 条件设置寄存器1	0x09A	16	read/ write	0x0000	0xFFFF
ADC121	-	-	-	ADCMPDR0	AD比较功能 窗口A下层 设置寄存器	0x09C	16	read/ write	0x0000	0xFFFF
ADC121	-	-	-	ADCMPDR1	AD比较功能 窗口A上层 设置寄存器	0x09E	16	read/ write	0x0000	0xFFFF

Table 3.3 Register description (20 of 44)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
ADC121	-	-	-	ADCMPSR0	A/D Compare Function Window A Channel Status Register 0	0x0A0	16	read/ write	0x0000	0xFFFF
ADC121	-	-	-	ADCMPSR1	A/D Compare Function Window A Channel Status Register 1	0x0A2	16	read/ write	0x0000	0xFFFF
ADC121	-	-	-	ADCMPSER	A/D Compare Function Window A Extended Input Channel Status Register	0x0A4	8	read/ write	0x00	0xFF
ADC121	-	-	-	ADCMPBNSR	A/D Compare Function Window B Channel Selection Register	0x0A6	8	read/ write	0x00	0xFF
ADC121	-	-	-	ADWINLLB	A/D Compare Function Window B Lower-Side Level Setting Register	0x0A8	16	read/ write	0x0000	0xFFFF
ADC121	-	-	-	ADWINULB	A/D Compare Function Window B Upper-Side Level Setting Register	0x0AA	16	read/ write	0x0000	0xFFFF
ADC121	-	-	-	ADCMPBSR	A/D Compare Function Window B Status Register	0x0AC	16	read/ write	0x0000	0xFFFF
ADC121	-	-	-	ADSSTRL	A/D Sampling State Register L	0x0DD	8	read/ write	0x0B	0xFF
ADC121	-	-	-	ADSSTRT	A/D Sampling State Register T	0x0DE	8	read/ write	0x0B	0xFF
ADC121	-	-	-	ADSSTRO	A/D Sampling State Register O	0x0DF	8	read/ write	0x0B	0xFF
ADC121	4	0x1	0-3	ADSSTR0%s	A/D Sampling State Register %s (Corresponding Channel is AN10%s)	0x0E0	8	read/ write	0x0B	0xFF
ADC121	3	0x1	5-7	ADSSTR0%s	A/D Sampling State Register %s (Corresponding Channel is AN10%s)	0x0E5	8	read/ write	0x0B	0xFF
ADC121	-	-	-	ADPGACR	A/D Programmable Gain Amplifier Control Register	0x1A0	16	read/ write	0x9999	0xFFFF
ADC121	-	-	-	ADPGAGS0	A/D Programmable Gain Amplifier Gain Setting Register 0	0x1A2	16	read/ write	0x0000	0xFFFF
ADC121	-	-	-	ADPGADCR0	A/D Programmable Gain Amplifier Differential Input Control Register	0x1B0	16	read/ write	0x0000	0xFFFF
TSN	-	-	-	TSCR	Temperature Sensor Control Register	0x00	8	read/ write	0x00	0xFF
DAC12	2	0x2	0,1	DADR%s	D/A Data Register %s	0x00	16	read/ write	0x0000	0xFFFF
DAC12	-	-	-	DACR	D/A Control Register	0x0004	8	read/ write	0x1F	0xFF
DAC12	-	-	-	DADPR	DADRm Format Select Register	0x0005	8	read/ write	0x00	0xFF
DAC12	-	-	-	DAADSCR	D/A-A/D Synchronous Start Control Register	0x0006	8	read/ write	0x00	0xFF
DAC12	-	-	-	DAAMPCR	D/A Output Amplifier Control Register	0x0008	8	read/ write	0x00	0xFF
DAC12	-	-	-	DAASWCR	D/A Amplifier Stabilization Wait Control Register	0x001C	8	read/ write	0x00	0xFF
DAC12	-	-	-	DAADUSR	D/A A/D Synchronous Unit Select Register	0xC0	8	read/ write	0x00	0xFF
USBHS	-	-	-	SYSCFG	System Configuration Control Register	0x000	16	read/ write	0x0020	0xFFFF
USBHS	-	-	-	BUSWAIT	CPU Bus Wait Register	0x002	16	read/ write	0x000F	0x3F3F

Table 3.3 寄存器说明（44个中的20个）

周边暗淡		昏暗的增量。		暗淡索引寄存器名称	Description	地址偏移	尺寸	访问	重置值	重置蒙版
ADC121	-	-	-	ADCMPSR0	AD比较功能 窗口A通道状态 Register 0	0x0A0	16	read/ write	0x0000	0xFFFF
ADC121	-	-	-	ADCMPSR1	AD比较功能 窗口A通道状态 Register 1	0x0A2	16	read/ write	0x0000	0xFFFF
ADC121	-	-	-	ADCMPSER	AD比较功能窗口A扩展输入 通道状态寄存器	0x0A4	8	read/ write	0x00	0xFF
ADC121	-	-	-	ADCMPBNSR	AD比较功能 窗口B通道选择 Register	0x0A6	8	read/ write	0x00	0xFF
ADC121	-	-	-	ADWINLLB	AD比较功能 窗口B下层 设置寄存器	0x0A8	16	read/ write	0x0000	0xFFFF
ADC121	-	-	-	ADWINULB	AD比较功能 窗口B上层 设置寄存器	0x0AA	16	read/ write	0x0000	0xFFFF
ADC121	-	-	-	ADCMPBSR	AD比较功能 窗口B状态寄存器	0x0AC	16	read/ write	0x0000	0xFFFF
ADC121	-	-	-	ADSSTRL	AD采样状态寄存器 L	0x0DD	8	read/ write	0x0B	0xFF
ADC121	-	-	-	ADSSTRT	AD采样状态寄存器 T	0x0DE	8	read/ write	0x0B	0xFF
ADC121	-	-	-	ADSSTRO	AD采样状态寄存器 O	0x0DF	8	read/ write	0x0B	0xFF
ADC121	4	0x1	0-3	ADSSTR0%s	AD采样状态寄存器%s（对应通道为AN10%s）	0x0E0	8	read/ write	0x0B	0xFF
ADC121	3	0x1	5-7	ADSSTR0%s	AD采样状态寄存器%s（对应通道为AN10%s）	0x0E5	8	read/ write	0x0B	0xFF
ADC121	-	-	-	ADPGACR	AD可编程增益放大器控制寄存器	0x1A0	16	read/ write	0x9999	0xFFFF
ADC121	-	-	-	ADPGAGS0	AD可编程增益 放大器增益设置 Register 0	0x1A2	16	read/ write	0x0000	0xFFFF
ADC121	-	-	-	ADPGADCR0	AD可编程增益放大器差分输入 控制寄存器	0x1B0	16	read/ write	0x0000	0xFFFF
TSN	-	-	-	TSCR	温度传感器控制 Register	0x00	8	read/ write	0x00	0xFF
DAC12	2	0x2	0,1	DADR%s	DA数据寄存器%s	0x00	16	read/ write	0x0000	0xFFFF
DAC12	-	-	-	DACR	DA控制寄存器	0x0004	8	read/ write	0x1F	0xFF
DAC12	-	-	-	DADPR	DADRm格式选择 Register	0x0005	8	read/ write	0x00	0xFF
DAC12	-	-	-	DAADSCR	DA-AD同步启动 控制寄存器	0x0006	8	read/ write	0x00	0xFF
DAC12	-	-	-	DAAMPCR	DA输出放大器控制 Register	0x0008	8	read/ write	0x00	0xFF
DAC12	-	-	-	DAASWCR	DA放大器稳定 等待控制寄存器	0x001C	8	read/ write	0x00	0xFF
DAC12	-	-	-	DAADUSR	DAAD同步单元 选择注册	0xC0	8	read/ write	0x00	0xFF
USBHS	-	-	-	SYSCFG	系统配置 控制寄存器	0x000	16	read/ write	0x0020	0xFFFF
USBHS	-	-	-	BUSWAIT	CPU总线等待寄存器	0x002	16	read/ write	0x000F	0x3F3F

Table 3.3 Register description (21 of 44)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
USBHS	-	-	-	SYSSTS0	System Configuration Status Register	0x004	16	read-only	0x0000	0x0000
USBHS	-	-	-	PLLSTA	PLL Status Register	0x006	16	read-only	0x0000	0x0001
USBHS	-	-	-	DVSTCTR0	Device State Control Register 0	0x008	16	read/write	0x0000	0x07F7
USBHS	-	-	-	TESTMODE	USB Test Mode Register	0x00C	16	read/write	0x0000	0x000F
USBHS	-	-	-	CFIFO	CFIFO Port Register	0x014	32	read/write	0x00000000	0xFFFFFFFF
USBHS	-	-	-	CFIFOL	CFIFO Port Register L	0x014	16	read/write	0x0000	0xFFFF
USBHS	-	-	-	CFIFOLL	CFIFO Port Register LL	0x014	8	read/write	0x00	0xFF
USBHS	-	-	-	CFIFOH	CFIFO Port Register H	0x016	16	read/write	0x0000	0xFFFF
USBHS	-	-	-	CFIFOHH	CFIFO Port Register HH	0x017	8	read/write	0x00	0xFF
USBHS	-	-	-	D0FIFO	D0FIFO Port Register	0x018	32	read/write	0x00000000	0xFFFFFFFF
USBHS	-	-	-	D0FIFOL	D0FIFO Port Register L	0x018	16	read/write	0x0000	0xFFFF
USBHS	-	-	-	D0FIFOLL	D0FIFO Port Register LL	0x018	8	read/write	0x00	0xFF
USBHS	-	-	-	D0FIFOH	D0FIFO Port Register H	0x01A	16	read/write	0x0000	0xFFFF
USBHS	-	-	-	D0FIFOHH	D0FIFO Port Register HH	0x01B	8	read/write	0x00	0xFF
USBHS	-	-	-	D1FIFO	D1FIFO Port Register	0x01C	32	read/write	0x00000000	0xFFFFFFFF
USBHS	-	-	-	D1FIFOL	D1FIFO Port Register L	0x01C	16	read/write	0x0000	0xFFFF
USBHS	-	-	-	D1FIFOLL	D1FIFO Port Register LL	0x01C	8	read/write	0x00	0xFF
USBHS	-	-	-	D1FIFOH	D1FIFO Port Register H	0x01E	16	read/write	0x0000	0xFFFF
USBHS	-	-	-	D1FIFOHH	D1FIFO Port Register HH	0x01F	8	read/write	0x00	0xFF
USBHS	-	-	-	CFIFOSEL	CFIFO Port Select Register	0x020	16	read/write	0x0000	0xCD27
USBHS	-	-	-	CFIFOCTR	CFIFO Port Control Register	0x022	16	read/write	0x0000	0xEFFE
USBHS	-	-	-	D0FIFOSEL	D0FIFO Port Select Register	0x028	16	read/write	0x0000	0xFD07
USBHS	-	-	-	D0FIFOCTR	D0FIFO Port Control Register	0x02A	16	read/write	0x0000	0xEFFE
USBHS	-	-	-	D1FIFOSEL	D1FIFO Port Select Register	0x02C	16	read/write	0x0000	0xFD07
USBHS	-	-	-	D1FIFOCTR	D1FIFO Port Control Register	0x02E	16	read/write	0x0000	0xEFFE
USBHS	-	-	-	INTENB0	Interrupt Enable Register 0	0x030	16	read/write	0x0000	0xFF00
USBHS	-	-	-	INTENB1	Interrupt Enable Register 1	0x032	16	read/write	0x0000	0xDB71
USBHS	-	-	-	BRDYENB	BRDY Interrupt Enable Register	0x036	16	read/write	0x0000	0xFFFF
USBHS	-	-	-	NRDYENB	NRDY Interrupt Enable Register	0x038	16	read/write	0x0000	0xFFFF
USBHS	-	-	-	BEMPENB	BEMP Interrupt Enable Register	0x03A	16	read/write	0x0000	0xFFFF

Table 3.3 寄存器说明（44个中的21个）

周边暗淡		昏暗的增量。	暗淡索引寄存器名称		Description	地址偏移	尺寸	访问	重置值	重置蒙版
USBHS	-	-	-	SYSSTS0	系统配置状态 Register	0x004	16	只读	0x0000	0x0000
USBHS	-	-	-	PLLSTA	PLL状态寄存器	0x006	16	只读	0x0000	0x0001
USBHS	-	-	-	DVSTCTR0	设备状态控制 Register 0	0x008	16	read/write	0x0000	0x07F7
USBHS	-	-	-	TESTMODE	USB测试模式寄存器	0x00C	16	read/write	0x0000	0x000F
USBHS	-	-	-	CFIFO	CFIFO端口寄存器	0x014	32	read/write	0x00000000	0xFFFFFFFF
USBHS	-	-	-	CFIFOL	CFIFO端口寄存器L	0x014	16	read/write	0x0000	0xFFFF
USBHS	-	-	-	CFIFOLL	CFIFO端口寄存器LL	0x014	8	read/write	0x00	0xFF
USBHS	-	-	-	CFIFOH	CFIFO端口寄存器H	0x016	16	read/write	0x0000	0xFFFF
USBHS	-	-	-	CFIFOHH	CFIFO端口寄存器HH	0x017	8	read/write	0x00	0xFF
USBHS	-	-	-	D0FIFO	D0FIFO端口寄存器	0x018	32	read/write	0x00000000	0xFFFFFFFF
USBHS	-	-	-	D0FIFOL	D0FIFO端口寄存器L	0x018	16	read/write	0x0000	0xFFFF
USBHS	-	-	-	D0FIFOLL	D0FIFO端口寄存器LL	0x018	8	read/write	0x00	0xFF
USBHS	-	-	-	D0FIFOH	D0FIFO端口寄存器H	0x01A	16	read/write	0x0000	0xFFFF
USBHS	-	-	-	D0FIFOHH	D0FIFO端口寄存器HH	0x01B	8	read/write	0x00	0xFF
USBHS	-	-	-	D1FIFO	D1FIFO端口寄存器	0x01C	32	read/write	0x00000000	0xFFFFFFFF
USBHS	-	-	-	D1FIFOL	D1FIFO端口寄存器L	0x01C	16	read/write	0x0000	0xFFFF
USBHS	-	-	-	D1FIFOLL	D1FIFO端口寄存器LL	0x01C	8	read/write	0x00	0xFF
USBHS	-	-	-	D1FIFOH	D1FIFO端口寄存器H	0x01E	16	read/write	0x0000	0xFFFF
USBHS	-	-	-	D1FIFOHH	D1FIFO端口寄存器HH	0x01F	8	read/write	0x00	0xFF
USBHS	-	-	-	CFIFOSEL	CFIFO端口选择寄存器	0x020	16	read/write	0x0000	0xCD27
USBHS	-	-	-	CFIFOCTR	CFIFO端口控制寄存器0x022		16	read/write	0x0000	0xEFFE
USBHS	-	-	-	D0FIFOSEL	D0FIFO端口选择寄存器0x028		16	read/write	0x0000	0xFD07
USBHS	-	-	-	D0FIFOCTR	D0FIFO端口控制 Register	0x02A	16	read/write	0x0000	0xEFFE
USBHS	-	-	-	D1FIFOSEL	D1FIFO端口选择寄存器0x02C		16	read/write	0x0000	0xFD07
USBHS	-	-	-	D1FIFOCTR	D1FIFO端口控制 Register	0x02E	16	read/write	0x0000	0xEFFE
USBHS	-	-	-	INTENB0	中断使能寄存器0	0x030	16	read/write	0x0000	0xFF00
USBHS	-	-	-	INTENB1	中断使能寄存器1	0x032	16	read/write	0x0000	0xDB71
USBHS	-	-	-	BRDYENB	BRDY中断使能 Register	0x036	16	read/write	0x0000	0xFFFF
USBHS	-	-	-	NRDYENB	NRDY中断使能 Register	0x038	16	read/write	0x0000	0xFFFF
USBHS	-	-	-	BEMPENB	BEMP中断使能 Register	0x03A	16	read/write	0x0000	0xFFFF

Table 3.3 Register description (22 of 44)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
USBHS	-	-	-	SOFCFG	SOF Pin Configuration Register	0x03C	16	read/ write	0x0000	0x0170
USBHS	-	-	-	PHYSET	PHY Setting Register	0x03E	16	read/ write	0x0033	0x8B3B
USBHS	-	-	-	INTSTS0	Interrupt Status Register 0	0x040	16	read/ write	0x0000	0xFF7F
USBHS	-	-	-	INTSTS1	Interrupt Status Register 1	0x042	16	read/ write	0x0000	0xDB71
USBHS	-	-	-	BRDYSTS	BRDY Interrupt Status Register	0x046	16	read/ write	0x0000	0xFFFF
USBHS	-	-	-	NRDYSTS	NRDY Interrupt Status Register	0x048	16	read/ write	0x0000	0xFFFF
USBHS	-	-	-	BEMPSTS	BEMP Interrupt Status Register	0x04A	16	read/ write	0x0000	0xFFFF
USBHS	-	-	-	FRMNUM	Frame Number Register	0x04C	16	read/ write	0x0000	0xC7FF
USBHS	-	-	-	UFRMNUM	uFrame Number Register	0x04E	16	read/ write	0x0000	0x0007
USBHS	-	-	-	USBADDR	USB Address Register	0x050	16	read/ write	0x0000	0x007F
USBHS	-	-	-	USBREQ	USB Request Type Register	0x054	16	read/ write	0x0000	0xFFFF
USBHS	-	-	-	USBVAL	USB Request Value Register	0x056	16	read/ write	0x0000	0xFFFF
USBHS	-	-	-	USBINDX	USB Request Index Register	0x058	16	read/ write	0x0000	0xFFFF
USBHS	-	-	-	USBLENG	USB Request Length Register	0x05A	16	read/ write	0x0000	0xFFFF
USBHS	-	-	-	DCPCFG	DCP Configuration Register	0x05C	16	read/ write	0x0000	0x0190
USBHS	-	-	-	DCPMAXP	DCP Maximum Packet Size Register	0x05E	16	read/ write	0x0040	0xF07F
USBHS	-	-	-	DCPCTR	DCP Control Register	0x060	16	read/ write	0x0000	0xF1F7
USBHS	-	-	-	PIPESEL	Pipe Window Select Register	0x064	16	read/ write	0x0000	0x000F
USBHS	-	-	-	PIPECFG	Pipe Configuration Register	0x068	16	read/ write	0x0000	0xC79F
USBHS	-	-	-	PIPEBUF	Pipe Buffer Register	0x06A	16	read/ write	0x0000	0x7CFF
USBHS	-	-	-	PIPEMAXP	Pipe Maximum Packet Size Register	0x06C	16	read/ write	0x0000	0xF7FF
USBHS	-	-	-	PIPEPERI	Pipe Cycle Control Register	0x06E	16	read/ write	0x0000	0x1007
USBHS	9	0x002	1-9	PIPE%sCTR	PIPE Control Register	0x070	16	read/ write	0x0000	0xF7E3
USBHS	5	0x004	1-5	PIPE%sTRE	PIPE Transaction Counter Enable Register	0x090	16	read/ write	0x0000	0x0300
USBHS	5	0x004	1-5	PIPE%sTRN	PIPE Transaction Counter Register	0x092	16	read/ write	0x0000	0xFFFF
USBHS	10	0x002	0-9	DEVADD%s	Device Address Configuration Register	0x0D0	16	read/ write	0x0000	0x7FC0
USBHS	-	-	-	DEVADDA	Device Address Configuration Register A	0x0E4	16	read/ write	0x0000	0x7FC0
USBHS	-	-	-	LPCTRL	Low Power Control Register	0x100	16	read/ write	0x0000	0x0081
USBHS	-	-	-	LPSTS	Low Power Status Register	0x102	16	read/ write	0x0000	0x4000
USBHS	-	-	-	BCCTRL	Battery Charging Control Register	0x140	16	read/ write	0x0000	0x033F

Table 3.3 寄存器说明（44中的22）

周边暗淡	昏暗的增量。	暗淡索引寄存器名称		Description	地址偏移	尺寸	访问	重置值	重置蒙版
USBHS	-	-	-	SOFCFG	SOF引脚配置 Register	0x03C	16	read/ write	0x0000	0x0170
USBHS	-	-	-	PHYSET	PHY设置寄存器	0x03E	16	read/ write	0x0033	0x8B3B
USBHS	-	-	-	INTSTS0	中断状态寄存器0	0x040	16	read/ write	0x0000	0xFF7F
USBHS	-	-	-	INTSTS1	中断状态寄存器1	0x042	16	read/ write	0x0000	0xDB71
USBHS	-	-	-	BRDYSTS	BRDY中断状态 Register	0x046	16	read/ write	0x0000	0xFFFF
USBHS	-	-	-	NRDYSTS	NRDY中断状态 Register	0x048	16	read/ write	0x0000	0xFFFF
USBHS	-	-	-	BEMPSTS	BEMP中断状态 Register	0x04A	16	read/ write	0x0000	0xFFFF
USBHS	-	-	-	FRMNUM	帧号寄存器	0x04C	16	read/ write	0x0000	0xC7FF
USBHS	-	-	-	UFRMNUM	uFrame编号寄存器	0x04E	16	read/ write	0x0000	0x0007
USBHS	-	-	-	USBADDR	USB地址寄存器	0x050	16	read/ write	0x0000	0x007F
USBHS	-	-	-	USBREQ	USB请求类型寄存器	0x054	16	read/ write	0x0000	0xFFFF
USBHS	-	-	-	USBVAL	USB请求值寄存器0x 056		16	read/ write	0x0000	0xFFFF
USBHS	-	-	-	USBINDX	USB请求索引寄存器0x 058		16	read/ write	0x0000	0xFFFF
USBHS	-	-	-	USBLENG	USB请求长度 Register	0x05A	16	read/ write	0x0000	0xFFFF
USBHS	-	-	-	DCPCFG	DCP配置寄存器	0x05C	16	read/ write	0x0000	0x0190
USBHS	-	-	-	DCPMAXP	DCP最大数据包大小 Register	0x05E	16	read/ write	0x0040	0xF07F
USBHS	-	-	-	DCPCTR	DCP控制寄存器	0x060	16	read/ write	0x0000	0xF1F7
USBHS	-	-	-	PIPESEL	管道窗口选择寄存器0x 064		16	read/ write	0x0000	0x000F
USBHS	-	-	-	PIPECFG	管道配置寄存器	0x068	16	read/ write	0x0000	0xC79F
USBHS	-	-	-	PIPEBUF	管道缓冲寄存器	0x06A	16	read/ write	0x0000	0x7CFF
USBHS	-	-	-	PIPEMAXP	管道最大数据包大小 Register	0x06C	16	read/ write	0x0000	0xF7FF
USBHS	-	-	-	PIPEPERI	管道循环控制寄存器	0x06E	16	read/ write	0x0000	0x1007
USBHS	9	0x002	1-9	PIPE%sCTR	管道控制寄存器	0x070	16	read/ write	0x0000	0xF7E3
USBHS	5	0x004	1-5	PIPE%sTRE	管道交易计数器 启用注册	0x090	16	read/ write	0x0000	0x0300
USBHS	5	0x004	1-5	PIPE%sTRN	管道交易计数器 Register	0x092	16	read/ write	0x0000	0xFFFF
USBHS	10	0x002	0-9	DEVADD%s	设备地址 配置寄存器	0x0D0	16	read/ write	0x0000	0x7FC0
USBHS	-	-	-	DEVADDA	设备地址 配置寄存器A	0x0E4	16	read/ write	0x0000	0x7FC0
USBHS	-	-	-	LPCTRL	低功耗控制寄存器	0x100	16	read/ write	0x0000	0x0081
USBHS	-	-	-	LPSTS	低功耗状态寄存器	0x102	16	read/ write	0x0000	0x4000
USBHS	-	-	-	BCCTRL	电池充电控制 Register	0x140	16	read/ write	0x0000	0x033F

Table 3.3 Register description (23 of 44)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
USBHS	-	-	-	PL1CTRL1	Function L1 Control Register 1	0x144	16	read/ write	0x0000	0x4FFF
USBHS	-	-	-	PL1CTRL2	Function L1 Control Register 2	0x146	16	read/ write	0x0000	0x1F00
USBHS	-	-	-	HL1CTRL1	Host L1 Control Register 1	0x148	16	read/ write	0x0000	0x0007
USBHS	-	-	-	HL1CTRL2	Host L1 Control Register 2	0x14A	16	read/ write	0x0000	0x9F0F
USBHS	-	-	-	PHYTRIM1	PHY Timing Register 1	0x150	16	read/ write	0x0605	0x7F8F
USBHS	-	-	-	PHYTRIM2	PHY Timing Register 2	0x152	16	read/ write	0x1106	0x738F
USBHS	-	-	-	DPUSR0R	Deep Standby USB Transceiver Control/Pin Monitor Register	0x160	32	read/ write	0x00000000	0xFF4FFFFF
USBHS	-	-	-	DPUSR1R	Deep Standby USB Suspend/Resume Interrupt Register	0x164	32	read/ write	0x00000000	0xFFFFFFFF
USBHS	-	-	-	DPUSR2R	Deep Standby USB Suspend/Resume Interrupt Register	0x168	16	read/ write	0x0000	0xFFFF
USBHS	-	-	-	DPUSRCR	Deep Standby USB Suspend/Resume Command Register	0x16A	16	read/ write	0x0000	0xFFFF
SDHI0,1	-	-	-	SD_CMD	Command Type Register	0x000	32	read/ write	0x00000000	0xFFFFFFFF
SDHI0,1	-	-	-	SD_ARG	SD Command Argument Register	0x008	32	read/ write	0x00000000	0xFFFFFFFF
SDHI0,1	-	-	-	SD_ARG1	SD Command Argument Register 1	0x00C	32	read/ write	0x00000000	0xFFFFFFFF
SDHI0,1	-	-	-	SD_STOP	Data Stop Register	0x010	32	read/ write	0x00000000	0xFFFFFFFF
SDHI0,1	-	-	-	SD_SECCNT	Block Count Register	0x014	32	read/ write	0x00000000	0xFFFFFFFF
SDHI0,1	-	-	-	SD_RSP10	SD Card Response Register 10	0x018	32	read-only	0x00000000	0xFFFFFFFF
SDHI0,1	-	-	-	SD_RSP1	SD Card Response Register 1	0x01C	32	read-only	0x00000000	0xFFFFFFFF
SDHI0,1	-	-	-	SD_RSP32	SD Card Response Register 32	0x020	32	read-only	0x00000000	0xFFFFFFFF
SDHI0,1	-	-	-	SD_RSP3	SD Card Response Register 3	0x024	32	read-only	0x00000000	0xFFFFFFFF
SDHI0,1	-	-	-	SD_RSP54	SD Card Response Register 54	0x028	32	read-only	0x00000000	0xFFFFFFFF
SDHI0,1	-	-	-	SD_RSP5	SD Card Response Register 5	0x02C	32	read-only	0x00000000	0xFFFFFFFF
SDHI0,1	-	-	-	SD_RSP76	SD Card Response Register 76	0x030	32	read-only	0x00000000	0xFFFFFFFF
SDHI0,1	-	-	-	SD_RSP7	SD Card Response Register 7	0x034	32	read-only	0x00000000	0xFFFFFFFF
SDHI0,1	-	-	-	SD_INFO1	SD Card Interrupt Flag Register 1	0x038	32	read/ write	0x00000000	0xFFFFFB5F
SDHI0,1	-	-	-	SD_INFO2	SD Card Interrupt Flag Register 2	0x03C	32	read/ write	0x00002000	0xFFFFFF7F
SDHI0,1	-	-	-	SD_INFO1_MASK	SD_INFO1 Interrupt Mask Register	0x040	32	read/ write	0x0000031D	0xFFFFFFFF
SDHI0,1	-	-	-	SD_INFO2_MASK	SD_INFO2 Interrupt Mask Register	0x044	32	read/ write	0x00008B7F	0xFFFFFFFF
SDHI0,1	-	-	-	SD_CLK_CTRL	SD Clock Control Register	0x048	32	read/ write	0x00000020	0xFFFFFFFF

Table 3.3 寄存器说明（44个中的23个）

周边暗淡	昏暗的增量。	暗淡索引寄存器名称		Description	地址偏移	尺寸	访问	重置值	重置蒙版
USBHS	-	-	PL1CTRL1	功能L1控制寄存器1	0x144	16	read/ write	0x0000	0x4FFF
USBHS	-	-	PL1CTRL2	功能L1控制寄存器2	0x146	16	read/ write	0x0000	0x1F00
USBHS	-	-	HL1CTRL1	主机L1控制寄存器1	0x148	16	read/ write	0x0000	0x0007
USBHS	-	-	HL1CTRL2	主机L1控制寄存器2	0x14A	16	read/ write	0x0000	0x9F0F
USBHS	-	-	PHYTRIM1	PHY时序寄存器1	0x150	16	read/ write	0x0605	0x7F8F
USBHS	-	-	PHYTRIM2	PHY时序寄存器2	0x152	16	read/ write	0x1106	0x738F
USBHS	-	-	DPUSR0R	深度待机USB Transceiver Control/Pin 监控寄存器	0x160	32	read/ write	0x00000000	0xFF4FFFFF
USBHS	-	-	DPUSR1R	深度待机USB Suspend/Resume Interrupt Register	0x164	32	read/ write	0x00000000	0xFFFFFFFF
USBHS	-	-	DPUSR2R	深度待机USB Suspend/Resume Interrupt Register	0x168	16	read/ write	0x0000	0xFFFF
USBHS	-	-	DPUSRCR	深度待机USB Suspend/Resume Command Register	0x16A	16	read/ write	0x0000	0xFFFF
SDHI0,1	-	-	SD_CMD	命令类型寄存器	0x000	32	read/ write	0x00000000	0xFFFFFFFF
SDHI0,1	-	-	SD_ARG	SD命令参数 Register	0x008	32	read/ write	0x00000000	0xFFFFFFFF
SDHI0,1	-	-	SD_ARG1	SD命令参数 Register 1	0x00C	32	read/ write	0x00000000	0xFFFFFFFF
SDHI0,1	-	-	SD_STOP	数据停止寄存器	0x010	32	read/ write	0x00000000	0xFFFFFFFF
SDHI0,1	-	-	SD_SECCNT	块计数寄存器	0x014	32	read/ write	0x00000000	0xFFFFFFFF
SDHI0,1	-	-	SD_RSP10	SD卡响应寄存器10	0x018	32	只读	0x00000000	0xFFFFFFFF
SDHI0,1	-	-	SD_RSP1	SD卡响应寄存器1	0x01C	32	只读	0x00000000	0xFFFFFFFF
SDHI0,1	-	-	SD_RSP32	SD卡响应寄存器32	0x020	32	只读	0x00000000	0xFFFFFFFF
SDHI0,1	-	-	SD_RSP3	SD卡响应寄存器3	0x024	32	只读	0x00000000	0xFFFFFFFF
SDHI0,1	-	-	SD_RSP54	SD卡响应寄存器54	0x028	32	只读	0x00000000	0xFFFFFFFF
SDHI0,1	-	-	SD_RSP5	SD卡响应寄存器5	0x02C	32	只读	0x00000000	0xFFFFFFFF
SDHI0,1	-	-	SD_RSP76	SD卡响应寄存器76	0x030	32	只读	0x00000000	0xFFFFFFFF
SDHI0,1	-	-	SD_RSP7	SD卡响应寄存器7	0x034	32	只读	0x00000000	0xFFFFFFFF
SDHI0,1	-	-	SD_INFO1	SD卡中断标志 Register 1	0x038	32	read/ write	0x00000000	0xFFFFFB5F
SDHI0,1	-	-	SD_INFO2	SD卡中断标志 Register 2	0x03C	32	read/ write	0x00002000	0xFFFFFF7F
SDHI0,1	-	-	SD_INFO1_MASK	SD_INFO1中断屏蔽 Register	0x040	32	read/ write	0x0000031D	0xFFFFFFFF
SDHI0,1	-	-	SD_INFO2_MASK	SD_INFO2中断屏蔽 Register	0x044	32	read/ write	0x00008B7F	0xFFFFFFFF
SDHI0,1	-	-	SD_CLK_CTRL	SD时钟控制寄存器	0x048	32	read/ write	0x00000020	0xFFFFFFFF

Table 3.3 Register description (24 of 44)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
SDHI0,1	-	-	-	SD_SIZE	Transfer Data Length Register	0x04C	32	read/ write	0x00000200	0xFFFFFFFF
SDHI0,1	-	-	-	SD_OPTION	SD Card Access Control Option Register	0x050	32	read/ write	0x000040EE	0xFFFFFFFF
SDHI0,1	-	-	-	SD_ERR_STS1	SD Error Status Register 1	0x058	32	read-only	0x00002000	0xFFFFFFFF
SDHI0,1	-	-	-	SD_ERR_STS2	SD Error Status Register 2	0x05C	32	read-only	0x00000000	0xFFFFFFFF
SDHI0,1	-	-	-	SD_BUF0	SD Buffer Register	0x060	32	read/ write	0x00000000	0x00000000
SDHI0,1	-	-	-	SDIO_MODE	SDIO Mode Control Register	0x068	32	read/ write	0x00000000	0xFFFFFFFF
SDHI0,1	-	-	-	SDIO_INFO1	SDIO Interrupt Flag Register 1	0x06C	32	read/ write	0x00000000	0xFFFFFFF9
SDHI0,1	-	-	-	SDIO_INFO1_MASK	SDIO_INFO1 Interrupt Mask Register	0x070	32	read/ write	0x0000C007	0xFFFFFFFF
SDHI0,1	-	-	-	SD_DMAEN	DMA Mode Enable Register	0x1B0	32	read/ write	0x00001010	0xFFFFFFFF
SDHI0,1	-	-	-	SOFT_RST	Software Reset Register	0x1C0	32	read/ write	0x00000007	0xFFFFFFFF
SDHI0,1	-	-	-	SDIF_MODE	SD Interface Mode Setting Register	0x1CC	32	read/ write	0x00000000	0xFFFFFFFF
SDHI0,1	-	-	-	EXT_SWAP	Swap Control Register	0x1E0	32	read/ write	0x00000000	0xFFFFFFFF
EDMAC0	-	-	-	EDMR	EDMAC Mode Register	0x00	32	read/ write	0x00000000	0xFFFFFFFF
EDMAC0	-	-	-	TRIMD	Transmit Interrupt Setting Register	0x07C	32	read/ write	0x00000000	0xFFFFFFFF
EDMAC0	-	-	-	EDTRR	EDMAC Transmit Request Register	0x08	32	read/ write	0x00000000	0xFFFFFFFF
EDMAC0	-	-	-	TBRAR	Transmit Buffer Read Address Register	0x0D4	32	read/ write	0x00000000	0xFFFFFFFF
EDMAC0	-	-	-	EDRRR	EDMAC Receive Request Register	0x10	32	read/ write	0x00000000	0xFFFFFFFF
EDMAC0	-	-	-	TDLAR	Transmit Descriptor List Start Address Register	0x18	32	read/ write	0x00000000	0xFFFFFFFF
EDMAC0	-	-	-	RDLAR	Receive Descriptor List Start Address Register	0x20	32	read/ write	0x00000000	0xFFFFFFFF
EDMAC0	-	-	-	EESR	ETHERC/EDMAC Status Register	0x28	32	read/ write	0x00000000	0xFFFFFFFF
EDMAC0	-	-	-	EESIPR	ETHERC/EDMAC Status Interrupt Enable Register	0x30	32	read/ write	0x00000000	0xFFFFFFFF
EDMAC0	-	-	-	TRSCER	ETHERC/EDMAC Transmit/ Receive Status Copy Enable Register	0x38	32	read/ write	0x00000000	0xFFFFFFFF
EDMAC0	-	-	-	RMFCR	Missed-Frame Counter Register	0x40	32	read/ write	0x00000000	0xFFFFFFFF
EDMAC0	-	-	-	TFTR	Transmit FIFO Threshold Register	0x48	32	read/ write	0x00000000	0xFFFFFFFF
EDMAC0	-	-	-	FDR	Transmit FIFO Threshold Register	0x50	32	read/ write	0x00000000	0xFFFFFFFF
EDMAC0	-	-	-	RMCR	Receive Method Control Register	0x58	32	read/ write	0x00000000	0xFFFFFFFF
EDMAC0	-	-	-	TFUCR	Transmit FIFO Underflow Counter	0x64	32	read/ write	0x00000000	0xFFFFFFFF
EDMAC0	-	-	-	RFOCR	Receive FIFO Overflow Counter	0x68	32	read/ write	0x00000000	0xFFFFFFFF
EDMAC0	-	-	-	IOSR	Independent Output Signal Setting Register	0x6C	32	read/ write	0x00000000	0xFFFFFFFF

Table 3.3 寄存器说明（44个中的24个）

周边暗淡	昏暗的增量。	暗淡索引寄存器名称		Description	地址偏移	尺寸访问		重置值	重置蒙版
SDHI0,1	-	-	-	SD_SIZE	传输数据长度 Register	0x04C	32	read/ write	0x00000200	0xFFFFFFFF
SDHI0,1	-	-	-	SD_OPTION	SD卡访问控制 选项寄存器	0x050	32	read/ write	0x000040EE	0xFFFFFFFF
SDHI0,1	-	-	-	SD_ERR_STS1	SD错误状态寄存器1	0x058	32	只读	0x00002000	0xFFFFFFFF
SDHI0,1	-	-	-	SD_ERR_STS2	SD错误状态寄存器2	0x05C	32	只读	0x00000000	0xFFFFFFFF
SDHI0,1	-	-	-	SD_BUF0	标清缓冲寄存器	0x060	32	read/ write	0x00000000	0x00000000
SDHI0,1	-	-	-	SDIO_MODE	SDIO模式控制寄存器0x068		32	read/ write	0x00000000	0xFFFFFFFF
SDHI0,1	-	-	-	SDIO_INFO1	SDIO中断标志 寄存器 1	0x06C	32	read/ write	0x00000000	0xFFFFFFF9
SDHI0,1	-	-	-	SDIO_INFO1_MASK	SDIO_INFO1中断屏蔽 Register	0x070	32	read/ write	0x0000C007	0xFFFFFFFF
SDHI0,1	-	-	-	SD_DMAEN	DMA模式使能寄存器	0x1B0	32	read/ write	0x00001010	0xFFFFFFFF
SDHI0,1	-	-	-	SOFT_RST	软件复位寄存器	0x1C0	32	read/ write	0x00000007	0xFFFFFFFF
SDHI0,1	-	-	-	SDIF_MODE	SD接口模式设置 Register	0x1CC	32	read/ write	0x00000000	0xFFFFFFFF
SDHI0,1	-	-	-	EXT_SWAP	交换控制寄存器	0x1E0	32	read/ write	0x00000000	0xFFFFFFFF
EDMAC0	-	-	-	EDMR	EDMAC模式寄存器	0x00	32	read/ write	0x00000000	0xFFFFFFFF
EDMAC0	-	-	-	TRIMD	发送中断设置 Register	0x07C	32	read/ write	0x00000000	0xFFFFFFFF
EDMAC0	-	-	-	EDTRR	EDMAC传输请求 Register	0x08	32	read/ write	0x00000000	0xFFFFFFFF
EDMAC0	-	-	-	TBRAR	发送缓冲区读取 地址寄存器	0x0D4	32	read/ write	0x00000000	0xFFFFFFFF
EDMAC0	-	-	-	EDRRR	EDMAC接收请求 Register	0x10	32	read/ write	0x00000000	0xFFFFFFFF
EDMAC0	-	-	-	TDLAR	传输描述符列表开始 地址寄存器	0x18	32	read/ write	0x00000000	0xFFFFFFFF
EDMAC0	-	-	-	RDLAR	接收描述符列表开始 地址寄存器	0x20	32	read/ write	0x00000000	0xFFFFFFFF
EDMAC0	-	-	-	EESR	ETHERC/EDMAC Status Register	0x28	32	read/ write	0x00000000	0xFFFFFFFF
EDMAC0	-	-	-	EESIPR	ETHERCEDMAC状态中断 使能寄存器	0x30	32	read/ write	0x00000000	0xFFFFFFFF
EDMAC0	-	-	-	TRSCER	ETHERCEDMAC发送接收状态 复制启用 Register	0x38	32	read/ write	0x00000000	0xFFFFFFFF
EDMAC0	-	-	-	RMFCR	Missed-Frame Counter Register	0x40	32	read/ write	0x00000000	0xFFFFFFFF
EDMAC0	-	-	-	TFTR	发送FIFO阈值 Register	0x48	32	read/ write	0x00000000	0xFFFFFFFF
EDMAC0	-	-	-	FDR	发送FIFO阈值 Register	0x50	32	read/ write	0x00000000	0xFFFFFFFF
EDMAC0	-	-	-	RMCR	接收方法控制 Register	0x58	32	read/ write	0x00000000	0xFFFFFFFF
EDMAC0	-	-	-	TFUCR	Transmit FIFO Underflow Counter	0x64	32	read/ write	0x00000000	0xFFFFFFFF
EDMAC0	-	-	-	RFOCR	接收FIFO溢出 Counter	0x68	32	read/ write	0x00000000	0xFFFFFFFF
EDMAC0	-	-	-	IOSR	独立输出信号 设置寄存器	0x6C	32	read/ write	0x00000000	0xFFFFFFFF

Table 3.3 Register description (25 of 44)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
EDMAC0	-	-	-	FCFTR	Flow Control Start FIFO Threshold Setting Register	0x70	32	read/ write	0x00070007	0xFFFFFFFF
EDMAC0	-	-	-	RPADIR	Receive Data Padding Insert Register	0x78	32	read/ write	0x00000000	0xFFFFFFFF
EDMAC0	-	-	-	RBWAR	Receive Buffer Write Address Register	0xC8	32	read/ write	0x00000000	0xFFFFFFFF
EDMAC0	-	-	-	RDFAR	Receive Descriptor Fetch Address Register	0xCC	32	read/ write	0x00000000	0xFFFFFFFF
EDMAC0	-	-	-	TDFAR	Transmit Descriptor Fetch Address Register	0xD8	32	read-only	0x00000000	0xFFFFFFFF
ETHERC0	-	-	-	ECMR	ETHERC Mode Register	0x00	32	read/ write	0x00000000	0xFFFFFFFF
ETHERC0	-	-	-	RFLR	Receive Frame Maximum Length Register	0x08	32	read/ write	0x00000000	0xFFFFFFFF
ETHERC0	-	-	-	ECSR	ETHERC Status Register	0x10	32	read/ write	0x00000000	0xFFFFFFFF
ETHERC0	-	-	-	ECSIPR	ETHERC Interrupt Enable Register	0x18	32	read/ write	0x00000000	0xFFFFFFFF
ETHERC0	-	-	-	PIR	PHY Interface Register	0x20	32	read/ write	0x00000000	0xFFFFFFF7
ETHERC0	-	-	-	PSR	PHY Status Register	0x28	32	read-only	0x00000000	0xFFFFFFFE
ETHERC0	-	-	-	RDMLR	Random Number Generation Counter Upper Limit Setting Register	0x40	32	read/ write	0x00000000	0xFFFFFFFF
ETHERC0	-	-	-	IPGR	IPG Register	0x50	32	read/ write	0x00000014	0xFFFFFFFF
ETHERC0	-	-	-	APR	Automatic PAUSE Frame Register	0x54	32	read/ write	0x00000000	0xFFFFFFFF
ETHERC0	-	-	-	MPR	Manual PAUSE Frame Register	0x58	32	write-only	0x00000000	0xFFFF0000
ETHERC0	-	-	-	RFCF	Received PAUSE Frame Counter	0x60	32	read-only	0x00000000	0xFFFFFFFF
ETHERC0	-	-	-	TPAUSER	PAUSE Frame Retransmit Count Setting Register	0x64	32	read/ write	0x00000000	0xFFFFFFFF
ETHERC0	-	-	-	TPAUSECR	PAUSE Frame Retransmit Counter	0x68	32	read-only	0x00000000	0xFFFFFFFF
ETHERC0	-	-	-	BCFRR	Broadcast Frame Receive Count Setting Register	0x6C	32	read/ write	0x00000000	0xFFFFFFFF
ETHERC0	-	-	-	MAHR	MAC Address Upper Bit Register	0xC0	32	read/ write	0x00000000	0xFFFFFFFF
ETHERC0	-	-	-	MALR	MAC Address Lower Bit Register	0xC8	32	read/ write	0x00000000	0xFFFFFFFF
ETHERC0	-	-	-	TROCR	Transmit Retry Over Counter Register	0xD0	32	read/ write	0x00000000	0xFFFFFFFF
ETHERC0	-	-	-	CDCR	Late Collision Detect Counter Register	0xD4	32	read/ write	0x00000000	0xFFFFFFFF
ETHERC0	-	-	-	LCCR	Lost Carrier Counter Register	0xD8	32	read/ write	0x00000000	0xFFFFFFFF
ETHERC0	-	-	-	CNDCR	Carrier Not Detect Counter Register	0xDC	32	read/ write	0x00000000	0xFFFFFFFF
ETHERC0	-	-	-	CEFCR	CRC Error Frame Receive Counter Register	0xE4	32	read/ write	0x00000000	0xFFFFFFFF
ETHERC0	-	-	-	FRECR	Frame Receive Error Counter Register	0xE8	32	read/ write	0x00000000	0xFFFFFFFF
ETHERC0	-	-	-	TSFRCR	Too-Short Frame Receive Counter Register	0xEC	32	read/ write	0x00000000	0xFFFFFFFF
ETHERC0	-	-	-	TLFRCR	Too-Long Frame Receive Counter Register	0xF0	32	read/ write	0x00000000	0xFFFFFFFF

Table 3.3 寄存器说明（44个中的25个）

周边暗淡		昏暗的增量。	暗淡索引寄存器名称		Description	地址偏移	尺寸	访问	重置值	重置蒙版
EDMAC0	-	-	-	FCFTR	流控制开始FIFO 阈值设置寄存器	0x70	32	read/ write	0x00070007	0xFFFFFFFF
EDMAC0	-	-	-	RPADIR	接收数据填充插入 Register	0x78	32	read/ write	0x00000000	0xFFFFFFFF
EDMAC0	-	-	-	RBWAR	接收缓冲区写入 地址寄存器	0xC8	32	read/ write	0x00000000	0xFFFFFFFF
EDMAC0	-	-	-	RDFAR	接收描述符获取 地址寄存器	0xCC	32	read/ write	0x00000000	0xFFFFFFFF
EDMAC0	-	-	-	TDFAR	传输描述符获取 地址寄存器	0xD8	32	只读	0x00000000	0xFFFFFFFF
ETHERC0	-	-	-	ECMR	ETHERC模式寄存器	0x00	32	read/ write	0x00000000	0xFFFFFFFF
ETHERC0	-	-	-	RFLR	接收帧最大值 长度寄存器	0x08	32	read/ write	0x00000000	0xFFFFFFFF
ETHERC0	-	-	-	ECSR	ETHERC状态寄存器	0x10	32	read/ write	0x00000000	0xFFFFFFFF
ETHERC0	-	-	-	ECSIPR	ETHERC中断使能 Register	0x18	32	read/ write	0x00000000	0xFFFFFFFF
ETHERC0	-	-	-	PIR	PHY接口寄存器	0x20	32	read/ write	0x00000000	0xFFFFFFF7
ETHERC0	-	-	-	PSR	PHY状态寄存器	0x28	32	只读	0x00000000	0xFFFFFFFE
ETHERC0	-	-	-	RDMLR	随机数生成计数器上限设置 Register	0x40	32	read/ write	0x00000000	0xFFFFFFFF
ETHERC0	-	-	-	IPGR	IPG Register	0x50	32	read/ write	0x00000014	0xFFFFFFFF
ETHERC0	-	-	-	APR	自动暂停帧 Register	0x54	32	read/ write	0x00000000	0xFFFFFFFF
ETHERC0	-	-	-	MPR	手动暂停帧 Register	0x58	32	只写	0x00000000	0xFFFF0000
ETHERC0	-	-	-	RFCF	收到暂停帧 Counter	0x60	32	只读	0x00000000	0xFFFFFFFF
ETHERC0	-	-	-	TPAUSER	暂停帧重传 计数设置寄存器	0x64	32	read/ write	0x00000000	0xFFFFFFFF
ETHERC0	-	-	-	TPAUSECR	暂停帧重传 Counter	0x68	32	只读	0x00000000	0xFFFFFFFF
ETHERC0	-	-	-	BCFRR	广播帧接收 计数设置寄存器	0x6C	32	read/ write	0x00000000	0xFFFFFFFF
ETHERC0	-	-	-	MAHR	MAC地址高位 Register	0xC0	32	read/ write	0x00000000	0xFFFFFFFF
ETHERC0	-	-	-	MALR	MAC地址低位 Register	0xC8	32	read/ write	0x00000000	0xFFFFFFFF
ETHERC0	-	-	-	TROCR	计数器传输重试 Register	0xD0	32	read/ write	0x00000000	0xFFFFFFFF
ETHERC0	-	-	-	CDCR	后期碰撞检测 计数器寄存器	0xD4	32	read/ write	0x00000000	0xFFFFFFFF
ETHERC0	-	-	-	LCCR	遗失承运人柜台 Register	0xD8	32	read/ write	0x00000000	0xFFFFFFFF
ETHERC0	-	-	-	CNDCR	运营商未检测计数器 Register	0xDC	32	read/ write	0x00000000	0xFFFFFFFF
ETHERC0	-	-	-	CEFCR	CRC错误帧接收 计数器寄存器	0xE4	32	read/ write	0x00000000	0xFFFFFFFF
ETHERC0	-	-	-	FRECR	帧接收错误 计数器寄存器	0xE8	32	read/ write	0x00000000	0xFFFFFFFF
ETHERC0	-	-	-	TSFRCR	帧接收过短 计数器寄存器	0xEC	32	read/ write	0x00000000	0xFFFFFFFF
ETHERC0	-	-	-	TLFRCR	帧接收过长 计数器寄存器	0xF0	32	read/ write	0x00000000	0xFFFFFFFF

Table 3.3 Register description (26 of 44)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
ETHERC0	-	-	-	RFCR	Received Alignment Error Frame Counter Register	0xF4	32	read/ write	0x00000000	0xFFFFFFFF
ETHERC0	-	-	-	MAFCR	Multicast Address Frame Receive Counter Register	0xF8	32	read/ write	0x00000000	0xFFFFFFFF
PTPEDMAC	-	-	-	EDMR	PTPEDMAC Mode Register	0x000	32	read/ write	0x00000000	0xFFFFFFFF
PTPEDMAC	-	-	-	EDTRR	EDMAC Transmit Request Register	0x008	32	read/ write	0x00000000	0xFFFFFFFF
PTPEDMAC	-	-	-	EDRRR	EDMAC Receive Request Register	0x010	32	read/ write	0x00000000	0xFFFFFFFF
PTPEDMAC	-	-	-	TDLAR	Transmit Descriptor List Start Address Register	0x018	32	read/ write	0x00000000	0xFFFFFFFF
PTPEDMAC	-	-	-	RDLAR	Receive Descriptor List Start Address Register	0x020	32	read/ write	0x00000000	0xFFFFFFFF
PTPEDMAC	-	-	-	EESR	PTP/EDMAC Status Register	0x028	32	read/ write	0x00000000	0xFFFFFFFF
PTPEDMAC	-	-	-	EESIPR	PTP/EDMAC Status Interrupt Enable Register	0x030	32	read/ write	0x00000000	0xFFFFFFFF
PTPEDMAC	-	-	-	RMFCR	Missed-Frame Counter Register	0x040	32	read/ write	0x00000000	0xFFFFFFFF
PTPEDMAC	-	-	-	TFTR	Transmit FIFO Threshold Register	0x048	32	read/ write	0x00000000	0xFFFFFFFF
PTPEDMAC	-	-	-	FDR	Transmit FIFO Threshold Register	0x050	32	read/ write	0x00000000	0xFFFFFFFF
PTPEDMAC	-	-	-	RMCR	Receive Method Control Register	0x058	32	read/ write	0x00000000	0xFFFFFFFF
PTPEDMAC	-	-	-	TFUCR	Transmit FIFO Underflow Counter	0x064	32	read/ write	0x00000000	0xFFFFFFFF
PTPEDMAC	-	-	-	RFOCR	Receive FIFO Overflow Counter	0x068	32	read/ write	0x00000000	0xFFFFFFFF
PTPEDMAC	-	-	-	IOSR	Independent Output Signal Setting Register	0x06C	32	read/ write	0x00000000	0xFFFFFFFF
PTPEDMAC	-	-	-	FCFTR	Flow Control Start FIFO Threshold Setting Register	0x070	32	read/ write	0x00070007	0xFFFFFFFF
PTPEDMAC	-	-	-	RPADIR	Receive Data Padding Insert Register	0x078	32	read/ write	0x00000000	0xFFFFFFFF
PTPEDMAC	-	-	-	TRIMD	Transmit Interrupt Setting Register	0x07C	32	read/ write	0x00000000	0xFFFFFFFF
PTPEDMAC	-	-	-	RBWAR	Receive Buffer Write Address Register	0x0C8	32	read/ write	0x00000000	0xFFFFFFFF
PTPEDMAC	-	-	-	RDFAR	Receive Descriptor Fetch Address Register	0x0CC	32	read/ write	0x00000000	0xFFFFFFFF
PTPEDMAC	-	-	-	TBRAR	Transmit Buffer Read Address Register	0x0D4	32	read/ write	0x00000000	0xFFFFFFFF
PTPEDMAC	-	-	-	TDFAR	Transmit Descriptor Fetch Address Register	0x0D8	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC_CFG	-	-	-	PTRSTR	EPTPC Reset Register	0x00	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC_CFG	-	-	-	STCSELR	STCA Clock Select Register	0x04	32	read/ write	0x00000006	0xFFFFFFFF
EPTPC_CFG	-	-	-	BYPASS	Bypass 1588 module Register	0x08	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC	-	-	-	MIESR	MINT Interrupt Source Status Register	0x000	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC	-	-	-	MIEIPR	MINT Interrupt Request Permission Register	0x004	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC	-	-	-	ELIPPR	ELC Output/IPLS Interrupt Request Permission Register	0x010	32	read/ write	0x00003F3F	0xFFFFFFFF

Table 3.3 寄存器说明（44个中的26个）

周边暗淡	昏暗的增量。	暗淡索引寄存器名称		Description	地址偏移	尺寸	访问	重置值	重置蒙版
ETHERC0	-	-	RFCR	收到对齐错误帧计数器寄存器	0xF4	32	read/ write	0x00000000	0xFFFFFFFF
ETHERC0	-	-	MAFCR	多播地址帧接收计数器寄存器	0xF8	32	read/ write	0x00000000	0xFFFFFFFF
PTPEDMAC	-	-	EDMR	PTPEDMAC模式寄存器	0x000	32	read/ write	0x00000000	0xFFFFFFFF
PTPEDMAC	-	-	EDTRR	EDMAC传输请求 Register	0x008	32	read/ write	0x00000000	0xFFFFFFFF
PTPEDMAC	-	-	EDRRR	EDMAC接收请求 Register	0x010	32	read/ write	0x00000000	0xFFFFFFFF
PTPEDMAC	-	-	TDLAR	传输描述符列表开始地址寄存器	0x018	32	read/ write	0x00000000	0xFFFFFFFF
PTPEDMAC	-	-	RDLAR	接收描述符列表开始地址寄存器	0x020	32	read/ write	0x00000000	0xFFFFFFFF
PTPEDMAC	-	-	EESR	PTPEDMAC状态寄存器0x	028	32	read/ write	0x00000000	0xFFFFFFFF
PTPEDMAC	-	-	EESIPR	PTPEDMAC状态中断启用注册	0x030	32	read/ write	0x00000000	0xFFFFFFFF
PTPEDMAC	-	-	RMFCR	Missed-Frame Counter Register	0x040	32	read/ write	0x00000000	0xFFFFFFFF
PTPEDMAC	-	-	TFTR	发送FIFO阈值 Register	0x048	32	read/ write	0x00000000	0xFFFFFFFF
PTPEDMAC	-	-	FDR	发送FIFO阈值 Register	0x050	32	read/ write	0x00000000	0xFFFFFFFF
PTPEDMAC	-	-	RMCR	接收方法控制 Register	0x058	32	read/ write	0x00000000	0xFFFFFFFF
PTPEDMAC	-	-	TFUCR	Transmit FIFO Underflow Counter	0x064	32	read/ write	0x00000000	0xFFFFFFFF
PTPEDMAC	-	-	RFOCR	接收FIFO溢出 Counter	0x068	32	read/ write	0x00000000	0xFFFFFFFF
PTPEDMAC	-	-	IOSR	独立输出信号设置寄存器	0x06C	32	read/ write	0x00000000	0xFFFFFFFF
PTPEDMAC	-	-	FCFTR	流控制开始FIFO阈值设置寄存器	0x070	32	read/ write	0x00070007	0xFFFFFFFF
PTPEDMAC	-	-	RPADIR	接收数据填充插入 Register	0x078	32	read/ write	0x00000000	0xFFFFFFFF
PTPEDMAC	-	-	TRIMD	发送中断设置 Register	0x07C	32	read/ write	0x00000000	0xFFFFFFFF
PTPEDMAC	-	-	RBWAR	接收缓冲区写入地址寄存器	0x0C8	32	read/ write	0x00000000	0xFFFFFFFF
PTPEDMAC	-	-	RDFAR	接收描述符获取地址寄存器	0x0CC	32	read/ write	0x00000000	0xFFFFFFFF
PTPEDMAC	-	-	TBRAR	发送缓冲区读取地址寄存器	0x0D4	32	read/ write	0x00000000	0xFFFFFFFF
PTPEDMAC	-	-	TDFAR	传输描述符获取地址寄存器	0x0D8	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC_CFG	-	-	PTRSTR	EPTPC复位寄存器	0x00	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC_CFG	-	-	STCSELR	STCA时钟选择寄存器	0x04	32	read/ write	0x00000006	0xFFFFFFFF
EPTPC_CFG	-	-	BYPASS	绕过1588模块 Register	0x08	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC	-	-	MIESR	MINT中断源状态 Register	0x000	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC	-	-	MIEIPR	MINT中断请求许可登记	0x004	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC	-	-	ELIPPR	ELC Output/IPLS Interrupt 请求许可 Register	0x010	32	read/ write	0x00003F3F	0xFFFFFFFF

Table 3.3 Register description (27 of 44)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
EPTPC	-	-	-	ELIPACR	ELC Output/IPLS Interrupt Permission Automatic Clearing Register	0x014	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC	-	-	-	STSR	STCA Status Register	0x040	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC	-	-	-	STIPR	STCA Status Notification Permission Register	0x044	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC	-	-	-	STCFR	STCA Clock Frequency Setting Register	0x050	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC	-	-	-	STMR	STCA Operating Mode Register	0x054	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC	-	-	-	SYNTOR	Sync Message Reception Timeout Register	0x058	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC	-	-	-	IPTSELR	IPLS Interrupt Request Timer Select Register	0x060	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC	-	-	-	MITSELR	MINT Interrupt Request Timer Select Register	0x064	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC	-	-	-	ELTSELR	ELC Output Timer Select Register	0x068	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC	-	-	-	STCHSELR	Time Synchronization Channel Select Register	0x06C	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC	-	-	-	SYNSTARTR	Slave Time Synchronization Start Register	0x080	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC	-	-	-	LCIVLDR	Local Time Counter Initial Value Load Directive Register	0x084	32	write-only	0x00000000	0xFFFFFFFF
EPTPC	-	-	-	SYNTDARU	Synchronization Loss Detection Threshold Registers	0x090	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC	-	-	-	SYNTDARL	Synchronization Loss Detection Threshold Registers	0x094	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC	-	-	-	SYNTDBRU	Synchronization Detection Threshold Registers	0x098	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC	-	-	-	SYNTDBRL	Synchronization Detection Threshold Registers	0x09C	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC	-	-	-	LCIVRU	Local Time Counter Initial Value Registers	0x0B0	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC	-	-	-	LCIVRM	Local Time Counter Initial Value Registers	0x0B4	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC	-	-	-	LCIVRL	Local Time Counter Initial Value Registers	0x0B8	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC	-	-	-	GETW10R	Worst 10 Acquisition Directive Register	0x124	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC	-	-	-	PLIMITRU	Positive Gradient Limit Registers	0x128	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC	-	-	-	PLIMITRM	Positive Gradient Limit Registers	0x12C	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC	-	-	-	PLIMITRL	Positive Gradient Limit Registers	0x130	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC	-	-	-	MLIMITRU	Negative Gradient Limit Registers	0x134	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC	-	-	-	MLIMITRM	Negative Gradient Limit Registers	0x138	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC	-	-	-	MLIMITRL	Negative Gradient Limit Registers	0x13C	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC	-	-	-	GETINFOR	Statistical Information Retention Control Register	0x140	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC	-	-	-	LCCVRU	Local Time Counters	0x170	32	read-only	0x00000000	0xFFFFFFFF

Table 3.3 寄存器描述（44中的27）

周边暗淡		昏暗的增量。	暗淡索引寄存器名称		Description	地址偏移	尺寸	访问	重置值	重置蒙版
EPTPC	-	-	-	ELIPACR	ELC Output/IPLS Interrupt 权限自动 清算登记	0x014	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC	-	-	-	STSR	STCA状态寄存器	0x040	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC	-	-	-	STIPR	STCA状态通知 许可登记	0x044	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC	-	-	-	STCFR	STCA时钟频率 设置寄存器	0x050	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC	-	-	-	STMR	STCA操作模式 Register	0x054	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC	-	-	-	SYNTOR	同步消息接收 超时寄存器	0x058	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC	-	-	-	IPTSELR	IPLS中断请求 定时器选择寄存器	0x060	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC	-	-	-	MITSELR	MINT中断请求 定时器选择寄存器	0x064	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC	-	-	-	ELTSELR	ELC输出定时器选择 Register	0x068	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC	-	-	-	STCHSELR	时间同步 通道选择寄存器	0x06C	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC	-	-	-	SYNSTARTR	从机时间同步 开始注册	0x080	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC	-	-	-	LCIVLDR	本地时间计数器初始值 价值加载指令 Register	0x084	32	只写	0x00000000	0xFFFFFFFF
EPTPC	-	-	-	SYNTDARU	同步丢失检测阈值 Registers	0x090	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC	-	-	-	SYNTDARL	同步丢失检测阈值 Registers	0x094	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC	-	-	-	SYNTDBRU	同步检测 阈值寄存器	0x098	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC	-	-	-	SYNTDBRL	同步检测 阈值寄存器	0x09C	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC	-	-	-	LCIVRU	本地时间计数器初始值 值寄存器	0x0B0	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC	-	-	-	LCIVRM	本地时间计数器初始值 值寄存器	0x0B4	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC	-	-	-	LCIVRL	本地时间计数器初始值 值寄存器	0x0B8	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC	-	-	-	GETW10R	最差10次收购 指令寄存器	0x124	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC	-	-	-	PLIMITRU	正梯度限制 Registers	0x128	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC	-	-	-	PLIMITRM	正梯度限制 Registers	0x12C	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC	-	-	-	PLIMITRL	正梯度限制 Registers	0x130	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC	-	-	-	MLIMITRU	负梯度限制 Registers	0x134	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC	-	-	-	MLIMITRM	负梯度限制 Registers	0x138	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC	-	-	-	MLIMITRL	负梯度限制 Registers	0x13C	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC	-	-	-	GETINFOR	统计资料 保留控制寄存器	0x140	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC	-	-	-	LCCVRU	本地时间计数器	0x170	32	只读	0x00000000	0xFFFFFFFF

Table 3.3 Register description (28 of 44)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
EPTPC	-	-	-	LCCVRM	Local Time Counters	0x174	32	read-only	0x00000000	0xFFFFFFFF
EPTPC	-	-	-	LCCVRL	Local Time Counters	0x178	32	read-only	0x00000000	0xFFFFFFFF
EPTPC	-	-	-	PW10VRU	Positive Gradient Worst 10 Value Registers	0x210	32	read-only	0x00000000	0xFFFFFFFF
EPTPC	-	-	-	PW10VRM	Positive Gradient Worst 10 Value Registers	0x214	32	read-only	0x00000000	0xFFFFFFFF
EPTPC	-	-	-	PW10VRL	Positive Gradient Worst 10 Value Registers	0x218	32	read-only	0x00000000	0xFFFFFFFF
EPTPC	-	-	-	MW10RU	Negative Gradient Worst 10 Value Registers	0x2D0	32	read-only	0x00000000	0xFFFFFFFF
EPTPC	-	-	-	MW10RM	Negative Gradient Worst 10 Value Registers	0x2D4	32	read-only	0x00000000	0xFFFFFFFF
EPTPC	-	-	-	MW10RL	Negative Gradient Worst 10 Value Registers	0x2D8	32	read-only	0x00000000	0xFFFFFFFF
EPTPC	6	0x10	0-5	TMSTTRU%s	Timer Start Time Setting Register %s	0x300	32	read/write	0x00000000	0xFFFFFFFF
EPTPC	6	0x10	0-5	TMSTTRL%s	Timer Start Time Setting Register %s	0x304	32	read/write	0x00000000	0xFFFFFFFF
EPTPC	6	0x10	0-5	TMCYCR%s	Timer Cycle Setting Registers %s	0x308	32	read/write	0x00000000	0xFFFFFFFF
EPTPC	6	0x10	0-5	TMPLSR%s	Timer Pulse Width Setting Register %s	0x30C	32	read/write	0x00000000	0xFFFFFFFF
EPTPC	-	-	-	TMSTARTR	Timer Start Register	0x37C	32	read/write	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	SYSR	SYNFP Status Register	0x000	32	read/write	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	SYIPR	SYNFP Status Notification Permission Register	0x004	32	read/write	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	SYMACRU	SYNFP MAC Address Registers	0x010	32	read/write	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	SYMACRL	SYNFP MAC Address Registers	0x014	32	read/write	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	SYLLCCTLR	SYNFP LLC-CTL Value Register	0x018	32	read/write	0x00000003	0xFFFFFFFF
EPTPC0	-	-	-	SYIPADDRR	SYNFP Local IP Address Register	0x01C	32	read/write	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	SYSPVRR	SYNFP Specification Version Setting Register	0x040	32	read/write	0x00000002	0xFFFFFFFF
EPTPC0	-	-	-	SYDOMR	SYNFP Domain Number Setting Register	0x044	32	read/write	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	ANFR	Announce Message Flag Field Setting Register	0x050	32	read/write	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	SYNFR	Sync Message Flag Field Setting Register	0x054	32	read/write	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	DYRQFR	Delay_Req Message Flag Field Setting Register	0x058	32	read/write	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	DYRPFR	Delay_Resp Message Flag Field Setting Register	0x05C	32	read/write	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	SYCIDRU	SYNFP Local Clock ID Registers	0x060	32	read/write	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	SYCIDRL	SYNFP Local Clock ID Registers	0x064	32	read/write	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	SYPNUMR	SYNFP Local Port Number Register	0x068	32	read/write	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	SYRVLDR	SYNFP Register Value Load Directive Register	0x080	32	write-only	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	SYRFL1R	SYNFP Reception Filter Register 1	0x090	32	read/write	0x00000000	0xFFFFFFFF

Table 3.3 寄存器说明（44个中的28个）

周边暗淡		昏暗的增量。	暗淡索引寄存器名称		Description	地址偏移	尺寸	访问	重置值	重置蒙版
EPTPC	-	-	-	LCCVRM	本地时间计数器	0x174	32	只读	0x00000000	0xFFFFFFFF
EPTPC	-	-	-	LCCVRL	本地时间计数器	0x178	32	只读	0x00000000	0xFFFFFFFF
EPTPC	-	-	-	PW10VRU	正梯度最差10值寄存器	0x210	32	只读	0x00000000	0xFFFFFFFF
EPTPC	-	-	-	PW10VRM	正梯度最差10值寄存器	0x214	32	只读	0x00000000	0xFFFFFFFF
EPTPC	-	-	-	PW10VRL	正梯度最差10值寄存器	0x218	32	只读	0x00000000	0xFFFFFFFF
EPTPC	-	-	-	MW10RU	负梯度最差10值寄存器	0x2D0	32	只读	0x00000000	0xFFFFFFFF
EPTPC	-	-	-	MW10RM	负梯度最差10值寄存器	0x2D4	32	只读	0x00000000	0xFFFFFFFF
EPTPC	-	-	-	MW10RL	负梯度最差10值寄存器	0x2D8	32	只读	0x00000000	0xFFFFFFFF
EPTPC	6	0x10	0-5	TMSTTRU%s	定时器开始时间设置Register %s	0x300	32	read/write	0x00000000	0xFFFFFFFF
EPTPC	6	0x10	0-5	TMSTTRL%s	定时器开始时间设置Register %s	0x304	32	read/write	0x00000000	0xFFFFFFFF
EPTPC	6	0x10	0-5	TMCYCR%s	定时器周期设置Registers %s	0x308	32	read/write	0x00000000	0xFFFFFFFF
EPTPC	6	0x10	0-5	TMPLSR%s	定时器脉冲宽度设置Register %s	0x30C	32	read/write	0x00000000	0xFFFFFFFF
EPTPC	-	-	-	TMSTARTR	定时器启动寄存器	0x37C	32	read/write	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	SYSR	SYNFP状态寄存器	0x000	32	read/write	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	SYIPR	SYNFP状态通知许可登记	0x004	32	read/write	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	SYMACRU	SYNFPMAC地址Registers	0x010	32	read/write	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	SYMACRL	SYNFPMAC地址Registers	0x014	32	read/write	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	SYLLCCTLR	SYNFP LLC-CTL ValueRegister	0x018	32	read/write	0x00000003	0xFFFFFFFF
EPTPC0	-	-	-	SYIPADDRR	SYNFP本地IP地址Register	0x01C	32	read/write	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	SYSPVRR	SYNFP规范版本设置寄存器	0x040	32	read/write	0x00000002	0xFFFFFFFF
EPTPC0	-	-	-	SYDOMR	SYNFP域号设置寄存器	0x044	32	read/write	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	ANFR	宣布消息标志字段设置寄存器	0x050	32	read/write	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	SYNFR	同步消息标志字段设置寄存器	0x054	32	read/write	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	DYRQFR	Delay_Req消息标志字段设置寄存器	0x058	32	read/write	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	DYRPFR	Delay_Resp消息标志字段设置寄存器	0x05C	32	read/write	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	SYCIDRU	SYNFP本地时钟IDRegisters	0x060	32	read/write	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	SYCIDRL	SYNFP本地时钟IDRegisters	0x064	32	read/write	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	SYPNUMR	SYNFP本地端口号Register	0x068	32	read/write	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	SYRVLDR	SYNFP寄存器值加载指令寄存器	0x080	32	只写	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	SYRFL1R	SYNFP接收过滤器Register 1	0x090	32	read/write	0x00000000	0xFFFFFFFF

Table 3.3 Register description (29 of 44)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
EPTPC0	-	-	-	SYRFL2R	SYNFP Reception Filter Register 2	0x094	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	SYTRENR	SYNFP Transmission Enable Register	0x098	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	MTCIDU	Master Clock ID Registers	0x0A0	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	MTCIDL	Master Clock ID Registers	0x0A4	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	MTPID	Master clock port number register	0x0A8	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	SYTLIR	SYNFP Transmission Interval Setting Register	0x0C0	32	read/ write	0x00000001	0xFFFFFFFF
EPTPC0	-	-	-	SYRLIR	SYNFP Received logMessageInterval Value Indication Register	0x0C4	32	read-only	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	OFMRU	offsetFromMaster Value Register	0x0C8	32	read-only	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	OFMRL	offsetFromMaster Value Register	0x0CC	32	read-only	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	MPDRU	meanPathDelay Value Register	0x0D0	32	read-only	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	MPDRL	meanPathDelay Value Register	0x0D4	32	read-only	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	GMPR	grandmasterPriority Field Setting Register	0x0E0	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	GMCQR	grandmasterClockQuality Field Setting Register	0x0E4	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	GMIDRU	grandmasterIdentity Field Setting Register	0x0E8	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	GMIDRL	grandmasterIdentity Field Setting Register	0x0EC	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	CUOTSR	currentUtcOffset/timeSource Field Setting Register	0x0F0	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	SRR	stepsRemoved Field Setting Register	0x0F4	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	PPMACRU	PTP-primary Message Destination MAC Address Setting Register	0x100	32	read/ write	0x00011B19	0xFFFFFFFF
EPTPC0	-	-	-	PPMACRL	PTP-primary Message Destination MAC Address Setting Register	0x104	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	PDMACRU	PTP-pdelay Message MAC Address Setting Register	0x108	32	read/ write	0x000180C2	0xFFFFFFFF
EPTPC0	-	-	-	PDMACRL	PTP-pdelay Message MAC Address Setting Register	0x10C	32	read/ write	0x0000000E	0xFFFFFFFF
EPTPC0	-	-	-	PETYPER	PTP Message EtherType Setting Register	0x110	32	read/ write	0x000088F7	0xFFFFFFFF
EPTPC0	-	-	-	PPIPR	PTP-primary Message Destination IP Address Setting Register	0x120	32	read/ write	0xE0000181	0xFFFFFFFF
EPTPC0	-	-	-	PDIPR	PTP-pdelay Message Destination IP Address Setting Register	0x124	32	read/ write	0xE000006B	0xFFFFFFFF
EPTPC0	-	-	-	PETOSR	PTP Event Message TOS Setting Register	0x128	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	PGTOSR	PTP general Message TOS Setting Register	0x12C	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	PPTTLR	PTP-primary Message TTL Setting Register	0x130	32	read/ write	0x00000080	0xFFFFFFFF

Table 3.3 寄存器说明（44中的29）

周边暗淡		昏暗的增量。	暗淡索引寄存器名称		Description	地址偏移	尺寸	访问	重置值	重置蒙版
EPTPC0	-	-	-	SYRFL2R	SYNFP接收过滤器 Register 2	0x094	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	SYTRENR	SYNFP传输启用 Register	0x098	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	MTCIDU	主时钟ID寄存器	0x0A0	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	MTCIDL	主时钟ID寄存器	0x0A4	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	MTPID	主时钟端口号寄存器	0x0A8	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	SYTLIR	SYNFP Transmission 间隔设置寄存器	0x0C0	32	read/ write	0x00000001	0xFFFFFFFF
EPTPC0	-	-	-	SYRLIR	SYNFP接收到的logMessageInterval值指示寄存器	0x0C4	32	只读	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	OFMRU	offsetFromMaster值寄存器	0x0C8	32	只读	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	OFMRL	offsetFromMaster值寄存器	0x0CC	32	只读	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	MPDRU	meanPathDelay值寄存器	0x0D0	32	只读	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	MPDRL	meanPathDelay值寄存器	0x0D4	32	只读	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	GMPR	grandmasterPriority字段设置寄存器	0x0E0	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	GMCQR	grandmasterClockQuality字段设置寄存器	0x0E4	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	GMIDRU	grandmasterIdentity字段设置寄存器	0x0E8	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	GMIDRL	grandmasterIdentity字段设置寄存器	0x0EC	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	CUOTSR	currentUtcOffsettimeSource字段设置寄存器	0x0F0	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	SRR	stepsRemoved字段设置寄存器	0x0F4	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	PPMACRU	PTP-primary Message 目标MAC地址 设置寄存器	0x100	32	read/ write	0x00011B19	0xFFFFFFFF
EPTPC0	-	-	-	PPMACRL	PTP-primary Message 目标MAC地址 设置寄存器	0x104	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	PDMACRU	PTP-pdelay消息MAC 地址设置寄存器	0x108	32	read/ write	0x000180C2	0xFFFFFFFF
EPTPC0	-	-	-	PDMACRL	PTP-pdelay消息MAC 地址设置寄存器	0x10C	32	read/ write	0x0000000E	0xFFFFFFFF
EPTPC0	-	-	-	PETYPER	PTP Message EtherType 设置寄存器	0x110	32	read/ write	0x000088F7	0xFFFFFFFF
EPTPC0	-	-	-	PPIPR	PTP-primaryMessageDestinationIPAddress 设置寄存器	0x120	32	read/ write	0xE0000181	0xFFFFFFFF
EPTPC0	-	-	-	PDIPR	PTP-pdelay消息目标IP 地址 设置寄存器	0x124	32	read/ write	0xE000006B	0xFFFFFFFF
EPTPC0	-	-	-	PETOSR	PTP事件消息服务条款 设置寄存器	0x128	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	PGTOSR	PTP通用消息服务条款 设置寄存器	0x12C	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	PPTTLR	PTP-primary Message TTL 设置寄存器	0x130	32	read/ write	0x00000080	0xFFFFFFFF

Table 3.3 Register description (30 of 44)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
EPTPC0	-	-	-	PDTTLR	PTP-pdelay Message TTL Setting Register	0x134	32	read/ write	0x00000001	0xFFFFFFFF
EPTPC0	-	-	-	PEUDPR	PTP Event Message UDP Destination Port Number Setting Register	0x138	32	read/ write	0x0000013F	0xFFFFFFFF
EPTPC0	-	-	-	PGUDPR	PTP general Message UDP Destination Port Number Setting Register	0x13C	32	read/ write	0x00000140	0xFFFFFFFF
EPTPC0	-	-	-	FFLTR	Frame Reception Filter Setting Register	0x140	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC0	2	0x8	0-1	FMAC%sRU	Frame Reception Filter MAC Address %s Setting Registers	0x160	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC0	2	0x8	0-1	FMAC%sRL	Frame Reception Filter MAC Address %s Setting Registers	0x164	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	DASYMRU	Asymmetric Delay Setting Registers	0x1C0	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	DASYMRL	Asymmetric Delay Setting Registers	0x1C4	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	TSLATR	Timestamp Latency Setting Register	0x1C8	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	SYCONFR	SYNFP Operation Setting Register	0x1CC	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	SYFORMR	SYNFP Frame Format Setting Register	0x1D0	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	RSTOUTR	Response Message Reception Timeout Register	0x1D4	32	read/ write	0x00000000	0xFFFFFFFF
SCI0-9	-	-	-	SMR	Serial Mode Register (SCMR.SMIF = 0)	0x00	8	read/ write	0x00	0xFF
SCI0-9	-	-	-	SMR_SMCI	Serial mode register (SCMR.SMIF = 1)	0x00	8	read/ write	0x00	0xFF
SCI0-9	-	-	-	BRR	Bit Rate Register	0x01	8	read/ write	0x00	0xFF
SCI0-9	-	-	-	SCR	Serial Control Register (SCMR.SMIF = 0)	0x02	8	read/ write	0x00	0xFF
SCI0-9	-	-	-	SCR_SMCI	Serial Control Register (SCMR.SMIF =1)	0x02	8	read/ write	0x00	0xFF
SCI0-9	-	-	-	TDR	Transmit Data Register	0x03	8	read/ write	0xFF	0xFF
SCI0-9	-	-	-	SSR	Serial Status Register(SCMR.SMIF = 0 and FCR.FM=0)	0x04	8	read/ write	0x84	0xFF
SCI0-9	-	-	-	SSR_FIFO	Serial Status Register(SCMR.SMIF = 0 and FCR.FM=1)	0x04	8	read/ write	0x80	0xFF
SCI0-9	-	-	-	SSR_SMCI	Serial Status Register(SCMR.SMIF = 1)	0x04	8	read/ write	0x84	0xFF
SCI0-9	-	-	-	RDR	Receive Data Register	0x05	8	read-only	0x00	0xFF
SCI0-9	-	-	-	SCMR	Smart Card Mode Register	0x06	8	read/ write	0xF2	0xFF
SCI0-9	-	-	-	SEMR	Serial Extended Mode Register	0x07	8	read/ write	0x00	0xFF
SCI0-9	-	-	-	SNFR	Noise Filter Setting Register	0x08	8	read/ write	0x00	0xFF
SCI0-9	-	-	-	SIMR1	I2C Mode Register 1	0x09	8	read/ write	0x00	0xFF
SCI0-9	-	-	-	SIMR2	I2C Mode Register 2	0x0A	8	read/ write	0x00	0xFF

Table 3.3 寄存器说明（44中的30）

周边暗淡		昏暗的增量。	暗淡索引寄存器名称		Description	地址偏移	尺寸	访问	重置值	重置蒙版
EPTPC0	-	-	-	PDTTLR	PTP-pdelay Message TTL 设置寄存器	0x134	32	read/ write	0x00000001	0xFFFFFFFF
EPTPC0	-	-	-	PEUDPR	PTP事件消息UDP目标端口号 设置寄存器	0x138	32	read/ write	0x0000013F	0xFFFFFFFF
EPTPC0	-	-	-	PGUDPR	PTP通用消息UDP 目的端口号 设置寄存器	0x13C	32	read/ write	0x00000140	0xFFFFFFFF
EPTPC0	-	-	-	FFLTR	帧接收滤波器 设置寄存器	0x140	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC0	2	0x8	0-1	FMAC%sRU	帧接收过滤器MAC 地址%s设置 Registers	0x160	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC0	2	0x8	0-1	FMAC%sRL	帧接收过滤器MAC 地址%s设置 Registers	0x164	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	DASYMRU	非对称延迟设置 Registers	0x1C0	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	DASYMRL	非对称延迟设置 Registers	0x1C4	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	TSLATR	时间戳延迟设置 Register	0x1C8	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	SYCONFR	SYNFP操作设置 Register	0x1CC	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	SYFORMR	SYNFP帧格式 设置寄存器	0x1D0	32	read/ write	0x00000000	0xFFFFFFFF
EPTPC0	-	-	-	RSTOUTR	响应消息 接收超时寄存器	0x1D4	32	read/ write	0x00000000	0xFFFFFFFF
SCI0-9	-	-	-	SMR	串行模式寄存器(SCMR.SMIF=0)	0x00	8	read/ write	0x00	0xFF
SCI0-9	-	-	-	SMR_SMCI	串行模式寄存器(SCMR.SMIF=1)	0x00	8	read/ write	0x00	0xFF
SCI0-9	-	-	-	BRR	比特率寄存器	0x01	8	read/ write	0x00	0xFF
SCI0-9	-	-	-	SCR	串行控制寄存器(SCMR.SMIF=0)	0x02	8	read/ write	0x00	0xFF
SCI0-9	-	-	-	SCR_SMCI	串行控制寄存器(SCMR.SMIF=1)	0x02	8	read/ write	0x00	0xFF
SCI0-9	-	-	-	TDR	发送数据寄存器	0x03	8	read/ write	0xFF	0xFF
SCI0-9	-	-	-	SSR	序列状态 Register(SCMR.SMIF = 0 and FCR.FM=0)	0x04	8	read/ write	0x84	0xFF
SCI0-9	-	-	-	SSR_FIFO	序列状态 Register(SCMR.SMIF = 0 and FCR.FM=1)	0x04	8	read/ write	0x80	0xFF
SCI0-9	-	-	-	SSR_SMCI	序列状态 Register(SCMR.SMIF = 1)	0x04	8	read/ write	0x84	0xFF
SCI0-9	-	-	-	RDR	接收数据寄存器	0x05	8	只读	0x00	0xFF
SCI0-9	-	-	-	SCMR	智能卡模式寄存器	0x06	8	read/ write	0xF2	0xFF
SCI0-9	-	-	-	SEMR	串行扩展模式 Register	0x07	8	read/ write	0x00	0xFF
SCI0-9	-	-	-	SNFR	噪声滤波器设置寄存器	0x08	8	read/ write	0x00	0xFF
SCI0-9	-	-	-	SIMR1	I2C模式寄存器1	0x09	8	read/ write	0x00	0xFF
SCI0-9	-	-	-	SIMR2	I2C模式寄存器2	0x0A	8	read/ write	0x00	0xFF

Table 3.3 Register description (31 of 44)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
SCI0-9	-	-	-	SIMR3	I2C Mode Register 3	0x0B	8	read/ write	0x00	0xFF
SCI0-9	-	-	-	SISR	I2C Status Register	0x0C	8	read-only	0x00	0xCB
SCI0-9	-	-	-	SPMR	SPI Mode Register	0x0D	8	read/ write	0x00	0xFF
SCI0-9	-	-	-	TDRHL	Transmit 9-bit Data Register	0x0E	16	read/ write	0xFFFF	0xFFFF
SCI0-9	-	-	-	FTDRHL	Transmit FIFO Data Register HL	0x0E	16	write-only	0xFFFF	0xFFFF
SCI0-9	-	-	-	FTDRH	Transmit FIFO Data Register H	0x0E	8	write-only	0xFF	0xFF
SCI0-9	-	-	-	FTDRL	Transmit FIFO Data Register L	0x0F	8	write-only	0xFF	0xFF
SCI0-9	-	-	-	RDRHL	Receive 9-bit Data Register	0x10	16	read-only	0x0000	0xFFFF
SCI0-9	-	-	-	FRDRHL	Receive FIFO Data Register HL	0x10	16	read-only	0x0000	0xFFFF
SCI0-9	-	-	-	FRDRH	Receive FIFO Data Register H	0x10	8	read-only	0x00	0xFF
SCI0-9	-	-	-	FRDRL	Receive FIFO Data Register L	0x11	8	read-only	0x00	0xFF
SCI0-9	-	-	-	MDDR	Modulation Duty Register	0x12	8	read/ write	0xFF	0xFF
SCI0-9	-	-	-	DCCR	Data Compare Match Control Register	0x13	8	read/ write	0x40	0xFF
SCI0-9	-	-	-	FCR	FIFO Control Register	0x14	16	read/ write	0xF800	0xFFFF
SCI0-9	-	-	-	FDR	FIFO Data Count Register	0x16	16	read-only	0x0000	0xFFFF
SCI0-9	-	-	-	LSR	Line Status Register	0x18	16	read-only	0x0000	0xFFFF
SCI0-9	-	-	-	CDR	Compare Match Data Register	0x1A	16	read/ write	0x0000	0xFFFF
SCI0-9	-	-	-	SPTR	Serial Port Register	0x1C	8	read/ write	0x03	0xFF
IRDA	-	-	-	IRCR	IrDA Control Register	0x00	8	read/ write	0x00	0xFF
SPI0,1	-	-	-	SPCR	SPI Control Register	0x00	8	read/ write	0x00	0xFF
SPI0,1	-	-	-	SSLP	SPI Slave Select Polarity Register	0x01	8	read/ write	0x00	0xFF
SPI0,1	-	-	-	SPPCR	RSPI Pin Control Register	0x02	8	read/ write	0x00	0xFF
SPI0,1	-	-	-	SPSR	SPI Status Register	0x03	8	read/ write	0x20	0xFF
SPI0,1	-	-	-	SPDR	SPI Data Register	0x04	32	read/ write	0x00000000	0xFFFFFFFF
SPI0,1	-	-	-	SPDR_HA	SPI Data Register (halfword access)	0x04	16	read/ write	0x0000	0xFFFF
SPI0,1	-	-	-	SPSCR	SPI Sequence Control Register	0x08	8	read/ write	0x00	0xFF
SPI0,1	-	-	-	SPSSR	SPI Sequence Status Register	0x09	8	read-only	0x00	0xFF
SPI0,1	-	-	-	SPBR	SPI Bit Rate Register	0x0A	8	read/ write	0xFF	0xFF
SPI0,1	-	-	-	SPDCR	SPI Data Control Register	0x0B	8	read/ write	0x00	0xFF
SPI0,1	-	-	-	SPCKD	SPI Clock Delay Register	0x0C	8	read/ write	0x00	0xFF

Table 3.3 寄存器说明（44中的31）

周边暗淡	昏暗的增量。	暗淡索引寄存器名称	Description	地址偏移	尺寸	访问	重置值	重置蒙版
SCI0-9	-	-	-	SIMR3	I2C模式寄存器3	0x0B	8	read/ write	0x00	0xFF
SCI0-9	-	-	-	SISR	I2C状态寄存器	0x0C	8	只读	0x00	0xCB
SCI0-9	-	-	-	SPMR	SPI模式寄存器	0x0D	8	read/ write	0x00	0xFF
SCI0-9	-	-	-	TDRHL	发送9位数据寄存器	0x0E	16	read/ write	0xFFFF	0xFFFF
SCI0-9	-	-	-	FTDRHL	发送FIFO数据寄存器HL	0x0E	16	只写	0xFFFF	0xFFFF
SCI0-9	-	-	-	FTDRH	发送FIFO数据寄存器H	0x0E	8	只写	0xFF	0xFF
SCI0-9	-	-	-	FTDRL	发送FIFO数据寄存器L	0x0F	8	只写	0xFF	0xFF
SCI0-9	-	-	-	RDRHL	接收9位数据寄存器	0x10	16	只读	0x0000	0xFFFF
SCI0-9	-	-	-	FRDRHL	接收FIFO数据寄存器HL	0x10	16	只读	0x0000	0xFFFF
SCI0-9	-	-	-	FRDRH	接收FIFO数据寄存器H	0x10	8	只读	0x00	0xFF
SCI0-9	-	-	-	FRDRL	接收FIFO数据寄存器L	0x11	8	只读	0x00	0xFF
SCI0-9	-	-	-	MDDR	调制占空比寄存器	0x12	8	read/ write	0xFF	0xFF
SCI0-9	-	-	-	DCCR	数据比较匹配控制寄存器	0x13	8	read/ write	0x40	0xFF
SCI0-9	-	-	-	FCR	先进先出控制寄存器	0x14	16	read/ write	0xF800	0xFFFF
SCI0-9	-	-	-	FDR	FIFO数据计数寄存器	0x16	16	只读	0x0000	0xFFFF
SCI0-9	-	-	-	LSR	线路状态寄存器	0x18	16	只读	0x0000	0xFFFF
SCI0-9	-	-	-	CDR	比较匹配数据Register	0x1A	16	read/ write	0x0000	0xFFFF
SCI0-9	-	-	-	SPTR	串口寄存器	0x1C	8	read/ write	0x03	0xFF
IRDA	-	-	-	IRCR	红外线控制寄存器	0x00	8	read/ write	0x00	0xFF
SPI0,1	-	-	-	SPCR	SPI控制寄存器	0x00	8	read/ write	0x00	0xFF
SPI0,1	-	-	-	SSLP	SPI从机选择极性Register	0x01	8	read/ write	0x00	0xFF
SPI0,1	-	-	-	SPPCR	RSPI引脚控制寄存器	0x02	8	read/ write	0x00	0xFF
SPI0,1	-	-	-	SPSR	SPI状态寄存器	0x03	8	read/ write	0x20	0xFF
SPI0,1	-	-	-	SPDR	SPI数据寄存器	0x04	32	read/ write	0x00000000	0xFFFFFFFF
SPI0,1	-	-	-	SPDR_HA	SPI数据寄存器（半字访问）	0x04	16	read/ write	0x0000	0xFFFF
SPI0,1	-	-	-	SPSCR	SPI序列控制Register	0x08	8	read/ write	0x00	0xFF
SPI0,1	-	-	-	SPSSR	SPI序列状态Register	0x09	8	只读	0x00	0xFF
SPI0,1	-	-	-	SPBR	SPI比特率寄存器	0x0A	8	read/ write	0xFF	0xFF
SPI0,1	-	-	-	SPDCR	SPI数据控制寄存器	0x0B	8	read/ write	0x00	0xFF
SPI0,1	-	-	-	SPCKD	SPI时钟延迟寄存器	0x0C	8	read/ write	0x00	0xFF

Table 3.3 Register description (32 of 44)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
SPI0,1	-	-	-	SSLND	SPI Slave Select Negation Delay Register	0x0D	8	read/ write	0x00	0xFF
SPI0,1	-	-	-	SPND	SPI Next-Access Delay Register	0x0E	8	read/ write	0x00	0xFF
SPI0,1	-	-	-	SPCR2	SPI Control Register 2	0x0F	8	read/ write	0x00	0xFF
SPI0,1	8	0x2	0-7	SPCMD%s	SPI Command Register %s	0x10	16	read/ write	0x070D	0xFFFF
SPI0,1	-	-	-	SPDCR2	SPI Data Control Register 2	0x20	8	read/ write	0x00	0xFF
CRC	-	-	-	CRCCR0	CRC Control Register0	0x00	8	read/ write	0x00	0xFF
CRC	-	-	-	CRCCR1	CRC Control Register1	0x01	8	read/ write	0x00	0xFF
CRC	-	-	-	CRCDIR	CRC Data Input Register	0x04	32	read/ write	0x00000000	0xFFFFFFFF
CRC	-	-	-	CRCDIR_BY	CRC Data Input Register (byte access)	0x04	8	read/ write	0x00	0xFF
CRC	-	-	-	CRCDOR	CRC Data Output Register	0x08	32	read/ write	0x00000000	0xFFFFFFFF
CRC	-	-	-	CRCDOR_HA	CRC Data Output Register (halfword access)	0x08	16	read/ write	0x0000	0xFFFF
CRC	-	-	-	CRCDOR_BY	CRC Data Output Register (byte access)	0x08	8	read/ write	0x00	0xFF
CRC	-	-	-	CRCSAR	Snoop Address Register	0x0C	16	read/ write	0x0000	0xFFFF
GPT32EH0-3,GPT32E4-7	-	-	-	GTWP	General PWM Timer Write-Protection Register	0x00	32	read/ write	0x00000000	0xFFFFFFFF
GPT32EH0-3,GPT32E4-7	-	-	-	GTSTR	General PWM Timer Software Start Register	0x04	32	read/ write	0x00000000	0xFFFFFFFF
GPT32EH0-3,GPT32E4-7	-	-	-	GTSTP	General PWM Timer Software Stop Register	0x08	32	read/ write	0xFFFFFFFF	0xFFFFFFFF
GPT32EH0-3,GPT32E4-7	-	-	-	GTCLR	General PWM Timer Software Clear Register	0x0C	32	write-only	0x00000000	0xFFFFFFFF
GPT32EH0-3,GPT32E4-7	-	-	-	GTSSR	General PWM Timer Start Source Select Register	0x10	32	read/ write	0x00000000	0xFFFFFFFF
GPT32EH0-3,GPT32E4-7	-	-	-	GTPSR	General PWM Timer Stop Source Select Register	0x14	32	read/ write	0x00000000	0xFFFFFFFF
GPT32EH0-3,GPT32E4-7	-	-	-	GTCSR	General PWM Timer Clear Source Select Register	0x18	32	read/ write	0x00000000	0xFFFFFFFF
GPT32EH0-3,GPT32E4-7	-	-	-	GTUPSR	General PWM Timer Up Count Source Select Register	0x1C	32	read/ write	0x00000000	0xFFFFFFFF

Table 3.3 寄存器描述（44中的32）

周边暗淡	昏暗的增量。	暗淡索引寄存器名称		Description	地址偏移	尺寸	访问	重置值	重置蒙版
SPI0,1	-	-	-	SSLND	SPI从机选择否定延迟寄存器	0x0D	8	read/ write	0x00	0xFF
SPI0,1	-	-	-	SPND	SPI下一次访问延迟Register	0x0E	8	read/ write	0x00	0xFF
SPI0,1	-	-	-	SPCR2	SPI控制寄存器2	0x0F	8	read/ write	0x00	0xFF
SPI0,1	8	0x2	0-7	SPCMD%s	SPI命令寄存器%s	0x10	16	read/ write	0x070D	0xFFFF
SPI0,1	-	-	-	SPDCR2	SPI数据控制寄存器2	0x20	8	read/ write	0x00	0xFF
CRC	-	-	-	CRCCR0	CRC Control Register0	0x00	8	read/ write	0x00	0xFF
CRC	-	-	-	CRCCR1	CRC Control Register1	0x01	8	read/ write	0x00	0xFF
CRC	-	-	-	CRCDIR	CRC数据输入寄存器	0x04	32	read/ write	0x00000000	0xFFFFFFFF
CRC	-	-	-	CRCDIR_BY	CRC数据输入寄存器（字节访问）	0x04	8	read/ write	0x00	0xFF
CRC	-	-	-	CRCDOR	CRC数据输出寄存器	0x08	32	read/ write	0x00000000	0xFFFFFFFF
CRC	-	-	-	CRCDOR_HA	CRC数据输出寄存器（半字访问）	0x08	16	read/ write	0x0000	0xFFFF
CRC	-	-	-	CRCDOR_BY	CRC数据输出寄存器（字节访问）	0x08	8	read/ write	0x00	0xFF
CRC	-	-	-	CRCSAR	窥探地址寄存器	0x0C	16	read/ write	0x0000	0xFFFF
GPT32EH0-3,GPT32E4-7	-	-	-	GTWP	通用PWM定时器写保护登记册	0x00	32	read/ write	0x00000000	0xFFFFFFFF
GPT32EH0-3,GPT32E4-7	-	-	-	GTSTR	通用PWM定时器软件启动寄存器	0x04	32	read/ write	0x00000000	0xFFFFFFFF
GPT32EH0-3,GPT32E4-7	-	-	-	GTSTP	通用PWM定时器软件停止寄存器	0x08	32	read/ write	0xFFFFFFFF	0xFFFFFFFF
GPT32EH0-3,GPT32E4-7	-	-	-	GTCLR	通用PWM定时器软件清除寄存器	0x0C	32	只写	0x00000000	0xFFFFFFFF
GPT32EH0-3,GPT32E4-7	-	-	-	GTSSR	通用PWM定时器启动源选择寄存器	0x10	32	read/ write	0x00000000	0xFFFFFFFF
GPT32EH0-3,GPT32E4-7	-	-	-	GTPSR	通用PWM定时器停止源选择寄存器	0x14	32	read/ write	0x00000000	0xFFFFFFFF
GPT32EH0-3,GPT32E4-7	-	-	-	GTCSR	通用PWM定时器清零源选择寄存器	0x18	32	read/ write	0x00000000	0xFFFFFFFF
GPT32EH0-3,GPT32E4-7	-	-	-	GTUPSR	通用PWM定时器启动计数源选择Register	0x1C	32	read/ write	0x00000000	0xFFFFFFFF

Table 3.3 Register description (33 of 44)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
GPT32EH0-3,GPT32E4-7	-	-	-	GTDNSR	General PWM Timer Down Count Source Select Register	0x20	32	read/ write	0x00000000	0xFFFFFFFF
GPT32EH0-3,GPT32E4-7	-	-	-	GTICASR	General PWM Timer Input Capture Source Select Register A	0x24	32	read/ write	0x00000000	0xFFFFFFFF
GPT32EH0-3,GPT32E4-7	-	-	-	GTICBSR	General PWM Timer Input Capture Source Select Register B	0x28	32	read/ write	0x00000000	0xFFFFFFFF
GPT32EH0-3,GPT32E4-7	-	-	-	GTCR	General PWM Timer Control Register	0x2C	32	read/ write	0x00000000	0xFFFFFFFF
GPT32EH0-3,GPT32E4-7	-	-	-	GTUDDTYC	General PWM Timer Count Direction and Duty Setting Register	0x30	32	read/ write	0x00000001	0xFFFFFFFF
GPT32EH0-3,GPT32E4-7	-	-	-	GTIOR	General PWM Timer I/O Control Register	0x34	32	read/ write	0x00000000	0xFFFFFFFF
GPT32EH0-3,GPT32E4-7	-	-	-	GTINTAD	General PWM Timer Interrupt Output Setting Register	0x38	32	read/ write	0x00000000	0xFFFFFFFF
GPT32EH0-3,GPT32E4-7	-	-	-	GTST	General PWM Timer Status Register	0x3C	32	read/ write	0x00008000	0xFFFFFFFF
GPT32EH0-3,GPT32E4-7	-	-	-	GTBER	General PWM Timer Buffer Enable Register	0x40	32	read/ write	0x00000000	0xFFFFFFFF
GPT32EH0-3,GPT32E4-7	-	-	-	GTITC	General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register	0x44	32	read/ write	0x00000000	0xFFFFFFFF
GPT32EH0-3,GPT32E4-7	-	-	-	GTCNT	General PWM Timer Counter	0x48	32	read/ write	0x00000000	0xFFFFFFFF
GPT32EH0-3,GPT32E4-7	-	-	-	GTCCRA	General PWM Timer Compare Capture Register A	0x4C	32	read/ write	0xFFFFFFFF	0xFFFFFFFF
GPT32EH0-3,GPT32E4-7	-	-	-	GTCCRB	General PWM Timer Compare Capture Register B	0x50	32	read/ write	0xFFFFFFFF	0xFFFFFFFF
GPT32EH0-3,GPT32E4-7	-	-	-	GTCCRC	General PWM Timer Compare Capture Register C	0x54	32	read/ write	0xFFFFFFFF	0xFFFFFFFF
GPT32EH0-3,GPT32E4-7	-	-	-	GTCCRE	General PWM Timer Compare Capture Register E	0x58	32	read/ write	0xFFFFFFFF	0xFFFFFFFF

Table 3.3 寄存器描述（44中的33）

周边暗淡	昏暗的增量。	暗淡索引寄存器名称		Description	地址偏移	尺寸访问		重置值	重置蒙版
GPT32EH0-3,GPT32E4-7	-	-	-	GTDNSR	通用PWM定时器停机计数源选择 Register	0x20	32	read/ write	0x00000000	0xFFFFFFFF
GPT32EH0-3,GPT32E4-7	-	-	-	GTICASR	通用PWM定时器输入捕获源选择 Register A	0x24	32	read/ write	0x00000000	0xFFFFFFFF
GPT32EH0-3,GPT32E4-7	-	-	-	GTICBSR	通用PWM定时器输入捕获源选择 Register B	0x28	32	read/ write	0x00000000	0xFFFFFFFF
GPT32EH0-3,GPT32E4-7	-	-	-	GTCR	通用PWM定时器控制 Register	0x2C	32	read/ write	0x00000000	0xFFFFFFFF
GPT32EH0-3,GPT32E4-7	-	-	-	GTUDDTYC	通用PWM定时器计数方向和占空比设置 Register	0x30	32	read/ write	0x00000001	0xFFFFFFFF
GPT32EH0-3,GPT32E4-7	-	-	-	GTIOR	通用PWM定时器IO控制寄存器	0x34	32	read/ write	0x00000000	0xFFFFFFFF
GPT32EH0-3,GPT32E4-7	-	-	-	GTINTAD	通用PWM定时器中断输出设置 Register	0x38	32	read/ write	0x00000000	0xFFFFFFFF
GPT32EH0-3,GPT32E4-7	-	-	-	GTST	通用PWM定时器状态 Register	0x3C	32	read/ write	0x00008000	0xFFFFFFFF
GPT32EH0-3,GPT32E4-7	-	-	-	GTBER	通用PWM定时器缓冲器启用注册	0x40	32	read/ write	0x00000000	0xFFFFFFFF
GPT32EH0-3,GPT32E4-7	-	-	-	GTITC	通用PWM定时器中断和AD转换器开始请求跳过设置寄存器	0x44	32	read/ write	0x00000000	0xFFFFFFFF
GPT32EH0-3,GPT32E4-7	-	-	-	GTCNT	通用PWM定时器计数器0x48		32	read/ write	0x00000000	0xFFFFFFFF
GPT32EH0-3,GPT32E4-7	-	-	-	GTCCRA	通用PWM定时器比较捕获寄存器A	0x4C	32	read/ write	0xFFFFFFFF	0xFFFFFFFF
GPT32EH0-3,GPT32E4-7	-	-	-	GTCCRB	通用PWM定时器比较捕捉寄存器B	0x50	32	read/ write	0xFFFFFFFF	0xFFFFFFFF
GPT32EH0-3,GPT32E4-7	-	-	-	GTCCRC	通用PWM定时器比较捕捉寄存器C	0x54	32	read/ write	0xFFFFFFFF	0xFFFFFFFF
GPT32EH0-3,GPT32E4-7	-	-	-	GTCCRE	通用PWM定时器比较捕捉寄存器E	0x58	32	read/ write	0xFFFFFFFF	0xFFFFFFFF

Table 3.3 Register description (34 of 44)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
GPT32EH0-3,GPT32E4-7	-	-	-	GTCCRD	General PWM Timer Compare Capture Register D	0x5C	32	read/write	0xFFFFFFFF	0xFFFFFFFF
GPT32EH0-3,GPT32E4-7	-	-	-	GTCCRF	General PWM Timer Compare Capture Register F	0x60	32	read/write	0xFFFFFFFF	0xFFFFFFFF
GPT32EH0-3,GPT32E4-7	-	-	-	GTPR	General PWM Timer Cycle Setting Register	0x64	32	read/write	0xFFFFFFFF	0xFFFFFFFF
GPT32EH0-3,GPT32E4-7	-	-	-	GTPBR	General PWM Timer Cycle Setting Buffer Register	0x68	32	read/write	0xFFFFFFFF	0xFFFFFFFF
GPT32EH0-3,GPT32E4-7	-	-	-	GTPDBR	General PWM Timer Cycle Setting Double-Buffer Register	0x6C	32	read/write	0xFFFFFFFF	0xFFFFFFFF
GPT32EH0-3,GPT32E4-7	-	-	-	GTADTRA	A/D Converter Start Request Timing Register A	0x70	32	read/write	0xFFFFFFFF	0xFFFFFFFF
GPT32EH0-3,GPT32E4-7	-	-	-	GTADTBRA	A/D Converter Start Request Timing Buffer Register A	0x74	32	read/write	0xFFFFFFFF	0xFFFFFFFF
GPT32EH0-3,GPT32E4-7	-	-	-	GTADTDBRA	A/D Converter Start Request Timing Double-Buffer Register A	0x78	32	read/write	0xFFFFFFFF	0xFFFFFFFF
GPT32EH0-3,GPT32E4-7	-	-	-	GTADTRB	A/D Converter Start Request Timing Register B	0x7C	32	read/write	0xFFFFFFFF	0xFFFFFFFF
GPT32EH0-3,GPT32E4-7	-	-	-	GTADTBRB	A/D Converter Start Request Timing Buffer Register B	0x80	32	read/write	0xFFFFFFFF	0xFFFFFFFF
GPT32EH0-3,GPT32E4-7	-	-	-	GTADTDBRB	A/D Converter Start Request Timing Double-Buffer Register B	0x84	32	read/write	0xFFFFFFFF	0xFFFFFFFF
GPT32EH0-3,GPT32E4-7	-	-	-	GTDTCR	General PWM Timer Dead Time Control Register	0x88	32	read/write	0x00000000	0xFFFFFFFF
GPT32EH0-3,GPT32E4-7	-	-	-	GTDVU	General PWM Timer Dead Time Value Register U	0x8C	32	read/write	0xFFFFFFFF	0xFFFFFFFF
GPT32EH0-3,GPT32E4-7	-	-	-	GTDVD	General PWM Timer Dead Time Value Register D	0x90	32	read/write	0xFFFFFFFF	0xFFFFFFFF
GPT32EH0-3,GPT32E4-7	-	-	-	GTDBU	General PWM Timer Dead Time Buffer Register U	0x94	32	read/write	0xFFFFFFFF	0xFFFFFFFF

Table 3.3 寄存器说明（44中的34）

周边暗淡	昏暗的增量。	暗淡索引寄存器名称		Description	地址偏移	尺寸	访问	重置值	重置蒙版
GPT32EH0-3,GPT32E4-7	-	-	-	GTCCRD	通用PWM定时器比较捕捉寄存器D	0x5C	32	read/write	0xFFFFFFFF	0xFFFFFFFF
GPT32EH0-3,GPT32E4-7	-	-	-	GTCCRF	通用PWM定时器比较捕捉寄存器F	0x60	32	read/write	0xFFFFFFFF	0xFFFFFFFF
GPT32EH0-3,GPT32E4-7	-	-	-	GTPR	通用PWM定时器周期设置寄存器	0x64	32	read/write	0xFFFFFFFF	0xFFFFFFFF
GPT32EH0-3,GPT32E4-7	-	-	-	GTPBR	通用PWM定时器周期设置缓冲寄存器	0x68	32	read/write	0xFFFFFFFF	0xFFFFFFFF
GPT32EH0-3,GPT32E4-7	-	-	-	GTPDBR	通用PWM定时器周期Setting Double-Buffer Register	0x6C	32	read/write	0xFFFFFFFF	0xFFFFFFFF
GPT32EH0-3,GPT32E4-7	-	-	-	GTADTRA	AD转换器启动请求时序寄存器A	0x70	32	read/write	0xFFFFFFFF	0xFFFFFFFF
GPT32EH0-3,GPT32E4-7	-	-	-	GTADTBRA	AD转换器启动请求时序缓冲寄存器A	0x74	32	read/write	0xFFFFFFFF	0xFFFFFFFF
GPT32EH0-3,GPT32E4-7	-	-	-	GTADTDBRA	AD转换器启动请求Timing Double-Buffer Register A	0x78	32	read/write	0xFFFFFFFF	0xFFFFFFFF
GPT32EH0-3,GPT32E4-7	-	-	-	GTADTRB	AD转换器启动请求时序寄存器B	0x7C	32	read/write	0xFFFFFFFF	0xFFFFFFFF
GPT32EH0-3,GPT32E4-7	-	-	-	GTADTBRB	AD转换器启动请求时序缓冲寄存器B	0x80	32	read/write	0xFFFFFFFF	0xFFFFFFFF
GPT32EH0-3,GPT32E4-7	-	-	-	GTADTDBRB	AD转换器启动请求Timing Double-Buffer Register B	0x84	32	read/write	0xFFFFFFFF	0xFFFFFFFF
GPT32EH0-3,GPT32E4-7	-	-	-	GTDTCR	通用PWM定时器死机时间控制寄存器	0x88	32	read/write	0x00000000	0xFFFFFFFF
GPT32EH0-3,GPT32E4-7	-	-	-	GTDVU	通用PWM定时器死机时间值寄存器U	0x8C	32	read/write	0xFFFFFFFF	0xFFFFFFFF
GPT32EH0-3,GPT32E4-7	-	-	-	GTDVD	通用PWM定时器死机时间值寄存器D	0x90	32	read/write	0xFFFFFFFF	0xFFFFFFFF
GPT32EH0-3,GPT32E4-7	-	-	-	GTDBU	通用PWM定时器死机时间缓冲寄存器U	0x94	32	read/write	0xFFFFFFFF	0xFFFFFFFF

Table 3.3 Register description (35 of 44)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
GPT32EH0-3,GPT32E4-7	-	-	-	GTDBD	General PWM Timer Dead Time Buffer Register D	0x98	32	read/write	0xFFFFFFFF	0xFFFFFFFF
GPT32EH0-3,GPT32E4-7	-	-	-	GTSOS	General PWM Timer Output Protection Function Status Register	0x9C	32	read-only	0x00000000	0xFFFFFFFF
GPT32EH0-3,GPT32E4-7	-	-	-	GTSOTR	General PWM Timer Output Protection Function Temporary Release Register	0xA0	32	read/write	0x00000000	0xFFFFFFFF
GPT328-13	-	-	-	GTWP	General PWM Timer Write-Protection Register	0x00	32	read/write	0x00000000	0xFFFFFFFF
GPT328-13	-	-	-	GTSTR	General PWM Timer Software Start Register	0x04	32	read/write	0x00000000	0xFFFFFFFF
GPT328-13	-	-	-	GTSTP	General PWM Timer Software Stop Register	0x08	32	read/write	0xFFFFFFFF	0xFFFFFFFF
GPT328-13	-	-	-	GTCLR	General PWM Timer Software Clear Register	0x0C	32	write-only	0x00000000	0xFFFFFFFF
GPT328-13	-	-	-	GTSSR	General PWM Timer Start Source Select Register	0x10	32	read/write	0x00000000	0xFFFFFFFF
GPT328-13	-	-	-	GTPSR	General PWM Timer Stop Source Select Register	0x14	32	read/write	0x00000000	0xFFFFFFFF
GPT328-13	-	-	-	GTCSR	General PWM Timer Clear Source Select Register	0x18	32	read/write	0x00000000	0xFFFFFFFF
GPT328-13	-	-	-	GTUPSR	General PWM Timer Up Count Source Select Register	0x1C	32	read/write	0x00000000	0xFFFFFFFF
GPT328-13	-	-	-	GTDNSR	General PWM Timer Down Count Source Select Register	0x20	32	read/write	0x00000000	0xFFFFFFFF
GPT328-13	-	-	-	GTICASR	General PWM Timer Input Capture Source Select Register A	0x24	32	read/write	0x00000000	0xFFFFFFFF
GPT328-13	-	-	-	GTICBSR	General PWM Timer Input Capture Source Select Register B	0x28	32	read/write	0x00000000	0xFFFFFFFF
GPT328-13	-	-	-	GTCR	General PWM Timer Control Register	0x2C	32	read/write	0x00000000	0xFFFFFFFF
GPT328-13	-	-	-	GTUDDTYC	General PWM Timer Count Direction and Duty Setting Register	0x30	32	read/write	0x00000001	0xFFFFFFFF
GPT328-13	-	-	-	GTIOR	General PWM Timer I/O Control Register	0x34	32	read/write	0x00000000	0xFFFFFFFF
GPT328-13	-	-	-	GTINTAD	General PWM Timer Interrupt Output Setting Register	0x38	32	read/write	0x00000000	0xFFFFFFFF
GPT328-13	-	-	-	GTST	General PWM Timer Status Register	0x3C	32	read/write	0x00008000	0xFFFFFFFF
GPT328-13	-	-	-	GTBER	General PWM Timer Buffer Enable Register	0x40	32	read/write	0x00000000	0xFFFFFFFF
GPT328-13	-	-	-	GTITC	General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register	0x44	32	read/write	0x00000000	0xFFFFFFFF
GPT328-13	-	-	-	GTCNT	General PWM Timer Counter	0x48	32	read/write	0x00000000	0xFFFFFFFF
GPT328-13	-	-	-	GTCCRA	General PWM Timer Compare Capture Register A	0x4C	32	read/write	0xFFFFFFFF	0xFFFFFFFF

Table 3.3 寄存器说明（44个中的35个）

周边暗淡	昏暗的增量。	暗淡索引寄存器名称		Description	地址偏移	尺寸	访问	重置值	重置蒙版
GPT32EH0-3,GPT32E4-7	-	-	GTDBD	通用PWM定时器死机时间缓冲寄存器D	0x98	32	read/write	0xFFFFFFFF	0xFFFFFFFF
GPT32EH0-3,GPT32E4-7	-	-	GTSOS	通用PWM定时器输出保护功能状态Register	0x9C	32	只读	0x00000000	0xFFFFFFFF
GPT32EH0-3,GPT32E4-7	-	-	GTSOTR	通用PWM定时器输出保护功能临时释放登记册	0xA0	32	read/write	0x00000000	0xFFFFFFFF
GPT328-13	-	-	GTWP	通用PWM定时器写保护登记册	0x00	32	read/write	0x00000000	0xFFFFFFFF
GPT328-13	-	-	GTSTR	通用PWM定时器软件启动寄存器	0x04	32	read/write	0x00000000	0xFFFFFFFF
GPT328-13	-	-	GTSTP	通用PWM定时器软件停止寄存器	0x08	32	read/write	0xFFFFFFFF	0xFFFFFFFF
GPT328-13	-	-	GTCLR	通用PWM定时器软件清除寄存器	0x0C	32	只写	0x00000000	0xFFFFFFFF
GPT328-13	-	-	GTSSR	通用PWM定时器启动源选择寄存器	0x10	32	read/write	0x00000000	0xFFFFFFFF
GPT328-13	-	-	GTPSR	通用PWM定时器停止源选择寄存器	0x14	32	read/write	0x00000000	0xFFFFFFFF
GPT328-13	-	-	GTCSR	通用PWM定时器清零源选择寄存器	0x18	32	read/write	0x00000000	0xFFFFFFFF
GPT328-13	-	-	GTUPSR	通用PWM定时器启动计数源选择Register	0x1C	32	read/write	0x00000000	0xFFFFFFFF
GPT328-13	-	-	GTDNSR	通用PWM定时器停机计数源选择Register	0x20	32	read/write	0x00000000	0xFFFFFFFF
GPT328-13	-	-	GTICASR	通用PWM定时器输入捕获源选择Register A	0x24	32	read/write	0x00000000	0xFFFFFFFF
GPT328-13	-	-	GTICBSR	通用PWM定时器输入捕获源选择Register B	0x28	32	read/write	0x00000000	0xFFFFFFFF
GPT328-13	-	-	GTCR	通用PWM定时器控制Register	0x2C	32	read/write	0x00000000	0xFFFFFFFF
GPT328-13	-	-	GTUDDTYC	通用PWM定时器计数方向和占空比设置Register	0x30	32	read/write	0x00000001	0xFFFFFFFF
GPT328-13	-	-	GTIOR	通用PWM定时器IO控制寄存器	0x34	32	read/write	0x00000000	0xFFFFFFFF
GPT328-13	-	-	GTINTAD	通用PWM定时器中断输出设置Register	0x38	32	read/write	0x00000000	0xFFFFFFFF
GPT328-13	-	-	GTST	通用PWM定时器状态Register	0x3C	32	read/write	0x00008000	0xFFFFFFFF
GPT328-13	-	-	GTBER	通用PWM定时器缓冲器启用注册	0x40	32	read/write	0x00000000	0xFFFFFFFF
GPT328-13	-	-	GTITC	通用PWM定时器中断和AD转换器开始请求跳过设置寄存器	0x44	32	read/write	0x00000000	0xFFFFFFFF
GPT328-13	-	-	GTCNT	通用PWM定时器计数器0x48		32	read/write	0x00000000	0xFFFFFFFF
GPT328-13	-	-	GTCCRA	通用PWM定时器比较捕获寄存器A	0x4C	32	read/write	0xFFFFFFFF	0xFFFFFFFF

Table 3.3 Register description (36 of 44)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
GPT328-13	-	-	-	GTCCRB	General PWM Timer Compare Capture Register B	0x50	32	read/ write	0xFFFFFFFF	0xFFFFFFFF
GPT328-13	-	-	-	GTCCRC	General PWM Timer Compare Capture Register C	0x54	32	read/ write	0xFFFFFFFF	0xFFFFFFFF
GPT328-13	-	-	-	GTCCRE	General PWM Timer Compare Capture Register E	0x58	32	read/ write	0xFFFFFFFF	0xFFFFFFFF
GPT328-13	-	-	-	GTCCRD	General PWM Timer Compare Capture Register D	0x5C	32	read/ write	0xFFFFFFFF	0xFFFFFFFF
GPT328-13	-	-	-	GTCCRF	General PWM Timer Compare Capture Register F	0x60	32	read/ write	0xFFFFFFFF	0xFFFFFFFF
GPT328-13	-	-	-	GTPR	General PWM Timer Cycle Setting Register	0x64	32	read/ write	0xFFFFFFFF	0xFFFFFFFF
GPT328-13	-	-	-	GTPBR	General PWM Timer Cycle Setting Buffer Register	0x68	32	read/ write	0xFFFFFFFF	0xFFFFFFFF
GPT328-13	-	-	-	GTDTCR	General PWM Timer Dead Time Control Register	0x88	32	read/ write	0x00000000	0xFFFFFFFF
GPT328-13	-	-	-	GTDVU	General PWM Timer Dead Time Value Register U	0x8C	32	read/ write	0xFFFFFFFF	0xFFFFFFFF
GPT_OPS	-	-	-	OPSCR	Output Phase Switching Control Register	0x00	32	read/ write	0x00000000	0xFFFFFFFF
GPT_ODC	-	-	-	GTDLYCR	PWM Output Delay Control Register	0x00	16	read/ write	0x0000	0xFFFF
GPT_ODC	-	-	-	GTDLYCR2	PWM Output Delay Control Register2	0x02	16	read/ write	0x0000	0xFFFF
GPT_ODC	4	0x4	0-3	GTDLYR%sA	GTIOC%sA Rising Output Delay Register	0x18	16	read/ write	0x0000	0xFFFF
GPT_ODC	4	0x4	0-3	GTDLYR%sB	GTIOC%sB Rising Output Delay Register	0x1A	16	read/ write	0x0000	0xFFFF
GPT_ODC	4	0x4	0-3	GTDLYF%sA	GTIOC%sA Falling Output Delay Register	0x28	16	read/ write	0x0000	0xFFFF
GPT_ODC	4	0x4	0-3	GTDLYF%sB	GTIOC%sB Falling Output Delay Register	0x2A	16	read/ write	0x0000	0xFFFF
KINT	-	-	-	KRCTL	KEY Return Control Register	0x00	8	read/ write	0x00	0xFF
KINT	-	-	-	KRF	KEY Return Flag Register	0x04	8	read/ write	0x00	0xFF
KINT	-	-	-	KRM	KEY Return Mode Register	0x08	8	read/ write	0x00	0xFF
CTSU	-	-	-	CTSUCR0	CTSU Control Register 0	0x00	8	read/ write	0x00	0xFF
CTSU	-	-	-	CTSUCR1	CTSU Control Register 1	0x01	8	read/ write	0x00	0xFF
CTSU	-	-	-	CTSUSDPRS	CTSU Synchronous Noise Reduction Setting Register	0x02	8	read/ write	0x00	0xFF
CTSU	-	-	-	CTSUSST	CTSU Sensor Stabilization Wait Control Register	0x03	8	read/ write	0x00	0xFF
CTSU	-	-	-	CTSUMCH0	CTSU Measurement Channel Register 0	0x04	8	read/ write	0x1F	0xFF
CTSU	-	-	-	CTSUMCH1	CTSU Measurement Channel Register 1	0x05	8	read/ write	0x1F	0xFF
CTSU	-	-	-	CTSUCHAC0	CTSU Channel Enable Control Register 0	0x06	8	read/ write	0x00	0xFF
CTSU	-	-	-	CTSUCHAC1	CTSU Channel Enable Control Register 1	0x07	8	read/ write	0x00	0xFF
CTSU	-	-	-	CTSUCHAC2	CTSU Channel Enable Control Register 2	0x08	8	read/ write	0x00	0xFF
CTSU	-	-	-	CTSUCHTRC0	CTSU Channel Transmit/ Receive Control Register 0	0x0B	8	read/ write	0x00	0xFF
CTSU	-	-	-	CTSUCHTRC1	CTSU Channel Transmit/ Receive Control Register 1	0x0C	8	read/ write	0x00	0xFF

Table 3.3 寄存器说明（44中的36）

周边暗淡	昏暗的增量。	暗淡索引寄存器名称		Description	地址偏移	尺寸	访问	重置值	重置蒙版
GPT328-13	-	-	GTCCRB	通用PWM定时器比较捕捉寄存器B	0x50	32	read/ write	0xFFFFFFFF	0xFFFFFFFF
GPT328-13	-	-	GTCCRC	通用PWM定时器比较捕捉寄存器C	0x54	32	read/ write	0xFFFFFFFF	0xFFFFFFFF
GPT328-13	-	-	GTCCRE	通用PWM定时器比较捕捉寄存器E	0x58	32	read/ write	0xFFFFFFFF	0xFFFFFFFF
GPT328-13	-	-	GTCCRD	通用PWM定时器比较捕捉寄存器D	0x5C	32	read/ write	0xFFFFFFFF	0xFFFFFFFF
GPT328-13	-	-	GTCCRF	通用PWM定时器比较捕捉寄存器F	0x60	32	read/ write	0xFFFFFFFF	0xFFFFFFFF
GPT328-13	-	-	GTPR	通用PWM定时器周期设置寄存器	0x64	32	read/ write	0xFFFFFFFF	0xFFFFFFFF
GPT328-13	-	-	GTPBR	通用PWM定时器周期设置缓冲寄存器	0x68	32	read/ write	0xFFFFFFFF	0xFFFFFFFF
GPT328-13	-	-	GTDTCR	通用PWM定时器死机时间控制寄存器	0x88	32	read/ write	0x00000000	0xFFFFFFFF
GPT328-13	-	-	GTDVU	通用PWM定时器死机时间值寄存器U	0x8C	32	read/ write	0xFFFFFFFF	0xFFFFFFFF
GPT_OPS	-	-	OPSCR	输出相位切换控制寄存器	0x00	32	read/ write	0x00000000	0xFFFFFFFF
GPT_ODC	-	-	GTDLYCR	PWM输出延迟控制Register	0x00	16	read/ write	0x0000	0xFFFF
GPT_ODC	-	-	GTDLYCR2	PWM输出延迟控制Register2	0x02	16	read/ write	0x0000	0xFFFF
GPT_ODC	4	0x4	0-3	GTDLYR%sA	GTIOC%sA上升输出延迟寄存器	0x18	16	read/ write	0x0000	0xFFFF
GPT_ODC	4	0x4	0-3	GTDLYR%sB	GTIOC%sB上升输出延迟寄存器	0x1A	16	read/ write	0x0000	0xFFFF
GPT_ODC	4	0x4	0-3	GTDLYF%sA	GTIOC%sA下降输出延迟寄存器	0x28	16	read/ write	0x0000	0xFFFF
GPT_ODC	4	0x4	0-3	GTDLYF%sB	GTIOC%sB下降输出延迟寄存器	0x2A	16	read/ write	0x0000	0xFFFF
KINT	-	-	-	KRCTL	KEY返回控制寄存器0x 00		8	read/ write	0x00	0xFF
KINT	-	-	-	KRF	KEY返回标志寄存器	0x04	8	read/ write	0x00	0xFF
KINT	-	-	-	KRM	KEY返回模式寄存器	0x08	8	read/ write	0x00	0xFF
CTSU	-	-	-	CTSUCR0	CTSU控制寄存器0	0x00	8	read/ write	0x00	0xFF
CTSU	-	-	-	CTSUCR1	CTSU控制寄存器1	0x01	8	read/ write	0x00	0xFF
CTSU	-	-	-	CTSUSDPRS	CTSU同步降噪设置寄存器	0x02	8	read/ write	0x00	0xFF
CTSU	-	-	-	CTSUSST	CTSU传感器稳定等待控制寄存器	0x03	8	read/ write	0x00	0xFF
CTSU	-	-	-	CTSUMCH0	CTSU Measurement通道寄存器0	0x04	8	read/ write	0x1F	0xFF
CTSU	-	-	-	CTSUMCH1	CTSU Measurement通道寄存器1	0x05	8	read/ write	0x1F	0xFF
CTSU	-	-	-	CTSUCHAC0	CTSU通道启用控制寄存器0	0x06	8	read/ write	0x00	0xFF
CTSU	-	-	-	CTSUCHAC1	CTSU通道启用控制寄存器1	0x07	8	read/ write	0x00	0xFF
CTSU	-	-	-	CTSUCHAC2	CTSU通道启用控制寄存器2	0x08	8	read/ write	0x00	0xFF
CTSU	-	-	-	CTSUCHTRC0	CTSU Channel Transmit/接收控制寄存器0	0x0B	8	read/ write	0x00	0xFF
CTSU	-	-	-	CTSUCHTRC1	CTSU Channel Transmit/接收控制寄存器1	0x0C	8	read/ write	0x00	0xFF

Table 3.3 Register description (37 of 44)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
CTSU	-	-	-	CTSUCHTRC2	CTSU Channel Transmit/ Receive Control Register 2	0x0D	8	read/ write	0x00	0xFF
CTSU	-	-	-	CTSUDCLKC	CTSU High-Pass Noise Reduction Control Register	0x10	8	read/ write	0x00	0xFF
CTSU	-	-	-	CTSUST	CTSU Status Register	0x11	8	read/ write	0x00	0xFF
CTSU	-	-	-	CTSUSSC	CTSU High-Pass Noise Reduction Spectrum Diffusion Control Register	0x12	16	read/ write	0x0000	0xFFFF
CTSU	-	-	-	CTSUSO0	CTSU Sensor Offset Register 0	0x14	16	read/ write	0x0000	0xFFFF
CTSU	-	-	-	CTSUSO1	CTSU Sensor Offset Register 1	0x16	16	read/ write	0x0000	0xFFFF
CTSU	-	-	-	CTSUSC	CTSU Sensor Counter	0x18	16	read-only	0x0000	0xFFFF
CTSU	-	-	-	CTSURC	CTSU Reference Counter	0x1A	16	read-only	0x0000	0xFFFF
CTSU	-	-	-	CTSUERRS	CTSU Error Status Register	0x1C	16	read-only	0x0000	0x7FFF
AGT0,1	-	-	-	AGT	AGT Counter Register	0x00	16	read/ write	0xFFFF	0xFFFF
AGT0,1	-	-	-	AGTCMA	AGT Compare Match A Register	0x02	16	read/ write	0xFFFF	0xFFFF
AGT0,1	-	-	-	AGTCMB	AGT Compare Match B Register	0x04	16	read/ write	0xFFFF	0xFFFF
AGT0,1	-	-	-	AGTCR	AGT Control Register	0x08	8	read/ write	0x00	0xFF
AGT0,1	-	-	-	AGTMR1	AGT Mode Register 1	0x09	8	read/ write	0x00	0xFF
AGT0,1	-	-	-	AGTMR2	AGT Mode Register 2	0x0A	8	read/ write	0x00	0xFF
AGT0,1	-	-	-	AGTIOC	AGT I/O Control Register	0x0C	8	read/ write	0x00	0xFF
AGT0,1	-	-	-	AGTISR	AGT Event Pin Select Register	0x0D	8	read/ write	0x00	0xFF
AGT0,1	-	-	-	AGTCMSR	AGT Compare Match Function Select Register	0x0E	8	read/ write	0x00	0xFF
AGT0,1	-	-	-	AGTIOSEL	AGT Pin Select Register	0x0F	8	read/ write	0x00	0xFF
ACMPHS0	-	-	-	CMPCTL	Comparator Control Register	0x000	8	read/ write	0x00	0xFF
ACMPHS0	-	-	-	CMPSEL0	Comparator Input Select Register	0x004	8	read/ write	0x00	0xFF
ACMPHS0	-	-	-	CMPSEL1	Comparator Reference Voltage Select Register	0x008	8	read/ write	0x00	0xFF
ACMPHS0	-	-	-	CMPMON	Comparator Output Monitor Register	0x00C	8	read-only	0x00	0xFF
ACMPHS0	-	-	-	CPIOC	Comparator Output Control Register	0x010	8	read/ write	0x00	0xFF
ACMPHS1-5	-	-	-	CMPCTL	Comparator Control Register	0x000	8	read/ write	0x00	0xFF
ACMPHS1-5	-	-	-	CMPSEL0	Comparator Input Select Register	0x004	8	read/ write	0x00	0xFF
ACMPHS1-5	-	-	-	CMPSEL1	Comparator Reference Voltage Select Register	0x008	8	read/ write	0x00	0xFF
ACMPHS1-5	-	-	-	CMPMON	Comparator Output Monitor Register	0x00C	8	read-only	0x00	0xFF
ACMPHS1-5	-	-	-	CPIOC	Comparator Output Control Register	0x010	8	read/ write	0x00	0xFF

Table 3.3 寄存器说明（44中的37）

周边暗淡		昏暗的增量。	暗淡索引寄存器名称		Description	地址偏移	尺寸	访问	重置值	重置蒙版
CTSU	-	-	-	CTSUCHTRC2	CTSU Channel Transmit/ 接收控制寄存器2	0x0D	8	read/ write	0x00	0xFF
CTSU	-	-	-	CTSUDCLKC	CTSU High-Pass Noise 减少控制寄存器	0x10	8	read/ write	0x00	0xFF
CTSU	-	-	-	CTSUST	CTSU状态寄存器	0x11	8	read/ write	0x00	0xFF
CTSU	-	-	-	CTSUSSC	CTSU High-Pass Noise 还原光谱 扩散控制寄存器	0x12	16	read/ write	0x0000	0xFFFF
CTSU	-	-	-	CTSUSO0	CTSU传感器偏移 Register 0	0x14	16	read/ write	0x0000	0xFFFF
CTSU	-	-	-	CTSUSO1	CTSU传感器偏移 Register 1	0x16	16	read/ write	0x0000	0xFFFF
CTSU	-	-	-	CTSUSC	CTSU传感器计数器	0x18	16	只读	0x0000	0xFFFF
CTSU	-	-	-	CTSURC	CTSU参考计数器	0x1A	16	只读	0x0000	0xFFFF
CTSU	-	-	-	CTSUERRS	CTSU错误状态寄存器	0x1C	16	只读	0x0000	0x7FFF
AGT0,1	-	-	-	AGT	AGT计数器寄存器	0x00	16	read/ write	0xFFFF	0xFFFF
AGT0,1	-	-	-	AGTCMA	AGT比较匹配A Register	0x02	16	read/ write	0xFFFF	0xFFFF
AGT0,1	-	-	-	AGTCMB	AGT比较匹配B Register	0x04	16	read/ write	0xFFFF	0xFFFF
AGT0,1	-	-	-	AGTCR	AGT控制寄存器	0x08	8	read/ write	0x00	0xFF
AGT0,1	-	-	-	AGTMR1	AGT模式寄存器1	0x09	8	read/ write	0x00	0xFF
AGT0,1	-	-	-	AGTMR2	AGT模式寄存器2	0x0A	8	read/ write	0x00	0xFF
AGT0,1	-	-	-	AGTIOC	AGTIO控制寄存器	0x0C	8	read/ write	0x00	0xFF
AGT0,1	-	-	-	AGTISR	AGT事件引脚选择 Register	0x0D	8	read/ write	0x00	0xFF
AGT0,1	-	-	-	AGTCMSR	AGT比较匹配 功能选择寄存器	0x0E	8	read/ write	0x00	0xFF
AGT0,1	-	-	-	AGTIOSEL	AGT引脚选择寄存器	0x0F	8	read/ write	0x00	0xFF
ACMPHS0	-	-	-	CMPCTL	比较器控制寄存器0x 000		8	read/ write	0x00	0xFF
ACMPHS0	-	-	-	CMPSEL0	比较器输入选择 Register	0x004	8	read/ write	0x00	0xFF
ACMPHS0	-	-	-	CMPSEL1	比较器参考电压选择寄存器	0x008	8	read/ write	0x00	0xFF
ACMPHS0	-	-	-	CMPMON	比较器输出监视器 Register	0x00C	8	只读	0x00	0xFF
ACMPHS0	-	-	-	CPIOC	比较器输出控制 Register	0x010	8	read/ write	0x00	0xFF
ACMPHS1-5	-	-	-	CMPCTL	比较器控制寄存器0x 000		8	read/ write	0x00	0xFF
ACMPHS1-5	-	-	-	CMPSEL0	比较器输入选择 Register	0x004	8	read/ write	0x00	0xFF
ACMPHS1-5	-	-	-	CMPSEL1	比较器参考电压选择寄存器	0x008	8	read/ write	0x00	0xFF
ACMPHS1-5	-	-	-	CMPMON	比较器输出监视器 Register	0x00C	8	只读	0x00	0xFF
ACMPHS1-5	-	-	-	CPIOC	比较器输出控制 Register	0x010	8	read/ write	0x00	0xFF

Table 3.3 Register description (38 of 44)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
USBFS	-	-	-	SYSCFG	System Configuration Control Register	0x000	16	read/ write	0x0000	0xFFFF
USBFS	-	-	-	SYSSTS0	System Configuration Status Register 0	0x004	16	read-only	0x0000	0x0000
USBFS	-	-	-	DVSTCTR0	Device State Control Register 0	0x008	16	read/ write	0x0000	0xFFFF
USBFS	-	-	-	CFIFO	CFIFO Port Register	0x014	16	read/ write	0x0000	0xFFFF
USBFS	-	-	-	CFIFOL	CFIFO Port Register L	0x014	8	read/ write	0x00	0xFF
USBFS	-	-	-	D0FIFO	D0FIFO Port Register	0x018	16	read/ write	0x0000	0xFFFF
USBFS	-	-	-	D0FIFOL	D0FIFO Port Register L	0x018	8	read/ write	0x00	0xFF
USBFS	-	-	-	D1FIFO	D1FIFO Port Register	0x01C	16	read/ write	0x0000	0xFFFF
USBFS	-	-	-	D1FIFOL	D1FIFO Port Register L	0x01C	8	read/ write	0x00	0xFF
USBFS	-	-	-	CFIFOSEL	CFIFO Port Select Register	0x020	16	read/ write	0x0000	0xFFFF
USBFS	-	-	-	CFIFOCTR	CFIFO Port Control Register	0x022	16	read/ write	0x0000	0xFFFF
USBFS	-	-	-	D0FIFOSEL	D0FIFO Port Select Register	0x028	16	read/ write	0x0000	0xFFFF
USBFS	-	-	-	D0FIFOCTR	D0FIFO Port Control Register	0x02A	16	read/ write	0x0000	0xFFFF
USBFS	-	-	-	D1FIFOSEL	D1FIFO Port Select Register	0x02C	16	read/ write	0x0000	0xFFFF
USBFS	-	-	-	D1FIFOCTR	D1FIFO Port Control Register	0x02E	16	read/ write	0x0000	0xFFFF
USBFS	-	-	-	INTENB0	Interrupt Enable Register 0	0x030	16	read/ write	0x0000	0xFFFF
USBFS	-	-	-	INTENB1	Interrupt Enable Register 1	0x032	16	read/ write	0x0000	0xFFFF
USBFS	-	-	-	BRDYENB	BRDY Interrupt Enable Register	0x036	16	read/ write	0x0000	0xFFFF
USBFS	-	-	-	NRDYENB	NRDY Interrupt Enable Register	0x038	16	read/ write	0x0000	0xFFFF
USBFS	-	-	-	BEMPENB	BEMP Interrupt Enable Register	0x03A	16	read/ write	0x0000	0xFFFF
USBFS	-	-	-	SOFCFG	SOF Output Configuration Register	0x03C	16	read/ write	0x0000	0xFFFF
USBFS	-	-	-	INTSTS0	Interrupt Status Register 0	0x040	16	read/ write	0x0000	0xFF7F
USBFS	-	-	-	INTSTS1	Interrupt Status Register 1	0x042	16	read/ write	0x0000	0xFFFF
USBFS	-	-	-	BRDYSTS	BRDY Interrupt Status Register	0x046	16	read/ write	0x0000	0xFFFF
USBFS	-	-	-	NRDYSTS	NRDY Interrupt Status Register	0x048	16	read/ write	0x0000	0xFFFF
USBFS	-	-	-	BEMPSTS	BEMP Interrupt Status Register	0x04A	16	read/ write	0x0000	0xFFFF
USBFS	-	-	-	FRMNUM	Frame Number Register	0x04C	16	read/ write	0x0000	0xFFFF
USBFS	-	-	-	DVCHGR	Device State Change Register	0x04E	16	read/ write	0x0000	0xFFFF
USBFS	-	-	-	USBADDR	USB Address Register	0x050	16	read/ write	0x0000	0xFFFF
USBFS	-	-	-	USBREQ	USB Request Type Register	0x054	16	read/ write	0x0000	0xFFFF

Table 3.3 寄存器描述（44中的38）

周边暗淡	昏暗的增量。	暗淡索引寄存器名称	Description	地址偏移	尺寸	访问	重置值	重置蒙版
USBFS	-	-	-	SYSCFG	系统配置控制寄存器	0x000	16	read/ write	0x0000	0xFFFF
USBFS	-	-	-	SYSSTS0	系统配置状态 Register 0	0x004	16	只读	0x0000	0x0000
USBFS	-	-	-	DVSTCTR0	设备状态控制 Register 0	0x008	16	read/ write	0x0000	0xFFFF
USBFS	-	-	-	CFIFO	CFIFO端口寄存器	0x014	16	read/ write	0x0000	0xFFFF
USBFS	-	-	-	CFIFOL	CFIFO端口寄存器L	0x014	8	read/ write	0x00	0xFF
USBFS	-	-	-	D0FIFO	D0FIFO端口寄存器	0x018	16	read/ write	0x0000	0xFFFF
USBFS	-	-	-	D0FIFOL	D0FIFO端口寄存器L	0x018	8	read/ write	0x00	0xFF
USBFS	-	-	-	D1FIFO	D1FIFO端口寄存器	0x01C	16	read/ write	0x0000	0xFFFF
USBFS	-	-	-	D1FIFOL	D1FIFO端口寄存器L	0x01C	8	read/ write	0x00	0xFF
USBFS	-	-	-	CFIFOSEL	CFIFO端口选择寄存器	0x020	16	read/ write	0x0000	0xFFFF
USBFS	-	-	-	CFIFOCTR	CFIFO端口控制寄存器0x 022		16	read/ write	0x0000	0xFFFF
USBFS	-	-	-	D0FIFOSEL	D0FIFO端口选择寄存器0x 028		16	read/ write	0x0000	0xFFFF
USBFS	-	-	-	D0FIFOCTR	D0FIFO端口控制 Register	0x02A	16	read/ write	0x0000	0xFFFF
USBFS	-	-	-	D1FIFOSEL	D1FIFO端口选择寄存器0x 02C		16	read/ write	0x0000	0xFFFF
USBFS	-	-	-	D1FIFOCTR	D1FIFO端口控制 Register	0x02E	16	read/ write	0x0000	0xFFFF
USBFS	-	-	-	INTENB0	中断使能寄存器0	0x030	16	read/ write	0x0000	0xFFFF
USBFS	-	-	-	INTENB1	中断使能寄存器1	0x032	16	read/ write	0x0000	0xFFFF
USBFS	-	-	-	BRDYENB	BRDY中断使能 Register	0x036	16	read/ write	0x0000	0xFFFF
USBFS	-	-	-	NRDYENB	NRDY中断使能 Register	0x038	16	read/ write	0x0000	0xFFFF
USBFS	-	-	-	BEMPENB	BEMP中断使能 Register	0x03A	16	read/ write	0x0000	0xFFFF
USBFS	-	-	-	SOFCFG	SOF输出配置 Register	0x03C	16	read/ write	0x0000	0xFFFF
USBFS	-	-	-	INTSTS0	中断状态寄存器0	0x040	16	read/ write	0x0000	0xFF7F
USBFS	-	-	-	INTSTS1	中断状态寄存器1	0x042	16	read/ write	0x0000	0xFFFF
USBFS	-	-	-	BRDYSTS	BRDY中断状态 Register	0x046	16	read/ write	0x0000	0xFFFF
USBFS	-	-	-	NRDYSTS	NRDY中断状态 Register	0x048	16	read/ write	0x0000	0xFFFF
USBFS	-	-	-	BEMPSTS	BEMP中断状态 Register	0x04A	16	read/ write	0x0000	0xFFFF
USBFS	-	-	-	FRMNUM	帧号寄存器	0x04C	16	read/ write	0x0000	0xFFFF
USBFS	-	-	-	DVCHGR	设备状态更改 Register	0x04E	16	read/ write	0x0000	0xFFFF
USBFS	-	-	-	USBADDR	USB地址寄存器	0x050	16	read/ write	0x0000	0xFFFF
USBFS	-	-	-	USBREQ	USB请求类型寄存器	0x054	16	read/ write	0x0000	0xFFFF

Table 3.3 Register description (39 of 44)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
USBFS	-	-	-	USBVAL	USB Request Value Register	0x056	16	read/ write	0x0000	0xFFFF
USBFS	-	-	-	USBINDX	USB Request Index Register	0x058	16	read/ write	0x0000	0xFFFF
USBFS	-	-	-	USBLENG	USB Request Length Register	0x05A	16	read/ write	0x0000	0xFFFF
USBFS	-	-	-	DCPCFG	DCP Configuration Register	0x05C	16	read/ write	0x0000	0xFFFF
USBFS	-	-	-	DCPMAXP	DCP Maximum Packet Size Register	0x05E	16	read/ write	0x0040	0xFFFF
USBFS	-	-	-	DCPCTR	DCP Control Register	0x060	16	read/ write	0x0040	0xFFFF
USBFS	-	-	-	PIPESEL	Pipe Window Select Register	0x064	16	read/ write	0x0000	0xFFFF
USBFS	-	-	-	PIPECFG	Pipe Configuration Register	0x068	16	read/ write	0x0000	0xFFFF
USBFS	-	-	-	PIPEMAXP	Pipe Maximum Packet Size Register	0x06C	16	read/ write	0x0000	0xFFBF
USBFS	-	-	-	PIPEPERI	Pipe Cycle Control Register	0x06E	16	read/ write	0x0000	0xFFFF
USBFS	5	0x002	1-5	PIPE%sCTR	Pipe %s Control Register	0x070	16	read/ write	0x0000	0xFFFF
USBFS	4	0x002	6-9	PIPE%sCTR	Pipe %s Control Register	0x07A	16	read/ write	0x0000	0xFFFF
USBFS	5	0x004	1-5	PIPE%sTRE	Pipe %s Transaction Counter Enable Register	0x090	16	read/ write	0x0000	0xFFFF
USBFS	5	0x004	1-5	PIPE%sTRN	Pipe %s Transaction Counter Register	0x092	16	read/ write	0x0000	0xFFFF
USBFS	6	0x002	0-5	DEVADD%s	Device Address %s Configuration Register	0x0D0	16	read/ write	0x0000	0xFFFF
USBFS	-	-	-	PHYSLEW	PHY Cross Point Adjustment Register	0x0F0	32	read/ write	0x0000000E	0xFF4CFFFF
USBFS	-	-	-	DPUSR0R	Deep Software Standby USB Transceiver Control/Pin Monitor Register	0x400	32	read/ write	0x00000000	0xFF4CFFFF
USBFS	-	-	-	DPUSR1R	Deep Software Standby USB Suspend/Resume Interrupt Register	0x404	32	read/ write	0x00000000	0xFFFFFFFF
PDC	-	-	-	PCCR0	PDC Control Register 0	0x000	32	read/ write	0x00000000	0xFFFFFFFF
PDC	-	-	-	PCCR1	PDC Control Register 1	0x004	32	read/ write	0x00000000	0xFFFFFFFF
PDC	-	-	-	PCSR	PDC Status Register	0x008	32	read/ write	0x00000002	0xFFFFFFFF
PDC	-	-	-	PCMONR	PDC Pin Monitor Register	0x00C	32	read-only	0x00000000	0xFFFFFFFF
PDC	-	-	-	PCDR	PDC Receive Data Register	0x010	32	read-only	0x00000000	0xFFFFFFFF
PDC	-	-	-	VCR	Vertical Capture Register	0x014	32	read/ write	0x00000000	0xFFFFFFFF
PDC	-	-	-	HCR	Horizontal Capture Register	0x018	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	256	0x4	0-255	GR1_CLUT0[%s]	Color Palette 0 Plane for Graphics 1 Plane	0x0000	32	read/ write	0x00000000	0x00000000
GLCDC	256	0x4	0-255	GR1_CLUT1[%s]	Color Palette 1 Plane for Graphics 1 Plane	0x0400	32	read/ write	0x00000000	0x00000000
GLCDC	256	0x4	0-255	GR2_CLUT0[%s]	Color Palette 0 Plane for Graphics 2 Plane	0x0800	32	read/ write	0x00000000	0x00000000
GLCDC	256	0x4	0-255	GR2_CLUT1[%s]	Color Palette 1 Plane for Graphics 2 Plane	0x0C00	32	read/ write	0x00000000	0x00000000

Table 3.3 注册描述（44中的39）

周边暗淡	昏暗的增量。	暗淡索引寄存器名称	Description	地址偏移	尺寸访问	重置值	重置蒙版
USBFS	-	-	-	USBVAL	USB请求值寄存器0x 056	16	read/ write	0x0000	0xFFFF
USBFS	-	-	-	USBINDX	USB请求索引寄存器0x 058	16	read/ write	0x0000	0xFFFF
USBFS	-	-	-	USBLENG	USB请求长度 Register	0x05A	16	read/ write	0x0000	0xFFFF
USBFS	-	-	-	DCPCFG	DCP配置寄存器	0x05C	16	read/ write	0x0000	0xFFFF
USBFS	-	-	-	DCPMAXP	DCP最大数据包大小 Register	0x05E	16	read/ write	0x0040	0xFFFF
USBFS	-	-	-	DCPCTR	DCP控制寄存器	0x060	16	read/ write	0x0040	0xFFFF
USBFS	-	-	-	PIPESEL	管道窗口选择寄存器0x 064	16	read/ write	0x0000	0xFFFF
USBFS	-	-	-	PIPECFG	管道配置寄存器	0x068	16	read/ write	0x0000	0xFFFF
USBFS	-	-	-	PIPEMAXP	管道最大数据包大小 Register	0x06C	16	read/ write	0x0000	0xFFBF
USBFS	-	-	-	PIPEPERI	管道循环控制寄存器	0x06E	16	read/ write	0x0000	0xFFFF
USBFS	5	0x002	1-5	PIPE%sCTR	管道%s控制寄存器	0x070	16	read/ write	0x0000	0xFFFF
USBFS	4	0x002	6-9	PIPE%sCTR	管道%s控制寄存器	0x07A	16	read/ write	0x0000	0xFFFF
USBFS	5	0x004	1-5	PIPE%sTRE	管道%s事务 计数器使能寄存器	0x090	16	read/ write	0x0000	0xFFFF
USBFS	5	0x004	1-5	PIPE%sTRN	管道%s事务 计数器寄存器	0x092	16	read/ write	0x0000	0xFFFF
USBFS	6	0x002	0-5	DEVADD%s	设备地址%s 配置寄存器	0x0D0	16	read/ write	0x0000	0xFFFF
USBFS	-	-	-	PHYSLEW	PHY交叉点调整 Register	0x0F0	32	read/ write	0x0000000E	0xFF4CFFFF
USBFS	-	-	-	DPUSR0R	深度软件待机USB Transceiver Control/Pin 监控寄存器	0x400	32	read/ write	0x00000000	0xFF4CFFFF
USBFS	-	-	-	DPUSR1R	深度软件待机USB Suspend/Resume Interrupt Register	0x404	32	read/ write	0x00000000	0xFFFFFFFF
PDC	-	-	-	PCCR0	PDC控制寄存器0	0x000	32	read/ write	0x00000000	0xFFFFFFFF
PDC	-	-	-	PCCR1	PDC控制寄存器1	0x004	32	read/ write	0x00000000	0xFFFFFFFF
PDC	-	-	-	PCSR	PDC状态寄存器	0x008	32	read/ write	0x00000002	0xFFFFFFFF
PDC	-	-	-	PCMONR	PDC管脚监控寄存器	0x00C	32	只读	0x00000000	0xFFFFFFFF
PDC	-	-	-	PCDR	PDC接收数据寄存器0x 010	32	只读	0x00000000	0xFFFFFFFF
PDC	-	-	-	VCR	垂直捕捉寄存器	0x014	32	read/ write	0x00000000	0xFFFFFFFF
PDC	-	-	-	HCR	水平捕捉寄存器0x 018	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	256	0x4	0-255	GR1_CLUT0[%s]	调色板0平面 图形1平面	0x0000	32	read/ write	0x00000000	0x00000000
GLCDC	256	0x4	0-255	GR1_CLUT1[%s]	调色板1平面用于 图形1平面	0x0400	32	read/ write	0x00000000	0x00000000
GLCDC	256	0x4	0-255	GR2_CLUT0[%s]	调色板0平面 图形2平面	0x0800	32	read/ write	0x00000000	0x00000000
GLCDC	256	0x4	0-255	GR2_CLUT1[%s]	调色板1平面用于 图形2平面	0x0C00	32	read/ write	0x00000000	0x00000000

Table 3.3 Register description (40 of 44)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
GLCDC	-	-	-	BG_EN	Background Plane Setting Operation Control Register	0x1000	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	-	-	-	BG_PERI	Background Plane Setting Free-Running Period Register	0x1004	32	read/ write	0x00170017	0xFFFFFFFF
GLCDC	-	-	-	BG_SYNC	Background Plane Setting Synchronization Position Register	0x1008	32	read/ write	0x00010001	0xFFFFFFFF
GLCDC	-	-	-	BG_VSIZE	Background Plane Setting Full Image Vertical Size Register	0x100C	32	read/ write	0x00070010	0xFFFFFFFF
GLCDC	-	-	-	BG_HSIZE	Background Plane Setting Full Image Horizontal Size Register	0x1010	32	read/ write	0x00060010	0xFFFFFFFF
GLCDC	-	-	-	BG_BGC	Background Plane Setting Background Color Register	0x1014	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	-	-	-	BG_MON	Background Plane Setting Status Monitor Register	0x1018	32	read-only	0x00000000	0xFFFFFFFF
GLCDC	2	0x100	1,2	GR%s_VEN	Graphics %s Register Update Control Register	0x1100	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	2	0x100	1,2	GR%s_FLMRD	Graphics %s Frame Buffer Read Control Register	0x1104	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	2	0x100	1,2	GR%s_FLM1	Graphics %s Frame Buffer Control Register 1	0x1108	32	read/ write	0x00000003	0xFFFFFFFF
GLCDC	2	0x100	1,2	GR%s_FLM2	Graphics %s Frame Buffer Control Register 2	0x110C	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	2	0x100	1,2	GR%s_FLM3	Graphics %s Frame Buffer Control Register 3	0x1110	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	2	0x100	1,2	GR%s_FLM5	Graphics %s Frame Buffer Control Register 5	0x1118	32	read/ write	0x000F0000	0xFFFFFFFF
GLCDC	2	0x100	1,2	GR%s_FLM6	Graphics %s Frame Buffer Control Register 6	0x111C	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	2	0x100	1,2	GR%s_AB1	Graphics %s Alpha Blending Control Register 1	0x1120	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	2	0x100	1,2	GR%s_AB2	Graphics %s Alpha Blending Control Register 2	0x1124	32	read/ write	0x00060010	0xFFFFFFFF
GLCDC	2	0x100	1,2	GR%s_AB3	Graphics %s Alpha Blending Control Register 3	0x1128	32	read/ write	0x00050010	0xFFFFFFFF
GLCDC	2	0x100	1,2	GR%s_AB4	Graphics %s Alpha Blending Control Register 4	0x112C	32	read/ write	0x00060010	0xFFFFFFFF
GLCDC	2	0x100	1,2	GR%s_AB5	Graphics %s Alpha Blending Control Register 5	0x1130	32	read/ write	0x00050010	0xFFFFFFFF
GLCDC	2	0x100	1,2	GR%s_AB6	Graphics %s Alpha Blending Control Register 6	0x1134	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	2	0x100	1,2	GR%s_AB7	Graphics %s Alpha Blending Control Register 7	0x1138	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	2	0x100	1,2	GR%s_AB8	Graphics %s Alpha Blending Control Register 8	0x113C	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	2	0x100	1,2	GR%s_AB9	Graphics %s Alpha Blending Control Register 9	0x1140	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	2	0x100	1,2	GR%s_BASE	Graphics %s Background Color Control Register	0x114C	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	2	0x100	1,2	GR%s_CLUTINT	Graphics %s CLUT Table Interrupt Control Register	0x1150	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	2	0x100	1,2	GR%s_MON	Graphics %s Status Monitor Register	0x1154	32	read-only	0x00000000	0xFFFFFFFF
GLCDC	3	0x40	G,B,R	GAM%s_LATCH	Gamma %s Register Update Control Register	0x1300	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	-	-	-	GAM_SW	Gamma Correction Block Function Switch Register	0x1304	32	read/ write	0x00000000	0xFFFFFFFF

Table 3.3 注册描述（40的44）

周边暗淡		昏暗的增量。	暗淡索引寄存器名称		Description	地址偏移	尺寸	访问	重置值	重置蒙版
GLCDC	-	-	-	BG_EN	后台平面设置操作控制寄存器	0x1000	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	-	-	-	BG_PERI	背景平面设置 Free-Running Period Register	0x1004	32	read/ write	0x00170017	0xFFFFFFFF
GLCDC	-	-	-	BG_SYNC	背景平面设置同步位置 Register	0x1008	32	read/ write	0x00010001	0xFFFFFFFF
GLCDC	-	-	-	BG_VSIZE	背景平面设置 完整图像垂直尺寸 Register	0x100C	32	read/ write	0x00070010	0xFFFFFFFF
GLCDC	-	-	-	BG_HSIZE	背景平面设置全图水平尺寸 Register	0x1010	32	read/ write	0x00060010	0xFFFFFFFF
GLCDC	-	-	-	BG_BGC	背景平面设置背景颜色寄存器	0x1014	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	-	-	-	BG_MON	背景平面设置 状态监控寄存器	0x1018	32	只读	0x00000000	0xFFFFFFFF
GLCDC	2	0x100	1,2	GR%s_VEN	图形%s寄存器 更新控制寄存器	0x1100	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	2	0x100	1,2	GR%s_FLMRD	图形%s帧缓冲区 读取控制寄存器	0x1104	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	2	0x100	1,2	GR%s_FLM1	图形%s帧缓冲区 控制寄存器1	0x1108	32	read/ write	0x00000003	0xFFFFFFFF
GLCDC	2	0x100	1,2	GR%s_FLM2	图形%s帧缓冲区 控制寄存器2	0x110C	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	2	0x100	1,2	GR%s_FLM3	图形%s帧缓冲区 控制寄存器3	0x1110	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	2	0x100	1,2	GR%s_FLM5	图形%s帧缓冲区 控制寄存器5	0x1118	32	read/ write	0x000F0000	0xFFFFFFFF
GLCDC	2	0x100	1,2	GR%s_FLM6	图形%s帧缓冲区 控制寄存器6	0x111C	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	2	0x100	1,2	GR%s_AB1	图形%sAlpha混合 控制寄存器1	0x1120	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	2	0x100	1,2	GR%s_AB2	图形%sAlpha混合 控制寄存器2	0x1124	32	read/ write	0x00060010	0xFFFFFFFF
GLCDC	2	0x100	1,2	GR%s_AB3	图形%sAlpha混合 控制寄存器3	0x1128	32	read/ write	0x00050010	0xFFFFFFFF
GLCDC	2	0x100	1,2	GR%s_AB4	图形%sAlpha混合 控制寄存器4	0x112C	32	read/ write	0x00060010	0xFFFFFFFF
GLCDC	2	0x100	1,2	GR%s_AB5	图形%sAlpha混合 控制寄存器5	0x1130	32	read/ write	0x00050010	0xFFFFFFFF
GLCDC	2	0x100	1,2	GR%s_AB6	图形%sAlpha混合 控制寄存器6	0x1134	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	2	0x100	1,2	GR%s_AB7	图形%sAlpha混合 控制寄存器7	0x1138	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	2	0x100	1,2	GR%s_AB8	图形%sAlpha混合 控制寄存器8	0x113C	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	2	0x100	1,2	GR%s_AB9	图形%sAlpha混合 控制寄存器9	0x1140	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	2	0x100	1,2	GR%s_BASE	图形%s背景 颜色控制寄存器	0x114C	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	2	0x100	1,2	GR%s_CLUTINT	图形%sCLUT表 中断控制寄存器	0x1150	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	2	0x100	1,2	GR%s_MON	图形%s状态监视器 Register	0x1154	32	只读	0x00000000	0xFFFFFFFF
GLCDC	3	0x40	G B R	GAM%s_LATCH	Gamma%s寄存器更新 控制寄存器	0x1300	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	-	-	-	GAM_SW	伽玛校正模块功能切换寄存器	0x1304	32	read/ write	0x00000000	0xFFFFFFFF

Table 3.3 Register description (41 of 44)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
GLCDC	3	0x40	G,B,R	GAM%s_LUT1	Gamma %s Correction Block Table Setting Register 1	0x1308	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	3	0x40	G,B,R	GAM%s_LUT2	Gamma %s Correction Block Table Setting Register 2	0x130C	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	3	0x40	G,B,R	GAM%s_LUT3	Gamma %s Correction Block Table Setting Register 3	0x1310	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	3	0x40	G,B,R	GAM%s_LUT4	Gamma %s Correction Block Table Setting Register 4	0x1314	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	3	0x40	G,B,R	GAM%s_LUT5	Gamma %s Correction Block Table Setting Register 5	0x1318	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	3	0x40	G,B,R	GAM%s_LUT6	Gamma %s Correction Block Table Setting Register 6	0x131C	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	3	0x40	G,B,R	GAM%s_LUT7	Gamma %s Correction Block Table Setting Register 7	0x1320	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	3	0x40	G,B,R	GAM%s_LUT8	Gamma %s Correction Block Table Setting Register 8	0x1324	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	3	0x40	G,B,R	GAM%s_AREA1	Gamma %s Correction Block Area Setting Register 1	0x1328	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	3	0x40	G,B,R	GAM%s_AREA2	Gamma %s Correction Block Area Setting Register 2	0x132C	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	3	0x40	G,B,R	GAM%s_AREA3	Gamma %s Correction Block Area Setting Register 3	0x1330	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	3	0x40	G,B,R	GAM%s_AREA4	Gamma %s Correction Block Area Setting Register 4	0x1334	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	3	0x40	G,B,R	GAM%s_AREA5	Gamma %s Correction Block Area Setting Register 5	0x1338	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	-	-	-	OUT_VLATCH	Output Control Block Register Update Control Register	0x13C0	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	-	-	-	OUT_SET	Output Control Block Output Interface Register	0x13C4	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	-	-	-	OUT_BRIGHT1	Output Control Block Brightness Correction Register 1	0x13C8	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	-	-	-	OUT_BRIGHT2	Output Control Block Brightness Correction Register 2	0x13CC	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	-	-	-	OUT_CONTRAST	Output Control Block Contrast Correction Register	0x13D0	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	-	-	-	OUT_PDTHA	Output Control Block Panel Dither Correction Register	0x13D4	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	-	-	-	OUT_CLKPHASE	Output Control Block Output Phase Control Register	0x13E4	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	-	-	-	TCON_TIM	TCON Reference Timing Setting Register	0x1404	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	2	0x8	A,B	TCON_STV%s1	TCON Vertical Timing Setting Register %s1	0x1408	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	2	0x8	A,B	TCON_STV%s2	TCON Vertical Timing Setting Register %s2	0x140C	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	2	0x8	A,B	TCON_STH%s1	TCON Horizontal Timing Setting Register STH%s1	0x1418	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	2	0x8	A,B	TCON_STH%s2	TCON Horizontal Timing Setting Register STH%s2	0x141C	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	-	-	-	TCON_DE	TCON Data Enable Polarity Setting Register	0x1428	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	-	-	-	SYSCNT_DTCTEN	System Control Block State Detection Control Register	0x1440	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	-	-	-	SYSCNT_INTEN	System Control Block Interrupt Request Enable Control Register	0x1444	32	read/ write	0x00000000	0xFFFFFFFF

Table 3.3 寄存器说明（41的44）

周边暗淡	Dim	昏暗的增量。	暗淡索引寄存器名称	Register name	Description	地址偏移	尺寸访问		重置值	重置蒙版
GLCDC	3	0x40	G,B,R	GAM%s_LUT1	伽玛%s校正块 表设置寄存器1	0x1308	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	3	0x40	G,B,R	GAM%s_LUT2	伽玛%s校正块 表设置寄存器2	0x130C	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	3	0x40	G,B,R	GAM%s_LUT3	伽玛%s校正块 表设置寄存器3	0x1310	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	3	0x40	G,B,R	GAM%s_LUT4	伽玛%s校正块 表设置寄存器4	0x1314	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	3	0x40	G,B,R	GAM%s_LUT5	伽玛%s校正块 表设置寄存器5	0x1318	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	3	0x40	G,B,R	GAM%s_LUT6	伽玛%s校正块 表设置寄存器6	0x131C	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	3	0x40	G,B,R	GAM%s_LUT7	伽玛%s校正块 表设置寄存器7	0x1320	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	3	0x40	G,B,R	GAM%s_LUT8	伽玛%s校正块 表设置寄存器8	0x1324	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	3	0x40	G B R	GAM%s_AREA1	Gamma%s校正块 区域设置寄存器1	0x1328	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	3	0x40	G B R	GAM%s_AREA2	Gamma%s校正块 区域设置寄存器2	0x132C	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	3	0x40	G B R	GAM%s_AREA3	Gamma%s校正块 区域设置寄存器3	0x1330	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	3	0x40	G B R	GAM%s_AREA4	Gamma%s校正块 区域设置寄存器4	0x1334	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	3	0x40	G B R	GAM%s_AREA5	Gamma%s校正块 区域设置寄存器5	0x1338	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	-	-	-	OUT_VLATCH	输出控制块 寄存器更新控制 Register	0x13C0	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	-	-	-	OUT_SET	输出控制块输出 接口寄存器	0x13C4	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	-	-	-	OUT_BRIGHT1	输出控制块亮度校正 Register 1	0x13C8	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	-	-	-	OUT_BRIGHT2	输出控制块亮度校正 Register 2	0x13CC	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	-	-	-	OUT_CONTRAST	输出控制块 对比度校正寄存器	0x13D0	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	-	-	-	OUT_PDTHA	输出控制块面板 抖动校正寄存器	0x13D4	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	-	-	-	OUT_CLKPHASE	输出控制块输出 相位控制寄存器	0x13E4	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	-	-	-	TCON_TIM	TCON参考时序 设置寄存器	0x1404	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	2	0x8	A,B	TCON_STV%s1	TCON垂直时序设置寄存器%s1	0x1408	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	2	0x8	A,B	TCON_STV%s2	TCON垂直时序设置寄存器%s2	0x140C	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	2	0x8	A,B	TCON_STH%s1	TCON水平时序设置寄存器STH%s1	0x1418	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	2	0x8	A,B	TCON_STH%s2	TCON水平时序设置寄存器STH%s2	0x141C	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	-	-	-	TCON_DE	TCON数据使能极性 设置寄存器	0x1428	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	-	-	-	SYSCNT_DTCTEN	系统控制块状态 检测控制寄存器	0x1440	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	-	-	-	SYSCNT_INTEN	系统控制块 中断请求使能 控制寄存器	0x1444	32	read/ write	0x00000000	0xFFFFFFFF

Table 3.3 Register description (42 of 44)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
GLCDC	-	-	-	SYSCNT_STCLR	System Control Block Status Clear Register	0x1448	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	-	-	-	SYSCNT_STMON	System Control Block Status Monitor Register	0x144C	32	read-only	0x00000000	0xFFFFFFFF
GLCDC	-	-	-	SYSCNT_PANEL_CLK	System Control Block Version and Panel Clock Control Register	0x1450	32	read/ write	0x01100000	0xFFFFFFFF
DRW	-	-	-	CONTROL	Geometry Control Register	0x00	32	write-only	0x00000000	0xFFFFFFFF
DRW	-	-	-	STATUS	Status Control Register	0x00	32	read-only	0x00000000	0xFFFFFFFF
DRW	-	-	-	CONTROL2	Surface Control Register	0x04	32	write-only	0x00000000	0xFFFFFFFF
DRW	-	-	-	HWREVISION	Hardware Version and Feature Set ID Register	0x04	32	read-only	0x0FBE0107	0xFFFFF000
DRW	6	0x4	1-6	L%sSTART	Limiter %s Start Value Register	0x10	32	write-only	0x00000000	0xFFFFFFFF
DRW	6	0x4	1-6	L%sXADD	Limiter %s X-Axis Increment Register	0x28	32	write-only	0x00000000	0xFFFFFFFF
DRW	6	0x4	1-6	L%sYADD	Limiter %s Y-Axis Increment Register	0x40	32	write-only	0x00000000	0xFFFFFFFF
DRW	2	0x4	1,2	L%sBAND	Limiter %s Band Width Parameter Register	0x58	32	write-only	0x00000000	0xFFFFFFFF
DRW	-	-	-	COLOR1	Base Color Register	0x64	32	write-only	0x00000000	0xFFFFFFFF
DRW	-	-	-	COLOR2	Secondary Color Register	0x68	32	write-only	0x00000000	0xFFFFFFFF
DRW	-	-	-	PATTERN	Pattern Register	0x74	32	write-only	0x00000000	0xFFFFFFFF
DRW	-	-	-	SIZE	Bounding Box Dimension Register	0x78	32	write-only	0x00000000	0xFFFFFFFF
DRW	-	-	-	PITCH	Framebuffer Pitch And Spanstore Delay Register	0x7C	32	write-only	0x00000000	0xFFFFFFFF
DRW	-	-	-	ORIGIN	Framebuffer Base Address Register	0x80	32	write-only	0x00000000	0xFFFFFFFF
DRW	-	-	-	LUSTART	U Limiter Start Value Register	0x90	32	write-only	0x00000000	0xFFFFFFFF
DRW	-	-	-	LUXADD	U Limiter X-Axis Increment Register	0x94	32	write-only	0x00000000	0xFFFFFFFF
DRW	-	-	-	LUYADD	U Limiter Y-Axis Increment Register	0x98	32	write-only	0x00000000	0xFFFFFFFF
DRW	-	-	-	LVSTARTI	V Limiter Start Value Integer Part Register	0x9C	32	write-only	0x00000000	0xFFFFFFFF
DRW	-	-	-	LVSTARTF	V Limiter Start Value Fractional Part Register	0xA0	32	write-only	0x00000000	0xFFFFFFFF
DRW	-	-	-	LVXADDI	V Limiter X-Axis Increment Integer Part Register	0xA4	32	write-only	0x00000000	0xFFFFFFFF
DRW	-	-	-	LVYADDI	V Limiter Y-Axis Increment Integer Part Register	0xA8	32	write-only	0x00000000	0xFFFFFFFF
DRW	-	-	-	LVYXADDF	V Limiter Increment Fractional Parts Register	0xAC	32	write-only	0x00000000	0xFFFFFFFF
DRW	-	-	-	TEXPITCH	Texels Per Texture Line Register	0xB4	32	write-only	0x00000000	0xFFFFFFFF
DRW	-	-	-	TEXMASK	Texture Size or Texture Address Mask Register	0xB8	32	write-only	0x00000000	0xFFFFFFFF
DRW	-	-	-	TEXORIGIN	Texture Base Address Register	0xBC	32	write-only	0x00000000	0xFFFFFFFF
DRW	-	-	-	IRQCTL	Interrupt Control Register	0xC0	32	write-only	0x00000000	0xFFFFFFFF

Table 3.3 寄存器描述（42的44）

周边暗淡		昏暗的增量。	暗淡索引寄存器名称		Description	地址偏移	尺寸	访问	重置值	重置蒙版
GLCDC	-	-	-	SYSCNT_STCLR	系统控制块状态清除注册	0x1448	32	read/ write	0x00000000	0xFFFFFFFF
GLCDC	-	-	-	SYSCNT_STMON	系统控制块状态监控寄存器	0x144C	32	只读	0x00000000	0xFFFFFFFF
GLCDC	-	-	-	SYSCNT_PANEL_CLK	系统控制块版本和面板时钟控制寄存器	0x1450	32	read/ write	0x01100000	0xFFFFFFFF
DRW	-	-	-	CONTROL	几何控制寄存器	0x00	32	只写	0x00000000	0xFFFFFFFF
DRW	-	-	-	STATUS	状态控制寄存器	0x00	32	只读	0x00000000	0xFFFFFFFF
DRW	-	-	-	CONTROL2	表面控制寄存器	0x04	32	只写	0x00000000	0xFFFFFFFF
DRW	-	-	-	HWREVISION	硬件版本和功能集ID寄存器	0x04	32	只读	0x0FBE0107	0xFFFFF000
DRW	6	0x4	1-6	L%sSTART	限制器%s起始值Register	0x10	32	只写	0x00000000	0xFFFFFFFF
DRW	6	0x4	1-6	L%sXADD	限制器%sX轴增量Register	0x28	32	只写	0x00000000	0xFFFFFFFF
DRW	6	0x4	1-6	L%sYADD	限制器%sY轴增量Register	0x40	32	只写	0x00000000	0xFFFFFFFF
DRW	2	0x4	1,2	L%sBAND	限制器%s带宽参数寄存器	0x58	32	只写	0x00000000	0xFFFFFFFF
DRW	-	-	-	COLOR1	基色寄存器	0x64	32	只写	0x00000000	0xFFFFFFFF
DRW	-	-	-	COLOR2	二次色彩套准	0x68	32	只写	0x00000000	0xFFFFFFFF
DRW	-	-	-	PATTERN	模式寄存器	0x74	32	只写	0x00000000	0xFFFFFFFF
DRW	-	-	-	SIZE	边界框尺寸Register	0x78	32	只写	0x00000000	0xFFFFFFFF
DRW	-	-	-	PITCH	帧缓冲间距和Spanstore延迟寄存器	0x7C	32	只写	0x00000000	0xFFFFFFFF
DRW	-	-	-	ORIGIN	帧缓冲基地址Register	0x80	32	只写	0x00000000	0xFFFFFFFF
DRW	-	-	-	LUSTART	U限制器起始值Register	0x90	32	只写	0x00000000	0xFFFFFFFF
DRW	-	-	-	LUXADD	U限制器X轴增量Register	0x94	32	只写	0x00000000	0xFFFFFFFF
DRW	-	-	-	LUYADD	U限制器Y轴增量Register	0x98	32	只写	0x00000000	0xFFFFFFFF
DRW	-	-	-	LVSTARTI	V限制器起始值整数零件寄存器	0x9C	32	只写	0x00000000	0xFFFFFFFF
DRW	-	-	-	LVSTARTF	V限制器起始值小数部分寄存器	0xA0	32	只写	0x00000000	0xFFFFFFFF
DRW	-	-	-	LVXADDI	V限制器X轴增量整数部分寄存器	0xA4	32	只写	0x00000000	0xFFFFFFFF
DRW	-	-	-	LVYADDI	V限制器Y轴增量整数部分寄存器	0xA8	32	只写	0x00000000	0xFFFFFFFF
DRW	-	-	-	LVYXADDF	V限制器增量小数部分寄存器	0xAC	32	只写	0x00000000	0xFFFFFFFF
DRW	-	-	-	TEXPITCH	每条纹理线的纹素Register	0xB4	32	只写	0x00000000	0xFFFFFFFF
DRW	-	-	-	TEXMASK	纹理大小或纹理地址掩码寄存器	0xB8	32	只写	0x00000000	0xFFFFFFFF
DRW	-	-	-	TEXORIGIN	纹理基地址Register	0xBC	32	只写	0x00000000	0xFFFFFFFF
DRW	-	-	-	IRQCTL	中断控制寄存器	0xC0	32	只写	0x00000000	0xFFFFFFFF

Table 3.3 Register description (43 of 44)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
DRW	-	-	-	CACHECTL	Cache Control Register	0xC4	32	write-only	0x00000000	0xFFFFFFFF
DRW	-	-	-	DLISTSTART	Display List Start Address Register	0xC8	32	write-only	0x00000000	0xFFFFFFFF
DRW	2	0x4	1,2	PERFCOUNT%s	Performance Counter %s	0xCC	32	read/write	0x00000000	0xFFFFFFFF
DRW	-	-	-	PERFTRIGGER	Performance Counters Control Register	0xD4	32	write-only	0x00000000	0xFFFFFFFF
DRW	-	-	-	TEXCLADDR	CLUT Start Address Register	0xDC	32	write-only	0x00000000	0xFFFFFFFF
DRW	-	-	-	TEXCLDATA	CLUT Data Register	0xE0	32	write-only	0x00000000	0xFFFFFFFF
DRW	-	-	-	TEXCLOFFSET	CLUT Offset Register	0xE4	32	write-only	0x00000000	0xFFFFFFFF
DRW	-	-	-	COLKEY	Color Key Register	0xE8	32	write-only	0x00000000	0xFFFFFFFF
JPEG	-	-	-	JCMOD	JPEG Code Mode Register	0x000	8	read/write	0x00	0xFF
JPEG	-	-	-	JCCMD	JPEG Code Command Register	0x001	8	write-only	0x00	0x00
JPEG	-	-	-	JCQTN	JPEG Code Quantization Table Number Register	0x003	8	read/write	0x00	0xFF
JPEG	-	-	-	JCHTN	JPEG Code Huffman Table Number Register	0x004	8	read/write	0x00	0xFF
JPEG	-	-	-	JCDRIU	JPEG Code DRI Upper Register	0x005	8	read/write	0x00	0xFF
JPEG	-	-	-	JCDRID	JPEG Code DRI Lower Register	0x006	8	read/write	0x00	0xFF
JPEG	-	-	-	JCVSZU	JPEG Code Vertical Size Upper Register	0x007	8	read/write	0x00	0xFF
JPEG	-	-	-	JCVSZD	JPEG Code Vertical Size Lower Register	0x008	8	read/write	0x00	0xFF
JPEG	-	-	-	JCHSZU	JPEG Code Horizontal Size Upper Register	0x009	8	read/write	0x00	0xFF
JPEG	-	-	-	JCHSZD	JPEG Coded Horizontal Size Lower Register	0x00A	8	read/write	0x00	0xFF
JPEG	-	-	-	JCDTCU	JPEG Code Data Count Upper Register	0x00B	8	read-only	0x00	0xFF
JPEG	-	-	-	JCDTCM	JPEG Code Data Count Middle Register	0x00C	8	read-only	0x00	0xFF
JPEG	-	-	-	JCDTCD	JPEG Code Data Count Lower Register	0x00D	8	read-only	0x00	0xFF
JPEG	-	-	-	JINTE0	JPEG Interrupt Enable Register 0	0x00E	8	read/write	0x00	0xFF
JPEG	-	-	-	JINTS0	JPEG Interrupt Status Register 0	0x00F	8	read/write	0x00	0xFF
JPEG	-	-	-	JCDERR	JPEG Code Decode Error Register	0x010	8	read/write	0x0A	0xFF
JPEG	-	-	-	JCRST	JPEG Code Reset Register	0x011	8	read-only	0x00	0xFF
JPEG	-	-	-	JIFECNT	JPEG Interface Compression Control Register	0x040	32	read/write	0x00000000	0xFFFFFFFF
JPEG	-	-	-	JIFESA	JPEG Interface Compression Source Address Register	0x044	32	read/write	0x00000000	0xFFFFFFFF
JPEG	-	-	-	JIFESOFST	JPEG Interface Compression Line Offset Register	0x048	32	read/write	0x00000000	0xFFFFFFFF

Table 3.3 注册描述（43/44）

周边暗淡		昏暗的增量。	暗淡索引寄存器名称		Description	地址偏移	尺寸	访问	重置值	重置蒙版
DRW	-	-	-	CACHECTL	高速缓存控制寄存器	0xC4	32	只写	0x00000000	0xFFFFFFFF
DRW	-	-	-	DLISTSTART	显示列表起始地址 Register	0xC8	32	只写	0x00000000	0xFFFFFFFF
DRW	2	0x4	1,2	PERFCOUNT%s	性能计数器%s	0xCC	32	read/write	0x00000000	0xFFFFFFFF
DRW	-	-	-	PERFTRIGGER	性能计数器控制寄存器	0xD4	32	只写	0x00000000	0xFFFFFFFF
DRW	-	-	-	TEXCLADDR	CLUT起始地址寄存器0x DC		32	只写	0x00000000	0xFFFFFFFF
DRW	-	-	-	TEXCLDATA	CLUT数据寄存器	0xE0	32	只写	0x00000000	0xFFFFFFFF
DRW	-	-	-	TEXCLOFFSET	CLUT偏移寄存器	0xE4	32	只写	0x00000000	0xFFFFFFFF
DRW	-	-	-	COLKEY	颜色键寄存器	0xE8	32	只写	0x00000000	0xFFFFFFFF
JPEG	-	-	-	JCMOD	JPEG代码模式寄存器	0x000	8	read/write	0x00	0xFF
JPEG	-	-	-	JCCMD	JPEG代码命令 Register	0x001	8	只写	0x00	0x00
JPEG	-	-	-	JCQTN	JPEG码量化表号寄存器	0x003	8	read/write	0x00	0xFF
JPEG	-	-	-	JCHTN	JPEG代码霍夫曼表号码寄存器	0x004	8	read/write	0x00	0xFF
JPEG	-	-	-	JCDRIU	JPEG代码DRI上 Register	0x005	8	read/write	0x00	0xFF
JPEG	-	-	-	JCDRID	JPEG代码DRI下限 Register	0x006	8	read/write	0x00	0xFF
JPEG	-	-	-	JCVSZU	JPEG代码垂直大小高位寄存器	0x007	8	read/write	0x00	0xFF
JPEG	-	-	-	JCVSZD	JPEG代码垂直大小低位寄存器	0x008	8	read/write	0x00	0xFF
JPEG	-	-	-	JCHSZU	JPEG代码水平尺寸高位寄存器	0x009	8	read/write	0x00	0xFF
JPEG	-	-	-	JCHSZD	JPEG编码水平尺寸低位寄存器	0x00A	8	read/write	0x00	0xFF
JPEG	-	-	-	JCDTCU	JPEG代码数据计数高位寄存器	0x00B	8	只读	0x00	0xFF
JPEG	-	-	-	JCDTCM	JPEG代码数据计数中间寄存器	0x00C	8	只读	0x00	0xFF
JPEG	-	-	-	JCDTCD	JPEG代码数据计数低位寄存器	0x00D	8	只读	0x00	0xFF
JPEG	-	-	-	JINTE0	JPEG中断启用 Register 0	0x00E	8	read/write	0x00	0xFF
JPEG	-	-	-	JINTS0	JPEG中断状态 Register 0	0x00F	8	read/write	0x00	0xFF
JPEG	-	-	-	JCDERR	JPEG代码解码错误 Register	0x010	8	read/write	0x0A	0xFF
JPEG	-	-	-	JCRST	JPEG代码重置寄存器	0x011	8	只读	0x00	0xFF
JPEG	-	-	-	JIFECNT	JPEG接口压缩控制 Register	0x040	32	read/write	0x00000000	0xFFFFFFFF
JPEG	-	-	-	JIFESA	JPEG接口压缩源地址寄存器	0x044	32	read/write	0x00000000	0xFFFFFFFF
JPEG	-	-	-	JIFESOFST	JPEG接口压缩线偏移 Register	0x048	32	read/write	0x00000000	0xFFFFFFFF

Table 3.3 Register description (44 of 44)

Peripheral	Dim	Dim incr.	Dim index	Register name	Description	Address offset	Size	Access	Reset value	Reset mask
JPEG	-	-	-	JIFEDA	JPEG Interface Compression Destination Address Register	0x04C	32	read/ write	0x00000000	0xFFFFFFFF
JPEG	-	-	-	JIFESLC	JPEG Interface Compression Source Line Count Register	0x050	32	read/ write	0xFFF8FFF8	0xFFFFFFFF
JPEG	-	-	-	JIFDCNT	JPEG Interface Decompression Control Register	0x058	32	read/ write	0x00000000	0xFFFFFFFF
JPEG	-	-	-	JIFDSA	JPEG Interface Decompression Source Address Register	0x05C	32	read/ write	0x00000000	0xFFFFFFFF
JPEG	-	-	-	JIFDDOFST	JPEG Interface Decompression Line Offset Register	0x060	32	read/ write	0x00000000	0xFFFFFFFF
JPEG	-	-	-	JIFDDA	JPEG Interface Decompression Destination Address Register	0x064	32	read/ write	0x00000000	0xFFFFFFFF
JPEG	-	-	-	JIFDSDC	JPEG Interface Decompression Source Data Count Register	0x068	32	read/ write	0xFFF8FFF8	0xFFFFFFFF
JPEG	-	-	-	JIFDDLC	JPEG Interface Decompression Destination Line Count Register	0x06C	32	read/ write	0xFFF8FFF8	0xFFFFFFFF
JPEG	-	-	-	JIFDADT	JPEG Interface Decompression alpha Set Register	0x070	32	read/ write	0x00000000	0xFFFFFFFF
JPEG	-	-	-	JINTE1	JPEG Interrupt Enable Register 1	0x08C	32	read/ write	0x00000000	0xFFFFFFFF
JPEG	-	-	-	JINTS1	JPEG Interrupt Status Register 1	0x090	32	read/ write	0x00000000	0xFFFFFFFF
QSPI	-	-	-	SFMSMD	Transfer Mode Control Register	0x000	32	read/ write	0x00000000	0xFFFFFFFF
QSPI	-	-	-	SFMSSC	Chip Selection Control Register	0x004	32	read/ write	0x00000037	0xFFFFFFFF
QSPI	-	-	-	SFMSKC	Clock Control Register	0x008	32	read/ write	0x00000008	0xFFFFFFFF
QSPI	-	-	-	SFMSST	Status Register	0x00C	32	read-only	0x00000080	0xFFFFFFFF
QSPI	-	-	-	SFMCOM	Communication Port Register	0x010	32	read/ write	0x00000000	0xFFFFFF00
QSPI	-	-	-	SFMCMD	Communication Mode Control Register	0x014	32	read/ write	0x00000000	0xFFFFFFFF
QSPI	-	-	-	SFMCST	Communication Status Register	0x018	32	read/ write	0x00000000	0xFFFFFFFF
QSPI	-	-	-	SFMSIC	Instruction Code Register	0x020	32	read/ write	0x00000000	0xFFFFFFFF
QSPI	-	-	-	SFMSAC	Address Mode Control Register	0x024	32	read/ write	0x00000002	0xFFFFFFFF
QSPI	-	-	-	SFMSDC	Dummy Cycle Control Register	0x028	32	read/ write	0x0000FF00	0xFFFFFFFF
QSPI	-	-	-	SFMSPC	SPI Protocol Control Register	0x030	32	read/ write	0x00000010	0xFFFFFFFF
QSPI	-	-	-	SFMPMD	Port Control Register	0x034	32	read/ write	0x00000000	0xFFFFFFFF
QSPI	-	-	-	SFMCNT1	External QSPI Address Register 1	0x804	32	read/ write	0x00000000	0xFFFFFFFF

Peripheral name = Name of peripheral
Dim = Number of elements in an array of registers
Dim inc = Address increment between two simultaneous registers of a register array in the address map

Table 3.3 寄存器说明（44的44）

周边暗淡		昏暗的增量。		暗淡索引寄存器名称	Description	地址偏移	尺寸	访问	重置值	重置蒙版
JPEG	-	-	-	JIFEDA	JPEG接口压缩目标 地址寄存器	0x04C	32	read/ write	0x00000000	0xFFFFFFFF
JPEG	-	-	-	JIFESLC	JPEG接口压缩源行 计数寄存器	0x050	32	read/ write	0xFFF8FFF8	0xFFFFFFFF
JPEG	-	-	-	JIFDCNT	JPEG接口 减压控制 Register	0x058	32	read/ write	0x00000000	0xFFFFFFFF
JPEG	-	-	-	JIFDSA	JPEG接口解压源 地址寄存器	0x05C	32	read/ write	0x00000000	0xFFFFFFFF
JPEG	-	-	-	JIFDDOFST	JPEG接口 减压线偏移 Register	0x060	32	read/ write	0x00000000	0xFFFFFFFF
JPEG	-	-	-	JIFDDA	JPEG接口解压目的地 地址寄存器	0x064	32	read/ write	0x00000000	0xFFFFFFFF
JPEG	-	-	-	JIFDSDC	JPEG接口解压源数据 计数寄存器	0x068	32	read/ write	0xFFF8FFF8	0xFFFFFFFF
JPEG	-	-	-	JIFDDLC	JPEG接口 减压目的地 行数寄存器	0x06C	32	read/ write	0xFFF8FFF8	0xFFFFFFFF
JPEG	-	-	-	JIFDADT	JPEG接口 解压alpha集 Register	0x070	32	read/ write	0x00000000	0xFFFFFFFF
JPEG	-	-	-	JINTE1	JPEG中断启用 Register 1	0x08C	32	read/ write	0x00000000	0xFFFFFFFF
JPEG	-	-	-	JINTS1	JPEG中断状态 Register 1	0x090	32	read/ write	0x00000000	0xFFFFFFFF
QSPI	-	-	-	SFMSMD	传输模式控制 Register	0x000	32	read/ write	0x00000000	0xFFFFFFFF
QSPI	-	-	-	SFMSSC	芯片选择控制 Register	0x004	32	read/ write	0x00000037	0xFFFFFFFF
QSPI	-	-	-	SFMSKC	时钟控制寄存器	0x008	32	read/ write	0x00000008	0xFFFFFFFF
QSPI	-	-	-	SFMSST	状态寄存器	0x00C	32	只读	0x00000080	0xFFFFFFFF
QSPI	-	-	-	SFMCOM	通讯端口 Register	0x010	32	read/ write	0x00000000	0xFFFFFF00
QSPI	-	-	-	SFMCMD	通讯方式 控制寄存器	0x014	32	read/ write	0x00000000	0xFFFFFFFF
QSPI	-	-	-	SFMCST	通讯状态 Register	0x018	32	read/ write	0x00000000	0xFFFFFFFF
QSPI	-	-	-	SFMSIC	指令码寄存器	0x020	32	read/ write	0x00000000	0xFFFFFFFF
QSPI	-	-	-	SFMSAC	地址模式控制 Register	0x024	32	read/ write	0x00000002	0xFFFFFFFF
QSPI	-	-	-	SFMSDC	虚拟循环控制 Register	0x028	32	read/ write	0x0000FF00	0xFFFFFFFF
QSPI	-	-	-	SFMSPC	SPI协议控制 Register	0x030	32	read/ write	0x00000010	0xFFFFFFFF
QSPI	-	-	-	SFMPMD	端口控制寄存器	0x034	32	read/ write	0x00000000	0xFFFFFFFF
QSPI	-	-	-	SFMCNT1	外部QSPI地址 Register 1	0x804	32	read/ write	0x00000000	0xFFFFFFFF

外设名称=外设名称
Dim=寄存器数组中的元素数
Diminc=地址映射中寄存器阵列的两个同时寄存器之间的地址增量

Dim index = Sub string that replaces the %s placeholder within the register name
Register name = Name of register
Description = Register description
Address offset = Address of the register relative to the base address defined by the peripheral of the register
Size = Bit width of the register
Access = Register access rights:
Read-only: Read access is permitted. Write operations have undefined results.
Write-only: Write access is permitted. Read operations have undefined results.
Read/write: Both read and write accesses are permitted. Writes affect the state of the register and reads return a value related to the register.
Reset value = Default reset value of a register
Reset mask = Identifies which register bits have a defined reset value

暗淡索引=替换寄存器名称中的%s占位符的子字符串
寄存器名称=寄存器名称描述=寄
存器描述
地址偏移量=相对于寄存器外设定义的基地址的寄存器地址
大小=寄存器的位宽
访问=注册访问权限：
只读：允许读访问。写操作有未定义的结果。只写：允许写访问。读取操作具
有未定义的结果。
读写：允许读写访问。写入会影响寄存器的状态，读取会返回与寄存器相关的值。复位值=寄存器的默认复位值

复位掩码=标识哪些寄存器位具有定义的复位值

Revision History — RA6M3 Group User's Manual

Rev.	Date	Chapter	Summary
1.00	Oct 8, 2019	—	First Edition issued
1.10	Dec 25, 2020	—	Second Edition issued
		section 1, Overview	Updated Figure 1.2, Part numbering scheme
		section 4, Address Space	Updated Figure 4.1 and Figure 4.2
		section 7, Option-Setting Memory	Updated description for HOCOEN bit
		section 9, Clock Generation Circuit	Updated description for CKSEL[2:0] bits
			Updated description for HCSTP bit, HOCOSF flag
			Updated section 9.7, Internal Clock
			Updated Figure 9.14 and Figure 9.15
		section 11, Low Power Modes	Updated Note 18. in Table 11.2, Operating conditions of each low power mode
			Updated description for OPE bit
			Updated description in Invalid register write accesses by the DTC or DMAC
		section 20, I/O Ports	Updated Table 20.2, I/O port functions and Table 20.9, Register settings for I/O pin functions (PORT2)
		section 23, General PWM Timer (GPT)	Updated section 23.2.20, General PWM Timer Compare Capture Register n (GTCCRn) (n = A to F)
			Updated Figure 23.81
			Updated section 23.3.11.6, Event Link Controller (ELC) output
		section 25, Asynchronous General-Purpose Timer (AGT)	Updated Figure 25.2
			Updated section 25.4.11, When Switching Source Clock
		section 26, Realtime Clock (RTC)	Updated section 26.6.8, When Switching Source Clock
		section 32, USB 2.0 Full-Speed Module (USBFS)	Updated description for TRNENSEL bits in section 32.2.12, SOF Output Configuration Register (SOFCFG) and section 32.2.16, NRDY Interrupt Status Register (NRDYSTS)
		section 36, I²C Bus Interface (IIC)	Updated description for NACKE bit in section 36.2.6, I²C Bus Function Enable Register (ICFER)
			Updated description for AL flag in section 36.2.10, I²C Bus Status Register 2 (ICSR2)
			Updated Figure 36.23
			Updated section 36.7.3, Device-ID Address Detection
			Updated Figure 36.28, Figure 36.39, and Figure 36.49
			Updated section 36.12.2, Extra SCL Clock Cycle Output Function
			Updated Table 36.11, Register states when issuing each condition
		section 39, Quad Serial Peripheral Interface (QSPI)	Updated the bit name for SFMMD3 in section 39.2.1, Transfer Mode Control Register (SFMSMD)
			Updated Figure 39.4, Figure 39.5, Figure 39.6 and Figure 39.7
			Updated section 39.4.2, SPI Mode
			Removed Section 39.5.9 Serial Data Receiving Latency
			Updated the Note in section 39.10.3, Generating the SPI Bus Cycle during Direct Communication
		section 46, Secure Cryptographic Engine (SCE7)	Updated Table 46.1, SCE7 specifications
			Updated Figure 46.1
		section 47, 12-Bit A/D Converter (ADC12)	Updated description in section 47.1, Overview
		section 50, High-Speed Analog Comparator (ACMPHS)	Updated section 50.5, ACMPHS Interrupts
		section 55, Flash Memory	Added section 55.3.4, Factory MCU Information Flash Root Table (FMIFRT)
			Added section 55.3.5, Unique ID Register n (UIDRn) (n = 0 to 3)
			Added section 55.3.6, Part Numbering Register n (PNRn) (n = 0 to 3)
			Added section 55.3.7, MCU Version Register (MCUVER)
		section 57, JPEG Codec (JPEG)	Updated Figure 57.7

修订记录 — RA6M3组用户手册

Rev.	Date	Chapter	Summary
1.00	Oct 8, 2019	—	第一版发行
1.10	Dec 25, 2020	—	第二版发行
		第1节，概述	更新了图1.2，零件编号方案
		第4节，地址空间	更新了图4.1和图4.2
		第7节，选项设置记忆	更新了HOCOEN位的描述
		第9节，时钟生成电路	更新了CKSEL[2:0]位的描述
			更新了HCSTP位、HOCOSF标志的描述
			更新了第9.7节，内部时钟
		更新了图9.14和图9.15第11节，低功耗模式	更新了表11.2中的注18，每种低功耗模式的工作条件
			更新了OPE位的描述
			更新了DTC或DMAC的无效寄存器写访问中的描述
		第20节，IO端口	更新了表20.2，IO端口功能和表20.9，I的寄存器设置O引脚功能(PORT2)
		第23节，通用PWM定时器(GPT)	更新了第23.2.20节，通用PWM定时器比较捕捉寄存器n(GTCCRn)（n=A到F）
			更新了图23.81
			更新了第23.3.11.6节，事件链接控制器(ELC)输出
		第25节，异步通用定时器(AGT)	更新了图25.2
			更新了第25.4.11节，切换源时钟时
		第26节，实时时钟(RTC)	更新了第26.6.8节，切换源时钟时
		第32节，USB2.0全速模块(USBFS)	更新了第32.2.12节，SOF输出配置寄存器(SOFCFG)和第32.2.16节，NRDY中断状态寄存器(NRDYSTS)中TRNENSEL位的描述
		第36节，I2C总线接口(IIC)	更新了第36.2.6节中对NACKE位的描述，I2C总线功能启用寄存器(ICFER)
			更新了第36.2.10节中AL标志的描述，I2C总线状态寄存器2(ICSR2)更新了图36.23
			更新了第36.7.3节，设备ID地址检测更新了图36.28、图36.39和图36.49
			更新了第36.12.2节，额外SCL时钟周期输出功能更新了表36.11，发出每个条件时的寄存器状态
		第39节，四路串行外设接口(QSPI)	在第39.2.1节，传输模式控制中更新了SFMMD3的位名称Register (SFMSMD)
			更新了图39.4、图39.5、图39.6和图39.7
			更新了第39.4.2节，SPI模式
			删除了第39.5.9节串行数据接收延迟
			更新了第39.10.3节中的注释，在期间生成SPI总线周期直接沟通
		第46节，安全加密引擎(SCE7)	更新了表46.1，SCE7规范
			更新了图46.1
		第47节，12位模数转换器(ADC12)	更新了第47.1节概述中的描述
		第50节，高速模拟比较器(ACMPHS)	更新了第50.5节，ACMPHS中断
		第55节，闪存	添加了第55.3.4节，工厂MCU信息闪存根表(FMIFRT)
			添加了第55.3.5节，唯一ID寄存器n(UIDRn)（n=0到3）
			添加了第55.3.6节，部件编号寄存器n(PNRn)（n=0到3）
			添加了第55.3.7节，MCU版本寄存器(MCUVER)
		第57节，JPEG编解码器(JPEG)	更新了图57.7

Rev.	Date	Chapter	Summary
1.10	Dec 25, 2020	section 60, Electrical Characteristics	Updated Note 4. and Note 5. in Table 60.16, Timing of recovery from low power modes
			Updated Figure 60.81
		section 2, Package Dimensions	Updated Figure 2.4, 144-pin LQFP
		section 3, I/O Registers	Changed the address offset of the D/A Amplifier Stabilization Wait Control Register from 0x101C to 0x001C in Table 3.3, Register description

Rev.	Date	Chapter	Summary
1.10	Dec 25, 2020	第60节，电气特性	更新了表60.16中的注4和注5，从低功耗模式恢复的时序更新了图60.81
		第2节，包装尺寸	更新了图2.4，144引脚LQFP
		第3节，IO寄存器	更改了DA放大器稳定的地址偏移 表3.3中从0x101C到0x001C的等待控制寄存器，寄存器说明

RA6M3 Group User's Manual: Hardware

Publication Date: Rev.1.10 Dec 25, 2020

Published by: Renesas Electronics Corporation

RA6M3组用户手册：硬件

Publication Date: Rev.1.10 Dec 25, 2020

Published by: 瑞萨电子公司

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